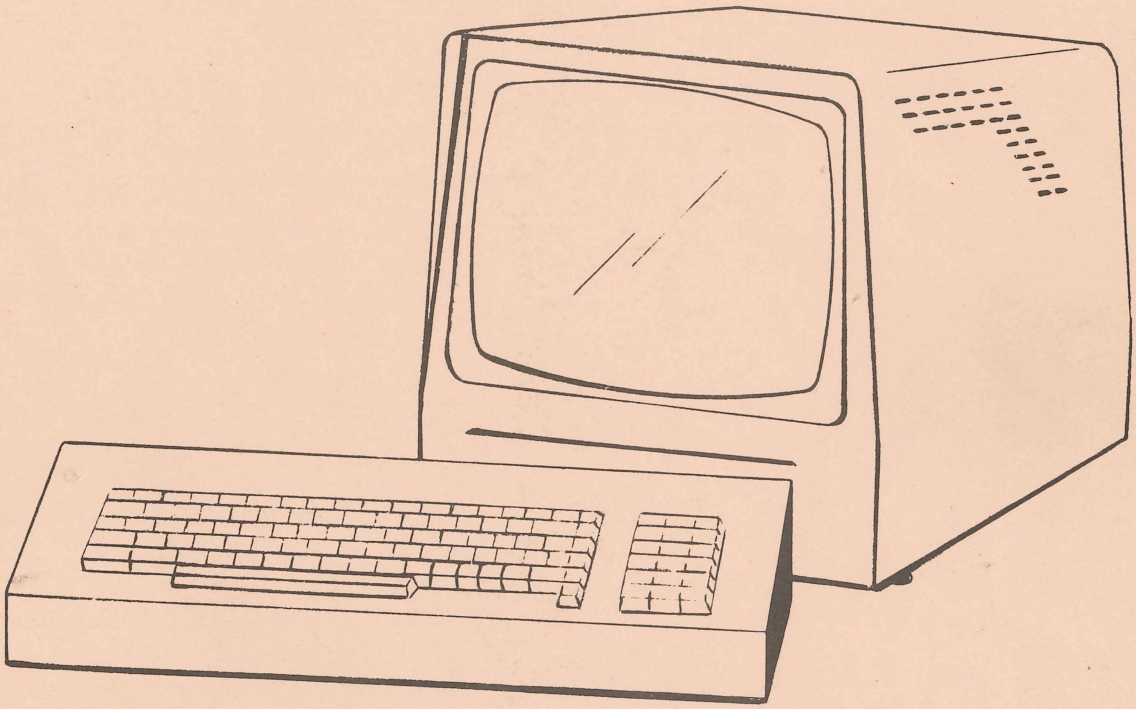
TELERAY

1000 SERIES

CRT DATA TERMINAL



REFERENCE MANUAL

RESEARCH INC
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June, 1979

KA055047

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IM927000

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Section I

SPECIFICATIONS

TELERAY MODEL 1061
SPECIFICATION

GENERAL

The Model 1061 TELERAY is a microprocessor controlled CRT terminal with a display capacity of 1920 characters (24 lines of 80 columns). It operates either Half or Full Duplex, Scroll or Page mode, and in either Character or Block transmission mode. The terminal provides text editing and formatting capability, enhanced display and protected fields, full cursor control and addressing, and cursor position readout. It also provides many programmable features (down-loadable or keyboard-loadable), including communications speeds, wide character display (24 lines x 40 columns), and 32 functions. The Modular "no tools" design enables operator replacement of malfunctioning modules.

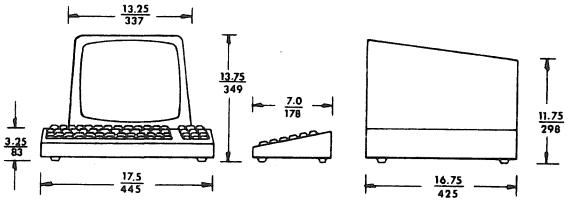
Weight: Terminal - 31-1/2 lbs. (14.3 Kg)
Keyboard - 8 lbs. (3.6 Kg)

Power: 115 or 230 VAC ±10%, 52 watts, 50 or 60 Hz.

Operating Temperature: 40° to 115°F (4° to 46°C)

Storage Temperature: -40° to 149°F (-40° to 65°C)

Relative Humidity: 10-90%, non-condensing



Dimensions in inches / mm

Modularity: Logic, power supply, keyboard and display modules accessible and replaceable without tools.

DISPLAY

Type: CRT, 12" diagonal, P4 phosphor, non-glare faceplate

Presentation: Display area - 6" High by 8½" Wide
Color - White characters on black background (inverse - internal jumper)
Format - 24 lines by 80 columns, or 24 lines by 40 columns, selectable by ESC sequence

Refresh Rate: 60 Hz (50 Hz strap selectable)

Display Character Set: Monitor mode - All 128 ASCII characters are displayed.
Normal mode - ASCII upper/lower case and numerics (95 characters) plus STX and ETX; other control characters, escape sequences and delete not displayed.
All 128 ASCII characters are generated.

Character Formation: 7 x 9 dot matrix, in 10 x 12 field

Character Size:

	Normal Mode	Wide Mode
inches:	.10 wide, .20 high	.20 wide, .20 high
mm:	2.5 wide, .5 high	.5 wide, .5 high

Cursor: Block character, blinking at 1 Hz rate.

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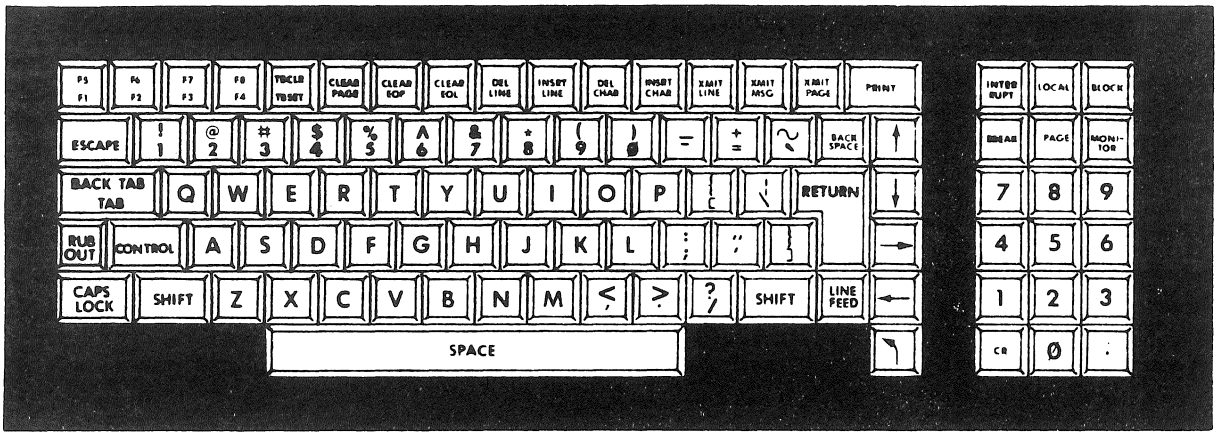
T8S103

KEYBOARD

Style: 97 key, typewriter-paired (except brackets unshifted, braces shifted), including numeric pad, cursor control pad, function, edit and transmit keys. The cursor control pad, transmit, print, clear and edit keys perform local functions only (do not transmit). European versions are optionally available.



Switches: Single-action contact switches except for five keys (Local/Remote, Block/Character, Scroll/Page, Monitor and Caps Lock) which are alternate-action switches

Rollover: N-key

Repeat: Auto-repeat at 15 characters per second when any key (except Control, Shift and Caps Lock) or combination of keys is held down longer than a half second

REAR PANEL CONTROLS AND CONNECTORS

Controls:

On/Off - power on/off switch

Contrast - display contrast potentiometer

Logic Variables - two banks of eight DIP switches each, mounted on the logic board, are accessible through an elongated hole in the rear panel. Their functions are as follows:

	UP	Switch No.	DOWN	
Right Most Switch	Display Field Modifiers	1		
	Xmit to Cursor	2	Xmit to End	**Right Block**
	Xmit an ETX	3		
	Full	4	Half Duplex	
	Wrap	5		
	New Line	6		
	New Line on CR	7	New Line on LF	
	I-Loop	8	RS-232	
	Baud 1	1		
	Baud 2	2		
	Baud 3	3		
	Baud 4	4		**Left Block**
	Even	5	ODD	
	Parity Enabled	6	No Parity	
	1 Stop Bit	7	2 Stop Bits	
Left Most Switch	7 Bits	8	8 Bits	

Connectors:

Power -Standard 3-pin (grounded) line cord connector

Serial I/O -DP25S connector, 25-pin miniature - for on-line communications interfacing in Remote mode. Pin assignments:

RS232C Standard			Current Loop (Optional)		
1	-	Protective Ground	12	-	Transmitted Data +
2	-	Transmitted Data	24	-	Transmitted Data -
3	-	Received Data	13	-	Received Data +
4	-	Request to Send	25	-	Received Data -
5	-	Clear to Send (must be asserted for Transmit)			
7	-	Signal Ground			
8	-	Carrier Detect (must be asserted for Receive)			
20	-	Data Terminal Ready			

Peripheral Interface -DP25S connector, 25-pin miniature - for interfacing with RS232 printer or other peripheral device. Pin assignments:

1	-	Protective Ground
3	-	RS232 Serial Data Out
5	-	Clear to Send (+12 V)
6	-	Data Set Ready (+12 V)
7	-	Signal Ground
8	-	Data Carrier Detect (+12 V)

Keyboard Interface -DP25P Connector, 25-pin miniature - for keyboard/terminal interconnection.

COMMUNICATIONS MODES

Character/Block Modes

In Character mode, each character code is transmitted individually as the appropriate data key is pressed; blocks may be transmitted by pressing the transmit keys.

In Block mode, keyed data goes to the TELERAY display and is only transmitted by the transmit functions.

Half/Full Duplex Modes

Full Duplex operation is used with Full Duplex type modems (Bell 103); Half Duplex mode with Half Duplex modems (Bell 202). These modes are selected by a rear panel switch.

Full Duplex Operation

When the TELERAY is in Character mode and Full Duplex mode, keyed data are transmitted; the data will not go to the TELERAY display unless the remote computer echoes it. The Serial I/O Request to Send signal is held ON in these modes. In the Block and Full Duplex modes, keyed data goes to the TELERAY display and does not go to the Serial I/O port. Keyed data is transmitted only by the transmit functions.

Half Duplex Operation

If the TELERAY is in Character mode and Half Duplex mode, a local copy is imaged on the screen as items are keyed and transmitted. The Serial I/O Request to Send signal is asserted upon initiation of keyboard data entry and negated following transmission of Line Feed or New Line code.

In the Half Duplex and Block modes, the Request to Send signal is asserted only during a block transmission. Keyed data goes only to the TELERAY display and can be transmitted only by the transmit function.

Local/Remote Modes

In Local mode the TELERAY keyboard and programmable functions are executed within the TELERAY. No data is transmitted and the Request to Send and Data Terminal Ready signals are negated. The Print function will operate in Local mode. In Remote mode these signals are determined by Full/Half Duplex mode and keyed data is transmitted as determined by the Full/Half Duplex and Character/Block modes.

COMMUNICATIONS CHARACTER MODES

One/Two Stop Bit Modes

These rear panel switch selected modes determine if one or two stop bit(s) will be appended to each transmitted character.

Parity Enable/Disable Modes

The parity Enable/Disable switch enables and disables both the parity generation and the parity checking. If parity is disabled a parity bit will not be generated and the communications character, which is transmitted, will be one bit shorter than the character transmitted when parity is enabled.

Seven/Eight Bit Modes

The 7 bits or 8 bits switch controls the length of the communications character exclusive of the parity or stop bit positions. When set to 8 bits the TELERAY will automatically put a 1 in the 8th bit position on transmission and will ignore the 8th bit on reception.

Commonly Used Communications Character Mode Settings

Parity Odd	Set to Parity ENABLE, 7 Bits, 1 or 2 Stop Bits
Parity Even	Set to Parity ENABLE, 7 Bits, 1 or 2 Stop Bits
Parity High	Set to Parity DISABLE, 8 Bits, 1 or 2 Stop Bits
No Parity	Set to Parity DISABLE, 7 Bits, 1 or 2 Stop Bits

NOTE: The combination of Parity Enable and eight bit modes should generally be avoided.

Baud Rates

The Serial I/O baud rate can be changed from the rate selected on the rear panel baud rate switches to any other of the fifteen available rates by an ESC [followed by the appropriate character shown in Table 2. Once changed, the baud rate remains fixed until it is changed again, until a Reset to Initial State sequence (ESC g) has been initiated, or until power is turned off. In the latter two cases, the rate reverts to the rate set by the rear panel switches. The peripheral baud rate can be changed to any of the other fifteen available rates by an ESC \ followed by the appropriate character shown in Table 2. Once changed, the rate remains fixed until it is changed again, or until power is turned off, in which case the rate reverts to the rate set by the rear panel switches.

OPERATING MODES

Wide/Normal Character Modes

The normal display format of the TELERAY is 24 lines of 80 characters. Receipt of an ESC m sequence will change the format to 24 lines of 40 characters (Wide mode). In Wide mode the first 40 characters of each line are expanded to twice their normal size. The display memory still contains 80 characters on each line and all wrap and cursor positioning operations will be performed accordingly. The TELERAY will remain in Wide mode until an ESC l (lower case L) or a Reset to Initial State is entered; either will return the format to 24 lines or 80 characters.

Monitor Mode

When the TELERAY is placed in this mode (via keyboard switch) all control characters including ESCAPE and Delete are treated as data, entered into the display memory, and displayed in the form shown in Table 3. This mode allows the TELERAY to be used as a line monitor and also allows entry of control characters for subsequent block transmission.

New Line Mode

This mode is selected by a rear panel switch. In New Line mode the receipt of the New Line character causes both a Carriage Return and a Line Feed to be executed by the terminal. The New Line character can be selected as either the LF character or the CR character by an additional rear panel switch. Pressing either the CR or LF key will cause the cursor to go to the first column of the next line in New Line mode. When the TELERAY is not in New Line mode, the Line Feed and Carriage Return commands are treated as separate functions.

Right Margin Wrap Mode

When this mode is selected by the rear panel switch and data is entered in the 80th column of any line, the cursor will automatically be positioned in the first column of the next line. A cursor right function from column 80 will also cause the cursor to go to the first column of the next line. This "wrap" can cause a scroll to occur or can cause the cursor to go to the top line (depending on the condition of Scroll/Page mode) if the cursor was in the 24th line.

If Right Margin Wrap mode is not selected and the cursor is in the 80th column, a cursor right function or entry of any data which moves the cursor will not advance the cursor; the cursor will remain in the 80th column and the data in that column will be rewritten.

Scroll/Page Modes

These modes are selected by the keyboard switch legended "Scroll." In Scroll mode (down position), attempts to position the cursor below the bottom line will cause all displayed data to move up one line. The top line of data is irrecoverably lost and a blank line inserted on the bottom of the displayed page. In Page mode when an attempt is made to position the cursor below the bottom line, the cursor will "wrap" to the top line. No scrolling occurs. When the TELERAY is placed in Protect mode, the TELERAY will automatically go to Page mode.

Protect Mode

The TELERAY will enter Protect mode upon receipt of an ESC W sequence and will leave Protect mode when it receives an ESC X. These sequences may come from the keyboard, a programmable function, or from the Serial I/O. The fields which are to be protected must be defined before the TELERAY is placed in Protect mode (see "Fields"). The cursor cannot be placed in protected fields nor can these fields be modified in Protect mode. All field modifier characters (within protect fields or not) are protected. The Clear functions will erase only unprotected data.

In Protect mode, scrolling, editing functions, and columnar tabs are disabled. The first nonprotected character position to the right of each protected field becomes the tab stop for tabbing operations. In Protect mode, the protected fields are not transmitted; a single FS code is substituted for them.

Keyboard Lock Mode

In the Keyboard Lock mode, all keyboard entered data are discarded. The Keyboard Lock mode is entered by an ESC b sequence from either the keyboard or the Serial I/O. The Keyboard Unlock sequence, ESC c, is accepted only from the I/O port. The Interrupt key on the keyboard may be pressed to unlock the keyboard manually. The Keyboard Lock mode is automatically entered during any extended time operation (such as Print). Upon completion of these operations the keyboard will be unlocked.

Disable/Enable Display Modes

When Disable Display mode (ESC e) is entered, subsequent data from the keyboard, or from one of the functions, or from Serial I/O port, will not go to the TELERAY display. The data will be routed to the programming area for one of the programmable functions, to the peripheral port, or to the serial port, as appropriate, but will not go to the display portion of the TELERAY. Control codes (for example: Clear Screen) will not be executed in the terminal but will be merely passed on to the appropriate point. When the Enable Display (ESC f) mode is entered, the TELERAY returns to normal. The Disable Display mode will allow the remote computer to download the functions in the TELERAY without interfering with the operator. A typical download sequence might include the following:

A. Lock keyboard (ESC b)
B. Disable display (ESC e)
C. Define function (ESC U #)
D. The message which is to be loaded into the function
E. End definition (ESC V)
F. Enable display (ESC f)
G. Enable keyboard (ESC c)

The Disable Display mode is also useful within the function programming to exclude portions or all of the function programming from going to the TELERAY screen. For example: If the functions were programmed to initiate sequences for control of the Teledisk, operator may not want these sequences to go to the display area of the TELERAY but would want to transmit them to the Teledisk. These function definitions would then contain a Disable Display in the beginning of the programming and an Enable Display in the end of the programming.

OPERATOR COMMUNICATIONS

Fields

Dim, Blink, Underline, Inverse Video and Protected fields may be established on the TELERAY in any combination. These fields are started, changed, or ended by entering a special character (field modifier) in the TELERAY memory. Any combination of field modifiers occupy only one display memory location. The field modifiers are entered in the memory using the sequence ESC R followed by the modifier code (see Table 4). All data following the field modifier in the display (until the end of the 80 character line) will have the characteristics shown in Table 4. To change or terminate a field before the end of the line, another field modifier character is entered in the memory.

Field modifiers are displayed as either a space or as a "||" depending on the position of the rear panel switch. On transmission of data in unprotected mode, a space code will be substituted for the modifiers in Protect mode, an FS (File Separator code) will be substituted for the protected field.

Undesired field modifiers can be removed using the Search and Clear modifier function (ESC S). This function will search the display in the forward direction until a field delimiter is found, will remove that modifier and position the cursor in the modifier position. In Protect mode, those modifiers in protected fields will not be removed. The search will "wrap" from the end to the beginning of the display; if no modifier is found, the cursor will be repositioned on the starting location.

Bell

An audible tone, approximately 100 msec. duration, is produced on receipt of the BEL control code from either the keyboard (Control G) or the Serial I/O interface. When keyboard entry moves the cursor past the 72nd character position in any line or into the 24th line the bell tone is also produced. Serial I/O cursor manipulation will <u>not</u> generate the tone, nor will Tab absolute cursor position, etc.

Interrupt

The Interrupt switch may be used by the operator to abort any operation currently underway and return the terminal to a ready state. When performed the interrupt will "ring" the bell; the contents of the display memory will not be changed by this function.

Break

When pressed this switch will generate a 250 msec "break" (space) signal on the Serial I/O transmitted data line. This function does not affect internal operations of the TELERAY.

Parity Error

If parity is enabled and a parity error or a framing error (stop bits missing) occurs an ASCII SUB character will be substituted for the erroneous character. The SUB character will be displayed as ^{S}B.

PROGRAMMABLE FUNCTIONS

The TELERAY contains 32 programmable functions. Any ASCII sequence may be assigned to these functions; 527 characters of memory are available to be used by the functions in any combination. The functions can be used to store forms, control sequences, answerback messages. A function should not call itself or call another function. Functions can be initiated by an appropriate ESC sequence (see below); the first eight also can be initiated by keyboard keys assigned to them. Other keyboard arrangements with additional keys assigned to these functions are available, consult factory for details.

Use of the Programmable Functions

The functions will be initiated by either the appropriate keys on the keyboard (first 8) or may be initiated by 3-character sequence - ESC T followed by the function number. The function number must be a two digit number from 01 through 32, inclusive. Both digits must be used (e.g., 01, 02, etc.) If an illegal or undefined function number is given the sequence will be ignored. When a function is initiated, the ASCII sequence stored in the function memory is treated by the TELERAY as a keyboard input. Control characters and ESC sequences will be executed and/or transmitted as determined by the operating modes.

Programming the Programmable Functions

Programming of the functions will be initiated by the sequence ESC U, followed by function number. The programming of any function will be terminated by the sequence ESC then V. If the definition sequence is given for a function which has been previously defined, the old program will be discarded and a new one entered. As the functions are being programmed, the program data will also be executed. For example: if the program sequence contains a Clear Page function the screen will be cleared.

PERIPHERAL INTERFACE

The peripheral port provides an RS232 serial asynchronous interface for a printer or other peripheral device. Following a peripheral-on command (DC2) from the keyboard or the I/O interface, data are transmitted to the peripheral port as received or as entered on the keyboard. The peripheral baud rate will be set to the I/O baud rate, either as set by rear panel switches or as changed by ESC sequence (Table 2), for concurrent printing. A peripheral-off command (DC4) will turn off the peripheral interface.

Any displayed data can also be transmitted to the peripheral port in "block" fashion by pressing the Print key. All data, including protected fields (with space characters substituted for field delimiters), are transmitted at the peripheral baud rate.

TRANSMITS AND BUFFERING

Partial Line: With the rear panel switch in the Xmit to Cursor position, the Transmit Line function transmits the data from the start of line to the cursor position.

Line: With the rear panel switch in the Xmit to End position, the Transmit Line function transmits the line the cursor is on.

Message: With the cursor positioned at the end of the message to be transmitted, the Transmit message function transmits the data from the first ETX preceding the cursor (or Home), to the cursor position. An ETX (displayed as "E_X" but not transmitted) is entered at the cursor position before transmission.

Partial Page: With the rear panel switch in the Xmit to Cursor position. the Transmit Page function transmits the data from Home to the cursor position.

Full Page: With the rear panel switch in the Transmit to End position, the Xmit Page function transmits the entire page.

These transmissions can be initiated by ESC followed by i, l, or Z for line, message or page, respectively or by the Xmit Line, Xmit Msg and Xmit Page keys. During these transmissions the keyboard is locked and the cursor scans the transmitted data. When transmission is completed, the cursor returns to its original position except after a Transmit Message the cursor is placed in the character position immediately following the ETX which was entered. Non-written spaces to the right of any data on each

line are suppressed. LF and CR, or New Line codes are appended to the end of each line as selected by the New Line and NL on LF-NL on CR switches. An ETX code will or will not be appended to each transmission as selected by the position of the rear panel ETX on Transmit switch. Any Control characters or ESC sequences entered in the display while the TELERAY was in MONITOR mode will be transmitted (but not executed).

Buffering

Block transmission from the Teleray can be suspended by a DC3 from a sending device. A DC1 code will cause transmission to resume. Block transmission is aborted if any character, number or control code precedes the resume command. A Busy/Ready mode can be selected to permit the Teleray to suspend data entry from a computer equipped to detect and decode the proper commands. The mode is enabled in the Teleray when an ESC h command is received. When this mode is enabled the Teleray sends a DC3 command (Busy) when its input buffer is 10 characters from full. When the Teleray buffer is 10 characters from empty a DC1 (Ready) command is sent to the computer to resume data transmission. Once enabled this mode can only be disabled by an ESC g (reset to initial state) command or if power to the Teleray is shut off.

CURSOR MANIPULATION

Basic Moves

The cursor can be moved one position up, down, right, left or to home (line one, column one), using either the non transmitting keyboard keys or by using the sequence: ESC and A, B, C, D or H respectively. Backspace will move the cursor one left; the space character one character to the right (destructively). Line Feed moves the cursor one down; Carriage Return places the cursor on the left margin (also, see New Line mode).

Margin Wraps

When a cursor left function is initiated with the cursor in the first column, the cursor will move to the 80th column of the preceding line (assuming the 80th column of that line is not protected). When a cursor left function is initiated with the cursor in the Home position, the cursor moves to the 80th column of the 24th line. A one up function in the top line, will position the cursor in the same column, Line 24. The actions taken on the right and bottom margins depend on the condition of the WRAP and SCROLL modes as previously described.

Cursor Address Write and Read

The cursor can be moved directly to any line-column coordinate using the sequence ESCape Y - line code - column code. The sequence ESC a will cause the TELERAY to transmit its cursor position in that order. The line code and column code for each position is given in Table 1. An illegal coordinate in an addressing sequence will be ignored; this allows the cursor to be moved to another line without changing the column or to another column without changing the line.

Tabs

The TELERAY accommodates a total of 16 columnar tab stops. A columnar tab stop can be set in any column position by moving the cursor to that position and pressing the Tab Set key, or by the sequence ESC F. Any existing tab stop can be cleared by moving the cursor to that position and pressing the Tab Clear (shifted Tab Set) key. The Clear Tabs function (ESC G) clears all Tab Stops simultaneously. Tab stops do not occupy display positions.

When the Tab/Back Tab key is pressed, the cursor moves forward or backward, respectively, to the next tab stop (which movement may include right or left margin wrap, as appropriate). In Protect mode, the columnar tabs are ignored and the character position to the right of each protected field acts as a tab stop. If no tab stops have been set the cursor will not move.

CLEARS AND EDITS

Clear Functions

The Clear EOL function clears from the cursor to the end of the line; Clear EOP function clears from the cursor to the end of the page. The Clear Page function clears the entire page. Reset to Initial State will abort any operation underway and place the TELERAY in the "power up" state: memory is clear, tab stops are removed, peripheral is disabled and cursor is at home. These functions are initiated by ESC K for Clear EOL and ESC J for Clear EOP. Clear Page is initiated by ESC j or by Form Feed; Reset to Initial State by ESC g. The Clear EOL, EOP and Page functions do not erase protected fields in Protect mode, Reset to Initial State will erase them in any mode.

Edit Functions

The Insert Character, Delete Character, Insert Line, and Delete Line functions are initiated by the sequences ESC then P, Q, L or M, respectively, or are initiated by the appropriate keyboard key. An

Insert Character function is performed by shifting all data in and to the right of the cursor on the cursor line one character to the right. Data shifted past column 80 is irrevocably lost; subsequent lines are not affected. The cursor position is not changed. The Delete Character function is performed by shifting all data in and to the right of the cursor position on the cursor line one character to the left. A space character is placed in column 80; subsequent lines are not affected. The cursor position is not changed.

The TELERAY performs an Insert Line function by shifting all data lines including and below the cursor line, one line down. A line of spaces is written in the cursor line and the cursor is positioned at the left margin on this line. Data shifted past line 24 is irrevocably lost. A Delete Line function is performed by moving all the data below the cursor line up one line. The cursor is positioned at the left margin on the current line. A line of spaces is written in line 24.

The Insert and Delete functions will not operate when the TELERAY is in Protect mode.

Table I

CURSOR COORDINATE POSITIONING

1) Press ESC . . . then Y . . .

2) then Line Code . . . 3) then Column Code

LINE CODES		COLUMN CODES					
Line No.	Char.	Col. No.	Char.	Col. No.	Char.	Col. No.	Char.
1	Space	1	Space	28	;	55	V
2	!	2	!	29	<	56	W
3	"	3	"	30	=	57	X
4	#	4	#	31	>	58	Y
5	$	5	$	32	?	59	Z
6	%	6	%	33	@	60	[
7	&	7	&	34	A	61	\
8	'	8	'	35	B	62	]
9	(	9	(	36	C	63	^
10	)	10	)	37	D	64	_
11	*	11	*	38	E	65	`
12	+	12	+	39	F	66	a
13	,	13	,	40	G	67	b
14	-	14	-	41	H	68	c
15	.	15	.	42	I	69	d
16	/	16	/	43	J	70	e
17	0	17	0	44	K	71	f
18	1	18	1	45	L	72	g
19	2	19	2	46	M	73	h
20	3	20	3	47	N	74	i
21	4	21	4	48	O	75	j
22	5	22	5	49	P	76	k
23	6	23	6	50	Q	77	l
24	7	24	7	51	R	78	m
		25	8	52	S	79	n
		26	9	53	T	80	o
		27	:	54	U		

Note: Any undefined coordinate character will be ignored.

FUNCTIONAL SUMMARY

Communications Modes

- Character/Block ..... Keyboard Switch
- Half/Full Duplex ..... Rear Panel Switch
- Local/Remote ..... Keyboard Switch

Communications Character Modes

- One/Two Stop Bit ..... Rear Panel Switch
- Parity Enable/Disable ..... Rear Panel Switch
- Seven/Eight Bit ..... Rear Panel Switch
- Baud Rates ..... Rear Panel Switch or ESC [Table 1

Operating Modes

- Wide/Normal Characters ..... ESC m / ESC l
- Monitor ..... Keyboard Switch
- New Line ..... Rear Panel Switches
- Right Margin Wrap ..... Rear Panel Switch
- Scroll/Page ..... Keyboard Switch
- Enter/Leave Protect ..... ESC W / ESC X
- Keyboard Lock/Unlock ..... ESC b / ESC c
- Disable/Enable Display ..... ESC e /ESC f

Operator Communications

- Fields ..... ESC R and Table 2
- Search & Clear Delimiter ..... ESC S
- Bell ..... BEL (CTRL G)
- Interrupt ..... Keyboard Switch
- Break ..... Keyboard Switch
- Parity Error ..... Automatic ^{S}B display

Programmable Functions

- Execute Programmed Function ..... ESC T Number (2 digit, 01 through 32)
- Define Function ..... ESC U Number (2 digit, 01 through 32)
- End Function Definition ..... ESC V

Peripheral Interface

- Print ..... Keyboard Switch or ESC O (oh)
- Peripheral On ..... DC2 (CTRL R)
- Peripheral Off ..... DC4 (CTRL T)
- Change Peripheral Baud ..... ESC \ Table 1

Transmits and Buffering

- Line ..... Keyboard Switch or ESC i
- Message ..... Keyboard Switch or ESC I
- Page ..... Keyboard Switch or ESC Z
- Xmit to Cursor/End ..... Rear Panel Switch
- Xmit an ETX ..... Rear Panel Switch
- Time Fill ..... NUL
- Suspend/Busy ..... DC3 (CTRL S)
- Resume/Ready ..... DC1 (CTRL Q)
- Enable Busy/Ready ..... ESC h

Cursor Manipulation

- One Up ..... Keyboard Switch or ESC A
- One Down ..... Keyboard Switch or ESC B or LF (CTRL J)
- One Right ..... Keyboard Switch or ESC C or Space
- One Left ..... Keyboard Switch or ESC D or BS (CTRL H)
- Home ..... Keyboard Switch or ESC H
- Left Margin ..... CR (see New Line)
- Absolute Position ..... ESC Y Table 4
- Position Read ..... ESC a
- Tab Set ..... Keyboard Switch or ESC F
- Clear This Tab ..... Keyboard Switch
- Clear All Tabs ..... ESC G
- Tab ..... Keyboard Switch or HT (CTRL I)
- Back Tab ..... Keyboard Switch or ESC d

Clears and Edits

- Clear EOL ..... Keyboard Switch or ESC K
- Clear EOP ..... Keyboard Switch or ESC J
- Clear Page ..... Keyboard Switch or j or FF (CTRL L)
- Reset to Initial State ..... ESC g
- Insert Character ..... Keyboard Switch or ESC P
- Delete Character ..... Keyboard Switch or ESC Q
- Insert Line ..... Keyboard Switch or ESC L
- Delete Line ..... Keyboard Switch or ESC M

Table 2 Baud Rate

Program Sequence Serial I/O: ESC [then / Peripheral ESC \ then	Baud Rate	Rear Panel Switch Positions 4	3	2	1
0	50	U	U	U	U
1	75	D	U	U	U
2	110	U	D	U	U
3	134.5	D	D	U	U
4	150	U	U	D	U
5	300	D	U	D	U
6	600	U	D	D	U
7	1200	D	D	D	U
8	1800	U	U	U	D
9	2000	D	U	U	D
:	2400	U	D	U	D
;	3600	D	D	U	D
<	4800	U	U	D	D
=	7200	D	U	D	D
>	9600	U	D	D	D
?	Res	D	D	D	D

U = Up
D = Down

Table 4 Field Modifiers

ESC R Then	Field Characteristics
@	Normal (ends all others)
A	Blink
B	Dim
C	Dim, Blink
D	Inverse
E	Inverse, Blink
F	Inverse, Dim
G	Inverse, Dim, Blink
H	Underline
I	Underline, Blink
J	Underline, Dim
K	Underline, Dim, Blink
L	Underline, Inverse
M	Underline, Inverse, Blink
N	Underline, Inverse, Dim
O	Underline, Inverse, Dim, Blink
P	Protect Only
Q	Protect Blink
R	Protect, Dim
S	Protect, Dim, Blink
T	Protect, Inverse
U	Protect, Inverse, Blink
V	Protect, Inverse, Dim
W	Protect, Inverse, Dim, Blink
X	Protect, Underline
Y	Protect, Underline, Blink
Z	Protect, Underline, Dim
[	Protect, Underline, Dim, Blink
\	Protect, Underline, Inverse
]	Protect, Underline, Inverse, Blink
^	Protect, Underline, Inverse, Dim
_	Protect, Underline, Inverse, Dim, Blink

Table 3 Control Character Generation and Monitor Mode Display

Displayed As	Control Character	Press* Control &
A_K	ACK	F
B_L	BEL	G
B_S	BS	H
C_N	CAN	X
C_R	CR	M
D_1	DC1	Q
D_2	DC2	R
D_3	DC3	S
D_4	DC4	T
D_L	DLE	P
E_M	EM	Y
E_Q	ENQ	E
E_T	EOT	D
E_C	ESC	[
E_B	ETB	W
E_X	ETX	C
F_F	FF	L
F_S	FS	:
G_S	GS	]
H_T	HT	I
L_F	LF	J
N_K	NAK	U
N_U	NUL	2
R_S	RS	\
S_I	SI	O
S_O	SO	N
S_H	SOH	A
S_X	STX	B
S_B	SUB	Z
S_Y	SYN	V
U_S	US	?
V_T	VT	K

*Dedicated keys on keyboard for several of these codes. See Keyboard description.

CODING SUMMARY

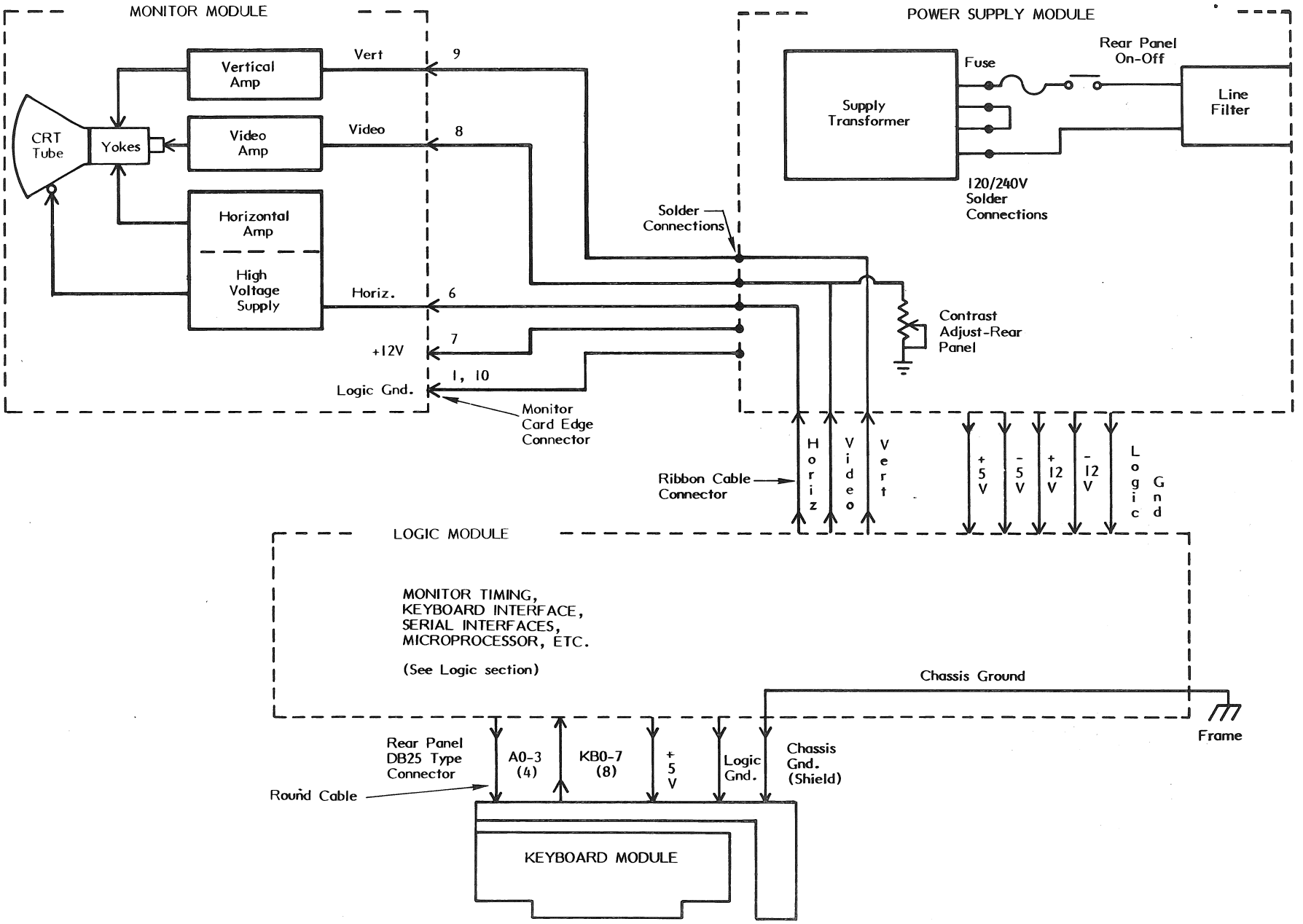
Row \ COL	Control Characters 0	Control Characters 1	Escape Sequences 4	Escape Sequences 5	Escape Sequences 6
0	NUL "Time Fill"	DLE	@	P Insert Char	
1	SOH	DC1 Resume/ Ready	A One Up	Q Delete Character	a Table 4 Read Cursor Posn.
2	STX Limit Transmit	DC2 Peripheral On	B One Down	R Table 2 Field Modifier	b Lock Keyboard
3	ETX	DC3 Suspend/ Busy	C One Right	S Search/Clr. Modifier	c Unlock Keyboard
4	EOT	DC4 Peripheral Off	D One Left	T Execute Programmed Function	d Back Tab
5	ENQ	NAK	E Clear Tab Stop	U Define Function	e Disable Display
6	ACK	SYN	F Set Tab Stop	V End Function Definition	f Enable Display
7	BEL Bell	ETB	G Clear All Tab Stops	W Enable Protect	g Reset to Initial State
8	BS One Left	CAN	H Home	X Leave Protect	h Enable Ready/Busy
9	HI Tab	EM	I Transmit Message	Y Table 4 Load Cursor Position	i Transmit Line
10	LF Line Feed	SUB Parity Error	J Clear to EOP	Z Transmit Page	j Clear Page
11	VT	ESC Introduce Sequence	K Clear to EOL	[Table 1 Set I/O Baud	k
12	FF Clear Page	FS	L Insert Line	/ Table 1 Set Periph Baud	l Normal Character Format
13	CR Cursor Return	GS	M Delete Line	]	m Wide Character Format
14	SO	RS	N	^	n
15	SI	US	O Print	-	o

Section 2

MACHINE ORGANIZATION

The Teleray consists of a display cabinet and an optional detached keyboard module. The display cabinet contains a Monitor module, Power Supply module and Logic module. These modules are accessible without using tools for exchange and/or repair. The Teleray instruction manual graphically illustrates module replacement.

The Module Signal Flow and Cabling Diagram describes the signal flow between modules. All connectors used are keyed to prevent incorrect insertion. The ribbon cable used is symmetrical, the cable may be reversed end-to-end. Pin numbers on the cables are provided in each section.



MODULE SIGNAL FLOW AND CABLING DIAGRAM

Section 3

MONITOR MODULE

Zenith DTI

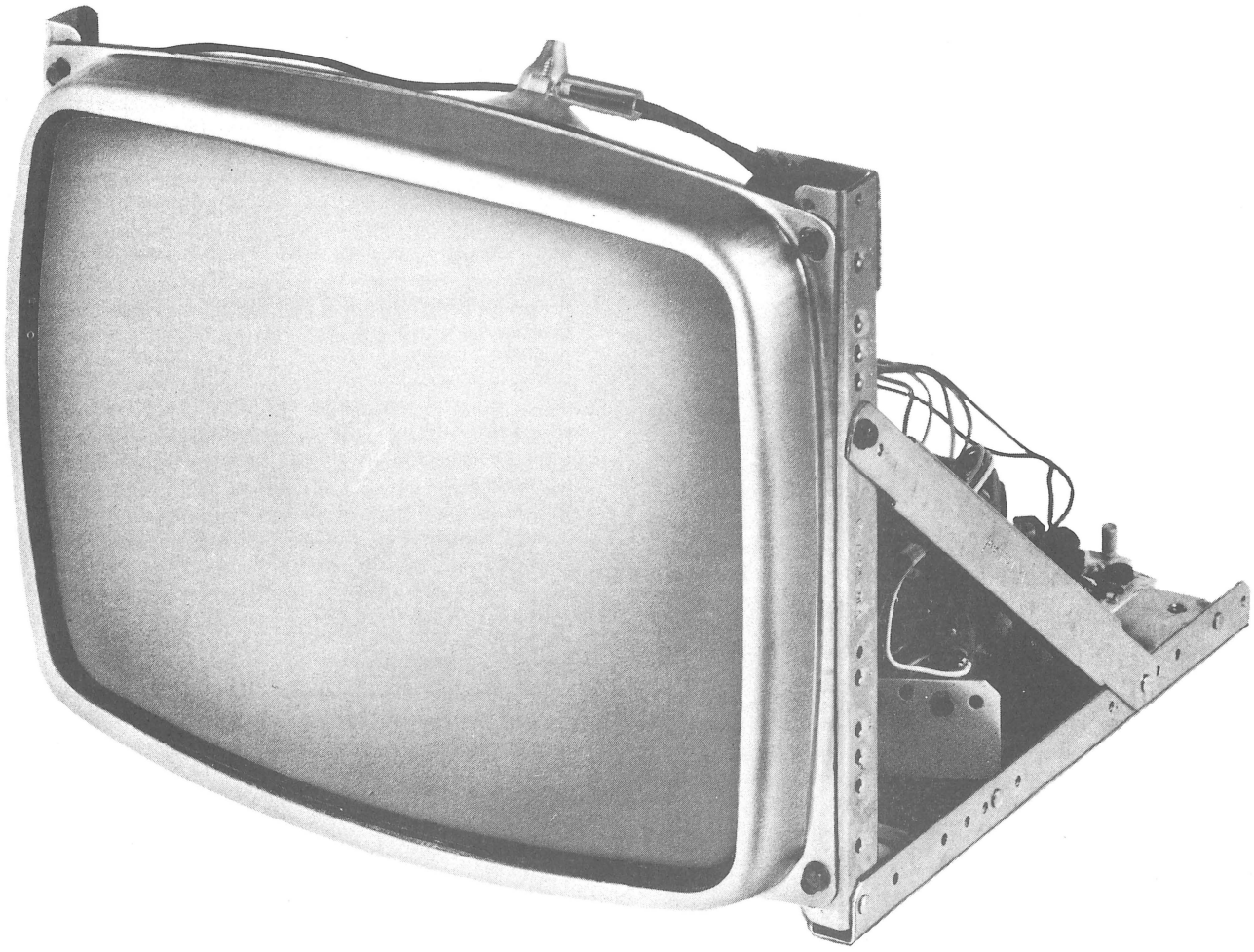
- Servicing Guidelines
- Theory of Operation
- Adjustments
- Schematics
- Parts Lists

DT1

DT1

ZENITH®

SERVICE MANUAL



DT1

D12 SERIES DATA DISPLAY TERMINALS

ZENITH RADIO CORPORATION

1000 MILWAUKEE AVENUE, GLENVIEW, ILLINOIS 60025

DT-1
5CRR

PRINTED IN U.S.A.
NOV., 1978

$2.00
923-924

PRODUCT SAFETY SERVICING GUIDELINES FOR ZENITH DATA DISPLAY TERMINALS

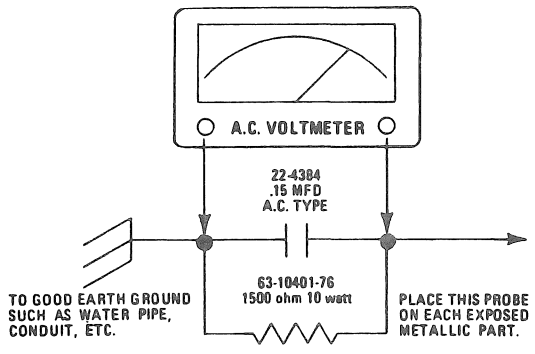
CAUTION: No modification of any circuit should be attempted. Service work should be performed only after you are thoroughly familiar with all of the following safety checks and servicing guidelines. To do otherwise increases the risk of potential hazards and injury to the user.

SAFETY CHECKS

After the original service problem has been corrected, a check should be made of the following:

SUBJECT: FIRE & SHOCK HAZARD

1. Be sure that all components are positioned in such a way to avoid possibility of adjacent component shorts. This is especially important on those chassis which are transported to and from the repair shop.
2. Never release a repair unless all protective devices such as insulators, barriers, covers, shields, strain reliefs, and other hardware have been reinstalled per original design.
3. Soldering must be inspected to uncover possible cold solder joints, frayed leads, damaged insulation, solder splashes or sharp solder points. Be certain to remove all loose foreign material.
4. Check "across-the-line" capacitor (if used) and other components for physical evidence of damage or deterioration and replace if necessary. Follow original layout, lead length and dress.
5. No lead or component should touch a resistor rated at 1 watt or more. Lead tension around protruding metal surfaces must be avoided.
6. All critical components (shaded on the schematic diagram and parts lists) such as: fuses, flameproof resistors, capacitors, etc., must be replaced with exact Zenith types. Do not use replacement components other than those specified or make unrecommended circuit modifications.
7. After re-assembly of the terminal always perform an AC leakage test on all exposed metallic parts of the cabinet and screws to be sure the terminal is safe to operate without danger of electrical shock. DO NOT USE A LINE ISOLATION TRANSFORMER DURING THIS TEST. Use an AC voltmeter having 5000 ohms per volt or more sensitivity in the following manner: Connect a 1500 ohm 10 watt resistor (63-10401-76), paralleled by a 0.15 mfd., 150V AC type capacitor (22-4384) between a known good earth ground (water pipe, conduit, etc.) and the exposed metallic parts, one at a time. Measure the AC voltage across the combination 1500 ohm resistor and 0.15 mfd. capacitor. Reverse the AC plug and repeat AC voltage measurements for each exposed metallic part. Voltage measured must not exceed 0.75 volts RMS. This corresponds to 0.5 milliamp AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.



SUBJECT: IMPLOSION PROTECTION

1. All Zenith picture tubes are equipped with an integral implosion protection system, but care should be taken to avoid damage during installation. Avoid scratching the tube.
2. Use only Zenith replacement tubes.

SUBJECT: X-RADIATION

1. Be sure procedures and instructions to all service personnel cover the subject of X-radiation. The only potential source of X-rays is the picture tube. However, this tube does not emit X-rays when the HV is at the factory-specified level. It is only when the HV is excessive that X-radiation can be generated. The basic precaution which must be exercised is to keep the HV at the factory-recommended level. Refer to the X-ray Precaution Label which is located inside each terminal for the correct high voltage. The proper value is also given in the schematic diagram. Operation at higher voltages may cause a failure of the picture tube or high voltage supply and, also, under certain circumstances, may produce radiation in excess of desirable levels.
2. Only Zenith-specified CRT anode connectors must be used.
3. It is essential that the serviceman has available at all times an accurate high voltage meter. The calibration of this meter should be checked periodically against a reference standard.
4. When the high voltage circuitry is operating properly there is no possibility of an X-radiation problem. Every time a chassis is serviced, the brightness should be run up and down while monitoring the high voltage with a meter to be certain that the high voltage does not exceed the specified value and that it is regulating correctly. We suggest that you and your service organization review test procedures so that voltage regulation is always checked as a standard servicing procedure, and that the reason for this prudent routine be clearly understood by everyone.
5. When trouble shooting and making test measurements in a terminal with a problem of excessive high voltage, do not operate the chassis longer than is necessary to locate the cause of excessive voltage.

IMPORTANT NOTE: DAG GROUNDING.

Each unit provides for grounding of the main P.C. Board and CRT socket board to the dag of the CRT through the dag grounding spring.

The ground wires are connected to the shell bond or T-band through a terminal lug. Upon installing the Video Display in a terminal, this grounding procedure should be followed to provide adequate high voltage filtering and arc protection. This especially pertains to mounting the video display as a kit version.

CAUTION

NO WORK SHOULD BE ATTEMPTED ON ANY EXPOSED MONITOR CHASSIS BY ANYONE NOT FAMILIAR WITH SERVICING PROCEDURES AND PRECAUTIONS.

GENERAL INFORMATION

This service manual introduces the Zenith D12 series of Video Displays. The series includes three basic forms: the D12-PF which is complete with power supply and frame, the D12-NF without power supply, the D12-NK in kit form which comes without frame or power supply.

The D12 series incorporate precision CRT's which provide uniformity of display and controlled spot size and geometry. The display may be operated from a standard 15 volt D.C. supply (or optional 12 V.D.C.) or from 120 volts A.C.

Input and output connections for the displays are made through a 10 pin edge connector on the main circuit board. Provision has been made for an optional remote brightness control. Schematic reference numbers are printed on the circuit board to aid in the location and identification of components for servicing.

Vertical and horizontal linearity is maintained within specifications without the use of linearity controls or adjustable devices. Excellent vertical linearity is assured by the extensive use of current feedback and horizontal linearity is achieved with a fixed saturable reactor.

Vertical and horizontal deflection systems sustain scan even in the absence or interruption of synchronizing signals. Vertical and horizontal synchronization is automatic and stable throughout the entire specified operating frequency range.

SPECIFICATIONS

CATHODE RAY TUBE

12'' diagonal measure, 90° deflection, 12.5 KV nominal high voltage at 50 μA. beam current. Available with bonded anti-reflective face plate option. P4 phosphor is standard and other EIA phosphors are available.

NOMINAL DISPLAY AREA

51 sq. in. defined by a rectangle 8½"x6" centered on the CRT. (Other display dimensions optional.)

INPUT SIGNALS (TTL LEVEL)

HORIZONTAL
4 to 40 μsec. duration (positive going standard).
VERTICAL
50 to 1400 μsec. duration (negative going standard).
VIDEO
1.0V to 2.5V P-P (user supplies 500 ohm contrast control for higher input levels).
Positive polarity for white characters. (Other polarities are available for horizontal and vertical sync.)

POWER SUPPLY

120V ± 10% or 240V ± 10%
(customer strappable) 47 to 63 Hz., or
15V DC at 800 ma. max., or
12V DC at 1100 ma. max.

BRIGHTNESS CONTROL

Internal or Customer supplied 100 KΩ potentiometer (accessible at pins 2, 3 and 4 of edge connector).

INTERCONNECT TO CUSTOMER SYSTEM

Via standard 10-pin edge connector.
VIKING #25V10S/1-2
AMP #225-21031-101
CINCH #250-10-30-170

RESOLUTION

900 vertical lines minimum at center of display and 700 vertical lines at the corners. Pulse rise time less than 20 nanoseconds, for 30V rise at CRT. Bandwidth is within 3db from 10 Hz. to 18 MHz.

GEOMETRY

NOTE: Measurements made with an input of 1.0-2.5V P-P and with the display adjusted to 6" highx8½" wide.
VERTICAL
a. Height of display at left side shall be within ± 2.0 percent of height at right side.
b. Top and bottom pincushion or barrel shall be within 1.25% of the average height.

HORIZONTAL
a. Width of display at top shall be within ± 2.5 percent of width at bottom.
b. Side pincushion or barrel shall be within 1.0% of the average width.

LINEARITY

No character shall vary in width or height by more than ± 10% of the average width or height of all the characters in a row or column respectively. No specific character shall vary in width or height more than ± 10% of an adjacent character.

SYNCHRONIZATION

HORIZONTAL
15.75 ± 0.5KHz.
18.60 ± 0.5KHz. (Optional)
Horizontal Blanking
10.0 μ sec. min.
Horizontal Phasing Control
10.0 μ sec. min. adjustment
VERTICAL
47 to 63 Hz.
VERTICAL RETRACE TIME
850 μ sec. max.

STORAGE

55° C. max. with bonded anti-reflective faceplate.
65° C. max. for plain faced CRT's.

ENVIRONMENT

Operating temperature
55° max. (free air temperature of display electronics).
Altitude
40,000 ft. + storage & shipment.
10,000 ft. max. operating.

WEIGHT

11.5 lbs. max. without optional power supply.
13.5 lbs. max. with optional power supply.
9.0 lbs. max. without frame.

THEORY OF OPERATION

POWER SUPPLY

Power Transformer TX201 is designed for use with 120V or 240V A.C. source. The secondary provides power to bridge rectifier (CR501, CR502, CR503 and CR504). The positive output of the bridge rectifier (junction of CR503 and CR504), forms the raw B+ supply (~ 20VDC).

Voltage regulation is accomplished in the negative leg of the power supply through a feedback network consisting of transistors QX501 and QX502 and their associated circuitry. The emitter voltage of QX501 is maintained by diodes CR505, CR506 and CR507. The base voltage is provided by potentiometer RX506.

If B+ increases, diodes CR505, CR506 and CR507 will draw more current to maintain the emitter voltage of QX501. Additionally, the voltage developed across RX506 will increase, resulting in a higher positive voltage at the base of QX501 which will result in less conduction. This reduces the base current of QX502 since QX501 provides the emitter/base current path for QX502. When QX502 conducts less, the voltage drop across Q502 is increased thus lowering B+.

If B+ decreases, diodes CR505, CR506 and CR507 will reduce conduction to maintain the emitter voltage of QX501. Additionally, the base voltage provided by RX506 will decrease. Less voltage on the base of QX501 will cause it to increase conduction, resulting in a greater emitter/base current flow in QX502. With this condition the voltage drop for Q502 is less and B+ is increased.

HORIZONTAL

The low-level horizontal section, which consists of transistors Q101 and Q102 (and associated circuitry), functions as a variable time delay monostable multivibrator. The input trigger for this circuit is provided by the horizontal drive pulse. The pulse is injected into the base or emitter (for either positive or negative pulse respectively) of Q101 through injection network C101, C111, R101, R110 and CR101. By varying the recovery time of the multivibrator, potentiometer R104 adjusts video information position (with respect to raster scan). Output of the monostable multivibrator, derived at the collector of Q102, is injected through a coupling network consisting of C110 and CR103. The resulting "Lock" signal is rereceived by one side of a precision astable multivibrator at the emitter of Q103. The astable multivibrator circuit is completed through Q104 and associated circuitry. This circuit will act as a free running oscillator until the "Lock" signal is received from the previous stage. Once locked, an output pulse is formed at the emitter of Q104 which is then D.C. coupled to the base of the horizontal driver transistor, Q105.

Remainder of the horizontal circuit is straightforward. Features to be noted are: Width and Linearity Coils LX102 and LX101 in series with the yoke (TX202). Linearity is fixed and an adjustable coil is provided for width. The linearity coil has a magnetically biased core which makes the inductance of the coil dependent upon its current. Pincushion and geometric corrections are made at the factory by the addition of rubber magnets around the plastic ring of the yoke. D.C. operation of 12 volts is accomplished by the (optional) addition of a boost circuit at the horizontal sweep transformer.

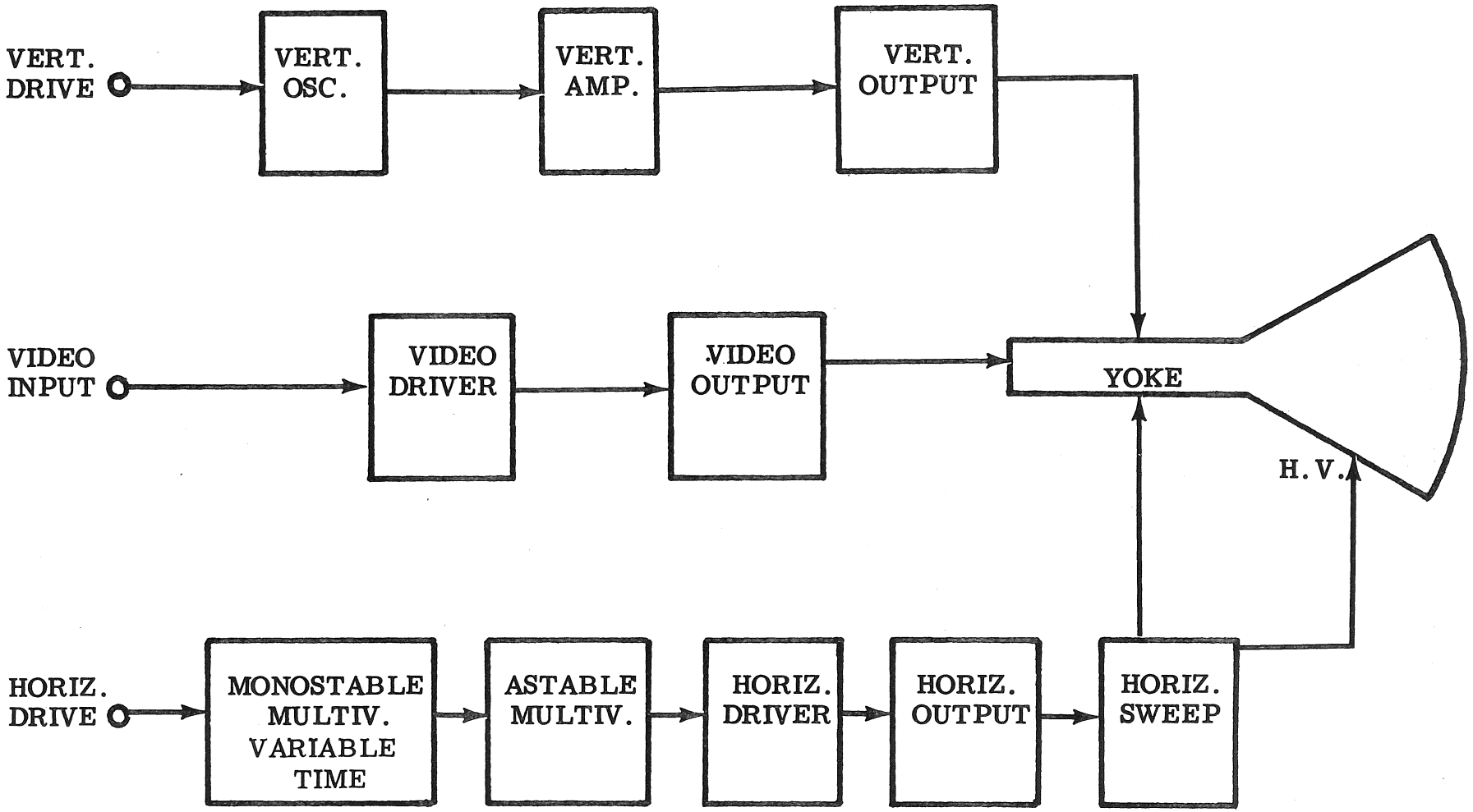
VERTICAL

The vertical circuit includes an oscillator consisting of transistors Q301 and Q302 and associated circuitry. Amplification is provided by transistors Q303 and Q304 with the emitter of Q304 feeding the base of the vertical driver Q305. The vertical output transistors, Q306 and Q307 are wired in the standard push-pull configuration. One feature of this vertical circuit is the addition of transistor Q308. This transistor doubles B+ during retrace, thus maintaining less than 800μ sec. of retrace time.

VIDEO

The video amplifier circuit consists of transistors Q401 and Q402 and associated circuitry. The circuit comprises a cascode amplifier which is triggered by a positive pulse at pin 8 of the edge connector. Upon receiving the input pulse, conduction is initiated and the collector voltage of Q402 is lowered. Amplification of low frequency voltage gain is fixed by the ratio of R407 and R408. Gain is maintained to 18 MHz by the bandwidth enhancing components R406, C403, and L401. Resistors R402 and R403 provide bias for the amplifier.

The collector output of Q401 is D.C. coupled to the cathode of the C.R.T. through resistor R201. Raster cut-off is adjusted with the brightness control R114 which is connected to G1 of the C.R.T.

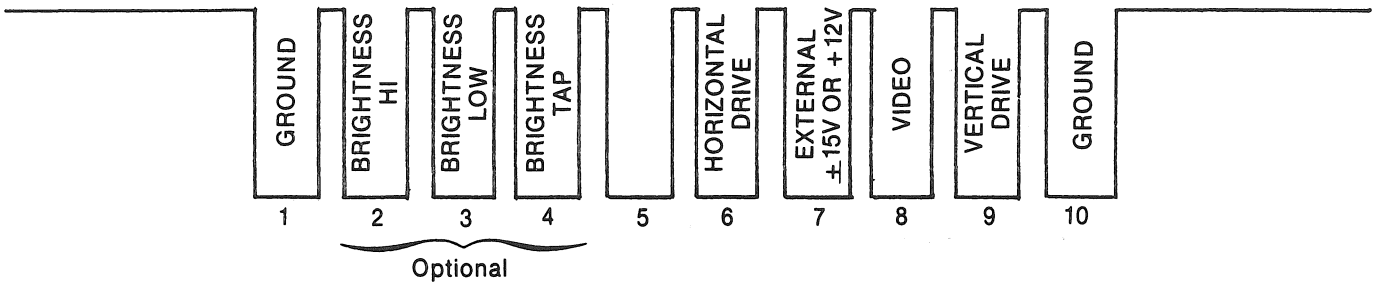

VERT.
DRIVE
VERT.
OSC.
VERT.
AMP.
VERT.
OUTPUT
VIDEO
INPUT
VIDEO
DRIVER
VIDEO
OUTPUT
YOKE
H.V.
HORIZ.
DRIVE
MONOSTABLE
MULTIV.
VARIABLE
TIME
ASTABLE
MULTIV.
HORIZ.
DRIVER
HORIZ.
OUTPUT
HORIZ.
SWEEP

ADJUSTMENT PROCEDURES FOR D12 VIDEO DISPLAY

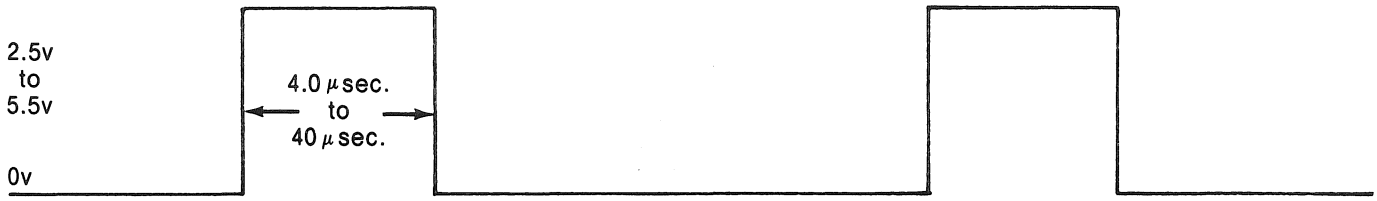
1. External power is applied to the monitor through an AC line cord or a 4 pin molex connector. The unit is wired for 120 VAC 50/60 Hz operation. (240 VAC 50/60 Hz optional)

2. INPUT SIGNALS: Input signals are connected to the display board through a 10 pin edge connector.

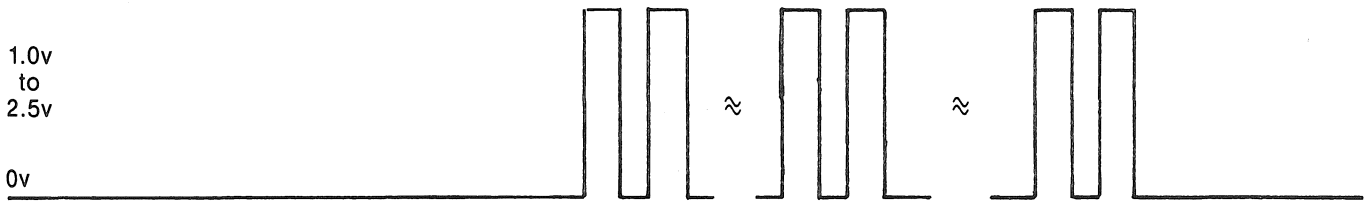
Component Side of Display Board



A. Horizontal drive signal — 15750 Hz ± 500 Hz

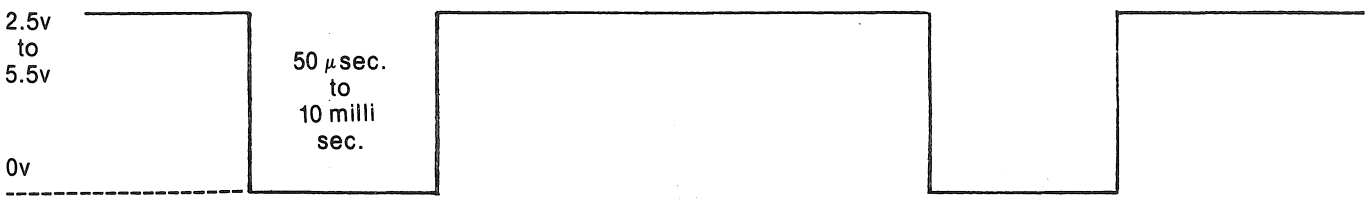


B. Video drive signal



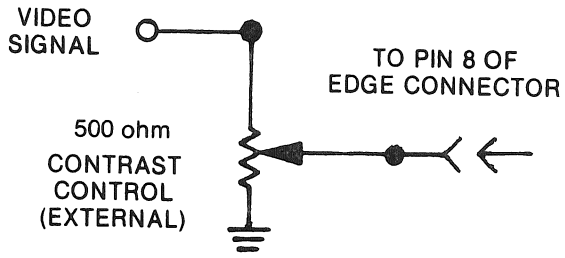
At a horizontal frequency of 15.7KHZ the video drive signal should start 11 microseconds ±5 μ sec. after the leading edge of horizontal sync, and 900 microseconds or greater after the leading edge of vertical sync.

C. Vertical drive signal — 47 Hz to 63 Hz



In normal operation the horizontal and vertical drive signals and signal ground are connected to the edge connector through a cable assembly. If this is not the case connect pins 1 & 10 together with a jumper wire at the edge connector.

Should the video drive level exceed the 2.5 volts specified, an external contrast control must be provided. The video drive signal is connected to the top end of the 500Ω pot, the bottom end is grounded and the wiper arm connects to the video input of the edge connector as shown.



3. Once power is applied to the display and the input signals connected, adjust the brightness control until the edges of the raster are visible.

4. Depending on the requirements for height and width of the video presentation, the vertical size control and width coil should be adjusted accordingly.

5. The power supply board also has a control to adjust the regulated B+ of the monitor to +15V. Check for proper adjustment.

6. Adjust the phase control to center the video information within the raster. (The contrast control may have to be adjusted to obtain a display of the video information.)

7. Adjust brightness control for visual cutoff of the raster.

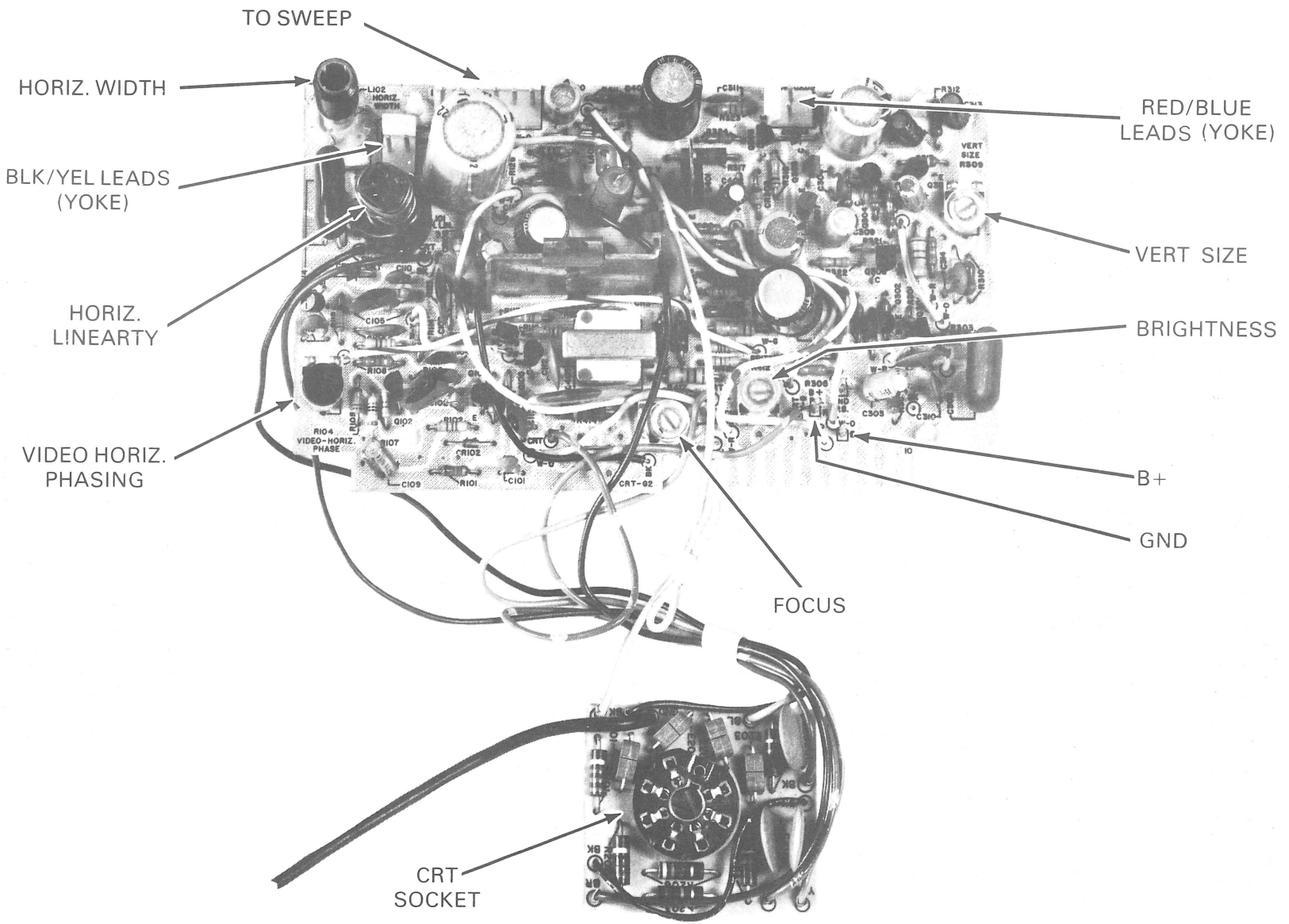
8. Adjust external contrast control for desired luminance.

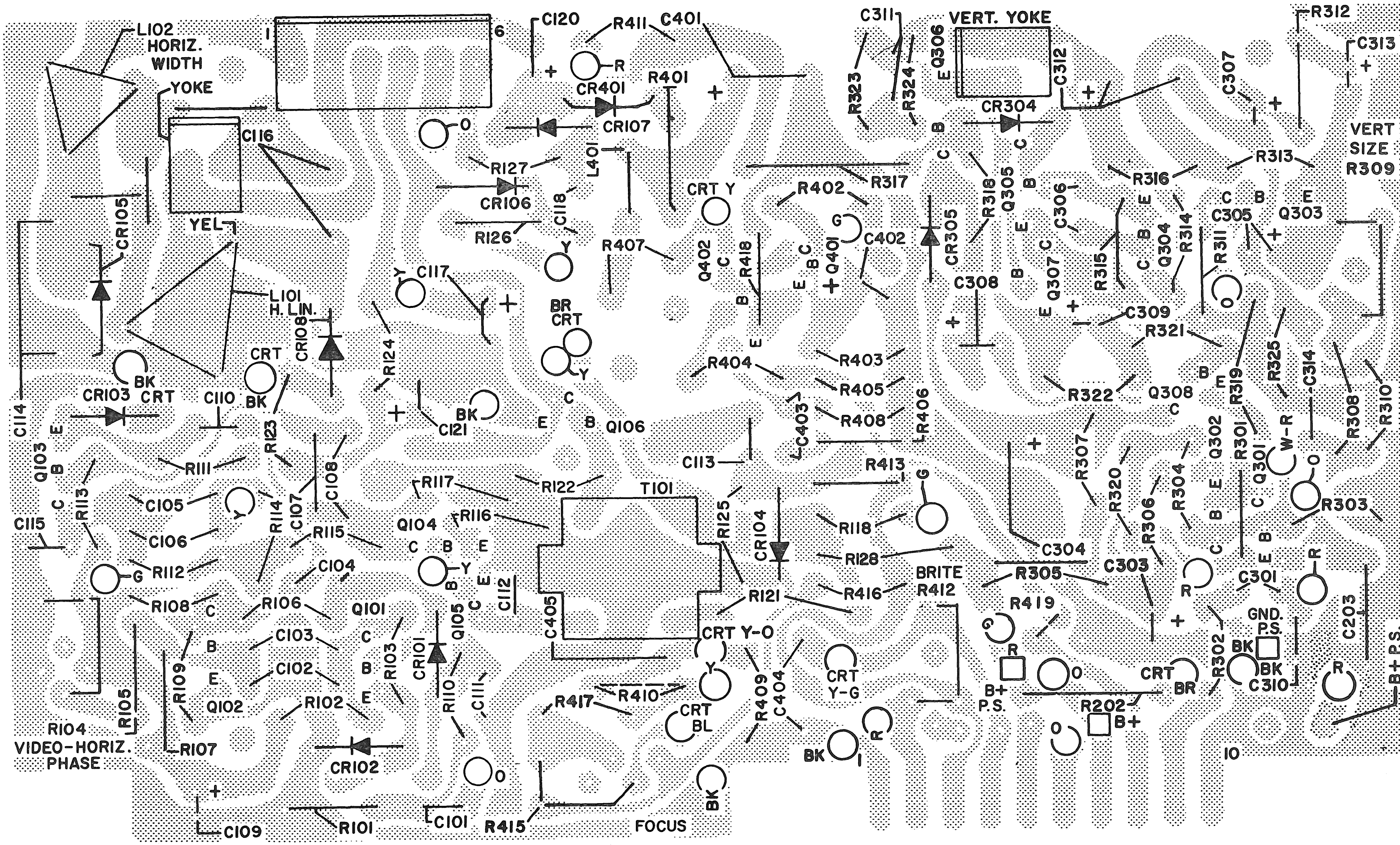
9. Adjust focus control for best possible overall focus.

IMPORTANT NOTE: DAG GROUNDING.

Each unit provides for grounding of the main P.C. Board and CRT socket board to the dag of the CRT through the dag grounding spring.

The ground wires are connected to the shell bond or T-band through a terminal lug. Upon installing the Video Display in a terminal, this grounding procedure should be followed to provide adequate high voltage filtering and arc protection. This especially pertains to mounting the video display as a kit version.

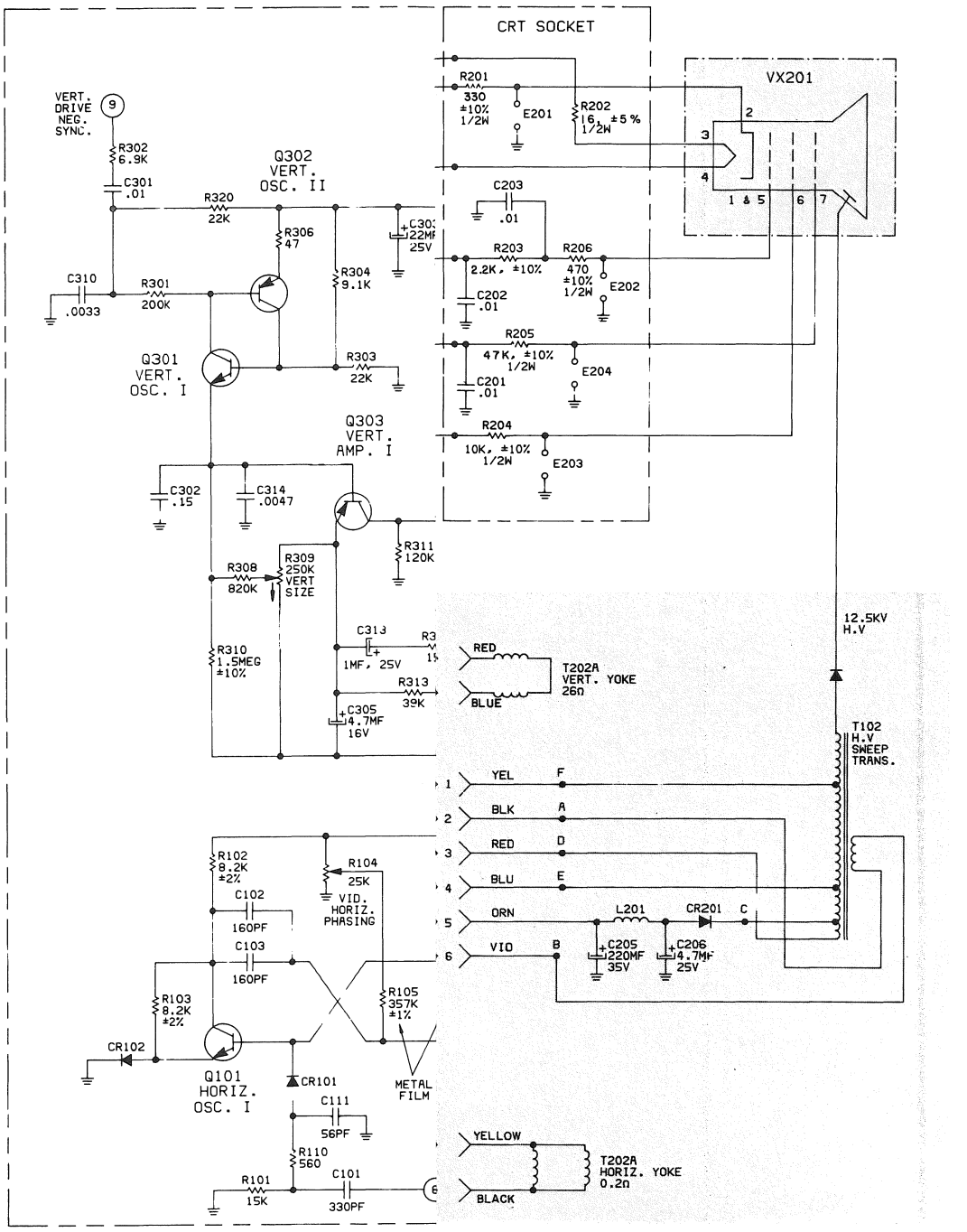

TO SWEEP
HORIZ. WIDTH
BLK/YEL LEADS (YOKE)
HORIZ. LINEARTY
VIDEO HORIZ. PHASING
RED/BLUE LEADS (YOKE)
VERT SIZE
BRIGHTNESS
B+
GND
FOCUS
CRT SOCKET

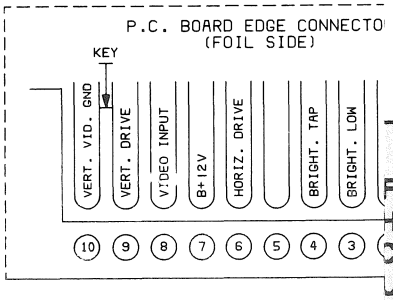

L102 HORIZ. WIDTH
YOKE
YEL
L101 H. LIN.
CR105
CR103
CRT
BK
C114
Q103
C115
R104 VIDEO-HORIZ. PHASE
R105
R107
C109
R101
C101
R415
FOCUS
CR102
Q102
Q101
R102
C102
C103
R106
R108
R109
R112
R113
C105
C106
R111
R114
C107
C108
R115
C104
R123
C110
C116
CR108
R124
+
C121
C117
R117
R116
Q104
Q105
CR101
R110
C111
R103
C112
C120
R411
C401
CR401
R401
CR107
R127
CR106
R126
C118
L401
R407
BR CRT
Q106
R122
T101
C405
R417
R410
CRT BL
CRT Y-O
R409
C404
CRT Y-G
R125
CR104
R121
C113
CRT Y
Q402
R418
Q401
R402
R317
C402
R404
R403
R405
R408
R406
C403
R413
R118
R128
R416
BRITE R412
R419
B+ P.S.
R202
B+
C311
R323
R324
Q306
VERT. YOKE
C312
CR304
CR305
R318
Q305
C308
Q307
C306
C304
R305
C303
R316
R315
Q304
R314
C309
R321
R322
Q308
R307
R320
R306
R304
Q302
R301
Q301
W-R
C301
R311
R319
R325
C314
C307
R312
C313
R313
VERT SIZE R309
C305
Q303
R308
R310
R303
R302
C310
GND. P.S.
C203
B+ P.S.
10

LEGEND

ITEM NO.	PART NO.	DESCRIPTION
C101	22-7614-06A	330 PFD CAPACITOR 20% DISC 50V
C102	22-7619-39A	160 PFD CAPACITOR 5% DISC NPO 50V
C103	22-7619-39A	160 PFD CAPACITOR 5% DISC NPO 50V
C104	22-7622-28A	56 PFD CAPACITOR 10% DISC NPO 50V
C105	22-7619-39A	160 PFD CAPACITOR 5% DISC NPO 50V
C106	22-7619-39A	160 PFD CAPACITOR 5% DISC NPO 50V
C107	22-7619-39A	160 PFD CAPACITOR 5% DISC NPO 50V
C108	22-7619-39A	160 PFD CAPACITOR 5% DISC NPO 50V
C109	22-7152-03	4.7 MFD CAPACITOR +100%—10% ELEC 25V
C110	22-7613A	100 PFD CAPACITOR 10% DISC 50V
C111	22-7622-28A	56 PFD CAPACITOR 10% DISC 50V
C112	22-7613-24A	.01 MFD CAPACITOR 10% DISC 50V
C113	22-7440	.0047 MFD CAPACITOR 10% DISC 500V
CX114	22-7530-07	.015 MFD CAPACITOR 5% POLYESTER 400V
C115	22-7656-13A	22 PFD CAPACITOR 10% DISC 50V
C116	22-7313	10 MFD CAPACITOR 20% NP ELEC 25V
C117	22-7718-09	100 MFD CAPACITOR 20% ELEC 25V
CX118	22-3748	.001 MFD CAPACITOR 10% DISC 1KV
C119		
C120	22-7722-02	2.2 MFD CAPACITOR 20% ELEC 100V
C121	22-7722-01	1 MFD CAPACITOR 20% ELEC 100V
C201	22-4905-01	.01 MFD CAPACITOR +80%—20% 500V
C202	22-4905-01	.01 MFD CAPACITOR +80%—20% 500V
C203	22-4905-01	.01 MFD CAPACITOR +80%—20% 500V
C204		
CX205	22-7144-09	220 MFD CAPACITOR +100%—10% ELEC 35V
CX206	22-7142-03	4.7 MFD CAPACITOR +100%—10% ELEC 25V
C301	22-7613-24A	.01 MFD CAPACITOR 10% DISC 50V
C302	22-7548	.15 MFD CAPACITOR 10% POLYESTER 50V
C303	22-7152-05	22 MFD CAPACITOR +100%—10% ELEC 25V
C304	22-7720-09	100 MFD CAPACITOR 20% ELEC 50V
C305	22-7579-03	4.7 MFD CAPACITOR ELEC 16V
C306	22-7614-04A	220 PFD CAPACITOR 20% DISC 50V
C307	22-7389-02	1 MFD CAPACITOR 20% ELEC 25V
C308	22-7718-08	47 MFD CAPACITOR 20% ELEC 25V
C309	22-7152-04	10 MFD CAPACITOR +100%—10% ELEC 25V
C310	22-7614-18A	.0033 MFD CAPACITOR 20% DISC 50V
C311	22-7615-08A	.022 MFD CAPACITOR +80%—20% DISC 50V
C312	22-7579-04	1000 MFD CAPACITOR 10% ELEC 16V
C313	22-7389-02	1 MFD CAPACITOR 20% ELEC 25V
C314	22-7614-20A	.0047 MFD CAPACITOR 20% DISC 50V
C315		
C401	22-7722-08	47 MFD CAPACITOR 20% ELEC 100V
C402	22-7721-04	4.7 MFD CAPACITOR 20% ELEC 63V
C403	22-7613A	100 PFD CAPACITOR 10% DISC 50V
C404	22-7724	.02 MFD CAPACITOR +80%—20% DISC 500V
C405	22-3512	.01 MFD CAPACITOR +40%—10% DISC 1KV
R101	63-9922	15K OHM RESISTOR 5% FILM 1/4W
R102	63-9919-94	8.2K OHM RESISTOR 2% FILM 1/4W
R103	63-9919-94	8.2K OHM RESISTOR 2% FILM 1/4W
R104	63-10651-06	CONTROL 25K OHM (HORIZ PHASE)
R105	63-10533-05	357K OHM RESISTOR 1% METAL FILM 1/4W
R106	63-9922-14	56K OHM RESISTOR 5% FILM 1/4W
R107	63-10533-04	267K OHM RESISTOR 1% METAL FILM 1/4W
R108	63-9921-94	8.2K OHM RESISTOR 5% FILM 1/4W
R109	63-9921-94	8.2K OHM RESISTOR 5% FILM 1/4W
R110	63-9921-66	560 OHM RESISTOR 5% FILM 1/4W
R111	63-9919-96	10K OHM RESISTOR 2% FILM 1/4W
R112	63-9919-92	6.8K OHM RESISTOR 2% FILM 1/4W
R113	63-10533-04	267K OHM RESISTOR 1% METAL FILM 1/4W
R114	63-10533-04	267K OHM RESISTOR 1% METAL FILM 1/4W
R115	63-9919-84	3.3K OHM RESISTOR 2% FILM 1/4W
R116	63-9921-79	2K OHM RESISTOR 5% FILM 1/4W
R117	63-9919-86	3.9K OHM RESISTOR 2% FILM 1/4W
RX118	63-10559-48	100 OHM RESISTOR 5% FILM 1/4W
R119		
R120		
RX121	63-10565-24	10 OHM RESISTOR 5% FILM 1/2W
R122	63-9921-46	82 OHM RESISTOR 5% FILM 1/4W
RX123	63-10559-40	47 OHM RESISTOR 5% FILM 1/4W
RX124	63-10559-68	680 OHM RESISTOR 5% FILM 1/4W
R125	63-9922-44	1 MEGOHM RESISTOR 5% FILM 1/4W
R126	63-9922-20	100K OHM RESISTOR 5% FILM 1/4W
RX127		
RX128	63-10565	1 OHM RESISTOR 5% FILM 1/2W
R201	63-7763	330 OHM RESISTOR 5% CARBON COMP 1/2W
R202	63-7710	16 OHM RESISTOR 5% CARBON COMP 1/2W
R203	63-7799	2.2K OHM RESISTOR 10% CARBON COMP 1/2W
R204	63-7827	10K OHM RESISTOR 10% CARBON COMP 1/2W
R205	63-7855	47K OHM RESISTOR 10% CARBON COMP 1/2W
R206	63-7771	470 OHM RESISTOR 10% CARBON COMP 1/2W
R301	63-9922-27	200K OHM RESISTOR 5% FILM 1/4W
R302	63-9921-92	6.8K OHM RESISTOR 5% FILM 1/4W

ITEM NO.	PART NO.	DESCRIPTION
R303	63-9922-04	22K OHM RESISTOR 5% FILM 1/4W
R304	63-9921-95	9.1K OHM RESISTOR 5% FILM 1/4W
R305	63-9922-10	39K OHM RESISTOR 5% FILM 1/4W
R306	63-9921-40	47 OHM RESISTOR 5% FILM 1/4W
RX307	63-10559-36	33 OHM RESISTOR 5% FILM 1/4W
R308	63-9922-42	820K OHM RESISTOR 5% FILM 1/4W
R309	63-10651-08	CONTROL 250K OHM VERT SIZE
R310	63-9924-48	1.5 MEGOHM RESISTOR 10% FILM 1/4W
R311	63-9922-22	120K OHM RESISTOR 5% FILM 1/4W
R312	63-9922	15K OHM RESISTOR 5% FILM 1/4W
R313	63-9922-10	39K OHM RESISTOR 5% FILM 1/4W
R314	63-9921-78	1.8K OHM RESISTOR 5% FILM 1/4W
R315	63-9922	15K OHM RESISTOR 5% FILM 1/4W
R316	63-9921-69	750 OHM RESISTOR 5% FILM 1/4W
R317	63-7816	5.6K OHM RESISTOR 5% CARBON COMP 1/2W
R318		
RX319	63-10565-56	220 OHM RESISTOR 5% FILM 1/2W
R320	63-9922-04	22K OHM RESISTOR 5% FILM 1/4W
R321	63-9921-45	75 OHM RESISTOR 5% FILM 1/4W
R322	63-9921-84	3.3K OHM RESISTOR 5% FILM 1/4W
R323	63-9921-70	820 OHM RESISTOR 5% FILM 1/4W
R324	63-9921-44	68 OHM RESISTOR 5% FILM 1/4W
R325	63-9921-10	2.7 OHM RESISTOR 5% FILM 1/4W
R401		
R402	63-9921-72	1K OHM RESISTOR 5% FILM 1/4W
R403	63-9921-72	1K OHM RESISTOR 5% FILM 1/4W
R404	63-9921-40	47 OHM RESISTOR 5% FILM 1/4W
R405	63-9921-98	12K OHM RESISTOR 5% FILM 1/4W
R406	63-9921-32	22 OHM RESISTOR 5% FILM 1/4W
R407	63-10371-70	820 OHM RESISTOR 5% FILM 2W
R408	63-9921-40	47 OHM RESISTOR 5% FILM 1/4W
R409		
R410		
R411	63-9922-04	22K OHM RESISTOR 5% FILM 1/4W
R412	63-10651-05	CONTROL 100K OHM BRIGHTNESS
R413	63-9922-04	22K OHM RESISTOR 5% FILM 1/4W
R414	63-7952	10 MEGOHM RESISTOR 5% CARBON 1/2W
R415	63-10651-07	CONTROL 2 MEGOHM FOCUS
R416	63-9922-18	82K OHM RESISTOR 5% FILM 1/4W
R417	63-9922-40	680K OHM RESISTOR 5% FILM 1/4W
R418	63-9922	15K OHM RESISTOR 5% FILM 1/4W
R419		
L101	20-3906	COIL, RCF LINEARITY
LX102	20-3882	COIL, RCF TUNABLE WIDTH
LX201	20-3824	COIL, HORIZ FILTER
L401	20-3887-10C	COIL, RCF 6.8 uh
T101	95-3136-03	TRANSFORMER HORIZ DRIVER
TX102	95-3395-01	HV SWEEP TRANSFORMER
TX202 A,B	95-3397	DEFLECTION YOKE
CR101	103-142-01	DIODE
CR102	103-142-01	DIODE
CR103	103-142-01	DIODE
CR104	103-261-04A	DIODE
CR105	103-263A	DIODE
CR106	212-76	DIODE
CR107	103-298-04	DIODE
CR108	103-261-02A	DIODE
CR201	103-280-02	DIODE ALT: 103-263 (2) IN PARALLEL
CR301		
CR302		
CR303		
CR304	103-142-01	DIODE
CR305	103-261-02A	DIODE
CR401	103-295-02A	DIODE
Q101	121-975	TRANSISTOR #I HORIZ OSC
Q102	121-975	TRANSISTOR #II HORIZ OSC
Q103	121-975	TRANSISTOR #III HORIZ OSC
Q104	121-975	TRANSISTOR #IV HORIZ OSC
Q105	121-819	TRANSISTOR HORIZ DRIVER
QX106	121-1039	TRANSISTOR HORIZ OUTPUT
Q301	121-975	TRANSISTOR #I VERT OSC
Q302	121-699	TRANSISTOR #II VERT OSC
Q303	121-699	TRANSISTOR #I VERT AMP
Q304	121-975	TRANSISTOR #II VERT AMP
Q305	121-972	TRANSISTOR VERT DRIVER
Q306	121-819	TRANSISTOR VERT OUTPUT I
Q307	121-973	TRANSISTOR VERT OUTPUT II
Q308	121-819	TRANSISTOR VERT RETRACE CONTROL
Q401	121-1034	TRANSISTOR VIDEO OUTPUT
Q402	121-895	TRANSISTOR VIDEO DRIVER
E201	52-2240-01	SPARK GAP (PART OF CRT SOCKET ASSY)
E202	52-2240-01	SPARK GAP (PART OF CRT SOCKET ASSY)
E203	52-2240-01	SPARK GAP (PART OF CRT SOCKET ASSY)
E204	52-2240-01	SPARK GAP (PART OF CRT SOCKET ASSY)
VX201	100-684	12″ CRT *OR*
	100-684-02	12″ CRT

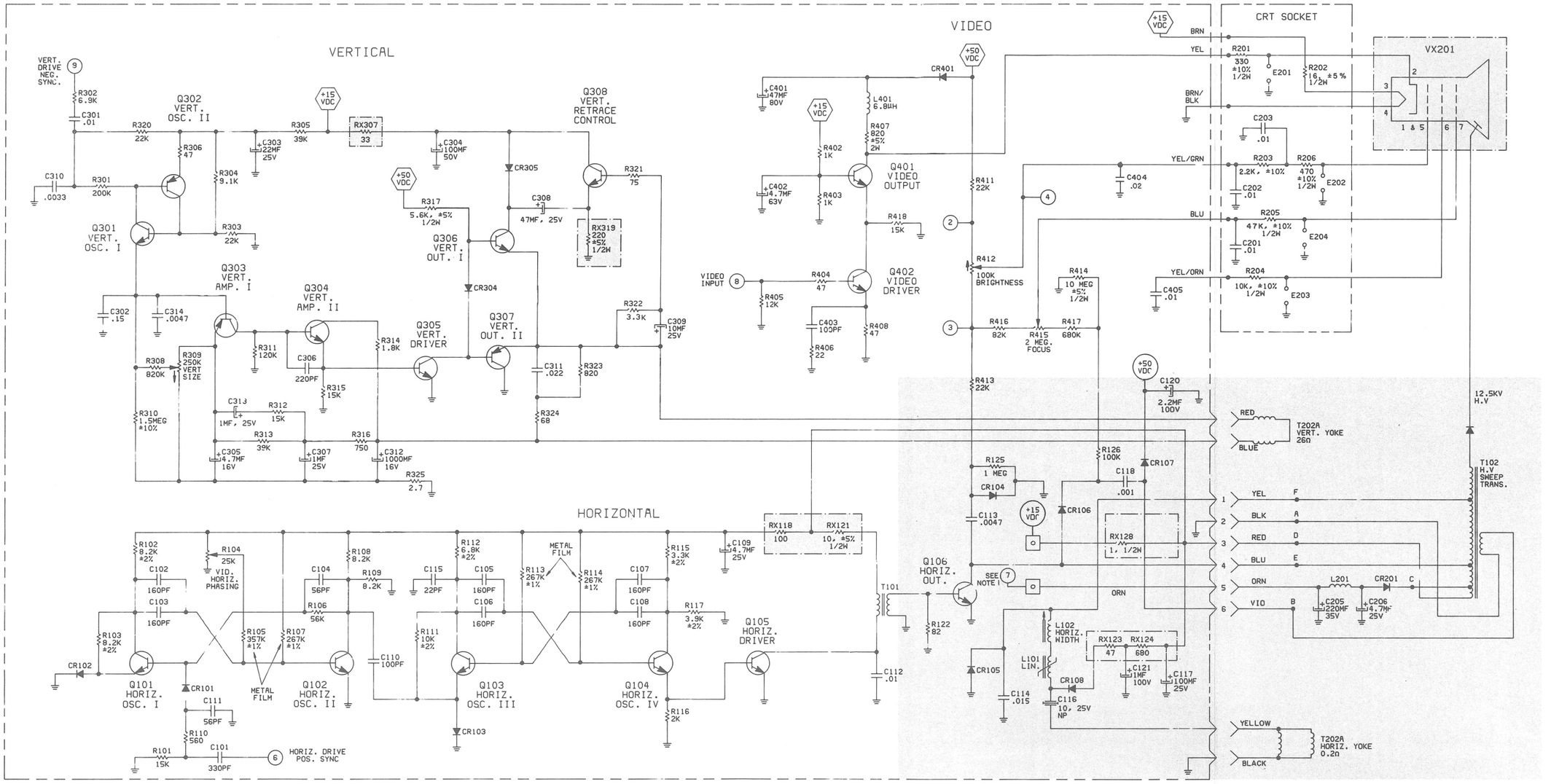


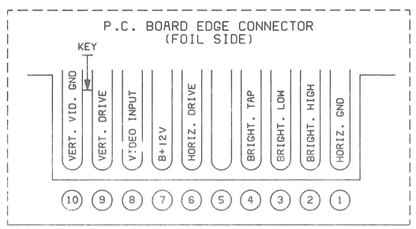


IMPORTANT SAFETY NOTICE

FOR X-RADIATION, FIRE OR SHOCK HAZARD PREVENTION, CERTAIN SPECIAL OR REDUNDANT PARTS ARE USED. USE ONLY EXACT REPLACEMENTS. DO NOT ALTER THE CIRCUIT OR DEFEAT THE FUSES. FAILURE TO COMPLY MAY BE UNLAWFUL.

D12 VIDEO DISPLAY 15.7KHz





= DC VOLTAGE SOURCE

= DC VOLTAGE APPLIED

NOTE: 1. CUSTOMER SUPPLIED EXTERNAL DC SOURCE ON PIN 7 EDGE CONNECTOR

IMPORTANT SAFETY NOTICE

When servicing this chassis, under no circumstances should the original design be modified or altered without permission from the Zenith Radio Corporation. All components should be replaced only with types identical to those in the original circuit. Special components are used to prevent shock and fire hazard. These critical components are shaded on the schematic and parts list for easy identification.

This circuit diagram may occasionally differ from the actual circuit used. This way, implementation of the latest safety and performance improvement changes into the set is not delayed until the new service literature is printed.

IMPORTANT SAFETY NOTICE

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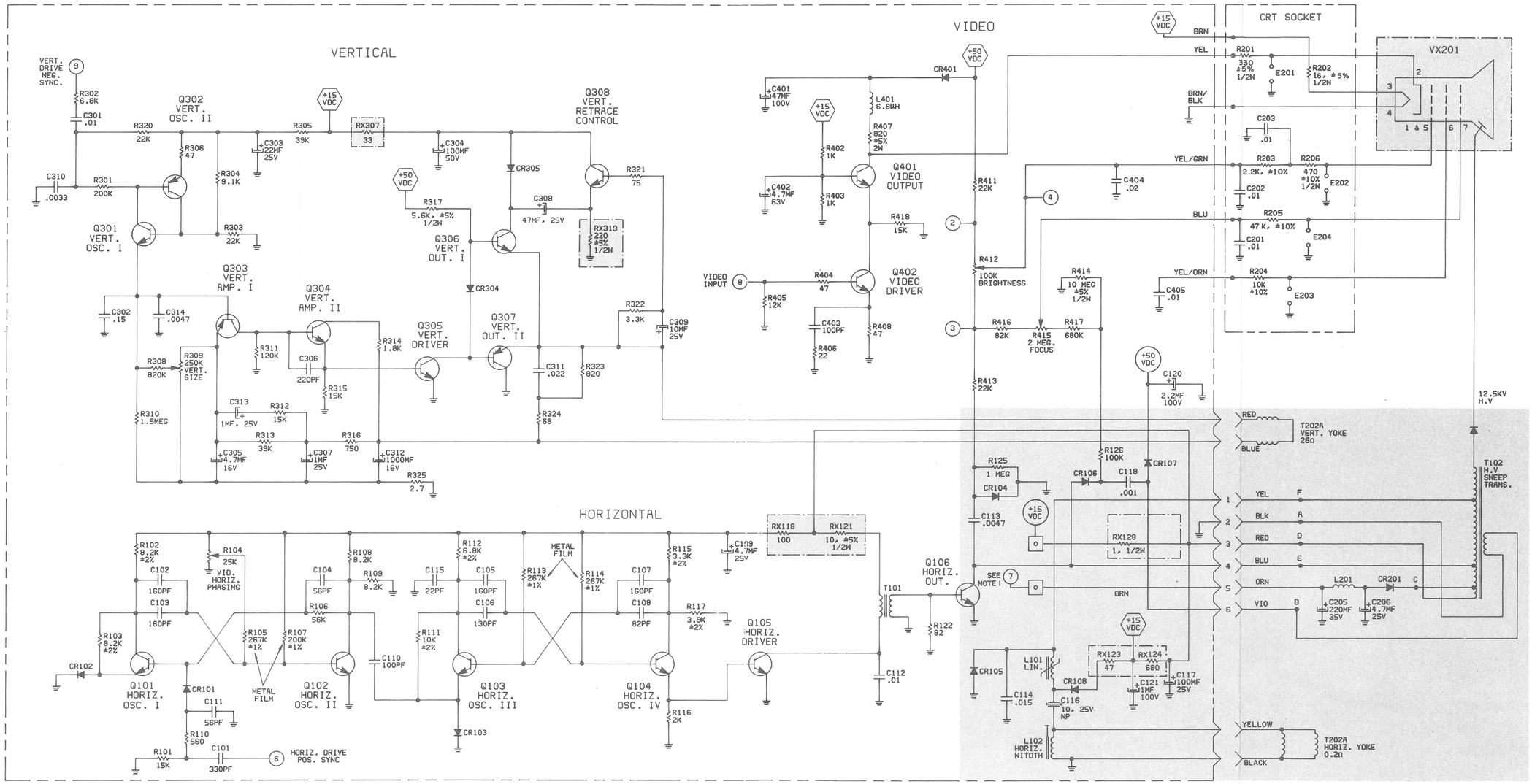
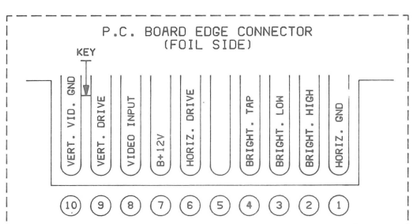
D12 VIDEO DISPLAY 18.6KHz





= DC VOLTAGE SOURCE

= DC VOLTAGE APPLIED

NOTE: 1. CUSTOMER SUPPLIED EXTERNAL DC SOURCE ON PIN 7 EDGE CONNECTOR

IMPORTANT SAFETY NOTICE

When servicing this chassis, under no circumstances should the original design be modified or altered without permission from the Zenith Radio Corporation. All components should be replaced only with types identical to those in the original circuit. Special components are used to prevent shock and fire hazard. These critical components are shaded on the schematic and parts list for easy identification.

This circuit diagram may occasionally differ from the actual circuit used. This way, implementation of the latest safety and performance improvement changes into the set is not delayed until the new service literature is printed.

IMPORTANT SAFETY NOTICE

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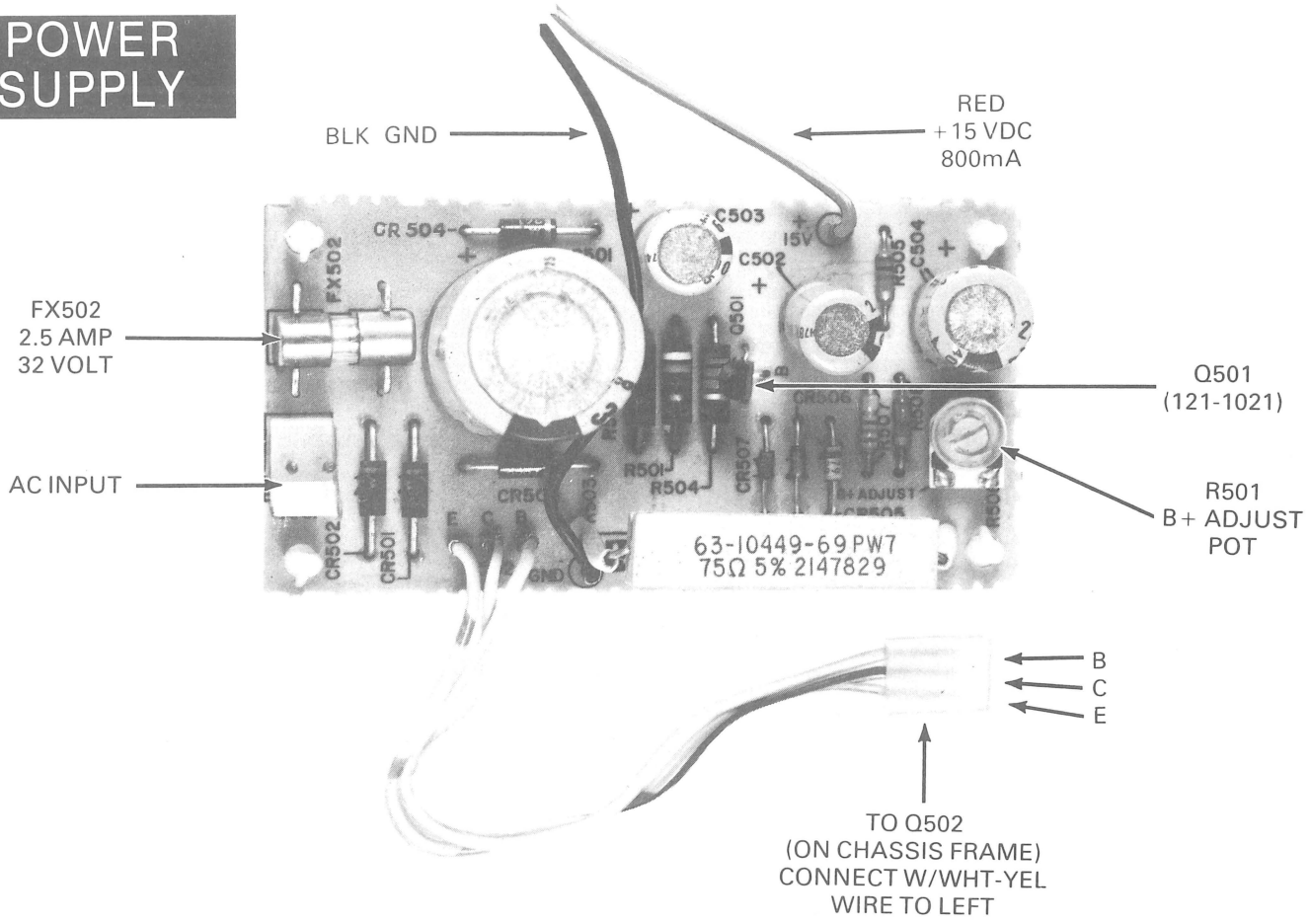
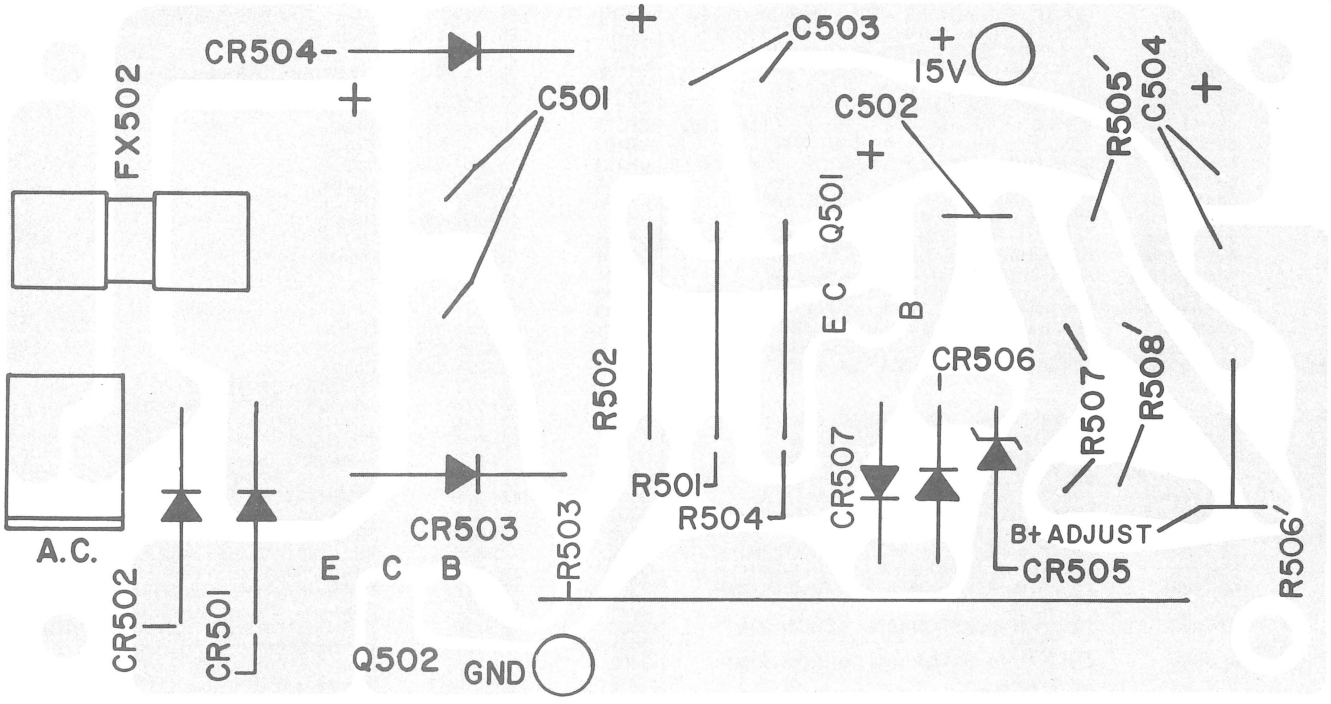
LEGEND

ITEM NO.	PART NO.	DESCRIPTION
C101	22-7614-06A	330 PFD CAPACITOR 20% DISC 50V
C102	22-7619-39A	160 PFD CAPACITOR 5% DISC NPO 50V
C103	22-7619-39A	160 PFD CAPACITOR 5% DISC NPO 50V
C104	22-7622-28A	56 PFD CAPACITOR 10% DISC 50V
C105	22-7619-39A	160 PFD CAPACITOR 5% DISC NPO 50V
C106	22-7619-37A	130 PFD CAPACITOR 5% DISC NPO 50V
C107	22-7619-39A	160 PFD CAPACITOR 5% DISC NPO 50V
C108	22-7619-32A	82 PFD CAPACITOR 5% DISC NPO 50V
C109	22-7152-03	4.7 MFD CAPACITOR +100%—10% ELEC 25V
C110	22-7613A	100 PFD CAPACITOR 10% DISC 50V
C111	22-7622-28A	56 PFD CAPACITOR 10% DISC 50V
C112	22-7613-24A	.01 MFD CAPACITOR 10% DISC 50V
C113	22-7440	.0047 MFD CAPACITOR 10% DISC 500V
CX114	22-7530-07	.015 MFD CAPACITOR 5% POLYESTER 400V
C115	22-7656-13A	22 PFD CAPACITOR 10% DISC 50V
C116	22-7313	10 MFD CAPACITOR 20% NP ELEC 25V
C117	22-7718-09	100 MFD CAPACITOR 20% ELEC 25V
CX118	22-3748	.001 MFD CAPACITOR 10% DISC 1KV
C119		
C120	22-7722-02	2.2 MFD CAPACITOR 20% ELEC 100V
C121	22-7722-01	1 MFD CAPACITOR 20% ELEC 100V
C201	22-4905-01	.01 MFD CAPACITOR +80%—20% DISC 500V
C202	22-4905-01	.01 MFD CAPACITOR +80%—20% DISC 500V
C203	22-4905-01	.01 MFD CAPACITOR +80%—20% DISC 500V
C204		
CX205	22-7144-09	220 MFD CAPACITOR +100%—10% ELEC 35V
CX206	22-7142-03	4.7 MFD CAPACITOR +100%—10% ELEC 25V
C301	22-7613-24A	.01 MFD CAPACITOR 10% DISC 50V
C302	22-7548	.15 MFD CAPACITOR 10% POLYESTER 50V
C303	22-7152-05	22 MFD CAPACITOR +100%—10% ELEC 25V
C304	22-7720-09	100 MFD CAPACITOR 20% ELEC 25V
C305	22-7579-03	4.7 MFD CAPACITOR 10% ELEC 16V
C306	22-7614-04A	220 PFD CAPACITOR 20% DISC 50V
C307	22-7389-02	1 MFD CAPACITOR 20% ELEC 25V
C308	22-7718-08	47 MFD CAPACITOR 20% ELEC 50V
C309	22-7152-04	10 MFD CAPACITOR +100%—10% ELEC 25V
C310	22-7614-18A	.0033 MFD CAPACITOR 20% DISC 50V
C311	22-7615-08A	.022 MFD CAPACITOR +80%—20% DISC 50V
C312	22-7579-04	1000 MFD CAPACITOR 10% ELEC 16V
C313	22-7389-02	1 MFD CAPACITOR 20% ELEC 25V
C314	22-7614-20A	.0047 MFD CAPACITOR 20% DISC 50V
C401	22-7722-08	47 MFD CAPACITOR 20% ELEC 100V
C402	22-7721-04	4.7 MFD CAPACITOR 20% ELEC 63V
C403	22-7613A	100 PFD CAPACITOR 10% DISC 50V
C404	22-7724	.02 MFD CAPACITOR +80%—20% DISC 500V
C405	22-3512	.01 MFD CAPACITOR +40%—10% DISC 1KV
R101	63-9922	15K OHM RESISTOR 5% FILM 1/4W
R102	63-9919-94	8.2K OHM RESISTOR 2% FILM 1/4W
R103	63-9919-94	8.2K OHM RESISTOR 2% FILM 1/4W
R104	63-10651-06	CONTROL 25K OHM (HORIZ PHASE)
R105	63-10533-04	267K OHM RESISTOR 1% (METAL FILM) 1/4W
R106	63-9922-14	56K OHM RESISTOR 5% FILM 1/4W
R107	63-10533-11	200K OHM RESISTOR 1% METAL FILM 1/4W
R108	63-9921-94	8.2K OHM RESISTOR 5% FILM 1/4W
R109	63-9921-94	8.2K OHM RESISTOR 5% FILM 1/4W
R110	63-9921-66	560 OHM RESISTOR 5% 1/4W
R111	63-9919-96	10K OHM RESISTOR 2% FILM 1/4W
R112	63-9919-92	6.8K OHM RESISTOR 2% FILM 1/4W
R113	63-10533-04	267K OHM RESISTOR 2% FILM 1/4W
R114	63-10533-04	267K OHM RESISTOR 1% METAL FILM 1/4W
R115	63-9919-84	3.3K OHM RESISTOR 2% METAL FILM 1/4W
R116	63-9921-79	2K OHM RESISTOR 2% FILM 1/4W
R117	63-9919-86	3.9K OHM RESISTOR 2% FILM 1/4W
RX118	63-10559-48	100 OHM RESISTOR 5% FILM 1/4W
R119		
R120		
RX121	63-10565-24	10 OHM RESISTOR 5% FILM 1/2W
R122	63-9921-46	82 OHM RESISTOR 5% FILM 1/4W
RX123	63-10559-40	47 OHM RESISTOR 5% FILM 1/4W
RX124	63-10559-68	680 OHM RESISTOR 5% FILM 1/4W
R125	63-9922-44	1 MEGOHM RESISTOR 5% FILM 1/4W
R126	63-9922-20	100K OHM RESISTOR 5% FILM 1/4W
RX128	63-10565	1 OHM RESISTOR 5% FILM 1/2W
R201	63-7763	330 OHM RESISTOR 5% CARBON COMP 1/2W
R202	63-7710	16 OHM RESISTOR 5% CARBON COMP 1/2W
R203	63-7799	2.2K OHM RESISTOR 10% CARBON COMP 1/2W
R204	63-7827	10K OHM RESISTOR 10% CARBON COMP 1/2W
R205	63-7855	47K OHM RESISTOR 10% CARBON COMP 1/2W
R206	63-7771	470 OHM RESISTOR 10% CARBON COMP 1/2W
R301	63-9922-27	200K OHM RESISTOR 5% FILM 1/4W
R302	63-9921-92	6.8K OHM RESISTOR 5% FILM 1/4W
R303	63-9922-04	22K OHM RESISTOR 5% FILM 1/4W

ITEM NO.	PART NO.	DESCRIPTION
R304	63-9921-95	9.1K OHM RESISTOR 5% FILM 1/4W
R305	63-9922-10	39K OHM RESISTOR 5% FILM 1/4W
R306	63-9921-40	47 OHM RESISTOR 5% FILM 1/4W
RX307	63-10559-36	33 OHM RESISTOR 5% FILM 1/4W
R308	63-9922-42	820K OHM RESISTOR 5% FILM 1/4W
R309	63-10651-08	CONTROL 250K OHM VERT SIZE 1/4W
R310	63-9924-48	1.5 MEGOHM RESISTOR 10% FILM 1/4W
R311	63-9922-22	120K OHM RESISTOR 5% FILM 1/4W
R312	63-9922	15K OHM RESISTOR 5% FILM 1/4W
R313	63-9922-10	39K OHM RESISTOR 5% FILM 1/4W
R314	63-9921-78	1.8K OHM RESISTOR 5% FILM 1/4W
R315	63-9922	15K OHM RESISTOR 5% FILM 1/4W
R316	63-9921-69	750 OHM RESISTOR 5% FILM 1/4W
R317	63-7816	5.6K OHM RESISTOR 5% CARBON COMP 1/2W
R318		
RX319	63-10565-56	220 OHM RESISTOR 5% FILM 1/2W
R320	63-9922-04	22K OHM RESISTOR 5% FILM 1/4W
R321	63-9921-45	75 OHM RESISTOR 5% FILM 1/4W
R322	63-9921-84	3.3K OHM RESISTOR 5% FILM 1/4W
R323	63-9921-70	820 OHM RESISTOR 5% FILM 1/4W
R324	63-9921-44	68 OHM RESISTOR 5% FILM 1/4W
R325	63-9921-10	2.7 OHM RESISTOR 5% FILM 1/4W
R401		
R402	63-9921-72	1K OHM RESISTOR 5% FILM 1/4W
R403	63-9921-72	1K OHM RESISTOR 5% FILM 1/4W
R404	63-9921-40	47 OHM RESISTOR 5% FILM 1/4W
R405	63-9921-98	12K OHM RESISTOR 5% FILM 1/4W
R406	63-9921-32	22 OHM RESISTOR 5% FILM 1/4W
R407	63-10371-70	820 OHM RESISTOR 5% FILM 2W
R408	63-9921-40	47 OHM RESISTOR 5% FILM 1/4W
R409		
R410		
R411	63-9922-04	22K OHM RESISTOR 5% FILM 1/4W
R412	63-10651-05	CONTROL 100K OHM BRIGHTNESS
R413	63-9922-04	22K OHM RESISTOR 5% FILM 1/4W
R414	63-7952	10 MEGOHM RESISTOR 5% CARBON COMP 1/2W
R415	63-10651-07	CONTROL 2 MEGOHM FOCUS
R416	63-9922-18	82K OHM RESISTOR 5% FILM 1/4W
R417	63-9922-40	680K OHM RESISTOR 5% FILM 1/4W
R418	63-9922	15K OHM RESISTOR 5% FILM 1/4W
L101	20-3906-02	COIL, RCF LINEARITY
LX102	20-3905	COIL, RCF TUNABLE WIDTH
LX201	20-3824	COIL, HORIZ FILTER CHOKE
L401	20-3887-10C	COIL, RCF 6.8 uh
T101	95-3136-01	TRANSFORMER HORIZ DRIVER
TX102	95-3395-01	HV SWEEP TRANSFORMER
TX202 A,B	95-3397	DEFLECTION YOKE
CR101	103-142-01	DIODE
CR102	103-142-01	DIODE
CR103	103-142-01	DIODE
CR104	103-261-04A	DIODE
CR105	103-263A	DIODE
CR106	212-76	DIODE
CR107	103-298-04	DIODE
CR108	103-261-02A	DIODE
CR201	103-280-02	DIODE
CR301		
CR302		
CR303		
CR304	103-142-01	DIODE
CR305	103-261-02A	DIODE
CR401	103-295-02A	DIODE
Q101	121-975	TRANSISTOR I HORIZ OSC
Q102	121-975	TRANSISTOR II HORIZ OSC
Q103	121-975	TRANSISTOR III HORIZ OSC
Q104	121-975	TRANSISTOR IV HORIZ OSC
Q105	121-819	TRANSISTOR HORIZ DRIVER
QX106	121-1039	TRANSISTOR HORIZ OUTPUT
Q301	121-975	TRANSISTOR VERT OSC #1
Q302	121-699	TRANSISTOR VERT OSC #2
Q303	121-699	TRANSISTOR VERT AMP #1
Q304	121-975	TRANSISTOR VERT AMP #2
Q305	121-972	TRANSISTOR VERT DRIVER
Q306	121-819	TRANSISTOR VERT OUTPUT 1
Q307	121-973	TRANSISTOR VERT OUTPUT 2
Q308	121-819	TRANSISTOR VERT RETRACE CONTROL
Q401	121-1034	TRANSISTOR VIDEO OUTPUT
Q402	121-895	TRANSISTOR VIDEO DRIVER
E201	52-2240-01	SPARK GAP (PART OF CRT SOCKET ASSY)
E202	52-2240-01	SPARK GAP (PART OF CRT SOCKET ASSY)
E203	52-2240-01	SPARK GAP (PART OF CRT SOCKET ASSY)
E204	52-2240-01	SPARK GAP (PART OF CRT SOCKET ASSY)
VX201	100-684	12″ CRT *OR*
	100-684-02	12″ CRT

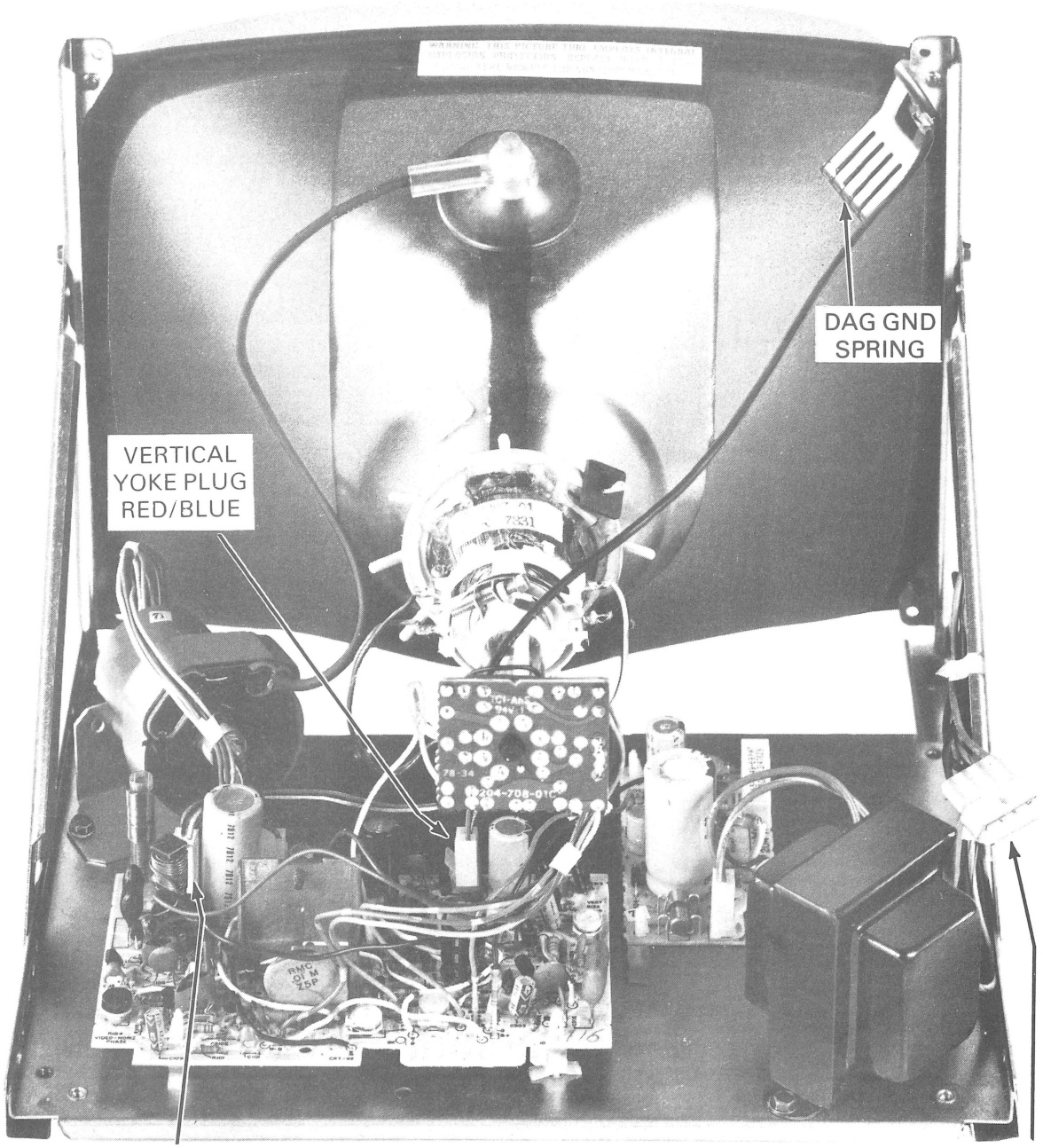
POWER SUPPLY

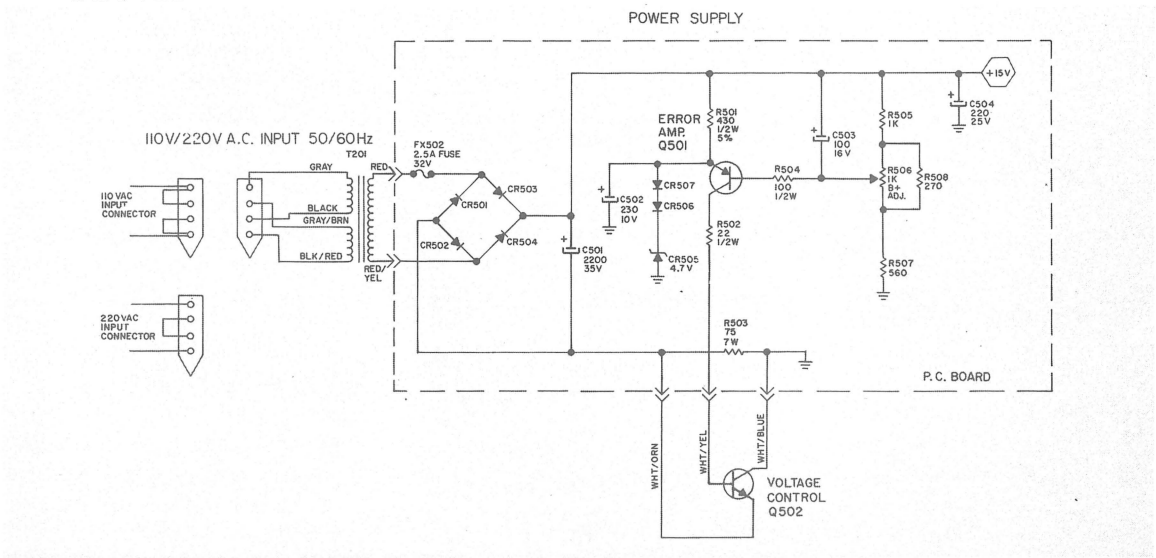




LEGEND

ITEM NO.	PART NO.	DESCRIPTION	ITEM NO.	PART NO.	DESCRIPTION
C501	22-7154-13	2200 MFD CAP ELECT +100%—10% 35V	RX508	63-9921-58	270 OHM RESISTOR 5% FILM 1/4W
C502	22-7152-08	100 MFD CAP ELECT +100%—10% 25V	T201	95-3396	TRANSFORMER, POWER 110/220V
C503	22-7717-09	100 MFD CAP ELECT 20% 16V	CR501	103-261-04A	DIODE
C504	22-7154-08	100 MFD CAP ELECT +100%—10% 35V	CR502	103-261-04A	DIODE
R501	63-7769	430 OHM RESISTOR 5% CARBON COMP 1/2W	CR503	103-261-04A	DIODE
R502	63-7715	22 OHM RESISTOR 10% CARBON COMP 1/2W	CR504	103-261-04A	DIODE
R503	63-10449-69	75 OHM RESISTOR WW 5% 7W	CR505	103-279-09A	DIODE ZENER 4.7V
R504	63-7743	100 OHM RESISTOR 10% CARBON COMP 1/2W	CR506	103-142-01	DIODE
			CR507	103-142-01	DIODE
RX505	63-9921-72	1K OHM RESISTOR 5% FILM 1/4W	Q501	121-1021	TRANSISTOR ERROR AMP
RX506	63-10651-01	CONTROL 1K OHM (B+ ADJ)	QX502	121-992-01	TRANSISTOR VOLTAGE CONTROL
RX507	63-9921-66	560 OHM RESISTOR 5% FILM 1/4W	FX502	136-120-06	FUSE 2.5 AMP 32V


DAG GND SPRING
VERTICAL YOKE PLUG RED/BLUE
HORIZONTAL YOKE PLUG BLK/YEL
AC INPUT


POWER SUPPLY
110V/220V A.C. INPUT 50/60Hz
T201
110 VAC INPUT CONNECTOR
220 VAC INPUT CONNECTOR
GRAY
BLACK
GRAY/BRN
BLK/RED
RED
RED/YEL
FX502 2.5A FUSE 32V
CR501
CR502
CR503
CR504
C501 2200 35V
ERROR AMP. Q501
R501 430 1/2W 5%
C502 230 10V
CR507
CR506
CR505 4.7V
R502 22 1/2W
R504 100 1/2W
C503 100 16V
R505 1K
R506 1K B+ ADJ.
R508 270
R507 560
+15V
C504 220 25V
R503 75 7W
P.C. BOARD
WHT/ORN
WHT/YEL
WHT/BLUE
VOLTAGE CONTROL Q502

DT1

Section 4

POWER SUPPLY MODULE

A. Theory of Operation

The power supply is designed for full wave center tapped operation with series pass regulation. One center tapped winding is used to develop the +5 volt supply. A 5 volt, 3 terminal regulator is used to develop a 3 amp regulated output capability. The regulator is virtually blowout proof and has internal current limiting, power limiting and thermal shutdown. A second center tapped winding is used to develop the ±12 volt supplies. The -5 volt supply is derived from the -12 volt supply. These supplies are also implemented using 3 terminal regulators. These regulators have a 1 amp output capability with internal current limiting, power limiting and thermal shutdown.

The power supply is designed for convection cooling. The 3 terminal regulators are attached to the aluminum rear panel for thermal conduction; the rear panel is black-anodized to maximize radiation. Thermally conductive pads are installed between the regulators and the rear panel. If a regulator is replaced the pads must also be replaced or a thermally conductive grease applied.

PARTS LIST

Title: ASSY-POWER SUPPLY, 1061 #D53615 Rev: D

ITEM	DESCRIPTION	PART NO.	INVENTORY	1	2	3	4
1	Assy-Power Supply, 1061		3B2159	X			
2	Trimpot - 500 Ohrn	91X	6B0311	X			
3	IC-LIN, Voltage Regulator 5V	LM323K-5	33B0363	X			
4	IC-LIN, Voltage Regulator 12V	7812CK	33B0364	X			
5	IC-LIN, Voltage Regulator -12V	7912UC	33B0365	X			
6	IC-LIN, Voltage Regulator -5V	79M05UC	33B0256	X			
7	Diode	IN5624	32B0271				X
8	Diode	IN4003	32C0133		X		
9	Capacitor-10,000 MFD/15V, Ele.	TVA1175.8	15B0306	X			
10	Capacitor-2500 MFD/25V, Elec.	TVA1213.5	15B0307		X		
11	Capacitor-10 MFD/63V, Elec.	VTT10D63	15B0196				X
12	Capacitor-.1 MFD/50V, Disc.	DG015E104Z	15B0304			X	
13	Fuse - 1 Amp, 125V, Slo-Blo	313001	17B0183	X			
14	Transformer	023-2851	7B0240	X			

ORDERING INFORMATION

1) For ordering information and latest prices, contact your local representative or the RESEARCH, Incorporated factory in Minneapolis, Minnesota.

2) When ordering spare parts, please include references both to this parts list number and revision level, plus, the Model Number and Serial Number of the instrument for which these parts are being ordered.

Section 5

KEYBOARD MODULE

A. Theory of Operation

The keyboard consists of mechanically sealed switches connected in a matrix which is located directly in the microprocessor memory space. The microprocessor scans the addresses at which keys are located and determines when a key has been pressed. Thus, the keyboard is encoded by the microprocessor. Functions such as switch debouncing, n-key rollover and automatic repeat of "held" keys are performed by the microprocessor. A diode is connected electrically in series with each switch to isolate the switches from each other.

The address lines from the logic card are labeled KA0 through KA3. The data lines to the logic card are labeled KB0 through KB7. A one-of-16-decoder is used to decode the address lines and drive the data lines. The switches are connected in series between the decoder and the data lines. A pull up resistor on the logic card holds the data lines at +5 volts; when a key is pressed (and the microprocessor addresses the line that the switch is connected to) the active low output of the decoder will pull the data line to near 0 volts. The microprocessor senses a logic 0 for keys which are active and a 1 for keys which are not active.

An LED is supplied on the keyboard which illuminates whenever the keyboard is correctly plugged into the terminal and power is applied to the terminal. The keyboard cable connects to the rear of the Teleray. A round shielded cable is used. The shield is connected to chassis ground and to the metal key mounting surface to discharge operator induced static electricity.

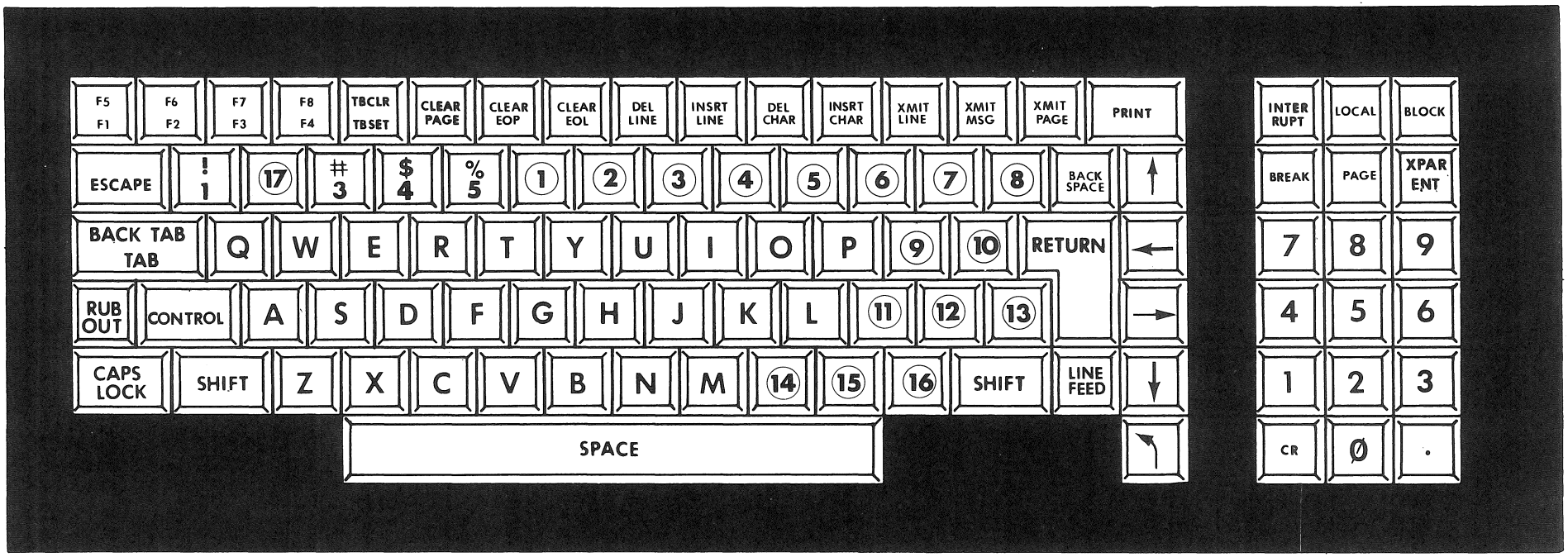
Key Legend	No Shift	Shift	Control	Key Legend	No Shift	Shift	Control
Space	Space	Space	Space	W	w	W	ETB
↖	↖	↖	↖	E	e	E	ENQ
Caps Lock	-	Caps Lock	-	R	r	R	DC2
Shift	-	Shift	-	T	t	T	DC4
Z	z	Z	SUB	Y	y	Y	EM
X	x	X	CAN	U	u	U	NAK
C	c	C	ETX	I	i	I	HT
V	v	V	SYN	O	o	O	SI
B	b	B	STX	P	p	P	DLE
N	n	N	SO	[	[	{	ESC
M	m	M	CR	\	\	¦	FS
,	,	<	NUL	←	←	←	←
.	.	>	NUL	ESCAPE	ESC	ESC	ESC
/	/	?	US	1	1	!	NUL
Shift	-	Shift	-	2	2	@	NUL
Line Feed	LF	LF	LF	3	3	#	NUL
↓	↓	↓	↓	4	4	$	NUL
DEL	DEL	DEL	DEL	5	5	%	NUL
Control	-	Control	-	6	6	^	NUL
A	a	A	SOH	7	7	&	NUL
S	s	S	DC3	8	8	*	NUL
D	d	D	EOT	9	9	(	NUL
F	f	F	ACK	Ø	Ø	)	NUL
G	g	G	BEL	-	-	—	NUL
H	h	H	BS	=	=	+	NUL
J	j	J	LF	`	`	~	RS
K	k	K	VT	Bk Space	BS	BS	BS
L	l	L	FF	↑	↑	↑	↑
;	;	:	NUL	F1	F1	F5	**
'	'	"	NUL	F2	F2	F6	**
]	]	}	GS	F3	F3	F7	**
Return	CR	CR	CR	F4	F4	F8	**
→	→	→	→	Tab Set	Tab Set	Tab Clr	**
Tab	Tab	Back Tab	**	Clr Page	-	Clear Page	-
Q	q	Q	DC1	Clr EOP	-	Clear EOP	-

Key Legend	No Shift	Shift	Control
Clear EOL	Clear EOL	Clear Line	**
Del Line	-Delete Line-		
Insert Line	-Insert Line-		
Del Char	-Delete Character-		
Insert Char	-Insert Character-		
Xmit Line	-Transmit Line-		
Xmit Msg	-Transmit Message-		
Xmit Page	-Transmit Page-		
Print	-Print All-		
CR	CR	CR	CR
Ø	Ø	Ø	Ø
.	.	.	.
1	1	1	1
2	2	2	2
3	3	3	3
4	4	4	4
5	5	5	5
6	6	6	6
7	7	7	7
8	8	8	8
9	9	9	9
Break	270 msec Break-		
Interrupt (to NMI)			

	Key Up (Logic 1)	Key Down (Logic 0)
LOCAL	ON LINE	Local Mode
SCROLL	Page Mode	Scroll Mode
XPRINT	Normal	Xparent Mode
BLOCK	Character	Block Mode

Note: On these keys the control key input is ignored. Control overrides shift except for keys marked ** in Control column; on the marked keys the control input is ignored.

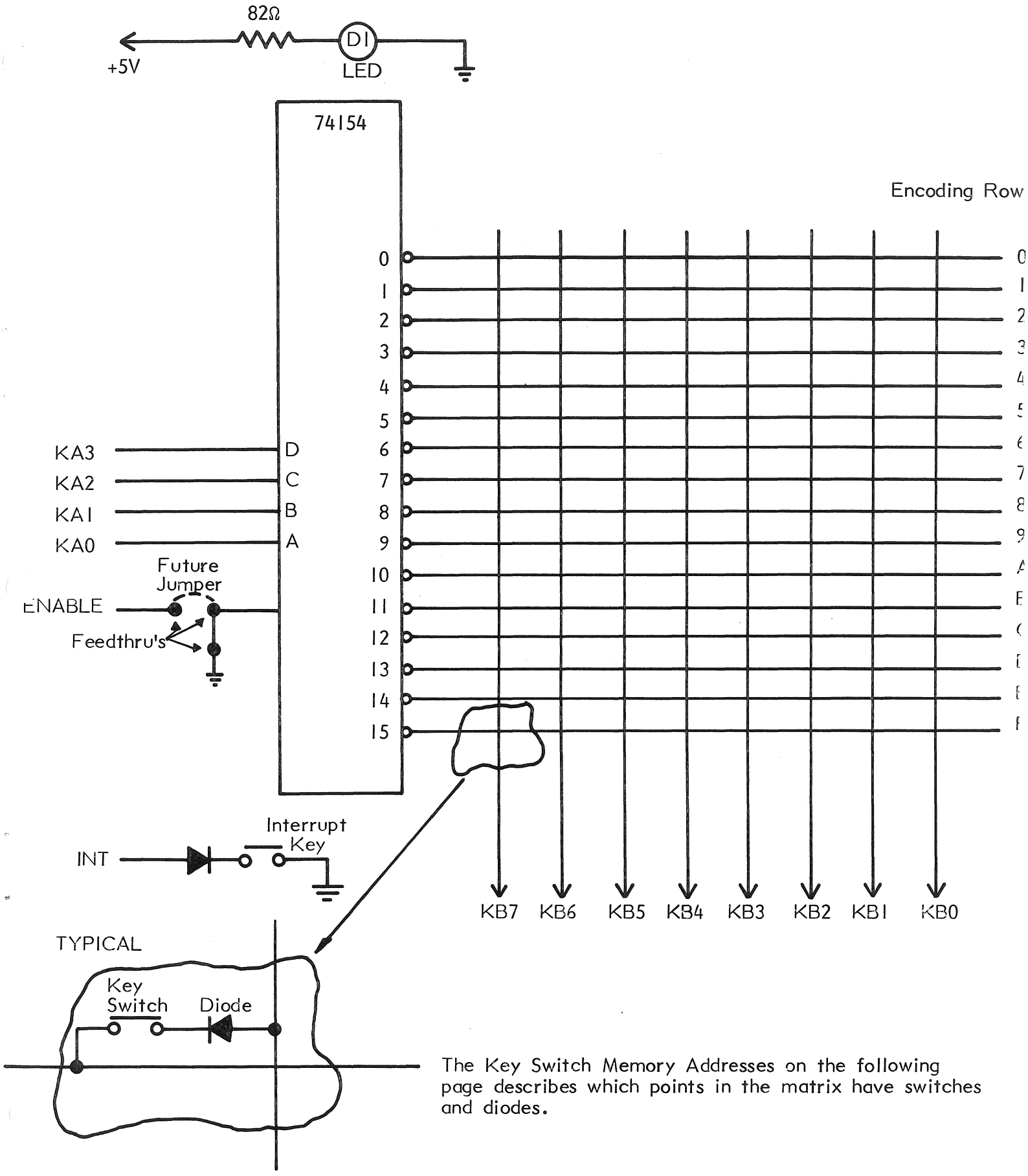
KEYBOARD CODING - STANDARD



Keyboard Coding - Numbered keys are those whose coding and/or legend changes for the European version of the keyboard. The coding and legend changes for these keys are shown on the following page.

EUROPEAN KEYBOARD LEGENDS/CODING

Keytop for Circled Number	LEGEND Swedish Keytop	LEGEND German	LEGEND Norwegian Danish	Unshift	ASCII Coding Shift	CTRL
1	& 6	'& 6	& 6	6	&	NUL
2	/ 7	/ 7	/ 7	7	/	NUL
3	(8	(8	(8	8	(	NUL
4	) 9	) 9	) 9	9	)	NUL
5	= 0	= 0	= 0	0	=	NUL
6	? +	? +	? +	+	?	NUL
7	none E'	§ \	@ \	'	@	NUL
8	> <	> <	> <	>	<	NUL
9	none Å	none Ü	Å	}	]	GS
10	none Ü	^ ß	^ ~	~	^	RS
11	none Ö	none Ö	none Ø	|	\	FS
12	none Ä	none Ä	none Æ	{	[	NUL
13	* '	* '	* '	'	*	NUL
14	; ,	; ,	; ,	,	;	NUL
15	: .	: .	: .	.	:	NUL
16	— -	— -	— -	-	—	US
17	" 2	" 2	" 2	2	"	NUL



The Key Switch Memory Addresses on the following page describes which points in the matrix have switches and diodes.

KEYBOARD SCHEMATIC

KA		KB7	KB6	KB5	KB4	KB3	KB2	KB1	KB0
3210									
0000	0	7	6	5	4	3	2	1	0
0001	1							9	8
0010	2	G	F	E	D	C	B	A	Space
0011	3	O	N	M	L	K	J	I	H
0100	4	W	V	U	T	S	R	Q	P
0101	5	=					Z	Y	X
0110	6	/	.	=	,	;	'		
0111	7								
1000	8	DEL	BREAK	RETURN		ESC	LF	TAB	BS
1001	9	CLEAR EOP	CLEAR PAGE	TAB SET	CLEAR EOL	F4	F3	F2	F1
1010	A	PRINT	XMT PAGE	XMT MSG	XMT LINE	INST CHAR	DEL CHAR	INST LINE	DEL LINE
1011	B								
1100	C*	7	6	5	4	3	2	1	0
1101	D*	CTRL		CR			.	9	8
1110	E	SHIFT	CAPS LOCK						SHIFT
1111	F	LOCAL	TRANS-PARENT					BLOCK	SCROLL

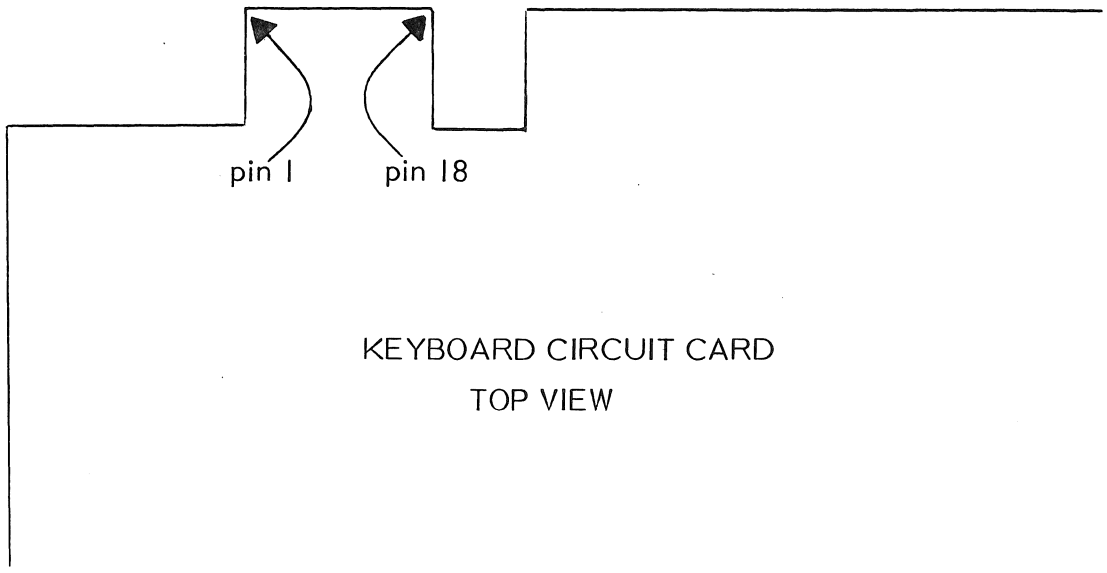
Interrupt = dedicated line to connector
*These rows contain the numeric block

All Addresses (KA) located at 000 X$_{16}$
Keyswitch Memory Addresses

KEYBOARD SCHEMATIC - Continued

KEYBOARD CONNECTOR/CABLE PIN ASSIGNMENT

Keyboard Pin No.	Signal Name	Wire Color	Rear Panel Connector Pin No.
1	Logic Ground	White-Red	23
2	+5V	Green	6
3	KA0	Orange	4
4	KA1	Brown	2
5	KA2	Black	1
6	KA3	Red	3
7	Interrupt	Blue	7
8	KB7	White	10
9	KB4	Grey	9
10	KB6	Yellow	5
11	KB5	Violet	8
12	KB3	White-Yellow	24
13	KB2	White-Brown	12
14	KB1	White-Orange	25
15	KB0	White-Black	11
16	Unused		
17	Chassis Ground	White-Blue	13
18	Unused		



KEYBOARD CIRCUIT CARD

TOP VIEW

KEYBOARD PARTS LIST

Title	Quantity Used
1062 Keyswitch, momentary	91
1062 Keyswitch, locking	6
Diode, IN914 or equivalent	97
IC, 1 of 16 decoder 74154	1
LED GE# LED 55B or equivalent	1
Resistor, 47Ω , 1/4 watt, carbon	1

Section 6

LOGIC MODULE

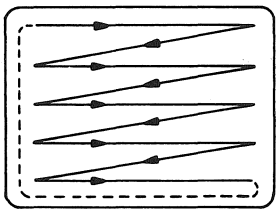
A. Architecture

The Teleray logic is a microprocessor oriented bus structured design. Specialized hardware is provided for the display of data from RAM on the CRT (display refresh hardware, character generator). Specialized hardware is also provided for enhancing the data display (Field Modifier Logic). Bus oriented interfaces are provided for the keyboard, the Serial Input/Output and for the rear panel switches. Program space for ROM and RAM is also provided. the Logic Module Architecture Diagram shows this structure; the Logic Module Block Diagram further details the organization.

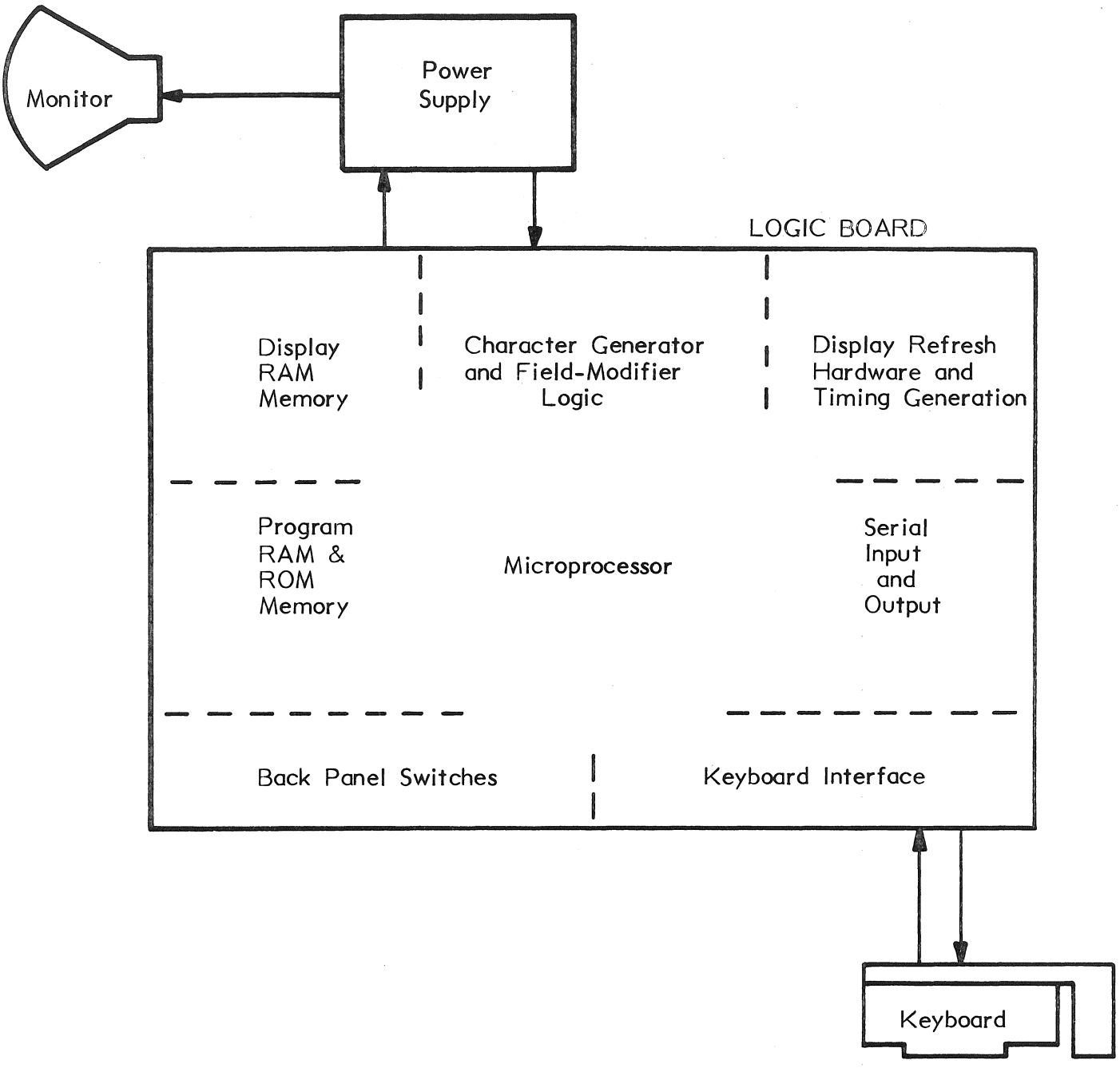
B. Theory of Operation

1. Display Refresh Hardware

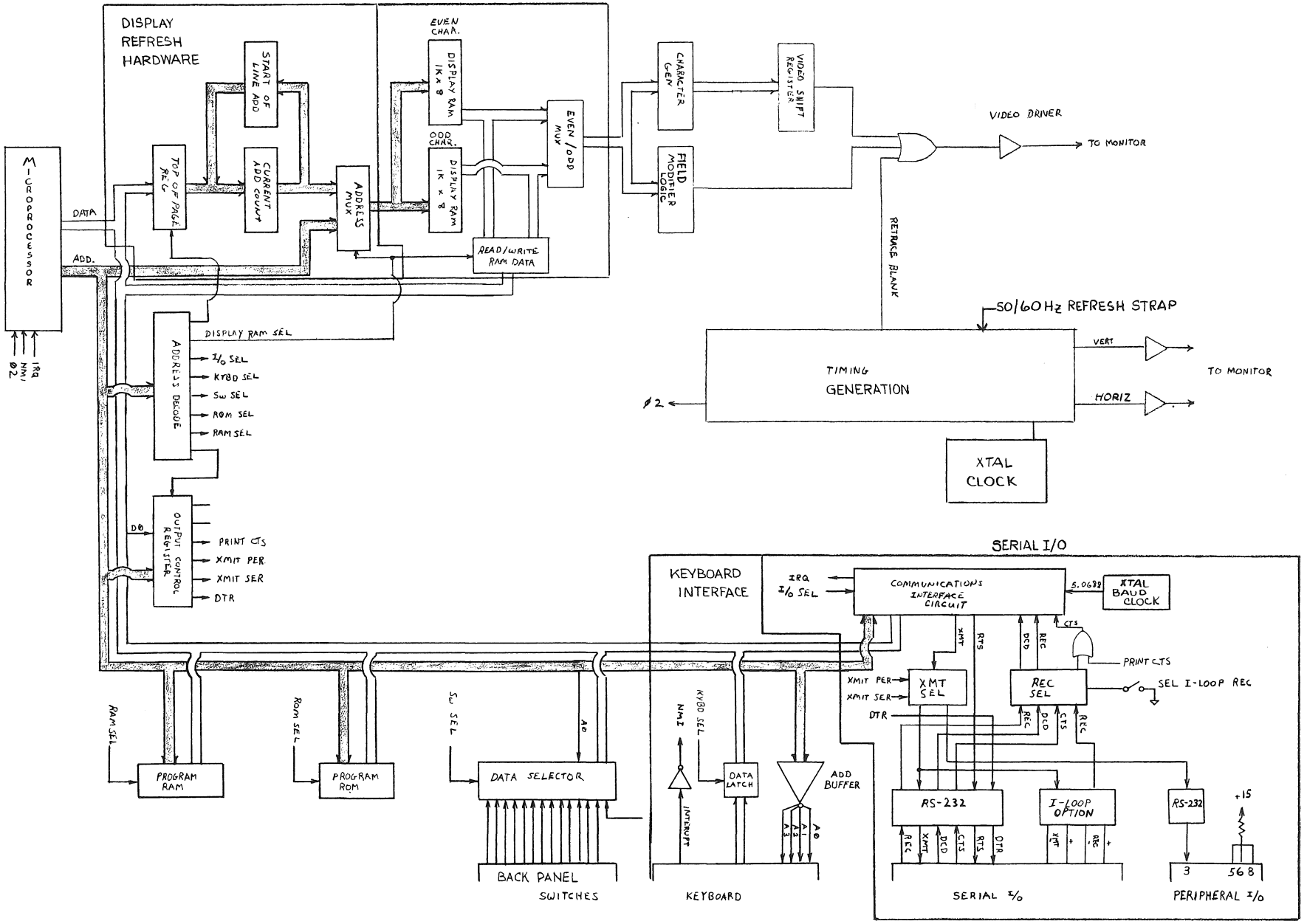
This logic controls the monitor and provides time and address references for retrieving data from memory. The display on the TELERAY monitor is a "raster" scan. The electronic beam scans the face of the CRT 60 times a second following the generalized pattern shown below. The pattern is "non-interlaced"; i.e., the beam starts at the same place every time and horizontal lines remain distinct. The "vertical sync" signal causes the beam to return to the top left corner of the screen; the "horizontal drive" signal causes the beam to start a new line. The characters are formed when the beam is moving from left to right by illuminating a given position as the beam passes. The signal which provides the "illumination" information to the monitor is the video signal. The timing section of the TELERAY logic provides the Horizontal Drive and Vertical Sync and controls the Video signal.



The characters are formed within a 7 x 9 dot matrix. There are seven dots horizontally and nine dots vertically. In addition, there are three dots (horizontally) of intercharacter separation and three lines of vertical interline separation. Each character position then occupies 12 horizontal lines of ten dots per line, and the characters themselves are formed on a 7 x 9 matrix field within this 10 x 12 position field.



LOGIC MODULE ARCHITECTURE DIAGRAM



LOGIC MODULE BLOCK DIAGRAM

Eighty characters are formed on each horizontal line (a total of 80 x 10 = 800 dots per scan line). Timing for an additional 20 character positions is provided on each line to allow the beam to return from the right side of the CRT to the left side and to provide a "margin" on each side of the data on the CRT screen. Each horizontal line contains a total of 80 + 20 = 100 character positions. As mentioned earlier, 12 horizontal lines are used to write a single row of characters. The TELERAY is capable of displaying 24 character rows in a page, or frame. The timing additionally provides for more rows to give the beam time to return from the bottom of the CRT to the top, and leave a margin at top and bottom. A total of 310 scan lines are thus used as the beam scans the entire face of the CRT (one frame). When the TELERAY is set for 50 Hertz refresh, 372 scan lines are used.

Characters are formed by selectively illuminating the proper dot positions within the matrix. Ten dots are allowed horizontally for each character, 100 characters for each line, 12 lines for each character row, and 25 and 10/12 character rows per frame. At 50 Hertz refresh there are 31 character rows per frame.

A crystal oscillator provides the base for all timing. The period of the oscillator controls the width of one dot. The dot counter then counts groups of ten dots (- by 10) to indicate horizontal character positions. The dot counter is also used to clock out the video information.

The character-per-line counter counts 100 characters (÷ by 100). The horizontal drive signal is derived from this "character-per-line timing counter". Decoding is used to correctly set the relationship between the video information and the horizontal drive signal. This counter is also used to generate the microprocessor clock.

The Character Scan counter counts scan lines and divides by 12 (counts to 12) to indicate when a character line has been completed. Outputs from this counter also go to the character generator to indicate which line within the character is to be displayed.

The Character Line Counter counts the character rows. Decoding on this counter locates the Vertical Sync signal to center the video information on the CRT face vertically. If the TELERAY is set for 50 Hz refresh this counter is modified so that 31 character rows are counted.

Some frequencies associated with the above discussion follow:

Master OSC	18.6 MHZ	53.8 nsec period
Dot Counter Output	18.6 KHZ	53.8 nsec period
Horizontal Drive	18.6 KHZ	53.8 usec period
Character Row	1.55 KHZ	64.5 usec peirod
Vertical Sync	60 HZ	16.67 msec period
OR	50 HZ	20 msec period

The display hardware maintains a set of address counters called Current Address Counters. At the beginning of each frame the starting address of the frame is loaded from the microprocessor written Top of Page Register (TOPR) into these counters. Two characters are read out of the display memory during Ø1; the UP only uses the RAM during Ø2. This hardware address counter controls which characters are read from the display RAM. Scrolls are effected by changing the contents of TOPR. If the hardware display counters reach the end of the display memory, the Clear Current Address Counter (CLC) signal will be generated resetting the counters to the start of display memory.

Clocks for the Current Address Counters are derived from the Dot Counter, the Character Counter, the Character Scan Counter and from the Line Counter. There will be 80 clocks on the beginning of every Character Scan to advance the Current Address Counters. Since the Character Counter is used to clock both these counters and to generate the microprocessor clocks, the microprocessor and the Current Address Counters are always in synchronization with each other. During Clock Ø1, the Address Counters are used to access the Display RAM; during Clock Ø2 the microprocessor can access Display RAM.

Wide mode is controlled by the microprocessor. When the Output Control Register bit is set to a 1 the display refresh hardware goes to Wide mode; the video clocks run at half their normal speed - horizontal and vertical remain unchanged, of course. In Wide mode, the Address Counters count at half their normal speed except during the twelveth scan. During this scan the counters always count at their normal rate to ensure that they will be at the correct location for the start of scan 1 on the following character line.

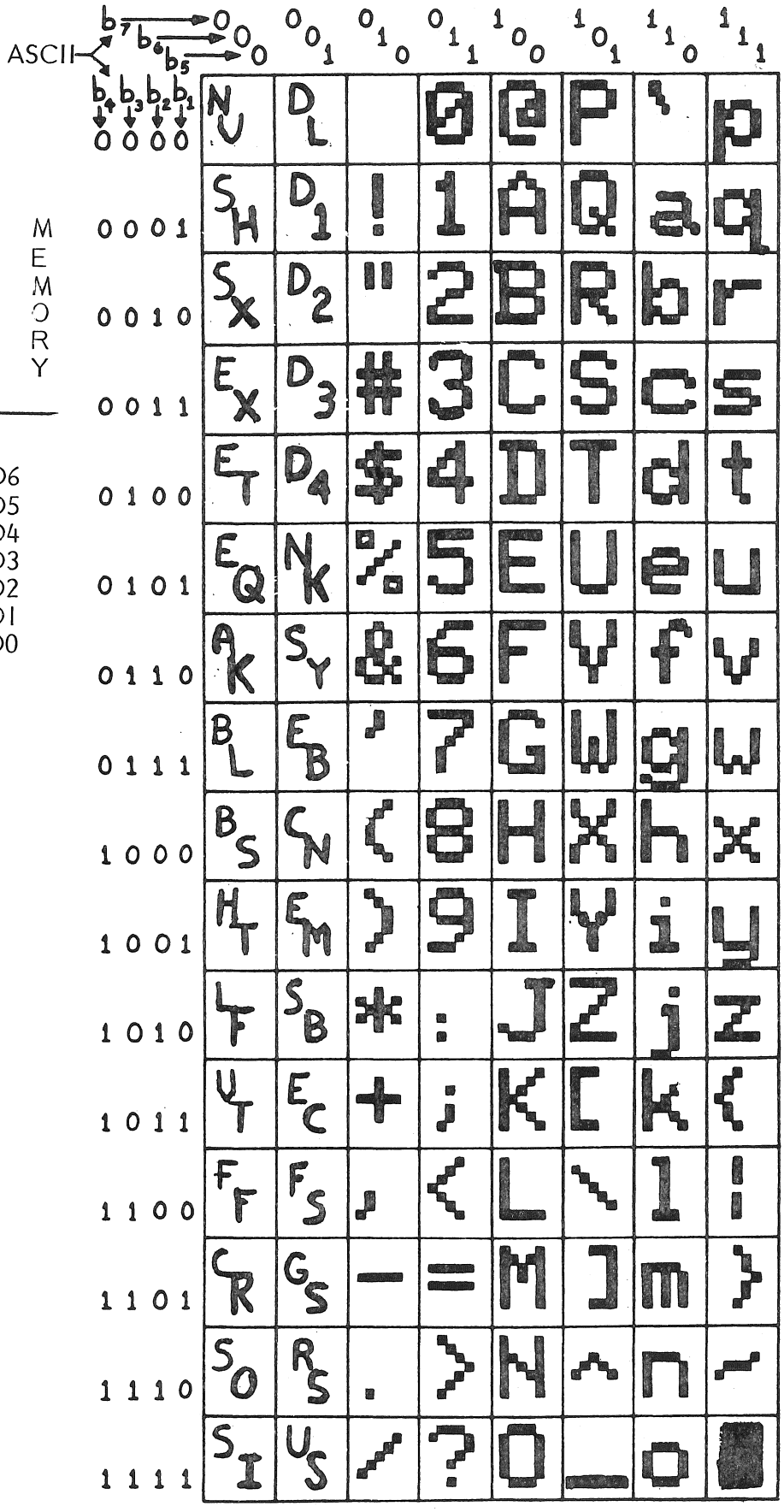
2. Character Generator and Field Modifier Logic

The Teleray uses a ROM to convert the ASCII coded information in the display memory to a dot pattern forming characters on the CRT face. All seven dots are outputted by the character generator ROM in parallel. These dots are serialized by the video shift register and are presented to the video amplifier of the monitor one at a time. The video shift register uses clocks developed from the dot counter to clock the dots to the video amplifier.

A mask programmed 2K by 8 ROM is used as the character generator. Ultraviolet erasable (UVEPROM) versions of this ROM are available. The ROM has 8 data outputs, the eighth bit is unused for all characters. The four least significant address lines are controlled by the character scan counter. These lines are used to determine which row of dots within the character will be displayed. The seven most significant address lines are the ASCII coded dots from the display memory. The Teleray display font is shown on the following page.

Characters are accessed from the Display Memory in pairs. A bus is used to route this data one character at a time to both the character generator and to the Field Modifier logic. The Display Memory bit map shows the coding used within the Display Memory. If memory bit 7 is a 1; the character is treated as a field modifier character and the character is loaded into a latch. The outputs of this latch, when set to a 1 will:

TELERAY Display Font



ASCII DISPLAY MEMORY

b7 D6
b6 D5
b5 D4
b4 D3
b3 D2
b2 D1
b1 D0

Coding Example

Seven Most Significant Address Lines = 4 D
Character = "M"

ROM Scan Address Lines (4 LSB)	DOTS (ROM Outputs) 7 6 5 4 3 2 1 0
0000	0 1 0 0 0 0 0 1
0001	0 1 1 0 0 0 1 1
0010	0 1 0 1 0 1 0 1
0011	0 1 0 0 1 0 0 1
0100	0 1 0 0 1 0 0 1
0101	0 1 0 0 0 0 0 1
0110	0 1 0 0 0 0 0 1
0111	0 1 0 0 0 0 0 1
1000	0 1 0 0 0 0 0 1
1001	0 Normally all zero
1010	0 used for characters w/tails below line such as "g"
1011	0
1100	0
1101	0 All Zero
1110	0 Unused
1111	0 0 0 0 0 0 0 0

BIT	FIELD MODIFIER CHARACTER	DATA CHARACTER
7	I	0
6	Z	X (b7 in ASCII)
5	Y (Underscore)	X (b6 in ASCII)
4	Y (Inverse)	X (b5 in ASCII)
3	Y (Dim)	X (b4 in ASCII)
2	Y (Blink)	X (b3 in ASCII)
1	Z	X (b2 in ASCII)
0	Z	X (b1 in ASCII)

Legend

X = data bits, ASCII coded
Y = attribute bits
Z = reserved (currently unused)

DISPLAY MEMORY BIT MAP

BLINK - the Blink oscillator is ANDed with serial video
UNDERSCORE - the serial video is ORed with a 1 during scan 12
INVERSE - the serial video is INVERTED, except during retrace
and DIM - the serial video amplitude is clamped to a potentiometer preset value which is lower than the normal value.

A special attribute character is formed using the dot counter to generate a "11" video pattern. The character generator video is disregarded during the attribute character time interval.

3. Display Memory and Program Memory

The Display Memory is implemented with 4 of 1K by 4 static RAMs. These RAMs are organized into an even bank of 8 bits and an odd bank of 8 bits. The refresh hardware accesses one character from each bank during microprocessor Ø1. These characters are stored in a buffer register and fed to the character generator and attribute logic one at a time. There are 2048 bits of display memory but only 1920 are needed for the display of 24 by 80 characters. The remaining 128 bits are used by the program. See the memory maps for the description of their use. 1024 additional bits of RAM memory are provided for program use. Again, see the memory maps. 4K bits of ROM space are installed for the standard program. An additional 1K bit can be installed if necessary.

4. Keyboard and Switch Interfaces

The rear panel switches and the keyboard can be read directly by the microprocessor. The switches and the keyboard are located in the microprocessor address space and during a read operation the appropriate switches are gated onto the microprocessor data bus by tri-state integrated circuits. The switches and the keyboard are scanned by the microprocessor. No interrupts are generated by the hardware. A hardware timer does generate an interrupt every 645 microseconds to help the microprocessor "time" its scans. See the memory maps for the switch and keyboard memory locations.

The microprocessor converts the key contact inputs to ASCII characters. The microprocessor keyboard coding table lists the hexidecimal codes generated for each memory address.

MEMORY ADDRESS/ BIT	Code In No Shift	Code In Shift	Code In Control	MEMORY ADDRESS/ BIT	Code With No Shift	Code With Shift	Code With Control	MEMORY ADDRESS/ BIT	No Shift	Shift	Control
2 0 Space	20	20	20	5 3 W	77	57	17	9 4 Clear EOL	LF Clear EOL	LF Clear Line	**
B 0 ↑	Home LF	Home LF	Home LF	2 5 E	65	45	05	A 0 Del Line	LF	Delete Line	LF
E 6	KF	Caps Lock	KF	4 2 R	72	52	12	A 1 Insert Line	LF	Insert Line	
E 7	KF	Shift	KF	4 4 T	74	54	14	A 2 Del Char.	LF	Delete Char.	
5 2 z	7A	5A	1A	5 1 y	79	59	19	A 3 Insert Char.	LF	Insert Char.	
5 0 x	78	78	18	4 5 u	75	55	15	A 4 Trans. Line	LF	Trans. Line	
2 3 c	63	43	03	3 1 I	69	49	09	A 5 Trans. Msg.	LF	Trans. Message	
4 6 v	76	56	16	3 7 o	6F	4F	0F	A 6 Trans. Page	LF	Trans. Page	
2 2 B	62	42	02	4 0 p	70	50	10	A 7 Print	LF	Print All	LF
3 6 N	6E	4E	0E	5 3[	5B	7B	1B	D 5 CR	0D	0D	0D
3 5 M	6D	4D	0D	5 4 \	5C	7C	1C	C 0 0	30	30	30
3 4 ,	2C	3C	00	B 3 ←	LF	One Left	LF	C 2 .	2E	2E	2E
6 6 .	2E	3E	00	8 3 ESC	1B	1B	1B	C 1 1	31	31	31
6 7 /	2F	3F	1F	0 1 1	31	21	00	C 2 2	32	32	32
E 0 Shift	KF	KF	KF	0 2 2	32	40	00	C 3 3	33	33	33
8 2 LF	0A	0A	0A	0 3 3	33	23	00	C 4 4	34	34	34
B 1 ↓	LF	One Down	LF	0 4 4	34	24	00	C 5 5	35	35	35
8 7 DEL	7F	7F	7F	0 5 5	35	25	00	C 6 3	36	36	36
D 7	KF	Control	KF	0 6 6	36	5E	00	C 7 7	37	37	37
2 1 A	61	41	01	0 7 7	37	26	00	C 8 8	38	38	38
4 3 S	73	53	13	0 8 8	38	2A	00	C 9 9	39	39	39
2 4 D	64	44	04	0 9 9	39	28	00	8 6 Break Int	LF	Break Interrupt(NMI)	LF
2 6 F	66	46	06	0 0 0	30	29	00		LF		LF
2 7 G	67	47	07	5 7 -	2D	5F	00				
3 0 H	68	48	08	6 5 =	3D	2B	00				
3 2 J	6A	4A	0A	6 0 '	60	7E	1E				
3 3 K	6B	4B	0B	8 0 Bksp	08	08	08				
3 4 L	6C	4C	0C	B 4 ↑	LF	One Up	LF				
6 3 ;	3B	3A	00	9 0 F1	F1	F5	**				
6 2 '	27	22	00	9 1 F2	F2	F6	**		Legend	Key Up	Key Down
5 5]	5D	7D	1D	9 2 F3	F3	F7	**	F7	Local	On Line	Local
8 5 Return	0D	0D	0D	9 3 F4	F4	F8	**	F0	Scroll	Page Mode	Scroll
B 2 →	LF	One Right	LF	9 5 Tab Set	LF Tab Set	LF Tab Clr	**	F6	Xprnt	Normal Mode	Xprnt
8 1 Tab	0.9	LF Back Tab	**	9 6 Clr Pg	LF	Clear Pg	LF	F1	Block	Char.	Block
4 1 G	71	51	11	9 7 Clr EOP	LF	Clear/End of Page	LF				

LF = Local Function
KF = Keyboard Function
**Control input has no effect on unmarked inputs control overrides shift

MICROPROCESSOR KEYBOARD CODING

5. Serial Input/Output

The serializing and deserializing of characters and the majority of the protocol signal generation is performed by programming of the 2651 serial I/O integrated circuits. The details of this circuit are included on the following pages.

NOTE

The 2651 is being driven in the asynchronous mode.

The output control register contains bits which allow the software to steer the 2651 serial output data stream to the serial I/O and/or to the peripheral I/O interface. EIA RS232 drivers and receivers are supplied as standard, a current loop may be optionally installed and switch selected. When the current loop is selected the half duplex protocol signals are forced to the enabled condition by the interface hardware.

DESCRIPTION

The Signetics 2651 PCI is a universal synchronous/asychronous data communications controller chip designed for microcomputer systems. It interfaces directly to the Signetics 2650 microprocessor and may be used in a polled or interrupt driven system environment. The 2651 accepts programmed instructions from the microprocessor and supports many serial data communication disciplines, synchronous and asynchronous, in the full or half-duplex mode.

The PCI serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

The 2651 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode.

The PCI is constructed using Signetics n-channel silicon gate depletion load technology and is packaged in a 28-pin DIP.

FEATURES

- **Synchronous operation**
  - **5 to 8-bit characters**
  - **Single or double SYN operation**
  - **Internal character synchronization**
  - **Transparent or non-transparent mode**
  - **Automatic SYN or DLE-SYN insertion**
  - **SYN or DLE stripping**
  - **Odd, even, or no parity**
  - **Local or remote maintenance loop back mode**
  - **Baud rate: dc to 0.8M baud (1X clock)**
- **Asynchronous operation**
  - **5 to 8-bit characters**
  - **1, 1 1/2 or 2 stop bits**
  - **Odd, even, or no parity**
  - **Parity, overrun and framing error detection**
  - **Line break detection and generation**
  - **False start bit detection**
  - **Automatic serial echo mode**
  - **Local or remote maintenance loop back mode**
  - **Baud rate: dc to 0.8M baud (1X clock)**
    - **dc to 50K baud (16X clock)**
    - **dc to 12.5K baud (64X clock)**

OTHER FEATURES

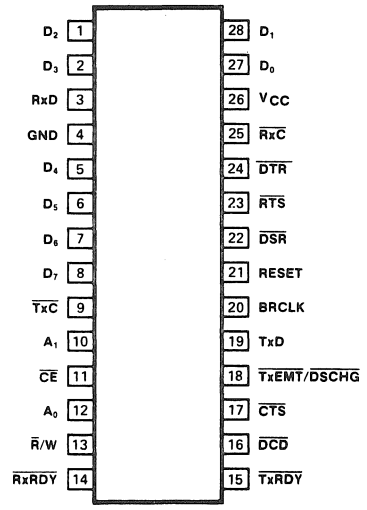
- **Internal or external baud rate clock**
- **16 internal rates-50 to 19,200 baud**
- **Double buffered transmitter and receiver**
- **Full or half duplex operation**
- **Fully compatible with 2650 CPU**
- **TTL compatible inputs and outputs**
- **Single 5V power supply**
- **No system clock required**
- **28-pin dual in-line package**

APPLICATIONS

- **Intelligent terminals**
- **Network processors**
- **Front end processors**
- **Remote data concentrators**
- **Computer to computer links**
- **Serial peripherals**

PIN CONFIGURATION

I PACKAGE



PIN DESIGNATION

PIN NO.	SYMBOL	NAME & FUNCTION	TYPE
27,28,1,2, 5-8	D_0-D_7	8-bit data bus	I/O
21	RESET	Reset	I
12,10	A_0-A_1	Internal register select lines	I
13	$\overline{R}$/W	Read or write command	I
11	$\overline{CE}$	Chip enable input	I
22	$\overline{DSR}$	Data set ready	I
24	$\overline{DTR}$	Data terminal ready	O
23	$\overline{RTS}$	Request to send	O
17	$\overline{CTS}$	Clear to send	I
16	$\overline{DCD}$	Data carrier detected	I
18	$\overline{TxEMT/DSCHG}$	Transmitter empty or data set change	O
9	$\overline{TxC}$	Transmitter clock	I/O
25	$\overline{RxC}$	Receiver clock	I/O
19	TxD	Transmitter data	O
3	RxD	Receiver data	I
15	$\overline{TxRDY}$	Transmitter ready	O
14	$\overline{RxRDY}$	Receiver ready	O
20	BRCLK	Baud rate generator clock	I
26	V_{CC}	+5V supply	I
4	GND	Ground	I

BLOCK DIAGRAM

The PCI consists of six major sections. These are the transmitter, receiver, timing, operation control, modem control and SYN/DLE control. These sections communicate with each other via an internal data bus and an internal control bus. The internal data bus interfaces to the microprocessor data bus via a data bus buffer.

Operation Control

This functional block stores configuration and operation commands from the CPU and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with the microprocessor via the data bus and contains Mode Registers 1 and 2, the Command Reg-

Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
50	0.8 KHz	0.8 KHz	--	50/50	6336
75	1.2	1.2	--	50/50	4224
110	1.76	1.76	--	50/50	2880
134.5	2.152	2.1523	0.016	50/50	2355
150	2.4	2.4	--	50/50	2112
300	4.8	4.8	--	50/50	1056
600	9.6	9.6	--	50/50	528
1200	19.2	19.2	--	50/50	264
1800	28.8	28.8	--	50/50	176
2000	32.0	32.081	0.253	50/50	158
2400	38.4	38.4	--	50/50	132
3600	57.6	57.6	--	50/50	88
4800	76.8	76.8	--	50/50	66
7200	115.2	115.2	--	50/50	44
9600	153.6	153.6	--	48/52	33
19200	307.2	316.8	3.125	50/50	16

NOTE

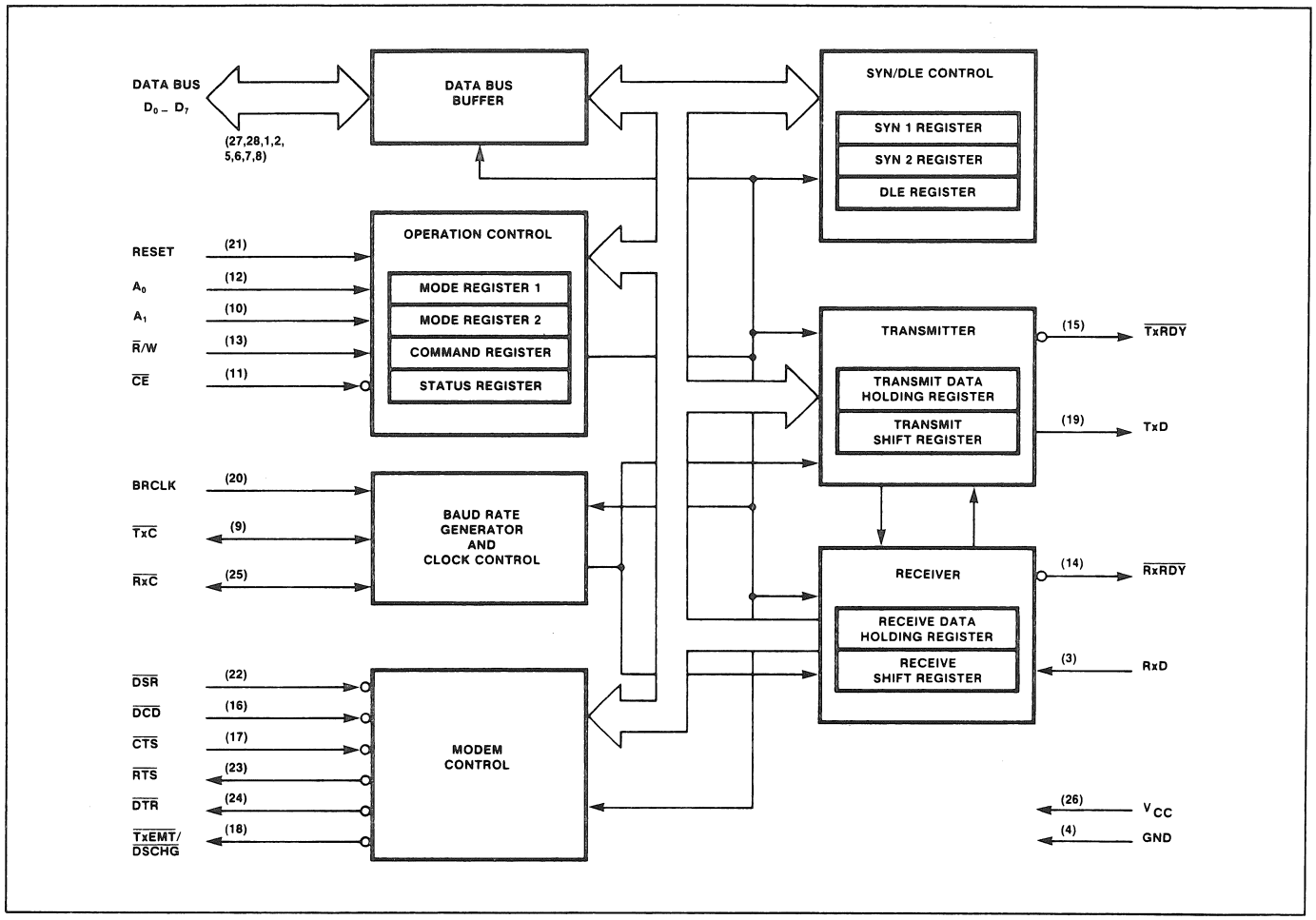
16X clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1X and duty cycle is 50%/50% for any baud rate.

Table 1 BAUD RATE GENERATOR CHARACTERISTICS
Crystal Frequency = 5.0688MHz

PIN NAME	PIN NO.	INPUT/OUTPUT	FUNCTION
V_{CC}	26	I	+5V supply input
GND	4	I	Ground
RESET	21	I	A high on this input performs a master reset on the 2651. This signal asynchronously terminates any device activity and clears the Mode, Command and Status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.
A_1-A_0	10,12	I	Address lines used to select internal PCI registers.
$\overline{R}/W$	13	I	Read command when low, write command when high.
$\overline{CE}$	11	I	Chip enable command. When low, indicates that control and data lines to the PCI are valid and that the operation specified by the $\overline{R}/W$, A_1 and A_0 inputs should be performed. When high, places the D_0-D_7 lines in the tri-state condition.
D_7-D_0	8,7,6,5, 2,1,28,27	I/O	8-bit, three-state data bus used to transfer commands, data and status between PCI and the CPU. D_0 is the least significant bit; D_7 the most significant bit.
$\overline{TxRDY}$	15	O	This output is the complement of Status Register bit SR0. When low, it indicates that the Transmit Data Holding Register (THR) is ready to accept a data character from the CPU. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{RxRDY}$	14	O	This output is the complement of Status Register bit SR1. When low, it indicates that the Receive Data Holding Register (RHR) has a character ready for input to the CPU. It goes high when the RHR is read by the CPU, and also when the receiver is disabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{TxEMT}/\overline{DSCHG}$	18	O	This output is the complement of Status Register bit SR2. When low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. This output goes high when the Status Register is read by the CPU, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the CPU for this line to go high. It is an open drain output which can be used as an interrupt to the CPU.

Table 2 CPU-RELATED SIGNALS

BLOCK DIAGRAM



ister, and the Status Register. Details of register addressing and protocol are presented in the PCI PROGRAMMING section of this data sheet.

Timing

The PCI contains a Baud Rate Generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full duplex operation. See Table 1.

Receiver

The Receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU.

Transmitter

The Transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

Modem Control

The modem control section provides interfacing for three input signals and three output signals used for "handshaking" and status indication between the CPU and a modem.

SYN/DLE Control

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the CPU. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

INTERFACE SIGNALS

The PCI interface signals can be grouped into two types: the CPU-related signals (shown in Table 2), which interface the 2651 to the microprocessor system, and the device-related signals (shown in Table 3), which are used to interface to the communications device or system.

OPERATION

The functional operation of the 2651 is programmed by a set of control words supplied by the CPU. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc. The programming procedure is described in the PCI PROGRAMMING section of this data sheet.

After programming, the PCI is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the CPU to a serial bit stream. These actions are accomplished within the framework specified by the control words.

Receiver

The 2651 is conditioned to receive data when the $\overline{DCD}$ input is low and the RxEN bit in the command register is true. In the asynchronous mode, the receiver looks for

PIN NAME	PIN NO.	INPUT/OUTPUT	FUNCTION
BRCLK	20	I	5.0688MHz clock input to the internal baud rate generator. Not required if external receiver and transmitter clocks are used.
$\overline{RxC}$	25	I/O	Receiver clock. If external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X or 64X the baud rate, as programmed by Mode Register 1. Data is sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin becomes an output at 1X the programmed baud rate.
$\overline{TxC}$	9	I/O	Transmitter clock. If external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X or 64X the baud rate, as programmed by Mode Register 1. The transmitted data changes on the falling edge of the clock. If internal transmitter clock is programmed, this pin becomes an output at 1X the programmed baud rate.
RxD	3	I	Serial data input to the receiver. "Mark" is high, "Space" is low.
TxD	19	O	Serial data output from the transmitter. "Mark" is high, "Space" is low. Held in Mark condition when the transmitter is disabled.
$\overline{DSR}$	22	I	General purpose input which can be used for Data Set Ready or Ring Indicator condition. Its complement appears as Status Register bit SR7. Causes a low output on $\overline{TxEMT/DSCHG}$ when its state changes.
$\overline{DCD}$	16	I	Data Carrier Detect input. Must be low in order for the receiver to operate. Its complement appears as Status Register bit SR6. Causes a low output on $\overline{TxEMT/DSCHG}$ when its state changes.
$\overline{CTS}$	17	I	Clear to Send input. Must be low in order for the transmitter to operate.
$\overline{DTR}$	24	O	General purpose output which is the complement of Command Register bit CR1. Normally used to indicate Data Terminal Ready.
$\overline{RTS}$	23	O	General purpose output which is the complement of Command Register bit CR5. Normally used to indicate Request to Send.

Table 3 DEVICE-RELATED SIGNALS

a high to low transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and the stop bit(s) have been assembled. The data is then transferred to the Receive Data Holding Register, the RxRDY bit in the status register is set, and the $\overline{RxRDY}$ output is asserted. If the character length is less than 8 bits, the high order unused bits in the Holding Register are set to zero. The Parity Error, Framing Error, and Overrun Error status bits are set if required. If a break condition is detected (RxD is low for the entire character as well as the stop bit [s]), only one character consisting of all zeros (with the FE status bit set) will be transferred to the Holding Register. The RxD input must return to a high condition before a search for the next start bit begins.

When the PCI is initialized into the synchronous mode, the receiver first enters the hunt mode. In this mode, as data is shifted into the Receiver Shift Register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly mode begins. If single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise, the PCI returns to the hunt mode. (Note that the sequence SYN1-SYN1-SYN2 will not achieve synchronization). When synchronization has been achieved, the PCI continues to assemble characters and transfer them to the Holding Register, setting the RxRDY status bit and asserting the $\overline{RxRDY}$ output each time a character is transferred. The PE and OE status bits are set as appropriate. Further receipt of the appropriate SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the Holding Register. Note that the SYN characters used to establish initial synchronization are not transferred to the Holding Register in any case.

Transmitter

The PCI is conditioned to transmit data when the $\overline{CTS}$ input is low and the TxEN command register bit is set. The 2651 indicates to the CPU that it can accept a character for transmission by setting the TxRDY status bit and asserting the $\overline{TxRDY}$ output. When the CPU writes a character into the Transmit Data Holding Register, these conditions are negated. Data is transferred from the Holding Register to the Transmit Shift Register when it is idle or has completed transmission of the previous character. The TxRDT conditions are then asserted again. Thus, one full character time of buffering is provided.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the stop bits, a new character is not available in the Transmit Holding Register, the TxD output remains in the marking (high) condition and the $\overline{TxEMT/DSCHG}$ output and its corresponding status bit are asserted. Transmission resumes when the CPU loads a new character into the Holding Register. The transmitter can be forced to output a continuous low (BREAK) condition by setting the Send Break command bit high.

In the synchronous mode, when the 2651 is initially conditioned to transmit, the TxD output remains high and the TxRDY condition is asserted until the first character to be transmitted (usually a SYN character) is loaded by the CPU. Subsequent to this, a continuous stream of characters is transmitted. No extra bits (other than parity, if commanded) are generated by the PCI

unless the CPU fails to send a new character to the PCI by the time the transmitter has completed sending the previous character. Since synchronous communications does not allow gaps between characters, the PCI asserts TxEMT and automatically "fills" the gap by transmitting SYN1s, SYN1-SYN2 doublets, or DLE-SYN1 doublets, depending on the command mode. Normal transmission of the message resumes when a new character is available in the Transmit Data Holding Register. If the SEND DLE bit in the command register is true, the DLE character is automatically transmitted prior to transmission of the message character.

PCI PROGRAMMING

Prior to initiating data communications, the 2651 operational mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The PCI can be reconfigured at any time during program execution. However, the receiver and transmitter should be disabled if the change has an effect on the reception or transmission of a character. A flowchart of the initialization process appears in Figure 1.

The internal registers of the PCI are accessed by applying specific signals to the CE, $\overline{R}/W$, A_1 and A_0 inputs. The conditions necessary to address each register are shown in Table 4.

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions $A_1=0$, $A_0=1$, and $\overline{R}/W=1$. The first operation loads the SYN1 register. The next loads the SYN2 register, and the third loads the DLE register. Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses Mode Register 1, and a subsequent operation addresses Mode Register 2. If more than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 Register and Mode Register 1 by a RESET input or by performing a "Read Command Register" operation, but are unaffected by any other read or write operation.

The 2651 register formats are summarized in Tables 5, 6, 7 and 8. Mode Registers 1 and 2 define the general operational characteristics of the PCI, while the Command Register controls the operation within this basic frame-work. The PCI indicates its status in the Status Register. These registers are cleared when a RESET input is applied.

2651 INITIALIZATION FLOW CHART

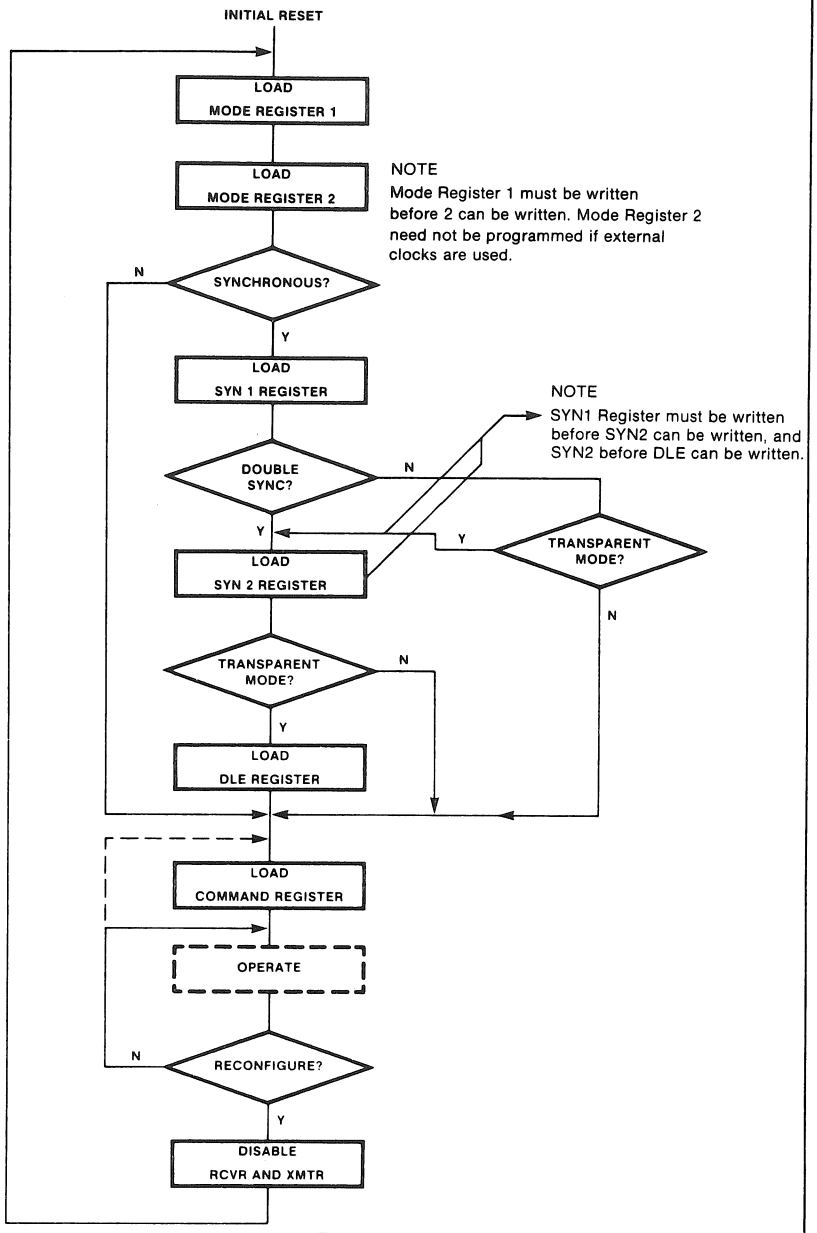


Figure 1

$\overline{CE}$	A_1	A_0	$\overline{R}/W$	FUNCTION
1	X	X	X	Tri-state data bus
0	0	0	0	Read receive holding register
0	0	0	1	Write transmit holding register
0	0	1	0	Read status register
0	0	1	1	Write SYN1/SYN2/DLE registers
0	1	0	0	Read mode registers 1/2
0	1	0	1	Write mode registers 1/2
0	1	1	0	Read command register
0	1	1	1	Write command register

NOTE
See AC Characteristics section for timing requirements.

Table 4 2651 REGISTER ADDRESSING

MR17	MR16	MR15	MR14	MR13	MR12	MR11	MR10
		Parity Type	Parity Control	Character Length		Mode and Baud Rate Factor	
ASYNCH: STOP BIT LENGTH 00 = INVALID 01 = 1 STOP BIT 10 = 1 1/2 STOP BITS 11 = 2 STOP BITS		0 = ODD 1 = EVEN	0 = DISABLED 1 = ENABLED	00 = 5 BITS 01 = 6 BITS 10 = 7 BITS 11 = 8 BITS		00 = SYNCHRONOUS 1X RATE 01 = ASYNCHRONOUS 1X RATE 10 = ASYNCHRONOUS 16X RATE 11 = ASYNCHRONOUS 64X RATE	
SYNCH: NUMBER OF SYN CHAR 0 = DOUBLE SYN 1 = SINGLE SYN	SYNCH: TRANSPARENCY CONTROL 0 = NORMAL 1 = TRANSPARENT						

NOTE
Baud rate factor in asynchronous applies only if external clock is selected. Factor is 16X if internal clock is selected.

Table 5 MODE REGISTER 1 (MR1)

MR27	MR26	MR25	MR24	MR23	MR22	MR21	MR20
		Transmitter Clock	Receiver Clock	Baud Rate Selection			
NOT USED		0 = EXTERNAL 1 = INTERNAL	0 = EXTERNAL 1 = INTERNAL	0000 = 50 BAUD 0001 = 75 0010 = 110 0011 = 134.5 0100 = 150 0101 = 300 0110 = 600 0111 = 1200		1000 = 1800 BAUD 1001 = 2000 1010 = 2400 1011 = 3600 1100 = 4800 1101 = 7200 1110 = 9600 1111 = 19,200	

Table 6 MODE REGISTER 2 (MR2)

Mode Register 1 (MR1)

Table 5 illustrates Mode Register 1. Bits MR11 and MR10 select the communication format and baud rate multiplier. 00 specifies synchronous mode and 1X multiplier. 1X, 16X, and 64X multipliers are programmable for asynchronous format. However, the multiplier in asynchronous format applies only if the external clock input option is selected by MR24 or MR25.

MR13 and MR12 select a character length of 5, 6, 7, or 8 bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits in asynchronous mode.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14.

In asychronous mode, MR17 and MR16 select character framing of 1, 1.5, or 2 stop bits. (If 1X baud rate is programmed, 1.5 stop bits defaults to 2 stop bits on transmit). In synchronous mode, MR17 controls the number of SYN characters used to establish synchronization and for character fill when the transmitter is idle. SYN1 alone is used if MR17 = 1, and SYN1-SYN2 is used when MR17 = 0. If the transparent mode is specified by MR16, DLE-SYN1 is used for character fill, but the normal synchronization sequence is used.

Mode Register 2 (MR2)

Table 6 illustrates Mode Register 2. MR23, MR22, MR21, and MR20 control the frequency of the internal baud rate generator (BRG). Sixteen rates are selectable. When driven by a 5.0688 MHz input at the BRCLK input (pin 20), the BRG output has zero error except at 134.5, 2000, and 19,200 baud, which have errors of +0.016%, +0.235%, and +3.125% respectively. The clock supplied to the receiver and transmitter (as selected by MR24 and MR25) has a 50%/50% duty cycle except in asynchronous mode, at 9600 baud, where the duty cycle is 48%/52%.

MR25 and MR24 select either the BRG or the external inputs TxC and RxC as the clock source for the transmitter and receiver, respectively. If the BRG clock is selected, the baud rate factor in asynchronous mode is 16X regardless of the factor selected by MR11 and MR10. In addition, the corresponding clock pin provides an output at 1X the baud rate.

Command Register (CR)

Table 7 illustrates Command Register. Bits CRO (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. If the transmitter is disabled, it will complete the transmission of the character in the Transmit Shift Register (if any) prior to terminating operation. The TxD output will then remain in the marking state (high). If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be neglected.

Bits CR1 (DTR) and CR5 (RTS) control the $\overline{\text{DTR}}$ and $\overline{\text{RTS}}$ outputs. Data at the outputs is the logical complement of the register data.

In asynchronous mode, setting CR3 will force and hold the TxD output low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The TxD line will go high for a least one bit time before beginning transmission of the next character in the Transmit Data Holding Register. In synchronous mode, setting CR3 causes the transmission of the DLE register contents prior to sending the character in the Transmit Data Holding Register. CR3 should be reset in response to the next TxRDY.

Setting CR4 causes the error flags in the Status Register (SR3, SR4, and SR5) to be

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Operating Mode		Request to Send	Reset Error		Receive Control (RxEN)	Data Terminal Ready	Transmit Control (TxEN)
00 = NORMAL OPERATION 01 = ASYNCH: AUTOMATIC ECHO MODE SYNCH: SYN AND/OR DLE STRIPPING MODE 10 = LOCAL LOOP BACK 11 = REMOTE LOOP BACK		0 = FORCE $\overline{RTS}$ OUTPUT HIGH 1 = FORCE $\overline{RTS}$ OUTPUT LOW	0 = NORMAL 1 = RESET ERROR FLAG IN STATUS REG (FE, OE, PE/DLE DETECT)	**ASYNCH: FORCE BREAK** 0 = NORMAL 1 = FORCE BREAK **SYNCH: SEND DLE** 0 = NORMAL 1 = SEND DLE	0 = DISABLE 1 = ENABLE	0 = FORCE $\overline{DTR}$ OUTPUT HIGH 1 = FORCE $\overline{DTR}$ OUTPUT LOW	0 = DISABLE 1 = ENABLE

Table 7 COMMAND REGISTER (CR)

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
Data Set Ready	Data Carrier Detect	FE/SYN Detect	Overrrun	PE/DLE Detect	TxEMT/DSCHG	RxRDY	TxRDY
0 = $\overline{DSR}$ INPUT IS HIGH 1 = $\overline{DSR}$ INPUT IS LOW	0 = $\overline{DCD}$ INPUT IS HIGH 1 = $\overline{DCD}$ INPUT IS LOW	**ASYNCH:** 0 = NORMAL 1 = FRAMING ERROR **SYNCH:** 0 = NORMAL 1 = SYN CHAR DETECTED	0 = NORMAL 1 = OVERRUN ERROR	**ASYNCH:** 0 = NORMAL 1 = PARITY ERROR **SYNCH:** 0 = NORMAL 1 = PARITY ERROR OR DLE CHAR RECEIVED	0 = NORMAL 1 = CHANGE IN $\overline{DSR}$ OR $\overline{DCD}$, OR TRANSMIT SHIFT REGISTER IS EMPTY	0 = RECEIVE HOLDING REG EMPTY 1 = RECEIVE HOLDING REG HAS DATA	0 = TRANSMIT HOLDING REG BUSY 1 = TRANSMIT HOLDING REG EMPTY

Table 8 STATUS REGISTER (SR)

cleared. This bit resets automatically.

The PCI can operate in one of four sub-modes within each major mode (synchronous or asynchronous). The operational sub-mode is determined by CR7 and CR6. CR7-CR6 = 00 is the normal mode, with the transmitter and receiver operating independently in accordance with the Mode and Status Register instructions.

In asynchronous mode, CR7-CR6 = 01 places the PCI in the Automatic Echo mode. Clocked, regenerated received data is automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2 = 1), but the transmitter need not be enabled. CPU to receiver communications continues normally, but the CPU to transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected. The following conditions are true while in Automatic Echo mode:

1. Data assembled by the receiver is automatically placed in the Transmit Holding Register and retransmitted by the transmitter on the TxD output.
2. Transmit clock = receive clock.
3. $\overline{TxRDY}$ output = 1.
4. The $\overline{TxEMT/DSCHG}$ pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In synchronous mode, CR7-CR6 = 01 places the PCI in the Automatic SYN/DLE Stripping mode. The exact action taken depends on the setting of bits MR17 and MR16:

1. In the non-transparent, single SYN mode (MR17-MR16 = 10), characters in the data stream matching SYN1 are not transferred to the Receive Data Holding Register (RHR).
2. In the non-transparent, double SYN mode (MR17-MR16 = 00), characters in the data stream matching SYN1, or SYN2 if immediately preceded by SYN1, are not transferred to the RHR. However, only the first SYN1 of an SYN1-SYN1 pair is stripped.
3. In transparent mode (MR16 =1), characters in the data stream matching DLE, or SYN1 if immediately preceded by DLE, are not transferred to the RHR. However, only the first DLE of a DLE-DLE pair is stripped.

Note that Automatic Stripping mode does not affect the setting of the DLE Detect and SYN Detect status bits (SR3 and SR5).

Two diagnostic sub-modes can also be configured. In Local Loop Back mode (CR7-CR6 = 10), the following loops are connected internally:

1. The transmitter output is connected to the receiver input.
2. $\overline{DTR}$ is connected to $\overline{DCD}$ and $\overline{RTS}$ is connected to $\overline{CTS}$.
3. Receive clock = transmit clock.
4. The $\overline{DTR}$, $\overline{RTS}$ and $\overline{TxD}$ outputs are held high.
5. The $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ and RxD inputs are ignored.

Additional requirements to operate in the Local Loop Back mode are that CR0 (TxEN), CR1 (DTR), and CR5 (RTS) must be set to 1. CR2 (RxEN) is ignored by the PCI.

The second diagnostic mode is the Remote Loop Back mode (CR7-CR6 = 11). In this mode:

1. Data assembled by the receiver is automatically placed in the Transmit Holding Register and retransmitted by the transmitter on the TxD output.
2. Transmit clock = receive clock.
3. No data is sent to the local CPU, but the error status conditions (PE, OE, FE) are set.
4. The $\overline{RxRDY}$, $\overline{TxRDY}$, and $\overline{TxEMT/DSCHG}$ outputs are held high.
5. CR1 (TxEN) is ignored.
6. All other signals operate normally.

Status Register

The data contained in the Status Register (as shown in Table 8) indicate receiver and transmitter conditions and modem/data set status.

SR0 is the Transmitter Ready (TxRDY) status bit. It, and its corresponding output, are valid only when the transmitter is enabled. If equal to 0, it indicates that the Transmit Data Holding Register has been loaded by the CPU and the data has not been transferred to the Transmit Shift Register. If set equal to 1, it indicates that the Holding Register is ready to accept data from the CPU. This bit is initially set when the Transmitter is enabled by CR0, unless a character has previously been loaded into the Holding Register. It is not set when the Automatic Echo or Remote Loop Back modes are programmed. When this bit is set, the $\overline{\text{TxRDY}}$ output pin is low. In the Automatic Echo and Remote Loop Back modes, the output is held high.

SR1, the Receiver Ready (RxRDY) status bit, indicates the condition of the Receive Data Holding Register. If set, it indicates that a character has been loaded into the Holding Register from the Receive Shift Register and is ready to be read by the CPU. If equal to zero, there is no new character in the Holding Register. This bit is cleared when the CPU reads the Receive Data Holding Register or when the receiver is disabled by CR2. When set, the $\overline{\text{RxRDY}}$ output is low.

The TxEMT/DSCHG bit, SR2, when set, indicates either a change of state of the $\overline{\text{DSR}}$ or $\overline{\text{DCD}}$ inputs or that the Transmit Shift Register has completed transmission of a character and no new character has been loaded into the Transmit Data Holding Register. Note that in synchronous mode this bit will be set even though the appropriate "fill" character is transmitted. It is cleared when the transmitter is enabled by CR0 and does not indicate transmitter condition until at least one character is transmitted. It is also cleared when the Status Register is read by the CPU. When SR2 is set, the $\overline{\text{TxEMT}}$/$\overline{\text{DSCHG}}$ output is low.

SR3, when set, indicates a received parity error when parity is enabled by MR14. In synchronous transparent mode (MR16 = 1), with parity disabled, it indicates that a character matching the DLE Register has been received. However, only the first DLE of two successive DLEs will set SR3. This bit is cleared when the receiver is disabled and by the Reset Error command, CR4.

The Overrun Error status bit, SR4, indicates that the previous character loaded into the Receive Holding Register was not read by the CPU at the time a new received character was transferred into it. This bit is cleared when the receiver is disabled and by the Reset Error command, CR4.

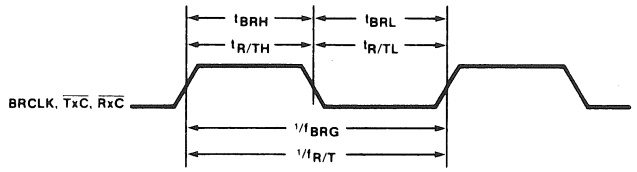
In asynchronous mode, bit SR5 signifies that the received character was not framed by the programmed number of stop bits. (If 1.5 stop bits are programmed, only the first stop bit is checked.) In synchronous non-transparent mode (MR16 = 0), it indicates receipt of the SYN1 character is single SYN mode or the SYN1-SYN2 pair in double SYN mode. In synchronous transparent mode (MR16 = 1), this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1-SYN2) and, after synchronization has been achieved, when a DLE-SYN1 pair is received. The bit is reset when the receiver is disabled, when the Reset Error command is given in asynchronous mode, and when the Status Register is read by the CPU in the synchronous mode.

$\overline{\text{SR6}}$ and $\overline{\text{SR7}}$ reflect the conditions of the $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ inputs respectively. A low input sets its corresponding status bit and a high input clears it.

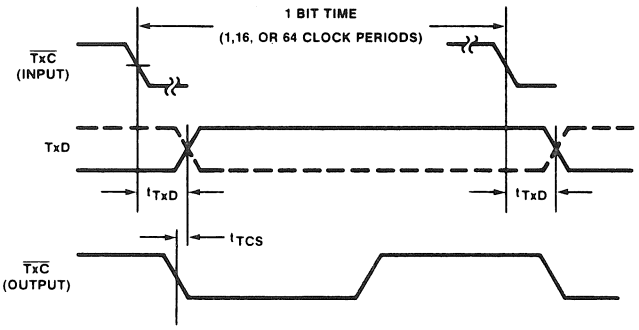
TIMING DIAGRAMS

RESET

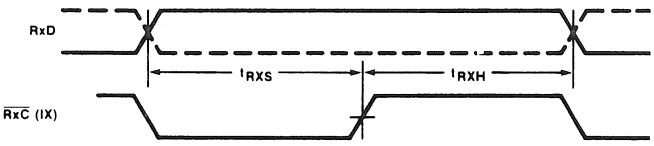
CLOCK



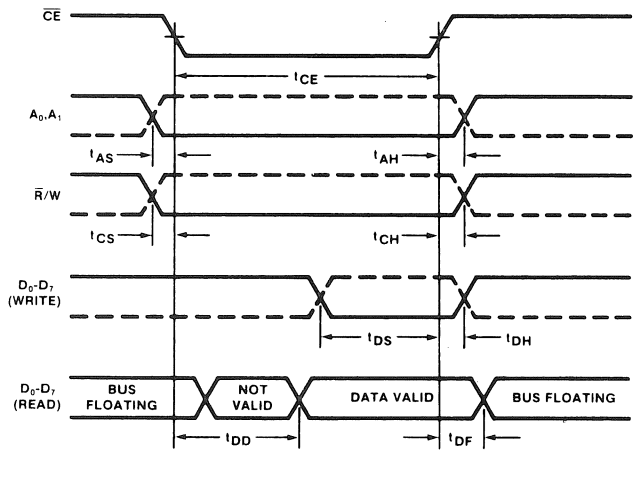
TRANSMIT



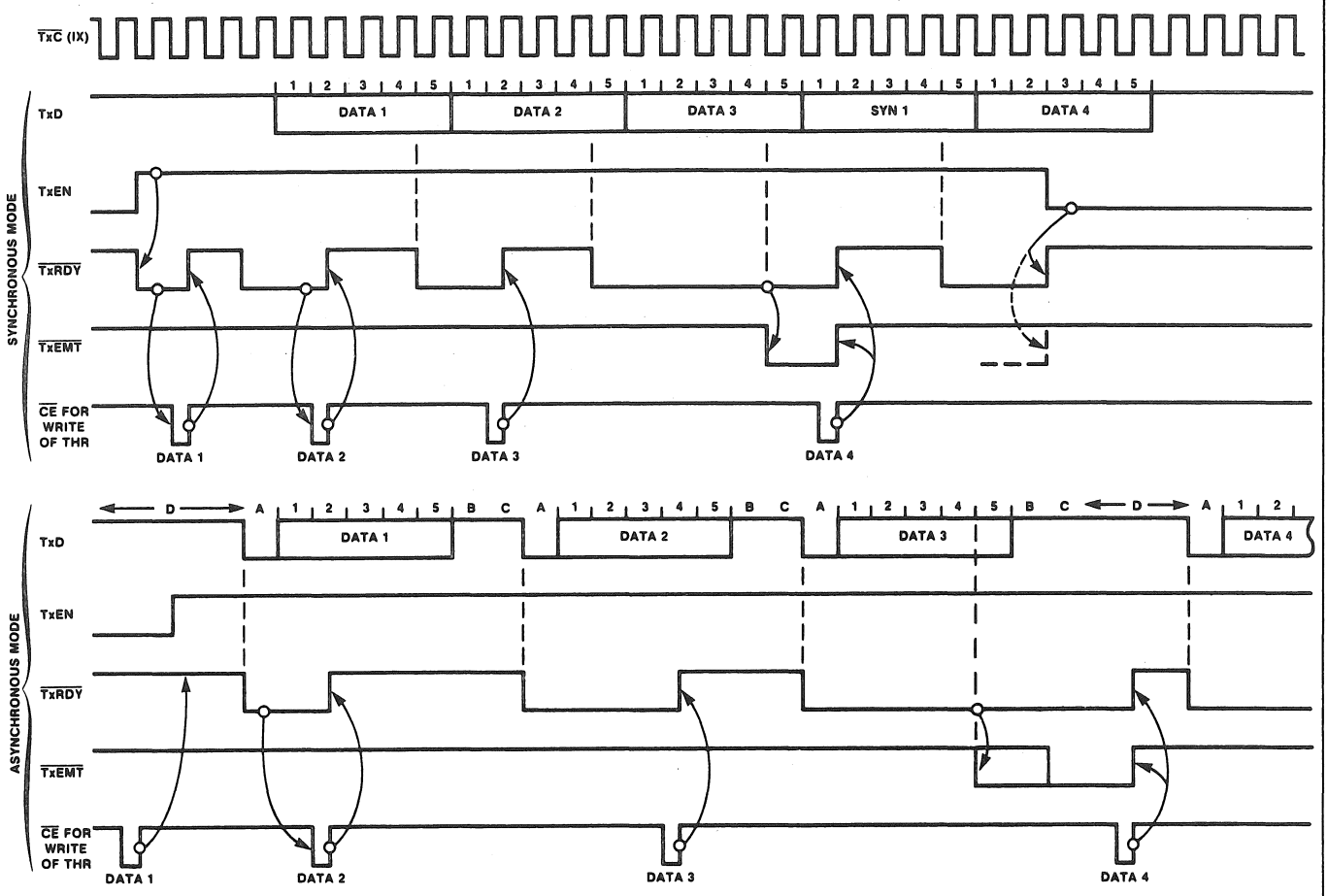
RECEIVE



READ AND WRITE



TxRDY, TxEMT (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



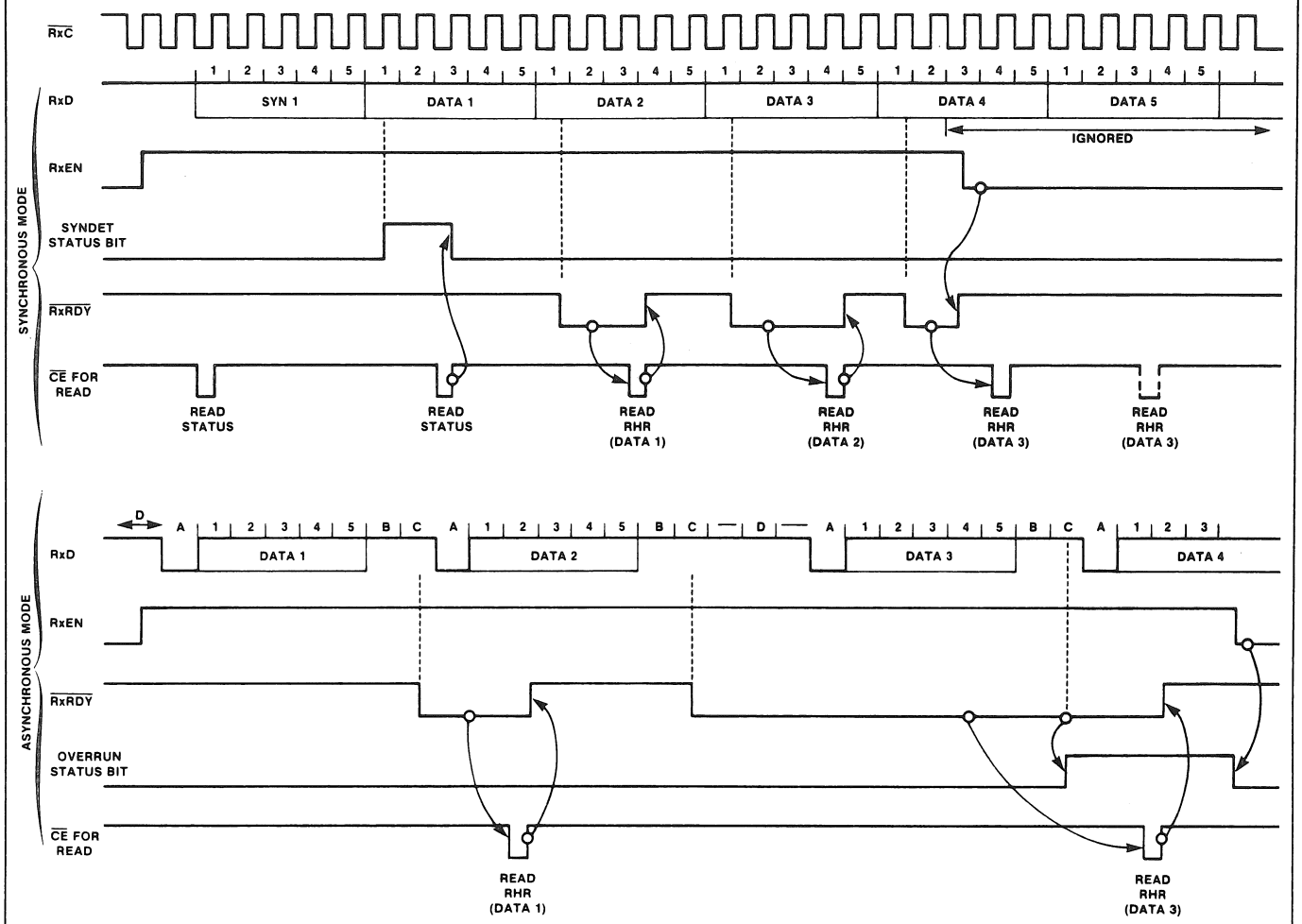
NOTES

A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition

TxEMT goes low at the beginning of the last data bit, or, if parity is enabled, at the beginning of the parity bit.

TIMING DIAGRAMS (Cont'd)

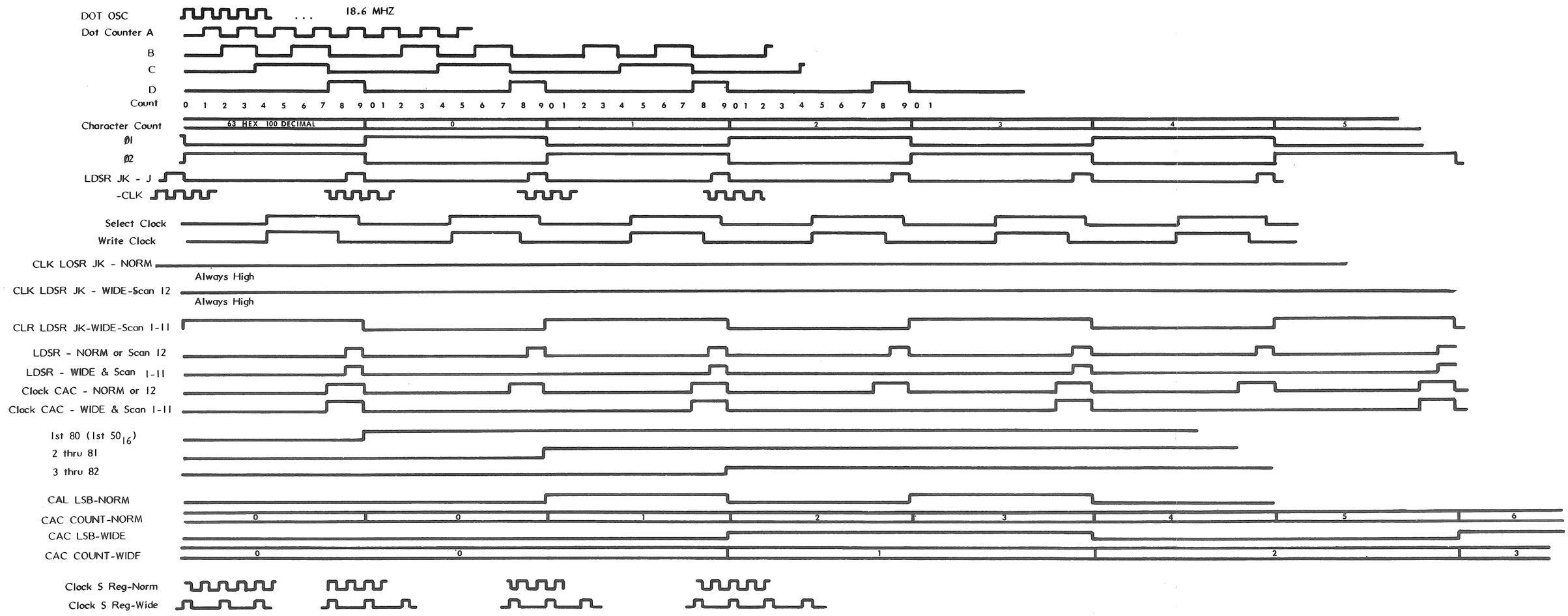
RxRDY (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])

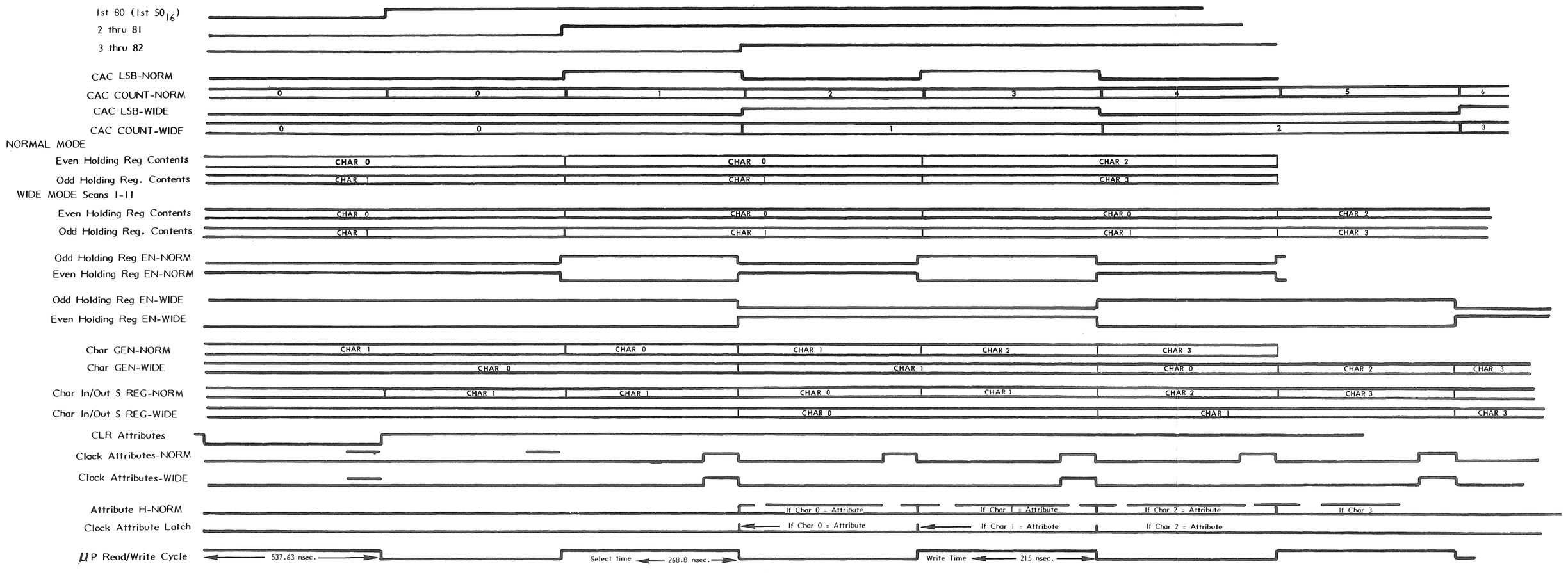


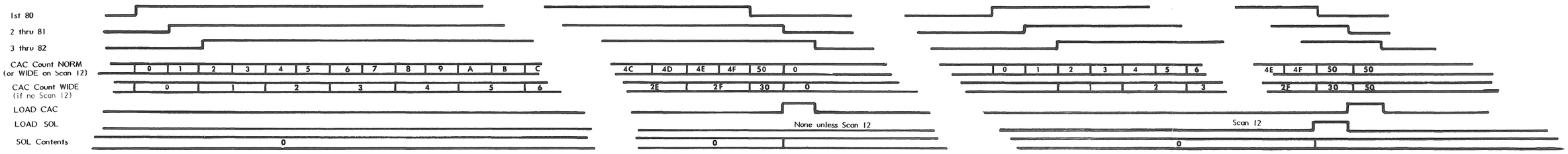
NOTES

A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition

C. TIMING CHARTS


DOT OSC
18.6 MHZ
Dot Counter A
B
C
D
Count
0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1
Character Count
63 HEX 100 DECIMAL
0
1
2
3
4
5
Ø1
Ø2
LDSR JK - J
-CLK
Select Clock
Write Clock
CLK LOSR JK - NORM
Always High
CLK LDSR JK - WIDE-Scan 12
Always High
CLR LDSR JK-WIDE-Scan 1-11
LDSR - NORM or Scan 12
LDSR - WIDE & Scan 1-11
Clock CAC - NORM or 12
Clock CAC - WIDE & Scan 1-11
1st 80 (1st 50_{16})
2 thru 81
3 thru 82
CAL LSB-NORM
CAC COUNT-NORM
0 0 1 2 3 4 5 6
CAC LSB-WIDE
CAC COUNT-WIDE
0 0 1 2 3
Clock S Reg-Norm
Clock S Reg-Wide


1st 80 (1st 50$_{16}$)
2 thru 81
3 thru 82
CAC LSB-NORM
CAC COUNT-NORM
0 0 1 2 3 4 5 6
CAC LSB-WIDE
CAC COUNT-WIDE
0 0 1 2 3
NORMAL MODE
Even Holding Reg Contents
CHAR 0 CHAR 0 CHAR 2
Odd Holding Reg. Contents
CHAR 1 CHAR 1 CHAR 3
WIDE MODE Scans 1-11
Even Holding Reg Contents
CHAR 0 CHAR 0 CHAR 0 CHAR 2
Odd Holding Reg. Contents
CHAR 1 CHAR 1 CHAR 1 CHAR 3
Odd Holding Reg EN-NORM
Even Holding Reg EN-NORM
Odd Holding Reg EN-WIDE
Even Holding Reg EN-WIDE
Char GEN-NORM
CHAR 1 CHAR 0 CHAR 1 CHAR 2 CHAR 3
Char GEN-WIDE
CHAR 0 CHAR 1 CHAR 0 CHAR 2 CHAR 3
Char In/Out S REG-NORM
CHAR 1 CHAR 1 CHAR 0 CHAR 1 CHAR 2 CHAR 3
Char In/Out S REG-WIDE
CHAR 0 CHAR 1 CHAR 3
CLR Attributes
Clock Attributes-NORM
Clock Attributes-WIDE
Attribute H-NORM
If Char 0 = Attribute
If Char 1 = Attribute
If Char 2 = Attribute
If Char 3
Clock Attribute Latch
If Char 0 = Attribute
If Char 1 = Attribute
If Char 2 = Attribute
μP Read/Write Cycle
537.63 nsec.
Select time
268.8 nsec.
Write Time
215 nsec.


1st 80
2 thru 81
3 thru 82
CAC Count NORM
(or WIDE on Scan 12)
0 1 2 3 4 5 6 7 8 9 A B C
4C 4D 4E 4F 50 0
0 1 2 3 4 5 6
4E 4F 50 50
CAC Count WIDE
(if no Scan 12)
0 1 2 3 4 5 6
2E 2F 30 0
1 2 3
2F 30 50
LOAD CAC
LOAD SOL
None unless Scan 12
Scan 12
SOL Contents
0
0
0

D. MEMORY MAPS

TABLE I

MEMORY MAP

HEX		ADDR	
FC00	thru	FFFF	PROM FC00 (-1)
F800	thru	FBFF	PROM F800 (-2)
F400	thru	F7FF	PROM F400 (-3)
F000	thru	F3FF	PROM F000 (-4)
0C00	thru	0FFF	PROM 0C00 (-5)
0B80	thru	0BFF	RAM - Software use
0400	thru	0B7F	DISPLAY RAM organized 24 lines of 80 (50_{16}) Line 1 (Top of Screen) = 0400 through 044F Line 24 (Bottom of Screen) = -B30 through 0B7F
0040	thru	03FF	Scratch Pad RAM - Software use - stack, function keys, etc.
0050	thru	005F	T.O.P.R. (Top of Page Register)
0040	thru	004F	OUTPUT CONTROL REGISTER (See Table 2)
0030	thru	003F	Serial I/O (See Table 3)
0020	thru	002F	Reserved for "Not-normally-installed" switch inputs
0010	thru	001F	Switch Inputs (See Table 4)
0000	thru	000F	Keyboard (See Keyboard Section)

TABLE 2

OUTPUT CONTROL REGISTER MEMORY MAP

$A_3A_2A_1A_0$	Data BUS DO = 1	Data BUS D0 = 0
X 1 1 1	ENABLE Xmit Serial I/O	DISABLE
X 1 1 0	ENABLE Xmit Periph I/O	DISABLE
X 1 0 1	RESERVED	ENABLE REV PERIPH I/O
X 1 0 0	Jam Printer Clear to Send	NORMAL CLEAR TO SEND
X 0 1 1	ENABLE DATA TERM RDY	DISABLE
X 0 1 0	ENABLE WIDE (40) MODE	ENABLE NORMAL (80) MODE
X 0 0 1	Bell OFF	Bell ON
X 0 0 0	NORMAL	RESET TIMER

TABLE 3

SERIAL I/O MEMORY MAP

$A_3A_2A_1A_0$	OPERATION	REGISTER
X X 1 1		Receive Holding Register
X X 1 0		Status Register
X X 0 1	READ	Mode Registers 1/2
X X 0 0		Command Register
X X 1 1		Transmit Holding Register
X X 1 0	WRITE	SYN1/SYN2/DLE Registers
X X 0 1		Mode Registers 1/2
X X 0 0		Command Register

TABLE 4

SWITCH MEMORY MAPS

ADDRESS (HEX)	7	6	5	4	3	2	1	0
0010	New Line	LF-NL/CR-NL	Wrap	Half/Full	Baud 2^3	Baud 2^2	Baud 2^1	Baud 2^0
0011	Stop Bits	Timer E_x	Even/Odd	Parity En	Reserved	7 or 8 bits	Xmit CSR	Xmit ETX
0020	NA	NA	NA	NA	Reserved - Hardware not installed			
0021	NA	NA	NA	NA	Reserved - Hardware not installed			

NA = Not Available

TABLE 5

SOFTWARE RAM USAGE

0B80	thru	OBFF	Programmable Function Pointers
0400	thru	0B7F	Display Memory
01F0	thru	03FF	Programmable Function Storage
0180	thru	01EF	Keyboard Counters/Registers
0140	thru	017F	Microprocessor Stack Registers
0100	thru	0135	Serial Input Buffer
0060	thru	00FF	Program Storage Register - Scratch Pad

E. Logic Module Test Points

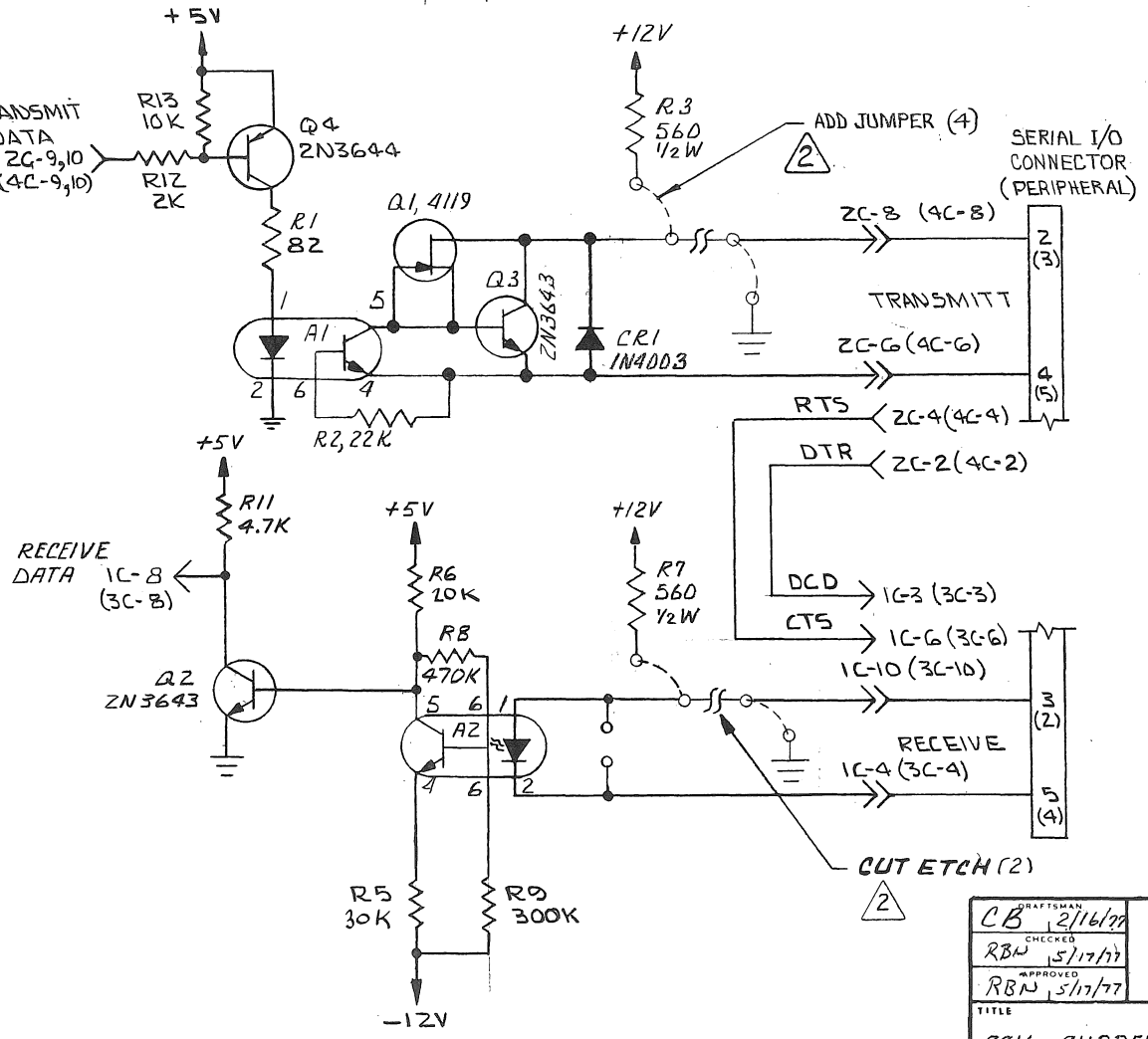
The following is a list of Test Points provided within the TELERAY and a description of the signal on each. Test points are marked on the TELERAY board by a square and the Test Point number.

Test Point	Grid Location	Description
GND	3G	This test point is ground and is provided for grounding test equipment.
1	6B	This test point is the trigger portion of the Master Reset Timer Circuitry. To initiate a Master Reset without removing power from the unit, this point can be momentarily grounded. It's normal state is +5 volts.
2	7D	This is the clock to the cursor address counters. There should be 80 low going clocks on every scan line. This clock advances the counters through the display ROM address space.
3	1K	This is video to the monitor. This signal should normally be at a ground level with high going pulses for video. The height of the pulses will depend upon the setting of the contrast pot.
4	1K	This is a vertical synchronization signal to the monitor. Signal should sit at +5 volts with a signal going to ground every 16.67 milliseconds for 60 Hz (every 20 milliseconds for 50 Hz refresh). The signals low going duration is approximately 600 microseconds.
5	1J	This Test Point is located on the horizontal drive signal to the monitor. Signal should have a repetition rate of 53.8 microseconds in both 60 and 50 Hz refresh. The pulse duration will be 5 microseconds.
6	7D	This test point is located on the output control register WIDE mode signal. It can be momentarily forced high for Wide mode or low for Narrow mode for test purposes.
7	7E	This is the clear current address counter signal. It will go low for the period of the clock current address counter signal when the address counters reach the end of display memory (10 pulses low going every 538 usec., each pulse 1.06 usec. long).
8	4C	This is the serial data out of the 2651 circuit. It should sit at a high when no data is being transmitted. Signal format is per EIA standard and rear panel switch settings.
9	7B	This is serial data input to the 2651 circuit. Format is the same as for test point 8 above.

Module Logic Test Points Continued

Test Point	Grid Location	Description
10	4C	Baud oscillator. This is the 5.0688MHZ oscillator which is used by the 2651 to develop the bit rate timing. Duty cycle should be approximately 50%.
11	5D	This is a common interrupt line going to the microprocessor to indicate that one of the peripheral devices, (peripheral to the microprocessor), requires service. In normal operation this signal will have low going pulses for the timer interrupt, additional low going pulses occur when a serial data character is received by the 2651.
13 Bell 14	3B	These test points may be used to silence or to temper the volume of the bell. See instruction manual.
50 Hz GND	2J	A jumper between these test points causes the screen to be refreshed at 50 Hz - see instruction manual.
INVRS GND	4M	A jumper between these test points covers the screen to go to a black-on-white display. See instruction manual.

F. SCHEMATICS



REVISIONS			
SYM.	DESCRIPTION	DRAFT.	E
A		ASW	4-5-77
B	CHG R9 TO 27K, WAS 22K	[illegible]	5-16-77
C	ADD INV NO	SJ	10/11/77
D	ADDED Q4, R12, 13	AKB	11-23-77
E	REMOVED R10, R4, R1 WAS 100, R6 WAS 5.1K R9 WAS 27K, R5 WAS 7.5K	AKB	12-13-77
F	R6 WAS 43K, & R5 WAS 68K	SJ	3/21/78
G	2C-9 TIED TO 2C-10 ARTWORK CHG	MDG	10/6/78
H	DTR, 2C-2 & 4C-2 WERE DTS, 2C-3, 4C-3	AKB	2-19-79

NOTES:

1. FOR MAIN I/O CURRENT LOOP INSTALL IN POSISTIONS 1C, 2C AND FOR PERIPHERAL CURRENT LOOP, INSTALL IN POSITION 3C & 4C.
2. CUT ETCH (2) AND ADD JUMPERS (4) FOR CURRENT SOURCE OPTION.

3B2016	4041	B50939-2
3B2015	4041	B50939-1
INVENTORY	USED ON	ASSEMBLY

DRAFTSMAN CB 2/16/77	K = 10^3 M = 10^6	UNLESS OTHERWISE INDICATED
CHECKED RBW 5/17/77	CONNECTION NO CONNECTION	• RESISTANCE IN OHMS ± 10% ¼ WATT • CAPACITANCE IN MFD ± 20% • INDUCTANCE IN HENRIES • USE 60/40 ROSIN CORE SOLDER • USE NO CORROSIVE FLUX
APPROVED RBW 5/17/77		

INVENTORY 3D2017

TITLE: SCH-CURRENT LOOP/SOURCE OPTION

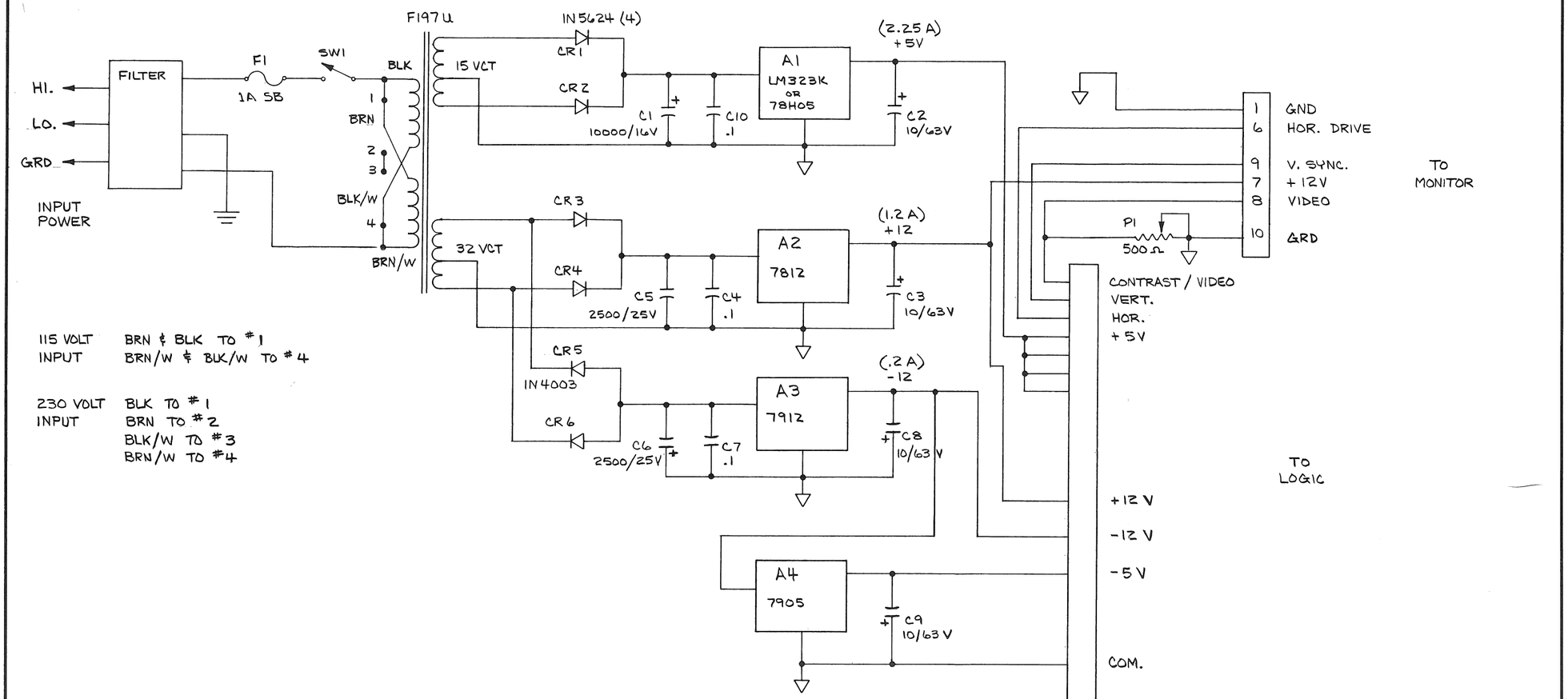
NUMBER: KB50940 REV

SHEET 1 OF 1

R·I CONTROLS
A DIVISION OF RESEARCH, INCORPORATED
MINNEAPOLIS, MINNESOTA 55424

TELEDYNE POST (4-75)
OCT 3 1 1977

REVISIONS					
SYM.	ZONE	DESCRIPTION	DRAFT.	CHECK.	DATE
A		CLARIFY DWG., CAP. VOLTAGES & POL. FI, AMP RATE & TYPE	AKB		11-16-78
B		DOCUMENTED FOR IMS SYS.	CLR		3-16-79



	1060	D055093
	1060	D053615
	USED ON	ASSEMBLY

DRAFTSMAN MJP (REA) 7/20/78
CHECKED
APPROVED H W Wilke 12 May 79

K = 10^3 M = 10^6
CONNECTION NO CONNECTION

UNLESS OTHERWISE INDICATED
- RESISTANCE IN OHMS ± 10% ½ WATT
- CAPACITANCE IN MFD ± 20%
- INDUCTANCE IN HENRIES
- USE 60/40 ROSIN CORE SOLDER
- USE NO CORROSIVE FLUX

MODEL 3D2167

TITLE SCHEMATIC - POWER SUPPLY, 1060

NUMBER KC053617 -000 REV. B

SHT. 1 OF 1

CONTROLS DIVISION • RESEARCH, INCORPORATED • MINNEAPOLIS 24, MINNESOTA

SWITCHES

UP = Closed
DOWN = Open

Switch Position UP	Switch Position DOWN	Switch	Goal Loc.
DISPLAY DELIMITER	NORMAL	1	
XMIT TO CURSOR----------	XMT TO END----------	2	
XMIT AN ETX	NORMAL	3	
FULL DUPLEX----------	HALF DUPLEX----------	4	7A
WRAP	NORMAL	5	
NEW LINE ENABLE----------	NORMAL----------	6	
NEW LINE ON CR	NEW LINE ON LF	7	
CURRENT LOOP----------	RS-232----------	8	
BAUD 1		1	
2		2	
3		3	
4		4	6A
EVEN PARITY	ODD PARITY	5	
PARITY ENABLE----------	NO PARITY----------	6	
1 STOP BIT	2 STOP BITS	7	
7 BIT CHAR----------	8 BIT CHAR----------	8	

SWITCH SETTINGS 4 3 2 1	BAUD RATE	SWITCH SETTINGS 4 3 2 1	BAUD RATE
U U U U	50	U U U D	1800
D U U U	75	D U U D	2000
U D U U	110	U D U D	2400
D D U U	134.5	D D U D	3600
U U D U	150	U U D D	4800
D U D U	300	D U D D	7200
U D D U	600	U D D D	9600
D D D U	1200	D D D D	Reserved

JUMPERS

HZ - 50 Hertz Refresh Rate - Grid 2K
Add jumper from pin marked 50 Hz to GND.

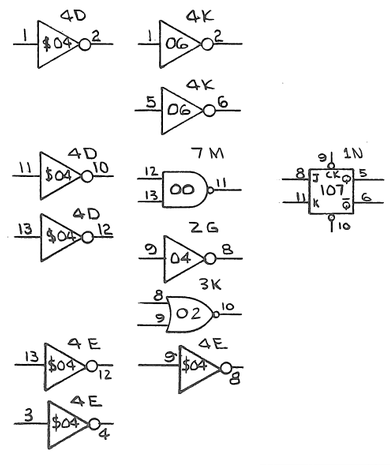
IV - Inverse Video - Grid 4N
Add jumper from pins INVERSE to GND.

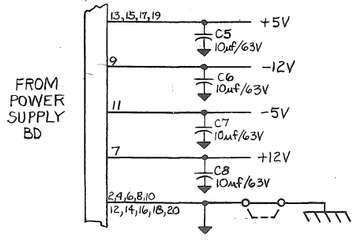
OPTIONS

CODE	TITLE	PROCEDURE
CLP	Current Loop	Add RI Assembly ~~KB50939-001~~ into 1C and 2C on logic board with board number away from power connector.
220V	220V Line Input	Move brown wire from hole 1 to hole 2; move brown/white wire from hole 4 to hole 3 located on power supply board.

DES	TYPE	+5V	-5V	-12V	+12V	GND
00	74L$00	14				7
02	74L$02	14				7
04	74L$04	14				7
06	74L$06	14				7
10	74L$10	14				7
20	74L$20	14				7
30	74L$30	14				7
32	74L$32	14				7
86	74L$86	14				7
107	74L$107	14				7
153	74L$153	16				8
155	74L$155	16				8
163	74L$163	16				8
165	74L$165	16				8
174	74L$174	16				8
257	74L$257	16				8
259	74L$259	16				8
374	74L$374	20				10
8304	AM8304	20				10
88	HDI-1488-5			1	14	7
89	HDI-1489-5	14				7
6502	MCS6502	8				1,21
2651	2651	26				4
2708	C2708	24	21		19	12
8316	8316B	24				12
40L45	40L45-45	18				9
$00	74$00	14				7
$04	74$04	14				7
555	NE555V	8				1

UNUSED IC PORTIONS





REVISIONS

SYM.	ZONE	DESCRIPTION	DRAFT.	CHECK.	DATE
A		SCH. No. WAS C53025 ADDED 4D, 13E & R29, C3 WAS 15pf	AKB		9-15-78
B		CHG. MASTER OSCILLATOR CKT	AKB		11-22-78
C		CHG'D R30 WAS 91 NOW 120	CAS		3-28-79
D		DOCUMENTED FOR IMS SYS.	CLR		3-29-79
		ARTWORK CHANGE. JUMPER OPTION AT ROM 5, 'COPY' OPTION AT 3H, 2G.	MDG		4-4-79

1060	D053887
1060	D053626
USED ON	ASSEMBLY

DRAFTSMAN AKB 9-15-78
CHECKED
APPROVED Bob Wyatt

K = 10^3 M = 10^6
CONNECTION NO CONNECTION

UNLESS OTHERWISE INDICATED
- RESISTANCE IN OHMS ± 10% ¼ WATT
- CAPACITANCE IN MFD ± 20%
- INDUCTANCE IN HENRIES
- USE 60/40 ROSIN CORE SOLDER
- USE NO CORROSIVE FLUX

MODEL 3D2169

TITLE SCHEMATIC - TELERAY LOGIC BOARD MODEL 1060

NUMBER KC053625 -000 REV. D

SHT. 1 OF 3

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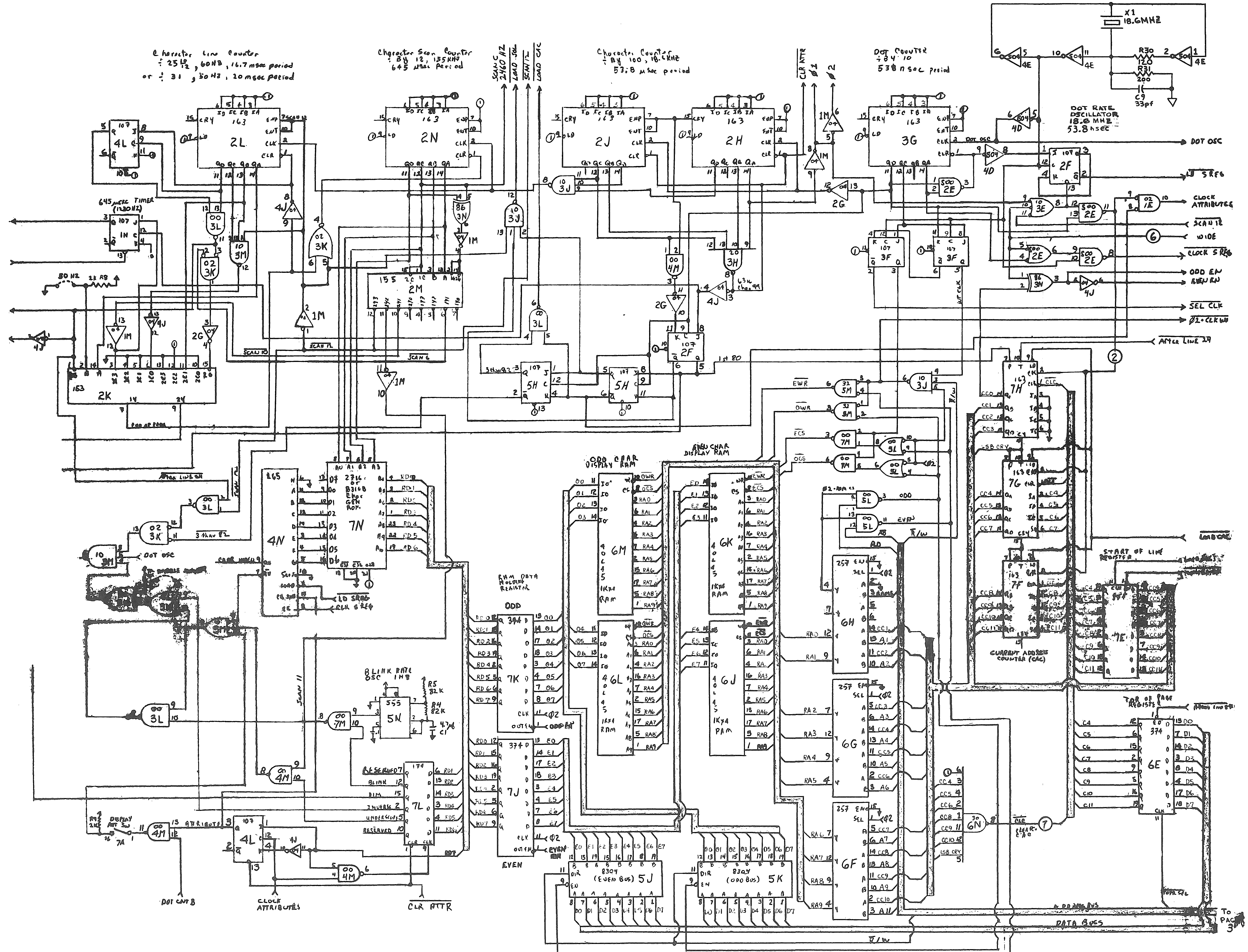

KC053625D -000

POWER UP RESET

+5 V

RESET

CHIP SELECT DECODING

PROGRAM E PROM

2708-1 1J

2708-2 1K

2708-3 1H

2708-4 1G

2708-5 1F

BUS BUFFERS

ADDRESS BUS

DATA BUS

OUTPUT CONTROL REGISTER

BELL

6502

5E

4H 1K x 4 RAM

4G 1K x 4 RAM

NOT INSTALLED AS STANDARD

5B

6B

7B

4B

4A

TO KYBD

SERIAL & PERIPHERAL I/O

2651 5C

BAUD RATE OSC

5.0688 MHz

Connector Serial I/O

Connector Peripheral I/O

KC053625D-000

SHT 3 OF 3

G. PARTS LISTS

PARTS LIST

Title: ASSY-LOGIC BD, 1061 #D53626 Rev. D

ITEM	DESCRIPTION	PART NO.	INVENTORY	1	2	3	4	
1	Assembly-Logic Board, 1061		3B2156	X				
2	Trimpot - 200 Ohm	72P-200	6B0310	X				
3	Resistor Network - 2.2K, SIP	4308R-101 222	14B0676					5
4	Crystal - 18.600 MHZ	B53714	34B0185	X				
5	Crystal - 5.06880 MHZ (Sm.)	B52233	34B0182	X				
6	Alarm Device	EAF-14R06C	26B0149	X				
7	IC-TTL, LS, QD 2-In Pos Nand Gate	74LS00PC	33B0284					5
8	IC-TTL, LS, QD 2-In Nor Gate	DM74LS02	33B0283		X			
9	IC-TTL, LS Hex Inverter	DM74LS04	33B0282					5
10	IC-TTL, Hex Inverter	SN7406N	33B0200		X			
11	IC-TTL, LS 3-In Pos Nand Gate	DM74LS10	33B0328			X		
12	IC-TTL, LS 4-In Pos Nand Gate	DM74LS20	33B0329	X				
13	IC-TTL, LS 8-In Pos Nand Gate	DM74LS30	33B0331	X				
14	IC-TTL, LS, Quad 2 Pos Or Gate	DM74LS32	33B0332		X			
15	IC-TTL, LS QD 2-In EXCL or Gate	DM74LS86	33B0280	X				
16	IC-TTL, LS Dual J-K Flip-Flop	DM74LS107	33B0279					5
17	IC-TTL, LS 4/1 Data Select/Mult	DM74LS153	33B0301	X				

ORDERING INFORMATION

1) For ordering information and latest prices, contact your local representative or the RESEARCH, Incorporated factory in Minneapolis, Minnesota.

2) When ordering spare parts, please include references both to this parts list number and revision level, plus, the Model Number and Serial Number of the instrument for which these parts are being ordered.

PARTS LIST

Title: ASSY, CURRENT LOOP (Optional) #B50939 Rev. E

ITEM	DESCRIPTION	PART NO.	INVENTORY
1	Sch-Current Loop/Source, 1061	B50940	3D2017
2	Transistor C1	ITE4119	34B0155
3	Transistor Q2, Q3	2N3643	34B0114
4	Transistor Pad Q2, Q3	7717-8IN WHT	5A0209
5	Diode CR1	IN4003	32C0133
6	IC-Lin, Phototrans Opto-Isolat A1, A2	IL-1	33B0130
7	Resistor-82, 1/4W, 5%, Carbon R1		14C0652
8	Resistor-20K, 1/4W, 5% Carbon R6		14C0409
9	Resistor-30K, 1/4W, 5%, Carbon R5		14C0657
10	Resistor-22K, 1/4W, 5%, Carbon R2		14C0280
11	Resistor-560, 1/2W, 5%, Carbon R3, R7		14C0151
12	Wire-#24, Blk, PVC	W76B	10C0223
13	Resistor-4.7K, 1/4W, 5%, Carbon R11		14C0284
14	PCB Connector-14 Pin	614-AG1	4A0447
15	Resistor-470K, 1/4W, 5%, Carbon R8		14C0279
16	Resistor-27K, 1/4W, 5%, Carbon R9		14C0295
17	Resistor-300K, 1/4W, 5%, Carbon R12		14C0488
18	Resistor-10K, 1/4W, 5%, Carbon R13		14C0267
19	Transistor Q4	2N3644	34B0111

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