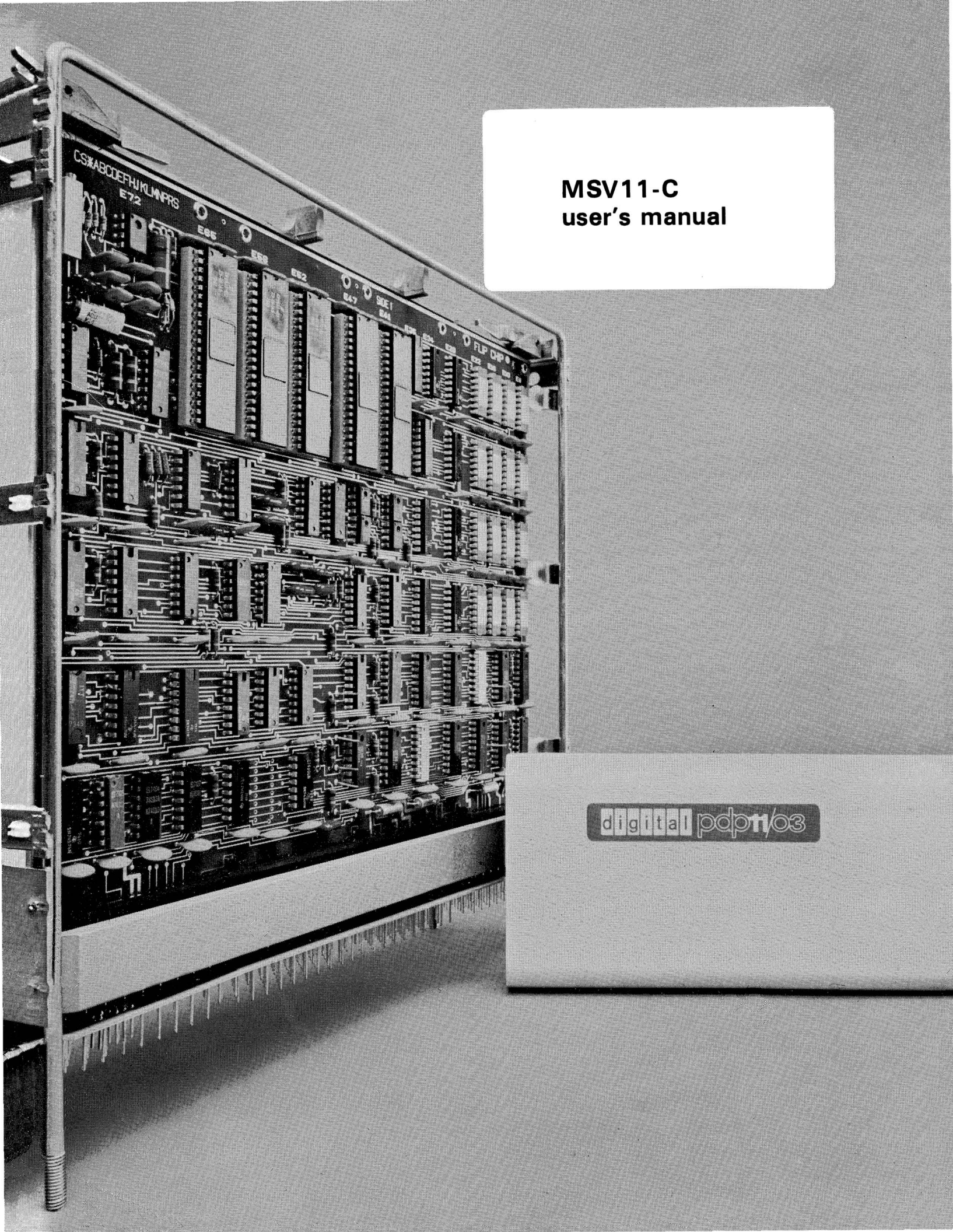
MSV11-C
user's manual
digital pdp11/03

EK-MSV11-OP-001

MSV11-C
user's manual

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CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION

This manual contains all user information required for installing, operating, and using the MSV11-C-series dynamic metal oxide semiconductor (MOS) read/write memory options. Four memory options are covered in this manual:

Model	Description
MSV11-CA	4K by 16-bit read/write memory
MSV11-CB	8K by 16-bit read/write memory
MSV11-CC	12K by 16-bit read/write memory
MSV11-CD	16K by 16-bit read/write memory (Figure 1-1).

All MSV11-C models are LSI-11 bus-compatible, and can be installed in any backplane location in the LSI-11, PDP-11/03, or PDP-11V03 system.

1.2 GENERAL DESCRIPTION

The MSV11-C consists of a single "quad" (four sets of backplane pins) module (printed circuit board) that plugs into any standard LSI-11 backplane. Memory contents are volatile; that is, when operating power is lost, memory data is lost. In addition to the basic 4K, 8K, 12K, or 16K memory capability (depending upon model), all MSV11-C options feature:

1. On-board refresh circuit that eliminates its need for refresh signals on the LSI-11 bus.
2. The system memory address space to which the option will respond is user-configured via switches contained on the module. An address can start at any 4K bank boundary.
3. It will perform DATI, DATO, DATOB, DATIO, and DATIOB bus cycles according to LSI-11 bus protocol.
4. Jumpers allow the module to be configured for using external bus refresh signals and disabling the internal refresh function.
5. No special power is required. Only the normal +5 and +12 Vdc voltages are necessary. An on-board charge pump circuit provides the necessary -5 V operating voltage to the memory chips.
6. Jumpers allow the user to implement battery backup power.

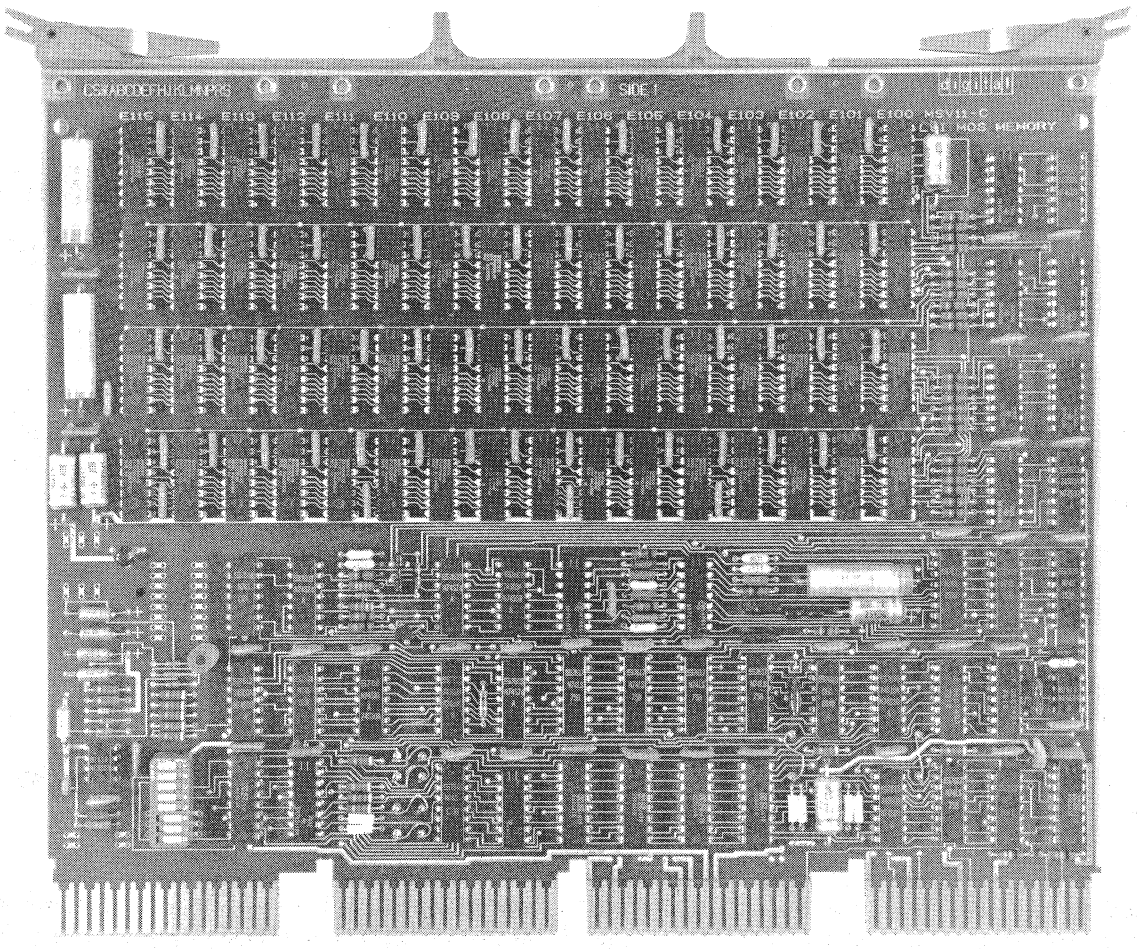

Figure 1-1 MSV11-CD 16K by 16-Bit Read/Write Memory

1.3 SPECIFICATIONS

1.3.1 Electrical

Power Requirements

System Power	Operating	Standby
+5 V ± 5%	1.1 A typ. (2.0 A max.)	1.1 A typ. (2.0 A max.)
+12 V ± 5%	0.54 A typ. (0.56 A max.)	0.16 A typ. (0.2 A max.)
Power	12 W typ. (16.7 W max.)	7.7 W typ. (12.4 W max.)

Battery Backup Power

+5 V -+ 5%	0.8 A typ. (1.4 A max.)
+12 V ± 5%	0.16 A typ. (0.2 A max.)

Operating Speed – The operating speeds stated below are based upon the bus not attempting a memory cycle during a refresh operation and that an arbitration was not necessary.

Access Time:

Bus Cycle Type	**Access Time**
DATI, DATIO	300 ns typ. (350 ns max. from RSYNC H)
DATO(B)	300 ns typ. (350 ns max. from RDOUT H).

Cycle Time:

Bus Cycle Type	**Cycle Time**
DATI	650 ns typ. (750 ns max. from RSYNC H)
DATO(B)	650 ns typ. (750 ns max. from RDOUT H)

NOTE

If a bus cycle is being done as a result of winning the synchronization arbitration, the bus cycle will be delayed or increased from 0 to 80 ns. If a refresh operation is in progress when a cycle is requested, a delay from 0 to 750 ns will occur before the bus cycle starts.

1.3.2 Environmental

Operating Temperature – 5° to 50° C (41° F to 122° F) with a relative humidity of 10% to 95% (no condensation), with adequate airflow across the module. When operating at the maximum temperature (50° C or 122° F), air flow must maintain the inlet to outlet air temperature rise across the modules to 7° C (12.5° F), maximum.

1.3.3 Mechanical

Size

Height - 26.6 cm (10.5 in)
Length - 22.8 cm (8.9 in)
Width - 1.27 cm (0.5 in)

NOTE

Length as stated is approximate and includes metal handles. Actual module length is 21.6 cm (8.5 in).

1.3.4 Backplane Pinning Utilization

MSV11-C backplane pin utilization is shown in Table 1-1. Blank spaces indicate pins not used by the MSV11-C.

1.4 REFERENCES

Additional DIGITAL publications that will assist the user in installing and maintaining the MSV11-C memory option include:

Microcomputer Handbook
PDP-11V03 System Manual

Table 1-1 Backplane Pin Utilization

A Connector			B Connector			C Connector			D Connector
Side 1	Pin	Side 2	Side 1	Pin	Side 2	Side 1	Pin	Side 2	
	A	+5 V	BDCOK H	A	+5 V		A		
	B			B			B		
BAD16 L	C	GND		C	GND		C		
BAD17 L	D			D	+12 V		D		
	E	BDOUT L		E	BDAL02 L		E		
	F	BRPLY L		F	BDAL03 L		F		
	H	BDIN L		H	BDAL04 L		H		
GND	J	BSYNC L	GND	J	BDAL05 L		J		
	K	BWTBT L	-5 V	K	BDAL06 L		K		
TMARGIN	L		-5 V	L	BDAL07 L		L		
GND	M	BIAKI L	GND	M	BDAL08 L		M	BIAKI L	
	N	BIAKO L		N	BDAL09 L		N	BIAKO L	
	P			P	BDAL10 L		P		
BREF L	R	BDMGI L		R	BDAL11 L		R	BDMGI L	
+12B	S	BDMGO L		S	BDAL12 L		S	BDMGO L	
GND	T		GND	T	BDAL13 L		T		
	U	BDAL00 L		U	DBAL14 L		U		
+5 V	V	BDAL01 L	+5 V	V	BDAL15 L		V		

CHAPTER 2
INSTALLATION

2.1 GENERAL

This chapter contains information required for configuring and installing the MSV11-C in the LSI-11 system backplane. Configuring the module involves selecting the module's address range via switches and other functional operations implemented or disabled via jumpers. Proper installation will ensure normal MSV11-C operation in the system and eliminate the possibility of physical damage to the MSV11-C module or backplane in which it is installed. Details are provided in the following paragraphs.

2.2 CONFIGURING THE MSV11-C

2.2.1 General

Configuring the MSV11-C will alter its operation for a specific system application. The following items can be configured:

1. Select the starting address for the contiguous memory contained on the module.
2. Refresh mode: on-board or external refresh, and reply to external refresh signals.
3. Battery backup power.
4. Bus grant (BIAK L and BDMG L) signals.

In most applications, the user will simply configure the starting address and install the module. Refer to the following paragraphs for procedures for configuring each item.

2.2.2 Address Selection

The MSV11-C's address can start at any 4K band boundary. The address configured is the starting address for the contiguous portion of memory (4K, 8K, 12K, or 16K) contained on the module. Set the switches, located as shown on Figure 2-1, to the desired starting address as listed in Table 2-1. Note that the module is designed to accommodate a 128K system addressing capability; however, the present addressing capability of the LSI-11 system, including all PDP11/03 and PDP11-V03 systems, is 32K. By PDP-11 convention, the upper 4K address space is normally reserved for peripheral device and register addresses. Thus, with the present LSI-11 maximum addressing capability of 32K, Bank 7 (addresses 160000–177777) normally should not be used for system memory.

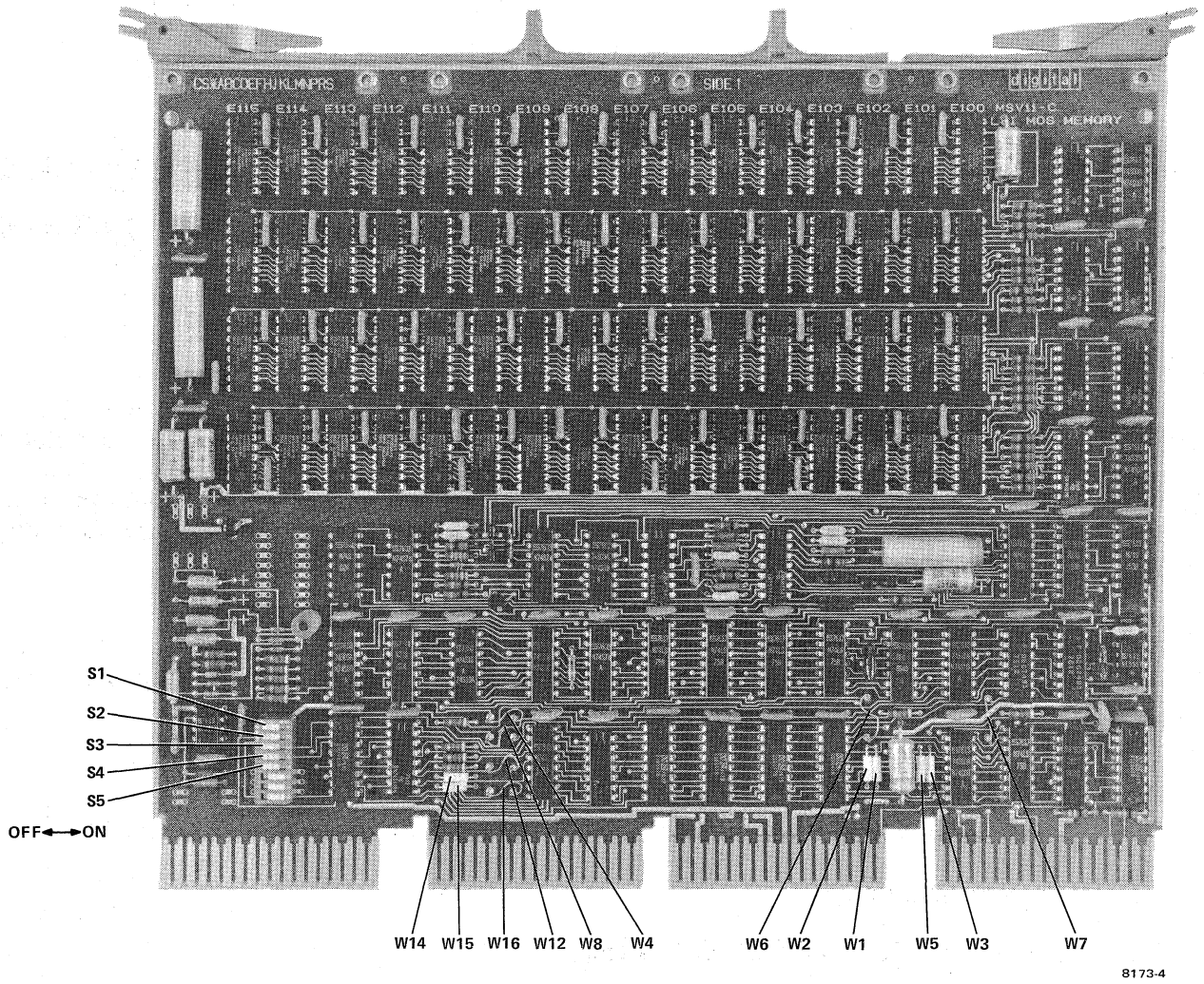

Figure 2-1 MSV11-C Switch and Jumper Locations

2.2.3 Refresh Mode Selection

The MSV11-C module is factory-configured for internal (on-board) memory refresh and no reply (assertion of BRPLY L) in response to refresh cycles on the LSI-11 bus. Factory-installed wire-wrap jumpers W6 and W7, located as shown in Figure 2-1, provide these functions. W7, when installed, enables internal refresh. W6, when removed, enables the MSV11-C to reply to external (SLI-11 bus) refresh cycles. External refresh cycles can be controlled by the LSI-11 microcomputer module (M7264 or M7264-YA), or by a DMA device, such as the REV11-A and REV11-C options. W6 must be installed if W7 is installed to prevent erroneous assertion of the BRPLY L signal. A summary of refresh mode jumpers is provided in Table 2-2.

The reply to external refresh cycles is normally enabled when the module is deemed the slowest dynamic MOS memory device in the system. The slowest device (in this application) is generally the device located the greatest electrical distance from the LSI-11 microcomputer or DMA device generating the refresh bus cycles. Only one device should be permitted to reply to refresh bus signals.

Table 2-1 MSV11-C Addressing Summary

Starting Address	Contiguous Memory Addresses Selected for Each Model								Switch Settings				
	MSV11-CA		MSV11-CB		MSV11-CC		MSV11-CD						
	Bank	Address Range	Banks	Address Range	Banks	Address Range	Banks	Address Range	S1	S2	S3	S4	S5
0	0	0-17777	0, 1	0-37777	0-2	0-57777	0-3	0-77777	1	1	1	1	1
20000	1	20000-37777	1, 2	20000-57777	1-3	20000-77777	1-4	20000-117777	0	1	1	1	1
40000	2	40000-57777	2, 3	40000-77777	2-4	40000-117777	2-5	40000-137777	1	0	1	1	1
60000	3	60000-77777	3, 4	60000-117777	3-5	60000-137777	3-6	60000-157777	0	0	1	1	1
100000	4	100000-117777	4, 5	100000-157777	4-6	100000-157777	4-7	100000-177777	1	1	0	1	1
120000	5	120000-137777	5, 6	120000-157777	5-7	120000-177777	5-10	120000-217777	0	1	0	1	1
140000	6	140000-157777	6, 7	140000-177777	6-10	140000-217777	6-11	140000-237777	1	0	0	1	1
160000	7	160000-177777	7, 10	160000-217777	7-11	160000-237777	7-12	160000-257777	0	0	0	1	1
200000	10	200000-217777	10, 11	200000-237777	10-12	200000-257777	10-13	200000-277777	1	1	1	0	1
220000	11	220000-237777	11, 12	220000-257777	11-13	220000-277777	11-14	220000-317777	0	1	1	0	1
240000	12	240000-257777	12, 13	240000-277777	12-14	240000-317777	12-15	240000-337777	1	0	1	0	1
260000	13	260000-277777	13, 14	260000-317777	13-15	260000-337777	13-16	260000-357777	0	0	1	0	1
300000	14	300000-317777	14, 15	300000-337777	14-16	300000-357777	14-17	300000-377777	1	1	0	0	1
320000	15	320000-337777	15, 16	320000-357777	15-17	320000-377777	15-10	320000-417777	0	1	0	0	1
340000	16	340000-357777	16, 17	340000-377777	16-20	340000-417777	16-21	340000-437777	1	0	0	0	1
360000	17	360000-377777	17, 20	360000-417777	17-21	360000-437777	17-22	360000-457777	0	0	0	0	1
400000	20	400000-417777	20, 21	400000-437777	20-22	400000-457777	20-23	400000-477777	1	1	1	1	0
420000	21	420000-437777	21, 22	420000-457777	21-23	420000-477777	21-24	420000-517777	0	1	1	1	0
440000	22	440000-457777	22, 23	440000-477777	22-24	440000-517777	22-25	440000-537777	1	0	1	1	0
460000	23	460000-477777	23, 24	460000-517777	23-25	460000-537777	23-26	460000-557777	0	0	1	1	0
500000	24	500000-517777	24, 25	500000-537777	24-26	500000-557777	24-27	500000-577777	1	1	0	1	0
520000	25	520000-537777	25, 26	520000-557777	25-27	520000-577777	25-30	520000-617777	0	1	0	1	0
540000	26	540000-557777	26, 27	540000-577777	26-30	540000-617777	26-31	540000-637777	1	0	0	1	0
560000	27	560000-577777	27, 30	560000-617777	27-31	560000-637777	27-32	560000-657777	0	0	0	1	0
600000	30	600000-617777	30, 31	600000-637777	30-32	600000-657777	30-33	600000-677777	1	1	1	0	0
620000	31	620000-637777	31, 32	620000-657777	31-33	620000-677777	31-34	620000-717777	0	1	1	0	0
640000	32	640000-657777	32, 33	640000-677777	32-34	640000-717777	32-35	640000-737777	1	0	1	0	0
660000	33	660000-677777	33, 34	660000-717777	33-35	660000-737777	33-36	660000-757777	0	0	1	0	0
700000	34	700000-717777	34, 35	700000-737777	34-36	700000-757777	34-37	700000-777777	1	1	0	0	0
720000	35	720000-737777	35, 36	720000-757777	35-37	720000-777777	x	x-x	0	1	0	0	0
740000	36	740000-757777	36, 37	740000-777777	x	x-x	x	x-x	1	0	0	0	0
760000	37	760000-777777	x	x-x	x	x-x	x	x-x	0	0	0	0	0

NOTES

1. **Switch settings:**
   1 = ON
   0 = OFF
2. **Horizontal lines indicate present upper address limit in LSI-11 systems.**
3. **Dotted horizontal lines indicate present normal upper address limit for LSI-11 system memory.**
4. **Each memory bank = one 4K address space.**

Table 2-2 Refresh Mode Selection

Jumper		Refresh Mode Function
W6	W7	
in	in	Factory configuration. Internal refresh; no reply.
in	out	External refresh; no reply
out	in	Illegal–do not use.
out	out	External refresh; reply enabled.

2.2.4 Battery Backup Power

MSV11-C modules are supplied with all power jumpers (W1, W2, W3, and W5) installed. The jumpers connect normal system power to battery backup power pins. If battery backup power is to be used with the MSV11-C, cut or remove jumpers W1 and W5; the module will receive DC operating voltages (+5 V and +12 V) from the battery backup power source, only. If battery backup power is available, but battery backup power is not desired for a particular MSV11-C module, cut or remove jumpers W2 and W3; jumpers W1 and W5 must remain installed.

2.2.5 Bus Grant Continuity

Bus grant continuity jumpers W14 and W15 are factory installed and normally should not be removed.

2.2.6 Bank Select Enable

Bank select enable jumpers W4, W8, W12, and W16 are factory-configured for the particular MSV11-C model ordered. They are wire-wrapped jumpers that normally should not be changed. Their use is described in Chapter 4.

2.3 INSTALLING THE MSV11-C MODULE

MSV11-C modules must be installed or removed only when dc power is removed from the backplane. The PDP-11/03 contains a control/indicator panel on the front of the power supply; the DC ON/OFF switch allows the user to turn off dc power for safe module insertion and removal.

Modules must be installed in the backplane with components facing row 1, as shown in Figure 2-2.

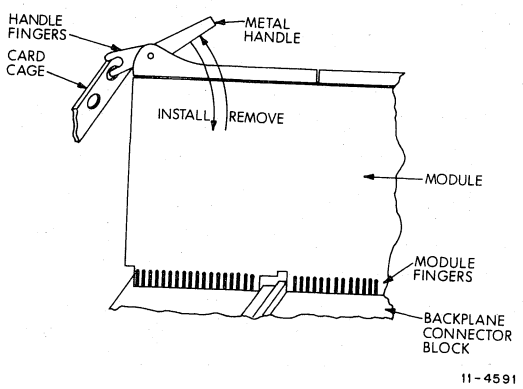

Figure 2-2 Module Installation

MSV11-C modules are equipped with metal handles that facilitate module installation and removal. When installing an MSV11-C into the H9270 backplane (or the DDV11-B backplane equipped with the H0341 card cage assembly), carefully start the module fingers into the backplane connector block while inserting the metal handle fingers into the card cage as shown in Figure 2-2. Once the module has been started into the backplane in this manner, insertion can be completed by pressing downward on the handles; both handles must be pressed simultaneously. Module removal can be accomplished by simultaneously raising both handles until the handle fingers clear the card cage. The module can then be removed easily.

CAUTION

The LSI-11 modules and the backplane assembly mounting blocks may be damaged if the modules are plugged in backward.

DC power must be removed from the backplane during module insertion or removal.

CHAPTER 3
TECHNICAL DESCRIPTION

3.1 GENERAL

The basic functions that comprise the MSV11-C are shown in Figure 3-1. All signals interface with the LSI-11 bus via bus receivers, bus drivers, and bus transceivers, which contain both receiver and driver functions. The receiver function of the bus transceivers shown in the figure distributes the 16 input data/address lines (DI00–15 H) to the memory array and to addressing logic.

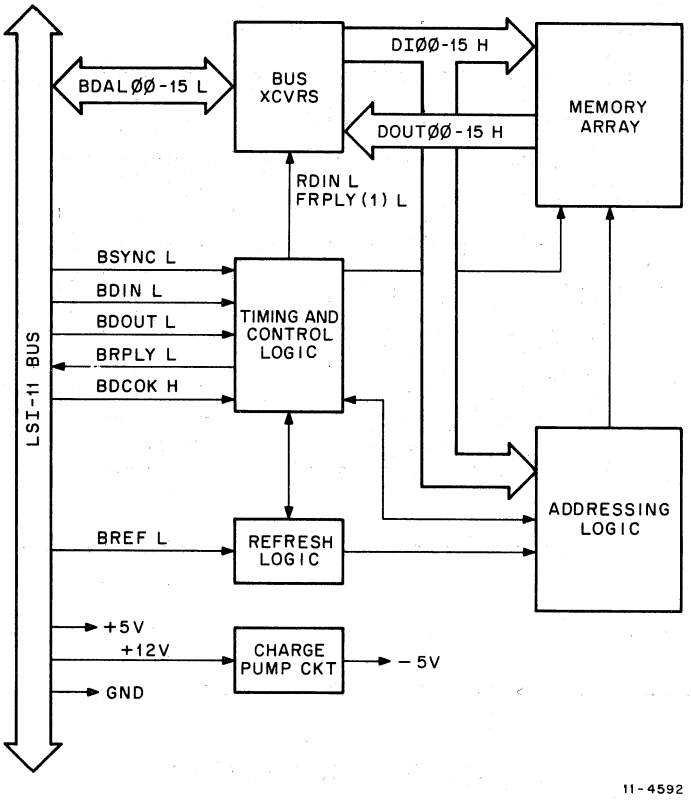

Figure 3-1 MSV11-C Block Diagram

Timing and control logic receives BSEL H from the addressing logic whenever the bus address received is within the range configured by the operator. This is the signal that allows the timing and control logic to communicate with the bus and generate appropriate timing and control signals from the option.

The memory responds to address and control signals by storing (writing) an 8-bit byte or 16-bit word, or by outputting 16-bit (word) read data to the LSI-11 bus.

Additional functions include refresh logic and a charge pump circuit. The refresh logic is capable of responding to LSI-11 bus ("external") refresh signals, or it can produce refresh signals (including row address) independent of the LSI-11 bus ("internal refresh"). Memory chips are refreshed by forcing a read cycle at all 64 row addresses once every 2 ms, maximum. The MSV11-C refresh logic refreshes one row address every 25 μs.

The charge pump circuit eliminates the need for backplane power other than the standard +5 V and +12 V. It contains an inverter circuit that receives +12 V input power and produces a negative voltage output. A Zener-diode regulator produces -5 V for the memory integrated circuits.

3.2 MEMORY ARRAY

The memory array (Figure 3-2) consists of 16 4K by 1-bit integrated circuits per memory bank; four memory banks are included in the option. Hence, 64 integrated circuits comprise the array. Each integrated circuit provides one bit by 4096-location storage.

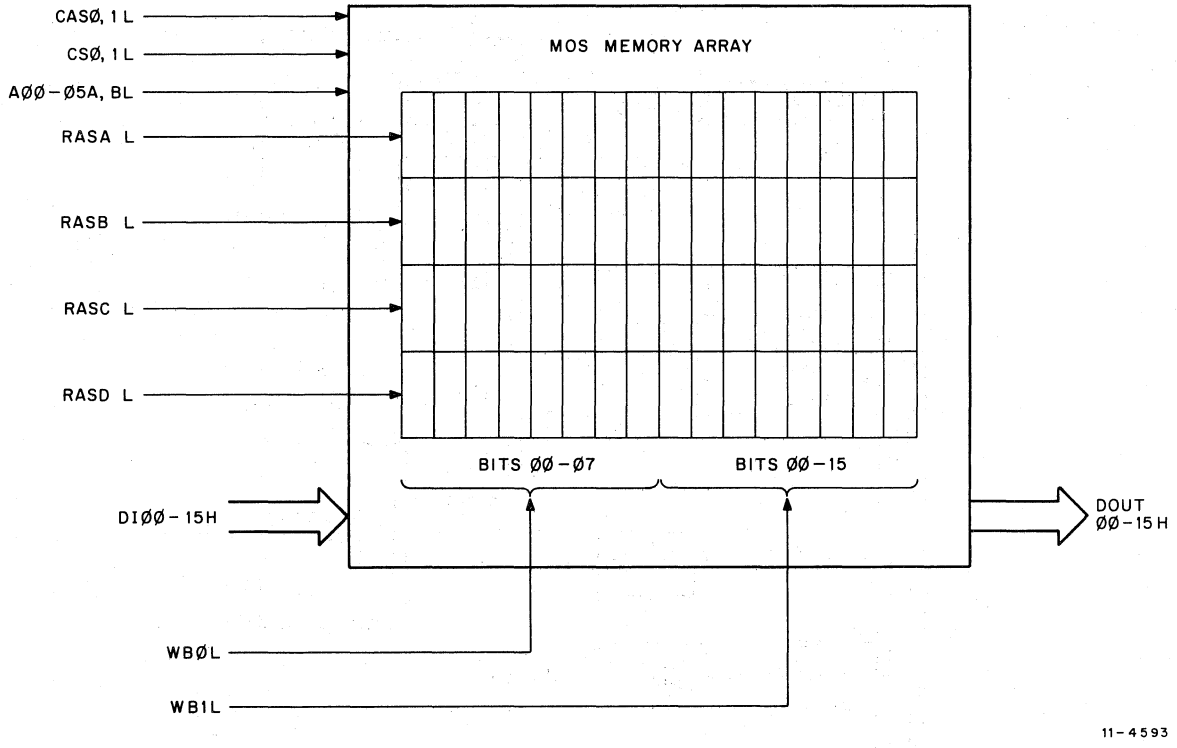

Figure 3-2 Memory Array

The memory array is arranged so that one bank out of four can be accessed at a time. The row address strobe (RASAL, RASBL, RASCL, and RASDL) signals select the desired bank. During a write operation, control signals WB0 L and WB1 L enable writing in the "low" byte (data bits 00–07) or "high" byte (data bits 08–15), or full word (both bytes accessed simultaneously).

Duplicate drivers are used for certain signals. These signals include column address strobe (CAS), chip select (CS), and address lines 00–05.

The duplicate driver output signals include:

Drivers	Output Signals
CAS	CAS0 L and CAS1 L
CS	CS0 L and CS1 L
Address	A00–05A L and A00–05B L

Each memory integrated circuit has six address input pins and contains a 12-bit address latch. Addressing the 4096 locations is accomplished by multiplexing the 12-bit address in two 6-bit segments. The low-order six bits (bus address bits 01–06) are first multiplexed onto A00–05A L/A00–05B L, signal lines and latched in the addressed sixteen integrated circuits by the active row address strobe signal. This is followed by multiplexing the high-order six bus address bits 07–12 onto the same six address lines; the column address strobe signals latch the address bits in the memory integrated circuits. The memory array is ready for the read or write operation once the addressing sequence has been completed. A detailed description of the complete addressing and read or write sequence is included in Paragraphs 3.3 and 3.4.

3.3 ADDRESSING LOGIC

The addressing logic (Figure 3-3) decodes a memory bank within the user-defined address space, latches the word or byte address within the selected bank, and routes time-multiplexed 6-bit address segments to the memory array for one of 4096 word addresses within the bank. In addition, it routes the refresh address to the memory bank during a refresh cycle. The following paragraphs describe addressing logic functions in detail. Generation of the control signals and how they relate to a complete memory read or write operation is described in Paragraph 3.4.

A memory read or write cycle is initiated by the addressing portion of the LSI-11 bus cycle. (A detailed description of LSI-11 bus cycles and timing is contained in the *Microcomputer Handbook*, Section 1, Chapter 3.) The "bus master" first places the address on BDALO0–15 L and BAD16 and 17 L. (BAD16 and 17 L are not used presently by LSI-11 system hardware, but are available for future system configurations.) The bus master then asserts BSYNC L indicating that a valid address is on the bus. LATCH L occurs on the leading edge of BSYNC L, latching the received address bits RAO–17 H and the received bus write/byte control signal, RWBT H, for the duration of the bus cycle. Note that RWBT H is active during the addressing portion of DATO or DATOB bus cycles, indicating that a memory write operation will follow.

Start address switches S1–S5 are configured by the user to select the address space that the 16K memory will occupy. ADDR OFFSET 13–17 L signals are the encoded starting address switch bits. The bits are applied to the adder and decoder logic, where they are added to the latched address bits LA13–17 L. One decoded output (ROWO–3 L) goes active (low) only when the latched address is within the 16K address space selected by the user. When the latched address is not within the assigned address space, the decoder outputs remain passive (high). These signals are applied to the BSEL H and bank select OR gates. Any active output (or an active LAT EXT REF L signal) produces an active (high) BSEL H signal; BSEL H enables the timing and control logic to start a memory cycle.

Bank select OR gates receive one active ROW signal via jumper W4, W8, W12, or W16 or an active REF L signal and produce one active BANK A–D H for normal memory cycles, or all active BANK A-D H signals during a memory refresh operation. The active BANK A–D H signal is ANDed with TRAS(1) H for proper timing during the memory cycle. The appropriate row address driver then produces one active RAS A–D L signal that enables one memory bank; all four signals go to the active state during a refresh operation to allow all memory banks to be refreshed simultaneously.

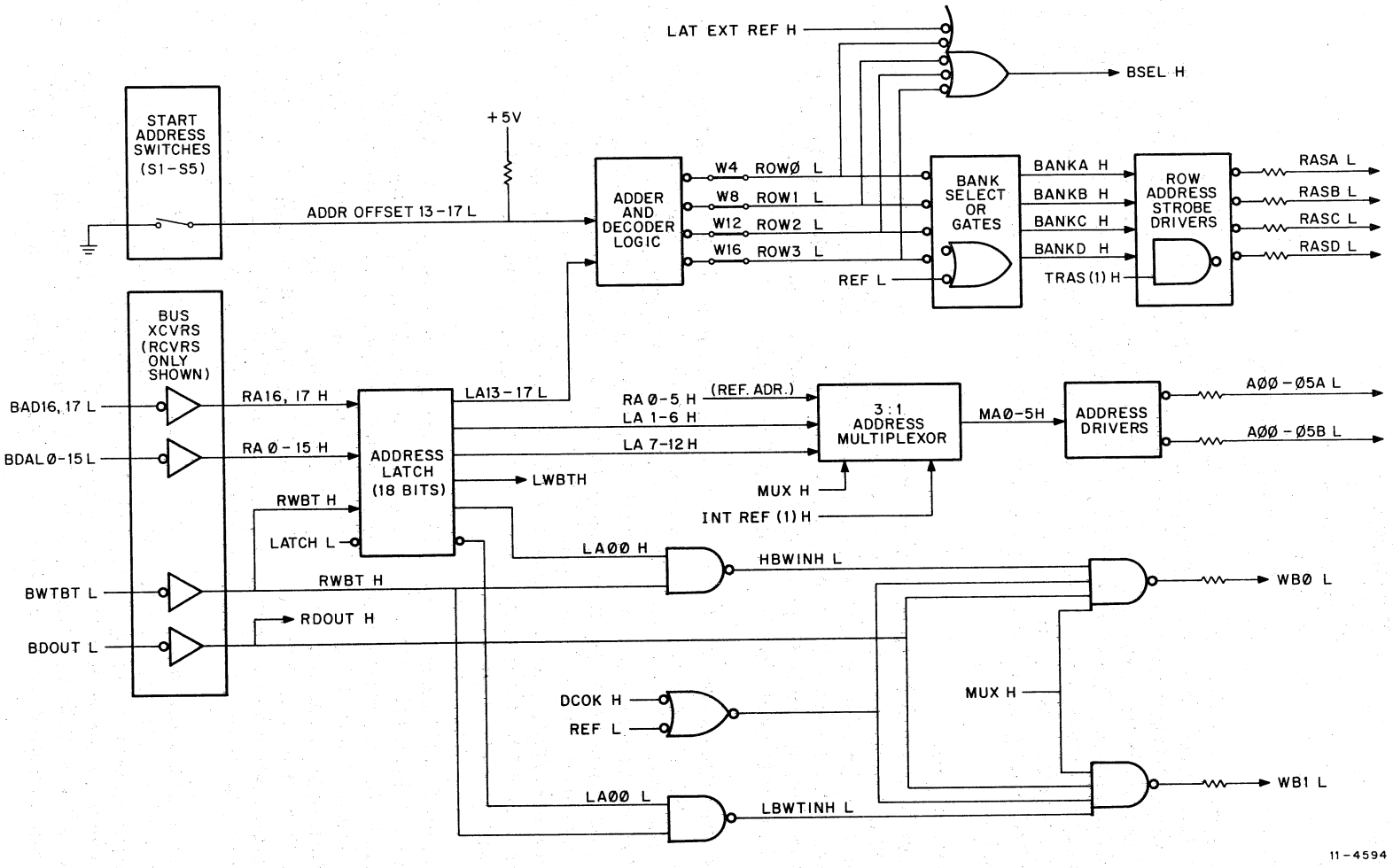

Figure 3-3 Addressing Logic

The 3:1 address multiplexor and address drivers select and apply the 6-bit address to the memory array. During a normal (non-refresh) memory cycle, MUX H and INT REF(1) H are passive (low); and low-order six address bits are applied to the memory array and latched in each memory integrated circuit. MUX H then goes high, selecting the high-order six bits which are then latched in the memory integrated circuits to comprise the 12-bit address. During an internal memory refresh operation, INT REF(1) H goes active, selecting the refresh address bits (RAO–5 H), which are applied to the memory array. If the external memory refresh mode of operation is configured by the user, the low-order address bits (LA1–6 H) are used for the refresh address.

During a write operation, the bus I/O sequence can be a DATO (word) or DATOB (byte) cycle. Bus signal BWTBT L goes passive during the data portion of a DATO cycle, enabling writing in all 16 bits of the addressed word. RWBT H goes low, inhibiting the byte inhibit gates and HBWINH L and LBWINH L go passive (high) enabling WBO L and WB1 L memory array drivers. The drivers are enabled only during an output data transfer (BDOUT L is active) and a non-refresh operation. The active MUX H signal gates the drivers on at the proper time during the bus cycle. During a DATOB bus cycle, RWBT H goes active, enabling the byte inhibit gates. Latched address bit 0 (signals LAOO H and LAOO L) inhibit the WBO L or WB1 L signals, as appropriate, to enable writing in only the addressed 8-bit byte within the addressed 16-bit location.

When backplane power is abnormal, DCOK H goes low. This signal inhibits WB0 L and WB1 L, preventing erroneous write operations.

3.4 TIMING AND CONTROL LOGIC

3.4.1 General

Timing and control logic (Figure 3-4) interfaces the MSV11-C to the LSI-11 bus and produces the internal control signals required for memory operation. This function produces timing and control signals for three types of memory cycles: read (DATI), write (DATO or DATOB), and refresh. In addition, read-modify-write cycles (DATIO or DATIOB) can be executed according to LSI-11 bus protocol. The MSV11-C will also respond to externally generated refresh cycles if that refresh mode is configured by the user.

3.4.2 Memory Read Operation

The control signal sequence for a memory read operation is shown in Figure 3-5; also refer to the logic functions shown in Figure 3-4. All bus transactions involving the MSV11-C are initiated by the addressing portion of the bus cycle. The bus master first places an address on the BDAL00–15 L (and optional BAD16, 17 L) lines and asserts BSYNC L. BSYNC L is received and distributed on the MSV11-C as RSYNC H and LATCH L. The leading edge of LATCH L latches the address in the addressing logic and the address will remain valid for the duration of the bus transaction (during the active state of BSYNC L).

Initially, NO DIN L and LOCKOUT L are passive (high) enabling two inputs of the Read Cycle Initiate gate. RSYNC H enables a third input to the gate. When the latched address is within the MSV11-C's address space configured by the user, BSEL H goes high, producing a low (active) Read Cycle Initiate gate output. The low signal is ORed, producing an active GOTIM H signal. This is the signal that starts the memory cycle.

GOTIM H is then applied to the 80-ns delay circuit. The delay circuit inserts an 80-ns delay only during internal refresh operation, as described in Paragraph 3.5.2. The delay circuit is shown in Figure 3-6.

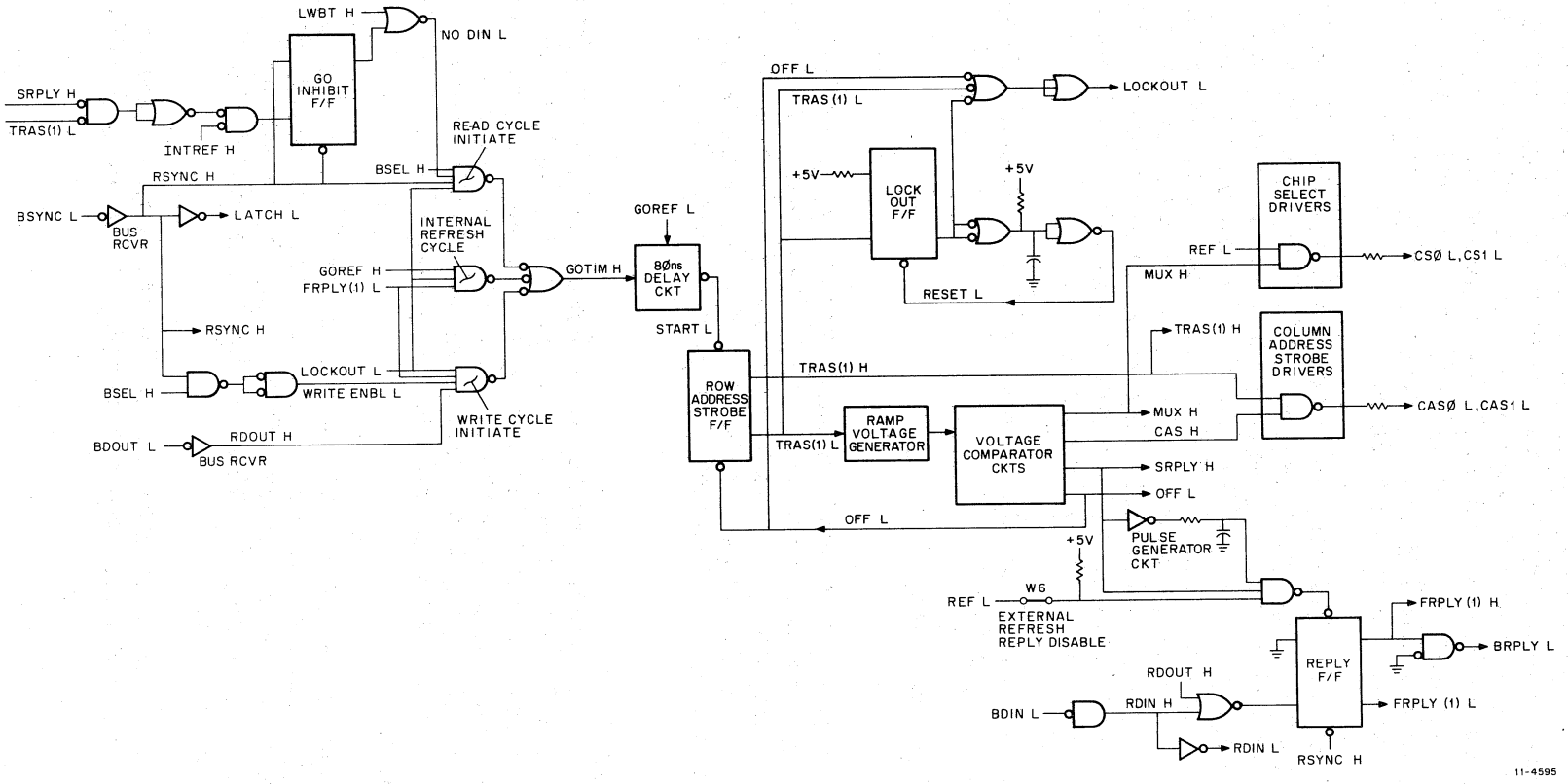

Figure 3-4 Timing and Control Logic

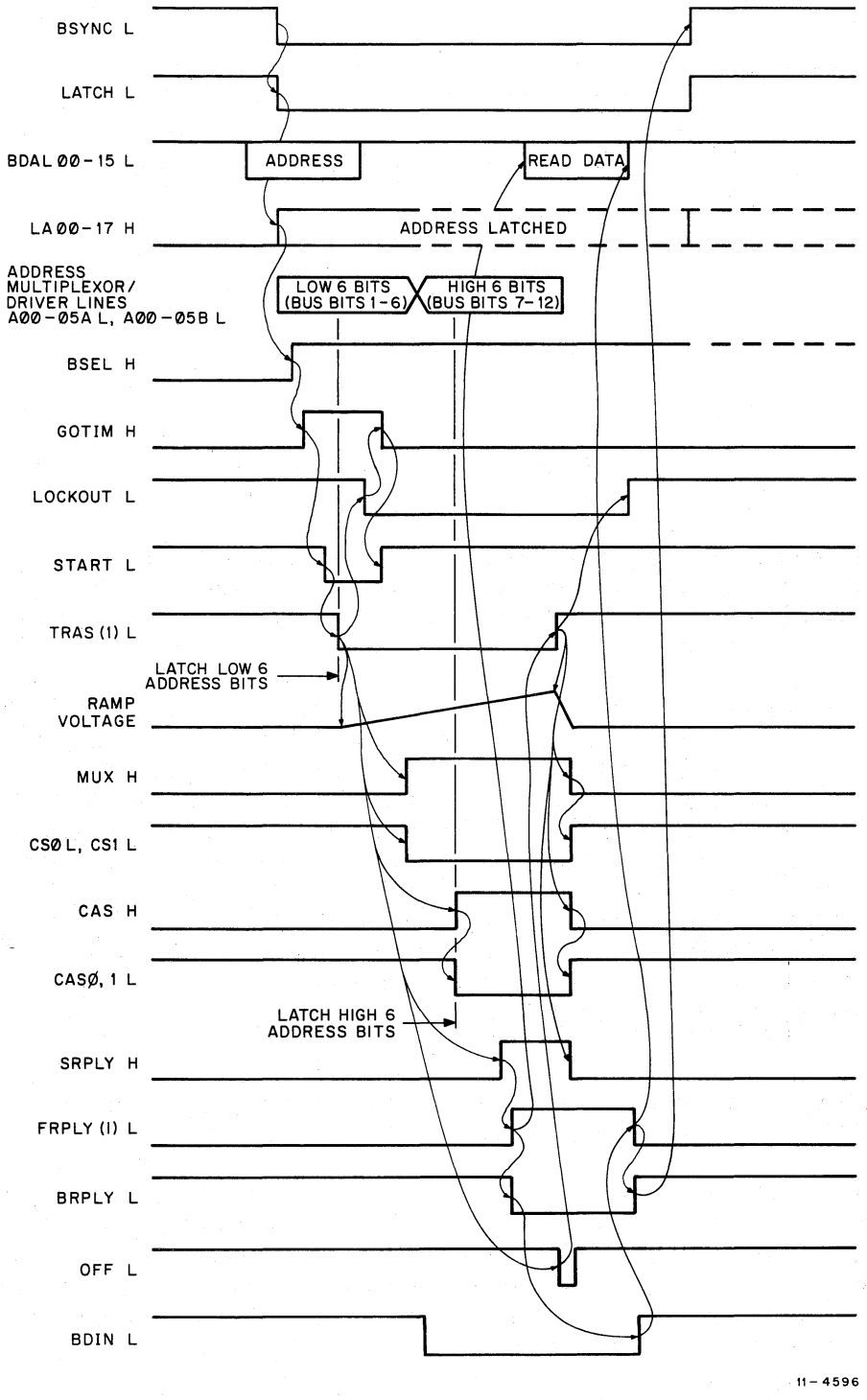

Figure 3-5 Read (DATI) Sequence

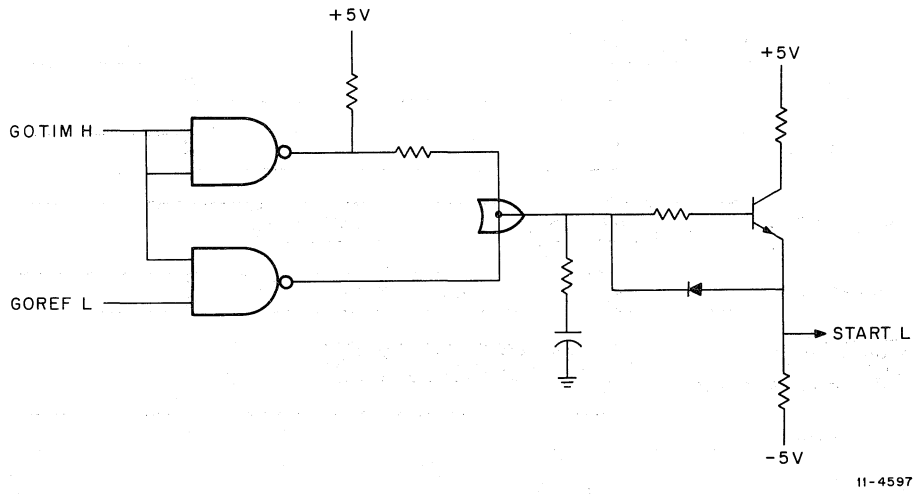

Figure 3-6 80 ns Delay Circuit

If an internal refresh cycle is in progress when BSYNC L is asserted, the memory read or write cycle cannot be executed until the refresh cycle has been completed. However, if an internal refresh cycle is requested after GOTIM H is generated for a read or write cycle, the read or write cycle is first executed.

START L is the active (low) delay circuit output and it sets the Row Address Strobe flip-flop. Active TRAS(1) H and TRAS(1) L signals are produced. Active TRAS(1) L is ORed with OFF L and the Lockout flip-flop to generate LOCKOUT L. LOCKOUT L is ANDed in the Read Cycle Initiate gate, the Write Cycle Initiate gate and the Internal Refresh gate to inhibit the GOTIM H signal from occurring until the present cycle is complete. The Lockout flip-flop is used to generate a delay from the reset of TRAS(1) L to ensure proper memory timing. TRAS(1) L is gated with passive (low) SRPLY H and INTREF H signals producing a high signal that clocks the Go Inhibit flip-flop to the set state; note that the high (active) RSYNC H signal applied to the data input of the flip-flop when clocked by the leading edge of TRAS(1) L enables the set state on the positive-going leading edge of the clock input to the flip-flop. The resulting high flip-flop output signal is ORed to produce an active (low) NODIN L signal that inhibits the Read Cycle Initiate gate to prevent multiple DATI cycles from occurring without RSYNC H being reset

TRAS(1) H enables column address strobe drivers that latch the high-order 6-bit address in the memory array later in the read cycle

TRAS(1) L activates an R-C ramp voltage generator that applies a rising voltage (Figure 3-5) to the voltage comparator circuits. Four voltage comparators, each having different reference voltage inputs, produce the four control signals: MUX H, CAS H, SRPLY H, and OFF L. The reference voltage applied to a comparator determines the point along the ramp voltage at which the comparator's output will change logical state. Hence, the reference voltage, relative to the ramp voltage, determines the time delay produced by each comparator circuit.

The first active signal produced by the comparator circuit is MUX H. MUX H selects the high order six address bits that are applied to the memory array. MUX H is ANDed with the passive REF L signal producing the active chip select (SC0 L and SC1 L) signals.

The next voltage comparator output signal that goes active is CAS H. CAS H is ANDed with the active TRAS(1) H signal producing the active column address strobe (CAS0 L and CAS1 L) signals. These signals latch the high-order six address bits in the memory array integrated circuits, completing the 12-bit address within the accessed 4K bank. Read data is then available on DOUTOO–15 H.

The next voltage comparator output signal that goes active is SRPLY H. SRPLY H is applied to a pulse generator circuit whose 30 ns output pulse is ANDed with the passive REF L signal; the resulting low pulse sets the Reply flip-flop, and FRPLY(1) H FRPLY(1) L signals go to their active states. The BRPLY L bus driver asserts the BRPLY L signal and driver portions of the bus transceivers, enabled by RDIN L (received BDIN L) and FRPLY(1) L, place the memory read data on BDAL00–15 L.

The last voltage comparator signal produced is OFF L. OFF L clears the Row Address strobe flip-flop and TRAS(1) H and TRAS(1) L go to their passive states. The passive (low) TRAS(1) H signal inhibits the column address strobe drivers and CAS0 L and CAS1 L go to their passive states. The passive (high) TRAS(1) L signal resets the ramp voltage and MUX H, CS0 L, CS1 L, CAS H, SRPLY H, and OFF L go to their passive states.

The bus master responds to the active BRPLY L signal by reading the data from the bus and terminating the BDIN L signal. BDIN L (passive) is received and inverted producing a negative-going trailing edge on BDIN H. RDIN H is ORed with RDOUT H producing a positive-going transition at the clock input of the Reply flip-flop. This transition clocks the flip-flop to the reset state. FRPLY(1) H goes low, inhibiting the BRPLY L bus driver and FRPLY(1) L goes high, inhibiting the BDAL00–15 L read data bus drivers. The bus master responds by terminating BSYNC L, and the memory read cycle is completed.

3.4.3 Memory Write Operation

A memory write (DATO or DATOB) cycle is somewhat similar to the memory read cycle described in Paragraph 3.4.2. However, during the addressing portion of the cycle, the bus master asserts BWTBT L, indicating an output (write) operation is to follow. The signal sequence for the timing and control logic write operation is shown in Figure 3-7. BWTBT is received (RWBT H) and latched by the active LATCH L signal; the address bits are latched in the same manner, as previously described. The latched signal (LWBT H) inhibits the Read Cycle Initiate gate and prevents immediate generation of the GOTIM H signal. However, the latched row address bits LA1–6 H are routed via the 3:1 address multiplexor to the memory array.

The bus master then places the write data on the BDAL bus and asserts BDOUT L. BDOUT L is received producing RDOUT H. RDOUT H is gated with passive (high) LOCKOUT L, FRPLY(1) L, and active WRITE ENBL H signals to produce the active GOTIM H signal.

Operation of the timing and control logic continues as described for read operation generation of the MUX H, CAS H, SRPLY H, and OFF L signals. However, the RDOUT signal enables WB0 L and/or WB1 L signal generation in the addressing logic, as described in Paragraph 3.2, and the received data is written in the addressed location.

The bus master responds to the BRPLY L signal by terminating BDOUT L and removing the write data from the BDAL bus lines. RDOUT H, which is ORed with the passive RDIN H signal, goes low, and the low to high transition resets the Reply flip-flop. BRPLY L then goes passive (high). The bus master responds by terminating BSYNC L and the write operation is completed.

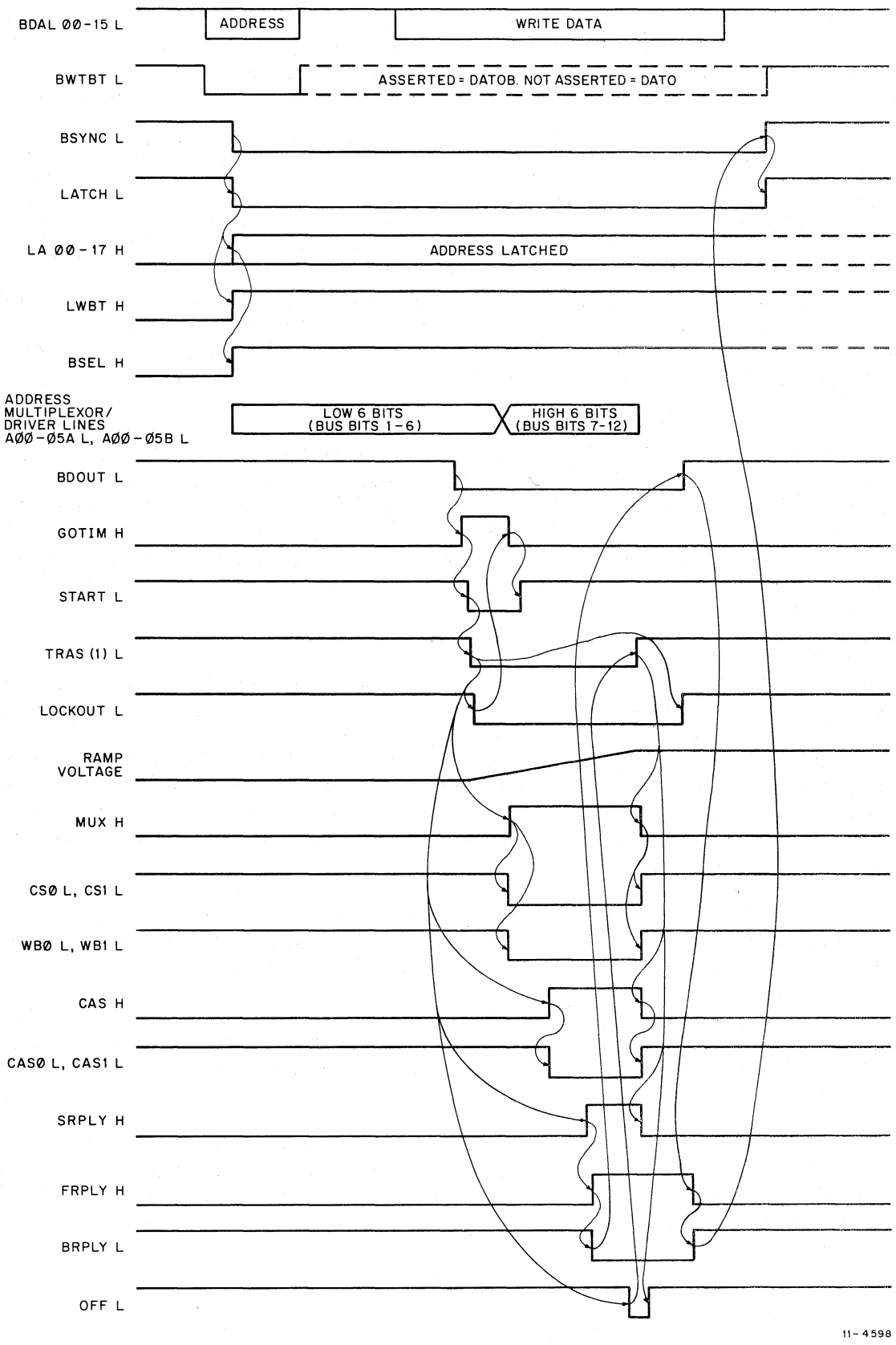

Figure 3-7 Write (DATO or DATOB) Sequence

3.4.4 Memory Read-Modify-Write Operation

The memory read-modify-write operation is produced by the DATIO (or DATIOB) bus cycle. The bus master first initiates a "memory read" operation at the addressed location. However, instead of terminating BSYNC L after the read portion of the cycle has been completed, BSYNC L remains asserted; the bus master places the write (modified) data on the bus and asserts BDOUT L. The MSV11-C responds by writing the data in the addressed word or byte location. The BWTBT L signal is asserted with the write data to indicate a DATIO bus cycle is in progress, when appropriate. Except for the addressing portion being omitted for the write portion of the DATIO (or DATIOB) bus cycle, operation of the MSV11-11 is as previously described for memory read and memory write operations.

3.5 MEMORY REFRESH OPERATION

3.5.1 General

Dynamic MOS memory integrated circuits comprising the memory array require periodic refreshing in order to retain stored data. This is accomplished by forcing a memory read operation on each of the 64 row addresses; one read operation is required for each row address. Each row address must be refreshed in this manner once every 2 ms (maximum).

MSV11-C memory refresh can be accomplished by using the on-board (internal) refresh logic signals, or by using refresh signals present on the LSI-11 bus (external refresh). The internal refresh circuit is most transparent to the LSI-11 system since it automatically refreshes one row address every 25 μs; neither LSI-11 microcomputer-generated refresh cycles nor DMA arbitration is required when the internal refresh mode is selected. When other memory system components in the LSI-11 system require LSI-11 bus memory refresh signals, such as the KD11-F's resident memory and the MSV11-B 4K memory option, the MSV11-C internal refresh mode can be disabled and the refresh operation can be controlled externally by LSI-11 bus signals.

Normally, external refresh is controlled by either the LSI-11 processor or by an intelligent DMA device. Processor-generated refresh signals consist of a series of 64 successive bus transactions. Each series of bus refresh transactions takes approximately 135 μs to complete and occurs at approximately 1.8 ms intervals. The REV11-A and REV11-C DMA refresh/bootstrap options are intelligent DMA devices. They execute one DMA refresh cycle with one memory row address every 25 μs (approximately). Note that when the external refresh mode is selected, all system memory components are refreshed simultaneously.

3.5.2 Internal Refresh

The MSV11-C refresh logic circuit is shown in Figure 3-8. The sequence of internal refresh operation is shown in Figure 3-9. When the internal refresh mode is selected, jumper W7 is installed, producing the active (high) CLK EN H signal. This signal activates the 25 μs clock and places a high level at the Internal Refresh Cycle flip-flop's data input. The positive-going transition of the 25 μs clock clocks the flip-flop to the set state, causing GO REF L and GO REF H to go to their active states (low and high, respectively). GO REF H conditions the data input of the Internal Refresh flip-flop.

When the MSV11-C is not involved in a read or write operation, FRPLY(1) L and LOCKOUT L are passive (Figure 3-4). These passive signals are gated with the active GO REF H signal, producing an active GOTIM H signal. The leading edge of GOTIM H clocks the Internal Refresh flip-flop to the set state and INTREF(1) H goes high. INTREF(1) H is ORed with the passive LAT EXT REF H signal to produce an active (low) REF L signal.

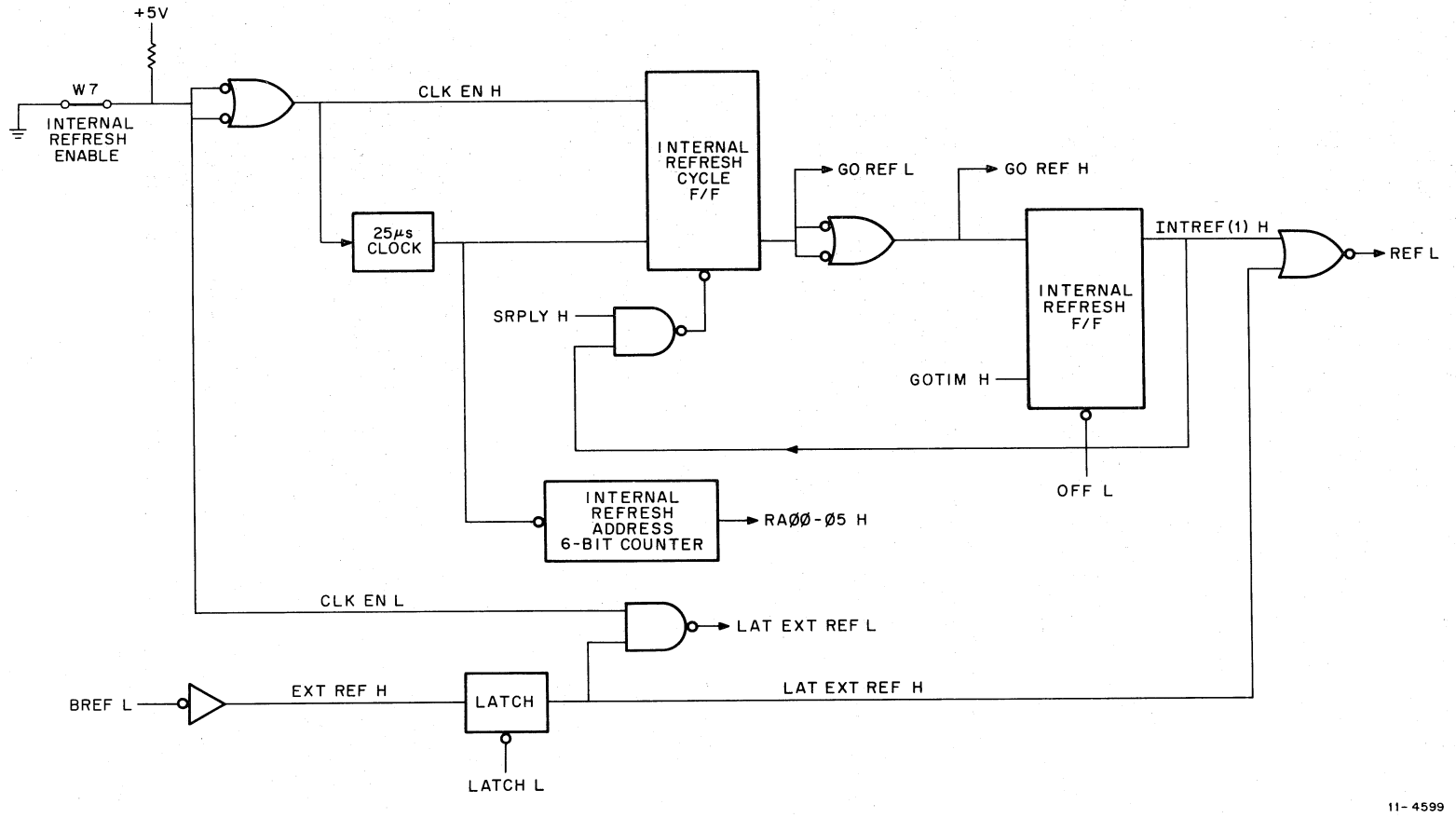

Figure 3-8 Refresh Logic

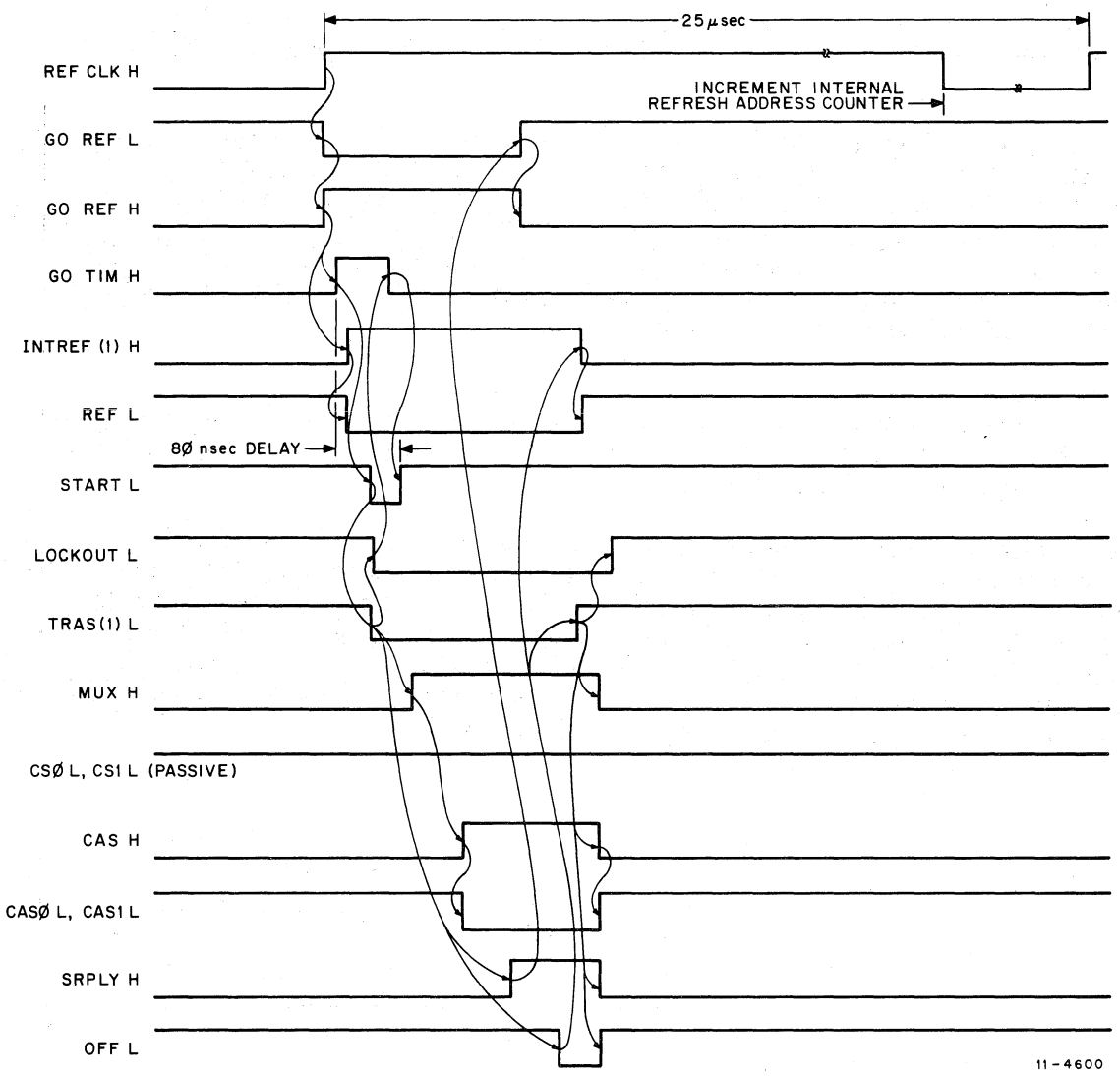

Figure 3-9 Internal Refresh Sequence

GO REF L is applied to the 80-ns delay dircuit (Figure 3-6) forcing the 80-ns delay to occur. The delay provides settling time for the Interrupt Refresh flip-flop. After the 80-ns delay has completed, START L goes active, setting the Row Address Strobe flip-flop, and TRAS(1) L and TRAS(1) H go to their active states. TRAS(1) L produces an active LOCKOUT L signal, inhibiting the GOTIM H signal. Operation then continues as in the memory read cycle, except the active INT REF(1) H signal selects RAOO–05 H refresh address (row) bits, which are routed through the address multiplexor and applied to the memory array; passive (low) column address bits are applied to the memory array during the active state of MUX H, but are not significant during the refresh operation. The active REF L signal, applied to the reply circuit via jumper W6, also inhibits SRPLY H from setting the Reply flip-flop and generating an erroneous BRPLY L signal.

SRPLY H is gated with INTREF(1) H, producing a low clear signal for the Internal Refresh Cycle flip-flop, and GO REF L and GO REF H go passive. GOTIM H goes passive and the 80-ns Delay Circuit START L signal goes passive. OFF L then goes active (low) clearing the Internal Refresh and Row Address Strobe flip-flops; REF L TRAS(1) L, LOCKOUT L, MUX H, CAS H, SRPLY H, and OFF L signals go to their passive states.

The internal refresh counter is incremented by the trailing edge of REF CLK H prior to the next internal refresh operation. Hence, each successive internal refresh operation uses the next sequential row address.

When a memory read or write operation is initiated just prior to the refresh operation, and the read or write cycle is still in progress, the leading edge of GOTIM H clocks the passive (low) GO REF H signal into the Internal Refresh flip-flop; INTREF(1) H remains reset for the duration of the memory cycle. The refresh operation will not be enabled until LOCKOUT L and FRPLY(1) L go passive (high) at the end of the read or write cycle, enabling a new GOTIM H signal. If this condition occurs, the leading edge of the new GOTIM H signal clocks the active (high) GO REF F signal into the Internal Refresh flip-flop, and the refresh operation continues as described previously.

3.5.3 External Refresh

When the external refresh mode is selected, jumper W7 is removed. CLK EN H goes low, and the Internal Refresh Cycle flip-flop cannot be set by the 25 μs clock signal. CLK EN L goes high, enabling one input to the LAT EXT REF L gate.

An external refresh cycle is initiated by the bus master asserting BREF L; EXT REF H goes high. The bus master places the refresh row address on the BDAL 1–6 L lines and asserts BSYNC L. BSYNC L produces the active (low) LATCH L signal that latches the 6-bit address in the address latch (Figure 3-3), and the EXT REF H signal (Figure 3-8), producing the active (high) LAT EXT REF H signal. This signal is gated with CLK EN L producing the LAT EXT REF L signal and forcing an active BSEL H signal in the addressing logic. Thus, the MSV11-C is addressed and enabled for the refresh operation. The external refresh signal sequence is shown in Figure 3-10.

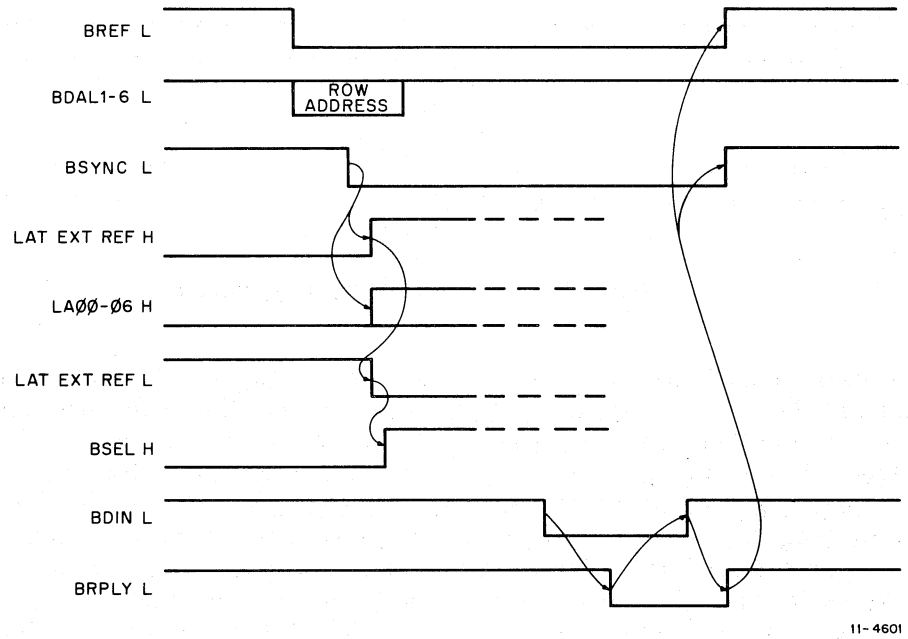

Figure 3-10 External Refresh Signal Sequence

The refresh operation continues as described for a memory read operation, except the active REF L signal (produced by the active LAT EXT REF H signals) inhibits a BRPLY L signal, as described for the internal refresh operation. If the MSV11-C must reply during the external refresh bus transaction, jumper W6 is removed; REF L will not inhibit the reply circuit and BRPLY L will be generated. Only one MOS memory module in a system is required to reply to the refresh bus transactions. The module that should reply is the module with the slowest access time relative to the bus master device. This module is generally the module located the greatest electrical distance on the LSI-11 bus from the bus master device controlling the refresh operation.

3.6 CHARGE PUMP CIRCUIT

The charge pump circuit (Figure 3-11) provides the -5 V power for the MOS memory array integrated circuits. The input power source for this circuit is +12 V. An oscillator circuit, running at approximately 40 kHz, produces a square wave drive signal to the rectified circuit. Q2 switches the ground alternation for the charge pump capacitors, reducing the switching current requirement for the oscillator circuit. The rectifier output is -10 V (approximately). The -5 V output is Zener diode regulated. Note that this circuit eliminates the need for backplane power other than the standard +5 V and +12 V. The circuit remains active when battery backup power is used and normal system power fails.

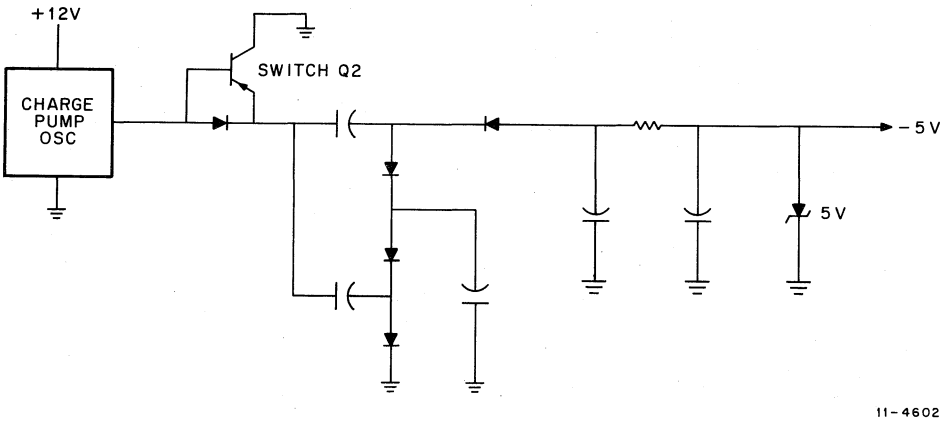

Figure 3-11 Charge Pump Circuit

CHAPTER 4
MAINTENANCE

4.1 GENERAL

Diagnostic programs are available to thoroughly test the MSV11-C memory. Memory diagnostic programs are included in the ZJV01-RB paper tape software option and the ZJ215-AY floppy disk software option. Detailed operating instructions and program listings are included with each diagnostic software option. Operating instructions involving the general use of system diagnostics (paper tape and floppy disk) are included in the *Microcomputer Handbook*, Section 1, Chapter 9.

When running diagnostics for testing the MSV11-C, "worst case" timing can be forced through the use of a "margin node" signal pin. This pin is located under the module at AL1. Normally it is not connected. However, by first connecting it to +5 V and running diagnostics and then connecting it to GND and running diagnostics, the worst case timing of the timing and control logic is forced. The MSV11-C should pass diagnostic tests under these conditions.

If faults are detected by the diagnostic program, either the module can be returned to DIGITAL for service as directed in the *Microcomputer Handbook*, Section 5, Chapter 3, or repaired by the user. A flowchart describing normal MSV11-C operation is included in Figure 4-1 as a troubleshooting aid. Also, refer to the troubleshooting chart (Table 4-1) and diagnostic symptoms to isolate faults.

A faulty module in which one or more 4K memory banks remain operative can be reconfigured and used, less the faulty bank. Wire-wrap jumpers W4, W8, W12, and W16 provide this function. A procedure for this operation is provided in the following paragraphs.

4.2 CONFIGURING JUMPERS W4, W8, W12, AND W16

4.2.1 Configuring the MSV11-CB (Figure 4-2)

If one 4K bank is faulty and one bank remains operative, proceed as directed below. The MSV11-CB will then function as a 4K memory and its starting address can be configured as directed for the MSV11-CA in Table 2-1.

First Bank Faulty

1. Remove jumpers W4 and W8.
2. Connect (wire-wrap) a new jumper from W4 to W8A.

Second Bank Faulty

1. Remove jumper W8. No additional configuring is required.

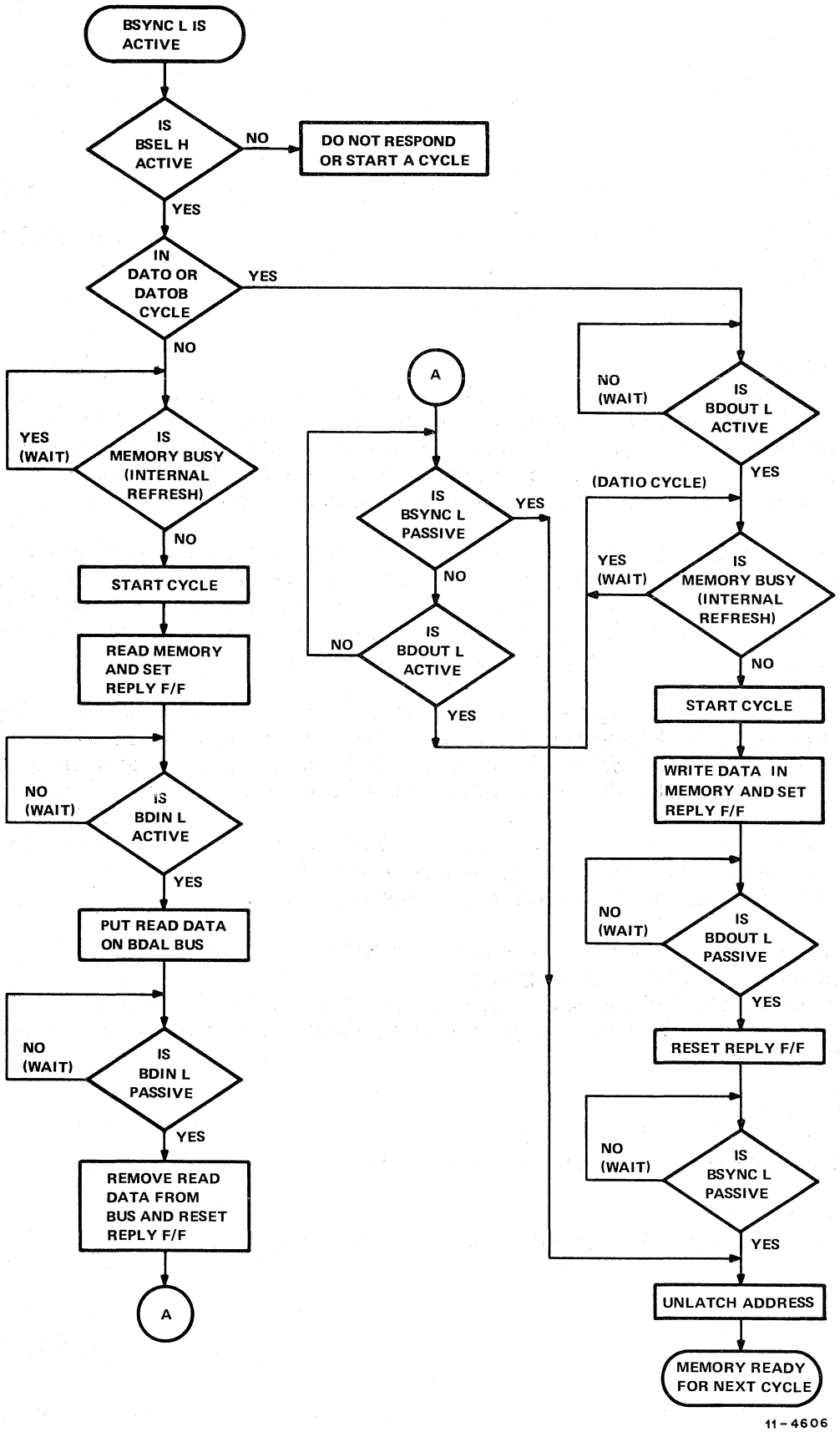

Figure 4-1 Normal MSV11-C Operation

Table 4-1 MSV11-C Troubleshooting Chart

Possible Fault / Failure Symptom	-5.1 V	BDAL bus transceivers	BSYNC L receiver	BDIN L receiver	BDOUT L receiver	BDCOK H receiver	BWTBT L receiver or latch	Address latch	Address multiplexor	Address space selection logic	GOTIM H logic	Logic signal timing	Read cycle Go Inhibit F/F	Reply F/F and bus driver	LOCKOUT L logic	Byte addressing logic	CASO L, CAS1 L drivers	RASA-D L drivers	Address drivers	BREF L bus receiver and latch	Internal refresh logic flip-flops	Int. Ref. Cycle Init. logic	25 μsec. clock	Int. ref. addr. counter	Memory array*	Memory array integrated circuit	+5 V	+12 V
Memory does not respond to BSYNC L			•	•	•					•	•	•	•	•	•					•	•	•					•	
Memory hangs bus		•										•		•														
DATI fails	•	•	•	•				•	•	•	•	•	•	•	•	•	•	•	•	•	•	•			•		•	•
DATO fails	•	•	•		•	•	•	•	•	•	•	•		•	•	•	•	•	•	•	•	•			•		•	•
DATIO fails	•	•					•						•		•	•												
Byte failure		•					•									•									•			
Many bits fail with internal ref.	•								•		•	•	•		•						•	•	•	•	•		•	•
Many bits fail with external ref.	•											•								•	•				•		•	•
Intermittent bit failures	•											•			•						•	•	•			•	•	•
Drops bits	•											•								•	•	•	•		•	•	•	•
4 bits fail		•																							•			
1 bit fails		•																							•	•		
Fails all addresses	•		•	•	•	•		•	•	•		•					•	•	•						•		•	•
Fails A1-A6		•						•	•			•						•	•									
Fails A7-A12		•						•	•			•					•		•									
Fails A13-A17		•						•		•																		

***NOTE: Memory array failures consist of shorted or open circuit board etch or multiple memory integrated circuit failures.**

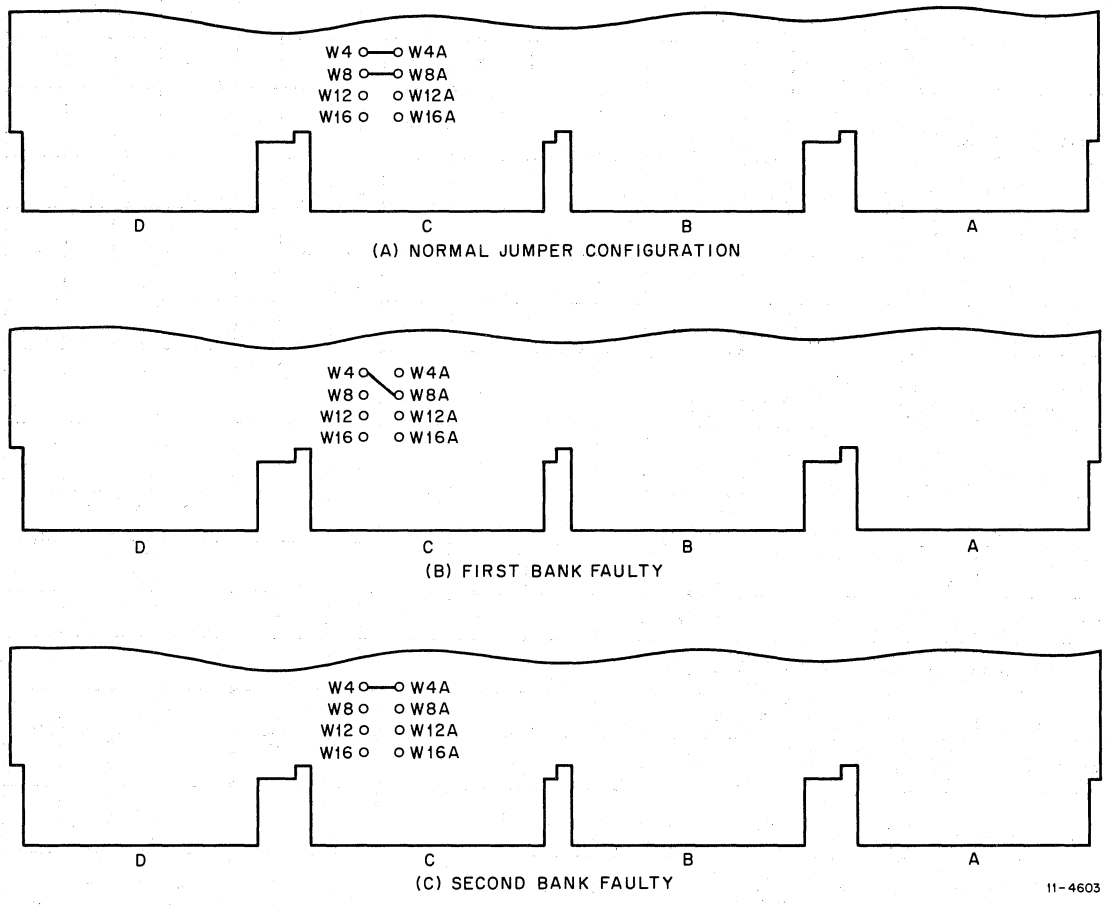

Figure 4-2 Reconfiguring MSV11-CB Bank Jumpers

4.2.2 Configuring the MSV11-CC (Figure 4-3)

If one 4K bank is faulty and two banks remain operative, proceed as directed below. The MSV11-CC will then function as an 8K memory and its starting address can be configured as directed for the MSV11-CB in Table 2-1.

First Bank Faulty

1. Remove jumpers W4 and W12.
2. Connect a new jumper from W4 to W12A.

Second Bank Faulty

1. Remove jumpers W8 and W12.
2. Connect a new jumper from W8 to W12A.

Third Bank Faulty

1. Remove jumper W12. No additional configuring is required.

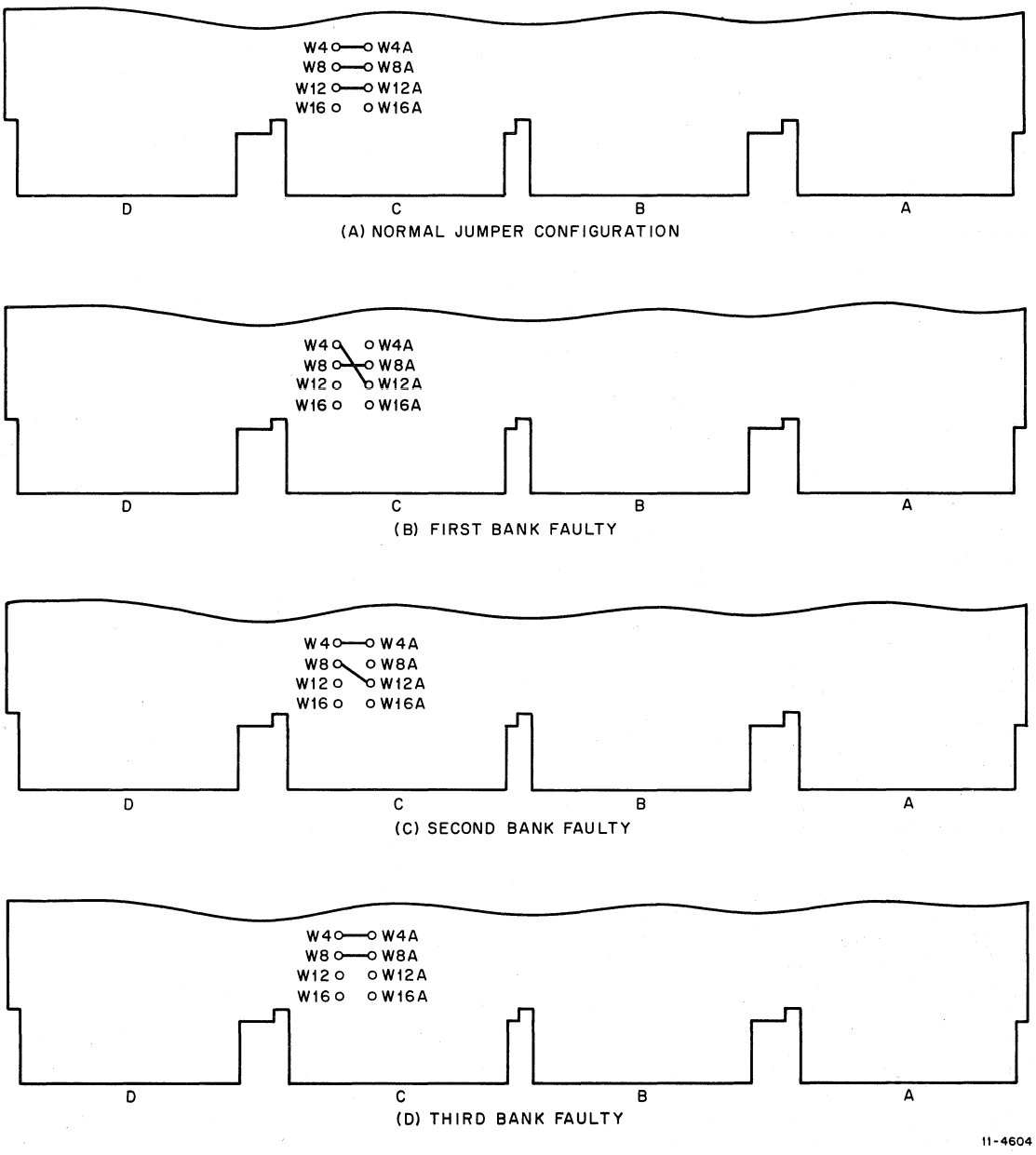

Figure 4-3 Reconfiguring MSV11-CC Bank Jumpers

4.2.3 Configuring the MSV11-C (Figure 4-4)

If one 4K bank is faulty and three banks remain operative, proceed as directed below. The MSV11-C will then function as a 12K memory and its starting address can be configured as directed for the MSV11-CC in Table 2-1.

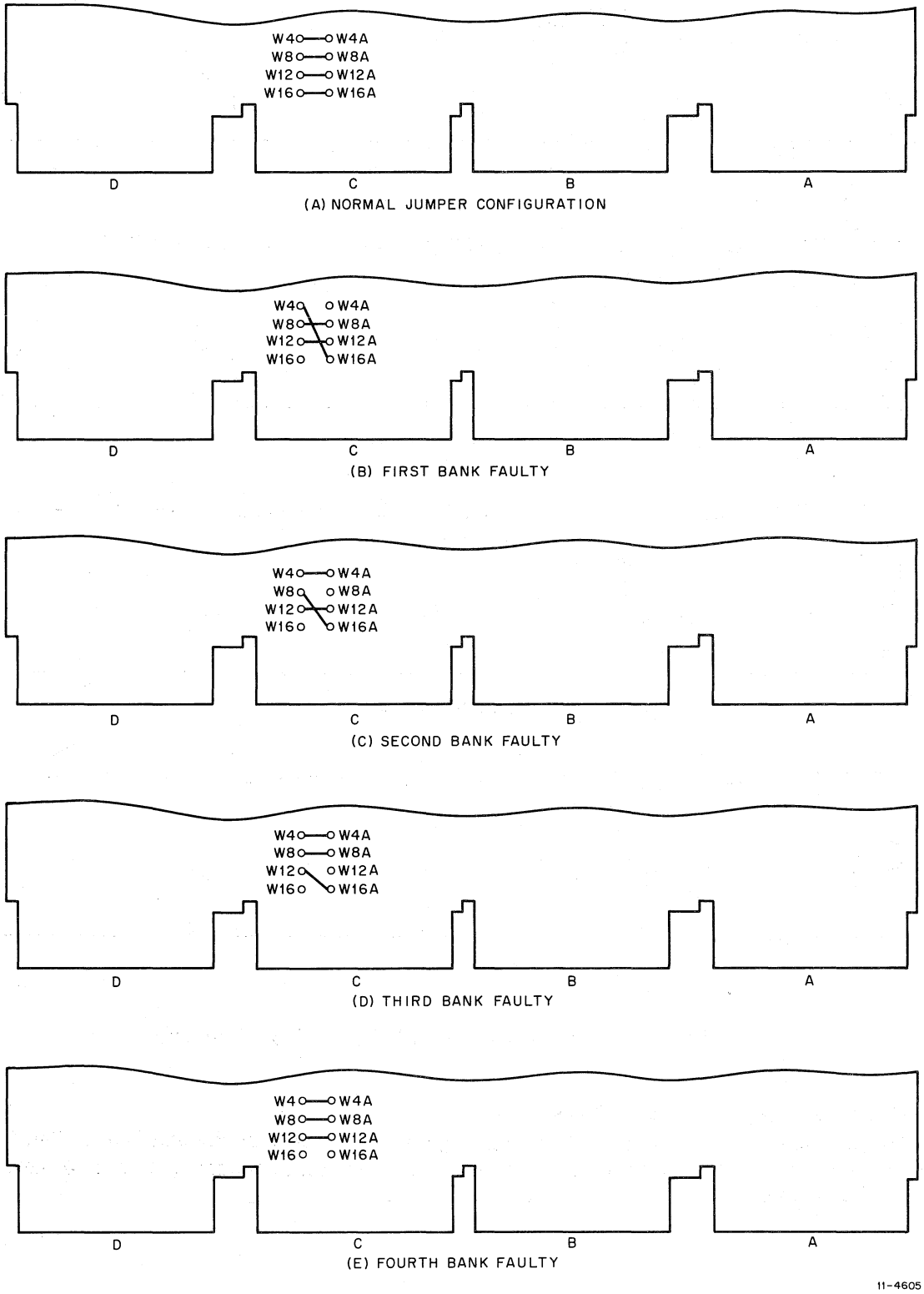

Figure 4-4 Reconfiguring MSV11-CD Bank Jumpers

First Bank Faulty

1. Remove jumpers W4 and W16.
2. Connect a new jumper from W4 to W16A.

Second Bank Faulty

1. Remove jumpers W8 and W16.
2. Connect a new jumper from W8 to W16A.

Third Bank Faulty

1. Remove jumpers W12 and W16.
2. Connect a new jumper from W12 to W16A.

Fourth Bank Faulty

1. Remove jumper W16. No additional configuring is required.

MSV11-C USER'S MANUAL
EK-MSV11-OP-001

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