pdp11

M7850 parity controller maintenance manual

digital

EK-M7850-MM-001

M7850 parity controller maintenance manual

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CHAPTER 1
INTRODUCTION

1.1 GENERAL

This manual describes the theory and function of the M7850 parity controller. The function of the M7850 is to increase confidence that the data retrieved from a memory address is the same data that was put in. The parity controller checks the data by the use of a code referred to as *parity*.

The M7850 contains circuitry to generate and check parity, as well as circuitry which reacts to a parity error (data not checked as correct). The controller also contains a Control and Status Register (CSR) which stores information in case of a parity error. The CSR also contains control bits used elsewhere in the parity controller. The CSR has its own address and can be read (DATI) or written into (DATO) by any system device acting as Unibus master.

1.2 PARITY CONCEPT

The controller generates parity bits based on the data written into memory (DATO). One parity bit is assigned to each data byte in a data word. The two parity bits are designated P0 (assigned to an even byte) and P1 (assigned to an odd byte). The parity bit is based on the number of 1s which exist in a byte of data. The M7850 uses ODD parity. ODD parity means that the parity bit will be set or cleared in order to make the number of 1s ODD. (Refer to Figure 1-1.) The parity bits are stored in memory along with the data bytes.

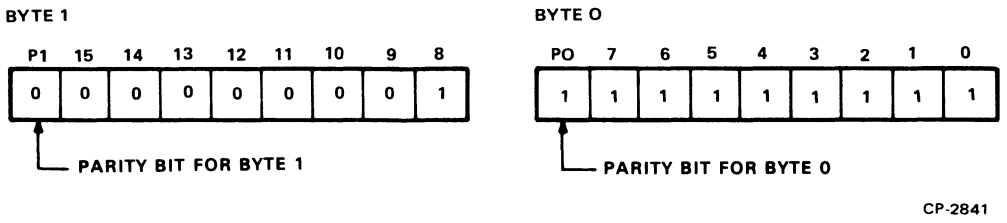


Figure 1-1 Parity Byte Assignment

When data is retrieved from memory (DATI), the data and the stored parity bits (P0, P1) are presented to the parity controller. The parity of the data from memory is recalculated and compared to the stored parity bits (P0, P1). If the parity bits correspond, the data is assumed to be correct; if the parity bits do not correspond, the data is assumed to be unreliable.

1.3 PARITY LIMITATION

The parity check does have a limitation. If a memory error causes an even number of bits to change state in a data byte, the parity remains the same. Therefore, an incorrect data byte is checked as correct.

1.4 SYSTEM INTERRELATIONSHIP BETWEEN M7850 AND MEMORY MODULES

The M7850 parity controller is a double-height module that fits into any modified Unibus slot of the backplane. It is a PDP-11 system requirement that there be one M7850 in each backplane which contains a parity memory module(s). One M7850 will generate and check parity on data for all memory modules placed in its backplane.

A 9-slot backplane (DD11-P or DD11-D) can contain from one to six memory modules and a 4-slot backplane (DD11-C) can contain one or two memory modules. The memory modules are all hex-height modules which contain 4K to 16K bytes of data. Therefore, an M7850 can accommodate from 4K to 96K bytes of memory data in a 9-slot backplane and from 4K to 32K bytes in a 4-slot backplane. One backplane can contain core or MOS memory, or a combination of both types. The M7850 does not differentiate between core and MOS memory. Refer to Table 1-1 for a list of available memories.

Table 1-1 Memories Used with M7850 Parity Controller

Memory	Memory Description	Applicable Manual
MM11-CP	8K CORE	MM11-C/CP
MM11-DP	16K CORE	MM11D/DP
MS11-EP	4K MOS	MS11-E-J
MS11-FP	8K MOS	MS11-E-J
MS11-JP	16K MOS	MS11-E-J

The parity controller and memory communicate data and address information with the rest of the PDP-11 system via the Unibus. Other communication between the parity controller and the memory modules is achieved via an internal bus. The internal bus is present on all but the first and last slots of the backplane and does *not* leave the backplane. (Refer to Figure 1-2.)

1.5 M7850 ELECTRICAL SPECIFICATIONS

The electrical specifications of the M7850 parity controller are given in Table 1-2.

Table 1-2 M7850 Parity Controller Specifications

Voltage Requirements	+5 V ±5% with less than 0.05 V p-p ripple
Current Requirements	1.0 A max, 0.75 A typical
Power Dissipation	5 W max
Environmental	
Ambient Temperature	0° to 60° C (32° to 140° F)
Relative Humidity	0–90% (non-condensing)
Unibus Unit Load	1

The access times required for a data transfer between a system device and a memory module or the M7850 are given in Table 1-3.

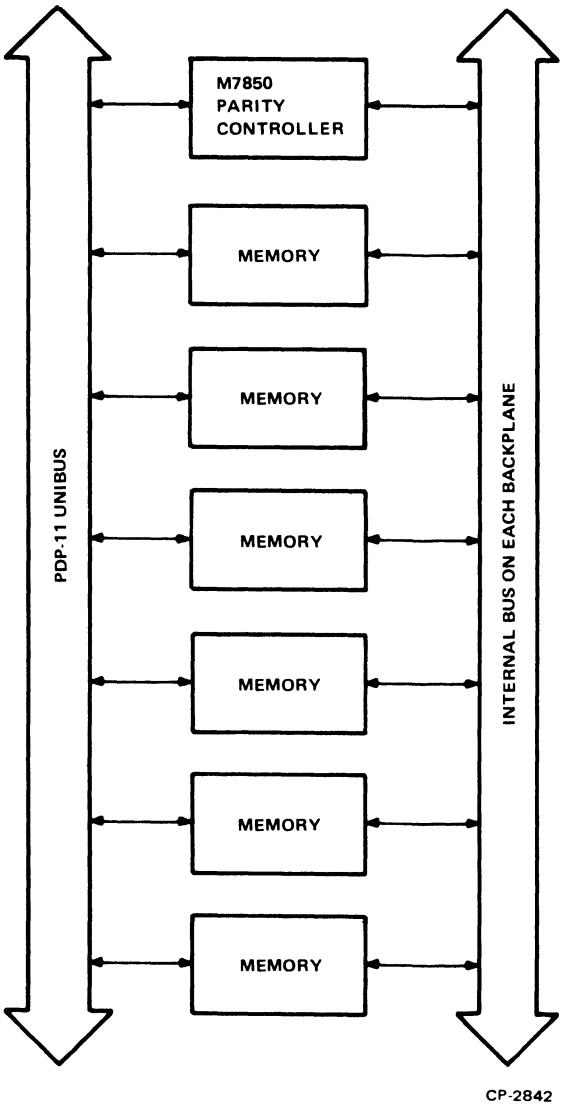


Figure 1-2 Unibus/Internal Bus Simplified Block Diagram

Table 1-3 Maximum Access Times

Bus Mode	Access Time
DATI-DATIP (Memory)	No parity error: mem. acc. time + 150 ns With parity error: mem. acc. time + 200 ns
DATO-DATOB (Memory)	mem. acc. time + 40 ns
DATI-DATIP (CSR)	120 ns
DATO-DATOB (CSR)	120 ns

NOTES:

1. The access times for the parity controller are defined from INT BUS SSYN L (pin BE1) to BUS SSYN L (pin BU1).

2. The parity computation time (DATO-DATOB) is 55 ns max, defined from the time data is valid at the output of the parity module receivers to when parity bits P0 and P1 are asserted on the "internal" bus.

The M7850 parity control module is shown in Figure 1-3.

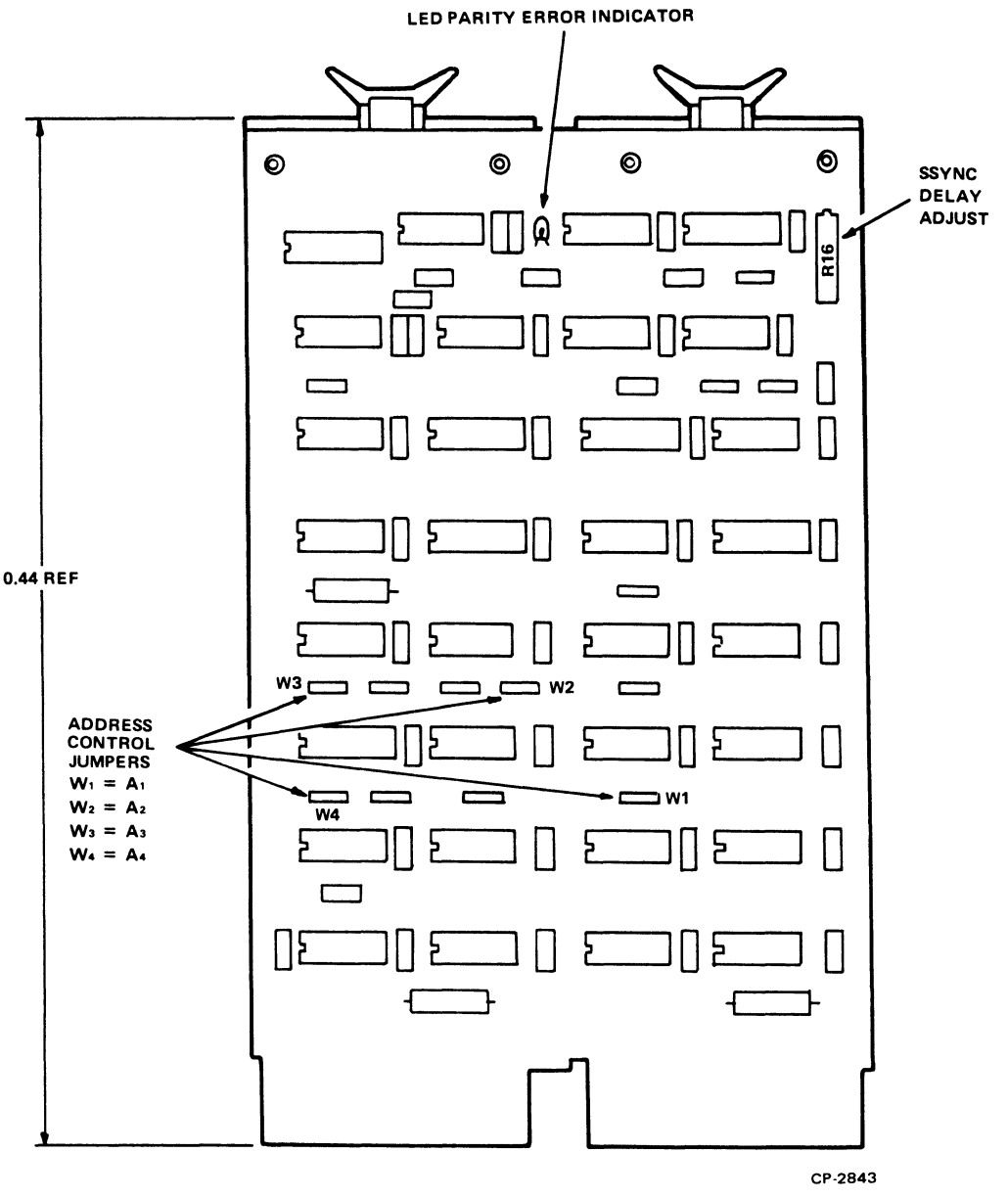


Figure 1-3 Physical Layout of M7850

CHAPTER 2
FUNCTIONAL DESCRIPTION

2.1 COMMUNICATION LINES BETWEEN M7850 AND MEMORY MODULES

The M7850 parity controller and memory modules communicate via the internal bus. They communicate with the rest of the PDP-11 system via the Unibus. (Refer to Figure 2-1.)

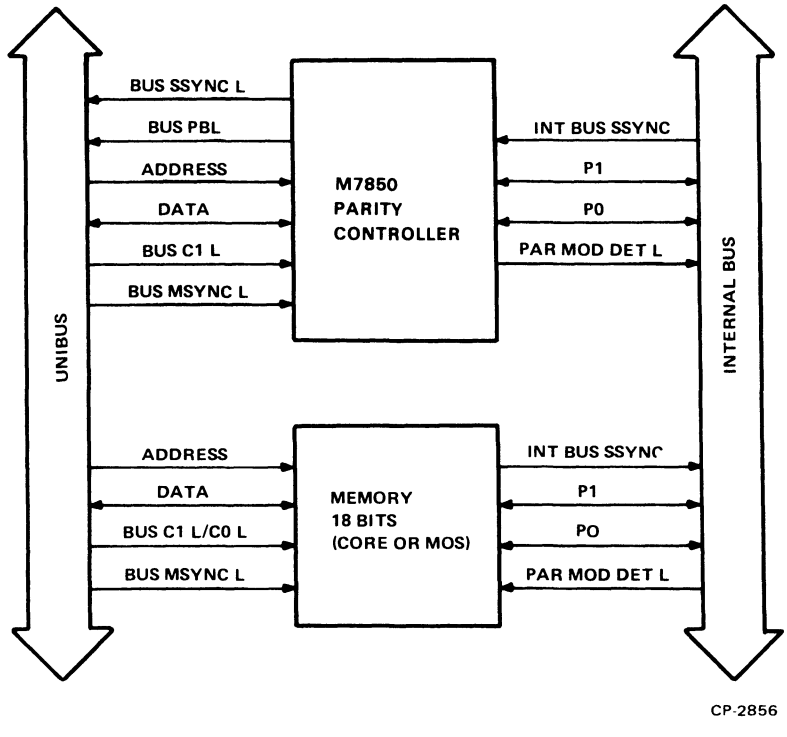


Figure 2-1 Unibus/Internal Bus Connections

The memory modules and the parity controller receive address (A17–A00) data (D15–D00) and control (BUS MSYNC, BUS C1) information from the Unibus. The parity controller has its own address. The M7850 need not be addressed to activate its parity control function. The parity controller will either generate or check parity as soon as data is available on the Unibus. The address of the parity controller is only used by the PDP-11 system to access the parity control CSR register.

The internal bus is for communication between the parity controller and the memory modules only. This bus consists of four signal lines which carry the following signals.

1. Parity Module Detect (PAR MOD DET L) - This signal is asserted whenever the M7850 parity module is plugged into the backplane. Once asserted, this signal switches control of BUS SSYN from the memory modules to the parity controller. The parity controller issues BUS SSYN instead of a memory module.

2. Internal Bus Slave Sync (INT BUS SSYN L) - This signal is asserted by a memory module when the memory has placed or latched in data on the Unibus (DATO or DATI). The signal causes the assertion of BUS SSYN by the M7850 when it too has finished its part of a data transfer (DATO or DATI). No action is taken by the Unibus master in the time between the assertion of INT BUS SSYN and BUS SSYN. In a DATI only, the assertion of INT BUS SSYN also initiates part of the parity check circuitry in the M7850.

3. INT BUS P0 H - This is the parity bit for byte 0 of a data word.

4. INT BUS P1 H - This is a parity bit for byte 1 of a data word.

NOTES:

1. ODD parity is used.

2. P0 and P1 are on a two-way bus (passes in both directions between memory and M7850).

The internal bus is physically placed in the modified Unibus section of the backplane. The position of the internal bus in both the 9-slot (DD11-D, DD11-P) and 4-slot (DD11-C) backplanes is shown in Figure 2-2.

Each bus line passes through a connector in slots 2–8 in a 9-slot backplane or in slots 2–3 in the 4-slot backplane. The connector and pin assignments are as follows:

1. PAR P0 - section A, pin P, side 1 (e.g., A07P1)
2. PAR P1 - section A, pin N, side 1 (e.g., A07N1)
3. PAR MOD DET L - section B, pin E, side 2 (e.g., B07E2)
4. INT SSYN - section B, pin E, side 1 (e.g., B07E1)

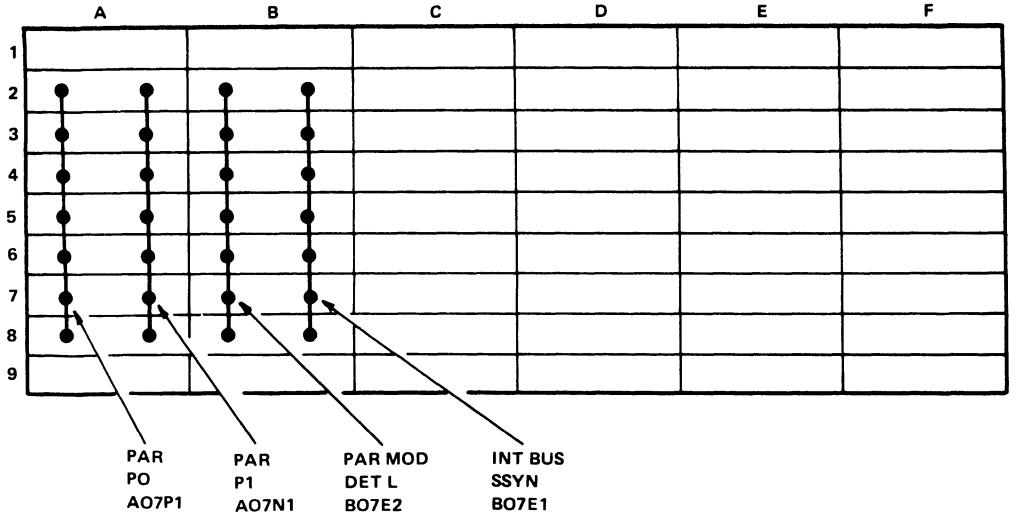
Refer to the applicable maintenance manual for a detailed explanation of the backplane connections.

An internal bus does not connect to other backplanes in the PDP-11 system.

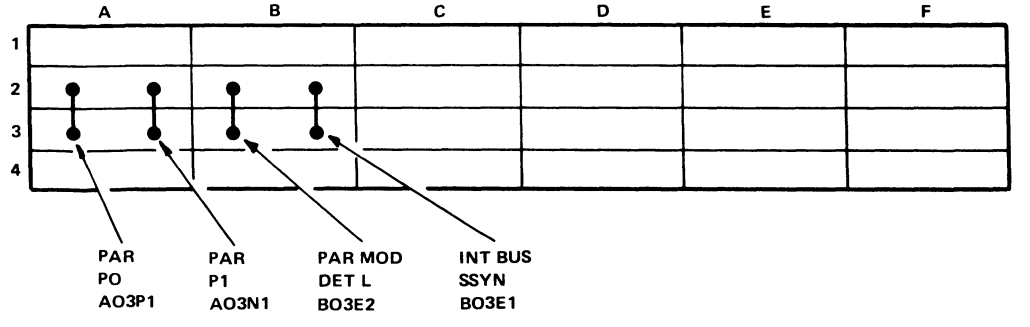
NOTE

The M7259 (old parity module) is not compatible with the M7850. The M7259 goes into a dedicated memory slot. Refer to maintenance manual EK-MF11-U/UP-MM-003.

Figure 2-3 is a block diagram of the M7850. The M7850 contains circuitry for the generation and checking of parity, as well as the CSR, which can be accessed by a Unibus master. The action taken by the M7850 in a data transfer is examined in the remaining sections of this chapter.



INTERNAL BUS ON 9 SLOT BACK PLANE (DD11-D or DD11-P)



INTERNAL BUS ON 4 SLOT BACKPLANE

CP-2855

Figure 2-2 Internal Bus Physical Location

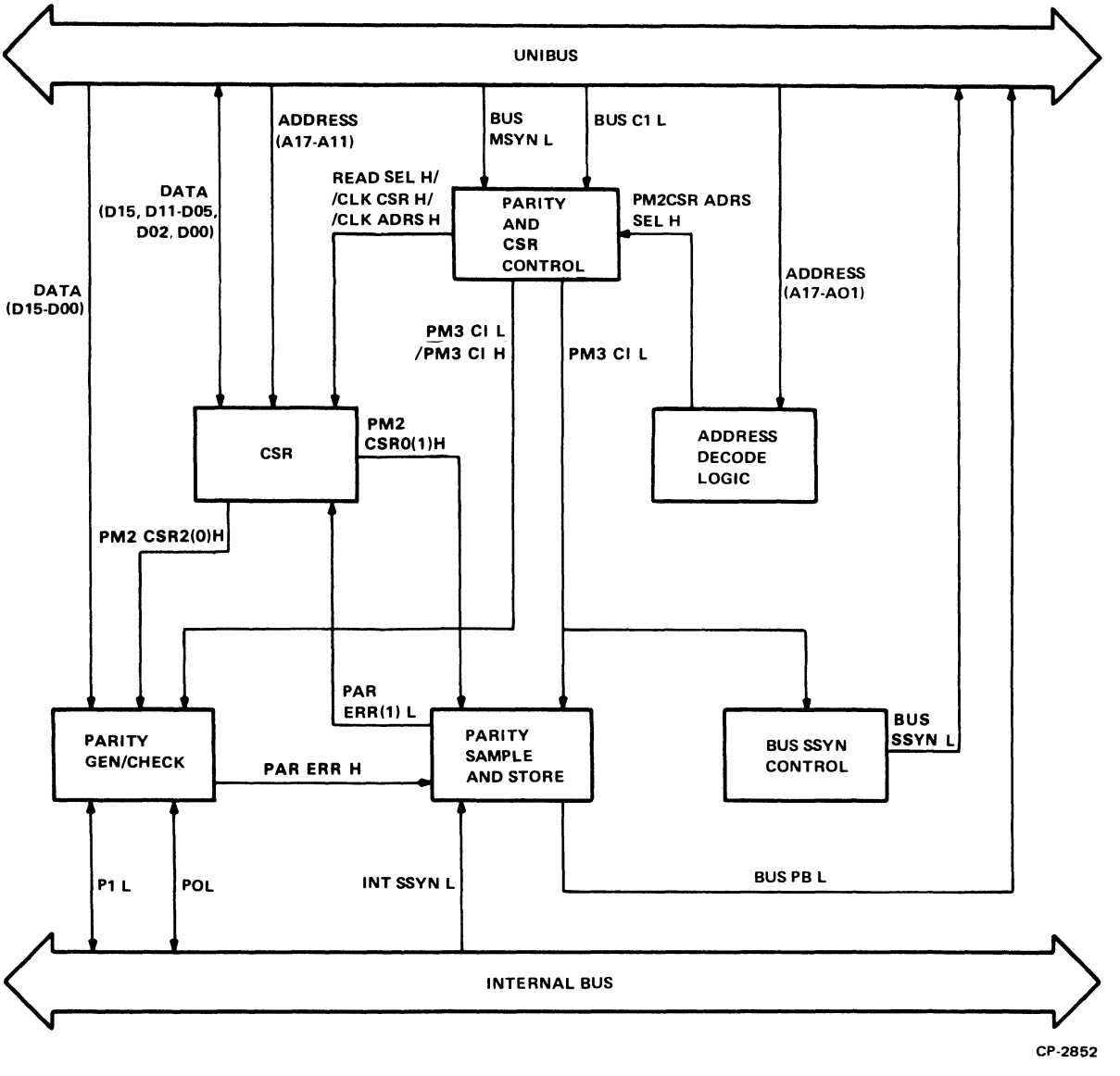


Figure 2-3 M7850 Block Diagram

2.2 DATO/DATOB DATA TRANSFER ACCESSING MEMORY MODULE

The M7850 parity controller is activated when a memory module is accessed for retrieval (DATI) or storage (DATO) of data. To write data into memory (DATO/DATOB) the Unibus master presents address, data, and control information to the M7850 and to the memory modules via the Unibus. The address (A17–A00) on the Unibus is for a location in memory and control signal BUSC1 is asserted, indicating a DATO/DATOB. (Refer to Figure 2-4.)

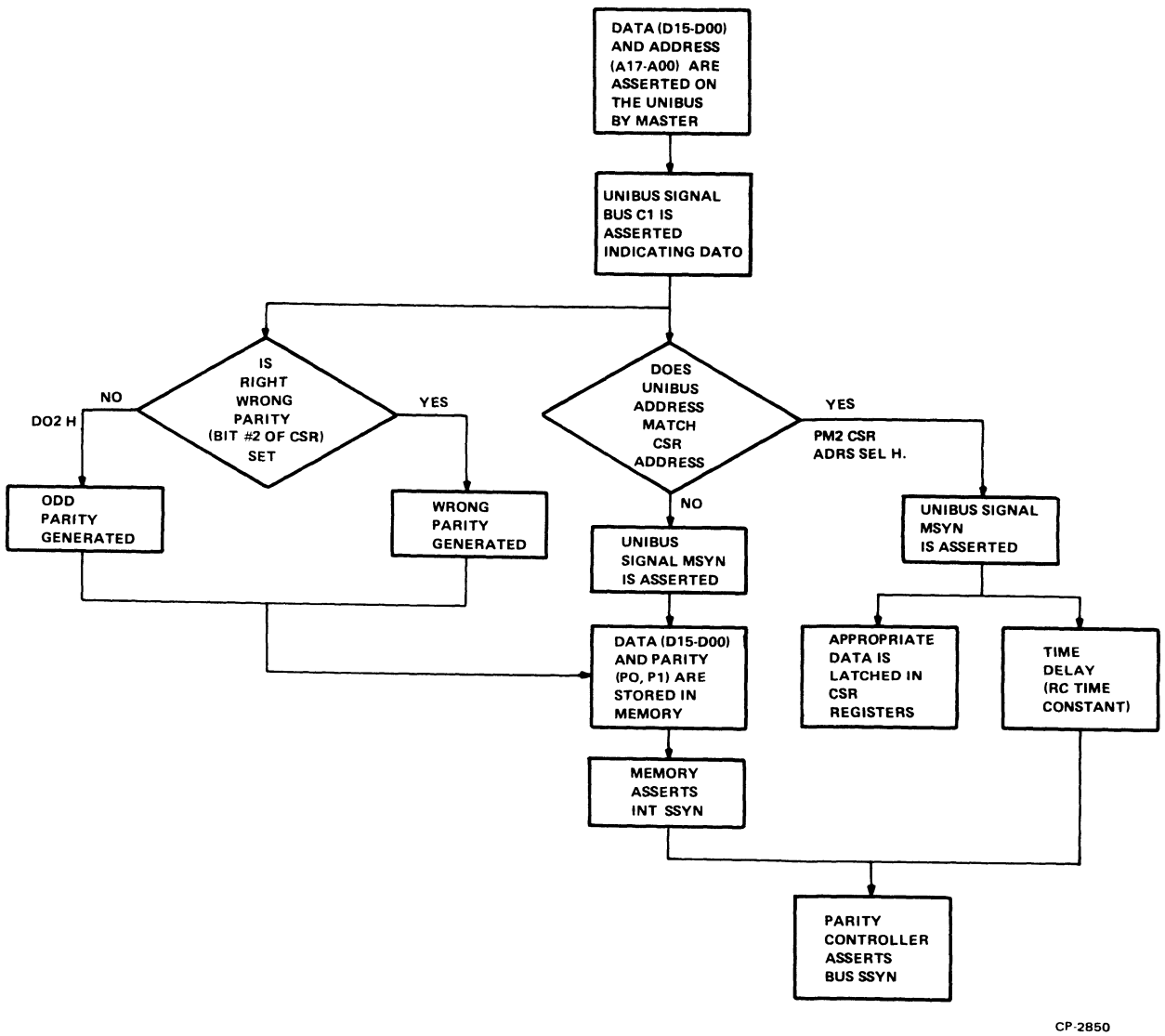


Figure 2-4 DATO Flow Diagram

The assertion of BUS C1 enables the M7850 to generate parity based on data which is present on the Unibus. The type of parity generated depends on the status of bit 2 in the CSR. Under normal operating conditions, ODD parity is generated (bit 2 is cleared). For diagnostic purposes, the wrong (even) parity can be produced (bit 2 is set). Refer to Paragraph 2.5 for a discussion of the CSR.

The generated parity bits (P0, P1) are placed on the internal bus by the M7850.

When the Unibus master asserts MSYN, the appropriate memory module recognizes the Unibus address (A17–A00) and then latches in and stores the Unibus data and the corresponding parity. The memory asserts INT SSYN after it has latched in the information. The memory takes no further external action in this DATO data transfer.

The assertion of INT SSYN causes the M7850 to assert BUS SSYN. This signal tells the Unibus master that the memory and parity controller have finished their tasks.

2.2.1 DATO Data Transfer Accessing the CSR (Figure 2-4)

For diagnostic purposes, the Unibus master can write data (DATO) in the CSR which is contained in the M7850. The address (A17–A00) presented on the Unibus is the CSR address, and BUS C1 is asserted, indicating a DATO/DATOB. The M7850 decodes the address on the Unibus and indicates address recognition by asserting PM2 CSR ADRS SEL H. The assertion of both BUS C1 and PM2 CSR ADRS SEL H causes the M7850 to latch in the Unibus data when MSYN is asserted by the Unibus master. The MSYN signal is also used by the M7850 to generate the BUS SSYN signal. The BUS MSYN signal is delayed by an RC time constant before it asserts BUS SSYN. The assertion of BUS SSYN by the M7850 indicates to the Unibus master that the M7850 has finished its task.

2.3 DATI-DATIP TRANSFER ACCESSING MEMORY

The M7850 parity controller is activated when a memory module is accessed for retrieval (DATI) or storage (DATO) of data. To read data from memory (DATI/DATIP) the Unibus master presents address and control information to the M7850 and the memory modules via the Unibus. The address (A17–A00) presented on the Unibus is for a location in memory and control signal BUS C1 is *not* asserted, indicating a DATI/DATIP. (Refer to Figure 2-5.)

When the Unibus master asserts MSYN, the appropriate memory module places the desired data (specified by A17–A00) on the Unibus (D15–D00), and its corresponding parity bits (P0, P1) on the internal bus. The memory module also asserts INT SSYN which is delayed 110 ns by the M7850 circuitry. The assertion of INT SSYN indicates to the M7850 that the memory module has placed data on the Unibus and parity bits on the internal bus.

The parity of the data on the Unibus is recalculated and compared to the corresponding parity bits (P0, P1) on the internal bus. The delayed INT SSYN signal then commands the parity controller to sample and store the results of the parity check. If there is a parity error, the stored signal PM3 PAR ERR is asserted and appropriate action is taken. Refer to Paragraph 2.4 for a discussion of the effects of a parity error. If no parity error exists, the parity controller takes no further action other than asserting BUS SSYN.

2.3.1 DATI Data Transfer Accessing CSR (Figure 2-5)

For diagnostic purposes, the Unibus master can read data (DATI) from the CSR, which is contained in the M7850. The address (A17–A00) presented on the Unibus is the CSR address and BUS C1 is *not* asserted, indicating a DATI/DATIP.

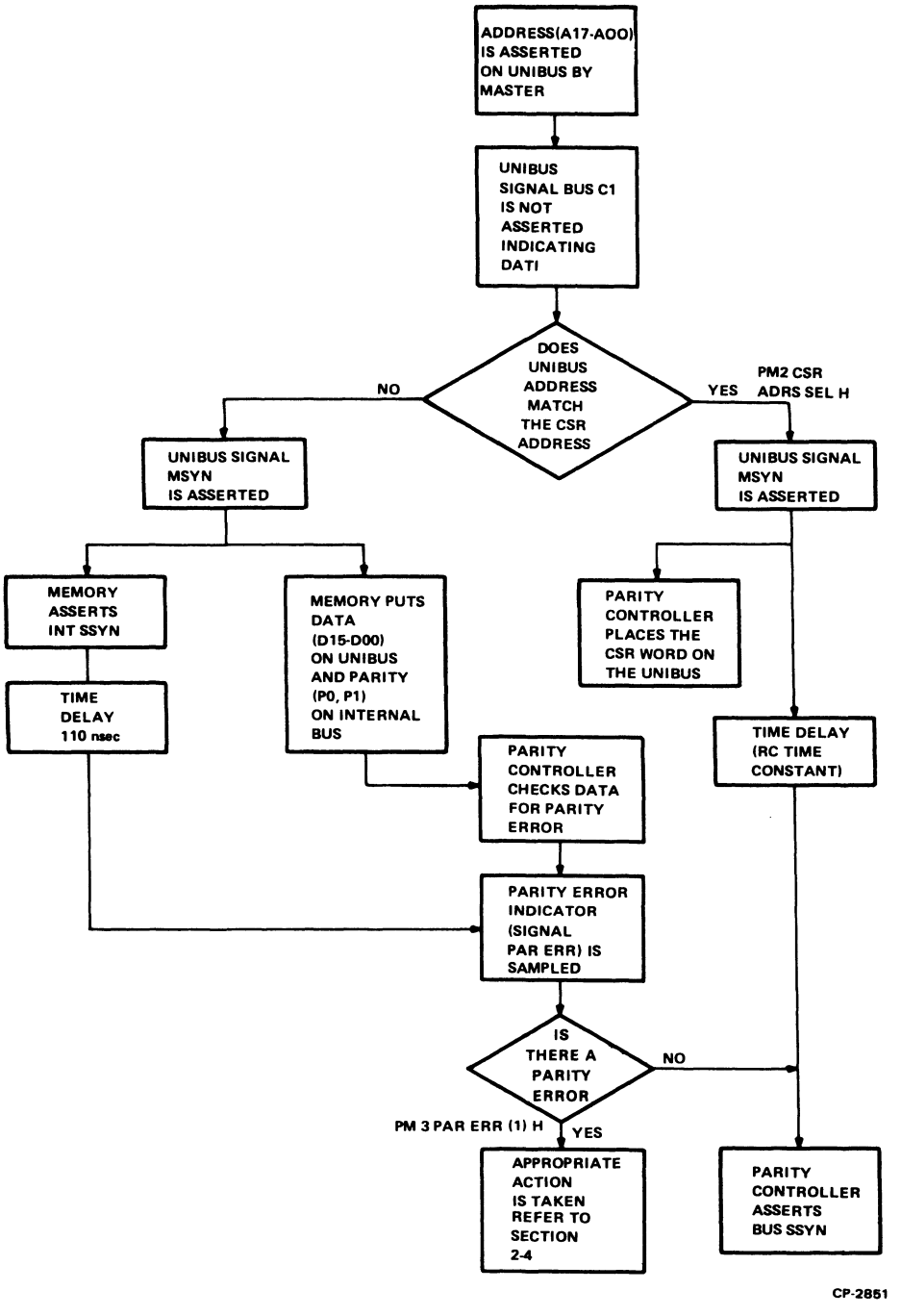


Figure 2-5 DATI Flowchart

The M7850 decodes the address (A17–A00) on the Unibus and indicates address recognition by asserting PM2 CSR ADRS SEL H. The assertion of PM2 CSR ADSR SEL H when BUS C1 is *not* asserted causes the M7850 to place the data contained in the CSR on the Unibus when BUS MSYN is asserted by the Unibus master. Signal BUS MSYN is also used by the M7850 to generate the BUS SSYN signal. The BUS MSYN signal is delayed by an RC time constant before it asserts BUS SSYN. The assertion of the BUS SSYN by the M7850 indicates to the Unibus master that the M7850 has finished its task.

2.4 REACTION TO A PARITY ERROR

Once a parity error has been detected, the M7850 initiates several of the following actions. (Refer to the flowchart in Figure 2-6.)

1. Bit 15 of the CSR is set (to DATA1).

2. Part of the address (A11–A17) of the faulty data word is recorded in the CSR (bits 5–11).

NOTE

Steps 1 and 2 have no affect on the PDP-11 system unless the CSR is read by the processor at a later time. The CSR is discussed in Paragraph 2.5 of this manual.

3. A LED, located toward the back of the M7850 circuit board, is turned on, *providing a visual indication of a parity error*, which may be useful for debugging purposes. The LED stays on until bit 15 of the CSR is reset by the software.

4. If bit 0 in the CSR register is set (DATA1) the parity controller asserts BUS PB. Bit 0 is not affected by a parity error. This bit was written into the CSR by a Unibus master in a previous DATO data transfer. The assertion of BUS PB is a warning given to the processor that a parity error has occurred.

5. The M7850 waits an extra 25 ns before asserting BUS SSYN. This time delay is referenced to the time BUS SSYN would have been asserted if there was no parity error.

The time delay gives the parity controller enough time to carry out the previous steps.

A general discussion of how a PDP-11 system processor reacts to a parity error is presented here. A detailed discussion is presented in the applicable processor manual. The assertion of BUS PB by the M7850 indicates to the processor that a parity error has occurred. There is a wire jumper on the processor board referred to as the parity jumper. If this jumper is installed in the proper position, the processor will recognize the assertion of BUS PB by setting a parity flag. Once the parity flag is set, the processor can service the parity error at the end of the current instruction of the main program.

NOTE

Refer to the applicable processor manual for priority service order.

To service a parity error the processor performs a trap. The trap vector is 114. This location contains the starting address of the parity error routine. The subsequent action of the processor is dependent on the PDP-11 system software for a parity error.

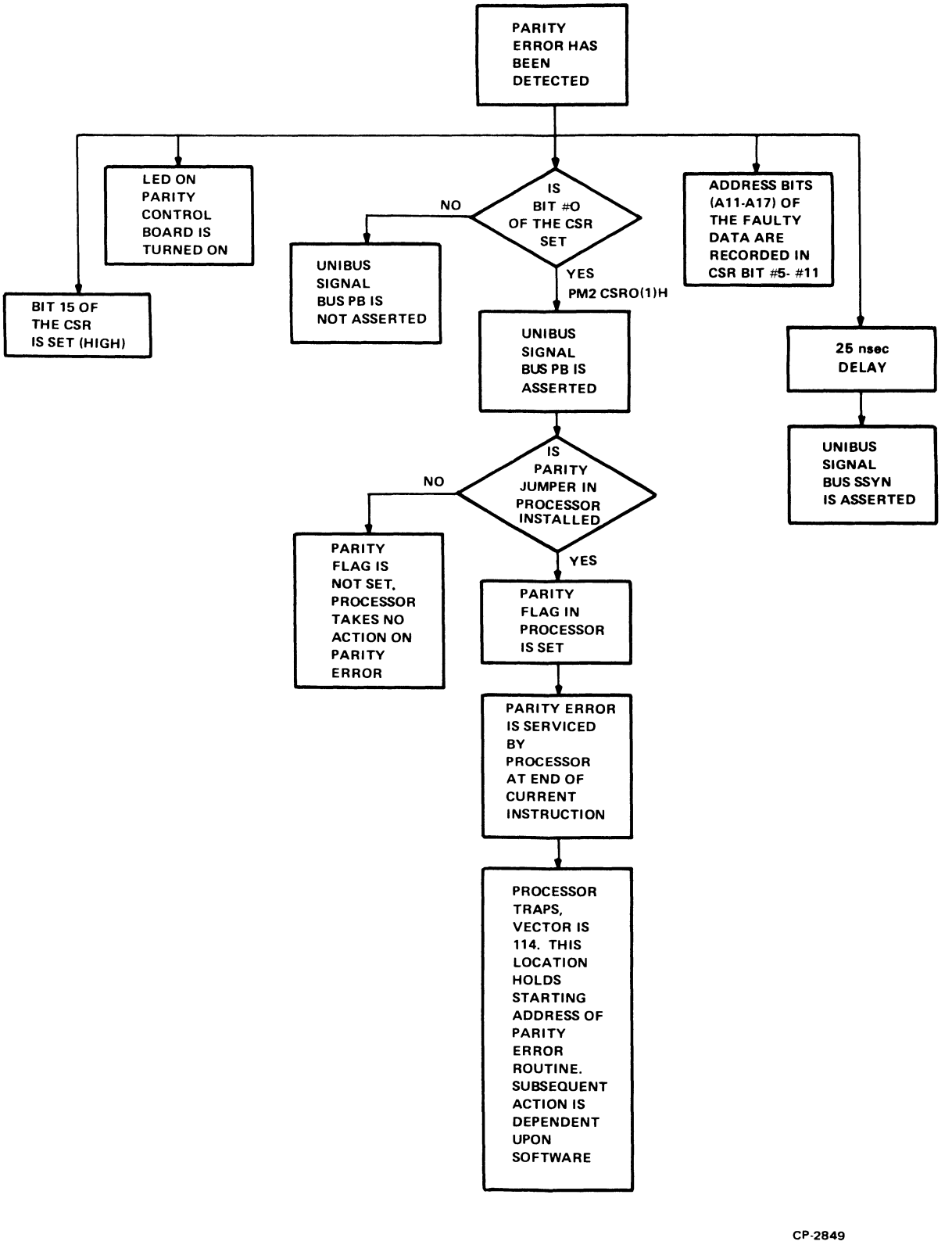


Figure 2-6 Parity Error Flowchart

2.5 CONTROL AND STATUS REGISTER (CSR)

A group of data registers contained in the M7850 are collectively referred to as the CSR. The CSR can be thought of as one 16-bit register which has its own location address. The contents of the CSR can be either read (DATI) or changed (DATO) by a Unibus master via the Unibus. The CSR contents are also changed when a parity error has occurred. The CSR bit assignments are illustrated in Figure 2-7 and are described as follows:

1. Bits 1, 3, 4, 12, 13, and 14 are not used. They contain no data. These bits are always read as a DATA 0.

2. Bit 0 (Error Indication Enable) – If this bit is set (DATA1) the M7850 will assert BUS PB when a parity error occurs. If this bit is not set (DATA0) BUS PB cannot be asserted under any condition. The state of bit 0 can be changed by the Unibus master in a DATO data transfer to the CSR. Unibus signal BUS INIT clears this bit.

3. Bit 2 (Write-Wrong Parity) – If this bit is cleared (DATA0) the parity controller will generate odd parity based on data transferred into memory (DATO/DATOB). If bit 2 is set (DATA 1) even (incorrect) parity will be generated. A parity error is then caused on a read (DATI) cycle of this data. The state of bit 2 can be changed by the Unibus master in a DATO data transfer to the CSR. Unibus signal BUS INIT clears this bit.

4. Bits 5–11 (Error Address) – Once a parity error has occurred, these bits contain the six highest-order address bits (A17–A11) of the faulty data which caused the parity error. The stored address bits describe the location of faulty data to within 1K of memory. Therefore, the memory module involved in the parity error can be located by using the partial address contained in bits 5–11. The software operating system has the ability to lock out (prevent the access of) a 1K block of memory that is specified by a programmer.

5. Bit 15 (Parity Error Bit) – This bit is set (DATA1) by the M7850 when a parity error occurs. Bit 15 is a flag, but it does *not* cause a parity error trap in the processor. Unibus signal BUS INIT clears this bit.

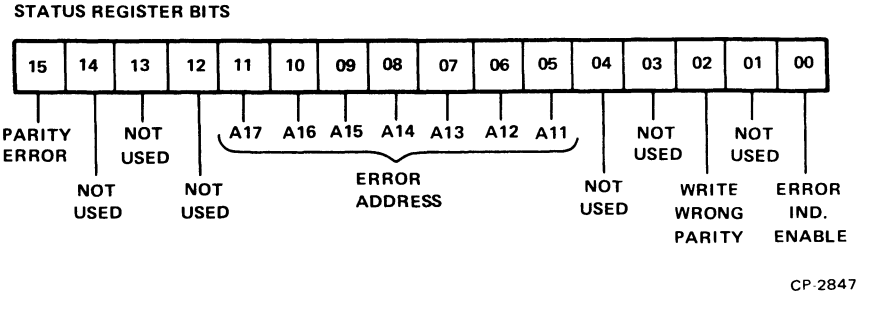


Figure 2-7 Control and Status Register Bit Allocation

The address of the CSR is determined in the M7850 circuitry; the address bits are shown in Figure 2-8.

Address bit A00 is not decoded by the address select logic. Address bits (A04–A01) are determined by wired jumpers (W4–W1) on the M7850 circuit board which are placed on the board during installation. Refer to Table 4-1 for further information on jumper installation (W4–W1).

NOTE

The CSR address has NO relevance to either the number or addresses of the memory modules that are controlled by an M7850 parity controller.

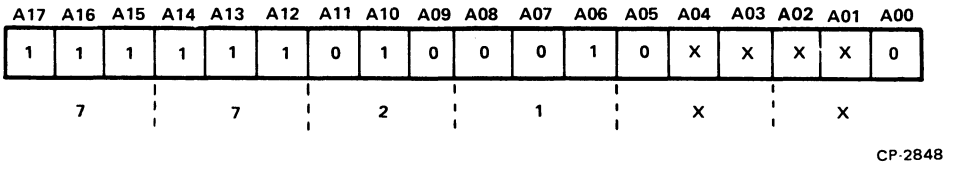


Figure 2-8 CSR Address Bits

CHAPTER 3
DETAILED CIRCUIT DESCRIPTION

3.1 INTRODUCTION

This chapter discusses the circuitry involved in the M7850. Refer to Figure 2-3 for the M7850 block diagram.

The address decode logic and the CSR control are discussed in Paragraphs 3.2.1 and 3.2.2, respectively. The CSR is discussed in Paragraph 2.5. The parity control and parity generation/checking (gen/check) circuitry are discussed in Paragraphs 3.3, 3.3.1, and 3.3.2. The parity sample and store circuitry, and its effect when a parity error has occurred, is discussed in Paragraphs 3.4 and 3.4.1. The BUS SSYN control circuitry, which applies when a memory module is accessed, is discussed in Paragraph 3.4.2.

3.2 CIRCUITRY INVOLVING ACCESS TO THE CSR

The CSR has its own address and can be read from (DATI) or written into (DATO) by a Unibus master. The CSR, its control circuit, and the address decode logic are shown in Figure 3-1.

3.2.1 Address Decode Logic

From the Unibus, data receivers E2, E3, E11, and E12 accept data information; address receivers E28, E29, E18, and E26 accept address information. Logic devices E30, E19, and E27 collectively decode the address (A17–A01) on the Unibus. When the CSR address (772100–772136) is on the Unibus, the outputs of decoding gates E30, E19, and E27 are all asserted, which results in the assertion of CSR ADRS SEL H (E31 pin 1). The assertion of CSR ADRS SEL H tells the CSR control circuit that the CSR is to be accessed by the Unibus master in a DATI or DATO data transfer.

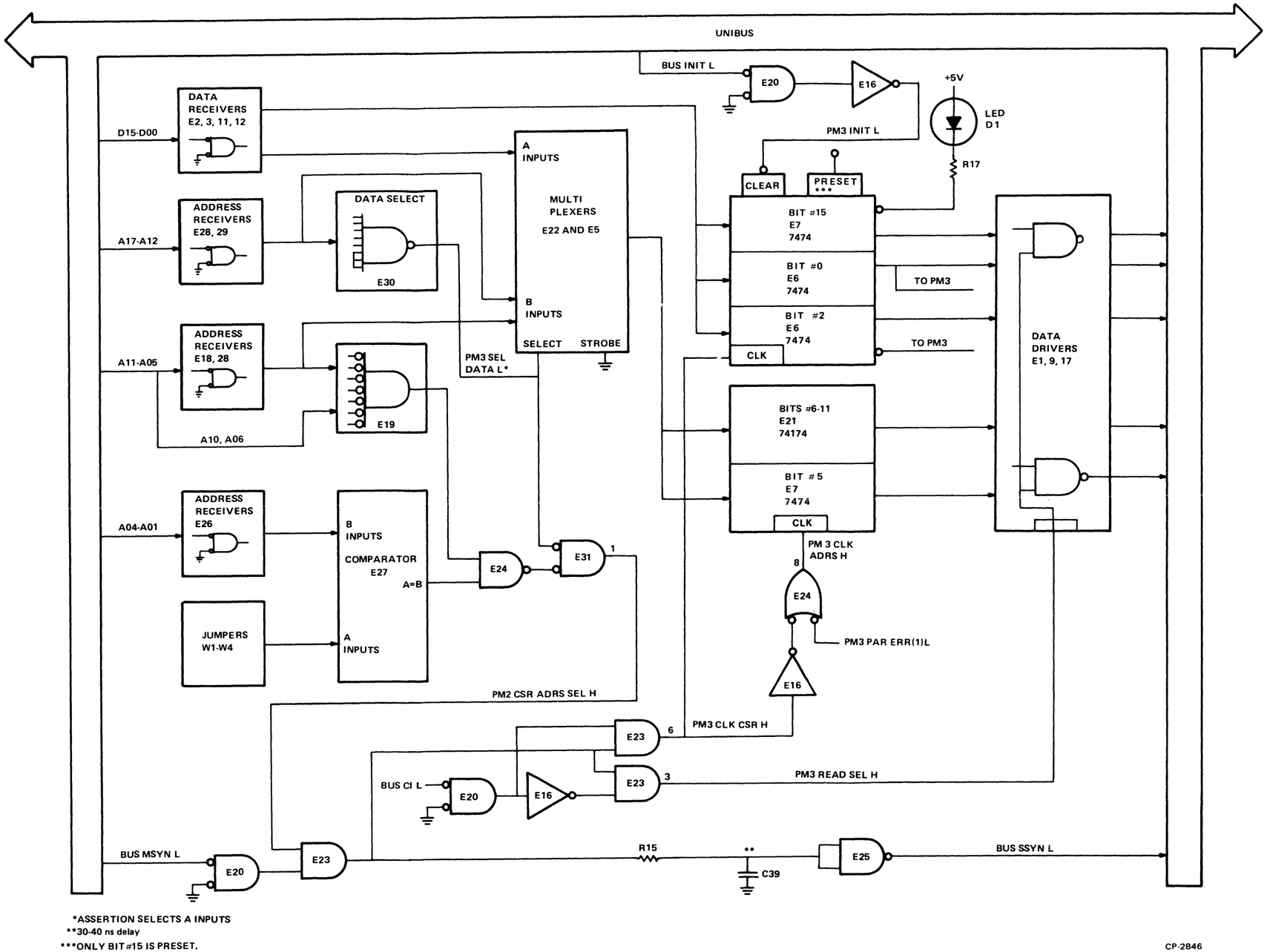
The assertion of SEL DATA L (E30) also presents the A inputs (D15–D05) of the multiplexers (E5, E22) to bits 5–11 of the CSR. When the CSR is *not* accessed by the Unibus master (SEL DATA L NOT asserted) the B inputs (A17–A11) are presented to bits 5–11 of the CSR. Data received from the Unibus is presented directly to bits 0, 2, and 15 of the CSR.

3.2.2 CSR Control Circuit

The CSR control circuit (E20, E23, E16, E24) determines when the CSR is written into (DATO) or read from (DATI). The control circuit has three signal inputs.

In a DATO data transfer involving the CSR, both CSR ADRS SEL H and BUS C1 L are asserted. Therefore, when BUS MSYN is asserted, two other signals are asserted which clock the data into the CSR. Signal CLK CSR H (E23 pin 6) clocks in bits 15, 0, 2; signal CLK ADRS H (E24 pin 8) clocks in bits 5–11.

In a DATI data transfer involving the CSR, signal CSR ADDRS SEL H is asserted but BUS C1 L is *not* asserted. Therefore, when BUS MSYN is asserted, signal READ SEL H is also asserted (E23 pin 3), which enables the data drivers (E1, E9, E17) to place the contents of the CSR on the Unibus.



*ASSERTION SELECTS A INPUTS
**30-40 ns delay
***ONLY BIT#15 IS PRESET.

CP-2846

Figure 3-1 CSR Address and Control Circuitry

3.2.3 BUS SSYN Control When the CSR is Accessed

In both a DATO and DATI involving the CSR, the BUS MSYN signal is also used to generate BUS SSYN. The BUS MSYN signal is delayed 30 to 40 ns by an RC time constant ($\tau = R_{15} C_{39}$) before asserting BUS SSYN. The time delay ensures the M7850 enough time to finish its part of a data transfer before BUS SSYN is asserted.

NOTE

The Unibus signal BUS INIT L is asserted for a short time by the processor after system power has come up, or in response to a reset instruction. The assertion of BUS INIT L results in clearing (DATAO) bits 0, 2, and 15 in the CSR. This prevents the M7850 from immediately signaling a parity error (BUS PBL disabled) before the first DATI data transfer. The generation of ODD (write) parity during the first DATO data transfer is also ensured.

3.3 PARITY GENERATION/CHECKING DEVICES

When a Unibus master writes (DATO/DATOB) into memory, the M7850 generates parity; when the Unibus master reads (DATI/DATIP) from memory, the M7850 checks parity. Figure 3-2 presents the circuitry used to generate parity (DATO/DATOB) and check parity (DATI/DATIP). The major components of the circuitry are the data receivers, the parity gen/check devices (E13, E4), the multiplexer (E14), and the internal bus drivers (E10). The following applies to both parity generation and parity checking.

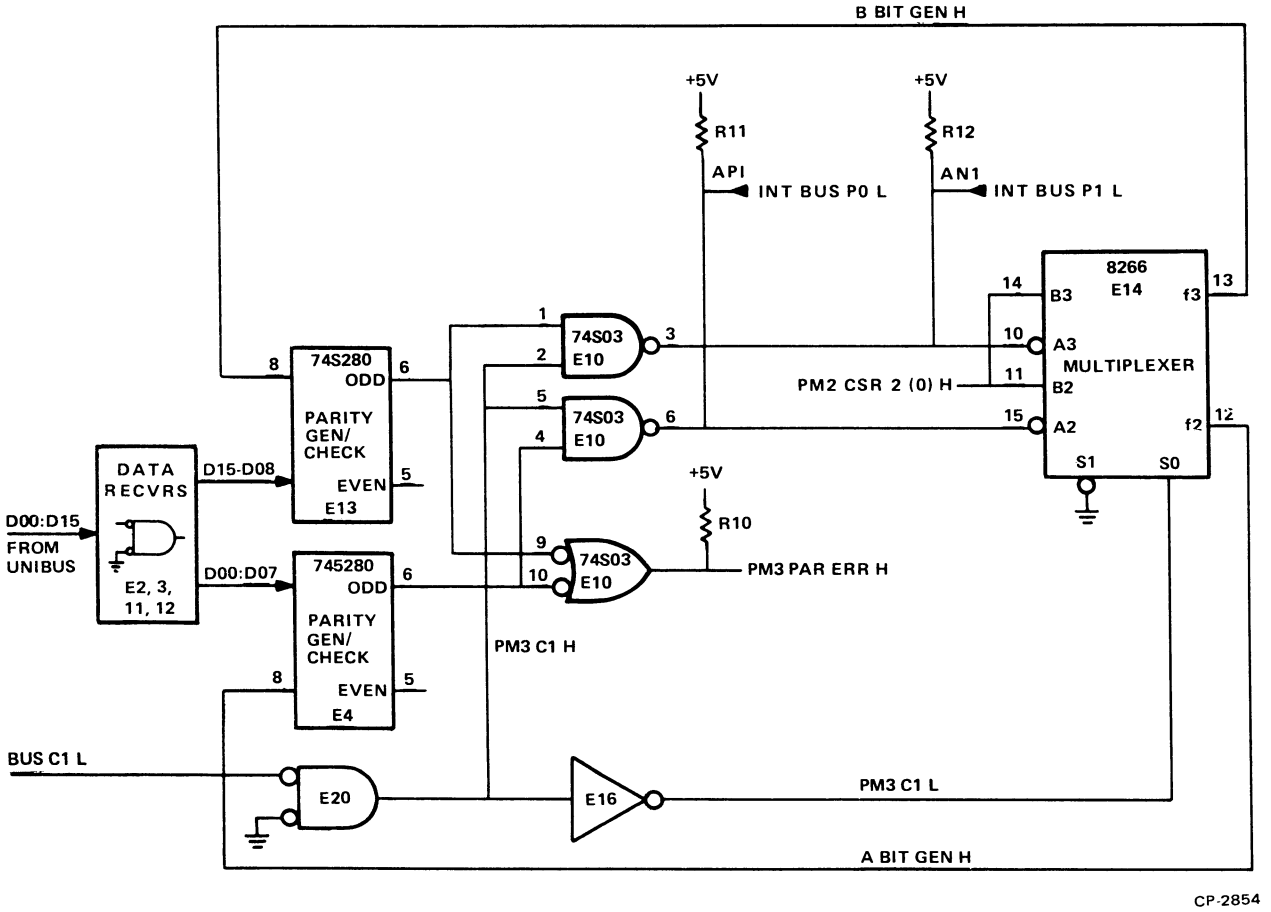


Figure 3-2 Parity Generation and Check Circuit

Data from the Unibus (D15–D00) is applied to the parity gen/check devices (E13, E14) via data receivers (E2, E3, E11, E12). Byte 0 (D07–D00) of the data word is applied to device E4, which is associated with parity bit P0, and data byte 1 (D15–D08) is applied to device E13, which is associated with P1. The ninth data input of each parity generator (A BIT GEN H, B BIT GEN H) is provided by the multiplexer (E14) for control purposes.

The parity gen/check output is determined by the number of DATA1s (signal high) present in the 9-bit input. Refer to the function table.

Function Table for Parity Gen/Check Devices

No. of DATA1 Inputs	Even Output (pin 5)	Odd Output (pin 6)
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = signal high
L = signal low

The ODD output is used in the M7850. Additional information on the parity gen/check devices is contained in Paragraph A.6.

3.3.1 Parity Generation

When a Unibus master writes data (DATO/DATOB) into memory, the M7850 generates parity bits based on the Unibus data. The parity bits are then stored with the corresponding data in memory. (Refer to Figure 3-2.)

The Unibus data (D15–D00) being presented to the memory modules is also applied to the parity gen/check devices as explained in Paragraph 3.3. The state of bit 2 in the CSR determines the type of parity generation (write-wrong) by the M7850 during a DATO/DATOB data transfer. The inverted state of bit 2 in the CSR [PM2 CSR 2 (0)H] is fed to the "B" inputs of multiplexer E14. The assertion of BUS C1 L (indicating DATO/DATOB) causes the mux to present its "B" inputs to both parity gen/check devices. When bit 2 of the CSR is cleared (DATA0), both signals A BIT GEN H and B BIT GEN H are asserted, causing both parity gen/check devices to yield ODD (the correct) parity. A parity bit (P0, P1) is either set (DATA1) or cleared (DATA0) so that the total number of DATA1s become ODD once the parity bit is added to its data byte in memory. When bit 2 of the CSR is set (DATA1), both parity gen/check devices yield even (wrong) parity. These parity bits (P0, P1) are inverted with respect to the parity bits produced by ODD parity generation.

The assertion of BUS C1 L (indicating DATO/DATOB) enables the internal bus drivers (E10) to place the parity bits (P0, P1) on the internal bus. The internal bus signals (P0L, P1L) when asserted represent a DATA1 parity bit.

3.3.2 Parity Checking

When the Unibus master reads data (DATI/DATIP) from memory, the data and the stored parity bits are presented to the M7850. The parity of the data from memory is recalculated and compared to the stored parity bits (P0, P1) to see if a parity error has occurred. (Refer to Figure 3-2.)

The data from memory which is on the Unibus (D15–D00) is presented to the parity gen/check devices via the data receivers as explained in Paragraph 3.3. Each parity bit (P0, P1) is fed to an A input of the multiplexer (E14) from memory via the internal bus. Unibus signal BUS C1 L is not asserted (DATI/DATIP), which causes the mux (E14) to present each A input to its respective parity gen/check device (P0→A BIT GEN H, P1→B BIT GEN H). The mux inverts its A inputs; therefore, a DATA1 parity bit corresponds to a DATA1 bit from the Unibus which is inverted by the data receivers.

If the parity bits (P0, P1) presented to the M7850 are both correct, the number of DATA1s at the input of each parity gen/check device is ODD. Therefore, the ODD outputs of both parity gen/check devices are HIGH which results in the parity error signal (PAR ERR H) *not* being asserted.

If *one* or *both* of the parity bits (P0, P1) is *not* correct, the output of the corresponding parity gen/check device is low. This results in the assertion of signal PAR ERR H by device E10.

Since BUS C1 L is *not* asserted (DATI/DATIP) the internal bus drivers are disabled and cannot place the output of a parity gen/check device on the internal bus.

3.4 PARITY SAMPLE AND STORE

Once the parity of data retrieved from memory is checked for a parity error, the parity error signal (PAR ERR H) is sampled and stored. If a parity error has occurred (PAR ERR H asserted) the M7850 takes appropriate action. Otherwise, only BUS SSYN is asserted by the M7850. Figure 3-3 presents the circuitry which accomplishes the preceding in the following manner.

Once the appropriate memory module has placed data on the Unibus in a DATI/DATIP data transfer the memory asserts INT SSYN. The assertion of INT SSYN triggers a one-shot (E8) in the M7850. Once triggered, the one-shot output (E8 pin 4) stays low for approximately 110 ns (determined by R5 and R16), and then goes high. The one-shot provides the clock pulse for the PAR ERR and SSYN INHIBIT flip-flops (E15). Both flip-flops sample the parity error signal (PAR ERR H) on the rising edge of the one-shot output. Therefore, the parity error signal (PAR ERR H) is sampled approximately 110 ns after the assertion of INT SSYN, which gives the parity gen/check circuitry enough time to yield a valid parity error signal.

During a DATO data transfer, BUS C1 L is asserted which causes the assertion of PM3 C1 L. The one-shot (E8) is disabled by the assertion of PM3 C1 L. Therefore, the parity error signal (PAR ERR H) is not sampled during a DATO.

3.4.1 Parity Error Action Caused by Sample and Store

At sampling time, the PAR ERR FLOP (E15) is set (DATA1) if a parity error has occurred (PAR ERR H asserted). Once it is set, the PAR ERR flip-flop initiates four parity error steps that are carried out in the following manner. Refer to the timing diagram in Figure 3-4.

1. The signal PAR ERR (1) L is asserted (E15 pin 6), which presets flip-flop E7 (bit 15) of the CSR to a DATA1. Flip-flop E7 in turn causes the LED on the back of the M7850 circuit board to turn ON.

2. The assertion of PAR ERR (1) L (E15 pin 6) also causes gate E24 of the CSR control circuitry to assert CLK ADRS H. The assertion of CLK ADRS H clocks address bits A17–A11 from the Unibus into bits 11–15 in the CSR. These stored address bits from the Unibus represent the partial address to within 1K of the faulty data which caused the parity error. Since a data location cannot be in the upper regions of memory (address 77XXXX), the CSR address decode logic did not assert SEL DAT L. Therefore, the multiplexers (E5, E22) presented address information to the CSR inputs (bits 5–11). Refer to Figure 3-1 for CSR information.

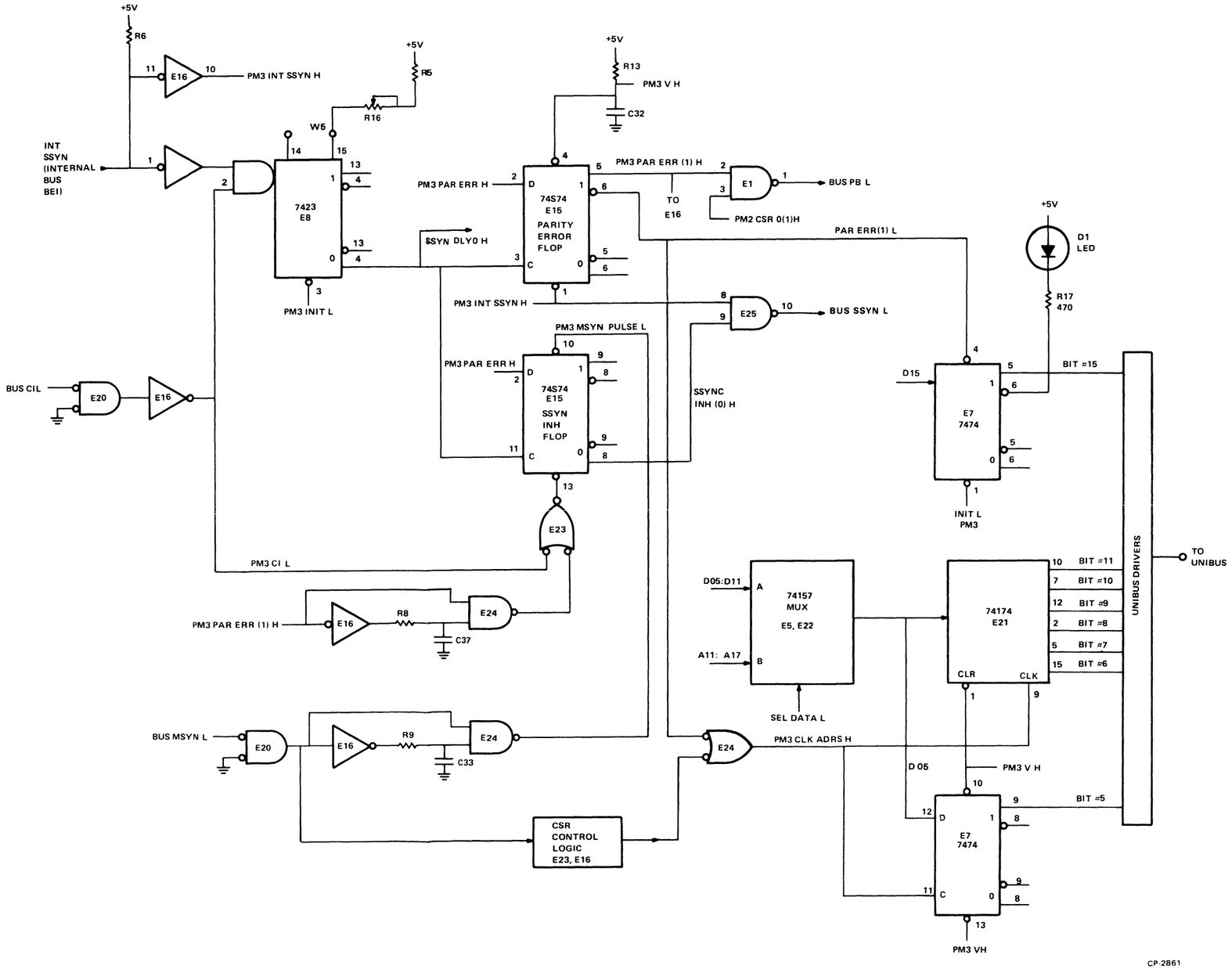


Figure 3-3 Sample Parity and BUS SSYN Control Circuitry

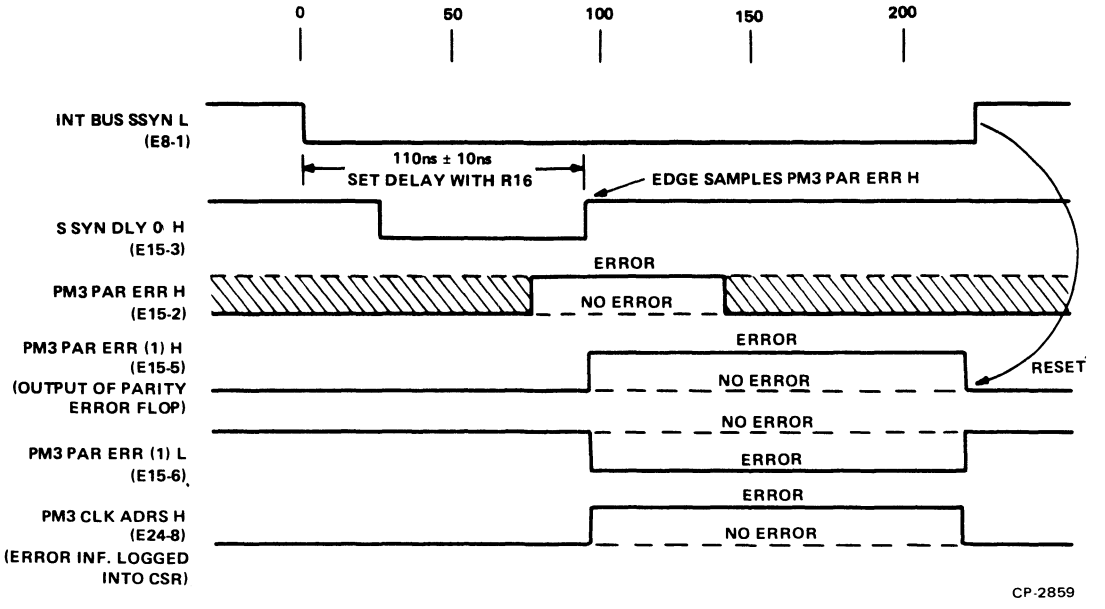


Figure 3-4 Timing Diagram of CSR Error Logging

3. The signal PAR ERR (1) H is asserted (E15 pin 5) which results in the assertion of BUS PB L by gate E25 if bit 0 of the CSR is set [CSRO (1) H asserted].

4. The assertion of PAR ERR (1) H (E15 pin 5) also causes the M7850 to delay the assertion of BUS SSYN by an extra 25 ns. This extra delay yields enough time for the M7850 to execute the parity error actions described in steps 1, 2, and 3. Refer to Paragraph 3.4.2 for a discussion of BUS SSYN assertion by the M7850.

3.4.2 BUS SSYN Control

The M7850 parity controller is activated when a memory module is accessed for retrieval (DATI) or storage (DATO) of data. Once the memory module and the parity controller have finished their part of a data transfer, gate E25 (pin 10) in the M7850 asserts BUS SSYN. (Refer to Figure 3-3.)

The assertion of BUS SSYN (E25 pin 10) is controlled by the INT SSYN signal via an inverter (E16) and the state of the Slave Sync Inhibit flip-flop (E15). Refer to the timing diagram in Figure 3-5.

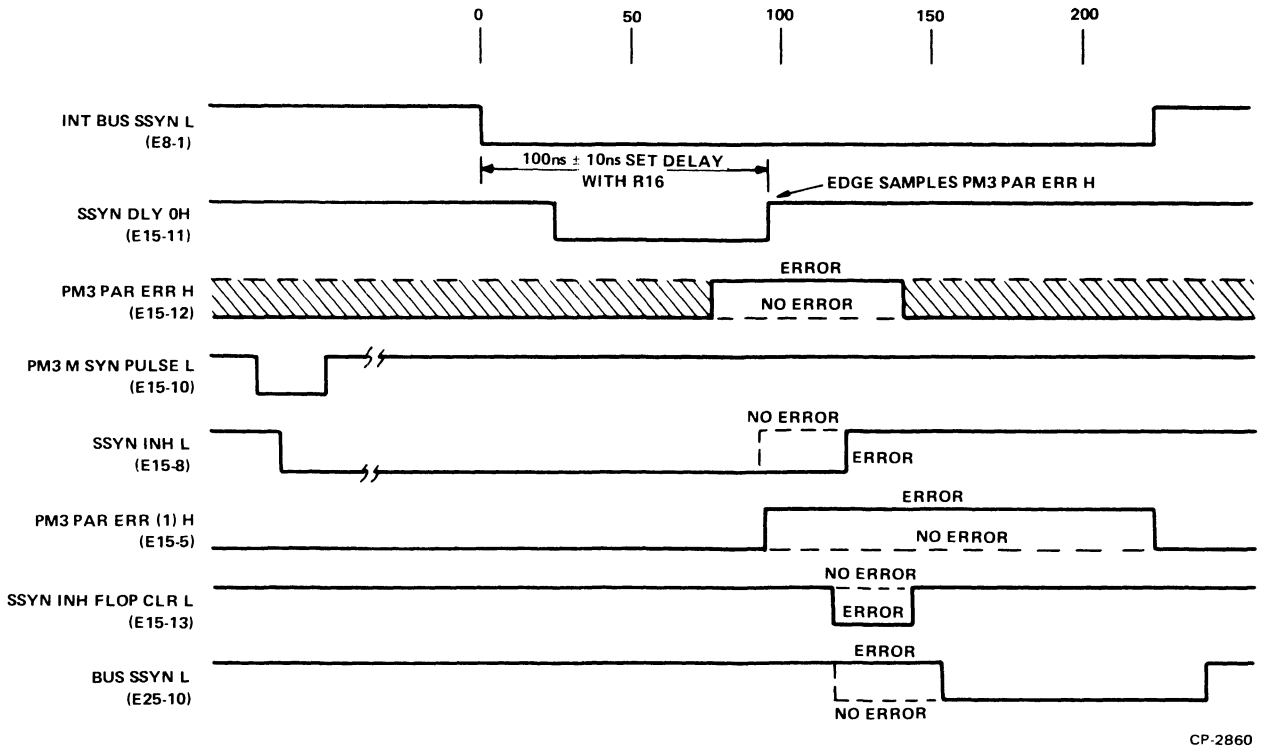


Figure 3-5 Timing Diagram of BUS SSYN Control

When BUS MSYN is asserted, its falling edge is used (by E20, E16, E24) to generate a low-going pulse 25–30 ns wide. This pulse is then used to preset the SSYN IN H FLOP. The pulse width (25–30 ns) is determined by R9 and C33. Once the inhibit flip-flop is preset, the signal SSYN INH (0) H (E15 pin 8) is *not* asserted which prevents BUS SSYN from being asserted. The SSYN INH FLOP is then cleared at different times, depending on the type of data transfer (DATO or DATI), and whether a parity error has occurred during a DATI.

1. When a parity error occurs during a DATI data transfer, both the PAR ERR FLOP and the SSYN INH FLOP are set (DATA1) approximately 110 ns after assertion of INT SSYN. Since the SSYN INH FLOP is already set, the assertion of BUS SSYN is delayed until the flip-flop can be cleared in another fashion. Once set, the PAR ERR FLOP asserts PAR ERR (1) H, which is used (by E16, E24) to create a pulse 25–30 ns wide. The trailing edge of this pulse is then used to clear the SSYN INH FLOP (E15 pin 13). Signal SSYN INH (0) H is asserted and since INT SSYN is still asserted, gate E25 asserts BUS SSYN. Therefore, BUS SSYN is asserted approximately 160 ns after INT SSYN is first asserted by memory.

2. When *no* parity error occurs in a DATI data transfer, both the PAR ERR FLOP and the SSYN INH FLOP are cleared (DATA0) approximately 130 ns after the assertion of INT SSYN. Signal SSYN INH (0) H is asserted, and since INT SSYN is still asserted, gate E25 asserts BUS SSYN. Therefore, BUS SSYN is asserted approximately 130 ns after INT SSYN is first asserted by memory.

3. In a DATO transfer, BUS C1 L is asserted, which clears the SSYN IN H FLOP (E15 pin 13) via E20, E16, and E23. Therefore, signal SSYN INH (0) H is always asserted so BUS SSYN is asserted by E25 as soon as INT SSYN is asserted by memory.

CHAPTER 4
INSTALLATION AND TROUBLESHOOTING

4.1 INSTALLATION

After unpacking the M7850 parity controller, perform the following procedures.

4.1.1 Locate CSR Address

Select a unique address for the CSR in each M7850 by cutting jumpers W1–W4 in accordance with Table 4-1.

The address of the CSR in each M7850 is hardwired within the range 772100–772136. Within this range, the exact CSR address is selected with jumpers W1–W4 which determine bits A1–A4, respectively, of the CSR address. Removing a jumper selects a 1 for an address bit. Jumper locations are shown in Figure 1-3. The CSR is discussed in Paragraph 2.5.

Table 4-1 CSR Address Selection

Machine Address (Words) B	W4 A4	W3 A3	W2 A2	W1 A1
772100	IN	IN	IN	IN
772102	IN	IN	IN	OUT
772104	IN	IN	OUT	IN
772106	IN	IN	OUT	OUT
772110	IN	OUT	IN	IN
772112	IN	OUT	IN	OUT
772114	IN	OUT	OUT	IN
772116	IN	OUT	OUT	OUT
772120	OUT	IN	IN	IN
772122	OUT	IN	IN	OUT
772124	OUT	IN	OUT	IN
772126	OUT	IN	OUT	OUT
772130	OUT	OUT	IN	IN
772132	OUT	OUT	IN	OUT
772134	OUT	OUT	OUT	IN
772136	OUT	OUT	OUT	OUT

4.1.2 Placement of M7850 in Backplane

Ensure that power to the backplane is OFF. Install the M7850 module in connectors A and B of any modified Unibus slot in the backplane (slots 2–8 for DD11-D, slot 2 or 3 for DD11-C). Refer to Figure 4-1.

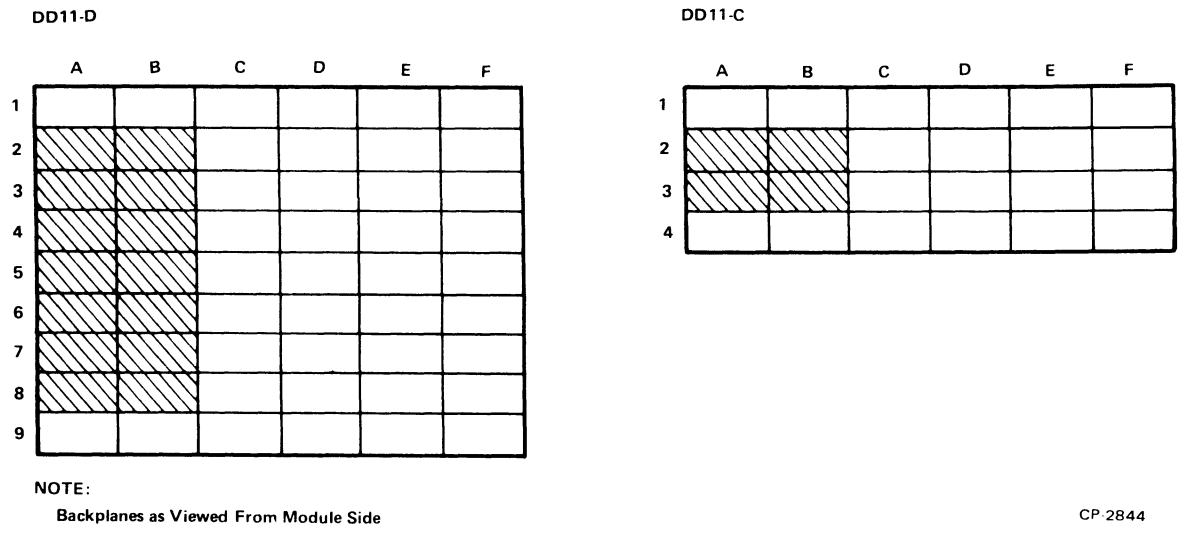


Figure 4-1 M7850 Backplane Placement

One M7850 parity module is necessary in each backplane which contains parity memory module(s) (core and/or MOS). One M7850 generates and checks parity for all parity memory modules in its backplane. A further discussion is presented in Paragraph 1.4.

4.1.3 SSYN DLY (0) H Timing Adjust

Once the M7850 and associated parity memory modules are in the backplane, adjust the timing of SSYN DLY (0) H in the M7850 in the following manner.

1. Both SSYN DLY (0) H and INT BUS SSYN must be monitored with an oscilloscope. Put one scope probe on backplane pin BE1 (INT BUS SSYN) and the other scope probe on pin BB2 [SSYN DLY (0) H]. Pin BC2 on the backplane is signal ground.

2. Load a branch dot instruction (OP CODE 000777) into an even address within the addressing range of the memories controlled by the M7850.

   A branch dot instruction tells the processor to read the contents of the same address which was just read (address contains branch dot instruction). The processor repeatedly reads the same address, which results in a pulse train on the oscilloscope for both signals.

3. Observe the two waveforms and adjust R16 until a time of 110 ns ± 10 ns is obtained between the falling edge of INT BUS SSYN and the rising edge of SSYN DLY (0) H. (Refer to Figure 4-2.) The physical location of R16 is shown in Figure 1-3.

4. To stop the pulse train on the scope, toggle the HALT switch on the front console.

   The SSYN DLY (0) H timing determines when the parity error signal is sampled. This in turn controls when BUS SSYN is asserted on the Unibus. If the timing is set too early, a false parity error could be detected or true parity errors could be missed. If the timing is set too late, the memory access time is increased; (i.e., BUS SSYN is asserted later on the Unibus).

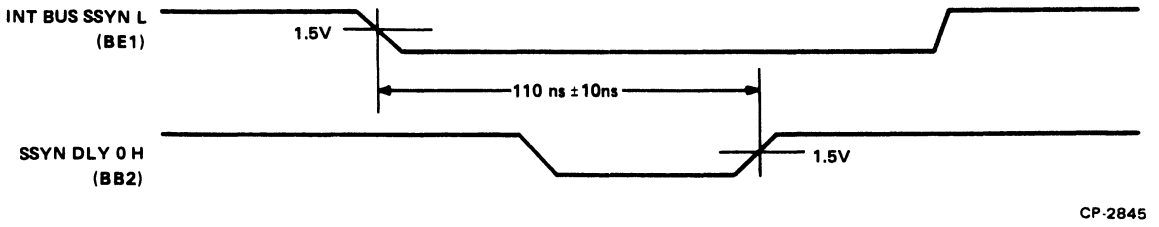


Figure 4-2 Timing Adjust

4.1.4 Diagnostic Program Testing

With known good memories, run diagnostic MAINDEC-11-DCMFA-C-D. This program finds the addresses of all M7850 modules present in the PDP-11 system. The memory locations associated with each M7850 are also found. The M7850 addresses and associated memory locations are printed out, forming a map of the system memory. The parity modules and the associated memory modules presented in the map are then tested. Data is written into and read from all appropriate memory locations. Data is written into memory with both correct (ODD) parity generated, and wrong (incorrect) parity generated. The ODD parity is generated to see that the M7850 does not issue a false parity error when the data is correct. Wrong parity is generated to see that the M7850 *does* issue a parity error when the data is bad.

4.2 M7850 TROUBLESHOOTING

Diagnostic program MAINDEC-11-DCMFA-C-D should be run with known good memories. The operation of this program is discussed briefly in Paragraph 4.1.4.

There are three types of error messages using combinations of the following error type routines:

PC = ZZZZZZ	PC of failing error call. Refer to this address in the listing for an explanation of the error.
ICNT = YYYYYY	Current iteration count of failing test
MPR = XXXXXX	Address of parity CSR register under test
MPR DATA = VVVVVV	Contents of parity CSR register under test
TEST LOC = XXXXXX	Memory location under test
S/B: XXXXXX	Contents of memory location should be
WAS: XXXXXX	Contents of memory location was.

If repeated error reports indicate the same M7850 but different memory modules under its control, the M7850 is probably at fault. The M7850 should be replaced and retested. Refer to Paragraph 4.1 for installation instructions.

4.2.1 M7850 Signal Check

To test M7850 input/output signals, a software SCOPE LOOP program should be placed in a good section of memory. (Use the diagnostic readout to determine a good section of memory.) The SCOPE LOOP programs are listed in Table 4-2. A two-step SCOPE LOOP program continually accesses the memory in a data transfer (DATI or DATO). Address and data information to be used in a SCOPE LOOP program should be taken from the error listing of the diagnostic program. The routine uses CPU registers R4 and R5 to store data and address information.

WARNING

Before testing signals using the SCOPE LOOP routines, disable the ERROR INDICATE BIT (bit 0 of the CSR). This can be done using the DATO SCOPE LOOP routine with the address of the CSR in R5 and data word 000000 in R4.

If this is not done, a repeated parity trap might prevent the generation of a pulse train necessary for a signal check. This data word (000000) also clears the write-wrong parity bit (bit 2 of the CSR) which should result in the generation of correct parity.

Table 4-2 SCOPE LOOP Programs

DATO SCOPE LOOP

	Mnemonic	Op Code	
START	(1) MOV #NUM,SP	012706 NUMBER	
	(2) MOV #DATA,R4	012704 DATA	PROGRAM INITIALIZATION
	(3) MOV #ADRS,R5	012705 ADRS	
LOOP	(4) MOV R4,(R5)	010415	PROGRAM
	(5) BR 376	000776	LOOP

R4(777704) → contains the data to be written into memory.
R5(777705) → contains the memory address to be accessed.

DATI SCOPE LOOP

	Mnemonic	Op Code	
START	(1) MOV#NUM,SP	012706 NUMBER	
	(2) MOV#0,R4	012704 000000	PROGRAM INITIALIZATION
	(3) MOV#ADRS,R5	012705 ADRS	
LOOP	(4) MOV (R5),R4	011504	PROGRAM
	(5) BR 376	000776	LOOP

R4(777704) → contains the data read from memory.
R5(777705) → contains the memory address to be accessed.

Signals should be monitored at the backplane. Signal pins used by the M7850 are presented in Table 4-3. Unibus signal BUS C1 can be used to externally sync the scope. Unibus signal BUS MSYN can be used as a reference to determine when a bus cycle (DATI or DATO) has started. Due to the storage of the SCOPE LOOP routine in memory, three bus cycles are required to implement a LOOP once (to FETCH MOV, EXECUTE MOV, FETCH BR). Only the EXECUTE MOV bus cycle (one out of three) transfers the programmed data which should result in the expected parity bits. In the DATO SCOPE LOOP, the transfer of the programmed data is the only DATO bus cycle.

The waveforms associated with the data transfers are presented in Figures 4-3 and 4-4. A DATO and DATI SCOPE LOOP routine should be implemented (DATO first), using the same programmed data and address information for both routines. The appropriate signals should be checked during each routine. If the parity bits are not as expected during a DATO SCOPE LOOP the M7850 is probably bad. If the parity bits are not as expected during a DATI SCOPE LOOP the memory is probably bad. If INT SSYN does not appear and the memory input signals are okay the memory is probably bad.

Using the DATO SCOPE LOOP, the write-wrong parity bit can be set (to wrong parity) by placing data word 000004 in the CSR. To test if BUS INIT is working properly, a RESET instruction (000005) must be issued. Figure 4-5 is a troubleshooting chart which indicates common failures and the probable causes of these failures.

Table 4-3 M7850 Parity Module Pin Out

	Connector A		Connector B	
Pin No.	Side 1	Side 2	Side 1	Side 2
A	BUS INIT L	+5 V	-	+5 V
B	-	-	-	SSYN DLY (0) H
C	BUS D00L	GND	-	GND
D	BUS D02L	BUS D01L	-	-
E	BUS D04L	BUS D03L	INT BUS SSYN L	INT BUS PAR MOD DET L
F	BUS D06L	BUS D05L	-	-
H	BUS D08L	BUS D07L	BUS A01L	-
J	BUS D10L	BUS D09L	BUS A03L	BUS A12L
K	BUS D12L	BUS D11L	BUS A05L	BUS A14L
L	BUS D14L	BUS D13L	BUS A07L	BUS A06L
M	-	BUS D15L	BUS A09L	BUS A08L
N	INT BUS P1L	BUS PBL	BUS A11L	BUS A10L
P	INT BUS P0L	-	BUS A13L	BUS A12L
R	-	-	BUS A15L	BUS A14L
S	-	-	BUS A17L	BUS A16L
T	GND	-	GND	BUS C1L
U	-	-	BUS SSYN L	BUS C0L
V	-	-	BUS MSYN L	-

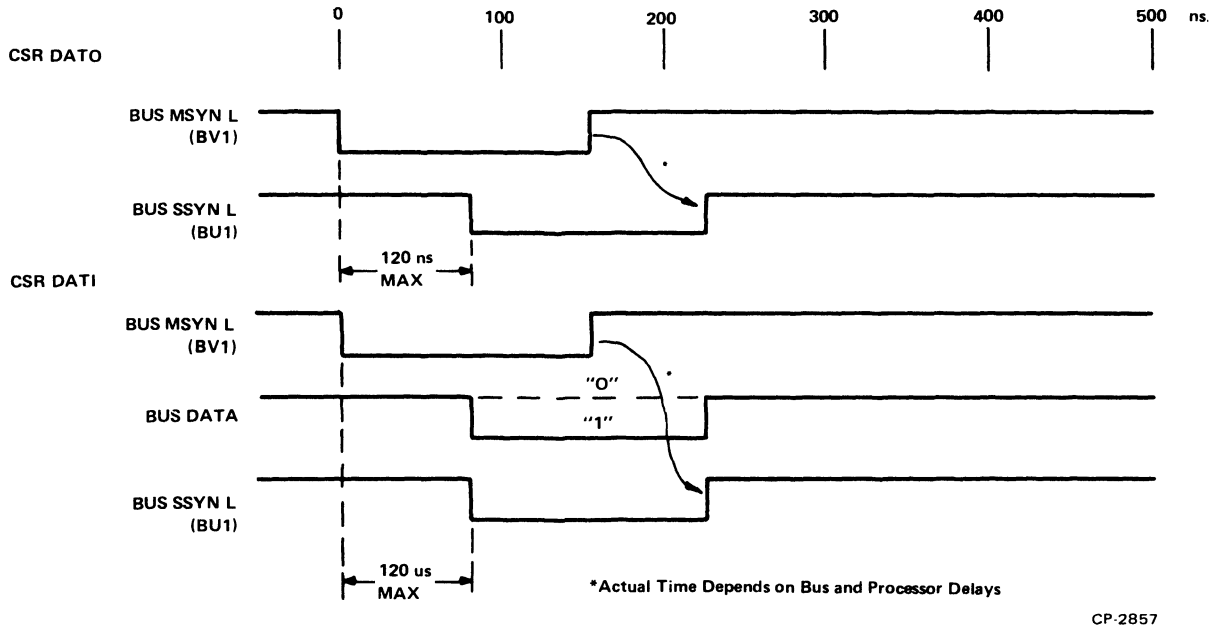


Figure 4-3 Typical Timing Waveforms When Addressing CSR

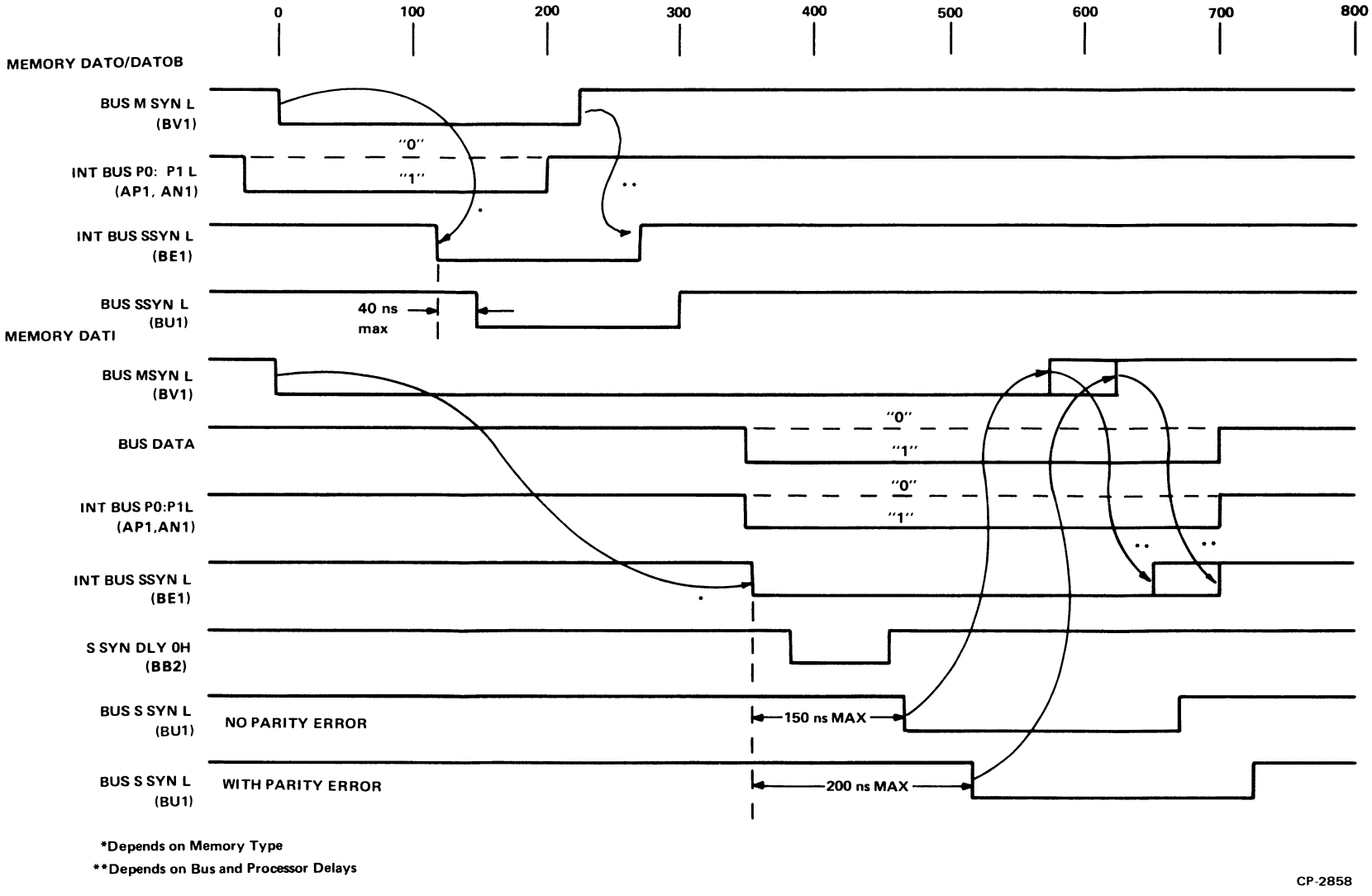


Figure 4-4 Typical Timing Waveforms When Addressing Memory

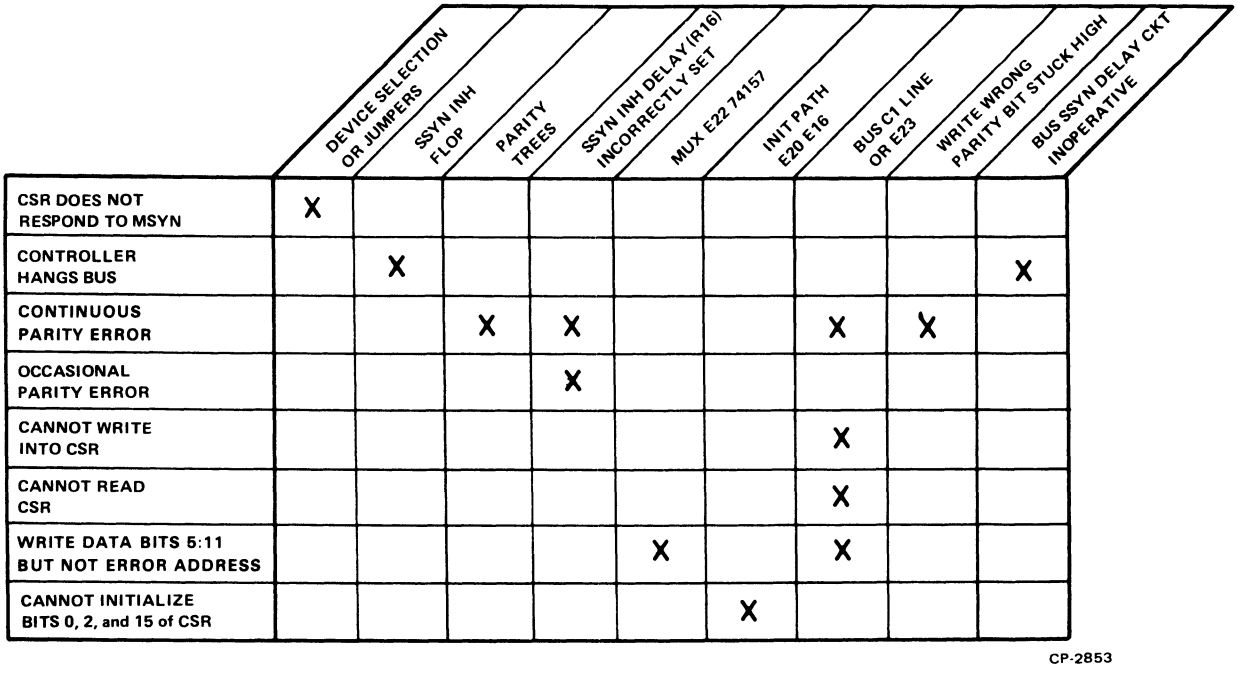


Figure 4-5 Troubleshooting Chart

APPENDIX A
INTEGRATED CIRCUIT DESCRIPTIONS

A.1 INTRODUCTION

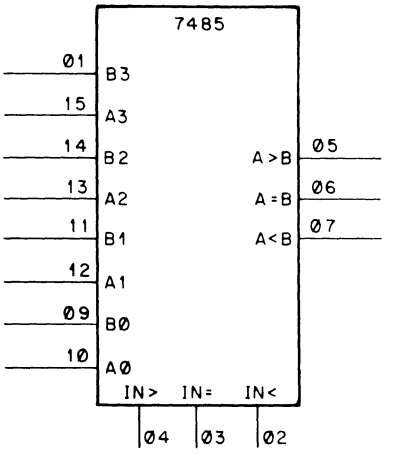
This appendix contains descriptions of the integrated circuits depicted by boxes on the M7850 engineering drawings. Those ICs whose functions are readily apparent from the input and output labels are not included. The ICs described are listed below.

Type	Function
7485	4-Bit Magnitude Comparator
74157	Quad 2 to 1 Line Multiplexer
74174	Hex D Type Flip-Flop
8266	Quad 2 to 1 Line Multiplexer
74S280	9-Bit Parity Generator and Checker

The descriptions include logic diagrams, pin numbers, and truth tables.

7485 4-BIT COMPARATOR

The 7485 performs magnitude comparison of straight binary or straight BCD codes. Three fully decoded decisions (A > B, A < B, A = B) about two 4-bit words (A,B) are made and externally available at three outputs.



VCC = PIN 16
OND = PIN 08

TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	IN >	IN <	IN =	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

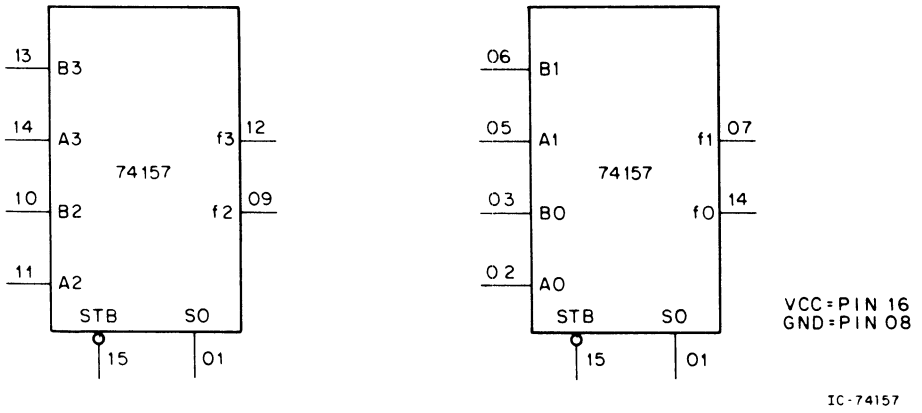
NOTE: H = high level, L = low level, X = irrelevant

IC-7485

74157 QUAD 2 TO 1 MULTIPLEXER

INPUTS				OUTPUT
STB	S0	A	B	f
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant.

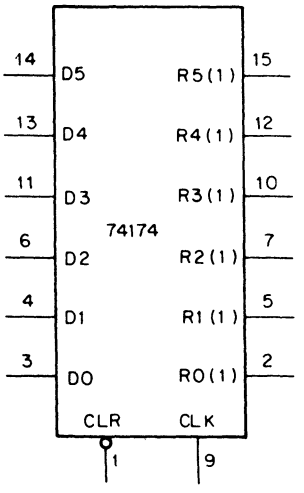


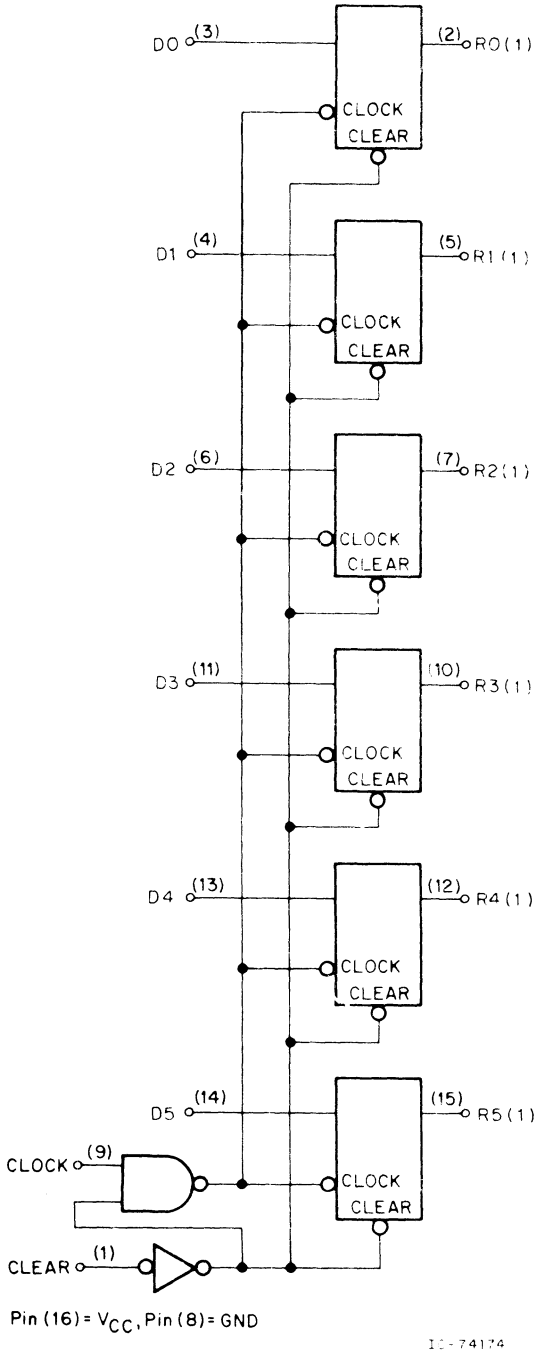
74174 HEX D FLIP-FLOP REGISTER

TRUTH TABLE

INPUT t_n D	OUTPUT t_{n+1} R(1)
H	H
L	L

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.





Pin (16) = V_{CC}, Pin (8) = GND

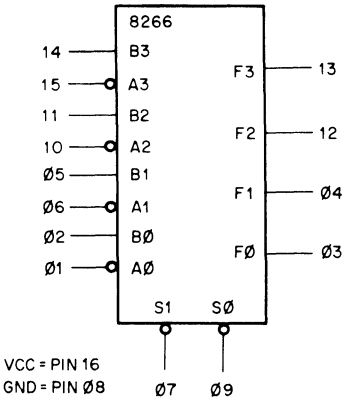
IC-74174

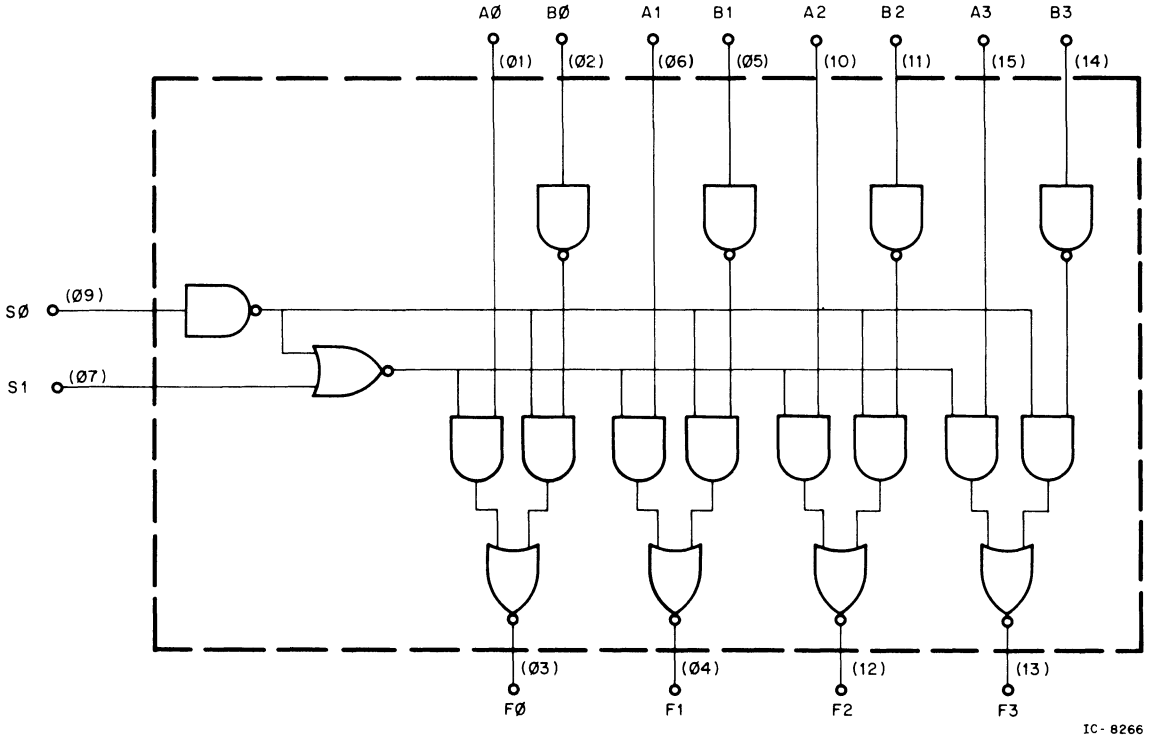
8266 2-INPUT, 4-BIT DIGITAL MULTIPLEXER

The multiplxer is able to choose from two different input sources, each containing 4 bits: A = (A0, A1, A2, A3), B = (B0, B1, B2 B3). The selection is controlled by the input S0, while the seccond control input, S1, is held at zero.

TRUTH TABLE

SELECT LINES		OUTPUTS
SØ	S1	F_n(0, 1, 2, 3)
0	0	B_n
0	1	B_n
1	0	$\bar{A}_n$
1	1	1





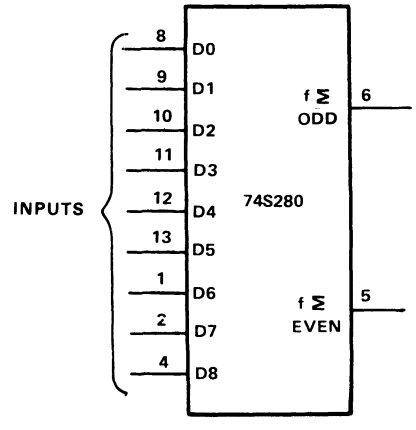
TYPE 74S280 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

This IC gives a high logic level on the ODD output and a low logic level on the even output when there are an odd number of "1s" or high levels on the nine input pins. The converse is true for an even number of "1s" on the nine input pins.

Function Table

Number of Inputs (A–1) That are High	Even	Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = High Level
L = Low Level



M7850 PARITY CONTROLLER
MAINTENANCE MANUAL
EK-M7850-MM-001

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