KT11-D
memory management
option manual

pdp11

digital

DEC-11-HKTDA-B-D

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option manual

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INTRODUCTION

This manual describes the KT11-D Memory Management Unit, which is a hardware option available for use with the PDP-11 Programmed Data Processor. The purpose of this manual is to:

1. Provide an overall understanding of how the KT11-D functions in a PDP-11 system.
2. Explain how the KT11-D hardware can be used in the development of the memory management module of a software operating system.
3. Describe the KT11-D logic in sufficient detail to enable maintenance personnel to perform on-site troubleshooting and repair.

The KT11-D interacts with the KD11-A Central Processor Unit and operating system software to achieve PDP-11 system management objectives. The use of the KJ11 Stack Limit option is also utilized for expanded kernel stacking flexibility. For this reason, a background description of memory management system objectives and programming information is included in this manual.

Chapter 1 introduces the purpose and use of the memory management unit.

Chapter 2 contains operation and programming reference information. It describes the internal registers and their application from a software viewpoint. Programming details, hints, and exceptions of interest to programmers are included.

Chapter 3 provides a block diagram and detailed description of how the logic functions. The content and organization of this chapter is based upon the block schematics contained in the separate Engineering Drawings volume.

Chapter 4 references the installation and maintenance procedures provided in the *PDP-11/40 System Maintenance Manual*. There are KT11-D wiring change procedures provided in this manual.

Detailed descriptions of the processor, console, Unibus, and memory logic that interface with the memory management unit are provided in the following related documents.

PDP-11/40 System Maintenance Manual	DEC-11-H40SA-A-3
KD11-A Processor Manual	DEC-11-HKDAA-A-D
PDP-11 Unibus Interface Manual (2nd Edition)	DEC-11-HIAB-D

CHAPTER 1
GENERAL DESCRIPTION

1.1 PURPOSE AND USE OF KT11-D OPTION

The KT11-D Memory Management Unit is a PDP-11 hardware option that:

a. Expands the basic 32K-word address capability of the KD11-A to 128K words.

b. Provides a "virtual" address space with memory relocation and protection for multi-user timesharing systems.

c. Implements the separate address spaces for the PDP-11 Kernel, and User modes of operation.

d. Provides memory management information for use of memory in multi-user, multi-program systems.

These features are briefly reviewed in the following paragraphs. The essential details required to thoroughly understand the memory management option from the PDP-11 system programmer's viewpoint are presented in Chapter 2, Operation and Programming.

1.1.1 Memory Expansion

The KT11-D option extends the basic PDP-11 physical address capability to 128K words. The 16-bit word length of the KD11 limits the memory address capability of the basic PDP-11 to 32K words. (The least significant address bit is used for byte addressing.) The upper 4K of the address space is always reserved for internal register and external device addresses. Therefore, the total memory address capability is extended from 28K to 124K words.

This is accomplished by converting the 16-bit virtual address generated by the processor to an 18-bit physical address. Several sets of relocation registers are the key to this feature. A complete description of how the active page address registers (PAR) are used to construct the physical address is provided in Paragraph 2.2.2.

1.1.2 Virtual Address Space

Because the KT11-D relocates, if enabled, all addresses automatically, the KD11-A may be considered to be operating in a virtual address space. This means that no matter where a program is loaded into physical memory, it will not have to be "re-linked"; it always appears to be at the same virtual location in memory.

1.1.3 Minimal Memory Fragmentation

The virtual address space is divided into eight separate 4K-word pages. Each page is relocated separately. This is a useful feature in multi-programmed timesharing systems. It permits a new large program to be loaded into discontinuous blocks of physical memory.

In addition, the KT11-D provides a means of allocating a page as small as 32 words, so that short procedures or data areas need occupy only as much memory as required. This is a useful feature in real-time control systems that contain many separate small tasks. It is also a useful feature for stack and buffer control.

1.1.4 Memory Protection

Each virtual page has a separate protection key associated with it. There are three possible basic protection levels. These are listed, in order of increasing protection, as follows:

1. All read or write accesses allowed.
2. Only read accesses allowed.
3. No access allowed.

Any attempt to violate any of these forms of protection is prevented by the KT11-D hardware. For example, an illegal "read" attempt (attempting to read from a page that is protection keyed for no access) does not result in obtaining the contents of the location. An illegal "write" attempt does not result in the modification of the contents of the location. All such illegal access attempts cause an immediate trap (called an "abort") to the Kernel space.

The KT11-D hardware records and preserves abort status information so that the offending user can be notified of the violation. It is not generally possible to recover from these aborts.

1.1.5 Operating Mode Control

In a multi-programmed, timeshared system, user programs must be prevented from modifying or destroying the operating system and each other. The KT11-D implements the Kernel/User modes of PDP-11 operation upon which the timeshared system is based. A page address register/page descriptor register (PAR/PDR) set is provided for each mode of operation. The KT11-D analyzes every memory reference, based on the processor status word, to enable the correct PAR/PDR set. Thus, a User mode program, for example, is prevented from operating in space assigned to Kernel programs.

Compilers, utility programs, and other shared source programs, might be assigned to User mode address space, with access codes keyed to permit read-only access.

1.1.6 Memory Management

In a multi-program, multi-user environment, memory space must be used in the most efficient way, to accommodate as many users as possible with minimum delay. The KT11-D logic maintains a bit which indicates whether the associated page has ever been written into. The software memory management system can interrogate each PDR to determine whether or not that page has been used. If a current active page has been written into, the memory management operating system needs to be informed, so that the modified program can be rewritten into secondary storage before that page is overlayed.

1.2 KT11-D MEMORY MANAGEMENT UNIT SPECIFICATIONS

A summary of specifications and technical characteristics for the KT11-D Memory Management Unit option is listed in Table 1-1.

Table 1-1
Abridged Specifications Summary

Characteristic	Specification or Description
Memory Expansion	Expands PDP-11 memory address capability up to 124K words.
Interface	Address line outputs compatible with PDP-11 Unibus.
Delay	Adds 150 ns to every memory reference.

Table 1-1 (Cont)
Abridged Specifications Summary

Characteristic	Specification or Description
Modes of Operation	Implements the KD11 Central Processor Kernel, and User modes.
Available Pages	Provides eight pages for each mode.
Page Length	A page can vary in length from one 32-word block up to 128 32-word blocks, in 32-word increments. Maximum page length is therefore 4096 words.
Program capacity	Eight 4096-word pages will accommodate a 32K-word program.
Physical description	Option consists of one standard hex module (15 x 8.5 in.) that mounts in PDP-11/40 CPU backplane assembly.
Module M7236	Located in slot 8 rows A through F.
Environmental	Refer to overall PDP-11/40 specifications listed in system manual, DEC-11-H40SA-A-D.

1.3 REFERENCE LITERATURE

The following list of references covers some of the more general aspects of "memory management" tasks of interest to systems programmers. It is part of the recommended bibliography of the National Academy of Engineering for its course outline on "Operating System Principles".

The following abbreviations are used in the bibliography:

ACM	Association for Computing Machinery
IEEE	Institute for Electrical and Electronics Engineers
IEEETC	IEEE Transactions on Computers
CACM	Communications of the ACM
JACM	Journal of the ACM
CS	Computing Surveys (ACM)
FJCC	Fall Joint Computer Conference
SJCC	Spring Joint Computer Conference
2SOSP	Second Symposium on Operating Systems Principles (proceedings available from ACM, 1133 Avenue of the Americas, New York, N.Y. 10036.

Abate, J., and Dubner, H. *Optimizing the Performance of a Drum-Like Storage.* IEEE Trans. C-18, 11 (Nov. 1969), 992-997.

Belady, L.A. *A Study of Replacement Algorithms for Virtual Storage Computers.* IBM Sys. J. 5, 2 (1966), 78-101.

Bensoussan, A., Clingen, C.T., and Daley, R.C. *The Multics Virtual Memory.* Proc. 2SOSP (Oct. 1969).

Denning, P.J. *The Working Set Model for Program Behavior.* Comm. ACM 11, 5 (May 1968), 323-333.

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Dennis, J.B. *Segmentation and the Design of Multiprogrammed Computer Systems.* JACM 12, 4 (Oct. 1965), 589-602.

Kilburn, T. et al. *One-Level Storage System.* IRE Trans. EC-11, 2 (Apr. 1962), 223-235.

Knuth, D.E. *The Art of Computer Programming (Vol. 1).* Addison-Wesley (1969), Ch.2.

Mattson, R.L., Gecsei, J., Slutz, D.R., and Traiger, I.L. *Evaluation Techniques for Storage Hierarchies.* IBM Sys. J. 9, 2 (1970), 78-117.

Randell, B., and Keuhner, C.J. *Dynamic Storage Allocation Systems.* Comm. ACM11, 5 (May 1968), 297-305.

Sayre, D. *Is Automatic Folding of Programs Efficient Enough to Displace Manual?* CACM 12, 12 (Dec. 1969), 656-660.

Wilkes, M.V. *Slave Memories and Dynamic Storage Allocation.* IEEE Trans. EC-14 (Apr. 1965), 270-271.

Wilkes, M.V. *Time-Sharing Computer Systems.* Am. Elsevier (1969).

CHAPTER 2
OPERATION AND PROGRAMMING

2.1 MEMORY MANAGEMENT SYSTEM INTRODUCTION

The purpose of this chapter is to describe the capabilities and objectives of the PDP-11 memory management system. The operating characteristics of the KT11-D Memory Management Unit, which performs the hardware functions in the paging system, are described from the system programmer's viewpoint. Although it may not be necessary to understand the overall system in order to maintain the KT11-D hardware, much of the information presented in this chapter is relevant to the detailed logic descriptions in Chapter 3.

Suggested techniques that are included in this chapter are presented only for the purpose of illustrating hardware operating characteristics and as examples of how system programmers can use the KT11-D in developing an operating system. This information is also presented to provide a better understanding of the hardware for maintenance purposes.

NOTE
The information in this chapter does not describe the DEC Operating System for the PDP-11.

In the following paragraphs, the general features of the KT11-D Memory Management Unit are introduced, beginning with the basic memory relocation and extended memory addressing capability. Next, some of the general requirements of a memory management system are described, along with illustrations of how the KT11-D hardware can be used to implement such a system. Following that, the overall memory protection requirements and corresponding facilities provided by the KT11-D are described.

The system programmer has the option of using any or all of the KT11-D memory management capabilities, depending upon whether simple relocation into extended memory is required or complex dynamic memory allocation systems are required.

2.2 MEMORY RELOCATION

A basic KT11-D function is to perform memory relocation and provide extended memory addressing capability for systems with more than 28K of physical memory. The KT11-D uses two sets of page address registers to relocate virtual addresses to physical addresses in memory. These sets are used as hardware relocation registers that permit several user's programs, each starting at virtual address 0, to simultaneously reside in physical memory.

2.2.1 Program Relocation

The page address registers are used to determine the starting address of each relocated program in physical memory. Figure 2-1 shows a simplified example of the relocation concept. A more detailed example of how memory relocation works is shown in Figure 2-3.

In Figure 2-1, Program A starting address 0 is relocated by a constant to provide physical address 6400_8.

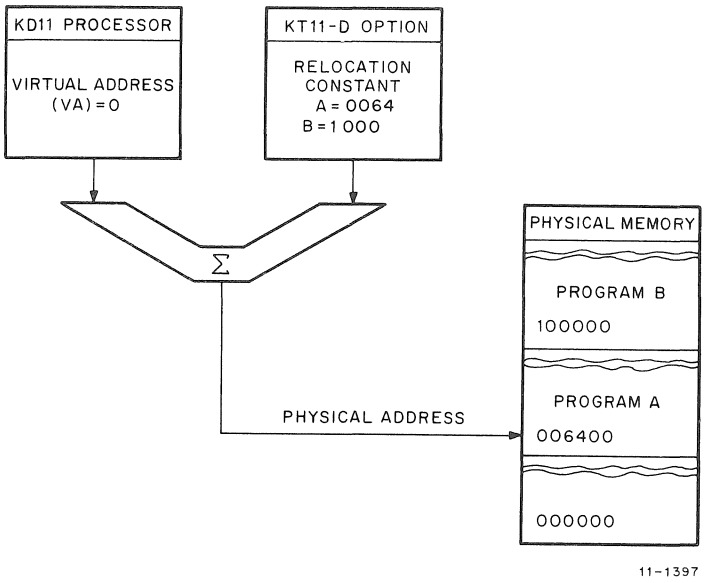


Figure 2-1 Simplified Memory Relocation Example

If the next processor virtual address is 2, the relocation constant will then cause physical address 6402_8, which is the second item of Program A, to be accessed. When Program B is running, the relocation constant is changed to 100000_8. Then, Program B virtual addresses starting at 0, are relocated to access physical addresses starting at 100000_8. Using the active page address registers to provide relocation eliminates the need to "re-link" a program each time it is loaded into a different physical memory location. The program always appears to start at the same address.

In the PDP-11 systems, a program is relocated in pages. A page can consist of from 1 to 128 blocks. Each block is 32 words in length. Thus, the maximum length of a page is 4096 (128 x 32) words. Using all of the eight available active page registers in a set, a maximum program length of 32,768 words can be accommodated. Each of the eight pages can be relocated anywhere in the physical memory, as long as each relocated page begins on a boundary that is a multiple of 32 words. However, for pages that are smaller than 4K words, only the memory actually allocated to the page may be accessed.

The relocation example shown in Figure 2-2 illustrates several points about memory relocation. These points are:

1. Although the program appears to be in contiguous address space to the processor, the 32K-word virtual address space is actually scattered through several separate areas of physical memory. As long as the total available physical memory space is adequate, a program can be loaded. The physical memory space need not be contiguous.

2. Pages may be relocated to higher or lower physical addresses, with respect to their virtual address ranges. In the example of Figure 2-2, page 1 is relocated to a higher range of physical addresses, page 4 is relocated to a lower range, and page 3 is not relocated at all (even though its relocation constant is non-zero).

3. All of the pages shown in the example start on 32-word boundaries.

4. Each page is relocated independently. There is no reason why two or more pages could not be relocated to the same physical memory space. Using more than one page address register in the set to access the same space would be one way of providing different memory access rights to the same data, depending upon which part of a program was referencing that data. Further information about memory protection is provided in Paragraph 2.4. In the example shown in Figure 2-2, note the relocation constant assigned to pages 4 and 6. As a result, virtual addresses within both address ranges access the same physical addresses in memory, using separate page address registers.

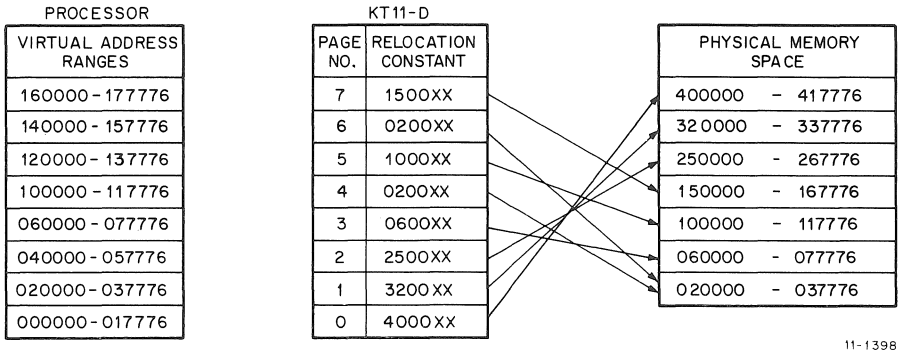


Figure 2-2 Relocation of a 32K Word Program
Into 124K Word Physical Memory

NOTE
Where xx is the address within the block number given by the PAR

2.2.2 Extended Memory Addressing

When the KT11-D Memory Management Unit option is added to the PDP-11 system, the 16-bit KD11 address output is no longer interpreted as the direct physical address of a device or a memory location. Instead, it is considered as a 16-bit virtual address that contains information to be used by the KT11-D to construct an 18-bit physical address.

Refer to Figure 2-3 which shows how the 18-bit physical address is constructured. Virtual address bits VA (15:13) are interpreted as an active page field (APF) to select one of eight active page registers in a set. Virtual address bits (12:06) provide the block number (0 to 127_{10}) within the page. VA (05:00) indicate the displacement within each 32-word block.

The PAR contains a page address field (PAF) that is written into the PAR under program control at the time the complete PAR/PDR set is defined for a program page. Consider the PAF as the base address of the page. The block number, VA (12:06) is added to the base address PAF (11:00) to provide the 12 most significant bits of the physical address. This, plus virtual address bits VA (05:00) (unchanged by relocation), forms the 18-bit physical address.

2.3 MEMORY MANAGEMENT

The following paragraphs describe some of the memory management tasks that might be required of an operating system. The KT11-D hardware features aid the system software in the performance of these tasks.

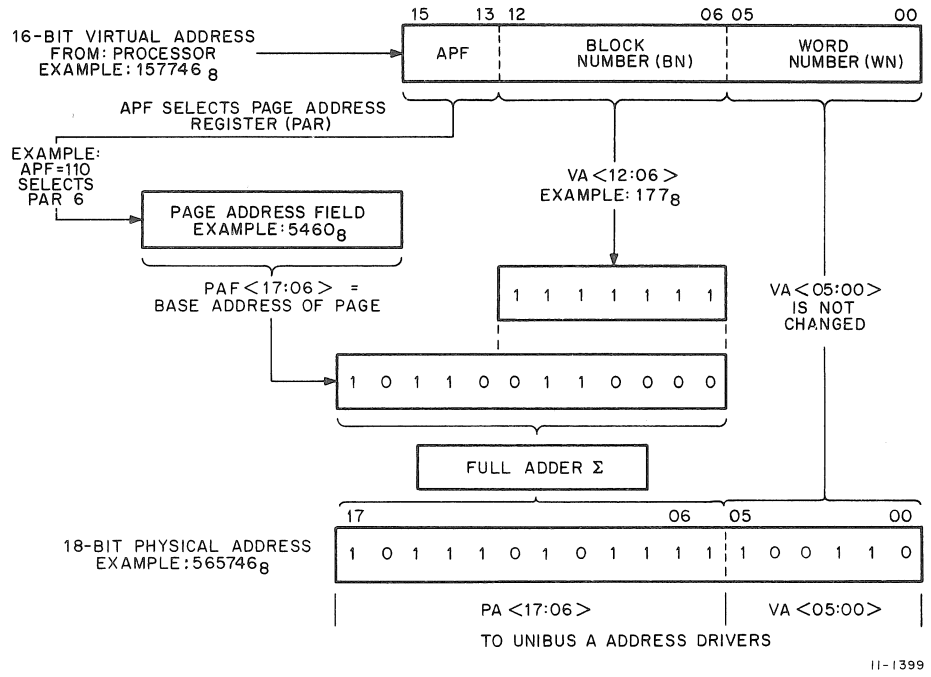


Figure 2-3 Construction of an 18-Bit Physical Address

2.3.1 Program Relocation

A timesharing system which swaps programs between physical memory and some backing store (such as an RF11 disk) can be efficiently implemented, because the programs need not be restricted to run in any particular memory locations.

When it is time to swap a program in, all that is required is that there be sufficient memory available in which to read the program and then set up the KT11-D to "relocate" the program so that it thinks it has been loaded at location 0.

2.3.2 Dynamic Memory Allocations

The KT11-D provides hardware-implemented features that enable the operating system to dynamically allocate memory upon demand, while a program is being run. These features are particularly useful when running higher-level language programs, such as ALGOL and PL/1, where, for example, arrays are constructed at execution time. No fixed space is reserved for them by the compiler. Lacking the dynamic memory allocation capability, the programmer must calculate and allow sufficient memory space to accommodate the worst case. This is time consuming and in many cases memory space is wasted.

Monitor primitives to allocate (de-allocate) memory, either by adding (deleting) a page or by increasing (decreasing) the size of an existing page, may be implemented. A running program can request, and subsequently return, memory used for a temporary buffer and the like, thus efficiently using the physical store and removing the worst case memory size restrictions.

To illustrate how dynamic memory allocation might be used, suppose an assembler initially requests enough memory for 64 symbols, say 256 words. If this symbol table overflows, then the assembler requests an additional 256 words, and so on, until a request is denied, at which time (and only at which time) an actual symbol table overflow has

occurred. This algorithm is clearly more efficient with respect to memory utilization than one which initially grabs a large chunk of memory for symbols.

NOTE

Any use of page lengths less than 4K words causes holes to be left in the virtual address space.

2.3.3 Memory Management Statistics

In a multiprogramming timeshared system, programs tend to be swapped between the main memory and some backing store, such as a disk. Needless to say, the performance of such a system is certainly dependent on the efficiency of the swapping algorithm.

Those portions of memory which have not been modified, (i.e., written into) since the last time they were swapped in, need not be swapped out when the space they occupy is required for something else. Instead, the memory can be used as is, because the copy of it on the backing store is still current. Thus, "half" the swapping time can be saved for those unmodified portions of main memory.

The KT11-D logic provides two mechanisms to help implement efficient swapping:

1. Pages may be designated read only. Such pages cannot be modified.
2. A flag, the "W-bit", is automatically set by hardware whenever a potentially writable page is actually written into.

2.3.4 Memory Management Instructions

Memory Management provides the ability to communicate between two spaces, as determined by the Extended Processor Status Word, PS(15–12). This capability is implemented by the addition of two unique instructions to the KD11-A Instruction repertoire:

MTPI – Move To Previous Space (0066 DD).

MFPI – Move from Previous Space (0065 SS).

These instructions are operational in a KD11-A system, otherwise an Illegal Instruction Trap will result on an attempted execution.

Memory Management does not have to be enabled (SR0 bit 0 set) for interstack communications although relocation and protection will be disabled. If these two instructions are examined from a programmer's point of view, they appear somewhat complex. However, from a hardware viewpoint, it is evident that they are modified MOV instructions.

In investigating the memory management instructions, the following facts must be kept in mind:

1. There are two possible modes of operation:
   a. Kernel (Monitor)
   b. User.

2. The selection of mode is made by expanding and utilizing the Processor Status Word (PSW). The possible machine states specified by PS(15:12) are as follows:

PS(15:12)	Current Mode (CM)	Previous Mode (PM)
00 00	Kernel	Kernel
11 11	User	User
11 00	User	Kernel
00 11	Kernel	User

3. The MFPI and MTPI instructions are most likely to be used in current mode Kernel, previous mode User.

4. The current mode specifies the Page Relocation and Descriptor Register set used to convert the KD11-A virtual address to a KT11-D physical address.

Examining the MFPI instruction, the general instruction format is:

MFPI i.e., OP CODE and a Source address field.
(0065 SS)

When MFPI SS is fetched, the KD11-A will transform and encode it into the following:

MFPI SS → MOV SS, – (SP)

It will send it back to the processor over the RD Bus, reclock it into the IR Register, and execute it in conjunction with Memory Management space selection logic.

The calculation of the Source address is done in current space. That is, any index word or indirect addresses used in the address calculation are fetched using the KT11-D Page Address Registers selected by the current mode bits of the PSW. The final fetch of the Source operand in which data is to be moved *from* is made in previous space, i.e., using the KT11-D Page Address Registers selected by the previous mode bits in the PSW. Note that if the Source field is mode 0 Register 6, the SP selected is made by the previous mode bits of the PSW. But with any other mode and R6, the SP selected is by the current mode bits of PSW; since in these cases, the register is part of the address calculation and is not the final operand. The Source operand is then pushed on the current mode stack.

Examining the MTPI DD instruction, it has the following general format:

MTPI DD i.e., op code and a Destination address field.
(0066 DD)

A similar transformation to a MOV instruction is done to MTPI DD.

MTPI DD → MOV (SP) +, DD

The calculation of the Destination address is done in current space. That is, any index or indirect addresses used in the address calculation are fetched using the KT11-D Page Address Registers selected by the current mode bits of the PSW. The final fetch of the Destination operand in which data is to be stored, is made in previous space. Note that if the Destination field is mode 0 Register 6, the SP selected is made by the previous mode bits of the PSW. But with any other Destination mode and R6, the SP selected is made by the current mode bits of the PSW. Since in these cases, the register is part of the address calculation and is not the final operand, this instruction pops a word off the current stack determined by PS(15:14) and stores that word into a Destination address in previous space determined by PS(13:12).

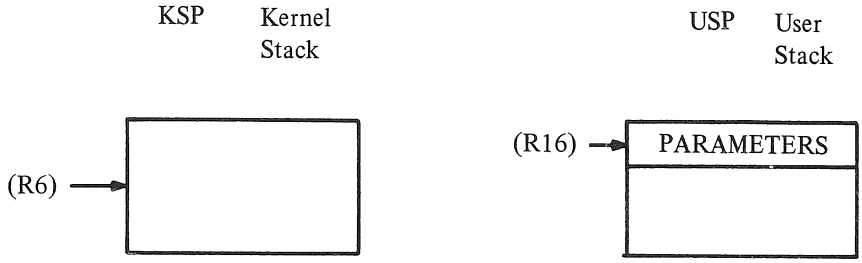
Thus, these instructions are used in memory managed systems to allow the exchange of data between the monitor (Kernel) and a user.

The following is an example of how Memory Management instructions can be used in an operating system. In advanced software systems, a user can not be allowed to handle his own I/O directly. The I/O address space is not available to a user (this is controlled by the contents of the UPAR's, which are set up by the monitor). Users initiate I/O requests to the monitor by means of a trap such as EMT.

Prior to the trap, the user pushes on to his stack (R16) certain parameters such as command, word count, and buffer address. The trap sequence sets up the PS(15:12) such that the current mode is Kernel (monitor) and the previous mode was User.

The Kernel must now retrieve the I/O parameters from the user core space, using the MFPI instruction.

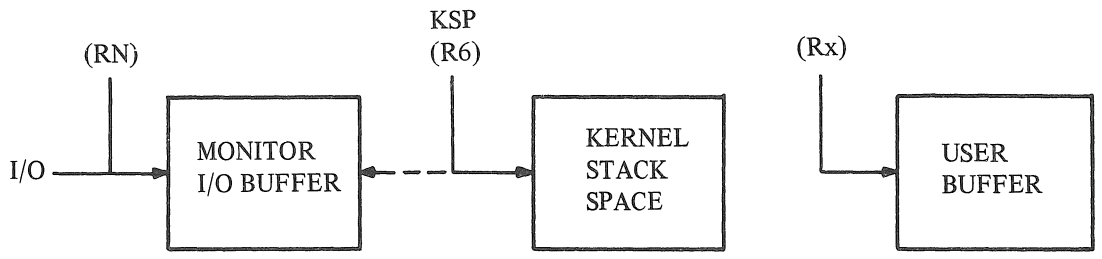
Example 1 – Retrieve parameter from User stack.




```
XX      /MOV #UPCNT, RA              ;STORE NUMBER OF USER
                                     ;PARAMETERS IN A REGISTER.

        /MFPI R6                     ;GET USER STACK POINTER (USP)
        CONVERTS TO MOV R16, - (R6)  ;ONTO THE KERNEL STACK.

        /MOV (R6) +, RN              ;PUT USP IN A REGISTER

LOOP    /MFPI (RN) +                 ;PUT USER PARAMETERS
        CONVERTS TO MOV (RN) +, - (R6) ;ONTO KERNEL STACK.

        /CMP RN, RA + RB             ;HAVE ALL PARAMETERS BEEN
                                     ;TRANSFERRED TO KERNEL.

        /BLT LOOP                    ;IF NOT GET ANOTHER
                                     ;PARAMETER.
```

The monitor can now initiate the required command to the I/O. Although all devices have the capability of accessing all of physical core (meaning the ability to access user core), this practice usually is not preferred because the user is subject to being "swapped out" at any time. Therefore, data is normally placed into a monitor (Kernel) buffer. The monitor must then transfer that data to user core by means of the MTPI instruction.

Example 2 – Transferring data read from a device to user core.




```
XX      /MOV I/O BUFADR, RN              ;POINT RN TO I/O BUFADR.

        /MOV UBUFADR, RX                 ;POINT RX TO USER
                                         ;BUFFER.

LOOP    /MOV (RN) +, - (R6)              ;PUSH I/O DATA ONTO THE
                                         ;KERNEL STACK.

        /MTPI (RX) +                     ;MOV I/O DATA TO USER
        CONVERTS TO MOV (R6) +, (RX) +   ;BUFFER CORE.

        /CMP RN, I/O BUFADR + WORD CNT   ;HAS ALL I/O DATA
                                         ;BEEN TRANSFERRED
                                         ;TO USER CORE

        /BLT LOOP                        ;IF NOT GET ANOTHER
                                         ;DATA WORD.
```

Examples 1 and 2 do not reflect any user software system but are meant mearly as examples of the operation and uses of MFPI and MTPI.

2.4 MEMORY PROTECTION

A timesharing system performs multiprogramming; it allows several programs to reside in memory simultaneously, and to operate sequentially. Access to these programs, and the memory space they occupy, must be strictly defined and controlled. Several types of memory protection must be afforded a timesharing system. For example:

a. User programs must not be allowed to expand beyond allocated space, unless authorized by the system.

b. Users must be prevented from modifying common subroutines and algorithms that are resident for all users.

c. Users must be prevented from gaining control of or modifying the operating system software.

The KT11-D option provides the hardware facilities to implement all of the above types of memory protection. The following paragraphs describe the memory protection features afforded by the KT11-D.

2.4.1 Inaccessible Memory

Each page has a 2-bit access control key associated with it. The key is assigned under program control. When the key is set to 0, the page is defined as non-resident. Any attempt by a user program to access a non-resident page is prevented by an immediate abort. Using this feature to provide memory protection, only those pages associated with the current program are set to legal access keys. The access control keys of all other program pages are set to 0, which prevents illegal memory references.

2.4.2 Read-Only Memory

The access control key for a page can be set to 2, which allows read (fetch) memory references to the page, but immediately aborts any attempt to write into that page. This read-only type of memory protection can be afforded to pages that contain common data, subroutines, or shared algorithms. This type of memory protection allows the access rights to a given information module to be user-dependent. That is, the access right to a given information module may be varied for different users by altering the access control key.

A page address register in each of the sets (Kernel and User modes) may be set up to reference the same physical page in memory and each may be keyed for different access rights. For example, the User access control key might be 2 (read-only access), and the Kernel access control key might be 6 (allowing complete read/write access).

2.4.3 Multiple Address Space

There are two completely separate PAR/PDR sets provided by the KT11-D: one set for Kernel mode and one set for User mode. This affords the timesharing system with another type of memory protection capability. The mode of operation is specified by the Processor Status Word current mode field, or previous mode field, as determined by the current instruction. (MTPI and MFPI are the two instructions that use previous mode.)

Assuming the current mode PSW bits are valid, the active page register sets are enabled as follows:

PS (15:14)	PAR/PDR Set Enabled
00	Kernel mode
01	Illegal (all references aborted on access)
10	
11	User mode

2.4.4 Mode Description

With memory management the modes of operation provide the following flexibility and restrictions:

In Kernel Mode, the operating program has unrestricted use of the machine except for the added time to a bus cycle created by the KT11-D Logic of a 150ns. The User also sees this delay plus the operating restrictions listed below:

1. Attempted execution of the instruction HALT traps as a Reserved Instruction via location 10;
2. Execution of a RESET instruction results in a no-operation execution of a NOP instruction (1.5μsec).

3. User Processor Status restrictions are as follows:

	USER RTI, RTT	USER TRAPS, INTERRUPTS	EXPLICIT PSW ACCESS
CC (3:0)	Loaded from Stack	Loaded from Vector	*
T (4)	Loaded from Stack	Loaded from Vector	Cannot be changed
PRIORITY (7:5)	Cannot be changed	Loaded from Vector	*
PREVIOUS (13:12)	Cannot be changed	Copied from PS (15:14)	*
Current (15:14)	Cannot be changed	Loaded from Vector	*

* = Explicit operations can be made if the Processor Status is mapped in User space.

4. Stack Limit Violations are disabled in User. Stack protection provided by memory protect features. Another difference between the two modes is the use of separate stack pointer registers:

   Kernel – KD11 Register 6 (R6)

   User – KD11 Register 16 (R16)

   On a trap or an interrupt, the vector is always referenced via Kernel space and the old PS and PC are pushed onto the stack determined by the new current mode of the PSW from the vector.

Thus, a User mode program is relocated by its own PAR/PDR set, as are Kernel programs. This makes it impossible for a program running in one mode to accidentally reference space allocated to another mode when the active page registers are set correctly. For example, a user cannot transfer to Kernel space. The Kernel mode address space may be reserved for resident system monitor functions, such as the basic Input/Output Control (IOC) routines, memory management trap handlers, and timesharing scheduling modules. By dividing the types of timesharing system programs functionally between the Kernel and User modes, a minimum amount of space control housekeeping is required as the timeshared operating system sequences from one user program to the next. For example, only the User PAR/PDR set needs to be updated as each new user program is serviced. The two PAR/PDR sets implemented in the KT11-D Memory Management Unit option are shown in Figure 2-4.

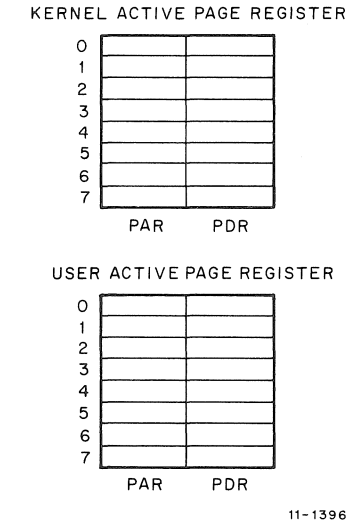


Figure 2-4 KT11-D Memory Management Unit Active Page Registers

2.5 PAR/PDR REGISTERS

The KT11-D Memory Management Unit provides two sets of eight PAR/PDR pairs. Figure 2-4 shows how the two sets are organized. Each pair consists of a Page Address Register (PAR) and a Page Descriptor Register (PDR). These registers are always used as a pair and contain all the information required to locate and describe the current active pages for each mode of operation. As indicated in Figure 2-4, one PAR/PDR set is used in Kernel mode and the other is used in User mode. The current mode bits (or in some cases, the previous mode bits) of the Processor Status Word determine which set will be referenced for each memory access. A program operating in one mode cannot use the PAR/PDR sets of the other mode to access memory. Thus, the two sets are a key feature in providing a full-protected environment for a timeshared multi-programming system.

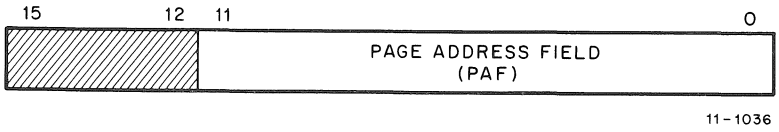


Figure 2-5 Page Address Register (PAR) Format

A specific processor I/O address is assigned to each PAR and PDR of each set. Table 2-1 is a complete list of address assignments.

NOTE
Unibus devices cannot access PARs or PDRs.

In a fully-protected multi-programming environment, the implication is that only a program operating in the Kernel mode would be allowed to write into the PAR and PDR locations for the purpose of mapping user's programs. However, there are no restraints imposed by the KT11-D logic that will prevent User mode programs from writing into these registers. The option of implementing such a feature in the operating system, and thus explicitly protecting these locations from user's programs, is available to the system software designer.

Table 2-1
PAR/PDR Address Assignments

Kernel Active Page Registers			User Active Page Registers		
No.	PAR	PDR	No.	PAR	PDR
0	772340	772300	0	777640	777600
1	772342	772302	1	777642	777602
2	772344	772304	2	777644	777604
3	772346	772306	3	777646	777606
4	772350	772310	4	777650	777610
5	772352	772312	5	777652	777612
6	772354	772314	6	777654	777614
7	772356	772316	7	777656	777616

2.5.1 Page Address Registers (PAR)

The Page Address Register (PAR), shown in Figure 2-5, contains the 12-bit Page Address Field (PAF) that specifies the base address of the page.

Bits (15:12) of the PAR are not implemented in the hardware.

The Page Address Register may be alternatively thought of as a relocation constant, or as a base register containing a base address. Either interpretation indicates the basic function of the Page Address Register (PAR) in the relocation scheme.

2.5.2 Page Descriptor Registers (PDR)

The Page Descriptor Register (PDR), shown in Figure 2-6, contains information relative to page expansion, page length, and access control.

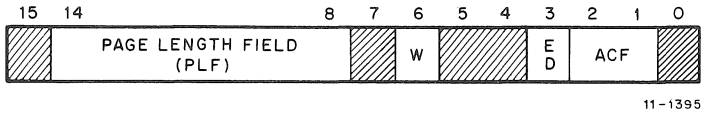


Figure 2-6 Page Descriptor Register (PDR) Format

2.5.2.1 Access Control Field (ACF) – This 2-bit field, ACF (02:01) of the PDR describes the access rights to this particular page. The access codes or "keys" specify the manner in which a page may be accessed and whether or not a given access should result in an abort of the current operation. A memory reference that causes an abort is not completed and is terminated immediately.

Aborts are caused by attempts to access non-resident pages, page length errors, or access violations, such as attempting to write into a read-only page. Traps are used as an aid in gathering memory management information.

In the context of access control, the term "write" is used to indicate the action of any instruction which modifies the contents of any addressable word. A "write" is synonymous with what is usually called a "store" or "modify" in many computer systems. Table 2-2 lists the ACF keys and their functions. The ACF is written into the PDR under program control.

Table 2-2
Access Control Field Keys

ACF	Key	Description	Function
00	0	Non-resident (NR)	Abort any attempt to access this non-resident page.
01	2	Resident read-only (RRO)	Abort any attempt to write into this page.
10	4	Illegal	Abort all accesses.
11	6	Resident read/write (RRW)	Read or Write allowed. No trap or abort occurs.

2.5.2.2 **Expansion Direction (ED)** – The ED bit located in PDR bit position 03 indicates the authorized direction in which the page can expand. A logic 0 in this bit (ED=0) indicates the page can expand upward from relative zero. A logic 1 in this bit (ED=1) indicates the page can expand downward toward relative zero. The ED bit is written into the PDR under program control. When the expansion direction is upward (ED=0), the page length is increased by adding blocks with higher relative addresses. Upward expansion is usually specified for program or data pages to add more program or table space. An example of page expansion upward is shown in Figure 2-7.

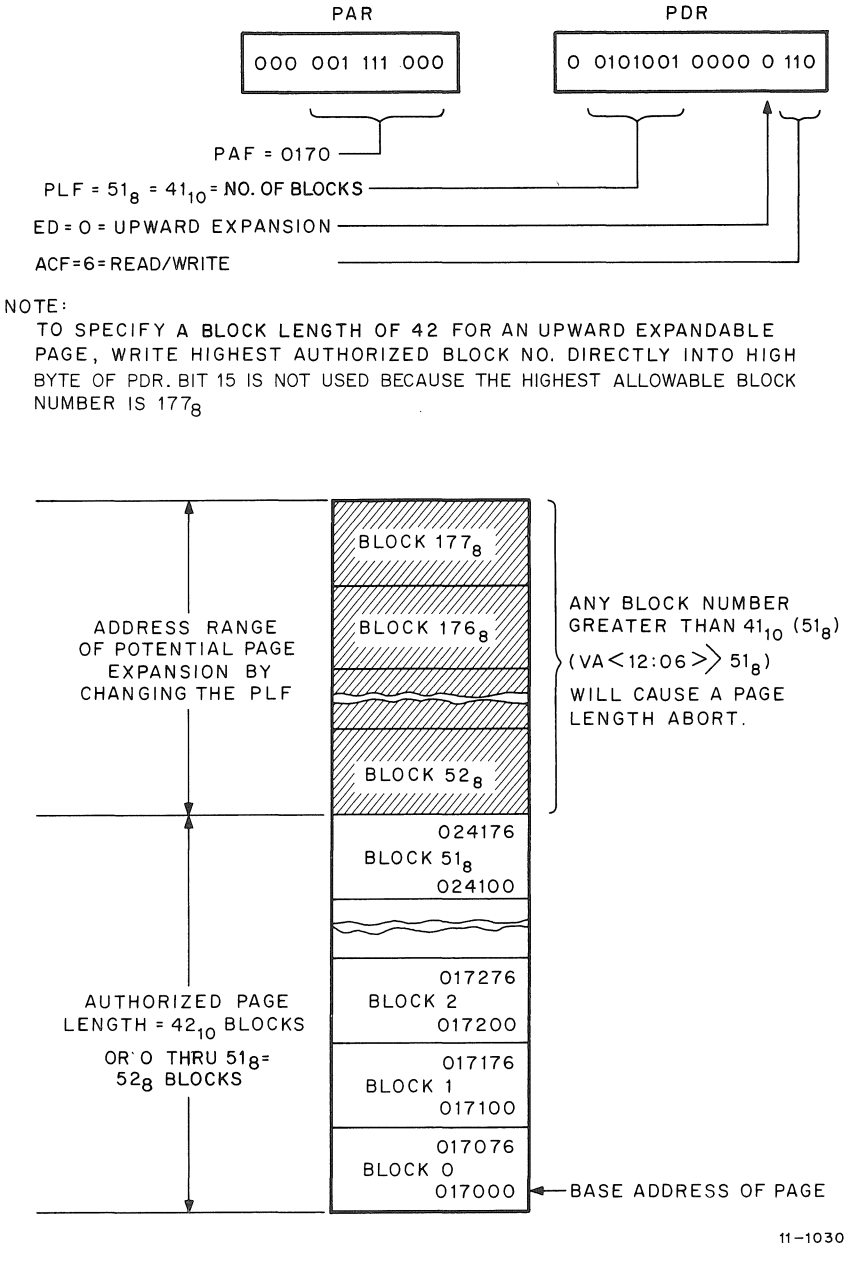


Figure 2-7 Example of an Upward Expandable Page

When the expansion direction is downward (ED=1), the page length is increased by adding blocks with lower relative addresses. Downward expansion is specified for stack pages so that more stack space can be added. An example of page expansion downward is shown in Figure 2-8.

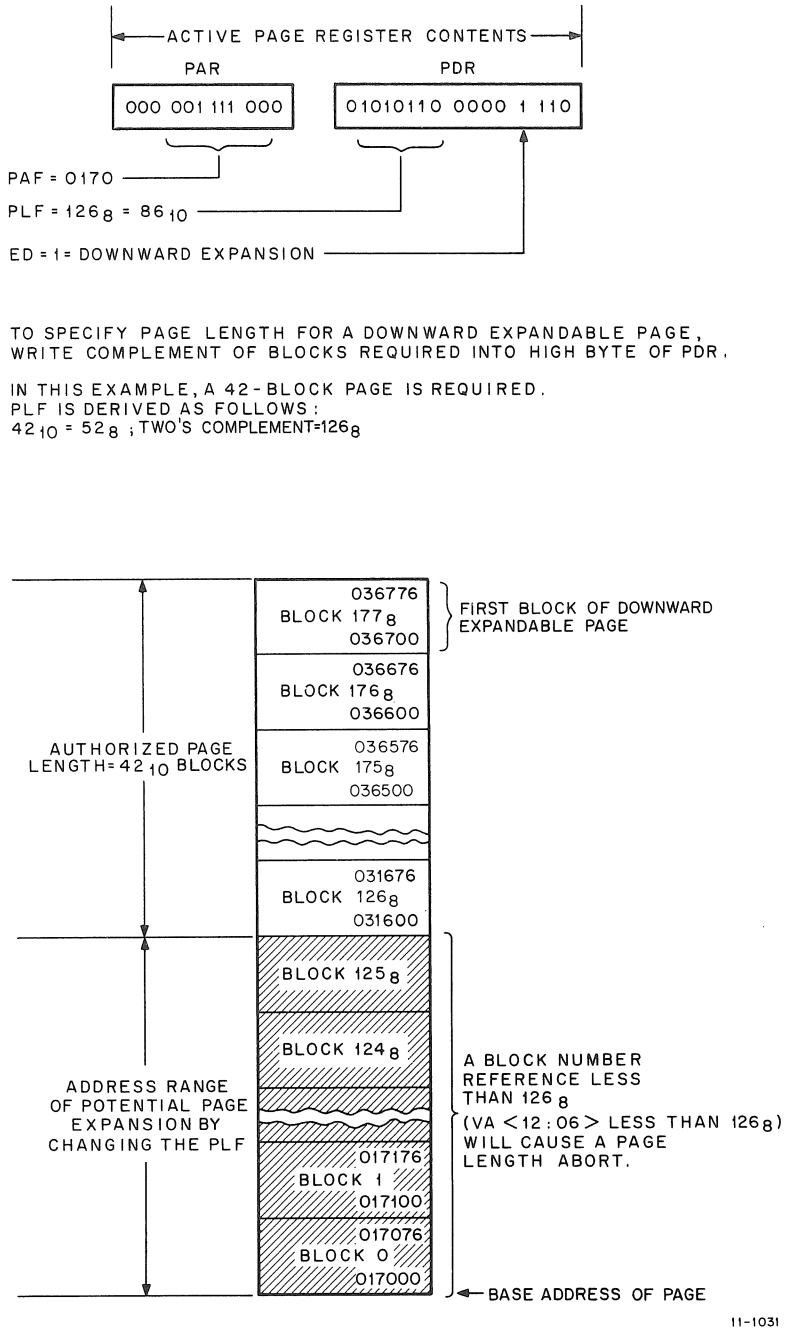


Figure 2-8 Example of a Downward Expandable Page

2.5.2.3 **Written Into (W)** – The W bit located in PDR bit position 06 indicates *whether the page has been written* into since it was loaded into memory. W=1 is affirmative. The W bit is automatically cleared when the PAR or PDR of that page is written into. It can only be set by KT11-D control logic.

In disk swapping and memory overlay applications, the W bit (bit 6) can be used to determine which pages in memory have been modified by a user. Those that have been written into must be saved in their current form. Those that have not been written into (W=0), need not be saved and can be overlayed with new pages, if necessary.

NOTE

The W bit cannot be set by a memory access of a KT11-D internal register (SR0) or a memory access that causes an abort.

2.5.2.4 **Page Length Field (PLF)** – The 7-bit PLF located in PDR bits (14:08) specifies the authorized length of the page, in 32-word blocks. The PLF holds block numbers from 0 to 177_8, thus allowing any page length from 1 to 128_{10} blocks. The PLF is written in the PDR under program control.

2.5.3 PLF for an Upward Expandable Page

When the page expands upward, the PLF must be set to one less than the intended number of blocks authorized for that page. For example, if 52_8 (42_{10}) blocks are authorized, the PLF is set to 51_8 (41_{10}) (Figure 2-7) block 0 being the page boundary and the first block of that page. The KT11-D hardware compares the virtual address block number, VA (12:06) with the PLF to determine if the virtual address is within the authorized page length.

When the virtual address block number is less than or equal to the PLF, the virtual address is within the authorized page length. If the virtual address is greater than the PLF, a page length fault (address too high) is detected by the hardware and an abort occurs. In this case, the virtual address space legal to the program is non-contiguous because the three most significant bits of the virtual address are used to select the PAR/PDR set.

2.5.4 PLF for a Downward Expandable Page

The capability of providing downward expansion for a page is intended specifically for those pages that are to be used as stacks. In the PDP-11, a stack starts at the highest location reserved for it and expands downward toward the lowest address as items are added to the stack. The first block of the downward expandable page being block 177_8.

When the page is to be downward expandable, the PLF must be set to authorize a page length, in blocks, that starts at the highest address of the page. That is always Block 177_8. Refer to Figure 2-8, which shows an example of a downward expandable page. A page length of 42_{10} blocks is arbitrarily chosen so that the example can be compared with the upward expandable example shown in Figure 2-7.

NOTE

The same PAF is used in both examples. This is done to emphasize that the PAF, as the base address, always determines the lowest address of the page, whether it is upward or downward expandable.

The rationale for complementing the number of blocks required to obtain the PLF is as follows:

MAXIMUM BLOCK NO.	MINUS	REQUIRED LENGTH	EQUALS	PLF
177_8	–	52_8	=	125_8

2.6 MEMORY MANAGEMENT STATUS REGISTERS

Aborts generated by the KT11-D logic are vectored through Kernel space address location 250.

The KT11-D has three status registers of which two are functional; SR0, SR2 and SR1 responding with all zeros.

Status Register SR0 and SR2 can be referenced by fault recovery routines to determine why the abort occurred. The following paragraphs describe the formats of both status registers.

2.6.1 Status Register 0 (SR0)

SR0 contains abort error flags, memory management enable, plus other essential information required by an operating system to recover from an abort or service a memory management trap. The SR0 format is shown in Figure 2-9.

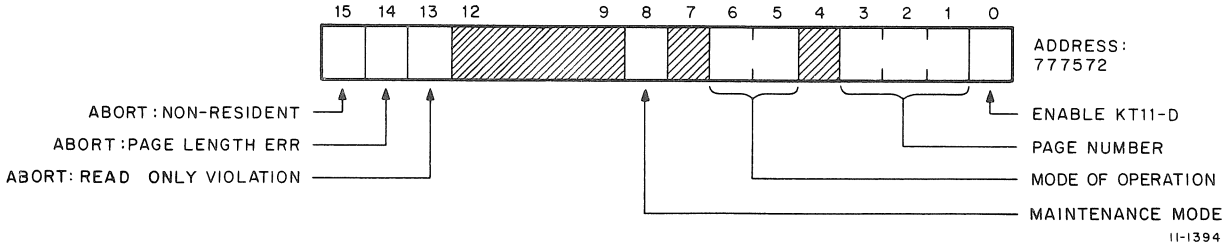


Figure 2-9 Format of Status Register 0 (SR0)

Bits (15:13) are the abort flags and are enabled when an address is being relocated by the KT11-D. This implies that either SR0, bit 0 is equal to 1 (KT11-D operating) or that SR0, bit 8, is equal to 1 and the memory reference is the final one of a destintion calculation (maintenance/destination mode).

NOTE

Bit 15, 14, or 13, when set (abort conditions) cause KT11-D logic to freeze the contents of SR0 bits 1-6 and status register SR2. This is done to determine the cause of the abort.

Note that SR0 bits 0 and 8 can be set under program control to provide meaningful memory management control information. However, information written into all other bits is not meaningful. Only that information which is automatically written into these remaining bits as a result of hardware actions is useful as a monitor of the status of the memory management unit. Setting bits (15:13) under program control will not cause traps to occur. These bits, however, must be reset to 0 after an abort or trap has occurred in order to resume monitoring memory management.

2.6.1.1 Abort-Nonresident – Bit 15 is the "Abort-Nonresident" bit. It is set by attempting to access a page with an access control field (ACF) key equal to 0 or 4 and setting PS (15:14) to an illegal mode.

2.6.1.2 Abort – Page Length – Bit 14 is the "Abort-Page Length" bit. It is set by attempting to access a location in a page with a block number (virtual address bits 12:06) that is outside the area authorized by the Page Length Field (PLF) of the PDR for that page.

2.6.1.3 Abort-Read Only – Bit 13 is the "Abort-Read Only" bit. It is set by attempting to write in a "Read-Only" page having an access key of 2.

NOTE

There are no restrictions that any abort bits could not be set simultaneously by the same access attempt.

2.6.1.4 Maintenance/Destination Mode – Bit 8 specifies maintenance use of the memory management unit. It is used for KT11-D diagnostic purposes. For the instructions used in the initial diagnostic program, bit 8 is set so that only the final destination reference is relocated. It is useful to prove that the KT11-D is capable of relocating addresses.

2.6.1.5 Mode of Operation – Bits 5 and 6 indicate the CPU mode (User or Kernel) associated with the page causing the abort. (Kernel=00, User=11). These bits are controlled by the KT11-D logic that decodes current previous mode bits of the PSW.

2.6.1.6 Page Number – Bits 3–1 contain the page number of reference. Pages, like blocks, are numbered from 0 upwards. The page number bit is used by the error recovery routine to identify the page being accessed if an abort occurs.

2.6.1.7 Enable KT11-D – Bit 0 is the "Enable KT11-D" bit. When it is set to 1, all addresses are relocated and protected by the memory management unit. When bit 0 is set to 0, the memory management unit is disabled and addresses are neither relocated nor protected.

2.6.2 Status Register 2 (SR2)

SR2 is loaded with the 16-bit Virtual Address (VA) at the beginning of each instruction fetch but is not updated if the instruction fetch fails. SR2 is read only; a write attempt will not modify its contents. SR2 is the Virtual Address Program Counter (Figure 2-10). Upon an abort, the results of SR0 bits 15, 14, or 13 being set, SR2 will freeze until the SR0 abort flags are cleared.

Figure 2-10 Format of Status Register 2 (SR2)

2.7 DETERMINING THE PROGRAM PHYSICAL ADDRESS

A 16-bit virtual address can specify up to 32K words, in the range from 0 to 177776_8 (word boundaries are even octal numbers). The three most significant virtual address bits designate the PAR/PDR set to be referenced during page address relocation. Table 2-3 lists the virtual address ranges that specify each of the PAR/PDR sets.

To calculate the physical address, disregard the three most significant VA bits and add the remainder to the PAR contents, right-shifted six places. Example:

```
VA = 167456 =      xxx0 111   100 101 110
+(PAR) = 3456 =    011  100 101 110
 PA = 355256 =     011  101 101  010 101 110
```

Where x indicates these bits are not used in the calculation.

Table 2-3
Relating Virtual Address to PAR/PDR Set

Virtual Address Range	PAR/PDR Set
000000-17776	0
020000-37776	1
040000-57776	2
060000-77776	3
100000-117776	4
120000-137776	5
140000-157776	6
160000-177776	7

CHAPTER 3
LOGIC DESCRIPTION

The purpose of this chapter is to describe the KT11-D Memory Management Unit logic in sufficient detail so that maintenance personnel can quickly determine the function and purpose of the logic circuits shown on the block schematics in the engineering drawings. Because the block schematics are drawn to show more than one functional section of logic per sheet, the major paragraphs in this chapter follow the sequence of block schematic organization.

3.1 PDP-11 SYSTEM INTERFACE

In the PDP-11 system the KT11-D Memory Management Unit is located between the KD11-A Central Processor Unit and the Unibus A address lines, as shown in Figure 3-1. Once installed, the Processor ceases to supply address information to the Unibus. Instead, addresses are sent to the KT11-D where they are either throughput without change or relocated by various constants computed within the KT11-D.

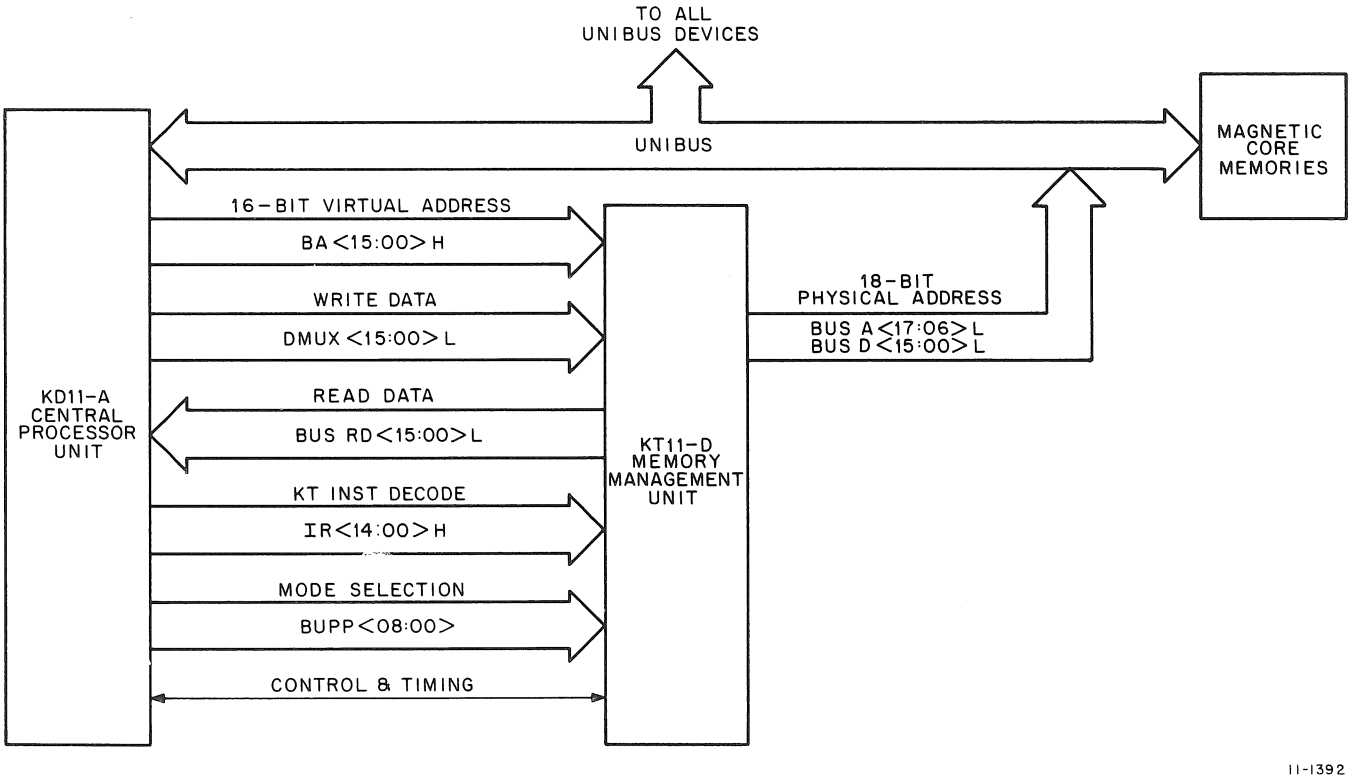


Figure 3-1 KT11-D Memory Management Unit System Hardware Interface

The address provided to the Unibus as BUS A (17:00) L is the result of the KT11-D supplying an 18-bit physical address, PBA (17:00) H, which is created by manipulating a 16-bit virtual address from the processor Bus Address Register, BA (15:00) (1) H. The KT11-D internal registers are all assigned specific physical addresses to enable manipulation under program control. Access to these registers is derived by decoding the processor bits BA (05:00) (1) H and the KT11-D derived PBA (17:06) H. Data to these registers is received from the processor internal Multiplexed Data bus, DMUX (15:00) H, while data from the KT11-D is made available via a DATI bus cycle through the Unibus Data bus, BUS D (15:00) L. Data from implicit operations under internal processor control (as in traps, RTI, etc.) is received by the KD11-A (processor) through an internal Register Data Bus, BUS RD (15:00) L, for temporary storage and current or future manipulations. The implementation of the KT11-D instructions is made by sampling the KD11-A internal Instruction Register, IR (14:00) (1) H, to supply various mode and conditional restrictive uses.

With the installation of memory management, the Processor no longer is responsible for decoding various registers (REG ADRS, PS ADRS, SR ADRS, and SLR ADRS) because address selection is now comprised of an 18-bit address and no longer that of the internal Bus Address Register, BA (15:00) (1) H.

In order for the KT11-D to perform its function, certain modifications to normal processor operation must be made. These include actual wiring changes to the Processor and signal interactions that revise the way in which the Processor reacts to certain situations.

These are termed "hooks" and are described in detail in Chapter 4, Installation.

3.2 KT11-D ORGANIZATION

The general operation of the KT11-D can be traced in Figure 3-2. A 16-bit virtual address BA (15:00) H is received and applied to both the BA Buffer on drawing KT-8 and the SP Select Multiplexer (KT-5). The Buffer is used to eliminate BA Bus loading, and to further distribute the virtual address (VBA (15:00) H) to the SR2 Register (KT-8), to an ALU on KT-4, to write enable logic on KT-6, and to a PAR/PDR Address Select Multiplexer on KT-5.

The SR2 register is used to store the virtual bus address at the beginning of each fetch cycle making it a Virtual Address Program Counter. Its contents are then made available to the Unibus through the KT DATAMUX (KT-8, 9) and BUSD drivers, where it may be read via a DATI to the Processor.

The ALU of KT-4 is identical to that used in the KD-11 except that only three throughput modes of operation are utilized. The output of the ALU is the physical address supplied by the Memory Management option to the Unibus. The physical address PBA (17:06) H, reflects three different Memory Management conditions:

1. Supplying in non-relocate mode straight throughput of the Virtual Address, VBA (15:06) H, and the processor BA (05:00) H to the physical bus.

2. Supplying in relocate mode, as the result of KT-3. Relocate (0) H flag, a relocated virtual address from the processor. This is obtained by adding a base constant from a virtual page PAR, PAR (11:00) (1) H, to the Virtual Address, VBA (12:06) H, resulting in an 18 bit Physical Address, PBA (17:06) H, plus virtual Bus Address, BA (05:00) (1) H.

3. Under console control the address specified by the 18 bit Switch Register, REG SR, is straight throughput to the Physical Address bus, PBA (17:06) H, plus virtual Bus Address, BA (05:00) (1) H.

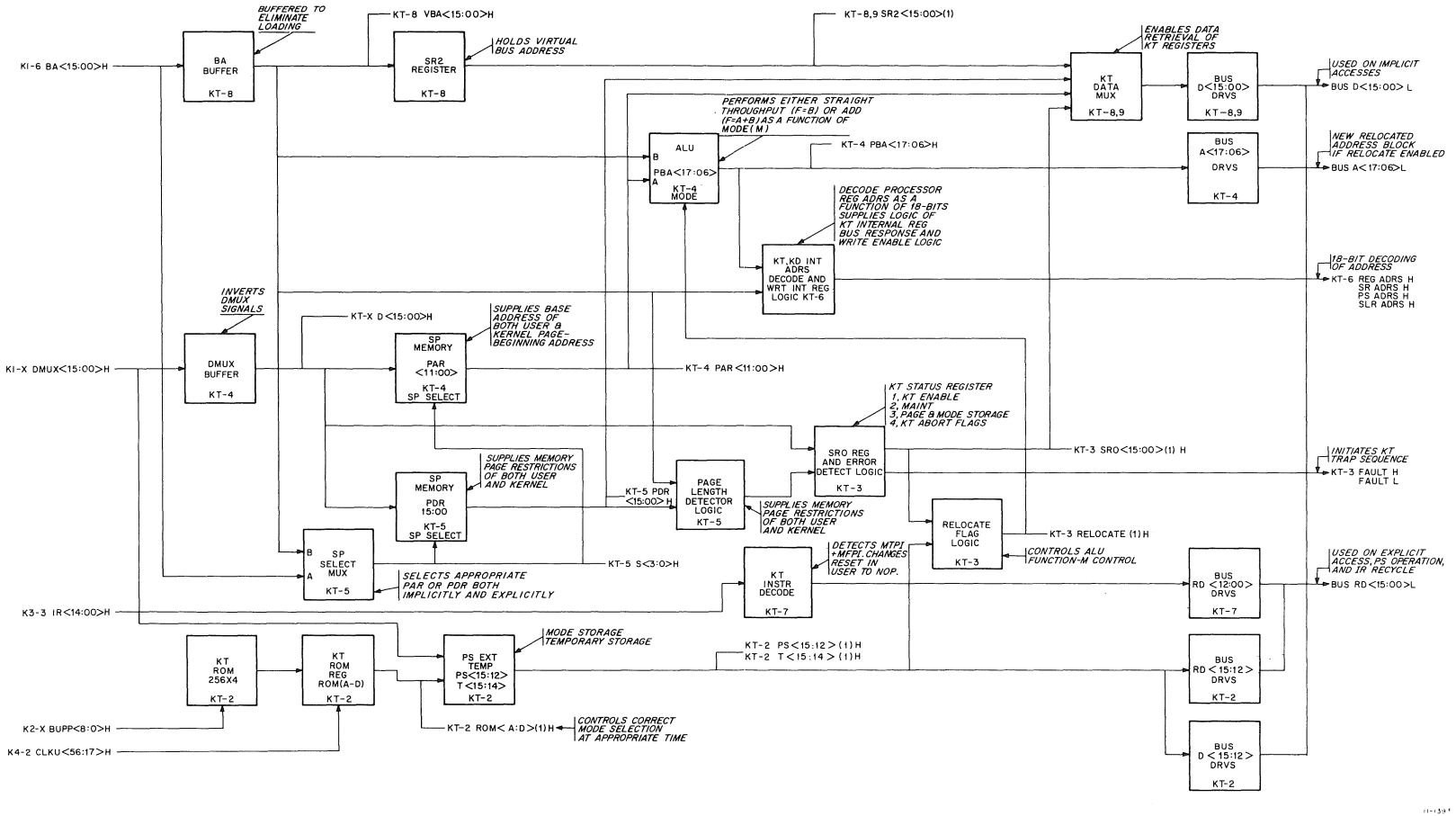


Figure 3-2 KT11-D Memory Management Block Diagram

The KT/KD Internal Address Decoder on KT-6 receives inputs from both the BA Buffer and the ALU. It is used to determine whether the address is internal to the KT11-D or internal to the Processor. This circuit decodes all the processor registers as a function of 18 bits (REG ADRS H, SR ADRS H, PS ADRS H, SLR ADRS H) or registers internal to the KT11-D. If it is an internal address to the KT11-D, Memory Management generates a false bus cycle by inhibiting MSYN to the bus and generating a false SSYN, thereby eliminating it as an external bus cycle.

To load the PAR/PDR registers under program control, selection is made by utilizing the physical address assigned. This appropriate selection, using a physical address, is made by the KT11-D decoding an internal address utilizing VBA (03:01) and PBA06 to enable selection under program or manual control.

Once the KT11-D has set up the proper selection of a PAR or PDR register, the data (DMUX (15:00) H) is fed through the DMUX Buffer on KT-4 to the two scratch pad REGISTERS PAR and PDR. It is also sent to the KT Status Register SRO (KT-3). If the address is to be relocated, SRO 00 is set to a 1. This is the RELOCATE ENABLE bit used to set the Relocate Flag logic on KT-3. As described earlier, this controls the Mode functions of the ALU.

While the PAR is being accessed to setup a physical relocated address; the output of the PDR contains a Page length Field and an Access Control Field that contain the restrictions of the virtual address being monitored. Memory Management then monitors logic on KT-5, Page Length Detector logic and Error Detect logic on KT-3 and if an error is detected, various error flags are set in the Error Detect logic of SRO on KT-3. Setting any of these flags results in a KT-3 Fault signal being sent to the processor where it initiates a Memory Management trap sequence.

When an instruction is fetched, the data portion of that address is decoded as an instruction. The Processor, however, is unable to recognize the Move To Previous (MTP) and Move From Previous (MFP) instructions and would normally trap as an "illegal instruction" when they were issued. The KT11-D, however, is capable of decoding these instructions. This is done by intercepting the IR (14:00) H bits and feeding them to the KT Instruction Decoder on KT-6 where a signal is created to cause the Processor to recycle in Fetch. Meanwhile this circuit jams correction bits on the RD Bus (in KT-7) to cause these instructions to appear to the Processor as a MOV instruction on the Fetch recycle.

When in User Mode, this same circuitry prevents the Processor from executing an INIT on a RESET instruction. This is done in the same way as above, causing a Fetch recycle and jamming the RD Bus to 240, thereby simulating a NOP instruction.

The Branch Microprogram Pointer bits (BUPP (08:00) H) are fed to the KT11-D ROM on KT-2. This is a 256 word 4-bit ROM that acts as an extension to the ROM internal to the Processor. The ROM outputs are buffered in a 4-bit REGISTER (KT ROM REG) also on KT-2. This output is used to control correct mode selection at appropriate Processor Flow ROM words. This is fed also to the PS EXT TEMP register on KT-2 that functions as a mode storage or temporary storage.

The KT PS EXT is an expansion of the internal KD11-A Processor Status Word. Access of this register can be made either explicitly or through implicit operations. Explicit operations are made by a DATI or DATO Unibus cycle. Implicit operations are conducted on the Processor RD Bus (15:00).

The output of the mode/temporary storage [PS (15:12) (1) H and T (15:14) (1) H] is then fed to the Relocate Flag Logic on KT-3, and to both the Bus D and the Bus RD through appropriate drivers on KT-2.

3.3 KT11-D CIRCUIT DESCRIPTIONS

These discussions are keyed to the logic contained on each block schematic in the print set. Where necessary, cross reference to other schematics is given. They are provided as an aid to understanding the way in which the KT11-D performs its function but they cannot as such give a complete picture of the ways in which they interact, or the way they perform in conjunction with the KD11-A. It is recommended that these discussions be read while referring to the flow diagrams provided for both the KT11-D and the KD11-A. Reference should also be made to the block diagram discussion in Paragraph 3.2.

3.3.1 KT PS Extension Logic

The KT11-D PS Extension Logic is shown on Drawing KT-2. This circuit contains the KT Extended Processor Status bits PS (l5:14) (current mode), and PS (13:12) (previous mode) together with the temporary mode bits T (15:14). The circuit comprises a portion of the DMUX Buffer, feeding the PS Extension Register which, in turn, feeds both a Mode Multiplexer and two sets of bus drivers (D and RD). The Mode Multiplexer is fed also by an instruction/mode decoder conditioned by the two memory management instructions (MFPI and MTPI) and combinations of the KT ROM Register (A:D). This ROM Register controls the selection of the "current", "previous", or "temporary" modes on explicit and implicit access operations to an appropriate stack or space.

The ROM Register is fed by the KT ROM, used to control various functions within the Memory Management option. The KT ROM is a 256-word, 4-bit-wide device, used in conjunction with the KD11-A ROM to perform various functions at appropriate flow function words. Being a 4-bit field, the KT11-D logic utilizes only 7 of the 2^4(16) possible control patterns. The KT ROM patterns used are as follows:

NOTE
Also see table on Drawing KT-2.

	A	B	C	D
1	0	0	0	0
2	0	0	0	1
3	0	0	1	0
4	0	1	0	0
5	0	1	1	0
6	1	0	0	1
7	1	1	0	0

ROM A and ROM B are utilized to select the appropriate source of mode/space to be used on a memory access. These patterns are described as follows:

ROM A	ROM B	DESCRIPTION
0	0	Current Mode; PS (15:14) used to determine operating mode/space.
0	1	Temporary Mode; T (15:14) used to determine operating mode/space.
1	0	MTPI/D; Previous Mode, PS (13:12) used to determine operating mode/space.
		NOT–MTPI/D; Current Mode, PS (15:14) used to determine operating mode/space.
1	1	MFPI/D; Previous Mode, PS (13:12) used to determine operating mode/space.
		NOT–MFPI/D; Current Mode, PS (15:14) used to determine operating mode/space.

ROM C is used to enable clocking of PS (15:14) (current mode) into PS (13:12) (previous mode) for future controlled access and clocking of T (15:14).

ROM D bit is placed in conjunction with the final bus cycle of the KD11-A instruction for relocation in destination mode only.

The KT11-D ROM fields described above are documented in the KD11-A Processor Flows. A KT11-D ROM field is indicated as MM=xx and that ROM pattern exists when that particular ROM word in the Processor is in logic control. This information is collected and presented in Table 3-1.

Referring specifically to drawing KT-2, at location D-6, the AND/NOR (E86) is used to make a distinction between an explicit and implicit access to the Processor Status Word.'The output of E86 clocks DMUX bits 15:12 into flip-flops PS15, 14, 13, 12. An explicit access to the PSW would be via a bus operation. The lower set of signals feeding E86 are generated on implicit accesses such as traps, RTIs, etc.

Table 3-1
Memory Management ROM Fields in KD11-A Flow Diagrams

KTROM Field		KT/KD ROM ADS		PROC ROM WD	Access Mode	Description
ABCD	MM=	Octal	Decimal			
			ALLDOP* -SM0			
1100	14	142	098	SRC01	SM2	Get Source Data: Modify
1100	14	144	100	SRC02	SM4	Get Source Data: Modify
1100	14	141	097	SRC00	SM1	Get Source Data
1100	14	242	162	SRC08	SM6	Get Indexed Source Data
1100	14	246	166	SRC13	SM3 SM5 SM7	Get Source Data
			(PARTDOP* SM0 + ALLDOP)* -DM0 or PARTDOP ← SM0 ← DM0			
0001	01	162	114	DST01	DM2	Get Destination Data: Modify
0001	01	164	116	DST02	DM4	Get Destination Data: Modify
0001	01	161	113	DST00	DM1	Get Destination Data
0001	01	262	178	DST10	DM(6+7)	Get Indexed Destination Data
0001	01	265	181	DST13	DM(6+7) *IR03 DM3,DM5	Get Destination Data

Table 3-1 (Cont)
Memory Management ROM Fields in KD11-A Flow Diagrams

KT ROM Field		KT/KD ROM ADS		PROC ROM WD	Access Mode	Description
ABCD	MM=	Octal	Decimal			
			MOV			
1001	11	200	128	MOV16	-SM0*-BYTE	Store Data
0001	11	201	129	MOV17	SM0*-BYTE	Store Data
1000	10	204	132	MOV20	SM0*DM0	Store Data
0001	01	205	133	MOV15		Store Justified Data
			TRAP			
0100	04	215	141	TRP02		Get Kernel space vector on MM fact
0100	04	007	007	TRP08		Get New Status from Kernel vector space
0110	06	115	077	TRP09		Store New Status. Store T (15, 14) with New Status
0100	04	326	214	TRP10		Modify Stack Pointer
0100	04	327	215	TRP11		Store Old Status on Stack space determined by new status
0100	04	113	075	TRP12		Deskew Word for DATO
0100	04	330	216	TRP13		Modify Stack Pointer
0100	04	331	217	TRP14		Store Old R [PC] on Stack
0100	06	077	063	TRP15		Enable New Status
0010	02	140	096	TRP16		Load New Status. (Shifts 15:14 to 13:12 and clears T 15,14).
0100	04	332	218	TRP20		Get New R [PC]
			PARTDOP* -DM0			
0001	01	224	148	DOP07	SM0 XOR -SUB	Operate upon B. Source: Store
0001	01	225	149	DOP03	-SUB-SM0	Operate upon B, Source: Store

Table 3-1 (Cont)
Memory Management ROM Fields in KD11-A Flow Diagrams

KT ROM Field		KT/KD ROM ADS		PROC ROM WD	Access Mode	Description
ABCD	MM=	Octal	Decimal			
			PARTDOP*-DM0 (Cont)			
0001	01	365	245	DOP06	SUB	Subtract B from Dest: Store
0001	01	366	246	DOP11	OB	Duplicate Lower Byte: Store
			SXT* -DM0			
0001	01	234	156	SXT01		Extend Sign: Store
			SOPMORE+SWAB			
0001	01	221	145	SSL04	NEG	Negate Dest: Store
0001	01	236	158	SSL05	SWAB	Swap Bytes: Store
0001	01	220	144	SSL06	-(Next SWAB	Operate Upon Dest: Store
0001	01	374	252	SSL09	OB	Duplicate Byte: Store
			ROTSHF (R)* -DM0			
0001	01	275	189	RSR07	-BYTE	Store Destination
0001	01	276	190	RSR09	BYTE	Duplicate Byte: Store

To set up the current mode, either 0s or 1s are loaded into bits PS (15:14), and every time that is done, the previous contents of 15:14 are loaded into bits 13:12 by virtue of PS (15:14) (0) H being gated to PS (13:12) D inputs. It can be seen from this that bits 13 and 12 always indicate the previous mode. This is "previous" storage and the logic for PS (15:14) constitutes the extended PS word.

PS bits 15:12 are applied to two sets of drivers, one set for Bus D and one for Bus RD. The Bus D drivers are used for explicit accesses and the drivers for Bus RD are used for implicit accesses.

Flip-flops T15 and T14 are used as "temporary storage" of a temporary mode. These flip-flops are clocked or cleared on combinations of the outputs of the ROM Register. The table on the right hand side of the drawing shows the combinations of ROM A:B that select the MODE to use. These ROM outputs are further decoded by the gate at E69 as a function of the instruction (MFPI/MTPI) to control the MODE MUX yielding MODE SEL 1 or MODE SEL 0. These signals are sent to a register on KT-3 to update the mode field of SR0.

3.3.2 Status Register Zero (SR0)

Status Register Zero logic is shown on Drawing KT-3. This is one of the two functional status registers in the KT11-D. This register contains the abort error flags, memory management enable bit, plus other status information.

The Mode Mux output on KT-2 is fed to the register at E51 as MODE SEL (1) H and MODE SEL (0) H. The current mode that was selected by the registers of the PS word in T (15:14) and PS (15:12) on KT-2 go through the multiplexer on that drawing to this multiplexer and are applied to the register at E49 to update the mode (SR0 (06:05)). Virtual Bus Address bits 15:13 update the page on every access (SR0 (03:01)). These are constantly updated with the mode and virtual page number being clocked by P CLK MSYN into the SR0 register on every bus cycle, unless an abort has occurred.

The signal ABORT (at location C-4) occurs as a result of any KT error flag being set. If any *are* set, notice that ABORT H folds back and disables a NAND gate at E73, thereby preventing P CLK MSYN from further clocking the SR0 register and freezing its contents.

The bits in SR0 are as follows (see right-hand side of KT-3):

a. Bit 00, the Relocate Enable bit is the most important bit in the register. No matter what mode the KT11-D is in, User or Kernel, no protection qualities of the KT11-D are available unless this bit is set. This must be set to utilize memory management relocation, etc.

b. Bits 01 through 03 are updated with the current virtual page number. That current page being the virtual BA bits 15:13. When the BA bits are received, these bits indicate a particular pair of Page Address and Page Descriptor Registers used in the last relocated bus access.

c. Bits 05 and 06 are the mode bits. This field indicates what mode the KT11-D was in as determined by the register in the middle of KT-3, which is, in turn, the result of the ROM output and the PS bits (see table on KT-2) of the last relocated bus access.

d. Bit 08 causes the KT11-D to relocate on destination mode only. This bit is used for maintenance purposes only. It causes relocation only on the destination calculation. Referring to the right-hand side of the print KT-3, setting SR0 00 and 08 to a 1 will result in RELOCATE (1)/(0) H to enable the control of the M bit of the ALU function (on KT-4).

The signal CLK BUS H at C-7 is used to update the current mode on every bus operation into the register @E51. Detection logic for the KT Fault flags is shown on the left side of the print. If any of these flags are set, the detection output through an OR gate enables the generation of the signal KT FAULT. This signal goes into the Processor to enable a trap sequence. The trap vector for KT FAULT is 250.

To get a KT FAULT, the KT11-D must be in relocation [RELOCATE (1) H], must not be in a [STALL (1) L], no odd address error must exist [CKODA (1) H], and the system must not be in a console loop [CONSL (1) L]. All this guarantees that the system is under program control and running a program.

3.3.3 Page Address Register and Physical Bus Address (KT-4)

The logic shown on KT-4 supplies the base address of both the User and Kernel page, and provides a means of relocating a virtual address. The circuit comprises a DMUX Buffer (DMUX (11:00) H), a PAR Register, and an ALU (PBA (17:06)).

The DMUX signals are used, in this print, to load the PAR. This is a scratch pad memory controlled by signals S (3:0) as generated on KT-5 by the S MUX. These signals select one of 16 base address registers, 8 each for either User or Kernel mode.

The output of the PAR is then fed directly to the Physical Bus Address Register (ALU). Note that if RELOCATE ENABLE is not set, this output means nothing.

In the KD11-A processor flows, at an appropriate time, the signal K4-5 BUS FM BA H is generated. This signal supplies the Bus Address Register, BA (15:06) (1) H to the Unibus Bus A. This is what the processor would normally do on a bus cycle, but when the KT11-D is installed in the processor, the processor no longer supplies an address to the Unibus, BUS A (17:06) L. The KT11-D Physical Bus Address Register PBA (17:06) H and Bus Address BA (05:00)H, will now supply all addressing to the bus.

3.3.4 Page Descriptor Register (KT-5)

The Page Descriptor Word logic (PDR) is shown on KT-5. These registers hold information pertaining to page restrictions of both User and Kernel pages. The circuit comprises a 2-to-1 multiplexer (S MUX), enabled by the internal address condition PAR + PAR SEL (1) H, four register chips configured to hold only the *useable* bits in the PDW, and two comparators that constantly compare the PLF field with bits 12:06 of the virtual address yielding either VBA > PLF H or VBA < PLF H. The outputs PDR (14:08) specify the authorized length of the page in 32-word blocks. This permits page lengths between 1 and 177_8 blocks. The output of this comparator, VBA < PLF H, is sent to KT-3 where it joins the other bits in this register to generate a FAULT condition.

Note that the W bit is a flip-flop that is cleared by B INIT L, clocked by CLK MSYN H, and conditioned by the state of PDR 06. This bit is used to indicate whether the page has been written into by the User of a page since that page was loaded into memory. To prevent that bit from setting when the KT11-D looks at its own registers, the signal SR0 SELECT H is generated on KT-6 to disable the PDR 06 register write logic.

If PDR 06 is enabled (SR0 SELECT H is false), it sets the W bit which ANDs with KT-6 PAR + PDR L to recirculate the set condition.

3.3.5 Internal Address Decoder (KT-6)

The Internal Address Decoder, shown on KT-6, decodes Processor and KT11-D internal addresses as a function of an 18 bit physical address. In addition, it provides logic for KT11-D internal register bus response, and write enable logic.

As illustrated in the overall block diagram (Figure 3-2), the KT11-D uses both the virtual address (VBA) and the physical address (PBA) to decode internal addresses. In regular internal bus addresses, bits (05:00) are not relocated but are sent straight through without going through the KT11-D. But even though bits VBA (15:06) are not relocated they automatically become a physical bus address in that bits (15:06) are automatically changed to bits VBA (17:06) since if bits 15, 14, 13 are set, bits 17:16 are set also. The KT11-D therefore automatically decodes particular addresses such as the Processor REGISTER Addresses shown in the lower right-hand corner of the print. Internal KT11-A addresses are also decoded as an 18-bit instead of a 16-bit address.

The KT11-D has two internal address flip-flops (ADRS and INT ADRS). One is initially set when an internal address has been detected and is clocked when MSYN (1) H is asserted. The one-shot PMSYN delays the CLK MSYN thereby buffering the ADRS flip-flops into the INT ADRS flip-flop. Notice now that two flip-flops are set indicating that an internal address has been detected. Once set, these two flip-flops set another one-shot (74123 @ E-85) for an additional 200 ns. This, in turn, clears the ADRS flip-flop, and at the same time initiates the next one-shot called WRT (write).

When accessing a PDR, an internal address is decoded thereby setting off this chain of flip-flops and one-shots. The signal INT ADRS (1) H results in the signal NO MSYN L, which prevents MSYN from being sent to the bus in the processor. The WRT one-shot causes a false slave sync (BUS SSYN) to be sent out on the bus thereby terminating the bus cycle. There will be a nonresponded BUS MSYN on the bus.

Outputs of the WRT REG provide the write enable logic for internal KT11-D registers. Its decoded outputs are applied to two sets of buffers enabled by either K4-4 DOUT LOW H or K4-4 DOUT HIGH H. These result in the High/Low Write signals permitting the data to be written into the appropriate registers at the proper time.

On accesses of the registers, DATI (IN L) is decoded by looking at K4-4 BC1 (0) H. This is inverted and conditioned by a signal that indicates its an internal register [INT ADRS (1) H]. This yields DMUX ENABLE L permitting the KT11-D to multiplex its data onto the data bus. This is accomplished on KT-8, 9 where it is used to enable the strobe (STB) on the DMUX.

3.3.6 KT Instruction Decoder (KT-7)

The KT11-D Instruction Decoder is shown on Drawing KT-7. This logic detects the two memory management instructions and performs certain operations on the RD Bus to modify the Processor's response to these instructions.

When, on an instruction fetch, data is received from an address, this data is clocked into an IR register in the processor because it is to be decoded as an instruction. There are two instructions that are unique to the KT11-D option. These are the Move From Previous (MFPI) and Move To Previous (MTPI) instructions. Since these two instructions are unfamiliar to the Processor, once the KT11-D recognizes them, it causes the Processor to go back to a Fetch cycle and read the RD Bus again. At the same time it jams appropriate bits onto the RD Bus to cause that instruction to look like a MOV instruction.

The KT instruction decoding logic is comprised of decoding the Processor Instruction Register, IR (14:06) H, and two flags indicating the decoding of a MFP or MTP instruction. Upon decoding of these instructions the signal KT INSTR L is created. This signal is sent to the Processor to initiate a KT RECYCLE to reFETCH the previous PC and jam a new instruction into the IR Register; being the equivalent processor execution of a Mov instruction as previously discussed in the programming section. There also exists logic of which the signals K3-6 PRIV INSTR L, PS 15 (1) H and IR 00 (1) H prevents the execution of a RESET instruction when in User mode, and causing the coding of a NOP instruction to be executed in its place again as the result of a KT jamming of the RD Bus initiated by a KT RECYCLE.

3.3.7 Status Register 2 and Data MUX (07:00) (KT-8)

The logic for SR2 is shown on Drawing KT-8. This circuit comprises a BA Buffer, the Status Register (SR2 (15:00)), a Data Multiplexer (DMUX (07:00)), and Bus D drivers.

The status register functions as the virtual address program counter storing the address from the Processor every time the IR is clocked (every Fetch cycle).

Note that on the trailing edge of CLK IR H (location B-8) the SR2 register is clocked if no abort condition exists (ABORT H is low). If an abort occurs as a result of any of the control logic or detection circuits on KT-3, ABORT H will freeze the contents of this register.

The data multiplexer is enabled by DMUX ENABLE L on KT-6 which is the result of an internal address detection of either a PAR, a PDR, an SR0, or an SR2. When enabled, the KT11-D can put any one of these four internal address data into the Processor Bus D as selected by the signal PAR + PDR SELECT (0) H ANDed with either VBA05 H or VBA02 H. These detect which of the four registers is being called for.

3.3.8 Data Mux (15:08), SP Select, and KT Console Control (KT-9)

The logic on Drawing KT-9 comprises a "hook" multiplexer that selects the appropriate signals from the processor to select the correct stack, a KT Console Control Register to allow the switches to access a full physical 128K of core, and the rest of the KTDMUX with its buffering to Bus D.

The Console Control Register (SR (17:16)) is fed by the Processor console signals SR (17:16). Its output feeds the BA Mux bits 17:16 and the console via cable where the two status lights VIRTUAL and USER are enabled to indicate the mode of operation and Bus A indicator leds 17 and 16.

It is necessary, when the system is in console mode, to access the entire 128K possible physical memory from the console switch register. This is accomplished by the KY11-D SR (17:16) signals from the console being fed into the

SR (17:16) register at B-7. The AND of BUT05 H and PS (P1 + P3 H) indicates that the system is in the console loop and is used to clock the contents of the switch register into buffers and back to the processor where it is displayed. These contents are also fed to the A inputs of the BA MUX to be sent as A (17:16) to the input of the ALU at location D-4 on KT-4.

When the system is not in the console mode, the Processor detects the fact that bits BA (15:13) are set, and creates the signal BA (17:16) H. This signal is fed to the B inputs of the BA MUX and if the signal BA (17:16) H is asserted, A (17:16) H is created which enables the Physical Bus Address to the external peripheral bank.

The operation of the "hook" circuitry in the upper left-hand corner of the print pertains to using the appropriate space of an MTP or MFP instruction. These instructions move contents from one space to another space either from Kernel space to User space or from one User space to another User space. Move To and Move From Previous instructions utilize bits 15:13 of the Processor Status Extension with the previous mode being determined by the contents of bits 13:12 and the current mode by the contents of bits 15:14. In these bit positions User mode is indicated by 1s and Kernel mode by 0s.

When the Move From Previous instruction is executed in source mode 0 and previous mode = current mode, the destination stack is normally decremented before access. This is undesirable as the stack should be updated so that it can be used. The HOOK MUX logic is provided to correct this fault by causing an increment to update the stack. Logic to the left of that multiplexer detect whether it is a source mode zero (SM=0 L) or a destination mode zero (DM=0 L). These are each ANDed with instruction detection (MFPI (1) L or MTPI (1) L) flags. The logic also detects whether it is an R6 Stack Pointer Register (IR (2:0)=6 L or IR (8:6) L) used for Kernel mode, or an R16 Stack Pointer Register (K5-5 SBC=16 L) used for User mode. These conditions are then combined to yield MFP SM0 L, that is sent back to the Processor Status Constants logic where it chooses the correct source stack address; and to further generate S HOOK H and D HOOK H. These latter two signals are sent to the Processor Internal Register Selection circuitry on K1-8 where they enable the correct selection of User and Kernel stacks in either explicit or implicit operations.

3.4 KT11-D SIGNAL SUMMARY

The signals that are generated by the KT11-D and supplied to the KD11-A Processor and Console are listed and described in Table 3-2.

Table 3-2
KT-D Signal Summary

Signal Name	Function
KT-2 INH PS CLK 2 L	Inhibits the clocking of Current Mode PS (15:14), Previous Mode PS (13:12) on implicit operations during an RTI, RTT Sequence, in User Mode.
KT-2 MODE SEL1 H, KT-2 MODE SEL0 H	With the use of ROM bit control, the correct mode is multiplexed from the PSW to enable detection logic and Mode Status in SR0.
KT-2 ROMD (1) H	KT11-D ROM control bit used to enable relocation.
KT-7 KT INSTR L	The decoding of the instructions Move From Previous Space (MFPI, MFPD), Move To Previous Space (MTPI, MTPD), or the Privileged Instruction in User Mode of Reset, this signal causes the recycle of partial fetch to catch KT Instruction on RD Bus.

Table 3-2 (Cont)
KT-D Signal Summary

Signal Name	Function
KT-9 MFP SM0 L	This signal is used to enable the instruction MFPI/D R6, when the source is R6 Mode 0 to load the previous stack pointer to the address of the present stack, not decrementing the SP before the DATI; i.e., Previous SP = 100, Current SP = 200, MOV 100,200.
KT-9 D HOOK H KT-9 S HOOK H	These signals enable the current reference to either the User or Kernel stack depending upon execution of a KT instruction and Current/Previous modes.
KT-9 A17 H KT-9 A16 H	With the KT11-D option installed in a KD11-A, an 18-bit Unibus Address is made available from the KT11-D under RELOCATE ENB; and, under console control, from the switch register.
KT-9 KT SR17 L KT-9 KT SR16 L	Under console control, these two signals are used to drive the address LEDs on the Console.
KT-9 RELOCATE ENB L	When the KT11-D is installed in the KD11-A, this signal drives the console LED indicator VIRTUAL. It indicates to the operator that the physical Address on the bus is not necessarily the address of the internal data path bus address; i.e., of the KD11-A Processor. With the KT11-D not installed or disabled, this indicator is not lit.
KT-9 PS15 L	When the KT11-D is installed in the KD11-A, this signal enables the lighting of the USER indicator. This indicator signals the operator that the user has control of the Processor Bus.

CHAPTER 4
INSTALLATION AND MAINTENANCE REFERENCE INFORMATION

4.1 INSTALLATION

The installation procedure for the KT11-D Memory Management Unit option is included as part of the complete PDP-11 system installation procedure described in Chapter 2 of the *PDP-11/40 System Manual*. Specific procedures for wiring changes to the Processor are given below with descriptions of hook operations that require no wiring changes. When the KT11-D is included as part of the initial PDP-11 system, the M7236 module is installed prior to shipment. If the KT11-D option is being added to an existing PDP-11 system, the installation procedure is straightforward. The M7236 module is installed in slot 8, rows A-F of the CPU backplane assembly.

The wiring modifications to the KD11-A Processor that are necessary are as follows:

a. Refer to Processor Block Schematic K1-6, location A-6, and move jumper W10 to the ground inputs of the 8881 gates. This change disables the KD11-A from giving an address to the Unibus (Figure 4-1).

b. Refer to Processor Block Schematic K1-8, location C/D-8, and remove jumpers W5, W6, and W9. This change enables the correct selection of User and Kernel stacks in either explicit or implicit operations (Figure 4-2).

c. Refer to Processor Block Schematic K1-7, location C/D-3, and remove jumpers W1, W2, W3, and W4. This change enables the KT11-D to use an 18-bit virtual address to decode all internal register addressing (Figure 4-3).

d. Refer to Processor Block Schematic K4-4, location C-5. Remove jumper W2 and connect jumper W2A. This change connects pins 10, 11, and 12 of 74H55 module at location E-6 to A07H2 (KT-3 FAULT H). This change enables the KT11-D to start a trap sequence for a KT Abort condition (Figure 4-4).

e. Refer to Processor Block Schematic K1-9, location D-5. Remove jumpers W7 and W8. This change disables automatic operation of console address lights BA (17:16) on assertion of K1-6 BA (17:16) from the Processor (Figure 4-5).

f. Refer to Processor Block Schematic K4-4, location C-4. Add capacitor C113 (680 mmf, 100 WVDC) DEC Part Number 10-00026. This change extends the CLK MSYN H delay from 150 ns to 300 ns to enable memory management logic to propagate a new address to the Unibus while retaining bus specifications (Figure 4-6).

g. Refer to Processor Block Schematic K4-4, location D-4. Add capacitor C114 (560 mmf, 100 WVDC) DEC Part Number 10-00025. This change increases the delay of fast MSYN in the Processor from 75 ns to 225 ns (Figure 4-6).

Once installed, the KT11-D option is ready to be checked out, using the diagnostic programs supplied with the option.

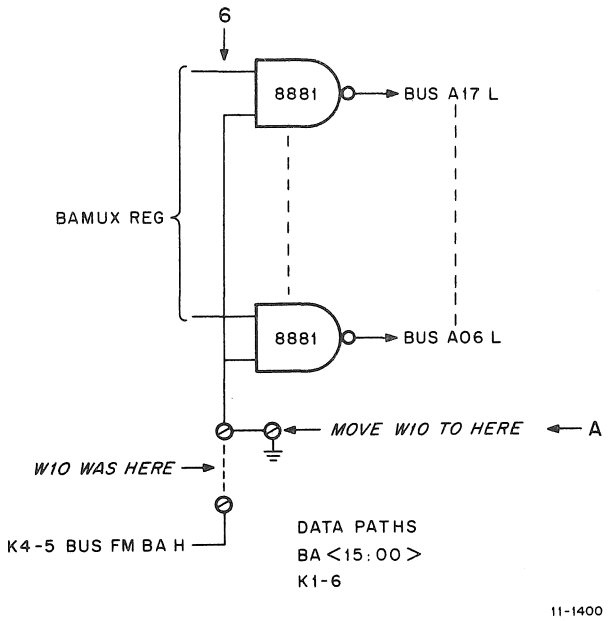


Figure 4-1 KD11-A Wiring Change No. 1

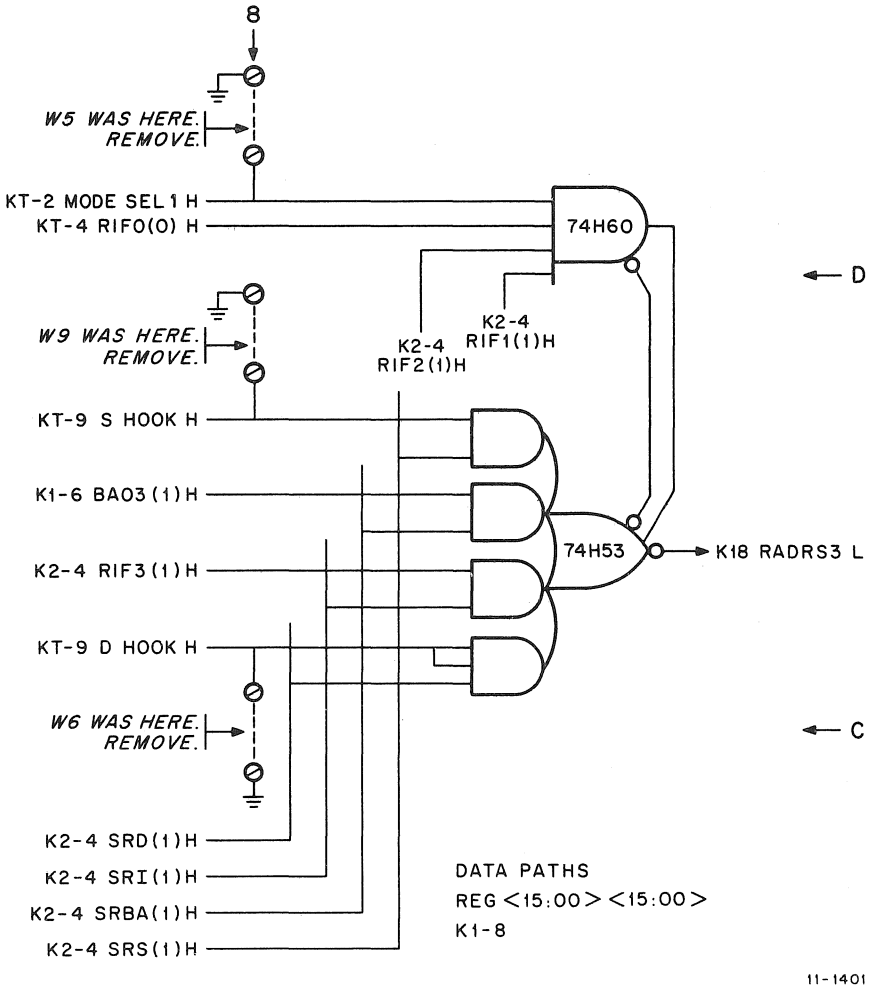


Figure 4-2 KD11-A Wiring Change No. 2

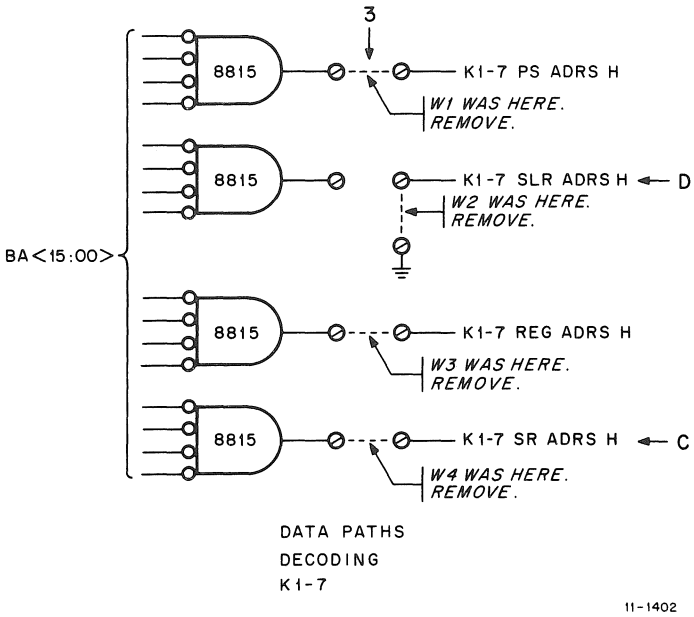


Figure 4-3 KD11-A Wiring Change No. 3

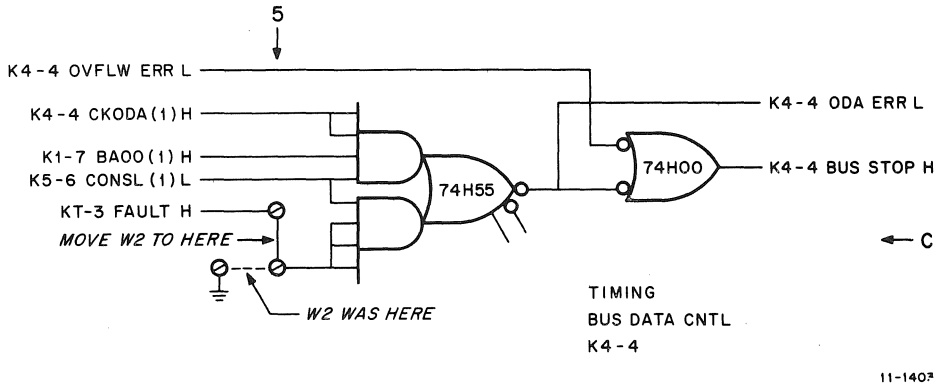


Figure 4-4 KD11-A Wiring Change No. 4

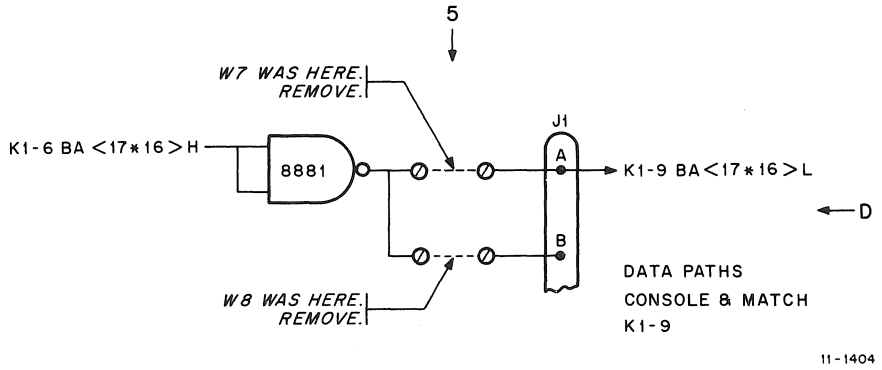


Figure 4-5 KD11-A Wiring Change No. 5

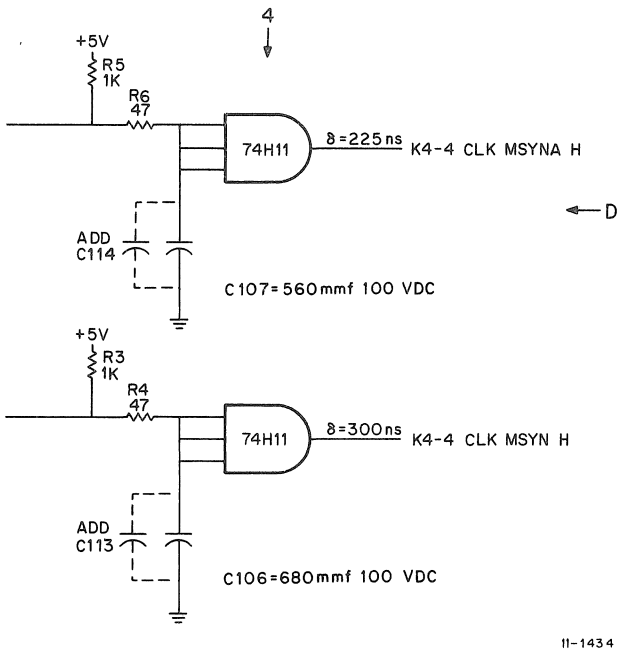


Figure 4-6 KD11-A Wiring Changes No. 6 and No. 7

Other hooks, that do not include wiring changes but do represent signals sent from the KT11-D to the KD11-A to modify its operation with the Memory Management Option, include the following functions;

a. As shown on Processor Drawing K3-2, location B-3, and in Figure 4-7, as a result of KT-3 FAULT H starting a Trap Sequence, KT-3 FAULT L going to F05M2 forces a jam to the correct flow path in the Trap Sequence on a UBF 10.

b. As shown on Processor Drawing K3-5, location C-4, and in Figure 4-8, on a detection of an instruction unique to memory management, the KT11-D signals the KD11-A to recycle in the fetch flow to decode the new instruction.

c. As shown on Processor Drawing K3-6, location C-3 and in Figure 4-9, KT-2 PS15(0)H indicates User mode. This signal controls the restricted use of a reset in User mode and the KT11-D creates the KT INSTR L signal to recycle the Reset Instruction as a NOP Instruction.

d. As shown on Processor Drawing K4-4, location D-6 and in Figure 4-10, KT-2 PS15(0)H (when LOW) is used to disable stack overflow detection in User mode.

e. As shown on Processor Drawing K4-4, location D-3 and in Figure 4-11, KT-6 NO MSYN L is created by the KT11-D on an internal access and will disable BUS MSYN to the Bus.

f. As shown on Processor Drawing K5-2, location C-6 and in Figure 4-12, KT-2 INH PS CLK L disables the clocking of CLK PS (07:T) in User mode.

g. As shown on Processor Drawing K5-5, location B-2 and in Figure 4-13, the signal KT-9 MFP SMO L is a signal that chooses the correct destination stack address on a MFP R6 instruction.

h. As shown on Processor Drawing K5-7, location C-3 and in Figure 4-14, the signal KT-9 RELOCATE ENB L enables the VIRTUAL lamp on the Console. KT-9 PS15 L is used to enable the USER lamp on the Console. Signals KT-9 SR16 L and KT-9 SR17 L are used to enable the BA 16 and BA 17 lamps on the Console.

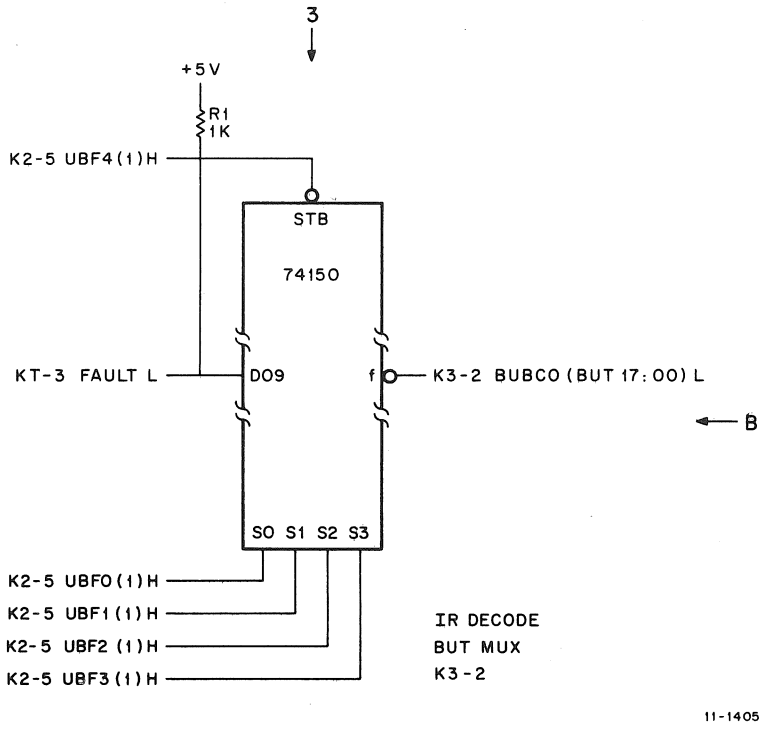


Figure 4-7 KT-3 Fault H Hook In KD11-A

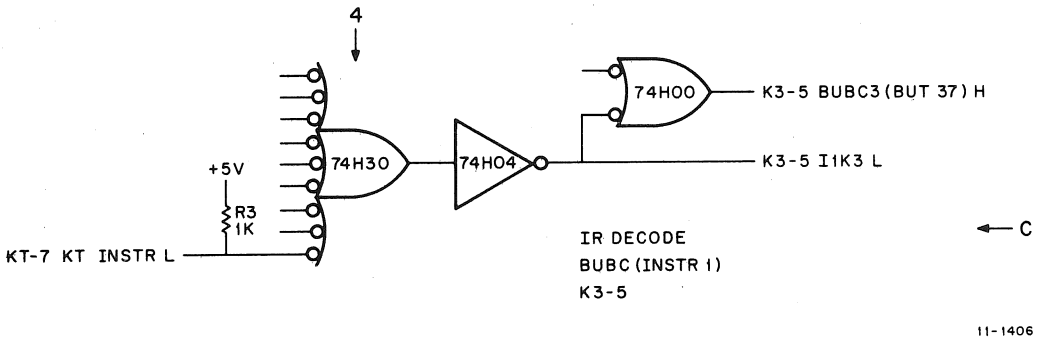


Figure 4-8 KT-7 KT INSTR L Hook In KD11-A

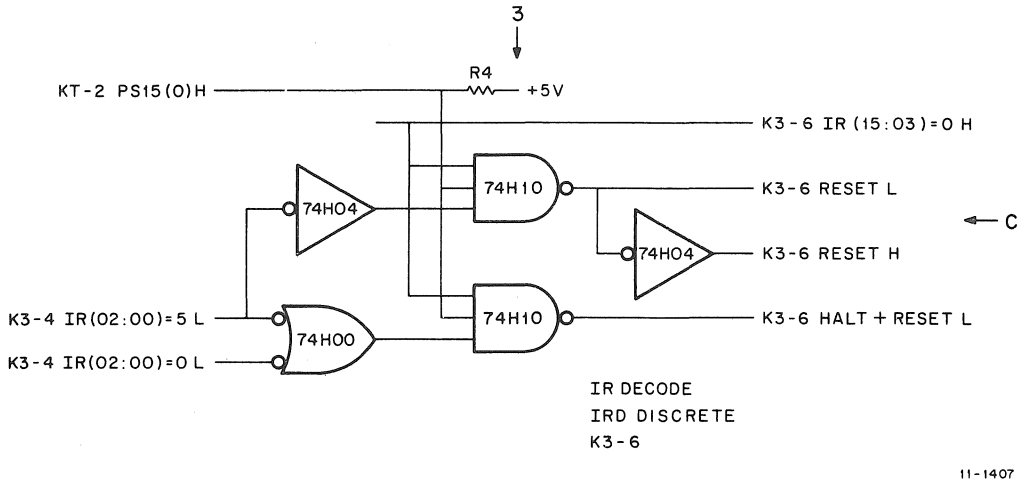


Figure 4-9 KT-2 PS15(0)H Hook In KD11-A

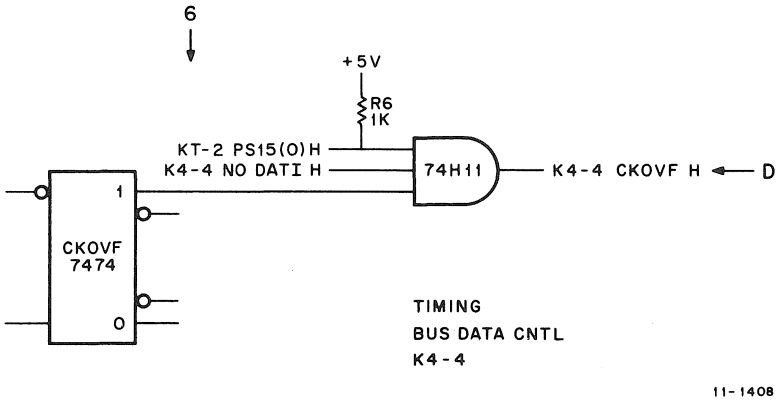


Figure 4-10 KT-2 PS15(0)L Hook In KD11-A

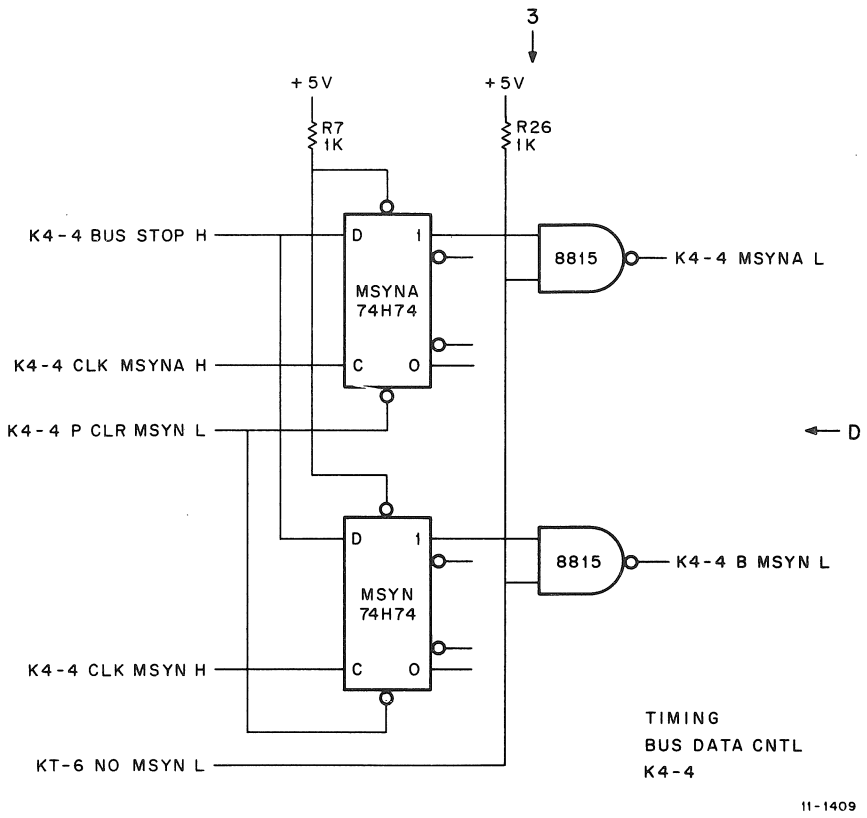


Figure 4-11 KT-6 No MSYN L Hook in KD11-A

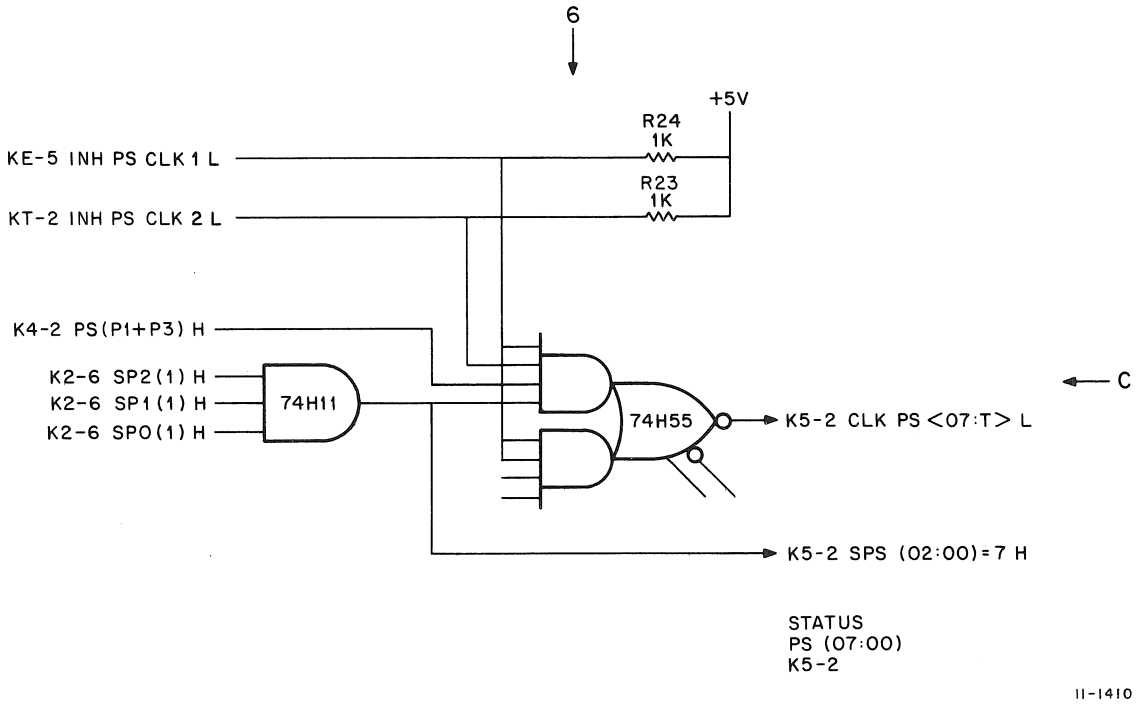


Figure 4-12 KT-2 INH PS CLK 2 L Hook in KD11-A

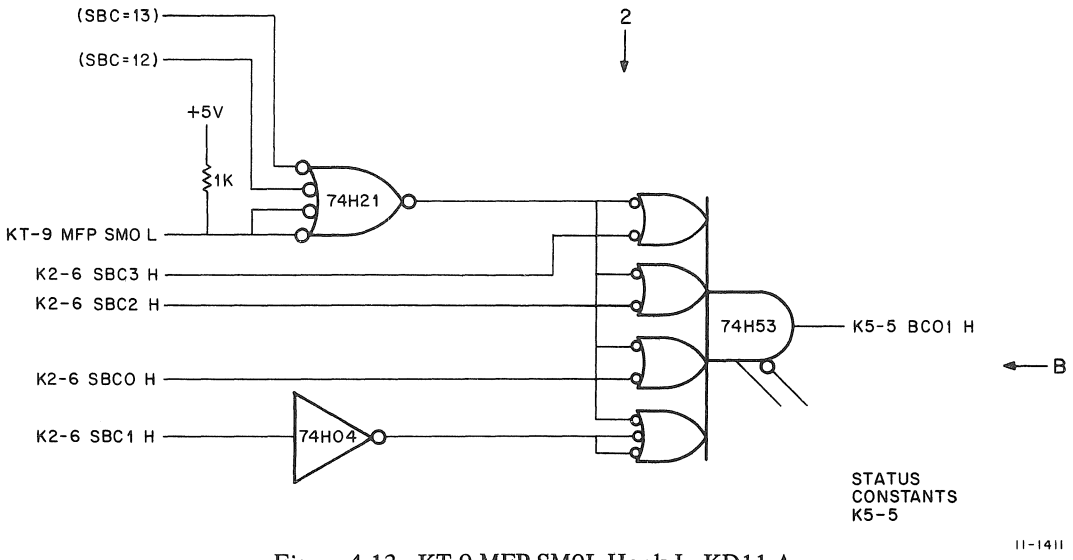


Figure 4-13 KT-9 MFP SM0L Hook In KD11-A

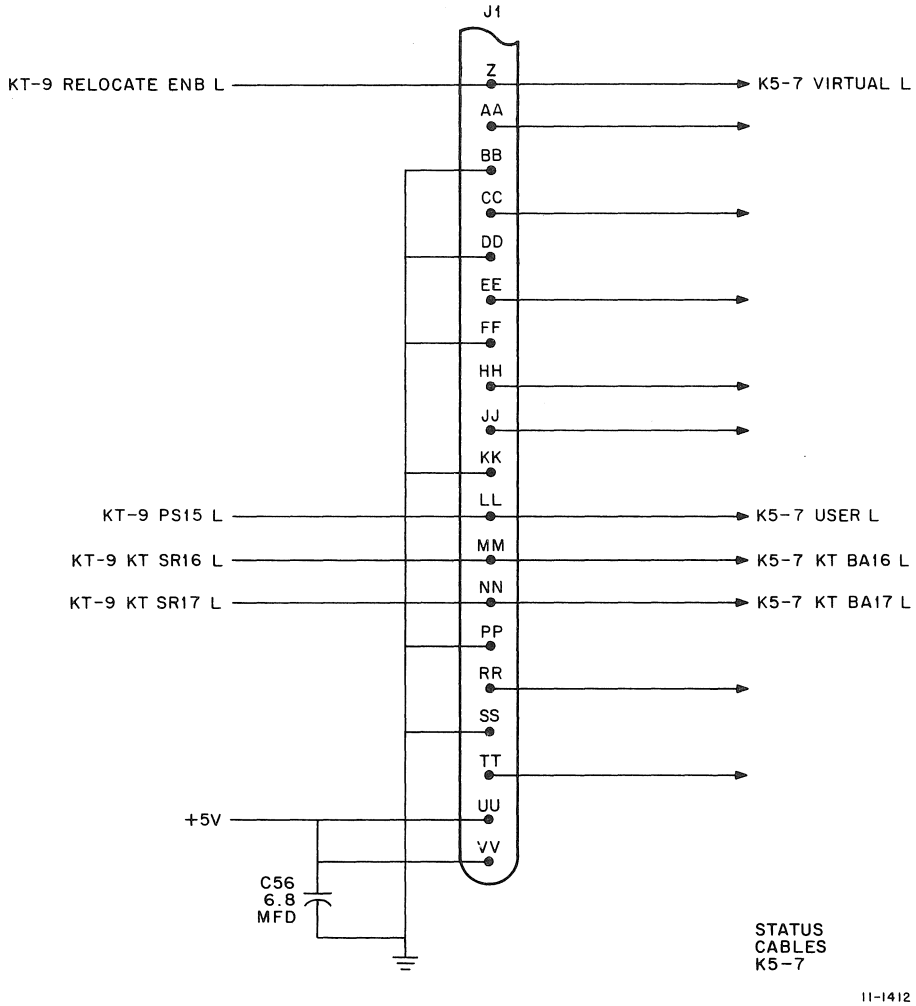


Figure 4-14 Console MM Enable Hooks In KD11-A

4.2 MAINTENANCE

The design, construction, and implementation of the M7236 module that makes up the KT11-D Memory Management Unit option is similar to those used in the KD11-A Central Processor and other options. Maintenance procedures for the entire system are described in the *PDP-11/40 System Manual,* Chapter 7. There are no special maintenance procedures for the KT11-D option.

4.2.1 Diagnostic Programs

The *PDP-11/40 System Manual* includes a list of the KT11-D diagnostic programs. These programs are part of a complete package of basic processor and option diagnostics. The sequence of running the diagnostics is set up to completely test the KD11-A Central Processor Unit before attempting to run KT11-D diagnostic programs, thus eliminating the KD11-A as a possible cause of a memory management failure.

The MAINDEC (maintenance descriptions) for each diagnostic program indicates how the program is to be loaded and run. The program listing indicates the functional logic that is being tested by each routine. The diagnostic programs are written along functional lines to test and exercise all of the KT11-D logic.

4.2.2 Troubleshooting Test Procedures

The KM11 Maintenance Console provides the user with a means of manually operating the system and monitoring status during maintenance operations.

The maintenance module is a W130/W131 board containing four switches and 28 indicators that monitor various signals within the processor. When an indicator is lit, it means that the associated logic level is high. An overlay can be attached to the module to indicate which signals are being monitored. This overlay is necessary because the module is designed as a general-purpose device and can be used, without modification other than using different overlays, in many PDP-11 devices. The specific functions monitored by the module depend on the logic signals wired to the device receptacle that receives the module.

The module is used for monitoring operation of the KT11-D Memory Management Option by the addition of the KT11-D overlay (Figure 4-15). In this application, the module is inserted into processor slot E1 and the 16 indicators on the left of the overlay are used. Note that none of the switches are operational when the module is used for this purpose. The functions monitored by the indicators are listed in Table 4-1.

NOTE

The functions described in Table 4-1 indicate the general purpose of the indicator. At times, a single indicator may indicate any number of functions, depending on the current state of the processor and/or option. Therefore, to use the maintenance module properly, the flow diagrams should be followed to determine exactly what the light is indicating at that specific time.

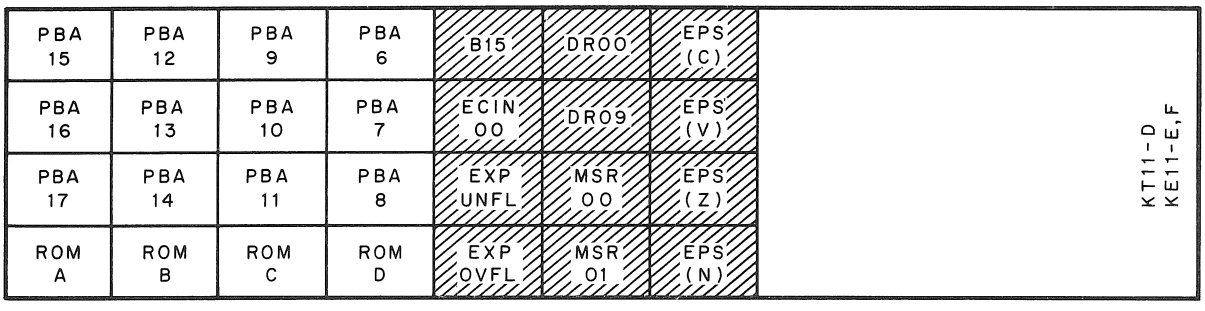


Figure 4-15 KT11, Maintenance Console Overlay

Table 4-1
Maintenance Module Indicators

Indicator	Indication (when lit)	Print Showing Signal Origin
PBA 6 through PBA 15	Indicates a logic 1 in the associated bit of the physical bus address. Note that the physical bus address is the address from the KT11-D and may be different than the address in the Bus Address Register of the processor.	KT-4
ROM A, ROM B	These two lights form a pattern to indicate the appropriate mode and the space to be used on a memory access. The pattern is listed below. A 0 indicates the light is off; a 1 indicates it is lit. **ROM A** **ROM B** 0 0 current mode 0 1 temporary mode 1 0 MTPI/D, previous mode or not MTPI/D, current mode 1 1 MFPI/D, previous mode or not MFPI/D, current mode	KT-2
ROM C	Indicates presence of ROM bit C which is used to enable clocking of PS (15:14) current mode into PS (13:12 previous mode for future controlled access and clocking of T (15:14).	KT-2
ROM D	Indicates presence of ROM bit D which is placed in conjunction with the final bus cycle of the KD11 instructions for relocation in destination mode only.	KT-2

4.2.3 Maintenance Sample Program

The following program is intended to aid in verifying relocation capabilities and accessabilities of core banks, utilizing a simple program that can be loaded from the Console Switch Register.

Assuming the program will reside in bank 0 (although it can be in any of the existing virtual memory banks 0–6), the KPAR and KPDR of the virtual memory bank of the program can be manually set up as follows:

1. Map the KPAR0 with a relocation constant x by depositing into KPAR0 (772340) = x, where x is the block number of the physical location of the relocated program code (Figure 4-16).

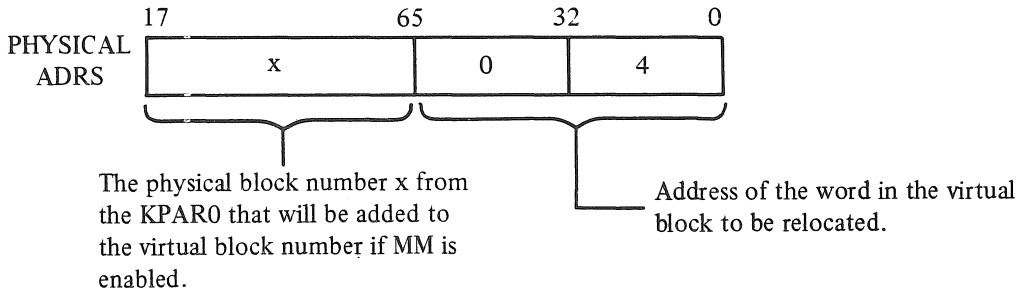


Figure 4-16 Physical Address

2. Describe how to use this physical core location by mapping its KPDR0 with a contents y, where y is the restrictions, if any, of the relocated blocks. In this case the physical location will be read/write, expand direction upwards, and full page length. Therefore, deposit into KPDR0 (772300) = 77406.

3. Map KPAR7 to enable access to the processor registers or KT registers when MM is enabled by depositing the following:

   KPAR7 (772356) = 7600
   KPDR7 (772316) = 77406

With the above KT11-D register set up, the program can be deposited in core as follows:

```
200 / 005237 ; INC@#SR0      ;Enable MM

202 / 177572

204 / 00000 ; HALT           ;If we don't relocate, halt.

x+204 / 00777 ; BR           ;Program executes a branch
                             ;on self if relocation is
                             ;successful.
```

Where x is shown in Table 4-2 that lists the values of x that could be deposited in KPAR0 to enable access to any physical core bank.

Table 4-2
Values of x

Bank	Starting Address	x	Bank	Starting Address	x
1st 8K	000000	0000	9th 8K	400000	4000
2nd 8K	040000	0400	10th 8K	440000	4400
3rd 8K	100000	1000	11th 8K	500000	5000
4th 8K	140000	1400	12th 8K	540000	5400
5th 8K	200000	2000	13th 8K	600000	6000
6th 8K	240000	2400	14th 8K	640000	6400
7th 8K	300000	3000	15th 8K	700000	7000
8th 8K	340000	3400	16th 8K	740000	7400

The code at x+204 does not have to be a BR. It can be any code that indicates execution in that respective bank.

READER'S COMMENTS

KT11-D MEMORY MANAGEMENT
OPTION MANUAL
DEC-11-HKTDA-B-D

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