DR11-B/DA11-B manual

DEC-11-HDRBA-D-D

DR11-B/DA11-B manual

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CHAPTER 1
INTRODUCTION

1.1 GENERAL DESCRIPTION

The DR11-B is a general-purpose, direct memory access (DMA) interface to the PDP-11 Unibus (see Figure 1-1). The DR11-B operates directly to or from memory, moving data between the Unibus and the user device, rather than using program controlled data transfers.

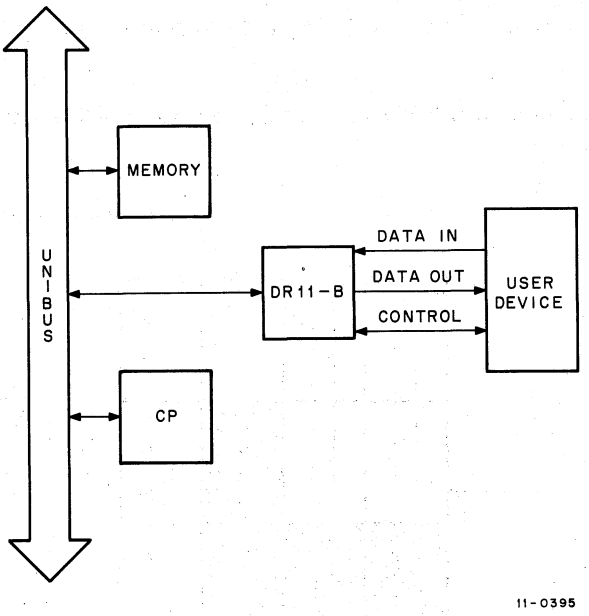


Figure 1-1 System Block Diagram

The interface consists of four registers: command and status, word count, bus address, and data. Operation is initialized under program control by:

a. Loading word count with the 2's complement of the number of transfers;

b. Specifying the initial memory or bus address where the block transfer is to begin;

c. Loading the command/status register with function bits.

The user device recognizes these function bits and responds by setting up the control inputs. If the user device requests data from memory or a Unibus device, the DR11-B performs a Unibus data transfer (DATI) and loads its data register with the information held at the referenced bus address. The outputs of this register are available to the user device. *This output data is buffered in a 16-bit flip-flop register.*

If the user device requests data to be written into memory, the DR11-B performs a Unibus data transfer (DATO), moving data from the user device to the referenced bus address. *This input data from the user is not buffered and must be held as levels for the duration of the Unibus transfer.* Transfers normally continue at a user defined rate until the specified number of words is transferred.

The user is given a number of control lines, which provide flexible operation. Burst modes, read-modify-restore operations, and byte addressing are possible with the control structure.

1.2 PHYSICAL DESCRIPTION

The DR11-B is packaged in one standard system unit for convenient incorporation into a PDP-11 System (see Figure 1-2). An M920 Unibus Jumper Module is supplied with the unit. Power is applied to the logic through the power harness already provided in the BA11 Mounting Box. Current requirements are 3.3A at +5V.

Connections to the user device are made through two M957 Split-Lug Cable Boards, which are supplied with the unit. Alternatively, an M920 can be used to jumper all user signals to an adjacent BB11 Blank Mounting Panel, which can package some (or all) of the device logic. Refer to Appendix B for more detailed information.

NOTE
The additional M920 and the BB11 are not supplied with the unit.

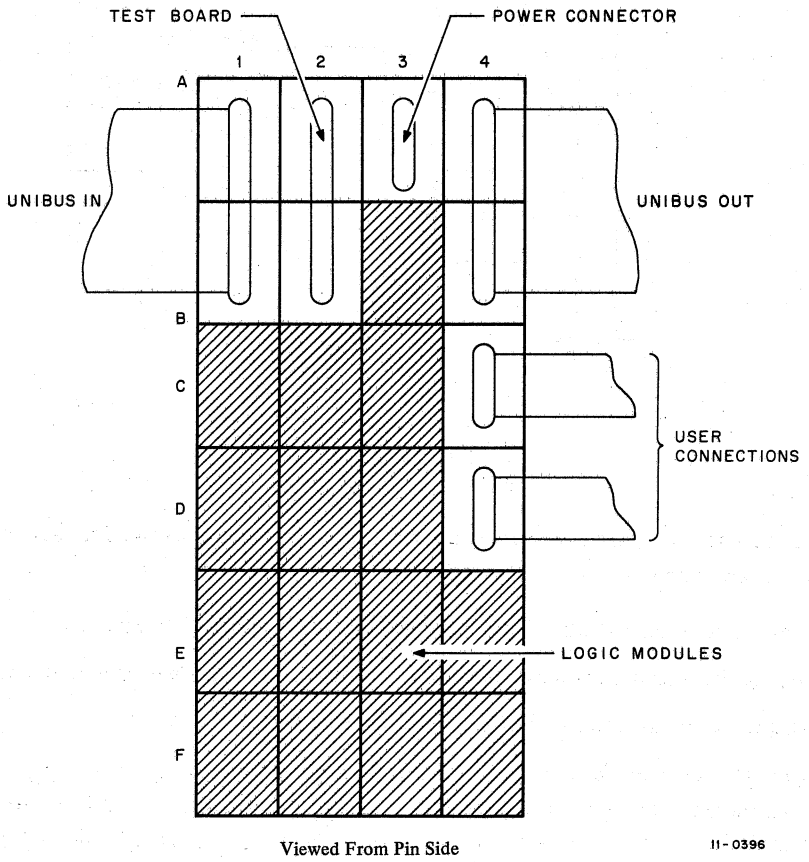


Figure 1-2 DR11-B System Unit

CHAPTER 2
SOFTWARE INTERFACE

This chapter presents a detailed description of the four DR11-B registers (see Figure 2-1). These registers are assigned bus addresses and can be read or loaded (with the exceptions noted) using any instruction that refers to their addresses. *INIT* refers to the initialization signal produced on power up, power down, caused by the RESET instruction or by the START switch on the console. *R/W* stands for read/write. Note that the INIT signal is held asserted internal to the DR11-B whenever an interlock error occurs (M968 test board is not in slots AB02 for normal operation or in CD04 for maintenance mode).

2.1 STATUS and COMMAND REGISTER (DRST)

The DRST is used to give commands to the user device and to provide status indicators of the DR11-B control and the user device (refer to Table 2-1).

2.2 WORD COUNT REGISTER (DRWC)

DRWC is a 16-bit R/W register. It is initially loaded with the 2's complement of the number of transfers to be made and normally increments up toward zero after each bus cycle. Incrementation can be inhibited by the user device; refer to the WC INC ENB user signal. When overflow occurs (all 1s to all 0s), the READY bit of DRST is set and the bus cycle stops.

NOTE

DRWC is a word register; do not use byte instructions when loading this register.

DRWC is cleared by INIT.

2.3 BUS ADDRESS REGISTER (DRBA)

DRBA is a 15-bit R/W register. Bit 0, corresponding to address line A00, is provided by the user device. Along with XBA16 and 17 in DRST, DRBA is used to specify BUS A <17:01> in direct bus access. The register is normally incremented (+2) after each bus cycle, advancing the address to the next sequential word location on the bus. If DRBA (corresponding to A <15:01>) overflows (all 1s to all 0s), the ERROR bit in DRST is set. This error condition (BAOF) is cleared by loading DRBA or INIT. Incrementation can be inhibited by the user device (refer to the BA INC ENB user signal). With this control signal and A00 provided externally, DRBA can be used to address sequential bytes.

NOTE

This is a word register; do not use byte instructions when loading this register.

DRBA is cleared by INIT.

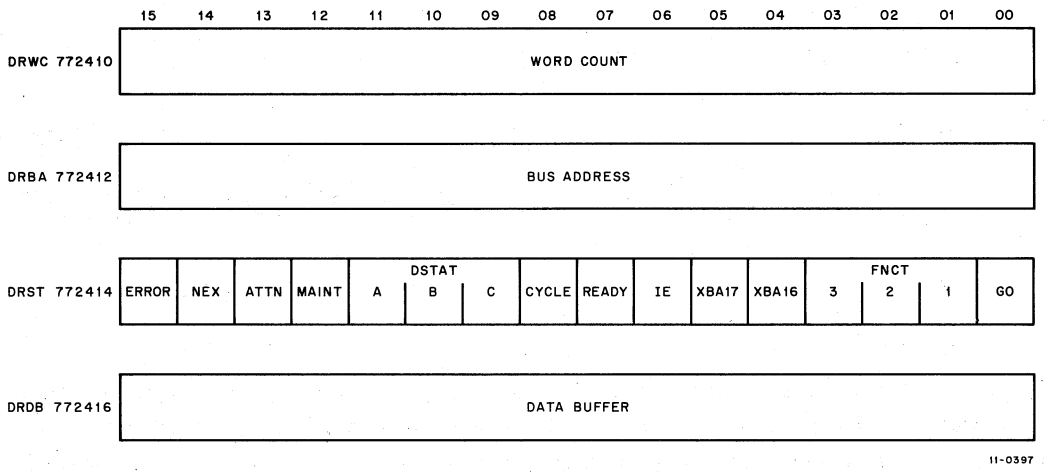


Figure 2-1 Register Assignments

2.4 DATA BUFFER REGISTER (DRDB)

The DRDB serves two functions:

a. **A 16-bit write only register.** The outputs of this register are available to the user device (refer to the DATA OUT signals). The register, which can be loaded under program control, is also used to buffer information when data is being transferred from the Unibus to the user device (when DR11-B does a DATI cycle).

b. **A 16-bit read only register.** Information to be read is provided by the user device on the DATA IN signal lines. These lines are not buffered and must be held until either read under program control or transferred directly to memory (DATO bus cycle).

NOTE

DRDB is a word register; do not use byte instructions when loading this register.

DRDB is cleared by INIT.

Table 2-1
DRST Bit Description

Bit	Name	Meaning and Operation
15	ERROR (read only)	1. Indicates an error condition: a. Either NEX (BIT 14), b. ATTN (BIT 13), c. interlock error (test board is not in slot AB02 or CD04); d. or bus address overflow (BAOF:DRBA incremented from all 1's to all 0's.) 2. Sets READY (BIT 7) and causes interrupt if IE (BIT 6) is set. 3. Cleared by removing all four possible error conditions: a. Interlock error is removed by inserting test board in CD04 for diagnostic tests or in AB02 for normal operation; b. Bus address overflow is cleared by loading DRBA; c. NEX is cleared by loading bit 14 with a zero; d. ATTN is cleared by user device.
14	NEX (read/write 0)	1. Non-existent memory indicates that as Unibus master, the DR11-B did not receive a SSYN response 20 μs after asserting MSYN. 2. Sets ERROR. 3. Cleared by INIT or loading with a 0; cannot be loaded with a 1.
13	ATTN (read only)	1. Attention bit reads the state of the ATTN user signal. 2. Sets ERROR. (Used for device initiated interrupt.) 3. Set and cleared by user control only.
12	MAINT (read/write)	1. Maintenance bit used with diagnostic programs. 2. Cleared by INIT. (Refer to Chapter 5.)
11 10 09	DSTAT A DSTAT B DSTAT C } (read only)	1. Device status bits that read the state of the DSTAT A, B, and C user signals. (Not tied to interrupt.) 2. Set and cleared by user control only.
08	CYCLE (read/write)	1. CYCLE is used to prime bus cycles. 2. If set when GO is issued, an immediate bus cycle occurs. 3. Cleared when bus cycle begins; cleared by INIT. 4. CAUTION: Do not write into this bit when the DR11-B is not READY and is under user device control.

Table 2-1 (Cont)
DRST Bit Description

Bit	Name	Meaning and Operation
07	READY (read only)	1. Indicates that the DR11-B is able to accept a new command. 2. Set by INIT or ERROR; set on word count overflow. 3. Cleared by GO. 4. Causes interrupt if bit 6 is set. Forces DR11-B to release control of the Unibus and prevents further DMA cycles.
06	IE (read/write)	1. Enables interrupt to occur when either ERROR or READY is set. 2. Cleared by INIT.
05 04	XBA17 XBA16 } (read/write)	1. Extended bus address bits 17 and 16, in conjunction with DRBA, specify A<17:01> for direct memory transfers. 2. Cleared by INIT. 3. XBA17 & 16 do *not* increment when DRBA overflows; instead ERROR is set.
03 02 01	FNCT3 FNCT2 FNCT1 } (read/write)	1. Three bits made available to the user device. User defined. 2. Cleared by INIT.
00	GO (write only)	1. Causes a pulse to be sent to the user device indicating a command has been issued. 2. Clears READY and allows DMA operation. 3. Always reads as a zero.

2.5 ADDRESS AND VECTOR ASSIGNMENTS

The direct bus access level and priority interrupt level are as follows:

Direct bus access level: NPR (hardwired)

Priority interrupt level: BR5 (hardwired) (Refer to appendices for changes.)

Table 2-2
Address Assignments

No. of DR11-Bs	Register Addresses	Vector Address
1st DR11-B	772410-772417	124
2nd DR11-B	772430-772437	*
3rd DR11-B	772450-772457	*
4th DR11-B	772470-772477	*
*Assigned by user.		

Register addresses are selected by jumpers on the M7219. The vector address is selected by jumpers on the M7821.

NOTE

In earlier models where an M7219 prior to etch revision D is used, address bit 3 must be a 1 (logical restriction). Also where an M7820 is used rather than the M7281, Vector Address bit 2 is hardwired to a 1.

CHAPTER 3
USER INPUT/OUTPUT SIGNALS

This chapter describes the signals made available to the user device to control the operation of the DR11-B. Section 3.1 defines the user input/outout signals; Section 3.2 details the timing considerations and restrictions on the use of the signals.

3.1 SIGNAL LIST

Tables 3-1 and 3-2 list the signals available to the user device. Input loading refers to the number of TTL unit loads the input signal must drive. A unit load is defined as:

$2.4V \leqslant$ Input high voltage $\leqslant 5.0V$ @ 40 μA

$0.0V \leqslant$ Input low voltage $\leqslant 0.4$ @ -1.6 mA

where current flow is defined positive into the driven gate. All inputs, except 3 inputs, represent 1 unit load. This provides a noise margin of 0.4V minimum.

All output signals are driven with 74H40 gates. These are active pull-up TTL circuits capable of sourcing 1.5 mA at an output high voltage of greater than 2.4V and sinking 60 mA at an output low voltage of less than 0.4V. This represents a fanout of 37 standard TTL unit loads.

Table 3-1
User Input Signals

Name	No. of Signals	Loading	Description
DAT15 IN– DAT00 IN	16	1 each	Data input from user device. The levels presented on these lines can be examined by reading the DRDB register (e.g., MOV DRDB, R0) and are transferred directly to memory when the DR11-B performs a DATO bus cycle. Levels are: +3V = logical 1; ground = logical 0.
C1 CONTROL C0 CONTROL	1 1	5 1	These two control signals specify the type of Unibus cycle the DR11-B is to perform. They correspond logically with the Unibus signals C1 and C0. Levels are: +3V = logical 1; ground = logical 0. Note: polarities on Unibus are inverted.

C1 Control	C0 Control		Cycle Performed
0	0	DATI	To transfer data from Unibus to the user device.
0	1	DATIP	
1	0	DATO	To transfer data from user device to Unibus.
1	1	DATOB	

Table 3-1 (Cont)
User Input Signals

Name	No. of Signals	Loading	Description
			Refer to the *Unibus Interface Manual* for a full description of these cycles.
CYCLE REQUEST A,B	2	1 each	The logical OR of these two signals is used to set the CYCLE flip-flop in the DR11-B. CYCLE initiates the sequence of requesting bus use and triggering the Unibus cycle after the DR11-B obtains control of the bus. Either of these two inputs should be pulsed positive for 100 ns minimum duration to initiate a bus transfer sequence. CYCLE sets on the +3V-to-ground transition of the input.
WC INC ENB	1	1	Word Count Increment Enable. In most operations this signal is wired to a logical 1 (+3V) source, allowing the DRWC register to count each bus cycle performed by the DR11-B. However, in read-modify-write sequences, for example, incrementation would be disabled for the DATIP cycle and enabled for the subsequent DATO.
BA INC ENB	1	1	Bus Address Increment Enable. In most operations, this signal is tied to a logical 1 (+3V) source, allowing the DRBA register to step after each bus cycle. However, in read-modify-restore operations, for example, incrementation must be inhibited for the DATIP cycle and enabled for the subsequent DATO.
A00	1	2	Bus Address Bit 00. The signal level applied on this line reads as bit 0 of the DRBA register and specifies address line 00 when the DR11-B performs a Unibus cycle. Levels are: +3V = logical 1; ground = logical 0. A00 is usually tied to ground, forcing sequential word addressing; but it can be controlled externally to allow for byte addressing.
DSTAT A,B,C	3	1 each	Device Status Bits A,B,C. The signal *levels* applied to these lines appear as bits 11, 10 and 09 of DRST. Levels are: +3V = logical 1; ground = logical 0.
ATTN	1	2	Attention. The signal *level* applied to this line appears as bit 13 of DRST. A logical 1 (+3V) forces an error condition in the DR11-B and stops further bus cycles. An interrupt occurs if IE is set. Must be grounded if not used.
SINGLE CYCLE	1	1	This signal is normally tied to a logical 1 (+3V) source, and after each bus cycle performed by the DR11-B, bus mastership is released. When the next cycle is to be performed, the DR11-B makes another request for bus use. This procedure allows other devices on the Unibus to interleave cycles with the DR11-B. If burst modes or read-modify-write operations are to be performed, then bus mastership must be held for the complete string of cycles. In this case, SINGLE CYCLE is held at a logical 0 (ground). At a logical 0, this signal requests bus control and holds it until the signal returns to logical 1 or until READY is set by either an error condition or word count overflow. In the burst mode, a bus cycle is not triggered until CYCLE is set by either CYCLE REQUEST A or B.

Table 3-2
User Output Signals

Name	No. of Signals	Description
DATI5 OUT–DAT00 OUT	16	Data output to user device. These signals represent the contents of the DRDB register, which is loaded either under program control (e.g., MOV R0, DRDB) or when the DR11-B performs a DATI cycle. Levels are: +3V = logical 1; ground = logical 0. All lines cleared to 0 by INIT.
INITIALIZE	1	This line is true (+3V) whenever the Unibus is initialized, which occurs on power up, power down, console start, RESET instruction, or interlock error.
FNCT 3,2,1	3	These 3 lines are derived from the function bits in DRST (bits 3, 2, 1) and are used to specify device operation. Levels are: +3V = logical 1, ground = logical 0. Clear by INIT.
READY	1	This signal is derived from the READY bit in DRST (bit 7). This signal is true (+3V) after INIT; it becomes false (ground) when the GO bit is loaded, indicating that a command has been given; and it becomes true again when word count overflows or an error condition develops.
BUSY	1	BUSY indicates that a bus sequence is in progress. It is true (+3V) when CYCLE is set and becomes false (ground) when the bus cycle is complete. BUSY follows the CYCLE bit when the CYCLE bit is under program control.
END CYCLE	1	This pulse is a $\simeq$ 100-ns positive pulse that indicates that the bus cycle is complete.
GO	1	This pulse is a $\simeq$ 200-ns positive pulse that results from the setting of the GO bit in DRST. Indicates that a new operation is to be performed.

3.2 TIMING CONSIDERATIONS

The negation of READY, as well as the GO signal, indicates to the user device that the GO bit has been set and the FNCT bits now indicate a valid command. The user device responds by providing the following set of signals: DATA <15:00> IN, C1 CONTROL, C0 CONTROL, WC INC ENB, and A00. This set of signals must be established 100 ns prior to the negative transition of CYCLE REQUEST A or B and held for the duration of the bus cycle. The trailing edge of CYCLE REQUEST A or B causes BUSY to become true, indicating that DR11-B is requesting bus use or in the process of executing a bus cycle. At the completion of the bus cycle, the END CYCLE pulse is generated, and BUSY goes false. For the duration of BUSY (from CYCLE REQUEST to END CYCLE), the above set of signals must be held. No new cycle request should be made while BUSY is set.

The BA INC ENB user signal need not be established until BUSY becomes true; but, unlike WC INC ENB, it must be held for the duration of the bus cycle plus the duration of the END CYCLE pulse.

As soon as SINGLE CYCLE becomes false (and READY is clear), the DR11-B requests control of the Unibus. However, a bus cycle is not initiated until CYCLE is set. If CYCLE is clear, the assertion of SINGLE CYCLE will release control of the bus; if CYCLE is set when SINGLE CYCLE is asserted, bus control will not be released

until the bus cycle is complete. Thus, in order to ensure that bus control is held until a bus cycle is requested, SINGLE CYCLE must be held false until CYCLE (and consequently BUSY) is set. Refer to Section 6.3.

No timing is involved with DSTAT A, B, or C, because they are simply levels that appear as bits in DRST. The effect of ATTN is different, because it forces an error condition, which, in turn, forces the DR11-B to release control of the bus. Thus, in read-modify-write sequence (DATIP-DATO), ATTN must not be asserted to report a possible error condition until the DATO cycle is complete. Also, ATTN must not be asserted during the interval between the assertion of CYCLE REQUEST A or B and the receiving of the END CYCLE pulse. If ATTN is asserted during this interval, Unibus timing is violated because of the uncontrolled release of Unibus control.

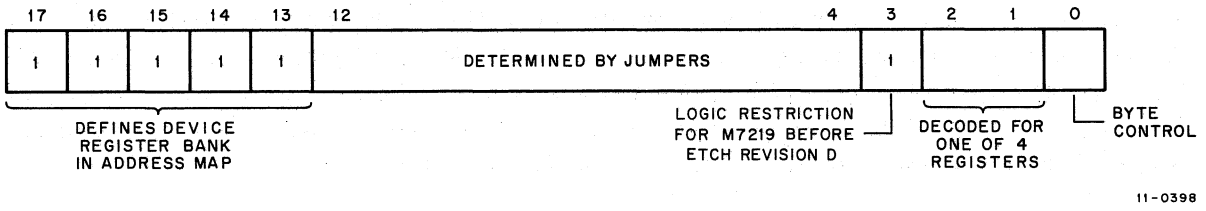
Note that the CYCLE bit in DRST can be loaded under program control. Setting this bit causes BUSY to become true, but a bus cycle is inhibited until READY is cleared by setting GO. This sequence allows the DR11-B to be *primed*, that is, no CYCLE REQUEST A or B is necessary for the first bus cycle.

CHAPTER 4
THEORY OF OPERATION

The DR11-B basically comprises four interface registers that are controlled in two modes: slave or master. The slave mode is essentially the program controlled mode when the DR11-B, as a slave to the processor, responds to its addresses on the Unibus. The master mode is when the DR11-B gains control of the Unibus, via the NPR request line, and (as bus master) performs a data transfer operation. (See Figure 4-1.) For DR11-B signal naming conventions, refer to Chapter 7.

4.1 SLAVE MODE RESPONSE

The four DR11-B registers are assigned unique addresses on the PDP-11 Unibus (refer to Section 2.5). These addresses are in the following form:



Address lines <17:13> must be 1s; A<12:04> are determined by jumpers on the M7219 module; A03 must be a 1 on M7219 modules before etch revision D; A<02:01> are decoded to select one of the four registers; and A00 is used by byte addressing.

The circuit that performs the address decoding is shown on Dwg. D-CS-M7219-0-1 Sheet 1 and is essentially the same as that used on the M105 Address Selector. When the proper address is decoded and BUS MSYN is received, ADRS ENB becomes true (low). After a small RC time delay (approximately 150 ns), BUS SSYN is asserted, indicating the response of the DR11-B to the master's request.

BUS C1, BUS C0, and BUS A00 are received and decoded to produce:

a. IN (DR11-B responds by putting the data of the selected register onto the bus.)

b. OUT LOW (DR11-B loads low byte of selected register.)

c. OUT HIGH (DR11-B loads high byte of the selected register.)

Note that both OUT LOW and OUT HIGH are true when a word is being loaded into a DR11-B register.

When data is to be loaded into one of the four DR11-B registers, the following list of signals is used:

Signal Name	Logical Equation
BUS TO DRWC	ADRS ENB * BA03 * -BA02 * -BA01 * OUT LOW * -BSSYN
BUS TO DRBA	ADRS ENB * BA03 * -BA02 * BA01 * OUT LOW * -BSSYN
BUS TO DRST	ADRS ENB * BA02 * -BA01 * OUT LOW
BUS TO DRST+1	ADRS ENB * BA02 * -BA01 * OUT HIGH * -BSSYN
BUS TO DRDB	DATA WAIT + ADRS ENB * BA02 * BA01 * -IN * -BSSYN

Note that DRWC, DRBA, and DRDB are defined to be word registers; thus, BUS TO DRWC, BUS TO DRBA, and BUS TO DRDB are used to load a full 16-bit register regardless of whether a byte operation was specified. However, either byte of DRST can be selectively loaded.

The purpose of -BSSYN in the above list of signals is to cause a short pulse to appear on the loading signal. A loading signal becomes true when BUS MSYN is received (MSYN qualifies ADRS ENB). BUS MSYN, after a short delay, triggers the BUS SSYN response, which, in turn, produces BSSYN and turns the loading signal off.

BUS TO DRWC (derived on Dwg. D-CS-M7219-0-1 Sheet 1) is applied to the word count register (see Sheet 3). BUS TO DRBA (produced on Dwg. D-CS-M7219-0-1 Sheet 1) is applied to the bus address register (see Sheet 4). BUS TO DRST and BUS TO DRST+1 (produced on Dwg. D-BS-DR11-B-0-3) are used on Dwgs. D-BS-DR11-B-03 and 02. BUS TO DRDB (produced on Dwg. D-BS-DR11-B-0-3) is used to load the data registers, as shown on Dwg. D-BS-DR11-B-04.

When data is requested from the selected register (ADRS ENB*IN*BA03), the MUX ENB signal is produced. This signal is applied to the data multiplexer circuits shown on Dwg. D-CS-M7219-0-1 Sheet 2. As a function of the BA01 and BA02 signals (derived from address lines 01 and 02) one of four possible data sources (that is, one of the four DR11-B registers) is selected, and this information is applied to the Unibus data lines. Also shown on Dwg. D-CS-M7219-0-1 Sheet 2 are the 16 receivers for the Unibus data lines.

4.2 MASTER-MODE

The previous section describes how the DR11-B responds as a slave on the Unibus. This section describes how the DR11-B becomes bus master and either performs a data transfer operation or an interrupt operation.

4.2.1 Interrupt Operation

As defined in the programming specification, the DR11-B interrupts, via its vector address, when either an error or ready condition exists and interrupt is enabled. On Dwg. D-BS-DR11-B-02, Master Control B of the M7821 is dedicated to the interrupt function. Master Control B is triggered when the AND condition at its input is met. The following two conditions are necessary:

a. INT ENB must be present (Bit 6 of the DRST register must be loaded with a 1).

b. READY (Bit 7 of the DRST) must be set.

An error condition sets READY; therefore, READY is sufficient to qualify an interrupt for either READY or ERROR.

When the input condition on the M7821 is met, a bus request is made, and after the bus grant is received and other UNIBUS conditions are met, the DR11-B becomes bus master and MASTER B becomes true (low).

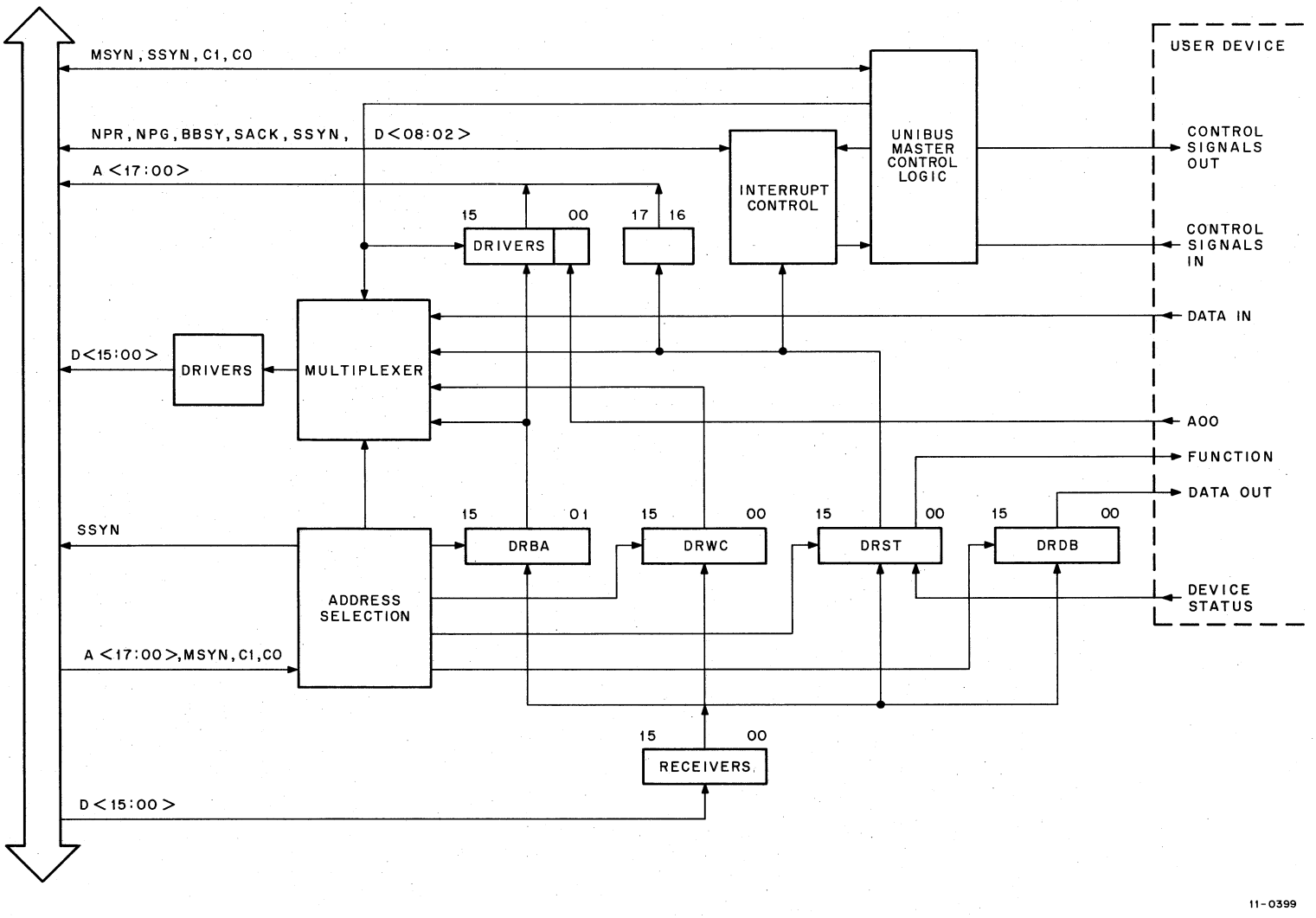
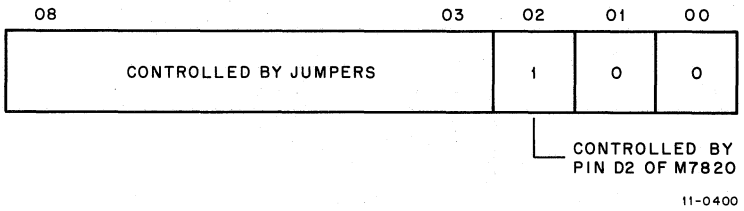


Figure 4-1 DR11-B Block Diagram

MASTER B is fed directly into the INTR CONTROL section of the M7821, where a vector address is placed on the bus and BUS INTR is asserted. The address placed on the bus is of the following form:



Vector address bits (08:03) are determined by jumpers on the M7821 (a jumper "in" indicates a 1 for the M7821 and for the M7820 in earlier models a jumper "in" indicates a 0). Bit 02 of the address is controlled by pin D2 of the M7821; because this input is at a high level whenever the interrupt operation is occurring, bit 02 of the vector address will be a 1. Pin D2 can be rewired and a ground applied to it, thereby causing bit 02 of the address to be a 0.

Note that the interrupting condition is momentarily (for $\simeq$ 100 ns) disabled by a one shot on the M796 when GO (bit 0 of the DRST) is issued or an error condition develops. This situation allows the transition of the ERROR bit to cause an interrupt even though the READY bit is set and allows an immediate interrupt to occur if any error condition remains present when GO is issued.

4.2.2 Direct Memory Access

The second reason for the DR11-B to gain bus control is to perform a data transfer operation. In this case data is transferred directly between the user device and a device (usually memory) on the Unibus. The DR11-B can perform all four of the Unibus data transfer operations: DATI, DATIP, DATO, DATOB. (Refer to the *Unibus Interface Manual* for a full description of these cycles.)

After the program has set up the bus address and word count registers, it issues a GO pulse by loading bit 0 of the status register. GO clears the DR11-B READY bit, and DMA operation can begin. The following paragraphs describe the bus transfer sequence. (Refer to Dwg. D-BS-DR11-B-02 and the timing diagrams, Figures 4-2 and 4-3.

Action is initiated on the trailing edge of a positive pulse applied to CYCLE REQUEST A or B. This action sets the CYCLE bit, which, in turn, sets BUSY. BUSY is applied to the MASTER CONTROL A section of the M7821. (Assume that SINGLE CYCLE is asserted high.) If READY is clear (indicating that a GO pulse was given, no error conditions exist, and word count has not overflowed), then a request is made on the NPR line. When the NPR bus grant is received and other Unibus conditions are met, the DR11-B becomes bus master and asserts BUS BBSY, and MASTER A becomes true (low).

The logical condition CYCLE (1)*MASTER A*-BSSYN produces the START signal internal to the M796 Unibus Master Control. (-BSSYN ensures that the previous bus cycle is complete.) START triggers a Unibus cycle. BUS C1 and BUS C0 are asserted as a function of C1 and C0 CONTROL (user controlled). Simultaneously, the ADRS TO BUS signal becomes true, which is applied to the set of bus drivers shown on Dwg.D-CS-M7219-0-1 Sheet 4. These drivers place the contents of DRBA and XBA17 and XBA16 onto the Unibus Address lines A <17:00>.

If an output operation was specified by C1 and C0 CONTROL (either DATO or DATOB), then the DATA TO BUS signal is activated. DATA TO BUS is applied on Dwg. D-CS-M7219-0-1 Sheet 1 to produce MUX ENB, and on Sheet 2 to force the multiplexer to select DAT <15:00> IN (user supplied data) as the source of information to be placed on the Unibus data lines. If an input operation was specified (DATI or DATIP), then DATA TO BUS is not active.

Next, after a 150-ns delay, BUS MSYN is asserted. The selected slave recognizes its address; either accepts the data on the Unibus or places the requested data on the Unibus; and then asserts BUS SSYN. BUS SSYN is received by the DR11-B and BSSYN is applied to the M796. If the master is expecting data from the slave (DATI or DATIP), the DATA WAIT signal is produced. This signal is a 75-ns pulse that allows for data deskewing. DATA WAIT produces BUS TO DRDB on Dwg. D-BS-DR11-B-03, which, in turn, is applied to the DRDB register on Dwg. D-BS-DR11-B-04. The data is strobed into the DRDB register by the trailing edge of the DATA WAIT pulse. The output lines from the DRDB register are DAT <15:00> OUT, which assume the new data values within the gate delay times of this trailing edge.

After the data is strobed into the DRDB register in the case of a DATI or DATIP (or as soon as BUS SSYN is received in the case of a DATO or DATOB), BUS MSYN is negated. After 75 ns, ADRS TO BUS, BUS C1, BUS C0 and DATA TO BUS are negated. At this point, the bus cycle is complete, and the END CYCLE pulse is produced.

END CYCLE is used to clear the BUSY flip-flop and is also applied on Dwg. D-CS-M7219-0-1 Sheet 4 to increment the DRBA (if enabled). BUSY clearing removes the enabling condition to the M7821, and the DR11-B relinquishes bus control.

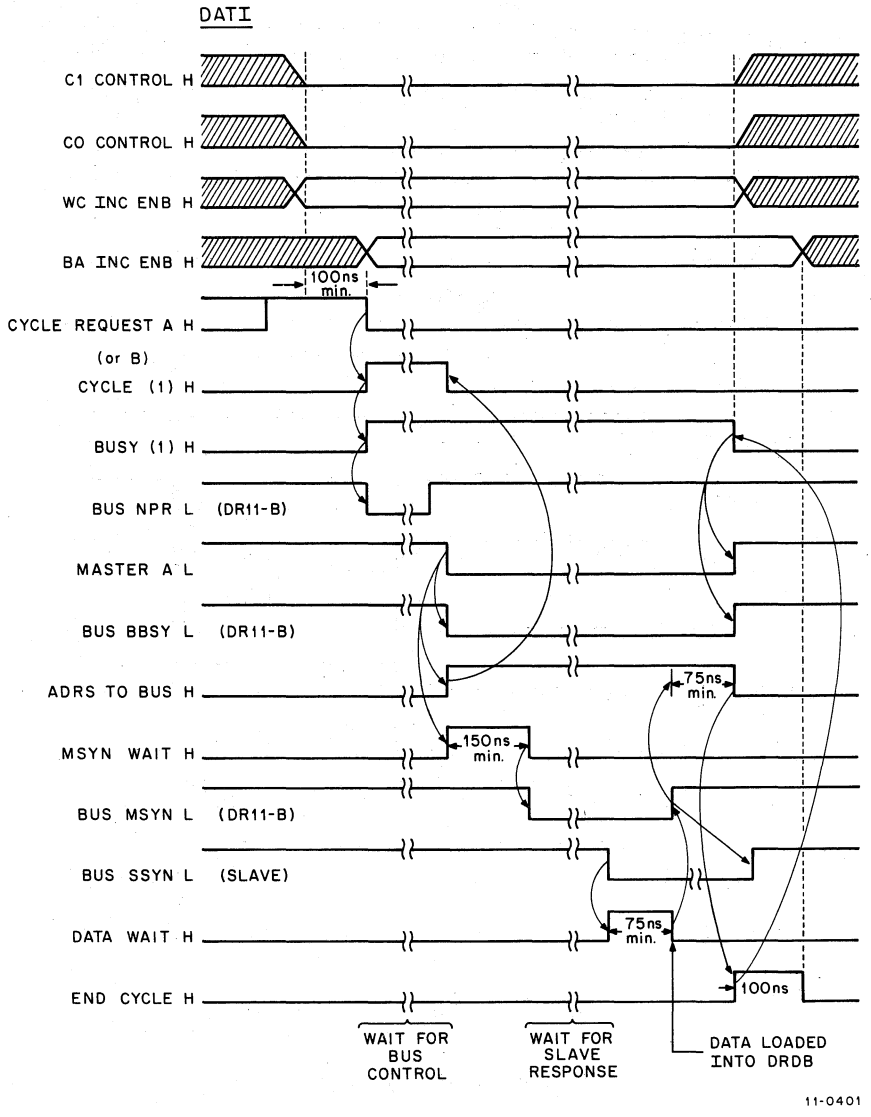


Figure 4-2 DATI

The entire sequence is repeated for each subsequent data cycle until word count overflow. The ADRS TO BUS signal on Dwg. D-BS-DR11-B-02 is used to produce WC INC on Dwg. D-BS-DR11-B-03, which, in turn, is applied to DRWC on D-CS-M7219-0-1 Sheet 3. The actual incrementing of the register occurs on the positive going (trailing edge) of the low pulse applied to counter. The WCOF signal on Dwg. D-CS-M7219-0-1 Sheet 3 follows the WC INC signal when all bits of the counter are 1s. Thus, WCOF is true (low) during the last bus cycle; when the cycle is complete, DRWC increments to all 0s, and WCOF becomes false (high). This positive transition of WCOF is applied to the clock of the READY flip-flop on Dwg. D-BS-DR11-B-03, which sets the flip-flop. Thus, for the last bus cycle, the READY flip-flop sets when ADRS TO BUS goes false, which is approximately the same time that the END CYCLE pulse is generated.

The setting of READY can be tested under program control or can initiate an interrupt sequence if INT ENB (bit 6) is set. READY set disqualifies the AND input condition on the M7821; as a result, further NPR cycles are inhibited.

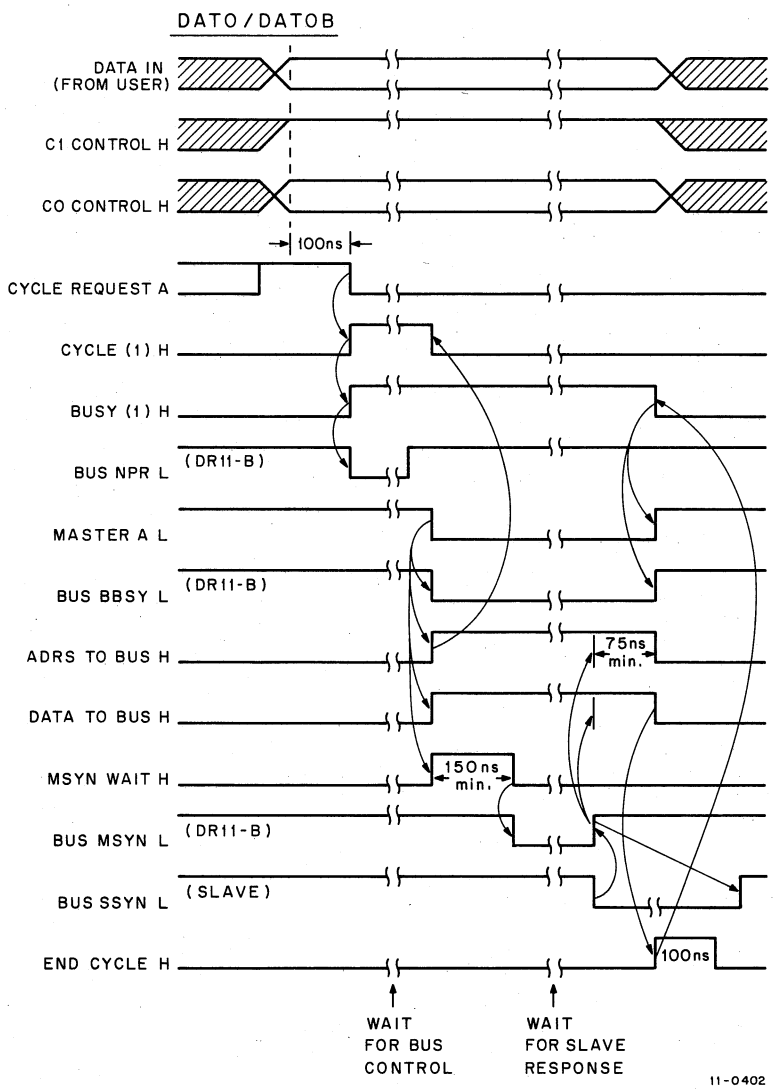


Figure 4-3 DATO/DATOB

4.3 MISCELLANEOUS LOGIC DESCRIPTION

SINGLE CYCLE is ORed with BUSY on Dwg. D-BS-DR11-B-02 to request the Unibus for a data transfer. Thus, when SINGLE CYCLE is false (low), an NPR request is immediately made (as long as READY is clear). However, a bus cycle is not triggered until CYCLE is set, via CYCLE REQUEST A or B. SINGLE CYCLE must be held low until BUSY is set to ensure that bus control is not relinquished before the cycle starts. Refer to Section 6.3.

The CYCLE bit on Dwg. D-BS-DR11-B-02 can be controlled by either the software (it reads and loads as bit 8 of the DRST register) or the user device (set by CYCLE REQUEST A or B). If CYCLE is set when the GO pulse is issued, the DR11-B immediately performs a bus operation. This feature is useful when it is necessary to *prime* the control for the first transfer.

BAOF on Dwg. D-CS-M7219-0-1 indicates that the DRBA register overflowed (from all 1s to all 0s). Contrary to other Digital Equipment Corporation device interfaces, this overflow condition does not ripple through to increment the extended bus address bits 16 and 17. Instead BAOF is used on Dwg. D-BS-DR11-B-03 to force an error condition. BAOF is cleared by reloading the DRBA register or by INIT.

NEX (bit 14 of the DRST register) sets if, after asserting BUS MSYN, the DR11-B did not receive a BUS SSYN reply within 20 μs. This situation indicates that either no slave is assigned to the address being used or the slave at that address has malfunctioned. The setting of NEX terminates the bus cycle and forces the DR11-B to release bus control. The DRWC and DRBA registers are incremented if enabled to do so. NEX is cleared by loading bit 14 of the DRST register with a 0.

NO LOCK on Dwg. D-BS-DR11-B-03 is used to ensure that the DR11-B Test Board is inserted into the proper slot. When in AB02, the ground applied to pin A02U2 is jumpered to pin A02T2, via the test board, and thus pulls to ground the NO LOCK signal. Similarly, when in slots CD04 (during diagnostic testing), a ground is applied to C04R1, which pulls NO LOCK to ground. Unless there is a ground applied to NO LOCK, the signal will be pulled high and INIT will become true. INIT forces READY set and ERROR asserted, and operation of the DR11-B is inhibited.

CHAPTER 5
MAINTENANCE

5.1 MAINTENANCE MODE

Checkout and testing of the DR11-B is accomplished by using the MAINT bit in DRST in conjunction with a special maintenance module (M968) to simulate the user device. Rather than using the M957s to cable user signals out to the device, the maintenance module plugs into the two slots normally occupied by the cable boards and jumpers the output signals to the input signals. Thus, the M968 is simply an etch board with electrical shorts between selected pins. The connections are listed below:

Output Signals	Input Signals
DATA OUT	DATA IN
FNCT 3	DSTAT A, SINGLE CYCLE
FNCT 2	DSTAT B
FNCT 1	DSTAT C, C1 CONTROL
gnd	C0 CONTROL
gnd	ATTN
+3V	BA INC ENB
+3V	WC INC ENB
gnd	A00
END CYCLE	CYCLE REQUEST A
GO	CYCLE REQUEST B

Dwg. D-IC-DR11-B-07 is a diagram of these interconnections.

The MAINT bit in DRST has one special effect: it allows the FNCT bits to function as a 3-bit counter that increments following each bus cycle performed by the DR11-B.

Because FNCT 1 is tied to C1 CONTROL and because FNCT 1 toggles after each bus cycle, the DR11-B in maintenance mode does alternating DATIs and DATOs on sequential bus addresses. Thus, if FNCT 1 is initially cleared and DRBA is loaded with an address, a DATI is performed on location *X*. After the DATI, FNCT 1 is set, and the subsequent bus cycle is a DATO to location *X*+2; next, a DATI from *X*+4; followed by a DATO to *X*+6; etc., until word count overflows.

The series of bus cycles is initiated by setting the GO bit. The GO output signal is tied to the CYCLE REQUEST B input Subsequent cycles are self-sustaining, because END CYCLE is tied to CYCLE REQUEST A.

If the MAINT bit is not set, then the FNCT bits do not increment and either a string of DATIs or DATOs results.

FNCT 3 is tied to SINGLE CYCLE. Thus, when FNCT 3 is clear, a burst mode is entered in which the DR11-B does consecutive bus cycles without releasing bus control until word count overflows. If MAINT is set, FNCT 3 toggles every fourth bus cycle and a string of four cycles in burst mode alternates with a series of four single cycles.

Testing the DR11-B in maintenance mode is not an absolutely complete logic test. The following are not exercised:

1. Inhibiting DRWC and DRBA from incrementing.
2. C0 CONTROL, A00, and ATTN input signals.
3. READY, BUSY, and INITIALIZE output signals.

When not being used in maintenance mode, the M968 Test Module must be inserted in slots AB02, otherwise an interlock error occurs, forcing the ERROR bit to set and inhibiting DR11-B operation.

CHAPTER 6
EXAMPLES

6.1 BASIC INTERFACE

Figure 6-1 illustrates a typical user device interface, consisting of a basic control section and a data assembly register. In this example, FNCT1 is defined as a READ/WRITE control bit. Because FNCT1 is tied to C1 CONTROL, FNCT 1 set (read operation) causes the DR11-B to perform a DATO operation transferring data present on DAT <15:00> IN to memory. FNCT clear (write operation) causes a DATI operation, and data read from memory is made available on DAT <15:00> OUT.

Operation is initiated by the GO pulse. The user device determines whether a read or write operation is requested by FNCT1. When data is ready for transfer to the Unibus or data is required from the Unibus, a high-to-low transition on DATA REQUEST activates CYCLE REQUEST. (Note that CYCLE REQUEST need not necessarily be a pulsed signal.) When the requested cycle is completed, the END CYCLE pulse is received by the control, which normally would initiate the next data cycle. ATTN reports a possible user device error condition.

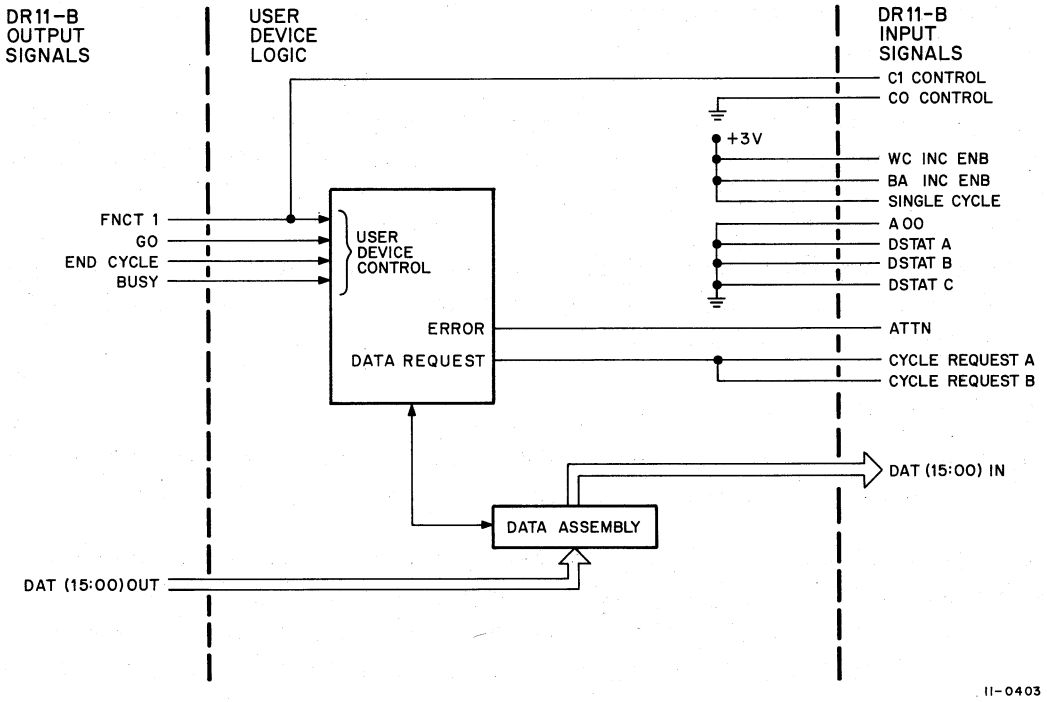


Figure 6-1 Basic Interface

6.2 BYTE ADDRESSING

Figure 6-2 represents a typical circuit necessary to control A00 and BA INC ENB to address sequential byte addresses. The flip-flop is initially cleared (even byte) and incrementation is disabled. After the first cycle is complete, the flip-flop toggles and the odd byte is addressed. During this cycle, however, incrementation is enabled, allowing the address to advance to the even byte of the next word location.

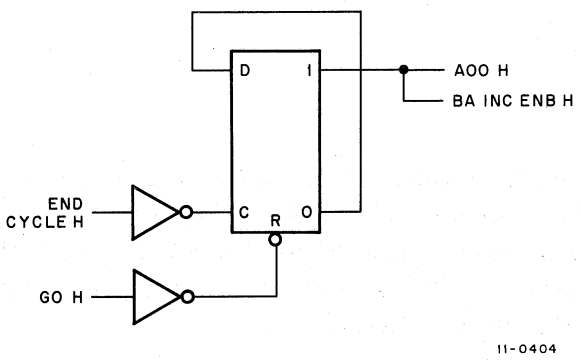


Figure 6-2 Byte Addressing

During byte operations to memory (DATOB), it is necessary for the user to justify the byte data on either DAT <15:08> IN (odd byte) or DAT <07:00> IN (even byte). However, no harm is done if the byte of data is placed on both bytes of the data lines simultaneously, because the addressed slave is responsible for retrieving the significant byte of data.

When requesting data from memory or any other device on the Unibus (either a DATI or DATIP operation), a full word of data is always transferred. Thus, both odd and even bytes of the requested word are made available to the user device on DAT <15:08> OUT and DAT <07:00> OUT, respectively.

Figure 6-3 is operationally similar to Figure 6-2 in that it controls A00 and BA INC ENB for byte addressing. However, in addition, this circuit provides the ability to initially specify A00. When GO is issued, bit 00 of the data register is loaded into the flip-flop.

6.3 DATIP-DATO SEQUENCE

The DATIP-DATO sequence is used to modify a location in memory. Figure 6-4 represents the control necessary to perform a byte-swapping modification. The timing is shown for one cycle in Figure 6-5.

Operation is initiated by the GO pulse that clears flip-flops A and B. GO is tied to CYCLE REQUEST A; because C1 CONTROL = 0 and C0 CONTROL = 1, a DATIP cycle is initiated. During this first cycle, word count and bus address are inhibited from incrementing. When the DATIP cycle is complete, END CYCLE toggles the A flip-flop and initiates a DATO cycle, via CYCLE REQUEST B. Note that C1 and C0 CONTROL and WC INC ENB are altered by the leading edge of END CYCLE, whereas the subsequent cycle is not initiated until the trailing edge of END CYCLE. This delay is a required set-up time for these signals.

SINGLE CYCLE is initially false; consequently, at the end of the DATIP cycle, bus control is not released. SINGLE CYCLE is held false until BUSY sets for the DATO cycle, at which point it becomes true. Thus, at the end of the DATO cycle, bus control is released. Note that SINGLE CYCLE must be held false until BUSY sets, ensuring that the DR11-B does not release Unibus control before the DATO cycle is initiated.

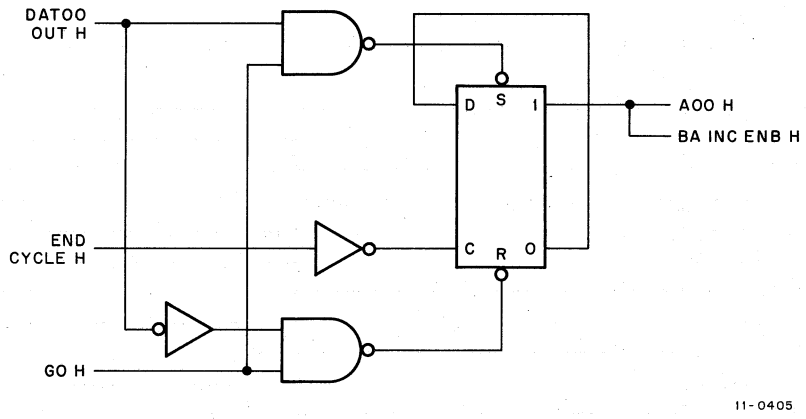


Figure 6-3 Byte Addressing, Additional Function
(Compare with Figure 6-2.)

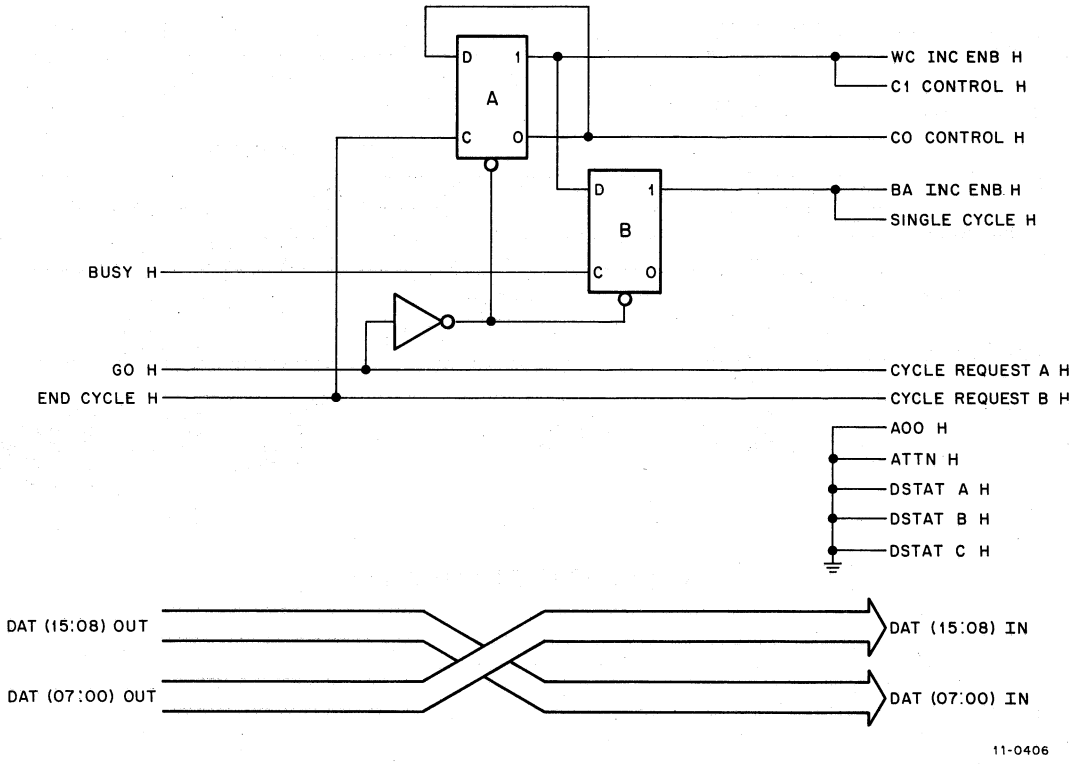


Figure 6-4 Swap Byte by DATIP-DATO

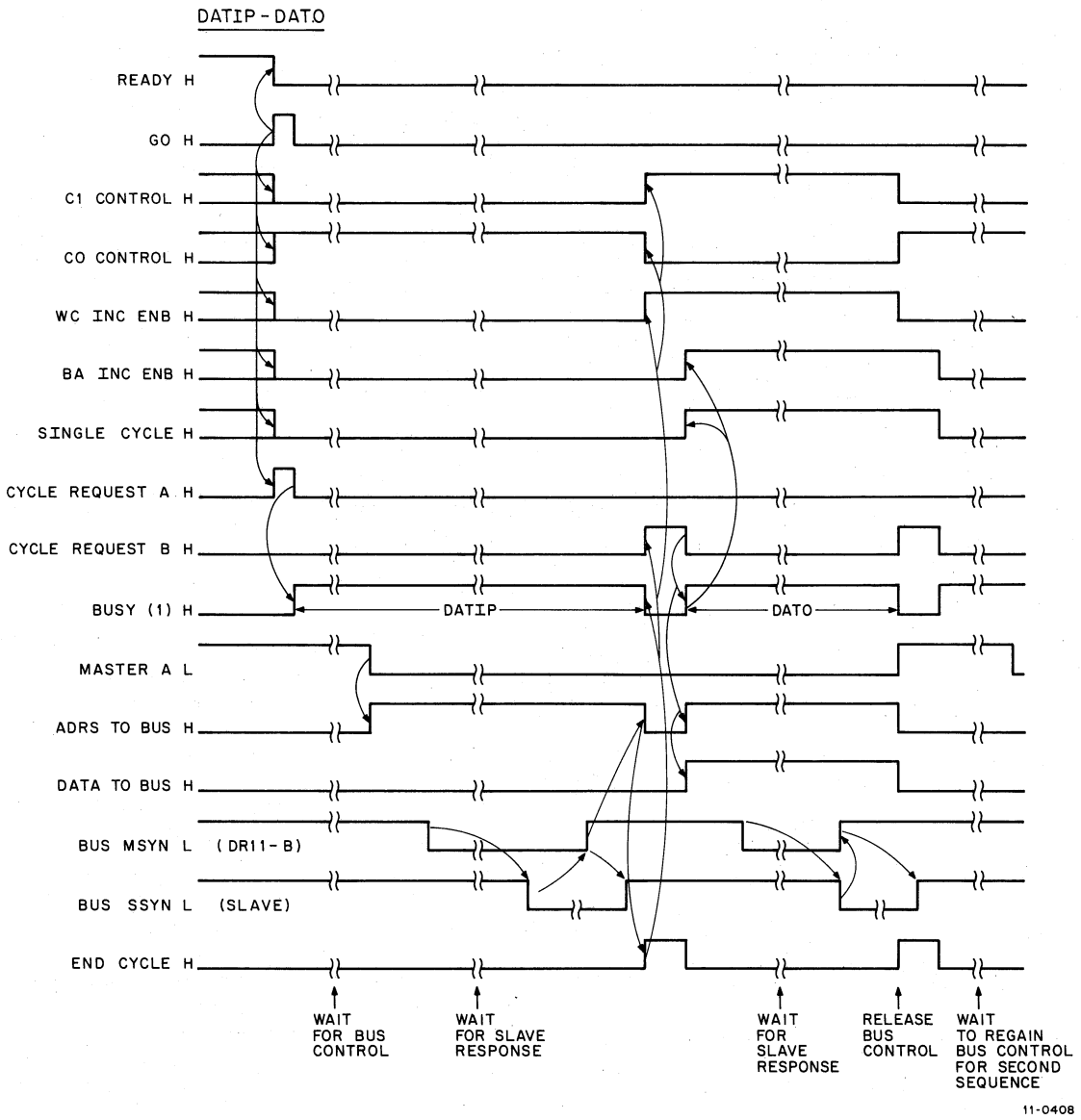


Figure 6-5 DATIP-DATO Timing

CHAPTER 7
ENGINEERING DRAWING SET

7.1 SIGNAL NOMENCLATURE CONVENTIONS

7.1.1 Print Set

The DR11-B print set is contained in a separate volume, *DR11-B Engineering Drawings.* Signal names in the DR11-B print set are in the basic form:

SOURCE	ASSERTION	SIGNAL NAME	POLARITY

SOURCE indicates the drawing number of the print where the signal originates. The drawing number of a print is located in the lower right-hand corner of the print title block.

ASSERTION is either blank or a NOT sign (–). A blank indicates that reference is being made to the asserted state (the true state) of the signal; a NOT sign indicates reference to the negated state (the false state) of the signal.

SIGNAL NAME is the name proper of the signal.

POLARITY is either *H* or *L* to indicate the voltage level of the signal; *H* means +3V; *L* means ground. For example the signal

D1-2 -BD14 L

originates on the Sheet 2 of Drawing D1 (Dwg. D-CS-M7219-0-1) and is read "*when BD14 is not true, this signal is at ground.*" Note that this signal is electrically equivalent to D1-2 BD14 H; however, it is being used in a different logical sense.

Signals originating from flip-flops do not use the NOT sign to indicate *ASSERTION*; instead, they use a 1 or 0 in parentheses following the signal name for assertion indication. For example:

D3 READY (0) L

originates on Dwg. D3 (D-BS-DR-B-03) and is read "*when the READY flip-flop is clear (holding a zero), this signal is at ground.*" Note that D3 READY (1) H and D3 READY (0) L refer to the same electrical point - the 1 side of the flip-flop. Likewise, D3 READY (0) H and D3 READY (1) L both refer electrically to the 0 side of the flip-flop.

Unibus signal lines do not carry a SOURCE indicator. These signal names represent a bidirectional wire-ORed bus; as a result, multiple sources for a particular bus signal can exist. Each Unibus signal name is prefixed with *BUS.*

7.1.2 Wire List

The alphabetical signal name listing of the backpanel wiring is included with the DR11-B drawings. Entries in the list designate the electrical connections of backpanel pins and, thus, do not indicate signal assertion. For example, -BD14 L is entered as BD14-H.

In addition to listing signal names, polarities, and pin numbers, the wire list also indicates the drawing location for a particular pin. For example, BD14 H on pin E03P1 can be found on Dwg. D3 (Dwg. D-BS-DR11-B-03). The drawing entry for BD14 H on pin C01H1 is D1-2S'3'4. This indicates that the signal appears on three prints: D1-2, D1-3 and D1-4 (Dwg. D-CS-M7219-0-1 Sheets 2, 3, and 4). In this case, the connections between the three points are made by etch runs on the module. The *S* indicates the drawing on which the signal originates. For BD14 H, the source drawing is D1-2 (Dwg. D-CS-M7219-0-1 Sheet 2).

APPENDIX A
ALTERATION OF PRIORITY INTERRUPT LEVEL

The DR11-B is factory wired to interrupt at priority level 5. Changing this level involves rewiring: 1) BR request line, 2) BG IN (bus grant) and 3) BG OUT. Note that in the following lists, the Bus Grant lines not being used must remain jumpered between Unibus In (slots AB01) and Unibus Out (slots AB04).

First, remove priority level 5:

Step	Procedure	Location		
1	Remove BUS BR5 L.	E02P1	to	B01C1
2	Remove BUS BG5 IN H.	B01B1	to	E02E1
3	Remove BUS BG5 OUT H.	E02A1	to	B04B1
4	Add BUS BG5 H.	B01B1	to	B04B1

Then, add the selected priority level, as indicated in Sections A.1 through A.3.

A.1 FOR LEVEL 4

Step	Procedure	Location		
1	Remove BUS BG4 H.	B01E2	to	B04E2
2	Add BUS BG4 IN H.	B01E2	to	E02E1
3	Add BUS BG4 OUT H.	E02A1	to	B04E2
4	Add BUS BR4 L.	E02P1	to	B01D2

A.2 FOR LEVEL 6

Step	Procedure	Location		
1	Remove BUS BG6 H.	B01A1	to	B04A1
2	Add BUS BG6 IN H.	B01A1	to	E02E1
3	Add BUS BG6 OUT H.	E02A1	to	B04A1
4	Add BUS BR6 L.	E02P1	to	A01U2

A.3 FOR LEVEL 7

Step	Procedure	Location		
1	Remove BUS BG7 H.	A01V1	to	A04V1
2	Add BUS BG7 IN H.	A01V1	to	E02E1
3	Add BUS BG7 OUT H.	E02A1	to	A04V1
4	Add BUS BR7 L.	E02P1	to	A01T2

APPENDIX B
USER DEVICE CONNECTIONS

The following describes several methods of connection between the user device and the DR11-B system unit.

B.1 M957 CABLE CONNECTOR

Two M957 Cable Connectors are supplied with the DR11-B to allow for user input/output signal connections. Pin assignments for the two connectors are shown on drawing D-IC-DR11-B-06 which is included in this manual. The connector, as shown in Figure B-1, consists of 36 split lugs to which cable wires can be soldered.

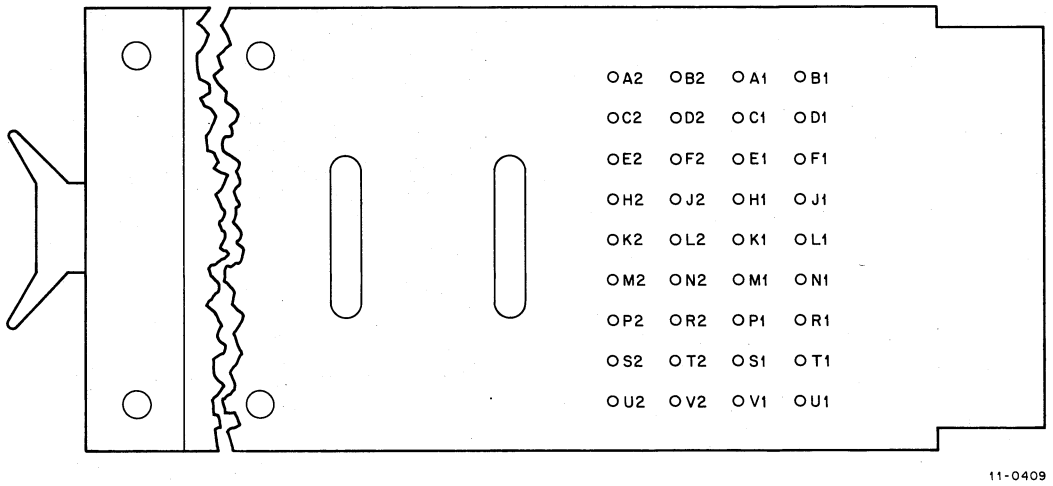


Figure B-1 M957 Cable Connector Pinning Detail

For distances above two feet, transmission line effects must be carefully considered. These effects include signal reflections (ringing) and signal cross-talk. Reflections are generated when a cable is not terminated in its characteristic impedance. Reflections on data lines are not critical if sufficient time is allowed for the reflections to settle before the data is strobed or clocked. However, on timing signal lines, reflections can be avoided or reduced by proper parallel termination at the receiving end of the line.

Cross-talk is the tendency for activity on one signal line to induce or couple an unwanted signal (noise) into adjacent lines. The effect of cross-talk is accumulative over the length of the cable and with the number of lines active at one time. An effective approach to reduce cross-talk, is to arrange signal lines into isolated groups. For

example, data signals can be cabled separately from control signals. This isolation is best implemented by use of flat, ribbon-type cable with proper signal grouping. Bundled, twisted-pair cable is not recommended because the isolation between signal groups is difficult to achieve. However, in cases where this type of cable must be used, cross-talk can be reduced by using series terminations at the transmitting end of the lines.

B.2 LOCAL LOGIC

The *user device* in some cases consists almost entirely of logic circuits; few, if any, connections are needed to the "outside world". In these special cases, rather than using the M957 Cable Connectors to provide signals from an external user device, the logic of the device can be made local, that is, internal to the mounting box of the DR11-B.

The user device signals can be jumpered to an adjacent system unit (BB11, Blank Mounting Panel) by a M920 Connector module, as shown below:

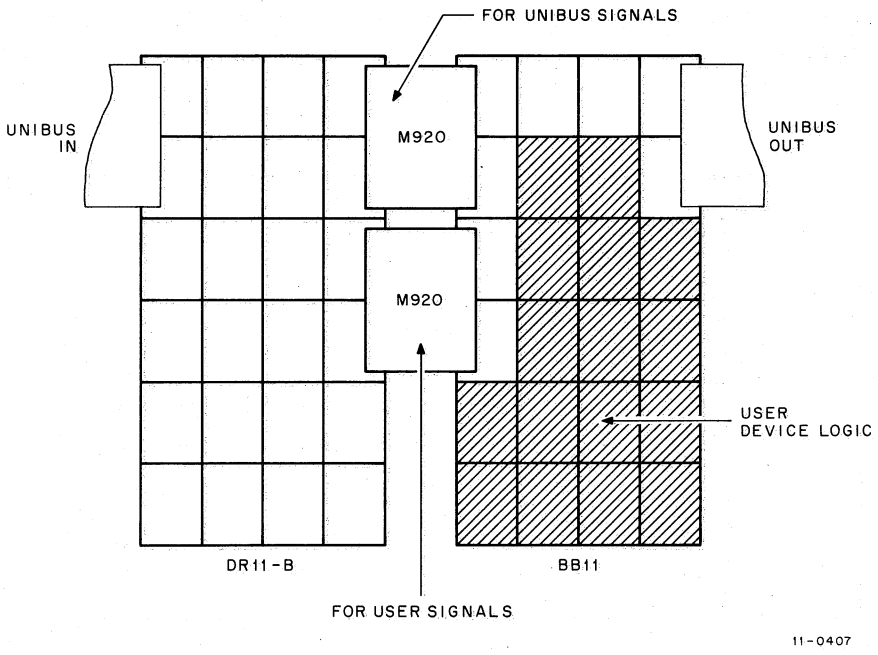


Figure B-2 DR11-B/BB11 Connection

In this configuration, 16 slots are available in the BB11 for user device logic.

CAUTION

The BB11 has -15V wired to pin B2 of all logic slots; the M920 Connector Module assumes B2 to be a ground pin. Thus, before an M920 can be used between the DR11-B and BB11, -15V must be removed from pins C01B2 and D01B2 of the BB11.

In the exceptional case where the user device logic is minimal (less than 25 dual-in-line integrated circuit packages), no cabling is necessary if this small amount of logic is packaged on a double-height module that plugs into the user device slots (CD04) of the DR11-B. The W943 Wire Wrappable Module, which allows custom design of logic boards, is available from DEC for this purpose.

B.3 M9760 TWISTED PAIR CABLE CONNECTOR

For improved noise immunity, a M9760 cable connector module is supplied with each DR11-B. Each signal line driven by the DR11-B has a 75-ohm series resistor. It is recommended that the user receive all lines with high threshold gates such as DEC 380 and drive all lines to the DR11-B through a 75-ohm series resistor. As shown on drawing D-CS-M9760-0-1, the user can easily modify the terminations for custom design to suit his particular application.

M611 C03

D3 FNCT1 (1)H — F1 H1 E2 F2
D3 FNCT2 (1)H — J1 K1 H2 J2
D3 READY (1)L — N1 P1
D3 FNCT3 (1)H — L1 M1 K2 L2
D4 DAT11 OUT (1)L — R1 S1
D4 DAT15 OUT (1)L — P2 R2
D4 DAT09 OUT (1)L — V1 U1
D4 DAT14 OUT (1)L — S2 T2
D4 DAT07 OUT (1)L — U2 V2
D4 DAT13 OUT (1)L — A1 B1
D4 DAT05 OUT (1)L — D1 E1
D4 DAT12 OUT (1)L — F1 H1
D4 DAT03 OUT (1)L — E2 F2
D4 DAT10 OUT (1)L — J1 K1
D4 DAT01 OUT (1)L — H2 J2
D4 DAT08 OUT (1)L — L1 M1
D4 DAT00 OUT (1)L — K2 L2
D4 DAT06 OUT (1)L — N1 P1
D4 DAT04 OUT (1)L — R1 S1
D4 DAT02 OUT (1)L — P2 R2
D3 GO L — V1 U1

C1 M2 N2

M611 D03 (C1 M2 N2)

M957 D04

A1	D6 BA INC ENB H
A2	+5V
B1	(SPARE)
B2	
C1	(SPARE)
C2	
D1	
D2	(SPARE)
E1	
E2	D6 FNCT1 H
F1	D6 C0 CONTROL H
F2	D6 C1 CONTROL H
H1	D6 FNCT2 H
H2	D6 SINGLE CYCLE H
J1	D6 READY H
J2	D6 FNCT3 H
K1	D6 DAT11 OUT H
K2	D6 DAT15 OUT H
L1	D6 DAT09 OUT H
L2	D6 DAT14 OUT H
M1	D6 DAT07 OUT H
M2	D6 DAT13 OUT H
N1	D6 DAT05 OUT H
N2	D6 DAT12 OUT H
P1	D6 DAT03 OUT H
P2	D6 DAT10 OUT H
R1	D6 DAT01 OUT H
R2	D6 DAT08 OUT H
S1	D6 DAT00 OUT H
S2	D6 DAT06 OUT H
T1	
T2	D6 DAT04 OUT H
U1	
U2	D6 DAT02 OUT H
V1	D6 GO H
V2	

D6 CYCLE REQUEST B H

M113 F03 — U1 — +3VF03U1

D2 END CYCLE L — A1 M611 C03 B1 — D6 END CYCLE OUT H

M957 C04

A1	D6 CYCLE REQUEST A H
A2	+5V
B1	
B2	
C1	D6 DAT00 IN H
C2	
D1	D6 DAT01 IN H
D2	D6 DAT02 IN H
E1	D6 DAT03 IN H
E2	D6 DAT04 IN H
F1	D6 DAT05 IN H
F2	D6 DAT06 IN H
H1	D6 DAT07 IN H
H2	D6 DAT08 IN H
J1	D6 DAT09 IN H
J2	D6 DAT10 IN H
K1	D6 DAT11 IN H
K2	D6 DAT12 IN H
L1	D6 DSTAT B H
L2	D6 DAT13 IN H
M1	D6 ATTN H
M2	D6 DAT14 IN H
N1	
N2	D6 DAT15 IN H
P1	
P2	D6 DSTAT A H
R1	D3 NO LOCK H
R2	D6 DSTAT C H
S1	
S2	D6 BUSY H
T1	
T2	D6 A00 H
U1	+3VF03U1
U2	D3 INIT H
V1	D6 WC INC ENB H
V2	

D2 BUSY (1)L — D1 M611 C03 E1 — D6 BUSY H

FIRST USED ON OPTION/MODEL: DRII-B	QTY.	DESCRIPTION — PARTS LIST	PART NO. / ITEM NO.
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES: DECIMALS .XXX = .005, .XX = .02, .X = .1; ANGLES ±0° 30'	DRN. W.MAJOR	DATE 2/19/71	digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
	CHK'D.	DATE 3-4-71	TITLE: USER DEVICE CONNECTIONS D6
	ENG.	DATE 3/4/71	
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓	PROJ ENG.	DATE 3-17-71	
MATERIAL	PROD.	DATE 3/22/71	
FINISH	NEXT HIGHER ASSY. A-ML-DRII-B	SIZE D / CODE IC / NUMBER DRII-B-06 / REV.	
	SCALE	SHEET 1 OF 1	DIST.

REVISIONS: REV | CHANGE NO. | CHK

DEC FORM NO DRD 102-B

APPENDIX C
DA11-B INTERPROCESSOR LINK

C.1 INTRODUCTION

C.1.1 General Description

The DA11-B Interprocessor Link can be used to form a direct memory access (DMA), parallel data transfer channel between two PDP-11 computer systems. The DA11-B includes an accessory kit designed for use with the DR11-B General Purpose DMA Interface. The kit consists of a set of modules and cables that connect two DR11-Bs in a back-to-back manner, so that the data signal lines from one are routed via the link to the input signal connections of the other. The link also passes control information and interrupt requests between the two computer interfaces. The complete interprocessor channel is illustrated in Figure C-1.

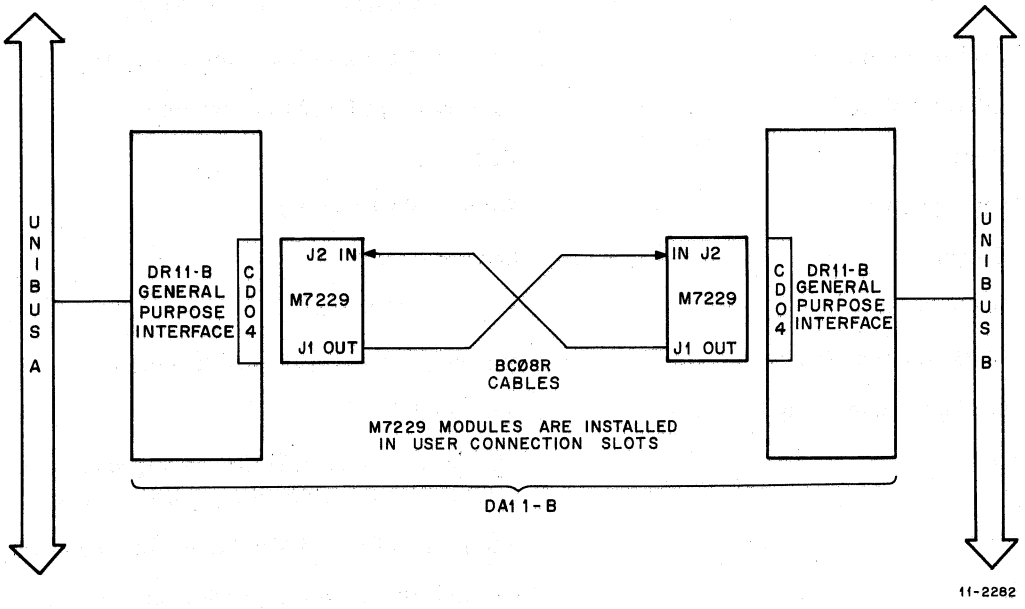


Figure C-1 Block Diagram of PDP-11 DMA Interprocessor Channel

The half-duplex interprocessor communications channel of the DA11-B transfers data from memory to memory in blocks of up to 32K words, with a maximum transfer rate of 500,000 words per second. (The rate can be adjusted according to system configuration.)

The DA11-B occupies one system unit space in each PDP-11; the M7229 buffer modules are installed in user connection slots of their respective DR11-Bs.

C.1.2 DA11-B Option Designations

a. DA11-BD = DMA Interprocessor Link with 25-foot cables
b. DA11-BE = DMA Interprocessor Link with 50-foot cables
c. DA11-BF = DMA Interprocessor Link with 100-foot cables.

C.1.3 DA11-B Specification Summary

Installation	M7229 module is installed in user connection slots (CD04) in each DR11-B.
Maximum Cable Length	100 ft.
Prerequisite	Two PDP-11 computer systems.
Programming Features	
Addressable Registers	Four addressable registers in each interface: Word Count (DRWC) Bus Address (DRBA) Control and Status (DRST) Data Buffer (DRDB)
Register Addresses	Same as DR11-B (772410 for first unit)
Interrupt Vector	Same as DR11-B (124 for first unit).
BR Level	BR5.
Operating Modes	Word or block transfer.
Direction	Send or receive.
Word Size	16 bits parallel data.
Block Transfer Method	Direct memory access via NPR control.
Maximum Block Length	32K words.
Installation	Channel occupies one system unit space in each computer. Can be installed in any PDP-11 mounting box.
DC Power	4.0 A (max) from +5 Vdc supply for each interface.
Bus Load	One unit Unibus load for each interface.
Unibus Compatibility	Can be used with any PDP-11 family processor.

C.2 THEORY OF OPERATION

C.2.1 General

Since the DA11-B Interprocessor Link is based on the DR11-B General Purpose DMA Interface, its operation is defined primarily by the DR11-B. The nomenclature used in connection with the DR11-B is used to describe the DA11-B.

The DA11-B link operates as a half-duplex communications channel. Half-duplex means that, although the channel has the capability of transmitting data in both directions, it is dedicated to transmitting in only one direction at a given time. The following description generally refers to one-way data flow; it should be understood that information can also flow in the opposite direction.

C.2.2 Operating Modes

The DA11-B operates in two different modes, Word and Block. In Word mode, information can be passed between computers one word at a time by interrupt-driven program commands. In Block mode, the link transmits blocks of consecutive locations from the memory in one computer to the memory in the other using the DMA (NPR) facility in each machine. The block transfer is, then, transparent to the programs in the two computers.

Each computer has independent program control of its own interface. Therefore, the programs in the two machines must cooperate in establishing channel direction and in priming Word Count and Bus Address registers in their respective DR11-B interfaces. The Word mode is used primarily to pass information relating to this channel set-up operation prior to a block transfer. However, it is not restricted to this function; the Word mode can also be used to transfer any other types of parameters between the computers as long as a DMA transfer is not in progress.

C.2.3 Block Diagram

Figure C-2 shows a simplified block diagram of the complete interprocessor DMA communications system. As shown in this figure, there are two separate channels through the link in opposite directions. However, since the link operates as a half-duplex device, only one channel is active at a time.

The Data Buffer register (DRDB) is connected through the link to the bus data multiplexer in the opposite computer. In Word mode, DRDB can be loaded with a full 16-bit word by the program on one side and read by the program in the other computer. In Block mode, DRDB serves as temporary storage for the word being transferred via NPR control.

The Control and Status registers (DRST) are cross-coupled via three bits in each direction. When DRST ⟨3:1⟩ are loaded on one side, the information appears in DRST ⟨11:9⟩ in the opposite computer. These bits also connect to the DA11-B control logic in each interface to define the following operations:

Signal	Transmitter	Receiver
Interrupt Request	DRST 3	DRST 11
Direction	DRST 2	DRST 10
Mode	DRST 1	DRST 9

The DA11-B control logic is cross-coupled to activate interrupt requests and coordinate the NPR cycles on each Unibus.

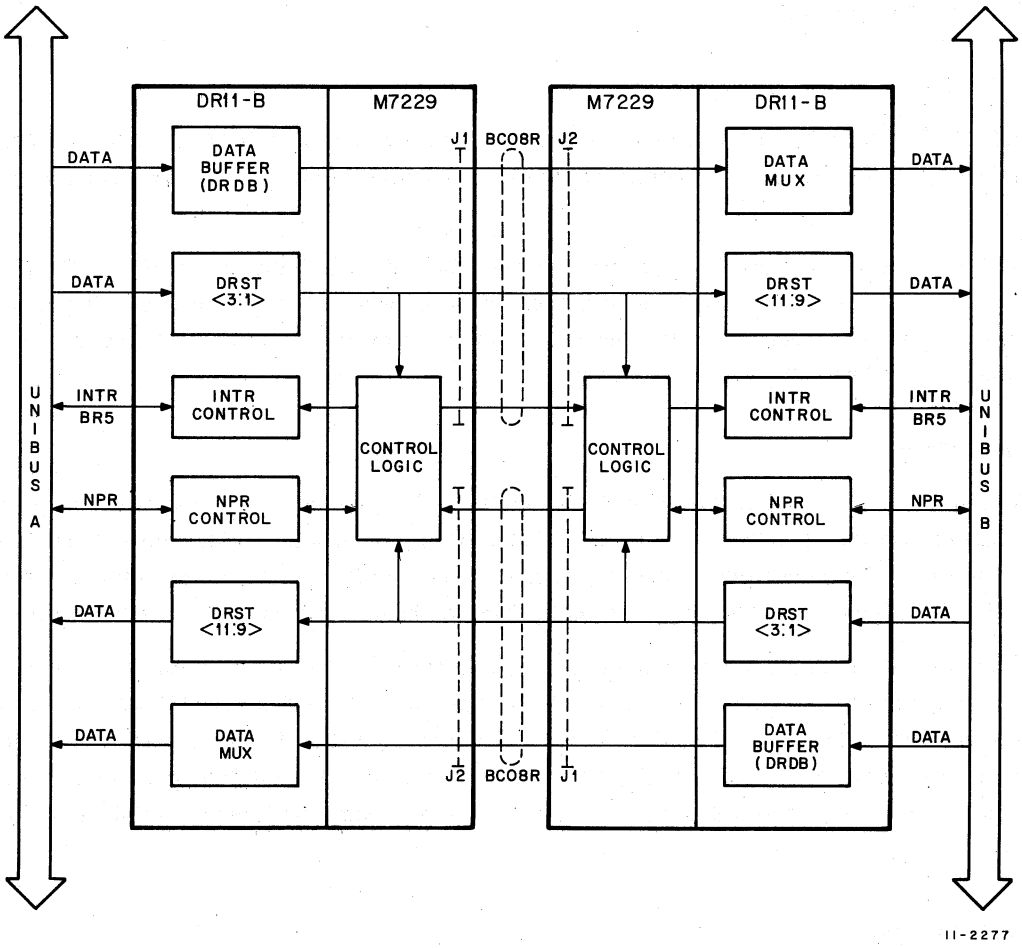


Figure C-2 DMA Interprocessor Channel Functional Block Diagram

C.2.4 Cross-Interrupt Connection

Figure C-3 shows the block diagram of the cross-interrupt connection in one direction. (There is, of course, an identical circuit in the opposite direction.) When DRST 3 is set in one computer, a binary 1 appears in DRST 11 of the opposite interface. At the same time, the M7229 generates a 500 ns pulse on the ATTN line into the receiving DR11-B. This pulse sets the READY flag (DRST 7), and also appears briefly on the ATTN flag (DRST 13). If INTERRUPT ENABLE (DRST 6) of the receiver has been set previously, the action of setting READY produces an interrupt request into the processor on the receiver's bus. (Note that READY also produces interrupt requests due to other conditions, as described in Paragraph C.3.) When the interrupt service routine responds to the request, it can identify the interrupt as coming from the companion computer by inspecting DRST 11.

When one of the processors issues an INIT (initialization) pulse to clear the devices on its bus (including its DR11-B), the INIT pulse is transmitted to the other computer where it sets READY and causes an interrupt request as described above. Note that an INIT command will abort a Block mode transfer because it clears all DR11-B registers on its bus; thus, the link cannot be used whenever INIT is asserted.

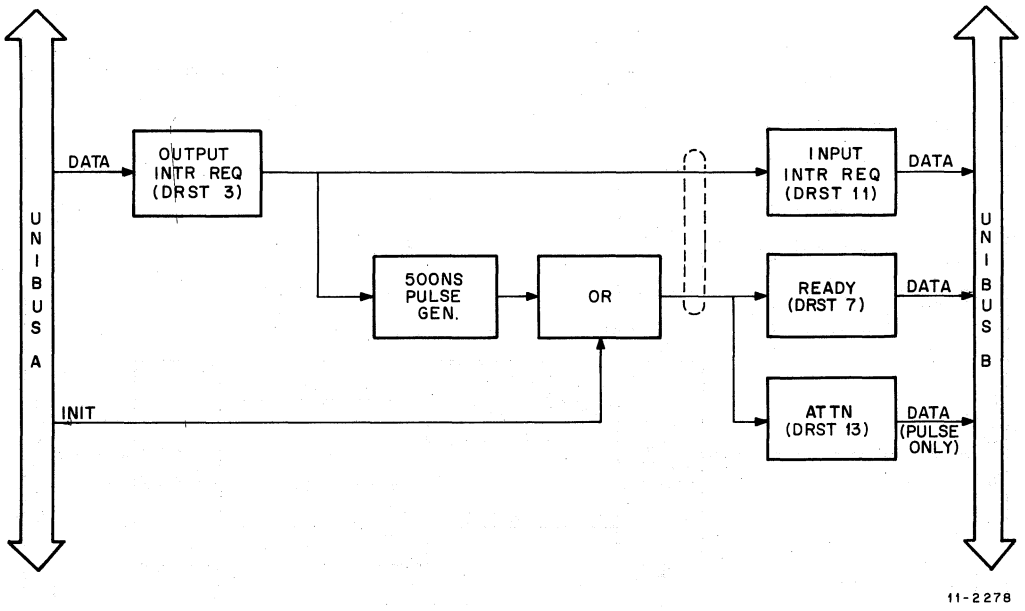


Figure C-3 Cross-Interrupt Block Diagram

C.2.5 NPR Interlocking Control

Figure C-4 shows the block diagram of the control circuits used to interlock the alternating NPR cycles on the appropriate buses during Block mode transfers. Two factors must be taken into account to start the NPR transfer. First, a program in either computer may request the transfer operation. Second, the data may flow in either direction. (Figure C-4 shows only the circuits required to establish a transfer from Unibus A to Unibus B. Duplicate circuits exist for the other direction.)

The NPR cycles always occur in pairs (i.e., one on each bus). The first cycle is a DATI (read from memory) by the transmitter (Unibus A in Figure C-4). The second cycle is a DATO (write into memory) by the receiver (Unibus B). These alternating pairs of cycles keep repeating until the entire block has been transmitted. The control circuits illustrated in Figure C-4 perform two functions.

The circuits associated with the GO commands (DRST 0) are used in conjunction with the programming procedure described below to generate the first NPR cycle by the transmitter.

The END CYCLE circuits produce all subsequent NPR cycles required by the block transfer.

The programming procedure to initiate a block transfer follows:

1. The requesting computer sets up the Word Count and Bus Address registers in its own DR11-B. It then loads the following information into its Status register:
   a. GO (DRST 0) is set to a 1 to clear READY (DRST 7).
   b. MODE (DRST 1) is cleared to a 0 to indicate Block mode.
   c. DIRECTION (DRST 2) is cleared to a 0 to indicate Transmit or set to a 1 to indicate Receive.
   d. INT REQ (DRST 3) is set to a 1 to interrupt the other computer.

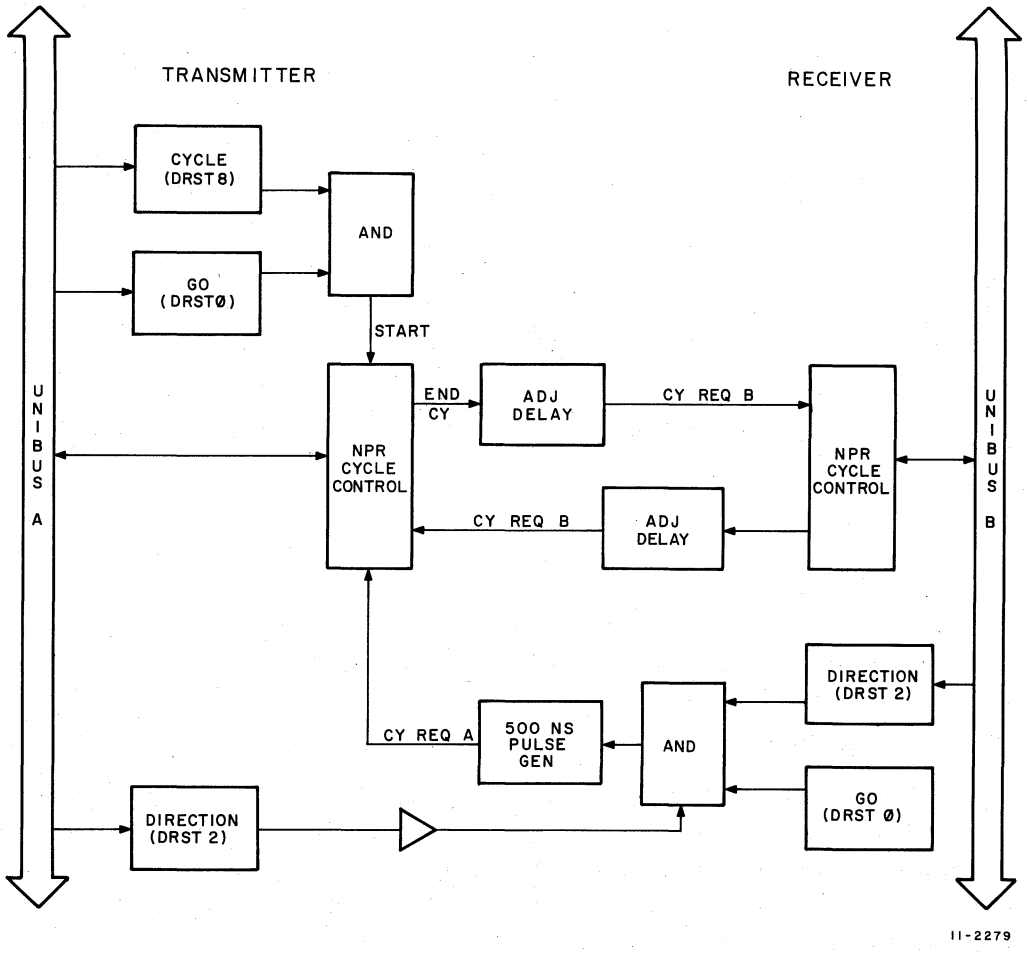


Figure C-4 NPR Interlocking Control Block Diagram

2. Upon receiving the interrupt, the requested computer sets up its Word Count and Bus Address registers and loads its Status register as follows:

   a. MODE (DRST 1) is cleared to a 0 to indicate Block mode.

   b. DIRECTION (DRST 2) is set or cleared to indicate direction. Note that this flag *must* be opposite to the Direction flag in the requesting computer.

   c. If the *requested* computer is the receiver (Processor B), it sets GO (DRST 0) to generate a GO pulse that is passed through the M7229 as CYCLE REQUEST A to the transmitter.

   OR

   d. If the *requested* computer is the transmitter (Processor A), it sets both GO (DRST 0) and CYCLE (DRST 8) to generate a START command to its own NPR cycle control circuit.

When the transmitter has read the data word from its memory and loaded it into its data buffer (DRDB), its NPR cycle control logic generates an END CYCLE pulse. This pulse is stretched by an adjustable delay and sent as CYCLE REQUEST B to the receiving computer. The trailing edge of the stretched pulse triggers an NPR cycle that writes the data word into the receiver's memory. The termination of the write cycle likewise produces an END CYCLE pulse to initiate the next read operation in the transmitter. This alternating sequence continues until the Word Count registers overflow and halt the block transfer.

The interval between successive NPR cycles on a UNIBUS is equal to the sum of the two adjustable delay timers plus the time required to request and accomplish two NPR cycles. Each delay is adjustable from approximately 5 to 50 μs. Therefore, the interval between NPR requests to one of the processors can be adjusted over the range of approximately 10 to 100 μs, yielding an interprocessor data rate of 10K to 100K words per second. If a higher rate is desired, the capacitor in the adjustable delay circuit can be reduced in value to shorten the delay. The maximum interprocessor data rate is one-half the cycle rate of the memories being addressed.

C.3 PROGRAMMING

C.3.1 General

The programming characteristics of the DA11-B Interprocessor Link are basically the same as those of the DR11-B Interface. However, when two DR11-Bs are interconnected by the DA11-B, the Control and Status register and the Data Buffer register definitions are modified slightly (as indicated in subsequent paragraphs) to reflect this particular application.

Refer to the *DR11-B Manual,* Chapter 2, for complete details regarding the programmable registers.

C.3.2 Word Count Register (DRWC)

This 16-bit R/W register is initially loaded with the 2's complement of the number of transfers to be made. It increments toward zero after each bus cycle until DRWC overflows, setting READY (DRST 7). DRWC is a word register. DO NOT USE BYTE INSTRUCTIONS WHEN LOADING THIS REGISTER.

C.3.3 Bus Address Register (DRBA)

This register is used only as a 15-bit register; bit 00 is permanently set to 0. Interprocessor transfers can be made for full words only. DO NOT USE BYTE INSTRUCTIONS WHEN LOADING THIS REGISTER.

C.3.4 Control and Status Register (DRST)

This register provides status indicators for the DA11-B and the DR11-B, as shown in Figure C-5 and described in Table C-1.

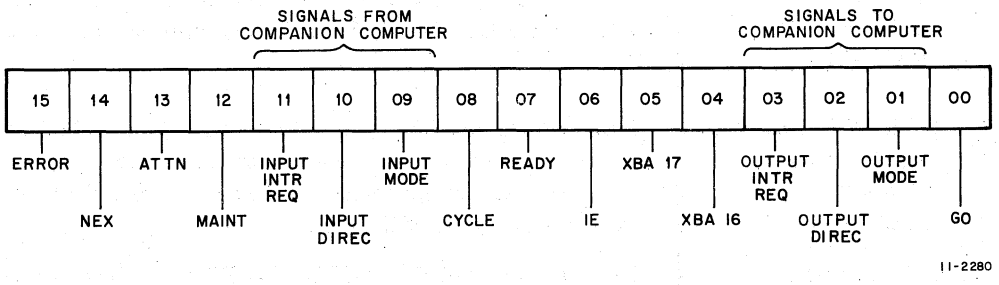


Figure C-5 DRST Register Assignments

Table C-1
Control and Status Register (DRST) Bit Description

Bit	Name	Meaning and Operation
15	ERROR (Read Only)	Indicates an error or the external interrupt flag. Sets under the following conditions: a. The DR11-B attempts to address nonexistent memory (also indicated by NEX). Cleared when NEX is cleared by loading DRST 14 with a 0. b. The companion computer asserts ATTN (DRST 13) because of an Input Interrupt Request or an Initialize (INIT) pulse. Cleared when ATTN is automatically cleared by the companion computer. c. The test module is not inserted in slot AB02 or CD04 of the DR11-B. Cleared when the test module is inserted in slot AB02 for normal operation or slot CD04 for diagnostic tests. d. The Bus Address register (DRBA) overflows by incrementing from all 1s to all 0s. Cleared by reloading the Bus Address register. ERROR sets READY (DRST 7) and causes an interrupt if INTERRUPT ENABLE (DRST 6) is set.
14	NEX (Nonexistent Memory) (Read/Write)	Indicates that, as Unibus master, the DR11-B did not receive an SSYN response within 20 μs after asserting MSYN. Sets ERROR and READY and causes an interrupt request if IE has been set. Cleared by INIT or by loading with a 0; cannot be loaded with a 1.
13	ATTN (Attention) (Read Only)	Reads the status of the ATTN pulse from the companion computer. When that computer requests an interprocessor interrupt, the ATTN pulse (which sets ERROR) is generated by Input Interrupt Request (INPUT INTR REQ) (DRST 11) of that computer (lasts approximately 500 ns), or by INIT (lasts up to 20 ms). Because the ATTN signal is a pulse, this bit should be ignored by the interprocessor programs. Cleared automatically by the DA11-B link.
12	MAINT (Maintenance) (Read/Write)	Used exclusively by the DR11-B diagnostic programs. (Refer to the *DR11-B Manual*, Chapter 5, for further information.) Cleared by INIT.
11	INPUT INTR REQ (Input Interrupt Request) (Read Only)	Reads the status of the OUTPUT INTR REQ bit of the companion computer. When set, indicates that an interprocessor interrupt has been requested by the companion computer. Sets READY and causes an interrupt request if IE is set.
10	INPUT DIREC (Input Direction) (Read Only)	Reads the status of the OUTPUT DIREC bit of the companion computer. Indicates the transfer direction; 0 indicates that companion computer is transmitter, 1 indicates that companion computer is receiver.
09	INPUT MODE (Read Only)	Reads the status of the OUTPUT MODE bit of the companion computer, and indicates the mode in which the DA11-B is to be used; 0 indicates Block mode, 1 indicates Word mode.

Table C-1 (Cont)
Control and Status Register (DRST) Bit Description

Bit	Name	Meaning and Operation
08	CYCLE (Read/Write)	Used to initiate the block transfer when this DR11-B is both the transmitter and the requested computer. When set together with GO (DRST 0), an immediate bus cycle occurs. Cleared by INIT. Also set each time the companion computer requests a bus cycle via CYCLE REQUEST A or B, and cleared when the cycle begins (refer to Paragraph C.2.5, NPR Interlocking Control), but these pulses should be ignored by the interprocessor programs.
07	READY (Read Only)	Indicates that the DR11-B is ready to accept a new command. When set, forces the DR11-B to release control of the Unibus and inhibits further DMA cycles; if IE is set, causes an interrupt. Set by INIT, ERROR, or word count overflow. Cleared by GO. Must be cleared before initiating block transfer.
06	IE (Interrupt Enable) (Read/Write)	When set, allows the DR11-B to generate an interrupt request if ERROR, READY, or INPUT INTR REQ is set. Cleared by INIT.
05	XBA 17	Extended Bus Address bit 17. Cleared by INIT.
04	XBA 16	Extended Bus Address bit 16. Cleared by INIT.
03	OUTPUT INTR REQ (Output Interrupt Request) (Read/Write)	Used to send an interrupt request to the companion computer. When set, sets INPUT INTR REQ and READY in the companion computer and causes an interrupt request in the other computer if its IE is set. Cleared by INIT.
02	OUTPUT DIREC (Output Direction) (Read/Write)	Used to indicate status of this DR11-B during subsequent block transfer. 0 indicates transmitter, 1 indicates receiver. Must be set opposite to INPUT DIREC. Cleared by INIT.
01	OUTPUT MODE (Read/Write)	Used to indicate the mode in which the DA11-B is to be used. 0 indicates Block mode, 1 indicates Word mode. This bit is not used in any way by the DA11-B control logic, but is simply displayed in the companion computer. May be used by the interprocessor programs to keep track of the progress of the cross-communications dialogue that precedes a block transfer, and also to note that a block transfer is in process. Cleared by INIT.
00	GO (Write Only)	Causes a pulse to initiate the first DMA cycle in the block transfer. When set together with CYCLE, causes the first cycle to occur in this computer if this DR11-B is the transmitter. When set by itself, causes the first cycle to occur in the companion computer if that DR11-B is the transmitter. (Note that both DIRECTION bits should be set properly before the GO command is issued.) When set, clears READY. GO always reads as a 0.

C.3.5 Data Buffer (DRDB)

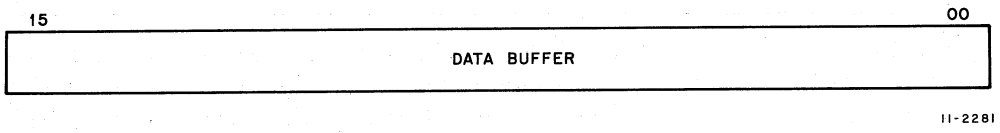
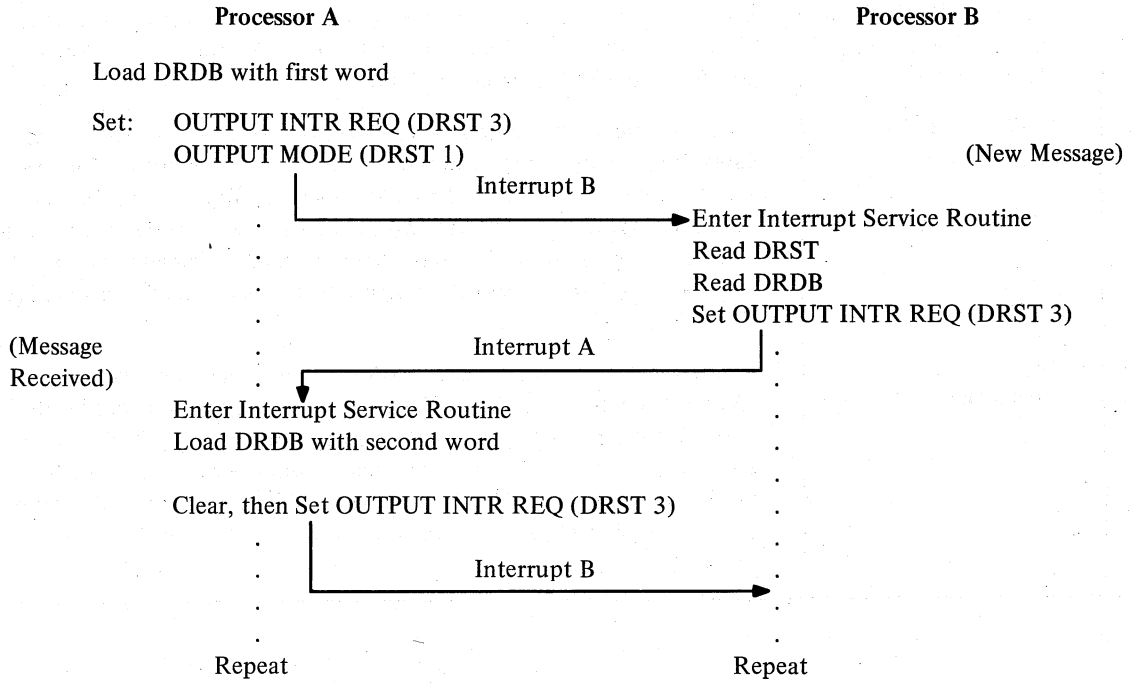


Figure C-6 Data Buffer (DRDB) Register Assignments

The Data buffer (DRDB) performs two separate functions in the interprocessor channel (Figure C-6). In Word mode, DRDB is used as a 16-bit addressable register to transfer information between computers under program control. In Block mode, DRDB serves as a temporary storage register that holds the word being transferred under NPR control.

C.3.5.1 Word Mode – During program-controlled transfers, DRDB is a write-only register for data transmitted to the companion computer and a read-only register for data received. Since there is only a single flip-flop register for each direction, data must be maintained in DRDB until read by the companion computer. It is recommended that the cross-interrupt facility in DRST be used in conjunction with DRDB to pass parameters between computers as illustrated in the following example.

Assume Processor A is sending a file header to Processor B.



C.3.5.2 **Block Mode** – During block transfers under NPR control, DRDB temporarily stores the word read by the transmitter until it is written into memory by the receiver. Because this sequence of operations is transparent to the program, DRDB may *not* be used for Word mode transfers until the block transfer has been completed. If DRDB is loaded by the program during a block transfer, incorrect data may be transmitted between computers. DRDB is cleared by INIT.

NOTE
DRDB is a word register; do not use byte instructions when loading this register.

C.3.6 Bus Address and Vector Assignments

The interfaces used in the DA11-B Interprocessor Link are assigned bus addresses and vectors in accordance with the procedure used for standard DR11-B interfaces. Refer to the DR11-B manual, Paragraph 2.5.

C.3.7 Interrupt Flags

Table C-2 shows the bits that will be set in DRST following an interrupt request. If several interrupt conditions occur simultaneously, DRST will contain the inclusive OR of all the bits noted in the table for all requests that are pending.

Table C-2
DRST Interrupt Request Bit Status

Interrupt Caused By	15 ERROR	14 NEX	13 ATTN	11 INPUT INTR REQ	07 READY
Nonexistent memory address from DR11-B	1	1	0	0	1
INIT pulse asserted on companion computer's bus	1*	0	1*	0	1
Test module not inserted	1	0	0	0	1
DRBA overflow	1	0	0	0	1
Input interrupt request from companion computer	0	0	0	1	1
DRWC overflow indicating block transfer complete	0	0	0	0	1

*Asserted for duration of pulse only.

C.3.8 Notes on Programming the Interprocessor Channel

The interprocessor channel provides four modes of operation: Transmit or Receive, with either Word or Block mode data transfers. These four modes are specified by setting the appropriate function bits in the two status registers. Before initiating a Block mode (i.e., NPR) transfer, the DIRECTION bits in the two status registers must be of opposite value. This point of possible conflict must be resolved by the programs in the two computers. Because either computer may initiate a transfer, clearing the function bits after each transfer can help to avoid this conflict.

Cross-communication between the two computers is best accomplished by using the interprocessor interrupt bits. Because the signals between computers are not interlocked with Unibus operations, it is not advisable to execute instructions on the status registers at a time when signals may be received from the companion computer. By passing information only under interrupt control, a software interlock can be achieved and there will be no danger of losing information.

C.4 INSTALLATION AND MAINTENANCE

C.4.1 Installation Procedure

The DA11-B Interprocessor Link is easily installed between any two PDP-11 family computers, using the following procedure.

1. Install one DR11-B Interface in a System Unit Mounting Box in each computer and connect to each computer's Unibus.
2. Select the bus address and vector for each DR11-B as described in Paragraph C.3.4. Cut the appropriate jumper patterns on the M7213 Address Select and M7821 Interrupt Control modules in each interface.
3. Insert the M968 Test Boards in slots AB02 of each interface.
4. Insert the M7229 Interprocessor Link modules in slots CD04 of each interface.
5. Connect the two BC08R cables supplied as part of the DA11-B Link between the M7229 modules. Each cable should connect the Output connector of one module to the Input connector of the other as illustrated in Figure C-1.

C.4.2 Checkout Procedure

In order to check out the complete Interprocessor channels, each DR11-B Interface should first be checked out individually. Then the DA11-B Interprocessor Link should be installed and the Interprocessor Link Exerciser program run. The complete checkout procedure is as follows:

1. Check out each DR11-B Interface.
   a. Insert the M968 Test Board in slot CD04 of the DR11-B.
   b. Run the option checkout portion of the DR11-B diagnostic program as specified in the program listing.
   c. Remove the test board from slot CD04 and insert it in slot AB02 of the DR11-B.
2. Install the DA11-B Interprocessor Link as described in Paragraph C.4.1.
3. Run the Interprocessor Link portion of the DR11-B diagnostic program as specified in the program listing.

The Interprocessor Channel should now be ready for normal programmed operation.

C.4.3 Maintenance

Refer to the *DR11-B Maintenance Manual* for information on maintaining that portion of the interprocessor channel. Standard troubleshooting techniques for logic circuits are used to maintain the DA11-B. No special equipment or techniques are required.

C.4.4 Adjusting the Interprocessor Data Transfer Rate

The DA11-B option offers the capability of adjusting the rate of interprocessor data transfers, thereby regulating the NPR load on each system. The first step is to select an appropriate position on the NPR priority chain of each computer. DR11-B interfaces are normally installed after high-speed DMA devices such as disks or magnetic tape drives. This step, in itself, will ensure that the interprocessor channel does not interfere with transfers by the high-speed equipment.

The second step is to adjust the potentiometers on the rear edges of the M7229 modules. These potentiometers determine the interval between successive END CYCLE pulses. The adjustment procedure is as follows:

1. Load and run the DA11-B Interprocessor Link portion of the DR11-B diagnostic.
2. Observe the END CYCLE pulse generated by one of the DR11-Bs on an oscilloscope at the system unit backplane slot C04 pin B1.
3. With both potentiometers set for the minimum interval between pulses, first adjust one potentiometer and then the other unit until the desired rate is achieved.

Potentiometer Adjustment	Approximate Pulse Interval
Both set to minimum	15 μs
Adjust first potentiometer	50 μs max
Adjust second potentiometer	85 μs max

If a different adjustment range is desired, remove capacitor C8 from both M7229 modules and replace as noted:

C8	Approximate Range
200 pF	1.5 to 8.5 μs
0.02 μF	150 to 850 μs

DR11-B/DA11-B
DEC-11-HDRBA-D-D

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