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91A24/91AE24
SERVICE MANUAL ADDENDUM

TO THE DAS 9100 SERIES SERVICE MANUAL
(PART NUMBERS 062-5848-00, -01, AND UP)

The 062-5848-00 manual set is a package consisting of loose leaf binders with manuals and addenda. Each manual and addendum in the set has its own part number starting with the prefix 070. You can find your manual part number in the bottom left conrner of the manual title page.

This addendum contains service information specific to the 91A24 and 91AE24 Data Acquisition Modules. Refer to the *DAS 9100 Series Service Manual* for information on other DAS products, including mainframes, instrument modules, probes, and options.

How To Use This Addendum. This addendum is organized similarly to the *DAS 9100 Series Service Manual:* sections in the addendum correspond to the sections in the service manual. You can either leave the addendum whole and place it in one of the service manual binders, or you can separate the sections and insert them after the corresponding section in the main manual.

> NOTE: You can order an extra service manual binder (Vol. III) by using P/N 016-0769-00.

PLEASE CHECK FOR CHANGE INFORMATION
AT THE REAR OF THIS MANUAL

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> ## WARNING
>
> *The following service instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so.*

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OPERATOR'S SAFETY SUMMARY

The general safety information in this summary is for both operators and service personnel. Specific cautions and warnings are found throughout the manual where they apply but may not appear in this summary.

TERMS IN THIS MANUAL

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

TERMS AS MARKED ON EQUIPMENT

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property, including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS AS MARKED ON EQUIPMENT

⚡ **DANGER** — High voltage.

⏚ Protective ground (earth) terminal.

⚠ **ATTENTION** — refer to manual.

GROUNDING THE PRODUCT

The mainframe in which this product is installed is intended to operate from a power source that does not apply more than 250 V rms between the supply conductors or between either supply conductor and ground.

This product is grounded through the mainframe in which it is operating. To avoid electrical shock, plug the power cord of the mainframe into a properly wired receptacle before connecting to the product. A protective-ground connection by way of the grounding conductor in the power cord is essential for safe operation.

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including keys and controls that may appear to be insulated) can render an electric shock.

DO NOT OPERATE WITHOUT COVERS

To avoid personal injury, do not operate this product without mainframe covers or panels installed. Circuit boards and components can become very hot during operation.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

SERVICE SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY
Refer also to the preceding Operator's Safety Summary.

DO NOT SERVICE ALONE

Do not perform service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

USE CARE WHEN SERVICING WITH POWER ON

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before soldering or replacing components.

DO NOT WEAR JEWELRY

Remove jewelry prior to servicing. Rings, necklaces, and other metallic objects could come into contact with dangerous voltages.

NOTE

Observe safety precautions stated in the DAS 9100 Series Service Manual *concerning CRT safety, X-ray emission, and loose objects.*

INTRODUCTION AND SPECIFICATIONS

DESCRIPTION

The 91A24 and 91AE24 Data Acquisition Modules are plug-in circuit board assemblies compatible with any DAS 9100 Series mainframe. They feature acquisition rates of up to 10 MHz non-multiplexed, and 20 MHz multiplexed. Each module uses three P6460 or P6462 Data Acquisition Probes.

A maximum of one 91A24 module may be installed in a DAS mainframe. Up to three 91AE24 modules may also be installed to increase the width to 96 channels. The 91AE24s are expander modules and can only be used if a 91A24 module is installed.

MODES OF OPERATION

DATA ACQUISITION

Each 91A24 and 91AE24 module provides twenty-four incoming data channels supplied by three P6460 Data Acquisition probes.

The 91A24 and 91AE24 modules can acquire data using the DAS internal clock at intervals ranging from 5 ms to 100 ns, or using an external clock's rising or falling edge (20 MHz maximum). The maximum memory depth in this mode is 1023 words.

91A24 and 91AE24 triggering can be positioned in the beginning, center, or end of acquisition memory; or it may be delayed for up to 32,767 clock cycles.

Data may be displayed in either the State Table or Timing Diagram menus.

ARMS TRIGGER MODE

The 91A24 and 91AE24 modules can be used in an ARMS trigger mode with 91A04 and 91A08 Data Acquisition Modules. In this mode, the two types of modules run simultaneously, but at different clock rates. The 91A04/91A08 trigger enables the 91A24/91AE24 modules to begin looking for a trigger.

The resulting time-aligned display can be viewed in either the State Table or Timing Diagram menus. In the ARMS mode, the 91A24/91AE24 data display is limited to the last 512 words acquired.

STANDARD AND OPTIONAL ACCESSORIES

91A24 DATA ACQUISITION MODULE

The following lists include the standard and optional accessories for the 91A24 Data Acquisition Module.

Standard Accessories

3	010-6460-01	P6460 Data Acquisition Probes with lead sets
1	070-4540-00	*91A24, 91AE24, and P6460 Operator's Manual Addendum* (to the *DAS 9100 Series Operator's Manual*)
1	175-8165-00	External SYNC OUTPUT cable
1	070-4672-00	*91A24 Data Acquisition Module Instructions*

Optional Accessories

1	070-4541-00	*91A24 and 91AE24 Service Manual Addendum* (to the *DAS 9100 Series Service Manual*)
1	175-8166-00	11-inch Interconnect Cable

91AE24 DATA ACQUISITION MODULE

The following lists include the standard and optional accessories for the 91AE24 (Expander) Data Acquisition Module.

Standard Accessories

3	010-6460-01	P6460 Data Acquisition Probes with lead sets
7	175-8167-00	3-inch Interconnection cable assembly.
1	070-4671-00	*91AE24 Data Acquisition Module Instructions*

Optional Accessories

There are no optional accessories for the 91AE24 module.

P6460 DATA ACQUISITION PROBE

The following lists include the standard and optional accessories for the P6460 Data Acquisition Probe.

Standard Accessories

1	070-4345-00	*P6460 Data Acquisition Probe Instructions*
1	012-0747-00	Lead set, 10 inch
1	020-0720-00	Package of 12 Probe Tips (each tip is a 206-0222-00)
2	012-0989-00	Ground (or VL) Sense Leads, 5-inch with Pomona Hook Tips (344-0267-00)
2	344-0046-00	Alligator Clips (substitute for hook tips above)

Optional Accessories

012-0987-00	Flying Lead Set, 12.5 cm (5 inches)
012-0800-00	Flying Lead Set, 25 cm (10 inches)
012-1000-00	Diagnostic Lead Set, 10 inch
012-0989-01	Package of 10 Ground (or VL) Sense Lead Tips with Pomona Hook Tips (344-0267-00)
103-0209-00	GPIB Connector/Adapter
003-0709-00	IC Extractor, 16 pin
015-0330-00	Adapter, Test Clip, 16 DIP
015-0339-02	Adapter, Test Clip, 40 DIP, 10 cm cable (requires 380-0560-05 Adapter)
015-0338-02	Adapter, Test Clip, 40 DIP, 30 cm cable (requires 380-0560-05 Adapter)
380-0560-05	Adapter, required for use with 40 DIP Adapters
119-1474-00	Probe Holder

P6462 DATA ACQUISITION PROBE

The following lists include the standard and optional accessories for the P6462 Data Acquisition Probe.

Standard Accessories

1	070-4724-00	*P6462 Data Acquisition Probe Instructions*
1	012-0747-00	Lead set, 10 inch
1	020-0720-00	Package of 12 Probe Tips (each tip is a 206-0222-00)
1	012-0989-00	Ground (or VL) Sense Leads, 5-inch with Pomona Hook Tips (344-0267-00)
1	343-1048-00	Flat Mount Cable
2	344-0046-00	Alligator Clips (substitute for hook tips above)

Optional Accessories

012-0987-00	Flying Lead Set, 12 cm (5 in.)
012-0800-00	Flying Lead Set, 25 cm (10 in.)
012-1000-00	DAS Diagnostic Lead Set, 25 cm (10 inch)
012-0556-00	1240 Diagnostic Lead Set, 25 cm (10 inch)
012-0989-01	Package of 10 Ground (or VL) Sense Lead Tips with Pomona Hook Tips (344-0267-00)
103-0209-00	GPIB Connector/Adapter
003-0709-00	IC Extractor, 16 pin
015-0330-00	Adapter, Test Clip, 16 DIP
015-0339-02	Adapter, Test Clip, 40 DIP, 10 cm cable (requires 380-0560-05 Adapter)
015-0339-00	Adapter, Test Clip, 40 DIP, 30 cm cable (requires 380-0560-05 Adapter)
380-0560-05	Adapter, required for use with 40 DIP Adapters

SPECIFICATIONS

Table 1-1
91A24 AND 91AE24 ELECTRICAL SPECIFICATIONS: DATA ACQUISITION AND STORAGE

Characteristics	Performance Reqmnts.	Supplemental Information
Maximum Sampling Rate	10 MHz (non-multiplexed)	Internal or External Clocking (multiplexed 20 MHz)
Acquisition Memory Memory Depth		1023 Words
Memory Width		24 Channels (one 91A24, 3 probes); expandable to 96 channels (one 91A24, three 91AE24s, 12 probes).
Data Setup (period data valid prior to clock edge)	25 ns min. (using P6460 probe)	Same requirement for multiplexed data.
Data Hold (period data valid beyond clock edge)	0 ns max. (using P6460 probe)	Same requirement for multiplexed data.
Trigger Position		Selectable for BEGIN, CENTER, END, DELAY. In DELAY mode, trigger sequence = 1015 − DELAY value.
External Trigger Enable		TTL LS input to mainframe BNC connector. Rising edge enables sequential word recognizer trigger on next clock cycle.
Setup Time Hold Time	25 ns min. 0 ns max.	
91A24 ARMS Modes		High-speed module is armed to look for trigger within ten 91A24 clock cycles after 91A24 trigger event.
Requirement for Time Alignment		1. No data qualifiers are used (91A24 clock qualifiers are permitted). 2. High-speed module operation must overlap 91A24 operation by at least 5 master clocks. 3. High-speed clock rate must be at least twice that of 91A24 master clocks. 4. Trigger words for both the high-speed and 91A24 modules must be in memory.

Table 1-2
91A24 AND 91AE24 ELECTRICAL SPECIFICATIONS: CLOCKING

Characteristic	Performance Reqmnts.	Supplemental Information
Internal Clock		Interval is selectable from 100 ns to 5 ms in a 1-2-5 sequence. May be qualified using 91A24's pod C qualifier.
External Clocks & Qualifiers		3 clocks, 3 qualifiers
Source		Via acquisition probes connected to 91A24
Selection		Boolean combinations used to form 3 POD CLOCK expressions.
Raw Clock Rate	20 MHz max.	Time between *qualified* master clocks may be no less than 100 ns. Other POD CLOCKs must occur $\geqslant$ 20 ns before next cycle's master clock.
Clock Pulse Width	25 ns min., high and low (using P6460 probe)	
Qualifier Setup Time	25 ns min. (using P6460 probe)	
Qualifier Hold Time	0 ns max. (using P6460 probe)	

Table 1-3
91A24 AND 91AE24 ELECTRICAL SPECIFICATIONS: WORD RECOGNIZER FUNCTIONS

Characteristic	Performance Reqmnts.	Supplemental Information
Word Recognizer Width		Same as channel width
BEGIN STORE IF		Up to 2 ORed word recognizers
END STORE IF		Up to 2 ORed word recognizers
STORE ONLY IF		Up to 2 ORed word recognizers
RESET Word Recognizer		Resets sequential word recognizer to Level 1, and resets timer.
Independent Trigger		Parallel word recognizer ORed to sequential word recognizer. Not affected by trigger input signal.
Sequential Word Recognizer		Up to 16 levels of word recognition
OCCURS Counter		Number of event occurrences (1-4096) may be specified at each level.
Intermediate Level Actions		THEN, RUN TIMER, STOP TIMER, SYNC OUT selections
Final Level Actions		TRIGGER, INCR CNTR (12 decimal digits), SYNC & TRG, NEVER TRG selections
Timer Accuracy	Indicated value ± 2%, ± 100 ns each time started	Times to over 27 hours.
Sync Output Signal	TTL output level, terminated into 1 MΩ	Remains high until completion of a subsequent word recognizer level with no sync-output specified.
Sync Output Delay	3 master clocks + 45 ns ± 10 ns between event occurrence and rising edge of sync-output	Measured from master clock's active edge to connector output.
Word Recognizer Output		TTL-level signal output by mainframe BNC connector. 4 Master clock cycles after trigger event, signal goes and remains high.

Table 1-4
91A24 AND 91AE24 ELECTRICAL SPECIFICATIONS: PROBE INTERFACE AND SUPPORT

Characteristic	Performance Reqmnts.	Supplemental Information
Probe-to-Module Signals		8 data (91A24 & 91AE24), 1 clock, 1 qualifier (91A24 only)
Module-to-Probe Signals		
Threshold Reference Voltage		
Fixed (TTL)		+1.40 V
Variable (VAR)		−6.40 V to +6.35 V in 50 mV steps. Default is −1.30 V.
TTL and VAR Threshold Accuracy (to input of attached probe)	Indicated value ± 0.5%, ± 65 mV	

91A24 AND 91AE24 ENVIRONMENTAL SPECIFICATIONS

The environmental specifications for the operation of this instrument meet or exceed those specified for the operation of the DAS9109 Mainframe and the DAS9129 Mainframe. For details, refer to the *DAS 9100 Series Operator's Manual*.

Table 1-5
P6460 ELECTRICAL SPECIFICATIONS

Characteristic	Description
User's Ground Sense	<100 Ω to user's ground
Input Impedance	1 MΩ ± 1%, 5 pF nominal; lead set adds approx. 5 pF
Max. Non-Destructive Input Voltage Range	±40 V (dc + peak ac)
Max. Voltage Between Any Two Inputs	±60 V (dc + peak ac)
Operating Input Voltage Range	From −40 V to input threshold's voltage + 10 V (+30 V for RS-232 only)
Threshold Offset and Accuracy	±0.25% of threshold ±50 mV
Minimum Input Swing	0.5 V p-p centered on the threshold
Minimum Pulse Width (with input 250 mV over the threshold from +0.5 V and −0.5 V)	4 ns at threshold

Table 1-6
P6460 ENVIRONMENTAL
SPECIFICATIONS

Characteristic	Description
Temperature Operating Storage	$-15°C$ to $+55°C$ $-62°C$ to $+75°C$
Humidity	95% to 97% relative humidity
Altitude Operating Non-operating	4.5 km (15,000 ft.) 15 km (50,000 ft.)
Electrical Discharge	5 kV maximum from 200 pF with 2 kΩ series resistance

Table 1-7
P6460 PHYSICAL SPECIFICATIONS

Characteristic	Description
Weight	340 g (12 oz.)
Overall Dimensions	
Pod	11.4 cm (4.5 in.) long, 5.6 cm (2.2 in.) wide, 2.2 cm (0.85 in.) deep
Cable	2 m (78.8 in.) $\pm10\%$

Table 1-8
P6462 ELECTRICAL SPECIFICATIONS

Characteristic	Performance Reqmnts.	Supplemental Information
Interface Presented to the User's System Input Capacitance		8 pF nominal
Max. Non-Destructive Input Voltage Range		−2 to +7 V (DC + peak AC)
Low-Level Input Current		−0.18 mA max.
High-Level Input Current		10 μA max.
Minimum Input Signal	TTL (0.8 to 2.0 V)	
Nominal Threshold Voltage		1.4 V at 25° C w/Vcc = 5.000 V ±5 mV
Threshold Temperature Dependence		5.5 mV/deg. C (referenced to 25 deg. C)
Threshold Temperature Power Supply Voltage Dependence (delta V-th/delta V-cc)		one-to one
Minimum Pulse Width (with min TTL signal input centered around the threshold and rise and fall times ≤ 2 ns)		10 ns at threshold
Internal Probe Characteristics Bandwidth Clock Channel Independent Input Channel		 50 MHz 25 MHz

Table 1-9
P6462 ENVIRONMENTAL
SPECIFICATIONS

Characteristic	Description
Temperature Operating Storage	-15°C to +55°C -62°C to +85°C
Humidity	95% to 97% relative humidity
Altitude Operating Non-operating	4.5 km (15,000 ft.) 15 km (50,000 ft.)
Electrical Discharge	10 kV maximum from 200 pF with 2K Ω series resistance

Table 1-10
P6462 PHYSICAL SPECIFICATIONS

Characteristic	Description
Weight	340 g (12 oz.)
Overall Dimensions	
Pod	4.5 in. long, 2.2 in. wide, 0.85 in. deep
Cable	78.75 in. (2 m)

OPTIONS

There are no options to the 91A24 Data Acquisition Module, the 91AE24 Data Acquisition Module, the P6460 Data Acquisition Probe, or the P6462 Data Acquisition Probe. For information regarding DAS system options, refer to the *DAS 9100 Series Service Manual*.

OPERATING INSTRUCTIONS

This section describes the installation and basic operation of 91A24 and 91AE24 modules. For detailed operating instructions refer to the *91A24, 91AE24, and P6460 Operator's Manual Addendum* to the *DAS 9100 Series Operator's Manual.*

Repackaging Information. All DAS 9100 Series products are shipped in specially designed transportation packaging. If you need to ship a product, use its original packaging. If the original packaging is no longer fit for use, contact your nearest Tektronix Field Office and obtain new DAS packaging.

If you need to ship any part of your 91A24/91AE24 system to a Tektronix Service Center, always include all components of the system: both your 91A24 and 91AE24 modules, and their P6460 probes and grabber-tipped leads.

When you ship a product to a Tektronix Service Center, be sure to attach an identifying tag to the product (inside the packaging). On this tag include your name, the name of your company, the name and serial number of the enclosed product, and a description of the service requested.

FIRMWARE AND HARDWARE COMPATIBILITY

Firmware Update Requirements. To operate with 91A24/91AE24 modules, your DAS must be equipped with firmware version 1.11 or higher. If your DAS has a lower firmware version, it will display the error message NEEDS FIRMWARE VERSION > = 1.11 at power-up. You can determine your mainframe's firmware version by looking in the upper right corner of the power-up display.

Firmware version 1.11 requires that 91A04 modules be equipped with version 2 (or higher) firmware. You can determine if your 91A04 has the correct firmware by checking the 91A04 listing on the DAS powerup display: V2 (or higher) should appear at the right of this line.

To obtain version 1.11 update kits for your mainframe and/or 91A04, contact your Tektronix representative.

Hardware Update Requirements. For use with 91A24/91AE24 modules, your DAS system may require certain hardware updates. These updates can be performed by your Tektronix Service Center, or you can order the appropriate DAS hardware update kit. The following updates are necessary:

- DAS mainframes with serial numbers lower than B030100 require a controller board modification.
- 91A08 modules with serial numbers lower than B020100 require modification to operate in 91A24 ARMS 91A08 mode.
- PMA 100 Personality Module Adapters with serial numbers lower than B020100 require a new backpanel label.

Should any of your equipment require an update, contact your Tektronix representative.

MODULE INSTALLATION

NOTE

For information on setting up the modules for functional or performance checks, see Section 5, Verification and Adjustment Procedures *in this addendum.*

The following paragraphs describe the installation requirements for the 91A24 and 91AE24 modules and their probes. Operator's checkout procedures are discussed later in this section.

Throughout the following discussion, it is assumed that you are already familiar with the procedures for removing the mainframe top panel and module compartment cover, and with the procedures for installing modules into the mainframe bus slots. If you are not familiar with these procedures, refer to *Section 3, Operating Instructions* of the *DAS 9100 Series Service Manual.*

Do not remove or install a 91A24 or 91AE24 module until you have read the following warnings, cautions, adjustment procedures, and configuration requirements.

{ *CAUTION* }

When you install instrument modules, turn off the mainframe and unplug it from its power source. You may damage the module's circuitry if the mainframe is receiving power while you install a module.

CONFIGURATION REQUIREMENTS

The power and configuration requirements for the 91A24 and 91AE24 modules are as follows:

1. The 91A24 module can only share a +5 V Power Supply with a 91A32, 91AE04, or 91AE24 Data Acquisition Module, or an empty bus slot. It cannot share a power supply with any other type of module.

{ *CAUTION* }

If the 91A24 is installed in a bus slot sharing a +5 V Power Supply with any type of module other than those specified above, the +5 V Power Supply may lose voltage regulation, causing the DAS modules to malfunction.

When positioning modules around the 91A24, be sure to allow for the power supply restriction. Table 3-1 shows the recommended positioning of 91A24 and 91AE24 modules.

You can see which power supplies are present in the mainframe by checking the chrome pins visible through holes in the black cover over the power supply area. A +5 V power supply is present if a chrome pin is visible in the hole. The label next to each power supply indicator tells which bus slots that power supply supports. See *Section 6, Maintenance: General Information* of the *DAS 9100 Series Service Manual* for instructions on removing power supply area cover.

2. Without violating the power supply restriction, the 91A24 and 91AE24 modules must be positioned in adjacent bus slots. All 91AE24 modules must be positioned to the same side (either all to the right or all to the left) of the 91A24 module. Table 3-1 shows one possible bus slot positioning for 91A24 and 91AE24 modules.

Table 3-1
RECOMMENDED BUS SLOT PLACEMENT

Bus Slot	Module
0	Controller
1	91A24 Data Acquistion Module
2	91AE24 Data Acquisition Module
3	91AE24 Data Acquisition Module
4	91AE24 Data Acquisition Module
5	Any module other than a 91A24, or a 91AE24, or empty bus slot
6	Any module other than a 91A24, or a 91AE24, or empty bus slot
7	Trigger/Time Base

MODULE INTERCONNECTION PROCEDURES

When one or more 91AE24 expander modules are installed in the mainframe, interconnect pins on the top edge of the modules are used to communicate word recognizer and clock signals.

Each 91AE24 module comes with seven 3-inch twisted-pair cables. These cables connect the 91A24 and 91AE24 modules' word recognizer and clock interconnect pins. In addition, some of the 91A24's square-pin jumpers move to interconnect pins on the 91AE24 furthest from the 91A24. Interconnect cables and square-pin jumpers must be correctly installed for the modules to operate properly.

Figure 3-1 illustrates how these cables are connected.
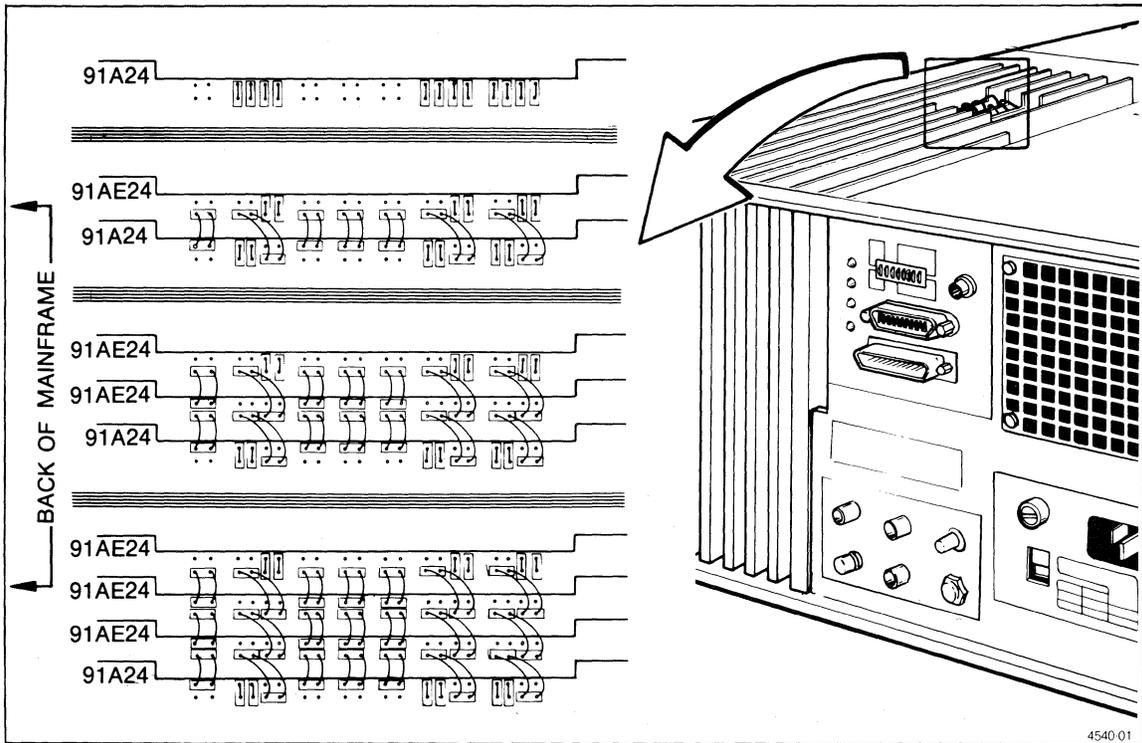
Figure 3-1. Connecting the cables between the 91A24 and 91AE24 modules. This illustration shows correct configurations of interconnect cables and square-pin jumpers. Four possible cases are shown: a 91A24 without 91AE24s, and configurations with one, two, and three 91AE24s installed.

Sync Output Cable. The 91A24 module comes equipped with a 2-meter coaxial cable. This cable is used to carry a TTL sync-output signal. The signal can be synchronized with the occurrence of events defined in the Trigger Specification sub-menu's sequential word recognizer.

The sync-output cable is connected to the 91A24 through back-panel openings on the mainframe.

The cable plug-in jack is located on the back edge of the 91A24 module, immediately below the pod C connector. Connection of the sync-output cable is shown in Figure 3-2.

4540-02
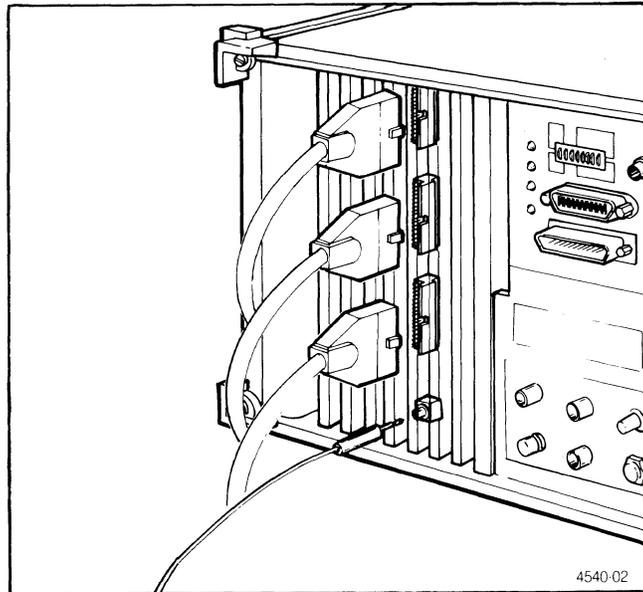
Figure 3-2. Connecting acquisition probes and the sync output cable.

CONNECTING ACQUISITION PROBES

You can use either P6460 or P6462 Data Acquisition Probes with 91A24/91AE24 modules. All probes must be of the same type. All probes connect to the 91A24 and 91AE24 modules through back-panel openings on the mainframe as shown in Figure 3-2. The probes attach to the modules' Pod A, Pod B, and Pod C connectors.

To connect probes to modules:

1. Grasp the probe by its cable holder.
2. Align the cable holder with the module's pod connector. Be sure the raised tab on the cable holder is facing towards bus slot 0, and is aligned with the opening on the module's pod connector.
3. Gently push the cable holder onto the connector. Do not force the connection.

    To disconnect the probe, grasp the cable holder and pull gently.

CAUTION

You may damage the probe if you try to disconnect it by pulling on the cable rather than the cable holder.

P6460 PROBE CHARACTERISTICS

The P6460 is a 100 MHz, 9-channel data acquisition probe. Each P6460 provides the 91A24 module with eight data input channels, one qualifier channel, and one clock channel. When connected to a 91AE24 module, only the data channels are active. For P6460 specifications and signal characteristics, refer to Table 1-5.

Figure 3-3 illustrates the various elements and features of the P6460 probe.
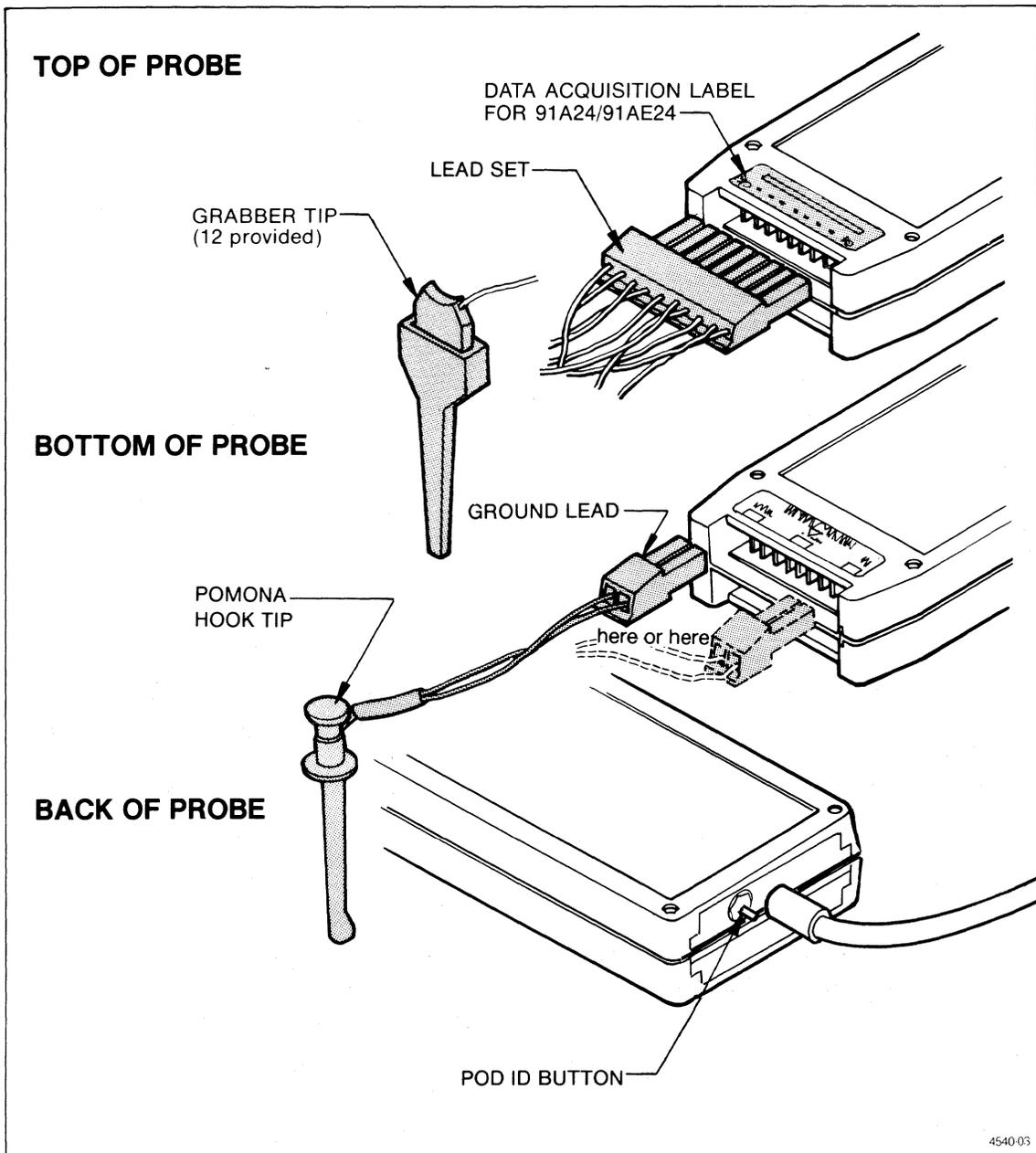
Figure 3-3. P6460 Data Acquisition Probe characteristics and lead connections.

P6462 PROBE CHARACTERISTICS

The P6462 is a 50 MHz, 9-channel data acquisition probe. Each P6462 provides the 91A24 module with eight data input channels, one qualifier channel, and one clock channel. When connected to a 91AE24 module, only the data channels are active. For P6462 specifications and signal characteristics, refer to Table 1-8.

Unlike the P6460, the P6462 has a NORM/AUX switch. For use with the DAS, set this switch to AUX. Also unlike the P6460, the P6462 has a flat ribbon cable instead of a round cable. With these exceptions, Figure 3-3 represents major P6462 features and accessories.

OPERATOR'S CHECKOUT PROCEDURE

The following paragraphs describe basic operator's checkout procedures. For more detailed instructions refer to the *DAS 9100 Series Operator's Manual.*

POWER-UP SELF TEST

When the DAS mainframe is powered up, any installed 91A24 and 91AE24 modules will be listed on the power-up configuration display. A PASS or FAIL notation will appear next to each module to denote the results of that module's power-up testing. Table 3-2 lists the power-up errors for the 91A24 and 91AE24 modules.

Table 3-2
POWER-UP ERROR CONDITIONS

Error Condition	Definition
91A24 Data Acquisition Module FAIL	The 91A24 module has failed the power-up test. The module will not operate properly.
	This failure does not affect the operation of any installed pattern generation modules or other data aqcuisition modules, except for 91AE24s. 91AE24 modules will not operate without a working 91A24 module.
91AE24 Data Acquisition Module FAIL	The 91AE24 module has failed the power-up test. The module will not operate properly.
	This failure will occur if the clock and word recognizer jumpers and cables are disconnected or configured incorrectly. Power down the mainframe, check the cables and jumpers, then power up the mainframe.
	This failure does not affect the operation of the 91A24 module, other 91AE24 modules, any other data acquisition modules, or any pattern generator modules.

PROBE SELF-TEST

The general procedure for the probe self-test is described in the *DAS 9100 Series Operator's Manual*. Testing P6460 and P6462 probes requires modifications to the main test that are described in this section.

- The 91A24/91AE24 modules may be in any valid slots (restrictions are detailed under *Configuration Requirements*, earlier in this section). The probe may be connected to any 91A24 or 91AE24 pod connector.

- If you are testing a P6462, set the NORM/AUX switch to NORM. Leave the Channel Specification menu threshold value set to TTL +1.40 V (the default value).

- If you are using a P6460, there is no NORM/AUX switch to set. If you are getting the test pattern through a P6455 TTL/MOS pattern generator probe, leave the Channel Specification menu threshold value set to TTL +1.40 V (the default value). If you are getting the test pattern through a P6455 ECL pattern generator probe, set the threshold to VAR -1.30 V.

- When you enter the Timing Diagram menu to see the test results, you will need to change the value of the POD field to match the 91A24 bus slot and the pod where you have the probe connected. For example, if the 91A24 is in slot 1, and the probe is in pod A, enter 1A in the POD field).

In all other respects, this procedure is identical to the one detailed in the *DAS 9100 Series Operator's Manual*.

THEORY OF OPERATION

SECTION ORGANIZATION

This section is designed to familiarize service personnel with the operation of 91A24 and 91AE24 circuitry. It is divided into three main parts. The *System Architecture* part describes how 91A24 and 91AE24 modules fit into the DAS architecture. The *General System Description* describes both modules at the function block level. Last is the *Detailed Circuit Description*, which describes the module operation at the component level.

Throughout this section, references are made to the 91A24 and 91AE24 block diagrams and schematics located in the *Diagrams* section at the back of this addendum. The schematic and block diagram pages have tabs indicating the page title and, on schematics, the numbered diamond assigned to the schematic. Schematics are often referred to by the numbered diamond on the schematic tab.

For a more complete understanding of the 91A24 and 91AE24 modules, you may also want to refer to the signal glossary in the *Reference Information* section and to the diagnostic information in the *Maintenance: Troubleshooting* section.

LOGIC CONVENTIONS

In this manual, digital logic is described using the positive logic convention. The more positive voltage indicates a true or 1 state; the more negative voltage indicates a false or 0 state. In logic descriptions, the more positive voltage is referred to as high, and the more negative voltage is referred to as low. The specific voltage that specifies a high or low state varies depending on the type of logic device. TTL, ECL, and CMOS devices all have different logic threshold levels.

Signal names on schematics are normally asserted high. Only signal names with overscores are asserted low. This same convention is used in the text.

SYSTEM ARCHITECTURE

91A24 and 91AE24 Data Acquisition Modules are designed to reside in any of the instrument bus slots (1 through 6) of any DAS 9100 mainframe. All 91A24 and 91AE24 modules should be placed in adjacent bus slots. The mainframe must contain firmware version 1.11 or higher, along with the hardware changes associated with the firmware version. More information on firmware version 1.11 is located in the *Operating Instructions* section of this addendum.

Both types of modules are initialized and read by the Controller board in the DAS mainframe. The firmware that allows the Controller board to operate the modules is located on the 91A24. Some of the 91A24 trigger circuitry is located on the Trigger/Time Base board, which also provides the clock for asynchronous acquisition.

91A24 DATA ACQUISITION MODULE

The 91A24 module is a 24-channel data acquisition module with a maximum clock rate of 100 ns. The 91A24 can take two separate samples within the 100 ns period, however, so its maximum sample rate is 20 MHz. The acquisition memory is 1023 words deep. Only one 91A24 module may be installed in a mainframe at one time, but the memory and trigger word can be widened by connecting 91AE24 modules to the 91A24 module.

The 91A24 has five independent word recognizers, one of which is stack-based so it can look for different words at different points in the trigger sequence. The four non-stack-based word recognizers may be used as either trigger conditions or as data qualifiers to selectively store only certain data.

When external clocks are used, the 91A24 can create a separate sample clock for each acquisition probe. Each clock controls when data is stored from its probe. The clocks are created from boolean expressions combining any of the three clock inputs and three qualifier inputs.

The 91A24 also provides signals and connectors to drive 91AE24 modules. The 91A24 sends clock signals to the 91AE24 modules. The 91A24 module also receives word recognition signals from the 91A24. These signals are transmitted through cables attached to the top of all the modules.

Probes. Full use of the 91A24 module requires three data acquisition probes. Each probe acquires eight channels of data, one clock qualifier, and one clock.

At this writing, P6460 and P6462 Data Acquisition Probes can be used with 91A24 modules. However, only one type of probe should be used with any set of 91A24 and 91AE24 modules at a given time. P6460 and P6462 probes have different propagation delays, so if probe types are mixed, setup and hold times may be violated.

91AE24 DATA ACQUISITION MODULE

The 91AE24 module is a depopulated version of the 91A24 module. The 91AE24 receives its clocks from the 91A24 module and sends word recognition signals back to the 91A24. The 91A24 determines when storage should occur and when trigger conditions are met. As many as three 91AE24 modules can be controlled by a 91A24. The wires that carry the controlling signals are daisy-chained across the top of all the modules.

Probes. Each 91AE24 module accepts up to three data acquisition probes. All 91AE24 modules should use the same type of probe that the 91A24 uses. If probe types are mixed, setup and hold times may be violated.

GENERAL SYSTEM DESCRIPTION

The function blocks used in this description are shown in the 91A24 and 91AE24 block diagram in the *Diagrams* section of this addendum. Refer to the block diagram while reading the description.

91A24 DATA ACQUISITION MODULE

91A24 Controller Interface and ROMs

The controller interface allows communication between the DAS Controller board and the 91A24. Any block in the 91A24 general block diagram identified with an asterisk (*) uses the 91A24 controller interface.

The three ROMs in the controller interface are read by the Controller board to control the 91A24 and any 91AE24 modules in the mainframe.

Data Acquisition Probes

The 91A24 uses three data acquisition probes. Each probe acquires eight data channels. Each probe also accepts one clock signal and one clock qualifier signal, for a total of three clocks and three qualifiers. Each probe is an active device that converts unbalanced signals to differential ECL signals for transmission to the acquisition module.

Probe Receivers

The 91A24 receives differential ECL signals from the probes. The probe receivers convert data signals from the probes into TTL level signals. The probe receivers also buffer the clock and qualifier signals out of the probes, but these signals remain differential ECL.

Clock Qualifier Generator

Before the 91A24 starts acquiring data, the Controller board programs the clock qualifier generator to pass the correct qualifier signals from the probes to the clock generator. The clock generator requires three qualifier signals per clock, and any of the three signals may be inverted, non-inverted, or don't cared. So the clock qualifier generator sends a total of nine clock qualifiers to the clock generator.

Clock Generator

The clock generator is programmed to create the three clocks that clock data from the probe receivers into the login registers. The clocks created match the clock expressions entered in the 91A24 Clock Specification sub-menu of the Trigger Specification menu. Clocks can be generated from the three external clocks acquired by the 91A24, or from the internal clocks from the Trigger/Time Base board.

The qualifiers in the clock expressions are received from the clock qualifier generator, where they are conditioned to match the expressions in the 91A24 Clock Specification sub-menu.

The three clocks from the clock generator regulate the acquisition circuitry on the 91A24 and all 91AE24 modules in the system. The clocks are sent to the 91AE24 modules through three of the wires running across the tops of the modules.

The clock generator also selects the 91A24 master clock from the three generated clocks. This master clock runs the data registers, the word recognizers, and the acquisition memory.

Login Registers

The login registers latch data from the probe receivers, so that stable data can be clocked into the data registers. The login registers operate from three separate clocks; one clock for the data from each probe.

When required, the login registers also demultiplex data from probe A into both the A and B memories. This is also the point where diagnostics can enter the 91A24 data stream for diagnostic testing.

Data Registers

The data registers clock in data from the login registers. The data registers prepare the acquired data for the word recognizers and for storage in the acquisition memory.

Data Qualifier

The data qualifier contains four independent word recognizers as well as the logic that determines the 91A24's response to a recognized word.

The four words to be recognized are loaded into the word recognition RAM by the controller interface. The controller interface programs the logic to control how the module will react to a recognized word.

The data qualifier only recognizes a word when all 91A24 and 91AE24 modules recognize their portions of a word at the same time. The 91AE24 modules indicate qualifier recognition through wires running to 91A24 J176 and J178.

Signals from the data qualifier block control the trigger block, the memory address register for the acquisition memory, and the stack pointer for the stack word recognizer. The signal to the trigger block completes the 91A24 trigger sequence. The signal to the memory address register starts or stops incrementing the acquisition memory address, which starts or stops data acquisition. The signal to the stack pointer resets the stack pointer to zero so the stack word recognizer restarts its sequence.

The data qualifier also stops storage when acquisition is done. When the trigger sequence is finished, the 91A24 signals the Trigger/Time Base to start its delay counter. When the delay counter is done, the Trigger/Time Base pulls the 91A32 QUAL signal on the Interconnect low. When this signal is low, the data qualifier stops the 91A24 memory address register from incrementing, which stops data storage.

Memory Address Register

The memory address register is a 10-bit counter that is clocked by the master clock. The counter provides the address for the acquisition memory.

The data qualifier can prevent the memory address register from incrementing. When the memory address register stops incrementing, the same acquisition memory address is reloaded each time new data is clocked in, which effectively stops data acquisition.

Acquisition Memory

The acquisition memory stores data from the data registers once every master clock cycle. The memory address register determines the address of the acquisition RAM.

Stack Word Recognizer

The stack word recognizer is capable of recognizing sixteen separate words. The stack pointer determines which of the sixteen words is active at a given time. Each time the active word is recognized, the stack word recognizer increments the stack occurrence counter.

The stack word recognizer also includes a RAM that determines the 91A24 reaction to each stack level. One bit causes the SYNC OUT output to go active, two bits start and stop the stack counter/timer, and one bit activates the 91A24 trigger.

Stack Occurrence Counter

The stack occurrence counter determines the number of times each word in the stack word recognizer must occur before moving to the next stack level.

The stack occurrence counter has two parts; the count RAM and the counter. Whenever the 91A24 starts, or enters a new stack level, a new count value is loaded from the count RAM into the counter. The stack pointer addresses the count RAM, so values loaded from the RAM into the counter correspond to the new stack level.

The stack word recognizer increments the counter each time it recognizes the word for the current stack level. The counter only increments when the stack word from the 91A24 and from all 91AE24 modules is satisfied. J171 carries stack word recognition signals from 91AE24 modules to the 91A24. When the counter runs out, it increments the stack pointer, which moves the stack word recognizer down another level.

Stack Pointer

The stack pointer sets the stack word recognizer level. Initializing the 91A24 sets the stack pointer to zero (level 1 of the sequential word recognizer in the 91A24 Trigger Specification sub-menu).

When the stack occurrence counter completes a level, it increments the stack pointer. So whenever the conditions for one stack level are completed, the stack occurrence counter moves the pointer to the next level. The signal that increments the 91A24 stack pointer is also sent to all 91AE24 modules, through J181, so they increment their stack pointers at the same time.

The stack pointer can also be set back to zero by the data qualifier. This happens whenever the data qualifier recognizes the RESET word in the 91A24 Trigger Specification sub-menu.

Stack Counter/Timer

Before acquisition begins, the stack counter/timer is initialized to act either as a counter or as a timer. If it acts as a timer, a 10 MHz oscillator drives the counter. In this configuration, the 10 MHz oscillator starts incrementing the counter when a RUN TIMER stack level is entered. The counter stops incrementing when a STOP TIMER level is completed or when the 91A24 triggers. When the counter/timer is initialized to act as a counter, the counter increments each time the INCR CNTR stack level is completed.

The counter/timer has 16 bits, but the 91A24 uses the DAS Z80 to extend the maximum count. Whenever the counter wraps around, the Z80 on the Controller board receives an interrupt. This interrupt causes the Z80 to increment a word in the Controller RAM. When the 91A24 stops acquisition, the Controller board adds the value from the counter to the value in the Controller RAM. This sum is the total elapsed time or the total count displayed on the DAS screen.

Trigger

The trigger is programmed to monitor triggering conditions. When the trigger conditions are met, the trigger pulls the EVENT 1 signal on the Interconnect low. This signals the Trigger/Time Base board that the 91A24 trigger has occurred. The Trigger/Time Base then finishes the acquisition stopping sequence with its delay counter. When the Trigger/Timer Base delay counter is done, the Trigger/Time Base stops the 91A24 module from acquiring more data by pulling the 91A32 QUAL signal on the Interconnect low.

Memory Readback

The memory readback circuits place the data in the 91A24 acquisition memory onto the Interconnect's CPU bus. The Controller board then processes and displays this data on the DAS screen.

91AE24 DATA ACQUISITION MODULE

All 91AE24 modules are driven by the 91A24 module. The 91A24 sends clocks and control signals to the 91AE24 modules. The 91AE24s return word recognition signals to the 91A24 for processing.

91AE24 Controller Interface

The controller interface allows communication between the DAS Controller board and the 91AE24. Any block in the 91AE24 general block diagram identified with an asterisk (*) uses the 91AE24 controller interface.

Data Acquisition Probes

The 91AE24 uses three data acquisition probes. Each probe acquires eight data channels. Probes attached to a 91AE24 do not acquire clock or qualifier signals, since the clocks for 91AE24 modules are created by the master 91A24. Each probe is an active device that converts unbalanced signals to differential ECL signals for transmission to the acquisition module.

Probe Receivers

The 91AE24 receives differential ECL signals from the probes. The probe receivers convert data signals from the probes into TTL level signals. 91AE24 modules do not use the probe's clock and qualifier channels.

Clock Generator

The 91AE24 clock generator buffers the three pod clocks received from the 91A24. The clock generator also selects the 91AE24 master clock from the three received clocks. This master clock runs the data registers, the word recognizers, and the acquisition memory.

Login Registers

The login registers latch data from the probe receivers, so that stable data can be clocked into the data registers. The login registers operate from three separate clocks; one clock for the data from each probe. The 91AE24 receives these clocks from the 91A24 through the wires attached to the top of the modules.

When required, the login registers also demultiplex data from probe A into both the A and B memories. This is also the point where diagnostics can enter the 91A24 data stream for diagnostic testing.

Data Registers

The data registers clock in data from the login registers. The data registers prepare the acquired data for the word recognizers and for storage in the acquisition memory.

Data Qualifier

The data qualifier contains four independent word recognizers as well as the logic that determines the 91AE24's response to a recognized word.

The four words to be recognized are loaded into the word recognition RAM by the controller interface. The controller interface programs the logic to control how the module will react to a recognized word.

The data qualifier only recognizes a word when all 91A24 and 91AE24 modules recognize their portions of a word at the same time. The 91A24 and 91AE24 modules share their qualifier recognition signals through wires running to J176 and J178.

Signals from the data qualifier block control the memory address register for the acquisition memory, and the stack pointer for the stack word recognizer. The signal to the memory address register starts or stops incrementing the acquisition memory address, which starts or stops data acquisition. The signal to the stack pointer resets the stack pointer to zero so the stack word recognizer restarts its sequence.

The data qualifier is also stops acquisition when the trigger is completed. When the trigger sequence is finished, the 91A24 signals the Trigger/Time Base to start its delay counter. When the delay counter is done, the Trigger/Time Base pulls the 91A32 QUAL signal on the Interconnect low. When this signal is low, the data qualifier stops the 91AE24 memory address register from incrementing, which stops data storage.

Memory Address Register

The memory address register is a 10-bit counter that is clocked by the master clock from the 91A24. The counter provides the address for the acquisition memory.

The data qualifier can prevent the memory address register from incrementing. When the memory address register stops incrementing, the same acquisition memory address is loaded each time new data is clocked in, which effectively stops data acquisition.

Acquisition Memory

The acquisition memory stores data from the data registers once every master clock cycle. The memory address register determines the address of the acquisition RAM.

Stack Word Recognizer

The stack word recognizer is capable of recognizing sixteen separate words. The stack pointer determines which of the sixteen words is active at a given time. Each time the active word is recognized, the stack word recognizer sends a signal to the 91A24 module.

Stack Pointer

The stack pointer sets the stack word recognizer level. Initializing the 91AE24 sets the stack pointer to zero (level 1 of the sequential word recognizer in the 91A24 Trigger Specification sub-menu).

The 91A24 module sends a signal to all 91AE24 modules whenever the 91A24 stack pointer increments. This signal increments all 91AE24 stack pointers so they stay at the same level as the 91A24.

The stack pointer can also be set back to zero by the data qualifier. This happens whenever the data qualifier recognizes the RESET word in the 91A24 Trigger Specification sub-menu.

Memory Readback

The memory readback circuits place the data in the 91AE24 acquisition memory onto the Interconnect's CPU bus. The Controller board then processes and displays this data on the DAS screen.

DETAILED CIRCUIT DESCRIPTION

Refer to schematics in the *Diagrams* section of this manual while reading this detailed circuit description. The numbered diamonds on the schematic tabs in the *Diagrams* section are keyed to the numbered diamonds in the detailed circuit descriptions.

Signal names which are asserted low are indicated with an overscore on the schematics and in the text. Signal names are assumed to be asserted high unless otherwise indicated.

Table 4-1 shows the assembly numbers of all etched circuit boards referred to in this circuit description. These assembly numbers are used to identify the board or assembly where a component is mounted. For example, A35Q101 is transistor Q101 located on the 91A24 module (A35).

NOTE

Assembly numbers are etched or printed on circuit boards when possible. Boards that are supplied by a vendor or special Tektronix boards may not have assembly numbers etched on them. Boards may be located using the board locator illustrations in the Diagrams *section of this addendum or the DAS 9100 Series Service Manual.*

Table 4-1
ASSEMBLY NUMBERS

A1	DAS9109 Interconnect
A6	DAS9109 Monochrome Controller board
A10	Trigger/Time Base board
A31	DAS9129 Interconnect
A33	DAS9129 Color Controller board
A35	91A24 Data Acquisition module
A36	91AE24 Data Acquisition module
A70	P6460 Data Acquisition Probe
A71	P6462 TTL Fixed Threshold Acquisition Probe

91A24 DATA ACQUISITION MODULE

The 91A24 Data Acquisition Module can acquire 24 independent channels of information at speeds up to 10 MHz. The 91A24 module also has five word recognizers, one of which is stack-based. The module stores up to 1023 data sequences.

All component numbers in the 91A24 module circuit description are assumed to have an A35 preface unless otherwise noted.

The 91A24 circuit description is organized by schematic, and then by functional blocks on the schematic. Numbers in diamonds refer to the numbers on schematic tabs in the *Diagrams* section of this addendum. Refer to those schematics while reading the circuit description. For an overview of the 91A24 module's circuits, refer to the *General System Description*, earlier in this section.

91A24 CONTROLLER INTERFACE ⟨68⟩

The controller interface allows communication between the DAS Controller board and the 91A24. Any block in the 91A24 block diagram identified with an asterisk (*) uses the 91A24 controller interface.

The 91A24 controller interface performs two major functions:

1. It takes data from the DAS Controller board and writes it to appropriate 91A24 registers. The registers are selected by decoding the lowest five bits on the address bus and interpreting $\overline{\text{BWR}}$, $\overline{\text{BPORT}}$, and $\overline{\text{BRD}}$ from the DAS Controller board.

2. It puts data from the 91A24 module on the data bus at the command of the DAS Controller board.

91A24 interface decoding and receiving circuitry is shown on schematic 68; readback circuitry is shown on schematic 69.

Receiving Control Data. As an example of how the 91A24 receives control data, suppose the Controller board is writing data into port 0, the map register (U968 on schematic 68). The Controller board sets the low five bits of the address bus to 00_{16}, places the data on the data bus, and asserts $\overline{\text{BWR}}$ and $\overline{\text{PORT}}$. The 91A24 reacts as follows:

1. Asserting $\overline{\text{PORT}}$ enables U768 (schematic 68). This transmits data from the data bus to the D inputs of the map register.

2. $\overline{\text{BWR}}$, $\overline{\text{PORT}}$, and A4 being low together enable decoder U958 (schematic 68).

3. U958 decodes the 0_{16} on A0-A3 to assert the $\overline{\text{MAP REG}}$ signal. The rising edge when $\overline{\text{MAP REG}}$ is unasserted clocks the value on the data bus into the map register. Waiting for the rising edge of $\overline{\text{MAP REG}}$ allows adequate setup time for the data on the data bus.

Sending Data. The readback procedure is similar, except $\overline{\text{BRD}}$ is asserted instead of $\overline{\text{BWR}}$. As an example of how the 91A24 sends data, suppose the Controller is reading the card ID from port 0 (register U791 on schematic 69). There are only 16 readback ports, so only address bits A0-A3 are decoded. The Controller board sets the low four bits of the address bus to 0_{16}, and asserts $\overline{\text{BRD}}$ and $\overline{\text{PORT}}$. The 91A24 reacts as follows:

1. $\overline{\text{BRD}}$ and $\overline{\text{PORT}}$ being low together enable decoder U998 (schematic 69).

2. U998 decodes the 0_{16} on the address bus to assert the $\overline{\text{CARD ID}}$ signal. The $\overline{\text{CARD ID}}$ signal enables tri-state buffer U791, which places the card ID on the data bus.

There are three exceptions to the read process. When ports 2 (DATA CLOCK), 8 ($\overline{\text{CNTR CLR}}$) and F ($\overline{\text{INT3 CLR}}$) are read, the Controller board does not expect to read any data back. Reading port 2 clocks serial probe status information out of the probes (on schematic 69). Reading port 8 clears the counter/timer (on schematic 76), and reading port F clears the INT3 register (U491B on schematic 76).

Table 4-2 shows which registers are connected to the data bus and the $\overline{\text{BWR}}$, $\overline{\text{BRD}}$, and $\overline{\text{PORT}}$ signals.

Table 4-2
91A24 CONTROLLER INTERFACE MAP

Hex Addr	BWR	BRD	PORT	Line Name	ICs Affected U Number	Schem
XXX0	X	L	L	CARD ID	U791	69
XX00	L	X	L	MAP REG	U968	68
XXX1	X	L	L	POD STATUS	U775	69
XX01	L	X	L	THRESHOLD	U918	71
XXX2	X	L	L	DATA CLOCK	J101, J401, J701	69
XX02	L	X	L	PROBE R/W	U925	71
XXX3	X	L	L	MAR LOW	U135	69
XX03	L	X	L	CNTL1	U761	68
XXX4	X	L	L	MAR HIGH	U235	69
XX04	L	X	L	STACK A WE	U148	75
XXX5	X	L	L	CNTR RDBK0	U788	76
XX05	L	X	L	STACK B WE	U248	75
XXX6	X	L	L	CNTR RDBK1	U795	76
XX06	L	X	L	STACK C WE	U448	75
XXX7	X	L	L	DQ STATUS	U778	69
XX07	L	X	L	STACK CNTL	U555	75
XXX8	X	L	L	CNTR CLR	U475C, U198D, U471A, U298B, U585, U588, U478A, U591, U595	76
XX08	L	X	L	OCCR CNTR LD	U265A, U165B, U158, U258, U458	75
XX09	L	X	L	SINGLE STEP	U125, U225, U425	72
XXXA	X	L	L	STACK CNTL RD	U785	69
XX0A	L	X	L	OCCR CNTR RAM LD1	U455	75
XXXB	X	L	L	A MEM RD	U131	69
XX0B	L	X	L	OCCR CNTR RAM LD0	U155, U255	75
XXXC	X	L	L	B MEM RD	U231	69
XX0C	L	X	L	CNTL2	U758	68
XXXD	X	L	L	C MEM RD	U431	69
XX0D	L	X	L	STACK PTR CLK	U568C, U485A, U575D, U571	76
XXXE	X	L	L	TRIGGERED RD	U771	69
XXXF	X	L	L	INT3 CLR	U478A, U168C, U491B	76
XX0F	L	X	L	PADQ WE	U151	74
XX10	L	X	L	PBDQ WE	U351	74
XX11	L	X	L	PCDQ WE	U551	74
XX12	L	X	L	CLK INIT	U291D, U741B, U745B, U751, U841B, U845B, U851B, U478A	78
XX13	L	X	L	PC0	U938	77
XX14	L	X	L	PC1	U935	77
XX15	L	X	L	PC2	U941	77
XX16	L	X	L	PC3	U928	77
XX17	L	X	L	PC4	U945	77
XX18	L	X	L	PC5	U931	77
XX1B	L	X	L	CNTL3	U765	68
XX1E	L	X	L	TIMER CLK	U491A	76
XX1F	L	X	L	OCCR CLK	U165A	75

91A24 CONTROLLER INTERFACE READBACK CIRCUITRY ◇69◇

This schematic shows the tri-state readback buffers that pass data from the 91A24 to the DAS Controller board. Data passes through these buffers from locations throughout the module. The buffers are enabled by U998 (schematic 69). Table 4-2 provides a list of the signals that enable these buffers.

Schematic 69 also shows part of the communication interface to the acquisition probes. 91A24 compatible probes have a serial communication line for probe identification. Data is clocked out of the probes by the DATA CLOCK signal through pin 28 of J101, J401, and J701 (schematic 69). Data is received back from the probes through pin 34 of J101, J401, and J701 (schematic 69). For more information about these signals refer to the probe interface circuit shown on schematic 71.

91A24 PROBE A AND B RECEIVERS ◇70◇

Probe A Receiver

The probe receivers translate signals from the probes into the voltage levels required by the 91A24. The probe receivers convert the eight data channels from the probe into TTL level signals. The two remaining probe channels, the clock and qualifier signals, are left as differential ECL signals.

The clock and qualifier signals from the probe are terminated then buffered by a comparator. Qualifier signals go to schematic 77, and clock signals go to schematic 78.

All eight of the data receivers are identical. They convert differential ECL signals into the TTL signals that the login registers expect. Figure 4-1 shows one of the channels. This description refers to Figure 4-1.
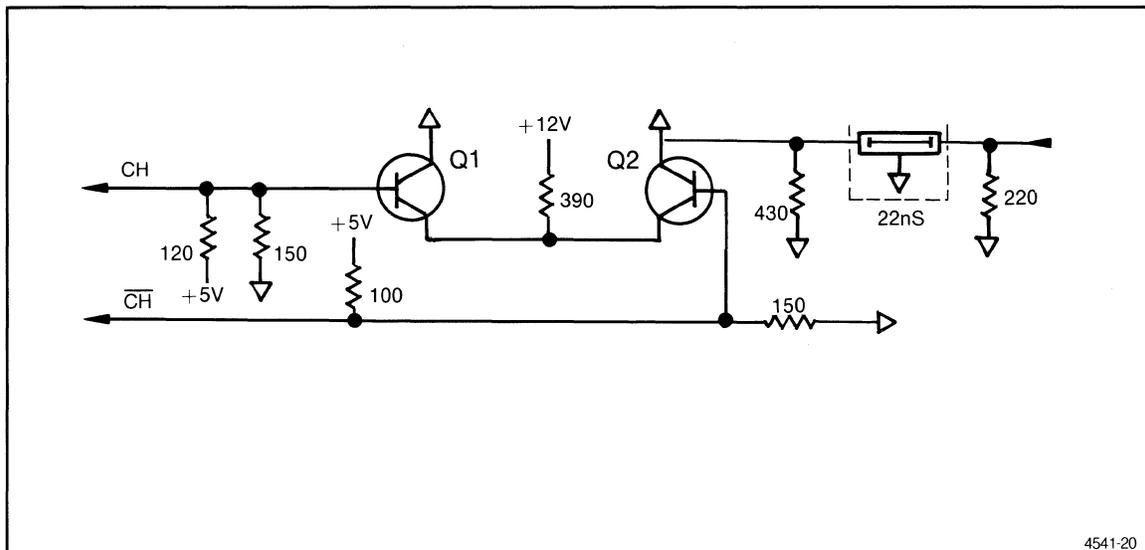
Figure 4-1. 91A24 probe receiver.

Transistors Q1 and Q2 and the 390 Ω resistor are a differential TTL-to-ECL translator. The 150 Ω and 120 Ω resistors are line terminators that match the impedance of the transmission line. The 22 ns delay line adds time to the data signal so the corresponding clock and qualifier signals can be processed before the data is clocked in. The 430 Ω and 220 Ω resistors are signal terminators for the delay line.

Probe B Receiver

The probe B receiver is identical to the probe A receiver. Refer to the probe A receiver description for more information.

91A24 PROBE INTERFACE AND PROBE C RECEIVER ⟨71⟩

Probe C Receiver

The probe C receiver is identical to the probe A receiver. Refer to the probe A receiver description for more information.

Probe Interface

The probe interface controls the probe's acquisition threshold and reads the probe status.

Probe Status Readback. The DAS polls all 91A24 probe connectors to see if probes are attached. The DAS uses the same circuitry to sense if the Pod ID botton is depressed and to identify the type of probe attached. Each probe is identified by an eight-bit code that is received serially by the 91A24.

The DAS polls the probe by pulling the probe's R(L)/W(H) line high. The DAS does this by writing ones into bits 4, 5, and 6 of register U925 (91A24 schematic 71). At this writing, only P6460 and P6462 acquisition probes can be used with the 91A24. Since neither of these probes use the DATA IN signal from the module, bits 0, 1, and 2 of this register are not used.

Once the R(L)/W(H) signal is high, the 91A24 toggles the DATA CLOCK signal through data selector U998 (shown on schematic 69). Each rising edge from DATA CLOCK clocks out one bit of a word from each attached probe. DATA OUT from the probes is read through register U775 (on schematic 69).

When no probe is plugged in, the DATA OUT signal is pulled high by pull-up resistors on the 91A24 module. Any probe plugged into the module pulls this line low, which is how the DAS knows when a probe is plugged in. To read the probe type or monitor the Pod ID button, the 91A24 toggles the DATA CLOCK signal eight times. The first seven serial bits from the probe identify the type of probe and the probe's state. The eighth bit is low when the Pod ID button is depressed.

Probe Threshold DAC. Digital-to-analog converter U918 (on schematic 71) sets the threshold voltage of the 91A24 probes. To program the digital-to-analog converter (DAC), the 91A24 controller interface places a control word on D0-D7 and toggles the $\overline{\text{THRESHOLD}}$ line. Programming the DAC with FF_{16} sets the DAC voltage to $+6.40$ V, while 00_{16} sets the voltage to -6.35 V. If the DAC is programmed with 80_{16}, the DAC outputs 0.00 V.

Potentiometer R902 adjusts the offset of the DAC, so that when the DAC is programmed with 80_{16}, the DAC outputs 0 V. R110 adjusts the DAC gain so that a setting of FF_{16} puts the DAC voltage at $+6.35$ V.

Op amp U808C is configured as an inverting buffer for the DAC output. So the output of U808C, at TP910, is the negative of the voltage from the DAC. Because this is an inverting buffer stage, programming the DAC with FF_{16} results in a probe threshold of -6.35. U808C drives the threshold sensors for the three probes.

Probe Threshold Sensors. There are three probe threshold sensors, one for each probe. Since the three circuits are identical, only the circuit for pod A is described here.

Op amps U711A and D (schematic 71) regulate the threshold for probe A. U711D is configured as a differential amplifier. The inverting input to U711D receives the threshold voltage from the DAC buffer (U808C). The non-inverting side of U711D receives USERS GND from the probe. This arrangement adjusts the output of U711D for differences between the DAS ground and the user's ground. Since the threshold voltage goes to U711D's inverting input, the output voltage is the negative of the desired voltage. The next stage inverts the signal again so the signal from the module has the correct polarity.

Op amp U771A (schematic 71) is also a differential amplifier, but its gain and offset are controlled by the attached probe. The probe provides a feedback resistor between VTHRESH and VTHRESH SENSE so the voltage received from the op amp has the correct gain factor. For example, a P6460 acquisition probe provides a 10,500 Ω feedback resistor which, in parallel with 200K Ω R706, gives the circuit a gain of $-1/4$.

The probe also provides the OFFSET SENSE signal to offset U771A's output voltage into the range required by the probe. For example, a P6460 acquisition probe provides -1.2 V as the OFFSET SENSE, so the output signal is referenced to -1.2 V rather than ground. This op amp is also configured as an inverter, which cancels out the inversion in the previous stage.

91A24 LOGIN REGISTERS ⟨72⟩

Clock Distribution

The clock distribution functional block is where the acquisition clocks generated by the 91A24 are sent to the attached 91AE24 modules. When the 91A24 is operating alone, J173, J183, and J185 (on schematic 72) are jumpered as shown on the schematic. When 91AE24 modules are included in the system, the jumper on pins 7 and 3 and the jumper on pins 8 and 3 are removed, as shown in the schematic inset. A twisted-pair cable runs from pins 7 and 8 to the adjacent 91AE24 module.

Comparators U275A, B, and C in the clock distribution block convert differential ECL into single-ended ECL clock signals. These clock signals are used by the data login registers (on schematic 72) and by the master clock selector (U721 on schematic 77).

V$_{bb}$ Generator

U745D pin 11 (schematic 72) generates an ECL threshold voltage (V_{bb}). ECL-to-TTL converters in the login clock generator block and master clock distribution block use this voltage. Op amp U808B and transistor Q902 form a voltage follower with moderate current handling capabilities. This voltage follower buffers the V_{bb} source and supplies the voltage to the ECL-to-TTL converters.

Login Clock Generator

Transistors Q318, Q319, Q519, Q520, Q628, and Q629 (on schematic 72) are ECL-to-TTL converters. They convert the single-ended ECL clock signals coming from the clock distribution block into clocks for the data and mux mode login registers. ECL buffers U718B, C, and D reduce the interaction between the clock distribution block and the login clock generator.

Login Registers

There are seven login registers (shown on schematic 72), which latch data in to the data storage and word recognition system of the 91A24. Only three of these registers operate at any one time. The login registers operate in three different modes:

1. System data login (U125, U225, and U425), for loading word recognizers and running diagnostics.

2. Probe data login (U118, U221, and U421), for normal acquisition of data from the probes.

3. Probe data login with demultiplexing (U118, U121, and U421), where data from probe A is acquired in both the probe A and the probe B acquisition memories.

System Data Login

The system data login registers (U125, U225, and U425) load data from the DAS Controller into 91A24 word recognizers and data qualifiers. These registers are also used by the diagnostic routines which exercise circuitry at power-up and on command from the Diagnostics menu.

During acquisition, the outputs of these registers are tri-stated by pulling the $\overline{\text{A DIAG EN}}$, $\overline{\text{B DIAG EN}}$ and $\overline{\text{C DIAG EN}}$ signals high. When word recognizers are being loaded or the diagnostics are running on the 91A24, data can be logged into these registers from the controller interface (using the LB0-LB7 bus and the $\overline{\text{SINGLE STEP TTL}}$ signals). Data logged into these registers may then be placed on the LID0-LID23 bus. Data entering the 91A24 data stream at this point is used to test the data registers, the acquisition memory, and all five word recognizers.

Probe Data Login

Registers U118, U221, and U421 (on schematic 72) log in data from the probe receivers (shown on schematics 70 and 71). Clocks created by the the 91A24 clock generator (shown on schematic 78) latch data arriving from the probes into the probe data login registers. The outputs of the probe data login registers are next sampled by the data registers (U128, U228, and U428 on schematic 73).

Whenever any of the system data login registers (U125, U225, and U425 on schematic 72) are used, all the probe data login registers are tri-stated. This tri-stating results from inverting the enable signal for the system data login register. The inverted signal tristates the corresponding probe data login register. For example, $\overline{\text{C DIAG EN}}$ is inverted through U218B. The inversion of $\overline{\text{C DIAG EN}}$ tristates U421 whenever U425 is enabled.

Mux Mode Login

The mux mode login register (U121 on schematic 72) is only used when the 91A24 Clock Specification sub-menu is set to demultiplex data acquired through 91A24 pod A into the acquisition memory and word recognizers for pod B. When demultiplexing is selected,

- Probe A data is clocked into Probe A memory through U118 by the Pod A clock;

- Probe A data is clocked into Probe B memory through U121 by the Pod B clock;

- Probe B data (at U221) is disabled; and

- Probe C data is clocked into Probe C memory through U421 by the Pod C clock.

The DAS selects demultiplexing by setting the MUX MODE signal high. This signal enables the mux mode login register, U121, and disables the probe B data login register, U221. The mux mode login register, U121, receives its data from probe A, but it receives the same clock as the probe B login register. U121 then places its data on the probe B section of the LID0-LID24 bus, effectively replacing the probe B login register.

91A24 ACQUISITION MEMORY ⟨73⟩

The acquisition memory consists of four parts:

1. Data registers to allow setup time before data is stored.

2. A chip-select generator that determines when data is stored in the acquisition memory.

3. The acquisition memory RAM which stores the acquired data.

4. A memory address register that determines the RAM address where storage occurs.

Acquisition Memory Data Registers

Acquired data comes from the login registers (shown on schematic 72) and is clocked into the acquisition memory data registers (U128, U228, and U428 on schematic 73). The data register clock, MASTER CLK II, comes from the master clock selector (U721 on schematic 77). The master clock is selected by the MASTER CLOCK field in the 91A24 Trigger Specification sub-menu.

Data output by the data registers is stored in the acquisition RAM and used as inputs to the data qualifier and stack-based word recognizers. By latching incoming data, the data registers give the acquisition memory and the word recognizers the setup time they need.

Chip-Select Generator

The chip-select generator is a mono-stable multivibrator. It creates a pulse in response to a falling edge from MASTER CLK III. C468 (on schematic 73) determines the pulse width. Figure 4-2 shows the timing of the chip-select generator.
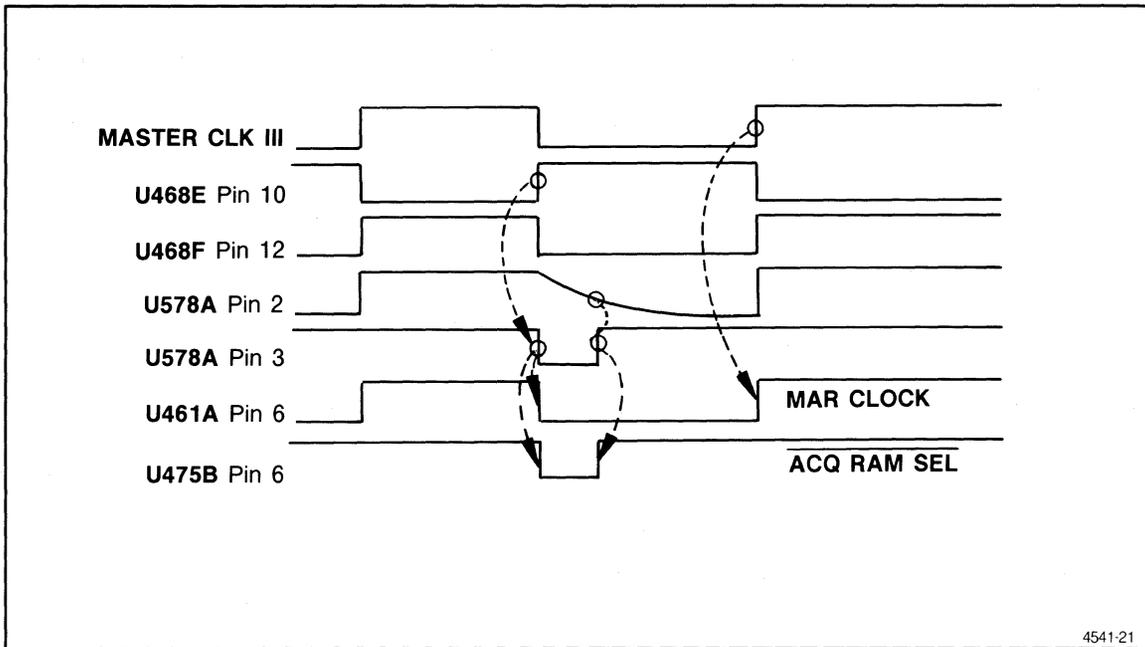
Figure 4-2. 91A24 acquisition memory chip select timing.

Before acquisition starts, the controller interface sets READ ACQ low. When READ ACQ is low, U475B (on schematic 73) passes $\overline{\text{ACQ RAM SEL}}$ signals to the acquisition RAM.

A high level on MASTER CLK III enters the chip-select circuitry block (on schematic 73). The signal is inverted by U468E, and again by U468F. The high level at U468F pin 12 turns on Q465 and charges C467 and C468. This sets U578A pin 2 high.

On the next falling edge from MASTER CLK III, U578A pin 1 goes high, and U578A pin 3 goes low, asserting $\overline{\text{ACQ RAM SEL}}$. U578A pin 3 stays low until C467 and C468 have discharged through R468. U578A pin 3 then returns high. C468 must be adjusted so that the pulse width of the $\overline{\text{ACQ RAM SEL}}$ signal at TP465 is 45 ns. The output at U578A pin 3 is used both for the chip select on the acquisition memory RAMs and to set U461A pin 6 (MAR CLOCK).

The chip-select generator has two outputs: MAR CLOCK which comes from U461A, and $\overline{\text{ACQ RAM SEL}}$ which comes from U475B. $\overline{\text{ACQ RAM SEL}}$ controls the write cycle of the acquisition RAM. The $\overline{\text{ACQ RAM SEL}}$ signal's 45 ns pulse width allows the RAM's address adequate setup time. When data is read from the acquisition memory, $\overline{\text{ACQ RAM SEL}}$ is activated by the READ ACQ signal from the controller interface.

The MAR CLOCK signal clocks the memory address register on the rising edge of MASTER CLK III. When data is being acquired, MAR CLOCK rising edges cause the acquisition memory address to increment. A low MAR EN signal from the data qualifier circuit prevents MAR CLOCK rising edges. Stopping these rising edges prevents the acquisition memory address from incrementing, so data in the acquisition memory is overwritten. This is how the data qualifier stops data acquisition.

Acquisition Memory RAM

The acquisition memory RAM (U141, U145, U241, U245, U441, and U445 on schematic 73) stores acquired data for later readback by the DAS Controller board.

Data Storage. Before acquisition, The controller interface selects a master clock. Then the controller interface programs the READ ACQ and the acquisition memory RAM's $\overline{\text{WEA}}$-$\overline{\text{WEC}}$ inputs low.

During acquisition the master clock, selected in the 91A24 Trigger Specification sub-menu, generates the MASTER CLK II and MASTER CLK III signals. These two clocks load acquired data into the data registers (U128, U228, and U428 on schematic 73) and run the chip-select generator.

Data is loaded from the data registers into the acquisition memory RAM. The acquisition memory write cycle is controlled by the chip-select generator. The chip-select generator creates the $\overline{\text{ACQ RAM SEL}}$ signal which induces data storage.

The $\overline{\text{MAR EN}}$ signal determines which data is saved. When input data is recognized as qualified by the data qualifier, $\overline{\text{MAR EN}}$ goes low and MAR CLOCK increments the memory address register. When input data does not meet the data qualification requirements the RAM address does not increment, so the data just stored will be over-written on the next storage cycle.

Data Readback. When data is not being stored, the DAS Controller pulls the $\overline{\text{WEA}}$-$\overline{\text{WEC}}$ signals high to prevent further data storage. The current value of the memory address register is read first, since that address in the acquisition memory RAM contains invalid data. The invalid data at this address results from the data qualification scheme.

After reading the latest value of the memory address register, the Controller board reads data from the acquisition RAM by loading an address into the memory address register, then asserting READ ACQ. Asserting READ ACQ places the stored data on the DR0-DR23 bus, and tristates the input data registers (U128, U228, and U428 on schematic 73). The DAS Controller board reads DR0-DR23 through the controller interface readback circuitry shown on schematic 69.

Memory Address Registers

The memory address registers (U138, U238, and U438 on schematic 73) provide the address for acquisition memory storage and readback. The memory address register is a ten-bit up counter that is clocked by the MAR CLOCK signal.

Data Storage. Before any data is stored, the memory address register is loaded with 0s in the ten low bits. The top two bits of the counter are not used for a RAM address, and they are loaded with 1s. So the initial value of the memory address register is $C00_{16}$.

During data acquisition, the memory address is incremented by every rising edge on the MAR CLOCK signal. When the address has incremented 400_{16} times (so all memory locations have been used), the counter wraps around to all zeros. New data is then loaded over the old data in the acquisition memory.

Register U461B (on schematic 73) indicates when all locations in the acquisition memory contain valid data. Before acquisition starts, register U461B is set so the ALL FULL signal is low. The counter wrapping to all 0s clocks a 0 into the register U461B so the Q output goes low. A low from the Q output resets the register, so the $\overline{\text{Q}}$ output (ALL FULL) goes high. When ALL FULL is high, all acquisition memory RAM locations have had data loaded in at least once.

Data Readback. The memory address register (MAR) value is always available to the DAS Controller board through the controller interface readback circuitry shown on schematic 69. To select the address of data read from the acquisition memory RAM, the controller interface loads the RAM address into the MAR in parallel. To increment the memory address, the controller interface loads the LB0-LB7 bus and toggles the $\overline{\text{MAR LD1}}$ signal. The lowest two bits on LB0-LB7 are loaded into the top two memory address bits. The low eight address bits increment because $\overline{\text{MAR LD1}}$ is connected to ENP and ENT inputs of U138.

91A24 DATA QUALIFIER WORD RECOGNIZERS ⟨74⟩

This schematic shows the circuitry for the four non-stack based word recognizers. These word recognizers are controlled through the 91A24 Trigger Specification sub-menu. The word recognizers can control data storage (BEGIN STORE IF, END STORE IF, and STORE ONLY IF conditions), control the stack-based word recognizer (RESET), and control triggering (OR TRIGGER).

This schematic also shows the 91A24 acquisition start and stop circuitry.

Data Qualifier Word Recognizer RAM

The data qualifier word recognizer is RAM-based, much like the 91A32 Data Acquisition module word recognizers. The RAMs (U151, U351, and U551 on schematic 74) are programmed to react to specific words on the DR0-DR23 bus.

To understand how the RAM is used for word recognition, consider the RAM as a set of addressable registers. The RAM is programmed by writing 1s in all the addresses that correspond to the words to be recognized. 0s are written into all other addresses. After programming, the stream of data containing the word to be recognized is used to address the RAM. The RAM indicates word recognition by outputting a 1.

Since the words to be recognized may have X (don't care) as an element, programming becomes slightly more complicated. For every X (don't care) entered in a word recognizer field, twice as many words meet the triggering requirements. For example, if the word to be recognized is 10100110_2 a single 1 must be written into RAM address 10100110_2. If $X0100110_2$ is to be recognized, 1s must be loaded into both addresses 00100110_2 and 10100110_2. If $XX100110_2$ is to be recognized, 1s must be loaded at four different addresses. So, if $XXXXXXXX_2$ is to be recognized, all 256 addresses must have 1s written in them.

Since 24 bits must be monitored for word recognition, three RAMs with 8 address lines each are used (for a total of 24 address lines). Each RAM recognizes 8 of the 24 bits involved. All three of the RAMs must recognize their word segments at the same time for word recognition to occur.

Each of the three RAMs have four data lines, so four independent words can be recognized. All four of the data lines in each RAM are programmed independently, so signals A1, B1 and C1 are used to recognize one word. Signals A2, B2, and C2 recognize another word.

Data Qualifier Word Recognizer

The data qualifier word recognizer completes the work of the data qualifier word recognizer RAM. AND gates U168B and U261A, B, and C (on schematic 74) make sure that all three 8-bit segments of a word are true before a word is recognized.

The outputs of the four AND gates are wire ANDed with all the data qualifier output signals from 91AE24 modules. These signals come from the 91AE24 modules through the cables across the top of the modules. Wire ANDing these signals means that all 91A24 and 91AE24 modules must recognize their portions of a word at the same time for word recognition to occur.

The output of inverting-input OR gate U568D (from the start/stop circuit) is also wire ANDed with the word qualifier signals through inverters U278A, B, E, and F (on schematic 74). The 91A24 start/stop circuit controls the 91A24 module through the data qualifier. Refer to the 91A24 start/stop circuit description, later, for more information.

The four word recognition signals that result from all these wire ANDed signals are buffered by U198B and U291A, B, and C (schematic 74). Exclusive-OR gates U291A, B, and C allow three of the signals to be inverted by changing one bit at the controller interface. OR gate U198B allows the DAS Controller board to assert the ENABLE signal through the controller interface.

Storage Control Circuitry

The circuitry surrounding U281, U288, and U478B (on schematic 74) determines when data is stored depending on the data qualifier word recognizer conditions. U281 determines when the BEGIN STORE IF conditions in the 91A24 Trigger Specification sub-menu are met. U478B saves the BEGIN STORE IF condition from the previous cycle as the STORING DATA signal. U288 uses the word recognizer conditons and the STORING DATA signal to control the memory address register for the acquisition memory.

There are three basic operating modes for the data qualifier.

1. In the default condition, the data qualifier is controlled by a BEGIN STORE IF (ENABLE) and an END STORE IF ($\overline{\text{DISABLE}}$) word. To set up this mode, the DUAL QUAL signal is programmed low. In this mode the RESET word clears the stack word recognizer (schematic 75), and the $\overline{\text{OR TRIG}}$ word triggers the 91A24 module (schematic 76).

2. For dual qualifier operation, the RESET and $\overline{\text{OR TRIG}}$ signals are used as additional qualifiers. In this mode, the RESET word functions as the second BEGIN STORE IF or STORE ONLY IF word, and the $\overline{\text{OR TRIG}}$ word functions as the second END STORE IF word. This mode is enabled by programming the DUAL QUAL signal high.

3. For STORE ONLY IF operation, the END STORE word is set to OFF on the 91A24 Trigger Specification sub-menu display. The DISABLE WORD word recognizer is programmed so the $\overline{\text{DISABLE}}$ signal is always low (active), so storage only occurs when the ENABLE signal is active. If the DUAL QUAL signal is asserted, the word recognizer programming is the same but storage only occurs when either the ENABLE or the RESET signal is active.

A closer look at the DUAL QUAL signal shows when DUAL QUAL is low, two of the four AND gates in U281 (schematic 74) are disabled. The remaining AND gates (U281C and D) cause STORING DATA to go active if either ENABLE and $\overline{\text{DISABLE}}$ are both high or if STORING DATA and $\overline{\text{DISABLE}}$ are both high. This sets up the BEGIN STORE IF condition, so once storing is enabled it is held enabled by the STORING DATA signal until $\overline{\text{DISABLE}}$ goes active (low).

When DUAL QUAL is high, AND gates U281C and D are disabled, and U281A and B control the STORING DATA signal. U281A goes active when $\overline{\text{DISABLE}}$ and $\overline{\text{OR TRIG}}$ are both high and either RESET or ENABLE are high. U281B goes active when $\overline{\text{DISABLE}}$ and $\overline{\text{OR TRIG}}$ are both high and STORING DATA is active. This sets up the BEGIN STORE IF condition, so once storing is enabled it is held enabled by the STORING DATA signal until the $\overline{\text{DISABLE}}$ or the $\overline{\text{OR TRIG}}$ signals go active (low).

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U288 actually controls data storage with the $\overline{\text{MAR EN}}$ signal. When $\overline{\text{MAR EN}}$ is low, the MAR CLOCK signal increments the memory address register. When input data does not meet the data qualification requirements then $\overline{\text{MAR EN}}$ is high, which prevents the memory address register from incrementing. When the memory address register does not increment, the data just stored will be overwritten on the next storage cycle.

When DUAL QUAL is low, AND gates U288C and D are both enabled. U288C enables storage when both STORING DATA and $\overline{\text{DISABLE}}$ are high. U288D enables storage whenever the ENABLE signal is high.

When DUAL QUAL is high, AND gates U288A, B, and D are enabled. U288A enables storage when the $\overline{\text{DISABLE}}$, $\overline{\text{OR TRIG}}$, and STORING DATA signals are all high. U288B enables storage when RESET is high, and U288D enables storage when ENABLE is high.

U198A determines whether the $\overline{\text{OR TRIG}}$ signal is being used as a second END STORE word or as an alternate trigger word. When DUAL QUAL is high, the $\overline{\text{OR TRIG}}$ signal is prevented from reaching the trigger circuitry on schematic 76.

91A24 Start/Stop

The 91A24 start/stop circuitry (register U488A and inverting-input OR gates U581B and U568D on schematic 74) delays 91A24 data acquisition until valid data is clocked into the acquisition memory data registers (U128, U228, and U428 on schematic 73). The start/stop circuitry also stops the 91A24 when the trigger condition is met and the delay count is complete. The start/stop circuitry operates by taking control of the data qualifier.

The DAS Controller board starts and stops the 91A24 using the 91A32 QUAL signal on the interconnect. 91A32 QUAL is held low prior to acquisition. This low passes through, and is inverted by, inverting-input OR gate U568D. This signal holds all of the data qualifier word recognizer signals low through buffers U278A, B, E, and F. By holding the data qualifiers low, the master clock can run freely without data being acquired.

MASTER CLK I logs the inverse of the 91A32 QUAL signal into register U488A. Once logged in, 91A32 QUAL goes high to start acquisition, but the data qualifier signals are not released until the next MASTER CLK I edge. The first master clock edge with 91A32 QUAL high starts acquisition.

After the 91A24 has signaled the DAS Trigger board that a trigger has occurred, the Trigger board finishes the trigger sequence with its delay counter. When the Trigger/Time Base board's delay counter finishes, the Trigger board pulls the 91A32 QUAL signal low, which stops 91A24 acquisition.

The $\overline{\text{91A24 INIT}}$ signal sets register U488A (schematic 74), so the 91A24 initializes with acquisition turned off.

91A24 System Clock

The system clock circuit provides the Trigger/Time Base board with a modified version of the 91A24 master clock called $\overline{\text{FIRST CLOCK}}$. $\overline{\text{FIRST CLOCK}}$ is also acquired by high speed modules for time alignment purposes. The rising edge of MASTER CLK I causes each falling edge of $\overline{\text{FIRST CLOCK}}$. $\overline{\text{FIRST CLOCK}}$ only runs under two conditions.

1. $\overline{\text{FIRST CLOCK}}$ runs when U488A pin 6 (schematic 74) is low. Pin 6 of U488 is low when the 91A24 is initialized and ready to acquire data, but is not yet acquiring data because the 91A32 QUAL signal is still low. The Trigger/Time Base board needs a copy of the 91A24 master clock before acquisition starts to clear the Trigger/Time Base pipelined internal timing sequencer (schematic 17).

2. After acquisition starts $\overline{\text{FIRST CLOCK}}$ drives the delay counter on the Trigger/Time Base board (schematic 18). The 91A24 module uses the delay counter on the Trigger/Time Base board as its delay counter to save circuit board space. Because the delay counter should only increment when data is stored, $\overline{\text{FIRST CLOCK}}$ only runs when $\overline{\text{MAR EN}}$ is active (low). $\overline{\text{MAR EN}}$ is only active when data can be stored in the 91A24 acquisition memory.

Register U481B and inverter U578C (schematic 74) act as a one-shot with a 20-30 ns high pulse. The high pulse is triggered by a rising edge from MASTER CLK I. When either pin 6 of U488A or $\overline{\text{MAR EN}}$ are low, the D input of U481B receives a high which is clocked in on every MASTER CLK I rising edge. The high is clocked through the Q output and inverted by U578C. A low from U578C resets register U481B so the Q output returns low. R190 and C190 determine the width of the output pulse.

Resistors R954, R955, and R956 convert the TTL output from register U481B to ECL levels. NOR gates U921B and C double drive the ECL $\overline{\text{FIRST CLK}}$ signal across the DAS Interconnect to the Trigger/Time Base board.

A low on $\overline{\text{FIRST CLK EN}}$ holds the outputs of U921B and C low. $\overline{\text{FIRST CLK EN}}$ is used whenever any module other than the 91A24 needs to use the $\overline{\text{FIRST CLK}}$ path on the DAS Interconnect.

91A24 STACK WORD RECOGNIZER ⟨75⟩

The stack word recognizer is the hardware implementation of the sequential word recognizer in the 91A24 Trigger Specification sub-menu. The stack word recognizer is based around RAMs U148, U248, and U448 (on schematic 75). The RAMs recognize words by receiving acquired data on their address lines.

Sixteen levels of triggering are accomplished with a 4-bit stack pointer SP0-SP3 from U571 (on schematic 76). The stack pointer addresses the stack word recognizer RAMs. The value from the stack pointer effectively divides the stack word recognizer RAMs into sixteen separate sections. The stack pointer also provides the address for the stack occurrence counter RAM (U155, U255, and U455 on schematic 75). The stack occurrence counter RAM controls the number of times a word must be recognized to advance to the next stack level. The stack pointer provides the address for the stack control RAM as well. The stack control RAM is loaded with the action to be performed at each stack level (for example: run timer, stop timer, or sync out).

Stack Word Recognizer RAM

The stack word recognizer is RAM-based, much like the data qualifier word recognizers. The RAMs (U148, U248, and U448 on schematic 75) are programmed to react to specific words on the DR0-DR23 bus according to the value of the stack pointer (SP0-SP3).

To understand how the RAM is used for word recognition, consider the RAM as a set of addressable registers. The stack word recognizer uses three RAMs with 12 address lines each; four of the address bits indicate the position in the stack, the other eight address bits are used for word recognition. The four stack pointer bits (SP0-SP3) effectively divide the RAMs into sixteen separate segments. The word recognizer segments are activated according to the value on SP0-SP3.

The remaining eight bits of each RAM perform the actual word recognition. The RAM is programmed by writing 1s in all the addresses that correspond to the words to be recognized. 0s are written into all other addresses. After programming, the stream of data containing the word to be recognized is used to address the RAM. The RAM indicates word recognition by outputting a 1.

Since the words to be recognized may have X (don't care) as an element, programming becomes slightly more complicated. For every X (don't care) entered in a word recognizer field, twice as many words meet the triggering requirements. If the word to be recognized is 10100110_2 a single 1 must be written into the RAM at address 10100110_2. If $X0100110_2$ is to be recognized, 1s must be loaded into both addresses 00100110_2 and 10100110_2. If $XX100110_2$ is to be recognized, 1s must be loaded at four different addresses. So, if $XXXXXXXX_2$ is to be recognized, all 256 addresses in the selected RAM segment must have 1s written in them.

Since 24 bits must be monitored for word recognition, three RAMs with 8 word recognition lines each are used (for a total of 24 word recognition lines). Each RAM recognizes one byte of the 24 bits involved. All three of the RAMs must recognize their byte of the word at the same time for word recognition to occur.

Stack Occurrence Counter RAM

Before acquisition starts, the stack occurrence counter RAMs (U155, U255, and U455) are loaded with the complement of the number of times a word must be recognized to move to the next stack level. For example, for an occurrence count of 1, FFE_{16} is loaded into the RAM. During operation the occurrence counter RAM is addressed by the stack pointer (SP0-SP3). When the stack pointer increments, a new value is output by the occurrence counter RAM which is then loaded into the stack occurrence counter (U158, U258, and U458 on schematic 75).

Stack Occurrence Counter

The stack occurrence counter (U158, U258, and U458 on schematic 75) is a 12 bit up counter. The counter increments each time the word at the current stack level is recognized by the stack word recognizer RAM.

Before acquisition starts, the stack occurrence counter RAM (U155, U255, and U455 on schematic 75) is loaded with the complement of the number of event occurrences required to complete each stack level. Then the DAS Controller board sets the stack pointer to 0. Finally, the Controller board toggles $\overline{\text{OCCR CNTR LD}}$ to load the stack 0 level occurrence count from the RAM into the counter.

During acquisition, the occurrence counter increments every time a word is recognized. When the counter increments to FFF_{16}, NAND gate U161 outputs a low edge that increments the stack pointer. When the stack pointer changes, a new value is output by the occurrence counter RAM. On the next rising edge from MASTER CLK II the Q output of U165B goes low, and this loads the new value into the occurrence counter. As soon as the new value is loaded, NAND gate U161 outputs a high and the occurrence counter returns to increment mode.

The counter is incremented by pulses from register U165A (schematic 75). When a word is recognized, the D input to U165A goes high. This high is clocked through on the next rising edge of MASTER CLK II. Inverter U268B inverts the high output caused by the clock. The inverted output resets the register, but the RC combination R266B and C165 acts as an integrator to delay the reset for about 30 ns. When the reset goes active, the Q output of U165A has a falling edge that increments the counter and removes the reset signal.

Stack Word Recognizer Control

At its simplest level, the stack word recognizer control circuit is a multiple input AND gate that outputs a high when all parts of the stack word are recognized. U168A is the AND gate for the three 91A24 stack word recognizer RAMs (schematic 75). When all three of the stack word recognizer RAMs (U148, U248, and U448) output high levels, AND gate U168A outputs a high to indicate word recognition.

The output of AND gate U168A (schematic 75) is wire ANDed through J171 to the stack word recognizer outputs of all 91AE24 modules in the mainframe. So all 91A24 and 91AE24 modules must recognize their stack words at the same time for stack word recognition to occur.

Exclusive OR gate U291C (schematic 75) implements the WHEN/WHEN NOT field in the 91A24 Trigger Specification sub-menu. While the stack is at a WHEN level, the SC3 signal is high, so the word recognition signal is inverted. This inversion means the stack occurrence counter increments when the programmed word is recognized. When a WHEN NOT level is reached, SC3 goes low, so the word recognition signal is not inverted. Since the signal is not inverted, the stack occurrence counter increments every time the word to be recognized is not present.

Inverting-input AND gate U485C (schematic 75) stops stack word recognition when the data qualifier stops acquisition. When $\overline{\text{MAR EN}}$ goes high, U485C prevents the stack word recognition signal from reaching the stack occurrence counter.

The Trigger Input BNC on the back of the mainframe controls the 91A24 trigger through the 91A24 stack word recognizer. When the 91A24 module is initialized before acquisition starts, register U488B (schematic 75) is reset by $\overline{\text{91A24 INIT}}$. If the Trigger Input is low after the module is initialized, the EXT TRIG EN signal is low so U488B remains reset. The $\overline{\text{Q}}$ output of U488B then prevents stack word recognition with the ENABLE TRIG signal. When EXT TRIG EN goes high, register U488B is set, which enables stack word recognition until acquisition is stopped.

Stack Control RAM

The DAS Controller board loads the stack control RAM (U555 on schematic 75) with stack level conditions before acquisition starts. Then during acquisition, the RAM is addressed by the stack pointer (SP0-SP3). The RAM outputs control signals SC0-SC3 as appropriate for each of the stack levels. The conditions controlled by the RAM are:

- TRIGGER and last level (SC0)
- RUN TIMER, STOP TIMER, and INC CNTR (SC1)
- SYNC OUT (SC2)
- WHEN and WHEN NOT (SC3)

91A24 TRIGGER CIRCUITRY ⟨76⟩

Schematic 76 shows the circuits that complete the operations of the stack word recognizer (schematic 75). The stack pointer block controls the stack level of the stack word recognizer.

The reset circuitry block reacts when the RESET word is recognized by clearing the stack pointer and reloading the stack occurrence counter (schematic 75).

When all trigger conditions have been met in the 91A24, the trigger circuitry block tells the Trigger/Time Base to run its delay counter. The Trigger/Time Base stops acquisition when the delay count is done.

The remaining blocks on schematic 76 comprise the counter/timer that is controlled by the stack word recognizer.

Stack Pointer

The stack pointer (U571 on schematic 76) is a four-bit synchronous up counter. The POINTER CLK signal, which increments the stack pointer, comes from the stack occurrence counter block on schematic 75. The POINTER CLK signal also goes to all 91AE24 modules in the mainframe through J181 at the top of the module. The stack pointer can also be incremented by the DAS Controller board by pulling $\overline{\text{STACK CLK EN}}$ low and toggling $\overline{\text{STACK PTR CLK}}$.

Inverter U578D prevents the stack pointer from wrapping from 1111_2 to 0000_2 by disabling the counter. SC0 going low means the 91A24 is at the last programmed level of the stack, so SC0 being low disables the counter. The stack pointer is cleared by the reset circuitry (schematic 76), and loaded by the $\overline{\text{STACK PTR LD}}$ signal.

Reset Circuitry

The reset circuitry (schematic 76) clears the stack occurrence counter (schematic 75) and the stack pointer (schematic 76) when the RESET word is recognized. U558A NANDs the RESET signal with $\overline{\text{STACK WR}}$, $\overline{\text{OR TRIGGER}}$, and $\overline{\text{DUAL QUAL}}$. This NAND operation disables the reset circuitry when the module is in dual qualifier mode, or when the stack word or the OR trigger word (from the data qualifier) is recognized.

If the RESET signal makes it through NAND gate U558A, it may still be masked out by the $\overline{\text{MAR EN}}$ signal at U575B (schematic 76). $\overline{\text{MAR EN}}$ only allows the RESET operation to occur while data is being stored.

If the RESET signal passes through U575B, it clears the stack pointer (U571 on schematic 76) and triggers a monostable multivibrator built around register U471B. If an active RESET signal is at the D input to U471B (RESET is active low at this pin) when MASTER CLK III has a rising edge, the Q output of the register goes low. This low reloads the stack occurrence counter (schematic 75) with the $\overline{\text{LOAD OCCR CNTR AFTER RESET}}$ signal.

The low from U471B's Q output may also pass through U475C and U198D to clear the counter/timer block to all 0s. This clear may be masked, however, by the $\overline{\text{RESET CNTR EN}}$ signal.

Register U471B and inverter U495B (schematic 76) act as a one-shot. The pulse is triggered by a rising edge from MASTER CLK III. When the D input of U471B receives a low, a high is clocked through the $\overline{\text{Q}}$ output and inverted by U495B. A low from U495B sets register U471B so the $\overline{\text{Q}}$ output returns low. R398, R397, and C396 determine the width of the output pulse.

Register U478A (schematic 76) is provided for readback purposes. Whenever the counter/timer is reset, register U478A is reset, causing the CNTR RESET signal to go high. Before acquisition starts this register is set by the $\overline{\text{INT3 CLR}}$ signal.

Trigger Circuitry

Triggers come from two possible sources: the stack word recognizer and the OR TRIGGER word. Register U298A latches the $\overline{\text{OR TRIGGER}}$ if it is not masked by $\overline{\text{MAR EN}}$ (by inverting-input NAND gate U575A). $\overline{\text{MAR EN}}$ deactivates $\overline{\text{OR TRIGGER}}$ when the data qualifier is preventing data acquisition.

Register U481A clocks in trigger indications from the stack word recognizer. When the stack word recognizer trigger requirements are complete, SC0 goes low. This low is logged into U471A (schematic 76) when POINTER INC and MASTER CLK III both go active. If the last level of the stack is programmed with NEVER TRIGGER, then the NEVER TRIGGER signal is programmed low by the DAS Controller board. NEVER TRIGGER holds register U481A set, so the stack word recognizer can never cause a trigger.

The outputs of registers U298A and U481A are ORed together by inverting-input NOR gate U475A. If either of these trigger signals goes active, the active (low) signal is clocked through registers U798A and B. These registers delay the trigger by two TRIG CLK cycles, so the number of cycles the 91A24 trigger requires equals the number of cycles required by a 91A32 module. Inverting-input OR gate U581D is the driver for the trigger signal, called EVENT 1, to the Trigger/Time Base board. The 91A24 always keeps the EVENT 3 signal low when it is using the Trigger/Time Base, so no other module can disrupt acquisition.

When some module other than the 91A24 needs to use the EVENT 1 or EVENT 3 signals, the DAS Controller board programs the 91A24 TRIG DIS signal low. This low makes the 91A24 output a high impedance to these two lines so other modules can control the signals.

Register U471A (schematic 76) provides the SYNC OUT pulse which comes from the stack word recognizer. When the stack reaches a SYNC OUT level, the stack control RAM (U555 on schematic 75) sends SC2 high. This high is logged into U471A (schematic 76) when POINTER INC and MASTER CLK III both go active. Inverter U568A is the driver for the signal out the back of the module through J801.

Counter/Timer Multiplexer

The counter/timer multiplexer (U295 on schematic 76) controls the behaviour of the counter/timer. The DAS Controller board programs U295 with the CT SEL0 and CT SEL1 signals. Table 4-3 shows how the state of CT SEL0 and CT SEL1 control the counter/timer.

Table 4-3
COUNTER/TIMER MULTIPLEXER CONTROL

Inputs			
U285C pin 8	CT SEL1	CT SEL0	Operation Selected
0	0	0	Disable both counter and timer. Neither the counter nor the timer is needed.
0	0	1	Operate the timer in non-stop mode. Used by the diagnostics.
0	1	0	Operate in counter mode. Counter started and stopped by CS1 high.
0	1	1	Operate in timer mode. Timer started and stopped by CS1 high.
1	X	X	Stop the timer or counter — a trigger has occurred.

Inverter U495D and AND gate U475D (schematic 76) generate the clock for the counter/timer when it is in counter mode. The clock has a rising edge when both MASTER CLK III and POINTER INC are active, which indicates that the pointer has just incremented one level.

Register U298B (schematic 76) uses the counter clock to latch in the timer enable signal. U298B holds the timer enable signal until either the stack moves to a level where the timer is turned off (SC1 goes low) or the RESET word is recognized (which resets the register).

Register U491A and inverter U495C (schematic 76) act as a one-shot. Pulses from this one-shot drive the counter/timer block. The pulse is triggered by a rising edge from U295 pin 9 while U295 pin 7 is high. When the D input of U491A receives a high, a high is clocked through the Q output and inverted by U495C. A low from U495C resets register U471B so the Q output returns low. R296, R399, and C397 determine the width of the output pulse. The diagnostics can also exercise this register by toggling the $\overline{\text{TIMER CLK}}$ signal, which triggers the one-shot action by setting the register.

Timer Oscillator

The timer oscillator is built around 10 MHz crystal Y498 (on schematic 76). This 10 MHz oscillator drives the counter/timer circuit when it is in timer mode.

Counter/Timer

The counter/timer (U585, U588, U591, and U595 on schematic 76) is a 16-bit synchronous up counter. The clock is provided by the counter/timer multiplexer (U295). The counter can also be cleared by the reset circuitry.

Counter/Timer Interrupt Generator

The counter/timer generates an interrupt for the DAS Controller board when it rolls over from FFFF_{16} to 0000_{16}. The interrupt is generated by register U491B when the most significant counter/timer bit goes from high to low. The Controller board increments a counter in software when it receives the interrupt. This is how the counter/timer function of the 91A24 counts past 65,535. When the Controller board has reacted to the interrupt, the Controller toggles (low) the INT3 EN signal to set the register so the interrupt can be performed as many times as necessary during the count.

Counter/Timer Readback

Tri-state buffers U788 and U795 allow the DAS Controller board to read the counter/timer after acquisition is complete. The least significant byte is read through U788, which is activated by the $\overline{\text{CNTR RDBK0}}$ signal. The most significant byte is read through U795, which is activated by the $\overline{\text{CNTR RDBK1}}$ signal.

91A24 CLOCK QUALIFIER ⟨77⟩

The 91A24 clock qualifier circuitry selects qualifier signals received from the acquisition probes. The signals are selected according to the 91A24 Clock Specification sub-menu. Schematic 77 also shows the master clock selector and drivers.

Clock/Clock-Qualifier Selector

The clock/clock-qualifier selector controls the clocks and clock qualifiers with a set of CMOS registers (U928, U931, U935, U938, U941, and U945 on schematic 77). Power for the registers is supplied through Q951, which drops the +5 V supply down to approximately +4.5 V. +4.5 V is used for the register's power supply so the register's outputs are ECL compatible.

The clock/clock-qualifier selector receives programmed information from the 91A24 Clock Specification sub-menu and generates:

- Enable signals for the clock qualifier generator on schematic 77. These signals come from registers U928, U931, and U935 on schematic 77.

- Enable signals for the clock generator on schematic 78. These signals come from registers U938, U941, and U945 on schematic 77.

- Enable signals for the master clock selector (U721 on schematic 77). These signals come from registers U938, U941, and U945 on schematic 77.

Inputs PC0-PC5 from the controller interface (on schematic 68) are latch clocks. D0-D7 contain programmed information which selects the proper enabling outputs.

Clock Qualifier Generator

The clock qualifier generator passes qualifier signals to the clock generator (on schematic 78). These qualifier signals determine whether a clock received from the probes will cause data acquisition.

The clock qualifier generator receives differential qualifier signals (three qualifier signals and their inverses) from probes A, B, and C. Qualifier enabling signals determine how the clock qualifier generator combines the qualifiers for each pod clock. These enabling signals are programmed in the 91A24 Clock Specification sub-menu and are controlled by the clock/clock-qualifier selector.

The most complicated expression possible in the 91A24 Clock Specification sub-menu uses all three qualifiers for all three clock expressions. As a result, nine qualifier generators are needed — one for each qualifier position in the menu. The menu also allows for the selection of an inverted or non-inverted qualifier.

Each inverting-input NAND gate in the clock qualifier generator block (on schematic 77) is programmed to pass either an inverted or a non-inverted qualifier signal. The DAS programs each of the inverting-input NAND gate pairs so only one or the other (or neither) of the qualifier signals is output. Additionally, the NAND gates are programmed to pass the inverse of the desired signal. For example, if the inverse of QA is used in the pod A clock expression, U825B would pass $\overline{QA}$. Table 4-4 shows how each NAND gate pair matches a qualifier position in the 91A24 Clock Specification sub-menu.

Table 4-4
CLOCK QUALIFIER GENERATOR DISTRIBUTION

Qualifier	Pod Clocks		
	Pod C	**Pod B**	**Pod A**
QA	U831B	U828B	U825B
QB	U831A	U828A	U825A
QC	U728A	U728B	U731A

Each of the inverting-input NAND gate pairs is controlled by two bits; an even bit and an odd bit. Table 4-5 shows how the NAND gate pairs react to the possible bit values.

Table 4-5
CLOCK QUALIFIER CONTROL BITS

Odd Bit QA5, QA3, QA1 QB5, QB3, QB1 QC5, QC3, QC1	Even Bit QA4, QA2, QA0 QB4, QB2, QB0 QC4, QC2, QC0	Clock Qualifier Reaction
0	0	Always allow clocks
0	1	Allow clocks when signal is high
1	0	Allow clocks when signal is low
1	1	Never allow clocks

In addition to the programming allowed, the qualifier C outputs are hardwired to the qualifier A and B inputs. This automatically ANDs qualifier C with all other clocks in the pod clock expression. This is also why the inverting-input NAND gates for qualifiers A and B each have three inputs, while the inverting-input NAND gates for qualifier C have only two inputs. As a result of this ANDing, the output qualifier C for a pod expression must be true (low) before the A or B qualifiers in the same expression can become true (low).

Master Clock Selector

The AND gates in U721 (on schematic 77) select the master clock. The master clock is chosen in the 91A24 Trigger Specification sub-menu with the MASTER CLK field. Once the selection is made, one of control bits CA6, CB6, CC6, or CA7 goes high to pass the selected clock. The other bits remain low so the clocks they control are masked out.

CA7 only goes high to select the single step clock. $\overline{\text{SINGLE STEP}}$ is used only for diagnostics and to program 91A24 and 91AE24 acquisition modules.

Master Clock Distribution

The master clock distribution circuitry translates the single-ended ECL output of the selected pod clock to TTL levels. The resulting master clock is divided into three identical clocks, MASTER CLK I, II, and III, to distribute the loading on the clocks.

91A24 CLOCK GENERATOR ⟨78⟩

The 91A24 clock generator takes the clocks from the acquisition probes and the processed qualifier signals from the clock qualifier generator to produce three independent acquisition clocks. The clock generator can also produce acquisition clocks from the $\overline{\text{91A32 CLK}}$ or $\overline{\text{91A08 CLK}}$.

Clock Generator

The clock generator uses the nine clock qualifier signals generated on schematic 77 ($\overline{\text{PAQA}}$, $\overline{\text{PBQA}}$, and $\overline{\text{PCQA}}$) to control the three clocks (and their inverses) received from the probes. Each qualifier signal controls one clock and its inverse. Since all clocks are programmed similarly, only the programming of pod A clocks is described.

U741A and U841A (on schematic 78) are programmed to generate clocks from the probe A input clocks (CLK1, $\overline{\text{CLK1}}$). To generate a clock on the rising edge, the CA0 signal is programmed low, thereby enabling U741A to be clocked by the rising edge of CLK1. If qualifier $\overline{\text{PAQA}}$ at U741A pin 7 is low on the rising edge of CLK1, that low level will be clocked through to U741A pin 3 as a high level. This low-to-high transition is sent through OR gate U538A as CLK A.

The same rising edge of CLK1 also clocks U741B, causing U741B's Q output to go low. RC network R751D (1.5K), and C751 (100 pF) delays this signal for approximately 20 ns. U848A inverts this low to a high, which sets all the flip-flops associated with CLK1. The high level on the set input of U741A causes the $\overline{\text{Q}}$ output (U741A pin 3) to return low, completing the clock pulse. The set on U741B pin 12 causes the Q output to go high, removing the set on the CLK1 flip-flops.

The last row of flip-flops, U741B, U841B, U751B, U851B, U745B, and U845B (schematic 78) are used to pulse-shape the pod clocks.

At run time, CLK INIT(L) is toggled low, causing the pulse-shaping flip-flops to generate one set pulse to preset all the clock flip-flops into a known state.

When an internal clock is selected, all the external clocks are disabled by programming all the clock enable signals high (CA0-CA5, CB0-CB5, and CC0-CC5). To select the $\overline{\text{91A32 CLK}}$, CC7 (U731B pin 11) is programmed low, and CB7 (U731B pin 14) is programmed high. On the rising edge of $\overline{\text{91A32 CLK}}$, if $\overline{\text{PAQC}}$ is low, U748A will pulse, sending a clock to all three pod clocks.

+3 V Power Supply

The +3 V power supply is a voltage-regulated current sink for the ECL terminating resistors.

Voltage divider R905 and R906 (on schematic 78) set a reference voltage of +3 V for the non-inverting input of op amp U904. The feedback loop through Q901 biases the transistor so the emitter follows the reference voltage. Since Q901 acts as a current sink for terminators, there is always sufficient current to maintain the +3 V.

91AE24 DATA ACQUISITION MODULE

The 91AE24 Data Acquisition module is a depopulated version of the 91A24 module. The 91AE24 receives its clocks from the 91A24 module and sends word recognition signals back to the 91A24. As many as three 91AE24 modules are controlled through cables connecting them to the 91A24. The 91A24 determines when storage should occur and when trigger conditions are met.

All component numbers in the 91AE24 module circuit description are assumed to have an A36 preface unless otherwise noted.

The 91AE24 circuit description is divided first by schematic, and then by functional blocks on the schematic. Numbers in diamonds refer to the numbers on schematic tabs in the *Diagrams* section of this addendum. Refer to those schematics while reading the circuit description. For an overview of the 91AE24 module's circuits, refer to the *General System Description*, earlier in this section.

As a depopulated version of the 91A24 module, the 91AE24 module has approximately 75% of the ICs installed in the board. Table 4-6 shows the ICs omitted from the circuit board when a 91AE24 is manufactured.

Table 4-6
INTEGRATED CIRCUITS INTENTIONALLY OMITTED
FROM 91AE24 CIRCUIT BOARDS

U155	U295	U491	U591	U741	U821	U845	U948
U158	U298	U495	U595	U745	U825	U848	U951
U161	U455	U535	U725	U751	U828	U851	U968
U165	U458	U538	U728	U781	U831	U921	U971
U255	U471	U581	U731	U788	U835	U928	U981
U258	U481	U585	U735	U795	U838	U931	U988
U278	U488	U588	U738	U798	U841	U935	U991

91AE24 CONTROLLER INTERFACE ⟨79⟩

The controller interface allows communication between the DAS Controller board and the 91AE24. Any block in the 91AE24 block diagram identified with an asterisk (*) uses the 91AE24 controller interface.

The 91AE24 controller interface performs two major functions:

1. It takes data from the DAS Controller board and writes it to appropriate 91AE24 registers. The registers are selected by decoding the lowest five bits on the address bus and interpreting $\overline{BWR}$, $\overline{BPORT}$, and $\overline{BRD}$ from the DAS Controller board.

2. It puts data from the 91AE24 module on the data bus at the command of the DAS Controller board.

91AE24 interface decoding and receiving circuitry is shown on schematic 79; readback circuitry is shown on schematic 80.

Receiving Control Data. As an example of how the 91AE24 receives control data, suppose the Controller board is writing data into port 01, the digital-to-analog converter that controls the probe threshold (U918 on schematic 82). The Controller board sets the low five bits of the address bus to 01_{16}, places the data on the data bus, and asserts $\overline{BWR}$ and $\overline{PORT}$. The 91AE24 react as follows:

1. Asserting $\overline{PORT}$ enables U768 (schematic 79). This transmits data from the data bus to the digital-to-analog converter.

2. $\overline{BWR}$, $\overline{PORT}$, and A4 being low together enable decoder U958 (schematic 79).

3. U958 decodes the 1_{16} on A0-A3 to assert the $\overline{THRESHOLD}$ signal. The rising edge when $\overline{THRESHOLD}$ is unasserted clocks the data on the address bus into the map register. Waiting for the rising edge of $\overline{THRESHOLD}$ allows adequate setup time for the data on the data bus.

Sending Data. The readback procedure is similar, except $\overline{BRD}$ is asserted instead of $\overline{BWR}$. As an example of how the 91AE24 sends data, suppose the Controller is reading the card ID from port 0 (register U791 on schematic 80). There are only 16 readback ports, so only address bits A0-A3 are decoded. The Controller board sets the low four bits of the address bus to 0_{16}, and asserts $\overline{BRD}$ and $\overline{PORT}$. The 91AE24 reacts as follows:

1. $\overline{BRD}$ and $\overline{PORT}$ being low together enable decoder U998 (schematic 80).

2. U998 decodes the 0_{16} on A0-A3 to assert the $\overline{CARD\ ID}$ signal. The $\overline{CARD\ ID}$ signal enables tri-state buffer U791, so the card ID is placed on the data bus.

Table 4-7 shows which registers are connected to the data bus and the $\overline{BWR}$, $\overline{BRD}$, and $\overline{PORT}$ signals.

Table 4-7
91AE24 CONTROLLER INTERFACE MAP

Hex Addr	$\overline{BWR}$	$\overline{BRD}$	$\overline{PORT}$	Line Name	ICs Affected U Number	Schem
XXX0	X	L	L	CARD ID	U791	80
XXX1	X	L	L	POD STATUS	U775	80
XX01	L	X	L	THRESHOLD	U918	82
XXX2	X	L	L	DATA CLOCK	J101, J401, J701	80
XX02	L	X	L	PROBE R/$\overline{W}$	U925	82
XXX3	X	L	L	MAR LOW	U135	80
XX03	L	X	L	CNTL1	U761	79
XXX4	X	L	L	MAR HIGH	U235	80
XX04	L	X	L	STACK A WE	U148	86
XX05	L	X	L	STACK B WE	U248	86
XX06	L	X	L	STACK C WE	U448	86
XXX7	X	L	L	DQ STATUS	U778	80
XX07	L	X	L	STACK CNTL	U555	86
XX09	L	X	L	SINGLE STEP	U125, U225, U425	87
XXXA	X	L	L	STACK CNTL RD	U785	80
XXXB	X	L	L	A MEM RD	U131	80
XXXC	X	L	L	B MEM RD	U231	80
XX0C	L	X	L	CNTL2	U758	79
XXXD	X	L	L	C MEM RD	U431	80
XX0D	L	X	L	STACK PTR CLK	U568C, U485A, U575D U571	86
XXXE	X	L	L	TRIGGERED RD	U771	80
XX0F	L	X	L	PADQ WE	U151	85
XX10	L	X	L	PBDQ WE	U351	85
XX11	L	X	L	PCDQ WE	U551	85
XX13	L	X	L	PC0	U938	87
XX15	L	X	L	PC2	U941	87
XX17	L	X	L	PC4	U945	87
XX1B	L	X	L	CNTL3	U765	79

91AE24 CONTROLLER INTERFACE READBACK CIRCUITRY ◇80◇

This schematic shows the tri-state readback buffers that pass data from the 91AE24 to the DAS Controller board. Data passes through these buffers from locations throughout the module. The buffers are enabled by U998 (schematic 80). Table 4-7 provides a list of the signals that enable these buffers.

Schematic 80 also shows part of the communication interface to the acquisition probes. 91AE24 compatible probes have a serial communication line for probe identification. Data is clocked out of the probes with the DATA CLOCK signal through pin 28 of J101, J401, and J701 (schematic 80). Data is received back from the probes through pin 34 of J101, J401, and J701 (schematic 80). For more information about these signals refer to the probe interface circuit shown on schematic 82.

91AE24 PROBE A AND B RECEIVERS ◈81▷

Probe A Receiver

91AE24 modules receive 8 data channels from each probe, but no clock or qualifier signals; those are received exclusively by 91A24 modules. All eight of the receiver channels are identical. They convert differential ECL signals into the TTL signals that the login registers expect. Figure 4-3 shows one of the channels. This description refers to Figure 4-3.
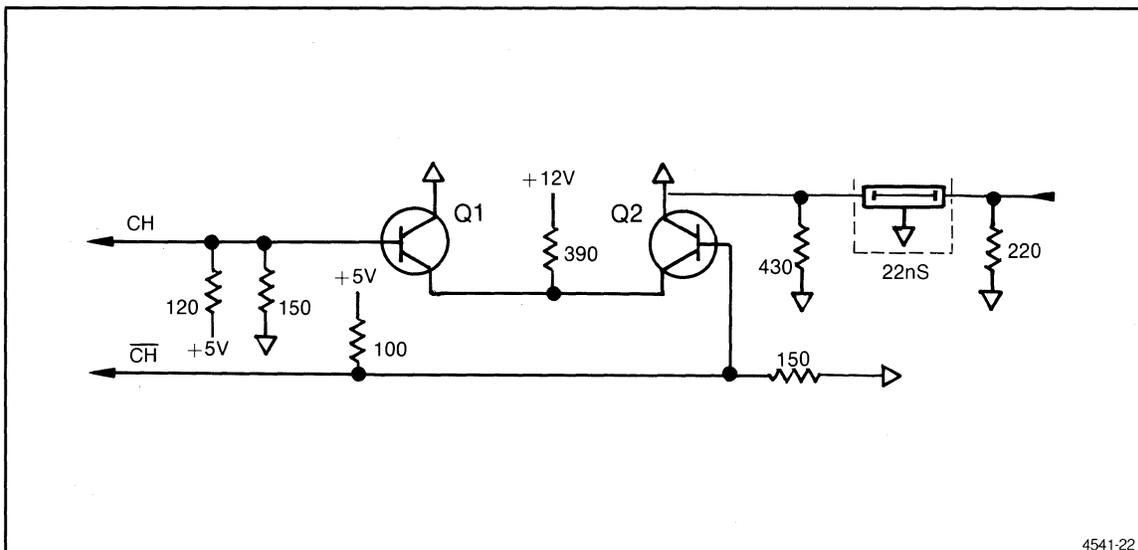
Figure 4-3. 91AE24 probe receiver.

Transistors Q1 and Q2 and the 390 Ω resistor are a differential TTL-to-ECL translator. The 150 Ω and 120 Ω resistors are line terminators that match the impedance of the transmission line. The 22 ns delay line adds time to the data signal so the corresponding clock and qualifier signals can be processed before the data is clocked in. The 430 Ω and 220 Ω resistors are signal terminators for the delay line.

Probe B Receiver

The probe B receiver is identical to the probe A receiver. Refer to the probe A receiver description for more information.

91AE24 PROBE INTERFACE AND PROBE C RECEIVER ◈82▷

Probe C Receiver

The probe C receiver is identical to the probe A receiver. Refer to the probe A receiver description for more information.

Probe Interface

The probe interface controls the probe's acquisition threshold and reads the probe status.

Probe Status Readback. The DAS polls all 91AE24 probe connectors to see if probes are attached. The same circuitry is used to sense if the Pod ID button is depressed and to identify the type of probe attached. Each probe is identified by an eight-bit code that is received serially by the 91AE24.

The DAS polls the probe by pulling the probe's R(L)/W(H) line high. The DAS does this by writing ones into bits 4, 5, and 6 of register U925 (schematic 82). At this writing, only P6460 and P6462 acquisition probes can be used with the 91AE24. Since neither of these probes use the DATA IN signal from the module, bits 0, 1, and 2 of this register are not used.

Once the R(L)/W(H) signal is high, the 91AE24 toggles the DATA CLOCK signal through data selector U998 (shown on schematic 80). Each rising edge from DATA CLOCK clocks out one bit of a word from each attached probe. This DATA OUT signal from each probe is read through register U775, also on schematic 80.

When no probe is plugged in, the DATA OUT signal is pulled high by pull-up resistors on the 91AE24 module. Any probe plugged into the module pulls this line low, which is how the DAS knows when a probe is plugged in. To read the probe type or monitor the Pod ID button, the 91AE24 toggles the DATA CLOCK signal eight times. The first seven serial bits from the probe identify the type of probe and the probe's state. The eighth bit is low when the Pod ID button is depressed.

Probe Threshold DAC. Digital-to-analog converter U918 (on schematic 82) sets the threshold voltage of the 91AE24 probes. To program the digital-to-analog converter (DAC), the 91AE24 controller interface places a control word on D0-D7 and toggles the $\overline{\text{THRESHOLD}}$ line. Programming the DAC with FF_{16} sets the DAC voltage to $+6.40$ V, while 00_{16} sets the voltage to -6.35 V. If the DAC is programmed with 80_{16}, the DAC outputs 0.00 V.

Potentiometer R902 adjusts the offset of the DAC, so when the DAC is programmed with 80_{16}, the DAC outputs 0 V. R110 adjusts the DAC gain so a DAC setting of FF_{16} puts the DAC voltage at $+6.35$ V.

Op amp U808C is configured as an inverting buffer for the DAC output. So the output of U808C, at TP910, is the negative of the voltage from the DAC. Because this is an inverting buffer stage, programming the DAC with FF_{16} results in a probe threshold of -6.35. U808C drives the threshold sensors for the three probes.

Probe Threshold Sensors. There are three probe threshold sensors, one for each probe. Since the three circuits are identical, only the circuit for pod A is described here.

Op amps U711A and D (schematic 82) regulate the threshold for probe A. U711D is configured as a differential amplifier. The inverting input to U711D receives the threshold voltage from DAC buffer (U808C). The non-inverting side of U711D receives USERS GND from the probe. This arrangement adjusts the output of U711D for differences between the DAS ground and the user's ground. Since the threshold voltage goes to U711D's inverting input, the output voltage is the negative of the desired voltage. The next stage inverts the signal again so the signal from the module has the correct polarity.

Op amp U771A (schematic 82) is also a differential amplifier, but its gain and offset are controlled by the attached probe. The probe provides a feedback resistor between VTHRESH and VTHRESH SENSE so the voltage received from the op amp has the correct gain factor. For example, a P6460 acquisition probe provides a 10,500 Ω feedback resistor which, in parallel with 200K Ω R706, gives the circuit a gain of $-1/4$.

The probe also provides the OFFSET SENSE signal to offset U771's output voltage into the range required by the probe. For example, a P6460 acquisition probe provides -1.2 V as the OFFSET SENSE, so the output signal is referenced to -1.2 V rather than ground. This op amp is also configured as an inverter, which cancels out the inversion in the previous stage.

91AE24 LOGIN REGISTERS ◇83◇

The login registers schematic shows the 91AE24 login registers and the clock distribution circuits. The 91AE24 circuitry on this schematic is identical to the 91A24 circuitry shown on schematic 72. The only difference between the two schematics is the way the clock distribution circuits are connected. For this reason, the clock distribution circuit on schematic 83 is described next.

Clock Distribution

The clock distribution functional block is where the acquisition clocks generated by the 91A24 are received by the attached 91AE24 modules. The last 91AE24 in the daisy chain has J173, J183, and J185 (on schematic 83) jumpered as shown on the schematic. 91AE24 modules between the 91A24 and the final 91AE24 have the jumper on pins 7 and 3 and the jumper on pins 8 and 4 removed, as shown in the schematic inset. A twisted-pair cable runs from pins 7 and 8 to the next 91AE24 module.

Comparators U275A, B, and C in the clock distribution block convert differential ECL into single-ended ECL clock signals. These clock signals are used by the data login registers (on schematic 83) and by the master clock selector (U721 on schematic 87).

All Other Circuits On Schematic ◇83◇

For descriptions of all other circuits on schematic 83, refer to the *91A24 Login Registers* (schematic 72) description. The 91A24 login clock generator, V_{bb} generator, and login registers are shown on schematic 72.

91AE24 ACQUISITION MEMORY ◇84◇

The acquisition memory consists of four parts:

1. Data registers to allow setup time before data is stored.

2. A chip-select generator that determines when data is stored in the acquisition memory

3. The acquisition memory RAM which stores the acquired data.

4. A memory address register that determines the RAM address where storage occurs.

The 91AE24 acquisition memory circuits are identical to the 91A24 acquisition memory. Refer to the *91A24 Acquisition Memory* (schematic 73) theory of operation for a description.

91AE24 DATA QUALIFIER WORD RECOGNIZERS ◇85◇

This schematic shows the circuitry for the four non-stack based word recognizers. These word recognizers are controlled through the 91A24 Trigger Specification sub-menu. The word recognizers can control data storage (BEGIN STORE IF, END STORE IF, and STORE ONLY IF conditions), control the stack-based word recognizer (RESET), and control triggering (OR TRIGGER).

Data Qualifier Word Recognizer RAM

The data qualifier word recognizer is RAM-based, much like the 91A32 Data Acquisition module word recognizers. The RAMs (U151, U351, and U551 on schematic 85) are programmed to react to specific words on the DR0-DR23 bus.

To understand how the RAM is used for word recognition, consider the RAM as a set of addressable registers. The RAM is programmed by writing 1s in all the addresses that correspond to the words to be recognized. 0s are written into all other addresses. After programming, the stream of data containing the word to be recognized is used to address the RAM. The RAM indicates word recognition by outputting a 1.

Since the words to be recognized may have X (don't care) as an element, programming becomes slightly more complicated. For every X (don't care) entered in a word recognizer field, twice as many words meet the triggering requirements. For example, if the word to be recognized is 10100110_2 a single 1 must be written into the RAM. If $X0100110_2$ is to be recognized, 1s must be loaded into both addresses 00100110_2 and 10100110_2. If $XX100110_2$ is to be recognized, 1s must be loaded at four different addresses. So, if $XXXXXXXX_2$ is to be recognized, all 256 addresses must have 1s written in them.

Since 24 bits must be monitored for word recognition, three RAMs with 8 address lines each are used (for a total of 24 address lines). Each RAM recognizes 8 of the 24 bits involved. All three of the RAMs must recognize their word segments at the same time for word recognition to occur.

Each of the three RAMs have four data lines, so four independent words can be recognized. All four of the data lines in each RAM are programmed independently, so signals A1, B1 and C1 are used to recognize one word. Signals A2, B2, and C2 recognize another word.

Data Qualifier Word Recognizer

The data qualifier word recognizer completes the work of the data qualifier word recognizer RAM. AND gates U168B and U261A, B, and C (on schematic 85) make sure that all three 8-bit segments of a word are true before a word is recognized.

The outputs of the four AND gates are wire ANDed with the data qualifier word recognizer outputs from the 91A24 and all other 91AE24 modules. These word recognizer signals come from the other modules through the cables that go across the top of the modules. Wire ANDing these signals means that all 91A24 and 91AE24 modules must recognize their portions of a word at the same time for word recognition to occur.

The four word recognition signals that result from all these wire ANDed signals are buffered by U198B and U291A, B, and C (schematic 85). Exclusive-OR gates U291A, B, and C allow three of the signals to be inverted by changing one bit at the controller interface. OR gate U198B allows the DAS Controller board to assert the ENABLE signal through the controller interface.

Storage Control Circuitry

The circuitry surrounding U281, U288, and U478B (on schematic 85) determines when data is stored depending on the data qualifier word recognizer conditions. This circuitry operates identically, and is always programmed identically, to the 91A24 storage control circuitry. For more information on this circuit, refer to the *91A24 Storage Control Circuitry* description. The 91A24 storage control circuitry is shown on schematic 74.

91A24 STACK WORD RECOGNIZER ⬦86⬦

The stack word recognizer is the hardware implementation of the sequential word recognizer in the 91A24 Trigger Specifiction sub-menu. The stack word recognizer is based on RAMs U148, U248, and U448 (on schematic 86). The RAMs recognize words by receiving acquired data on their address lines.

Sixteen levels of triggering are accomplished with a 4-bit stack pointer SP0-SP3 from U571 (on schematic 86). The stack pointer addresses the stack word recognizer RAMs. The value from the stack pointer effectively divides the stack word recognizer RAMs into sixteen separate sections. The stack pointer provides the address for the stack control RAM as well. The stack control RAM contains control bits for whether the recognition condition is WHEN or WHEN NOT.

Stack Pointer

The stack pointer (U571 on schematic 86) is a four-bit synchronous up counter. The POINTER CLK signal, which increments the stack pointer, comes through J181 from the 91A24 stack occurrence counter on schematic 75. This signal increments the 91AE24 stack pointer whenever the 91A24 stack pointer increments, so the 91A24 and the 91AE24 are always at the same stack level. The stack pointer can also be incremented by the DAS Controller board by pulling $\overline{\text{STACK CLK EN}}$ low and toggling $\overline{\text{STACK PTR CLK}}$.

Inverter U578D prevents the stack pointer from wrapping from 1111_2 to 0000_2 by disabling the counter. The stack pointer is cleared by the reset circuitry through J181 (shown on 91A24 schematic 76), and loaded by the $\overline{\text{STACK PTR LD}}$ signal.

SC0 from stack control RAM U555 is connected to an enable pin of the stack pointer. SC0 goes low when the 91A24 is at the last programmed level of the stack, so SC0 being low disables the counter. This prevents the stack from incrementing past the last programmed level.

U588A clears the stack pointer when the reset word is recognized by the data qualifier circuit. The $\overline{\text{OR TRIGGER}}$, $\overline{\text{DUAL QUAL}}$, and $\overline{\text{STACK WR}}$ signals prevent the reset word from clearing the stack pointer except under the proper conditions.

Stack Word Recognizer RAM

The stack word recognizer is RAM-based, much like the data qualifier word recognizers. The RAMs (U148, U248, and U448 on schematic 86) are programmed to react to specific words on the DR0-DR23 bus according to the value of the stack pointer (SP0-SP3).

To understand how the RAM is used for word recognition, consider the RAM as a set of addressable registers. The stack word recognizer uses three RAMs with 12 address lines each; four of the address bits indicate the position in the stack, the other eight address bits are used for word recognition. The four stack pointer bits (SP0-SP3) effectively divide the RAMs into sixteen separate segments. The word recognizer segments are activated according to the value on SP0-SP3.

The remaining eight bits of each RAM perform the actual word recognition. The RAM is programmed by writing 1s in all the addresses that correspond to the words to be recognized. 0s are written into all other addresses. After programming, the stream of data containing the word to be recognized is used to address the RAM. The RAM indicates word recognition by outputting a 1.

Since the words to be recognized may have X (don't care) as an element, programming becomes slightly more complicated. For every X (don't care) entered in a word recognizer field, twice as many words meet the triggering requirements. If the word to be recognized is 10100110_2 a single 1 must be written into the RAM at address 10100110_2. If $X0100110_2$ is to be recognized, 1s must be loaded into both addresses 00100110_2 and 10100110_2. If $XX100110_2$ is to be recognized, 1s must be loaded at four different addresses. So, if $XXXXXXXX_2$ is to be recognized, all 256 addresses in the selected RAM segment must have 1s written in them.

Since 24 bits must be monitored for word recognition, three RAMs with 8 word recognition lines each are used (for a total of 24 word recognition lines). Each RAM recognizes one byte of the 24 bits involved. All three of the RAMs must recognize their byte of the word at the same time for word recognition to occur.

Stack Word Recognizer Control

The stack word recognizer control circuit has two parts: a three-input AND gate and an exclusive OR gate.

U168A is the AND gate for the three 91AE24 stack word recognizer RAMs (schematic 86). When all three of the stack word recognizer RAMs (U148, U248, and U448) output high levels, AND gate U168A outputs a high to indicate word recognition.

The output of AND gate U168A (schematic 86) is wire ANDed through J171 to the stack word recognizer outputs of all 91A24 and 91AE24 modules in the mainframe. So all 91A24 and 91AE24 modules must recognize their stack words at the same time for stack word recognition to occur.

Exclusive OR gate U291C (schematic 86) implements the WHEN/WHEN NOT field in the 91A24 Trigger Specification sub-menu. While the stack is at a WHEN level, the SC3 signal is high, so the word recognition signal is inverted. When a WHEN NOT level is reached, SC3 goes low, so the word recognition signal is not inverted. The output of the exclusive OR gate is used by four-input NAND gate U558A to prevent the pointer from being reset whenever a valid stack word is recognized.

Stack Control RAM

The DAS Controller board loads the stack control RAM (U555 on schematic 86) with stack level conditions before acquisition starts. Then during acquisition, the RAM is addressed by the stack pointer (SP0-SP3). The RAM outputs control signals SC0-SC3 as appropriate for each of the stack levels. The 91AE24 module only uses SC0 and SC3. SC1 and SC2 are not used. SC0 and SC3 control:

- last level (SC0)

- WHEN and WHEN NOT (SC3)

91AE24 MASTER CLOCK SELECTOR ◈87◈

Master Clock Selector

The master clock selector chooses the master 91AE24 clock with a set of CMOS registers (U938, U941, and U945 on schematic 87). Power for the registers is supplied through Q951, which drops the +5 V supply down to approximately +4.5 V. +4.5 V is used for the register's power supply so the register's outputs are ECL compatible.

Inputs PC0, PC2, and PC4 from the controller interface (on schematic 79) are latch clocks. When one of these signals is toggled, the data on D0-D7 is loaded into the corresponding register to enable the correct master clock.

The AND gates in U721 (on schematic 87) select the master clock. The master clock is chosen in the 91A24 Trigger Specification sub-menu with the MASTER CLK field. Once the selection is made, one of control bits CA6, CB6, CC6, or CA7 goes high to pass the selected clock. The other bits remain low so the clocks they control are masked out.

CA7 only goes high to select the single step clock. $\overline{\text{SINGLE STEP}}$ is used only for diagnostics and to program 91A24 and 91AE24 acquisition modules.

Master Clock Distribution

The master clock distribution circuitry translates the single-ended ECL output of U721 to TTL levels. The resulting master clock is divided into two identical clocks, MASTER CLK II and III, to distribute the loading on the clocks. MASTER CLK I is not used by 91AE24 modules.

+3 V Power Supply

The +3 V power supply is a voltage-regulated current sink for the ECL terminating resistors.

Voltage divider R905 and R906 (on schematic 87) set a reference voltage of +3 V for the non-inverting input of op amp U904. The feedback loop through Q901 biases the transistor so the emitter follows the reference voltage. Since Q901 acts as a current sink for terminators, there is always sufficient current to maintain the +3 V.

91A24/91AE24 VERIFICATION PROCEDURES

INTRODUCTION

This portion of the 91A24/91AE24 Service Addendum contains three main parts: the functional check procedures, the adjustments procedures, and the performance check procedures. These procedures, along with the test setup information at the beginning, allow a qualified technician to verify the operation of a 91A24 or 91AE24 module.

These instructions are limited to the procedures necessary to verify the modules. Detailed information about normal menu operation may be found in the *91A24, 91AE24, and P6460 Operator's Addendum* and the *DAS 9100 Series Operator's Manual*. Detailed information about diagnostic menu operation is located in the *DAS 9100 Series Service Manual*. Service information for the P6460 Data Acquisition Probe is covered in the *P6460 Instructions*.

Functional Check Procedures. These tests verify that the module is basically operational. The procedures exercise the main user interfaces of the module to verify their operation. The procedures also check the main internal features for operation. These tests can be used to see if adjustment and/or repair is necessary.

Adjustment Procedures. These procedures are designed to bring the module to or within product specifications. If the module cannot meet the specification, repair is necessary.

Performance Check Procedures. These tests provide a detailed check of internal and external product characteristics. All specifications listed in the performance requirement column of the specifications are verified. These checks can be extensive and time-consuming. Under normal circumstances the functional check procedures provide an adequate test of product performance in a less costly or time-consuming manner.

TEST SETUP INFORMATION

The setups for each functional and performance verification procedure rely on the setups left from the previous test. If you are not starting at the beginning test and working through sequentially, be sure to check that you have the equivalent setup for that point in the procedure.

SUGGESTED TEST INSTRUMENTS

There are three different sets of procedures in this section: the functional check, the adjustments, and the performance check. Following are lists of the instruments that are used at some point in each of these procedures, along with their Tektronix equivalents.

NOTE

Each separate procedure will use only some of the instruments given in these tables. Check the procedure in question before appropriating test instruments.

Table 5-1
EQUIPMENT NEEDED FOR THE FUNCTIONAL CHECK PROCEDURES

Equipment	Specifications	Equivalent Tektronix Equipment
DAS 9100 Series Mainframe	No substitute allowed	
91A24 Data Acquisition Module	No substitute allowed	
91E24 Data Acquisition Module (Optional)	No substitute allowed	
91P16 Pattern Generator Module	No substitute allowed	
91P32 Pattern Generator Module	No substitute allowed	
P6460 Data Acquisition Probe kits (3 needed to test only 91A24; 4 needed to test 91AE24 and 91A24)	No substitute allowed (Kits include leads and TTL-type grabber tips.)	10" lead set is Tektronix P/N 012-0747-00. TTL-type grabber tips have Tektronix P/N 020-0720-00 (Optional) Diagnostic lead sets (3); can be used in place of the grabber tips if you are testing only a 91A24 module. Tektronix P/N 012-1000-00
P6455 Pattern generator probe kits (4 needed)	No substitute allowed. (Kits include twisted pair lead set and grabber tips.)	Lead set is Tektronix P/N 012-0926-00
(Optional) 91A24 Interconnect Cable Assembly, 28 cm (11 in.) (7 required)	No substitute allowed	Tektronix P/N 175-8166-00
10-pin square pin connectors (3)	0.025 inch diameter square pins, 10-in-line	Tektronix P/N 131-1934-00 (Note: This pin set comes with 36 pins in-line; break to length.)
(Optional) Oscilloscope	Dual trace, 100 MHz	465
(Optional) Oscilloscope probe	X10, 100 MHz	P6106
Ground bar	Short length of uninsulated wire (approx. 5-10 inches) to ground probes	

Table 5-2
EQUIPMENT NEEDED FOR THE ADJUSTMENT PROCEDURES

Specifications	Equipment	Equivalent Tektronix Equipment
DAS 9100 Mainframe	No substitute allowed	
91A24 Data Acquisition Module	No substitute allowed	
91AE24 Data Acquisition Module (Optional)	No substitute allowed	
DAS 9100 Series Service Maintenance Kit (for extender board)	No substitute allowed	
91A24 Interconnect Cable Assembly, 28 cm (11 in.) (7 required)	No substitute allowed	Tektronix P/N 175-8166-00
Oscilloscope	Dual trace, 100 MHz	465
Oscilloscope probe	X10, 100 MHz	P6106
Digital Multimeter (DMM)	0.05% dc V accuracy	DM 501A (with TM 500 mainframe)

Table 5-3
EQUIPMENT NEEDED FOR THE PERFORMANCE CHECK PROCEDURES

Specifications	Equipment	Equivalent Tektronix Equipment
DAS 9100 Mainframe	No substitute allowed	
91A24 Data Acquisition Module	No substitute allowed	
91AE24 Data Acquisition Module (Optional)	No substitute allowed	
P6460 Data Acquisition Probe Kits (3) (kit includes lead sets and grabber tips)	No substitute allowed	
DAS 9100 Series Service Maintenance Kit	No substitute allowed	Tektronix P/N 067-0980-00
91A24 Interconnect Cable Assembly, 28 cm (11 in.) (7 required)	No substitute allowed	Tektronix P/N 175-8166-00

Table 5-3 (cont.)
EQUIPMENT NEEDED FOR THE PERFORMANCE CHECK PROCEDURES

Specifications	Equipment	Equivalent Tektronix Equipment
Dual-trace Oscilloscope system	Dual-trace, 250 MHz bandwidth, two x10 250 MHz oscilloscope probes	485 oscilloscope with P6106 probes
10-pin square pin connectors (3)	0.025 inch diameter square pins, 10-in-line	Tektronix P/N 131-1934-00 (Note: This pin set comes with 36 pins in-line; break to length.)
Pulse generator	250 MHz	PG 502
Pulse generator	50 MHz	PG 508
Digital multimeter (DMM)	0.05% dc V accuracy	DM 501A
TM 500 Mainframe	No substitute allowed	TM 504 or higher
Setup and Hold Time Test Fixture (including lead sets)	No substitute allowed	Tektronix P/N 067-1037-00
(Optional) 10-wide comb with harmonica connector (1 per probe)		Tektronix P/N 012-0800-00
10-inch BNC cables (4)		Tektronix P/N 012-0208-00
BNC T adapters (3)		Tektronix P/N 103-0030-00
Probe-tip-to-BNC adapters (2)		Tektronix P/N 013-0084-01
Dual-lead adapter		Tektronix P/N 015-0325-00
Probe tip, flexible		Tektronix P/N 206-0193-00

FUNCTIONAL CHECK PROCEDURES

The functional check procedures verify that all the major sections of the module being checked are operational. You can used these tests to determine whether adjustment or repair is necessary.

All of the tests in this section are designed to test either the 91A24 or the 91AE24 with the following exceptions:

- When testing a 91AE24 module, skip the SYNC OUT portion of functional test 8. (This test is marked *91A24 only.)*

- There are no input driver clock tests performed on the 91AE24 itself; the clock signal is acquired from the 91A24 module. Clock tests for the 91AE24 verify the latches and CLK I, II, and III.

- Equipment setup directions and probe connections for testing 91AE24 modules are indicated where relevent.

- Only one 91AE24 is verified at a time. To verify additional 91AE24 modules, replace the tested module with an untested module, and rerun the tests.

NOTE

If you are testing a 91A24 module by itself (without any 91AE24 modules), disconnect any 91AE24 modules in the mainframe. Taking this precaution eliminates the risk of a word recognizer failure on a 91AE24 module causing a diagnostics failure on the 91A24 module.

You will need the following equipment to perform the functional check:

- DAS 9100 Mainframe, with:
    1 91A24 Data Acquisition module in slot 1
    1 (Optional) 91AE24 Data Acquisition module in slot 2
    3 P6460 Data Acquisition probe kits (kit includes lead sets and grabber tips)
    1 91P32 Pattern Generator module in slot 3
    1 91P16 Pattern Generator module in slot 4
    4 P6455 Pattern Generator probe kits (kit includes lead sets and
        grabber tips)
    3 10-pin square pin connectors

- 1 (Optional) 100 MHz dual-trace oscilloscope with probes

(1) Mainframe Setup for the Functional Check

The following steps configure the DAS for the functional check.

NOTE

Although you can place modules in other slots for the following procedures, the setup listed here is recommended. Using the same module configuration each time you perform the procedure allows you to save test patterns on tape. For instructions on how to save tape files, see the DAS 9100 Series Operator's Manual.

CAUTION

Do not install or remove any electrical module or sub-assembly while the power is on. Doing so may damage the sub-assembly.

1.   Turn off the mainframe.

2.   Install the data acquisition and pattern generation modules as listed in Table 5-4.

Table 5-4
MODULE BUS-SLOT PLACEMENT

Module	Slot
91A24	1
91AE24 (optional)	2
91P32	3
91P16	4

3.   Check that the factory-installed jumpers on the 91A24 module are in the correct positions:

•   J173, J183, and J185 should each have four jumpers installed parallel to the edge of the board.

•   J271 (pins 1 and 2) and J272 (pins 1 and 2) should each have black jumpers installed perpendicular to the edge of the board.

If you have a 91AE24 module installed, also check the interconnect cables between the 91A24 and the 91AE24, as well as the jumpers on the 91A24. See Figure 5-1.
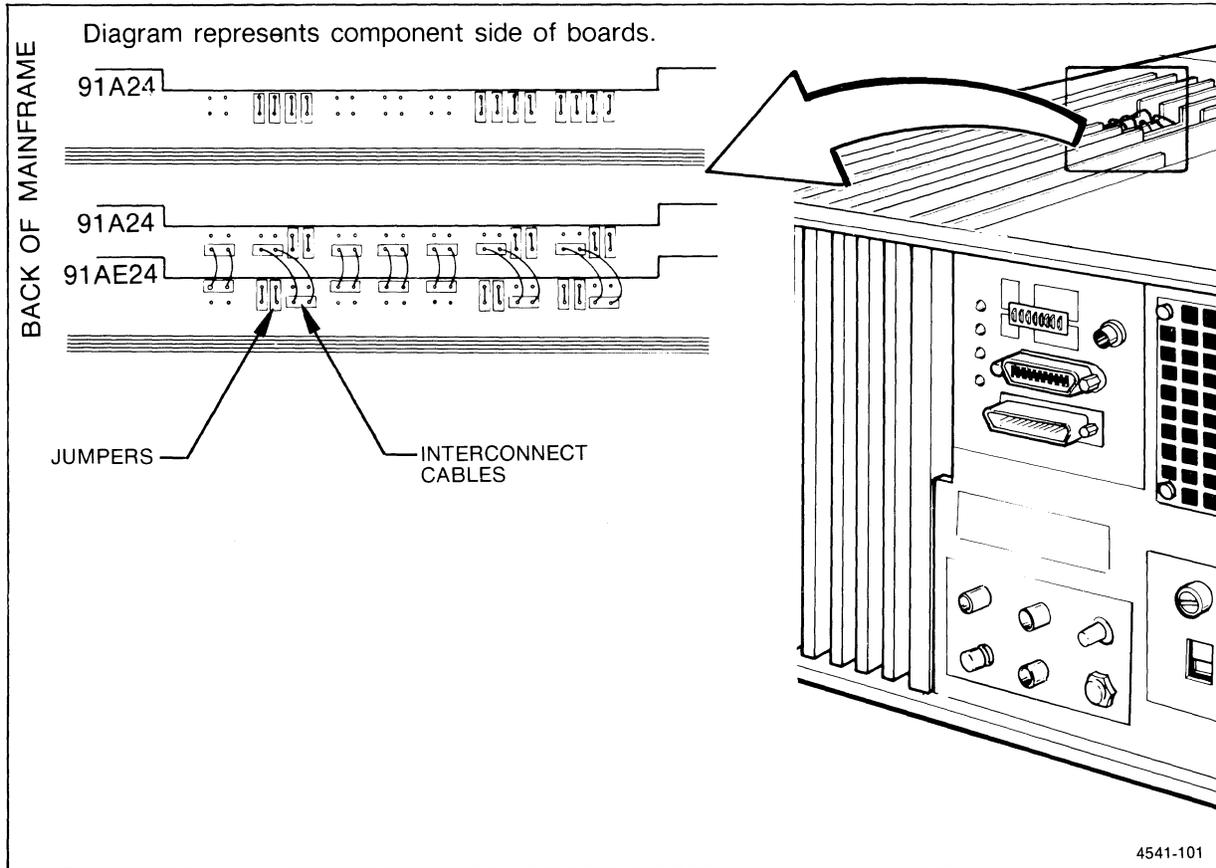
Figure 5-1. 91A24 and 91AE24 jumpers and interconnect cables. The jumpers are the small black 2-pin connectors. Interconnect cables are pin connector assemblies with wires.

DIAGNOSTIC TESTS

(2) Executing the Diagnostic Self-Test
(91A24 Diagnostic Functions 0-5)
(91EA24 Diagnostic Functions 0-3)

NOTE

Refer to the Maintenance: Troubleshooting *section of this addendum for a detailed description of these tests.*

Use the following procedure to enter the DAS diagnostics menu and operate all of the ALL mode tests at each level.

1. Turn on the mainframe while holding down the STOP key on the keyboard. This causes the power-up self-test to fail.

2. Press START SYSTEM to enter the Diagnostics menu.

3. Select SINGLE in module field.

4. Move cursor to slot field, enter 1 to test the 91A24 in slot 1. (If you are testing a 91AE24, enter 2 for slot 2.)

5. Leave the MODE field set to ALL (the default value).

6. Press START SYSTEM to begin test execution.

The DAS diagnostics will perform all available tests on the slot. Diagnostics tests CNTR TIMR, MEM ADDR, ACQ MEM, STK PNTR, WRD REC, and OCCR CNTR should all pass. (Tests PRB CLK EXC and DAC are not run.)

PROBE TESTS

(3) Probe Connector Functional Tests

For these tests, a single P6460 probe must be connected successively to pods A, B, and C of the 91A24 Data Acquisition module.

This test verifies the pod ID, probe present, and probe disconnected functions. Specifically it verifies:

*   The operation of the probe R/W line (U958-3 — 91A24 schematic 68, 91AE24 schematic 79) and the pod R/W IC U925 (91A24 schematic 71, 91AE24 schematic 82).
*   The runs from U925 (91A24 schematic 71, 91AE24 schematic 82) to the probe connectors.
*   The POD STATUS register U775 (91A24 schematic 69, 91AE24 schematic 80) and its selector U998 (91A24 schematic 69, 91AE24 schematic 80).

To run this test:

1. Connect a P6460 probe to the pod A connector of the 91A24 in slot 1. Verify that the message PROBE CONNECTED appears in the upper left corner of the DAS display.

2. Press the pod ID button on the P6460 probe in pod A, and verify that the display shows POD 1A in the upper left corner.

3. Remove the probe and verify that POD 1A DISCONNECTED appears in the upper left corner of the DAS display.

4. Repeat steps 1 through 3 of this test sequence for pods B and C on the 91A24 module.

(4) Probe Clock Exerciser (PRB CLK EX) Test
(91A24 Diagnostic Function 7)
(91AE24 Diagnostic Function 5)

This test verifies the clock generator circuitry of a 91A24 module, and the clock driver circuitry of a 91AE24 module. For details of the circuitry covered by this test, see the explanation of the PRB CLK EX diagnostic test in section 7 of this addendum. This test requires three P6460 probes to test a 91A24 and six P6460 probes to test a 91AE24.

1. **91A24.** If you are testing only a 91A24, disconnect it from any 91AE24 modules in the mainframe, and terminate those connections with jumpers as shown in Figure 5-1.

    91AE24. To test a 91AE24 module, first complete the test for the 91A24 module. Reconnect the 91A24 to the 91AE24 with interconnect cables and jumpers (as shown in Figure 5-1).

2. **91A24.** Connect one P6460 probe to each 91A24 pod connector (pods A, B, and C).

    91AE24. In addition to the three P6460 probes connected to the 91A24, connect three P6460 probes to the 91AE24 (pods A, B, and C).

3. **91A24.** Select SINGLE mode and the PRB CLK EX test in the DAS Diagnostics menu.

    91AE24. Select SLOT 2, SINGLE mode, and the PRB CLK EX test in the DAS Diagnostics menu.

4. Press START SYSTEM.

5. Verify that all tests pass.

PATTERN GENERATOR-DRIVEN TESTS

(5) Setup for Pattern Generator-Driven Tests
(Functional Tests 6-13)

91A24 Probe Setup. The probe setup described in this section supports testing a 91A24 module (three channels). To test a 91AE24 module you must also make the probe connections described under the heading *91AE24 Probe Setup*.

The 91A24 probe connections are presented in three different formats: they are summarized in Table 5-5, illustrated in Figure 5-2, and described in detail in the following text.

Table 5-5
PROBE CONNECTIONS FOR 91A24 FUNCTIONAL TEST

91A24 P6460 Probe	91P16 P6455 Probe	91P32 P6455 Probe
A pod to square pins to B pod to square pins to C pod to square pins to	B pod C pod	 A pod
A Clock (CLK, white) to B Clock (CLK, white) to C Clock (CLK, white) to	B Strobe (white) C Strobe (white)	 A Strobe (white)
A Qualifier (Q, gray) to B Qualifier (Q, gray) to C Qualifier (Q, gray) to		B bit 0 (black) B bit 1 (brown) B bit 2 (red)
A pod user's ground to B pod user's ground to C pod user's ground to all pod's user's gnds to (use ground bar)	B pod VL C pod VL both pod's VLs	 A pod VL both pod's VLs

NOTE

If only a 91A24 is being tested, a diagnostic lead set can be used in place of the square-pin connector and flying lead sets. (The diagnostic lead set is included in the Service Maintenance Kit.)

For further details on connecting probes with the lead sets, refer to the DAS 9100 Series Service Manual.
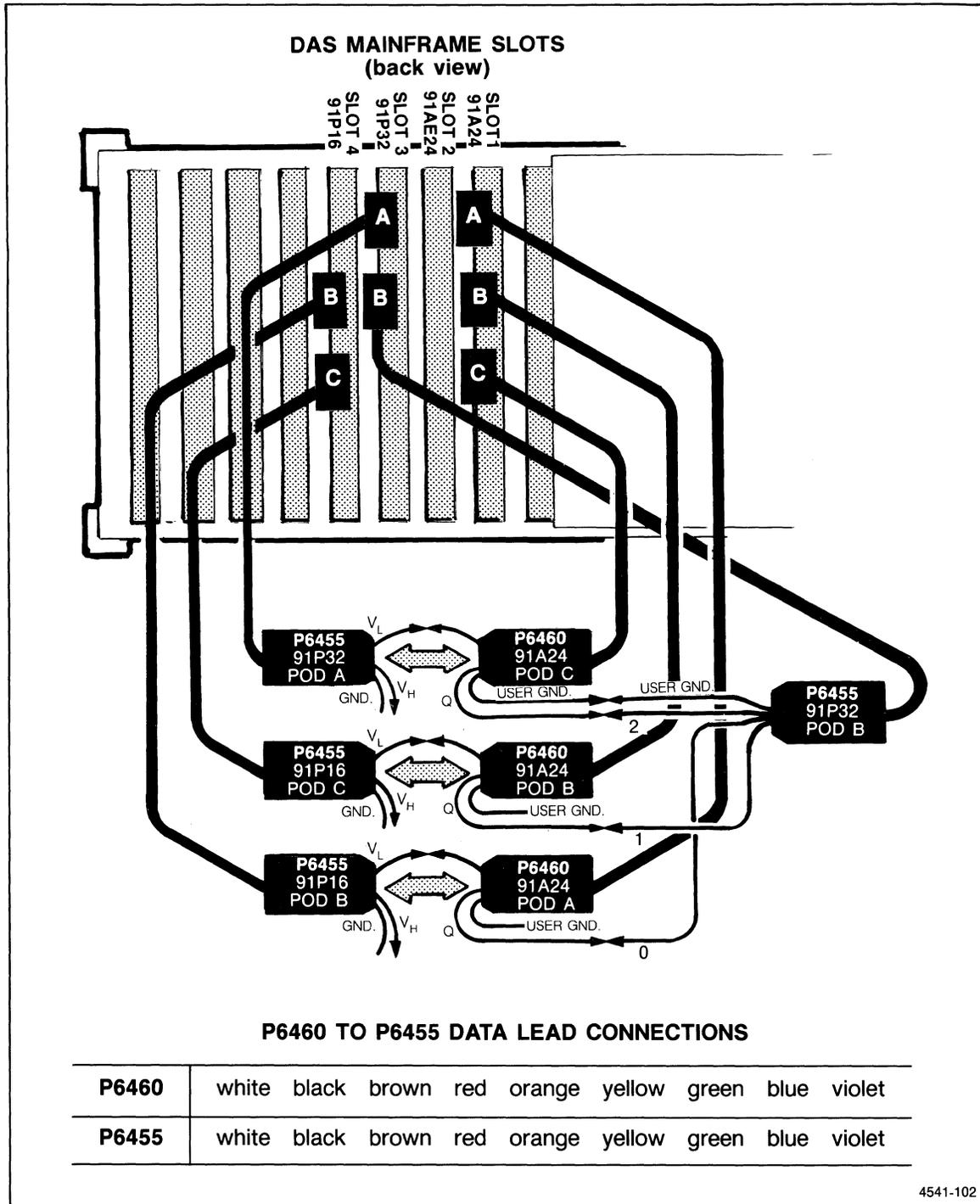
Figure 5-2. Probe connections for the 91A24 functional tests.

1. Connect two P6455 pattern generator probes to pod connectors B and C of the 91P16. Set the diagnostic slide switch on the back of both probes to AUX.

2. Connect the other two P6455 probes to pod connectors A and B of the 91P32. Set the diagnostic slide switch on the back of both probes to AUX.

3. Connect three P6460 acquisition probes to pod connectors A, B, and C of the 91A24. When the P6460 is installed, the mainframe should beep and the message POD XA CONNECTED should show on the screen (where X represents the slot number).

4. Connect a 10-inch lead set to each of the data acquisition probes from the 91A24 or 91AE24.

5. Connect these leads to 10-pin square pin connectors (one set of leads to each 10-pin square pin connector). Do not attach the gray lead to the connector.

6. Connect a pattern generator lead set to the pattern generator probes from pod connectors B and C of the 91P16, and from pod connectors A and B of the 91P32.

7. Connect the twisted-pair leads from the pattern generator probes to the square-pin assemblies attached to the data acquisition probes as follows:

   • 91A24 probe from pod connector A to 91P16 probe from pod connector B;
   • 91A24 probe from pod connector B to 91P16 probe from pod connector C;
   • 91A24 probe from pod connector C to 91P32 probe from pod connector A.

   Connect the pattern generator (twisted-pair) leads color-to-color to the acquisition leads (straight) with the following qualifications:

   • Connect the white lead of the black-white twisted pair to the square pin assembly opposite the white lead from the data acquisition probe. Connect the black wire of the black-white twisted pair to a ground bar. You can use any short length (5 - 10 inches) of bare wire for the ground bar. You will use this wire to ground all the probes.
   • Do not connect the gray-black twisted-pair from the pattern generator probe to the square pin assembly.

8. Connect the Q lead (gray) from the data acquisition probe from 91A24 pod A to the bit 0 lead (black) from the pattern generator probe connected to 91P32 pod B.

9. Connect the Q lead (gray) from the data acquisition probe from 91A24 pod B to the bit 1 lead (brown) from the pattern generator probe connected to 91P32 pod B.

10. Connect the Q lead (gray) from the data acquisition probe from 91A24 pod C to the bit 2 lead (red) from the pattern generator probe connected to 91P32 pod B.

11. Connect user's ground from all P6460 probes to VL of all P6455 probes using a bar adapter.

91AE24 Probe Setup. To test a 91AE24 module you must make the following probe connections:

1. Make all 91A24 probe connections described under *91A24 Probe Setup.*

2. Connect a fourth P6460 probe to the 91AE24. You will need to connect this probe successively from pods A to B to C to test all channels of the 91AE24 module.

3. Connect the 91AE24 probe to the corresponding probe on the 91A24. For example, when the 91AE24 probe is in the pod A connector, connect that probe to the 91A24 probe in pod A. Make this connection by attaching grabber tips from the 91AE24 probe leads to the exposed section of pin on the square pin adapter already connected to the 91A24 probe. If for some reason using the grabber tips is not adequate, you can connect the leads directly by attaching them to a duplexed square pin adapter. To make a duplexed square pin adapter, take two square pin assemblies and interlace them to form a row of 10 Xs. Solder at each of the 10 connections.

4. Enter the Channel Specification menu and group the channels to match your probe connections. For example, if you are testing 91AE24 pod A, group those channels with the 91A24 pod A channels.

5. Enter the Trigger Specification menu. Program the word recognizer for the 91AE24 pod you are testing to match the corresponding 91A24 pod. For example, if you are testing 91AE24 pod A, match its word recognizer values to those of the 91A24 pod A. Use DON'T CARE values for all pod word recognizers not under test.

(6) Enable/Disable Functions
Stack Word Recognizers
Run Timer and Stop Timer Functions

The following test verifies:

- the dual enable and disable functions.
- stack word recognizers 1 through 6.
- the RUN TIMER and STOP TIMER functions.

To run the test:

1. Enter the Pattern Generator menu. Load the program listed in Figure 5-3.

Function Exercised	SEQ	LABEL	POD3DC HEX	POD3BA HEX	POD4CB HEX	INSTRUCTIONS	STROBES
PATTERN GENERATOR: **PROGRAM**　　　INTERRUPT: CALL ▮▮▮ ON **J**

CLOCK: **100nS**　**TTL**　+ 1.40V　PAUSE ON: **1**　INHIBIT ON: **1**

Function Exercised	SEQ	LABEL	POD3DC HEX	POD3BA HEX	POD4CB HEX	INSTRUCTIONS	STROBES
	0	0	0000	0099	9999		▮▮▮
dual enable	1		0000	0066	6666 ○		
	2		0000	0023	2323 ○		
	3		0000	0049	4949 ○		
disable	4		0000	00B6	B6B6		
	5		0000	00F6	F6F6		
	6		0000	0059	5959		
enable/disable	7		0000	00A6	A6A6 ○		
	8		0000	00E6	E6E6		
	9		0000	002F	2F2F		
	10		0000	00D9	D9D9	REPEAT	255
enable, WR1	11		0000	002E	2E2E ○		
enable	12		0000	0024	2424 ○		
disable	13		0000	00B6	B6B6		
	14		0000	0051	5151	REPEAT	10
enable	15		0000	00AE	AEAE ○		
	16		0000	00EE	EEEE ○		
dual enable	17		0000	0066	6666 ○		
	18		0000	0029	2929 ○		
WR2	19		0000	00D6	D6D6 ○		
	20		0000	0096	9696 ○		
	21		0000	002E	2E2E ○		
	22		0000	00D1	D1D1 ○	REPEAT	5
	23		0000	00D6	D6D6 ○		
WR3, occurrence 1	24		0000	00C5	C5C5 ○		
WR3, occurrence 2	25		0000	00C5	C5C5 ○		
	26		0000	003A	3A3A ○		
WR3, occurrence 3	27		0000	00C5	C5C5 ○		
	28		0000	0085	8585 ○		
dual enable, WR4	29		0000	0064	6464 ○		
WR5	30		0000	008E	8E8E ○		
	31		0000	00AD	ADAD ○		
dual disable	32		0000	0052	5252		
	33		0000	0012	1212		
	34		0000	0049	4949		
	35		0000	00B6	B6B6		
	36		0000	00F6	F6F6		
	37		0000	00D9	D9D9		
dual enable/disable	38		0000	0026	2626		
	39		0000	0006	0606		
enable	40		0000	00AE	AEAE		
	41		0000	000F	0F0F		
WR6	42		0000	00F0	F0F0		
	43		0000	00F2	F2F2		
disable	44		0000	00B6	B6B6	GOTO	0

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Figure 5-3. Pattern generator program for Functional Test 6. A dot next to a program line indicates data you should acquire when you run test 6. The callouts label which function that part of the test exercises. (See Figure 5-5 to see this data in the State Table display.)

2. Go to the Channel Specification menu and change the radix of all groups to BIN (binary). If you are testing a 91AE24, you also need to group the channels to match your probe connections. For example, if you are testing 91AE24 pod A, group those channels with the 91A24 pod A channels.

NOTE

If you are testing a 91AE24, group the pods you are not testing toward the end of the Channel Specification menu. Doing so will make these channels show as the least significant bytes in the Trigger Specification menu, making it easy to change them to DON'T CARE values.

Figure 5-4. **91A24 Trigger Specification menu setup for Functional Test 6.** Hexadecimal values (shown with numbered callouts) indicate possible recognized words.

3. Go to the Trigger Specification menu. If you are testing a 91A24, change the menu to match Figure 5-4. If you are testing a 91AE24, program the word recognizers for the 91AE24 pod being tested to match those of the corresponding 91A24 pod. For example, if you are testing 91AE24 pod A, match its word recognizer values to those of the 91A24 pod A. Use DON'T CARE values for all pods not under test.

NOTE

If you are looking at both 91A24 and 91AE24 values in the Trigger Specification menu in binary, only one group at a time will be displayed. To see the other two groups, press SHIFT SCROLL.

4. Enter the Clock Specification sub-menu and set the internal clock rate to 100 ns.

5. Press the START SYSTEM key.

6. Verify that the TIME= field shows 3.2 μS.

7. Go to the Channel Specification menu. Change the radix of all groups to hexadecimal.

8. Verify the data acquired. Compare your data with Figure 5-5. If any of the acquired data is different from the data shown, use the callout on that line of the State Table display to identify the function tested by that part of the program. For example, if your data corresponding to sequence 518 in Figure 5-5 is other than AE AE AE, suspect the enable function. If you have acquired extra data that is not shown in the State Table display, look at the callouts in the pattern generator program shown in Figure 5-3 to determine which function is suspect.

9. When the data matches the State Table display in Figure 5-5, press the STORE key on the DAS keyboard.

10. Press the COMPARE ≠ key.

11. Verify that the test runs for at least 5 RESTARTS.

12. Press the STOP key.

STATE TABLE DISPLAY: `ACQUISITION`   COMPARE: START SEQ `510`
                                                           STOP SEQ `541`
TIME =   3.2 µS
SRCH =   `XX` `XX` `XX`

SEQ	A	B	C	Function Exercised
`510` T	F0	F0	F0	trigger; WR6
511	F2	F2	F2	
512	66	66	66	dual enable
513	23	23	23	
514	49	49	49	
515	A6	A6	A6	enable/disable
516	2E	2E	2E	timer on; enable, WR1
517	24	24	24	enable
518	AE	AE	AE	enable
519	EE	EE	EE	
520	66	66	66	dual enable
521	29	29	29	
522	D6	D6	D6	timer off; WR2
523	96	96	96	
524	2E	2E	2E	timer on
525	D1	D1	D1	repeat 5
526	D1	D1	D1	
527	D1	D1	D1	
528	D1	D1	D1	
529	D1	D1	D1	
530	D6	D6	D6	timer off
531	C5	C5	C5	timer on; WR3, occurrence 1
532	C5	C5	C5	timer on; WR3, occurrence 2
533	3A	3A	3A	
534	C5	C5	C5	timer on; WR3, occurrence 3
535	85	85	85	
536	64	64	64	dual enable, WR4
537	8E	8E	8E	WR5
538	AD	AD	AD	
539	26	26	26	enable/disable
540	AE	AE	AE	enable
541	0F	0F	0F	

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Figure 5-5. State Table display of data acquired using Functional Test 6.

(7) Stack Reset Function
TRIGGER Function (OR IF Field)

This test:

- Verifies the stack RESET function from U291-3 (91A24 schematic 74, 91AE24 schematic 85) to U558-2,6 (91A24 schematic 76, 91AE24 schematic 86) to U575-5,6 (91A24 schematic 76, 91AE24 schematic 86) to the stack pointer U571-1 (91A24 schematic 76, 91AE24 schematic 86).

- Verifies the trigger function of the OR IF field (the parallel start word recognizer).

To run this test:

1. Leave the Pattern Generator menu program as you set it up for Functional Test 6. Figure 5-6 shows this same pattern generator program with the callouts that identify the functions tested when you run Functional Test 7.

2. Go to the Channel Specification menu and change the radix of all groups to BIN (binary). If you are testing a 91AE24, you also need to group the channels to match your probe connections. For example, if you are testing 91AE24 pod A, group those channels with the 91A24 pod A channels.

NOTE

If you are testing a 91AE24, group the pods you are not testing toward the end of the Channel Specification menu. Doing so will make these channels show as the least significant bytes in the Trigger Specification menu, making it easy to change them to DON'T CARE values.

PATTERN GENERATOR: █PROGRAM█   INTERRUPT: CALL █████ ON █I█

CLOCK: █100nS█   █TTL█ + 1.40V   PAUSE ON: █1█ INHIBIT ON: █1█

Function Exercised	SEQ	LABEL	POD3DC HEX	POD3BA HEX	POD4CB HEX	INSTRUCTIONS	STROBES
	0	0	0000	0099	9999		██████
	1		0000	0066	6666		
	2		0000	0023	2323		
	3		0000	0049	4949		
	4		0000	00B6	B6B6		
	5		0000	00F6	F6F6		
	6		0000	0059	5959		
enable/disable	7		0000	00A6	A6A6 ○		
	8		0000	00E6	E6E6		
	9		0000	002F	2F2F		
	10		0000	00D9	D9D9	REPEAT 255	
enable, WR1	11		0000	002E	2E2E ○		
reset	12		0000	0024	2424 ○		
disable	13		0000	00B6	B6B6		
	14		0000	0051	5151	REPEAT 10	
enable	15		0000	00AE	AEAE ○		
	16		0000	00EE	EEEE ○		
	17		0000	0066	6666 ○		
	18		0000	0029	2929 ○		
	19		0000	00D6	D6D6 ○		
	20		0000	0096	9696 ○		
	21		0000	002E	2E2E ○		
	22		0000	00D1	D1D1 ○	REPEAT 5	
	23		0000	00D6	D6D6 ○		
WR3, occurrence 1	24		0000	00C5	C5C5 ○		
WR3, occurrence 2	25		0000	00C5	C5C5 ○		
	26		0000	003A	3A3A ○		
WR3, occurrence 3	27		0000	00C5	C5C5 ○		
	28		0000	0085	8585 ○		
WR4	29		0000	0064	6464 ○		
WR5	30		0000	008E	8E8E ○		
	31		0000	00AD	ADAD ○		
	32		0000	0052	5252 ○		
	33		0000	0012	1212 ○		
	34		0000	0049	4949 ○		
	35		0000	00B6	B6B6		
	36		0000	00F6	F6F6		
	37		0000	00D9	D9D9		
dual enable/disable	38		0000	0026	2626 ○		
	39		0000	0006	0606		
enable	40		0000	00AE	AEAE ○		
	41		0000	000F	0F0F ○		
WR6	42		0000	00F0	F0F0 ○		
	43		0000	00F2	F2F2 ○		
disable	44		0000	00B6	B6B6	GOTO 0	

4541-106

Figure 5-6. Pattern generator menu program for Functional Test 7. This program is the same as the program for Functional Test 6. The callouts in this illustration label which function that part of the program exercises when you are performing Test 7. A dot next to a program line indicates data you should acquire when you run Test 7. (See Figure 5-8 to see this data in the State Table display.)

3. Go to the Trigger Specification menu. If you are testing a 91A24, change the menu to match Figure 5-7. If you are testing a 91AE24, program the word recognizers for the 91AE24 pod being tested to match those of the corresponding 91A24 pod. For example, if you are testing 91AE24 pod A, match its word recognizer values to those of the 91A24 pod A. Use DON'T CARE values for all pods not under test.

NOTE

If you are looking at both 91A24 and 91AE24 values in the Trigger Specification menu in binary, only one group at a time will be displayed. To see the other two groups, press SHIFT SCROLL.

① 26, 2E, A6, AE ⑥ 64
② 52 ⑦ 8E
③ 26, 27, 2E, 2F ⑧ F0
④ 96, B6, D6, F6 ⑨ 24, 26, 64, 66
⑤ C5 ⑩ 26, 36, A6, B6

Figure 5-7. Trigger Specification menu setup for Functional Test 7. Lines marked with a dot are changes from the Trigger Specification menu setup for Test 6 (shown in Figure 5-4).

4. Press the START SYSTEM key.

5. Go to the Channel Specification menu and change the radix of all groups to hexadecimal.

6. Compare the time and data in the State Table menu display with Figure 5-8. If any of the acquired data is different from the data shown, use the callout on that line of the State Table display to identify the function tested by that part of the program. For example, if your data corresponding to sequence 521 in Figure 5-8 is other than AE AE AE, suspect the enable function. If you have acquired extra data that is not shown in the State Table display, look at the callouts in the pattern generator program shown in Figure 5-6 to determine which function is suspect.

```
STATE TABLE DISPLAY: ACQUISITION              COMPARE: START SEQ  510
                                                       STOP  SEQ  541
TIME =    1.1 µS
SRCH =    XX  XX  XX


  SEQ     A    B    C    Function Exercised

  509     AD   AD   AD
  510  T  52   52   52   OR trigger
  511     12   12   12
  512     49   49   49
  513     26   26   26   reset
  514     AE   AE   AE   enable
  515     0F   0F   0F
  516     F0   F0   F0   trigger 1; enable WR6
  517     F2   F2   F2
  518     A6   A6   A6   enable/disable
  519     2E   2E   2E   timer on; enable, WR1
  520     24   24   24   reset
  521     AE   AE   AE   enable
  522     EE   EE   EE
  523     66   66   66   reset
  524     29   29   29
  525     D6   D6   D6   timer off
  526     96   96   96
  527     2E   2E   2E   timer on
  528     D1   D1   D1   repeat 5
  529     D1   D1   D1
  530     D1   D1   D1
  531     D1   D1   D1
  532     D1   D1   D1
  533     D6   D6   D6   timer off
  534     C5   C5   C5   timer on; WR3, occurrence 1
  535     C5   C5   C5   timer on; WR3, occurrence 2
  536     3A   3A   3A
  537     C5   C5   C5   timer on; WR3, occurrence 3
  538     85   85   85
  539     64   64   64   WR4
  540     8E   8E   8E   WR5
  541     AD   AD   AD
                                            4541-108
```

Figure 5-8. State Table display of Functional Test 7. The callouts label the function exercised by that part of the test. If you acquire extra data not shown in this display, look at the pattern generator program shown in Figure 5-6 to determine which function is suspect.

7. Verify that the TIME= field shows 1.1 μS.

8. When the data matches the State Table display in Figure 5-8, press the STORE key.

9. Press the COMPARE ≠ key.

10. Verify that the test runs for at least 5 RESTARTS.

11. Press the STOP key.

(8) INC CNTR Function (with INT3)
Sequential Word Recognizer WHEN NOT Function
Sync Out Function

This test:

• Verifies the INCR CNTR (Increment Counter) function when used with INT 3. The signal path begins at U468-1,2 (91A24 schematic 76) where it continues to U491-11,8 (91A24 schematic 76) and finally ends at U495-11,10 (91A24 schematic 76).

• Verifies sequential word recognizer WHEN NOT function.

• Verifies the SYNC OUT circuit consisting of U161-9 (91A24 schematic 75), U268-9,8 (91A24 schematic 76), U265-12,11 (91A24 schematic 76), U471-3,6 (91A24 schematic 76), and finally U568-1,2,3 (91A24 schematic 76).

To run this test:

1. Load the Pattern Generator program shown in Figure 5-9.

2. Change the Pattern Generator Timing menu to match Figure 5-10.

```
PATTERN GENERATOR: PROGRAM                    INTERRUPT: CALL ████ ON ⊓

         CLOCK: ██ 100nS ██   █TTL█  + 1.40V   PAUSE ON: █1█  INHIBIT ON: █1█

              POD3DC POD3BA POD4CB
   SEQ  LABEL  █HEX█  █HEX█  █HEX█  INSTRUCTIONS  STROBES

    █0█  ████  █0000█ █0000█ █0000█              ████████
     1         0000   0800   0000
     2    0    0000   0700   0000                   12
     3         0000   0711   1111
     4         0000   0722   2222
     5         0000   0733   3333
     6         0000   0744   4444                    0
     7         0000   0755   5555
     8         0000   0066   6666                   12
     9         0000   0077   7777
    10         0000   0088   8888
    11         0000   0099   9999
    12         0000   00AA   AAAA                    0
    13         0000   00BB   BBBB
    14         0000   00CC   CCCC   GOTO    0
    15         0000   00DD   DDDD
    16         0000   00EE   EEEE              4541-109
```

Figure 5-9. Pattern Generator program for Test 8.

```
PATTERN GENERATOR: █TIMING█

START PAT GEN MODE: █RUN█

            POD   DELAY      WIDTH     SHAPE
  STROBE 5  3D  ██ 70nS ██  ██ 40nS ██  █⊓█

  STROBE 4  3C  ██ 70nS ██  ██ 40nS ██  █⊓█

  STROBE 3  3B  ██ 70nS ██  ██ 40nS ██  █⊓█

  STROBE 2  3A  ██ 270nS ██ ██ 80nS ██  █⊓█

  STROBE 1  4C  ██ 70nS ██  ██ 80nS ██  █⊓█

  STROBE 0  4B  ██ 70nS ██  ██ 80nS ██  █⊓█
                                      4541-110
```

Figure 5-10. Pattern Generator Timing menu for Functional Test 8.

3. Go to the Channel Specification menu and change the THRESHOLD field value to +2.50 V. This setting reduces effects from probe noise.

4. Change the Trigger Specification menu to match Figure 5-11.

```
 TRIGGER  SPECIFICATION                    MODE:     91A24 ONLY

                                           TRIGGER POSITION:  CENTER

                             A   B   C
            BEGIN STORE IF    XX  XX  XX
            THEN

     1:       WHEN     XX  XX  XX  OCCURS    1   SYNC OUT
     2:THEN   WHEN NOT 11  11  11  OCCURS    1   THEN
     3:       WHEN     3X  XX  XX  OCCURS    1   INCR  CNTR
     4:
     5:
     6:
     7:
     8:
     9:
    10:
    11:
    12:
 OR
        RESET     IF   CC  CC  CC

 END STORE    OFF                                          4541-111
```
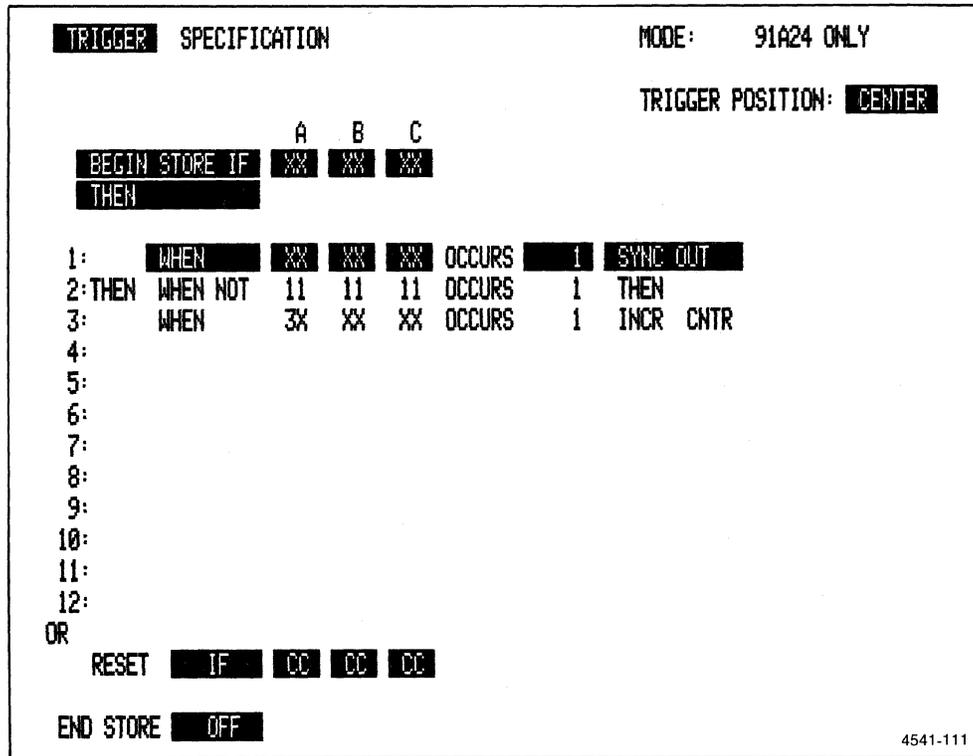
Figure 5-11. Trigger Specification menu setup for Functional Test 8.

5. Enter the Clock Specification sub-menu and verify that the internal clock is set to 100 ns.

6. Press the START SYSTEM key.

7. Verify that the DAS display shows a changing count value which eventually becomes greater than 65000. This information will be displayed on the line reading WAITING FOR MANUAL STOP   CNTR= XXXXX.

8. (91A24 only. Optional.) Connect the SYNC OUT cable to the 91A24 module, and to an oscilloscope. Verify that the pulse coming from the cable is approximately 200 ns wide, with a period of 1.3 μs.

9. Press STOP and verify that the data acquired repeats as shown in Figure 5-12. Note that the sequence numbers on your display will be different because of the lack of a trigger word.

```
STATE TABLE DISPLAY: ACQUISITION          COMPARE: START SEQ   0
                                                   STOP  SEQ  511
CNTR =    1,242,694
SRCH =    XX  XX  XX


    SEQ   A    B    C

    502   33   33   33
    503   44   44   44
    504   55   55   55
    505   66   66   66
    506   77   77   77
    507   88   88   88
    508   99   99   99
    509   AA   AA   AA
    510   BB   BB   BB
    511   CC   CC   CC
    512   00   00   00
    513   11   11   11
    514   22   22   22
    515   33   33   33
    516   44   44   44
    517   55   55   55                            4541-112
```

Figure 5-12. State Table display of Functional Test 8.

CLOCK AND CLOCK QUALIFIER TESTS

The following tests check the rising and falling edges of the clocks and clock qualifiers.

NOTE

Since the trigger word is set to DON'T CAREs (XXXXXX), the sequence numbers for particular lines of data displayed in the State Table may vary.

(9) Clock Test 1: Rising Edge

This test:

• Verifies all rising-edge external clock flip-flops listed below. All of these ICs are found on 91A24 schematic 78.

U735	U738	U741
U745	U751	U948

To run this test:

1. Enter the Trigger Specification menu and change:

   RESET field to OFF
   X3 to XX (in level 3 of the sequential word recognizer)
   INCR CNTR field to TRIGGER (in the last line of the sequential word recognizer)

2. Enter the Clock Specification sub-menu and change 91A24 CLOCK from INTERNAL to EXTERNAL.

3. Change the 91A24 clock setup as shown in Figure 5-13.

```
┌──────────────────────────────────────────────────────────────┐
│  CLOCK  SPECIFICATION                                          │
│                                            POD1A POD1B POD1C   │
│                                 QUALIFIERS:  QA    QB    QC    │
│   91A24  CLOCK:  EXTERNAL          CLOCKS: CLKA  CLKB  CLKC    │
│                                                                │
│        DATA FOR:  MEM 1A/1B     MEM 2A/2B                      │
│   ACQUIRED FROM:  POD 1A/1B     POD 2A/2B                      │
│                                                                │
│   MASTER CLOCK:  PODA                                          │
│                                                                │
│   PODA CLOCKS =   CLKAʃ      +  CLKBʃ       + CLKCʃ            │
│                                                                │
│   PODB CLOCKS =   CLKAʃ      +  CLKBʃ       + CLKCʃ            │
│                                                                │
│   PODC CLOCKS =   CLKAʃ      +  CLKBʃ       + CLKCʃ            │
│                                                         4541-113│
└──────────────────────────────────────────────────────────────┘
```

Figure 5-13. Clock Specification sub-menu for Functional Test 9.

4. Press START PAT GEN followed by START ACQ. Verify that the test triggers, and that the display matches Figure 5-14.

```
STATE TABLE DISPLAY: ACQUISITION          COMPARE: START SEQ    0
                                                   STOP  SEQ   511

TRIG =    00   00   00
SRCH =    XX   XX   XX


     SEQ    A    B    C

     508    88   88   88
     509    AA   AA   AA
     510 T  00   00   00
     511    22   22   22
     512    44   44   44
     513    66   66   66
     514    88   88   88
     515    AA   AA   AA
     516    00   00   00
     517    22   22   22
     518    44   44   44
     519    66   66   66
     520    88   88   88
     521    AA   AA   AA
     522    00   00   00
     523    22   22   22                                4541-114
```
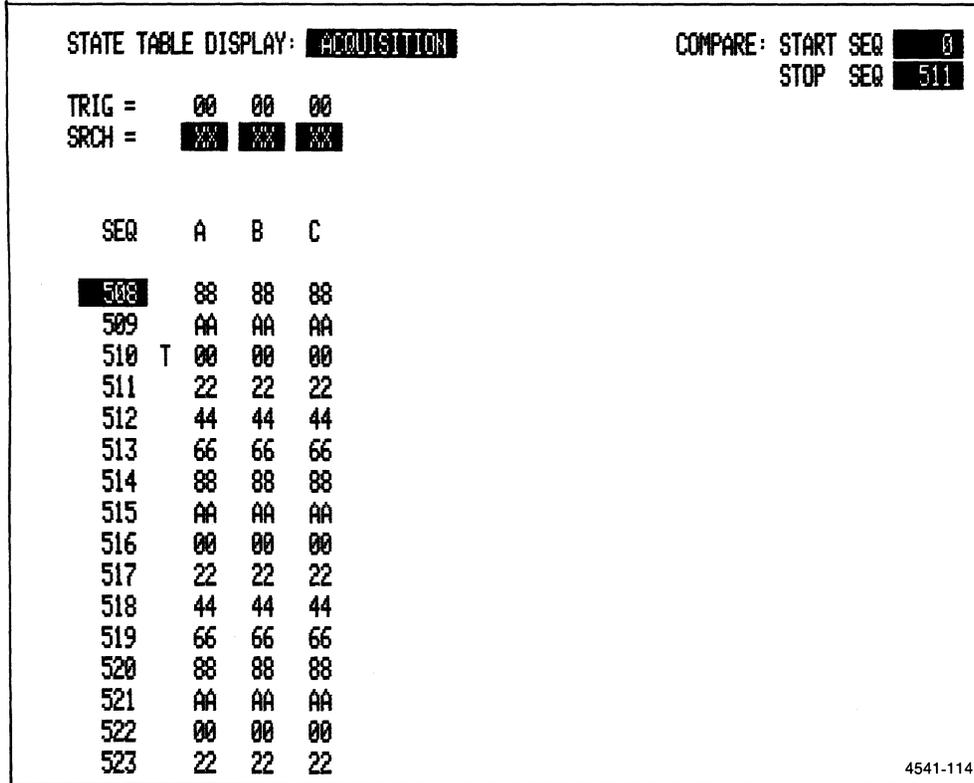
Figure 5-14. State Table display of Functional Test 9.

(10) Clock Test 2: Falling Edge

This test:

• Verifies all falling edge external clock flip-flops listed below. These ICs are all found on 91A24 schematic 78.

U835	U838	U841
U845	U851	U951

To run this test:

1. Go to the Clock Specification sub-menu.

2. Change the 91A24 clock setup to match Figure 5-15.

```
┌───────────────────────────────────────────────────────────────────────┐
│  ▐▌CLOCK▐▌ SPECIFICATION                                                 │
│                                                      POD1A POD1B POD1C   │
│                                           QUALIFIERS:  0A    0B    0C    │
│  91A24  CLOCK: ▐▌EXTERNAL▐▌                    CLOCKS: CLKA  CLKB  CLKC   │
│                                                                         │
│         DATA FOR: MEM 1A/1B       MEM 2A/2B                             │
│   ACQUIRED FROM: ▐▌POD 1A/1B▐▌   ▐▌POD 2A/2B▐▌                          │
│                                                                         │
│   MASTER CLOCK: ▐▌PODA▐▌                                                │
│                                                                         │
│   PODA CLOCKS = ▐▌CLKA1▐▌    + ▐▌CLKB1▐▌    + ▐▌CLKC1▐▌    ▐▌  ▐▌        │
│                                                                         │
│   PODB CLOCKS =   CLKA1      +   CLKB1      +   CLKC1                    │
│                                                                         │
│   PODC CLOCKS =   CLKA1      +   CLKB1      +   CLKC1          4541-115  │
└───────────────────────────────────────────────────────────────────────┘
```
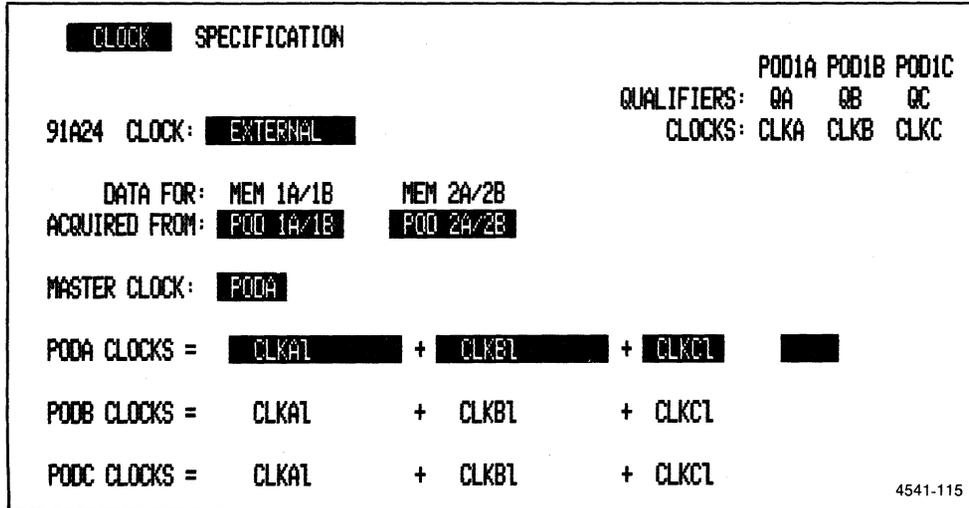
Figure 5-15. Clock Specification submenu setup for Functional Test 10.

2. Press the START PAT GEN key followed by the START ACQ key.

3. Verify that the test triggers and displays the repeating pattern in Figure 5-16.

```
┌───────────────────────────────────────────────────────────────────────┐
│  STATE TABLE DISPLAY: ▐▌ACQUISITION▐▌        COMPARE: START SEQ ▐▌  0 ▐▌ │
│                                                       STOP  SEQ ▐▌511▐▌ │
│  TRIG =    99  99  99                                                   │
│  SRCH =   ▐▌XX▐▌ ▐▌XX▐▌ ▐▌XX▐▌                                          │
│                                                                         │
│     SEQ     A    B    C                                                 │
│                                                                         │
│   ▐▌508▐▌   55   55   55                                                │
│     509     77   77   77                                                │
│     510  T  99   99   99                                                │
│     511     BB   BB   BB                                                │
│     512     11   11   11                                                │
│     513     33   33   33                                                │
│     514     55   55   55                                                │
│     515     77   77   77                                                │
│     516     99   99   99                                                │
│     517     BB   BB   BB                                                │
│     518     11   11   11                                                │
│     519     33   33   33                                                │
│     520     55   55   55                                                │
│     521     77   77   77                                                │
│     522     99   99   99                                                │
│     523     BB   BB   BB                                      4541-116  │
└───────────────────────────────────────────────────────────────────────┘
```
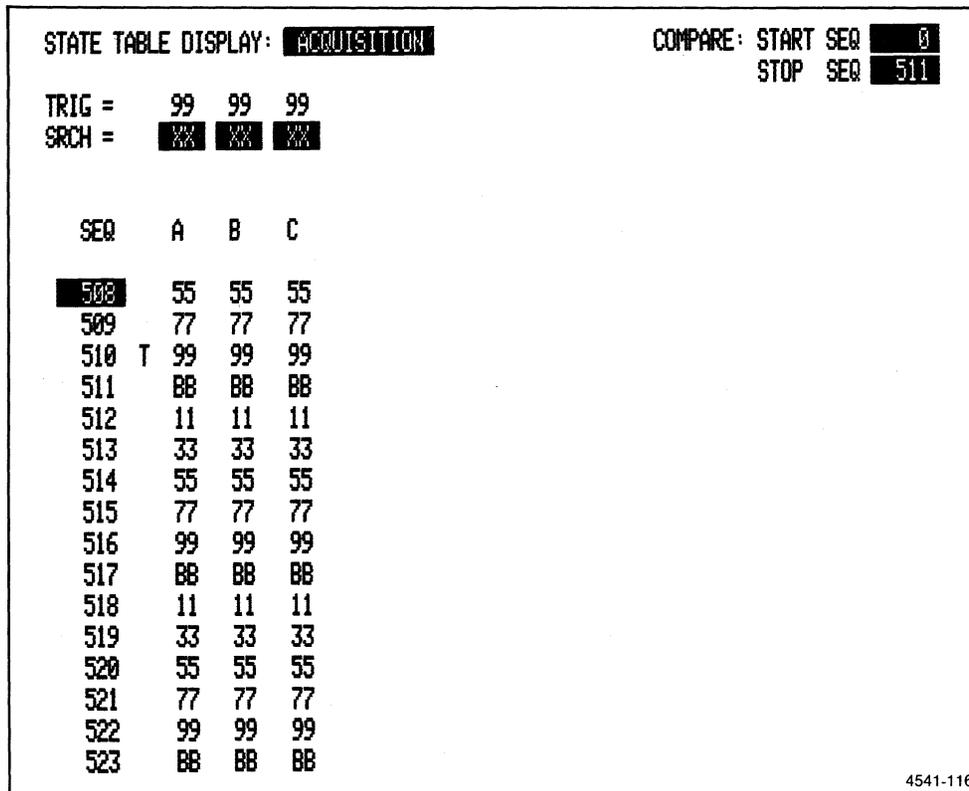
Figure 5-16. State Table display of Functional Test 10.

(11) Active-High Clock Qualifier Test

This test:

*   Verifies that the active-high (positive) qualifiers are working.

To run this test:

1. Go to the Clock Specification sub-menu.

2. Change the 91A24 clock status to match Figure 5-17.

```
CLOCK  SPECIFICATION
                                          POD1A POD1B POD1C
                             QUALIFIERS:   QA    QB    QC
91A24  CLOCK: EXTERNAL          CLOCKS:  CLKA  CLKB  CLKC

    DATA FOR: MEM 1A/1B      MEM 2A/2B
ACQUIRED FROM: POD 1A/1B      POD 2A/2B

MASTER CLOCK: PODA

PODA CLOCKS = ( (CLKAↃ ꭕ QA) + (CLKBↃ ꭕ QB) + CLKCↃ ) ꭕ QC

PODB CLOCKS = ( (CLKAↃ ꭕ QA) + (CLKBↃ ꭕ QB) + CLKCↃ ) ꭕ QC

PODC CLOCKS = ( (CLKAↃ ꭕ QA) + (CLKBↃ ꭕ QB) + CLKCↃ ) ꭕ QC
                                                        4541-117
```

Figure 5-17. Clock Specification sub-menu setup for Functional Test 11.

3. Press the START PAT GEN key followed by the START ACQ key.

4. Verify that the test triggers and displays the repeating pattern in Figure 5-18.

```
STATE TABLE DISPLAY: ▓ACQUISITION▓          COMPARE: START SEQ ▓   0
                                                     STOP  SEQ ▓ 511

TRIG =    44   44   44
SRCH =   ▓XX▓ ▓XX▓ ▓XX▓


  SEQ     A    B    C

 ▓508▓    00   00   00
  509     22   22   22
  510  T  44   44   44
  511     00   00   00
  512     22   22   22
  513     44   44   44
  514     00   00   00
  515     22   22   22
  516     44   44   44
  517     00   00   00
  518     22   22   22
  519     44   44   44
  520     00   00   00
  521     22   22   22
  522     44   44   44
  523     00   00   00
                                                              4541-118
```

Figure 5-18. State Table display of Functional Test 11.

(12) Active-Low Clock Qualifier Test

This test:

• Verifies all active-low (negative) qualifiers.

To run this test:

1. Go to the Clock Specification sub-menu.

2. Change the 91A24 clock status to match Figure 5-19.

```
┌────────────────────────────────────────────────────────────────┐
│  ███CLOCK███  SPECIFICATION                                      │
│                                          POD1A POD1B POD1C       │
│                                QUALIFIERS:  QA    QB    QC        │
│  91A24  CLOCK: ███EXTERNAL███      CLOCKS: CLKA  CLKB  CLKC       │
│                                                                  │
│        DATA FOR:  MEM 1A/1B      MEM 2A/2B                        │
│  ACQUIRED FROM: ███POD 1A/1B███ ███POD 2A/2B███                  │
│                                                                  │
│  MASTER CLOCK: ███PODA███                                        │
│                                                                  │
│  PODA CLOCKS = ( ███(CLKAↃ ✱ /QA)███ + ███(CLKBↃ ✱ /QB)███ + ███CLKCↃ███ ) ✱ ███/QC███ │
│                                                                  │
│  PODB CLOCKS = (  (CLKAↃ ✱ /QA)  +  (CLKBↃ ✱ /QB)  +  CLKCↃ  ) ✱  /QC │
│                                                                  │
│  PODC CLOCKS = (  (CLKAↃ ✱ /QA)  +  (CLKBↃ ✱ /QB)  +  CLKCↃ  ) ✱  /QC │
│                                                            4541-301│
└────────────────────────────────────────────────────────────────┘
```
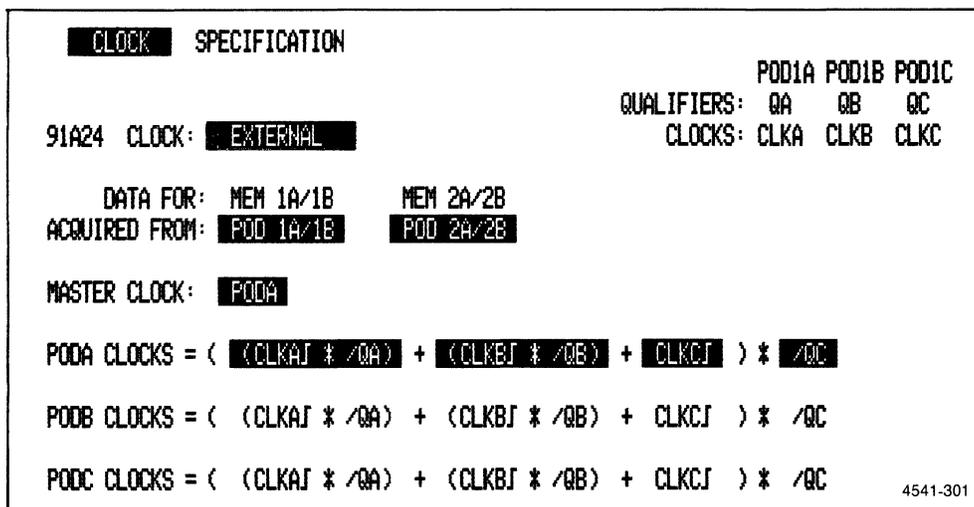
Figure 5-19. Clock Specification sub-menu setup for Functional Test 12.

3. Press the START PAT GEN key followed by the START ACQ key.

4. Verify that the test triggers and displays the repeating pattern in Figure 5-20.

```
┌────────────────────────────────────────────────────────────────┐
│  STATE TABLE DISPLAY: ███ACQUISITION███    COMPARE: START SEQ ███0███ │
│                                                     STOP  SEQ ███511███│
│  TRIG =    66  66  66                                             │
│  SRCH =   ███XX███ ███XX███ ███XX███                             │
│                                                                  │
│                                                                  │
│     SEQ    A   B   C                                             │
│                                                                  │
│  ███508███ 88  88  88                                            │
│     509    AA  AA  AA                                            │
│     510  T 66  66  66                                            │
│     511    88  88  88                                            │
│     512    AA  AA  AA                                            │
│     513    66  66  66                                            │
│     514    88  88  88                                            │
│     515    AA  AA  AA                                            │
│     516    66  66  66                                            │
│     517    88  88  88                                            │
│     518    AA  AA  AA                                            │
│     519    66  66  66                                            │
│     520    88  88  88                                            │
│     521    AA  AA  AA                                            │
│     522    66  66  66                                            │
│     523    88  88  88                                            │
│                                                            4541-302│
└────────────────────────────────────────────────────────────────┘
```
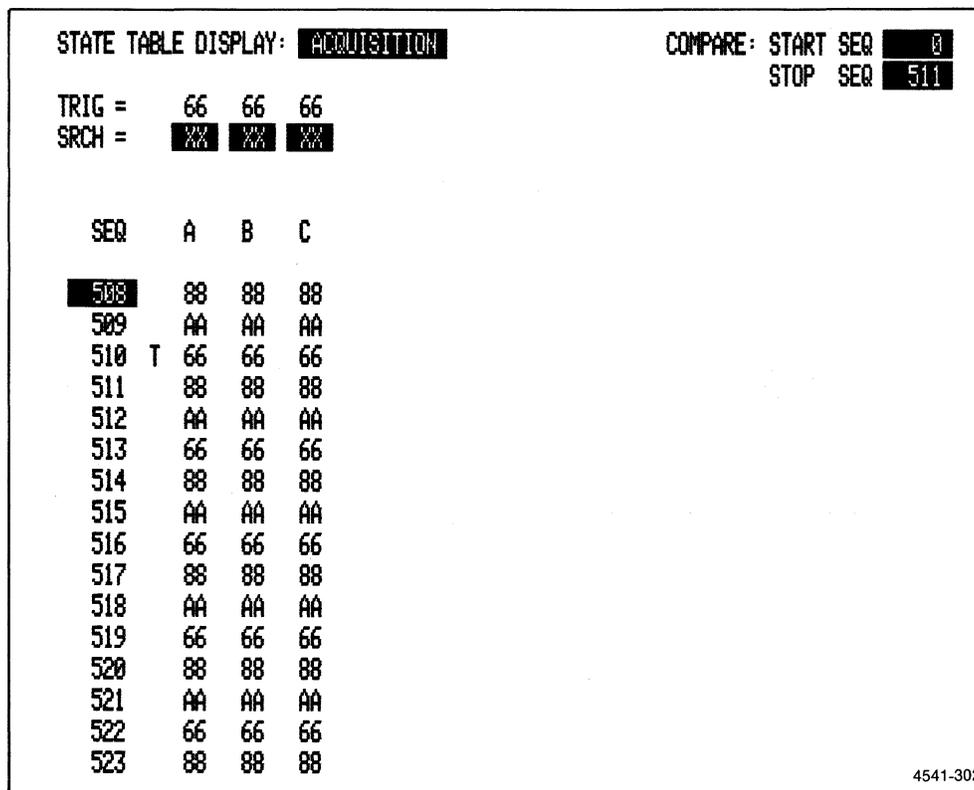
Figure 5-20. State Table display for Functional Test 12.

DEMUX MODE TEST

(13) DEMUX MODE Test

> *NOTE*
>
> *Since the trigger word is set to DON'T CAREs (XX XX XX), the number of se-
> quences displayed in the State Table may vary.*

This test:

- Verifies internal clock circuit ICs U731B, U748A, U921A, and U535A,B, and U538A. These ICs
  are all found on 91A24 schematic 78.
- Verifies the input multiplexing circuit consisting of U758 (91A24 schematic 68, 91AE24
  schematic 79), U218D (91A24 schematic 72, 91AE24 schematic 83), and U121 (91A24
  schematic 72, 91AE24 schematic 83).

To run this test:

1. Remove pod B probe from the 91A24 module under test.

2. Press the START PAT GEN key followed by the START ACQ key.

3. Verify that pod B acquires all zeros.

4. Change the ACQUIRED FROM field (in the Clock Specification sub-menu) from POD 1A/1B to
   POD 1A.

5. Press the START PAT GEN key followed by the START ACQ key.

6. Verify that the test triggers and the data matches Figure 5-21.

ARMS MODE TEST

(14) 91A24 ARMS 91A08

This test verifies that the 91A24 module can successfully arm a 91A08 module. Verifying the arming
function for the 91A08 also verifies it for 91A04-type modules.

1. Connect the probes and modules as shown in Figure 5-22. This setup adds the 91A08 to the
   setup given at the beginning of the Functional Check section (shown in Figure 5-3). The
   connections between the 91A24, the 91P16, the 91P32, and their probes are unchanged.

```
STATE TABLE DISPLAY: ACQUISITION          COMPARE: START SEQ   0
  POD 3B                                            STOP  SEQ  511
TRIG =      88   88   88
SRCH =      XX   XX   XX


    SEQ     A    B    C

    508     88   88   88
    509     AA   AA   AA
    510  T  88   88   88
    511     AA   AA   AA
    512     88   88   88
    513     AA   AA   AA
    514     88   88   88
    515     AA   AA   AA
    516     88   88   88
    517     AA   AA   AA
    518     88   88   88
    519     AA   AA   AA
    520     88   88   88
    521     AA   AA   AA
    522     88   88   88
    523     AA   AA   AA
                                                          4541-303
```

Figure 5-21. State Table display of Functional Test 13.

DAS MAINFRAME SLOTS
(back view)

P6460 TO P6455 DATA LEAD CONNECTIONS

P6460	white	black	brown	red	orange	yellow	green	blue	violet
P6455	white	black	brown	red	orange	yellow	green	blue	violet

4541-304
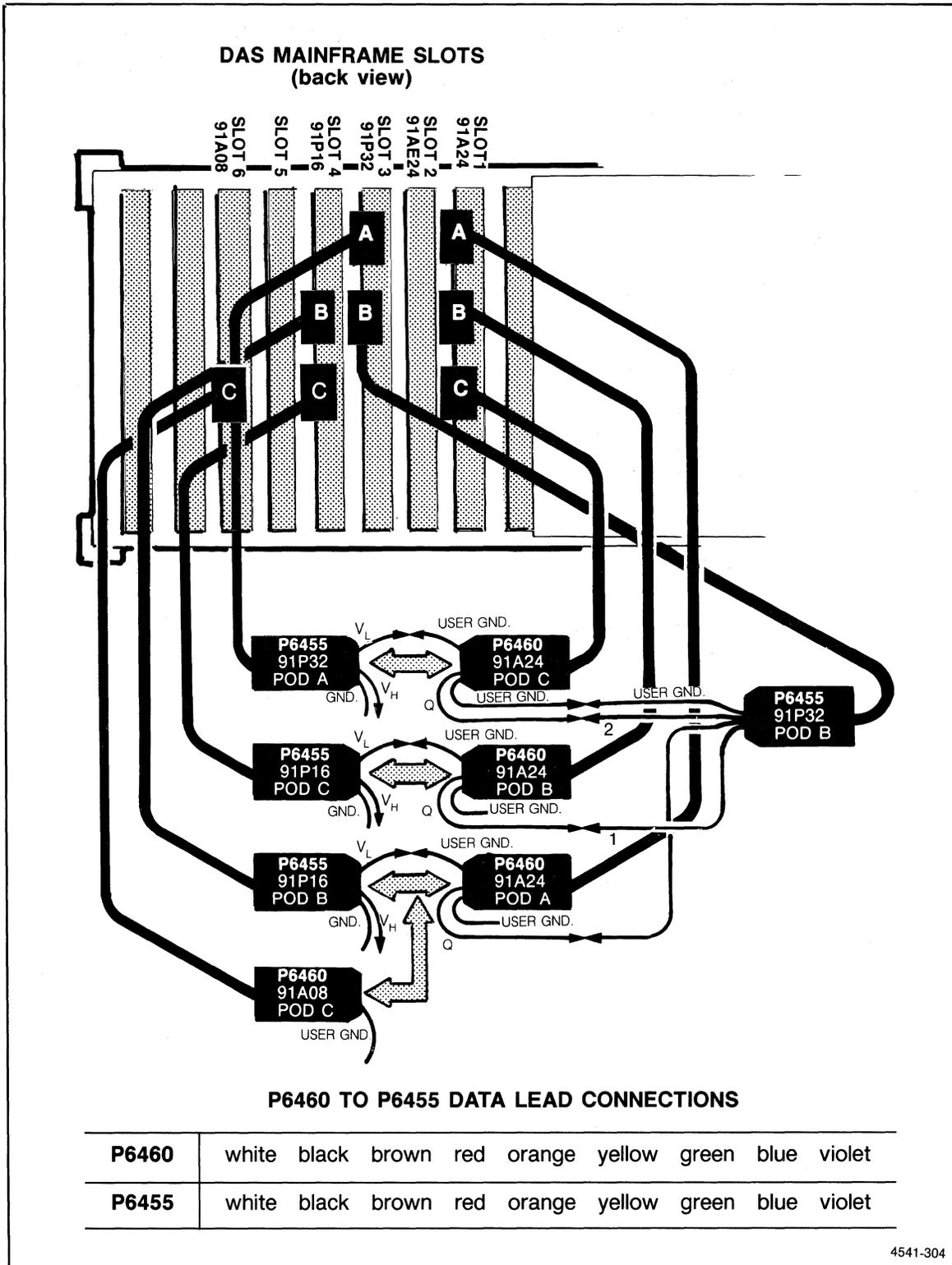
Figure 5-22. Test equipment setup for Functional Test 14.

2. Enter the Trigger Specification menu. Select 91A24 ARMS 91A08 mode. Change the menu to match Figure 5-23.
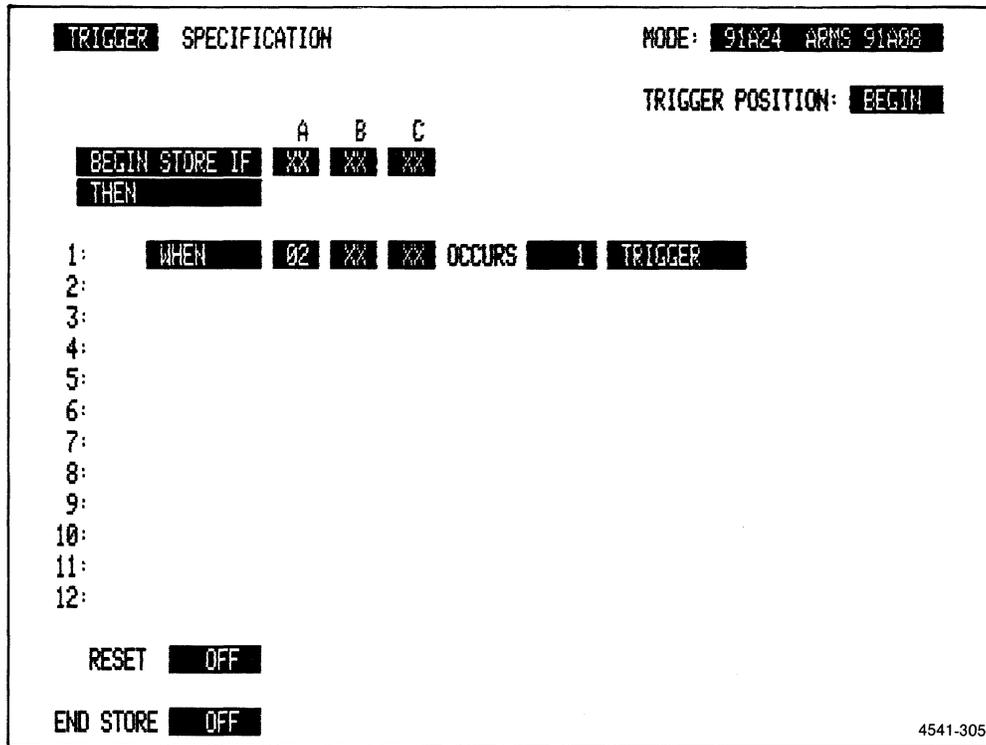
Figure 5-23. Trigger Specification menu setup for Functional Test 14.

3. Enter the Clock Specification sub-menu. Change the value in the 91A24 CLOCK field to 2 μS.

4. Enter the Pattern Generator menu. Change the field values to match those shown in Figure 5-24, and enter the pattern generator program as shown.

```
PATTERN GENERATOR:  PROGRAM                        INTERRUPT:  CALL ████  ON █

          CLOCK:  ████ 2µS ████   TTL  + 1.40V   PAUSE ON: █  INHIBIT ON: █

                  POD3DC POD3BA POD4CB
       SEQ  LABEL  HEX    HEX    HEX   INSTRUCTIONS   STROBES

        0          0000   0000   0000   GOTO    1   ████
        1    1     0000   0001   0101
        2          0000   0002   0202
        3          0000   0004   0404
        4          0000   0008   0808
        5          0000   0010   1010
        6          0000   0020   2020
        7          0000   0040   4040
        8          0000   0080   8080
        9          0000   00FF   FFFF
       10          0000   00FE   FEFE
       11          0000   00FD   FDFD
       12          0000   00FB   FBFB
       13          0000   00F7   F7F7
       14          0000   00EF   EFEF
       15          0000   00DF   DFDF
       16          0000   00BF   BFBF
       17          0000   007F   7F7F
       18          0000   0000   0000
       19          0000   00AA   AAAA
       20          0000   0055   5555
       21          0000   0000   0000
       22          0000   00FF   FFFF   GOTO    1        4541-306
```

Figure 5-24. Pattern Generator menu setup for Functional Test 14.

5. Press the START SYSTEM key. Verify that the data matches the State Table display shown in Figure 5-25. It may be necessary to make multiple acquisitions before you will obtain matching data. When the data matches, press the STORE key.

```
STATE TABLE DISPLAY: ACQUISITION        COMPARE: START SEQ  17
                                                 STOP  SEQ  30

TRIG =   02   02   02   FF
SRCH =   XX   XX   XX   XX


 SEQ     A    B    C    D

  15                     02
  16  ▌ 02   02   02    02
  17                     04
  18    04   04   04    04
  19                     08
  20    08   08   08    08
  21                     10
  22    10   10   10    10
  23                     20
  24    20   20   20    20
  25                     40
  26    40   40   40    40
  27                     80
  28    80   80   80    80
  29  ▌                 FF
  30    FF   FF   FF    FF
```

4541-307

Figure 5-25. State Table display for Functional Test 15.

6. Press the COMPARE = key. When the acquisition memory equals the reference memory, the DAS exits the COMPARE = function, and the test passes. If the test fails, check the implementation of both 91A08 and 91A24 module hardware modifications.

To add the 91A08 to the original functional check setup (Figure 5-3), follow these steps:

a. Install a 91A08 module in slot 6.

b. Connect a P6452 Data Acquisition Probe to the 91A08 pod A.

c. Connect this P6452 to the P6455 from pod B of the 91P16.

Since the P6452 probe is already connected to the P6460 from pod A of the 91A24, you will need to connect the new probe to the exposed portions of the square-pin connector joining the P6455 and the P6460. To do so, put grabber tips on the P6452 leads, then connect the leads color-to-color (e.g., white-to-white, etc.).

ADJUSTMENT PROCEDURES

INTRODUCTION

This section contains procedures for adjusting the 91A24 and 91AE24 Data Acquisition Modules so that they meet or exceed performance specifications. All three of the adjustments can be used on either module. If the modules cannot be made to meet specifications by using these procedures, repair is necessary.

NOTE

Before adjusting any module, verify that the +12 V supply on the Main Power Supply board meets specifications. Directions for this check are given in the Verification and Adjustment Procedures *section of the* DAS Service Manual. *Having the +12 V supply out of adjustment can cause intermittent failures.*

The adjustments covered in this section include the power-up tests, the DAC adjustment, and the write-enable adjustment.

EQUIPMENT SETUP

The adjustments require the test equipment listed in Table 5-6.

Table 5-6
EQUIPMENT NEEDED FOR THE ADJUSTMENT PROCEDURES

Equipment	Specifications	Equivalent Tektronix Equipment
DAS Mainframe	No substitute allowed	
91A24 Data Acquisition Module	No substitute allowed	
91AE24 Data Acquisition Module (Optional)	No substitute allowed	
DAS 9100 Series Service Maintenance Kit (for extender board)	No substitute allowed	Tektronix P/N 067-0980-00
91A24 Interconnect Cable Assembly, 28 cm (11 in.) (7 required)	No substitute allowed	Tektronix P/N 175-8166-00
Oscilloscope	Dual trace, 100 MHz	465
Oscilloscope probe	X10, 100 MHz	P6106
Digital Multimeter (DMM)	0.05% dc V accuracy	DM 501A (with TM 500 mainframe)

ADJUSTMENTS

Power-up Tests

The power-up tests:

- Verify that all power supplies are operating within limits.
- Verify +3 volt supply parts U904 (91A24 schematic 78 and 91AE24 schematic 87) and Q901 (91A24 schematic 78, 91AE24 schematic 87).
- Verify Q951 (91A24 schematic 77, 91AE24 schematic 87) of the +4.5 volt supply.
- Verify DAC potentiometer R103 (91A24 schematic 71, 91AE24 schematic 82).
- Verify that Q902 (91A24 schematic 72, 91AE24 schematic 83) and U808B (91A24 schematic 72, 91AE24 schematic 83) are operating properly for Vbb.

1. Install the 91A24 on an extender board. If you are testing a 91AE24, put it on an extender board as well.

2. Check that all power supplies are within the tolerances indicated in Table 5-7. There are useful ground test points near the following ICs: above U718, U441, and U591; and under U261.

Table 5-7
POWER SUPPLY VOLTAGE CHECK

Voltage	Measured at	Limits
+ 3	top of C901 (+)	2.80 — 3.20
+ 4.5	U938, pin 20	4.30 — 4.70
+ 5	any IC Vcc	4.85 — 5.15
+ 6	R526-1	5.82 — 6.18
+12	R103, pin 3	11.82 — 12.82
−12	R103, pin 1	−10.80 — 13.20
− 5	U904, pin 4	−4.85 — 5.15
Vbb	Q902 emitter	3.7

DAC Adjustment

(91A24 Diagnostic Function 6)
(91AE24 Diagnostic Function 4)

The DAC adjustment test verifies proper operation of the DAC IC U918, op amps U808, U711, and their associated components (91A24 schematic 71, 91AE24 schematic 82).

1. Enter the Diagnostics menu by powering-down the DAS, then powering-up again while holding down any key.

   Select SINGLE mode and test function 6 in the DAS Diagnostics menu.

2. Press START SYSTEM.

3. Verify that the DAC test menu selection is set to 0.00 volts.

4. Connect the DMM black lead to ground and the positive lead to TP910 (91A24 schematic 71, 91AE24 schematic 82).

5. Adjust R103 (91A24 schematic 71, 91AE24 schematic 82) for a DMM reading of 0.00 volts.

6. Change the DAC test menu selection to +6.40 volts.

7. Adjust R110 (91A24 schematic 71, 91AE24 schematic 82) until the DMM reads +6.40 volts.

8. Move the DMM positive lead to test points 707, 711, and 808, and verify that the DMM reading is −6.40 volts (±50 mV).

9. Change the DAC menu selection to -6.35 V and verify that the measurements in step 8 are − 6.35 V (±50 mV).

10. Connect the oscilloscope probe to TP910 and ground. Set the oscilloscope to:

> TIME BASE — 10 ms/div.
>
> CH. 1 — 2 V/div.
>
> TRIGGER — AUTO

Press the SELECT key until the menu displays ramping.

11. Verify a linear ramp on the scope display. This verifies that all DAC input values can be programmed.

12. Press the STOP key.

13. Remove all DMM and scope probes.

Write-Enable Adjustment

The write-enable test verifies that 'MASTER CLOCK III' gets through U468-11,10 to the pulse-shaper circuit made up of U468-13,12, Q465, C468, and U578-1,2,3. The pulse must also pass through U475-4,5,6 to reach the storage RAM-select pin 8 of U141, U145, U241, U245, U441, and U445.

> *NOTE*
>
> *All parts specified in this write-enable adjustment can be found on 91A24 schematic 73, 91AE24 schematic 84.*

1. Remove all probes from the 91A24 module.

2. Press the Trigger Specification menu key.

3. In the 91A24 Trigger Specification menu, set the first level of the sequential word recognizer to FX XX XX. Press the START SYS key.

4. Verify that the display shows WAITING FOR 91A24 LEVEL: 1.

5. Connect a scope probe to TP465 and ground.

6. Adjust C468 for a 45 ns wide negative-going pulse at the 1.4 volt level.

7. Press the STOP key and verify that acquired data is all zeros.

8. Remove the scope probe.

PERFORMANCE CHECK

These procedures check the performance specifications for a 91A24 or 91AE24 module. You will need to run these tests once for each 91A24 or 91AE24 module you have installed. All tests in this section apply to both 91A24 and 91AE24 modules, although the setups differ slightly.

Completing all the 91A24/91AE24 performance check procedures verifies that the 91A24/91AE24 system can:

- acquire synchronous data at speeds up to 10 MHz (20 MHz in demultiplexing mode), and
- consistently store data with 25 ns setup and 0 ns hold times with TTL-level data.

You need the following equipment to complete this performance check procedure:

- DAS mainframe with:
    91A24 in slot 1
    (optional) 91AE24 in slot 2
    four P6460 Probes with leads and grabber tips (three probes if you are only testing a
        91A24 and no 91AE24s)
- TM 504 Mainframe with:
    one digital multimeter
    one 250 MHz pulse generator
    one 50 MHz pulse generator
    one Set-Up and Hold Time Test Fixture

NOTE
No more than four TM 504 mainframe slots are required for any single test.

- Dual-trace 100 MHz oscilloscope and probes
- Connectors:
    three 10-inch BNC cables
    three BNC T fittings
    two probe-to-BNC adapters
    three 10-wide square pin connectors
    (optional) one 10-wide comb and harmonica connector lead set per probe

PERFORMANCE CHECK SETUP PROCEDURE

Figures 5-26 and 5-27 show the basic equipment setup you need to begin the performance check. Detailed connection instructions follow.

Equipment Setup

1. Connect the 50 MHz pulse generator to the Setup and Hold Time Test Fixture as follows:

    a. Attach a BNC T connector to the TRIG GATE IN connector of the 50 MHz pulse generator.

    b. Connect one end of a 10 inch piece of coax cable to one arm of the BNC T connector on the pulse generator, and the other end to the CLOCK IN connector of the test fixture.

2. Connect the 250 MHz pulse generator to the 50 MHz pulse generator as follows:

   a. Connect a second BNC T adapter to one arm of the first BNC T (connector 1 in Figure 5-26).

   b. Connect a probe tip adapter to one arm.

   c. Connect one end of a 10 inch piece of coax to the remaining free arm of the second BNC T, and the other end of the coax to the OUTPUT connector of the 250 MHz pulse generator.

   b. Connect the base of the second BNC T adapter to the free arm of the first BNC T adapter (on the 50 MHz pulse generator).

3. Connect a third BNC T adapter to the OUTPUT connector on the 50 MHz pulse generator. Attach one end of a length of coax to one arm of the BNC and the other end to the EXT DELAY connector of the test fixture. Attach a probe tip adapter to the free arm of the BNC T adapter.

4. Attach the oscilloscope probe from channel 1 to the probe tip adapter on the doubled BNC connector (connector 2 in Figure 5-26).

5. Attach the oscilloscope probe from channel 2 to the probe tip adapter on the single BNC connector (connector 3 in Figure 5-26).
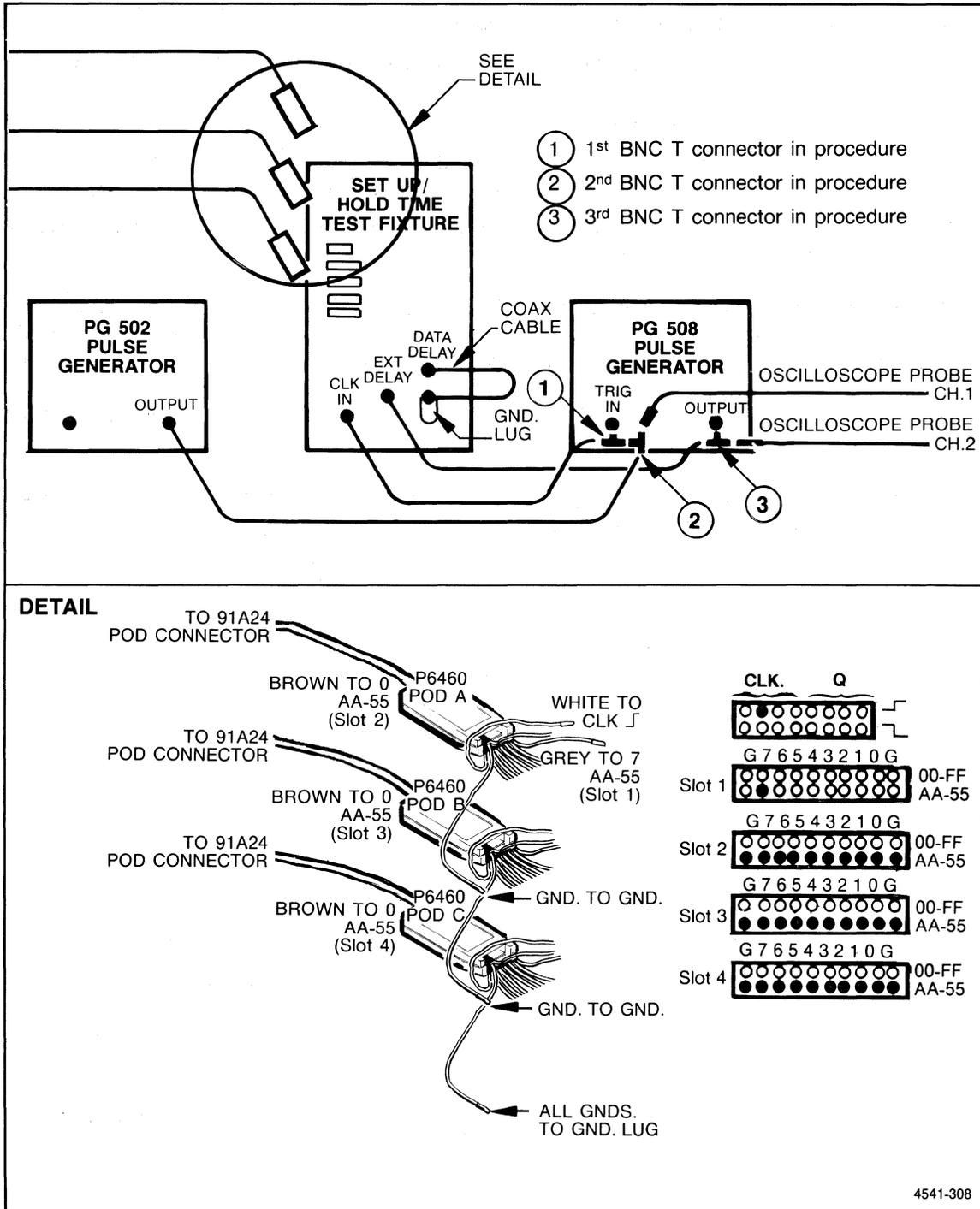
Figure 5-26. 91A24 performance check test equipment connections. The three BNC T connectors are numbered to help you distinguish between them in the detailed connection instructions given under *Equipment Setup.*

SEE DETAIL

(1) 1st BNC T connector in procedure
(2) 2nd BNC T connector in procedure
(3) 3rd BNC T connector in procedure

SET UP/
HOLD TIME
TEST FIXTURE

PG 502
PULSE
GENERATOR

OUTPUT

COAX CABLE

DATA DELAY

EXT DELAY

CLK IN

GND. LUG

PG 508
PULSE
GENERATOR

TRIG IN

OUTPUT

(1)

(2) (3)

DETAIL

TO 91A24
POD CONNECTOR

TO 91A24
POD CONNECTOR

P6460
POD X

BROWN TO 0
AA-55
(Slot 2)

P6460
POD A

TO 91A24
POD CONNECTOR

GND.

BROWN TO 0
AA-55
(Slot 3)

P6460
POD B

TO 91A24
POD CONNECTOR

GND. TO GND.

BROWN TO 0
AA-55
(Slot 4)

P6460
POD C

GND. TO GND.

GND. TO GND.

ALL GNDS.
TO GND. LUG

WHITE
TO CLK

CLK.   Q

G 7 6 5 4 3 2 1 0 G

Slot 1   00-FF
AA-55

G 7 6 5 4 3 2 1 0 G

Slot 2   00-FF
AA-55

G 7 6 5 4 3 2 1 0 G

Slot 3   00-FF
AA-55

G 7 6 5 4 3 2 1 0 G

Slot 4   00-FF
AA-55

4541-309

Figure 5-27. 91AE24 performance check test equipment connections. The three BNC T connectors are numbered to help you distinguish between them in the detailed connection instructions given under *Equipment Setup.*

Waveform Adjustments

1. Set up the 250 MHz pulse generator to display the waveform shown in Figure 5-28. This will be displayed on channel 1 of the oscilloscope.

    If you are using a Tektronix PG 502, set the controls as follows:

Pulse duration	—	SQ. WAVE
Period	—	0.1 μS
Output level	—	2 volts p-p around ground
Back term	—	OUT
NORM	—	OUT
Variables	—	X1

2. Set up the 50 MHz pulse generator to display the waveform shown in Figure 5-29. This will be displayed on channel 2 of the oscilloscope.
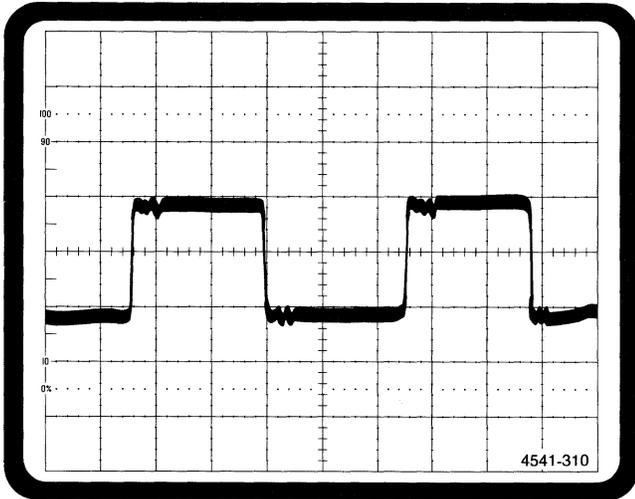
Figure 5-28. 250 MHz pulse generator waveform.

Figure 5-29. 50 MHz pulse generator waveform.

If you are using a Tektronix PG 508, set the controls as follows:

Period	—	0.2 μS
Delay	—	10 nS
Duration	—	10 nS
Mode	—	Delay
Triggering	—	Slope +
		Sync gate
Transition Time	—	5 nS
leading	—	X1
trailing	—	X1
Duration var	—	See *Preliminary Equipment Adjustments*
		below
Output Volts	—	Low level/High level: 2V p-p around GND
		COMP
		Var
Trig Gate In	—	Internally set to 50 Ω

NOTE

When you are using the PG 508, adjust the TRIG/GATE LEVEL until the TRIG'D GATED LED flickers. When the LED is not flickering, no pulse is being generated.

3. Set up the Setup and Hold Time Test Fixture as follows:

    a. Press in the EXT DELAY button.

    b. Connect P6460 probes to the Setup and Hold Time Test Fixture as follows:

    91A24: Connect three P6460 probes from pods A, B, and C of the 91A24 to the AA-55 pattern pins on the lower three connectors. Connect the white clock lead from the P6460 probe in pod A to one of the clock ⎍ output pins. Connect the gray qualifier lead from the same P6460 to bit 7 of the bottom (AA-55 pattern) row of the top data source connector.

    Connect the USR GRND leads from all P6460 probes to the ground lug on the test fixture.

    See Figure 5-26 for 91A24 connections.

    91AE24: Connect three P6460 probes from pods A, B, and C of the 91AE24 to the AA-55 pattern pins on the lower three connectors.

    Connect a fourth P6460 probe from the 91A24 module (pod A) to the test fixture by connecting the white clock lead from the 91A24 probe to one of the clock ⎍ output pins.

    Connect the USR GRND leads from all P6460 probes to the ground lug on the test fixture.

    See Figure 5-27 for 91AE24 connections.

4. Set up the dual-trace, 100 MHz oscilloscope to display the Setup and Hold Time Test Fixture clock and data. Since you have no input yet, these traces will be flat.

If you are using a Tektronix 485, set the controls as follows:

CHANNEL 1	—	500 mV/div.
GND	—	1.4 V above center graticule
CHANNEL 2	—	1 V/div.
GND	—	1.4 V above center graticule
TRIGGER MODE	—	Channel 2
DISPLAY MODE	—	Alt.
TIME BASE	—	10 nS/div.

Preliminary Equipment Adjustments

1. Disconnect the oscilloscope probes from the pulse generators.

2. Connect the oscilloscope grounds to the test fixture ground lug.

3. Using probe tip adapters, connect the oscilloscope probes to the Setup and Hold Time Test Fixture as indicated below:

CH 1	—	CLK ⌐
CH 2	—	Bit 0 of the top data source connector (AA-55 pattern)

4. Adjust channel 1 for a 25 ns positive pulse width using the PG 508 DURATION variable control.

5. Adjust the PG 508 DELAY variable so that the rising edge of channel 1 occurs 25 ns after the rising edge of channel 2.

    Figure 5-30 shows this waveform at 50 ns/dv; Figure 5-31 shows the same waveform at 10 ns/div.

Figure 5-30. 100 MHz oscilloscope waveform for step 5 of the performance check (time base = 50 ns).
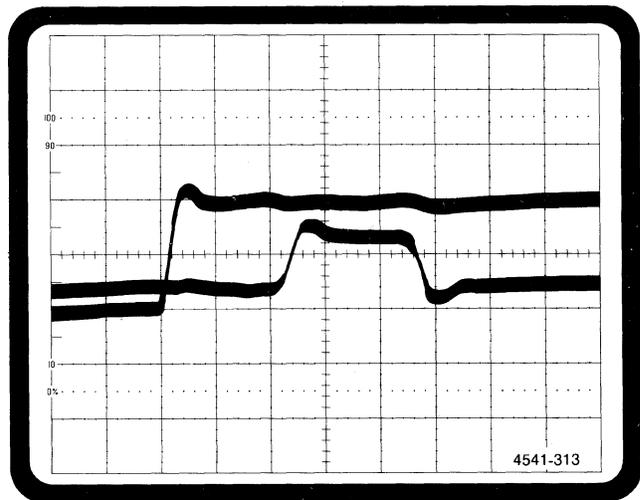
Figure 5-31. 100 MHz oscilloscope waveform for step 5 of the performance check (time base = 10 ns).

6. Readjust the 50 MHz pulse generator duration if necessary.

7. Set up the DAS as follows:

    a. Power the DAS down, then up.

    b. Enter the Channel Specification menu and change the threshold setting to -1.3 V.

    c. Enter the Trigger Specification menu. If you are testing a 91A24, change word recognizer #1 to AX XX XX. If you are testing a 91AE24, change word recognizer #1 to AXXX XXXX XXXX.

    d. Enter the Clock Specification sub-menu and select EXT CLK.

    e. Change all clock expressions to (CLKA ⌐ * QA).

    f. Enter the State Table menu and change the START SEQ field value to 14.

8. Press the START ACQUISITION key. You should acquire only AAs.

9. Press the STORE key.

SETUP AND HOLD TESTS

To test setup and hold times on a 91A24 or 91AE24 module, you will need to perform six tests. These tests are summarized in Table 5-8. The initial test connections for a 91A24 module are shown in Figure 5-26; initial connections for a 91AE24 are shown in Figure 5-27.

For each of the six tests:

- make the connections and menu expression changes listed in Table 5-8,
- make any probe connection changes indicated under the numbered test directions, then
- follow the procedure listed under *Setup and Hold Test Sequence.*

Table 5-8
SETUP FOR SETUP AND HOLD TESTS

Test[1]	91A24 Clock Menu Expression[2] *(for all pod clocks: A, B, C)*	S & H Connections CLK	QUAL[3]	91A24 Master Clock
1. Pod A Clock ⌐	CLKA ⌐ * QA	⌐	bit 7	A
2. Pod A Clock ⌐	CLKA ⌐ * /QA	⌐	bit 6	A
3. Pod B Clock ⌐	CLKB ⌐ * QA	⌐	bit 7	B
4. Pod B Clock ⌐	CLKB ⌐ * /QA	⌐	bit 6	B
5. Pod C Clock ⌐	CLKC ⌐ * QA	⌐	bit 7	C
6. Pod C Clock ⌐	CLKC ⌐ * /QA	⌐	bit 6	C

[1] The pod indicated in the Test column indicates which pod's clock and qualifier are used in that test (e.g., use the clock and qualifier from the probe in pod A to run test 1).

[2] Enter the indicated clock expression for all three pod clocks (A, B, and C).

[3] Connect the gray qualifier lead from the P6460 probe to bit 7 or 6 (as indicated for each test) of the AA-55 row of the top data source connector on the Setup and Hold Time Test Fixture.

Test 1: Pod A Clock ⌐

Set all pod clock values in the DAS Clock Specification sub-menu to match the clock expression shown for test 1 in Table 5-8. Make the indicated connections to the test fixture. Follow the test sequence.

Test 2: Pod A Clock ⌐

Set all pod clock values in the DAS Clock Specification sub-menu to match the clock expression shown for test 2 in Table 5-8. Make the indicated connections to the test fixture. Follow the test sequence.

Test 3: Pod B Clock ⎍

91A24: At the 91A24 module, swap the probes in pods A and B.

91AE24: Leave the probes as initially set up. Set all pod clock values in the DAS Clock Specification sub-menu to match the clock expression shown for test 3 in Table 5-8. Make the indicated connections to the test fixture. Follow the test sequence.

Test 4: Pod B Clock ⎏

Leave the probes as set up for test 3. Set all pod clock values in the DAS Clock Specification sub-menu to match the clock expression shown for test 4 in Table 5-8. Make the indicated connections to the test fixture. Follow the test sequence.

Test 5: Pod C Clock ⎍

91A24: At the 91A24 module, swap the probe in the pod A connector with the probe in the pod C connector.

91AE24: Leave the probes as initially set up. Set all pod clock values in the DAS Clock Specification sub-menu to match the clock expression shown for test 5 in Table 5-8. Make the indicated connections to the test fixture. Follow the test sequence.

Test 6: Pod C Clock ⎏

Leave the probes as set up for test 5. Set all pod clock values in the DAS Clock Specification sub-menu to match the clock expression shown for test 6 in Table 5-8. Make the indicated connections to the test fixture. Follow the test sequence.

Setup and Hold Test Sequence

1. Press the COMPARE ≠ key and verify that the module restarts.

2. Press the TH 0nS button on the test fixture and verify that the module continues to restart.

3. Press the STOP key.

4. Press in the EXT DELAY button on the test fixture.

MUX MODE TEST

1. Reconnect all probes to the 91A24 as follows:

   a. Connect the 91A24 pod A probe to the DAS and to the AA-55 pins of the data output port third up from the bottom on the Setup and Hold Time Test Fixture.

   b. Connect 91A24 pods B and C probes to the DAS and to the AA-55 pins of the two lower data output ports on the Setup and Hold Time Test Fixture. Connect the 91A24 pod A lead set CLK lead (white) to the CLK ⌐ top data source connector on the test fixture.

   c. Connect the USER GND on all P6460 probes to the ground lug on the test fixture.

2. Enter the 91A24 Clock Specification sub-menu, and change all pod clock expressions to CLKA ⌐.

3. Change the Master Clock field to POD A.

4. Enter the 91A24 Trigger Specification sub-menu. Move the cursor to LEVEL 1 word recognizer and enter AX XX XX.

5. Press the START ACQ key. The DAS should acquire a repeating AA-55 pattern.

6. Acquire data until the data shows the AA-55 pattern, then press the STORE key.

7. Remove the P6460 from pod B.

8. Press the START ACQUISITION key and verify that the test triggers. Also verify that pod B data is all zeros while the other pods show AA-55 patterns.

9. Enter the 91A24 Clock Specification sub-menu. Change the ACQUIRED FROM field from 1A/1B to 1A.

10. Press the COMPARE ≠ key and verify that the system restarts.

11. Press the TH 0ns button on the test fixture and verify that the module continues to restart.

12. Press the STOP key on the DAS.

13. Disconnect all test equipment.

MAINTENANCE: GENERAL INFORMATION

Tektronix maintains repair and recalibration facilities at its local Field Service Centers and the Factory Service Center. For further information or assistance, contact your local Tektronix Field Office or representative.

SPECIAL 91A24 MAINTENANCE INFORMATION

INSTALLING OR REMOVING INSTRUMENT MODULES

See the *Operating Instructions* portion of this addendum for instructions on installing or removing 91A24 and 91AE24 modules.

USING EXTENDER BOARDS

To operate a 91AE24 module on an extender board you need 11-inch interconnect cables to connect the 91AE24 module to the 91A24 module. These long interconnect cables are included as part of the Service Maintenance Kit. They can also be ordered separately.

GENERAL MAINTENANCE PRECAUTIONS

The maintenance procedures for 91A24/91AE24 modules and the P6460 and P6462 probes are similar to the procedures for any other DAS module or probe. Refer to the *DAS 9100 Series Service Manual* for general maintenance procedures and precautions.

SOLDERING

Most of the components in the instrument are soldered in place. If it is necessary to replace a soldered part, use a 15 W soldering iron to prevent heat damage to the circuit board or components. Excessive heat will lift circuit runs on the circuit board.

The flux in the solder may leave a residue on the circuit board that can provide a high resistance leakage path and affect instrument operation. Be sure to clean off this residue. Isopropyl alcohol is effective.

STATIC PRECAUTIONS

$$\{\ CAUTION\ \}$$

Static discharge can damage any semiconductor in this instrument.

This instrument contains electrical components that are susceptible to damage from static discharge. See Table 6-1 for the relative susceptibility of various classes of semiconductors. Static voltages of 1—30 kV are common in unprotected environments.

Observe the following precautions to avoid damage:

1. Minimize handling of static-sensitive components.

2. Transport and store static-sensitive components or assemblies in their original containers, on a metal rail, or on conductive foam. Label any package that contains static-sensitive components or assemblies.

3. Discharge the static voltage from your body by wearing a wrist strap while handling these components. Servicing static-sensitive assemblies should be performed only in a static-free work station by qualified service personnel.

4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.

5. Keep the component leads shorted together whenever possible.

6. Pick up components by the body, never by the leads.

7. Do not slide the components over any surface.

8. Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.

9. Use a soldering iron that is connected to earth ground.

10. Use only special anti-static suction-type or wick-type desoldering tools.

NOTE

Damage to electrical components may not be immediately apparent. Always follow the precautionary measures listed above when handling static-sensitive components.

Table 6-1
RELATIVE SUSCEPTIBILITY OF SEMICONDUCTORS
TO STATIC DISCHARGE DAMAGE

Semiconductor Class	Danger Voltage[a]
MOS or CMOS	100 - 500 V
ECL	200 - 500 V
Schottky signal diodes	250 V
Schottky TTL	500 V
High-frequency bipolar transistors	400 - 600 V
JFETs	600 - 800 V
Linear microcircuits	400 - 1000 V
Low-power Schottky TTL	1200 V

[a]Voltage discharged from a 100 pF capacitor through a resistance of 100 Ω.

TEST EQUIPMENT REQUIRED FOR MAINTENANCE

Test equipment required to service the instrument is listed under *Troubleshooting Equipment* in the *Maintenance: Troubleshooting* section of this manual.

TOOLS REQUIRED FOR MAINTENANCE

The following tools are those most often needed when servicing the instrument:

Table 6-2
TOOLS REQUIRED FOR MAINTENANCE

Tool	Tektronix Part No.
1. Soldering iron, (15 W)	
2. Rosin core solder, 60/40	
3. Isopropyl alcohol	
4. Lint-free dust cloth	
5. Soft-bristle brush	
6. IC extractor	
7. Desolder tool	
8. Solder wick	
9. Magnetic screwdrivers, 7 inch shank and 4 inch shank	
10. POZIDRIV-type magnetic bits, 2 inch and 1 inch	
11. TORX-type magnetic bit, size T-20	003-0866-00
12. Angled tweezers, 6 inch	
13. Long-nose pliers	
14. 1/4 inch combination open/box wrench	
15. Plastic alignment tool, 5 inch	
16. Fiber adjustment tool, 9 inch	
17. Open-end wrench, 7/16 inch	
18. Allen wrenches, 0.050 inch, 1/16 inch and 5/64 inch	
19. Circuit board ejector	214-3154-00

MAINTENANCE: TROUBLESHOOTING

Tektronix maintains repair and recalibration facilities at its local Field Service Centers and the Factory Service Center. For further information or assistance, contact your local Tektronix Field Office or representative.

HOW TO USE THIS SECTION

WARNING

Read the troubleshooting precautions before using any of the troubleshooting procedures provided in this section.

This section contains troubleshooting information for the 91A24 and 91AE24 Data Acquisition modules. Most of the troubleshooting procedures rely on the self-diagnostics.

If you are not familiar with the DAS Diagnostics menu, read the description of it later in this section.

The self-diagnostics progressively test each module. The diagnostics test the smallest possible failure area first and gradually expand to test as much of the module as possible. Therefore, the first diagnostic test to fail will have isolated a small number of possible component failures.

Troubleshooting Procedures. To troubleshoot a module:

1. Enter the Diagnostics menu and turn on LOOPING.

2. Run the diagnostics on the suspect module. Stop when you reach the first function failure.

3. Note the failed function name and test number. Then look up the failed module, function, and test number in the Table of Contents at the front of this addendum. The page number indicated has the desired troubleshooting information.

4. Turn to the page indicated and follow the instructions given there.

Diagnostic Descriptions. Detailed descriptions of the diagnostic tests follow the corresponding troubleshooting information. The descriptions are useful when a diagnostic test has failed, but the troubleshooting information has not diagnosed the problem. In these situations, use the test description to understand how the diagnostic test works and perform your own diagnosis.

TROUBLESHOOTING PRECAUTIONS

INTERNAL INSTRUMENT ACCESS

WARNING

Electric shock hazards inside the DAS mainframe may be exposed when protective covers are removed.

SOLDERING

Most of the components in the instrument are soldered in place. If it is necessary to replace a soldered part, use a 15 W soldering iron to prevent heat damage to the circuit board or components. Excessive heat will lift circuit runs on the circuit board.

The flux in the solder may leave a residue on the circuit board that can provide a high-resistance leakage path and affect instrument operation. Be sure to clean off this residue with isopropyl alchohol or a similar solvent.

STATIC DISCHARGE DAMAGE

{ *CAUTION* }

All devices in the instrument are susceptible to damage by static discharge.

Most of the devices in the DAS are static-sensitive and may be damaged by improper handling. See Table 7-1 for the relative susceptibility of various classes of semiconductors. Static voltages of 1 to 30 kV are common in unprotected environments.

Table 7-1
RELATIVE SUSCEPTIBILITY OF SEMICONDUCTORS
TO STATIC DISCHARGE DAMAGE

Semiconductor Class	Danger Voltage [a]
MOS or CMOS	100 - 500 V
ECL	200 - 500 V
Schottky signal diodes	250 V
Schottky TTL	500 V
High frequency bipolar transistors	400 - 600 V
JFETs	600 - 800 V
Linear microcircuits	400 - 1000 V
Low-power Schottky TTL	1200 V

[a] Voltage discharged from a 100 pF capacitor through a resistance of 100 Ω.

TROUBLESHOOTING EQUIPMENT

The following equipment, or equivalent, is recommended for troubleshooting the DAS 91A24 and 91AE24 modules:

• A DAS Mainframe.

• DAS 9100 Series Service Maintenance Kit (see the optional accessories list in under *Optional Accessories* in the *Introduction and Specifications* section for the part number).

• A two-channel oscilloscope and two probes. The scope and probe bandwidth should be at least 100 MHz.

- A 250 MHz pulse generator with variable pulse width and period (for example, the Tektronix PG502 Pulse Generator).

- A 3.5 digit, 1% accuracy digital multimeter (for example, a Tektronix DM 502A Digital Multimeter).

- A variable voltage source.

- A logic analyzer is required to troubleshoot some bus problems.

TROUBLESHOOTING AIDS

The DAS contains a set of self-diagnostic tests. These tests can be used by the troubleshooter to isolate the section of a circuit board that failed, and in some instances, to indicate the specific component at fault.

The self-diagnostics are the basis for most of the troubleshooting information provided in this section. How to use and access this troubleshooting information is discussed at the beginning of this section.

As an additional troubleshooting aid, schematics for the 91A24 and 91AE24 modules show the signal flow of the self-diagnostics with colors. For information on how to use the color coding on the schematics, refer to the introduction to the *Diagrams* section.

THE DIAGNOSTICS MENU

DAS diagnostics information is presented in two menus: the power-up display and the Diagnostics menu.

The DAS self-diagnostics are only accessible when the power-up display shows that one of the modules has failed the power-up diagnostics. The power-up diagnostics are a limited number of brief functional tests that are run whenever the DAS is powered up. These tests verify the basic functions of the DAS, but are not comprehensive.

A module in the DAS can fail in such a way that the power-up diagnostics do not detect the failure. To access the self-diagnostics in this situation, the operator can induce a power-up diagnostic failure from the keyboard by holding down any key on the keyboard (other than SHIFT or START) from the time the DAS is turned on until the power-up diagnostics are finished.

When the power-up diagnostics fail, the power-up display should be similar to Figure 7-1. To enter the Diagnostics menu, press the START SYSTEM key.

NOTE

Do not press any key other than START SYSTEM. If you do, you may leave the power-up display and lose access to the Diagnostics menu. The diagnostics are only accessible when the power-up display shows a failure (or over GPIB).

```
┌─────────────────────────────────────────────────────────────────┐
│ TEKTRONIX DAS 9100 SELF TEST IN PROGRESS        FIRMWARE VERSION 1.11 │
│                                                                   │
│ CONFIGURATION:                                                    │
│                                                                   │
│      SLOT 0    CONTROLLER                                    PASS  │
│      SLOT 1    91A24    24 CHANNEL /100nS ACQUISITION MODULE V1  FAIL  0 │
│      SLOT 2    91AE24   24 CHANNEL /100nS ACQUISITION MODULE     PASS  │
│      SLOT 3                                                        │
│      SLOT 4                                                        │
│      SLOT 5                                                        │
│      SLOT 6    91A08     8 CHANNEL / 10nS ACQUISITION MODULE     PASS  │
│      SLOT 7    TRIGGER / TIME BASE                           PASS  │
│      SLOT 8    I/O OPTION                                          │
│                                                                   │
│                                                                   │
│                                                                   │
│                                                                   │
│      PRESS:  START SYSTEM  TO ENTER DIAGNOSTICS.                   │
│              DON'T CARE  TO BEGIN OPERATION.          4541-748     │
└─────────────────────────────────────────────────────────────────┘
```

Figure 7-1. Failure in the power-up self test.

When first entered, the Diagnostics menu should look similar to Figure 7-2. The Diagnostics menu is controlled by the cursor keys, the SELECT key, and the data entry keys.

All changeable fields in the menu are shown in reverse video. Change fields by moving the blinking screen cursor into the field to be changed. Move the cursor by pressing the up, down, right, and left cursor arrows, and the NEXT key. Change the field value by using the SELECT key, or by entering a hexadecimal value from the data entry keys.

```
┌─────────────────────────────────────────────────────────────────┐
│ DAS 9100 DIAGNOSTICS       MODULE: SINGLE  SLOT: 1    LOOPING: OFF │
│                                                                   │
│                            MODE: SINGLE  FUNCTION: 0              │
│                                                                   │
│ FUNCTIONS FOR SLOT: 1, 91A24                                      │
│         0 CNTR TIMR    4 WRD REC                                   │
│         1 MEM ADDR     5 OCCR CNTR                                 │
│         2 ACQ MEM      6 DAC THRSH                                 │
│         3 STK PNTR     7 PRB CLK EX                                │
│                                                                   │
│ PRESS: START SYSTEM  TO BEGIN TEST.                               │
│ ─────────────────────────────────────────────────────────────    │
│                                                      4541-750     │
└─────────────────────────────────────────────────────────────────┘
```

Figure 7-2. Diagnostics menu.

After the menu is set to run the desired test, start the test by pressing the START SYSTEM key. Tests then stop themselves or can be stopped by pressing the STOP key.

Exit the Diagnostics menu may by pressing any menu selection key while no tests are running. This will display the selected menu on the screen. You cannot re-enter the diagnostics from the standard menus.

DIAGNOSTICS CONTROL SUMMARY

In summary, the diagnostics are controlled in the following way:

- Force a power-up diagnostic failure by pressing and holding down a keyboard key immediately after the DAS is turned on.

- Press the START SYSTEM key to enter the Diagnostics menu.

- Change the reverse-video fields on the display to the desired values using the cursor control keys and the data entry keys.

- Press the START SYSTEM key to start the diagnostic test or function.

- The function will stop by itself, or you can press the STOP key to stop the function.

- To exit the Diagnostics menu, press a menu selection key while no tests are running. You must turn off or reset the DAS to re-enter the Diagnostics menu.

DIAGNOSTIC MENU FIELDS

There are six user-changeable fields normally in the Diagnostics menu. All of these fields can apply to any diagnostic test. These fields and the procedures for changing them are described next. There may also be other changeable fields associated with individual functions. These unique fields are explained by the Diagnostics menu with prompting messages or field names.

MODULE

Use this field to specify whether a single module or all of the modules are to be tested. You may set the field to a value of either SINGLE or ALL by using the SELECT key.

If the field is set to ALL, all modules in the DAS are run through a limited number of diagnostic functions. To keep the running time reasonable, not all of the diagnostic functions are run when ALL is selected to.

If the field is set to SINGLE, another field (SLOT) appears that allows the user to select the specific module to be tested. You can then run all available functions for that module.

SLOT

This field appears when the MODULE field is set to SINGLE. Use the SLOT field to specify which individual module is to be tested. Specify the module by entering the module's slot number into the field.

MODE

The MODE field appears when a bus-slot number is entered in the SLOT field. The MODE field specifies whether a single function or all of the module functions are to be tested. Use the SELECT key to set the MODE field to either SINGLE or ALL.

When the cursor moves into the MODE field, a list of module functions appears on the DAS screen. If the MODE field is set to ALL, all of these module functions will be tested.

If the MODE field is set to SINGLE, a new field (FUNCTION) appears that allows testing of individual functions.

FUNCTION

The FUNCTION field appears when the MODE field is set to SINGLE. The FUNCTION field is used to specify which one of the displayed list of functions will be tested. Specify a function by entering its number into the FUNCTION field.

LOOPING

NOTE

When the DAS self-diagnostics are in looping mode, the signal at TP191 on the Trigger/Time Base assembly (slot 7) pulses low at the end of each execution of any diagnostic test in the DAS. Use this test point to trigger an oscilloscope or a logic analyzer.

The LOOPING field is always present and may be set either ON or OFF with the SELECT key. When the field is set to ON, the looping feature allows one test or a sequence of tests to be run continuously. If it is set to OFF, the selected function tests run once, then stop.

The DAS loops differently depending on other Diagnostics menu settings. If the MODULE field is set to ALL with looping on, the DAS tests all modules in the mainframe then goes back to the beginning to repeat the tests. This mode is useful for finding intermittent failures on some unknown module in the mainframe. When an error occurs, it is highlighted and remains on the screen. Errors remain displayed even if the same module passes during a later loop.

If the MODULE field is set to SINGLE, but the MODE field says ALL, then all functions on the selected module are tested repeatedly. The DAS behaviour is similar to looping on all modules.

If the MODE field says single, the DAS loops on a single test in the selected function. The looping sequence starts by running the first test in a function, test 0. Press the SELECT key to advance to the next test. You can select any test in the function by pressing the SELECT key repeatedly.

DISPLAY

The DISPLAY field only appears on the screen when the LOOPING field is set to ON and the MODE field is set to SINGLE. The field may be used to turn off the video screen refresh while a test is looping. This is useful when tracing signals with an oscilloscope, since it helps to stablize the oscilloscope's traces.

Use the SELECT key to set the DISPLAY field to ON or OFF. If the field is set to ON, the video screen display is present. If the field is set to OFF, the screen is blank.

NOTE

When the DISPLAY field is turned OFF, the test loop being run can only be terminated by pressing the STOP key or turning off power to the DAS.

When the DISPLAY field has been set to OFF and a test is being run, the following keys have these effects:

- Pressing STOP ends the test and returns the display to normal.

- Pressing SELECT displays the results of the previous test momentarily, then turns the display off and runs the next test.

- Pressing any key on the keyboard (except SHIFT) turns the display on momentarily.

If an error occurs while a diagnostic test is running and the DISPLAY field is set to OFF, the LOCK-OUT and REMOTE indicators on the keyboard light up.

QUICK REFERENCE FUNCTION DESCRIPTIONS

The following list briefly describes the diagnostic functions for the 91A24 and 91AE24 Data Acquisition modules. If functions are run individually, they should be run in the listed order under the module type. Only the functions for the module in question need be run.

There are a few diagnostic functions that do not have self-readback capability (digital-to-analog converter tests, for example). These tests require the technician to monitor test points while the test is running. Non-readback tests are indicated by an * (asterisk) after the test name.

The tests in each function can be selected individually only when the diagnostics are in a looping mode. For more information, refer to the description of LOOPING earlier in this section.

91A24

CNTR TIMR. This function verifies that the Counter/Timer counters can be cleared, clocked, and read. Most of the circuitry tested by the CNTR TIMR function is on schematics 68 and 76.

MEM ADDR. This function verifies the operation of the memory address registers and the write enable generators. These tests check the circuitry that addresses the acquisition RAMs. Most of the circuitry tested by the MEM ADDR function is on schematics 69, 73, and 77.

ACQ MEM. This function verifies the address and data independence of the 91A24 acquisition memory, and checks associated write and readback circuits. The ACQ MEM function tests the RAMs that are used by the 91A24 to store acquired data. Most of the circuitry tested by the ACQ MEM function is on schematics 69, 72, and 73.

STK PNTR. This function verifies that the occurrence stack pointer (U571) can be loaded and clocked, and runs a memory test on the control stack RAM (U555). Most of the circuitry tested by the STK PNTR function is on schematics 75 and 76.

WRD REC. This function tests the 91A24 word recognizer by verifying the operation of the word recognition RAMs. Most of the circuitry tested by this function is on schematics 74 and 75.

OCCR CNTR. This function verifies that the occurrence counter can be loaded and clocked, and runs a memory test on the occurrence counter RAM. This function also tests the stack word recognizer trigger and the OR trigger. Most of the circuitry tested by this function is on schematics 74, 75, and 76.

DAC THRSH*. This function exercises the probe threshold DAC to verify voltage accuracy, and to make sure all voltages may be selected. The circuitry exercised by this function is on schematic 71.

PRB CLK EX. This function tests the probe clock receiver and clock qualifier circuitry, and verifies the operation of the login registers. Most of the circuitry tested by this function is on schematics 70, 71, 72, 77, and 78.

NOTE

Probes with variable threshold capability must be installed on the 91A24 for the PRB CLK EX function to run properly.

91AE24

MEM ADDR. This function verifies the operation of the memory address registers and the write enable generators. These tests check the circuitry that addresses the acquisition RAMs. Most of the circuitry tested by the MEM ADDR function is on schematics 79, 80, 84, and 87.

ACQ MEM. This function verifies the address and data independence of the 91AE24 acquisition memory, and checks associated write and readback circuits. The ACQ MEM function tests the RAMs that are used by the 91AE24 to store acquired data. Most of the circuitry tested by the ACQ MEM function is on schematics 80, 83, 84, and 85.

STK PNTR. This function verifies that the occurrence stack pointer (U571) can be loaded and clocked, and runs a memory test on the control stack RAM (U555). Most of the circuitry tested by the STK PNTR function is on schematics 86.

WRD REC. This function tests the 91AE24 word recognizer by verifying the operation of the word recognition RAMs. Most of the circuitry tested by this function is on schematics 85 and 86.

DAC THRSH*. This function exercises the probe threshold DAC to verify voltage accuracy, and to make sure all voltages may be selected. The circuitry exercised by this function is on schematic 82.

PRB CLK EX. This function tests the probe clock receiver and clock qualifier circuitry, and verifies the operation of the login registers. Most of the circuitry tested by this function is on schematics 81, 82, and 83.

NOTE

Probes with variable threshold capability must be installed on the 91A24 for the PRB CLK EX function to run properly.

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*Non-readback functions require test point monitoring.

91A24 FUNCTION 0 CNTR TIMR

CIRCUIT OVERVIEW

The CNTR TIMER (counter/timer) function tests the stack word recognizer's counter/timer circuit. This circuit contains a 16-bit counter, and associated control and readback circuitry. For a more detailed description of the counter/timer operation, see the *Theory of Operation* section.

FUNCTION DESCRIPTION

The CNTR TIMR function consists of a single test. The function verifies that the counter/timer counters can be cleared, clocked, and read. Also, since this function (function 0) is the first to exercise the 91A24 Controller Interface, a PASS on the CNTR TIMR function indicates that a significant portion of the 91A24 controller interface is functional (See 91A24 schematic 68).

Readback Ports

Results of counter/timer test 0 are read through U788 (port 05) and U795 (port 06) on schematic 76.

91A24 CNTR TIMR TEST 0 TROUBLESHOOTING

Reading the Error Codes

Test 0 of the CNTR TIMR function provides test results like those shown in Figure 7-3.
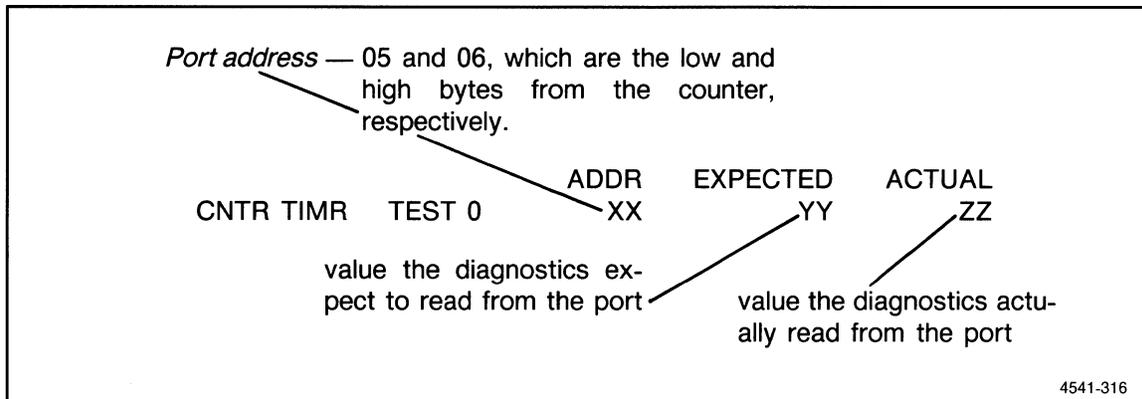
Figure 7-3. **91A24 CNTR TIMR test 0 readback display.** The ACTUAL value is read from the counter/timer low byte first, followed by the high byte. The EXPECTED value may be 00, 55, or AA.

Error Indication

		ADDR	EXPECTED	ACTUAL
CNTR TIMR	TEST 0	XX	00	ZZ

Possible Cause	Action
Address decoder malfunction.	Loop test 0. With an oscilloscope, check U558B pin 8 for low pulses; if none, suspect U558B (on schematic 68). Otherwise, check U965 pin 13 for low pulses; if none, suspect U965.
Data buffer enable malfunction.	While test 0 is still looping, check U768 pins 1 and 19 (schematic 68) for low pulses. If low pulses are present, the data buffer enable is okay.
	If low pulses are not present at U768 pins 1 and 9, check U975 pins 14 and 16 (on schematic 68) for low pulses; if not present, suspect U975. Otherwise, suspect U285.
$\overline{CNTL2}$ malfunction.	Loop test 0. Check U758 pin 11 for low pulses. If no low pulses, suspect U958 (on schematic 68).
$\overline{RESET\ CNTR\ EN}$ malfunction.	While test 0 is still looping, check U758 pin 9 for low; if not low, suspect U758 (schematic 68).
$\overline{CNTR\ CLR}$ malfunction.	Check U998 pin 9 for low pulses; if none, suspect U998 (on schematic 69).
U471B malfunction (on schematic 76).	Check U475C pin 10 for high level; if not high, check U495B pin 4 for a low. If U495B pin 4 is low, suspect U471 (on schematic 76); otherwise suspect U495 (also on schematic 76).
No clear pulse to counters.	Check U475C pin 8 for low pulses; if no low pulses, suspect U475 (schematic 76). If there are low pulses on U475C pin 8, check U198D pin 11 for low pulses; if no low pulses, suspect U198 (on schematic 76).
Counter malfunction.	Check outputs of U585, U588, U591, and U595 on schematic 76. If any outputs are high, suspect the device with the high output.
Counter/timer readback malfunction.	Check U788 pin 1 and U795 pin 1 for low pulses. If no low pulses on either, suspect U998 (on schematic 68). If there are low pulses present, suspect U788 or U795 (on schematic 76).

Error Indication

			ADDR	EXPECTED	ACTUAL
CNTR TIMR		TEST 0	XX	$\underline{\text{YY}}$	ZZ
				Not 00	

Possible Cause	Action
Malfunctioning counter readback signals.	Loop test 0. With a scope, monitor U998 pins 6 and 7 (on schematic 69) for low pulses. If low pulses are not present, suspect U998.
Malfunctioning $\overline{\text{TIMER CLK}}$.	With test 0 still looping, look for high pulses on U491A pin 5 (schematic 76). If pulses are present, $\overline{\text{TIMER CLK}}$ is okay, proceed to the next possible cause. Otherwise, check for low pulses on U965 pin 16 (schematic 68); if low pulses are not present, suspect U965. If low pulses are present on U965 pin 16, check U495C pins 5 and 6 (schematic 76) to see if they are always opposite each other. If they are not always opposite, suspect U495. Otherwise, suspect U491A.
Malfunctioning counters.	Look for toggling output signals at pins 11, 12, 13, 14, and 15 of U585, U588, U591 (on schematic 76), and pins 11, 12, 13, and 14 of U595 (on schematic 76). If any signal does not change states, suspect that IC.
Malfunctioning readback buffers.	Suspect U788 or U795 (on schematic 76). If a logic analyzer is available, acquire data from the inputs and from the outputs of these buffers, with the logic analyzer clocking off of the enable signal. When compared on a state table, if the acquired inputs and outputs of one buffer are not equal, suspect that buffer. If the inputs equal the outputs on both buffers, examine the acquired input data. If data input to the buffers from one of the counters (U585, U588, U591, or U595) does not equal 0_{16}, 5_{16}, or A_{16}, suspect that counter.

91A24 CNTR TIMR TEST 0 DESCRIPTION
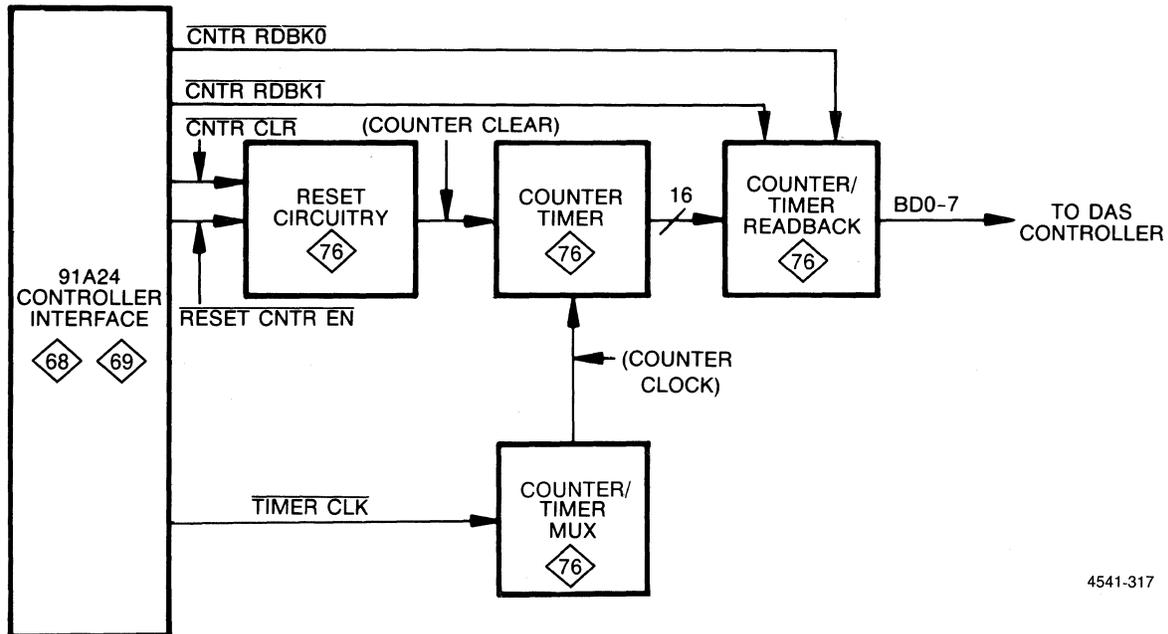
Figure 7-4. Blocks of the 91A24 tested by the CNTR TIMR function, test 0.

CNTR TIMR test 0 checks the clear, readback, and clocking circuits of the counter/timer. The test contains five separate steps which include clearing, clocking, and reading the counters.

1. Clear the counter/timer, then read high and low bytes. Display an error if 00_{16} is not read both times.

2. Clock the counter/timer to 0055, then read and verify both bytes.

3. Clock the counter/timer to 00AA, then read and verify both bytes.

4. Clock the counter/timer to 5555, then read and verify both bytes.

5. Clock the counter/timer to AAAA, then read and verify both bytes.

Test 0 Readback Port

Test 0 results are read back through buffers U788 (port address 05) and U795 (port address 06) on schematic 76.

Test 0 Initial Conditions

Before the test starts, the module is set up by disabling counter/timer interrupts and disabling clocks to the counter from normal sources.

1. 00_{16} is written to U761 (on schematic 68), which clocks U761 pins 2, 5, and 9 low.

2. U761 pin 2 (INT3 EN) goes low, to disable interrupts from the counter/timer during this test.

3. U761 pin 5 (CT SEL0) and U761 pin 9 (CT SEL1) on schematic 68 go low, which makes U295 pins 7 and 9 (on schematic 76) low, to inhibit clocks to the counter through U295.

Test 0 Run Sequence

After the module is prepared, the counter/timer is clocked through the 91A24 controller interface and the results read back. The test follows this sequence:

1. The counters are cleared by setting $\overline{\text{RESET CNTR EN}}$ (U758 pin 9 on schematic 68) and $\overline{\text{CNTR CLR}}$ (U998 pin 9 on schematic 69) low. These signals pass through U475C and U198D (on schematic 76) to clear counters U585, U588, U591, and U595 (also on schematic 76).

2. The counters are read by making $\overline{\text{CNTR RDBK0}}$ (U998 pin 6 on schematic 69) low. This places the low byte of the counter onto the data bus (BD0-BD7) through U788 (on schematic 76).

   Then $\overline{\text{CNTR RDBK1}}$ (U998 pin 7 on schematic 69) is made low, which places the high byte of the counter onto the data bus (BD0-BD7) through U795 (on schematic 76).

   If the results read back do not equal 00_{16} in both cases, an error is reported and the test stops.

3. The counters are clocked by making $\overline{\text{TIMER CLK}}$ (U965 pin 16 on schematic 68) low. This low goes to U491A pin 4 (on schematic 76), making U491A pin 5 (output) high.

   The counters increment on each rising edge from U491A pin 5. When U491A pin 4 returns high, U491A pin 5 is reset low through U495C.

   The counter is clocked 55_{16} times. After this clocking the counter is read, as in step 2. The value read is expected to equal 0055_{16}.

4. The counter is clocked 55_{16} more times. After this clocking the counter is read, as in step 2, and the read value compared to $00AA_{16}$.

5. The counter is then clocked $54AB_{16}$ times. Then the counter is read, as in step 2. The value read is expected to equal 5555_{16}.

6. The counter is finally clocked 5555_{16} more times. After this clocking the counter is read, as in step 2 and value read is expected to equal $AAAA_{16}$.

91A24 FUNCTION 1 MEM ADDR
91EA24 FUNCTION 0 MEM ADDR

CIRCUIT OVERVIEW

The MEM ADDR function tests the memory address register (MAR). The MAR consists of a 10-bit up-counter (U138, U238, and U438 on 91A24 schematic 73 and 91AE24 schematic 84) that supplies the address for the acquisition memory. When these counters roll over from $3FF_{16}$ to 000_{16}, a status bit (ALL FULL) is set.

For a more detailed treatment of memory address register theory, see the *Theory of Operation* section.

FUNCTION DESCRIPTION

The MEM ADDR function consists of four separate tests.

Test 0 writes a value to each of the low eight bits of the MAR (MAR0-MAR7, U138 and U238 on 91A24 schematic 73 and 91AE24 schematic 84) and reads back the results. This indicates that the eight low-order bits of the MAR are independent and can be read. Additionally, because MEM ADDR test 0 is the first test run on 91AE24 modules, a PASS on MEM ADDR test 0 indicates that a significant portion of the 91AE24 controller interface is functional.

Test 1 writes a value to each of the high two bits of the MAR (MAR8 and MAR9, U438 on schematic 73 or 84) and reads back the results. This indicates that the two high-order bits of the MAR are independent and can be read.

Test 2 clocks the MAR to count from 000_{16} to $3FF_{16}$. When this test runs at power-up, the MAR is only clocked from 000_{16} to $00F_{16}$. This test verifies that the MAR counts correctly.

Test 3 clears the ALL FULL bit by loading the MAR with $3FF_{16}$, then sets the ALL FULL bit by clocking the MAR once, so its count goes from $3FF_{16}$ to 000_{16}. This test verifies the operation of the ALL FULL flip-flop (U461B on 91A24 schematic 73 or 91AE24 schematic 84).

Loading the Data

To test the MAR, the DAS loads data onto BD0-BD7 of the controller interface (91A24 schematic 68 or 91AE24 schematic 79). BD0-BD7 are buffered by U768, U561 and U565 (on schematic 68 or 79) to provide LB0-LB7. MAR CLOCK, coming from U461A pin 6 (on schematic 73 or 84), clocks the data on LB0-LB7 into the MAR.

Readback Ports

Test data is read from U135 and U235 (on 91A24 schematic 69 or 91AE24 schematic 80). When U998 pin 4 ($\overline{\text{MAR LOW}}$ on schematic 69 or 80) goes low, U135 (on schemtic 69 or 80) is enabled, and data is read from MAR0-MAR7 onto the data bus (BD0-BD7).

When U998 pin 5 ($\overline{\text{MAR HIGH}}$) goes low, U235 (on schematic 69 or 80) is enabled, and data is read from MAR8 and MAR9 onto the data bus (BD0-BD7).

91A24 AND 91AE24 MEM ADDR TEST 0 TROUBLESHOOTING

Reading the Test 0 Error Codes

Test 0 of the MEM ADDR function provides test results like those shown in Figure 7-5. The EXPECTED value depends on which of eight passes the test stopped on. These values and their meanings are shown in Table 7-2.
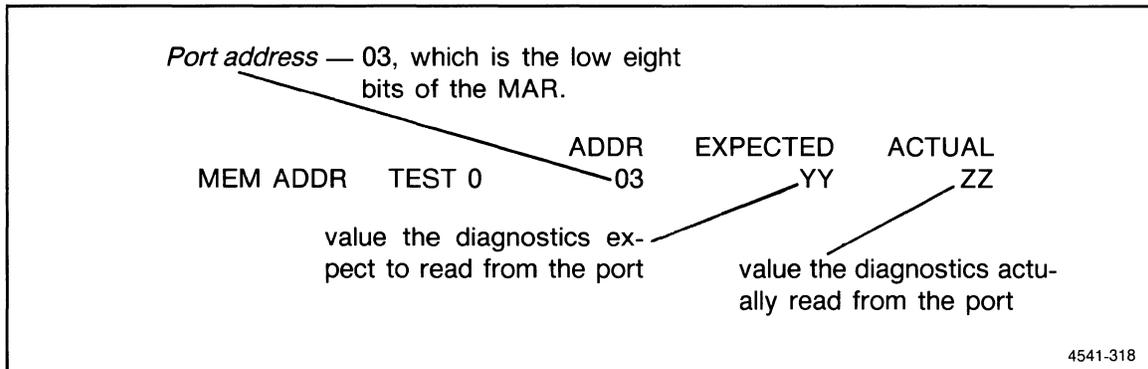
Figure 7-5. MEM ADDR test 0 readback display. The ACTUAL value is read from the low eight bits of the MAR. The EXPECTED field may have any of the values shown in Table 7-2.

Table 7-2
EXPECTED DIAGNOSTIC READBACK VALUES FOR TEST 0

Pass	MAR Bit	Loaded and Expected Value
1	7	80
2	6	40
3	5	20
4	4	10
5	3	08
6	2	04
7	1	02
8	0	01

Error Indication: 91A24

		ADDR	EXPECTED	ACTUAL
MEM ADDR	TEST 1	03	80	ZZ

Possible Cause	Action
CNTL3 malfunction.	Looping test 0. Check U965 pin 13 (on schematic 68) for low pulses; if none, suspect U965.
MAR LD0 malfunction.	While test 0 is still looping, check U765 pin 2 (schematic 68) for low level; if not low, suspect U765.
MEM RD or CNTL1 malfunction.	Check U761 pin 16 (schematic 68) for high level; if not high, suspect U761. If replacing U761 does not correct the problem, suspect U958 (schematic 68).
ENABLE malfunction.	Check U198B pin 6 (on schematic 74) for high level; if not high, suspect U198.
MAR EN malfunction.	Check U288 pin 8 (schematic 74) for low level; if not low, suspect U288.
SINGLE STEP malfunction.	Check U958 pin 10 (on schematic 68) for low pulses; if none, suspect U958.
CA7 malfunction.	Check U945 pin 1 (on schematic 77) for low level; if not low, suspect R921 (schematic 77). If U945 pin 1 is low, check U945 pin 9 (on schematic 77) for high level; if not high, suspect U945 (on schematic 77) or U965 (on schematic 68).
MASTER CLK III malfunction.	Check U461A pin 3 (schematic 73) for low pulses. If pulses are present, MASTER CLK III is okay.

Check U721 pin 2 (schematic 77) for low ECL level pulses; if none, check for high levels on any of the following inputs: U721 pins 12, 10, and 7. If any of these are high, suspect U945 (on schematic 77) or U965 (on schematic 68). If none of the above signals are high, suspect U721.

If low pulses are present on U721 pin 2, check for low pulses on the collector of Q544; if no low pulses, suspect Q543 or Q544. |
MAR CLOCK malfunction.	Check U461A pin 6 (schematic 73) for low pulses; if not pulsing and signal is steady high, check for low pulses on U461A pin 4. If no low pulses on U461A pin 4, refer to the *91AE24 Chip Select Generator* description of ACQ RAM SEL generation in the *Theory of Operation*. If low pulses are present at U461A pin 4, suspect U461.
MAR counter or input buffer malfunction.	Check U238 pin 6 (schematic 73) for high pulses; if none, suspect U565 (schematic 73). If high pulses are present, check U238 pin 11 for high level or high pulses; if none, suspect U238 (schematic 73).
MAR LOW or output buffer malfunction.	Check U998 pin 4 (schematic 69) for low pulses; if none, suspect U998. If low pulses, suspect U135 (schematic 69).

Error Indication: 91A24

		ADDR	EXPECTED	ACTUAL
MEM ADDR	TEST 0	03	YY	ZZ
			40 to 01	

Possible Cause	Action
MAR counter, I/O device malfunction.	Loop test 0. With a logic analyzer, acquire data from inputs of U138 and U238 (schematic 73). Clock the analyzer off of U138 pin 9 (MAR LD0) falling edge. If expected values never present, suspect U561 or U565 (on schematic 68). If expected values present at inputs, use the analyzer to check for expected value on outputs of U138 and U238. If values not present, suspect U138 or U238. If expected values present, suspect U135 (on schematic 69).

Error Indication: 91AE24

		ADDR	EXPECTED	ACTUAL
MEM ADDR	TEST 0	03	80	ZZ

91AE24 fails, but 91A24 passes MEM ADDR test 0. If the 91A24 fails also, troubleshoot the 91A24 first.

Possible Cause	Action
Address decoder malfunction.	Loop test 0. With an oscilloscope, check U558B pin 8 for low pulses; if none, suspect U558B (on schematic 79). Check U285B pin 6 for occasional low pulses (signal pulses low once during each loop); if no low pulses suspect U285 or U975 (on schematic 79). Otherwise, check U965 pin 13 for low pulses; if none, suspect U965.
Data buffer enable malfunction.	While test 0 is still looping, check U768 pins 1 and 19 (schematic 79) for low pulses. If low pulses are present, the data buffer enable is okay.
	If low pulses are not present at U768 pins 1 and 9, check U975 pins 14 and 16 (on schematic 79) for low pulses; if not present, suspect U975. Otherwise, suspect U285.
MAR LD0 malfunction.	Check U765 pin 2 (on schematic 79) for low level; if signal is low, MAR LD0 is okay.
	If U765 pin 2 is not low, check U768 pins 3, 5, 7, 9, 12, 14, 16, and 18 for toggling signals. If any of these signals do not toggle, suspect U768. Otherwise suspect U765.
MEM RD malfunction.	Check U761 pin 16 (on schematic 79) for high level; if not high, suspect U761 or U958 (on schematic 79).
ENABLE malfunction.	Check U198B pin 6 (on schematic 85) for high level; if not high, suspect U198.

Error Indication: 91AE24 (cont.)

		ADDR	EXPECTED	ACTUAL
MEM ADDR	TEST 0	03	80	ZZ

MAR EN malfunction.	Check U288 pin 8 (schematic 85) for low level; if not low, suspect U288.
SINGLE STEP malfunction.	Check U958 pin 10 (on schematic 79) for low pulses; if none, suspect U958.
CA7 malfunction.	Check U945 pin 1 (on schematic 87) for low level; if not low, suspect R921 (schematic 87). If U945 pin 1 is low, check U945 pin 9 (on schematic 87) for high level; if not high, suspect U945 (on schematic 87) or U965 (on schematic 79).
MASTER CLK III malfunction.	Check U461A pin 3 (schematic 84) for low pulses. If pulses are present, MASTER CLK III is okay.
	Check U721 pin 2 (schematic 87) for low ECL level pulses; if none, check for high levels on any of the following inputs: U721 pins 12, 10, and 7. If any of these are high, suspect U945 (on schematic 87). If none of the above signals are high, suspect U721.
	If low pulses are present on U721 pin 2, check for low pulses on the collector of Q544; if no low pulses, suspect Q543 or Q544.
MAR CLOCK malfunction.	Check U461A pin 6 (on schematic 84) for low pulses; if low pulses are present, the MAR CLOCK is okay. If U461A pin 6 is steady high, check for low pulses on U461A pin 4. If low pulses are present at U461A pin 4, suspect U461. If U461A pin 4 is static, refer to the *91AE24 Chip Select Generator* in the *Theory of Operation* to troubleshoot.
MAR counter or input buffer malfunction.	Check U238 pin 6 (on schematic 84) for high pulses; if none, suspect U565 (on schematic 79). If high pulses present, check U238 pin 11 (on schemaic 84) for high level or high pulses; if none, suspect U238.
MAR LOW or output buffer malfunction.	Check U998 pin 4 (on schematic 80) for low pulses; if none, suspect U998. If low pulses, suspect U135 (schematic 80).

Error Indication: 91AE24

			ADDR	EXPECTED	ACTUAL
MEM ADDR	TEST 0		03	YY	ZZ

40 to 01

Possible Cause	Action
MAR counter, I/O device malfunction.	Loop test 0. With a logic analyzer, acquire data from inputs of U138 and U238 (schematic 84). Clock the analyzer off of U138 pin 9 (MAR LD0) falling edge. If expected values never present, suspect U561 or U565 (on schematic 79). If expected values present at inputs, use the analyzer to check for expected value on outputs of U138 and U238. If values not present, suspect U138 or U238. If expected values present, suspect U135 (on schematic 80).

91A24 AND 91AE24 MEM ADDR TEST 0 DESCRIPTION
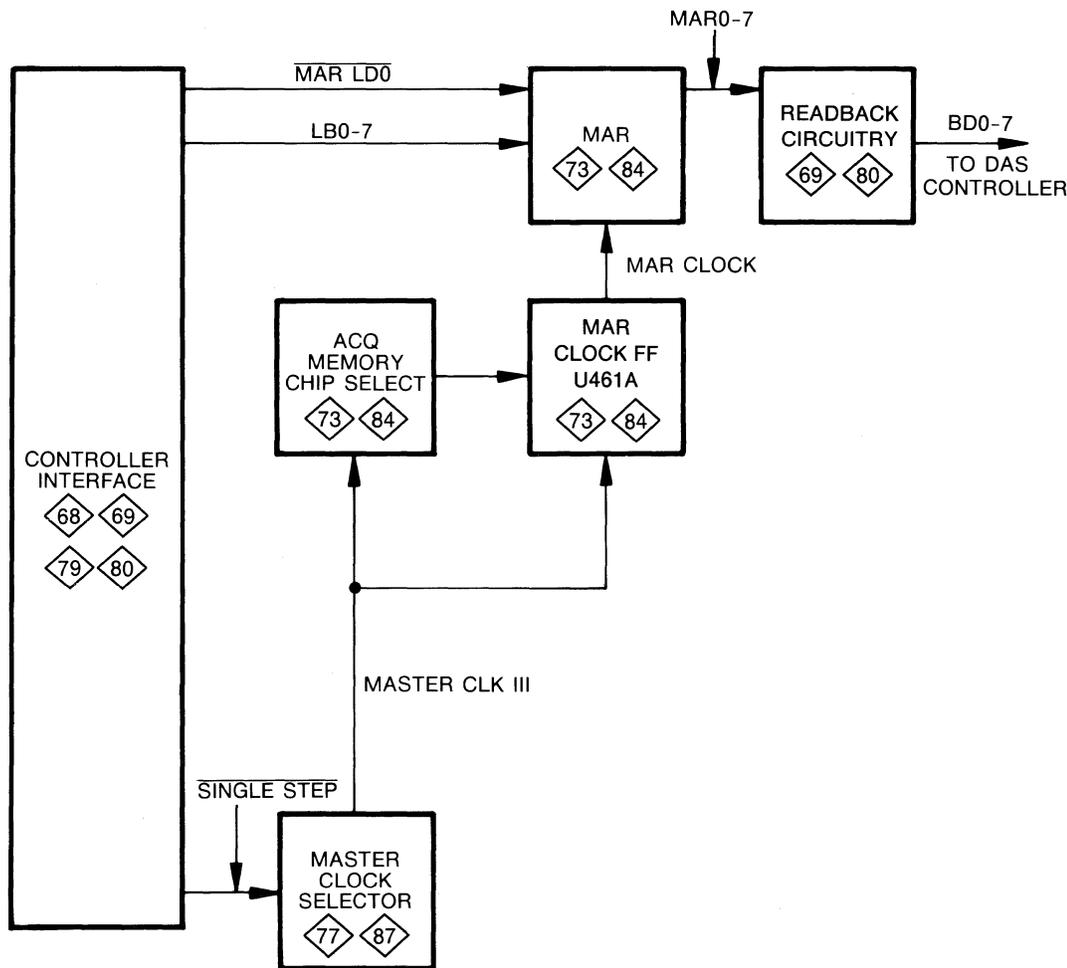
4541-702

Figure 7-6. Blocks of the 91A24 tested by the MEM ADDR function, test 0.

MEM ADDR test 0 walks a high bit (1) through the low byte of the memory address register (see Table 7-3 for values). The high bit is walked from bit 7 down to bit 0. After loading each bit pattern, the MAR is verified for the correct pattern. If an incorrect result is read during any of the eight passes, the test stops and no other passes are made.

Test 0 Readback Port

All test 0 results are read through U135 (port 03) on 91A24 schematic 69 or 91AE24 schematic 80.

Test 0 Initial Conditions

The DAS sets the first four initial conditions outside of the test loop. So when the test is looping, these events occur only once before the loop is entered and never happen again. Watching for these events with an oscilloscope is not advised.

1. On the 91A24, registers U928, U931, U935, U938, U941, and U945 (on schematic 77) are initialized with 00 through PC0-PC5.

2. If a 91AE24 is being tested, registers U938, U941, and U945 (on schematic 87) are initialized with 00 through PC0-PC5.

3. 80_{16} is written onto D0-7, and U965 pin 8 (PC4 on 91A24 schematic 68 or 91AE24 schematic 79) is toggled low. This asserts U721 pin 5 (on schematic 77 or 87) high, selects the single-step clock to drive MASTER CLK III.

4. 20_{16} is written to U761 (on schematic 68 or 79), which sets U761 pin 16 (MEM RD) high. The high from U761 pin 16 goes through U198B (on schematic 74 or 85) and sets U288 pin 8 (MAR EN on schematic 74 or 85) low. This enables U461A (on schematic 73 or 84) to load the MAR.

Initial condition 5 is inside the test loop, so it can be observed with an oscilloscope.

5. $F7_{16}$ is written to U765 (on schematic 68 or 79). This sets U765 pin 2 ($\overline{\text{MAR LD0}}$) low, which sets U138 pin 9 and U238 pin 9 (on schematic 73 or 84) low, enabling loading of the low eight bits of the MAR.

Test 0 Run Sequence

This test takes eight passes to complete. During each pass, a different value is loaded into the MAR and read back. The values loaded during each pass are given in Table 7-2. For each of the eight passes:

1. The test value is first loaded into the MAR by setting U958 pin 10 ($\overline{\text{SINGLE STEP}}$ on schematic 68 or 79) low. This low passes through U721, Q543 and Q544 (on schematic 77 or 87) to produce MASTER CLK III on U461A pin 3 (schematic 73 or 84). MASTER CLK III produces MAR CLOCK, which clocks the test value on LB0-LB7 into U138 and U238 (on schematic 73 or 84).

2. The test value is read from the MAR onto the data bus through U135 (on schematic 69 or 80).

91A24 AND 91AE24 MEM ADDR TEST 1 TROUBLESHOOTING

Reading the Test 1 Error Codes

Test 1 of the 91A24 MEM ADDR function provides test results like those shown in Figure 7-7.
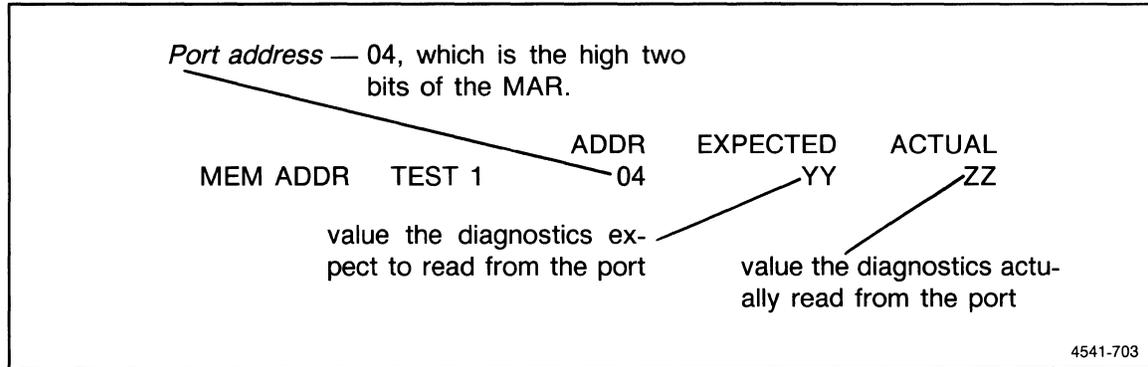
Figure 7-7. MEM ADDR test 1 readback display. The ACTUAL value is read from the high two bits of the MAR. The EXPECTED field may have any of the values shown in Table 7-3.

Table 7-3
EXPECTED DIAGNOSTIC READBACK VALUES FOR TEST 0

Pass	MAR Bit	Loaded and Expected Value
1	9	02
2	8	01

Error Indication:

```
                               ADDR    EXPECTED    ACTUAL
          MEM ADDR    TEST 1    04        YY          ZZ
```

Possible Cause	Action
CNTL3 malfunction.	Loop test 1. Check U965 pin 13 (on 91A24 schematic 68 or 91AE24 schematic 79) for low pulses; if none, suspect U965.
MAR LD1 malfunction.	While test 1 is still looping, check U765 pin 19 (on schematic 68 or 79) for low; if not low, suspect U765.
MAR counter malfunction.	Check for expected value on outputs of U438 (schematic 73 or 84); if values not present, suspect U438.
MAR HIGH malfunction.	Check U235 pin 1 (on schematic 69 or 80) for low pulses; if none, suspect U998 (on schematic 69 or 80). If low pulses are present, suspect U235.

91A24 AND 91AE24 MEM ADDR TEST 1 DESCRIPTION
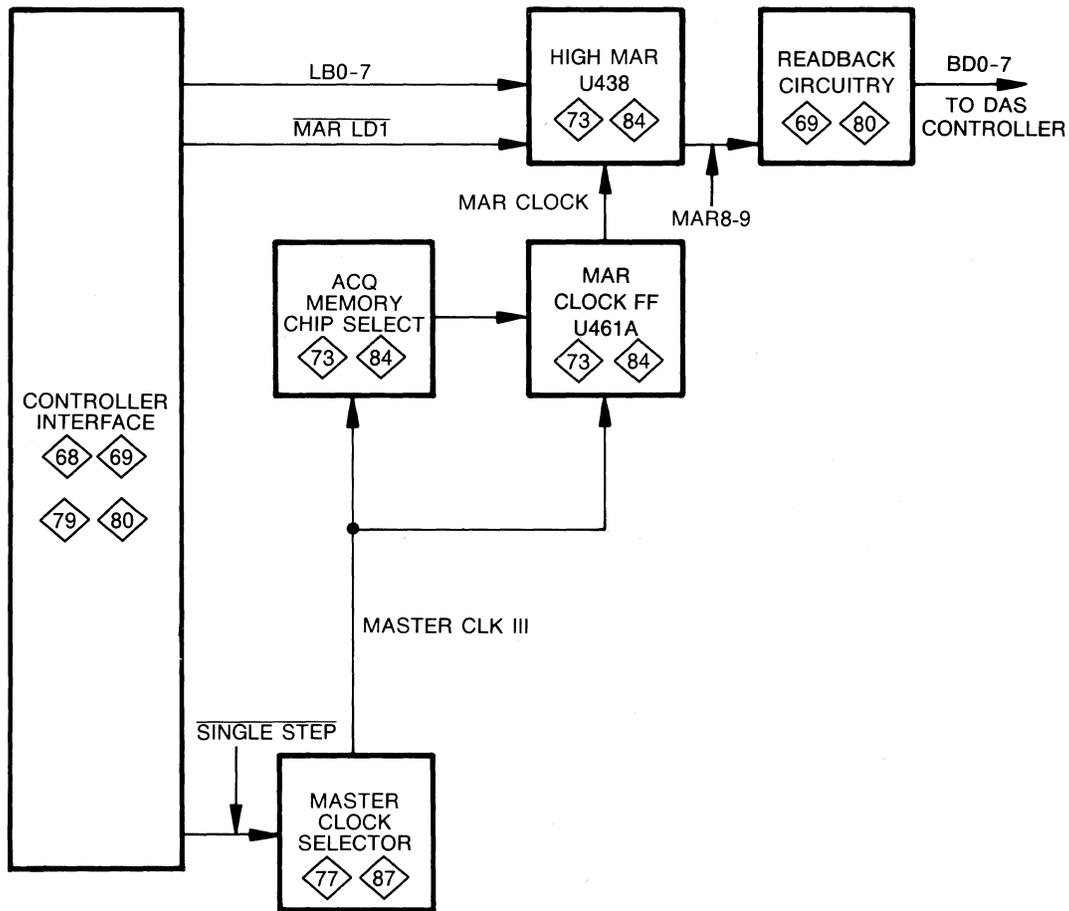
4541-704

Figure 7-8. Blocks of the 91A24 tested by the MEM ADDR function, test 1.

MEM ADDR test 1 walks a high bit (1) through the high two bits of the MAR (see Table 7-3 for values). The high bit is walked from bit 9 down to bit 8 (bit 1 down to bit 0 on U438 on 91A24 schematic 73 or 91AE24 schematic 84). After the system loads each pattern, the pattern is verified by reading U235 (schematic 69 or 80). If an error is detected on the first pass, the second pass is not made.

Test 1 Readback Port

Test 1 results are read through U235 (port 04) on 91A24 schematic 69 or 91AE24 schematic 80.

Test 1 Initial Conditions

The DAS sets the first four initial conditions before test 0 starts and never sets them again. The conditions remain true, however, and are necessary for test 1 to pass.

1. On the 91A24, registers U928, U931, U935, U938, U941, and U945 (on schematic 77) are initialized with 00_{16} through PC0-PC5.

2. If a 91AE24 is being tested, registers U938, U941, and U945 (on schematic 87) are initialized with 00_{16} through PC0-PC5.

3. 80_{16} is written onto D0-D7, and U965 pin 8 (PC4 on 91A24 schematic 68 or 91AE24 schematic 79) is toggled low. This asserts U721 pin 5 (on schematic 77 or 87), which selects the single-step clock to drive MASTER CLK III.

4. 20_{16} is written to U761 (on schematic 68 or 79), which sets U761 pin 16 (MEM RD) high. The high from U761 pin 16 goes through U198B (on schematic 74 or 85) and sets U288 pin 8 (MAR EN on schematic 74 or 85) low. This enables U461A (on schematic 73 or 84) to load the MAR.

Initial condition 5 is inside the test 1 loop, so it can be observed with an oscilloscope.

5. EF_{16} is written to U765 (on schematic 68 or 79). This sets U765 pin 19 ($\overline{MAR\ LD1}$) low, which sets U438 pin 9 (on schematic 73 or 84) low, enabling loading of the upper two bits of the MAR.

Test 1 Run Sequence

This test takes two passes to complete. During each pass, a different value is loaded into the MAR and read back. The values loaded during each pass are given in table 7-3. For each of the two passes:

1. The test value is first loaded into the MAR by setting U958 pin 10 ($\overline{SINGLE\ STEP}$ on schematic 68 or 79) low. This low passes through U721, Q543 and Q544 (on schematic 77 or 87) to produce MASTER CLK III on U461A pin 3 (schematic 73 or 84). MASTER CLK III produces MAR CLOCK, which clocks the test value on LB0 and LB1 into U438 (on schematic 73 or 84).

2. The test value is read from the MAR onto the data bus through U235 (on schematic 69 or 80).

91A24 AND 91AE24 MEM ADDR TEST 2 TROUBLESHOOTING

Reading the Test 2 Error Codes

Test 2 of the 91A24 MEM ADDR function provides test results like those shown in Figure 7-9.

Port address — 03 or 04, the low byte or high two bits of the MAR, respectively.

| | | ADDR | EXPECTED | ACTUAL |
| MEM ADDR | TEST 2 | XX | YY | ZZ |

value the diagnostics expect to read from the port

value the diagnostics actually read from the port

4541-705
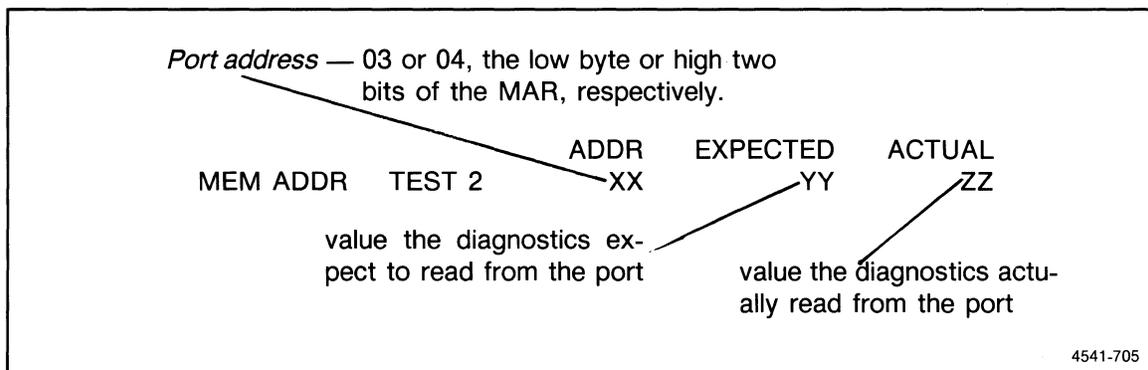
Figure 7-9. MEM ADDR test 2 readback display. The ACTUAL value is read from the MAR. The EXPECTED value depends on the port read. If port address 04 is read, the expected value may be 00-03. If port address 03 is read, the expected value may be 00-FF.

Error Indication

		ADDR 03	EXPECTED 01	ACTUAL 00
MEM ADDR	TEST 2			

Possible Cause	Action
CNTL3 malfunction.	Loop test 2. Check U765 pin 11 (on 91A24 schematic 68 or 91AE24 schematic 79) for low pulses; if none, suspect U965.
MAR LD0 malfunction.	While test 2 is still looping, check U765 pin 2 for high with low pulses; if present, suspect U138 (schematic 73 or 84); if none, suspect U765 (schematic 68 or 79).

Error Indication

		ADDR 03	EXPECTED 10	ACTUAL 0F
MEM ADDR	TEST 2			

Possible Cause	Action
MAR counter malfunction.	Check U238 pin 10 (91A24 schematic 73 or 91AE24 schematic 84) for high pulses; if present, suspect U238; if not present, suspect U138 (schematic 73 or 84).

Error Indication

		ADDR 04	EXPECTED 01	ACTUAL 00
MEM ADDR	TEST 2			

Possible Cause	Action
CNTL3 malfunction.	Loop test 2. Check U965 pin 13 (on 91A24 schematic 68 or 91AE24 schematic 79) for low pulses; if none, suspect U965.
MAR LD1 malfunction.	While test 2 is still looping, check U765 pin 19 (on schematic 68 or 79) for high with low pulses; if not present, suspect U765. If low pulses are present, suspect U438 (on schematic 73 or 84).
MAR counter malfunction.	Check U438 pin 10 (on schematic 73 or 84) for high pulses; if present, suspect U438; if not present, suspect U238 (on schematic 73 or 84).

Error Indication

		ADDR	EXPECTED	ACTUAL
MEM ADDR	TEST 2	XX	YY	ZZ

Possible Cause	Action
MAR counters malfunctioning.	If ADDR field says 04, then suspect U438 (on 91A24 schematic 73 or 91AE24 schematic 84). If ADDR field says 03 and EXPECTED is greater than $0F_{16}$ then suspect U238 (on schematic 73 or 84). Otherwise suspect U138 (on schematic 73 or 84).

91A24 AND 91AE24 MEM ADDR TEST 2 DESCRIPTION
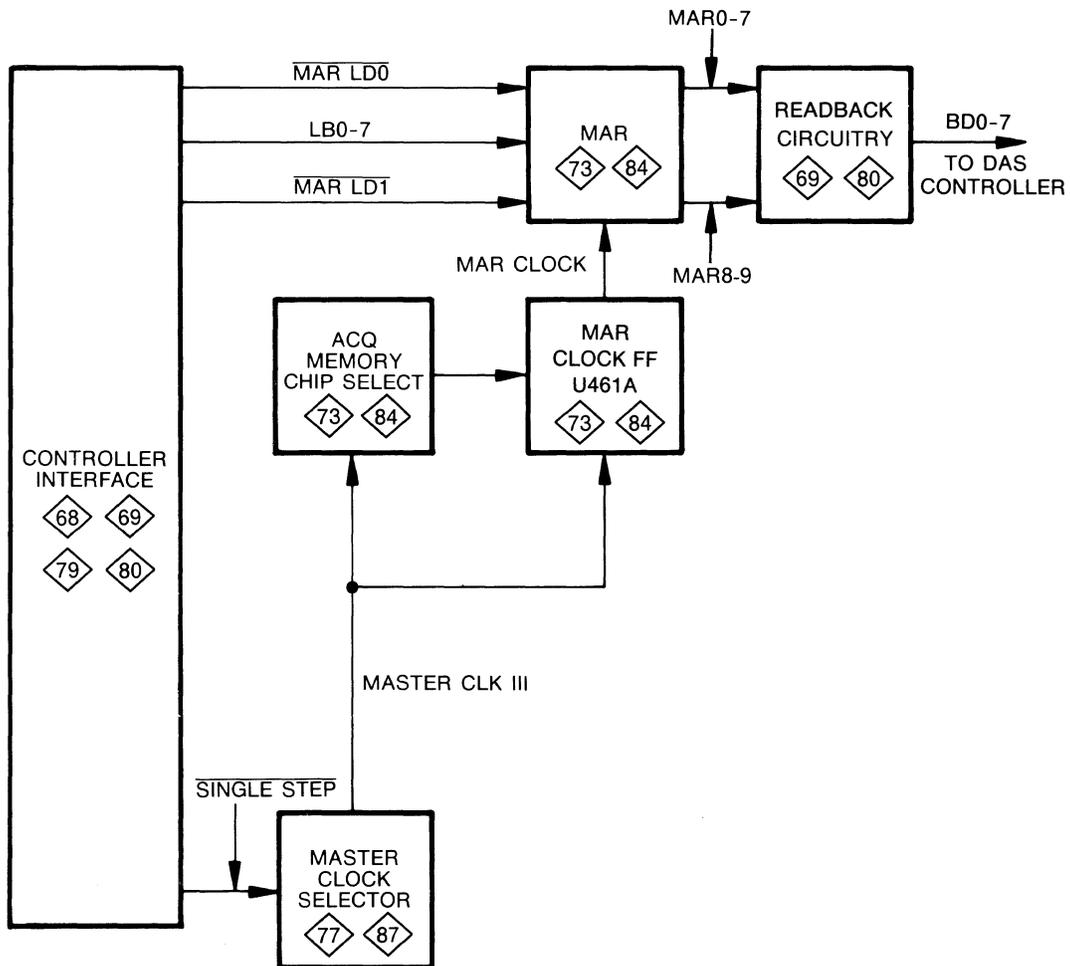
4541-706

Figure 7-10. Blocks of the 91A24 tested by the MEM ADDR function, test 2.

MEM ADDR test 2 loads the MAR with 000_{16} and then single-steps it to $3FF_{16}$. After each step, the MAR is read to verify that it contains the correct count. If an incorrect count is detected, the test stops.

Test 2 is also run on power-up, where it loads the MAR with 0's and then single-steps the MAR to 0F.

NOTE

In this test, the MAR is read back in two parts: the low byte of the MAR first, followed by the two highest bits. If a failure occurs, the part that failed can be determined by the I/O port address that is displayed. 03 corresponds to the low byte of the MAR and 04 to the two highest MAR bits. On each pass both parts are read, but if an error is detected on the low byte of the MAR, the high MAR result is not displayed.

Test 2 Readback Port

The low MAR (MAR0-MAR7) results are read through U135 (port 03 on 91A24 schematic 69 or 91AE24 schematic 80), and the high MAR (MAR8 and MAR9) results are read through U235 (port 04 on 91A24 schematic 69 or 91AE24 schematic 80).

Test 2 Initial Conditions

The DAS sets the first four initial conditions before test 0 starts and never sets them again. The conditions remain true, however, and are necessary for test 2 to pass.

1. On the 91A24, registers U928, U931, U935, U938, U941, and U945 (on schematic 77) are initialized with 00_{16} through PC0-PC5.

2. If a 91AE24 is being tested, registers U938, U941, and U945 (on schematic 87) are initialized with 00_{16} through PC0-PC5.

3. 80_{16} is written onto D0-D7, and U965 pin 8 (PC4 on 91A24 schematic 68 or 91AE24 schematic 79) is toggled low. This asserts U721 pin 5 (on schematic 77 or 87), which selects the single-step clock to drive MASTER CLK III.

4. 20_{16} is written to U761 (on schematic 68 or 79), which sets U761 pin 16 (MEM RD) high. The high from U761 pin 16 goes through U198B (on schematic 74 or 85) and sets U288 pin 8 (MAR EN on schematic 74 or 85) low. This enables U461A (on schematic 73 or 84) to load the MAR.

Initial conditions 5 through 9 are inside the test 2 loop, so they can be observed with an oscilloscope. To finish the set up for test 2, the MAR is loaded with 000_{16}, as described below.

5. $F7_{16}$ is written to U765 (91A24 schematic 68 or 91AE24 schematic 79). This sets U765 pin 19 ($\overline{\text{MAR LD0}}$ on schematic 68 or 79) low. This low is transmitted to U138 pin 9 and U238 pin 9 (on schematic 73 or 84), and enables loading the low eight bits of the MAR.

6. 00_{16} is written to U958 pin 10 ($\overline{\text{SINGLE STEP}}$ on schematic 68 or 79) which clocks a low into the low MAR (MAR0-MAR7) through U461A (on schematic 73 or 84).

7. EF_{16} is written to U765 (schematic 68 or 79). This sets U765 pin 2 ($\overline{\text{MAR LD1}}$) low. This low is transmitted to U438 pin 9 (on schematic 73 or 84) to enable loading the high two bits of the MAR (MAR8, MAR9).

8. 00_{16} is written to U958 pin 10 ($\overline{\text{SINGLE STEP}}$ on schematic 68 or 79) which clocks 0s into U438 (MAR8, MAR9 on schematic 73 or 84) through U461A (on schematic 73 or 84).

9. FF_{16} is written to U765 (on schematic 68 or 79). This sets $\overline{\text{MAR LD0}}$ and $\overline{\text{MAR LD1}}$ high at U765 pins 2 and 19, and at pin 9 of U138, U238, and U438 (on schematic 73 or 84). This allows the MAR to increment.

Test 2 Run Sequence

The MAR is clocked from 000_{16} to $3FF_{16}$ as follows:

1. U958 pin 10 ($\overline{\text{SINGLE STEP}}$ on 91A24 schematic 68 or 91AE24 schematic 79) is written low. This, in turn produces MAR CLOCK from U461A (on schematic 73 or 84) which increments the MAR (U138, U238, and U438 on schematic 73 or 84).

2. After each clock, both high and low MAR are read for the correct data. The low MAR is read from U135 (on schematic 69 or 80) enabled by U998 pin 4 ($\overline{\text{MAR LOW}}$ on schematic 69 or 80), and the high MAR is read from U235 (on schematic 69 or 80) enabled by U998 pin 5 ($\overline{\text{MAR HIGH}}$ on schematic 69 or 80).

91A24 AND 91AE24 MEM ADDR TEST 3 TROUBLESHOOTING

Reading the Test 3 Error Codes

Test 3 of the 91A24 MEM ADDR function provides test results like those shown in Figure 7-11.
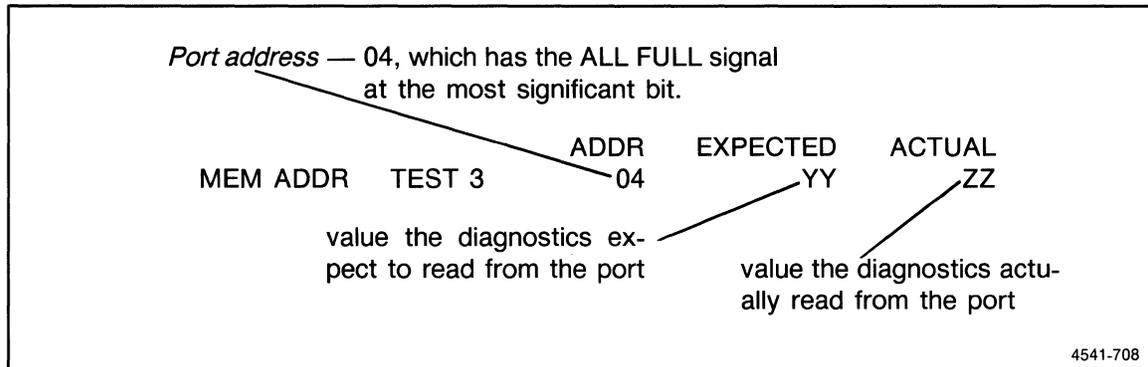
Figure 7-11. **MEM ADDR test 3 readback display.** The ACTUAL value is read from the ALL FULL flip-flop. The EXPECTED value depends on when the port is read. 00 indicates that the ALL FULL bit is low, and 80 indicates that the ALL FULL bit is high (set).

Error Indication

		ADDR	EXPECTED	ACTUAL
MEM ADDR	TEST 3	04	00	80

Possible Cause	Action
ALL FULL flip-flop (U461B) malfunction.	Loop test 3. Check U461B pin 8 (on 91A24 schematic 73 or 91AE24 schematic 84) for low; if not low, suspect U461. If U461B pin 8 is low, suspect U235 (on schematic 69 or 80).

Error Indication

		ADDR	EXPECTED	ACTUAL
		04	80	00
MEM ADDR	TEST 3			

Possible Cause	Action
MAR circuitry malfunction.	Loop test 3. Check U438 pins 5 and 6 (on 91A24 schematic 73 or 91AE24 schematic 84) for high; if not high, suspect R536 (on schematic 73 or 84). If U438 pins 5 and 6 are high, check U468B pin 3 (on schematic for 73 or 84) for low pulses; if none, suspect U438. If there are low pulses, check U468B pin 4 for high pulses; if present, suspect U461 (on schematic 73 or 84); if not present, suspect U468 (on schematic 73 or 84).

91A24 AND 91AE24 MEM ADDR TEST 3 DESCRIPTION
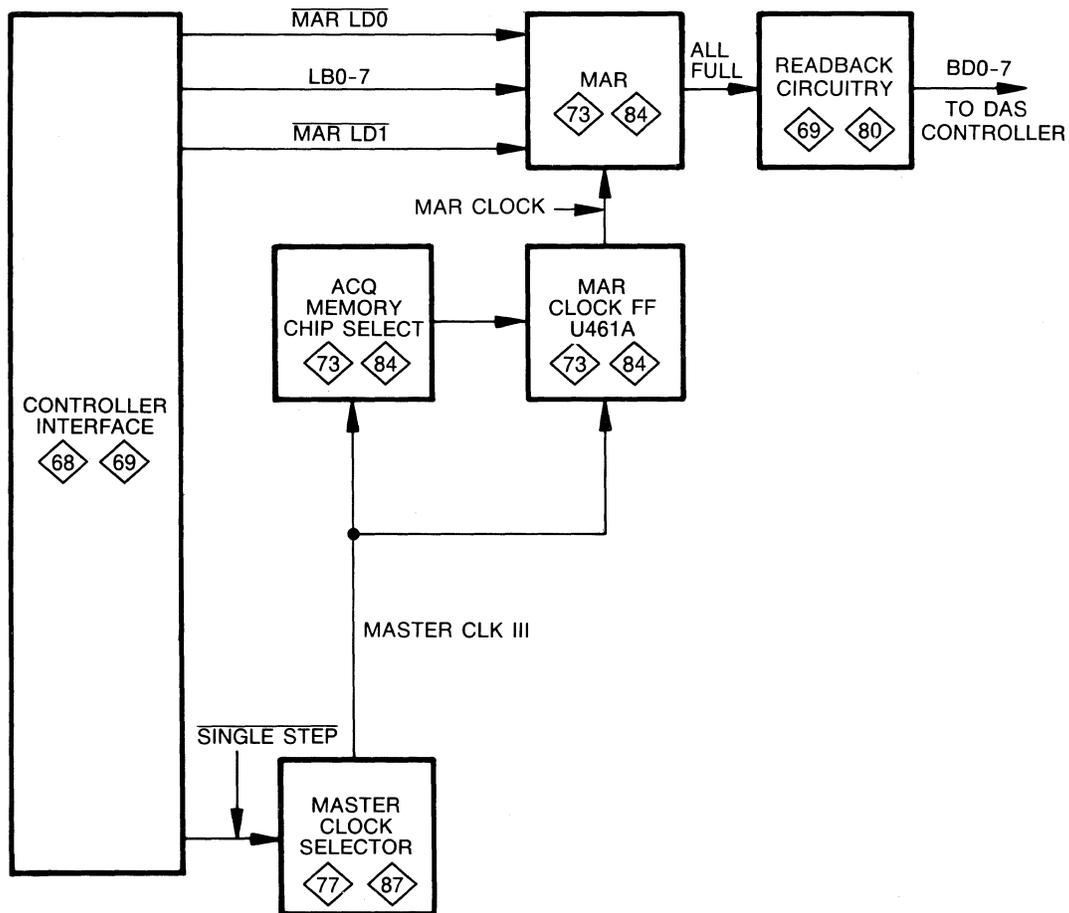
4541-709

Figure 7-12. Blocks of the 91A24 tested by the MEM ADDR function, test 3.

This test loads the MAR with $3FF_{16}$, checks to see that the ALL FULL signal is low, then single-steps the MAR to set the ALL FULL signal high. The ALL FULL signal is read through U235 (bit 7) (shown on 91A24 schematic 69 or 91AE24 schematic 80).

Test 3 Readback Port

Test 3 results are read through U235 (port 04) on 91A24 schematic 69 or 91AE24 schematic 80.

Test 3 Initial Conditions

The DAS sets the first four initial conditions before test 0 starts and never sets them again. The conditions remain true, however, and are necessary for test 3 to pass.

1. On the 91A24, registers U928, U931, U935, U938, U941, and U945 (on schematic 77) are initialized with 00_{16} through PC0-PC5.

2. If a 91AE24 is being tested, registers U938, U941, and U945 (on schematic 87) are initialized with 00_{16} through PC0-PC5.

3. 80_{16} is written onto D0-D7, and U965 pin 8 (PC4 on 91A24 schematic 68 or 91AE24 schematic 79) is toggled low. This asserts U721 pin 5 (on schematic 77 or 87), which selects the single-step clock to drive MASTER CLK III.

4. 20_{16} is written to U761 (on schematic 68 or 79), which sets U761 pin 16 (MEM RD) high. The high from U761 pin 16 goes through U198B (on schematic 74 or 85) and sets U288 pin 8 (MAR EN on schematic 74 or 85) low. This enables U461A (on schematic 73 or 84) to load the MAR.

Initial conditions 5 and 6 are inside the test 1 loop, so they can be observed with an oscilloscope. These steps load the MAR with $3FF_{16}$ as follows:

5. $\overline{\text{MAR LD0}}$ is asserted (low), and the low byte of the MAR (U138 and U238 on schematic 73 or 84) is loaded with FF. $\overline{\text{MAR LD0}}$ is applied to U461B pin 10 (on schematic 73 or 84), which makes U461B pin 8 (ALL FULL) low.

6. The high two bits of the MAR (MAR8 and MAR9) is loaded with 3_{16}. All 10 bits of the MAR are now set to $3FF_{16}$. (This sets the MAR to FFF_{16}. The MAR is actually a 12 bit counter, with the two most significant bits set high. The most significant bits, U438 pins 5 and 6, are hard-wired high). So writing $3FF_{16}$ to the MAR sets the MAR to FFF_{16}.

Test 3 Run Sequence

1. U998 pin 5 ($\overline{\text{MAR HIGH}}$ on 91A24 schematic 69 or 91AE24 schematic 80) enables U235 (on schematic 69 or 80). U235 is read to see if the ALL FULL signals is low. If ALL FULL is high, the test fails.

2. The MAR is clocked once by writing to U958 pin 10 ($\overline{\text{SINGLE STEP}}$ on schematic 68 or 79). This clocks the MAR to 000_{16}, making U438 pin 11 low (on schematic 73 or 84). The signal from U438 pin 11 is inverted by U468B and clocks U461B, which sets U461 pin 8 (ALL FULL) high (also on schematic 73 or 84).

3. The status of the ALL FULL bit is read through U235 (on schematic 68 or 79).

91A24 FUNCTION 2 ACQ MEM
91AE24 FUNCTION 1 ACQ MEM

CIRCUIT OVERVIEW

The ACQ MEM function tests the 91A24 and 91AE24 acquisition memory. The acquisition memory consists of six 1024 $\times$ 4 bit RAMs for a total of 1024 words by 24 bits. For a more detailed treatment of the acquisition memory, see the *Theory of Operation* section.

FUNCTION DESCRIPTION

The acquisition memory RAM is loaded from the test bus (LB0-LB7) and read one byte (eight bits) at a time. A 24-bit word is assembled in the system data login registers (on 91A24 schematic 72 or 91AE24 schematic 83) using the $\overline{\text{SINGLE STEP TTL}}$ clock, and then written into the RAM by the master clock.

The ACQ MEM function consists of two separate tests:

Test 0 exercises the inputs and outputs of the acquisition memory data registers and RAM. Test 0 also verifies pod independence and checks the write enable and memory read logic.

Test 1 checks the acquisition memory RAM for address and bit independence.

Loading the Data

Loading the system data login registers (on 91A24 schematic 72 or 91AE24 schematic 83) and MAR (memory address register on schematic 73 or 84) involves writing data onto BD0-BD7 in the controller interface (schematic 68 or 79). BD0-BD7 are buffered first by U768 then by U561 and U565 (all on schematic 68 or 79) to provide LB0-LB7. LB0-LB7 transmits data to the system data login registers (U125, U225, and U425 on schematic 72 or 83) and to the MAR (on schematic 73 or 84). The system data login outputs LID0-LID23 are loaded into the acquisition memory data registers by MASTER CLK II and into the acquisition memory RAM by MASTER CLK III and $\overline{\text{WEA--}}$ $\overline{\text{WEC}}$.

Readback Ports

Test results are read through memory readback ports 0B (U131), 0C (U231), and 0D (U431 on 91A24 schematic 69 or 91AE24 schematic 80). Port 0B transmits data from pod A memory. Port 0C transmits data from pod B memory. Port 0D transmits data from pod C memory.

91A24 AND 91AE24 ACQ MEM TEST 0 TROUBLESHOOTING

Reading the Test 0 Error Codes

Test 0 of the 91A24 ACQ MEM function provides test results like those shown in Figure 7-13.
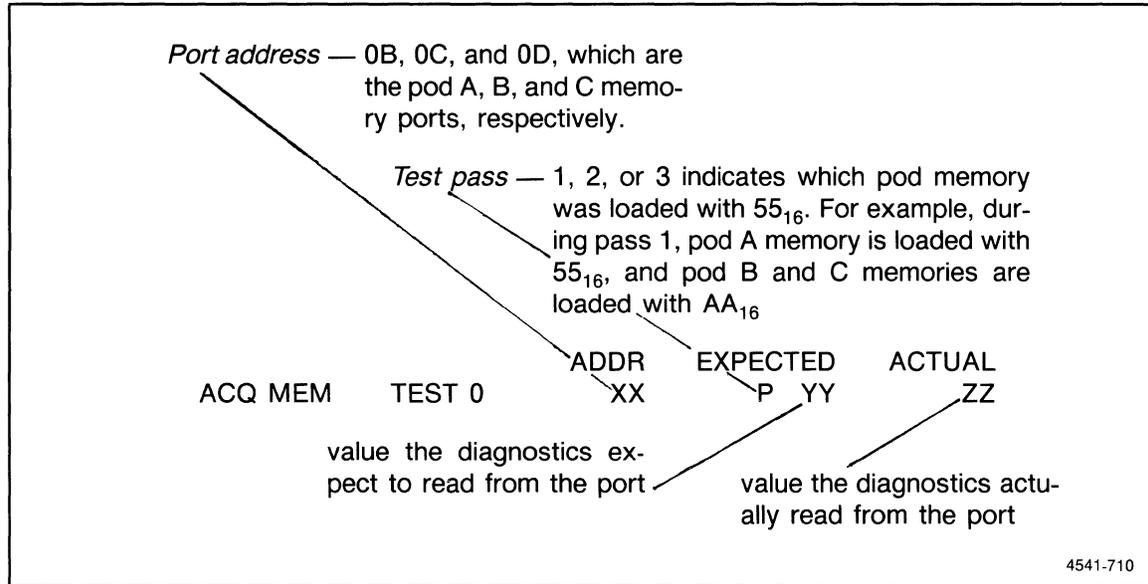
Figure 7-13. **ACQ MEM test 0 readback display.** The ACTUAL value is read from one of the acquisition RAMs, indicated by the port number. The EXPECTED field may show either 55 or AA, depending on the test pass and the port read back.

Error Indication

ACQ MEM function fails along with CNTR TIMR or MEM ADDR functions.

Possible Cause	Action
Circuits required by the ACQ MEM function are malfunctioning.	Debug according to the failed function with the smallest number.

Error Indication

		ADDR	EXPECTED	ACTUAL
ACQ MEM	TEST 0	XX	AA or 55	55 or AA

Possible Cause	Action
Write enable malfunction.	Check U765 pins 5, 6, and 9 (on schematic 68 or 79) for low pulses; if any do not pulse low, suspect U765.
Acquisition memory readback malfunction.	Loop test 0. Check U998 pins 13, 14, and 15 (91A24 schematic 69 or 91AE24 schematic 80) for port address signals as follows: • Low pulses on U998 pin 13 verifies port address 0B. • Low pulses on U998 pin 14 verifies port address 0C. • Low pulses on U998 pin 15 verifies port address 0D. If any of U998 pins 13, 14 or 15 do not show low pulses, suspect U998.
CNTL3 malfunction.	While the test is still looping, check U965 pin 13 (on schematic 68 or 79) for low pulses; if none, suspect U965.

Error Indication

		ADDR	EXPECTED	ACTUAL
ACQ MEM	TEST 0	XX	AA or 55	$\underbrace{\text{XX}}$
				Not AA or 55

Possible Cause	Action
Diagnostic enable malfunction.	Loop test 0. Check U758 pins 16, 12, and 15 (on schematic 68 or 79) for steady low. If any pin is not low, suspect U758.
System data login register malfunction.	With test 0 still looping, check the outputs of the following registers (on schematic 72 or 83) for AA_{16} or 55_{16} outputs. • Check U125 output for AA or 55; • Check U225 output for AA or 55; • Check U425 output for AA or 55. If any of these registers do not output AA or 55, suspect that chip.
Readback buffer or RAM malfunction.	With a logic analyzer, acquire the outputs of each of the acquisition memory readback registers (U131, U231, and U431 on schematic 69 or 80). Use pin 1 or 19 of each register to clock the analyzer. If any chip does not output AA_{16} or 55_{16} suspect that chip. With a logic analyzer, acquire the inputs of each of the acquisition memory readback registers (U131, U231, and U431 on schematic 69 or 80). Use pin 1 or 19 of each register to clock the analyzer. If any chip is not receiving AA_{16} or 55_{16}, suspect the RAM that is supplying the input (the RAM is shown on schematic 73 or 84). If the inputs are all AA_{16} or 55_{16}, suspect the readback register the data is acquired from.

91A24 AND 91AE24 ACQ MEM TEST 0 DESCRIPTION
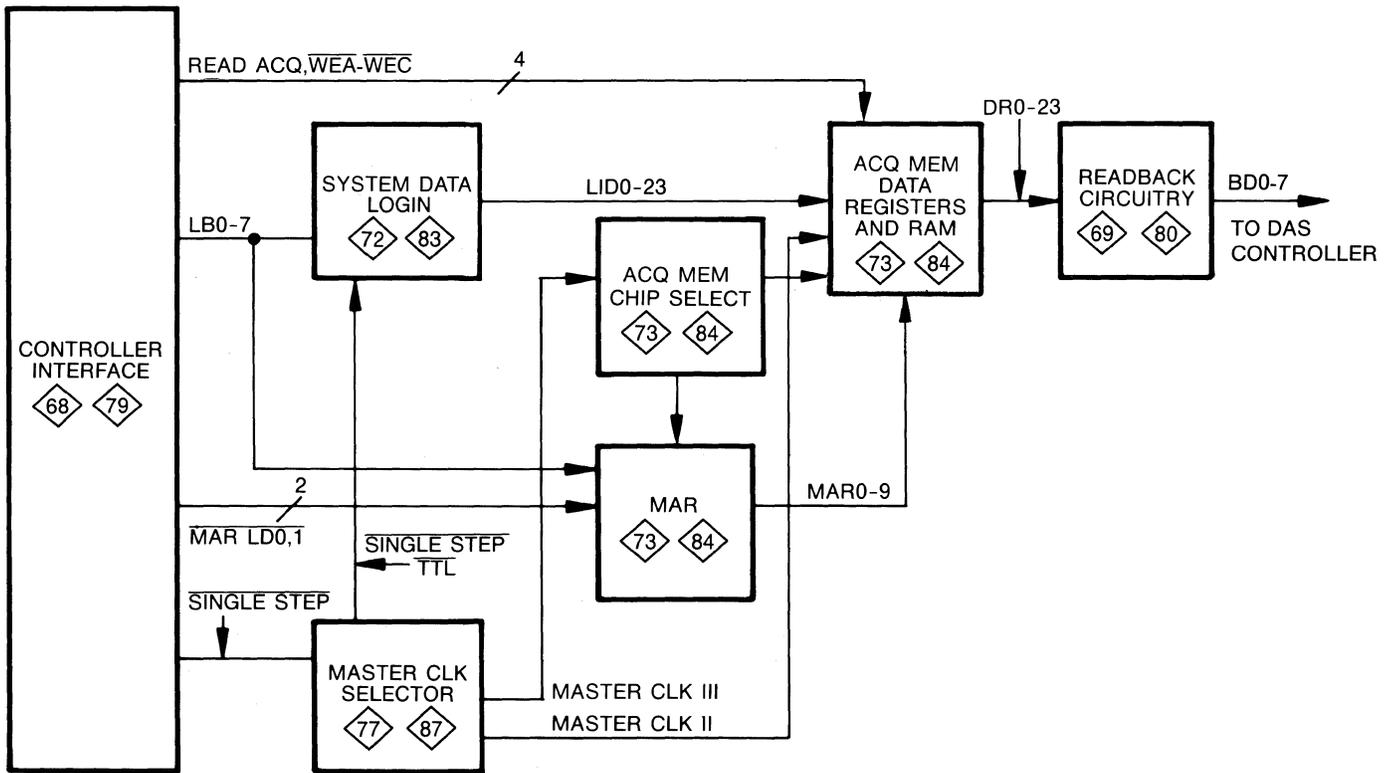
4541-711

Figure 7-14. Blocks of the 91A24 tested by the ACQ MEM function, test 0.

ACQ MEM test 0 checks the write enable and the read logic on the module. This is done in three passes. On each pass two of the three bytes of the acquisition memory at location 000_{16} are filled with AA_{16} and the third is written with 55_{16}. The byte that receives 55 is determined by the pass.

- On the first pass the low byte (RAMs U141 and U145 on 91A24 schematic 73 or 91AE24 schematic 84) is written with 55_{16}.

- On the second pass the middle byte (RAMs U241 and U245 on schematic 73 or 84) is written with 55_{16}.

- On the third pass the high byte (RAMs U441 and U445 on schematic 73 or 84) is written with 55_{16}.

After each pass, all three bytes are read and compared to the value loaded. If an error is detected, the test stops with that pass.

Table 7-4 shows the expected RAM contents after each pass.

Table 7-4
EXPECTED RAM CONTENTS AFTER EACH ACQ MEM TEST 0 PASS

| Pass | Memory Content | | |
	Pod A Read Port 0B	Pod B Read Port 0C	Pod C Read Port 0D
1	55	AA	AA
2	AA	55	AA
3	AA	AA	55

Test 0 Readback Port

Test 0 results are read through U131 (port 0B), U231 (port 0C), and U431 (port 0D) on 91A24 schematic 69 or 91AE24 schematic 80.

Test 0 Initial Conditions

Before this test runs, the following setup is performed:

1. 20_{16} is written to U761 (on schematic 68 or 79). This sets U761 pin 16 (MEM RD) high. The high from MEM RD sets U461A pin 2 ($\overline{\text{MAR EN}}$ on schematic 73 or 84) low (through U198B and U288 on schematic 74 or 85), which enables loading the memory address register (MAR).

2. $0B_{16}$ is written to U758 (on schematic 68 or 79), setting U758 pins 16, 12, and 15 (A, B, and C DIAG EN on schematic 68 or 79) low. These lows enable the system data login registers (U125, U225, and U425 on schematic 72 or 83). This also disables the run-time login registers (U121, U118, U221, and U421 on schematic 72 or 83).

3. 80_{16} is written onto D0-D7, and U965 pin 8 (PC4 on schematic 68 or 79) is asserted. This asserts U721 pin 5 (on schematic 77 or 87) and connects MASTER CLK III to $\overline{\text{SINGLE STEP}}$. This clock will load the MAR and clock data into the acquisition memory.

4. The MAR is loaded with 000_{16}.

    a. $F7_{16}$ is written to U765 (on schematic 68 or 79). This makes U765 pin 2 ($\overline{\text{MAR LD0}}$) low. $\overline{\text{MAR LD0}}$ low asserts U138 pin 9 and U238 pin 9 (on schematic 73 or 84), to enable loading the low 8 bits of the MAR.

    b. 00_{16} is written to U958 pin 10 ($\overline{\text{SINGLE STEP}}$ on schematic 68 or 79) which clocks 0's into U138, U238 (the low byte of the MAR on schematic 73 or 84) through U461A (on schematic 73 or 84).

    c. EF_{16} is written to U765 (on schematic 68 or 79), which makes U765 pin 19 ($\overline{\text{MAR LD1}}$) low. The low $\overline{\text{MAR LD1}}$ goes to U438 pin 9 (on schematic 73 or 84) to enable loading the high 2 bits of the MAR.

    d. 00_{16} is written to U958 pin 10 ($\overline{\text{SINGLE STEP}}$ on schemtic 68 or 79) which clocks 0_{16} into U438 (the two high MAR bits on schematic 73 or 84) through U461A (on schematic 73 or 84).

Test 0 Run Sequence

1. On all 91A24 and 91AE24 modules in the mainframe, 10_{16} is written to U761 (on schematic 68 or 79). This makes U761 pin 6 (READ ACQ) and U761 pin 16 (MEM RD) low. READ ACQ being low enables the acquisition memory RAMs (U141, U145, U241, U245, U441, and U445 on schematic 73 or 84) to store the data from acquisition memory data registers U128, U228, and U428 (on schematic 72 or 83).

   MEM RD being low, along with TN0-TN2 being set low in initial condition 4a, sets U461A pin 2 ($\overline{\text{MAR EN}}$ on schematics 73 and 84) high to prevent the MAR from incrementing during this test.

3. For each of the three passes (1, 2, or 3), a value is written to U765 (on schematic 68 or 79). This value sets one of the acquisition RAM write enable bits low (active), and the others high. The low bit is $\overline{\text{WEA}}$ for pass 1, $\overline{\text{WEB}}$ for pass 2, and $\overline{\text{WEC}}$ for pass 3.

4. 55_{16} is written onto LB0-LB7 and U958 pin 10 ($\overline{\text{SINGLE STEP}}$) is asserted three times. In this way, 55_{16} is clocked through the three system data login registers (U125, U225, and U425 on schematic 72 or 83), and into the acquisition memory data registers (U128, U228, and U428 on schematic 73 or 84).

   On each write, the $\overline{\text{SINGLE STEP}}$ clock produces MASTER CLK III. Each MASTER CLK III rising edge produces a low from U578A pin 3 (on schematic 73 or 84) to the chip select inputs, pin 8 of acquisition memory RAMs (U141, U145, U241, U245, U441, and U445 on schematic 73 or 84). This low causes the data output by the data registers (U128, U228, and U448 on schematic 73 or 84) to be stored in the acquisition memory RAMs if their write enables (WEA(L), WEB(L), and WEC(L)) are low.

5. A value is written to U765 (on schematic 68 or 79), which makes the previously low $\overline{\text{WE}}$ signal high, and the other two $\overline{\text{WE}}$ signals low. In pass 1 $\overline{\text{WEB}}$ and $\overline{\text{WEC}}$ are enabled (low). In pass 2 $\overline{\text{WEA}}$ and $\overline{\text{WEC}}$ are enabled. In pass 3 $\overline{\text{WEA}}$ and $\overline{\text{WEB}}$ are enabled.

6. AA_{16} is written onto D0-D7, and U958 pin 10 ($\overline{\text{SINGLE STEP}}$ on schematic 68 or 79) is asserted three times. This loads AA_{16} into the enabled acquisition RAMs.

7. $1F_{16}$ is written to U765 (on schematic 68 or 79), which makes U765 pins 6, 9, 5 ($\overline{\text{WEA}}$-$\overline{\text{WEC}}$) high. This stops the acquisition RAM from storing data.

8. 31_{16} is written to U761 (on schematic 68 or 79), which sets U761 pin 6 (READ ACQ) high. READ ACQ high disables the outputs from memory latches U128, U228, and U428 (on schematic 73 or 84).

   Asserting READ ACQ also enables writing data from the acquisition memory RAMs (U141, U145, U241, U245, U441, and U445 on schematic 73 or 84) to the memory readback ports (U131, U231, and U431 on schematic 69 or 80) by resetting U475B pin 6 low through U468D (on schematic 73 or 84).

9. At the end of each pass, the three bytes of stored data are read through the memory readback ports (U131, U231, and U431 on schematic 69 or 80) and checked for correctness.

91A24 AND 91AE24 ACQ MEM TEST 1 TROUBLESHOOTING

Reading the Test 1 Error Codes

Test 1 of the 91A24 ACQ MEM function provides test results like those shown in Figure 7-15.
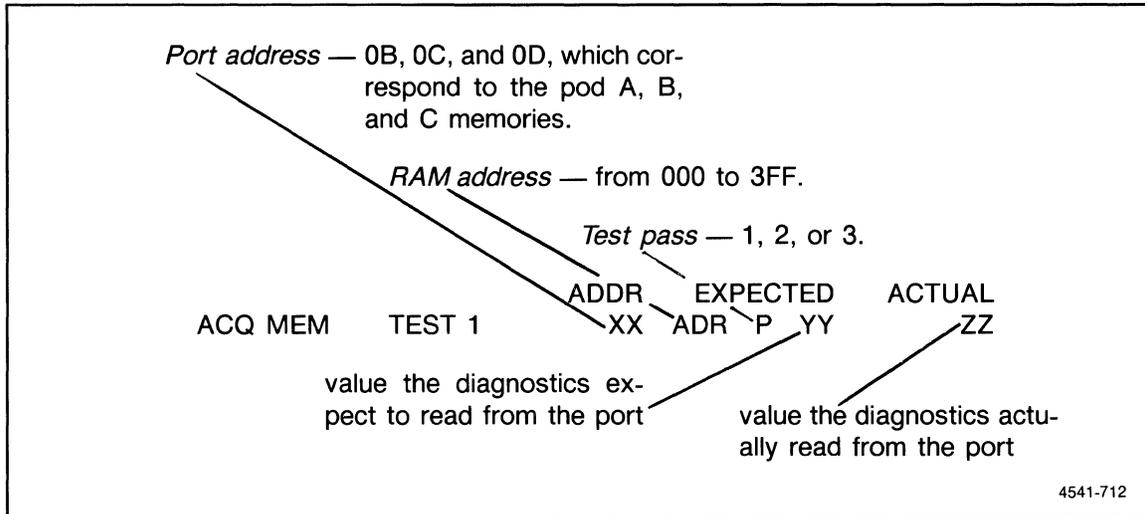
Figure 7-15. **ACQ MEM test 1 readback display.** The ACTUAL value is read from acquisitin RAM ports 0B, 0C, and 0D. The EXPECTED value may be CA, A1, or 1C.

Error Indication

		ADDR	EXPECTED	ACTUAL
ACQ MEM	TEST 1	0B	XXX 1 YY	ZZ

Possible Cause	Action
MAR address failure (MAR0-MAR9)	Turn looping off and run the ACQ MEM test. When test 1 stops, see if the A0-A9 inputs of U141 (on schematic 73 or 84) are equal to the failure RAM address plus 1 ($XXX_{16} + 1$) in the Diagnostics menu display. If inputs do not equal the failure location plus 1, trace signals to the MAR (U138, U238, and U438 on schematic 73 or 84) to locate the suspect device.

Error Indication

		ADDR	EXPECTED	ACTUAL
ACQ MEM	TEST 1	XX	XXX P YY	ZZ

Possible Cause	Action
Memory device malfunction.	Turn looping off and run the ACQ MEM test. If one digit of the ACTUAL value is incorrect, suspect the following devices: • With a failure at port 0B, suspect U141 for low four bits, or U145 for high four bits (on schematic 73 or 84). • With a failure at port 0C, suspect U241 for low four bits, or U245 for high four bits (on schematic 73 or 84). • With a failure at port OD, suspect U441 for low four bits, or U445 for high four bits (on schematic 73 or 84).

91A24 AND 91AE24 ACQ MEM TEST 1 DESCRIPTION
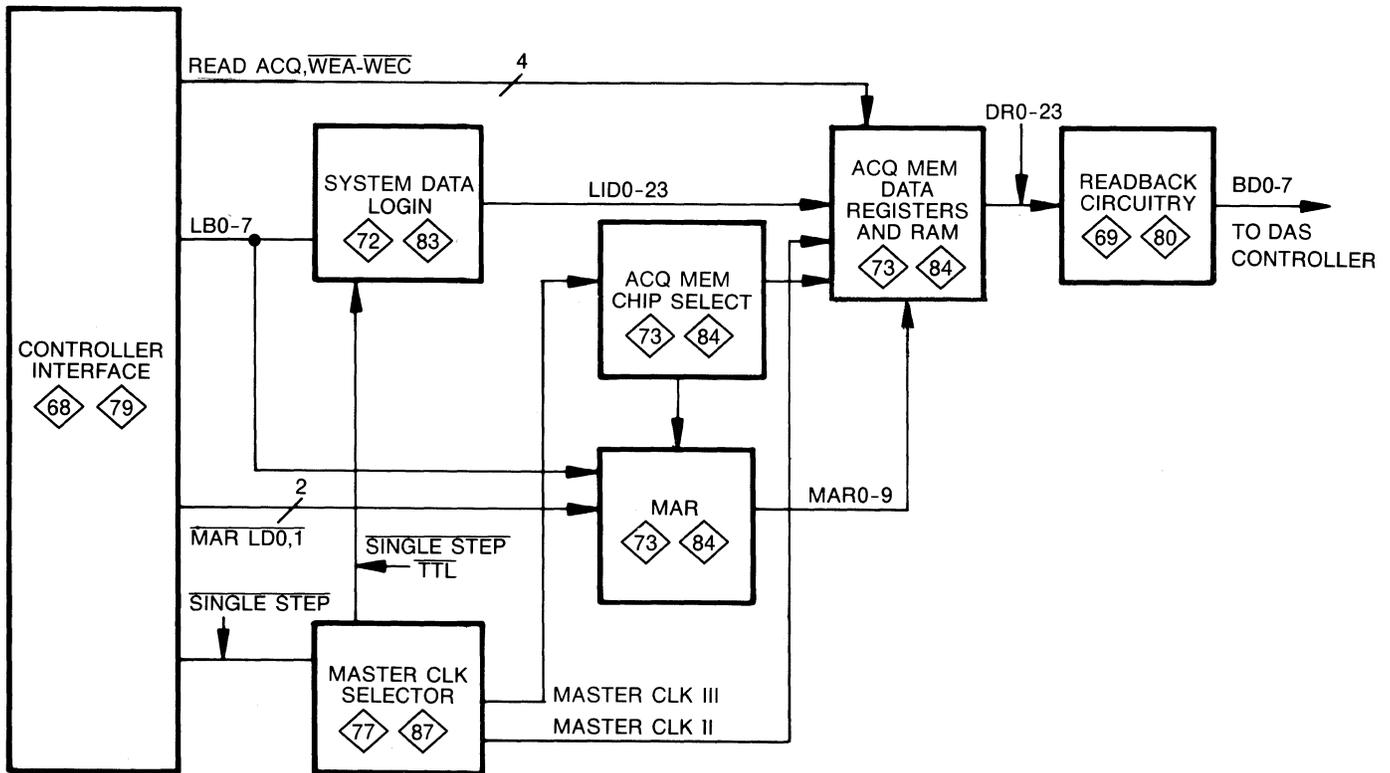
4541-714

Figure 7-16. Blocks of the 91A24 tested by the ACQ MEM function, test 1.

ACQ MEM test 1 checks for address and bit independence in the acquisition memory and associated readback and select logic. The test makes three passes and uses three different patterns. These patterns are CA, A1, and 1C, as shown in Table 7-5. Each memory location is loaded with CACACA, A1A1A1, or 1C1C1C. On each pass a different pattern is written to each location, so after three passes all three values have been loaded at each location. The three patterns used ensure bit independence and, since the patterns repeat in multiples of three, they ensure address independence.

With each pass the entire memory is filled, then read back to verify correctness. Also, since this test takes considerable time to execute, you can abort the test during readback by pressing the stop key.

This test also runs on power-up to test acquisition RAM addresses 000_{16} through 008_{16}. With each pass the first nine addresses are filled and then read to verify correctness. CA, A1, and 1C are written 11 times in sequence (nine locations tested plus two writes to get through the the login registers and the acquisition memory data registers). Table 7-5 shows the value loaded and expected for each pass.

Table 7-5
EXPECTED RAM VALUES FOR EACH ACQ MEM TEST 1 PASS

Memory Address	Expected Value		
	Pass 1	Pass 2	Pass 3
000	CACACA	A1A1A1	1C1C1C
001	A1A1A1	1C1C1C	CACACA
002	1C1C1C	CACACA	A1A1A1
003	CACACA	A1A1A1	1C1C1C
004	A1A1A1	1C1C1C	CACACA
...	...	...	...

Test 1 Readback Port

Test 1 results are read through U131 (port 0B), U231 (port 0C), and U431 (port 0D) on 91A24 schemtic 69 or 91AE24 schematic 80.

Test 1 Initial Conditions

These initial conditions are set as initial conditions for test 0. They remain true during test 1, however, and are necessary for test 1's execution. Since these initial conditions are not inside the loop, they cannot be observed with an oscilloscope.

1. $0B_{16}$ is written to U758 (on schematic 68 or 79), setting U758 pins 16, 12, and 15 (A, B, and C DIAG EN on schematic 68 or 79) low. These lows enable the system data login registers (U125, U225, and U425 on schematic 72 or 83). This also disables the run-time login registers (U121, U118, U221, and U421 on schematic 72 or 83).

2. 80_{16} is written onto D0-D7, and U965 pin 8 (PC4 on schematic 68 or 79) is asserted. This asserts U721 pin 5 (on schematic 77 or 87) and connects MASTER CLK III to $\overline{\text{SINGLE STEP}}$. This clock will load the MAR and clock data into the acquisition memory.

Test 1 Run Sequence

At the beginning of each pass, the acquisition memory is entirely filled with a pattern. The pattern loading is described in the next three steps.

1. 30_{16} is written to U761 (on 91A24 schematic 68 or 91AE24 schematic 79). This sets U761 pin 16 (MEM RD) high, and U461A pin 2 ($\overline{\text{MAR EN}}$ on schematic 73) low, so the MAR can increment while patterns are being stored.

2. The MAR is loaded with $3FE_{16}$ at the beginning of each pass. Storage begins at address 000_{16}. However, the MAR is loaded to 000 minus 2 to compensate for the pipeline effect of the login registers and acquisition memory data registers.

3. The write enables for all three pods ($\overline{\text{WEA}}$, $\overline{\text{WEB}}$, and $\overline{\text{WEC}}$, from U765 on schematic 68 or 79) are set low to enable storage in the RAM.

4. CA, A1, and 1C are written 1026_{10} times in sequence (1024 locations tested plus 2 writes for the pipeline). These patterns are written as in ACQ MEM Test 0, except that U461A pin 2 ($\overline{\text{MAR EN}}$ on schematic 73 or 84) is reset low and U461A pin 6 (MAR CLOCK on schematic 73 or 84) is asserted by MASTER CLK III, incrementing the MAR with each write.

When the entire address space of the RAM is filled, the contents of the memory are read and compared with the expected value. This read and compare sequence is described in steps 5-9.

5. The write enables for the acquisition memory ($\overline{\text{WEA}}$, $\overline{\text{WEB}}$, and $\overline{\text{WEC}}$, from U765 on schematic 68 or 79) are set high and the MAR is loaded with 000_{16}, which is the first location to be read.

6. 31_{16} is written to U761 (on schematic 68 or 79). This makes U761 pin 6 (READ ACQ) high, which disables the acquisition memory data registers, and resets U475B pin 6 ($\overline{\text{ACQ RAM SEL}}$ on schematic 73 or 84) low, which enables the acquisition memory RAMs to be read.

7. The location in RAM addressed by the MAR is read through U131, U231, and U431 (on schematic 69 or 80), and compared to the expected value. Ports U131, U231, and U431 are enabled by U998 pins 13, 14, and 15 ($\overline{\text{A MEM RD-C MEM RD}}$ on schematic 69 or 80).

8. If no error is detected, the DAS writes to port 09, which toggles the $\overline{\text{SINGLE STEP}}$ clock (U958 pin 10 on schematic 68 or 79) $\overline{\text{SINGLE STEP}}$ clocks U461A (on schematic 73 or 84) which causes the MAR to increment.

9. Steps 6-8 are repeated until all memory locations have been read. All the above procedures, both write and read phases, are repeated three times to complete the three passes.

91A24 FUNCTION 3 STK PNTR
91AE24 FUNCTION 2 STK PNTR

CIRCUIT OVERVIEW

The STK PNTR (stack pointer) function tests the 91A24 and 91AE24 stack pointer and stack control RAM. The stack pointer is a 4-bit counter (U571 on 91A24 schematic 76 or 91AE24 schematic 86) which provides part of the address for the sequential word recognizer. The stack control RAM is the 16 × 4-bit RAM (U555 on 91A24 schematic 75 or 91AE24 schematic 86) that is loaded with sequential word recognizer events, such as START TIMER and NEVER TRIGGER. For more information on these circuits, refer to the *Theory of Operation*.

FUNCTION DESCRIPTION

The STK PTR function consists of three separate tests.

Test 0 loads a walking-ones pattern into the stack pointer counter (U571 on 91A24 schematic 76 or 91AE24 schematic 86) and reads back the loaded values.

Test 1 loads test patterns into the stack control RAM (U555 on 91A24 schematic 75 or 91AE24 schematic 86). The patterns are read back and compared to the loaded values.

Test 2 clocks the stack pointer counter (U571 on schematic 76 or 86) to see if the counter will increment from 0_{16} to F_{16}.

Readback Ports

Test 0 and test 2 results are read through port 04 (U235 on schematic 69 or 80).

Test 1 results are read through port 0A (U785 on schematic 69 or 80).

91A24 AND 91AE24 STK PNTR TEST 0 TROUBLESHOOTING

Reading the Test 0 Error Codes

Test 0 of the STK PNTR function provides test results like those shown in Figure 7-17.
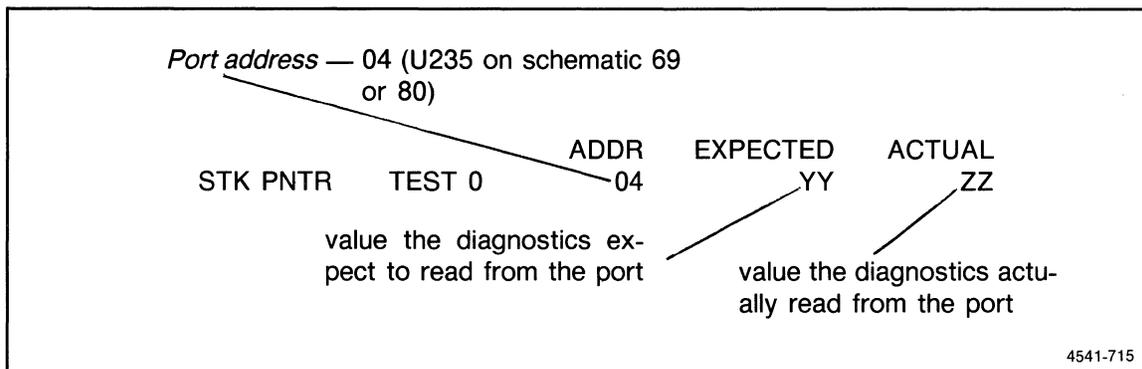
Figure 7-17. **STK PNTR test 0 readback display.** The ACTUAL value is read from the pointer. The EXPECTED value may be 20, 10, 08, or 04.

Error Indication

STK PNTR function fails along with CNTR TIMR, MEM ADDR, or ACQ MEM functions.

Possible Cause	Action
Circuits feeding into STK PNTR test are not functional.	Debug according to the failed function with the smallest number.

Error Indication: 91A24

STK PNTR test 0 fails on the 91A24.

Possible Cause	Action
If a 91AE24 is connected to the 91A24, the 91AE24 may cause the failure.	Turn off the DAS. Disconnect interconnect cables from J181 at the top of the 91A24 module. Turn on the DAS and re-run STK PTR test 0 on the 91A24 module. If the test fails with the cables disconnected, the 91A24 is at fault. If the test passes, suspect incorrectly installed interconnect cables or a 91AE24 module.

Error Indication: 91AE24

STK PNTR test 0 fails on the 91AE24.

Possible Cause	Action
Misconnected cables and staps on the 91AE24 may cause the failure.	Turn off the DAS. make sure cables and straps are properly connected to J181 of the 91AE24. Directions for these connections are located in the *Operating Instructions* section of this manual. I the test still fails after cable connections are verified, continue on to next possible cause.

Error Indication

STK PNTR	TEST 0	ADDR 04	EXPECTED 20	ACTUAL 00

Possible Cause	Action
STACK PTR LD not functional.	Loop test 0. Check U761 pin 19 (on schematic 68 or 79) for low; if not low, suspect U761.
STACK CLK EN not functional.	While still looping on test 0, check U758 pin 6 (on schematic 68 or 79) for low; if not low, suspect U758.
POINTER CLK not functional.	Check U575D pin 12 (on schematic 76 or 86) for steady low. If low, POINTER CLK is okay, go to next possible cause. If U575D not low, the 91A24 is at fault. On the 91A24, check U958 pin 9 (schematic 68) for a steady high; if not high, suspect U958. If U958 pin 9 is high, on the 91A24 check U265A both pins 1 and 3 (on schematic 75) for the same state. If pins 1 and 3 are not in the same state, suspect U265. If both pins are in the same state, suspect 91A24 U165 (on schematic 75).
STACK PTR CLK not functional.	Check U958 pin 15 (on schematic 68 or 79) for low pulses; if none, suspect U958. If low pulses present, check U568C pin 8 (schematic 76 or 86) for high pulses; if none, suspect U568. If high pulses present, check U485A pin 1 (schematic 76 or 86) for low pulses; if none, suspect U485. If low pulses present, check U575D pin 11 (on schematic 76 or 86) for low pulses; if none, suspect U575.
Stack pointer malfunction.	Check U571 pin 1 (on schematic 76 or 86) for a high level; if not, trace low back on schematics to find faulty IC. Check for 08_{16} on outputs of U571. If outputs not 08_{16} suspect U571; otherwise suspect U235 (on schematic 69 or 80).

Error Indication

STK PNTR	TEST 0	ADDR 04	EXPECTED YY	ACTUAL ZZ

Possible Cause	Action
Readback circuitry not functional.	Loop test 0. Check that the SP0-SP3 inputs to U235 (on schematic 69 or 80) match the outputs of U235 whenever U235 pin 1 is low. If inputs do not match outputs, suspect U235. Otherwise, suspect U571 (on schematic 76 or 86).

91A24 AND 91AE24 STK PNTR TEST 0 DESCRIPTION
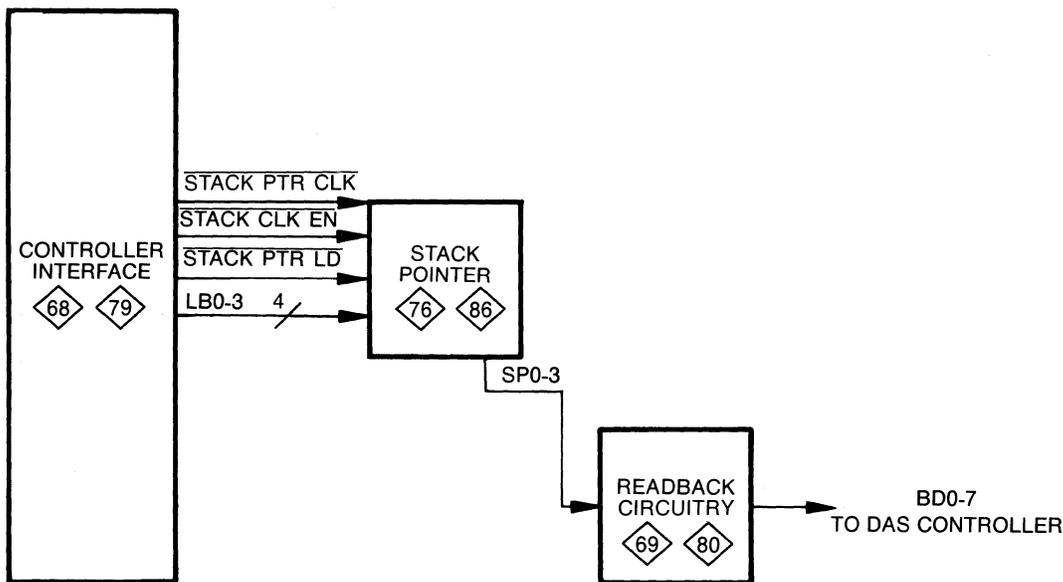
4541-716

Figure 7-18. Blocks of the 91A24 tested by the STK PNTR function, test 0.

STK PNTR test 0 verifies that the stack pointer counter (U571 on schematic 76 or 86) can be loaded and that the bits are independent. Test 0 makes four passes to walk a 1 from bit 3 to bit 0 of the counter. At the end of four passes a 1 has been loaded into and read from every bit position in the stack pointer counter. If an error is detected, the test stops.

The stack pointer counter outputs (SP0-SP3) are read back through bits 2-5 of U235 (on schematic 69 or 80). The DAS masks all undesired bits to 0s. Table 7-6 shows the values loaded and expected for each test pass.

Table 7-6
EXPECTED STACK POINTER COUNTER CONTENTS FOR STK PNTR TEST 0

Pass	Binary Value Loaded On LB0-LB7	Binary Value Read On BD0-BD7	Expected Value
1	00001000	XX1000XX	20_{16}
2	00000100	XX0100XX	10_{16}
3	00000010	XX0010XX	08_{16}
4	00000001	XX0001XX	04_{16}

Test 0 Readback Port

All test 0 results are read through U235 (port 04) on 91A24 schematic 69 or 91AE24 schematic 80.

Test 0 Initial Conditions

Before test 0 runs the pointer is set to load mode. The next two steps describe the process.

1. 80_{16} is written to U761 (on schematic 68 or 79), which makes U761 pin 15 (DUAL QUAL) high and pin 19 ($\overline{\text{STACK PTR LD}}$) low. DUAL QUAL low forces U571 pin 1 (on schematic 76 or 86) high. $\overline{\text{STACK PTR LD}}$ low goes to U571 pin 9 (on schematic 76 or 86) and sets the stack pointer in the load mode.

2. 00_{16} is written to U758 (on schematic 68 or 79), which makes U758 pin 6 ($\overline{\text{STACK CLK EN}}$) low. When $\overline{\text{STACK CLK EN}}$ is low, the stack pointer counter can be clocked through U568C, U485A, and U575D (on schematic 76 or 86).

Test 0 Run Sequence

1. One of the four test patterns (see Table 7-6) is loaded into the stack pointer counter (U571 on schematic 76 or 86) by writing the value onto LB0-LB3 and asserting U958 pin 15 ($\overline{\text{STACK PTR CLK}}$ on schematic 68 or 79). This low on $\overline{\text{STACK PTR CLK}}$ is inverted by U568C (on schematic 76 or 76) and passed through U485A and U575D (schematic 76 or 86) to clock the value on LB0-LB3 into U571.

2. After a pattern is loaded, the stack pointer counter outputs (SP0-SP3 from U571 on schematic 76 or 86) are read through buffer U235 (on schematic 69 or 80) by asserting U998 pin 5 ($\overline{\text{MAR HIGH}}$ on schematic 69 or 80). The read value is then compared with the loaded value.

3. If no error is detected, steps 1 and 2 are repeated until all four patterns have been loaded and read.

91A24 AND 91AE24 STK PNTR TEST 1 TROUBLESHOOTING

Reading the Test 1 Error Codes

Test 1 of the 91A24 STK PNTR function provides test results like those shown in Figure 7-19.
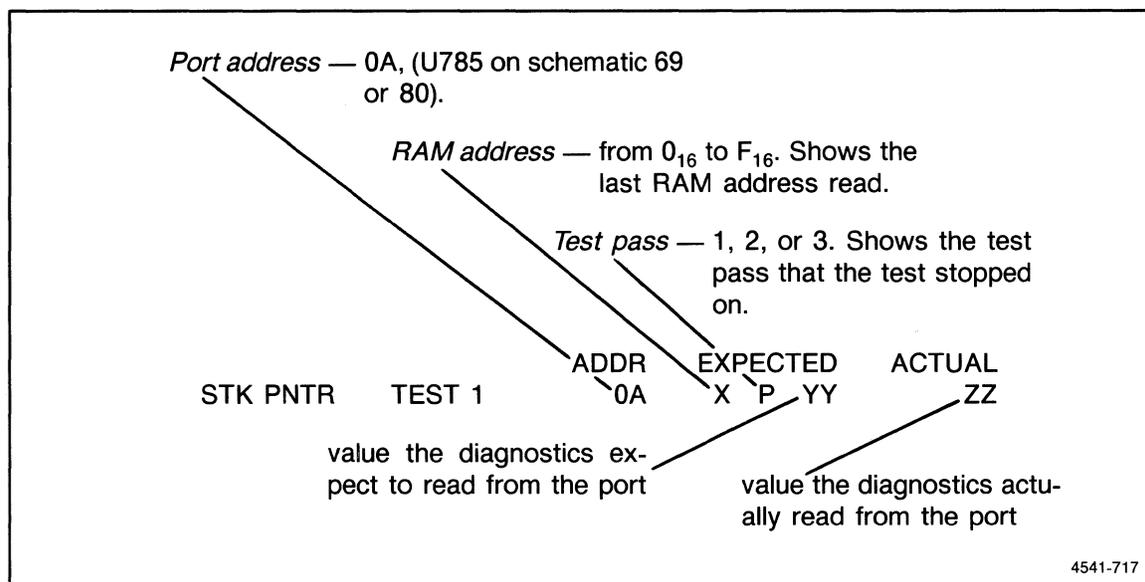
Figure 7-19. STK PNTR test 1 readback display. The ACTUAL value is read from the RAM. The EXPECTED value may be A0, 10, or C0.

Error Indication

STK PNTR function fails along with CNTR TIMR, MEM ADDR, or ACQ MEM functions.

Possible Cause	Action
Circuits feeding into STK PNTR test are not functional.	Debug according to the failed function with the smallest number.

Error Indication: 91A24

STK PNTR test 1 fails on the 91A24.

Possible Cause	Action
If a 91AE24 is connected to the 91A24, the 91AE24 may cause the failure.	Turn off the DAS. Disconnect interconnect cables from J181 at the top of the 91A24 module. Turn on the DAS and re-run test 1. If the test fails with the cables disconnected, the 91A24 is at fault. If the test passes, suspect incorrectly installed interconnect cables or a 91AE24 module.

Error Indication

		ADDR	EXPECTED	ACTUAL
STK PNTR	TEST 0	0A	0 1 A0	ZZ

Possible Cause	Action
$\overline{\text{STACK CNTL}}$ not functional.	Loop test 1. Check U958 pin 8 (on 91A24 schematic 68 or 91AE24 schematic 79) for low pulses; if none, suspect U958.
Chip select not functional.	With test 1 still looping, check U555 pin 2 (on schematic 75 or 86) for low; if not low, suspect R753 (on schematic 75 or 86).
$\overline{\text{STACK CNTL RD}}$ not functional.	Check U998 pin 11 (on schematic 69 or 80) for low pulses; if none, suspect U998.
Readback circuitry or RAM not functional.	See if U785 (on schematic 69 or 80) inputs SC0-SC3 match the outputs of U785 when U785 pin 1 is low. If inputs do not match outputs, suspect U785. If inputs and outputs match, suspect U555 (on schematic 75 or 86).

91A24 AND 91AE24 STK PNTR TEST 1 DESCRIPTION
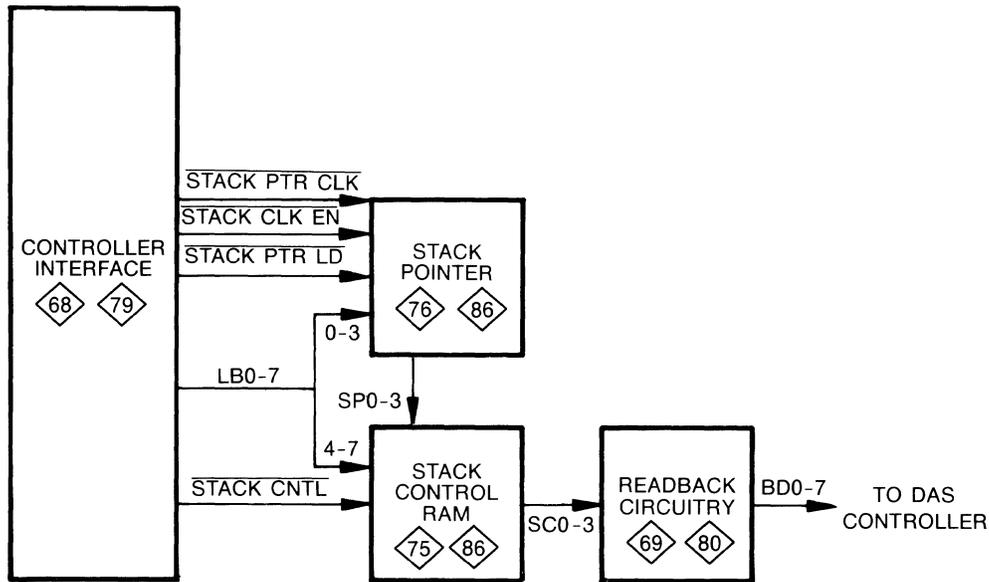
Figure 7-20. Blocks of the 91A24 tested by the STK PNTR function, test 1.

STK PNTR test 1 checks the stack control RAM. This is done in three passes. In each pass a repeating test pattern is written to the 16 RAM addresses. The patterns loaded during each pass are shown in Table 7-7. The patterns were selected to verify both address and storage bit independence when all three passes are complete.

The patterns used in this test are A, 1, and C as in other RAM tests. When these patterns are written to the stack control RAM, they are shifted left four bits and inverted since the stack control RAM loads and reads from the high four bits (7 through 4) and has inverting outputs.

On each pass, at every location, an address is loaded into the stack pointer and a data pattern is written to the RAM. For example, the first value written to location 0 (on LB0-LB7) in the stack control RAM is 01010000 (50_{16}). Only the four most significant bits (LB7-LB4) are stored by the RAM. The stack control RAM inverts its output data, so if this address passes, 1010_2 (A_{16}) will be read on SC0-SC3. After each write pass (16 writes) the stack pointer is again loaded with the addresses and the stack control RAM is read for the correct contents. If a failure is detected at any address on any pass, the test stops with that failure and an error message is displayed.

Table 7-7 shows the loaded and expected values for each pass.

Table 7-7
EXPECTED STACK CONTROL RAM VALUES FOR STK PNTR TEST 1

Stack Address	Expected Value: Write/Read		
	Pass 1	Pass 2	Pass 3
0	50/AX	E0/1X	30/CX
1	E0/1X	30/CX	50/AX
2	30/CX	50/AX	E0/1X
3	50/AX	E0/1X	30/CX
4	E0/1X	30/CX	50/AX
...	...	...	...

Test 1 Readback Port

All test 1 results are read through U785 (port 0A) on 91A24 schematic 69 or 91AE24 schematic 80.

Test 1 Initial Conditions

The following initial conditions repeat those of STK PNTR test 0.

1. 80_{16} is written to U761 (on schematic 68 or 79), which makes U761 pin 19 ($\overline{\text{STACK PTR LD}}$) low. $\overline{\text{STACK PTR LD}}$ low goes to U571 pin 9 (on schematic 76 or 86) and sets the stack pointer in the load mode.

2. 00_{16} is written to U758 (on schematic 68 or 79), which makes U758 pin 6 ($\overline{\text{STACK CLK EN}}$) low. When $\overline{\text{STACK CLK EN}}$ is low, the stack pointer counter can be clocked through U568C, U485A, and U575D (on schematic 76 or 86).

Test 1 Run Sequence

1. The stack control RAM address is first written onto LB0-LB3 and U958 pin 15 ($\overline{\text{STACK PTR CLK}}$ on schematic 68 or 79) is asserted. This loads the stack pointer counter (U571 on schematic 76 or 86) with the RAM address, which then addresses the stack control RAM (U555 on schematic 75 or 86).

2. The test pattern is written onto LB7-LB4 and $\overline{\text{STACK CNTL}}$ is asserted, which loads the pattern into the stack control RAM (U555 on schematic 75 or 86).

3. Steps 1 and 2 are repeated for all 16 stack control RAM addresses (U555 on schematic 75 or 86).

4. The stack control RAM address is again established as in step 1.

5. The stack control RAM outputs (SC0-SC3) are then read from U785 (on schematic 69 or 80) on the assertion of U998 pin 11 ($\overline{\text{STACK CNTL RD}}$ schematic 69 or 80). If the data read from a RAM address does not equal the data written to a RAM address, the DAS displays an error and the test stops.

6. Steps 4 and 5 are repeated for all 16 addresses.

7. Steps 1 through 6 are repeated two more times to complete all three passes.

91A24 AND 91AE24 STK PNTR TEST 2 TROUBLESHOOTING

Reading the Test 2 Error Codes

Test 2 of the 91A24 STK PNTR function provides test results like those shown in Figure 7-21.
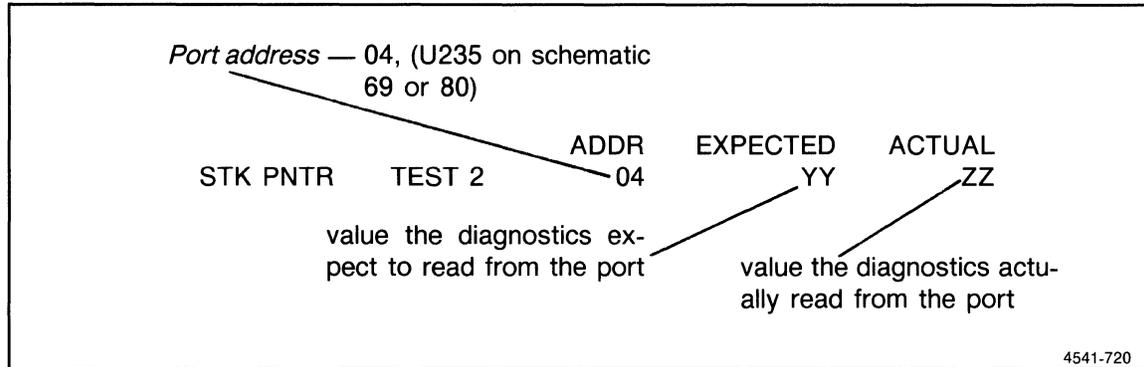
Figure 7-21. **STK PNTR test 2 readback display.** The ACTUAL value is read from the stack pointer. The EX-PECTED value may be any of the following: 00, 04, 08, 0C, 10, 14, 18, 1C, 20, 24, 28, 2C, 30, 34, 38, or 3C,.

Error Indication

STK PNTR function fails along with CNTR TIMR, MEM ADDR, or ACQ MEM functions.

Possible Cause	Action
Circuits feeding into STK PNTR test are not functional.	Debug according to the failed function with the smallest number.

Error Indication: 91A24

STK PNTR Test 2 fails on the 91A24.

Possible Cause	Action
If a 91AE24 is connected to the 91A24, the 91AE24 may cause the failure.	Turn off the DAS. Disconnect interconnect cables from J181 at the top of the 91A24 module. Turn on the DAS and re-run test 2. If the test fails with the cables disconnected, the 91A24 is at fault. If the test passes, suspect incorrectly installed interconnect cables or a 91AE24 module.

Error Indication

		ADDR	EXPECTED	ACTUAL
STK PNTR	TEST 0	04	YY	ZZ

Possible Cause	Action
STACK PTR LD or stack pointer not functional.	Loop test 2. Check U761 pin 19 (on 91A24 schematic 68 or 91AE24 schematic 79) for high with low pulses; if not high with low pulses, suspect U761; otherwise suspect U571 (schematic 76 or 86).

91A24 AND 91AE24 STK PNTR TEST 2 DESCRIPTION
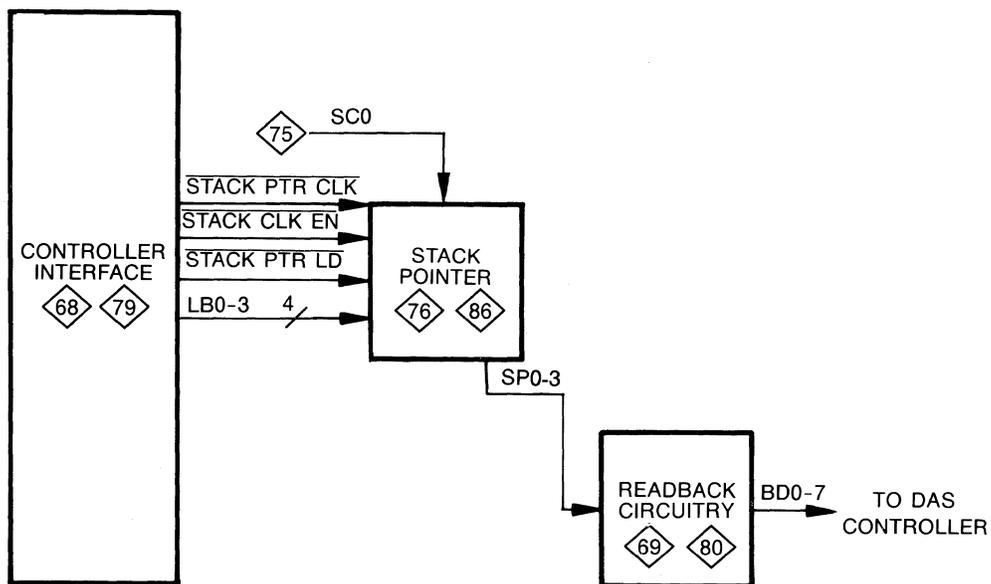
4541-721

Figure 7-22. Blocks of the 91A24 tested by the STK PNTR function, test 2.

STK PNTR test 2 verifies the stack pointer's (U571 on schematic 76 or 86) ability to operate in count mode. The stack control RAM (U555 on 91A24 schematic 75 or 91AE24 schematic 86) is first loaded (on LB4-LB7) with 0s which are inverted to 1s at the output (SC0-SC3). The stack pointer is then loaded with 0_{16} on LB0-LB3.

After the stack pointer is loaded with 0_{16}, SC0 is asserted to enable the stack pointer, and the stack pointer is clocked from 0_{16} to F_{16} using $\overline{\text{STACK PTR CLK}}$. After each clock the stack pointer is read for the correct value. If an error is detected during any of the steps, the test stops with that failure.

NOTE

The loading function of the stack pointer is not tested in this test — only the counting function is tested. Stack pointer loading is tested in test 0, where each stack pointer address location is manually loaded and clocked into the stack control RAM. In this test, the stack pointer counter (U571) is enabled by SC0 to increment and generate addresses internally following a clocking signal.

Test 2 Readback Port

All test 2 results are read back through U235 (port 04) on 91A24 schematic 69 or 91AE24 schematic 80. The port reads the four stack pointer bits as the middle four bits of a byte. For example, a 1_{16} from the stack pointer is read as 04 (00000100_2) and an F_{16} from the pointer is read as 3C (00111100_2).

Test 2 Initial Conditions

1. 80_{16} is written to U761 (on schematic 68 or 79), which makes U761 pin 19 ($\overline{\text{STACK PTR LD}}$) low. $\overline{\text{STACK PTR LD}}$ low goes to U571 pin 9 (on schematic 76 or 86) and sets the stack pointer in the load mode.

2. 00_{16} is written to U758 (on schematic 68 or 79), which makes U758 pin 6 ($\overline{\text{STACK CLK EN}}$) low. When $\overline{\text{STACK CLK EN}}$ is low, the stack pointer counter can be clocked through U568C, U485A, and U575D (on schematic 76 or 86).

3. The stack control RAM (U555 on schematic 75 or 86) is filled with 0s, which are inverted to 1s by the RAM outputs.

4. 00_{16} is written to U958 pin 15 ($\overline{\text{STACK PTR CLK}}$ on schematic 68 or 79), which loads U571 (on schematic 76 or 86) with 0s

5. 90_{16} is written to U761 (on schematic 68 or 79), making U761 pin 19 ($\overline{\text{STACK PTR LD}}$) high which enables the stack pointer to count.

Test 2 Run Sequence

1. The stack pointer (U571 on 91A24 schematic 76 or 91AE24 schematic 86) is read back through U235 (SP0-SP3 on schematic 69 or 80), and compared against the expected value. The expected values are, in sequence: 00, 04, 08, 0C, 10, 14, 18, 1C, 20, 24, 28, 2C, 30, 34, 38, or 3C.

2. The stack pointer is incremented by writing 00_{16} to U958 pin 15 ($\overline{\text{STACK PTR CLK}}$).

3. Steps 1 and 2 are repeated until an error is detected or the stack pointer reaches F_{16}.

91A24 FUNCTION 4 WRD REC
91AE24 FUNCTION 3 WRD REC

CIRCUIT OVERVIEW

The WRD REC (word recognizer) function tests all word recognizers on the 91A24 and 91AE24 modules. There are two separate word recognizer circuits on the modules: the stack word recognizer, and the data qualifier word recognizer.

Stack Word Recognizer. This circuit provides the module's 16-level word recognizer. The circuit is centered around three 4096 × 1 bit RAMS (U148, U248, and U448 on 91A24 schematic 75 or 91AE24 schematic 86). Four bits of the RAM address (SP0-SP3) indicate the position of a stack pointer (U571 on schematic 76 or 86). SP0-SP3 increments to set the sequential word recognizer set to watch for the next word in the trigger sequence.

The data being logged into acquisition memory (DR0-DR23 on schematic 73 or 84) provide the remaining address signals for the word recognizer RAMs. A RAM output goes high whenever the DR0-DR23 signals and the SP0-SP3 signals all point to a word to be recognized. The outputs of all three RAMs (SW0-SW2 from U148, U248, and U448 on schematic 75 or 86) must be high for a word to be recognized, because the outputs are ANDed by U168A (schematic 75 or 86).

Data Qualifier Circuit. This circuit controls the four programmable word recognizers that are independent of the stack word recognizer. The center of the circuit is three 256 × 4 bit RAMs (U151, U351, and U551, on 91A24 schematic 74 or 91AE24 schematic 85). The data about to be logged into the acquisition memory (DR0-DR23 on schematic 73 or 84) provides the address for the word recognizer RAMs.

When DR0-DR23 correspond to a word to be recognized, the same output of all three RAMs goes high. Since each RAM has four outputs, four different words can be recognized. All three RAMs must recognize their portion of the word at the same time for a word to be recognized, because of AND gates U261A, B, and C, and U168B (on schematic 74 or 85).

FUNCTION DESCRIPTION

The WRD REC function consists of two separate tests.

Test 0 exercises the stack word recognizer by loading test patterns into the three RAMs and reading them back.

Test 1 exercises the data qualifier word recognizer by loading patterns into the three RAMs and reading them back.

Readback Ports

All the test 0 results are read through 91A24 port 0E (U771 on schematic 69 or 80).

All the test 1 results are read through 91A24 port 07 (U778 on schematic 69 or 80).

91A24 AND 91AE24 WRD REC TEST 0 TROUBLESHOOTING

Reading the Test 0 Error Codes

Test 0 of the WRD REC function provides test results like those shown in Figure 7-23.
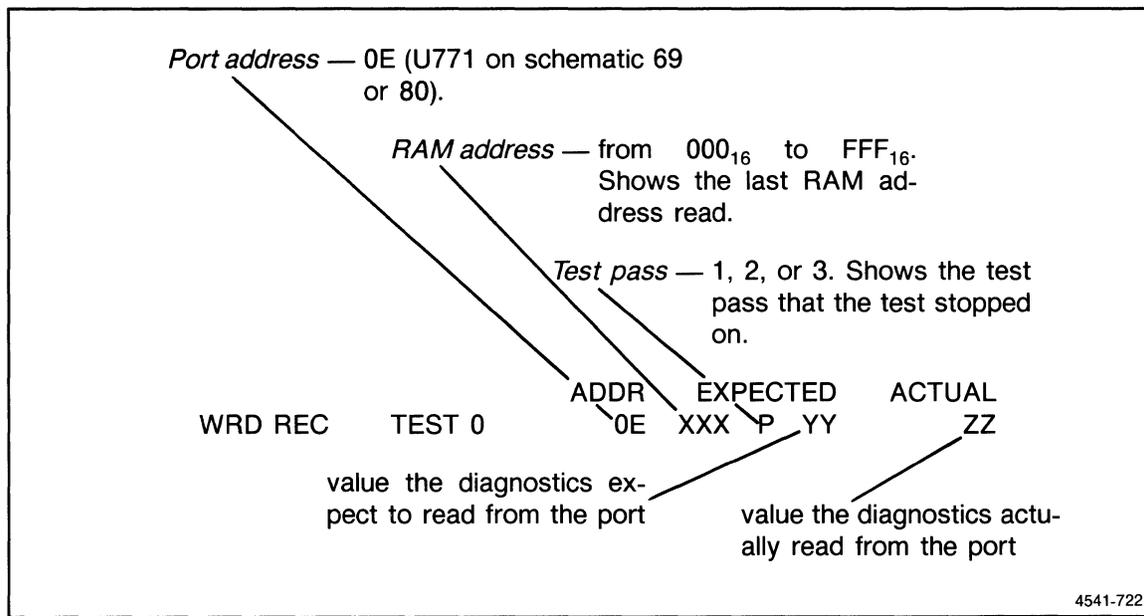
Figure 7-23. WRD REC test 0 readback display. The ACTUAL value is read from the RAM. The EXPECTED value depends on the test pass and address. Refer to Table 7-9 for expected values.

Error Indication

WRD REC function fails along with CNTR TIMR, MEM ADDR, ACQ MEM, or STK PNTR functions.

Possible Cause	Action
Circuits feeding into WRD REC test are not functional.	Debug according to the failed function with the smallest number.

Error Indication: 91A24

WRD REC test 0 fails on the 91A24.

Possible Cause	Action
If a 91AE24 is connected to the 91A24, the 91AE24 may cause the failure.	Turn off the DAS. Disconnect interconnect cable from J181 at the top of the 91A24 module. Turn on the DAS and re-run test 1. If the test fails with the cable disconnected, the 91A24 is at fault. If the test passes, suspect incorrectly installed interconnect cables or a 91AE24 module.

Error Indication

		ADDR	EXPECTED	ACTUAL
WRD REC	TEST 0	0E	XXX 1 40	ZZ

000, 001, or 002

Possible Cause	Action
Stack write enable signals malfunctioning.	Loop test 0 and examine pins 5, 6, and 7 of U958 (on schematic 68 or 79) with a scope. If any pins do not pulse low, suspect U958.
Stack word recognizer chip select malfunction.	While test is still looping, check U148 pin 10 (on schematic 75 or 86) for low; if not low, suspect R149 (on schematic 75 or 86).
Readback circuitry malfunctioning.	Loop test 0 and check U998 pin 16 (on schematic 69 or 80) for low pulses; if none, suspect U998. If low pulses are present, check that inputs SW0-SW2 to U771 (schematic 69 or 80) match the outputs during the low pulse at U771 pin 1. If inputs to U771 do not match outputs when U771 pin 1 is low, suspect U771; otherwise continue to the next possible cause.

Error Indication

		ADDR	EXPECTED	ACTUAL
WRD REC	TEST 0	0E	XXX P YY	ZZ

WRD REC test 0 fails and none of the previously listed test 0 failures occurred.

Possible Cause	Action
RAM malfunction. Suspect U148, U248, or U448 (on schematic 75 or 86).	Suspect the RAM indicated by Table 7-8. Failure of multiple RAMs is unlikely. If multiple RAM failures are indicated, check the other failures described earlier. The DAS will not show ACTUAL values other than those in Table 7-8.

Table 7-8
STACK WORD RECOGNIZER RAM FAILURE INDICATIONS

		Expected		
		20	40	80
Actual	00	Suspect U448	Suspect U248	Suspect U148
	20	No failure	Suspect U248 or U448	Suspect U148 or U448
	40	Suspect U248 or U448	No failure	Suspect U148 or U248
	60	Suspect U248	Suspect U448	Suspect U148, U248, or U448
	80	Suspect U148 or U448	Suspect U148 or U248	No failure
	A0	Suspect U148	Suspect U148, U248, or U448	Suspect U448
	C0	Suspect U148, U248, or U448	Suspect 148	Suspect U248
	E0	Suspect U148, or U248	Suspect U148 or U448	Suspect U248 or U448

91A24 AND 91AE24 WRD REC TEST 0 DESCRIPTION
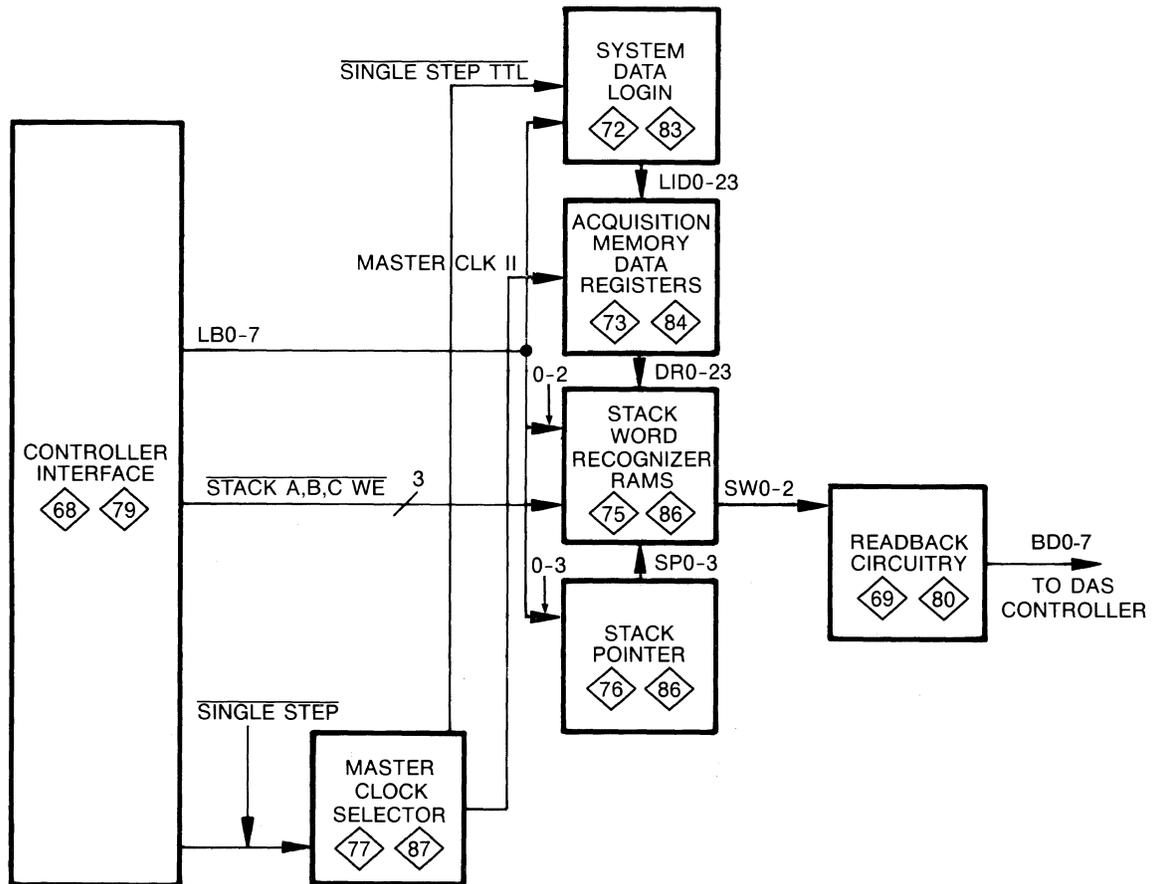
4541-723

Figure 7-24. Blocks of the 91A24 tested by the WRD REC function, test 0.

WRD REC test 0 verifies the operation of all three stack word recognizer RAMs (U148, U248, and U448 on 91A24 schematic 75 or 91AE24 schematic 86).

The ACQ MEM function has already verified the bus that loads the word recognizer RAMs (LB0-LB2 on schematic 68 or 79). The ACQ MEM function has also verified the eight most significant address bits to the word recognizer RAMs (DR0-DR23 on schematic 73 or 84). If the ACQ MEM function passes, then the bus that loads the test into the word recognizer RAM, and the eight most significant address bits to the RAM, are functional.

The STK PNTR function has already verified the four least significant address lines to the stack word recognizer RAMs (SP0-SP3 on schematic 76 or 86). If the STK PNTR function passes, the four least significant address lines to the RAM are functional.

If both the ACQ MEM and STK PNTR functions pass, then all input signals to the word recognizer RAMs are verified except $\overline{\text{STACK A WE}}$-$\overline{\text{STACK C WE}}$ and the chip select signals (U148 pin 10, U248 pin 10, and U448 pin 10 on schematic 75 or 86).

When test 0 runs at power-up, only addresses 000_{16} - $04F_{16}$ in the RAM are tested. If the test is run at any time other than power-up, all 4096 addresses are checked.

Newly tested circuitry includes:

* The $\overline{\text{STACK A WE}}$, $\overline{\text{STACK B WE}}$, and $\overline{\text{STACK C WE}}$, signals.

* Stack word recognizer RAMs U148, U248, and U448 (schematic 75 or 86).

* The SW0-SW2 bus (on schematic 75 or 86).

* Readback port U771 (schematic 69) and its enable signal, $\overline{\text{TRIGGERED RD}}$.

Test 0 treats the three word recognizer RAMs, U148, U248, and U448, (on schematic 75 or 86) as one 4096 $\times$ 3 bit RAM. The RAM is tested in three passes. The test patterns loaded into the RAM are described in Table 7-9.

* The least significant loaded bit goes to U148.

* The middle loaded bit goes to U248.

* The most significant loaded bit goes to U448.

Table 7-9
TEST PATTERNS USED IN WRD REC TEST 0

Hex RAM Addr	Pass 1		Pass 2		Pass 3	
	Loaded	Read	Loaded	Read	Loaded	Read
000	010	40	001	80	100	20
001	001	80	100	20	010	40
002	100	20	010	40	001	80
003	010	40	001	80	100	20
...	...	...	...	...	...	...

Test 0 Readback Port

All test 0 results are read through U771 (port 0E) on 91A24 schematic 69 or 91AE24 schematic 80.

Test 0 Initial Conditions

1. 80_{16} is written to U761 (on schematic 68 or 79), so $\overline{\text{STACK PTR LD}}$ goes low. This allows loading the stack pointer (U571 on schematic 76 or 86).

2. On all 91A24 and 91AE24 modules, 00_{16} is written to U758 (on schematics 68 and 79). This sets $\overline{\text{STACK CLK EN}}$ and $\overline{\text{A DIAG EN}}$ - $\overline{\text{C DIAG EN}}$ low.

3. On all 91A24 and 91AE24 modules, 80_{16} is written to U945 (on schematics 77 and 87). This enables the $\overline{\text{SINGLE STEP}}$ clock.

Test 0 Run Sequence

1. The address of the RAMs is placed on the two buses controlling the address (SP0-SP3 and DR0-DR23).

2. The data to be loaded into the RAM is then written to ports 04_{16}, 05_{16}, and 06_{16} ($\overline{\text{STACK WE A}}$-- $\overline{\text{STACK WE C}}$ ports from U958, on schematic 68 or 79). All three RAMs are completely loaded from address 000_{16} to FFF_{16} at the beginning of each test pass, before the DAS reads back the RAM contents.

NOTE

The DAS will not stop 91A24 WRD REC test 0 while the RAM is being loaded. This loading takes about 20 seconds at the beginning of each test pass. After the RAMs are loaded, the test may be stopped with the STOP key.

3. After loading the entire memory, the DAS reads the RAM contents over the SW0-SW2 bus. This bus goes to the three most significant bits of U771 (on schematic 69 or 80). The output of this port goes to the DAS Controller data bus on the Interconnect board.

    The readback from the RAMs occupies the highest three-out-of-eight bits of U771. The readback through U771 has the bit significance reversed from the input data. So if 100_2 is written into the RAM, the diagnostics read back 001_2, and display 20_{16}. The bottom five readback bits are masked, in this example to $001[00000]_2$, by the diagnostics.

4. Steps 1-3 are repeated two more times, using different input values (see Table 7-9).

91A24 AND 91AE24 WRD REC TEST 1 TROUBLESHOOTING

Reading the Test 1 Error Codes

Test 1 of the WRD REC function provides test results like those shown in Figure 7-25.

Port address — 07, (U778 on schematic 69 or 80).

RAM address — from 00_{16} to FF_{16}. Shows the last RAM address read.

RAM being tested — A = U151, B = U351, C = U551.

Test pass — 1, 2, or 3. Shows the test pass that the test stopped on.

| | | ADDR | EXPECTED | ACTUAL |
WRD REC   TEST 0   07   00 A 1 YY   ZZ

value the diagnostics expect to read from the port

value the diagnostics actually read from the port

4541-724
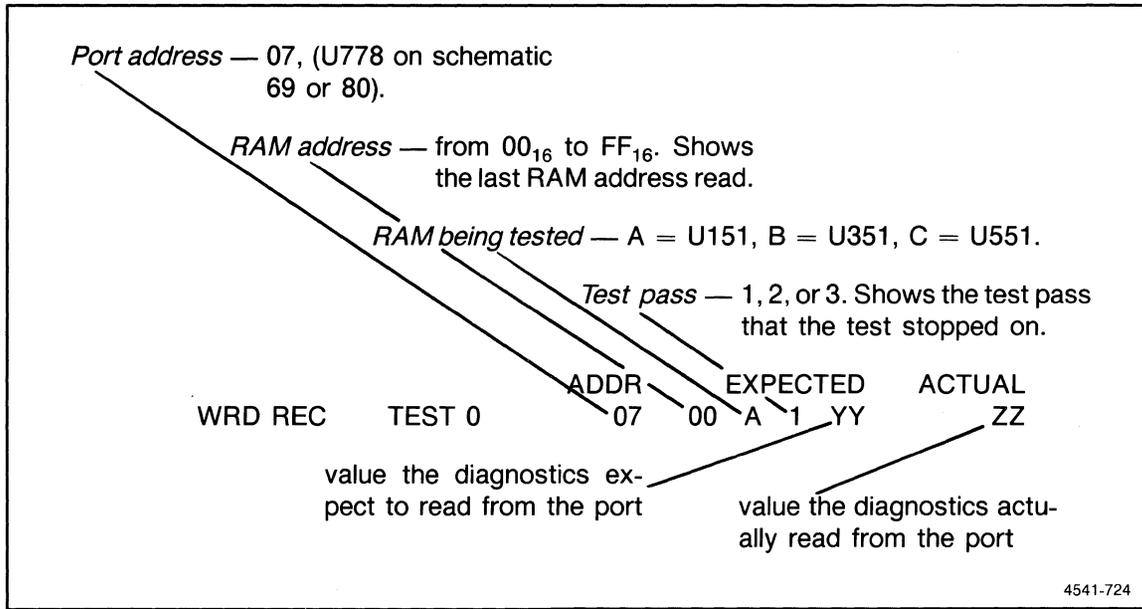
Figure 7-25. WRD REC test 1 readback display. The ACTUAL value is read from the RAM. The EXPECTED values are shown in Table 7-10.

Error Indication

WRD REC function fails along with CNTR TIMR, MEM ADDR, ACQ MEM, or STK PNTR functions.

Possible Cause	Action
Circuits feeding into WRD REC test are not functional.	Debug according to the failed function with the smallest number.

Error Indication: 91A24

WRD REC test 1 fails on the 91A24.

Possible Cause	Action
If a 91AE24 is connected to the 91A24, the 91AE24 may cause the failure.	Turn off the DAS. Disconnect interconnect cables from J176 and J178 at the top of the 91A24 module. Turn on the DAS and re-run test 1. If the test fails with the cables disconnected, the 91A24 is at fault. If the test passes, suspect incorrectly installed interconnect cables or a 91AE24 module.

Error Indication: 91A24

```
                              ADDR         EXPECTED     ACTUAL
          WRD REC    TEST 1    07   XX  A  1  0A          ZZ
                              00, 01, or 02
```

Test 1 fails at RAM address 00, 01, or 02, test pass 1 on the 91A24.

Possible Cause	Action
Data qualifier disabling circuitry is malfunctioning.	Loop test 1. Examine pin 11 of U568D (schematic 74). If this pin is static low, the data qualifier disabling circuitry is probably okay. Continue on to the next possible cause. If U568D pin 11 is not static low, examine pin 5 of U581B (91A32 QUAL on schematic 74). If this pin is not static high, then suspect the Interconnect or the Trigger/Time Base board, which supply this signal. Examine pin 4 of U581B ($\overline{\text{91A24 INIT}}$ signal on schematic 74). If this pin is not static high, suspect U761. Examine pin 3 of U488A (MASTER CLK I on schematic 74). This pin should carry occasional clock pulses (while the test reads and writes). If there is no clock signal, suspect Q545 or Q546 (schematic 77). Examine pin 6 of U488A (on schematic 74). If this pin is not static high, suspect U488. Examine pin 11 of U568D. If this pin is not low, suspect U568.

Error Indication: 91A24 and 91AE24

```
                              ADDR         EXPECTED     ACTUAL
          WRD REC    TEST 1    07   XX  A  1  0A          ZZ
                              00, 01, or 02
```

Test 1 fails at RAM address 00, 01, or 02, test pass 1 on either module type.

Possible Cause	Action
Write enable signals to one of the word recognizer RAMs are malfunctioning.	Loop test 1. Check pin 17 of U958 ($\overline{\text{PADQ WE}}$ on schematic 68 or 79) with a scope. If the pin does not show occasional low pulses, suspect U958. Check pins 1 and 2 of U965 ($\overline{\text{PBDQ WE}}$ and $\overline{\text{PCDQ WE}}$ on schematic 68 or 79) with a scope. If one or both of these pins do not show occasional low pulses, suspect U965.

Error Indication: 91A24 and 91AE24 (cont.)

			ADDR				EXPECTED	ACTUAL
WRD REC		TEST 1	07	XX	A	1	0A	ZZ
				00, 01, or 02				

One of the word recognizer RAMs is malfunctioning.	While test is looping, examine pins 10, 12, 14, and 16 of U151 (schematic 74 or 85) with a scope. If these pins do not toggle, suspect U151.

Examine pins 10, 12, 14, and 16 of U351 (schematic 74 or 85). These pins should be high most or all of the time. If one of these pins is stuck low, suspect U351.

Examine pins 10, 12, 14, and 16 of U551 (schematic 74). These pins should be high most or all of the time. If any pins are stuck low, suspect U551. |
| ANDing circuit is malfunctioning. | Loop test 1. Examine U261A, B, C, pins 6, 8, and 12 and U168B pin 6 (on schematic 74 or 85) with a scope. If all these pins toggle, then the ANDing circuit works; proceed to the next probable cause. Otherwise, go to the next paragraph.

If one or all of pins 6, 8, or 12 on U261A, B, C is stuck, but U168B pin 6 operates properly, then U261 (on schematic 74 or 85) has probably failed. If U261 is not causing the problem, suspect U278 (on the 91A24 only, schematic 74).

If only U168B pin 6 is stuck low, then U168 has probably failed. Suspect U168 (on schematic 74 or 85). If U168 is not causing the problem, suspect U278 (on the 91A24 only, schematic 74).

If all of U261A, B, C, pins 6, 8, and 12 and U168B pin 6 are stuck, then U278 (on the 91A24 only, schematic 74) has probably failed. |
| Word recognizer output control logic is malfunctioning. | Loop test 1. Examine U778 pins 11, 13, 15, and 17 (schematic 69 or 80). If all of these pins toggle, then the word recognizer output control logic is probably functional. Proceed to the next probable cause.

If any of U778 pins 11, 13, 15 or 17 do not toggle, examine U765 pins 12, 15, and 16 (TN0-TN3 on schematic 68 or 79). If any of these pins are high, then suspect U765.

Examine U761 pin 16 (MEM RD on schematic 68 or 79). If this pin is stuck high, then suspect U761.

Examine U291A, B, D, pins 3, 6, and 11 (on schematic 74 or 85). If any of these pins do not toggle, then suspect U291.

Examine U198B pin 6 (schematic 74 or 85). If this pin does not toggle, then suspect U198. |
| Readback circuitry is malfunctioning. | Loop test 1. Check U998 pin 8 ($\overline{\text{DQ STATUS}}$ on schematic 69 or 80) for low pulses; if none, suspect U998. Otherwise suspect U778 (on schematic 69 or 80). |

Error Indication

		ADDR	EXPECTED	ACTUAL
WRD REC	TEST 1	07	XX A X YY	ZZ

Test 1 fails during a test pass on RAM A.

Possible Cause	Action
RAM malfunction. Prime suspect is U151. Secondary suspects are U351 and U551.	Suspect U151 (on schematic 74 or 85). Because the outputs of all three RAMs are ANDed together, the fault may be with one of the other two RAMs. If replacing U151 does not re-solve the failure, try replacing U351 and/or U551.

Error Indication

		ADDR	EXPECTED	ACTUAL
WRD REC	TEST 1	07	XX B X YY	ZZ

Test 1 fails during a test pass on RAM B.

Possible Cause	Action
RAM malfunction.	Suspect U351 (on schematic 74 or 85).

Error Indication

		ADDR	EXPECTED	ACTUAL
WRD REC	TEST 1	07	XX C X YY	ZZ

Test 1 fails during a test pass on RAM C.

Possible Cause	Action
RAM malfunction.	Suspect U551 (on schematic 74 or 85).

91A24 AND 91AE24 WRD REC TEST 1 DESCRIPTION
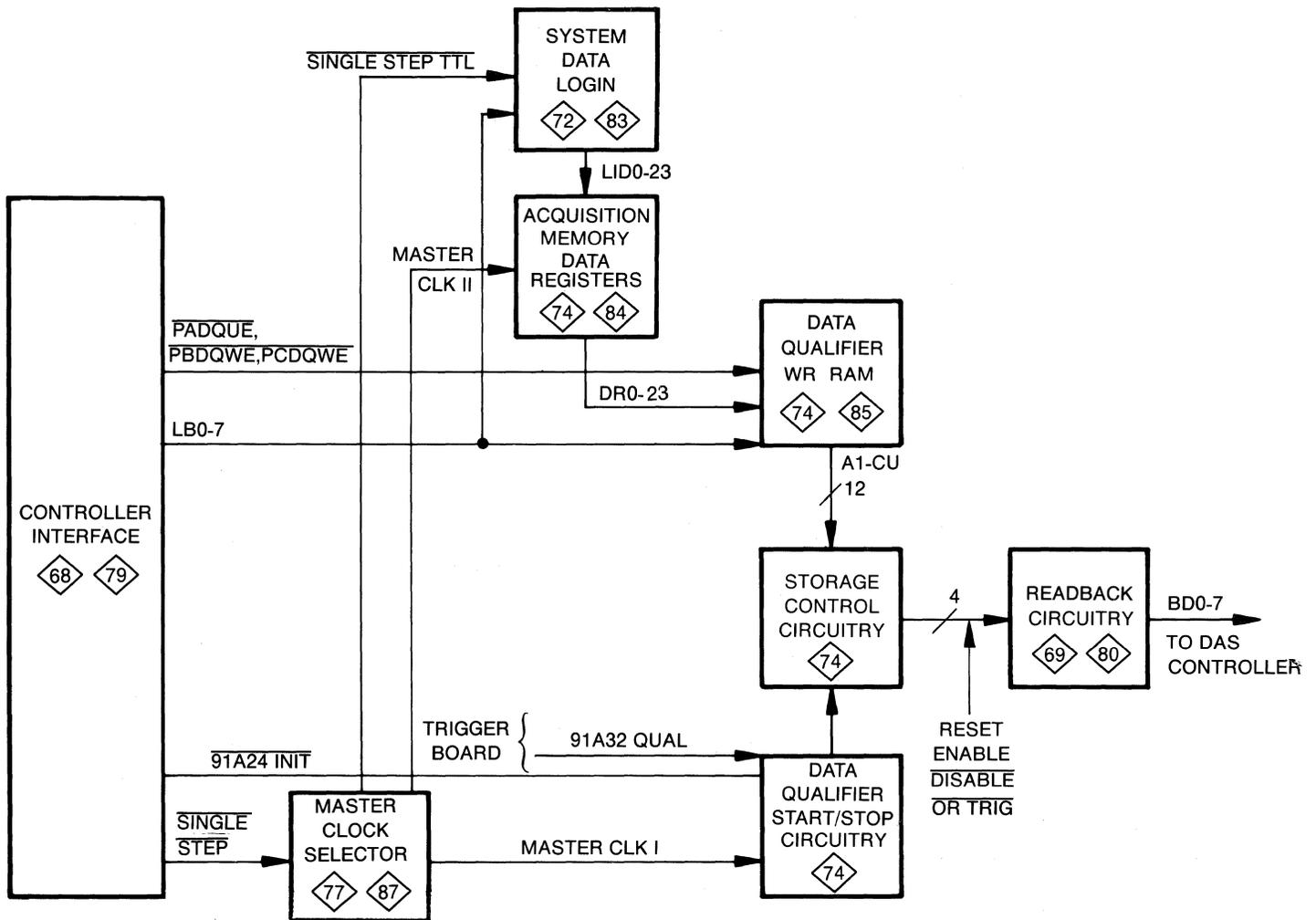
4541-726

Figure 7-26. Blocks of the 91A24 tested by the WRD REC function, test 1. The Storage Control and Data Qualifier Start/Stop circuitry on the 91A24 is used to test both 91A24 and 91AE24 modules.

WRD REC test 1 verifies operation of all three data qualifier word recognizer RAMs (U151, U351, and U551 on 91A24 schematic 74 or 91AE24 schematic 85).

Test 0 has already verified the data and address buses that load the word recognizer RAMs. The only input signals to the RAM that were not verified by test 0 are $\overline{PADQ\,WE}$, $\overline{PBDQ\,WE}$, and $\overline{PCDQ\,WE}$.

When test 1 runs at power-up, only addresses 00_{16} - 04_{16} in the RAM are tested. If the test is run at any time other than power-up, all 256 addresses are checked.

Newly tested circuitry includes

• The $\overline{PADQ\,WE}$, $\overline{PBDQ\,WE}$, and $\overline{PCDQ\,WE}$ signals (from U958 and U965 on schematic 68 or 79).

- Word recognizer RAMs U151, U351, and U551 (schematic 74 or 85).

- The A1-C4 bus from the word recognizer (schematic 74 or 85).

- AND gates U261A, B, and C, and U168B (schematic 74 or 85).

- Disable circuitry U488A, U581B, U568D, and U278A, B, E, and F (only on 91A24 schematic 74).

- The TN0-TN2 bus and exclusive OR gates U291A, B, and D (schematic 74 or 85).

- The MEM RD signal and OR gate U198B (schematic 74 or 85).

- Readback port U778 (schematic 69 or 80) and its enable signal, $\overline{\text{DQ STATUS}}$.

Test 1 Readback Port

Test 1 results are read through U778 (port 07) on 91A24 schematic 69 or 91AE24 schematic 80.

Test 1 Initial Conditions

The readback from the RAMs passes through some active circuits before arriving at the RESET, ENABLE, $\overline{\text{DISABLE}}$, $\overline{\text{OR TRIG}}$ bus (on schematic 74 or 85). For proper readback to occur from the RAMs, these circuits must be partially functional, and the incoming control lines must be at the proper levels.

On the 91A24, the following control lines are placed in the states given below in order to turn off the disable circuits on the 91A24 built around flip-flop U488A, NAND gates U568D and U581B, and inverters U278A, B, E, and F (schematic 74).

- $\overline{\text{91A24 INIT}}$ must be high.

- 91A32 QUAL from the Trigger/Time Base must be high.

- MASTER CLK I must be able to make at least one rising edge.

The following control lines must be in the given states to prevent the output signal onto the RESET, ENABLE, $\overline{\text{DISABLE}}$, $\overline{\text{OR TRIG}}$ bus from being inverted.

- All three TN0-TN2 signals must be low.

- The MEM RD signal must be low.

Finally, the RESET WORD and ENABLE WORD signals (J176, schematic 74 or 85) and the DISABLE WORD and OR TRIG WORD signals (J178, schematic 74 or 85) must be high on all 91A24 and 91AE24 modules not being tested. These signals are set high by writing FF to U151, U351, and U551 (schematic 74 or 85) on all 91A24 and 91AE24 modules not being tested.

Test 1 Run Sequence

At the beginning of each pass the data qualifier RAMs are entirely filled with a pattern. The pattern loading is described in the next five steps.

1. DR0-DR23 is loaded with 000000_{16} at the beginning of each test pass. DR0-DR23 provides the address of the RAMs under test. The address comes from the LID0-LID23 bus, where it is initially latched into the system data login registers (U125, U225, and U425 on schematic 72 or 83).

2. The test value for that address is loaded into the RAM under test by writing the value on LB0-LB7 and asserting $\overline{PADQ\ WE}$, $\overline{PBDQ\ WE}$, or $\overline{PCADQ\ WE}$. The proper test value is shown in Table 7-10. RAMs U151 and U351 are loaded from LB0-LB3, and RAM U551 is loaded from LB4-7.

3. F_{16} is loaded into the same address on the other two RAMs. To do this, LB0-LB7 are loaded with FF_{16}, and the write enables of the two RAMs are asserted.

4. The address on the DR0-DR23 bus is increased. For the purposes of this test, DR0-DR23 is divided into three parts. For the second loaded address to be 01_{16}, DR0-DR23 is set to 010101_{16}. The third DR0-DR23 value is 020202_{16}, and so on up to $EFEFEF_{16}$ and $FFFFFF_{16}$.

5. Steps 2 through 4 are repeated until all addresses of all three RAMs are loaded with the value appropriate to the test pass.

When all addresses are filled, the contents of the RAM are read and compared to the expected value. This read and compare sequence is described in steps 6 through 10.

6. DR0-DR23 is loaded with 000000_{16} as described in step 1.

7. Port 07 (U778 on schematic 69 or 80) is read by asserting $\overline{DQ\ STATUS}$. The top four bits from port 07 are compared to the expected value. If the values do not match, an error is displayed and the test stops.

8. If no error is found, the DR0-DR23 value is increased (as described in step 4).

9. Steps 7 and 8 are repeated until all 256 addresses have been read or an error is found.

10. Steps 1 through 9 are repeated two more times using different test values on the same RAM. After three passes, that RAM is completely tested.

11. Steps 1 through 10 are repeated two more times, once each on the remaining RAMs for a total of nine test passes.

Table 7-10
TEST PATTERNS USED IN WRD REC TEST 1

Hex RAM Addr	Pass 1		Pass 2		Pass 3	
	Loaded	Read	Loaded	Read	Loaded	Read
00	1010	A0	0001	10	1100	C0
01	0001	10	1100	C0	1010	A0
02	1100	C0	1010	A0	0001	10
03	1010	A0	0001	10	1100	C0
..	....	..	....	..	....	..

91A24 FUNCTION 5 OCCR CNTR

CIRCUIT OVERVIEW

The OCCR CNTR (occurrence counter) function verifies the sequential word recognizer's occurrence counter (on schematic 75) and the RAMs that load it. The occurrence counter is a 12-bit up-counter. The three 16 × 4 bit RAMs that load the counter value are configured as a single 12-bit × 16 deep RAM.

FUNCTION DESCRIPTION

The OCCR CNTR function has five tests. Test 0 verifies that the occurrence counter and each address in the occurrence counter RAM can be loaded. Test 1 verifies that the occurrence counter can count. Test 2 verifies that the occurrence counter RAM will load the counter with the next value when a count is complete. Tests 3 and 4 verify that the 91A24 can trigger.

The occurrence counter is loaded from the occurrence counter RAM. The occurrence counter RAM is loaded by placing the desired address into the stack pointer (U571 on schematic 76), writing the data onto LB0-LB7, and asserting $\overline{OCCR\ CNTR\ RAM\ LD0}$ then $\overline{OCCR\ CNTR\ RAM\ LD1}$ low.

Readback Ports

Tests 0, 1, 3, and 4 results are read back through U771 (port 0E) on schematic 69.

Test 2 results are read back through U771 (port 0E) and U235 (port 04) on schematic 69.

91A24 OCCR CNTR TEST 0 TROUBLESHOOTING

Reading the Test 0 Error Codes

Test 0 of the OCCR CNTR function provides test results like those shown in Figure 7-27.
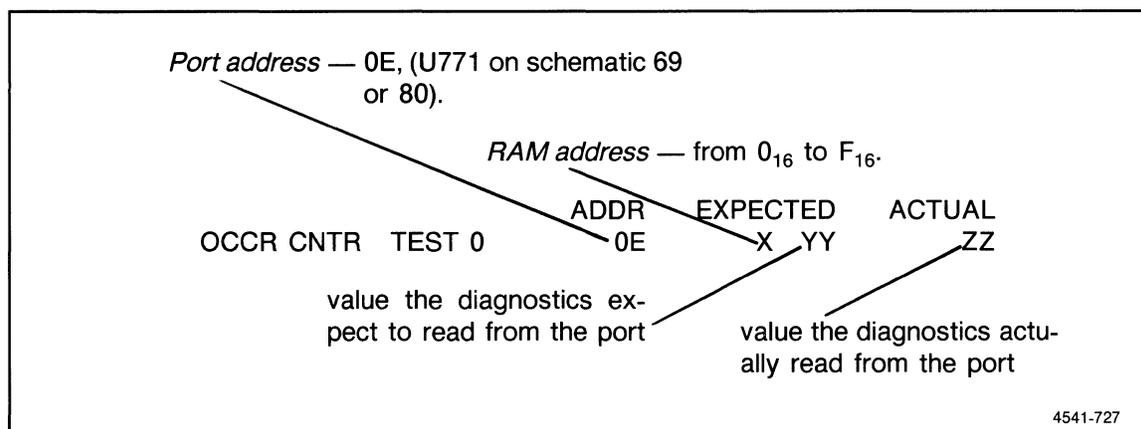
Figure 7-27. OCCR CNTR test 0 readback display. The ACTUAL value is read from the counter. The EXPECTED value depends on the RAM address. Refer to Table 7-11 for expected values.

Error Indication

OCCR CNTR test 0 fails.

Possible Cause	Action
If a 91AE24 is connected to the 91A24, the 91AE24 may cause the failure.	Turn off the DAS. Disconnect interconnect cables from J181 at the top of the 91A24 module. Turn on the DAS and re-run the test. If the test fails with the cables disconnected, the 91A24 is at fault. If the test passes, suspect incorrectly installed interconnect cables or a 91AE24 module.

Error Indication

OCCR CNTR function fails along with CNTR TIMR, MEM ADDR, ACQ MEM, STK PNTR, or WRD REC functions.

Possible Cause	Action
Circuits feeding into OCCR CNTR test are malfunctioning.	Debug according to the failed function with the smallest number.

Error Indication

		ADDR	EXPECTED	ACTUAL
OCCR CNTR	TEST 0	0E	X YY	ZZ

Possible Cause	Action
Occurrence counter RAM chip select malfunction.	Loop test 0. Check U155 pin 2 (on schematic 75) for low; if not low, suspect R753 (on schematic 75).
Write enables malfunctioning.	While test 0 is still looping, check U958 pins 11 and 13 (on schematic 68 for low pulses; if either pin does not show low pulses, suspect U958.
$\overline{\text{OCCR CNTR LD}}$ malfunction.	Check U958 pin 9 (on schematic 68) for low pulses; if none, suspect U958. If low pulses present, check U265A pin 1 (on schematic 75) for high level; if not high, suspect U165 (on schematic 75). If U265A pin 1 is high, check U265A pin 3 for low pulses. If no low pulses, suspect U265.
RAM malfunction.	Check the outputs (pins 5, 7, 9, and 11) of U155, U255, and U55 (on schematic 75) for toggling signals. Suspect any RAM with non-toggling outputs.
Counter malfunction.	Check the outputs (pins 2, 5, 9, and 12) of U158, U258, and U458 (on schematic 75) for toggling signals. Suspect any counter with non-toggling outputs.
Readback circuitry malfunctioning.	Check U998 pin 16 (on schematic 69) for low pulses; if none, suspect U998. If low pulses present, check that OCCR1-OCCR3 inputs to U771 (on schematic 69) match outputs of U771 during low pulses on U771 pin 1. If inputs to U771 do not match the corresponding outputs, suspect U771.

91A24 OCCR CNTR TEST 0 DESCRIPTION
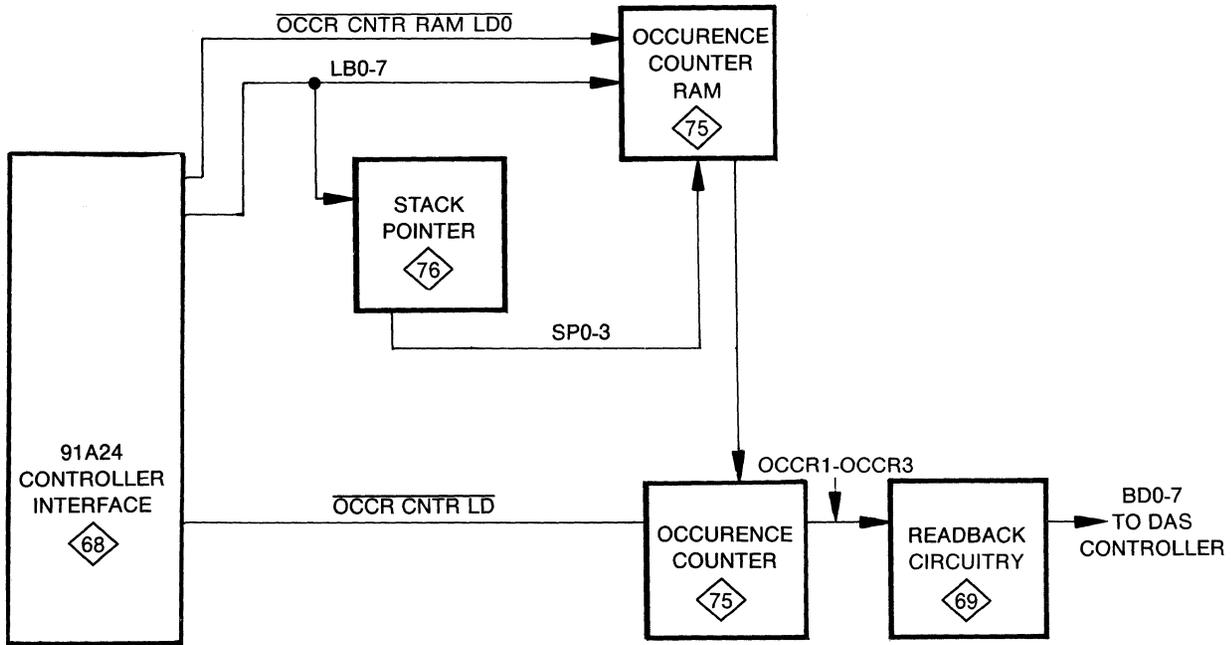
4541-728

Figure 7-28. Blocks of the 91A24 tested by the OCCR CNTR function, test 0.

OCCR CNTR test 0 checks the occurrence counter RAM and verifies that the occurrence counters can be loaded. This is done by loading the RAM with 16 patterns and then loading these patterns into the occurrence counters to be read. Only three bits are read back from the occurrence counters, so the patterns used in the diagnostic routine cause these three lines to increment from 0 to 7 twice. The patterns also toggle all the bits that the DAS cannot read, so they can be observed with a scope.

Table 7-11 shows the values loaded into each RAM address, and the readback data expected by the DAS. Since the three readback lines are connected to U771 in reverse order and in the middle of the byte, the data read from the port appears reversed as Table 7-11 shows.

Table 7-11
CONTENTS OF OCCURRENCE COUNTER RAM
AND EXPECTED VALUES FOR OCCR CNTR TEST 0

RAM Address	RAM Output			Expected Result	
	11-8	7-4	3-0	Binary	Hex
0	0 1 0 1	0 0 0 1	0 1 0 1	XXX000XX	00
1	1 0 1 0	1 0 1 0	1 0 0 0	XXX001XX	04
2	0 1 0 1	0 1 0 1	0 1 0 1	XXX010XX	08
3	1 0 1 0	1 1 1 0	1 0 0 0	XXX011XX	0C
4	0 1 0 1	0 0 0 1	0 1 1 1	XXX100XX	10
5	1 0 1 0	1 0 1 0	1 0 1 0	XXX101XX	14
6	0 1 0 1	0 1 0 1	0 1 1 1	XXX110XX	18
7	1 0 1 0	1 1 1 0	1 0 1 0	XXX111XX	1C
8	0 1 0 1	0 0 0 1	0 1 0 1	XXX000XX	00
9	1 0 1 0	1 0 1 0	1 0 0 0	XXX001XX	04
A	0 1 0 1	0 1 0 1	0 1 0 1	XXX010XX	08
B	1 0 1 0	1 1 1 0	1 0 0 0	XXX011XX	0C
C	0 1 0 1	0 0 0 1	0 1 1 1	XXX100XX	10
D	1 0 1 0	1 0 1 0	1 0 1 0	XXX101XX	14
E	0 1 0 1	0 1 0 1	0 1 1 1	XXX110XX	18
F	1 0 1 0	1 1 1 0	1 0 1 0	XXX111XX	1C

Test 0 Readback Port

All test 0 results are read through U771 (port 0E) on schematic 69.

Test 0 Initial Conditions

Before test 0 actually starts, the DAS initializes the 91A24 module as described in the following steps.

1. 80_{16} is written to U761 (on schematic 68 or 79), which makes U761 pin 15 (DUAL QUAL) high and pin 19 ($\overline{\text{STACK PTR LD}}$) low. DUAL QUAL low forces U571 pin 1 (on schematic 76 or 86) high. $\overline{\text{STACK PTR LD}}$ low goes to U571 pin 9 (on schematic 76 or 86) and sets the stack pointer in the load mode.

2. 00_{16} is written to U758 (on schematic 68 or 79), which makes U758 pin 6 ($\overline{\text{STACK CLK EN}}$) low. When $\overline{\text{STACK CLK EN}}$ is low, the stack pointer counter can be clocked through U568C, U485A, and U575D (on schematic 76 or 86).

Test 0 Run Sequence

Test 0 loads values into the occurrence counter RAM. This loading process is described in the next four steps.

1. For each of the 16 passes, an address (0-F_{16}) is written onto D0-D7, and U958 pin 15 (STACK PTR CLK on schematic 68) is asserted. This loads the address into the stack pointer (U571 on schematic 76) and establishes an address for the occurrence counter RAMs (U155, U255, and U455 on schematic 75).

2. The low eight bits of one of the patterns are then written onto D0-D7, and U958 pin 13 (OCCR CNTR RAM LD0 on schematic 68) is asserted. This loads the pattern into the low byte of the RAM (U155 and U255 on schematic 75).

3. The high four bits of the pattern are then written onto D0-D4 and U958 pin 11 (OCCR CNTR RAM LD1 on schematic 68) is asserted. This loads the pattern into RAM U455 (on schematic 75).

4. Steps 1-3 are repeated until all 16 addresses of the occurrence counter RAM are filled.

After the RAM is entirely filled, the DAS reads the values from the RAM through the occurrence counter. Steps 5 through 8 describe this readback process.

5. DAS now reads the contents of the RAM in 16 passes. For each of these passes, an address (0-F_{16}) is written onto D0-D7, and U958 pin 15 (STACK PTR CLK on schematic 68) is asserted.

6. The contents of the occurrence counter RAM at the address loaded in step 5 is then loaded into the occurrence counter (U158, U258, and U458 on schematic 75). The DAS causes this loading by toggling U958 pin 9 (OCCR CNTR LD on schematic 68) low. The low on U958 pin 9 passes through U265 (on schematic 75) to pin 1 of U158, U258, and U458 (on schematic 75), which loads the pattern from the occurrence counter RAM.

7. The DAS then reads the three bits of the pattern that can be read (OCCR1-OCCR3) through U771 (on schematic 69), which is enabled by U998 pin 16 (TRIGGERED RD on schematic 69).

8. Steps 5-7 are repeated until all 16 patterns have been read or until an error is detected.

91A24 OCCR CNTR TEST 1 TROUBLESHOOTING

Reading the Test 1 Error Codes

Test 1 of the OCCR CNTR function provides test results like those shown in Figure 7-29.
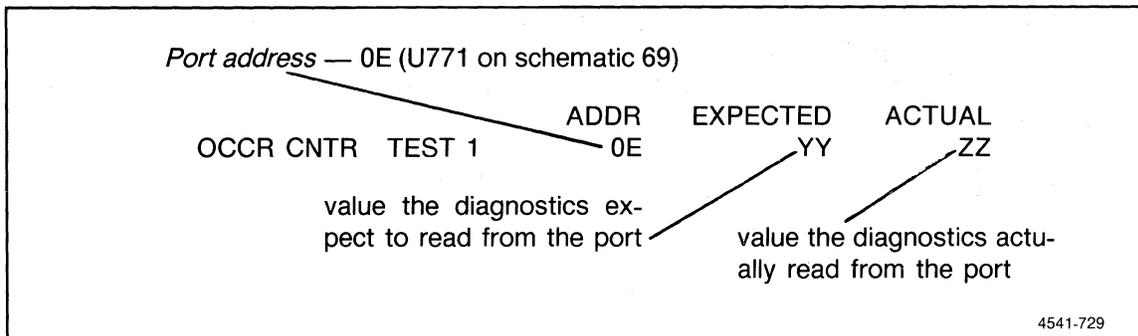
Figure 7-29. OCCR CNTR test 1 readback display. The ACTUAL value is read from the RAM. The EXPECTED value may be 10, 08, or 04.

Error Indication

OCCR CNTR function fails along with CNTR TIMR, MEM ADDR, ACQ MEM, STK PNTR, or WRD REC functions.

Possible Cause	Action
Circuits feeding into OCCR CNTR test are malfunctioning.	Debug according to the failed function with the smallest number.

Error Indication

OCCR CNTR test 1 fails.

Possible Cause	Action
If a 91AE24 is connected to the 91A24, the 91AE24 may cause the failure.	Turn off the DAS. Disconnect interconnect cables from J181 at the top of the 91A24 module. Turn on the DAS and re-run OCCR CNTR test 1. If the test fails with the cables disconnected, the 91A24 is at fault. If the test passes, suspect incorrectly installed interconnect cables or a 91AE24 module.

Error Indication

	ADDR	EXPECTED	ACTUAL
OCCR CNTR TEST 1	0E	YY	ZZ

Possible Cause	Action
$\overline{\text{OCCR CLK}}$ malfunction.	Loop test 1. Check U965 pin 17 (on schematic 68) for low pulses; if none, suspect U965. If low pulses present check U165A pin 5 (on schematic 75) for high pulses. If U165A shows high pulses, then $\overline{\text{OCCR CLK}}$ is okay. Proceed to the next possible cause. If U165A pin 5 is steady low, suspect U165. If U165A pin 5 is steady high, check U165A pin 1 (on schematic 75) for low; if low, suspect U165. If U165A pin 1 is high, check U268B pin 4 (on schematic 75) for low; if low, suspect R266 (also on schematic 75); otherwise suspect U268 (on schematic 75).
Counter malfunction.	Determine from EXPECTED and ACTUAL values which bit is at fault. 1. If bit 4 is bad, suspect U158 (on schematic 75). 2. If bit 3 is bad, suspect U258 (on schematic 75). 3. If bit 2 is bad, suspect U458 (on schematic 75).

91A24 OCCR CNTR TEST 1 DESCRIPTION
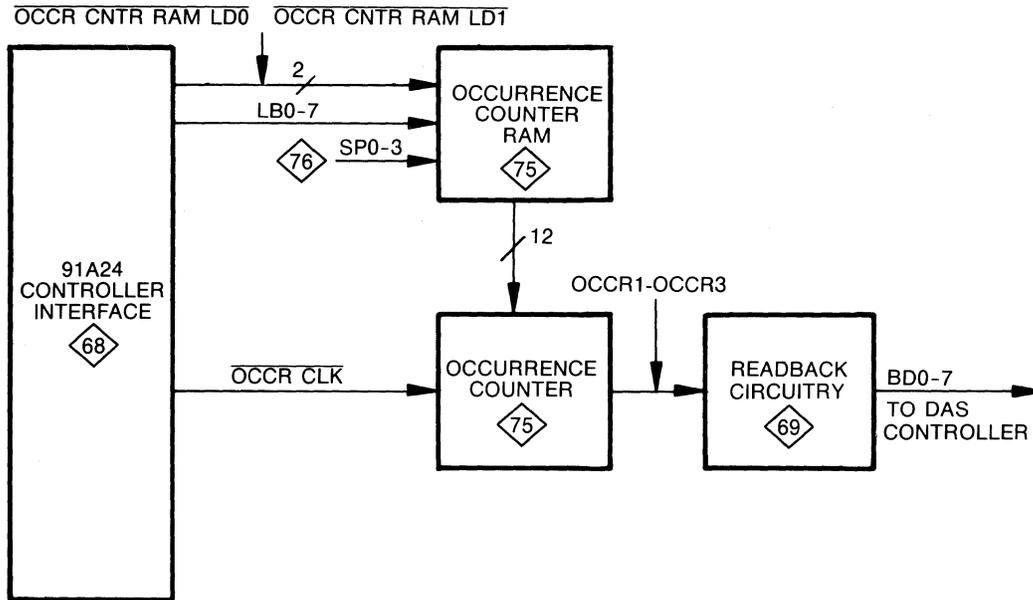
4541-730

Figure 7-30. Blocks of the 91A24 tested by the OCCR CNTR function, test 1.

OCCR CNTR test 1 test checks the occurrence counter's ability to count. This is accomplished by loading 0 into the occurrence counter, clocking the counters to three different values, and reading back the results. The test has three parts:

* First, the counters are loaded with 000_{16}, clocked twice, then checked for 002_{16}.

* Next, the counters are clocked 62 more times, and the counters checked for 040_{16}.

* Last, the counters are clocked 1984 more times, and the counters checked for 800_{16}.

Test 1 Readback Port

All test 1 results are read through U771 (port 0E) on schematic 69.

Test 1 Initial Conditions

Before test 1 runs, the stack occurrence counter RAM address is set to 0_{16}. Then the RAMs are loaded with 000_{16} at that address. Finally the 000_{16} in the RAMs is loaded into the occurrence counter, so it will start its count from 000_{16}.

The first two steps are performed as initial conditions to test 0, but they remain true in test 1 and are required for the test to pass.

1. 80_{16} is written to U761 (on schematic 68 or 79), which makes U761 pin 15 (DUAL QUAL) high and pin 19 ($\overline{\text{STACK PTR LD}}$) low. DUAL QUAL low forces U571 pin 1 (on schematic 76 or 86) high. $\overline{\text{STACK PTR LD}}$ low goes to U571 pin 9 (on schematic 76 or 86) and sets the stack pointer in the load mode.

2. 00_{16} is written to U758 (on schematic 68 or 79), which makes U758 pin 6 ($\overline{\text{STACK CLK EN}}$) low. When $\overline{\text{STACK CLK EN}}$ is low, the stack pointer counter can be clocked through U568C, U485A, and U575D (on schematic 76 or 86).

The remaining initial conditions are set immediately before test 1 begins.

3. 00_{16} is written onto D0-D7 and U958 pin 15 ($\overline{\text{STACK PTR CLK}}$ on schematic 68) is asserted. This loads the stack pointer (U571 on schematic 76) with 0s.

4. The low byte of the occurrence counter RAM is loaded with 00_{16} by writing FF_{16} onto D0-D7 and asserting U958 pin 13 ($\overline{\text{OCCR CNTR RAM LD0}}$ on schematic 68). FF_{16} is inverted by the occurrence counter RAM to produce 0s on the RAM outputs.

5. The high four bits of the occurrence counter RAM are loaded with 0s by writing FF_{16} onto D0-D7 and asserting U958 pin 11 ($\overline{\text{OCCR CNTR RAM LD1}}$ on schematic 68). FF_{16} is inverted by the occurrence counter RAM (U455 on schematic 75) to produce 0s on the outputs.

6. The occurrence counter (U158, U258, and U458 on schematic 75) is then loaded with the 0s that were loaded into the RAM in steps 2 and 3. The counter is loaded by writing 00_{16} to U958 pin 9 ($\overline{\text{OCCR CNTR LD}}$ on schematic 68).

Test 1 Run Sequence

After the counter is loaded with 000_{16}, it is clocked and the clocked value is read for comparison with the expected value.

1. The occurrence counter is clocked to 002_{16} by writing to port 1F twice ($\overline{\text{OCCR CLK}}$, U965 pin 17 on schematic 68). This causes two low pulses on U165A pins 4 and 5 which clocks U158 pin 8 (all on schematic 75).

2. The three bits that can be read from the occurrence counter (OCCR1-OCCR3) are then read from U771 (on schematic 69) and compared to the expected value. If an error is detected, the test will stop here.

3. The occurrence counter is then clocked to 040_{16} by writing to port 1F 62 more times ($\overline{\text{OCCR CLK}}$, U965 pin 17 on schematic 68).

4. The occurrence counter is again read as in step 2, and if an error is detected here, the test stops.

5. The occurrence counter is clocked to 800_{16} by writing to port 1F 1984 more times ($\overline{\text{OCCR CLK}}$, U965 pin 17 on schematic 68).

6. The occurrence counter is read as in step 2, and this value is compared to the expected value.

91A24 OCCR CNTR TEST 2 TROUBLESHOOTING

Reading the Test 2 Error Codes

Test 2 of the OCCR CNTR function provides test results like those shown in Figure 7-31.
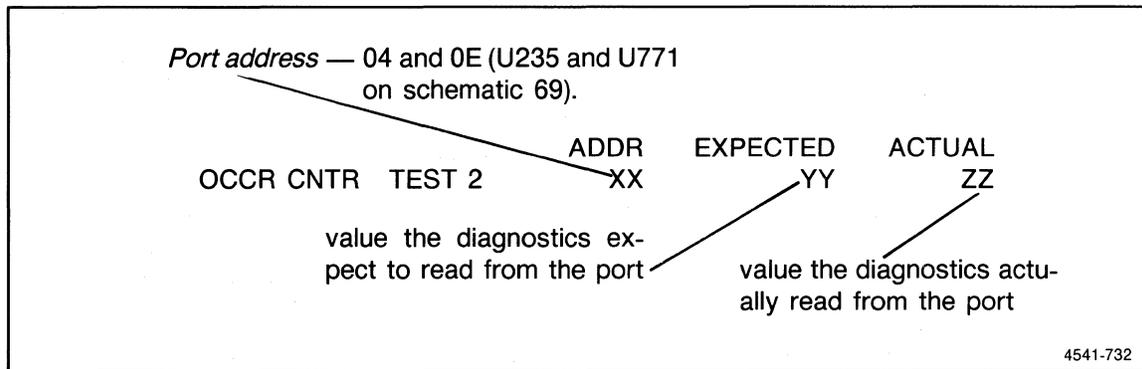
Figure 7-31. OCCR CNTR test 2 readback display. The ACTUAL value is read from the counter. The EXPECTED value is 04 from port 04, and 08 from port 0E.

Error Indication

OCCR CNTR function fails along with CNTR TIMR, MEM ADDR, ACQ MEM, STK PNTR, or WRD REC functions.

Possible Cause	Action
Circuits feeding into OCCR CNTR test are not functional.	Debug according to the failed function with the smallest number.

Error Indication

OCCR CNTR Test 2 fails.

Possible Cause	Action
If a 91AE24 is connected to the 91A24, the 91AE24 may cause the failure.	Turn off the DAS. Disconnect interconnect cables from J171 and J181 at the top of the 91A24 module. Turn on the DAS and re-run the test. If the test fails with the cables disconnected, the 91A24 is at fault. If the test passes, suspect incorrectly installed interconnect cables or a 91AE24 module.

Error Indication

		ADDR	EXPECTED	ACTUAL
OCCR CNTR	TEST 2	04	01	00

Possible Cause	Action
POINTER CLK malfunction.	Loop test 2. Check U165B pin 8 (on schematic 75) for high pulses. If high pulses are present, POINTER CLK is okay. Continue to the next possible cause. If high pulses are not present, check U165B pin 13 (on schematic 75) for a steady high. If signal is steady high, go to the next paragraph. If U165B pin 13 is not steady high, trace signal back through U471B (on schematic 76) to find the problem. If U165 pin 13 is static high, check U165B pin 10 (on schematic 75) for low pulses. If no low pulses on U165B pin 10, trace through U265A (schematic 75) and U265A (also in schematic 75) to correct; otherwise suspect U165 (on schematic 75).
$\overline{\text{POINTER INC}}$ malfunction.	With test 2 still looping, check U161 pin 9 (on schematic 75) for toggling signal. If signal is steady low, suspect U161 (on schematic 75). If U161 pin 9 is steady high, check U161 inputs for a steady low. Suspect any input that is steady low.

Error Indication

		ADDR	EXPECTED	ACTUAL
OCCR CNTR	TEST 2	0E	YY	ZZ

Possible Cause	Action
Counter won't load itself.	Loop test 2. Check U165B pin 9 (on schematic 75) for low pulses; if none, suspect U165. Check for low pulses on U265A pin 1; if none, suspect DL195 (on schematic 75). Check for low pulses on U265A pin 3; if none, suspect U265 (on schematic 75).

91A24 OCCR CNTR TEST 2 DESCRIPTION
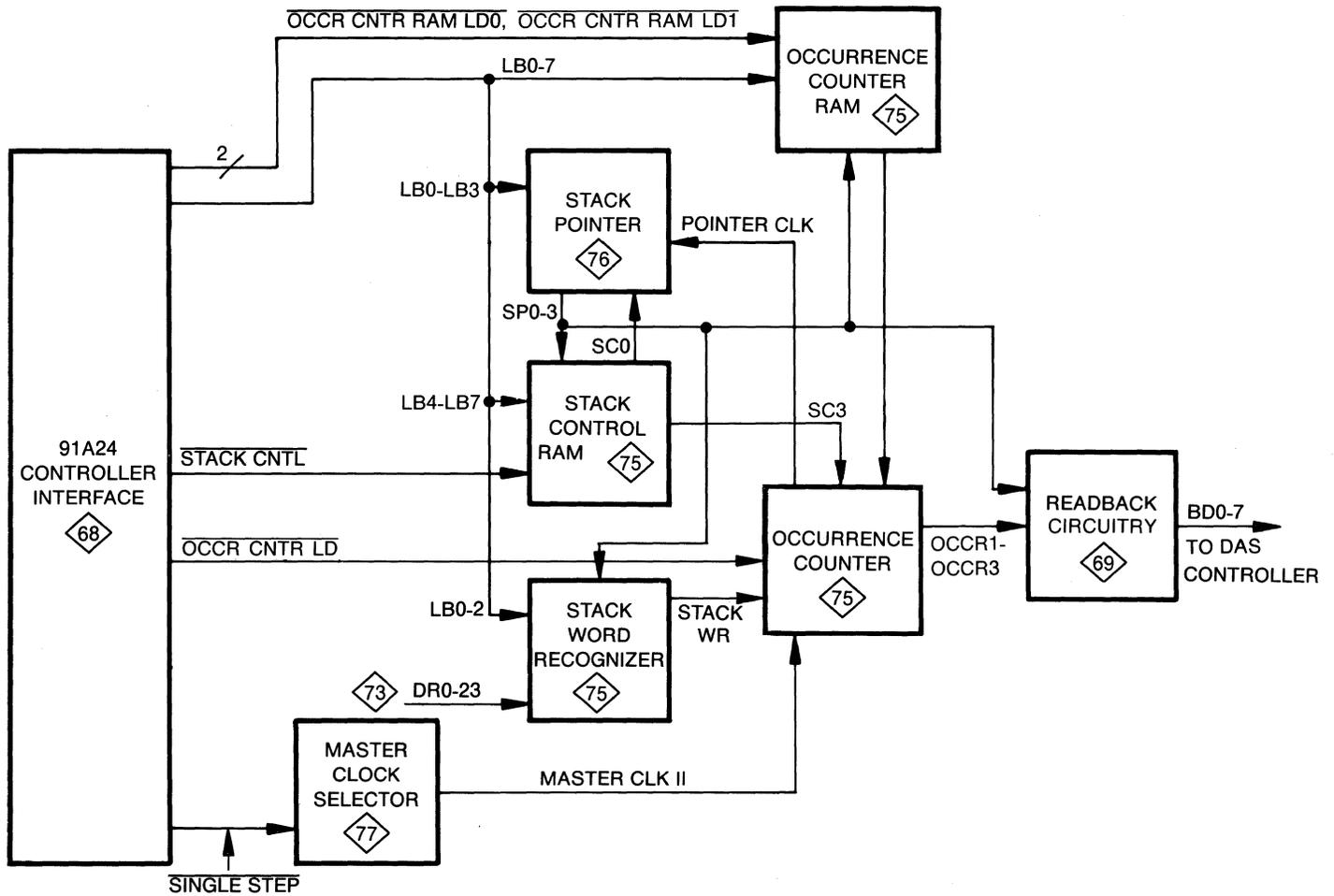
4541-733

Figure 7-32. Blocks of the 91A24 tested by the OCCR CNTR function, test 2.

OCCR CNTR test 2 checks the ability of the occurrence counter to load itself from the occurrence counter RAM. This is done by:

1. loading address 0_{16} of the occurrence counter RAM with FFF_{16},
2. loading address 1_{16} of the occurrence counter RAM with FBF_{16},
3. setting the stack pointer to 0_{16},
4. clocking the occurrence counter,
5. then reading the counter and comparing the value to the value loaded into occurrence counter RAM address 1_{16}.

Test 2 Readback Port

Test 2 results are read through U771 (port 0E) and U235 (port 04) on schematic 69.

Test 2 Initial Conditions

The first two steps are performed as initial conditions to test 0, but they remain true in test 2 and are required for the test to pass.

1. 80_{16} is written to U761 (on schematic 68 or 79), which makes U761 pin 15 (DUAL QUAL) high and pin 19 ($\overline{\text{STACK PTR LD}}$) low. DUAL QUAL low forces U571 pin 1 (on schematic 76 or 86) high. $\overline{\text{STACK PTR LD}}$ low goes to U571 pin 9 (on schematic 76 or 86) and sets the stack pointer in the load mode.

2. 00_{16} is written to U758 (on schematic 68 or 79), which makes U758 pin 6 ($\overline{\text{STACK CLK EN}}$) low. When $\overline{\text{STACK CLK EN}}$ is low, the stack pointer counter can be clocked through U568C, U485A, and U575D (on schematic 76 or 86).

The remaining initial condition is set immediately before test 2 begins.

3. The internal master clock is selected on all 91A24s and 91AE24s in the DAS by writing 80_{16} to D0-D7 and asserting U965 pin 8 (PC4 on 91A24 schematic 68 and 91AE24 schematic 79).

Test 2 Run Sequence

The stack pointer on all 91A24 and 91AE24 modules is set to 0_{16}, as shown in steps 1 through 4. Step 3 also sets the stack word recognizer address (DR0-DR23) to 00_{16}.

1. 00_{16} is written to U758 (on schematics 68 and 79) on all 91A24 and 91AE24 modules in the DAS. This asserts $\overline{\text{STACK CLK EN}}$, which sets U485A pin 2 (on schematics 76 and 86) low, to enable clocking the stack pointer (U571 on schematics 76 and 86).

2. $A0_{16}$ is written to U761 (on schematics 68 and 79) on all 91A24 and 91AE24 modules in the DAS. This sets U571 pin 9 (on schematics 76 and 86) low, to enable loading the stack pointer.

3. The data registers (DR0-DR23 on schematics 73 and 84) on all of the 91A24 and 91AE24 modules in the DAS are initialized to 00_{16} by writing 00_{16} onto D0-D7 and asserting U958 pin 10 ($\overline{\text{SINGLE STEP}}$ on schematics 68 and 79) twice. This sets the address of stack word recognizer RAMs U148, U248, and U448 to 00_{16}.

4. The stack pointers on all of the 91A24 and 91AE24 modules are set to 0_{16} by writing 00_{16} onto D0-D7 and asserting U958 pin 15 ($\overline{\text{STACK PTR CLK}}$ on schematics 68 and 79).

In steps 5, 6, and 7 values are loaded into the stack control RAM at address 0, the occurrence counter RAMs at address 0, and the stack word recognizers.

5. The stack control RAM (U555 on schematics 75 and 86) on all 91A24 and 91AE24 modules is set to F_{16} by writing 0_{16} on LB4-LB7 and asserting U958 pin 8 ($\overline{\text{STACK CNTL}}$ on schematics 68 and 79). The RAM inverts this 0_{16} to produce F_{16} on its outputs.

6. The outputs of the stack word recognizers (U148, U248, and U448 on schematics 75 and 86) on all 91A24 and 91AE24 modules are set high by writing 07_{16} to D0-D7 and asserting U958 pins 5, 6, and 7 ($\overline{\text{STACK A WE}}$, $\overline{\text{STACK B WE}}$, and $\overline{\text{STACK C WE}}$ on schematics 68 and 79). This sets U168A pin 12 (on schematics 75 and 86) high on all of the modules.

7. The occurrence counter RAM (U155, U255, and U455 on schematic 75) has FFF_{16} loaded at address 0_{16} by writing 000_{16} onto LB0-LB7 and asserting U958 pins 13 and 11 ($\overline{\text{OCCR CNTR RAM LD0}}$ and $\overline{\text{OCCR CNTR RAM LD1}}$ on schematic 68). These 0s are inverted to produce Fs at the RAM output.

In steps 8, 9, 10, and 11 the stack pointer is incremented to 1_{16}. With the new stack pointer value, data is loaded into the stack control RAM at address 1_{16}, the occurrence counter RAMs at address 1_{16}, and the stack word recognizers.

8. The stack pointers (U571 on schematics 76 and 86) on all 91A24 and 91AE24 modules are incremented to 1_{16} by toggling U958 pin 15 ($\overline{\text{STACK PTR CLK}}$ on schematics 68 and 79) low.

9. The stack control RAMs (U555 on schematics 75 and 86) on all 91A24 and 91AE24 modules are set to F_{16} by writing 00_{16} onto LB4-LB7 and asserting U958 pin 8 ($\overline{\text{STACK CNTL}}$ on schematics 68 and 79) low. The RAM inverts the loaded 0_{16} to produce F_{16} on its outputs.

10. The outputs of the stack word recognizers (U148, U248, and U448 on schematics 75 and 86) on all 91A24 and 91AE24 modules are set high by writing 07_{16} onto D0-D7 and asserting U958 pins 5, 6, and 7 ($\overline{\text{STACK A WE}}$, $\overline{\text{STACK B WE}}$, and $\overline{\text{STACK C WE}}$ on schematics 68 and 79) low. This sets U168A pin 12 (on schematics 75 and 86) high on all of the modules.

11. The occurrence counter RAM (U155, U255, and U455 on schematic 75) is loaded with 040_{16} at address 1_{16} by writing BF_{16} onto D0-D7 and asserting U958 pin 13 ($\overline{\text{OCCR CNTR RAM LD0}}$ on schematic 68) and then writing FF_{16} onto D0-D7 and asserting U958 pin 11 ($\overline{\text{OCCR CNTR RAM LD1}}$ on schematic 68). This pattern is inverted by the RAM outputs to produce 040_{16}.

Now that all necessary RAM addresses are loaded, the stack pointer is re-initialized, the occurrence counter is loaded with FFF_{16}, and the occurrence counter is prepared to increment. This is described in steps 12 through 15.

12. The stack pointers on all 91A24 and 91AE24 modules are set to 0_{16} again by setting U958 pin 15 low ($\overline{\text{STACK PTR CLK}}$ on schematic 68).

13. The occurrence counter (U158, U258, and U458 on schematic 75) is loaded with FFF_{16} from address 0 in the occurrence counter RAM by toggling U958 pin 9 low ($\overline{\text{OCCR CNTR LD}}$ on schematic 68).

14. $F0_{16}$ written to U761 (on schematics 68 and 79) on all 91A24 and and 91AE24 modules. This makes U761 pin 19 ($\overline{\text{STACK PTR LD}}$) high, which pulls U571 pin 9 high (on schematics 76 and 86) to enable the stack pointer to count.

15. 01_{16} is written to U758 (on schematics 68 and 79) on all 91A24 and 91AE24 modules. This makes U758 pin 6 ($\overline{\text{STACK CLK EN}}$) high, which pulls U485A pin 2 high (on schematics 68 and 79) to enable POINTER CLK through U575D (on schematics 76 and 86).

Finally, the test is ready to run. The $\overline{\text{SINGLE STEP}}$ clock increments the the stack pointer and loads a new value from address 1_{16} of the occurrence counter RAM into the counter. Step 16 describes the sequence of events.

16. U958 pin 10 ($\overline{\text{SINGLE STEP}}$ on schematic 68) is toggled low, to clock U165B pin 11 (on schematic 75). This causes a high pulse on U165B pin 8 (POINTER CLK on schematic 75). This increments the stack pointer (U571 on schematic 76) from 0_{16} to 1_{16}. The new pointer value changes the occurrence counter RAM address to 1_{16}.

When POINTER CLK goes high, U165B produces a low pulse which passes through U265A, to load the occurrence counter with the data from address 1_{16} of the occurrence counter RAM. This low pulse is also applied to U165B pin 10, to SET flip-flop U165B back to its default condition.

The remainder of the test reads the stack pointer and occurrence counter values to see if the test was successful.

17. The stack pointer (U571 on schematic 76) is read to ensure that it incremented to 1_{16}. The stack pointer is read through U235 (on schematic 69). If the stack pointer is not at 1_{16}, an error is displayed from readback port 04 with an expected value of 04, and the test stops.

18. If the expected value was read in step 17, then the occurrence counter is read through U771 (on schematic 69). The read value is compared to the pattern (040_{16}) loaded into address 1_{16} of the occurrence counter RAM. If an unexpected value is read, an error is displayed from readback port 0E with an expected value of 08.

91A24 OCCR CNTR TEST 3 TROUBLESHOOTING

Reading the Test 3 Error Codes

Test 3 of the 91A24 OCCR CNTR function provides test results like those shown in Figure 7-33.
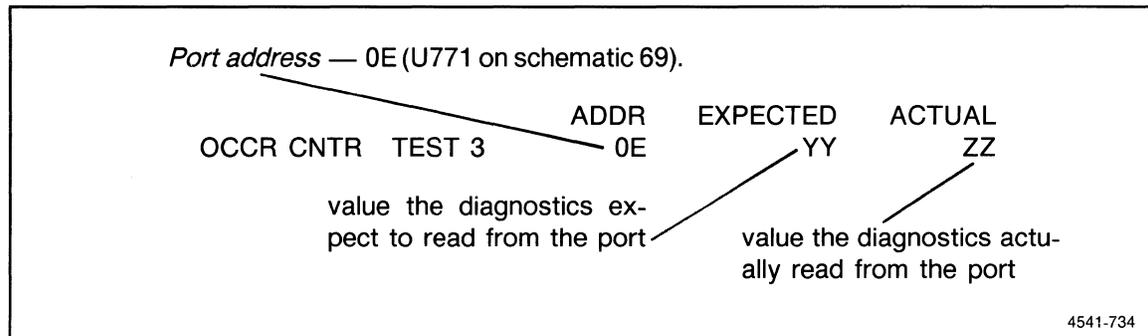
Figure 7-33. OCCR CNTR test 3 readback display. The ACTUAL value is read from the counter. The EXPECTED values are 00 and 02.

Error Indication

		ADDR	EXPECTED	ACTUAL
OCCR CNTR	TEST 3	0E	02	00

Possible Cause	Action
91A24 INIT malfunction.	Loop test 3. Check U761 pin 12 (on schematic 68) for low pulses; if none, suspect U761 (on schematic 68).
Triggered flip-flop malfunction.	With test 3 still looping, check U798 pins 9 and 5 (on schematic 76) for high level; if not high level suspect U798.
Readback circuitry malfunction.	Check U771 pin 8 (on schematic 69) for high whenever U771 pin 1 is low. If high, suspect U771.

Error Indication

		ADDR	EXPECTED	ACTUAL
OCCR CNTR	TEST 3	0E	00	02

Possible Cause	Action
91A24 INIT malfunction.	Loop test 3. Check U761 pin 12 (on schematic 68) for low pulses; if none, suspect U761.
POINTER INC malfunction.	With test 3 still looping, check U265D pin 12 (on schematic 76) for high or pulses. If neither high nor pulsing, suspect U268 or U161 (on schematic 75). If high or pulsing, check U265D pin 11 (on schematic 76) for low pulses; if none, suspect U265.
NEVER TRIG malfunction.	Check U758 pin 2 (on schematic 68) for low pulses; if low pulses not present, suspect U758.
U481A malfunction.	Check U481A pin 5 (on schematic 76) for low or low pulses; if none, suspect U481.
TRIG CLK malfunction.	Check U481B pin 8 (schematic 74) for low pulses. If no low pulses, suspect U481B or U578B and C (on schematic 74).
U475A malfunction.	Check U475A pin 3 (on schematic 76) for low or low pulses; if none, suspect U475; otherwise suspect U798 (on schematic 76).
Readback circuitry malfunction.	See if U771 pins 8 and 12 (on schematic 69) are at the same state while U771 pin 1 is low. If they have different states, suspect U771.

91A24 OCCR CNTR TEST 3 DESCRIPTION
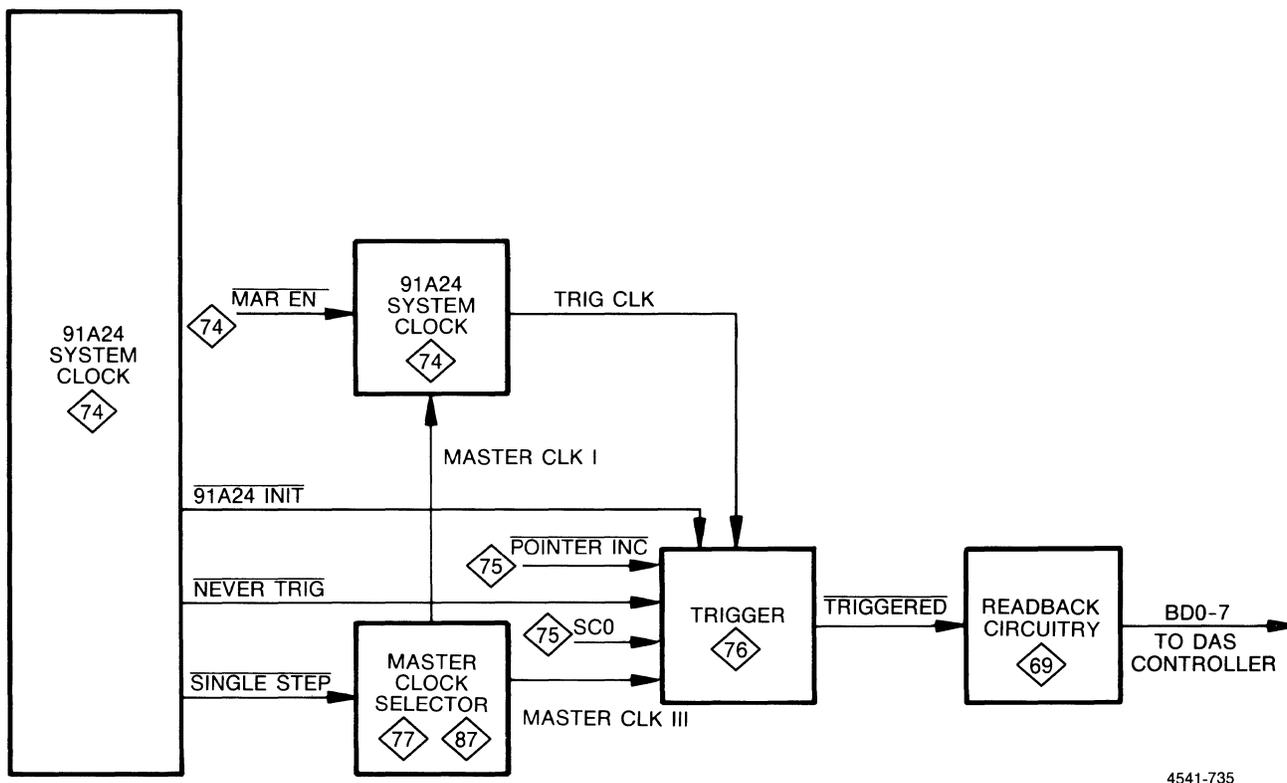
Figure 7-34. Blocks of the 91A24 tested by the OCCR CNTR function, test 3.

OCCR CNTR test 3 checks the triggered flip-flop, (U798A and B on schematic 76) to ensure that the 91A24 stack word recognizer can trigger and assert the TRIGGERED signal (on schematic 76). First the TRIGGERED signal is set high by resetting 91A24 INIT low, which sets U798 (on schematic 76). TRIGGERED is then read to ensure that the module has not triggered. Then the stack word recognizer trigger is asserted, the 91A24 is clocked twice, and TRIGGERED (on schematic 76) is checked for a low (triggered) state.

Test 3 Readback Port

Test 3 results are read through U771 (port 0E) on schematic 69.

Test 3 Initial Conditions

1. The internal single-step clock is selected by writing 80_{16} onto D0-D7 and asserting PC4 (U965 pin 8 on schematic 68).

2. 90_{16} is written to LB0-LB7 and U958 pin 8 (STACK CNTL on schematic 68) is asserted. This resets SC0 from U555 (on schemtic 75) low so that the stack pointer (U571 on schematic 76) will not increment.

3. The outputs of the occurrence counter RAMs (U155, U255, and U455 on schematic 75) are set high by writing 00_{16} to ports 0A and 0B (OCCR CNTR RAM LD1 and OCCR CNTR RAM LD0 from U958 on schematic 68).

4. The occurrence counter (U158, U258, and U458 on schematic 75) is loaded with FFF_{16} from the occurrence counter RAM by writing to port 08 ($\overline{\text{OCCR CNTR LD}}$, U958 pin 9 on schematic 68).

5. The acquisition memory data registers (U128, U228, and U428) are loaded with zeros by writing 00_{16} three times to LB0-LB7 and asserting U958 pin 10 ($\overline{\text{SINGLE STEP}}$ on schematic 68).

6. U168 pin 12 (on schematic 75) is made low by writing 00_{16} to U958 pin 5 ($\overline{\text{STACK A WE}}$ on schematic 68). This, along with the low from SC3 (U555 pin 11 on schematic 75) makes U291C pin 8 low (on schematic 75).

Test 3 Run Sequence

After the initialization is complete, the test is set up in steps 1 through 4.

1. $B0_{16}$ is written to U761 (on schematic 68). This makes $\overline{\text{91A24 INIT}}$ low to set U298A, U798A and U798B (on schematic 76).

   The $B0_{16}$ to U761 also sets MEM RD high, which makes $\overline{\text{MAR EN}}$ (from U288 on schematic 74) low. Due to the lows on $\overline{\text{MAR EN}}$, ENABLE TRIG, and CS3, and the highs on the occurrence counter outputs, $\overline{\text{POINTER INC}}$ (from U161 pin 9 on schematic 75) goes low.

2. 03_{16} is written to U758 (on schematic 68) to make $\overline{\text{NEVER TRIG}}$ low.

3. $F0_{16}$ is written to U761 (on schematic 68). This makes U761 pin 12 ($\overline{\text{91A24 INIT}}$) high so that U798 (on schematic 76) is not held in the set condition. In addition, DUAL QUAL is set high, which sets $\overline{\text{OR TRIGGER}}$ high.

4. $0B_{16}$ is written to U758 (on schematic 68). This makes U758 pin 2 ($\overline{\text{NEVER TRIG}}$) high to enable U481A (on schematic 76).

Now the test starts. There are two parts to the test. In the first part, steps 5, 6 and 7 make sure that the trigger signal is not premature. In the second part, steps 8 and 9 verify that a trigger is indicated when expected.

5. $\overline{\text{TRIGGERED}}$ is read from U771 pin 12 (on schematic 69). $\overline{\text{TRIGGERED}}$ should be high, because U798A (on schematic 76) was set by the $\overline{\text{91A24 INIT}}$ signal.

6. The 91A24 is then clocked by writing to address 09 ($\overline{\text{SINGLE STEP}}$, U958 pin 10 on schematic 68). $\overline{\text{SINGLE STEP}}$ drives the TRIG CLK signal which clocks a low from U475A (on schematic 76) into U798B (also on schematic 76).

7. U771 (on schematic 69) is then read to ensure that bit 1 ($\overline{\text{TRIGGERED}}$) is high. If it is low, the test stops with an error message.

8. The 91A24 is again clocked by writing to address 09 ($\overline{\text{SINGLE STEP}}$, U958 pin 10 on schematic 68). This clocks a low from U798B into U798A (both on schematic 76), resetting $\overline{\text{TRIGGERED}}$ low.

9. U771 (on schematic 69) is again read to ensure that bit 1 ($\overline{\text{TRIGGERED}}$) is low. If the bit is high the DAS reports an error.

91A24 OCCR CNTR TEST 4 TROUBLESHOOTING

Reading the Test 4 Error Codes

Test 4 of the OCCR CNTR function provides test results like those shown in Figure 7-35.

Port address — 0E (U771 on schematic 69)

OCCR CNTR TEST 4   ADDR 0E   EXPECTED YY   ACTUAL ZZ

value the diagnostics expect to read from the port

value the diagnostics actually read from the port

4541-736
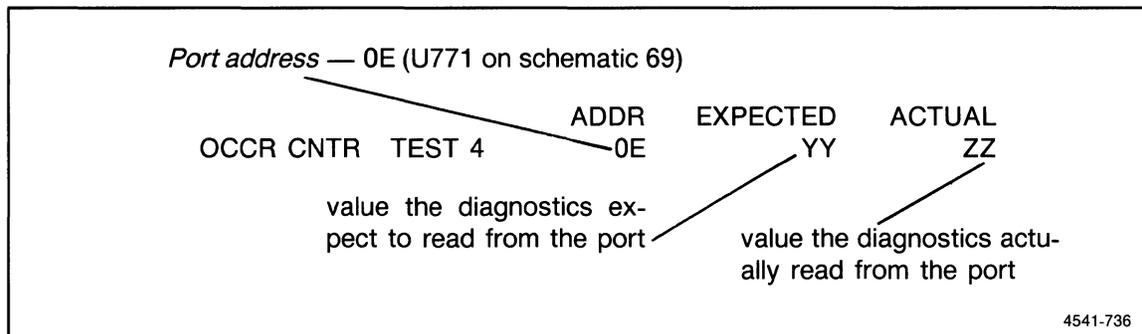
Figure 7-35. OCCR CNTR test 4 readback display. The ACTUAL value is read from the RAM. The EXPECTED value may be 00, 02.

Error Indication

	ADDR	EXPECTED	ACTUAL
OCCR CNTR TEST 4	0E	00	02

Possible Cause	Action
DUAL QUAL malfunction.	Loop test 4. Check U761 pin 15 (on schematic 68) for low; if not low, suspect U761.
TN2 malfunction.	While test 4 is still looping, check U765 pin 15 (on schematic 68) for low; if not low, suspect U765.
OR TRIGGER malfunction.	Check U198A pin 3 (on schematic 74) for low. If not low, check U198A pin 2 for low; if pin 2 is low, suspect U198.
U298A malfunction.	Check U298A pin 5 (on schematic 76) for low or low pulses; if low, suspect U475 (on schematic 76). If high, check U298A pin 2 (on schematic 76) for low or low pulses; if low, suspect U298. Otherwise suspect U575A (on schematic 76).

91A24 OCCR CNTR TEST 4 DESCRIPTION
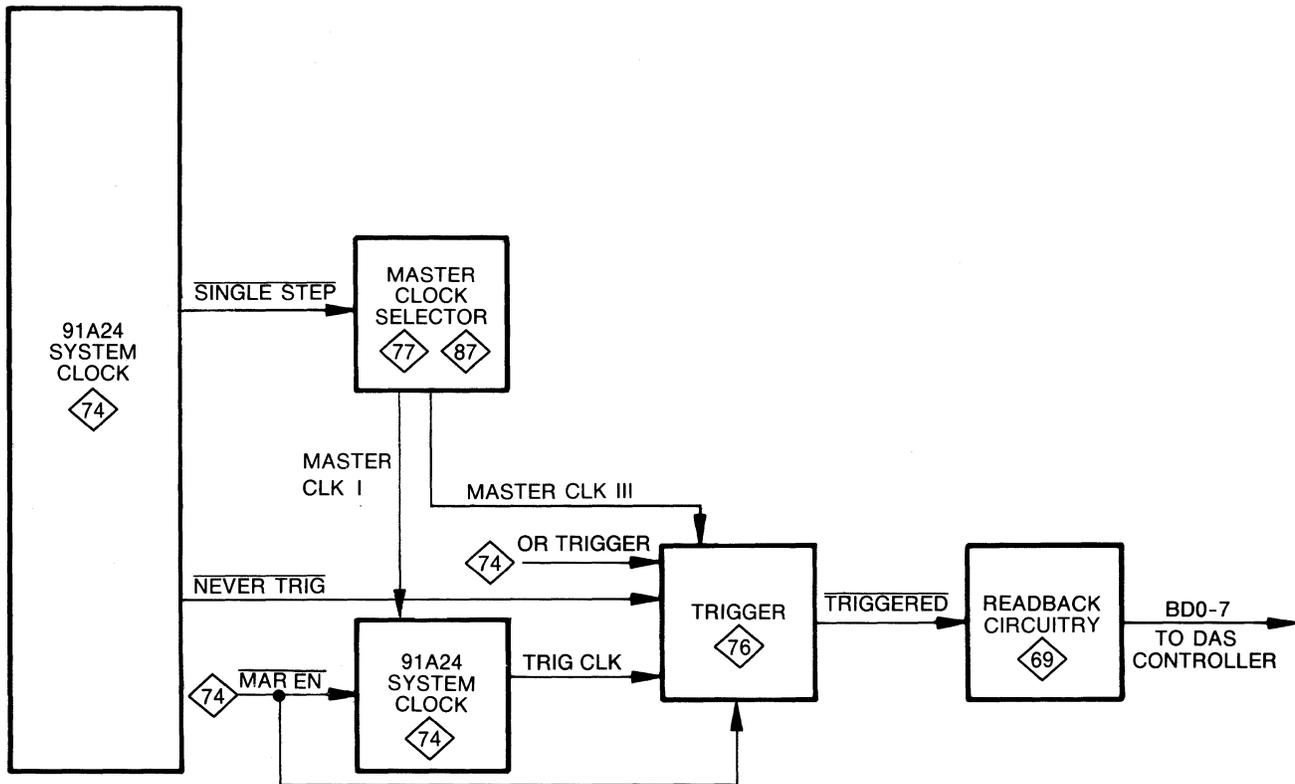
4541-738

Figure 7-36. Blocks of the 91A24 tested by the OCCR CNTR function, test 4.

OCCR CNTR test 4 test checks the triggered flip-flop (U798A and B on schematic 76) to ensure that the 91A24 can trigger and assert TRIGGERED (on schematic 76) low by way of the OR trigger mode. First, the TRIGGERED line is set high by resetting 91A24 INIT low, which sets U798 (on schematic 76). TRIGGERED is then read to ensure that it is not triggered. Then the 91A24 is set to a state where it will trigger using the OR trigger mode, clocked twice, and checked for a triggered state.

Test 4 Readback Port

Test 4 results are read through U771 (port 0E) on schematic 69.

Test 4 Initial Conditions

The internal single-step clock is selected by writing 80_{16} to U945 (on schematic 77) and toggling U965 pin 8 (PC4 on schematic 68).

Test 4 Run Sequence

After the 91A24 module is initialized, the test begins. Steps 1 through 4 set up the test.

1. 07_{16} is written to U765 (on schematic 68). This makes TN2 low, which makes OR TRIG from U291D (on schematic 74) low.

2. 30_{16} is written to U761 (on schematic 68). This makes U761 pin 12 ($\overline{\text{91A24 INIT}}$) low to set flip-flops U298A and U798A and B (on schematic 76). $\overline{\text{91A24 INIT}}$ also sets U488A (on schematic 74) so the $\overline{\text{MAR EN}}$ output of U288 (schematic 74). The 30_{16} also makes U761 pin 15 (DUAL QUAL on schematic 68) low. DUAL QUAL pulls U198A pin 1 low (on schematic 74) to make $\overline{\text{OR TRIGGER}}$ low.

3. 13_{16} is written to U758 (on schematic 68). This sets U758 pin 2 ($\overline{\text{NEVER TRIG}}$) low.

4. 70_{16} is written to U761 (on schematic 68). This makes U761 pin 12 ($\overline{\text{91A24 INIT}}$) high so that U798 (on schematic 76) is not held set.

Now the test starts. The first part, steps 5 and 6, makes sure that the trigger signal is not premature. The second part, steps 7 and 8, verify that a trigger is indicated when expected.

5. U771 (on schematic 69) is read to ensure that bit 1 ($\overline{\text{TRIGGERED}}$) is high. If it is low, the test stops with an error message.

6. The 91A24 is clocked by writing to port 09 ($\overline{\text{SINGLE STEP}}$, U958 pin 10 on schematic 68). $\overline{\text{SINGLE STEP}}$ pulses TRIG CLK (on schematic 74) which clocks a low from U475A (from schematic 76) into U798B (also on schematic 76).

7. U771 (on schematic 69) is again read to ensure that bit 1 ($\overline{\text{TRIGGERED}}$) is high. If it is low, the test stops with an error message.

8. The 91A24 is again clocked by writing to port 09 ($\overline{\text{SINGLE STEP}}$, U958 pin 10 on schematic 68). This clocks a low from U798B into U798A (both on schematic 76), resetting $\overline{\text{TRIGGERED}}$ low.

9. U771 (on schematic 69) is read a last time to ensure that bit 1 ($\overline{\text{TRIGGERED}}$) is low. If the bit is high the DAS reports an error.

91A24 FUNCTION 6 DAC THRSH
91AE24 FUNCTION 4 DAC THRSH

CIRCUIT OVERVIEW

The DAC THRSH (DAC threshold) function tests the circuitry that controls the thresholds for the three acquisition probes. Schematic 71 shows the 91A24 threshold control circuitry. Schematic 82 shows the corresponding circuits on the 91AE24. The threshold circuit is a monolithic digital-to-analog converter (U918) and an op amp (U808C) which acts as an inverting buffer. There are also six more op amps (U711A, B, C, and D and U808A and D) that adjust the voltage from the DAC to match the requirements of the probes. For more information about this circuit refer to *Probe Interface* in the *Theory of Operation* section.

FUNCTION DESCRIPTION

The DAS cannot read back from the DAC circuitry, so you must connect a DMM or oscilloscope to TP910 on the module for test results. The function sets the DAC to three different voltages, then sweeps the output voltage with a ramp. Select the test voltage in the DAC THRESHOLD SET field with the SELECT key.

Setting the DAC Voltage. The controller interface loads the DAC by placing a hexadecimal value on D0-D7 and toggling the $\overline{\text{THRESHOLD}}$ signal.

Test Points. The DAC output is tested at TP910. The first half of the three output buffer circuits can be tested at TP707, TP711, and TP808. The second half of the output buffer circuits can be tested at U711 pins 1 and 7 and at U808 pin 1.

91A24 AND 91AE24 DAC THRSH TROUBLESHOOTING

Error Indication

Threshold of all three probes is stuck at the same voltage regardless of menu setting.

Possible Cause	Action
$\overline{\text{THRESHOLD}}$ signal is stuck.	Set the DAC THRSH function to RAMPING. With an oscilloscope, monitor U918 pin 10 (on schematic 71 or 82). If the signal is not toggling at TTL levels, suspect U958 ($\overline{\text{THRESHOLD}}$'s source on schematic 68 or 79).
DAC has failed.	With the Diagnostics menu still set to RAMPING, monitor pin 18 of U918 (the DAC output on schematic 71 or 82) with an oscilloscope. If this signal does not ramp downward, suspect the DAC (U918).
Op amp U808 has failed.	If U918 pin 18 shows a ramp down on an oscilloscope, but the signal at TP910 does not change or is very small, suspect U808 (on schematic 71 or 82).

Error Indication

Threshold of all three probes changes, but not to the expected voltage.

Possible Cause	Action
DAC is out of adjustment.	Adjust the DAC according to the instructions in the *Verification and Adjustments* section.
DAC cannot be brought into adjustment.	Trimmer potentiometers R902 and R110 (on schematic 71 or 82) may be bad. Use a DMM to verify that trimmer potentiometers R902 and R110 are operating properly.
	If the trimmers work well, use the diagnostics DAC THRSH function to compare the voltage at TP910 to the voltage at U918. If the voltages are not inverse centered around ground, suspect U808 (on schematic 71 or 82). If the voltages do track properly, suspect U918 (on schematic 71 or 82).

Error Indication

DAC circuit is in adjustment, but one or more pods do not track the threshold.

Possible Cause	Action
The probe is not functional.	Install a known good probe in the pod connector and see if the threshold tracks the threshold value specified in the Channel Specification menu. If the channel now behaves correctly, suspect the old probe.
The channel's threshold buffer circuit is not functional.	Suspect the buffer op amps (on schematics 71 or 82). Suspect U711 for problems in pods A and B. Suspect U808 for problems in pod C.

Error Indication

Threshold is correct except at some menu settings.

Possible Cause	Action
The DAC has a stuck bit.	Set the DAC THRSH diagnostics function to RAMPING and set the DISPLAY field to OFF. With an oscilloscope, monitor test point TP910. The voltage at the test point should show a linear ramp wave. If you look closely, you will see very small steps. If steps in the ramp are missing, suspect U918.
	If the steps are all uniform, and there are no missing steps, readjust the DAC according to the instructions in the *Verification and Adjustments* section. If the adjustment makes no difference in performance, suspect DACU918 is non-linear, or the resistors are out of tolerance.

91A24 AND 91AE24 DAC THRSH FUNCTION DESCRIPTION
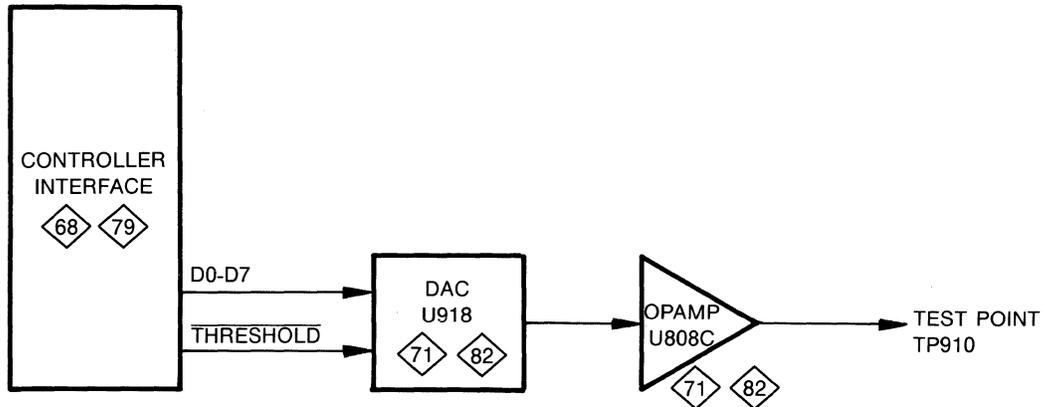
4438-539

Figure 7-37. Blocks of the 91A24 and 91AE24 tested by the DAC THRSH function.

This function has four operations that can be selected with the SELECT key on the DAS. The four selections set the DAC to 0.00 volts by writing 80_{16} to the DAC, set the DAC to -6.40 volts by writing 00_{16}, set the DAC to +6.35 volts by writing FF_{16}, and ramp the DAC by continuously writing decrementing values from FF to 00. The voltage values can be measured at test point TP910 to adjust and verify accuracy.

While ramping, a scope can be connected to test point TP910. The scope should show a staircase display which makes malfunctioning bits visible. To produce a steady and consistent display while ramping, select LOOPING ON with the DISPLAY OFF in the Diagnostics menu.

91A24 FUNCTION 7 PRB CLK EX
91AE24 FUNCTION 5 PRB CLK EX

NOTE

This function fails unless variable threshold probes are connected to the 91A24 module and to all 91AE24 modules being tested, even though the tested circuitry may be functional.

CIRCUIT OVERVIEW

The PRB CLK EX (probe clock exerciser) function verifies the 91A24 and 91AE24 circuits that lie between the inputs from the probes and system data login registers (U125, U225, and U425). This circuitry includes the probe receivers, the probe data login registers (U118, U221, and U421), and the multiplex mode login register (U121). Test 0 of the PRB CLK EX function also checks the 91A24 clock qualifier circuits (schematic 77) and clock generator circuits (schematic 78).

FUNCTION DESCRIPTION

All three tests in this function cause the probes attached to the module to output data. This data then stimulates the module's data-receiving circuits and external clock circuits. The acquired data is analyzed to give the test results.

Because data actually comes from the probes to run this function, three probes with variable thresholds must be connected to the 91A24 and the probe leads left unconnected. P6462 probes will not work, because their threshold is fixed. Three additional variable threshold probes must also be connected to each tested 91AE24 module.

Do not connect any of the probe leads to voltage sources. Certain voltage levels on the probe leads could cause this test to fail. This is because the test swings the probe threshold to the high and low limits to cause the probes to output data. If the probe is connected to voltages near or above maximum thresholds, the probes may not detect a change in state.

Test 0 uses levels from the 91A24 probes as inputs to the 91A24 clock and qualifier circuits shown on schematics 77 and 78. Test 0 runs on the 91AE24 also, but only verifies the 91AE24 circuitry that receives clocks from the 91A24.

Test 1 acquires data bytes out of the probe to see if the login registers work. The 91A24 login registers are on schematic 72, and the 91AE24 login registers are on schematic 83.

Test 2 acquires data bytes out of the probe into the multiplex mode login register U121 (91A24 schematic 72 and 91AE24 schematic 83). This verifies the integrity of the demultiplexing mode data path.

Readback Ports

Test 0 results are read back through U135 on both the 91A24 (schematic 69) and the 91AE24 (schematic 80). This is port 03.

Tests 1 and 2 results are read back through U131 (port 0B), U231 (port 0C), and U431 (port 0D) on both the 91A24 (schematic 69) and the 91AE24 (schematic 80).

91A24 AND 91AE24 PRB CLK EX TEST 0 TROUBLESHOOTING

Reading the Test 0 Error Codes

Test 0 of the PRB CLK EX function provides test results like those shown in Figure 7-38. Along with the usual diagnostic information, this test also indicates which pod clock (see Table 7-12) was being tested when the test stopped.

Port address — always 03, which is the memory address register port.

Bank — 1, 2, or 3. 1 = PODC CLOCKS, 2 = PODB CLOCKS, and 3 = PODA CLOCKS in the Clock Specification sub-menu.

Q — appears if error occurs while qualifier signal is being tested.

Clock Signal — 0, 1, 2, 3, 4, or 5

ADDR   EXPECTED   ACTUAL

PRB CLK EX   TEST 0   03 1 Q 1 YY   ZZ

value the diagnostics expect to read from the port

value the diagnostics actually read from the port

4541-740

Figure 7-38. 91A24 and 91AE24 PRB CLK EX, test 0 readback display. The ACTUAL value is read from the MAR. The EXPECTED value may be 00 or 02.

Table 7-12
CLOCK SIGNAL CORRELATION FOR TEST 0 ERROR CODE DISPLAY

Displayed Clock Signal Number	Clock Signal Input Probe	Clock Signal Name (Schematic 78)
0	A	CLK1
1	A	$\overline{\text{CLK1}}$
2	B	CLK2
3	B	$\overline{\text{CLK2}}$
4	C	CLK3
5	C	$\overline{\text{CLK3}}$

Table 7-13
COMPONENTS FOR BANK AND CLOCK SIGNAL VALUES IN ERROR INDICATION

		Bank			
		1	2	3	Set Flip-Flop
	0	U735A	U735B	U741A	U741B
	1	U835A	U835B	U841A	U841B
CLOCK	2	U948A	U948B	U751A	U751B
SIGNAL	3	U951A	U951B	U851A	U851B
	4	U738A	U738B	U745A	U745B
	5	U838A	U838B	U845A	U845B

Error Indication

PRB CLK EX function fails along with CNTR TIMR, MEM ADDR, ACQ MEM, STK PNTR, WRD REC, OCCR CNTR, or DAC THRSH functions.

Possible Cause	Action
Circuits required by the PRB CLK EX function are malfunctioning.	Debug according to the failed function with the smallest number.

Error Indication

Any or all 91A24 and 91AE24 modules fail.

Possible Cause	Action
Incorrect probes	Verify that 91A24 compatible probes with variable threshold capability are connected to the all pod connectors of the 91A24 and any other tested modules. The test will fail if fixed threshold probes are used.
Bad probe	Move the probes around to new pod connectors. If the failure indication changes, suspect one of the probes.

Error Indication

PRB CLK EX Test 0 fails on both the 91A24 and a 91AE24.

Possible Cause	Action
If a 91AE24 is connected to the 91A24, the 91AE24 may cause the failure.	Turn off the DAS. Disconnect interconnect cables from J173, J183, and J185 at the top of the 91A24 module, then replace the square pin jumpers as shown in the *Operating Instructions* section. You must replace the jumpers to properly terminate the 91A24's clock signals. Turn on the DAS and re-run test 0 on the 91A24. If the test fails with the cables disconnected, the 91A24 is at fault. If the test passes, suspect incorrectly installed interconnect cables or a 91AE24 module.

Error Indication: 91A24

	ADDR	EXPECTED	ACTUAL
PRB CLK EX TEST 0	03 B	P 00	01

Possible Cause	Action
If probes are not connected the function will not pass.	Make sure that probes are connected to all three pod connectors on the 91A24 module.
CLK INIT malfunction.	Loop test 0. Check U965 pin 3 (on schematic 68) for low pulses; if none, suspect U965. If low pulses are present, check U921D pin 12 (on schematic 78) for low pulses. If no low pulses, suspect R917, R916, or R915 (schematic 78). If low pulses on U921D pin 12, check U921D pin 15 for high pulses; if none, suspect U921 (schematic 78). If high pulses are present, refer to Table 7-13 for the applicable set flip-flop and check for low pulses on pin 15 of that flip-flop. If there are no low pulses on pin 15, suspect the set flip-flop or U848 (schematic 78).
Clock receiver flip-flops malfunctioning.	Refer to the displayed error code and Table 7-13 to decide on a suspect flip-flop (shown on schematic 78). While test 0 is looping, check for a high or high pulses on pin 9 of the suspected flip-flop. If pin 9 is steady low, trace the applicable CLK or CLK back to find the faulty IC. If pin 9 is steady high, check the applicable flip-flop Q output for a steady low. If Q is not steady low, then replace the suspect flip-flop.

Error Indication: 91A24

			ADDR	EXPECTED	ACTUAL
PRB CLK EX	TEST 0		03 B Q P 00	01

Possible Cause	Action
Pod qualifier ($\overline{\text{PXQX}}$) malfunction (schematic 78).	Refer to the displayed error code and Table 7-13 to decide on a suspect flip-flop (shown on schematic 78). Loop test 0. While looping, check for pulses on the D input to that flip-flop. If high pulses are present, suspect that flip-flop. If no high pulses, trace the D input signal ($\overline{\text{PXQX}}$ pod qualifier line) to its source device in the clock-qualifier generator (schematic 77). Check that the QX and $\overline{\text{QX}}$ inputs to the device are of opposite polarity. If the QX and $\overline{\text{QX}}$ inputs are not toggling opposite to each other, suspect U725A, B, or C (on schematics 70 and 71). (U725 contains the clock buffers for all three probes, but the individual buffers are shown on different schematics.)

Otherwise, check that the clock qualifier (Table 7-13) enable line (QX0-QX5 on schematic 77) from the clock/clock-qualifier selector to the suspect device carries high pulses. If no high pulses are present, trace that enable signal to its source and suspect that device in the clock/clock-qualifier selector (U935, U928, or U931 on schematic 77). If high pulses are present on the enable lines to the suspect device in the clock-qualifier generator, replace the device in the clock qualifier generator (schematic 77). |

Error Indication: 91A24

	ADDR	EXPECTED	ACTUAL
PRB CLK EX TEST 0	03 B	P 02	00

Possible Cause	Action
Clock enable malfunction (schematic 78).	Refer to the displayed error code and Table 7-13 to decide on a suspect flip-flop (shown on schematic 78). Loop test 0. Then, while looping, check for high pulses on the CXX clock enable input (CC0-CC5, CB0-CB5, or CA0-CA5) of the suspect flip-flop. If there are no high pulses, trace the signal to its source in the clock/ clock-qualifier selector (on schematic 77) to locate the faulty component.
Clock receiver flip-flop malfunction (schematic 78).	Refer to Table 7-13 to determine the suspect device; then, while test 0 is still looping, check for a low or low pulses on pin 9 of that device. If pin 9 is never low, trace the signal back to correct. Otherwise, check for high pulses on the CXX clock enable input to that device (CC0-CC5, CB0-CB5, or CA0-CA5). If no high pulses on the CXX clock enable, trace the signal back to locate the faulty device. If there are high pulses on the CXX input, check for high pulses on the $\overline{Q}$ output of the suspect device. If there are no high pulses, replace the flip-flop (schematic 78).

Error Indication: 91AE24

91AE24 fails PRB CLK EX test 0, but the 91A24 module does not.

Possible Cause	Action
Probes must be connected to both the 91A24 and the 91AE24.	Make sure that variable threshold probes are connected to all three pod connectors of the the 91A24 as well as to the 91AE24.
Cables are not properly connected between the 91A24 and 91AE24	Check the interconnect cable connections and jumper positions. After cables and jumpers are properly installed, re-run the test to see if the failure has gone away.

Error Indication: 91AE24

	ADDR	EXPECTED	ACTUAL
PRB CLK EX TEST 0	03 1	0 XX	XX

Possible Cause	Action
CLKC receiver may be malfunctioning.	Loop test 0. Examine U721 pin 6 (on schematic 87) with a scope. If pulses are not present, suspect U275C (on schematic 83). If pulses are present on U721 pin 6, then examine U721 pin 7 (also on schematic 87). If pin 7 is high, suspect U721. If pin 7 is low, examine U938 pin 11 for pulses. If U938 pin 11 is pulsing, suspect U938. If U938 pin 11 is static, suspect U965 on schematic 79.

Error Indication: 91AE24

	ADDR	EXPECTED	ACTUAL
PRB CLK EX TEST 0	03 2	0 XX	XX

Possible Cause	Action
CLKB receiver may be malfunctioning.	Loop test 0. Examine U721 pin 11 (on schematic 87) with a scope. If pulses are not present, suspect U275B (on schematic 83). If pulses are present on U721 pin 11, then examine U721 pin 10 (also on schematic 87). If pin 10 is high, suspect U721. If pin 10 is low, examine U941 pin 11 for pulses. If U941 pin 11 is pulsing, suspect U941. If U941 pin 11 is static, suspect U965 on schematic 79.

Error Indication: 91AE24

	ADDR	EXPECTED	ACTUAL
PRB CLK EX TEST 0	03 3	0 XX	XX

Possible Cause	Action
CLKA receiver may be malfunctioning.	Loop test 0. Examine U721 pin 13 (on schematic 87) with a scope. If pulses are not present, suspect U275A on schematic 83. If pulses are present on U721 pin 13, then examine U721 pin 12 (also on schematic 87). If pin 12 is high, suspect U721. If pin 12 is low, examine U945 pin 11 for pulses. If U945 pin 11 is pulsing, suspect U945. If U945 pin 11 is static, suspect U965 on schematic 79.

91A24 AND 91AE24 PRB CLK EX TEST 0 DESCRIPTION

Figure 7-39. Blocks of the 91A24 tested by the PRB CLK EX function, test 0.

PRB CLK EX test 0 checks the probe clocks and qualifiers. This is done with three checks for both levels (positive and negative) of each clock (A, B, and C), and each pod (A, B, and C). There are, therefore, a total of 54 possible test results when the three checks are applied to all cases.

All three checks in PRB CLK EX test 0 verify 91A24's clock generator. All three checks use the memory address register (MAR) as a detector to see if clocks occur.

- The first check exercises the clock generator flip-flops (on schematic 78), the clock qualifier generator and clock/clock qualifier selector (on schematic 77), and the clock receivers (on schematics 70 and 71). It verifies that inputs to the clock generator flip-flops can be set so clocks are not generated.

- The second check exercises the same circuits as the first, except the qualifier receivers, rather than the clock receivers, are checked. It verifies that the qualifiers can be set so that clocks are not generated.

- The third check verifies that every clock generator flip-flop can generate clocks.

Test 0 Readback Port

Test 0 results are read back through U135 on schematic 69 (port 03), which is the memory address register port.

Test 0 Initial Conditions

The test is executed in two parts: a setup and the three checks. The setup is described here, the checks are described later. The first step in the initial conditions is performed only once at the beginning of the test. The setup is performed at the beginning of each loop through the test. The test loops 18 times.

1. U965 pins 5, 7, and 9 (PC1, PC3, and PC5 on schematic 68) are set low, disabling all of the qualifiers from U935, U928, and U931.

The remaining initial conditions are executed at the beginning of each loop through the test. The test loops 18 times to complete.

2. The clock flip-flops (on schematic 78) are initialized by setting U965 pin 3 ($\overline{\text{CLK INIT}}$ on schematic 68) low. This sets the clock one-shots (U741B, U841B, U751B, U851B, U745B, and U845B on schematic 78), which set the clock flip-flops

3. The clock/clock-qualifier selector registers on all of the 91A24s and 91AE24s are initialized by writing 80_{16} onto D0-D7 and asserting U965 pins 4 and 6 (PC0, PC2 on schematic 68); and writing 0 to U965 pins 5, 7, 8, and 9 (PC1, PC3, PC4, and PC5 on schematic 68).

4. The MAR is loaded with 000_{16}.

5. The threshold is set low for a positive clock, or high for a negative clock. This sets the clock input to the clock flip-flop high so that it cannot be clocked by the select bit (CC0-CC5, CB0-CB5, or CA0-CA5 on schematic 77).

6. The clock flip-flops are initialized by setting U965 pin 3 ($\overline{\text{CLK INIT}}$ on schematic 68) low. This initializes any flip-flops that were clocked when the threshold changed.

Test 0 Run Sequence

These are the three checks that are executed after the setup given previously. Each of the three checks is described in even greater detail later.

Each clock generator flip-flop is tested individually. The combination of the initial conditions and the next three steps complete the first check. The first check verifies that no clocks are generated when the qualifier is true, but the clock signal is disabled.

1. The clock (A, B, or C) whose flip-flop is being tested is selected by writing bit 6 high in the appropriate clock select register (U938, U941, U945 on schematic 77). This enables the selected clock through U721 (on schematic 77).

2. The clock select bit for the flip-flop being tested is set high and then set low. This should not clock the flip-flop because the common clock input should be high from a previous step.

3. The low eight bits of the MAR are read from U135 (on schematic 69) to ensure that the MAR did not increment. If the MAR reads other than 0, the test stops at this point.

The second check occupies steps 4 through 9. This check verifies that the clock qualifier generator (on schematic 77) passes qualifier signals. This is done by setting the qualifier signal false, passing the false qualifier through the clock qualifier generator, and attempting to cause a clock in the clock generator (schematic 78). No clock should result, so the MAR should not increment.

4. The clock being tested is de-selected by setting bit 6 of its clock select register low. This prevents the following threshold change from incrementing the MAR.

5. The threshold is now set so that the common clock input to the flip-flop being tested is low, enabling clocking from the clock select bit.

6. The clock flip-flops are initialized by setting U965 pin 3 ($\overline{\text{CLK INIT}}$ on schematic 68) low. This initializes any flip-flops that were clocked when the threshold changed.

7. The qualifier input to the flip-flop being tested is set high by setting the appropriate bit (0-5) of the appropriate register U965 pin 5, 7, or 9 (PC1, PC3, or PC5 on schematic 68) high. This prevents a clock from being generated.

8. The flip-flop being tested is selected and clocked as in steps 1 and 2.

9. The MAR is read as in step 3, and tested for 0. If the MAR does not contain 0, the test stops here.

The remaining steps finish the loop and complete the third check. The third check verifies that every clock generator flip-flop can generate clocks.

10. The qualifier bit for the flip-flop being tested is set low.

11. The flip-flop is clocked as in steps 1 and 2. This will cause a clock to be produced by clocking the flip-flops' $\overline{Q}$ output high.

12. The clocks are de-selected as in step 4.

13. The clock flip-flops are then initialized by setting U965 pin 3 ($\overline{\text{CLK INIT}}$ on schematic 68) low. This sets all of the clock flip-flops so that they may be re-clocked.

14. The flip-flop under test is once again clocked as in steps 1 and 2.

15. The MAR is read as in step 3 and tested for a count of 2. If the DAS does not read 02_{16} from the MAR, the test stops looping and writes an error message.

91A24 AND 91AE24 PRB CLK EX TEST 1 TROUBLESHOOTING

Reading the Test 1 Error Codes

Test 1 of the PRB CLK EX function provides test results like those shown in Figure 7-40.
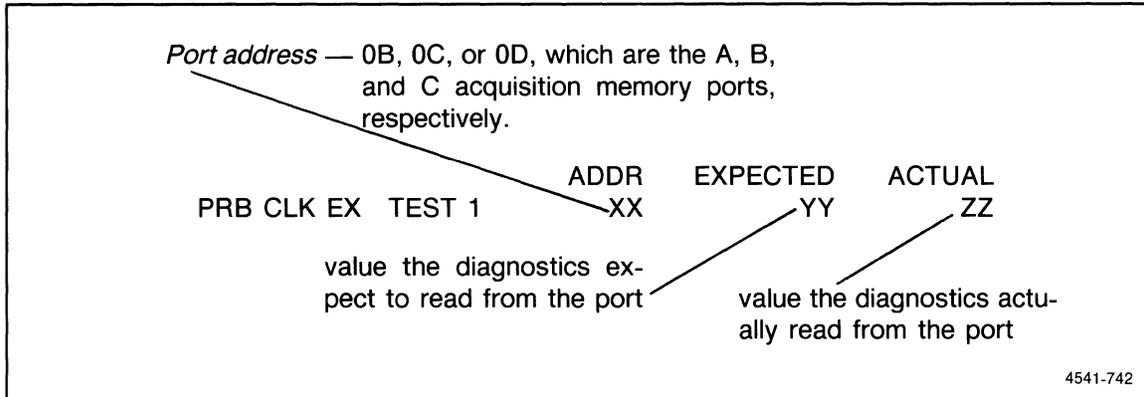
Figure 7-40. 91A24 and 91AE24 PRB CLK EX, test 1 readback display. The ACTUAL value is read from the acquisition memory. The EXPECTED value may be 00 or FF.

Error Indication

PRB CLK EX function fails along with CNTR TIMR, MEM ADDR, ACQ MEM, STK PNTR, WRD REC, OCCR CNTR, or DAC THRSH functions.

Possible Cause	Action
Circuits feeding into PRB CLK EX test are malfunctioning.	Debug according to the failed function with the smallest number.

Error Indication

PRB CLK EX Test 1 fails.

Possible Cause	Action
If a 91AE24 is connected to the 91A24, the 91AE24 may cause the failure.	Turn off the DAS. Disconnect interconnect cables from J173, J183, and J185 at the top of the 91A24 module. Turn on the DAS and re-run test 1. If the test fails with the cables disconnected, the 91A24 is at fault. If the test passes, suspect incorrectly installed interconnect cables or a 91AE24 module.

Error Indication

		ADDR	EXPECTED	ACTUAL
PRB CLK EX	TEST 1	0X	00	FF

Possible Cause	Action
Login not enabled (91A24 schematic 68 or 91AE24 schematic 79).	Loop test 1. Check U758 pins 16, 12, and 15 (on schematic 68 or 79) for high signals; if any of these three pins are not high, suspect U758. Otherwise, check U218 pins 3, 6, and 8 for lows; if any pins are not low, suspect U218.

Error Indication

		ADDR	EXPECTED	ACTUAL
PRB CLK EX	TEST 1	0X	00	XX

Possible Cause	Action
Logins are not being clocked.	Loop test 1. Check pin 11 of U118, U221, and U421 (on 91A24 schematic 72 or 91AE24 schematic 83) for high pulses. If any pin does not show high pulses, trace the missing clock signal back through the login clock generator (on schematic 72 or 83) to discover the faulty component.

Error Indication

		ADDR	EXPECTED	ACTUAL
PRB CLK EX	TEST 1	0X	XX	XX

Possible Cause	Action
Probe receiver malfunction.	Loop test 1. Check that all of the PXDX inputs to U118, U221, and U421 (on schematic 72 or 83) are toggling to the level indicated by the EXPECTED field on the display. If one of the inputs is not toggling to the proper level, trace those signals back and correct. If all inputs are toggling to the correct level, then suspect the following devices: • Suspect U118 (schematic 72 or 83) for error address 0B. • Suspect U221 (schematic 72 or 83) for error address 0C. • Suspect U421 (schematic 72 or 83) for error address 0D.

91A24 AND 91AE24 PRB CLK EX TEST 1 DESCRIPTION
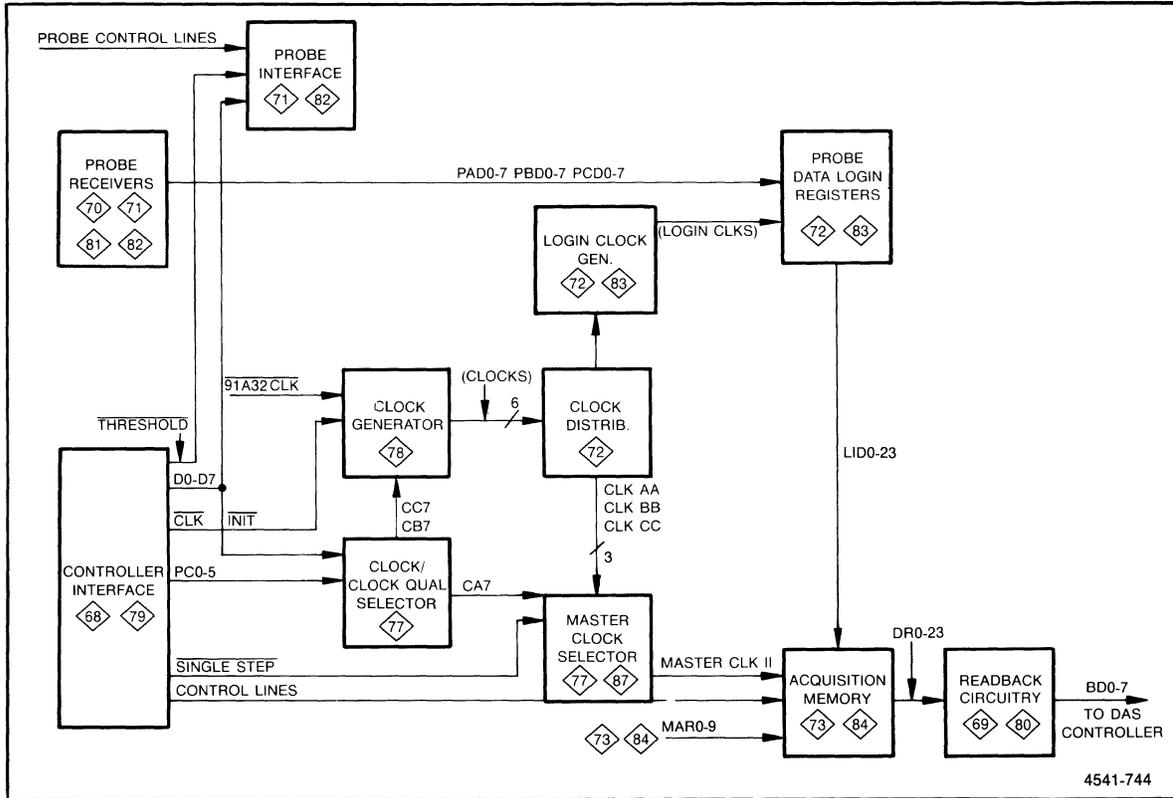
Figure 7-41. Blocks of the 91A24 and 91AE24 tested by the PRB CLK EX function, test 1.

This test verifies that the probe data login registers can transmit both 1s and 0s.

First, the probe threshold is set so that the probe inputs are 0; then the probe data login registers are clocked using the internal 91A24 clock on the Trigger/Time Base.

Then the acquisition memory receives three internal single-step clocks. The memory is then read to ensure that pods A, B, and C contain 0s. If any pod contains other than 0s the DAS reports an error; otherwise the probe thresholds are set so the probe inputs are high and the clocking sequence is performed again. The acquisition memory is then checked for 1s.

Test 1 Readback Ports

Test 1 results are read back through U131 (pod A memory port), U231 (pod B memory port), and U431 (pod C memory port) on 91A24 schematic 69 or 91AE24 schematic 80 (ports 0B, 0C, and 0D).

Test 1 Initial Conditions

Before any checks are done, the module is set up to perform the diagnostic test. The test itself is described next, under *Test 1 Run Sequence*.

1. The single-step clock from the Trigger/Time Base is selected by writing E8 to 91A32 CLK on the Trigger board. This clock is used later to clock the probe data login registers.

2. The system data login registers are disabled and the probe data login registers (U118, U121, and U421 on schematic 72 or 83) are enabled by writing EB_{16} to U758 (on schematic 68 or 79). This makes U758 pins 12, 15, and 16 high. This write also sets U758 pin 19 (MUX MODE on schematic 68 or 79) low which disables the multiplex mode login register U121 (on schematic 72 or 83).

3. The DAS writes 20_{16} to U761 (on schematic 68 or 79). This makes U761 pin 16 (MEM RD on schematic 68 or 79) high, and U461A pin 2 ($\overline{\text{MAR EN}}$ on schematic 73 or 84) low, allowing loading of the MAR (U138, U238, and U438 on schematic 73 or 84).

4. On the 91A24, $7F_{16}$ is written onto D0-D7, and U965 pin 4 (PC0 on schematic 68) is asserted. This sets U731B pin 11 (CC7 on schematic 78) low, which enables the 91A32 clock through U731B to clock the login registers.

5. Still on the 91A24, 80_{16} is written onto D0-D7, and U965 pins 5-9 (PC1-PC5 on schematic 68) are toggled. This selects the single-step clock through U721 (schematic 77).

6. If a 91AE24 is being tested, 80_{16} is written onto the 91AE24 D0-D7, and U965 pin 8 (PC4 on schematic 79) is asserted on the board being tested. This enables the 91AE24 single-step clock through U721.

Test 1 Run Sequence

Test 1 performs two checks, the first verifies that 0s can be clocked in, the second verifies that 1s can be clocked in.

1. The MAR is loaded with 000_{16}. At the same time, 18_{16} is written to U765 (on 91A24 schematic 68 or 91AE24 schematic 79). This makes $\overline{\text{WEA-WEC}}$ (U765 pins 5, 6, and 9) to the acquisition memory RAMs low.

2. 10_{16} is written to U761, on schematic 68 and 79, on all of the 91A24s and 91AE24s in the DAS. This makes U761 pin 16 (MEM RD on schematics 68 and 79) low and sets U461A pin 2 ($\overline{\text{MAR EN}}$ on schematics 73 and 84) high so that the MAR will not increment during this test.

3. The threshold is run to its highest limit by writing FF onto D0-D7 and asserting U958 pin 2 ($\overline{\text{THRESHOLD}}$ on schematic 68 or 79). This makes all of the probe inputs appear low.

4. On the 91A24, 0 is written to U965 pin 3 ($\overline{\text{CLK INIT}}$ on schematic 68) to clear all the clock flip-flops on schematic 78 that may have been clocked when the threshold was set high. A set flip-flop could inhibit the 91A32 clock at U535 (schematic 78).

5. 0 is written to $\overline{\text{SINGLE STEP}}$ on the Trigger/Time Base board. This causes a clock that is passed through U731B, U748A, U535A, B, and C (on 91A24 schematic 78), and U275A, B, and C (on 91A24 schematic 72 and 91AE24 schematic 83) to clock 0s into the probe data login registers.

6. The 0s in the login registers are loaded into the acquisition memory by writing 0 to U958 pin 10 ($\overline{\text{SINGLE STEP}}$ on schematic 68 or 79) three times. This generates three internal master clocks.

7. $1F_{16}$ is written to U765 (schematic 68 or 79). This makes U765 pins 5, 6, and 9 ($\overline{\text{WEA}}$-$\overline{\text{WEC}}$) high to the acquisition memory RAMs (on schematic 73 or 84).

8. 31_{16} is written to U761 (on schematic 68 or 79). This makes U761 pin 6 (READ ACQ on schematic 68 or 79) high. This enables the contents of the acquisition memory to be read by disabling the acquisition memory data registers (U128, U228, and U428 on schematic 73 or 84).

9. The three bytes of acquisition memory are read from the acquisition memory ports, U131, U231, and U431 (on schematic 69 or 80), to verify that only 0s were acquired.

10. The threshold is set to its lower limit.

11. 10_{16} is written to U761 of the board under test (on schematic 68 or 79). This makes U761 pin 16 (MEM RD on schematic 68 or 79) low and sets U461A pin 2 ($\overline{\text{MAR EN}}$ on schematic 73 or 84) high so that the MAR will not increment.

12. Steps 3 through 8 are repeated. Then the acquisition memory is read to verify that only 1s were acquired.

91A24 AND 91AE24 PRB CLK EX TEST 2 TROUBLESHOOTING

Reading the Test 2 Error Codes

Test 2 of the PRB CLK EX function provides test results like those shown in Figure 7-42.

Port address — 0B, 0C, or 0D, which are the A, B, and C acquisition memory ports, respectively.

ADDR   EXPECTED   ACTUAL

PRB CLK EX   TEST 2   XX   YY   ZZ

value the diagnostics expect to read from the port

value the diagnostics actually read from the port

4541-745
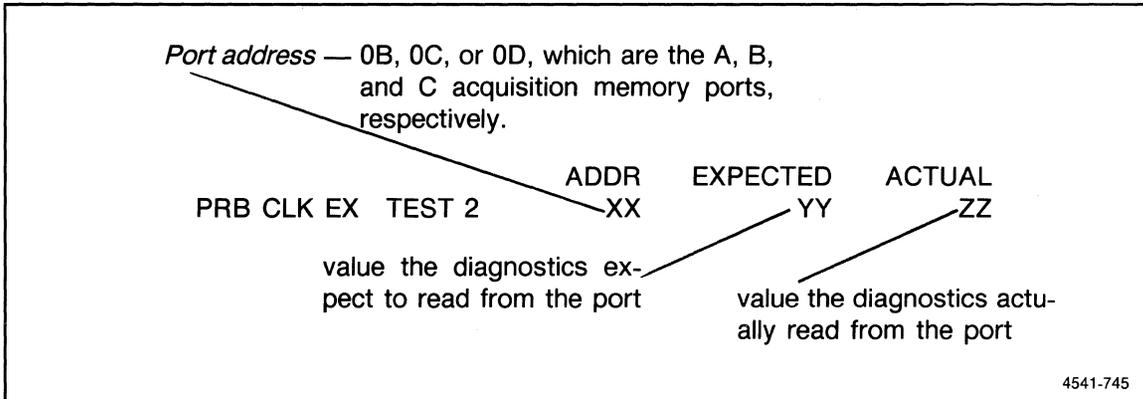
Figure 7-42. 91A24 and 91AE24 PRB CLK EX, test 2 readback display. The ACTUAL value is read from the acquisition memory. The EXPECTED value may be 00 or FF.

Error Indication

PRB CLK EX function fails along with CNTR TIMR, MEM ADDR, ACQ MEM, STK PNTR, WRD REC, OCCR CNTR, or DAC THRSH functions.

Possible Cause	Action
Circuits feeding into PRB CLK EX test are malfunctioning.	Debug according to the failed function with the smallest number.

Error Indication

PRB CLK EX Test 2 fails.

Possible Cause	Action
If a 91AE24 is connected to the 91A24, the 91AE24 may cause the failure.	Turn off the DAS. Disconnect interconnect cables from J173, J183, and J185 at the top of the 91A24 module. Turn on the DAS and re-run test 1. If the test fails with the cables disconnected, the 91A24 is at fault. If the test passes, suspect incorrectly installed interconnect cables or a 91AE24 module.

Error Indication

	ADDR	EXPECTED	ACTUAL
PRB CLK EX TEST 2	0X	00	XX

Possible Cause	Action
Multiplex mode latch malfunctioning (on 91A24 schematic 72 or 91AE24 schematic 83)	Suspect U121 (on schematic 72 or 83).

91A24 AND 91AE24 PRB CLK EX TEST 2 DESCRIPTION
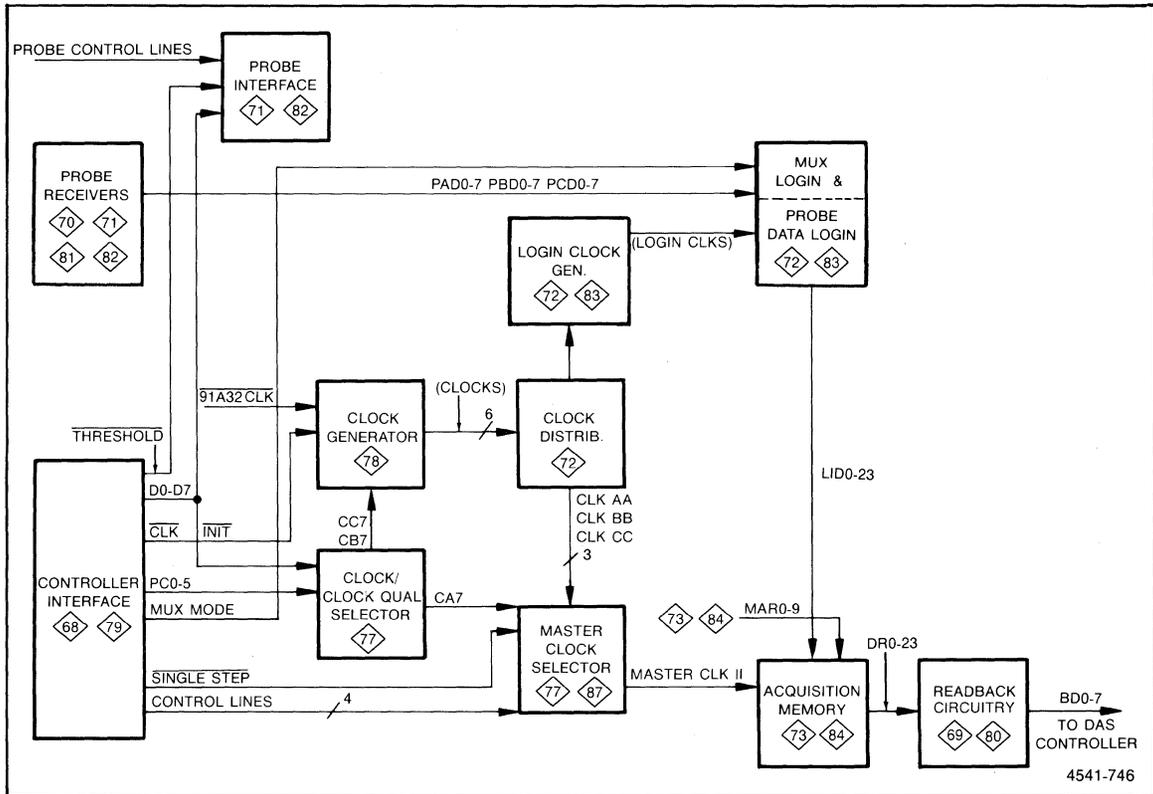
Figure 7-43. Blocks of the 91A24 and 91AE24 tested by the PRB CLK EX function, test 2.

This test verifies that the probe data login registers can transmit both 1s and 0s in demultiplexing mode.

First, the probe threshold is set so that the probe inputs are 0; then the probe data and multiplex mode login registers are clocked using the internal 91A24 clock on the Trigger/Time Base.

Then the acquisition memory receives three internal single-step clocks. The memory is then read to ensure that pods A, B, and C contain 0s. If any pod contains other than 0s the DAS reports an error; otherwise the probe thresholds are set so the probe inputs are high and the clocking sequence is performed again. The acquisition memory is then checked for 1s.

Test 2 Readback Ports

Test 2 results are read back through U131 (pod A memory port), U231 (pod B memory port), and U431 (pod C memory port) on 91A24 schematic 69 or 91AE24 schematic 80 (ports 0B, 0C, and 0D).

Test 2 Initial Conditions

Before any checks are done, the module is set up to perform the diagnostic test. A description of the test itself follows, under *Test 2 Run Sequence*.

1. The single-step clock from the Trigger/Time Base is selected by writing E8 to 91A32 CLK on the Trigger board. This clock is used later to clock the probe data login registers.

2. The system data login registers are disabled and the probe data login registers (U118, U121, and U421 on schematic 72 or 83) are enabled by writing FB_{16} to U758 (on schematic 68 or 79). This makes U758 pins 12, 15, and 16 high. This write also sets U758 pin 19 (MUX MODE on schematic 68 or 79) high which enables the multiplex mode login register U121 (on schematic 72 or 83).

3. The DAS writes 20_{16} to U761 (on schematic 68 or 79). This makes U761 pin 16 (MEM RD on schematic 68 or 79) high, and U461A pin 2 ($\overline{\text{MAR EN}}$ on schematic 73 or 84) low, allowing loading of the MAR (U138, U238, and U438 on schematic 73 or 84).

4. On the 91A24, $7F_{16}$ is written onto D0-D7, and U965 pin 4 (PC0 on schematic 68) is asserted. This sets U731B pin 11 (CC7 on schematic 78) low, which enables the 91A32 clock through U731B to clock the login registers.

5. Still on the 91A24, 80_{16} is written onto D0-D7, and U965 pins 5-9 (PC1-PC5 on schematic 68) are toggled. This selects the single-step clock through U721 (schematic 77).

6. If a 91AE24 is being tested, 80_{16} is written onto the 91AE24 D0-D7, and U965 pin 8 (PC4 on schematic 79) is asserted on the board being tested. This enables the 91AE24 single-step clock through U721.

Test 1 Run Sequence

Test 1 performs two checks, the first verifies that 0s can be clocked in, the second verifies that 1s can be clocked in.

1. The MAR is loaded with 000_{16}. At the same time, 18_{16} is written to U765 (on 91A24 schematic 68 or 91AE24 schematic 79). This makes $\overline{\text{WEA}}\text{-}\overline{\text{WEC}}$ (U765 pins 5, 6, and 9) to the acquisition memory RAMs low.

2. 10_{16} is written to U761, on schematic 68 and 79, on all of the 91A24s and 91AE24s in the DAS. This makes U761 pin 16 (MEM RD on schematic 68 and 79) low and sets U461A pin 2 ($\overline{\text{MAR EN}}$ on schematics 73 and 84) high so that the MAR will not increment during this test.

3. The threshold is run to its highest limit by writing FF onto D0-D7 and asserting U958 pin 2 ($\overline{\text{THRESHOLD}}$ on schematic 68 or 79). This makes all of the probe inputs appear low.

4. On the 91A24, 0 is written to U965 pin 3 ($\overline{\text{CLK INIT}}$ on schematic 68) to clear all the clock flip-flops on schematic 78 that may have been clocked when the threshold was set high. A set flip-flop could inhibit the 91A32 clock at U535 (schematic 78).

5. 0 is written to $\overline{\text{SINGLE STEP}}$ on the Trigger/Time Base board. This causes a clock that is passed through U731B, U748A, U535A, B, and C (on 91A24 schematic 78), and U275A, B, and C (on 91A24 schematic 72 and 91AE24 schematic 83) to clock 0s into the probe data login registers.

6. The 0s in the login registers are loaded into the acquisition memory by writing 0 to U958 pin 10 ($\overline{\text{SINGLE STEP}}$ on schematic 68 or 79) three times. This generates three internal master clocks.

7. $1F_{16}$ is written to U765 (schematic 68 or 79). This makes U765 pins 5, 6, and 9 ($\overline{\text{WEA-WEC}}$) high to the acquisition memory RAMs (on schematic 73 or 84).

8. 31_{16} is written to U761 (on schematic 68 or 79). This makes U761 pin 6 (READ ACQ on schematic 68 or 79) high. This enables the contents of the acquisition memory to be read by disabling the acquisition memory data registers (U128, U228, and U428 on schematic 73 or 84).

9. The three bytes of acquisition memory are read from the acquisition memory ports, U131, U231, and U431 (on schematic 69 or 80), to verify that only 0s were acquired.

10. The threshold is set to its lower limit.

11. 10_{16} is written to U761 of the board under test (on schematic 68 or 79). This makes U761 pin 16 (MEM RD on schematic 68 or 79) low and sets U461A pin 2 ($\overline{\text{MAR EN}}$ on schematic 73 or 84) high so that the MAR will not increment.

12. Steps 3 through 8 are repeated. Then the acquisition memory is read to verify that only 1s were acquired.

MAINTENANCE: DIAGNOSTIC TEST DESCRIPTIONS

For diagnostic test descriptions, see section 7 of this addendum, *Maintenance: Troubleshooting*. The diagnostic information has been integrated with the troubleshooting information.

REFERENCE INFORMATION

This section contains the following information:

- 91A24/91AE24 error and prompter messages
- 91A24/91AE24 test point, jumper, and adjustment locations
- 91A24/91AE24 I/O map
- 91A24/91AE24 signal glossary

ERROR AND PROMPTER MESSAGES
(Additions with Firmware Version 1.11)

Table 9-1 lists the error and prompter messages added to the DAS by Firmware Version 1.11.

Table 9-1
ERROR AND PROMPTER MESSAGES

ACQUISITION STARTED -- CONTINUOUS	If you hold down the START ACQ or START SYSTEM keys for an extended period, the DAS continuously acquires and displays data until you press the STOP key.
	Holding down START SYSTEM also begins automatic restart of the Pattern Generator.
ALL LEVELS USED	You are attempting to add levels to the stack even though all 16 levels have been allocated.
MUST ASSIGN 1 CLOCK TO POD [X]	You must specify at least one clock term in the POD[X] CLOCK expression, where [X] equals A, B or C.
MUST BE A SUBSET OF STORE ONLY IF	You have specified a word recognizer value that is not a subset of your STORE ONLY IF value. You may not exit the menu while this condition exists.
	Each incorrect sequence is marked with a highlighted question mark (if it is visible on the screen) or indicated by a highlighted M (if you need to scroll it onto the screen).
NEEDS FIRMWARE VERSION >= 1.11	You must have firmware version 1.11 or higher.
NOT AN ACQ POD	You have attempted to specify a non-acquisition pod ID in a Channel Specification menu POD field. Specify an acquisition pod.

Table 9-1 (cont.)

UNDISPLAYABLE GROUP	The data entry field for the channel group requires more than 30 characters for display, and therefore cannot fit on the screen. In the Channel Specification menu, change the group's display radix and/or reduce the number of channels in the group.
WAITING FOR LEVEL: [1-16]	The sequential word recognizer's current level [1-16] is not yet satisfied.
WAITING FOR LEVEL: [1-16] TIME = [value]	If you have specified RUN TIMER in the sequential word recognizer, and the DAS is waiting to trigger, the TIME = message shows you the timer's current total.
WAITING FOR LEVEL: [1-16] CNTR = [value]	If you have specified INCR CNTR in the sequential word recognizer, and the DAS is waiting to trigger, the CNTR = message gives you the counter current total.
WAITING FOR MANUAL STOP	Either the NEVER TRG level or the CNTR level has been satisfied. Press STOP to end acquisition.

91A24/91AE24 TEST POINT, JUMPER, AND ADJUSTMENT LOCATIONS

The following illustration and text are intended as a fast reference for adjusting and troubleshooting the 91A24/91AE24. For further information on verifying, adjusting, or troubleshooting the 91A24/91AE24, refer to the *Verification and Adjustment Procedures* section and the *Maintenance: Troubleshooting* section of this addendum.

4541-747
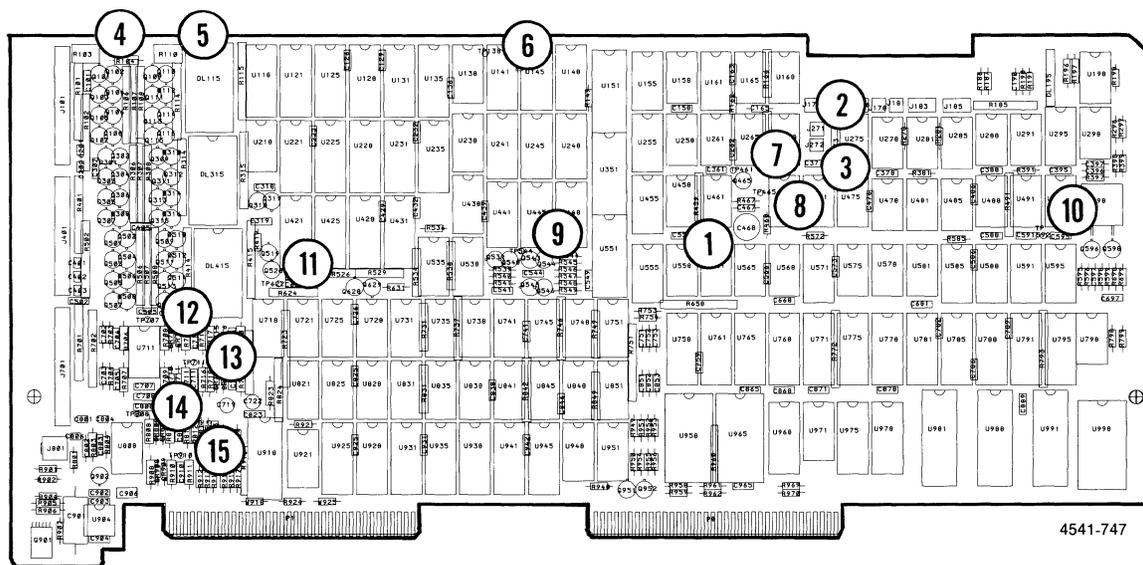
Figure 9-1. 91A24/91AE24 test point, jumper, and adjustment locations.

1. **C468.** This trimmer capacitor adjusts the width of the acquisition memory RAM chip-select pulse. The pulse width should be adjusted to 45 ns while monitoring TP 465. Be sure to ground your oscilloscope probe to the nearest ground point (TP461).

2. **J271** (91A24 only). These pins are normally shorted together. Opening the connection halts the stack word recognizer for troubleshooting.

3. **J272** (91A24 only). These pins are normally shorted together. Opening the connection disables the OR trigger.

4. **R103.** DAC offset adjustment. This trimmer resistor is used to set the offset voltage of the DAC to 0 volts.

5. **R110.** DAC gain adjustment. This trimmer resistor is used to set the voltage output of the DAC to +6.40 volts at TP910.

6. **TP138** <73>, <84>. This test point is used to verify that the MAR is clocking correctly.

7. **TP461** <68>, <79>. System ground.

8. **TP465** <73>, <84>. The ACQ RAM SEL(L) line. This test point is a monitoring point for the acquisition memory RAM chip select pulse. This pulse should be 45 ns wide. Monitor this test point while adjusting C468.

9. **TP544** <68>, <79>. System ground.

10. **TP592** <68>, <79>. System ground.

11. **TP622** <68>, <79>. System ground.

12. **TP707** <71>, <82>. This test point is used to set the threshold DAC reference voltage for pod A to -6.40 volts.

13. **TP711** <71>, <82>. This test point is used to set the threshold DAC reference voltage for pod B to -6.40 volts.

14. **TP808** <71>, <82>. This test point is used to set the threshold DAC reference voltage for pod C to -6.40 volts.

15. **TP910** <71>, <82>. This test point is used to monitor the DAC output while adjusting the DAC offset voltage (at R103) and gain (at R110).

91A24/91AE24 I/O MAP

The following table lists all the I/O ports on the 91A24/91AE24. Bit maps are supplied for multi-function control registers and readback buffers. You can use this table with the on-line debugging tool (ODT) to access any part of the 91A24 or 91AE24 that the DAS firmware writes to or reads from.

Table 9-2
91A24/91AE24 I/O MAP

I/O Address	Read (R) Write (W)	91A24 (A) 91AE24 (AE)	Description and Location (<91A24>, <91AE24>)
00	R	A-AE	Module identification (82 Hex); U791 <69>, <80>
00	W	A	Clocks ROM select latch; U968 <68> Output address 00 selects ROM U981 <68> Output address 01 selects ROM U988 <68> Output address 10 selects ROM U991 <68>
01	R	A-AE	Pod status register; U775 <69>, <80> Bit 0: Pod A status readback Bit 1: Pod B status readback Bit 2: Pod C status readback Bits 3-7: not connected
01	W	A-AE	Enables D/A converter; U918 <71>, <82>
02	R	A-AE	Clocks acquisition probe for status
02	W	A-AE	Sets acquisition probe for read/write; U925 <71>, <82> Bits 0, 1, 2: Not used Bits 3, 7: Not connected Bits 4, 5, 6: R(L)/W(H) lines to probes A, B, and C
03	R	A-AE	MAR0-MAR7 readback; U135 <69>, <80> Bits 0-7: MAR readback lines MAR0-MAR7

03	W	A-AE	Clocks control register; U761 <68>, <79>
			Bit 0(H): Enable read of acquisition memory
			Bit 1, 2: Counter/timer function select
			    Bit 1 Bit 2
			      1 1 Enable timer function
			      0 1 Enable counter function
			Bit 3(H): Enables INT3(L) <76> signal
			Bit 4(L): Loads stack pointer
			Bit 5(H): Enables acquisition memory read
			Bit 6(H): Sets flip-flops to temporarily inhibit word recognition and triggering operations
			Bit 7(H): Makes RESET qualifier an ENABLE, and the OR trigger qualifier a DISABLE

04	R	A-AE	Enables readback of MAR8, 9; SP0-SP3; STORING DATA; and ALL FULL; U235 <69>, <80> Bits 0, 1: MAR8, 9 readback Bits 2-5: Stack pointer status readback Bit 6: STORING DATA status readback Bit 7: Memory Address Register (MAR) ALL FULL status readback

Table 9-2 (cont.)
91A24/91AE24 I/O MAP

I/O Address	Read (R) Write (W)	91A24 (A) 91AE24 (AE)	Description and Location (<91A24>, <91AE24>)
04	W	A-AE	Writes probe A data into stack word recognizer; U148 <75>, <86>
05	R	A	Enables readback of counter/timer bits 0-7; U788 <76>
05	W	A-AE	Writes probe B data into stack word recognizer; U248 <75>, <86>
06	R	A	Enables readback of counter/timer bits 8-15; U795 <76>
06	W	A-AE	Writes probe C data into stack word recognizer; U448 <75>, <86>
07	R	A-AE	Enables readback of data qualifier status; U778 <69>, <80> Bits 0-2: Not connected Bit 3: Stack word recognizer status readback Bit 4: RESET word recognizer/qualifier status readback Bit 5: ENABLE word recognizer/qualifier status readback. Bit 6: DISABLE word recognizer/qualifier status readback. Bit 7: OR Trigger word recognizer/qualifier status readback.
07	W	A-AE	Writes system control and stack pointer data into stack control RAM; U555 <75>, <86> U555 outputs function as follows: SC0(L): Disables stack pointer and triggers 91A24 SC1(H): Enables counter/timer. SC2(H): Enables SYNC OUT. SC3(H): NOT function for stack word recognizer output.
08	R	A	Clears counter/timer <76>
08	W	A	Controls loading of stack occurrence counter <75>
09	W	A-AE	Single-step clock <77>, <87>
0A	R	A-AE	Enables readback of stack control status bits and counter reset status; U785 <69>, <80> Bits 0-2: Not connected. Bit 3: CNTR RESET status readback. Bits 4-7: Stack control RAM output status readback.
0A	W	A	Writes system control and stack pointer data into bits 8-11 of stack occurrence counter RAM; U455 <75>
0B	R	A-AE	Enables readback of bits 0-7 of acquisition memory; U131 <69>, <80>

Table 9-2 (cont.)
91A24/91AE24 I/O MAP

I/O Address	Read (R) Write (W)	91A24 (A) 91AE24 (AE)	Description and Location (<91A24>, <91AE24>)
0B	W	A	Writes system control and stack pointer data into bits 0-7 of stack occurrence counter RAM; U155, 255 <75>
0C	R	A-AE	Enables readback of bits 8-15 of acquisition memory; U231 <69>, <80>
0C	W	A-AE	Clocks control register; U758 <68>, <79> Bit 0(L): Enables stack pointer clock Bit 1(L): Enables CNTR RESET Bit 2(L): Disables 91A24 trigger Bit 3(L): Prevents triggering of stack word recognizer Bit 4(H): Selects MUX MODE for probe data login Bits 5-7(L): Enables diagnostic login registers and disables probes A, B, and C login registers
0D	R	A-AE	Enables readback of bits 16-23 of acquisition memory; U431 <69>, <80>
0D	W	A-AE	Clocks stack pointer; <76>, <86>
0E	R	A-AE	Enables readback of INT3(L), TRIGGERED(L), OCCR1-OCCR3, and SW0-SW2; U771 <69>, <80> Bit 0: INT3(L) status readback Bit 1: 91A24 triggered status readback Bits 2-4: Occurrence counter status readback Bits 5-7: Readback of stack word recognizer RAM outputs for probes A, B, and C
0F	R	A	Sets INT3(L) <76> high, removing interrupt
0F	W	A-AE	Writes probe A and system control data into data qualifier word recognizer RAM; U151 <74>, <85>
10	W	A-AE	Writes probe B and system control data into data qualifier word recognizer RAM; U351 <74>, <85>
11	W	A-AE	Write probe C and system control data into data qualifier word recognizer RAM; U551 <74>, <85>
12	W	A	Initializes clock generator latches; <78>
13	W	A-AE	Clocks clock selector register; U938 <77>, <87>
14	W	A	Clocks clock-qualifier selector register; U935 <77>
15	W	A-AE	Clocks clock selector register; U941 <77>, <87>
16	W	A	Clocks clock-qualifier selector register; U928 <77>
17	W	A-AE	Clocks clock selector register; U945 <77>, <87>
18	W	A	Clocks clock-qualifier selector register; U931 <77>

Table 9-2 (cont.)
91A24/91AE24 I/O MAP

I/O Address	Read (R) Write (W)	91A24 (A) 91AE24 (AE)	Description and Location (<91A24>, <91AE24>)

1B	W	A-AE	Clocks control register; U765 <68>, <80>
			   Bits 0-2(L): Enables write of probes A, B, and C data into acquisition memory RAMs
			   Bit 3(L): Enables loading of the low 8 bits (MAR0-7) of the MAR counter
			   Bit 4(L): Enables loading of the upper 2 bits (MAR8,9) of the MAR counter
			   Bits 5-7(H): Polarity control lines for the RESET, DISABLE, and OR TRIG word recognizer/ qualifiers

1E	W	A	Clocks counter/timer in timer mode; U491A <76>
1F	W	A	Clocks stack occurrence counter during diagnostic routines; U165A <75>

SIGNAL GLOSSARY

This signal glossary lists the signals used in the 91A24 and 91AE24. The signals are arranged alphabetically, then numerically. The signal description contains the signal mnemonics, the long-form signal name, a brief description of the signal function, and a schematic location.

NOTE

1. *Signals occurring on both the 91A24 and 91AE24 are marked with an asterisk. Signals without an asterisk occur only on the 91A24.*

2. *Schematic reference indicates schematic where the signal is generated, or where it enters or leaves the 91A24/91AE24.*

3. *Multiple signals having identical functions are normally grouped under one heading. Look for the signal name that occurs first alphabetically.*

*A DIAG EN(L), B DIAG EN(L), C DIAG EN(L): <68> <79> — Signals generated by 91A24/91AE24 controller interface that enable both the diagnostic login and probe data login registers.

*A MEM RD(L), B MEM RD(L), C MEM RD(L): <69> <80> — Signals that enable the acquisition memory readback buffers for probe A, B, and C data.

*A0-A12: <68> <79> — 91A24/91AE24 address bus. These signals originate at the DAS Controller.

*ACQ RAM SEL(L): <73> <84> Acquisition RAM select — Signal that selects the acquisition memory RAMs for write or read operation.

*ALL FULL: <73> <84> — Memory Address Register (MAR) status bit that is asserted on the next master clock after the MAR counter reaches full count. It indicates that all data in the acquisition memory RAM is valid.

*BA0-BA12: <68> <79> — Buffered 91A24/91AE24 address lines that connect the DAS Controller board to the 91A24/91AE24 via the CPU bus.

*BD0-BD7: <69> <80> — Buffered data lines on the CPU bus that connect the DAS Controller board to the 91A24/91AE24.

*BRD(L): <68> <79> — Buffered read enable signal from the DAS Controller.

*BWR(L): <68> <79> — Buffered write enable signal from the DAS Controller.

CA0-CA7, CB0-CB7, CC0-CC7: <77> — Clock enable inputs for pod A, B, and C differential clocks in the clock generator.

*CARD ID(L): <69> <80> — Enable signal for readback of card identification register U291.

*CH0-CH7, CH0(L)-CH7(L): <70>, <71>; <81>, <82> — Differential data inputs from a probe.

CH8, CH8(L): <70>, <71> — Incoming, differential qualifier signals from a probe.

CLK, CLK(L): <70>, <71> — Differential clock inputs from a probe.

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* Signals marked with an asterisk occur on both the 91A24 and 91AE24. Signals without an asterisk occur only on the 91A24.

CLK1, CLK1(L); CLK2, CLK2(L); CLK3, CLK3(L): <70> <71> — Differential, buffered clock inputs from probes A, B, and C.

CLK INIT(L): <68> Clock Initialization — Clock pulse programmed low at run time to preset all clock generator flip-flops to a known state.

CLKA, CLKA(L); CLKB, CLKB(L); CLKC, CLKC(L): <78> — Probe A, B, and C differential ECL clock outputs from the clock generator.

*CLK AA, CLK BB, CLK CC: <72> <83> — Probe A, Band C single-ended ECL clock.

*CNTL1(L), CNTL2(L), CNTL3(L): <68> <79> — Control 1, 2, 3 Clocking signals for control registers in the 91A24/91AE24 controller interface.

CNTR CLR(L): <69> Counter Clear — This signal clears counter/timer counters to 000 at load time.

CNTR RDBK0(L): <69> Counter Readback 0 — Counter readback enable signal that enables readback buffer for U585 and U588 <76>

CNTR RDBK1(L): <69> Counter Readback 1 — Counter readback enable signal that enables readback buffer for U591 and U595 <76>

CNTR RESET: <76> Counter Reset — Readback status bit from the trigger circuitry. CNTR RESET, when asserted, indicates that a reset has occurred in timer mode.

CT SEL0, CT SEL1: <68> Counter/Timer Select — Select signals to the counter/timer multiplexer. When CT SEL0 is (H) and CT SEL1 is (H), the timer function is enabled. When CT SEL0 is (L) and CT SEL1 is (H), the counter function is enabled.

*D0-D7: <68> <79> — 91A24/91AE24 data bus whose inputs come from the DAS Controller.

*DATA CLOCK: <69> <80> — Signal line to a data acquisition probe that enables readback of probe status.

*DATA IN: <71> <82> — Data input line to acquisition probe — not active for the 91A24/91AE24.

*DATA OUT A, DATA OUT B, DATA OUT C: <69> <80> — Signal line on which status of data acquisition probe is read.

*DISABLE(L): <74> <85> — 91A24/91AE24 qualification signal. A low on DISABLE(L) stops storage of data in the acquisition memory.

*DISABLE WORD: <74> <85> — Output of data qualifier word recognizer. When high, DISABLE WORD indicates that the programmed disable word has been recognized.

*DQ STATUS(L): <69> <80> Data Qualifier Status — Enables readback buffer for data qualifier and stack word recognizer status — reads STACK WR (91A24 only), RESET, ENABLE/ DISABLE(L) and OR TRIG(L).

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*Signals marked with an asterisk occur on both the 91A24 and 91AE24. Signals without an asterisk occur only on the 91A24.

*DR0-DR23: <73> <84> Data Register — Probe data input that has been processed through the acquisition memory data registers.

*DUAL QUAL: <68> <79> Dual Qualification Control signal from the 91A24/91AE24 controller interface to the data qualifier. When asserted high, DUAL QUAL turns the RESET qualifier into an ENABLE, and the OR Trigger qualifier into a DISABLE.

*DUAL QUAL(L): <74> <85> Dual Qualification Control signal from the data qualifier to the trigger circuitry <76>. When asserted low, DUAL QUAL(L) turns the RESET qualifier into an ENABLE, and the OR Trigger qualifier into a DISABLE.

*ENABLE: <74> <85> — 91A24/91AE24 qualification signal. A high on ENABLE enables storage of data.

ENABLE TRIG: <75> — Signal derived from EXT TRIG EN <75> that holds off the stack word recognizer until EXT TRIG EN is asserted.

*ENABLE WORD: <74> <85> — Output of data qualifier word recognizer. When high, indicates that the programmed enable word has been recognized.

EVENT 1: <76> — Output of the 91A24 trigger circuitry that is used by the DAS Trigger/Time Base event conditioner to develop the 91A24 trigger signals.

EVENT 3: <76> — Output of the 91A24 trigger circuitry that is used by the DAS Trigger/Time Base event conditioner to develop the 91A24 trigger signals.

EXT TRIG EN: <75> External Trigger Enable — External trigger input to the 91A24. Connection is through a BNC connector on the back of the DAS.

FIRST CLK(L): <74> — Storage-enabling signal from the 91A24 to the DAS Trigger board.

FIRST CLK EN(L): <77> First Clock Enable — Enables FIRST CLK(L) to other DAS modules when 91A24 ONLY mode is selected. In modes other than 91A24 ONLY, holds FIRST CLK(L) off.

INT3 CLR(L): <69> Interrupt 3 Clear — Turns off CNTR RESET after counter/timer counters are reset; also clears U491B, removing INT3(L).

INT3 EN: <68> Interrupt 3 Enable — This signal controls the INT3(L) line. Enables INT3(L) when counter and timer functions are selected. A low on INT3 EN holds off INT3(L).

INT3(L): <76> Interrupt 3 — Readback status line for interrupt 3.

*LID0-LID23: <72> <83> Login Data — Probe input data at the outputs of the probe data login registers.

*LB0-LB7: <68> <79> Load Bus — Derived data signals from the DAS Controller BD0-BD7 bus.

LOAD OCCR CNTR AFTER RESET(L): <76> — Generated at run time in normal mode whenever a reset occurs. When asserted, the signal causes the occurrence counter to be reprogrammed at level 0 when a reset occurs.

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* Signals marked with an asterisk occur on both the 91A24 and 91AE24. Signals without an asterisk occur only on the 91A24.

MAP REG(L): <68> Map Register — Clock signal that drives U968 <68> to select a particular 91A24 ROM for readout.

*MAR CLOCK: <73> <84> Memory Address Register (MAR) Clock — Clocking signal that increments the MAR.

*MAR LD0(L): <68> <79> MAR Load 0 — Signal from the 91A24/91AE24 controller interface that enables loading the lower 8 bits (MAR0-MAR7) of the MAR counter.

*MAR LD1(L): <68> <79> MAR Load 1 — Signal from the 91A24/91AE24 controller interface that enables loading the upper 2 bits (MAR8, MAR9) of the MAR counter.

*MAR EN(L): <74> <85> MAR Enable Enable signal from the data qualifier that, when asserted low, causes the MAR to be incremented on the next clock. MAR EN(L) allows qualified data to be written into the acquisition memory.

*MAR HIGH(L): <69> <80> — Enables readback buffer U235 <69> <80> to allow sampling of MAR8, MAR9, STORING DATA, ALL FULL, and SP0-SP3 by the DAS Controller.

*MAR LOW(L): <69> <80> MAR Low — Enables readback buffer U135 <69> <80> to allow sampling of MAR0-MAR7 by the DAS Controller.

*MAR0-MAR9: <73> <84> — MAR counter outputs that address the acquisition memory RAMs.

*MASTER CLK I (91A24 only), MASTER CLK 11,MASTER CLK 111: <77> <87> — 91A24/91AE24 internal clock, divided into two (91AE24) or three (91A24) separate clocks for fanout reasons.

*MEM RD: <68> <79> Memory Read — Signal that asserts MAR EN(L) after the delay counter has finished, enabling the MAR to read data from the acquisition memory.

*MUX MODE: <68> <79> Multiplexer Mode — Signal that allows the demultiplexing of probe A data by the probe A clock through U118 <72> <83> and by the probe B clock through U121.

NEVER TRIG(L): <68> — Asserted when NEVER TRIG or INCR CNTR is selected in the menu; prevents triggering in stack word recognizer, but does not affect OR TRIG.

*OC(L): <77> <87> Output Control — Output enable signal for a number of flip-flops.

OCCR CLK(L): <68> Occurrence Clock — Signal from the 91A24 controller interface to the stack occurrence counter that is used only during diagnostics to clock the stack occurrence counter.

OCCR CNTR RAM LD0(L): <68> Occurrence Counter RAM Load 0 — Signal that loads the lower 8 bits of the occurrence count for a specific stack level into stack occurrence counter RAMs U155 and U255.

OCCR CNTR RAM LD1(L): <68> Occurrence Counter RAM Load 1 — Signal that loads the upper 4 bits of the occurrence count for a specific stack level into Stack Occurrence Counter RAM U455.

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* Signals marked with an asterisk occur on both the 91A24 and 91AE24. Signals without an asterisk occur only on the 91A24.

OCCR CNTR LD(L): <68> Occurrence Counter Load — Signal from the 91A24 controller interface to the stack occurrence counter that loads the occurrence count from the stack occurrence counter RAMs into the stack occurrence counter <75>.

OCCR1-OCCR3: <75> Occurrence — Signal lines that sample the status of the stack occurrence counter for readback (through U771 <69>).

*OR TRIG(L): <74> <85> — Signal derivation of OR TRIG WORD that will cause the 91A24 to trigger independently from the stack word recognizer when the 91A24 is in normal mode, and functions as a disable word in dual qualification mode. OR Trigger = disable is programmed as OR IF in the Trigger Specification menu on the line below END STORE.

*OR TRIGGER(L): <74> <85> — Signal derived from OR TRIG(L) that will trigger the 91A24 independently from the stack word recognizer in normal mode.

*OR TRIG WORD: <74> <85> — Output of data qualifier word recognizer. When high, indicates that the programmed OR trigger word has been recognized.

*OFFSET SENSE: <71> <82> — Acquisition probe sense line for offset voltage.

*PAD0-PAD7, PBD0-PBD7, PCD0-PCD7: <70>, <71>; <81>, <82> — Probe input data for Probes A, B, or C (TTL-level).

PAQA(L)-PAQC(L), PBQA(L)-PBQC(L), PCQA(L)-PCQC(L): <77> — Probe A, B, and C qualifiers A-C from the clock qualifier generator <77> to the clock generator <78>.

*PADQ WE(L), PBDQ WE(L), PCDQ WE(L): <68> <79> — Probe A, B, and C data qualifier write enable signals from the 91A24/91AE24 controller interface to the data qualifier RAMs <74>.

*PC0, PC2, PC4: <68> <79> Pod Control — Signals from the controller interface that clock the clock registers <77> <87> in order to logically combine and select probe clocks.

PC1, PC3, PC5: <68> Pod Control — Signals from the controller interface that clock the clock-qualifier registers <77> in order to logically combine and select probe qualifiers.

PERSONALITY(L): <68> — A memory map output from the DAS Controller that enables selection and readout of the 91A24 personality ROMs.

*POD STATUS(L): <69> <80> — Enable line to read back buffer U775 <69> <80> that allows sampling of probe status lines DATA OUT A, DATA OUT B, and DATA OUT C.

POINTER CLK: <75> — Signal from the stack occurrence counter <75> to the stack pointer <76> that increments the stack pointer by 1.

POINTER INC(L): <75> Pointer Increment — Signal from the occurrence counter output that enables the function that is specified upon recognition of an event. The function may be to increment the stack pointer, enable or disable the timer, trigger, or assert the SYNC OUT signal.

*PORT(L): <68> <79> — Signal from the DAS Controller to the 91A24/91AE24 that, when asserted with BRD(L) or BWR(L), enables read and write operations to and from the 91A24/91AE24.

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*Signals marked with an asterisk occur on both the 91A24 and 91AE24. Signals without an asterisk occur only on the 91A24.

*PROBE R/W(L): <68> <79> — Signal that enables reads to, and writes from, the data acquisition probes.

QA, QA(L); QB, QB(L); QC, QC(L): <70> <71> — Differential qualifier input signals from probes A, B, and C.

QA0-QA5, QB0-QB5, QC0-QC5: <77> — These signals program the clock qualifiers. In each of the three groups of six signals, bits 0 and 1 program the probe A qualifiers; bits 2 and 3 program the probe B qualifiers; and bits 4 and 5 program the probe C qualifiers.

*R(L)/W(H): <71> <82> — Data acquisition probe read/write enable line.

*RD(L): <68> <79> Read — Read enable signal from the DAS Controller.

*READ ACQ: <68> <79> Read Acquisition — Input to the acquisition memory that disables the data registers during acquisition memory readback <73> <84>.

*RESET: <74> <85> — Signal derived from RESET WORD, that resets the stack word recognizer to 0 in normal mode, and functions as a second enable word in dual qualification mode. The reset = enable function is initiated by programming line two in the Trigger Specification menu with OR IF.

RESET(L): <76> — Reset signal from the DAS Controller to the 91A24.

*RESET WORD: <74> <85> — Output of data qualifier word recognizer. When high, indicates that the programmed reset word has been recognized.

RESET CNTR EN(L): <68> Reset Counter Enable — Input to the trigger circuitry that allows the counter/timer counters to be cleared.

*SC0-SC3: <75> <86> Stack Control — Stack control status bits from the stack control RAM.
SC0: Trigger bit - When low, disables the stack pointer and causes the 91A24 to trigger.
SC1: Counter and timer enable bit; readback only on 91AE24.
SC2: Sync out bit; readback only on 91AE24.
SC3: Creates NOT function for stack word recognizer output.

SEL SLOT(L): <68> Select Slot — Signal from the DAS Controller slot select logic that, along with RD(L) addresses U971 <68> and enables selection and readout of the 91A24 personality ROMs.

*SINGLE STEP(L): <68> <79> — Signal that, when asserted, initiates the 91A24/91AE24 master clock in a single-step fashion during diagnostics setup, and at load time.

*SINGLE STEP TTL(L): <77> <87> — Signal that, when asserted, initiates the 91A24/91AE24 master clock in a single-step fashion during diagnostics and at load time.

*SP0-SP3: <76> <86> Stack Pointer — Outputs from the stack pointer <76> <86> that indicate the current stack pointer level.

*STACK A WE(L), STACK B WE(L), STACK C WE(L): <68> <79> — Write enable signals from the 91A24/91AE24 controller interface to the stack word recognizer RAMs.

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* Signals marked with an asterisk occur on both the 91A24 and 91AE24. Signals without an asterisk occur only on the 91A24.

*STACK CNTL RD(L): <69> <80> Stack Control Read — Enables readback buffer U785 <69> <80> for CNTR RESET (91A24 only) and SC0-SC3.

*STACK CNTL(L): <68> <79> Stack Control — Write enable signal for the stack control RAM <75> <86>.

*STACK PTR LD (L): <68> <79> Stack Pointer Load — Stack pointer load enable signal from the 91A24/91AE24 controller interface.

*STACK PTR CLK(L): <68> <79> Stack Pointer Clock — Clocking signal that loads the stack pointer from the LB0-LB3 bus at load time.

*STACK CLK EN(L): <68> <79> Stack Clock Enable — Clocks the stack pointer counter to set it to 00 at load time.

*STACK WR: <75> Stack Word Recognizer — Stack word recognizer status line that is read back by the DAS Controller through U778 <69>.

*STACK WR(L): <75> <86> Stack Word Recognizer — Stack word recognizer output <75> <86>.

*STORING DATA: <74> <85>, STORING DATA(L) <74>, <85> — Output of the data qualifier that establishes enable storage status and maintains it until a DISABLE word occurs.

*SW0-SW2: <75> <86> Stack word recognizer — These signals are the outputs of the stack word recognizer RAMs. SW0 corresponds to probe A, SW1 to probe B, and SW2 to probe C.

SYNC OUT: <76> — Synchronizing output signal from the 91A24 that is asserted when programmed in the Trigger Specification menu.

*THRESHOLD(L): <68> <79> — Enable line for digital-to-analog converter U918 <71> <82>. When THRESHOLD(L) is asserted, the threshold voltage encoded on the D0-D7 inputs of U918 is output on U918 pin 18.

TIMER CLK(L): <68> — Clocking signal for the counter/timer, used only for diagnostic routines.

*TN0-TN2: <68> <79> Then Not — Signal lines exclusive-ORed to the outputs of the RESET, DISABLE and OR TRIG data qualifier word recognizers. These lines control the polarity of RESET, DISABLE(L) and OR TRIG(L). This includes the programmed THEN NOT function on the Trigger Specification menu.

TRIG CLK: <74> — A trigger clocking signal, delayed in the trigger circuitry, that asserts EVENT1 <76> to indicate the 91A24 has triggered, and enable the delay counter.

*TRIGGERED RD(L): <69> <80> Triggered Read — Signal that enables readback buffer U771 <69> <80> and allows sampling of INT3(L) (91A24 only), TRIGGERED(L) (91A24 only), OCCR1OCCR3 (91A24 only), and SW0-SW2.

TRIGGERED(L): <76> — Used during diagnostic routines to verify trigger circuitry.

*USER GND: <71> <82> — Acquisition probe line which senses user's system ground.

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*Signals marked with an asterisk occur on both the 91A24 and 91AE24. Signals without an asterisk occur only on the 91A24.

*VTHRESH SENSE: <71> <82> — Voltage Threshold Sense Part of acquisition probe feedback circuitry to control threshold voltage.

*VTHRESH: <71> <82> — Voltage threshold line from the 91A24/91AE24 to the data acquisition probe.

*Vbb: <72> <83> — Voltage source which sets threshold for ECL-to-TTL translator transistors.

*WEA(L)-WEC(L): <68> <79> — Write enable lines (one for each probe) to the acquisition memory RAMs <73> <84>.

*WR(L): <68> <79> Write — Write enable signal from the DAS Controller.

91A08 CLK(L): <78> — DAS internal clock, generated by the DAS Trigger/Time Base. May be selected by the 91A24 as system clock when user selects internal clock on Clock Specification Menu.

91A24 INIT(L): <68> 91A24 Initialize — Multi-purpose signal from the 91A24 controller interface.

91A24 INIT(L): when asserted
1. Holds off the data qualifier word recognizers <74>;
2. Holds off the stack word recognizer and stack trigger. <75>, <76>.
3. Holds off the OR trigger <76>.

91A24 TRIG DIS(L): <68> Trigger Disable — When asserted low, sends EVENT 3 high, and EVENT 1 low, disabling the 91A24 trigger, and enabling 91A32 operation. When high, holds off Q952 <76>, disabling EVENT 3 and enabling EVENT 1.

91A32 CLK(L): <78> — DAS internal clock, generated by the DAS Trigger/Time Base. May be selected by the 91A24 as system clock when user selects internal clock on Clock Specification Menu.

*91A32 QUALIFIER: <74> <85> — Signal from the DAS Trigger/Time Base that controls the 91A24 start and stop. A low on 91A32 QUALIFIER disables the data qualifier word recognizers.

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*Signals marked with an asterisk occur on both the 91A24 and 91AE24. Signals without an asterisk occur only on the 91A24.

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.　　　　　component number

A23R1234　　　　A23　　R1234

Assembly number　　　　　　　Circuit number

Read: Resistor 1234 of Assembly 23

Example b.　　　　　　component number

A23A2R1234　　A23　　A2　R1234

Assembly number　　　　Subassembly number　Circuit number

Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC.		
	SEMICONDUCTOR GROUP	P.O. BOX 5012	DALLAS, TX 75222
01961	PULSE ENGINEERING, INC.	7250 CONVOY COURT	SAN DIEGO, CA 92111
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867	MYRTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF		
	FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
18324	SIGNETICS CORP.	811 E. ARQUES	SUNNYVALE, CA 94086
24546	CORNING GLASS WORKS, ELECTRONIC		
	COMPONENTS DIVISION	550 HIGH STREET	BRADFORD, PA 16701
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
32997	BOURNS, INC., TRIMPOT PRODUCTS DIV.	1200 COLUMBIA AVE.	RIVERSIDE, CA 92507
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL.	SUNNYVALE, CA 94086
34649	INTEL CORP.	3065 BOWERS AVE.	SANTA CLARA, CA 95051
55680	NICHICON/AMERICA/CORP.	6435 N PROESEL AVENUE	CHICAGO, IL 60645
56289	SPRAGUE ELECTRIC CO.	87 MARSHALL ST.	NORTH ADAMS, MA 01247
57668	R-OHM CORP.	16931 MILLIKEN AVE.	IRVINE, CA 92713
57924	BOURNS INC NETWORKS DIV 12155	MAGNOLIA AVE	RIVERSIDE, CA 92503
59660	TUSONIX INC.	2155 N FORBES BLVD	TUCSON, AZ 85705
73138	BECKMAN INSTRUMENTS, INC., HELIPOT DIV.	2500 HARBOR BLVD.	FULLERTON, CA 92634
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601
96733	SAN FERNANDO ELECTRIC MFG CO	1501 FIRST ST	SAN FERNANDO, CA 91341

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1	670-7933-00			CKT BOARD ASSY:DATA ACQUISITION MODULE	80009	670-7933-00
A2	670-7944-00			CKT BOARD ASSY:DATA ACQUISITION MODULE	80009	670-7944-00
A1	670-7933-00			CKT BOARD ASSY:DATA ACQUISITION MODULE	80009	679-7933-00
A1C101	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C126	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C129	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C136	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C143	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C158	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C163	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C165	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A1C190	281-0809-00			CAP.,FXD,CER DI:200PF,5%,100V	96733	R2915
A1C201	283-0204-00			CAP.,FXD,CER DI:0.01UF,20%,50V	96733	R2676
A1C202	283-0204-00			CAP.,FXD,CER DI:0.01UF,20%,50V	96733	R2676
A1C222	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C232	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C262	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C302	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C318	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C319	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C361	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C371	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C378	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C388	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C395	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C396	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A1C397	281-0798-00			CAP.,FXD,CER DI:51PF,1%,100V	96733	R2928
A1C401	283-0204-00			CAP.,FXD,CER DI:0.01UF,20%,50V	96733	R2676
A1C402	283-0204-00			CAP.,FXD,CER DI:0.01UF,20%,50V	96733	R2676
A1C403	283-0204-00			CAP.,FXD,CER DI:0.01UF,20%,50V	96733	R2676
A1C405	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C429	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C432	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C439	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C467	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A1C468	281-0167-00			CAP.,VAR,CER DI:9-45PF,200V	59660	538-011D9-45
A1C476	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C486	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C502	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C505	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C508	283-0204-00			CAP.,FXD,CER DI:0.01UF,20%,50V	96733	R2676
A1C524	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C541	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C544	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C549	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C558	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C566	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C573	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C586	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C588	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C591	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C595	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C597	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1C622	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C668	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C681	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C697	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C702	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A1C703	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A1C704	283-0422-00			CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
A1C705	283-0422-00			CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
A1C707	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C708	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C711	283-0422-00			CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
A1C712	283-0422-00			CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
A1C716	283-0422-00			CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
A1C718	283-0422-00			CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
A1C719	290-0891-00			CAP.,FXD,ELCTLT:1UF,+75-10%,50V	55680	ULA1H010TEA
A1C722	290-0891-00			CAP.,FXD,ELCTLT:1UF,+75-10%,50V	55680	ULA1H010TEA
A1C726	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C741	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C751	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A1C752	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A1C753	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A1C759	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C782	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C786	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C789	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C801	283-0204-00			CAP.,FXD,CER DI:0.01UF,20%,50V	96733	R2676
A1C802	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A1C803	283-0422-00			CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
A1C804	283-0204-00			CAP.,FXD,CER DI:0.01UF,20%,50V	96733	R2676
A1C806	283-0204-00			CAP.,FXD,CER DI:0.01UF,20%,50V	96733	R2676
A1C808	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C809	281-0816-00			CAP.,FXD,CER DI:82PF,5%,100V	96733	R3247
A1C810	283-0422-00			CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
A1C813	283-0422-00			CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
A1C814	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A1C823	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C825	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C838	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C846	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C851	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A1C852	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A1C853	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A1C865	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C868	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C871	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C878	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C889	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C901	290-0743-00			CAP.,FXD,ELCTLT:100UF,+50-10%,16V	56289	500D146
A1C902	283-0164-00			CAP.,FXD,CER DI:2.2UF,20%,25V	04222	SR402E225MAA
A1C903	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C904	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C906	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A1C910	283-0422-00			CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
A1C925	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z

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A1C931	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C942	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C965	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1CR708	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR709	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR710	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR711	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR715	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR716	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR717	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR718	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR808	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR809	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR812	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR813	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR908	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR909	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1DL115	119-1664-00			DELAY LINE,ELEC:22NS,200 OHM	01961	PE22612
A1DL195	119-1381-00			DELAY LINE,ELEC:30NS,100 OHM,TAPPED	01961	PE 20664
A1DL315	119-1664-00			DELAY LINE,ELEC:22NS,200 OHM	01961	PE22612
A1DL415	119-1664-00			DELAY LINE,ELEC:22NS,200 OHM	01961	PE22612
A1Q101	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q102	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q103	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q104	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q105	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q106	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q107	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q108	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q109	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q110	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q111	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q112	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q113	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q114	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q115	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q116	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q301	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q302	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q303	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q304	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q305	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q306	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q307	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q308	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q309	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q310	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q311	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q312	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q313	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q314	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q315	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q316	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q318	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236

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A1Q319	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236
A1Q465	151-0447-00			TRANSISTOR:SILICON,NPN	04713	SRF502-1
A1Q501	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q502	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q503	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q504	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q505	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q506	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q507	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q508	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q509	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q510	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q511	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q512	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q513	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q514	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q515	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q516	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q519	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236
A1Q520	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236
A1Q539	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236
A1Q540	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236
A1Q543	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236
A1Q544	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236
A1Q545	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236
A1Q546	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236
A1Q596	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A1Q598	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A1Q628	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236
A1Q629	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236
A1Q901	151-0429-00			TRANSISTOR:SILICON,PNP	04713	SJE957
A1Q902	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A1Q951	151-0301-00			TRANSISTOR:SILICON,PNP	27014	2N2907A
A1Q952	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A1R101	307-0695-00			RES NTWK,FXD FI:9,150 OHM,2%,0.2W EACH	01121	110A151
A1R102	307-0695-00			RES NTWK,FXD FI:9,150 OHM,2%,0.2W EACH	01121	110A151
A1R103	311-1245-00			RES.,VAR,NONWIR:10K OHM,10%,0.50W	73138	72-28-0
A1R104	321-0763-07			RES.,FXD,FILM:1.12K OHM,0.1%,0.125W	91637	MFF1816C11200B
A1R106	307-0486-00			RES,NTWK,THK FI:100 OHM,20%,1.125W	91637	MSP10A01-101J
A1R107	307-0736-00			RES,NTWK,THK FI:10,390 OHM,2%,0.19W	91637	CSP11G01391G
A1R108	307-0832-00			RES NTWK,FXD,FI:9,120 OHM,2%,0.15W	01121	210A121
A1R110	311-1236-00			RES.,VAR,NONWIR:250 OHM,10%,0.50W	73138	72-22-0
A1R114	307-0674-00			RES NTWK,THK,FI:9,430 OHM,2%,1.25W	01121	210A431
A1R115	307-0592-00			RES,NTWK,FXD FI:9,220 OHM,2%,2W	91637	MSP10A01-221G
A1R149	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A1R162	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A1R166	307-0540-00			RES,NTWK,FXD,FI:(5) 1K OHM,10%,0.7W	57924	4306R-101-102
A1R185	307-0598-00			RES NTWK,FXD FI:7,330 OHM,2%,1.0W	91637	MSP08A01331G
A1R186	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A1R187	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A1R190	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A1R191	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A1R196	321-0140-00			RES.,FXD,FILM:280 OHM,1%,0.125W	91637	MFF1816G280R0F
A1R197	321-0124-00			RES.,FXD,FILM:191 OHM,1%,0.125W	91637	MFF1816G191R0F

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A1R198	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R266	307-0717-00			RES NTWK,FXD FI:4,100 OHM,2%,0.3W	01121	208B101
A1R273	307-0546-00			RES NTWK,FXD FI:5,75 OHM,5%,0.15W	91637	MSP06A01750J
A1R278	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A1R281	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A1R296	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A1R297	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A1R306	307-0486-00			RES,NTWK,THK FI:100 OHM,20%,1.125W	91637	MSP10A01-101J
A1R307	307-0736-00			RES,NTWK,THK FI:10,390 OHM,2%,0.19W	91637	CSP11G01391G
A1R308	307-0832-00			RES NTWK,FXD,FI:9,120 OHM,2%,0.15W	01121	210A121
A1R314	307-0674-00			RES NTWK,THK,FI:9,430 OHM,2%,1.25W	01121	210A431
A1R315	307-0592-00			RES,NTWK,FXD FI:9,220 OHM,2%,2W	91637	MSP10A01-221G
A1R381	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A1R391	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A1R397	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A1R398	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A1R399	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A1R401	307-0695-00			RES NTWK,FXD FI:9,150 OHM,2%,0.2W EACH	01121	110A151
A1R414	307-0674-00			RES NTWK,THK,FI:9,430 OHM,2%,1.25W	01121	210A431
A1R415	307-0592-00			RES,NTWK,FXD FI:9,220 OHM,2%,2W	91637	MSP10A01-221G
A1R419	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A1R459	307-0540-00			RES,NTWK,FXD,FI:(5) 1K OHM,10%,0.7W	57924	4306R-101-102
A1R467	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A1R468	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A1R491	307-0541-00			RES,NTWK,THK FI:(7)1K OHM,10%,1W	91637	MSP08A01-102G
A1R502	307-0695-00			RES NTWK,FXD FI:9,150 OHM,2%,0.2W EACH	01121	110A151
A1R506	307-0486-00			RES,NTWK,THK FI:100 OHM,20%,1.125W	91637	MSP10A01-101J
A1R507	307-0736-00			RES,NTWK,THK FI:10,390 OHM,2%,0.19W	91637	CSP11G01391G
A1R508	307-0832-00			RES NTWK,FXD,FI:9,120 OHM,2%,0.15W	01121	210A121
A1R526	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A1R529	307-0488-00			RES,NTWK,FXD,FI:100 OHM,20%,0.75W	01121	106A101
A1R534	307-0546-00			RES NTWK,FXD FI:5,75 OHM,5%,0.15W	91637	MSP06A01750J
A1R536	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R538	307-0546-00			RES NTWK,FXD FI:5,75 OHM,5%,0.15W	91637	MSP06A01750J
A1R539	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A1R540	315-0111-00			RES.,FXD,CMPSN:110 OHM,5%,0.25W	01121	CB1115
A1R541	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A1R544	315-0111-00			RES.,FXD,CMPSN:110 OHM,5%,0.25W	01121	CB1115
A1R545	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A1R546	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R547	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R548	315-0111-00			RES.,FXD,CMPSN:110 OHM,5%,0.25W	01121	CB1115
A1R549	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A1R572	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R585	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R595	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A1R596	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A1R598	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R599	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A1R624	307-0546-00			RES NTWK,FXD FI:5,75 OHM,5%,0.15W	91637	MSP06A01750J
A1R631	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A1R658	307-0675-00			RES NTWK,FXD FI:9,1K OHM,2%,1.25W	01121	210A102
A1R698	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A1R699	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015

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A1R701	307-0695-00			RES NTWK,FXD FI:9,150 OHM,2%,0.2W EACH	01121	110A151
A1R702	307-0695-00			RES NTWK,FXD FI:9,150 OHM,2%,0.2W EACH	01121	110A151
A1R703	315-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	01121	CB3925
A1R704	315-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	01121	CB3925
A1R706	321-0414-04			RES.,FXD,FILM:200K OHM,0.1%,0.125W	91637	MFF1816D20002B
A1R707	321-0414-04			RES.,FXD,FILM:200K OHM,0.1%,0.125W	91637	MFF1816D20002B
A1R708	321-0318-07			RES.,FXD,FILM:20K OHM,0.1%,0.125W	24546	NE55E2002B
A1R709	321-0318-07			RES.,FXD,FILM:20K OHM,0.1%,0.125W	24546	NE55E2002B
A1R710	321-0318-07			RES.,FXD,FILM:20K OHM,0.1%,0.125W	24546	NE55E2002B
A1R711	321-0318-07			RES.,FXD,FILM:20K OHM,0.1%,0.125W	24546	NE55E2002B
A1R715	321-0289-02			RES.,FXD,FILM:10K OHM,0.5%,0.125W	91637	CMF55-116D10001D
A1R716	321-0289-02			RES.,FXD,FILM:10K OHM,0.5%,0.125W	91637	CMF55-116D10001D
A1R717	321-0924-07			RES.,FXD,FILM:40K OHM,0.1%,0.125W	91637	MFF1816C40001B
A1R718	321-0924-07			RES.,FXD,FILM:40K OHM,0.1%,0.125W	91637	MFF1816C40001B
A1R720	321-0289-02			RES.,FXD,FILM:10K OHM,0.5%,0.125W	91637	CMF55-116D10001D
A1R721	321-0289-02			RES.,FXD,FILM:10K OHM,0.5%,0.125W	91637	CMF55-116D10001D
A1R722	307-0489-00			RES,NTWK,FXD,FI:100 OHM,20%,1W	57924	4308R-101-101
A1R723	307-0832-00			RES NTWK,FXD,FI:9,120 OHM,2%,0.15W	01121	210A121
A1R731	307-0546-00			RES NTWK,FXD FI:5,75 OHM,5%,0.15W	91637	MSP06A01750J
A1R737	307-0539-00			RES NTWK,THK FI:(7)510 OHM,10%,1W	01121	208A511
A1R746	307-0539-00			RES NTWK,THK FI:(7)510 OHM,10%,1W	01121	208A511
A1R749	307-0546-00			RES NTWK,FXD FI:5,75 OHM,5%,0.15W	91637	MSP06A01750J
A1R751	307-0719-00			RES NTWK,FXD,FI:9,1.5K OHM,1%,0.15W EACH	32997	4310R101152F
A1R753	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A1R754	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R772	307-0446-00			RES,NTWK,FXD FI:10K OHM,20%,(9) RES	91637	MSP10A01-103M
A1R793	307-0675-00			RES NTWK,FXD FI:9,1K OHM,2%,1.25W	01121	210A102
A1R798	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R799	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A1R801	315-0390-00			RES.,FXD,CMPSN:39 OHM,5%,0.25W	01121	CB3905
A1R803	321-0414-04			RES.,FXD,FILM:200K OHM,0.1%,0.125W	91637	MFF1816D20002B
A1R804	315-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	01121	CB3925
A1R808	321-0318-07			RES.,FXD,FILM:20K OHM,0.1%,0.125W	24546	NE55E2002B
A1R810	321-0318-07			RES.,FXD,FILM:20K OHM,0.1%,0.125W	24546	NE55E2002B
A1R811	321-0289-02			RES.,FXD,FILM:10K OHM,0.5%,0.125W	91637	CMF55-116D10001D
A1R812	321-0924-07			RES.,FXD,FILM:40K OHM,0.1%,0.125W	91637	MFF1816C40001B
A1R813	321-0318-07			RES.,FXD,FILM:20K OHM,0.1%,0.125W	24546	NE55E2002B
A1R814	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A1R823	321-0261-00			RES.,FXD,FILM:5.11K OHM,1%,0.125W	91637	MFF1816G51100F
A1R824	307-0611-00			RES NTWK,FXD FI:7,150 OHM,5%,1.125W	32997	4308R101-151J
A1R831	307-0546-00			RES NTWK,FXD FI:5,75 OHM,5%,0.15W	91637	MSP06A01750J
A1R842	307-0539-00			RES NTWK,THK FI:(7)510 OHM,10%,1W	01121	208A511
A1R849	307-0546-00			RES NTWK,FXD FI:5,75 OHM,5%,0.15W	91637	MSP06A01750J
A1R901	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A1R902	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A1R904	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A1R905	321-0222-07			RES.,FXD,FILM:2K OHM,0.1%,0.125W	91637	MFF1816C20000B
A1R906	321-0239-00			RES.,FXD,FILM:3.01K OHM,1%,0.125W	91637	MFF1816G30100F
A1R907	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A1R908	321-0318-07			RES.,FXD,FILM:20K OHM,0.1%,0.125W	24546	NE55E2002B
A1R910	321-0289-02			RES.,FXD,FILM:10K OHM,0.5%,0.125W	91637	CMF55-116D10001D
A1R911	321-0289-02			RES.,FXD,FILM:10K OHM,0.5%,0.125W	91637	CMF55-116D10001D
A1R912	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A1R913	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015

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A1R914	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A1R915	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A1R916	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A1R917	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R918	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9) RES	91637	MSP10A01-472M
A1R921	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A1R924	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A1R948	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A1R949	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A1R950	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A1R951	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A1R952	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A1R953	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R954	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A1R955	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A1R956	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R958	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A1R959	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A1R960	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9) RES	91637	MSP10A01-472M
A1R961	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A1R962	315-0432-00			RES.,FXD,CMPSN:4.3K OHM,5%,0.25W	01121	CB4325
A1R969	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A1R970	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A1U118	156-1704-00			MICROCIRCUIT,DI:OCTAL D-TYPE FF,W/3-ST OUT	07263	74F374(PCQR OR D
A1U121	156-1704-00			MICROCIRCUIT,DI:OCTAL D-TYPE FF,W/3-ST OUT	07263	74F374(PCQR OR D
A1U125	156-0982-02			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-02
A1U128	156-1704-00			MICROCIRCUIT,DI:OCTAL D-TYPE FF,W/3-ST OUT	07263	74F374(PCQR OR D
A1U131	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A1U135	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A1U138	156-1198-01			MICROCIRCUIT,DI:SYNCHRONOUS 4 BIT CNTR	01295	SN74S163J4
A1U141	156-1695-00			MICROCIRCUIT,DI:SRAM,1024 X 4	34649	D2149H-2/S7570
A1U145	156-1695-00			MICROCIRCUIT,DI:SRAM,1024 X 4	34649	D2149H-2/S7570
A1U148	156-1690-00			MICROCIRCUIT,DI:SCAM,4096 X 1	34649	D2147H-2/S7578
A1U151	156-1360-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1360-01
A1U155	156-1189-00			MICROCIRCUIT,DI:16 X 4 RAM	34335	AM74S189J
A1U158	156-1183-00			MICROCIRCUIT,DI:PRESET BINARY LATCH/CNTR	80009	156-1183-00
A1U161	156-0472-03			MICROCIRCUIT,DI:13 INPUT NAND GATE,SCRN	01295	SN74S133
A1U165	156-0331-03			MICROCIRCUIT,DI:DUAL D TYPE POS EDGE TRIG	80009	156-0331-03
A1U168	156-1680-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT & GATE	01295	SN74S15
A1U198	156-0739-02			MICROCIRCUIT,DI:QUAD 2 INP OR GATE,SCRN	01295	SN74S32
A1U218	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A1U221	156-1704-00			MICROCIRCUIT,DI:OCTAL D-TYPE FF,W/3-ST OUT	07263	74F374(PCQR OR D
A1U225	156-0982-02			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-02
A1U228	156-1704-00			MICROCIRCUIT,DI:OCTAL D-TYPE FF,W/3-ST OUT	07263	74F374(PCQR OR D
A1U231	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A1U235	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A1U238	156-1198-01			MICROCIRCUIT,DI:SYNCHRONOUS 4 BIT CNTR	01295	SN74S163J4
A1U241	156-1695-00			MICROCIRCUIT,DI:SRAM,1024 X 4	34649	D2149H-2/S7570
A1U245	156-1695-00			MICROCIRCUIT,DI:SRAM,1024 X 4	34649	D2149H-2/S7570
A1U248	156-1690-00			MICROCIRCUIT,DI:SCAM,4096 X 1	34649	D2147H-2/S7578
A1U255	156-1189-00			MICROCIRCUIT,DI:16 X 4 RAM	34335	AM74S189J
A1U258	156-1183-00			MICROCIRCUIT,DI:PRESET BINARY LATCH/CNTR	80009	156-1183-00
A1U261	156-1680-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT & GATE	01295	SN74S15
A1U265	156-0459-02			MICROCIRCUIT,DI:QUAD 2 INPUT & GATE,BURN	01295	SN74S08

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A1U268	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A1U275	156-1640-01			MICROCIRCUIT,DI:SCREENED	04713	MC10H116(LD OR P
A1U278	156-0403-02			MICROCIRCUIT,DI:HEX INVERTER,SCRN	01295	SN74S05
A1U281	156-0703-02			MICROCIRCUIT,DI:4-2-3-2 INPUT & OR GATE	07263	74S64
A1U285	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A1U288	156-0703-02			MICROCIRCUIT,DI:4-2-3-2 INPUT & OR GATE	07263	74S64
A1U291	156-1800-00			MICROCIRCUIT,DI:QUAD 2 INPUT EXCLUSIVE OR	07263	74F86(PCQR OR DC
A1U295	156-0325-02			MICROCIRCUIT,DI:DUAL 4-1 LINE DATA,BURN-IN	01295	SN74S153JP3
A1U298	156-0331-03			MICROCIRCUIT,DI:DUAL D TYPE POS EDGE TRIG	80009	156-0331-03
A1U351	156-1360-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1360-01
A1U421	156-1704-00			MICROCIRCUIT,DI:OCTAL D-TYPE FF,W/3-ST OUT	07263	74F374(PCQR OR D
A1U425	156-0982-02			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-02
A1U428	156-1704-00			MICROCIRCUIT,DI:OCTAL D-TYPE FF,W/3-ST OUT	07263	74F374(PCQR OR D
A1U431	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A1U438	156-1198-01			MICROCIRCUIT,DI:SYNCHRONOUS 4 BIT CNTR	01295	SN74S163J4
A1U441	156-1695-00			MICROCIRCUIT,DI:SRAM,1024 X 4	34649	D2149H-2/S7570
A1U445	156-1695-00			MICROCIRCUIT,DI:SRAM,1024 X 4	34649	D2149H-2/S7570
A1U448	156-1690-00			MICROCIRCUIT,DI:SCAM,4096 X 1	34649	D2147H-2/S7578
A1U455	156-1189-00			MICROCIRCUIT,DI:16 X 4 RAM	34335	AM74S189J
A1U458	156-1183-00			MICROCIRCUIT,DI:PRESET BINARY LATCH/CNTR	80009	156-1183-00
A1U461	156-0331-03			MICROCIRCUIT,DI:DUAL D TYPE POS EDGE TRIG	80009	156-0331-03
A1U468	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A1U471	156-0331-03			MICROCIRCUIT,DI:DUAL D TYPE POS EDGE TRIG	80009	156-0331-03
A1U475	156-0459-02			MICROCIRCUIT,DI:QUAD 2 INPUT & GATE,BURN	01295	SN74S08
A1U478	156-0331-03			MICROCIRCUIT,DI:DUAL D TYPE POS EDGE TRIG	80009	156-0331-03
A1U481	156-0331-03			MICROCIRCUIT,DI:DUAL D TYPE POS EDGE TRIG	80009	156-0331-03
A1U485	156-0690-03			MICROCIRCUIT,DI:QUAD 2 INP NOR GATE,BURN IN	01295	SN74S02
A1U488	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A1U491	156-0331-03			MICROCIRCUIT,DI:DUAL D TYPE POS EDGE TRIG	80009	156-0331-03
A1U495	156-0403-02			MICROCIRCUIT,DI:HEX INVERTER,SCRN	01295	SN74S05
A1U535	156-1682-00			MICROCIRCUIT,DI:DUAL 4-5 INPUT OR/NOR GATE	04713	MC10H109(LD OR P
A1U538	156-1682-00			MICROCIRCUIT,DI:DUAL 4-5 INPUT OR/NOR GATE	04713	MC10H109(LD OR P
A1U551	156-1360-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1360-01
A1U555	156-1189-00			MICROCIRCUIT,DI:16 X 4 RAM	34335	AM74S189J
A1U558	156-0304-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	01295	SN74S20
A1U561	156-0459-02			MICROCIRCUIT,DI:QUAD 2 INPUT & GATE,BURN	01295	SN74S08
A1U565	156-0459-02			MICROCIRCUIT,DI:QUAD 2 INPUT & GATE,BURN	01295	SN74S08
A1U568	156-0180-04			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74S00NP3
A1U571	156-1198-01			MICROCIRCUIT,DI:SYNCHRONOUS 4 BIT CNTR	01295	SN74S163J4
A1U575	156-0739-02			MICROCIRCUIT,DI:QUAD 2 INP OR GATE,SCRN	01295	SN74S32
A1U578	156-0413-02			MICROCIRCUIT,DI:QUAD 2-INP SCHMITT TRIG	80009	156-0413-02
A1U581	156-1393-01			MICROCIRCUIT,DI:QUAD 2 INPUT NAND BFR,SCRN	01295	SN74S38
A1U585	156-1044-01			MICROCIRCUIT,DI:4 BIT SYNC BIN CNTR,SCRN	07263	F93S16DCQR
A1U588	156-1044-01			MICROCIRCUIT,DI:4 BIT SYNC BIN CNTR,SCRN	07263	F93S16DCQR
A1U591	156-1044-01			MICROCIRCUIT,DI:4 BIT SYNC BIN CNTR,SCRN	07263	F93S16DCQR
A1U595	156-1044-01			MICROCIRCUIT,DI:4 BIT SYNC BIN CNTR,SCRN	07263	F93S16DCQR
A1U711	156-1200-01			MICROCIRCUIT,LI:OPERATIONAL AMPL,QUAD	01295	TL074CN/PEP3
A1U718	156-0759-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE,SCRN	04713	MC10103PD/LD
A1U721	156-1674-00			MICROCIRCUIT,DI:SCREENED	04713	MC10H104
A1U725	156-0860-02			MICROCIRCUIT,DI:TRIPLE LINE RECEIVER,SCRN	04713	MC10116PD/LD
A1U728	156-1214-01			MICROCIRCUIT,DI:DUAL 2 WIDE,3 INPUT OR GATE	04713	SC22689
A1U731	156-1214-01			MICROCIRCUIT,DI:DUAL 2 WIDE,3 INPUT OR GATE	04713	SC22689
A1U735	156-1639-01			MICROCIRCUIT,DI:SCREENED	04713	MC10H131PD OR PL
A1U738	156-1639-01			MICROCIRCUIT,DI:SCREENED	04713	MC10H131PD OR PL

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A1U741	156-1639-01			MICROCIRCUIT,DI:SCREENED	04713	MC10H131PD OR PL
A1U745	156-1639-01			MICROCIRCUIT,DI:SCREENED	04713	MC10H131PD OR PL
A1U748	156-1639-01			MICROCIRCUIT,DI:SCREENED	04713	MC10H131PD OR PL
A1U751	156-1639-01			MICROCIRCUIT,DI:SCREENED	04713	MC10H131PD OR PL
A1U758	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A1U761	156-0982-02			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-02
A1U765	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A1U768	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A1U771	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A1U775	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A1U778	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A1U781	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A1U785	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A1U788	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A1U791	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A1U795	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A1U798	156-0331-03			MICROCIRCUIT,DI:DUAL D TYPE POS EDGE TRIG	80009	156-0331-03
A1U808	156-1200-01			MICROCIRCUIT,LI:OPERATIONAL AMPL,QUAD	01295	TL074CN/PEP3
A1U821	156-1640-01			MICROCIRCUIT,DI:SCREENED	04713	MC10H116(LD OR P
A1U825	156-1214-01			MICROCIRCUIT,DI:DUAL 2 WIDE,3 INPUT OR GATE	04713	SC22689
A1U828	156-1214-01			MICROCIRCUIT,DI:DUAL 2 WIDE,3 INPUT OR GATE	04713	SC22689
A1U831	156-1214-01			MICROCIRCUIT,DI:DUAL 2 WIDE,3 INPUT OR GATE	04713	SC22689
A1U835	156-1639-01			MICROCIRCUIT,DI:SCREENED	04713	MC10H131PD OR PL
A1U838	156-1639-01			MICROCIRCUIT,DI:SCREENED	04713	MC10H131PD OR PL
A1U841	156-1639-01			MICROCIRCUIT,DI:SCREENED	04713	MC10H131PD OR PL
A1U845	156-1639-01			MICROCIRCUIT,DI:SCREENED	04713	MC10H131PD OR PL
A1U848	156-0542-01			MICROCIRCUIT,DI:HEX INVERTER,SCRN	04713	MC10189PD/LD
A1U851	156-1639-01			MICROCIRCUIT,DI:SCREENED	04713	MC10H131PD OR PL
A1U904	156-0067-00			MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	01295	MICROA741CP
A1U918	156-1311-00			MICROCIRCUIT,LI:D/A CONVERTER	18324	NE5018N-11B
A1U921	156-0205-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN	04713	MC10102PD/LD
A1U925	156-1327-00			MICROCIRCUIT,DI:3 STATE OCTAL D FF,SCRN	27014	MM74C374
A1U928	156-1327-00			MICROCIRCUIT,DI:3 STATE OCTAL D FF,SCRN	27014	MM74C374
A1U931	156-1327-00			MICROCIRCUIT,DI:3 STATE OCTAL D FF,SCRN	27014	MM74C374
A1U935	156-1327-00			MICROCIRCUIT,DI:3 STATE OCTAL D FF,SCRN	27014	MM74C374
A1U938	156-1327-00			MICROCIRCUIT,DI:3 STATE OCTAL D FF,SCRN	27014	MM74C374
A1U941	156-1327-00			MICROCIRCUIT,DI:3 STATE OCTAL D FF,SCRN	27014	MM74C374
A1U945	156-1327-00			MICROCIRCUIT,DI:3 STATE OCTAL D FF,SCRN	27014	MM74C374
A1U948	156-1639-01			MICROCIRCUIT,DI:SCREENED	04713	MC10H131PD OR PL
A1U951	156-1639-01			MICROCIRCUIT,DI:SCREENED	04713	MC10H131PD OR PL
A1U958	156-0078-02			MICROCIRCUIT,DI:1 OF 16 DECODER DEMUX,SCRN	01295	SN74154
A1U965	156-0078-02			MICROCIRCUIT,DI:1 OF 16 DECODER DEMUX,SCRN	01295	SN74154
A1U968	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A1U971	156-0541-02			MICROCIRCUIT,DI:DUAL 2 TO 4 LINE DCDR	01295	SN74LS139NP3
A1U975	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A1U978	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A1U981	160-1997-00			MICROCIRCUIT,DI:8192 X 8 PROM	80009	160-1997-00
A1U988	160-1998-00			MICROCIRCUIT,DI:8192 X 8 PROM	80009	160-1998-00
A1U991	160-1999-00			MICROCIRCUIT,DI:8192 X 8 PROM	80009	160-1999-00
A1U998	156-1026-02			MICROCIRCUIT,DI:4/1 LINE DECODER,BURN-IN	80009	156-1026-02
A1W918	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A1W925	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A1Y498	158-0248-00			XTAL UNIT,QTZ:10MHZ, 0.01%,SERIES	80009	158-0248-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2	670-7944-00			CKT BOARD ASSY:DATA ACQUISITION MODULE	80009	670-7944-00
A2C101	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C126	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C129	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C136	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C143	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C158	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C163	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C201	283-0204-00			CAP.,FXD,CER DI:0.01UF,20%,50V	96733	R2676
A2C202	283-0204-00			CAP.,FXD,CER DI:0.01UF,20%,50V	96733	R2676
A2C222	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C232	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C262	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C302	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C318	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C319	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C361	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C371	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C378	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C388	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C395	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C401	283-0204-00			CAP.,FXD,CER DI:0.01UF,20%,50V	96733	R2676
A2C402	283-0204-00			CAP.,FXD,CER DI:0.01UF,20%,50V	96733	R2676
A2C403	283-0204-00			CAP.,FXD,CER DI:0.01UF,20%,50V	96733	R2676
A2C405	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C429	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C432	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C439	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C467	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A2C468	281-0167-00			CAP.,VAR,CER DI:9-45PF,200V	59660	538-011D9-45
A2C476	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C486	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C502	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C505	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C508	283-0204-00			CAP.,FXD,CER DI:0.01UF,20%,50V	96733	R2676
A2C524	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C541	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C544	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C549	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C558	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C566	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C573	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C586	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C588	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C591	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C595	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C622	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C668	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C681	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C702	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A2C703	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A2C704	283-0422-00			CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
A2C705	283-0422-00			CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
A2C707	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2C708	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C711	283-0422-00			CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
A2C712	283-0422-00			CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
A2C716	283-0422-00			CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
A2C718	283-0422-00			CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
A2C719	290-0891-00			CAP.,FXD,ELCTLT:1UF,+75-10%,50V	55680	ULA1H010TEA
A2C722	290-0891-00			CAP.,FXD,ELCTLT:1UF,+75-10%,50V	55680	ULA1H010TEA
A2C726	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C741	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C759	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C782	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C786	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C789	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C801	283-0204-00			CAP.,FXD,CER DI:0.01UF,20%,50V	96733	R2676
A2C802	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A2C803	283-0422-00			CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
A2C804	283-0204-00			CAP.,FXD,CER DI:0.01UF,20%,50V	96733	R2676
A2C806	283-0204-00			CAP.,FXD,CER DI:0.01UF,20%,50V	96733	R2676
A2C808	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C809	281-0816-00			CAP.,FXD,CER DI:82PF,5%,100V	96733	R3247
A2C810	283-0422-00			CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
A2C813	283-0422-00			CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
A2C823	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C865	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C868	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C871	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C878	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C889	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C901	290-0743-00			CAP.,FXD,ELCTLT:100UF,+50-10%,16V	56289	500D146
A2C902	283-0164-00			CAP.,FXD,CER DI:2.2UF,20%,25V	04222	SR402E225MAA
A2C903	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C904	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C906	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A2C910	283-0422-00			CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
A2C925	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C942	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C965	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2CR708	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2CR709	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2CR710	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2CR711	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2CR715	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2CR716	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2CR717	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2CR718	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2CR808	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2CR809	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2CR812	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2CR813	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2CR908	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2CR909	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2DL115	119-1664-00			DELAY LINE,ELEC-22NS,200 OHM	01961	PE22612
A2DL315	119-1664-00			DELAY LINE,ELEC-22NS,200 OHM	01961	PE22612
A2DL415	119-1664-00			DELAY LINE,ELEC-22NS,200 OHM	01961	PE22612

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2Q101	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q102	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q103	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q104	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q105	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q106	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q107	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q108	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q109	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q110	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q111	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q112	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q113	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q114	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q115	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q116	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q301	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q302	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q303	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q304	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q305	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q306	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q307	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q308	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q309	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q310	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q311	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q312	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q313	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q314	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q315	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q316	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q318	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236
A2Q319	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236
A2Q465	151-0447-00			TRANSISTOR:SILICON,NPN	04713	SRF502-1
A2Q501	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q502	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q503	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q504	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q505	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q506	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q507	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q508	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q509	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q510	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q511	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q512	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q513	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q514	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q515	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q516	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q519	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236
A2Q520	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236
A2Q539	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2Q540	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236
A2Q543	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236
A2Q544	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236
A2Q628	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236
A2Q629	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236
A2Q901	151-0429-00			TRANSISTOR:SILICON,PNP	04713	SJE957
A2Q902	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A2Q951	151-0301-00			TRANSISTOR:SILICON,PNP	27014	2N2907A
A2R101	307-0695-00			RES NTWK,FXD FI:9,150 OHM,2%,0.2W EACH	01121	110A151
A2R102	307-0695-00			RES NTWK,FXD FI:9,150 OHM,2%,0.2W EACH	01121	110A151
A2R103	311-1245-00			RES.,VAR,NONWIR:10K OHM,10%,0.50W	73138	72-28-0
A2R104	321-0763-07			RES.,FXD,FILM:1.12K OHM,0.1%,0.125W	91637	MFF1816C11200B
A2R106	307-0486-00			RES,NTWK,THK FI:100 OHM,20%,1.125W	91637	MSP10A01-101J
A2R107	307-0736-00			RES,NTWK,THK FI:10,390 OHM,2%,0.19W	91637	CSP11G01391G
A2R108	307-0832-00			RES NTWK,FXD,FI:9,120 OHM,2%,0.15W	01121	210A121
A2R110	311-1236-00			RES.,VAR,NONWIR:250 OHM,10%,0.50W	73138	72-22-0
A2R114	307-0674-00			RES NTWK,THK,FI:9,430 OHM,2%,1.25W	01121	210A431
A2R115	307-0592-00			RES,NTWK,FXD FI:9,220 OHM,2%,2W	91637	MSP10A01-221G
A2R149	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A2R162	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A2R186	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A2R187	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A2R273	307-0546-00			RES NTWK,FXD FI:5,75 OHM,5%,0.15W	91637	MSP06A01750J
A2R278	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A2R281	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A2R306	307-0486-00			RES,NTWK,THK FI:100 OHM,20%,1.125W	91637	MSP10A01-101J
A2R307	307-0736-00			RES,NTWK,THK FI:10,390 OHM,2%,0.19W	91637	CSP11G01391G
A2R308	307-0832-00			RES NTWK,FXD,FI:9,120 OHM,2%,0.15W	01121	210A121
A2R314	307-0674-00			RES NTWK,THK,FI:9,430 OHM,2%,1.25W	01121	210A431
A2R315	307-0592-00			RES,NTWK,FXD FI:9,220 OHM,2%,2W	91637	MSP10A01-221G
A2R401	307-0695-00			RES NTWK,FXD FI:9,150 OHM,2%,0.2W EACH	01121	110A151
A2R414	307-0674-00			RES NTWK,THK,FI:9,430 OHM,2%,1.25W	01121	210A431
A2R415	307-0592-00			RES,NTWK,FXD FI:9,220 OHM,2%,2W	91637	MSP10A01-221G
A2R419	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A2R459	307-0540-00			RES,NTWK,FXD,FI:(5) 1K OHM,10%,0.7W	57924	4306R-101-102
A2R467	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A2R468	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A2R491	307-0541-00			RES,NTWK,THK FI:(7)1K OHM,10%,1W	91637	MSP08A01-102G
A2R502	307-0695-00			RES NTWK,FXD FI:9,150 OHM,2%,0.2W EACH	01121	110A151
A2R506	307-0486-00			RES,NTWK,THK FI:100 OHM,20%,1.125W	91637	MSP10A01-101J
A2R507	307-0736-00			RES,NTWK,THK FI:10,390 OHM,2%,0.19W	91637	CSP11G01391G
A2R508	307-0832-00			RES NTWK,FXD,FI:9,120 OHM,2%,0.15W	01121	210A121
A2R526	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A2R529	307-0488-00			RES,NTWK,FXD,FI:100 OHM,20%,0.75W	01121	106A101
A2R536	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2R539	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A2R540	315-0111-00			RES.,FXD,CMPSN:110 OHM,5%,0.25W	01121	CB1115
A2R541	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A2R544	315-0111-00			RES.,FXD,CMPSN:110 OHM,5%,0.25W	01121	CB1115
A2R545	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A2R546	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2R585	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2R624	307-0546-00			RES NTWK,FXD FI:5,75 OHM,5%,0.15W	91637	MSP06A01750J
A2R631	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2R658	307-0675-00			RES NTWK,FXD FI:9,1K OHM,2%,1.25W	01121	210A102
A2R701	307-0695-00			RES NTWK,FXD FI:9,150 OHM,2%,0.2W EACH	01121	110A151
A2R702	307-0695-00			RES NTWK,FXD FI:9,150 OHM,2%,0.2W EACH	01121	110A151
A2R703	315-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	01121	CB3925
A2R704	315-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	01121	CB3925
A2R706	321-0414-04			RES.,FXD,FILM:200K OHM,0.1%,0.125W	91637	MFF1816D20002B
A2R707	321-0414-04			RES.,FXD,FILM:200K OHM,0.1%,0.125W	91637	MFF1816D20002B
A2R708	321-0318-07			RES.,FXD,FILM:20K OHM,0.1%,0.125W	24546	NE55E2002B
A2R709	321-0318-07			RES.,FXD,FILM:20K OHM,0.1%,0.125W	24546	NE55E2002B
A2R710	321-0318-07			RES.,FXD,FILM:20K OHM,0.1%,0.125W	24546	NE55E2002B
A2R711	321-0318-07			RES.,FXD,FILM:20K OHM,0.1%,0.125W	24546	NE55E2002B
A2R715	321-0289-02			RES.,FXD,FILM:10K OHM,0.5%,0.125W	91637	CMF55-116D10001D
A2R716	321-0289-02			RES.,FXD,FILM:10K OHM,0.5%,0.125W	91637	CMF55-116D10001D
A2R717	321-0924-07			RES.,FXD,FILM:40K OHM,0.1%,0.125W	91637	MFF1816C40001B
A2R718	321-0924-07			RES.,FXD,FILM:40K OHM,0.1%,0.125W	91637	MFF1816C40001B
A2R720	321-0289-02			RES.,FXD,FILM:10K OHM,0.5%,0.125W	91637	CMF55-116D10001D
A2R721	321-0289-02			RES.,FXD,FILM:10K OHM,0.5%,0.125W	91637	CMF55-116D10001D
A2R749	307-0546-00			RES NTWK,FXD FI:5,75 OHM,5%,0.15W	91637	MSP06A01750J
A2R753	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A2R754	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2R772	307-0446-00			RES,NTWK,FXD FI:10K OHM,20%,(9) RES	91637	MSP10A01-103M
A2R793	307-0675-00			RES NTWK,FXD FI:9,1K OHM,2%,1.25W	01121	210A102
A2R798	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2R799	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A2R803	321-0414-04			RES.,FXD,FILM:200K OHM,0.1%,0.125W	91637	MFF1816D20002B
A2R804	315-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	01121	CB3925
A2R808	321-0318-07			RES.,FXD,FILM:20K OHM,0.1%,0.125W	24546	NE55E2002B
A2R810	321-0318-07			RES.,FXD,FILM:20K OHM,0.1%,0.125W	24546	NE55E2002B
A2R811	321-0289-02			RES.,FXD,FILM:10K OHM,0.5%,0.125W	91637	CMF55-116D10001D
A2R812	321-0924-07			RES.,FXD,FILM:40K OHM,0.1%,0.125W	91637	MFF1816C40001B
A2R813	321-0318-07			RES.,FXD,FILM:20K OHM,0.1%,0.125W	24546	NE55E2002B
A2R823	321-0261-00			RES.,FXD,FILM:5.11K OHM,1%,0.125W	91637	MFF1816G51100F
A2R901	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A2R902	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A2R904	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A2R905	321-0222-07			RES.,FXD,FILM:2K OHM,0.1%,0.125W	91637	MFF1816C20000B
A2R906	321-0239-00			RES.,FXD,FILM:3.01K OHM,1%,0.125W	91637	MFF1816G30100F
A2R907	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A2R908	321-0318-07			RES.,FXD,FILM:20K OHM,0.1%,0.125W	24546	NE55E2002B
A2R910	321-0289-02			RES.,FXD,FILM:10K OHM,0.5%,0.125W	91637	CMF55-116D10001D
A2R911	321-0289-02			RES.,FXD,FILM:10K OHM,0.5%,0.125W	91637	CMF55-116D10001D
A2R912	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A2R913	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A2R914	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A2R918	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9) RES	91637	MSP10A01-472M
A2R921	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A2R951	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A2R952	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A2R953	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A2R959	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A2R960	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9) RES	91637	MSP10A01-472M
A2R962	315-0432-00			RES.,FXD,CMPSN:4.3K OHM,5%,0.25W	01121	CB4325
A2R969	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A2R970	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015

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A2U118	156-1704-00			MICROCIRCUIT,DI:OCTAL D-TYPE FF,W/3-ST OUT	07263	74F374(PCQR OR D
A2U121	156-1704-00			MICROCIRCUIT,DI:OCTAL D-TYPE FF,W/3-ST OUT	07263	74F374(PCQR OR D
A2U125	156-0982-02			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-02
A2U128	156-1704-00			MICROCIRCUIT,DI:OCTAL D-TYPE FF,W/3-ST OUT	07263	74F374(PCQR OR D
A2U131	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U135	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U138	156-1198-01			MICROCIRCUIT,DI:SYNCHRONOUS 4 BIT CNTR	01295	SN74S163J4
A2U141	156-1695-00			MICROCIRCUIT,DI:SRAM,1024 X 4	34649	D2149H-2/S7570
A2U145	156-1695-00			MICROCIRCUIT,DI:SRAM,1024 X 4	34649	D2149H-2/S7570
A2U148	156-1690-00			MICROCIRCUIT,DI:SCAM,4096 X 1	34649	D2147H-2/S7578
A2U151	156-1360-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1360-01
A2U168	156-1680-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT & GATE	01295	SN74S15
A2U198	156-0739-02			MICROCIRCUIT,DI:QUAD 2 INP OR GATE,SCRN	01295	SN74S32
A2U218	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A2U221	156-1704-00			MICROCIRCUIT,DI:OCTAL D-TYPE FF,W/3-ST OUT	07263	74F374(PCQR OR D
A2U225	156-0982-02			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-02
A2U228	156-1704-00			MICROCIRCUIT,DI:OCTAL D-TYPE FF,W/3-ST OUT	07263	74F374(PCQR OR D
A2U231	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U235	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U238	156-1198-01			MICROCIRCUIT,DI:SYNCHRONOUS 4 BIT CNTR	01295	SN74S163J4
A2U241	156-1695-00			MICROCIRCUIT,DI:SRAM,1024 X 4	34649	D2149H-2/S7570
A2U245	156-1695-00			MICROCIRCUIT,DI:SRAM,1024 X 4	34649	D2149H-2/S7570
A2U248	156-1690-00			MICROCIRCUIT,DI:SCAM,4096 X 1	34649	D2147H-2/S7578
A2U261	156-1680-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT & GATE	01295	SN74S15
A2U265	156-0459-02			MICROCIRCUIT,DI:QUAD 2 INPUT & GATE,BURN	01295	SN74S08
A2U268	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A2U275	156-1640-01			MICROCIRCUIT,DI:SCREENED	04713	MC10H116(LD OR P
A2U281	156-0703-02			MICROCIRCUIT,DI:4-2-3-2 INPUT & OR GATE	07263	74S64
A2U285	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A2U288	156-0703-02			MICROCIRCUIT,DI:4-2-3-2 INPUT & OR GATE	07263	74S64
A2U291	156-1800-00			MICROCIRCUIT,DI:QUAD 2 INPUT EXCLUSIVE OR	07263	74F86(PCQR OR DC
A2U351	156-1360-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1360-01
A2U421	156-1704-00			MICROCIRCUIT,DI:OCTAL D-TYPE FF,W/3-ST OUT	07263	74F374(PCQR OR D
A2U425	156-0982-02			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-02
A2U428	156-1704-00			MICROCIRCUIT,DI:OCTAL D-TYPE FF,W/3-ST OUT	07263	74F374(PCQR OR D
A2U431	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U438	156-1198-01			MICROCIRCUIT,DI:SYNCHRONOUS 4 BIT CNTR	01295	SN74S163J4
A2U441	156-1695-00			MICROCIRCUIT,DI:SRAM,1024 X 4	34649	D2149H-2/S7570
A2U445	156-1695-00			MICROCIRCUIT,DI:SRAM,1024 X 4	34649	D2149H-2/S7570
A2U448	156-1690-00			MICROCIRCUIT,DI:SCAM,4096 X 1	34649	D2147H-2/S7578
A2U461	156-0331-03			MICROCIRCUIT,DI:DUAL D TYPE POS EDGE TRIG	80009	156-0331-03
A2U468	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A2U475	156-0459-02			MICROCIRCUIT,DI:QUAD 2 INPUT & GATE,BURN	01295	SN74S08
A2U478	156-0331-03			MICROCIRCUIT,DI:DUAL D TYPE POS EDGE TRIG	80009	156-0331-03
A2U485	156-0690-03			MICROCIRCUIT,DI:QUAD 2 INP NOR GATE,BURN IN	01295	SN74S02
A2U551	156-1360-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1360-01
A2U555	156-1189-00			MICROCIRCUIT,DI:16 X 4 RAM	34335	AM74S189J
A2U558	156-0304-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	01295	SN74S20
A2U561	156-0459-02			MICROCIRCUIT,DI:QUAD 2 INPUT & GATE,BURN	01295	SN74S08
A2U565	156-0459-02			MICROCIRCUIT,DI:QUAD 2 INPUT & GATE,BURN	01295	SN74S08
A2U568	156-0180-04			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74S00NP3
A2U571	156-1198-01			MICROCIRCUIT,DI:SYNCHRONOUS 4 BIT CNTR	01295	SN74S163J4
A2U575	156-0739-02			MICROCIRCUIT,DI:QUAD 2 INP OR GATE,SCRN	01295	SN74S32
A2U578	156-0413-02			MICROCIRCUIT,DI:QUAD 2-INP SCHMITT TRIG	80009	156-0413-02

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A2U711	156-1200-01			MICROCIRCUIT,LI:OPERATIONAL AMPL,QUAD	01295	TL074CN/PEP3
A2U718	156-0759-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE,SCRN	04713	MC10103PD/LD
A2U721	156-1674-00			MICROCIRCUIT,DI:SCREENED	04713	MC10H104
A2U758	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A2U761	156-0982-02			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-02
A2U765	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A2U768	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U771	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U775	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U778	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U785	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U791	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U808	156-1200-01			MICROCIRCUIT,LI:OPERATIONAL AMPL,QUAD	01295	TL074CN/PEP3
A2U904	156-0067-00			MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	01295	MICROA741CP
A2U918	156-1311-00			MICROCIRCUIT,LI:D/A CONVERTER	18324	NE5018N-11B
A2U925	156-1327-00			MICROCIRCUIT,DI:3 STATE OCTAL D FF,SCRN	27014	MM74C374
A2U938	156-1327-00			MICROCIRCUIT,DI:3 STATE OCTAL D FF,SCRN	27014	MM74C374
A2U941	156-1327-00			MICROCIRCUIT,DI:3 STATE OCTAL D FF,SCRN	27014	MM74C374
A2U945	156-1327-00			MICROCIRCUIT,DI:3 STATE OCTAL D FF,SCRN	27014	MM74C374
A2U958	156-0078-02			MICROCIRCUIT,DI:1 OF 16 DECODER DEMUX,SCRN	01295	SN74154
A2U965	156-0078-02			MICROCIRCUIT,DI:1 OF 16 DECODER DEMUX,SCRN	01295	SN74154
A2U975	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U978	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U998	156-1026-02			MICROCIRCUIT,DI:4/1 LINE DECODER,BURN-IN	80009	156-1026-02

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).

Resistors = Ohms (Ω).

──── **The information and special symbols below may appear in this manual.** ────

Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.

COLORS ON SCHEMATICS

Introduction

Some of the schematics in this section are color-coded. This coding indicates the flow of the self-diagnostic tests contained in the DAS. Each separate color stands for an individual diagnostic function. The correlation between colors and functions is indicated in the legend at the lower left corner of each color schematic.

PARTS OF THE COLOR SCHEMATICS

There are three parts to each color schematic in this manual:

- **Color.** The color follows the lines of the schematics that are first used by a diagnostic function.

- **Legend.** The legend makes the correlation between colors and specific diagnostic functions.

- **Function Tags.** The function tag at the beginning and end of each colored line indicates all functions that are present on the line.

The colors on the schematics indicate the presence of a diagnostic self-test at the point the color is present. The specific color at any point on the schematic indicates only the first diagnostic function that is run at that point on the board. (This has been done to avoid possible confusion arising from trying to show multiple colors on a single line.)

Note, however, that if the diagnostic test functions are run in the recommended sequence, then any circuitry that was tested by a previous test is not shown in the color of the most recent test. Only the new circuitry that is tested by a diagnostic function is indicated in the colors of the schematics.

NOTE

Any color will always stand for the same test on all schematics for one board. That same color may be used on schematics for another board and signify an entirely different diagnostic test function. Colors are consistent on any one board, but do not try to relate colors on one board to colors on another board -- there is no correlation.

To indicate which colors correspond to each diagnostic test, there is a legend near the lower left corner of the schematic. Refer to this legend whenever the DAS self-diagnostics are used to troubleshoot a board. On any schematic or set of schematics for a board, one color always stands for the same diagnostic function.

At the point where a colored line enters or leaves a schematic, there is a note that refers to the functions on that line. Use these function tags when tracing the sources of diagnostic tests through the schematics or when looking for circuitry common to more than one test. All diagnostic functions that enter or leave the page at that point are indicated by the function tag.

USING THE COLOR IN TROUBLESHOOTING

The color on the schematics is designed exclusively as a troubleshooting aid. Three examples follow that show how the colors can be used to find circuit faults.

One Diagnostic Function Failure

Start the troubleshooting procedure by running all the DAS diagnostic functions on the board to be repaired. Suppose only one of the tests failed. Note the function that failed, and flip to the schematics for that board. Refer to the legend on the schematic page to see which color corresponds to the function that failed. Any point on the schematic that shows the color corresponding the the diagnostic function is the probable location of the failure.

Multiple Diagnostic Function Failures

Start the troubleshooting procedure by running all the DAS diagnostic functions on the board to be repaired. Suppose more than one of the tests failed. Note the functions that failed as well as the numbers of the functions. Flip to the schematics for the board to be repaired. Refer to the legend on the schematic page to find out which color corresponds to the diagnostic function with the lowest number.

Since more than one diagnostic function failed, the failure must be in circuitry that is common to all of the failed tests. This means the failure is on the color that corresponds to the lowest function number. Find the areas on the schematics that show that color. Now refer to the function tags at the beginnings and ends of lines of this color. Use the function tags to define an area in the failed color that contains all of the failed diagnostic functions. This area will probably be much smaller than the area covered by the selected color.

No Diagnostic Function Failures

When troubleshooting failures not detected by the diagnostics, first define the type of failure and the possible causes. Next, examine the white (uncolored) areas of the schematics that might contain this type of circuit fault. (You need only examine the white areas since all colored areas are covered by the diagnostics.)

Table 11-1
IC PIN INFORMATION

Device Type	V_{CC} or V_{DD}	GND
10102	1,16	8
10103	1,16	8
10H104	1,16	8
10H109	1,16	8
10116	1,16	8
10118	1,16	8
10H131	1,16	8
10189	1,16	8
2147H-2	18	9
2149H-2	18	9
5018	19	17
741	7	4
74S00(LS)	14	7
74S02	14	7
74S04	14	7
74S05	14	7
74S08	14	7
74S15	14	7
74S20	14	7
74S32(LS)	14	7
74S38	14	7
74S64	14	7
74S74(LS)	14	7
74S86	14	7
74S132	14	7
74S133	16	8
74LS139	16	8
74S153	16	8
74154(LS)	24	12
74S161	16	8
74S163	16	8
74S189	16	8
74S197	14	7
74LS244	20	10
74LS273	20	10
74LS374	20	10
74C374(F)	20	10
TL074	4	11

@
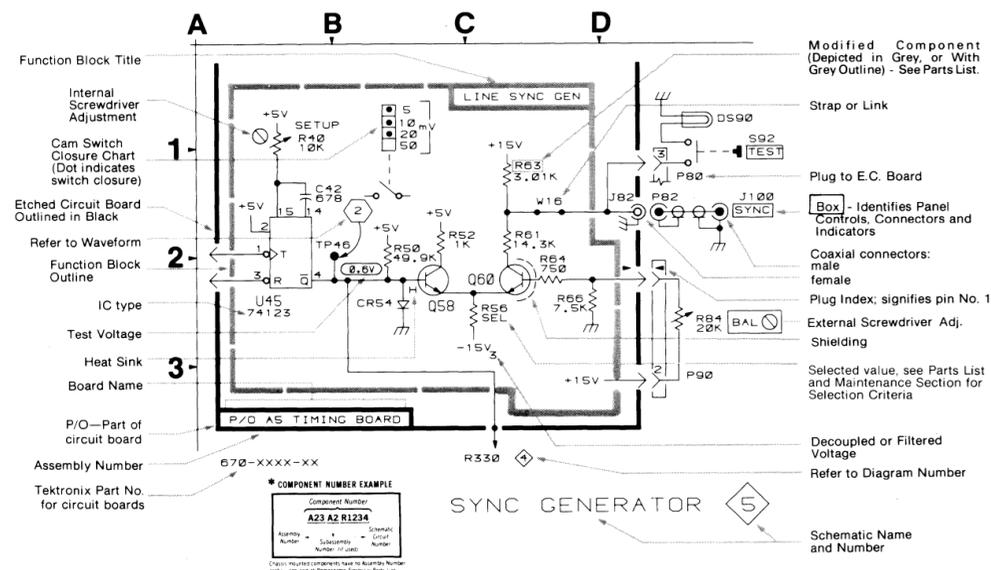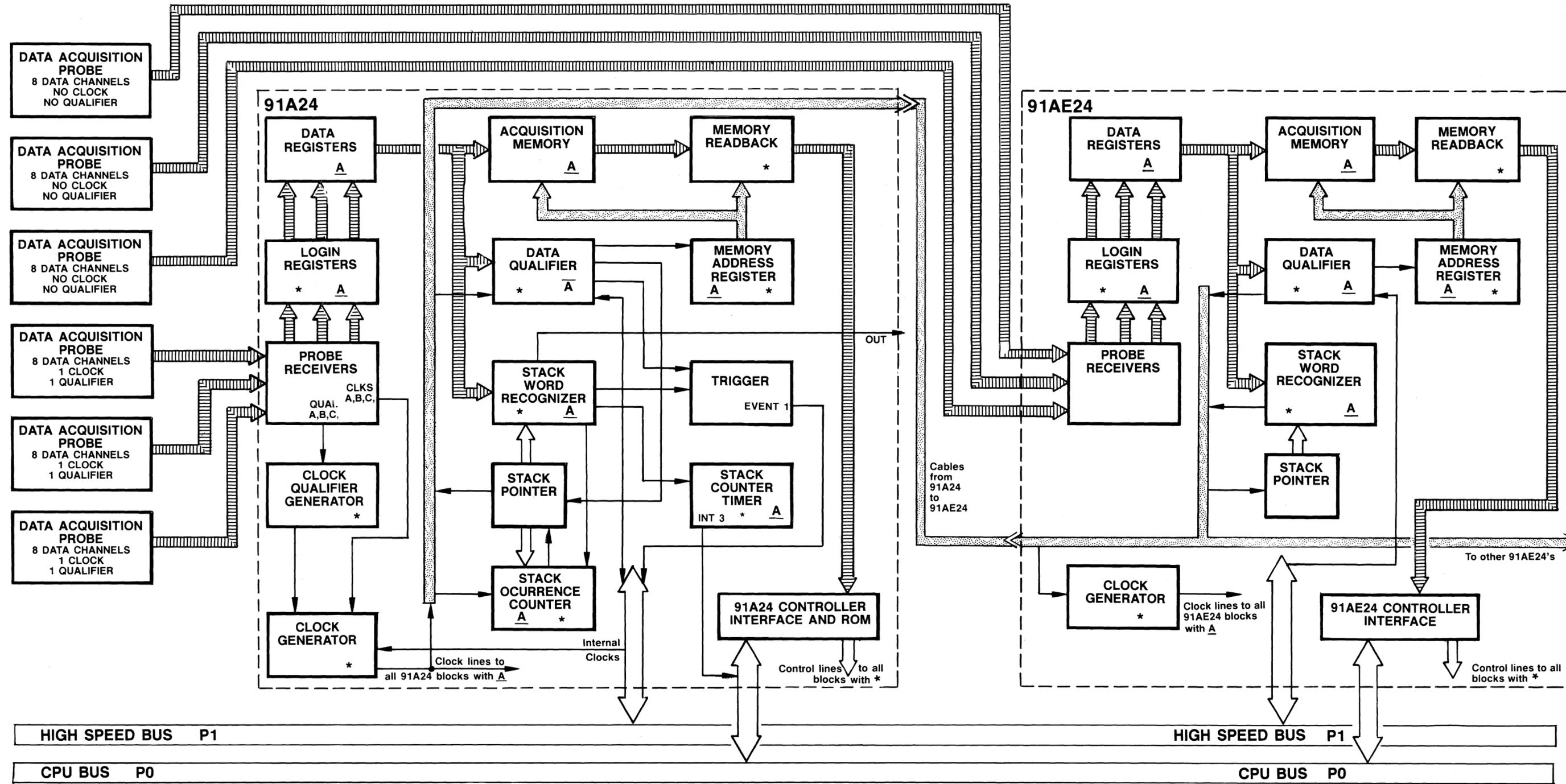
91A24 & 91AE24 BLOCK DIAGRAM

A35 91A24 DATA ACQUISITION
MODULE COMPONENT LOCATIONS
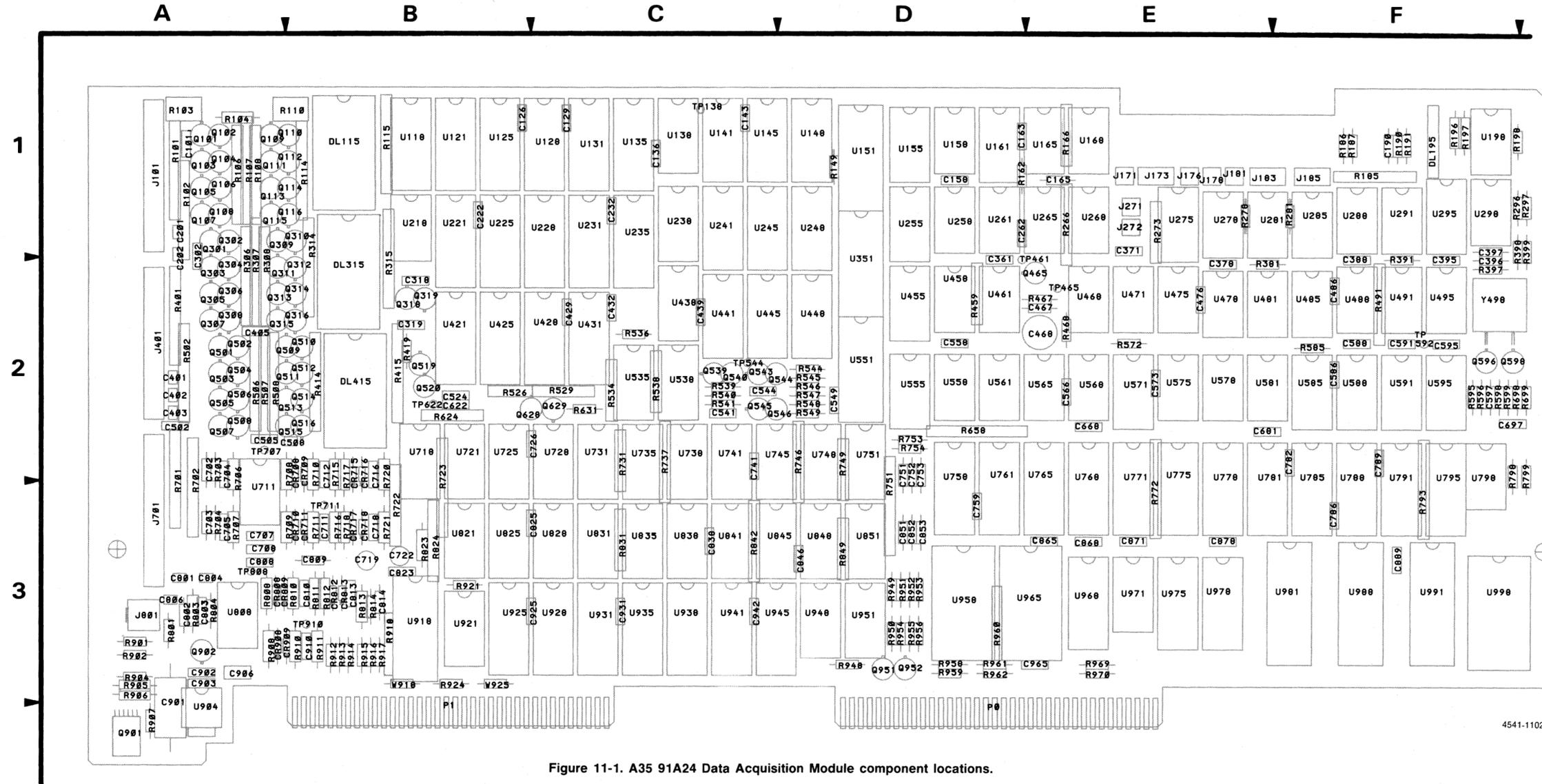
Figure 11-1. A35 91A24 Data Acquisition Module component locations.

4541-1102

DATA ACQUISITION MODULE
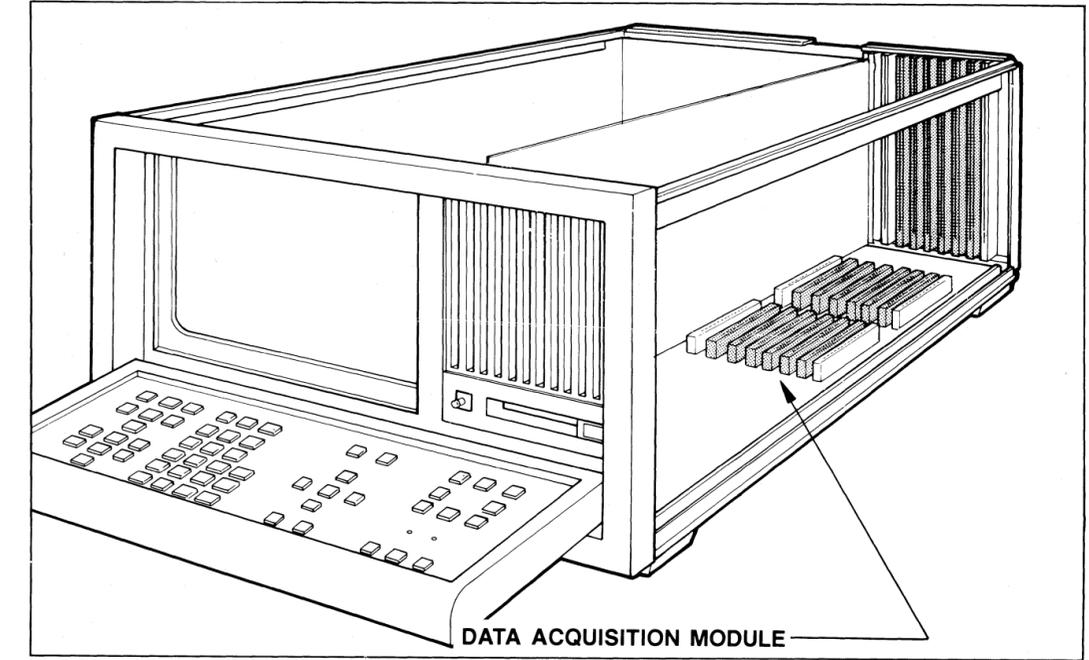
CONFIGURATION GUIDELINES

Module	Max. per Mainframe	Recommended Bus Slot(s)	Functional in Bus Slot(s)	Comments
Controller	1	0	0	Required
Trigger/Time Base	1	7	7	Required
91A08	4	6 (5, 4, 3)	6 (5, 4, 3)	Required: first 91A08 in slot 6, additional 91A08s in descending slots (5, 4, 3).
91A32	3	2-6	1-6	
91P16	1	1	1-6	
91P32	2	2-6	1-6	Will not function without a 91P16 installed.
91A04/A	1	1-6	1-6	
91AE04/A	3	1-6	1-6	Will not function without a 91A04/A installed. All expander modules must be on the same side of the 91A04/A module.
91A24	1	1-6	1-6	
91AE24	3	1-6	1-6	Will not function without a 91A24 installed. All expander modules must be on the same side of the 91A24 module.

4541-1103

Figure 11-2. 91A24 (A35) and 91AE24 (A36) module location.

Static Sensitive Devices
See Maintenance Section

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C101	B5	A1	C846	B5	D3
C126	B5	B1	C865	B5	E3
C129	B5	C1	C868	B5	E3
C136	B5	C1	C871	A3	E3
C143	B5	C1	C878	B5	F3
C158	B5	D1	C889	B5	E3
C163	B5	D1	C965	A3	E3
C222	B5	B1	P0	A1	D3
C232	B5	C1	P1	A5	B3
C262	B5	D1	R658A	E5	D2
C302	B5	A2	R658B	A5	D2
C318	B5	B2	R658H	E3	D2
C361	B5	D2	R772A	D2	E3
C371	A3	E1	R960A	E2	D3
C378	B5	E2	R960B	E2	D3
C388	B5	F2	R960C	E2	D3
C395	A3	F2	R960D	E2	D3
C405	A3	A2	R960E	E2	D3
C429	B5	C2	R960F	E2	D3
C432	B5	C2	R960G	F1	D3
C439	B5	C2	R969	A2	E2
C476	B5	E2	TP461	A4	A4
C486	B5	F2	TP544	A4	C2
C502	B5	A2	TP592	A4	F2
C505	B5	B2	TP622	A4	B2
C524	B5	B2	U285A	B3	F1
C558	B5	E2	U285B	B3	F1
C566	B5	E2	U285D	C3	F1
C573	B5	E2	U558B	D2	D2
C586	B5	F2	U561	D4	D2
C588	B5	F2	U565	D5	E2
C591	B5	F2	U758	E3	D3
C666	B5	E2	U761	E4	D3
C681	B5	E2	U765	E5	D3
C707	A3	A3	U768	D3	E3
C708	A3	A3	U781	C2	E3
C726	A3	A3	U958	E2	E3
C741	B5	C2	U965	D2	E3
C759	B5	D3	U968	A5	E3
C782	B5	F2	U971	B4	E3
C786	B5	F3	U975	B2	E3
C789	B5	F3	U978	B2	E3
C808	A3	A3	U981	C4	E3
C825	B5	C3	U988	C4	F3
C838	B5	C3	U991	C4	F3

The colors on this page correspond to the following 91A24 diagnostic functions:

0	CNTR TIMR
1	MEM ADDR
2	ACQ MEM
3	STK PNTR
4	WRD REC
5	OCCR CNTR
6	DAC THRSH
7	PRB CLK EX

The function numbers at the beginning and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information refer to the introduction of this Diagrams section.

P/O A35 91A24 DATA ACQ. CONTROLLER INTERFACE

COMPONENT NUMBER EXAMPLE

Component Number

A23 A2 R1234

Assembly Number — Subassembly Number (if used) — Schematic Circuit Number

Chassis mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

NOTE: Table 11-1 shows IC Pinout. (VCC & Gnd).

P/O CONTROLLER INTERFACE   P/O A35 91A24 DATA ACQUISITION BD.

Table 11-3
91A24 CONTROLLER INTERFACE READBACK CIRCUITRY

91A24 DATA ACQUISITION BOARD, ASSEMBLY A35

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
J101	A3	A1	U131	D5	C1
J101	F3	A1	U135	C5	C1
J401	F1	A2	U231	E5	C1
J401	A3	A2	U235	B5	C1
J701	F1	A3	U268	C3	E1
J701	A4	A3	U431	F5	C2
P0	F3	D3	U771	B3	E3
R772C	B4	E3	U775	C3	E3
R772E	B3	E3	U778	C3	E3
R772G	B3	E3	U785	D3	E3
R798G	E3	F2	U791	E3	F3
R799	E3	F2	U998	A1	F3

The colors on this page correspond to the following 91A24 diagnostic functions:

0 CNTR TIMR
1 MEM ADDR
2 ACQ MEM
3 STK PNTR
4 WRD REC
5 OCCR CNTR
6 DAC THRSH
7 PRB CLK EX

The function numbers at the beginning and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information refer to the introduction of this Diagrams section.

COMPONENT NUMBER EXAMPLE

Component Number

A23 A2 R1234

Assembly Number — Subassembly Number (if used) — Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

P/O CONTROLLER INTERFACE

P/O A35 91A24 DATA ACQUISITION BD.

MEMORY READBACK

Static Sensitive Devices
See Maintenance Section

NOTE: Table 11-1 shows IC Pinout. (VCC & Gnd).
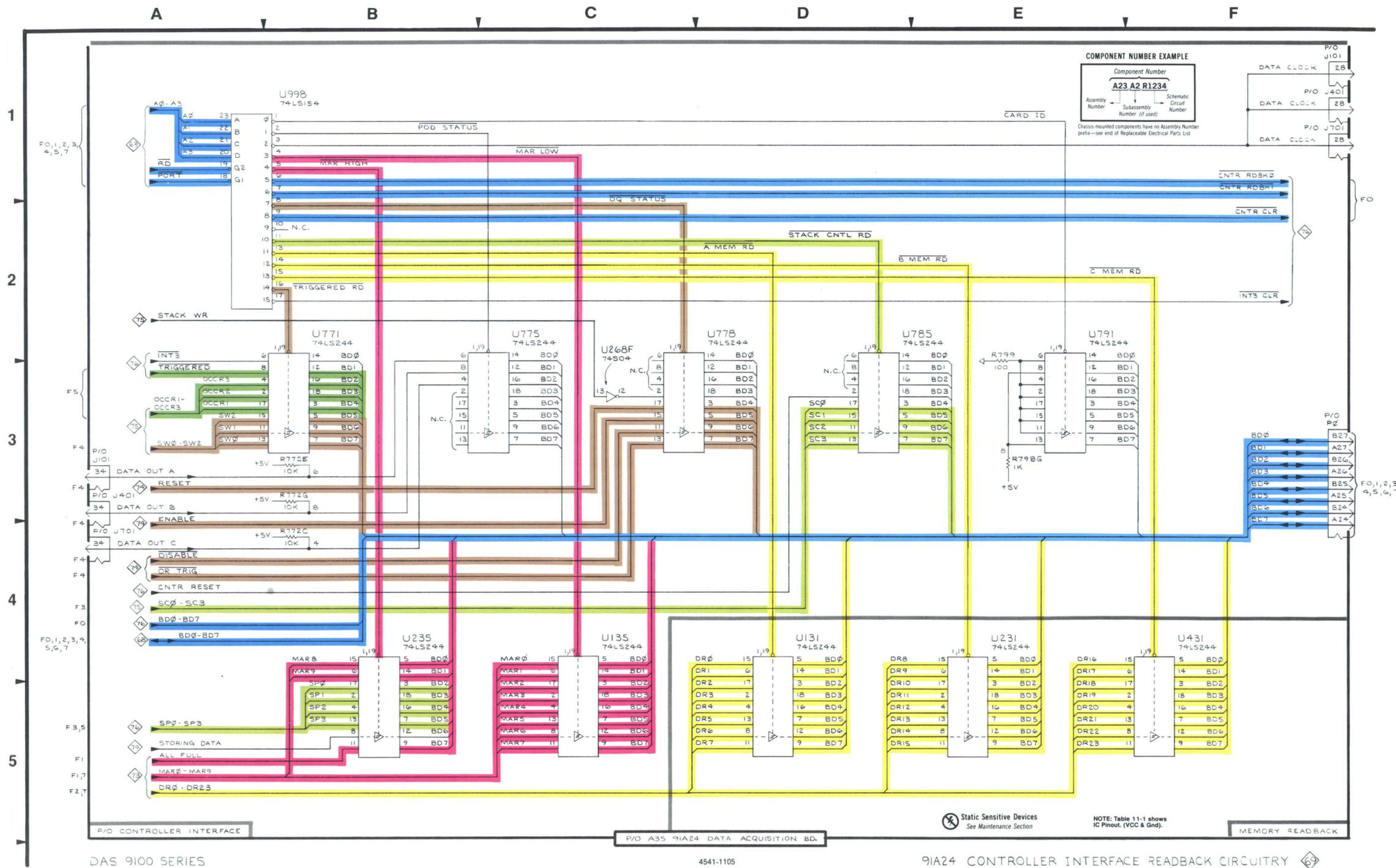
Table 11-4
91A24 PROBE A AND B RECEIVERS ⬦70
91A24 DATA ACQUISITION BOARD, ASSEMBLY A35

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
DL115	C5	B1	R106C	A4	A1	R308C	D4	A2
DL315	F5	B2	R106D	A4	A1	R308G	D3	A2
J101	D1	A2	R106F	A3	A1	R308H	D2	A2
J401	A1	A2	R106G	A3	A1	R308I	D2	A2
Q101	B5	A1	R106H	A2	A1	R314B	F5	B2
Q102	B5	A1	R106I	A2	A1	R314C	F5	B2
Q103	B4	A1	R107B	B5	A1	R314C	F4	B2
Q104	B4	A1	R107C	B4	A1	R314D	F4	B2
Q105	B3	A1	R107D	B4	A1	R314E	F3	B2
Q106	B3	A1	R107E	B3	A1	R314E	F3	B2
Q107	B2	A1	R107F	B2	A1	R314H	F2	B2
Q108	B2	A1	R107G	B3	A1	R314I	F2	B2
Q109	B4	B1	R107I	B1	A1	R315A	F5	B2
Q110	B4	B1	R107J	B2	A1	R315B	F5	B2
Q111	B3	A1	R108A	A5	A1	R315C	F4	B2
Q112	B3	B1	R108B	A4	A1	R315D	F4	B2
Q113	B2	A1	R108C	A4	A1	R315E	F3	B2
Q114	B2	A1	R108D	A3	A1	R315H	F2	B2
Q115	B1	A1	R108F	A3	A1	R315I	F2	B2
Q116	B1	A1	R108G	A2	A1	R315I	F2	B2
Q301	E5	A1	R108I	A1	A1	R401A	E5	A2
Q302	E5	A1	R114A	B5	B1	R401C	D5	A2
Q303	E4	A2	R114B	B5	B1	R401D	E5	A2
Q304	E4	A2	R114C	B4	B1	R401D	E5	A2
Q305	E3	A2	R114E	B3	B1	R401F	D4	A2
Q306	E3	A2	R114G	B3	B1	R401G	D4	A2
Q307	E2	A2	R114H	B2	B1	R401I	D4	A2
Q308	E2	B1	R114H	B2	B1	R401	D2	A2
Q309	E5	B1	R114I	B1	B1	R502B	D1	A2
Q310	E5	B1	R115A	C5	B1	R502B	D3	A2
Q311	E4	B2	R115B	C4	B1	R502C	D3	A2
Q312	E4	B2	R115C	C4	B1	R502D	D3	A2
Q313	E3	B2	R115D	C3	B1	R502E	E3	A2
Q314	E3	B2	R115E	C3	B1	R502F	E3	A2
Q315	E2	B2	R115F	C2	B1	R502G	D2	A2
Q316	E2	B2	R115G	C2	B1	R502H	D2	A2
R101A	A5	A1	R115I	C1	B1	R502I	D1	A2
R101B	A5	A1	R306A	E5	A2	R722A	A1	B3
R101C	A4	A1	R306B	E4	A2	R722C	A1	B3
R101D	B5	A1	R306C	E4	A2	R722D	B1	B3
R101E	A4	A1	R306D	E4	A2	R722E	E1	B3
R101F	B4	A1	R306F	E3	A2	R723A	A1	B3
R101G	B3	A1	R306G	E3	A2	R723B	B1	B2
R101H	A3	A1	R306H	E2	A2	R723I	E1	B2
R101I	A1	A1	R306I	E2	A2	R824A	B1	B2
R102A	A3	A1	R307B	E5	A2	R824C	A1	B2
R102B	B4	A1	R307C	E5	A2	R824F	E1	B3
R102C	B3	A1	R307D	E4	A2	R824G	E1	B3
R102D	B3	A1	R307F	E3	A2	U725C	D1	B2
R102E	A2	A1	R307G	E4	A2	U725C	D1	B2
R102F	B2	A1	R307H	E3	A2	U821A	B1	B3
R102G	A2	A1	R307I	E2	A2	U821B	E1	B3
R102H	A1	A1	R307J	E2	A2			
R102I	A1	A1	R824A	B1	B2			
R106A	A5	A1	R308A	D5	A2			
R106B	A5	A1	R308B	D5	A2			

The colors on this page correspond to the following 91A24 diagnostic functions:

0 CNTR TIMR
1 MEM ADDR
2 ACQ MEM
3 STK PNTR
4 WRD REC
5 OCCR CNTR
6 DAC THRSH
7 PRB CLK EX

The function numbers at the beginning and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information refer to the introduction of this Diagrams section.

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number — Subassembly Number (if used) — Schematic Circuit Number

Chassis mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

PROBE A RECEIVER (INPUT FROM POD A CONNECTOR)

P/O A35 91A24 DATA ACQUISITION BD.

Ⓧ Static Sensitive Devices
See Maintenance Section

NOTE: Table 11-1 shows IC Pinout. (VCC & Gnd).

PROBE B RECEIVER (INPUT FROM POD B CONNECTOR)

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C201	F2	A1	Q516	B1	B2	R702H	A1	A3
C202	F2	A2	R103	D4	A2	R702I	B2	A2
C401	F4	A2	R104	D4	A2	R703	F2	A2
C402	F4	A2	R110	D4	B5	R704	B2	A3
C403	F3	A2	R414A	B5	B1	R706	F2	A3
C508	F2	B2	R414C	B4	B2	R707	F3	A3
C702	F3	A2	R414E	B3	B2	R708	E3	A3
C703	F3	A3	R414F	B3	B2	R709	E3	B2
C704	F2	A3	R414G	B2	B2	R710	E2	B2
C705	F3	A3	R414H	B2	B2	R711	E2	B2
C711	E2	B2	R414I	B1	B2	R715	E3	B2
C712	F2	B2	R415A	C5	B2	R716	E4	B2
C716	F2	B2	R415B	C4	B2	R717	E2	B2
C718	F3	B3	R415C	C4	B2	R718	E2	B3
C719	D4	B3	R415D	C3	B2	R720	E2	B3
C722	F4	A3	R415F	C3	B2	R721	E4	B2
C801	F4	A3	R415G	C2	B2	R722C	A1	A3
C802	F5	A3	R415H	C2	B1	R722G	B1	B2
C803	F5	A3	R415I	C1	B2	R723D	A1	B2
C804	F5	A3	R506A	A5	A2	R723H	A1	B2
C806	F5	A3	R506B	A5	A2	R803	F4	A3
C809	D4	B3	R506C	A4	A2	R804	F5	A3
C810	E5	B3	R506D	A4	A2	R808	E5	A3
C813	F5	B3	R506F	A3	A2	R810	E4	B3
C823	D4	B3	R506G	A3	A2	R811	E5	B3
C910	D3	B3	R506H	A2	A2	R812	D4	B3
CR708	E2	B2	R506I	A2	A2	R813	D3	B3
CR709	E2	B2	R507B	B4	A2	R823	D4	B3
CR710	E3	B3	R507B	B5	A2	R824B	B1	A3
CR711	E3	B3	R507C	B4	A2	R824E	B1	A3
CR715	F2	B3	R507F	B4	A2	R902	D4	A3
CR716	F2	B2	R507F	B2	A2	R908	D3	D3
CR717	F3	B3	R507G	B3	A2	R910	D3	D3
CR718	F3	B3	R507H	B1	A2	R911	E5	D3
CR808	E5	A3	R507I	A5	A2	R912	F4	D3
CR809	E5	B3	R508A	A5	A2	R913	E5	D3
CR812	F5	B3	R508B	A4	A2	R914	F2	D3
CR813	F5	B3	R508D	A4	A2	R918A	D3	D3
CR908	D3	A3	R508F	A3	A2	R918B	D3	D3
CR909	D3	B3	R508G	A2	A2	R918C	D3	D3
DL415	C5	B2	R508H	A2	A2	R918D	D3	D3
J101	F1	A3	R508I	B4	A2	R918E	D3	D3
J701	F4	A3	R701A	A1	A1	R918F	D3	D3
J701	A1	A3	R701B	A5	A2	R918G	D3	D3
Q501	B5	A2	R701D	B5	A2	R918H	D3	D3
Q502	B5	A2	R701D	B5	B5	TP707	E2	A3
Q503	B4	A2	R701E	A4	A2	TP711	E2	A3
Q504	B4	A2	R701F	A4	A2	TP808	E4	A3
Q505	B3	A2	R701G	A3	A2	TP910	D3	A3
Q506	B3	A2	R701H	A3	A2	U711A	F3	A3
Q507	B2	A2	R701I	B4	A2	U711B	F3	A3
Q508	B2	A2	R702A	A1	A1	U711C	F3	A3
Q509	B4	B2	R702B	B3	A2	U711D	E2	A3
Q510	B4	B2	R702C	A3	A3	U725B	B1	B2
Q511	B3	B2	R702D	A3	A3	U808A	F5	A3
Q512	B3	B2	R702E	B2	A3	U808C	E3	A3
Q513	B2	B2	R702F	B2	A3	U808D	E3	A3
Q514	B2	B2	R702G	A3	A3	U821C	B1	D3
Q515	B1	B2				U918	D3	B3
						U925	D2	A3

The colors on this page correspond to the following 91A24 diagnostic functions:

0 CNTR TIMR
1 MEM ADDR
2 ACQ MEM
3 STK PNTR
4 WRD REC
5 OCCR CNTR
6 DAC THRSH
7 PRB CLK EX

The function numbers at the beginning and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information refer to the introduction of this Diagrams section.

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C319	C5	B2	R624A	B1	B2
C544	C5	C2	R624B	B3	B2
J173	A1	E1	R624C	C3	B2
J183	A3	E1	R624D	B4	B2
J185	A4	F1	R624E	C4	B2
Q318	C3	B2	R631	C1	C2
Q319	C3	B2	R901	C5	A3
Q519	C4	B2	U118	E2	B1
Q520	C4	B2	U121	E1	B1
Q628	C2	C2	U125	D2	D1
Q629	C2	C2	U218A	E2	E4
Q902	C5	A3	U218B	E4	E4
R186	B4	F1	U218C	E3	B1
R187	B4	F1	U218D	E1	B1
R273A	B2	E1	U221	E3	B1
R273B	B1	E1	U225	D3	D3
R273C	B3	E1	U275A	B2	E1
R273D	B4	E1	U275B	B3	E1
R273E	B1	E1	U275C	B4	E1
R278	B3	E1	U275D	B5	E1
R281	B3	F1	U421	E5	B2
R419	C3	B2	U425	D5	B2
R526A	C1	C2	U718B	B4	B2
R526B	C2	B2	U718C	B3	B2
R526C	C4	B2	U718D	B2	B2
R529D	C2	C2	U808B	C5	A3
R529E	C4	C2			

The colors on this page correspond to the following 91A24 diagnostic functions:

0 CNTR TIMR
1 MEM ADDR
2 ACQ MEM
3 STK PNTR
4 WRD REC
5 OCCR CNTR
6 DAC THRSH
7 PRB CLK EX

The function numbers at the beginning and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information refer to the introduction of this Diagrams section.

COMPONENT NUMBER EXAMPLE

A23 A2 R1234

Assembly Number / Subassembly Number (if used) / Schematic Circuit Number

Chassis mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

LOGIN CLOCK GENERATOR
SYSTEM DATA LOGIN
MUX MODE LOGIN
PROBE DATA LOGIN
CLOCK DISTRIBUTION
Vbb GENERATOR
P/O A35 91A24 DATA ACQUISITION BD.

*JUMPERS SHOWN ARE FOR 91A24 ALONE. WITH 91AE24 MODULES, USE THE JUMPERING SHOWN BELOW.

Static Sensitive Devices
See Maintenance Section

NOTE: Table 11-1 shows IC Pinout (VCC & Gnd).

P/O A35 91A24 DATA ACQ. LOGIN REGISTERS ⬦72

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C467	B4	E2	U238	E4	C1
C468	B4	E2	U241	C2	C1
Q465	B4	E2	U245	C3	C1
R459B	B5	D2	U428	B3	C2
R467	B4	E2	U438	E5	C2
R468	B4	E2	U441	C3	C2
R536	D5	C2	U445	C3	C2
R658I	D3	D2	U461A	B5	D2
TP138	B4	C1	U461B	F5	D2
TP465	B4	E2	U468D	E5	E2
U128	B1	C1	U468B	B4	E2
U138	E3	C1	U468E	B4	E2
U141	C1	C1	U468F	B4	E2
U145	C2	C1	U475B	B4	E2
U228	B2	C1	U578A	B4	E2

The colors on this page correspond to the following 91A24 diagnostic functions:

0	CNTR TIMR
1	MEM ADDR
2	ACQ MEM
3	STK PNTR
4	WRD REC
5	OCCR CNTR
6	DAC THRSH
7	PRB CLK EX

The function numbers at the beginning and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information refer to the introduction of this Diagrams section.

COMPONENT NUMBER EXAMPLE

Component Number

A23 A2 R1234

Assembly Number / Subassembly Number (if used) / Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

*NOTE: THIS BLOCK IS COMMON TO ALL 2149H'S SHOWN ON THIS PAGE.

MEMORY ADDRESS REGISTERS

ACQUISITION MEMORY DATA REGISTERS

CHIP SELECT GENERATOR

ACQUISITION MEMORY RAM

Ⓧ Static Sensitive Devices
See Maintenance Section

NOTE: Table 11-1 shows IC Pinout. (VCC & Gnd).

P/O A35 91A24 DATA ACQUISITION BD.

P/O A35 91A24 DATA ACQ. ACQUISITION MEMORY

Table 11-8
91A24 DATA QUALIFIER WORD RECOGNIZERS 74
91A24 DATA ACQUISITION BOARD, ASSEMBLY A35

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C190	E5	F1	U261C	C3	D1
J176	C2	E1	U265C	E1	E1
J178	C3	E1	U268C	C2	E1
P1	A1	B3	U278A	C2	E1
P1	F4	B3	U278B	C2	C2
R162	D5	D1	U278E	C3	E1
R185D	C1	F1	U278F	C4	C4
R185E	C2	F1	U281	C2	E2
R185F	C3	F1	U288	E3	E1
R185G	C3	F1	U291A	D1	F1
R190	E5	F1	U291B	D3	F1
R491A	C4	F2	U291D	D3	F1
R491B	F3	F2	U351	B3	D1
R491D	C5	F2	U478B	F3	D5
R585	D5	F2	U481B	D5	D5
R754	C5	D2	U485B	E2	F2
R954	E4	D3	U485D	E2	F2
R955	E4	D3	U488A	C5	F2
R956	E5	D3	U551	B5	D1
R9151	B2	D1	U568D	D5	C5
U168B	C1	E1	U578C	E5	E2
U198A	E4	F1	U581B	C5	C5
U198B	D2	F1	U921B	E4	B3
U198C	E1	F1	U921C	E5	B3
U261A	C3	D1	W918	F4	B3
U261B	C2	D1			

The colors on this page correspond to the following 91A24 diagnostic functions:

- 0 CNTR TIMR
- 1 MEM ADDR
- 2 ACQ MEM
- 3 STK PNTR
- 4 WRD REC
- 5 OCCR CNTR
- 6 DAC THRSH
- 7 PRB CLK EX

The function numbers at the beginning and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information refer to the introduction of this Diagrams section.

DATA QUALIFIER WORD RECOGNIZER
91A24 START/STOP
DATA QUALIFIER WORD RECOGNIZER RAM
STORAGE CONTROL CIRCUITRY
STORING DATA
91A24 SYSTEM CLOCK

Component Number Example

A23 A2 R1234 — Assembly Number / Subassembly Number (if used) / Schematic Circuit Number

Chassis mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices — See Maintenance Section

NOTE: Table 11-1 shows IC Pinout. (VCC & Gnd).

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P/O A35 91A24 DATA ACQUISITION BD.

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91A24 DATA QUALIFIER WORD RECOGNIZERS 74

Table 11-9
91A24 STACK WORD RECOGNIZER ⬦75
91A24 DATA ACQUISITION BOARD, ASSEMBLY A35

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C165	E2	E1	U165B	F4	E1
DL195	E5	F1	U168A	D2	E1
J171	D1	E1	U248	B3	D1
J271	E1	E1	U255	C3	D1
P1	A1	B3	U258	E4	D1
R149	A4	D1	U265A	D5	E1
R166E	E5	E1	U268B	E2	F1
R191	D2	F1	U291C	D2	F1
R196	E5	F1	U448	B4	D2
R197	E5	F1	U455	C4	D2
R266	E2	E1	U458	E5	D2
U148	C2	D1	U468C	B1	E2
U155	C2	D1	U485C	B2	F2
U158	E3	D1	U488B	C1	F2
U161	F4	D1	U495A	D1	F2
U165A	E2	E1	U555	C5	D2

The colors on this page correspond to the following 91A24 diagnostic functions:

0 CNTR TIMR
1 MEM ADDR
2 ACQ MEM
3 STK PNTR
4 WRD REC
5 OCCR CNTR
6 DAC THRSH
7 PRB CLK EX

The function numbers at the beginning and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information refer to the introduction of this Diagrams section.

DAS 9100 SERIES   4541-1111   91A24 STACK WORD RECOGNIZER ⬦75

Table 11-10
91A24 TRIGGER CIRCUITRY ⟨76⟩

91A24 DATA ACQUISITION BOARD, ASSEMBLY A35

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C396	C2	F2	U265B	B2	E1
C397	D4	F1	U265D	B5	E1
C597	E4	F2	U268E	B5	E1
C697	F4	F2	U285C	C5	F1
J181	B2	E1	U295	D4	F1
J272	B4	E1	U298A	C4	F1
J801	F5	A3	U298B	C4	F1
P0	F3	D3	U468A	E3	E2
P0	A3	D3	U471A	B5	E2
P1	F5	B3	U471B	C2	E2
Q596	E4	F2	U475A	C5	E2
Q598	F4	F2	U475C	C3	E2
Q952	F5	D3	U475D	C4	E2
R166	E3	E1	U478A	C3	E2
R198	D5	F1	U481A	B5	E2
R296	E4	F1	U485A	B2	F2
R297	E3	E1	U491A	D4	E2
R381	D4	E2	U491B	E3	E2
R391	D4	F2	U495B	C2	E2
R397	C2	F2	U495C	E4	E2
R398	C2	F2	U495D	C4	B4
R399	E4	F1	U495E	F3	F2
R491E	B4	F2	U495F	F4	F2
R491F	C4	F2	U558A	B2	D2
R491G	F2	F2	U558A	C5	E2
R572	C2	E2	U568A	B2	E2
R585	D5	F2	U568B	C5	C1
R595	E4	F2	U568C	B2	E2
R596	E4	F2	U571	C1	E2
R598	E4	F2	U575A	B4	E2
R599	F4	F2	U575B	B5	E2
R658C	B5	D2	U575D	B2	E2
R698	F4	F2	U578D	B1	
R699	F4	F2	U581D	E1	
R793A	E5	F3	U585	E1	E1
R798	E5	F2	U588	E2	E2
R801	C5	A3	U591	E2	E2
R924	E5	B3	U595	E3	F2
R948	E5	D3	U788	E1	F3
R958	E5	D3	U795	E3	F3
R961	E5	D3	U798A	E5	F2
U168C	B3	E1	U798B	D5	F2
U198D	C3	F1	W925	E5	B3
			Y498	F4	F2

The colors on this page correspond to the following 91A24 diagnostic functions:

0 CNTR TIMR
1 MEM ADDR
2 ACQ MEM
3 STK PNTR
4 WRD REC
5 OCCR CNTR
6 DAC THRSH
7 PRB CLK EX

The function numbers at the beginning and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information refer to the introduction of this Diagrams section.

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91A24 TRIGGER CIRCUITRY ⟨76⟩

P/O A35 91A24 DATA ACQ. TRIGGER CIRCUITRY

Table 11-11
91A24 CLOCK QUALIFIER ⟨77⟩
91A24 DATA ACQUISITION BOARD, ASSEMBLY A35

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C541	F1	C2	R831B	A3	C3
C549	F2	D2	R831C	A4	C3
C622	F4	B2	R831D	A4	C3
C925	B2	C3	R831E	A4	C3
C931	D2	C3	R842G	D4	C3
C942	C2	C3	R921	A1	B3
Q539	E4	C2	R949	B4	D3
Q540	F4	C2	R950	C4	D3
Q543	E2	C2	R951	D2	D3
Q544	F2	C2	R952	D2	D3
Q545	E5	C2	R953	A1	D3
Q546	F5	C2	R959	A1	D3
Q951	A1	D3	R962	A1	D3
R539	F4	C2	U575C	E3	E2
R540	F4	C2	U721	E1	B2
R541	E3	C2	U728A	B5	C2
R544	F2	C2	U728B	C5	C2
R545	E2	D2	U731A	D5	C2
R546	F2	D2	U825A	D4	B3
R547	F5	D2	U825B	D3	B3
R548	E4	D2	U828A	C4	C3
R549	E4	C2	U828B	C3	C3
R731D	A5	C2	U831A	B4	B3
R731E	A5	C2	U831B	B3	C3
R737C	D4	C2	U928	B2	C3
R737D	C5	C2	U931	D1	C3
R737E	B4	C2	U935	B5	C3
R737F	C4	C2	U938	B1	C3
R737G	B5	C2	U941	C1	C3
R746E	D5	D2	U945	D1	C3
R749E	E1	D2			

The colors on this page correspond to the following 91A24 diagnostic functions:

0	CNTR TIMR
1	MEM ADDR
2	ACQ MEM
3	STK PNTR
4	WRD REC
5	OCCR CNTR
6	DAC THRSH
7	PRB CLK EX

The function numbers at the beginning and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information refer to the introduction of this Diagrams section.

Table 11-12
91A24 CLOCK GENERATOR ◇ 78

91A24 DATA ACQUISITION BOARD, ASSEMBLY A35

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C751	E2	D2	R904	F4	A3
C752	E3	D2	R905	F4	A3
C753	E5	D2	R906	E5	A3
C814	C5	B3	R907	F4	A3
C851	E2	D3	R915	C5	B3
C852	E4	D3	R916	C5	B3
C853	E4	D3	R917	C5	B3
C901	F4	A3	U535A	E1	C2
C902	E5	A3	U535B	E2	C2
C903	F4	A3	U538A	E4	C2
C904	F5	A3	U731B	B5	C2
C906	F4	A3	U735A	B1	C2
P1	A5	B3	U735B	C1	C2
Q901	F4	A3	U738A	B4	C2
R534A	B1	C2	U738B	C4	C2
R534C	E5	C2	U741A	D1	C2
R534C	B3	C2	U741B	D1	C2
R534D	D2	C2	U745A	D4	C2
R534E	B4	C2	U745B	D4	C2
R538A	D3	C2	U748B	C5	C2
R538B	D3	C2	U751A	D3	D2
R538C	D4	C2	U751B	D3	D2
R538D	C2	C2	U835A	B2	C3
R538E	C4	C2	U835B	C2	C3
R737A	E2	C2	U838A	B5	C3
R737B	E2	C2	U838B	C5	C3
R746C	D5	D2	U841A	D2	D2
R746D	B5	D2	U841B	D2	D2
R746F	E3	D2	U845A	D5	D2
R749B	A2	D2	U845B	D5	D2
R749C	A4	D2	U848A	E1	D3
R749D	A3	D2	U848B	E2	D3
R751D	E2	D3	U848C	E3	D3
R751E	E2	D3	U848D	E3	D3
R751F	E3	D3	U848E	E5	D3
R751G	E5	D3	U848F	E4	D3
R751H	E5	D3	U851A	D3	D3
R751I	E4	D3	U851B	D3	D3
R814	C5	B3	U904	F4	A3
R842C	D5	C3	U921A	D5	B3
R842D	D5	C3	U921D	D5	B3
R842F	E2	C3	U948A	C3	D3
R842F	E3	C3	U948B	C3	D3
R849A	A5	D3	U951A	B3	D3
R849B	A2	D3	U951B	C3	D3
R849C	A3	D3			

The colors on this page correspond to the following 91A24 diagnostic functions:

0	CNTR TIMR
1	MEM ADDR
2	ACQ MEM
3	STK PNTR
4	WRD REC
5	OCCR CNTR
6	DAC THRSH
7	PRB CLK EX

The function numbers at the beginning and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information refer to the introduction of this Diagrams section.

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Figure 11-3. A36 91AE24 Data Acquisition Expander Module component locations.

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Static Sensitive Devices
See Maintenance Section

Table 11-13
CONTROLLER INTERFACE 〈79〉
91AE24 DATA ACQUISITION EXPANDER BOARD, ASSEMBLY A36

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C101	A4	A1	C782	A4	F3
C126	A4	B1	C786	A4	F3
C129	A4	C1	C789	A4	F3
C136	A4	C1	C808	A4	A3
C143	A4	C1	C865	A4	E3
C158	A4	D1	C868	A4	E3
C163	A4	D1	C871	A4	E3
C222	A4	B1	C878	A4	E3
C232	A4	C1	C889	A4	F3
C262	A4	D1	C965	A4	D3
C302	A4	A2	P0	A1	A5
C318	A4	B2	P1		A5
C361	A4	E1	R658A	E5	D3
C371	A4	E1	R658H	E3	D2
C378	A4	E2	R772A	C2	D2
C388	A4	F2	R960A	D2	D3
C395	A4	F2	R960C	D2	D3
C405	A3	A2	R960G	F1	D3
C429	A4	C2	R969	B2	B3
C432	A4	C2	R970	A4	B3
C439	A4	E2	TP461	A4	A4
C476	A4	F2	TP544	A4	C2
C486	A4	F2	TP592	A4	F2
C502	A4	A2	TP622	A4	B2
C505	A4	B2	U285A	C3	F1
C524	A4	B2	U285D	C3	F1
C558	A4	E2	U558C	C2	D2
C566	A4	E2	U561	D4	D2
C573	A4	E2	U565	D5	D2
C586	A4	F2	U758	E3	D2
C588	A4	F2	U761	E4	D2
C591	A4	F2	U765	E5	E2
C595	A4	E2	U768	C5	E2
C668	A4	E2	U958	E2	D3
C681	A4	E2	U965	D2	D2
C707	A3	A3	U975	B3	E3
C708	A3	A3	U978	B1	E3
C726	A4	C2			
C741	A4	C2			
C759	A4	D3			

The colors on this page correspond to the following 91AE24 diagnostic functions:

- 0 MEM ADDR
- 1 ACQ MEM
- 2 STK PNTR
- 3 WRD REC
- 4 DAC THRSH
- 5 PRB CLK EX

The function numbers at the beginning and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information refer to the introduction of this Diagrams section.

P/O CONTROLLER INTERFACE

P/O A36 91AE24 DATA ACQUISITION EXPANDER BD

Static Sensitive Devices
See Maintenance Section

NOTE: Table 11-1 shows IC Pinout. (VCC & Gnd).

COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number | Subassembly Number (if used) | Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Table 11-14
91AE24 CONTROLLER INTERFACE READBACK CIRCUITRY 80

91AE24 DATA ACQUISITION EXPANDER BOARD, ASSEMBLY A36

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
J101	A3	A1	U131	D5	C1
J101	F1	A1	U135	C4	C1
J401	A3	A2	U231	E5	C1
J401	F1	A2	U235	B5	C1
J701	A4	A3	U268F	C3	E1
J701	F1	A3	U431	F5	C2
P0	F3	B3	U771	B3	E2
R772C	B4	E3	U775	C3	E2
R772E	B3	E3	U778	C3	E2
R772G	B3	E3	U785	D3	F2
R793G	E3	F3	U791	E3	F2
R799	E3	F2	U998	A1	F3

The colors on this page correspond to the following 91AE24 diagnostic functions:

- 0 MEM ADDR
- 1 ACQ MEM
- 2 STK PNTR
- 3 WRD REC
- 4 DAC THRSH
- 5 PRB CLK EX

The function numbers at the beginning and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information refer to the introduction of this Diagrams section.

COMPONENT NUMBER EXAMPLE

A23 A2 R1234

Static Sensitive Devices
See Maintenance Section

NOTE: Table 11-1 shows IC Pinout (VCC & Gnd).

P/O CONTROLLER INTERFACE

P/O A36 91AE24 DATA ACQUISITION EXPANDER BD.

MEMORY READBACK

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
DL115	C1	B1	R102G	B1	A1	R306H	D2	A2
DL315	E1	B2	R102H	B1	A1	R306I	D1	A2
J101	A1	A1	R102I	A1	A1	R307B	E4	A2
J401	D1	A2	R106A	A5	A1	R307C	E5	A2
Q101	B5	A1	R106B	A4	A1	R307D	E4	A2
Q102	A5	A1	R106C	A4	A1	R307G	E2	A2
Q103	B4	A1	R106D	A3	A1	R307H	E3	A2
Q104	A4	A1	R106F	A2	A1	R307I	E1	A2
Q105	B3	A1	R106G	A2	A1	R307J	E2	A2
Q106	A3	A1	R106H	A2	A1	R308A	D5	A2
Q107	B2	A1	R106I	A1	A1	R308B	D4	A2
Q108	A2	A1	R107B	B5	A1	R308D	D4	A2
Q109	B4	B1	R107C	B4	A1	R308F	D3	A2
Q110	A4	B1	R107D	B4	A1	R308G	D2	A2
Q111	B3	A1	R107E	B3	A1	R308H	D2	A2
Q112	A3	A1	R107F	B2	A1	R308I	D1	A2
Q113	B2	A1	R107G	B3	A1	R314A	E5	B2
Q114	A2	A1	R107I	B2	A1	R314B	E4	B2
Q115	B1	A1	R107J	B2	A1	R314C	E4	B2
Q116	A1	B1	R108A	A5	A1	R314E	E3	B2
Q301	D5	A1	R108B	A4	A1	R314G	E3	B2
Q302	E5	A1	R108C	A4	A1	R314H	E2	B2
Q303	E4	A2	R108D	A3	A1	R314I	E1	B2
Q304	D4	A2	R108F	A3	A1	R315A	F5	B2
Q305	E3	A2	R108G	A2	A1	R315C	F4	B2
Q306	D3	A2	R108H	A2	A1	R315D	F3	B2
Q307	E2	A2	R108I	A1	A1	R315E	F2	B2
Q308	D2	A2	R114A	B5	B1	R315F	F2	B2
Q309	E4	A1	R114B	B4	B1	R315H	F2	B2
Q310	D4	B1	R114C	B4	B1	R315I	F1	B2
Q311	E3	A2	R114D	B3	B1	R401A	E5	A2
Q312	D3	B2	R114E	B3	B1	R401B	D5	A2
Q313	E2	B2	R114G	B2	B1	R401C	E4	A2
Q314	D2	B2	R114H	B2	B1	R401D	E4	A2
Q315	E1	A2	R114I	B1	B1	R401E	D4	A2
Q316	D1	B2	R115A	C5	B1	R401G	D3	A2
R101A	A5	A1	R115B	C4	B1	R401H	E3	A2
R101B	B5	A1	R115C	C4	B1	R502B	E3	A2
R101C	A4	A1	R115D	C3	B1	R502C	D3	A2
R101D	B4	A1	R115E	C3	B1	R502D	D2	A2
R101E	A4	A1	R115F	C2	B1	R502E	E2	A2
R101F	B4	A1	R115H	C2	B1	R502F	E2	A2
R101G	B3	A1	R115I	C1	B1	R502G	D2	A2
R101H	A3	A1	R306A	D5	A2	R502H	D1	A2
R102A	A3	A1	R306B	D4	A2	R502I	E1	A2
R102B	A3	A1	R306C	D4	A2			
R102D	B2	A1	R306D	D4	A2			
R102E	A2	A1	R306F	D3	A2			
R102F	B2	A1	R306G	D2	A2			

The colors on this page correspond to the following 91AE24 diagnostic functions:

0 MEM ADDR
1 ACQ MEM
2 STK PNTR
3 WRD REC
4 DAC THRSH
5 PRB CLK EX

The function numbers at the beginning and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information refer to the introduction of this Diagrams section.

PROBE A RECEIVER (INPUT FROM POD A CONNECTOR)

P/O A36 91AE24 DATA ACQUISITION EXPANDER BD.

Ⓧ Static Sensitive Devices
See Maintenance Section

NOTE: Table 11-1 shows IC Pinout. (VCC & Gnd).

PROBE B RECEIVER (INPUT FROM POD B CONNECTOR)

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234

Assembly Number — Subassembly Number (if used) — Schematic Circuit Number

Chassis mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

DAS 9100 SERIES

4541-1118

Table 11-16
91AE24 PROBE INTERFACE AND PROBE C RECEIVER ◇ 82

91AE24 DATA ACQUISITION EXPANDER BOARD, ASSEMBLY A36

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C201	F2	A1	Q512	B2	B2	R702C	A3	A2
C202	F1	A1	Q513	B2	B2	R702D	A3	B2
C401	F3	A2	Q514	B1	B2	R702E	A3	B2
C403	F3	A2	Q515	B1	B2	R702F	A2	B2
C508	F2	B2	Q516	B1	B2	R702G	A2	B2
C702	F2	A2	R103	D4	A1	R702H	A1	B1
C703	F3	A3	R104	D4	A1	R702I	A1	B2
C704	F1	A2	R110	D4	B1	R703	F2	A2
C705	F3	A3	R414A	B5	B2	R704	F3	A3
C711	E3	B3	R414B	B4	B2	R706	F1	A2
C712	E2	B2	R414C	B4	B2	R707	F3	E1
C716	F2	B2	R414E	B3	B2	R708	F3	E1
C718	F3	B3	R414F	B3	B2	R709	E3	E2
C719	D4	B3	R414G	B2	B2	R710	E2	E2
C722	F3	B3	R414H	B2	B2	R711	E3	E2
C801	F4	A3	R414I	B1	B2	R715	F3	E2
C802	F5	A3	R415A	C5	B2	R716	F3	E2
C803	F4	A3	R415C	C4	B2	R717	F3	E2
C804	F5	A3	R415D	C4	B2	R718	F3	E2
C806	F5	A3	R415E	C3	B2	R720	E3	B2
C809	D3	B3	R415F	C2	B2	R721	E3	B2
C810	E5	B3	R415G	C2	B2	R803	F4	E4
C813	F5	B3	R415H	C1	B2	R804	F5	E4
C823	D4	B3	R415I	C1	B2	R808	E4	E4
C910	D3	B2	R506A	A5	A2	R810	E4	E4
CR708	E2	B2	R506B	A5	A2	R811	E5	E4
CR709	E2	B2	R506C	A4	A2	R812	F4	D3
CR710	E3	B3	R506D	A4	A2	R813	F3	D3
CR711	E3	B3	R506F	A4	A2	R823	D4	D4
CR715	F2	B2	R506G	A4	A2	R902	E2	A3
CR716	F2	B2	R506H	A2	A2	R908	D3	D3
CR717	F3	B3	R506I	A1	A2	R910	D3	D3
CR718	F3	B3	R507A	B4	A2	R911	E4	D3
CR808	E4	A3	R507B	B5	A2	R912	F5	D3
CR809	E4	B3	R507C	B4	A2	R913	F3	D3
CR812	F4	B3	R507D	B4	A2	R914	F2	F5
CR813	F4	B3	R507F	B2	A2	R918A	A3	D3
CR908	D3	A3	R507G	B2	A2	R918B	A3	D3
CR909	D3	B3	R507H	B1	A2	R918C	B1	C3
DL415	C1	B2	R507I	B1	A2	R918D	B1	D3
J101	F1	A1	R508A	A5	A2	R918E	A5	D3
J401	F3	A2	R508B	A4	A2	R918F	B2	C3
J701	A1	A3	R508C	A4	A2	R918G	C3	C3
J701	F4	A3	R508D	A4	A2	R918H	C3	C3
Q501	B5	A2	R508E	A4	A2	TP707	F3	E3
Q502	B5	A2	R508G	A2	A2	TP808	E4	E3
Q503	B4	A2	R508H	A1	A2	TP910	D3	E3
Q504	B4	A2	R701B	B5	A3	U711A	F2	F2
Q505	B2	A2	R701C	B5	A2	U711B	F3	E3
Q506	B2	A2	R701D	B4	A2	U711C	E3	E3
Q507	B1	A2	R701E	B4	A2	U711D	E2	F2
Q508	B1	A2	R701F	B4	A2	U808A	F4	F4
Q509	B4	B2	R701G	B1	A2	U808B	E3	F4
Q510	B4	B2	R701H	A3	A2	U808C	D4	E3
Q511	B3	B2	R701I	A3	B3	U808D	E4	E4
			R702B	B3	B3	U918	D3	D3
						U925	D1	B3

The colors on this page correspond to the following 91AE24 diagnostic functions:

0 MEM ADDR
1 ACQ MEM
2 STK PNTR
3 WRD REC
4 DAC THRSH
5 PRB CLK EX

The function numbers at the beginning and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information refer to the introduction of this Diagrams section.
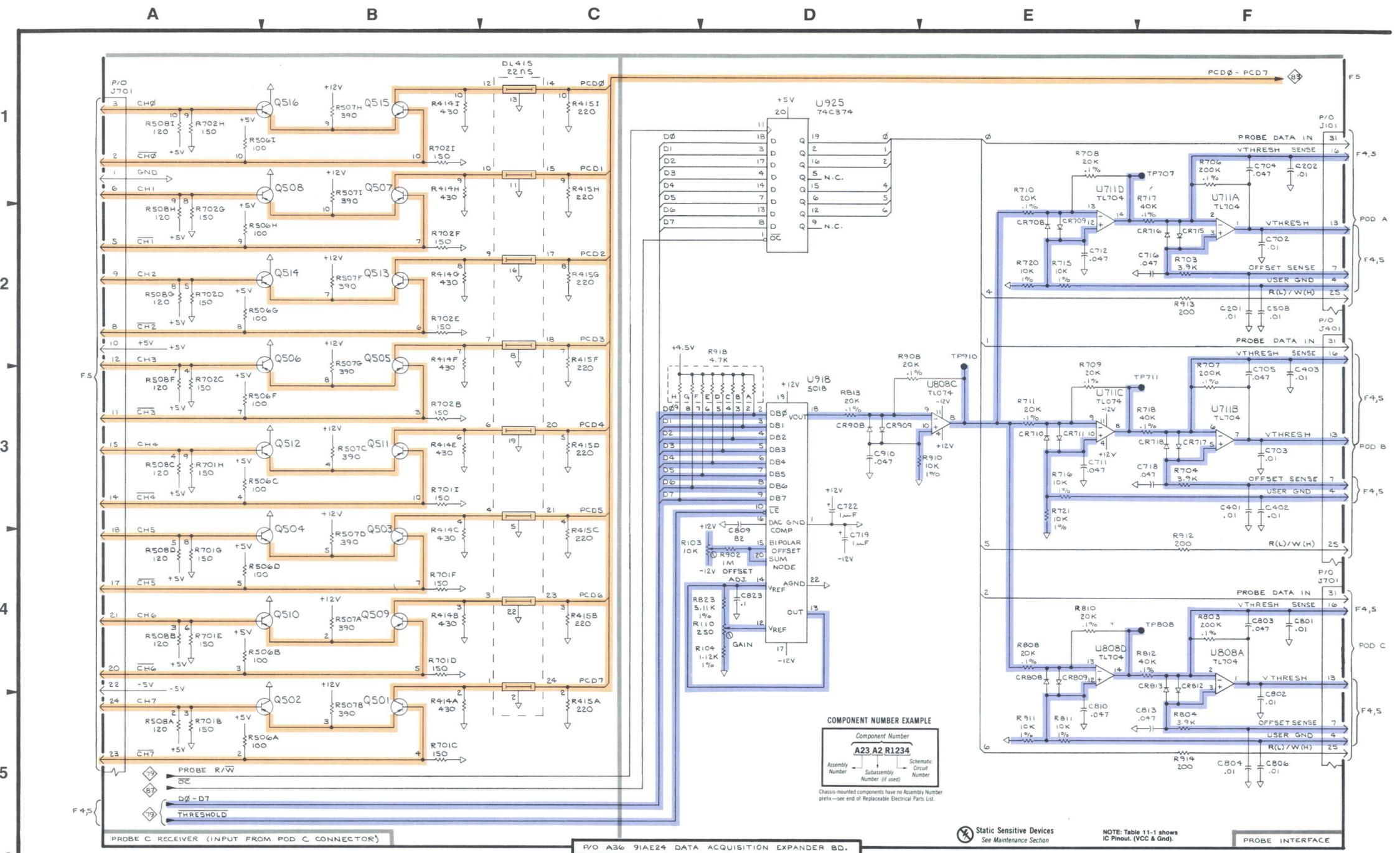
DAS 9100 SERIES

4541-1119

91AE24 PROBE INTERFACE AND PROBE C RECEIVER ◇ 82

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C319	C5	B2	R529D	C2	C2
C544	C5	B2	R529E	C4	C4
J173	A1	E1	R624A	B1	B2
J173	B1	E1	R624B	B3	B2
J183	A3	E1	R624C	C3	B2
J183	B3	E1	R624D	B4	B2
J185	B4	F1	R624E	C4	B2
J185	A4	F1	R631	C1	C2
Q318	C3	B2	R901	C5	A3
Q319	C3	B2	U118	E2	B1
Q519	C4	B2	U121	E1	B1
Q520	C4	B2	U125	D2	B1
Q628	C2	C2	U218A	E2	B1
Q629	C2	C2	U218B	E4	B1
Q902	C5	A3	U218C	E3	B1
R186	B4	F1	U218D	E1	B1
R187	B4	F1	U221	E3	B1
R273A	B2	E1	U225	D3	B1
R273B	B2	E1	U275A	D3	B1
R273C	B3	E1	U275B	B3	E1
R273D	B4	E1	U275C	B4	E1
R273E	B1	E1	U275D	B5	E1
R278	B3	E1	U421	E5	B2
R281	B3	F2	U425	D5	B1
R419	C3	B2	U718B	B4	B2
R526A	C1	B2	U718C	B3	B2
R526B	C2	B2	U718D	B1	B2
R526C	C4	B2	U808B	C5	A3

The colors on this page correspond to the following 91AE24 diagnostic functions:

0 MEM ADDR
1 ACQ MEM
2 STK PNTR
3 WRD REC
4 DAC THRSH
5 PRB CLK EX

The function numbers at the beginning and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information refer to the introduction of this Diagrams section.

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number — Subassembly Number (if used) — Schematic Circuit Number

Chassis mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

LOGIN CLOCK GENERATOR
SYSTEM DATA LOGIN
MUX MODE LOGIN
PROBE DATA LOGIN
CLOCK DISTRIBUTION
Vbb GENERATOR
P/O A36 91AE24 DATA ACQUISITION EXPANDER BD.

⚠ Static Sensitive Devices
See Maintenance Section

NOTE: Table 1-1 shows IC Pinout. (VCC & Gnd).

※ JUMPERS SHOWN ARE FOR THE LAST 91AE24 MODULE IN THIS DAISY CHAIN. FOR 91AE24 MODULES BETWEEN THE 91A24 AND THE LAST 91AE24, USE THE JUMPERING SHOWN BELOW.

P/O A36 91AE24 DATA ACQ. EXP. ⟨83⟩
LOGIN REGISTERS
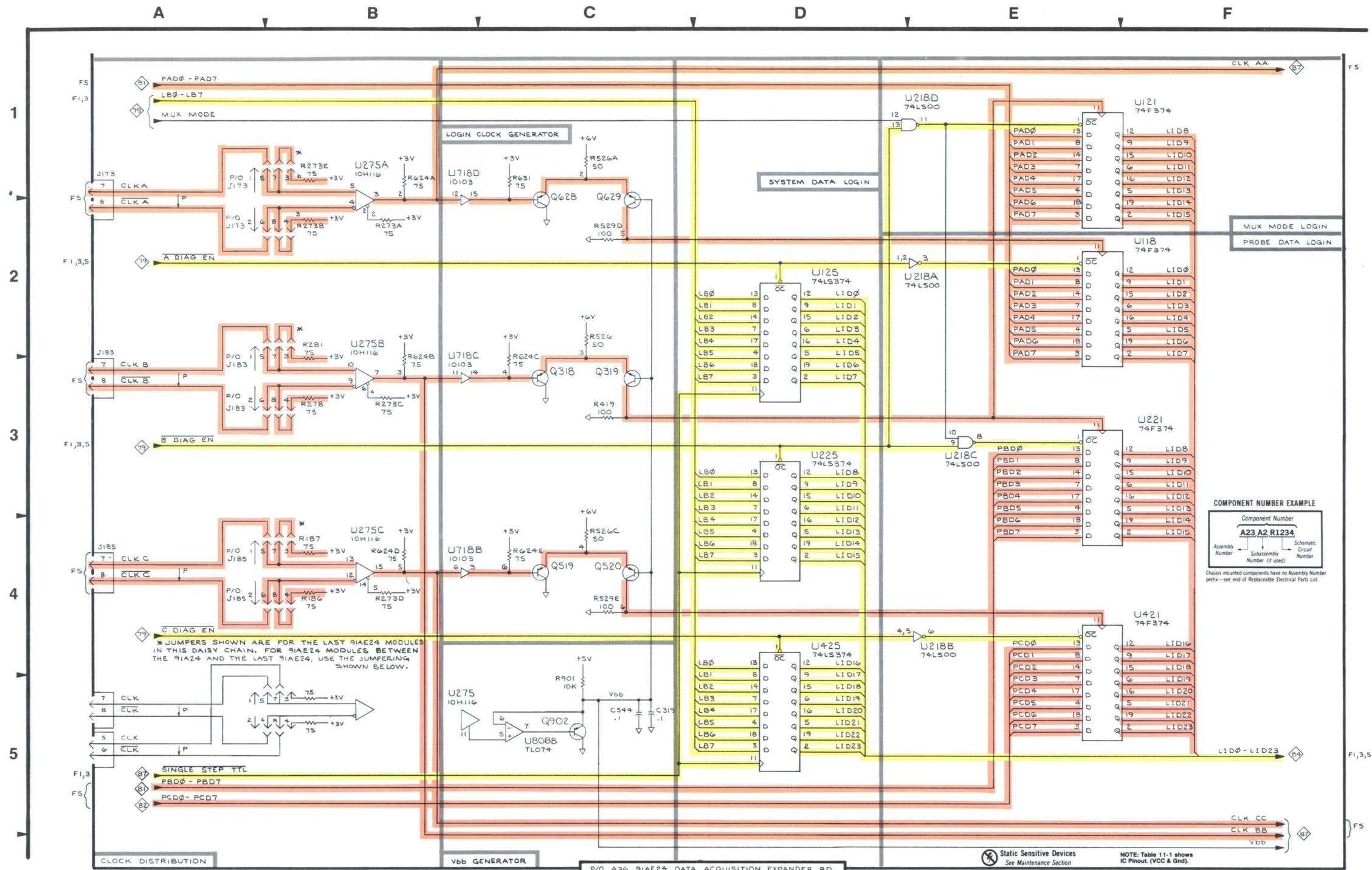
Table 11-18
91AE24 ACQUISITION MEMORY ◇84◇

91AE24 DATA ACQUISITION EXPANDER BOARD, ASSEMBLY A36

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C467	B4	E2	U238	E4	C1
C468	B4	E2	U241	C2	C1
Q465	B4	E2	U245	C3	C1
R459B	B5	D2	U428	B3	C2
R467	B4	E2	U438	E5	C2
R468	B4	E2	U441	C3	C2
R536	D5	C2	U445	C4	C2
R658I	D3	D2	U461A	B5	D2
TP138	C4	C1	U461B	F5	D2
TP465	B4	C2	U468B	E5	E2
U128	B1	C1	U468D	B4	E2
U138	E3	C1	U468E	B4	E2
U141	C1	C1	U468F	B4	E2
U145	C2	C1	U475B	B4	E2
U228	B2	C1	U578A	B4	E2

The colors on this page correspond to the following 91AE24 diagnostic functions:

▬▬	0 MEM ADDR
▬▬	1 ACQ MEM
	2 STK PNTR
	3 WRD REC
	4 DAC THRSH
	5 PRB CLK EX

The function numbers at the beginning and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information refer to the introduction of this Diagrams section.

Table 11-19
91AE24 DATA QUALIFIER WORD RECOGNIZERS ◇85

91AE24 DATA ACQUISITION EXPANDER BOARD, ASSEMBLY A36

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
J176	C2	E1	U261C	C3	D1
J178	C3	E1	U265C	E2	E1
P1	A5	D3	U268C	E2	E1
R162	D5	D1	U281	E2	E3
R491B	F3	F2	U288	E3	F1
R585	D5	F2	U291A	D1	F1
R754	D5	D2	U291B	D3	F1
U151	B2	D1	U291D	D3	F1
U168B	C1	E1	U351	B3	D2
U198A	E4	F1	U478B	F3	D2
U198B	D2	F1	U485B	E2	F2
U198C	E1	F1	U485D	E2	F2
U261A	C3	D1	U551	B5	D2
U261B	C2	D1			

The colors on this page correspond to the following 91AE24 diagnostic functions:

- ■ 0 MEM ADDR
- ■ 1 ACQ MEM
- ■ 2 STK PNTR
- ■ 3 WRD REC
- ■ 4 DAC THRSH
- ■ 5 PRB CLK EX

The function numbers at the beginning and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information refer to the introduction of this Diagrams section.

DATA QUALIFIER WORD RECOGNIZER RAM

P/O A36 91AE24 DATA ACQUISITION EXPANDER BD.

DATA QUALIFIER WORD RECOGNIZER CONTROL

STORAGE CONTROL CIRCUITRY

COMPONENT NUMBER EXAMPLE

Component Number

A23 A2 R1234

Assembly Number — Subassembly Number (if used) — Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Ⓧ Static Sensitive Devices
See Maintenance Section

NOTE: Table 11-1 shows IC Pinout. (VCC & Gnd).
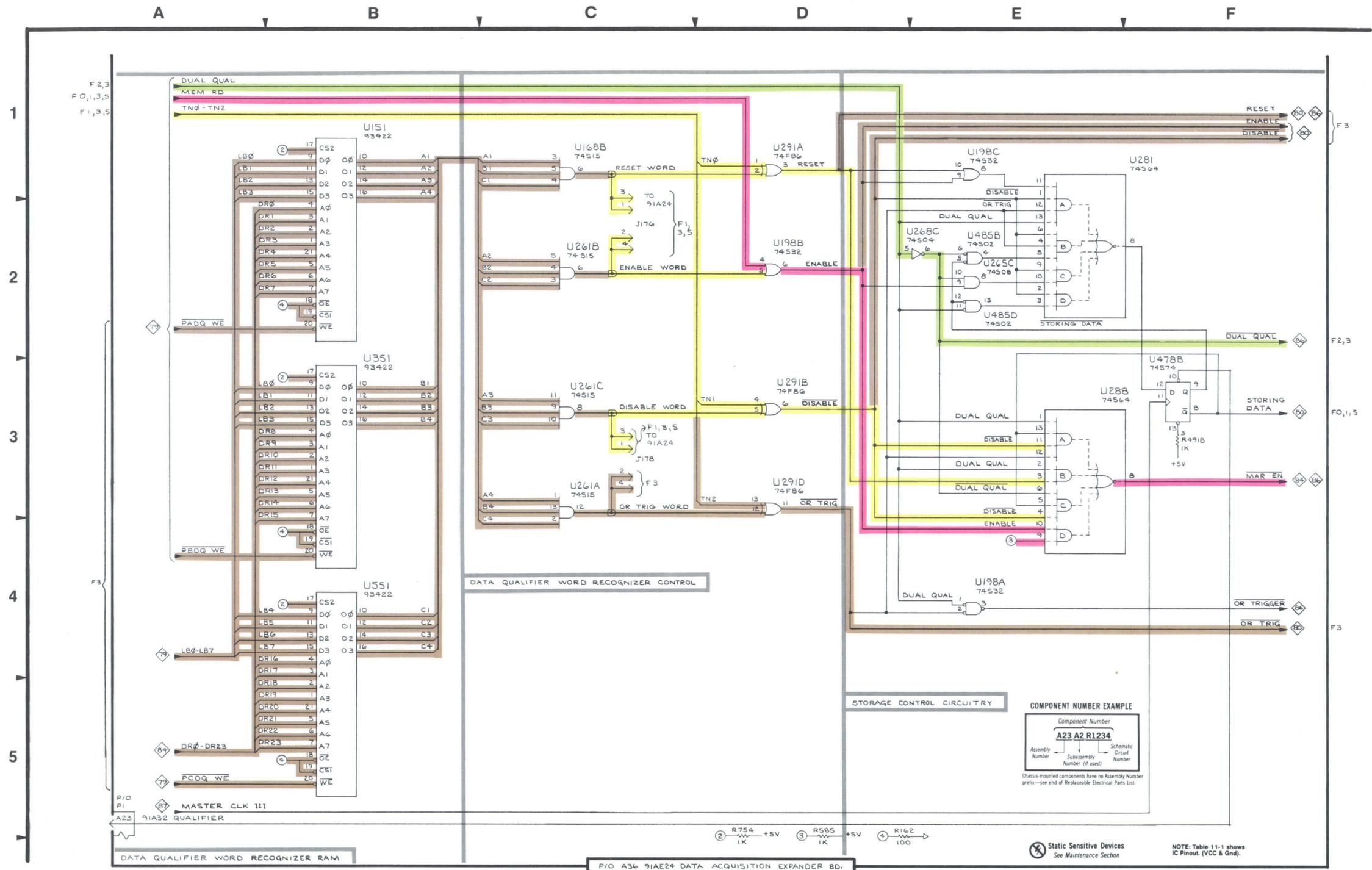
Table 11-20
91AE24 STACK WORD RECOGNIZER 86

91AE24 DATA ACQUISITION EXPANDER BOARD, ASSEMBLY A36

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
J171	F2	E1	U448	E2	D2
J181	B2	E1	U485A	B2	F2
R149	D3	D1	U555	E4	D2
R753	D4	D2	U558A	B3	D2
U148	C2	D1	U568C	A2	E2
U168A	E3	D1	U571	B2	E2
U248	C4	D1	U575B	B3	E2
U265B	A3	E1	U575D	B2	E2
U291C	F3	F1	U578D	B1	E2
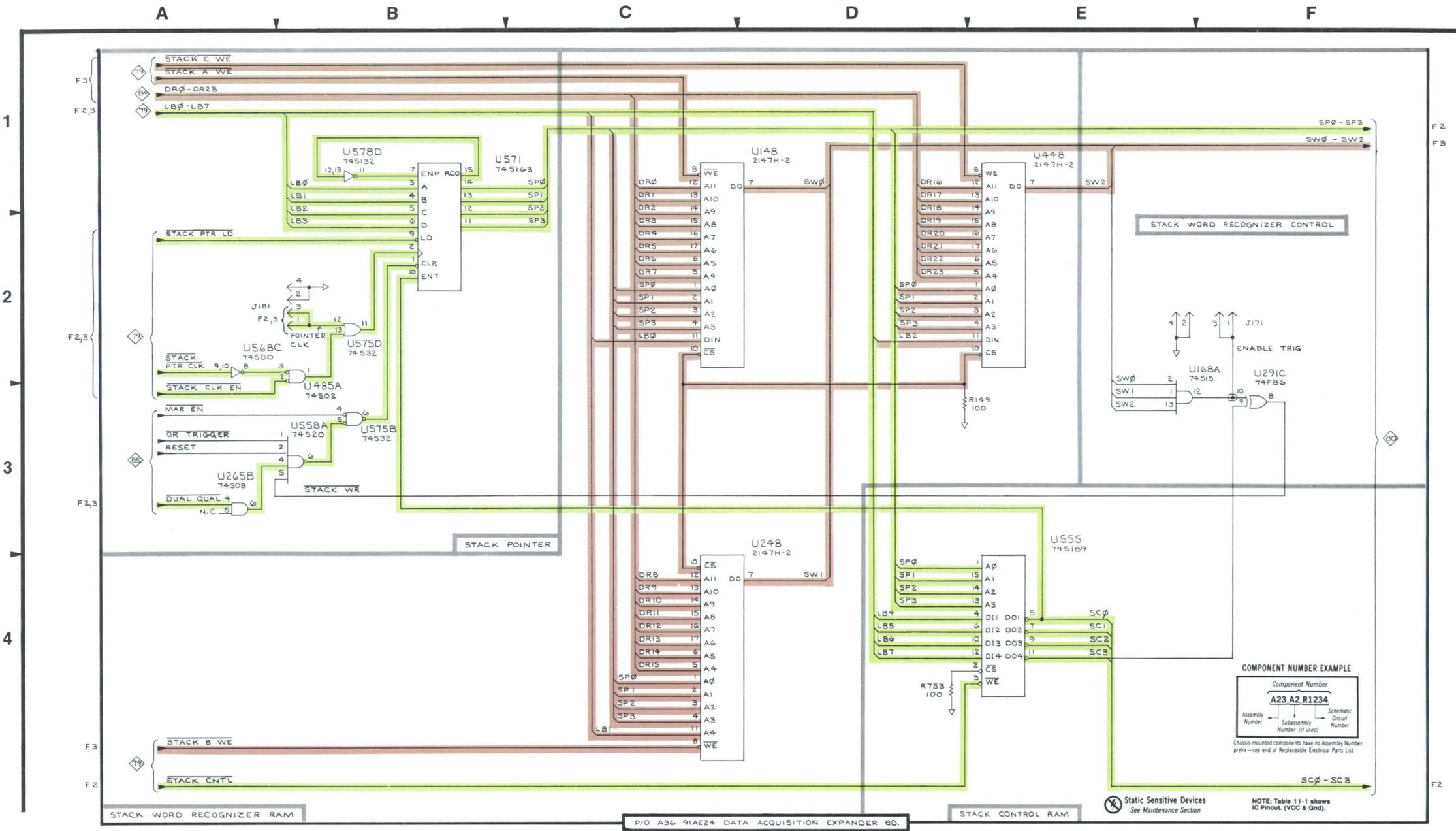
The colors on this page correspond to the following 91AE24 diagnostic functions:

- 0 MEM ADDR
- 1 ACQ MEM
- 2 STK PNTR
- 3 WRD REC
- 4 DAC THRSH
- 5 PRB CLK EX

The function numbers at the beginning and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information refer to the introduction of this Diagrams section.

STACK WORD RECOGNIZER CONTROL

STACK POINTER

COMPONENT NUMBER EXAMPLE

Component Number

A23 A2 R1234

Assembly Number — Subassembly Number (if used) — Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

STACK WORD RECOGNIZER RAM

P/O A36 91AE24 DATA ACQUISITION EXPANDER BD.

STACK CONTROL RAM

Static Sensitive Devices
See Maintenance Section

NOTE: Table 11-1 shows IC Pinout. (VCC & Gnd).

Table 11-21
91AE24 FIRST CLOCK SELECTOR ◇87

91AE24 DATA ACQUISITION EXPANDER BOARD, ASSEMBLY A36

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C541	E1	C2	R545	E2	D2
C549	E2	D2	R546	E2	D2
C622	E3	B2	R749E	E5	D2
C901	D3	A3	R904	C3	A3
C902	B3	A3	R905	B3	A3
C903	C3	A3	R906	B3	A3
C904	C3	A3	R907	C3	A3
C906	D3	A3	R921	B1	B3
C925	B1	B3	R951	D5	D3
C942	C1	C3	R952	D5	D3
Q539	E3	C2	R953	D5	D3
Q540	E3	C2	R959	A1	D3
Q543	E1	D2	R962	A1	D3
Q544	F1	D2	U575C	E5	E4
Q901	C3	A3	U721	E4	E4
Q951	A1	D3	U904	C3	B2
R539	E3	C2	U938	B2	C3
R540	E3	C2	U941	C1	C3
R541	E2	C2	U945	D2	C3
R544	E2	D2			

The colors on this page correspond to the following 91AE24 diagnostic functions:

Color	Function
0	MEM ADDR
1	ACQ MEM
2	STK PNTR
3	WRD REC
4	DAC THRSH
5	PRB CLK EX

The function numbers at the beginning and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information refer to the introduction of this Diagrams section.

P/O A36 91AE24 DATA ACQ. EXP.
FIRST CLOCK SELECTOR ◇87

MASTER CLOCK DISTRIBUTION

+3V POWER SUPPLY

MASTER CLOCK SELECTOR

P/O A36 91AE24 DATA ACQUISITION EXPANDER BD.

COMPONENT NUMBER EXAMPLE

Component Number

A23 A2 R1234

Assembly Number / Subassembly Number (if used) / Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

NOTE: Table 1-1 shows IC Pinout. (VCC & Gnd).

REPLACEABLE
MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

   1 2 3 4 5   Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
   - - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
   - - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
   - - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ABBREVIATIONS

"	INCH	ELCTRN	ELECTRON	IN	INCH	SE	SINGLE END
#	NUMBER SIZE	ELEC	ELECTRICAL	INCAND	INCANDESCENT	SECT	SECTION
ACTR	ACTUATOR	ELCTLT	ELECTROLYTIC	INSUL	INSULATOR	SEMICOND	SEMICONDUCTOR
ADPTR	ADAPTER	ELEM	ELEMENT	INTL	INTERNAL	SHLD	SHIELD
ALIGN	ALIGNMENT	EPL	ELECTRICAL PARTS LIST	LPHLDR	LAMPHOLDER	SHLDR	SHOULDERED
AL	ALUMINUM	EQPT	EQUIPMENT	MACH	MACHINE	SKT	SOCKET
ASSEM	ASSEMBLED	EXT	EXTERNAL	MECH	MECHANICAL	SL	SLIDE
ASSY	ASSEMBLY	FIL	FILLISTER HEAD	MTG	MOUNTING	SLFLKG	SELF-LOCKING
ATTEN	ATTENUATOR	FLEX	FLEXIBLE	NIP	NIPPLE	SLVG	SLEEVING
AWG	AMERICAN WIRE GAGE	FLH	FLAT HEAD	NON WIRE	NOT WIRE WOUND	SPR	SPRING
BD	BOARD	FLTR	FILTER	OBD	ORDER BY DESCRIPTION	SQ	SQUARE
BRKT	BRACKET	FR	FRAME or FRONT	OD	OUTSIDE DIAMETER	SST	STAINLESS STEEL
BRS	BRASS	FSTNR	FASTENER	OVH	OVAL HEAD	STL	STEEL
BRZ	BRONZE	FT	FOOT	PH BRZ	PHOSPHOR BRONZE	SW	SWITCH
BSHG	BUSHING	FXD	FIXED	PL	PLAIN or PLATE	T	TUBE
CAB	CABINET	GSKT	GASKET	PLSTC	PLASTIC	TERM	TERMINAL
CAP	CAPACITOR	HDL	HANDLE	PN	PART NUMBER	THD	THREAD
CER	CERAMIC	HEX	HEXAGON	PNH	PAN HEAD	THK	THICK
CHAS	CHASSIS	HEX HD	HEXAGONAL HEAD	PWR	POWER	TNSN	TENSION
CKT	CIRCUIT	HEX SOC	HEXAGONAL SOCKET	RCPT	RECEPTACLE	TPG	TAPPING
COMP	COMPOSITION	HLCPS	HELICAL COMPRESSION	RES	RESISTOR	TRH	TRUSS HEAD
CONN	CONNECTOR	HLEXT	HELICAL EXTENSION	RGD	RIGID	V	VOLTAGE
COV	COVER	HV	HIGH VOLTAGE	RLF	RELIEF	VAR	VARIABLE
CPLG	COUPLING	IC	INTEGRATED CIRCUIT	RTNR	RETAINER	W/	WITH
CRT	CATHODE RAY TUBE	ID	INSIDE DIAMETER	SCH	SOCKET HEAD	WSHR	WASHER
DEG	DEGREE	IDENT	IDENTIFICATION	SCOPE	OSCILLOSCOPE	XFMR	TRANSFORMER
DWR	DRAWER	IMPLR	IMPELLER	SCR	SCREW	XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
00779	AMP, INC.	P.O. BOX 3608	HARRISBURG, PA 17105
09922	BURNDY CORPORATION	RICHARDS AVENUE	NORWALK, CT 06852
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
82389	SWITCHCRAFT, INC.	5555 N. ELSTON AVE.	CHICAGO, IL 60630

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5 Name & Description	Mfr Code	Mfr Part Number
1-1	----- -----			1	CKT BOARD ASSY:DATA ACQ MODULE(SEE REPL)		
-2	131-2797-00	B010100	B010135	3	.CONN,RCPT,ELEC:RTANG HEADER,2 X 17,0.1 CT	22526	65461-033
				-	.(91A24 ONLY)		
	131-3087-00	B010136		3	.CONN,RCPT,ELEC:HEADER,RIGHT ANGLE 2 X 17	22526	SK9687
				-	.(91A24 ONLY)		
	131-2797-00	B010100	B010134	3	.CONN,RCPT,ELEC:RTANG HEADER,2 X 17,0.1 CT	22526	65461-033
				-	.(91AE24 ONLY)		
	131-3087-00	B010135		3	.CONN,RCPT,ELEC:HEADER,RIGHT ANGLE 2 X 17	22526	SK9687
				-	.(91AE24 ONLY)		
-3	131-3068-00			1	.JACK,TELEPHONE:SUBMINIATURE,CKT BD MT,2 C	82389	MDPC-2A-RA
	----- -----			-	.(91A24 ONLY)		
-4	214-0579-00			10	.TERM,TEST POINT:BRS CD PL	80009	214-0579-00
-5	136-0751-00			3	.SKT,PL-IN ELEK:MICROCKT,24 PIN	09922	DILB24P108
-6	136-0752-00			7	.SKT,PL-IN ELEK:MICROCIRCUIT,20 DIP	09922	DILB20P-108
-7	136-0755-00			3	.SKT,PL-IN ELEK:MICROCIRCUIT,28 DIP	09922	DILB28P-108
	----- -----			-	.(91A24 ONLY)		
-8	214-1337-00			1	.PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-9	105-0160-04			1	.EJECTOR,CKT BD:YELLOW PLASTIC	80009	105-0160-04
-10	131-0993-00			14	.BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
	----- -----			-	.(91A24 ONLY)		
-11	131-0608-00			4	.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	----- -----			-	.(91A24 ONLY)		
-12	131-2985-00			1	.CONN,RCPT,ELEC:HEADER,RTANG,2X17,0.1 CTR	22526	65624-134

STANDARD ACCESSORIES

-13	175-8167-00			1	CABLE ASSY,RF:50 OHM COAX,3.0 INCH LONG	80009	175-8167-00
	----- -----			-	(91A24 ONLY)		
	070-4672-00			1	MANUAL,TECH:INSTRUCTION	80009	070-4672-00
	----- -----			-	(91A24 ONLY)		
-14	175-8165-00			7	CABLE ASSY,RF:50 OHM COAX,79.0 INCH LONG	80009	175-8165-00
	----- -----			-	(91AE24 ONLY)		
	070-4672-00			1	MANUAL,TECH:INSTRUCTION	80009	070-4672-00
	----- -----			-	(91AE24 ONLY)		
	010-6460-01			3	PROBE,DATA ACQ:	80009	010-6460-01
	----- -----			-	(SEE 070-4345-00 MANUAL FOR BREAKDOWN OF		
	----- -----			-	REPLACEABLE PARTS)		
	070-4540-00			1	MANUAL,TECH:OPERATORS ADDENDUM	80009	070-4540-00
	070-3694-02			1	MANUAL,TECH:OPERATORS	80009	070-3694-02
	----- -----			-	(91A24 ONLY)		

OPTIONAL ACCESSORIES

	070-4541-00			1	MANUAL,TECH:SERVICE ADDENDUM	80009	070-4541-00
	175-8166-00			1	CA ASSY,SP,ELEC:10.0 INCH LONG	80009	175-8166-00
	062-6939-00			1	SOFTWARE,PKG:UTILITY MNEUMONICS II	80009	062-6939-00
	020-1041-00			1	ACCESSORY PKG:40 PIN UNIV PROBE INTERFACE	80009	020-1041-00
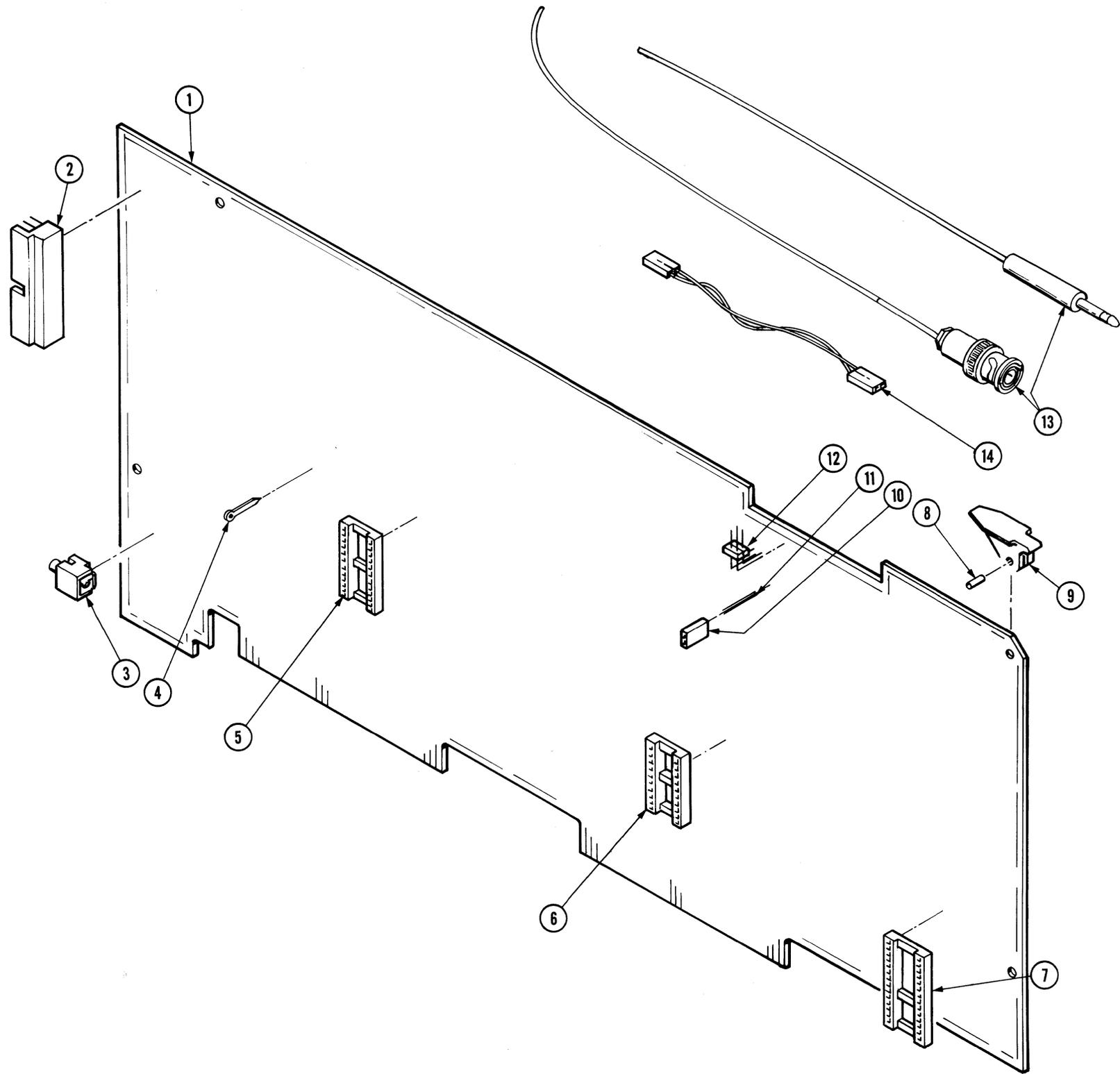
FIG. 1 EXPLODED

DESCRIPTION

DIAGRAM AND ELECTRICAL PARTS LIST CHANGES

The following have value and partnumber changes.

R823	321-0260-09	4.99K ohm
R104	321-0159-08	442 ohm
R110	311-1248-01	500 ohm variable resistor
U918	156-1311-01	

The above parts are located on diagram 71 for the 91A24 and diagram 82 for the 91AE24.

000-2775-00D

DESCRIPTION

* DAS 9120 SN B060100 & UP
  DAS 9100 SN B050326 & UP

TEXT AND ELECTRICAL PARTS LIST CHANGES

Front Cover 2nd paragraph

CHANGE TO:
    This addendum contains service information about the upgraded +5
    Volts Poser Supply Module for the DAS 9100 Series Mainframes. All
    DAS mainfrmaes will use the upgraded +5 V power supply 620-0296-
    01 as well as the previous model 620-0296-00.

Front cover

Delete 1st NOTE paragraph

EPL CHANGE

C258, Q224, and R257

CHANGE TO:
    C258   283-0696-00   CAP,FXD,CER,DI,2300 PF,1%,500V
    Q224   151-0302-00   TRANSISTOR:SILICON,PNP
    R257   305-0271-00   RES,FXD,CMPSN,270 OHM,5%,2W

000-2775-00D

DESCRIPTION

THIS IS A PAGE PULL AND REPLACEMENT PACKAGE

1. Remove the designated pages from your manual and insert the following pages 5-47 and 5-48.

2. Keep this cover sheet in the Change Information section at the back of your manual for a permanent record.

000-2775-00D

d. Trigger on the external trigger output of the pulse generator.

e. Position the trace at the graticule center line.

7. Move the oscilloscope probe tip to pin 20 of U448, and connect the probe ground to TP449 (ground test point).

8. Press START ACQUISITION.

9. Carefully center the rising edge of the clock pulse on the vertical and horizontal center lines of the graticule (see Figure 5-9).

10. Move the P6201 FET probe tip to pin 15 of U448.

11. Verify that the pulse geometry of the trigger input signal at pin 15 is at least 2.7 ns high and at least 2.7 ns low.

12. Verify that the setup time is ⩾1.1 ns and hold time is ⩾0.7 ns as shown in Figure 5-9.
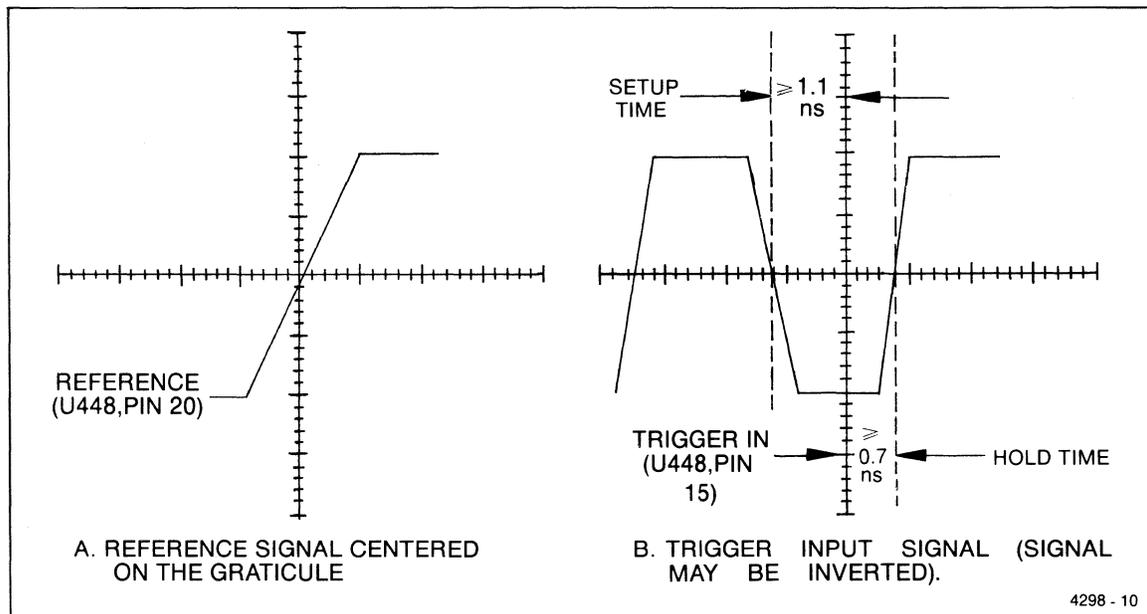
Figure 5-9. 91A04A high-speed clock setup and hold times.

(16) 91AE04A to 91A04A High-Speed Word Recognizer Timing

The following steps verify timing of the word recognizer circuits in any 91AE04A expander modules installed.

CAUTION

Do not install or remove any instrument modules in the DAS mainframe with the power on. Doing so can damage the module.

1. Power down the DAS.

2. Place the 91AE04A to be tested and the 91A04A master module on module extenders so that the short clock and word recognizer cables can be used.

3. Power up the DAS and perform the *Module Deskewing* procedure located in the *Operating Instructions* section of this addendum.

4. Connect channels 0 and 1 on the 91A04A P6453 probe to data channels 0 and 1 on the test fix-ture, connect channels 0 and 1 on the 91AE04A P6453 probe to data channels 2 and 3 on the test fixture, and connect the unused probe channels to the deskew connectors on the probe.

5. Enter the DAS Trigger Specification menu and select:

   • falling-edge triggering in the 91A04 External Trigger sub-menu, and

   • XX11 XX11 (binary) as the trigger word

6. Set up the oscilloscope as follows:

   a. Set the sensitivity at 200 mV/div.

   b. Set the sweep rate at 500 ps/div.

   c. Connect the P6201 FET probe tip to 100 K threshold at TP533, and connect the probe ground to the ground (G) test point next to U435.

   d. Trigger on the the external trigger output of the pulse generator.

   e. Position the trace at the graticule center line (reference).

7. Move the oscilloscope probe tip to pin 20 of U448 on the 91A04A master module, and connect the probe ground to TP449 (ground test point).

8. Press START ACQUISITION.

9. Carefully center the rising edge of the clock pulse on the center vertical and horizontals lines of the graticule (see Figure 5-9).

10. Move the P6201 FET probe tip to pin 15 of U448 on the 91A04A master module.

11. Verify that the pulse geometry of the trigger input signal at pin 15 is at least 2.3 ns high and at least 2.3 ns low.

12. Verify that the setup time is $\geqslant$1.1 ns and hold time is $\geqslant$0.7 ns as shown in Figure 5-9.

13. Repeat this procedure (16) for each 91AE04A in the system. This completes the performance check of the 91A04A and 91AE04A system. The test setup may now be dismantled. Turn off the DAS mainframe before removing any modules in order to prevent damage to the modules or the mainframe.

6453 DATA ACQUISITION PROBE PERFORMANCE CHECK

Perform the *P6453 Data Acquisition Probe Function Check* that appears in the *Functional Check* subsection of this *Verification and Adjustments* section.

DESCRIPTION

THIS IS A PAGE PULL AND REPLACE PACKAGE

1. Remove the designated pages from your manual and insert the following page 5-23 and 5-24.

2. Keep this cover sheet in the Change Information section at the back of your manual for a permanent record.

000-2775-00D

Table 5-6
CHANNELS, TEST POINTS, AND OFFSET
ADJUSTMENTS FOR FLUKE 5101B METHOD

CHANNEL	RED CONNECTOR	OSCILLOSCOPE PROBE TIP	ADJUSTMENT (RXXX)
Data 0	U218, pin 1 (top of R203)	U218, pin 1	R201
Data 1	U311, pin 2 (top of R303)	U418, pin 1	R301
Data 2	U411, pin 2 (top of R403)	U518, pin 1	R401
Data 3	U511, pin 2 (top of R503)	U618, pin 1	R501
Clock (91A04A only)	U115, pin 2 (top of R113)	U121, pin 13	R111

5. Perform the following measurements for each channel listed in Table 5-6.

   a. Program the Fluke 5101B to output 15.080 mA, and adjust RXXX for a solid ECL high (approximately 4.1 V) on the oscilloscope with no noise present.

   b. Program the Fluke 5101B to output 14.920 mA, and adjust RXXX for a solid ECL low (approximately 3.3 V) on the oscilloscope with no noise present.

   c. Program the Fluke 5101B to output 15.060 mA, and adjust RXXX for a solid ECL high with very little noise present.

   d. Program the Fluke 5101B to output 14.940 mA, and adjust RXXX for a solid ECL low with very little noise present.

   e. Program the Fluke 5101B to output 15,040 mA, and adjust RXXX for a solid ECL high; some noise may be present.

   f. Program the Fluke 5101B to output 14.960 mA, and adjust RXXX for a solid ECL low; some noise may be present.

ADJUSTING COMPARATOR OFFSETS USING A TEKTRONIX
PG502 250 MHz PULSE GENERATOR AS A SIGNAL SOURCE

This procedure describes an alternate method of adjusting comparator offset levels in a 91A04A or 91AE04A Data Acquisition Module using a Tektronix PG502 250 MHz Pulse Generator as a signal source. Performing this test requires that the P6453 Data Acquisition Probe be kept with the data acquisition module with which it was calibrated.

Test Equipment Required

Table 5-7 lists test equipment required for comparator offset adjustment using a Tektronix PG502 250 MHz Pulse Generator as a signal source. Unless otherwise specified, equivalent test equipment may be used.

Table 5-7
EQUIPMENT REQUIRED FOR THE COMPARATOR OFFSET
ADJUSTMENT USING THE TEKTRONIX PG502

QTY	FUNCTION	RECOMMENDED TYPE
1	logic analyzer mainframe	DAS 9100 Series (no substitute)
1	module extender	DAS Main Extender Board, p/n 670-6748-00 (no substitute)
1	⩾400 MHz oscilloscope	Tektronix 7904 mainframe with a 7A19 vertical amplifier, a 7B10 timebase, and Tektronix P6201 X10 FET probe
1	250 MHz pulse generator	Tektronix PG502 250 MHz Pulse Generator
1	high-speed acquisition test fixture	Tektronix p/n 067-1139-00 (no substitute)
1	5-1/4 inch probe ground cable	Tektronix p/n 175-0848-01

Equipment Setup Procedure

$\{ CAUTION \}$

Do not install or remove any electrical module or sub-ssembly in a DAS mainframe while the power is on. Doing so can cause damage to the module or subassembly.