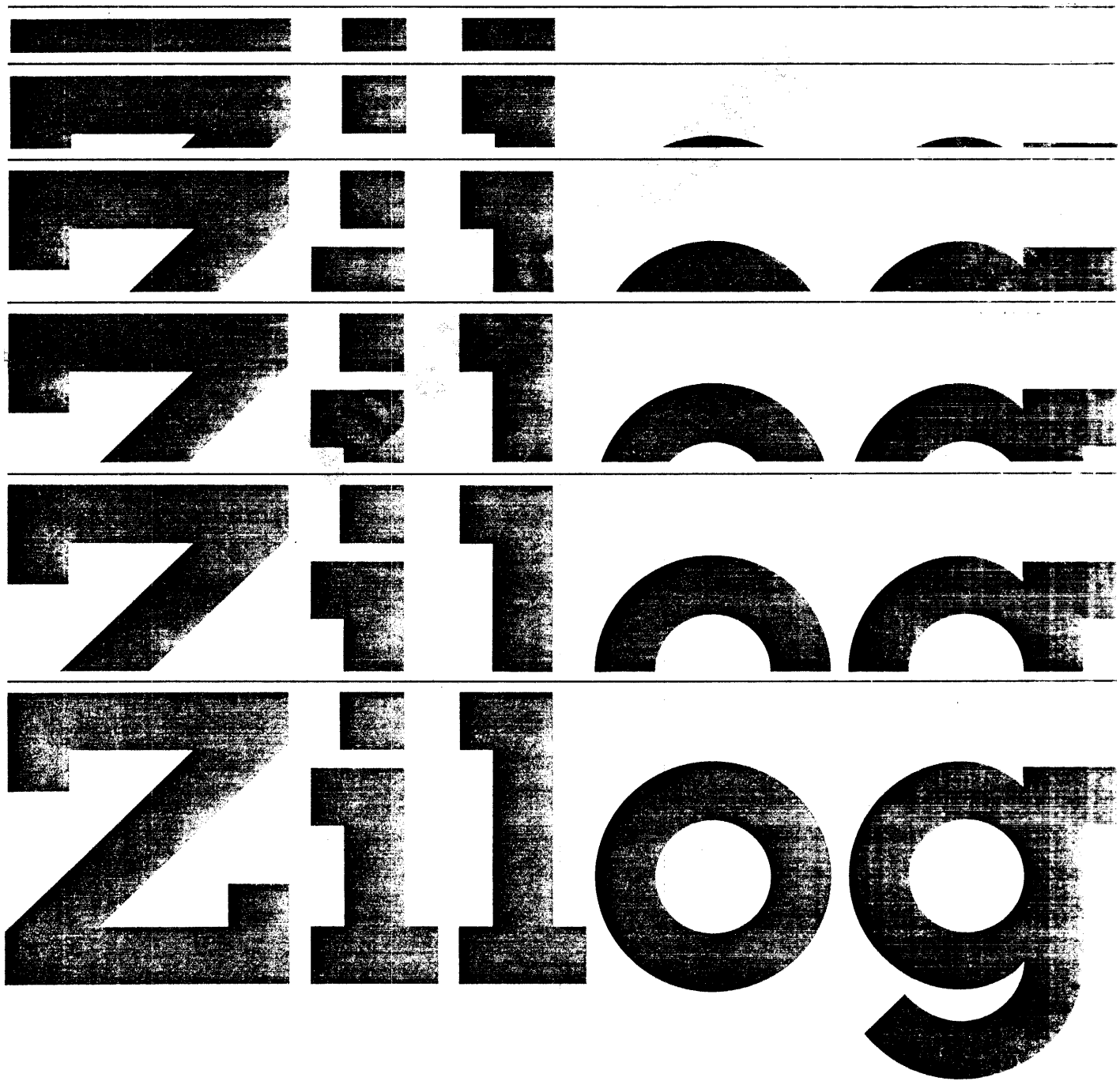
System 8000
Models 21 Plus/31 Plus

Hardware Reference Manual



Ø3-3237-Ø6B

April, 1984

FCC WARNING

This equipment generates and uses radio frequency energy and if not installed and used properly, i.e., in strict accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing or peripheral device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment.

Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

Acceptable operation of this equipment requires the hood of all external interconnect cables be properly grounded to the system to eliminate radio interference.

To insure system integrity, all covers supplied by the factory must remain installed.

Zilog

SYSTEM 8000
HARDWARE REFERENCE MANUAL
MODELS 21 PLUS/31 PLUS
03-3237-06B

This document is an Advance Copy of a manual scheduled for final release during the second quarter 1984. Precaution has been taken to ensure that the information contained in this document is technically correct and up to date.

Some of the information contained in this document will undergo modification and change before the final release of this manual.

SYSTEM 8000 HARDWARE REFERENCE MANUAL

Preface

The System 8000 Hardware Reference Manual for Models 21 Plus/31 Plus provides a functional as well as an operational overview of the standard system configuration.

The intended audience of this manual includes the Field Engineer (FE), service personnel, and the System Administrator.

There are five sections and three appendices contained in the manual as follows:

Section 1 - introduces the standard configuration of the System 8000. System options are listed with a brief description about each option.

Section 2 - provides the specifications and characteristics of the System 8000. I/O interconnections as well as ZBI connections and pin assignments are also included.

Section 3 - provides the step-by-step instructions to install the system, from receipt of the equipment to system power-up and diagnostic.

Section 4 - contains a theory of operation section that provides a high level discussion of the system's operation. Differences between the models are noted within text.

Section 5 - describes a maintenance program (Preventive Maintenance) designed to minimize system degradation. A removal and replacement subsection that pertains to items most likely to be difficult or critical to remove and replace are included.

Appendix A - provides an area to log and record the field upgrades performed to the system.

Appendix B - contains the mnemonics and their interpretation for this manual.

Appendix C - contains a complete listing of possible error conditions for the cartridge tape unit.

Appendix D - contains the Monitor Mode Program for the system.

Appendix E - contains the system SPUD Error List.

This manual and the related manuals listed below provide the technical documentation for the System 8000.

Title	Zilog Part Number
System 8000 ZEUS Administrator Manual	03-3246
System 8000 ZEUS Languages/Programming Tools Manual	03-3249
System 8000 ZEUS Utilities Manual	03-3250
System 8000 ZEUS Reference Manual	03-3255
System 8000 Central Processing Unit (CPU) Hardware Reference Manual	03-3200
System 8000 Winchester Disk Controller (WDC) Hardware Reference Manual	03-3203
System 8000 SADIE Reference Manual	03-3264
System 8000 Site Preparation Manual	03-3271

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SECTION 1
OVERVIEW

1.1. General Description

The Zilog System 8000 Models 21 Plus/31 Plus (Figure 1-1) combine sophisticated software and compact microcomputer hardware for business, scientific, and general purpose applications.

The Zilog System 8000 is a multi-user system, based on the 16-bit segmented Z8001A microprocessor that runs the ZEUS Operating System (Zilog Enhanced UNIX*).

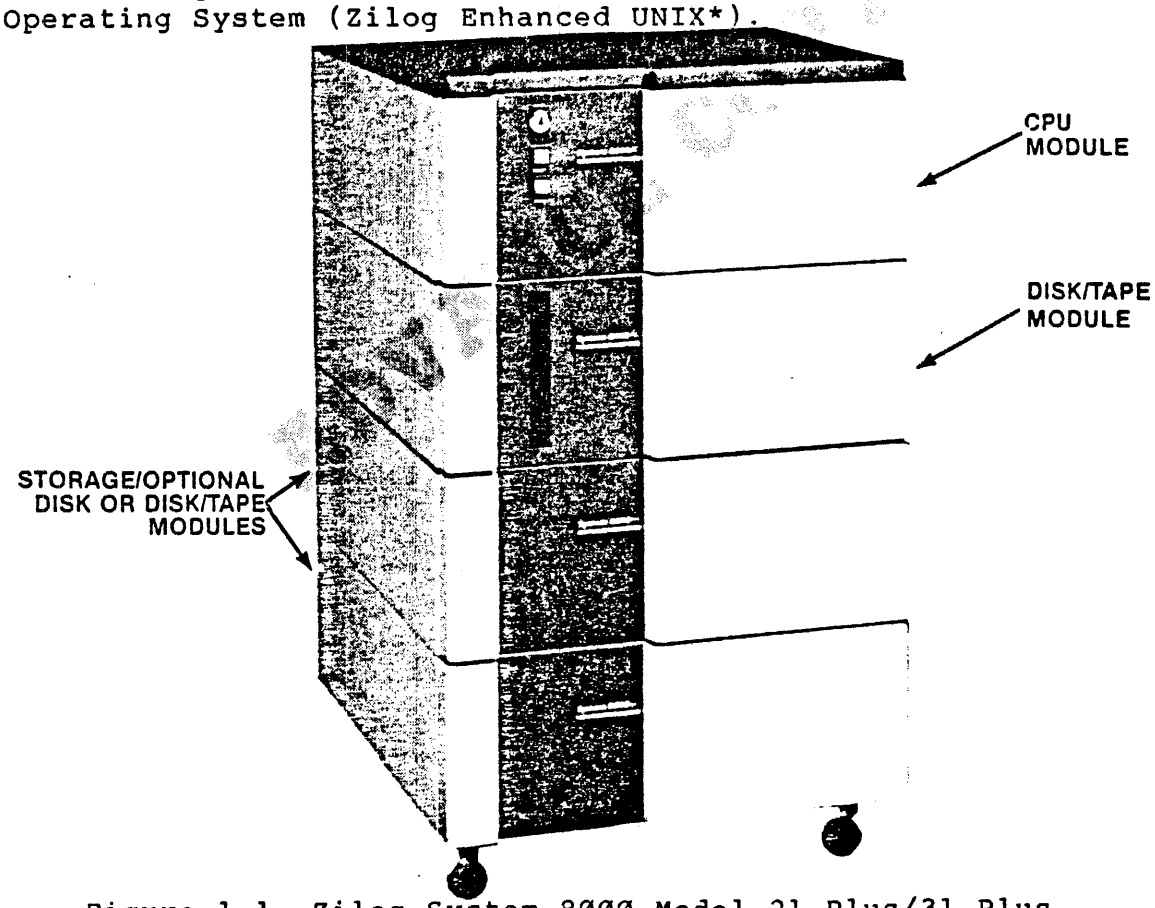

Figure 1-1 Zilog System 8000 Model 21 Plus/31 Plus

* UNIX is a trademark of Bell laboratories. Zilog is licensed by AT&T.

1.2. System Description

The System 8000 Models 21 Plus/31 Plus are similar in their exterior, overall appearance. Both have four integrated, self-contained modules, which are united into one free-standing unit.

Certain unique model configurations are highlighted and referenced to other areas within the text. Reference Section 1.3 of this manual for system options. Model variations are addressed throughout this manual and include the following:

Model 21 Plus - contains a mini Winchester Disk Controller-II (mWDC-II) board that interfaces with a 5-1/4 inch Winchester disk drive (with approximately 52M bytes of drive storage capacity).

Model 31 Plus - contains a Storage Module Device Controller (SMDC) board that interfaces with an 8 inch Storage Module Drive (SMD) (with approximately 168M bytes of drive storage capacity).

The CPU module, the top physical module, is the nucleus of the System 8000. It contains the Central Processing Unit (CPU) board and other system controller boards within its ten-slot card cage. System power is also distributed from the CPU module.

I/O connections, located at the back of the CPU module, provide the I/O links to the lower module(s) for disk, tape, and terminal communication.

The Disk/Tape module, directly beneath the CPU module, contains a disk drive (refer to drive model variations above), and a 17M byte tape cartridge drive. Disk and tape I/O connectors are located at the rear of the I/O panel.

The two Accessory modules, located directly beneath the Disk/Tape module, can have an optional disk or disk/tape drive installed, which interconnects to the above Disk/Tape module.

Terminal distribution panels for additional serial terminal and parallel printer connections can be added to these modules. System options are described in Subsection 1.3. Additional information can be obtained from your Zilog Field Service representative.

The PCBs are horizontally inserted in the ten-slot Printed Circuit Board (PCB) card cage in the CPU module.

The lower two card slots (slots 9 and 1Ø) are dedicated to system memory*. Card slots 7 and 8 can be optionally configured for additional memory boards*. (Refer to System Options, Subsection 1.3.)

Figures 1-2 through 1-8 are photos of most of the PCBs in the system, and have been placed at the end of this chapter for convenience.

The PCBs for the system (memory is optionally selected) are as follows:

- CPU Board
- mini Winchester Disk Controller-II Board (Model 21 Plus)
- Storage Module Device Controller A and B Boards (Model 31 Plus)
- Tape Cartridge Controller Board
- Error Checking and Correction (ECC) Controller Board
- ECC Memory Array Board(s)
- Parity Memory Board(s)

1.3. System Options

The addition of some system options (refer to Appendix A) may require a change in the system software. Reference the ZEUS Administrator Manual or call your Zilog Field Service representative for software configuration information.

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* System Memory can be either the Error Checking and Correction Controller board with its Memory Array board(s), or Parity Memory board(s).

Upgrading the system with additional memory boards will increase the system's physical memory. (This does not include the small bootstrap memory on the CPU board.) Adding options that allow additional memory boards to be inserted into card slots 7 and 8, enhances the system to a four memory board slot configuration.

System options are listed below. Additional information can be obtained by contacting your Zilog Field Service representative.

Options

1. Memory Jumper Board Field Upgrade - TO BE RELEASED -

2. 16 to 24 User Field Upgrade - Installing a Secondary Serial Board in the system enhances the standard 8 user system to a 16 user system. With two Secondary Serial Boards, the system is further upgraded to a 24 user system.

3. Model 31 Plus 168M Byte SMD Field Upgrade - For additional disk storage capacity, up to three 168M byte drives can be added to the system.

4. Model 21 Plus 52M Byte Drive Field Upgrade - TO BE RELEASED -

5. Model 31 Plus 168M Byte Disk/Tape Module Field Upgrade - Installing a 168M byte Disk/Tape module increases disk storage and tape capacity for the system.

6. Model 21 Plus 52M Byte Disk/Tape Module Field Upgrade - TO BE RELEASED -

7. Floating Point Processor Field Upgrade - TO BE RELEASED

8. Nine-Track Subsystem Field Upgrade - Installing a Nine-Track subsystem increases data storage and transfer retrieval capabilities.

9. Cartridge Tape Drive Field Upgrade - One additional cartridge tape drive can be added to the system.

1Ø. Intelligent Communications Processor (ICP) 8/02 Field Upgrade - TO BE RELEASED -

1.4. Functional Description

Figures 1-2 through 1-9 ilustrate most of the PCBs (standard and optional) which configure the system. The PCBs share the Z-Bus Backplane Interconnect (ZBI), which is a high performance, high speed, application oriented, 32-bit, parallel bus (refer to Figure 1-1Ø).

The paragraphs that follow provide an overview of the system functions which communicate over the ZBI bus.

1.4.1. Central Processing Unit (CPU) Board

The CPU is the controlling center of the system (refer to Figure 1-2). It contains sequencing and processing facilities for instruction execution. The CPU initiates and controls transactions on the system bus. As the host, it controls the ZBI and all primary parallel and serial I/O ports.

Eight serial I/O ports and a parallel I/O port are supported by the CPU. Standard serial ports are compatible with RS-232C interface. The parallel ports (with the appropriate jumpers inserted) are compatible with a Centronics or Data Products line printer interface. For more detailed information about the CPU, refer to Section 4.

1.4.2. mini Winchester Disk Controller-II (mWDC-II) Board

The mWDC-II is a 16-bit Z8ØØ1A based 5 1/4-inch disk controller board (Figure 1-3) that interfaces to the host processor as an intelligent slave peripheral device on the ZBI bus. It controls information access to and from the 5 1/4-inch drive.

The mWDC-II uses a Z8065 Burst Error Processor to detect and correct error bursts up to 12 bits in length. A 32-bit ECC code is appended to the ID and DATA fields on all hard disk sectors. Optimum disk utilization is provided with a sector sparing algorithm that maps out defective blocks at format time.

The mWDC-II also provides fast multisector R/W operations (up to six full track per track revolution) made possible with a full track buffer.

The primary functions of the mWDC-II are:

1. Buffering and execution of all secondary mass storage host commands.

2. Supervisory control of the hard disk mass storage sub-system.

3. Management and verification of disk data integrity.

4. 16-bit DMA transfers between main memory and local buffer over the 8M byte address range at the full bandwidth of the ZBI.

The main features of the mWDC-II are:

1. 16-bit, Z8001 based, Intelligent mini Winchester Disk Controller-II.

2. Standard storage of the system 5 1/4-inch drive(s).

3. 32-bit ECC processor can detect and correct error bursts of up to 12 bits.

4. Fast multisector read/write operations (maximum of 17 physically contiguous sectors/track revolution).

5. Sector sparing format algorithm optimized disk utilization.

6. Supports up to four 5 1/4-inch drive(s).

7. Supports overlapped seeks in multi-disk system configurations???.

8. Flexible "command packet buffer" message based host interface facilities with simple and powerful host/controller communications. ????

9. The mWDC-II provides a 16-bit block transfer at full bus bandwidth. ????.

For more detailed information about the mWDC, refer to Section 4. A specifications and characteristics table for the WDC is provided in Section 2.

1.4.3. Storage Module Device Controller (SMDC) Boards

The SMDC is a high performance controller for the Model 31 Plus, that links the ZBI system bus to the Storage Module Device.

The SMDC consists of two boards, SMDC A and SMDC B hereinafter referred to as the A board and the B board (refer to Figures 1-3 and 1-4).

The A board connects to the ZBI at the 96-pin board connector P1, and the daisy-chain cable at P2. The A and B boards are joined together by a cable that connects to JB on the A boad, and JA on the board B.

The B boad can connect to as many as four cables. All drive connections are through the P2 backplane connector.

Bit slice processor and sequencer logic control all the operations of the SMDC.

SMDC features include:

- Packet control
- Overlapped seeks
- Automatic error recovery
- Data buffering
- Flagged sectors
- Long writes and reads
- Self-test on power-up or system initialization

The SMDC can be interrupt driven (factory default configuration), or it can operate in the polled mode to the host when a packet is complete. For more information about SMDC, refer to Section 4. A specifications and characteristics table for the 168M byte drive is provided in Section 2, Table 2-4.

1.4.4. Tape Cartridge Controller (TCC) Board

The TCC is the intelligent interface between the CPU and the tape cartridge drive (refer to Figure 1-5).

A Zilog Z8ØB microprocessor controls the operation of the controller. The controller uses Direct Memory Access (DMA) to transfer data between the TCC drive and the CPU.

When the CPU wants to initiate an operation, it sends a command to the controller. The controller completes the operation and interrupts the CPU to notify it that the operation is complete. For more detailed information about the TCC refer to Section 4.

1.4.5. Memory Subsystem

The Memory Subsystem for the System 8ØØØ (refer to Figures 1-6 through 1-8) can include:

- Error Checking and Correcting (ECC) Controller (Board)
- ECC Memory Array (Board)
- Parity Memory (Board)

1.4.5.1 ECC Controller Board: The ECC Controller can control the operation of up to ???4M bytes ???of dynamic read/write memory. Data can be transferred as bytes (8 bits), words (16 bits), and long words (32 bits). The controller translates the width of the data and places the data in the proper locations.

The controller uses a logging system that counts soft errors in each 64K byte block of memory. The controller transparently corrects all single bit errors (soft) and detects all double bit errors (hard). A high speed 32-bit bus connects the Memory Array board to the ECC Controller board.

During memory transactions, all data passes through the memory controller.

1.4.5.2 ECC 1M Byte Memory Array Board: The ECC Memory Array board has data storage space and additional storage for the check bits used by the error checking and correcting logic.

1.4.5.3 Parity Memory Board: Parity Memory supplies up to 512K bytes per board of dynamic Random Access Memory. The board is designed to separate the memory array into two banks. One bank is refreshed transparently while the other is acessed.

The memory is functionally designed to be accessed in byte or 16-bit words from the ZBI. Associated with every byte is a parity bit which is written to on write operations, and read out for consistency checks during read operations.

For more detailed explanations about the Memory Subsystem, refer to Section 4.

1.4.6. Secondary Serial Board (SSB)

The SSB boards can expand the I/O terminal distribution from the standard 8 user system to a 16 user system, or from 16 to a 24 user system (refer to System Options in Section 1.3).

Each SSB provides eight Input/Output (I/O) asynchronous full duplex serial channels for terminal distribution to TTYs 8 - 15 or 16 - 23. Each SSB also provides a Centronics (factory default) or Data Products parallel printer port.

The SSBs are connected to the system backplane through connector P2, and supplement the serial and parallel I/O on the CPU board.

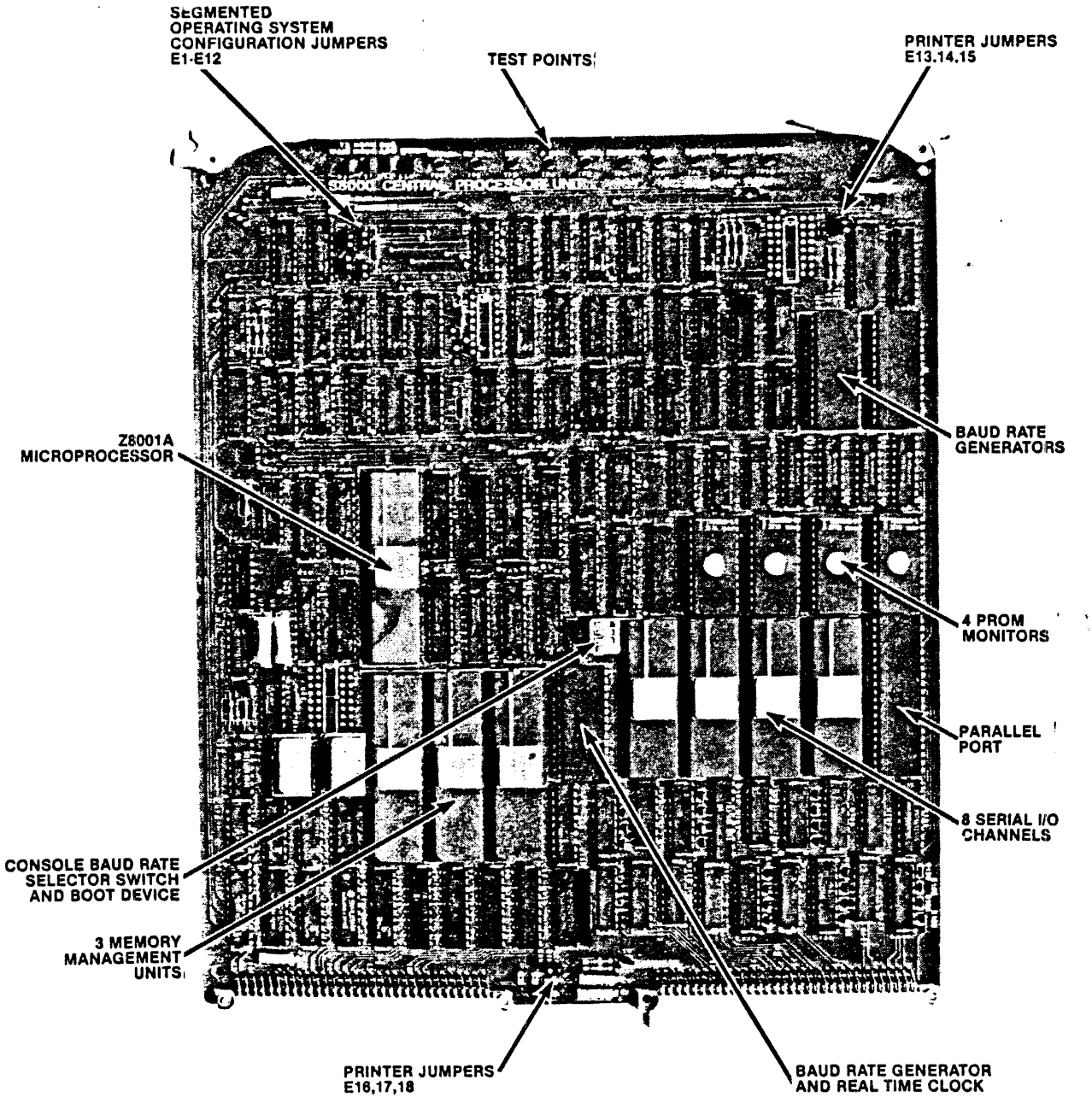


Figure 1-2 Central Processing Unit Board

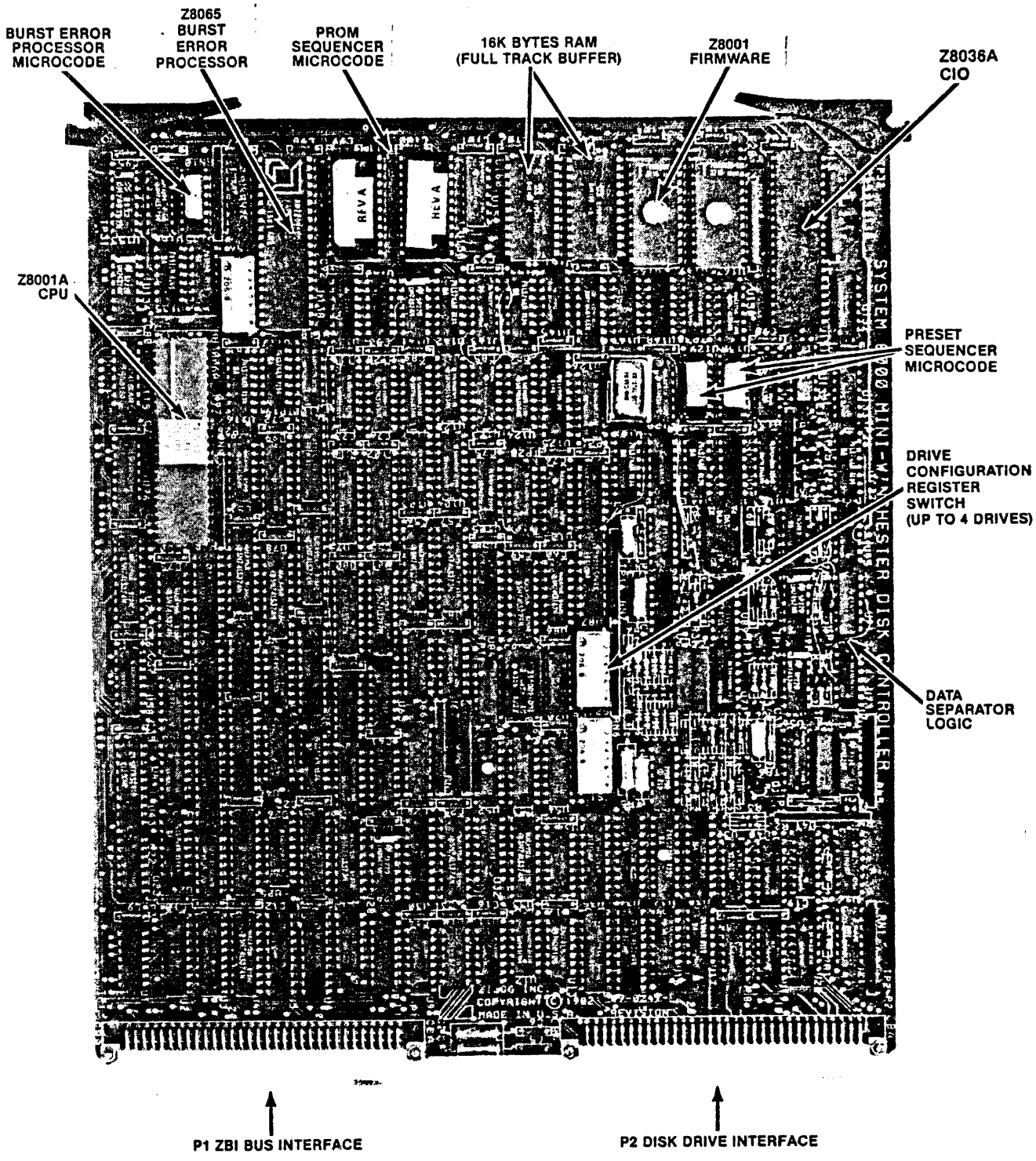


Figure 1-3 Model 21 Plus mini Winchester Disk Controller-II

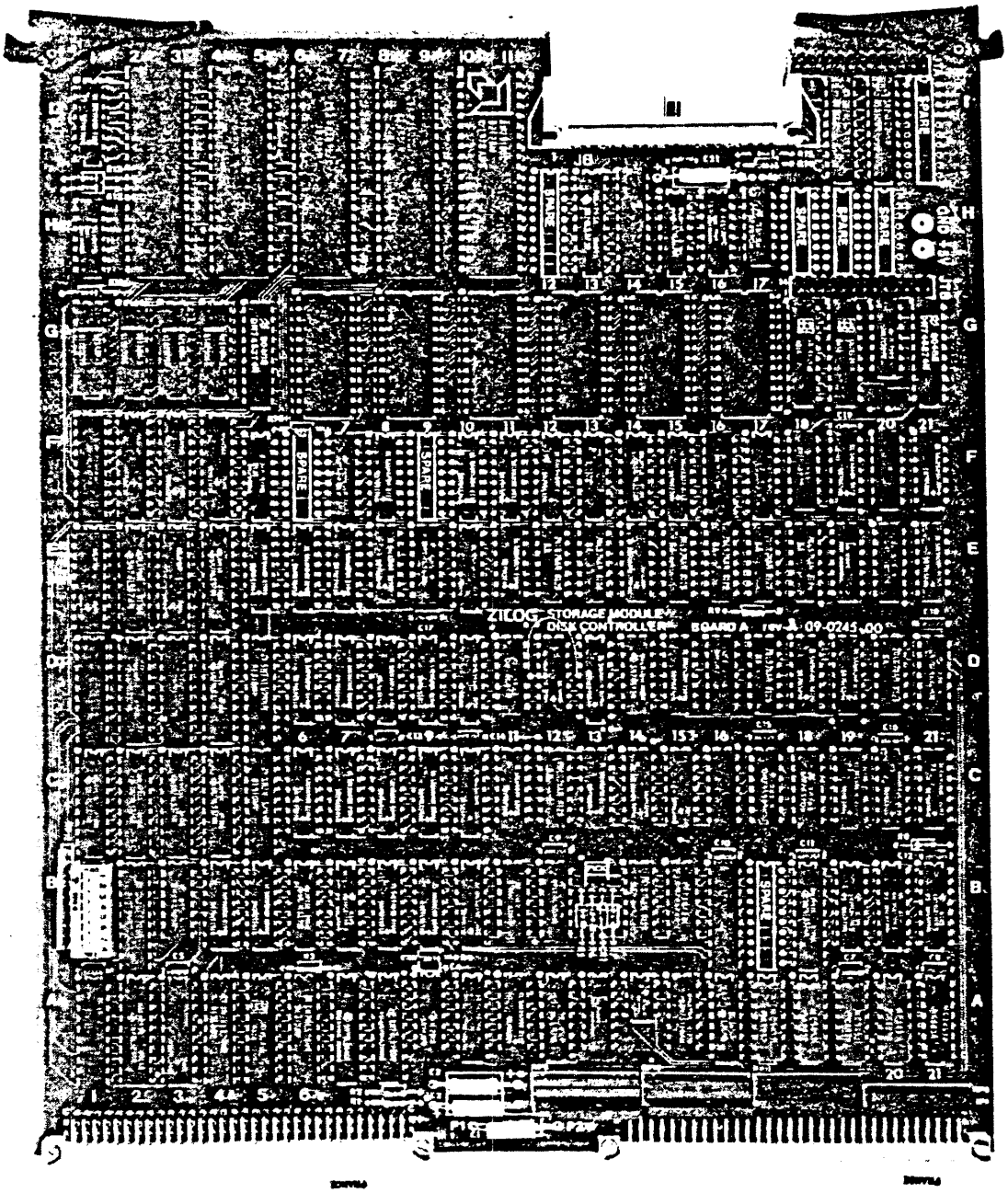


Figure 1-4 Model 31 Plus Storage Module Device Controller A

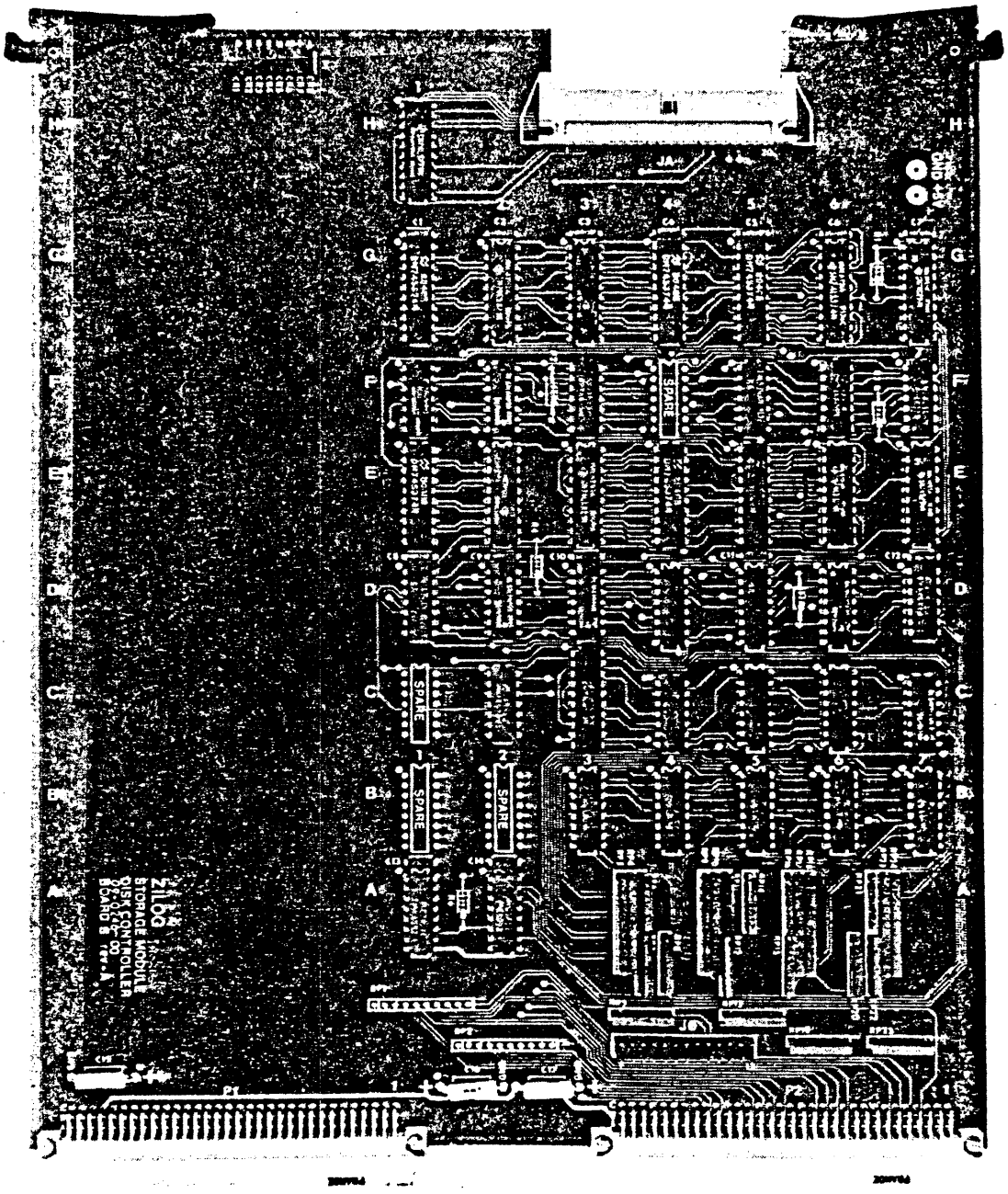


Figure 1-5 Model 31 Plus Storage Module Device Controller B

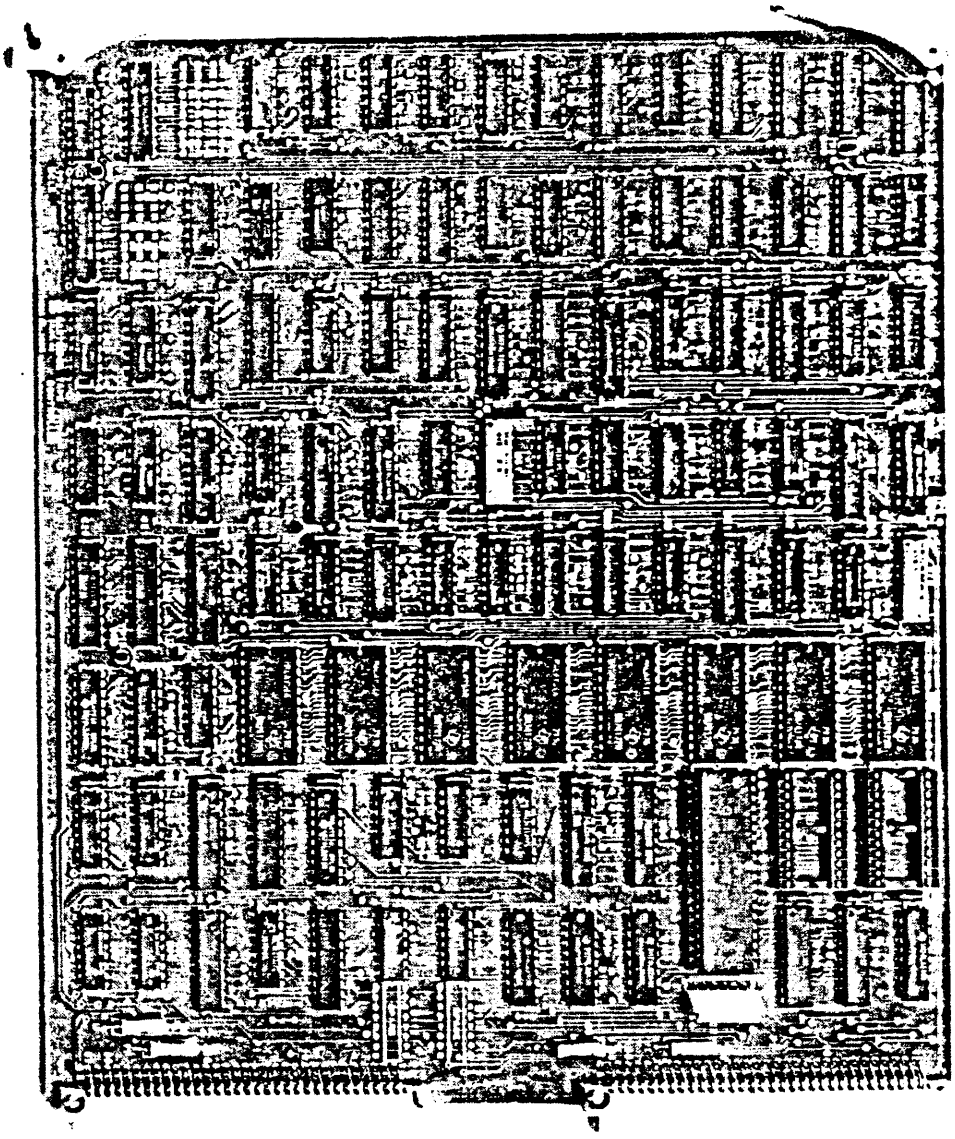


Figure 1-6 Tape Cartridge Controller

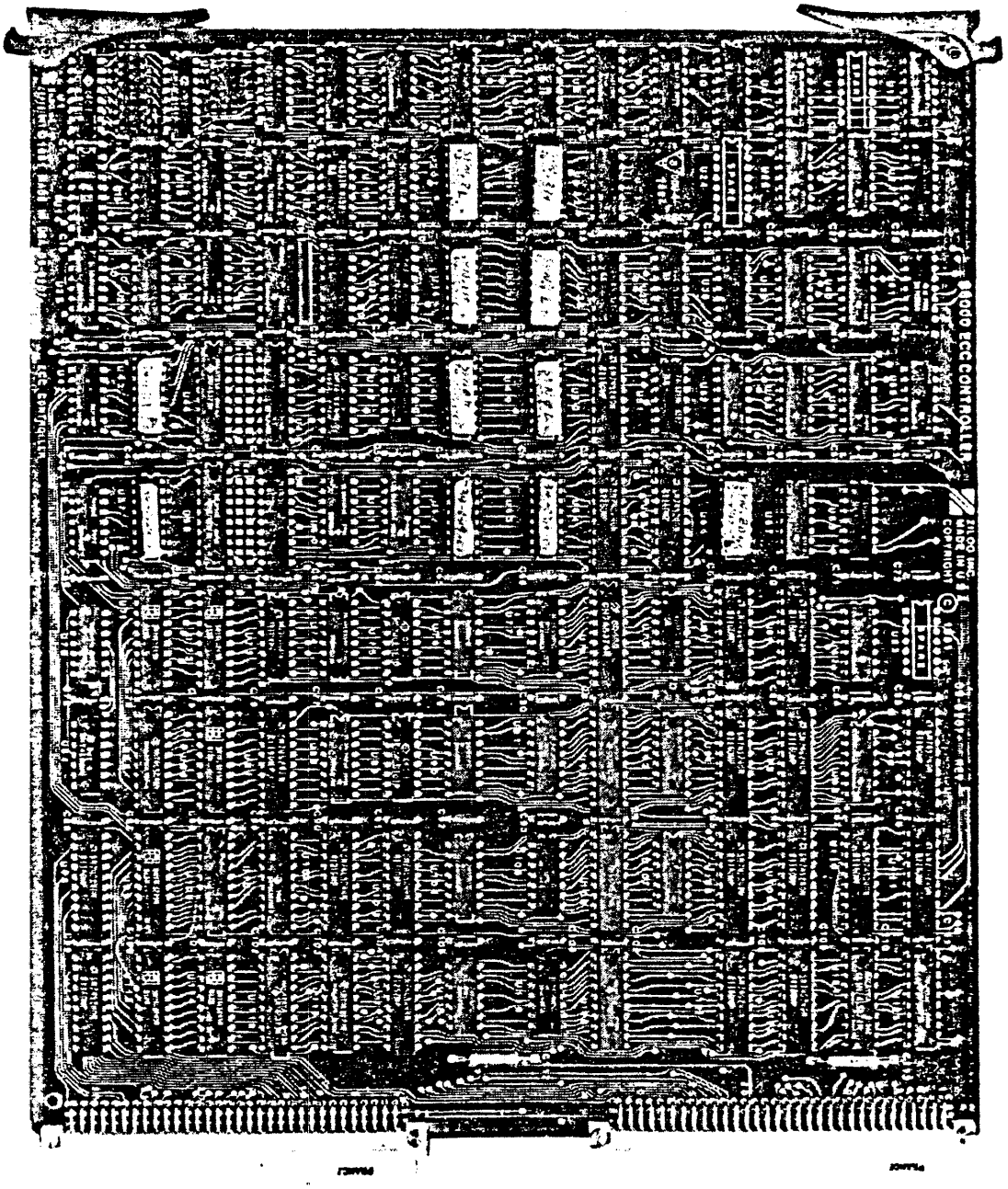


Figure 1-7 Error Checking and Correction Controller

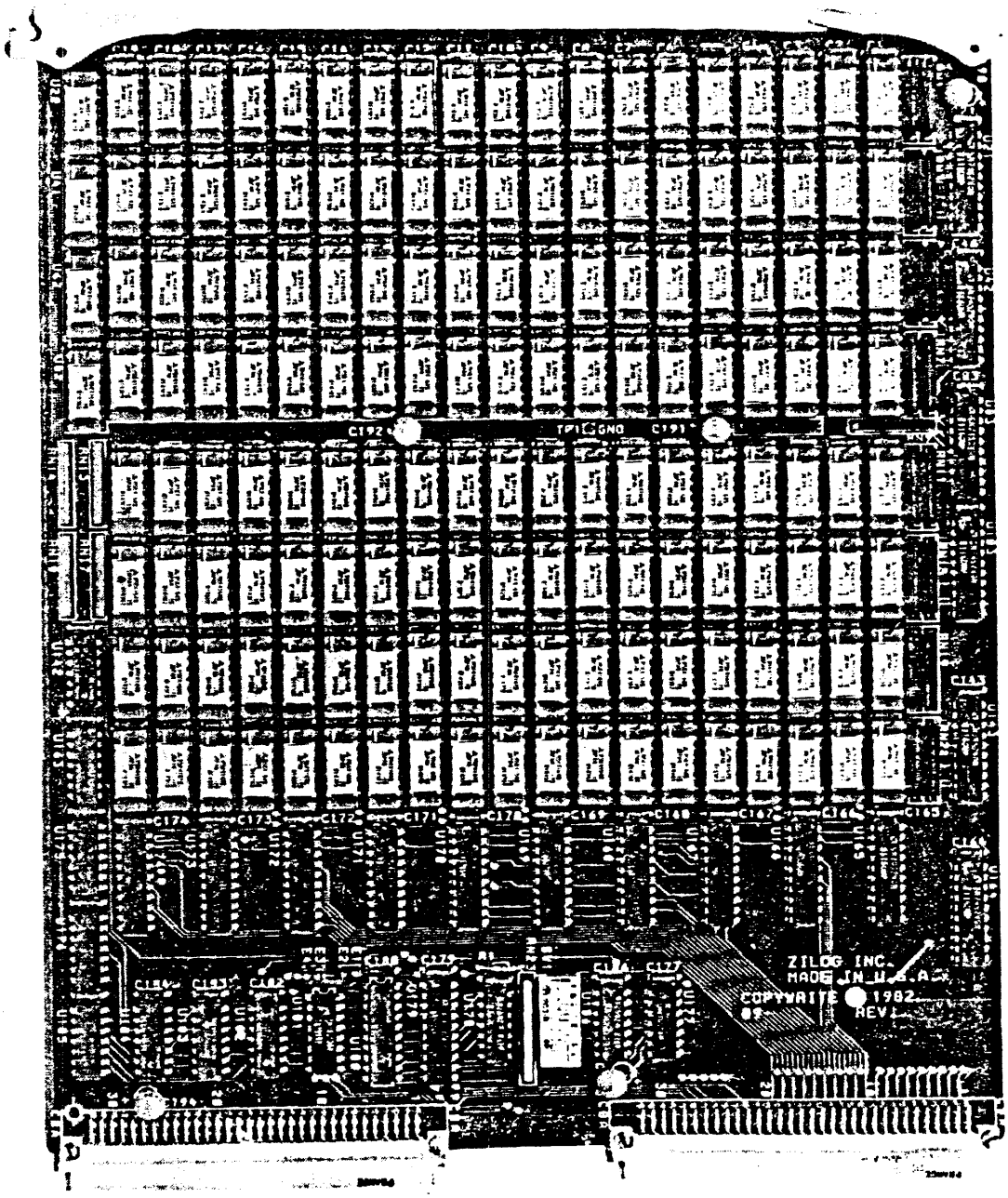


Figure 1-8 ECC 1M Byte Memory Array Board

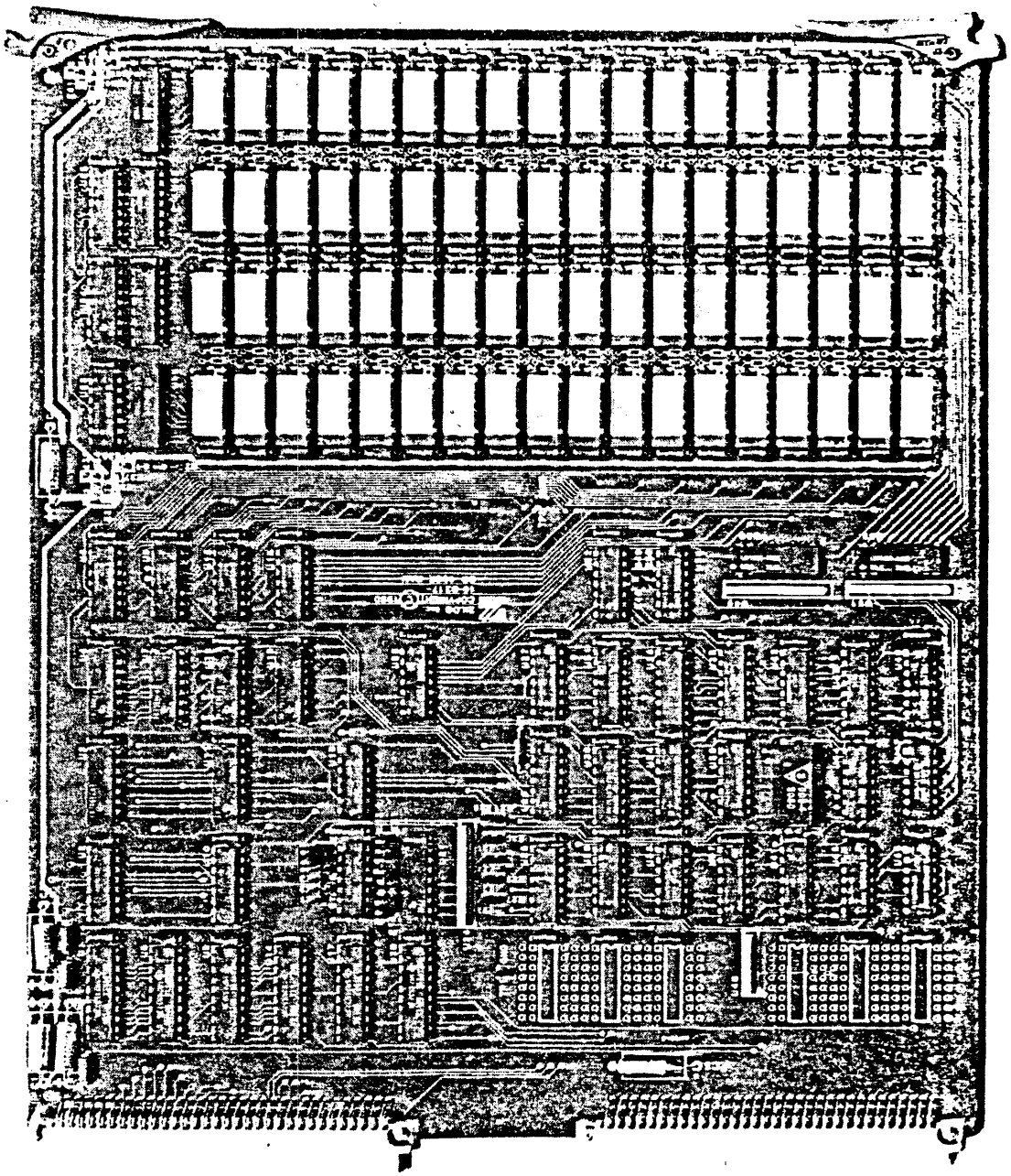


Figure 1-9 Parity Memory Board

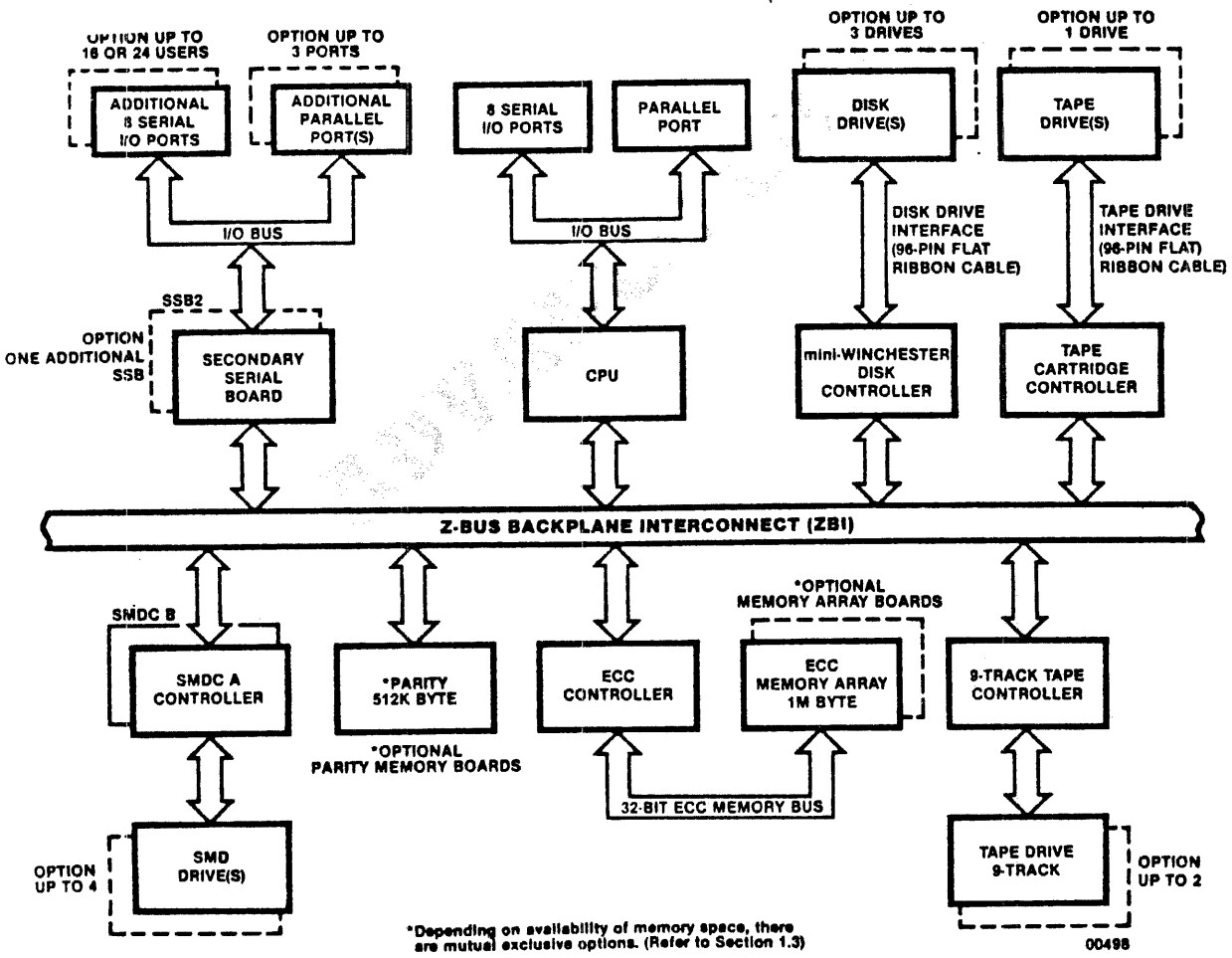


Figure 1-10 System 8000 Z-Bus Interconnections

SECTION 2
SYSTEM SPECIFICATIONS

2.1. Overview

This section provides the electrical, physical, and environmental specifications for a standard Zilog System 8000*. I/O connections for peripheral devices, as well as ZBI backplane pin assignments for the printed circuit boards contained within the standard system are also included.

2.2. System 8000 Specifications and Characteristics

Electrical and power specifications for the standard Zilog System 8000 are provided in Table 2-1. Ac input voltages are for single phase, at 50/60 Hertz.

NOTE

Optional add-ons may change the standard requirements listed in Table 2-1 below. Direct any questions about current loads for options and add-ons to Zilog Field Service.

Table 2-1 Standard System Electrical/Power Specifications

	NOMINAL LINE VOLTAGE	SYSTEM CURRENT (SUSTAINED APPROXIMATE)	CURRENT (SURGE) (EACH)
USA	115 Vac ±12%	5.6A max.	10A max.
Japan	100 Vac ±12%	6.8A max.	10A max.
Europe	220 Vac ±12%	3.0A max.	5A max.
UK	240 Vac ±12%	3.0A max.	5A max.

* The standard System 8000 as defined within this manual represents four stacked modules consisting of a CPU module, a Disk/Tape module with one disk drive, and two Accessory modules.

2.3. Zilog System 8000 Modules

In a basic stand-alone configuration, the system modules are stacked into one free-standing unit (refer to Figure 1-1).

Each system module can be separately rack mounted, with its side panels removed, in a standard 19-inch horizontal rack. Questions about system configurations should be directed to Zilog Field Service.

Dimensions of each system module, with its side panels removed, are shown in Figure 2-1.

Floor clearance for the standard system configuration is provided in Table 2-2. Refer to the System 8000 Site Preparation Manual for additional (floor clearance) information.

Table 2-2 System Module Clearance

SYSTEM CABINET/RACK	CABINET/RACK DIMENSIONS
Front/Rear Clearance:	30 inches (76.2 cm) from cabinet
Side Clearance:	24 inches (60.96 cm) from cabinet

The standard specifications and characteristics for the Zilog System 8000 are listed in Table 2-3.

Standard specifications and characteristics for the 52M byte Winchester disk drive (Model 21 Plus) and the 168M byte SMD disk drive (Model 31 Plus) are provided in Tables 2-4 and 2-5.

The tape cartridge drive specifications and characteristics are listed in Table 2-6.

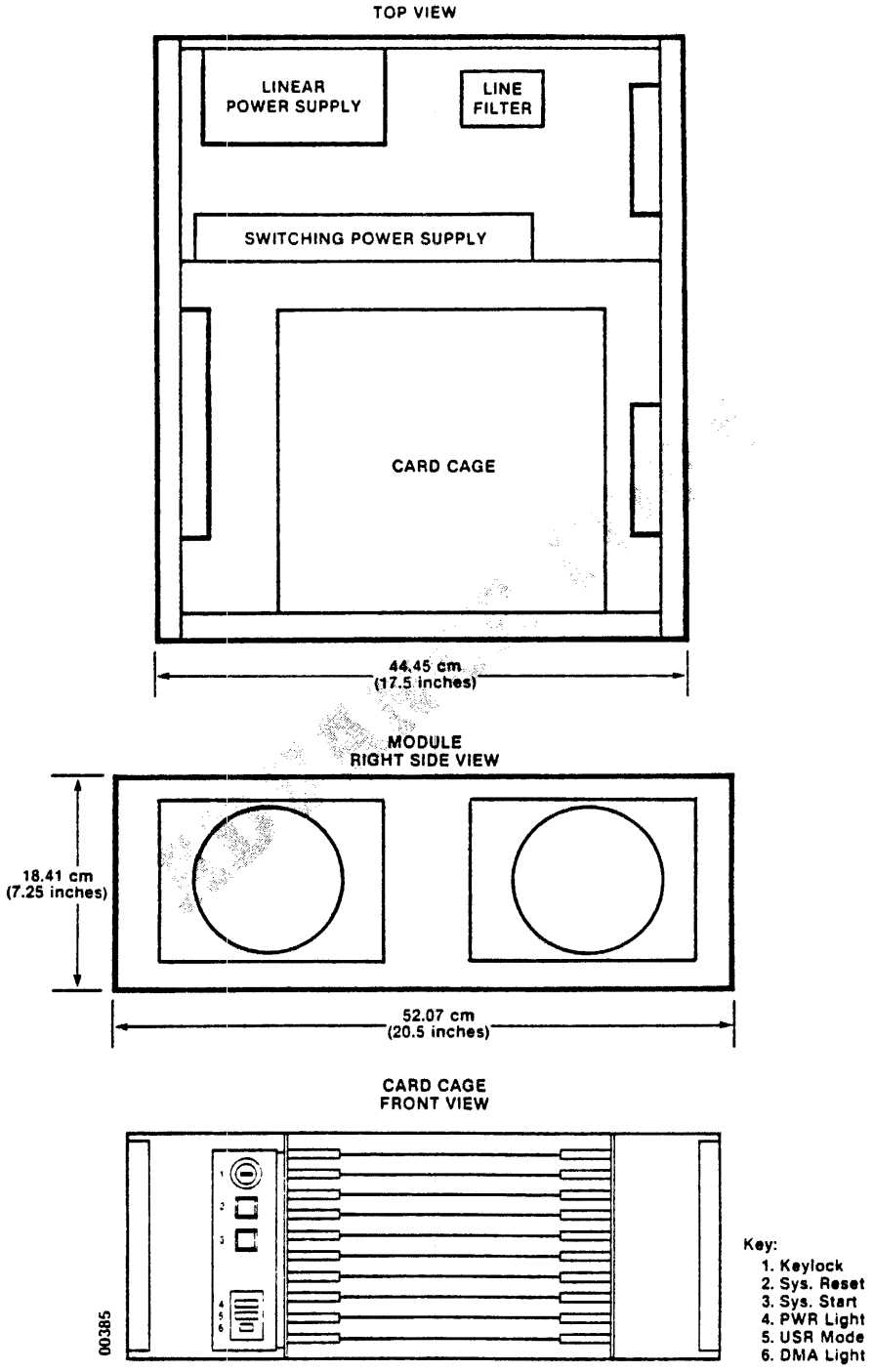


Figure 2-1 System Module Dimensions

Table 2-3 Standard Zilog System 8000 Specifications And Characteristics

SYSTEM OPERATION	SYSTEM SPECIFICATIONS
Processor:	Segmented 48-pin Z8001A CPU
CPU Clock Frequency:	5.5 MHz
Input/Output:	Up to 24 RS-232C compatible serial I/O ports and three parallel printer ports (factory set for Centronics Interface).
Baud Rate:	110 to 19,200 baud (optionally set by software).
System Controls and Indicators:	System panel has cutouts for key-lock ON/OFF, RESET, and START switches. Translucent panel indicators are lit by three indicator lamps: POWER (+5V dc), USER (CPU is in normal state), and Direct Memory Access (DMA) (CPU relinquishes the bus to DMA devices).
I/O Interconnect	Up to eight 96-pin I/O Panels: panel connectors interface the module to other Disk/Tape module I/O panels and terminal distribution panels. Each terminal distribution panel has eight DB255 25-pin user terminal connections and one 25-pin printer port. (TTY1 is labeled "console" for the System Administrator.)
SYSTEM ENVIRONMENT	CHARACTERISTICS
Operating Temperature Range:	59 degrees F (15 degrees C) minimum 104 degrees F (40 degrees C) maximum
Relative Humidity:	80% non-condensing

(continued)

Table 2-3 Standard Zilog System 8000
Specifications And Characteristics
(continued)

SYSTEM STACK/MODULE	CHARACTERISTICS
Modular Stack:	Height: 33 inches (84 cm) Width: 19 inches (48 cm) Depth: 24 inches (61 cm)
Rack Mount:	Height: 5 feet 8.5 inches (174 cm) Width: 22.3 inches (56.7 cm) Depth: 31.5 inches (70.9 cm)
Modular Stack:	Approximately 250 pounds (114 kg)
Rack Mount:	Approximately 400 pounds (182 kg)
CPU module:	Approximately 65 pounds (28.2 kg)
Model 21 Plus Disk/Tape module:	Approximately 59 pounds (26.8 kg)
Model 31 Plus Disk/Tape module:	Approximately 75 pounds (34.1 kg)
Model 21 Plus Disk module:	Approximately 55 pounds (25.0 kg)
Model 31 Plus Disk module:	Approximately 71 pounds (32.2 kg)
Empty module:	Approximately 18 pounds (8.2 kg)
Nine-Track module:	Approximately 100 pounds (45.5 kg)

Table 2-4 52M Byte Drive Specifications and Characteristics
(Model 21 Plus)

DRIVE	CHARACTERISTIC
Storage Capacity (Formatted):	84,660,000 bytes
Number of Cylinders:	830
Number of Sectors:	
Cylinder Capacity (Formatted):	
Tracks per Cylinder:	
Track Capacity (Formatted):	
Average Latency:	
Positioning Time	To be supplied
Track to Track:	
Average Seek:	
Maximum Seek:	
Rotational Speed:	
Start/Stop Time:	
Data Transfer Rate:	
Encoding Method:	
Interface Data:	
Interface:	
Recording Density:	
Track Density:	960 tracks per inch (tpi)

Table 2-5 168M Byte Drive Specifications and Characteristics (Model 31 Plus)

DRIVE	CHARACTERISTIC
Storage Capacity (Formatted):	134,217,728 bytes
Number of Cylinders:	1024
Number of Sectors:	32 active, 1 spare
Cylinder Capacity (Formatted):	131,072 bytes
Tracks per Cylinder:	8
Track Capacity (Formatted):	16,384 bytes
Average Latency:	8.55 ms
Positioning Time	
Track to Track:	5 ms
Average:	20 ms
Maximum:	40 ms
Rotational Speed:	3510 RPM ±1%
Start/Stop Time:	<35/ <25 sec
Data Transfer Rate:	1.198K byte/sec
Encoding Method:	MFM
Interface Data:	NRZ
Interface:	SMD
Recording Density:	9420 bits per inch (bpi)
Track Density:	960 tracks per inch (tpi)

Table 2-6 Tape Cartridge Drive Specifications and Characteristics

DRIVE	CHARACTERISTIC
Storage Capacity:	17.2M bytes max per 450 feet of tape
Read/Write Speed:	30 inches per second (ips)
Rewind/Search Speed:	90 inches per second (ips)
Tracks:	4
Recording Density:	6400 bits per inch (bpi) MFM
Data Transfer Rate:	192,000 bits per sec
Error Rates:	<1 Error in 10^8 bits

2.4. Input/Output Connectors

Figures 2-2 and 2-3 identify the CPU module 96-pin terminal, disk or SMD, tape, and optional connectors which are located on the system I/O panels.

The two connector panels are cabled to the I/O and terminal distribution panels on the Disk/Tape and Accessory modules. The terminal distribution panel is located at the rear of the Disk/Tape module (this panel may be located elsewhere in different system configurations). Table 2-7 provides the I/O mating cable connectors and sources by vendor and part numbers.

Table 2-8 contains the pin assignments of the (serial) TTY - I/O connectors for 7-wire and 3-wire configuration.

Table 2-9 contains the pin assignments of the parallel printer connectors.

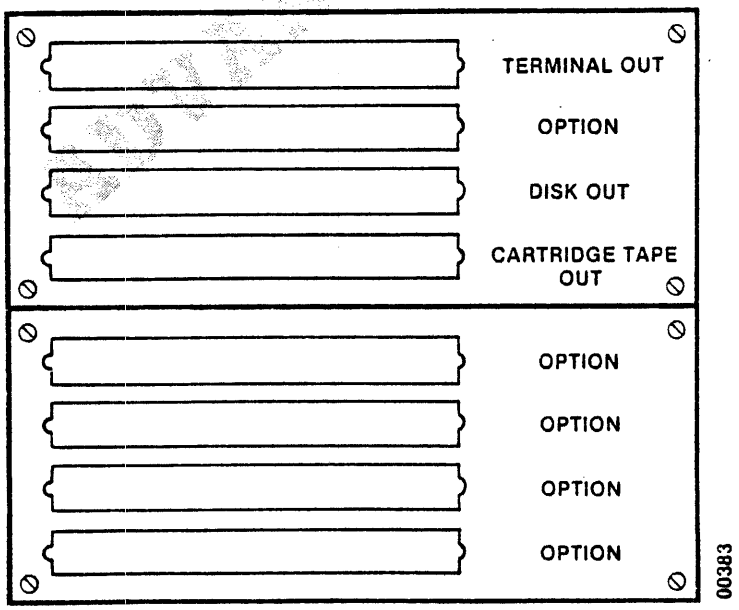


Figure 2-2 Model 21 Plus CPU Module I/O Connector Panel

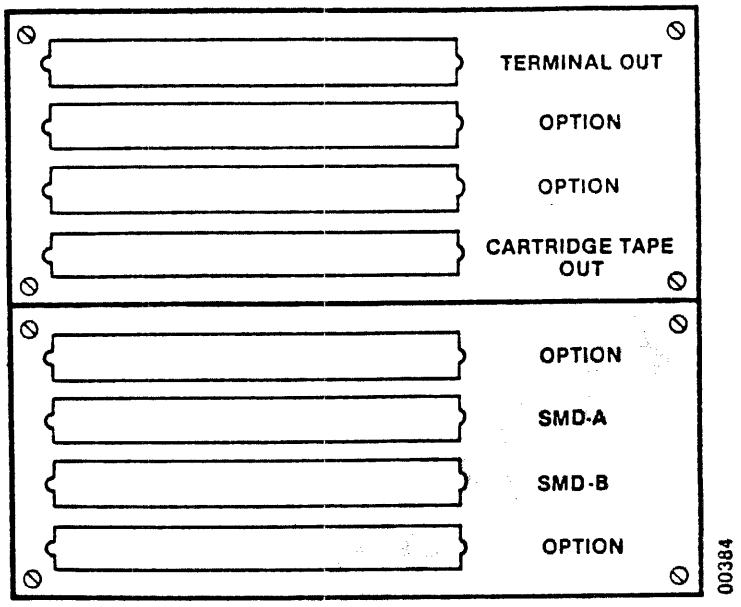


Figure 2-3 Model 31 Plus CPU Module I/O Connector Panel

Table 2-7 Input/Output Cable Connectors

DESIGNATION	DESCRIPTION	VENDOR/PART NUMBER
Printer	25-pin D Connector	AMP745Ø17-6
TTYØ-TTY7	25-pin D Connector	AMP745Ø17-6
Terminal Expansion Cable	96-pin Din Connector (both ends)	Zilog Cable P/N 59-Ø217
Disk Drive Cable	96-pin Din Connector (both ends)	Zilog Cable P/N 59-Ø29Ø
Tape Drive Cable	96-pin Din Connector (both ends)	Zilog Cable P/N 59-Ø217

Table 2-8 TTY Connector and Pin Assignments

SIGNAL NAME	7-WIRE CONFIG PIN	SIGNAL NAME	3-WIRE CONFIG PIN
TD	2	TD	2
RD	3	RD	3
RTS	4	RTS	4*
CTS	5	CTS	5*
DSR	6	DSR	6*
SG	7	SG	7
DTR	20	DTR	20*

* Pins 4 and 5, 6 and 20 are tied together for the 3-wire configuration (terminal and system connectors).

LEGEND

TD	=	Transmitted Data
RD	=	Received Data
RTS	=	Request to Send
CTS	=	Clear to Send
DSR	=	Data Set Ready
SG	=	Signal Ground
DTR	=	Data Terminal Ready

NOTE

Table 2-9 Parallel Printer and Connector, Pin Assignments are located on the following page. A listing of ZBI I/O Connectors and Pin Assignments starts on page 2-13.

Table 2-9 Parallel Printer and Connector, Pin Assignments

CENTRONICS INTERFACE			
SIGNAL NAME	P2 BACKPLANE	PRINTER PORT CONNECTOR PINS	PRINTER CONNECTOR PINS
DATA Ø	P2-1C	1	2
DATA 1	P2-2C	2	3
DATA 2	P2-3C	3	4
DATA 3	P2-5C	4	5
DATA 4	P2-6C	5	6
DATA 5	P2-8C	6	7
DATA 6	P2-9C	7	8
DATA 7	Not Used	Not Used	Not Used
DATA STROBE	P2-12C	9	1
INPUT PRIME	Not Used	Not Used	Not Used
ACKNOWLEDGE	P2-16C	11	1Ø
FAULT	P2-2ØC	12	32
GROUND	P2-32C	18	24
GROUND	P2-32B	19	25
GROUND	P2-32A	2Ø	26
BUSY	P2-17C	23	11
SELECT	P2-21C	24	13

DATA PRODUCTS INTERFACE			
SIGNAL NAME	P2 BACKPLANE	PRINTER PORT CONNECTOR PINS	PRINTER CONNECTOR PINS
DATA Ø	P2-1C	1	B
DATA 1	P2-2C	2	F
DATA 2	P2-3C	3	L
DATA 3	P2-5C	4	R
DATA 4	P2-6C	5	V
DATA 5	P2-8C	6	Z
DATA 6	P2-9C	7	n
DATA 7	Not Used	Not Used	Not Used
DATA STROBE	P2-12C	9	j
INPUT PRIME	Not Used	Not Used	Not Used
DATA DEMAND	P2-16C	11	E
INVALID	P2-2ØC	12	C
READY	P2-17C	23	cc
ONLINE	P2-21C	24	y
SIGNAL GROUND	P2-19C	22	X

2.5. ZBI I/O Backplane Connectors and Pin Assignments

Figure 2-4 for Model 21 Plus and Figure 2-5 for Model 31 Plus provide the CPU PCB I/O backplane slot assignments for the system.

The 96-pin connectors designated J11 through J20 (on the right side P1 of the backplane) are ZBI system bus connections. The 96-pin connectors designated J21 through J30 (on the left side, P2 of the backplane) are auxiliary connectors.

Connectors (for both system models) J22, J23, J27, and J28 are labeled optional and allow for upgraded system configurations.

Pin assignments of all ZBI connectors are the same. Pin assignments for the ZBI backplane connector are listed in Table 2-10.

Table 2-11 through 2-17 contain pin assignments for PCBs installed in backplane connectors P2/J21 through P2/J30 as follows:

Table 2-11, Connector J21, CPU Board

Table 2-12, Connector J22, Secondary Serial Board

Table 2-13, Connector J23, mini Winchester Disk Controller-II Board (Model 21 Plus)

Table 2-14, Connector J24, Tape Cartridge Controller Board

Table 2-15, Connector J26, Storage Module Device Controller A (Model 31 Plus)

Table 2-16, Connector J27, Storage Module Device Controller B (Model 31 Plus)

Table 2-17, Connectors J28 through J30 are dedicated for the Memory Bus (Memory Subsystem Controller and Memory boards).

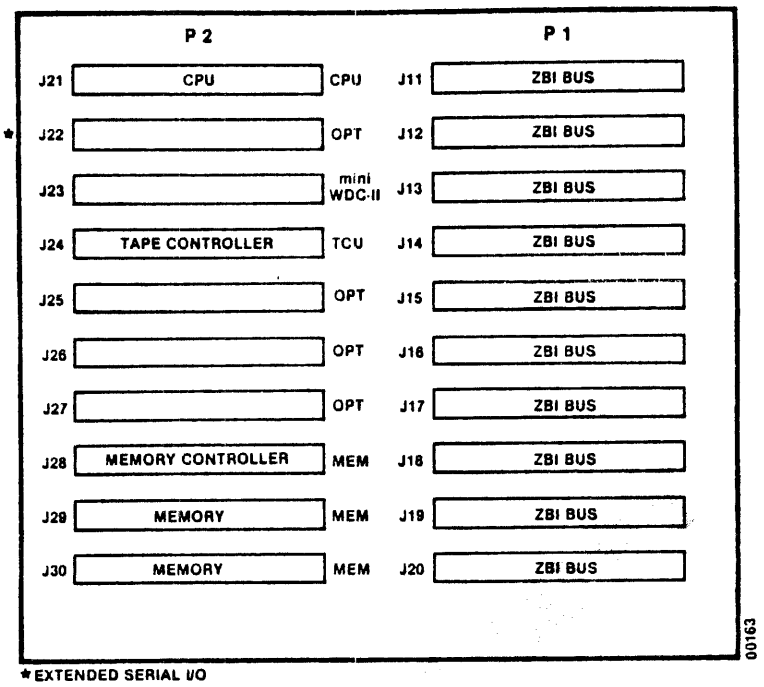


Figure 2-4 Model 21 Plus Backplane Slot Assignments for CPU Module PCBs

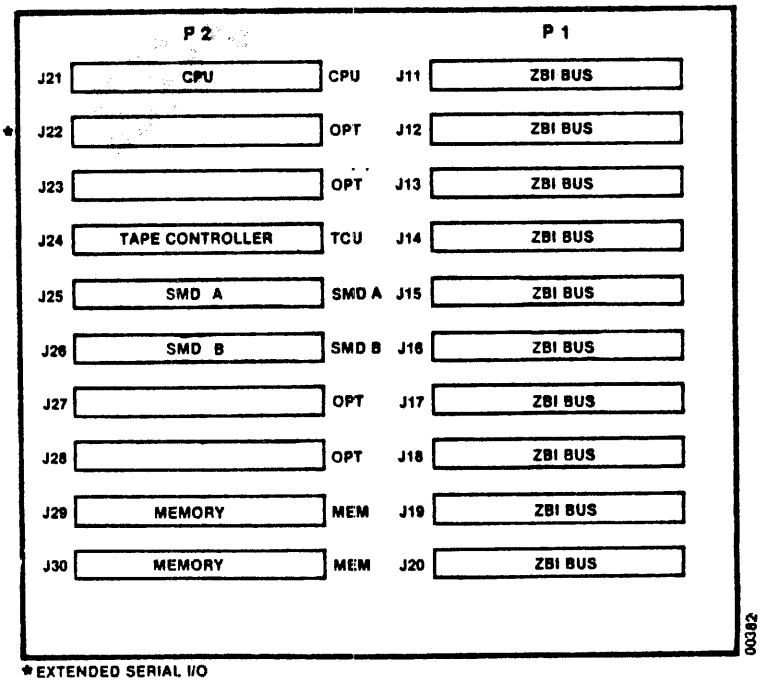


Figure 2-5 Model 31 Plus Backplane Slot Assignments for CPU Module PCBs

Table 2-10 ZBI Backplane Connector Pin Assignments (J11 through J20)

PIN	ROW A SIGNAL	ROW B SIGNAL	ROW C SIGNAL
1	RESET\	WAIT\	CAVAIL
2	CAI\	CAO\	CPUREQ\
3	BAI\	BAO\	BUSREQ\
4	MMAI\	MMAO\	GND
5	IEI3	IEO3	MMREQ\
6	IEI2	IEO2	-
7	IEI1	IEO1	GND
8	INT1\	INT2\	INT3\
9	R/W\	B/W\	W/LW\
10	S2	S3	S4
11	S0	S1	GND
12	ME\	AS\	DS\
13	-	STOP\	N/S\
14	-	-	-
15	AD31	-	GND
16	AD28	AD29	AD30
17	AD25	AD26	AD27
18	AD22	AD23	AD24
19	AD20	AD21	GND
20	AD17	AD18	AD19
21	AD14	AD15	AD16
22	AD11	AD12	AD13
23	AD9	AD10	GND
24	AD6	AD7	AD8
25	AD3	AD4	AD5
26	AD0	AD1	AD2
27	PWRBAD\	MCLK	BLCK
28	+5V	+5V	+5V
29	-5V	-5V	-5V
30	+12V	+12V	+12V
31	-12V	-12V	-12V
32	GND	GND	GND

* -12V is allocated space on the ZBI backplane, but is not used or generated by the System 8000.

Table 2-11 CPU Board
Connector P2/J21

PIN	ROW A SIGNAL	ROW B SIGNAL	ROW C SIGNAL
1	TXRTNØ	RXDØ	DATAØ
2	TXDØ	CTSØ	DATA1
3	RTSØ	DTRØ	DATA2
4	DSRØ	RXD1	GND
5	TXD1	CTS1	DATA3
6	RTS1	DTR1	DATA4
7	DSR1	RXD2	GND
8	TXD2	CTS2	DATA5
9	RTS2	DTR2	DATA6
1Ø	DSR2	RXD3	DATA7
11	TXD3	CTS3	GND
12	RTS3	DTR3	DATA STROBE/DATA STROBE\
13	DSR3	RXD4	NOT USED/INPUT PRIME
14	TXD4	CTS4	TXRTN1
15	RTS4	DTR4	GND
16	DSR4	RXD5	D.D./ACKNOWLEDGE\
17	TXD5	CTS5	BUSY\
18	RTS5	DTR5	TXRTN2
19	DSR5	RXD6	GND
2Ø	TXD6	CTS6	IFVALID/FAULT\
21	RTS6	DTR6	ON-LINE/SELECT
22	DSR6	RXD7	F.P BUSACK INDICATOR
23	TXD7	CTS7	F.P. POWER-ON INDICATOR (GND)
24	RTS7	DTR7	F.P. NORMAL INDICATOR
25	DSR7	TXRTN5	NMI SWITCH (NORMALLY CLOSED)
26	TXRTN3	TXRTN6	NMI SWITCH (NORMALLY OPEN)
27	TXRTN4	TXRTN7	SW RESET
28	+5V	+5V	F.P. INDICATOR V+ (+5V)
29	-5V	-5V	-5V
3Ø	+12V	+12V	+12V
31	-12V	-12V	-12V
32	GND	GND	GND

Table 2-12 Secondary Serial Board
Connector P2/J22

ROW A PIN	ROW B SIGNAL	ROW C SIGNAL	SIGNAL
1	TXRTNØ	RXDØ	DATAØ
2	TXDØ	CTSØ	DATA1
3	RTSØ	DTRØ	DATA2
4	DSRØ	RXD1	GND
5	TXD1	CTS1	DATA3
6	RTS1	DTR1	DATA4
7	DSR1	RXD2	GND
8	TXD2	CTS2	DATA5
9	RTS2	DTR2	DATA6
1Ø	DSR2	RXD3	DATA7
11	TXD3	CTS3	GND
12	RTS3	DTR3	DATA STROBE/DATA STROBE\
13	DSR3	RXD4	N.U/INPUT PRIME
14	TXD4	CTS4	TXRTN1
15	RTS4	DTR4	GND
16	DSR4	RXD5	D.D./ACKNOWLEDGE\
17	TXD5	CTS5	BUSY\
18	RTS5	DTR5	TXRTN2
19	DSR5	RXD6	GND
2Ø	TXD6	CTS6	IFVALID/FAULT\
21	RTS6	DTR6	ON-LINE/SELECT
22	DSR6	RXD7	
23	TXD7	CTS7	GND
24	RTS7	DTR7	N.U./LP. CONT
25	DSR7	TXRTN5	
26	TXRTN3	TXRTN6	
27	TXRTN4	TXRTN7	
28	+5V	+5V	+5V
29	-5V	-5V	-5V
3Ø	+12V	+12V	+12V
31	-12V	-12V	-12V
32	GND	GND	GND

Table 2-13 mini Winchester Disk Controller-II
Connector J23 (Model 21 Plus)

PIN	ROW A SIGNAL	ROW B SIGNAL	ROW C SIGNAL
1	STEP	DRIVE 3 SELECTED	DIRECTION
2	GND	REDUCED WRITE CURRENT	GND
3	DRIVE SELECT Ø	RESERVED A (RAD DRIVE 3)	DRIVE SELECT 1
4	SPARE A (RAD DRIVE 3)	HEAD SELECT 2**Ø	GND
5	HEAD SELECT 2**1	RESERVED B (RAD DRIVE 3)	HEAD SELECT2**2
6	DRIVE SELECT 2	WRITE GATE	DRIVE SELECT 3
7	DRIVE Ø SELECTED	DRIVE 1 SELECTED	GND
8	DRIVE READY	DRIVE 3 +MFM WRITE DATA	SEEK COMPLETE
9	WRITE FAULT	DRIVE 3 -MFM WRITE DATA	TRACK ØØØ
1Ø	INDEX	DRIVE Ø -MFM READ DATA	DRIVE Ø +MFM READ DATA
11	DRIVE 1 -MFM READ DATA	DRIVE 1 +MFM READ DATA	GND
12	DRIVE Ø +MFM WRITE DATA	DRIVE 3 +MFM READ DATA	DRIVE Ø -MFM WRITE DATA
13	DRIVE 1 +MFM WRITE DATA	DRIVE 3 -MFM READ DATA	DRIVE 1 -MFM WRITE DATA
14	GND	SLAD 1 (F)	RESERVED (DAISY CHAIN)
15		GND	GND
16		DRIVE 2 +MFM READ DATA	IDS
17		DRIVE 2 -MFM READ DATA	
18		RESERVED A (RAD DRIVE Ø)	
19		D1 (F)	GND
2Ø		SPARE B (RAD DRIVE 3)	
21		GND	
22		RESERVED A (RAD DRIVE 1)	

(continued)

Table 2-13 mini Winchester Disk Controller-II
Connector J23 (Model 21 Plus)
(continued)

PIN	ROW A SIGNAL	ROW B SIGNAL	ROW C SIGNAL
23	SPARE A (RAD DRIVE Ø)	RESERVED B (RAD DRIVE Ø)	GND
24	SPARE B (RAD DRIVE Ø)	SPARE A (RAD DRIVE 1)	RESERVED B (RAD DRIVE 1)
25	SPARE B (RAD DRIVE 1)	SPARE A (RAD DRIVE 2)	DRIVE 2 +MFM WRITE DATA
26	DRIVE 2 SELECTED	RESERVED A (RAD DRIVE 2)	DRIVE 2 -MFM WRITE DATA
27	RESERVED B	SPARE B (RAD DRIVE 2)	GND (RAD DRIVE 2)
28	+5 Vdc	+5 Vdc	+5 Vdc
29	-5 Vdc	-5 Vdc	-5 Vdc
3Ø	+12 Vdc	+12 Vdc	+12 Vdc
31	-12 vdc	-12 Vdc	-12 Vdc
32	GND	GND	GND

Table 2-14 Tape Cartridge Controller
Connector P2/J24

PIN	ROW A SIGNAL	ROW B SIGNAL	ROW C SIGNAL
1		SLD\	GND
2		RDY\	GND
3		WND\	GND
4		FLG\	GND
5		LPS\	GND
6		FUP\	GND
7		BSY\	GND
8		EWS\	GND
9		RWD\	GND
10		REV\	GND
11		FWD\	GND
12		HSP\	GND
13		WEN\	GND
14		SL1\	GND
15		SL2\	GND
16		SL4\	GND
17		SLG\	GND
18		RNZ\	GND
19		RDS\	GND
20		DAD\	GND
21		WDE\	GND
22		WNZ\	GND
23		TR2\	GND
24		WDS\	GND
25		TR1\	GND
26			
27			
28	+5V	+5V	+5V
29	-5V	-5V	-5V
30	+12V	+12V	+12V
31	-12V	-12V	-12V
32	GND	GND	GND

Table 2-15 Storage Module Device Controller Board A Connector P2/J26 (Model 31 Plus)

PIN	ROW A SIGNAL	ROW B SIGNAL	ROW C SIGNAL
1	CYLTAG+	SELTAG-	SELTAG+
2	CYLTAG-	HEADTAG+	HEADTAG-
3		CONTAG-	CONTAG+
4	SEL2-	SEL2+	GND
5		SEL8-	SEL8+
6		SEL4+	SEL4-
7	SEL1+	SEL1-	GND
8			
9		BIT2+	BIT1-
10		BIT0-	BIT1+
11	BIT2-	BIT0+	GND
12	BIT3-	BIT3+	BIT7-
13	BIT9+	SPARE-	BIT7+
14	SPARE+		BIT9-
15	BIT4-	BIT4+	GND
16		BIT5+	BIT5-
17		BIT8-	BIT8+
18		BIT6-	BIT6+
19	INDEX+	INDEX-	GND
20			
21		HOLD/PICK+	HOLD/PICK-
22		FAULT+	FAULT-
23	OPENCABLE-	OPENCABLE+	GND
24	SECTOR-	ONCYL-	ONCYL+
25	SKERR-	SECTOR+	SKERR+
26	READY-	WPROT+	WPROT-
27	READY+	BUSY-	BUSY+
28	+5Vdc	+5Vdc	+5Vdc
29	-5Vdc	-5Vdc	-5Vdc
30	+12Vdc	+12Vdc	+12Vdc
31	-12Vdc	-12Vdc	-12Vdc
32	GND	GND	GND

Table 2-16 Storage Module Device Controller B Connector P2/J27 (Model 31 Plus)

PIN	ROW A SIGNAL	ROW B SIGNAL	ROW C SIGNAL
1			
2		3.SERVOCLK-	3.SERVOCLK+
3		3.READDATA-	3.READDATA+
4	3.WRITECLK-	3.READCLK-	GND
5	3.WRITECLK+	3.READCLK+	3.SELECTED-
6	3.WRITEDATA+	3.SELECTED+	3.SEEKEND-
7	3.WRITEDATA-	3.SEEKEND+	GND
8			
9			2.SERVOCLK-
10		2.SERVOCLK+	2.READDATA-
11	2.WRITECLK+	2.READDATA+	GND
12	2.WRITECLK-	2.READCLK-	2.READCLK+
13	2.WRITEDATA-	2.SELECTED-	2.SELECTED+
14	2.WRITEDATA+	2.SEEKEND-	2.SEEKEND+
15		1.SERVOCLK-	GND
16		1.SERVOCLK+	1.READDATA-
17	1.WRITECLK-	1.READDATA+	1.READCLK-
18	1.WRITECLK+	1.READCLK+	1.SELECTED-
19	1.WRITEDATA+	1.SELECTED+	GND
20	1.WRITEDATA-	1.SEEKEND-	1.SEEKEND+
21		Ø.SEEKEND-	Ø.SEEKEND+
22		Ø.SELECTED+	Ø.SELECTED-
23		Ø.WRITEDATA+	GND
24		Ø.WRITEDATA-	Ø.WRITECLK-
25		Ø.WRITECLK+	Ø.READCLK-
26		Ø.READCLK+	Ø.READDATA-
27	Ø.SERVOCLK+	Ø.READDATA+	Ø.SERVOCLK-
28	+5Vdc	+5Vdc	+5Vdc
29	-5Vdc	-5Vdc	-5Vdc
30	+12Vdc	+12Vdc	+12Vdc
31	-12Vdc	-12Vdc	-12Vdc
32	GND	GND	GND

Table 2-17 Memory Bus
Connector P2/J28 to P2/J30

PIN	ROW A SIGNAL	ROW B SIGNAL	ROW C SIGNAL
1	MD38\	MD37\	
2	MD36\	MD35\	
3	MD34\	MD33\	
4	MD32\	MD31\	GND
5	MD30\	MD29\	
6	MD28\	MD27\	
7	MD26\	MD25\	GND
8	MD24\	MD23\	
9	MD22\	MD21\	
10	MD20\	MD19\	
11	MD18\	MD17\	GND
12	MD16\	MD15\	
13	MD14\	MD13\	
14	MD12\	MD11\	
15	MD10\	MD09\	GND
16	MD08\	MD07\	
17	MD06\	MD05\	
18	MD04\	MD03\	
19	MD02\	MD01\	GND
20	MD00\	MA16	RC7\
21	MA17	MA18	BD SELECT\
22	MA19	MA20	READ\
23	MA21	MA22	GND
24	MA23	RC0\	RAS\
25	RC1\	RC2\	REF\
26	RC3\	RC4\	CAS\
27	RC5\	RC6\	WRITE\
28	+5V	+5V	+5V
29	-5V	-5V	-5V
30	+12V	+12V	+12V
31	-12V	-12V	-12V
32	GND	GND	GND

SECTION 3
INSTALLATION

3.1. Overview

The Zilog System 8000 Models 21 Plus/31 Plus are shipped as fully loaded configurations. All Printed Circuit Boards (PCBs) are installed. Tape cartridge cables and disk drive cables are also installed.

NOTE

The system power cord may be packed in the bottom Accessory module, or in the documentation shipping container.

Detailed step by step instructions to install a Zilog System 8000, from site verification to System Power-Up Diagnostics (SPUD) are as follows:

- Overview
- Site Verification
- Shipping and Receiving
- System Interconnection
- System Installation

Refer to the Stand-Alone Diagnostic Interactive Executive (SADIE) Reference Manual for system diagnostic test functions.

3.2. Site Verification

System installation usually requires a minimum amount of site verification. Certain areas of consideration should be reviewed before receiving and installing the system. These considerations include environment, power, and space allocations.

Reference the Zilog System 8000 Site Preparation Manual for pre-site considerations prior to system installation.

Refer to Section 2 of this manual for a composite of the Models 21 Plus/31 Plus system specifications and characteristics.

Another suggested consideration for site verification is the on-site positioning of the system. Ensure that the system is setup where it can easily be moved away from the walls or other equipment for maintenance purposes.

3.3. Shipping and Receiving

This section contains information about the system's shipping container (paragraph 3.3.1), unpacking and inspecting it, (paragraph 3.3.2), and the recommended instructions for unpacking and inspecting the system. A re-packing procedure is also provided (paragraph 3.3.3).

3.3.1. Shipping Container

The system is shipped in a specially designed shipping container (refer to Figure 3-1.) The foam lined top cover, back panel, and side panel protect the system during shipment.

The shipping container has a unique front cover with a dual purpose. During shipment, the front cover is part of the shipping container. After receipt of the system, the front cover is designed to be an unloading/loading ramp.

The shipping container is secured to the pallet with straps that pass under the pallet and over the top cover. The pallet sits on four large circular rubber shock mounts which are permanently secured to the pallet.

One additional container is shipped with the system. It contains the system documentation, a set of system keys that are packaged with the operating system tape (ZEUS), a scratch tape, and the SADIE diagnostic tape.

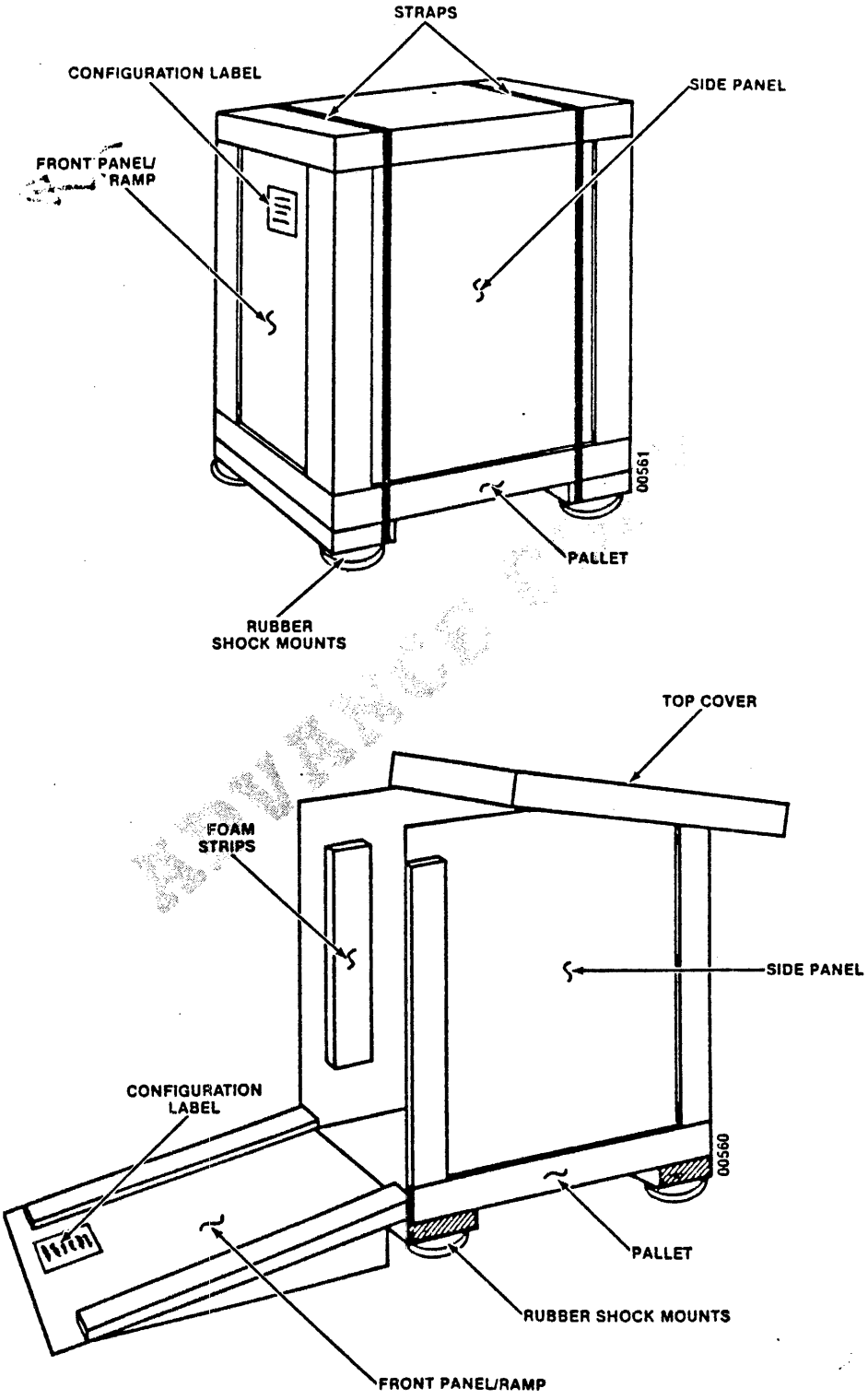


Figure 3-1 System Shipping Container

3.3.2. Unpacking and Inspection

The following paragraphs provide specific instructions for systematically unpacking and inspecting the system:

Unpacking the System

Visual Inspection of the System

Verification of the CPU Line Voltage Selection

Disk/Tape Module Visual Inspection

Disk/Tape Power Supply Verification

The Zilog System 8000 was factory inspected and tested prior to shipment. Sometimes during shipment, and unbeknownst to the shipping carrier, a problem occurs that can affect the system's operation and performance. This could be something as simple as excessive movement which may loosened some of the system cables or harnesses.

Damage to the system, external or internal, MUST be reported to the carrier's agent within 48 hours. Original packing material (i.e. container, straps, pallet, etc.) MUST be retained to support any claim of shipping damage.

Refer to Figure 3-1 while performing the following steps:

1. Using the shipper or waybill, check that all shipping containers have arrived. Manuals, tapes, and keys are packaged separately.

2. Check the shipping configuration label (located on the front panel of the shipping container) for system information.

3. Verify system configuration with the waybill.

4. Visually inspect the exterior of the shipping container for possible shipping damage. If damage is present, report it to the carrier's agent within 48 hours as follows:

   a. Fill out a shipping damage report.

b. Record the damage found on the waybill.

c. Have the shipping agent sign the waybill.

d. Make three copies of the report and the waybill.

e. Send a copy of the damage report and the waybill to the shipping agent carrier, to Zilog, Inc., and retain a copy for your records.

WARNING

The standard configured system weighs approximately 250 pounds (114 kg). To avoid personal injury, request assistance when you move the system.

3.3.2.1. Unpacking the System: The following steps are the recommended instructions to unpackage the system.

1. Carefully cut the straps from around the shipping container; remove the straps.

NOTE

When performing the following steps, avoid scratching the system covers.

2. Carefully lift and remove the shipping container's top cover.

3. Remove the piece of styrofoam from inside the front panel of the shipping container.

4. Carefully lift the front panel up and remove it from the pallet, and turn it over.

5. Place the front panel wedge-side down, and directly in front of the system. The front panel is now the unloading ramp for the system.

7. Carefully roll the system down off the pallet onto the floor.

8. Again visually inspect the exterior of the shipping container for possible shipping damage. If damage is present, follow the steps in paragraph 3.3.2, Step 4. Return to paragraph 3.3.2.2.

3.3.2.2. Visual Inspection of the System: Follow the steps below to inspect the system after shipment.

1. Visually inspect the system cabinet for possible damage. If damage is present, follow Step 4 in the preceding paragraphs, then continue.

2. Carefully position the system on site. Position the other peripheral equipment, if required.

NOTE

The following provides the steps to inspect the CPU and the Disk/Tape module for possible internal shipping damage.

3. Remove the front panel from the CPU module. Remove the foam insert inside the CPU module.

4. At the back of the system, loosen the cable cover thumbscrews and slide it off the module.

5. Remove the CPU module top panel by loosening the two thumbscrews and slide it off the module.

6. Remove the CPU module top plate by lifting it up and out of the module.

7. Remove and save the four Phillips-head screws that secure the power supply cover to the power supply; remove the cover.

8. Remove the sheet metal cover from the card cage.

9. Using Figure 2-2 for Model 21 Plus or Figure 2-5 for Model 31 Plus, verify the PCB board card slot locations. (Options may change the PCB locations.) Visually examine each PCB board to ensure it is properly seated in its appropriate backplane connector.

10. Examine the cable harnesses for possible broken terminals, loose, frayed, or broken wires, and/or broken cable straps.

11. Examine the Z-Bus Backplane Interconnect (ZBI) on the back of the card cage for possible cracks or damaged connectors.

12. Check the I/O connector panel at the rear of the CPU module for cracks, loose or broken wires, or broken cable straps.

3.3.2.3 Verification of the CPU Line Voltage Selection: The following steps verify the CPU power supply line voltage.

CAUTION

Line voltage setting must ONLY be performed by Zilog Field Service personnel. Improper switch settings could damage the system.

Figures 3-2 for Model 21 Plus and 3-3 for Model 31 Plus shows the line voltage selection matrix which is silk-screened on the power supply cover.

Verify that the CPU ac line voltage setting on the power supply agrees with the ac voltage specified on the system ID plate as follows:

The Model 21 Plus has switches S1, S2, and S3 which are set for a line voltage of a ???-??? (Vac).

The Model 31 Plus has switches S1, S2, and S3 which are for a line voltage of 11Ø-13Ø (Vac). If there is a difference, notify Zilog Field Service before proceeding.

TO BE SUPPLIED

Figure 3-2 Model 21 Plus Model AC Line Voltage

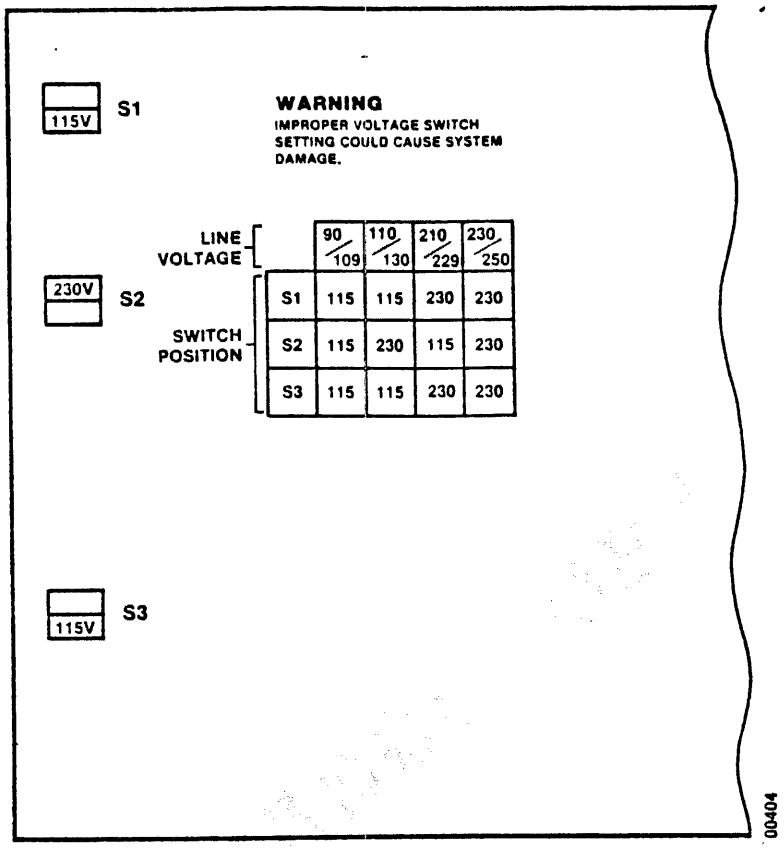


Figure 3-3 Model 31 Plus CPU Model AC Line Voltage

3.3.2.4 Disk/Tape Module Visual Inspection: The steps that follow remove the CPU module from the system to allow access to the Disk/Tape module for visual inspection of its cabling.

1. Remove the CPU module as follows:

   a. Label and remove the I/O cables and the ac power cable from the CPU module.

   b. Unfasten two intermodule captive fasteners at the back of the module.

   c. Be careful not to damage the RFI gaskets while performing the following. Request assistance when necessary. Carefully slide the CPU module back and disengage it from the Disk/Tape module guide posts. Remove the CPU module and carefully set aside.

2. Visually examine the data, tape drive and other internal cables. Ensure that they are securely fastened to their mating connectors.

3. Visually examine the Disk/Tape module cable harnesses for broken terminals, loose or broken wires, or broken cable straps.

NOTE

The Model 21 Plus has a 52M byte Winchester disk drive with heads that lock automatically when the system is powered down.

4. For the Model 31 Plus, verify that the drive actuator locking lever is in the LOCK position (Figure 3-4).

5. Inspect the physical mounting of the drive to ensure that the drive is secure at all mounting points, and all ribbon cables are securely connected.

CAUTION

Improper orientation of the drive power cable and connector can result in serious damage to the drive. Verify its connection before applying power to the disk drive.

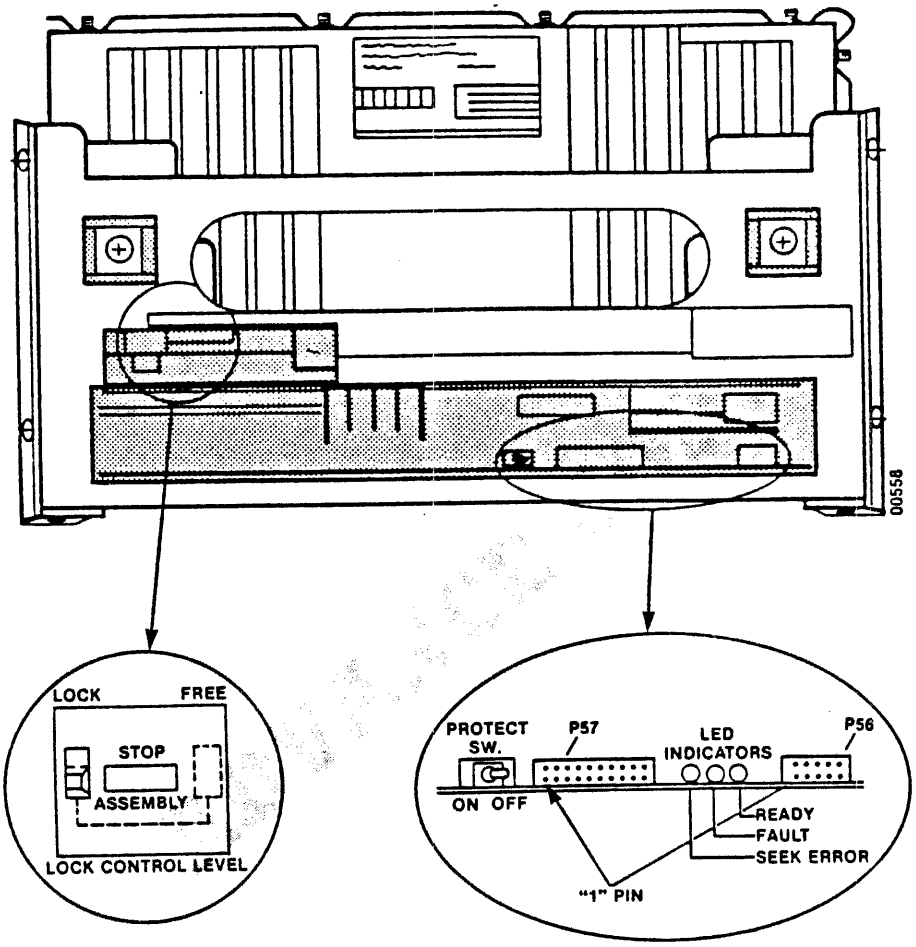


Figure 3-4 Model 31 Plus Drive Locking Lever

3.3.2.5 Disk/Tape Power Supply Verification: Line voltage setting must ONLY be performed by Zilog Field Service personnel. Improper switch settings could damage the system. For the Model 21 Plus - Figure 3-5 shows the line voltage selection matrix which is silk-screened on the power supply. Switch S1 is set for a line voltage of 100-115 (Vac)???.

For the Model 31 Plus - Figure 3-6 shows the line voltage selection matrix which is silk-screened on the power supply cover. Switches S1, and S2 are set for a line voltage of 110-130 (Vac). The following steps verify the line voltage for each system model.

1. Verify that the ac line voltage setting on the power supply agrees with the ac voltage specified on the system ID plate.

   If there is a difference, notify Zilog Field Service before proceeding.

2. Re-assemble the Disk/Tape module and re-connect the cables. Carefully replace the CPU module module. Reconnect the I/O cables and the ac power cables, verifying connections. Refer to Figure 3-7 for cabling connector identification for a typical 8 user system.

TO BE SUPPLIED

Figure 3-5 Model 21 Plus Disk/Tape AC Line Voltage

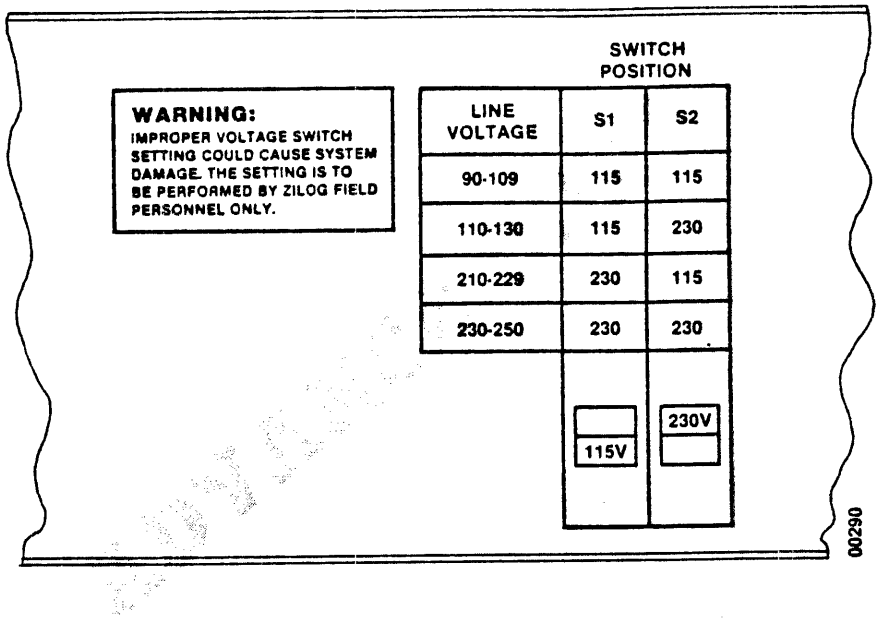


Figure 3-6 Model 31 Plus Disk/Tape AC Line Voltage

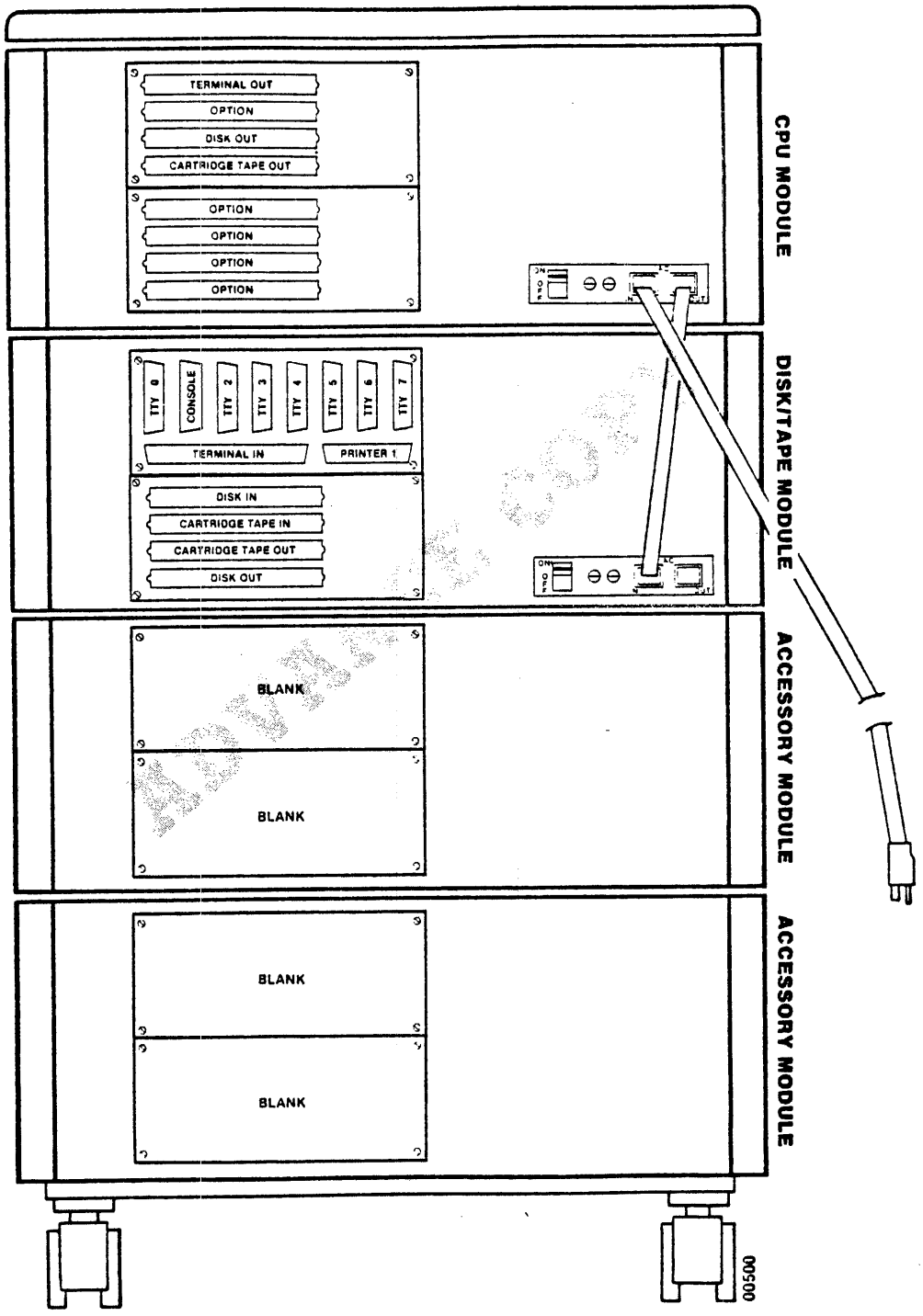


Figure 3-7 Typical 8 User Connector Configuration

3.3.3. Re-Package The System

Perform a tape dump before bringing the system down. Refer to the ZEUS Administrator Manual for the recommended tape dump procedure.

The steps listed below provide the recommended instructions to re-package the system whenever the system is to be moved or relocated:

WARNING

ALL POWER CABLES MUST BE DISCONNECTED AND REMOVED FROM THE MAIN POWER SOURCE TO PREVENT PERSONAL INJURY WHILE PERFORMING THE FOLLOWING STEPS.

1. Power-down the system as described in the AC Power Removal Section 5.2 of this manual. (Reference the ZEUS Administrator Manual, Section 2.)

NOTE

Step 2 applies only to the Model 31 Plus.

2. Allow the drive to spin down for approximately one minute before proceeding.
3. At the rear of the system, loosen the cable cover thumbscrews. Open the top cable cover.
4. Label and disconnect the intermodule ac cables. Place the cables in the Accessory module.
5. Label and disconnect the terminal cables. Place the cables in the Accessory module.
6. Place the ZEUS operating system tape, the SADIE diagnostic tape, and the newly created system dump tape in the Accessory module.

CAUTION

Damage to the Model 31 Plus drive can occur if the drive heads are not locked before moving the system. Step 7 applies only to the Model 31 Plus.

7. Move the drive actuator locking lever to the LOCK position (reference Figure 3-4).

8. Turn the system key to the LOCK position. Remove the key and put it in an envelope. Place the envelope in the Accessory module.

9. Using the original shipping container and pallet, remove the shipping container's top cover. Remove the front cover and place it wedge-side down in front of the shipping pallet. Refer to Figure 3-1 for ramp orientation.

/ **WARNING**

THE STANDARD CONFIGURED SYSTEM WEIGHS APPROXIMATELY 25Ø POUNDS (114 kg). TO AVOID PERSONAL INJURY, REQUEST ASSISTANCE WHEN YOU HAVE TO MOVE THE SYSTEM.

1Ø. Position the system with the cables toward the back of the shipping container and carefully roll the system onto the pallet and into the shipping container.

11. Carefully lift the ramp up, turn it over (wedge-end down) and replace it in its slot in the shipping container.

12. Place a piece of styrofoam between the front of the system and the shipping container to prevent the container from making contact with the system.

13. Carefully place the shipping container's top cover on top of the shipping container, over the system.

14. Re-strap the shipping container to the pallet.

3.4. System Installation

The following subsections contain the recommended procedures to install, interconnect, and power-up the system. This section is divided into the following subsections:

Cable Interconnect

Disk Drive Configuration Checks

Line Printer Installation

Modem Installation

Disk Power-On Procedure

System Power-Up and Diagnostics (SPUD)

3.4.1. Cable Interconnect

The following ten steps are the recommended instructions to interconnect the system, including its peripheral devices.

1. Using Figures 3-8 through 3-11 (Figure 3-9 applies only to the Model 21 Plus), verify the system I/O panel and terminal distribution panel connections.

   Figures 3-9 through 3-11 show typical (intermodule) system cabling configurations for 8, 16 and 24 users (cable covers are removed for clarity).

NOTE

System and ac cables may be shipped in separate containers or placed in the Accessory module. Disk drive dependencies are identified when required.

2. Table 3-1 provides a list of (system) interface cables. (The Model 31 Plus SMD A and SMD B interface cables connect directly to the SMD interface board.) Verify system cables and connections.

   Reference the appropriate Field Upgrade Procedure for connector information, or contact your Zilog Field Service personnel for additional connector information.

Table 3-1 System Interface Cables

CABLE	TYPE	VENDOR/PART NUMBER
Model 21 Plus		
Signal	40-conductor ribbon cable max. 30 feet (9.1 cm)	
	Connector (Open strain relief)	TO BE SUPPLIED
DC Power	10-conductor, 18 gauge wire max. 4 feet (1.2 m)	
	Connector	
Model 31 Plus		
SMDC B Signal	26-conductor ribbon	Zilog 59-0235
SMDC A Signal	60-conductor twisted	Zilog 59-0234
AC Power	14-conductor,18 gauge wire, radial	Zilog 59-xxxx
AC Power SMD	3-wire ac, 120V Fan	N/A

NOTE

The display terminals and high-speed printers connect to the system through eight RS-232C serial ports and one parallel printer port. These ports are located on the back of the terminal distribution panel for each Disk/Tape module.

3. Verify that the drive and tape interface cables are connected as follows:

   a. From the CPU I/O panel - CARTRIDGE TAPE OUT is connected to CARTRIDGE TAPE IN - on the Disk/Tape module.

   b. Model 21 Plus - From the CPU I/O panel - DISK OUT is connected to DISK IN - on the Disk/Tape module.

   c. Model 31 Plus - From the CPU I/O panel - SMD A OUT is connected to SMD A IN - on the Disk/Tape module.

   d. Model 31 Plus - From the CPU I/O panel - SMD B OUT is connected to SMD B IN - on the Disk/Tape module.

NOTE

The Intermodule cabling discussion continues on page 3-23.

TO BE SUPPLIED

Figure 3-8 Typical System Cabling Configuration

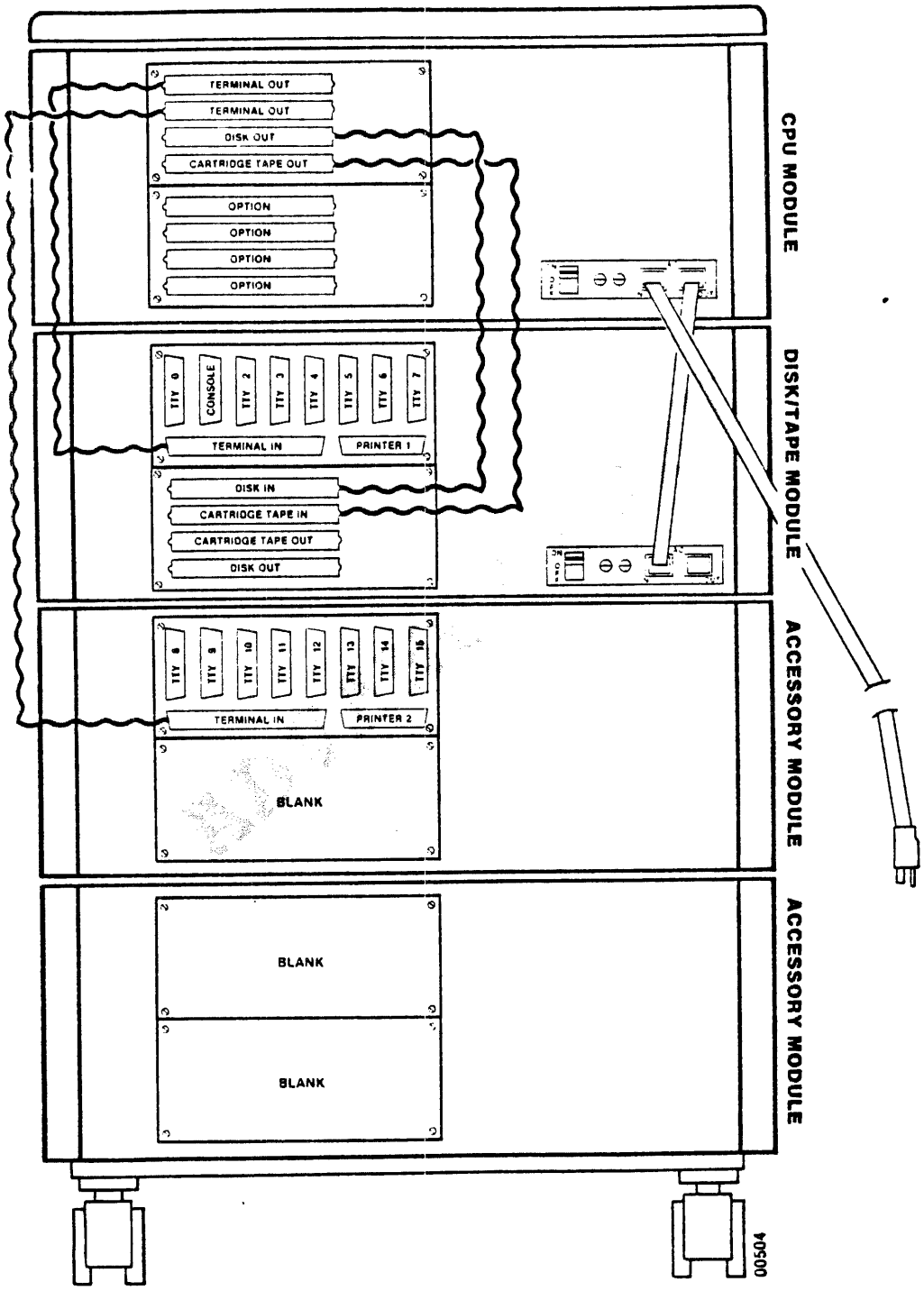


Figure 3-9 Model 21 Plus Typical 16 User Cabling Configuration

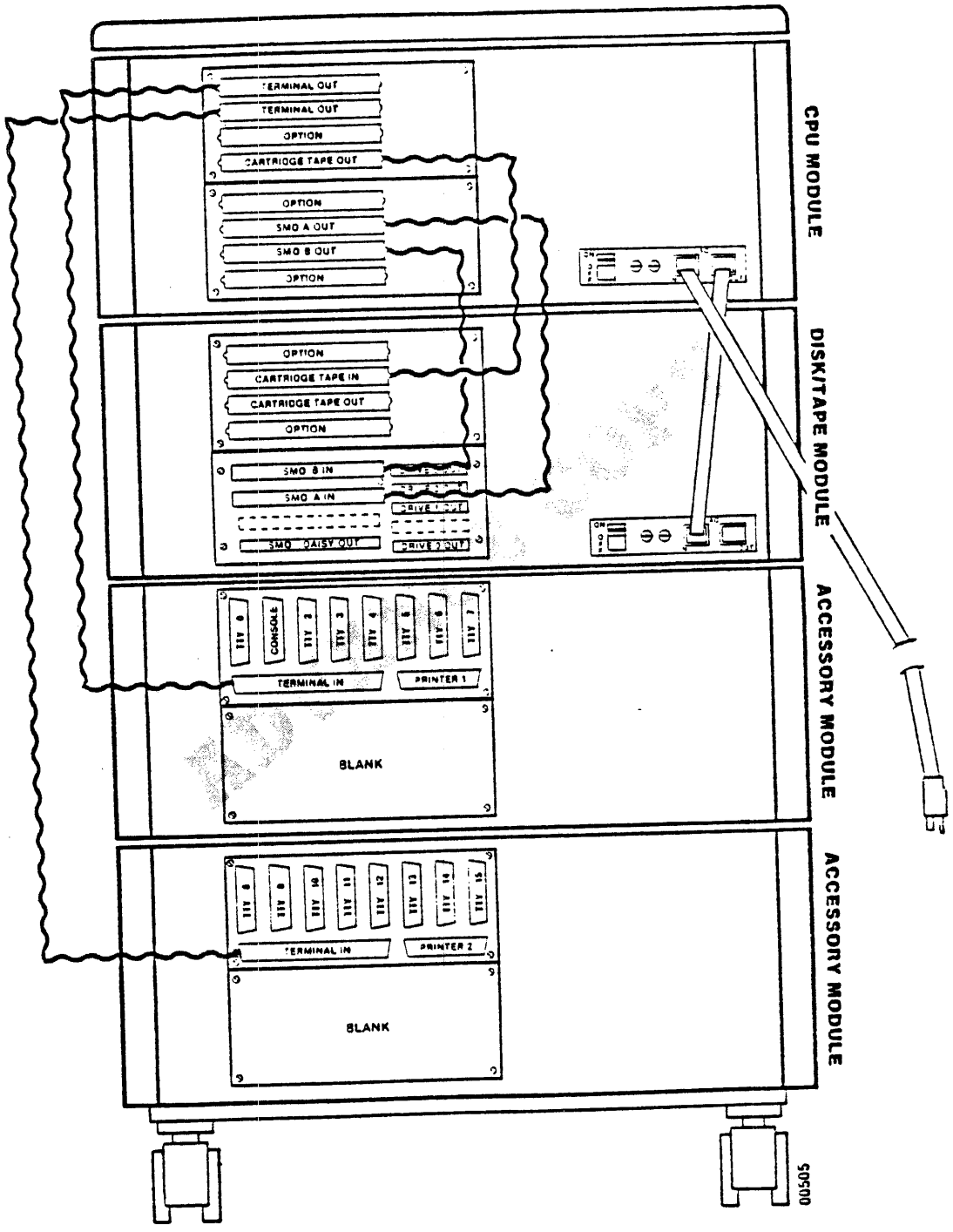


Figure 3-10 Model 31 Plus Typical 16 User Cabling Configuration

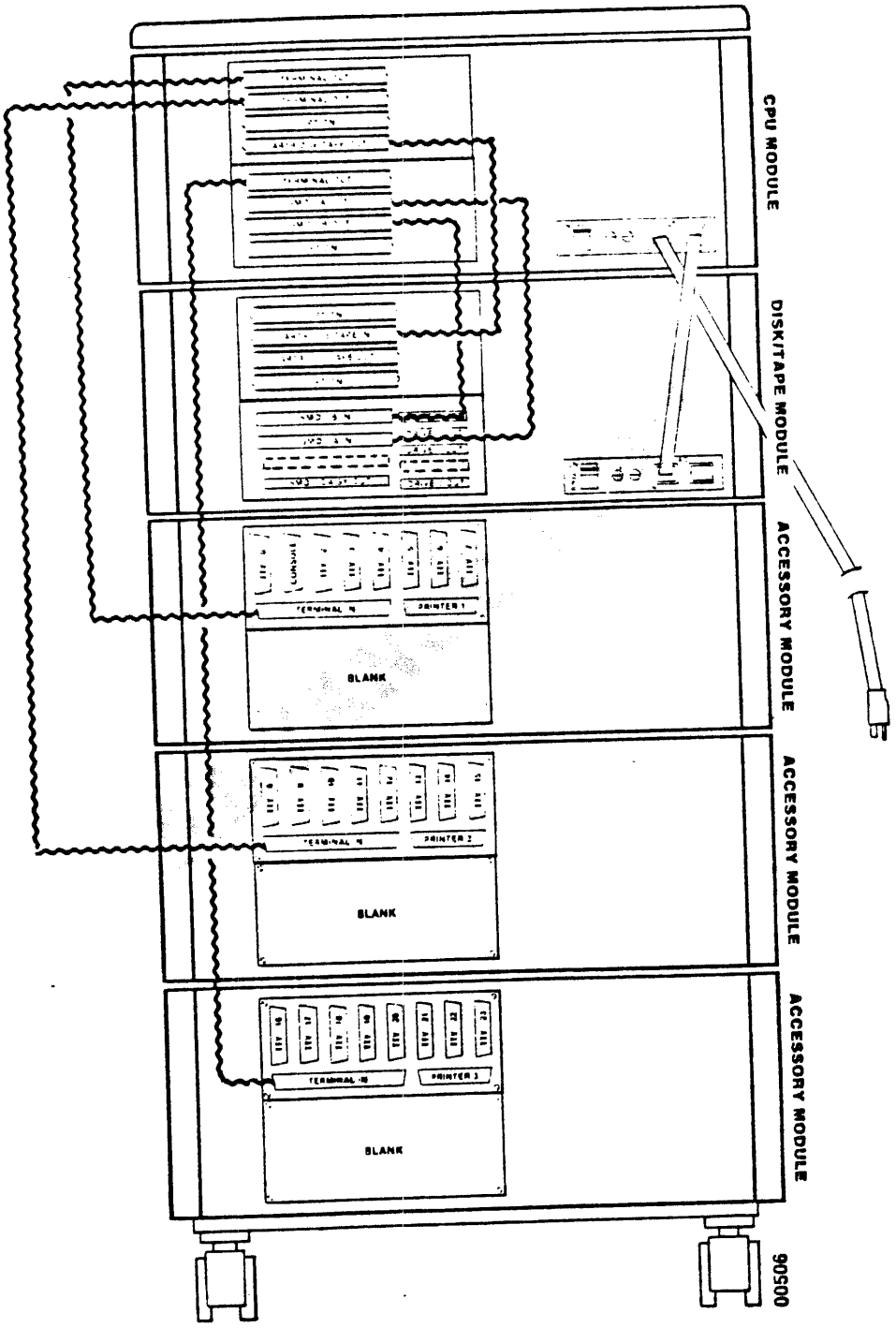


Figure 3-11 Model 31 Plus Typical 24 User Cabling Configuration

4. Verify the terminal interface cable connection is installed between the CPU module - from TERMINAL OUT connector and the first terminal distribution panel - TERMINAL IN connector.

5. Install, in a daisy-chain configuration, the (short) ac power cables between the modules, starting with the top (CPU) module.

6. Plug the main power cord into the CPU module.

7. Check the peripheral devices and ensure that they are placed in reach of the required connectors at the terminal distribution panel I/O ports, and the facility ac power.

NOTE

Refer to the ZEUS Administrator Manual, Section 7, for adding terminals.

8. Label the tty terminal to be used for the system bootstrap as "console". Connect it to the terminal I/O port labeled "console".

9. Connect the user terminals, as required, to the terminal I/O ports labeled TTY0, TTY2 through TTY7. If the system is configured for the 16 user option, reference Figure 3-8 and connect the next eight terminals to I/O ports TTY8 through TTY15.

10. Connect the line printer interface cable to the first terminal distribution panel parallel port labeled "printer". (refer to paragraph 3.4.3 for additional information about line printer installation).

    If a second terminal distribution panel is part of the system configuration, connect the printer interface cable to the I/O port labeled "printer2"

3.4.2. Disk Drive Configuration Checks

The system is shipped with either a 52M byte 5 1/4 inch Winchester drive installed in the Model 21 Plus, or a 168M byte Storage Module Device (SMD) drive installed in the Model 31 Plus.

The drive is mounted in place with its cables installed. The paragraphs that follow provide the information needed to verify:

Disk Drive Cabling

Disk Drive Configuration

Disk Drive Installation Mode Switch "14A" (Model 31 Plus)

Disk Drive Status Indicators

Disk Drive Head Locking And Unlocking Actuator (Model 31 Plus)

Disk Drive Cable Termination

NOTE

Differences in the system models will be identified in the text.

3.4.2.1. Disk Drive Cabling: Figures 3-12 (Model 21 Plus) and 3-13 (Model 31 Plus) illustrate the interface cabling for the A and B Interface cables that interconnect to the 60-pin and 26-pin drive connectors.

Figures 3-14 (Model 21 Plus) and 3-15 (Model 31 Plus) illustrate the drive cable connection locations.

Figures 3-16 (Model 21 Plus) and 3-17 (Model 31 Plus) shows the drive power connectors and pin assignments.

CAUTION

Severe damage to the drive will occur if the power cable is plugged in incorrectly. Exercise extreme caution when reconnecting the power cable. Verify its installation BEFORE applying power to the drive.

TO BE SUPPLIED

Figure 3-12 Model 21 Plus Drive Interface Cabling

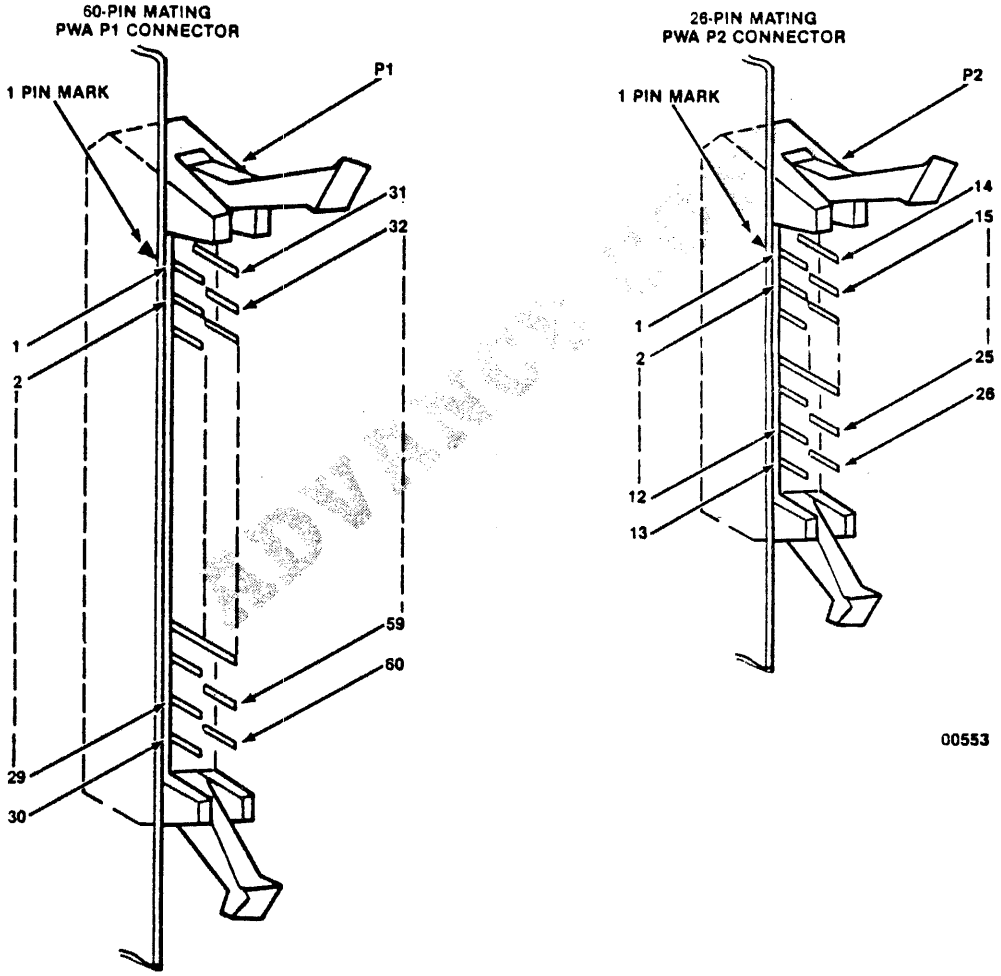


Figure 3-13 Model 31 Plus Drive Interface Cabling

TO BE SUPPLIED

Figure 3-14 Model 21 Plus Cable Connector Locations

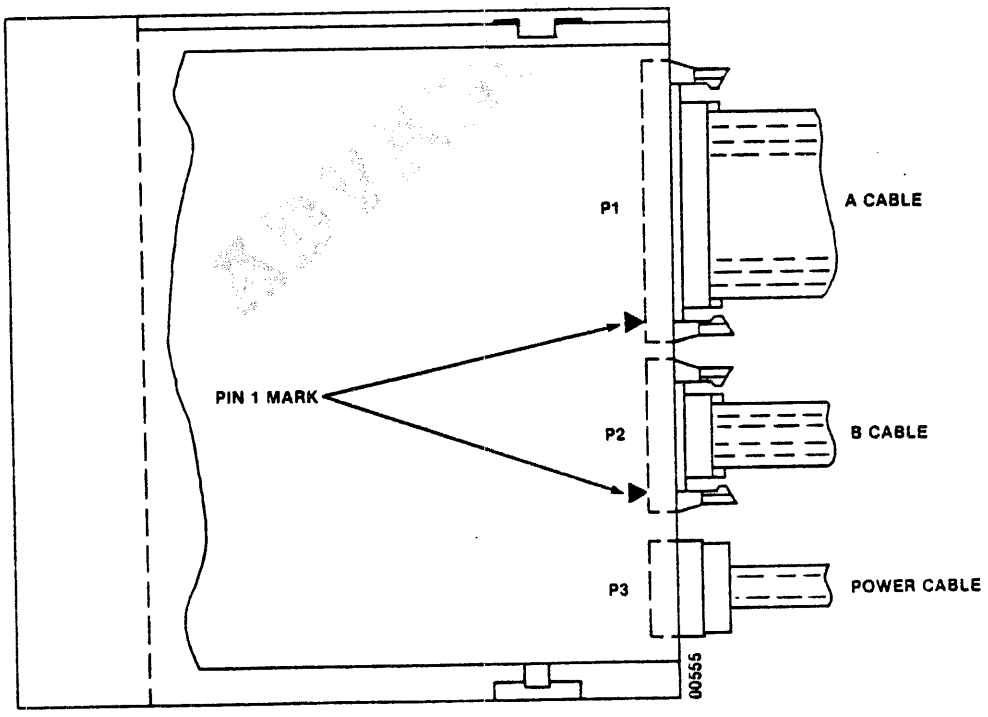
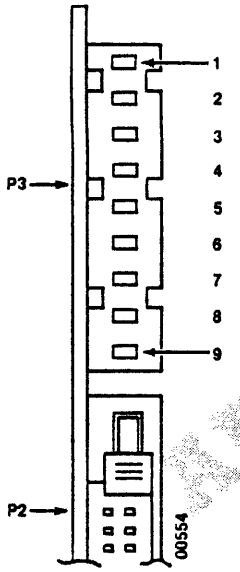


Figure 3-15 Model 31 Plus Cable Connector Locations

TO BE SUPPLIED

Figure 3-16 Model 21 Plus DC Power Cable Connector And Pin Assignments



PIN NUMBER	FUNCTION
1	GND (+5)
2	+5V
3	+5V
4	-5V
5	-12V
6	GND (+12)
7	+12V
8	+24V
9	24V-RETURN

Figure 3-17 Model 31 Plus DC Power Cable Connector And Pin Assignments

3.4.2.2. Disk Drive Configuration: Figure 3-18 (Model 21 Plus) and Figure 3-19 (Model 31 Plus) shows an exposed view of the SEALED disk drives. (The view of the drive is for general information only.)

CAUTION

Do not disassemble the disk drive. Damage to the disk drive will result if the drive is unsealed.

The Model 21 Plus disk drive has four disk platters, with seven R/W heads and one servo head.

The Model 31 Plus disk drive has five disk platters, with eight R/W heads and one servo head.

TO BE SUPPLIED

Figure 3-18 Model 21 Plus Disk Drive Configuration

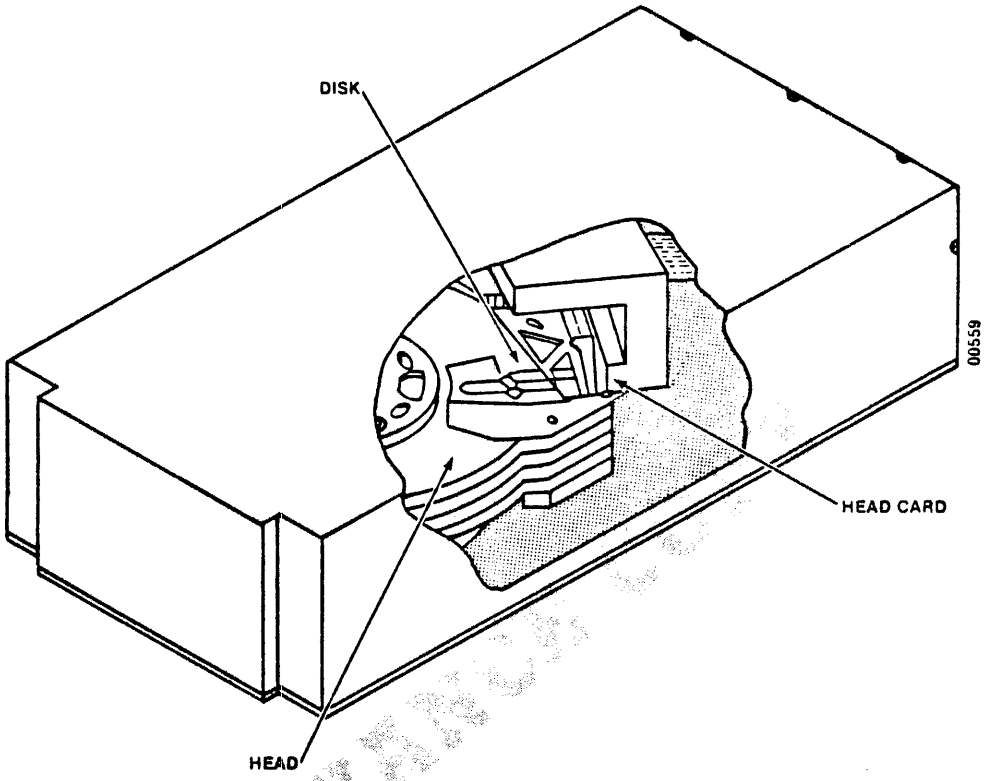


Figure 3-19. Model 31 Plus Disk Drive Configuration

3.4.2.3. Model 21 Plus Drive Installation Mode Switch:

TO BE SUPPLIED

TO BE SUPPLIED

Figure 3-2Ø Model 21 Plus Drive
Installation Mode Switch

3.4.2.4. Model 31 Plus Drive Installation Mode Switch "14A": When the drive is installed in the system, the Mode Select Dual-Inline-Package (DIP) Switch is set according to system requirements.

The drive is configured to select the next consecutive logical unit drive address number by setting the Address Select Mode DIP Switch (SW1). The DIP Switch is located on the Logic and Servo PCB assembly for the drive (Figure 3-21).

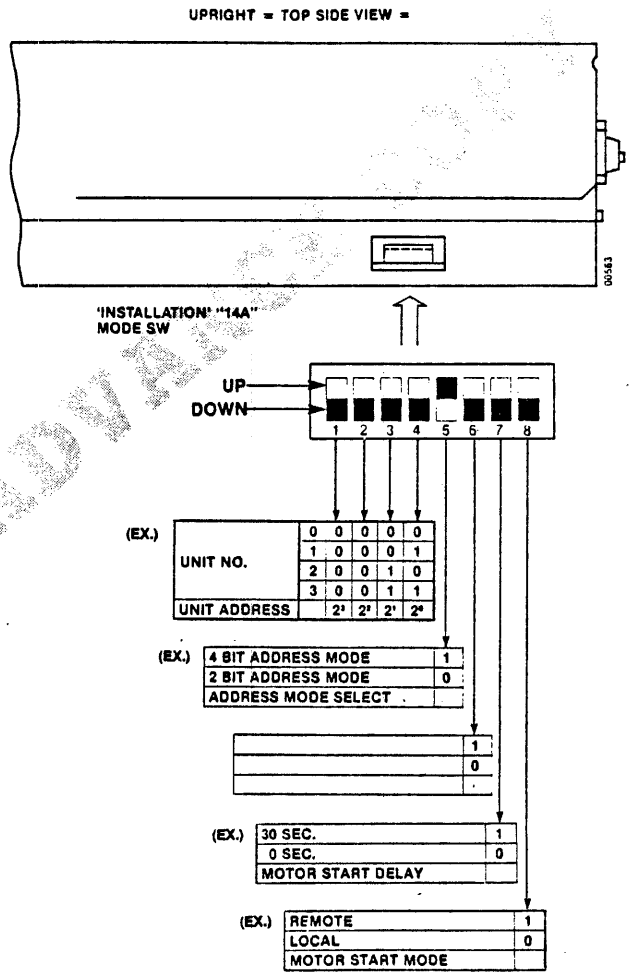


Figure 3-21 Model 31 Plus Drive Installation Switch 14A

If the system is configured with more than one disk drive, be sure to re-configure the logical unit number of the drive address to sequentially select each disk for a unique address.

NOTE

DIP switches Control Mode "13" and Sector Switch "14M" for the drive are set at the factory. Do not change the position of these switches.

The drive controller has one 16-bit I/O port. The I/O port address is "7FXY"; where XY is specified by the DIP switch keys 2 through 8. The I/O address must be EVEN. The first key is reserved and should be in the "ON" position. The functions of each key are described in Table 3-2.

Table 3-2 Drive Key Functions

KEY	FUNCTION	POSITION FOR "7FØØ"
1	Reserved	ON {ON = Ø}
2	Address Ø1	ON {OFF = 1}
3	Address Ø2	ON
4	Address Ø3	ON
5	Address Ø4	ON
6	Address Ø5	ON
7	Address Ø6	ON
8	Address Ø7	ON

3.4.2.5. Model 21 Plus Disk Drive Status Indicators:

TO BE SUPPLIED

3.4.2.6. Model 31 Plus Disk Drive Status Indicators: The 168M byte drive has three LED indicators:

RDY (Ready) Indicator: Green

The RDY indicator, when illuminated, indicates the initial seek has been performed, and the basic Ready conditions are satisfied.

FLT (Fault Status) Indicator: Red

A fault status condition is indicated when the light is illuminated.

SKE (Seek Error) Indicator: Orange

A seek error status condition is indicated when the light is illuminated.

NOTE

The File Protect Switch, the write protect for the drive, inhibits any write operation if incorrectly placed in the ON position. Be sure that it is in the OFF position.

3.4.2.7. Model 31 Plus drive Head Locking Unlocking Actuator: The Model 31 Plus drive has a head locking and unlocking actuator lever located at the front of the drive (refer to Figure 3-3).

The following steps unlock the drive R/W heads. (The procedure to lock the R/W heads is provided for future reference.)

Steps to unlock the drive R/W heads follow on the next page:

1. Remove the front panel of the disk module to access the disk locking/unlocking actuator.
2. Move the drive actuator locking lever to the FREE position releasing the drive heads.
3. Replace the front panel of the disk module.

To lock the drive R/W heads:

1. Remove the front panel of the disk module to access the disk locking/unlocking actuator. Allow the drive to spin down to a complete stop before proceeding.

2. Move the drive actuator locking level to the LOCK position, locking the heads.

3. Replace the front panel of the disk module. To lock the Read/Write heads, reverse the above order and move the drive actuator locking lever to the LOCK position.

4. If the system is configured with more than one drive, the logical unit number of the drive address must be re-configured to sequentially select a unique address for each additional disk drive (refer to paragraph 3.4.2.3.).

5. Verify the drive cable termination before proceeding. Refer to paragraph 3.4.2.6.

6. The drive is now ready to power up. Reference paragraph 3.4.5 the drive power-up procedure. Continue with paragraph 3.4.6 System Power-Up Diagnostics (SPUD), then return to Step 7.

CAUTION

Certain SADIE diagnostics are DATA-DESTRUCTIVE and could result in overwriting the disk media. Be sure to ONLY execute the SMDCRC diagnostic.

7. Using the SADIE Reference Manual, run the SMDCRC SADIE Diagnostic to ensure operability of the disk drive.

3.4.2.8. Model 21 Plus Winchester Drive Cable Termination:

TO BE SUPPLIED

TO BE SUPPLIED

Figure 3-22 Model 21 Plus Drive Cable Termination

3.4.2.9. Model 31 Plus Cable Termination: Verify that the A cable signals are terminated by four resistor networks (16-pin DIPs) on the interface board of the last disk drive only (refer to Figure 3-23).

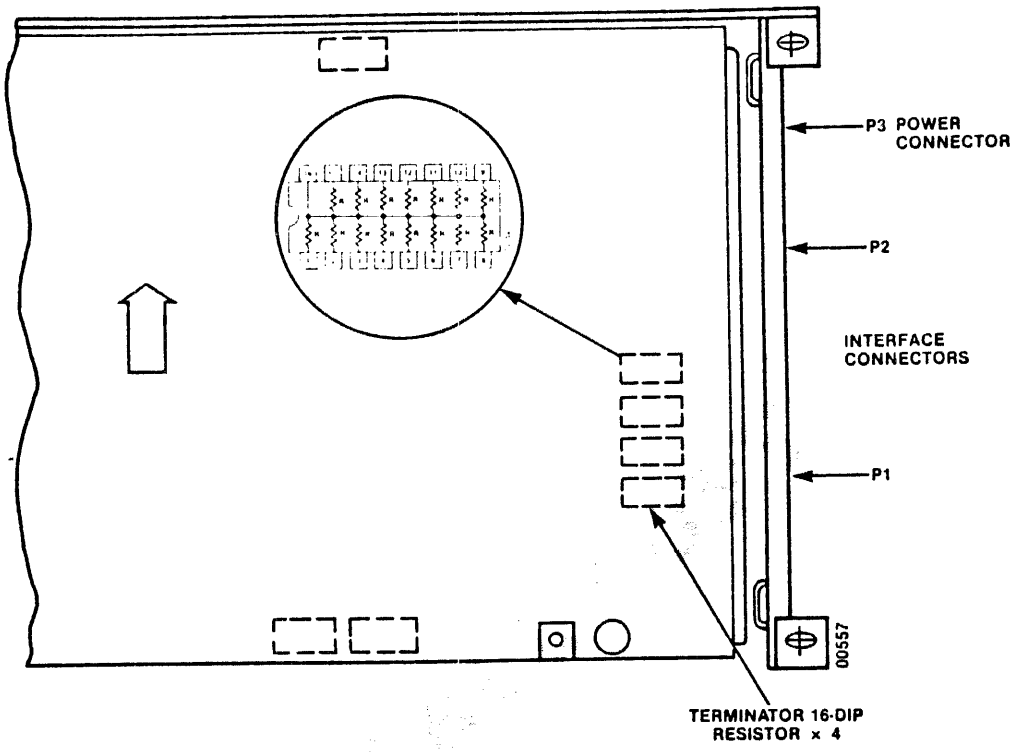


Figure 3-23 Model 31 Plus Drive Cable Terminators

3.4.3. Line Printer Installation

This procedure provides information to install the hardware interface between the printer and the host system.

The Zilog operating system will support printers with a Centronics or Data Products interface. The line printer driver has been tested with the following printers:

Zilog PRZ 2/1Ø - Centronics interface

Zilog PRZ 3/3Ø - Centronics interface

Zilog PRZ 3/6Ø - Centronics interface

The line printer installation procedure is as follows:

1. Remove all ac power, refer to Subsection 5.2.

2. Disengage the thumbscrews in back of the system modules. Open the cable covers on all modules.

3. Attach the line printer interface cable to the first connector labeled "printer" on the terminal distribution panel. Refer to Figure 3-6 for connector identification.

4. Dress the line printer interface cable(s) flush to the system and close the cable covers on all modules.

5. Remove the CPU module front panel.

6. Unseat and remove the CPU board from slot 1 of the card cage.

NOTE

The printer port on the first terminal distribution panel is controlled by jumpers on the CPU board. Factory default setting is for a Centronics interface.

7. Verify that the printer configuration jumpers are installed on the CPU Board as shown in Table 3-3.

Table 3-3 Printer Interface Connection for CPU

Printer Interface	Jumper Group
Centronics	E13 to E14 E17 to E18
Data Products	E14 to E15 E16 to E17

8. Reseat the CPU board into card slot 1.

9. If the system is configured for two line printers, unseat and remove the Secondary Serial Board (SSB) from its appropriate card slot. If the system is configured with two SSB boards, only re-configure the first SSB board if required in Step 1Ø below.

NOTE

The printer port on the second terminal distribution panel is controlled by jumpers on the first of two possible optional SSB boards.

10. Verify that the printer jumpers are installed on the SSB board as shown in Table 3-4.

Table 3-4 Printer Interface Connector for SSB

Printer Interface	Jumper Group
Centronics	E2 to E3 E4 to E5
Data Products	E1 to E2 E5 to E6

11. Reseat the SSB into its appropriate slot.

NOTE

For line printer software consideration refer to the ZEUS Administrator Manual, Section 7, Line Printer Information.

3.4.4. Modem Installation

The system requires a "null" modem cable to communicate properly with customer supplied modems. The recommended cable configuration is provided in Table 3-5.

Table 3-5 System 8000 Cable Configuration

System Pin #	Signal Name	Modem Pin #
2	TXD	3
3	RXD	2
4	RTS	5
5	CTS	4
6	DSR	20
7	SGD	7
20	DTR	6

Some modems may require other signals, such as RLSD, Pin 8, that are not listed above. The vendor's modem manual should be consulted for additional hardware and cable wiring requirements for the modem's specific signal needs.

User File Set-Up

NOTE

Refer to the ZEUS Reference Manual for additional information about Remote(1) and CU(1). Refer to the ZEUS Utilities Manual for additional information about UUCP.

The following steps provide the instructions to set-up the system for Remote(1) and CU(1):

1. Modify the files for Remote(1) as follows:

   Edit the file

   /usr/spool/uucp/remotelines

   Enter into the file a key word (any word will do), and the dial-out port number, followed by the baud rate. For example:

   dialout /dev/tty2 1200

Invoke remote(1). Your command line will be:

```
remote dialout
```

2. Modify the files for cu(1) as follows:

Edit the file

```
/usr/lib/uucp/L-devices
```

If you are running ZEUS 2.2, the file needs to contain an entry such as:

```
DIR tty2 12Ø0
```

Invoke CU(1). Your command line should be:

```
cu -s 12Ø0 -l /dev/tty12 dir
```

3. Remove the listener for the port on which you will be dialing out.

Edit /etc/ttys OR /etc/inittab, depending on the revision level of ZEUS.

For /etc/ttys, change the first column of the port's entry to a "Ø". Change the second column to a "3" or a "5" for consistency.

Issue the command:

```
kill -2 1
```

4. To remove the login on the port that has been changed, in /etc/inittab, remove the state 2 entry for the port.

Issue the command:

```
init 2
```

Do a "ps -aef".

NOTE

You may have to kill the process that was running on the selected port.

5. Be sure the modes on the selected port are 666. If not, change them.

6. Remove any files starting with LCK in /usr/spool/uucp.

3.4.5. Disk Power-Up Procedure

The following paragraphs are the steps to safely apply power to the system drive(s).

The drive is a nonvolatile storage media; therefore, once data is recorded, it is not lost when power is turned off.

Drive status information can be obtained from its status (LED) indicators. Refer to paragraph 3.4.2.5 for Model 21 Plus or paragraph 3.4.2.6 for Model 31 Plus. Also note the file protect information.

CAUTION

Improper orientation of the drive power cable and connector will result in serious damage to the drive.

The following checks must be performed prior to applying power to the system drive(s).

1. Verify the drive power cable and connection before applying power to the disk drive.

NOTE

Step 2 only applies to the Model 31 Plus.

2. Verify the head locking actuator lever for the Model 31 Plus drive is in the FREE position (refer to Figure 3-3).

3. Apply power to the drive. (The actuator mechanism performs the first seek operation in less than one minute; the R/W heads move from the landing area into the data area of the disk). Continue with paragraph 3.4.6, System Power-Up Diagnostics (SPUD).

3.4.6. System Power-Up Diagnostics (SPUD)

The System Power-Up Diagnostics (SPUD) reside in Read Only Memory (ROM) on the CPU board. When system power is applied (Power switch turned ON. Front panel key turned ON), SPUD automatically executes when pressing RESET and START.

SPUD can also be initiated from the CPU monitor by pressing RESET and entering T <CARRIAGE RETURN>.

SPUD tests the primary functions of the CPU and peripheral components. Its test verifies the system's ability to execute a limited number of instructions and to communicate with the disk drive and Tape Cartridge Controller.

The specific functions of SPUD are:

1. System 8000 Instruction Test - Specified system instructions are tested.

2. MMU Test - All accessible internal registers and the segment trap functions are tested.

3. Memory Test - All memory locations are tested for read and write functions.

4. ECC Memory Test - Tests the system's error detection capabilities.

5. Peripheral Equipment Test - Does a cursory check of the disk drive and Tape Cartridge Controller, Nine-Track, ICP, and Secondary Serial Board(s).

The system console (tty labeled "console") displays a message indicating the state of the memory management jumpers on the CPU board is segmented. System error messages are sent to the console.

NOTE

For a baud rate configuration verification, refer to Section 4, Table 4-12. Refer to the ZEUS Administrator Manual for booting and initializing the system.

If SPUD detects a system problem, an error message is displayed on the tty labeled "console" for the system administrator (ZEUS super-user).

Appendix E provides a list of the possible error messages and descriptions.

NOTE

The following should NOT be attempted until ac power is removed from the system. Refer to Section 5 of this manual for ac power removal.

A possible solution to a power-up error condition may be that the connectors are not properly mated. Verify that all system boards are properly seated in their backplane connectors. Return to paragraph 3.3.2.2 for a visual inspection check.

CAUTION

IF an incorrect SADIE diagnostic is run, it can be DATA-DESTRUCTIVE and result in overwriting the disk media. Be sure that the correct diagnostic is run on the system.

If a problem still exists, run the Stand-Alone Diagnostic Interactive Executive (SADIE) diagnostic programs. Refer to the SADIE Reference Manual, or contact Zilog Field Service for technical assistance.

SECTION 4
THEORY OF OPERATION

4.1. General

This section provides an overview of the Zilog System 8000 its functional application and its overall operation. The following subsections provide detailed information about

Z-BUS Backplane Interconnect Overview - which includes:

- ZBI Conventions
- ZBI Control Signals
- ZBI and Z-BUS Component Interconnection - which includes:

    CPU Interconnect

    CPU Board

    CPU I/O

    mini Winchester Disk Controller-11 Interconnect

    Storage Module Device Controller Interconnect

    Tape Cartridge Controller Interconnect

    ECC Memory Subsystem Controller

System Reset

Non-Maskable Interrupts (NMI)

Vectored Interrupts

Memory Management Unit (MMU) - which includes:

    Segmented Operation

    MMU Configurations

    Break Registers

    User Segment Access

    System Segments and Protection

4.2. Z-Bus Backplane Interconnect (ZBI) Overview

Figure 4-1 identifies the major components of the system connected to the 32-bit Z-Bus Backplane Interconnect (ZBI) system. The ZBI is an application oriented system bus on which all communications with the system components take place. The ZBI is located on the card cage backplane, and connected to connectors J11 through J20. (The logic diagrams and assembly drawings for the printed circuit boards show the signal line connections of the ZBI to the P1 connectors.)

The CPU is the ZBI system bus controller (refer to paragraph 4.2.3.1 for CPU Interconnect).

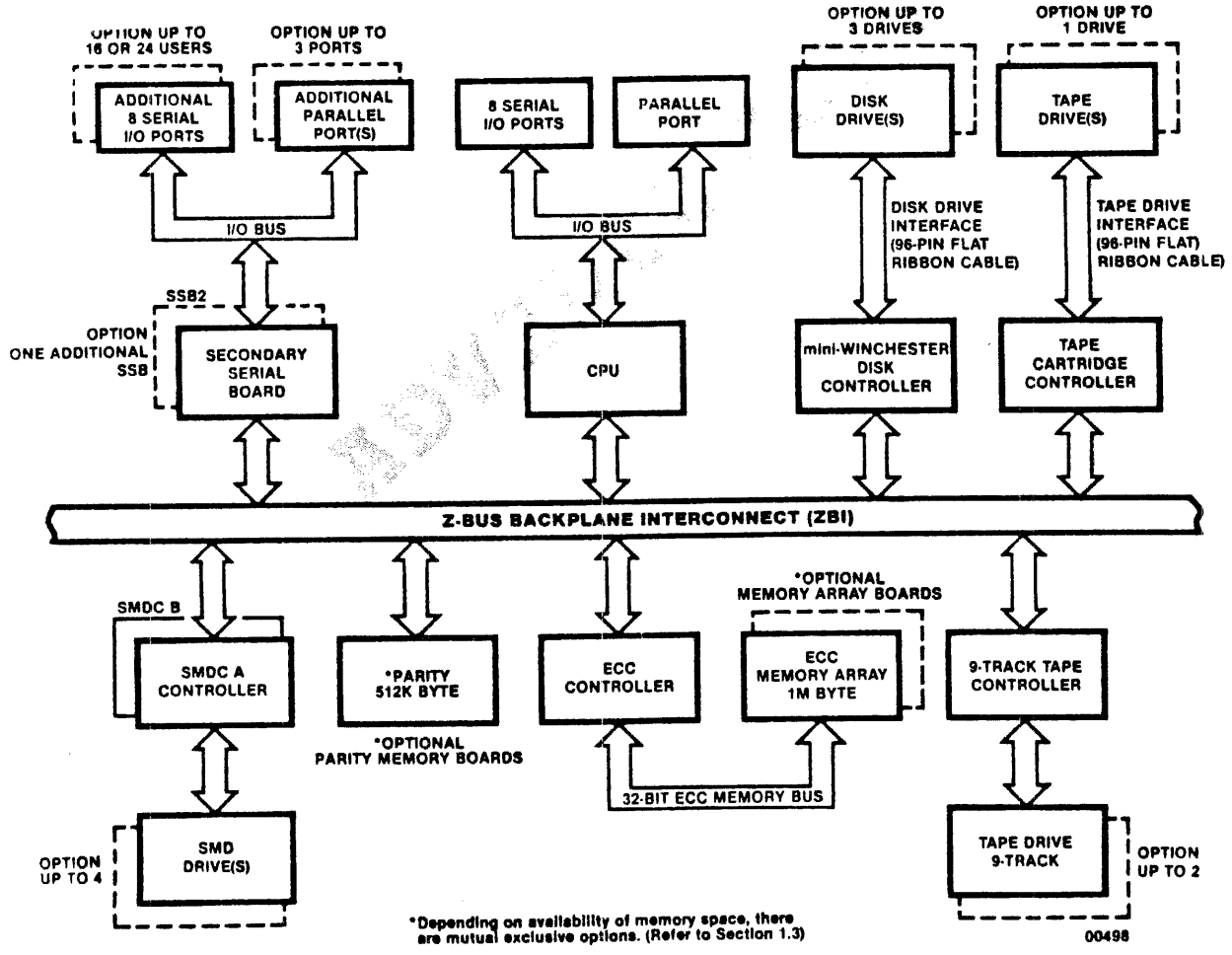


Figure 4-1 Zilog System 8000 ZBI Functional Relationships

4.2.1. ZBI Conventions

ZBI signals may be active in either a high or a low state. All signals that use the bus have names or mnemonics that identify them, and they also indicate the active state of the signal. (Refer to Appendix B for Mnemonics listing.) For example, the signal AS\ (Address Strobe) is an active low signal because it has a backslash appended to it.

If the signal appears as AS with no backslash, it is active high. The backslash is the same notation as the overbar that indicates the logical complement of a signal.

NOTE

Throughout this section, note that an H denotes hexadecimal value.

Active low signals can also have a minus sign appended to them as in AS-. The overbar, the backslash, and the minus sign all mean the same thing. This publication makes use of the backslash. Some of the drawings use either the overbar or the minus sign (-).

4.2.2. ZBI Control Signals

Table 4-1 lists and defines the ZBI signal lines. One signal name can designate more than one signal line. In this case, the signal name is followed by numbers in angle brackets (<>) which indicate the quantity of lines and their designations.

As an example, the signal designated AD<31:Ø> is the name for the 32 address and data lines (ADØ through AD31) that are part of the bus. Within the angled brackets, the 31 indicates the most significant line.

The status lines, ST<4:Ø>, and the data width lines, B/W\ and W/LW\, form specific codes that cause a number of discrete operations to occur.

Tables 4-2 and 4-3 list the various codes on the status and data width lines respectively, and the operations the codes initiate.

Table 4-1 Bus Signal Lines

SIGNAL NAME/ MNEMONIC	NUMBER OF LINES	FUNCTION
AD<31:Ø>	32	Multiplexed Address/Data lines: These lines are driven by the bus master. The Address Strobe (AS\) and Data Strobe (DS\) determine when the information on these lines is valid.
ME\	1	Memory Error: During a memory access, if the memory controller detects an uncorrectable error, the controller sends the ME\ signal to the bus master.
ST<4:Ø>	5	Status Lines: These active high lines indicate the type of transaction currently occurring on the bus. (Refer to Table 4-2 for the various codings and their associated transactions).
R/W	1	Read-Write: When this line is high, the current operation is a read; when this line is low, the operation is a write.
N/S\	1	Normal-System: Indicates the mode of operation of the master which is currently controlling the bus.
B/W\	1	Byte-Word Select: This signal is used with signal W/LW\ to define the data access width (refer to Table 4-3 for coding).
W/LW\	1	Word/Long Word Select: This signal is used with signal B/W\ to define the data access width (refer to Table 4-3 for coding).

Table 4-1 Bus Signal Lines (continued)

SIGNAL NAME/ MNEMONIC	NUMBER OF LINES	FUNCTION
AS\	1	Address Strobe The bus master drives this line low to initiate a bus transaction. The rising/trailing edge indicates that the current address and status are valid.
DS\	1	Data Strobe The bus master uses this signal to time the movement of data to and from itself along the data bus.
WAIT\	1	Wait: By forcing this line low, a bus slave causes the bus master to suspend operation while the slave completes its activity.
STOP\	1	Stop Line: This line, when driven low by an EPU device, causes a Z8000 CPU to generate null transactions. During a null transaction, the data strobe (DS\) remains high.
BAI\	1	Bus Acknowledge In: This signal along with BAO\ forms the bus priority chain.
BAO\	1	Bus Acknowledge Out: This signal, along with BAI\ forms the bus priority chain.
BUSREQ\	1	Bus Request: A module uses the BUSREQ\ signal to gain access to the bus. This signal is part of the priority scheme that is set up by the connection of signals BAI\ and BAO\.

Table 4-1 Bus Signal Lines (continued)

SIGNAL NAME/ MNEMONIC	NUMBER OF LINES	FUNCTION
CAI\	1	CPU Acknowledge In: Not currently implemented, the CAI, CAO, CPUREQ, and CAVAIL signals are designed to allow multiple CPUs to share a single bus.
CAO\	1	CPU Acknowledge Out: Not currently implemented--reserved
CPUREQ\	1	CPU Request: Not currently implemented--reserved
CAVAIL	1	CPU Available: Not currently implemented--reserved
INT1\	1	Level-1 Interrupt: This is the highest priority interrupt in the system. When driven by a slave, it generates a Non-Maskable Interrupt (NMI). The front panel START button also generates one.
INT2\	1	Level-2 Interrupt: This is the second to the highest priority interrupt in the system. When driven by a slave, it generates a vectored interrupt.
INT3\	1	Level-3 Interrupt: This is the lowest priority interrupt in the system. When driven by a slave, it generates a non-vectored interrupt.

Table 4-1 Bus Signal Lines (continued)

SIGNAL NAME/ MNEMONIC	NUMBER OF LINES	FUNCTION
IEI1	1	Level-1 Interrupt Enable In: This signal works with Level-1 Interrupt Enable Out to form the NMI acknowledge daisy-chain.
IEO1	1	Level-1 Interrupt Enable Out.
IEI2	1	Level-2 Interrupt Enable In: This signal works with Level-2 Interrupt Enable Out to form the VI acknowledge daisy-chain.
IEO2	1	Level-2 Interrupt Enable Out.
IEI3	1	Level-3 Interrupt Enable In: This signal works with Level-3 Interrupt Enable Out to form the NVI acknowledge daisy-chain.
IEO3	1	Level-3 Interrupt Enable Out.
MMREQ\	1	Multi-micro Request: When this signal is active a module can request the use of a common resource. The MMREQ\ signal works with signals MMAI\ and MMAO\.
MMAI\	1	Multi-micro Acknowledge In: This signal works with signal MMAO\ to form the resource-request daisy-chain.
MMAO\	1	Multi-micro Acknowledge Out: This signal works with signal MMAI\ to form the resource-request daisy-chain.

Table 4-1 Bus Signal Lines (continued)

SIGNAL NAME/ MNEMONIC	NUMBER OF LINES	FUNCTION
PWRBAD\	1	Power Bad: The processor power supply generates this as an early warning to the system that the dc power will soon fall below the minimum TTL power requirements.
MCLK	1	Master Clock: This signal is the system clock and is the foundation for all timing in the system. The frequency of the MCLK signal is four times that of the Bus clock (BCLK).
BCLK	1	Bus Clock: The system derives this clock from the Master Clock (MCLK). The BCLK is one fourth the frequency of the Master Clock and synchronizes the operation of the elements in the system that require synchronization. All bus transfers are synchronized to this clock. The system CPU board is the generator of this clock and MCLK above.
RESET\	1	Reset: The master RESET signal for the entire system. This signal is generated by the front panel master reset switch or during power-up by the power-up reset circuit. When it is forced low, it initializes the entire system.

Table 4-2 ZBI Status Lines Transaction Coding

S	S	S	S	S	TRANSACTION
Ø	Ø	Ø	Ø	Ø	Internal operation
Ø	Ø	Ø	Ø	1	Memory refresh
Ø	Ø	Ø	1	Ø	I/O reference
Ø	Ø	Ø	1	1	Special I/O reference
Ø	Ø	1	Ø	Ø	Segment trap acknowledge
Ø	Ø	1	Ø	1	INT 1 Interrupt acknowledge
Ø	Ø	1	1	Ø	INT 3 Interrupt acknowledge
Ø	Ø	1	1	1	INT 2 Interrupt acknowledge
Ø	1	Ø	Ø	Ø	Data memory request
Ø	1	Ø	Ø	1	Stack memory request
Ø	1	Ø	1	Ø	Transfer between data memory and an EPU
Ø	1	Ø	1	1	Transfer between stack memory and an EPU
Ø	1	1	Ø	Ø	Program reference, nth cycle
Ø	1	1	Ø	1	Program reference, 1st cycle
Ø	1	1	1	Ø	Transfer between CPU and EPU
Ø	1	1	1	1	Reserved
1	X	X	X	X	Reserved

Table 4-3 Data Width Codes: Byte, Word, and Long Word

B/W\	W/LW	DATA WIDTH
1	1	Sets the data width to byte width, 8 bits; data on lines AD<7:Ø>.
Ø	1	Sets data width to word size, 16 bits; data on lines AD<15:Ø>.
1	Ø	Sets data width to double-word size, 32 bits; data on lines AD<31:Ø>.
Ø	Ø	Reserved.

4.2.3. ZBI and Z-BUS Component Interconnection

The system modules communicate directly with the CPU over the ZBI with one exception, the ECC Memory array. This array communicates to the bus through the Memory Subsystem Controller. The following paragraphs describe the individual system module interfaces to the ZBI.

4.2.3.1. CPU Interconnect: The CPU is the I/O bus controlling device, and is sometimes referred to as the host. The CPU (refer to Figure 4-2) at P2/J21 connects directly to and controls the I/O bus. All other transactions pass through either the parallel port or one of the eight serial I/O ports. Table 4-4 lists the CPU I/O bus signals and their definitions.

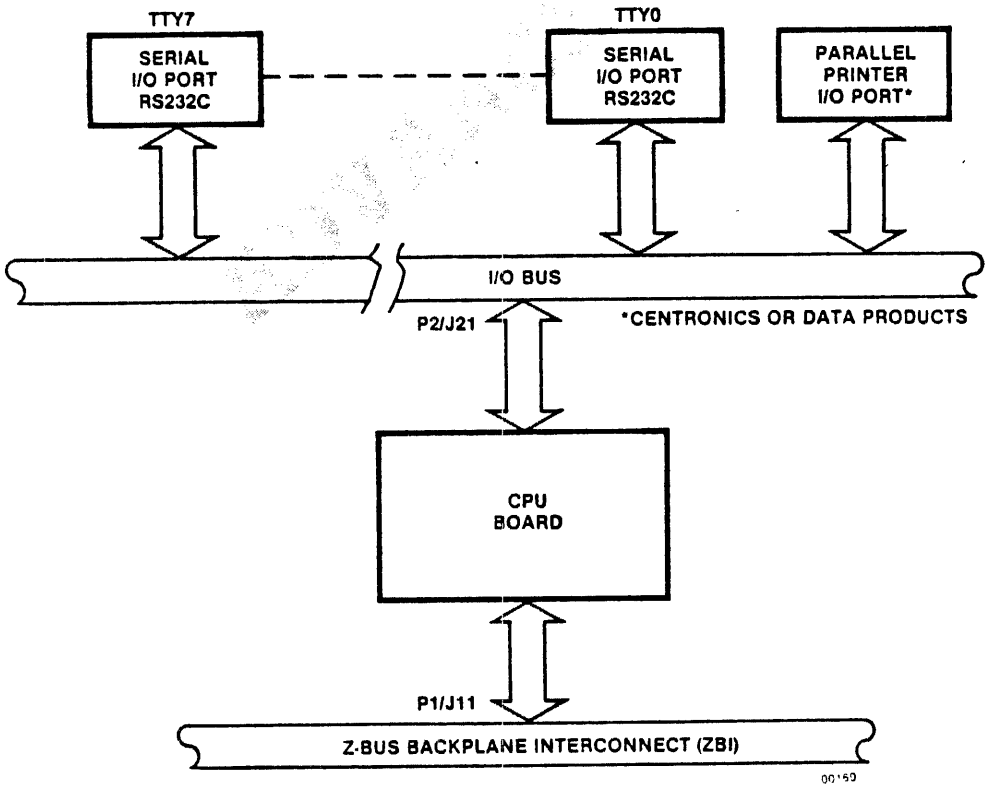


Figure 4-2 CPU Board Functional Diagram

Table 4-4 CPU I/O Bus Signal Definitions

SIGNAL NAME	DEFINITION
TXD7 to TXDØ	Transmit Data
RXD7 to RXDØ	Receive Data
CTS7 to CTSØ	Clear To Send
DTR7 to DTRØ	Data Terminal Ready
RTS7 to RTSØ	Request To Send
DSR7 to DSRØ	Data Set Ready
TXRTN7 to TXRTNØ	Transmit Return
DATA7 to DATAØ	PIO Data
DATA STROBE	Data Products Data Strobe
DATA STROBE\	Centronics* Data Strobe, Active Low
DATA DEMAND/ ACKNOWLEDGE\	Demand (Data Products*) Active High Acknowledge (Centronics*) Active Low
BUSY\	Printer Busy, Active Low
IFVALID\	Interface Valid (Data Products*), Active Low
FAULT\	Paper Empty Indication (Centronics*), Active Low
ON-LINE/SELECT	ON-LINE (Data Products*), SELECT (Centronics*)
BUSACK INDICATOR	DMA In Process Disk or Tape Controller In
POWER-ON INDICATOR (Gnd)	Ground For Power-On Indicator

*** Hardware Jumpers can be set for either Centronics (factory default) or Data Products printer interface. (Refer to Table 4-6.)**

Table 4-4 CPU I/O Bus Signal Definitions (continued)

SIGNAL NAME	DEFINITION
POWER-ON INDICATOR V+	Indicates System Is On
NORMAL INDICATOR	CPU Running User Process
SWITCH N.C. START	Auto Boot
SWITCH N.O START	Auto Boot
SWITCH RESET	Resets System

4.2.3.2. CPU Board: The CPU board is configured for a segmented operating system with ZEUS 3.2 or higher. Refer to Table 4-5. The CPU board is software supported and should not be re-configured in the field.

Table 4-5 CPU Board Jumper Selection

E1 to E2 E5 to E6 E8 to E9 E1Ø to E12

4.2.3.3 CPU I/O: The CPU board contains the devices that control both the serial and parallel I/Os. These devices form eight serial I/O channels and one parallel I/O channel.

The serial channels support the RS-232C standard; the parallel ports can be configured for either the Data Products or Centronics (factory default for Centronics). One parallel port, Port B of a Z8Ø-PIO, is the data-out port; parallel Port A handles status and control information.

The CPU board can be set for a Centronics or Data Products interface (factory default is Centronics interface). Connect jumpers E13 through E18 as shown in Table 4-6.

Table 4-7 provides the control signals for the parallel printers (Port A). Table 4-8 provides the printer's status signals (Port A). Table 4-9 lists the data output of Port B. Serial I/O comprises four Z8ØB-SIO/2 devices. Each device has two channels. Table 4-1Ø lists the devices and their assigned channels.

Table 4-6 CPU Interface Settings

CENTRONICS INERFACE	DATA PROCUCTS INTERFACE
E13 to E14	E14 to E15
E17 to E18	E16 to E17

Table 4-7 Parallel Printer Output Control Signals, Port A

BIT NUMBER	CENTRONICS	DATA PRODUCTS
Ø	Data Strobe	Data Strobe
1	Not used	Not used
2	Not used	Not used
3	Not used	Not used

Table 4-8 Parallel Printer Input Status Signals, Port A

BIT NUMBER	CENTRONICS	DATA PRODUCTS
4	Busy	Busy
5	Select	Online
6	Fault	Interface Valid
7	Acknowledge	Data Demand

Table 4-9 Paralled Printer Data, Port B

BIT NUMBER	CENTRONICS	DATA PRODUCTS
Bit Ø	Data Bit Ø	Data Bit Ø
Bit 1	Data Bit 1	Data Bit 1
Bit 2	Data Bit 2	Data Bit 2
Bit 3	Data Bit 3	Data Bit 3
Bit 4	Data Bit 4	Data Bit 4
Bit 5	Data Bit 5	Data Bit 5
Bit 6	Data Bit 6	Data Bit 6

Table 4-1Ø Serial I/O Devices and Channel Assignments

DEVICE NUMBER	CHANNEL ASSIGNMENT
U93 Ø	Channels Ø and 1 (Console is 1)
U93 1	Channels 2 and 3
U93 2	Channels 4 and 5
U93 3	Channels 6 and 7

Each channel of the serial I/O connects to its own baud rate generator. These generators are channels in Z8ØB-CTC devices. The SIO channels and their corresponding baud rate generators are listed in Table 4-11.

The baud rate clock comes from an independent baud rate oscillator. The frequency of the baud rate clock is 1.2288 megahertz.

Table 4-11 Serial Channels and Baud Rate Generators

IO	SIO CHANNELS	BAUD NO.	CTC NO.	CTC CHANNELS
Ø	Ø	Ø	Ø	Ø
Ø	1	1	Ø	1
1	2	2	Ø	2
1	3	3	1	Ø
2	4	4	1	1
2	5	5	1	2
3	6	6	2	Ø
3	7	7	2	1

The console serial channel baud rate selection is identical to every other serial channel except the on-board monitor on the CPU board. It uses channel 1 to communicate with the system operator when the system is turned on.

The initial baud rate for channel 1 is factory set for 96ØØ by switch U7Ø. It can be set to one of the four values listed in Table 4-12. These settings permit the use of a variety of terminals as the system console.

After the system has been booted, the console baud rate can be changed under software control.

The 4-pole DIP switch on the CPU board selects the primary boot device, setting the baud rate for the monitor console.

The primary boot device will always be listed and tested first by the SPUD Diagnostics (reference Appendix E).

Table 4-12 CPU Setting

SWITCH 1, 4	BAUD RATE	SWITCH 2, 3	PRIMARY BOOT DEVICE
ON ON	300 Baud	OFF OFF	8" Disk (Model 31 Plus)
OFF ON	1200 Baud	ON OFF	5.25" Disk (Model 21 Plus)
ON OFF	9600 Baud	OFF ON	SMDC (Model 31 Plus)
OFF OFF	19200 Baud	ON ON	Reserved

System software accesses the I/O channels using standard Z8000 I/O instructions. Table 4-13 lists the CPU I/O addresses of the I/O channels, SSB I/O addresses are also included. The CPU address FFE1 is decoded by the hardware for one generation of Z80 RETI instruction.

Table 4-14 identifies the system I/O space allocations, including device type and its current use.

Table 4-13 I/O Channels and Their Addresses

CPU I/O ADDRESS	I/O DEVICE AND CHANNEL
FF81	SIO Ø, channel Ø, data
FF83	SIO Ø, channel 1, data
FF85	SIO Ø, channel Ø, control
FF87	SIO Ø, channel 1, control
FF89	SIO 1, channel 2, data
FF8B	SIO 1, channel 3, data
FF8D	SIO 1, channel 2, control
FF8F	SIO 1, channel 3, control
FF91	SIO 2, channel 4, data
FF93	SIO 2, channel 5, data
FF95	SIO 2, channel 4, control
FF97	SIO 2, channel 5, control
FF99	SIO 3, channel 6, data
FF9B	SIO 3, channel 7, data
FF9D	SIO 3, channel 6, control
FF9F	SIO 3, channel 7, control
FFA1	CTC Ø, channel Ø (baud Ø for SIO Ø, channel Ø)
FFA3	CTC Ø, channel 1 (baud 1 for SIO 1, channel 1)
FFA5	CTC Ø, channel 2 (baud 2 for SIO 1, channel 2)
FFA7	CTC Ø, channel 3
FFA9	CTC 1, channel Ø (baud 3 for SIO 1, channel 3)
FFAB	CTC 1, channel 1 (baud 4 for SIO 2, channel 4)
FFAD	CTC 1, channel 2 (baud 5 for SIO 2, channel 5)
FFAF	CTC 1, channel 3
FFB1	CTC 2, channel Ø (baud 6 for SIO 3, channel 6)
FFB3	CTC 2, channel 1 (baud 7 for SIO 3, channel 7)
FFB5	CTC 2, channel 2
FFB7	CTC 2, channel 3
FFB9	PIO Ø, channel A, data
FFBD	PIO Ø, channel A, control
FFBB	PIO Ø, channel B, data
FFBF	PIO Ø, channel B, control
FFC1	SCR, read/write, System Configuration Register
FFC9	SBR, read/write, System Break Register
FFD1	NBR, read/write, Normal Break Register

(continued)

Table 4-13 I/O Channels and Their Addresses (continued)

CPU I/O ADDRESS	I/O DEVICE AND CHANNEL (continued)
FFD9	SVR, read segment trap segment address
FFE1	Z8Ø RETI, return from interrupt
FFE9	Soft Reset
FFF1	Low-Byte Register, read segment trap low-byte address
FFF9	Low-Byte Register, read segment trap IF1 low-byte

SSB I/O ADDRESS	I/O DEVICE AND CHANNEL
FFØ1	DART Ø, channel 16, data
FFØ3	DART Ø, channel 17, data
FFØ5	DART Ø, channel 16, control
FFØ7	DART Ø, channel 17, control
FFØ9	DART 1, channel 18, data
FFØB	DART 1, channel 19, data
FFØD	DART 1, channel 18, control
FFØF	DART 1, channel 19, control
FF11	DART 2, channel 2Ø, data
FF13	DART 2, channel 21, data
FF15	DART 2, channel 2Ø, control
FF17	DART 2, channel 21, control
FF19	DART 3, channel 22, data
FF1B	DART 3, channel 23, data
FF1D	DART 3, channel 22, control
FF1F	DART 3, channel 23, control
FF21	CTC Ø, channel Ø, (baud Ø for DART Ø, channel 16)
FF23	CTC Ø, channel 1, (baud 1 for DART Ø, channel 17)
FF25	CTC Ø, channel 2, (baud 2 for DART 1, channel 18)
FF27	CTC Ø, channel 3, unusable
FF29	CTC 1, channel Ø, (baud Ø for DART 1), channel 19)
FF2B	CTC 1, channel 1, (baud 3 for DART 2), channel 2Ø)
FF2D	CTC 1, channel 2, (baud 4 for DART 2), channel 21)
FF2F	CTC 1, channel 3, Unused single rank

(continued)

Table 4-13 I/O Channels and Their Addresses (continued)

SSB I/O ADDRESS	I/O DEVICE AND CHANNEL (continued)
FF31	CTC 2, channel Ø, (baud 6 for DART 3, channel 22)
FF33	CTC 2, channel 1, (baud 7 for DART 3, channel 23)
FF35	CTC 2, channel 2, unused double rank (chained)
FF37	CTC 2, channel 3, unused double rank (chained)
FF39	PIO Ø, channel A, data (3rd printer I/O control)
FF3B	PIO Ø, channel B, data (printer data I/O)
FF3D	PIO Ø, channel A, control (3rd printer data I/O)
FF3F	PIO Ø, channel B, control (printer data I/O)
FF41	DART Ø, channel 8, data
FF43	DART Ø, channel 9, data
FF45	DART Ø, channel 8, control
FF47	DART Ø, channel 9, control
FF49	DART 1, channel 1Ø, data
FF4B	DART 1, channel 11, data
FF4D	DART 1, channel 1Ø, control
FF4F	DART 1, channel 11, control
FF51	DART 2, channel 12, data
FF53	DART 2, channel 13, data
FF55	DART 2, channel 12, data
FF57	DART 2, channel 13, control
FF59	DART 3, channel 14, data
FF5B	DART 3, channel 15, data
FF5D	DART 3, channel 14, control
FF5F	DART 3, channel 15, control
FF61	CTC Ø, channel Ø, (baud Ø for DART Ø, channel 8)
FF63	CTC Ø, channel 1, (baud 1 for DART Ø, channel 9)
FF65	CTC Ø, channel 2, (baud 2 for DART 1, channel 1Ø)
FF67	CTC Ø, channel 3, unusable
FF69	CTC 1, channel Ø, (baud 3 for DART 1, channel 11)
FF6B	CTC 1, channel 1, (baud 4 for DART 2, channel 12)
FF6D	CTC 1, channel 2, (baud 5 for DART 3, channel 13)
FF6F	CTC 1, channel 3, unused single rank

(continued)

Table 4-13 I/O Channels and Their Addresses (continued)

SSB I/O ADDRESS	I/O DEVICE AND CHANNEL
FF71	CTC 2, channel Ø, (baud 6 for DART 3, channel 14)
FF73	CTC 2, channel 1, (baud 7 for DART 3, channel 15)
FF75	CTC 2, channel 2, unused double rank (chained)
FF77	CTC 2, channel 3, unused double rank (chained)
FF79	CTC Ø, channel A, data (Printer Control I/O)
FE7B	PIO Ø, channel A, control (Printer Control I/Ø)
FF7D	PIO Ø, channel B, data (Printer data I/O)
FF7F	PIO Ø, channel B, control (Printer data I/O)
FFEØ	Return from interrupt

Table 4-14 System I/O Space Allocations

I/O Space	Device Class	Current Use
ØØØØ - ØØ3F	Memory Devices	ECC ØØØØ - ØØØ3
ØØ4Ø - ØØ7F	Tape	TCU ØØ4Ø - ØØ4F
ØØ8Ø - OFFF	Other Memory Devices	None
1ØØØ - 1FFF	Tape Devices	9-Track 1ØØØ - 1Ø1F
2ØØØ - 2ØØF	Reserved	
2Ø1Ø - 6FFF	Reserved	
7ØØØ - 8FFF	Disk Devices:	
	SMD (Model 31 Plus)	7FFØ - 7FFF
	mWDC-II (Model 21 Plus)	8ØØØ - 8ØFF
9ØØØ - 9FFF	Available to User	
AØØØ - ØFFF	Reserved	
EØØØ - FFFF	Communication Devices:	
	CPU	FFC1 - FFFF
	ICP	EFØ1 - EFØF
	SSB	FF41 - FF7F
	SSB	FFØ1 - FF3F

4.2.3.4. mini Winchester Disk Controller-II Interconnect: The mini Winchester Disk Controller-II (mWDC-II) board is an intelligent controller for the 5 1/4-inch Winchester disk drive. The mWCD-II uses the MFM encoding method for data recording. Figure 4-3 shows the preamble and postamble format of the data field generated by the mWDC-II.

The mWDC-II controls the fully buffered transfer of data between the CPU (host) and the 5 1/4-inch drive. The block diagram in Figure 4-4 shows the relationship between the controller, the ZBI, and the disk drives.

All transactions between the controller and the host pass through the 96-pin connectors P1 and J13 and over the ZBI. Transactions between the controller and a selected disk drive pass through connectors P2 and J23. Data signals are cabled to the drives from the backplane connectors. Control signals are cabled to the drives from the 34-pin, daisy chain connector, J6.

The mWDC-II features a 16-bit Z8001A microprocessor for off-loading the host processor of mass storage I/O management. The mWDC-II monitors intelligent control of the mass storage subsystem while also providing data transfer between the host main memory and the drives. Control of disk drives is by a flexible command set. System level commands include:

FORMAT TRACK
READ MULTISECTOR (with implicit seek)
WRITE MULTISECTOR (with implicit seek)
EXPLICIT SEEK
RECALIBRATE DRIVE
READ DRIVE PARAMETERS
READ SECTOR SPARING MAP
TEST DRIVE READY

The paragraphs that follow describe:

- Drive Configuration
- Drive Interface
- Command Packet Buffer

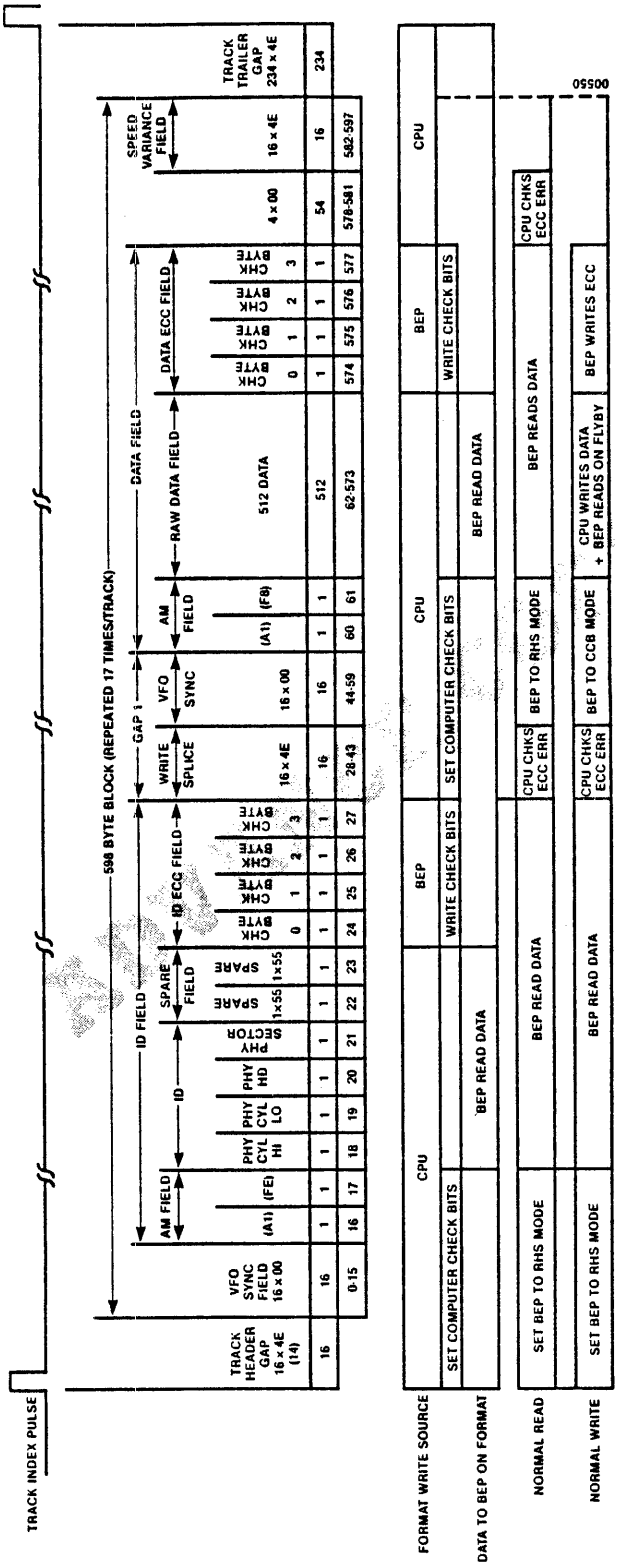


Figure 4-3 mWDC-II Data Field

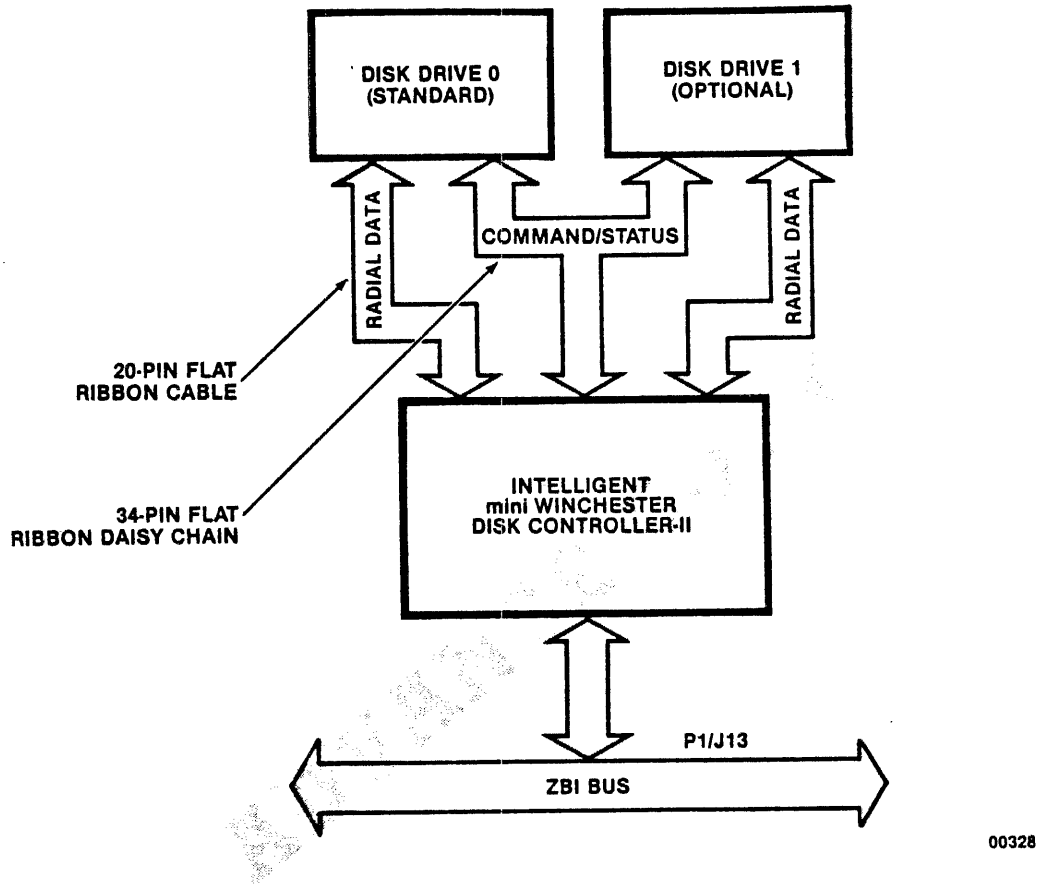


Figure 4-4 mini Winchester Disk Controller-II, Functional Relationships

The controller performs a retry-recovery sequence after not finding a sector and returns the appropriate error status at completion of the command. The controller buffers one command per unit drive at any one time. Detailed completion status is returned to the host at the end of each operation.

Drive Configuration

CAUTION

The configuration switch is factory set for the units shipped. Do not change these settings.

Two 8-bit DIP configuration switches SW2 and SW3 on the mWDC-II board can support up to four drives (Figure 4-5). Bit assignments and the corresponding drive types for switch SW2 and SW3 are shown in Figure 4-5.

TO BE SUPPLIED

Figure 4-5 Disk Drive Switch Settings

Drive Interface

Communications between the mWDC-II and the drive travel over the P2/J23 mating connectors. Control and data (drive) signals are taken from its slot and placed on the backplane connector and selected drive data connector. These connectors are then cabled to the control and data connectors on the drive. Table 4-15 lists and defines the signals on these lines.

The paragraphs that follows contains the controller command set descriptions for the command opcodes that control the bus between the mWDC-II and the drive.

Table 4-15 mWDC-II and Drive Interface Signals

SIGNAL NAME	FUNCTION
REDUCED WRITE CURRENT\	This line, when active low together with WRITE GATE, causes the write circuitry to write on disk with a lower write current.
WRITE GATE\	This signal, when active low, enables write data to be written on the disk. The inactive state of this signal enables data to be read from disk.
HEAD SELECT 2\	These three lines allow selection of each read/write head in a binary coded sequence. HEAD SELECT 2\ is the least significant line. Heads are numbered Ø through 7. When all Head Select lines are high (inactive) Head 7 will be selected.
DIRECTION IN\	This signal determines the direction of motion of the R/W head when the STEP line is pulsed. When low, the direction of motion is in toward the center of the disk. When high, the direction of motion is away from the center of the disk.

(continued)

Table 4-15 mWDC-II and Disk Drive Interface Signals (continued)

SIGNAL NAME	FUNCTION
STEP\	The control signal moves the R/W heads in the direction defined by the DIRECTION IN line.
DRIVE SELECT\	These lines, when low, connect the drive to the control signals. All control lines are enabled by their respective DRIVE SELECT.
SEEK COMPLETE\	This line is active (low) when the R/W heads have settled on the final track at the end of a seek. Reading or writing when false (high) results in a fatal error.
TRACK Ø\	This signal will be true only when the drive's R/W heads are positioned at cylinder Ø, the outermost cylinder.
WRITE FAULT\	When active (low), a drive condition exists that may cause improper writing. Further writing and stepping is inhibited at the drive until corrected. WRITE FAULT cannot be reset by the controller until the condition is corrected.
INDEX\	Provided by the drive once every revolution, this normally high signal makes the transition to a low level to indicate the beginning of a track.
READY\	When true together with SEEK COMPLETE, this signal indicates the drive is ready to read, write, or seek and drive signals are valid. When false, all writing and seeking is inhibited.

(continued)

Table 4-15 mWDC-II and Disk Drive Interface Signals (continued)

SIGNAL NAME	FUNCTION
DRIVE SELECTED\	This status line is provided as part of a data cable from J2 to inform the host system of the selection status.
MFM WRITE DATA	When the WRITE GATE signal is active (low), a pair of balanced signals +MFM WRITE DATA and -MFM WRITE DATA are used for the transfer of data. Transition of +MFM WRITE DATA more positive than the -MFM WRITE DATA will cause a flux reversal on the track. In the read mode, +MFM WRITE DATA must be driven more negative than -MFM WRITE DATA.
MFM READ DATA	The data recovered by reading a prerecorded track is transferred to the controller by the differential pair of +MFM READ DATA and -MFM READ DATA. Transition of +MFM READ DATA more positive than -MFM READ DATA represents a flux reversal on the track of the selected head.

Command Packet Buffer

The Command Packet Buffer is a series of command words that reside in main memory at an address specified by the host when generating a software RESET. This series of command words provides the command and parametic inputs to the mWDC-II board.

The command packet buffer is divided into a single dispatch word and a subpacket for each disk drive. Word assignment of the command packet buffer is provided in Table 4-16.

Table 4-18 provides the unit number assignments for the drive.

Table 4-16 mWDC-II Drive Command Packet Buffer

COMMAND WORD	FUNCTION
DWO	Dispatch Word
	SUBPACKET FOR DRIVE Ø
CWØ*	Command Field and Opcode
CW1*	Logical Block Number
CW2*	Transfer Sector Count
CW3*	Transfer Address Bits Ø-15
CW4*	Transfer Address Bits 16-31
CW5*	Status and Interrupt Vector

* CWØ through CW5 describe a single subpacket for a disk unit.

Table 4-17 mWDC-II Drive Unit Numbers

UNIT	DRIVE
Ø	mini-disk
1	mini-disk
2	mini-disk, not used
3	mini-disk, not used
4	not used
5	not used

There are four units and four subpackets each identical to the other except for unit number. The command word and bit descriptions are:

DWØ DISPATCH WORD

MSB	15 . . . 8	7 6	5 4	3 2	1 Ø	LSB
	x --------- x	b a	b a	b a	b a	
	Reserved	Unit 3	Unit 2	Unit 1	Unit Ø	

Bit a = Input from host indicating that the subpacket is ready to be read for the appropriate unit.

Bit b = Output to host indicating a command is pending (command has been read but not yet completed).

Bit x = Reserved, must be zero.

The dispatch word (DWØ) implements a handshake between the controller and the host system. Setting any unit's bit "a" indicates to the controller the command subpacket for the unit is ready to be read.

Bit "b" is set when the controller has finished reading the command subpacket.

The host must not issue a command when bits "a" and "b" are set. Bits "a" and "b" will be cleared by the mWDC-II when the command is complete.

CWØ Command Word (COMMAND FIELD AND OPCODE)

MSB 15 14 x x x 1Ø 9 8 7 x x x x x x Ø LSB
Retry Reserved EI SMD Command Opcode

COMMAND FIELD BITS	FUNCTION
Bit 15	After command completion, if a correctable error occurred, this bit will be a 1. Otherwise, it will always be zero.
Bits 1Ø through 14	Reserved
Bit 9	SMD Mode (Sector Map Disabled)
Bit 8	Enable Interrupt on command complete.

COMMAND OPCODE

Bits Ø through 7	Specific controller command codes are input to the controller through these bits.

CW1 LOGICAL BLOCK NUMBER WORD

Bits Ø through 15	The mWDC-II accepts a 16-bit block number from the host.

CW2 TRANSFER SECTOR / BLOCK COUNT WORD

Bits Ø through 15	The host may pass up to sixteen bits that signify the number of sectors to be transferred. If this will cause a pack overflow, an illegal cylinder error will be returned.

CW3 TRANSFER ADDRESS BITS Ø - 15 WORD

Bits Ø through 15	The host must pass a 24-bit address to the controller for commands involving I/O. This transfer address is the location of the first word of a block of memory allocated for the transfer. The direction of transfer is determined by the command. Read sector moves data from the disk to host memory. Write sector moves data from the host to the disk. These bits are used to pass the low order 16 bits of a 24-bit transfer address.

CW4 TRANSFER ADDRESS BITS 16 - 31 WORD

Bits Ø through 7	These bits are used to pass the high order 8 bits of a 24-bit transfer address (Segment number).
Bits 8 through 15	Reserved for transfer address Bits 24-31.

CW5 STATUS WORD

Bits Ø through 7	Interrupt Vector: Input from host indicating the desired interrupt vector for the current command. (Non-significant if in polled mode.)

Bits 8 through 12 At command completion, the output from the mWDC-II is the completion status code.

BINARY 12 8	COMPLETION CODE
00000	No error
00001	Read abort
00010	Wait abort condition (Fatal)
00011	Parity error during bus transfer
00100	Write fault condition (Fatal)
00101	Seek not complete (Fatal)
00110	Cylinder not found
00111	Drive not selected (Fatal)
01000	Head and/or sector/record not found
01001	Invalid command
01010	No track 0 found (Fatal)
01011	Drive not ready (Fatal)
01100	Bad interrupt generated within mWDC-II
01101	Cylinder 0 defective or greater than 45 bad sectors on disk (Fatal)
01110	Illegal cylinder selected or beyond disk boundry
01111	Burst Error Processor (BEP) error
10000	Soft BEP error
10001	Soft head and/or sector not found
10010	Soft cylinder not found
10011	Soft read abort

Bits 13 through 15 On command completion, the logical unit number

BIT 15	14	13	LOGICAL UNIT
0	0	0	Unit number 0 mini-disk
0	0	1	Unit number 1 mini-disk
0	1	0	Unit number 2 mini-disk, not used
0	1	1	Unit number 3 mini-disk, not used
1	0	0	Reserved
1	0	1	Reserved

Bits 8 - 15 On command input, these bits are normally set by the host to zeros. However, the host may request that only part of the last sector (see CW2) be transferred by setting Bits 8-15 to the number of words to be read from the last sector.

CONTROLLER COMMAND SET

The command set for the mWDC-II is described in Table 4-18 for the following binary command opcodes (Bit 7- Bit Ø).

OPCODE	COMMAND
ØØØØØØØØ LSB	Test Drive Ready
ØØØØØØØ1	Read Drive Parameters
ØØØØØ1Ø1	Read Sector Sparing Map
ØØØ1ØØØØ	Read Multiple Sector
ØØØ1ØØØ1	Write Multiple Sector
ØØØ1ØØ11	Recalibrate Drive
ØØØ1Ø1ØØ	Format Track
ØØØ1Ø1Ø1	Seek

Table 4-18 Command Set Descriptions

COMMAND	DESCRIPTION
TEST DRIVE READY / UNIT/	Test Drive Ready selects the drive and verifies drive ready.
READ DRIVE PARAMETERS /UNIT/ ADDRESS	The host reads the drive parameters at the address specified.
READ SECTOR SPARING MAP /UNIT/ ADDRESS	The host reads the sector sparing map at the address specified.
READ MULTI SECTOR /UNIT/ LOGICAL BLOCK NUMBER / BLOCK COUNT / ADDRESS	Generates an implicit seek. Requires disk address (unit, logical block number) and system buffer address (block count, address).
WRITE MULTI SECTOR /UNIT/ LOGICAL BLOCK NUMBER / BLOCK COUNT / ADDRESS	Generates an implicit seek. Requires disk address (unit, logical block number) and host system buffer address (block count, address).

(continued)

Table 4-18 Command Set Description (continued)

COMMAND	DESCRIPTION
TEST DRIVE READY / UNIT/	Test Drive Ready selects the drive and verifies drive ready.
READ DRIVE PARAMETERS /UNIT/ ADDRESS	The host reads the drive parameters at the address specified.
READ SECTOR SPARING MAP /UNIT/ ADDRESS	The host reads the sector sparing map at the address specified.
READ MULTI SECTOR /UNIT/ LOGICAL BLOCK NUMBER / BLOCK COUNT / ADDRESS	Generates an implicit seek. Requires disk address (unit, logical block number) and system buffer address (block count, address).
WRITE MULTI SECTOR /UNIT/ LOGICAL BLOCK NUMBER / BLOCK COUNT / ADDRESS	Generates an implicit seek. Requires disk address (unit, logical block number) and host system buffer address (block count, address).
RECALIBRATE /UNIT/	Positions drive heads to Track Ø restoring the drive seek logic. Execution is slower than seek command.
FORMAT TRACK / UNIT/ LOGICAL BLOCK NUMBER/ ADDRESS	Format a track designated by target cylinder, head, and sector numbers. The host provides the appropriate format buffer.
SEEK / UNIT / LOGICAL BLOCK NUMBER	The mWDC-II does an explicit seek and read and then compares the cylinder number for the correct cylinder.

4.2.3.5. Storage Module Device Controller (SMDC) Interconnect: The SMDC is a high performance controller that links the ZBI system bus to each drive interface board.

The SMDC consists of two boards, SMDC A and SMDC B, hereinafter referred to as the A board and the B board.

The A board is the ZBI control signal connection to the I/O panel SMD A OUT connector. External cabling to SMD A IN on the Disk/Tape module connects the ZBI signals through a 60-pin SMD A cable I/O connector to the drive interface board.

The B board is the data I/O connection through I/O panel SMD B OUT on the CPU and SMD B IN on the Disk/Tape modules. I/O data to and from the CPU module is provided at the SMD B panel connectors that connect up to four 26-pin SMD B cables directly to the interface of each drive.

Local interface signals between the two boards are cabled on a flat 40-pin cable to the front of both boards.

All drive connections are made by cabling backplane connectors to the SMD A and SMD B I/O connectors on the processor SMD I/O panel and from the I/O panel to the SMD A and SMD B inputs on the Disk/Tape module.

The A board ZBI connection is through P1/J16. Figure 4-6 shows the A and B board's relationship to the system.

All data transfers and I/O addresses are 16 bits. All data addresses are 24 bits. The interrupt vector is programmable by the host CPU.

The paragraphs that follow describe:

- Command Packet Control
- Self Test
- Power-Up
- Dispatch Table
- Commands
- Sector Format

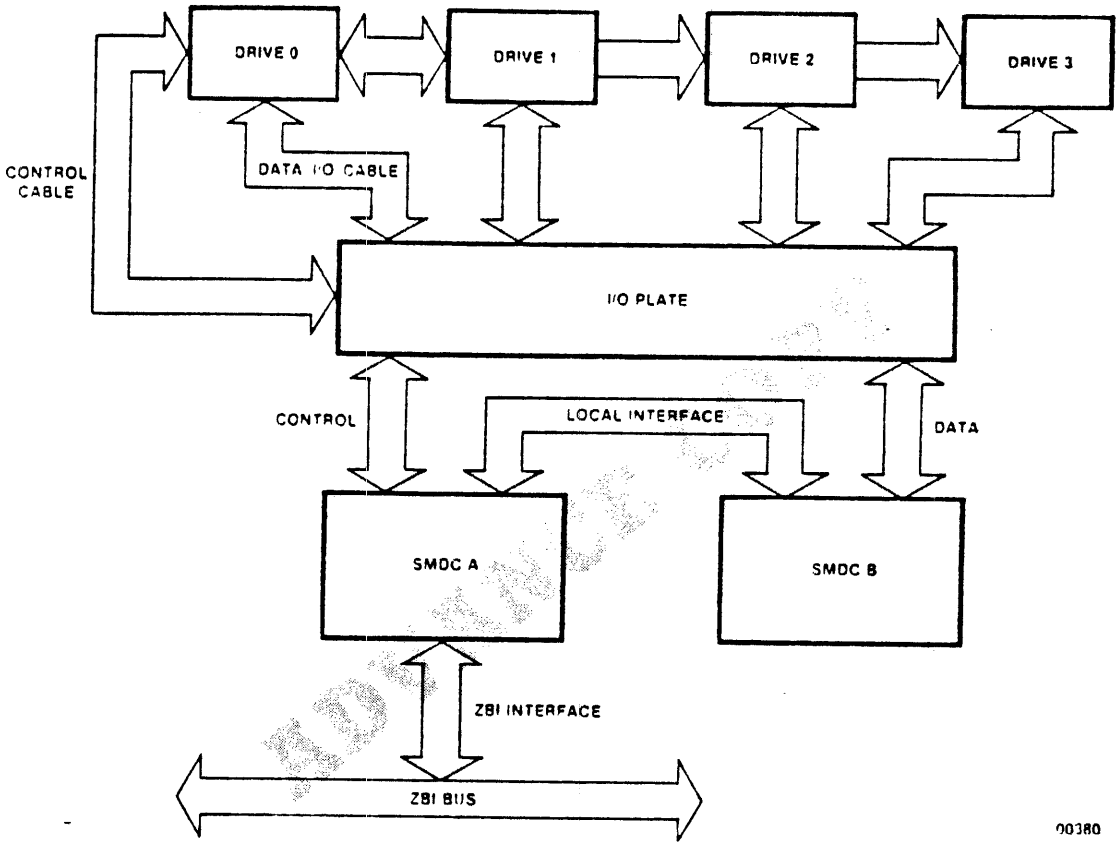


Figure 4-6 SMDC System Configuration

Command Packet Control

Commands are sent to the controller in the form of 32-byte packets that describe the operation to be performed. At any given time, the controller may be executing one command packet for each drive. Upon completion of the command, the packet is written back into main memory and the appropriate status registers are updated.

The controller maintains a separate packet address for each drive. Most commands are sent to the SMDC in a packet of 32 bytes. However, certain information, such as packet address and interrupt controls, are communicated by one 16-bit Write-Only command and one 16-bit Read-Only status register that share a common address (refer to Figure 4-7 and Figure 4-8).

Command Register

15 ... 8	7	6	5	4	3	2	1	Ø
DTA	INIT	RI	DI	EI	WK	CMD		

NAME	BITS	FUNCTION
CR:CMD	Ø-2	COMMAND Ø - NOP 1 - Read packet addresses from DT 2 - Reserved 3 - Reserved 4 - Dispatch table address byte Ø (lsb) ?? 5 - Dispatch table address byte 1 6 - Dispatch table address byte 2 (msb) ?? 7 - Interrupt vector
CR:WK	3	Wake up
CR:EI	4	Enable interrupts (reset by IUS)
CR:DI	5	Disable interrupts
CR:RI	6	Reset IP and IUS
CR:INIT	7	Initialize controller
CR:DTA	8-15	Dispatch table address byte or interrupt vector

Figure 4-7 Command Register Functions

Status Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRV		ES: Ending Status						NDT	Ø	Ø	Ø	Ø	IP	IUS	BZ

NAME	BIT	MEANING
SR:BZ	Ø	Controller busy from CR:CMD
SR:IUS	1	Interrupt under service
SR:IP	2	Interrupt pending
-	3-6	Reserved
SR:NDT	7	No dispatch table/interrupt vector
SR:ES	8-13	Packet ST or self-test code
SR:DRV	14-15	Drive number Ø-3

Figure 4-8 Status Register Functions

Self-Test

On power-up or after controller initialization (CR:INIT), the controller will be busy (SR:BZ) until the self-test routine and initialization are complete.

If the self-test fails, the SMDC will remain busy. The status register (SR:ES) may contain one of the following error codes:

8: 291Ø sequencer error

9: 29Ø1 ALU error

A: Internal memory error

The status register should be examined only after it has been determined that the busy bit was not reset. The self-test takes less than a second when successful.

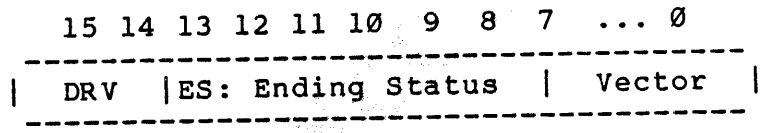
Power-Up

The SMDC's SR:NDT status bit will be on after power-up or controller initialization (CR:INIT). This indicates that the dispatch table address and interrupt vector have not yet been sent by the host (refer to Figure 4-9).

Four bytes are sent with the CR command. After each byte is sent, the controller will briefly be busy (SR:BZ) while the byte is absorbed. The host waits until SR:BZ goes to zero after sending each byte. The READ-PACKET-ADDRESSES command is then given. When all five commands have been given, SR:NDT is reset.

When a PACKET command is complete and the SMDC command register CR:EI bit is set, the SMC interrupts the host.

Interrupt Acknowledge Vector (IV)



IVNAME	BITS	CONTENTS
IV:VEC	0-7	Vector from CR
IV:ES	8-13	Packet command ending status
IV:DRV	14-15	Drive number 0-3

Figure 4-9 Interrupt Acknowledge Vector Functions

Dispatch Table

The dispatch table (refer to Figure 4-10) provides the address and status of each of four packets. If fewer than four drives are present, the dispatch table entries corresponding to nonexistent drives should be present but set to zero.

The dispatch table may not cross a 64K byte boundary. Before the dispatch table address is sent to the controller, all packet status entries should be initialized to IDLE(0), all packets should be initialized to 0.

	15 14 13 12 11 10 9 8 6 5 4 3 2 1 0
ØØ PSØ	Packet Status - Drive Ø
Ø2 PS1	Packet Status - Drive 1
Ø4 PS2	Packet Status - Drive 2
Ø6 PS3	Packet Status - Drive 3
Ø8 PHØ	Packet Address Msh - Drive Ø
ØA PLØ	Packet Address Lsh - Drive Ø
ØC PH1	Packet Address Msh - Drive 1
ØE PL1	Packet Address Lsh - Drive 1
1Ø PH2	Packet Address Msh - Drive 2
12 PL2	Packet Address Lsh - Drive 2
14 PH3	Packet Address Msh - Drive 3
16 PL3	Packet Address Lsh - Drive 3

DT:PS VALUES: Ø = IDLE (set by host)
1 = GO (set by host)
2 = BUSY (set by SMDC)
4 = DONE (set by SMDC)

Figure 4-1Ø Dispatch Table Status

When an operation is to be initiated, the control information must be loaded into the appropriate packet and the corresponding dispatch table status word (DT:PS) set to GO.

A command word is then issued with CR:WK (wakeup) and optionally CR:EI (Enable Interrupt). When the controller is idle, it interrogates the wake up bit, sees it turned on, turns it off, and reads the dispatch table.

Any dispatch table entries with packet status = GO cause the corresponding packets to be read into the SMDC's internal packet tables and DT:PS to be set to Busy.

Internally, seeks are initiated on any drive with an active packet requiring a seek.

When a seek is complete, or if no seek is required (e.g. select command), the command is performed and the packet in host memory is updated with status. The dispatch table status is set to DONE and IP is posted. The host may be scanning SR:IP or waiting for an interrupt with CR:EI set.

Once IP is turned on or the interrupt acknowledged, the host reads SR and then issues CR:RI to reset IP and IUS regardless of whether the interrupts were enabled.

Once IP is reset, the controller may interrupt again. The interrupt enable flag in the controller is reset by CR:DI, which may be issued with CR:RI, if desired.

Ending status and interrupting drive number are made available in the high-order byte of the interrupt vector returned by the controller during an interrupt acknowledge transaction. The drive number is also available in SR:DRV until CR:RI is issued.

Commands

CM defines the current operation by the CMD code (refer to Figure 4-11). Several command modifier flags are shown in Table 4-19.

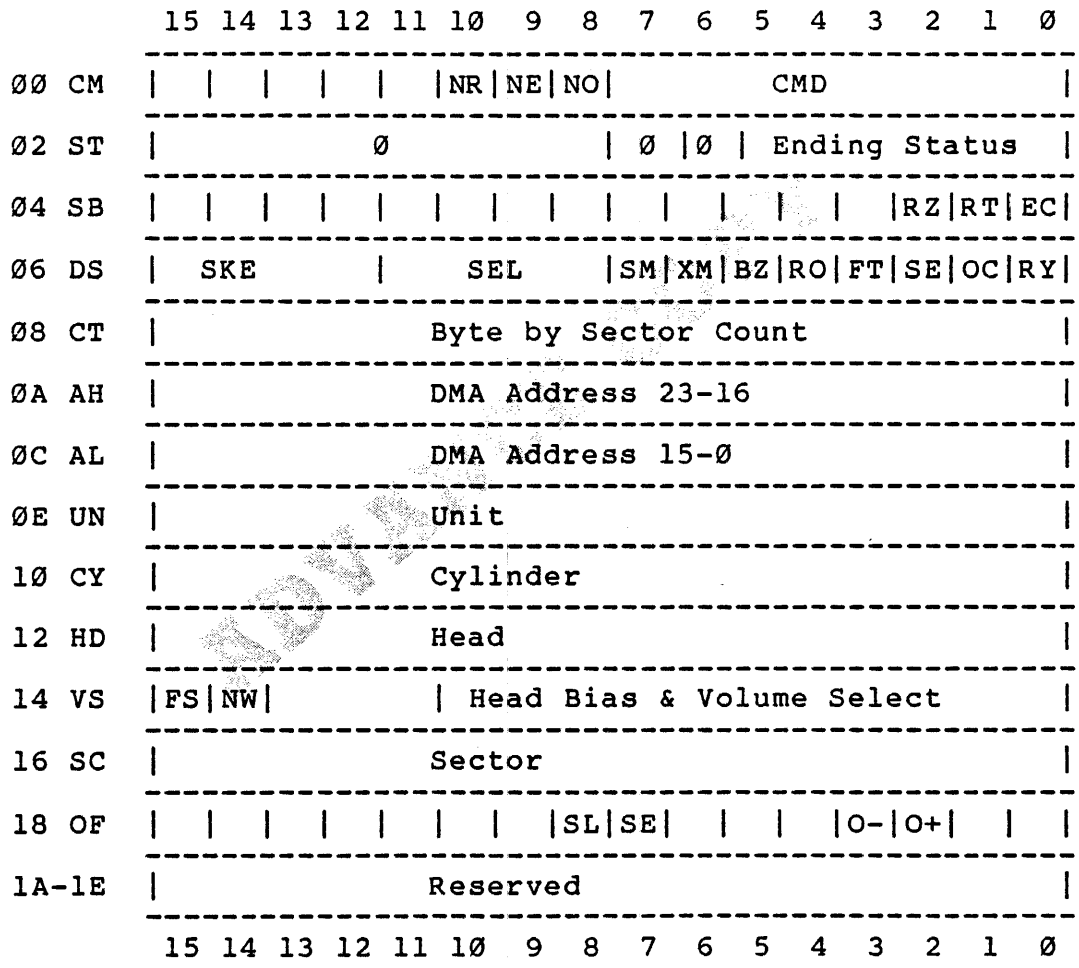


Figure 4-11 Packet Table Status

Table 4-19 CMD Code and Commands

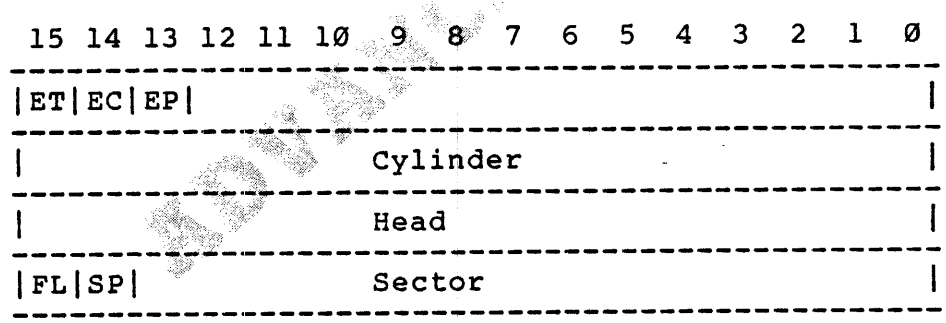
CM:NR: No retries; use OF
CM:NE: No error correction
CM:NO: No offsets during retries
CM:CMD: Ø: NOP
1: Write RAM
2: Read RAM
2: Read RAM
4: Priority select
5: Release
6: Reset fault
7: Position (seek/re-zero)
8: Write format
9: Write long
A: Write
B: Reserved
C: Read format
D: Read long
E: Read
F: Size disk

COMMAND	FUNCTION
NOP	is provided for diagnostic purposes. IP is posted immediately. The microcode revision is returned in CT.
WRITE RAM	copies data from the specified host memory address to the data buffer space of the controller from location Ø up to local variable and packet storage. This is provided for diagnostic purposes.
READ RAM	copies data from controller memory, starting at location Ø, to host memory. This is provided for diagnostic purposes.
SELECT	causes the specified drive to be selected and its status returned in DS.
PRIORITY SELECT	is provided for dual access support.
RELEASE	is provided for dual-access support.
RESET FAULT	is provided for diagnostic and error recovery. A RESET FAULT command is issued to the specified drive.

(continued)

Table 4-19 CMD Code and Commands (continued)

COMMAND	FUNCTION
POSITION	is provided for diagnostic purposes, a seek is performed to the specified cylinder. If reset fault occurs rather than seek.
WRITE FORMAT	initializes the ID and data fields of one or more sectors in a track. The host prepares the IDs contiguously in a buffer, four words per sector. CT is set to the number of sectors to be formatted; SC specifies the starting sector. Sector numbers may be arranged as desired. One or more sectors may be flagged as bad or spare. The sector ID's buffer prepared by the host contains the following four words for each sector to be formatted:



ID	CONTENTS
ID:ET	Flags last sector on a track
ID:EC	Flags last sector on a cylinder
ID:EP	Flags last sector on a disk pack
ID:FL	Flags a sector as bad
ID:SP	Flags a sector as a spare

(continued)

Table 4-19 CMD Code and Commands (continued)

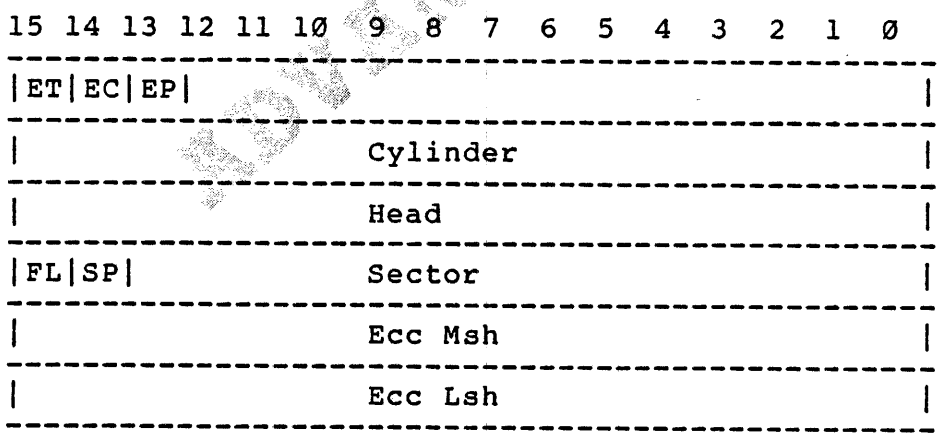
COMMAND	FUNCTION
WRITE	causes data to be written to a specific location on a specified drive. If a partial sector is written with WRITE or WRITE LONG, the contents of the remainder of the sector are undefined.
WRITE LONG	is similar to WRITE, except the data ECC field is written from the four bytes following the data instead of being internally computed. This command is provided for diagnostic purposes.
READ FORMAT	is the inverse of WRITE FORMAT, except that the ID ECC is read along with each ID. Six words are returned for each sector specified. Sectors are read in physical order starting with the sector specified by SC. ID contents are passed directly without error checking.
READ LONG	causes sectors to be read along with their ECCs, which are appended to the end of each data block. This is provided for diagnostic purposes to test error correction. The host writes a sector with a normal WRITE, reads it back with READ LONG, induces an error by switching one or more bits, writes the erroneous buffer with WRITE LONG, and then reads the sector with a normal READ command.
READ	causes the specified sector(s) to be read and transferred to host memory. If necessary and not suppressed, error correction and retry procedures are invoked.
SIZE DISK	causes the controller to examine the specified drive and return, in the packet cylinder, head and sector words, number of cylinders, heads, and sectors on the drive. The controller finds the size by scanning the IDs and looking for end-of-track, cylinder, and pack ID flags. This command takes several seconds. If the controller scans past cylinder 4Ø96 without finding an end-of-pack bit, a pack overflow error is declared.

Sector Format

Each sector contains an ID field and a data field separated by gaps. The gap sizes depend on the drive type, as does the number of sectors per track (refer to Figure 4-12).

One sector on each track is reserved to serve as a spare sector. If a bad sector is found during formatting, it is flagged and the spare is substituted. If two sectors are found to be bad, the drive will abort the format due to the lack of spare sectors.

The SMDC finds sectors by searching for a matching ID (cylinder, head and sector). The formatter program can implement sector reassignment and sector interleaving when formatting a track by properly setting the ID fields. The gap figures provided (refer to Table 4-2Ø) are for one drive and may vary for other drives.



ID	CONTENTS
ID:ET	Flags the last sector on each track
ID:EC	Flags the last sector on each cylinder
ID:EP	Flags the last sector on the pack
ID:FL	Flagged (bad) sector
ID:SP	Spare (unused) sector

Figure 4-12 Sector ID Format

Table 4-2Ø Drive Gap

ITEM	BYTES	DESCRIPTION
SECTOR MARK	~1	Marks beginning of each sector
GAP 1	8+16	Head scatter + PLO lock time
ID SYNC	2	x'ØØFØ'
ID	8	Flags cylinder, head, sector
ID ECC	4	ID error checking
GAP 2	1+16	Write splice + PLO lock time
DATA SYNC	2	x'ØØFØ'
DATA	512	
DATA ECC	4	Data error detection and correction
GAP 3	1+8	Pad + end of track

Status Lines (ST) is returned by the SMDC when the operation is complete. ST contains an error identification code (refer to Table 4-21).

For some errors, it is necessary to refer to status bit error conditions (Table 4-22). Drive Select (DS) contains status bits returned from the selected drive (refer to Table 4-23).

The bit assignments for DS:SKE and DS:SEL correspond to Ports Ø-3, not Drives Ø-3. For the drives and ports to correspond, Drive Ø is plugged into Port Ø, Drive 1 into Port 1, etc.

CT is the number of bytes to be read or written in read/write operations or the number of sectors to be read or written in read/write format operations. If a CT byte count is odd, the command is rejected. A NOP command returns the microcode revision in CT.

AH and AL form the DMA starting address for operations involving a data transfer. If AL is odd, the command is rejected. UN is the drive unit number Ø-15 to be used for the operation. CY is the starting cylinder number Ø-n. HD is the starting head number Ø-n. VS contains control information for multivolume drives. For the drive, it is set for Ø. VS:HB is ORed into the head ID field during a format write.

VS:FS	Force seek for volume select (CMD)
VS:NW	No wait for On-Cylinder (MMD fixed heads)
VS:HB	Head bias (volume select for CMD)

SC is the starting sector number Ø-n. OF specifies four bits of head offset and strobe timing data to be used if CM:NR (no retry) is set.

OF:Ø+	Servo offset plus
OF:Ø-	Servo offset minus
OF:SE	Data strobe early
OF:SL	Data strobe late

Table 4-21 Status Lines (ST) Error Identification Codes

CODE	CONDITION
Ø:	No error
1:	Initialization error (no DT or IV) CR:CMD 4-7 and 1 must be given
2:	Sector overrun error; read or write gate on at end of sector
3:	DMA memory error (ME) returned in SR:ES. (When SMDC detects a parity error, it does NOT rewrite packet, or update packet status in the dispatch table to DONE. An ME code in SR:ES is the only indication of a DMA parity error.)
4:	Select error; no drive or multiple drives selected
5:	CT (count) invalid
6:	Drive dual access busy
7:	Multiple re-zero error, re-zero didn't correct drive fault
8:	Drive status error (see DS)
9:	Odd DMA address
1Ø:	Pack overflow, multiple-sector read/write past end of pack
11:	Power failure detected during read/write
12:	Undefined operation (CM:CMD)
13:	Unrecovered data error
14:	Sector not found
15:	Write protect violation, timeout errors.
32:	Idle loop
33:	Waiting for IP and IUS to clear
34:	Waiting for DMA to complete
35:	Waiting for drive on-cylinder
36:	Waiting for drive servo clock
37:	Waiting for drive data clock
38:	Waiting for sector/index mark
39:	Waiting for ID sync
4Ø:	Waiting for data sync

Table 4-22 Status Bit Error Condition

NAME	BIT	MEANING
	SB:EC	Ø
	SB:RT	1
	SB:RZ	2

Table 4-23 DS Error Conditions

NAME	BIT	MEANING
	DS:RY	Ø
	DS:OC	1
	DS:SE	2
	DS:FT	3
	DS:RO	4
	DS:BZ	5
	DS:XM	6
	DS:SM	7
	DS:SEL	8-11
	DS:SKE	12-15

Drive Interface

SMDC interface signals to the drives consist of the address and control functions transferred on the SMDC A with Bit Ø through Bit 9 signals.

The information on these lines is indicated by the following tag lines when true: CYLTAG, HEADTAG, CONTAG and SELTAG.

CYLTAG- When active low, the ten bus lines carry the cylinder address to the drive. Since it is a direct

addressing device, the SMDC need only place the new address on the lines and strobe the lines with CYLTAG-. The drive must be On-Cylinder before CYLTAG- is sent. The bus lines should be stable throughout the tag time.

HEADTAG- When active low, this tagline (signal) is the head address selected by the bits on the bus line.

CONTAG- This tagline (signal) enables individual control bits, and must be active for the entire control operation as follows:

- Write Gate (Bit Ø) - The Write Gate line enables the write driver.
- Read Gate (Bit 1) - Enables the digital read data on the transmission lines.
- Servo Offset (Bit 2) - When active, the actuator is offset from the nominal On-Cylinder position toward the spindle.
- Servo Offset (Bit 3) - When active, the actuator is offset from the nominal On-Cylinder position away from the spindle.
- Fault Clear (Bit 4) - A pulse is sent to the device to clear the fault if the condition no longer exists.
- AM Enable (Bit 5) - The Address Mark (AM) Enable together with Write Gate or Read Gate allows the writing or recovering of address marks.
- RTZ (Bit 6) - A Return To Zero pulse, when sent to the device, will cause the actuator to seek track Ø, reset the head register, and clear the Seek Error flip-flop.
- Data Strobe Early (Bit 7) - When active, the device PLO Data Separator will strobe data earlier than normal.
- Data Strobe Late (Bit 8) - When active, the device PLO Data Separator strobes the data later than normal.
- Bit 9 - Reserved

SELTAG - Using SEL1 through SEL8, the Unit Select Tag gates the desired binary logic number of the unit selected into the logic number compare circuit.

The following are drive control functions:

SECTOR - The sector mark is derived from the servo track. Timing integrity is maintained throughout seek operations. The number of sectors per revolution is switch selectable and determined by sector clocks, a signal.

FAULT - When active, a fault condition exists in the drive. The following types of faults are detected: dc voltage, Head Select, Write, Write or Read while Off-Cylinder, and Write Gate during a Read operation. The line may be cleared by Control Select or Fault Clear with the CONTAG enable.

SKERR - When this line is active, a Seek Error has occurred. This line indicates the unit was unable to complete a move within 500 ms or the carriage has moved to a position outside the recording field or received an illegal track address. A Return To Zero (RTZ) clears the Seek Error and returns the heads to cylinder zero while enabling the ONCYL signal to the controller.

ONCYL - The On-Cylinder status indicates the servo has positioned the heads over a track. The status is cleared with any seek instruction causing carriage movement or zero-track seek.

INDEX - The signal occurs once per revolution and its leading edge is considered the leading edge of sector zero. Timing integrity is retained throughout seek operations for all drives.

READY - When active, with the device selected this line indicates: drive is up to speed, the heads are positioned over the recording tracks, and no fault condition exists within the drive.

OPENCABLE - The open cable detector circuit disables the interface when the SMD A interface cable is disconnected or controller power is lost.

SEL1, SEL2, SEL4, SEL8 - These four lines are binary coded to select the logical number of one of sixteen devices. The individual unit number (0 - 15) is selectable by a logic plug on the unit's operator panel.

SELECTED - When the four lines (SEL1, SEL2, SEL4, SEL8) select and compare the logical number with the selectable individual unit and the SELTAG is received, the SELECTED-line becomes true and transmitted to the controller on the SMD B cable.

WPROT - Enabling the Write Protect function inhibits the writer under all conditions, illuminates an LED, and sends the WPROT- signal to the SMDC A controller. The Write Protect function is enabled by a switch on the operator panel.

SEEKEND - Seek End is a combination of On-Cylinder or Seek Error, indicating that a seek operation has terminated.

HOLD/PICK - Applying ground to the Pick and Hold lines enables the first drive in a power-up sequence. Once up to speed, the PICK- signal is transferred to the next active drive.

BUSY - If the device is already reserved and/or selected, a Busy is issued to the controller on the SMD A cable and SELECTED is issued on the SMD B cable.

WRITEDATA (Ø-3) - This line carries data (NRZ Form) which is to be recorded on the disk pack.

READDATA (Ø-3) - This line transmits the recovered data to the controller in the NRZ form.

SERVOCLK (Ø-3) - The Servo Clock is a phased-locked 9.677 MHz clock generated from a signal on the drive and used to generate write data. This signal is available at all times to the controller.

READCLK (Ø-3) - The Read Clock defines the beginning of a data cell. It is an internally derived clock signal and is synchronous with the detected data. It is transmitted continuously to the controller.

WRITECLK (Ø-3) - The Write Clock signal is synchronized to the NRZ data. The Write Clock is the received Servo Clock which is retransmitted by the controller during a write operation.

4.2.3.6. Tape Cartridge Controller Interconnect - The tape controller is the intelligent interface between the CPU and the tape drive.

The controller derives its intelligence from its on-board Z8ØB microprocessor. Figure 4-13 shows the basic relationship between the controller and both the system bus (ZBI) and the tape drive.

NOTE

The paragraph that follows assumes that the Tape Cartridge Controller board is inserted into the CPU card slot 4.

Information flows between the controller and the CPU over the ZBI mating connectors P1/J14. The flow of information between the controller and a selected tape drive is through mating connectors P2/J24 of slot 4 only of the system backplane. The allocation of the I/O address of the controller is shown in Figure 4-14.

ZBI Interface

The controller and the host communicate through eight 16-bit (word) read/write registers. These registers appear in the hosts I/O space at addresses 4ØH through 4EH (H denotes hexadecimal). Table 4-24 lists these registers and their assignments.

NOTE

The on-board (etched) jumpers described in the following paragraph should not be changed.

On-board jumpers provide a means of changing the ZBI address of the controller board. These jumpers are listed in Table 4-25.

The bit assignments of the upper byte of the interrupt vector are listed in Table 4-26.

The commands that the host sends to the controller are listed in Table 4-27, Table 4-28 defines the bits in the status register.

Table 4-29 lists the bits in the Master Interrupt Control (MIC) register. Appendix C supplies all of the possible error conditions for the Tape Cartridge Controller.

Drive Interface

The tape controller sends commands to the tape drive to control its operation. These commands set the drive address, track address, and motion controls.

Table 4-30 lists the interface signals that the controller sends to the drive. The drive responds to the controller by sending information back to the controller.

Table 4-31 lists the interface signals that the tape drive sends to the controller.

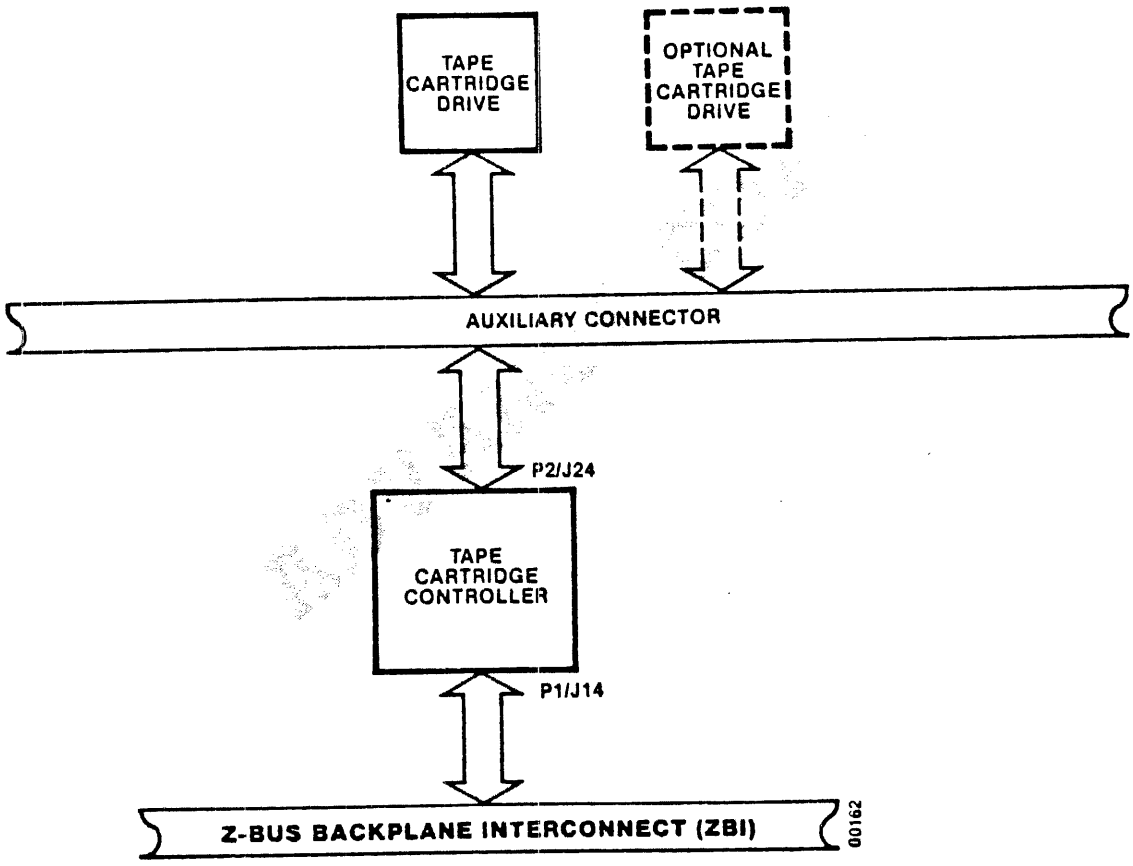


Figure 4-13 Tape Cartridge Controller Functional Relationships

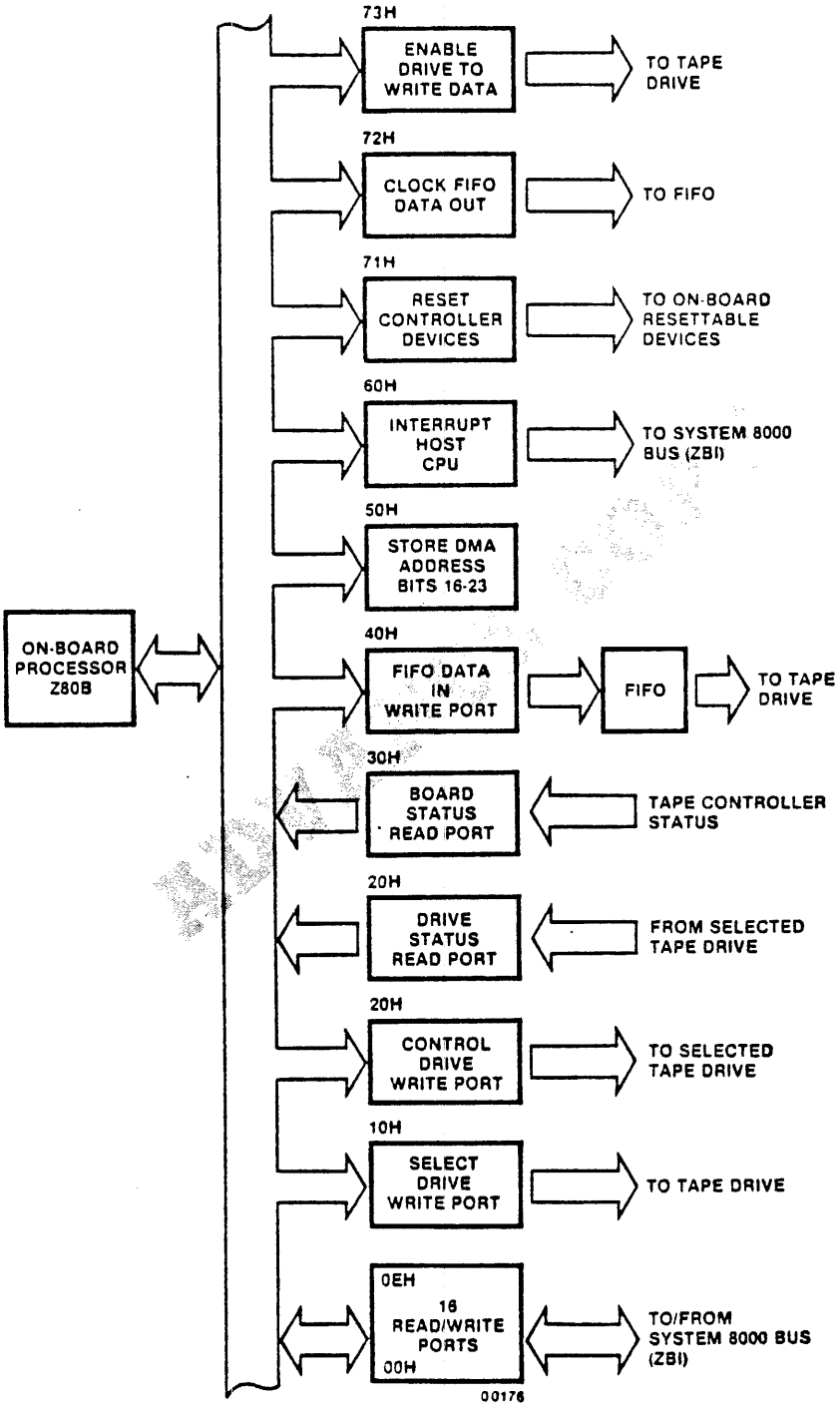


Figure 4-14 Tape Cartridge Controller I/O Address Space

Table 4-24 ZBI Tape Controller Interface Registers/Assignments

ADDRESS	REGISTER	DESCRIPTION
40H	Interrupt Vector	The low-order byte contains the interrupt vector the host CPU writes to the controller. The high-order byte contains status information the controller sends to the host.
42H	Command	The host sends commands to this register. The controller accepts only valid commands.
44H	Low DMA Start Address	The host sends the low word of the DMA starting address in this register. Bit 0 of this byte must be a 0, so the address starts on a word boundary.
46H	High DMA Start Address	This register contains the high-order byte (Bits 16 to 23) of the DMA start address.
48H	DMA Length	This register contains the length of the DMA transfer. This value must be $\leq$32K bytes.
4AH	Status	The controller stores information about the tape drive and controller in this register. The host reads this information.
4CH	Status 1	Bits 0 to 3 define the number of retries for a read or write command. Bits 8 to 15 define the number of blocks or files that have been skipped during a skip command.
4EH	Interrupt Control	This is the master interrupt control register.

Table 4-25 Tape Controller Jumper Selection for Base Address

JUMPER GROUP (ETCHED)	PURPOSE	CONNECTION AND RESULT
E1, E2, E3	Set to expect either a low or high Bit SAD15.	E1 to E2 (normal): Bit SAD15 low E2 to E3: Bit SAD15 high
E4, E5, E6	Set to expect either a low or high Bit SAD14.	E4 to E5 (normal): Bit SAD14 low E5 to E6: Bit SAD14 high
E7, E8, E9	Set to expect either a low or high Bit SAD13.	E7 to E8 (normal): Bit SAD13 low E8 to E9: Bit SAD13 high
E10,E11,E12	Set to expect either a low or high Bit SAD12.	E10 to E11 (normal): Bit SAD12 low E11 to E12: Bit SAD12 high
E13,E14,E15	Set to expect either a low or high Bit SAD11.	E13 to E14 (normal): Bit SAD11 low E14 to E15: Bit SAD11 high
E16,E17,E18	Set to expect either a low or high Bit SAD10.	E16 to E17 (normal): Bit SAD10 low E17 to E18: Bit SAD10 high
E19,E20,E21	Set to expect either a low or high Bit SAD09.	E19 to E20 (normal): Bit SAD09 low E20 to E21: Bit SAD09 high
E22,E23,E24	Set to expect either a low or high Bit SAD08.	E22 to E23 (normal): Bit SAD08 low E23 to E24: Bit SAD08 high
E25,E26,E27	Set to expect either a low or high Bit SAD07.	E25 to E26 (normal): Bit SAD07 low E26 to E27: Bit SAD07 high

Table 4-25 Tape Controller Jumper Selection for Base Address (continued)

JUMPER GROUP (ETCHED)	PURPOSE	CONNECTION AND RESULT
E28,E29,E3Ø	Set to expect either a low or high Bit SADØ6.	E28 to E29: Bit SADØ6 low E29 to E3Ø (normal): Bit SADØ6 high
E31,E32,E33	Set to expect either a low or high Bit SADØ5.	E31 to E32 (normal): Bit SADØ5 low E32 to E33: Bit SADØ5 high
E34,E35,E36	Set to expect either a low or high Bit SADØ4.	E34 to E35 (normal): Bit SADØ4 low E35 to E36: Bit SADØ4 high
E37,E38,E39	Set to enable or disable the controller board	E37 to E38 (normal): enables board to receive address from ZBI bus. E38 to E39: disable board.

Table 4-26 Tape Interrupt Vector Bit Definitions

BIT	NAME	MEANING
Bit 8	INTV	The current operation requires intervention.
Bit 9	BUSY	The controller is busy executing the last command.
Bit 1Ø	CMDREJ	The controller rejects the current command.
Bit 11	DATERR	An uncorrectable data error has occurred.
Bit 12	SKNDNE	The current skip operation has not been completed.
Bit 13	OVERFL	A buffer overflow has occurred.
Bit 14	FFERR	A FIFO error has occurred.
Bit 15	Not Used	

Table 4-27 Host-Tape Controller Commands

CODE (HEX)	NAME	DEFINITION
ØØØØ	NOP	The controller loops while waiting for a command from the host.
ØØØ1	READ	The controller reads one block. If necessary, controller backspaces and retries.
ØØØ2	WRITE	The controller writes one block. If necessary the controller backspaces, erases three inches of tape and retries.
ØØØ3	REWIND	Controller rewinds tape to the logical load point, 6 inches past the physical load point.
nnØ4	SKBF	Controller skips nn blocks forward; nn is any value from Ø to 255.
nnØ5	SKBR	Controller skips nn blocks in reverse; nn=Ø to 255.
nnØ6	SKFF	Controller skips nn files forward nn= Ø to 255. A file is a group of blocks followed by a file mark.
nnØ7	SKFR	Controller skips nn files in reverse; nn=Ø to 255.
ØØØ8	WFM	Controller writes a file mark on the tape.
ØØØ9	LOAD	Controller moves the tape from the physical load point to the logical load point; beginning of tape, track Ø is selected.
ØØØA	UNLD	Controller moves the tape to the physical load point.
ØnØB	SEL	Controller selects a new drive; address is n, a value from Ø to 3.

(continued)

Table 4-27 Host-Tape Controller Commands (continued)

CODE (HEX)	NAME	DEFINITION
ØnØC	MRTRY	This sets the maximum number of retries the controller is allowed for reads and writes. At power-on, the default is 1Ø retries; n=Ø to 15.
ØnØE	STRK	Controller rewinds the tape and selects new track; n=Ø to 3.
ØnØF	MODE	Controller changes to mode n; n=Ø,1. In mode 1, tape is divided into four separate tracks. The logical beginning of tape is at the beginning of each track. Logical end of tape is at the end of each track. REWIND moves the tape to the start of each track; skips do not carry from track to track. In mode Ø, tape is one long track. Logical beginning of tape is at the start of track Ø and the logical end of tape is at the end of track 3. REWIND moves the tape to the start of track Ø; skips carry from track to track. At power-on, the default is mode Ø.
ØØ1Ø	DIAG	The controller executes a diagnostic test, checking the ROM, the FIFO, and the host interface ports.

Table 4-28 Status Register Bit Definitions

BIT	NAME	DEFINITION
Bit Ø	NOTAP	No tape cartridge in drive
Bit 1	FMDET	File mark detected during read or skip blocks
Bit 2	HWERR	Hardware error
Bit 3	INVAL	Invalid command
Bit 4	INAP	Inappropriate command
Bit 5	(Not Used)	
Bit 6	BPARM	Bad DMA parameters
Bit 7	BLKTAP	Blank tape
Bit 8	PROT	Tape cartridge write protected
Bit 9	LBOT	Tape at logical beginning of tape
Bit 1Ø	LEOT	Tape at logical end of tape
Bit 11	RTRYAT	One or more retries attempted
Bit 12	UNITØ	Tape drive address Bit Ø
Bit 13	UNIT1	Tape drive address Bit 1
Bit 14	TRKØ	Track address Bit Ø
Bit 15	TRK1	Track address Bit 1

Table 4-29 Master Interrupt Control (MIC) Register, Bit Definitions

BIT	NAME	DEFINITION
Bit Ø	MIE	Master Interrupt Enabled
Bit 1	IE	Interrupt Enabled
Bit 2	DLC	Disable Lower Chain
Bit 3		Not defined
Bit 4		Not defined
Bit 5		Not defined
Bit 6	IUS	Interrupt Under Service
Bit 7	IP	Interrupt Pending

Table 4-3Ø Tape Controller to Drive Interface Signals

SIGNAL	DEFINITION
RWD\	Rewinds the tape.
REV\	Moves the tape backwards.
FWD\	Moves the tape forward.
WEN\	Enables writing and erasing on the tape.
WDE\	Enables sending of write-data strobes and the writing of data on the tape.
WNZ\	Serial data to be written to the tape drive.
TR1\,TR2\	Selects tracks during read, write, and erase track operation, according to the following code:

Track Number	TR2\	TR1\
Ø	High	Low
1	Low	High
2	Low	Low
3	High	High

SLG\	Allows selection of tape drive designated by unit select codes: SL4\, SL2\, SL1\.
SL4\,SL2\,SL1\	These form the unit (drive) select code listed below:

Drive Selected	SL4\	SL2\	SL1\
Ø	H	H	L
1	H	L	H
2	H	L	L
3	L	H	H

Table 4-31 Tape Drive to Controller Interface Signals

SIGNAL	DEFINITION
SLD\	Selected drive informs controller that the drive has received its unit address.
RDY\	Tape cartridge is installed.
WND\	Selected drive has received a write enable signal.
FLG\	Rewind completed.
LPS\	Load point sensed.
FUP\	Installed tape cartridge is unprotected.
BSY\	The drive is doing one of the following: 1) Automatic rewind after cartridge is installed. 2) Executing rewind, forward, or reverse command.
EWS\	The upper early warning hole in forward direction has been reached.
WDS\	The drive is examining the state of WNZ\ signal.

Tape Controller Operation

To start a tape operation, the host CPU reads the high-order byte of the controller's interrupt vector to see if the Busy bit is set. If Busy bit is set, the controller is still executing the last command; if not, the host initializes the interface registers, then writes a non-zero command in the controller's command register. The flowchart in Figure 4-15 shows the steps taken by the host.

The controller normally loops while it waits for a non-zero command from the host. When the controller receives a command, it resets the Interrupt Pending (IP) bit in the Master Interrupt Control register.

The controller sets the Busy bit in the upper byte of the Interrupt Vector register. This will inform the host it is busy with the current command. However, before the controller processes the command, it checks its validity.

After processing the command, the controller resets the command After processing the command, the controller resets the command register. If MIE and IE = 1, the controller sets the IVS bit.

If MIE and IE are not both equal to 1, the controller sets the IP bit and clears the Busy bit. The controller then loops while waiting for a new command. When the host sees the IP bit set, it reads the MIC register and the status registers. The controller clears the Busy bit and then loops while waiting for a new command. The controller then sends an interrupt to the host and waits for an acknowledgement. The controller sends its interrupt vector in response to the acknowledgement.

An upper byte of zero means that no errors occurred. The controller also sets the Interrupt Under Service (IUS) bit.

The host reads the vector from the controller and processes the interrupt. At the end of the interrupt routine, the host clears the controller's IUS bit. This action ends the interrupt subroutine for the host.

4.2.3.7. ECC Memory Subsystem Controller: The Memory Subsystem controller controls up to 4M bytes of dynamic R/W memory. The controller can perform R/W operations with byte (8-bit), word (16-bit), and long word (32-bit) quantities.

Figure 4-16 shows the functional relationship between the controller and the ZBI and the memory modules that it controls.

The controller stores data as 32-bit long words and adds to this seven bits of information for use by the error detection and correction circuits. Figure 4-17 shows the overall organization of memory.

During memory transactions, the controller accepts a 24-bit address and the B/W\ and W/LW\ control signals over the ZBI. The two least-significant address bits and the B/W and W/LW\ signals select one of the four bytes at the location to be read or modified.

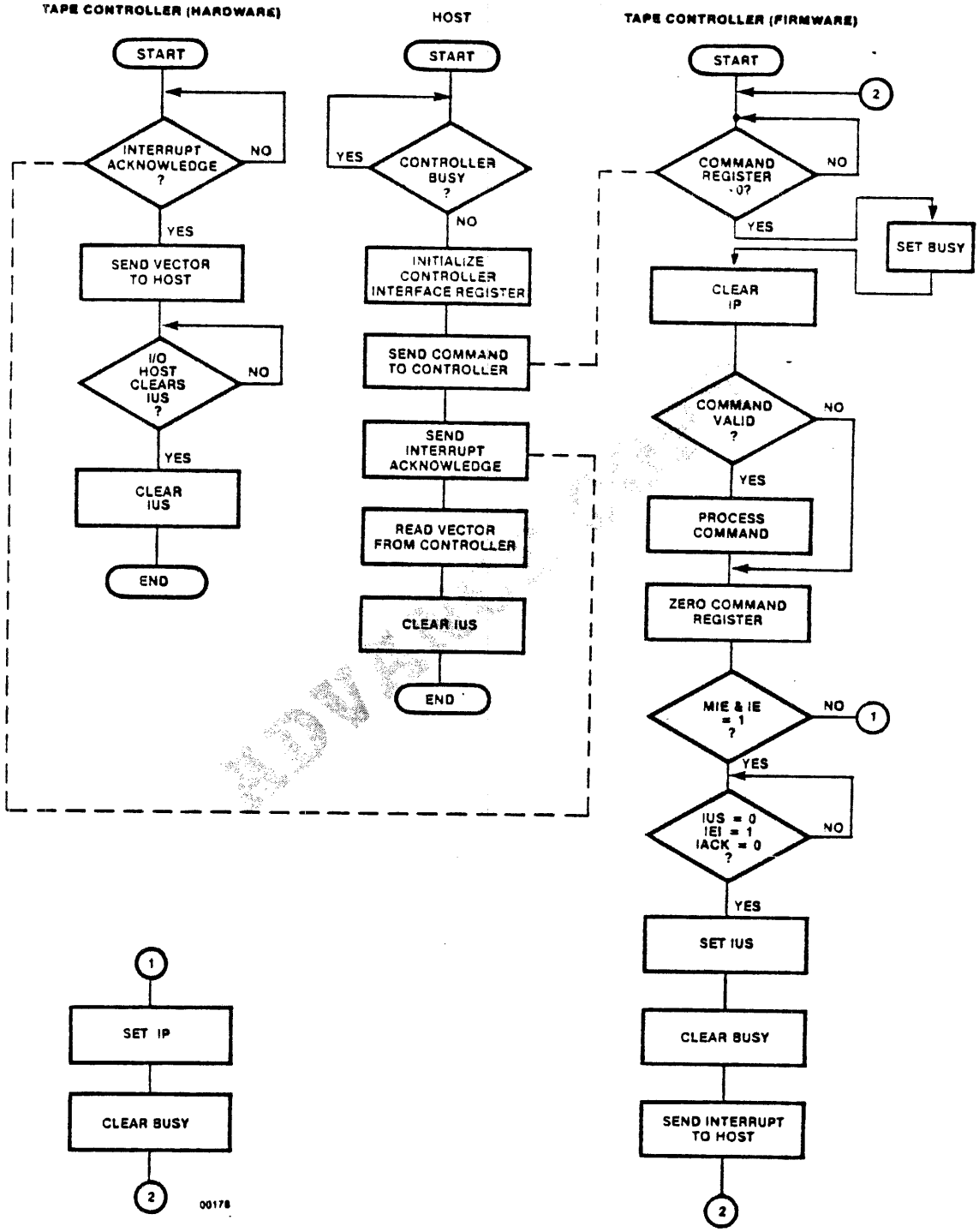


Figure 4-15 Tape Cartridge Controller, Command Processing

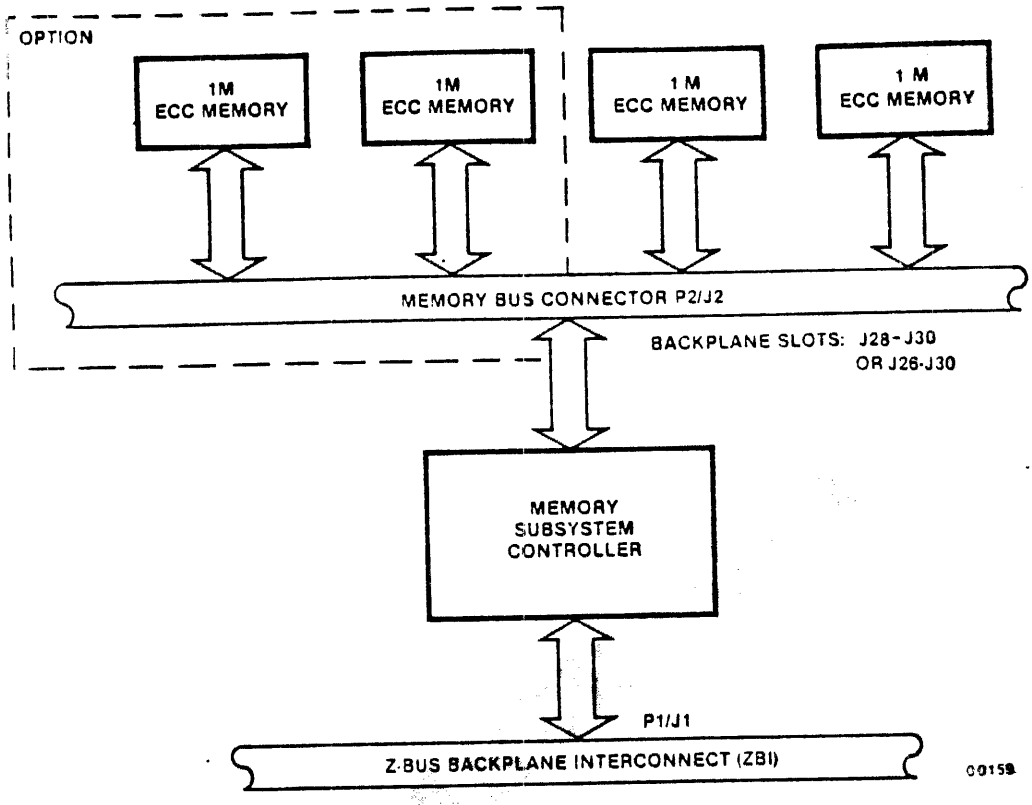


Figure 4-16 Memory Subsystem Controller, Functional Relationships

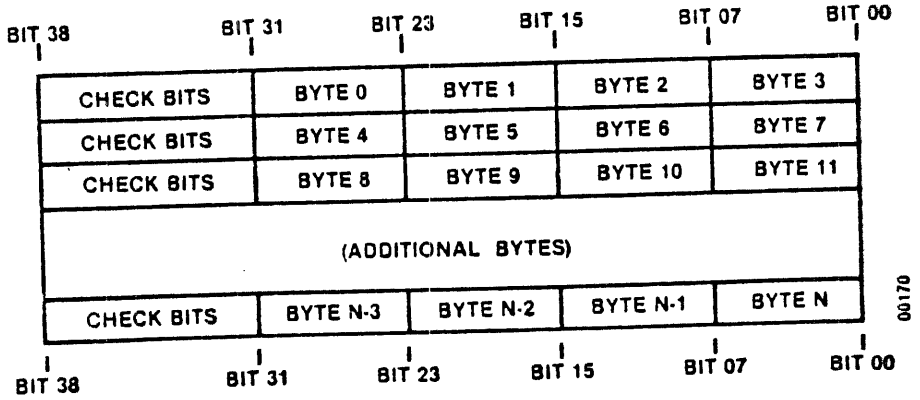


Figure 4-17 Memory Organization

Byte Translation

During transactions involving bytes, the controller receives a data byte from ZBI lines ADØ through AD7. Figure 4-18 shows the flow from a register, through the controller, and to memory.

The controller places byte A, the first byte, in location Ø (Bits 31 to 24). For this transaction, the bus controller sets both the B/W\ and W/LW\ control lines high to identify the current transfer as a byte transfer. The bus controller also places low levels (Ø) on ZBI address lines ADØØ and ADØ1 to tell the memory controller to place byte A in Bit positions 31 to 24.

Next, the memory controller places byte B, C, and D in the succeeding memory locations to fill up the current double word of memory. The memory controller places the fifth byte in the first location of the next double word of memory, Bits 31 through 24 of byte 4 (not shown).

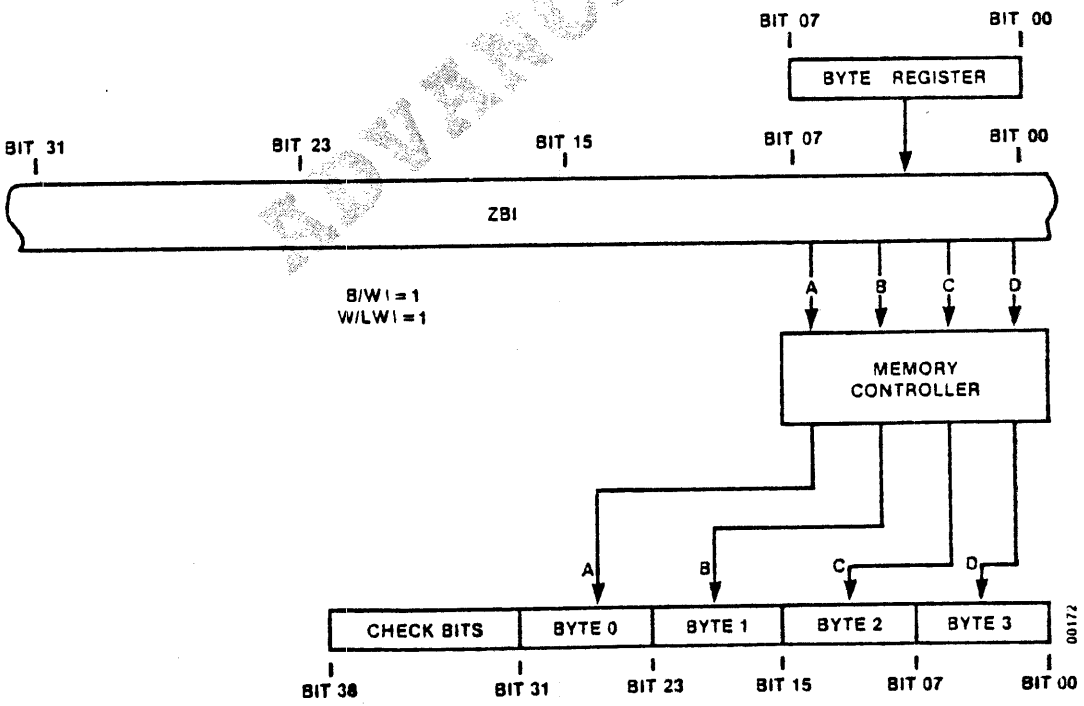


Figure 4-18 Byte Translation

Word Translation

For word (16-bit) translations, the bus controller sets line B/W\ low and W/LW\ high. This code tells the memory controller that the current transfer is a 16-bit transfer. The bus controller places the 24-bit address on the ZBI to point to the double word location in memory where the memory controller is to place the current transfer.

Only the 22 most significant bits of the address point to the memory location. The memory controller ignores the least-significant address Bit (AD00); the state of address Bit AD01 tells the memory controller to store the current word (16 bits) in either the upper half or lower half of the double-word space in memory. Figure 4-19 shows the path of two 16-bit words, E and F. The controller stores word E in the word 0 location (Bits 31 to 16) and stores word F in the word 1 location (Bits 15 to 0). All word-size transfers must occur only on a word boundary.

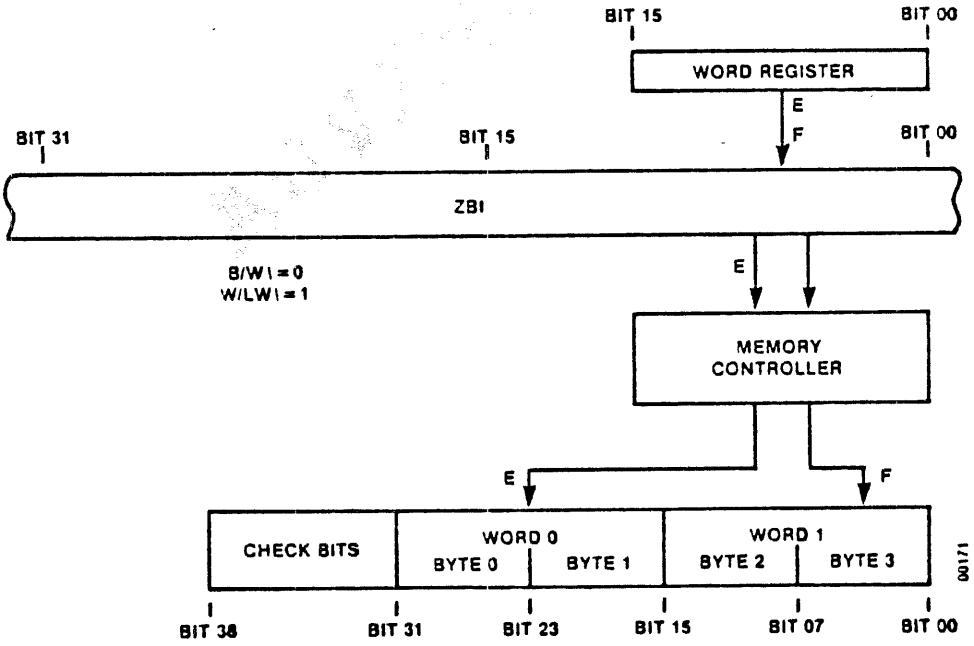


Figure 4-19 Word Translation

Long Word Translation

Long words (Figure 4-2Ø contain four bytes (32 bits) and occupy the entire width of the ZBI and memory controller, and end up in a location in memory. The 22 most-significant address bits point to the location; the controller ignores the two least-significant bits, ADØØ and ADØ1.

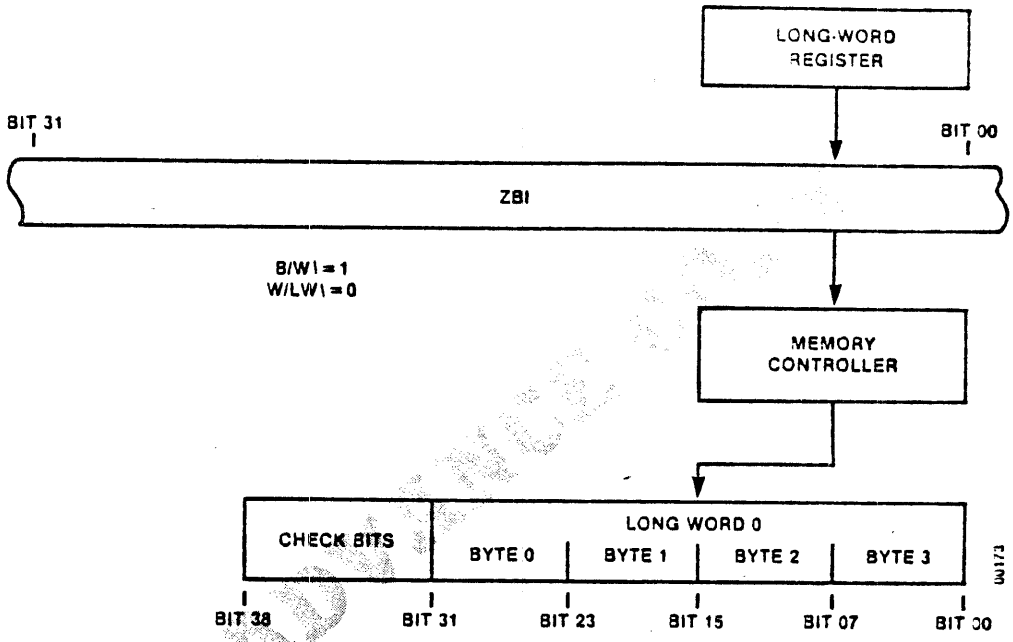


Figure 4-2Ø Long Word Translation

4.3. System Reset

A system reset can be generated from a power-up circuit on the CPU board or by the RESET button on the front panel of the system.

The power-up reset circuit makes certain that all functions in the system start in an orderly manner.

The RESET button on the front panel is disabled by the ON/LOCK keylock switch when in the LOCK position.

When the system is reset, the following actions occur:

1. All eight serial I/O channels are disabled. All SIO control registers must be initialized.

2. All CTC channels stop counting and all interrupt enable bits are cleared. CTC control registers must be initialized.

3. Parallel data is inhibited.

4.4. Non-Maskable Interrupts

Non-Maskable Interrupts (NMI) are typically reserved for external events that require immediate attention. They cannot be disabled (masked) by software.

The System 8000 provides three sources of NMI:

- Manual NMI
- Power-Fail NMI
- ECC Memory Error NMI

4.4.1. Manual NMI

A manual NMI can be generated in the system from the START pushbutton on the front panel. The NMI can be disabled by placing the ON/LOCK keylock switch in the LOCK position.

When the START pushbutton is pressed immediately after a manual or power-up reset, the System Power-Up Diagnostics (SPUD) firmware is invoked.

At the conclusion of the diagnostic, if no errors have been recorded, the message "POWER-UP DIAGNOSTICS COMPLETE" appears on the console screen and the ZEUS operating system is automatically booted.

4.4.2. Power-Fail NMI

A power-fail NMI is sent to the Z8001A CPU when the system power supply detects a decrease in line voltage signifying a potential power failure. After receiving a power-fail NMI, the system has about 2 msec to power-down.

When a power-fail NMI identifier is read by the operating system, the operating system generates a software reset, which in turn, becomes a hardware system reset, thus the drives are protected from crashing during a power failure.

4.4.3. ECC Memory Error NMI

A NMI will be sent to the CPU when a double-bit non-correctable ECC memory error is flagged by the ECC Controller, and when the Clear ECC Error bit of the System Configuration Register (SCR) is set to enable an ECC NMI. The error bit is initially cleared at the SCR during a system reset or power-up.

4.4.4. NMI Identifier

When a NMI is detected by the CPU, the subsequent initial instruction fetch cycle is initiated, but aborted. The Program Counter (PC) is not updated, but the system Stack Pointer is decremented.

The next CPU machine cycle is the Interrupt Acknowledge cycle. This cycle acknowledges the interrupt and reads a 16-bit Identifier word (all 16 bits can represent peripheral device status and ID information) from the device that generated the interrupt (in this case, an NMI source).

This identifier word, along with the program status information, is stored on the system stack and new status information is loaded into the PC and FCW (Flag and Control Word register).

When the CPU generates an NMI acknowledge status code (Ø1Ø1), the source of the NMI will be either a manual, power-fail, or ECC memory error. Dedicated logic on the CPU board enables a 4-bit error buffer to place a 4-bit NMI identifier on multiplexed address/data lines ADØ to AD3, as follows in Table 4-32.

Table 4-32 NMI Identifier for Multiplexed Lines

AD3	AD2	AD1	ADØ	SOURCE
Ø	Ø	Ø	1	Manual NMI
Ø	Ø	1	Ø	Power-Fail NMI
Ø	1	Ø	Ø	ECC Memory Error NMI

Bits AD4 to AD15 are "don't care" bits in an NMI acknowledge identifier word if the NMI source is any one of the three listed sources of NMI in the system.

If the NMI source is external to the CPU and not one of the three listed sources of the NMI, the NMI buffer will remain off and the 16-bit identifier word will be read from the system bus.

4.5. Vectored Interrupts

When the CPU acknowledges an interrupt from a peripheral device, it reads a 16-bit identifier word to identify the source of the interrupt. In vectored interrupts, the identifer is also used by the CPU as a pointer to select a particular interrupt service routine associated with the peripheral that was the source of the interrupt.

The system CPU can configure the Parallel I/O Controller, (PIO) Counter/Timer Circuit (CTC), and Serial I/O (SIO) Controller peripheral devices for vectored interrupt operation. The interrupt vectors associated with these peripherals can be loaded at any time, since these devices are initialized with their interrupts disabled (masked).

NOTE

It is recommended that vectored interrupts be disabled by the CPU until all peripherals on the system CPU have been properly initialized because of the vectored interrupt daisy-chain.

Since there are several Z8ØB peripheral devices on the CPU board, an interrupt daisy-chain is used to prioritize the devices and to accelerate their interrupt request time.

Each Z8ØB device contains lines that function as links in the daisy-chain: Interrupt Enable In (IEI), (INPUT, active high) and Interrupt Enable Out (IEO), (OUTPUT, active high).

The Z8ØB peripherals on the CPU board are prioritized in a daisy-chain as indicated in Table 4-33.

Certain model configurations require a different priority interrupt daisy-chain. The daisy-chain is controlled by jumper pins on the ZBI backplane.

NOTE

The standard system was daisy-chain configured at the factory before it was shipped. However, if an optional configuration is installed in the field, reference Section 3 of this manual, or contact Zilog Field Service for the correct priority interrupt daisy-chain.

Vectored interrupts from any of the peripherals, 1 to 8 (Table 4-33 for the system) automatically disable interrupts from lower priority peripheral devices in the chain. Off-board devices have the lowest priority in the chain.

Table 4-33 Device Priority Scheme

PRIORITY	PERIPHERAL DEVICE	FUNCTION
1	CTC Ø	Single Step, also generates BAUDØ, BAUDl, BAUD2
2	CTC 1	Generates BAUD3, BAUD4, BAUD5
3	CTC 2	Generates BAUD6, BAUD7, and the Real Time Clock
4	SIO Ø	Serial Channels Ø, 1
5	SIO 1	Serial Channels 2, 3
6	SIO 2	Serial Channels 4, 5
7	SIO 3	Serial Channels 6, 7
8	PIO Ø	Line Printer Interface
9	(OFF CPU BOARD I/O)	SSB
1Ø	Addition I/O	SSB
11	*SMD Controller	
12	**Tape Controller	

*When Used in slot 3
**When used in slot 4

4.6. Memory Management Unit (MMU)

The Z8Ø1Ø Memory Management Unit manages the 16M byte main memory address space of the System 8ØØØ CPU. The MMU also provides the following features:

1. Flexible and efficient allocation of main memory resources during the execution of both operating system and user tasks.

2. Support multiple, independent tasks that share access to common resources.

3. Protection from unauthorized or unintentional access to data or other memory resources.

4. Detection of incorrect use of memory by an executing task.

5. Partitioning of main memory resources to separate user functions from system functions.

4.6.1. Segmented Operation

A segmented operating system uses MMU M1 (code) to provide an address space consisting of up to 63 segments, e.g., segments Ø to 62. In a segmented operating system, all 128 segments are usable.

Segment 63 is used to run non-segmented user programs. Since the attribute flags in the segment descriptor registers of MMU M3 (stack) are used to configure different segments, no separation between code, data or stack references is required.

A segmented user program uses M2 and M3 to provide an address space consisting of 124 or 128 segments, without separating code, data, and stack areas.

4.6.1.1 Segmented Operating System, Non-Segmented User: For operating systems executing in this configuration, the normal/system status line is checked; if in system mode, all program and memory references go through MMU M1; if in normal mode (user mode), all instruction space accesses will be routed through MMU M1 (code).

For memory references other than program references, the logical address offset generated by the CPU is compared against the contents of the NBR. If the result of the

comparison is less than zero, the select logic enables MMU M2 (data); otherwise, MMU M3 (stack) is enabled.

In order for the operating system to access user memory that is mapped through MMU2 or MMU3, the segment descriptor must first be copied into MMU1. (By convention, segment 63 is recommended for running user programs.)

4.6.1.2 Segmented Operating System, Segmented User: For operating systems executing in this configuration, the normal/system status line is checked; if in system mode, all program and memory references go through MMU M1; if the CPU is in normal mode, all references to segments Ø through 63 will enable MMU M2, and all references to segments 64 through 127 will enable MMU M3.

In order for the operating system to access user memory, the appropriate segment descriptor must be copied from MMU2 or MMU3 to MMU1. (By convention, the user stack is placed in segment 127.)

4.6.2. MMU Configurations

The MMU configuration is set by hardware jumpers on the CPU board and by the operating system software. The jumpers are used to configure the MMU select logic for either a segmented or non-segmented operating system.

The operating system software configures the System Configuration Register (SCR) for running segmented or non-segmented user processes (programs). Refer to Table 4-5 for possible jumper configurations.

4.6.3. Break Registers

Two 8-bit hardware registers, the System Break Register (SBR) and the Normal Break Register (NBR), are accessible as I/O ports on the CPU board.

During any memory reference, the 16-bit logical address offset generated by the CPU is compared to the break value given by the contents of either the SBR or the NBR.

The SBR is referenced for the break value if the segment number is zero or one, and the NBR if it is otherwise.

If the logical address offset is less than the break value, the current reference is for data (MMU M2 is enabled). Otherwise, it is a stack reference (MMU M3 is enabled).

4.6.4. User Segment A

To access a user segment, the operating system can use a free segment slot and set its Segment Descriptor Register to point at the same memory area as the target user segment's SDR.

To access the user code segment, one of the unused segment slots is set to point at the code segment; for example, number 62. The SDRs for this segment slot in M2 and M3 are both set to point at the code segment, negating the contents of the NBR.

4.6.5. System Segments and Protection

Logic on the CPU board partitions segments into system segments (logical segments 2 to 63 and 66 to 127).

Any reference to a system segment always enables the System Break Register for comparison with the logical address offset, while any reference to a user segment always enables the Normal Break Register. These comparisons are independent of whether the Z8001 CPU is executing in system or normal mode.

The function of the system segment detection logic is to prohibit normal mode programs from accessing system mode segments.

Normal mode references to system segments are not valid and cause no MMU to be selected, and a segment violation is forced upon the CPU. This violation is maintained until cleared by the segment trap acknowledge status of the CPU.

SECTION 5
MAINTENANCE

5.1. Introduction

This section provides the maintenance procedures that are necessary and important to maintain the System 8000.

The objective of any maintenance program is to provide maximum equipment availability to the customer. Preventive Maintenance (PM) provided in this section is designed to minimize the effect of known failures on the equipment, and to enhance mean-time-between-failures for maximum customer operating equipment availability.

Maintenance for the system should be performed by a qualified and trained Field Engineer (FE). The tools and other materials listed in paragraph 5.1.1 should be on site and available to the FE before starting PM. System documentation should also be available (refer to Section 1 for a listing of the system's related documentation).

Two fundamental considerations in the preventive maintenance of electrical equipment are:

- Visual Inspection

  Visual inspection is the FE's most valuable preventive maintenance tool. Most mechanical equipment failures will have given visual indications of their presence long before the actual failure occurs.

- Electrical Checks

  Electrical checks, consisting of diagnostic programs and voltage measurements, are effective in locating potential and intermittent problems.

FEs should place special emphasis on safety when performing electrical test procedures (see paragraph 5.1.2.). Static information is provided in paragraph 5.1.3.

CAUTION

Be sure to remove ac power whenever performing maintenance on the system. Reference Subsection 5.2 for the recommended ac power removal instructions.

5.1.1. Tools and Test Equipment

The following is a list of tools and test equipment needed for the preventive maintenance to be performed in Subsection 5.2.

1. Standard FE tool kit
2. Serial I/O cable
3. Centronics parallel interface cable
4. A serial I/O modem test cable
5. One scratch cartridge tape
6. One scratch nine-track tape
7. Cotton swabs
8. Isopropyl alcohol (99%)
9. Clean soft brush or source of compressed air
10. HP 3466A multimeter or equivalent

5.1.2. Safety Considerations

Maintenance personnel should observe the following safety procedures and precautions.

1. All WARNINGS, CAUTIONS, and NOTES contained within the manual should be read and exercised with the following understanding:

WARNING

CALLS ATTENTION TO A SPECIFIC PROCEDURE THAT MAY RESULT IN PERSONAL INJURY IF IMPROPERLY PERFORMED.

CAUTION

Calls attention to a specific procedure that may result in damage to the equipment if improperly performed.

NOTE

Calls attention to and stresses the importance of a situation documented in the associated text.

2. Whenever the removal of ac power is required, use the procedure in Subsection 5.2 of this manual.

3. If the system must be moved or relocated, follow the repacking procedure in Section 3, paragraph 3.3.3 of this manual.

4. When performing PM, observe the following:

   a. Keep all beverages off the system.

   b. Keep pens, pencils and other foreign objects off the system.

   c. As a good practice, discharge body static by placing one hand on a conductive surface grounded to a common earth ground before touching the system.

5.1.3. Static

Electrostatic charge generation cannot be completely eliminated, therefore, it should be controlled to prevent possible electrostatic discharge damage to static sensitive devices. Electrostatic discharge can exist without the realization of the user.

Suggested corrective safety measures and procedures to avoid problems that are associated with static are as follows:

1. Discharge body static by placing one hand on a conductive surface grounded to a common earth ground.

2. Avoid placing cartridge tapes directly next to system terminal CRTs.

3. When installing a system option involving PCB(s), avoid placing the PCB(s) on bubble plastic, styrofoam, or other synthetic type materials which are not antistatic (unless specially treated).

5.2. AC Power Removal

Most of the preventive maintenance procedures require the removal of ac power from the system. Be sure that ac power (and cables) are removed from the system whenever removing and/or replacing equipment.

The following steps bring the system down:

1. Notify all users that the system is to be brought down using the wall(M)* command. By using this command, the administrator can send a message to each terminal, notifying all logged-in users of the impending shut-down.

NOTE

Down(M) is the utility for bringing the system down into single-user mode. However, it can be done manually as described in Steps 3 and 4.

2. Execute the utility command down(M), which will bring the system down into single-user mode, skip to Step 4.

3. Issue the command

```
init 1      or      kill -1  1
```

This kills all multi-user related processes running on the system. This command must be issued by the super-user. The system is left running a single-user csh process that receives commands from the tty labelled "console".

4. Issue the commands

```
sync; sync
```

---

* The (M) next to the command "down" points the reader to a particular section of the Zeus Reference Manual that describes the command, and includes examples of its usage.

from the system console. This forces all outstanding I/O on the system to completion.

5. Turn keylock switch to ON.

6. Press the RESET button.

7. At the system console type in

   T <carriage return>

   The console displays an indication of the active peripherals. Record this information for future reference.

8. Turn the system power switch to OFF.

9. Unplug the ac power cables from the main power source.

5.3. Preventive Maintenance

Successful preventive maintenance requires the performance of systematic inspections and maintenance programs.

Preventive maintenance consists of routine cleaning procedures and adjustments performed in compliance with schedules provided in the Preventive Maintenance Schedule.

5.3.1. Preventive Maintenance (PM) Schedule

NOTE

The drive assemblies are sealed units and therefore do not require PM procedures.

Table 5-1 provides the FE with a schedule suggesting what equipment requires PM, how often PM is required, and the procedure number to follow.

Table 5-1 Preventive Maintenance (PM) Schedule

ITEM	USAGE HOURS	PROCEDURE
Fan Filters	as required	5.3.1.1
Tape Drive Magnetic Head Cleaning	8 hours	5.3.1.2
Tape Cleaner Cleaning	8 hours	5.3.1.3
Motor Capstan Cleaning	8 hours	5.3.1.4
Heat Sink, Circuit Board, and Sensor Hole Cleaning	as required	5.3.1.5
Power Supply Voltage Checks as follows:	as required	5.4
AC Input Voltage Check	as required	5.4.1
CPU Module DC Voltage Test	as required	5.4.2
Disk/Tape Module AC Voltage Test	as required	5.4.3
Disk/Tape Module (Model 21 Plus) DC Voltage Test	as required	5.4.4
Disk/Tape Module (Model 31 Plus) DC Voltage Test	as required	5.4.5
Tape Cartridge Drive Voltage Adjustments	as required	5.4.6.

5.3.1.1. Fan Filters: The fan filters in the CPU module as well as the Disk Tape module should be visually inspected and cleaned as required.

The following steps are provided if the filter needs replacing:

1. Power-down the system (refer to Subsection 5.2, AC Power Removal).

2. Remove the CPU module and/or Disk/Tape module's side panel by unscrewing the four Phillips head screws.

NOTE

Perform the following steps only if it applies.

3. If the system has a removable filter, remove the two screws that secure the filter to the fan. Replace the filter if required.

   If the system has a grille, carefully clean the grille with a soft cleaning cloth. Avoid allowing any accumulated dust to drop into the system module.

5.3.1.2. Tape Drive Magnetic Head Cleaning: The magnetic head should be cleaned daily if the tape drive is in regular use (refer to Figure 5-1). Dirty heads can cause the loss of data during read and write operations.

CAUTION

Do not use spray cleaners as overuse will contaminate the motor bearings. Also, never use hard objects to clean the heads. Damage to the heads will result.

Use a nonresidue, noncorrosive cleaning agent, such as 99% isopropyl alcohol, and a soft cotton swab to clean the head assembly.

After completion, it is recommended that tape cleaner cleaning (5.3.1.3), and motor capstan cleaning (5.3.1.4) be included in the head cleaning PM schedule.

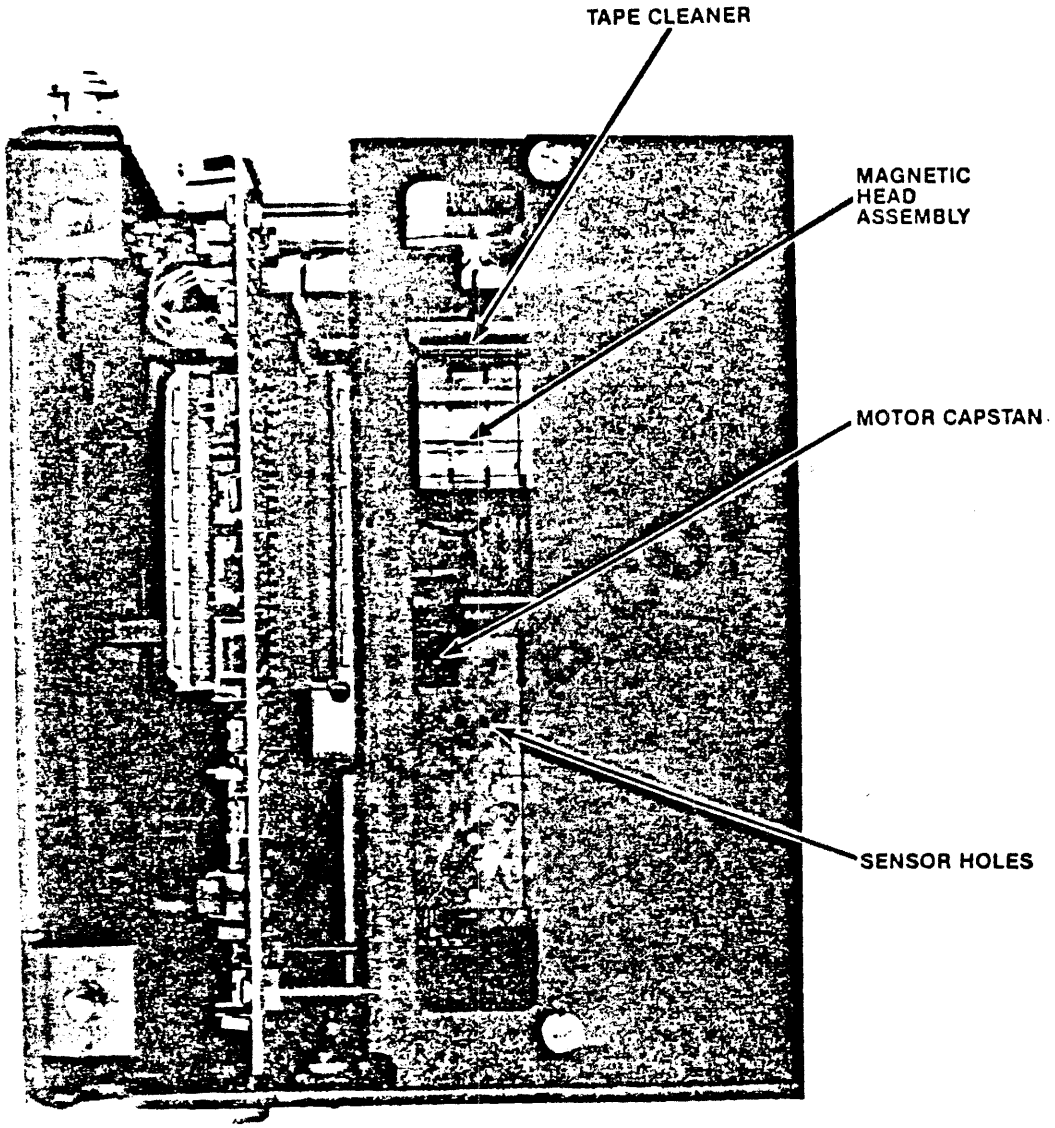


Figure 5-1 Tape Drive Maintenance Locations

5.3.1.3. Tape Cleaner Cleaning: The tape cleaner removes loose tape oxide and other foreign material from the tape before it contacts the head. This foreign material accumulates in and around the tape cleaner and must be removed. The tape cleaner should be cleaned on the same schedule as the head cleaning.

CAUTION

Do not use hard objects to clean the tape cleaner. If the tape cleaner becomes chipped, it will scratch the tape surface, resulting in lost data and/or permanent tape damage.

To clean the tape cleaner:

1. Insert a folded sheet of paper into the bottom of the cleaning slot of the cleaner.

2. Slide the paper up, lifting the foreign material from the tape cleaner.

3. Compressed air or a clean soft brush can be used to remove the foreign material from the area around the tape cleaner and head assembly. Alternatively, the tape cleaner can be cleaned using the same materials used to clean the magnetic heads.

CAUTION

Do not allow cleaning solvent to contaminate the drive motor bearings or damage to the motor could result.

5.3.1.4. Motor Capstan Cleaning: The drive capstan is composed of hard polyurethane and must be cleaned after foreign material has built up. Clean, using 99% isopropyl alcohol and a soft cotton swab. The cleaning schedule is the same as for the head cleaning (refer to Figure 5-1).

CAUTION

Be sure ac power is removed from the system.

5.3.1.5. Heat Sink, Circuit Board, and Sensor Hole Cleaning: To prevent possible overheating, dust and dirt must be removed from the heat sink and drive assembly components.

Use a soft brush and/or a clean source of compressed air. The sensor holes are cleaned in the same manner.

The time period between cleanings varies widely, depending on the operating environment.

NOTE

The SMD disk drive assembly is a sealed unit and therefore does not require PM procedures.

5.4. Power Supply Voltage Checks

NOTE

Power supply voltages should be checked by qualified Field Service (FE) personnel, and the voltages should be checked each time on-premise maintenance is performed.

The FE should ensure that each power supply is within tolerance to maintain normal system operations.

The following paragraphs are broken down as follows:

AC Input Voltage Check

CPU Module DC Voltage Test

Disk/Tape Module DC Voltage Test (Model 21 Plus)

Disk/Tape Module DC Voltage Test (Model 31 Plus)

Tape Cartridge Drive Voltage Adjustment

5.4.1. AC Input Voltage Check

NOTE

HP 3466A multimeter or equivalent is required to perform the following procedure.

Using the multimeter, check ac voltage at the facility outlet where the system will be plugged in. Ensure that the voltage reading is within the range specified by the switch settings on the CPU and Disk/Tape module power supplies.

5.4.2. CPU Module DC Voltage Test

The following steps check the CPU voltage:

1. Remove ac power, refer to Section 5.2.

2. Remove the module top cover by unfastening the captive fasteners at the rear of the cover. Pull the cover toward the rear of the module and remove it.

3. Remove the sheet metal cover on the front portion of the module. Lift the cover to clear the cover guides and pull toward the front of the module.

4. Test points are located in the upper right-hand corner of the card cage backplane. Unseat all boards in system prior to applying ac power.

5. Power up the system, reference ZEUS Administrator manual.

6. Check the following dc output voltages at their respective test points as shown in Figure 5-2.

   a. +5 Vdc +Ø.25/-Ø.1 at TP2

   b. +12 Vdc ±Ø.1 at TP3

   c. -5 Vdc ±Ø.1 at TP5

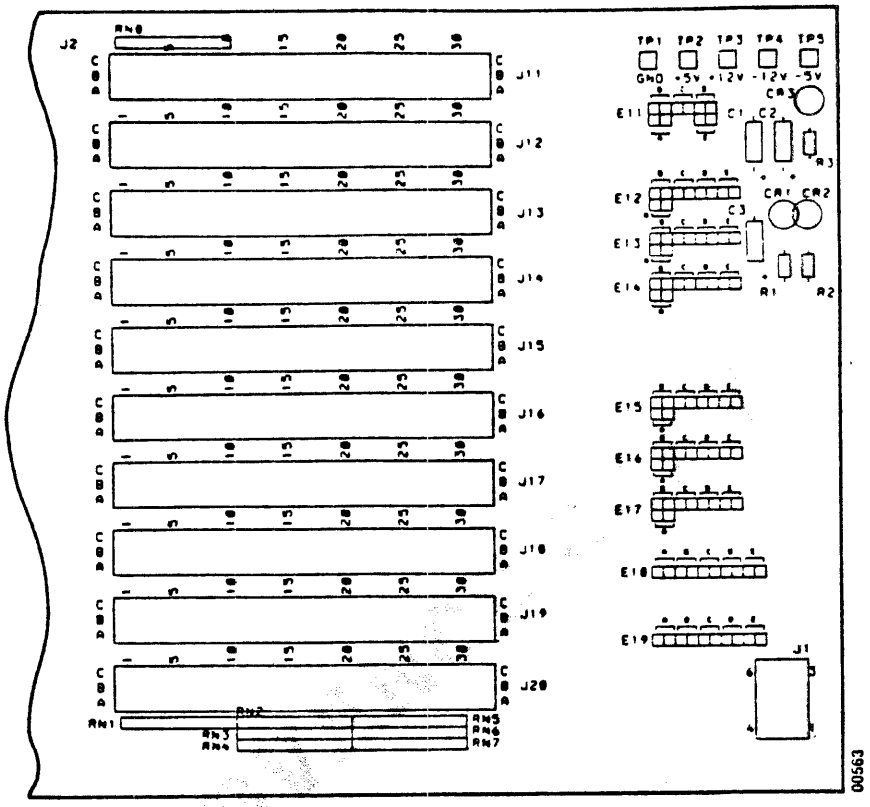


Figure 5-2 CPU Module Power Supply Voltage Test Points

4. Voltage adjustments can be checked at the following locations in the CPU module:

CAUTION

Do NOT adjust Power Fail. Doing so could cause system damage, or false power problems. Power Fail is set at the factory.

a. On the switching power supply, voltage adjustments are for +5 Vdc (V. ADJ.) and for Power Fail (PF).

b. Voltage adjustments on the linear power supply are for -5 Vdc (5 ADJ.) and +12 Vdc (12 ADJ.).

5.4.3. Disk/Tape Module (Model 21 PLUS) DC Voltage Test

The following steps check the dc voltage:

1. Using paragraph 3.3.2.4 "Disk/Tape Module Visual Inspection" as a reference, remove the CPU module from the top of the Disk/Tape module.

2.

3.

4. Do not re-install the CPU module until the Cartridge Tape/Drive voltage has been checked (refer to Section 5.3.5).

TO BE SUPPLIED

Figure 5-3 Disk/Tape DC Voltage Test Points
Model 21 Plus

5.4.4. Disk/Tape Module (Model 31 Plus) DC Voltage Test

The following steps test the dc voltage:

1. Using paragraph 3.3.2.4 "Disk/Tape Module Visual Inspection" as a reference, remove the CPU module from the top of the Disk/Tape module.

2. Drive voltage adjustments on the power supply are for +5Vdc (+5Vdc ADJ), -12Vdc (-12Vdc ADJ), and +24Vdc (+24Vdc ADJ). (See Figure 5-4 for locations.)

CAUTION

Ensure that the power connector (P2) is installed with Pin 1 oriented correctly to avoid damage to drive.

TO BE SUPPLIED

Figure 5-4 Disk/Tape DC Voltage Test Points
Model 31 Plus

5.4.5. Tape Cartridge Drive Voltage Adjustment

The following steps test and verify the tape cartridge drive voltage

1. Tape cartridge drive voltage adjustments may include one additional power supply output adjustment for the Disk/Tape module. Voltage adjustment for the -24Vdc can be checked at the connector labelled J2 on the power supply The +24 is Pin 5 (orange wire) and -24 is Pin 6 (violet wire). If the -24 is in need of adjustment, use the -24 Adj ±2% (refer to Figure 5-5).

2. Re-install the CPU module removed for Disk/Tape module dc voltage test.

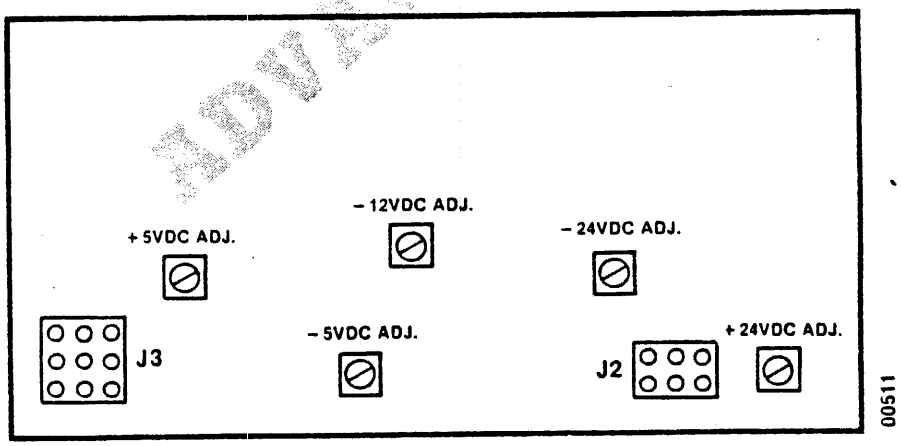


Figure 5-5 Disk/Tape Power Supply Voltage Adjustments

5.5. System Monitor

The system monitor program resides in a PROM plugged into the CPU. The monitor includes basic debugging commands, I/O control, and interface software for use with a serial interface to a remote computer system.

Refer to Appendix D for additional information about the monitor program.

5.6. System Parameters

System parameters are described in Table 5-4. The monitor program (refer to Appendix D) sets up program status blocks as provided in Table 5-5. Port addresses used in the monitor program are provided in Appendix D.

Table 5-4 System Parameters

NAME	PARAMETER
NULLCT	Null Count %43F6 This address stores the number of null characters that are inserted after a line feed. Modifying the null count adapts the system to the return delays of various terminals. NULLCT is initialized to Ø.
LINDEL	Line Delete %43F3 This address stores the character intercepted by the input line procedure as a line delete. When it is read from the terminal, this procedure purges the buffer and continues reading the input stream. LINDEL is initialized to %7F (RUB).
CHRDEL	Character Delete %43F2 This address stores the character intercepted by the input line procedure as a character delete. When it is read from the terminal, the last character entered is purged from the input buffer. Multiple character deletes can be used to delete the last n characters entered. CHRDEL is initialized to %Ø8 (control-h).

(continued)

Table 5-4 System Parameters (continued)

NAME PARAMETER

XOFCHR X/OFF Character %43F5

The character stored at this address is interpreted by the input interrupt procedure as a character that stops outputting data to the terminal.

When it is read from the terminal, all output is suspended until an X/ONCHR is received. XOFCHR is initialized to %3 (control-s).

X/ONCHR X/ON Character %43F4

The character stored at this address is interpreted by the input interrupt procedure as a character that resumes output after XOFCHR is entered.

When it is read from the terminal, all output is resumed. X/ONCHR is initialized to %11 (control-q).

STACK Stack Pointer %40A0

This address is the base of the user stack set by the monitor program at reset. The top of the stack is %4000.

PSAREA Program Status Area %4400

The Program Status Area for entering various interrupts and trap handling procedures starts at this address. This area includes the program status blocks (FCW and PC) for different types of interrupts and traps.

The monitor program sets up program status blocks. Refer to Table 5-5.

Table 5-5 Program Status Area

WORD	VALUE	COMMENT
Ø-1	unused	RESERVED
2-3	unused	RESERVED
4-5	unused	Unimplemented instruction
6-7	unused	Unimplemented instruction
8-9	unused	PRIVILEGED INSTRUCTION
A-B	unused	PRIVILEGED INSTRUCTION
C-D	%4ØØØ	SYSTEM CALL entered in Segmented mode
E-F	#BREAK	Address of BREAK interrupt procedure
1Ø-11	unused	SEGMENT TRAP
12-13	unused	SEGMENT TRAP
14-15	%4ØØØ	FCW for NONMASKABLE interrupt procedure
16-17	#NMINT	Address of NONMASKABLE interrupt procedure
18-19	unused	NONVECTORED INTERRUPT
1A-1B	unused	NONVECTORED INTERRUPT
1C-1D	%4ØØØ	FCW for all VECTORED INTERRUPTS
1E-1F	unused	VECTOR Ø
2Ø-21	unused	VECTOR 2
22-23	unused	VECTOR 4 -- CTCØ, CH.3
24-25	unused	VECTOR 6 -- BREAK and NEXT
26-27	unused	VECTOR 8
28-29	unused	VECTOR A
2A-2B	unused	VECTOR C
2C-2D	unused	VECTOR E
2E-2F	unused	VECTOR 1Ø
3Ø-31	unused	VECTOR 12
32-33	#PTYINT	VECTOR 14 (SIO Channel B input interrupt procedure address)
34-35	#CHASRC	VECTOR 16 (SIO Channel B special receive condition procedure address)
36-37	unused	VECTOR 18
38-39	unused	VECTOR 1A
3A-3B	#MCZINT	VECTOR 1C (SIO Channel A input interrupt procedure address)
3C-3D	#CHASRC	VECTOR 1E (SIO Channel A special receive condition procedure address)
3E-3F	unused	VECTOR 2Ø
4Ø-41	unused	VECTOR 22
42-43	unused	VECTOR 24
44-45	unused	VECTOR 26
46-47	unused	VECTOR 28
48-49	unused	VECTOR 2A
4A-4B	unused	VECTOR 2C
4C-4D	unused	VECTOR 2E
4E-4F	unused	VECTOR 3Ø

5.7. Removal and Replacement Procedure

The removal and replacement procedures that follow pertain to items most likely to be removed and replaced, as well as those items which are difficult or critical to remove and replace.

Before starting the removal and replacement procedures, power-down the system. Refer to Subsection 5.2 for the ac power removal procedure.

WARNING

THE SYSTEM MUST BE POWERED-DOWN BEFORE MAINTENANCE IS PERFORMED ON THE SYSTEM, OR PHYSICAL INJURY MAY RESULT.

This subsection contains removal and replacement procedures for the following:

System Disassembling Instructions

Model 21 Plus Disk Drive (TO BE SUPPLIED)

Model 31 Plus Disk Drive (TO BE SUPPLIED)

CPU Power Supply (TO BE SUPPLIED)

Disk/Tape Power Supply TO BE SUPPLIED

Memory Boards

Disk/Tape Cartridge Module (TO BE SUPPLIED)

5.7.1. System Disassembling Instructions

The following are the steps to disassemble the system. Be sure to remove ac power (refer to Section 5.2).

Be sure to label (when necessary) and save all hardware, ties, etc. for reassembling the system.

1. Disengage the thumbscrews, open the cable covers and remove the intermodule cables from the system.

2. Remove the terminal and printer cables from the I/O panel ports.

3. Loosen the captive fasteners on the rear of the CPU and Disk/Tape modules.

4. Disengage the CPU module from the guide posts on the front of the Disk/Tape module, and remove the module.

CAUTION

Be careful not to damage gaskets on the Disk/Tape module while performing Step 5.

5. Remove each of the modules, as described above.

5.7.2. CPU Power Supply

TO BE SUPPLIED

Disk/Tape Cartridge Drive Module

TO BE SUPPLIED

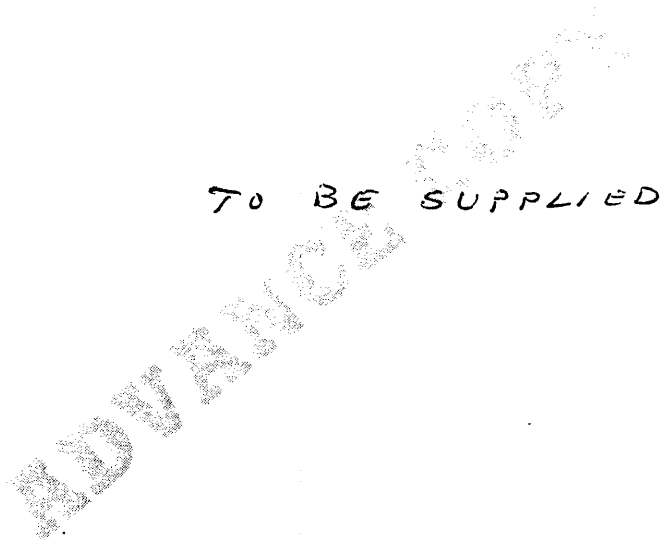


Figure 5-6 Tape Cartridge Drive Address Switch and Terminating Resistor

5.7.3. Disk/Tape Power Supply

To Be Supplied

NOTE

Be sure to re-install the CPU module. Reconnect ac power and daisy-chain the cables. Verify connections.

5.7.4. Memory Boards

The following paragraphs provide the instructions to remove and replace the memory boards, as well as set the memory address for the ECC Memory board and the Parity Memory board.

It is assumed that the system has been brought down and ac power has been removed. Reference Section 5.2 of this manual for ac power removal.

5.7.4.1 Parity Memory Board: Remove, replace, and set memory addressing for parity as follows:

1. Remove the front panel from the CPU module.

2. Each memory array board will require different settings for jumpers E4, E6, E19, and E17 to allow correct addressing. Memory segments must be allocated sequentially from Ø up; the largest arrays must occupy the lowest segment numbers.

NOTE

Use Table 5-7 with the following steps.

   a. Add the number of segments being installed in the system to the maximum segment number noted in step 1 above. (Addition of 256K bytes memory array adds four segments; addition of 512K bytes array adds eight, etc.)

   b. Set the new board jumpers to match this new highest memory segment. If 512K byte boards are mixed with 256K byte boards in a system, all 512K byte boards must be installed at lower segment numbers than the 256K byte boards.

3. As the correct jumper setting is made for each array board, install it in the card cage. Although the boards will work in any slot, it is recommended that the lowest order memory segments be put furthest from the CPU card. Tables 5-8, and 5-9 illustrate two cases of memory allocation.

4. Reconnect power to the system and power-up.

5. Press the RESET button. Verify that the system passes power-up diagnostics and the system indicates correct memory size.

Table 5-7 Parity Memory Addressing

MEMORY SEGMENT	SHUNT SETTINGS				MEMORY ARRAY SIZE
ØØ-Ø3	E4-E3	E6-E5	E19-E18	E17-E16	256K byte
Ø4-Ø7	E4-E8	E6-E5	E19-E18	E17-E16	256K byte
Ø8-ØB	E4-E3	E6-E9	E19-E18	E17-E16	256K byte
ØC-ØF	E4-E8	E6-E9	E19-E18	E17-E16	256K byte
1Ø-13	E4-E3	E6-E5	E19-E12	E17-E16	256K byte
14-17	E4-E8	E6-E5	E19-E12	E17-E16	256K byte
18-1B	E4-E3	E6-E9	E19-E12	E17-E16	256K byte
1C-1F	E4-E8	E6-E9	E19-E12	E17-E16	256K byte
2Ø-23	E4-E3	E6-E5	E19-E18	E17-E11	256K byte
24-27	E4-E8	E6-E5	E19-E18	E17-E11	256K byte

Table 5-8 System with 256K Bytes - Three Boards

MEMORY SEGMENT	SHUNT SETTINGS			MEMORY ARRAY SIZE
ØØ-Ø3	E4-E3	E6-E5	E19-E18	256K byte
Ø4-Ø7	E4-E8	E6-E5	E19-E18	256K byte
Ø8-ØB	E4-E3	E6-E9	E19-E18	256K byte
ALL	E17-E16	E15-E14	E21-E2Ø	

Table 5-9 System with 512K Byte and 256K Byte Boards

MEMORY SEGMENT	SHUNT SETTINGS			MEMORY ARRAY SIZE
ØØ-Ø7	E4-E3	E6-E5	E19-E18	512K byte
Ø8-ØF	E4-E3	E6-E9	E19-E18	512K byte
1Ø-13	E4-E3	E6-E5	E19-E12	256K byte
14-17	E4-E8	E6-E5	E19-E12	256K byte
ALL	E17-E16	E15-E14	E21-E2Ø	

5.7.4.2 ECC Memory Board: Remove, replace and set memory addressing for ECC as follows:

NOTE

H denotes hexadecimal value.

1. Each memory array board requires a different setting of switch SW1 to allow for correct addressing. Memory segments must be allocated sequentially from ØØ up; the largest memory arrays must occupy the lowest segment numbers. The sizes of the boards are provided as follows:

1M byte Array Board	1ØH segments
512K byte Array Board	Ø8H segments
256K byte Array Board	Ø4H segments

2. Set the switch elements of the largest array to address ØØ (refer to Table 5-1Ø).

3. Set the switch elements of the next largest array to the next highest memory segment. This segment changes with the size and number of installed array boards.

4. Repeat Step 3 for each array board.

NOTE

If ECC 1M byte array boards are mixed with 512K byte boards in a system, all 1M byte boards must be installed at lower segment numbers than the 512K byte boards. If 512K byte boards are mixed with 256K boards in a system, all 512K byte boards must be installed at a lower segment number than the 256K byte boards.

5. As the correct switch setting is made for each array board, install it in the card cage. Although the boards will work in any slot assigned to memory, it is recommended that the lower order memory segments be put furthest away from the ECC Controller board.

6. Reconnect power to the system and power-up.

7. Press the RESET button, then type in: T <CR>

   Verify that the system passes power-up diagnostics and indicates the correct memory size.

Table 5-10 Memory Boundaries (ECC)

MEMORY SEGMENT	SWITCH ELEMENT 8	7	6	5	4	3	2	1	MEMORY ARRAY SIZE
00-03	ON	ON	ON	ON	ON	ON	ON	ON	256K byte
04-07	ON	ON	ON	OFF	ON	ON	ON	ON	256K byte
08-0B	ON	ON	OFF	ON	ON	ON	ON	ON	256K byte
0C-0F	ON	ON	OFF	OFF	ON	ON	ON	ON	256K byte
10-13	ON	ON	ON	ON	ON	ON	ON	OFF	256K byte
14-17	ON	ON	ON	OFF	ON	ON	ON	OFF	256K byte
18-1B	ON	ON	OFF	ON	ON	ON	ON	OFF	256K byte
1C-1F	ON	ON	OFF	OFF	ON	ON	ON	OFF	256K byte
20-23	ON	ON	ON	ON	ON	ON	OFF	ON	256K byte
24-27	ON	ON	ON	OFF	ON	ON	OFF	ON	256K byte
28-2B	ON	ON	OFF	ON	ON	ON	OFF	ON	256K byte
2C-2F	ON	ON	OFF	OFF	ON	ON	OFF	ON	256K byte
30-33	ON	ON	ON	ON	ON	ON	OFF	OFF	256K byte
00-07	ON	OFF	ON	ON	ON	ON	ON	ON	512K byte
08-0F	ON	OFF	OFF	ON	ON	ON	ON	ON	512K byte
10-17	ON	OFF	ON	ON	ON	ON	ON	OFF	512K byte
18-1F	ON	OFF	OFF	ON	ON	ON	ON	OFF	512K byte
20-27	ON	OFF	ON	ON	ON	ON	OFF	ON	512K byte
28-2F	ON	OFF	OFF	ON	ON	ON	OFF	ON	512K byte
30-37	ON	OFF	ON	ON	ON	ON	OFF	OFF	512K byte
00-0F	OFF	OFF	ON	ON	ON	ON	ON	ON	1M byte
10-1F	OFF	OFF	ON	ON	ON	ON	ON	OFF	1M byte
20-2F	OFF	OFF	ON	ON	ON	ON	OFF	ON	1M byte
30-3F	OFF	OFF	ON	ON	ON	ON	OFF	OFF	1M byte

APPENDIX A
FIELD UPGRADE PROCEDURE RECORD LOG

SN#_____

Instructions

After installing a field upgrade, record the installation below Date the installation procedure and insert it sequentially in back of this log

RECORD LOG

DATE	SYSTEM MODEL	PROCEDURE TITLE/NO.	INSTALLER	COMMENTS

RECORD LOG

DATE	SYSTEM MODEL	PROCEDURE TITLE/NO.	INSTALLER	COMMENTS

APPENDIX B
MNEMONICS

The following is a listing of used mnemonics (terms) used throughout this manual, and their interpretation.

AD	- Address Data Lines
AM	- Address Mark
AS\	- Address Strobe
B/W\	- Byte-Word
BAI\	- Bus Acknowledge In
BAO\	- Bus Acknowledge Out
BCLK	- Bus Clock
BLKTAP	- Blank Tape
BPARM	- Bad DMA Parameters
BSY	- Busy
BUSREQ\	- Bus Request
BZ	- Drive Busy
CAI\	- CPU Acknowledge In
CAO\	- CPU Acknowledge Out
CAVAIL	- CPU Available
CPUREQ\	- CPU Request
CR:INIT	- Controller Initialization
CSE	- Controller Seek Error
CTCK1	- Control Check 1
CTCK2	- Control Check 2
CTCL	- Control Clock
CTO	- Controller Time Out
CTS	- Clear to Send
DAT	- Data Cyclic Redundancy Check
DE	- Disable Error
DF	- Drive Fault
DI	- Disable Implicit
DMA	- Direct Memory Address
DMFL	- DC Motor Failure
DS	- Drive Select
DSR	- Data Set Ready
DS\	- Date Strobe
DTR	- Data Terminal Ready
EWS	- Early Warning System
FWD	- Forward
FCW	- Flag Control Words
FMDET	- File Mark Detected
FT	- Fault
HWERR	- Hardware Error
I	- Interrupt
IEI	- Interrupt Enable In
IEI1	- Level-1 Interrupt Enable In

IEI2 - Level-2 Interrupt Enable In
IEI3 - Level-3 Interrupt Enable In
IEO - Interrupt Enable Out
IEO1 - Level-1 Interrupt Enable Out
IEO2 - Level-2 Interrupt Enable Out
IEO3 - Level-3 Interrupt Enable Out
ILCYL - Illegal Cylinder Check
INAP - Inappropriate
INT1\ - Level-1 Interrupt
INT2\ - Level-2 Interrupt
INT3\ - Level-3 Interrupt
INTMOT - Initial Seek Time Out
INVAL - Invalid
LNMGB - Linear Mode Guard Band
LPS - Load Point Sensed
LUN - Logical Unit Number
MCLK - Master Clock
ME\ - Memory Error
MFM - Modified Frequency Modulation
MMAI\ - Multimicro Acknowledge In
MMAO\ - Multimicro Acknowledge Out
MMREQ\ - Multimicro Request
N/S\ - Normal-System
NOTAP - No Tape Cartridge
NRZ - No Return to Zero
OC - On Cylinder
OVSHT - Overshoot Check
PC - Program Counters
PROT - Protected
PWRBAD\ - Power Bad
R/W\ - Read/Write
RD - Received Data
RDY - Ready
REV - Reverse
RO - Read Only
RTOGB - RTZ Outer Guard Band
RTS - Request To Send
RTZ - Return To Zero
RWCK1 - Read/Write Check 1
RWCK2 - Read/Write Check 2
RWCK3 - Read/Write Check 3
RWCK4 - Read/Write Check 4
RWD - Rewind
RXD - Receive Data
RY - Ready
SE - Seek Error
SEKGB - Seek Guard Band
SG - Signal Ground
SKE - Seek End
SM - Sector Mark
SLD - Select Drive

ST	- Status Lines
STOP	- Stop Line
TD	- Transmitted Data
TMOT	- Time-Out
TXD	- Transmit Data
TXRTN	- Transmit Return
VCMHT	- VCM Overheat
WDE	- Write Data Enable
W/LW\	- Word/Long-Word
WF	- Write Fault
XM	- Index Mark

APPENDIX C
CARTRIDGE TAPE ERROR CONDITIONS

C.1. General

Table C-1 lists the error conditions that can result from the commands that the tape controller receives from the host CPU. The table lists the commands, the resulting conditions, and the status bits which the conditions set.

Table C-1 Cartridge Tape Error Conditions

COMMAND RECEIVED	CONDITION	STATUS BITS SET
Initialization	Tape (if present) rewinds for more than 88 sec	INTV and HWERR
DIAG	ROM checksum error	INTV and HWERR
DIAG	FIFO test error	INTV and HWERR
DIAG	Handshake test failed	INTV and HWERR
Any command	No drive	CMDREJ, INTV, INAP, and HWERR
Any command	Host wrote to ports in byte or double word mode	CMDREJ
Any undefined command		CMDREJ and INVAL
Any command except DIAG	Drive busy, or drive not selected	CMDREJ, INTV, INAP, and HWERR
Any command except DIAG, MRTRY, SEL, MODE	No tape	CMDREJ, INTV, and NOTAP

Table C-1 Cartridge Tape Error Conditions (continued)

COMMAND RECEIVED	CONDITION	STATUS BITS SET
Any command except DIAG, MRTRY, SEL, LOAD, MODE	Tape not logically loaded	CMDREJ and INAP
WRITE, WFM EGP	Tape write-protected	CMDREJ, INAP, and PROT
LOAD	Tape already logically loaded	CMDREJ and INAP
READ, WRITE, SKBF, SKFF, EGP	Tape at logical end of tape	CMDREJ, INAP, and LEOT
SKBR, SKFR, REWIND	Tape at logical beginning of tape	CMDREJ, INAP, and LBOT
READ, WRITE	DMA buffer length greater than or equal to 32K bytes (K=1024 bytes)	CMDREJ and BPARM
READ, WRITE	DMA start address and DMA length greater than 24 bits	CMDREJ and BPARM
READ	DMA buffer length not even (bit 0=0)	CMDREJ and BPARM
READ	Blank tape (more than 48 inches) encountered	DATERR and BLKTAP
READ	Attempted buffer overflow during DMA	OVERFL

Table C-1 Cartridge Tape Error Conditions (continued)

COMMAND RECEIVED	CONDITION	STATUS BITS SET
READ, WRITE, WFM	Bad read (read after write for WRITE and WFM) as indicated by a bad CRCC after retrying the operation the maximum permissible number of times	DATERR
READ	File mark encountered	CMDREJ and FMDET
READ, WRITE	FIFO error (overflow or underrun) after retrying the operation the maximum permissable number of times	FFERR
WRITE	Deck stopped taking data during write	INTV and HWERR
READ, WRITE, WFM	One or more retry attempts made	RTRYAT and number of retries in low byte of status 1 register
Any command except READ, WRITE, WFM		Number of retries in low byte of status 1 register = Ø
WRITE, WFM	Encountered end of tape before WRITE began or retry after error pushes the beginning of the block past the end of tape	CMDREJ, INAP, and LEOT (and RTRYAT and number of retries in low byte of status 1 register if retries attempted)

Table C-1 Cartridge Tape Error Conditions (continued)

COMMAND RECEIVED	CONDITION	STATUS BITS SET
SKBF, SKFF	Encounterd logical end of tape	SKNDE and LEOT and number of blocks/files skipped in high byte of status 1
SKBR, SKFR	Encountered logical beginning of tape	SKNDNE and LBOT and number of blocks/files skipped in high byte of status 1
SKBF, SKFF	Blank tape (more than 48 inches) encountered	SKNDNE and BLKTAP and number of blocks/files skipped in high byte of status 1 register
SKBF, SKBR	File mark encountered	SKNDNE and FMDET and number of blocks skipped in high byte of status 1 register
SKBF, SKBR, SKFF, SKFR		Number of blocks/ files skipped in high byte of status 1 register
Any command except SKBF, SKBR, SKFF, SKFR		High byte of status 1 register = Ø
READ, WRITE, SKBF, SKFF, UNLD, REWIND, STRK	Rewind takes more than 88 seconds. Rewind occurs whenever track boundaries are crossed	INTV and HWERR

Table C-1 Cartridge Tape Error Conditions (continued)

COMMAND RECEIVED	CONDITION	STATUS BITS SET
SKFR	During forward motion (after FM detected) blank tape or end of tape encountered	INTV and HWERR
SKBR, SKFR, READ WRITE, WFM	During forward motion (after track boundary) tape failed to move off BOT for greater than 166 ms	INTV and HWERR
Any command	Tape write-protected	PROT
Any command	Tape at logical load point	LLP
Any command	Tape at end of tape	LEOT
Any command		UNITØ, 1 and TRKØ, 1 set to indicate unit and track selected. TRKØ, 1 = Ø if drive not logically loaded
READ, WRITE, WFM, SKBF, SKBR, SKFF, SKFR	Data detected for > 40" (32K bytes)	INTV and HWERR
REWIND, STRK, READ, WRITE, WFM, EGP, SKBF, SKBR, SKFF, SKFR	Tape moves forward > 2.1 sec and fails to move from BOT to LPS	INTV and HWERR

Table C-1 Cartridge Tape Error Conditions (continued)

COMMAND RECEIVED	CONDITION	STATUS BITS SET
READ, WRITE, WFM, SKBR, SEL, MODE	No block found where one is known to exist	INTV and HWERR
READ, WRITE, WFM	During retry blank tape found while moving in reverse	INTV and HWERR

APPENDIX D
MONITOR MODE PROGRAM

D.1. General

The explanations about the monitor program are provided as follows:

Monitor Program Software Environment

Monitor Program Conventions

Monitor Mode Commands

Monitor Program Download Mode Command

Monitor I/O Procedures

D.2. Monitor Program Software Environment

The monitor program software environment sets software breakpoints for program debugging. A breakpoint is a command that interrupts or stops program execution at a specified address in the program.

The address specified in the breakpoint is the address of the instruction. When encountered during program execution, the breakpoint suspends execution of the user's program and saves all registers, program Counters (PC), and the Flag Control Words (FCW) in the memory area provided. It then displays a message reporting the break and the address where it occurred.

Any number of breakpoints can be set manually by setting the instruction at the desired breakpoint address to %7FØØ (% indicates the address is in hexadecimal notation). This interrupts the executing program and jumps (traps) to the breakpoint procedure. When the breakpoint is no longer required, the original instruction must be manually restored.

The BREAK command saves the address where the breakpoint is being set and the instruction that it is replacing.

When the breakpoint is cleared, the instruction is automatically restored. The BREAK command also stores a repetition counter, n. Execution is not suspended until the nth time

this breakpoint is encountered unless another breakpoint is encountered first.

The steps that follow provide the restrictions necessary to set breakpoints.

1. This program must be able to execute with interrupts enabled after encountering the breakpoint.

2. The program should not be timing-dependent because there will be some timing distortion each time the breakpoint is encountered.

3. The user program must not use Channel 3 of the Z80B Counter Timer Circuit (CTC #0), because it is used to implement the multiple execution feature.

4. The breakpoint cannot be within an interrupt procedure entered by an interrupt from Channels 0 through 2 of the Z80B CTC #0.

The BREAK and the NEXT commands use instruction modification and the interrupt system. Therefore, the program being debugged cannot be in the PROM area and cannot involve modification of the interrupt status.

Any set breakpoints must be cleared by hitting RESET before a new program is loaded from the system; otherwise, previously set breakpoints continue to operate on the new program during debugging.

The user stack is used whenever a JUMP or GO command is executed. The command must be set to some address within writable memory.

If the JUMP or GO address has a system breakpoint set, it does not cause suspension of execution.

D.3. Monitor Program Conventions

The following conventions are used in command descriptions:

< > Angle brackets enclose descriptive names for the quantities to be entered.

[ ] Square brackets denote optional quantities.

A bar denotes an OR condition. For example, W|B means either W or B can be used.

<CR> Carriage Return and linefeed.

[A single square left bracket is the monitor prompt.

% Symbol for hexadecimal value, for example %4F or %4FFF.

Apply the following when entering commands and options:

1. All commands and options must be entered in uppercase.

2. Commands can be abbreviated to the first letter.

3. Numbers are represented in hexadecimal notation.

4. The first character typed on a new line identifies which command is being invoked. If an invalid character is entered, a "?[" is displayed, prompting a new command.

5. Addresses are specified by an optional segment number in angle brackets, followed by a hexadecimal address. If no segment number is specified, segment Ø is assumed.

   For example, <ØØ>4ØØØ or 4ØØØ, <ØØ>Ø or Ø, <Ø1>F8ØØ or F8ØØ for segment Ø.

D.4. Monitor Mode Commands

A summary of Monitor mode commands and its parameters with examples are provided in Table D-1. The identifier numbers in Table D-1 (1 through 14 located in column one) have been provided for command identity only.

NOTE

All outputs in Monitor mode can be suspended with X/OFF (%13 or control-s) and resumed with X/ON (%11 or control-q).

Table D-1 Monitor Mode Commands

IDENTIFIER	COMMAND NAME(Syntax)	PARAMETERS
1	DISPLAY(D)	<address> [<# of long words/words/bytes>] [L|W|B] Display and alter memory
2	REGISTER(R)	[<register name>] Display and alter registers
3	BREAK(B)	[<address>] [<n>] Set and Clear breakpoint
4	NEXT(N)	[<n>] Step instruction
5	GO(G)	Branch to last PC set in user register array
6	JUMP(J)	<address> Branch to address
7	FILL(F)	<address1> <address2> <data> Fill memory
8	IOPORT(I)	<port address> [W|B] I/O port read/write
9	MOVE(M)	<address1> <address2> Move memory block
1Ø	COMPARE(C)	<address1> <address2> Compare memory blocks
11	QUIT(Q)	Enter Transparent mode
12	PORT(P)	<port address> [W|B] Special I/O read/write
13	TEST(T)	Enter Test mode
14	ZBOOT(ZD,ZS,ZT)	Read BOOTSTRAP prog(s) from SMD*,disk/cartridge tape, execute: ZD = Read BOOTSTRAP from mWDC-II* ZS = Read BOOTSTRAP from SMD* ZT = Read BOOTSTRAP from Tape

* Note mWDC-II = Model 21 Plus, SMD = Model 31 Plus.

1
COMMAND NAME: DISPLAY

SYNTAX: D <address> <# of long words/words/bytes> [L|W|B]

DESCRIPTION:
This command displays at the terminal the contents of specified memory locations starting at the given address for the given number of bytes. If the count parameter is specified, the contents of the memory locations are displayed in hexadecimal notation and as ASCII characters.

If the count parameter is not specified, the memory locations are displayed as words one at a time, with an opportunity to change the contents of each location.

For each location, the address is displayed, followed by the contents of L|W|B and a space. To change the contents at a given location, enter the new contents in the form long word|word|byte. If RETURN is pressed, either alone or after the new contents, the next sequential location is displayed. Entering a "Q" for QUIT), followed by a RETURN terminates the command.

EXAMPLE:

Display memory starting at Segment Ø, %52ØØ for 16 words.
D 52ØØ 1Ø <CR>

ØØ> 52ØØ 18Ø8 FE2B 2ØØ4 D923 7ED9 CD35 2238 OAED
5"8..*
ØØ> 521Ø 6F23 ED6F 2B1E Ø118 EDD9 2218 14D9 5778
o#.o+...H...Wx*

EXAMPLE:

Display memory starting at Segment Ø, %52ØØ for 16 bytes. D 52ØØ 1Ø B <CR>

<ØØ> 52ØØ 18 Ø8 FE 2B 2Ø Ø4 D9 23 7E D9 CD 35 22 38 OA ED
...+..#...5"8..

EXAMPLE: Display memory location Segment Ø, %52ØØ and alter its contents. [D 52ØØ <CR>

<ØØ> 52ØØ 18Ø8 ?1922 <CR> <ØØ> 52Ø1 FE2B ?<CR> <ØØ> 52Ø2 2ØØ4 ?<CR>

2
COMMAND NAME: REGISTER

SYNTAX: R [<register name>]

DESCRIPTION:
The REGISTER command is used to examine or modify a specified register. If no register name is given, all registers RØ, R1, R2 ... R15 PC and FCW are displayed. If a register name is given, the specified register name is displayed, followed by a space. To change the contents of that register, enter the new contents followed by <CR>. CR> alone or after the new contents displays the next register. A "Q" followed by a <CR> terminates the command.

The following register names can be used in the command:

1. Any of the sixteen 16-bit registers named RØ, R1, R2 ... R15.

2. Any of the sixteen 8-bit registers named RHØ, RLØ, RH1, RL1 ... RH7, RL7.

3. Any of the eight 32-bit registers named RRØ, RR2, RR4 ... RR14.

4. Program counter register named PC.

NOTE

The new contents of the program counter must be given in even hexadecimal numbers.

5. Flag and control word named FC.

EXAMPLE:

Display all registers.
[R <CR>

```
RØ   R1   R2   R3   R4   R5   R6   R7   SG   PC   FC   RF
ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ

R8   R9   R1Ø  R11  R12  R13  R14  R15  N4   N5   PS   PO
ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ
```

COMMAND NAME: REGISTER (continued)

EXAMPLE:

Display 32-bit word register RR4 and alter its contents.
[R RR4 <CR>

RR4 ØØØØØØØØ ?A2557FFFF <CR>

RR6 ØØØØØØØØ ?Q <CR>

3
COMMAND NAME: BREAK

SYNTAX: B [<address>] [<n>]

DESCRIPTION:
The BREAK command sets a breakpoint at a given even address after clearing any previously set breakpoint.

If <n> is given, program execution is not interrupted until the nth time the breakpoint instruction is encountered (<n> is in the range %1-%FFFF).

If <n> is not given, 1 is assumed.

If the BREAK command is issued with no parameters, any previously set breakpoint is cleared.

When program execution is suspended by the BREAK command, the monitor program displays a message reporting the break and the address where it occurred.

EXAMPLE:

[B 6A5E <CR>

Message: BREAK AT 6A5E

EXAMPLE:

[D 8ØØØ <CR>
<ØØ> 8ØØØ (XXXX)? <8DØ7> <CR>
<ØØ> 8ØØ2 (XXXX)? <Q> <CR>
[B 8ØØ2 <CR>
[J 8ØØØ <CR>
BREAK AT 8ØØ2
[

4
COMMAND NAME: NEXT

SYNTAX: N [<n>]

DESCRIPTION:
The NEXT command causes the execution of the next n machine instructions, starting at the current PC, and displays all registers after executing each instruction.

(<n> is in the range %1-%FFFF.) If <n> is not given, 1 is assumed.

EXAMPLE:

```
[F 8000 9000 8D07 <CR>
[D 9000 <CR>
<00> 9000 8D07 ? <7F00> <CR>
<00> 9002 XXXX ? <Q> <CR>
[R SG <CR>
RSG XXXX ? <0> <CR>
RPC XXXX ? <8000> <CR>
RFC XXXX ? <C000> <CR>
RRF XXXX ? <Q> <CR>
[N <CR>
R0  R1  R2  R3  R4  R5  R6  R7  SG    PC    FC    RF
X   X   X   X   X   X   X   X   0000  8002  C000  X
R8  R9  R10 R11 R12 R13 R14 R15 N4  N5  PS  PO
X   X   X   X   X   X   X   X   X   X   X   X
[N2 <CR>
R0  R1  R2  R3  R4  R5  R6  R7  SG    PC    FC    RF
X   X   X   X   X   X   X   X   0000  8004  C000  X
R8  R9  R10 R11 R12 R13 R14 R15 N4  N5  PS  PO
X   X   X   X   X   X   X   X   X   X   X   X
R0  R1  R2  R3  R4  R5  R6  R7  SG    PC    FC    RF
X   X   X   X   X   X   X   X   0000  8006  C000  X
R8  R9  R10 R11 R12 R13 R14 R15 N4  N5  PS  PO
X   X   X   X   X   X   X   X   X   X   X   X
[
```

5
COMMAND NAME: GO

SYNTAX: G

"DESCRIPTION:
This command causes a branch to the current PC, continuing program execution from the location where it was last interrupted. All registers and the FCW are restored before branching.

EXAMPLE: ".lp Execute/continue executing program [G <CR>.

6
COMMAND NAME:
"JUMP

SYNTAX: J <address>

DESCRIPTION:
The JUMP command branches unconditionally to the given even address. All registers and the FCW are restored before branching.

EXAMPLE:

Execute user program starting at %5000.
[JUMP 5000 <CR>

7
COMMAND NAME: FILL

SYNTAX: F <address1> <address2> <data>

DESCRIPTION:
The FILL command stores the given data word in a memory location, from address1 to address2. The command address must be an even hex number.

EXAMPLE:

Store data FFFF in memory from %5400 to %5410.
[F 5400 5410 FFFF <CR>
[

8
COMMAND NAME: IOPORT

SYNTAX: I <port address> [W|B]

DESCRIPTION:
This command reads data in either byte or word form from the given port address and displays the value.

Enter a hex value to be output to the specified port; or enter only if the W|B parameter is not given, byte data is read from the I/O port.

EXAMPLE:

Output data FF to port address %FF29.
[I FF29 <CR>
FF29 ØØ ? <FF> <CR>
[

9
COMMAND NAME: MOVE

SYNTAX: M <address1> <address2> <n>

DESCRIPTION:
This command moves the contents of a block of memory from the source address specified by <address1> to the destination address specified by <address2>. <n> is the number of bytes to be moved.

EXAMPLE:

Move memory from address %5ØØØ to %6ØØØ for 256 bytes.
[M 5ØØØ 6ØØØ 1ØØ <CR>

1Ø
COMMAND NAME: COMPARE

SYNTAX: C <address1> <address2> <n>

DESCRIPTION:
This command compares the contents of two blocks of memory. <address1> and <address2> specify the starting addresses of the two blocks, and <n> specifies the number of words to be compared. If any locations of the two blocks differ, the addresses and contents of those locations are displayed.

COMMAND NAME: COMPARE (continued)

EXAMPLE:

Compare two blocks of memory with starting addresses %4000 and %5000 for 32 words.

```
[C 4000 5000 20 <CR>
[
or on MISCOMPARE:
<00> 5000=XX <00> 4000=YY
[
```

11
COMMAND NAME: QUIT

SYNTAX: Q

DESCRIPTION:
The QUIT command is used to enter Transparent mode from Monitor mode.

In Transparent mode, all keyboard inputs and console outputs are passed between the remote computer system and the local system. The console controls the remote computer operating system. Channels A and B of the SIO2 must be set to the same baud rate when operating in Transparent mode. (The remote system connects to TTY0 on the rear panel of the local system.)

The START switch on the System 8000 is used to return to Monitor mode.

12
COMMAND NAME: PORT

SYNTAX: P <port address> [W|B]

DESCRIPTION:
The PORT command is similar to the IOPORT command; however, it is used to read or write special I/O devices.

EXAMPLE:

```
[P FC <CR>
00FC XX ? <CR>
[
```

13
COMMAND NAME: TEST

SYNTAX: T

DESCRIPTION:
The TEST command executes the SPUD System Power-Up Diagnostic tests. (See Section 3, paragraph 3.4.6 and Appendix E for more information.)

EXAMPLE:

T <CR>

14
COMMAND NAME: ZBOOT

SYNTAX: Z [D|S|T]

DESCRIPTION:
This command is commonly used to manually bootstrap the ZEUS Operating System. The ZBOOT command reads a 512-byte program from block Ø of the device determined by S/SMD, T/Tape Cartridge. Generally, there is no return to the monitor.

EXAMPLE:

Z T <CR>

D.5. Monitor Program Download Mode Command

NOTE

Filenames can be specified in either uppercase or lowercase. Filenames can be full pathnames.

Download mode transfers data to the system from a remote computer system. Channels A and B of the SIO2 must be set to the same baud rates when operating in Download mode. (The remote system is connected to TTYØ on the rear panel.)

The LOAD program is required on the remote system to perform download functions through console I/O. A summary of commands in Download mode are provided in Table D-2. A description of the command name LOAD follows the discussion about the format of the LAST RECORD.

Table D-2 Download Mode Commands

COMMAND NAME	PARAMETER
LOAD	<filename> Load S/W from System 8000

The Download mode uses the Tektronix record format, which uses only ASCII characters. Each record contains two checksum values, a starting address, and a maximum of 30 bytes of data.

The format of the record(s) is: RECORDS 1 to n

<address(4)> <count(2)> <checksum1(2)> <data(2)>...
<data(2)> <checksum2(2)> <carriage return>

where:

<address(4)>:	Is the address of the first byte of data in the record (address is represented in four ASCII characters)
<count(2)>:	is the number of <data> in current record (two ASCII characters)
<checksum1(2)>:	is the checksum for the address and count field (two ASCII characters)
<data(2)>:	is the value of byte data (represented in two ASCII characters)
<checksum2(2)>:	is the checksum for the data portion of the record (two ASCII characters)
<carriage return>:	indicates the end of the record

No segment information is transferred. All downloaded data is loaded into segment 0 with the LOAD command. Data for segments other than 0 must be transferred to Segment 0 by the MOVE command.

The format of the last record is: LAST RECORD

<entry address(4)> ØØ <checksum(4)> <carriage return>

where:

<entry address>: is the starting execution address for the program.

<checksum>: is the checksum for the entry address.

NOTE

A record with ØØ in the count field indicates the end of load data.

If either the local or remote system has to abort the load process, it sends a RECORD WITH ERROR MESSAGE of the form:

/ <error messages in ASCII text> <carriage return>

ACKNOWLEDGE

During the loading process, after each record is received from the remote system, an acknowledge (ASCII Ø) is sent when the checksum values are verified.

If a nonacknowledge (ASCII 7) is received, the remote system attempts to load the same data record up to ten times. After the tenth try, the monitor program returns to Monitor mode for the next command.

An abort-acknowledge (ASCII 9) is sent to the remote system if the escape (ESC) key is pressed, aborting the loading process. The monitor program then returns to Monitor mode for the next command.

The address used in the data record during the loading process is provided by the file description record; it must be greater than %8ØØØ.

The following is a description of the command name LOAD.

COMMAND NAME: LOAD

SYNTAX: L <filename>

DESCRIPTION:
This command downloads a Z8000 program named <filename> that resides in the remote system. The monitor program transmits the exact command line to the remote system.

The command causes a remote procedure file (LOAD) to be executed, to open the file specified by <filename>. The binary data in the file is converted to Tektronix record format and transmitted to the local system.

The monitor program verifies the two checksum values in the receiving record and stores the data in RAM memory as specified by the address indicated in the record. An acknowledgement from the system causes the next record to be downloaded from the remote system. A nonacknowledgement from the remote system causes the current record to be retransmitted up to ten times, after which a record with an error message is sent, and the monitor program returns to Monitor mode.

The LOAD program in the remote system is also aborted. When the loading process is complete, the entry point received on the first record is displayed.

Pressing ESC aborts the LOAD command. Any breakpoints set from a previous program must be cleared before a new program is loaded from the remote system. (Ensure that the remote system is connected to TTY0 on the rear panel).

ERROR MESSAGES:

/ABORT
/UNABLE TO OPEN FILE (XX), where (XX) is the ZEUS error code from the remote system
/FILENAME ERROR
/NOT PROCEDURE FILE
/ERROR IN READING FILE (XX), where (XX) is the ZEUS error code from the remote system
/RECORD CHECKSUM ERROR

EXAMPLE:

Transfer file names MYFILE from the remote system to the local system RAM memory.

[LOAD MYFILE <CR>

NOTE

The address of RAM memory and the entry address used in the download process are provided by the information in the descriptor record of the file specified by <filename> in the LOAD command.

D.6. Monitor I/O Procedures

The I/O procedures most frequently used in the monitor program are:

TYIN

TYWR

PUTMSG

TTY

CRLG

These procedures are accessed by system calls in user programs to perform console I/O functions.

NOTE

Refer to the ZEUS Adminstrator and Reference Manuals.

PROCEDURE NAME: TYIN

DESCRIPTION:

Gets a character from the keyboard buffer. If the buffer is empty, this procedure waits for a character to appear. The character is stored in register RLØ, and the contents of register RHØ are lost.

EXAMPLE:

```
CONSTANT
     TYIN :=%Ø4
          .
          .
          .
     SC    #TYIN
```

Port addresses provided in the following table are used in the monitor program.

Table D-3 System Hardware I/O Port Addresses

PORT	ADDRESS
CTC CHANNEL Ø	FFA1
CTC CHANNEL 1	FFA3
CTC CHANNEL 2	FFA5
CTC CHANNEL 3	FFA7
SIO DATA CHANNEL A	FF81
SIO DATA CHANNEL B	FF83
SIO CONTROL CHANNEL A	FF85
SIO CONTROL CHANNEL B	FF87
RETI PORT	FFE1
SYSTEM CONFIGURATION PORT (or REGISTER)	FFC1 - 2 bits baud rate, 2 bits boot device, 4 bits other configurations

APPENDIX E
SYSTEM POWER-UP DIAGNOSTIC (SPUD) ERROR LIST

ERROR #	P1	P2	P3	P4	CHRS * PRINTED	DESCRIPTION
0000	—	—	—	—	P	No External Memory**
0001	SEG #	ADDR	RD	—	O	Seg. Addr Fault **
0100	SEG #	ADDR	TD	RD	W	Mem. Addr Fault
0101	SEG #	ADDR	TD	RD		Data Line Fault
0102	SEG #	ADDR	TD	RD		'As' Data Fault
0103	SEG #	ADDR	TD	RD		'5s' Data Fault
0104	—	—	—	—		No Good Segments Above Zero**
0100	SEG #	ADDR	TD	RD	E	Segment Zero Memory Test
0101	SEG #	ADDR	TD	RD		(Descriptions As Above)
0102	SEG #	ADDR	TD	RD		
0103	SEG #	ADDR	TD	RD		
0200					R (sp)	ECC Single-bit Correction Failure
0201					U	ECC two-bit trap failure
0202					P (sp)	ECC two-bit error not reported
0203	SEG #	ADDR				ECC Check Byte RAM error
0300	MMU PORT #	SDR FIELD #	TD	RD	D	MMU's Not Individually Addressable
0301	MMU PORT #	SDR FIELD #	TD	RD		SAR or DSCR Indexing Fault
0302	MMU PORT #	SDR FIELD #	TD	RD		SDR 'As' or '5s' Data Fault
0303	MMU CMD #	TD	RD	—		MMU Control Register 'As' or '5s' Fault
0304	REG #	TD	RD	—		System/Normal Break Register 'As' or '5s' Fault
0305	MMU ID #	SDR #	VDAT	—	I	Stack MMU Did Not Trap On Limit Test
0305					A	Unexpected Trap
0305					G	Unexpected Trap
0305					N	Data MMU Did Not Trap On Limit Test
0305					O	Stack MMU Did Not Trap On Read-Only Test
0305					S	Data MMU Did Not Trap On Read-Only Test
0306	MMU Port #	SDR #	TD	RD	T	Translation Fault On Data MMU
0307	MMU PORT #	SDR #	VDAT	—		Unexpected Trap
0308	MMU PORT #	SDR #	TD	RD	I	Translation Fault On Stack MMU
0309	MMU PORT #	SDR #	VDAT	—		Unexpected Trap
0310	MMU PORT #	SDR #	TD	RD	C	Translation Fault On Code MMU
0311	MMU PORT #	SDR #	VDAT	—		Unexpected Trap
0312	MMU PORT #	SDR #	—	—	S (sp)	No Trap On Code MMU Limit Test

SPUD Error List (continued)

ERROR #	P1	P2	P3	P4	CHRS * PRINTED	DESCRIPTION
1000	—	—	—	—		No m-WDC Board In System
1001	DS1	DS2	DS3	DS4		m-WDC Self Test Error
1002	—	—	—	—		m-WDC Drive 0 Error
2000	—	—	—	—		No TCC Board In System
2001	—	—	—	—		Busy Bit Always Set***
2002	REG #	TD	RD	—		'5s' Data Fault
2003	REG #	TD	RD	—		'As' Data Fault
2004	IV REG	STATO REG	MIC REG	—		TCC Self-Test Error***
2005	IV REG	STATO REG	MIC REG	—		TCC Hardware Error***
3000						m-WDC Not Responding
3001	ADDR	—	—	—		RAM Error (P1 holds location)
3002						PROM Checksum Error
3003						Time Out Condition
3004						Read ABORT Error
3005						Wait ABORT Error
3006						Parity Error
3007						Not Used But Reserved
3008						Seek Not Complete Error
3009						Cylinder Not Found
3010						Drive Not Selected
3011						Head/Secter Not Found
3012						Invalid Command
3013						No Track 0 Found
3014						Drive Not Ready
3015						Bad Interrupt
3016						Bad MAP
3017						Illegal Cylinder Selected
3018						BEP Error
4000						SMC Not Responding
4001						SMC Initialization Error
4002						SMC RAM Error
4003	STATUS	—	—	—		SMC Self Test Timed Out Host Waiting (P1 holds SMC status register)
4004						Drive 0 Not Selected
4005						Drive 0 Not Ready
4006						Drive 0 Not On Cylinder
4007						Drive 0 Read Only
4008						Drive 0 Drive Fault
4009						Drive 0 Seek Error
4010						Drive 0 Not Formatted (Can't Size Disk)
COMPLETE						Last Characters of SPUD Message

SPUD Error List (continued)

LEGEND

* — Characters of SPUD message printed before entering test

** — Fatal error preventing further memory-related tests from being run

*** — The TCU test may take up to two minutes if the drive is busy or if the 'busy' status bit is stuck. The last two TCU error messages dump out the contents of the status registers for troubleshooting.

Pn — Test parameters of error printed (in hexadecimal):

SEG #	—	segment number
ADDR	—	address offset
TD	—	test data
RD	—	returned data
MMU PORT #	—	full work port number of MMU under test
MMU CMD #	—	MMU port number with command 'ored' in
SDR FIELD #	—	indicates a particular SDR in the range 0-255
MMU ID #	—	ID of MMU(s) returned from a segment trap
	—	1 = code MMU
	—	2 = data MMU
	—	4 = stack MMU
SDR #	—	logical segment number or set of SDR's (0-63)
VDAT	—	violation data from a single MMU trapping
	(HB)—	bus cycle status register data
	(LB)—	violation type register data
DS1	—	WDC detailed status - always 0
DS2	—	- always 0
DS3	—	- operation error status
DS4	—	- self-test error status
REG #	—	register port number of unit under test
—	—	no parameter printed
STATUS	—	SMC status port contents

When the diagnostics are complete, the maximum available segment number will be displayed as follows (xx in hexadecimal):

MODEL 21 PLUS (STD.CONFIG.)

POWER UP DIAGNOSTICS
ACTIVE PERIPHERALS:
  WDC
  TCC
  ECC (optional)
  SSB0, SSB1 (optional)
  MTC (optional)
  ICP0-7 (optional)
COMPLETE
SEGMENTED JUMPERS
MAXSEG = <xx>

MODEL 31 PLUS (STD.CONFIG.)

POWER UP DIAGNOSTICS
ACTIVE PERIPHERALS:
  SMC
  TCC
  ECC
  SSB0, SSB1 (optional)
  MTC (optional)
  ICP0-7 (optional)
COMPLETE
SEGMENTED JUMPERS
MAXSEG = <xx>

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