

# DISK CONTROLLER AND DRIVES

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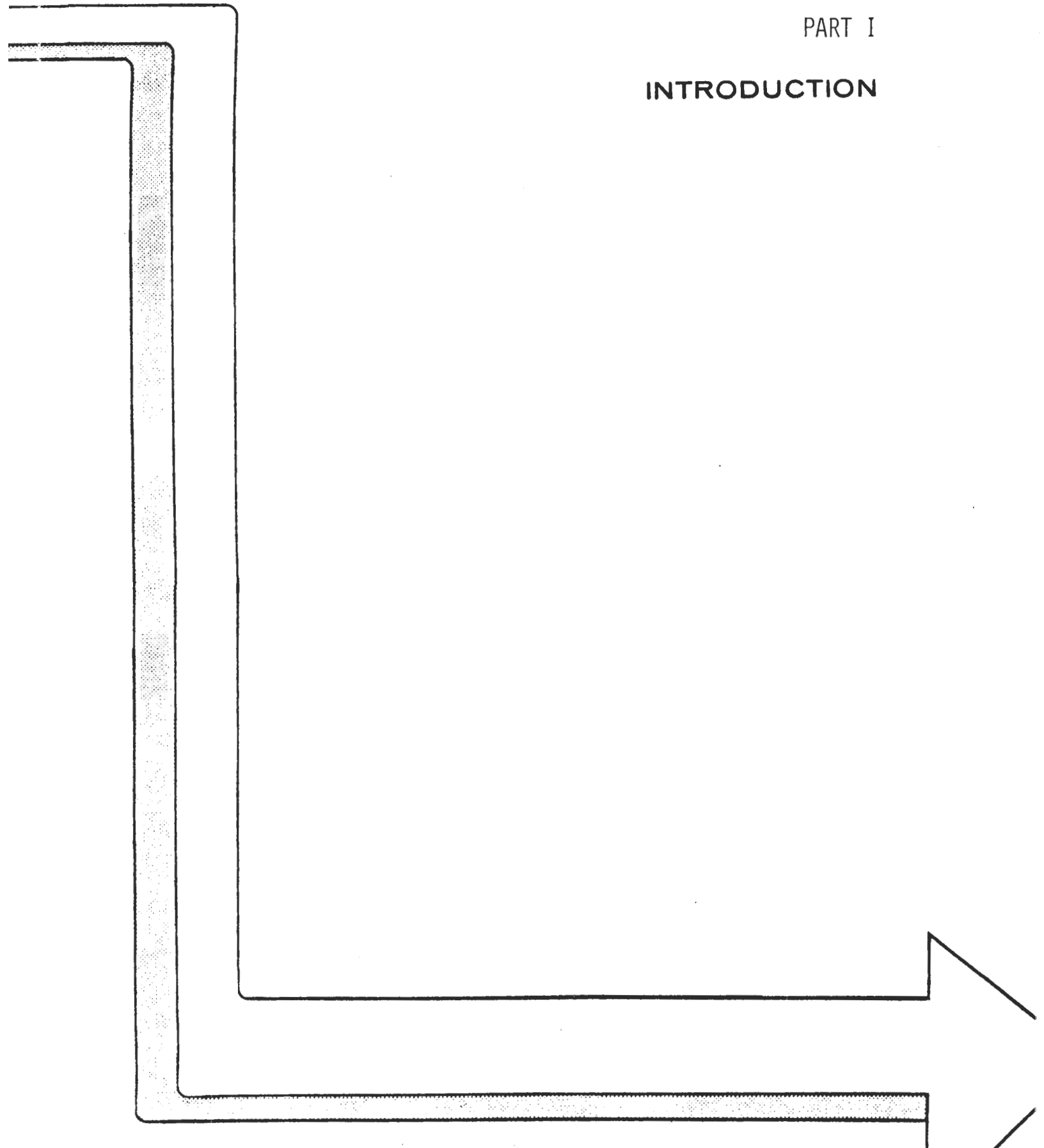
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PART I

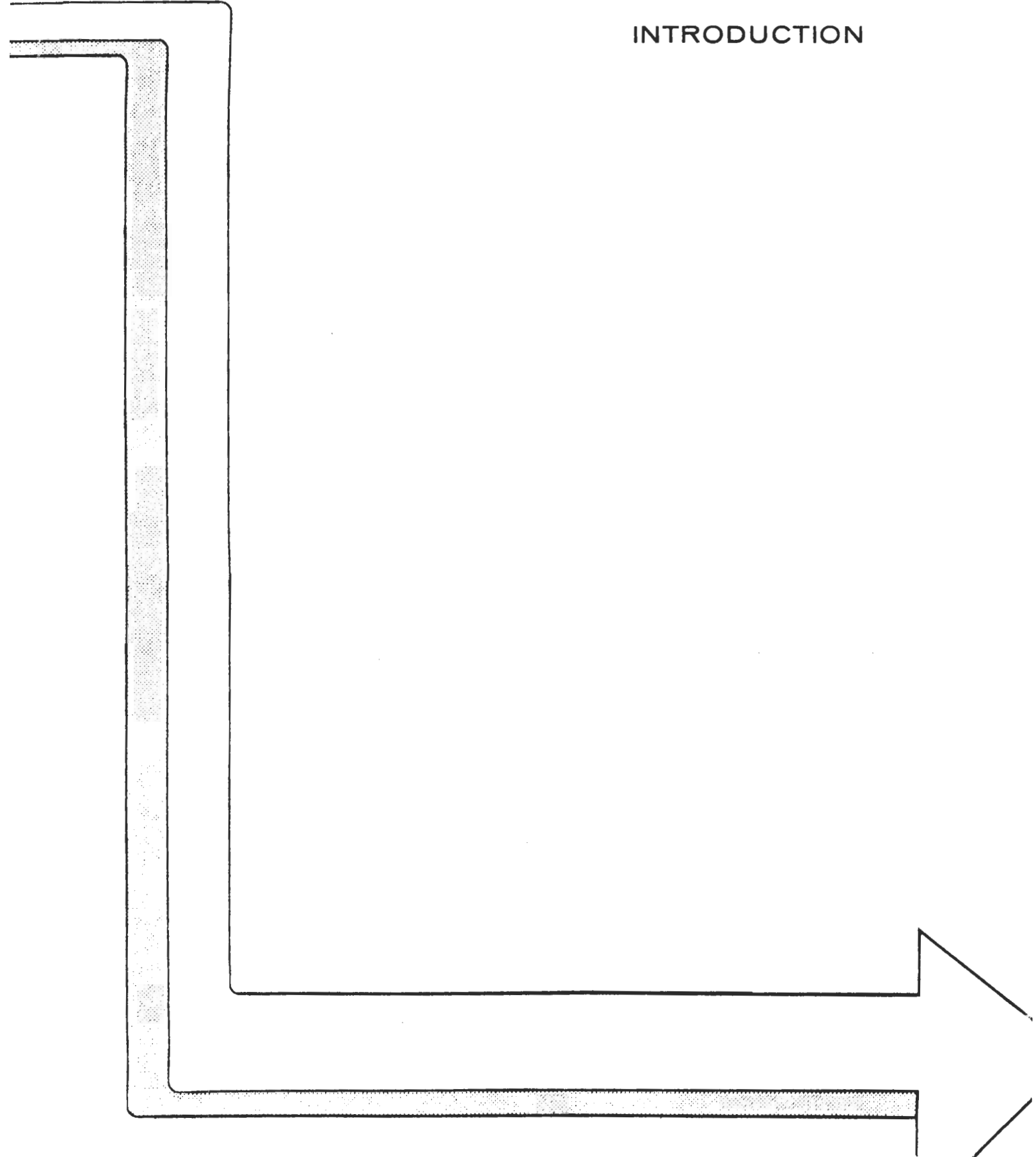
**INTRODUCTION**







# INTRODUCTION





The Z-207 is a floppy disk controller board. It functions as an intelligent interface between the CPU and the disk drives. The Z-207 selects the correct drive in a multi-drive system and properly handles the data flow to and from the drives. This allows the H/Z-100 to store and retrieve large quantities of data.

The Z-207 operates as a slave processor. This means the disk controller board contains its own processor which is controlled by the master CPU. Thus, the disk controller board takes commands from the master CPU and converts them into the necessary signals required to control the drives. This type of system allows the master CPU to do other tasks while the disk controller board processor actually does the work of controlling the disk drives.

The Z-207 is versatile. It can support up to four 5-1/4" and four 8" disk drives. User software will select the type of drive used and the density of the media. However, present Heath Company software limits the number of drives to three.

The Z-207 can be operated in three different modes; Wait State, Polled I/O, or Interrupt. This allows the disk controller board to support almost all available soft-sectored disk formats. When placed in the H/Z-100, the disk controller board uses the Wait State mode of operation. By using the Wait State mode, the board can be jumpered to operate at speeds up to 6 MHz.

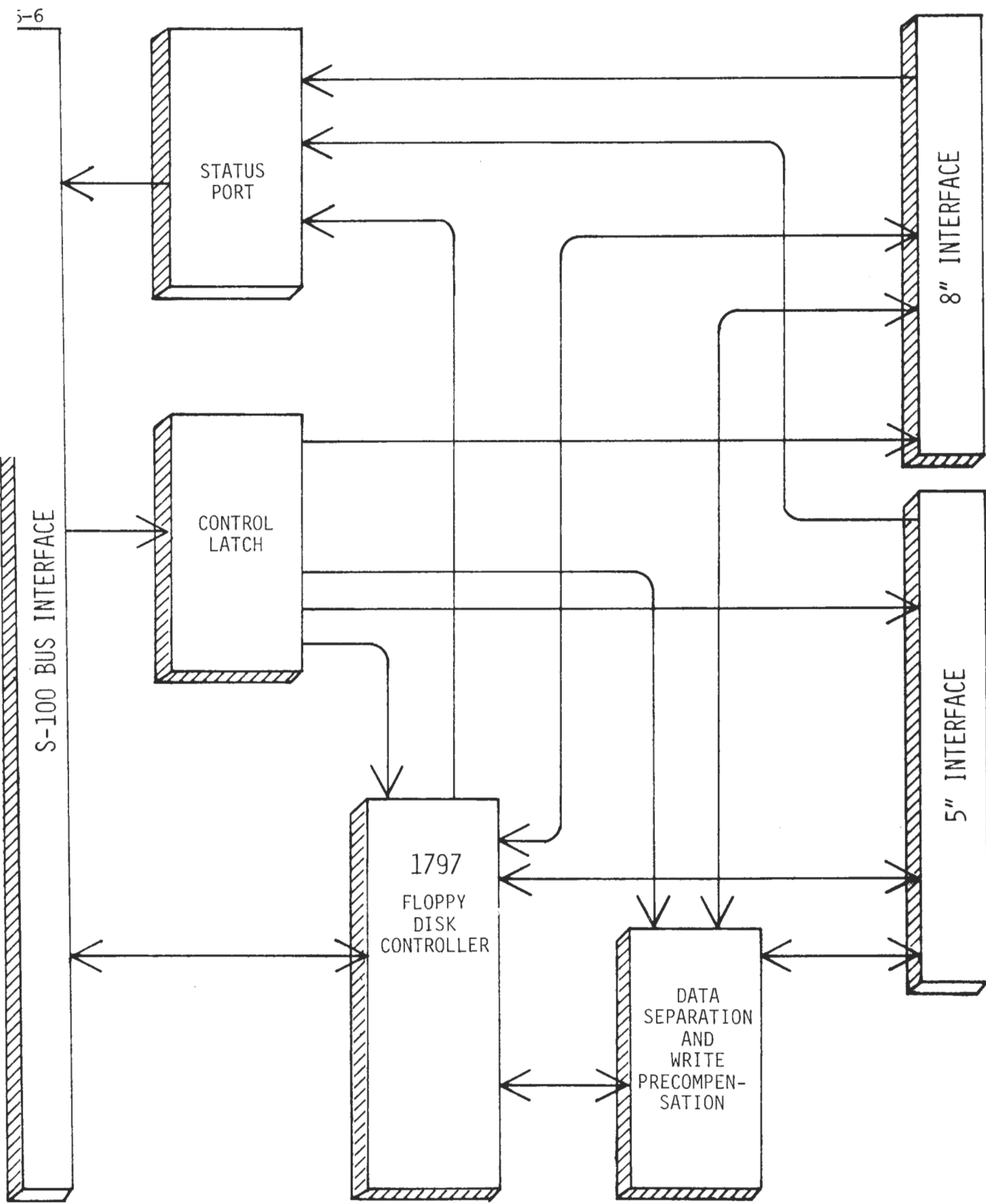
Because the Z-207 is a S-100 compatible card, it can be installed in other makes of computers using the S-100 bus. Additional features that make the controller board acceptable to other computers are: user selectable addressing, software controllable formatting, Shugart compatible 8" interface, and adjustable precompensation.

The information provided in this section of the manual will familiarize you with the operation and troubleshooting of the drive system. Using this information, you will be able to troubleshoot the disk controller board to the component level and determine the condition of the disk drives.



## CIRCUIT DESCRIPTION

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Z-207 BLOCK DIAGRAM

## BLOCK DIAGRAM DESCRIPTION

Refer to the H/Z-207 block diagram as you read the following.

The H/Z-207 Floppy Disk controller board consists of seven major sections: the bus interface, the status port, the control latch, the 1797 floppy disk controller, the data separation & write precompensation circuits, and the two drive interfaces.

The bus interface is made up of two octal bus buffers, an octal tri-state latch, an address comparator, and some miscellaneous enabling circuitry. These components interface the H/Z-207 to the S-100 bus in the H/Z-100.

The status port is a read-only device that tells the CPU the status of the disk drives and the controller. This includes track density, number of recording sides to the disk, and if precompensation is being used.

The control latch accepts commands to the disk drives such as DRIVE SELECT, 5" FASTEP, and others that have to do with the selection and mode of the drives.

The 1797 controller controls the placement of information on the diskette. That is, the movement of the drive head, the formation of written data, and the separation of the read data is controlled by the 1797.

The data separation and write precompensation circuitry control how the data is read to or written from the diskette. It does this by separating the data from the clock signal during read operations and precompensating data during the double-density write operations.

The 8" and 5.25" drive interfaces include buffers and filter circuitry. Up to four drives can be connected to each interface.

## DETAILED CIRCUIT DESCRIPTION

### S-100 BUS INTERFACE

The S-100 Bus Interface is compatible with any IEEE 696-standard S-100 Bus. See the S-100 specification sheets in the appendices of this manual for definitions of the lines.

#### DATA IN

Data in to the bus (out from the controller board) travels through signal lines 91-95 and signal lines 41-43 on the bus interface. These pins are used in read operations from the status latch or from the 1797 controller. The data is buffered from the board's internal data bus to the S-100 bus by means of U36, a 74LS244 buffer.

#### DATA OUT

Data out from the bus (into the controller board) travels through pins 35, 36, 38, 39, 40, 88, 89, and 90 on the bus interface plug. This data is latched by tri-state latch U35. The latch is used because data on the S-100 bus is not present long enough for the 1797 to receive properly. The tri-state latch holds the data on the board's internal data bus so that the 1797 can read it. Valid data is latched in U35 on every write cycle. The latch is enabled through pin 1 when the ALE (Address Latch Enable) signal latches an asserted sOUT (Status Out) signal via U20.

#### ADDRESS LINES

The address lines from the bus enter the board through pins 29, 30, 31, 79, and 80 through 83 of the bus interface. They are buffered by the 74LS244 chip, U34.



### CONTROL LINES

The control lines from the S-100 bus enter the board through pins 24, 25, 45, 46, and 75 through 78 of the bus interface. These lines are buffered by U33.

### VECTOR INTERRUPT LINES

The vector interrupt lines from the bus enter the board at pins 4 through 11 of the bus interface. They may be driven by U32.

### READY LINE

The ready line, RDY, enters through pin 72 of the bus interface. It is driven by U32. The controller board uses this line to put the CPU in a wait state during some operations to give the controller time to finish the operation.

## RESET CIRCUITS

### POWER UP/RESET

On power up, the CPU sends RESET\* through the S-100 bus to the H/Z-207 board. This places the 1797 controller, the control latch, the write precompensation control, and the U26 flip-flops in a known state before the CPU accesses the board.

In the 1797, the reset line sets the command register of 03H, the sector register to 01H, and bit 7 of the status register (Not Ready bit) to logic zero.

After the reset line goes high, the 1797 executes the restore command. The drive read/write head seeks track 0 and sends an interrupt to the computer once the track is found. See the 1797 IC data sheets for more details.

The reset line connects to pin 1 of the control latch, U30, to clear all of the outputs.

The reset state of the phase lock loop control, U1, makes the phase four ( $\phi_4$ ) input equal to 0 (see the 1691 IC data sheets).

Finally, the U26 Q-outputs are made equal to 1; pin 9 sends an RDY (ready) signal to the CPU and pin 5 provides part of the qualification needed for read/write enabling through U27-11.

### POWER-UP WRITE PROTECTION

On power up, the TTL circuits will be at an undefined state until the power supply voltage rises above 4 volts. This could generate a write command in the drives and damage any disks that may be installed.

To protect the disk, the WG (write gate) output from the 1797 is coupled to the 5" and 8" drives through Q3 and Q2. These transistors are biased by R25, D3-D1, and R24 to remain cut off until the power supply voltage is at or above 4 volts. When the supply reaches this value, Q2 and Q3 are biased near their operating region and will conduct whenever WG is asserted.

## CPU/CONTROLLER LOGIC

Reading and writing in the H/Z-207 board involves three types of information: data which can be read or written, status signals, and control signals. Status signals can only be read and control signals can only be written.

### READ STATUS LATCH (U31)

Assume a status signal needs to be read. There are two sources of status information for the S-100 bus, the status port at U31 and the 1797 status register in U22.

To read from the status port, the CPU selects the H/Z-207 by placing the address of the board on the address lines, A0-A7. Lines A3-A7 are checked by the address comparator, U29, for the proper address. The proper address is defined by the user by setting DIP switch DS1. If the address is correct, the EOUT signal pin 19 asserts.

The EOUT signal is gated through U28-13 by I/O at pin 12. I/O asserts on a data transfer between the CPU and an I/O port. If I/O is low, indicating that the sINP signal or sOUT signal is asserted, then the simultaneous assertion of EOUT and I/O signals sends a logic one to U20-2. This logic one is latched onto pin 5 when ALE (address latch enable) asserts. ALE, derived from pSTVAL\* and pSYNC, goes high when the H/Z-207 port address is stable.

The Q output of U20 is Nanded with pDBIN from the S-100 bus to form  $\overline{\text{RDME}}$  at U27-8. This line goes low to indicate that the H/Z-207 board is being read by the CPU, and activates the status latch, U31-1.

The status latch still can not be read until the status port select line (STPS) is asserted at pin 15 of U31. This line comes from U17-14, the I/O address decoder.

The I/O address decoder activates STPS by decoding the address lines A0, A1, and A2. If A0 and A1 are low and A2 is high, and if BDSEL or board select is active, then U17's Y1 line goes low. This causes U31 to place the status word onto the board's internal data bus, where it is buffered by U36 to the S-100 bus.

The organization of the status latch is as follows:

BIT	SIGNAL NAME	FUNCTION	
0	INTRQ	0 = no interrupt request	1 = interrupt request from 1797
1	MOTORON (5")	0 = spindle motor not running	1 = spindle motor running
3	96TP1	0 = 5.25" drives are 48 TPI	1 = 5.25" drives are 96 TP1
4	PRECOMP	0 = 5.25" drives do not need precomp	1 = 5.25" drives need precomp
6	TWOSIDED	0 = 8" diskette not two sided	1 = 8" diskette two sided
7	DRQ	0 = not ready for data transfer	1 = ready for data transfer

#### READ STATUS REGISTER OF 1797 (U22)

Assume now that the 1797's status register is to be read. The procedure is the same as described previously, except that address lines A0, A1, and A2 are low. Because the address bits A0-A2 are different, the I/O address decoder (U17) does not enable the status latch (U31). Instead the status register of the 1797 is selected and read onto the data bus.

## WRITE CONTROL LATCH (U30)

The control latch, U30, is written at the falling edge of CLEN, which is the simultaneous assertion of pWR and the Y0 output of the I/O address decoder. The pWR signal comes directly from the CPU, and the Y0 signal occurs when A0, A1, and A2 are high, low, and high, respectively. The Y0 and pWR signals are ORed at U21-6 to form CLEN.

The organization of each bit in the control latch is as follows:

BIT	SIGNAL NAME	FUNCTION
0,1	DSA, DSB	00 = select drive 1      10 = select drive 3 01 = select drive 2      11 = select drive 4
2	8"/5"	0 = select 5.25"          1 = select 8"
3	DSEN	0 = deselect all drives      1 = select drive specified by bits 0, 1, and 2
4	PRECOMP*	
	5.25" DDEN	0 = precomp all tracks      1 = disable precomp
	8" DDEN	0 = precomp all tracks      1 = precomp tracks 44-76
5	5" FASTEP	0 = 1797 operates as specified by bit 2      1 = 1797 operates in 8" mode
6	WAITEN	0 = wait state enable      1 = wait state enable
7	SDEN	0 = double density          1 = single density

\*(Note: Precomp is disabled in single density.)

When the WAITEN bit in the control latch is asserted, a wait state is initiated on the next read or write of the data register. WAITEN couples through U23, U26, and U32 to the S-100 RDY line. RDY goes low to put the CPU in a wait state until the disk controller asserts DRQ at U22-38.

Upon DRQ becoming active, an additional delay is needed to fulfill the access time requirements of the 1797 Controller. The access delay and synchronization to the S-100 Bus are both accomplished by counting system clocks. An on-board jumper selects whether one system clock is counted (for systems with clocks up to 3 MHz) or two system clocks are counted (for systems with clocks up to 6 MHz). For operation at less than 3 MHz, jumper J1 (near U19) should be jumpered between F and G. For operation between 3 and 6 MHz, this jumper should be between F and E (normal position for the H/Z-100).

At the completion of the access delay, the wait state is cleared. RDY is asserted, and the CPU completes the read or write of the data register in the 1797. A RESET or an INTRQ signal also clears the wait state, so that the CPU does not hang up after an error during a disk access.

#### WRITE COMMAND REGISTER IN THE 1797 (U22)

The command register in the 1797 can be written when A0, A1, and A2 are all low. The FDWR signal at U22-2 is asserted when both FDEN and pWR\* are logic zero. The signal pWR comes directly from the CPU, while FDEN is a composite signal made up of FDSEL and U26-5. The output of U26-5 is the signal that starts the access of the 1797 controller at the end of the wait state.

## DATA READ/WRITE OPERATIONS

During a data write operation, the controller board is enabled by the proper address and by pWR\*. After the proper control words are sent to select the proper drive, address lines A0 and A1 are made high and A2 is made low. This connects the data register of the 1797 to the internal data bus. As long as A0 and A1 are high and A2 and FDWR are low, the data from the S-100 bus will go to the 1797 data register and be shifted out serially on pin 31, the write output line. Also, on pin 31, clock pulses are inserted between each bit.

The track and sector registers in the 1797 determine where the data is to be written to on the disk. Whenever a sector is filled with data, software determines the next sector to be written to by making the A0 and A1 signals equal to 0 and 1, A2 equal to 0. Software then writes the sector number to the sector register and the track number to the track register.

The 1797 translates the track numbers into the proper step and direction commands to the drive.

A read operation requires the board to be enabled as described earlier. However, the I/O address decoder does not enable the status latch because the address provided by the CPU is not correct for a status read from the latch. Instead, the address lines causes the 1797 to dump the bits in its data register onto the internal data bus of the H/Z-207, which connects to the U36 buffer and the S-100 bus.

The 1797 fills its data register from the data shift register, which fills serially from the RAWREAD data stream at U22-27. See "Data Separation and Precompensation" for a discussion on RAWREAD data processing.

## RDY DELAY

U19 is a quad flip-flop that acts as a delay line for the DRQ signal from the 1797 to the S-100 RDY line. The input at U19-4, D1, is output at Q1 after one clock cycle. Q1 is tied to D2 and is output to Q2 after another clock cycle. Q2 is also tied to U25-1 and D3.

From U25-12, the D2 signal presets flip-flop U26. Flip-flop U26 qualifies the FDSEL signal to enable read/write operations in anticipation of the RDY line being made active.

From D3 of U19, the delayed DRQ signal is output to Q3, which is connected to D4 and to jumper J1, post G. Post G is connected to Post F in 3 MHz operations, which do not need additional delay of the DRQ signal. Instead, the output of Q4, which contains the DRQ signal delayed by three to four clock cycles, is connected to jumper J1, post E. For 6 MHz operation, J1 is connected between post E and post F.

## INTERRUPTS

There are two interrupts that the H/Z-207 board can make. They are the interrupt request (INTRQ) and the data request (DRQ). Both of these interrupts originate from the 1797. The INTRQ signal is sent to indicate a command completion or an error. The DRQ signal is sent to indicate data will be accepted in response to a disk read or write command.

The interrupts can be detected two ways, as either a vectored interrupt on any of the bus interface pins from 4 to 11, or as a bit set in the status port, U31, which can then be polled by the CPU.

The INTRQ signal pulls the bus out of a wait state caused by a logic zero at U26-9. When pin 39 of the 1797 asserts, it is inverted at U25-6 to set pin 9 of U26.



## CONTROLLER/DISK-DRIVE LOGIC

### DATA SHAPING

Data pulses to the drive are reshaped by U16, a one-shot multivibrator, to 400 ns. Raw data from the drive are reshaped to 250 ns.

### DATA SEPARATION AND PRECOMPENSATION

Data separation and precompensation are performed primarily by U1, U3, U4, U5, and U22. The data separation circuits are used when the controller is receiving data from the disk drive, while the precompensation circuits are used when the controller is writing data to the disk.

#### Data Separation

$\overline{\text{READDATA}}$  ( $\overline{\text{RDD}}$ ) from the drive couples through U9 and U16 to U1-11 and U22-27 ( $\overline{\text{RAWREAD}}$ ).  $\overline{\text{RDD}}$  contains both data bits and clock bits. U1 extracts the clock bits and sends them to U22-26 as RCLK. These pulses are synchronized with RDD. The 1797 uses the RCLK signal to extract the data bits from the  $\overline{\text{RAWREAD}}$  stream. U22 then formats the data and sends it to the CPU.

U1 uses a phase-locked loop to keep RCLK in phase with the incoming data stream. The phase-locked loop consists of U5, U4, U13, and U1. U5 is a 4-MHz voltage-controlled oscillator that drives U4 and U13. U4 and U13 select either 4 MHz or 2 MHz, depending on the disk size. If a 5-1/4" disk is being read, U4-9 is low. This couples the 2-MHz signal to U1-16. Four megahertz is coupled to U1 for 8" drives.

If the phase of RCLK should drift with respect to the incoming  $\overline{\text{RDD}}$  signal, U1 will send feedback pulses from U1-13 or U1-14 to the VCO at U5. These pulses will increase or lower the VCO frequency. In turn, the VCO frequency will increase or decrease the RCLK frequency until it again in phase with  $\overline{\text{RDD}}$ . Here's how...

If the frequency of  $\overline{\text{RDD}}$  is higher than RCLK, then  $\overline{\text{RDD}}$  will go low at the beginning of RCLK. The pump-up output (PU) at U1-13 will go from a high-impedance state to a logic one. This increases the VCO frequency which increases frequency of RCLK.

If the frequency of  $\overline{RDD}$  is lower than RCLK, then  $\overline{RDD}$  will go low at the end of RCLK. The pump-down output ( $\overline{PD}$ ) responds by going from a high-impedance state to logic zero. This decreases the VCO frequency and thus decreases the frequency of RCLK.

If RCLK and  $\overline{RDD}$  are in phase, then PU and  $\overline{PD}$  are in a high-impedance state and the VCO frequency remains constant.

Pins 5, 7, and 8 of U1 allow the 1797 to control clock separation and data recovery. When pins 7 and 8 are low, the data recovery circuits are enabled. If pin 7 is high, which happens during a write operation, then the data recovery circuits are disabled.

Pin 8, DDEN, controls the frequency of RCLK. When pin 8 is logic one, the frequency of RCLK is equal to the VCO frequency divided by 16. When pin 8 is logic zero, RCLK is equal to the VCO frequency divided by 8.

#### Data Precompensation

Precompensation, used for 80-track double-density disk write operations, places data properly on the disk so that it can be read back with minimum error. Error is introduced by the shifting of old data that is adjacent to new data being written. This shifting is due to the nature of the magnetic fields on the disk (like fields repel).

The precompensation circuits consist of U22, U1, and U3. U22 sends the write data from pin 31 to U1-1. U3 provides delay timing for the write data in U1. U22 selects the amount of precompensation by setting the logic levels on pin 18 (LATE) and pin 17 (EARLY).

Here's what happens...

When the 1797 sends a data bit to U1-1, the strobe line at U1-5 latches high. This triggers U3-11 and causes a negative-going pulse to ripple through  $\overline{\Phi 1}$ ,  $\overline{\Phi 2}$ ,  $\overline{\Phi 3}$ , and  $\overline{\Phi 4}$ . R3 sets the pulse width of these signals and, therefore, the amount of precompensation.

With no precompensation (EARLY = LATE = 0), the data pulse is coupled to U1-6 at  $\overline{\Phi 2}$  time. If LATE precompensation is selected, the data bit leaves U1-6 at  $\overline{\Phi 3}$  time. EARLY precompensation synchronizes the data bit to  $\overline{\Phi 1}$ .

When  $\overline{\Phi 4}$  pulses low, it couples through U7 to U1-19 to clear the strobe at U1-5 in anticipation of the next write data pulse.

Precompensation must be enabled for double-density operation. The CPU does this by setting U30-19 to logic one and sending it to the DDEN input at U1-15. The CPU also asserts the  $\overline{\text{PRECOMP}}$  line at U30-12. This couples through U6-8 to TG43 at U1-9. TG43 must be high before precompensation can take place.

Even if  $\overline{\text{PRECOMP}}$  isn't asserted, the write data should be precompensated on the inner tracks, where the data is packed closer together. This condition is taken care of by U22-29, which asserts on tracks greater than 43. The TG43 signal couples through U6-8 to the TG43 input of U1.

#### HEAD LOAD TIMING

The single-shot at U15 provides read/write head-load timing. When the 1797 sends a head-load command, pin 28 goes high to load the drive head and to trigger U15.

U15-7 goes low for about 50 mS. This signal couples to U22-23 to prevent a data read or write until U15 times out. This delay compensates for bounce when the read/write head contacts the disk surface.

### 1797 TIMING

U18, U12, U14, and U30 provide timing and control of timing to the 1797. Depending on the state of U14, the clock frequency to U22-24 will be either 1 MHz or 2 MHz.

The operating frequency of the 1797 is automatically switched from 1 MHz to 2 MHz when changing from 5-1/4" drives to 8" drives. This is done by U30-6 and is coupled through U7-11 to the latch at U14.

One drawback of the 1797 is that it won't allow 5-1/4" drives to step at a 3-mS rate during track seek. To circumvent this problem, U30-15 sets the 5" FASTSTEP signal. This signal couples through U7-12 to U14. U14 increases the operating frequency to 2 MHz to speed up the step rate. At the end of the track-seek function, the clock frequency is reduced to 1 MHz again for normal 5-1/4" operation.

### 8" DRIVE INTERFACE

The 8" drive interface is through P1. All output signals to the drives are buffered through U8 and U10 except WG and HLD. The WG signal is sent through transistor Q2, as described previously. The HLD signal is inverted by U7-10 before being transmitted to the drives.

All input signals except READY and TWOSIDED are buffered through the upper section of U9 when enabled by a high on the 8"/5" line. The READY signal is inverted at U6-6, while the TWOSIDED signal is inverted at U6-11.

### 5" DRIVE INTERFACE

The 5" drive interface is through P2. All output signals to the drives are buffered through U10 and U11 except WG and MOTOR. The WG signal is sent through transistor Q3, as described previously. The MOTOR signal turns on the disk drive motor whenever a logic zero is present at pins 9, 10, 12, and 13 of U23. The single-shot at U15 keeps the drive motor on for about 20 seconds after the disk access is complete. This provides a proper turn-off delay.

All input signals are buffered through the lower section of U9, which is enabled by a low on the 8"/5" line.

## Z-207 FLOPPY DISK CONTROLLER BOARD DEFINITIONS

A0-A7	Address bits.
ALE	Address latch enable. Data and address lines from the CPU have valid information.
BDSEL	Board Select. The Z-207 board is selected (enabled).
CLK	Clock signal.
CS	Chip select. When asserted, the 1797 chip is enabled.
D0-D7	Data bits on the Z-207 board's internal data bus.
DDEN	Double density enable.
D10-D17	Data-in bits on the S-100 bus ("in" with respect to the CPU, not the Controller).
DIR	Direction of drive head. When high, the drive head is stepping in. When low, the drive head is stepping out.
D00-D07	Data-out bits on the S-100 bus ("out" with respect to the CPU, not the Controller).
DRQ	Data request. The 1797 data register needs data for write operations or the register has data for read operations.
DSA	Drive select A. Used with DSB to address the drives.
DSB	Drive select B. Used with DSA to address the drives.
EARLY	Write data bit early to disk drive (used for precompensation).
HLD	Head load.

HLT	Head load timing. The drive head is engaged when this signal is high.
INDEX	The index hole on the diskette has been detected.
INTRQ	Interrupt request. Z-207 board has input for the CPU.
LATE	Write data bit late for drive precompensation.
MR	Master reset pin on the 1797 Controller chip that sets all registers in the chip to a known state.
pSTAVAl*	Status valid.
pSYNC	New bus cycle may begin.
PD	Pump down. Decreases the frequency of the raw read data tracking clock.
PRECOMP	Enables precompensation when low.
PU	Pump up. Increases frequency of the raw read data tracking clock.
pWR	Valid data is on data-out bus (write bus).
RAW READ	Unprocessed data from the drive.
RCLK	Clock that separates data from drive data and clock stream.
RDD	Data and clock stream from the drive.
RDME	Data or status signals input for the bus are enabled.
RDY	Slave board is ready. (Z-207 board is a slave board.)
RE	Read enable. Enables the 1797 chip for read operations when low.
READY	The 8" disk drive is ready.

RESET	Reset signal.
SIDE1	Otherwise known as side select output. When high, side 1 is selected in the drive. When low, side 0 is selected.
sINP	Status signal signifying data input to the bus (read cycle) may occur.
sOUT	Status signal signifying data output from the bus (write cycle) may occur.
STEP	Steps the drive head one step per pulse.
STB	Strobe output from the 1691 (U1) phase lock loop control.
TG43	Track greater than 43. The drive read/write head is over or past track 43 (track of mandatory precompensation in double density 8" drive).
TKØ	Track 0. The drive read/write head is over track 0 on the diskette.
TWOSIDED	The 8" drive is set for two-sided operation with a two-sided diskette.
VFOE/WF	VFO enable/write fault. This input is used in conjunction with the WG signal to enable the data recovery circuit. When WG is high, a write operation is taking place and the data recovery circuits are disabled.
V1Ø*-V17*	Vector interrupts.
WAIT	RDY line is low (not ready).
WAITEN	Wait enable. Set RDY line low on all accesses of the 1797 data register.
WD	Write data. Contains the data to be written onto the diskettes as well as the clock signals.
WDIN	Write data into the 1691 phase lock loop control.

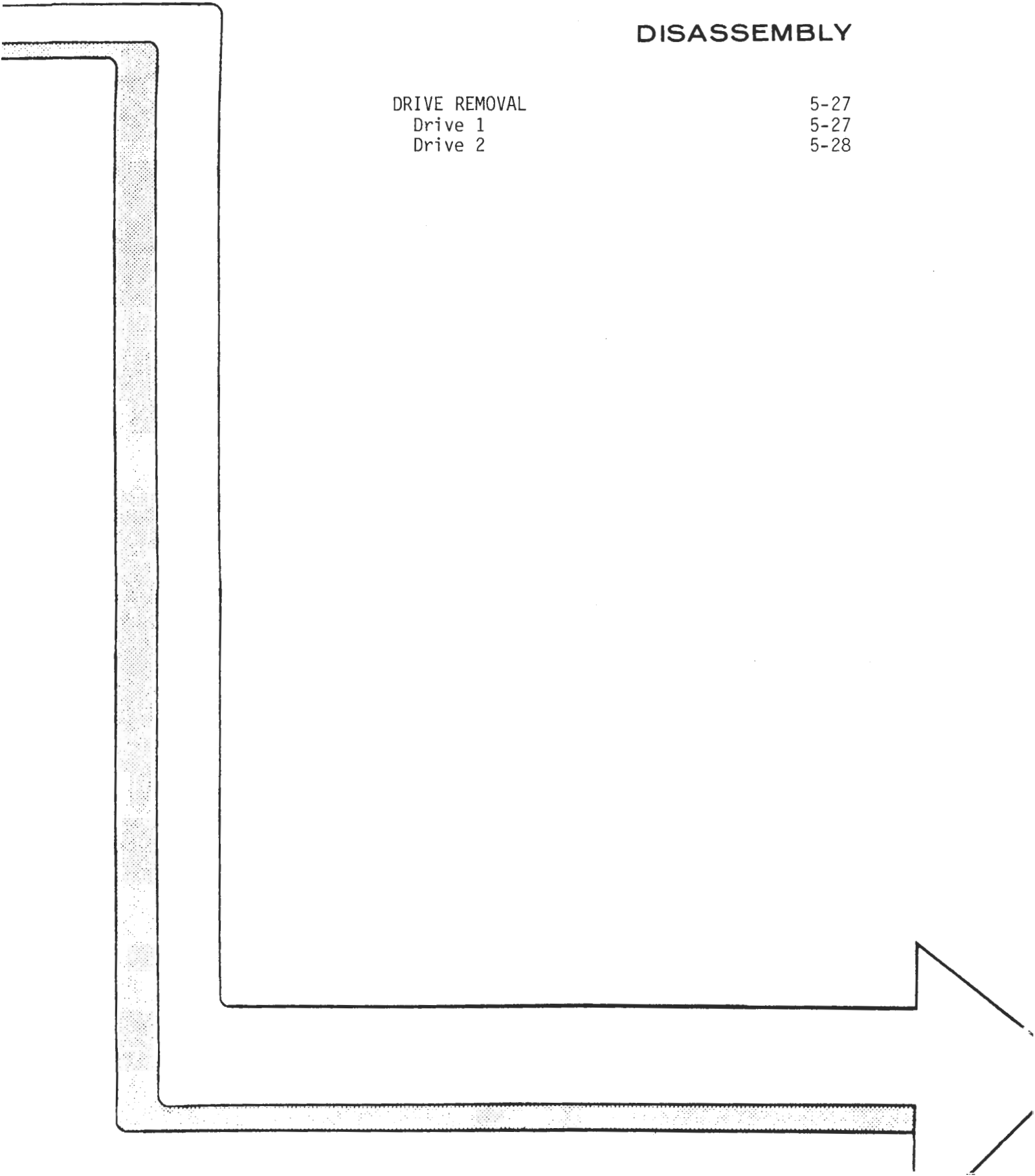
WDOUT	Write data out of the 1691 phase lock loop and precompensation controller.
WG	Write gate. Output to the disk drive is valid.
WE	Write enable. Enables the 1797 floppy disk controller chip for write operations.
WPRT	Write protect. When this signal is received, no write command can take place and write protect bit in the status register is set.
WRDATA	Precompensated write data pulses that have been reshaped by U16.
5DS0-5DS3	Five inch drive select signals.
5"FASTEP	Enables fast stepping in the 5.25" drives.
8"/5"	Selects between the 8" and the 5.25" drives.
8DS0-8DS3	Eight-inch drive select signals.
CLOCK	Master clock signal.
Φ1-Φ4	Precompensation phase signals.



# DISASSEMBLY

DRIVE REMOVAL  
Drive 1  
Drive 2

5-27  
5-27  
5-28

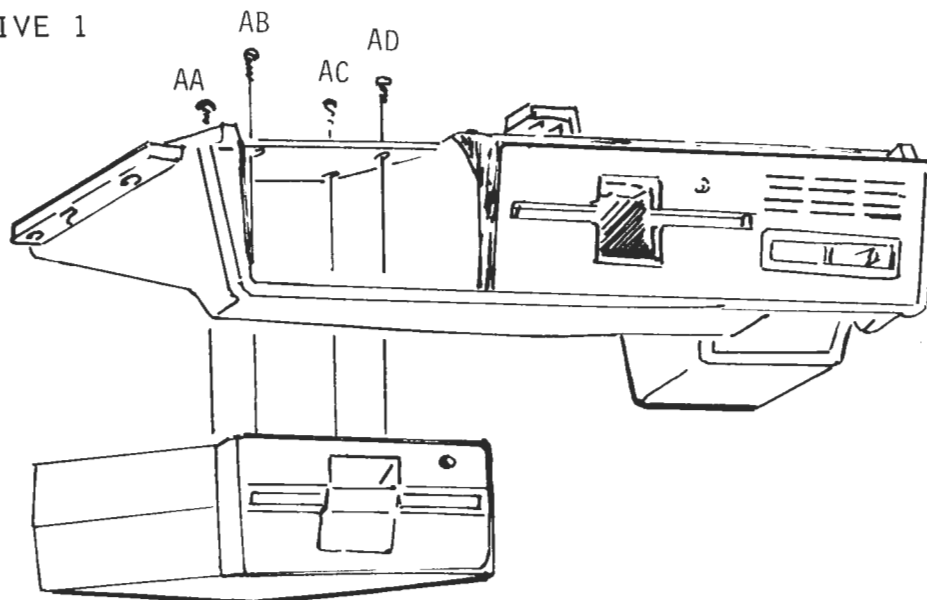




## DRIVE REMOVAL

Follow the appropriate procedure to remove either drive 1, drive 2, or both drives from the H/Z-100 Low-Profile computer.

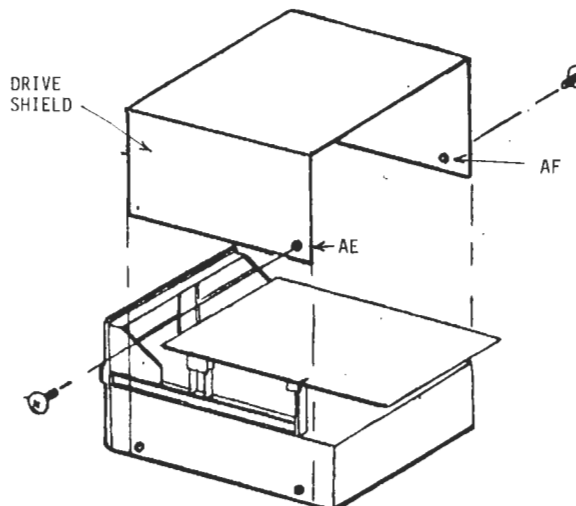
### DRIVE 1



- Place the disk drive assembly upside down and remove the four 6-32 x 5/8" hex-head screws from AA, AB, AC, and AD.
- Carefully lift the drive shelf off the drive and set it aside.

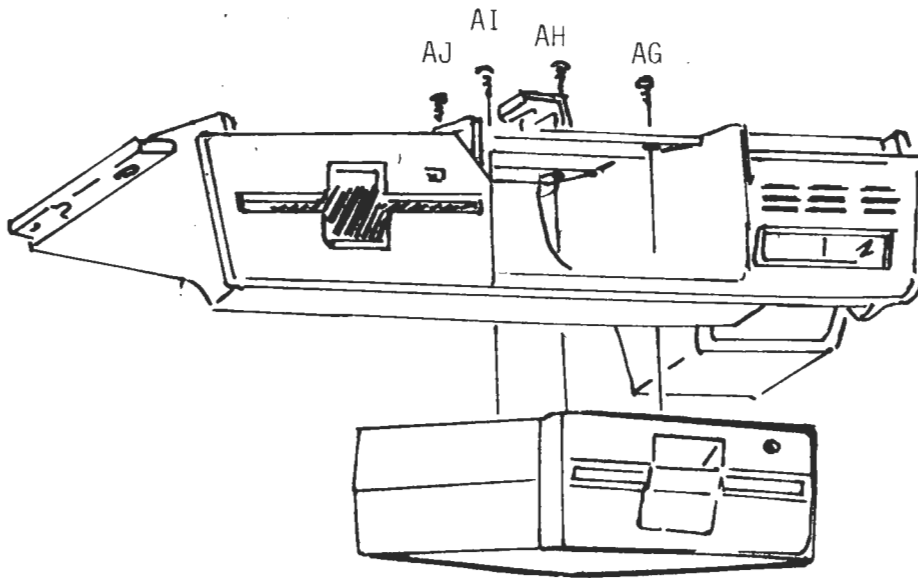
- Turn the drive right-side-up and remove the two 6-32 x 1/4" flat-head screws from AE and AF.

- Lift the drive shield from the drive.



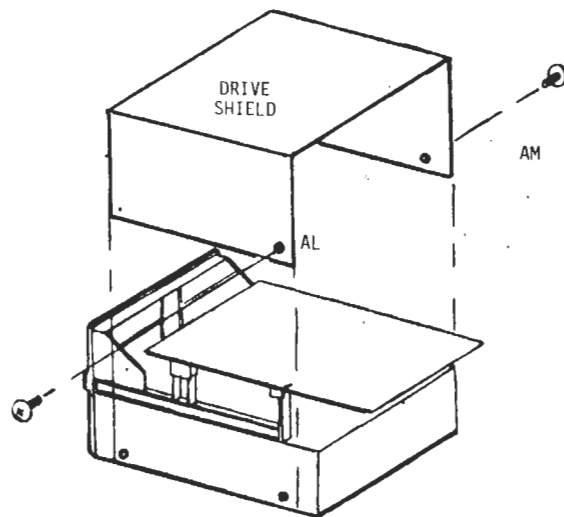
This completes Drive 1 Removal. Reverse the procedure to reinstall the drive in the drive shelf.

## DRIVE 2



- Place the disk drive assembly upside down and remove the four 6-32 x 5/8" hex-head screws from AG, AH, AI, and AJ.
- Carefully lift the drive shelf off the drive and set it aside.

- Turn the drive right-side-up and remove the two 6-32 x 1/4" flat-head screws from AK and AL.
- Lift the drive shield from the drive.



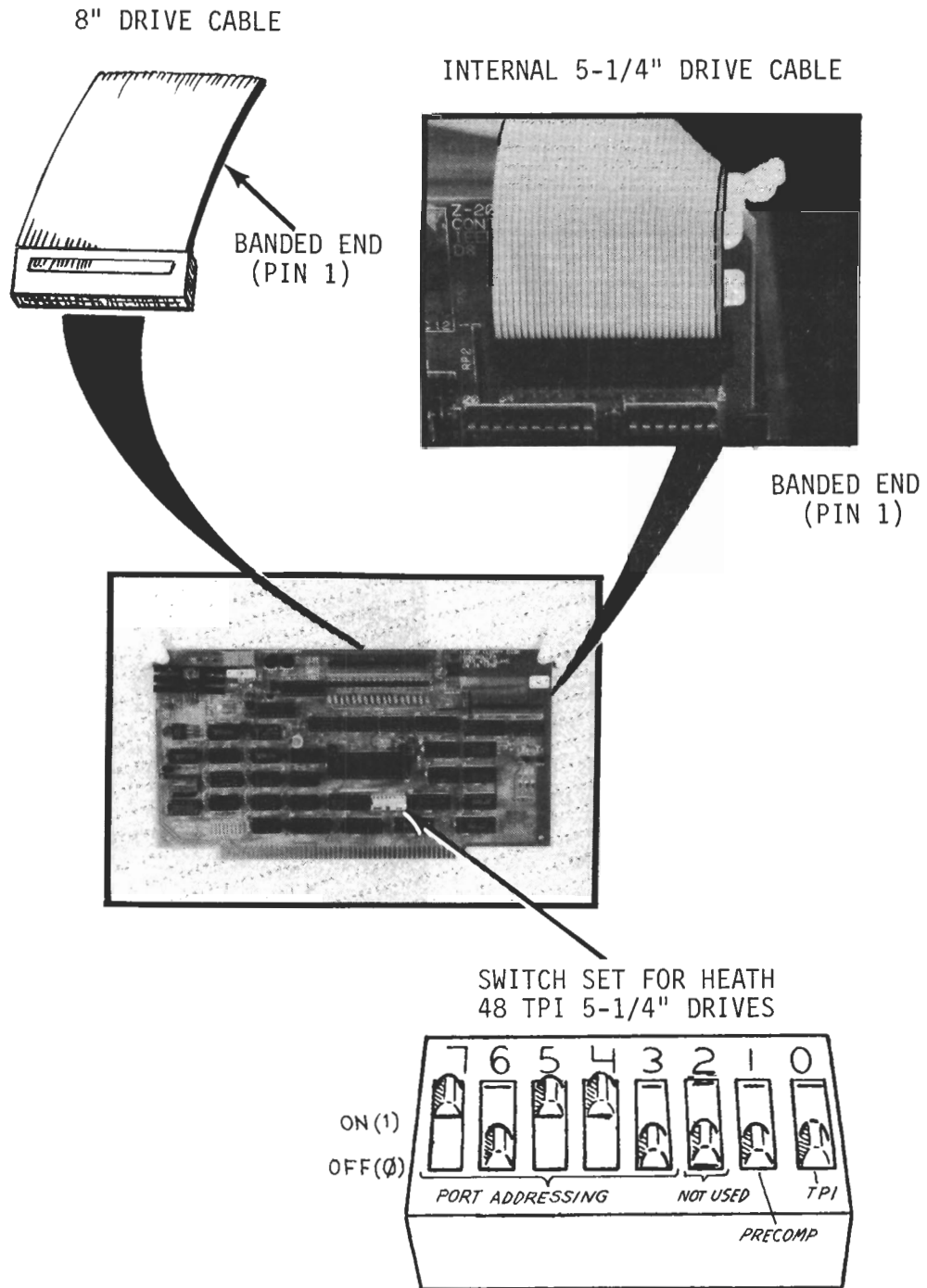
This completes Drive 2 Removal. Reverse the procedure to reinstall the drive in the drive shelf.

## VISUAL CHECKS

DISK CONTROLLER BOARD CABLE CONNECTIONS AND SWITCH POSITIONS	5-31
DISK CONTROLLER BOARD 5 1/4" DISK DRIVE CONNECTIONS	5-32
COMPONENT LOCATIONS AND VALUES	5-33



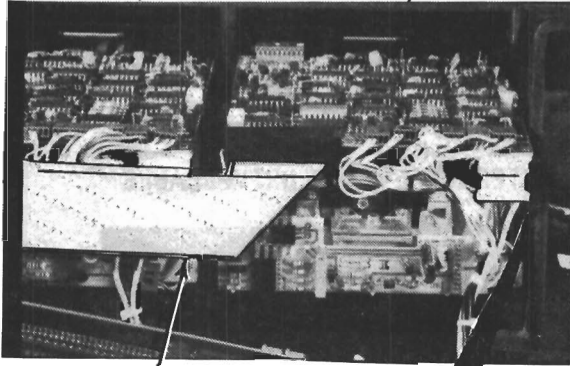
# DISK CONTROLLER BOARD CABLE CONNECTIONS AND SWITCH POSITIONS



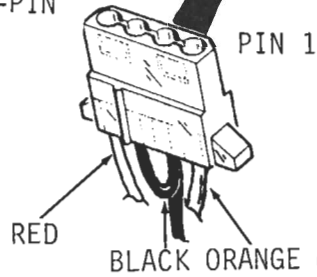
# DISK CONTROLLER BOARD 5-1/4" DISK DRIVE CONNECTIONS

LOW PROFILE COMPUTER (SHOWN WITH DRIVE SHIELDS REMOVED)

(Viewed from Rear)

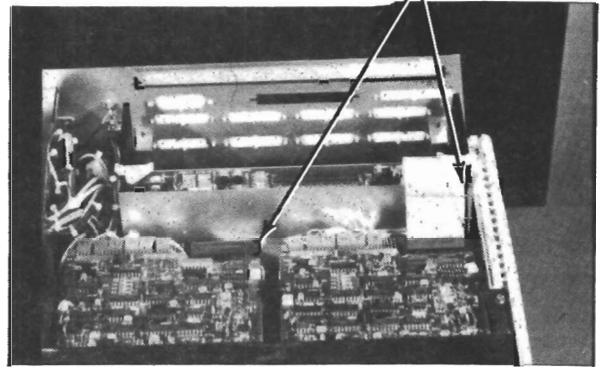


BANDED END OF 34-PIN CONNECTOR



PIN 1

BANDED END OF 34-PIN CONNECTOR



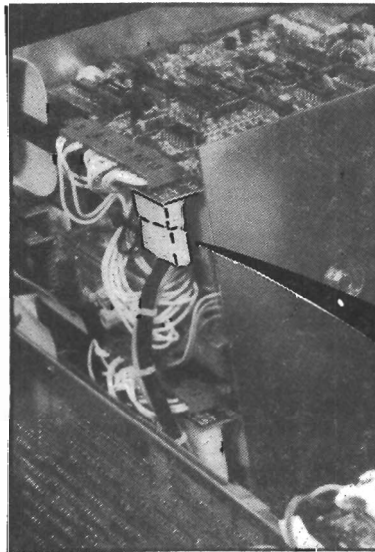
(Viewed from Top)

## ALL-IN-ONE COMPUTER

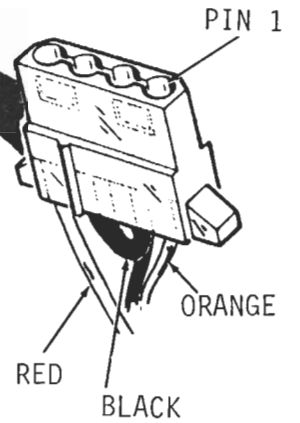
BANDED END OF 34-PIN CONNECTOR



(Viewed from Right Side)



(Viewed from Left Top)



PIN 1

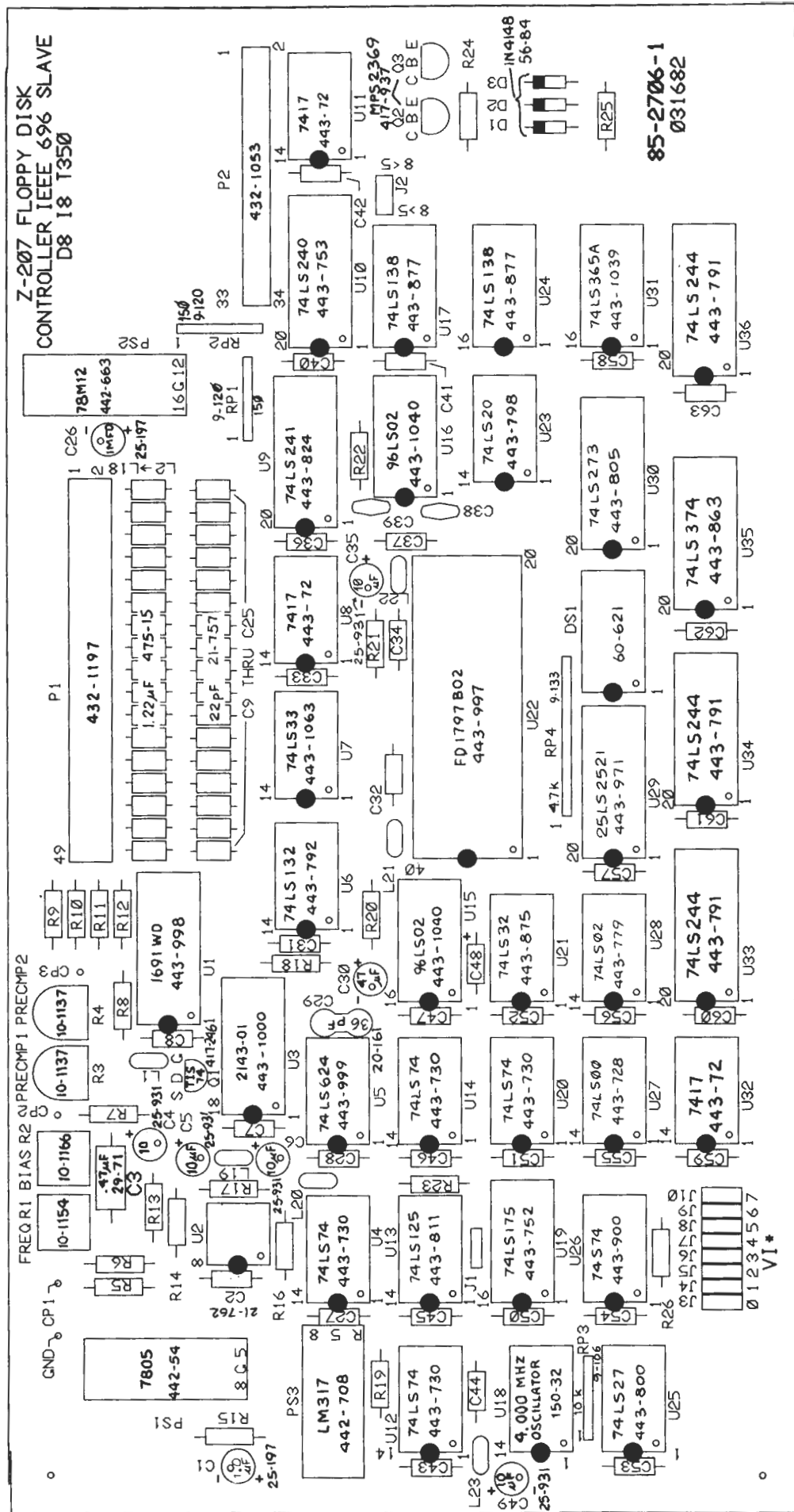
RED

BLACK

ORANGE



COMPONENT LOCATIONS AND VALUES



Z-207 FLOPPY DISK  
CONTROLLER IEEE 696 SLAVE  
D8 18 T350

85-2706-1  
031682

DISK CONTROLLER CIRCUIT BOARD (HE-181-3763-1)



## ADJUSTMENTS

INTRODUCTION	5-37
EQUIPMENT NEEDED	5-37
DATA SEPARATOR ADJUSTMENT	5-37



## INTRODUCTION

In this section of the manual, instructions will be given on how to calibrate the Z-207 Disk Controller Board. By following the procedure below, adjustment of the VCO bias voltage and VCO center frequency are performed.

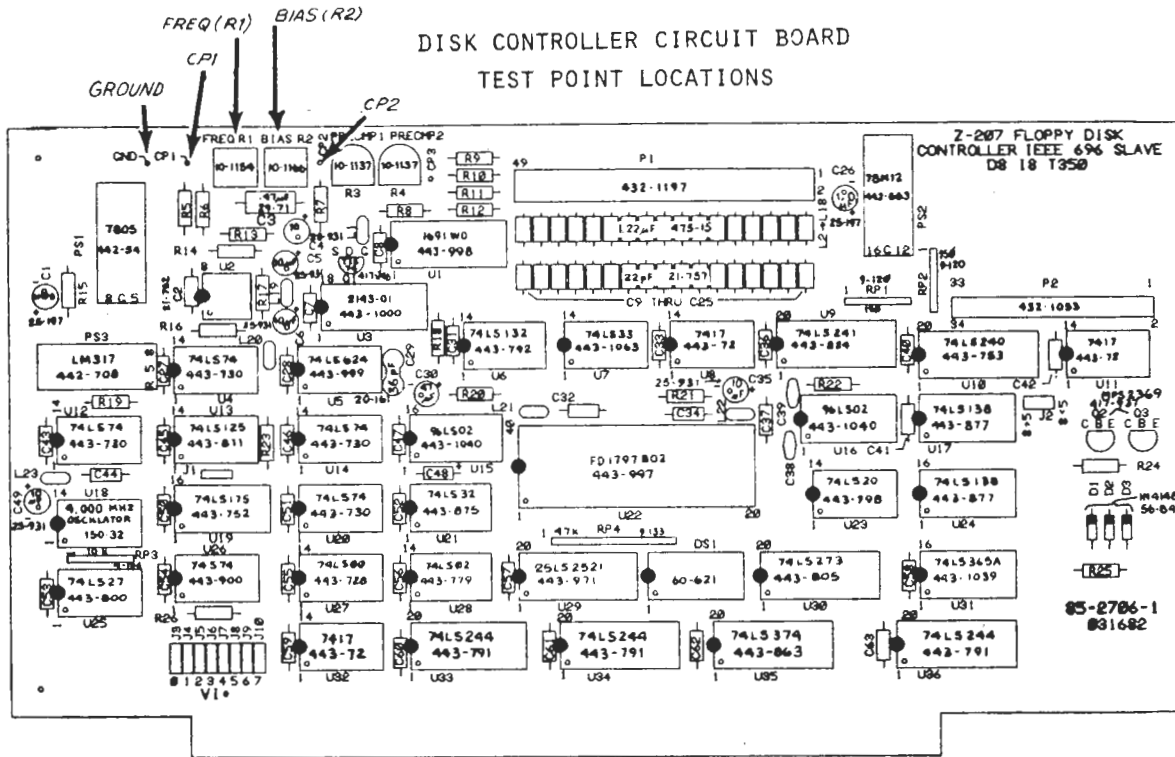
## EQUIPMENT NEEDED

<u>Frequency Counter</u>	IM-2420 or equivalent.
<u>Low Capacitance Probe</u>	PKW-105 or equivalent.
<u>Multimeter</u>	IM-2202 or equivalent.

## DATA SEPARATOR ADJUSTMENT

Perform the following steps to adjust the data separator.

- Allow a fifteen minute warm-up of the board with the top cover of the computer in place.
- Remove the top cover of the computer.



Refer to the illustration above for the location of the test points.

-- Connect the common test lead of the multimeter to the GND test point.

-- Connect the positive test lead to the CP2 test point.

-- Adjust the BIAS control (R2) until the multimeter display shows +1.40 VDC. You will want to switch the multimeter to lower ranges to perform this adjustment accurately. A reading of +1.40 VDC (+.05 volts) will result in proper operation.

-- Disconnect the multimeter.

-- Connect the common lead of the frequency counter to the GND test point.

-- Connect the test probe of the frequency counter to the CP1 test point.

-- Adjust the FREQ control (R1) until the frequency counter display shows 4.000 MHz.

-- Disconnect the frequency counter.

The adjustments to the Data Separator are now complete.

## TROUBLESHOOTING

INTRODUCTION	5-41
SETUP	5-42
CHECKOUT PROCEDURE	5-43
Z-207 DISK CONTROLLER TEST	5-44





## INTRODUCTION

The following procedure tests the ability of the Z-207 controller board to boot a 5-1/4" disk. Refer to the schematic for general logic states for troubleshooting the 8" portion of the board.

If there's a disk problem that only shows up after the disk is booted, you will need to use diagnostic programs. Check the Diagnostics section of this Manual for more comprehensive disk tests. As diagnostic programs become available, we will publish them for inclusion in the Diagnostics section of this manual. Also, if you develop any troubleshooting techniques or diagnostic programs that you'd like to share, send it to:

Heath Company  
Service Publications and Training  
Dept. 741  
Benton Harbor, Mi. 49022

We will evaluate your submission and, when approved, publish it for inclusion in the Service Bulletins or Diagnostics sections of this manual. Be sure to include a complete description of the troubleshooting technique, symptoms caused by the failed component, and any special equipment needed to repair the problem. If submitting a diagnostic program, we will need a copy of the source listing; preferably on disk.

## SETUP

- Remove the disk controller board from a known-good H/Z-100 and install the H/Z-207 board to be tested into the H/Z-100.
- Connect at least one 48 TPI, 5-1/4" disk drive to P1.
- Refer to the configuration section and configure the system to 48 TPI, 5-1/4" soft-sector disk for the primary boot device. Set the configuration to defeat the auto-boot option.
- Turn on the computer.

As you make the following measurements, press the (B)oot key and press RETURN. Logic states located inside parenthesis indicate that the probe pulses one or more times while "Read Completed" is being printed onto the screen. In the case of a (P) indication, the pulse rate (as indicated by the logic probe) will momentarily change during the "Read Completed" interval.

The schematic shows the logic states after a CTRL/RESET has been performed. Refer to these logic states for troubleshooting areas not covered in the following charts.

## CHECKOUT PROCEDURE

In the following tests, you need only test the ICs in the left column indicated by an asterisk (\*). If you don't get the suggested logic state, then check each IC listed immediately to the right. The logic states for these ICs are listed in the left column below the ICs with the asterisks.

Continue tracing backwards using this procedure until you test an IC that matches the suggested logic state. The previous IC that you tested is likely the bad IC.

Before you replace the suspected IC, check the other lines leading up to it. You must do this because this checkout procedure gives only the most likely causes to the problem. It doesn't cover such things as open ground foils, foil runs shorted together, open resistors, or missing power supplies.

To help you locate the IC on the schematic, the schematic number is shown in parenthesis to the right of the IC under test.

Unless instructed otherwise, perform these tests with the H/Z-100 configured for 5-1/4" drives (primary) and with auto-boot defeated. See the Configuration section. Also, unless noted otherwise, all logic states are those present after a hard reset.

## Z-207 DISK CONTROLLER TEST

CHECK	IF NOT OKAY, CHECK
*Q3 Collector = Z	U21-8
*U1-16 = 2 MHz	U13-6
*U7-4 = L	U7-5 (Also press and release CTRL/RESET. U7-4 should remain low for about 18 seconds. If not, then replace U15.)
*U9-19 = L	U30 or the data bus is defective.
*U10-12 = H	U10 or U22 is defective.
*U10-14 = H	U10 or U22 is defective.
*U10-16 = H	U10 or U22 is defective.
*U11-4 = H	U11-3
*U11-6 = H	U11-5
*U11-8 = H	U11-9
*U11-10 = L	U11-11
*U11-12 = H	U11-13
*U22-2 = (H)	U21-11
*U22-3 = (H)	U21-3
*U22-23 = (H)	U15-7
*U22-24 = 1 MHz	U13-8
*U22-27 = P	U16-9
*U22-34 = L	U9 is defective.
*U22-35 = L	U9 is defective.
*U22-36 = H	U9 is defective.
*U31-1 = (H)	U27-8
*U31-15 = (H)	U17-14
*U32-6 = (H)	U32-5
*U35-11 = (P)	U28-4
*U36-1 = (H)	U27-8
*U36-19 = (H)	U27-8

End of test.

---

U4-3 = 4 MHz	U5-8
U4-5 = 2 MHz	U4-3
U4-9 = L	U4-11, U4-12
U4-11 = P	U4-5
U4-12 = L	U30 or the data bus is defective.
U5-8 = 4 MHz	U5 or U1 defective; R1 or R2 incorrectly adjusted.
U7-5 = H	U23-8
U7-11 = L	U30 or the data bus is defective.
U7-12 = L	U30 or the data bus is defective.
U7-13 = H	U7-11, U7-12
U10-3 = L	U10-17
U10-17 = H	U33-9
U11-3 = H	U16-7
U11-5 = H	U24-14
U11-9 = H	U24-12
U11-11 = L	U24-15
U11-13 = H	U24-13
U12-3 = 4 MHz	U18 is bad.
U12-5 = 2 MHz	U12-3
U12-9 = 1 MHz	U12-11
U12-11 = 2 MHz	U12-5
U13-4 = L	U4-9
U13-5 = 2 MHz	U4-5
U13-6 = 2 MHz	U13-4, U13-5
U13-8 = 1 MHz	U13-9, U13-10
U13-9 = 1 MHz	U12-9
U13-10 = L	U14-8
U14-8 = L	U14-11, U14-12
U14-11 = 1 MHz	U12-9
U14-12 = H	U7-13
U15-4 = H	U22 or the data bus is defective.
U15-7 = (H)	U15-4
U16-4 = L	U1 or U22 is defective.
U16-7 = H	U16-4
U16-9 = P	U16-11
U16-11 = P	U9 is defective.

U17-1 = P	U34-18
U17-2 = P	U34-16
U17-4 = (H)	U20-6
U17-6 = P	U34-14
U17-7 = L	U19-1
U17-14 = (H)	U17-1, U17-2, U17-4, U17-6
U17-15 = (H)	U17-1, U17-2, U17-4, U17-6
U19-1 = (L)	U26-8
U19-14 = L	U19-1
U20-1 = (L)	U28-13
U20-2 = (L)	U28-13
U20-3 = P	U27-6
U20-5 = (L)	U20-1, U20-2, U20-3
U20-6 = (H)	U20-1, U20-2, U20-3
U21-1 = (H)	U27-11
U21-2 = (H)	U27-8
U21-3 = (H)	U21-1, U21-2
U21-4 = (H)	U17-15
U21-5 = (P)	U33-12
U21-6 = (H)	U21-4, U21-5
U21-8 = L	U21-10
U21-10 = L	U22 of data bus is defective.
U21-11 = (H)	U21-12, U21-13
U21-12 = (H)	U27-11
U21-13 = (P)	U33-12
U22-39 = (L)	Check the data bus at pins 7 through 14. These lines pulse from a high impedance state while "Read Completed" is being printed. If not, then check the components along the data bus.
U23-2 = (L)	U30-16
U23-4 = P	U34-18
U23-5 = P	U34-16
U23-6 = (H)	U23-2, U23-4, U23-5
U23-8 = H	U23-13
U23-13 = L	U24-15

U24-1 = L	U30 or the data bus is defective.
U24-2 = L	U30 or the data bus is defective.
U24-3 = L	U30 or the data bus is defective.
U24-6 = H	U30 or the data bus is defective.
U24-12 = H	U24-1, U24-2, U24-3, U24-6
U24-13 = H	U24-1, U24-2, U24-3, U24-6
U24-14 = H	U24-1, U24-2, U24-3, U24-6
U24-15 = L	U24-1, U24-2, U24-3, U24-6
U25-1 = L	U19-7
U25-2 = L	U10-3
U25-3 = L	U10-3
U25-4 = (L)	U22-39
U25-5 = L	U19-14
U25-6 = (H)	U25-3, U25-4, U25-5
U25-12 = (H)	U25-1, U25-2, U25-13
U25-13 = (L)	U22-39
U26-2 = (H)	U23-6
U26-3 = (L)	U20-5
U26-4 = (H)	U25-12
U26-5 = (H)	U26-2, U26-3, U26-4
U26-8 = (L)	U26-10, U26-11, U26-12
U26-10 = (H)	U25-6
U26-11 = (L)	U20-5
U26-12 = (H)	U23-6
U27-1 = (L)	U22-39
U27-3 = (H)	U27-1
U27-4 = P	U33 defective.
U27-5 = P	U33 defective.
U27-6 = P	U27-5, U27-4
U27-8 = (H)	U27-9, U27-10
U27-9 = P	U33 defective.
U27-10 = (L)	U20-5
U27-11 = (H)	U27-12, U27-13
U27-12 = (L)	U28-10
U27-13 = (H)	U26-5
U28-1 = (H)	U28-2, U28-3
U28-2 = (L)	U33 defective.
U28-3 = (L)	U33 defective.
U28-4 = (P)	U28-6

U28-6 = (P)  
U28-8 = (H)  
U28-9 = P  
U28-10 = (L)  
U28-11 = (P)  
U28-12 = (H)  
U28-13 = (L)

U29-19 = (P)

U30-1 = H  
U30-11 = (H)  
U30-16 = (L)

U32-5 = (H)

U33-9 = H  
U33-12 = (P)

U34-14 = P  
U34-16 = P  
U34-16 = P  
U34-18 = P

U33-12  
U20-6  
U34-14  
U28-8, U28-9  
U29-19  
U28-1  
U28-11, U28-12

U29, U34, or DS1 defective.

U33-9  
U21-6  
U30-1, U30-11, or data bus  
problem.

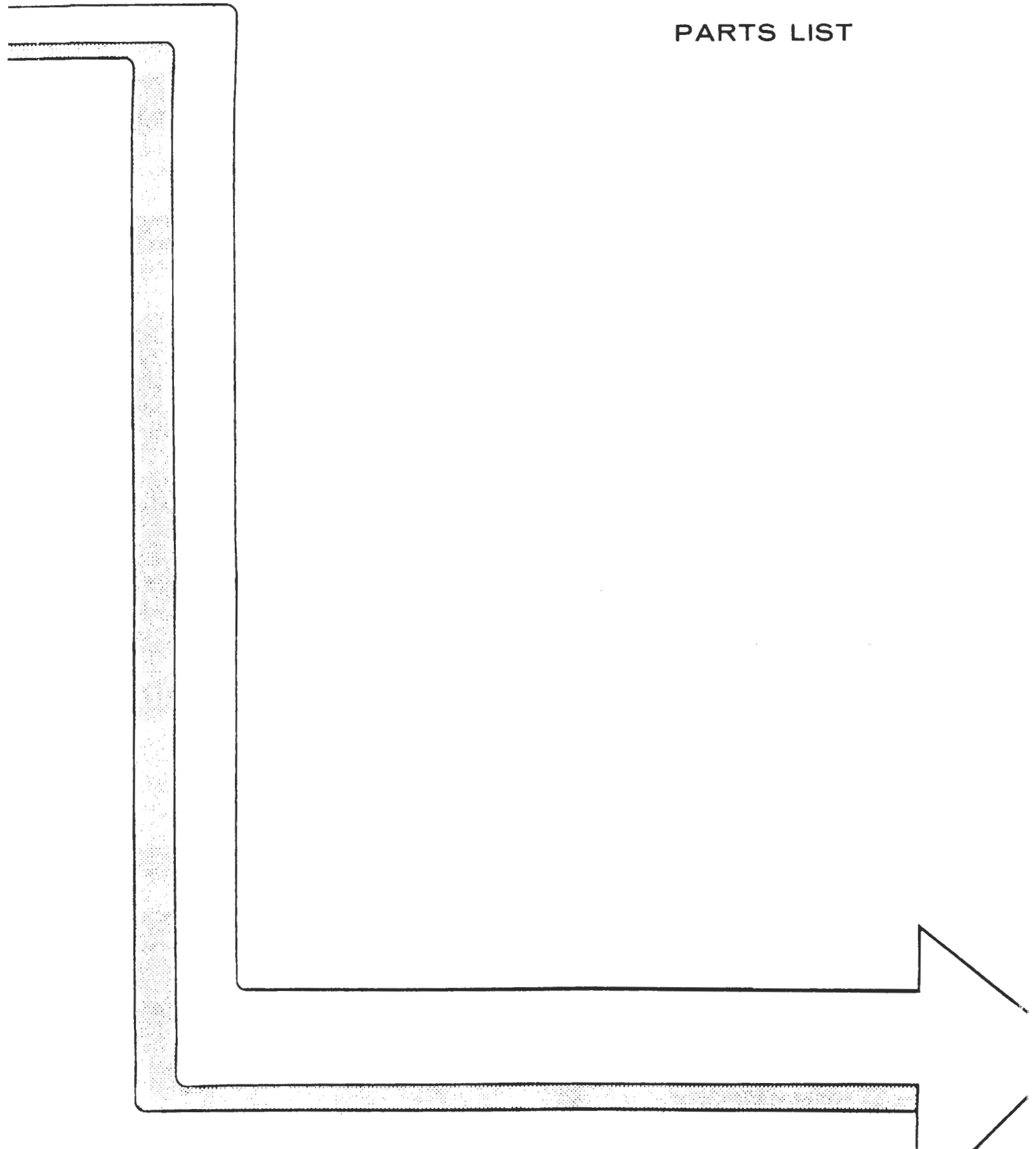
U27-3

U33 defective.  
U33 defective.

U34 defective.  
U34 defective.  
U34 defective.  
U34 defective.



PARTS LIST





# PARTS LIST

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.	CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
<b>DISK CONTROLLER BOARD PART LIST (Assembled HE 181-3763-1)</b>					
<b>CAPACITORS</b>					
C1	1.0 uF tantalum	HE 25-197	C40	.1 uF ceramic	HE 21-762
C2	none		C41	.1 uF ceramic	HE 21-762
C3	.47 uF polycarbonate	HE 29-71	C42	.1 uF ceramic	HE 21-762
C4	10 uF electrolytic	HE 25-931	C43	.1 uF ceramic	HE 21-762
C5	10 uF electrolytic	HE 25-931	C44	.1 uF ceramic	HE 21-762
C6	10 uF electrolytic	HE 25-931	C45	.1 uF ceramic	HE 21-762
C7	.1 uF ceramic	HE 21-762	C46	.1 uF ceramic	HE 21-762
C8	.1 uF ceramic	HE 21-762	C47	.1 uF ceramic	HE 21-762
C9	22 pF ceramic	HE 21-757	C48	1.0 uF tantalum	HE 25-197
C10	22 pF ceramic	HE 21-757	C49	10 uF electrolytic	HE 25-931
C11	22 pF ceramic	HE 21-757	C50	.1 uF ceramic	HE 21-762
C12	22 pF ceramic	HE 21-757	C51	.1 uF ceramic	HE 21-762
C13	22 pF ceramic	HE 21-757	C52	.1 uF ceramic	HE 21-762
C14	22 pF ceramic	HE 21-757	C53	.1 uF ceramic	HE 21-762
C15	22 pF ceramic	HE 21-757	C54	.1 uF ceramic	HE 21-762
C16	22 pF ceramic	HE 21-757	C55	.1 uF ceramic	HE 21-762
C17	22 pF ceramic	HE 21-757	C56	.1 uF ceramic	HE 21-762
C18	22 pF ceramic	HE 21-757	C57	.1 uF ceramic	HE 21-762
C19	22 pF ceramic	HE 21-757	C58	.1 uF ceramic	HE 21-762
C20	22 pF ceramic	HE 21-757	C59	.1 uF ceramic	HE 21-762
C21	22 pF ceramic	HE 21-757	C60	.1 uF ceramic	HE 21-762
C22	22 pF ceramic	HE 21-757	C61	.1 uF ceramic	HE 21-762
C23	22 pF ceramic	HE 21-757	C62	.1 uF ceramic	HE 21-762
C24	22 pF ceramic	HE 21-757	C63	.1 uF ceramic	HE 21-762
C25	22 pF ceramic	HE 21-757	<b>INDUCTORS</b>		
C26	1.0 uF tantalum	HE 25-197	L1	35 uH	HE 235-229
C27	.1 uF ceramic	HE 21-762	L2	1.22 uH bead	HE 475-15
C28	.1 uF ceramic	HE 21-762	L3	1.22 uH bead	HE 475-15
C29	36 pF ceramic	HE 21-709	L4	1.22 uH bead	HE 475-15
C30	47 uF electrolytic	HE 25-921	L5	1.22 uH bead	HE 475-15
C31	.1 uF ceramic	HE 21-762	L6	1.22 uH bead	HE 475-15
C32	.1 uF ceramic	HE 21-762	L7	1.22 uH bead	HE 475-15
C33	.1 uF ceramic	HE 21-762	L8	1.22 uH bead	HE 475-15
C34	.1 uF ceramic	HE 21-762	L9	1.22 uH bead	HE 475-15
C35	10 uF electrolytic	HE 25-931	L10	1.22 uH bead	HE 475-15
C36	.1 uF ceramic	HE 21-762	L11	1.22 uH bead	HE 475-15
C37	.1 uF ceramic	HE 21-762	L12	1.22 uH bead	HE 475-15
C38	180 pF ceramic	HE 21-746	L13	1.22 uH bead	HE 475-15
C39	180 pF ceramic	HE 21-746	L14	1.22 uH bead	HE 475-15
<b>INDUCTORS (CONTINUED)</b>					
L15	1.22 uH bead	HE 475-15	R1	10 kilohm control	HE 10-1154
L16	1.22 uH bead	HE 475-15	R2	100 kilohm control	HE 10-1180
L17	1.22 uH bead	HE 475-15	R3	2 kilohm control	HE 10-1137
L18	1.22 uH bead	HE 475-15	R4	2 kilohm control	HE 10-1137
L19	35 uH	HE 235-229	R5	47 ohm 1/4 watt, 5%	HE 6-470-12
L20	35 uH	HE 235-229	R6	none	HE 6-473-12
L21	35 uH	HE 235-229	R7	47 kilohm 1/4 watt, 5%	HE 6-473-12
L22	35 uH	HE 235-229	R8	jumper	HE 6-105-12
L23	35 uH	HE 235-229	R9	1 megohm 1/4 watt, 5%	HE 6-102-12
<b>RESISTORS</b>					
R10	1000 ohm 1/4 watt, 5%	HE 6-102-12	R10	1000 ohm 1/4 watt, 5%	HE 6-102-12
R11	3900 ohm 1/4 watt, 5%	HE 6-392-12	R11	3900 ohm 1/4 watt, 5%	HE 6-392-12
R12	1800 ohm 1/4 watt, 5%	HE 6-182-12	R12	1800 ohm 1/4 watt, 5%	HE 6-182-12
R13	47 kilohm 1/4 watt, 5%	HE 6-473-12	R13	47 kilohm 1/4 watt, 5%	HE 6-473-12
R14	jumper	HE 6-7200-12	R14	jumper	HE 6-7200-12
R15	720 ohm 1/4 watt, 1%	HE 6-124-12	R15	720 ohm 1/4 watt, 1%	HE 6-124-12
R16	none	HE 6-2370-12	R16	none	HE 6-2370-12
R17	none	HE 6-105-12	R17	none	HE 6-105-12
R18	120 kilohm 1/4 watt, 5%	HE 6-105-12	R18	120 kilohm 1/4 watt, 5%	HE 6-105-12
R19	237 ohm 1/4 watt, 1%	HE 6-105-12	R19	237 ohm 1/4 watt, 1%	HE 6-105-12
R20	1 megohm 1/4 watt, 5%	HE 6-3901-12	R20	1 megohm 1/4 watt, 5%	HE 6-3901-12
R21	3900 ohm 1/4 watt, 1%	HE 6-2201-12	R21	3900 ohm 1/4 watt, 1%	HE 6-2201-12
R22	2200 ohm 1/4 watt, 5%	HE 6-102-12	R22	2200 ohm 1/4 watt, 5%	HE 6-102-12
R23	1000 ohm 1/4 watt, 5%	HE 6-124-12	R23	1000 ohm 1/4 watt, 5%	HE 6-124-12
R24	120 kilohm 1/4 watt, 5%	HE 6-102-12	R24	120 kilohm 1/4 watt, 5%	HE 6-102-12
R25	1000 ohm 1/4 watt, 5%	HE 6-102-12	R25	1000 ohm 1/4 watt, 5%	HE 6-102-12
R26	1000 ohm 1/4 watt, 5%	HE 6-102-12	R26	1000 ohm 1/4 watt, 5%	HE 6-102-12

# PARTS LIST

CIRCUIT  
Comp. No.

HEATH  
Part No.

CIRCUIT  
Comp. No.

HEATH  
Part No.

CIRCUIT  
Comp. No.

DESCRIPTION

DESCRIPTION

## RESISTOR PACKS

RP1 150 ohm HE 9-120  
 RP2 150 ohm HE 9-120  
 RP3 10 kilohm HE 9-106  
 RP4 4.7 kilohm HE 9-133

## INTEGRATED CIRCUITS

PS1 7805 5V regulator HE 442-54  
 PS2 78M12 +12V regulator HE 442-663  
 PS3 LM317 +adj regulator HE 442-708  
 U1 WD1691 HE 443-998  
 U2 none  
 U3 2143-01 HE 443-1000  
 U4 74LS74 HE 443-730  
 U5 74LS624 HE 443-999  
 U6 74LS132 HE 443-792  
 U7 74LS33 HE 443-1063  
 U8 7417 HE 443-72  
 U9 74LS241 HE 443-824

U10 74S240 HE 443-753  
 U11 7417 HE 443-72  
 U12 74LS74 HE 443-730  
 U13 74LS125 HE 443-811  
 U14 74LS74 HE 443-730  
 U15 96LS02 HE 443-1040  
 U16 96LS02 HE 443-877  
 U17 74LS138 HE 443-877  
 U18 4.000 MHz oscillator HE 150-132  
 U19 74LS175 HE 443-752

U20 74LS74 HE 443-730  
 U21 74LS32 HE 443-875  
 U22 FD1797B02 HE 443-997  
 U23 74LS20 HE 443-798  
 U24 74LS138 HE 443-877  
 U25 74LS27 HE 443-800  
 U26 74S74 HE 443-900  
 U27 74LS00 HE 443-728  
 U28 74LS02 HE 443-779  
 U29 25LS2521 HE 443-971

U30 74LS273 HE 443-805  
 U31 74LS305A HE 443-1039  
 U32 7417 HE 443-72  
 U33 74LS244 HE 443-791  
 U34 74LS244 HE 443-791  
 U35 74LS374 HE 443-863  
 U36 74LS244 HE 443-791

## OTHER CIRCUIT COMPONENTS

D1 1N4148 diode HE 56-84  
 D2 1N4148 diode HE 56-84  
 D3 1N4148 diode HE 56-84  
 DS1 8-section slide switch HE 60-621  
 Q1 TIS74 transistor HE 417-246  
 Q2 MPS2369 transistor HE 417-937  
 Q3 MPS2369 transistor HE 417-937

## CONNECTORS - SOCKETS

P1 50-pin right-angle connector HE 432-1197  
 P2 34-pin right-angle connector HE 432-1053  
 P1 14-pin IC socket HE 434-298  
 P2 16-pin IC socket HE 434-299  
 P3 18-pin IC socket HE 434-310  
 P4 20-pin IC socket HE 434-311  
 P5 40-pin IC socket HE 434-253  
 P6 1-pin connector HE 432-121  
 P7 34-pin right-angle connector HE 432-1053  
 P8 50-pin right-angle connector HE 432-1197

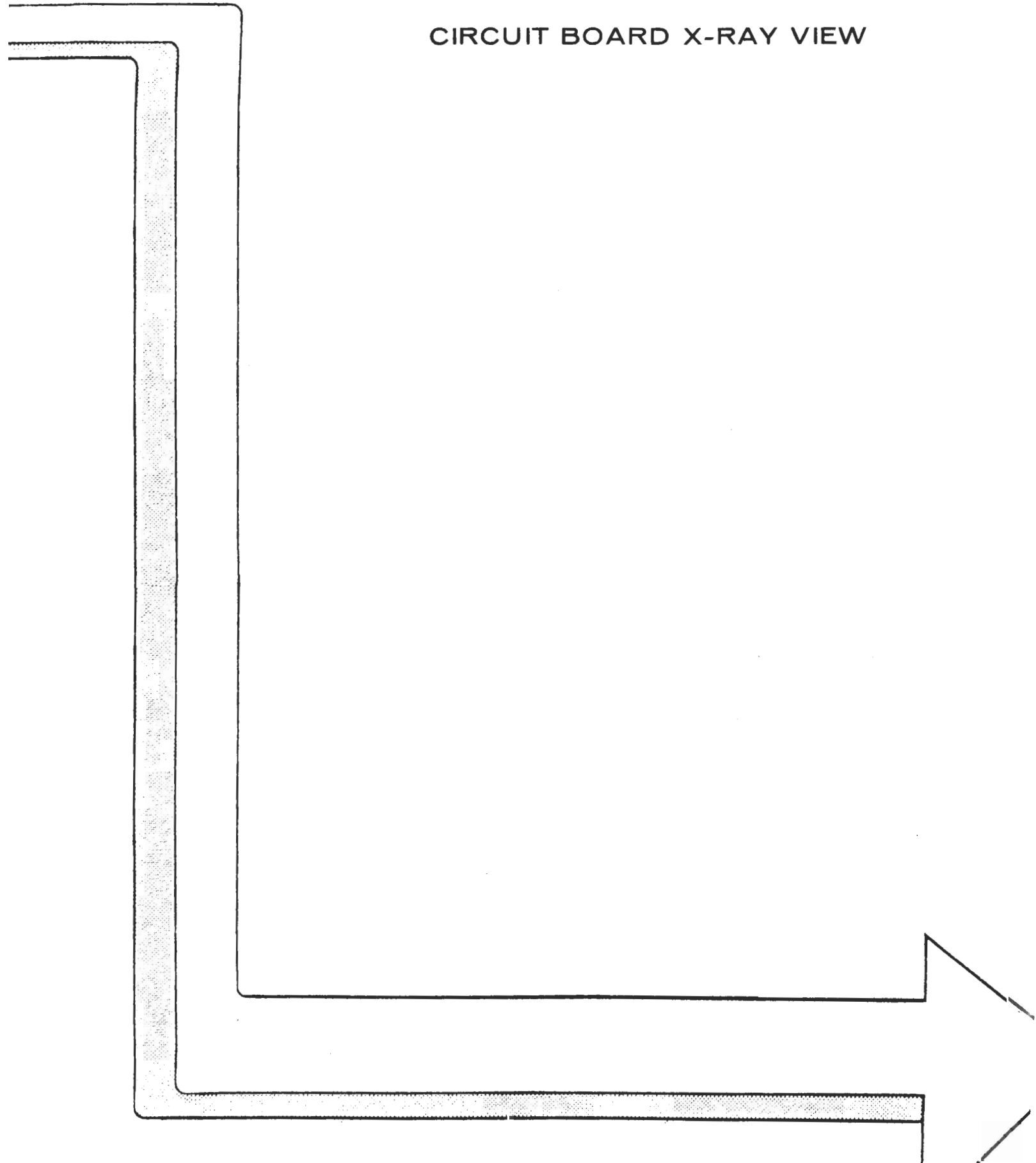
## HARDWARE

#4 lockwasher HE 254-9  
 4-40 nut HE 252-2  
 4-40 x 5/16" screw HE 250-213

## MISCELLANEOUS

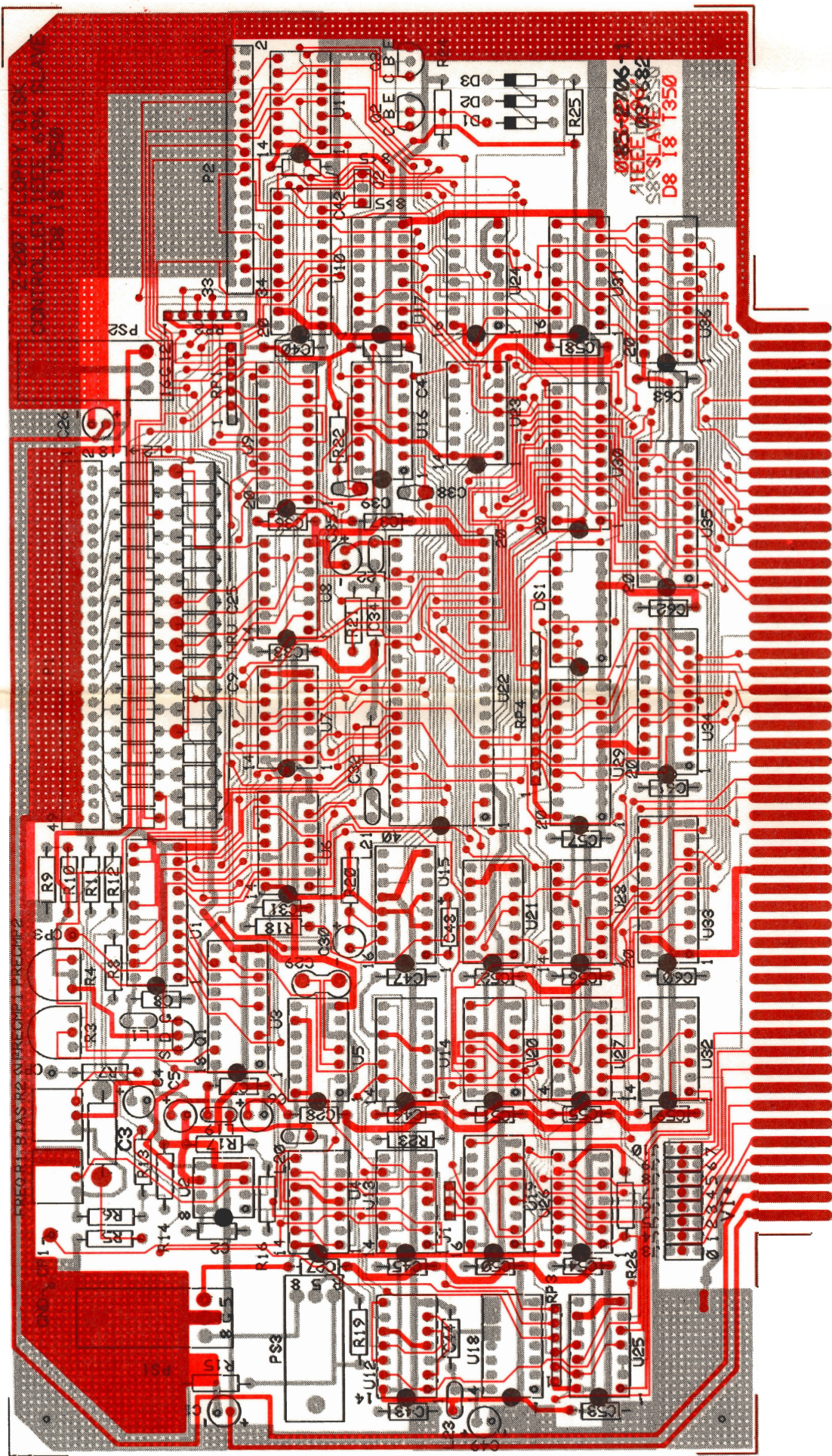
Heat sink HE 215-669  
 PC board (Z-207, early) HE 85-2706-1  
 PC board (H-207 and later Z-207) HE 85-2757-1  
 S-100 circuit board HE 266-1203  
 Wire, solid HE 340-8

CIRCUIT BOARD X-RAY VIEW









DISK CONTROLLER BOARD (#HE-181-3763-1)  
(SHOWN FROM COMPONENT SIDE)



## 48 TPI DISK DRIVE DATA

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## SECTION I

# INTRODUCTION TO THE TM-100-1 AND -2 DISK DRIVES, 48 TPI

### 1. INTRODUCTION

This section contains a description of the physical and functional specifications for the TM-100-1 and -2 disk drives, 48 tracks per inch (TPI), manufactured by Tandon Corporation.

#### 1.1 PURPOSE OF THE DISK DRIVE

The disk drive is a "mini" disk memory designed for random access data entry, storage, and retrieval applications. These applications typically are intelligent terminal controllers, microcomputers, word processing systems, data communications systems, error logging, microprogram loading, and point-of-sale terminals.

The disk drive is capable of recording and reading digital data, using FM, MFM, M2FM or GCR techniques.

#### 1.2 PHYSICAL DESCRIPTION OF THE DISK DRIVE

The disk drive can be mounted in any vertical or horizontal plane. However, when mounted horizontally, the logic circuit board must be up.

The spindle is belt driven by a DC motor with an integral tachometer. The servo control circuit, suitably sized pulleys, and the tachometer control the speed of the spindle. The Read/Write, double-sided head assembly is positioned by means of a stepper motor, split band, and a suitably sized pulley.

The Read/Write/Erase head assembly is a glass-bonded ferrite/ceramic structure. It has a life in excess of 20,000 hours.

For diskette loading, operator access is provided via a slot which is located at the front of the unit.

The electronic components of the disk drive are mounted on two Printed Circuit Board Assemblies (PCBA's), one of which (logic) is located above the chassis, the other of which (servo) is mounted at the rear of the unit. Power and interface signals are routed through connectors that plug directly into the logic PCBA.

#### 1.3 FUNCTIONAL DESCRIPTION OF THE DISK DRIVE

The disk drive is fully self-contained. It requires no operator intervention during normal operation. The disk drive consists of a Spindle Drive system, a Head Positioning system, and a Read/Write/Erase system.

The TM-100-1 is a single-sided disk drive. The TM-100-2 is a double-sided disk drive. The only difference between the two units is the number of heads in the disk drive. The Logic PCB is identical in both models.

When the front door is opened, access is provided for the insertion of a diskette. The diskette is accurately positioned by plastic guides and by the front latch inhibitor. The in/out location is ensured by the backstop.

Closing the front door activates the cone/clamp system, resulting in centering of the diskette and clamping of the diskette to the drive hub. The drive hub is driven at a constant speed of 300 rpm by a servo-controlled DC motor. The magnetic head is loaded into contact with the recording medium whenever the front door is closed.

The magnetic head is positioned over the desired track by means of a stepper motor/band assembly and its associated electronics. This positioner employs a one-step rotation to cause a one-track linear movement. When a write-protected diskette is inserted into the disk drive, the Write Protect sensor disables the write electronics of the disk drive, and a Write Protect output signal is applied to the interface.

When performing a write operation, a 0.33 mm (0.013-inch) (nominal) data track is recorded. Then, this track is tunnel erased to 0.30 (0.012 inch) (nominal).

Data recovery electronics include a low-level read amplifier, a differentiator, a zero crossing detector, and digitizing circuits.

No data decoding ability is provided in the basic disk drive.

The disk drive is also supplied with the following sensor systems:

1. A Track 00 switch that senses when the Head/Carriage assembly is positioned at Track 00.
2. The Index sensor, which consists of a LED light source and phototransistor, is positioned such that a digital signal is generated when an index hole is detected. The Index sensor is a high resolution device that can distinguish holes placed close together, i.e., index sector holes in a hard-sectored diskette.
3. The Write Protect sensor disables the disk drive write electronics whenever a write-protect tab is applied to the diskette (see Section 1.13).

#### 1.4 DISKETTES

The disk drive uses a standard 133.4 mm (5.25 inch) diskette. Diskettes are available with a single index hole or with index and sector holes.

Single index hole diskettes are used when sector information is pre-recorded on the diskette. Multiple index hole diskettes provide sector pulses by means of the Index sensor and electronics.

#### 1.5 MECHANICAL AND ELECTRICAL SPECIFICATIONS

The mechanical and electrical specifications of the disk drive are listed in Table 1-1.

#### 1.6 INTERFACE CIRCUIT SPECIFICATIONS

The interface circuits are designed so that a disconnected wire results in a false signal.

Levels:

True = +0.4 V (maximum)

False = +2.4 V (minimum)

TABLE 1-1  
MECHANICAL AND ELECTRICAL SPECIFICATIONS

Media	Industry-Standard 5.25" diskette
Dimensions	
Height	85.85 mm (3.38 inches)
Width	149.1 mm (5.87 inches)
Length	203.2 mm (8.00 inches)
Weight	1.45 Kg (3.2 pounds)
Temperature (Exclusive of Media)	
Operating	10°C to 44°C (50°F to 112°F)
Nonoperating	-40°C to 71°C (-40°F to 160°F)
Relative Humidity (Exclusive of Media)	
Operating	20% to 80% (Noncondensing)
Nonoperating	5% to 95% (Noncondensing)
Head Settling Time	15 msec (Last Track Addressed)
Error Rates (Maximum)	
Soft Read	1 per 10 <sup>9</sup> bits (Recoverable)
Hard Read	1 per 10 <sup>12</sup> bits (Nonrecoverable)
Head Life	20,000 Hours (Normal Use)
Media Life	3.6 x 10 <sup>6</sup> Passes Per Track
Disk Speed	300 rpm ± 1.5% (Long Term)
Instantaneous Speed Variation	± 3%
Start/Stop Time	250/150 msec (Maximum)
Transfer Rate	FM: 125,000 BPS MFM: 250,000 BPS
Bits Per Disk (Unformatted)	2 Million (FM)
Recording Modes (Typical)	FM, MFM, MMFM
Power	+ 12 VDC ± 0.6 VDC @ 900 mA (Average Maximum) + 5 VDC ± 0.25 VDC @ 600 mA (Average Maximum) with 100 mv P/P Ripple

### 1.7 UNCRATING THE DISK DRIVE

The disk drive is shipped in a protective container which, when bulk packaged, minimizes the possibility of damage during shipment. The following procedure is the recommended method for uncrating the disk drive.

1. Place the shipping container on a flat work surface.
2. Remove the upper half of the inner container.
3. Remove the disk drive from the lower half of the inner container.
4. Check the model number and top assembly description against the packing slip.
5. Examine the contents of the shipping container for possible damage.
6. Notify the carrier immediately if any damage is noted.

### 1.8 PHYSICAL CHECKOUT OF THE DISK DRIVE

Before applying power to the disk drive, the following inspection procedure should be performed:

1. Remove the plastic bag.
2. Remove the cable harness from the door latch of the disk drive.
3. Check that the front latch opens and closes. Note that when the door is opened, the head arm raises.
4. Ensure that the front panel is secure.
5. Manually rotate the drive hub. The drive hub should rotate freely.
6. Check that the PCBA's are secure.
7. Check that the connectors are firmly seated.
8. Check for debris or foreign material between the heads.
9. Notify the carrier immediately if any damage is noted.

### 1.9 INTERFACE CONNECTIONS

Signal connections for the disk drive are made via a user-supplied 34-pin, flat ribbon connector (3M Part Number 3463-0001 or equivalent). This connector mates directly with the PCBA connector at the rear of the disk drive. The DC power connector is a four-pin connector (Amp Mate-N-Lok Part Number 1-480424-0), which mates with the connector on the logic PCBA at the top rear of the disk drive.

The signal connector harness should be of the flat ribbon or twisted pair type, have a maximum length of ten (10) feet, and have a 22-to-24 gauge conductor compatible with the connector that is to be used.

Power connections should be made with 18-AWG cable (minimum). In addition, the PCBA-mounted, DC power connector is keyed.

## 1.10 CHASSIS GROUND

To ensure proper operation of the disk drive, the chassis should be connected to earth ground. A 3/16-inch male QC lug, located at the rear of the chassis, is provided to facilitate this connection.

### 1.10.1 Isolated Ground

The power return of the disk drive is connected to the drive chassis. If a particular application does not require this, the mounting screw near the middle of the servo PCB may be replaced with a nylon screw. This isolates the power return from the chassis ground.

## 1.11 MOUNTING THE DISK DRIVE

The disk drive has been designed such that it can be mounted in any plane, i.e.: upright, horizontal, or vertical. The only restriction is that the logic PCBA side of the chassis must be uppermost when the disk drive is mounted horizontally. Eight (8) 6-32 tapped holes are provided for mounting: two (2) on each side and four (4) on the bottom of the housing (see Figure 1-1).

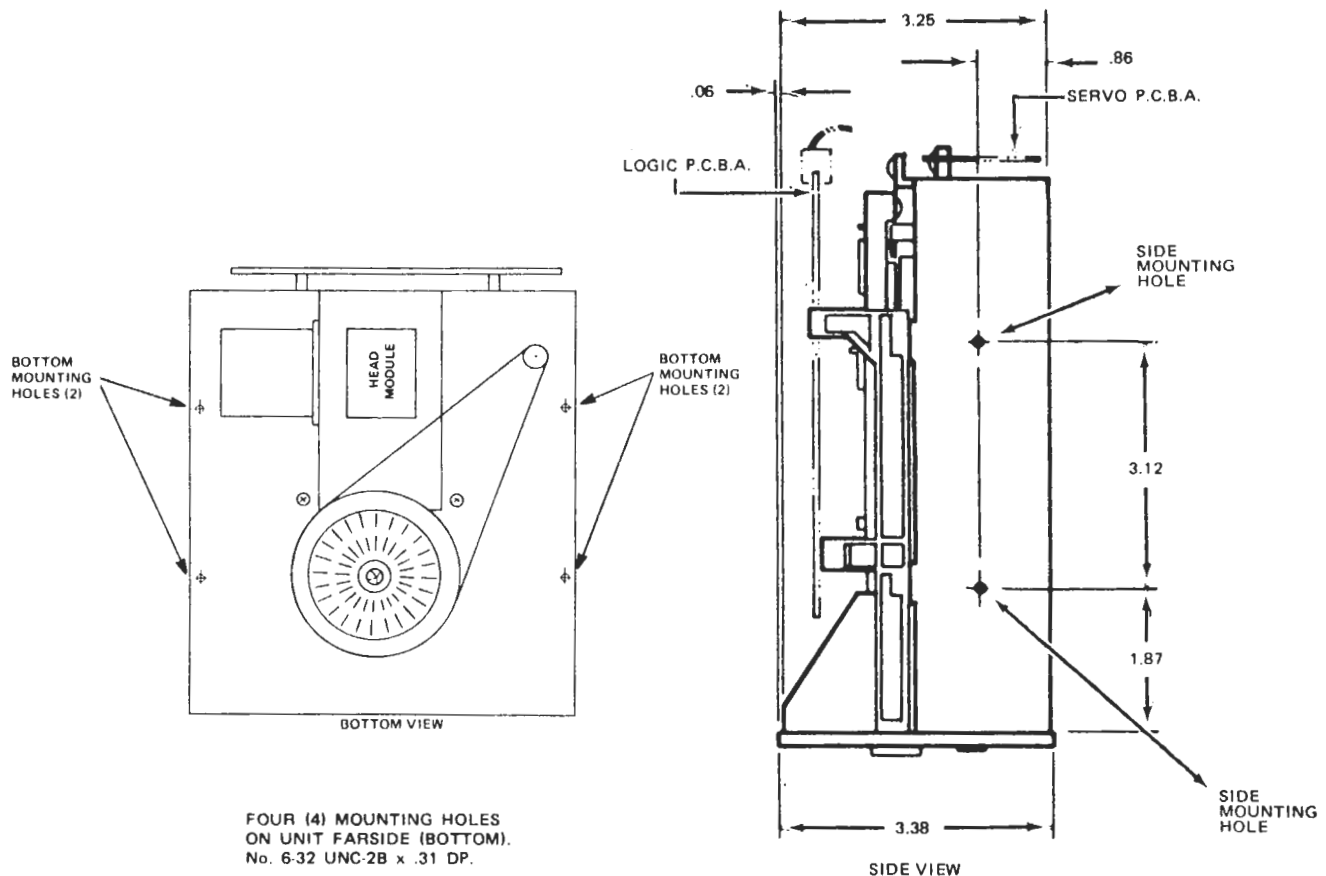


Figure 1-1  
TM-100 Disk Drive Mounting Configuration

### 1.11.1 Hardware

The disk drive is manufactured with certain critical internal alignments that must be maintained. Hence, it is important that the mounting hardware does not introduce significant stress on the disk drive.

Any mounting scheme in which the disk drive is part of the structural integrity of the enclosure may cause equipment operating problems and should be avoided.

Mounting schemes should allow for adjustable brackets or incorporate resilient members to accommodate tolerances.

#### 1.11.2 Dust Cover

The design of an enclosure should incorporate a means to prevent contamination from loose items — e.g., dust, lint, paper chad — since the disk drive does not have a dust cover.

#### 1.11.3 Cooling System Requirements

Heat dissipation from a single disk drive is normally 15 watts (51 Btu/Hr.) under high line conditions. When the disk drive is mounted so that the components have access to the free flow of air, normal convection cooling allows operation over the specified temperature range.

When the disk drive is mounted in a confined environment, air flow must be provided to maintain specified air temperatures in the vicinity of the motors, the PCBA's, and the diskette.

### 1.12 DISKETTE CARE, HANDLING, AND STORAGE

It is important that the diskette be cared for, handled, and stored properly so that the integrity of the recorded data is maintained. A damaged or contaminated diskette can impair or prevent recovery of data, and can result in damage to the Read/Write heads of the disk drive.

The following list contains information on how the diskette can optimally be cared for, handled, and stored.

1. Keep the diskette away from magnetic fields.
2. Do not touch the precision surface of the diskette with fingers.
3. Insert the diskette carefully into the disk drive until the backstop is encountered.
4. Do not bend or fold the diskette.
5. Put the diskette into its jacket when it is not in use.
6. Store the diskette at temperatures between 10°C and 52°C or 50°F and 125°F.

### 1.13 WRITE PROTECT

The disk drive is equipped with a Write Protect Switch Assembly. This sensor operates in conjunction with a diskette that has a slot cut in the protective jacket.

When the slot is covered with a self-adhesive tab, the diskette is write protected. The slot must be uncovered to write on the diskette.

### 1.14 OPERATION OF THE DISK DRIVE

The disk drive consists of the mechanical and electrical components necessary to record and to read digital data on a diskette. User-provided DC power at +12 V and +5 V is required for operation of the disk drive.

## 1.15 ORGANIZATION OF THE DISK DRIVE

All electrical subassemblies in the disk drive are constructed with leads that terminate in 4- to 5-pin connectors, enabling the individual assemblies to be removed.

The magnetic heads are connected to the PCBA via cables that terminate in 5-pin female connectors and their associated male sockets, which are located in close proximity to the Read/Write data electronics.

Interface signals and power are provided via connectors at the rear of the disk drive.

## 1.16 COMPONENTS OF THE DISK DRIVE

The disk drive consists of seven (7) functional groups:

1. Index Pulse Shaper
2. Write Protect Sensor
3. Track 00 Sensor
4. Spindle Drive Control
5. Carriage Position Control
6. Write/Erase Control
7. Read Amplifier and Digitizer

Figure 1-2 is a functional block diagram of the disk drive. It should be referred to in conjunction with the following sections. The data in the ensuing figures is primarily represented in simplified form.

### 1.16.1 Index Pulse

An index pulse is provided to the user system via the Index Pulse interface line. The index circuitry consists of an Index LED, an Index Photo Transistor, and a Pulse Shaping Network. As the index hole in the disk passes the Index LED/Photo Transistor combination, light from the LED strikes the Index Photo Transistor, causing it to conduct. The signal from the Index Photo Transistor is passed to the Pulse Shaping Network, which produces a pulse for each hole detected. This pulse is presented to the user on the Index Pulse Interface line.

### 1.16.2 Write Protect

A Write Protect signal is provided to the user's system via the Write Protect interface line. The Write Protect circuitry consists of a Write Protect sensor and circuitry that routes the signal that is produced.

When a write protected diskette is inserted in the disk drive, the sensor is activated and the logic disables the write electronics and supplies the status signal to the interface.

### 1.16.3 Track 00 Switch

The level on the Track 00 interface line is a function of the position of the magnetic head assembly. When the head is positioned at Track 00 and the stepper motor is at the home position, a true (low) level signal is generated at the interface.

### 1.16.4 Spindle Drive System

The Spindle Drive system consists of a spindle assembly driven through a drive belt by a DC motor/tachometer combination.



The servo electronics required for speed control are associated with the spindle drive motor.

The control circuitry also includes a current limiter and interface control line. When the Drive Motor Enable interface line is true, the drive motor is allowed to come up to speed. When the current through the drive motor exceeds 1.3 ampere, the current limit circuitry disables the motor drive.

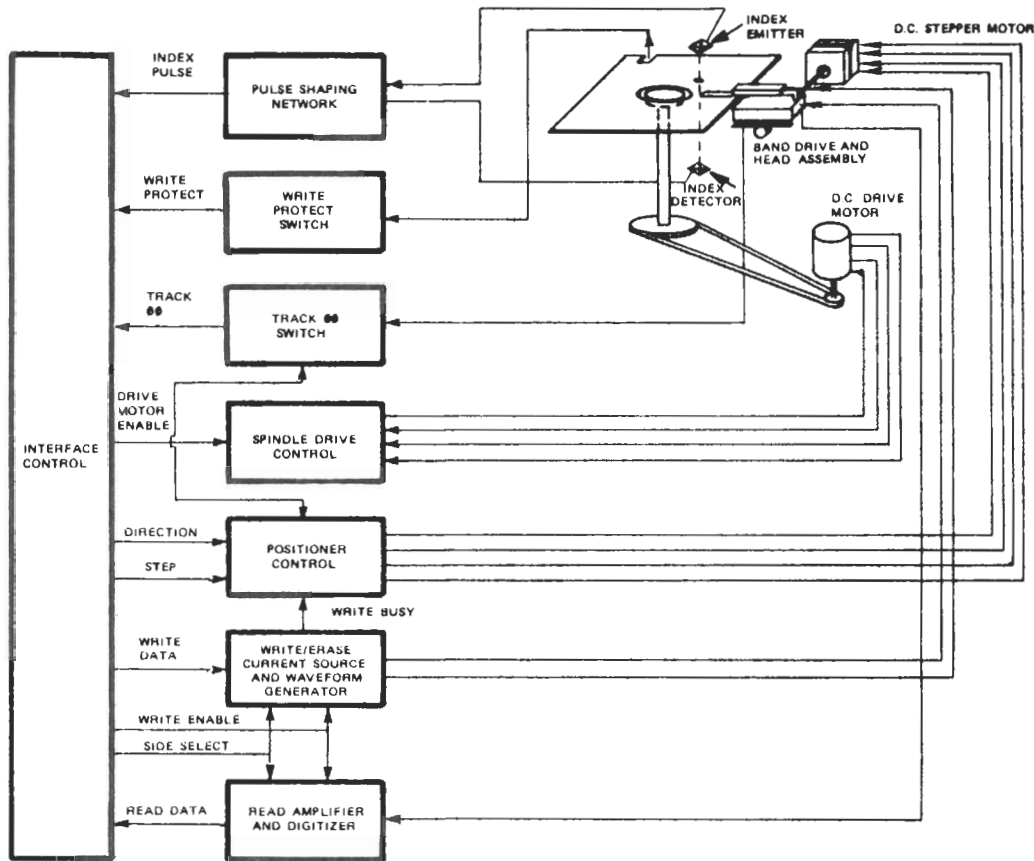


Figure 1-2  
TM-100 Disk Drive Functional Block Diagram

### 1.16.5 Positioner Control

The Head Positioning system utilizes a four-phase stepper motor drive, which changes one phase for each track advancement of the Read/Write carriage. In addition to the logic necessary for motion control, a gate is provided which inhibits positioner motion during a write operation.

### 1.16.6 Data Electronics

Information can be recorded on the diskette by using a double-frequency code. Figure 1-3 illustrates the magnetization profiles in each bit cell for the number sequence shown for FM recording.

The erase gaps provide a guard band on either side of the recorded track. This provides flexibility in track positioning.

All signals required to control the data electronics are provided by the user system and are shown in the TM-100 disk drive functional block diagram (see Figure 1-2). These control signals are:

1. Select
2. Write Enable
3. Write Data
4. Side Select

The Read Data composite signal is sent to the user system via the interface.

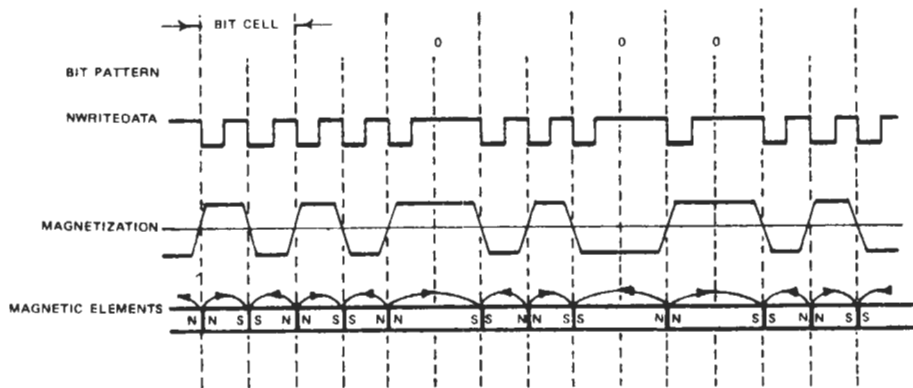


Figure 1-3  
FM Recording Magnetization Profiles

#### 1.16.6.1 Data Recording

The write electronics consist of a Write Current Source, a Write Waveform Generator, an Erase Current Source, the Trim Erase Control Logic, and the Head Select Logic (see Figure 1-2).

The read/write winding on the magnetic head is center-tapped. During a write operation, current from the Write Current Source flows in alternate halves of the winding, under control of the Write Waveform Generator.

The conditions required for recording, i.e., unit ready, must be established by the user system, as follows:

1. Drive speed stabilization occurs 250 msec after the drive motor is started.
2. Subsequent to any step operation, the positioner must be allowed to settle. This requires 20 msec after the last step pulse is initiated, i.e., 5 msec for the step motion and 15 msec for settling.
3. The foregoing operations can be overlapped, if required.

Figure 1-4 illustrates the timing diagram for a write operation. At  $t = 0$ , when the unit is ready, the Write Enable interface line goes true. This enables the Write Current Source.

The Trim Erase control goes true 390 msec after the Write Enable interface line since the trim erase gaps are behind the read/write gap. It should be noted that this value is optimized between the requirements at Track 00 and at Track 39, so that the effect of the trim erase gaps on previous information is minimized.

Figure 1-4 shows the information on the Write Data interface line and the output of the Write Waveform Generator, which toggles on the leading edge of every Write Data pulse.

Note that a minimum of 4 usec and a maximum of 8 usec between Write Enable going true and the first Write Data pulse is only required if faithful reproduction of the first Write Data Transition is significant.

At the end of recording, at least one additional pulse on the Write Data line must be inserted after the last significant Write Data pulse to avoid excessive peak shift effects.

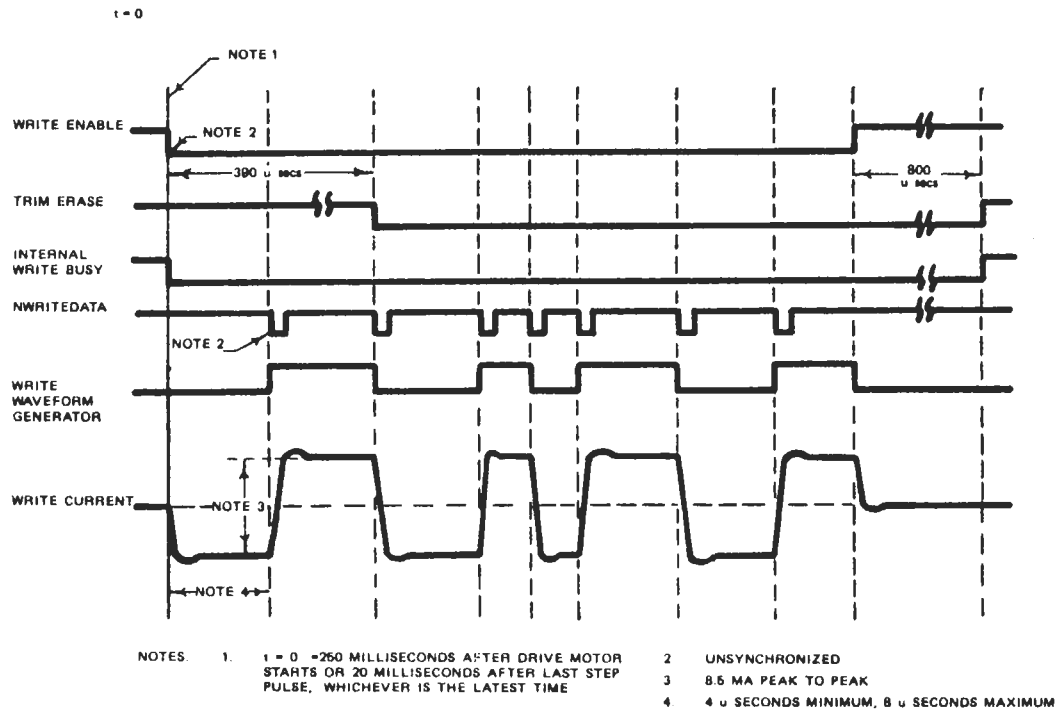


Figure 1-4  
Write Operation Timing Diagram

The duration of a write operation is from the true going edge of Write Enable to the false going edge of Trim Erase. This is indicated by the internal Write Busy waveform shown (see Figure 1-4).

The Read electronics consist of:

1. Read Switch/Side Select
2. Read Amplifier
3. Filter
4. Differentiator
5. Comparator and Digitizer

The Read switch is used to isolate the Read Amplifier from the voltage excursion across the magnetic head during a Write operation. The side select is used to enable one of the Read/Write/Erase heads.

The disk drive must be in a ready condition before reading can begin. As with the data recording operation, this ready condition must be established by the user system. In addition to the requirements established in this section, a 100 usec delay must exist from the trailing edge of the Trim Erase signal to allow the Read Amplifier to settle after the transient caused by the Read switch returning to the Read mode.

The output signal from the Read/Write head is amplified by a Read Amplifier and filtered by a linear phase filter to remove noise (see Figure 1-5). The linear output from the filter is passed to the Differentiator, which generates a waveform whose zero crossovers correspond to the peaks of the Read signal. Then, this signal is fed to the Comparator and the Digitizer circuitry.

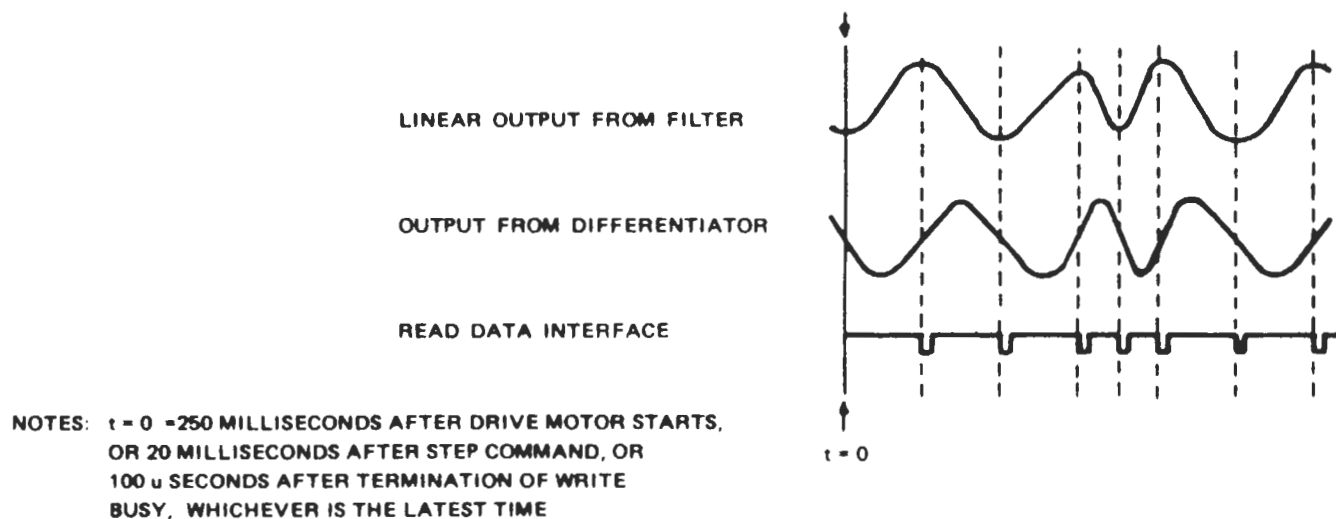


Figure 1-5  
Read Timing Diagram

The Comparator and the Digitizer circuitry generate a 1 usec Read Data pulse, corresponding to each peak of the Read signal. Then, the Composite Read Data signal is sent to the user system via the Read Data interface line.

## 1.17 INTERFACE ELECTRONICS

All interface signals are TTL-compatible. Logic true (low) is +0.4V (maximum); logic false (high) is +2.4V (minimum). The maximum interface cable length is ten (10) feet.

It is recommended that the interface cable be flat ribbon cable, having a characteristic impedance of 100 ohms, or equivalent twisted pairs.

### 1.17.1 Interface Connector Pin Assignments, J1/P1

The interface connector pin assignments, J1/P1, are listed in Table 1-2.

### 1.17.2 Power Connector Pin Assignments

The power connector pin assignments are listed in Table 1-3.

## 1.18 OPTION SELECT

### 1.18.1 Input Line Terminations

The disk drive has the capability of terminating the following input lines:

1. Motor On
2. Direction Select
3. Step
4. Write Data

TABLE 1-2  
INTERFACE CONNECTOR PIN ASSIGNMENTS, J1/P1

<b>CONTROLLER-TO-DISK DRIVE</b>		
<b>Ground</b>	<b>Signal</b>	<b>Mnemonic Description</b>
1	2	Connector Clamp
3	4	Spare
5	6	Select 3 (NDS3)
9	10	Select 0 (NDS0)
11	12	Select 1 (NDS1)
13	14	Select 2 (NDS2)
15	16	Drive Motor Enable (N MOTOR ON)
17	18	Direction (DIR)
19	20	Step (N STEP)
21	22	Write Data (N WRITE DATA)
23	24	Write Gate (N WRITE ENABLE)
31	32	Side Select (N SIDE SELECT)
33	34	Connector Clamp

<b>DISK DRIVE-TO-CONTROLLER</b>		
<b>Ground</b>	<b>Signal</b>	<b>Mnemonic Description</b>
7	8	Index (N INDEX / SECTOR)
25	26	Track 00 (N TRK 00)
27	28	Write Protect (N WRITE PROTECT)
29	30	Read Data (N READ DATA)

TABLE 1-3  
POWER CONNECTOR PIN ASSIGNMENTS

Pin	Supply Voltage
1	+ 12 VDC
2	Return (+ 12 VDC)
3	Return (+ 5 VDC)
4	+ 5 VDC

- 5. Side Select
- 6. Write Gate

These input lines are terminated through a 150 ohm resistor pack that is installed in the dip socket located at IC location 2F. In a single-drive system, this resistor pack should be kept in place to provide the proper terminations. In a multiple-drive system (Program Shunt position MX open), only the last drive on the interface is to be terminated. All other drives on the interface must have the resistor pack removed (see Figure 1-6).

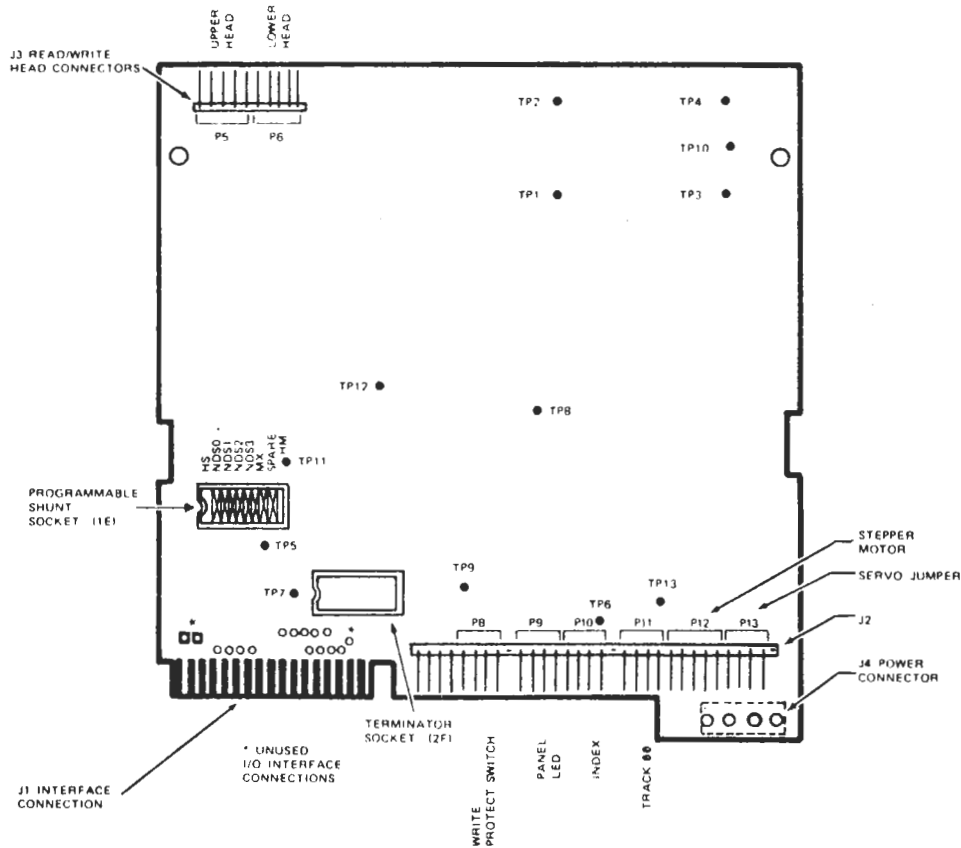


Figure 1-6  
Logic Printed Circuit Board Assembly

### 1.18.2 Drive Select

As shipped from the factory, the disk drive is configured to operate in a single-drive system. The user can easily modify it to operate with other drives in a multiplexed, multiple-drive system. The user can activate the multiplex option by cutting the MX position of the programmable shunt, located at IC location 1E, which allows the input/output (I/O) lines to be multiplexed.

The Select lines provide a means of selecting and deselecting a disk drive. These four (4) lines — NDS0 through NDS3 — select one of the four (4) disk drives attached to the controller.

When the signal logic level is true (low), the disk drive electronics are activated and the disk drive is conditioned to respond to Step or to Read/Write commands. When the signal logic level is false (high), the Input Control lines and the Output Status lines are disabled.

A Select line must remain stable in the true (low) state until the execution of a Step or Read/Write command is completed.

The disk drive address is determined by a Select Shunt on the PCBA. Select lines zero-through-three (0-3) provide a means of daisy chaining a maximum of four (4) disk drives to a controller. Only one (1) line can be true (low) at a time. An undefined operation might result if two or more units are assigned the same address or if two or more Select lines are in the true (low) state simultaneously (see Figure 1-6).

The Program Shunt is AMP Part Number 435704-7. The Program Shunt positions can be cut using AMP's Part Number 435705. The Program Shunt is installed in a dip socket. At the user's option, the Program Shunt may be removed and replaced by a dip switch. In addition, the user may choose to have the Program Shunts preprogrammed and/or color coded by AMP. For this service, contact your local AMP representative.

### 1.19 POWER SAVE OPTION

As shipped from the factory, the disk drive is configured to operate in a single-drive system. Jumper (0 ohm resistor) R51 maintains the power to the stepper motor whether or not the disk drive is selected. However, the jumper in position R51 may be moved to position R50. R50 removes the power to the stepper motor when the disk drive is not selected, for a savings approximately equal to 3.8 watts per drive. When R50 is used, at the time the disk drive is reselected, the user must ensure the track location.

## SECTION II MAINTENANCE CHECKS AND ADJUSTMENTS

### 2. INTRODUCTION

This section is designed for the use of the OEM Repair Department. It contains the maintenance checks and adjustments that are used during the normal life of the disk drive.

Before applying power to the unit or doing any checks or adjustments, visually inspect the disk drive to ensure that it has no missing or broken parts.

The following equipment is required for checks and adjustments:

1. A dual-channel, wideband oscilloscope (HP 1740A or equivalent).
2. An exerciser or software routine capable of stepping the disk drive to any track, selecting the upper or lower head, and writing a 1F (all zeros if FM) or a 2F (all ones if FM) pattern.
3. A Phillips screwdriver.
4. A .050" Allen wrench.
5. A flat blade screwdriver.
6. A 3/16" nut driver.
7. A work diskette.
8. An alignment diskette (Dysan P/N 222/2A).

### 2.1 DRIVE MOTOR CHECKS AND ADJUSTMENTS

The long-term drive motor speed adjustment ensures that the motor's speed is within the range of tolerance specified. The motor speed specification is 300 rpm  $\pm$  1.5%.

#### 2.1.1 Long-Term Drive Motor Speed Checks and Adjustment

##### 2.1.1.1 Preliminary checks required:

Verify power: + 12 VDC  $\pm$  .6 V  
+ 5 VDC  $\pm$  .25 V

- 2.1.1.2 Apply power to the disk drive.
- 2.1.1.3 Activate the drive motor on the interface line.
- 2.1.1.4 Insert a work diskette.
- 2.1.1.5 Observe the speed disk on the spindle pulley under fluorescent lighting (see Figure 2-1).
- 2.1.1.6 Adjust R4, located on the Servo PCBA, until the applicable pattern on the pulley appears stationary (see Figure 2-2).



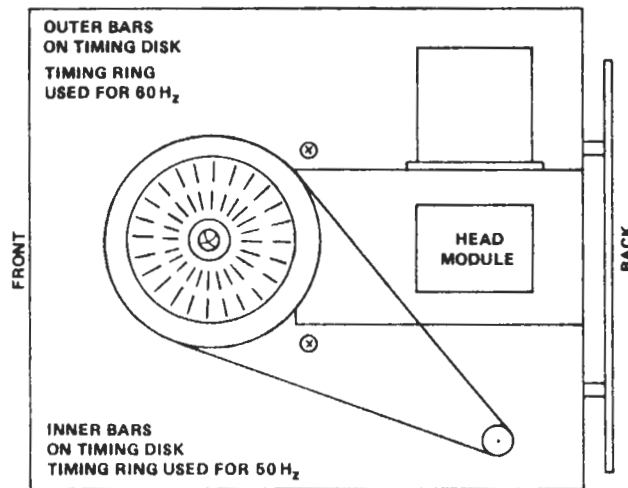


Figure 2-1  
Bottom View of The TM-100 Disk Drive

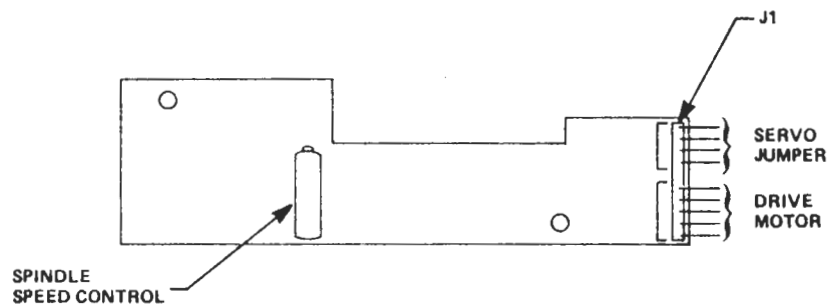


Figure 2-2  
Location of R4 Speed Control Pot

### 2.1.2 Instantaneous Speed Variation Check

The Instantaneous Speed Variation (ISV) checks the smoothness of the spindle's rotation. This is determined by the disk drive system, which consists of the drive motor, drive belt, pulleys, hub, and hub bearings.

2.1.2.1 With the work diskette inserted, write a 2F (all ones) pattern on any track.

2.1.2.2 Connect a wideband oscilloscope to Test Point 5 on the logic PCBA, using Test Point 6 as a ground.

2.1.2.3 Set up a dual-channel, wideband oscilloscope, as follows:

Vertical: 2 Volts Per Division

Time Base: 1 usec Per Division

Internal Trigger: Positive Edge

2.1.2.4 Observe the following pattern (see Figure 2-3).

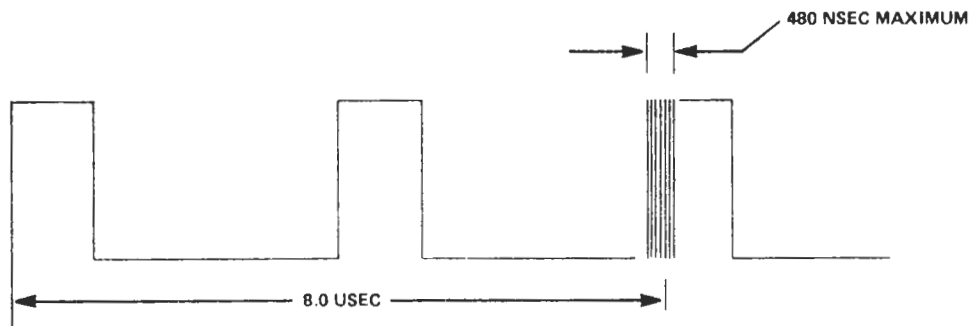


Figure 2-3  
ISV Pulse Pattern

- 2.1.2.5 Measure the amount of jitter present on the leading edge of the third pulse (see Figure 2-3). The leading edge of the third pulse should start  $8 \text{ usec} \pm 240 \text{ nsec}$  from the trigger pulse. Jitter on the third pulse of greater than  $\pm 240 \text{ nsec}$  (480 nsec edge-to-edge) indicates excessive ISV.
- 2.1.2.6 Confirm the measurement (see Section 2.1.2.5) with a second work diskette.
- 2.1.2.7 If the ISV is excessive, replace the drive belt (see Section 5.1), and remeasure the Instantaneous Speed Variation (ISV) (see Section 2.1.2).
- 2.1.2.8 If the ISV is excessive, replace the drive motor (see Section 5.10), and remeasure the ISV (see Section 2.1.2).
- 2.1.2.9 If replacing the drive belt and the drive motor does not cure the excessive ISV, see Section IV (Troubleshooting Guide).

## 2.2 CATS EYE ALIGNMENT CHECK AND ADJUSTMENT

The Cats Eye (CE) alignment procedure locates the magnetic read/write head at the proper radial distance from the hub center line, thus ensuring that the track location is accurate (see Figure 2-4). This adjustment is necessary only after service or if diskette interchange problems are suspected.

### 2.2.1 CE Alignment Check

2.2.1.1 Set up a dual-channel, wideband oscilloscope, as follows:

Channel A: Test Point 1

Channel B: Test Point 2

Ground: Test Point 10

Read Differentially: A plus B, B inverted

Time Base: 20 msec Per Division

External Trigger: Test Point 7, Positive Edge

## 2.2.1.2 Apply power to the disk drive.

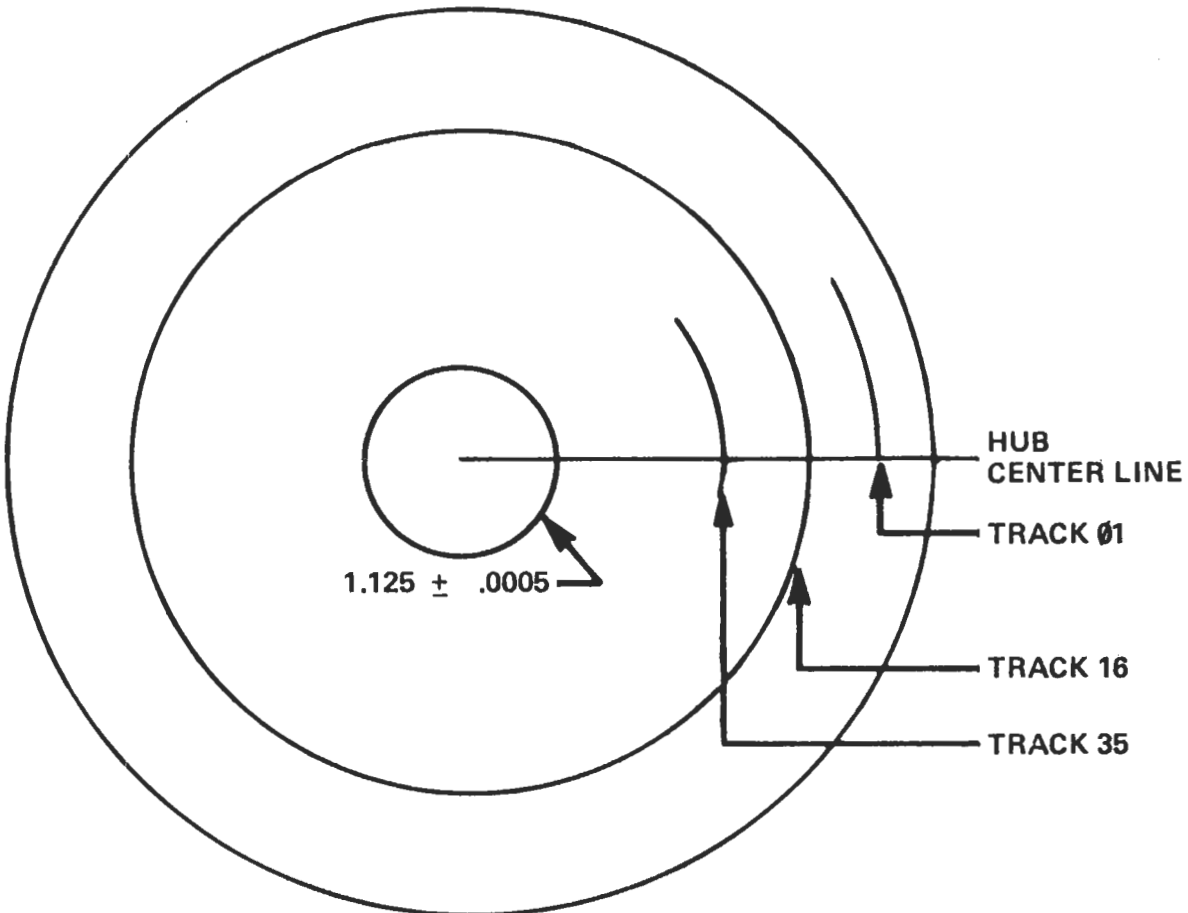


Figure 2-4  
Hub Center Line and Track Locations

NOTES

The Track 16 radius is 1.9167. Other track locations are computed based upon 48 TPI.

- 2.2.1.3 Select the disk drive with the interface logic.
- 2.2.1.4 Insert a Cats Eye alignment diskette (Dysan alignment diskette number 800180) into the disk drive.
- 2.2.1.5 Select Head 00, the lower head.
- 2.2.1.6 Read Track 16 for Cats Eye alignment of the lower magnetic head.
- 2.2.1.7 Adjust the dual-channel, wideband oscilloscope to observe a Cats Eye pattern (see Figure 2-5).
- 2.2.1.8 Verify that the smaller of the two (2) Cats Eye patterns is not less than 75% in amplitude of the other one.

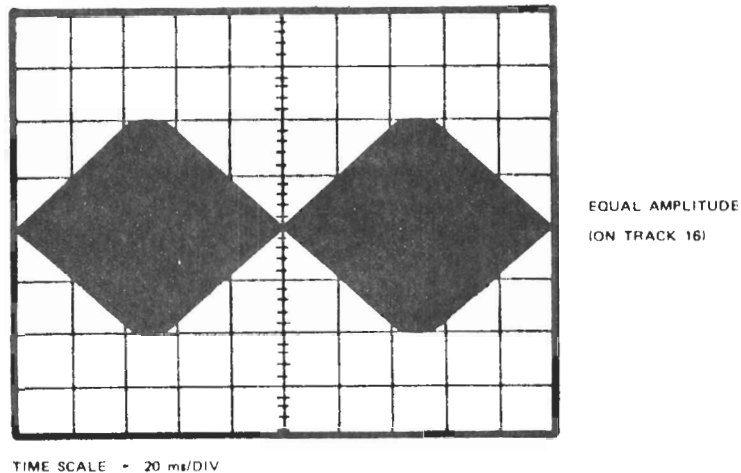


Figure 2-5  
Cats Eye Pattern

NOTE

The 75% figure is for use with an alignment diskette that has been verified against a standard alignment diskette.

- 2.2.1.9 Step the disk drive to Track 00; then, step it back to Track 16.
- 2.2.1.10 Reverify the Cats Eye pattern.
- 2.2.1.11 Step the disk drive to Track 26 or a higher track; then, step it back to Track 16.
- 2.2.1.12 Reverify the Cats Eye pattern.
- 2.2.1.13 Switch to Head 01, the upper magnetic head.
- 2.2.1.14 Read Track 16 to verify the alignment of the upper magnetic head.
- 2.2.1.15 Verify the Cats Eye pattern.
- 2.2.1.16 Step the disk drive to Track 00; then, step it back to Track 16.
- 2.2.1.17 Reverify the Cats Eye pattern.
- 2.2.1.18 Step the disk drive to Track 26 or a higher track; then, step it back to Track 16.
- 2.2.1.19 Reverify the Cats Eye pattern.
- 2.2.1.20 If all of the checks listed above verify or reverify, the Cats Eye alignment of the magnetic head is acceptable.
- 2.2.1.21 If any of the checks listed above does not meet the conditions stated in Section 2.2.1.8, the corresponding magnetic head must be adjusted.

## 2.2.2 Head Adjustment

- 2.2.2.1 Turn the three (3) module retaining screws – two of which are located underneath and one of which is located at the back of the disk drive in the center – counterclockwise one-half (1/2) turn (see Figure 2-6) with a Phillips screwdriver.
- 2.2.2.2 Turn the cam screw (see Figure 2-6) counterclockwise with a flat blade screwdriver.

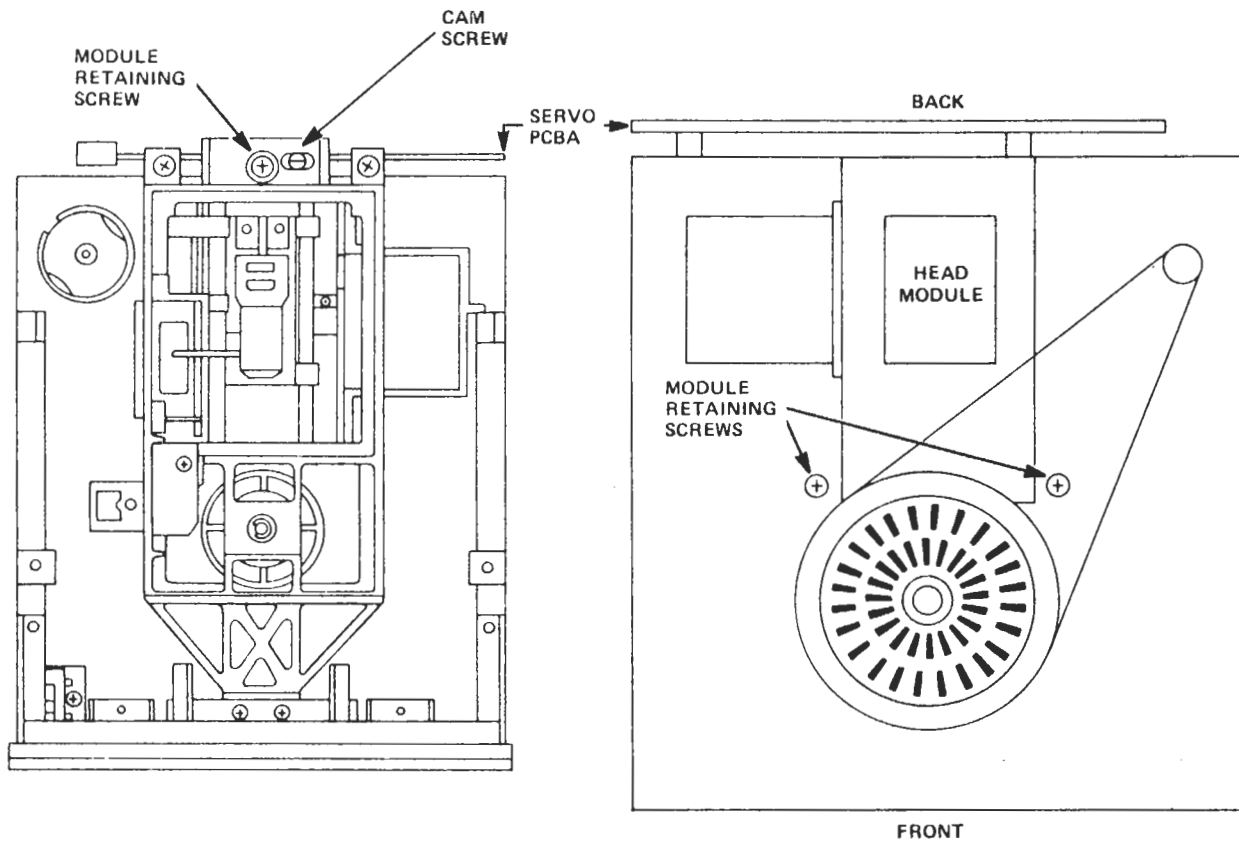


Figure 2-6  
Head Module Retaining and Cam Screws

- 2.2.2.3 Observe the Cats Eye pattern at the magnetic head that is farthest out of alignment.
- 2.2.2.4 Using a flat blade screwdriver, turn the cam screw until the Cats Eye pattern meets the conditions stated in Section 2.2.1.8.
- 2.2.2.5 Tighten the three (3) module retaining screws (see Figure 2-6) with a Phillips screwdriver.
- 2.2.2.6 Reverify the Cats Eye alignment (see Section 2.2.1).
- 2.2.3 Track 00 Stop Adjustment
- 2.2.3.1 The Track 00 stop screw does not allow the carriage assembly to seek to a track lower than Track 00.

- 2.2.3.2 The Track 00 stop screw should be adjusted when the Cats Eye pattern is adjusted or the carriage seeks to a track lower than Track 00.
- 2.2.3.3 Apply power to the disk drive.
- 2.2.3.4 Select the disk drive with the control logic.
- 2.2.3.5 Monitor the output at Test Point 1.
- 2.2.3.6 Monitor the output at Test Point 2.
- 2.2.3.7 Set the dual-channel, wideband oscilloscope to read differentially, A and B, B inverted.
- 2.2.3.8 Insert an alignment diskette.
- 2.2.3.9 Read the information at Track 00.
- 2.2.3.10 Turn the Track 00 stop screw counterclockwise two (2) turns with a .050" Allen wrench (see Figure 2-7).

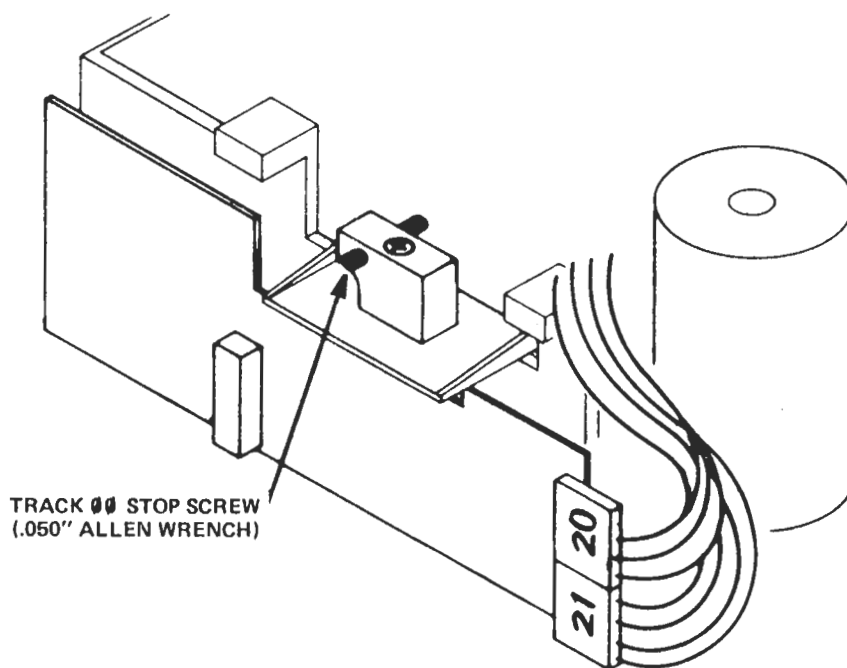


Figure 2-7  
Track 00 Stop

- 2.2.3.11 Slowly turn the Track 00 stop screw clockwise until the output amplitude shown on the dual-channel, wideband oscilloscope begins to decrease.
- 2.2.3.12 Turn the Track 00 stop screw counterclockwise until the amplitude stops increasing.
- 2.2.3.13 Turn the Track 00 stop screw counterclockwise an additional one-eighth (1/8) turn.

## 2.3 INDEX CHECKS AND ADJUSTMENT

The index adjustment changes the time period from the index pulse to the start of the data. The adjustment should be checked after the disk drive has been aligned (see Section 2.1.1) or when diskette interchange errors are suspected.

### 2.3.1 Index Checks

- 2.3.1.1 Check the speed of the long-term drive motor.
- 2.3.1.2 Apply power to the disk drive.
- 2.3.1.3 Select the disk drive with the control logic.
- 2.3.1.4 Set up a dual-channel, wideband oscilloscope, as follows:

External Trigger: Test Point 7, Positive Edge

Read Differentially: A plus B, B inverted

Channel A to Test Point 1

Channel B to Test Point 2

Time Base: 50 usec Per Division

- 2.3.1.5 Insert an alignment diskette.
- 2.3.1.6 Select Track 01.
- 2.3.1.7 Select Head 00, the lower magnetic head.
- 2.3.1.8 Read the trigger point to the start of the first data pulse width (see Figure 2-8).

### NOTE

The specification is 200 usec  $\pm$  100 usec.



TIME SCALE: 50 USEC PER DIVISION

Figure 2-8  
Index-To-Data Pulse

- 2.3.1.9 For double-sided disk drives, if Head 00, the lower head, meets the specification, check Head 01, the upper head.

#### NOTE

Head 01 should meet the same specification.

- 2.3.1.10 If either Head 00 or Head 01 does not meet the specification, adjust the index sensor (see Section 2.3.2.1).
- 2.3.1.11 Recheck both indexes after they are adjusted.
- 2.3.1.12 When both index measurements on a double-sided disk drive or the one index measurement on a single-sided disk drive meet the specification, check the index on Track 34.
- 2.3.1.13 On a double-sided disk drive, check Heads 01 and 00, the upper and lower heads.

#### NOTES

If any index measurement does not meet the specification, the index sensor must be adjusted (see Section 2.3.2.1).

If the index measurements meet the specification, the index sensor does not need to be adjusted.

- 2.3.1.14 Recheck all indexes after each adjustment.
- 2.3.2 Index Adjustment
- 2.3.2.1 From the bottom of the chassis, loosen the index sensor's retaining screw counterclockwise one-quarter (1/4) turn (see Figure 2-9) with a Phillips screwdriver.
- 2.3.2.2 Adjust the index sensor with a flat blade screwdriver until the data pulse begins 200 usec  $\pm$  100 usec from the trigger point.
- 2.3.2.3 Tighten the index sensor's retaining screw with a Phillips screwdriver.
- 2.3.2.4 Verify the indexes.

## 2.4 COMPLIANCE CHECK AND ADJUSTMENT

Compliance is the maximized output of the magnetic head when the pressure of the felt pressure pad is centered over the read/write gap. For single-sided disk drives, a compliance check and adjustment can be made in the field. For double-sided disk drives, a compliance check and adjustment must be made at the factory.

- 2.4.1 Compliance Check
- 2.4.1.1 Rest the disk drive on its cast base.
- 2.4.1.2 Remove the two (2) screws that attach the Logic PCBA to the guide rails.
- 2.4.1.3 Lift out the Logic PCBA, and lay it on the disk drive.



**NOTE**

This allows the operator to reach inside the disk drive to move the magnetic head.

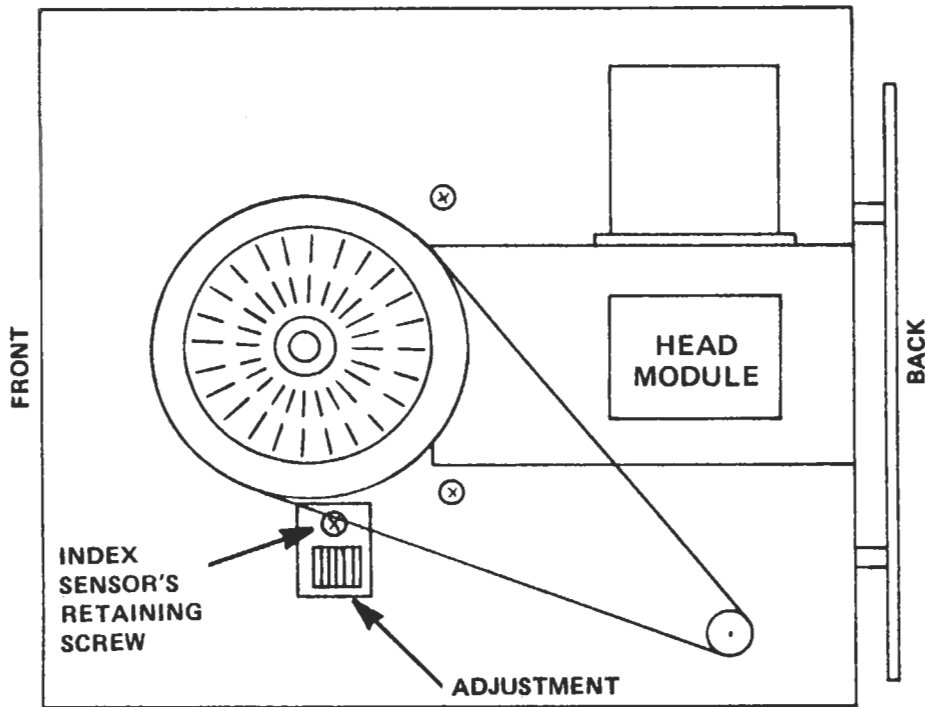


Figure 2-9  
Index Sensor's Retaining Screw and Adjustment

- 2.4.1.4 Apply power to the disk drive.
- 2.4.1.5 Select the disk drive with the control logic.
- 2.4.1.6 Insert a work diskette.
- 2.4.1.7 Write information on Track 34.
- 2.4.1.8 Read the information on Track 34.
- 2.4.1.9 Set up a dual-channel, wideband oscilloscope, as follows:
  - Channel A: Test Point 1
  - Channel B: Test Point 2
  - Ground: Test Point 10

Read Differentially: A and B, B Inverted

Time Base: 10 msec per Division

External Trigger: Test Point 7, Positive Edge

- 2.4.1.10 Read the output voltage.
- 2.4.1.11 With a gram gauge, carefully apply fifteen (15) grams pressure to the upper arm, increasing the load force on the magnetic head.

Note

Fifteen grams is about the weight of a quarter.

- 2.4.1.12 If the output shown on the dual-channel, wideband oscilloscope increases by more than ten percent (10%), adjust the compliance.

#### 2.4.2 Compliance Adjustment

The compliance is adjusted by using the same procedure as is used in the compliance check (see Section 2.4.1).

- 2.4.2.1 Turn the two (2) nuts that attach the upper arm to the carriage assembly (see Figure 2-10) counter-clockwise one-quarter ( $1/4$ ) turn with a  $3/16$ " nut driver.

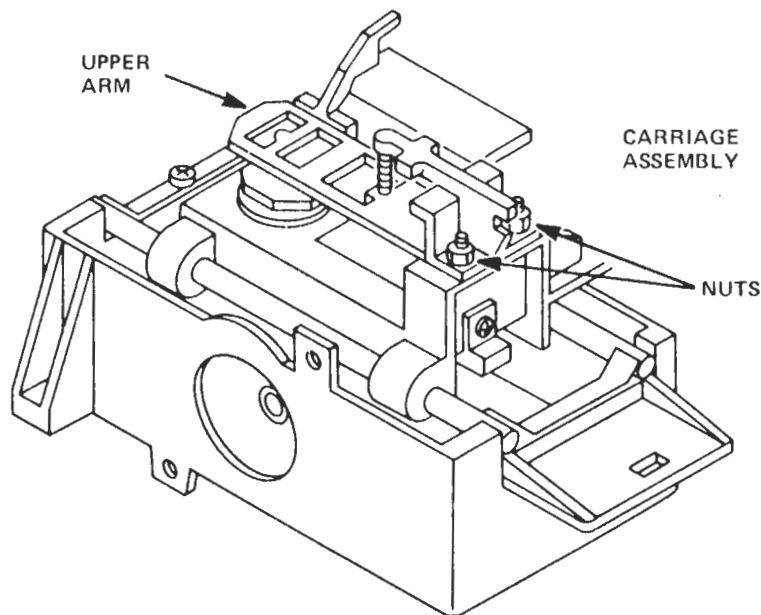


Figure 2-10  
Upper Arm and Nuts

- 2.4.2.2 While monitoring the output, move the upper arm around the axis of the head until the output is the highest.

- 2.4.2.3 Turn the two (2) nuts that attach the upper arm to the carriage assembly clockwise with a 3/16" nut driver while holding the arm in the highest position.
- 2.4.2.4 Reverify the compliance of the magnetic head.
- 2.4.2.5 If the compliance cannot be adjusted, replace the upper arm (see Section 5.13).

2.5 WRITE PROTECT SWITCH ADJUSTMENT PROCEDURE

- 2.5.1 Connect the disk drive to an exercisor or computer with a direct monitor of write printed output (Pin 28 of J1) or, with no power to the disk drive, disconnect Plug 8, and check the continuity with an ohmeter.
- 2.5.2 With a non-write protected diskette inserted, verify that there is no continuity between the two (2) wires of Plug 8 or that there is a non-write protected output to the exercisor or computer, i.e., a high at Pin 28 of J1.
- 2.5.3 With a write protected diskette inserted, verify that there is continuity between the two (2) wires of Plug 8 or that there is a write-protect true output to the controller or exercisor (low at Pin 28 of J1).

Note

A defective circuit board can be responsible for a write protect problem. Test Point 9 should be high for a write-protected disk drive, and low for a non-write protected disk drive.

- 2.5.4 To adjust the write protect switch, loosen the screw that holds the switch to the bracket on the side farthest from the front of the disk drive. Move the switch up or down, as required, to satisfy the condition of Section 2.5.2 and Section 2.5.3 above (see Figure 2-11).

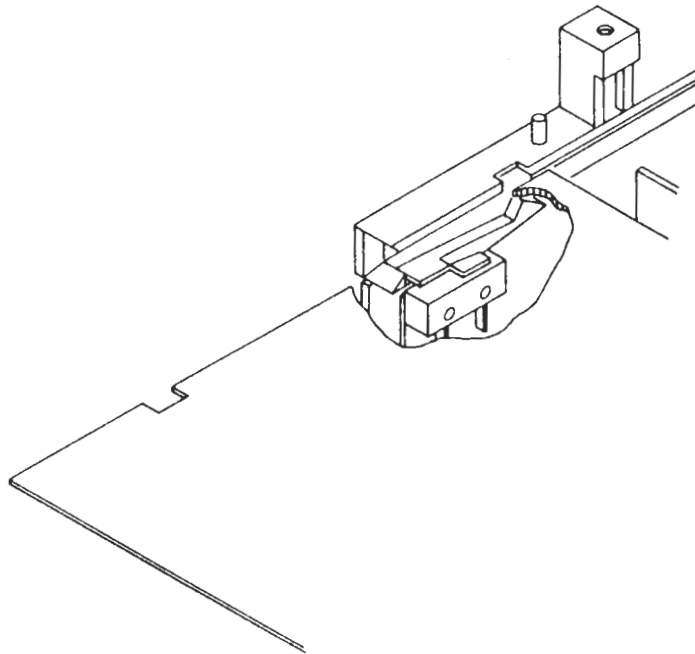


Figure 2-11  
Write Protect Switch Adjustment

## SECTION III PRINTED CIRCUIT BOARD OPERATION

### 3. INTRODUCTION

This section contains the interface description and the mechanical and the electrical adjustments necessary for the TM-100-1 and -2 Disk Drives, 48 TPI. In addition, Section 3.2 and Section 3.3 contain schematic diagrams of the Logic Printed Circuit Board Assembly (PCBA) installed in the disk drive. Section 3.4 contains a schematic diagram of the Servo PCBA installed in the disk drive.

#### 3.1 EXPLANATION OF SYMBOLS AND ABBREVIATIONS

Table 3-1 contains a list of all of the symbols and abbreviations found on the schematic diagrams in this section. In addition, in the functional and circuit descriptions, a specification line "N MOTOR ON" stands for the negative true motor on signal.

#### 3.2 PHYSICAL DESCRIPTION OF THE LOGIC PCBA

The Logic PCBA is approximately 146 mm (5.75 inches) long by 146 mm (5.75 inches) wide. Figure 3-1 contains an illustration of the placement of test points and connectors.

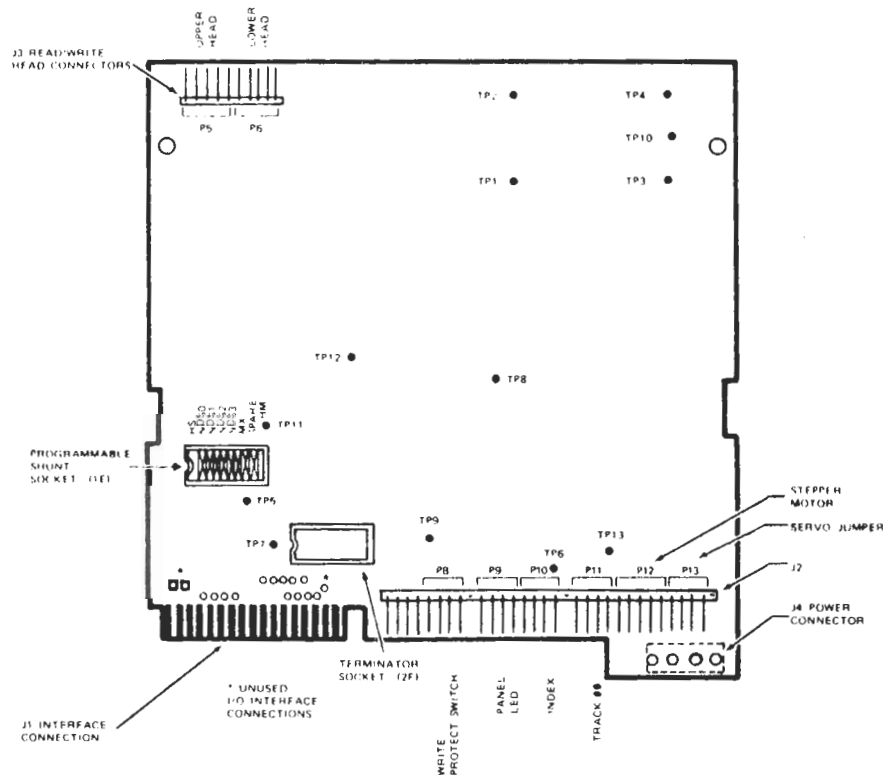












Figure 3-1  
Logic PCBA

TABLE 3-1  
SYMBOLS AND ABBREVIATIONS

Symbol	Meaning
	Erase Coils
	Read/Write Coils
	Normal Transistor
	Photo Transistor
	Driver
	Driver, Open Collector Output
	Driver, Inverted
	Inverter, Open Collector Output
	"AND" Gate, Open Collector Output
	"AND" Gate, Inverted

### 3.3 INTERFACE ELECTRONICS SPECIFICATIONS

All interface signals are TTL compatible. Logic true (low) is +0.4 V (minimum). Figure 3-2 illustrates the interface configuration. The maximum interface cable length is ten (10) feet.

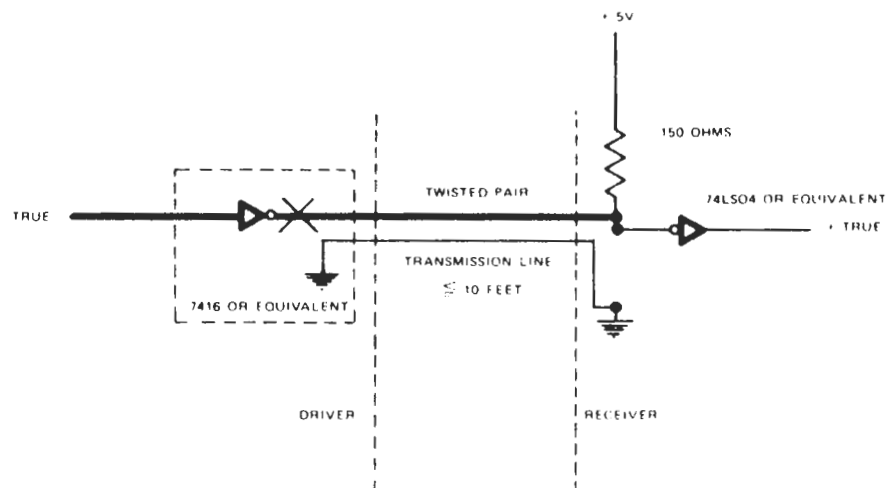


Figure 3-2  
Interface Configuration

It is recommended that the interface cable be flat ribbon cable, with a characteristic impedance of 100 ohms (or equivalent twisted pairs).

Interface connector pin assignments and power connector pin assignments are given in Table 3-2 and Table 3-3.

## 3.3.1 Input Control Lines

TABLE 3-2  
INTERFACE CONNECTOR PIN ASSIGNMENTS, J1/P1

<b>CONTROLLER-TO-DISK DRIVE</b>		
<b>Ground</b>	<b>Signal</b>	<b>Mnemonic Description</b>
1	2	Connector Clamp
3	4	Spare
5	6	Select 3 (NDS3)
9	10	Select 0 (NDS0)
11	12	Select 1 (NDS1)
13	14	Select 2 (NDS2)
15	16	Drive Motor Enable (NMOTOR ON)
17	18	Direction (DIR)
19	20	Step (NSTEP)
21	22	Write Data (NWRITE DATA)
23	24	Write Gate (NWRITE ENABLE)
31	32	Side Select (NSIDE SELECT)
33	34	Connector Clamp

<b>DISK DRIVE-TO-CONTROLLER</b>		
<b>Ground</b>	<b>Signal</b>	<b>Mnemonic Description</b>
7	8	Index (NINDEX / SECTOR)
25	26	Track 00 (NTRK 00)
27	28	Write Protect (NWRITE PROTECT)
29	30	Read Data (NREAD DATA)

TABLE 3-3  
POWER CONNECTOR PIN ASSIGNMENTS

Pin	Supply Voltage
1	+ 12 VDC
2	Return (+ 12 VDC)
3	Return (+ 5 VDC)
4	+ 5 VDC

3.3.1.1 Select Lines (NDS0-NDS3)

Functional Description

The select lines (see Figure 3-3) provide a means of selecting and deselecting a disk drive. These four (4) lines (NDS0-NDS3 standard) select one (1) of the four (4) disk drives attached to the controller. When the signal logic level is true (low), the disk drive electronics are activated and the disk drive is conditioned to respond to Step or Read/Write commands. When the logic level is false (high), the input control lines and output status lines are disabled.

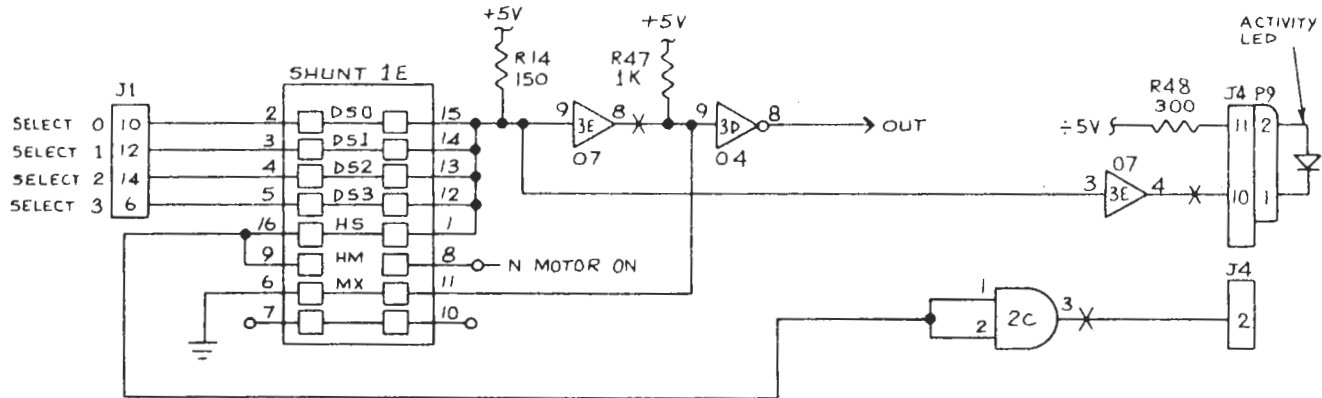


Figure 3-3  
Select Lines Schematic Diagram

A select line must remain stable in the true (low) state until the execution of a Step or Read/Write command is completed.

The disk drive address is determined by a Select Shunt on the PCBA. Select lines 0-3 provide a means of daisy chaining a maximum of four (4) disk drives to a controller. Only one line can be true (low) at a time. An undefined operation might result if two or more units are assigned the same address or if two or more select lines are in the true (low) state simultaneously.



When the disk drive is selected, the activity (front panel) LED will be on.

In a multiple disk drive system, the MX jumper must be cut. If not, the disk drive will always be active.

#### Circuit Description

R14 holds the output of the appropriate select line high until the line is driven low. This is buffered through IC 3E 9-to-8 to IC 3D 9-to-8. IC 3D, Pin 8, is the output that enables the drive electronics. Note that when the MX jumper is not cut, the disk drive is always enabled (Pin 3D-8 high).

The front panel LED is driven by the select logic through IC 3E, Pin 3 to 4. Note that if the disk drive is not selected through the select jumpers, and the MX jumper is not cut, the drive electronics will be active but the front panel LED will not be on.

Normally, Tandon Corporation's disk drives have no head load solenoid. Hence, the HS and the HM jumpers are not used. In no case should both the HS and the HM jumpers be in since this would allow interaction between the Select signal and the Motor On signal. However, if the optional head load solenoid is installed, IC 2C, Pins 1, 2, & 3 drive it. This is selected by either the HS or the HM jumper. The HS jumper enables the head load solenoid driver when the unit is selected. The HM jumper enables the head load solenoid driver when the Motor On signal to the disk drive is true.

#### 3.3.1.2 Drive Motor Enable (N MOTOR ON)

#### Functional Description

When the Drive Motor Enable signal line logic level goes true (low), the disk drive's motor accelerates to its nominal speed of 300 rpm and stabilizes in less than 250 msec. When the logic level goes false (high), the disk drive's motor decelerates to a stop.

Test Point 13 (see Figure 3-4) is low (true) for the Motor On condition.

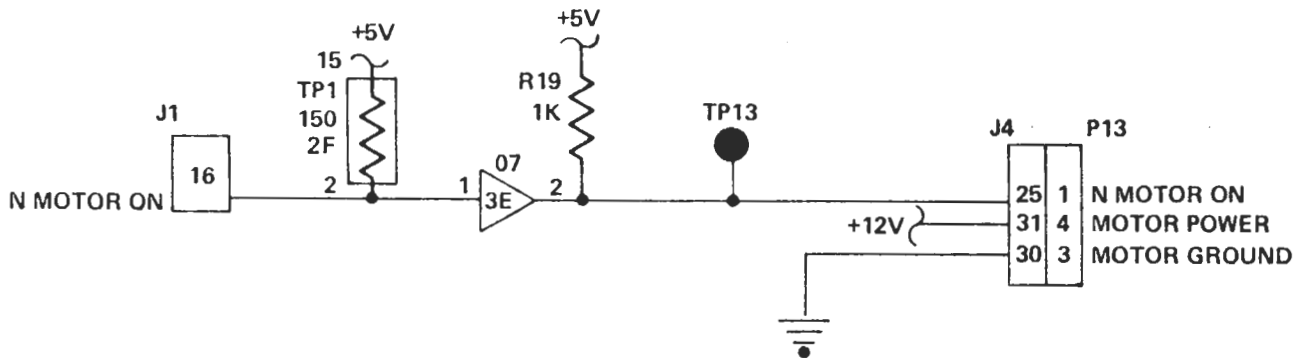


Figure 3-4  
Drive Motor Enable Schematic Diagram

#### Circuit Description

The disk drive's Motor On signal comes in on Pin 16 and is buffered through IC 3E, Pin 1 and Pin 2 to the servo board.

### 3.3.1.3 Direction and Step Lines (Two Lines) (DIR) (N STEP)

#### Functional Description

When the disk drive is selected, a true (low) pulse with a time duration greater than 200 nsec on the Step line initiates the access motion. The direction of motion is determined by the logic state of the Direction line when a Step pulse is issued. The motion is toward the center of the disk drive if the Direction line is in the true (low) state when a Step pulse is issued. The direction of motion is away from the center of the disk drive if the Direction line is in the false (high) state when a Step pulse is issued. To ensure proper positioning, the direction line should be stable 100 usec (minimum) before the trailing edge of the corresponding Step pulse. The Direction line should remain stable until 100 usec after the trailing edge of the Step pulse. The access motion is initiated on the trailing edge of the Step pulse.

Test Point 8 (see Figure 3-5) is low (true) when the carriage is positioned at Track 00 and the step motor is at Phase 0.

When stepping in or out, Test Point 12 (see Figure 3-5) is a high going pulse for each step of the carriage (see Table 3-4).

TABLE 3-4  
STEPPER LOGIC TRUTH

Step In (Toward Track 00)					Step Out (Toward Track 40)						
Pin No.	Phase					Pin No.	Phase				
	0	3	2	1	0		0	1	2	3	0
4C-5	0	1	1	0	0	4C-5	0	0	1	1	0
4C-6	1	0	0	1	1	4C-6	1	1	0	0	1
4C-9	0	0	1	1	0	4C-9	0	1	1	0	0
4C-8	1	1	0	0	1	4C-8	1	0	0	1	1

#### Circuit Description

The direction line comes in on Pin 18 of the interface connector. A high signal directs the step logic to step in toward Track 00. A low signal directs the step logic to step out toward Track 39.

The direction line sets the proper phase to the exclusive OR gates of IC 5D. This signal is also buffered by IC 3D to gate IC 4F to inhibit stepping inward when the disk drive is already at Track 00. This is done at Pin 4 of IC 4B.

The step pulses come in at Pin 20 of the interface connector. They are buffered by 2E and gated at IC 4B by the unit select, the Not Write signal, and by the inward step inhibit at the Track 00 signal. Then, the step pulses go to the C inputs of the two (2) flip flops at IC 4C. The direction of the step, hence the selection of the flip flop to be toggled, is done by the two (2) exclusive OR gates of IC 5D. These gates are controlled by the step direction line and by the state of the two (2) flip flop outputs.

IC 3E, Pins 5 and 6, resets the two (2) flip flops after a Power On.

The output of the two (2) flip flops drives the stepper motor through the drivers of IC 4D. The diodes are for voltage spike elimination.

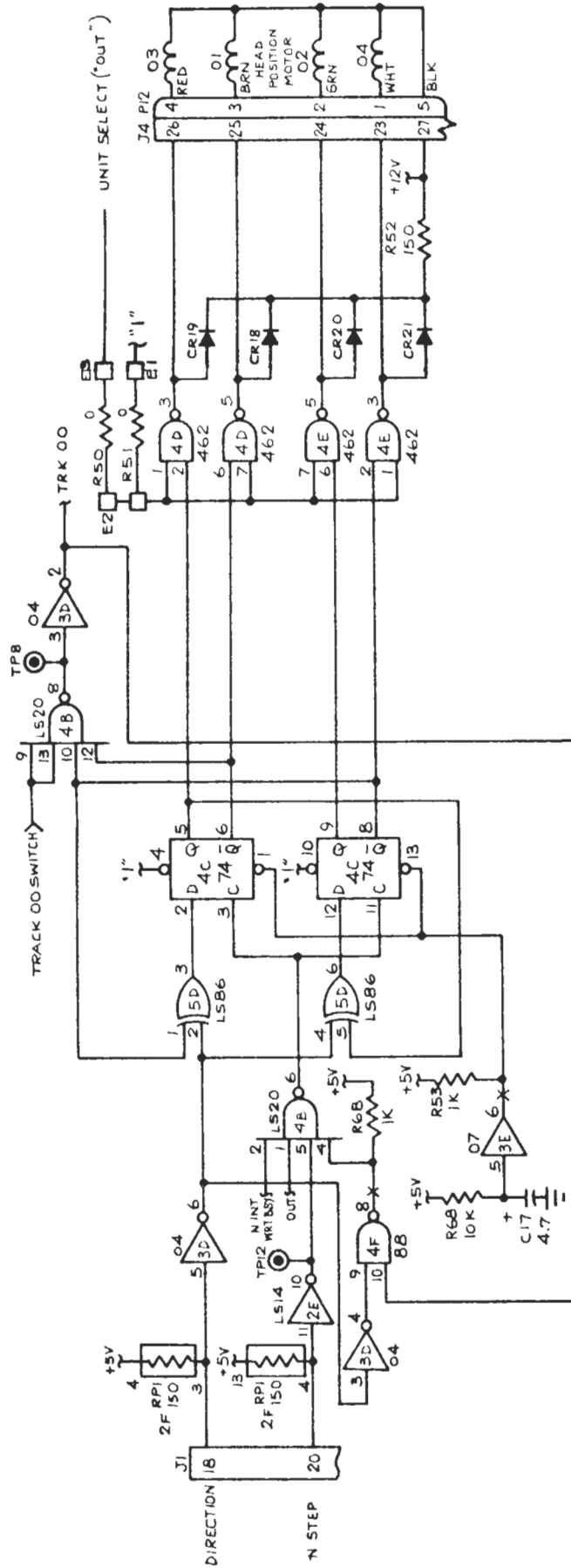


Figure 3-5  
Direction and Step Lines Schematic Diagram

The disk drive is shipped with R50 in place and with R51 not in place. If the resistor is moved to position R51, the power is only on to the stepper motor when the disk drive is selected. 3.8 watts of power are saved because power is not applied to the stepper motor unless the disk drive is selected.

#### 3.3.1.4 Write Enable (N WRITE ENABLE)

##### Functional Description

When the Write Enable signal is true (low), the write electronics are prepared for writing data (read electronics disabled). This signal turns on the write current in the read/write head. Data is written under control of the Write Data input line. It is generally recommended that changes of state on the Write Enable line occur before the first Write Data pulse. However, the separation between the leading edge of Write Enable and the first significant Write Data pulse should not be less than four (4) usec and not greater than eight (8) usec. The same restrictions exist for the relationship between the least significant Write Data pulse and the termination of the Write Enable signal. When the Write Enable line is false (high), all write electronics are disabled.

When a write-protected diskette is installed in the disk drive, the write electronics are disabled, irrespective of the state of the Write Enable line. Stepping is also disabled by a true (low) Write Enable (see Section 3.3.1.3).

Tandon Corporation recommends that the controller wait one (1) msec after the N WRITE ENABLE goes false before any step pulses are sent to the disk drive.

##### Circuit Description

The Write Gate signal comes in on Pin 24 of the interface connector. It is buffered through IC 3D, and gated at IC 3B by the Write Protect and the Unit Select signals, becoming the N WRITE signal. The N WRITE signal goes to Pin 9 of IC 3C, which is configured as a delay. The output at Pin 12 goes high 390 usec after the N WRITE signal goes true.

The N WRITE signal also goes to IC 3C, Pin 1, which is configured as a one-shot delay. The output at Pin 13 goes low only 900 usec after it stops getting pulses at Pin 2 (the pulse from the write data circuit), and the N WRITE goes high or false.

The N ERASE signal is gated through IC 3B. It is true 390 usec after a write true and 900 usec after a write false. This signal enables the erase driver IC 2C. R58 controls the erase current, which is approximately 80 mA.

Pin 4 of IC 3C is the Not Internal Write Busy signal. It enables Q5 through IC 3E, and gates twelve (12) volts to the selected head. This signal also disables the data output at IC 5E, Pin 11. The Not Internal Write Busy signal also enables the write flip flop IC 5C through IC 2E, Pin 12 and Pin 13.

Finally, the Not Internal Write Busy signal goes to driver 2B, Pin 10 and Pin 11, to disable the signal from the heads to the first-stage amplifier, using diodes CR11 and CR12 as gates.

#### 3.3.1.5 Write Data (N WRITE DATA)

##### Functional Description

When the disk drive is selected, the write data line provides the bit-serial Write Data pulses that control the switching of the write current in the heads. The write electronics must be conditioned for writing by the Write Enable line (see Section 3.3.1.4).

For each high-to-low transition on the Write Data line, a flux change is produced at the head write gap. This causes a flux change to be stored on the disk drive. (See Figure 3-6.)

When the double-frequency type encoding technique is used (in which data and clock form the combined Write Data signal), it is recommended that the repetition of the high-to-low transitions, when writing all zeros, be equal to the nominal data rate  $\pm 0.1$  percent. The repetition rate of the high-to-low transitions, when writing all ones, should be equal to twice the nominal data rate  $+ 0.1$  percent. The data transfer rate is 125,000 Bits Per Second (BPS) at single density; it is 250,000 BPS at double density.

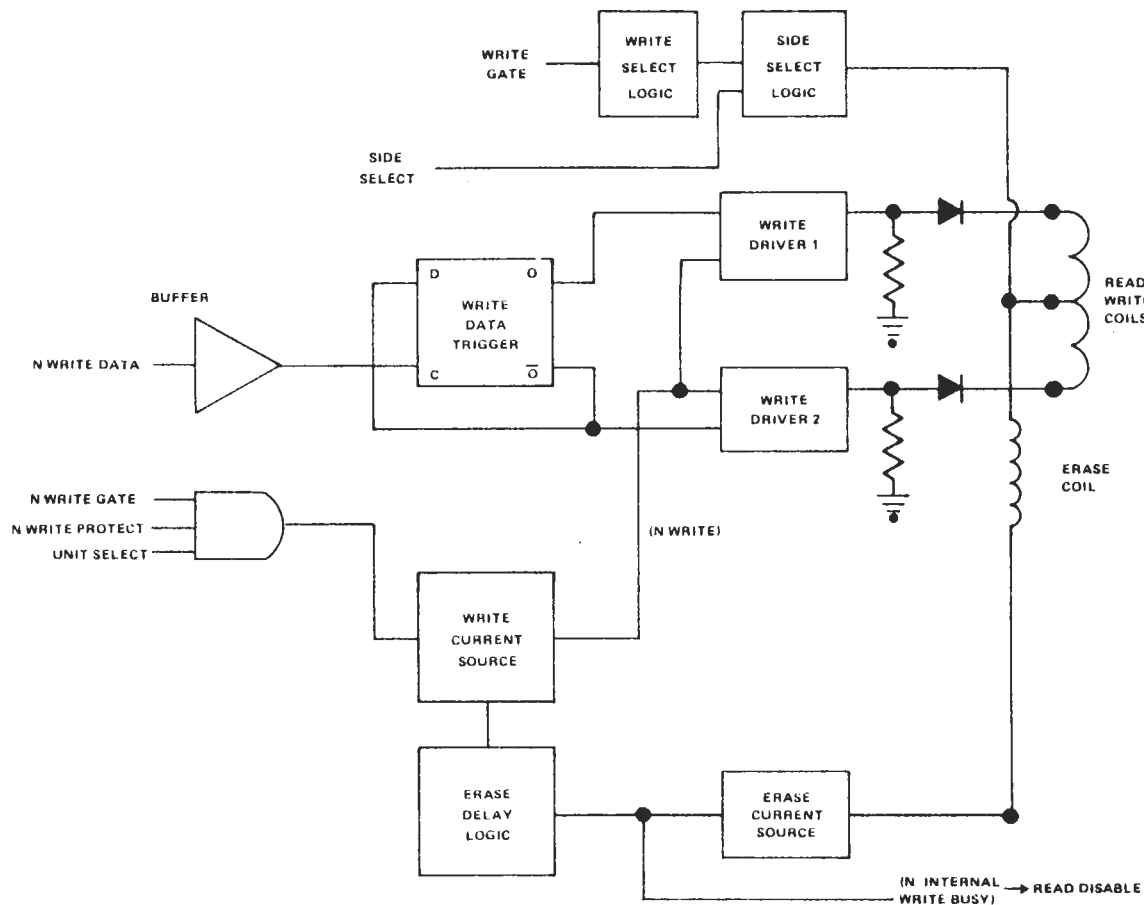


Figure 3-6  
Write Data Circuit Block Diagram

### Circuit Description

Data comes in on Pin 22 of the interface connector in pulse form. Subsequently it is buffered by IC 2E, then fed to a flip flop, IC 5C. The two outputs of the flip flop, through drive IC 2B, alternately turn on Q1 and Q2, which alternates the write current to the selected head. R31 controls the amount of write current. (See Figure 3-7.)

Q3 is activated by the write gate through IC 2B, IC 3B, and IC 3D (see Section 3.3.1.5).

Q4 is designed to allow write current to flow only after the five-volt line is high enough to forward-bias CR14, CR 15, and CR 16, which protects the disk from extraneous data being written when power is initially applied to the disk drive.

### 3.3.1.6 Side Select (N SIDE SELECT)

#### Functional Description

When the Side Select signal is true (low), Side 1 of the disk drive is selected for read/write operations. When this signal is false (high), Side 0 of the disk drive is selected (see Figure 3-10). The Side Select signal must be stable during an entire read or write operation. This signal is best implemented in synchronization with the Device Select line signal (see Section 3.3.1.1).

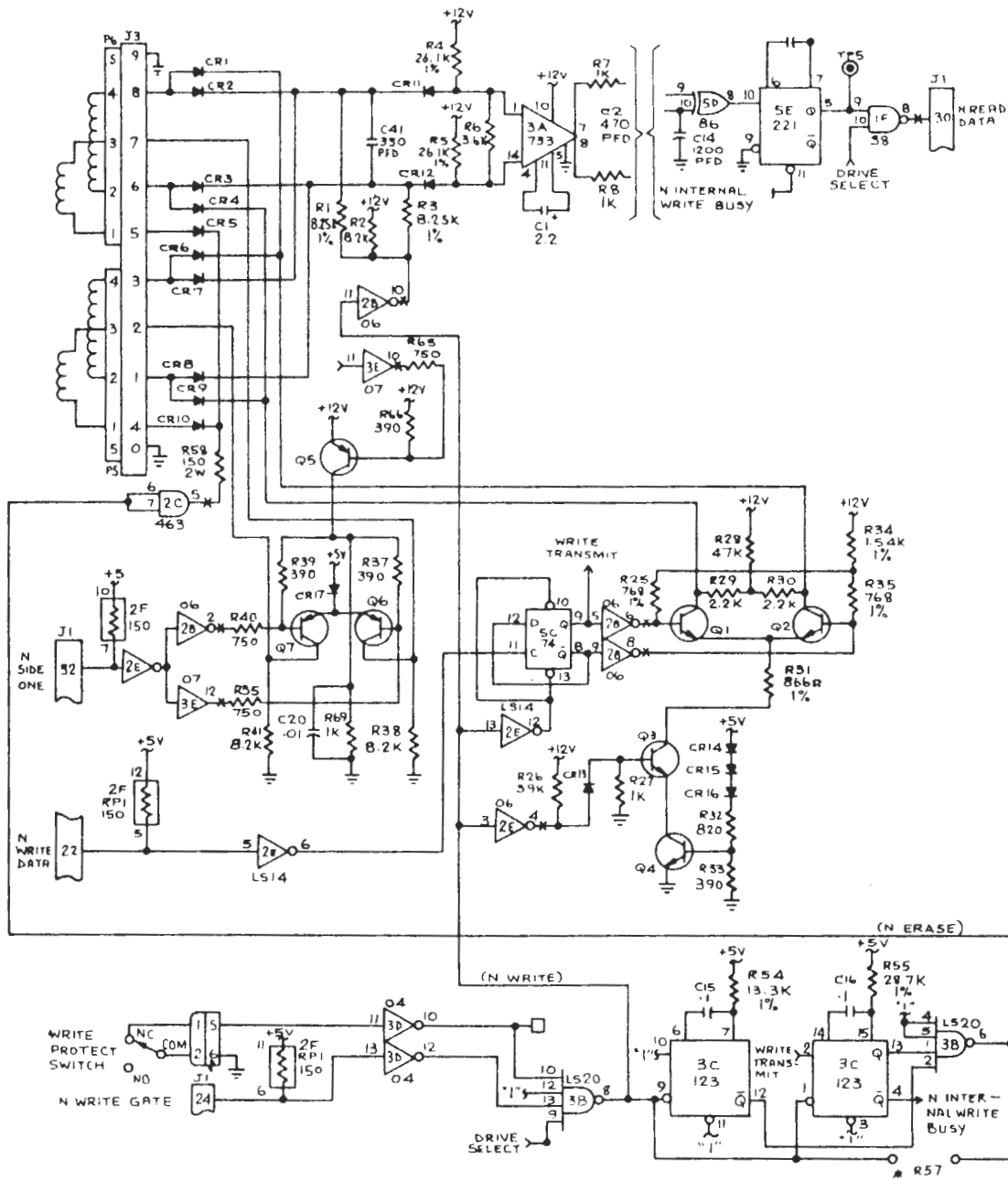


Figure 3-7  
Write Data Schematic Diagram

Circuit Description

The Side Select signal comes in on Pin 32 of the interface connector. If this signal is high, Side 0 is selected. This signal is buffered through IC 2E (see Figure 3-8). From there, the Side Select signal is sent through IC 2B and IC 3E to Drive Q7 or Drive Q6. Drive Q7 sends current to the upper head (Head 1). Drive Q6 sends current to the lower head (Head 0).

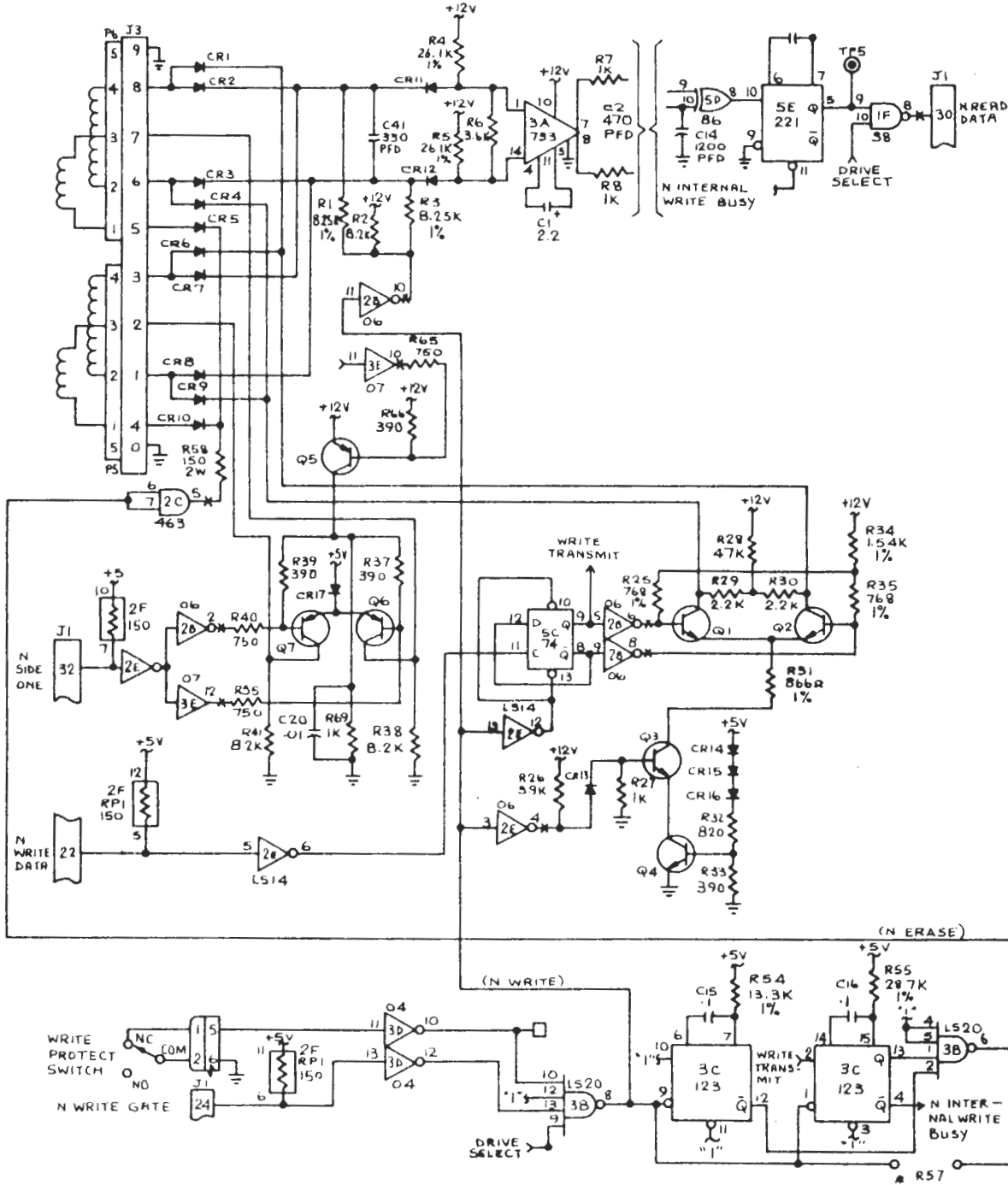


Figure 3-8  
Side Select Schematic Diagram

### 3.3.2 Outputs

#### 3.3.2.1 Index (N INDEX/SECTOR)

##### Functional Description

The Index signal is provided once each revolution (200 msec, nominal) to indicate the beginning of a track to the controller. The Index line remains in the true (low) state for the duration of the Index pulse. The duration of an Index pulse is nominally 4.0 msec.

The leading edge of an Index pulse must always be used to ensure diskette interchangeability between disk drives.

With a standard, soft-sectored diskette installed, Test Point 7 (see Figure 3-9 and Figure 3-10) is a high going pulse, nominally 4.5 msec in duration, every 200 msec.

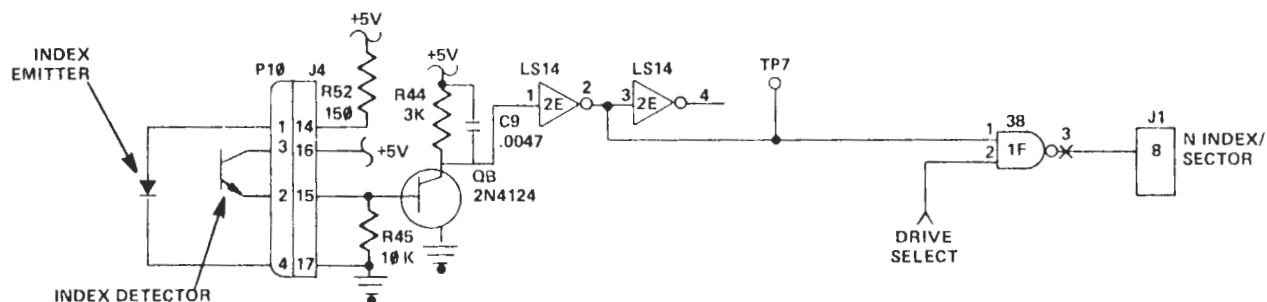


Figure 3-9  
Index Schematic Diagram

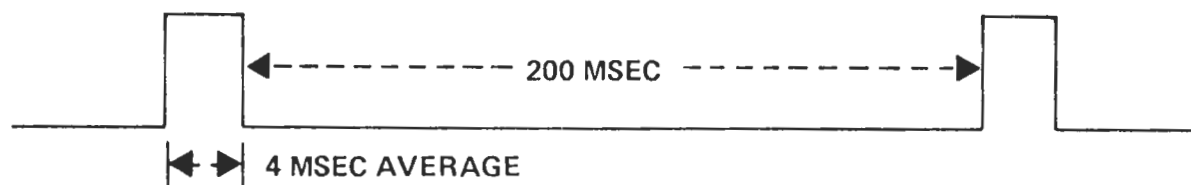


Figure 3-10  
Waveform at Test Point 7 (Soft Sectored)

##### Circuit Description

The Index signal from the disk drive comes in on J4, Pin 15. The Index signal is derived from an infrared LED and a photo-transistor detector. When the index hole in the disk drive allows the light to turn on the detector, Q8 is turned on, sending a signal through IC 2E to IC 1F to be gated by the Drive Select signal to produce a low output at Pin 8 of the interface connector.

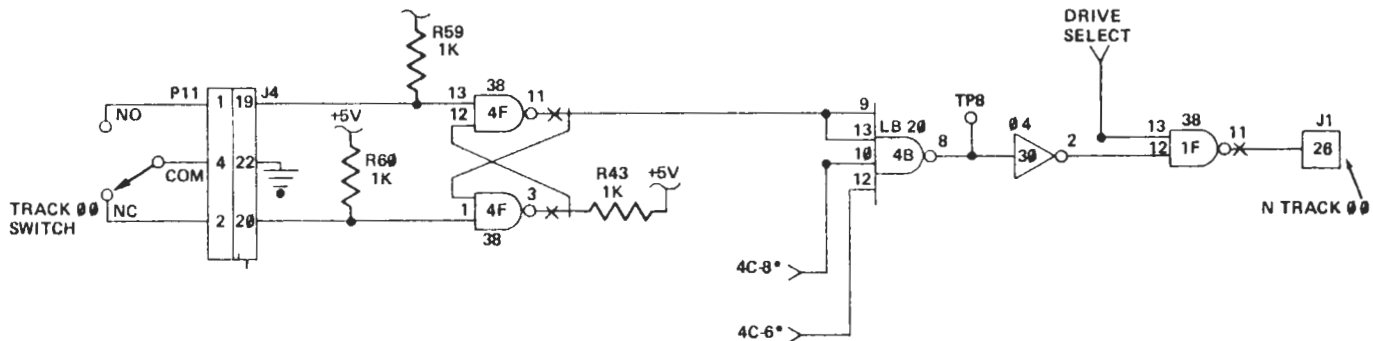


### 3.3.2.2 Track 00 (N TRK 00)

#### Functional Description

When the disk drive is selected, the Track 00 Interface signal indicates, to the controller, that the read/write head is positioned at Track 00. The Track 00 signal remains true (low) until the head is moved away from Track 00. The Track 00 switch usually is deactivated between Track 1 and Track 2.

Test Point 8 (see Figure 3-11) is true (low) when the carriage is positioned at Track 00 and the Step Motor phase is correct.



\*4C-8 and 4C-6 are high on Phase 0 only.

Figure 3-11  
Track 00 Schematic Diagram

#### Circuit Description

The Track 00 switch is internal to the disk drive. Its signal comes in on Connector 11. 4F is a latch that debounces the switch noise. The Track 00 switch is activated between Track 00 and Track 3. The combination of the Track 00 switch being activated and the proper stepping motor phase (Phase 0), produces all "high" signals at IC 4B, Pins 9, 10, 12, and 13. This signal subsequently is buffered through IC 3D, Pin 1 and Pin 2. IC 1F Pins 11, 12, and 13 gate the Track 00 output with the disk drive select output, to give a Track 00 output to the controller at Pin 26 of the interface connector.

### 3.3.2.3 Write Protect (N WRITE PROTECT)

#### Functional Description

When the disk drive is selected and the diskette is write protected, the Write Protect signal line logic level goes true (low). The write electronics are internally disabled when the diskette is write protected.

It is recommended that the Write data line be inactive whenever Write Enable is false, i.e., in a Read state, J1, Pin 24.

When the level on this line is false (high), the write electronics are enabled and the write operation can be performed. It is recommended that the controller not issue a Write command when the Write Protect signal is true (low).

When a write protected diskette is installed in the disk drive, Test Point 9 (see Figure 3-12) is high.

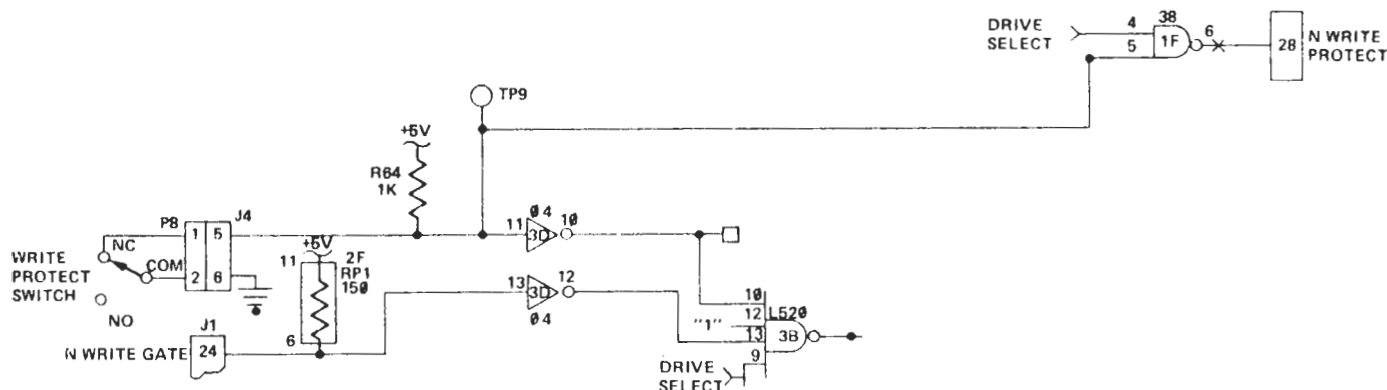


Figure 3-12  
Write Protect Schematic Diagram

### Circuit Description

The Write Protect signal comes in at Connector 8. Test Point 9 is held low when the switch is closed by a non-write protected diskette. The Write Protect output at Pin 28 of the interface is enabled at IC1F, Pins 4, 5, and 6, by the Drive Select signal.

### 3.3.2.4 Read Data (N READ DATA)

#### Functional Description

The Read Data interface line transmits the readback data to the controller when the disk drive is selected. It provides a pulse for each flux transition recorded on the media. The Read Data output line goes true (low) for a duration of one (1) usec for each flux change recorded.

The leading edge of the Read Data output pulse represents the true positions for the flux transitions on the diskette surface.

Test Point 1 and Test Point 2 (see Figure 3-13) are provided to observe the differential output of the first stage of Read signal amplification. Test Point 3 and Test Point 4 are provided to observe the differential output of the second stage amplifier and differentiated Read signal. Test Point 5 is the output of the single shot used in the Read section, nominally 1.0 usec for each flux transition detected. Test Point 10 is signal ground.

#### Circuit Description

The read signal comes from the selected head on the disk drive. It is gated to the first amplifier (IC 3A) by the N WRITE signal to IC 2B, Pin 11 and Pin 10, which forward-biases diodes CR11 and CR12. Then the Read signal passes through C2, L1, L2, C3, C4, and C5, which is a bandpass filter. The Read signal is then at the input IC 4A, the differentiator, which is also Test Point 1 and Test Point 2.

The output of IC 4A goes through DC blocking capacitors C7 and C8 to the crossover detector, IC 5B, which digitizes the AC signal. This puts the signal into a standard TTL format. IC's 5D, 5E, and 5C comprise a comparator circuit. Any pulses that occur outside of the normal duty cycle of IC 5B are eliminated. IC 5D is an edge detector. IC 5E acts as a one-shot. IC 5C is the actual comparator.

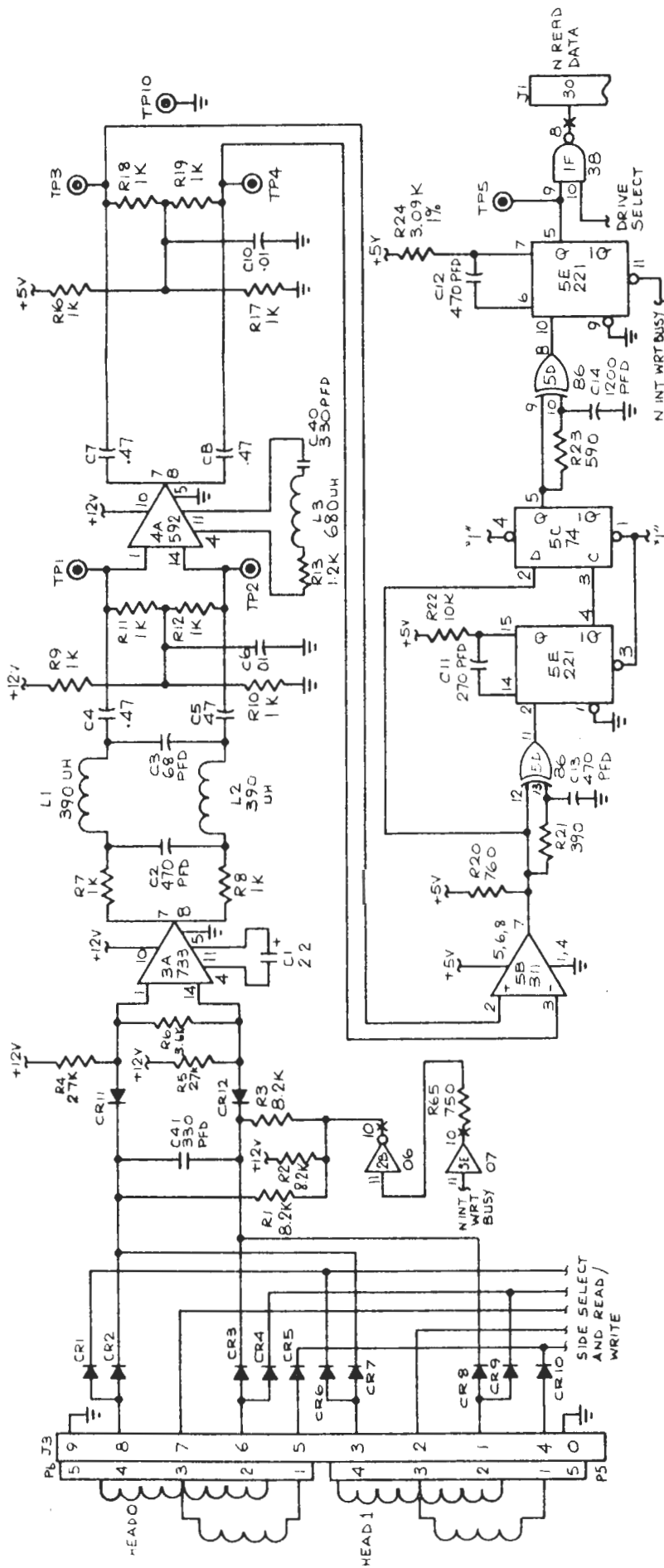


Figure 3-13  
Read Data Schematic Diagram

The Read signal is presented to IC 5D, which is another edge detector, and then goes to IC 5E, where the pulses are shaped to 1 usec. This output is gated at IC 1F with the Unit Select signal to produce a digital output at Pin 30 of the interface connector (see Figure 3-14).

NOTE

IC 5E, the final one shot, is enabled only when the disk drive is in a Read state (Pin 11).

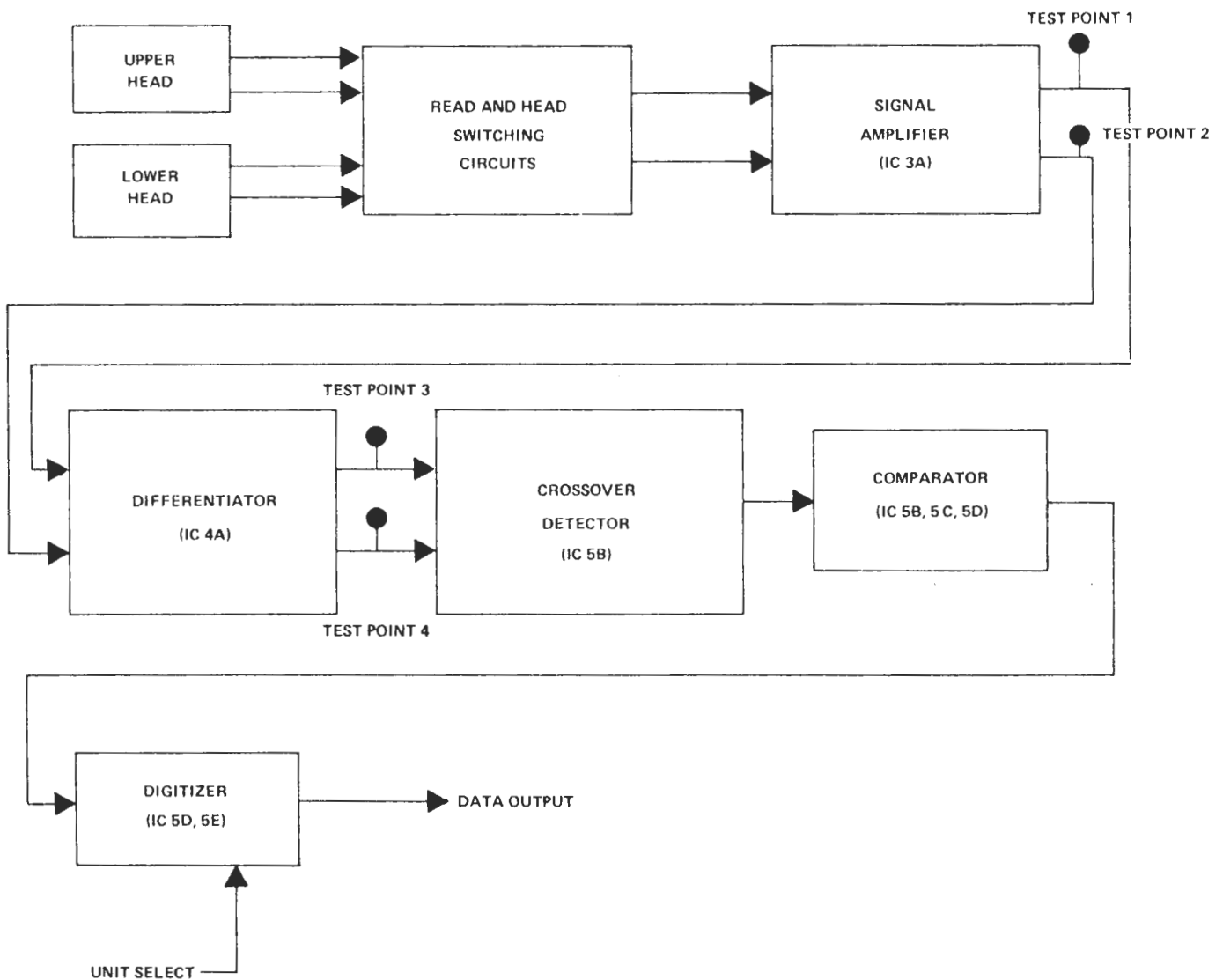


Figure 3-14  
Read Circuit Block Diagram

### 3.4 PHYSICAL DESCRIPTION OF THE SERVO PCBA

The Servo PCBA is approximately 127 mm (5.0 inches) long by 38 mm (1.5 inches) wide. Figure 3-15 illustrates the placement of test points and connectors.

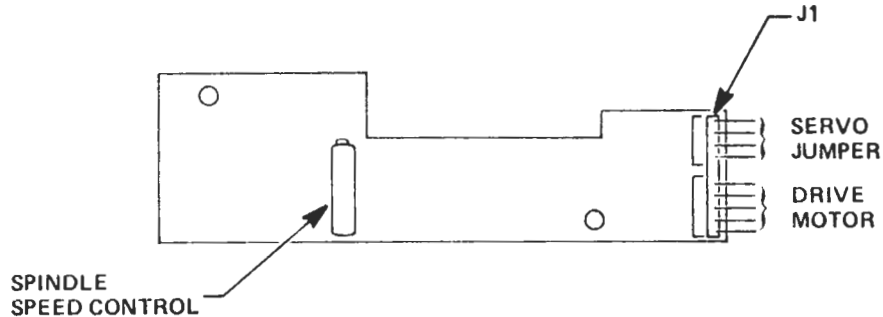


Figure 3-15  
Servo PCBA

#### 3.4.1 Input Control Lines

##### Functional Description

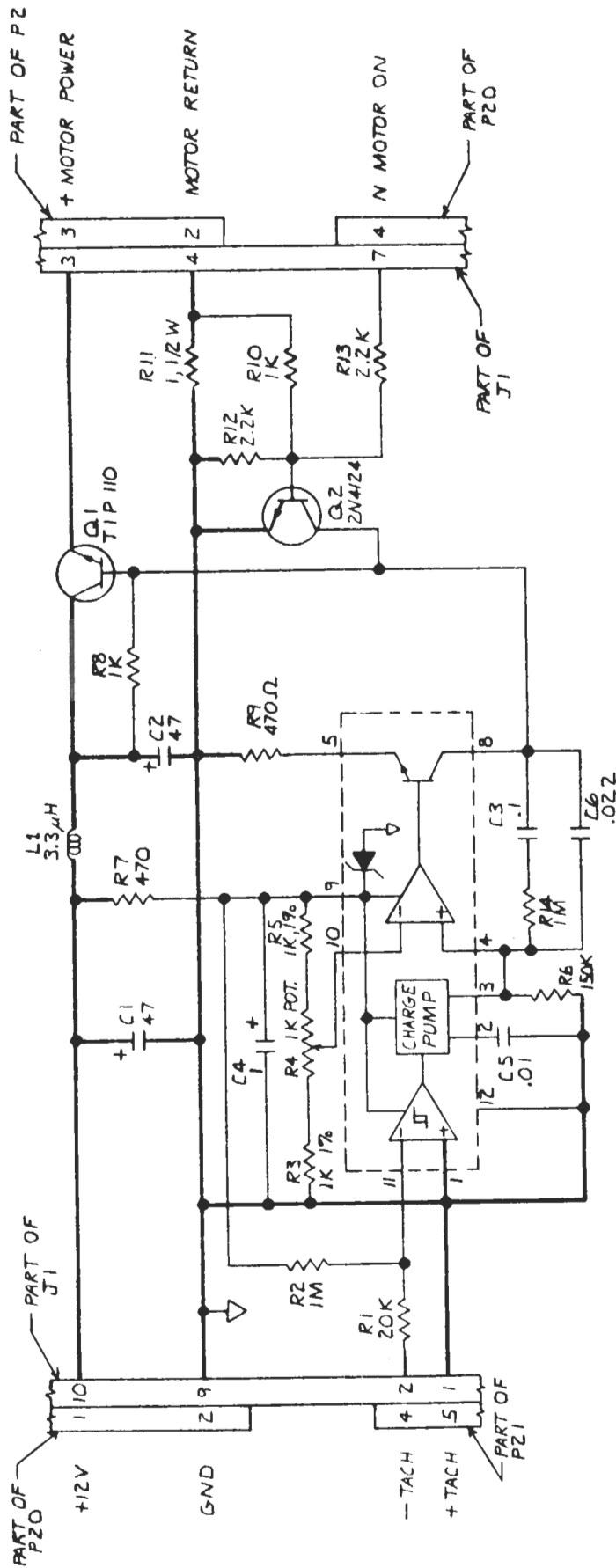
When the logic board receives a true (low) Motor On signal, a true (low) signal is sent to the servo board (N MOTOR ON) (see Figure 3-16). This signal turns on the regulator (Q1), and the motor's speed accelerates to 300 rpm ( $\pm 1.5\%$ ).

R4 is adjusted for a motor speed of 300 rpm.

The motor supplies a 12-volt AC tachometer signal to the servo board for regulation control.

##### Circuit Description

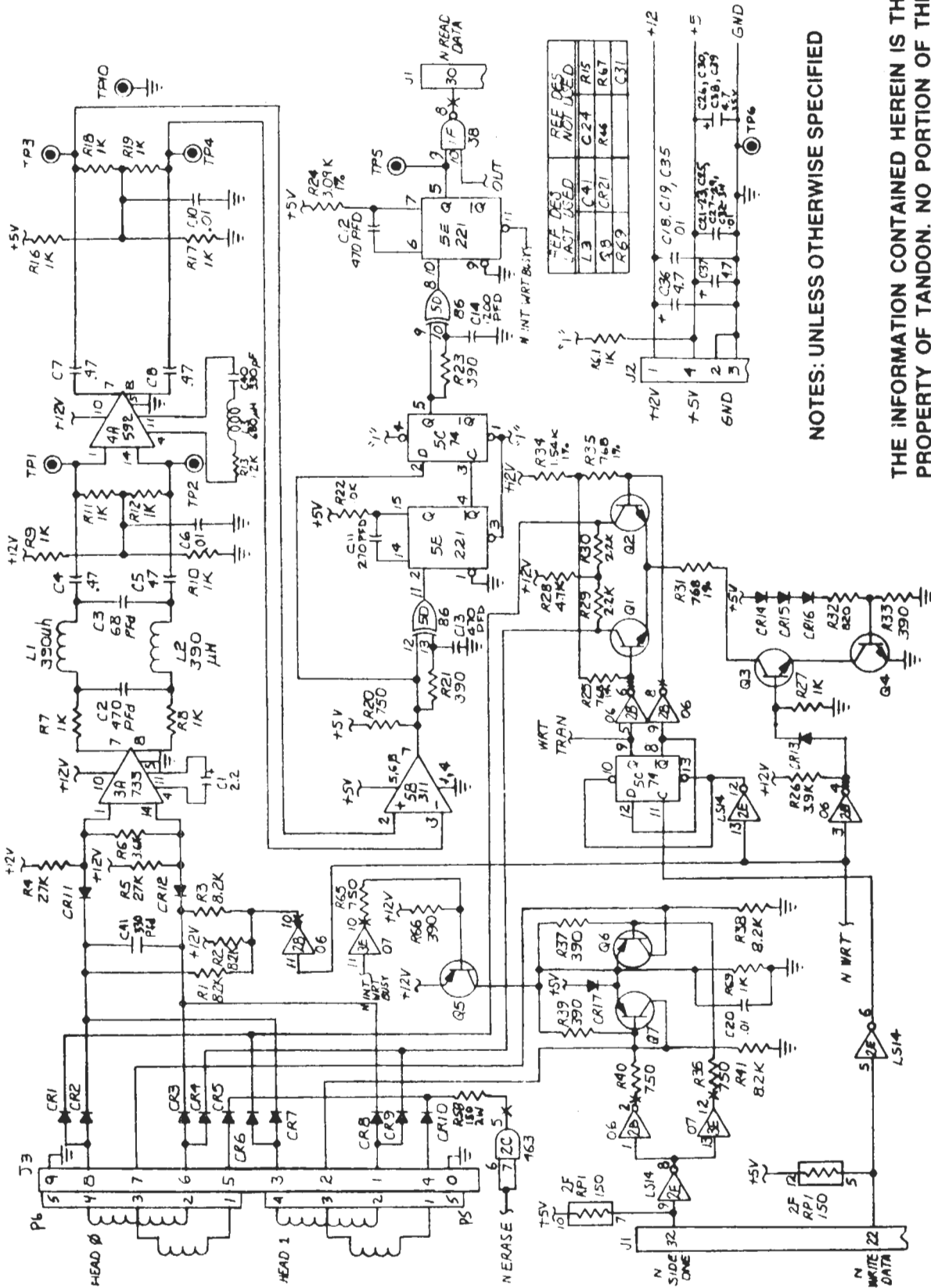
The Motor On signal comes in at Pin 7 of the servo board (see Section 3.3.1.2). This turns off Q2, allowing the signal to be sent to the base of Q1. The signal to the base of Q1 is the output of the regulator IC Pin 8. This is controlled by the tach input at Pin 1 and Pin 2 of the servo board. The tach signal is an AC signal of twelve (12) volts. The other input to the regulator is from the voltage divider R3, R4, and R5. This voltage is adjustable by R4, a potentiometer, to produce the proper amount of current through Q1 to the drive motor.



- NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTORS ARE IN OHMS, ±5%, 1/4 W.
  2. 1% RESISTORS ARE 1/8 W.
  3. CAPACITORS ARE IN μF, ±20%, 35V.

THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF TANDON. NO PORTION OF THIS DATA SHALL BE RELEASED, DISCLOSED, USED, OR DUPLICATED. FOR USE IN PROCUREMENT OR MANUFACTURING WITHOUT SPECIFIC, WRITTEN PERMISSION FROM TANDON.

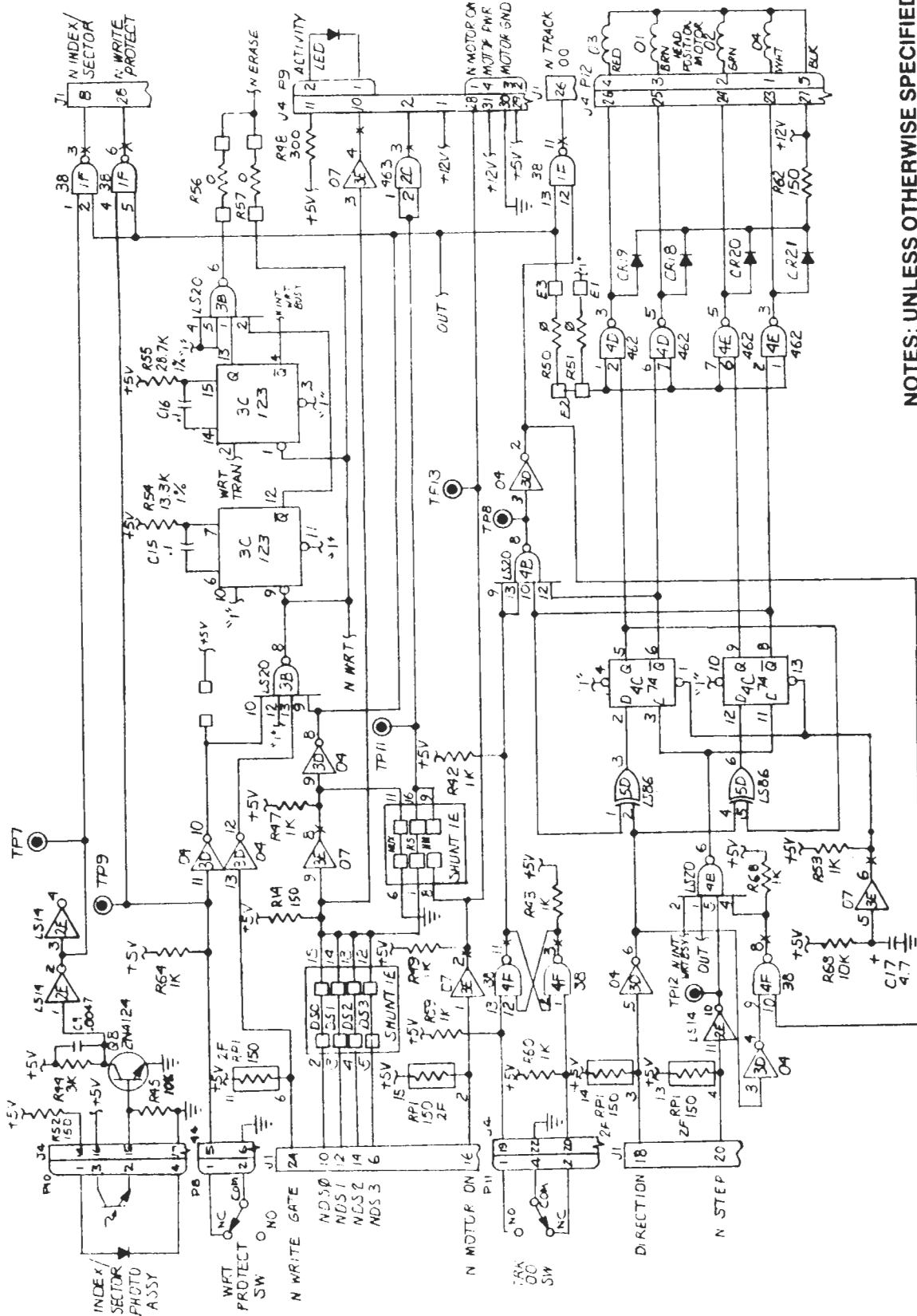
Figure 3-16  
Servo Board Schematic Diagram



NOTES: UNLESS OTHERWISE SPECIFIED

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LOGIC SCHEMATIC



NOTES: UNLESS OTHERWISE SPECIFIED

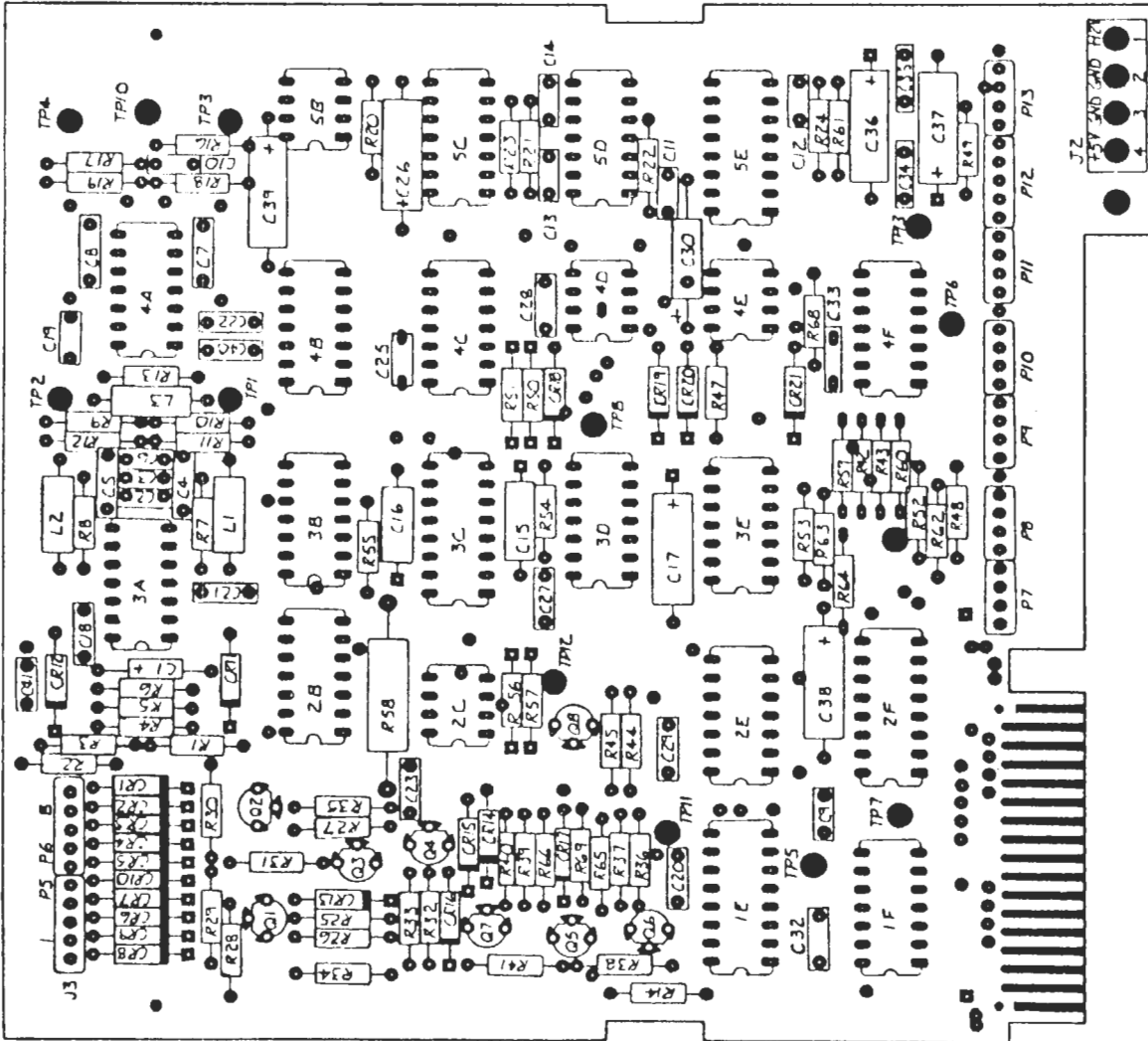
1. ALL RESISTORS ARE IN OHMS, 1/4 W, 5%
2. ALL CAPS ARE IN µFD.
3. ALL DIODES ARE IN 4446.
4. ALL TRANSISTORS NPN ARE 2n4124 & PNP ARE 2N4125.

### LOGIC SCHEMATIC

THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF TANDON. NO PORTION OF THIS DATA SHALL BE RELEASED, DISCLOSED, USED, OR DUPLICATED, FOR USE IN PROCUREMENT OR MANUFACTURING WITHOUT SPECIFIC, WRITTEN PERMISSION FROM TANDON.

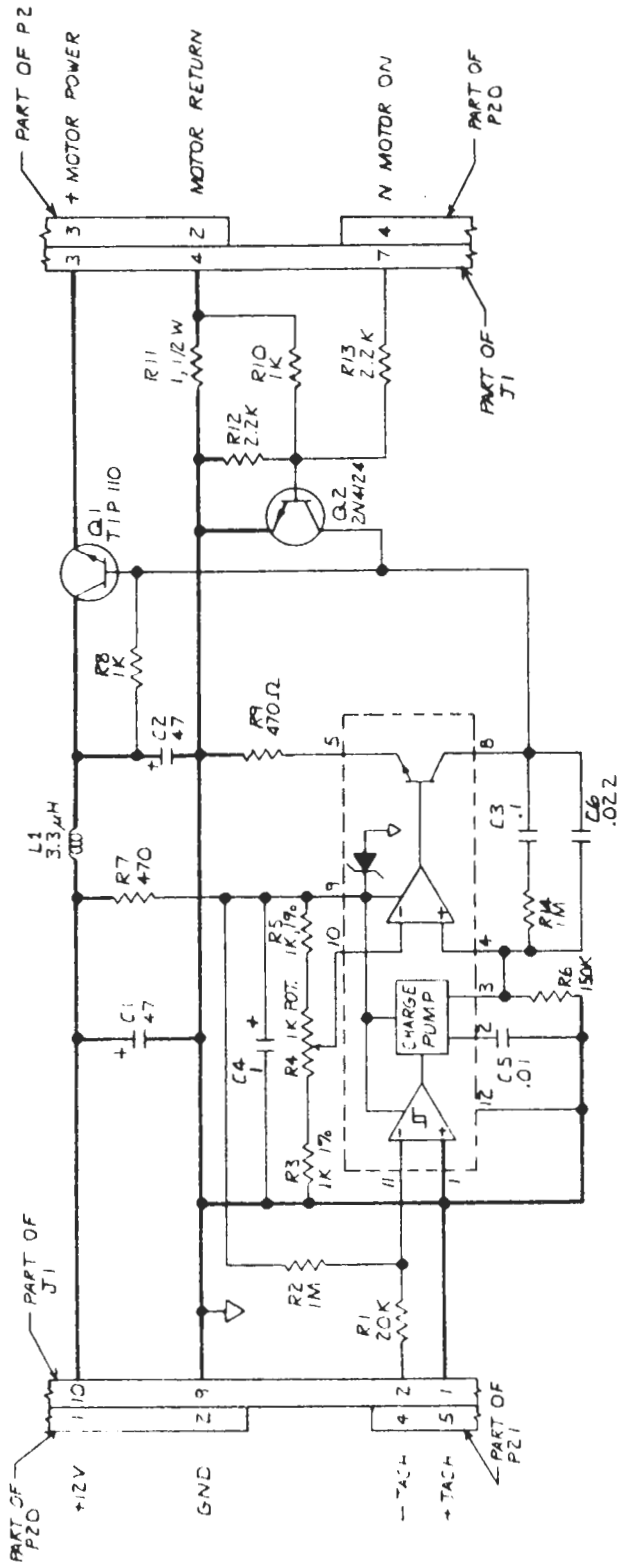


THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF TANDON. NO PORTION OF THIS DATA SHALL BE RELEASED, DISCLOSED, USED, OR DUPLICATED, FOR USE IN PROCUREMENT OR MANUFACTURING WITHOUT SPECIFIC, WRITTEN PERMISSION FROM TANDON.



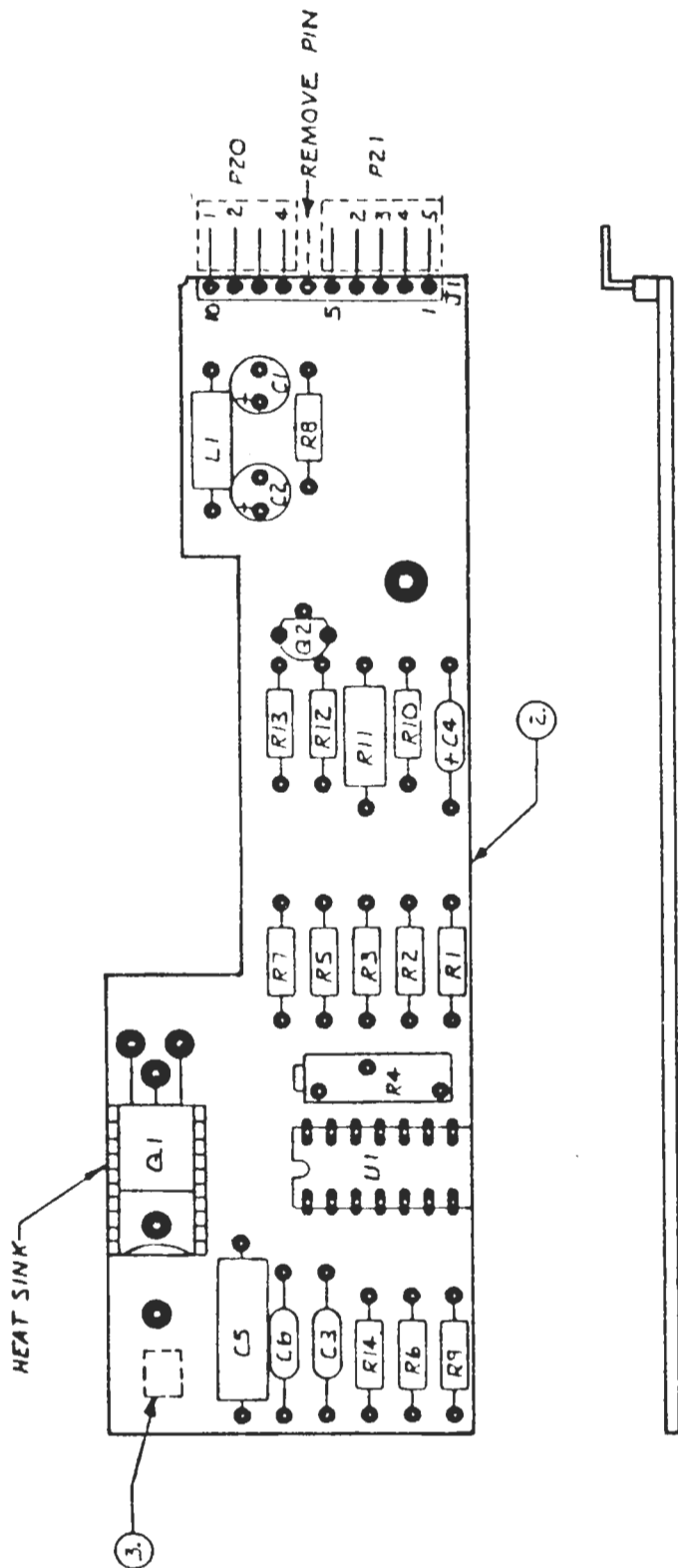
- NOTES: UNLESS OTHERWISE SPECIFIED
1. COMPONENT HEIGHT NOT TO EXCEED .35 ABOVE P.C. BOARD.

### LOGIC PCBA ASSEMBLY DRAWING



**SERVO PCB A,  
LINEAR**

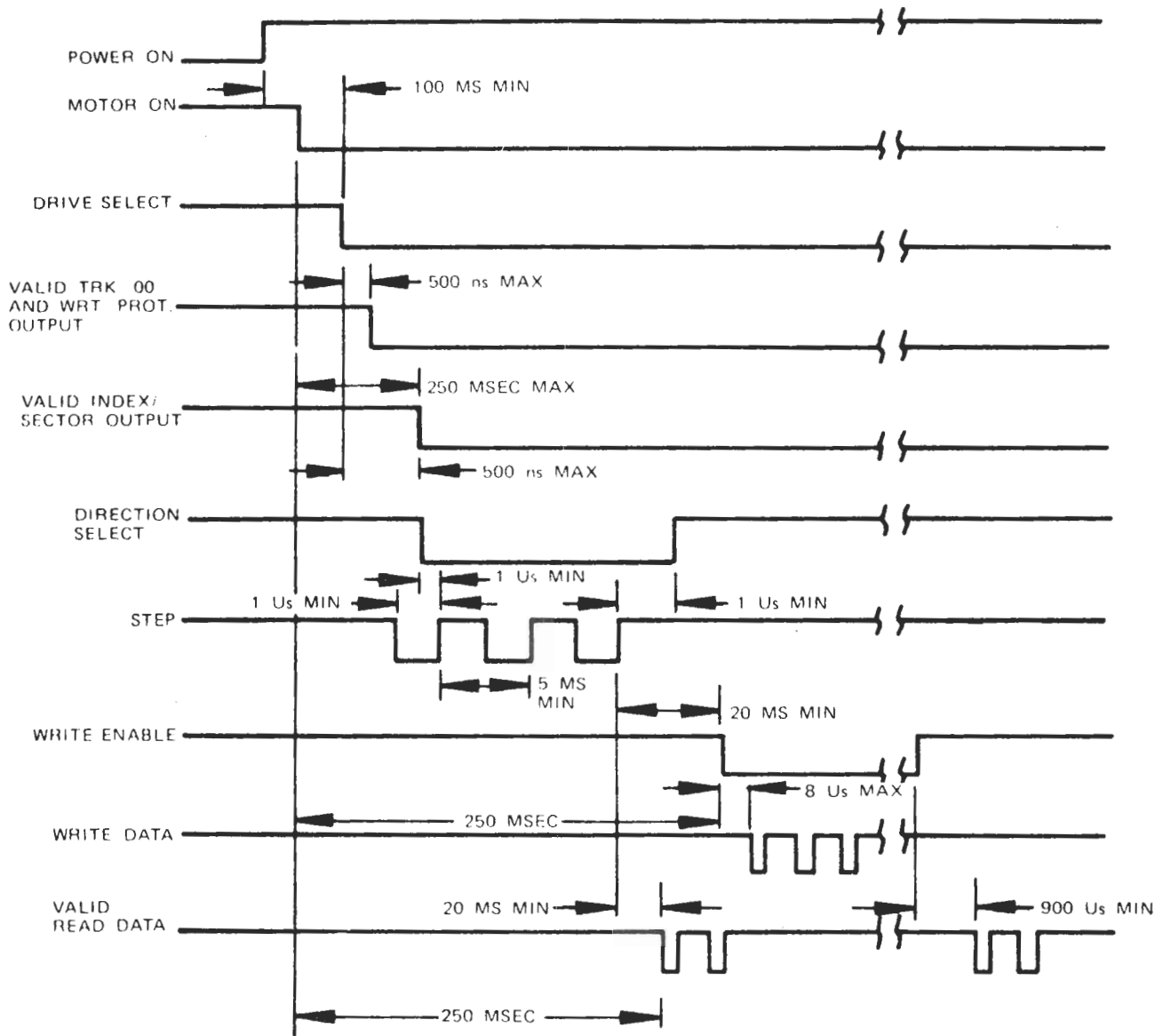
- NOTES: UNLESS OTHERWISE SPECIFIED**
1. RESISTORS ARE IN OHMS,  $\pm 5\%$ , 1/4 W.
  2. 1% RESISTORS ARE 1/8 W.
  3. CAPACITORS ARE IN  $\mu\text{F}$ ,  $\pm 20\%$ , 35 V.



- NOTES: UNLESS OTHERWISE SPECIFIED
1. ASSEMBLE PER STANDARD MANUFACTURING METHODS.
  2. THIS ASSEMBLY SHALL BE MADE FROM PCB DETAIL 178901-001, REVISION A.

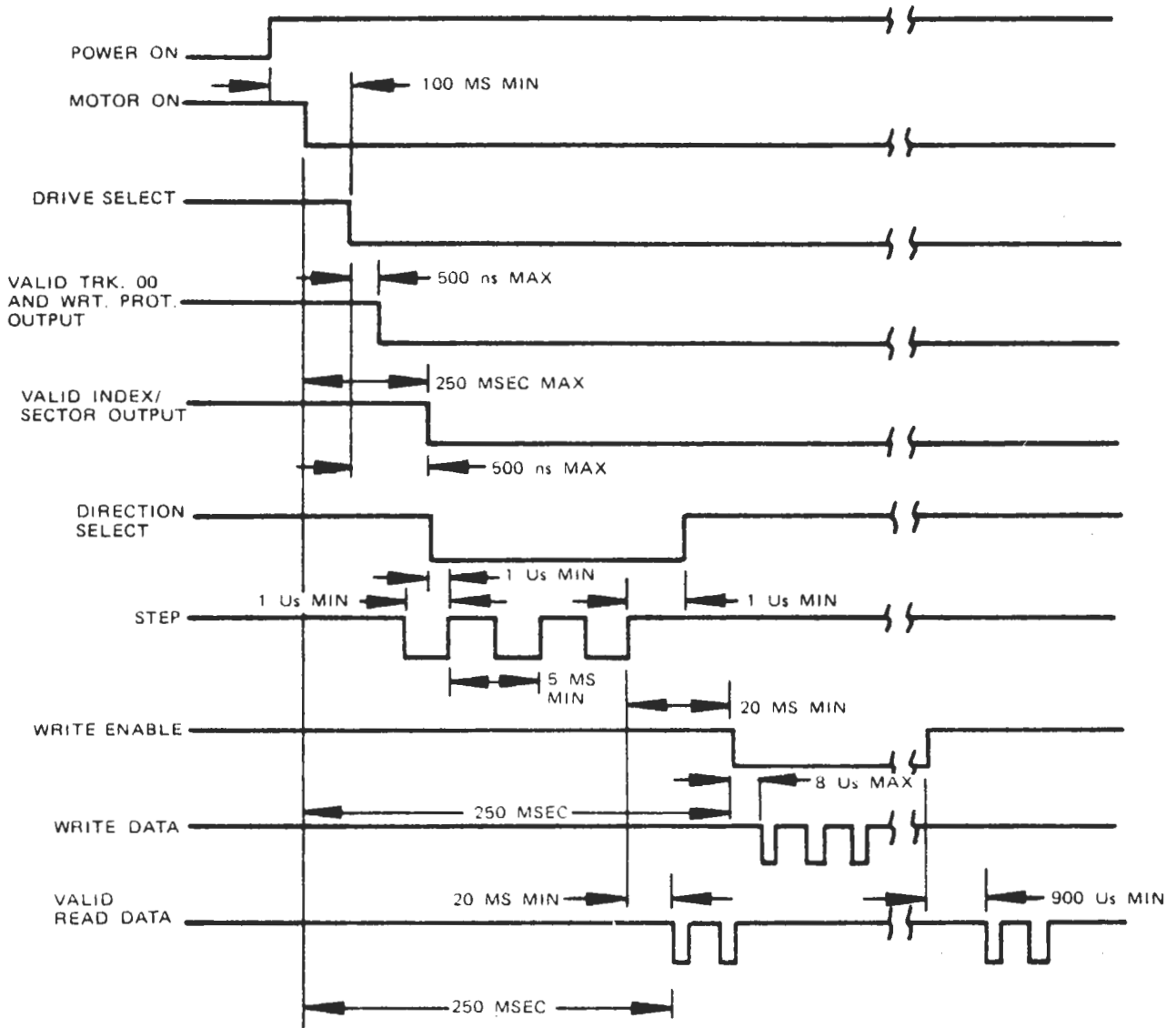
THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF TANDON. NO PORTION OF THIS DATA SHALL BE RELEASED, DISCLOSED, USED, OR DUPLICATED, FOR USE IN PROCUREMENT OR MANUFACTURING WITHOUT SPECIFIC, WRITTEN PERMISSION FROM TANDON.

**SERVO PCBA,  
LINEAR**



MODEL TM-100 GENERAL CONTROL AND DATA TIMING REQUIREMENTS

**MODEL TM-100-1  
PRODUCT SPEC.**  
MINI SINGLE-SIDED RECORDING  
FLEXIBLE DISK DRIVE

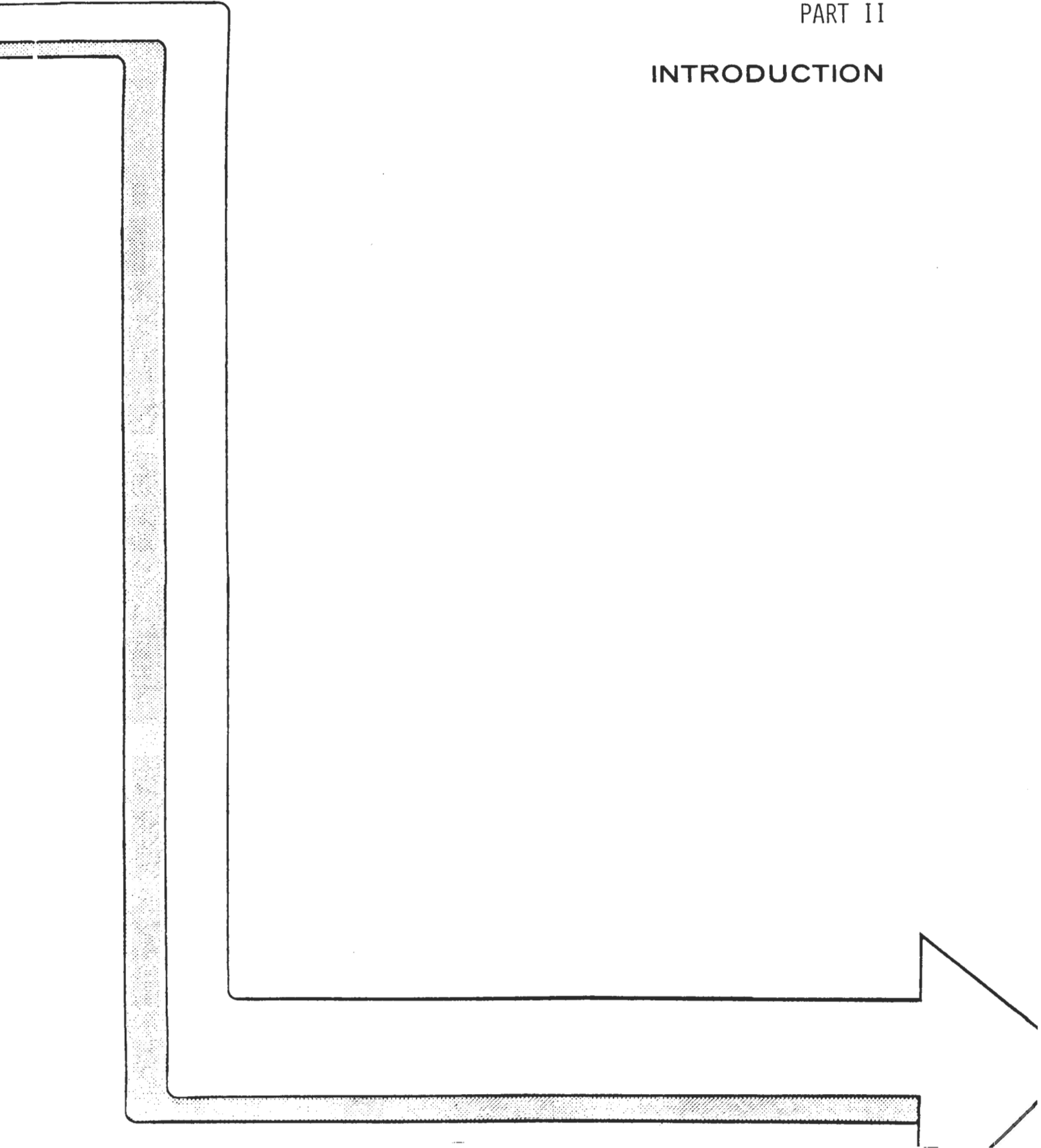


MODEL TM-100 GENERAL CONTROL AND DATA TIMING REQUIREMENTS

**MODEL TM-100-2**  
**PRODUCT SPEC.**  
 MINI DOUBLE-SIDED RECORDING  
 FLEXIBLE DISK DRIVE

PART II

INTRODUCTION





The H-207 is a floppy disk controller board. It functions as an intelligent interface between the CPU and the disk drives. The H-207 selects the correct drive in a multi-drive system and properly handles data transfer to and from the disk drives.

The H-207 operates as a slave processor. This means the disk controller board contains its own processor which is controlled by the master CPU. Thus, the disk controller board takes commands from the master CPU and converts them into the necessary signals required to control the drives. This type of system allows the master CPU to do other tasks while the disk controller board processor actually does the work of controlling the disk drives.

The H-207 is versatile. It can support up to four 5-1/4" and four 8" disk drives. User software selects the type of drive used and the density of the media. However, present Heath Company software limits the number of drives to three.

The H-207 can be operated in three different modes; Wait State, Polled I/O, or Interrupt. This allows the disk controller board to support almost all available soft-sectored disk formats. By using the Wait State mode, the board can be jumpered to operate at speeds up to 6 MHz.

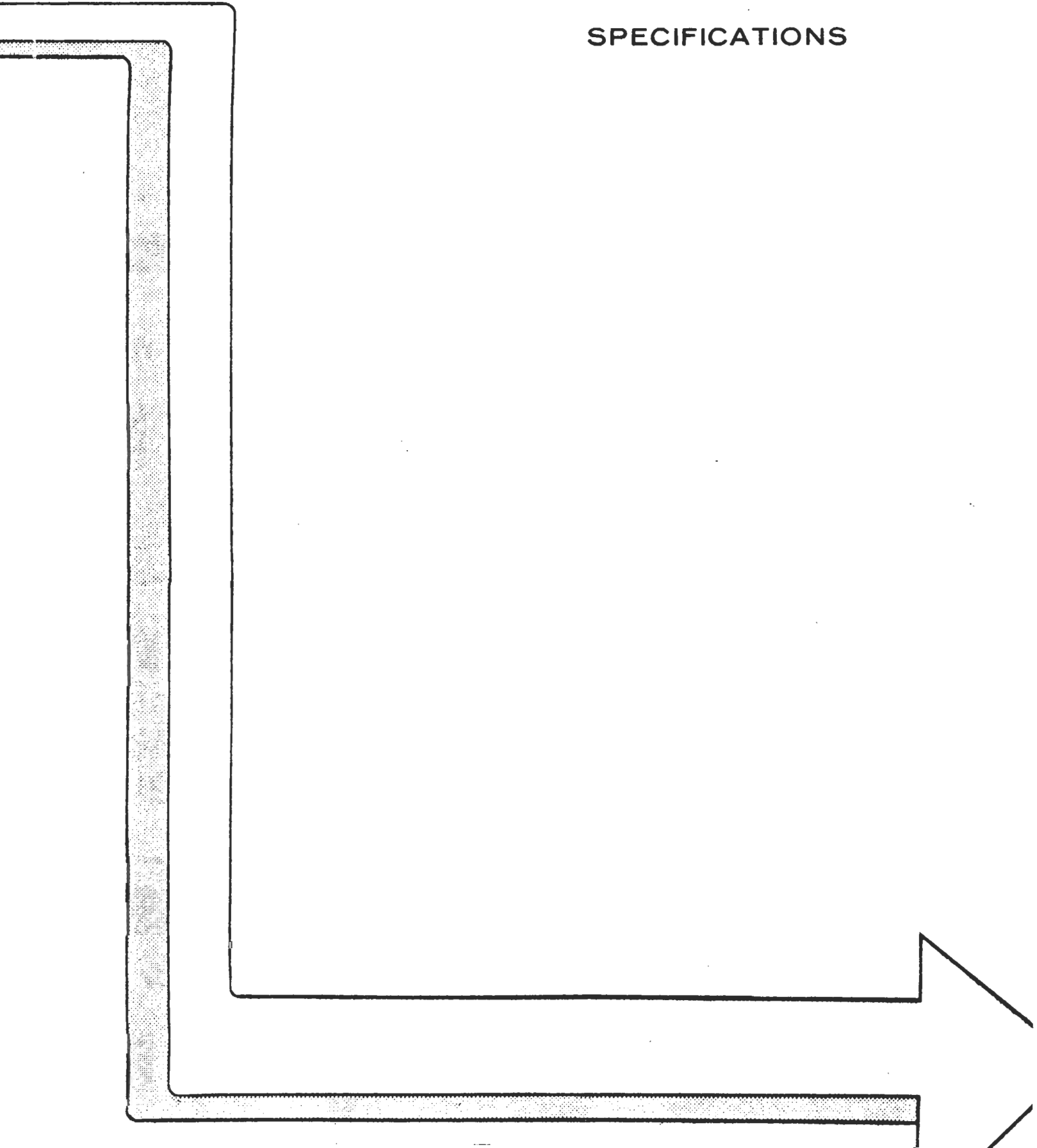
Because the H-207 is a IEEE 696 Standard S-100 compatible card, it can be installed in other makes of computers using the IEEE Standard. Additional features that make the controller board acceptable to other computers are: user selectable addressing, software controllable formatting, Shugart compatible 8" interface, and adjustable precompensation.

The information provided in this section of the manual will familiarize you with the operation and troubleshooting of the H-207. Using this information, you will be able to troubleshoot the disk controller board to the component level.





# SPECIFICATIONS





Type ..... WD1797.

Drives Supported ..... Up to four each.

5-1/4" ..... Single/double-sided, 48/96  
TPI, single/double density.

Capacity (formatted) ... 80K, 160K, 320K, or 640K;  
depending on the number of  
sides and density.

Track Format ..... 4K, eight sectors of 512 bytes  
each.

Stepping Speed ..... 6 milliseconds per track or  
faster.

8" ..... Single/double-sided,  
single/double density.

Interface type ..... Shugart 850 or equivalent.

Data Separator ..... Phase-locked loop.

Precompensation ..... Variable independently for  
both 5-1/4" and 8" sizes.

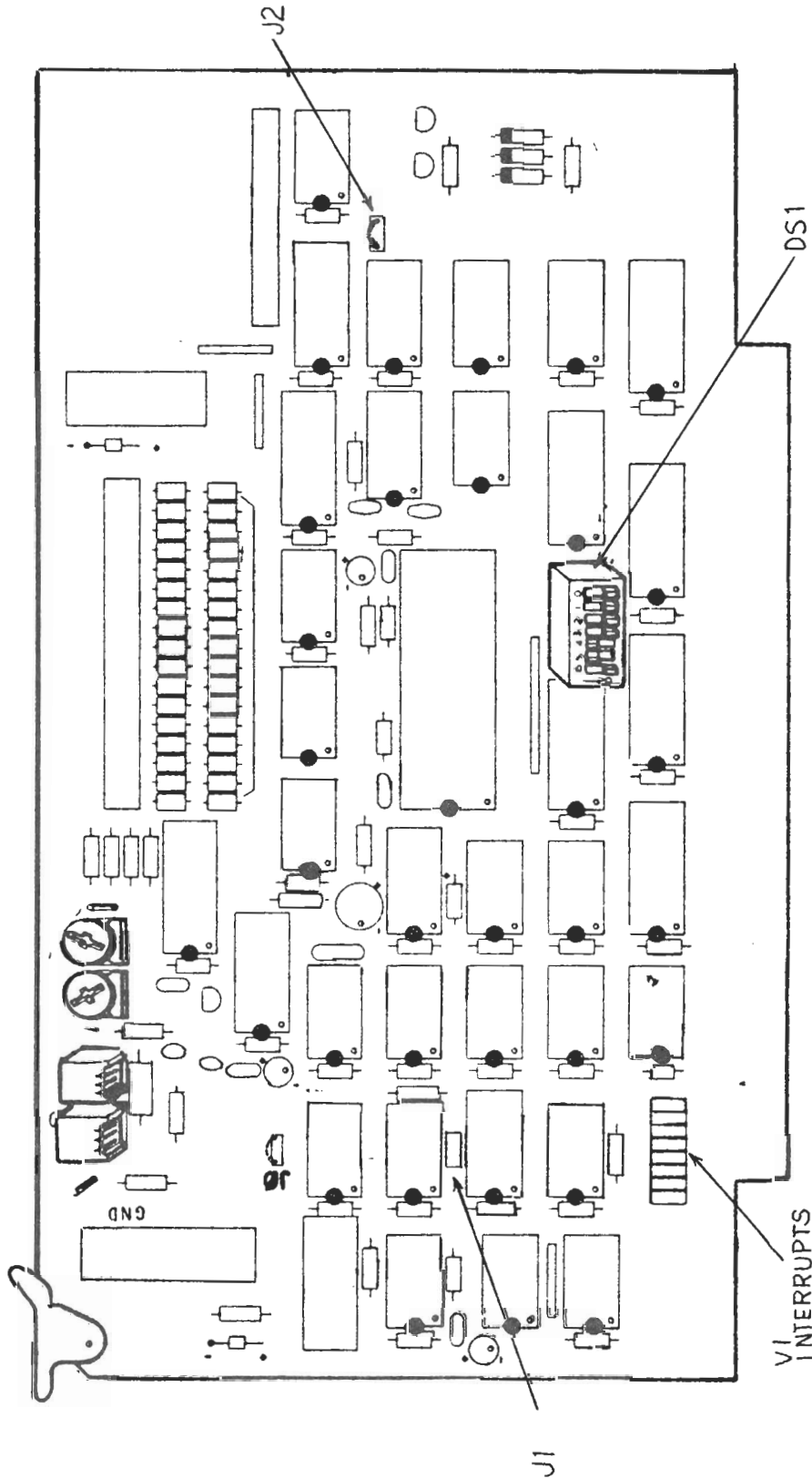
Data Transfer ..... Programmed using wait states,  
interrupt or polling.

*The Heath Company reserves the right to discontinue products and to change specifications at any time without incurring any obligation to incorporate new features in products previously sold.*



## OPERATION

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8" Disk Drive Connector	5-124



H-207 CONTROLLER BOARD

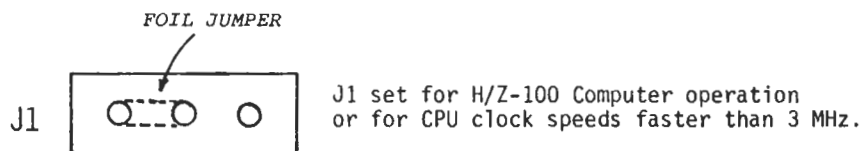
JUMPER AND SWITCH LOCATIONS

## INTRODUCTION

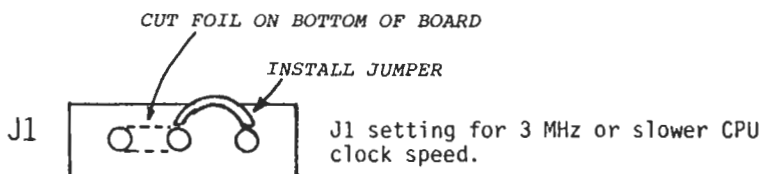
To permit the H-207 to operate in many different types of computers, a number of jumpers and a slide switch are incorporated into the design of the board. These devices permit configuring the controller board for the computer environment in which the H-207 is installed. There are three main areas of concern: clock speed jumpering, selection of interrupt jumpers and the setting of the slide switch, DS1. Refer to the pictorial on the adjacent page for the location of the jumpers and the slide switch.

## CLOCK SPEED

The host computer clock speed that the H-207 will operate with is determined by the jumpering at J1. As received, J1 is jumpered by a foil run on the bottom of the board. (See illustration below.) This jumpering enables the H-207 to operate in computers that have a CPU clock speed faster than 3 MHz. This jumpering is normal when the H-207 is installed in a H/Z-100.



For the H-207 to operate in a computer that has a CPU clock speed at or slower than 3 MHz, the jumpering of J1 must be altered. This is accomplished by cutting the foil jumper on the bottom of the circuit board and installing a 1" wire jumper from the middle hole of J1 to the rightmost hole. Refer to the illustration below when performing this alteration.

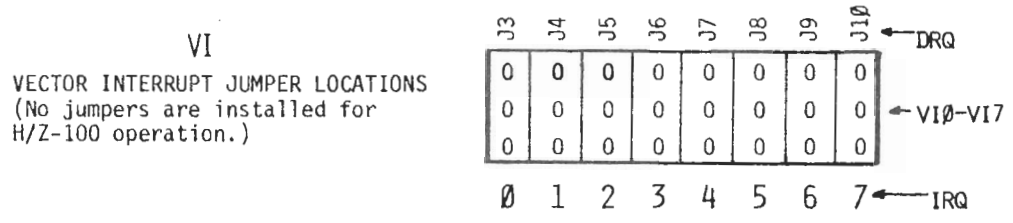




### INTERRUPT JUMPERS

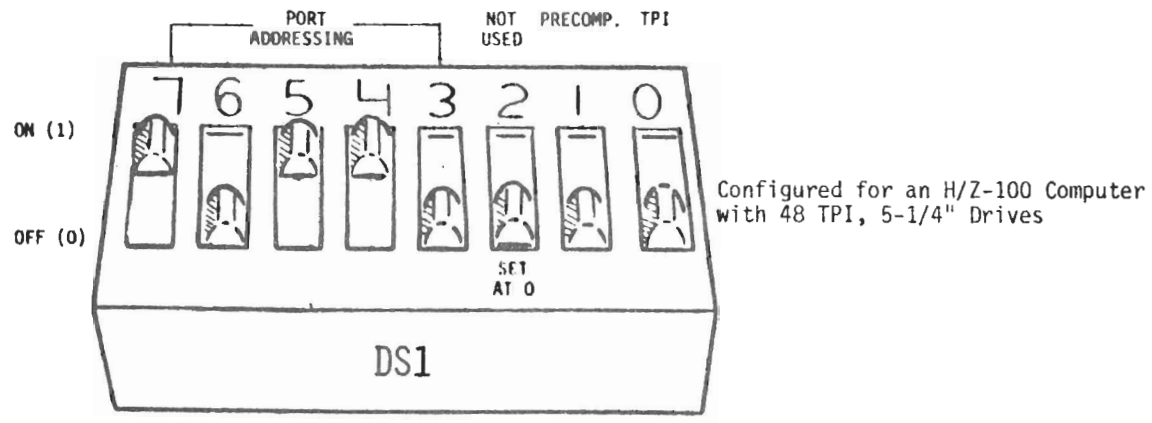
The Vectored Interrupt jumper locations, VI, are located on the lower left-hand corner of the controller board. The data request line, DRQ, from the 1797 is connected to holes J3 through J10 shown in the illustration below. The center row of holes numerically correspond with the S-100 interrupt lines VI0 through VI7. The interrupt request line, IRQ, from the 1797 is connected to holes 0 through 7. When jumpered, these locations route IRQ and/or DRQ from the 1797 controller to the S-100 interrupt lines.

No jumpers are installed in these locations when the H-207 is used in a H/Z-100. These jumper locations are only used when the H-207 is installed in computers that require interrupt protocol. The configuration of the jumpers is determined by the customer's computer documentation.



### SLIDE SWITCH (DS1)

DS1, an 8-section slide switch, determines the port address and the condition of bits 3 and 4 of the status port. The sections of DS1 are defined as follows:



## DS1

HEATH SOFTWARE DEFINED		HARDWARE DEFINED	
Section	Definition	Section	Definition
0	This bit determines the TPI of the 5-1/4" disk drive.  0 = 48 TPI. 1 = 96 TPI.	0	Status port bit 4.
1	This bit determines whether precomp is on or off.  0 = precomp off. 1 = precomp on.	1	Status port bit 3.
2	Not used.	2	Not used. Leave at 0.
3-4-5-6-7	Port addressing.	3-4-5-6-7	Port addressing (MSB).

The H-207 occupies a block of eight contiguous I/O port addresses. The three low-order bits in this block select 1797 registers, the control latch, or the status port. The H/Z-100 computer series place the H-207 at port address BOH. A map of the I/O port is shown below.

I/O ADDR. (Binary)	READ	WRITE	PORT DESIGNATION
SSSS000*	•		1797 Status Register
SSSS000		•	1797 Command Register
SSSS001	•	•	1797 Track Register
SSSS010	•	•	1797 Sector Register
SSSS011	•	•	1797 Data Register
SSSS100		•	Control Latch
SSSS101	•		Status Port

\* S = dip switch bit

The dip switch bits are simply defined from the binary equivalent of the switches. For example, the port address for the H/Z-100 is shown below.

SSSSXXX\*\* = 10110XXX = Port B0 - B7.

\*\* X = 1797 register, control latch, or status port.

## OUTPUT CONNECTORS

### 5" DISK DRIVE CONNECTOR (P2)

This 34-pin connector provides the necessary signals to drive a 5-1/4" disk drive. Refer to the pictorial at the left for a description of the pinouts of this connector. All numbered pins are grounded.

6	DS3
8	INDEX
10	DS0
12	DS1
14	DS2
16	MOTOR
18	DIR
20	STEP
22	WRDATA
24	WG
26	TK0
28	WPRT
30	RDD
32	SIDE 1

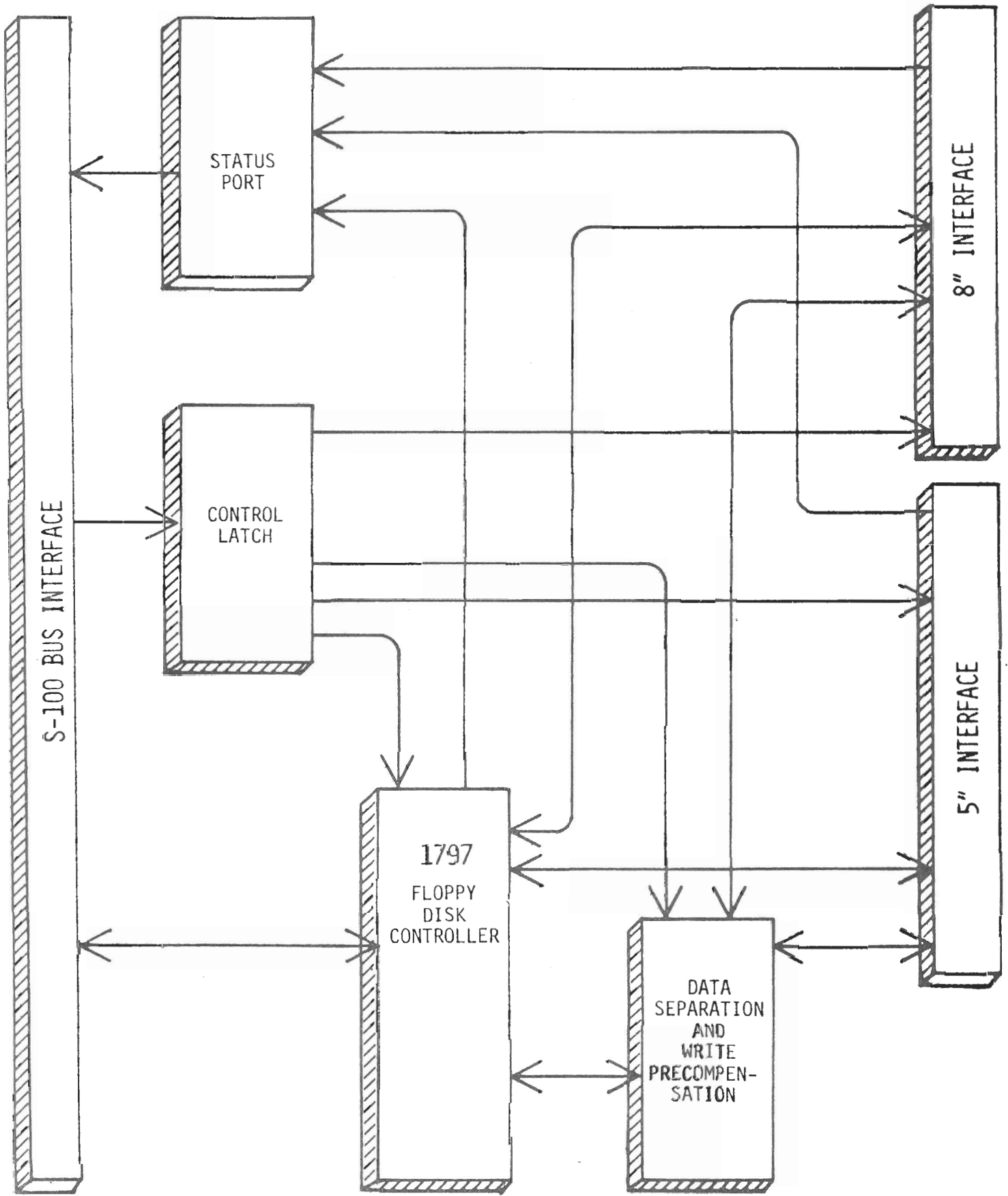
### 8" DISK DRIVE CONNECTOR (P1)

This 50-pin connector provides the necessary signals to drive an 8" Shugart compatible disk drive. Refer to the pictorial at the left for a description of the pinouts of this connector. All odd numbers pins are grounded.

2	TG43
10	TWO SIDED
14	SIDE 1
18	HEADLOAD
20	INDEX
22	RDY
26	DS0
28	DS1
30	DS2
32	DS3
34	DIR
36	STEP
38	WRDATA
40	WG
42	TK0
44	WPRT
46	RDD

## CIRCUIT DESCRIPTION

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H-207 BLOCK DIAGRAM

## BLOCK DIAGRAM DESCRIPTION

Refer to the H-207 block diagram as you read the following.

The H-207 Floppy Disk controller board consists of seven major sections: the bus interface, the status port, the control latch, the 1797 floppy disk controller, the data separation & write precompensation circuits, and the two drive interfaces.

The bus interface is made up of two octal bus buffers, an octal tri-state latch, an address comparator, and some miscellaneous enabling circuitry. These components interface the H-207 to the S-100 bus in the H/Z-100.

The status port is a read-only device that tells the CPU the status of the disk drives and the controller. This includes track density, number of recording sides to the disk, and if precompensation is being used.

The control latch accepts commands to the disk drives such as DRIVE SELECT, 5" FASTEP, and others that have to do with the selection and mode of the drives.

The 1797 controller controls the placement of information on the diskette. That is, the movement of the drive head, the formation of written data, and the separation of the read data is controlled by the 1797.

The data separation and write precompensation circuitry control how the data is read to or written from the diskette. It does this by separating the data from the clock signal during read operations and precompensating data during the double-density write operations.

The 8" and 5.25" drive interfaces include buffers and filter circuitry. Up to four drives can be connected to each interface.

## DETAILED CIRCUIT DESCRIPTION

### S-100 BUS INTERFACE

The S-100 Bus Interface is compatible with any IEEE 696-standard S-100 Bus. See the S-100 specification sheets in the appendices of this manual for definitions of the lines.

#### DATA IN

Data into the bus (out from the controller board) travels through signal lines 91-95 and signal lines 41-43 on the bus interface. These pins are used in read operations from the status latch or from the 1797 controller. The data is buffered from the board's internal data bus to the S-100 bus by means of U36, a 74LS244 buffer.

#### DATA OUT

Data out from the bus (into the controller board) travels through pins 35, 36, 38, 39, 40, 88, 89, and 90 on the bus interface plug. This data is latched by tri-state latch U35. The latch is used because data on the S-100 bus is not present long enough for the 1797 to receive properly. The tri-state latch holds the data on the board's internal data bus so that the 1797 can read it. Valid data is latched in U35 on every write cycle. The latch is enabled through pin 1 when the ALE (Address Latch Enable) signal latches an asserted sOUT (Status Out) signal via U20.

#### ADDRESS LINES

The address lines from the bus enter the board through pins 29, 30, 31, 79, and 80 through 83 of the bus interface. They are buffered by the 74LS244 chip, U34.

#### CONTROL LINES

The control lines from the S-100 bus enter the board through pins 24, 25, 45, 46, and 75 through 78 of the bus interface. These lines are buffered by U33.

## VECTOR INTERRUPT LINES

The vector interrupt lines from the bus enter the board at pins 4 through 11 of the bus interface. They may be driven by U32.

## READY LINE

The ready line, RDY, enters through pin 72 of the bus interface. It is driven by U32. The controller board uses this line to put the CPU in a wait state during some operations to give the controller time to finish the operation.

## RESET CIRCUITS

### POWER-UP/RESET

On power up, the CPU sends RESET\* through the S-100 bus to the H-207 board. This places the 1797 controller, the control latch, the write precompensation control, and the U26 flip-flops in a known state before the CPU accesses the board.

In the 1797, the reset line sets the command register at 03H, the sector register to 01H, and bit 7 of the status register (Not Ready bit) to logic zero.

After the reset line goes high, the 1797 executes the restore command. The drive read/write head seeks track 0 and sends an interrupt to the computer once the track is found. See the 1797 IC data sheets for more details.

The reset line connects to pin 1 of the control latch, U30, to clear all of the outputs.

The reset state of the phase lock loop control, U1, makes the phase four ( $\phi_4$ ) input equal to 0 (see the 1691 IC data sheets).

Finally, the U26 Q-outputs are made equal to 1; pin 9 sends an RDY (ready) signal to the CPU and pin 5 provides part of the qualification needed for read/write enabling through U27-11.



## POWER-UP WRITE PROTECTION

On power up, the TTL circuits will be at an undefined state until the power supply voltage rises above 4 volts. This could generate a write command in the drives and damage any disks that may be installed.

To protect the disk, the WG (write gate) output from the 1797 is coupled to the 5" and 8" drives through Q3 and Q2. These transistors are biased by R25, D3-D1, and R24 to remain cut off until the power supply voltage is at or above 4 volts. When the supply reaches this value, Q2 and Q3 are biased near their operating region and will conduct whenever WG is asserted.

## CPU/CONTROLLER LOGIC

Reading and writing in the H-207 board involves three types of information: data which can be read or written, status signals, and control signals. Status signals can only be read and control signals can only be written.

### READ STATUS LATCH (U31)

Assume a status signal needs to be read. There are two sources of status information for the S-100 bus, the status port at U31 and the 1797 status register in U22.

To read from the status port, the CPU selects the H-207 by placing the address of the board on the address lines, A0-A7. Lines A3-A7 are checked by the address comparator, U29, for the proper address. The proper address is defined by the user by setting DIP switch DS1. If the address is correct, the EOUT signal pin 19 asserts.

The EOUT signal is gated through U28-13 by I/O at pin 12. I/O asserts on a data transfer between the CPU and an I/O port. If I/O is low, indicating that the sINP signal or sOUT signal is asserted, then the simultaneous assertion of EOUT and I/O signals sends a logic one to U20-2. This logic one is latched onto pin 5 when ALE (address latch enable) asserts. ALE, derived from pSTVAL\* and pSYNC, goes high when the H-207 port address is stable.

The Q output of U20 is NANDed with pDBIN from the S-100 bus to form  $\overline{RDME}$  at U27-8. This line goes low to indicate that the H-207 board is being read by the CPU, and activates the status latch, U31-1.

The status latch still can not be read until the status port select line (STPS) is asserted at pin 15 of U31. This line comes from U17-14, the I/O address decoder.

The I/O address decoder activates STPS by decoding the address lines A0, A1, and A2. If A0 and A1 are low and A2 is high, and if BDSEL or board select is active, then U17's Y1 line goes low. This causes U31 to place the status word onto the board's internal data bus, where it is buffered by U36 to the S-100 bus.

The organization of the status latch is as follows:

BIT	SIGNAL NAME	FUNCTION	
0	INTRQ	0 = no interrupt request	1 = interrupt request from 1797
1	MOTORON (5")	0 = spindle motor not running	1 = spindle motor running
3	96TP1	0 = 5.25" drives are 48 TPI	1 = 5.25" drives are 96 TPI
4	PRECOMP	0 = 5.25" drives do not need precomp	1 = 5.25" drives need precomp
6	TWOSIDED	0 = 8" diskette not two sided	1 = 8" diskette two sided
7	DRQ	0 = not ready for data transfer	1 = ready for data transfer

#### READ STATUS REGISTER OF 1797 (U22)

Assume now that the 1797's status register is to be read. The procedure is the same as described previously, except that address lines A0, A1, and A2 are low. Because the address bits A0-A2 are different, the I/O address decoder, U17, does not enable the status latch, U31. Instead the status register of the 1797 is selected and read onto the data bus.

## WRITE CONTROL LATCH (U30)

The control latch, U30, is written at the falling edge of CLEN, which is the simultaneous assertion of pWR and the Y0 output of the I/O address decoder. The pWR signal comes directly from the CPU, and the Y0 signal occurs when A0, A1, and A2 are high, low, and high, respectively. The Y0 and pWR signals are ORed at U21-6 to form CLEN.

The organization of each bit in the control latch is as follows:

BIT	SIGNAL NAME	FUNCTION
0,1	DSA, DSB	00 = select drive 1 01 = select drive 2 10 = select drive 3 11 = select drive 4
2	8"/5"	0 = select 5.25" 1 = select 8"
3	DSEN	0 = deselect all drives 1 = select drive specified by bits 0, 1, and 2
4	PRECOMP*	
	5.25" DDEN	0 = precomp all tracks 1 = disable precomp
	8" DDEN	0 = precomp all tracks 1 = precomp tracks 44-76
5	5" FASTEP	0 = 1797 operates as specified by bit 2 1 = 1797 operates in 8" mode
6	WAITEN	0 = wait state enable 1 = wait state enable
7	SDEN	0 = double density 1 = single density

\*(Note: Precomp is disabled in single density.)

When the WAITEN bit in the control latch is asserted, a wait state is initiated on the next read or write of the data register. WAITEN couples through U23, U26, and U32 to the S-100 RDY line. RDY goes low to put the CPU in a wait state until the disk controller asserts DRQ at U22-38.

Upon DRQ becoming active, an additional delay is needed to fulfill the access time requirements of the 1797 Controller. The access delay and synchronization to the S-100 Bus are both accomplished by counting system clocks. An on-board jumper selects whether one system clock is counted (for systems with clocks up to 3 MHz) or two system clocks are counted (for systems with clocks up to 6 MHz). For operation at less than 3 MHz, jumper J1 (near U19) should be jumpered between F and G. For operation between 3 and 6 MHz, this jumper should be between F and E (normal position for the H/Z-100).

At the completion of the access delay, the wait state is cleared. RDY is asserted, and the CPU completes the read or write of the data register in the 1797. A RESET or an INTRQ signal also clears the wait state, so that the CPU does not hang up after an error during a disk access.

#### WRITE COMMAND REGISTER IN THE 1797 (U22)

The command register in the 1797 can be written when A0, A1, and A2 are all low. The FDWR signal at U22-2 is asserted when both FDEN and pWR\* are logic zero. The signal pWR comes directly from the CPU, while FDEN is a composite signal made up of FDSEL and U26-5. The output of U26-5 is the signal that starts the access of the 1797 controller at the end of the wait state.

## DATA READ/WRITE OPERATIONS

During a data write operation, the controller board is enabled by the proper address and by pWR\*. After the proper control words are sent to select the proper drive, address lines A0 and A1 are made high and A2 is made low. This connects the data register of the 1797 to the internal data bus. As long as A0 and A1 are high and A2 and FDWR are low, the data from the S-100 bus will go to the 1797 data register and be shifted out serially on pin 31, the write output line. Also, on pin 31, clock pulses are inserted between each bit.

The track and sector registers in the 1797 determine where the data is to be written to on the disk. Whenever a sector is filled with data, software determines the next sector to be written to by making the A0 and A1 signals equal to 0 and 1, A2 equal to 0. Software then writes the sector number to the sector register and the track number to the track register.

The 1797 translates the track numbers into the proper step and direction commands to the drive.

A read operation requires the board to be enabled as described earlier. However, the I/O address decoder does not enable the status latch because the address provided by the CPU is not correct for a status read from the latch. Instead, the address lines causes the 1797 to dump the bits in its data register onto the internal data bus of the H-207, which connects to the U36 buffer and the S-100 bus.

The 1797 fills its data register from the data shift register, which fills serially from the RAWREAD data stream at U22-27. See "Data Separation and Precompensation" for a discussion on RAWREAD data processing.

## RDY DELAY

U19 is a quad flip-flop that acts as a delay line for the DRQ signal from the 1797 to the S-100 RDY line. The input at U19-4, D1, is output at Q1 after one clock cycle. Q1 is tied to D2 and is output to Q2 after another clock cycle. Q2 is also tied to U25-1 and D3.

From U25-12, the D2 signal presets flip-flop U26. Flip-flop U26 qualifies the FDSEL signal to enable read/write operations in anticipation of the RDY line being made active.

From D3 of U19, the delayed DRQ signal is output to Q3, which is connected to D4 and to jumper J1, post G. Post G is connected to post F in 3 MHz operations, which do not need additional delay of the DRQ signal. Instead, the output of Q4, which contains the DRQ signal delayed by three to four clock cycles, is connected to jumper J1, post E. For 6 MHz operation, J1 is connected between post E and post F.

## INTERRUPTS

There are two interrupts that the H-207 board can make. They are the interrupt request (INTRQ) and the data request (DRQ). Both of these interrupts originate from the 1797. The INTRQ signal is sent to indicate a command completion or an error. The DRQ signal is sent to indicate data will be accepted in response to a disk read or write command.

The interrupts can be detected two ways, as either a vectored interrupt on any of the bus interface pins from 4 to 11, or as a bit set in the status port, U31, which can then be polled by the CPU.

The INTRQ signal pulls the bus out of a wait state caused by a logic zero at U26-9. When pin 39 of the 1797 asserts, it is inverted at U25-6 to set pin 9 of U26.

## CONTROLLER/DISK-DRIVE LOGIC

### DATA SHAPING

Data pulses to the drive are reshaped by U16, a one-shot multivibrator, to 400 ns. Raw data from the drive are reshaped to 250 ns.

### DATA SEPARATION AND PRECOMPENSATION

Data separation and precompensation are performed primarily by U1, U3, U4, U5, and U22. The data separation circuits are used when the controller is receiving data from the disk drive, while the precompensation circuits are used when the controller is writing data to the disk.

### DATA SEPARATION

$\overline{\text{READDATA}}$  ( $\overline{\text{RDD}}$ ) from the drive couples through U9 and U16 to U1-11 and U22-27 ( $\overline{\text{RAWREAD}}$ ).  $\overline{\text{RDD}}$  contains both data bits and clock bits. U1 extracts the clock bits and sends them to U22-26 as RCLK. These pulses are synchronized with RDD. The 1797 uses the RCLK signal to extract the data bits from the  $\overline{\text{RAWREAD}}$  stream. U22 then formats the data and sends it to the CPU.

U1 uses a phase-locked loop to keep RCLK in phase with the incoming data stream. The phase-locked loop consists of U5, U4, U13, and U1. U5 is a 4-MHz voltage-controlled oscillator that drives U4 and U13. U4 and U13 select either 4 MHz or 2 MHz, depending on the disk size. If a 5-1/4" disk is being read, U4-9 is low. This couples the 2-MHz signal to U1-16. Four megahertz is coupled to U1 for 8" drives.

If the phase of RCLK should drift with respect to the incoming  $\overline{RDD}$  signal, U1 will send feedback pulses from U1-13 or U1-14 to the VCO at U5. These pulses will increase or lower the VCO frequency. In turn, the VCO frequency will increase or decrease the RCLK frequency until it again in phase with RDD. Here's how:

If the frequency of  $\overline{RDD}$  is higher than RCLK, then  $\overline{RDD}$  will go low at the beginning of RCLK. The pump-up output (PU) at U1-13 will go from a high-impedance state to a logic one. This increases the VCO frequency which increases frequency of RCLK.

If the frequency of  $\overline{RDD}$  is lower than RCLK, then  $\overline{RDD}$  will go low at the end of RCLK. The pump-down output ( $\overline{PD}$ ) responds by going from a high-impedance state to logic zero. This decreases the VCO frequency and thus decreases the frequency of RCLK.

If RCLK and  $\overline{RDD}$  are in phase, then PU and  $\overline{PD}$  are in a high-impedance state and the VCO frequency remains constant.

Pins 5, 7, and 8 of U1 allow the 1797 to control clock separation and data recovery. When pins 7 and 8 are low, the data recovery circuits are enabled. If pin 7 is high, which happens during a write operation, then the data recovery circuits are disabled.

Pin 15, DDEN, controls the frequency of RCLK. When pin 15 is logic one, the frequency of RCLK is equal to the VCO frequency divided by 16. When pin 15 is logic zero, RCLK is equal to the VCO frequency divided by 8.

#### DATA PRECOMPENSATION

Precompensation, used for 80-track double-density disk write operations, places data properly on the disk so that it can be read back with minimum error. Error is introduced by the shifting of old data that is adjacent to new data being written. This shifting is due to the nature of the magnetic fields on the disk (like fields repel).

The precompensation circuits consist of U22, U1, and U3. U22 sends the write data from pin 31 to U1-1. U3 provides delay timing for the write data in U1. U22 selects the amount of precompensation by setting the logic levels on pin 18 (LATE) and pin 17 (EARLY).



Here's what happens...

When the 1797 sends a data bit to U1-1, the strobe line at U1-5 latches high. This triggers U3-11 and causes a negative-going pulse to ripple through  $\overline{\phi 1}$ ,  $\overline{\phi 2}$ ,  $\overline{\phi 3}$ , and  $\overline{\phi 4}$ . R3 sets the pulse width of these signals and, therefore, the amount of precompensation.

With no precompensation (EARLY = LATE = 0), the data pulse is coupled to U1-6 at  $\overline{\phi 2}$  time. If LATE precompensation is selected, the data bit leaves U1-6 at  $\overline{\phi 3}$  time. EARLY precompensation synchronizes the data bit to  $\overline{\phi 1}$ .

When  $\overline{\phi 4}$  pulses low, it couples through U7 to U1-19 to clear the strobe at U1-5 in anticipation of the next write data pulse.

Precompensation must be enabled for double-density operation. The CPU does this by setting U30-19 to logic one and sending it to the DDEN input at U1-15. The CPU also asserts the  $\overline{\text{PRECOMP}}$  line at U30-12. This couples through U6-8 to TG43 at U1-9. TG43 must be high before precompensation can take place.

Even if  $\overline{\text{PRECOMP}}$  isn't asserted, the write data should be precompensated on the inner tracks, where the data is packed closer together. This condition is taken care of by U22-29, which asserts on tracks greater than 43. The TG43 signal couples through U6-8 to the TG43 input of U1.

## HEAD LOAD TIMING

The single-shot multivibrator at U15 provides read/write head-load timing. When the 1797 sends a head-load command, pin 28 goes high to load the drive head and to trigger U15.

U15-7 goes low for about 50 mS. This signal couples to U22-23 to prevent a data read or write until U15 times out. This delay compensates for bounce when the read/write head contacts the disk surface.

## 1797 TIMING

U18, U12, U14, and U30 provide timing and control of timing to the 1797. Depending on the state of U14, the clock frequency to U22-24 will be either 1 MHz or 2 MHz.

The operating frequency of the 1797 is automatically switched from 1 MHz to 2 MHz when changing from 5-1/4" drives to 8" drives. This is done by U30-6 and is coupled through U7-11 to the latch at U14.

One drawback of the 1797 is that it won't allow 5-1/4" drives to step at a 3-mS rate during track seek. To circumvent this problem, U30-15 sets the 5" FASTSTEP signal. This signal couples through U7-12 to U14. U14 increases the operating frequency to 2 MHz to speed up the step rate. At the end of the track-seek function, the clock frequency is reduced to 1 MHz again for normal 5-1/4" operation.

## 8" DRIVE INTERFACE

The 8" drive interface is through P1. All output signals to the drives are buffered through U8 and U10 except WG and HLD. The WG signal is sent through transistor Q2, as described previously. The HLD signal is inverted by U7-10 before being transmitted to the drives.

All input signals except READY and TWOSIDED are buffered through the upper section of U9 when enabled by a high on the 8"/5" line. The READY signal is inverted at U6-6, while the TWOSIDED signal is inverted at U6-11.

## 5" DRIVE INTERFACE

The 5" drive interface is through P2. All output signals to the drives are buffered through U10 and U11 except WG and MOTOR. The WG signal is sent through transistor Q3, as described previously. The MOTOR signal turns on the disk drive motor whenever a logic zero is present at pins 9, 10, 12, and 13 of U23. The single-shot at U15 keeps the drive motor on for about 20 seconds after the disk access is complete. This provides a proper turn-off delay.

All input signals are buffered through the lower section of U9, which is enabled by a low on the 8"/5" line.

## CALIBRATION CIRCUIT BOARD

The calibration circuit compares the end of the write pulse with a narrow pulse of a known delay. When the two happen simultaneously, the LED on the calibration board is latched on. This indicates that the length of the write pulse is properly adjusted.

The write pulse coming from CP3 is applied to NAND gate U501D. U501D inverts the pulse and applies it to inverter U501C and to delay line DL501. Within DL501 the pulse is delayed 120 nS between pins 1 and 10 and 160 nS between pins 1 and 6. These two delayed pulses are then compared by NAND gates U501A and U501B. The result of the comparison is a pulse 40 nS wide and 120 nS delayed in reference to the write pulse.

If the write pulse has been adjusted for a 120 nS pulse width, the write pulse at the D flip-flop U502B-11 will go high when the 40 nS delayed pulse is low. This condition causes U502B to latch a low on the Q output, U502B-9. A low at this point turns on the LED, D501.

By adjusting the precompensation controls into this 40 nS "window", it is possible to "tune" write precompensation to be not only between 120 and 160 nS, but also much closer to 120 nS than 160 nS.

To gain additional delay for greater write precompensation, DL502 (optional HE 41-10) can be added to the circuit. DL502 provides four additional delay taps with an additional 40 nS of delay per tap.

## H-207 FLOPPY DISK CONTROLLER BOARD DEFINITIONS

A0-A7	Address bits.
ALE	Address latch enable. Data and address lines from the CPU have valid information.
BDSEL	Board select. The H-207 board is selected (enabled).
CLK	Clock signal.
CS	Chip select. When asserted, the 1797 chip is enabled.
D $\emptyset$ -D7	Data bits on the H-207 board's internal data bus.
DDEN	Double density enable.
D1 $\emptyset$ -D17	Data-in bits on the S-100 bus ("in" with respect to the CPU, not the Controller).
DIR	Direction of drive head. When high, the drive head is stepping in. When low, the drive head is stepping out.
D0 $\emptyset$ -D07	Data-out bits on the S-100 bus ("out" with respect to the CPU, not the Controller).
DRQ	Data request. The 1797 data register needs data for write operations or the register has data for read operations.
DSA	Drive select A. Used with DSB to address the drives.
DSB	Drive select B. Used with DSA to address the drives.
EARLY	Write data bit early to disk drive (used for precompensation).
HLD	Head load.

HLT	Head load timing. The drive head is engaged when this signal is high.
INDEX	The index hole on the diskette has been detected.
INTRQ	Interrupt request. H-207 board has input for the CPU.
LATE	Write data bit late for drive precompensation.
MR	Master reset pin on the 1797 Controller chip that sets all registers in the chip to a known state.
pSTVAL*	Status valid.
pSYNC	New bus cycle may begin.
PD	Pump down. Decreases the frequency of the raw read data tracking clock.
PRECOMP	Enables precompensation when low.
PU	Pump up. Increases frequency of the raw read data tracking clock.
pWR	Valid data is on data-out bus (write bus).
RAWREAD	Unprocessed data from the drive.
RCLK	Clock that separates data from drive data and clock stream.
RDD	Data and clock stream from the drive.
RDME	Data or status signals input for the bus are enabled.
RDY	Slave aboard is ready. (H-207 board is a slave board.)
RE	Read enable. Enables the 1797 chip for read operations when low.
READY	The 8" disk drive is ready.

RESET        Reset signal.

SIDE1        Otherwise known as side select output. When high side 1 is selected in the drive. When low, side 0 is selected.

sINP         Status signal signifying data input to the bus (read cycle) may occur.

sOUT         Status signal signifying data output from the bus (write cycle) may occur.

STEP         Steps the drive head one step per pulse.

STB          Strobe output from the 1691 (U1) phase lock loop control.

TG43         Track greater than 43. The drive read/write head is over or past track 43 (track of mandatory precompensation in double density 8" drive.

TK $\emptyset$         Track 0. The drive read/write head is over track 0 on the diskette.

TWOSIDED    The 8" drive is set for two-sided operation with a two-sided diskette.

VFOE/WF     VFO enable/write fault. When WG is asserted, VFOE/WF flags write faults when deasserted, terminating any write commands. When WG is deasserted, VFDE/WF enables the data separator in the 1691.

V1 $\emptyset$ \*-V17\*   Vector interrupts.

WAIT         RDY line is low (not ready).

WAITEN      Wait enable. Set RDY line low on all accesses of the 1797 data register.

WD          Write data. Contains the data to be written onto the diskettes as well as the clock signals.

WDIN        Write data into the 1691 phase lock loop control.

WDOUT Write data out of the 1691 phase lock loop and precompensation controller.

WG Write gate. Output to the disk drive is valid.

WE Write enable. Enables the 1797 chip for write operations.

WPRT Write protect. When this signal is received, no write command can take place and write protect bit in the status register is set.

WRDATA Precompensated write data pulses that have been reshaped by U16.

5DS $\phi$ -5DS3 Five-inch drive select signals.

5"FASTEP Enables fast stepping in the 5.25" drives.

8"/ $\bar{5}$ " Selects between the 8" and the 5.25" drives.

8DS $\phi$ -8DS3 Eight-inch drive select signals.

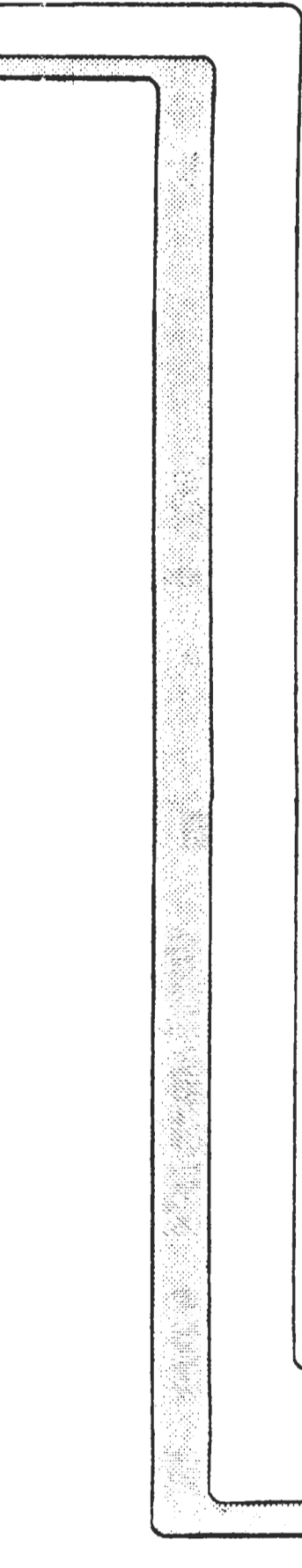
CLOCK Master clock signal.

$\phi$ 1 -  $\phi$ 4 Precompensation phase signals.

# DISASSEMBLY

INTRODUCTION  
ALL-IN-ONE  
LOW PROFILE

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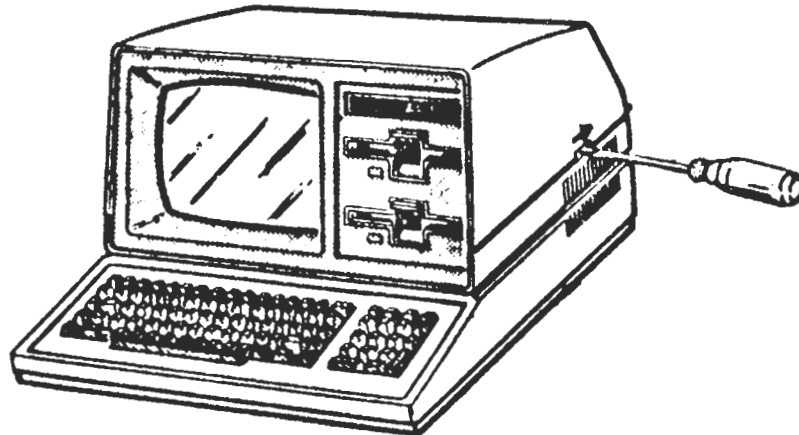




## INTRODUCTION

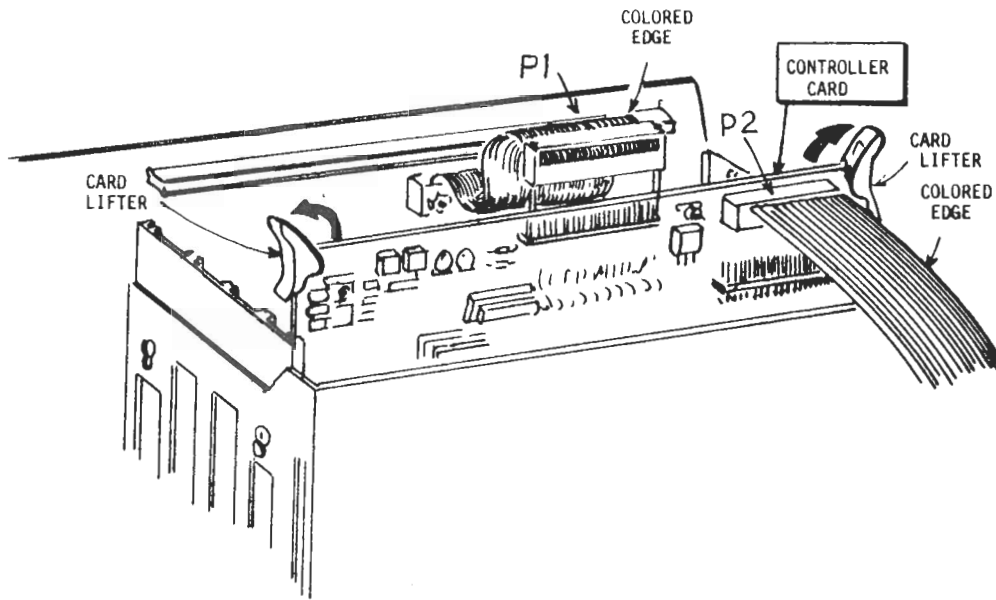
The procedures on the following pages show you how to remove the H-207 Floppy Disk Controller Board from the two different models of the H/Z-100. Find the appropriate procedure and follow the instructions.

### ALL-IN-ONE



-- With a flat-blade screwdriver, slide the latch bracket to the center of the slot in the cabinet top. The latch bracket is spring loaded, so you will have to work with one side of the cabinet top at a time. While holding the latch in the center position, lift that side of the cabinet top. After one side is freed, perform the procedure on the other side. Be sure to hold the freed side up, so it will not snap back down.

-- Remove the cabinet top and set it aside in a safe place.

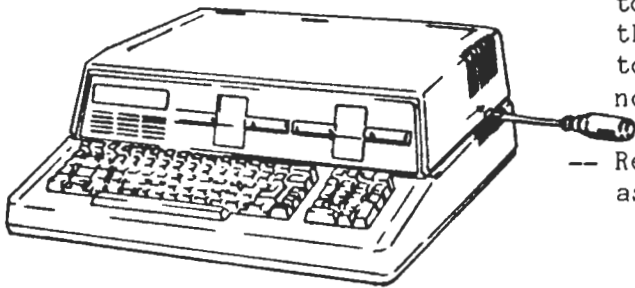


- Disconnect the 50-conductor cable at P1 and the 34-conductor cable at P2 from the H-207 board.
- Lift up on the H-207 board extractors to pop the board free from the S-100 bus connector.
- Now lift the H-207 board from the card cage.

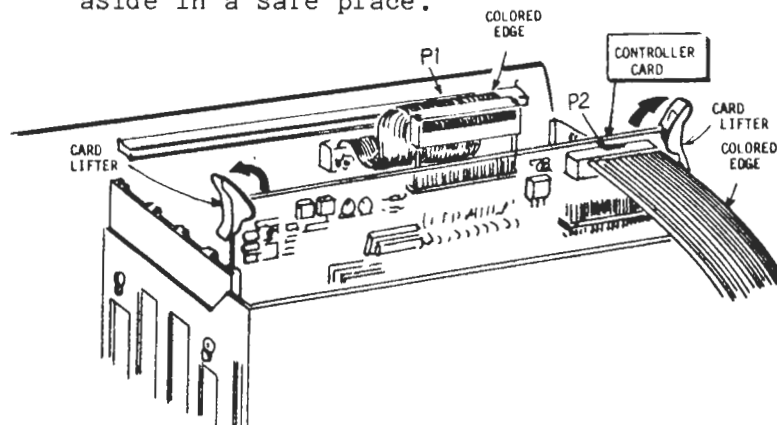
This completes the removal of the H-207 board from the H/Z-100 All-in-One computer. Reverse the procedure to install the board into the computer.

## LOW PROFILE

- With a flat-blade screwdriver, slide the latch bracket to the center of the slot in the cabinet top. The latch is spring loaded, so you will have to work with one side of the cabinet top at a time. While holding the latch in the center position, lift that side of the cabinet top. After one side is freed, perform the procedure on the other side. Be sure to hold the freed side up, so it will not snap back down.



- Remove the cabinet top and set it aside in a safe place.



- Disconnect the 50-conductor cable at P1 and the 34-conductor cable at P2 from the H-207 board.
- Lift up on the H-207 board extractors to pop the board free from the S-100 bus connector.
- Now lift the H-207 board from the card cage.

This completes the removal of the H-207 board from the H/Z-100 Low-Profile computer. Reverse the procedure to install the board into the computer.

TECHNICIAN NOTES:

## VISUAL CHECKS

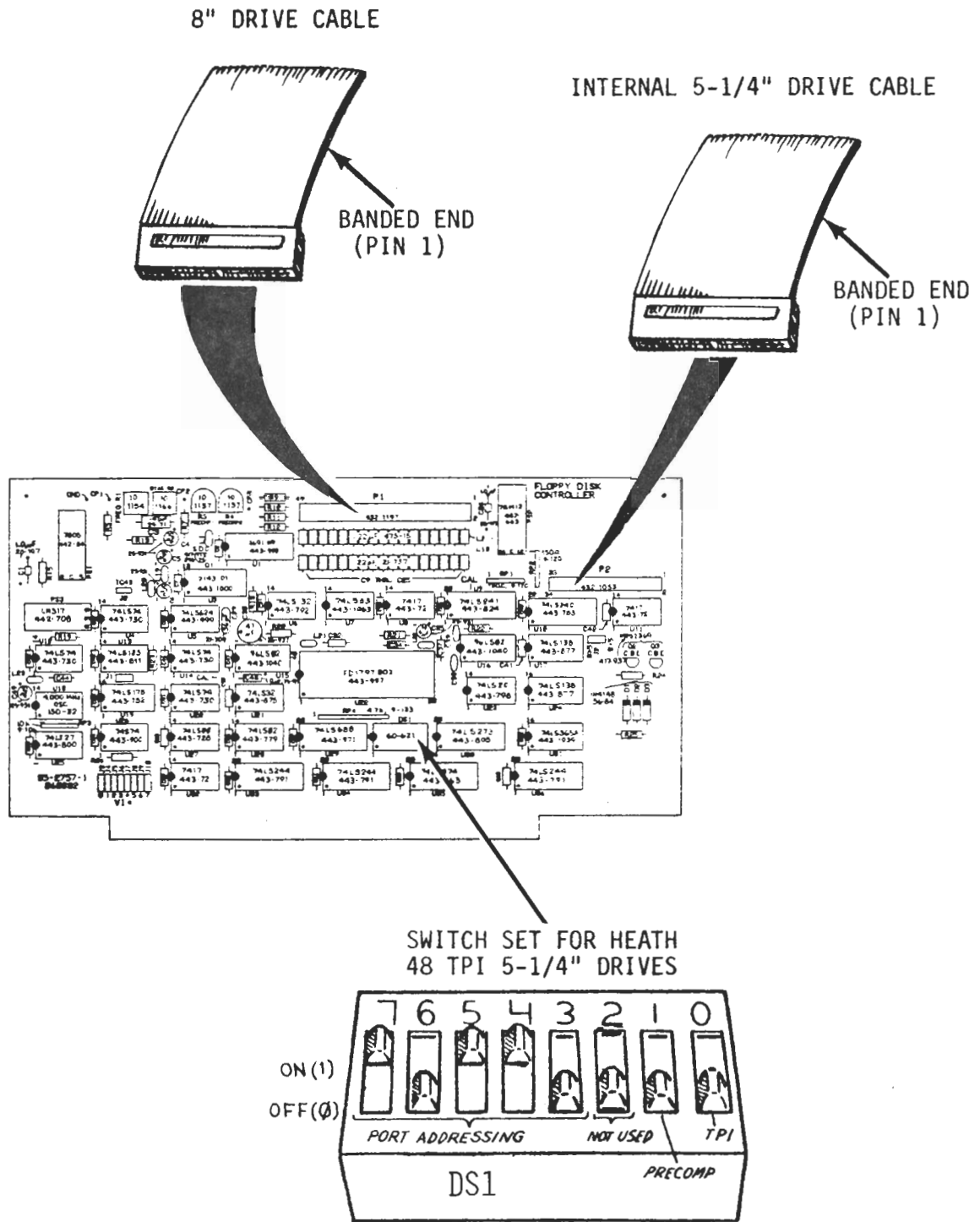
DISK CONTROLLER BOARD CABLE CONNECTIONS  
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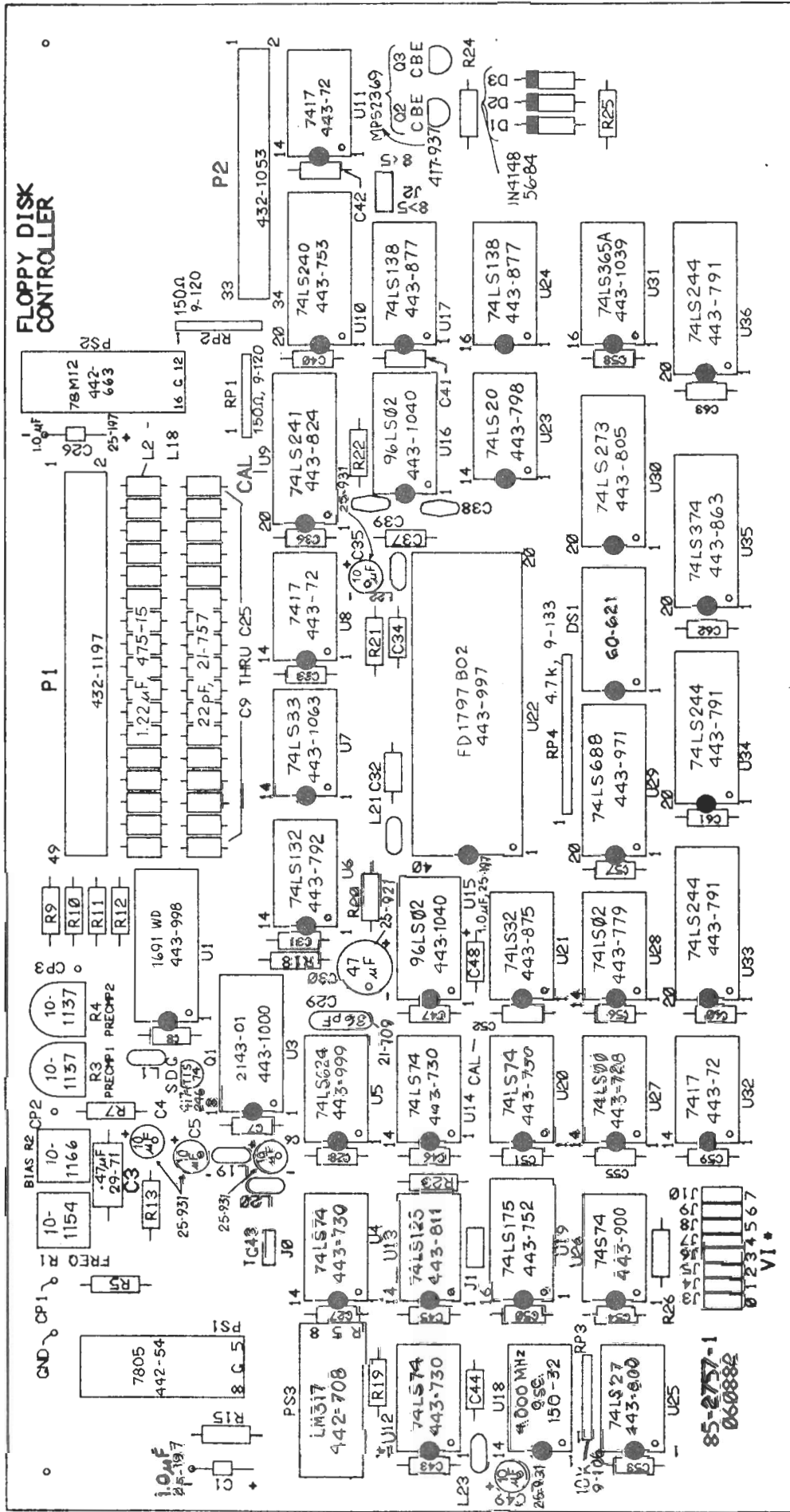


# DISK CONTROLLER BOARD CABLE CONNECTIONS AND SWITCH POSITIONS (IN AN H/Z-100 ENVIRONMENT)





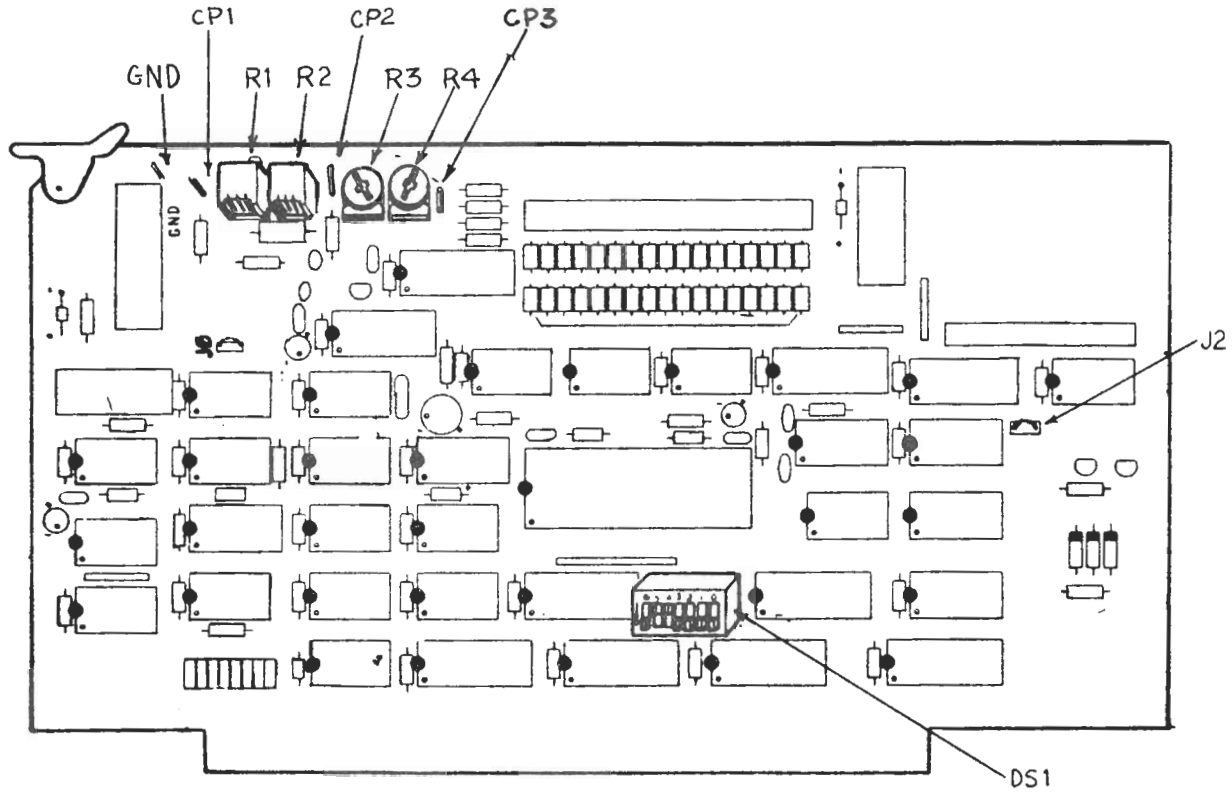
CIRCUIT COMPONENT LOCATIONS AND VALUES



H-207 FLOPPY DISK CONTROLLER

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H-207 CONTROLLER BOARD  
CONTROLS AND JUMPER LOCATIONS

## INTRODUCTION

In this section of the manual, instructions will be given on how to calibrate the H-207 Disk Controller Board. There are two adjustments that the controller board may require. These are Data Separator adjustments and Write Precompensation adjustments. Follow the procedures below to perform these two adjustments.

## EQUIPMENT NEEDED

<u>Frequency Counter</u>	IM-2420 or equivalent (optional).
<u>Low Capacitance Probe</u>	PKW-105 or equivalent.
<u>Multimeter</u>	IM-2202 or equivalent.
<u>Oscilloscope</u>	IO-4510 or equivalent.
<u>H-207 Calibration Board</u>	See H-207 assembly manual (HE 595-2909) for parts list and assembly details.

## DATA SEPARATOR ADJUSTMENT

Located on the following pages are two methods to adjust the data separator. The first procedure is the preferred method because of its ease and accuracy. The second procedure is the same method given to kitbuilders of the H-207. Locate the procedure you wish to use and follow the steps in that procedure.

## FREQUENCY COUNTER METHOD

- Allow a fifteen minute warm-up of the board with the top cover of the computer in place.
- Remove the top cover of the computer.
- Connect the common test lead of the multimeter to the GND test point at the upper left side of the controller board. Refer to the H-207 Controls and Jumper Locations pictorial.
- Connect the positive test lead to the CP2 test point.
- Adjust the BIAS control (R2) until the multimeter display shows +1.40 VDC (±.05 volts). Switch the multimeter to lower ranges to perform this adjustment accurately.
- Disconnect the multimeter.
- Connect the common lead of the frequency counter to the GND test point.
- Connect the test probe of the frequency counter to the CP1 test point.
- Adjust the FREQ control (R1) until the frequency counter display shows 4.000 MHz.
- Disconnect the frequency counter.

The adjustments to the Data Separator are now complete. Proceed to WRITE PRECOMPENSATION ADJUSTMENTS.

## KIT BUILDER METHOD

- Remove the controller board from the computer.
- Remove U9, U22, and U30 from their sockets.
- Tack solder a length of wire between pins 1 and 20 of the socket for U9.
- Tack solder wires to interconnect pins 30, 33, 37, and 20 of the socket for U22.
- Set the PRECMP 2 control (R4) to a fully clockwise position.
- Set the PRECMP 1 control (R3) to a fully counterclockwise position.
- Connect the common test lead of the multimeter to the GND test point.
- Reinstall the controller board into the computer.
- Connect the positive test lead to the CP2 test point and apply power to the computer.
- Adjust the BIAS control (R2) until the multimeter display shows +1.40 VDC (±.05 volts). You will want to switch the multimeter to lower ranges to perform this adjustment accurately.
- Allow a period of 15 minutes for drifting; then perform the R2 adjustment again.
- Power down the computer and remove the controller board.
- Tack solder a length of wire between the two holes marked CAL.
- Reinstall the controller board and apply power to the computer.
- Adjust the FREQ control (R1) for a multimeter display of +1.40 VDC (±0.05 volts) at test point CP2.
- Power down the computer and remove the controller board.
- Remove all the temporarily installed jumper wires.
- Install U9, U22, and U30 in their respective sockets.
- Reinstall the controller board into the computer.

The adjustments to the Data Separator are now complete. Proceed to WRITE PRECOMPENSATION ADJUSTMENTS.

## WRITE PRECOMPENSATION ADJUSTMENTS

Located on the following pages are two methods to adjust write precompensation. The first method uses the calibration circuit board that is included in the H-207 kit. The second method requires the use of an oscilloscope and precompensation data about the drives that are used with the controller board. The first method is the preferred method because of its ease. The second method is required, however, when precompensation values not included on the calibration circuit board are needed for a particular drive. Locate the procedure you wish to use and follow the steps in that procedure.

### CALIBRATION CIRCUIT BOARD METHOD

The calibration circuit board method is primarily used to adjust the H-207 for use within a H/Z-100. By using this method, the 5-1/4" drive section of the controller board is set for a write precompensation value of 120 nS. This is the value used for Heath/Zenith 48 TPI, 5-1/4" disk drives that are included in the H/Z-100s. The jumpers at J0 and J2 remain at the stock position. That is, J0 is out and J2 is in the 8 < 5 position (foil bridge).

You may use the calibration circuit board for other values of precompensation. By installing DL502, you may choose from five values of precompensation. These being 120 nS, 160 nS, 200 nS, 240 nS, and 280 nS. However, you may have a customer application that requires a precompensation value not mentioned above. In this case, proceed to Oscilloscope Method of Write Precompensation.

You may also use the calibration circuit board for setting write precompensation for 8" disk drives. Again, if the precompensation value needed is not obtainable with the calibration board, use the Oscilloscope Method. Remember when setting precompensation for 8" drives, you will have to determine if the 8" value is greater than the 5-1/4" value. If it is, you will have to jumper J2 so it is in the 8 > 5 position. Also remember, that R4 is the control that needs to be adjusted instead of R3.

## PROCEDURE

- Obtain a calibration circuit board (see H-207 manual HE 595-2909 for construction).
- Connect the alligator clip of the calibration board to a source of +5 volts on the H-207 controller board. The positive end of any .1 uF glass capacitor is a good source.
- Connect the black wire from the calibration board to the GND test point on the H-207 board.
- Connect the yellow wire from the calibration board to the CP3 test point of the H-207 board.
- If not already done, set R3 fully counterclockwise and R4 fully clockwise.
- Set the jumper select wire of the calibration board to 120 nS. If the drive requires more precompensation, set the jumper to the desired position.
- Turn on the computer.
- Boot up a system disk. Refer to the appropriate operating system manual and start the disk format program.
- While the format program is running, adjust R3 on the H-207 board until the LED on the calibration board just turns on.
- Turn off the computer and disconnect the calibration circuit board.

This completes write precompensation adjustment.

NOTE: All diskettes should be reformatted before being used.



## OSCILLOSCOPE METHOD

The oscilloscope method of write precompensation adjustment is primarily used to adjust the H-207 for non Heath/Zenith disk drives. To understand the relationship that exists between the PRECOMP switch setting of DS1 and jumper J0, refer to the table below. This table shows how to set the PRECOMP switch of DS1 and J0 for the particular system you are working on. Now perform the following steps to adjust write precompensation. Refer to the illustration at the beginning of this section for the locations of the test points.

TYPE OF DRIVE	DESIRED RESULTS		
	Precomp no tracks	Precomp all tracks	Precomp tracks >43
8" Double-Density	N/A	Precomp = 0 J0 = X	Precomp = 1 J0 = X
5-1/4", 48 TPI, Double-Density	Precomp = 1 J0 = X	Precomp = 0 J0 = X	N/A
5-1/4", 96 TPI, Double-Density	Precomp = 1 J0 = IN	Precomp = 0 J0 = X	Precomp = 1 J0 = OUT

\*Precomp is bit 4 in the control latch

X = Don't Care

NOTE: Precomp is automatically disabled in single-density operation.

- Set the PRECMP 2 control (R4) to a fully clockwise position.
- Set the PRECMP 1 control (R3) to a fully counterclockwise position.

The position of J2 will determine which of the two following procedures you will use when adjusting write precompensation. Refer to the manufacturer's suggested write precompensation value for the type of drives in the system. If the system has only 8" disk drives, or only 5-1/4" disk drives, or the 8" write precompensation figure is less than the 5-1/4" write precompensation figure, use the procedure under "J2 = 8 < 5". If the system has disk drives where the 8" write precompensation figure is greater than the 5-1/4" write precompensation figure, use the procedure under "J2 = 8 > 5".

Typical values of precompensation are:

5-1/4" disk drives	125 to 200 nS	typical 150 nS.
8" disk drives	125 to 175 nS	typical 135 nS

## J2 = 8 &lt; 5 PROCEDURE

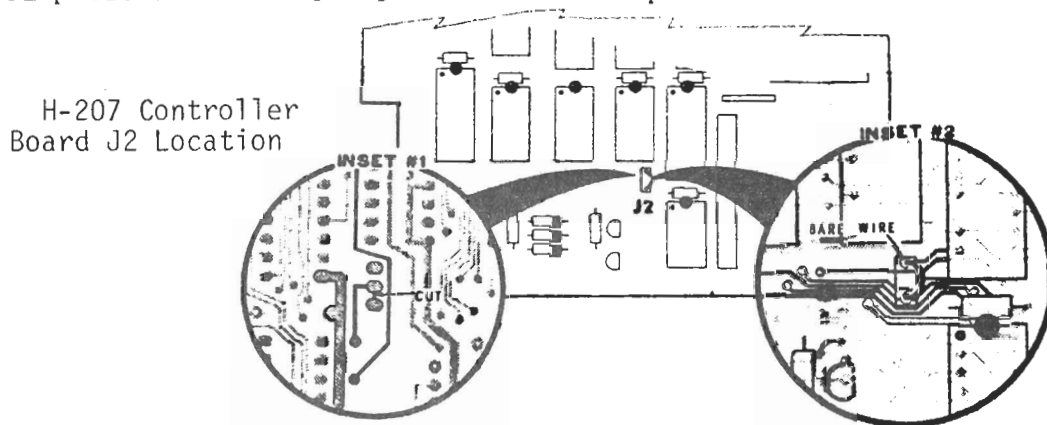
- Connect the oscilloscope probe to GND and CP3.  
Set the probe to X10 and set the oscilloscope at 50 nS/division to display a 100 to 300 nS negative going pulse.
- Apply power to the computer.
- If the system has 8" disk drives, start the format routine on an 8" diskette. While format is running, adjust the PRECMP 1 control (R3) until the pulse width displayed on the oscilloscope corresponds to the manufacturer's suggested write precompensation for that type of drive.
- If there are 5-1/4" disk drives in addition to 8" disk drives in the system, start the format routine on a 5-1/4" diskette. While format is running, adjust the PRECMP 2 control (R4) until the pulse width displayed on the oscilloscope corresponds to the manufacturer's suggested write precompensation for that type of drive.
- If the system only has Heath/Zenith 5-1/4" 96 TPI disk drives or non Heath/Zenith disk drives that require write precompensation adjustment, start the format routine on a 5-1/4" diskette. While format is running, adjust the PRECMP 1 control (R3) until the pulse width displayed on the oscilloscope corresponds to the manufacturer's suggested write precompensation value for that drive.
- Power down the computer.
- Disconnect the oscilloscope probe.

This completes write precompensation adjustment.

NOTE: All diskettes should be reformatted before being used.

## J2 = 8 &gt; 5 PROCEDURE

- Remove the controller board from the computer.
- Refer to the H-207 J2 location pictorial and cut the foil that connects the middle of the J2 position to the 8 < 5 position of J2.
- Install a jumper wire connecting the middle hole of the J2 position to the 8 > 5 hole of the J2 position.



- Install the floppy board into the computer.
- Connect the oscilloscope probe to GND and CP3. Set the probe to X10 and set the oscilloscope at 50 nS/division to display a 100 to 300 nS negative going pulse.
- Apply power to the computer.
- While formatting a 5-1/4" diskette, adjust the PRECMP 1 control (R3) until the pulse width displayed on the oscilloscope corresponds with the manufacturer's suggested write precompensation value.
- While formatting an 8" diskette, adjust the PRECMP 2 control (R4) until the pulse width displayed on the oscilloscope corresponds with the manufacturer's suggested write precompensation value.
- Power down the computer.
- Disconnect the oscilloscope probe.

This completes the write precompensation adjustment.

NOTE: All diskettes should be reformatted before being used.

## TROUBLESHOOTING

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## INTRODUCTION

To troubleshoot the H-207 Floppy Disk Controller, use this section of the manual in conjunction with the schematic. Located in this section of the manual are service hints that will aid you in servicing the board. The schematic contains voltages and logic levels of a normally functioning board after a hard reset. By using standard troubleshooting techniques, most problems can be quickly located and corrected.

## EQUIPMENT NEEDED

<u>Frequency Counter</u>	IM-2420 or equivalent.
<u>Logic Probe</u>	IT-4710 or equivalent.
<u>Low Capacitance Probe</u>	PKW-105 or equivalent.
<u>Multimeter</u>	IM-2260 or equivalent.
<u>Oscilloscope</u>	IO-4510 or equivalent.

## H/Z-100 TEST FIXTURE

The H/Z-100 test fixture is set up so that the 5-1/4", 48 TPI disk drives are the primary boot device. Also, auto boot is defeated (See "Configuration").

It is assumed that the H-207 board is configured for operation within the H/Z-100. That is, J1 is jumpered for a 3 MHz or greater clock speed and DS1 is configured for port B0 (Hex), 48 TPI, and precompensation disabled.

## PREWORK

Once you have received a H-207 Floppy Controller Board in for service, use the checkout procedure below. Included in the procedure are problems that may be identified before power is applied to the circuit board. Many of the checks below may have already been implemented in your preworking.

## CHECKOUT PROCEDURE

Check the H-207 Controller Board for:

- Polarized capacitors installed backwards.
- Q1, Q2, or Q3 installed incorrectly.
- D1, D2, or D3 installed backwards.
- ICs installed backwards.
- Dirty S-100 board contacts.
- Solder bridges.
- Cold solder joints.
- Resistor packs installed backwards.
- Correct jumpering.
- Switch settings of DS1.
- Correct voltage regulator for location:

7805 at PS1.  
78M12 at PS2.  
LM317 at PS3.

After making these checks, install the H-207 into your H/Z-100 test fixture and confirm the customer's complaint. If the board appears to operate properly, align the controller board using the procedure in the Alignment and Adjustments section of this manual.

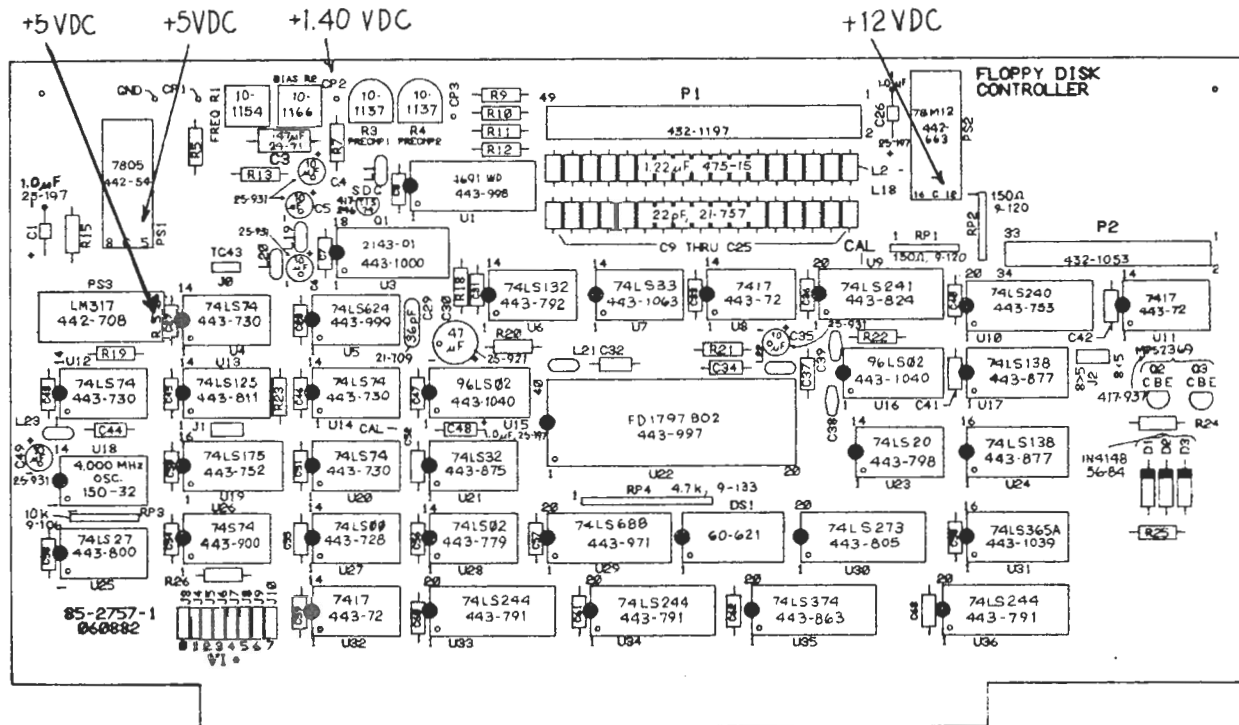
If the problem still exists, proceed to Service Hints.

## SERVICE HINTS

## VOLTAGE CHECKS

With the H-207 installed in your test fixture, perform the following voltage checks with your multimeter. The GND test point is a good place to connect the common lead of the multimeter. It is assumed that the disk drive cables are disconnected from the controller board.

- The voltage at PS1-5 is +5 VDC.
- The voltage at PS2-12 is +12 VDC.
- The voltage at PS3-5 is +5 VDC.
- The voltage at CP2 is +1.40 VDC.



If the voltages at these test points are within 5% of the values stated, it can be safely assumed U1, U5, and the voltage regulators are operating properly. Assuming the problem still exists, further aid can be found in Logic Level Checks and Waveforms. Otherwise, proceed to the Alignment and Adjustments.



## LOGIC LEVEL CHECKS

On the following pages is a logic probe analysis of the H-207 board. When performing the tests, you need only to test the ICs in the left column indicated by an asterisk (\*). If you don't get the suggested logic state, then check each IC listed immediately to the right. The logic states for these ICs are listed in the left column below the ICs with the asterisks.

Continue tracing backwards using this procedure until you test an IC that matches the suggested logic state. The previous IC that you tested is likely the bad IC.

Before you replace the suspected IC, check the other lines leading up to it. You must do this because this checkout procedure gives only the most likely causes to the problem. It doesn't cover such things as open ground foils, shorted foil runs, or open resistors.

As you make the following checks, press the (B)oot key and press RETURN. Logic states located inside parenthesis indicates that the probe pulses one or more times while "Read Completed" is printed on the screen. In the case of a (P) indication, the pulse rate (as indicated by the logic probe) will momentarily change during the "Read Completed" interval.

The schematic shows the logic states after a CTRL/RESET has been performed. Refer to these logic states for troubleshooting areas not covered in the following tests.

To setup the H-207 for the following test, connect at least one 48 TPI, 5-1/4" disk drive to P1 and turn on the computer.

## H-207 DISK CONTROLLER TEST

CHECK	IF NOT OKAY, CHECK
*Q3 Collector = Z	U21-8
*U1-16 = 2 MHz	U13-6
*U7-4 = L	U7-5 (Also press and release CTR/RESET. U7-4 should remain low for about 18 seconds. If not, then replace U15.)
*U9-19 = L	U30 or the data bus is defective.
*U10-12 = H	U10 or U22 is defective.
*U10-14 = H	U10 or U22 is defective.
*U10-16 = H	U10 or U22 is defective.
*U11-4 = H	U11-3
*U11-6 = H	U11-5
*U11-8 = H	U11-9
*U11-10 = L	U11-11
*U11-12 = H	U11-13
*U22-2 = (H)	U21-11
*U22-3 = (H)	U21-3
*U22-23 = (H)	U15-7
*U22-24 = 1 MHz	U13-8
*U22-27 = P	U16-9
*U22-34 = L	U9 is defective.
*U22-35 = L	U9 is defective.
*U22-36 = H	U9 is defective.
*U31-1 = (H)	U27-8
*U31-15 = (H)	U17-14
*U32-6 = (H)	U32-5
*U35-11 = (P)	U28-4
*U36-1 = (H)	U27-8
*U36-19 = (H)	U27-8

End of test.

---

U4-3 = 4 MHz  
 U4-5 = 2 MHz  
 U4-9 = L  
 U4-11 = P  
 U4-12 = L

U5-8 = 4 MHz

U7-5 = H  
 U7-11 = L  
 U7-12 = L  
 U7-13 = H

U10-3 = L  
 U10-17 = H

U11-3 = H  
 U11-5 = H  
 U11-9 = H  
 U11-11 = L  
 U11-13 = H

U12-3 = 4 MHz  
 U12-5 = 2 MHz  
 U12-9 = 1 MHz  
 U12-11 = 2 MHz

U13-4 = L  
 U13-5 = 2 MHz  
 U13-6 = 2 MHz  
 U13-8 = 1 MHz  
 U13-9 = 1 MHz  
 U13-10 = L

U14-8 = L  
 U14-11 = 1 MHz  
 U14-12 = H

U15-4 = H  
 U15-7 = (H)

U16-4 = L  
 U16-7 = H  
 U16-9 = P  
 U16-11 = P

U5-8  
 U4-3  
 U4-11, U4-12  
 U4-5  
 U30 or the data bus is defective.

U5 or U1 defective; R1 or R2  
 incorrectly adjusted.

U23-8  
 U30 or the data bus is defective.  
 U30 or the data bus is defective.  
 U7-11, U7-12

U10-17  
 U33-9

U16-7  
 U24-14  
 U24-12  
 U24-15  
 U24-13

U18 is bad.  
 U12-3  
 U12-11  
 U12-5

U4-9  
 U4-5  
 U13-4, U13-5  
 U13-9, U13-10  
 U12-9  
 U14-8

U14-11, U14-12  
 U12-9  
 U7-13

U22 or the data bus is defective.  
 U15-4

U1 or U22 is defective.  
 U16-4  
 U16-11  
 U9 is defective.

U17-1 = P	U34-18
U17-2 = P	U34-16
U17-4 = (H)	U20-6
U17-6 = P	U34-14
U17-7 = L	U19-1
U17-14 = (H)	U17-1, U17-2, U17-4, U17-6
U17-15 = (H)	U17-1, U17-2, U17-4, U17-6
U19-1 = (L)	U26-8
U19-14 = L	U19-1
U20-1 = (L)	U28-13
U20-2 = (L)	U28-13
U20-3 = P	U27-6
U20-5 = (L)	U20-1, U20-2, U20-3
U20-6 = (H)	U20-1, U20-2, U20-3
U21-1 = (H)	U27-11
U21-2 = (H)	U27-8
U21-3 = (H)	U21-1, U21-2
U21-4 = (H)	U17-15
U21-5 = (P)	U33-12
U21-6 = (H)	U21-4, U21-5
U21-8 = L	U21-10
U21-10 = L	U22 of data bus is defective.
U21-11 = (H)	U21-12, U21-13
U21-12 = (H)	U27-11
U21-13 = (P)	U33-12
U22-39 = (L)	Check the data bus at pins 7 through 14. These lines pulse from a high impedance state while "Read Completed" is being printed. If not, then check the components along the data bus.
U23-2 = (L)	U30-16
U23-4 = P	U34-18
U23-5 = P	U34-16
U23-6 = (H)	U23-2, U23-4, U23-5
U23-8 = H	U23-13
U23-13 = L	U24-15

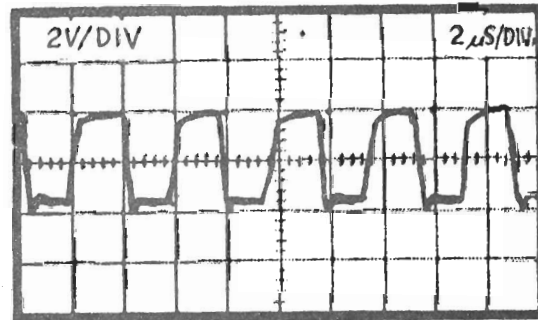
U24-1 = L	U30 or the data bus is defective.
U24-2 = L	U30 or the data bus is defective.
U24-3 = L	U30 or the data bus is defective.
U24-6 = H	U30 or the data bus is defective.
U24-12 = H	U24-1, U24-2, U24-3, U24-6
U24-13 = H	U24-1, U24-2, U24-3, U24-6
U24-14 = H	U24-1, U24-2, U24-3, U24-6
U24-15 = L	U24-1, U24-2, U24-3, U24-6
U25-1 = L	U19-7
U25-2 = L	U10-3
U25-3 = L	U10-3
U25-4 = (L)	U22-39
U25-5 = L	U19-14
U25-6 = (H)	U25-3, U25-4, U25-5
U25-12 = (H)	U25-1, U25-2, U25-13
U25-13 = (L)	U22-39
U26-2 = (H)	U23-6
U26-3 = (L)	U20-5
U26-4 = (H)	U25-12
U26-5 = (H)	U26-2, U26-3, U26-4
U26-8 = (L)	U26-10, U26-11, U26-12
U26-10 = (H)	U25-6
U26-11 = (L)	U20-5
U26-12 = (H)	U23-6
U27-1 = (L)	U22-39
U27-3 = (H)	U27-1
U27-4 = P	U33 defective.
U27-5 = P	U33 defective.
U27-6 = P	U27-5, U27-4
U27-8 = (H)	U27-9, U27-10
U27-9 = P	U33 defective.
U27-10 = (L)	U20-5
U27-11 = (H)	U27-12, U27-13
U27-12 = (L)	U28-10
U27-13 = (H)	U26-5
U28-1 = (H)	U28-2, U28-3
U28-2 = (L)	U33 defective.
U28-3 = (L)	U33 defective.
U28-4 = (P)	U28-6

U28-6 = (P)	U33-12
U28-8 = (H)	U20-6
U28-9 = P	U34-14
U28-10 = (L)	U28-8, U28-9
U28-11 = (P)	U29-19
U28-12 = (H)	U28-1
U28-13 = (L)	U28-11, U28-12
U29-19 = (P)	U29, U34, or DS1 defective.
U30-1 = H	U33-9
U30-11 = (H)	U21-6
U30-16 = (L)	U30-1, U30-11, or data bus problem.
U32-5 = (H)	U27-3
U33-9 = H	U33 defective.
U33-12 = (P)	U33 defective.
U34-14 = P	U34 defective.
U34-16 = P	U34 defective.
U34-18 = P	U34 defective.

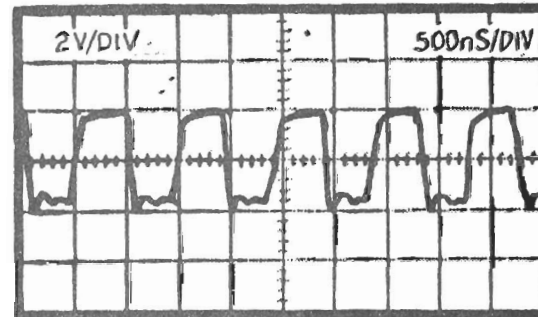
## WAVEFORMS

The waveforms shown in this section are generated by a normally functioning controller board in an idle state. Use these waveforms as a reference when checking waveforms on the board you are servicing.

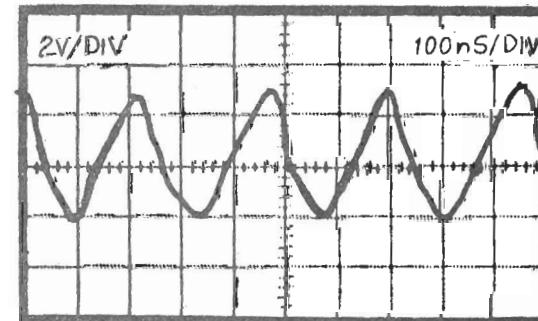
The waveform at the right was taken from U22-26. This is the RCLK signal that originates at U1-12. In an idle state the frequency of RCLK is around 250 kHz.



The waveform at the right was taken from U22-24. This is the CLK signal that originates from the oscillator circuits. The frequency of this signal is 1 MHz when the board is in an idle state.



The waveform at the right was taken from CP1. This is the VCO signal that originates from the VCO, U5-8. The frequency of this signal is 4 MHz when the board is in an idle state.



## PARTS LISTS

DISK CONTROLLER CIRCUIT BOARD  
CALIBRATION CIRCUIT BOARD

5-179  
5-180





# PARTS LIST

## DISK CONTROLLER CIRCUIT BOARD

CIRCUIT DESCRIPTION HEATH Part No.

CIRCUIT DESCRIPTION HEATH Part No.

CIRCUIT DESCRIPTION HEATH Part No.

CIRCUIT DESCRIPTION HEATH Part No.

### CAPACITORS

C1 1.0 uF tantalum HE 25-197  
 C2 none  
 C3 .47 uF polycarbonate HE 29-71  
 C4 10 uF tantalum HE 25-220  
 C5 10 uF tantalum HE 25-220  
 C6 10 uF tantalum HE 25-220  
 C7 .1 uF ceramic HE 21-762  
 C8 .1 uF ceramic HE 21-762  
 C9 22 pF ceramic HE 21-757  
 C10 22 pF ceramic HE 21-757  
 C11 22 pF ceramic HE 21-757  
 C12 22 pF ceramic HE 21-757  
 C13 22 pF ceramic HE 21-757  
 C14 22 pF ceramic HE 21-757  
 C15 22 pF ceramic HE 21-757  
 C16 22 pF ceramic HE 21-757  
 C17 22 pF ceramic HE 21-757  
 C18 22 pF ceramic HE 21-757  
 C19 22 pF ceramic HE 21-757

### CAPACITORS (CONTINUED)

C46 .1 uF ceramic HE 21-762  
 C47 .1 uF ceramic HE 21-762  
 C48 1.0 uF tantalum HE 25-197  
 C49 10 uF tantalum HE 25-220  
 C50 .1 uF ceramic HE 21-762  
 C51 .1 uF ceramic HE 21-762  
 C52 .1 uF ceramic HE 21-762  
 C53 .1 uF ceramic HE 21-762  
 C54 .1 uF ceramic HE 21-762  
 C55 .1 uF ceramic HE 21-762  
 C56 .1 uF ceramic HE 21-762  
 C57 .1 uF ceramic HE 21-762  
 C58 .1 uF ceramic HE 21-762  
 C59 .1 uF ceramic HE 21-762  
 C60 .1 uF ceramic HE 21-762  
 C61 .1 uF ceramic HE 21-762  
 C62 .1 uF ceramic HE 21-762  
 C63 .1 uF ceramic HE 21-762

### INDUCTORS

L1 35 uH HE 235-229  
 L2 1.22 uH bead HE 475-15  
 L3 1.22 uH bead HE 475-15  
 L4 1.22 uH bead HE 475-15  
 L5 1.22 uH bead HE 475-15  
 L6 1.22 uH bead HE 475-15  
 L7 1.22 uH bead HE 475-15  
 L8 1.22 uH bead HE 475-15  
 L9 1.22 uH bead HE 475-15  
 L10 1.22 uH bead HE 475-15  
 L11 1.22 uH bead HE 475-15  
 L12 1.22 uH bead HE 475-15  
 L13 1.22 uH bead HE 475-15  
 L14 1.22 uH bead HE 475-15  
 L15 1.22 uH bead HE 475-15  
 L16 1.22 uH bead HE 475-15  
 L17 1.22 uH bead HE 475-15  
 L18 1.22 uH bead HE 475-15  
 L19 35 uH HE 235-229  
 L20 35 uH HE 235-229  
 L21 35 uH HE 235-229  
 L22 35 uH HE 235-229  
 L23 35 uH HE 235-229

### RESISTORS

R1 10 kilohm control HE 10-1154  
 R2 100 kilohm control HE 10-1180  
 R3 2 kilohm control HE 10-1137  
 R4 2 kilohm control HE 10-1137  
 R5 47 ohm 1/4 watt, 5% HE 6-470-12  
 R6 none  
 R7 47 kilohm 1/4 watt, 5% HE 6-473-12  
 R8 jumper  
 R9 1 megohm 1/4 watt, 5% HE 6-105-12  
 R10 1000 ohm 1/4 watt, 5% HE 6-102-12  
 R11 3900 ohm 1/4 watt, 5% HE 6-392-12  
 R12 1800 ohm 1/4 watt, 5% HE 6-182-12  
 R13 47 kilohm 1/4 watt, 5% HE 6-473-12  
 R14 jumper  
 R15 720 ohm 1/4 watt, 1% HE 6-7200-12  
 R16 none  
 R17 none  
 R18 120 kilohm 1/4 watt, 5% HE 6-124-12  
 R19 237 ohm 1/4 watt, 1% HE 6-2370-12  
 R20 1 megohm 1/4 watt, 5% HE 6-105-12  
 R21 3900 ohm 1/4 watt, 1% HE 6-3901-12  
 R22 2200 ohm 1/4 watt, 1% HE 6-2201-12  
 R23 1000 ohm 1/4 watt, 5% HE 6-102-12  
 R24 120 kilohm 1/4 watt, 5% HE 6-124-12  
 R25 1000 ohm 1/4 watt, 5% HE 6-102-12  
 R26 1000 ohm 1/4 watt, 5% HE 6-102-12

### RESISTOR PACKS

RP1 150 ohm HE 9-120  
 RP2 150 ohm HE 9-120  
 RP3 10 kilohm HE 9-106  
 RP4 4.7 kilohm HE 9-133

# PARTS LIST

5-180

CIRCUIT DESCRIPTION  
Comp. No. HEATH Part No.

## DISK CONTROLLER CIRCUIT BOARD (CONTINUED)

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
<b>INTEGRATED CIRCUITS</b>		
P51	7805 5V regulator	HE 442-54
P52	78M12 +12V regulator	HE 442-663
P53	LM317 +adj regulator	HE 442-708
U1	WD1691	HE 443-998
U2	none	
U3	2143-01	HE 443-1000
U4	74LS74	HE 443-730
U5	74LS624	HE 443-999
U6	74LS132	HE 443-792
U7	74LS33	HE 443-1063
U8	7417	HE 443-72
U9	74LS241	HE 443-824
U10	74LS240	HE 443-753
U11	7417	HE 443-72
U12	74LS74	HE 443-730
U13	74LS125	HE 443-811
U14	74LS74	HE 443-730
U15	96LS02	HE 443-1040
U16	96LS02	HE 443-1040
U17	74LS138	HE 443-877
U18	4,000 MHz oscillator	HE 150-132
U19	74LS175	HE 443-752
U20	74LS74	HE 443-730
U21	74LS32	HE 443-875
U22	FD1797B02	HE 443-997
U23	74LS20	HE 443-798
U24	74LS138	HE 443-877
U25	74LS27	HE 443-800
U26	74S74	HE 443-900
U27	74LS00	HE 443-728
U28	74LS02	HE 443-779
U29	74LS688	HE 443-971
U30	74LS273	HE 443-805
U31	74LS365A	HE 443-1039
U32	7417	HE 443-72
U33	74LS244	HE 443-791
U34	74LS244	HE 443-791
U35	74LS374	HE 443-863
U36	74LS244	HE 443-791

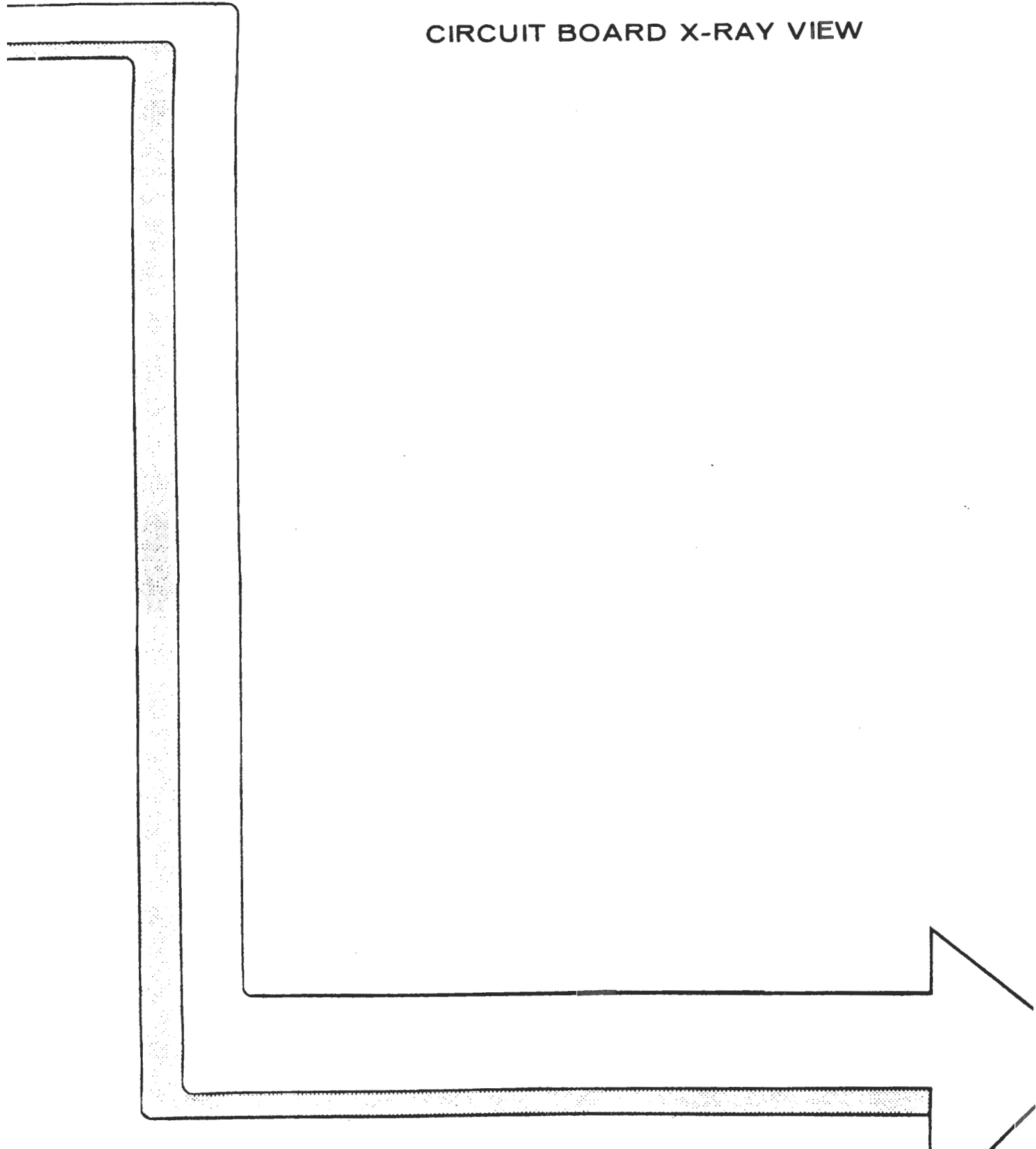
CIRCUIT DESCRIPTION  
Comp. No.

HEATH Part No.

## CALIBRATION CIRCUIT BOARD

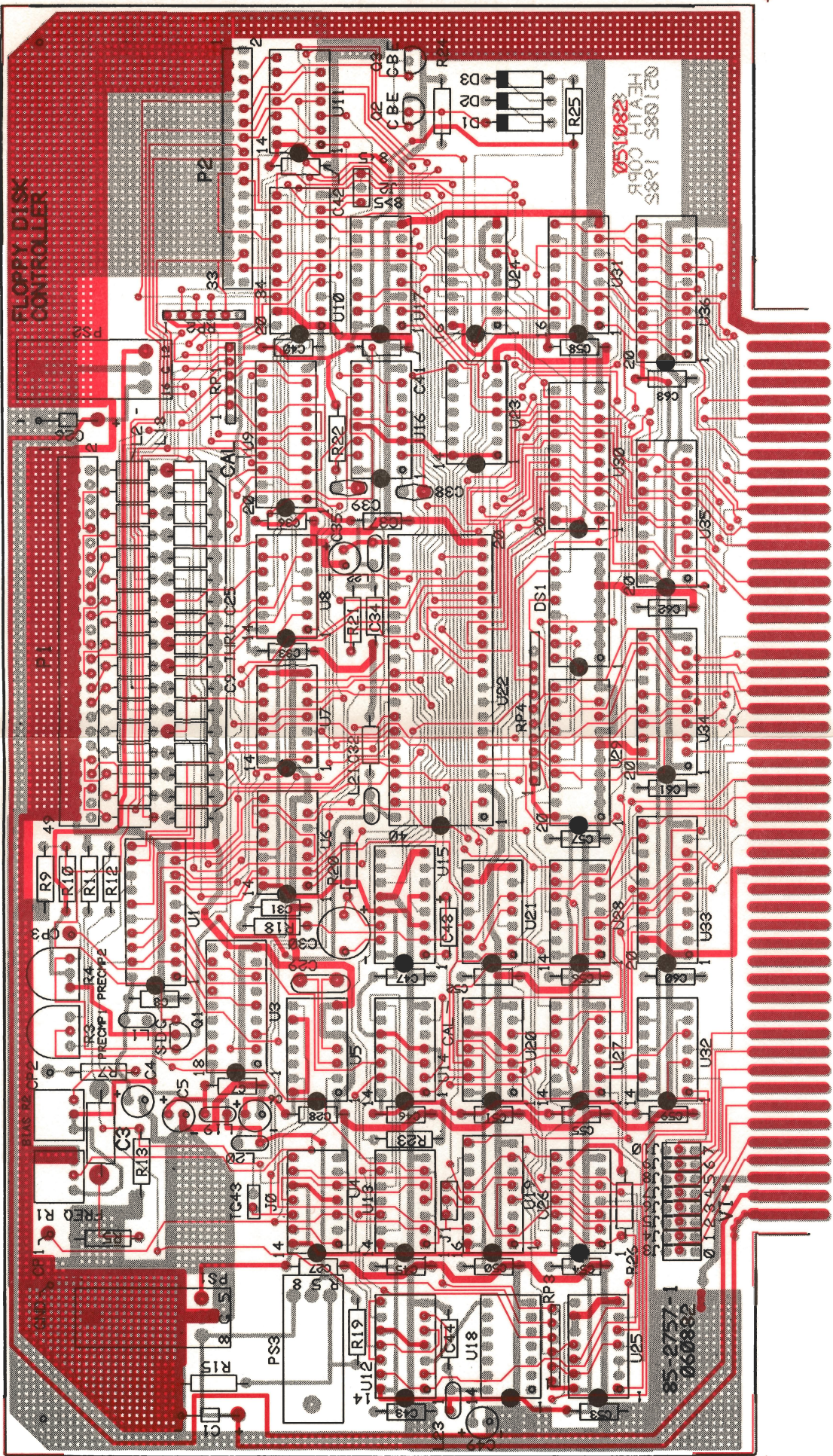
CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
<b>OTHER CIRCUIT COMPONENTS</b>		
D1	1N4148 diode	HE 56-84
D2	1N4148 diode	HE 56-84
D3	1N4148 diode	HE 56-84
DS1	8-section slide switch	HE 60-621
Q1	TIS74 transistor	HE 417-246
Q2	MPS2369 transistor	HE 417-937
Q3	MPS2369 transistor	HE 417-937
<b>CONNECTORS - SOCKETS</b>		
P1	50-pin right-angle connector	HE 432-1197
P2	34-pin right-angle connector	HE 432-1053
P3	40-pin IC socket	HE 434-253
P4	20-pin IC socket	HE 434-311
P5	18-pin IC socket	HE 434-310
P6	16-pin IC socket	HE 434-299
P7	14-pin IC socket	HE 434-298
P8	8-pin inline IC socket	HE 434-230
P9	1-pin connector	HE 423-121
<b>HARDWARE</b>		
U501	#4 lockwasher	HE 254-9
U502	4-10 nut	HE 252-2
	4-40 x 5/16" screw	HE 250-213
<b>MISCELLANEOUS</b>		
	Heat sink	HE 215-669
	H-207 manual	HE 595-2909
	PC board	HE 85-2757-2
	Silicone grease	HE 352-13
	S-100 circuit board extractor	HE 266-1203
	Wire, solid	HE 340-8
	Wire, white solid	HE 344-59
R501	10 kilohm 1/4 watt, 5%	HE 6-103-12
R502	330 ohm 1/4 watt, 5%	HE 6-331-12
C501	.1 uF ceramic	HE 21-762
DL501	Delay line	HE 41-10
	Alligator clip insulator	HE 73-34
	PC board	HE 85-2800-1
	Alligator clip	HE 260-16
	Wire, black stranded	HE 344-90
	Wire, red stranded	HE 344-92
	Wire, white stranded	HE 344-94
D501	LST5053 LED	HE 412-640
	1-pin socket	HE 432-120
	14-pin IC socket	HE 434-298
U501	74LS00	HE 443-728
U502	74LS74	HE 443-730

CIRCUIT BOARD X-RAY VIEW





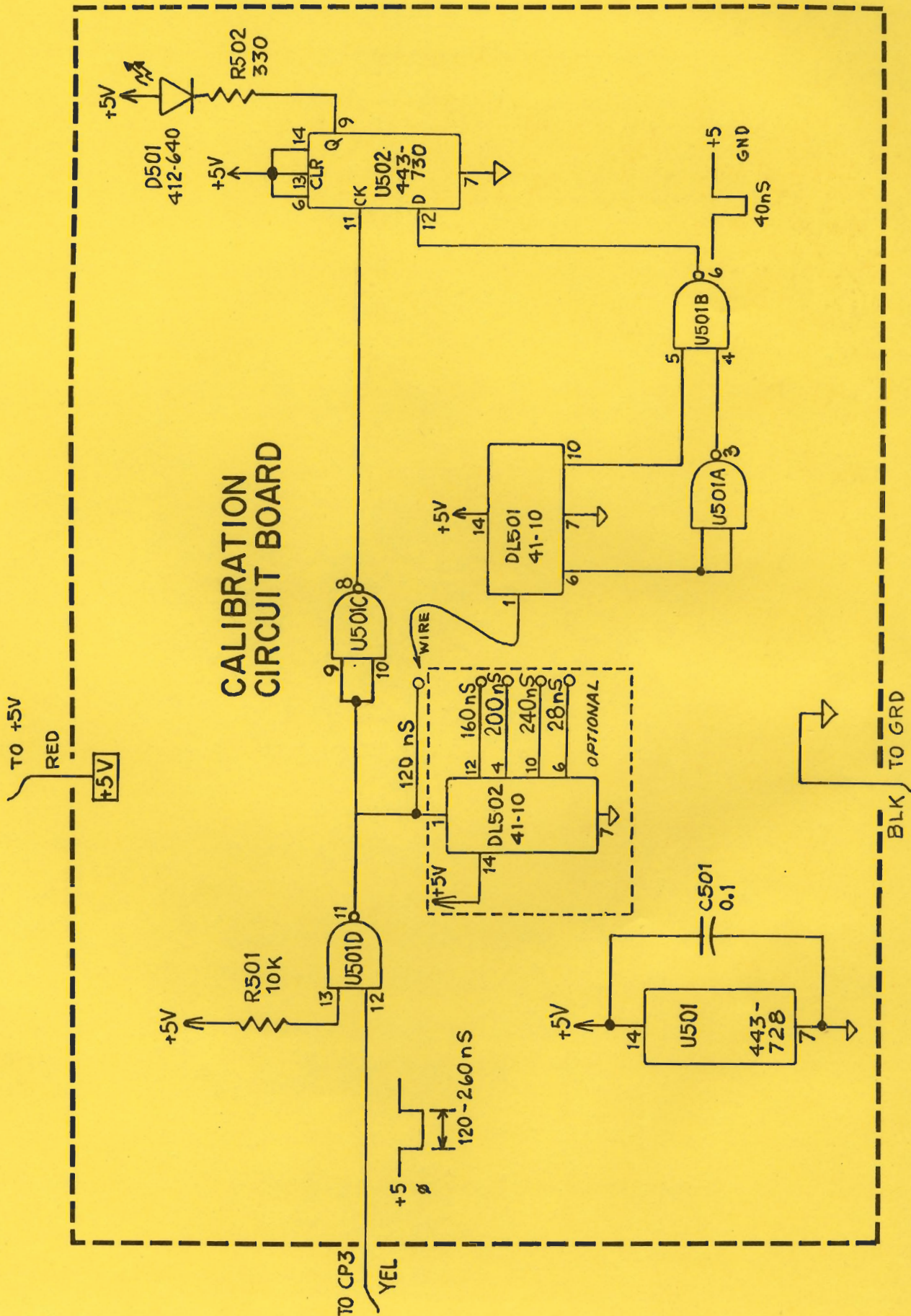




DISK CONTROLLER CIRCUIT BOARD (#HE-85-2757-1)

(SHOWN FROM COMPONENT SIDE)





# VIDEO MONITOR

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