MODEL 450

USER'S MANUAL

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SECTION 1: SPECIFICATIONS

1.0 GENERAL

The Xylogics Model 450 Disk Controller interfaces up to four SMD interface disk drives to IEEE P796 Multibus systems. The 450 implements data transfers via Direct Memory Access (DMA), allowing maximum throughput; it implements system control via Input/Output Parameter Blocks (IOPBs) and byte Input/Output (I/O) Registers. The 450 circuitry includes two sequencers, and a microprocessor for control.

1.1 USING THIS MANUAL

This manual provides two System Software Reference Cards for fast reference of the IOPB structure and codes (See insert). Sections 2.1 and 2.6 give a good overview of the 450's programming procedures. Section 2.3 describes the 450's registers; Section 2.4 describes the IOPB; and Section 2.5 describes the 450's commands. Section 3 details how to install and test the 900-450-9xx series 450 controller; Section 4 details how to install the 902-450-9xx series 450; and Section 5 details certain 450 maintenance aids.

1.1.1 Abbreviations

This manual uses the following mnemonics:

CDC	Control Data Corporation
CMD	Cartridge Module Drive
CPU	Central Processing Unit and/or Computer
CSR	Control and Status Register
DMA	Direct Memory Access
ECC	Error Correction Code
ESD	Embedded Servo Drive
FIFO	First In / First Out Buffer
H	Notation For Numerical Values Expressed In Hexadecimal
(H)	A High Level Active Signal
IOPB	Input / Output Parameter Block
I/O	Input / Output
KB	Kilobyte
KBS	Kilobytes Per Second
(L)	A Low Level Active Signal
LED	Light Emitting Diode
LMD	Lark Module Drive
MB	Megabyte
MBS	Megabytes Per Second
PCB	Printed Circuit Board
RAM	Random Access Memory
ROM	Read Only Memory
SMD	Storage Module Drive

1.2 DESIGN RELIABILITY

Xylogics implements the following features to minimize the likelihood (and expense) of product failure:

- o Low parts count, through microprogramming.
- o Low-power Schottky integrated circuits.
- o Low-stress design on all components.
- o All components burned-in.
- o One card; resides in backplane or expansion chassis.
- o Controller is power-cycled under thermal stress during test.

1.3 PHYSICAL

Packaging — The 450 completely resides on one printed circuit board (PCB). It plugs into any 16, 20 or 24-bit Intel Multibus or IEEE P796 card cage.

Dimensions — 12-inch length x 6.75-inch height (30.48 cm X 17.15 cm); the 450 is identical in form-factor to the standard Intel Multibus, and IEEE P796 printed circuit board (PCB).

Shipping Weight — 3 pounds (1.4 kg).

1.4 ENVIRONMENTAL

The Model 450 Disk Controller environmental requirements are similar to the Intel 86/12 SBC or equivalent Multibus processors (typically 0-55°C; up to 90% relative humidity without condensation). The 450 requires sufficient air circulation for cooling.

1.5 ELECTRICAL

Power — The 450 requires 6.2 Amperes at +5 Volts DC and 1.0 Ampere at -5 Volts DC. Optional on-board -5 VDC regulator requires 1.0 Amperes at -12 VDC.

Tolerance — Voltages must be within plus or minus five percent (4.75 to 5.25; -11.4 to -12.6 if the -5 VDC regulator option is installed).

Grounding — Common earth ground must be established between the disk drives and the CPU chassis, backplane, and expansion cabinets.

1.6 SYSTEM RELATED SPECIFICATIONS

Transfer Control — Direct Memory Access (DMA).

DMA Throttle Control — Programmable throttle value supports any Multibus throughput speed.

Interrupt Priority -- INT5/ standard; others jumper selectable.

1.6 SYSTEM RELATED SPECIFICATIONS (continued)

Interrupts — Non-bus vectored.

Control Technique -- Channel Driven Control — Programmable microprocessor.

Addressing Capability -- 16, 20 and 24-bit.

Controller I/O Parameter Block (IOPB) Length — 24-bytes.

Controller Registers — Six 8-bit I/O Registers; byte addressable only.

I/O Addressing Capability -- The 450 decodes byte addresses for its on-board registers. It responds to 8 or 16-bit I/O addresses.

Data Transfer Modes — The 450 transfers data in bytes or words.

Data Buffering — On-board FIFO memory accomodates 2K-bytes in Word mode and 1K-bytes in Byte mode. Optional buffer accomodates 8K-bytes.

Data Transfer Limit — Data transfer length, from 1 to 65,535 sectors.

Software Support — Standard software drivers supplied for use in UNIX[1] or RMX-86[2] based systems (source included).

Diagnostic Support — Comprehensive set of stand-alone diagnostics written in 'C' are available.

Test Station — The XYCAT Customer Acceptance Tester supports the 450 with stand-alone diagnostics for incoming inspection and field testing of the controller. This is a single Multibus 68000-based board with CPU, RAM and ROM-based diagnostics.

Error Detection and Correction — The 450 uses a 32-bit ECC word. Software controls automatic detection and correction.

Status LEDs — The 450 implements two status LEDs. L1 indicates successful completion of on-board diagnostics; L2 indicates the controller is active.

DMA Data Transfer Rate — The 450 adds less than 500 nanoseconds (ns) overhead on each word it transfers. Assuming 500 ns memory, the total transfer time is approximately 1000 ns for a DMA rate of approximately 2.0 MBS. With 300 ns memory, the 450 DMAs at approximately 2.5 MBS.

Overlap Seek Capability -- When chained IOPBs request more than one drive, the controller may initiate implicit overlap seeking.

Bit Cell Time — 62 ns, minimum.

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1. UNIX is a trademark of Western Electric.
2. RMX-86 is a trademark of Intel Corporation.

1.6 SYSTEM RELATED SPECIFICATIONS (continued)

Disk Data Transfer Rate — Continuous transfers at disk speeds of up to 2.0 MBS.

Cabling — Standard SMD flat cabling.

Dual Port — The 450 supports dual port drives.

Defective Sectors — System software may slip defective sectors to spare sectors on each track.

Read Defect Map Feature — The 902-450-9xx series 450 controller can read the manufacturer's defect information directly from the disk.

1.7 DISK DRIVE RELATED SPECIFICATIONS

Disk Interface — Storage Module Drive (SMD) and SMD+ (up to 2.0 MBS).

Maximum Disk Capacity — More than 2.4 Gigabytes of on-line storage (drive limitation).

Number of Disk Drives — The 450 supports up to four disk drives, including any mix of capacities or speeds.

Disk Sector Format — The 450 sector format includes a header field separated from a data field by a splice area.

Header Format — Header contains sector, Head, cylinder address, Drive Type and header ECC. The 450 only writes headers once during formatting.

Data Verification — Built-in 32-bit ECC word exists on the header and data portions of the sector. The ECC word detects and corrects error bursts up to 11-bits long, assuring data integrity.

Implied Seek Capability — Data transfer instructions contain an Implied Seek command. Data transfers cross sector, head, and cylinder boundaries as required (spiral read/write).

1.8 PROGRAMMABLE FEATURES

- Software Controlled 16 or 20/24-bit Address Bus Support.
- Jumper Selectable 20 or 24-bit Extended Address Bus Support.
- Software Controlled 8 or 16-bit Data Transfers.
- Software Controlled Interrupt or Software Polled Operation.
- Software Programmable DMA Throttle.
- Software Programmable Drive Size Parameters.
- Sector Interleaving — Standard 1:1; Software Programmable.

1.8.1 450 Internal Registers

Section 2.3 describes the use of specific bits within the 450 I/O Registers. The software driver establishes commands by loading and reading the 450's internal registers (See Table 2-1).

1.8.2 I/O Parameter Block

Section 2.4 describes the use of specific bits within the IOPB. Table 2-2 lists the IOPB formats.

1.8.3 Command Technique

The 450 command technique allows command-chaining and concurrent host and disk controller operations. Channel control allows a software driver to establish a disk command and parameters in an I/O Parameter Block (IOPB) in system memory. The software driver initiates commands or command chains by loading the memory address of the first IOPB in the chain into the 450 Relocation and Address Registers. It then sets bit 7 (GBSY) in the Control and Status Register (CSR), which remains set until the 450 completes the command chain or an error occurs.

The 450 reads the command IOPB from system memory by Direct Memory Access (DMA) and performs the required function. When the 450 completes an IOPB, or detects an error, it writes the status and a Completion Code into Bytes 2 and 3 of the related IOPB. At any time, system software may reset the 450 by reading the Controller Reset/Update Register.

1.8.4 Chained Commands

The 450 provides inherent command-chaining capability for complex operations. The software driver sets up a string of commands (e.g., disk-to-disk copy) which execute a series of disk operations without operating system intervention. At any time, system software can use the Attention protocol to add new IOPBs and/or remove completed IOPBs from the chain. Overlap Seek operations may be implemented in multidrive systems by setting the CHEN and Extended Function bits.

SECTION 2: PROGRAMMING REFERENCE

2.0 GENERAL

This section describes programming procedures for the Xylogics Model 450 Disk Controller. The 450 easily interfaces many different processors with a wide variety of disk drives.

2.1 PROGRAMMING TECHNIQUES

Set up the 450 commands by preparing an I/O Parameter Block (IOPB) in system memory. Initiate a command by loading the IOPB address into the 450's registers and setting the Go/Busy (GBSY) bit in the CSR. GBSY remains set until the controller completes all the commands in the IOPB chain, or a hard error occurs. When the 450 completes a command, it writes the corresponding status and Completion Codes into Bytes 2 and 3 of the completed IOPB in system memory. Table 2-2 lists the bytes in an IOPB.

The IOPB, located in system memory, passes command level information between the 450 and the CPU. The CPU writes and reads the IOPB with normal byte or word instructions. The 450 reads and writes the IOPB in Byte mode.

System software builds an IOPB in system memory with the appropriate information and then passes the IOPB address by loading the first four I/O Registers. The software driver then sets the GBSY bit in the CSR. The 450 transfers the IOPB from memory to its RAM at the start of a command. It then processes the command and resets GBSY on completion. While processing the command, the 450 may access the IOPB again and it may also DMA data to or from memory. Software may chain IOPBs together. Command-chaining allows the 450 to initiate Overlap Seek operations on multiple drives, and execute data transfers without operating system intervention.

Each byte in the IOPB has an address relative to the Command byte. Reserve all 24 bytes of allowable IOPB space to maintain IOPB integrity.

2.2 MULTIBUS ADDRESS RELOCATION

The 450 uses a technique called Address Relocation to access Multibus memory. Address Relocation is the addition of two addresses to form a larger physical address. The 450 supports two types of Address Relocation: 20-bit relocation and 24-bit relocation. Use either type of relocation when specifying 16-bits of memory address. Load the Relocation Register with zero for 16-bit memory addressing. A jumper on the 450 board selects either 20 or 24-bit relocation. Bit 3 (ADMD) in the CSR indicates the Addressing mode (if set, the board is jumpered for 24-bit relocation).

NOTE

This manual refers to both IOPB relocation and data relocation. Do not confuse them. IOPB relocation refers to the address at which the IOPB resides in memory. Data relocation refers to the address at which the data buffer exists. Data relocation may be affected by bit 6 (RELO) of Command Byte 0, but IOPB relocation is not. The jumper for 20/24-bit address selection affects Address Relocation for both data and IOPBs.

2.2.1 20-Bit Address Relocation

The 450 forms a 20-bit physical address by adding a 16-bit Address word to a shifted 16-bit Relocation word. The Relocation word shifts by four bits (See Figure 2-1A).

2.2.2 24-Bit Address Relocation

The 450 calculates a 32-bit physical address for 24-bit Address Relocation. The Address word comprises the least significant 16 bits, and the Relocation word comprises the most significant 16 bits. When addressing memory, the 450 only uses the lower 24 bits of the physical address (See Figure 2-1B).

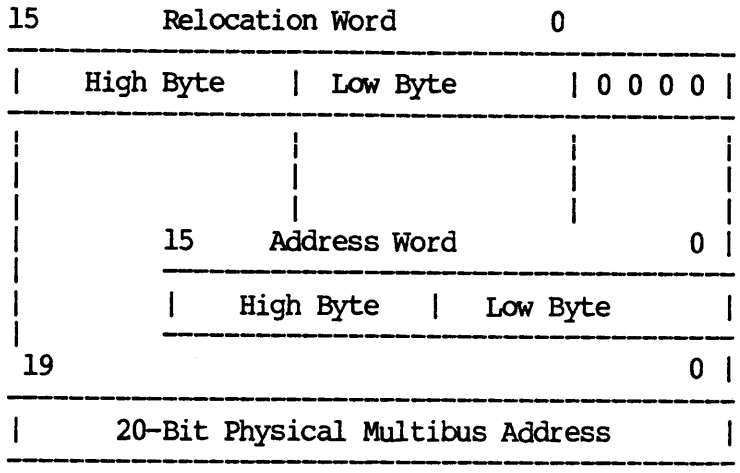


Figure 2-1A. 20-Bit Multibus Address Relocation

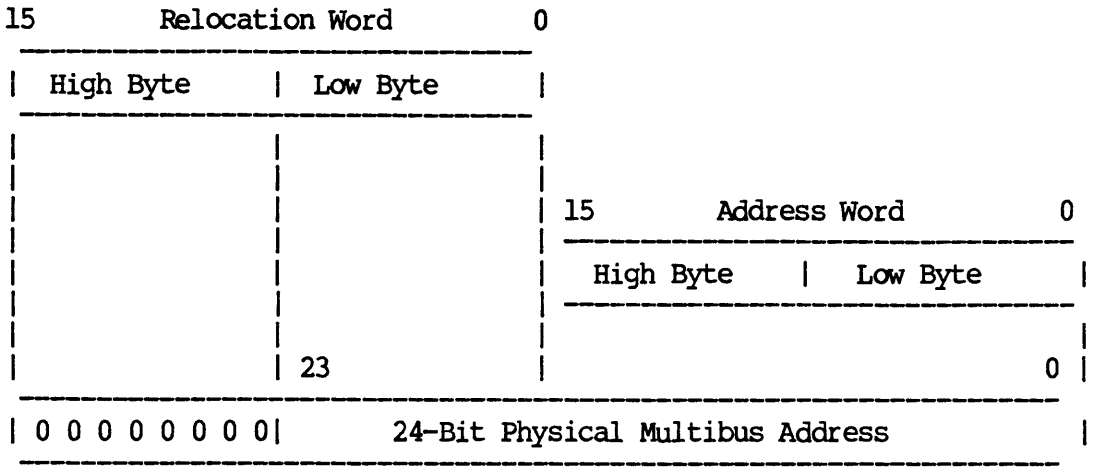


Figure 2-1B. 24-Bit Multibus Address Relocation

FIGURE 2-1. MULTIBUS ADDRESS RELOCATION

2.2.3 IOPB Address Relocation

IOPB relocation occurs whenever a non-zero value is loaded into the IOPB Relocation Registers. The IOPB Address Registers and IOPB Relocation Registers combine to form a 20-bit or 24-bit physical memory address (See Figure 2-1).

When chaining IOPBs, the 450 uses the IOPB Relocation Registers along with the Next IOPB Address bytes to form a new 20-bit or 24-bit physical Multibus address. This address points to the next IOPB in the chain. All IOPBs in a chain must reside in the same 64K-byte segment whose base address is in the Relocation Registers. The 450 computes the base address by shifting the Relocation Registers 4 or 16 bits to the left, depending on the Relocation mode (See Figure 2-1).

2.2.4 Data Transfer Address Relocation

IOPB Bytes C, D, E and F specify the starting memory address for a data transfer operation. If RELO is clear, the Data Address bytes (IOPB Bytes C and D) specify the physical Multibus address for the transfer. If RELO is set, the 450 uses Bytes E and F as the Data Relocation bytes, and Bytes C and D as the Data Address bytes. Data relocation occurs in the same manner as IOPB relocation (Figure 2-1 illustrates how the 450 determines data relocation addresses).

2.3 450 I/O REGISTERS

STANDARD I/O ADDRESSES (HEX)

USE	8-Bit	16-Bit
IOPB Relocation Register Low Byte	40	EE40
IOPB Relocation Register High Byte	41	EE41
IOPB Address Register Low Byte	42	EE42
IOPB Address Register High Byte	43	EE43
Control and Status Register (CSR)	44	EE44
Controller Reset/Update Register	45	EE45

TABLE 2-1. 450 INPUT/OUTPUT REGISTERS

2.3.1 450 I/O Register Addressing

The 450 Input/Output Registers are addressed as input-output byte ports on the Multibus. The I/O Registers use a standard base address of 40H or EE40H. Table 2-1 summarizes the 450 I/O Registers (See Section 3.2.1 for alternate base addresses).

2.3.2 450 I/O Register Definitions

2.3.2.1 Relocation Registers

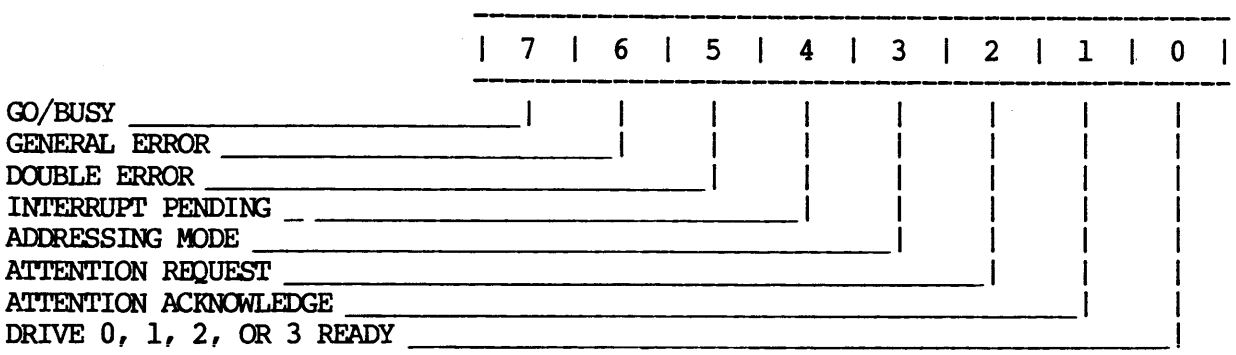
There are two Relocation Registers: one contains the low byte of the relocation address, the other contains the high byte. The two Relocation Registers are the most significant portion of the IOPB memory address. The 450 clears these registers on power-up. Set them to zero when using 16-bit addresses (writing anything but zero to these registers causes IOPB relocation). Figure 2-1 illustrates how the 450 determines 20 and 24-bit addresses.

2.3.2.2 Address Registers

There are two Address Registers: one contains the low byte of the IOPB address, the other contains the high byte. These registers are the least significant portion of the IOPB memory address. The 450 clears these registers on power-up.

2.3.2.3 Control and Status Register

Control and Status Register — (I/O Address 44 or EE44)



BIT	MNEMONIC	ACCESS	MEANING
7	GBSY	R/W	GO/BUSY - Set it to start a transfer. When set, it indicates the 450 is busy executing a command. GBSY remains set until the 450 completes the current IOPB command or command chain. The 450 then clears GBSY to show readiness for another IOPB operation. Only GBSY, IPND and AACK are valid while the 450 is busy. When clear, the controller is ready to perform another function.
6	ERR	R/W	GENERAL ERROR - Sets when the 450 encounters a hard error and terminates the command execution. Clear this bit before executing another command (write a "1" to ERR [Error Reset] or execute a Controller Reset). ERR only sets on fatal errors. ERR is only valid if GBSY is clear. When clear, the last IOPB did not end in a hard error.

2.3.2.3 Control and Status Register (continued)

BIT	MNEMONIC	ACCESS	MEANING
5	DERR	R	DOUBLE ERROR - When set, indicates an error occurred and a previous error condition has not been cleared. This usually means the 450 cannot properly DMA the Status bytes to memory as a result of an error. Executing an Error Reset or a Controller Reset clears a single or double error. DERR is only valid if GBSY is clear. If DERR is clear but ERR is set, a single error occurred (STAT2 contains the appropriate Completion Code).

NOTE

It is more efficient to clear an error on the 450 by executing an Error Reset (writing a "1" to the ERR bit) than by executing a Controller Reset. Clearing an error by executing a Controller Reset is supported for 440-compatibility (a Controller Reset requires up to 90 microseconds to complete; an Error Reset completes in 30 microseconds).

4	IPND	R/W	INTERRUPT PENDING - Sets when an IOPB is complete, the 450 has interrupted, and the interrupt has not been serviced. Clear this condition before executing another command (except IOPB update) by executing an Interrupt Reset (write a "1" to the IPND bit) or by executing a Controller Reset. System software may only write IPND and AREQ in the CSR while the 450 is busy. IPND is always valid.

NOTE

It is more efficient to acknowledge an interrupt by executing an Interrupt Reset than by executing a Controller Reset. Acknowledging an interrupt with a Controller Reset is supported for 440-compatibility (a Controller Reset requires approximately 80 microseconds to complete; an Interrupt Reset completes in approximately 30 microseconds).

3	ADRM	R	ADDRESSING MODE - Sets when the 450 is in 24-bit Addressing mode. Clear indicates the 450 is in 20-bit Addressing mode. A hardware jumper on the 450 board selects the Addressing mode; it is not software selectable (See Section 3.2.2).

2.3.2.3 Control and Status Register (continued)

BIT	MNEMONIC	ACCESS	MEANING
2	AREQ	R/W	ATTENTION REQUEST - System software sets AREQ (to gain the attention of the 450 when it is busy processing commands) and waits until the 450 acknowledges the request with AACK. After the 450 sets AACK, system software may remove completed IOPBs and/or add new IOPBs. When System software completes work on the IOPB chain, it clears AREQ, and the 450 clears AACK and resumes operation.
1	AACK	R	ATTENTION ACKNOWLEDGE - The 450 sets AACK to acknowledge an AREQ by system software. The 450 may complete the current IOPB in process before it sets AACK. The 450 clears AACK after system software clears AREQ. If IEI and IEN are set, the 450 generates an interrupt after it sets AACK.
0	DRDY	R	DRIVE READY - The 450 sets DRDY when the last drive selected is Ready/On-cylinder. The 450 updates this status after a Controller Reset. When clear, the drive is either not ready or not on-cylinder.

NOTE

While the controller is busy, only bits 2 and 4 of the CSR have write access to the 450's registers. Any other access attempts result in a Busy Conflict error.

2.3.2.4 Controller Reset/Update Register (I/O Address 45 or EE45)

This special register performs the following functions:

1. The 450 executes a Controller Reset when it reads the Controller Reset/Update Register (i.e., the 450 clears the registers along with IPND, ERR and DERR; reselects the last selected drive (if none, Drive 0), latches the Ready status, and releases the drive). A Controller Reset does not release all previously reserved dual port drives. GBSY remains set during a Controller Reset operation.

2.3.2.4 Controller Reset/Update Register (continued)

2. When the 450 writes the Controller Reset/Update IOPB Register (actual data written is insignificant), it updates the IOPB whose address is currently stored in the Address and Relocation Registers. The Update IOPB command writes the information contained in the 450's internal registers to the current IOPB. Writing this register causes GBSY to set until the update is complete.

   After the 450 completes an IOPB, the Update function updates the IOPB to reflect the final disk and data address. The updated IOPB also reflects the final sector count, and any ECC error. The sector count and the Completion Code are zero if the 450 successfully completes an IOPB.

2.3.3 Register Response

The time required to read or write registers is approximately 400 ns. After any write to a register, the on-board microprocessor updates the information in its own RAM. A read or write to a 450 register immediately following a write to any register, or a read from the Reset/Update Register, causes the 450 to delay its response to the second transfer.

This delay, required by the microprocessor, is less than 20 microseconds for an Address Register write. Writing the CSR and reading or writing the Reset/Update Register requires up to 100 microseconds. The delay starts after a write to any register or a read from the Reset/Update Register, and does not use any bus time unless another register is accessed before the delay ends.

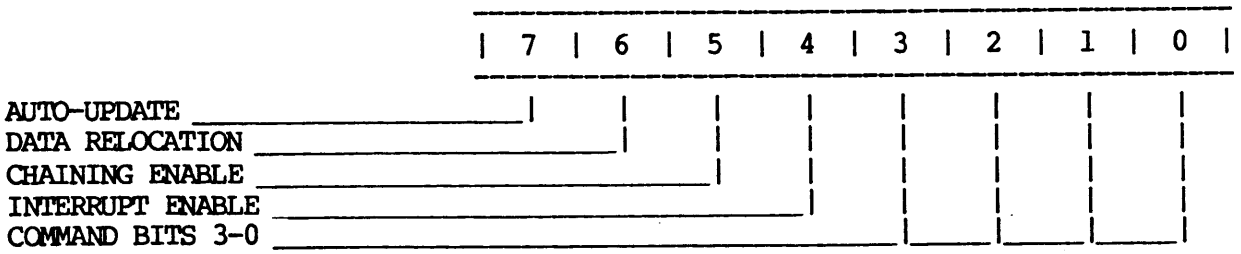
2.4 IOPB DESCRIPTION

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	AUD	RELO	CHEN	IEN	Command Code			
1 - IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
2 - STAT1	ERRS	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	B/W	Interleave Factor				Throttle		
5 - DRIVE	Drive Type		AFE	0			Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0					Cyl. Addr. High		
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	ESD	EHDT	Head Offset					
11 - SUBFUN	Subfunction Code							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High				0			
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

FIGURE 2-2. 450 IOPB FORMAT

2.4.1 Command Byte (IOPB Byte 0)

Command Byte -- (COMM)



BIT	MNEMONIC	MEANING
7	AUD	AUTO-UPDATE - When set, the 450 updates the current IOPB upon its completion. The Sector, Head, Cylinder, Sector Count and Data Address bytes reflect the result of IOPB execution. When clear, the 450 only updates Status Bytes 1 and 2. Typically, AUD is set.
6	RELO	RELOCATION - If clear, the 450 generates Multibus data addresses as 16-bit values, sets bits 16 through 23 to zero, and ignores the Data Relocation Address bytes. If set, software forms 20 or 24-bit physical Multibus addresses (See Figure 2-1).
		NOTE RELO only controls data relocation. IOPB relocation occurs whenever the IOPB Relocation Registers are non-zero.
5	CHEN	CHAINING ENABLE - If clear, the 450 executes the current IOPB and clears GBSY upon completion. If set, the 450 starts processing the next IOPB. The Next IOPB Address bytes and the Relocation Registers specify the new IOPB address. If the Extended Function bit is set, the 450 optimizes transfers by examining all chained IOPBs and performing any possible Overlap Seek operations.
4	IEN	INTERRUPT ENABLE - If clear, the 450 does not generate interrupts. If set, the 450 generates a hardware interrupt, and sets IPND in the CSR, after completing a single IOPB in Non-chain mode, or after completing a chain of IOPBs in Chain mode. If IEI and IEN are set, the 450 interrupts after it completes each IOPB, or when it sets AACK during an Attention protocol.

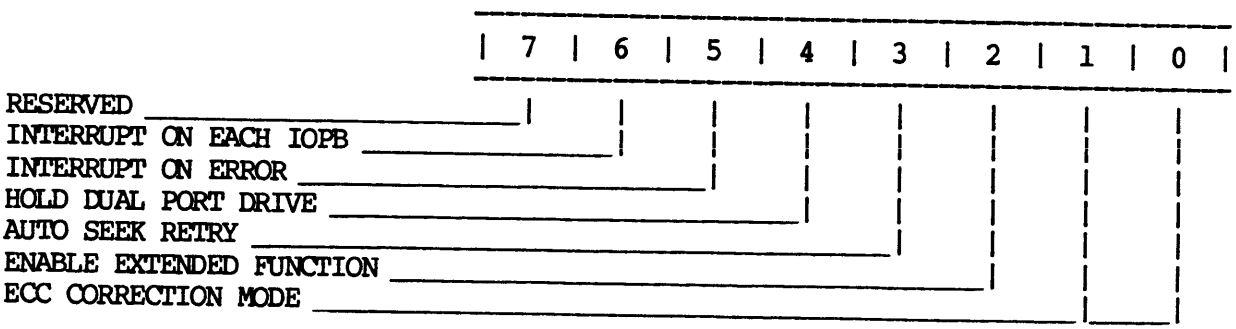
2.4.1 Command Byte (continued)

BIT	MNEMONIC	MEANING
3-0	COM	COMMAND - Interpret as follows (See Section 2.5):

Hex Value	Command
0	No Operation (NOP)
1	Write
2	Read
3	Write Track Headers
4	Read Track Headers
5	Seek
6	Drive Reset
7	Write Format
8	Read Header, Data, and ECC
9	Read Drive Status
A	Write Header, Data, and ECC
B	Set Drive Size
C	Self Test
D	DMA Test
E	Maintenance Buffer Load
F	Maintenance Buffer Dump

2.4.2 Interrupt Mode / Function Modification (IOPB Byte 1)

Interrupt Mode / Function Modification — (IMODE)



BIT	MNEMONIC	MEANING
7		RESERVED.
6	IEI	INTERRUPT ON EACH IOPB - When interrupts are enabled, and IEI is set, the 450 interrupts each time it completes an IOPB, or after it sets AACK in the CSR.
5	IERR	INTERRUPT ON ERROR - IERR is provided for 440-compatibility and has no effect on the operation of the 450.
4	HDP	HOLD DUAL PORT DRIVE - On a dual port drive, setting HDP prevents the 450 from releasing the drive after it completes an IOPB. When clear, the 450 releases the drive after each IOPB.

2.4.2 Interrupt Mode / Function Modification (continued)

BIT	MNEMONIC	MEANING
3	ASR	AUTO SEEK RETRY - Enables the 450 to recalibrate the drive once on either a Drive Fault, or a Hard Seek error, and to retry the transfer. If an Auto Seek Retry is successful, the 450 returns the Completion Code 13H.
2	EEF	ENABLE EXTENDED FUNCTION - When set, enables Commands 3, 4, and overlap seeking. When clear, the 450 does not initiate overlap seeks.
1,0	ECM	ECC CORRECTION MODE

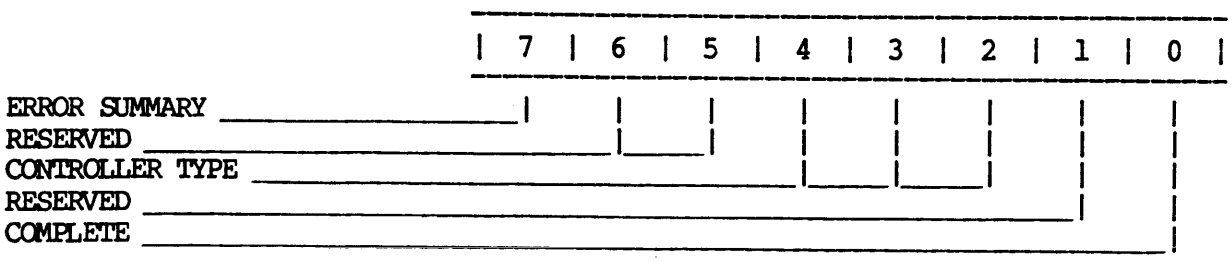
Mode	450 Action on Error
0	o Provides an ECC pattern and offset. o Stops a chained transfer (fatal error). o Reports an ECC error status (1EH or 06H). o Loses at least one revolution.
1	o Does not correct or flag an error. o Continues a command chain (soft error only). o Does not lose a revolution.
2*	o Corrects error, if possible. o Updates IOPB with ECC error status (1FH or 06H). o Continues a command chain (soft error only). o Loses one revolution.
3*	o Does not correct an error. o Flags an ECC error (06H). o Continues a command chain. o Does not lose a revolution.

NOTE

Another error can mask soft errors that do not stop a transfer. For example, in a multisector transfer, the second sector has an ECC recovered error, the transfer resumes and the fifth sector has a Header Not Found error. In this case, the Header Not Found status writes over the ECC recovered error status.

2.4.3 Status Byte 1 (IOPB Byte 2)

Status Byte 1 -- (STAT1)



BIT	MNEMONIC	MEANING
7	ERRS	ERROR SUMMARY - Sets when a hard error occurs during IOPB processing. Clear indicates successful completion.
		NOTE ERRS does not set on a soft error, or on a ECC Mode 3 hard error.
6-5		RESERVED.
4-2	CTYP	CONTROLLER TYPE - Xylogics assigns each Multibus controller a Controller Type code as follows:

Bit 4	Bit 3	Bit 2	Controller
0	0	0	440
0	0	1	450
0	1	0	472

1		RESERVED.
0	DONE	DONE - Sets when the IOPB is complete; Status Byte 2 holds the Completion Code for the IOPB. If clear, the IOPB is incomplete.
		NOTE System software must clear (zero) Status Bytes 1 and 2 before giving the IOPB to the 450. If DONE is set, the 450 reads the IOPB and considers it complete (therefore, it cannot execute the IOPB again).

2.4.4 Status Byte 2 (IOPB Byte 3)

After the 450 executes the IOPB, Status Byte 2 contains its Completion Code. Table 2-3 summarizes the Completion Codes. The following sections describe Completion Codes, along with any required corrective action. Unless otherwise noted, executing either an Error Reset (writing a "1" to ERR) or a Controller Reset clears a hard error. Soft errors do not stop chained IOPB execution.

2.4.4 Status Byte 2 (IOPB Byte 3) (continued)

CODE	TYPE	DEFINITION
00	Status	Successful Completion
01	Hard	Interrupt Pending
02	-	Reserved
03	Hard	Busy Conflict
04	Hard	Operation Timeout
05	Hard	Header Not Found
06	Hard	Hard ECC Error
07	Hard	Illegal Cylinder Address Error
08,09	-	Reserved
0A	Hard	Illegal Sector Address
0B,0C	-	Reserved
0D	Hard	Last Sector Too Small
0E	Hard	Slave ACK Error (Non-existent Memory)
0F,10,11	-	Reserved
12	Hard	Cylinder and Head/Header Error
13	Soft	Seek Retry Required
14	Hard	Write-protect Error
15	-	Reserved
16	Hard	Drive Not Ready
17	Hard	Sector Count Zero
18	Hard	Drive Faulted
19	Hard	Illegal Sector Size
1A	Hard	Self Test A
1B	Hard	Self Test B
1C	Hard	Self Test C
1D	-	Reserved
1E	Hard	Soft ECC Error
1F	Soft	Soft ECC Error Recovered
20	Hard	Illegal Head Error
21	Hard	Disk Sequencer Error
22,23,24	-	Reserved
25	Hard	Seek Error

TABLE 2-3. SUMMARY OF COMPLETION CODES (IOPB BYTE 3)

2.4.4.1 Completion Code Descriptions

CODE DESCRIPTION

00 SUCCESSFUL COMPLETION — Not an error; the 450 successfully completed the command; software may remove the IOPB from the queue.

01 INTERRUPT PENDING ERROR — The 450 attempted an operation with a previous interrupt still pending. Only Interrupt Reset, Update IOPB, Controller Reset, or Error Reset operations are allowed while an interrupt is pending.

02 RESERVED.

2.4.4.1 Completion Code Descriptions (continued)

CODE DESCRIPTION

03 BUSY CONFLICT — A register write is attempted while GBSY is set. Only bits 2 and 4 in the CSR have write access while the 450 is busy.

04 OPERATION TIMEOUT — The 450 did not complete the IOPB within two seconds. The most common problems associated with this error are:

- o Dual port access is not available.
- o The drive failed to complete a seek.

05 HEADER NOT FOUND ERROR — The 450 did not find the requested sector. It reads other headers and determines if the head and cylinder are correct. Some possible causes include:

- o The requested Drive Type and the Drive Type in the header do not match. Verify and correct the Drive Type.
- o The header ECC does not match the header the 450 found.
- o If the Drive Type is correct and the error still occurs, try reformatting. If the error still occurs after reformatting, there may be a media defect in the header area. System software should slip the sector, or log the sector bad, and discontinue its use.
- o The actual number of physical sectors in the drive exceeds the maximum number of sectors plus 5. The 450 compares headers for the maximum number of sectors plus 5. Initiate a Read Drive Status command to determine the actual number of sectors per track, the Drive Type, and the maximum sector number (See Section 2.5.10). For example, if Drive Type 01 = 32 sectors + 5, then the 450 searches 37 sectors for header compare. If the drive has 47 actual sectors, the 450 may not compare 10 sectors for valid headers.

06 HARD ECC ERROR — Only occurs on a Read command when the 450 detects a data error in the data field longer than eleven bits, or when the ECC Correction mode is disabled (ECC Mode 3). Retry the previous Read operation. If the error still occurs, try writing the data onto the sector in question. If the error persists, system software should slip the sector, or log the sector bad, and discontinue its use.

07 ILLEGAL CYLINDER ADDRESS — Software specified a cylinder address greater than the maximum cylinder number allowed. Check the cylinder address and the drive parameters, then retry the operation.

08,09 RESERVED.

0A ILLEGAL SECTOR ADDRESS — Software specified a sector address greater than the maximum sector number allowed. Check the sector address and the maximum sector parameter for that Drive Type, then retry the IOPB operation.

0B,0C RESERVED.

2.4.4.1 Completion Code Descriptions (continued)

CODE DESCRIPTION

0D LAST SECTOR TOO SMALL — The very last sector (phantom or runt), or all the sectors, are too small to write a complete header. Check the drive sector switches (See Section 3.4.2).

0E SLAVE ACKNOWLEDGE ERROR (NON-EXISTENT MEMORY) -- The memory addressed by the 450 fails to respond. The microprocessor provides a 10 ms timeout for the DMA sequencer to perform up to 128 transfers. When the timer interrupts, the 450 tests to see if it is bus master. If it is, a Slave ACK Error occurs; if it's not, a Disk Sequencer error occurs. Validate the memory address or memory itself and retry the command.

0F-11 RESERVED.

12 CYLINDER AND HEAD/HEADER ERROR — The cylinder or head address read from the disk does not match the IOPB Cylinder and Head Address bytes. The following conditions may cause this error:

- o The disk drive fails to seek to the correct cylinder. Issue a Drive Reset and retry the operation.
- o The disk format is corrupt. Reformat the sector in question, rewrite the data for the sector, and retry the operation. If the error persists, system software should slip the sector or log the sector bad, and discontinue its use.
- o The Head byte written on the disk does not match the selected head address. This may be due to a bad format or a hardware problem.

13 SEEK RETRY REQUIRED — The 450 encountered a seek error. It automatically recalibrates the disk drive, clears the error, and completes the seek (See ASR in Section 2.4.2).

14 WRITE-PROTECT ERROR — The 450 attempted a Write operation on a drive which is write-protected. Turn off the write-protect and retry the Write operation.

15 RESERVED.

16 DRIVE NOT READY — The selected drive is not ready or possibly faulted. Issue a Drive Reset to the drive in question. If the drive does not become ready, check these possible causes:

- o Drive not up-to-speed, or hardware error.
- o Bad or improperly connected "A" cable.
- o No drive of the specified Unit Number is connected to the 450.
- o "ACLO" signal on the Multibus backplane P2 connector is low.
- o Dual port access may not have been granted.

17 SECTOR COUNT ZERO — Software issued the 450 an IOPB with a sector count of zero. All data transfer operations require a positive sector count. Correct the program in error and start the transfer again.

2.4.4.1 Completion Code Descriptions (continued)

CODE DESCRIPTION

18 DRIVE FAULTED — A fault exists in the selected disk drive. Issue a Drive Reset. If the fault persists, you must correct the drive fault.

19 ILLEGAL SECTOR SIZE — The drive sectoring does not allow enough room for the 450 to write the header and data fields (See Section 3.4.2):

- o The runt sector may be too small. For 1.2 MBS drives, the runt should include at least 100 bytes; for 1.9 MBS drives, it should include at least 150 bytes.
- o The drive has more sector pulses than the number of specified data sectors plus five.
- o The last sector is too small to be a data sector, but is included in the specified maximum sector. Adjust the drive to more sectors, or the Drive Type to fewer sectors.

1A SELF TEST A FAILURE — Either the microprocessor or its internal RAM failed diagnostics.

1B SELF TEST B FAILURE — Either the microprocessor or Header Shift Register failed diagnostics.

1C SELF TEST C FAILURE — The buffer RAM failed diagnostics.

1D RESERVED.

1E SOFT ECC ERROR — During a Read operation, in ECC Mode 0, the 450 detected a correctable 11-bit (or less) error in the data field of the current sector.

1F SOFT ECC RECOVERED ERROR — The 450 corrected one or more ECC errors, in ECC Mode 2, during the transfer.

20 ILLEGAL HEAD ADDRESS — Software specified a head address greater than the maximum head address allowed. The maximum head address varies for each Drive Type. Correct the Drive Type and the head address for the drive in use, and retry the operation.

21 DISK SEQUENCER ERROR — The disk sequencer did not finish its operation within the alloted time. Several factors may cause this problem (also see error 0E, Slave ACK):

- o The 450 did not receive the servo clock signal from the selected disk drive. Check the "B" cable; if the connection is good, try a different "B" cable port on the 450.
- o The 450 is not receiving any read data from the selected drive. Check the "B" cable.

2.4.4.1 Completion Code Descriptions (continued)

CODE DESCRIPTION

21 DISK SEQUENCER ERROR (continued)

o The Multibus may be preventing the 450 from gaining proper access.

22-24 RESERVED.

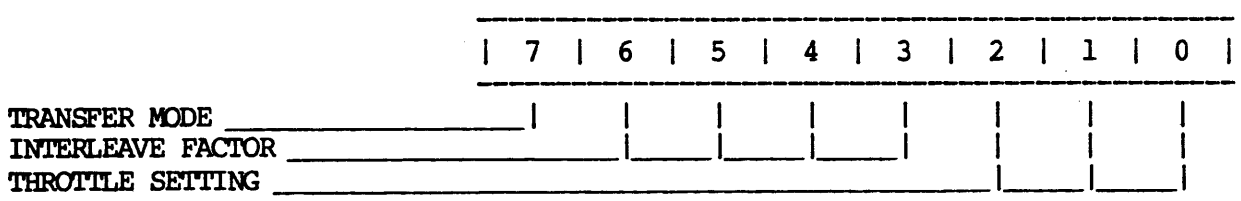
25 SEEK ERROR — Software selected a cylinder higher than the drive maximum, or selected a head beyond that supported by the drive. Check the drive parameters for the Drive Type you are using.

2.4.5 Throttle (IOPB Byte 4)

2.4.5.1 Throttle Byte Description

The Throttle byte selects the number of DMA cycles in a DMA burst, Word or Byte mode transfers, and the interleave factor.

Throttle — (IOPB Byte 4)



BIT	MNEMONIC	MEANING
7	BWM	TRANSFER MODE - Selects either word or byte DMA transfers between the 450 and system memory, allowing the 450 to operate with word and byte-oriented memory mixtures. Clear BWM when reading or writing 16-bit words in memory. Set BWM when reading or writing 8-bit bytes in memory. BWM does not affect IOPB DMA.
6-3	INTF	INTERLEAVE FACTOR - The 450 uses INTF during Format, Write Track Headers, and Write Header, Data, and ECC operations. For 1:1 interleaving, the interleave factor is zero. The interleave factor for other ratios is (n+1):1, where n is the interleave factor. When formatting interleaved, always format full tracks starting with Sector 0.

Interleave Factor Bits 6-3	Ratio
0	1:1
1	2:1
2	3:1
:	:
F	16:1

TABLE 2-4. 450 INTERLEAVE FACTORS

2.4.5.1 Throttle Byte Description (continued)

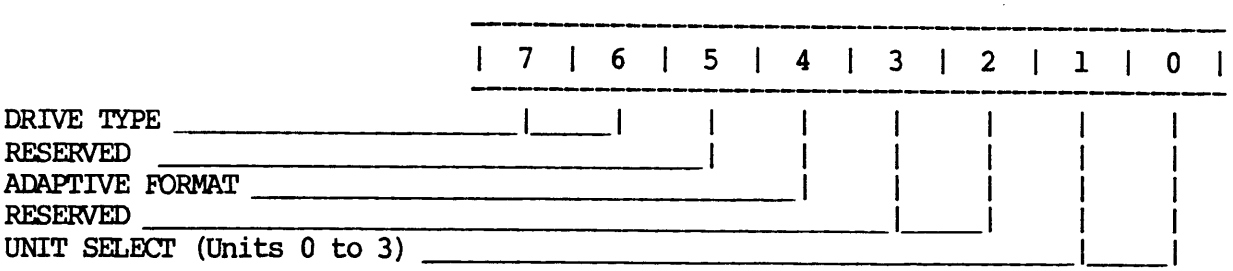
BIT	MNEMONIC	MEANING
2-0	THRO	THROTTLE SETTING - Selects the maximum number of DMA cycles the 450 executes each time it becomes bus master (See Table 2-4). The throttle value determines the DMA burst length for both data and IOPB DMA transfers.

Value of Bits 0-2	DMA Cycles
0	2
1	4
2	8
3	16
4	32
5	64
6	128
7	128

TABLE 2-5. 450 THROTTLE SETTINGS

2.4.6 Drive Type / Unit Select (IOPB Byte 5)

Drive Type / Unit Select — (IOPB Byte 5)



BIT	MNEMONIC	MEANING
7-6	DT	DRIVE TYPE - Selects a specific drive size. The Drive Type bits give software control of drives of mixed capacities, without regard to either the connecting 450 "B" cable port, or the drive's logical Unit Number. A Set Drive Size command specifies and defines the particular characteristics of a drive (such as head offset, max head, max sector, and max cylinder) for each Drive Type (See Section 2.5.12).
5		RESERVED.
4	AFE	ADAPTIVE FORMAT - Only valid with the Read Drive Status command. If set, the 450 is configured for 450-standard format; if clear, the 450 is configured for 440-compatible format (See Section 2.5.10).

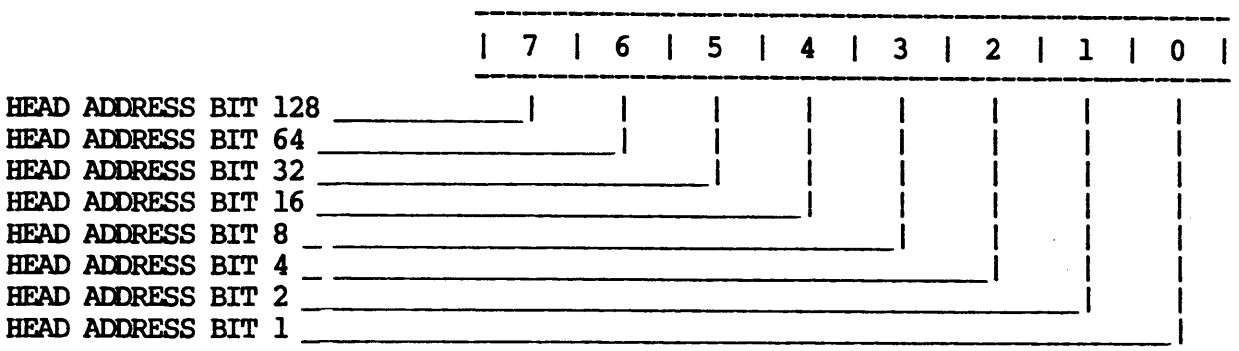
2.4.6 Drive Type / Unit Select (continued)

BIT	MNEMONIC	MEANING
3-2		RESERVED.
1-0	UNIT	UNIT SELECT - Contains the physical Unit Number of the disk drive to be accessed.

2.4.7 Head Byte (IOPB Byte 6)

The Head byte specifies the starting head number for a transfer. Head numbers start with zero. An Illegal Head Address error occurs if software attempts to access a head number larger than the maximum head.

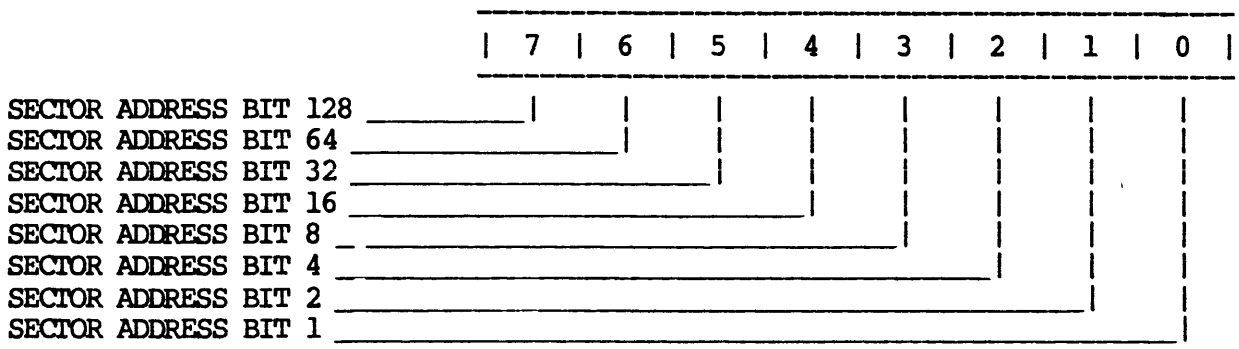
Head Byte — (IOPB Byte 6)



2.4.8 Sector Byte (IOPB Byte 7)

The Sector byte specifies the starting sector number for a transfer. All commands that read or write the disk use sector numbers.

Sector Byte — (IOPB Byte 7)



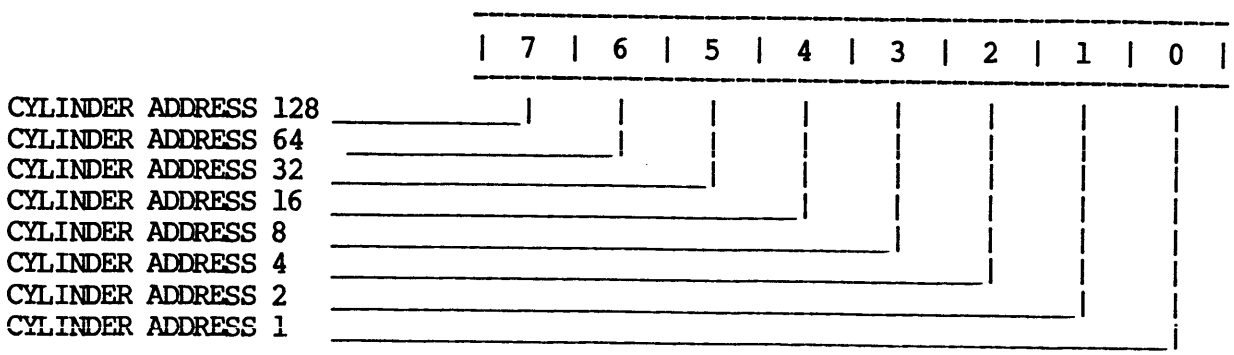
2.4.9 Cylinder Address (IOPB Bytes 8 and 9)

IOPB Bytes 8 and 9 specify the cylinder address. IOPB Byte 8 is the least significant portion of the cylinder address; IOPB Byte 9 is the most significant portion of the cylinder address.

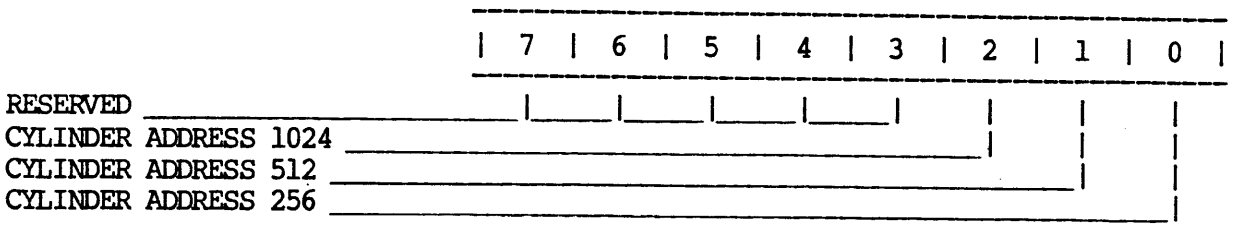
2.4.9 Cylinder Address (continued)

The cylinder address is an 11-bit binary number. The lowest cylinder address is zero; the largest cylinder address is the total number of cylinders minus 1.

Cylinder Address -- (IOPB Byte 8)



Cylinder Address -- (IOPB Byte 9)



2.4.10 Sector Count (IOPB Bytes A and B)

The 450 transfers information in whole sectors. The sector count, a 16-bit number stored as two bytes in the IOPB, is the number of sectors to be transferred. Byte A of the IOPB is the least significant half of the sector count; Byte B is the most significant half. With a 16-bit sector count the 450 transfers up to 65,535 sectors with one IOPB (memory permitting).

The 450 supports standard sector sizes of 256, 512, 1024, and 2048-bytes per sector. Special firmware handles custom sector sizes, ranging in even byte sizes from 256 to 4,096-bytes per sector.

2.4.10.1 Sector Count For Read Drive Status Command (IOPB Byte A)

On a Read Drive Status command, Byte A contains status information from the selected drive (See Section 2.5.10 for a detailed definition of this byte).

2.4.11 Data Address (IOPB Bytes C and D)

The data address comprises two bytes. Byte C is the Data Address Low byte; Byte D is the Data Address High byte. The data address is the starting memory address for a data transfer.

When RELO is set, the 450 adds the 16-bit data address to a shifted Data Relocation word to form the physical starting address for a data transfer (See Figure 2-1).

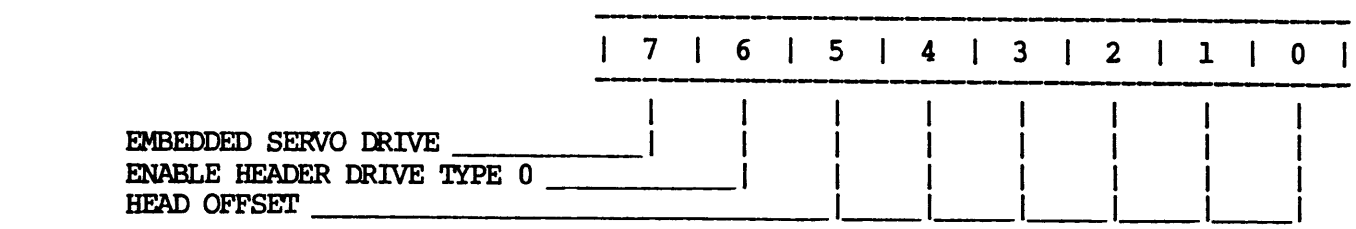
2.4.12 Data Relocation Pointer (IOPB Bytes E and F)

The data relocation pointer comprises two bytes in the IOPB. Byte E is the low byte, and Byte F is the high byte. When forming a physical address, the 450 uses the Data Relocation bytes and Data Address bytes to create Multibus addresses (See Figure 2-1). The 450 ignores the Data Relocation bytes if RELO (in the IOPB Command byte) is clear.

2.4.13 Head Offset / Embedded Servo Drive (IOPB Byte 10)

Only valid with Set Drive Size and Read Drive Status commands (See Section 2.5.10. Section 2.6.6.5 describes the Enable Header Drive Type 0 option).

Head Offset / Embedded Servo Drive — (IOPB Byte 10)



2.4.14 Subfunction Code (IOPB Byte 11)

The 450 combines Subfunction Codes with standard command codes to create new commands. The Read Defect Map command is currently the only command which uses a Subfunction Code (See Section 2.5.17).

2.4.15 Next IOPB Address (IOPB Bytes 12 and 13)

When using command-chaining, system software must specify the starting address of the next IOPB. The 450 combines Bytes 12 and 13 with the IOPB Relocation Registers to determine the Next IOPB Address. They are the missing links in the IOPB chain.

Byte 12 is the low byte, and Byte 13 is the high byte of the Next IOPB Address. These two bytes comprise a 16-bit address identical to the IOPB Address Register. The 450 adds the Next IOPB Address to the IOPB Relocation Register to form a physical address (See Figure 2-1). This physical address is 20 or 24-bits long, depending on the Addressing mode, and points to the next IOPB in the chain. All IOPBs in a chain are relative to the same relocation address, and must be within a 64K-byte block of memory. Setting CHEN in the Command byte of the IOPB enables command-chaining. The 450 ignores Bytes 12 and 13 if CHEN is clear.

2.4.16 ECC Pattern Word (IOPB Bytes 14 and 15)

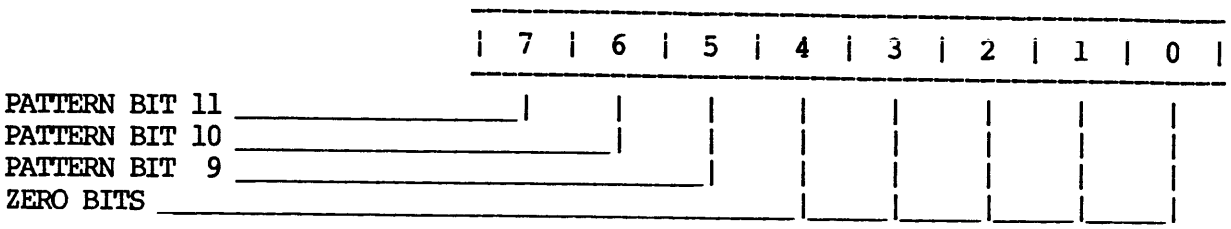
The ECC Pattern or Mask word is an 11-bit word used in the soft ECC correction procedure. The 450 stores the ECC Pattern word in IOPB Bytes 14 and 15. A soft ECC error is any single error of 11-bits or less. The 450 also considers

2.4.16 ECC Pattern Word (continued)

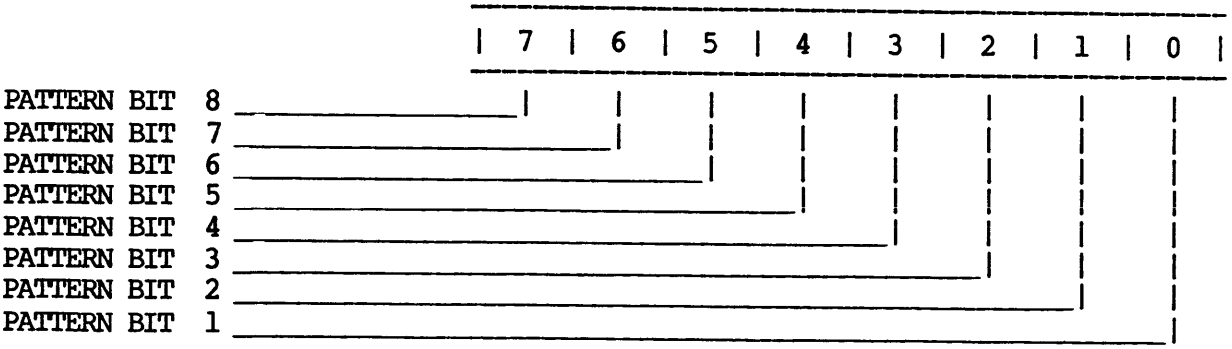
an error soft if the bits at each end of an 11-bit word are wrong, but the bits in the center are correct. The ECC Pattern word provides a pattern for correcting data in memory.

The 450 calculates the ECC Pattern word in reverse order, in IOPB Bytes 14 and 15 (See figures below). Execute a bit-reversal process to correct the direction of this mask before using the ECC Pattern word (it is reversed, in relation to the data stream it corrects). After the reversal process, the equivalent word has Pattern bit 0 in bit 16, Pattern bit 1 in bit 15, etc. The five least significant bits are zero (See Section 2.6.3.7).

ECC Pattern Word — (IOPB Byte 14)



ECC Pattern Word — (IOPB Byte 15)



2.4.17 ECC Address Word (IOPB Bytes 16 and 17)

When a soft ECC error occurs, the 450 calculates an ECC Address word. Two bytes comprise the ECC Address word: IOPB Byte 17 is the most significant byte; IOPB Byte 16 is the least significant byte. The ECC Address word points to the bit within a sector where the data in error starts. System software may correct this error by exclusive-ORing the ECC mask with this bit string.

2.5 COMMANDS

An IOPB diagram follows each command description. The diagrams are highlighted to indicate which bytes the 450 requires for command execution, and which bytes return after execution.

The four least significant bits of the Command byte are the IOPB Command bits. These four bits enable up to sixteen possible commands. Each 450 command is 24-bytes long. Generally, all commands use Bytes 0 through 0FH (certain commands use Bytes 10H through 17H). Only the Read command uses ECC Bytes 14H through 17H. Reserve all 24 bytes to maintain IOPB integrity.

2.5.1 NOP Command (Command Code 0)

2.5.1.1 General

On a No Operation (NOP) command, the controller selects a disk drive, saves DRDY (bit 0 in the CSR) and releases the drive.

2.5.1.2 IOPB

NOP

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	AUD	RELO	CHEN	IEN	Command Code			
1 - IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
2 - STAT1	ERRS	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	B/W	Interleave Factor				Throttle		
5 - DRIVE	Drive Type		AFE	0			Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0					Cyl. Addr. High		
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	ESD	EHDT	Head Offset					
11 - SUBFUN	Subfunction Code							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High				0			
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

Required For Execution Returned Value

2.5.2 Write Command (Command Code 1)

2.5.2.1 General

The Write command transfers data to the disk. It starts at the disk and memory addresses specified in the IOPB, and transfers as many sectors as requested. The 450 crosses cylinder, head and sector boundaries as required.

2.5.2.2 IOPB

WRITE

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	AUD	RELO	CHEN	IEN	Command Code			
1 - IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
2 - STAT1	ERRS	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	B/W	Interleave Factor				Throttle		
5 - DRIVE	Drive Type		AFE	0			Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0						Cyl. Addr. High	
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	ESD	EHDT	Head Offset					
11 - SUBFUN	Subfunction Code							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High				0			
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

Required For Execution Returned Value

2.5.2.3 Detailed Description

2.5.2.3.1 Implied Seeks

The 450 issues an implied seek on a Write command. The seek is issued as the first operation after reading the IOPB from system memory. If CHEN and EEF are set, the 450 scans the remainder of the chain for the possibility of initiating overlap seeks.

2.5.2.3.2 Filling The Buffer

When the drive completes its seek, the 450 accesses the IOPB to determine the command parameters, and begins to fill the FIFO buffer. The 450 looks for sector coincidence after it transfers at least one sector of data to the buffer. This ensures enough data is available in the buffer when the Write operation begins.

2.5.2.3.3 Sector Coincidence

The 450 selects the proper head and tests the write-protect status of the drive. The 450 then reads each sector header and compares it to the requested disk address. The data transfer begins when it finds a match. The 450 reports an error (5 or 12) if it does not find a match within one revolution plus five sectors.

2.5.2.3.4 Write Data

After the 450 finds a valid header, the disk sequencer counts the appropriate number of bytes, and writes the Sync bits. It then takes words out of the FIFO, serializes them, generates a new ECC value, and writes them to the disk. As the 450 removes data from the FIFO, it replaces it with appropriate DMAs from system memory.

2.5.2.3.5 Throttle

The throttle is the maximum number of transfers allowed each time the 450 becomes bus master. On a Write operation, the first DMA bursts are at the programmed throttle value until the buffer fills. After the 450 starts moving data to the disk, the typical burst is less than the throttle value. The 450 continues to transfer words into the FIFO until the buffer holds enough data to complete the operation.

2.5.2.3.6 ECC

After the 450 writes the data field of a sector, it writes the ECC value generated from the data field.

2.5.2.3.7 Incrementing Disk Address

The 450 increments the sector address by one as it writes each sector. If the sector address is greater than max sector, the 450 resets it to zero and increments the head address. If the resulting head address is greater than max head, the 450 resets it to zero, and increments the cylinder address. The 450 reports an error if the cylinder address is greater than max cylinder when it issues a seek.

2.5.2.3.8 Completing a Transfer

The 450 decrements the sector count by one as it transfers each sector. The 450 tests the sector count at the end of each transfer to determine if it is complete. If the transfer is not complete, it transfers the next sector. The controller issues a seek each time it increments the cylinder address.

When it completes the transfer, the 450 updates the two Status bytes of the IOPB, and generates an interrupt, if enabled. The 450 updates the IOPB if the Auto-update (AUD) bit of the IOPB Command byte is set.

The 450 stops a transfer that ends in a hard error, updates the two Status bytes of the IOPB, and generates an interrupt, if enabled. Any chained operations halt. The IOPB Address and Relocation Registers point to the IOPB which caused the error. The 450 updates the IOPB if AUD is set.

If the transfer ends with a soft error, the 450 updates the two Status bytes of the IOPB, and generates an interrupt, if enabled. Any chained operations continue. The 450 updates the IOPB if AUD is set. The 450 does not set the ERR bit in the CSR on a soft error.

2.5.3 Read Command (Command Code 2)

2.5.3.1 General

The Read command transfers data from the disk to memory. The transfer starts at the disk and memory addresses specified in the IOPB, and crosses sector, head, and cylinder boundaries as required.

2.5.3.2 IOPB

READ

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	AUD	RELO	CHEN	IEN	Command Code			
1 - IMODE	0	IEI	IERR	HDP	ASR	ECCF	ECC Mode	
2 - STAT1	ERRS	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	B/W	Interleave Factor					Throttle	
5 - DRIVE	Drive Type	AFE	0				Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0						Cyl. Addr. High	
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	ESD	EHDT	Head Offset					
11 - SUBFUN	Subfunction Code							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High	0						
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

Required For Execution Returned Value

2.5.3.3 Detailed Read Description

2.5.3.3.1 Implied Seeks

The 450 issues an implied seek on a Read command. The 450 issues the seek as the first operation after reading the IOPB from system memory. If CHEN and EEF are set, the 450 scans the remainder of the chain for the possibility of initiating overlap seeks.

2.5.3.3.2 Seek End

The 450 scans the drives, and determines when each drive completes its seek.

2.5.3.3.3 Sector Coincidence

The 450 reads each sector header and compares it to the requested disk address. The data transfer begins when it finds a match. The 450 reports an error if it cannot find a match within one revolution plus five sectors.

2.5.3.3.4 Read Data

After it finds a valid header, the disk sequencer waits for the Sync bits of the data field. After the 450 synchronizes to the data, it deserializes the data and places it into the FIFO buffer. When data is available at the other end of the FIFO, the 450 requests the bus, and DMAs the data to memory. The 450 also uses the serial data stream to generate an ECC.

2.5.3.3.5 Throttle

The throttle is the maximum number of transfers allowed each time the 450 becomes bus master. The first DMA bursts on a Read operation are at minimum value since the limiting factor of the DMA burst length is the number of words available from the FIFO. After the initial few DMA bursts, the typical burst length increases, possibly approaching the throttle limit. The controller continues to transfer words until the sector count goes to zero and the buffer is empty.

2.5.3.3.6 ECC

After the 450 reads the data field of a sector, it compares the read-generated ECC value to the write-generated ECC value on the disk.

2.5.3.3.7 Incrementing Disk Address

The 450 increments the sector address by one as it reads each sector. If the sector address is greater than max sector, the 450 resets it to zero, and increments the head address. If the resulting head address is greater than max head, the 450 resets it to zero, and increments the cylinder address by one. The 450 reports an error if the cylinder address is greater than max cylinder when it issues a seek.

2.5.3.3.8 Completing a Transfer

The 450 tests the sector count after it transfers each sector. If the transfer is not complete, it transfers the next sector. The 450 issues a seek each time it increments the cylinder address.

When the 450 completes the transfer, it updates the two Status bytes of the IOPB, and generates an interrupt, if enabled. The 450 updates the IOPB if AUD in the IOPB Command byte is set.

The 450 stops a transfer that ends in a hard error, updates the two Status bytes of the IOPB, and generates an interrupt, if enabled. Any chained operations halt. The IOPB Address and Relocation Registers point to the IOPB which caused the error. The 450 updates the IOPB if AUD is set.

If the transfer ends with a soft error, the 450 updates the two Status bytes of the IOPB, and generates an interrupt, if enabled. Any chained operations continue. The 450 updates the IOPB if AUD is set. The 450 does not set ERR in the CSR, or STAT1, on a soft error.

2.5.3.3.9 Read Command Encounters an ECC Error in ECC Mode 0 (440-Compatible)

The 450 stops reading if it calculates an ECC value on a Read operation which does not match the ECC value written on the disk. It writes all the data for that sector to memory, and begins a shifting and counting process which determines the offset and pattern of the error.

If the 450 encounters an error larger than 11 bits (hard error), it writes the Completion Code 06 into the Completion Code byte.

If the 450 encounters an error of 11-bits or less (soft error), it writes the ECC Pattern and Address words to their IOPB bytes and returns the Completion Code 1E.

When the 450 encounters an ECC error: the disk address points to the sector containing the error, the data and relocation addresses point to the first byte of data from the sector following the sector in error, and the sector count equals the number of sectors remaining plus one. To retrieve this information, either set AUD and retry the transfer, or write the IOPB Reset/Update Register.

To continue the transfer after a soft error, update the sector count (subtract one), increment the disk address, and restart the IOPB.

2.5.3.3.10 Read Command Encounters an ECC Error in Mode 1

The 450 does not detect ECC errors in Mode 1. The data transfer continues since no error can occur.

2.5.3.3.11 Read Command Encounters an ECC Error in Mode 2

If the 450 encounters an ECC correctable error in Mode 2, it stops the transfer, corrects the data in memory (if possible) and resumes the data transfer on the next revolution of the disk. The 450 posts a Soft ECC Recovered error status in the IOPB and, if CHEN is set, continues the chain. The controller posts a Completion Code of 06H if the error cannot be recovered. The 450 performs corrections in byte-wide DMA transfers.

2.5.3.3.12 Read Command Encounters an ECC Error in Mode 3

If the 450 detects an ECC error in Mode 3, it continues the data transfer as if there is no error. When it completes the transfer, the 450 posts the Completion Code 06H (hard ECC error) in the IOPB, indicating it encountered one or more uncorrected ECC errors. The 450 reports this error as "soft", as it does not stop a chain. The 450 does not set ERR or ERRS on this error in Mode 3.

2.5.4 Write Track Headers (Command Code 3)

2.5.4.1 General

Write Track Headers and Read Track Headers enable the controller to avoid media defects by slipping sectors. The Write Track Headers command formats an entire track with header data obtained from system memory. The Read Track Headers command transfers header data into system memory. This data is the actual header for each sector on the track, starting at physical index (including bad and spare sectors). Since this is a Format command, it overwrites all data on the track. Setting the EEF bit enables this command (See Section 2.6.4).

NOTE

System software must specify a non-zero sector count when using this command.

2.5.4.2 IOPB

WRITE TRACK HEADERS

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	AUD	RELO	CHEN	IEN	Command Code			
1 - IMODE	0	IBI	IERR	HDP	ASR	EEF	ECC Mode	
2 - STAT1	ERRB	0			Controller Type		0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	R/W	Interleave Factor					Throttle	
5 - DRIVE	Drive Type	AFE	0				Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0						Cyl. Addr. High	
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	ESD	EHDT	Head Offset					
11 - SUBFUN	Subfunction Code							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High	0						
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

Required For Execution Returned Value

2.5.4.3 Detailed Description

2.5.4.3.1 Data Buffer

Software must construct a data buffer in system memory before issuing a Write Track Headers command. The Read Track Headers command constructs a proper buffer in host memory. This buffer consists of four bytes of data for each sector; the total buffer length is four bytes times the total number of sectors on the track, including spare and bad sectors. The 450 counts the actual number of sectors on the disk and uses this value for the Write Track Headers command. The first four bytes comprise the header data for the first sector after the index pulse. The next four bytes comprise header data for the next sector, etc.

2.5.4.3.2 Implied Seeks

The 450 issues an implied seek on a Write Track Headers command. The 450 issues the seek as the first operation after reading the IOPB from system memory. If CHEN and EEF are set, the 450 scans the remainder of the chain for the possibility of initiating overlap seeks.

2.5.4.3.3 Seek End

The 450 scans the drives, and determines when each drive completes its seek. When the requested drive completes its seek, the 450 accesses the IOPB to determine the command parameters, then begins to fill its buffer. When the buffer has enough data, the 450 searches for the index pulse.

2.5.4.3.4 Throttle

The throttle is the maximum number of DMA transfers allowed each time the 450 becomes bus master. The DMA bursts on a Write Track Headers operation are at the specified throttle. The 450 continues the DMA transfer until enough data is available to format an entire track.

2.5.4.3.5 Pseudo Index

The 450 has two different format schemes: 440-compatible and 450-standard. Pseudo index and physical index are the same in the 440-compatible format. Pseudo index is delayed from physical index by one sector per track in the 450-standard format. When physical index arrives under the head, the 450 uses the first four bytes of data to format that sector. The 450 automatically calculates and appends the ECC to the header.

2.5.4.3.6 Format the Track

The 450 takes four bytes from the buffer and uses them as the header for each successive sector that arrives under the head. The Write Track Headers command does not write the data field portion of the sector; the data is invalid after this operation. The 450 formats every sector on the requested track.

2.5.4.3.7 Incrementing Disk Address

The 450 increments the head address by one after it successfully completes a command. If the resulting head address is greater than max head, the 450 resets it to zero, and increments the cylinder address.

2.5.4.3.8 Completing a Transfer

The 450 formats an entire track (if no errors occur), and updates the two Status bytes. The 450 updates the IOPB, if AUD is set, and generates an interrupt, if enabled.

The 450 stops a transfer that ends in a hard error, terminates any chained operations, updates the two Status bytes, and generates an interrupt, if enabled. The 450 updates the IOPB if AUD is set.

The 450 completes a transfer that ends in a soft error, continues any chained operations, updates the two Status bytes, and generates an interrupt, if enabled. The 450 updates the IOPB if AUD is set.

2.5.5 Read Track Headers (Command Code 4)

2.5.5.1 General

Read Track Headers and Write Track Headers enable the 450 to avoid media defects by slipping sectors. The Read Track Headers command reads the header from each physical sector, starting at physical index, and transfers the header data (in order) to system memory. The headers may not be in sequential order due to interleaving and sector slip. The 450 can write the headers back to the track with a Write Track Headers command. The buffer contains the actual header data from each sector on the track, starting at physical index (including bad and spare sectors). Setting the EEF bit enables the Read Track Headers command.

NOTE

System software must specify a non-zero sector count when using this command.

2.5.5.2 IOPB

READ TRACK HEADERS

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	AUD	RELO	CHEN	IEN	Command Code			
1 - IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
2 - STAT1	ERRS	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	B/W	Interleave Factor					Throttle	
5 - DRIVE	Drive Type	AFE	0				Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0						Cyl. Addr. High	
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	ESD	EHDT	Head Offset					
11 - SUBFUN	Subfunction Code							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High	0						
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

Required For Execution Returned Value

2.5.5.3 Detailed Description

2.5.5.3.1 Data Buffer

Software must allocate a data buffer in system memory before issuing a Read Track Headers command. The total buffer length is four bytes times the total number of sectors on the track, including spare and bad sectors. The 450 counts the actual number of sectors on the drive and uses this value as the number of sectors for the Read Track Headers command.

2.5.5.3.2 Implied Seeks

The 450 issues an implied seek on a Read Track Headers command. It issues the seek as the first operation after reading the IOPB from system memory. If CHEN and EEF are set, the 450 scans the remainder of the chain for the possibility of initiating overlap seeks.

2.5.5.3.3 Seek End

The 450 scans the drives, and determines when each drive completes its seek. When the requested drive completes its seek, the 450 accesses the IOPB to determine the command parameters and initiates a search for index.

2.5.5.3.4 Pseudo Index vs. Physical Index

The 450 has two different format schemes: 440-compatible and 450-standard. Pseudo index and physical index are the same in the 440-compatible format. Pseudo index is delayed from physical index by one sector per track in the 450-standard format. When index arrives under the head, the 450 reads the header from that sector, and transfers the data to the buffer.

2.5.5.3.5 Read the Track

As each sector arrives under the head, the 450 reads four bytes from the header and transfers them to the buffer. The controller repeats this operation for each sector on the requested track.

2.5.5.3.6 Empty the Buffer

After it reads a complete track, the 450 DMAs the header data to system memory.

2.5.5.3.7 Throttle

The throttle is the maximum number of DMA transfers allowed each time the 450 becomes bus master. On a Read Track Headers operation the DMA bursts are at the specified throttle value. The 450 continues the DMA transfer until system memory has all the data.

2.5.5.3.8 Incrementing Disk Address

The 450 increments the head address by one after it successfully completes a command. If the resulting head address is greater than max head, the 450 resets it and increments the cylinder address.

2.5.5.3.9 Completing a Transfer

The 450 reads the headers of an entire track (if no errors occur). When it completes the transfer, the 450 updates the two Status bytes, and generates an interrupt, if enabled. The 450 updates the IOPB if AUD is set.

The 450 stops a transfer that ends in a hard error, terminates any chained operations, updates the two Status bytes, and generates an interrupt, if enabled. The 450 updates the IOPB if AUD is set.

The 450 completes a transfer that ends in a soft error, continues any chained operations, updates the two Status bytes, and generates an interrupt, if enabled. The 450 updates the IOPB if AUD is set.

2.5.6 Seek Command (Command Code 5)

2.5.6.1 General

The Seek command moves the heads of the selected disk drive to the address specified in the IOPB cylinder address. Software uses a Seek command for diagnostic purposes only, since an implied seek is inherent in data transfer commands. The 450 may initiate overlap seeking when software chains IOPBs for different drives.

2.5.6.2 IOPB

SEEK

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	AUD	RELO	CHEN	IEN	Command Code			
1 - IMODE	0	IE1	IERR	HDP	ASR	EEF	ECC Mode	
2 - STAT1	ERRS	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	B/W	Interleave Factor					Throttle	
5 - DRIVE	Drive Type	AFE	0				Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0						Cyl. Addr. High	
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	ESD	EHDT	Head Offset					
11 - SUBFUN	Subfunction Code							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High	0						
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

Required For Execution Returned Value

2.5.6.3 Detailed Description

A Seek command sends the cylinder address to the disk drive. The 450 scans the drives, and determines when each drive completes its seek. After the drive completes its seek, the 450 marks the associated IOPB complete. The 450 overlaps Explicit Seek commands if the EEF bit is set (like implied seeks).

2.5.7 Drive Reset (Command Code 6)

2.5.7.1 General

A Drive Reset command clears a drive fault and returns the drive to Cylinder 0 (return to zero or recalibrate).

2.5.7.2 IOPB

DRIVE RESET

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	AUX	RELO	CHEN	IEN	Command Code			
1 - IMODE	0	IEI	IERR	HDE	ASR	EEF	ECC Mode	
2 - STAT1	ERRS	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	B/W	Interleave Factor					Throttle	
5 - DRIVE	Drive Type		AFE	0			Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0						Cyl. Addr. High	
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	ESD	EHDT	Head Offset					
11 - SUBFUN	Subfunction Code							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High				0			
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

Required For Execution Returned Value

2.5.7.3 Detailed Description

The Drive Reset command issues a Fault Clear command to the disk drive and then issues a Recalibrate command. Since Recalibrate is a form of the Seek command, the 450 completes the IOPB when the disk drive completes its seek.

2.5.8 Write Format (Command Code 7)

2.5.8.1 General

The Write Format command formats a disk with header information. The 450 writes header information on the disk, crossing sector, head, and cylinder boundaries, as required. The IOPB is complete when the sector count is zero.

To use the Sector Slip function, the drive must be configured properly and software must issue a Set Drive Size command to the 450 (See Section 2.5.8.3.1).

2.5.8.2 IOPB

FORMAT

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	AUD	RELO	CHEN	IEN	Command Code			
1 - IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
2 - STAT1	ERRS	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	R/W	Interleave Factor				Throttle		
5 - DRIVE	Drive Type	AFE	0				Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0						Cyl. Addr. High	
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	ESD	EHDT	Head Offset					
11 - SUBFUN	Subfunction Code							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High	0						
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

Required For Execution Returned Value

2.5.8.3 Detailed Description

2.5.8.3.1 Allocating Spare Sectors

Determine both the maximum number of sectors per track available on the drive and the number of sectors per track you wish to allocate as spares. Set the drive sector switches to the maximum number of sectors per track. The maximum sector number set by the Set Drive Size command equals the total number of sectors per track minus the number of sectors you allocate as spares.

For example, if the disk drive supports 34-sectors per track, set the drive sector switches to 34. If you are allocating 2-sectors per track as spares, set the drive size to 32-sectors per track. This automatically allocates two sectors as spares (See Section 3.4.2).

2.5.8.3.2 Implied Seeks

The 450 issues an implied seek on a Format command. It issues the seek as the first operation after reading the IOPB from system memory. If CHEN and EEF are set, the 450 scans the remainder of the chain for the possibility of initiating overlap seeks.

2.5.8.3.3 Test Track Size

When the drive completes the seek, the 450 accesses the IOPB and determines the command parameters. The 450 determines if the sector size and max sector are within limits by timing a track, counting sector pulses and checking the size of the sectors. The 450 performs this once per drive, per Unit Select, as part of the Format function. The 450 determines if there are spare or runt sectors on each track, and formats them accordingly.

2.5.8.3.4 Sector Coincidence

The 450 waits for index and then counts the appropriate number of sector pulses until the sector to be formatted arrives under the heads.

NOTE

> If you are interleaving the disk, software must specify the interleave factor at format time so the 450 formats the sectors in the proper sequence. Format full multiples of tracks, starting with Sector 0, to ensure format integrity while interleaving.

2.5.8.3.5 Write Header and ECC

After the 450 senses the sector pulse for the requested sector, the disk sequencer counts the appropriate number of bytes and writes the Sync bits. It then takes the Header words out of the FIFO, serializes them, generates a new ECC value, and writes the header to the disk. The ECC value generated for the Header words becomes part of the header on the disk.

2.5.8.3.6 Sector Data

The 450 writes the data field portion of the sector with all zeros.

2.5.8.3.7 Incrementing Disk Address

The 450 increments the sector address by one. If the resulting sector address is greater than max sector, the 450 resets it to zero and increments the head address. If the resulting head address is greater than max head, the 450 resets the head address to zero and increments the cylinder address by one. An error occurs if the cylinder address is greater than max cylinder when the 450 issues a seek.

2.5.8.3.8 Completing a Transfer

The 450 decrements the sector count by one each time the disk passes over a sector boundary during formatting. The 450 formats each sector, and then tests the sector count, until all the sectors are formatted. The controller issues a seek each time it increments the cylinder address.

When the 450 completes the transfer, it updates the two Status bytes of the IOPB, and generates an interrupt, if enabled. The 450 updates the IOPB if AUD is set.

The 450 stops a transfer that ends in a hard error and marks it as complete with error. Any chained operations terminate. The IOPB Address and Relocation Registers point to the IOPB which caused the error.

If the transfer ends with a soft error, the 450 continues any chained operations.

2.5.9 Read Header, Data, and ECC (Command Code 8)

2.5.9.1 General

The Read Header, Data, and ECC command reads sectors from the disk to the memory locations specified by the data address. The 450 reads an additional eight bytes for each sector (See Table 2-7). Software must specify the interleave factor for the 450 to read the sectors in the correct sequence from the drive.

NOTE

The sector address specified in the IOPB is an absolute value and does not take into consideration any slipped sectors.

2.5.9.2 IOPB

READ HDE

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	AUD	RELO	CHEN	IEN	Command Code			
1 - IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
2 - STAT1	ERRS	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	R/W	Interleave Factor				Throttle		
5 - DRIVE	Drive Type	AFE	0				Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0						Cyl. Addr. High	
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	ESD	EHDT	Head Offset					
11 - SUBFUN	Subfunction Code							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High	0						
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

Required For Execution Returned Value

2.5.9.3 Detailed Description

2.5.9.3.1 Implied Seeks

The 450 issues an implied seek on a Read Header, Data, and ECC command. It issues the seek as the first operation after reading the IOPB from system memory. If CHEN and EEF are set, the 450 scans the remainder of the chain for the possibility of initiating overlap seeks.

2.5.9.3.2 Seek End

The 450 scans the drives to determine when each drive completes its seek.

2.5.9.3.3 Sector Coincidence

The 450 waits for index from the drive, counts the appropriate number of sector pulses (to locate the specified sector), and reads the sector. System software must specify the interleave factor in the IOPB.

2.5.9.3.4 Read Data

The disk sequencer waits for the Sync bits of the header field. As the 450 reads the header from the disk, it deserializes it and places it into the FIFO buffer. After the 450 reads two Header words into the FIFO, the sequencer waits for the Sync bits of the data field. After synchronizing with the data field, the 450 reads the data in, deserializes it, and puts it into the FIFO buffer. The ECC words at the end of the data field are the last two words it reads. When data is available at the other end of the FIFO, the 450 requests the bus and transfers the data to memory. The 450 transfers an additional eight bytes per sector, which are the header and ECC fields.

2.5.9.3.5 Throttle

The throttle is the maximum number of transfers allowed each time the 450 becomes bus master. On a Read Header, Data, and ECC operation, the first DMA requests are at minimum value since the limiting factor of the burst length is the number of words available from the FIFO. After the initial few DMA bursts, the typical burst length increases, possibly approaching the throttle limit. The 450 continues to transfer words until the sector count overflows and the buffer is empty.

2.5.9.3.6 ECC

This command does not support ECC. The 450 reads the two ECC words written on the sector and places them into memory as data.

2.5.9.3.7 Incrementing the Disk and Cylinder Addresses

The 450 increments the sector address after it reads a sector. It does not increment the head address on this command.

2.5.9.3.8 Completing a Transfer

At the end of each sector, the 450 decrements the sector count and tests it to determine if the transfer is complete. If the transfer is not complete, it transfers the next sector. A Disk Sequencer error occurs if the sector address is greater than the physical number of sectors on the disk. When the 450 completes the transfer, it updates the Status bytes of the IOPB, and generates an interrupt, if enabled. The 450 updates the IOPB if AUD is set.

The 450 stops a transfer that ends with a hard error, updates the two Status bytes of the IOPB, and generates an interrupt, if enabled. Any chained operations halt. The IOPB Address and Relocation Registers point to the IOPB which caused the error. The 450 updates the IOPB if AUD is set.

If the transfer ends with a soft error, the 450 updates the two Status bytes of the IOPB, and generates an interrupt, if enabled. Any chained operations continue. The 450 updates the IOPB if AUD is set. The 450 does not set ERR in the CSR on a soft error.

DESCRIPTION	SECTOR SIZE AND BYTE NUMBER WITHIN SECTOR		
Sector Size	256-Byte	512-Byte	N-Byte
Cylinder Address Low	1	1	1
Cylinder Address High and Sector Address 64/128	2	2	2
Head Number	3	3	3
Sector and Drive Type	4	4	4
Sector Data	5-260	5-517	5-N+4
Data ECC	261-264	517-520	(N+5)-(N+8)

TABLE 2-7. HEADER, DATA, AND ECC BYTES

2.5.10 Read Drive Status (Command Code 9)

2.5.10.1 General

On a Read Drive Status command, the 450 posts configuration information, and specific Drive Type and status information, for the selected drive.

2.5.10.2 IOPB

READ DRIVE STATUS

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	AUD	RELO	CHEN	IEN	Command Code			
1 - IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
2 - STAT1	ERRS	0		Controller Type			0	DONE
3 - STAT2	Error on Completion Code							
4 - THROT	B/W	Interleave Factor					Throttle	
5 - DRIVE	Drive Type		RFF				Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0						Cyl. Addr. High	
A - SCNTL	ONCL	DRDY	WRPT	DPB	SKER	DFLT	0	
B - SCNTH	Firmware Revision Level							
C - DATAL	Bytes Per Sector Low							
D - DATAH	Bytes Per Sector High							
E - DATARL	Actual Sectors Per Track							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	HSD	HHDT	Head Offset					
11 - RES	0							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High				0			
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

Required For Execution Returned Value

2.5.10.3 Detailed Description

Read Drive Status has two purposes: it indicates the current size of the Drive Type specified, and the status of the drive unit specified. The IOPB must contain the Drive Type and Unit Number in the Drive Type/Unit Select byte. The 450 returns these values in Bytes 6 through E, and 10, of the resulting IOPB. This command does not require the Drive Type to match the Unit Number of a disk drive.

2.5.10.3.1 Returned Values

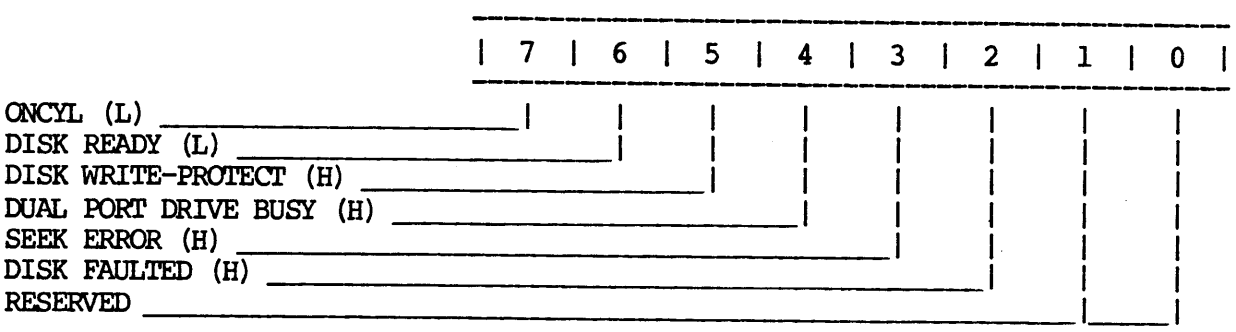
On a Read Drive Status command, the 450 returns the following information:

Drive Type Specified	450	Selected Drive
Maximum Sector	Code Revision	Drive Status
Maximum Head	Sector Size	Number of Sectors/Track
Maximum Cylinder	Adaptive Format Flag	
Head Offset		
Embedded Servo Drive		

2.5.10.3.2 Drive Status

The 450 selects the drive, latches the following information, and releases the drive. Byte A contains the latched drive information.

Drive Status -- (IOPB Byte A)



BIT	MNEMONIC	MEANING
7	ONCL	ON-CYLINDER (L) - Represents the On-cylinder status of the drive whose drive number is in the Drive byte of this IOPB. If the drive is ready and ONCL is clear, the drive is not seeking. If ONCL is set, the heads of the selected drive are not positioned over a cylinder.
6	DRDY	DISK READY (L) - When clear, the selected drive is ready.
5	WRPT	DISK WRITE-PROTECT (H) - When set, the selected disk is write-protected.
4	DPB	DUAL PORT BUSY (H) - Sets when the 450 attempts to select a dual port drive which is connected to another controller. Clear indicates the selected drive is not busy or not ready.
3	SKER	HARD SEEK ERROR (H) - Sets if the selected drive reports a seek error in its logic.
2	DFLT	DISK FAULT (H) - Sets if the selected drive reports any type of fault in its logic.
0,1		RESERVED.

2.5.10.3.3 Drive Type Parameters

- o Maximum Sector
- o Maximum Head
- o Maximum Cylinder
- o Head Offset
- o Embedded Servo Drive

The 450 loads the drive size parameters into Bytes 6 through 9, and 10H. It loads the maximum sector value into Byte 7; the maximum head value into Byte 6; and the maximum cylinder value into Bytes 8 and 9. The 450 returns the head offset value and the status of the embedded servo flag (typically zero for a drive that does not have fixed and removable media) in Byte 10H. The Embedded Servo Select bit is also located in Byte 10H (set it to zero for drives that do not have fixed and removable media).

2.5.10.3.4 450 Parameters

The Read Drive Status command provides the sector size in bytes per sector, the adaptive format flag, and firmware revision of the 450. Byte B contains a Revision Code where 1=A, 2=B, etc. Bytes C and D contain the number of bytes per sector.

The 450 defines the Drive Type/Unit Select byte (IOPB Byte 5), bit 4, as the Adaptive Format bit (AFE). This bit indicates the 450 format configuration: 440 or 450. When set, the controller accepts the 450-standard format (i.e., the sectors are skewed). Clear indicates the controller is 440-compatible. Revision C (and future revisions) of the 450 microcode include this bit.

2.5.10.3.5 Drive Parameters

The 450 counts the total number of sectors per track. This number includes all sectors, even if one of the sectors is too small (runt sector) to be a data sector. The 450 returns this count in Byte E.

2.5.11 Write Header, Data, and ECC (Command Code A)

2.5.11.1 General

This command writes the header, data, and ECC for one or more sectors. The 450 takes the header, data, and ECC from memory, as specified by the data transfer address. It then writes eight additional bytes per sector on the disk (Table 2-7 illustrates the order of the bytes). System software must specify the interleave factor for the 450 to write sectors in the correct order on the disk.

NOTE

The sector address specified in the IOPB is an absolute value and does not take into consideration any slipped sectors.

2.5.11.2 IOPB

WRITE HDE

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	AUD	RELO	CHEN	IEN	Command Code			
1 - IMODE	0	IEI	IERR	HDP	ASR	EEP	ECC Mode	
2 - STAT1	HRBS	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	B/W	Interleave Factor					Throttle	
5 - DRIVE	Drive Type	AFE	0				Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0						Cyl. Addr. High	
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	ESD	EHDT	Head Offset					
11 - SUBFUN	Subfunction Code							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High	0						
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

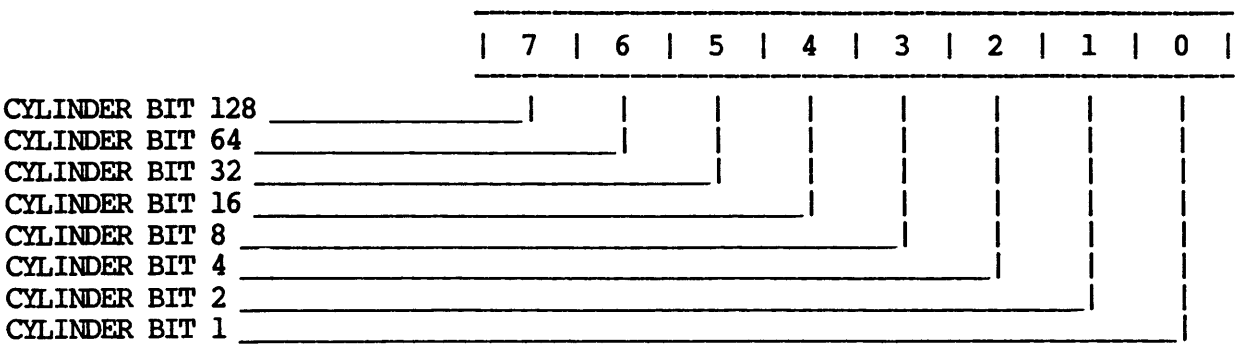
Required For Execution Returned Value

2.5.11.3 Detailed Description

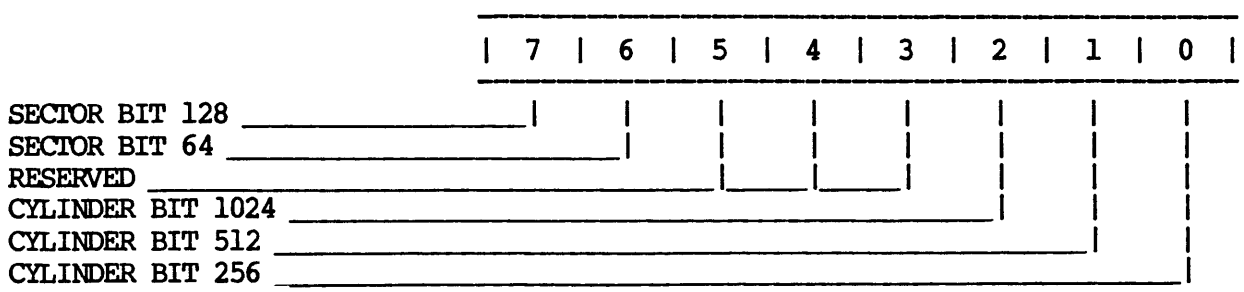
2.5.11.3.1 Data Buffer

System software must create a data buffer in system memory before issuing the IOPB for a Write Header, Data, and ECC command. The first four bytes in the buffer comprise the Header bytes. (The following diagrams illustrate the proper layout for these bytes.) The next 512 bytes (for 512-byte sectors) comprise the data to be written on the sector. The last four bytes comprise the ECC bytes to be written on the sector.

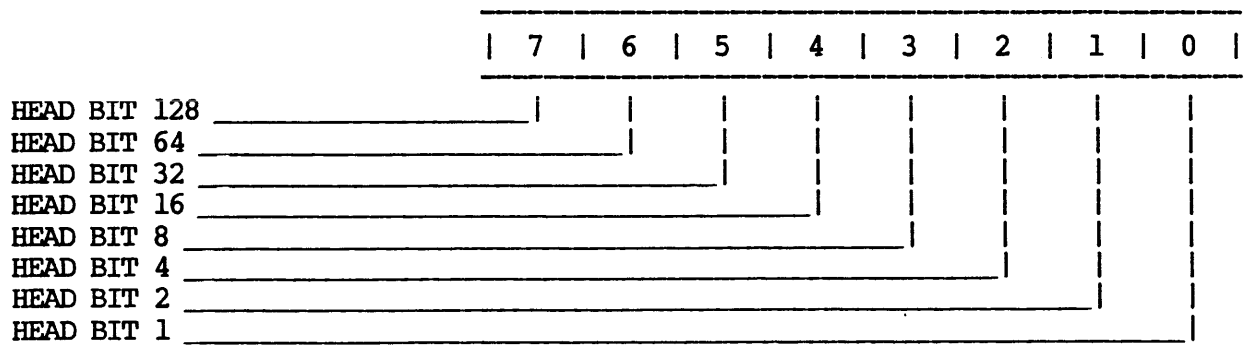
Buffer Byte 0



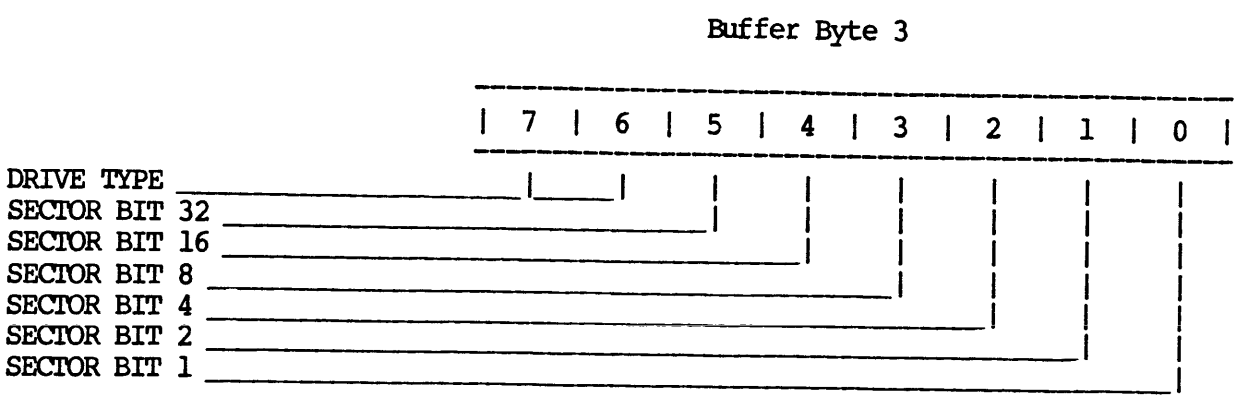
Buffer Byte 1



Buffer Byte 2



2.5.11.3.1 Data Buffer (continued)



2.5.11.3.2 Implied Seeks

The 450 issues an implied seek on a Write Header, Data, and ECC command. It issues the seek as the first operation after reading the IOPB from system memory. If CHEN and EEF are set, the 450 scans the remainder of the chain for the possibility of initiating overlap seeks.

2.5.11.3.3 Filling The Buffer

When the drive completes its seek, the 450 accesses the IOPB to determine the command parameters, and begins to fill the buffer. The 450 searches for a requested sector when the buffer contains one sector of data. This ensures enough data is available in the buffer at the start of the Write operation.

2.5.11.3.4 Sector Coincidence

The 450 waits for the index pulse from the drive, counts the appropriate number of sector pulses (to locate the specified sector), and writes that sector. System software must specify the interleave factor in the IOPB.

2.5.11.3.5 Write Data

The disk sequencer counts the appropriate number of bytes after sector coincidence, and then writes the Sync bits. It takes two words out of the FIFO, serializes them, generates a new ECC value, and writes them and the ECC to the disk as the new header. The sequencer counts an appropriate number of bytes and then writes the Data Sync bits. It takes the data from the FIFO, serializes it, and writes the data to the disk. As the sequencer removes data from the FIFO, system memory replaces it with the appropriate DMAs.

2.5.11.3.6 Throttle

The throttle is the maximum number of DMA transfers allowed each time the 450 becomes bus master. On a Write Header, Data, and ECC operation, the first DMA bursts are at maximum value until the buffer fills. After the 450 starts moving words to the disk, the typical burst is less than the throttle value. The 450 continues to transfer data until the buffer has enough data to complete the operation.

2.5.11.3.7 ECC

After the 450 writes the data field, it takes the ECC words from the buffer and writes them to the disk.

2.5.11.3.8 Incrementing Disk Address

The 450 increments the sector address by one. The 450 does not increment the head address on this command.

2.5.11.3.9 Completing a Transfer

The 450 decrements the sector count by one each time it increments the DMA address over a sector boundary. The 450 tests the sector count each time it transfers a sector. If the transfer is not complete, it transfers the next sector. A Disk Sequencer error occurs if the sector address increments beyond max sector.

When the 450 completes the transfer, it updates the two Status bytes of the IOPB, and generates an interrupt, if enabled. The 450 updates the IOPB if AUD is set.

The 450 stops a transfer that ends with a hard error, updates the two Status bytes of the IOPB, and generates an interrupt, if enabled. Any chained operations halt. The IOPB Address and Relocation Registers point to the IOPB which caused the error. The 450 updates the IOPB if AUD is set.

If the transfer ends with a soft error, the 450 updates the two Status bytes of the IOPB, and generates an interrupt, if enabled. Any chained operations continue. The 450 updates the IOPB if AUD is set.

2.5.12 Set Drive Size (Command Code B)

2.5.12.1 General

The Set Drive Size command allows system software to configure the drive size parameters. Software modifies the parameters for the Drive Type specified in Byte 5. Byte 7 specifies the new max sector value; Byte 6 specifies the new max head value; and Bytes 8 and 9 specify the new max cylinder value (Byte 9 is the most significant byte). Byte 10H specifies the head offset value; set bit 7 (ESD) if you are using an embedded servo drive.

Power-up, or a Multibus INIT/, resets any size parameters modified by a Set Drive Size command to the default values in EPROM.

2.5.12.2 IOPB

SET DRIVE SIZE

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	MOD	RELO	CHEN	IEN	Command Code			
1 - IMODE	0	IEI	IERR	HDE	ASR	REE	ECC Mode	
2 - STAT1	ERRS	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	B/W	Interleave Factor				Throttle		
5 - DRIVE	Drive Type		0				Unit Select	
6 - HEAD	Number of Heads							
7 - SECT	Number of Sectors Per Track							
8 - CYLL	Number of Cylinders Low							
9 - CYLH	0					No. Cyl. High		
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	ESD		Head Offset					
11 - RES	0							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High	0						
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

Required For Execution Returned Value

2.5.12.3 Detailed Description

The Set Drive Size command allows you to customize the 450 to operate with drives of any number of sectors, heads and cylinders.

2.5.12.3.1 Disk Sectors Per Track

The IOPB must contain the maximum value of sectors per track minus one. If the disk you are using has 32-sectors per track, the 450 refers to them as Sectors 0 through 31. Enter 1FH in Byte 7 (the hexadecimal equivalent of 31).

2.5.12.3.2 Disk Heads Per Cylinder

The IOPB must contain the maximum value of disk heads minus one. If the disk you are using has 19 heads, the 450 refers to them as Heads 0 through 18. Enter 12H in Byte 7.

If you are specifying a Drive Type for a fixed/removable disk, system software must set the maximum head value for the fixed or removable sections. For example, the Drive Type that specifies the removable portion of a CDC 96 MB CMD drive has a maximum head address of one, since it has two heads; the Drive Type that specifies the fixed portion of the disk has a maximum head address of four, and a head offset value of 10H.

2.5.12.3.3 Disk Cylinders

The IOPB must contain the maximum value of cylinders minus one. If the disk you are using has 823 cylinders, the 450 refers to them as Cylinders 0 through 822. Enter 36H in Byte 8 and 03 in Byte 9 (336H is the hex equivalent of 822).

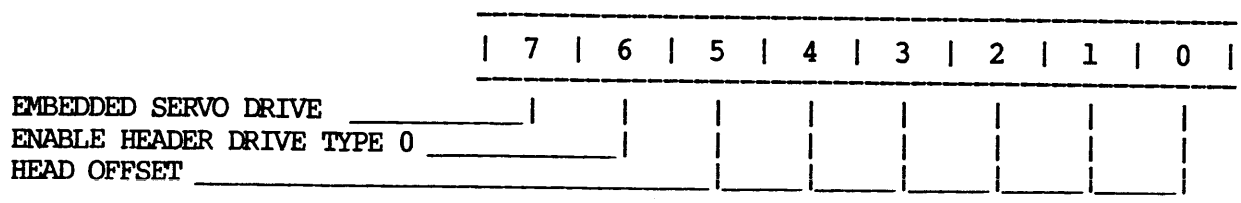
2.5.12.3.4 Head Offset / Embedded Servo Drive (IOPB Byte 10)

System software must specify a head offset value for fixed/removable drives such as the CMD and Lark. Software specifies two Drive Types: one Drive Type specifies the removable portion of the drive; the other specifies the fixed portion. The offset value is a hex number which the 450 adds to the head number in order to select either the fixed or removable portion of the disk. The head offset value for the removable portion of a CMD is zero; the head offset value for the fixed portion is 10H. Reference the appropriate vendor manual to determine the head offset values for the fixed and removable portions of the disk.

When bit 7 in IOPB Byte 10 is set, software selects a seek after every Head Change mode (required by embedded servo disk drives). Configure the embedded servo drive to the mode that requires the 450 to issue a seek on each head change. The drive requires this seek to lock onto the new track (See Sections 2.5.10 and 2.5.12).

2.5.12.3.4 Head Offset / Embedded Servo Drive (continued)

Head Offset / Embedded Servo Drive — (IOPB Byte 10)



2.5.12.3.5 Enabling Header Drive Type 0 (902-450-9xx Series Only)

Enable Header Drive Type 0 by setting bit 6 in the Head Offset byte, during a Set Drive Size command, for the drive you wish to reset. You can selectively enable this option on a per Drive Type basis.

When using a Drive Type that enables Drive Type 0, all operations that compare headers expect a zero in the Header Drive Type. The 450 puts a zero in the Header Drive Type during Format operations (See Section 2.6.6.5).

2.5.12.3.6 Default Parameters

Power-up, or a Multibus INIT/, resets the drive size parameters to the default parameters in EPROM. The following table describes the defaults:

Drive Type	MB	Heads	ESD	Cylinder	Sector	Drive
00	300	19	0	823	32	CDC 9766
01	80	5	0	823	32	CDC 9762
02	474	20	0	842	46	Fujitsu 2351
03	*	255	0	2047	128	(Maximum Config.)

TABLE 2-8. DEFAULT PARAMETERS

2.5.13 Self Test Command (Command Code C)

2.5.13.1 General

The Self Test command starts the same self test that runs automatically on power-up. The 450 reports a success status if it successfully completes the test. If an error occurs, the 450 reports the appropriate error status. Only use this command if CHEN is clear.

2.5.13.2 IOPB

SELF TEST

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	ATN	RELO	CHEN	IEN	Command Code			
1 - IMODE	0	IE1	IERR	HDP	ASR	EEF	ECC Mode	
2 - STAT1	ERRS	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	B/W	Interleave Factor				Throttle		
5 - DRIVE	Drive Type		AFE	0			Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0					Cyl. Addr. High		
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	ESD	EHDT	Head Offset					
11 - SUBFUN	Subfunction Code							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High			0				
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

Required For Execution Returned Value

2.5.14 DMA Test (Command Code D)

2.5.14.1 General

The DMA Test command is for diagnostic purposes only. It verifies whether the 450 can successfully DMA to and from system memory. The DMA Test command reads the first 16 bytes of the IOPB into the 450 FIFO, then DMAs them to the IOPB address plus 32. The 450 does not update Status Bytes 1 or 2 on this command, and it will not run the DMA test if EEF and DONE are set at the same time. Zero IMODE (Byte 1) and STAT1 (Byte 2) before issuing a DMA Test command. Bytes 3 through 0F can be any pattern desired. This command allows fast verification of 450 operation before system software is ready to test.

2.5.14.2 IOPB

DMA TEST

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	AUD	RELO	CHEN	IEN	Command Code			
1 - IMODE	0	IEL	IERR	HDP	ASR	EEF	ECC Mode	
2 - STAT1	ERRS	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	B/W	Interleave Factor				Throttle		
5 - DRIVE	Drive Type		AFE	0			Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0						Cyl. Addr. High	
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	ESD	EHDT	Head Offset					
11 - SUBFUN	Subfunction Code							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High				0			
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

Required For Execution Returned Value

2.5.15 Maintenance Buffer Load (Command Code E)

2.5.15.1 General

The Maintenance Buffer Load command is for diagnostic purposes only. It sets an address in the 450 which the Maintenance Buffer Dump command uses. Only chain a Maintenance Buffer Load command to a Maintenance Buffer Dump command. Write a pattern in memory, starting at the specified buffer address, to implement a Maintenance Buffer Load command (the buffer is 200H-bytes long).

2.5.15.2 IOPB

BUFFER LOAD

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	MOD	RELO	CHEN	IBR	Command Code			
1 - IMODE	0	IBI	IBRR	HDP	ASR	EEF	ECC Mode	
2 - STAT1	ERRS	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	B/W	Interleave Factor				Throttle		
5 - DRIVE	Drive Type		AFE	0			Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0					Cyl. Addr. High		
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	ESD	EHDT	Head Offset					
11 - SUBFUN	Subfunction Code							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High			0				
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

Required For Execution Returned Value

2.5.16 Maintenance Buffer Dump (Command Code F)

2.5.16.1 General

The Maintenance Buffer Dump command is for diagnostic purposes only. The 450 DMAs exactly 200H-bytes of data from the address specified in the Maintenance Buffer Load command into the FIFO buffer. After the 450 completes the DMA, it DMAs the data from the buffer back to the memory address specified in this command. Only chain a Maintenance Buffer Dump command to a Maintenance Buffer Load command (reset EFF before setting CHEN).

2.5.16.2 IOPB

BUFFER DUMP

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	AUD	RELO	CHEN	IEN	Command Code			
1 - IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
2 - STAT1	ERRS	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	B/W	Interleave Factor					Throttle	
5 - DRIVE	Drive Type		AFE	0			Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0						Cyl. Addr. High	
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	ESD	EHDT	Head Offset					
11 - SUBFUN	Subfunction Code							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High			0				
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

Required For Execution Returned Value

2.5.17 Read Defect Map (Command Code 8, Subfunction 1) (902-450-9xx Only)

2.5.17.1 General

The Read Defect Map command reads the external defect format or flaw information certain drive manufacturers write on the media. You lose this information when you format or write the disk. Your version of the 450 may not support this optional command (in which case, a Disk Sequencer error, or a normal Read Header, Data, and ECC function occurs). Only the 902-450-9xx series 450 supports this feature.

NOTE

This command is only valid if: a) the manufacturer writes the information onto the disk; and b) it is issued before the disk is formatted for the first time.

2.5.17.2 IOPB

READ DEFECT MAP

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	AUD	RELO	CHEN	IEN	Command Code			
1 - IMODE	0	IEI	IERR	DDP	ASR	EEF	ECC Mode	
2 - STAT1	ERRS	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	R/W	Interleave Factor				Throttle		
5 - DRIVE	Drive Type	ARB	0				Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0					Cyl. Addr. High		
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	ESD	EHDT	Head Offset					
11 - SUBFUN	Subfunction Code							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High	0						
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

Required For Execution Returned Value

2.5.17.3 Detailed Description

2.5.17.3.1 Data Buffer

System software must allocate a data buffer in memory to accept the 24-bytes of information the 450 transfers. Each track contains this 24-byte map.

2.5.17.3.2 Implied Seeks

The 450 issues an implied seek to the drive on a Read Defect Map command. The seek is issued as the first operation after reading the IOPB from system memory. If CHEN and EEF are set, the 450 scans the remainder of the chain for the possibilty of initiating overlap seeks.

2.5.17.3.3 Seek End

The 450 scans all currently active drives to determine when one completes its seek. When a seek complete status exists, the 450 may reread the IOPB to determine the transfer parameters. The 450 then initiates a search for index.

2.5.17.3.4 Index

When index arrives under the head, the 450 synchronizes to the first Sync byte. It takes the remaining Sync byte, four Header bytes, and the data, and places them into the buffer.

2.5.17.3.5 Empty the Buffer

DMA begins as soon as data is available on the bus side of the buffer. The DMA burst size is small since there is a limited amount of data to transfer.

2.5.17.3.6 Set Up the Command Parameters

Issue a Set Drive Size command before issuing a Read Defect Map commmand if you are using a non-default Drive Type parameter. Combine a command code of 8 with a Subfunction Code of 01 (IOPB Byte 11) to initiate the Read Defect Map command. It is important to set the Head and Cylinder bytes (they determine which track is read). Software must specify a valid sector address; zero is fine. The sector count can be any non-zero number. The Read Defect Map IOPB indicates the required command parameters.

2.5.17.3.7 Completing a Transfer

The 450 reads the defect map into memory for the requested head and cylinder. It then updates the two Status bytes, and generates an interrupt, if enabled. If the transfer ends with an error, the controller sets the appropriate bits and posts a Completion Code in STAT2. The Read Defect Map command only reads one track per IOPB.

2.5.17.3.8 Defect Map Data Format

The Read Defect Map command places each byte of data into memory with the bit order reversed. Reverse the bits in each byte to reflect the following data:

Byte #	SB	Description
Byte 0	19H	Sync Byte
Bytes 1-2	xx	Cylinder Address H & L
Byte 3	xx	Head Address
Byte 4	00	Zeros
Bytes 5-6	xx	Position of First Defect H & L
Bytes 7-8	xx	Length of First Defect H & L
Bytes 9-10	xx	Position of Second Defect H & L
Bytes 11-12	xx	Length of Second Defect
Bytes 13-14	xx	Position of Third Defect
Bytes 15-16	xx	Length of Third Defect
Bytes 17-18	xx	Position of Fourth Defect
Bytes 19-20	xx	Length of Fourth Defect
Bytes 21	F0	Last Byte
Bytes 22-23	00	Zeros

The defect position represents the byte count from index. The length of the defect is in bits per byte (See Section 2.6.4.5).

2.6 PROGRAMMING THE 450

This section suggests methods for programming the 450 disk controller. Assume that interrupts are enabled. Ignore the references to interrupting if they are not enabled in your situation.

2.6.1 IOPB Processing With No Command-Chaining

- o Set up the IOPB

  Allocate a 24-byte long segment of memory to build an IOPB. Set the various bytes in this IOPB as required to perform a function (See Section 2.4).

- o Point the 450 to the IOPB

  Write the IOPB address into the 450 IOPB Address Registers.

- o Set Go

  Write an 80H (GBSY) to the CSR. This starts the operation. The host processor either polls the CSR for DONE, or waits for the interrupt.

  NOTE

  We do not recommend waiting for DONE in STAT1 since it sets while the controller is still busy.

  The 450 starts processing the IOPB after it detects GBSY is set in the CSR. It uses the Address and Address Relocation Registers to address Multibus memory and read the IOPB. It executes the function and, when complete, updates the Status bytes of the IOPB, resets GBSY, and interrupts.

- o Check for Errors

  Read both the CSR and Status Byte 2 to determine if the 450 completed the command without error. Test the CSR to determine if DERR is set, since this may indicate that Status Byte 2 was not updated. If DERR is not set, check ERR and the value in Status Byte 2.

  The 450 posts a Completion Code for a command in Status Byte 2. A code of zero indicates successful completion; any other value indicates an error status. Section 2.4.4 details the Completion Codes. Section 2.6.3 explains the error recovery procedures.

2.6.2 IOPB Processing With Command-Chaining Enabled

The 450 supports IOPB chaining so that many IOPBs may be queued and executed as fast as possible. The chain starts with the IOPB pointed to by the IOPB Address Registers and follows the address pointers in each IOPB to the next IOPB. The 450 completes all IOPBs or stops the chain when a hard error occurs. If the EEF bit is set, the 450 scans the IOPB chain and issues seeks to units that are not busy; the 450 may not execute commands in sequential order.

2.6.2.1 The Chain

Each IOPB has a field which points to the next IOPB in the chain. The 450 does not look at the chain pointer unless CHEN in the Command byte is set. The 450 uses the IOPB Relocation Registers to relocate the Next IOPB Address bytes to point to the next IOPB. All IOPBs in a chain must be located within the 64K-byte memory block starting at the base address in the IOPB Relocation Registers.

2.6.2.2 Executing the Chain With Overlap Seeks

Each time the 450 starts, or after each Attention Request (if overlap seeks are enabled), the controller scans the IOPB chain. When it finds an unprocessed IOPB for a disk which is not busy, the 450 initiates a seek (which moves the drive heads to the correct cylinder). The controller continues this procedure until it completes the IOPB chain.

When a drive reaches the desired cylinder, the 450 initiates the requested data transfer for that drive. Seek commands are complete at this point. If the EEF bit is set, the 450 completes the IOPBs in the order in which the drives complete their seeks.

If you are chaining commands, and the EEF and DONE bits are set, software must clear STAT1 and STAT2 before reissuing the IOPB.

2.6.2.3 Completing IOPBs

The 450 updates the IOPB Status bytes as it completes each IOPB. If the Interrupt On Each IOPB (IEI) bit is set, the controller interrupts as it completes each IOPB. Software acknowledges an interrupt by writing a "1" to the Interrupt Pending (IPND) bit in the CSR. Do not reset the Interrupt Pending and/or Error bits with a Controller Reset command, as this may cause drive faults and misposition errors when the 450 continues the chain. The 450 remains busy until it completes the chain or a hard error occurs.

2.6.2.4 Modifying the Chain During Execution

The 450's Attention protocol uses two bits in the CSR: Attention Request (AREQ) and Attention Acknowledge (AACK). System software must set the Attention Request (AREQ) bit to notify the 450 it wishes to add or remove IOPBs from the chain. When the 450 recognizes this request, it sets the Attention Acknowledge (AACK) bit in the CSR. If IEI is set, the 450 interrupts after it sets AACK.

System software may now remove those IOPBs marked complete, and/or may add new IOPBs to the chain (you may modify CHEN and the Next IOPB Address, but do not touch previously chained IOPBs that are not marked complete).

2.6.2.5 Restarting a Modified Chain

When system software completes adding or removing IOPBs, it clears AREQ, and the 450 clears AACK. At this point, make sure GBSY is still set. Due to processing delays, GBSY may be set when software sets AREQ but may no longer be set when software clears AREQ (if the 450 determines the IOPB chain is complete while AACK is set, it may clear GBSY). If GBSY is set, the 450 continues processing the IOPB chain. If GBSY is clear, reload the IOPB Address Registers, and set GBSY to start a new chain.

2.6.2.6 Chain Interrupts

The 450 provides a single interrupt at the end of an IOPB. If other events which normally cause interrupts occur while the interrupt is asserted, then one interrupt signals several events. Interrupts are not stacked; an interrupt occurs after the 450 completes one IOPB, completes several chained IOPBs, or sets AACK. System software must determine why the interrupt occurred, and if it occurred for multiple interrupt requests. If the 450 completes three IOPBs at the same time, it generates only one interrupt. The 450 assumes that any complete IOPB has been taken care of by system software (at the time of setting GBSY or IPND, or resetting AREQ).

2.6.2.7 Completing a Chain

When all IOPBs in a chain are complete, the chain is complete. The 450 terminates the chain with an error if one IOPB has a hard error, and generates an interrupt, if enabled.

NOTE

> If the 450 successfully completes the chain, and EEF and IEI are set, it remains busy until it rescans the entire chain, ensuring all IOPBs are complete before it clears GBSY.

2.6.3 Error Recovery

Certain procedures may recover some errors. The errors are grouped below according to the recommended recovery procedure.

2.6.3.1 Errors 01, 03, 07, 0A, 17, 19, 1A, 1B, 1C, and 20

01	Interrupt Pending
03	Busy Conflict
07	Illegal Cylinder Address
0A	Illegal Sector Address
17	Sector Count Zero
19	Illegal Sector Size
1A	Self Test A
1B	Self Test B
1C	Self Test C
20	Illegal Head Address

These errors are either programming errors or hard failures. Do not retry the operation (for further explanation see Section 2.4).

2.6.3.2 Errors 04, 05, 06, and 16

04	Operation Timeout
05	Header Not Found
06	Hard ECC Error
16	Drive Not Ready

Retrying the operation may recover these errors. Execute two retries. If the error persists, consider it unrecoverable.

2.6.3.3 Errors 12, 18, and 25

12	Cylinder and Head/Header Error
18	Drive Faulted
25	Hard Seek Error

These errors indicate the drive may be off-cylinder. Issue a Drive Reset command, then retry the transfer. Setting the ASR bit in Byte 1 automatically accomplishes this.

2.6.3.4 Error 0E

0E	Slave ACK Error

The 450 attempted to access non-existent memory. Check the parameters issued, correct them, and try again.

2.6.3.5 Errors 0D and 19

0D	Last Sector Too Small
19	Illegal Sector Size

These errors occur during format and indicate the drive may be configured for an improper number of sectors. Verify the sector switches on the drive and the drive size for this Drive Type (See Section 3.4.2). Execute a Read Drive Status command and verify the returned sector count is correct.

2.6.3.6 Errors 13, 14 and 1F

13	Seek Retry Required
14	Write-protect Error
1F	Soft ECC Recovered Error

Software may log these errors for informational purposes only.

2.6.3.7 Error 1E

1E	Soft ECC Error

This error occurs when the 450 encounters an ECC recoverable error; system software may recover the operation as follows:

2.6.3.7 Error 1E (continued)

For a byte-oriented system, e.g., 8080 or 8085:

1. Reserve 16-bits of storage for the ECC Mask word (two bytes), and initialize them to zero.

2. Take the Mask word from the IOPB, reverse its bit order, and save the result in the least significant 16 bits of the storage allocated in Step 1.

3. Get the Bit Address word from the IOPB and subtract one. Since the bit address always starts at one, this causes the start to be at zero.

4. Shift the stored Mask word left using the least significant three bits of the adjusted bit address from Step 3 as a count. These three bits are the starting bit number within the byte.

5. Divide the bit address by eight (by performing three logical shifts to the right). The result is the byte offset into the data field where the stored Mask word is exclusive-ORed with the data. Adding this to the address at the start of the bad sector creates a pointer to the first Data byte to be corrected.

6. Exclusive-OR the Data bytes in ascending order, with the two Mask bytes, using the least significant Mask byte first.

For word-oriented systems:

1. Reserve 32-bits of storage for the ECC mask (two words), and initialize them to zero.

2. Reverse the bit order of the ECC Mask word, and save the result in the least significant word of the two-word mask storage allocated in Step 1.

3. Get the ECC bit address from the IOPB and subtract one, causing the bit count to start at zero rather than one.

4. Shift the stored Address Mask bits left, using the four low order bits of the adjusted ECC address of Step 3 as a count.

5. Divide the bit address by 16 (by performing four logical shifts to the right). The result is the word offset into the bad sector. Adding this offset to the start of a sector memory address creates a pointer to the first word to be corrected.

6. Exclusive-OR two consecutive words in the data with the mask.

2.6.4 Formatting

This section briefly describes how to format a disk. Several of these features are only supported by the 450-standard format. A 450 controller with a 440-compatible format does not support adaptive format. A 450 controller with a 440-compatible format cannot access a disk drive formatted with a 450-standard format, and vice versa.

2.6.4.1 Set Drive Size Parameters

Set the number of sectors per track in the drive size parameters equal to the number of sectors in an entire track (or use the default drive size parameters). Do not subtract the number of sectors for use as spares for later slipped sectors.

2.6.4.2 Drives With Fixed and Removable Media

Any physical drive with fixed and removable media, like the CDC CMD, or LMD, uses two Drive Types, but is accessed as one logical unit (i.e., the removable media of Unit 0 is Drive Type 2, and the fixed media of Unit 0 is Drive Type 3). The head offset refers to the bit(s) that must be set during a drive head select sequence to select between the fixed and removable portions of the drive. The 450 refers to both the fixed and removable media by the same physical Unit Number (See Section 2.5.12.3.5).

2.6.4.3 Format

Format the disk using the Write Format command. Write, read and verify the data. Format one cylinder at a time. Use several different patterns to be sure system software finds all the media defects. As software verifies the disk, build a table in memory of all the media defects it encounters. Recommended patterns include (hex values):

AAAA
FFFF
EBD6
D7AD
AF5B
5EB7
6DB6

2.6.4.4 Media Defects

Disk drives produce a soft error in approximately one out of every 10^{10} transfers. A sector is not bad if it fails once with a soft error. Rewrite the pattern and read the sector up to ten times, or until a second error occurs. If only one error occurs, the sector is not defective and there is no need to slip it. If a second error occurs, add the sector to the bad sector table and indicate if the error was a bad header, hard ECC, or soft ECC.

2.6.4.5 Read Defect Map (902-450-9xx Series Only)

The Read Defect Map command allows system software to read the manufacturer's defect list from an unformatted drive into memory, without entering it by hand. It reads the information from the drive, if the drive manufacturer supports the external defect format, and the drive is not formatted from the time the vendor ships it. After system software transfers the information into memory, it validates it, and slips the appropriate sectors.

2.6.4.5.1 Obtain the Defect Information

Issue a Read Defect Map command (See Section 2.5.17). This places the data into memory with the bit order reversed. Reverse the bits in each byte to their proper location.

2.6.4.5.2 Validate the Data

Validate the data in memory. The defect map does not incorporate any checksum; system software must validate the data to ensure it read the proper data. The first byte is a 19H. The following two bytes masked with 7FFFH comprise the cylinder address. The fourth byte is the selected head; and the twenty-first byte is a 0FH. Validate the data against these values. If the data is not valid, mark the entire track bad, or enter the data for that track by hand.

2.6.4.5.3 Save the Information

You lose the information when you format the drive. We recommend saving this information in a file which can be accessed at a later date.

2.6.4.5.4 Determine the Defective Sector or Track

Determine if the most significant bit (MSB) of the cylinder address is set. The 450 sets this bit if the entire track is defective. If the MSB of the cylinder address is clear, you must determine which sector(s) are defective.

You must know the exact drive configuration, in bytes per sector, to determine which sector(s) are defective. For example, a Fujitsu 2351A drive with the switches set for 47 sectors has 600-bytes per sector. The same drive switched for 46 sectors has 613-bytes per sector. The drive manufacturer's manual contains enough information to determine the number of bytes per sector for the drive. Take the position of each defect and divide it by the the number of bytes per sector for your drive. The truncated value is the defective sector number. Use this defective sector number when marking bad sectors.

The following procedure determines the defective sector for adaptive format: Issue a Read Track Headers command. This fills the memory with sector headers. Multiply the defective sector number by four, and add this value to the buffer pointer. This value points to the Header bytes for the defective sector.

2.6.4.6 Reset Drive Size Parameters

Set the drive size parameters equal to the number of desired data sectors per track. This value equals the number of physical sectors the drive can hold minus the number of spare (slip) sectors desired, and the runt sector (if it exists).

2.6.4.7 Reformat the Disk

The Format command reformats the entire disk. The 450 formats all spare sectors with a header value of DDDDH, DDDDH; it formats the runt sector, if it exists, with a header value of EEEEH, EEEEH.

2.6.4.8 Slip Defective Sectors

Using the procedure in Section 2.6.5, slip the defective sectors and mark them bad.

2.6.5 Slip a Sector

This section describes how to slip sectors.

2.6.5.1 Read Track Headers

System software must allocate a buffer in system memory to store the sector header information during this procedure. The buffer length (in bytes) must be four times the total number of sectors. Issue a Read Track Headers command for the track that contains the sector(s) to be slipped.

2.6.5.2 Record Bad and Spare Sectors

Determine which sectors are spares, and which are bad. Build a table in memory with two variables: the physical sector number from index, and the status of that sector (good - bad - spare). The following example shows the data buffer contents after a Read Track Headers operation.

Data	Physical Sector	Logical Sector	Status
36H,03H,04H,40H	1	0	good
36H,03H,04H,41H	2	1	good
36H,03H,04H,42H	3	2	good
36H,03H,04H,43H	4	3	good
EEH,EEH,EEH,EEH	5	-	bad
36H,03H,04H,44H	6	4	good
: : : :	:	:	good
: : : :	:	:	good
36H,03H,04H,5FH	33	31	good
DDH,DDH,DDH,DDH	34	-	spare

A table constructed for the example above would consist of sectors 1-4 good, 5 bad, 6-33 good, and 34 spare.

2.6.5.3 Spare Sector Available

Determine if enough spare sectors are available. There must be a spare sector available for every sector to be slipped.

2.6.5.4 Determine Sector To Be Slipped

Determine which sector is to be slipped. First determine the absolute sector number in relation to index. Add it to the number of bad sectors that exist between index and the sector to be slipped. The absolute sector number equals the logical sector number if interleaving is 1:1, and there are no defective sectors. Add in the head number if you are using the 450-standard format (adaptive format).

The interleave factor must adjust the absolute sector number if the drive is interleaved. The following program determines the interleaving. It provides a vector of interleaved sector numbers such that:
A (physical) = interleaved.

<SECTOR SLIP SAMPLE PROGRAM TO BE SUPPLIED AT A LATER DATE>

For example, upon reading a track interleaved 2:1 (with Head 0), system software arranges the sectors as follows:

0, 16, 1, 17, EEEE, 2, 18, 3, 19, 4, 20, 5, 21, 6, 22, 7, 23, 8,
24, 9, 25, 10, 26, 11, 27, 12, 28, 13, 29, 14, 30, 15, 31, DDDD.

2.6.5.4 Determine Sector To Be Slipped (continued)

The table described in Section 2.6.5.2 lists sectors 1-4 good, 5 bad, 6-33 good, and 34 spare. Software determines logical sector 4 is defective. The algorithm determines the absolute sector number is 9. There is one defective sector between index and the sector to be slipped; the physical sector to be slipped is Sector 10. The table, with its new entry, reads: 1-4 good, 5 bad, 6-9 good, 10 bad, 11-33 good, and 34 spare.

2.6.5.5 Slip Sectors

Using the updated table in Section 2.6.5.3 and the vector generated in Section 2.6.5.4, modify the buffer in preparation for the Write Track Headers command. Start at the beginning of the buffer and set up the header for the first sector. The following procedure outlines the steps used to modify the buffer.

1. Get the physical sector number to be modified.

2. Multiply this number by four bytes and add it to the buffer start address to determine where that sector's header begins.

3. Determine if this sector is to be good, bad, or spare. If bad, the four Header bytes are EEH, EEH, EEH, EEH. If spare, the Header bytes are DDH, DDH, DDH, DDH. If this sector is good, the first byte is the LSB cylinder, the next byte is the MSB cylinder, the next byte is the head, and the last byte is the new sector number ORed with the Drive Type code (See Section 2.5.11.3.1).

4. Determine the new sector number (using the interleave algorithm), the physical sector number, and the number of bad sectors encountered so far. Take the physical sector number and subtract the number of bad sectors found between it and index. Use this value to determine the new sector number which software ORs with the Drive Type and places into the buffer.

5. Continue setting up the buffer for each physical sector on the track. Use the procedure outlined above to determine how to set up each sector.

NOTE

The physical locations of bad sectors must not be moved with relation to index. The media defects do not move when slipping sectors; any physical sector marked bad must remain bad. Runt sectors also cannot move with relation to index.

2.6.5.6 Marking Entire Tracks Defective

If an entire track is marked defective, use a pattern of 7FH in the four Header bytes (See Section 2.5.4). The 450 does not support track slipping.

2.6.5.7 Write Track Headers

Use the Write Track Headers command to write the modified headers to the disk to reformat the track with slipped sectors. Once reformatted, the defective sectors are transparent to the operating system through normal Read and Write commands. The 450 can access both good and defective sectors when using Read or Write Header, Data, and ECC operations.

2.6.5.8 Sector Slip With Live Data

If the disk has live data, the following procedure allows you to slip a sector and not lose the data on the disk. This procedure requires a full track buffer; we recommend using a stand-alone program.

1. Allocate a full track buffer in memory, and read a track into memory. Use ECC Mode 2 (it corrects the bad data, if possible).

   - OR -

   If a full track buffer is not available in memory, allocate disk space, and store the data in that space.

2. Use the sector slip procedure to slip the sector with the error.

3. Use a normal Write command to write the data from the buffer back to the disk. The 450 compensates for slipped sectors.

2.6.6 Using Drive Types

The 450 must know the drive size parameters, number of sectors per track, number of heads per cylinder, and number of cylinders. The 450 allows drive size information to be downloaded on a per Drive Type basis. On the 450, the function of defining a drive size parameter is linked to the Drive Type versus the Unit Number. The advantage of this is only one Set Drive Size command is necessary if all the connecting drives are the same size. Another advantage is the controller tests for the Drive Type during a Header Compare operation.

2.6.6.1 Drive Types Determine Drive Size

The Drive Type bits in IOPB Byte 5 indicate the size of the drive the 450 is working with. There are four Drive Types available, 0 through 3. The Set Drive Parameters command allows system software to assign a specific Drive Type to a specific drive size.

For example, a given system has four drives. Two of the four drives are CDC 9762 80 MB drives (call these Drive Type 1); the other two are CDC 9766 300 MB drives (Drive Type 2). Execute a Set Drive Parameters command, using the following parameters, to set Drive Type 1: 5 heads, 823 cylinders, and 32-sectors per track. Drive Type 2 uses the parameters: 19 heads, 823 cylinders, and 32-sectors per track. In this hypothetical system, whenever the 450 talks to an 80 MB drive, system software must access it as Drive Type 1 (along with the required Unit Number). System software refers to the 300 MB drives as Drive Type 2 and selects the appropriate Unit Number.

2.6.6.2 Drive Types Tested by the 450

Two bits in the sector field of each header on the disk comprise the Drive Type. The 450 compares the Drive Type bits in the expected header to the header it reads from the drive during a Header Compare operation.

2.6.6.3 Extended Use of Drive Type

The 450 also uses the Drive Type to differentiate between the fixed and removable portions of a disk drive. System software can specify a Head Offset byte to determine which portion of the drive it is referencing (See Section 2.5.12.3.4).

2.6.6.4 Controller Use of Drive Type

System software specifies the Drive Type so the 450 knows how to address the disk drive. Software writes the Drive Type into the header on the disk to prevent accidental addressing of a drive with the wrong Drive Type. A Read Header, Data, and ECC command on Sector 0 of Cylinder 0 retrieves the Drive Type from a formatted disk. Software may poll all the disks to determine Drive Types (See Section 2.5.11.3.1 to locate the Drive Type field in the header information).

Accessing a drive with an incorrect Drive Type results in a Header Not Found error. It is imperative that system software specify the correct Drive Type for the selected disk drive.

2.6.6.5 Header Drive Type Always Equals Zero (902-450-9xx Series Only)

The 450 normally puts the Drive Type bits in the header field of each sector on the disk. This ensures the controller and media are properly configured for each other, and for 440-compatibility. You can override this feature with an option during a Set Drive Size command. Use these definitions to clarify the following sections:

- o Drive Type : Refers to the bits in Byte 5 of the IOPB.
- o Header Drive Type : Refers to the bits placed in the header field of each sector.
- o Header Drive Type 0: Refers to this new option.

Typically, writing Drive Types in the header works well, but problems can occur. For example, a systems house can provide any four drives (out of a possible fifteen) with its configurations. System 1 includes Drives A, B, C, and E; each are assigned Drive Types 0 through 3, respectively. System 2 includes Drives D, E, F, and G; again, each are assigned Drive Types 0 through 3, respectively. This is fine as long as Drive E is not moved from System 1 to System 2 to exchange information.

The problem is that in System 1 Drive E was formatted with Drive Type 3, so the Header Drive Type is 3. When System 2 tries to read the disk, it will report a Header Not Found error since it is looking for Header Drive Type 1, not 3. You can easily work around this situation by assigning Drive Type 3 to Drive E on

2.6.6.5 Header Drive Type Always Equals Zero (continued)

both systems. The real difficulty arises when you have one hundred systems, each with different drives, and don't know in advance which drives will exchange software.

The 902-450-9xx series 450 firmware contains an option to set the Header Drive Type to 0, rather than setting it to the Drive Type specified in IOPB Byte 5. This allows the mixing and matching of more than four different drives, regardless of the Drive Type used during formatting.

2.6.6.5.1 Enabling Header Drive Type 0

Enable Header Drive Type 0 by setting bit 6 in the Head Offset byte (IOPB Byte 10), during a Set Drive Size command, for the Drive Type you wish to reset. You can selectively enable this option on a per Drive Type basis.

2.6.6.5.2 Function of Header Drive Type 0

When using a Drive Type that enables Drive Type 0, all operations that compare headers expect a zero in the Header Drive Type. The 450 puts a zero in the Header Drive Type during Format operations.

2.6.6.5.3 Using Header Drive Type 0 on Preformatted Disks

If a disk is formatted with a Drive Type other than zero, and this option is not enabled, all transfers to this disk must be specified with the formatted Drive Type, and this option may not be enabled.

If a disk is formatted with Drive Type 0, and/or this option is enabled, all transfers to this disk may be made with either Drive Type 0 (with or without this option enabled) or another Drive Type, with this option enabled.

2.6.7 Dual Port Drive Operation

Dual ported drives require system software to be more careful in its use of disk space. Software must be able to handle the possibility that one of the controllers will not release the drive, preventing the other controller from gaining access. When accessing a disk during file operations, keep the Hold Dual Port bit set to hold the drive until the directory is updated.

Many drives which have a dual port option also have a protection timeout that releases a channel after a specified time period if the drive is deselected, but not released. You can disable this timeout in the drive (refer to your drive manual).

2.6.7.1 Drive Space Allocation

Two controllers can write to dual ported drives. When system software allocates space on the disk, it is unaware that another controller may be allocating the same sectors. This can cause two files to corrupt each other. When using dual ported drives, it is a good idea to allow only one controller write access to the disk. If this is impractical, then configure one

2.6.7.1 Drive Space Allocation (continued)

controller to allocate the space on the disk, and the other to only write into that allocated space.

2.6.7.2 Failure to Gain Access

Occasionally, a controller fails to gain access to a dual ported drive. In this case, the 450 times out the operation after waiting two seconds after it completes the other IOPBs, or it posts a Drive Not Ready error. The 450 terminates the chain if an error occurs; system software may remove any IOPBs for that drive. Issue a Read Drive Status command to determine the dual port busy status.

2.7 PERFORMANCE CONSIDERATIONS

This section suggests how to get the best possible performance from the 450 for your particular application. It discusses the various tradeoffs, their advantages and disadvantages.

2.7.1 Throttle Considerations

From the 450 disk controller's viewpoint, the throttle value should be as high as possible, so the controller never has to skip revolutions. You may have a real time application that must access the bus periodically.

In these applications:

- Determine the maximum time the 450 can be bus master (less time than another unit can be without the bus).
- Determine your memory's response time, add 500 ns and divide that figure into the allowable 450 bus master time. The result is the maximum throttle value.
- Pick the figure closest to the 450 throttle value without going over the actual amount.

2.7.1.1 Common Bus Request (902-450-9xx Series Only)

If the Common Bus Request (CBRQ/) feature is enabled (See Section 4.2.7), the 450 tests the CBRQ/ signal at the end of each throttle burst. If CBRQ/ is asserted, the 450 releases the bus. If CBRQ/ is disabled at the end of a throttle burst, the 450 continues as bus master and executes the next transfer. Using CBRQ/ can improve throughput as it saves bus exchange overhead time in situations where no other master requires the bus. The 450 normally releases the bus after every DMA throttle burst.

2.7.1.2 High Throttle Advantages

- Maximum disk throughput with minimum missed revolutions.
- Maximum bus throughput with minimum bus overhead.

2.7.1.3 High Throttle Disadvantages

- Tendency to "hog" the bus - time critical devices fail.
- Other DMA units may not get enough bus time.

2.7.2 Word or Byte Mode

Word mode is definitely more efficient than Byte mode on the bus. It takes the same length of time to transfer a word in Word mode as it does a byte in Byte mode. Therefore, using Word mode effectively doubles the 450's throughput.

2.7.2.1 Word Mode Advantages

- Increased throughput with less bus utilization.
- Helps DMA keep up with the disk.

2.7.2.2 Word Mode Disadvantages

- Works only on word-oriented memory.

2.7.3 Transfers on Address Boundaries

The 450 reacts differently to transfers on various address boundaries. Word mode transfers on odd addresses must compensate for the odd address. The 450's internal architecture dictates how it handles transfers across page boundaries.

2.7.3.1 Odd Address Transfers

If you specify an odd address, the 450 transfers the data in Byte mode, even if Word mode was selected.

2.7.3.2 Transfers to Page Addresses

Each time the 450 crosses a 256-byte address boundary, the on-board microprocessor updates the upper address bits and restarts the DMA sequencer. Align transfers on address boundaries to minimize this occurrence (this is advantageous if you require the 450's absolute maximum throughput).

2.7.4 Interleaving

Interleaving increases throughput on either a fully loaded system or one in which the operating system response time is slow. Interleaving effectively cuts the disk speed in half for 2:1, or a third for 3:1 interleaving, etc. When formatting interleaved, format a full track or multiples of full tracks, starting with Sector 0.

2.7.4.1 Advantages of Interleaving

- Maximum throughput on fully loaded systems.

  Fully loaded systems usually have many DMA devices contending for bus time. In this environment, the 450 may fall behind the disk, stop the transfer, and wait one revolution before the next sector arrives under the head. This slows the disk subsystem. If the disk is interleaved, the data rate is much slower. Therefore, the 450's bus requirements are much lower.

2.7.4.1 Advantages of Interleaving (continued)

o Maximum throughput on slow software systems.

  Slow software systems cannot turn around interrupts in a reasonable amount of time, and usually transfer one sector at a time. In this environment, interleaving allows the system to catch many sectors per revolution instead of just one as on a non-interleaved disk.

o Less chance of missing revolutions.

2.7.4.2 Disadvantages of Interleaving

o Slows data throughput from the disk by the interleave factor.

2.7.5 Chaining Operations

Command-chaining results in several performance advantages:

The 450 may automatically initiate overlap seeking, which dramatically increases performance throughput in multidrive systems.

System software does not have to respond as rapidly at the end of a command; the 450 continues to the next command without any operating system intervention. The 450 interrupts at the end of each IOPB to notify the system that the IOPB is complete.

2.8 MEDIA FORMAT

The 450 supports two different media formats: the 440-compatible format, used for media compatibility with the 440 disk controller; and the 450-standard format. The new SMD+ (1.9 MBS) drives require the 450-standard format.

2.8.1 440-Compatible Format

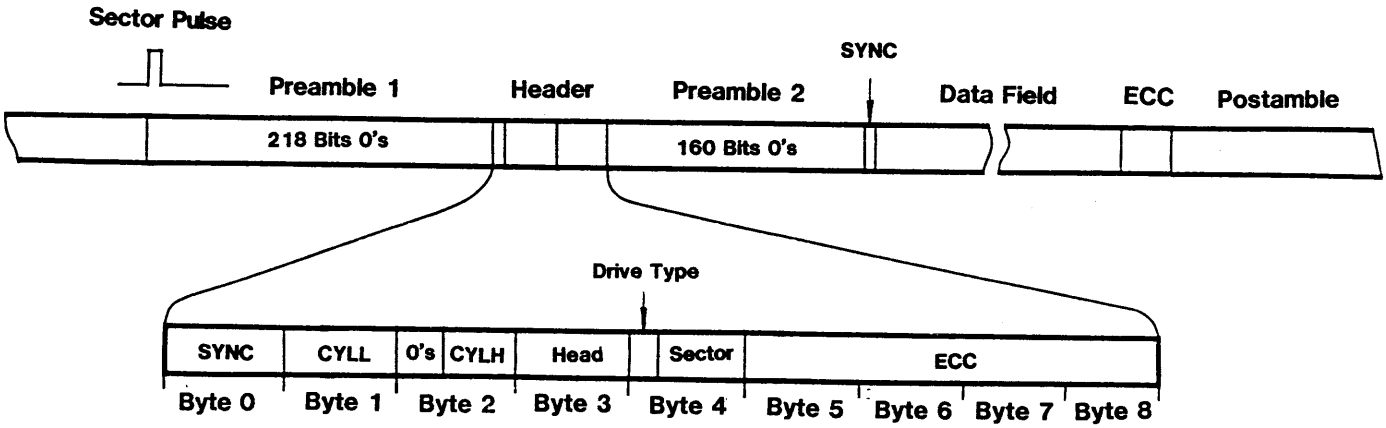
This format is compatible with the 440 disk controller. Figure 2-3 illustrates the actual format on the media with an enlarged view of the header area.

2.8.2 450-Standard Format

The 450-standard format is more efficient in its use of disk space. It allows more sectors per track than the 440-compatible format. Figure 2-4 illustrates the format with a layout of the Header bytes.

2.8.3 Adaptive Format

The 450-standard format uses adaptive format. The adaptive format causes logical Sector 0 to slip one sector from physical index for each track. The 450 resets the logical to physical relationship to 1:1 on Track 0 of each cylinder. This feature allows the 450 to store more data per track since the adaptive slip masks the head switching time. Figure 2-5 illustrates the relationship between index and logical sector mapping. This figure represents a 32-sector disk with two spare sectors.



SYNC=10011000

440-Format

FIGURE 2-3. 440-COMPATIBLE FORMAT

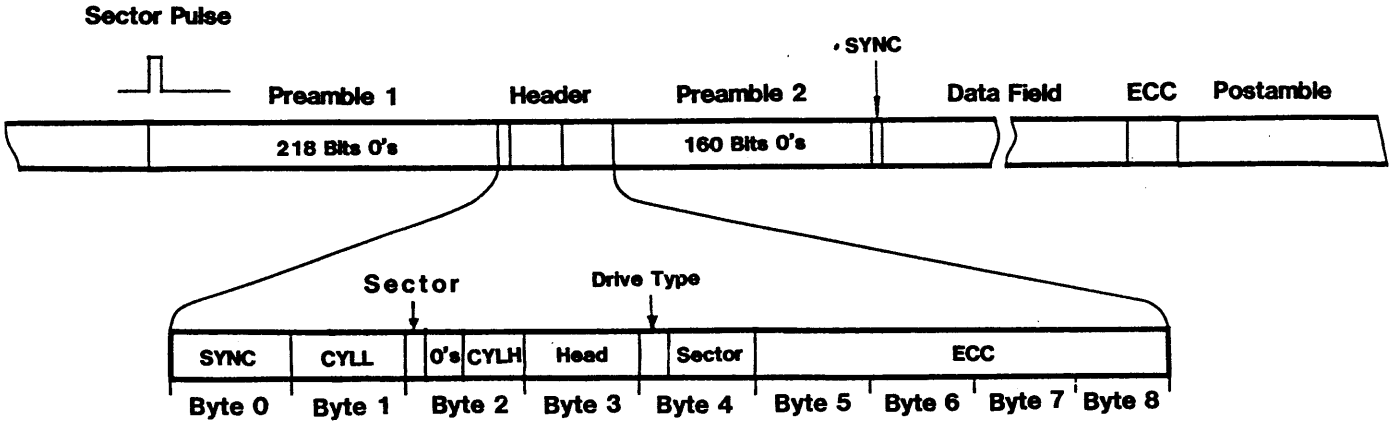
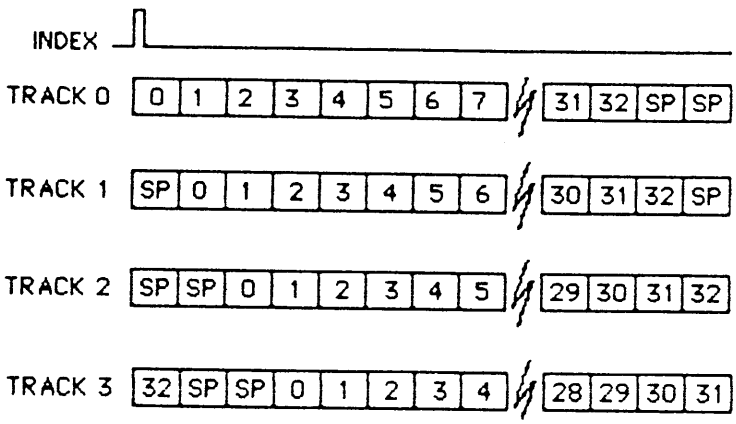


FIGURE 2-4. 450-STANDARD FORMAT



ADAPTIVE FORMAT

FIGURE 2-5. ADAPTIVE FORMAT

SECTION 3: INSTALLING AND TESTING THE 900-450-9xx SERIES 450

3.0 GENERAL

The following section describes how to unpack, configure, install, and test your 900-450-9xx series 450 controller. Section 4 describes how to configure the 902-450-9xx series.

3.1 UNPACKING AND INSPECTION

3.1.1 Inspect the Shipping Carton

Inspect the carton for possible shipping damage. If you determine there is damage, do not unpack the unit. Notify Xylogics and the freight carrier immediately.

If no damage is visible, carefully unpack the 450. Save the carton and other packing material for possible later use.

3.1.2 Contents

The 450 is a single printed circuit board. Optional items include a manual and/or software on a floppy diskette, or 1/2-inch magnetic tape.

If any items are missing or damaged, please contact Xylogics at one of the following telephone numbers:

United States :	(617) 272-8140
United Kingdom:	44-753-78921
International (Slough):	78921

3.1.3 Inspect the 450

Inspect the 450 for socketed parts that may have loosened during shipment. Assure that all parts are firmly seated in their sockets. If any parts must be reinserted, observe proper orientation.

3.2 CONFIGURING THE 450

You can configure the 450 with several jumper options. The following paragraphs describe these options (See Figure 3-1 for a board layout).

3.2.1 Base Address Selection

There are two separate parts to selecting the base address. First, select a response to 8 or 16-bit register addresses. Jumper JA/JB 10 controls this option.

JA/JB 10: installed = 8-bit address
removed = 16-bit address.

Jumpers JA/JB 2-9, JE 4-5, and JC/JD/JR 1-4 control the actual base address. If you select 8-bit addressing, the jumpers for address bits 0-7 are the only valid jumpers. Ignore the jumpers for bits 8-F. Table 3-1 shows how to set the jumpers for commonly used base addresses.

3.2.1 Base Address Selection (continued)

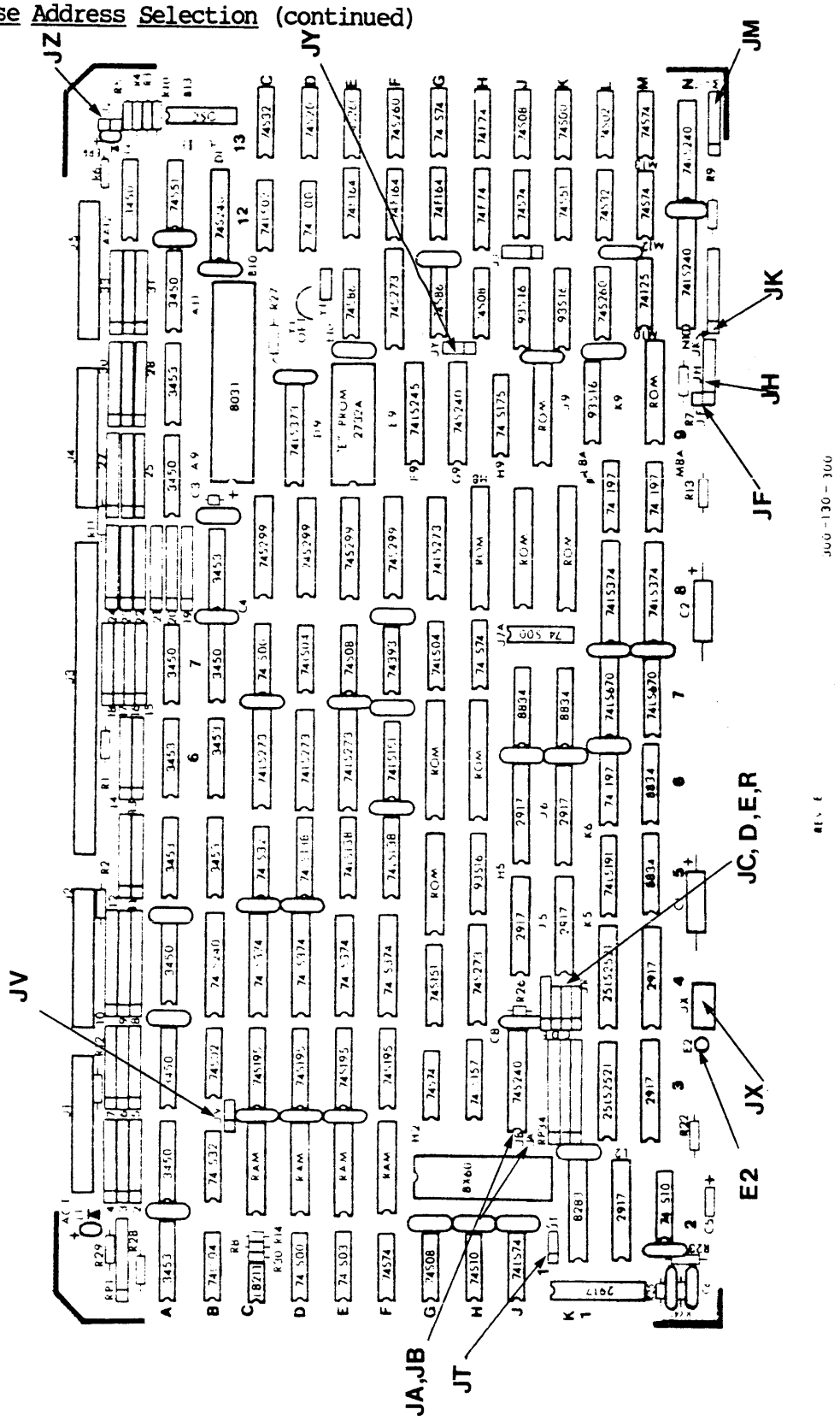


FIGURE 3-1. 450 COMPONENT LOCATION

3.2.1 Base Address Selection (continued)

Use Figure 3-2 and Table 3-1 in configuring the base address to your needs. The jumpers are divided into three groups: jumper blocks JA and JB control address bits 8-F; jumper blocks JR, JC, and JD control address bits 3-6; and jumper JE 4-5 controls address bit 7.

Inserting or removing a jumper between jumper blocks JA and JB controls address bits 8-F. Installing a jumper asserts a zero on the address comparator for that bit; no jumper asserts a one. Connect a jumper between similar pin numbers on each block. For example, if address bit D is to be a zero, install a jumper from JA pin 6 to JB pin 6.

Treat address bit 7 the same as bits 8-F, but connect the jumper from JE pin 4 to JE pin 5.

Jumper blocks JC, JR, and JD control address bits 3-6. Connect a jumper between blocks JR and JC to assert a one on the address comparator for that bit. Connect a jumper between blocks JC and JD to assert a zero on the address comparator for that bit. Install a jumper between JC pin 4 and JD pin 4 to assert a zero for address bit 3. Install a jumper between JR pin 3 and JC pin 3 to assert a one for address bit 4. Factory setting: 40 (8-bit).

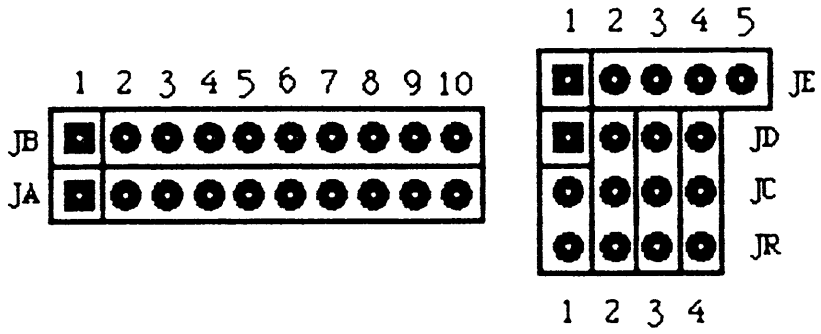


FIGURE 3-2. BASE ADDRESS SELECTION

3.2.1 Base Address Selection (continued)

Address Bits:	F	E	D	C	B	A	9	8	7	6	5	4	3	8/16
Pin Numbers:														
Jumper JR/JC/JD:										1	2	3	4	
Jumper JE 4-5:									X					
Jumper JA/JB:	2	4	6	8	9	7	5	3						10
Address:														
40 - 8-bit*	X	X	X	X	X	X	X	X	I	RC	CD	CD	CD	I
EE40 - 16-bit	O	O	O	I	O	O	O	I	I	RC	CD	CD	CD	O
50 - 8-bit	X	X	X	X	X	X	X	X	I	RC	CD	RC	CD	I
0050 - 16-bit	I	I	I	I	I	I	I	I	I	RC	CD	RC	CD	O

*Standard Factory Configuration

O = Out; I = In; X = Don't Care; RC = Jumper From JR To JC; CD = Jumper From JC To JD.

TABLE 3-1. BASE ADDRESS SELECTION

3.2.2 20/24-Bit Address Relocation

The 450 functions in backplanes of 16, 20 and 24-bit addresses. Jumpers select the 20-bit or 24-bit Addressing mode. Software selects the 16-bit Addressing mode. System software determines the status of the jumper by reading bit 3 of the CSR. If set, the board is jumpered for 24-bit addressing. Both 20 and 24-bit Addressing modes support 16-bit addressing.

Mode	JM 1-2	JM 3-4
16/20	Out	In; Factory Configuration
16/24	In	Out

3.2.3 24-Bit Address Jumpers

The 450 drives the upper address lines (with zero) in the 20-bit Addressing mode. If you require the address lines to float, remove the following jumpers (the factory installs these jumpers):

ADR14H	JM 5-6
ADR15H	JK 5-6
ADR16H	JK 1-2
ADR17H	JK 3-4

3.2.4 Interrupt Request Levels

You can choose any one of eight interrupt request levels. The factory jumpers the 450 for INT5/. To select an interrupt level, connect a jumper as per Table 3-2.

3.2.4 Interrupt Request Levels (continued)

Interrupt Request Level	Pin to Pin
INT0/	E2 JX 2
INT1/	E2 JX 7
INT2/	E2 JX 4
INT3/	E2 JX 5
INT4/	E2 JX 8
INT5/	E2 JX 3
INT6/	E2 JX 6
INT7/	E2 JX 1

TABLE 3-2. INTERRUPT REQUEST LEVELS

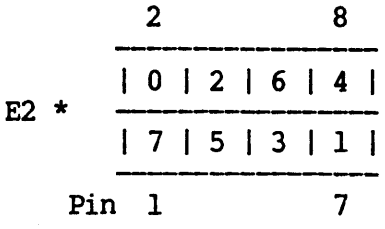


FIGURE 3-3. INTERRUPT LEVEL VS. LOCATION ON JX CONNECTOR

3.2.5 Disable Bus Priority Out

If you are using the 450 in parallel DMA arbitration (See Section 3.3.2.2), isolate the Bus Priority Out (BPRO/) signal from the Multibus by removing the jumper from JE 1-2. Factory setting: serial arbitration.

3.2.6 Power-fail Protection

Certain Multibus systems allow AC power-fail protection. Install jumper JH 1-2 and provide an appropriate power-fail signal on pin 18 of the P2 connector. This signal should go to ground when the AC power source fails. Using an AC (versus DC) power-fail indicator allows the 450 more time to protect the drive from accidental spiral writes. The 450 has on-board DC power loss detection circuitry. The 450 is normally configured with DC power-down protection. Factory setting: jumper JF/JH 1 installed.

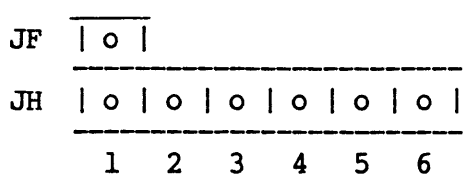


FIGURE 3-4. POWER PROTECTION / DMA CLOCK SELECTION

3.2.7 Remote Activity Indicator

An on-board LED indicates when the controller is busy. A remote activity indicator signal is available on the backplane; install jumper JK 7-8 and wire the remote LED between +5 volts and pin 42 of Multibus P2 connector. Factory setting: JK 7-8 out.

3.2.8 Factory Use Only

The 450 has several jumpers which should not be changed since they are for factory use only. Some of these jumpers are hard wired, and not jumper strips.

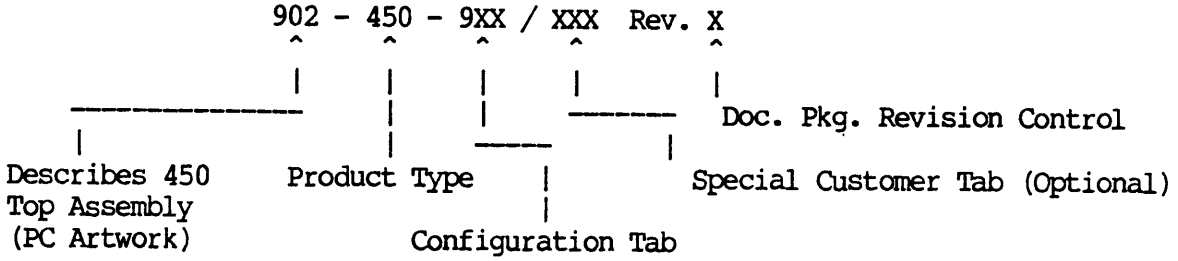
Jumper	Status	Description
JY 2-3	In	Closes ECC Feedback Loop
JY 1-2	Out	
JJ 1-2	Out	Selects Clock for Disk Sequencer
JJ 3-4	In	
JH 5-6	In	Selects Clock for DMA Sequencer
JH 3-4	Out	
JZ 1-2	In	Enables Crystal Clock

	Standard (2 KB)	Optional (8 KB)
JT 1-2	Out	In
JT 2-3	In	Out
JV 2-3	In	Out
JV 1-2	Out	In

3.2.9 Firmware and Sector Size

The disk sequencer PROMS contain parameters which control the sector size and format type. Use the following information to ensure your 450 was properly configured at the factory.

The following part numbers describe the product version, type, and configuration. These documentation package numbers (DPNs) are used throughout the ordering and manufacturing process. The DPN appears on the non-component side of every controller.



3.2.9 Firmware and Sector Size (continued)

PROMS for Various 450 Configurations

Order Number	Part Number 180-001-xxx Loc. J8	Loc. J9	Bytes/Sector	Buffer Size	Format Compatibility
900-450-900	961	962	512	2 KB	440
900-450-901	965	966	512	8 KB	440
900-450-902	967	968	256	2 KB	440
900-450-903	969	970	256	8 KB	440
900-450-904	954	956	512	2 KB	450
900-450-905	963	964	512	8 KB	450
900-450-906	971	972	256	2 KB	450
900-450-907	973	974	256	8 KB	450
900-450-908	975	976	1024	2 KB	450
900-450-909	977	978	1024	8 KB	450
900-450-910	961	962	512	2 KB	450
900-450-911	992	993	2048	8 KB	450
900-450-912	980	979	1056	2 KB	450
900-400-913	963	964	512	8 KB	450
900-450-914	980	979	1056	2 KB	450
900-450-915	029	030	768	8 KB	450

900-450-9xxV -5V Daughter Board Option

TABLE 3-3. SECTOR / BUFFER SIZE CONFIGURATIONS

3.2.9 Firmware and Sector Size (continued)

PROMS / PALS Not Modified

Location	Part Number	
M9	181-001-003	PAL
H8	180-001-953	Disk Sequencer
K8	180-001-955	
E9	180-001-952	EPROM
	180-001-981	EPROM
	180-001-997	EPROM
G5	180-001-949	DMA Sequencer
G6	180-001-950 or	
	180-001-996	
H6	180-001-951	

TABLE 3-4. PROM / PAL PART NUMBER AND LOCATION

3.3 PREPARING THE COMPUTER SYSTEM

The backplane of your system must provide a Multibus slot for the 450. The slot must be capable of handling a bus master, and the power source must handle the power consumption of the entire system, including the 450.

3.3.1 Card Cage Slot

The card cage must have a slot available for the 450. Placement of the 450 in the DMA priority chain may be critical; consider this when choosing a slot.

3.3.2 DMA Bus Arbitration

The 450 uses either serial or parallel DMA arbitration. Serial arbitration is much easier to implement, but has restrictions on the number of bus masters it can arbitrate. Parallel bus arbitration is more difficult to implement, but is more versatile and can handle more bus masters.

3.3.2.1 Serial DMA Priority

To implement serial priority, connect the BPRO/ and BPRN/ lines in a serial fashion (See Figure 3-5). The first slot has the highest priority, and must have its BPRN/ line grounded. The next slot has the next highest priority. A unit must have its BPRN/ line asserted to become bus master. If a unit is not currently a bus master, it passes the state of the BPRN/ to the BPRO/. If the unit is bus master, it deasserts its BPRO/ so the following units will not have their BPRN/ lines asserted and therefore cannot become bus master.

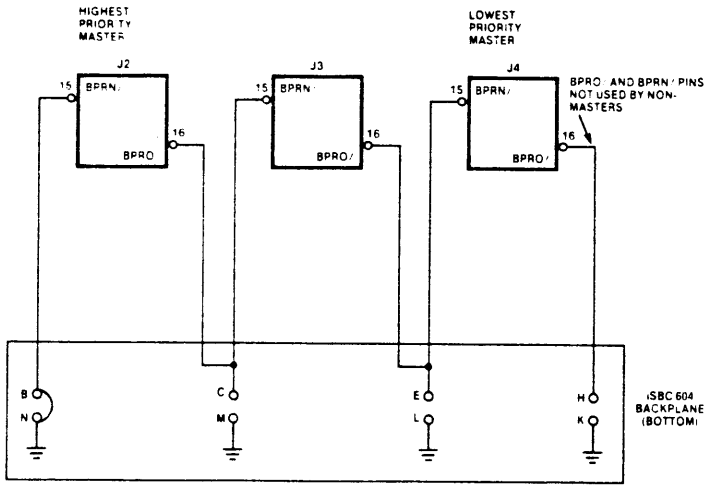


FIGURE 3-5. SERIAL DMA PRIORITY

3.3.2.2 Parallel DMA Priority

Parallel and serial priority use the same connections to each board. To implement parallel priority, connect these signals to an external circuit similar to that of Figure 3-6. The Bus Request (BREQ/) line requests the bus. The external circuit performs bus arbitration. Since the BPRN/ line of one board usually connects to the BPRN/ line of the next board, the circuit shown in Figure 3-6 has two outputs tied together. You can correct this by disabling BPRO/ from each board (See Section 3.2.4).

3.3.2.2 Parallel DMA Priority (continued)

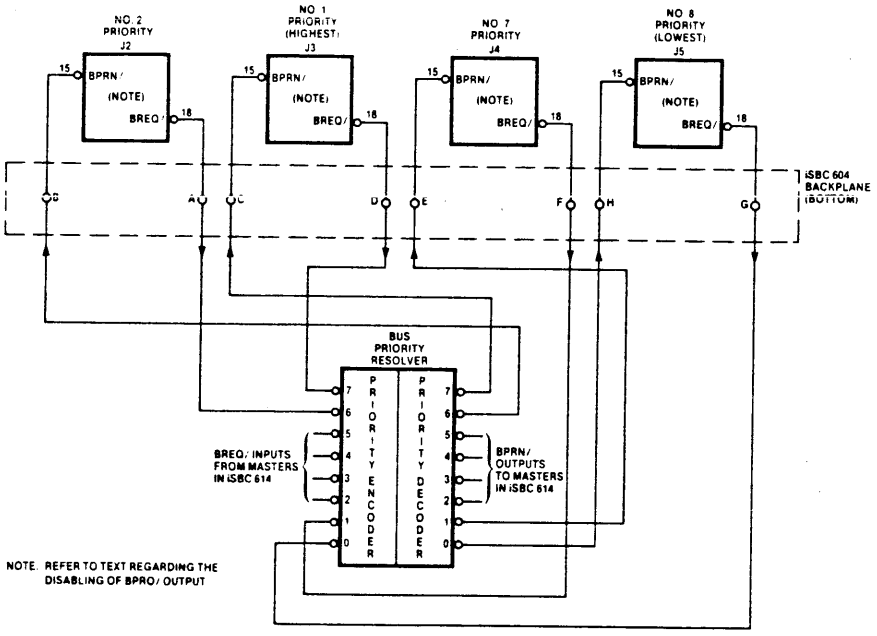


FIGURE 3-6. PARALLEL DMA PRIORITY

3.3.3 Power Considerations

The 450 uses -5 volts to power the differential drivers/receivers for the SMD interface. This helps keep heat-producing components off the controller board, and allows you to put them in a more appropriate location. The 450 can be configured with an optional regulator daughter board, which generates -5 VDC from -12 VDC; this option cannot be installed in the field (contact the factory for further information).

The 450 affects the power consumption of the entire computer system. Be sure the power supplies can handle the entire power load. Readjust the voltages AFTER plugging in the 450. A power supply that is just adequate may cause intermittent and unusual problems due to noise generated by occasionally going into overcurrent protection.

Limits: 5 volts (4.75 to 5.25 volts)
-5 volts (-4.75 to -5.25 volts).

3.4 DISK DRIVE PREPARATION

Inspect the shipping carton; if you suspect shipping damage, notify the carrier immediately. If no damage is visible, unpack the drive and remove any shipping constraints.

Configure the drive for use with the 450. This entails setting up such parameters as the Unit Select, number of sectors per track, and ensuring the sector and index pulses are provided on the "A" cable. Consult the drive manual for the exact method of configuring your drive.

3.4.1 Drive Unit Select

A plug on the front of the drive, or switches on one of the drive's internal circuit cards, usually selects the drive Unit Number. The 450 accesses drives with Unit Numbers ranging from 0 through 3. Set the first drive to Unit 0.

3.4.2 Number of Sectors Per Track

Switches on one of the drive's internal circuit cards usually select the number of sectors per track (See Table 3-5). The 450-standard format uses 88-bytes of overhead per sector. Table 3-6 indicates the sector switch settings for the Control Data Corporation 9762 disk drive.

If you are using the sector slip feature, the number of sectors available to the program is the number of allocated sectors less the spares (See Section 2.5.5 for more information on the Sector Slip command).

The actual setting of the drive switches may be different than the number of data sectors required. Most disk drives have a runt sector (a very small sector at the end of the disk). The 450 requires all sectors on a track to be formatted; it returns the Completion Code 19H if the runt sector is too small to format. Prevent this error by resetting the sector switches in the drive to compensate for the runt.

The 450 also returns the Completion Code 19H if the last sector is too small to be a data sector but it is included in the max sector value. For example, the Fujitsu 2351 has 46-data sectors per track. The last sector has 575 bytes (which is too small to be a data sector) if you set the drive switches to 46. If you set the drive to 47 sectors, all sectors are large enough to be formatted, and 46 sectors are large enough to be data sectors.

The minimum runt allowed for a SMD+ (1.9 MBS) speed drive is 150 bytes. A standard SMD (1.2 MBS) speed drive runt is 120 bytes. Either drive accepts a runt of zero.

3.4.2 Number of Sectors Per Track (continued)

Data Bytes Per Sector	256	512	256	512	1024	2048
Media Compatibility	440	440	450	450	450	450
Minimum Bytes/Sector*			344	600	1112	2136
Bytes/Track - Bit Cell						
13,440 - 155 ns	N/A	22	41	23	12	6
20,160 - 103 ns	60	32	60	33	17	9
20,480 - 102 ns	60	32	60	34	18	9
20,480 - 123 ns	60	33	63	35	18	9
28,160 - 66 ns	N/A	N/A	86	46	25	13

TABLE 3-5. MAXIMUM NUMBER OF SECTORS PER TRACK

Switch:	0	1	2	3	4	5	6	7	8	9	10	11
Sectors: 9	+	-	+	O	+	+	+	O	O	+	O	+
17	+	O	+	O	O	O	O	O	+	O	+	+
32	O	O	+	+	+	O	+	O	O	+	+	+
33	+	O	O	+	O	+	+	O	O	+	+	+
34	+	+	+	O	+	+	+	O	O	+	+	+
60	O	O	O	O	O	+	O	O	+	+	+	+
64	O	+	+	+	O	+	O	O	+	+	+	+

O = Closed; + = Open

TABLE 3-6. SECTOR SWITCH SETTINGS FOR CDC 976X

NOTE

Sector switch settings for running at 9 or 17 sectors are special settings and not described in the CDC drive manual.

3.4.3 Sector and Index Pulses

Both the "A" (Control) cable and the "B" (Radial) cable can provide the sector and index pulses. Disk vendors usually provide drives with sector and index on the "A" cable. The 450 requires the "A" cable to carry sector and index.

3.4.4 Disable Tags 4 and 5

Some disk drives use the spare interface lines for Maintenance functions. Other disk drives use the spare interface lines for Extended Cylinder bits. The 450 utilizes the extra lines as a cylinder address. Configure the disk drive to disable Tags 4 and 5.

3.5 INSTALL AND CABLE THE 450

3.5.1 Install the 450

Place the 450 into the computer card cage; make sure it is firmly seated. Be careful not to dislodge any socketed ICs. Situate the disk drive and connect it to the appropriate power source.

3.5.2 Cable the Subsystem

Install the "A" cable (daisy-chain), observing "pin 1" markings on both ends. This cable connects to the center 60-pin connector on the 450, and to the "A" cable connector on the drive. Use the "in" connector on the drive if there are two 60-pin connectors marked "in" and "out". The other connector should have a terminator, or the terminator should be built into the drive. Disable one of the ports if the drive is dual ported.

Only cable one disk drive for the initial system check. You can connect additional disk drives after this test, if necessary.

3.5.2.1 Connect The "B" Cable (Radial)

Install a "B" cable (26-pin cable) from any "B" cable port on the 450 to the appropriate connector on the disk drive. The 450's "B" cable ports are not keyed to the logical disk drive number (i.e., Drive 0 can connect to Port 2 of the 450). When installing this cable, make sure the black stripe on the shielded cable lines up with the "pin 1" markings on the controller and drive.

3.5.2.2 Mechanical Restraint

Make sure the "A" and "B" cables are mechanically restrained at both ends to prevent them from accidentally disconnecting.

3.5.2.3 Disk Drive Grounds

Install a ground braid wire between the ground terminal on the disk drive(s) and the computer system ground (See Figure 3-7).

3.6 INITIAL TESTS

This section relies upon your familiarity with the computer system's monitor.

3.6.1 Power-up and Self Test

The 450 initiates a self test upon power-up (indicated by an LED). The LED (L1) lights for a moment, and then goes off. If it remains on, the board is not functioning properly. Contact Xylogics for further assistance.

NOTE

Check the power supply voltages to ensure they are within limits (4.75 to 5.25 volts).

3.6.2 Drive Ready

Spin the drive up and wait for it to become ready. Read the Reset Register. This resets the 450, selects Drive 0, and tests the drive ready status. Read the CSR; it should contain 01H or 09H, depending on the 20/24-bit jumper.

If bit 0 is not set, recheck the drive cable connections and try again. If you are still unable to get the proper status, check the -5V supply on the Multibus. If the problem persists, check the disk drive for functionality with an off-line tester.

3.7 DIAGNOSTICS

When you run the diagnostics:

- Format the disk with either a diagnostic or format program.
- Run a full pass of the diagnostics.
- Cable and test any additional drives (See Section 3.8).

The Xylogics 450 XYCAT Diagnostic Manual details the available diagnostics.

3.8 CABLING MULTIPLE DRIVES

If you are using multiple drives, make sure the "A" and "B" cables are properly connected; observe the "pin 1" markings on both the cables and the drives.

3.8.1 Terminator

Remove the terminator from the drive currently connected to the controller. Install the terminator in the last drive in the chain (See Figure 3-7).

3.8.2 "A" Cable (Daisy-chain)

Connect the "A" cable directly from the first drive in the chain to the 450; connect additional drives together, starting with the initial drive (for example, the 450 connects to Drive 0; Drive 0 connects to Drive 1; Drive 1 connects to Drive 2, etc. Be careful; do not reverse the cables) Terminate the "A" cable at the last drive in the chain. The "A" cable's maximum total length is 100 feet (See Figure 3-7).

3.8.3 "B" Cable (Radial)

The "B" cables connect directly from each drive to a "B" cable port on the 450. A "B" cable may be up to 50-feet long (See Section 3.5.2.2).

3.8.4 Unit Select

If you are daisy-chaining drives, assign each drive a unique Unit Select number. The 450 accesses drives with Unit Numbers from 0 through 3.

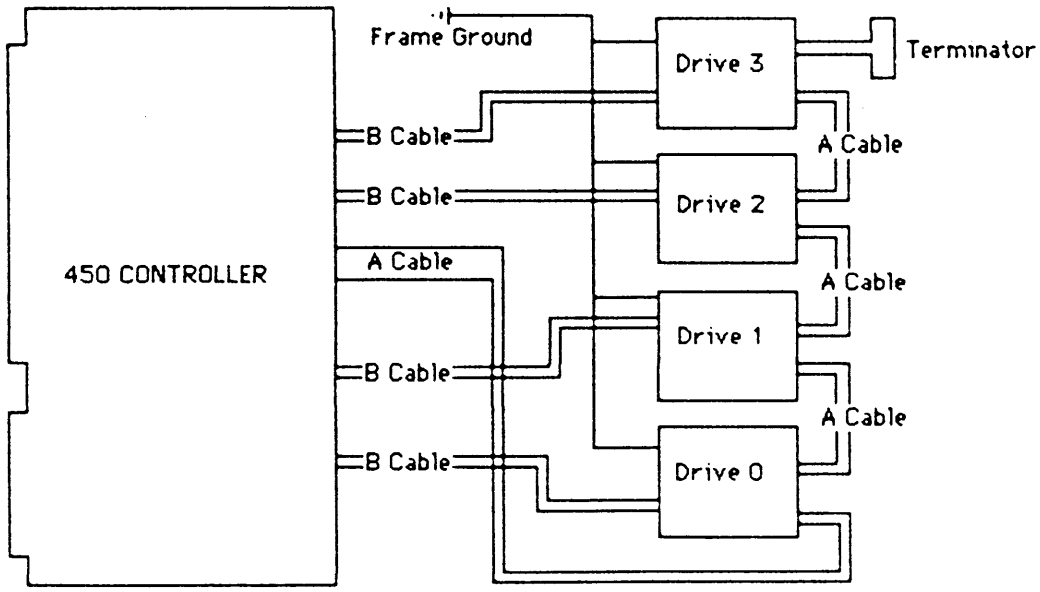


FIGURE 3-7. CABLING MULTIPLE DRIVES

SECTION 4: INSTALLING THE 902-450-9xx SERIES 450

4.0 GENERAL

This section describes how to unpack and configure your 902-450-9xx series 450 controller. The information in Sections 3.1, and 3.3 through 3.8, is pertinent to this series; this section does not repeat this information.

4.1 UNPACKING AND INSPECTION

See Section 3.1 for unpacking and inspection information.

4.2 CONFIGURING THE 450

You can configure the 450 with several jumper options. The following paragraphs describe these options (See Figure 4-2 for a board layout).

4.2.1 Base Address Selection

There are two separate parts to selecting the base address. First, select a response to 8 or 16-bit register addresses. Jumper JC controls this option. Factory setting: 8-bit register; JC installed.

JC: installed = 8-bit address
removed = 16-bit address.

Jumpers JA/JB 1-13 control the actual base address. If you select 8-bit addressing, the jumpers for address bits 0-7 are the only valid jumpers. Ignore the jumpers for bits 8-F. Table 4-1 shows how to set the jumpers for commonly used base addresses.

Use Figure 4-1 and Table 4-1 in configuring the base address to your needs. Inserting or removing a jumper between jumper blocks JA and JB controls I/O address bits 3-F. Installing a jumper asserts a zero on the address comparator for that bit; no jumper asserts a one. Factory setting: 40 (8-bit).

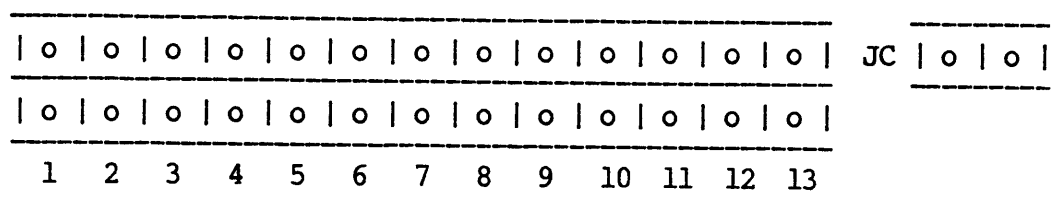


FIGURE 4-1. BASE ADDRESS SELECTION

4.2.1 Base Address Selection (continued)

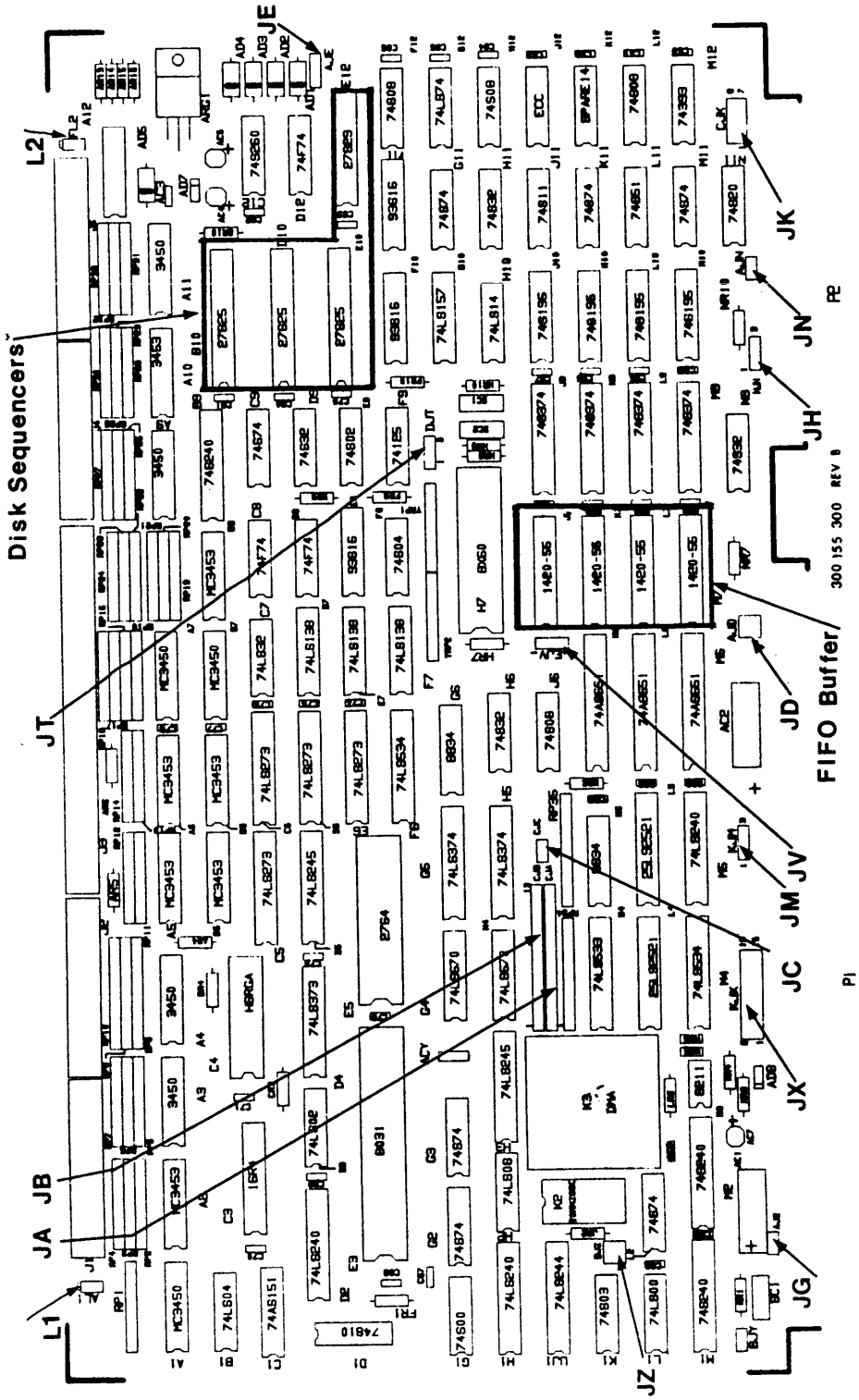


FIGURE 4-2. 450 COMPONENT LOCATION

4.2.1 Base Address Selection (continued)

Address Bits:	F	E	D	C	B	A	9	8	7	6	5	4	3	8/16
Pin Numbers:														
Jumper JA/JB:	1	2	3	4	5	6	7	8	9	10	11	12	13	
Jumper JC:														X
Address:														
40 - 8-bit*	X	X	X	X	X	X	X	X	O	I	O	O	O	I
EE40 - 16-bit	I	I	I	O	I	I	I	O	O	I	O	O	O	O
50 - 8-bit	X	X	X	X	X	X	X	X	O	I	O	I	O	I
0050 - 16-bit	O	O	O	O	O	O	O	O	O	I	O	I	O	O

* Standard Factory Setting

O = Out; I = In; X = Don't Care

TABLE 4-1. BASE ADDRESS SELECTION

4.2.2 20/24-Bit Address Relocation

The 450 functions in backplanes of 16, 20 and 24-bit addresses. Jumpers select the 20-bit or 24-bit Addressing mode. Software selects the 16-bit Addressing mode. System software determines the status of the jumper by reading bit 3 of the CSR. If set, the board is jumpered for 24-bit addressing. Both 20 and 24-bit Addressing modes support 16-bit addressing. Factory setting: 16/20-bit addressing.

Mode	Jumper JM	
16/20	JM 2-3	IN
16/24	JM 1-2	IN

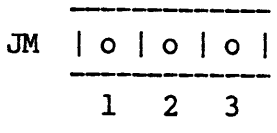


FIGURE 4-3. 20/24-BIT ADDRESS JUMPERS

4.2.3 24-Bit Address Jumpers

The 450 drives the upper address lines (with zero) in the 20-bit Addressing mode. If you require the address lines to float, remove the following jumpers (Factory setting: all jumpers installed):

Address Bit	Jumper Block JK
ADR14H	JK 7-8
ADR15H	JK 5-6
ADR16H	JK 3-4
ADR17H	JK 1-2

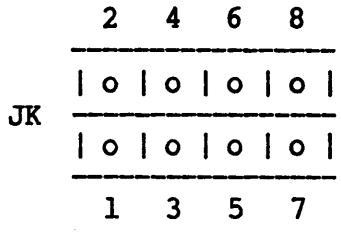


FIGURE 4-4. JUMPER BLOCK JK

4.2.4 Interrupt Request Levels

You can choose any one of eight interrupt request levels. To select an interrupt level, connect a jumper as per Table 4-2. Factory setting: INT5/.

Interrupt Request Level	Jumper Block JX
INT0/	JX 15-16
INT1/	JX 13-14
INT2/	JX 11-12
INT3/	JX 9-10
INT4/	JX 7-8
INT5/	JX 5-6
INT6/	JX 3-4
INT7/	JX 1-2

TABLE 4-2. INTERRUPT REQUEST LEVELS

4.2.4 Interrupt Request Levels (continued)

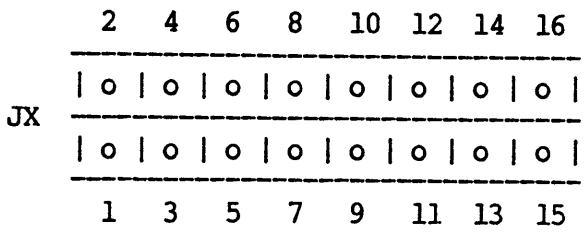


FIGURE 4-5. INTERRUPT LEVEL - JX JUMPER BLOCK

4.2.5 Disable Bus Priority Out

If you are using the 450 in parallel DMA arbitration (See Section 3.3.2.2), isolate the Bus Priority Out (BPRO/) signal from the Multibus by removing jumper JY. Factory setting: serial arbitration; JY installed.

4.2.6 Power-fail Protection

Certain Multibus systems allow AC power-fail protection. Install jumper JH 1-2, and provide an appropriate power-fail signal on pin 18 of the Multibus P2 connector. This signal should go to ground when the AC power source fails. Using an AC (versus DC) power-fail indicator allows the 450 more time to protect the drive from accidental spiral writes. The 450 has on-board DC power loss detection circuitry. The 450 is normally jumpered for DC power-down protection. Factory setting: jumper JH 2-3 in.

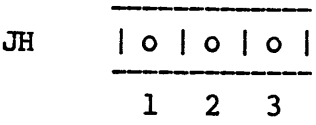


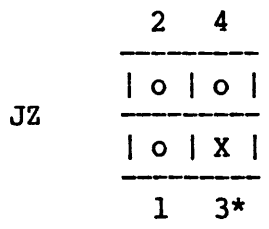
FIGURE 4-6. POWER-DOWN PROTECTION - JUMPER BLOCK JH

4.2.7 Common Bus Request

All potential bus masters drive the Common Bus Request (CBRQ/) Multibus signal. CBRQ/ informs the current bus master that another bus master wishes to use the bus. If no other master requests the bus when the current master completes its transfer, the master retains bus mastership without any bus exchange overhead. Factory setting: CBRQ/ disabled.

4.2.7 Common Bus Request (continued)

CBRQ/ Disabled	CBRQ/ Enabled
JZ 2-4 In	JZ 1-2 In



* Pin JZ 3 is not used.

FIGURE 4-7. COMMON BUS REQUEST - JUMPER BLOCK JZ

4.2.8 Remote Activity Indicator

An on-board LED (L1) indicates when the controller is busy. A remote activity indicator signal is available on the backplane; install jumper JN and wire the remote LED between +5 volts and pin 42 of the P2 connector. Factory setting: JN out.

4.2.9 -5 VDC Regulator Option

The 450 uses -5 volts to power the differential drivers/receivers for the SMD interface. This helps keep heat-producing components off the controller board, and allows you to put them in a more appropriate location.

You can also configure the 450 to utilize an on-board -5 VDC regulator which derives this voltage from the -12 VDC provided in most Multibus systems. Table 4-3 and Figure 4-8 detail the regulator option. Factory setting: -5 VDC; available from the backplane.

4.2.9 -5 VDC Regulator Option (continued)

-5 VDC Regulator	-5 VDC Available From Backplane
Jumper JD 1-2 In JD 3-4 In	Jumper JD 1-2 Out JD 3-4 Out
Jumper JE 1-2 In	Jumper JE 2-3 In
Jumper JG 1-2 Out	Jumper JG 1-2 In

TABLE 4-3. -5 VDC OPTION JUMPERS

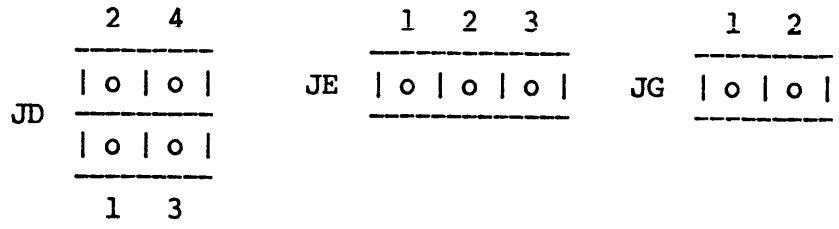


FIGURE 4-8. -5 VDC OPTION JUMPER BLOCKS

4.2.10 Factory Use Only

The 450 has two FIFO buffer options: 2 KB or 8 KB. You must order the correct FIFO size for your application since the parts are soldered in. Each buffer size requires jumpers which the factory sets.

2 KB Option	8 KB Option
JT 2-3 In	JT 1-2 In
JV 2-3 In	JV 1-2 In

TABLE 4-4. 2 KB / 8 KB JUMPERS

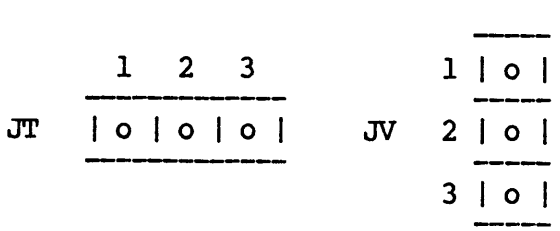
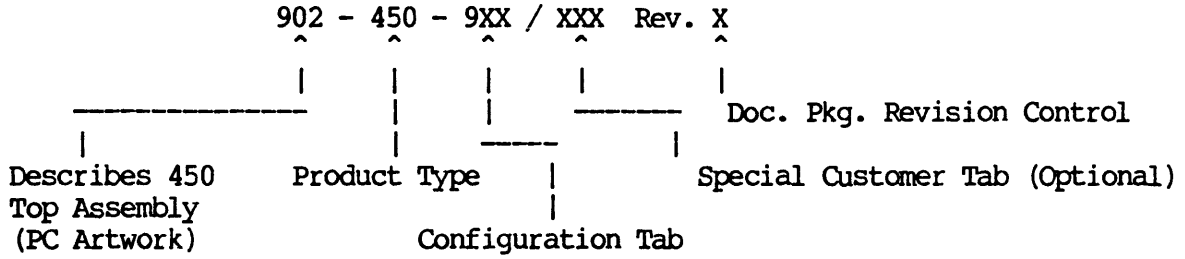


FIGURE 4-9. FIFO BUFFER JUMPER BLOCKS

4.2.11 Firmware and Sector Size

The disk sequencer PROMS contain parameters which control the sector size, buffer size, and format type. Use the following information to ensure your 450 was properly configured at the factory.

The following part numbers describe the product version, type, and configuration. These documentation package numbers (DPNs) are used throughout the ordering and manufacturing process. The DPN appears on the non-component side of every controller.



PROMS FOR VARIOUS CONFIGURATIONS

Order Number	Part Number 180-002-xxx Loc. D10 - Loc. E12		Bytes/Sector	Buffer Size	Format Compatibility
902-450-900	068	044	512	2 KB	440
902-450-901	045	044	512	8 KB	440
902-450-902	051	050	256	2 KB	440
902-450-903	052	050	256	8 KB	440
902-450-904	043	040	512	2 KB	450
902-450-905	038	040	512	8 KB	450
902-450-906	058	056	256	2 KB	450
902-450-907	057	056	256	8 KB	450
902-450-908	047	046	1024	2 KB	450
902-450-909	053	046	1024	8 KB	450
902-450-910	068	044	512	2 KB	450
902-450-911	055	054	2048	8 KB	450
902-450-912	049	048	1056	2 KB	450

TABLE 4-5. SECTOR / BUFFER SIZE CONFIGURATIONS

4.2.11 Firmware and Sector Size (continued)

Order Number	Part Number 180-002-xxx Loc. D10 - Loc. E12		Bytes/Sector	Buffer Size	Format Compatibility
902-400-913	038	040	512	8 KB	450
902-450-914	049	048	1056	2 KB	450
902-450-915	061	059	768	8 KB	450
902-450-916	064	063	528	2 KB	450

TABLE 4-5. SECTOR / BUFFER SIZE CONFIGURATIONS (continued)

PROMS / PALS NOT MODIFIED

Description	Location	Part Number
EPROM	E5	180-002-041 (Standard)
"	E5	180-002-065 (Tab 910)
"	E5	180-002-066 (Tab 913)
"	E5	180-002-067 (Tab 912)
PAL	C3	180-001-009
Disk Sequencer	B10	180-002-037
Disk Sequencer	E10	180-002-039

TABLE 4-6. PROM / PAL PART NUMBERS AND LOCATIONS

4.3 DISK DRIVE PREPARATION

This section describes special disk drive sector switch settings.

4.3.1 Sector Switch Setting For Fujitsu Eagle

Switches on one of the drive's internal circuit cards usually select the number of sectors per track. Table 4-7 indicates the special sector switch setting for the Fujitsu Eagle (M2351).

Fujitsu M2351 Setting (Forty-seven 512-Byte Data Sectors) (Jumper Installed):

BC7: 3-4, 5-6, 10-11, 13-14
BD7: 2-3, 6-7, 9-10, 13-14
BE7: 3-4, 5-6, 10-11, 13-14
BF7: 3-4, 6-7, 10-11, Spare

TABLE 4-7. SECTOR SWITCH SETTING FOR FUJITSU EAGLE

SECTION 5: MAINTENANCE AIDS

5.0 GENERAL

The following section provides useful information for installing and maintaining your Xylogics Model 450 Disk Controller.

5.1 MULTIBUS INTERFACE SIGNALS

Mnemonic	Conn.	Pin	Used By 450	Description
ADR0/	P1	57	Y	
ADR1/	P1	58	Y	
ADR2/	P1	55	Y	
ADR3/	P1	56	Y	
ADR4/	P1	53	Y	
ADR5/	P1	54	Y	
ADR6/	P1	51	Y	
ADR7/	P1	52	Y	
ADR8/	P1	49	Y	
ADR9/	P1	50	Y	
ADRA/	P1	47	Y	
ADRB/	P1	48	Y	
ADRC/	P1	45	Y	
ADRD/	P1	46	Y	Address Bus
ADRE/	P1	43	Y	
ADRF/	P1	44	Y	
ADR10/	P1	28	Y	
ADR11/	P1	30	Y	
ADR12/	P1	32	Y	
ADR13/	P1	34	Y	
ADR14/	P2	57	P	
ADR15/	P2	58	P	
ADR16/	P2	55	P	
ADR17/	P2	56	P	
DAT0/	P1	73	Y	
DAT1/	P1	74	Y	
DAT2/	P1	71	Y	
DAT3/	P1	72	Y	
DAT4/	P1	69	Y	
DAT5/	P1	70	Y	
DAT6/	P1	67	Y	
DAT7/	P1	68	Y	
DAT8/	P1	65	Y	Data Bus
DAT9/	P1	66	Y	
DATA/	P1	63	Y	
DATB/	P1	64	Y	
DATC/	P1	61	Y	
DATD/	P1	62	Y	
DATE/	P1	59	Y	
DATF/	P1	60	Y	

5.1 MULTIBUS INTERFACE SIGNALS (continued)

Mnemonic	Conn.	Pin	Used By 450	Description
STROBE				
IORC/	P1	21	Y	I/O Read Command
IOWC/	P1	22	Y	I/O Write Command
MRDC/	P1	19	Y	Memory Read Command
MWTC/	P1	20	Y	Memory Write Command
XACK/	P1	23	Y	XFER Acknowledge
INTERRUPTS				
INT0/	P1	41	P	
INT1/	P1	42	P	
INT2/	P1	39	P	
INT3/	P1	40	P	
INT4/	P1	37	P	Interrupt Request Levels
INT5/	P1	38	P	
INT6/	P1	35	P	
INT7/	P1	36	P	
[illegible]	P1	33	N	Interrupt Acknowledge
DMA				
BPRN/	P1	15	Y	Bus Priority In
BPRO/	P1	16	Y	Bus Priority Out
BREQ/	P1	18	P	Bus Request
BUSY/	P1	17	Y	Bus Busy
CBRQ/	P1	29	N	Common Bus Request
MISCELLANEOUS CONTROL				
BHEN/	P1	27	Y	Byte High Enable
BD RESET/	P2	36	N	Board Reset
HALT/	P2	28	N	Bus Master Wait State
INH1/	P1	24	N	Inhibit 1; Disable RAM
INIT/	P1	14	Y	Initialize
MISCELLANEOUS				
ACLO/	P2	18	P	AC Low
ALE/	P2	32	N	Bus Master ALE
AUX RESET/	P2	38	N	Reset Switch Reserved
LOCK/	P1	25	N	Inhibit 2; Disable PROM or ROM
MPRO/	P2	20	N	Memory-protect
PAR1/	P2	27	N	Parity 1
PAR2/	P2	29	N	Parity 2
WAIT/	P2	30	N	Bus Master Wait State

5.1 MULTIBUS INTERFACE SIGNALS (continued)

Mnemonic	Conn.	Pin	Used By 450	Description
CLOCKS				
BCLK/	P1	13	P	Bus Clock
CCLK/	P1	31	N	Constant Clock
PLC/	P2	31	N	Power Line Clock
POWER				
12VB	P2	11,12	N	+12 VDC Battery
5VB	P2	3	N	+5 VDC Battery
GVB	P2	4	N	Return
-5VB	P2	7,8	N	-5 VDC Battery
-12VB	P2	15,16	N	-12 VDC Battery
+5V	P1	3,4,5,6,81,82,83,84	Y	+5 VDC
+12V	P1	7,8	N	+12 VDC
+15V	P2	23,24	N	+15 VDC
-5V	P1	9,10	P	-5 VDC Supply
-12V	P1	79,80	P	-12 VDC
-15V	P2	25,26	N	-15 VDC
EEVPP	P2	6	N	E^2 PROM Power
GND	P1	1,2,11,12,75,76,85,86	Y	Signal GND
GND	P2	1,2,21,22	N	Signal GND

Y = Yes; N = No; P = Possibly (Jumper or Optionally Available)

5.2 STORAGE MODULE DRIVE INTERFACE

The SMD interface is compatible with several pin-numbering systems. This section lists both CDC's method, and the industry standard (STND). Xylogics follows the industry standard for pin-numbering.

NAME	CABLE	PIN +/- CDC	PIN +/- STND	DESCRIPTION
UNIT SELECT				
Unit Select Tag	A	52/22	44/43	Initiates a Unit Select sequence along with the Unit Select bits.
Unit Sel. Bit 0	A	53/23	46/45	These binary weighted signals determine which drive (out of sixteen) the 450 selects.
Unit Sel. Bit 1	A	54/24	48/47	
Unit Sel. Bit 2	A	56/26	52/51	
Unit Sel. Bit 3	A	57/27	54/53	
Open Cable Det.	A	44/14	28/27	The controller uses this signal to deselect the drive in the event of power failure.

5.2 STORAGE MODULE DRIVE INTERFACE (continued)

NAME	CABLE	PIN+/- CDC	PIN+/- STND	DESCRIPTION
Unit Selected	B	09/22	17/18	A "B" cable signal; indicates the drive has been selected.
Unit Ready	A	49/19	38/37	The selected drive is up to speed; the heads are loaded, and not faulted.
CONTROL				
Tag 1	A	31/01	02/01	Cylinder Select Tag; the drive seeks to the cylinder selected by Bus bits 0-10.
Tag 2	A	32/02	04/03	Head Select Tag; the drive selects the head specified by Bus bits 0-9.
Tag 3	A	33/03	06/05	Control Tag; the drive executes the function defined by Bus bits 0-9.
Pwr. Seq. Hold	A	59	58	Used for power-sequencing with Remote/Local; always enabled on the 450.
Sequence Pick In	A	29	57	Used for power-sequencing with Remote/Local; always enabled on the 450.
Bus Bit 0	A	34/04	08/07	Write Gate Enable or bit 0 of head or cylinder.
Bus Bit 1	A	35/05	10/09	Read Gate Enable or bit 1 of head or cylinder.
Bus Bit 2 *	A	36/06	12/11	Servo Offset (+) or bit 2 of head or cylinder.
Bus Bit 3 *	A	37/07	14/13	Servo Offset (-) or bit 3 of head or cylinder.
Bus Bit 4	A	38/08	16/15	Fault Clear or bit 4 of head or cylinder.
Bus Bit 5	A	39/09	18/17	Address Mark Enable or bit 5 of head or cylinder.
Bus Bit 6	A	40/10	20/19	Recalibrate or bit 6 of head or cylinder.

* Not Implemented On The 450

5.2 STORAGE MODULE DRIVE INTERFACE (continued)

NAME	CABLE	PIN+/- CDC	PIN+/- STND	DESCRIPTION
Bus Bit 7 *	A	41/11	22/21	Data Strobe Early or bit 7 of head or cylinder.
Bus Bit 8 *	A	42/12	24/23	Data Strobe Late or bit 8 of head or cylinder.
Bus Bit 9	A	43/13	26/25	Release or bit 9 of head or cylinder.
Bus Bit 10	A	60/30	60/59	Bit 10 of cylinder address.
CLOCKS and DATA				
Index	A	48/18	36/35	Pulses for every index mark.
Read Clock	B	17/05	08/09	Synchronizes read data.
Read Data	B	16/03	06/05	Reads data from drive.
Sector	A	55/25	50/49	Pulses for every sector (except during index).
Servo Clock	B	14/02	02/03	Synchronizes write data.
Write Clock	B	19/06	12/11	Clock sent to drive with synchronized write data.
Write Data	B	20/08	14/15	Write data sent to drive.
STATUS				
Address Mark *	A	50/20	39/40	The drive encountered a sector mark.
Busy	A	51/21	42/41	One port is busy in a dual port drive.
Fault	A	45/15	30/29	The drive is faulted.
On-cylinder	A	47/17	34/33	The drive is on-cylinder.
Seek End	B	23/10	20/19	The drive completed a seek, or loaded the heads.
Seek Error	A	46/16	32/31	The drive has a seek error.
Write-protect	A	58/28	56/55	The drive is write-protected.

* Not Implemented On The 450

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