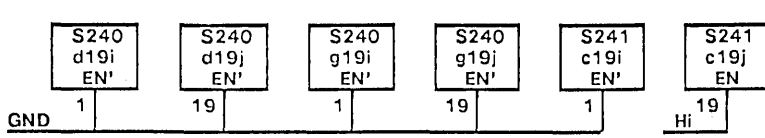
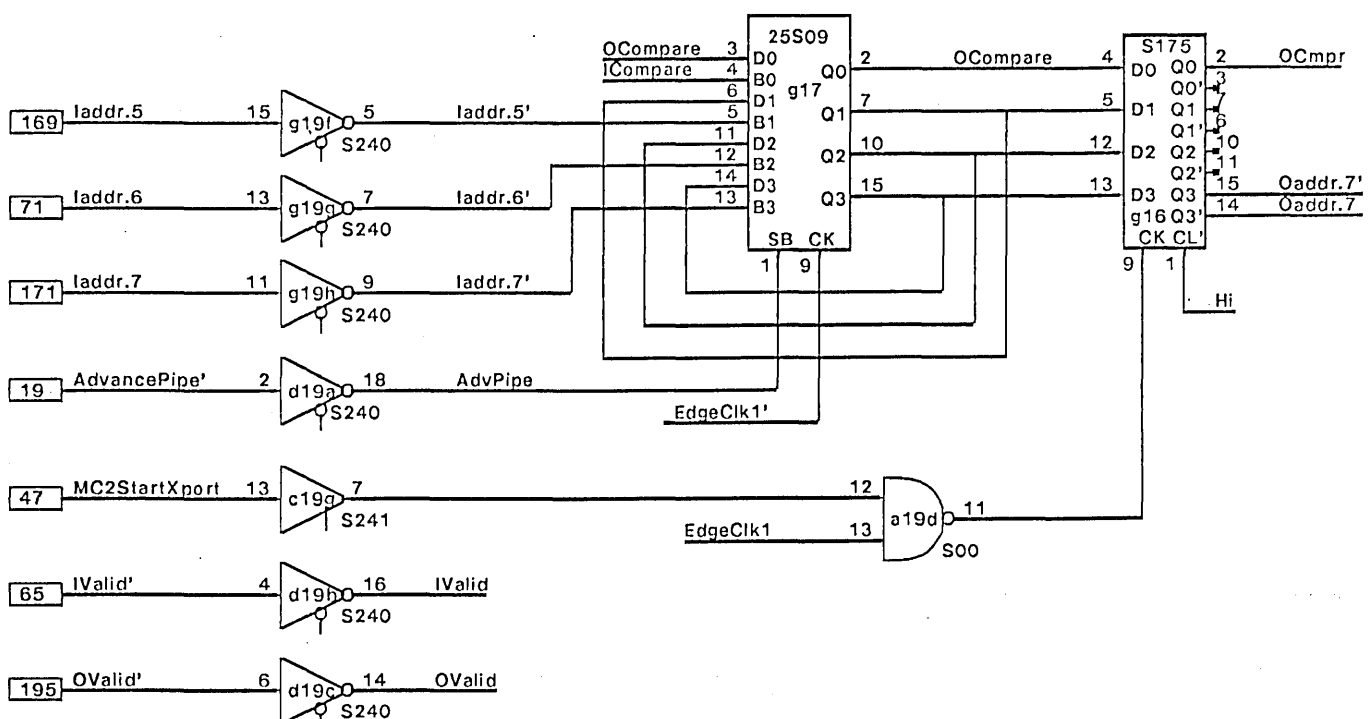
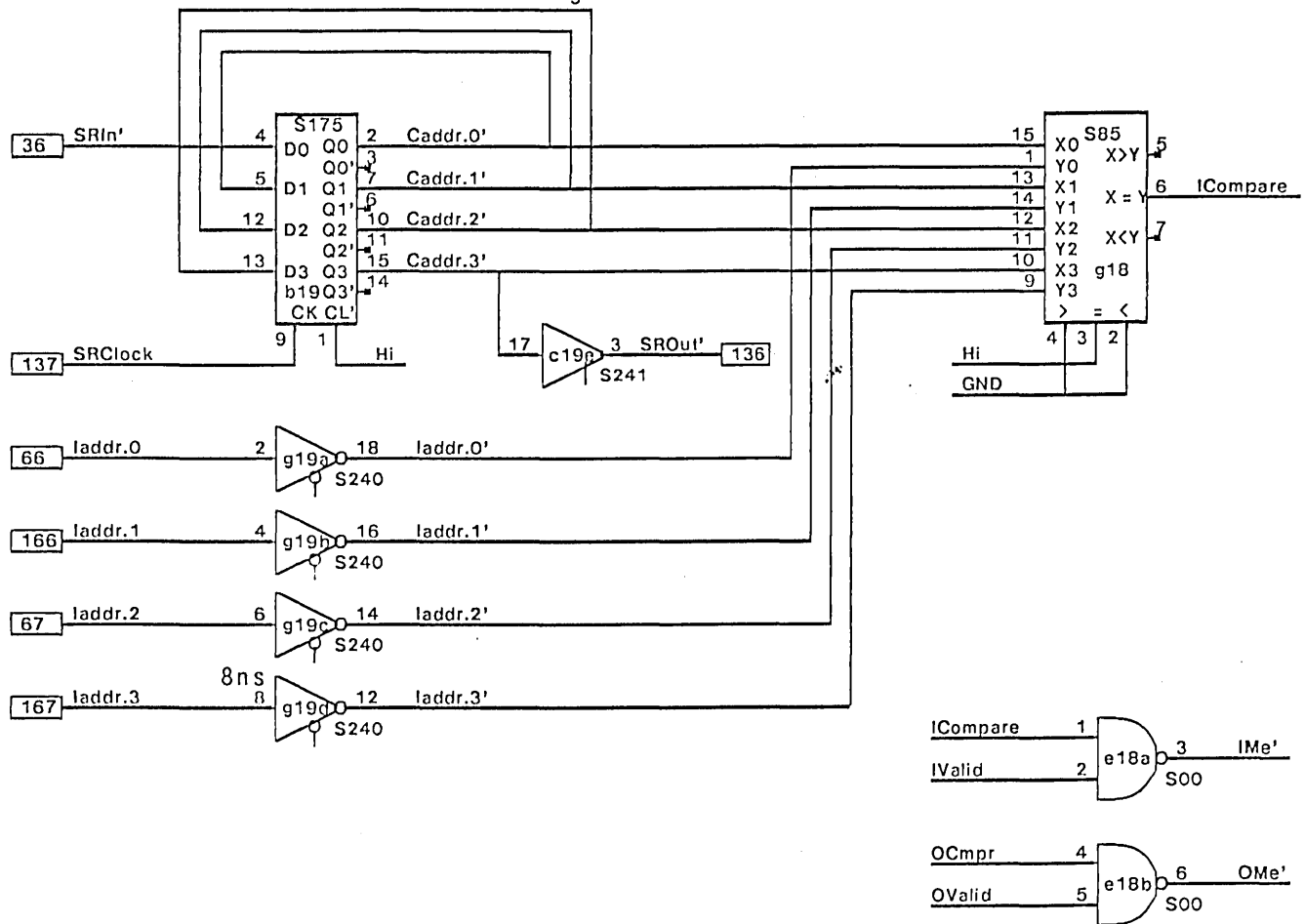
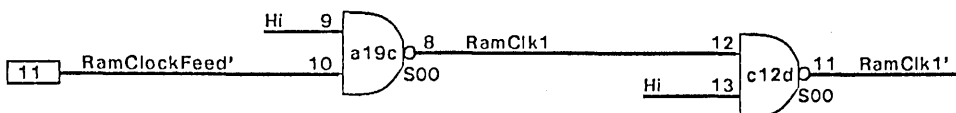
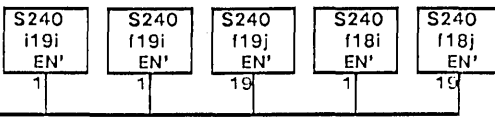
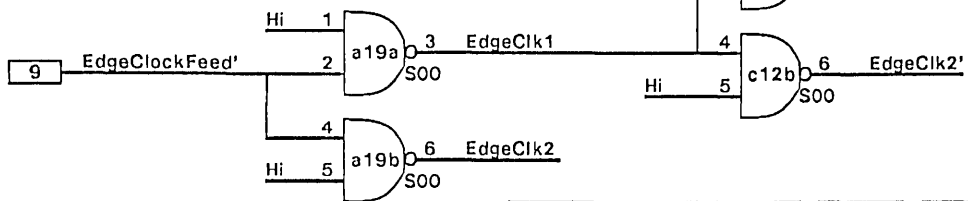
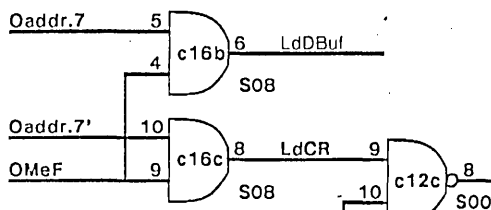
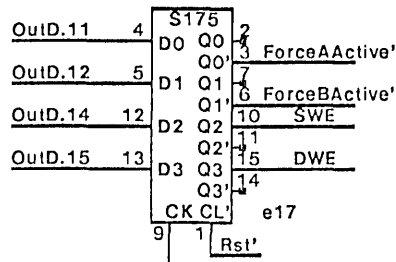
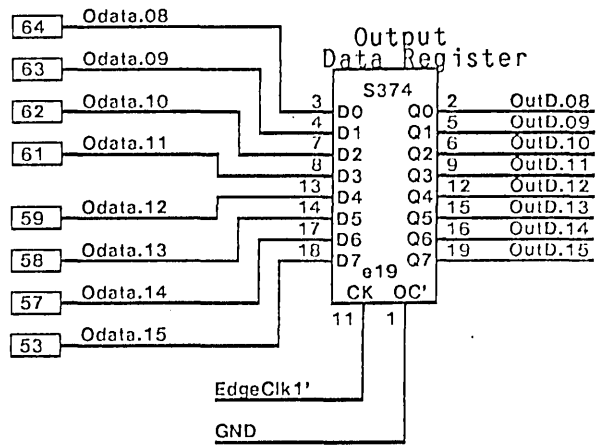
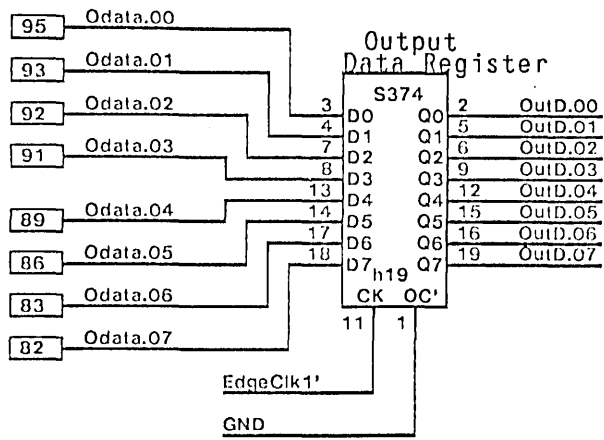
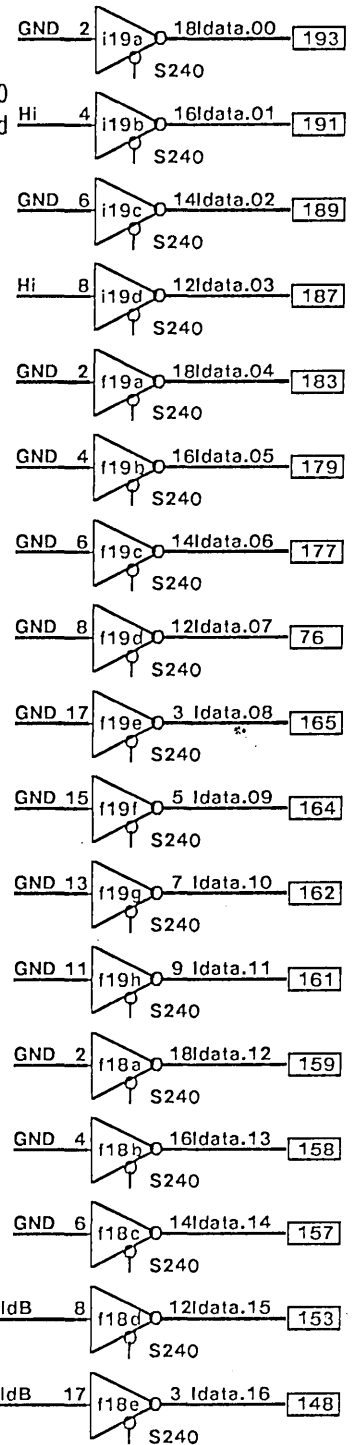


Controller Addressing

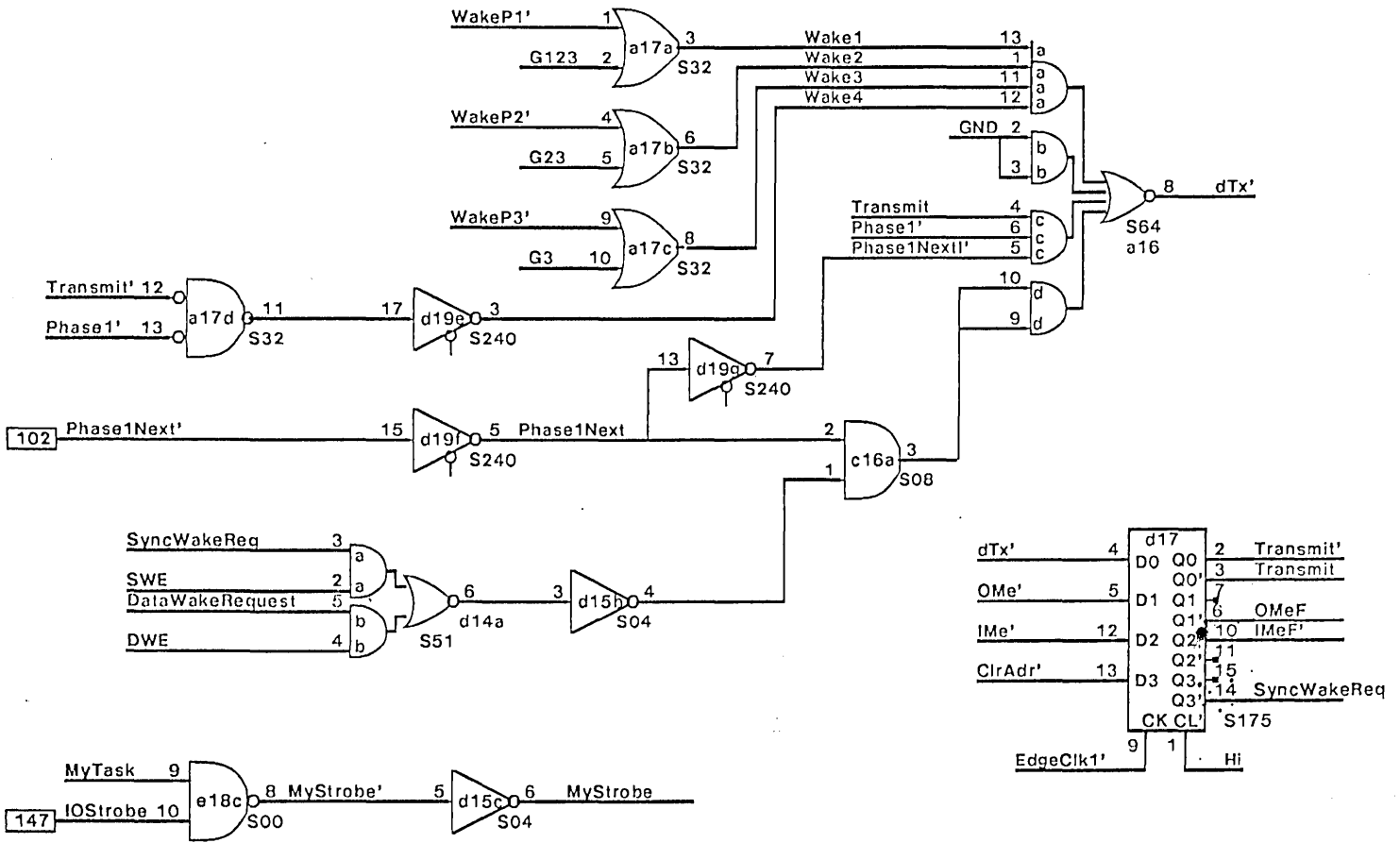
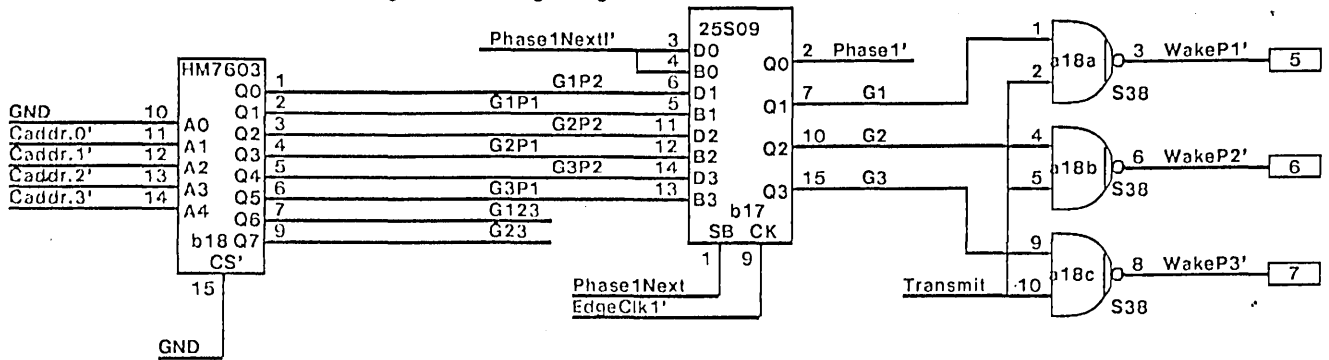




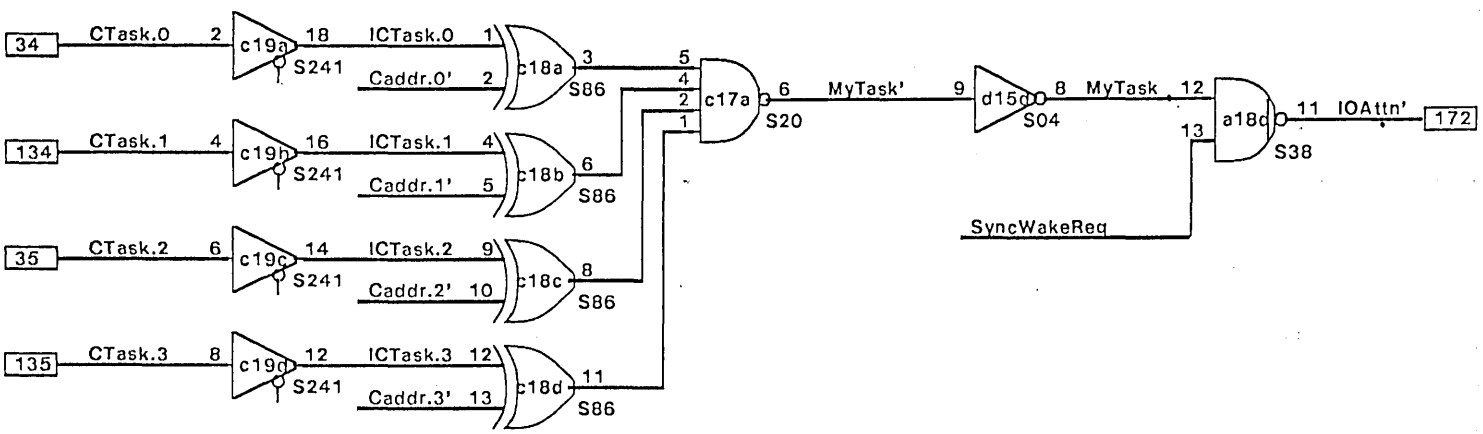
Returns 127..0  
as the ID word

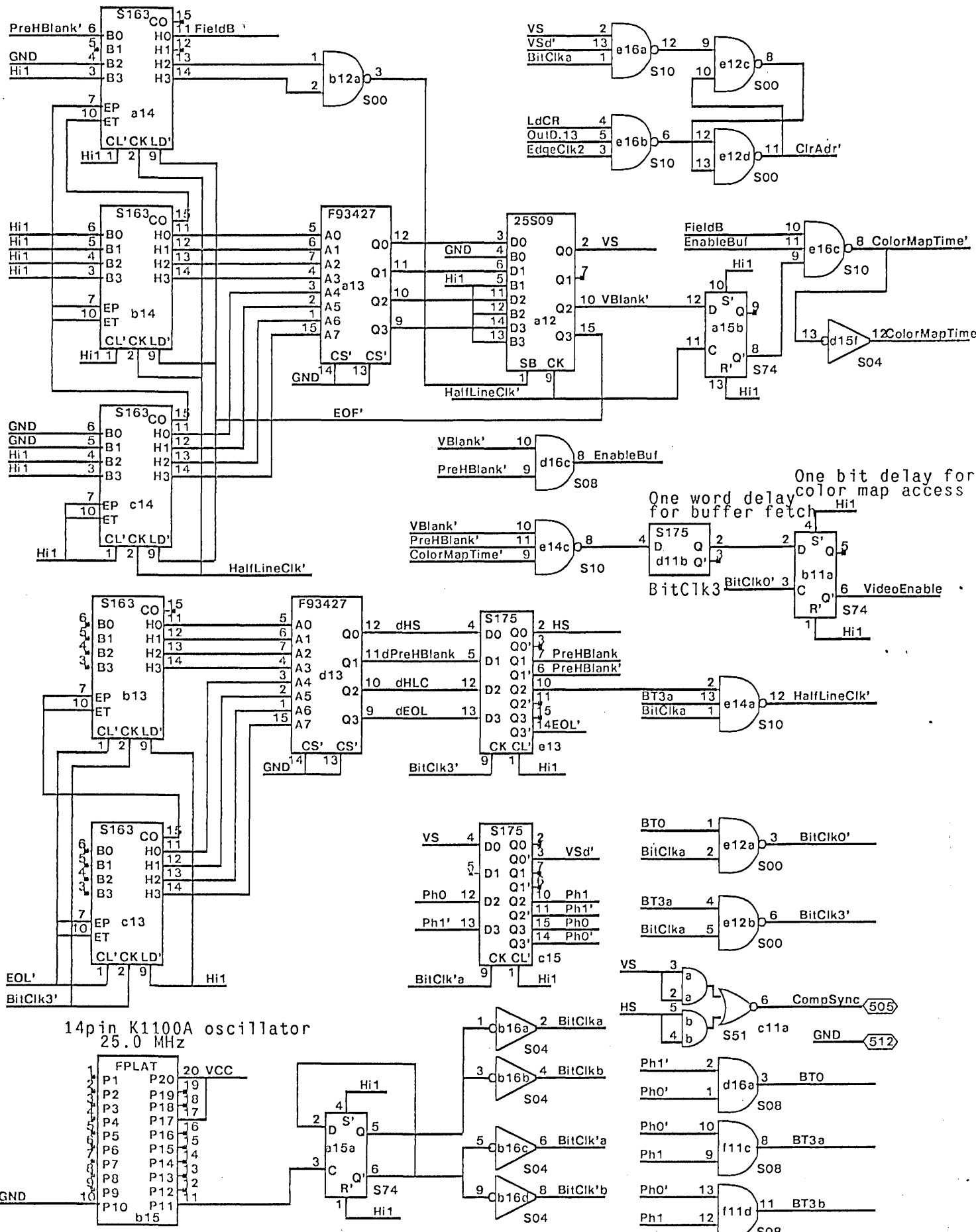


### WakeUp Priority Encoding Logic



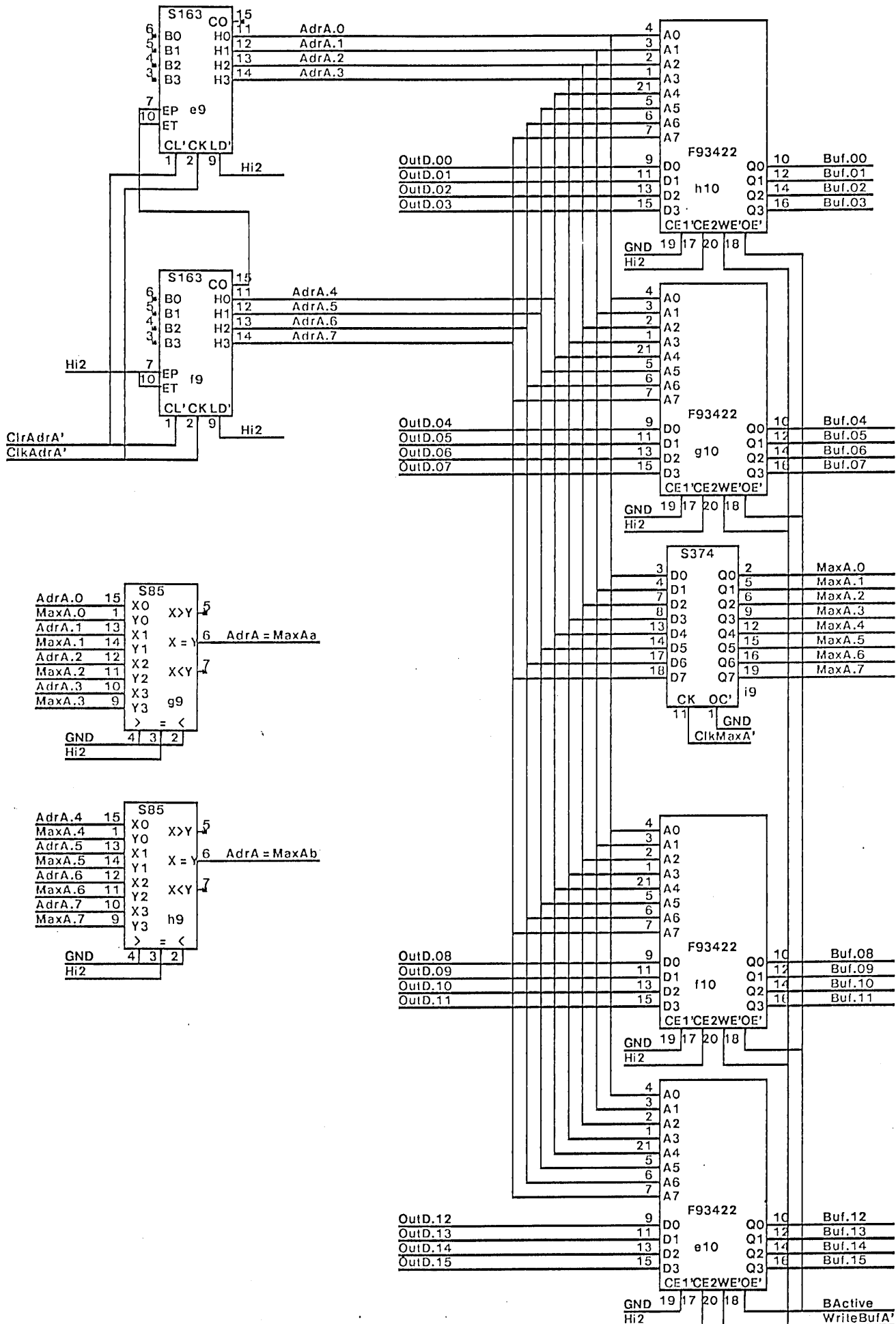
### Current Task Comparator (XOR) IO Attention Logic

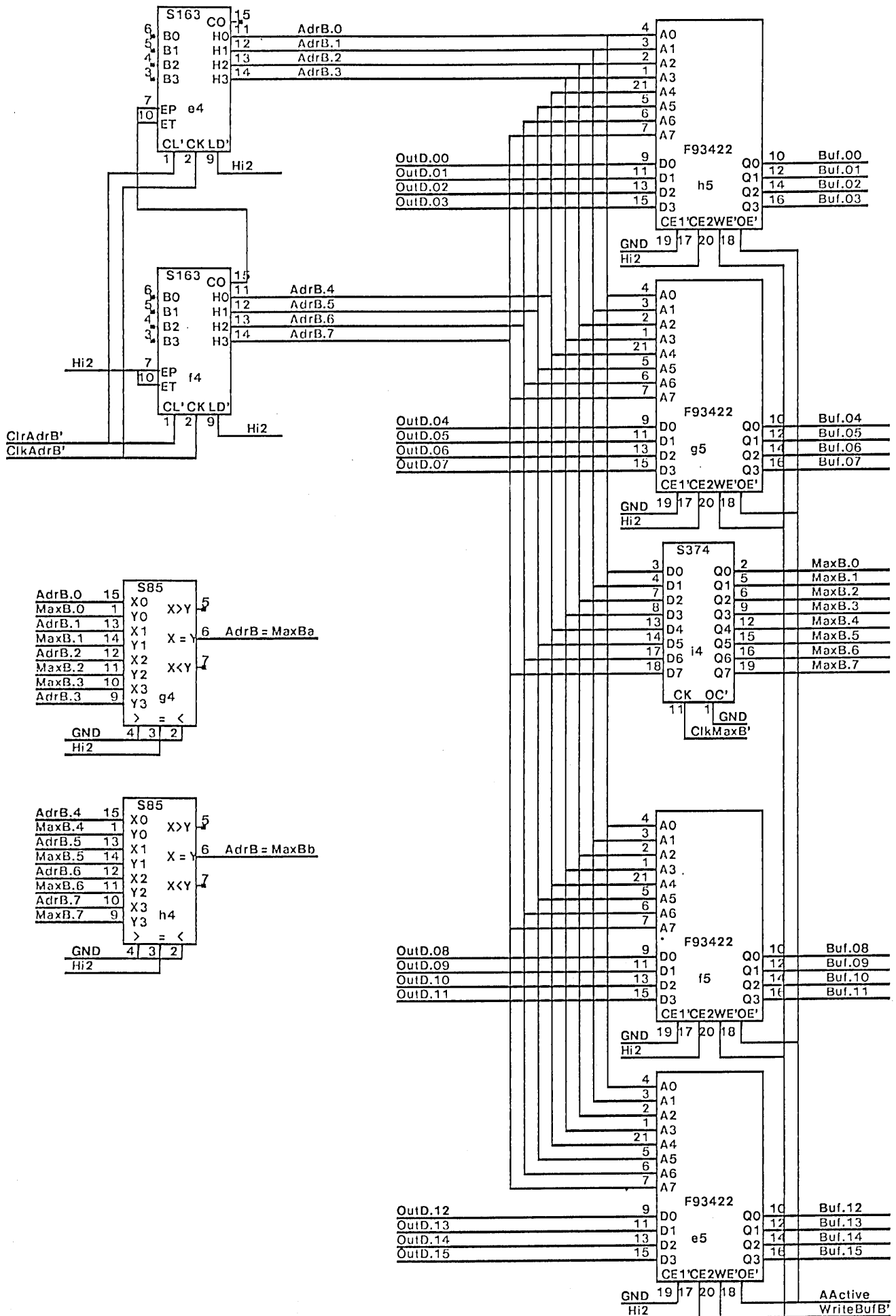


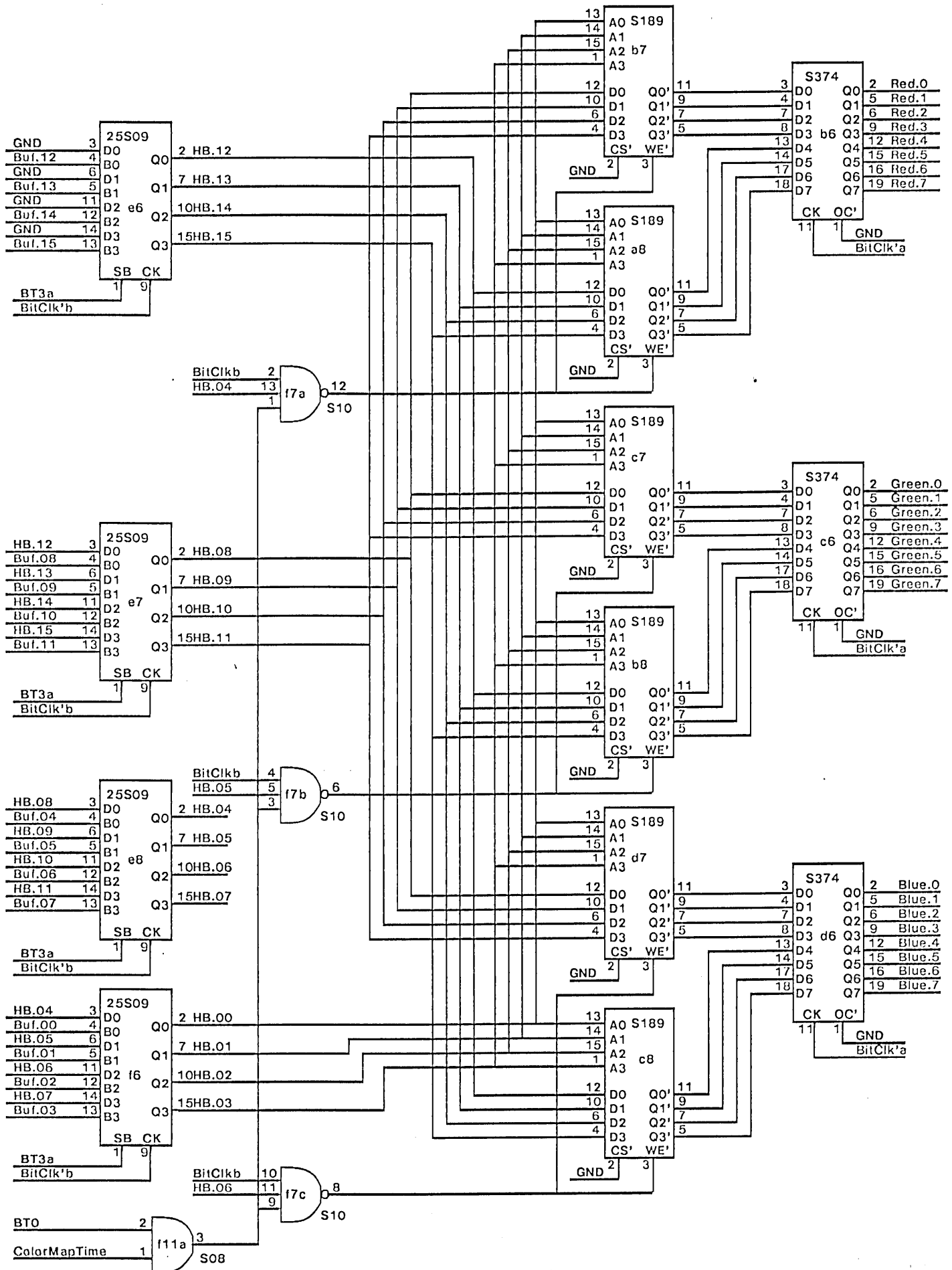


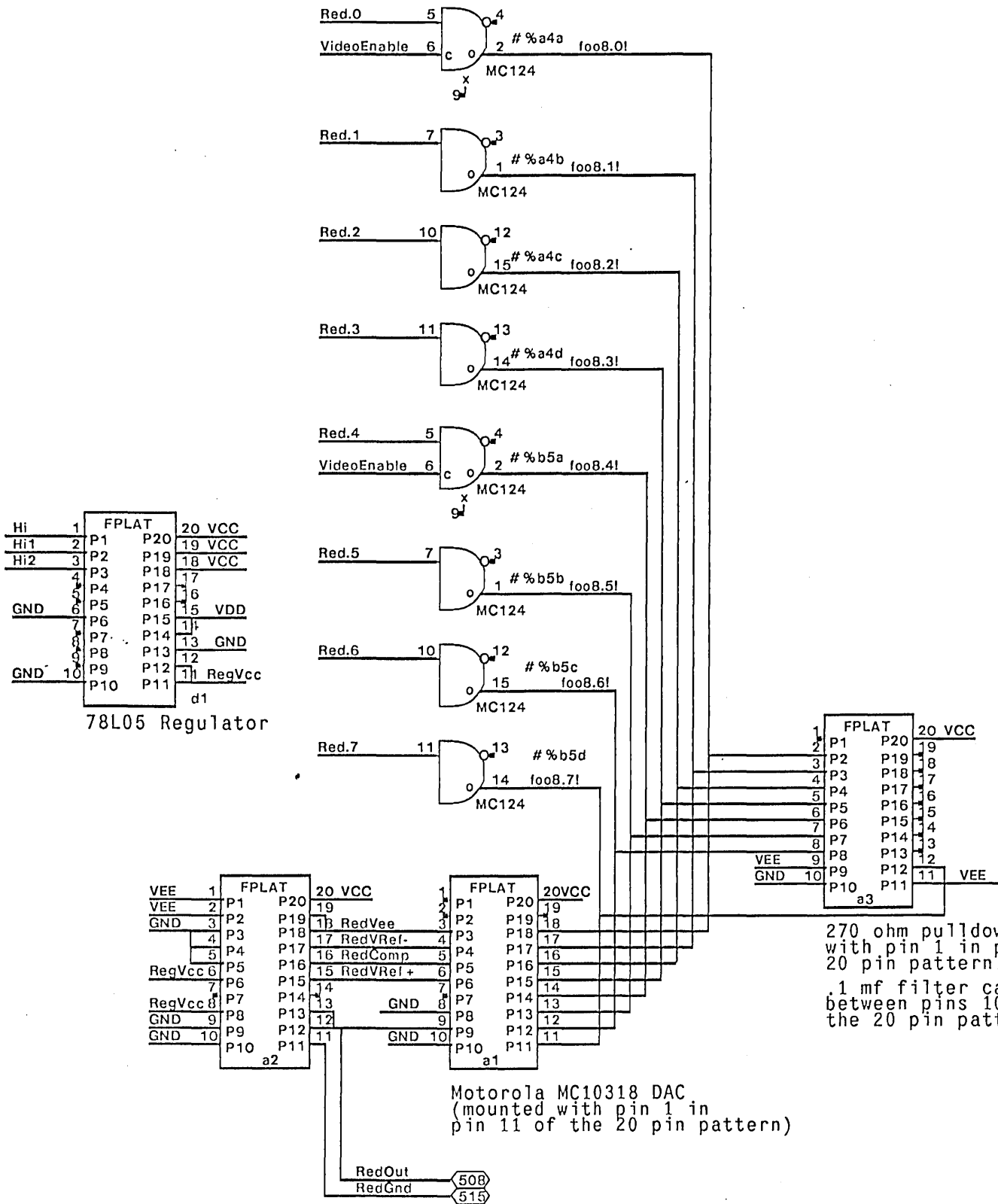
One bit delay for color map access  
 One word delay for buffer fetch

14pin K1100A oscillator  
 25.0 MHz

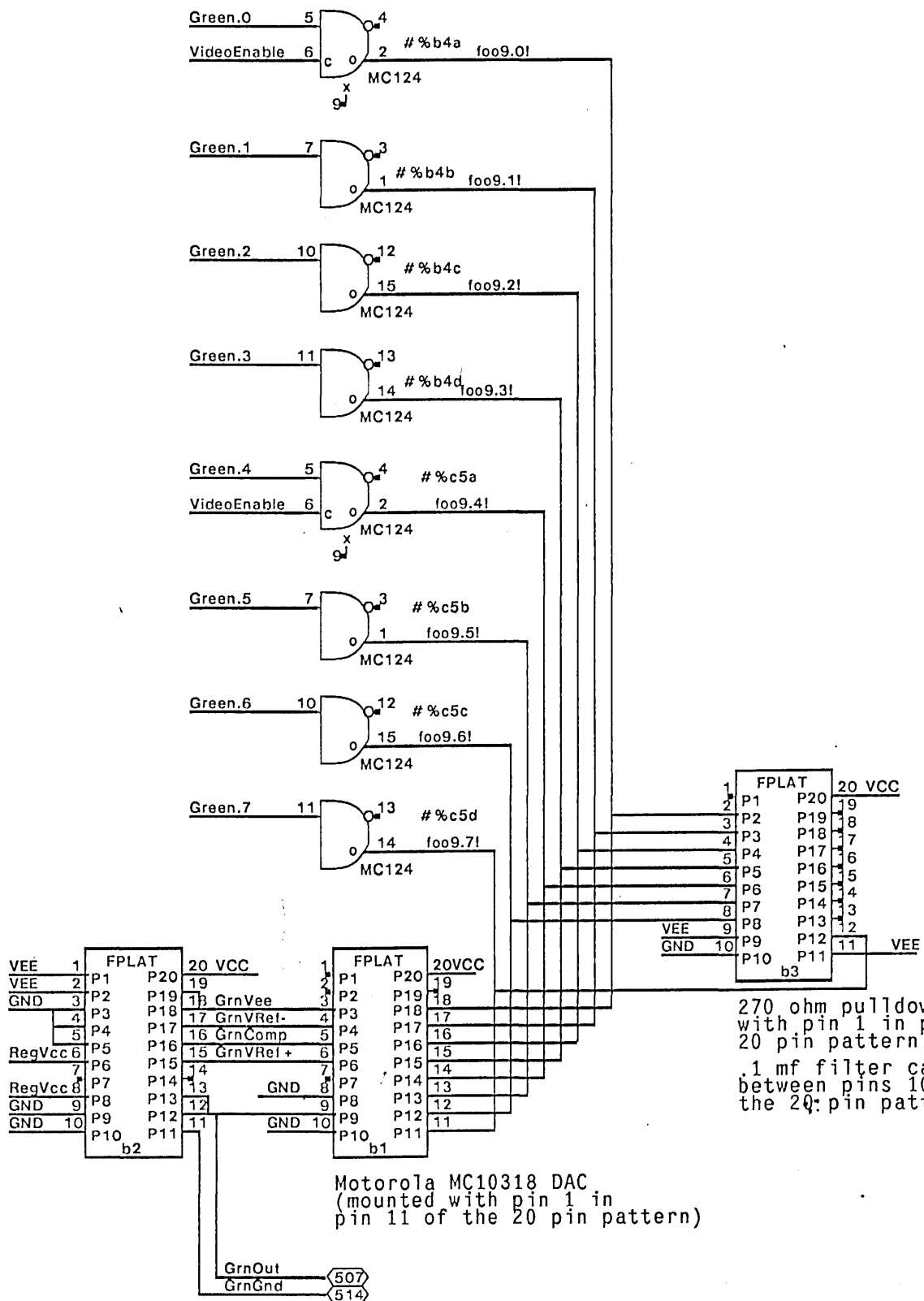


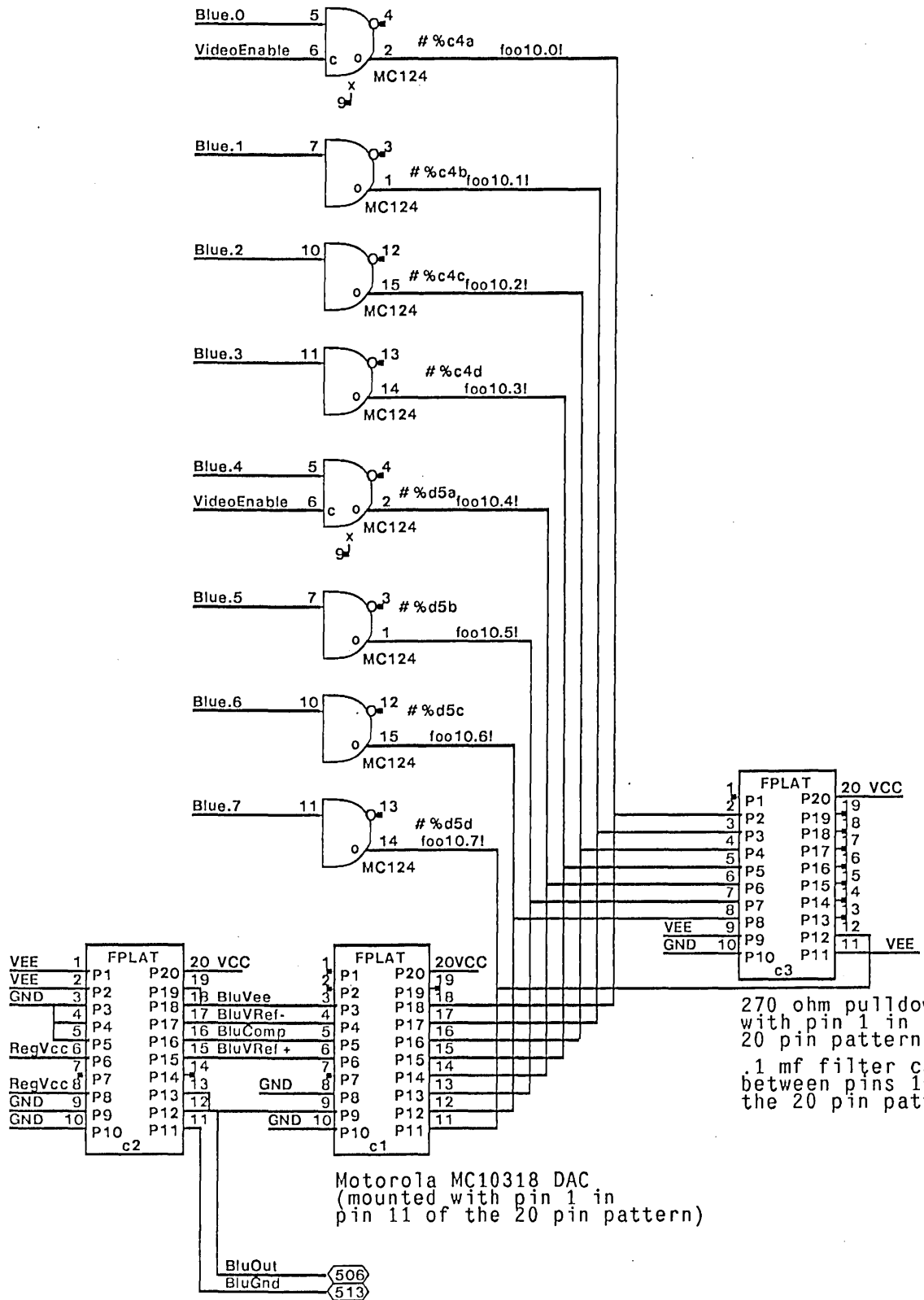






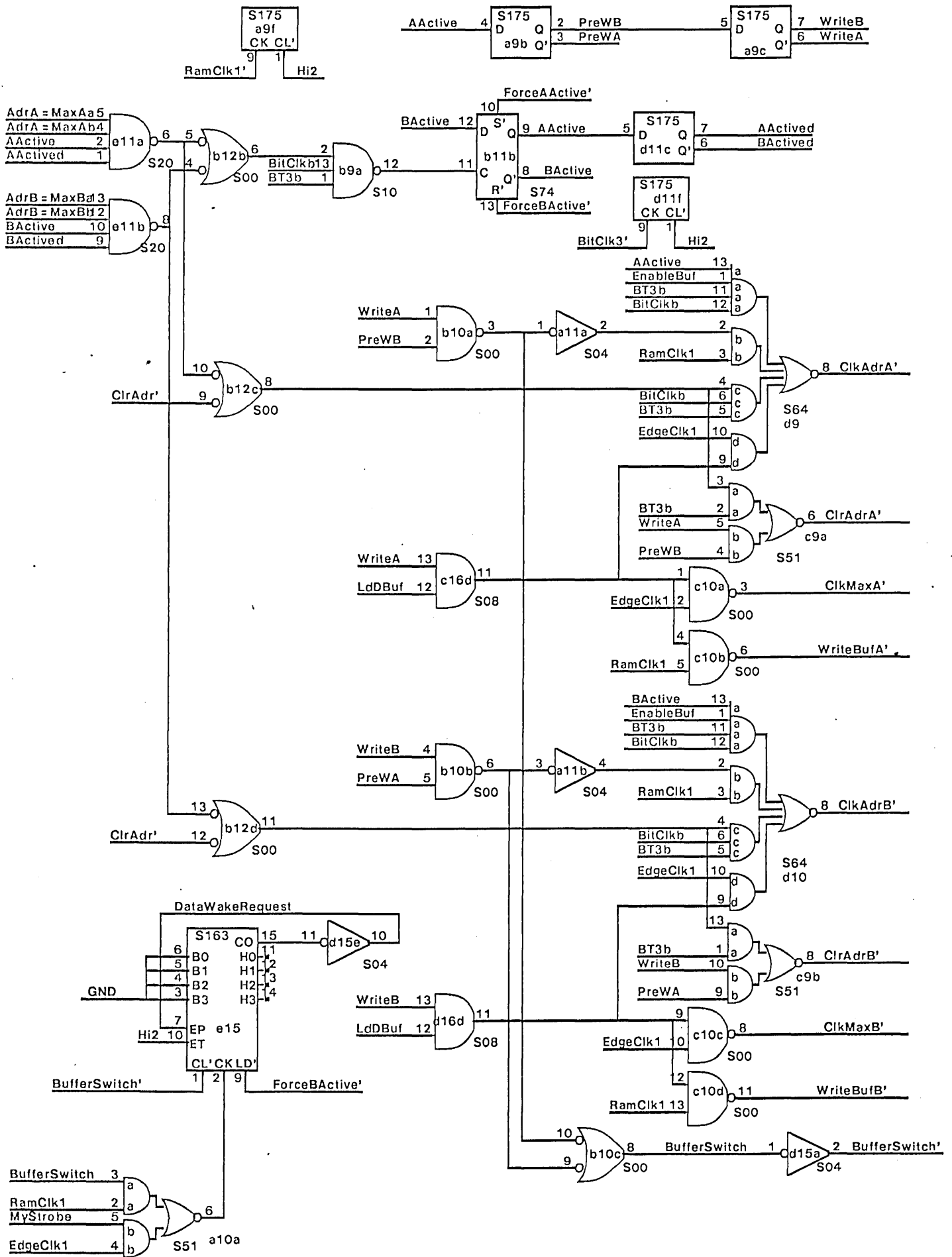






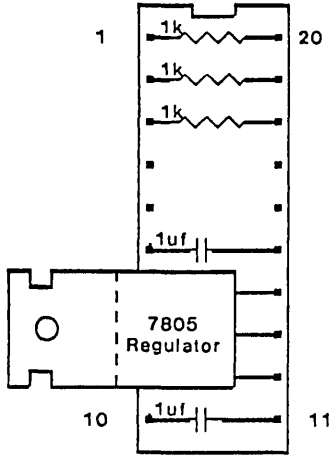
270 ohm pulldowns, mow  
with pin 1 in pin 12 of  
20 pin pattern.

.1 mf filter cap. mount  
between pins 10 and 11  
the 20 pin pattern.

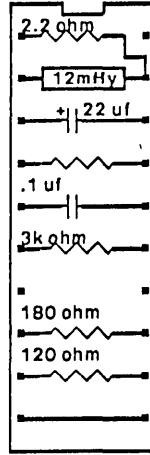


XEROX CSL	Project D0	Sync Generator	File CDC04.sil	Designer Thacker	Rev Ga	Date 9/8/79	Page 01
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Platform d1  
1 required.

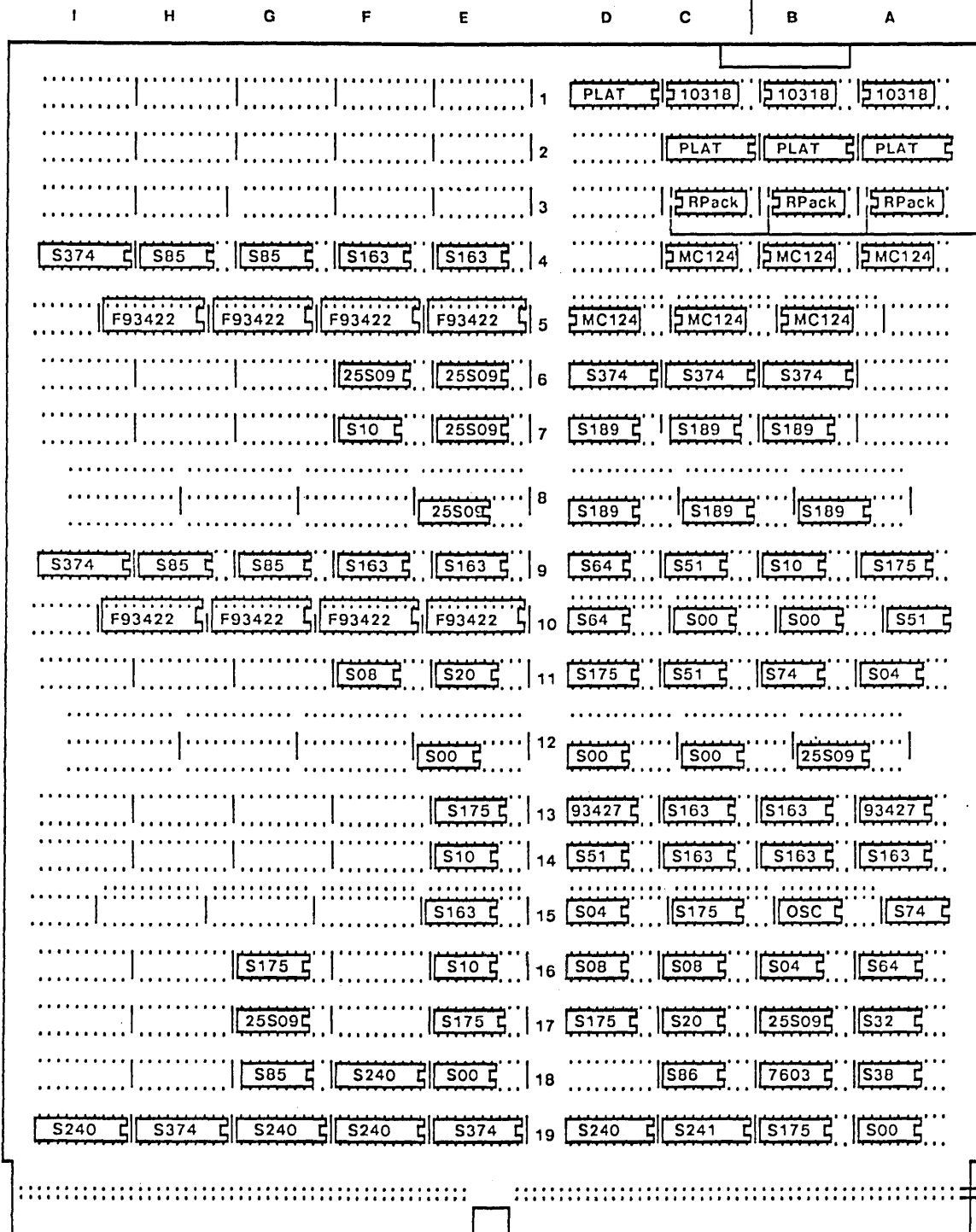


Platform a2, b2, c2  
3 required



Note: remove pins 7,8, and 9 from platform before mounting regulator.

15 Pin FEMALE Connector



10318 =  
MC10318 DAC

RPack =  
BB98-1-R270

.1uf cap  
3 places

101-200  
1-100

20pins: A



16pins: B



14pins: C



22pins: D



24 pins: E



Inverted 16-pin: F



Note: The short vertical lines indicate  
filter capacitor locations.