WIND RIVER

Wind River® Workbench for On-Chip Debugging

CONFIGURATION OPTIONS REFERENCE

2.6.1

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Wind River Workbench for On-Chip Debugging Configuration Options Reference, 2.6.1

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Contents

1 Introduction

This document describes the configuration options that are available for each target architecture that Wind River Workbench currently supports.

Configuration options change periodically, and may vary slightly depending on your architecture variant. This document is intended to provide you with general information about most of the CF options that are available for your target architecture.

Available configuration options for a given target may vary depending on whether you are connecting to the target with a Wind River ICE SX or a Wind River Probe.

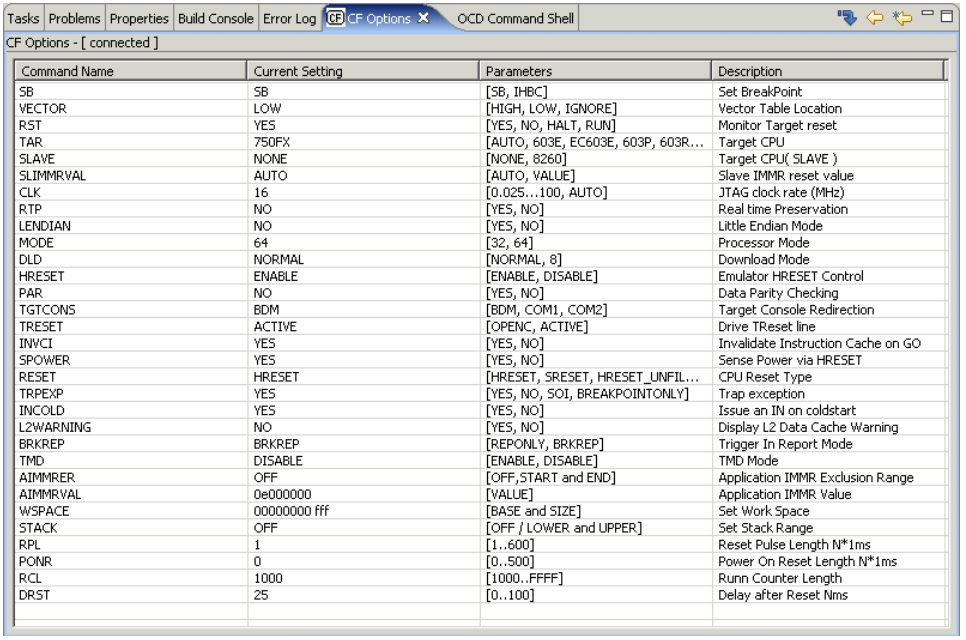
1.1 The CF Options View

To see the configuration options for your target architecture, use the **CF Options** view in Workbench. In the Workbench toolbar, select **Window** > **Show View** > **CF Options**.

NOTE: You must have your emulator connected to your host computer to see its CF options.

Figure 1-1 shows the available CF options for a Wind River Probe connected to a PPC750FX target.

Figure 1-1 **CF Options View**



Command Name	Current Setting	Parameters	Description
SB	SB	[SB, IHBC]	Set BreakPoint
VECTOR	LOW	[HIGH, LOW, IGNORE]	Vector Table Location
RST	YES	[YES, NO, HALT, RUN]	Monitor Target reset
TAR	750FX	[AUTO, 603E, EC603E, 603P, 603R...	Target CPU
SLAVE	NONE	[NONE, 8260]	Target CPU(SLAVE)
SLIMMRVAL	AUTO	[AUTO, VALUE]	Slave IMMR reset value
CLK	16	[0.025...100, AUTO]	JTAG clock rate (MHz)
RTP	NO	[YES, NO]	Real time Preservation
LENDIAN	NO	[YES, NO]	Little Endian Mode
MODE	64	[32, 64]	Processor Mode
DLD	NORMAL	[NORMAL, 8]	Download Mode
HRESET	ENABLE	[ENABLE, DISABLE]	Emulator HRESET Control
PAR	NO	[YES, NO]	Data Parity Checking
TGTCONS	BDM	[BDM, COM1, COM2]	Target Console Redirection
TRESET	ACTIVE	[OPENC, ACTIVE]	Drive TReset line
INVCI	YES	[YES, NO]	Invalidate Instruction Cache on GO
SPOWER	YES	[YES, NO]	Sense Power via HRESET
RESET	HRESET	[HRESET, SRESET, HRESET_UNFIL...	CPU Reset Type
TRPEXP	YES	[YES, NO, SOI, BREAKPOINTONLY]	Trap exception
INCOLD	YES	[YES, NO]	Issue an IN on coldstart
L2WARNING	NO	[YES, NO]	Display L2 Data Cache Warning
BRKREP	BRKREP	[REPONLY, BRKREP]	Trigger In Report Mode
TMD	DISABLE	[ENABLE, DISABLE]	TMD Mode
AIMMRER	OFF	[OFF,START and END]	Application IMMR Exclusion Range
AIMMRVAL	0e000000	[VALUE]	Application IMMR Value
WSPACE	00000000 fff	[BASE and SIZE]	Set Work Space
STACK	OFF	[OFF / LOWER and UPPER]	Set Stack Range
RPL	1	[1..600]	Reset Pulse Length N*1ms
PONR	0	[0..500]	Power On Reset Length N*1ms
RCL	1000	[1000..FFFF]	Runn Counter Length
DRST	25	[0..100]	Delay after Reset Nms

The **CF Options** view has four columns: **Command Name**, **Current Setting**, **Parameters**, and **Description**. An example entry is shown below:

Table 1-1 **CF Option Example**

Command Name	Current Setting	Parameters	Description
CHECKSTOP	YES	[YES, NO]	Enable Checkstop Interrupt

Command Name shows the low-level command you would use in the **OCD Command Shell** to change the configuration option.

Current Setting shows the parameter to which the option is currently set.

Parameters shows the available range of option parameters.

Description provides a description of the configuration option.

Choose an option and click on its entry under the **Current Settings** heading. A drop-down list will appear; scroll down the list to the parameter you want and click on it to reset the option. For example, to disable the Checkstop Interrupt, click on that option in the **Current Settings** column. The list of parameters (in this case **YES** and **NO**) will appear; click on **NO** to disable the option.

After you change the CF options, click the **Send All CF Options to Target** icon.

NOTE: Most CF options do not take effect until you issue a reset, either through the GUI or by entering the **IN** or **RST** command in the **OCD Command Shell**.

1.2 Changing CF Options with Low-Level Commands

You can also work with configuration options by using the **CF** command in the **OCD Command Shell**. At a **>BKM>** or **>ERR>** prompt, enter the command **CF**. This will bring up a list of your emulator's configuration options. You can change them using the syntax

CF *CommandName Parameter*

CommandName is the name given in the **Command Name** column in the **CF Options** view.

Parameter is the value you wish to change to.

In the example shown in Table 1-1, if the Checkstop Interrupt option is enabled and you wish to disable it, you would enter

```
CF CHECKSTOP NO
```

Enter **CF** again to see the list of options with the parameters changed. Most changes will not take effect until you issue a reset with the **IN** or **RST** command.

1.3 CF Options View Buttons

Button	Description
	Send all CF options to the target
	Restore selected CF option to the most recent valid setting
	Restore all CF options to the most recent valid settings
	Reset all CF options to target defaults

1.4 Other Resources

For more information on Workbench low-level commands, see the *Wind River Workbench On-Chip Debugging Command Reference*.

For more information on Wind River Workbench, see the *Wind River Workbench User's Guide*.

For more information on on-chip debugging, see the *Wind River Workbench On-Chip Debugging Guide*.

For more information on the Wind River ICE SX and Wind River Probe, see the *Wind River ICE SX for Wind River Workbench Hardware Reference* and the *Wind River Probe for Wind River Workbench Hardware Reference.*

For Tech Tips and Application Notes dealing with Workbench, the Wind River ICE SX and Wind River Probe tools, and various processor-specific issues, go to **http://www.windriver.com/support**.

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AMCC 40x Processors

This chapter describes the CF options that are available for AMCC 40x processors (formerly IBM 40x.).

Not all of these CF options apply to all target processors; in general, only applicable options will be visible for any given processor. Which options are visible also depends on whether you are using a Wind River Probe or Wind River ICE SX.

403 Folding (FOLDING)

CF FOLDING [YES, NO, ONRUN]

- **YES** -- (403GCX processors only) Folding is enabled on CPU, allowing multiple CPU instructions in its piped-in-queue.
- **NO** -- Folding is disabled, allowing conventional single-step operation through the emulator.
- **ONRUN** -- Folding is disabled during single-stepping, but allowed during code execution in **>RUN>** mode.

Check for Bus Error (BUSERRCHECK)

CF BUSERRCHECK[YES, NO]

This option configures the Check & Clear Bus Error Exception function.

When set to **YES** (the default), then when the target processor has a read/write Bus Error, the emulator will detect and clear exception to avoid another exception on a single step or **GO** command.

To disable the Check & Clear Bus Error Exception function, set this option to **NO**.

Debug Mode (DEBUGMODE)

CF DEBUGMODE[EXTERNAL, INTERNAL, BOTH]

This option determines whether Debug Mode relies on target codes' exception handlers.

When set to **EXTERNAL** (the default) Debug Mode does not rely on target codes' exception handlers. The emulator starts, stops, and freezes the CPU as required.

When set to **INTERNAL**, Debug Mode relies on target codes' exception handlers. This is typically used when running with ROM monitors in code.

When set to **BOTH**, Debug Mode uses the setup defined in the DBCR0 register.

Delay After Reset N*1ms (DRST)

CF DRST[0..100]

This option allows you to modify the delay after the release of **HRESET**. Delay can be set in milliseconds, from 0 to 100.

Drive TReset Line (TRESET)

CF TRESET[OPENC, ACTIVE]

This parameter controls the logic applied to the **TRESET** signal on the target. Selecting **OPENC** uses an **open collector** approach in which the active driver is released by tri-stating the line and allowing conditioning resistors on the target to return the signal to the non-active state. Selecting **ACTIVE** in this option causes the emulator to drive the **TRESET** signal to both active and inactive states. This is sometimes required on targets in which the conditioning resistors cause excessive rise or fall time on the signal when returning to an inactive state. This excessive time can cause the processor to come out of reset in an incorrect state.

Emulator HALT Command Control (CMDRST)

CF CMDRST[IN,RST,BOTH]

This configuration option is used for multicore debugging, and is used to define when the HRESET line is asserted during a reset. If the option is set to **BOTH**, any time an **IN** or a **RST** command is issued, all of the processors that are running are reset. If the option is set to **IN**, then all of the processors reset only when an **IN** command is issued. If a **RST** command is issued, only the processor that is being used is reset and the other ones are left running. If the option is set to **RST**, then all of the processors will reset if a **RST** command is issued. However, if an **IN** command is issued, only the processor that you are using will reset.

Except Handlers Available (HANDLERS)

CF HANDLERS [YES, NO]

This option indicates whether or not Exception Handler code is available to run if an exception occurs. The default is **YES**.

If this option is set to **NO**, and an Exception occurs, an error message will appear.

External Trigger In (TRGIN)

(Wind River ICE SX only)

CF TRGIN[OFF, LEVELHI, LEVELLO, EDGEHI, EDGELO]

This option sets the trigger input signal sense detection. When activated, **Trigger In** stops the target upon detection. **Trigger In** does not work with any events.

The following table describes the available settings for this option.

Table 2-1 **Trigger In Settings**

Setting	Description
OFF	Trigger signal detection is off.
LEVELHI	The trigger input level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger input level is set below 1.8 volts.

Table 2-1 **Trigger In Settings**

Setting	Description
EDGEHI	Configures the system to trigger on the rising edge of a pulse.
EDGELO	Configures the system to trigger on the falling edge of a pulse.

External Trigger In Mode (TRGINMODE)

(Wind River ICE SX only)

CF TRGINMODE[AUTO, BOTH]

This option allows users to determine where the trigger input signal sense detection come from when Wind River Trace is being used. When set to **AUTO**, the system automatically detects whether the source of the **TRGIN** is from the Wind River ICE SX or the Wind River Trace. When set to **BOTH**, the system will accept **TRGIN**s from both Wind River ICE SX and Wind River Trace. By default, this option is set to **AUTO**.

External Trigger Out (TRGOUT)

(Wind River ICE SX only)

CF TRGOUT[LEVELHI, LEVELLO, PULSEHI, PULSELO]

This option allows you to set the trigger output signal type and level. The following table describes the available settings for this option.

Table 2-2 **Trigger Out Settings**

Setting	Description
LEVELHI	The trigger output level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger output level is set below 1.8 volts.
PULSEHI	Trigger Out signal pin will be a pulse from LOW to HIGH and back to LOW when triggered.

Table 2-2 **Trigger Out Settings**

Setting	Description
PULSELO	Trigger Out signal pin will be a pulse from HIGH to LOW and back to HIGH when triggered.

FPU Available (FPU)

CF FPU [YES, NO]

Use this option to configure availability for Floating Point Units. The default is **NO**.

Flash Burst Mode (FLASHBURSTMODE)

CF FLASHBURST MODE [ENABLE, DISABLE]

When set to **DISABLE**, this option adds delays for downloads and commands to allow for slow devices whose settings have bursting disabled. When set to **ENABLE**, the option does not add delays.

The option is set to **DISABLE** by default.

Instruction-side On-chip Memory (ISOCM)

CF ISOCM [OFF , START and END]

The default is **OFF**.

Setting this option to **START and END** allows you to read and write the instruction-side on-chip memory (ISOCM), using device control registers (DCR) to display memory and set software breakpoints, on the Xilinx Virtex-4 processor.

START = starting address of the ISOCM

END = ending address of the ISOCM

Issue an IN on Coldstart (INCOLD)

CF INCOLD[YES,NO]

This option configures the emulator boot sequence.

Set this option to **YES** to issue an **IN** command, which asserts a reset on the target during a boot sequence.

Set this option to **NO** to issue a **SYNC** command instead of asserting reset on the target. The **SYNC** command does not reset the board. It establishes JTAG communications and captures the current context. This option is best if you want to hot plug the emulator into a running target.

The default is **NO**.

JTAG Clock Rate (MHz) (CLK)

CF CLK[0.025...100, AUTO]

This option configures the rate at which debug commands are clocked to the target. The default setting is **16**.

Little-endian Mode (LENDIAN)

CF LENDIAN[YES,NO]

This configuration value determines whether the debugger treats memory contents as little-endian (bits ordered 0..63) or big-endian (bits ordered 63..0.) This affects display and interpretation of opcodes in the debugger window, as well as the effects of symbolic manipulation of variables. Setting this option to **YES** means that little-endian is used; setting the option to **NO** means that big-endian is used.

Load Boot Table on IN (BL)

CF BL [ENABLE, DISABLE]

This option enables or disables the Linux bootline commands.

Logic Analyzer Trace (LATRACE)

CF LATRACE[NONE, AGILENT, TEKTRONIX]

This configuration option is necessary if you are using a Logic Analyzer for trace acquisition. Configuring and controlling the logic analyzer is dependant upon the manufacturer of the logic analyzer. Current support is available for Agilent and Tektronix solutions only. If you are not using a Logic Analyzer, set this option to **NONE**.

Memory Management Unit Mode (MMU)

CF MMU[ENABLE, DISABLE]

Use this option to enable or disable Linux Memory Management support.

Monitor Target Reset (RST)

CF RST[YES, NO, HALT, RUN]

This function continuously monitors the target reset signal. If a reset occurs, one of the following actions may be taken:

- **YES** - If a target reset occurs it is reported to the user and BDM control is lost.
- **NO** - If a target reset occurs it is ignored. This is normally used if the code contains a reset instruction, which causes a reset to the external hardware, but not reset the core.
- **HALT** - If the reset occurs in this mode the target is trapped at the restart vector.
- **RUN** - If the reset occurs in this mode the target is restarted and BDM control is maintained.

By default, this option is set to **YES**. It should only be changed to **NO** if you have a RESET instruction in your code.

Real Time Preservation (RTP)

CF RTP[YES, NO]

When this option is enabled, real-time preservation allows the target to run without the emulator stopping the target inadvertently.

Reset Option (RESET)

CF RESET[SYSTEM, CHIP, CORE]

This option determines the scope of the reset performed when you issue an **IN** or **INN** command.

- **SYSTEM** --The **IN** or **INN** command will assert the target processor's System Reset, which typically resets the entire target.
- **CHIP** --The **IN** or **INN** command will assert the target processor's Chip Reset only.
- **CORE** --The **IN** or **INN** command will assert the target processor's Core Reset only.

Retry Establishing Connection on IN/INN (RETRYIN)

CF RETRYIN[YES, NO]

This option configures whether the emulator will continue trying to connect to the target board after it has failed to connect. When set to **YES**, the emulator will try again after an **IN** or **INN** command fails. When set to **NO**, the emulator will try to connect only once.

The option is set to **NO** by default.

Set Breakpoint (SB)

CF SB[SB,IHBC]

This option remaps traditional software breakpoints to internal hardware breakpoints. It is set to Software Breakpoint (**SB**) by default. Setting it to **IHBC** means that all software breakpoints are translated to internal hardware breakpoints. This option is useful when you are debugging code out of Flash or PROM.

Setting this option to **IHBC** may cause limitations in the number of breakpoints that can be set, depending on the target processor.

Set SDRAM/SRAM Data Address Range (DATA)

CF DATA[OFF, LOWER and UPPER]

Set this option to **LOWER and UPPER** to set the SDRAM/SRAM data address range.

The option is set to **OFF** by default.

Set Stack Range (STACK)

CF STACK[OFF/Lower and **Upper]**

This setting is **OFF** by default. When stack limits are set, it prevents the emulator from walking through the stack, past the specified range, and causing accidental bus errors.

Set Work Space (WSPACE)

CF WSPACE[BASE and **SIZE]**

Flash programming requires a small amount of target RAM to program the flash algorithm. You must tell your emulator where writable RAM is located on your target for this purpose.

As part of the configuration process, the emulator will indicate exactly how much of the RAM workspace is required. Depending on the device family and type, this space is limited to under 2 KB. Note that more memory improves the speed of programming.

To configure the workspace for flash programming the parameters should be entered in hex, where **BASE** is the start address, and **SIZE** is the minimum bytes of target RAM required, as displayed in the **Flash Programmer** view. This command allocates memory on the target system that is used by the emulator for various functions, including flash programming.

Target Console Redirection (TGTCONS)

CF TGTCONS [**TGTCONS**, **BDM**] (for the Wind River ICE SX)

Wind River Probe

Target Console Redirection is not currently supported for the Wind River Probe. You do not need to set this option.

Wind River ICE SX

BDM -- Use this setting to connect I/O on a target board, using the Transparent Mode Driver, to the target's BDM connector. When **BDM** is selected, the Wind River ICE SX is in Transparent Mode, and all I/O data is redirected to the port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

For this type of connection to work, the target application must be linked to the Transparent Mode Driver. Refer to the *Wind River Workbench On-Chip Debugging Guide: Using the WDB Transparent Mode Driver* for more information.

TGTCONS -- Use this setting to connect a COM port on a target board to the TGTCONS port of a Wind River ICE SX. All I/O data is then redirected to port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

Target CPU (TAR)

CF TAR *target processor*

This option allows you to configure the emulator for the target that you are using. *target processor* is the name of your processor. For example, to configure the emulator for a PowerPC 405GP target, type:

```
CF TAR 405GP
```

Timer Options (TIMERS)

CF TIMERS[ON, OFF, OFFSTEP_ONGO]

This option controls the timers on the internal processor.

ON --The timers on the internal processor are left on.

OFF --The timers on the internal processor are forced (held) off while in Debug Mode (that is, when a **>BKM>** prompt is visible in the **OCD Command Shell**) and only application code can re-enable them.

OFFSTEP_ONGO --The timers on the internal processor are held off while in Debug Mode and while code stepping, and released on a **GO** command.

Trap Exception (TRPEXP)

CF TRPEXP[YES, NO, YES_LEAVEMSR_ONSTEP, NO_LEAVEMSR_ONSTEP, YES_ALL]

This option allows you to configure which run time exceptions are trapped.

- **YES** -- All exceptions or interrupts detected by the emulator will be trapped and the CPU will be halted.
- **NO** -- All exceptions will be ignored.
- **YES_LEAVEMSR_ONSTEP** -- The emulator will trap interrupts and exceptions but leave/restore the MSR as is when single-stepping.
- **NO_LEAVEMSR_ONSTEP** -- The emulator will ignore interrupts and exceptions, and allow the code's interrupt handlers to run on a **GO.** The emulator will leave/restore the MSR as is when single-stepping.
- **YES_ALL** -- The emulator will trap all exceptions and set Vector Location to allow stepping through exception vector code.

Trigger in Filter Mode (TRGINFILTER)

(Wind River ICE SX only)

CF TRGINFILTER[OFF,ON]

This option provides a filtering option for the Trigger In function. When set to **ON**, a detected signal is required for at least 2 clock periods, or 40ns. This option ensures that noise does not cause a trigger.

Trigger Out Mode (TRGOUTMODE)

(Wind River ICE SX only)

CF TRGOUTMODE[OFF, ONALLSTOPS, ONBREAKPOINT]

This option allows you to set the type of events that will cause a trigger output to occur.

OFF -- Trigger output is off.

ONALLSTOPS -- Triggers whenever the target stops running.

ONBREAKPOINT -- Triggers whenever a breakpoint is encountered.

(USENVRAMFLASHVALUES)

CF USENVRAMFLASHVALUES [YES, NO]

When set to **NO**, this option will use default reset flash values.

Default reset flash values usually have bursting disabled and may cause errors at the default clock speed. When set to **YES**, this option will use the default NVRAM register values, which normally have bursting enabled.

The option is set to **YES** by default.

Validate Memory Access (MEMCHECK)

CF MEMCHECK[YES, NO]

When this option is set to **YES** (the default), the emulator will check memory addresses for validity prior to accessing the target processor, to avoid target hangs.

To disable the memory check, set this option to **NO**.

Vector Table Location (VECTOR)

CF VECTOR[HIGH, LOW, IGNORE]

This command specifies the location of the exception vector that is used by the software breakpoints. Please note that this setting must match the MSR register setting for software breakpoints to function correctly.

2.1 CF Options for Wind River Trace

AMCC 40x processors use several configuration options that are only available when connected to a Wind River Trace.

Acquire Trace on GO (TRCAQU)

CF TRCAQU [OFF, ON}

Use this option to configure how Wind River Trace starts to store trace information.

When the target begins running code, Wind River Trace can either wait until an event occurs to start storing trace information, or it can start immediately.

When this option is set to **ON**, Wind River Trace starts acquiring trace information as soon as a **GO** command is issued, and does not stop until an event occurs to disable trace.

When this option is set to **OFF**, Wind River Trace does not begin acquiring trace information until an event occurs to turn trace on.

Clear Trace Buffer on GO (TRCCLR)

CF TRCCLR [YES, NO]

Use this option to control where to start saving trace data in the trace memory.

YES -- When a **GO** command is issued, all newly captured trace data will be stored starting at the first trace memory location. All previously stored trace data will be overwritten and lost.

NO -- When a **GO** command is issued, all newly captured trace data will be stored starting at the next trace memory location. Previously stored trace data will not be overwritten.

3

AMCC 44x Processors

This chapter describes the CF options that are available for AMCC 44x processors (formerly IBM 44x.)

Not all of these CF options apply to all target processors; in general, only applicable options will be visible for any given processor. Which options are visible also depends on whether you are using a Wind River Probe or Wind River ICE SX.

Check for Bus Error (BUSERRCHECK)

CF BUSERRCHECK[YES, NO]

This option configures the Check & Clear Bus Error Exception function.

When set to **YES** (the default), then when the target processor has a read/write Bus Error, the emulator will detect and clear exception to avoid another exception on a single step or **GO** command.

To disable the Check & Clear Bus Error Exception function, set this option to **NO**.

Debug Mode (DEBUGMODE)

CF DEBUGMODE[EXTERNAL, INTERNAL, BOTH]

This option determines whether Debug Mode relies on target codes' exception handlers.

When set to **EXTERNAL** (the default) Debug Mode does not rely on target codes' exception handlers. The emulator starts, stops, and freezes the CPU as required.

When set to **INTERNAL**, Debug Mode relies on target codes' exception handlers. This is typically used when running with ROM monitors in code.

When set to **BOTH**, Debug Mode uses the setup defined in the DBCR0 register.

Delay After Reset N*1ms (DRST)

CF DRST[0..100]

This option allows you to modify the delay after the release of **HRESET**. Delay can be set in milliseconds, from 0 to 100.

Drive TReset Line (TRESET)

CF TRESET[OPENC, ACTIVE]

This parameter controls the logic applied to the **TRESET** signal on the target. Selecting **OPENC** uses an **open collector** approach in which the active driver is released by tri-stating the line and allowing conditioning resistors on the target to return the signal to the non-active state. Selecting **ACTIVE** in this option causes the emulator to drive the **TRESET** signal to both active and inactive states. This is sometimes required on targets in which the conditioning resistors cause excessive rise or fall time on the signal when returning to an inactive state. This excessive time can cause the processor to come out of reset in an incorrect state.

Emulator HALT Command Control (CMDRST)

CF CMDRST[IN,RST,BOTH]

This configuration option is used for multicore debugging, and is used to define when the HRESET line is asserted during a reset. If the option is set to **BOTH**, any time an **IN** or a **RST** command is issued, all of the processors that are running are reset. If the option is set to **IN**, then all of the processors reset only when an **IN** command is issued. If a **RST** command is issued, only the processor that is being used is reset and the other ones are left running. If the option is set to **RST**, then all of the processors will reset if a **RST** command is issued. However, if an **IN** command is issued, only the processor that you are using will reset.

Except Handlers Available (HANDLERS)

CF HANDLERS [YES, NO]

This option indicates whether or not Exception Handler code is available to run if an exception occurs. The default is **YES**.

If this option is set to **NO**, and an exception occurs, an error message will appear.

External Trigger In (TRGIN)

(Wind River ICE SX only)

CF TRGIN[OFF, LEVELHI, LEVELLO, EDGEHI, EDGELO]

This option sets the trigger input signal sense detection. When activated, **Trigger In** stops the target upon detection. **Trigger In** does not work with any events.

The following table describes the available settings for this option.

Table 3-1 **Trigger In Settings**

Setting	Description
OFF	Trigger signal detection is off.
LEVELHI	The trigger input level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger input level is set below 1.8 volts.
EDGEHI	Configures the system to trigger on the rising edge of a pulse.
EDGELO	Configures the system to trigger on the falling edge of a pulse.

External Trigger In Mode (TRGINMODE)

(Wind River ICE SX only)

CF TRGINMODE[AUTO, BOTH]

This option allows users to determine where the trigger input signal sense detection come from when Wind River Trace is being used. When set to **AUTO**, the system automatically detects whether the source of the **TRGIN** is from the

Wind River ICE SX or the Wind River Trace. When set to **BOTH**, the system will accept **TRGIN**s from both Wind River ICE SX and Wind River Trace. By default, this option is set to **AUTO**.

External Trigger Out (TRGOUT)

(Wind River ICE SX only)

CF TRGOUT[LEVELHI, LEVELLO, PULSEHI, PULSELO]

This option allows you to set the trigger output signal type and level. The following table describes the available settings for this option.

Table 3-2 **Trigger Out Settings**

Setting	Description
LEVELHI	The trigger output level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger output level is set below 1.8 volts.
PULSEHI	Trigger Out signal pin will be a pulse from LOW to HIGH and back to LOW when triggered.
PULSELO	Trigger Out signal pin will be a pulse from HIGH to LOW and back to HIGH when triggered.

Flash Burst Mode (FLASHBURSTMODE)

CF FLASHBURST MODE [ENABLE, DISABLE]

When set to **DISABLE**, this option adds delays for downloads and commands to allow for slow devices whose settings have bursting disabled. When set to **ENABLE**, the option does not add delays.

The option is set to **DISABLE** by default.

FPU Available (FPU)

CF FPU [YES, NO]

Use this option to configure availability for Floating Point Units. The default is **NO**.

Invalidate Instruction Cache on GO (INVICACHEONGO)

CF INVICACHEONGO [YES,NO]

This option controls whether the contents of the target processor's Instruction Cache are invalidated when you issue a **GO** command. Setting this option to **YES** causes the cache contents to be invalidated.

Invalidate Instruction Cache on Single Step (INVICACHEONSTEP)

CF INVICACHEONSTEP[YES, NO]

This option controls whether the contents of the target processor's Instruction Cache are invalidated on each single-step. The default setting is **NO**.

Issue an IN on Coldstart (INCOLD)

CF INCOLD[YES,NO]

This option configures the emulator boot sequence.

Set this option to **YES** to issue an **IN** command, which asserts a reset on the target during a boot sequence.

Set this option to **NO** to issue a **SYNC** command instead of asserting reset on the target. The **SYNC** command does not reset the board. It establishes JTAG communications and captures the current context. This option is best if you want to hot plug the emulator into a running target.

The default is **NO**.

JTAG Clock Rate (MHz) (CLK)

CF CLK[0.025...100, AUTO]

This option configures the rate at which debug commands are clocked to the target. The default setting is **16**.

Little-endian Mode (LENDIAN)

CF LENDIAN[YES,NO]

This configuration value determines whether the debugger treats memory contents as little-endian (bits ordered 0..63) or big-endian (bits ordered 63..0.) This affects display and interpretation of opcodes in the debugger window, as well as the effects of symbolic manipulation of variables. Setting this option to **YES** means that little-endian is used; setting the option to **NO** means that big-endian is used.

Load Boot Table on IN (BL)

CF BL [ENABLE, DISABLE]

This option enables or disables the Linux bootline commands.

Logic Analyzer Trace (LATRACE)

CF LATRACE[NONE, AGILENT, TEKTRONIX]

This configuration option is necessary if you are using a Logic Analyzer for trace acquisition. Configuring and controlling the logic analyzer is dependant upon the manufacturer of the logic analyzer. Current support is available for Agilent and Tektronix solutions only. If you are not using a Logic Analyzer, set this option to **NONE**.

Memory Management Unit Mode (MMU)

CF MMU[ENABLE, DISABLE]

Use this option to enable or disable Linux Memory Management support.

Monitor Target Reset (RST)

CF RST[YES, NO, HALT, RUN]

This function continuously monitors the target reset signal. If a reset occurs, one of the following actions may be taken:

- **YES** - If a target reset occurs it is reported to the user and BDM control is lost.

- **NO** - If a target reset occurs it is ignored. This is normally used if the code contains a reset instruction, which causes a reset to the external hardware, but not reset the core.
- **HALT** - If the reset occurs in this mode the target is trapped at the restart vector.
- **RUN** - If the reset occurs in this mode the target is restarted and BDM control is maintained.

By default, this option is set to **YES**. It should only be changed to **NO** if you have a RESET instruction in your code.

Real Time Preservation (RTP)

CF RTP[YES, NO]

When this option is enabled, real-time preservation allows the target to run without the emulator stopping the target inadvertently.

Reset Chip for CPC0_SYS0/1 Updates (UPDATESYSREGS)

CF UPDATESYSREGS[YES, NO]

When set to **YES** (the default), when an **IN** or **INN** command is issued, the CPC0_SYS0 and CPC0_SYS1 registers on the target processor are updated with SIM register values and the target is reset. To stop these registers from being updated, set this option to **NO**.

Reset Configuration Word Location (RSTCONF)

CF RSTCONF[AUTO, HIGH, LOW]

The reset configuration word is read by the emulator during initialization to determine the reset IMMR value. When set to **AUTO**, the emulator searches all valid Reset Word locations to find the value.

Reset Option (RESET)

CF RESET[SYSTEM, CHIP, CORE]

This option determines the scope of the reset performed when you issue an **IN** or **INN** command.

- **SYSTEM** --The **IN** or **INN** command will assert the target processor's System Reset, which typically resets the entire target.
- **CHIP** --The **IN** or **INN** command will assert the target processor's Chip Reset only.
- **CORE** --The **IN** or **INN** command will assert the target processor's Core Reset only.

Retry Establishing Connection on IN/INN (RETRYIN)

CF RETRYIN[YES, NO]

This option configures whether the emulator will continue trying to connect to the target board after it has failed to connect. When set to **YES**, the emulator will try again after an **IN** or **INN** command fails. When set to **NO**, the emulator will try to connect only once.

The option is set to **NO** by default.

Set Breakpoint (SB)

CF SB[SB,IHBC]

This option remaps traditional software breakpoints to internal hardware breakpoints. It is set to Software Breakpoint (**SB**) by default. Setting it to **IHBC** means that all software breakpoints are translated to internal hardware breakpoints. This option is useful when you are debugging code out of Flash or PROM.

Setting this option to **IHBC** may cause limitations in the number of breakpoints that can be set, depending on the target processor.

Set SDRAM/SRAM Data Address Range (DATA)

CF DATA[OFF, LOWER and UPPER]

Set this option to **LOWER and UPPER** to set the SDRAM/SRAM data address range.

The option is set to **OFF** by default.

Set Stack Range (STACK)

CF STACK[OFF/Lower and **Upper]**

This setting is **OFF** by default. When stack limits are set, it prevents the emulator from walking through the stack, past the specified range, and causing accidental bus errors.

Set Work Space (WSPACE)

CF WSPACE[BASE and **SIZE]**

Flash programming requires a small amount of target RAM to program the flash algorithm. You must tell your emulator where writable RAM is located on your target for this purpose.

As part of the configuration process, the emulator will indicate exactly how much of the RAM workspace is required. Depending on the device family and type, this space is limited to under 2 KB. Note that more memory improves the speed of programming.

To configure the workspace for flash programming the parameters should be entered in hex, where **BASE** is the start address, and **SIZE** is the minimum bytes of target RAM required, as displayed in the **Flash Programmer** view. This command allocates memory on the target system that is used by the emulator for various functions, including flash programming.

Target Console Redirection (TGTCONS)

CF TGTCONS [TGTCONS, BDM] (for the Wind River ICE SX)

Wind River Probe

Target Console Redirection is not currently supported for the Wind River Probe. You do not need to set this option.

Wind River ICE SX

BDM -- Use this setting to connect I/O on a target board, using the Transparent Mode Driver, to the target's BDM connector. When **BDM** is selected, the Wind River ICE SX is in Transparent Mode, and all I/O data is redirected to the port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

For this type of connection to work, the target application must be linked to the Transparent Mode Driver. Refer to the *Wind River Workbench On-Chip Debugging Guide: Using the WDB Transparent Mode Driver* for more information.

TGTCONS -- Use this setting to connect a COM port on a target board to the TGTCONS port of a Wind River ICE SX. All I/O data is then redirected to port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

Target CPU (TAR)

CF TAR *target processor*

This option allows you to configure the emulator for the target that you are using. *target processor* is the name of your processor. For example, to configure the emulator for a PowerPC 440GX target, type:

```
CF TAR 440GX
```

Timer Options (TIMERS)

CF TIMERS[ON, OFF, OFFSTEP_ONGO]

This option controls the timers on the internal processor.

ON- -The timers on the internal processor are left on.

OFF --The timers on the internal processor are forced (held) off while in Debug Mode (that is, when a **>BKM>** prompt is visible in the **OCD Command Shell**) and only application code can re-enable them.

OFFSTEP_ONGO --The timers on the internal processor are held off while in Debug Mode and while code stepping, and released on a **GO** command.

Transparent Mode Driver (TMD)

CF TMD[ENABLE, DISABLE]

This command sets all of the configuration parameters that are required to use the Transparent Mode Driver (TMD). Select **ENABLE** to configure your system for use with the TMD, and **DISABLE** if you do not plan to use it.

Trap Exception (TRPEXP)

CF TRPEXP[YES, NO, YES_LEAVEMSR_ONSTEP, NO_LEAVEMSR_ONSTEP, YES_ALL]

This option allows you to configure which run time exceptions are trapped.

- **YES** -- All exceptions or interrupts detected by the emulator will be trapped and the CPU will be halted.
- **NO** -- All exceptions will be ignored.
- **YES_LEAVEMSR_ONSTEP** -- The emulator will trap interrupts and exceptions but leave/restore the MSR as is when single-stepping.
- **NO_LEAVEMSR_ONSTEP** -- The emulator will ignore interrupts and exceptions, and allow the code's interrupt handlers to run on a **GO.** The emulator will leave/restore the MSR as is when single-stepping.
- **YES_ALL** -- The emulator will trap all exceptions and set Vector Location to allow stepping through exception vector code.

Trigger in Filter Mode (TRGINFILTER)

(Wind River ICE SX only)

CF TRGINFILTER[OFF,ON]

This option provides a filtering option for the Trigger In function. When set to **ON**, a detected signal is required for at least 2 clock periods, or 40ns. This option ensures that noise does not cause a trigger.

Trigger Out Mode (TRGOUTMODE)

(Wind River ICE SX only)

CF TRGOUTMODE[OFF, ONALLSTOPS, ONBREAKPOINT]

This option allows you to set the type of events that will cause a trigger output to occur.

OFF -- Trigger output is off.

ONALLSTOPS -- Triggers whenever the target stops running.

ONBREAKPOINT -- Triggers whenever a breakpoint is encountered.

Use NVRAM Flash Values (USENVRAMFLASHVALUES)

CF USENVRAMFLASHVALUES [YES, NO]

When set to **NO**, this option will use default reset flash values.

Default reset flash values usually have bursting disabled and may cause errors at the default clock speed. When set to **YES**, this option will use the default NVRAM register values, which normally have bursting enabled.

The option is set to **YES** by default.

Validate Memory Access (MEMCHECK)

CF MEMCHECK[YES, NO]

When this option is set to **YES** (the default), the emulator will check memory addresses for validity prior to accessing the target processor, to avoid target hangs.

To disable the memory check, set this option to **NO**.

Vector Table Location (VECTOR)

CF VECTOR[HIGH, LOW, IGNORE]

This command specifies the location of the exception vector that is used by the software breakpoints. Please note that this setting must match the MSR register setting for software breakpoints to function correctly.

3.1 CF Options for Wind River Trace

AMCC 40x processors use several configuration options that are only available when connected to a Wind River Trace.

Acquire Trace on GO (TRCAQU)

CF TRCAQU [OFF, ON}

Use this option to configure how Wind River Trace starts to store trace information.

When the target begins running code, Wind River Trace can either wait until an event occurs to start storing trace information, or it can start immediately.

When this option is set to **ON**, Wind River Trace starts acquiring trace information as soon as a **GO** command is issued, and does not stop until an event occurs to disable trace.

When this option is set to **OFF**, Wind River Trace does not begin acquiring trace information until an event occurs to turn trace on.

Clear Trace Buffer on GO (TRCCLR)

CF TRCCLR [YES, NO]

Use this option to control where to start saving trace data in the trace memory.

YES -- When a **GO** command is issued, all newly captured trace data will be stored starting at the first trace memory location. All previously stored trace data will be overwritten and lost.

NO -- When a **GO** command is issued, all newly captured trace data will be stored starting at the next trace memory location. Previously stored trace data will not be overwritten.

The default is **NO**.

Trace Output Source (TRCSRC)

(440GX processors only)

CF TRCSRC [GPIO, EBMI]

Use this option to select a source for trace output.

Trace signals can come from the General Purpose Input/Output (GPIO) port, or the External Bus Master Interface (EBMI). The default is **GPIO**.

Portions of the trace signals coming out of the GPIO port are mixed with the Gigabit Ethernet control signals. If you want to use all available Gigabit modes, and still want to be able to debug with the trace, you can let these trace signals come from the external bus master interface by setting this option to **EBMI**.

4

PowerPC 5xx Processors

This chapter describes the configuration options available for PowerPC 5xx processors.

Not all of these CF options apply to all target processors; in general, only applicable options will be visible for any given processor.

29-31 Bits of ICTRL Register (ICTRLVAL)

CF ICTRLVAL[**0...7**]

Use this option to force the CPU 2 ICTRL Register bits 9-31 on the target processor to a value of **0...7**. This determines extra information cycles emitted onto the external CPU bus.

BDM Clock Rate (CLK)

CF CLK [**0.1, 0.5, 1, 3, 6, 12**]

Use this option to set the BDM clock frequency, in megahertz, that is used for BDM communications. The settings are used to control the **DSCLK** signal frequency on the 26/30 pin BDM connector. For brevity, the settings listed are approximations of the actual frequency. What setting you should use depends on the core frequency of your target processor. The maximum BDM clock frequency is limited to 20 per cent of the core frequency. Generally, the higher the core frequency, the higher the **CLK** parameter setting can be. A little experimenting with this setting will allow you to maximize the BDM communications speed. This is significant for maximizing image download and upload speeds. The default value is **12**.

Enable Target Machine Check (TRPMC)

CF TRPMC[YES, NO]

This option allows the user to configure the emulator to trap machine checks generated by the processor (option set to **YES**) or to allow the trap to be passed to the software exception handler and ignored by the emulator (option set to **NO**.)

External Trigger In (TRGIN)

CF TRGIN[OFF, LEVELHI, LEVELLO, EDGEHI, EDGELO]

This option sets the trigger input signal sense detection. When activated, **Trigger In** stops the target upon detection. **Trigger In** does not work with any events.

The following table describes the available settings for this option.

Table 4-1 **Trigger In Settings**

Setting	Description
OFF	Trigger signal detection is off.
LEVELHI	The trigger input level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger input level is set below 1.8 volts.
EDGEHI	Configures the system to trigger on the rising edge of a pulse.
EDGELO	Configures the system to trigger on the falling edge of a pulse.

External Trigger Out (TRGOUT)

CF TRGOUT[LEVELHI, LEVELLO, PULSEHI, PULSELO]

This option allows you to set the trigger output signal type and level. The following table describes the available settings for this option.

Table 4-2 **Trigger Out Settings**

Setting	Description
LEVELHI	The trigger output level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger output level is set below 1.8 volts.
PULSEHI	Trigger Out signal pin will be a pulse from LOW to HIGH and back to LOW when triggered.
PULSELO	Trigger Out signal pin will be a pulse from HIGH to LOW and back to HIGH when triggered.

Logic Analyzer Trace (LATRACE)

CF LATRACE[NONE, AGILENT, TEKTRONIX]

This configuration option is necessary if you are using a Logic Analyzer for trace acquisition. Configuring and controlling the logic analyzer is dependant upon the manufacturer of the logic analyzer. Current support is available for Agilent and Tektronix solutions only. If you are not using a Logic Analyzer, set this option to **NONE**.

Memory Management Unit (MMU)

CF MMU[OFF, LINUX]

Use this option to enable or disable Linux Memory Management support.

Monitor Target Reset (RST)

CF RST[YES, NO, HALT, RUN]

This function continuously monitors the target reset signal. If a reset occurs, one of the following actions may be taken:

- **YES** - If a target reset occurs it is reported to the user and BDM control is lost.
- **NO** - If a target reset occurs it is ignored. This is normally used if the code contains a reset instruction, which causes a reset to the external hardware, but not reset the core.

- **HALT** - If the reset occurs in this mode the target is trapped at the restart vector.
- **RUN** - If the reset occurs in this mode the target is restarted and BDM control is maintained.

By default, this option is set to **YES**. It should only be changed to **NO** if you have a RESET instruction in your code.

Real Time Preservation (RTP)

CF RTP[YES,NO]

When this option is enabled, real-time preservation allows the target to run without the emulator stopping the target inadvertently.

Set Breakpoint (SB)

CF SB[SB,IHBC]

This option remaps traditional software breakpoints to internal hardware breakpoints. It is set to Software Breakpoint (**SB**) by default. Setting it to **IHBC** means that all software breakpoints are translated to internal hardware breakpoints. This option is useful when you are debugging code out of flash or PROM.

Setting this option to **IHBC** may cause limitations in the number of breakpoints that can be set, depending on the target processor.

Set Work Space (WSPACE)

CF WSPACE[BASE and **SIZE]**

Flash programming requires a small amount of target RAM to program the flash algorithm. You must tell your emulator where writable RAM is located on your target for this purpose.

As part of the configuration process, the emulator will indicate exactly how much of the RAM workspace is required. Depending on the device family and type, this space is limited to under 2 KB. Note that more memory improves the speed of programming.

To configure the workspace for flash programming the parameters should be entered in hex, where **BASE** is the start address, and **SIZE** is the minimum bytes of

target RAM required, as displayed in the **Flash Programmer** view. This command allocates memory on the target system that is used by the emulator for various functions, including flash programming.

Software Breakpoint Emulation Method (SBE)

CF SBE [NORMAL, SPECIAL]

This command is used to configure the method that the emulator and the target use to handle software breakpoints. When set to **NORMAL**, which is the default setting, the system assigns the software breakpoints to use the software emulation exception as the method of setting breakpoints. When set to **SPECIAL**, the system assigns the software breakpoints to use a misalignment exception as the method of setting breakpoints. This selection is only necessary if the application being debugged uses software emulation for another purpose.

Target Console Redirection (TGTCONS)

CF TGTCONS [BDM, TGTCONS]

Wind River Probe

Target Console Redirection is not currently supported for the Wind River Probe. You do not need to set this option.

Wind River ICE SX

Use this option to set the target console setting. The default setting is **BDM**. The target console settings are used as follows:

BDM -- Use this setting to connect I/O on a target board, using the Transparent Mode Driver, to the target's BDM connector. When **BDM** is selected, the Wind River ICE SX is in Transparent Mode, and all I/O data is redirected to the port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

For this type of connection to work, the target application must be linked to the Transparent Mode Driver. Refer to the *Wind River Workbench On-Chip Debugging Guide: Using the WDB Transparent Mode Driver* for more information.

TGTCONS -- Use this setting to connect a COM port on a target board to the TGTCONS port of a Wind River ICE SX. All I/O data is then redirected to port

1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

Target CPU (TAR)

CF TAR *target processor*

This option allows you to configure the emulator for the target that you are using. *target processor* is the name of your processor. For example, to configure the emulator for a PowerPC 509 target, type:

```
CF TAR 509
```

Trap Exception (TRPEXP)

CF TRPEXP[YES, NO, DER]

This option allows you to configure which run time exceptions are trapped. Setting this option to **YES** causes the emulator to trap RST, CHSTP, MCI, ALI, TRE, SEI, LBRK, IBRK, EBRK, and DPI exceptions. Setting it to **NO** causes the emulator not to trap any exceptions other than TRE and SE. Setting the option to **DER** causes the emulator to trap exceptions as masked by the (previously set) DER register.

To set the DER register, enter

SR DER *value*

at the **>BKM>** prompt in the **Terminal** window.

Trigger in Filter Mode (TRGINFILTER)

CF TRGINFILTER[OFF,ON]

This option provides a filtering option for the Trigger In function. When set to **ON**, a detected signal is required for at least 2 clock periods, or 40ns. This option ensures that noise does not cause a trigger.

Trigger In Report Mode (BRKREP)

CF BRKREP [REPONLY, BRKREP]

When this option is set to **BRKREP**, which is the default setting, a Trigger In signal will be reported and set a breakpoint. When set to **REPONLY**, a Trigger in signal will be reported, but will not set a breakpoint.

Trigger Out Mode (TRGOUTMODE)

CF TRGOUTMODE[OFF, ONALLSTOPS, ONBREAKPOINT]

This option allows you to set the type of events that will cause a trigger output to occur.

OFF -- Trigger output is off.

ONALLSTOPS -- Triggers whenever the target stops running.

ONBREAKPOINT -- Triggers whenever a breakpoint is encountered.

Vector Table Location (VECTOR)

CF VECTOR[HIGH, LOW, IGNORE]

This command specifies the location of the exception vector that is used by the software breakpoints. Please note that this setting must match the MSR register setting for software breakpoints to function correctly.

Wait to Enter Background Mode N*100ms (FRZ)

CF FRZ [1...600]

This command sets the length of time that the system waits for the target to enter background mode before it times out. The **FRZ** command can be set between 1 and 600 ms. By default, the option is set to time out after 1 ms. Note that sometimes the response will be slow if the BUS master is an external device. If the timeout period expires, the emulator will report **Time Out Waiting for FREEZE**.

5 PowerPC 5xxx Processors

This chapter describes the configuration options available for PowerPC 5xxx processors.

Not all of these CF options apply to all target processors; in general, only applicable options will be visible for any given processor. Which options are visible also depends on whether you are using a Wind River Probe or Wind River ICE SX.

CPU Reset Type (RESET)

CF RESET[HRESET, SRESET, HRESET_UNFILTER, SRESET_UNFILTER]

This option allows you to generate either a **HRESET** or a **SRESET** signal when an **IN** or **INN** command is issued. Selecting **HRESET_UNFILTER** or **SRESET_UNFILTER** means that the reset signal is not sampled when an **IN** or **INN** command is issued.

Delay After Reset N*1ms (DRST)

CF DRST[0..100]

This option allows you to modify the delay after the release of **HRESET**. Delay can be set in milliseconds, from 0 to 100.

Display L2 Data Cache Warning (L2WARNING)

CF L2WARNING[YES,NO]

This option can display a warning when you try to read a value from data that has been stored in the L2 cache on your target. When set to **YES**, the warning displays and the memory value is read from RAM. When set to **NO**, the memory value is read from RAM and no warning is displayed.

Download Mode (DLD)

CF DLD[NORMAL,8]

This parameter controls the size of memory transfers when downloading code. Set this option to the width of the memory that you are planning to download your code to. Setting the option to **NORMAL** means that the bus width is 64 bits, and **8** means that the bus width is 8 bits.

Drive TReset Line (TRESET)

CF TRESET[OPENC, ACTIVE]

This parameter controls the logic applied to the **TRESET** signal on the target. Selecting **OPENC** uses an **open collector** approach in which the active driver is released by tri-stating the line and allowing conditioning resistors on the target to return the signal to the non-active state. Selecting **ACTIVE** in this option causes the emulator to drive the **TRESET** signal to both active and inactive states. This is sometimes required on targets in which the conditioning resistors cause excessive rise or fall time on the signal when returning to an inactive state. This excessive time can cause the processor to come out of reset in an incorrect state.

Emulator HRESET Control (HRESET)

CF HRESET[ENABLE, DISABLE]

This option determines whether the **HRESET** line is asserted when you issue an **IN** command. Selecting **ENABLE** asserts **HRESET**, and selecting **DISABLE** prevents **HRESET** from being asserted.

Emulator HRESET Command Control (CMDRST)

(Wind River ICE SX only)

CF CMDRST[IN,RST,BOTH]

This configuration option is used for multicore debugging, and is used to define when the HRESET line is asserted during a reset. If the option is set to **BOTH**, any time an **IN** or a **RST** command is issued, all of the processors that are running are reset. If the option is set to **IN**, then all of the processors reset only when an **IN** command is issued. If a **RST** command is issued, only the processor that is being used is reset and the other ones are left running. If the option is set to **RST**, then all of the processors will reset if a **RST** command is issued. However, if an **IN** command is issued, only the processor that you are using will reset.

Enable Checkstop Interrupt (CHECKSTOP)

CF CHECKSTOP[YES, NO]

Several different signals are multiplexed with the **CHKSTP_OUT** signal on the processor. The **CHKSTP_OUT** pin can be used for other purposes (such as data parity configuration) instead of for the **CHKSTP_OUT** signal, depending on what you need for development. If you do not plan to use this pin for the **CHKSTP_OUT** signal, set this configuration option to **NO**.

External Trigger In (TRGIN)

(Wind River ICE SX only)

CF TRGIN[OFF, LEVELHI, LEVELLO, EDGEHI, EDGELO]

This option sets the trigger input signal sense detection. When activated, **Trigger In** stops the target upon detection. **Trigger In** does not work with any events.

The following table describes the available settings for this option.

Table 5-1 **Trigger In Settings**

Setting	Description
OFF	Trigger signal detection is off.
LEVELHI	The trigger input level is set to a value of 1.8 volts or higher.

Table 5-1 **Trigger In Settings**

Setting	Description
LEVELLO	The trigger input level is set below 1.8 volts.
EDGEHI	Configures the system to trigger on the rising edge of a pulse.
EDGELO	Configures the system to trigger on the falling edge of a pulse.

External Trigger Out (TRGOUT)

(Wind River ICE SX only)

CF TRGOUT[LEVELHI, LEVELLO, PULSEHI, PULSELO]

This option allows you to set the trigger output signal type and level. The following table describes the available settings for this option.

Table 5-2 **Trigger Out Settings**

Setting	Description
LEVELHI	The trigger output level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger output level is set below 1.8 volts.
PULSEHI	Trigger Out signal pin will be a pulse from LOW to HIGH and back to LOW when triggered.
PULSELO	Trigger Out signal pin will be a pulse from HIGH to LOW and back to HIGH when triggered.

Invalidate Instruction Cache on GO (INVCI)

CF INVCI[YES,NO]

This option controls whether the contents of the target processor's Instruction Cache are invalidated when you issue a **GO** command. Setting this option to **YES** causes the cache contents to be invalidated.

Issue an IN on Coldstart (INCOLD)

CF INCOLD[YES,NO]

This option configures the emulator boot sequence.

Set this option to **YES** to issue an **IN** command, which asserts a reset on the target during a boot sequence.

Set this option to **NO** to issue a **SYNC** command instead of asserting reset on the target. The **SYNC** command does not reset the board. It establishes JTAG communications and captures the current context. This option is best if you want to hot plug the emulator into a running target.

The default is **NO**.

JTAG Clock Rate (MHz) (CLK)

CF CLK[0.025...100, AUTO]

This option configures the rate at which debug commands are clocked to the target. The default setting is **16**.

Load Boot Table on IN (BL)

CF BL [ENABLE, DISABLE]

This option enables or disables the Linux bootline commands.

Little-endian Mode (LENDIAN)

CF LENDIAN[YES,NO]

This configuration value determines whether the debugger treats memory contents as little-endian (bits ordered 0..63) or big-endian (bits ordered 63..0.) This affects display and interpretation of opcodes in the debugger window, as well as the effects of symbolic manipulation of variables. Setting this option to **YES** means that little-endian is used; setting the option to **NO** means that big-endian is used.

Logic Analyzer Trace (LATRACE)

CF LATRACE[NONE, AGILENT, TEKTRONIX]

This configuration option is necessary if you are using a Logic Analyzer for trace acquisition. Configuring and controlling the logic analyzer is dependant upon the manufacturer of the logic analyzer. Current support is available for Agilent and Tektronix solutions only. If you are not using a Logic Analyzer, set this option to **NONE**.

Memory Management Unit Mode (MMU)

CF MMU [ENABLE, DISABLE]

This option enables or disables the Linux memory management unit.

Monitor Target Reset (RST)

CF RST[YES,NO,HALT, RUN]

This function continuously monitors the target reset signal. If a reset occurs, one of the following actions may be taken:

- **YES** - If a target reset occurs it is reported to the user and BDM control is lost.
- **NO** - If a target reset occurs it is ignored. This is normally used if the code contains a reset instruction, which causes a reset to the external hardware, but not reset the core.
- **HALT** - If the reset occurs in this mode the target is trapped at the restart vector.
- **RUN** - If the reset occurs in this mode the target is restarted and BDM control is maintained.

By default, this option is set to **YES**. It should only be changed to **NO** if you have a RESET instruction in your code.

Power On Reset Length N*1ms (PONR)

CF PONR[0..500]

Some target designs implement reset logic that extends the duration of **HRESET** upon power up. This option allows you to specify the duration of the assertion of

the reset signal so that the emulator knows when to expect the target to release the signal. The number specified can be between 0 and 500, and it represents the number of milliseconds to wait.

Processor Mode (MODE)

CF MODE[32,64]

This parameter determines the operational mode of the processor. The processor can run in a 32-bit or a 64-bit memory mode, depending on the implementation on a target. This parameter compensates for the processor mode in memory accesses to ensure that the correct accesses are made for any given command.

Real Time Preservation (RTP)

CF RTP[YES,NO]

When this option is enabled, real-time preservation allows the target to run without the emulator stopping the target inadvertently.

Reset Pulse Length N*1ms (RPL)

CF RPL[1..600]

This configuration option allows you to adjust the duration of the assertion of the HRESET signal on the target board. The number you specify in this option is the number of milliseconds that HRESET is driven active on the target.

Sense Power via HRESET (SPOWER)

CF SPOWER[YES,NO]

This option lets the hardware determine if power is applied to the target by monitoring the HRESET level when it is released. This prevents the hardware from trying to continue the initialization sequence if power is not applied to the target board.

Set Breakpoint (SB)

CF SB[SB,IHBC]

This option remaps traditional software breakpoints to internal hardware breakpoints. It is set to Software Breakpoint (**SB**) by default. Setting it to **IHBC** means that all software breakpoints are translated to internal hardware breakpoints. This option is useful when you are debugging code out of Flash or PROM.

Setting this option to **IHBC** may cause limitations in the number of breakpoints that can be set, depending on the target processor.

Set Work Space (WSPACE)

CF WSPACE[BASE and **SIZE]**

Flash programming requires a small amount of target RAM to program the flash Algorithm. You must tell your emulator where writable RAM is located on your target for this purpose.

As part of the configuration process, the emulator will indicate exactly how much of the RAM workspace is required. Depending on the device family and type, this space is limited to under 2 KB. Note that more memory improves the speed of programming.

To configure the workspace for flash programming the parameters should be entered in Hex, where **BASE** is the start address, and **SIZE** is the minimum bytes of target RAM required, as displayed in the **Flash Programmer** view. This command allocates memory on the target system that is used by the emulator for various functions, including flash programming.

Target CPU (TAR)

CF TAR *target processor*

This option allows you to configure the emulator for the target that you are using. *target processor* is the name of your processor. For example, to configure the emulator for a PowerPC 5200 target, type:

```
CF TAR 5200
```

Target Console Redirection (TGTCONS)

CF TGTCONS [TGTCONS, BDM] (for the Wind River ICE SX)

Wind River Probe

Target Console Redirection is not currently supported for the Wind River Probe. You do not need to set this option.

Wind River ICE SX

BDM -- Use this setting to connect I/O on a target board, using the Transparent Mode Driver, to the target's BDM connector. When **BDM** is selected, the Wind River ICE SX is in Transparent Mode, and all I/O data is redirected to the port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

For this type of connection to work, the target application must be linked to the Transparent Mode Driver. Refer to the *Wind River Workbench On-Chip Debugging Guide: Using the WDB Transparent Mode Driver* for more information.

TGTCONS -- Use this setting to connect a COM port on a target board to the TGTCONS port of a Wind River ICE SX. All I/O data is then redirected to port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

Trap Exception (TRPEXP)

CF TRPEXP[YES, NO, BREAKPOINTONLY]

This option allows you to configure which run time exceptions are trapped. Setting this option to **YES** causes the emulator to trap RST, CHSTP, MCI, ALI, TRE, SEI, LBRK, IBRK, EBRK, and DPI exceptions. Setting it to **NO** causes the emulator not to trap any exceptions other than TRE and SE. Setting the option to **BREAKPOINTONLY** causes the emulator to trap exceptions only when a breakpoint is encountered.

Trigger In Mode (TRGINMODE)

(Wind River ICE SX only)

CF TRGINMODE[AUTO, BOTH]

This option allows users to determine where the trigger input signal sense detection come from when Wind River Trace is being used. When set to **AUTO**, the system automatically detects whether the source of the **TRGIN** is from the Wind River ICE SX or the Wind River Trace. When set to **BOTH**, the system will accept **TRGIN**s from both Wind River ICE SX and Wind River Trace. By default, this option is set to **AUTO**.

Trigger in Filter Mode (TRGINFILTER)

(Wind River ICE SX only)

CF TRGINFILTER[OFF,ON]

This option provides a filtering option for the Trigger In function. When set to **ON**, a detected signal is required for at least 2 clock periods, or 40ns. This option ensures that noise does not cause a trigger.

Trigger In Report Mode (BRKREP)

(Wind River ICE SX only)

CF BRKREP [REPONLY, BRKREP]

When this option is set to **BRKREP**, which is the default setting, a Trigger In signal will be reported and set a breakpoint. When set to **REPONLY**, a Trigger in signal will be reported, but will not set a breakpoint.

Trigger Out Mode (TRGOUTMODE)

(Wind River ICE SX only)

CF TRGOUTMODE[OFF, ONALLSTOPS, ONBREAKPOINT]

This option allows you to set the type of events that will cause a trigger output to occur.

OFF -- Trigger output is off.

ONALLSTOPS -- Triggers whenever the target stops running.

ONBREAKPOINT -- Triggers whenever a breakpoint is encountered.

Vector Table Location (VECTOR)

CF VECTOR[HIGH, LOW, IGNORE]

This command specifies the location of the exception vector that is used by the software breakpoints. Please note that this setting must match the MSR register setting for software breakpoints to function correctly.

6

PowerPC 55xx Processors

This chapter describes the CF options that are available for PowerPC 55xx processors.

Not all of these CF options apply to all target processors; in general, only applicable options will be visible for any given processor. Which options are visible also depends on whether you are using a Wind River Probe or Wind River ICE SX.

CPU Reset Type (RESET)

CF RESET[HRESET, SRESET, HRESET_UNFILTER, SRESET_UNFILTER]

This option allows you to generate either a **HRESET** or a **SRESET** signal when an **IN** or **INN** command is issued. Selecting **HRESET_UNFILTER** or **SRESET_UNFILTER** means that the reset signal is not sampled when an **IN** or **INN** command is issued.

Delay After Reset N*1ms (DRST)

CF DRST[0..6000]

This option allows you to modify the delay after the release of **HRESET**. Delay can be set in milliseconds, from 0 to 6000. The default is 100.

Download Mode (DLD)

CF DLD[NORMAL,8, 32]

This parameter controls the size of memory transfers when downloading code. Set this option to the width of the memory that you are planning to download your code to. Setting the option to **NORMAL** means that the bus width is 64 bits; **8** means that the bus width is 8 bits; and **32** means that the bus width is 32 bits.

Drive TReset Line (TRESET)

CF TRESET[OPENC, ACTIVE]

This parameter controls the logic applied to the **TRESET** signal on the target. Selecting **OPENC** uses an **open collector** approach in which the active driver is released by tri-stating the line and allowing conditioning resistors on the target to return the signal to the non-active state. Selecting **ACTIVE** in this option causes the emulator to drive the **TRESET** signal to both active and inactive states. This is sometimes required on targets in which the conditioning resistors cause excessive rise or fall time on the signal when returning to an inactive state. This excessive time can cause the processor to come out of reset in an incorrect state.

Emulator HRESET Command Control (CMDRST)

(Wind River ICE SX only)

CF CMDRST[IN,RST,BOTH]

This configuration option is used for multicore debugging, and is used to define when the HRESET line is asserted during a reset. If the option is set to **BOTH**, any time an **IN** or a **RST** command is issued, all of the processors that are running are reset. If the option is set to **IN**, then all of the processors reset only when an **IN** command is issued. If a **RST** command is issued, only the processor that is being used is reset and the other ones are left running. If the option is set to **RST**, then all of the processors will reset if a **RST** command is issued. However, if an **IN** command is issued, only the processor that you are using will reset.

Emulator HRESET Control (HRESET)

CF HRESET[ENABLE, DISABLE]

This option determines whether the **HRESET** line is asserted when you issue an **IN** command. Selecting **ENABLE** asserts **HRESET**, and selecting **DISABLE** prevents **HRESET** from being asserted.

Enable Checkstop Interrupt (CHECKSTOP)

CF CHECKSTOP[YES, NO]

Several different signals are multiplexed with the **CHKSTP_OUT** signal on the processor. The **CHKSTP_OUT** pin can be used for other purposes (such as data parity configuration) instead of for the **CHKSTP_OUT** signal, depending on what you need for development. If you do not plan to use this pin for the **CHKSTP_OUT** signal, set this configuration option to **NO**.

The 8260 processor has multiplexed several different signals with the **CHKSTP_OUT** on the package. If the application uses any of the other possible configurations, then this option needs to be set to **NO** to prevent the firmware from trapping the transitions of the signal as memory bus errors when the real indication is something else. Setting this option to **YES** causes the hardware to trap the assertion of this signal as a memory bus error.

External Trigger In (TRGIN)

(Wind River ICE SX only)

CF TRGIN[OFF, LEVELHI, LEVELLO, EDGEHI, EDGELO]

This option sets the trigger input signal sense detection. When activated, **Trigger In** stops the target upon detection. **Trigger In** does not work with any events.

The following table describes the available settings for this option.

Table 6-1 **Trigger In Settings**

Setting	Description
OFF	Trigger signal detection is off.
LEVELHI	The trigger input level is set to a value of 1.8 volts or higher.

Table 6-1 **Trigger In Settings**

Setting	Description
LEVELLO	The trigger input level is set below 1.8 volts.
EDGEHI	Configures the system to trigger on the rising edge of a pulse.
EDGELO	Configures the system to trigger on the falling edge of a pulse.

External Trigger Out (TRGOUT)

(Wind River ICE SX only)

CF TRGOUT[LEVELHI, LEVELLO, PULSEHI, PULSELO]

This option allows you to set the trigger output signal type and level. The following table describes the available settings for this option.

Table 6-2 **Trigger Out Settings**

Setting	Description
LEVELHI	The trigger output level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger output level is set below 1.8 volts.
PULSEHI	Trigger Out signal pin will be a pulse from LOW to HIGH and back to LOW when triggered.
PULSELO	Trigger Out signal pin will be a pulse from HIGH to LOW and back to HIGH when triggered.

Issue an IN on Coldstart (INCOLD)

CF INCOLD [YES,NO]

This option configures the emulator boot sequence.

Set this option to **YES** to issue an **IN** command, which asserts a reset on the target during a boot sequence.

Set this option to **NO** to issue a **SYNC** command instead of asserting reset on the target. The **SYNC** command does not reset the board. It establishes JTAG communications and captures the current context. This option is best if you want to hot plug the emulator into a running target.

The default is **NO**.

JTAG Clock Rate (MHz) (CLK)

CF CLK *value*

This option configures the rate at which debug commands are clocked to the target.

The available range of value depends on which emulator you are using. For the Wind River Probe, the range is [0.025...100]. For the Wind River ICE SX, the range is [0.025,0.3,0.5,1,3,6,12,16].

The default setting is **16**.

Little-endian Mode (LENDIAN)

CF LENDIAN[YES,NO]

This configuration value determines whether the debugger treats memory contents as little-endian (bits ordered 0..63) or big-endian (bits ordered 63..0.) This affects display and interpretation of opcodes in the debugger window, as well as the effects of symbolic manipulation of variables. Setting this option to **YES** means that little-endian is used; setting the option to **NO** means that big-endian is used.

Load Boot Table on IN (BL)

CF BL [ENABLE, DISABLE]

This option enables or disables the Linux bootline commands.

MMU Support Control (MMU)

CF MMU [ENABLE, DISABLE]

This option enables or disables the Linux memory management unit. It is set to **DISABLE** by default.

Monitor Target Reset (RST)

CF RST[YES,NO,HALT, RUN]

This function continuously monitors the target reset signal. If a reset occurs, one of the following actions may be taken:

- **YES** - If a target reset occurs it is reported to the user and BDM control is lost.
- **NO** - If a target reset occurs it is ignored. This is normally used if the code contains a reset instruction, which causes a reset to the external hardware, but not reset the core.
- **HALT** - If the reset occurs in this mode the target is trapped at the restart vector.
- **RUN** - If the reset occurs in this mode the target is restarted and BDM control is maintained.

By default, this option is set to **YES**. It should only be changed to **NO** if you have a RESET instruction in your code.

Power On Reset Length N*1ms (PONR)

CF PONR[0..500]

Some target designs implement reset logic that extends the duration of **HRESET** upon power up. This option allows you to specify the duration of the assertion of the reset signal so that the emulator knows when to expect the target to release the signal. The number specified can be between 0 and 500, and it represents the number of milliseconds to wait.

Real Time Preservation (RTP)

CF RTP[YES,NO]

When this option is enabled, real-time preservation allows the target to run without the emulator stopping the target inadvertently.

Reset Pulse Length N*1ms (RPL)

CF RPL[1..6000]

This configuration option allows you to adjust the duration of the assertion of the HRESET signal on the target board. The number you specify in this option is the number of milliseconds that HRESET is driven active on the target. The default is 1.

Sense Power via HRESET (SPOWER)

CF SPOWER[YES,NO]

This option lets the hardware determine if power is applied to the target by monitoring the HRESET level when it is released. This prevents the hardware from trying to continue the initialization sequence if power is not applied to the target board.

Set Breakpoint (SB)

CF SB[SB,IHBC]

This option remaps traditional software breakpoints to internal hardware breakpoints. It is set to Software Breakpoint (**SB**) by default. Setting it to **IHBC** means that all software breakpoints are translated to internal hardware breakpoints. This option is useful when you are debugging code out of Flash or PROM.

Setting this option to **IHBC** may cause limitations in the number of breakpoints that can be set, depending on the target processor.

Set Work Space (WSPACE)

CF WSPACE[BASE and **SIZE]**

Flash programming requires a small amount of target RAM to program the flash algorithm. You must tell your emulator where writable RAM is located on your target for this purpose.

As part of the configuration process, the emulator will indicate exactly how much of the RAM workspace is required. Depending on the device family and type, this space is limited to under 2 KB. Note that more memory improves the speed of programming.

To configure the workspace for flash programming the parameters should be entered in hex, where **BASE** is the start address, and **SIZE** is the minimum bytes of target RAM required, as displayed in the **Flash Programmer** view. This command allocates memory on the target system that is used by the emulator for various functions, including flash programming.

Target CPU (TAR)

CF TAR *target_processor*

This option allows you to configure the emulator for the target that you are using. *target_processor* is the name of your processor. For example, to configure the emulator for a PowerPC 5554 target, type:

```
CF TAR 5554
```

Target Console Redirection (TGTCONS)

CF TGTCONS [**TGTCONS**, **BDM**] (for the Wind River ICE SX)

Wind River Probe

Target Console Redirection is not currently supported for the Wind River Probe. You do not need to set this option.

Wind River ICE SX

BDM -- Use this setting to connect I/O on a target board, using the Transparent Mode Driver, to the target's BDM connector. When **BDM** is selected, the Wind River ICE SX is in Transparent Mode, and all I/O data is redirected to the port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

For this type of connection to work, the target application must be linked to the Transparent Mode Driver. Refer to the *Wind River Workbench On-Chip Debugging Guide: Using the WDB Transparent Mode Driver* for more information.

TGTCONS -- Use this setting to connect a COM port on a target board to the TGTCONS port of a Wind River ICE SX. All I/O data is then redirected to port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

TMD Mode (TMD)

CF TMD[ENABLE, DISABLE]

This command sets all of the configuration parameters that are required to use the Transparent Mode Driver (TMD). Select **ENABLE** to configure your system for use with the TMD, and **DISABLE** if you do not plan to use it.

Trap Exception (TRPEXP)

CF TRPEXP[YES, NO, SOI, BREAKPOINTONLY]

This option allows you to configure which run time exceptions are trapped. Setting this option to **YES** causes the emulator to trap RST, CHSTP, MCI, ALI, TRE, SEI, LBRK, IBRK, EBRK, and DPI exceptions. Setting it to **NO** causes the emulator not to trap any exceptions other than TRE and SE. Setting the option to **BREAKPOINTONLY** causes the emulator to trap exceptions only when a breakpoint is encountered. Setting the option to Step Over Interrupt (**SOI**) has the same characteristics as the **YES** option, except that while stepping, the emulator checks each step to see if it has stepped into an exception service routine. If so, it determines what line of code caused the exception and allows the processor to run through the exception and back to the next instruction to be stepped. Please refer to your processor documentation for actual bit position definitions.

Trigger in Filter Mode (TRGINFILTER)

(Wind River ICE SX only)

CF TRGINFILTER[OFF,ON]

This option provides a filtering option for the Trigger In function. When set to **ON**, a detected signal is required for at least 2 clock periods, or 40ns. This option ensures that noise does not cause a trigger.

TTrigger Out Mode (TRGOUTMODE)

(Wind River ICE SX only)

CF TRGOUTMODE[OFF, ONALLSTOPS, ONBREAKPOINT]

This option allows you to set the type of events that will cause a trigger output to occur.

OFF -- Trigger output is off.

ONALLSTOPS -- Triggers whenever the target stops running.

ONBREAKPOINT -- Triggers whenever a breakpoint is encountered.

7

PowerPC 6xx Processors

This chapter describes the configuration options available for PowerPC 6xx processors.

Not all of these CF options apply to all target processors; in general, only applicable options will be visible for any given processor. Which options are visible also depends on whether you are using a Wind River Probe or Wind River ICE SX.

CPU Reset Type (RESET)

CF RESET[HRESET, SRESET, HRESET_UNFILTER, SRESET_UNFILTER]

This option allows you to generate either a **HRESET** or a **SRESET** signal when an **IN** or **INN** command is issued. Selecting **HRESET_UNFILTER** or **SRESET_UNFILTER** means that the reset signal is not sampled when an **IN** or **INN** command is issued.

Data Parity Checking (PAR)

CF PAR[YES, NO]

This configuration option controls the generation of parity for data writes to memory as well as the validation of parity when reading from memory. Some targets do not support parity memory. If your target does not, set this option to **NO**; if it does support parity memory set it to **YES**.

Delay After Reset (DRST)

CF DRST[0..100]

This option allows you to modify the delay after the release of **HRESET**. Delay can be set in milliseconds, from 0 to 100.

Download Mode (DLD)

CF DLD[NORMAL,8]

This parameter controls the size of memory transfers when downloading code. Set this option to the width of the memory that you are planning to download your code to. Setting the option to **NORMAL** means that the bus width is 64 bits, and **8** means that the bus width is 8 bits.

Drive TReset Line (TRESET)

CF TRESET[OPENC, ACTIVE]

This parameter controls the logic applied to the **TRESET** signal on the target. Selecting **OPENC** uses an **open collector** approach in which the active driver is released by tri-stating the line and allowing conditioning resistors on the target to return the signal to the non-active state. Selecting **ACTIVE** in this option causes the emulator to drive the **TRESET** signal to both active and inactive states. This is sometimes required on targets in which the conditioning resistors cause excessive rise or fall time on the signal when returning to an inactive state. This excessive time can cause the processor to come out of reset in an incorrect state.

Emulator HRESET Command Control (CMDRST)

(Wind River ICE SX only)

CF CMDRST[IN,RST,BOTH]

This configuration option is used for multi-core debugging, and is used to define when the HRESET line is asserted during a reset. If the option is set to **BOTH**, any time an **IN** or a **RST** command is issued, all of the processors that are running are reset. If the option is set to **IN**, then all of the processors reset only when an **IN** command is issued. If a **RST** command is issued, only the processor that is being used is reset and the other ones are left running. If the option is set to **RST**, then all

of the processors will reset if a **RST** command is issued. However, if an **IN** command is issued, only the processor that you are using will reset.

Emulator HRESET Control (HRESET)

CF HRESET[ENABLE, DISABLE]

This option determines whether the **HRESET** line is asserted when you issue an **IN** command. Selecting **ENABLE** asserts **HRESET**, and selecting **DISABLE** prevents **HRESET** from being asserted.

External Trigger In (TRGIN)

CF TRGIN[OFF, LEVELHI, LEVELLO, EDGEHI, EDGELO]

This option sets the trigger input signal sense detection. When activated, **Trigger In** stops the target upon detection. **Trigger In** does not work with any events.

The following table describes the available settings for this option.

Table 7-1 **Trigger In Settings**

Setting	Description
OFF	Trigger signal detection is off.
LEVELHI	The trigger input level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger input level is set below 1.8 volts.
EDGEHI	Configures the system to trigger on the rising edge of a pulse.
EDGELO	Configures the system to trigger on the falling edge of a pulse.

External Trigger Out (TRGOUT)

CF TRGOUT[LEVELHI, LEVELLO, PULSEHI, PULSELO]

This option allows you to set the trigger output signal type and level. The following table describes the available settings for this option.

Table 7-2 **Trigger Out Settings**

Setting	Description
LEVELHI	The trigger output level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger output level is set below 1.8 volts.
PULSEHI	Trigger Out signal pin will be a pulse from LOW to HIGH and back to LOW when triggered.
PULSELO	Trigger Out signal pin will be a pulse from HIGH to LOW and back to HIGH when triggered.

Invalidate Instruction Cache on GO (INVCI)

CF INVCI[YES,NO]

This option controls whether the contents of the target processor's Instruction Cache are invalidated when you issue a **GO** command. Setting this option to **YES** causes the cache contents to be invalidated.

Issue an IN on Cold Start (INCOLD)

CF INCOLD[YES,NO]

This option configures the emulator boot sequence.

Set this option to **YES** to issue an **IN** command, which asserts a reset on the target during a boot sequence.

Set this option to **NO** to issue a **SYNC** command instead of asserting reset on the target. The **SYNC** command does not reset the board. It establishes JTAG communications and captures the current context. This option is best if you want to hot plug the emulator into a running target.

The default is **NO**.

JTAG Clock Rate (MHz) (CLK)

CF CLK[0.025...100, AUTO]

This option configures the rate at which debug commands are clocked to the target. The default setting is **16**.

Little-endian Mode (LENDIAN)

CF LENDIAN[YES,NO]

This configuration value determines whether the debugger treats memory contents as little-endian (bits ordered 0..63) or big-endian (bits ordered 63..0.) This affects display and interpretation of opcodes in the debugger window, as well as the effects of symbolic manipulation of variables. Set this option to **YES** to use little-endian; set the option to **NO** to use big-endian.

Load Boot Table on IN (BL)

CF BL [ENABLE, DISABLE]

This option enables or disables the Linux bootline commands.

Logic Analyzer Trace (LATRACE)

CF LATRACE[NONE, AGILENT, TEKTRONIX]

This configuration option is necessary if you are using a Logic Analyzer for trace acquisition. Configuring and controlling the Logic Analyzer is dependant upon the manufacturer of the logic analyzer. Current support is available for Agilent and Tektronix solutions only. If you are not using a Logic Analyzer, set this option to **NONE**.

Memory Management Unit Mode (MMU)

CF MMU [ENABLE, DISABLE]

This option enables or disables the Linux memory management unit.

Monitor Target Reset (RST)

CF RST[YES,NO,RUN,HALT]

This function continuously monitors the target reset signal. If a reset occurs, one of the following actions may be taken:

- **YES** - If a target reset occurs it is reported to the user and BDM control is lost.
- **NO** - If a target reset occurs it is ignored. This is normally used if the code contains a reset instruction, which causes a reset to the external hardware, but not reset the core.
- **HALT** - If the reset occurs in this mode the target is trapped at the restart vector.
- **RUN** - If the reset occurs in this mode the target is restarted and BDM control is maintained.

By default, this option is set to **YES**. It should only be changed to **NO** if you have a RESET instruction in your code.

Power On Reset Length N*1ms (PONR)

CF PONR[0..500]

Some target designs implement reset logic that extends the duration of **HRESET** upon power up. This option allows you to specify the duration of the assertion of the reset signal so that the emulator knows when to expect the target to release the signal. The number specified can be between 0 and 500, and it represents the number of milliseconds to wait.

Processor Mode (MODE)

CF MODE[32,64]

This parameter determines the operational mode of the processor. The processor can run in a 32-bit or a 64-bit memory mode, depending on the implementation on a target. This parameter compensates for the processor mode in memory accesses to ensure that the correct accesses are made for any given command.

Real Time Preservation (RTP)

CF RTP[YES,NO]

When this option is enabled, real-time preservation allows the target to run without the emulator stopping the target inadvertently.

Reset Pulse Length (RPL)

CF RPL[1..600]

This configuration option allows you to adjust the duration of the assertion of the HRESET signal on the target board. The number you specify in this option is the number of milliseconds that HRESET is driven active on the target.

Sense Power via HRESET (SPOWER)

CF SPOWER[YES,NO]

This option lets the hardware determine if power is applied to the target by monitoring the HRESET level when it is released. This prevents the hardware from trying to continue the initialization sequence if power is not applied to the target board.

Set Breakpoint (SB)

CF SB[SB,IHBC]

This option remaps traditional software breakpoints to internal hardware breakpoints. It is set to Software Breakpoint (**SB**) by default. Setting it to **IHBC** means that all software breakpoints are translated to internal hardware breakpoints. This option is useful when you are debugging code out of Flash or PROM.

Setting this option to **IHBC** may cause limitations in the number of breakpoints that can be set, depending on the target processor.

Set Stack Range (STACK)

CF STACK[OFF/Lower and **Upper]**

This setting is **OFF** by default. When stack limits are set, it prevents the emulator from walking through the stack, past the specified range, and causing accidental bus errors.

Set Work Space (WSPACE)

CF WSPACE[BASE and **SIZE]**

Flash programming requires a small amount of target RAM to program the flash algorithm. You must tell your emulator where writable RAM is located on your target for this purpose.

As part of the configuration process, the emulator will indicate exactly how much of the RAM workspace is required. Depending on the device family and type, this space is limited to under 2 KB. Note that more memory improves the speed of programming.

To configure the workspace for flash programming the parameters should be entered in hex, where **BASE** is the start address, and **SIZE** is the minimum bytes of target RAM required, as displayed in the **Flash Programmer** view. This command allocates memory on the target system that is used by the emulator for various functions, including flash programming.

Target Console Redirection (TGTCONS)

CF TGTCONS [TGTCONS, BDM] (for the Wind River ICE SX)

Wind River Probe

Target Console Redirection is not currently supported for the Wind River Probe. You do not need to set this option.

Wind River ICE SX

BDM -- Use this setting to connect I/O on a target board, using the Transparent Mode Driver, to the target's BDM connector. When **BDM** is selected, the Wind River ICE SX is in Transparent Mode, and all I/O data is redirected to the port 1237 of the Wind River ICE SX's IP address. You can then read and write the

I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

For this type of connection to work, the target application must be linked to the Transparent Mode Driver. Refer to the *Wind River Workbench On-Chip Debugging Guide: Using the WDB Transparent Mode Driver* for more information.

TGTCONS -- Use this setting to connect a COM port on a target board to the TGTCONS port of a Wind River ICE SX. All I/O data is then redirected to port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

Target CPU (TAR)

CF TAR *target processor*

This option allows you to configure the emulator for the target that you are using. *target processor* is the name of your processor. For example, to configure the emulator for a PowerPC 603P target, type:

```
CF TAR 603P
```

TMD Mode (TMD)

CF TMD[ENABLE, DISABLE]

This command sets all of the configuration parameters that are required to use the Transparent Mode Driver (TMD). Select **ENABLE** to configure your system for use with the TMD, and **DISABLE** if you do not plan to use it.

Trap Exception (TRPEXP)

CF TRPEXP[YES, NO, SOI, BREAKPOINTONLY]

This option allows you to configure which run time exceptions are trapped. Setting this option to **YES** causes the emulator to trap RST, CHSTP, MCI, ALI, TRE, SEI, LBRK, IBRK, EBRK, and DPI exceptions. Setting it to **NO** causes the emulator not to trap any exceptions other than TRE and SE. Setting the option to **BREAKPOINTONLY** causes the emulator to trap exceptions only when a breakpoint is encountered. Setting the option to Step Over Interrupt (**SOI**) has the same characteristics as the **YES** option, except that while stepping, the emulator

checks each step to see if it has stepped into an exception service routine. If so, it determines what line of code caused the exception and allows the processor to run through the exception and back to the next instruction to be stepped. Please refer to your processor documentation for actual bit position definitions.

Trigger in Filter Mode (TRGINFILTER)

CF TRGINFILTER[OFF,ON]

This option provides a filtering option for the Trigger In function. When set to **ON**, a detected signal is required for at least 2 clock periods, or 40ns. This option ensures that noise does not cause a trigger.

Trigger In Report Mode (BRKREP)

CF BRKREP [REPONLY, BRKREP]

When this option is set to **BRKREP**, which is the default setting, a Trigger In signal will be reported and set a breakpoint. When set to **REPONLY**, a Trigger in signal will be reported, but will not set a breakpoint.

Trigger Out Mode (TRGOUTMODE)

CF TRGOUTMODE[OFF, ONALLSTOPS, ONBREAKPOINT]

This option allows you to set the type of events that will cause a trigger output to occur.

OFF -- Trigger output is off.

ONALLSTOPS -- Triggers whenever the target stops running.

ONBREAKPOINT -- Triggers whenever a breakpoint is encountered.

Vector Table Location VECTOR)

CF VECTOR[HIGH, LOW, IGNORE]

This command specifies the location of the exception vector that is used by the software breakpoints. Please note that this setting must match the MSR register setting for software breakpoints to function correctly.

8

PowerPC 7xx Processors

This chapter describes the CF options that are available for PowerPC 7xx processors.

Not all of these CF options apply to all target processors; in general, only applicable options will be visible for any given processor. Which options are visible also depends on whether you are using a Wind River Probe or Wind River ICE SX.

Application IMMR Exclusion Range (AIMMRER)

CF AIMMRER[OFF, START STOP]

This option is only valid if you have an 8260 processor configured in Slave mode. If the application changes the IMMR during initialization from the reset IMMR value to the value contained in AIMMRVAL, the firmware still needs to be able to access the initialization code using the reset IMMR and then change to the new IMMR after it has been remapped. The **START STOP** option is the start and ending addresses of the code range in which the reset IMMR is still active. The following example illustrates the two ways that this command can be used.

```
CF AIMMRER OFF
CF AIMMRER FFF00100 FFF00300
```

Application IMMR Value (AIMMRVAL)

CF AIMMRVAL[*Hex_value*]

This option is only valid if you have a processor configured in Slave mode. If the application changes the IMMR from the reset value during execution, this value points the firmware to the correct memory location to retrieve the internal memory mapped registers. The value is only used if the current Program Counter value does not fall into the AIMMRER region.

CPU Reset Type (RESET)

CF RESET[**HRESET**, **SRESET**, **HRESET_UNFILTER**, **SRESET_UNFILTER**]

This option allows you to generate either a **HRESET** or a **SRESET** signal when an **IN** or **INN** command is issued. Selecting **HRESET_UNFILTER** or **SRESET_UNFILTER** means that the reset signal is not sampled when an **IN** or **INN** command is issued.

Data Parity Checking (PAR)

CF PAR[**YES**, **NO**]

This configuration option controls the generation of parity for data writes to memory as well as the validation of parity when reading from memory. Some targets do not support parity memory. If your target does not, set this option to **NO**; if it does support parity memory set it to **YES**.

Delay After Reset N*1ms (DRST)

CF DRST[**0..100**]

This option allows you to modify the delay after the release of **HRESET**. Delay can be set in milliseconds, from 0 to 100.

Display L2 Data Cache Warning (L2WARNING)

CF L2WARNING[**YES**,**NO**]

This option can display a warning when you try to read a value from data that has been stored in the L2 cache on your target. When set to **YES**, the warning displays

and the memory value is read from RAM. When set to **NO**, the memory value is read from RAM and no warning is displayed.

Download Mode (DLD)

CF DLD[NORMAL,8]

This parameter controls the size of memory transfers when downloading code. Set this option to the width of the memory that you are planning to download your code to. Setting the option to **NORMAL** means that the bus width is 64 bits, and **8** means that the bus width is 8 bits.

Drive TReset Line (TFRESET)

CF TRESET[OPENC, ACTIVE]

This parameter controls the logic applied to the **TRESET** signal on the target. Selecting **OPENC** uses an **open collector** approach in which the active driver is released by tri-stating the line and allowing conditioning resistors on the target to return the signal to the non-active state. Selecting **ACTIVE** in this option causes the emulator to drive the **TRESET** signal to both active and inactive states. This is sometimes required on targets in which the conditioning resistors cause excessive rise or fall time on the signal when returning to an inactive state. This excessive time can cause the processor to come out of reset in an incorrect state.

Emulator HRESET Command Control (CMDRST)

(Wind River ICE SX only)

CF CMDRST[IN,RST,BOTH]

This configuration option is used for multicore debugging, and is used to define when the HRESET line is asserted during a reset. If the option is set to **BOTH**, any time an **IN** or a **RST** command is issued, all of the processors that are running are reset. If the option is set to **IN**, then all of the processors reset only when an **IN** command is issued. If a **RST** command is issued, only the processor that is being used is reset and the other ones are left running. If the option is set to **RST**, then all of the processors will reset if a **RST** command is issued. However, if an **IN** command is issued, only the processor that you are using will reset.

Emulator HRESET Control (HRESET)

CF HRESET[ENABLE, DISABLE]

This option determines whether the **HRESET** line is asserted when you issue an **IN** command. Selecting **ENABLE** asserts **HRESET**, and selecting **DISABLE** prevents **HRESET** from being asserted.

External Trigger In (TRGIN)

CF TRGIN[OFF, LEVELHI, LEVELLO, EDGEHI, EDGELO]

This option sets the trigger input signal sense detection. When activated, **Trigger In** stops the target upon detection. **Trigger In** does not work with any events.

The following table describes the available settings for this option.

Table 8-1 **Trigger In Settings**

Setting	Description
OFF	Trigger signal detection is off.
LEVELHI	The trigger input level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger input level is set below 1.8 volts.
EDGEHI	Configures the system to trigger on the rising edge of a pulse.
EDGELO	Configures the system to trigger on the falling edge of a pulse.

External Trigger Out (TRGOUT)

CF TRGOUT[LEVELHI, LEVELLO, PULSEHI, PULSELO]

This option allows you to set the trigger output signal type and level. The following table describes the available settings for this option.

Table 8-2 **Trigger Out Settings**

Setting	Description
LEVELHI	The trigger output level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger output level is set below 1.8 volts.
PULSEHI	Trigger Out signal pin will be a pulse from LOW to HIGH and back to LOW when triggered.
PULSELO	Trigger Out signal pin will be a pulse from HIGH to LOW and back to HIGH when triggered.

Invalidate Instruction Cache on GO (INVCI)

CF INVCI[YES,NO]

This option controls whether the contents of the target processor's Instruction Cache are invalidated when you issue a **GO** command. Setting this option to **YES** causes the cache contents to be invalidated.

Issue an IN on Coldstart (INCOLD)

CF INCOLD[YES,NO]

This option configures the emulator boot sequence.

Set this option to **YES** to issue an **IN** command, which asserts a reset on the target during a boot sequence.

Set this option to **NO** to issue a **SYNC** command instead of asserting reset on the target. The **SYNC** command does not reset the board. It establishes JTAG communications and captures the current context. This option is best if you want to hot plug the emulator into a running target.

The default is **NO**.

JTAG Clock Rate (MHz) (CLK)

CF CLK[0.025...100, AUTO]

This option configures the rate at which debug commands are clocked to the target. The default setting is **16**.

Load Boot Table on IN (BL)

CF BL [ENABLE, DISABLE]

This option enables or disables the Linux bootline commands.

Little-endian Mode (LENDIAN)

CF LENDIAN[YES,NO]

This configuration value determines whether the debugger treats memory contents as little-endian (bits ordered 0..63) or big-endian (bits ordered 63..0.) This affects display and interpretation of opcodes in the debugger window, as well as the effects of symbolic manipulation of variables. Set this option to **YES** for little-endian; set the option to **NO** for big-endian.

Logic Analyzer Trace (LATRACE)

CF LATRACE[NONE, AGILENT, TEKTRONIX]

This configuration option is necessary if you are using a Logic Analyzer for trace acquisition. Configuring and controlling the Logic Analyzer is dependant upon the manufacturer of the logic analyzer. Current support is available for Agilent and Tektronix solutions only. If you are not using a Logic Analyzer, set this option to **NONE**.

Memory Management Unit Mode (MMU)

CF MMU [ENABLE, DISABLE]

This option enables or disables the Linux memory management unit.

Monitor Target Reset (RST)

CF RST[YES,NO,HALT, RUN]

This function continuously monitors the target reset signal. If a reset occurs, one of the following actions may be taken:

- **YES** - If a target reset occurs it is reported to the user and BDM control is lost.
- **NO** - If a target reset occurs it is ignored. This is normally used if the code contains a reset instruction, which causes a reset to the external hardware, but not reset the core.
- **HALT** - If the reset occurs in this mode the target is trapped at the restart vector.
- **RUN** - If the reset occurs in this mode the target is restarted and BDM control is maintained.

By default, this option is set to **YES**. It should only be changed to **NO** if you have a RESET instruction in your code.

Power On Reset Length N*1ms (PONR)

CF PONR[0..500]

Some target designs implement reset logic that extends the duration of **HRESET** upon power up. This option allows you to specify the duration of the assertion of the reset signal so that the emulator knows when to expect the target to release the signal. The number specified can be between 0 and 500, and it represents the number of milliseconds to wait.

Processor Mode (MODE)

CF MODE[32,64]

This parameter determines the operational mode of the processor. The processor can run in a 32-bit or a 64-bit memory mode, depending on the implementation on a target. This parameter compensates for the processor mode in memory accesses to ensure that the correct accesses are made for any given command.

Real Time Preservation (RTP)

CF RTP[YES,NO]

When this option is enabled, real-time preservation allows the target to run without the emulator stopping the target inadvertently.

Reset Pulse Length N*1ms (RPL)

CF RPL[1..600]

This configuration option allows you to adjust the duration of the assertion of the HRESET signal on the target board. The number you specify in this option is the number of milliseconds that HRESET is driven active on the target.

Run Counter Length (RCL)

CF RCL[1000..FFFF]

This option specifies the number of clock cycles that the emulator will permit before it gives up waiting for a memory operation to complete. Most memory operations complete in less than 1000 clock cycles, but certain hardware may require wait times that are longer. Set this option to accommodate longer wait times to prevent the emulator from timing out prematurely.

Sense Power via HRESET (SPOWER)

CF SPOWER[YES,NO]

This option lets the hardware determine if power is applied to the target by monitoring the HRESET level when it is released. This prevents the hardware from trying to continue the initialization sequence if power is not applied to the target board.

Set Breakpoint (SB)

CF SB[SB,IHBC]

This option remaps traditional software breakpoints to internal hardware breakpoints. It is set to Software Breakpoint (**SB**) by default. Setting it to **IHBC**

means that all software breakpoints are translated to internal hardware breakpoints. This option is useful when you are debugging code out of Flash or PROM.

Setting this option to **IHBC** may cause limitations in the number of breakpoints that can be set, depending on the target processor.

Set Stack Range (STACK)

CF STACK[OFF / Lower and Upper]

This setting is **OFF** by default. When stack limits are set, it prevents the emulator from walking through the stack, past the specified range, and causing accidental bus errors.

Set Work Space (WSPACE)

CF WSPACE[BASE and **SIZE]**

Flash programming requires a small amount of target RAM to program the flash Algorithm. You must tell your emulator where writable RAM is located on your target for this purpose.

As part of the configuration process, the emulator will indicate exactly how much of the RAM workspace is required. Depending on the device family and type, this space is limited to under 2 KB. Note that more memory improves the speed of programming.

To configure the workspace for flash programming the parameters should be entered in Hex, where **BASE** is the start address, and **SIZE** is the minimum bytes of target RAM required, as displayed in the **Flash Programmer** view. This command allocates memory on the target system that is used by the emulator for various functions, including flash programming.

Slave IMMR Reset Value (SLIMMRVAL)

CF SLIMMRVAL[AUTO, *value*]

This configuration option specifies how the IMMR value for the slave processor is set up, if you select one. Setting this option to **AUTO** means that the emulator tries to automatically detect the value. If you prefer, you can enter a hex *value* for this option.

Target CPU (TAR)

CF TAR *target processor*

This option allows you to configure the emulator for the target that you are using. *target processor* is the name of your processor. For example, to configure the emulator for a PowerPC 750FX target, type:

```
CF TAR 750FX
```

Target CPU (Slave) (SLAVE)

CF SLAVE[NONE,8260]

This configuration option allows the emulator to use the desired scan chain on a master processor, while retaining full access to the IMMR region of the QUICC on the 8260. This maps the 8260 QUICC register sets into another PowerPC processor that does not normally have access to the 8260 peripherals. This includes the ability to initialize the QUICC registers on the 8260 during an **IN** command.

Target Console Redirection (TGTCONS)

CF TGTCONS [TGTCONS, BDM] (for the Wind River ICE SX)

Wind River Probe

Target Console Redirection is not currently supported for the Wind River Probe. You do not need to set this option.

Wind River ICE SX

BDM -- Use this setting to connect I/O on a target board, using the Transparent Mode Driver, to the target's BDM connector. When **BDM** is selected, the Wind River ICE SX is in Transparent Mode, and all I/O data is redirected to the port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

For this type of connection to work, the target application must be linked to the Transparent Mode Driver. Refer to the *Wind River Workbench On-Chip Debugging Guide: Using the WDB Transparent Mode Driver* for more information.

TGTCONS -- Use this setting to connect a COM port on a target board to the TGTCONS port of a Wind River ICE SX. All I/O data is then redirected to port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

TMD Mode (TMD)

CF TMD[ENABLE, DISABLE]

This command sets all of the configuration parameters that are required to use the Transparent Mode Driver (TMD). Select **ENABLE** to configure your system for use with the TMD, and **DISABLE** if you do not plan to use it.

Trap Exception (TRPEXP)

CF TRPEXP[YES, NO, SOI, BREAKPOINTONLY]

This option allows you to configure which run time exceptions are trapped. Setting this option to **YES** causes the emulator to trap RST, CHSTP, MCI, ALI, TRE, SEI, LBRK, IBRK, EBRK, and DPI exceptions. Setting it to **NO** causes the emulator not to trap any exceptions other than TRE and SE. Setting the option to **BREAKPOINTONLY** causes the emulator to trap exceptions only when a breakpoint is encountered. Setting the option to Step Over Interrupt (**SOI**) has the same characteristics as the **YES** option, except that while stepping, the emulator checks each step to see if it has stepped into an exception service routine. If so, it determines what line of code caused the exception and allows the processor to run through the exception and back to the next instruction to be stepped. Please refer to your processor documentation for actual bit position definitions.

Trigger in Filter Mode (TRGINFILTER)

CF TRGINFILTER[OFF,ON]

This option provides a filtering option for the Trigger In function. When set to **ON**, a detected signal is required for at least 2 clock periods, or 40ns. This option ensures that noise does not cause a trigger.

Trigger In Report Mode (BRKREP)

CF BRKREP [REPONLY, BRKREP]

When this option is set to **BRKREP**, which is the default setting, a Trigger In signal will be reported and set a breakpoint. When set to **REPONLY**, a Trigger in signal will be reported, but will not set a breakpoint.

Trigger Out Mode (TRGOUTMODE)

CF TRGOUTMODE[OFF, ONALLSTOPS, ONBREAKPOINT]

This option allows you to set the type of events that will cause a trigger output to occur.

OFF -- Trigger output is off.

ONALLSTOPS -- Triggers whenever the target stops running.

ONBREAKPOINT -- Triggers whenever a breakpoint is encountered.

Vector Table Location (VECTOR)

CF VECTOR[HIGH, LOW, IGNORE]

This command specifies the location of the exception vector that is used by the software breakpoints. Please note that this setting must match the MSR register setting for software breakpoints to function correctly.

9

PowerPC 74xx Processors

This chapter describes the CF options that are available for PowerPC 74xx processors.

Not all of these CF options apply to all target processors; in general, only applicable options will be visible for any given processor. Which options are visible also depends on whether you are using a Wind River Probe or Wind River ICE SX.

The list of available options differs slightly for the MPC7400 and 7410 processors. For example, Data Parity Checking (**CF PAR**) is available on the MPC7400 and MPC7410 but not on other MPC74xx processors. This chapter includes all options available on any MPC74xx processors.

Application IMMR Exclusion Range (AIMMRER)

CF AIMMRER[OFF, START STOP]

This option is only valid if you have an 8260 processor configured in Slave mode. If the application changes the IMMR during initialization from the reset IMMR value to the value contained in AIMMRVAL, the firmware still needs to be able to access the initialization code using the reset IMMR and then change to the new IMMR after it has been remapped. The **START STOP** option is the start and ending addresses of the code range in which the reset IMMR is still active. The following example illustrates the two ways that this command can be used.

```
CF AIMMRER OFF
CF AIMMRER FFF00100 FFF00300
```

Application IMMR Value (AIMMRVAL)

CF AIMMRVAL[*hex_value*]

This configuration option is only valid if you have a processor configured in Slave mode. If the application changes the IMMR from the reset value during execution, this value points the firmware to the correct memory location to retrieve the internal memory mapped registers. The value is only used if the current Program Counter value does not fall into the AIMMRER region.

CPU Reset Type (RESET)

CF RESET[**HRESET**, **SRESET**, **HRESET_UNFILTER**, **SRESET_UNFILTER**]

This option allows you to generate either a **HRESET** or a **SRESET** signal when an **IN** or **INN** command is issued. Selecting **HRESET_UNFILTER** or **SRESET_UNFILTER** means that the reset signal is not sampled when an **IN** or **INN** command is issued.

Data Parity Checking (PAR)

CF PAR[**YES**, **NO**]

This configuration option controls the generation of parity for data writes to memory as well as the validation of parity when reading from memory. Some targets do not support parity memory. If your target does not, set this option to **NO**; if it does support parity memory set it to **YES**.

Delay After Reset N*1ms (DRST)

CF DRST[**0..100**]

This option allows you to modify the delay after the release of **HRESET**. Delay can be set in milliseconds, from 0 to 100.

Display L2 Data Cache Warning (L2WARNING)

CF L2WARNING[**YES**,**NO**]

This option can display a warning when you try to read a value from data that has been stored in the L2 cache on your target. When set to **YES**, the warning displays

and the memory value is read from RAM. When set to **NO**, the memory value is read from RAM and no warning is displayed.

Download Mode (DLD)

CF DLD[BURST,NORMAL,8,32]

This option controls the size of memory transfers when downloading code. Set this option to the width of the memory that you are planning to download your code to. Setting the option to **NORMAL** means that the bus width is 64 bits; **8** means that the bus width is 8 bits; and **32** means that the bus width is 32 bits.

Setting this option to **BURST** writes memory one cache line at a time through the service bus. One cache line is equal to 8 long words (8 * 4 = 32 bytes).

BURST mode is available only for 744x and 745x targets; it does not apply to the MPC7400 or the MPC7410.

Drive TReset Line (TRESET)

CF TRESET[OPENC, ACTIVE]

This parameter controls the logic applied to the **TRESET** signal on the target. Selecting **OPENC** uses an **open collector** approach in which the active driver is released by tri-stating the line and allowing conditioning resistors on the target to return the signal to the non-active state. Selecting **ACTIVE** in this option causes the emulator to drive the **TRESET** signal to both active and inactive states. This is sometimes required on targets in which the conditioning resistors cause excessive rise or fall time on the signal when returning to an inactive state. This excessive time can cause the processor to come out of reset in an incorrect state.

Emulator HRESET Command Control (CMDRST)

(Wind River ICE SX only)

CF CMDRST[IN,RST,BOTH]

This configuration option is used for multicore debugging, and is used to define when the HRESET line is asserted during a reset. If the option is set to **BOTH**, any time an **IN** or a **RST** command is issued, all of the processors that are running are reset. If the option is set to **IN**, then all of the processors reset only when an **IN** command is issued. If a **RST** command is issued, only the processor that is being

used is reset and the other ones are left running. If the option is set to **RST**, then all of the processors will reset if a **RST** command is issued. However, if an **IN** command is issued, only the processor that you are using will reset.

Emulator HRESET Control (HRESET)

CF HRESET[ENABLE, DISABLE]

This option determines whether the **HRESET** line is asserted when you issue an **IN** command. Selecting **ENABLE** asserts **HRESET**, and selecting **DISABLE** prevents **HRESET** from being asserted.

External Trigger In (TRGIN)

(**CF TRGIN[OFF, LEVELHI, LEVELLO, EDGEHI, EDGELO]**

This option sets the trigger input signal sense detection. When activated, **Trigger In** stops the target upon detection. **Trigger In** does not work with any events.

The following table describes the available settings for this option.

Table 9-1 **Trigger In Settings**

Setting	Description
OFF	Trigger signal detection is off.
LEVELHI	The trigger input level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger input level is set below 1.8 volts.
EDGEHI	Configures the system to trigger on the rising edge of a pulse.
EDGELO	Configures the system to trigger on the falling edge of a pulse.

External Trigger Out (TRGOUT)

CF TRGOUT[LEVELHI, LEVELLO, PULSEHI, PULSELO]

This option allows you to set the trigger output signal type and level. The following table describes the available settings for this option.

Table 9-2 **Trigger Out Settings**

Setting	Description
LEVELHI	The trigger output level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger output level is set below 1.8 volts.
PULSEHI	Trigger Out signal pin will be a pulse from LOW to HIGH and back to LOW when triggered.
PULSELO	Trigger Out signal pin will be a pulse from HIGH to LOW and back to HIGH when triggered.

Invalidate Instruction Cache on GO (INVCI)

CF INVCI[YES,NO]

This option controls whether the contents of the target processor's Instruction Cache are invalidated when you issue a **GO** command. Setting this option to **YES** causes the cache contents to be invalidated.

Issue an IN on Cold Start (INCOLD)

CF INCOLD[YES,NO]

This option configures the emulator boot sequence.

Set this option to **YES** to issue an **IN** command, which asserts a reset on the target during a boot sequence.

Set this option to **NO** to issue a **SYNC** command instead of asserting reset on the target. The **SYNC** command does not reset the board. It establishes JTAG communications and captures the current context. This option is best if you want to hot plug the emulator into a running target.

The default is **NO**.

JTAG Clock Rate (MHz) (CLK)

CF CLK[0.025...100, AUTO]

This option configures the rate at which debug commands are clocked to the target. The default setting is **16**.

Little-endian Mode (LENDIAN)

CF LENDIAN[YES,NO]

This configuration value determines whether the debugger treats memory contents as little-endian (bits ordered 0..63) or big-endian (bits ordered 63..0.) This affects display and interpretation of opcodes in the debugger window, as well as the effects of symbolic manipulation of variables. Set this option to **YES** to use little-endian; set the option to **NO** to use big-endian.

Load Boot Table on IN (BL)

CF BL [ENABLE, DISABLE]

This option enables or disables the Linux bootline commands.

Logic Analyzer Trace (LATRACE)

CF LATRACE[NONE, AGILENT, TEKTRONIX]

This configuration option is necessary if you are using a Logic Analyzer for trace acquisition. Configuring and controlling the logic analyzer is dependant upon the manufacturer of the logic analyzer. Current support is available for Agilent and Tektronix solutions only. If you are not using a Logic Analyzer, set this option to **NONE**.

Memory Access Type (MEMTYPE)

CF MEMTYPE[NORMAL,BURST]

This configuration option controls how memory is accessed. When set to **NORMAL**, all memory accesses are done in single beat form using the LSRL scan chain. When set to **BURST**, a data cache line is used to read and write data using a

burst cycle. The burst method is faster, but may not be compatible with all hardware.

Memory Block Access Field (MBA)

CF MBA[0..F]

The address bus for these processors is 36 bits wide. Wind River emulators are designed to communicate with a 32-bit address bus. Use this configuration option to manually specify the first digit of the 9 digit (36 bit) hex number.

MMU Support Control (MMU)

CF MMU[ENABLE, DISABLE]

Use this option to enable or disable Linux Memory Management support.

MMU Support for Internal Hardware Breakpoint (HBRMMU)

CF HBRMMU[ENABLE,DISABLE]

This configuration option allows internal hardware breakpoints to function correctly when MMU is enabled in your application code. When set to **ENABLE**, this option sets up the Translation Enable bit in the Instruction Address Breakpoint register or the Data Address Breakpoint register. The option is disabled by default.

Monitor Target Reset (RST)

CF RST[YES,NO,HALT, RUN]

This function continuously monitors the target reset signal. If a reset occurs, one of the following actions may be taken:

- **YES** - If a target reset occurs it is reported to the user and BDM control is lost.
- **NO** - If a target reset occurs it is ignored. This is normally used if the code contains a reset instruction, which causes a reset to the external hardware, but not reset the core.
- **HALT** - If the reset occurs in this mode the target is trapped at the restart vector.

- **RUN** - If the reset occurs in this mode the target is restarted and BDM control is maintained.

By default, this option is set to **YES**. It should only be changed to **NO** if you have a RESET instruction in your code.

Power On Reset Length N*1ms (PONR)

CF PONR[0..500]

Some target designs implement reset logic that extends the duration of **HRESET** upon power up. This option allows you to specify the duration of the assertion of the reset signal so that the emulator knows when to expect the target to release the signal. The number specified can be between 0 and 500, and it represents the number of milliseconds to wait.

Processor Mode (MODE)

CF MODE[32,64]

This parameter determines the operational mode of the processor. The processor can run in a 32-bit or a 64-bit memory mode, depending on the implementation on a target. This parameter compensates for the processor mode in memory accesses to ensure that the correct accesses are made for any given command.

Real Time Preservation (RTP)

CF RTP[YES,NO]

When this option is enabled, real-time preservation allows the target to run without the emulator stopping the target inadvertently.

Reset Pulse Length N*1ms (RPL)

CF RPL[1..600]

This configuration option allows you to adjust the duration of the assertion of the HRESET signal on the target board. The number you specify in this option is the number of milliseconds that HRESET is driven active on the target.

Run Counter Length (RCL)

CF RCL[1000..FFFF]

This option specifies the number of clock cycles that the emulator will permit before it gives up waiting for a memory operation to complete. Most memory operations complete in less than 1000 clock cycles, but certain hardware may require wait times that are longer. Set this option to accommodate longer wait times to prevent the emulator from timing out prematurely.

Sense Power via HRESET (SPOWER)

CF SPOWER[YES,NO]

This option lets the hardware determine if power is applied to the target by monitoring the HRESET level when it is released. This prevents the hardware from trying to continue the initialization sequence if power is not applied to the target board.

Set Breakpoint (SB)

CF SB[SB,IHBC]

This option remaps traditional software breakpoints to internal hardware breakpoints. It is set to Software Breakpoint (**SB**) by default. Setting it to **IHBC** means that all software breakpoints are translated to internal hardware breakpoints. This option is useful when you are debugging code out of Flash or PROM.

Setting this option to **IHBC** may cause limitations in the number of breakpoints that can be set, depending on the target processor.

Set Stack Range (STACK)

CF STACK[OFF / Lower and Upper]

This setting is **OFF** by default. When stack limits are set, it prevents the emulator from walking through the stack, past the specified range, and causing accidental bus errors.

Set Work Space (WSPACE)

CF WSPACE[**BASE** and **SIZE**]

Flash programming requires a small amount of target RAM to program the flash Algorithm. You must tell your emulator where writable RAM is located on your target for this purpose.

As part of the configuration process, the emulator will indicate exactly how much of the RAM workspace is required. Depending on the device family and type, this space is limited to under 2 KB. Note that more memory improves the speed of programming.

To configure the workspace for flash programming the parameters should be entered in hex, where **BASE** is the start address, and **SIZE** is the minimum bytes of target RAM required, as displayed in the **Flash Programmer** view. This command allocates memory on the target system that is used by the emulator for various functions, including flash programming.

Slave IMMR Reset Value (SLIMMRVAL)

CF SLIMMRVAL[**AUTO**, *value*]

This configuration option specifies how the IMMR value for the slave processor is set up, if you select one. Setting this option to **AUTO** means that the emulator tries to automatically detect the value. If you prefer, you can enter a hex *value* for this option.

Target CPU (TAR)

CF TAR *target processor*

This option allows you to configure the emulator for the target that you are using. *target processor* is the name of your processor. For example, to configure the emulator for a PowerPC 7410 target, type:

```
CF TAR 7410
```

Target CPU (Slave) (SLAVE)

CF SLAVE[NONE,8260]

This configuration option allows the emulator to use the desired scan chain on a master processor, while retaining full access to the IMMR region of the QUICC on the 8260. This maps the 8260 QUICC register sets into another PowerPC processor that does not normally have access to the 8260 peripherals. This includes the ability to initialize the QUICC registers on the 8260 during an **IN** command.

Target Console Redirection (TGTCONS)

CF TGTCONS [TGTCONS, BDM] (for the Wind River ICE SX)

Wind River Probe

Target Console Redirection is not currently supported for the Wind River Probe. You do not need to set this option.

Wind River ICE SX

BDM -- Use this setting to connect I/O on a target board, using the Transparent Mode Driver, to the target's BDM connector. When **BDM** is selected, the Wind River ICE SX is in Transparent Mode, and all I/O data is redirected to the port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

For this type of connection to work, the target application must be linked to the Transparent Mode Driver. Refer to the *Wind River Workbench On-Chip Debugging Guide: Using the WDB Transparent Mode Driver* for more information.

TGTCONS -- Use this setting to connect a COM port on a target board to the TGTCONS port of a Wind River ICE SX. All I/O data is then redirected to port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

TMD Mode (TMD)

CF TMD[ENABLE, DISABLE]

This command sets all of the configuration parameters that are required to use the Transparent Mode Driver (TMD). Select **ENABLE** to configure your system for use with the TMD, and **DISABLE** if you do not plan to use it.

Trap Exception (TRPEXP)

CF TRPEXP[YES, NO, SOI, BREAKPOINTONLY]

This option allows you to configure which run time exceptions are trapped. Setting this option to **YES** causes the emulator to trap RST, CHSTP, MCI, ALI, TRE, SEI, LBRK, IBRK, EBRK, and DPI exceptions. Setting it to **NO** causes the emulator not to trap any exceptions other than TRE and SE. Setting the option to **BREAKPOINTONLY** causes the emulator to trap exceptions only when a breakpoint is encountered. Setting the option to Step Over Interrupt (**SOI**) has the same characteristics as the **YES** option, except that while stepping, the emulator checks each step to see if it has stepped into an exception service routine. If so, it determines what line of code caused the exception and allows the processor to run through the exception and back to the next instruction to be stepped. Please refer to your processor documentation for actual bit position definitions.

Trigger in Filter Mode (TRGINFILTER)

CF TRGINFILTER[OFF,ON]

This option provides a filtering option for the Trigger In function. When set to **ON**, a detected signal is required for at least 2 clock periods, or 40ns. This option ensures that noise does not cause a trigger.

Trigger In Report Mode (BRKREP)

CF BRKREP [REPONLY, BRKREP]

When this option is set to **BRKREP**, which is the default setting, a Trigger In signal will be reported and set a breakpoint. When set to **REPONLY**, a Trigger in signal will be reported, but will not set a breakpoint.

Trigger Out Mode (TRGOUTMODE)

CF TRGOUTMODE[OFF, ONALLSTOPS, ONBREAKPOINT]

This option allows you to set the type of events that will cause a trigger output to occur.

OFF -- Trigger output is off.

ONALLSTOPS -- Triggers whenever the target stops running.

ONBREAKPOINT -- Triggers whenever a breakpoint is encountered.

Vector Table Location (VECTOR)

CF VECTOR[HIGH, LOW, IGNORE]

This command specifies the location of the exception vector that is used by the software breakpoints. Please note that this setting must match the MSR register setting for software breakpoints to function correctly.

10

PowerPC 8xx Processors

This chapter describes the configuration options available for PowerPC 8xx processors.

Not all of these CF options apply to all target processors; in general, only applicable options will be visible for any given processor.

29-31 Bits of ICTRL Register (ICTRLVAL)

CF ICTRLVAL[**0...7**]

Use this option to force the CPU 2 ICTRL Register bits 9-31 on the target processor to a value of **0...7**. This determines extra information cycles emitted onto the external CPU bus.

BDM Clock Rate (CLK)

CF CLK [**0.1, 0.5, 1, 3, 6, 12**]

Use this option to set the BDM clock frequency, in megahertz, that is used for BDM communications. The settings are used to control the **DSCLK** signal frequency on the 26/30 pin BDM connector. For brevity, the settings listed are approximations of the actual frequency. What setting you should use depends on the core frequency of your target processor. The maximum BDM clock frequency is limited to 20 per cent of the core frequency. Generally, the higher the core frequency, the higher the **CLK** parameter setting can be. A little experimenting with this setting will allow you to maximize the BDM communications speed. This is significant for maximizing image download and upload speeds. The default value is **12**.

Enable Target Machine Check (TRPMC)

CF TRPMC[YES, NO]

This option allows the user to configure the emulator to trap machine checks generated by the processor (option set to **YES**) or to allow the trap to be passed to the software exception handler and ignored by the emulator (option set to **NO**.)

External Trigger In (TRGIN)

CF TRGIN[OFF, LEVELHI, LEVELLO, EDGEHI, EDGELO]

This option sets the trigger input signal sense detection. When activated, **Trigger In** stops the target upon detection. **Trigger In** does not work with any events.

The following table describes the available settings for this option.

Table 10-1 **Trigger In Settings**

Setting	Description
OFF	Trigger signal detection is off.
LEVELHI	The trigger input level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger input level is set below 1.8 volts.
EDGEHI	Configures the system to trigger on the rising edge of a pulse.
EDGELO	Configures the system to trigger on the falling edge of a pulse.

External Trigger Out (TRGOUT)

CF TRGOUT[LEVELHI, LEVELLO, PULSEHI, PULSELO]

This option allows you to set the trigger output signal type and level. The following table describes the available settings for this option.

Table 10-2 **Trigger Out Settings**

Setting	Description
LEVELHI	The trigger output level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger output level is set below 1.8 volts.
PULSEHI	Trigger Out signal pin will be a pulse from LOW to HIGH and back to LOW when triggered.
PULSELO	Trigger Out signal pin will be a pulse from HIGH to LOW and back to HIGH when triggered.

Logic Analyzer Trace (LATRACE)

CF LATRACE[NONE, AGILENT, TEKTRONIX]

This configuration option is necessary if you are using a Logic Analyzer for trace acquisition. Configuring and controlling the Logic Analyzer is dependant upon the manufacturer of the logic analyzer. Current support is available for Agilent and Tektronix solutions only. If you are not using a Logic Analyzer, set this option to **NONE**.

Memory Management Unit (MMU)

CF MMU[OFF, LINUX]

Use this option to enable or disable Linux Memory Management support.

Monitor Target Reset (RST)

CF RST[YES, NO, HALT, RUN]

This function continuously monitors the target reset signal. If a reset occurs, one of the following actions may be taken:

- **YES** - If a target reset occurs it is reported to the user and BDM control is lost.
- **NO** - If a target reset occurs it is ignored. This is normally used if the code contains a reset instruction, which causes a reset to the external hardware, but not reset the core.

- **HALT** - If the reset occurs in this mode the target is trapped at the restart vector.
- **RUN** - If the reset occurs in this mode the target is restarted and BDM control is maintained.

By default, this option is set to **YES**. It should only be changed to **NO** if you have a RESET instruction in your code.

Real Time Preservation (RTP)

CF RTP[YES,NO]

When this option is enabled, real-time preservation allows the target to run without the emulator stopping the target inadvertently.

Set Breakpoint (SB)

CF SB[SB,IHBC]

This option remaps traditional software breakpoints to internal hardware breakpoints. It is set to Software Breakpoint (**SB**) by default. Setting it to **IHBC** means that all software breakpoints are translated to internal hardware breakpoints. This option is useful when you are debugging code out of flash or PROM.

Setting this option to **IHBC** may cause limitations in the number of breakpoints that can be set, depending on the target processor.

Set Work Space (WSPACE)

CF WSPACE[BASE and **SIZE]**

Flash programming requires a small amount of target RAM to program the flash algorithm. You must tell your emulator where writable RAM is located on your target for this purpose.

As part of the configuration process, the emulator will indicate exactly how much of the RAM workspace is required. Depending on the device family and type, this space is limited to under 2 KB. Note that more memory improves the speed of programming.

To configure the workspace for flash programming the parameters should be entered in hex, where **BASE** is the start address, and **SIZE** is the minimum bytes of

target RAM required, as displayed in the **Flash Programmer** view. This command allocates memory on the target system that is used by the emulator for various functions, including flash programming.

Software Breakpoint Emulation Method (SBE)

CF SBE [NORMAL, SPECIAL]

This command is used to configure the method that the emulator and the target use to handle software breakpoints. When set to **NORMAL**, which is the default setting, the system assigns the software breakpoints to use the software emulation exception as the method of setting breakpoints. When set to **SPECIAL**, the system assigns the software breakpoints to use a misalignment exception as the method of setting breakpoints. This selection is only necessary if the application being debugged uses software emulation for another purpose.

Stop by INT Retry Count (STOPINTRTRY)

CF STOPINTRTRY[1..30]

Use this option to set the number of times the target will retry after an interrupt occurs. There are eight interrupt sources for PPC8xx processors, not including the Non-Maskable Interrupt (NMI). On PPC8xx processors the interrupt event is non-specific, so any interrupt will be counted, except the NMI, which is not counted. When the number of interrupts reaches the count you set in this option, the target will halt.

Target Console Redirection (TGTCONS)

CF TGTCONS [BDM, TGTCONS]

Use this option to set the target console setting. The default setting is **BDM**. The target console settings are used as follows:

Wind River Probe

Target Console Redirection is not currently supported for the Wind River Probe. You do not need to set this option.

Wind River ICE SX

BDM -- Use this setting to connect I/O on a target board, using the Transparent Mode Driver, to the target's BDM connector. When **BDM** is selected, the Wind River ICE SX is in Transparent Mode, and all I/O data is redirected to the port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

For this type of connection to work, the target application must be linked to the Transparent Mode Driver. Refer to the *Wind River Workbench On-Chip Debugging Guide: Using the WDB Transparent Mode Driver* for more information.

TGTCONS -- Use this setting to connect a COM port on a target board to the TGTCONS port of a Wind River ICE SX. All I/O data is then redirected to port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

Target CPU (TAR)

CF TAR *target_processor*

This option allows you to configure the emulator for the target that you are using. *target_processor* is the name of your processor. For example, to configure the emulator for a PowerPC 860 target, type:

```
CF TAR 860
```

Trap Exception (TRPEXP)

CF TRPEXP[YES, NO, DER]

This option allows you to configure which run time exceptions are trapped. Setting this option to **YES** causes the emulator to trap RST, CHSTP, MCI, ALI, TRE, SEI, LBRK, IBRK, EBRK, and DPI exceptions. Setting it to **NO** causes the emulator not to trap any exceptions other than TRE and SE. Setting the option to **DER** causes the emulator to trap exceptions as masked by the (previously set) DER register.

To set the DER register, enter

SR DER *value*

at the **>BKM>** prompt in the **Terminal** window.

Trigger in Filter Mode (TRGINFILTER)

CF TRGINFILTER[OFF,ON]

This option provides a filtering option for the Trigger In function. When set to **ON**, a detected signal is required for at least 2 clock periods, or 40ns. This option ensures that noise does not cause a trigger.

Trigger In Report Mode (BRKREP)

CF BRKREP [REPONLY, BRKREP]

When this option is set to **BRKREP**, which is the default setting, a Trigger In signal will be reported and set a breakpoint. When set to **REPONLY**, a Trigger in signal will be reported, but will not set a breakpoint.

Trigger Out Mode (TRGOUTMODE)

CF TRGOUTMODE[OFF, ONALLSTOPS, ONBREAKPOINT]

This option allows you to set the type of events that will cause a trigger output to occur.

OFF -- Trigger output is off.

ONALLSTOPS -- Triggers whenever the target stops running.

ONBREAKPOINT -- Triggers whenever a breakpoint is encountered.

Vector Table Location (VECTOR)

CF VECTOR[HIGH, LOW, IGNORE]

This command specifies the location of the exception vector that is used by the software breakpoints. Please note that this setting must match the MSR register setting for software breakpoints to function correctly.

Wait to Enter Background Mode N*100ms (FRZ)

CF FRZ [1...600]

This command sets the length of time that the system waits for the target to enter background mode before it times out. The **FRZ** command can be set between 1 and 600 ms. By default, the option is set to time out after 1 ms. Note that sometimes the response will be slow if the BUS master is an external device. If the timeout period expires, the emulator will report **Time Out Waiting for FREEZE**.

11

PowerPC 82xx Processors

This chapter describes the CF options that are available for PowerPC 82xx processors.

Not all of these CF options apply to all target processors; in general, only applicable options will be visible for any given processor. Which options are visible also depends on whether you are using a Wind River Probe or Wind River ICE SX.

Application IMMR Exclusion Range (AIMMRER)

CF AIMMRER[OFF, START STOP]

This option is only valid if you have an 8260 processor configured in Slave mode. If the application changes the IMMR during initialization from the reset IMMR value to the value contained in AIMMRVAL, the firmware still needs to be able to access the initialization code using the reset IMMR and then change to the new IMMR after it has been remapped. The **START STOP** option is the start and ending addresses of the code range in which the reset IMMR is still active. The following example illustrates the two ways that this command can be used.

```
CF AIMMRER OFF
CF AIMMRER FFF00100 FFF00300
```

Application IMMR Value (AIMMRVAL)

CF AIMMRVAL[*Hex_value*]

This configuration option is only valid if you have a processor configured in Slave mode. If the application changes the IMMR from the reset value during execution,

this value points the firmware to the correct memory location to retrieve the internal memory mapped registers. The value is only used if the current Program Counter value does not fall into the AIMMRER region.

CPU Reset Type (RESET)

CF RESET[HRESET, SRESET, HRESET_UNFILTER, SRESET_UNFILTER]

This option allows you to generate either a **HRESET** or a **SRESET** signal when an **IN** or **INN** command is issued. Selecting **HRESET_UNFILTER** or **SRESET_UNFILTER** means that the reset signal is not sampled when an **IN** or **INN** command is issued.

CPU Type (TAR)

CF TAR *target_processor*

This option allows you to configure the emulator for the target that you are using. *target_processor* is the name of your processor. For example, to configure the emulator for a PowerPC 8260 target, type:

```
CF TAR 8260
```

Delay After Reset N*1ms (DRST)

CF DRST[0..100]

This option allows you to modify the delay after the release of **HRESET**. Delay can be set in milliseconds, from 0 to 100.

Download Mode (DLD)

CF DLD[NORMAL,8, 32]

This parameter controls the size of memory transfers when downloading code. Set this option to the width of the memory that you are planning to download your code to. Setting the option to **NORMAL** means that the bus width is 64 bits; **8** means that the bus width is 8 bits; and **32** means that the bus width is 32 bits.

Drive TReset Line (TRESET)

CF TRESET[OPENC, ACTIVE]

This parameter controls the logic applied to the **TRESET** signal on the target. Selecting **OPENC** uses an **open collector** approach in which the active driver is released by tri-stating the line and allowing conditioning resistors on the target to return the signal to the non-active state. Selecting **ACTIVE** in this option causes the emulator to drive the **TRESET** signal to both active and inactive states. This is sometimes required on targets in which the conditioning resistors cause excessive rise or fall time on the signal when returning to an inactive state. This excessive time can cause the processor to come out of reset in an incorrect state.

Emulator HRESET Command Control (CMDRST)

(Wind River ICE SX only)

CF CMDRST[IN,RST,BOTH]

This configuration option is used for multicore debugging, and is used to define when the HRESET line is asserted during a reset. If the option is set to **BOTH**, any time an **IN** or a **RST** command is issued, all of the processors that are running are reset. If the option is set to **IN**, then all of the processors reset only when an **IN** command is issued. If a **RST** command is issued, only the processor that is being used is reset and the other ones are left running. If the option is set to **RST**, then all of the processors will reset if a **RST** command is issued. However, if an **IN** command is issued, only the processor that you are using will reset.

Emulator HRESET Control (HRESET)

CF HRESET[ENABLE, DISABLE]

This option determines whether the **HRESET** line is asserted when you issue an **IN** command. Selecting **ENABLE** asserts **HRESET**, and selecting **DISABLE** prevents **HRESET** from being asserted.

Enable Checkstop Interrupt (CHECKSTOP)

CF CHECKSTOP[YES, NO]

Several different signals are multiplexed with the **CHKSTP_OUT** signal on the processor. The **CHKSTP_OUT** pin can be used for other purposes (such as data parity configuration) instead of for the **CHKSTP_OUT** signal, depending on what you need for development. If you do not plan to use this pin for the **CHKSTP_OUT** signal, set this configuration option to **NO**.

The 8260 processor has multiplexed several different signals with the **CHKSTP_OUT** on the package. If the application uses any of the other possible configurations, then this option needs to be set to **NO** to prevent the firmware from trapping the transitions of the signal as memory bus errors when the real indication is something else. Setting this option to **YES** causes the hardware to trap the assertion of this signal as a memory bus error.

External Trigger In (TRGIN)

(Wind River ICE SX only)

CF TRGIN[OFF, LEVELHI, LEVELLO, EDGEHI, EDGELO]

This option sets the trigger input signal sense detection. When activated, **Trigger In** stops the target upon detection. **Trigger In** does not work with any events.

The following table describes the available settings for this option.

Table 11-1 **Trigger In Settings**

Setting	Description
OFF	Trigger signal detection is off.
LEVELHI	The trigger input level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger input level is set below 1.8 volts.
EDGEHI	Configures the system to trigger on the rising edge of a pulse.
EDGELO	Configures the system to trigger on the falling edge of a pulse.

External Trigger Out (TRGOUT)

(Wind River ICE SX only)

CF TRGOUT[LEVELHI, LEVELLO, PULSEHI, PULSELO]

This option allows you to set the trigger output signal type and level. The following table describes the available settings for this option.

Table 11-2 **Trigger Out Settings**

Setting	Description
LEVELHI	The trigger output level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger output level is set below 1.8 volts.
PULSEHI	Trigger Out signal pin will be a pulse from LOW to HIGH and back to LOW when triggered.
PULSELO	Trigger Out signal pin will be a pulse from HIGH to LOW and back to HIGH when triggered.

IMMR Base Address Location At Reset (RSTIMMR)

CF RSTIMMR[VALUE,AUTO]

The Internal Memory Mapped Register (IMMR) contains the base address for all of the internal memory mapped registers. This configuration option allows you to change the IMMR value, thus changing the address of the internal memory mapped registers. When set to **AUTO**, the default IMMR value is used. The default value is 0x0F000000.

Invalidate Instruction Cache on GO (INVCI)

CF INVCI[YES,NO]

This option controls whether the contents of the target processor's Instruction Cache are invalidated when you issue a **GO** command. Setting this option to **YES** causes the cache contents to be invalidated.

Issue an IN on Coldstart (INCOLD)

CF INCOLD[YES,NO]

This option configures the emulator boot sequence.

Set this option to **YES** to issue an **IN** command, which asserts a reset on the target during a boot sequence.

Set this option to **NO** to issue a **SYNC** command instead of asserting reset on the target. The **SYNC** command does not reset the board. It establishes JTAG communications and captures the current context. This option is best if you want to hot plug the emulator into a running target.

The default is **NO**.

JTAG Clock Rate (MHz) (CLK)

CF CLK[0.025...100, AUTO]

This option configures the rate at which debug commands are clocked to the target. The default setting is **16**.

Little-endian Mode (LENDIAN)

CF LENDIAN[YES,NO]

This configuration value determines whether the debugger treats memory contents as little-endian (bits ordered 0..63) or big-endian (bits ordered 63..0.) This affects display and interpretation of opcodes in the debugger window, as well as the effects of symbolic manipulation of variables. Setting this option to **YES** means that little-endian is used; setting the option to **NO** means that big-endian is used.

Load Boot Table on IN (BL)

CF BL [ENABLE, DISABLE]

This option enables or disables the Linux bootline commands.

Logic Analyzer Clocking Type (CLKTYPE)

CF CLKTYPE[EXTERNAL,CUSTOM]

This configuration option only applies for Tektronix logic analyzers. If the logic analyzer is supported, it allows you to customize the clock setting. This option is set to **EXTERNAL** by default.

Logic Analyzer Trace (LATRACE)

CF LATRACE[NONE, AGILENT, TEKTRONIX]

This configuration option is necessary if you are using a Logic Analyzer for trace acquisition. Configuring and controlling the logic analyzer is dependant upon the manufacturer of the logic analyzer. Current support is available for Agilent and Tektronix solutions only. If you are not using a Logic Analyzer, set this option to **NONE**.

Memory Management Unit Mode (MMU)

CF MMU [ENABLE, DISABLE]

This option enables or disables the Linux memory management unit.

Monitor Target Reset (RST)

CF RST[YES,NO,HALT, RUN]

This function continuously monitors the target reset signal. If a reset occurs, one of the following actions may be taken:

- **YES** - If a target reset occurs it is reported to the user and BDM control is lost.
- **NO** - If a target reset occurs it is ignored. This is normally used if the code contains a reset instruction, which causes a reset to the external hardware, but not reset the core.
- **HALT** - If the reset occurs in this mode the target is trapped at the restart vector.
- **RUN** - If the reset occurs in this mode the target is restarted and BDM control is maintained.

By default, this option is set to **YES**. It should only be changed to **NO** if you have a RESET instruction in your code.

Power On Reset Length N*1ms (PONR)

CF PONR[0..500]

Some target designs implement reset logic that extends the duration of **HRESET** upon power up. This option allows you to specify the duration of the assertion of the reset signal so that the emulator knows when to expect the target to release the signal. The number specified can be between 0 and 500, and it represents the number of milliseconds to wait.

Processor Mode (MODE)

CF MODE[32,64]

This parameter determines the operational mode of the processor. The processor can run in a 32-bit or a 64-bit memory mode, depending on the implementation on a target. This parameter compensates for the processor mode in memory accesses to ensure that the correct accesses are made for any given command.

Real Time Preservation (RTP)

CF RTP[YES,NO]

When this option is enabled, real-time preservation allows the target to run without the emulator stopping the target inadvertently.

Reset Configuration Word Location (RSTCONF)

CF RSTCONF[AUTO,HIGH,LOW]

The reset configuration word is read by the emulator during initialization to determine the reset IMMR value. When set to **AUTO**, the emulator searches all valid Reset Word locations to find the value.

Reset Pulse Length N*1ms (RPL)

CF RPL[1..600]

This configuration option allows you to adjust the duration of the assertion of the HRESET signal on the target board. The number you specify in this option is the number of milliseconds that HRESET is driven active on the target.

Sense Power via HRESET (SPOWER)

CF SPOWER[YES,NO]

This option lets the hardware determine if power is applied to the target by monitoring the HRESET level when it is released. This prevents the hardware from trying to continue the initialization sequence if power is not applied to the target board.

Set Breakpoint (SB)

CF SB[SB,IHBC]

This option remaps traditional software breakpoints to internal hardware breakpoints. It is set to Software Breakpoint (**SB**) by default. Setting it to **IHBC** means that all software breakpoints are translated to internal hardware breakpoints. This option is useful when you are debugging code out of Flash or PROM.

Setting this option to **IHBC** may cause limitations in the number of breakpoints that can be set, depending on the target processor.

Set Code Range (CR)

CF CR[BASE and **RANGE]**

This option is for use with Wind River Trace. The option is used to specify the base address and size of the memory that is to be used for code storage. By default, the rest of the memory space will be used for data storage.

Set Stack Range (STACK)

CF STACK[OFF / Lower and Upper]

This setting is **OFF** by default. When stack limits are set, it prevents the emulator from walking through the stack, past the specified range, and causing accidental bus errors.

Set Work Space (WSPACE)

CF WSPACE[BASE and **SIZE]**

Flash programming requires a small amount of target RAM to program the flash algorithm. You must tell your emulator where writable RAM is located on your target for this purpose.

As part of the configuration process, the emulator will indicate exactly how much of the RAM workspace is required. Depending on the device family and type, this space is limited to under 2 KB. Note that more memory improves the speed of programming.

To configure the workspace for flash programming the parameters should be entered in hex, where **BASE** is the start address, and **SIZE** is the minimum bytes of target RAM required, as displayed in the **Flash Programmer** view. This command allocates memory on the target system that is used by the emulator for various functions, including flash programming.

Target CPU (SLAVE)

CF SLAVE[NONE,8260]

This configuration option allows the emulator to use the desired scan chain on a master processor, while retaining full access to the IMMR region of the QUICC on the 8260. This maps the 8260 QUICC register sets into another PowerPC processor that does not normally have access to the 8260 peripherals. This includes the ability to initialize the QUICC registers on the 8260 during an **IN** command.

Target Console Redirection (TGTCONS)

CF TGTCONS [TGTCONS, BDM] (for the Wind River ICE SX)

Wind River Probe

Target Console Redirection is not currently supported for the Wind River Probe. You do not need to set this option.

Wind River ICE SX

BDM -- Use this setting to connect I/O on a target board, using the Transparent Mode Driver, to the target's BDM connector. When **BDM** is selected, the Wind River ICE SX is in Transparent Mode, and all I/O data is redirected to the port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

For this type of connection to work, the target application must be linked to the Transparent Mode Driver. Refer to the *Wind River Workbench On-Chip Debugging Guide: Using the WDB Transparent Mode Driver* for more information.

TGTCONS -- Use this setting to connect a COM port on a target board to the TGTCONS port of a Wind River ICE SX. All I/O data is then redirected to port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

TMD Mode (TMD)

CF TMD[ENABLE, DISABLE]

This command sets all of the configuration parameters that are required to use the Transparent Mode Driver (TMD). Select **ENABLE** to configure your system for use with the TMD, and **DISABLE** if you do not plan to use it.

Trap Exception (TRPEXP)

CF TRPEXP[YES, NO, SOI, BREAKPOINTONLY]

This option allows you to configure which run time exceptions are trapped. Setting this option to **YES** causes the emulator to trap RST, CHSTP, MCI, ALI, TRE, SEI, LBRK, IBRK, EBRK, and DPI exceptions. Setting it to **NO** causes the emulator not

to trap any exceptions other than TRE and SE. Setting the option to **BREAKPOINTONLY** causes the emulator to trap exceptions only when a breakpoint is encountered. Setting the option to Step Over Interrupt (**SOI**) has the same characteristics as the **YES** option, except that while stepping, the emulator checks each step to see if it has stepped into an exception service routine. If so, it determines what line of code caused the exception and allows the processor to run through the exception and back to the next instruction to be stepped. Please refer to your processor documentation for actual bit position definitions.

Trigger in Filter Mode (TRGINFILTER)

(Wind River ICE SX only)

CF TRGINFILTER[OFF,ON]

This option provides a filtering option for the Trigger In function. When set to **ON**, a detected signal is required for at least 2 clock periods, or 40ns. This option ensures that noise does not cause a trigger.

Trigger In Report Mode (BRKREP)

(Wind River ICE SX only)

CF BRKREP [REPONLY, BRKREP]

When this option is set to **BRKREP**, which is the default setting, a Trigger In signal will be reported and set a breakpoint. When set to **REPONLY**, a Trigger in signal will be reported, but will not set a breakpoint.

Trigger Out Mode (TRGOUTMODE)

(Wind River ICE SX only)

CF TRGOUTMODE[OFF, ONALLSTOPS, ONBREAKPOINT]

This option allows you to set the type of events that will cause a trigger output to occur.

OFF -- Trigger output is off.

ONALLSTOPS -- Triggers whenever the target stops running.

ONBREAKPOINT -- Triggers whenever a breakpoint is encountered.

Vector Table Location (VECTOR)

CF VECTOR[HIGH, LOW, IGNORE]

This command specifies the location of the exception vector that is used by the software breakpoints. Please note that this setting must match the MSR register setting for software breakpoints to function correctly.

12

PowerPC 83xx Processors

This chapter describes the CF options that are available for PowerPC 83xx processors.

Not all of these CF options apply to all target processors; in general, only applicable options will be visible for any given processor. Which options are visible also depends on whether you are using a Wind River Probe or Wind River ICE SX.

Application IMMR Exclusion Range (AIMMRER)

CF AIMMRER[OFF, *START STOP*]

This option is only valid if you have an 8260 processor configured in Slave mode. If the application changes the IMMR during initialization from the reset IMMR value to the value contained in AIMMRVAL, the firmware still needs to be able to access the initialization code using the reset IMMR and then change to the new IMMR after it has been remapped. The **START STOP** option is the start and ending addresses of the code range in which the reset IMMR is still active. The following example illustrates the two ways that this command can be used.

```
CF AIMMRER OFF
CF AIMMRER FFF00100 FFF00300
```

Application IMMR Value (AIMMRVAL)

CF AIMMRVAL[*Hex_value*]

This configuration option is only valid if you have a processor configured in Slave mode. If the application changes the IMMR from the reset value during execution, this value points the firmware to the correct memory location to retrieve the internal memory mapped registers. The value is only used if the current Program Counter value does not fall into the AIMMRER region.

Configure Reset Configuration Word (RCW)

CF RCW [**NO**, *RCWL* and *RCWH*]

This option allows you to use the JTAG interface to override an existing Reset Configuration Word on your target board. This is useful if, for example, your target board is in Disable Mode by default.

RWCL and *RWCH* are user-assigned 32-bit hex values. *RWCL* (Reset Configuration Word Low) is the lower boundary of the memory address you want to set the Reset Configuration Word to; *RWCH* (Reset Configuration Word High) is the higher boundary.

To override an existing Reset Configuration Word, enter the low and high values in hex, lower value first. You do not need to precede the value with **0x**.

Example:

```
CF RCW 04300000 f460a000
```

This will set the memory address of the Reset Configuration Word, beginning at **0x04300000** and ending at **0xf460a000**.

The default setting is **NO**.

CPU Reset Type (RESET)

CF RESET[HRESET, SRESET, HRESET_UNFILTER, SRESET_UNFILTER]

This option allows you to generate either a **HRESET** or a **SRESET** signal when an **IN** or **INN** command is issued. Selecting **HRESET_UNFILTER** or **SRESET_UNFILTER** means that the reset signal is not sampled when an **IN** or **INN** command is issued.

CPU Type (TAR)

CF TAR *target_processor*

This option allows you to configure the emulator for the target that you are using. *target_processor* is the name of your processor. For example, to configure the emulator for a PowerPC 8343 target, type:

```
CF TAR 8343
```

Delay After Reset N*1ms (DRST)

CF DRST[0..100]

This option allows you to modify the delay after the release of **HRESET**. Delay can be set in milliseconds, from 0 to 100.

Download Mode (DLD)

CF DLD[NORMAL,8, 32]

This parameter controls the size of memory transfers when downloading code. Set this option to the width of the memory that you are planning to download your code to. Setting the option to **NORMAL** means that the bus width is 64 bits; **8** means that the bus width is 8 bits; and **32** means that the bus width is 32 bits.

Drive TReset Line (TRESET)

CF TRESET[OPENC, ACTIVE]

This parameter controls the logic applied to the **TRESET** signal on the target. Selecting **OPENC** uses an **open collector** approach in which the active driver is released by tri-stating the line and allowing conditioning resistors on the target to return the signal to the non-active state. Selecting **ACTIVE** in this option causes the emulator to drive the **TRESET** signal to both active and inactive states. This is sometimes required on targets in which the conditioning resistors cause excessive rise or fall time on the signal when returning to an inactive state. This excessive time can cause the processor to come out of reset in an incorrect state.

Emulator HRESET Command Control (CMDRST)

(Wind River ICE SX only)

CF CMDRST[IN,RST,BOTH]

This configuration option is used for multi-core debugging, and is used to define when the HRESET line is asserted during a reset. If the option is set to **BOTH**, any time an **IN** or a **RST** command is issued, all of the processors that are running are reset. If the option is set to **IN**, then all of the processors reset only when an **IN** command is issued. If a **RST** command is issued, only the processor that is being used is reset and the other ones are left running. If the option is set to **RST**, then all of the processors will reset if a **RST** command is issued. However, if an **IN** command is issued, only the processor that you are using will reset.

Emulator HRESET Control (HRESET)

CF HRESET[ENABLE, DISABLE]

This option determines whether the **HRESET** line is asserted when you issue an **IN** command. Selecting **ENABLE** asserts **HRESET**, and selecting **DISABLE** prevents **HRESET** from being asserted.

Enable CheckStop Interrupt (CHECKSTOP)

CF CHECKSTOP[YES, NO]

Several different signals are multiplexed with the **CHKSTP_OUT** signal on the processor. The **CHKSTP_OUT** pin can be used for other purposes (such as data parity configuration) instead of for the **CHKSTP_OUT** signal, depending on what you need for development. If you do not plan to use this pin for the **CHKSTP_OUT** signal, set this configuration option to **NO**.

The 8260 processor has multiplexed several different signals with the **CHKSTP_OUT** on the package. If the application uses any of the other possible configurations, then this option needs to be set to **NO** to prevent the firmware from trapping the transitions of the signal as memory bus errors when the real indication is something else. Setting this option to **YES** causes the hardware to trap the assertion of this signal as a memory bus error.

External Trigger In (TRGIN)

(Wind River ICE SX only)

CF TRGIN[OFF, LEVELHI, LEVELLO, EDGEHI, EDGELO]

This option sets the trigger input signal sense detection. When activated, **Trigger In** stops the target upon detection. **Trigger In** does not work with any events.

The following table describes the available settings for this option.

Table 12-1 **Trigger In Settings**

Setting	Description
OFF	Trigger signal detection is off.
LEVELHI	The trigger input level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger input level is set below 1.8 volts.
EDGEHI	Configures the system to trigger on the rising edge of a pulse.
EDGELO	Configures the system to trigger on the falling edge of a pulse.

External Trigger Out (TRGOUT)

(Wind River ICE SX only)

CF TRGOUT[LEVELHI, LEVELLO, PULSEHI, PULSELO]

This option allows you to set the trigger output signal type and level. The following table describes the available settings for this option.

Table 12-2 **Trigger Out Settings**

Setting	Description
LEVELHI	The trigger output level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger output level is set below 1.8 volts.

Table 12-2 **Trigger Out Settings**

Setting	Description
PULSEHI	Trigger Out signal pin will be a pulse from LOW to HIGH and back to LOW when triggered.
PULSELO	Trigger Out signal pin will be a pulse from HIGH to LOW and back to HIGH when triggered.

IMMR Base Address Location At Reset (RSTIMMR)

CF RSTIMMR[VALUE,AUTO]

The Internal Memory Mapped Register (IMMR) contains the base address for all of the internal memory mapped registers. This configuration option allows you to change the IMMR value, thus changing the address of the internal memory mapped registers. When set to **AUTO**, the default IMMR value is used. The default value is 0x0F000000.

Invalidate Instruction Cache on GO (INVCI)

CF INVCI[YES,NO]

This option controls whether the contents of the target processor's Instruction Cache are invalidated when you issue a **GO** command. Setting this option to **YES** causes the cache contents to be invalidated.

Issue an IN on Coldstart (INCOLD)

CF INCOLD[YES,NO]

This option configures the emulator boot sequence.

Set this option to **YES** to issue an **IN** command, which asserts a reset on the target during a boot sequence.

Set this option to **NO** to issue a **SYNC** command instead of asserting reset on the target. The **SYNC** command does not reset the board. It establishes JTAG communications and captures the current context. This option is best if you want to hot plug the emulator into a running target.

The default is **NO**.

JTAG Clock Rate (MHz) (CLK)

CF CLK[0.025...100, AUTO]

This option configures the rate at which debug commands are clocked to the target. The default setting is **16**.

Little-endian Mode (LENDIAN)

CF LENDIAN[YES,NO]

This configuration value determines whether the debugger treats memory contents as little-endian (bits ordered 0..63) or big-endian (bits ordered 63..0.) This affects display and interpretation of opcodes in the debugger window, as well as the effects of symbolic manipulation of variables. Setting this option to **YES** means that little-endian is used; setting the option to **NO** means that big-endian is used.

Load Boot Table on IN (BL)

CF BL [ENABLE, DISABLE]

This option enables or disables the Linux bootline commands.

Memory Management Unit Mode (MMU)

CF MMU [ENABLE, DISABLE]

This option enables or disables the Linux memory management unit.

Monitor Target Reset (RST)

CF RST[YES,NO,HALT, RUN]

This function continuously monitors the target reset signal. If a reset occurs, one of the following actions may be taken:

- **YES** - If a target reset occurs it is reported to the user and BDM control is lost.
- **NO** - If a target reset occurs it is ignored. This is normally used if the code contains a reset instruction, which causes a reset to the external hardware, but not reset the core.

- **HALT** - If the reset occurs in this mode the target is trapped at the restart vector.
- **RUN** - If the reset occurs in this mode the target is restarted and BDM control is maintained.

By default, this option is set to **YES**. It should only be changed to **NO** if you have a RESET instruction in your code.

Power On Reset Length N*1ms (PONR)

CF PONR[0..500]

Some target designs implement reset logic that extends the duration of **HRESET** upon power up. This option allows you to specify the duration of the assertion of the reset signal so that the emulator knows when to expect the target to release the signal. The number specified can be between 0 and 500, and it represents the number of milliseconds to wait.

Processor Mode (MODE)

CF MODE[32,64]

This parameter determines the operational mode of the processor. The processor can run in a 32-bit or a 64-bit memory mode, depending on the implementation on a target. This parameter compensates for the processor mode in memory accesses to ensure that the correct accesses are made for any given command.

Real Time Preservation (RTP)

CF RTP[YES,NO]

When this option is enabled, real-time preservation allows the target to run without the emulator stopping the target inadvertently.

Reset Configuration Word Location (RSTCONF)

CF RSTCONF[AUTO,HIGH,LOW]

The reset configuration word is read by the emulator during initialization to determine the reset IMMR value. When set to **AUTO**, the emulator searches all valid Reset Word locations to find the value.

Reset Pulse Length N*1ms (RPL)

CF RPL[1..9000]

This configuration option allows you to adjust the duration of the assertion of the HRESET signal on the target board. The number you specify in this option is the number of milliseconds that HRESET is driven active on the target.

Sense Power via HRESET (SPOWER)

CF SPOWER[YES,NO]

This option lets the hardware determine if power is applied to the target by monitoring the HRESET level when it is released. This prevents the hardware from trying to continue the initialization sequence if power is not applied to the target board.

Set Breakpoint (SB)

CF SB[SB,IHBC]

This option remaps traditional software breakpoints to internal hardware breakpoints. It is set to Software Breakpoint (**SB**) by default. Setting it to **IHBC** means that all software breakpoints are translated to internal hardware breakpoints. This option is useful when you are debugging code out of Flash or PROM.

Setting this option to **IHBC** may cause limitations in the number of breakpoints that can be set, depending on the target processor.

Set Work Space (WSPACE)

CF WSPACE[BASE and **SIZE]**

Flash programming requires a small amount of target RAM to program the flash algorithm. You must tell your emulator where writable RAM is located on your target for this purpose.

As part of the configuration process, the emulator will indicate exactly how much of the RAM workspace is required. Depending on the device family and type, this space is limited to under 2 KB. Note that more memory improves the speed of programming.

To configure the workspace for flash programming the parameters should be entered in hex, where **BASE** is the start address, and **SIZE** is the minimum bytes of target RAM required, as displayed in the **Flash Programmer** view. This command allocates memory on the target system that is used by the emulator for various functions, including flash programming.

Target Console Redirection (TGTCONS)

CF TGTCONS [TGTCONS, BDM] (for the Wind River ICE SX)

Wind River Probe

Target Console Redirection is not currently supported for the Wind River Probe. You do not need to set this option.

Wind River ICE SX

BDM -- Use this setting to connect I/O on a target board, using the Transparent Mode Driver, to the target's BDM connector. When **BDM** is selected, the Wind River ICE SX is in Transparent Mode, and all I/O data is redirected to the port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

For this type of connection to work, the target application must be linked to the Transparent Mode Driver. Refer to the Wind River *Transparent Mode Driver User's Manual* for more information.

TGTCONS -- Use this setting to connect a COM port on a target board to the TGTCONS port of a Wind River ICE SX. All I/O data is then redirected to port 1237 of the Wind River ICE's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

TMD Mode (TMD)

CF TMD[ENABLE, DISABLE]

This command sets all of the configuration parameters that are required to use the Transparent Mode Driver (TMD). Select **ENABLE** to configure your system for use with the TMD, and **DISABLE** if you do not plan to use it.

Trap Exception (TRPEXP)

CF TRPEXP[YES, NO, SOI, BREAKPOINTONLY]

This option allows you to configure which run time exceptions are trapped. Setting this option to **YES** causes the emulator to trap RST, CHSTP, MCI, ALI, TRE, SEI, LBRK, IBRK, EBRK, and DPI exceptions. Setting it to **NO** causes the emulator not to trap any exceptions other than TRE and SE. Setting the option to **BREAKPOINTONLY** causes the emulator to trap exceptions only when a breakpoint is encountered. Setting the option to Step Over Interrupt (**SOI**) has the same characteristics as the **YES** option, except that while stepping, the emulator checks each step to see if it has stepped into an exception service routine. If so, it determines what line of code caused the exception and allows the processor to run through the exception and back to the next instruction to be stepped. Please refer to your processor documentation for actual bit position definitions.

Trigger in Filter Mode (TRGINFILTER)

(Wind River ICE SX only)

CF TRGINFILTER[OFF,ON]

This option provides a filtering option for the Trigger In function. When set to **ON**, a detected signal is required for at least 2 clock periods, or 40ns. This option ensures that noise does not cause a trigger.

Trigger In Report Mode (BRKREP)

(Wind River ICE SX only)

CF BRKREP [REPONLY, BRKREP]

When this option is set to **BRKREP**, which is the default setting, a Trigger In signal will be reported and set a breakpoint. When set to **REPONLY**, a Trigger in signal will be reported, but will not set a breakpoint.

Trigger Out Mode (TRGOUTMODE)

(Wind River ICE SX only)

CF TRGOUTMODE[OFF, ONALLSTOPS, ONBREAKPOINT]

This option allows you to set the type of events that will cause a trigger output to occur.

OFF -- Trigger output is off.

ONALLSTOPS -- Triggers whenever the target stops running.

ONBREAKPOINT -- Triggers whenever a breakpoint is encountered.

Vector Table Location (VECTOR)

CF VECTOR[HIGH, LOW, IGNORE]

This command specifies the location of the exception vector that is used by the software breakpoints. Please note that this setting must match the MSR register setting for software breakpoints to function correctly.

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PowerPC 85xx Processors

This chapter describes the configuration options available for PowerPC 85xx processors.

Not all of these CF options apply to all target processors; in general, only applicable options will be visible for any given processor. Which options are visible also depends on whether you are using a Wind River Probe or Wind River ICE SX.

Acquire Trace on GO (TRCAQU)

CF TRCAQU [OFF, ON}

Use this option to configure how Workbench software trace starts to store trace information.

When the target begins running code, Workbench can either wait until an event occurs to start storing trace information, or it can start immediately.

When this option is set to **ON**, Workbench starts acquiring trace information as soon as a **GO** command is issued, and does not stop until an event occurs to disable trace.

When this option is set to **OFF**, Workbench does not begin acquiring trace information until an event occurs to turn trace on.

Clear Trace Buffer on GO (TRCCLR)

CF TRCCLR [YES, NO]

Use this option to control where to start saving trace data in the trace memory.

YES -- When a **GO** command is issued, Workbench stores all newly captured trace data starting at the first trace memory location. All previously stored trace data is overwritten and lost.

NO -- When a **GO** command is issued, Workbench stores all newly captured trace data starting at the next trace memory location. Previously stored trace data is not overwritten.

CPU Reset Type (RESET)

CF RESET [HRESET, SRESET, HRESET_UNFILTER, SRESET_UNFILTER]

This option allows you to generate either a **HRESET** or a **SRESET** signal when an **IN** or **INN** command is issued. Selecting **HRESET_UNFILTER** or **SRESET_UNFILTER** means that the reset signal is not sampled when an **IN** or **INN** command is issued.

Delay After Reset N*1ms (DRST)

CF DRST[0..6000]

This option allows you to modify the delay between the release of **HRESET** and the first JTAG communication attempt. The default is 1.

Download Mode (DLD)

CF DLD[NORMAL, 8, 32]

This parameter controls the size of memory transfers when downloading code. Set this option to the width of the memory that you are planning to download your code to. Setting the option to **NORMAL** means that the bus width is 64 bits; **8** means that the bus width is 8 bits; **32** means that the bus width is 32 bits.

Drive TReset Line (TRESET)

CF TRESET[OPENC, ACTIVE]

This parameter controls the logic applied to the **TRESET** signal on the target. Selecting **OPENC** uses an **open collector** approach in which the active driver is released by tri-stating the line and allowing conditioning resistors on the target to return the signal to the non-active state. Selecting **ACTIVE** in this option causes the emulator to drive the **TRESET** signal to both active and inactive states. This is sometimes required on targets in which the conditioning resistors cause excessive rise or fall time on the signal when returning to an inactive state. This excessive time can cause the processor to come out of reset in an incorrect state.

Emulator HRESET Command Control (CMDRST)

(Wind River ICE SX only)

CF CMDRST[IN,RST,BOTH]

This configuration option is used for multicore debugging, and is used to define when the HRESET line is asserted during a reset. If the option is set to **BOTH**, any time an **IN** or a **RST** command is issued, all of the processors that are running are reset. If the option is set to **IN**, then all of the processors reset only when an **IN** command is issued. If a **RST** command is issued, only the processor that is being used is reset and the other ones are left running. If the option is set to **RST**, then all of the processors will reset if a **RST** command is issued. However, if an **IN** command is issued, only the processor that you are using will reset.

Emulator HRESET Control (HRESET)

CF HRESET[ENABLE, DISABLE]

This option determines whether the **HRESET** line is asserted when you issue an **IN** command. Selecting **ENABLE** asserts **HRESET**, and selecting **DISABLE** prevents **HRESET** from being asserted.

Enable Checkstop Interrupt (CHECKSTOP)

CF CHECKSTOP[YES, NO]

Several different signals are multiplexed with the **CHKSTP_OUT** signal on the processor. The **CHKSTP_OUT** pin can be used for other purposes (such as data parity configuration) instead of for the **CHKSTP_OUT** signal, depending on what you need for development. If you do not plan to use this pin for the **CHKSTP_OUT** signal, set this configuration option to **NO**.

The 8260 processor has multiplexed several different signals with the **CHKSTP_OUT** on the package. If the application uses any of the other possible configurations, then this option needs to be set to **NO** to prevent the firmware from trapping the transitions of the signal as memory bus errors when the real indication is something else. Setting this option to **YES** causes the hardware to trap the assertion of this signal as a memory bus error.

Exception Taken Mask Value (ETM)

CF ETM[00000...FFFFF]

This option allows the CPU to halt core at exception vectors. The default is **C2010.** (A **1** allows core to halt - IVOR0, IVOR1, IVOR6, IVOR15.)

Execute PowerOnReset ABIST Test (PORABIST)

CF PORABIST[YES, NO]

This option controls the Automatic Built-In Self-Test (ABIST.) Setting the option to **YES** (the default) will run ABIST after release of HRESET. Setting it to **NO** does not run ABIST.

External Trigger In (TRGIN)

(Wind River ICE SX only)

CF TRGIN[OFF, LEVELHI, LEVELLO, EDGEHI, EDGELO]

This option sets the trigger input signal sense detection. When activated, **Trigger In** stops the target upon detection. **Trigger In** does not work with any events.

The following table describes the available settings for this option.

Table 13-1 **Trigger In Settings**

Setting	Description
OFF	Trigger signal detection is off.
LEVELHI	The trigger input level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger input level is set below 1.8 volts.
EDGEHI	Configures the system to trigger on the rising edge of a pulse.
EDGELO	Configures the system to trigger on the falling edge of a pulse.

External Trigger Out (TRGOUT)

(Wind River ICE SX only)

CF TRGOUT[LEVELHI, LEVELLO, PULSEHI, PULSELO]

This option allows you to set the trigger output signal type and level. The following table describes the available settings for this option.

Table 13-2 **Trigger Out Settings**

Setting	Description
LEVELHI	The trigger output level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger output level is set below 1.8 volts.
PULSEHI	Trigger Out signal pin will be a pulse from LOW to HIGH and back to LOW when triggered.
PULSELO	Trigger Out signal pin will be a pulse from HIGH to LOW and back to HIGH when triggered.

Flush Data Cache on Read (FLUSH_DCACHE)

CF FLUSH_DCACHE [YES, NO]

When running with the data cache enabled, the processor updates values in the data cache, not the memory. However, when you are examining values on the target with Wind River Workbench, for instance using the **Memory** view or the **Watch** view, Workbench queries the memory, not the data cache. So the information in the view may not be accurate. To avoid this problem, set **CF FLUSH_DCACHE** to **YES**. When this option is set to **YES**, any time there is a read command, such as a refresh in the **Memory** view, the memory location that the view is querying is updated from the data cache.

Setting this option does not cause the entire memory to be updated on any read command, because that would significantly slow performance. Only the memory location being queried is updated.

Because writing and reading to cache is much faster than writing and reading to memory, performance is faster when this option is set to **NO**, which is the default. If you do not need to examine values on the target, leave this option set to **NO**.

Issue an IN on Coldstart (INCOLD)

CF INCOLD[YES,NO]

This option configures the emulator boot sequence.

Set this option to **YES** to issue an **IN** command, which asserts a reset on the target during a boot sequence.

Set this option to **NO** to issue a **SYNC** command instead of asserting reset on the target. The **SYNC** command does not reset the board. It establishes JTAG communications and captures the current context. This option is best if you want to hot plug the emulator into a running target.

The default is **NO**.

JTAG Clock Rate (MHz) (CLK)

CF CLK[0.025...100, AUTO]

This option configures the rate at which debug commands are clocked to the target. The default setting is **16**.

L2 TLB Base Address for INN (L2TLB)

CF L2TLB [BASE]

When an **INN** command is issued, the emulator requires a minimum TLB entry for breakpoints when debugging ROM code. Use this option to enter the base address of the memory (RAM). The default value is address **0x0**.

Little-endian Mode (LENDIAN)

CF LENDIAN[YES,NO]

This configuration value determines whether the debugger treats memory contents as little-endian (bits ordered 0..63) or big-endian (bits ordered 63..0.) This affects display and interpretation of opcodes in the debugger window, as well as the effects of symbolic manipulation of variables. Setting this option to **YES** means that little-endian is used; setting the option to **NO** means that big-endian is used.

Load Boot Table on IN (BL)

CF BL [ENABLE, DISABLE]

This option enables or disables the Linux bootline commands.

Local Bus Clock Frequency > 133 MHz (LBCLK)

CF LBCLK[YES, NO]

This option implements LBC11 Errata for MPC85xx silicon:

YES - Does not implement errata if local bus frequency is greater than 133 MHz.

NO - Implements errata if local bus frequency is less than or equal to 133 MHz.

By default, the option is set to **NO**.

MMU Support Control (MMU)

CF MMU[ENABLE, DISABLE]

This option controls physical to virtual address translation.

ENABLE -- Informs the emulator that addresses should be checked for virtual mapping.

DISABLE -- Addresses will not be checked for virtual mapping.

Monitor Target Reset (RST)

CF RST[YES, NO, HALT, RUN]

This function continuously monitors the target reset signal. If a reset occurs, one of the following actions may be taken:

- **YES** - If a target reset occurs it is reported to the user and BDM control is lost.
- **NO** - If a target reset occurs it is ignored. This is normally used if the code contains a reset instruction, which causes a reset to the external hardware, but not reset the core.
- **HALT** - If the reset occurs in this mode the target is trapped at the restart vector.
- **RUN** - If the reset occurs in this mode the target is restarted and BDM control is maintained.

By default, this option is set to **YES**. It should only be changed to **NO** if you have a RESET instruction in your code.

Override Boot Mode (BOOTMODE)

CF BOOTMODE[I2C_DIS, HLDOFF_DIS, BOTH_DIS, NORMAL]

This option overrides external strapping of configuration pins. The option is set to **NORMAL** by default.

- **I2C_DIS**--Disables I2C boot sequencer, if enabled by external strapping.
- **HLDOFF_DIS** --Disables CPU boot hold off, if enabled by external strapping.
- **BOTH_DIS** --Disables both I2C boot sequencer and CPU boot hold off if enabled by external strapping.
- **NORMAL** --Disables overrides.

Override DDR DLL (DDR DLL)

CF DDR DLL [YES, NO]

This option allows the emulator to implement the workaround of the DDR **dll** errata problem (DDR9) for the MPC8540 and MPC8560 processors. The default value is **YES**.

Power On Reset Length N*1ms (PONR)

CF PONR[0..500]

Some target designs implement reset logic that extends the duration of **HRESET** upon power up. This option allows you to specify the duration of the assertion of the reset signal so that the emulator knows when to expect the target to release the signal. The number specified can be between 0 and 500, and it represents the number of milliseconds to wait.

Real Time Preservation (RTP)

CF RTP[YES,NO]

When this option is enabled, real-time preservation allows the target to run without the emulator stopping the target inadvertently.

Reset Pulse Length N 1*ms (RPL)

CF RPL[1..6000]

This configuration option allows you to adjust the duration of the assertion of the HRESET signal on the target board. The number you specify in this option is the number of milliseconds that HRESET is driven active on the target.

Sense Power via HRESET (SPOWER)

CF SPOWER[YES,NO]

This option lets the hardware determine if power is applied to the target by monitoring the HRESET level when it is released. This prevents the hardware from

trying to continue the initialization sequence if power is not applied to the target board.

Set Breakpoint (SB)

CF SB[SB,IHBC]

This option remaps traditional software breakpoints to internal hardware breakpoints. It is set to Software Breakpoint (**SB**) by default. Setting it to **IHBC** means that all software breakpoints are translated to internal hardware breakpoints. This option is useful when you are debugging code out of Flash or PROM.

Setting this option to **IHBC** may cause limitations in the number of breakpoints that can be set, depending on the target processor.

Set Work Space (WSPACE)

CF WSPACE[BASE and **SIZE]**

Flash programming requires a small amount of target RAM to program the Flash Algorithm. You must tell your emulator where writable RAM is located on your target for this purpose.

As part of the configuration process, the emulator will indicate exactly how much of the RAM workspace is required. Depending on the device family and type, this space is limited to under 2 KB. Note that more memory improves the speed of programming.

To configure the workspace for flash programming the parameters should be entered in hex, where **BASE** is the start address, and **SIZE** is the minimum bytes of target RAM required, as displayed in the **Flash Programmer** view. This command allocates memory on the target system that is used by the emulator for various functions, including flash programming.

Target Console Redirection (TGTCONS)

CF TGTCONS [**TGTCONS**, **BDM**] (for the Wind River ICE SX)

Wind River Probe

Target Console Redirection is not currently supported for the Wind River Probe. You do not need to set this option.

Wind River ICE SX

BDM -- Use this setting to connect I/O on a target board, using the Transparent Mode Driver, to the target's BDM connector. When **BDM** is selected, the Wind River ICE SX is in Transparent Mode, and all I/O data is redirected to the port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

For this type of connection to work, the target application must be linked to the Transparent Mode Driver. Refer to the *Wind River Workbench On-Chip Debugging Guide: Using the WDB Transparent Mode Driver* for more information.

TGTCONS -- Use this setting to connect a COM port on a target board to the TGTCONS port of a Wind River ICE SX. All I/O data is then redirected to port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

Target CPU (TAR)

CF TAR *target processor*

This option allows you to configure the emulator for the target that you are using. *target processor* is the name of your processor. For example, to configure the emulator for a PowerPC 8560 target, type:

```
CF TAR 8560
```

TMD Mode (TMD)

CF TMD[ENABLE, DISABLE]

This command sets all of the configuration parameters that are required to use the Transparent Mode Driver (TMD). Select **ENABLE** to configure your system for use with the TMD, and **DISABLE** if you do not plan to use it.

Trap Exception (TRPEXP)

CF TRPEXP[YES, NO, SOI, BREAKPOINTONLY]

This option allows you to configure which run time exceptions are trapped. Setting this option to **YES** causes the emulator to trap RST, CHSTP, MCI, ALI, TRE, SEI, LBRK, IBRK, EBRK, and DPI exceptions. Setting it to **NO** causes the emulator not to trap any exceptions other than TRE and SE. Setting the option to **BREAKPOINTONLY** causes the emulator to trap exceptions only when a breakpoint is encountered. Setting the option to Step Over Interrupt (**SOI**) has the same characteristics as the **YES** option, except that while stepping, the emulator checks each step to see if it has stepped into an exception service routine. If so, it determines what line of code caused the exception and allows the processor to run through the exception and back to the next instruction to be stepped. Please refer to your processor documentation for actual bit position definitions.

Trigger in Filter Mode (TRGINFILTER)

(Wind River ICE SX only)

CF TRGINFILTER[OFF,ON]

This option provides a filtering option for the Trigger In function. When set to **ON**, a detected signal is required for at least 2 clock periods, or 40ns. This option ensures that noise does not cause a trigger.

Trigger In Report Mode (BRKREP)

(Wind River ICE SX only)

CF BRKREP [REPONLY, BRKREP]

When this option is set to **BRKREP**, which is the default setting, a Trigger In signal will be reported and set a breakpoint. When set to **REPONLY**, a Trigger in signal will be reported, but will not set a breakpoint.

Trigger Out Mode (TRGOUTMODE)

(Wind River ICE SX only)

CF TRGOUTMODE[OFF, ONALLSTOPS, ONBREAKPOINT]

This option allows you to set the type of events that will cause a trigger output to occur.

OFF -- Trigger output is off.

ONALLSTOPS -- Triggers whenever the target stops running.

ONBREAKPOINT -- Triggers whenever a breakpoint is encountered.

14

PowerPC 86xx Processors

This chapter describes the configuration options available for PowerPC 86xx processors.

Not all of these CF options apply to all target processors; in general, only applicable options will be visible for any given processor. Which options are visible also depends on whether you are using a Wind River Probe or Wind River ICE SX.

Acquire Trace on GO (TRCAQU)

CF TRCAQU [OFF, ON}

Use this option to configure how Workbench software trace starts to store trace information.

When the target begins running code, Workbench can either wait until an event occurs to start storing trace information, or it can start immediately.

When this option is set to **ON**, Workbench starts acquiring trace information as soon as a **GO** command is issued, and does not stop until an event occurs to disable trace.

When this option is set to **OFF**, Workbench does not begin acquiring trace information until an event occurs to turn trace on.

Clear Trace Buffer on GO (TRCCLR)

CF TRCCLR [YES, NO]

Use this option to control where to start saving trace data in the trace memory.

YES -- When a **GO** command is issued, Workbench stores all newly captured trace data starting at the first trace memory location. All previously stored trace data is overwritten and lost.

NO -- When a **GO** command is issued, Workbench stores all newly captured trace data starting at the next trace memory location. Previously stored trace data is not overwritten.

CPU Reset Type (RESET)

CF RESET [HRESET, SRESET, HRESET_UNFILTER, SRESET_UNFILTER]

This option allows you to generate either a **HRESET** or a **SRESET** signal when an **IN** or **INN** command is issued. Selecting **HRESET_UNFILTER** or **SRESET_UNFILTER** means that the reset signal is not sampled when an **IN** or **INN** command is issued.

Delay After Reset N*1ms (DRST)

CF DRST[0..6000]

This option allows you to modify the delay between the release of **HRESET** and the first JTAG communication attempt. The default is 1.

Download Mode (DLD)

CF DLD[NORMAL, 8, 32]

This parameter controls the size of memory transfers when downloading code. Set this option to the width of the memory that you are planning to download your code to. Setting the option to **NORMAL** means that the bus width is 64 bits; **8** means that the bus width is 8 bits; **32** means that the bus width is 32 bits.

Drive TReset Line (TRESET)

CF TRESET[OPENC, ACTIVE]

This parameter controls the logic applied to the **TRESET** signal on the target. Selecting **OPENC** uses an **open collector** approach in which the active driver is released by tri-stating the line and allowing conditioning resistors on the target to return the signal to the non-active state. Selecting **ACTIVE** in this option causes the emulator to drive the **TRESET** signal to both active and inactive states. This is sometimes required on targets in which the conditioning resistors cause excessive rise or fall time on the signal when returning to an inactive state. This excessive time can cause the processor to come out of reset in an incorrect state.

Emulator HRESET Command Control (CMDRST)

(Wind River ICE SX only)

CF CMDRST[IN,RST,BOTH]

This configuration option is used for multicore debugging, and is used to define when the HRESET line is asserted during a reset. If the option is set to **BOTH**, any time an **IN** or a **RST** command is issued, all of the processors that are running are reset. If the option is set to **IN**, then all of the processors reset only when an **IN** command is issued. If a **RST** command is issued, only the processor that is being used is reset and the other ones are left running. If the option is set to **RST**, then all of the processors will reset if a **RST** command is issued. However, if an **IN** command is issued, only the processor that you are using will reset.

Emulator HRESET Control (HRESET)

CF HRESET[ENABLE, DISABLE]

This option determines whether the **HRESET** line is asserted when you issue an **IN** command. Selecting **ENABLE** asserts **HRESET**, and selecting **DISABLE** prevents **HRESET** from being asserted.

Enable Checkstop Interrupt (CHECKSTOP)

CF CHECKSTOP[YES, NO]

Several different signals are multiplexed with the **CHKSTP_OUT** signal on the processor. The **CHKSTP_OUT** pin can be used for other purposes (such as data parity configuration) instead of for the **CHKSTP_OUT** signal, depending on what you need for development. If you do not plan to use this pin for the **CHKSTP_OUT** signal, set this configuration option to **NO**.

The 8260 processor has multiplexed several different signals with the **CHKSTP_OUT** on the package. If the application uses any of the other possible configurations, then this option needs to be set to **NO** to prevent the firmware from trapping the transitions of the signal as memory bus errors when the real indication is something else. Setting this option to **YES** causes the hardware to trap the assertion of this signal as a memory bus error.

Exception Taken Mask Value (ETM)

CF ETM[00000...FFFFF]

This option allows the CPU to halt core at exception vectors. The default is **C2010.** (A **1** allows core to halt - IVOR0, IVOR1, IVOR6, IVOR15.)

Execute PowerOnReset ABIST Test (PORABIST)

CF PORABIST[YES, NO]

This option controls the Automatic Built-In Self-Test (ABIST.) Setting the option to **YES** (the default) will run ABIST after release of HRESET. Setting it to **NO** does not run ABIST.

External Trigger In (TRGIN)

(Wind River ICE SX only)

CF TRGIN[OFF, LEVELHI, LEVELLO, EDGEHI, EDGELO]

This option sets the trigger input signal sense detection. When activated, **Trigger In** stops the target upon detection. **Trigger In** does not work with any events.

The following table describes the available settings for this option.

Table 14-1 **Trigger In Settings**

Setting	Description
OFF	Trigger signal detection is off.
LEVELHI	The trigger input level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger input level is set below 1.8 volts.
EDGEHI	Configures the system to trigger on the rising edge of a pulse.
EDGELO	Configures the system to trigger on the falling edge of a pulse.

External Trigger Out (TRGOUT)

(Wind River ICE SX only)

CF TRGOUT[LEVELHI, LEVELLO, PULSEHI, PULSELO]

This option allows you to set the trigger output signal type and level. The following table describes the available settings for this option.

Table 14-2 **Trigger Out Settings**

Setting	Description
LEVELHI	The trigger output level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger output level is set below 1.8 volts.
PULSEHI	Trigger Out signal pin will be a pulse from LOW to HIGH and back to LOW when triggered.
PULSELO	Trigger Out signal pin will be a pulse from HIGH to LOW and back to HIGH when triggered.

Flush Data Cache on Read (FLUSH_DCACHE)

CF FLUSH_DCACHE [YES, NO]

When running with the data cache enabled, the processor updates values in the data cache, not the memory. However, when you are examining values on the target with Wind River Workbench, for instance using the **Memory** view or the **Watch** view, Workbench queries the memory, not the data cache. So the information in the view may not be accurate. To avoid this problem, set **CF FLUSH_DCACHE** to **YES**. When this option is set to **YES**, any time there is a read command, such as a refresh in the **Memory** view, the memory location that the view is querying is updated from the data cache.

Setting this option does not cause the entire memory to be updated on any read command, because that would significantly slow performance. Only the memory location being queried is updated.

Because writing and reading to cache is much faster than writing and reading to memory, performance is faster when this option is set to **NO**, which is the default. If you do not need to examine values on the target, leave this option set to **NO**.

Issue an IN on Coldstart (INCOLD)

CF INCOLD[YES,NO]

This option configures the emulator boot sequence.

Set this option to **YES** to issue an **IN** command, which asserts a reset on the target during a boot sequence.

Set this option to **NO** to issue a **SYNC** command instead of asserting reset on the target. The **SYNC** command does not reset the board. It establishes JTAG communications and captures the current context. This option is best if you want to hot plug the emulator into a running target.

The default is **NO**.

JTAG Clock Rate (MHz) (CLK)

CF CLK[0.025...100, AUTO]

This option configures the rate at which debug commands are clocked to the target. The default setting is **16**.

L2 TLB Base Address for INN (L2TLB)

CF L2TLB [BASE]

When an **INN** command is issued, the emulator requires a minimum TLB entry for breakpoints when debugging ROM code. Use this option to enter the base address of the memory (RAM). The default value is address **0x0**.

Little-endian Mode (LENDIAN)

CF LENDIAN[YES,NO]

This configuration value determines whether the debugger treats memory contents as little-endian (bits ordered 0..63) or big-endian (bits ordered 63..0.) This affects display and interpretation of opcodes in the debugger window, as well as the effects of symbolic manipulation of variables. Setting this option to **YES** means that little-endian is used; setting the option to **NO** means that big-endian is used.

Load Boot Table on IN (BL)

CF BL [ENABLE, DISABLE]

This option enables or disables the Linux bootline commands.

Local Bus Clock Frequency > 133 MHz (LBCLK)

CF LBCLK[YES, NO]

This option implements LBC11 Errata for MPC85xx silicon:

YES - Does not implement errata if local bus frequency is greater than 133 MHz.

NO - Implements errata if local bus frequency is less than or equal to 133 MHz.

By default, the option is set to **NO**.

MMU Support Control (MMU)

CF MMU[ENABLE, DISABLE]

This option controls physical to virtual address translation.

ENABLE -- Informs the emulator that addresses should be checked for virtual mapping.

DISABLE -- Addresses will not be checked for virtual mapping.

Monitor Target Reset (RST)

CF RST[YES, NO, HALT, RUN]

This function continuously monitors the target reset signal. If a reset occurs, one of the following actions may be taken:

- **YES** - If a target reset occurs it is reported to the user and BDM control is lost.
- **NO** - If a target reset occurs it is ignored. This is normally used if the code contains a reset instruction, which causes a reset to the external hardware, but not reset the core.
- **HALT** - If the reset occurs in this mode the target is trapped at the restart vector.
- **RUN** - If the reset occurs in this mode the target is restarted and BDM control is maintained.

By default, this option is set to **YES**. It should only be changed to **NO** if you have a RESET instruction in your code.

Override Boot Mode (BOOTMODE)

CF BOOTMODE[I2C_DIS, HLDOFF_DIS, BOTH_DIS, NORMAL]

This option overrides external strapping of configuration pins. The option is set to **NORMAL** by default.

- **I2C_DIS**--Disables I2C boot sequencer, if enabled by external strapping.
- **HLDOFF_DIS** --Disables CPU boot hold off, if enabled by external strapping.
- **BOTH_DIS** --Disables both I2C boot sequencer and CPU boot hold off if enabled by external strapping.
- **NORMAL** --Disables overrides.

Override DDR DLL (DDR DLL)

CF DDR DLL [YES, NO]

This option allows the emulator to implement the workaround of the DDR **dll** errata problem (DDR9) for the MPC8540 and MPC8560 processors. The default value is **YES**.

Power On Reset Length N*1ms (PONR)

CF PONR[0..500]

Some target designs implement reset logic that extends the duration of **HRESET** upon power up. This option allows you to specify the duration of the assertion of the reset signal so that the emulator knows when to expect the target to release the signal. The number specified can be between 0 and 500, and it represents the number of milliseconds to wait.

Real Time Preservation (RTP)

CF RTP[YES,NO]

When this option is enabled, real-time preservation allows the target to run without the emulator stopping the target inadvertently.

Reset Pulse Length N 1*ms (RPL)

CF RPL[1..6000]

This configuration option allows you to adjust the duration of the assertion of the HRESET signal on the target board. The number you specify in this option is the number of milliseconds that HRESET is driven active on the target.

Sense Power via HRESET (SPOWER)

CF SPOWER[YES,NO]

This option lets the hardware determine if power is applied to the target by monitoring the HRESET level when it is released. This prevents the hardware from

trying to continue the initialization sequence if power is not applied to the target board.

Set Breakpoint (SB)

CF SB[SB,IHBC]

This option remaps traditional software breakpoints to internal hardware breakpoints. It is set to Software Breakpoint (**SB**) by default. Setting it to **IHBC** means that all software breakpoints are translated to internal hardware breakpoints. This option is useful when you are debugging code out of Flash or PROM.

Setting this option to **IHBC** may cause limitations in the number of breakpoints that can be set, depending on the target processor.

Set Work Space (WSPACE)

CF WSPACE[BASE and **SIZE]**

Flash programming requires a small amount of target RAM to program the Flash Algorithm. You must tell your emulator where writable RAM is located on your target for this purpose.

As part of the configuration process, the emulator will indicate exactly how much of the RAM workspace is required. Depending on the device family and type, this space is limited to under 2 KB. Note that more memory improves the speed of programming.

To configure the workspace for flash programming the parameters should be entered in hex, where **BASE** is the start address, and **SIZE** is the minimum bytes of target RAM required, as displayed in the **Flash Programmer** view. This command allocates memory on the target system that is used by the emulator for various functions, including flash programming.

Target Console Redirection (TGTCONS)

CF TGTCONS [**TGTCONS**, **BDM**] (for the Wind River ICE SX)

Wind River Probe

Target Console Redirection is not currently supported for the Wind River Probe. You do not need to set this option.

Wind River ICE SX

BDM -- Use this setting to connect I/O on a target board, using the Transparent Mode Driver, to the target's BDM connector. When **BDM** is selected, the Wind River ICE SX is in Transparent Mode, and all I/O data is redirected to the port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

For this type of connection to work, the target application must be linked to the Transparent Mode Driver. Refer to the *Wind River Workbench On-Chip Debugging Guide: Using the WDB Transparent Mode Driver* for more information.

TGTCONS -- Use this setting to connect a COM port on a target board to the TGTCONS port of a Wind River ICE SX. All I/O data is then redirected to port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

Target CPU (TAR)

CF TAR *target processor*

This option allows you to configure the emulator for the target that you are using. *target processor* is the name of your processor. For example, to configure the emulator for a PowerPC 8641 target, type:

```
CF TAR 8641
```

TMD Mode (TMD)

CF TMD[ENABLE, DISABLE]

This command sets all of the configuration parameters that are required to use the Transparent Mode Driver (TMD). Select **ENABLE** to configure your system for use with the TMD, and **DISABLE** if you do not plan to use it.

Trap Exception (TRPEXP)

CF TRPEXP[YES, NO, SOI, BREAKPOINTONLY]

This option allows you to configure which run time exceptions are trapped. Setting this option to **YES** causes the emulator to trap RST, CHSTP, MCI, ALI, TRE, SEI, LBRK, IBRK, EBRK, and DPI exceptions. Setting it to **NO** causes the emulator not to trap any exceptions other than TRE and SE. Setting the option to **BREAKPOINTONLY** causes the emulator to trap exceptions only when a breakpoint is encountered. Setting the option to Step Over Interrupt (**SOI**) has the same characteristics as the **YES** option, except that while stepping, the emulator checks each step to see if it has stepped into an exception service routine. If so, it determines what line of code caused the exception and allows the processor to run through the exception and back to the next instruction to be stepped. Please refer to your processor documentation for actual bit position definitions.

Trigger in Filter Mode (TRGINFILTER)

(Wind River ICE SX only)

CF TRGINFILTER[OFF,ON]

This option provides a filtering option for the Trigger In function. When set to **ON**, a detected signal is required for at least 2 clock periods, or 40ns. This option ensures that noise does not cause a trigger.

Trigger In Report Mode (BRKREP)

(Wind River ICE SX only)

CF BRKREP [REPONLY, BRKREP]

When this option is set to **BRKREP**, which is the default setting, a Trigger In signal will be reported and set a breakpoint. When set to **REPONLY**, a Trigger in signal will be reported, but will not set a breakpoint.

Trigger Out Mode (TRGOUTMODE)

(Wind River ICE SX only)

CF TRGOUTMODE[OFF, ONALLSTOPS, ONBREAKPOINT]

This option allows you to set the type of events that will cause a trigger output to occur.

OFF -- Trigger output is off.

ONALLSTOPS -- Triggers whenever the target stops running.

ONBREAKPOINT -- Triggers whenever a breakpoint is encountered.

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ColdFire Processors

This chapter describes the configuration options that are available for Freescale ColdFire processors (formerly Motorola ColdFire.)

Not all of these CF options apply to all target processors; in general, only applicable options will be visible for any given processor. Which options are visible also depends on whether you are using a Wind River Probe or Wind River ICE SX.

BDM Clock Rate (CLK)

CF CLK [0.125, 0.25, 0.5, 1, 2, 4, 5, 6]

Use this option to set the BDM clock frequency, in megahertz, that is used for BDM communications. The 0.125, 0.25, 0.5, 1, 2, 4, 5 and 6 settings are used to control the **DSCLK** signal frequency on the 26/30 pin BDM connector. For brevity, the settings listed are approximations of the actual frequency. What setting you should use depends on the core frequency of the ColdFire processor on the target board. The maximum BDM clock frequency is limited to 20 per cent of the core frequency. Generally, the higher the core frequency, the higher the **CLK** parameter setting can be. A little experimenting with this setting will allow you to maximize the BDM communications speed. This is significant for maximizing image download and upload speeds. The default value is **2**.

Length of Reset Pulse N x 10ms (PLS)

CF PLS [1..100]

Use this option to set the length of time, in milliseconds, that the RESET# signal on the 26/30 pin BDM connector is pulsed low during initialization as a result of an **IN** or **INN** command. The pulse length setting can be specified from 1 to 100. The pulse length setting is multiplied by 10, which will produce a pulse length of 10 to 1000 milliseconds, respectively. The default setting is **4**.

Load PC and A7 Registers on IN or INN Command (LOAD_PC_A7)

CF LOAD_PC_A7 [YES, NO]

This option determines whether the **IN** or **INN** command will load the A7 and PC registers from the values stored in the boot Chip Select addresses **0x0** and **0x4**, respectively. The default setting is **YES**.

Mask Interrupts While Stepping (SIL)

CF SIL[0..7]

Use this option to set the interrupt level mask while stepping through code. The interrupt level mask setting can be specified from **0** (the default) to **7**. The interrupt level mask setting is written to the status register in the ColdFire processor prior to actually stepping the code. The status register is then restored to its original value after the step is completed. This allows you to control which interrupts to ignore while stepping through code.

This option should be set to **0** if the Step Over ISR (**CF SOI)** option is set to **YES**.

Monitor Target Reset (RST)

CF RST[YES, NO, HALT, RUN]

Use this option to configure the reset monitor, which monitors the status of the RESET# signal on the 26/30 pin BDM connector. The setting is used to determine what action is taken when a RESET# low condition is detected by the reset monitor:

- **YES** - This setting enables the reset monitor. A target reset will cause an error message to appear, stating that an unexpected reset occurred. The emulator will enter **>ERR>** mode.

- **NO** - This setting disables the reset monitor. A target reset will not cause an error message, and the emulator will remain in its current mode.
- **HALT** - This setting enables the reset monitor. A target reset will cause an error message to appear, stating that an unexpected reset occurred. The emulator will enter **>BKM>** mode. If the CF option **LOAD_PC_A7** is set to **YES**, the **A7** and **PC** registers will be set to the values stored in the boot Chip Select addresses **0x0** and **0x4**, respectively.
- **RUN** - This setting enables the reset monitor. A target reset will cause an error message to appear, stating that an unexpected reset occurred. The emulator will enter **>RUN>** mode. If the CF option **LOAD_PC_A7** is set to **YES**, the **A7** and **PC** registers will be set to the values stored in the boot Chip Select addresses **0x0** and **0x4**, respectively. The target will then be started at the location that was loaded into the **PC** register.

By default, this option is set to **YES**.

Preserve Registers on INN Command (PRINN)

CF PRINN[YES, NO]

Use this option to preserve register values as a result of an **INN** command. The default setting is **NO**. The Preserve Registers settings are used to determine whether the registers will be preserved as follows:

YES -- When an **INN** command is issued, all registers are preserved with their original values before the **INN** command was issued. The only exception to this is for the version 4 core ColdFire processors, which will not allow the D0 and D1 registers to be preserved.

NO -- When an **INN** command is issued, the A7 and PC registers will be set to the values stored in the boot Chip Select addresses **0x0** and **0x4**, respectively, if the **LOAD_PC_A7** option is set to **YES**.

NOTE: The Preserve Registers option applies only to the **INN** command. It will not affect an **IN** command.

PST Signals Available (PST)

CF PST[YES, NO]

This option is used to configure the emulator depending on whether or not the PST[0:3] signals from the ColdFire processor are available on the 26/30 pin BDM connector. Some ColdFire processors have multiplexed PST/PP or PST/GPIO pins that can be configured as either PST signal pins or PP (parallel port) signal pins or GPIO (General Purpose I/O) signal pins.

Setting this option to **YES** (the default) tells the emulator that the PST[0:3] signals are available on the 26/30 pin BDM connector. The PST[0:3] signals are then monitored to determine if the processor is running or halted. If the PST[0:3] signals are available, this option should always be set to **YES**.

Setting the option to **NO** tells the emulator that PST[0:3] signals are not available on the 26/30 pin BDM connector. In that case the CSR register is polled to determine if the processor is running or halted.

Real Time Preservation (RTP)

CF RTP [NONE, ALLOW_STEALS, FULL]

Use this option to control real-time preservation when a target is in **>RUN>** mode. The default setting is **NONE**. Real-time preservation settings determine which BDM commands are allowed to be processed while the target is in **>RUN>** mode. This includes all BDM commands, whether issued manually by the user or automatically by the debugger. The BDM commands will be processed based on the real-time preservation setting as follows:

NONE

- All core register reads and writes will be allowed, but the ColdFire processor will halt momentarily to process the command.
- All memory writes will be allowed and will not cause the ColdFire processor to be halted, but cycle steals will occur to process the command.
- All memory reads will be allowed and will not cause the ColdFire processor to be halted, but cycle steals will occur to process the command.

ALLOW_STEALS

- All core register reads and writes will not be allowed and a warning message will appear.

- All memory writes will not be allowed and a warning message will appear.
- All memory reads will be allowed and will not cause the ColdFire processor to be halted, but cycle steals will occur to process the command.

FULL

- All core register reads and writes will not be allowed and a warning message will appear.
- All memory reads will not be allowed and a warning message will appear.
- All memory writes will not be allowed and a warning message will appear.

Remap Software Breakpoint (SB)

CF SB [SB, IHBC, AUTO]

Use the SB option to remap software breakpoints. The default setting is **SB**. You can set software breakpoints by double-clicking on any line of code in the **Source** window.

NOTE: Software breakpoints are actually installed when the target is started, not when they are set.

The **SB**, **IHBC** and **AUTO** settings are used to remap software breakpoints as follows:

SB -- This setting will cause software breakpoints to be set as software breakpoints. Software breakpoints can only be installed in code that is running in read/write memory. If the software breakpoint was installed, the target will enter **>RUN>** mode when started. If the software breakpoint cannot be installed, the target will enter **>TRC>** mode when started.

IHBC -- This setting will cause software breakpoints to be set as internal hardware code breakpoints. Internal hardware code breakpoints are used to set breakpoints in code that is running in read-only memory.

You may not be able to set an internal hardware code breakpoint if all available internal hardware code breakpoints, for your particular ColdFire processor, have already been used.The maximum number of internal hardware code breakpoints that can be set varies by ColdFire processor type.

If the internal hardware code breakpoint could be set, the target will enter **>RUN>** mode when started. If the internal hardware code breakpoint could not be set, a

message will appear stating that the internal hardware code breakpoint could not be set, and the target will remain in **>BKM>** mode.

AUTO -- This setting will cause software breakpoints to be set as software breakpoints. As previously noted, software breakpoints are actually installed when the target is started. Software breakpoints can only be installed in code that is running out of read/write memory. If the software breakpoint was installed, the target will enter **>RUN>** mode when started. If the software breakpoint cannot be installed, and an internal hardware code breakpoint is available, the software breakpoint will automatically be converted to an internal hardware code breakpoint, and the target will enter **>RUN>** mode. If the software breakpoint cannot be installed, and an internal hardware code breakpoint is not available, a message will appear stating that the software breakpoint could not be changed to an internal hardware code breakpoint, and the target will remain in **>BKM>** mode.

Set VBR (SET_VBR)

CF SET_VBR [VALUE]

Use the **SET_VBR** parameter to set the Vector Base Register (VBR) to a specified value on an **IN** command. The value should be the same as what the code will set it to. The Vector Base Register needs to be set so that the debug exception handler address, which is defined in the Set Work Space (**CF WSPACE**) option, can be entered in the exception table. The default value is zero. Bits 0..19 are not used.

For example, the command

```
CF SET_VBR 20000000
```

will set the Vector Base Register to 20000000 when an **IN** command is issued.

Set Work Space (WSPACE)

CF WSPACE[**BASE** and **SIZE**]

Use this option to allocate a small amount of RAM, located on the target, for the emulator to use as a work space. The emulator uses the work space for loading the flash programming algorithm, and for loading data when programming flash. A large work space will improve flash programming speed.

The emulator also uses the work space to load a debug handler when performing filtered trace. The debug handler work space must be at least 400 bytes.

BASE -- Any valid address in RAM that is word aligned. Enter the value as a hex address. (Do not enter a leading **0x** before the **BASE** address) The default setting is **00000000.**

SIZE -- Any valid size that, when added to the **BASE** address, is not greater than **FFFFFFFE**. Enter the value in hex. (Do not enter a leading **0x** before the **SIZE** value.) The default setting is **8000**.

Step Over ISR (SOI)

CF SOI[YES, NO]

Use this option to step over an interrupt subroutine while stepping through code. The option determines what action is taken when an interrupt is detected.

YES -- The emulator will read the interrupt subroutine's return address from the stack frame and set a temporary breakpoint at that address. The status register interrupt level mask will be set to **7** and a **GO** command will be issued. When the breakpoint is hit, the status register will be restored to the value it held before the step. This sequence is repeated as many times as necessary while stepping to the desired code. Setting the option to **YES** will not disable interrupts. All interrupt subroutines will execute normally, though you will not step into them.

NO (default) -- The emulator will step into the interrupt subroutine if the interrupt level mask setting in the **Mask Interrupts While Stepping** (**CF SIL**) option is lower than the current interrupt level.

Target Console Redirection (TGTCONS)

CF TGTCONS [BDM, TGTCONS] (for Wind River ICE SX)

Use this option to set the target console setting. The default setting is **BDM**. The target console settings are used as follows:

Wind River Probe

Target Console Redirection is not currently supported for the Wind River Probe. You do not need to set this option.

Wind River ICE SX

BDM -- Use this setting to connect I/O on a target board, using the Transparent Mode Driver, to the target's BDM connector. When **BDM** is selected, the

Wind River ICE SX is in Transparent Mode, and all I/O data is redirected to the port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

For this type of connection to work, the target application must be linked to the Transparent Mode Driver. Refer to the Wind River *Transparent Mode Driver User's Manual* for more information.

TGTCONS -- Use this setting to connect a COM port on a target board to the TGTCONS port of a Wind River ICE SX. All I/O data is then redirected to port 1237 of the Wind River ICE's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

Target CPU (TAR)

CF TAR *target processor*

Use this option to configure the ColdFire CPU target type. For the emulator to function properly, this parameter must be configured to match the ColdFire processor type on your board. For example, to configure the emulator for a ColdFire 5206 target, type:

```
CF TAR 5206
```

Wait to Enter Background Mode (FRZ)

CF FRZ [1...600]

Use this option to set a delay, in milliseconds, for the emulator to wait between the time that the RESET# signal on the 26/30 pin BDM connector goes high and checking to see if the ColdFire processor is in background mode. This occurs during initialization as a result of an **IN** or **INN** command. This delay setting can be specified from 1 to 600. The delay setting is multiplied by 100, which will produce a delay of 100 to 60000 milliseconds, respectively. The default setting is **1**.

The ColdFire processor target board may have some reset logic between the RESET# signal on the 26/30 Pin BDM connector and the RSTI# signal pin on the ColdFire processor. Consequently, the RESET# signal from the 26/30 Pin BDM connector could be an input to the reset logic while the RSTI# signal to the ColdFire processor could be an output from the reset logic. If there is a delay between the reset logic input signal RESET# going high and the reset logic output signal RSTI#

going high, the emulator will think that the RSTI# signal has gone high prematurely. If this happens, the emulator will not see the PST[0:3] signals go high immediately after the RESET# signal goes high, since the ColdFire processor is really still being held in reset by the RSTI# signal. This will cause the emulator to think the target did not go into background mode, and the emulator will enter **>ERR>** mode. By setting **CF FRZ** to a higher value, you can add a delay after the RESET# signal is detected as going high, but before the emulator checks the PST[0:3] signals for the all-high state to see if it is in background mode.

15.1 CF Options for Wind River Trace

ColdFire processors use several configuration options that are only available when connected to a Wind River Trace.

Acquire Trace on GO (TRCAQU)

CF TRCAQU [OFF, ON}

Use this option to configure how Wind River Trace starts to store trace information on a **GO** command.

When the target begins running code, Wind River Trace can either wait until an event occurs to start storing trace information, or it can start immediately.

When this option is set to **ON**, Wind River Trace starts acquiring trace information as soon as a **GO** command is issued, and does not stop until an event occurs to disable trace.

When this option is set to **OFF**, Wind River Trace does not begin acquiring trace information until an event occurs to turn trace on.

Clear Trace Buffer on GO (TRCCLR)

CF TRCCLR [YES, NO]

Use this option to control where to start saving trace data in the trace memory.

YES -- When a **GO** command is issued, all newly captured trace data will be stored starting at the first trace memory location. All previously stored trace data will be overwritten and lost.

NO -- When a **GO** command is issued, all newly captured trace data will be stored starting at the next trace memory location. Previously stored trace data will not be overwritten.

The default is **NO**.

Code Range (CR)

CF CR [**BASE** and **RANGE**]

Use this option to set the code range. The code range must be set accurately when the **CF TRCREPORT** option is set to **YES**. Use the code range settings **BASE** and **RANGE** to set the base address and the range from the base address that the code runs in, as follows:

BASE -- Any valid address from 0 to FFFFFFFE that is word aligned. Enter the **BASE** address in hex. Do not enter a leading **0x** with the address. The default setting is 00000000.

RANGE -- Any valid range that, when added to the **BASE** setting, is not greater than FFFFFFFE. Enter the **RANGE** value in hex. Do not enter a leading **0x** with the value. The default setting is 1000.

Emit Operands on DDATA Pins (TRCREPORT)

CF TRCREPORT [**NO**, **YES**]

Use this option to select whether or not the ColdFire processor will emit read and write memory operands on the DDATA pins. The default setting is **NO**. The Trace Report settings are as follows:

NO -- When a **GO** command is issued, the CSR register is not configured to force the processor to emit read and write memory operands on the DDATA pins.

YES -- When a **GO** command is issued, the CSR register will force the processor to emit read and write memory operands on the DDATA pins. The memory operands are captured in the trace memory and displayed in the trace as memory cycles. If this option is set to **YES**, then the Code Range (**CR**) CF Option must be accurately set.

16

ARM Processors

This chapter describes the configuration options available for ARM9, ARM11, and ARM Cortex processors.

Not all of these CF options apply to all target processors; in general, only applicable options will be visible for any given processor. Which options are visible also depends on whether you are using a Wind River Probe or Wind River ICE SX.

Cache Configuration File Name (CACHECONF)

CF CACHECONF [NONE, CUSTOM]

Use this option to specify the cache dll that should be used for the target core that is connected. The default setting is **arm9x0tcache.dll.** To specify a different dll, enter **CF CACHEFILE** *filename*.

Drive TReset Line (TRESET)

CF TRESET[OPENC, ACTIVE]

This parameter controls the logic applied to the **TRESET** signal on the target. Selecting **OPENC** uses an **open collector** approach in which the active driver is released by tri-stating the line and allowing conditioning resistors on the target to return the signal to the non-active state. Selecting **ACTIVE** in this option causes the emulator to drive the **TRESET** signal to both active and inactive states. This is sometimes required on targets in which the conditioning resistors cause excessive rise or fall time on the signal when returning to an inactive state. This excessive time can cause the processor to come out of reset in an incorrect state.

Emulator HRESET Command Control (CMDRST)

CF CMDRST[IN,RST,BOTH]

This configuration option is used for multicore debugging, and is used to define when the HRESET line is asserted during a reset. If the option is set to **BOTH**, any time an **IN** or a **RST** command is issued, all of the processors that are running are reset. If the option is set to **IN**, then all of the processors reset only when an **IN** command is issued. If a **RST** command is issued, only the processor that is being used is reset and the other ones are left running. If the option is set to **RST**, then all of the processors will reset if a **RST** command is issued. However, if an **IN** command is issued, only the processor that you are using will reset.

Emulator HRESET Control (HRESET)

CF HRESET[ENABLE, DISABLE]

This option determines whether the **HRESET** line is asserted when you issue an **IN** command. Selecting **ENABLE** asserts **HRESET**, and selecting **DISABLE** prevents **HRESET** from being asserted.

External Trigger In (TRGIN)

(Wind River ICE SX only)

CF TRGIN[OFF, LEVELHI, LEVELLO, EDGEHI, EDGELO]

This option sets the trigger input signal sense detection. When activated, **Trigger In** stops the target upon detection. **Trigger In** does not work with any events.

The following table explains the available settings for this option.

Table 16-1 **Trigger In Settings**

Setting	Explanation
OFF	Trigger signal detection is off.
LEVELHI	The trigger input level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger input level is set below 1.8 volts.

Table 16-1 **Trigger In Settings**

Setting	Explanation
EDGEHI	Configures the system to trigger on the rising edge of a pulse.
EDGELO	Configures the system to trigger on the falling edge of a pulse.

External Trigger Out (TRGOUT)

(Wind River ICE SX only)

CF TRGOUT[LEVELHI, LEVELLO, PULSEHI, PULSELO]

This option allows you to set the trigger output signal type and level. The following table explains the available settings for this option.

Table 16-2 **Trigger Out Settings**

Setting	Explanation
LEVELHI	The trigger output level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger output level is set below 1.8 volts.
PULSEHI	Trigger Out signal pin will be a pulse from LOW to HIGH and back to LOW when triggered.
PULSELO	Trigger Out signal pin will be a pulse from HIGH to LOW and back to HIGH when triggered.

Invalidate Instruction Cache on GO (INVCI)

CF INVCI[YES,NO]

This option controls whether the contents of the target processor's Instruction Cache are invalidated when you issue a **GO** command. Setting this option to **YES** causes the cache contents to be invalidated.

JTAG Clock Rate (MHz) (CLK)

CF CLK *value*

This option configures the rate at which debug commands are clocked to the target. The range of available *value*s is determined by the emulator you are using.

For the Wind River Probe, the range is [**0.025** .. **100**] and the default is **6**.

For the Wind River ICE SX, the range is [**0.5, 1, 3, 6, 12, 16**, **20**] and the default is **3**.

Little-endian Mode (LENDIAN)

CF LENDIAN[YES,NO]

This configuration value determines whether the debugger treats memory contents as little-endian (bits ordered 0..63) or big-endian (bits ordered 63..0.) This affects display and interpretation of opcodes in the debugger window, as well as the effects of symbolic manipulation of variables. Setting this option to **YES** means that little-endian is used; setting the option to **NO** means that big-endian is used.

Monitor Target Reset (RST)

CF RST[YES, NO]

This function continuously monitors the target reset signal. If a reset occurs, one of the following actions may be taken:

- **YES** - If a target reset occurs it is reported to the user and BDM control is lost.
- **NO** - If a target reset occurs it is ignored. This is normally used if the code contains a reset instruction, which causes a reset to the external hardware, but not reset the core.

By default, this option is set to **YES**. It should only be changed to **NO** if you have a RESET instruction in your code.

Project Register Configuration File Name (REGFILE)

CF REGFILE [NONE, CUSTOM]

Use this option to specify a **.reg** file for your project. The default setting is **NONE**.

To specify a **.reg** file, use the syntax **CF REGFILE** *filename.* For example, to specify the register file **ARM920T.reg** for an ARM920T target, enter

```
CF REGFILE ARM920T.reg
```

Real Time Preservation (RTP)

CF RTP[**YES, NO**]

When this option is enabled, real-time preservation allows the target to run without the emulator stopping the target inadvertently.

Reset and TRST Tied Together (TIED)

CF TIED [**YES, NO**]

TRST and ICERESET signals may be tied together. Some ARM targets do not bring the TRST and ICERESET lines to the JTAG connector; they tie them together and bring the combination out as a single Reset. This works with Wind River tools if you bring this Reset line to the HRST line on the JTAG connector and inform the firmware of the connection by setting this option to **YES**.

The default setting is **NO**.

Reset Pulse Length N*1ms (RPL)

CF RPL[**1..600**]

This configuration option allows you to adjust the duration of the assertion of the HRESET signal on the target board. The number you specify in this option is the number of milliseconds that HRESET is driven active on the target.

Set Breakpoint (SB)

CF SB[**SB,IHBC**]

This option remaps traditional software breakpoints to internal hardware breakpoints. It is set to Software Breakpoint (**SB**) by default. Setting it to **IHBC** means that all software breakpoints are translated to internal hardware breakpoints. This option is useful when you are debugging code out of Flash or PROM.

Setting this option to **IHBC** may cause limitations in the number of breakpoints that can be set, depending on the target processor.

Set WRS Work Space (WSPACE)

CF WSPACE[BASE and **SIZE]**

Flash programming requires a small amount of target RAM to program the flash algorithm. You must tell your emulator where writable RAM is located on your target for this purpose.

As part of the configuration process, the emulator will indicate exactly how much of the RAM workspace is required. Depending on the device family and type, this space is limited to under 2 KB. Note that more memory improves the speed of programming.

To configure the workspace for flash programming the parameters should be entered in hex, where **BASE** is the start address, and **SIZE** is the minimum bytes of target RAM required, as displayed in the **Flash Programmer** view. This command allocates memory on the target system that is used by the emulator for various functions, including flash programming.

Target Console Redirection (TGTCONS)

CF TGTCONS[TGTCONS, BDM]

Wind River Probe

Target Console Redirection is not currently supported for the Wind River Probe. You do not need to set this option.

Wind River ICE SX

This option is for use when the Wind River ICE SX is to be used on a network and accessed remotely.

BDM -- Use this setting to connect I/O on a target board, using the Transparent Mode Driver, to the target's BDM connector. When **BDM** is selected, the Wind River ICE SX is in Transparent Mode, and all I/O data is redirected to the port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

For this type of connection to work, the target application must be linked to the Transparent Mode Driver. Refer to the Wind River *Transparent Mode Driver User's Manual* for more information.

TGTCONS -- Use this setting to connect a COM port on a target board to the TGTCONS port of a Wind River ICE SX. All I/O data is then redirected to port 1237 of the Wind River ICE's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

Target CPU (TAR)

CF TAR *target processor*

This option allows you to configure the emulator for the target that you are using. *target processor* is the name of your processor. For example, to configure the emulator for an ARM920T target, type:

```
CF TAR ARM920T
```

Transparent Mode Driver (TMD)

CF TMD[ENABLE, DISABLE]

This command sets all of the configuration parameters that are required to use the Transparent Mode Driver (TMD). Select **ENABLE** to configure your system for use with the TMD, and **DISABLE** if you do not plan to use it.

Trap Exceptions (TRAP)

CF TRAP [0xDF..0x0 | YES | NO]

This option acts as a Trap Exception "vector catch" hex-mask. Set the corresponding 1-bit for each item trapped by the emulator -- [FIQ | IRQ | 0 | D_Abt | P_Abt | SWI | UND | RST].

0x00 or **NO** traps no exceptions; **YES** traps all exceptions.

Wind River recommends that you use the **YES** or **NO** arguments whnever you want an all-or-nothing setting.

Trigger In Filter (TRGINFILTER)

(Wind River ICE SX only)

CF TRGINFILTER[OFF,ON]

This option provides a filtering option for the Trigger In function. When set to **ON**, a detected signal is required for at least 2 clock periods, or 40ns. This option ensures that noise does not cause a trigger.

Trigger Out Mode (TRGOUTMODE)

(Wind River ICE SX only)

CF TRGOUTMODE[OFF, ONALLSTOPS, ONBREAKPOINT]

This option allows you to set the type of events that will cause a trigger output to occur.

OFF -- Trigger output is off.

ONALLSTOPS -- Triggers whenever the target stops running.

ONBREAKPOINT -- Triggers whenever a breakpoint is encountered.

Wait to Enter Background Mode N*1ms (FRZ)

CF FRZ [1...30]

This command sets the length of time that the system waits for the target to enter background mode before it times out. The **FRZ** command can be set between 1 and 30 ms. By default, the option is set to time out after 1 ms. Note that sometimes the response will be slow if an external device is the BUS master. If the timeout period expires, the emulator will report **Time Out Waiting for FREEZE**.

17

ARMX (XScale) Processors

This chapter describes the configuration options available for ARMX (XScale) IXP, IOP, and PXA processors.

Not all of these CF options apply to all target processors; in general, only applicable options will be visible for any given processor. Which options are visible also depends on whether you are using a Wind River Probe or Wind River ICE SX.

Cache Configuration File Name (CACHEFILE)

CF CACHEFILE [NONE, CUSTOM]

Use this option to specify the cache dll that should be used for the target core that is connected. The default setting is **cachexscale.dll.** To specify a different dll, enter **CF CACHEFILE** *filename*.

Catch Vector Update Breakpoint (0x1234) (CATCHBKPT)

CF CATCHBKPT [YES, NO]

Setting this option to **YES** means the emulator will only catch breakpoint instructions while the core is running.

Disable OS Timers on Breakpoint Entry (TCTRL)

(IXP processors only)

CF TCTRL [YES, NO]

Use this option to select the firmware to stop the OS timers when the emulator enters Background Debug Mode as a result of a breakpoint instruction. The default setting is **NO**. Note that there will be some latency from detecting the breakpoint to disabling the timers.

Drive TReset Line (TRESET)

CF TRESET[OPENC, ACTIVE]

This parameter controls the logic applied to the **TRESET** signal on the target. Selecting **OPENC** uses an **open collector** approach in which the active driver is released by tri-stating the line and allowing conditioning resistors on the target to return the signal to the non-active state. Selecting **ACTIVE** in this option causes the emulator to drive the **TRESET** signal to both active and inactive states. This is sometimes required on targets in which the conditioning resistors cause excessive rise or fall time on the signal when returning to an inactive state. This excessive time can cause the processor to come out of reset in an incorrect state.

Emulator HRESET Control (HRESET)

CF HRESET[ENABLE, DISABLE]

This option determines whether the **HRESET** line is asserted when you issue an **IN** command. Selecting **ENABLE** asserts **HRESET**, and selecting **DISABLE** prevents **HRESET** from being asserted.

External Trigger In (TRGIN)

(Wind River ICE SX only)

CF TRGIN[OFF, LEVELHI, LEVELLO, EDGEHI, EDGELO]

This option sets the trigger input signal sense detection. When activated, a Trigger In signal stops the target upon detection. Trigger In does not work with any events.

The following table describes the available settings for this option.

Table 17-1 **Trigger In Settings**

Setting	Description
OFF	Trigger signal detection is off.
LEVELHI	The trigger input level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger input level is set below 1.8 volts.
EDGEHI	Configures the system to trigger on the rising edge of a pulse.
EDGELO	Configures the system to trigger on the falling edge of a pulse.

External Trigger Out (TRGOUT)

(Wind River ICE SX only)

CF TRGOUT[LEVELHI, LEVELLO, PULSEHI, PULSELO]

This option allows you to set the trigger output signal type and level. The following table describes the available settings for this option.

Table 17-2 **Trigger Out Settings**

Setting	Description
LEVELHI	The trigger output level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger output level is set below 1.8 volts.
PULSEHI	Trigger Out signal pin will be a pulse from LOW to HIGH and back to LOW when triggered.
PULSELO	Trigger Out signal pin will be a pulse from HIGH to LOW and back to HIGH when triggered.

Invalidate Instruction Cache on GO (INVCI)

CF INVCI[YES,NO]

This option controls whether the contents of the target processor's Instruction Cache are invalidated when you issue a **GO** command. Setting this option to **YES** causes the cache contents to be invalidated.

Internally Trap All Exceptions (INTRAP)

CF INTRAP [YES, NO, CUSTOM]

Use this option to configure the number of times you want the emulator to internally trap exceptions before reporting them. For example, when using VxWorks the number is typically 3. To set the value for VxWorks, enter

```
CF INTRAP 3
```

JTAG Clock Rate (MHz) (CLK)

CF CLK[0.5, 1, 3, 6, 12, 16]

This option configures the rate at which debug commands are clocked to the target. The default setting is **12**.

Little-endian Mode (LENDIAN)

CF LENDIAN[YES,NO]

This configuration value determines whether the debugger treats memory contents as little-endian (bits ordered 0..63) or big-endian (bits ordered 63..0.) This affects display and interpretation of opcodes in the debugger window, as well as the effects of symbolic manipulation of variables. Setting this option to **YES** means that little-endian is used; setting the option to **NO** means that big-endian is used.

Monitor Target Reset (RST)

CF RST[YES, RUN, HALT]

This function continuously monitors the target reset signal. If a reset occurs, one of the following actions may be taken:

- **YES** - If a target reset occurs it is reported to the user and BDM control is lost.
- **RUN** - If the reset occurs in this mode the target is restarted and BDM control is maintained.
- **HALT** - If the reset occurs in this mode the target is trapped at the restart vector.

Preserve PCI Bridge Setup Across Reset (BRIDGE)

CF BRIDGE [YES, NO]

If you have configured a PCI bridge on your target, setting this option to **YES** captures the data so you will not have to re-initialize the bridge after a reset.

Project Register Configuration File Name (REGFILE)

CF REGFILE [NONE, CUSTOM]

Use this option to specify a register file for your project. The default setting is **NONE**.

To specify a register file, use the syntax **CF REGFILE** *filename.* For example, to specify the register file **IXP425.reg** for an ARMX XScale IXP425 target, enter

```
CF REGFILE IXP425.reg
```


RAM Size to Scrub (SCRUB)

CF SCRUB [NONE, 0, 32, 64, 128, 256, 512]

This option is only needed for ECC Memory. If your target is using ECC memory, the emulator will need to set an area of memory to **0x0** before downloading any code.

Use this option to specify the size of the memory region to be scrubbed. When selected, all memory in the specified region is set to **0x0**.

The default setting is **NONE**.

Real Time Preservation (RTP)

CF RTP[YES,NO]

When this option is enabled, real-time preservation allows the target to run without the emulator stopping the target inadvertently.

Set Breakpoint (SB)

CF SB[SB,IHBC]

This option remaps traditional software breakpoints to internal hardware breakpoints. It is set to Software Breakpoint (**SB**) by default. Setting it to **IHBC** means that all software breakpoints are translated to internal hardware breakpoints. This option is useful when you are debugging code out of Flash or PROM.

Setting this option to **IHBC** may cause limitations in the number of breakpoints that can be set, depending on the target processor.

Set Debug Handler Virtual Address (DHVA)

CF DHVA *address*

Use this option to set the virtual address of the debug handler. The default setting is 0x800000.

Set Stack Range (STACK)

CF STACK[OFF / LOWER and UPPER]

This setting is **OFF** by default. When stack limits are set, it prevents the emulator from walking through the stack, past the specified range, and causing accidental bus errors.

Set WRS Work Space (WSPACE)

CF WSPACE[BASE and **SIZE]**

Flash programming requires a small amount of target RAM to program the flash algorithm. You must tell your emulator where writable RAM is located on your target for this purpose.

As part of the configuration process, the emulator will indicate exactly how much of the RAM workspace is required. Depending on the device family and type, this space is limited to under 2 KB. Note that more memory improves the speed of programming.

To configure the workspace for flash programming the parameters should be entered in hex, where **BASE** is the start address, and **SIZE** is the minimum bytes of target RAM required, as displayed in the **Flash Programmer** view. This command allocates memory on the target system that is used by the emulator for various functions, including flash programming.

Software Trace Mode (TRACE)

CF TRACE [OFF, ENABLE_WRAP, ENABLE_FILL]

OFF -- Software trace is disabled.

ENABLE_WRAP -- In this mode, the contents of the trace buffer will wrap, meaning that the trace will only display the code flow captured in the current buffer, regardless of where it is in the execution.

ENABLE_FILL -- In this mode, when the trace buffer is full, the target generates an interrupt, allowing the emulator to dump the contents of the buffer to a separate memory space. This allows you to preserve the entire trace (the limit being that once the buffer in the emulator fills, it will wrap.)

Target Console Redirection (TGTCONS)

CF TGTCONS [TGTCONS, JTAG] (for the Wind River ICE SX)

Wind River Probe

Target Console Redirection is not currently supported for the Wind River Probe. You do not need to set this option.

Wind River ICE SX

JTAG -- Use this setting to connect I/O on a target board, using the Transparent Mode Driver, to the target's JTAG connector. When **JTAG** is selected, the Wind River ICE SX is in Transparent Mode, and all I/O data is redirected to the port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

For this type of connection to work, the target application must be linked to the Transparent Mode Driver. Refer to the Wind River *Transparent Mode Driver User's Manual* for more information.

TGTCONS -- Use this setting to connect a COM port on a target board to the TGTCONS port of a Wind River ICE SX. All I/O data is then redirected to port 1237 of the Wind River ICE's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

Target CPU (TAR)

CF TAR *target processor*

This option allows you to configure the emulator for the target that you are using. *target processor* is the name of your processor. For example, to configure the emulator for an ARMX XScale IXP425 target, type:

```
CF TAR IXP425
```

Transparent Mode Driver (TMD)

CF TMD[ENABLE, DISABLE]

This command sets all of the configuration parameters that are required to use the Transparent Mode Driver (TMD). Select **ENABLE** to configure your system for use with the TMD, and **DISABLE** if you do not plan to use it.

Trap Exceptions (TRPEXP)

CF TRPEXP [YES, NO, CUSTOM]

This option allows you to configure which run time exceptions are trapped.

YES -- The emulator will trap all exceptions.

NO -- The emulator will ignore all exceptions.

CUSTOM -- This setting acts as a Trap Exception hex-mask. Set the corresponding 1-bit for each item trapped by the emulator --
[FIQ | IRQ | 0 | D_Abt | P_Abt | SWI | UND | RST].

0x00 traps no exceptions; **0xDF** traps all exceptions.

Trigger In Filter (TRGINFILTER)

(Wind River ICE SX only)

CF TRGINFILTER[OFF,ON]

This option provides a filtering option for the Trigger In function. When set to **ON**, a detected signal is required for at least 2 clock periods, or 40ns. This option ensures that noise does not cause a trigger.

Trigger In Mode (TRGINMODE)

(Wind River ICE SX only)

CF TRGINMODE[AUTO, BOTH]

This option allows users to determine where the trigger input signal sense detection come from when Wind River Trace is being used. When set to **AUTO**, the system automatically detects whether the source of the **TRGIN** is from the Wind River ICE SX or the Wind River Trace. When set to **BOTH**, the system will accept **TRGIN**s from both Wind River ICE SX and Wind River Trace. By default, this option is set to **AUTO**.

Trigger Out Mode (TRGOUTMODE)

(Wind River ICE SX only)

CF TRGOUTMODE[OFF, ONALLSTOPS, ONBREAKPOINT]

This option allows you to set the type of events that will cause a trigger output to occur.

OFF -- Trigger output is off.

ONALLSTOPS -- Triggers whenever the target stops running.

ONBREAKPOINT -- Triggers whenever a breakpoint is encountered.

Wait to Enter Background Mode N*100ms (FRZ)

CF FRZ [0...100]

This command sets the length of time that the system waits for the target to enter background mode before it times out. The option can be set between 0 and 100 ms. By default, the option is set to time out after 0 ms. Note that sometimes the response will be slow if the BUS master is an external device. If the timeout period expires, the emulator will report **Time Out Waiting for FREEZE.**

Wait to Release HOLD_RST Bit N*1000ms (HOLD_RST)

CF HOLD_RST [0..1000]

This command sets an additional length of time that the emulator will hold the target's internal **HOLD_RST** bit before releasing it. This is needed when the target is being used as a PCI Slave device and the emulator has no control over the PCI Reset to the target.

18

MIPS32 Processors

This chapter describes the configuration options available for MIPS32 processors. Supported processors include the MTI 4Kc, 4Kp, 4Km, and 4Kec, as well as IDT, Philips, Broadcom, and Alchemy processors.

Not all of these CF options apply to all target processors; in general, only applicable options will be visible for any given processor. Which options are visible also depends on whether you are using a Wind River Probe or Wind River ICE SX.

BDM Clock Rate (CLK)

CF CLK [0.1, 0.5, 1, 3, 6, 12, 16]

This option configures the rate at which debug commands are clocked to the target. The default setting is **16**.

Check ROCC Bit During Reset (ROCC)

CF ROCC [YES, NO]

When this option is set to **YES**, the emulator will monitor/clear the Reset Occurred (ROCC) bit during resets.

Delay After Reset (DRST)

CF DRST[0..1000]

This option allows you to modify the delay after the release of **HRESET**. Delay can be set in milliseconds.

Download Mode (DLD)

CF DLD [NORMAL, INTRUSIVE]

Use this option to configure Port/Bus/Size/width of memory transfers when downloading.

NORMAL -- Port/Bus/Size/width of memory transfers when downloading is typical for the target being used.

INTRUSIVE -- Pre-loads target handshaking procedure code co-executed during all downloads to improve performance.

Drive TReset Line (TRESET)

CF TRESET[OPENC, ACTIVE]

This parameter controls the logic applied to the **TRESET** signal on the target. Selecting **OPENC** uses an **open collector** approach in which the active driver is released by tri-stating the line and allowing conditioning resistors on the target to return the signal to the non-active state. Selecting **ACTIVE** in this option causes the emulator to drive the **TRESET** signal to both active and inactive states. This is sometimes required on targets in which the conditioning resistors cause excessive rise or fall time on the signal when returning to an inactive state. This excessive time can cause the processor to come out of reset in an incorrect state.

EJTAG Handshaking During Download (DLDHSHG)

CF DLDHSHG [YES, NO]

Set this option to **YES** to enable full handshaking of EJTAG communication protocol for each data set transferred during the download.

Set this option to **NO** (the default) to disable full handshaking of EJTAG communication protocol for each data set transferred during the download.

Emulator ECR Reset Control (ECRRST)

CF ECRRST [DISABLE, PRRST, PERRST, BOTH]

Use this option to control what gets reset when you are opening a connection to the target. The option sets selected bits in the EJTAG control register.

The settings are as follows:

DISABLE -- Reset only the EJTAG controller.

PRRST -- Reset the EJTAG controller and the processor.

PERRST -- Reset the EJTAG controller and the core peripherals.

BOTH -- Reset the EJTAG controller, the processor, and the core peripherals.

Emulator HRESET Command Control (CMDRST)

CF CMDRST [IN, RST, BOTH]

When your Wind River ICE SX is connected to a multi-core target, and **CF HRESET** is set to **ENABLE**, use this option to select the reset action for all cores when issuing an **IN** or **RST** command to a single core.

If **IN** is selected on a single core, then an **IN** command to that core will reset all target cores.

If **RST** is selected on a single core, then an **RST** command to that core will reset all target cores.

Setting this option to **BOTH** will cause either an **IN** or **RST** command to reset all cores.

Emulator HRESET Control (HRESET)

CF HRESET[ENABLE, DISABLE]

This option determines whether the **HRESET** line is asserted when you issue an **IN** command. Selecting **ENABLE** asserts **HRESET**, and selecting **DISABLE** prevents **HRESET** from being asserted.

Exception Vector Table Location (VECTOR)

CF VECTOR [NORMAL, BOOTSTRAP]

Use this option to control the location of the exception handler vector table in MIPS64 processors.

NORMAL -- The exception vector table is expected to be located in RAM starting at 0x80000000.

BOOTSTRAP -- The exception vector table is expected to be found in the boot ROM area starting at 0xBFC00200.

External Trigger In (TRGIN)

(Wind River ICE SX only)

CF TRGIN [OFF, LEVELHI, LEVELLO, EDGEHI, EDGELO]

This option sets the trigger input signal sense detection. When activated, **Trigger In** stops the target upon detection. **Trigger In** does not work with any events.

The following table describes the available settings for this option.

Table 18-1 **Trigger In Settings**

Setting	Description
OFF	Trigger signal detection is off.
LEVELHI	The trigger input level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger input level is set below 1.8 volts.
EDGEHI	Configures the system to trigger on the rising edge of a pulse.
EDGELO	Configures the system to trigger on the falling edge of a pulse.

External Trigger Out (TRGOUT)

(Wind River ICE SX only)

CF TRGOUT[LEVELHI, LEVELLO, PULSEHI, PULSELO]

This option allows you to set the trigger output signal type and level. The following table describes the available settings for this option.

Table 18-2 **Trigger Out Settings**

Setting	Description
LEVELHI	The trigger output level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger output level is set below 1.8 volts.
PULSEHI	Trigger Out signal pin will be a pulse from LOW to HIGH and back to LOW when triggered.
PULSELO	Trigger Out signal pin will be a pulse from HIGH to LOW and back to HIGH when triggered.

Idle Time Between Processor Accesses (N*32 tck) (ITPA)

CF ITPA [0..5]

Use this option to specify the time the emulator remains idle before accessing the target processor.

Invalidate Cache When Initialize (INVCA)

CF INVCA [YES, NO]

This option controls whether the contents of the target processor's instruction cache are invalidated when you issue an **IN** command. Setting this option to **YES** causes the cache contents to be invalidated. This option applies only to the **IN** command, not the **INN** or **INE** commands.

Little-endian Mode (LENDIAN)

CF LENDIAN[YES,NO]

This configuration value determines whether the debugger treats memory contents as little-endian (bits ordered 0..63) or big-endian (bits ordered 63..0.) This affects display and interpretation of opcodes in the debugger window, as well as the effects of symbolic manipulation of variables. Setting this option to **YES** means that little-endian is used; setting the option to **NO** means that big-endian is used.

Load Boot Table on IN (BL)

CF BL [ENABLE, DISABLE]

This option enables or disables the Linux bootline commands. The default is **DISABLE**. You should only set this option to **ENABLE** if the **CF MMU** option is set to **ENABLE**.

Memory Management Unit (MMU)

CF MMU [ENABLE, DISABLE]

Use this option to enable or disable the Linux Memory Management Unit.

Monitor Target Reset (RST)

CF RST[YES, NO, HALT, RUN]

This function continuously monitors the target reset signal. If a reset occurs, one of the following actions may be taken:

- **YES** - If a target reset occurs it is reported to the user and BDM control is lost.
- **NO** - If a target reset occurs it is ignored. This is normally used if the code contains a reset instruction, which causes a reset to the external hardware, but not reset the core.
- **HALT** - If the reset occurs in this mode the target is trapped at the restart vector.
- **RUN** - If the reset occurs in this mode the target is restarted and BDM control is maintained.

By default, this option is set to **YES**. It should only be changed to **NO** if you have a RESET instruction in your code.

Processor Mode (MODE)

CF MODE[32,64]

This parameter determines the operational mode of the processor. The processor can run in a 32-bit or a 64-bit memory mode, depending on the implementation on a target. This parameter compensates for the processor mode in memory accesses to ensure that the correct accesses are made for any given command.

Reset Pulse Length N*1ms (RPL)

CF RPL[0..600]

This configuration option allows you to adjust the duration of the assertion of the HRESET signal on the target board. The number you specify in this option is the number of milliseconds that HRESET is driven active on the target.

Set Breakpoint (SB)

CF SB[SB,IHBC]

This option remaps traditional software breakpoints to internal hardware breakpoints. It is set to Software Breakpoint (**SB**) by default. Setting it to **IHBC** means that all software breakpoints are translated to internal hardware breakpoints. This option is useful when you are debugging code out of Flash or PROM.

Set Stack Range (STACK)

CF STACK[OFF / LOWER and UPPER]

This setting is **OFF** by default. When stack limits are set, it prevents the emulator from walking through the stack, past the specified range, and causing accidental bus errors.

Set Work Space (WSPACE)

CF WSPACE[BASE and **SIZE]**

Flash programming requires a small amount of target RAM to program the flash algorithm. You must tell your emulator where writable RAM is located on your target for this purpose.

As part of the configuration process, the emulator will indicate exactly how much of the RAM workspace is required. Depending on the device family and type, this space is limited to under 2 KB. Note that more memory improves the speed of programming.

To configure the workspace for flash programming the parameters should be entered in hex, where **BASE** is the start address, and **SIZE** is the minimum bytes of target RAM required, as displayed in the **Flash Programmer** view. This command allocates memory on the target system that is used by the emulator for various functions, including flash programming.

Step in Delayed Slot (SIDS)

CF SIDS [YES, NO]

Jump and branch instructions change the control flow of a program. The instruction immediately following the jump or branch is known as the instruction in the delay slot. All jump and branch instructions occur with a delay of one instruction; that is, the instruction in the delay slot always executes while the target instruction is being fetched from storage.

YES -- On each single step through assembly code, the instruction in the delay slot will be stepped before taking the jump.

NO -- On each single step through assembly code, the instruction in the delay slot will not be stepped before taking the jump.

Target Break Type (TGTBRK)

CF TGTBRK [EJTAGBRK, DINT]

Use this option to select the method your emulator will use to halt target execution. **EJTAGBRK** uses the BREAK bit in the EJTAG control register to halt the target. **DINT** uses a dedicated input pin to cause a DEBUG exception on those target CPUs that support this feature.

Target Console Redirection (TGTCONS)

CF TGTCONS [**TGTCONS**, **BDM**] (for the Wind River ICE SX)

Wind River Probe

Target Console Redirection is not currently supported for the Wind River Probe. You do not need to set this option.

Wind River ICE SX

BDM -- Use this setting to connect I/O on a target board, using the Transparent Mode Driver, to the target's BDM connector. When **BDM** is selected, the Wind River ICE SX is in Transparent Mode, and all I/O data is redirected to the port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

For this type of connection to work, the target application must be linked to the Transparent Mode Driver. Refer to the *Wind River Workbench On-Chip Debugging Guide: Using the WDB Transparent Mode Driver* for more information.

TGTCONS -- Use this setting to connect a COM port on a target board to the TGTCONS port of a Wind River ICE SX. All I/O data is then redirected to port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

Target CPU (TAR)

CF TAR *target processor*

This option allows you to configure the emulator for the target that you are using. *target processor* is the name of your processor. For example, to configure the emulator for a MIPS NEC VR4133 target, type:

```
CF TAR VR4133
```

Transparent Mode Driver (TMD)

CF TMD[ENABLE, DISABLE]

This command sets all of the configuration parameters that are required to use the Transparent Mode Driver (TMD). Select **ENABLE** to configure your system for use with the TMD, and **DISABLE** if you do not plan to use it.

Trap Debug Exception (TRPEXP)

CF TRPEXP[YES, NO, BREAKPOINTONLY]

This option allows you to configure which run time exceptions are trapped. Setting this option to **YES** causes the emulator to trap RST, CHSTP, MCI, ALI, TRE, SEI, LBRK, IBRK, EBRK, and DPI exceptions. Setting it to **NO** causes the emulator not to trap any exceptions other than TRE and SE. Setting the option to **BREAKPOINTONLY** causes the emulator to trap exceptions only when a breakpoint is encountered.

Trigger In Filter Mode (TRGINFILTER)

(Wind River ICE SX only)

CF TRGINFILTER[OFF,ON]

This option provides a filtering option for the Trigger In function. When set to **ON**, a detected signal is required for at least 2 clock periods, or 40ns. This option ensures that noise does not cause a trigger.

Trigger Out Mode (TRGOUTMODE)

(Wind River ICE SX only)

CF TRGOUTMODE[OFF, ONALLSTOPS, ONBREAKPOINT]

This option allows you to set the type of events that will cause a trigger output to occur.

OFF -- Trigger output is off.

ONALLSTOPS -- Triggers whenever the target stops running.

ONBREAKPOINT -- Triggers whenever a breakpoint is encountered.

Use Current MMU Settings (USEERL)

CF USEERL [YES, NO]

YES -- The emulator bypasses the user application TLB definition to access memory.

NO -- The emulator uses the user application TLB definition to access memory.

19

MIPS64 Processors

This chapter describes the configuration options available for MIPS64 processors. Supported processors include the MTI 5Kc, 5Kf, and 20Kc, as well as Toshiba, PMC-Sierra, and NEC VR processors.

Not all of these CF options apply to all target processors; in general, only applicable options will be visible for any given processor. Which options are visible also depends on whether you are using a Wind River Probe or Wind River ICE SX.

BDM Clock Rate (CLK)

CF CLK [0.1, 0.5, 1, 3, 6, 12, 16]

This option configures the rate at which debug commands are clocked to the target. The default setting is **16**.

Check ROCC Bit During Reset (ROCC)

CF ROCC [YES, NO]

When this option is set to **YES**, the emulator will monitor/clear the Reset Occurred (ROCC) bit during resets.

Delay After Reset (DRST)

CF DRST[0..1000]

This option allows you to modify the delay after the release of **HRESET**. Delay can be set in milliseconds, from 0 to 1000.

Download Mode (DLD)

CF DLD [NORMAL, INTRUSIVE]

Use this option to configure Port/Bus/Size/width of memory transfers when downloading.

NORMAL -- Port/Bus/Size/width of memory transfers when downloading is typical for the target being used.

INTRUSIVE -- Pre-loads target handshaking procedure code co-executed during all downloads to improve performance.

Drive TReset Line (TRESET)

CF TRESET[OPENC, ACTIVE]

This parameter controls the logic applied to the **TRESET** signal on the target. Selecting **OPENC** uses an **open collector** approach in which the active driver is released by tri-stating the line and allowing conditioning resistors on the target to return the signal to the non-active state. Selecting **ACTIVE** in this option causes the emulator to drive the **TRESET** signal to both active and inactive states. This is sometimes required on targets in which the conditioning resistors cause excessive rise or fall time on the signal when returning to an inactive state. This excessive time can cause the processor to come out of reset in an incorrect state.

Emulator HRESET Command Control (CMDRST)

CF CMDRST [IN, RST, BOTH]

When your Wind River ICE SX is connected to a multi-core target, and **CF HRESET** is set to **ENABLE**, use this option to select the reset action for all cores when issuing an **IN** or **RST** command to a single core.

If **IN** is selected on a single core, then an **IN** command to that core will reset all target cores.

If **RST** is selected on a single core, then an **RST** command to that core will reset all target cores.

Setting this option to **BOTH** will cause either an **IN** or **RST** command to reset all cores.

Emulator HRESET Control (HRESET)

CF HRESET[ENABLE, DISABLE]

This option determines whether the **HRESET** line is asserted when you issue an **IN** command. Selecting **ENABLE** asserts **HRESET**, and selecting **DISABLE** prevents **HRESET** from being asserted.

Exception Vector Table Location (VECTOR)

CF VECTOR [NORMAL, BOOTSTRAP]

Use this option to control the location of the exception handler vector table in MIPS64 processors.

NORMAL -- The exception vector table is expected to be located in RAM starting at 0x80000000.

BOOTSTRAP -- The exception vector table is expected to be found in the boot ROM area starting at 0xBFC00200.

External Trigger In (TRGIN)

(Wind River ICE SX only)

CF TRGIN[OFF, LEVELHI, LEVELLO, EDGEHI, EDGELO]

This option sets the trigger input signal sense detection. When activated, **Trigger In** stops the target upon detection. **Trigger In** does not work with any events.

The following table describes the available settings for this option.

Table 19-1 **Trigger In Settings**

Setting	Description
OFF	Trigger signal detection is off.
LEVELHI	The trigger input level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger input level is set below 1.8 volts.
EDGEHI	Configures the system to trigger on the rising edge of a pulse.
EDGELO	Configures the system to trigger on the falling edge of a pulse.

External Trigger Out (TRGOUT)

(Wind River ICE SX only)

CF TRGOUT[LEVELHI, LEVELLO, PULSEHI, PULSELO]

This option allows you to set the trigger output signal type and level. The following table describes the available settings for this option.

Table 19-2 **Trigger Out Settings**

Setting	Description
LEVELHI	The trigger output level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger output level is set below 1.8 volts.
PULSEHI	Trigger Out signal pin will be a pulse from LOW to HIGH and back to LOW when triggered.
PULSELO	Trigger Out signal pin will be a pulse from HIGH to LOW and back to HIGH when triggered.

Invalidate Cache When Initialize (INVCA)

CF INVCA [YES, NO]

This option controls whether the contents of the target processor's instruction cache are invalidated when you issue an **IN** command. Setting this option to **YES** causes the cache contents to be invalidated. This option applies only to the **IN** command, not the **INN** or **INE** commands.

Little-endian Mode (LENDIAN)

CF LENDIAN[YES,NO]

This configuration value determines whether the debugger treats memory contents as little-endian (bits ordered 0..63) or big-endian (bits ordered 63..0.) This affects display and interpretation of opcodes in the debugger window, as well as the effects of symbolic manipulation of variables. Setting this option to **YES** means that little-endian is used; setting the option to **NO** means that big-endian is used.

Load Boot Table on IN (BL)

CF BL [ENABLE, DISABLE]

This option enables or disables the Linux bootline commands. The default is **DISABLE**. You should only set this option to **ENABLE** if the **CF MMU** option is set to **LINUX**.

Memory Management Unit (MMU)

CF MMU [OFF, LINUX, VXWORKS]

Use this option to enable or disable the Linux or VxWorks Memory Management Unit.

Monitor Target Reset (RST)

CF RST[YES, NO, HALT, RUN]

This function continuously monitors the target reset signal. If a reset occurs, one of the following actions may be taken:

- **YES** - If a target reset occurs it is reported to the user and BDM control is lost.
- **NO** - If a target reset occurs it is ignored. This is normally used if the code contains a reset instruction, which causes a reset to the external hardware, but not reset the core.
- **HALT** - If the reset occurs in this mode the target is trapped at the restart vector.
- **RUN** - If the reset occurs in this mode the target is restarted and BDM control is maintained.

By default, this option is set to **YES**. It should only be changed to **NO** if you have a RESET instruction in your code.

Reset Pulse Length N*1ms (RPL)

CF RPL[0..600]

This configuration option allows you to adjust the duration of the assertion of the HRESET signal on the target board. The number you specify in this option is the number of milliseconds that HRESET is driven active on the target.

Set Breakpoint (SB)

CF SB[SB,IHBC]

This option remaps traditional software breakpoints to internal hardware breakpoints. It is set to Software Breakpoint (**SB**) by default. Setting it to **IHBC** means that all software breakpoints are translated to internal hardware breakpoints. This option is useful when you are debugging code out of Flash or PROM.

Set Stack Range (STACK)

CF STACK[OFF / LOWER and UPPER]

This setting is **OFF** by default. When stack limits are set, it prevents the emulator from walking through the stack, past the specified range, and causing accidental bus errors.

Set Work Space (WSPACE)

CF WSPACE[BASE and **SIZE]**

Flash programming requires a small amount of target RAM to program the flash algorithm. You must tell your emulator where writable RAM is located on your target for this purpose.

As part of the configuration process, the emulator will indicate exactly how much of the RAM workspace is required. Depending on the device family and type, this space is limited to under 2 KB. Note that more memory improves the speed of programming.

To configure the workspace for flash programming the parameters should be entered in hex, where **BASE** is the start address, and **SIZE** is the minimum bytes of target RAM required, as displayed in the **Flash Programmer** view. This command allocates memory on the target system that is used by the emulator for various functions, including flash programming.

Step in Delayed Slot (SIDS)

CF SIDS [YES, NO]

Jump and branch instructions change the control flow of a program. The instruction immediately following the jump or branch is known as the instruction in the delay slot. All jump and branch instructions occur with a delay of one instruction; that is, the instruction in the delay slot always executes while the target instruction is being fetched from storage.

YES -- On each single step through assembly code, the instruction in the delay slot will be stepped before taking the jump.

NO -- On each single step through assembly code, the instruction in the delay slot will not be stepped before taking the jump.

Target Break Type (TGTBRK)

CF TGTBRK [EJTAGBRK, DINT]

Use this option to select the method your emulator will use to halt target execution. **EJTAGBRK** uses the BREAK bit in the EJTAG control register to halt the target. **DINT** uses a dedicated input pin to cause a DEBUG exception on those target CPUs that support this feature.

Target Console Redirection (TGTCONS)

CF TGTCONS [**TGTCONS**, **BDM**] (for the Wind River ICE SX)

Wind River Probe

Target Console Redirection is not currently supported for the Wind River Probe. You do not need to set this option.

Wind River ICE SX

BDM -- Use this setting to connect I/O on a target board, using the Transparent Mode Driver, to the target's BDM connector. When **BDM** is selected, the Wind River ICE SX is in Transparent Mode, and all I/O data is redirected to the port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

For this type of connection to work, the target application must be linked to the Transparent Mode Driver. Refer to the *Wind River Workbench On-Chip Debugging Guide: Using the WDB Transparent Mode Driver* for more information.

TGTCONS -- Use this setting to connect a COM port on a target board to the TGTCONS port of a Wind River ICE SX. All I/O data is then redirected to port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

Target CPU (TAR)

CF TAR *target processor*

This option allows you to configure the emulator for the target that you are using. *target processor* is the name of your processor. For example, to configure the emulator for a MIPS NEC VR4133 target, type:

```
CF TAR VR4133
```

Transparent Mode Driver (TMD)

CF TMD[ENABLE, DISABLE]

This command sets all of the configuration parameters that are required to use the Transparent Mode Driver (TMD). Select **ENABLE** to configure your system for use with the TMD, and **DISABLE** if you do not plan to use it.

Trap Debug Exception (TRPEXP)

CF TRPEXP[YES, NO, BREAKPOINTONLY]

This option allows you to configure which run time exceptions are trapped. Setting this option to **YES** causes the emulator to trap RST, CHSTP, MCI, ALI, TRE, SEI, LBRK, IBRK, EBRK, and DPI exceptions. Setting it to **NO** causes the emulator not to trap any exceptions other than TRE and SE. Setting the option to **BREAKPOINTONLY** causes the emulator to trap exceptions only when a breakpoint is encountered.

Trigger In Filter Mode (TRGINFILTER)

(Wind River ICE SX only)

CF TRGINFILTER[OFF,ON]

This option provides a filtering option for the Trigger In function. When set to **ON**, a detected signal is required for at least 2 clock periods, or 40ns. This option ensures that noise does not cause a trigger.

Trigger Out Mode (TRGOUTMODE)

(Wind River ICE SX only)

CF TRGOUTMODE[OFF, ONALLSTOPS, ONBREAKPOINT]

This option allows you to set the type of events that will cause a trigger output to occur.

OFF -- Trigger output is off.

ONALLSTOPS -- Triggers whenever the target stops running.

ONBREAKPOINT -- Triggers whenever a breakpoint is encountered.

Use Current MMU Settings (USEERL)

CF USEERL [YES, NO]

YES -- The emulator bypasses the user application TLB definition to access memory.

NO -- The emulator uses the user application TLB definition to access memory.

20

PWRficient Processors

This chapter describes the configuration options available for PWRficient integrated platform processors.

Not all of these CF options apply to all target processors; in general, only applicable options will be visible for any given processor. Which options are visible also depends on whether you are using a Wind River Probe or Wind River ICE SX.

Acquire Trace on GO (TRCAQU)

CF TRCAQU [OFF, ON}

Use this option to configure how Workbench software trace starts to store trace information.

When the target begins running code, Workbench can either wait until an event occurs to start storing trace information, or it can start immediately.

When this option is set to **ON**, Workbench starts acquiring trace information as soon as a **GO** command is issued, and does not stop until an event occurs to disable trace.

When this option is set to **OFF**, Workbench does not begin acquiring trace information until an event occurs to turn trace on.

Delay After Reset N*1ms (DRST)

CF DRST[0..100]

This option allows you to modify the delay between the release of **HRESET** and the first JTAG communication attempt. The default is **25**.

Drive TReset Line (TRESET)

CF TRESET[OPENC, ACTIVE]

This parameter controls the logic applied to the **TRESET** signal on the target. Selecting **OPENC** uses an **open collector** approach in which the active driver is released by tri-stating the line and allowing conditioning resistors on the target to return the signal to the non-active state. Selecting **ACTIVE** in this option causes the emulator to drive the **TRESET** signal to both active and inactive states. This is sometimes required on targets in which the conditioning resistors cause excessive rise or fall time on the signal when returning to an inactive state. This excessive time can cause the processor to come out of reset in an incorrect state.

Emulator HRESET Command Control (CMDRST)

(Wind River ICE SX only)

CF CMDRST [IN, RST, BOTH]

When your Wind River ICE SX is connected to a multi-core target, and **CF HRESET** is set to **ENABLE**, use this option to select the reset action for all cores when issuing an **IN** or **RST** command to a single core.

If **IN** is selected on a single core, then an **IN** command to that core will reset all target cores.

If **RST** is selected on a single core, then an **RST** command to that core will reset all target cores.

Setting this option to **BOTH** will cause either an **IN** or **RST** command to reset all cores.

Emulator HRESET Control (HRESET)

CF HRESET[ENABLE, DISABLE]

This option determines whether the **HRESET** line is asserted when you issue an **IN** command. Selecting **ENABLE** asserts **HRESET**, and selecting **DISABLE** prevents **HRESET** from being asserted.

Enable Physical Memory Access (MEMPHYSICAL)

CF MEMPHYSICAL [YES,NO]

When this option is set to **YES**, the emulator will access memory using the internal bus. When set to **NO**, the emulator will access memory using operation codes.

The default is **NO**.

Enable MBIST FPU Access (MBISTFPU)

CF MBISTFPU [YES,NO]

When this option is set to **YES**, the emulator will access floating-point unit (FPU) registers using the Memory Built-In Self-Test (MBIST) interface. When set to **NO**, the emulator will access FPU registers using operation codes.

The default is **NO**.

External Trigger In (TRGIN)

(Wind River ICE SX only)

CF TRGIN [OFF, LEVELHI, LEVELLO, EDGEHI, EDGELO]

This option sets the trigger input signal sense detection. When activated, **Trigger In** stops the target upon detection. **Trigger In** does not work with any events.

The following table describes the available settings for this option.

Table 20-1 **Trigger In Settings**

Setting	Description
OFF	Trigger signal detection is off.
LEVELHI	The trigger input level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger input level is set below 1.8 volts.
EDGEHI	Configures the system to trigger on the rising edge of a pulse.
EDGELO	Configures the system to trigger on the falling edge of a pulse.

External Trigger Out (TRGOUT)

(Wind River ICE SX only)

CF TRGOUT[LEVELHI, LEVELLO, PULSEHI, PULSELO]

This option allows you to set the trigger output signal type and level. The following table describes the available settings for this option.

Table 20-2 **Trigger Out Settings**

Setting	Description
LEVELHI	The trigger output level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger output level is set below 1.8 volts.
PULSEHI	Trigger Out signal pin will be a pulse from LOW to HIGH and back to LOW when triggered.
PULSELO	Trigger Out signal pin will be a pulse from HIGH to LOW and back to HIGH when triggered.

Invalidate Cache When Initialize (INVCA)

CF INVCA [YES, NO]

This option controls whether the contents of the target processor's instruction cache are invalidated when you issue an **IN** command. Setting this option to **YES** causes the cache contents to be invalidated. This option applies only to the **IN** command, not the **INN** or **INE** commands.

Issue an IN on Coldstart (INCOLD)

CF INCOLD[YES,NO]

This option configures the emulator boot sequence.

Set this option to **YES** to issue an **IN** command, which asserts a reset on the target during a boot sequence.

Set this option to **NO** to issue a **SYNC** command instead of asserting reset on the target. The **SYNC** command does not reset the board. It establishes JTAG communications and captures the current context. This option is best if you want to hot plug the emulator into a running target.

The default is **NO**.

JTAG Clock Rate (MHz) (CLK)

Wind River Probe

CF CLK[0.025...100]

Wind River ICE SX

CF CLK [0.025,0.5,1,3,6,12,16]

This option configures the rate at which debug commands are clocked to the target. The default setting is **16** for the Wind River Probe and **12** for the Wind River ICE SX.

Little-endian Mode (LENDIAN)

CF LENDIAN[YES,NO]

This configuration value determines whether the debugger treats memory contents as little-endian (bits ordered 0..63) or big-endian (bits ordered 63..0.) This affects display and interpretation of opcodes in the debugger window, as well as the effects of symbolic manipulation of variables. Setting this option to **YES** means that little-endian is used; setting the option to **NO** means that big-endian is used.

Load Boot Table on IN (BL)

CF BL [ENABLE, DISABLE]

This option enables or disables the Linux bootline commands.

MMU Support Control (MMU)

CF MMU[ENABLE, DISABLE]

This option controls physical to virtual address translation.

ENABLE -- Informs the emulator that addresses should be checked for virtual mapping.

DISABLE -- Addresses will not be checked for virtual mapping.

Monitor Target Reset (RST)

CF RST[YES, NO, HALT, RUN]

This function continuously monitors the target reset signal. If a reset occurs, one of the following actions may be taken:

- **YES** - If a target reset occurs it is reported to the user and BDM control is lost.
- **NO** - If a target reset occurs it is ignored. This is normally used if the code contains a reset instruction, which causes a reset to the external hardware, but not reset the core.
- **HALT** - If the reset occurs in this mode the target is trapped at the restart vector.
- **RUN** - If the reset occurs in this mode the target is restarted and BDM control is maintained.

By default, this option is set to **YES**. It should only be changed to **NO** if you have a RESET instruction in your code.

Power On Reset Length N*1ms (PONR)

CF PONR[0..500]

Some target designs implement reset logic that extends the duration of **HRESET** upon power up. This option allows you to specify the duration of the assertion of the reset signal so that the emulator knows when to expect the target to release the signal. The number specified can be between 0 and 500, and it represents the number of milliseconds to wait.

Real Time Preservation (RTP)

CF RTP[YES,NO]

When this option is enabled, real-time preservation allows the target to run without the emulator stopping the target inadvertently.

Reset Pulse Length N 1*ms (RPL)

CF RPL[1..9000]

This configuration option allows you to adjust the duration of the assertion of the HRESET signal on the target board. The number you specify in this option is the number of milliseconds that HRESET is driven active on the target.

Sense Power via HRESET (SPOWER)

CF SPOWER[YES,NO]

This option lets the hardware determine if power is applied to the target by monitoring the HRESET level when it is released. This prevents the hardware from trying to continue the initialization sequence if power is not applied to the target board.

Set Breakpoint (SB)

CF SB[SB,IHBC]

This option remaps traditional software breakpoints to internal hardware breakpoints. It is set to Software Breakpoint (**SB**) by default. Setting it to **IHBC** means that all software breakpoints are translated to internal hardware breakpoints. This option is useful when you are debugging code out of Flash or PROM.

Setting this option to **IHBC** may cause limitations in the number of breakpoints that can be set, depending on the target processor.

Set Stack Range (STACK)

CF STACK[OFF / LOWER and UPPER]

This setting is **OFF** by default. When stack limits are set, it prevents the emulator from walking through the stack, past the specified range, and causing accidental bus errors.

Set Work Space (WSPACE)

CF WSPACE[BASE and **SIZE]**

Flash programming requires a small amount of target RAM to program the Flash Algorithm. You must tell your emulator where writable RAM is located on your target for this purpose.

As part of the configuration process, the emulator will indicate exactly how much of the RAM workspace is required. Depending on the device family and type, this space is limited to under 2 KB. Note that more memory improves the speed of programming.

To configure the workspace for flash programming the parameters should be entered in hex, where **BASE** is the start address, and **SIZE** is the minimum bytes of target RAM required, as displayed in the **Flash Programmer** view. This command allocates memory on the target system that is used by the emulator for various functions, including flash programming.

Synchronized Halt (SYNCHALT)

CF SYNCHALT [YES,NO]

(Wind River ICE SX only)

Setting this option to **YES** sets the global debug-halt bit (GHALT).

This bit generates a debug-halt request to all cores whenever any core asserts its debug-halted bit (cNhst).

TMD Mode (TMD)

CF TMD[ENABLE, DISABLE]

This command sets all of the configuration parameters that are required to use the Transparent Mode Driver (TMD). Select **ENABLE** to configure your system for use with the TMD, and **DISABLE** if you do not plan to use it.

Target Console Redirection (TGTCONS)

CF TGTCONS [BDM, COM1, COM2] (for the Wind River ICE SX)

Wind River Probe

Target Console Redirection is not currently supported for the Wind River Probe. You do not need to set this option.

Wind River ICE SX

BDM -- Use this setting to connect I/O on a target board, using the Transparent Mode Driver, to the target's BDM connector. When **BDM** is selected, the Wind River ICE SX is in Transparent Mode, and all I/O data is redirected to the port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

For this type of connection to work, the target application must be linked to the Transparent Mode Driver. Refer to the *Wind River Workbench On-Chip Debugging Guide: Using the WDB Transparent Mode Driver* for more information.

COM1, COM2-- Use these settings to connect a COM port on a target board to the TGTCONS port of a Wind River ICE SX. All I/O data is then redirected to port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O

data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

Target CPU (TAR)

CF TAR *target processor*

This option allows you to configure the emulator for the target that you are using. *target processor* is the name of your processor. For example, to configure the emulator for a PA6T-1682M target, type:

```
CF TAR PA16X
```

Trap Exception (TRPEXP)

CF TRPEXP[YES, NO]

This option allows you to configure which runtime exceptions are trapped. Setting this option to **YES** causes the emulator to trap SYSRESET, IBRK, PEXTRAP, PEXFP, ILLGINST, DSTINT_DABR, and SFPH exceptions. Setting it to **NO** causes the emulator to trap only SYSRESET, IBRK, PEXTRAP, and DSTINT_DABR exceptions.

Trigger In Filter Mode (TRGINFILTER)

(Wind River ICE SX only)

CF TRGINFILTER[OFF,ON]

This option provides a filtering option for the Trigger In function. When set to **ON**, a detected signal is required for at least 2 clock periods, or 40ns. This option ensures that noise does not cause a trigger.

Trigger Out Mode (TRGOUTMODE)

(Wind River ICE SX only)

CF TRGOUTMODE[OFF, ONALLSTOPS, ONBREAKPOINT]

This option allows you to set the type of events that will cause a trigger output to occur.

OFF -- Trigger output is off.

ONALLSTOPS -- Triggers whenever the target stops running.

ONBREAKPOINT -- Triggers whenever a breakpoint is encountered.

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SyByte Processors

This chapter describes the configuration options available for SyByte processors.

Not all of these CF options apply to all target processors; in general, only applicable options will be visible for any given processor. Which options are visible also depends on whether you are using a Wind River Probe or Wind River ICE SX.

Core(s) Select (CORES)

CF CORES [AUTO, ALL]

If you are attached to multiple cores in a single debug session, setting this option to **AUTO** puts only a single core into Background Mode. Setting this option to **ALL** puts all attached cores into Background Mode.

The default is **AUTO**.

Delay After Reset N*1ms (DRST)

CF DRST [0..1000]

This option allows you to modify the delay between the release of **HRESET** and the first JTAG communication attempt. The default is **10**.

Drive TReset Line (TRESET)

CF TRESET [OPENC, ACTIVE]

This parameter controls the logic applied to the **TRESET** signal on the target. Selecting **OPENC** uses an **open collector** approach in which the active driver is released by tri-stating the line and allowing conditioning resistors on the target to return the signal to the non-active state. Selecting **ACTIVE** in this option causes the emulator to drive the **TRESET** signal to both active and inactive states. This is sometimes required on targets in which the conditioning resistors cause excessive rise or fall time on the signal when returning to an inactive state. This excessive time can cause the processor to come out of reset in an incorrect state.

Emulator HRESET Command Control (CMDRST)

(Wind River ICE SX only)

CF CMDRST [IN, RST, BOTH]

When your Wind River ICE SX is connected to a multi-core target, and **CF HRESET** is set to **ENABLE**, use this option to select the reset action for all cores when issuing an **IN** or **RST** command to a single core.

If **IN** is selected on a single core, then an **IN** command to that core will reset all target cores.

If **RST** is selected on a single core, then an **RST** command to that core will reset all target cores.

Setting this option to **BOTH** will cause either an **IN** or **RST** command to reset all cores.

Emulator HRESET Control (HRESET)

CF HRESET [ENABLE, DISABLE]

This option determines whether the **HRESET** line is asserted when you issue an **IN** command. Selecting **ENABLE** asserts **HRESET**, and selecting **DISABLE** prevents **HRESET** from being asserted.

External Trigger In (TRGIN)

(Wind River ICE SX only)

CF TRGIN [OFF, LEVELHI, LEVELLO, EDGEHI, EDGELO]

This option sets the trigger input signal sense detection. When activated, **Trigger In** stops the target upon detection. **Trigger In** does not work with any events.

The following table describes the available settings for this option.

Table 21-1 **Trigger In Settings**

Setting	Description
OFF	Trigger signal detection is off.
LEVELHI	The trigger input level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger input level is set below 1.8 volts.
EDGEHI	Configures the system to trigger on the rising edge of a pulse.
EDGELO	Configures the system to trigger on the falling edge of a pulse.

External Trigger Out (TRGOUT)

(Wind River ICE SX only)

CF TRGOUT [LEVELHI, LEVELLO, PULSEHI, PULSELO]

This option allows you to set the trigger output signal type and level. The following table describes the available settings for this option.

Table 21-2 **Trigger Out Settings**

Setting	Description
LEVELHI	The trigger output level is set to a value of 1.8 volts or higher.
LEVELLO	The trigger output level is set below 1.8 volts.

Table 21-2 **Trigger Out Settings**

Setting	Description
PULSEHI	Trigger Out signal pin will be a pulse from LOW to HIGH and back to LOW when triggered.
PULSELO	Trigger Out signal pin will be a pulse from HIGH to LOW and back to HIGH when triggered.

Invalidate Cache When Initialize (INVCA)

CF INVCA [YES, NO]

This option controls whether the contents of the target processor's instruction cache are invalidated when you issue an **IN** command. Setting this option to **YES** causes the cache contents to be invalidated. This option applies only to the **IN** command, not the **INN** or **INE** commands.

Issue an IN on Coldstart (INCOLD)

CF INCOLD [YES,NO]

This option configures the emulator boot sequence.

Set this option to **YES** to issue an **IN** command, which asserts a reset on the target during a boot sequence.

Set this option to **NO** to issue a **SYNC** command instead of asserting reset on the target. The **SYNC** command does not reset the board. It establishes JTAG communications and captures the current context. This option is best if you want to hot plug the emulator into a running target.

The default is **NO**.

JTAG Clock Rate (MHz) (CLK)

CF CLK [0.025,0.5,1,3,6,12,16]

This option configures the rate at which debug commands are clocked to the target. The default setting is **16**.

Little-endian Mode (LENDIAN)

CF LENDIAN [YES,NO]

This configuration value determines whether the debugger treats memory contents as little-endian (bits ordered 0..63) or big-endian (bits ordered 63..0.) This affects display and interpretation of opcodes in the debugger window, as well as the effects of symbolic manipulation of variables. Setting this option to **YES** means that little-endian is used; setting the option to **NO** means that big-endian is used.

Load Boot Table on IN (BL)

CF BL [ENABLE, DISABLE]

This option enables or disables the Linux bootline commands.

Memory Management Unit (MMU)

CF MMU [ENABLE, DISABLE]

This option controls physical to virtual address translation.

ENABLE -- Informs the emulator that addresses should be checked for virtual mapping.

DISABLE -- Addresses will not be checked for virtual mapping.

Monitor Target Reset (RST)

CF RST [YES, NO, HALT, RUN]

This function continuously monitors the target reset signal. If a reset occurs, one of the following actions may be taken:

- **YES** - If a target reset occurs it is reported to the user and BDM control is lost.
- **NO** - If a target reset occurs it is ignored. This is normally used if the code contains a reset instruction, which causes a reset to the external hardware, but not reset the core.
- **HALT** - If the reset occurs in this mode the target is trapped at the restart vector.
- **RUN** - If the reset occurs in this mode the target is restarted and BDM control is maintained.

By default, this option is set to **YES**. It should only be changed to **NO** if you have a RESET instruction in your code.

No Assertion of TRSET on IN/INN

STRST [ENABLE, DISABLE]

When this option is set to **ENABLE**, the emulator will not assert a Target Reset (TRSET) signal when you issue an initialization command (**IN** or **INN**.)

The option is set to **DISABLE** by default.

Reset Pulse Length N 1*ms (RPL)

CF RPL [1..600]

This configuration option allows you to adjust the duration of the assertion of the HRESET signal on the target board. The number you specify in this option is the number of milliseconds that HRESET is driven active on the target.

Set Breakpoint (SB)

CF SB [SB,IHBC]

This option remaps traditional software breakpoints to internal hardware breakpoints. It is set to Software Breakpoint (**SB**) by default. Setting it to **IHBC** means that all software breakpoints are translated to internal hardware breakpoints. This option is useful when you are debugging code out of Flash or PROM.

Setting this option to **IHBC** may cause limitations in the number of breakpoints that can be set, depending on the target processor.

Set Stack Range (STACK)

CF STACK [OFF / LOWER and UPPER]

This setting is **OFF** by default. When stack limits are set, it prevents the emulator from walking through the stack, past the specified range, and causing accidental bus errors.

Set Work Space (WSPACE)

CF WSPACE [BASE and SIZE]

Flash programming requires a small amount of target RAM to program the Flash Algorithm. You must tell your emulator where writable RAM is located on your target for this purpose.

As part of the configuration process, the emulator will indicate exactly how much of the RAM workspace is required. Depending on the device family and type, this space is limited to under 2 KB. Note that more memory improves the speed of programming.

To configure the workspace for flash programming the parameters should be entered in hex, where **BASE** is the start address, and **SIZE** is the minimum bytes of target RAM required, as displayed in the **Flash Programmer** view. This command allocates memory on the target system that is used by the emulator for various functions, including flash programming.

Step in Delayed Slot (SIDS)

CF SIDS [YES, NO]

Jump and branch instructions change the control flow of a program. The instruction immediately following the jump or branch is known as the instruction in the delay slot. All jump and branch instructions occur with a delay of one instruction; that is, the instruction in the delay slot always executes while the target instruction is being fetched from storage.

YES -- On each single step through assembly code, the instruction in the delay slot will be stepped before taking the jump.

NO -- On each single step through assembly code, the instruction in the delay slot will not be stepped before taking the jump.

Transparent Mode Driver (TMD)

CF TMD [ENABLE, DISABLE]

This command sets all of the configuration parameters that are required to use the Transparent Mode Driver (TMD). Select **ENABLE** to configure your system for use with the TMD, and **DISABLE** if you do not plan to use it.

Target Break Type (TGTBRK)

CF TGTBRK [**EJTAGBRK**, **DINT**]

Use this option to select the method your emulator will use to halt target execution. **EJTAGBRK** uses the BREAK bit in the EJTAG control register to halt the target. **DINT** uses a dedicated input pin to cause a DEBUG exception on those target CPUs that support this feature.

The default is **EJTAGBRK**.

Target Console Redirection (TGTCONS)

CF TGTCONS [**TGTCONS**, **BDM** (for the Wind River ICE SX)

Wind River Probe

Target Console Redirection is not currently supported for the Wind River Probe. You do not need to set this option.

Wind River ICE SX

BDM -- Use this setting to connect I/O on a target board, using the Transparent Mode Driver, to the target's BDM connector. When **BDM** is selected, the Wind River ICE SX is in Transparent Mode, and all I/O data is redirected to the port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

For this type of connection to work, the target application must be linked to the Transparent Mode Driver. Refer to the *Wind River Workbench On-Chip Debugging Guide: Using the WDB Transparent Mode Driver* for more information.

TGTCONS -- Use this setting to connect a COM port on a target board to the TGTCONS port of a Wind River ICE SX. All I/O data is then redirected to port 1237 of the Wind River ICE SX's IP address. You can then read and write the I/O data remotely by using an application such as a **telnet** window connected to the TGTCONS port (1237) with the Wind River ICE SX's IP address.

Target CPU (TAR)

CF TAR *target processor*

This option allows you to configure the emulator for the target that you are using. *target processor* is the name of your processor. For example, to configure the emulator for a BCM1250 target, type:

```
CF TAR BCM1250
```

Trap Debug Exception (TRPEXP)

CF TRPEXP [YES, NO, BREAKPOINTONLY]

This option allows you to configure which run time exceptions are trapped. Setting this option to **YES** causes the emulator to trap RST, CHSTP, MCI, ALI, TRE, SEI, LBRK, IBRK, EBRK, and DPI exceptions. Setting it to **NO** causes the emulator not to trap any exceptions other than TRE and SE. Setting the option to **BREAKPOINTONLY** causes the emulator to trap exceptions only when a breakpoint is encountered.

Trigger In Filter Mode (TRGINFILTER)

(Wind River ICE SX only)

CF TRGINFILTER [OFF,ON]

This option provides a filtering option for the Trigger In function. When set to **ON**, a detected signal is required for at least 2 clock periods, or 40ns. This option ensures that noise does not cause a trigger.

Trigger Out Mode (TRGOUTMODE)

(Wind River ICE SX only)

CF TRGOUTMODE [OFF, ONALLSTOPS, ONBREAKPOINT]

This option allows you to set the type of events that will cause a trigger output to occur.

OFF -- Trigger output is off.

ONALLSTOPS -- Triggers whenever the target stops running.

ONBREAKPOINT -- Triggers whenever a breakpoint is encountered.

Use Current MMU Settings (USEERL)

CF USEERL [YES, NO]

YES -- The emulator bypasses the user application translation lookaside buffer (TLB) definition to access memory.

NO -- The emulator uses the user application TLB definition to access memory.

The default is **YES**.