Western Digital

WD1006-WAH

USER'S GUIDE

June 1987

Preliminary

WD1006-WAH
WINCHESTER DISK CONTROLLER
USER'S GUIDE

PRELIMINARY DOCUMENT!!. INFORMATION SUBJECT TO CHANGE 8 JUNE '87 !!!

WD1368 6/87

PRODUCT DESCRIPTION

This document describes the hardware and software installation of the WD1006-WAH, a 16-bit disk controller for the IBM Personal Computer AT or AT-compatible computer. The WD1006-WAH's drive interface conforms to ST506/ST412 specifications. An advanced design implements the WD1006-WAH's most significant feature, 1:1 interleave. Refer to the "If You Have a Problem..." section for further information on the importance of interleave.

There are two versions of the WD1006-WAH:

Feature 001 (F001):	Cacheing firmware, NO wait state generator.
Feature 002 (F002):	Cacheing firmware, wait state generator.

HARDWARE INSTALLATION

This section briefly describes installation of the WD1006-WAH. If the disk drive(s) is (are) being installed internally, it is best to locate the controller in the closest available expansion slot relative to the drive.

CAUTION

Handle the controller board by the ends of the board. Some of the chips are static sensitive and damage may occur if the board is incorrectly handled.

Verify the controller jumper settings. Only verify the settings. Modification of the standard factory settings is rarely necessary. Modify jumpers only under the direction of a qualified individual, i.e. your dealer. Refer Table 1 for further information on jumper settings. Figure 1 illustrates the locations of the jumpers.

TABLE 1. JUMPER SETTINGS

JUMPER	PIN CONNECTS	FEATURE NUMBER	DESCRIPTION
W1	1-2	All Features	Sandard setting. Supports 16 heads. No REDUCED WRITE CURRENT (RWC).
	2-3		Supports 8 heads and RWC.
W2	NO JUMPER	F001	Not used with F001. F001 F001 does not contain the wait state hardware.
	1-2	F002	No wait states requested.
	3-4	F002	1 wait state requested.
	5-6	F002	2 wait states requested.
W3	1-2	All Features	Standard setting. Selects primary ports.
	2-3		Selects secondary ports. NOTE DOS supports only two drives. Modification of the device drivers is necessary to support more than two drives. Contact your dealer or distributor for information on third party software that modifies device drivers.
W4	JUMPERED	All Features	Drive LED is not latched, i.e. LED lights for drive selection. REMOVE W10 IF W4 IS INSTALLED.
W5 through W8	NO JUMPER	All Features	Reserved for WD1006-RAH.
W9	NO JUMPER	All Features	Enables cacheing for F001 and F002.
	1-2	F001, FOO2	Disables cacheing.
W10	NO JUMPER	All Features	Factory setting. Non-latched mode.
	1-2	All Features	Latched mode.

PRELIMINARY DOCUMENT!!. INFORMATION SUBJECT TO CHANGE 8 JUNE '87 !!!

Verify termination on last drive. Verify proper setting of drive select switches. Do NOT use the drive's radial select option. Refer to the drive owner's manual for information about proper drive termination and select switches.

Remove the blank expansion slot bracket. Put the bracket away and save it for possible future use. The screw will be used to hold the controller board in place.

Attach the 34-pin control cable connector to J4. Ensure that pin 1 on the cable and controller connector match.

Connect control connector to drive.

Attach drive 0's 20-pin data connector to J3.

Attach drive 1's 20-pin data connector to J2.

Connect the cable(s) tp the proper drive(s).

Attach the Winchester activity LED connector to J1. J1 is a reversible connector.

Install the controller board into the expansion slot. Ensure that the board is seated properly by pressing down on both ends of the board. Secure the board with the bracket screw.

Software Installation Instructions

This section contains instructions for preparing (low level formatting) the drive to be recognized by the operating system. Formatting the drive uses one of two software programs, the IBM Advanced Diagnostics (or equivalent for AT compatibles) or WDFMT.EXE. (Contact your dealer for a copy of WDFMT. If your dealer's name, address, and telephone number is not written on the back cover, make a quick note of the information yourself. Western Digital does not distribute WDFMT to end users.)

Insert your system diagnostic diskette (or equivalent).

Turn on the system power.

Boot diagnostic and setup option.

CAUTION

Avoid system damage by consulting your Technical Reference Manual to ensure that your drive type is supported by your host Basic Input/Ouput System (BIOS) ROM drive tables. Not all AT-compatibles share the same drive tables as IBM.

Set up the system for the proper configuration of diskette and fixed drives, base memory size, expansion memory size, and display.

NOTE

The following step requires execution of low level for matting. Use of Advanced Diagnostics (or similar program for IBM-compatibles) is necessary since the WD1006-WAH contains no on-board BIOS ROM. IBM Advanced Diagnostics will not format a drive at 1:1 interleave. Use of WDFMT, SpeedStor from Storage Dimensions, Disk Manger from Ontrack, or similar software is necessary to format the drive at 1:1 interleave. Contact your dealer for further assistance. Finally, formatting a drive destroys any data on the drive. If your drive contains useful data, backup the drive before execution of the low level format.

Insert your Advanced Diagnostics diskette (or equivalent) and execute low level format. Follow the menu and reference manual instructions.

Load and execute the FDISK and FORMAT programs. Follow the menu and reference manual instructions.

If You Have a Problem...

Listed below are some common problems.

PROBLEM: "Nothing Done Exit" message appears when formatting the drive.

CAUSE: "y" was not pressed. Initiate formatting procedure again. Be sure to press "y".

PROBLEM: Drive does not partition.

CAUSE: Check drive types. Note that the drive types for the AT and Compaq machines differ.

PROBLEM: "Error Reading Fixed Disk" appears when booting from hard drive.

CAUSE: DOS partition not active.

PROBLEM: Winchester activity LED continuously lit.

CAUSE: No problem! This is normal operation for ATs.

PROBLEM: Error code 1701.

CAUSE: Power supply is overloaded.

PROBLEM: Error code 20.

CAUSE: Controller component malfunction. Controller plugged in incorrectly. Cables reversed. For controller failures, contact your dealer.

PROBLEM: Error code 40.

CAUSE: Wrong drive type. Not enough drive power.

PROBLEM Error code 80.

CAUSE: Not enough drive power. Bad cables. Improper drive select or termination. Bad drive.

PROBLEM: DOS returns a seek or ID not found error.

CAUSE: One possible cause of this problem is a minor incompatibity between the WD1006-WAH and the older WD1003-WAH. If the drive has more than eight heads, for instance, a 16 head drive, the WD1003-WAH numbers heads 8 through 15 as 0 through 7 in the media's ID fields. Contrawise, the WD1006-WAH numbers heads 8 through 15 as 8 through 15. To solve the problem, backup and reformat the drive. This is not manifested in drives with less than eight heads. If this is not the cause of the error, then you have a drive problem.

PROBLEM: Slow and inefficient operation.

CAUSE: The biggest culprit for this problem is an incorrect interleave factor. Therefore, some experimentation with the interleave factor may be necessary. (Refer to the format instructions for setting interleave factor.) Interleave factors are very dependent on the host operating system and application.

PROBLEM: Western Digital technical support line is always busy.

CAUSE: Consult your dealer first. Use our technical support only if your or the dealer's troubleshooting failed. If the dealer's number is not written on the back cover, make a quick note of the number yourself. Thanks.

Master CM

PRELIMINARY

ENGINEERING SPECIFICATION

WINCHESTER FIXED DISK CONTROLLER MODULE

WD1006-WAH
SPECIFICATION NO. 96-000331

AUGUST 25, 1985

REVISION HISTORY

REV	ECO	DESCRIPTION	APPR	DATE

ENGINEERING SPECIFICATION
TABLE OF CONTENTS

1.0 SCOPE

This document describes the functional, electrical and logical design characteristics of the WD1006-WAH Winchester Disk Controller module. The board is used to interface two ST-412 compatible fixed disk drives to the PC-AT computer I/O Channel bus structure.

The module includes the WD5010 Winchester Disk Controller, the WD1015 Buffer Manager Control Processor, a WD10C20 Read/Write Controller, RAM sector buffer memory and associated control logic. The design features a Buffer Manager and Control (AMAC) gate array for module logic reduction and to allow data transfers to occur with a 1:1 sector interleave format.

Portions of the WD1015 control processor protocol specification (firmware) are included as a part of this document as is a description of the module self-test operation. Software which resides in the PC processor (either test or operational) or is installed in the module BIOS ROM is not included as a part of this document.

2.0 APPLICABLE DOCUMENTS

2.1 WD1006-WAH BOARD DOCUMENTS

61-000148	P/L & Assembly
60-000116	PWB Fabrication
65-000138	Artwork, PCB, 2 Layer
96-000330	Test Specification
xx-xxxxxx	Test Procedure
68-000149	Schematic Diagram

2.2 COMPONENT DOCUMENTS

	WD5010 Winchester Disk Controller
	WD10C20 Read/Write Controller
62-002030-80	WD1015-PLxx-xx Buffer Manager Control Processor
96-000034	AMAC Specification
68-000147	AMAC TTL Schematic Diagram (Reference only)
96-XXXXXX	PAL Specification, Address Decoder (U17)
96-XXXXXX	PAL Specification, BIOS ROM Option (U25)
96-XXXXXX	PAL Specification, Wait State Control (U16)
	WD1015-PL17-02 Firmware Listing
	WD1006-WAH BIOS Firmware Listing

3.0 DESIGN OVERVIEW

3.1 HARDWARE OVERVIEW

The WD1006-WAH Winchestery Disk Controller (reference code name "CHEETAH" is a PC-AT bus compatible printed-circuit module that interfaces two ST-412 type fixed disk drives to the system processor. The module fixed disk control logic includes the WD5010 and WD1015 Winchester disk control components, a WD10C20 Read/Write (Data) Controller and two 8192x8 static RAM's for sector data buffering.

A primary feature of the module is an 84-pin (PC-AT) Buffer Management and Control (AMAC) gate array used to minimize the module circuitry and to allow a 1:1 sector interleave data transfer format. Figure 3-1 is a simplified block diagram of the fixed disk control logic and each major block is briefly described below. The module logic is fully described in the referenced documents or in subsequent sections of this specification.

3.1.1 WD5010 WINCHESTER DISK CONTROLLER

The WD5010 Winchester Disk Controller (WDC) is an advanced design VLSI device that provides the fixed disk drive(s) data and control interface and sector data buffer control logic. The major features of the device include:

* Multiple sector read/write commands
* Error Correction Code (ECC) generation and error correction
* Programmable format and error recovery algorithms

3.1.2 WD1015 BUFFER MANAGER CONTROL PROCESSOR

The WD1015 Control Processor (CP) is an eight-bit microprocessor (type 8051) that operates with the WD5010 and the AMAC logic array to aid in processing the disk commands, to provide sector data buffer management, to help in error recovery procedures and to perform module diagnostics. The processor chip includes internal RAM and ROM memory.

3.1.3 WD10C20 READ/WRITE CONTROLLER

Winchester drive read data separation and write data pre-compensation is performed by the WD10C20 Read/Write Controller (RWC). The device contains all of the necessary components (except for a few passive external parts for complete MFM read/write data control.

3.1.4 AMAC LOGIC ARRAY

Module logic simplification and power reduction is provided by a VLSI logic array that replaces the standard WD1014 support device and several SSI/MSI components. The internal device logic includes the data buffer address registers and read/write control, WD5010 task file image registers, data buffer registers and interfaces to both the system and module (local) bus structures.

3.1.5 RAM DATA BUFFER

Two 8192x8 static RAM memories buffer the sector data between the drive(s) and the PC-AT system bus and ECC correction information between the WD5010 disk controller and the WD1015 control processor. The sector buffer and the above control components allow a 1:1 sector interleave format for optimized system performance.

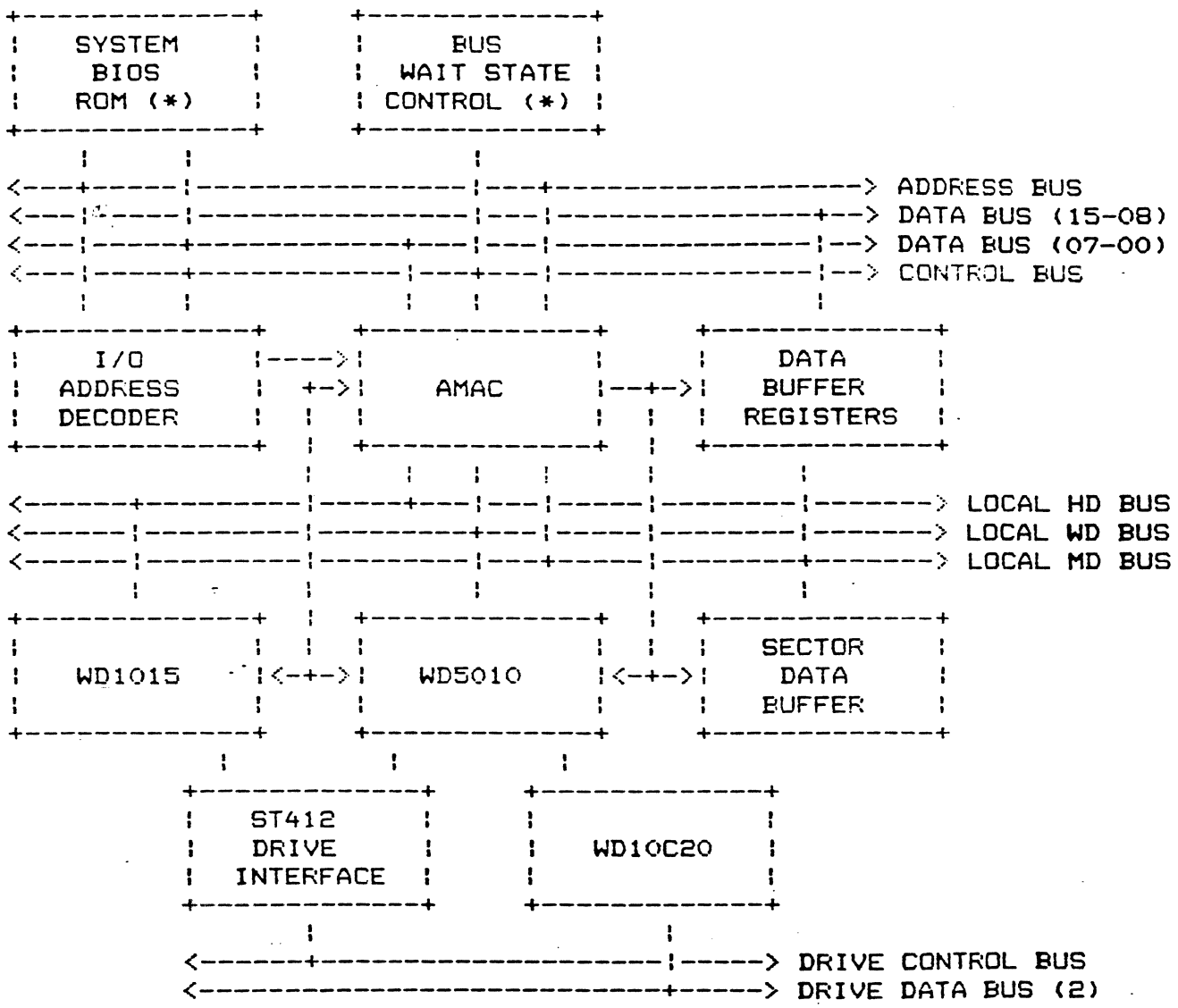
3.1.6 SYSTEM BUS INTERFACE

The module interfaces to the system bus address, data and I/O control signals. All fixed disk read/write data transfers are 16 bits wide and utilize the host fast I/O transfer protocol. Module control and status transfers are 8 bits wide and use the lower data byte (SD07-00) only. The controller register address map is fixed (at primary or secondary ranges) as is the bus interrupt request.

The system interface also includes an I/O 'wait state' control option to allow module operation in higher speed bus systems and a system 'BIOS' ROM option to support future drive types or system modifications.

3.1.7 WINCHESTER DRIVE INTERFACE

The controller interfaces to the fixed disk drives via one 34-pin control cable and two 20-pin data cables in conformance with standard ST-412 signal definitions. Drive power is not furnished via the WD1006-WAH module.



(*) OPTIONAL

FIGURE 3-1
SIMPLIFIED BLOCK DIAGRAM

3.2 SOFTWARE OVERVIEW

All control and data transfers between the host processor and the fixed disk controller use system programmed I/O. All data transfers are word wide (16 bits) and use the system 16-bit fast I/O control protocol. All control and status transactions use the lower data byte only. The module address range is fixed (at either of two ranges) as is the controller priority interrupt level assignment. The module address map and register definitions are given in Section 5.0 of this document.

3.2.1 FIXED DISK SECTION

3.2.1.1 Command Control Flow

The Winchester controller commands and status descriptors are well documented in the referenced specifications; however, it is very important to understand the relation between the system 'host', the WD5010, the WD1015 and the AMAC support registers. A typical command sequence is given below to help illustrate this relationship.

* In the idle state, the WD5010 drive control signals are off, the controller status indicates ready, selected drive status is valid, the controller interrupt is enabled (but not asserted), the AMAC control is in idle with host drive selection enabled and the WD1015 is in idle, waiting for the wakeup signal interrupt.

* The host processor outputs the command parameters to the AMAC task file image registers and outputs the operation command (seek, read, write, etc.) and the command attributes (long mode, retry control, etc.). For write operations the system processor also outputs the sector or format data.

* The command output is intercepted by the AMAC and is registered in the AMAC command register (although to the system processor it appeared that the command and command parameters were received by the WD5010).

* A read command output sets the AMAC wakeup control latch causing the controller status to indicate busy and the WD1015 wakeup interrupt to be asserted. 'Write' and 'Format' commands set the data request control latch (status signal DRQ asserted) to request the host data transfer. Completion of the write data transfer (sector length in bytes) then sets the WD1015 wakeup interrupt and busy status.

* The WD1015 examines the command, verifies command parameters and passes the command to the WD5010 for execution. The host command output also removes the AMAC from the idle state and the system processor is inhibited from altering the drive selection until the CP returns the AMAC to idle. This feature insures that the host cannot change the selected drive even if the controller is 'not busy' (the case during multi-sector transfers).

* The WD5010 executes the command providing drive positioning, data transfer control, error monitoring and completion status. Drive read/write data control is provided by the WD10C20 RWC for commands that require data transfer. For multi-sector transfers with a 1:1 interleave format the WD5010 and host will be accessing the sector data buffer during the same intervals. Memory access resolution and address control is provided by the AMAC control logic.

* As each sector operation completes (more than one for multi-sector operations), the WD5010 interrupts the WD1015 which again examines the command, status, etc., transfers the sector status to the AMAC task file image, sets the controller status to indicate 'not busy' and interrupts the system processor. For multi-sector operation, the host data transfer will again 'wakeup' the controller and the operation continues.

* On command final completion, the WD1015 and AMAC are returned to idle and the host may examine final controller status, select the alternate drive, issue new commands, etc..

3.2.1.2 Standard Commands

The WD5010 allows execution of the standard commands described in the WD5010 specification and listed below - refer to Section 5.0 for the WD1006-WAH command descriptions.

> Restore, Seek, Read Sector, Write Sector, Scan ID, Write Format, Compute (ECC) Correction and Set (Head and ECC) Parameters.

Of these, the Scan ID, Compute Correction and Set (Head and ECC) Parameters commands are not directly available to the system processor (although they may be executed by the WD1015 transparently to the host processor).

3.2.1.3 Non-Standard Commands

Fixed disk commands to the WD1006-WAH are intercepted by the WD1015 (with the aid of the AMAC logic) and thus commands not specified in the WD5010 command list may be defined.

* Set (Drive) Parameters - Non-standard command used to communicate drive parameters to the controller. The head, cylinder and sector definition for each drive is set by this command. The WD1015 uses the drive parameters in the execution of multi-sector commands and in evaluating legal controller commands.

* Read Verify - Command used to verify that a previous write command was correct. Read data is not input by the host processor. The command may be used with multi-sector operations. An error condition will abort a multi-sector verify on the error sector. The retry command operand may be used with this command.

* Diagnostic Command - The diagnostic command causes the WD1015 to execute an on-board diagnostic program and to report the test results (at the WD5010 Error Register Address).

3.2.1.4 Multi-sector Commands

Multiple sector read, write and verify commands of up to 256 sectors are allowed without restriction on track or cylinder boundaries. Non-recoverable control errors (drive not ready, write fault, etc.) or non-correctable read data errors will terminate a multi-sector command an the controller expects a 'new command' to continue operation. Corrected read data errors do not terminate the commmand and the controller expects a normal data transfer restart and continuation. The 'long' ECC diagnostic modes are not used in multi-sector operation. The drive parameters are checked during the execution of this command.

3.2.1.5 Diagnostic Commands

The controller on-board diagnostic is executed on command and verifies th WD1015 local storage, the sector data buffer storage and the WD1015, WD5010 and AMAC data paths. Results are encoded and are available to the system processor via the controller error register - refer to Section 8.0

3.2.2 EXTENDED MODE OPTIONS

3.2.2.1 Block Commands

To be supplied

3.2.2.2 Drive Commands

To be supplied

4.0 HARDWARE INTERFACE

This section provides detailed hardware interface information for the controler and includes a signal definition of the external signals used by the module. The signals are also listed in the Appendix along with their connector pin assignments. Further information on each signal is provided in the referenced literature.

4.1 SYSTEM BUS INTERFACE

The PC-AT I/O channel signals used by the WD1006-WAH are noted below and require both the P1 and P2 system bus connectors.

SA19-SA00
System Address bus - Inputs used to select the module bus I/O addresses and BIOS ROM address. The module decodes the lower I/O address input terms (SA09-00) to select the task file and support registers. The upper bits are used to select the BIOS ROM memory map address.

SD15-SD00
System Data bus - Bi-directional signals used to transfer 16-bit fixed disk data, 8-bit module control and status information and 8-bit BIOS ROM data.

AEN
Address Enable - Input control signal that indicates a valid I/O address is on the system bus. The controller decode logic uses this term to qualify the I/O address decoding.

BALE
Bus Address Latch Enable - Input control signal used to initiate a system bus data transfer. The AMAC logic uses this input to generate the system bus fast I/O transfer control signal and to enable the high order data byte control signals.

-IOCS16
I/O Control Signal 16 - Output signal used to indicate the fast 16-bit data transfer mode. The controller asserts this signal for all fixed disk 'data' transfers.

IOCHRDY
I/O Channel Ready - Output signal used to insert 0, 1 or 2 wait states in the 16-bit data transfer cycle.

IRQ14
Interrupt Request Level 14 - Controller output interrupt level to the processor requesting a data block transfer or indicating command completion. The level clears on a subsequent fixed disk command to the controller, host status input, programmed reset or a master system reset.

-IOR
I/O Read - Input read control strobe asserted by the system processor during bus 'read' transactions. The controller uses the signal (along with the system address bus decoding) to enable system I/O reads of both data and status information.

-IOW
I/O Write - Input control strobe asserted by the system processor during bus 'write' cycles. The module uses this strobe and the decoded bus address to receive both data and command information.

-SMEMR
System Memory Read - Input strobe used to enable the BIOS ROM.

SYSCLK
System Clock - System bus clock used to clock the I/O wait state control logic.

RESET
Reset - Input module reset used to initialize the WD5010, WD1015 and AMAC devices, clear the interrupt level and to halt drive operation. When reset clears, the WD1015 will automatically execute on-board diagnostic tests and load the test result status in the fixed disk error register.

4.2 FIXED DISK DRIVE INTERFACE

The Winchester drive control and data (ST-412) interface is well documented in the referenced literature and is included here for document completeness only.

4.2.1 CONTROL CABLE

DS1-/2-
Drive Select - Primary output control signal used to connect a drive interface to the control signals. The WD1006-WAH is limited to drive 1 o 2. The signals are negated by the control processor following a system master or programmed reset. The drive can only be selected by the host and then only when the AMAC is in the idle state.

HS3-/0-
Head Select - Binary-coded output head select signals (from the WD1015 only) allowing drives with up to sixteen R/W heads to be attached to the controller.

WG-
Write Gate - Write enable output control level to the selected drive. Th signal is negated by a write fault condition and by a master or programme reset.

STEP-
Output step signal to the selected drive for R/W head positioning. The step rate is programmable in the WD5010.

DIRIN-
Direction In - Step direction control signal to the selected drive. When asserted (low) the step direction is 'in' or toward the center of the disk.

SC-
Seek Complete - Control signal from the selected drive asserted when the R/W heads are stable on the final track. The signal is monitored by the WD5010 during seek and restore commands and during the implied 'seek' for read/write commands.

TRK00-
Track 00 - Positioning signal from the drive indicating R/W head location at the outermost data track. The signal is monitored by the WD5010 following drive 'restore' commands.

WF-
Write Fault - Signal from the selected drive indicating a fault condition at the drive which inhibits further writing (or stepping) to the drive.

INDEX-
Index - Positioning signal from the drive that occurs once per drive revolution and used by the WD5010 for command timeout and track formatting. The index signal is available (non-latched) to the host in the status byte.

RDY-
Drive Ready - Control signal from the drive indicating the drive is ready and that the I/O control signals are valid - available to WD5010 and to host controller status.

4.2.2 DATA (Radial) CABLES

RMFM1/2(+,-)
Read MFM - Differential read data input from each drive. The data received from each drive is gated by the drive select signals and is input to the WD10C20 RWC for data/clock separation.

WMFM1/2(+,-)
Write MFM - Differential signal to each drive that defines the data/ clock transitions to be written on each track. The write data is pre-conditioned by the RWC.

NOTE: The ST-412 'drive select 3/4' control lines are not implemented; thus, attached drives must be configured as drive unit 1 or 2 only. The HS3- signal (head select 3) is a dual purpose control line and may be selected to reflect the state of the WD5010 'reduced write current' control line (see logic diagram for jumper positioning).

4.3 INDICATORS

LED+/-
LED Indicator(s) - External indicator signals used to provide visual indication of fixed disk activity.

5.0 SOFTWARE INTERFACE

5.1 REGISTER ADDRESS MAP

The WD1006-WAH controller system I/O port address map is summarized in Figure 5-1 and includes the WD5010 task file area and the module auxiliary support registers. The primary address is listed first with the secondary address shown within parenthesis (see Section 7.0 for address selection jumper installation).

ADDRESS (HEX)	REGISTER	FUNCTION
1F0 (170) RW	HDDTR	Hard Disk Data Register (16 bits)
1F1 (171) WO	HDWPC	Write Pre-compensation Cylinder
1F1 (171) RO	HDERR	Error Register
1F2 (172) RW	HDSCT	Sector Count
1F3 (173) RW	HDSSN	Starting Sector Number
1F4 (174) RW	HDCLL	Cylinder Number - Low Byte
1F5 (175) RW	HDCLH	Cylinder Number - High Byte
1F6 (176) RW	HDSDH	Sector Size, Drive/Head Select
1F7 (177) WO	HDCMD	Command Register
1F7 (177) RO	HDSTT	Status Register
3F6 (376) WO	HDFDR	Fixed Disk (Control) Register
3F6 (376) RO	HDASR	Alternate Status Register
3F7 (377) RO	HDDIR	Digital Input Register

FIGURE 5-1
REGISTER ADDRESS MAP

5.2 TASK FILE REGISTERS

5.2.1 REGISTER DESCRIPTION

Figure 5-2 summarizes the controller task file registers (addresses 1F0/170 through 1F7/177) and their bit assignments with respect to the system processor lower byte bus terms (SD07-00). Certain register descriptions shown in Figure 5-2 may differ slightly from the standard descriptions contained in the referenced WD5010 documentation. It is ver important to remember that the host access to these registers is always via the register image contained within the AMAC array. The WD1015 control processor has access to both the WD5010 and AMAC registers.

REGISTER	7	6	5	4	3	2	1	0
HDWPC	CYLINDER NUMBER/4							
HDERR	BBD	ECC	0	INF	0	ACD	TK0	DNF
HDSCT	NUMBER OF SECTORS							
HDSSN	STARTING SECTOR NUMBER							
HDCLL	CYLINDER NUMBER LSB							
HDCLH	0	0	0	0	0	CYL NUMBER MSB		
HDSDH	1	SS1	SS0	DS2	HS3	HS2	HS1	HS0
HDCMD	COMMAND							
HDSTT	BSY	RDY	WFT	SKC	DRQ	CRD	IDX	ERR

FIGURE 5-2
WD5010 TASK FILE REGISTERS

5.2.2 COMMAND DESCRIPTION

The task file command register (HDCMD) accepts the commands and command attributes as shown in Figure 5-3. Commands will not be accepted when the controller is 'busy', and will terminate without execution if the drive seek complete and ready signals are false or if a write fault condition exists at the drive. Undefined command codes will also terminate with the 'aborted command' error.

COMMAND	7	6	5	4	3	2	1	0
RESTORE	0	0	0	1	RT3	RT2	RT1	RT0
SEEK	0	1	1	1	RT3	RT2	RT1	RT0
RD SECTOR	0	0	1	0	0	0	LNG	RTY
WRT SECTOR	0	0	1	1	0	0	LNG	RTY
FMAT TRACK	0	1	0	1	0	0	0	0
RD VERIFY	0	1	0	0	0	0	0	RTY
DIAGNOSE	1	0	0	1	0	0	0	0
SET PARAM	1	0	0	1	0	0	0	1

FIGURE 5-3
WD5010 COMMAND SUMMARY

where: RT3-0 = Drive stepping rate - refer to Figure 5-4

LNG = 0 = Normal mode, normal ECC functions are performed
= 1 = Long mode, the WD5010 is inhibited from generating or checking the ECC bytes. The WD5010 will append the additional bytes supplied by the drive (read) or system processor (write) to the normal data field.

RTY = 0 = Error retries and ECC correction are enabled
= 1 = Retries and ECC correction are disabled.

5.2.3 COMMAND DEFINITION

The following provides a brief overview of each command. Additional information is contained in the WD1006-WAH control processor firmware description and in the WD5010 specification. Again, it should be remembered that the WD1006-WAH does not allow all WD5010 commands (and command attributes) to the host - the commands are required to be in the format given in Figure 5-3.

RESTORE
A 'Scan ID' command is issued to the WD5010 and (if good) a seek command to cylinder 0 is issued. If the scan command errors a 'Restore' command is issued to the WD5010. During a 'restore', step pulses are issued to the selected drive until the Track 000 position flag from the drive is asserted. The restore step rate is governed by the drive seek complete signal. The command will abort with the error summation bit set in the status register (and a track 0 error set in the error register) if the position flag is not asserted within 2047 step pulses.

SEEK
The seek command positions the drive heads over the cylinder specified in the task file cylinder select registers (HDCLH/L). The step rate is specified by the RT3-0 command parameter bits (and when used for a restore provides a faster operation). The controller priority interrupt is generated on command completion. The buffered seek operational mode is supported.

READ SECTOR
A number of sectors (1-256) are read from the selected disk. If the drive is not positioned at the specified cylinder an implied 'seek' will occur. Drive furnished ECC check bits will be used if the 'read long' mode is specified. Data errors will be corrected if retries are enabled and the long mode is not selected. Uncorrectable errors will not inhibit the (error sector) data transfer, however multi-sector transfers will be terminated. The controller interrupt will occur as each sector is ready for system input.

WRITE SECTOR
A number of sectors (1-256) are written to the selected disk with an implied seek occurring if required. Multiple sector write (and read) operations may cross track and cylinder boundaries. System processor supplied ECC bytes will be appended in the 'write long' mode. The interrupt is generated as the data for each sector is required (except the first). The first data buffer is output by the system processor after the command has been issued and the data request status bit is on.

FORMAT TRACK
The track specified by the task file is formatted with identification, data and check fields in accordance with the interleave table transferred to the sector buffer. The sectors per track and sector size are specifie in the task file. Command completion will leave the data field initialized to 'zeros'. The completion interrupt is generated as each track is formatted.

READ VERIFY
The read verify command functions similar to a normal read command except that data is not input by the system processor. The ECC bytes are checke for data verification. Multiple sector operation is supported.

DIAGNOSE
The diagnose command causes the WD1015 to execute it's self test routines and to report a result descriptor in the error register (HDERR). Refer t Section 8.0 for a test description.

SET PARAMETERS
The set (drive) parameters commamd transfers the maximum sectors per trac (HDSCT register) and maximum heads per drive (HDSDH register) to the controller for each drive. The drive parameters are used by the WD1015 C during multi-sector command execution.

5.2.4 STEP RATES

The stepping rates for the encoded control bits (RT3-0) used with the 'restore' and 'seek' commands above are shown in Figure 5-4.

RT3-0 DECODE(H)	RATE (MS)	RT3-0 DECODE	RATE (MS)
0	35 US	8	4.00
1	0.50	9	4.50
2	1.00	A	5.00
3	1.50	B	5.50
4	2.00	C	6.00
5	2.50	D	6.50
6	3.00	E	3.2 US
7	3.50	F	16 US

FIGURE 5-4
DRIVE STEPPING RATES

NOTE: Rate decodes 0(H), E(H) and F(H) are per the WD5010 specification. The step rate will default to 6.50 MS if not initialized by a previous seek or restore command.

5.3 WD1006 CONTROL AND STATUS REGISTERS

5.3.1 HARD DISK ALTERNATE STATUS REGISTER (HDASR) 3F6/376 (RO)

This register is contained within the AMAC array and provides fixed disk status to the system processor. The register contains a 'real time' section (bits 7, 6, 3 and 1) and a 'register' section set by the control processor at sector transfer time (bits 5, 4, 2 and 0).

7	6	5	4	3	2	1	0
BZY	RDY	WFT	SKC	DRQ	CRD	IDX	ERR

FIGURE 5-5
ALTERNATE STATUS REGISTER

where:

BZY = Controller Busy Flag
RDY = Ready from selected drive
WFT = Write Fault Flag from WD1015
SKC = Seek Complete Flag from WD1015
DRQ = Data Transfer Request Flag
CRD = Corrected Data Flag from WD1015
IDX = Index Pulse from selected drive
ERR = Error Flag from WD1015

This register reflects the same status as the WD5010 status register except for bit position 1 where the drive index signal replaces the command in progress (CIP) flag. It should be remembered that the index bit is not latched and thus follows the drive control signal (approximately a 200 microsecond pulse every 16.7 milliseconds). For multi-sector read operations the reported sector number (flagged by the corrected data status bit) will be the 'error sector plus one'. All othe error conditions will report the 'error sector'.

The register may be interrogated by the host processor at any time withou interference with other control functions.

5.3.2 HARD DISK DIAGNOSTIC INPUT REGISTER (HDDIR) 3F7/377 (RO)

The fixed disk diagnostic input register reflects the current state of th fixed disk drive select, head select and drive write gate signals (complimented form). The head select bits are controlled by the WD1015 and are thus valid only following a command; i.e., they do not follow the SDH register directly.

7	6	5	4	3	2	1	0
---	WTG-	HS3-	HS2-	HS1-	HS0-	DS2-	DS1-

FIGURE 5-6
DIAGNOSTIC INPUT REGISTER

where:

WTG- = Write Gate on
HS3- = Head Select 3 (or Reduced Write Current Flag)
HS2-/0- = Drive Head Select (binary)
DS2-/1- = Drive Select

5.3.3 HARD DISK AUXILIARY CONTROL REGISTER (HDFDR) 3F6/376 (WO)

The Hard Disk Auxiliary Control Register is contained within the AMAC and is used to allow programable controller reset and to provide enable/disable control of the fixed disk priority interrupt.

7	6	5	4	3	2	1	0
0	0	0	0	0	RST	IDS	0

FIGURE 5-7
AUXILIARY CONTROL REGISTER

where:

RST = Program controlled (master) reset
IDS = Data Transfer Interrupt Disable

NOTE: The software controlled reset bit (RST) will maintain the fixed disk section logic reset as long as the bit is on. The bit must be turned on (for a minimum of 10.0 microseconds), then off, to complete the reset function.

Additionally, it should be noted that the interrupt disable control bit does not clear the interrupt level in the disabled state. A pending interrupt will occur when the interrupt is again enabled. The interrupt is disabled following a system master reset.

5.4 DATA REGISTERS

5.4.1 FIXED DISK DATA REGISTERS

The controller reserves system I/O address 1F0/170(H) for fixed disk programmed I/O data transfers and all system bus data transactions between the controller and the system processor at this address use the 16-bit word transfer bus mode. The controller (and AMAC array) provide read and write data 'pipeline' registers to allow the sector data memory to function as a dual port memory to support the 1:1 interleave format and multi-sector operations. For write operations (system to controller data transfers) the most significant byte (SD15/08) is written directly to a 8-bit storage register, while the LSB (SD07/00) is written to the AMAC 'post-write' pipeline register. The AMAC logic then writes both registered bytes to RAM in the interval between I/O cycles.

For read data transactions, the AMAC logic 'prefetches' the first data bytes to an internal AMAC register and external upper byte register. The first host input transfers data from these registers and initiates a prefetch of the next two bytes. Subsequent system read operations will transfer the MSB from the controller register and the LSB from the AMAC register and automatically prefetch the next bytes. The use of the pipeline registers permits memory access sharing between the host and the WD5010.

When the 'long' read or write mode is used the additional bytes must be transferred to or from the sector buffer using the system processor byte I/O mode. Refer to Figure 5-8 and 5-9 for a diagram of the read/write data transfer path and fixed disk data format.

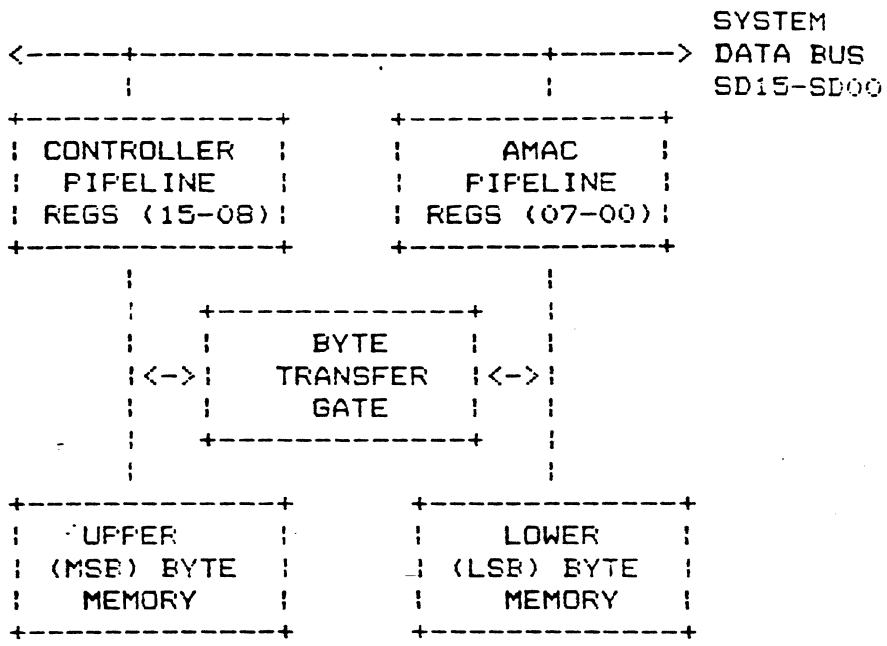


FIGURE 5-8
R/W DATA TRANSFER PATH

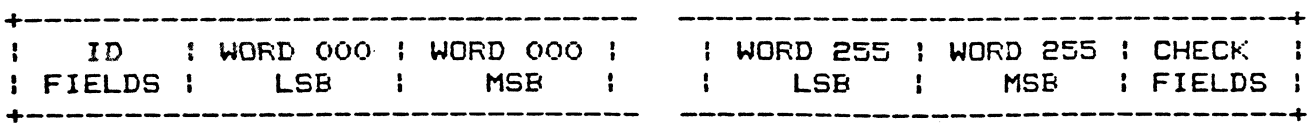


FIGURE 5-9
FIXED DISK (WORD) DATA FORMAT

5.5 SYSTEM INTERRUPTS

The controller requests fixed disk read/write data transfers via a system interrupt (IRQ14). The interrupt level is set by the WD1015 and will interrupt the system processor when the level is enabled (bit IDS in the auxiliary control register HDFDR reset) and the controller is not busy; i.e., a read sector is available for host transfer or a write sector is required. The interrupt level clears on any command from the system processor, programmed reset or master reset.

5.6 WD1015 COMMANDS

The WD1015 communicates with the AMAC support logic via a set of R/W commands at pre-set addresses. The commands are used internal to the controller only and are not available to the system processor. A description of each command is given in the AMAC specification.

ADDRESS	R/W	COMMAND
20	R/W	Host memory address block counter
21	R/W	WDC memory address block counter
22	W	Clear host memory address counter
22	R	Set sleep mode (clear busy)
23	W	Clear WDC memory address counter
23	R	Set 7 byte ECC mode
24	W	Set data request latch
24	R	Set interrupt
25	W	Set read mode
25	R	Set memory prefetch
26	W	Set multiple sector mode
26	R	Clear multiple sector mode
27	W	Set sector block counter
27	R	Set idle mode

FIGURE 5-10
CP SUPPORT COMMANDS

Addresses 00-07(H) and 10-17(H) are reserved for CP communication with the AMAC and WD5010 task file registers respectively. Address range 30-3F(H) is reserved for special IDE and command control.

NOTE: The two high order address bits are not used in the AMAC address decode of the WD1015 support commands. For example, the 'Set Multiple Mode' write command (26 hex) may appear in some of the referenced documentation as with the high order bits on (E6 hex).

5.7 BLOCK CONTROL

TO BE SUPPLIED

6.0 LOGIC DESCRIPTION

This section is intended to augment the descriptions of Sections 4 and 5 with a more detailed description of the controller logic with reference to the WD1006 schematic diagrams. It is assumed the reader is familiar with standard TTL components and conventional logic symbols. Further, it is necessary for the reader to be familiar with the referenced VLSI components (WD5010, WD1015, AMAC and WD10C20).

6.1 SIGNAL CHARACTERISTICS

6.1.1 LOGICAL NOTATION

Positive logic notation is used throughout and all signals which are active in the low state have the negation symbol (SIGNAL-) and are identified with the low state drawing identifier bubble; for example:

FUNCTION	DEFINITION			
	ELECTRICAL	LOGICAL	STATE	
SIGNAL	H	1 TRUE	ACTIVE, ASSERTED	
	L	0 FALSE		
SIGNAL-	L	1 TRUE	ACTIVE, ASSERTED	
	H	0 FALSE		

NOTE: The system bus signals which are active in the low state are shown with the negation symbol preceding the term (-SIGNAL). The controller logic diagrams follows this convention for system bus signals only.

6.1.2 ELECTRICAL DESCRIPTION

Signals that have the negation symbol have a logical/electrical relation that is:

LOGICAL STATE	ELECTRICAL STATE	RECEIVER	DRIVER
0	H = TTL HI STATE	5.25v>H>2.00v	5.25v>H>2.40v
1	L = TTL LO STATE	0.80v>L>0.50v	0.50v>L>0.00v

and signals that do not have the negation symbol have a logical/electrical relation that is:

LOGICAL STATE	ELECTRICAL STATE	RECEIVER	DRIVER
0	L = TTL LO STATE	0.80v>L>0.00v	0.50v>L>0.00v
1	H = TTL HI STATE	5.25v>H>2.00v	5.25v>H>2.40v

6.2 WD5010 WINCHESTER DISK CONTROLLER

The WD5010 Winchester disk controller device is shown on sheet 4. A complete description of the device and it's I/O signals is contained in the referenced documentation. It is important to note that the device data bus (WD7-0), register file address, chip select and read/write strobes connect directly to the AMAC where all bus switching, address selection, etc. is controlled.

The WD5010 accesses sector data memory via bus control and access arbitration logic in the AMAC device. Connection to the WD10C20 read/write controller is covered in the referenced WD10C20 documentation.

6.3 WD1015 BUFFER MANAGER CONTROL PROCESSOR

Primary control is provided by the WD1015 control processor (see sheet 5). The WD1015 can access registers in both the WD5010 and the AMAC array and functions primarily to aid in the execution of host generated commands, in management of the sector data buffer addressing and in error recovery procedures. The control processor also performs several module self-tests following a 'diagnose' command, master reset or programmed reset (refer to Section 8.0).

The processor input port (port 3) allows firmware interrupts from the WD5010 operation completion signal (INTRQ) and buffer request signal (BDRQ), the drive write fault signal and by the AMAC generated 'wakeup' signal (WAUP). The output port (port 2) is used to select the drive read/write head (HSEL3-0), to communicate with the WD5010 (BRDY and WF), to drive the activity indicator and to allow firmware enable/disable control of the drive control signals.

All processor program code and program-related data is stored in internal WD1015 ROM and RAM. The module RAM sector data buffer is restricted to disk read/ write data and the WD5010 ECC correction process; i.e., it is not used to store WD1015 program variables. The firmware descriptions and listings are contained in separate WD1015 and firmware 'protocol' specifications.

6.4 WD10C20 READ/WRITE CONTROLLER

Read data/clock separation and write data pre-compensation is accomplishe by the WD10C20 read/write controller. The controller is shown on sheet 4 of the logic diagrams. The WD10C20 and all associated components have their value and board positioning defined by a WD standard cell (see referenced documentation).

6.5 BUFFER MANAGER GATE ARRAY

The WD12C00-22 gate array logic is shown as a single logic block on sheet 3. The primary function of the AMAC logic is to provide host address and command decoding, task file control and status image registers, data transfer pipeline registers, bus controls and sector data RAM address control (see Figure 6-1).

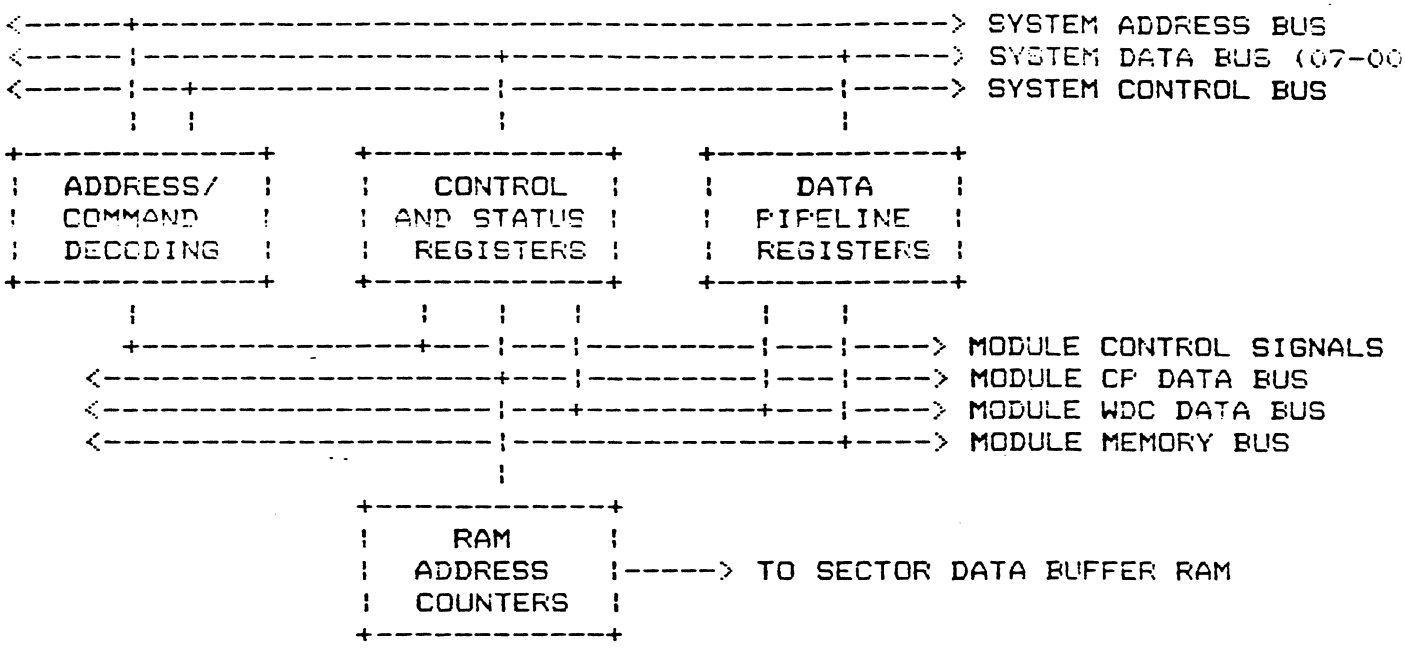


FIGURE 6-1
AMAC BLOCK DIAGRAM

6.5.2 ADDRESS DECODE

The AMAC device address and command decoding range is externally selected by the decode PAL and jumper select shown on the left portion of sheet 3. The decoding logic controls the host task file and auxiliary register address ranges (1F0-7/170-7 and 3F6-7/376-7). Individual register decoding is provided internal to the AMAC.

6.5.3 TASK FILE REGISTERS

The control and status task file registers within the AMAC are an image of the normal WD5010 registers. The host has access to the AMAC registers (only) while the control processor can access both the AMAC and WD5010 register set.

6.5.3 DATA PIPELINE REGISTERS

The lower byte data transfer pipeline registers for both host and WDC input prefetch and output postwrite are included in the AMAC. These registers (and their external upper byte equivalent) with their associate control logic allow the module to perform the concurrent host and WDC data memory access necessary for multi-sector 1:1 interleave operation. This necessity requires the AMAC to arbitrate simultaneous host and WDC requests and to gate the appropriate address counter to external memory. See Figure 6-2 for a simple timing and arbitration illustration.

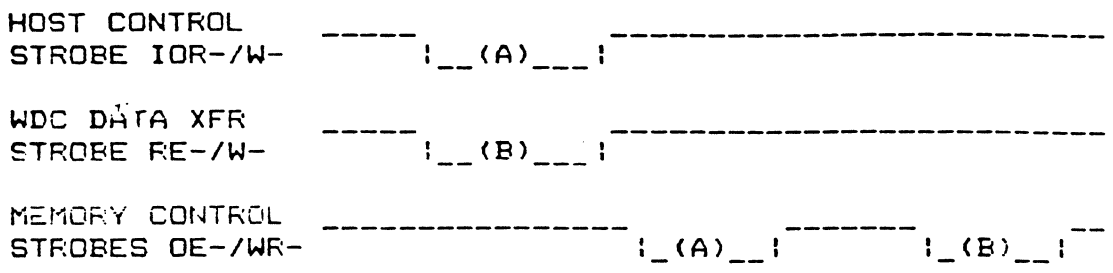


FIGURE 6-2
AMAC TIMING ILLUSTRATION

The timing of the two AMAC generated strobes is controlled by a clocked sequencer that resolves priority (in favor of the host request) and generates the external memory (and byte transfer gate) control signals.

6.5.4 MEMORY ADDRESS COUNTERS

The RAM address counters (host and WDC) are sequential 14-bit counters with the multiplexed high order 13 bits addressing the two 8K controller memories (the low order byte control is provided by the AMAC internal logic).

6.5.5 AMAC EQUATIONS

Refer to AMAC Engineering Specification

6.6 SYSTEM BUS INTERFACE

Sheet 3 shows the system bus address, data and control interface signals. It is particularly important to note that the I/O address lines (SA09-00) and the address control signal (AEN) connect to the address decode PAL fo module selection and lines SA9 and SA2-0 connect to the AMAC for individual register addressing. The low order data byte (SD07-00) connects directly to the AMAC and the device provides the necessary bus drive current. Figure 6-3 illustrates the I/O read and write signal relationship. The signal timing specification is included in Section 9.

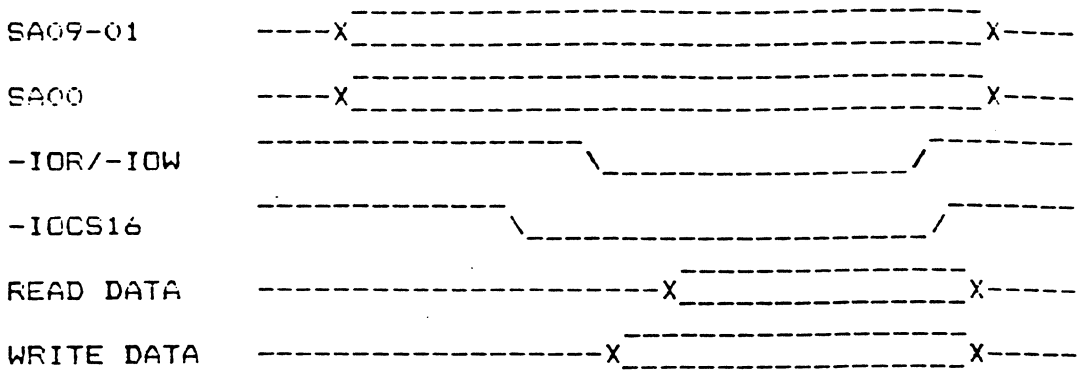


FIGURE 6-3
SYSTEM BUS SIGNALS
PROGRAMMED I/O CONTROL

6.7 FIXED DISK DRIVE INTERFACE

Sheets 4 and 5 show the data and control interface to the disk drives.

6.7.1 CONTROL INTERFACE

The control input signals (sheet 4) are terminated with standard 220/330 ohm line terminators and buffered by 74LS14 Schmitt Trigger inverters. The Index, Seek Complete, Write Fault and Drive Ready signals connect to the WD5010 and AMAC for control and status information. The drive cylinder positioning control signals (STEP- and DIRIN-) are output by the WD5010 and buffered by 7406 open-collector drivers.

Sheet 5 also shows the drive select, drive head select and write gate control drivers (type 7438). It should be noted that the control drivers can be disabled by the control processor or by a module reset condition.

6.7.2 R/W DATA INTERFACE

U1 and U2 are the differential data drivers and receivers for each of two drives and connect to separate radial data cables - refer to WD10C20 documentation for a complete description of the fixed disk read data separation and write data precompensation control.

6.8 BUFFER MEMORY

The RAM data buffer memory is shown on sheet 3. The RAM address is provided by the multiplexed output of the host and WD5010 address counter from the AMAC. The RAM chip select inputs (CS1- and CS2) are always enabled with the RAM write and output enable signals generated by the AMA logic.

6.9 CLOCK OSCILLATOR

The WD1015 and WD10C20 clock inputs are driven by a 10MHZ crystal oscillator (refer to sheet 5). The WD10C20 generates the WD5010 controller 5 MHZ write clock input.

6.10 MODULE RESET CIRCUIT

The module power on and low VCC monitor reset control circuitry is shown on sheet 3. Resistor R11 and Zener diode Q3 set the low VCC trip point at approximately 4.4 volts. The AMAC logic includes a clocked delay counter (approximately 12 milliseconds at a 10 MHZ input) to provide an adequate power on reset interval and to insure the module clock is operative.

6.11 LED DRIVER

The LED (activity) indicator driver and connector are shown on Sheet 4. The driver is controlled by the WD1015 and indicates controller activity. A current limiting resistor on the controller limits the indicator current to approximately 20 milliamperes.

6.12 BIOS ROM OPTION

TO BE SUPPLIED

6.13 WAIT STATE CONTROL OPTION

TO BE SUPPLIED

7.0 INSTALLATION

The controller module may be installed in any suitable PC slot that provides both the P1 and P2 connectors.

7.1 MECHANICAL

Figure 7-1 illustrates the general module IC placement and approximate drive connector locations. The module dimensions are 13.12 by 4.2 inches and a mounting bracket is included.

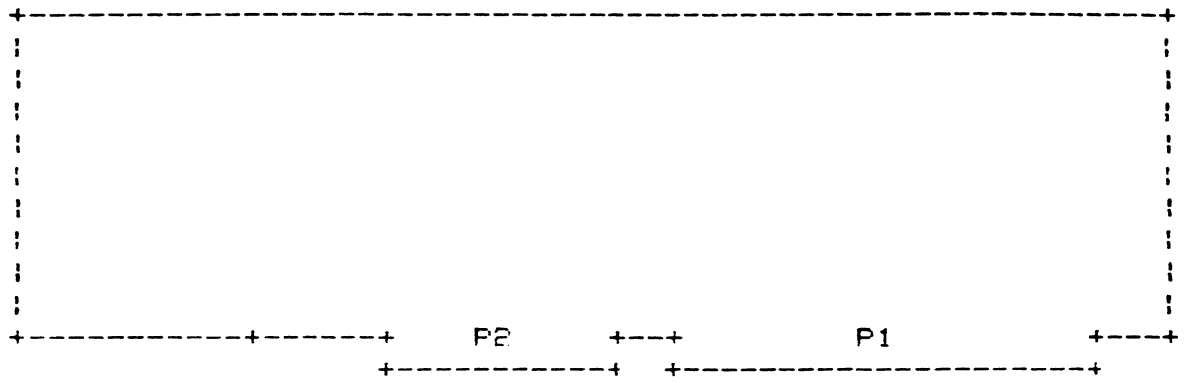


FIGURE 7-1
controller MODULE LAYOUT

7.2 ADDRESS SELECT JUMPERS

The module primary address range (1F0-1F7 and 3F6-3F7) is factory selecte by circuit etch at address jumper positions W31-W32. The secondary address range (170-177 and 376-377) is selected by cutting the circuit etch and adding a jumper to positions W32-W33.

7.3 MODE SELECT JUMPERS

7.3.1 DISK DRIVER CONTROL

Module jumper position W41-W42 enables the drive control drivers only whe the WD1015 asserts the active signal or when the host reads the controlle status or diagnostic registers. Positions W42-W43 enables the drivers i all cases except reset.

7.3.2 DIAGNOSTIC REGISTER LATCH CONTROL

Jumper position W101-W102 enables the diagnostic Digital Input Register t operate in the non-latched mode; i.e., the register outputs are allowed t follow the inputs. Position W102-W103 latches the input signals (preventing output change) when the register is read.

7.3.3 WD1015 MODE CONTROL

Jumpers W71, W72, W73, W81, W82 and W83 are used to provide two external mode selects to the control processor. The modes are not currently defined.

7.3.4 HEAD SELECT/RWC CONTROL

The head select 3 output is controlled by jumper position W11-W12 and is required for 16 head drives. Position W12-W13 outputs the WD5010 reduced write current signal on the same control connector pin. The 16 head mode is factory selected by circuit etch at position W11-W12.

7.3.5 I/O Channel Wait State Control

Jumper positions W21-W22, W23-W24 and W25-W26 are used to select 0, 1 or 2 bus wait states for the 16-bit I/O data transfers. The wait state generator is timed by the system bus clock.

7.3.6 BIOS ROM TYPE SELECT

Position W91-W92 is used to select BIOS ROM type 2716. Jumper W92-W93 is factory selected by circuit etch for types 2732 and 2764. The ROM socket is designed to accommodate any of the three types.

7.3.7 BIOS ROM ADDRESS MAP SELECT

The ROM system memory map address is selected by jumpers W51-W52 and W61-W62 as inputs to an address decode PAL - see referenced PAL specification for decode equations.

7.4 MOUNTING BRACKET JUMPER

Jumper connection W111-W112 is provided to allow grounding of the module mounting bracket to board logic ground. The jumper is not installed at the factory and is not normally used.

8.0 TESTING

8.1 CONTROLLER SELF TESTS

The encoded result descriptors for each controller self test are shown in Figure 8-1. The controller error register HDERR (hex address 1F1/171) is used to report the test result. The tests are executed following the 'diagnose' command or any reset.

The tests verify the WD1015 firmware checksum, the WD1015 RAM memory, the sector buffer RAM memory and the WD5010 and AMAC data paths. System bus or host interactive tests are not included.

RESULT	DESCRIPTION
01	No Errors
02	Controller Error
03	Sector Buffer Error
04	AMAC Device Error
05	Control Processor Error
06-FF	Undefined

FIGURE 8-1
SELF TEST ERROR CODES

where: 02 = WD1015/WD5010 register access error

03 = Sector buffer data error

04 = WD1015/AMAC register access error

05 = WD1015 ROM checksum error
= WD1015 RAM data error

8.2 SYSTEM TESTS

Module software tests designed to operate in the PC-AT system are not covered in this document. These tests would include the WD HDT/DAD diagnostic tests or any host test software.

9.0 GENERAL SPECIFICATIONS

9.1 POWER AND ENVIRONMENTAL

9.1.1 Power Requirements

+5 VDC	+/- 5.0%	< 1.000 amps
+12 VDC	+/- 10.0%	< 0.010 amps

9.1.2 Environmental

Temperature	
Operating	10 to 50 degrees celsius
Non-operating	-40 to 60 degrees celsius
Humidity	
Operating	8% to 85% non-condensing
Non-operating	5% to 95% non-condensing
Shock and Vibration	
Shock	35G/20MS square wave maximum
Vibration	1G/0-600Hz, dwell not to exceed 30 seconds at (any) resonance
Altitude	
Operating	0 to 3000 meters maximum
Non-operating	0 to 5000 meters maximum

9.2 FIXED DISK

9.2.1 RECORDING SPECIFICATIONS

Encoding Method	MFM
Data Rate	5.0 MBS
Sector format	512 bytes/sector, 17 sectors/track soft sectored format standard, 128 256 and 1024 bytes/sector available
Drives supported	2 maximum
Heads supported	16 maximum
Tracks supported	32,768 maximum (2048 cylinders)
Hard Error Rate	less than 1 per 10(E12) bits read
Soft Error Rate	less than 1 per 10(E10) bits read
Seek Error Rate	less than 1 per 10(E06) seeks

9.2.2 FIXED DISK READ/WRITE CONTROLLER SPECIFICATIONS

Maximum Acqusition time	12 usec @ 5.0 mbs/sec
Jitter rejection	> 35 db @ 2.5 MHz > 40 db when tracking
Bit Error Rate	<10(E10)
Bit Jitter Tolerance	+/- 34 nsec
W/C Asymmetry Margin	+/- 20 nsec
Kd-Pump Output	4/2 ma at pump pin
Ko-VCO Gain	5% per volt

9.2.3 ERROR CORRECTION SPECIFICATIONS

Method	Polynomial division
Degree	32
Forward polynomial	X^32 + X^28 + X^26 + X^19 + X^17 + X^10 + X^06 + X^02 + 1
Reciprocal polynomial	X^32 + X^30 + X^26 + X^22 + X^15 + X^13 + X^06 + X^04 + 1
Record length (r)	516 X 8 bits standard
Correction span (b)	5 bits
Single burst detection span	r = 516 X 8
With b = 0	32 bits
With b = 5	19 bits
Double burst detection span	r = 516 X 8
With b = 0	>3 bits
With b = 5	3 bits
Non-detection probability	(r = 516 X 8, b = 5) = 2.3(E-10)
Miscorrection probability	(r = 516 X 8, b = 5) = 1.57(E-5)

9.3 DRIVE INTERFACE

All control and data drivers, receivers and signal terminations are per the ST-412 interface specification. Drive attachment is restricted to two units. Drives with up to sixteen heads are supported.

9.3.1 FIXED DISK DRIVE CONTROL CONNECTOR

WD Part No. LE-8805 (Berg type 65610-134), Pin 15 polarization

9.3.2 FIXED DISK DATA CONNECTORS

WD Part No. LE-8804 (Berg type 65610-120), Pin 8 polarization

9.3.3 LED Connector

WD Part No. 41-001008-00 (Berg type 65500-104)

9.4 SYSTEM BUS INTERFACE

Programmed I/O is used for all fixed disk control and data transactions. All data transfers are 16-bits and use the channel 'fast I/O' protocol. All control transfers are 8-bits wide and use the lower bus data byte. The module I/O primary and secondary address ranges (1F0-1F7, 3F6-3F7 and 170-177, 376-377) and priority interrupt assignment (IRQ14) are fixed.

Bus loading for all controller input signals will not exceed 2 standard LSTTL loads in either logic sense. Module output low state sink current (Iol) at Vol = 0.4 volts is 12 ma. on all tri-state outputs and 16 ma. on open collector output -IOCS16.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
	-IOCS16 from SA09-01		78	nsec
	-IOCS16 from SA00		63	nsec
	+IOCS16 from +IOR/+IOW		80	nsec
	SD15-08 from -IOR		55	nsec
	SD07-00 from -IOR		85	nsec
	SD15-08 HIZ from +IOR		55	nsec
	SD07-00 HIZ from +IOR		87	nsec
	SD15-00 setup to +IOW	60		nsec
	+IOW to SD15-00 HIZ (hold time)	50		nsec
	-IOR/-IOW pulse width (16 bit I/O)	160		nsec
	-IOR/-IOW pulse width (8 bit I/O)	540		nsec
	+IOR/+IOW to -IOR/-IOW (16 bit I/O)	375		nsec

FIGURE 9-1
SYSTEM BUS TIMING CHARACTERISTICS

APPENDIX

A. SYSTEM BUS CONNECTOR P1

Fins and signals are viewed as looking down at the connector with the module component side to the right.

B01	GND	A01	
B02	RESET	A02	SD07
B03	VCC	A03	SD06
B04		A04	SD05
B05		A05	SD04
B06		A06	SD03
B07		A07	SD02
B08		A08	SD01
B09	+12VDC	A09	SD00
B10	GND	A10	I/OCHRDY
B11		A11	AEN
B12	-SMEMR	A12	SA19
B13	-IOW	A13	SA18
B14	-IOR	A14	SA17
B15		A15	SA16
B16		A16	SA15
B17		A17	SA14
B18		A18	SA13
B19		A19	SA12
B20	SYSCLK	A20	SA11
B21		A21	SA10
B22		A22	SA09
B23		A23	SA08
B24		A24	SA07
B25		A25	SA06
B26		A26	SA05
B27		A27	SA04
B28	BALE	A28	SA03
B29	VCC	A29	SA02
B30		A30	SA01
B31	GND	A31	SA00

B. SYSTEM BUS CONNECTOR P2

Pins and signals viewed as looking down on the connector with the module component side to the right

D01		C01	
D02	-I/OCS16	C02	
D03		C03	
D04		C04	
D05		C05	
D06		C06	
D07	IRQ14	C07	
D08		C08	
D09		C09	
D10		C10	
D11		C11	SD08
D12		C12	SD09
D13		C13	SD10
D14		C14	SD11
D15		C15	SD12
D16	VCC	C16	SD13
D17		C17	SD14
D18	GND	C18	SD15

C. FIXED DISK DRIVE CONTROL CONNECTOR J5

Drive control connector viewed as looking at the connector from module component side. (WD connector type LE-8805)

01	GND	02	HS3-
03	GND	04	HS2-
05	GND	06	WG-
07	GND	08	SC-
09	GND	10	TRK00-
11	GND	12	WF-
13	GND	14	HS0-
15	KEY	16	RESERVED
17	GND	18	HS1-
19	GND	20	INDEX-
21	GND	22	RDY-
23	GND	24	STEP-
25	GND	26	DS1-
27	GND	28	DS2-
29	GND	30	RESERVED
31	GND	32	RESERVED
33	GND	34	DIRIN-

D. FIXED DISK DRIVE DATA CONNECTORS J4/J3

The drive data connectors are shown as looking at the connector from the module component side. (WD connector type LE-8804)

01	RESERVED	02	GND
03	RESERVED	04	GND
05	SPARE	06	GND
07	RESERVED	08	KEY
09	NU	10	NU
11	GND	12	GND
13	WMFM1/2(+)	14	WMFM1/2(-)
15	GND	16	GND
17	RMFM1/2(+)	18	RMFM1/2(-)
19	GND	20	GND

E. EXTERNAL INDICATOR CONNECTOR J6

(WD connector type 41-001008-00)

01	LED+	02	LED-
03	LED-	04	LED+