WESTERN DIGITAL
CORPORATION

FILE

WD1003-WA2

WINCHESTER DISK/FLOPPY DISKETTE

CONTROLLER

PRELIMINARY OEM MANUAL

3/06/86

WD1003-WA2

Features

IBM® 100% PC AT Compatible Winchester and Floppy Controller

Controls 1 or 2 5¼" Winchester Drives (ST506/ST412)

Controls 1 or 2 Floppy Drives at Four Data Rates

Based on Industry Standard WD2010B-10 Winchester Controller Chip

Self-Adjusting Data Separator, WD10C20

On-Board Diagnostics

16-Bit Data Bus

Concurrent Transfers on a Floppy and a Winchester Drive

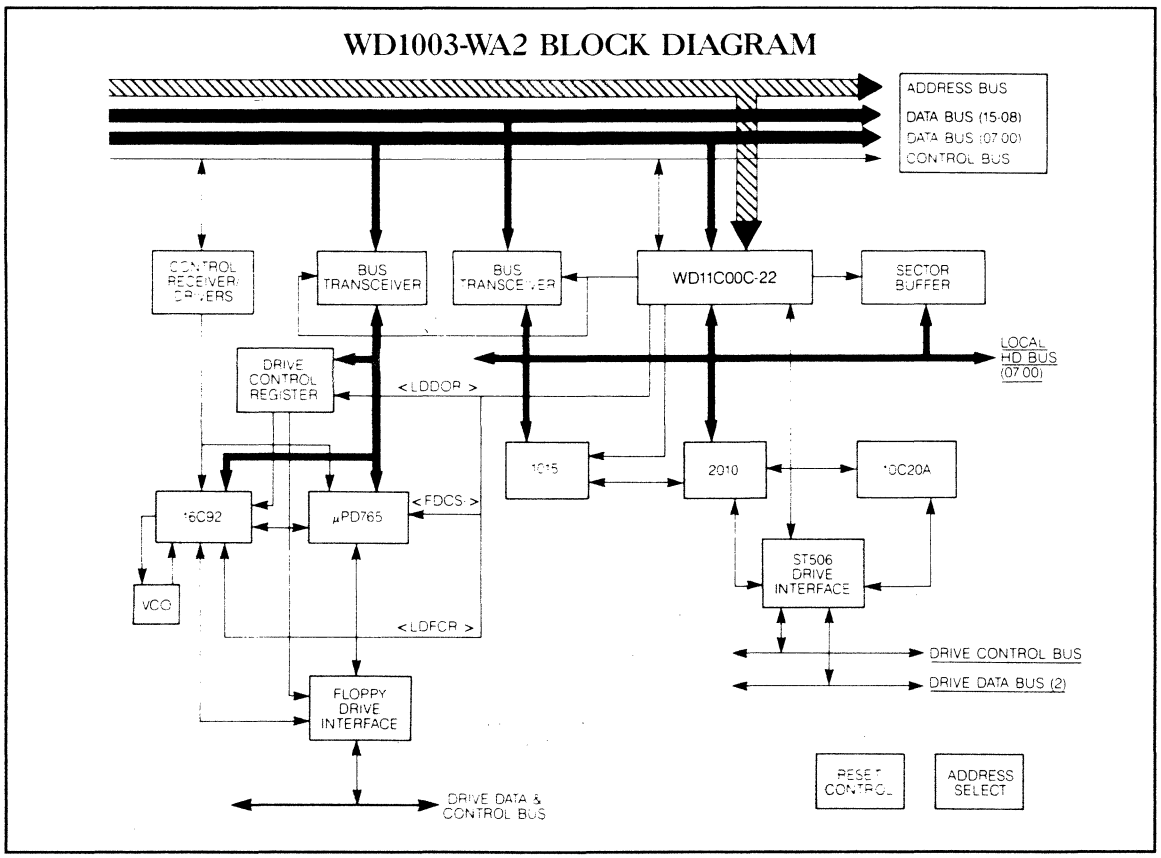
Certified to Comply with the Limits for a Class B Computing Device Pursuant to Subpart J of Part 15 of F.C.C. Rules

Description

The WD1003-WA2 is a storage controller that interfaces up to two rigid Winchester disk drives and up to two floppy disk drives to the IBM Personal Computer, model AT and compatibles.

The controller is based on Western Digital's industry standard Winchester controller device, the WD2010B-10, and on a self-adjusting Data Separator device, the WD10C20A-05. In addition, three other proprietary Western Digital devices are incorporated on the board, including WD11C00C-22 (Buffer Manager & Controller), WD16C92 (Floppy Read-Write Support Device) and WD1015-37A (Processor).

The WD1003-WA2 controls one or two ST506/ST412 Winchester disk drives and



WESTERN DIGITAL

Winchester/Floppy Disk Controller

one or two floppy disk drives. The Winchester interface accepts a 5 megabit per second data rate. The controller board supports drives with up to 16 read/write heads and 2048 cylinders.

The data rate for the floppy disk interface is programmable between 125Kbps, 250Kbps, 300Kbps, and 500Kbps.

The WD1003-WA2 contains all of the logic required for Winchester/floppy drive control, the Host interface, 32-bit error correction, data separation, and write precompensation.

A total storage solution for PC-AT compatibles is offered by Western Digital in this single board controller. Advanced LSI devices are used to achieve low cost/high performance storage control.

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W1131 3/87 5M

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F.C.C. CERTIFICATION

This Western Digital product has been certified to comply with the limits for a Class B computing device pursuant to Subpart J of Part 15 of F.C.C. Rules. This does not guarantee that interference will not occur in individual installations. Western Digital is not responsible for any television, radio, or other interference caused by unauthorized modifications of this product.

If interference problems do occur, please consult the system equipment owner's manual for suggestions. Some of these suggestions include relocation of the computer system away from the television or radio or placing the computer AC power connection on another circuit or outlet.

This product was tested and certified with external shielded interconnecting cable(s). Therefore, shieled cable(s) is(are) required to be used with this product.

IBM Personal Computer AT is a registered trademark of International Business Machines Corporation.

SECTION 1
INTRODUCTION

1.1 DOCUMENT SCOPE

This document provides the user with the information required to design related software drivers and interface connections for efficient use of the WD1003-WA2 Winchester/Floppy Controller Board. It is to the user's advantage to become familiar with the following related documents:

WD11C00A-22 IBM PC-AT Interface Controller Device - - Data Sheet
WD10C20 Winchester Data Separator and Write
Precompensation Device - - - - - - - - - - - - Data Sheet
WD2010-05 Winchester Disk Controller - - - - - - - Data Sheet
WD1015 Buffer Manager Control Processor - - - - - Data Sheet
uPD765A Single/Double Density Floppy Disk Controller - Data Sheet
NEC Electronics U.S.A. Inc.
Microcomputer Division
Natick, Massachusetts
ST-506 Micro Winchester Disk Interface - - - - - - - ST506
Seagate Technology
Scotts Valley, California

1.2 DESCRIPTION

The WD1003-WA2 is an IBM Personal Computer AT bus compatible Winchester/Floppy disk controller designed to interface up to two Winchester and up to two floppy disk drives. The board permits the concurrent operation of one floppy and one fixed disk drive. The Winchester drive interface is compatible to the Seagate Technology ST506/ST412 standard interface for 5 Mbs hard disk drives. The floppy disk drive interface supports 1.2 MB, 360 RPM drives as well as 360 kB (SA450) drives. The WD1003-WA2 includes all necessary receivers and drivers to allow direct connection to the drive(s).

1.3 FEATURES

- IBM PERSONAL COMPUTER AT COMPATIBLE WINCHESTER AND FLOPPY CONTROLLER
- CONTROLS UP TO TWO WINCHESTER DRIVES (ST506/ST412, 16 R/W HEADS EACH, 2048 CYLINDERS)
- CONTROLS UP TO TWO FLOPPY DISK DRIVES
  - DOUBLE-SIDED
  - DOUBLE DENSITY (360 kB, 250 kbs, MFM)
  - QUAD DENSITY (1.2 MB, 500 kbs, MFM)
  - FOUR DATA RATES (500 kbs, 300 kbs, 250 kbs, and 125 kbs)
  - SUPPORTS 360 AND 300 RPM SPINDLE SPEED
- WD2010A-05 WINCHESTER DISK CONTROLLER
- 8-BIT, BI-DIRECTIONAL BUS HOST INTERFACE FOR CONTROL AND STATUS TRANSFERS
- HIGH-SPEED, 16-BIT PIO DATA TRANSFERS
- 32-BIT ECC FOR WINCHESTER ERROR DETECTION AND CORRECTION, CRC FOR ID FIELDS
- DIAGNOSTIC MODE FOR ERROR CHECKING
- WD10C20 DATA SEPARATOR AND WRITE PRECOMPENSATION DEVICE
- WD11C00A-22 IBM PC-AT INTERFACE CONTROLLER AND WD16C92-00 FLOPPY DISK READ/WRITE CONTROLLER (FRWC) REDUCE POWER CONSUMTION AND COMPONENT COUNT
- ALLOWS CONCURRENT OPERATION OF ONE FLOPPY AND ONE WINCHESTER DRIVE

1.4 ARCHITECTURE

The WD1003-WA2 is based on the WD11C00A-22 IBM PC-AT Interface Controller device, WD2010A-05 Winchester Disk Controller, WD1015-37 Buffer Manager Control Processor WD10C20 Winchester Data Separator and Write Precompensation Device. 1K x 8 static RAM devices as a Sector Buffer, WD16C92-00 Floppy Disk Read/Write Controller, and an NEC uPD765A Floppy Disk Controller. Figure 1-1 is a functional block diagram of the WD1003-WA2.

1.4.1 WD11C00A-22

The WD11C00A-22 incorporates several functions in a single package. Implementation of these functions occurs by combining random logic and specialized circuits. The WD11C00A-22 performs the following functions:

Host hardware interface
Sector Buffer addressing and control
IRQ generation
Winchester head selection
WD1015-37 Wakeup
Controls Winchester activity LED
Addresses WD2010A-05 Task Files
Receives command and error information from WD1015-37

1.4.2 WD2010A-05 WINCHESTER DISK CONTROLLER

The WD2010A-05 controls all data transfers between the Sector Buffer and the drives. The WD2010A-05 performs multiple sector Read/Write, Implied and Buffered Seek commands. The WD2010A-05 also executes programmable format and error recovery algorithms. All Winchester commands are executed through the seven Task Files of the WD2010A-05 after limited intervention by the WD1015-37.

1.4.3 WD1015-37 BUFFER MANAGER CONTROL PROCESSOR

The WD1015-37 is an 8-bit microprocessor that controls and coordinates the activity of the Winchester disk drives and WD2010A-05. The WD1015-37 receives and sends command or status information over the internal WD1003-WA2 multiplexed address/data bus, HD0 through HD7. Controlling firmware resides in the WD1015-37's 2K internal ROM.

1.4.4 WD10C20 WINCHESTER DATA SEPARATOR AND WRITE PRECOMPENSATION DEVICE

The WD10C20 performs phase-locked loop data synchronization on read data from the Winchester drives. This device also conditions write data to be recorded on the disk. The WD10C20 includes both frequency and phase detection. Zero phase error start-up circuitry eliminates problems due to asymmetry. The WD10C20 requires no adjustments and contains all data separation circuitry in a single device.

1.4.5 SECTOR BUFFER RAM

The Sector Buffer is a 1K x 8 RAM used for storing data between transfer operations. Since the WD2010A-05 and WD1015-37 are 8-bit devices, the WD11C00A-22 separates each 16 bit word from the Host into two 8-bit bytes. The WD11C00-22 controls the placement of each 8-bit byte in the Sector Buffer. For data transfers to the Host, the WD11C00-22 assembles 8-bit bytes into 16-bit words. The Sector Buffer never contains more than 512 bytes.

1.4.6 WD16C92-00

The WD16C92 is a single chip support device for the NEC uPD765A. Control of the floppy disk data transfer rates is one of the functions of the WD16C92. Data transfer rates controlled by the WD16C92 are 500 kbs (MFM), 300 kbs (MFM), 250 kbs (MFM), and 125 kbs (FM). Other support functions provided by the WD16C92 include phase detection, pulse shaping, and clock generation for read data and write precompensation (+ 125 nsec write precompensation for all data rates except 300 kbs. 208.3 nsec write precompensation for 300 kbs.), write data clock, INTERRUPT REQUEST 6 (IRQ6) and DMA REQUEST 2 (DRQ2) generation. Specialized support functions furnished by the WD16C92 are phase locked loop gain selection and DRQ pulse delay. (Pulse delay is necessary to comply with AT timing constraints.) The only external circuitry required by the WD16C92 is a 24 MHz crystal, error amplifier, and dual voltage controlled oscillators (VCOs). Dual VCOs are necessary because the 300 kbs data rate is not a multiple of the 125 kbs data rate. VCO selection is performed by the WD16C92.

1.4.7 uPD765A SINGLE/DOUBLE DENSITY FLOPPY DISK CONTROLLER

The NEC uPD765A is a floppy disk controller. Host control over the NEC uPD765A is complete. No on-board processor controls the floppy controller. Floppy transfers are made in DMA mode. All floppy commands are supported.

NOTE

Refer to the NEC Microcomputer Division Catalog for more detailed information on this device. Where differences exist, the values and descriptions in this data sheet take precedence over the NEC documentation. For example, the sector size is set at 512 bytes per sector by the AT BIOS even though the NEC controller allows programmable sector sizes.

BLOCK DIAGRAM TBS

FIGURE 1-1. WD1003-WA2 BLOCK DIAGRAM

SECTION 2
SPECIFICATIONS

2.1 GENERAL

This section contains the overall specifications for the WD1003 WA2 Winchester/Floppy Disk Controller.

2.2 ELECTRICAL

2.2.1 HOST INTERFACE

Type	IBM Personnal Computer AT
Max Cable Length	Connects directly to Host motherboard with 62 pin and 36 pin card edge connectors

2.2.2 DRIVE INTERFACE

	Winchester Disk	Floppy Disk
Type	ST506/ST412 compatible	SA450 or Teac 55F/G-compatible
Max Cable Length:		
Control (Total Daisy Chain)	3 meters (10 feet)	
Data (Radial-each)	3 meters (10 feet)	
Signal (Flat or Twisted Pair - Total Daisy Chain)		6 meters (20 feet)

2.2.2.1 Recording Specifications

Encoding Method	MFM	FM and MFM
Data Rate	5Mbs	125kbs, 250kbs, 300kbs, 500kbs
Format	IBM AT compatible	IBM AT compatible
Sectoring	Soft, 512 byte by 17 per track (Numbered 1 through 17)	Soft, up to 15 by 512 byte sectors per track
Cylinders	2048	160 max
Heads	16 max	2 max
Drives	2	2
Soft Error Rate	1 in 10E10 bits read	1 in 10E09 bits read
Hard Error Rate	1 in 10E12 bits read	1 in 10E12 bits read
Seek Error Rate	1 in 10E6 seeks	1 in 10E6 seeks

2.2.2.1 Recording Specifications (CONT'D.)

	Winchester Disk	Floppy Disk
Precompensation	+/- 12 nsec, single-level MFM	+/- 125 nsec write pre-compensation for all data rates except 300 kbs. 208.3 nsec for 300 kbs
Interleave Factor	2 to 1 min	---
CRC Polynomial	x^16+x^12+x^5+1	
ECC Polynomial	x^32+x^28+x^26+x^19+ x^17+x^10+x^6+x^2+1	
ECC Polynomial Reciprocal	x^32+x^30+x^26+x^22+ x^15+x^13+x^6+x^4+1	
Record length (r)	516 x 8 bits max	
Correction span (b)	5 bits	
Single burst detection span	r = 516 x 8	
b = 0	32 bits	
b = 5	19 bits	
Double burst detection span	r = 516 x 8	
b = 0	> 3 bits	
b = 5	3 bits	
Non-detection probability	2.3 (E-10), r = 516 x 8, b = 5	
Miscorrection probability	1.57 (E-5), r = 516 x 8, b = 5	
ID Field CRC Polynomial		x^16+x^12+ x05+1
Data Field CRC Polynomial		x^16+x^12+ x^05+1

2.2.2.2 Read/Write Control Specifications

	Winchester Disk	Floppy Disk
Type	WD10C20	Analog with
Features	self-adjusting VCO reference clock, 0 phase startup, read pulse extension, DRUN generation, write precompensation	dual R-C VCO adjustment free VCO
Acquisition Time	12 usec at 5.0 Mbs	8 bytes max for MFM 4 bytes max for FM
Capture Range	+3% min	±5% min
Bit Jitter Tolerance	± 34 nsec	60% min of window
Jitter Rejection	>35 db at 2.5 MHz >40 db when tracking	
Bit Error Rate	<10(E10)	
W/C Asymmetry Margin	± 20 nsec	
Kd-Pump Output	4/2 mA at pump pin	
Ko-VCO Gain	5% per volt	
Phase Error		+/-10 deg

2.3 POWER

Logic Supply	+5V+5%, 1.2 A max
Supply Ripple	+100mV, p-p
Analog Supply 1	+12V+10%, 0.02 A max
Supply Ripple	+100 mV, p-p
Analog Supply 2	-12V+10%, 0.01 A max
Supply Ripple	+/-100 mV, p-p

2.4 PHYSICAL

Length	33.3 centimeters (13.1 inches)
Width	12.2 centimeters (4.80 inches)
Height	1.90 centimeters (0.75 inches)

2.5 ENVIRONMENTAL

2.5.1 TEMPERATURE

Operating	10 C to 50 C (50 F to 122 F)
Non-operating	-40oC to 60oC (-40oF to 140oF)

2.5.2 AIR FLOW

100 LFM min constant unidirectional, measured on a plane 1/4 in. equidistant from PCB surface.

2.5.3 HUMIDITY

Operating	8% to 80% non-condensing
Non-operating	5% to 95% non-condensing

2.5.4 ALTITUDE

Operating	0 to 3000 meters (0 to 10000 feet)
Non-operating	0 to 5000 meters (0 to 16000 feet)

2.5.5 VIBRATION

Operating	6 to 600 Hz at 1.0 G

2.6 MEAN TIME BETWEEN FAILURE (MTBF) AND MEAN TIME TO REPAIR (MTTR)

MTBF	100,000 POH
MTTR	30

SECTION 3
INTERFACE CONNECTIONS

3.1 ORGANIZATION

The WD1003-WA2 has seven interface connectors for user application.

P1 Host interface: 62 pin card edge connector
Component side - Pins A1 through A31
Conductor side - Pins B1 through B31

P2 Host interface: 36 pin card edge connector
Component side - Pins C1 through C18
Conductor side - Pins D1 through D18

J5 Winchester drive control: 34 pin dual row connector daisy chained to two drives. The control signals at the second drive from the WD1003-WA2 (no more than a total length of 3 meters or 10 feet) are terminated with a 220 ohm resistor to +5V and a 330 ohm resistor to ground.

J4, J3 Winchester drive data: 20 pin dual row header connectors, radially connected to the drives.

J1 Floppy control and data: 34 pin cable connector.

J6 Winchester activity LED connector: A 4 pin header that connects via cable to the Winchester front panel. The WD1003-WA2 lights the LED when the Winchester drive is busy or the Host asserts RESET.

3.2 HOST INTERFACE

P1, side A, plugs into the lower half (SD7 thru SD0) of the 16 bit Host data bus (SD15 thru SD0) and the Host address bus. SD7 thru SD0 transmit data and status information. P2, side C, plugs into the upper half (SD8 thru SD15) of the 16-bit Host data bus (SD15 thru SD0). SD8 thru SD15 transmit data only. P1, side B, and P2, side D, plug into the Host system control bus. Table 3-1 describes P1 pin assignments in detail. Table 3-2 describes P2 pin assignments in detail.

TABLE 3-1 HOST INTERFACE CONNECTOR (P1) PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
A1,A10, A12 thru A21	NC	NOT CONNECTED		
A2 thru A9	SD7 thru SD0	DATA BUS BITS 7 thru 0	I/O	Bi-directional, lower 8-bit data bus for data and status communication between the controller and the Host.
A11	AEN	ADDRESS ENABLE	I	When AEN is asserted, the DMA controller assumes control of the Host address bus, control bus, and data bus. I/O port adresses are no longer genera ted for I/O port access. In this mode, the I/O port is se lected by asserting DACK2-.
A22 thru A31	A9 thru A0	ADDRESS BUS BITS 9 thru 0	I	A 10-bit address bus for I/O port addressing by the Host.
B1,B10 B31	GND	GROUND		
B2	RST	RESET	I	When asserted, RST forces the WD1003-WA2 board into the ini- tial power-up state.
B3,B29	+5VDC	+5VDC		+5VDC
B6	DRQ2	DMA REQUEST CHANNEL 2		DRQ2 is asserted whenever data is available for transfer between the WD1003-WA2 under DMA control. Applies to floppy controller only.
B7	-12VDC	-12VDC		-12VDC
B9	+12VDC	+12VDC		+12VDC

TABLE 3-1 HOST INTERFACE CONNECTOR (P1) PIN DESCRIPTION (CONT'D.)

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
B4,B5, B8,B11, B12	NC	NOT CONNECTED		
B13	IOW-	I/O WRITE-	I	IOW- is asserted when the DMA controller or Host writes a data, status, or control byte to the WD1003-WA2.
B14	IOR-	I/O READ-	I	IOR- is asserted when the DMA controller or Host reads data from the WD1003-WA2.
B15 thru B21	NC	NOT CONNECTED		
B22	IRQ6	INTERRUPT REQUEST 6	O	IRQ6 is asserted to interrupt the Host upon completion of a command. Applies to floppy controller only.
B23, B24				
B25	NC	NOT CONNECTED		
B26	DACK2-	DMA-ACKNOWLEDGE-CHANNEL 2-	O	DACK2- is asserted in response to DMA request channel 2.
B27	T/C	TERMINAL COUNT	I	Indicates sending of the last byte in a floppy disk transfer.
B28	ALE	ADDRESS LATCH ENABLE	1	Indicates board address is available.
B29	+5V	+5V		
B30	NC	NOT CONNECTED		

TABLE 3-2 HOST INTERFACE CONNECTOR (P2) PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
C1 thru C10	NC			
C11 thru C18	SD8 thru SD15	DATA BIT 8 thru DATA BIT 15	I/O	Bi directional, upper 8-bit data bus for data transfers only between the controller and the Host.
D1	NC	NOT CONNECTED		
D2	I/O CS-16-	I/O 16-BIT-CHIP-SELECT-	I	I/O CS 16 signals the system board that the current data transfer is a 1 wait-state, 16-bit I/O cycle, derived from an address decode.
D3 thru D6	NC	NOT CONNECTED		
D7	IRQ14	INTERRUPT REQUEST 14		IRQ14 signals the Host that the Winchester controller needs attention. IRQ is generated when the IRQ line goes from low to high.
D8 thru D15, D17	NC	NOT CONNECTED		
D16	+5VDC	+5VDC		+5VDC
D18	GND	GROUND		

3.3 DRIVE INTERFACE

3.3.1 WINCHESTER DRIVE CONTROL

Control signals are common to all drives and are daisy-chained to the drives from a single connector, J5. To terminate the control signals on the WD1003-WA2 properly, the last drive on the daisy chain must have a 220/330 ohm resistor pack installed. Table 3-3 describes J5 pin assignments in detail.

TABLE 3-3 WINCHESTER DRIVE CONTROL CONNECTOR (J5) PIN DESCRIPTION

SIGNAL				I/O	FUNCTION
GND	PIN	MNEMONIC	NAME		
1	2	HS3-/RWC-	HEAD-SELECT3-/REDUCE-WRITE-CURRENT-	O	The WD1003-WA2 uses HS3- to select one of 16 R/W heads. RWC- is not used by drives with 16 head drives. RWC- is used by drives with 8 R/W heads. RWC- reduces the write current on the inner cylinders. This lessens the bit shift caused by greater bit density on these cylinders.
3	4	HS2-	HEAD-SELECT2-	O	HS2- is one of the head select signals decoded by the drive to select one of eight (or 16) R/W heads.
5	6	WG-	WRITE-GATE-	O	WG- is asserted when valid data is to be written on disk. The WD1003-WA2 de-asserts WG- when WF- is detected. Special circuitry is included to ensure the system output is free of glitches during power-on.
7	8	SC-	SEEK-COMPLETE-	I	SC- informs the WD1003-WA2 that the head of a selected drive has reached the desired cylinder and has stabilized
9	10	TK000-	TRACK000-		TK000- is asserted when the R/W heads are positioned over the outermost cylinder.
11	12	WF-	WRITE-FAULT-		WF- is asserted by the selected drive when a write error occurs While this signal is being asserted, the command in progress aborts and no other disk command can be executed.

TABLE 3-3 WINCHESTER DRIVE CONTROL CONNECTOR (J5) PIN DESCRIPTION (CONT'D.)

SIGNAL				I/O	FUNCTION
GND	PIN	MNEMONIC	NAME		
13	14	HS0-	HEAD-SELECT0-	O	HS0- is one of the head select signals decoded by the drive to select one of eight (or 16) R/W heads.
15*					
	16	NC	NOT CONNECTED		
17	18	HS1-	HEAD-SELECT1-	O	HS1- is one of the head select signals decoded by the drive to select one of eight (or 16) R/W heads.
19	20	INDEX-	INDEX-PULSE-	I	INDEX- indicates the start of a track. Used as a synchronization point during formatting and as a time-out mechanism for retries. Pulses once each disk revolution.
21	22	DRDY-	DRIVE READY-	I	DRDY- informs the controller that the drive motor is up to speed.
23	24	STEP-	STEP PULSE-	O	STEP-, with DIRIN-, positions the heads to the desired cylinder. STEP- pulses once for each step. DIRIN- determines the step direction.
25	26	DS0-	DRIVE-SELECT1-	O	DS1- is used to select drive 0.
27	28	DS1-	DRIVE-SELECT2-	O	DS2- is used to select drive 1.
29, 31.		GND			
	30, 32	NC	NOT CONNECTED		
33	34	DIRIN-	DIRECTION IN-	O	DIRIN- determines the direction in which the R/W heads move when the step line is pulsed. De-asserted=out; asserted=in.

*Pin 15 is reserved to polarize the connector.

3.4 Winchester Drive Data Connectors

The data lines between the WD1003-WA2 and the two Winchester disk drives are connected to J4 and J3. As the data lines are not identical, J4 must be connected to the cable from Winchester drive 1 and J3, to the cable from Winchester drive 2. Each drive is radially connected with a maximum cable length of 3 meters (10 feet). Each data connector is a 20-pin vertical header on 0.25 mm (0.01 inch) center. Data connector pin descriptions and signals are listed in Table 3-4.

TABLE 3-4 WINCHESTER DRIVE DATA CONNECTORS (J3, J4) PIN DESCRIPTION

SIGNAL GND	SIGNAL PIN	I/O	SIGNAL NAME
	1		NC
2			GND
	3		NC
4			GND
	5		NC
6			GND
	7		NC
8*			
	9		NC
	10		NC
11			GND
12			GND
	13	O	+MFMD Write Data
	14	O	-MFMD Write Data
15			GND
16			GND
	17	I	+MFMRD Read Data
	18	I	-MFMRD Read Data
19			GND
20			GND

*Pin 8 is reserved to polarize the connector

3.3.3 Floppy Drive Control and Data Connector

Thirty four pins comprise this connector. All odd numbered pins are ground. Pin 5 is reserved to polarize the connector. Table 3-5 describes J1 pin assignments and functions in detail.

TABLE 3-5 FLOPPY DRIVE CONTROL AND DATA CONNECTOR (J1) PIN DESCRIPTION

SIGNAL				I/O	FUNCTION
GND	PIN	MNEMONIC	NAME		
1	2	WCCNTRL-	WRITE-CURRENT-CONTROL-	O	Inverted form of SDO for read data. Selection of 300kbs data rate asserts WCCNTRL-.
3	4	NC	NOT CONNECTED		
5					Pin 5 is reserved to polarize the connector.
	6	NC	NOT CONNECTED		
7	8	INDEX-	INDEX-	I	Assertion indicates start of a track.
9	10	MOTEN1-	MOTOR-ENABLE1-	O	MOTEN1- (MOTEN2) turns on the floppy disk drive spindle.
15	16	MOTEN2-	MOTOR-ENABLE2-	O	MOTEN1- (MOTEN2-) and the appropriate drive select signal must be asserted at the same time.
11	12	DS2-	DRIVE-SELECT2-	O	Assertion selects drive 2. MOTEN2- must be asserted at the same time as DS2-.
13	14	DS1-	DRIVE-SELECT1-	O	Assertion selects drive 1. MOTEN1- must be asserted at the same time as DS1-.
17	18	DIR-	DIRECTION-	O	Assertion moves the selected read/write head inward. De-assertion moves the selected read/write head outward.
19	20	STEP-	STEP-PULSE-	O	Assertion moves the read/write head one track at a time. The head moves in direction determined by the DIR- signal).
21	22	WRT DATA-	WRITE-DATA-	O	MFM data.
23	24	WRT EN-	WRITE-ENABLE-	O	Assertion enables the writing of data on an unprotected diskette.

TABLE 3-5 FLOPPY DRIVE CONTROL AND DATA CONNECTOR (J1) PIN DESCRIPTION (CONT'D.)

SIGNAL				I/O	FUNCTION
GND	PIN	MNEMONIC	NAME		
25	26	TRK0-	TRACK0-	I	Assertion indicates that the read/write head is over the outermost track.
27	28	WRT PROT-	WRITE-PROTECT-	I	Assertion indicates a write protected diskette.
29	30	READ-DATA-	READ-DATA-	I	MFM Read Data.
31	32	HS1-	HEAD-	O	Assertion selects head 1.
33	34	DISKETTE-CHG-	DISKETTE-CHANGE-	I	Assertion indicates drive is not ready i.e., drive door open, no diskette in drive, or improper assertion of motor enable or drive select signals.

3.6 WINCHESTER LED CONNTECTOR

The front panel LED connector is a 4 pin header that connects via reversible cable to the Winchester front panel. The WD1003-WA2 lights the LED when the Winchester drive is busy or the Host asserts RESET. Table 3-6 describes J6 pin assignments and functions.

TABLE 3-6 WINCHESTER LED CONNECTOR (J6) PIN DESCRIPTION

SIGNAL PIN	SIGNAL NAME	DESCRIPTION
1,4	LED+	Connects to LED anode. Tied to +5V with a 240 ohm pull up resistor.
2,3	LED-	Connects to LED cathode. Assertion of LED- lights the LED.

SECTION IV
INTERFACE TIMING

SECTION V
COMMANDS DESCRIPTION

5.1 GENERAL

The WD1003-WA2 supports two command sets: the Winchester command set and the NEC uPD765A Floppy command set. Section 5.2 describes each Winchester command in detail. Section 5.3 describes each Floppy command in detail. Section 6, Theory of Operation, describes Winchester and Floppy command execution as well as the WD1003-WA2 register structure.

5.2 WINCHESTER COMMAND SET

The WD1003-WA2 Winchester command set contains eight commands. Five commands (Restore, Seek, Read Sector, Write Sector, and Format Track) are executed through the WD2010A-05 command register. (A sixth WD2010A-05 command, Scan ID is not directly available to the Host. Scan ID may be executed by the WD1015-37 transparently to the Host.) The three remaining commands (Read Verify, Diagnose, and Set Parameters) are executed through the WD1015-37. Table 5-1 describes the eight WD1003-WA2 Winchester commands and their bit assignments.

TABLE 5-1. WINCHESTER COMMANDS AND COMMAND CODES

COMMAND	BITS							
Restore	0	0	0	1	R3	R2	R1	R0
Seek	0	1	1	1	R3	R2	R1	R0
Read Sector	0	0	1	0	0	0	L	T
Write Sector	0	0	1	1	0	0	L	T
Format Track	0	1	0	1	0	0	0	0
Read Verify	0	1	0	0	0	0	0	T
Diagnose	1	0	0	1	0	0	0	0
Set Parameters	1	0	0	1	0	0	0	1

LEGEND

R3 through R0	Step rate selection bits. Refer to Table 5-2 for more detailed information.
L	Read or Write Long bit. Set to 1 enables Read or Write Long mode.
T	Retry bit. Set to 1 disables retries.

The stepping rates for the commands that perform implied seeks are set in the least significant nibble of the last executed RESTORE or SEEK command. Table 5-2 lists the Winchester step rates.

TABLE 5-2. STEPPING RATES

R3	R2	R1	R0	STEPPING RATE	R3	R2	R1	R0	STEPPING RATE
0	0	0	0	35 usec	1	0	0	0	4.0 msec
0	0	0	1	0.5 msec	1	0	0	1	4.5 msec
0	0	1	0	1.0 msec	1	0	1	0	5.0 msec
0	0	1	1	1.5 msec	1	0	1	1	5.5 msec
0	1	0	0	2.0 msec	1	1	0	0	6.0 msec
0	1	0	1	2.5 msec	1	1	0	1	6.5 msec
0	1	1	0	3.0 msec	1	1	1	0	3.2 usec
0	1	1	1	3.5 msec	1	1	1	1	16 usec

Note: After Diagnose or reset, stepping rate defaults to 6.5 msec

5.2.1 RESTORE

The Restore command is used to move the R/W heads to the Track 000 position. The controller issues step pulses to the drive until the Track 000 indicator from the drive is asserted. If Track 000 is not asserted within 2047 steps, the Error bit in the Status Register is set and and a Track 000 error is posted in the Error Register. The implied seek step rate may be set up according to Table 5-2 by the Restore command. The restore step rate is established by the SEEK COMPLETE- signal from the drive, i.e. each step pulse is issued only after SEEK COMPLETE- is asserted by the drive from the previous step. If the DRIVE READY- signal is de-asserted or WRITE FAULT- is asserted, this command terminates with the error bit set in the status register and the error register reports an aborted command.

5.2.2 SEEK

This command moves the R/W heads to the cylinder specified in the task file cylinder high and low registers. The implied seek step rate is also set by this command. The lower order four bits of the command are used to select one of 16 available step rates. An interrupt is generated at the completion of the command. If the DRIVE READY- signal is de-asserted or WRITE FAULT- is asserted, this command is terminated with the error bit set in the status register and the error register reports an aborted command.

5.2.3 READ SECTOR

A number of sectors (1 - 256) can be read from the selected drive with this command. The sector count register in the task file determines the number of sectors to be transferred. Multiple sector reads may cross head and cylinder boundaries.

If the Read command is issued prior to initializing a step rate, the default value of 6.5 msec is selected and a Recalibrate is performed prior to the Read.

If the R/W heads are not positioned over the target track, the controller performs an implied seek to the proper cylinder. The stepping rate used during the implied seek is the value specified during the previous Seek or Restore command.

The optional long bit (L set to 1 enables Read Long.) informs the WD1003-WA2 whether or not to include the four ECC bytes. These four ECC bytes are transferred as individual bytes, not words, as is the data field information. The data request bit in the status register must be valid before each byte transferred and at least 2 usec will pass between each byte transferred.

Data errors up to 5 bits in length will be automatically corrected on normal Read commands. If an uncorrectable error occurs, the data transfer will still take place, a multi-sector read, however, will terminate after the sector in error is read by the system.

The optional retry bit (T set to 1 disables retries.) disables or enables retries. The WD2010A-05 automatically retries for ten disk revolutions when the retry bit is enabled. The WD2010A-05 properly sets the error and status registers if the retries are unsuccessful. Disabling retries allows only two disk revolutions for automatic retries before the WD2010A-05 sets the error and status registers.

For ECC errors, eight Read retries are made at reading before a soft uncorrectable error is reported. A Read retry results in the reissuing of the WD2010A-05 Read Sector command. The WD2010A-05 Read Sector command attempts to verify the sector for ten disk revolutions, if T is set to 1, before returning an error. ECC correctable data errors are corrected after two consecutive matching ECC syndromes are detected. If the error is an uncorrectable error or an error is reported by the WD2010A-05, the command terminates.

Interrupts occur as each sector is ready to be read by the system. No interrupt is generated at the end of the command. If the DRIVE READY- signal is de-asserted or WRITE FAULT- asserted, this command terminates with the error bit set in the status register and the error register reports an aborted command.

5.2.4 WRITE SECTOR

A number of sectors (1 - 256) can be written to the selected drive. The sector count register in the task file determines the number of sectors to be transferred. Multiple sector writes may cross head and cylinder boundaries.

If the Write command is issued prior to initializing a step rate, the default value of 6.5 msec is selected and a Recalibrate is performed prior to the Write.

If the heads are not positioned at the cylinder specified in the cylinder high and low registers, the controller performs an implied seek. The step rate used is determined by the step rate field of the most recently executed Restore or Seek command.

The optional long bit (L set to 1 enables Write Long.) informs the WD1003-WA2 whether or not to append the Host supplied ECC bytes. These four bytes are transferred as individual bytes, not words, as is data field information. The data request bit in the status register must be valid before each byte transferred and at least 2 usec will pass between each byte transferred.

The optional retry bit (T set to 1 disables retries.) disables or enables retries. The WD2010A-05 automatically retries for ten disk revolutions when the retry bit is enabled. The WD2010A-05 properly sets the error and status registers if the retries are unsuccessful. Disabling retries allows only two disk revolutions before the WD2010A-05 sets the error and status registers.

The WD1003-WA2 interrupt is generated as the data for each sector is required to be transferred into the Sector Buffer (except the first sector) and at the end of the command. The first sector may be written to the buffer immediately after the command has been sent, and the data request status is set. If the DRIVE READY- signal is de-asserted or WRITE FAULT- is asserted, this command terminates with the error bit set in the status register and the error register reports an aborted command.

5.2.5 FORMAT TRACK

The track specified by the task file is formatted with ID and data fields according to the interleave table transferred to the buffer. The interleave table, consists of two bytes per sector as follows:

```
     00   PHYSICAL SECTOR 1
     00   PHYSICAL SECTOR 2
     00   PHYSICAL SECTOR 3
               .
               .
               .
     00   PHYSICAL SECTOR 17
```

The data transfer must be 512 bytes even though the table may be only 34 bytes. The sector count register must be loaded with the number of sectors per track before each Format Track command. The Format Track command supports no error reporting. A bad block may be specified by replacing a 00 table entry with an 80 hex. When switching between drives, a Restore command must be executed prior to attempting a format. Command completion will leave all data fields initialized to zeroes. The completion interrupt is generated after each track has been formatted.

5.2.6 READ VERIFY

This command functions similarly to a normal Read command except that data is not output to the Host. One to 256 sectors may be verified at one time. The generated ECC bytes are compared with the recorded ECC bytes for data verification. A single interrupt is generated upon completion of the command or in the event of an error.

If the Read Verify command is issued prior to initializing a step rate, the default value of 6.5 msec is selected and a recalibrate is performed prior to the Read Verify.

For ECC errors, eight Read retries are made at reading before a soft uncorrectable error is reported. A Read retry results in the reissuing of the WD2010A-05 Read Sector command. The WD2010A-05 Read Sector command attempts to verify the sector each disk revolution for ten disk revolutions, if T is set to 1, before returning an error. ECC correctable data errors are corrected after two consecutive matching ECC syndromes are detected. If the error is an uncorrectable error or an error is reported by the WD2010A-05, the command terminates. The WRITE FAULT- and DRIVE READY- inputs are checked throughout the command's execution.

5.2.7 DIAGNOSE

The Diagnose command causes the Controller to perform an on-board diagnostic and to report the result in the Error Register. An interrupt is performed upon completion of the command.

The Diagnose command performs tests on the WD1015-37's internal ROM and RAM, the WD11C00A-22, WD2010A-05, and the Sector Buffer. If any component fails, the appropriate error code is loaded into the error register. Error codes are as follows:

01	No errors
02	WD2010A-05 register access error
03	Sector Buffer RAM data error
04	WD1015-37 to WD11C00A-22 data path error
05	WD1015-37 ROM checksum or RAM data error
00, 06-FF	Not used. Undefined.

In addition, the Diagnose command sets the write pre-comp task file register to 32. This causes write pre-compensation to begin at cylinder 128 since the write pre-comp register holds the desired value divided by four. The sector count register is reset to one while the cylinder high, cylinder low, and SDH registers are all set to zero.

5.2.8 SET PARAMETERS

This command sets up the drive parameters regarding the maximum number of heads and sectors per track. The WD1003-WA2 uses these two parameters when performing multiple sector operations. The SDH task file register specifies the drive affected. The sector count and SDH registers must be set up before this command is issued. An interrupt is set at the completion of the command.

This command must be issued before any multiple sector operations are undertaken. By setting the SDH register for each of the two possible drives, this command allows the WD1003-WA2 to support two drives with different characteristics.

5.3 FLOPPY COMMANDS

The WD1003-WA2 supports all NEC uPD765A commands. Table 5-3 lists the NEC uPD765A commands and command codes. This section fully describes the NEC floppy disk controller commands. Section 6 describes command floppy protocols and command sequence.

TABLE 5-3. COMMAND CODE SUMMARY

COMMAND	COMMAND CODES							
	SDB7	SDB6	SDB5	SDB4	SDB3	SDB2	SDB1	SDB0
READ DATA*	MT	MF	SK	0	0	1	1	0
READ DELETED DATA*	MT	MF	SK	0	1	1	0	0
WRITE DATA*	MT	MF	0	0	0	1	0	1
WRITE DELETED DATA*	MT	MF	0	0	1	0	0	1
READ TRACK*	0	MF	SK	0	0	0	1	0
READ ID*	0	MF	0	0	1	0	1	0
FORMAT TRACK*	0	MF	0	0	1	1	0	1
SCAN EQUAL*	MT	MF	SK	1	0	0	0	1
SCAN LOW OR EQUAL*	MT	MF	SK	1	1	0	0	1
SCAN HIGH OR EQUAL*	MT	MF	SK	1	1	1	0	1
SENSE DRIVE STATUS*	0	0	0	0	0	1	0	0

TABLE 5-2. COMMAND CODE DESCRIPTION (CONT'D.)

COMMAND	COMMAND CODES							
	SDB7	SDB6	SDB5	SDB4	SDB3	SDB2	SDB1	SDB0
SEEK*	0	0	0	0	1	1	1	1
RECALIBRATE**	0	0	0	0	0	1	1	1
SENSE INTERRUPT STATUS	0	0	0	0	1	0	0	0
SPECIFY	0	0	0	0	0	0	1	1
			SRT			HUT		
				HLT				ND
INVALID	Invalid command codes: No operation - floppy controller enters standby state.							

*Second byte of command code for these commands is as follows:

SDB7 through SDB3: Set to zero. SDB2: HD. SDB1: 0. SDB0: 0

**Second byte of command code for Recalibrate is as follows:

SDB7 through SDB0: Set to zero.

LEGEND

MT	Multi-track	Set to one for multi-track operation. If set to one after execution of Read/Write operation on side 0, floppy controller automatically seaches for sector 1, side 1.
MF	FM/MFM mode	Set to zero for FM. Set to one for MFM.
SK	Skip	Set to one to skip deleted data address mark.
HD	Head	Set to one for head 1. Set to zero for head 0.
SRT	Step Rate Time	1 to 16 msec in 1 msec increments (0hex = 16 msec, 1hex = 15 msec ... Ehex = 2 msec, Fhex = 1 msec. Step rates apply to both drives.
HUT	Head Unload Time	16 to 240 msec in 16 msec increments.
HLT	Head Load Time	2 to 254 msec in 2 msec increments.
ND	Non-DMA Mode	Set to one for non-DMA mode.

NOTE

Each Floppy command description contains information from the NEC uPD765A data sheet. Reprinted with permission of and licensed by NEC Electronics Inc.

5.3.1 READ DATA

Phase	R/W	uPD765A Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MF	SK	0	0	1	1	0	Command codes.
	W	X	X	X	X	X	HD	US1	US0	X = don't care.
										Usually set to zero.
										US1 and US0 set to zero.
										Unit selection performed
										by Floppy Input Register.
	W	<---------- C ---------->								Sector ID information
	W	<---------- H ---------->								prior to command exe-
		<---------- R ---------->								cution. The four bytes
	W	<---------- N ---------->								are commanded against
	W	<----------EOT---------->								header on floppy disk.
	W	<----------GPL---------->								
	W	<----------DTL---------->								
Execution										Data transfer between
										floppy drive and Host.
Result	R	<----------ST0---------->								Status information
	R	<----------ST1---------->								after command execution.
	R	<----------ST2---------->								
	R	<---------- C ---------->								Sector ID information
	R	<---------- H ---------->								after command execution.
	R	<---------- R ---------->								
	R	<---------- N ---------->								

C (Cylinder number) designates the current (selected) cylinder (track) numbers 0 through 76 of the medium.

H (Head address) is the head number, 0 or 1, as specified in the ID field.

R (Record) indicates the sector number which will be read or written.

N (Number) represents the number of data bytes written in a sector.

EOT (End of Track) denotes the final sector number on a cylinder. During Read or Write operations, the uPD765A will stop data transfer after a sector number equal to EOT.

GPL (Gap Length) contains the length of gap 3. During Read/Write commands, this value determines the number of bytes that VCO SYNC will stay de-asserted after two CRC bytes. During the Format, GPL determines Gap 3's size.

DTL (Data Length) When N is defined as 00, DTL represents the data length which the Host is going to read out or write into the sector.

ST0 through ST3 (Status 0 through Status 3) describes the four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by de-assertion of SA0B). ST0 through ST3 may be read only after a command has been executed and contains information relevant to that particular command.

A set of nine bytes (illustrated above) are required to place the uPD765A into the Read Data mode. After the Read Data command has been issued the uPD765A loads the head (if the head is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number (R) stored in the ID register (IDR) compares with the sector number read off the diskette, then the uPD765A outputs data (from the data field) byte-to-byte to the Host via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a multi-sector read operation. The Read Data command may be terminated by assertion of the TERMINAL COUNT (T/C) signal. T/C should be issued at the same time that DACK2- for the last byte of data is sent. Upon receipt of this signal, the uPD765A stops outputting data to the Host, but continues to read data from the current sector, check CRC bytes, and then at the end of the sector terminate the Read Data command. The amount of data which can be handled with a single command to the uPD765A depends upon MT (multitrack), MF (MFM/FM), and N (number of bytes/sector, set by the Host BIOS).

The multitrack function (MT) allows the uPD765A to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at sector 1, side 0 and completing at sector L, side 1 (sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

Since N is non-zero (set to 02 on WD1003-WA2), DTL has no meaning and is set to FF hex.

At the completion of the Read Data command, the head is not unloaded until after the Head Unload time interval (specified in the Specify Command) has elapsed. If the Host issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the uPD765A detects the index hole twice without finding the right sector, indicated with R, then the uPD765A sets the ND (No Data) flag in ST1 to one, and terminates the Read Data command. (Status Register 0 also has bits seven and six set to 0 and 1 respectively.)

After reading the ID and data fields in each sector, the uPD765A checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the uPD765A asserts (sets to 1) the data error flag in Status Register 1, and if a CRC error occurs in the data field the uPD765A also asserts the data error in data field flag in Status Register 2, and terminates the Read Data command. (Status Register 0 also has bits seven and six set to 0 and 1 respectively.)

If the uPD765A reads a deleted address mark off the diskette, and the SK bit (bit D5 in the first command word) is de-asserted, then the uPD765A asserts the CM (Control Mark) flag in Status Register 2, and terminates the Read Data command, after reading all the data in the sector. If SK is asserted, the uPD765A skips the sector with the deleted address mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK is asserted.

During disk data transfers between the uPD765A and Host, via the System Data Bus, the uPD765A must be serviced by the Host every 27 usec in the FM mode, and every 13 usec in the MFM mode, or the uPD765A asserts the OR (Overrun) flag in Status Register 1, and terminates the Read Data command.

If the Host terminates a read (or write) operation in the uPD765A, then the ID information in the Result phase is dependent upon the state of the MT bit and EOT byte.

5.3.2 READ DELETED DATA

Phase	R/W	uPD765A Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MF	SK	0	1	1	0	0	Command codes.
	W	X	X	X	X	X	HD	US1	US0	X = don't care.
										Usually set to zero.
										US1 and US0 set to zero.
										Unit selection performed
										by Floppy Input Register.
	W	<---------- C ---------->								Sector ID information
	W	<---------- H ---------->								prior to command exe-
	W	<---------- R ---------->								cution. The four bytes
	W	<---------- N ---------->								are commanded against
	W	<----------EOT---------->								header on floppy disk.
	W	<----------GPL---------->								
	W	<----------DTL---------->								
Execution										Data transfer between
										floppy drive and Host.
Result	R	<----------ST0---------->								Status information
	R	<----------ST1---------->								after command execution.
	R	<----------ST2---------->								
	R	<---------- C ---------->								Sector ID information
	R	<---------- H ---------->								after command execution.
	R	<---------- R ---------->								
	R	<---------- N ---------->								

C (Cylinder number) designates the current (selected) cylinder (track) numbers 0 through 76 of the medium.
H (Head address) is the head number, 0 or 1, as specified in the ID field.
R (Record) indicates the sector number which will be read or written.
N (Number) represents the number of data bytes written in a sector.
EOT (End of Track) denotes the final sector number on a cylinder. During Read or Write operations, the uPD765A will stop data transfer after a sector number equal to EOT.
GPL (Gap Length) contains the length of gap 3. During Read/Write commands, this value determines the number of bytes that VCO SYNC will stay de-asserted after two CRC bytes. During the Format, GPL determines Gap 3's size.
DTL (Data Length) When N is defined as 00, DTL represents the data length which the Host is going to read out or write into the sector.
ST0 through ST3 (Status 0 through Status 3) describes the four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by de-assertion of SA0B). ST0 through ST3 may be read only after a command has been executed and contains information relevant to that particular command.

The Read Deleted Data command is identical to Read Data command except that when the uPD765A detects a data address mark at the beginning of a data field (SK de-asserted), the uPD765A reads all the data in the sector and asserts the CM flag in Status Register 2, and terminates the command. If SK is asserted, then the uPD765A skips the sector with the data address mark and reads the next sector.

5.3.3 WRITE DATA

Phase	R/W	uPD765A Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MF	0	0	0	1	0	1	Command codes.
	W	X	X	X	X	X	HD	US1	US0	X = don't care.
										Usually set to zero.
										US1 and US0 set to zero.
										Unit selection performed
										by Floppy Input Register.
	W	<---------- C ---------->								Sector ID information
	W	<---------- H ---------->								prior to command exe-
	W	<---------- R ---------->								cution. The four bytes
	W	<---------- N ---------->								are commanded against
	W	<---------- EOT ---------->								header on floppy disk.
	W	<---------- GPL ---------->								
	W	<---------- DTL ---------->								
Execution										Data transfer between
										Host and floppy drive.
Result	R	<---------- ST0 ---------->								Status information
	R	<---------- ST1 ---------->								after command execution.
	R	<---------- ST2 ---------->								
	R	<---------- C ---------->								Sector ID information
	R	<---------- H ---------->								after command execution.
	R	<---------- R ---------->								
	R	<---------- N ---------->								

C (Cylinder number) designates the current (selected) cylinder (track) numbers 0 through 76 of the medium.

H (Head address) is the head number, 0 or 1, as specified in the ID field.

R (Record) indicates the sector number which will be read or written.

N (Number) represents the number of data bytes written in a sector.

EOT (End of Track) denotes the final sector number on a cylinder. During Read or Write operations, the uPD765A will stop data transfer after a sector number equal to EOT.

GPL (Gap Length) contains the length of gap 3. During Read/Write commands, this value determines the number of bytes that VCO SYNC will stay de-asserted after two CRC bytes. During the Format, GPL determines Gap 3's size.

DTL (Data Length) When N is defined as 00, DTL represents the data length which the Host is going to read out or write into the sector.

ST0 through ST3 (Status 0 through Status 3) describes the four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by de-assertion of SA0B). ST0 through ST3 may be read only after a command has been executed and contains information relevant to that particular command.

A set of nine bytes is required to set the uPD765A into the Write Data mode. After the Write Data command has been issued, the uPD765A loads the head (if the head is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the uPD765A takes data from the Host byte-by-byte via the data bus and outputs the data to the uPD765A.

After writing data into the current sector, the sector number in R is incremented by one, and the next data field is written into. The uPD765A continues this multisector write operation until the assertion of T/C. If the T/C signal is asserted, the uPD765A continues writing into the current sector to complete the data field. If the T/C signal is asserted while a data field is being written, then the remainder of the data field is filled with zeroes.

The uPD765A reads the ID field of each sector and checks the CRC bytes. If the uPD765A detects a read error (CRC error) in one of the ID fields, the controller asserts the data error flag of Status Register 1 and terminates the Write Data command. (Status Register 0 also has bits seven and six set to 0 and 1 respectively.)

The Write command operates in much the same manner as the Read command. The following items are the same. Refer to the Read Data command (Section 5.3.1) for details.

Transfer capacity
End of cylinder flag
No data flag
Head uload time interval
ID information when the Host terminates command
DTL

In the Write Data mode, data transfers between the Host and uPD765A, via the System Data Bus, must occur every 27 usec in the FM mode and every 13 usec in the MFM mode. If the time interval between data transfers is longer than this, then the uPD765A asserts the overrun flag in Status Register 1 and terminates the Write Data command. (Status Register 0 also has bits seven and six set to 0 and 1 respectively.)

5.3.4 WRITE DELETED DATA

Phase	R/W	uPD765A Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MF	0	0	1	0	0	1	Command codes.
	W	X	X	X	X	X	HD	US1	US0	X = don't care.
										Usually set to zero.
										US1 and US0 set to zero.
										Unit selection performed
										by Floppy Input Register.
	W	<---------- C ---------->								Sector ID information
	W	<---------- H ---------->								prior to command exe-
	W	<---------- R ---------->								cution. The four bytes
	W	<---------- N ---------->								are commanded against
	W	<---------- EOT --------->								header on floppy disk.
	W	<---------- GPL --------->								
	W	<---------- DTL --------->								
Execution										Data transfer between
										floppy drive and Host.
Result	R	<---------- ST0 --------->								Status information
	R	<---------- ST1 --------->								after command execution.
	R	<---------- ST2 --------->								
	R	<---------- C ---------->								Sector ID information
	R	<---------- H ---------->								after command execution.
	R	<---------- R ---------->								
	R	<---------- N ---------->								

C (Cylinder number) designates the current (selected) cylinder (track) numbers 0 through 76 of the medium.

H (Head address) is the head number, 0 or 1, as specified in the ID field.

R (Record) indicates the sector number which will be read or written.

N (Number) represents the number of data bytes written in a sector.

EOT (End of Track) denotes the final sector number on a cylinder. During Read or Write operations, the uPD765A will stop data transfer after a sector number equal to EOT.

GPL (Gap Length) contains the length of gap 3. During Read/Write commands, this value determines the number of bytes that VCO SYNC will stay de-asserted after two CRC bytes. During the Format, GPL determines Gap 3's size.

DTL (Data Length) When N is defined as 00, DTL represents the data length which the Host is going to read out or write into the sector.

ST0 through ST3 (Status 0 through Status 3) describes the four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by de-assertion of SA0B). ST0 through ST3 may be read only after a command has been executed and contains information relevant to that particular command.

Write Deleted Data is identical to the Write Data command except a deleted data address mark is written at the beginning of the data field instead of the normal data address mark.

5.3.5 READ TRACK

Phase	R/W	uPD765A Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	MF	SK	0	0	0	1	0	Command codes.
	W	X	X	X	X	X	HD	US1	US0	X = don't care.
										Usually set to zero.
										US1 and US0 set to zero.
										Unit selection performed
										by Floppy Input Register.
	W	<---------- C ---------->								Sector ID information
	W	<---------- H ---------->								prior to command exe-
	W	<---------- R ---------->								cution. The four bytes
	W	<---------- N ---------->								are commanded against
	W	<----------EOT---------->								header on floppy disk.
	W	<----------GPL---------->								
	W	<----------DTL---------->								
Execution										Data transfer between
										floppy drive and Host.
										Floppy drive reads all
										data fields from index
										hole to EOT.
Result	R	<----------ST0---------->								Status information
	R	<----------ST1---------->								after command execution.
	R	<----------ST2---------->								
	R	<---------- C ---------->								Sector ID information
	R	<---------- H ---------->								after command execution.
	R	<---------- R ---------->								
	R	<---------- N ---------->								

C (Cylinder number) designates the current (selected) cylinder (track) numbers 0 through 76 of the medium.

H (Head address) is the head number, 0 or 1, as specified in the ID field.

R (Record) indicates the sector number which will be read or written.

N (Number) represents the number of data bytes written in a sector.

EOT (End of Track) denotes the final sector number on a cylinder. During Read or Write operations, the uPD765A will stop data transfer after a sector number equal to EOT.

GPL (Gap Length) contains the length of gap 3. During Read/Write commands, this value determines the number of bytes that VCO SYNC will stay de-asserted after two CRC bytes. During the Format, GPL determines Gap 3's size.

DTL (Data Length) When N is defined as 00, DTL represents the data length which the Host is going to read out or write into the sector.

ST0 through ST3 (Status 0 through Status 3) describes the four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These register should not be confused with the Main Status Register (selected by de-assertion of SA0B). ST0 through ST3 may be read only after a command has been executed and contains information relevant to that particular command.

The Read Track command is similar to the Read Data command except that this is a continuous Read operation where the entire data field from each of the sectors is read. Immediately after sensing the index hole, the uPD765A starts reading all data fields on the track as continuous blocks of data. If the uPD765A finds an error in the ID or data CRC check bytes, the floppy controller continues to read data from the track. The uPD765A compares the ID information read from each sector with the value stored in the IDR and asserts the no data flag of Status Register 1 if there is no comparison. Multitrack or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT. If the uPD765A does not find an ID address mark on the diskette after it senses the index hole for the second time, the floppy controller asserts the missing address mark flag in Status Register 1 and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

5.3.6 READ ID

Phase	R/W	uPD765A Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	MF	0	0	1	0	1	0	Command codes.
	W	X	X	X	X	X	HD	US1	US0	X = don't care.
										Usually set to zero.
										US1 and US0 set to zero.
										US1 and US0 set to zero.
										Unit selection performed by Floppy Input Register.
Execution										The first correct ID information on the cylinder is stored in Floppy Data Register.
Result	R	<---------- ST0 ----------								Status information
	R	<---------- ST1 ----------								after command execution.
	R	<---------- ST2 ----------								
	R	<---------- C ----------								Sector ID information
	R	<---------- H ----------								read during Execution
	R	<---------- R ----------								phase from floppy disk
	R	<---------- N ----------								

C (Cylinder number) designates the current (selected) cylinder (track) numbers 0 through 76 of the medium.
H (Head address) is the head number, 0 or 1, as specified in the ID field.
R (Record) indicates the sector number which will be read or written.
N (Number) represents the number of data bytes written in a sector.
EOT (End of Track) denotes the final sector number on a cylinder. During Read or Write operations, the uPD765A will stop data transfer after a sector number equal to EOT.
GPL (Gap Length) contains the length of gap 3. During Read/Write commands, this value determines the number of bytes that VCO SYNC will stay de-asserted after two CRC bytes. During the Format, GPL determines Gap 3's size.
DTL (Data Length) When N is defined as 00, DTL represents the data length which the Host is going to read out or write into the sector.
ST0 through ST3 (Status 0 through Status 3) describes the four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by de-assertion of SA0B). ST0 through ST3 may be read only after a command has been executed and contains information relevant to that particular command.

The Read ID command is used to give the present position of the recording head. The uPD765A stores the values from the first ID field the controller is able to read. If no proper ID address mark is found on the diskette before the index hole is encountered for the second time, then the missing address mark flag in Status Register 1 is asserted, and if no data is found then the no data flag is also asserted in Status Register 1. The command is then terminated with bits seven and six in Status Register 0 set to 0 and 1 respectively. During this command, there is no data transfer between the uPD765A and the Host except during the result phase.

5.3.7 FORMAT TRACK

Phase	R/W	uPD765A Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	MF	0	0	1	1	0	1	Command codes.
	W	X	X	X	X	X	HD	US1	US0	X = don't care.
										Usually set to zero.
										US1 and US0 set to zero.
										Unit selection performed by Floppy Input Register.
	W	<---------- N ---------->								Bytes/sector
	W	<---------- SC--------->								Sectors/track
	W	<----------GPL---------->								Gap 3
	W	<---------- D ---------->								Filler byte
Execution										uPD765A formats entire track.
Result	R	<----------ST0---------->								Status information after command execution.
	R	<----------ST1---------->								
	R	<----------ST2---------->								
	R	<---------- C ---------->								In this case, ID information has no meaning.
	R	<---------- H ---------->								
	R	<---------- R ---------->								
	R	<---------- N ---------->								

C (Cylinder number) designates the current (selected) cylinder (track) numbers 0 through 76 of the medium.
H (Head address) is the head number, 0 or 1, as specified in the ID field.
R (Record) indicates the sector number which will be read or written.
N (Number) represents the number of data bytes written in a sector.
EOT (End of Track) denotes the final sector number on a cylinder. During Read or Write operations, the uPD765A will stop data transfer after a sector number equal to EOT.
GPL (Gap Length) contains the length of gap 3. During Read/Write commands, this value determines the number of bytes that VCO SYNC will stay de-asserted after two CRC bytes. During the Format, GPL determines Gap 3's size.
DTL (Data Length) When N is defined as 00, DTL represents the data length which the Host is going to read out or write into the sector.
ST0 through ST3 (Status 0 through Status 3) describes the four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by de-assertion of SA0B). ST0 through ST3 may be read only after a command has been executed and contains information relevant to that particular command.

The Format Track command allows an entire track to be formatted. After the index hole is detected, data is written on the diskette; gaps, address marks, ID fields, and data fields. The format is controlled by the values programmed into N, SC, GPL, and D (data pattern) which are supplied by the Host during the Command phase. The data field is filled with the byte of data stored in D. The ID field for each sector is supplied by the Host; that is, four data requests/sector are made by the uPD765A for C, H, R, and N. This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The Host must send new values for C, H, R, and N to the uPD765A for each sector on the track. The uPD765A issues four DMA requests per sector. The contents of the R register are incremented by one after each sector is formatted; thus, the R register contains a value of R when it is read during the Result phase. This incrementing and formatting continues for the whole track until the uPD765A detects the index hole for the second time, whereupon it terminates the command.

If a fault signal is received from the floppy drive at the end of a write operation, then the uPD765A asserts the equipment check flag of Status Register 0 and terminates the command after setting bits seven and six of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes bits seven and six of Status Register 0 to be set to 0 and 1 respectively.

5.3.8 SCAN COMMANDS

Phase	R/W	uPD765A Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MF	SK	1	0	0	0	1	Command code for Scan Equal.
	W	MT	MF	SK	1	1	0	0	1	Command code for Scan Low or Equal.
	W	MT	MF	SK	1	1	1	0	1	Command code for Scan High or Equal.
	W	X	X	X	X	X	HD	US1	US0	X = don't care. Usually set to zero. US1 and US0 set to zero. Unit selection performed by Floppy Input Register.
	W	<---------- C ---------->								Sector ID information prior to command execution. The four bytes are commanded against header on floppy disk.
	W	<---------- H ---------->								
	W	<---------- R ---------->								
	W	<---------- N ---------->								
	W	<----------EOT---------->								
	W	<----------GPL---------->								
	W	<----------DTL---------->								
Execution										Data compared between floppy drive and Host.
Result	R	<----------ST0---------->								Status information after command execution.
	R	<----------ST1---------->								
	R	<----------ST2---------->								
	R	<---------- C ---------->								Sector ID information after command execution.
	R	<---------- H ---------->								
	R	<---------- R ---------->								
	R	<---------- N ---------->								

C (Cylinder number) designates the current (selected) cylinder (track) numbers 0 through 76 of the medium.
H (Head address) is the head number, 0 or 1, as specified in the ID field.
R (Record) indicates the sector number which will be read or written.
N (Number) represents the number of data bytes written in a sector.
EOT (End of Track) denotes the final sector number on a cylinder. During Read or Write operations, the uPD765A will stop data transfer after a sector number equal to EOT.
GPL (Gap Length) contains the length of gap 3. During Read/Write commands, this value determines the number of bytes that VCO SYNC will stay de-asserted after two CRC bytes. During the Format, GPL determines Gap 3's size.
DTL (Data Length) When N is defined as 00, DTL represents the data length which the Host is going to read out or write into the sector.
ST0 through ST3 (Status 0 through Status 3) describes the four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by de-assertion of SA0B). ST0 through ST3 may be read only after a command has been executed and contains information relevant to that particular command.

The Scan Commands allow data which is being read from the floppy disk to be compared against data which is being supplied from the Host. The uPD765A compares the data on a byte-by-byte basis and searches for a sector of data that meets the conditions of DuPD765A = DHOST, DuPD765A <= DHOST, or DuPD765A >= DHOST. The hexidecimal byte of FF either from memory or from the floppy drive can be used as a mask byte because it always meets the condition of the comparison. One's complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP --> R), and the scan operation is continued. The scan operation continues

until one of the following conditions occur:

1. Conditions for scan are met (equal, low, or high).
2. Last sector on track is reached.

3. Assertion of T/C.

If the conditions for scan are met, then the uPD765A asserts the Scan Hit (SH) flag of Status Register 2 and terminates the Scan command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder, then the uPD765A asserts Scan Not Satisfied (SN) flag of Status Register 2 and terminates the Scan command. The receipt of a T/C signal from the Host or DMA controller during the scan operation will cause the uPD765A to complete the comparison of the particular byte which is in process and then to

terminate the command.

If the uPD765A encounters a Deleted Data Address mark on one of the sectors (and SK = 0), then the controller regards the sector as the last sector on the cylinder, asserts the Control Mark (CM) flag of Status Register 2 and terminates the command. If SK = 1, the uPD765A skips the sector with the Deleted Address mark and reads the next sector. In the second case (SK = 1), the uPD765A asserts the CM flag of Status Register 2 to indicate that a

deleted sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02) sectors are read or the MT is programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26 and the Scan command is started at sector 21, then sectors 21, 22, 23, and 25 will be read. Sector 26 will be skipped. The index hole will be encountered before EOT value of 26 can be read. This results in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan command would be completed in

a normal manner.

During the Scan command, data is supplied by either the Host or DMA controller for comparison against the data read from the floppy disk. To avoid having the Overrun (OR) flag set in Status Register 1, it is necessary to have the data available in less than 27 usec (FM mode) or 13 usec (MFM mode). If an Overrun occurs, the uPD765A ends the command with bits seven and six of

Status Register 0 de-asserted and asserted, respectively.

5.3.9 SEEK

Phase	R/W	uPD765A Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	1	1	1	1	Command code
	W	X	X	X	X	X	HD	US1	US0	X = don't care.
										Usually set to zero.
										US1 and US0 set to zero.
										Unit selection performed
										by Floppy Input Register.
	W	<---------- NCN ---------->								New cylinder number
Execution										Head is moves to proper
										cylinder.

The read/write head within the floppy drive is moved from cylinder to cylinder under control of the Seek command. The Host uses two of the uPD765A's four independent Present Cylinder registers. (One register for each drive supported. Note that the WD1003-WA2 supports only two floppy drives.) These registers are cleared only after the Recalibrate command. The uPD765A compares the Present Cylinder Number (PCN) which is the current head position with the New Cylinder Number (NCN), and if there is a

difference, performs the following operations:

PCN < NCN: Asserts the DIRECTION (DIR) signal (A gate inverts this signal to DIR- for the drive.), and issues STEP IN pulses to the drive.

PCN > NCN: De-asserts the DIR signal and issues STEP OUT

pulses to the drive.

The rate at which step pulses are issued is controlled by Stepping Rate Time (STR) bits in the Specify command. After each step pulse issued, NCN is compared against PCN, and when NCN = PCN, the Seek End (SE) flag is asserted in Status Register 0, and the command is terminated. At this point, the FLOPPY INTERRUPT (FINT) is asserted. The four LSBs in the Main Status Register are asserted during the Seek operation and are cleared by the

Sense Interrupt Status command.

During the command phase of the Seek operation, the uPD765A is in the Busy state, but during the execution phase the floppy controller is in the nonBusy state. While the uPD765A is in the nonBusy state, another Seek command may be issued. This allows parallel simultaneous Seek operations for both drives. No other

command can be issued while the uPD765A is stepping the drive.

If the selected floppy drive is Not Ready at the start of the command execution phase or during the Seek operation, the Not Ready (NR) flag is asserted in Status Register 0 and the command is terminated after bits seven and six of Status Register 0 are

de-asserted and asserted respectively.
If the time to write three bytes of Seek command exceeds 150 usec, the timing between the first two step pulses may be shorter than

set in the Specify command by as much as 1 msec.

5.3.10 RECALIBRATE

Phase	R/W	uPD765A Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	0	1	1	1	Command code
	W	X	X	X	X	X	0	US1	US0	X = don't care.
										Usually set to zero.
										US1 and US0 set to zero.
										Unit selection performed
										by Floppy Input Register.
Execution										Head is retracted to
										Track 0.

The function of this command is to retract the read/write head in the floppy drive to the track 0 position. The uPD765A clears the contents of the PCN counter and checks the status of the TRACK 0- signal from the floppy drive. While the drive asserts TRACK 0-, the DIR- remains asserted and steps pulses are issued. When the drive de-asserts TRACK 0-, the uPD765A asserts the SE flag in Status Register zero and the command terminates. If TRACK 0- is asserted after 77 step pulses have been issued, the uPD765A asserts the SE and Equipment Check (EC) flags of Status Register 0. The command terminates after bits seven and six are de-

asserted and asserted respectively.
Overlapping of Recalibrate commands to multiple floppy drives and the loss of the READY, as described in the Seek command, also applies to the Recalibrate command. If the diskette has more than 77 tracks, then the Recalibrate command should be issued

twice to position the read/write head to track 0.

5.3.11 SENSE INTERRUPT STATUS

Phase	R/W	uPD765A Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	1	0	0	0	Command code
Result	R	<---------- ST0 ----------								Status information
		<---------- PCN ----------								about the uPD765A at the
										end of a Seek operation.

An interrupt signal (FINT is driven to the Host as IRQ6) is generated by the uPD765A for one of the following reasons:

1. Upon entering the Result phase of any command except Sense Drive Status, Invalid, or Sense Interrupt Status commands.
2. READY signal changes state.
3. End of Seek or Recalibrate command.

Interrupts caused by reason one occurs during normal command operations and are easily discernible by the Host. Reason one does not require issuance of a Sense Interrupt Status command. The interrupt is cleared by reading/writing to the uPD765A. Interrupts caused by reasons two and three may be uniquely identified with the aid of the Sense Interrupt Status command. This command when issued resets the interrupt signal and via bits five, six, and seven of Status Register 0 identifies the cause of the interrrupt as illustrate below.

SEEK END Bit 5	INTERRUPT CODE Bit 6	Bit 7	CAUSE
0	1	1	READY changed state.
1	0	0	Normal termination of Seek or Recalibrate command.
1	1	0	Abnormal termination of Seek or Recalibrate command.

The Sense Interrupt Status command is used with the Seek and Recalibrate commands which have no result phase. When the floppy drive has reached the desired head position, the uPD765A asserts FINT. The Host must then issue a Sense Interrupt Status command to determine the actual cause of the interrupt which could be Seek End or a change in ready status from one of the drives.

5.3.12 SPECIFY

Phase	R/W	uPD765A Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	0	0	1	1	Command code
Result	W	<---- SRT ---->				<---- HUT ---->				Step Rate Time (SRT). One to sixteen msec in one msec intervals. F16 = 1 msec, E16 = 2 msec, etc. Head Unload Time (HUT). Head unload time after occurence of a Read or Write operation (16 to 240 msec in 16 msec intervals).
	W	<---------- HLT ---------->							ND	Head Load Time (HLT). Two to 254 msec in 2 msec increments. Not used since the HEAD LOAD signal pin on the WD1003-WA2's uPD765A is not connected.
	W									Non-DMA (ND). Selects DMA or non-DMA mode. Remains de-asserted for WD1003-WA2. This bit is never asserted.

The Specify command sets the initial values for each of the three internal timers. The HUT defines the time from the end of the execution phase of one of the read/write commands to the head unload state. This timer is programmable from 16 to 240 msec in increments of 16 msec (0116 = 16 msec, 0216 = 32 msec, ... 0F16 = 240 msec.). SRT defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 msec in increments of 1 msec (F16 = 1 msec, E16 = 2 msec, etc.). HLT is not used since the HEAD LOAD signal pin is not connected.

The time intervals mentioned above are a direct function of the clock (CLK or FREP from the WD16C92). Times indicated above are for an 8MHz clock; if the clock runs at 4MHz, then all time intervals are increased by a factor of 2.

The ND bit in this command is set to zero since WD1003-WA2 operates in the DMA mode only.

5.3.13 SENSE DRIVE STATUS

Phase	R/W	uPD765A Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	0	1	0	0	Command code
	W	X	X	X	X	X	HD	US1	US0	X = don't care. Usually set to zero. US1 and US0 set to zero. Unit selection performed by Floppy Input Register.
Result	R	<---------- ST3 ---------->								Status Register 3 (not to be confused with the Main Status Register) contains status information about the floppy drive after command execution.

This command may be used by the Host to obtain the status of the floppy drive. Status Register 3 contains the drive status information stored internally in the uPD765A registers.

5.3.14 INVALID

Phase	R/W	uPD765A Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	<------ INVALID CODES -------->								Invalid command code (No Operation: uPD765A enters Standby state.)
Result	R	<---------- ST0 ---------->								Status Register 0 = 80_{16}.

If an Invalid command is sent to the floppy controller (a command not previously defined), then the uPD765A terminates the command after bits seven and six of Status Register 0 are asserted and de-asserted respectively. No interrupt is generated by the uPD765A during this condition. Bits six and seven (DIO and RQM) in the Main Status Register are both asserted, indicating to the Host that the uPD765A is in the Result phase and the contents of Status Register 0 must be read. When the Host reads Status Register 0, the Host finds an 80 hex, indicating an Invalid command was received.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate interrupt, otherwise the uPD765A will consider the next command invalid.

In some applications, the user may utilize this command as a No Op command to place the floppy controller in a standby (No Operation) state.

SECTION VI*
TASK FILES

6.1 GENERAL

This Section briefly describes the WD1003-WA2's, bus protocol, register structure, and command execution.

NOTE

Certain descriptions, e.g. the number of drives supported and floppy controller non-DMA mode, in this manual differ slightly from the NEC uPD765A documentation. Where differences exist, the values and descriptions in this manual take precedence over the NEC uPD765A documentation.

6.2 BUS PROTOCOL

6.2.1 WINCHESTER CONTROLLER

The Host directly loads all WD2010A-05 task file registers except the WD2010A-05 command register. The WD1015-37 loads the command register. Assertion of IRQ14 by the WD1003-WA2 indicates either command completion or the start of a data transfer. Completion of a data transfer occurs when the WD1003-WA2 de-asserts the BUSY flag in the status register. Therefore, the WD1003-WA2 Winchester disk controller does NOT use bus protocols or phases.

6.2.2 FLOPPY CONTROLLER

The NEC uPD765A command structure is fundamentally different from the Western Digital command structure. Each floppy command is initiated by a multibyte transfer from the Host, and the result after execution of the command may also be a multibyte transfer back to the Host. Because of this multibyte interchange of information between the uPD765A and the Host, it is convenient to consider each command as consisting of three phases:

Command Phase:	The uPD765A receives all information required to perform a particular operation from the Host.
Execution Phase:	The uPD765A performs the operation it was instructed to do.
Result Phase:	After completion of the operation, status and other housekeeping information are made available to the Host.

Most commands require nine command bytes and return seven bytes during the Result phase. No foreshortening of the Command or Result phases is allowed. Section 5 describes the required preset parameters and results for each command.

*Portions of this Section contain excerpts of the NEC uPD765A data sheet. Reprinted with permission of and licensed by NEC Electronics Inc. c 1985 NEC Electronic Inc.

6.3 REGISTER ADDRESS MAP

The WD1003-WA2 contains seven Read/Write Task File Registers in the WD2010A-05, a 16-bit Data Register, a Fixed Disk Register, Alternate Fixed Disk Status Register, a Digital Output Register, and a Digital Input Register. The WD16C92 contains a 2-bit Floppy Control Register. Main Floppy Status and Data Registers are in the NEC uPD765A. These registers are mapped into either a primary or secondary I/O address. All Winchester data, control, and status information pass between the Task Files or Data Register and the Host. The Host controls and communicates with the uPD765A directly. No on-board microprocessor controls the NEC uPD765A. Therefore, all floppy data, control, and status information pass between the floppy registers and the Host. All Winchester data transfers between the WD1003-WAH and Host are word transfers except ECC bytes in Read Longs and Write Longs. These ECC bytes are transferred in byte mode. Control and status bytes are also transferred between the Host and WD1003-WA2 in byte mode. The Task File Registers are multiplexed with IOR- and IOW- to give 14 possible ports. Five of the Task File Registers are bi-directional. Two of the Task File Registers have different definitions for read and write operation. Jumpers select the primary and secondary address. This allows two controllers in the same Host system. However, secondary ports on the WD1003-WA2 are NOT supported by any version of IBM DOS as of this publication date. Other operating systems are available that support this feature.

Table 6-1 summarizes the WD1003-WA2 I/O port address map. Figure 6-1 summarizes the WD2010A-05 Task File Registers bit assignments. Figure 6-2 summarizes the other I/O registers bit assignments for the WD1003-WA2. Bit assignments are with respect to the Host lower byte bus terms, SD7 through SD0. The fixed Size/Drive/Head (SDH) and Status Registers in the WD2010A-05 slightly differ from the standard descriptions in the WD2010-05 data sheet. Please note that the SDH Register is set for the ECC option mode and 512 bytes per sector. The SDH Register also limits the number of drives to two and the number of heads to 16. Bit 2 of the WD2010A-05 Status Register is designated as the Corrected Data bit. Assertion (setting to 1) of this bit indicates the sector read from the drive resulted in a correctable ECC error. Soft errors do not end multiple sector transfers. Bit 1 of the WD2010A-05 Status Register is designated as the Index bit. Assertion of this bit occurs each revolution of the currently selected drive. Refer to the WD2010-05 data sheet for a complete description of all other WD2010A-05 bit assignments. Table 6-2 describes the bit assignments for the other WD1003-WA2 control and status registers.

NOTE

Where differences exist, the values and descriptions for Figure 6-1 take precedence over the WD2010-05 data sheet.

The uPD765A contains two registers which may be accessed by the Host: the Main Floppy Status Register and the Floppy Data Register. The 8-bit Main Floppy Status Register contains the status information of the uPD765A, and may be accessed at any time. The 8-bit Floppy Data Register (which actually consists of several registers in a stack with only one register presented to the data bus at a time), stores data, command, parameters, and floppy drive status information. Data bytes are read out of, or written into, the Floppy Data Register in order to program or obtain the results after a particular command. Only the Main Floppy Status Register may be read and used to facilitate the transfer of data between the Host and uPD765A.

TABLE 6-1. WD1003-WA2 REGISTER ADDRESS MAP

I/O ADDRESS		READ	WRITE
PRIMARY	SECONDARY		
		DATA REGISTER	
1F0	170	DATA REGISTER (16 bits)	DATA REGISTER (16 bits)
		WD2010A-05 TASK FILE REGISTERS	
1F1	171	ERROR REGISTER	WRITE PRE-COMP
1F2	172	SECTOR COUNT	SECTOR COUNT
1F3	173	SECTOR NUMBER	SECTOR NUMBER
1F4	174	CYLINDER NUMBER (low byte)	CYLINDER NUMBER (low byte)
1F5	175	CYLINDER NUMBER (high byte)	CYLINDER NUMBER (high byte)
1F6	176	SDH REGISTER	SDH REGISTER
1F7	177	STATUS REGISTER	STATUS REGISTER
		CONTROL AND STATUS REGISTERS	
3F2	372		DIGITAL OUTPUT REGISTER
3F4	374	MAIN FLOPPY STATUS REGISTER (uPD765A)	MAIN FLOPPY STATUS REGISTER (uPD765A)
3F5	375	FLOPPY DATA REGISTER (uPD765A)	FLOPPY DATA REGISTER (uPD765A)
3F6	376	ALTERNATE FIXED DISK STATUS REGISTER	ALTERNATE FIXED DISK STATUS REGISTER
3F7	377	DIGITAL INPUT REGISTER	FLOPPY CONTROL REGISTER (WD16C92)

NOTE: All addresses in Table 6-1 are in hex. A Read or Write to I/O address 1F0 hex (170 hex) is a Read or Write for the Sector Buffer. Therefore, the hardware for the 16-bit data register is the Sector Buffer. The WD11C00A-22 also duplicates the WD2010A-05 Command and Error registers for control purposes. Error codes for the Host are actually stored in the WD11C00A-22.

REGISTER	BUS BIT POSITION							
	7	6	5	4	3	2	1	0
WRITE PRE-COMP	CYLINDER NUMBER DIVIDED BY 4							
ERROR	BB	ECC	0	ID	0	AC	TK	DM
SECTOR COUNT	NUMBER OF SECTORS							
SECTOR NUMBER	SECTOR NUMBER							
CYLINDER NO.	CYLINDER NUMBER (LOW BYTE)							
CYLINDER NO.	0	0	0	0	0	0	CYL. NO. MSB	
SDH	1	0	1	DS	HS3	HS2	HS1	HS0
COMMAND	COMMAND							
STATUS	BSY	RDY	WF	SC	DRQ	CRD	IDX	ERR

FIGURE 6-1. WD2010A-05 TASK FILE REGISTER BIT ASSIGNMENT

REGISTER	BUS BIT POSITION							
	7	6	5	4	3	2	1	0
DIGITAL OUTPUT	X	X	MOEN2	MOEN1	FDMAEN	FRST	X	FDSEL
MAIN FLOPPY STATUS (uPD765A)	RQM	DIO	EXM	CB	0	0	D1B	D0B
ALTERNATE STATUS	BSY	RDY	WFT	SKC	DRQ	CRD	IDX	ERR
FIXED DISK	0	0	0	0	HS3EN	RST	IEN-	0
DIGITAL INPUT	DCHG	WTG-	HS3-/RWC-	HS2-	HS1-	HS0-	DS2-	DS1-
FLOPPY CONTROL	TWO BIT REGISTERS IN WD16C92						SDB1	SDB0

FIGURE 6-2. WD1003-WA2 CONTROL AND STATUS REGISTERS

TABLE 6-2 WD1003-WA2 CONTROL AND STATUS REGISTER BIT DEFINITIONS

REGISTER	BIT MNEMONIC	BIT NAME
DIGITAL OUTPUT	X	Reserved.
	MOEN2	MOTOR ENABLE2 and MOTOR
	MOEN1	ENABLE1. Controls floppy drive motors. Setting this bit to 0 turns off the associated drive and drive selection can not occur.
	FDMAEN	FLOPPY DISK INTERRUPT and DMA ENABLE. Setting this bit to 1 gates floppy disk DMA and interrupt requests to the I/O interface. Setting to 0 disables the DMA and interrupt request drivers.
	FRST	Setting to 0 resets the floppy controller. Floppy reset time is 3.5 usec. Set to 1 by Host software enables the floppy controller.
	FDSEL	FLOPPY DISK SELECT. Set to 0 selects drive A. Set to 1 selects drive B. Appropriate MOTOR ENABLE bit must be set.
MAIN FLOPPY STATUS	X	Reserved.
	RQM	REQUEST FOR MASTER. Set to 1 to indicate that the floppy data register is ready for a data transfer. Used with DIO bit.
	DIO	DATA INPUT/OUTPUT. Controls data transfer direction. Set to 0 to indicate data transfer is from Host to floppy controller. Set to 1 to indicate data transfer is to Host from floppy controller.
	EXM	EXECUTION MODE. Set to 1 only during the execution phase in non-DMA mode.
	CB	Set to 1 to indicate a Read or Write command in process.

TABLE 6-2 WD1003-WA2 CONTROL AND STATUS REGISTER BIT DEFINITIONS (CONT'D.)

REGISTER	BIT MNEMONIC	BIT NAME
MAIN FLOPPY STATUS (CONT'D.)	D1B	Set to 1 when floppy drive B is in Seek mode.
	D0B	Set to 1 when floppy drive A is in Seek mode.
ALTERNATE FIXED DISK STATUS	BSY	Controller Busy Flag
	RDY	Ready from selected drive
	WFT	Write Fault from selected drive
	SKC	Seek Complete from selected drive
	DRQ	Data Transfer Request Flag
	CRD	Corrected Data Flag from WD1015-37
	IDX	Index pulse from selected drive
	ERR	Error Flag from WD1015-37
FIXED DISK	HS3EN	Set to 1: Enables HS3-. Set to 0: Enables RWC-
	RST	Reset. Program controlled reset to board. This bit maintains the WD1003-WA2 logic reset as long as this bit is on. This bit must be on for a minimum of 6.5 usec. After the bit is on for the minimum time, the bit must be turned off to complete reset function.
	IEN-	Interrupt Enable. Enables or disables IRQ14. This bit does not clear the interrupt level in the disabled state. A pending interrupt would occur when the interrupt is enabled again. A system master reset clears the interrupt but leaves the interrupt enabled.
DIGITAL INPUT	DCHG	DISKETTE CHANGE. Set to 1 if no diskette is in the drive, drive door is open, or the drive is not ready.

TABLE 6-2 WD1003-WA2 CONTROL AND STATUS REGISTER BIT DEFINITIONS (CONT'D.)

REGISTER	BIT MNEMONIC	BIT NAME
DIGITAL INPUT (CONT'D.)	WTG-	Write Gate on
	HS3- (RWC-) through HS0-	Drive head select or RWC- (bit 5) for drives using RWC-
	DS2-, DS1-	Drive select
FLOPPY CONTROL	SDB1, SDB0	The WD16C92 contains a two bit Floppy Control register. These registers control the data transfer rate between the controller and drive and the data encoding format. The Floppy Control register bit definitions are as follows: SDB1 SDB0 0 0 500 kbs MFM* 0 1 300 kbs MFM 1 0 250 kbs MFM 1 1 125 kbs FM**

*Default data rate after Reset.
**International exchange standard for 5 1/4 inch floppy diskettes.

Table 6-3 describes the WD1003-WA2 error codes for the Winchester controller.

TABLE 6-3 WD1003-WA2 ERROR REGISTER CODES (WINCHESTER CONTROLLER ONLY)

CODE	DESCRIPTION
01	No errors
02	WD2010A-05 register access error
03	Sector Buffer RAM data error
04	WD1015-37 to WD11C00A-22 register access error or WD11C00A-22 Byte 0 Pipeline register error
05	WD1015-37 ROM checksum or RAM data error
00, 06 thru FF	Not used. Undefined.

6.4 WINCHESTER COMMAND SEQUENCE DESCRIPTION

This section describes a typical Winchester command execution sequence. This description illustrates the relationship between Host and the major Winchester control components of the WD1003-WA2 during Winchester command execution.

In the idle state: the WD2010A-05 drive control signals are off. The controller status indicates ready. Drive status is valid. Controller interrupt is enabled but not asserted. The WD1015-37 is idle amd is monitoring the WAKEUP signal input.

The Host outputs the command parameters to the WD2010A-05 task file, the operation command (Seek, Read or Write) and the command attributes (Long mode, retry control, etc.). For write operations, the Host also outputs the sector or format data.

The command byte is intercepted by the WD11C00A-22 and is held for later interpretation by the WD1015-37.

A Read command output sets the module Wakeup latch that causes the controller status to indicate Busy and the WD1015-37 WAKEUP signal to be asserted. Write and Format commands first set the data request status signal DRQ. This initiates the Host data transfer. Completion of the data transfer (512 or 516 bytes) sets the WD1015-37 WAKEUP signal and Busy status.

The WD1015-37 examines the command, verifies command parameters, and passes the command to the WD2010A-05 for execution.

The WD2010A-05 executes the command providing drive positioning, data transfer control, error monitoring and completion status. The WD10C20 provides drive read and write data control for commands that require data transfers.

On command completion, the WD2010A-05 interrupts the WD1015-37. The WD1015-37 examines the command, status etc. for any additional requirements. If completion is indicated, the WD1015-37 sets the controller status to indicate ready and interrupts the Host.

The WD1003-WA2 returns to the idle state and the Host may examine drive and controller status, read input data, etc. as required to complete the operation.

6.6.5 NEC uPD765A FLOPPY DISK CONTROLLER

The uPD765A is an LSI Floppy Disk Controller chip which contains the circuitry and control functions for interfacing a Host processor to 2 floppy disk drives. There are two functional interfaces for the NEC uPD765A: the Host interface and drive interface.

During Command or Result phases the Main Status Register must be read by the Host before each byte of information is written into or read from the Floppy Data Register. After each byte of data read or written to the Floppy Data Register, the Host should wait for 12usec before reading the Main Floppy Status Register. Bits 6 and 7 in the Main Flopppy Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the uPD765A. Many of the commands require multiple bytes and, as a result, the Main Floppy Status Register must be read prior to each byte transfer to the uPD765A. On the other hand, during the Result phase, bits 6 and 7 in the Main Floppy Status Register must both be asserted (set to 1) before reading each byte from the Floppy Data Register. Note that this reading of the Main Floppy Status Register before each byte transfer to the uPD765A is required only in the Command and Result phases, and not during the Execution phase.

During the Execution phase, the Main Floppy Status Register need not be read. The uPD765A asserts DRQ2 when each byte of data is available. The Host DMA controller responds to this request by asserting DACK2- and IOR- signals. Assertion of DACK2- de-asserts the controller's DRQ2. For Write commands, the Host asserts IOW- instead of IOR-. After the Execution phase has been completed (T/C asserted) or the End of Track (EOT) sector read (or written) then the NEC u765A asserts IRQ6. This signifies the beginning of the Result phase. When the first byte of data is read during the Result phase, IRQ6 is de-asserted.

It is important to note that during the Result phase all bytes shown in Section 5 must be read. The Read Data command, for example, has seven bytes of data in the Result phase. All seven bytes must be reaad in order to successfully complete the Read Data command. The uPD765A will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result phase.

The uPD765A contains five Status Registers. The Main Floppy Status Register may be read by the Host at any time. The other four floppy controller Status Registers (ST0, ST1, ST2, and ST3) are available only during the Result phase and may be read only after completing a command. The particular command that has been executed determines how many of Status Registers will be read.

The DIO and RQM bits in the Main Floppy Status Register indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last IOR- or IOW- during a Command or Result phase and DIO and RQM getting set or reset is 12usec. For this reason every time the Main Floppy Status Register is read the Host should wait 12usec. The maximum time from the trailing edge of the last IOR- in the Result phase to when CB (floppy controller Busy - data bus bit 4) is de-asserted (set to 0) is 12usec.

The bytes of data which are sent to the uPD765A to form the Command phase and are read out of the uPD765A in the Result phase must occur in the order shown in Section 5. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result phase is allowed. After the last byte of data in the Command phase is sent to the uPD765A, the Execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result phase, the command is automatically ended and the uPD765A is ready for a new command.

The NEC uPD765A on the WD1003-WA2 is limited to basic drive control functions such as head selection and sending the STEP-, DIR-, and WRT EN- signals to the floppy drives. The NEC u765A also receives INDEX-, WR PROT-, and TRK0- for drive status. Unit selection is under direct control of the Host through the Digital Output register (external to the uPD765A). The NEC uPD765A does not directly drive write data or receive read data from the floppy drives. However, the NEC controller does produce write precompensation signals for the WD16C92.

SECTION VII
INSTALLATION

7.1 GENERAL

This Section describes the hardware and software installation of the WD1003-WA2 Winchester/Floppy Disk Controller.

7.2 HARDWARE INSTALLATION

This section briefly describes installation of the WD1003-WAH hardware. If the disk drive(s) are being installed internally, it is best to locate the controller in the closest available expansion slot relative to the drive.

CAUTION

Handle the controller board by the ends of the board. Some of the chips are static sensitive and damage may occur if the board is incorrectly handled.

NOTE

Only verify the jumper settings in Step 1. Modification of the Standard factory jumper settings on any equipment described in this document is rarely necessary.

1. Verify controller jumper settings. Refer to Table 7-1 and Figure 7-1 for jumper setting information.

TABLE 7-1. WD1003-WA2 JUMPER SETTINGS

PIN CONNECTS	DESCRIPTION
	NOTE
	DO NOT MOVE PRIMARY ADDRESS JUMPERS UNLESS THE OPERATING SYSTEM IS CONFIGURED TO ACCEPT TWO HARD DISK CONTROLLERS. CERTAIN OPERATING SYSTEMS SUPPORT TWO CONTROLLERS IN THE SAME SYSTEM. IBM DOS AND MANY IBM COMPATIBLE OPERATING SYSTEMS DO NOT SUPPORT THIS FEATURE.
E2 to E3	Standard factory setting. Selects primary addresses.
E5 to E6	Standard factory setting. Selects primary addresses.
E1 to E2	Selects secondary setting.
E4 to E5	Selects secondary setting.
E7 to E8	Standard factory setting. Supports 360 RPM floppy disk drives.
E8 to E9	Jumper in this position. Selects 300 RPM floppy disk drives.

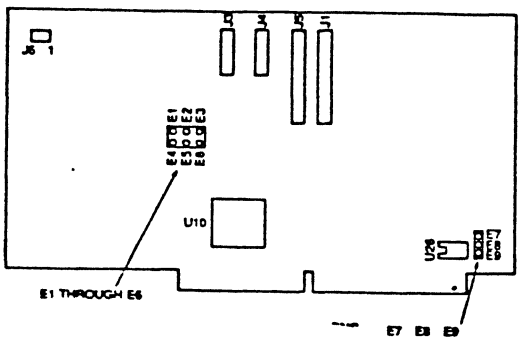

FIGURE 7-1 WD1003-WA2 JUMPER LOCATIONS

2. Verify termination on last drive. Verify proper setting of drive select switches on drive, i.e. set the drive select switches for drive select 1 or 2. Refer to your system owner's manual for information on information on proper drive termination and select switches.

3. Remove the blank expansion slot bracket. Put the bracket away and save it for possible future use. The screw will be used to hold the new controller board in place.

4. Attach 34-pin control connector pin 1 to J5 pin 1.

5. Connect control cable to drive.

6. Attach 20-pin data connector to J4.

7. Attach 20-pin data connector to J3 (drive 0 or 2).

8. Connect data cables to drives.

9. Attach 34-pin floppy cable connector to J1. Connect cable to floppy drive.

10. Attach Winchester activity LED connector to J6.

11. Install the controller board into the expansion slot. Make sure that the board is seated properly by pressing down on both ends of the board. Secure the board with the bracket screw.

12. Remove or disable any other floppy controller in your system.

7.3 SOFTWARE INSTALLATION

This section contains instructions for preparing (low level format, etc.) your operating system to recognize the Western Digital controller.

1. Insert your system Diagnostic Diskette (or equivalent).

2. Turn on the power.

3. Boot Diagnostic and select setup option.

4. Set clock etc.

CAUTION

Avoid system damage by consulting your Technical Reference manual to ensure that your drive type is supported by your Host BIOS drive tables. Not all AT-compatibles share the same drive tables as IBM.

5. Select proper Drive Type. Consult your Technical Reference Manual for further information on these parameters.

NOTE

Step 6 requires execution of low level formatting. Use of the IBM Advanced Diagnostic (or similar program for IBM-compatibles) is necessary since the WD1002-WA2 contains no on-board Basic Input/Output System (BIOS) ROM.

6. Insert your Advanced Diagnostic diskette and execute low level Format.

7. Insert System Diagnostic Diskette (or equivalent) after the system finishes the low level Format.

8. Load and execute the FDISK and FORMAT programs.

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WD1002-WA2 vs WD1003-WA2

HARDWARE DIFFERENCES

WD1002-WA2	WD1003-WA2
1. Host interface and buffer management is in discrete.	1. Uses WD11C00-22 (BMAC) or the WD11C00A-22 (RMAC) for host interface and buffer management.
2. Uses WD1010-05 Winchester controller.	2. Uses WD2010-05 Winchester controller.
3. Uses WD1014-01 for ECC.	3. Uses WD2010-05 which has on-chip ECC.
4.Floppydata separation is in discrete.	4. Uses WD16C92(FRWC) for integrated floppy data separation.
5. PCB is 4-layer design.	5. PCB is 2-layer design.

Comparison of Radiated Harmonics in IBM-AT System
of two W.D. Controllers

TABLE 1

Freq, Mhz	Production Board 1002-WA2	Final artwork 1003-WA2	Limit
40.07	49.5	-	58.1
41.45	-	48.5	57.8
47.00	-	48.9	57.2
60.07	42.5	-	55.5
63.36	49.8	-	55.9
66.08	-	44.9	56.1
72.08	-	49.1	56.4
75.11	43.8	-	56.7
81.32	49.7	49.3	57.0
84.97	49	-	57.3
86.7	50.4	47.5	57.3
110.23	-	42.0	59.3
115.6	-	43.9	58.8
120.10	-	49.3	58.4
132.1	51.5	53.8*	57.6
144.09	-	53.3	56.9
150.0	52.3	-	56.4
168.09	-	51.0	55.4
204.13	50.2	-	55.7
216.19	54.6	-	58.3
240.17	54.2	50.0*	55.8

*6 Mhz harmonic of IBM System Clock

This comparison shows the FCC testing done on both the WD1002-WA2 and the WD1003-WA2. In all cases except for those noted, WD1003-WA2 shows improvements over the WD1002-WA2.

The FCC Certificate of Approval is expected to be available by the end of April and can be provided at that time.

WESTERN DIGITAL
CORPORATION

WD1002-WA2 vs WD1003-WA2

FUNCTIONAL DIFFERENCES

WD1002-WA2

1. (Not avilable)

2. (Not available)

3. WD1002-WA2 Step Rates:

For 5 MHz WCLK:

R_3-R_0 =		
0000	≈35 μs.	1100 — 6.0 ms.
0001	.5 ms.	1101 — 6.5 ms.
0010	1.0 ms.	1110 — 7.0 ms.
0011	1.5 ms.	1111 — 7.5 ms.
0100	2.0 ms.	
0101	2.5 ms.	
0110	3.0 ms.	
0111	3.5 ms.	
1000	4.0 ms.	
1001	4.5 ms.	
1010	5.0 ms.	
1011	5.5 ms.	

4. (Not available)

WD1003-WA2

1. If Write Fault (WF) is latched, it can only be cleared by a reset (hardware/software).

2. If WF is detected during a Write operation, then the Write operatic is retried once before reporting a error (if retries are enabled).

3. WD1003-WA2 Step Rates:

For 5 MHz WCLK:

R3-R0 =		
0000	35μsec	
0001	.5msec	1100 — 6.0msec
0010	1.0msec	1101 — 6.5msec
0011	1.5msec	1110 — 3.2μsec
0100	2.0msec	1111 — 16μsec
0101	2.5msec	
0110	3.0msec	
0111	3.5msec	
1000	4.0msec	
1001	4.5msec	
1010	5.0msec	
1011	5.5msec	

4. Faster restore operation

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The attached comparison list shows the FCC testing done on both the WD1002-WA2 and the WD1003-WA2. In all cases except for those noted, the WD1003-WA2 board shows improvements over the WD1002-WA2.

The FCC Certidficate of Approval is expected to be available by the end of April, and can be provided at that time.