

CONFIGURATION TABLE

27	32	25	32
JPR	A/E	JPR	D/E
D/C		A/B	

WANG

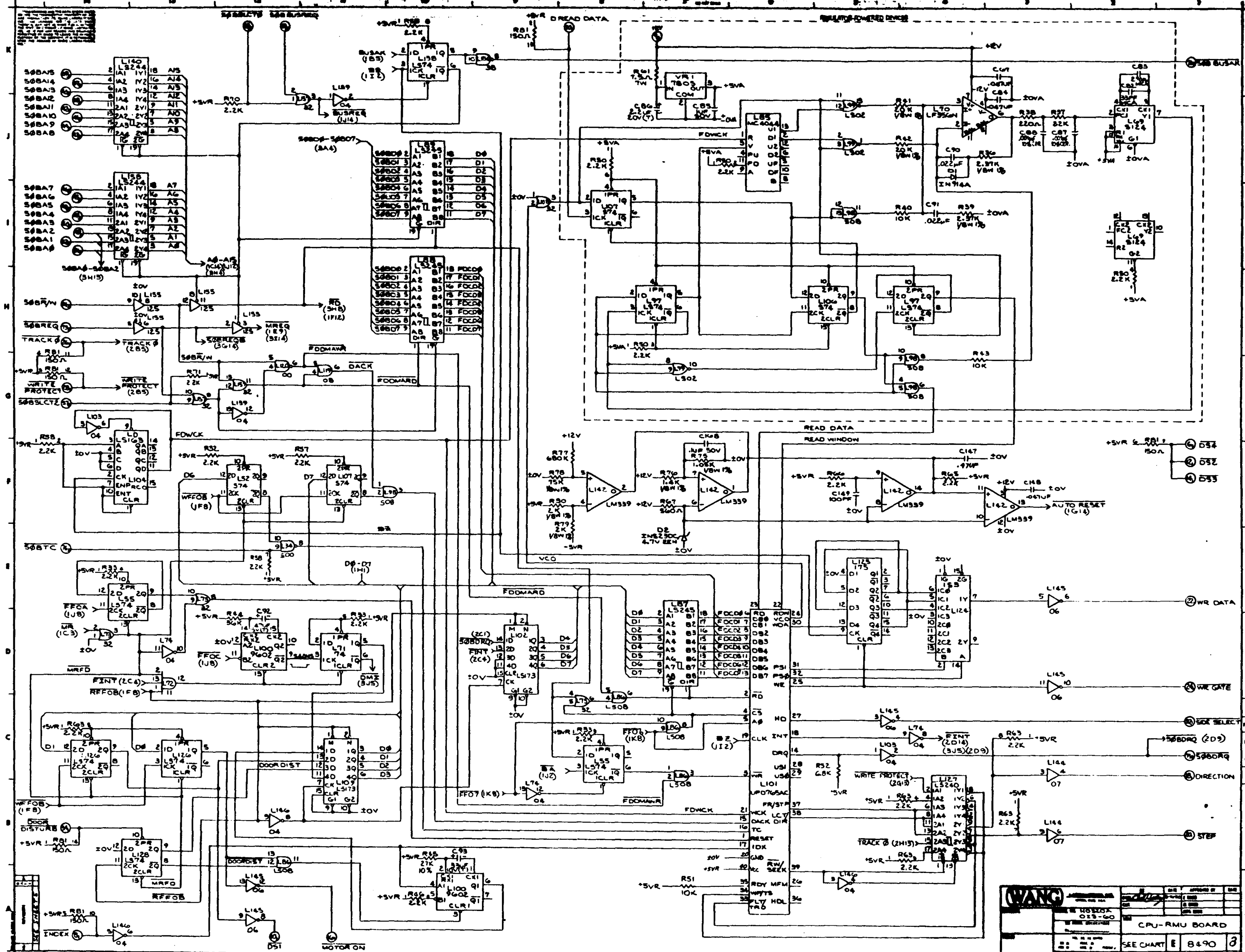
SEE CHART E 8490

CPU-RMU BOARD

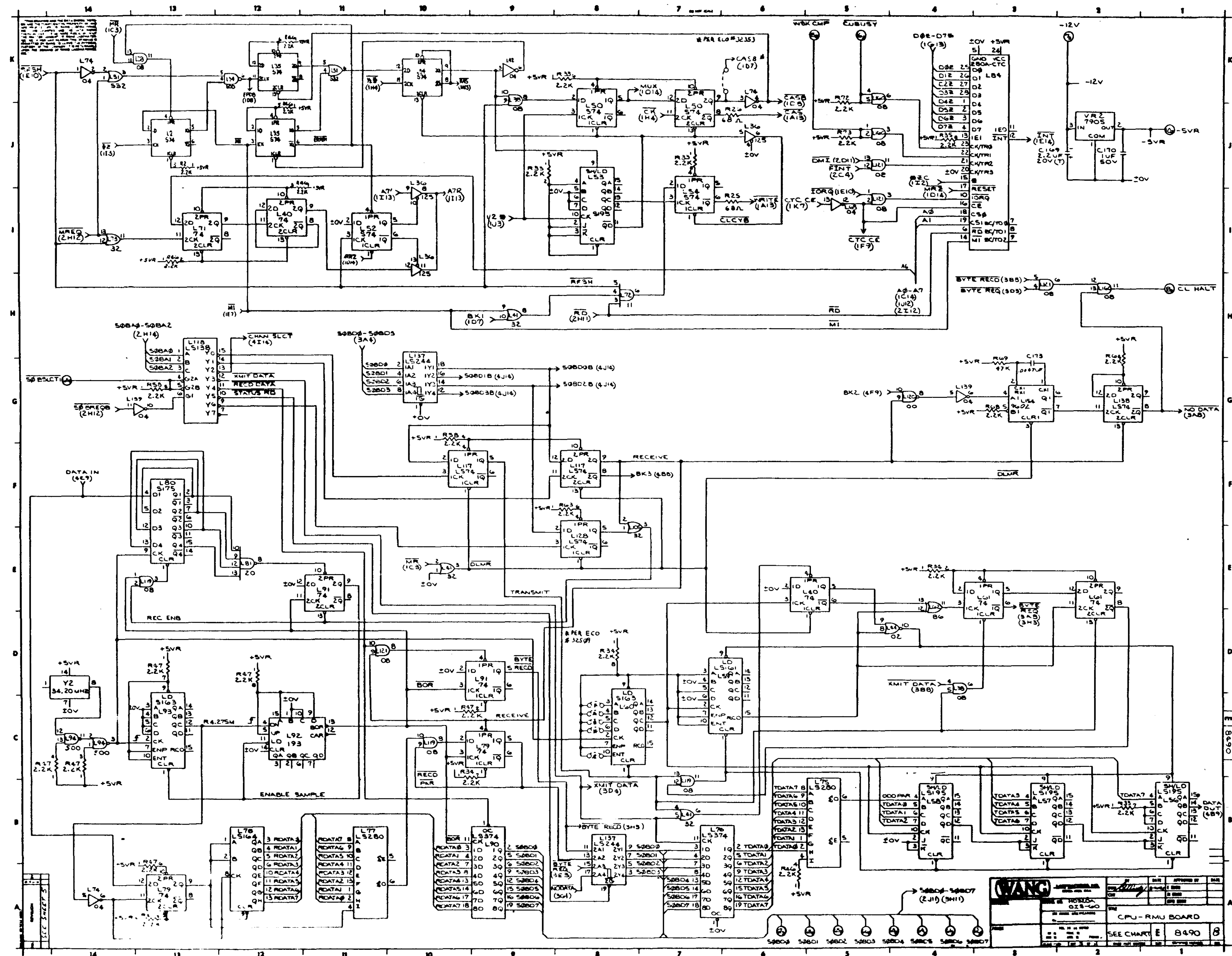
DATE: 10/10/68

DESIGNED BY: [Signature]

APPROVED BY: [Signature]

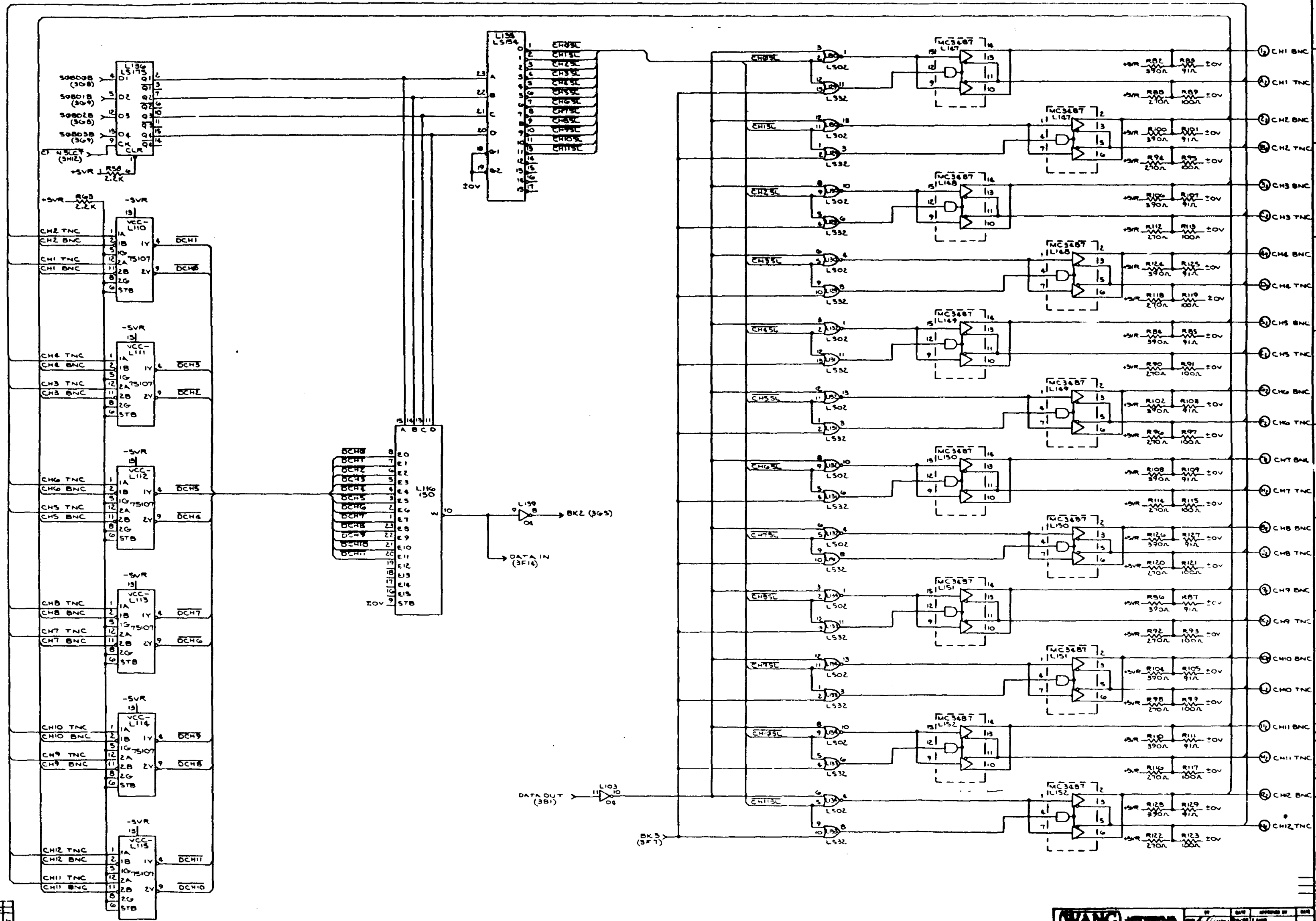


WANG		DATE	DESIGNED BY
CPU-RMU BOARD		DATE	DESIGNED BY
SEE CHART E 8490		DATE	DESIGNED BY
3		DATE	DESIGNED BY



WANG		DATE	DESIGNED BY	CHKD BY
CPU-RMU BOARD		REV	DATE	BY
SEE CHART E 8490		REV	DATE	BY
8490		REV	DATE	BY

14 13 12 11 10 9 8 7 6 5 4 3 2 1



SEC SHEET 5

WANG		DATE	DESIGNED BY	CHK
HORIZONTAL		03-1-60	W. J. G. /	
CPU-RMU BOARD				
SEE CHART	E 8490			

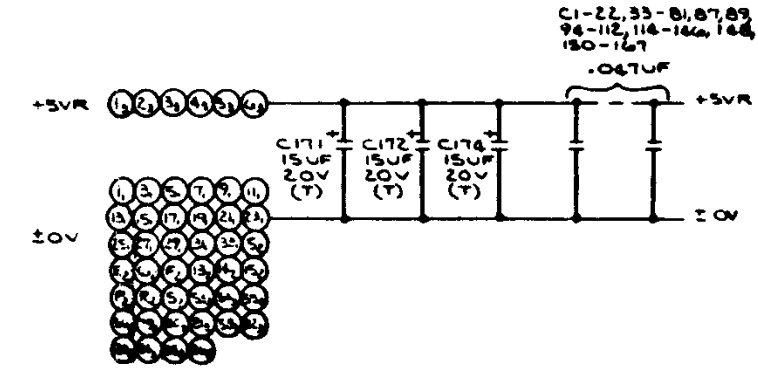
14 13 12 11 10 9 8 7 6 5 4 3 2 1

14 13 12 11 10 9 8 7 6 5 4 3 2 1

TYPE	E.C. LOC	SPARE
7400	L7	1
	L120	2
74000	L54	2
	L55	1
	L94	1
7402	L44	2
74502	L11	3
74552	L99	1
	L42	4
7404	L65	1
	L105	3
	L146	3
7406	L145	1
7407	L144	4
7408	L9	1
	L38	1
74508	L28	3
7410	L45	1
7411	L72	1
7420	L15	1
	L10	1
7432	L51	1
	L57	1
	L105	1
	L105	3
7457	L66	2
7458	L50	3
7474	L79	1
74574	L2	1
	L106	1
74574	L12	1
7486	L62	3
74125	L25	1
	L88	2
7402	L154	1
SPARE	L1	
	L67	
	L68	
	L145	

MNEMONICS	COORD
AG-A7	1K1
BUS-K	1A5
CHI BNC	4J1
CH2 BNC	4J1
CH3 BNC	4Z1
CH4 BNC	4H1
CH5 BNC	4H1
CH6 BNC	4F1
CH7 BNC	4F1
CH8 BNC	4E1
CH9 BNC	4E1
CH0 BNC	4D1
CH11 BNC	4C1
CH2 BNC	4C1
CHI TNC	4J1
CH2 TNC	4K1
CH3 TNC	4Z1
CH4 TNC	4H1
CH5 TNC	4H1
CH6 TNC	4F1
CH7 TNC	4F1
CH8 TNC	4E1
CH9 TNC	4D1
CH10 TNC	4D1
CH11 TNC	4C1
CH2 TNC	4B1
ELRAMP	3H1
END BUSREQ	1J14
EOBUSV	3K5
D READ DATA	2K6
CO-DT	1H1
DIRECTION	2B1
DOOR DISTOR	2B14
DOOR LOCK	2A12
DST	2C1
DST-DSE	2F1
INDEX	2A14
IN USE	2A11
MNDS	1J1
MOVOR ON	2A11
MRC	1A5
MREQ	1A4

MNEMONICS	COORD
ROI	1A4
SIDE SELECT	2C1
STEP	2B1
TRACKS	2H14
WR DATA	1A4
WR GATE	2C1
WRTE PROTECT	2G14
WRK CMP	3K5
EMRE	1J1
SOBAG-SOBA7	2J14
SOBAG-SOBA5	2J14
SOB BUSAK	2K1
SOB BUSREQ	2K12
SOBCC-SOCC7	3A5
SOBCC	2C1
SOBREQ	2H14
SOBR/W	2H14
SOBSCCTB	2K12
SOBSCCTP	3G14
SOBSCCTV	2G14
SOBYC	2E14
-5VR	3J1
-12V	3K2
+12V	2K7



Z10	Z09	Z10 = Z09 + 377 OR 378	Z10	Z10	Z10
8490-A	8490	L3, 4	L47	L84	L101
		310-007	378-004	377-0371	377-0420
				377-0368	

NOTES: ALL RES. ARE 1/4W 5% UNLESS OTHERWISE SPECIFIED.

1	2	3	4	5	6	7	8	9	10	11	12	13	14

REV 3

WANG	NO. 1000000	DATE	APPROVED BY
NO. 1000000	025-60		
CPU-RMU BOARD			
SEE CHART	E	8490	B