Technical Manual

DRAM512/2M

512Kbyte/2Mbyte DYNAMIC MEMORY MODULE

for the VMEbus

Revision B

Second Edition

1. General Product Description

The VMEspecialists DRAM512/2M (figure 1) is a series of high-performance dynamic RAM memory modules fully compatible with the VMEbus. These memory modules have the following features:

8, 16, and 32 bit data transfers

24 and 32 bit addressing

512 Kbyte (using 64K DRAMS) and 2 Mbyte (256K DRAMS) capacities

Data retention on power fail

Byte parity

Programmable interrupter

Error logging

Provisions for field upgrade to 2 Mbytes through device replacement/jumper change

Write/read access times: 215/255 ns. typ.

The memory module is constructed on a four layer printed circuit board. Extensive use is made of programmable logic and under the chip, low inductance capacitors. Machine screw sockets are optionally available for memory devices of the DRAM512. With this option, the board can be upgraded in the field to 2 Megabytes.

This series of high performance memory modules are exceptionally well suited for providing economical and reliable, high capacity, general purpose memory for VME-based computer systems.

2. Part Numbers

512Kbyte, 64K RAMS, memories in machine screw sockets: DRAM512-S
512Kbyte, 64K RAMS, without memory sockets: DRAM512-NS

2Mbyte, 256K RAMS, memories in machine screw sockets: DRAM2M

3. Greetings

All of us at VMEspecialists extend our welcome to you as you join our growing family of customers. We sincerely believe that product support is a crucial element of the product you have purchased. Please do not hesitate to contact us for applications assistance. Of course, the product manual is the most concise and accurate reference and careful attention here will in most instances prepare you for an easy and uneventful installation.

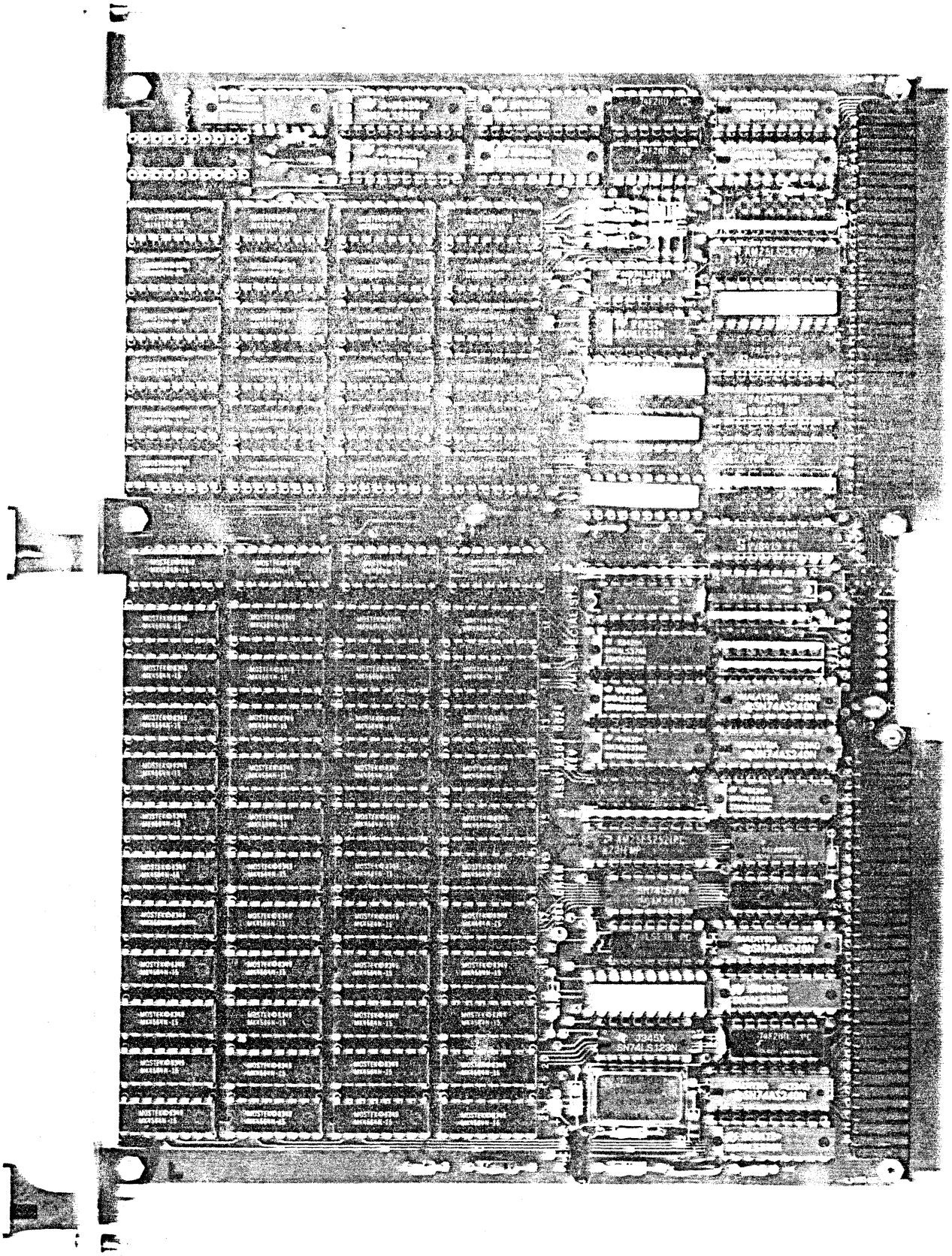


Figure 1.1 The DT-M512/2M Memory Module

5. Specifications

Capacity:	512k bytes (with 64k RAMS) 2M bytes (with 256k RAMS)
Word size:	8, 16, 32 bits
Addressing range:	24 or 32 bits of address (as set by address modifier)
Addressing:	In units of board capacity (memory) In 256 byte increments (control and status)
Error detection:	Byte parity (odd)
Access time:	215 ns. typ. (write) 255 ns. typ. (read)
Minimum cycle time:	333 ns. (write) 460 ns. (read)
	Address and cycle times given above assume a minimum time interval between address and data strobes.
Refresh:	Automatic, and transparent to user One 292 ns. cycle approx. every 14 microseconds.
Form factor:	VME double height
VME compatibility:	SLAVE DATA TRANSFER: Memory -- A32, D32 SLAVE Control registers: A16, D8 SLAVE INTERRUPTER: ANY ONE OF I(k) k=1..7 (STAT) PHYSICAL CONFIGURATION: EXP
Operating modes:	Memory read/write/read-modify-write Refresh Interrupt write interrupt vector read error log write control register
Environmental:	Operating temperature: 0 to 55 degrees C Storage temperature: -40 to 80 degrees C Operating humidity: 0 to 90% (no condensation) Storage humidity: 0 to 90% (no condensation) Operating altitude: -1000 to 10,000 feet ASL Storage altitude: -1000 to 20,000 feet ASL Vibration: Normal stresses of transport

Power requirements (2 Mbyte assembly):

Module configured for data retention during power fail:

Standby: 900 mA MAX (675 mA TYP) at +5SB
2.0 A MAX (1.4 A TYP) at +5, not required for data retention

Active reading/writing:

1.5 A MAX at +5SB (frequent 16 bit xfrs)
1.2 A TYP at +5SB (1 Mhz. 16 bit transfers)

2.0 A MAX (1.4 A TYP) at +5 VDC

Module not configured for retention during power fail:

Standby:
2.9 A MAX (2.1 A TYP) at +5 VDC

Active reading/writing:

4.4 A MAX at +5 VDC (max rate 32 bit transfers)
2.6 A TYP at +5 VDC, 1 Mhz, 16 bit data transfers

SIZE: 262 mm. high, 20 mm. wide, 180 mm. deep (viewed from front panel)

WEIGHT: 0.52 Kg, 1.15 pounds.

6. Installation and Jumper Options

Prior to installation, the board options must be configured by way of jumpers. Options include memory and I/O register addressing, interrupt level selection, and RAM power source selection. In addition, it may be necessary to jumper the VME backplane to insure proper continuity of the interrupt acknowledge daisy chain. Refer to figure 2 for assistance in locating jumper positions.

6.1 Memory addressing

For boards of 2Mbyte capacity, REMOVE jumpers: C1
C2
C6
C7

For boards of 512Kbyte capacity, INSERT jumpers: C6
C7

Memory modules are addressed in units of board capacity. For 512K boards addressing is based on the values of A19-A31, and for 2Mbyte boards, addressing is based on A21-A31. Address lines are mapped to jumper positions as follows:

A19 .... C1	A24 .... D1
A20 .... C2	A25 .... D2
A21 .... C3	A26 .... D3
A22 .... C4	A27 .... D4
A23 .... C5	A28 .... D5
	A29 .... D6
	A30 .... D7
	A31 .... D8 MSB

For those systems which are limited entirely to 24bits of address generation, D1-D8 may be ignored. An inserted jumper selects a corresponding address value of "0", a removed jumper selects "1". Boards are ordinarily shipped with a starting address of HEX 000000.

EXAMPLE: 512Kbyte module, starting address of 00200000 hex:

JUMPER C		JUMPER D		
5 ._.	A23	5 ._.	A28	
4 ._.	A22	4 ._.	A27	The ordering at left
6 ._.	(IN FOR 512K)	6 ._.	A29	matches the ordering
3 ._.	A21	3 ._.	A26	of jumpers on the board,
7 ._.	(IN FOR 512K)	7 ._.	A30	from top to bottom.
2 ._.	A20	2 ._.	A25	
1 ._.	A19	8 ._.	A31	
		1 ._.	A24	

6.2 Control Register Addressing

The control registers include the interrupt vector register, three error logging registers, and the mode control register. These are accessed using the supervisory short I/O transfer (16 bits of address). These registers may be entirely neglected if the user does not desire interrupts on error. However, it is important to be sure that there is no conflict with short I/O addresses of other modules in the VMEsystem.

Memory modules have been configured at the factory for a base I/O address of FF00 hex. The module occupies 256 bytes of I/O space.

Select a short I/O base address using jumpers B1-B8:

```
A15 .... B7
A14 .... B6
A13 .... B5
A12 .... B4
A11 .... B3
A10 .... B2
A9  .... B1
A8  .... B8
```

An inserted jumper selects a corresponding address value of "0", an absent jumper selects "1".

EXAMPLE: Select an I/O base address of 4E00.

Jumper B

```
A11  . .  3
A10  . .  2
A12  ._.  4
A9   . .  1
A13  ._.  5
A14  . .  6
A15  ._.  7
A8   ._.  8
```

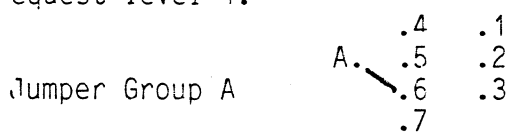
The ordering at left matches the ordering of jumpers on the board from top to bottom.

6.3 Interrupt Level Selection

If interrupt capability is desired, it is necessary to jumper a request level and an IDENTICAL acknowledge level. Interrupt levels range from 1 to 7, with level 7 having highest priority. Your board has been configured at the factory for interrupt level 6.

Jumper the request level with jumper group A. Wire-wrap a jumper from post "A" to the number of the corresponding interrupt level.

EXAMPLE: Use request level 4.



Use the following table to jumper the corresponding acknowledge level on jumper group E:

Interrupt Level	E1	E2	E3
1	OUT	IN	IN
2	IN	OUT	IN
3	OUT	OUT	IN
4	IN	IN	OUT
5	OUT	IN	OUT
6	IN	OUT	OUT
7	OUT	OUT	OUT

The sequence of jumpers on your board is, from top to bottom: E3
E2
E1

6.4 RAM Power Strapping

The VMEbus provides for an optional +5V standby power supply which can be used to maintain functions such as Time of Day clocks and non-volatile memories. There is a 1.5 Amp limit to the current any single card can draw from that supply. In systems which do not perform longword (32 bit) transfers, the RAM current draw on this dynamic memory board will meet those requirements and those users may choose to power the RAM chips and associated circuitry necessary for data retention from the standby power source. The factory wired configuration uses only the main +5V. source.

To use the +5V STANDBY power supply: JUMPER W2, REMOVE W1 and W1A.

To power the entire module from the normal +5V source: JUMPER W1, W1A.
REMOVE W2.

6.5 BERR* Assertion Option

As provided by the factory, BERR* is asserted only on an illegal longword transfer. Parity errors result in the generation of interrupts when interrupts are enabled. In this configuration, jumper W3 must be OUT.

You have the option of asserting BERR* on illegal transers or on parity errors. In this case, INSERT W3 and replace the socketed device at location 19B (part number 0204-0003) with part number 0204-0007. Because the cycle acknowledgement must now be delayed until the computation of the parity, this configuration delays the read access time by 80 ns.

6.6 Installation in a VMEsystem

The dynamic memory module connects all bus grants in to the corresponding bus grants out. It remains necessary to be sure of the following:

[1] The slot occupied by this module must have the interrupt acknowledge daisy chain jumper (P1-21A, P1-22A) removed.

[2] All empty slots in the system should provide continuity of the interrupt acknowledge and bus grant daisy chains:

JUMPER ON EMPTY SLOTS, P1 CONNECTOR:	21A-22A	IACK
	4B-5B	BG0
	6B-7B	BG1
	8B-9B	BG2
	10B-11B	BG3

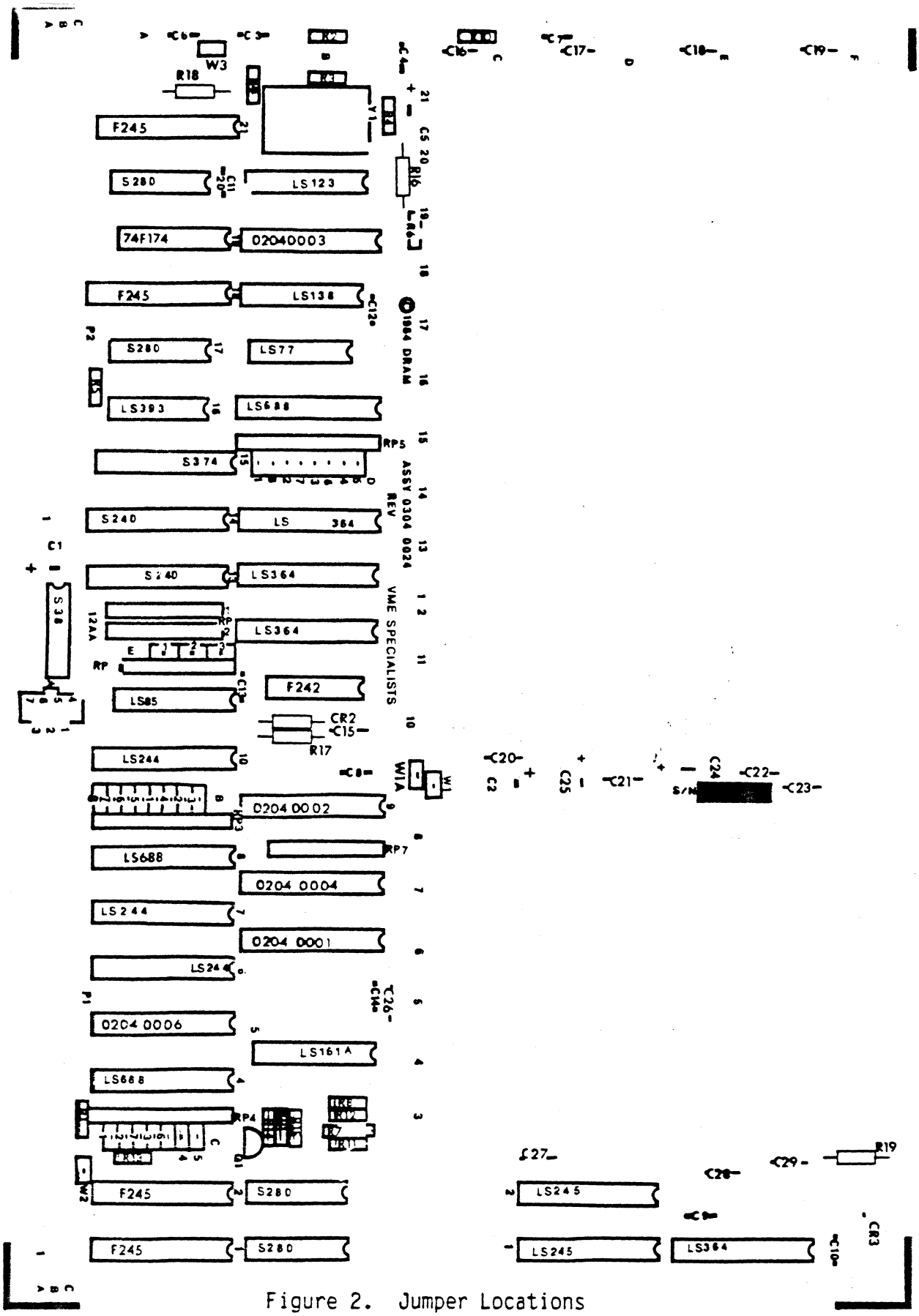


Figure 2. Jumper Locations

7. Theory of Operation

The memory array is organized as four banks of 64K (256K) by 18 bits. All memory devices share the same CAS/ address strobe, but there are four RAS/ lines, corresponding to the four banks. During a refresh operation, all four RAS/ lines act in unison. During a byte or word read, only one RAS/ is active and during a longword read, two RAS/ lines are active, to enable a full 36 bit transfer. Writes proceed similarly, except that there are two W/ write enable lines, one dedicated to the high byte, and one to the low byte. In this way, high byte, low byte, word, and longword writes are all possible through a combination of RAS/ and W/ signals (figure 3). CAS/ is, of course, active on every cycle except refesh. Those devices which are not selected see a CAS/ ONLY cycle which, in contrast to the RAS/ ONLY cycle, draws no added supply current.

Memory reads or writes are disabled on reset, or when the supply voltage drops below approximately 4.5 V. This minimum voltage for initiating a memory transfer is determined by the zener diode CR1. Transistor Q1 provides current gain and correspondingly higher sensitivity to variations in the supply voltage.

Extensive use is made of programmable logic for control and timing. Central to timing of the dynamic memories is a state machine, the device at 19B, clocked at 24 Mhz, which generates such signals as RAS/, CAS/, ROW ADDRESS ENABLE/, COL ADDRESS ENABLE/, RDERR/ (Parity error on memory read), REFRESH/, and DTACK*. Another programmable device at location 5A decodes address modifiers and signals when a memory transfer request MREQ/ or a control transfer IORQ/ is in progress.

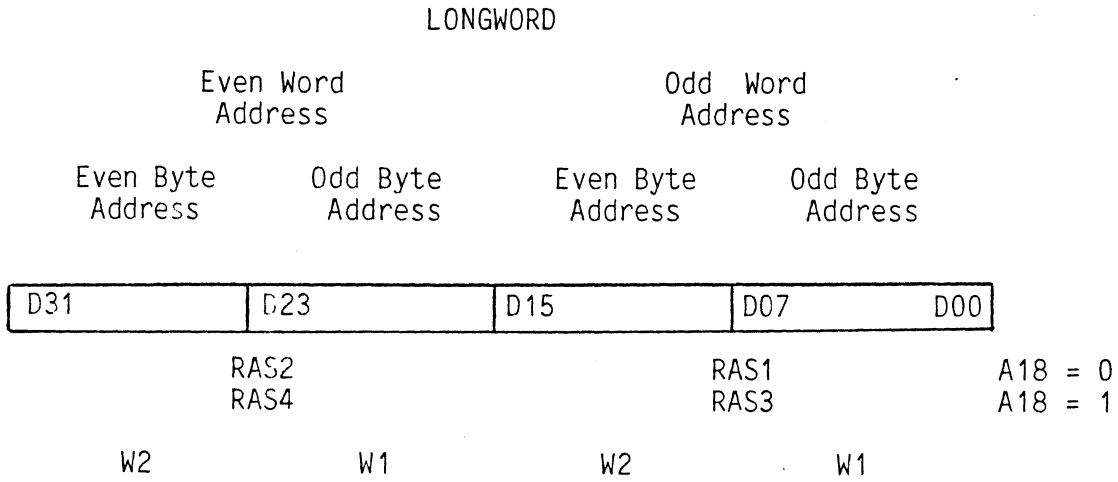
The module responds to memory transfer requests within any selected contiguous 512 or 2048 Kbyte block within a 4 Gbyte total address space. During short I/O control transfers, the module responds to any selected 256 byte block within the 64 Kbyte I/O space.

7.1 Modes of Operation

The memory module is capable of the following functions:

Memory read: Byte/Word/Longword
Memory write: Byte/Word/Longword
Memory read-modify-write: Byte/Word/Longword
Refresh
Interrupt
Control register write
Error logging register read
Interrupt vector write

All these functions occur in response to commands on the VMEbus except for refresh, which is automatically performed approximately once every 14 microseconds. While a refresh is in progress, requests for memory read or write will be held off until the refresh cycle is complete. During a refresh cycle, one row of all 72 dyanmic RAMS is recharged with a RAS/ only cycle.



Byte Adr	XX..X00	XX..X01	XX..X10	XX..X11
BYTE ACCESS				
LWORD*	high	high	high	high
A01	low	low	high	high
DS1*	low	high	low	high
DS0*	high	low	high	low
WORD ACCESS				
LWORD*	high		high	
A01	low		high	
DS1*	low	NOTE 1	low	NOTE 1
DS0*	low		low	
LONGWORD ACCESS				
LWORD*	low			
A01	low	NOTE 2	NOTE 2	NOTE 2
DS1*	low			
DS0*	low			

NOTES:

1. Not legal to access 16 bits of data at an odd byte address
2. Not legal to access 32 bits of data at odd byte or word addresses

Figure 3. Byte, Word, and Longword Addressing

7.2 Error Logging

When a parity error occurs on memory read, and interrupts have been enabled, the memory module generates an interrupt request on the preselected level and latches the offending address into a set of error logging registers which may be read at a later time for diagnostic purposes.

The three error logging registers are accessable through supervisory short-I/O byte reads. Their addresses (relative to the I/O BASE address defined in section 6.2) and contents are as follows:

ADDRL at address I/O BASE + 5

A6	A5	A4	A3	A2	A1	DS1/	DS0/

ADDRM at address I/O BASE + 3

A14	A13	A12	A11	A10	A9	A8	A7

ADDRH at address I/O BASE + 1

LWORD/	A21	A20	A19	A18	A17	A16	A15

7.3 Using the Control Register

The control register provides programmable control over interrupt enable and self-test functions. It is accessed by supervisory short I/O byte writes to the I/O base address (section 6.2) plus an offset of 3.

X	X	X	X	X	X	IE	FERR

X ..... Don't Care

IE ..... 1: Enable interrupts
0: Disable interrupts
On reset, interrupts are disabled

FERR ..... 1: Force a parity error on subsequent memory reads
0: No forced parity errors (normal operating mode)
On reset, the module returns to normal mode

The FERR capability aids in the testing of interrupt service software. It can also be used to test the board's interrupter and error logger.

7.4 Defining an Interrupt Vector

The interrupt vector resides in an on-board register. The vector value (0 to 255) may be specified dynamically through supervisory short I/O byte writes to the I/O base address (section 6.2) plus an offset of 1.

7.5 Address Modifier Codes

The memory module fully decodes the address modifier lines, and responds to those listed below:

Codes for memory read/write:

3E	Standard supervisory program access
3D	Standard supervisory data access
3A	Standard non-privileged program access
39	Standard non-privileged data access
0E	Extended supervisory program access
0D	Extended supervisory data access
0A	Extended non-privileged program access
09	Extended non-privileged data access

Code for control register read/write:

2D	Short supervisory I/O access

Short address uses 15 address lines (A01-A15)
Standard address uses 23 address lines (A01-A23)
Extended address uses 31 address lines (A01-A31)

7.6 Locating a failed RAM device

After an initial period of test, modern dynamic memory devices are remarkably reliable. The most common cause of failure is incorrect insertion into the socket, but devices can also be damaged by electrostatic charges and improper handling. Other possible causes of damage include operation at excessive temperatures or supply voltages. The table below will help in identifying the damaged device.

DATA BIT IN ERROR	A18 = 0	A18 = 1
31	21C	20C
30	19C	18C
29	19D	18D
28	19E	18E
27	19F	18F
26	21F	20F
25	21E	20E
24	21D	20D
23	17E	16E
22	17F	16F
21	15E	14E
20	17D	16D
19	17C	16C
18	15C	14C
17	15D	14D
16	15F	14F
15	6F	5F
14	6E	5E
13	6D	5D
12	6C	5C
11	4E	3E
10	4C	3C
9	4D	3D
8	4F	3F
7	11F	10F
6	13F	12F
5	13C	12C
4	11D	10D
3	11E	10E
2	11C	10C
1	13D	12D
0	13E	12E
PARITY BITS:		
D0-D7	8D	7D
D8-D15	8C	7C
D16-D23	8E	7E
D24-D31	8F	7F

8. VMEbus Interface Signals

P1 Connector Assignments:

PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5 STDBY	+12V
32	+5V	+5V	+5V

Notes:

BGIN lines are connected to BGOUT lines on board
The following lines are not used:
BBSY*, BCLR*, ACFAIL*, SYSFAIL*, BR0*, BR1*, BR2*, BR3*, SERCLK, SERDAT, -12V, +12V

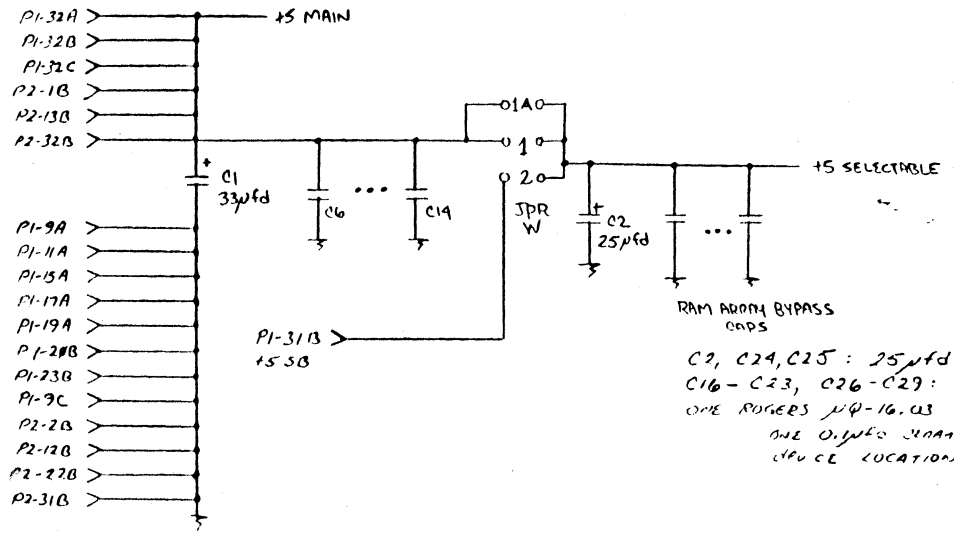
P2 Connector Pin Assignments:

PIN NUMBER	ROW B SIGNAL MNEMONIC
1	+5V
2	GND
3	RESERVED
4	A24
5	A25
6	A26
7	A27
8	A28
9	A29
10	A30
11	A31
12	GND
13	+5V
14	D16
15	D17
16	D18
17	D19
18	D20
19	D21
20	D22
21	D23
22	GND
23	D24
24	D25
25	D26
26	D27
27	D28
28	D29
29	D30
30	D31
31	GND
32	+5V

Notes: Rows A and C are not used.

I.C. POWER TABLE

QTY	TYPE	No. Pins	VCC	GND	REFERENCE DESIGNATIONS	POWER: MAIN/SELECTABLE
72	4164-15	16	8	16	C3-C21, D3-D21, E3-E21, F3-F21	S OPTIONALLY 41256-15
1	0209-0001	20	20	10	7B	M
1	0209-0002	20	20	10	9B	S
1	0209-0003	20	20	10	19B	S
1	0209-0004	20	20	10	8B	M
1	0209-0006	20	20	10	5A	S
5	74LS374	20	20	10	12B, 13B, 14B, 1E, 15A	12B-14B and 1E: M; 15A: S
3	74LS299	20	20	10	6A, 7A, 10A	M
4	74F245	20	20	10	1A, 2A, 18A, 21A	M
2	74F240	20	20	10	13A, 14A	M
4	74F280	14	14	7	1B, 2B, 17A, 20A	M
3	74LS688	20	20	10	9A, 8A, 16B	M
1	74LS393	14	14	7	16A	S
1	74F242	14	14	7	11B	M
1	7438	14	14	7	12AA	M
1	74LS161A	16	16	8	5B	M
1	74F138	16	16	8	18B	M
1	74LS77	14	4	11	17B	M
1	74LS85	16	16	8	11A	M
2	74LS245	20	20	10	1D, 2D	M
1	74LS123	16	16	8	20B	S
1	24 Mhz osc.	14	14	7	21B	S
1	74F174	16	16	8	19A	S



C2, C24, C25 : 25μfd TA
C16 - C23, C26 - C29 : 1.0μfd CERAM.
ONE ROGERS HQ-16.03 0.03μfd CAP and ONE 0.1MFD CERAMIC AT EVERY MEMORY DEVICE LOCATION.

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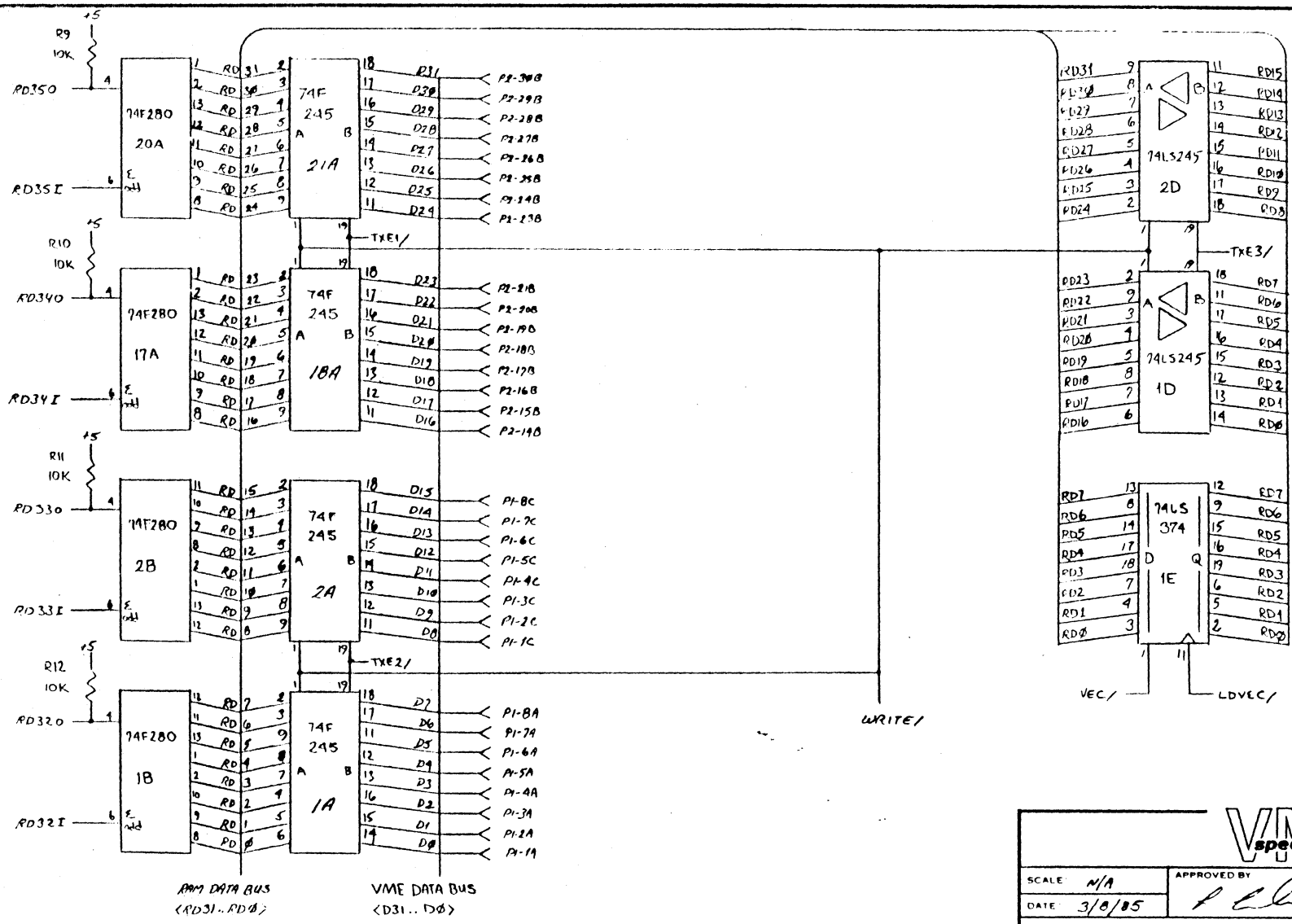
DATE 3/8/85		REVISED
DRAM 512/2M Pg. 1 of 7		REV B
POWER DISTRIBUTION		DRAWING NUMBER 0900-0017



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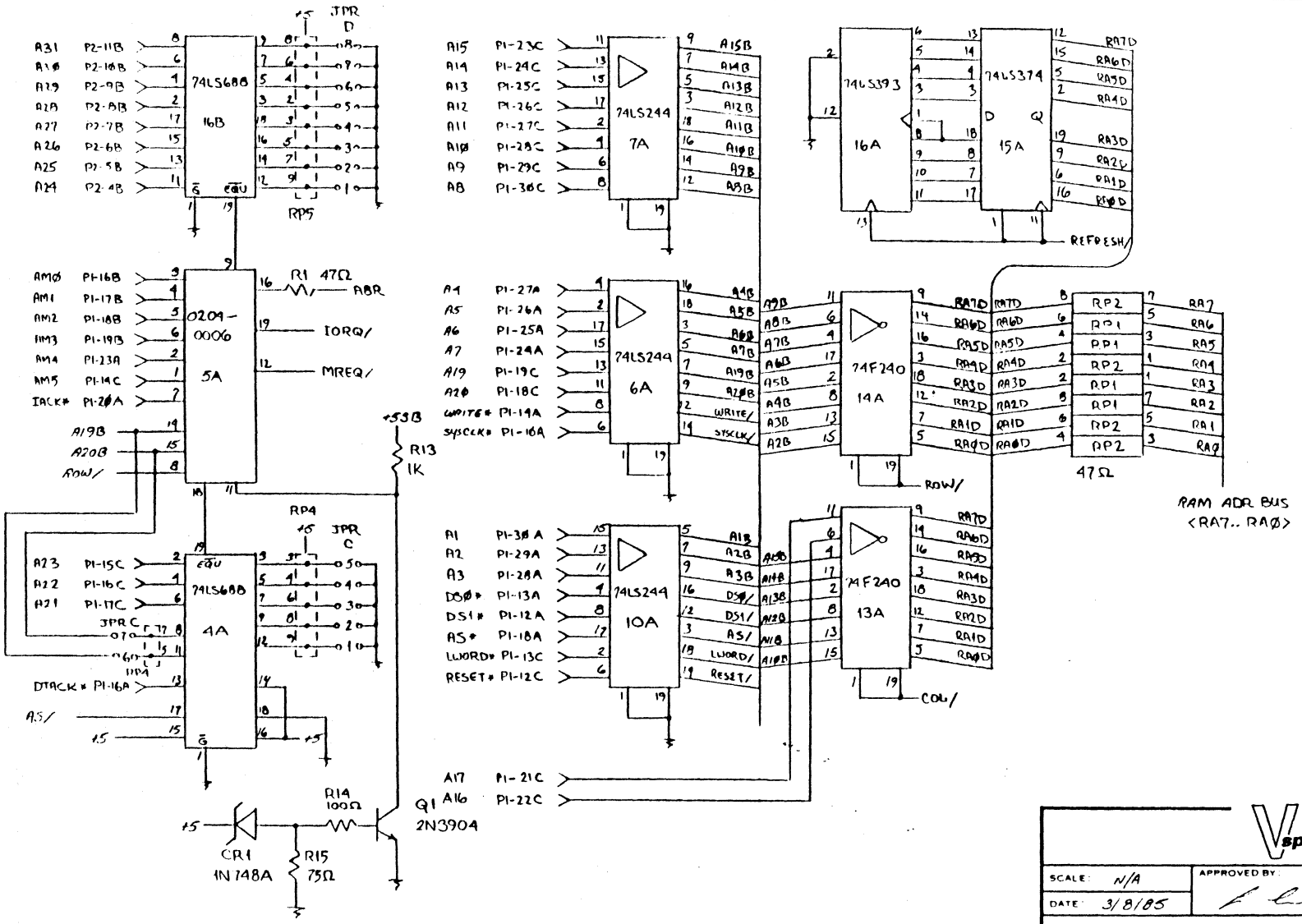
DRAM 512/2M pg 2 of 7		REV B
DATA PATHS		DRAWING NUMBER 0900-0017



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DRAM 512/2M Pg 3 of 7		REV B
ADDRESSING		DRAWING NUMBER 0500-0017

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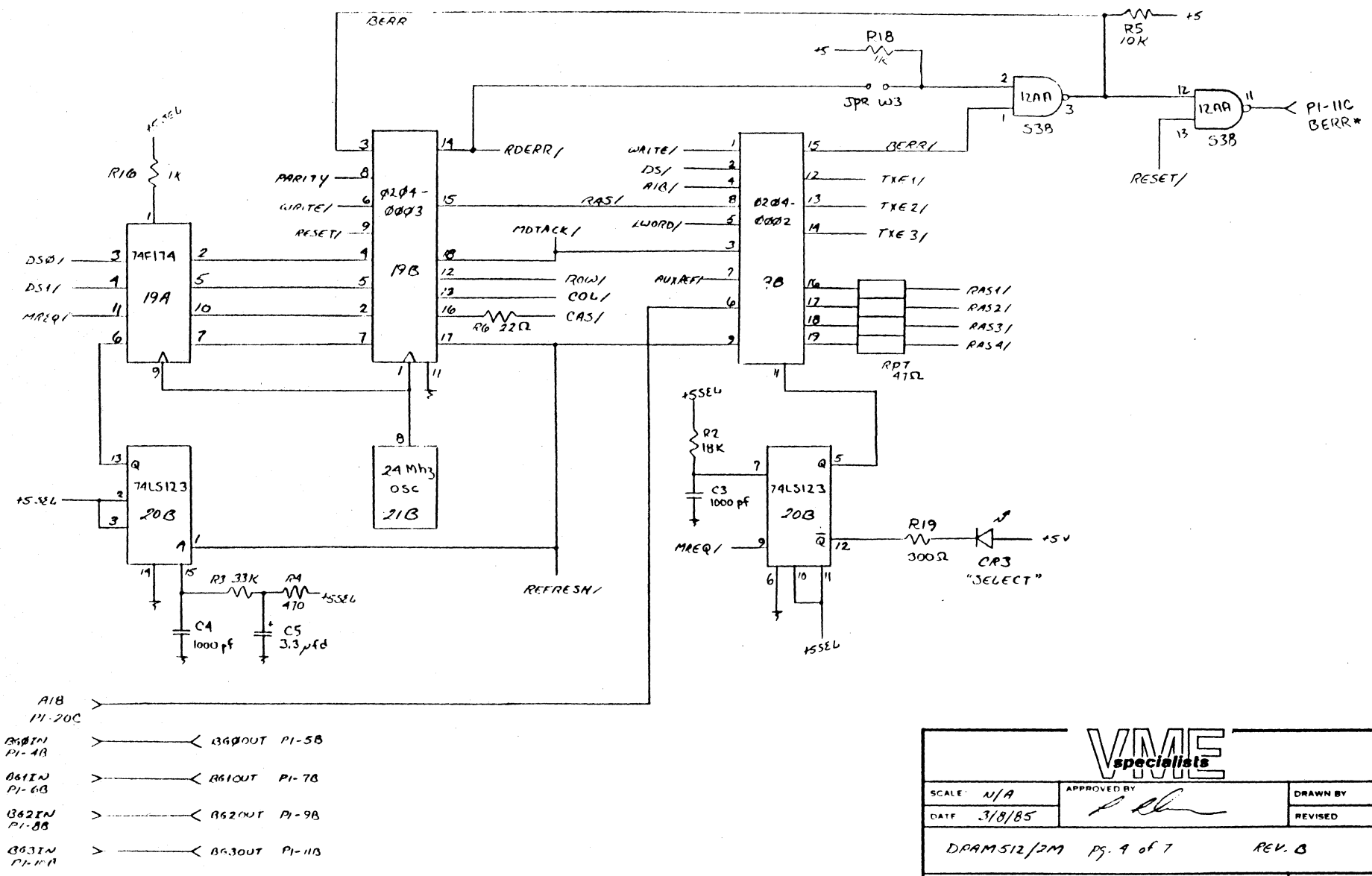

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DRAM512/2M pg. 4 of 7 REV. B

RAM CONTROL STATE MACHINE

DRAWING NUMBER 0900-0017

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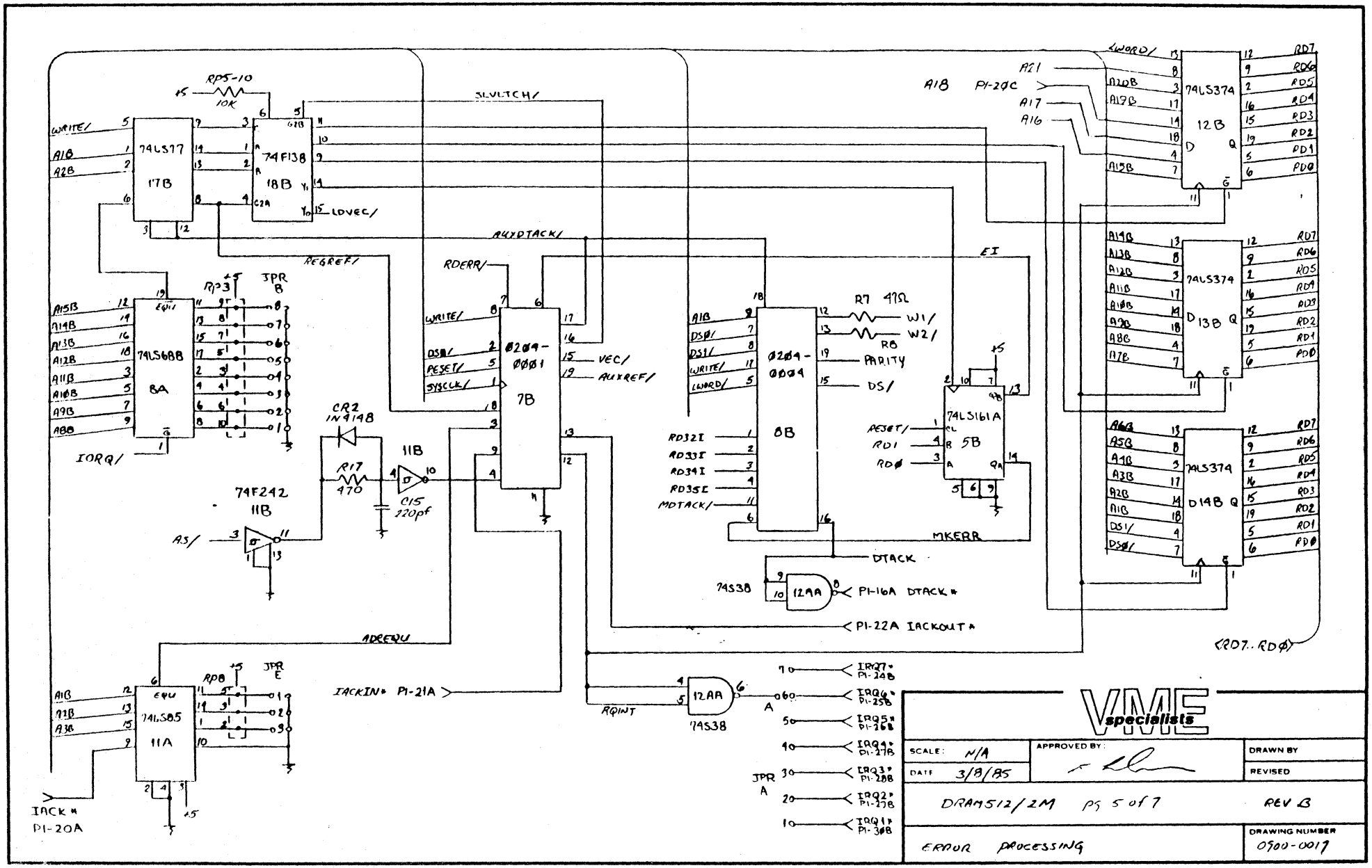

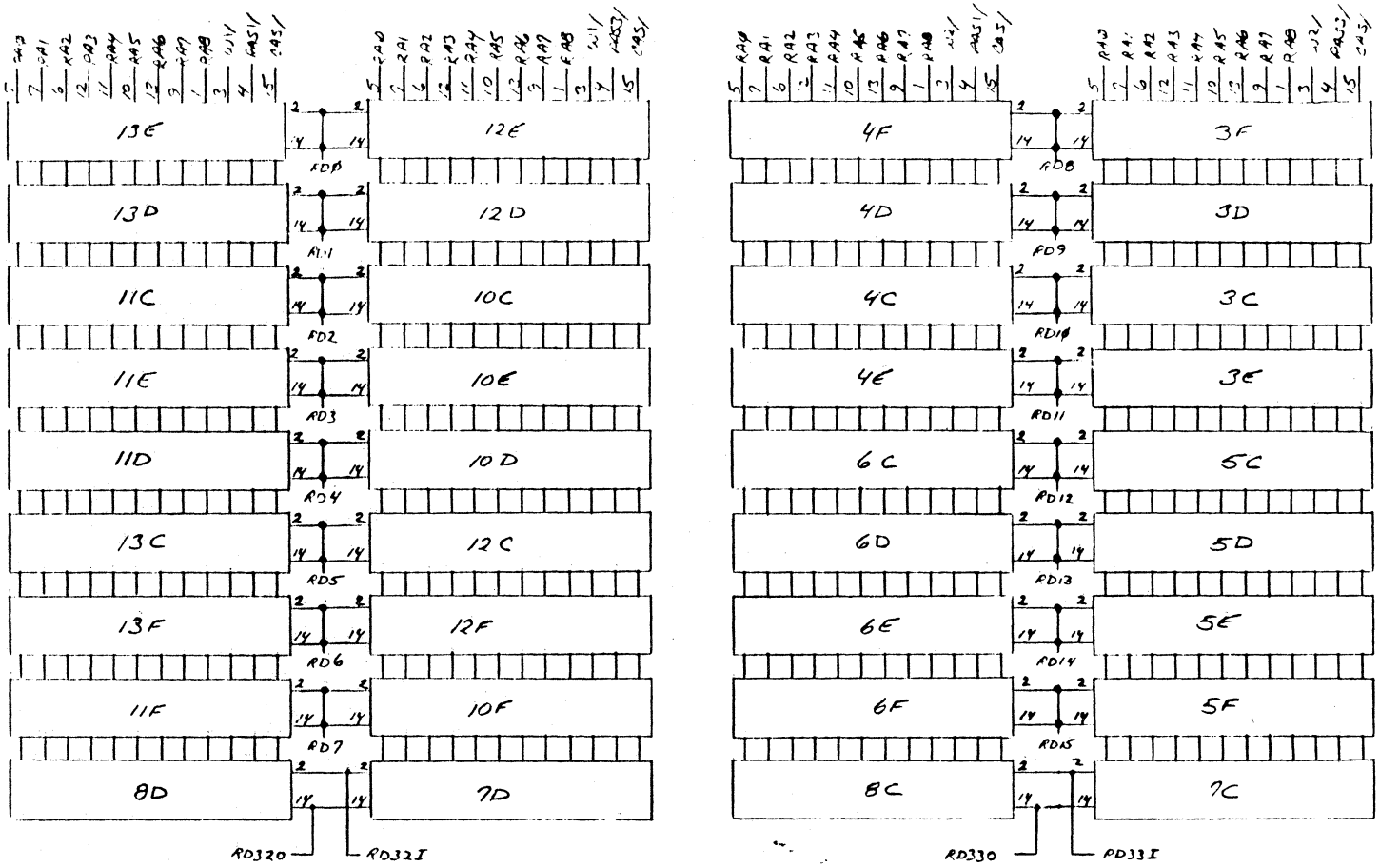

MOSTEK MK4564N-15
MOTOROLA MCM6665AP15
PANASONIC MN4164P-15
NEC D41256C-15
TOSHIBA TMM41256C-15

RAMS ARE 4164-15 OR 41256-15

NOTE V_{CC} - PIN 8
GND - PIN 16

RAM POWER IS JUMPER SELECTABLE +5, +5SB

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SCALE: N/A	APPROVED BY	DRAWN BY
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DRAM512/2M Pg. 6 of 7 REV B

MEMORY ARRAY PART 1 DRAWING NUMBER 0900-0017

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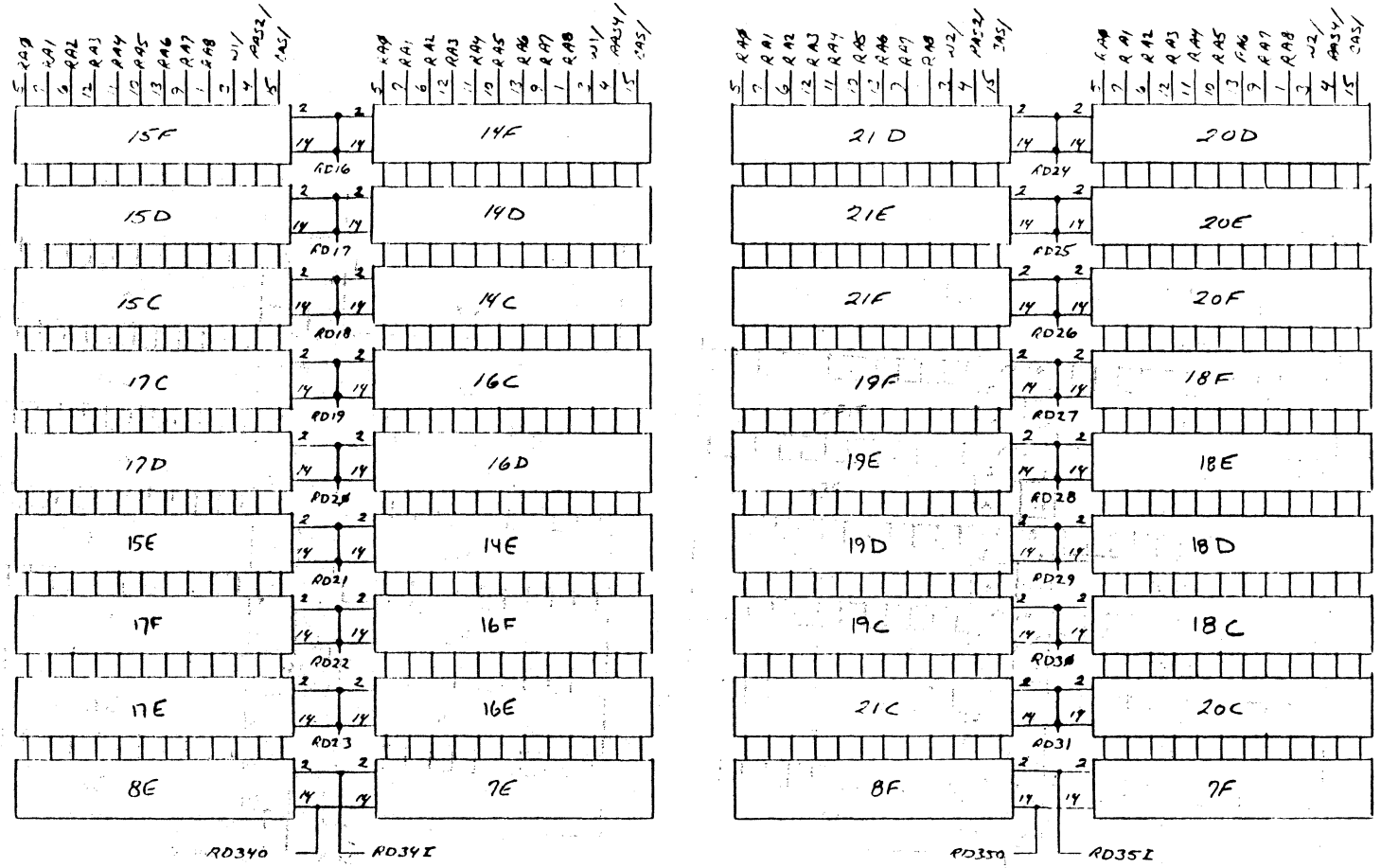

RAMS ARE 4164-15 OR 41256-15

NOTE Vcc - pin 8
GND - pin 16

RAM PWR JUMPER SELECTABLE AT JW #53B

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DATE 3/8/85			REVISED
DRAM512/2M Pg 7 of 7			REV B
MEMORY ARRAY part 2			DRAWING NUMBER 0900-0017