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70 SERIES MEMORY MAP OPERATION AND SERVICE MANUAL

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CHANGE RECORD

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Change Procedure:

When changes occur to this manual, updated pages are issued to replace the obsolete pages. On each updated page, a vertical line is drawn in the margin to flag each change and a letter is added to the page number. When the manual is revised and completely reprinted, the vertical line and page-number letter are removed.

LIST OF EFFECTIVE PAGES

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v through viii	references to old section 7 deleted
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TABLE OF CONTENTS

SECTION 1
GENERAL DESCRIPTION

SECTION 2
INSTALLATION

2.1 INSPECTION 2-1
2.2 PHYSICAL DESCRIPTION 2-1
2.3 DISCRETIONARY WIRING 2-1
2.4 INTERCONNECTION 2-2
2.5 CONFIGURATIONS 2-2
2.5.1 Normal Configuration 2-2
2.5.2 WCS Supported Configuration A 2-2
2.5.3 WCS Supported Configuration B 2-3
2.5.4 System Memory Lockout Configuration 2-3
2.5.5 Dual Memory Map Configuration 2-3

SECTION 3
OPERATION

3.1 I/O INSTRUCTIONS 3-1
3.2 OPERATING MODES 3-2
3.2.1 Inactive Mode 3-2
3.2.2 Executive Mode 3-2
3.2.3 User Mode 3-3
3.3 MAPPING 3-3
3.4 OPERATING SEQUENCES 3-3
3.4.1 Memory-Map Loading and Read-Back 3-3
3.4.2 Programmed I/O Read-Back 3-3
3.4.3 Executive Mode to Inactive Mode 3-6
3.4.4 Inactive Mode to Executive Mode 3-6
3.4.5 Executive Mode to User Mode 3-6
3.4.6 User Mode to Executive Mode 3-6
3.5 ACCESS-CONTROL MODES 3-8
3.6 MEMORY PROTECTION 3-8
3.6.1 Halt Errors 3-8
3.6.2 I/O Errors 3-8
3.6.3 Writing Errors 3-8
3.6.4 Jump Errors 3-9
3.6.5 Unassigned Errors 3-9
3.6.6 Instruction-Fetch Errors 3-9
3.6.7 I/O Data-Transfer Errors 3-9

SECTION 4
THEORY OF OPERATION

4.1 GENERAL 4-1
4.2 SYSTEM DESCRIPTION 4-1
4.3 FUNCTIONAL CIRCUITS 4-1
4.3.1 Key Multiplexor 4-5
4.3.2 RAM Address Multiplexor 4-5
4.3.3 Drivers and Row-Selection Decoder 4-5
4.3.4 RAM Array 4-6
4.3.5 I/O-Bus Data Multiplexor 4-6
4.3.6 I/O-Bus Drivers and Receivers 4-7
4.3.7 Word-Transfer Counter 4-8
4.3.8 Key and 64K-Mode Registers 4-8
4.3.9 Executive-State Register 4-9
4.3.10 Map-Address Counter 4-9
4.3.11 Input-Data Selection Register 4-9
4.3.12 DMA I/O Register 4-9
4.3.13 DMA Memory-Address Counter 4-9
4.3.14 I/O-Error Key Register 4-10
4.3.15 Instruction Address Register 4-10
4.3.16 Unassigned Address Register 4-10
4.3.17 Swapping Control 4-10
4.3.18 Access Control 4-10
4.3.19 Memory Address Drivers and Receivers 4-11
4.3.20 Active/Inactive Register 4-11
4.3.21 User/Executive Mode Register 4-11
4.3.22 Bypass Drivers 4-11
4.3.23 Memory-Data Circuits 4-11
4.3.24 Address Detection and Function Control 4-12
4.3.25 Memory Control 4-13
4.3.26 DMA Control 4-13
4.3.27 Mode Switching Control 4-14
4.3.28 Interrupt Control 4-14
4.4 MEMORY MAP TIMING 4-15

SECTION 5
MAINTENANCE

5.1 TEST EQUIPMENT 5-1
5.2 CIRCUIT BOARD REPAIR 5-1
5.3 CIRCUIT-COMPONENT IDENTIFICATION 5-1

SECTION 6
MNEMONICS

LIST OF ILLUSTRATIONS

Figure 1-1. Memory-Map Address Formation 1-2
Figure 2-1. Memory Map Board 2-1
Figure 2-2. Memory Map Interconnection 2-2
Figure 3-1. Data-Word Formats For Output-Data Transfers 3-4
Figure 3-2. Data-Word Formats For Input-Data Transfers 3-5
Figure 3-3. Data-Word Format For Memory-Map Loading and Read-Back Operations 3-6
Figure 3-4. User Mode to Execute Mode Flow Chart 3-7
Figure 4-1. Memory-Map System Block Diagram 4-1
Figure 4-2. Key Multiplexor Block Diagram 4-3/4-4
Figure 4-3. Memory Map Functional Block Diagram 4-5
Figure 4-4. Layout of RAM Array 4-6
Figure 4-5. RAM Array Block Diagram 4-7
Figure 4-6. I/O-Bus Data Multiplexor 4-7
Figure 4-7. I/O Bus Drivers 4-8
Figure 4-8. Executive-State Register Block Diagram 4-9
Figure 4-9. DMA I/O Register 4-9
Figure 4-10. Memory-Data Paths Between Processor and Expansion Memories 4-11
Figure 4-11. Data Flow for Map Loading Operation 4-13
Figure 4-12. Data Flow for Map Read-Back Operation 4-14
Figure 4-13. Programmed I/O Data Transfer 4-15
Figure 4-14. Memory-Map Loading via High-Speed DMA 4-16
Figure 4-15. Memory-Map Read-Back via High-Speed DMA 4-17
Figure 4-16. Memory Map Loading/Read-Back Termination 4-18
Figure 4-17. Memory Mapping 4-19
Figure 4-18. I/O and Halt Error Detection 4-20
Figure 4-19. Jump-Error Detection 4-20
Figure 4-20. Unassigned and Writing Error Detection 4-21
Figure 4-21. Instruction-Fetch Error Detection 4-21
Figure 4-22. I/O Data-Transfer Error Detection 4-22
Figure 4-23. Memory Protection Interrupt 4-22
Figure 4-24. Executive-Mode to Inactive-Mode Switching 4-23
Figure 4-25. Inactive-Mode to Executive-Mode Switching 4-23
Figure 4-26. Executive-Mode to User-Mode Switching 4-24
Figure 4-27. User-Mode to Executive-Mode Switching 4-24

LIST OF TABLES

Table 1-1. Memory Map Specifications 1-1
Table 1-2. Glossary 1-3
Table 3-1. I/O Instructions 3-1
Table 3-2. Executive-Mode States 3-3
Table 3-3. Access-Control Modes 3-8
Table 3-4. Interrupt Addresses 3-8
Table 4-1. Row-Selection Decoder Truth Table 4-6
Table 4-2. First Multiplexor Truth Table 4-8
Table 4-3. Second Multiplexor Truth Table 4-8
Table 4-4. Interrupt-Address Bit Configurations 4-8
Table 4-5. Access-Control Decoder Truth Table 4-10
Table 4-6. Memory-Data Multiplexor Truth Table 4-12
Table 4-7. EXC2 Decoder Truth Table 4-12
Table 4-8. Function Codes for SEN Instructions 4-12
Table 4-9. Output-Transfer Format Truth Table 4-13

SECTION 1
GENERAL DESCRIPTION

The **V70 Series Memory Map Manual** describes the SPERRY UNIVAC memory map and its interface with SPERRY UNIVAC V70 series computers.

The manual is divided into seven sections:

- Introduction to the memory map, related publications, specifications, and glossary
- Installation and interconnection data
- Operation
- Theory of operation
- Maintenance
- Mnemonics list
- Test programs

Documents such as logic diagrams, schematics and parts lists are supplied in a system documentation package. This documentation is assembled when the equipment is shipped, and reflects the configuration of a specific system.

The following list contains the document numbers of other manuals pertinent to the Varian 70 series computers (the x at the end of each document number is the revision number and can be any digit 0 through 9).

Title	Manual Number
Processor Manual	98 A 9906 02x
Semiconductor Memory Manual	98 A 9906 04x
16K Core Memory (990 NSec) Manual	98 A 9906 25x
Option Board Manual	98 A 9906 05x
Power Supply Manual	98 A 9906 06x
Microprogramming Guide	98 A 9906 07x
Writable Control Store Manual	98 A 9906 08x
V76 System Reference Manual	98 A 9906 23x
V77-600 System Reference Manual	98 A 9906 40x
V70 Architecture Manual	98 A 9906 00x
MAINTAIN III Manual	98 A 9952 07x
VORTEX Reference Manual	98 A 9952 10x
VORTEX II Reference Manual	98 A 9952 24x

(K = 1,024)

Mapping operations can be performed independently in up to sixteen 32K logical (virtual) memory areas. A 64K-mode of operation is available to provide eight 64K logical-memory areas. Map numbers 0 through 15 are used to identify the logical memory area, with map 0 being reserved for the VORTEX II operating system. The logical memory addresses are mapped into physical memory pages consisting of 512 words each. Page assignments for each logical memory are under control of the VORTEX II page-allocation routine.

NOTE

Although the VORTEX II operating system is referred to in this manual, the memory map consists of general-purpose hardware that allows operation in other software environments.

Figure 1-1 is a block diagram showing the address translation that is performed by the memory map. Either the processor or priority memory access (PMA) option generates a 16-bit logical address plus a 4-bit key. The most-significant seven bits of the address are combined with the key bits to address a location in the memory map's random-access-memory (RAM) array. When the 64K-mode enabling signal is set by an I/O output-data transfer instruction, the memory map is placed in the 64K mode of operation. The RAM array produces a 13-bit output consisting of three fields:

a. A 9-bit field that is concatenated with the least-significant 9-bit field of the logical address to form the 18-bit physical address.

b. A 2-bit field used for access control.

c. A 2-bit field used for swapping control.

The most-significant two bits of the physical address are decoded to select one of the four 64K memory buses. The other 16-bits of the physical address are used to address a location in the selected memory module.

Specifications for the memory map are listed in table 1-1.

Table 1-1. Memory Map Specifications

Parameter	Specification
Physical memory size	Up to 256K words.

(continued)

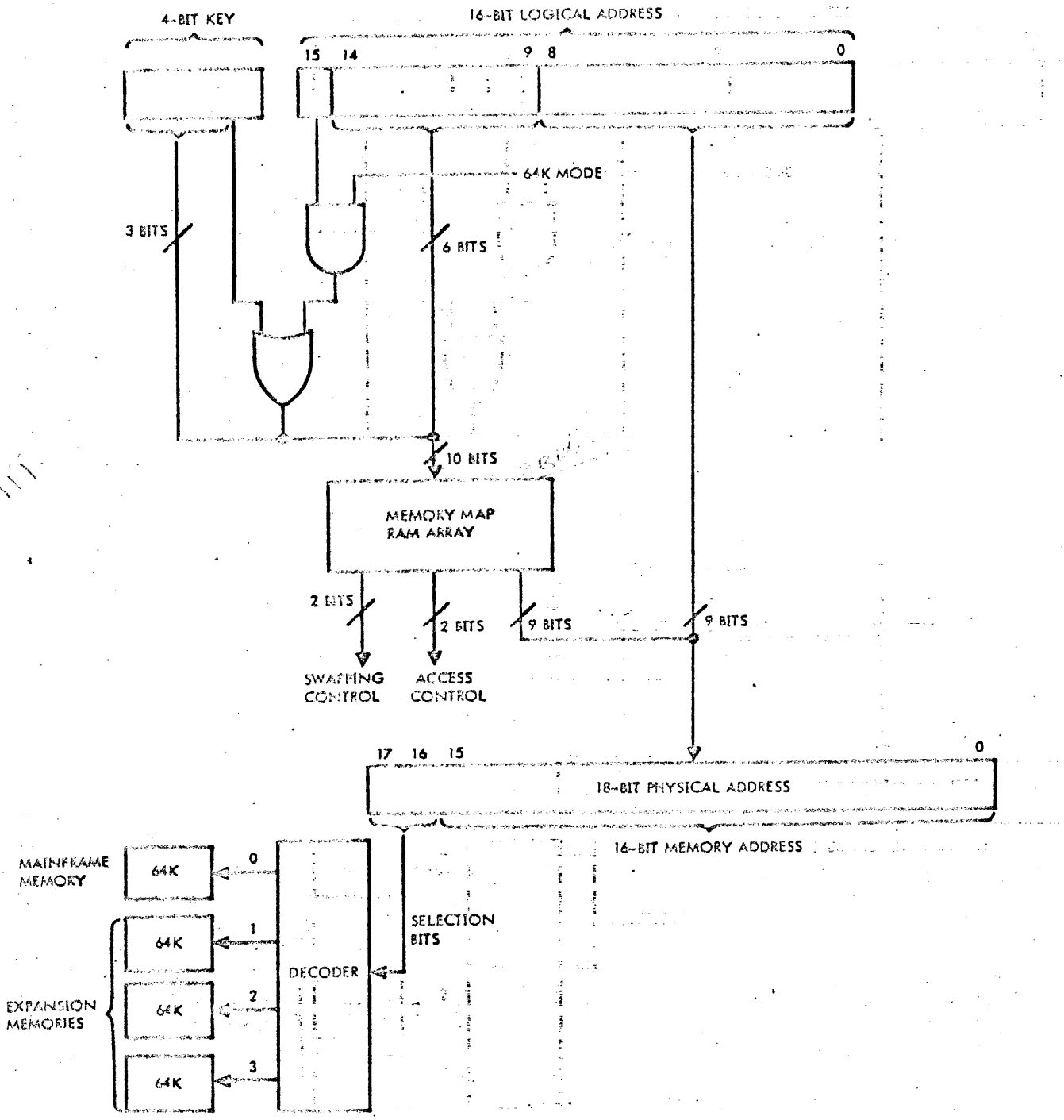

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Figure 1-1. Memory-Map Address Formation

Table 1-1. Memory Map Specifications *(continued)*

Parameter	Specification
Logical memory size	Two modes are available: a. up to 32K words b. up to 64K words
Page size	512 words.
Number of logical memory areas	Up to 16 with 32K words. Up to 8 with 64K words. A combination of 32K and 64K word sizes is possible.
Memory access times	With the memory map active, memory access is delayed 104 nanoseconds for the first 64K of memory and 156 nanoseconds for memory above 64K. With the memory map inactive, memory access is delayed by 27 nanoseconds. These are worst-case delays for standard operating modes.
System configuration	Provides mapping of addresses for processor, DMA, and PMA on one memory port. Mapping on more than one port requires one memory map for each port (not supported by VORTEX II).
Loading	The memory-map RAM array is loaded and read via DMA operations. The loading word rate is 715 kHz; the reading word rate is 358 kHz.
Operating modes	User mode, executive mode, and inactive mode.
Priority assignments	The memory map's memory-protection feature is assigned the highest system priority. Priority assignment for DMA operation is made independently.
Logic levels (internal)	High = +2.4 to +5.0V dc Low = 0 to +0.4V dc
Logic levels (I/O bus)	High = +2.8 to +3.6V dc Low = 0 to +0.5V dc
Dimensions	Contained on a 15.6 by 19 inch printed-circuit board.
Installation	Plugs into a V70 series mainframe chassis using one module slot.
Input power	+5V dc at 17 amperes.
Operational environment	0 to 50 degrees C, 0 to 90 percent relative humidity without condensation.

Table 1-2 is a glossary of terms used in this manual.

Table 1-2. Glossary

Term	Definition
Logical address	An address in a logical memory area.
Logical memory	A set of memory locations used by the programmer. Logical memory may or may not have contiguous physical memory locations.
Map numbers	Numbers 0 through 15 assigned to the maps used by the operating system and the various users. The numbers are determined by four key bits originating from either the BIC, PMA, map key register, or processor (using WCS microprogramming).
Mapping	The process of translating a logical memory address to a physical memory address.
Page	A 512-word block of physical memory.
Physical address	An address in physical memory.
Physical memory	Random-access memory defined by hardware.
Privileged instruction	Any instruction that causes a memory protection violation when used in the user mode (i.e., halt and I/O instructions). The halt instruction is only permitted in the inactive mode.
Swapping	The process of moving data between main and auxiliary memory in order to multiplex the use of main memory.

SECTION 2
INSTALLATION

2.1 INSPECTION

The SPERRY UNIVAC memory map has been packed and inspected to ensure its arrival in good working order. To prevent damage, take care during unpacking and handling. Check the shipping list to ensure that all equipment has been received. Immediately after unpacking, inspect the equipment for shipping damage. Ascertain that wires and cables are neither loose nor broken, and that hardware is secure. If damage exists:

a. Notify the transportation company.

b. Notify Sperry Univac.

c. Save all packing material.

2.2 PHYSICAL DESCRIPTION

The memory map circuits are on a 15.6 by 19 inch printed-circuit (PC) board (p/n 44P0685). Figure 2-1 shows dimensions and connectors of the memory map board.

2.3 DISCRETIONARY WIRING

Connections of the various jumper terminals on the memory map PC board are listed in the memory map option drawing 01A1541 (in system documentation package). These connections are normally installed at the factory, but are referenced here in case the user wishes to have his memory map system expanded or changed in the field. The jumper-terminal designations referred to in the option drawing appear on the memory map board adjacent to the particular terminal.

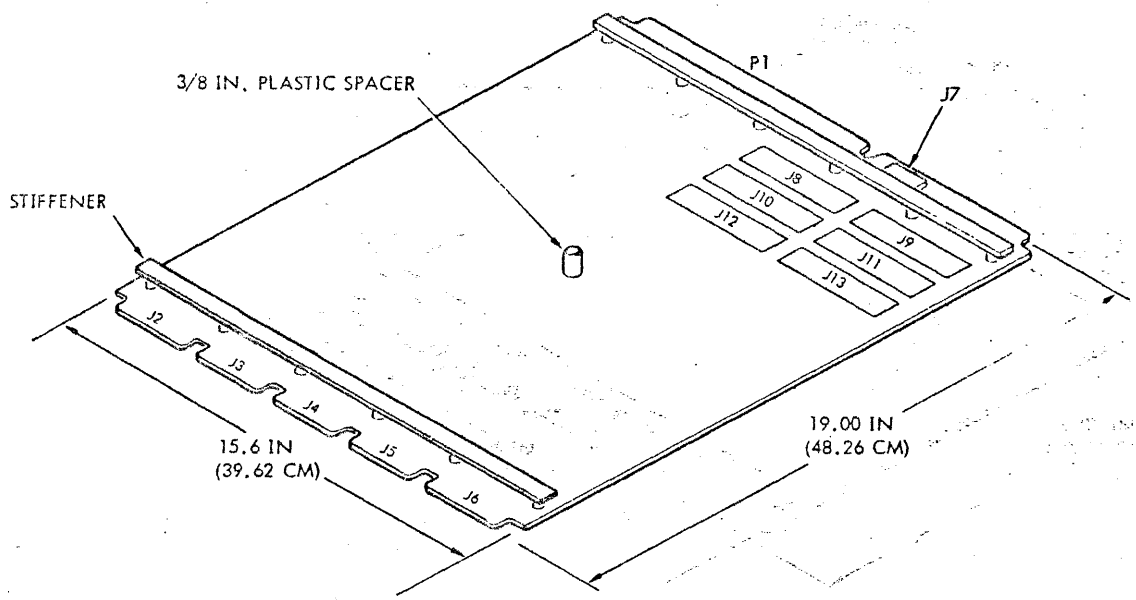

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Figure 2-1. Memory Map Board

2.4 INTERCONNECTION

The memory map board plugs into a single module slot of the V70 series mainframe chassis. Functions of the memory map board connectors are listed as follows:

P1, mainframe memory

J2, not used

J3, option-board auxiliary I/O bus

J4, processor

J5, I/O bus

J6, option board and processor

J7, power

J8, through J13, expansion memories

Power supplied to the memory map board via connector J7 is normally provided by a +5-volt power supply (p/n 01P12x0). It may also be supplied by excess +5-volt power from a memory expansion supply.

Figure 2-2 shows the memory map board interconnection in a V70 series mainframe. Pin assignments for the connectors on the memory map board are provided in the logic diagram (p/n 91C0448) in system documentation package.

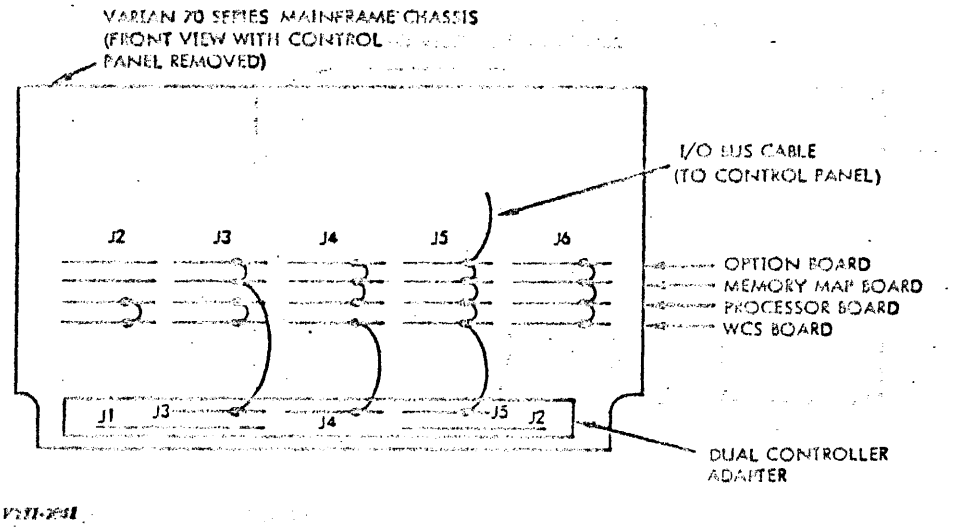


Figure 2-2. Memory Map Interconnection

2.5 CONFIGURATIONS

The following subsections describe the memory-map configurations that are available.

2.5.1 Normal Configuration

The normal memory map configuration is supported by VORTEX II and has the following characteristics:

a. The key bits are provided by the key register (section 4.3) on the memory map board.

b. The active memory map is placed in the executive mode (section 3.2) on any interrupt.

c. The memory map enters the user mode (section 3.2) by the EXC2 0246 instruction followed by a jump instruction (section 3.1).

d. Privileged instructions are assigned to map 0.

2.5.2 WCS Supported Configuration A

In this configuration, the key register on the processor board is used (instead of the key register on the memory map board) to permit rapid key changes through microprogramming rather than key changes over the I/O bus. Characteristics of this configuration are:

a. The key bits are provided by the key register on the processor board.

b. The active memory map is placed in the executive mode on any interrupt.

c. The memory map enters the user mode by the EXC2 0246 instruction followed by a jump instruction.

d. Privileged instructions can be assigned to map 0 as in the normal configuration, or they can be assigned to all maps in which case there is no privileged instructions.

2.5.3 WCS Supported Configuration B

This configuration is the same as the A version except that interrupts are handled with microprogramming instead of the executive mode. In this configuration, the executive mode is jumper disabled. Characteristics of this configuration are:

a. The key bits are provided by the key register on the processor board.

b. With the executive mode disabled, there is no hardware distinction between the executive and user modes.

c. The memory map enters the active mode by the EXC2 0146 instruction followed by a jump instruction.

d. Privileged instructions can be assigned to map 0 as in the normal configuration, or they can be assigned to all maps in which case there is no privileged instructions.

2.5.4 System Memory Lockout Configuration

Through jumper connections on the memory map board, this configuration connects a memory lockout signal (MHGY- or MHMY-) to one of the expansion memories (MHGYn-(1-3) or MHMYn-(1-3)).

2.5.5 Dual Memory Map Configuration

In this configuration, two memory map boards are used, one for each memory port. Systems using this configuration contain a PMA and processor on different memory ports. Characteristics of this configuration are:

a. The two memory maps are assigned the same device address.

b. The two memory maps are loaded simultaneously from the I/O bus via high-speed DMA.

c. The following functions are jumper disabled on the memory map connected to the PMA:

1. Memory protection (except writing errors)
2. Memory map read-back
3. Executive mode

d. To avoid possible conflicts in using the memory map, a software interlock is required between memory-map loading/read-back and PMA operations.

SECTION 3
OPERATION

The SPERRY UNIVAC memory map contains no operating controls or indicators. Operation of the memory map is normally controlled by the VORTEX II operating system. However, by writing his own control program, the user can operate the memory map without using VORTEX II. For maintaining and testing the memory map, a MAINTAIN III test program is available. The MAINTAIN III Reference Manual provides a full discussion of the Megamap Test Program, which verifies correct operation and isolates malfunctions of V70 memory map and megamap options.

3.1 I/O INSTRUCTIONS

Memory-map I/O instructions can only be executed from map 0 (operating system) or an inactive memory map. Table 3-1 lists the I/O instructions with the mnemonics and octal codes for device address 46. An alternate device address is 56.

Table 3-1. I/O Instructions

Mnemonic	Octal Code	Function
External Control		
EXC2 046	104046	Executive Mode to Inactive Mode. Places the memory map in the inactive mode upon fetching the contents at the effective address of the jump instruction that follows.
EXC2 0146	104146	Inactive Mode to Executive Mode. Places the memory map in the executive mode upon fetching the contents at the effective address of the jump instruction that follows.
EXC2 0246	104246	Executive Mode to User Mode. Places the memory map in the user mode upon fetching the contents at the effective address of the jump instruction that follows.
EXC2 0346	104346	Start DMA Transfer. Starts a memory map DMA transfer.
EXC2 0446	104446	Reset DMA Transfer. Resets the memory map's DMA-transfer logic.
EXC2 0546	104546	Clear Executive-Mode Mask. Removes the executive-mode mask.
EXC2 0646	104646	Enable Memory Protection. Enables the memory protection function of the memory map.
EXC2 0746	104746	Disable Memory Protection. Disables the memory protection function of the memory map.
Sense		
SEN 046	102046	Sense DMA Activity. Senses if the memory map is performing a DMA operation.

(continued)

Table 3-1. I/O Instructions *(continued)*

Mnemonic	Octal Code	Function
SEN 0146	102146	Sense Abnormal DMA Termination. Senses for the error termination of a DMA loading or read-back operation.
Transfer*		
IME 046	102046	Transfers data from memory map to main memory.
INA 046	102146	Transfers data from the memory map to the A register.
INB 046	102246	Transfers data from the memory map to the B register.
CIA 046	102546	Transfers data from the memory map to the cleared A register.
CIB 046	102646	Transfers data from the memory map to the cleared B register.
OME 046	103046	Transfers data from main memory to the memory map.
OAR 046	103146	Transfers data from the A register to the memory map.
OBR 046	103246	Transfers data from the B register to the memory map.

*These transfer instructions are for control registers in the memory map. Loading and reading of the memory-map RAM array occur with the high-speed DMA operations.

3.2 OPERATING MODES

The memory map has three modes of operation: inactive, executive, and user.

3.2.1 Inactive Mode

When the memory map is in the inactive mode, the first 32K of physical memory (64K if the writable control store is used) is available unmapped and all instructions are permitted. This mode is entered either by a system reset condition or a branch sequence from the executive mode consisting of the EXC2 046 instruction followed by any jump instruction.

3.2.2 Executive Mode

This mode is entered by an interrupt or by a branch from the inactive mode to an active-map condition. The branch sequence is actually an EXC instruction followed by any jump instruction. In this mode, all instructions except HLT are permitted. From the executive mode, the memory map can be switched to the inactive mode.

The executive mode has four states that define operations occurring between map 0 and the user maps. Setting up of the executive-mode states is accomplished with I/O instructions under control of the VORTEX II operating system. As shown in table 3-2, instruction- fetch operations are always from map 0, while operand-fetch and operand-store operations can be from any map depending on the executive-mode state. The following are exceptions:

a. To ensure that all instruction fetches are from map 0, indirect addressing must not exceed the first level in states 2 or 3 of the executive mode. This is because after the first level of indirect addressing, instruction fetches in some cases (i.e., SRE and IJMP instructions) are treated as operand fetches by the memory map.

(continued)

b. In all executive-mode states, the execution of a jump-and- mark instruction causes the program-counter contents to be stored in map 0.

c. In all executive-mode states, the execution of a LDAI, LDBI, or LDXI instruction always causes the effective register to be loaded with the operand fetched from map 0.

d. Any interrupt causes the memory map to enter the masked executive mode. This masked condition causes the executive mode to operate as if it were in state 0 even though the executive-state register may contain another value. In this condition, memory-map status is read into map 0 during the interrupt service routine. By executing the EXC2 0546 instruction, the mask is removed and the executive mode returns to the state determined by the value in the executive-state register.

Table 3-2. Executive-Mode States

State	Instruction Fetch	Operand Fetch	Operand Store
0	Map 0	Map 0	Map 0
1	Map 0	Map 0	Map n
2	Map 0	Map n	Map 0
3	Map 0	Map n	Map n

Notes:

1. Map 0 refers to the operating system.
2. Map n refers to the user map specified by the key bits.
3. States 1 through 3 cause an additional 142 nanoseconds delay in memory accessing.

3.2.3 User Mode

In this mode, all operands and instructions are mapped according to the key bits and contents of the RAM array. If an interrupt occurs, the memory map is switched to the executive mode. The memory map is switched from the executive mode to the user mode by the real-time executive in the VORTEX II operating system.

3.3 MAPPING

The mapping function is performed for either a DMA, PMA, or processor operation. In DMA operations, the mapped address utilizes the 4-bit key from the BIC plus the 16-bit logical address from the processor. In PMA operations, the mapped address utilizes the 4-bit key from the block-transfer controller (BTC) plus the 16-bit logical address from the PMA option. In processor operations, the mapped address is normally derived from the memory map's key register and the 16-bit logical address from the processor.

3.4 OPERATING SEQUENCES

This section describes the sequences of the various memory-map operations. Figures 3-1 and 3-2 show the data-word formats used with output- and input-data transfers, respectively. Figure 3-3 shows the data-word format for the memory-map loading and read-back operations.

3.4.1 Memory-Map Loading and Read-Back

The following sequences occur in memory-map loading and read-back operations via DMA (using map 0):

a. Using output-data transfer instructions, (OME, OAR, or OBR), the processor transfers three data words to the memory map. The first word contains the direction of DMA transfer and the initial 10-bit map address (figure 3-1b). The second word contains the initial 16-bit memory address of the DMA transfer (figure 3-1c). The third word contains the number of words in the DMA transfer (figure 3-1d).

b. The processor issues the EXC2 446 instruction to reset the DMA-control logic in the memory map.

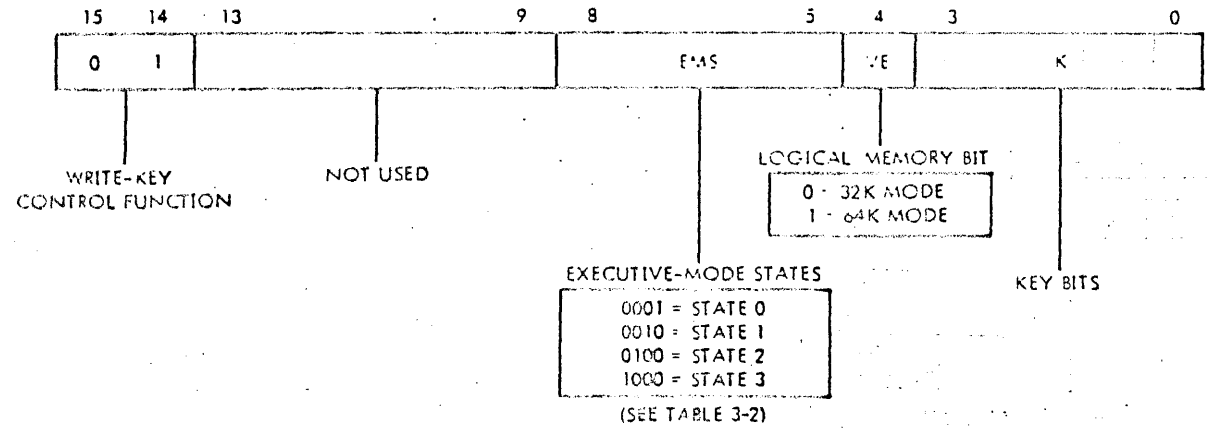
c. The processor issues the EXC2 0346 instruction to start the DMA transfer operation.

d. The standard method for verifying the completion of DMA transfers consists of using the two SEN instructions. The processor issues SEN 046 to sense if the memory map is still performing the DMA transfer. If it is not performing the DMA transfer, SEN 0146 is issued to sense if the DMA-transfer termination is due to an error.

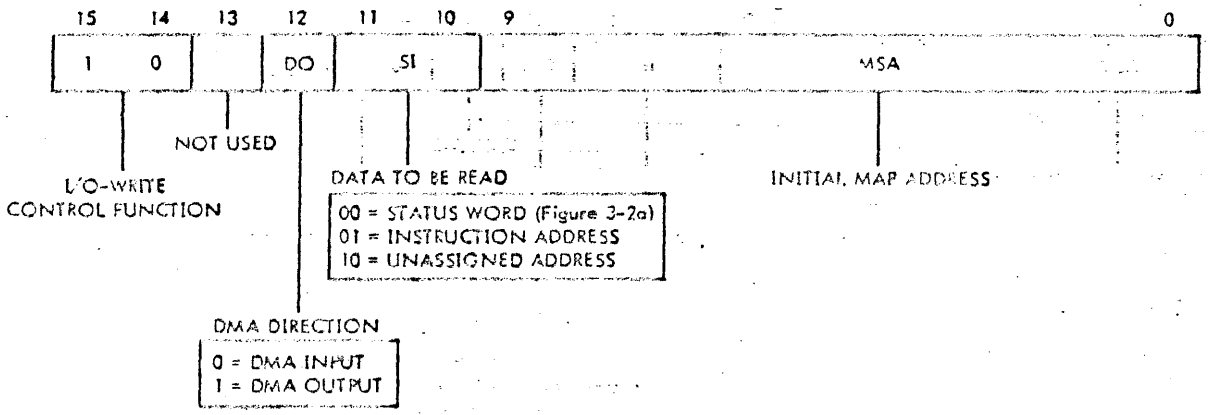
e. An optional method for verifying the completion of DMA transfers consists of using the DMA-completion interrupt. A counter in the memory map counts the number of DMA transfers and indicates when all transfers are complete. An interrupt is sent to the processor when either all transfers are completed or an error occurs during one of the transfers. When the interrupt is acknowledged, the processor is directed to memory address 016.

3.4.2 Programmed I/O Read-Back

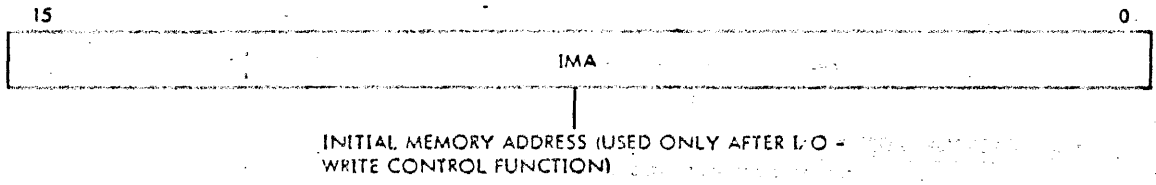
This operation provides a read-back function of the memory map's internal-status signals (figure 3-2a), instruction address register (figure 3-2b), and the unassigned



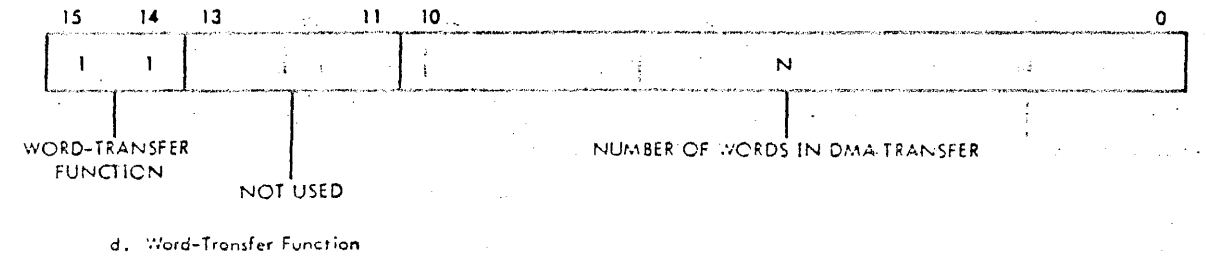
a. Write-Key Control Function



b. I/O-Write Control Function



c. Initial Memory Address of a DMA Transfer



d. Word-Transfer Function

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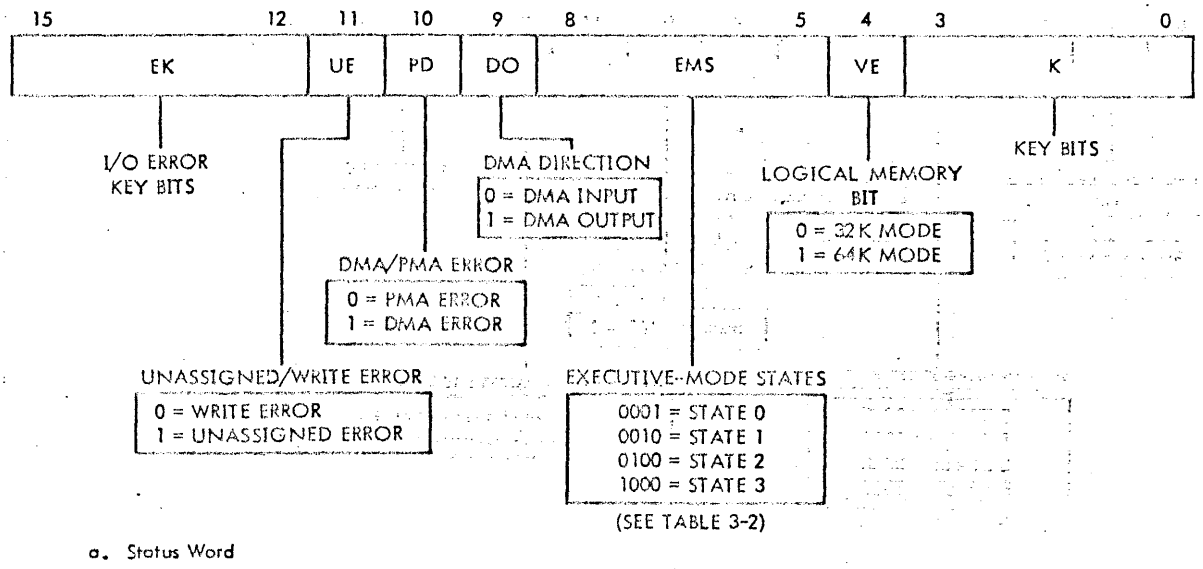
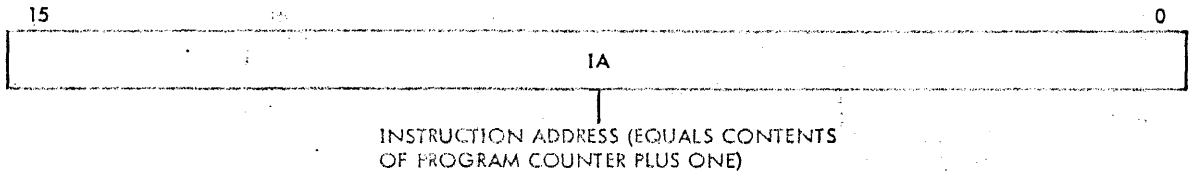
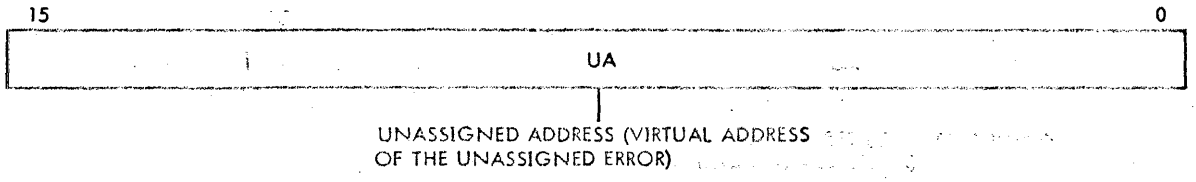
Figure 3-1. Data-Word Formats For Output-Data Transfers



a. Status Word



b. Instruction Address



c. Unassigned Address

VTII-2045

Figure 3-2. Data-Word Formats For Input-Data Transfers

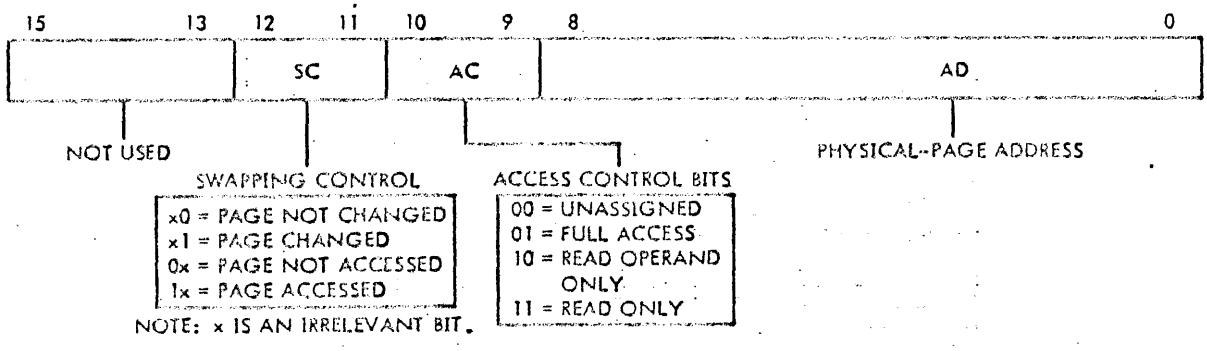


Figure 3-3. Data-Word Format For Memory-Map Loading and Read-Back Operations

address register (figure 3-2c). The sequences of operations are listed below:

a. Using an output-data transfer instruction, the processor transfers a data word (figure 3-1b) to the memory map. The type of data to be read back is specified by bits 10 and 11 of this data word.

b. Using an input-data transfer instruction (IME, INA, INB, CIA, or CIB), the processor reads back the data specified by the output-data word.

3.4.3 Executive Mode to Inactive Mode

The following sequences occur when the memory map is switched from the executive mode to the inactive mode:

a. The processor issues the EXC2 046 instruction to enable switching to the inactive mode.

b. The processor executes a jump instruction. If the jump condition is not met, the memory map remains in the executive mode.

c. If the jump condition is met, the memory map switches to the inactive mode when the contents of the effective jump address are fetched. The effective jump address is not mapped.

3.4.4 Inactive Mode to Executive Mode

The following sequences occur when the memory map is switched from the inactive mode to the executive mode:

a. The processor issues the EXC2 0146 instruction to enable switching to the executive mode.

b. The processor executes a jump instruction. If the jump condition is not met, the memory map remains in the inactive mode.

c. If the jump condition is met, the memory map switches to the executive mode when the contents of the effective jump address are fetched. The effective address is mapped using map 0.

3.4.5 Executive Mode to User Mode

The following sequences occur when the memory map is switched from the executive mode to the user mode:

a. The processor issues the EXC2 0246 instruction to enable switching to the user mode.

b. The processor executes a jump instruction. If the jump condition is not met, the memory map remains in the executive mode.

c. If the jump condition is met, the memory map switches to the user mode when the contents of the effective jump address are fetched. The effective address is mapped using the user map.

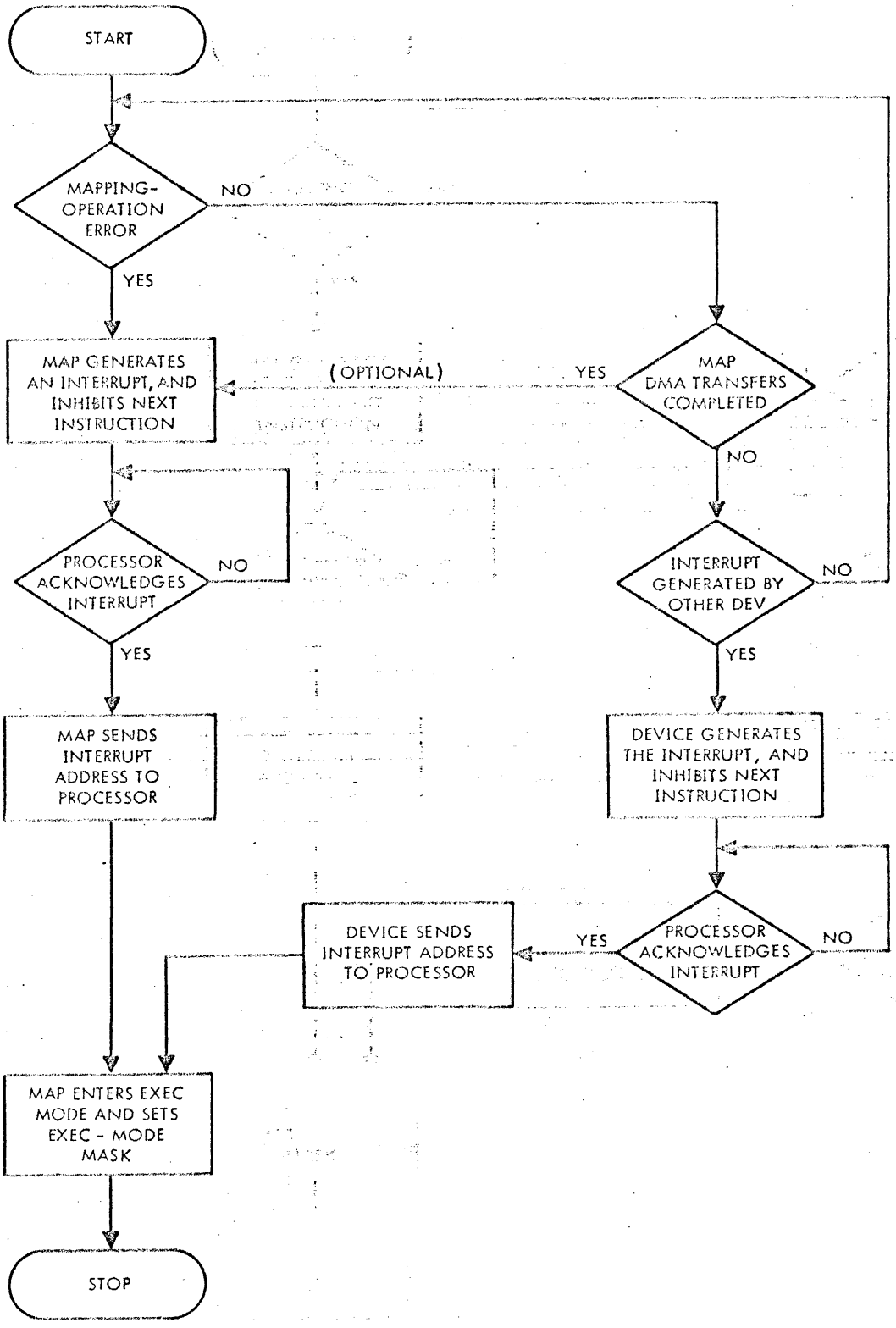
3.4.6 User Mode to Executive Mode

Switching the memory map from the user mode to the executive mode, can be initiated by interrupts resulting from the following:

a. an error during a mapping operation

b. an I/O system interrupt

The sequences of this operation are shown in the flow chart of figure 3-4.



VTII-2048

Figure 3-4. User Mode to Execute Mode Flow Chart

3.5 ACCESS-CONTROL MODES

Four access-control modes for mapping operations are provided by access-control bits 9 and 10 of the RAM-array data word. The four modes with corresponding binary values of bits 9 and 10 are listed in table 3-3.

Table 3-3. Access-Control Modes

Bits 10	Bits 9	Mode	Function
0	0	Unassigned	The logical address is unassigned (non-resident address).
0	1	Full access	All types of access are permitted in this page.
1	0	Read operand only	Only operand fetches are permitted. Instruction fetches from this page will not be executed. This restriction includes execution instructions (XEC, XOF, etc.).
1	1	Read only	Only instruction or operand fetches are permitted in this page (no operand-store operations permitted). The instruction fetches include single- and double-word instructions.

3.6 MEMORY PROTECTION

The memory protection function monitors the address of the instruction being processed on the basis of the access-control mode. When the memory map is active and its memory protection function is enabled, the instruction address register (in the memory map) is updated with each decoded instruction. When an error condition is detected, the memory protection function is disabled, and updating of the instruction-address register is inhibited until the EXC2 0646 instruction is executed. The detection of an error interrupts the program in process and directs it to one of seven preassigned memory addresses. These interrupt addresses are listed in table 3-4. Halt, I/O, and jump errors are detected earlier in the mapping operation to prevent them from being detected at the same time as the other errors.

Table 3-4. Interrupt Addresses

Octal Address	Error
20	Halt. The execution of a halt instruction is attempted.
22	I/O. The execution of an I/O instruction is attempted from a map number other than 0.
24	Write. An attempt is made to write into read-only or read-operand-only locations.
26	Jump. An attempt is made to jump into a read-operand-only location.
30	Unassigned. A read, write, or jump operation is attempted using an unassigned logical address.
32	Instruction fetch. An attempt is made to fetch an instruction from a read-operand-only location.
34	Data transfer. A write or unassigned error is detected during a DMA or PMA data transfer.

3.6.1 Halt Errors

When a halt error is detected, the execution of the halt instruction is allowed to be completed. However, due to the detection of the halt error, the memory map holds the memory-protection interrupt flag true (OINT–) so that the processor reenters the run mode immediately after halting. The processor then goes to an interupt-wait state until the program being processed is directed to the interrupt address 20. Upon completion of the interrupt subroutine the interrupt signal OINT– is reset. A halt error is not detected when the halt is initiated manually using the STEP/RUN switch on the computer control panel.

3.6.2 I/O Errors

When an I/O error is detected, the execution of the I/O instruction is allowed to be completed. However, all I/O control functions and data transfers between the processor and peripheral controllers are inhibited. By holding the I/O-instruction error flag true, the contents of memory and the A, B, and X registers can not be modified by the I/O instruction. When the execution of the I/O instruction is completed, the program being processed is directed to the interrupt address 022.

3.6.3 Writing Errors

When a writing error is detected, the execution of the instruction is allowed to be completed. To prevent memory modification, the writing cycle for memory is changed to a reading cycle. When the execution of the instruction is completed, the program being processed is directed to the interrupt address 024.

Even though the writing error is not detected because the memory protection function is disabled, the active memory map always changes the writing sequence to a reading

sequence if an attempt is made to write into a non full-access location. This protection applies to all DMA, PMA (if connected to memory map), and processor memory cycles.

3.6.4 Jump Errors

A jump error can occur during the following types of instructions:

a. All jump instructions including IJMP, JSR, and BT

b. All jump-and-mark instructions including SRE

A jump error occurs when an attempt is made to jump or skip to a read-operand-only location and if this location is the effective address of the jump or skip instruction.

When a jump error is detected, the execution of the instruction is allowed to be completed. For jump-and-mark instructions, the memory writing cycle is changed to a reading cycle to prevent memory modification. When the execution of the instruction is completed, the program being processed is directed to the interrupt address 026.

3.6.5 Unassigned Errors

When an unassigned error is detected, the execution of the instruction is allowed to be completed. If the memory writing cycle contains the unassigned error, it is changed to a reading cycle. The contents of the A, B, and X registers are not changed. When the execution of the instruction is completed, the program being processed is directed to the interrupt address 030. The unassigned logical address is contained in the memory map's unassigned address register, which can be read by the processor using an input-data transfer I/O instruction (figure 3-2c).

3.6.6 Instruction-Fetch Errors

When an instruction-fetch error is detected, the execution of the current instruction is allowed to be completed. The program being processed is directed to the interrupt address 032, and the next erroneous instruction is not executed.

3.6.7 I/O Data-Transfer Errors

The detection of an I/O data-transfer error during a DMA or PMA operation causes the memory map to generate an interrupt that directs the processor to the interrupt address 034.

When an I/O data-transfer error occurs during a DMA operation, the memory map holds the DMA termination signal (BIMES-I) true. This causes the BIC (or a user-designed controller) to terminate the data transfer on the trailing edge of the data-ready signal (DRYX-I or DRYF-I).

When a data-transfer error occurs during a PMA operation, the memory map holds the PMA termination signal (BTMES-I) true. This causes the block-transfer controller (or a user-designed controller) to terminate the data transfer immediately after receiving the termination signal.

When an I/O data-transfer error occurs, the memory map stores error-status data that include error-key number, writing or unassigned error, and DMA or PMA error. This error-status data (figure 3-2a) can be read by the processor by using an input-data transfer instruction.

When an I/O data-transfer error is detected during a memory-map DMA loading or read-back operation, the memory map generates a DMA error flag (PDMTRM+). In response to the SEN 046 instruction, the memory map provides a DMA not-busy status.

An optional mode of operation, for the detection of an I/O data-transfer error in a DMA loading or read-back operation, consists of using the DMA completion interrupt. When the error is detected, the memory map generates the interrupt directing the processor to the interrupt address 016. The same interrupt is also generated to signal the processor when the loading or read-back operation is successfully completed. Upon receipt of this interrupt, the processor can issue the SEN 0146 instruction to sense if the DMA transfer termination is due to an error.

SECTION 4
THEORY OF OPERATION

4.1 GENERAL

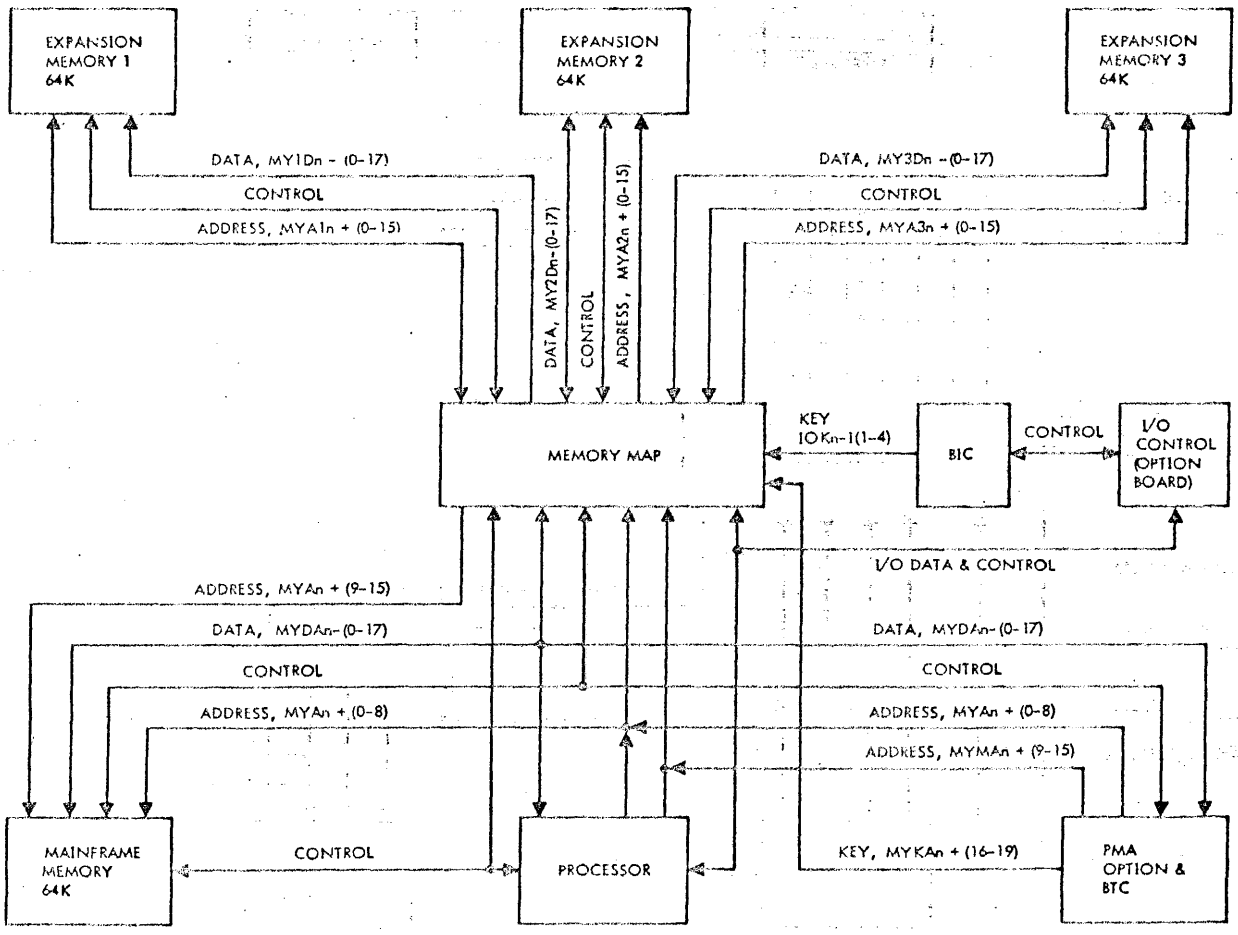
This section contains system and functional descriptions followed by timing waveforms for the various memory-map operations. For ease of reading, some mnemonics are written with the variable n in place of the actual numbers. For example, memory data mnemonics MYDA00- through MYDA17- are written MYDAn-(0-17). Mnemonic descriptions are provided in section 6.

4.2 SYSTEM DESCRIPTION

As illustrated in the system block diagram of figure 4-1, the memory map can be used with either the processor or PMA circuits. Address bits 0 through 8 are applied directly to the mainframe memory, while bits 9 through 15 are routed through the memory map. In addition to the mainframe-memory bus, the memory map provides buses for up to three expansion memories. The BIC provides I/O key bits for DMA memory mapping.

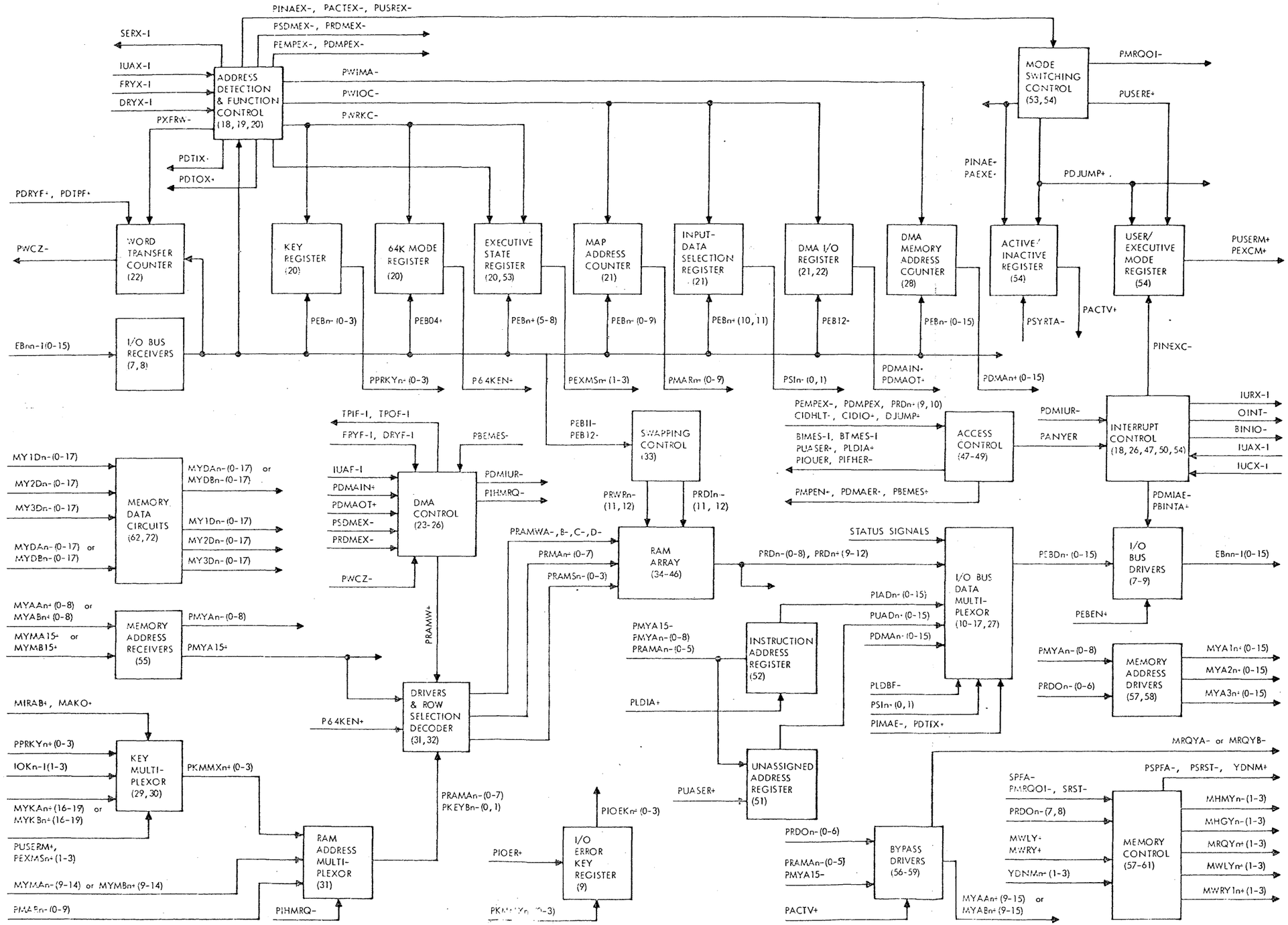
4.3 FUNCTIONAL CIRCUITS

The functional circuits of the memory map are shown in figure 4-2. Page numbers of the memory-map logic diagram (p/n 91C0448 in system documentation package) are provided in parentheses for each circuit block.



VTII-2049

Figure 4-1. Memory-Map System Block Diagram



VT12-4 II

Figure 4-2. Memory-Map Functional Block Diagram

4.3.1 Key Multiplexor

The key multiplexor supplies the 4-bit key PKMMXn + (0-3) to the RAM address multiplexor. The 4-bit key is selected from one of the following sources:

a. Key register, PPRKYn + (0-3)

b. BIC key, IOKn– I(0-3)

c. PMA key, MYKAn + (16-19) or MYKBn + (16-19)

As illustrated in figure 4-3, the key multiplexor contains two multiplexors, a latch, and a buffer. Depending on the jumper configuration, the processor key input of the first multiplexor comes from either the key register PPRKYn + (0-3) (standard for VORTEX II) or the latch PMAKYn + (0-3). PMA key bits are transferred through the latch when the PMA loading signal PLPMAK + is low (this loading signal is low until half-clock time of a memory request). The other input of the first multiplexor is connected directly to the PMA key bits. A high PKYMXE- disables the first multiplexor causing its output bits to be all low (map 0). A low PKYMXE- enables one of the two inputs to be selected. Selection is controlled by PMAKO +. When the processor has accepted a PMA request, a high PMAKO + transfers PMYKn + (16-19) through the first multiplexor. A low PMAKO + selects the other input PRMAKn + (0-3).

Input selection for the second multiplexor is controlled by I/O memory request signal PMIRAB +. A low PMIRAB + transfers the first multiplexor output PKYMXn + (0-3) through the second multiplexor. A high PMIRAB + selects the other input PBICKn + (0-3) from the buffer. BIC key bits IOKn–I(0-3) are transferred through the buffer on the positive-going transition of PKBICK +.

4.3.2 RAM Address Multiplexor

The RAM address multiplexor selects the RAM address consisting of PRAMAn–(0-7) and PKEYBn–(0,1) from either the map-address counter or the combination of key and memory-address bits. Input selection for the multiplexor is controlled by the inhibit-memory-request signal PIHMRQ–. A low PIHMRQ– selects contents of the map-address counter PMARn + (0-9); a high PIHMRQ– selects the key and memory-address bits PKMMX + (0-3) and either MYMAn + (9-14) or MYMBn + (9-14).

4.3.3 Drivers and Row-Selection Decoder

The nine signal lines consisting of PRAMAn–(0-7) and PRAMW + are routed through 36 drivers to provide the power required for driving the RAM arrays.

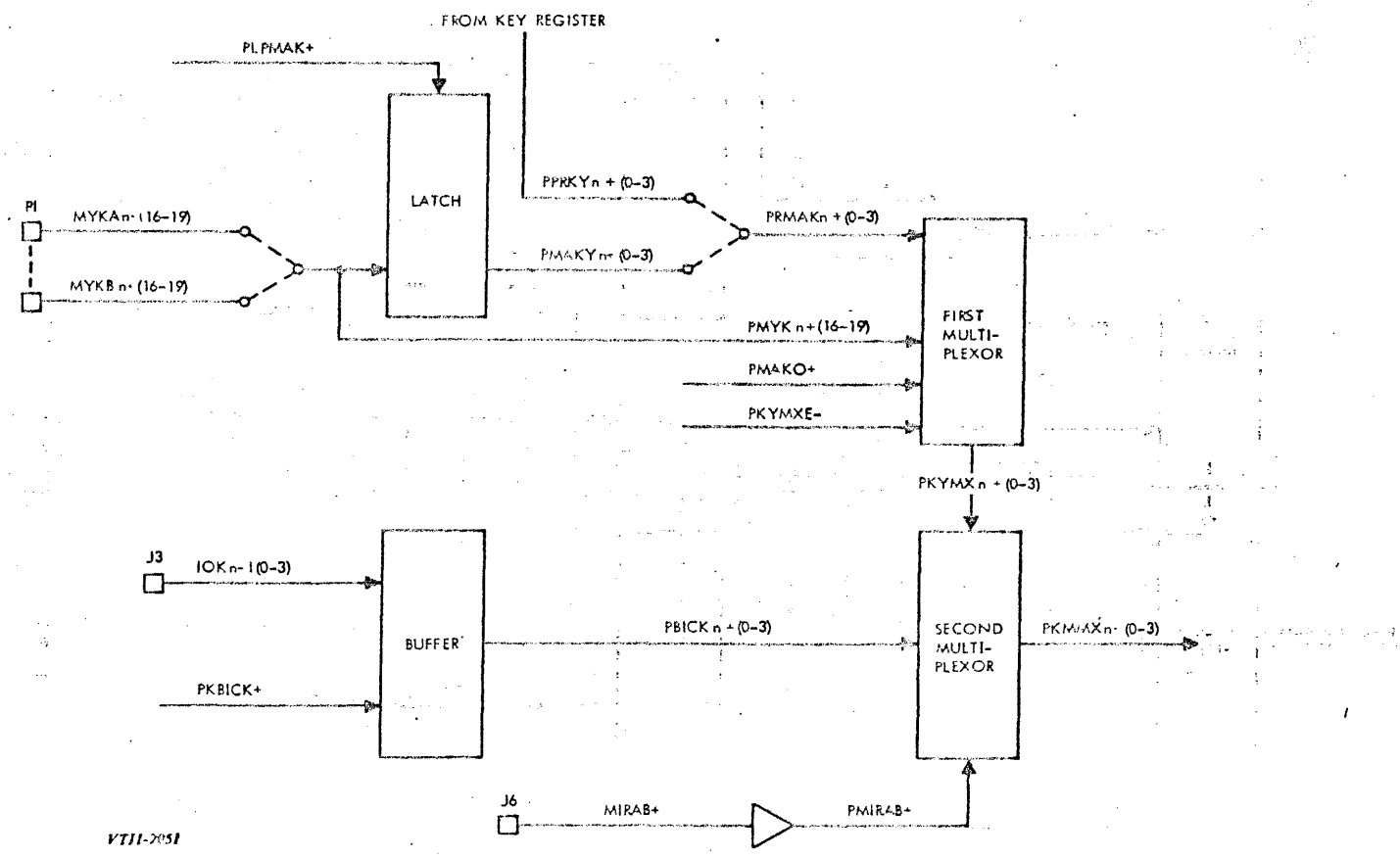


Figure 4-3. Key Multiplexor Block Diagram

The row-selection decoder consists of a selector that selects either PMARn+(6,7) or PKMMXn+(0,1) and a decoder that decodes the selector outputs. The decoded row-selection bits PRAMSn-(0-3) select one of the four rows of the R/M arrays. Table 4-1 is a truth table for the row-selection decoder.

Table 4-1. Row-Selection Decoder Truth Table

INPUTS		ROW-SELECTION OUTPUTS			
PMAR07+ OR PKMMX1+	PMAR06+ OR PKMMX0+	PRAMS3-	PRAMS1-	PRAMS2-	PRAMS0-
L	L	L			
L	H		L		
H	L			L	
H	H				L

NOTE: L = low, H = high

VTII-2079

4.3.4 RAM Array

The RAM array is a 1024-word by 13-bit read/write memory that stores physical page addresses along with access- and swapping-control bits. As illustrated in figure 4-4, it consists of 256-word by 1-bit arrays arranged in 13 columns and 4 rows. Address bits PRMAn-(0-7) (figure 4-5) select one of the 256 13-bit words in all four rows of the array. One of the four rows is selected by the associated row selector PRAMSn- going low.

During a writing operation, a high PRAMW+ enables data from the I/O bus receivers to be loaded into the addressed location of the array. During a reading operation, a low PRAMW+ enables addressed data to be read out of the array.

4.3.5 I/O Bus Data Multiplexor

This multiplexor selects I/O-bus data from one of the following sources:

a. RAM array: PRDOn-(0-8) and PRDOn+(9-12)

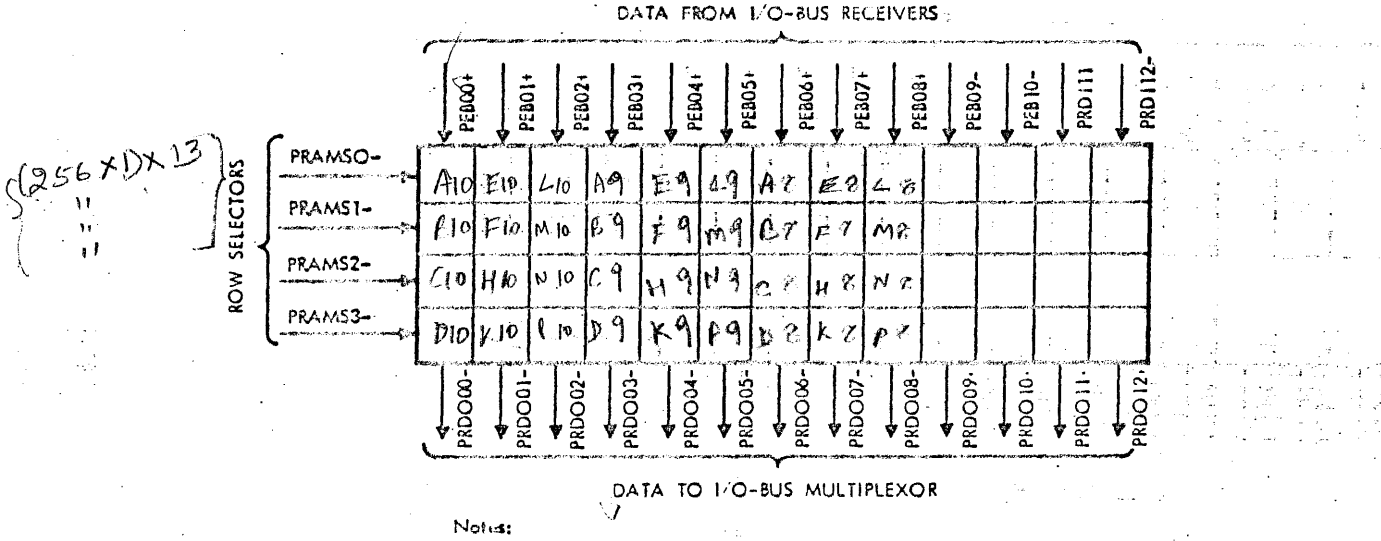
b. Instruction address register: PIADn+(0-15)

c. Unassigned address register: PUADn+(0-15)

d. Status signals: PPRKYn+(0-3), P64KEN+, PEMSnE+(0-3), PDMAOE+, PDMAER+, PIOUER+, PIOEKn+(0-3)

e. DMA memory address register: PDMAn+(0-15)

As illustrated in figure 4-6, the I/O-bus data multiplexor consists of two multiplexors and a buffer. On positive transitions of the buffer-loading signal PLDBF-, RAM-array data are transferred through the buffer to one input of the second multiplexor. Under control of selector signals PSIn+(0,1), the first multiplexor selects data from either the instruction-address register, unassigned- address

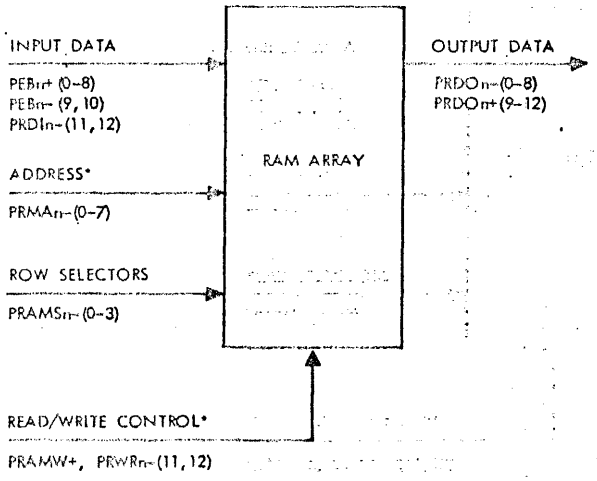


Notes:

1. Each square represents 256 1-bit words.
2. Read/write control PRAMW+ and address bits PRMAn-(0-7) are not shown.

VTII-2052

Figure 4-4. Layout of RAM Array



*Address and read/write control signals are routed through drivers before they are applied to the array.

VTII-2053

Figure 4-5. RAM Array Block Diagram

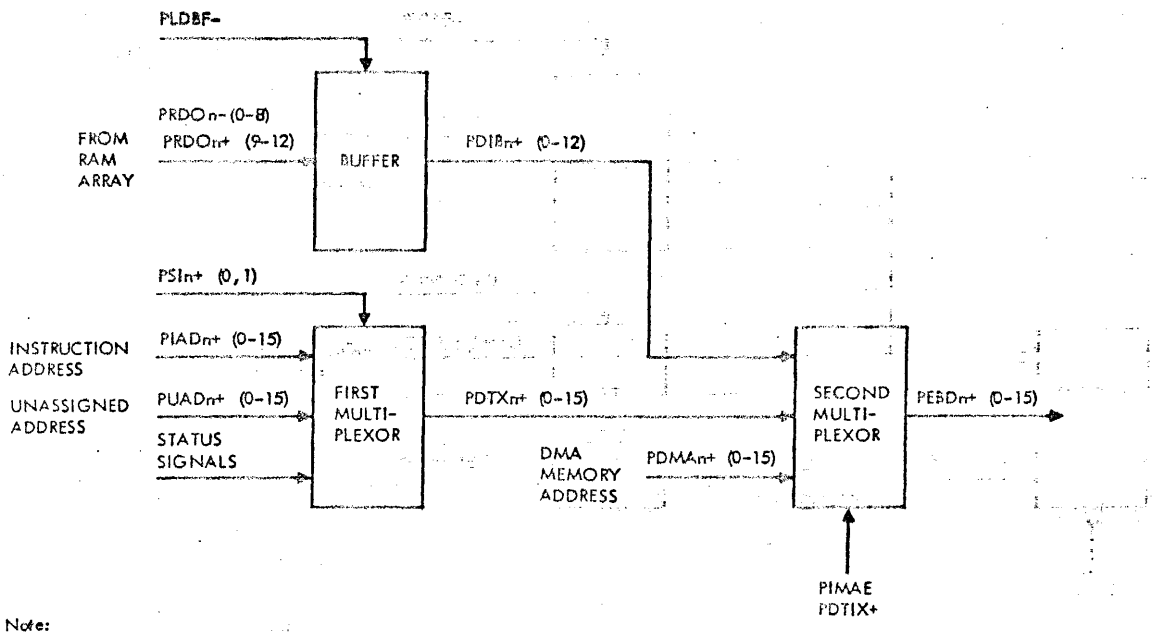
register, or internal-status register. Table 4-2 is a truth table for the first multiplexor. Under control of selector signals PIMAE- and PDTIX+, the second multiplexor selects data from either the buffer, first multiplexor, or DMA memory-address register. Table 4-3 is a truth table for the second multiplexor. Output data PEBDn+(0-15) are applied to the I/O bus drivers.

4.3.6 I/O-Bus Drivers and Receivers

As illustrated in figure 4-7, the I/O-bus drivers transfer either a 16-bit data word EBnn-I(0-15) or a 4-bit interrupt address EBnn-I(1-4) onto the bidirectional I/O bus.

During an input-data transfer, a high PEBEN+ transfers a 16-bit data word through the drivers onto the I/O bus. When an interrupt address is being generated, a low PEBEN+ disables the sixteen drivers causing all of their outputs to go high (all zeros). This allows the four I/O-bus drivers to transfer the interrupt address onto the I/O bus. Table 4-4 lists the bit configurations for the various interrupt address generated by the memory map.

The I/O-bus receivers convert I/O-bus data into PEBn(0-15) for use in various circuits of the memory map.



Note:
Status signals consists of: PPRKYn+(0-3), P64KEN+, PEMSnE+(0-3), PDMAOE+, PDMAER+, PIOUER+, PIOEKn+(0-3).

VTII-2054

Figure 4-6. I/O-Bus Data Multiplexor

Table 4-2. First Multiplexor Truth Table

SELECTORS		DATA INPUTS			OUTPUT
PSI1-	PSI0-	STATUS SIGNALS	PIADn+ (0-15)	PUADn+ (0-15)	PDTXn+ (0-15)
L	L	L			L
L	L	H			H
L	H		L		L
L	H		H		H
H	L			L	L
H	L			H	H
H	H				

NOTE: L = low, H = high, no H or L = irrelevant input

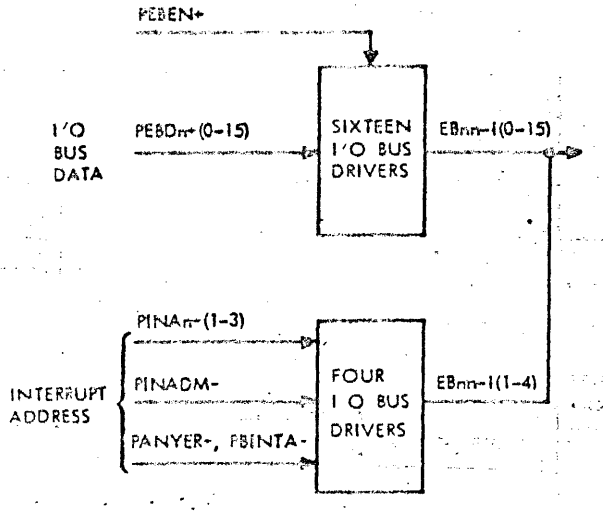
VTII-2682

Table 4-3. Second Multiplexor Truth Table

SELECTORS		DATA INPUTS			OUTPUT
PDTIX+	PIMAE-	PDMADn+ (0-15)	PDIDn+ (0-12)	PDTXn+ (0-15)	PEBDn+(0-15)
L	L	L			L
L	L	H			H
L	H		L		L
L	H		H		H
H	L			L	H
H	H			H	L
H	H				H

NOTE: L = low, H = high, no H or L = irrelevant input

VTII-2683



VTII-2655

Figure 4-7. I/O Bus Drivers

Table 4-4. Interrupt-Address Bit Configurations

I/O-Bus Bits EBn-1(1-4)				Interrupt Address (Octal)
4	3	2	1	
H	L	L	L	16
L	H	H	H	20
L	H	H	L	22
L	H	L	H	24
L	H	L	L	26
L	L	H	H	30
L	L	H	L	32
L	L	L	H	34

Note: L = low, H = high

4.3.7 Word-Transfer Counter

The word-transfer counter counts the number of words transferred during map loading and read-back operations. An 11-bit data word PEBn + (0-10), representing the number of words to be transferred, is loaded into the counter when PXFRW- is low. With each subsequent word-transfer, PDRYF + and PDTPF + go high causing the contents of the counter to decrease by one. When all words have been transferred, the output of the counter PWCZ- goes low. The low PWCZ- is sent to DMA control to indicate completion of the DMA transfers.

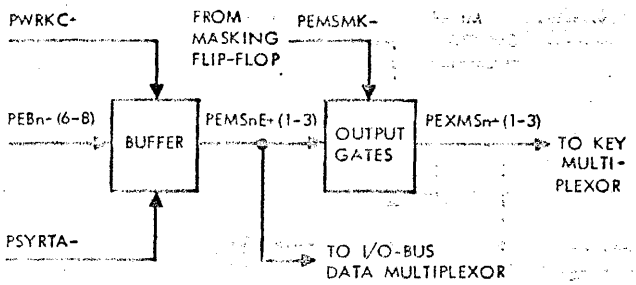
4.3.8 Key and 64K-Mode Registers

On the positive-going transition of the write-key control PWRKC +, PEBn + (0-3) and PEBO4 + are clocked into the key and 64K-mode registers, respectively. The 4-bit output of the key register PPRKYn + (0-3) is sent to the key multiplexor and to the I/O-bus data multiplexor as part of the status-signal input. The output bit of the 64K-mode register P64KEN + is also sent to the I/O-bus data multiplexor as part of the status-signal input. A high P64KEN + enables the 64K mode of operation. When P64KEN + is low, the 32K mode is used.

4.3.9 Executive-State Register

This register (figure 4-8) stores one of the four states of the executive mode. On positive-going transitions of the write-key control PWRKC+, PEBn+(6-8) are clocked into the executive-state buffer. This buffer is cleared with a low system reset PSYRTA-. Buffer-output bits PEMSnE+(1-3) are applied to the I/O-bus data multiplexor as well as the executive-state output gates. When the executive-state masking flip-flop is reset, a high PEMSMK- transfers the buffer-output bits through the output gates to the key multiplexor. Resetting of the flip-flop occurs during either the inactive mode of operation (PACTV+ low) or the decoding of an external control EXC2 0546) I/O instruction.

When an interrupt occurs, the executive-state masking flip-flop is set (PEMSMK- low) causing all bits of PEXMSn+(1-3) to go low. This results in executive-mode state 0 operation (executive map).



OUTPUT-BIT CONFIGURATION

PEXMSn- BITS 3	2	1	EXECUTIVE-MODE STATES
L	L	L	0
L	L	H	1
L	H	L	2
H	L	L	3

Note: L = low, H = high

VTII-2056

Figure 4-8. Executive-State Register Block Diagram

4.3.10 Map-Address Counter

When the I/O-write control PWIOC- is low, the initial map address PEBn+(0-9) is loaded into the counter and applied to the RAM address multiplexor. With each subsequent address-transfer, the content of the counter PMARn+(0-9) is increased by one with the positive-going transition of PIHMRQ-. After the loading of the initial map address, the counter can count up to 1023 before resetting to zero.

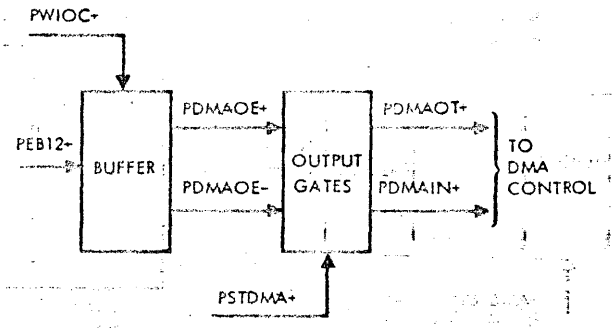
4.3.11 Input-Data Selection Register

On the positive-going transition of the I/O-write control PWIOC+, I/O data bits PEBn+(10,11) are clocked into the input-data selection register. The register contents PSIn+(0,1) are used to select one of three data inputs for the I/O-bus data multiplexor. Bit configurations for data-input selection are listed in the following table (L is low, H is high):

PSI1+	PSI0+	Selected Input Data
L	L	Status signals
L	H	Instruction address
H	L	Unassigned address

4.3.12 DMA I/O Register

On the positive-going transition of the I/O-write control PWIOC+, the I/O data bit PEB12+ is clocked into the DMA I/O register (figure 4-9). A low PEB12+ enables a DMA input transfer (PDMAOE- high); a high PEB12+ enables a DMA output transfer (PDMAOE+ high). When the start-DMA-transfer I/O instruction (EXC2 0346) is decoded, a high DMA start signal PSTDMA+ transfers the DMA input or output signal (PDMAIN+ or PDMAOT+) through the output gates to the DMA control circuits. When the DMA-reset instruction (EXC2 0446) is decoded, the output gates are disabled with a low PSTDMA+.



VTII-2057

Figure 4-9. DMA I/O Register

4.3.13 DMA Memory-Address Counter

The DMA memory-address counter provides memory addresses for the processor during the address phase of map loading and read-back operations. When the loading signal PWIMA- goes low, the initial memory address PEBn+(0-15) is loaded into the counter and is then applied to the I/O-bus data multiplexor. With each subsequent address-transfer, the counter content PDMAn+(0-15) is increased by one with the positive-going transition of PIMAE-. After the loading of the initial map address, the counter can count up to 65,535 before resetting to zero.

4.3.14 I/O-Error Key Register

When an error is detected during a DMA or PMA operation, the positive-going transition of PIOER+ clocks the error-key number PKMMXn+(0-3) into the I/O-error key register. The register contents PIOEKn+(0-3) are applied to the I/O-bus data multiplexor as part of the status-signal input.

4.3.15 Instruction Address Register

During preliminary decoding of each instruction, the instruction address register stores data from the processor's program counter. The register is updated with each instruction until an error is detected. Further updating is inhibited until the map's memory protection logic is enabled. During the error subroutine, the register contents are transferred to the processor by an input-data transfer instruction. The register contents equal P+1 where P is the logical address of the instruction that failed.

The inputs to the instruction address register PRAMAn−(0-5) and PMYAn−(0-8,15) come from the RAM address multiplexor and memory address receivers, respectively. On the positive-going transition of PLDIA+, these inputs are clocked into the register. During the time that the processor is performing preliminary instruction decoding (PCACID+ high) and the map's memory protection logic is enabled (PMPEN+ high), PLDIA+ goes high on the positive-going transition of the processor full clock PMFC+. The register contents PIADn+(0-15) are applied to the I/O-bus data multiplexor. The instruction address is transferred to the processor by an input-data transfer instruction.

4.3.16 Unassigned Address Register

The same inputs that are applied to the instruction address register are also applied to the unassigned address register. When an unassigned address is detected, it is loaded into the unassigned address register on the positive-going transition of PUASER+. Clock signal PUASER+ is generated when output data bits 9 and 10 of the RAM array are both false, and the map's memory protection logic is enabled (PMPEN+ high). The register contents PUADn+(0-15) are applied to the I/O-bus data multiplexor. The unassigned address is transferred to the processor by an input-data transfer instruction.

4.3.17 Swapping Control

Two swapping control bits are used by the memory map: change bit PDRI11-) and usage bit (PRDI12-). The change bit indicates if a page has been written into since the bit was last reset. The usage bit indicates if a page has been accessed since the bit was last reset. To facilitate scanning and counting the frequency of use, this bit is hardware reset whenever the processor reads the RAM array.

The swapping control circuit controls the setting and resetting of the swapping control bits and applies them to the RAM array.

During a map loading or read-back operation, a high PIHMRQ+ enables the state of PRDI11− to be the same as PEB11−. During a mapping operation, a low PIHMRQ+ causes PRDI11− to remain low regardless of the state of PEB11−.

During memory map loading (PDMAOT+ and PIHMRQ+ high), the state of PRDI12− is the inverse of PEB12+. If PDMAOT+ or PIHMRQ+ is low, the state of PEB12+ has no effect on PRDI12−.

4.3.18 Access Control

Access control bits PRDOn+(9,10) are decoded to produce control signals for the four access control modes:

a. Unassigned mode (PUNASG− low) indicates that the logical address is unassigned.

b. Full-access mode (PFULAC− low) indicates that both reading and writing operations are permitted.

c. Read-operand-only mode (PROPRD− low) indicates that only operand fetches are permitted. Instruction fetches from pages having this read-operand-only condition will not be executed.

d. Read-only mode (PRDO9+ and PRDO10+ high) indicates that only instruction or operand fetches are permitted. Instruction fetches include both words of any double-word instruction as well as single-word instructions.

Table 4-5 is the decoder truth table.

Table 4-5. Access-Control Decoder Truth Table.

Inputs		Outputs		
PRDO10+	PRDO09+	PUNASG−	PFULAC−	PROPRD−
L	L	L	H	H
L	H	H	L	H
H	L	H	H	L
H	H	H	H	H

Note: L = low, H = high

4.3.19 Memory Address Drivers and Receivers

Seven bits from the RAM array PRDOn– (0-6) and nine bits from the memory address receivers PMYAn– (0-8) are applied to the memory address drivers. The driver outputs MYA1n + (0-15), MYA2n + (0-15), and MYA3n + (0-15) are routed to the expansion memories.

Memory address bits 0 through 8 and bit 15 from either port A or B are applied to the memory address receivers. Receiver outputs are PMYAn– (0-8,15).

4.3.20 Active/Inactive Register

This register provides active and inactive status of the memory map. In the executive mode, the register is set (PACTV + high) indicating an active status. The register is set by the decoding of I/O instruction EXC2 0146 (PAEXE + high) and a jump instruction (PDJUMP + high).

In the inactive mode, the register is reset (PACTV– high) indicating the inactive status. The register is reset by either a system reset (PSYRTA– low) or by the decoding of I/O instruction EXC2 046 (PINAE + high) and a jump instruction (PDJUMP + high).

4.3.21 User/Executive Mode Register

This register provides control signals that indicate user- and executive-mode conditions. In the user mode, the register is set by the decoding of I/O instruction EXC2 0246 (PUSRE + high) and a jump instruction (PDJUMP + high). The register output (PUSER + high) is then gated with a high PACTV + to produce the user-mode control (PUSERM + high).

In the executive mode, the register is reset by the decoding of I/O instruction EXC2 0146 (PAEXE + high) and a jump instruction (PDJUMP + high). The register output (PUSER– high) is then gated with a high PACTV + to produce the executive-mode control (PEXCM + high).

4.3.22 Bypass Drivers

When the memory map is in the inactive mode (PACTV– high), address bits PRAMAn– (0-5) and PMYA15– bypass the RAM array and are transferred to memory port A or B. In addition, the high PACTV– transfers memory request MRQYA– or MRQYB– to the mainframe memory.

When the memory map is active (PACTV + high), data PRDOn– (0-6) from the RAM array are transferred to memory port A or B.

4.3.23 Memory-Data Circuits

The memory data circuits consist of a multiplexor to select data from expansion memories, an input buffer to buffer the multiplexor output, and drivers and receivers to drive and receive memory data. Figure 4-10 shows the data paths through the memory map between the processor and expansion memories for reading and writing operations.

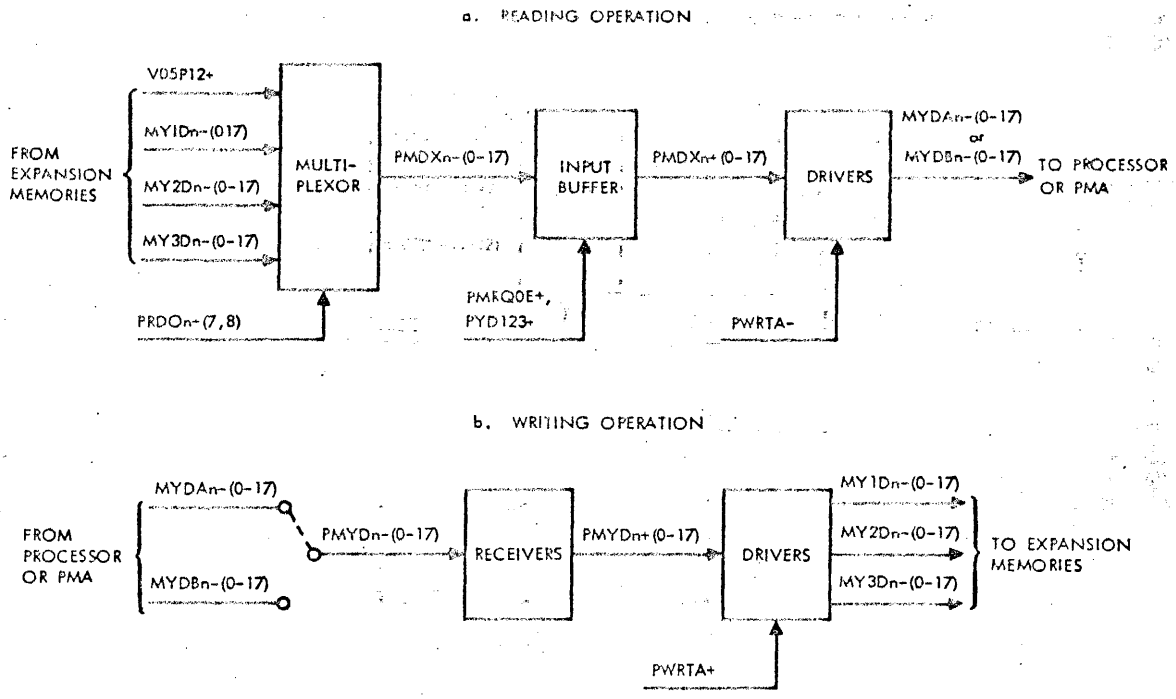


Figure 4-10. Memory-Data Paths Between Processor and Expansion Memories

During a reading operation (figure 4-10a), data from the expansion-chassis memories are applied to the multiplexor. Data selection is controlled by PRDO7+ and PRDO8+ from the RAM array (refer to table 4-6 for truth table). When data from the mainframe memory are read, both PRDO7+ and PRDO8+ are low causing no data to be transferred through the multiplexor. When enabled by either mainframe memory request (PMRQOE+ high) or a memory acknowledgment from expansion chassis 1, 2, or 3 (PYD123+ high), the input buffer inverts the multiplexor output PMDXn-(0-17) and applies it to the drivers. A high PWRTA- causes the drivers to invert the buffer output PMDXn+(0-17) and transfer it onto the memory bus. If data from the mainframe memory are read, all driver output bits are high. This occurs because mainframe memory data are transferred to the processor without going through the memory map.

Table 4-6. Memory-Data Multiplexor Truth Table

Selectors		Data Inputs				Output
PRDO8+	PRDO7+	V05P12+	MY1Dn- (0-17)	MY2Dn- (0-17)	MY3Dn- (0-17)	PMDXn- (0-17)
L	L	H				H
L	H		L			L
L	H		H			H
H	L			L		L
H	L			H		H
H	H				L	L
H	H				H	H

Notes: 1. L = low, H = high, no H or L = irrelevant input
2. V05P12+ is a constant high voltage level

During a writing operation (figure 4-10b), memory data from memory port A or B are applied to receivers. The receivers invert the data and apply them to drivers. A high PWRTA+ causes the drivers to invert the receiver output PMYDn+(0-17) and transfer it onto the three expansion memory buses. The memory request MRQY1+, MRQY2+, or MRQY3+ generated by the memory control circuit determines which expansion memory accepts the memory data.

4.3.24 Address Detection and Function Control

Address signal PADR46+ goes high when address 046 is decoded (or alternate address 056) from bits PEBn(0-5) and there are no DMA or interrupt requests (IIUAX-I high). An external control (EXC2) instruction is decoded when PEB15+ is high and PADR46+ is gated with the function ready control FRYX-I (PFRY46+ high). As illustrated in table 4-7, specific EXC2 instructions are executed by decoding the function code bits PEBn+(6,7,8). The decoded outputs correspond to the various EXC2 instructions and are described as follows:

a. PINAEX- places memory map in the inactive mode (EXC2 046).

Table 4-7. EXC2 Decoder Truth Table

INPUTS			OUTPUTS							
PEB08-	PEB07-	PEB06-	PINAEX-	PACTEX-	PUSREX-	PSDMEX-	PRDMEX-	PCLMEX-	PEMPEX-	PDMPEX-
L	L	L	L							
L	L	H		L						
L	H	L			L					
L	H	H				L				
H	L	L					L			
H	L	H						L		
H	H	L							L	
H	H	H								L

Notes:
1. L = low, H = high
2. For clarity, only the low or true states of the outputs are included in the table.

VTII-2081

b. PACTEX- switches memory map from inactive mode to executive mode (EXC2 0146).

c. PUSREX- switches memory map from executive mode to user mode (EXC2 0246).

d. PSDMEX- starts a memory-map DMA transfer (EXC2 0346).

e. PRDMEX- resets the memory map's DMA-transfer logic (EXC2 0446).

f. PCLMEX- removes the executive-mode mask (EXC2 0546).

g. PEMPEX- enables the memory protection function and instruction address updating (EXC2 0646).

h. PDMPEX- disables the memory protection function and instruction address updating (EXC2 0746).

Function code bits PEBn+(6,7,8) are also decoded for sense (SEN) instructions (PEB12+ high). Table 4-8 lists the function codes for the SEN instructions. If the condition sensed by the instruction is true, a sense response (SERX-I low) is sent to the processor.

Table 4-8. Function Codes for SEN Instructions

PEB08+	PEB07+	PEB06+	Instruction
L	L	L	SEN 046 (SEN0+ high)
L	L	H	SEN 0147 (SEN1+ high)

Note: L = low, H = high

Execution of input- and output-data transfer instructions consists of an instruction phase and a data phase. A high PEB13+ indicates an input-data transfer and high PEB14+ indicates an output-data transfer. When gated with a high PFRY46+, these signals start the instruction phase by setting the input- or output-transfer flip-flop (PDTIX+ or PDTOX+ high). The data phase is initiated when a low data-ready signal DRYX- resets the input- or output-transfer flip-flop. Control signals for the three

formats of output-data transfers are decoded from PEB14+ and PEB15+ (table 4-9). The control signals are:

a. PWRKC−, write key control

b. PWIOC−, write I/O control

c. PXFRW−, write number of words to be transferred via DMA

Table 4-9. Output-Transfer Format Truth Table

Inputs		Outputs		
PEB15+	PEB14+	PWRKC−	PWIOC−	PXFRW−
L	L	H	H	H
L	H	L	H	H
H	L	H	L	H
H	H	H	H	L

Note: L = low, H = high

4.3.25 Memory Control

By decoding output bits 7 and 8 of the RAM array with various other control signals, the memory control applies one of the memory request signals MRQYA−, MRQYB−, or MRQYn+(1-3) onto the appropriate memory bus (mainframe or an expansion memory).

In addition, the memory control provides the following control signals:

a. Read/write control signals for left and right memory bytes are applied to selected memory bus.

b. System reset (SRST−) and power-failure reset (SPFA−) signals are applied to the selected memory bus.

c. Memory lockout signals MHGYn−(1-3) or MHMYn−(1-3) are applied to the selected expansion-memory bus.

d. The expansion-memory acknowledgement signals YDNMn+(1-3) are delayed 30 nanoseconds and is transferred to the mainframe memory (YDNMA+ or YDNMB+). The delay ensures that data on the mainframe memory bus has stabilized.

4.3.26 DMA Control

The DMA control controls the memory-map loading and read-back operations. The following events occur during the loading operation (for timing waveforms see figure 4-14):

a. The processor executes the EXC2 0346 instruction to start the memory-map DMA transfer.

b. The memory map generates a trap-out request (TPOF− low).

c. The processor transfers the address to the memory and the data to the memory map via the I/O bus.

d. The memory map generates a write strobe (PRAMW+ high) to load the data into the RAM array.

The following events occur during the read-back operation (for timing waveforms refer to figure 4-15):

a. The processor executes the EXC2 0346 instruction to start the memory-map DMA transfer.

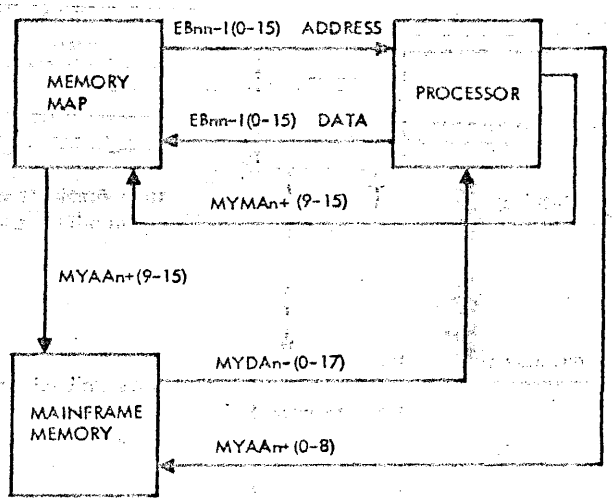
b. The memory map loads read-back data PRDOn(0-12) into buffer PDIBn+(0-12).

c. The memory map resets the usage bit (PRDI12−).

d. The memory map generates a trap-in request (TPIF− low).

e. When the processor acknowledges the trap-in request, the memory map places the read-back data onto the I/O bus for transferal to the processor.

The data flow for the map loading operation with port A of the mainframe memory is shown in figure 4-11. The data flow begins with the memory map sending a logical address EBnn-I(0-15) to the processor via the I/O bus (this occurs during the PFRYF+ phase of the DMA transfer). The processor sends the address to the mainframe memory mapped or unmapped depending on whether the memory map is active or inactive. Data contained at this physical address are then transferred to the processor as MPDAn-(0-17). To complete the loading operation, the processor then loads the data into the memory map via the I/O bus.



VTII-2059

Figure 4-11. Data Flow for Map Loading Operation

The data flow for the map read-back operation with port A of the mainframe memory is shown in figure 4-12. As in the loading operation, the data flow begins with the memory map sending a logical address EBnn-I(0-15) to the processor via the I/O bus (during the PFRYF+ phase of the DMA transfer). During the PDRYF+ phase, the memory map transfers RAM-array data onto the I/O bus and the processor transfers this data to the memory data bus. As in the loading operation, the processor applies the memory address to the mainframe memory and memory map. Data on the memory data bus are then written into the mapped physical address, thus completing the read-back operation.

Timing waveforms for the memory-map loading and read-back operations are shown in figures 4-14 and 4-15.

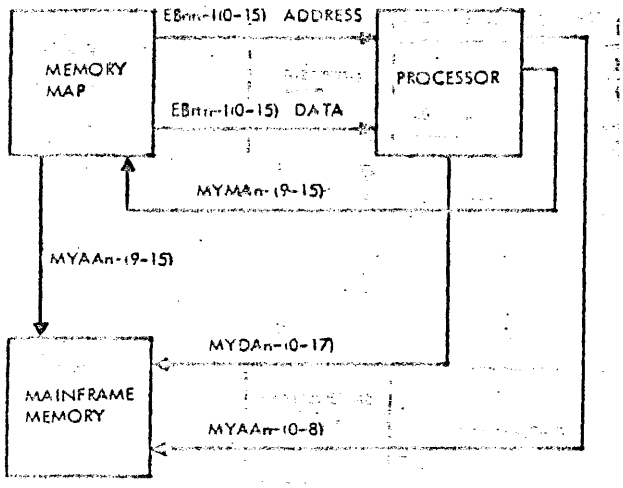


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Figure 4-12. Data Flow for Map Read-Back Operation

4.3.27 Mode Switching Control

This section controls switching of the memory-map modes of operation. As described in section 3.4, the modes of operation can be switched as follows:

a. Executive mode to inactive mode

b. Inactive mode to executive mode

c. Executive mode to user mode

d. User mode to executive mode

Timing waveforms for the mode switching operations are shown in figures 4-24 through 4-27.

4.3.28 Interrupt Control

This section provides interrupt control signals for the memory-protection and DMA-completion interrupts.

The following events occur with a memory-protection interrupt (for timing waveforms see figure 4-23):

a. The memory map detects an error (PANYER+ high).

b. The memory map synchronizes with the interrupt clock (PIUCX+), and raises an interrupt request (PBINTE+ high) which in turn sets the I/O bus interrupt request (IURX-I low).

c. Upon receipt of the interrupt acknowledgment (IUAX-I low), the memory map places the interrupt address on the I/O bus until the trailing edge of PFRYX+.

d. On the negative-going transition of PIUCX+, the memory map resets the interrupt request (IURX-I high).

The following events occur with a DMA-completion interrupt (for timing waveforms see figure 4-16):

a. A DMA transfer operation is complete when either the word-transfer counter is set to zero (PWCZ- low) or an error termination is detected (PDMTRM+ high).

b. The memory map synchronizes with the interrupt clock (PIUCX+) and sets an interrupt request (PIURF+ high) which in turn sets the I/O bus interrupt request (IURX-I low).

c. From this point on, the operation is the same as in steps c and d of the memory-protection interrupt.

4.4 MEMORY MAP TIMING

This section provides timing waveforms for the various memory-map operations. The operations with their figure numbers are listed below:

Figure 4-13, Programmed I/O Data Transfer

Figure 4-14, Memory-Map Loading via High-Speed DMA

Figure 4-15, Memory-Map Read-Back via High-Speed DMA

Figure 4-16, Memory-Map Loading/Read-Back Termination

Figure 4-17, Memory Mapping

Figure 4-18, I/O and Halt Error Detection

Figure 4-19, Jump-Error Detection

Figure 4-20, Unassigned and Writing Error Detection

Figure 4-21, Instruction-Fetch Error Detection

Figure 4-22, I/O Data-Transfer Error Detection

Figure 4-23, Memory Protection Interrupt

Figure 4-24, Executive-Mode to Inactive-Mode Switching

Figure 4-25, Inactive-Mode to Executive-Mode Switching

Figure 4-26, Executive-Mode to User-Mode Switching

Figure 4-27, User-Mode to Executive-Mode Switching

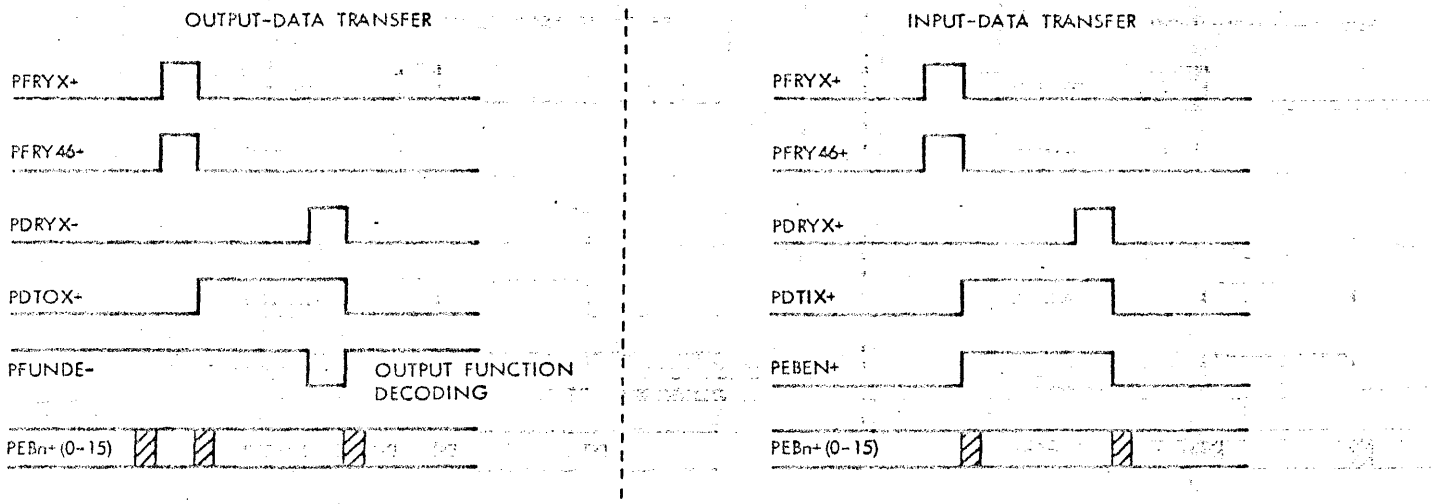

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Figure 4-13. Programmed I/O Data Transfer

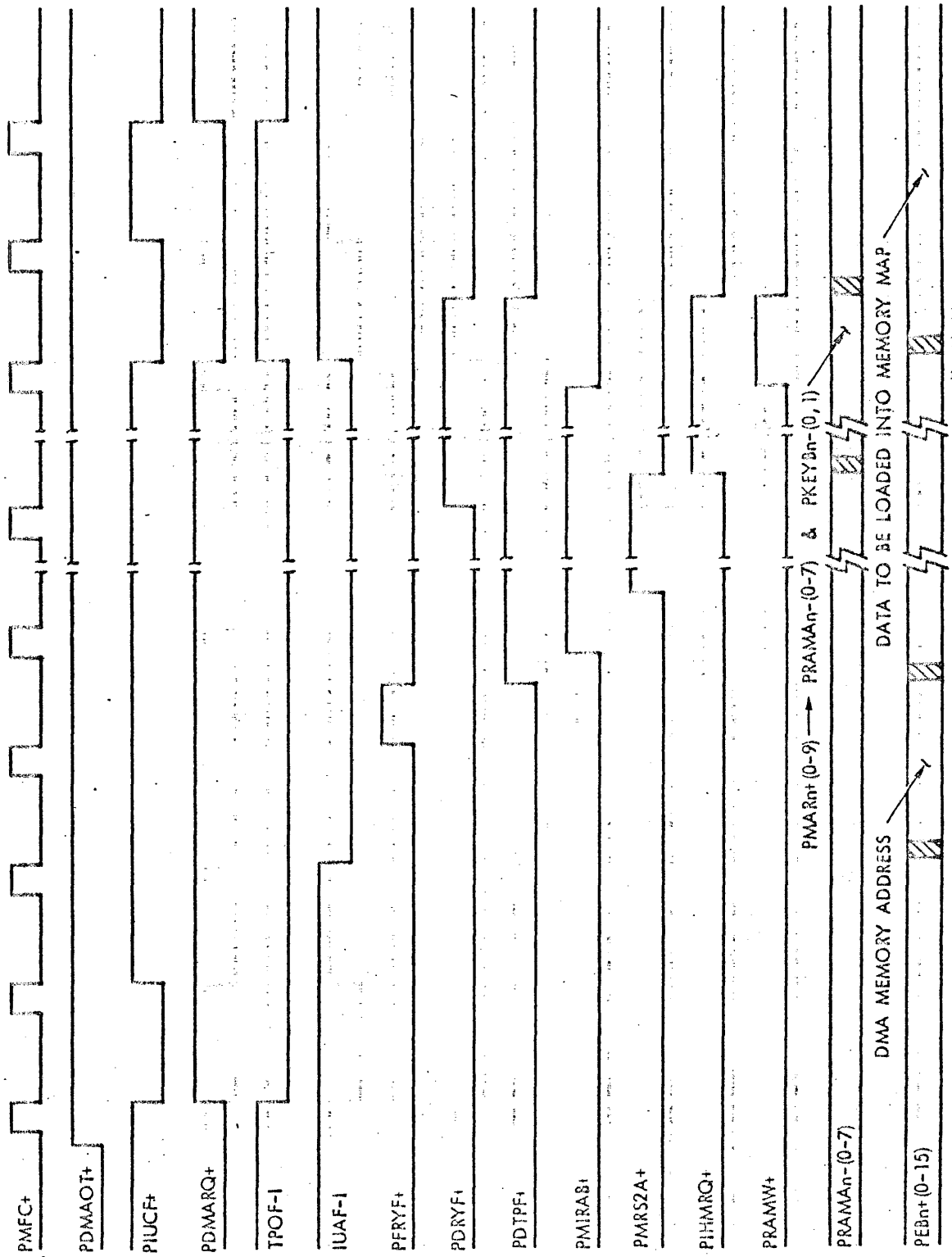

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Figure 4-14. Memory-Map Loading via High-Speed DMA

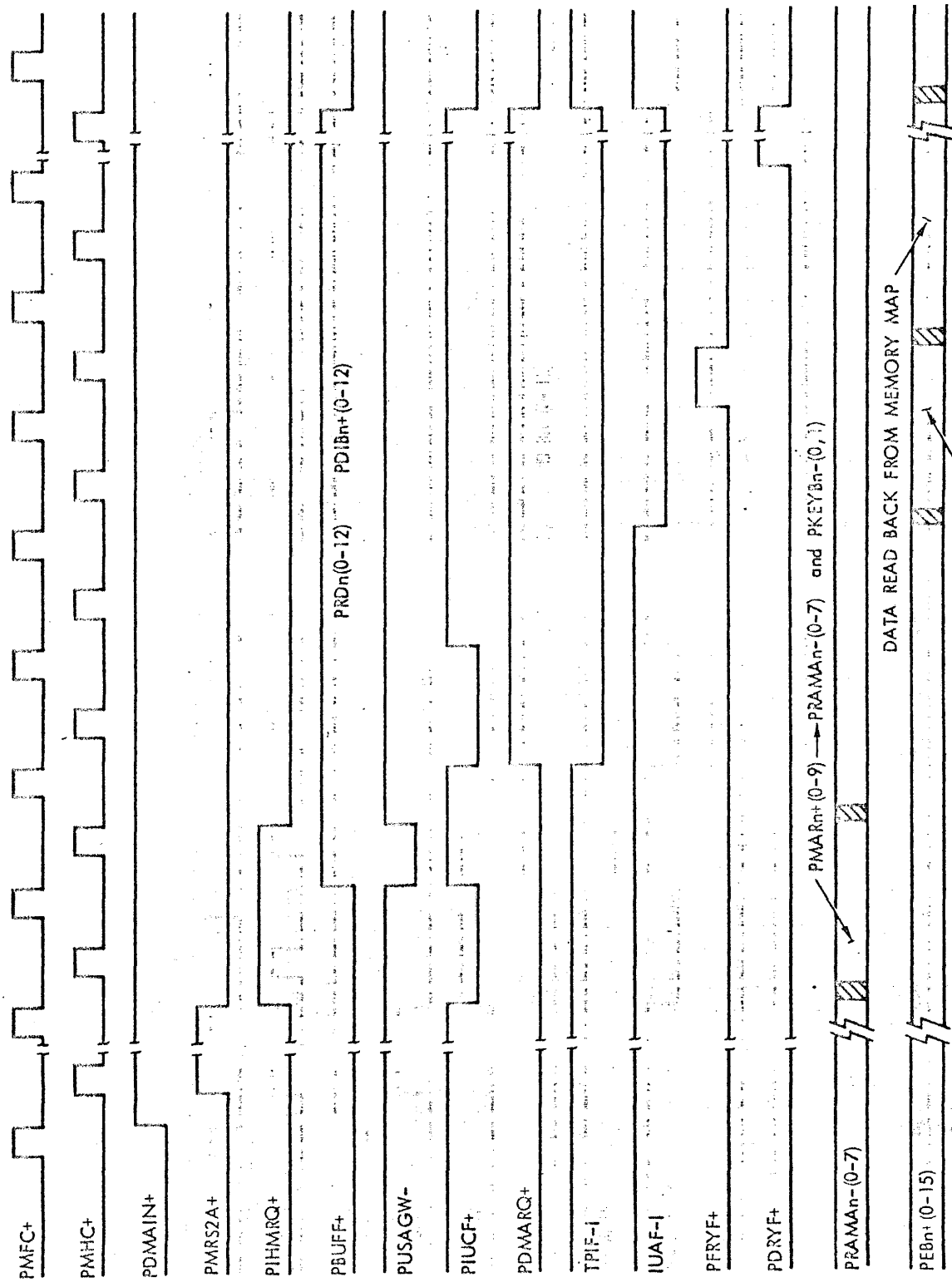

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Figure 4-15. Memory-Map Read-Back via High-Speed DMA

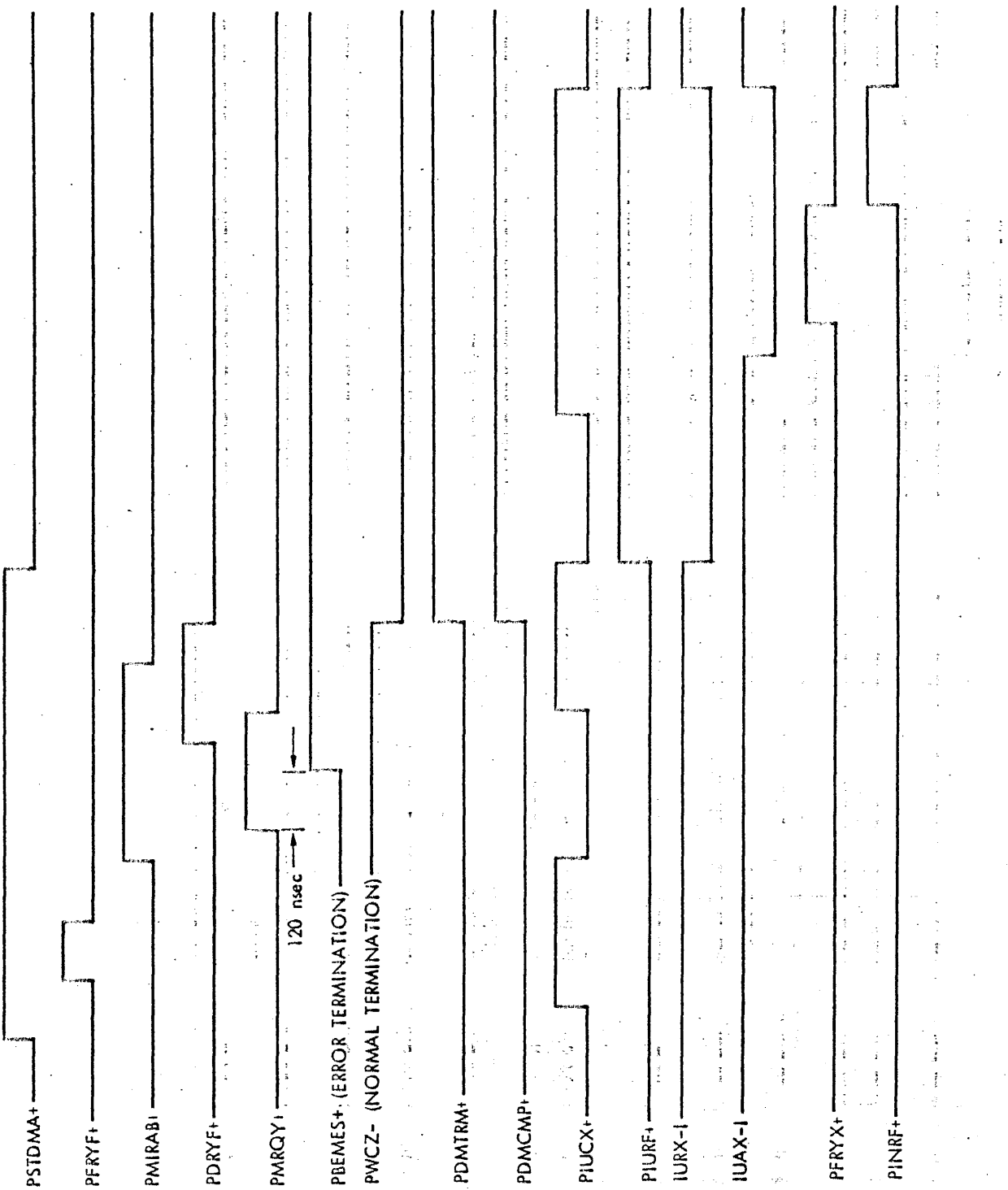

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Figure 4-16. Memory Map Loading/Read-Back Termination

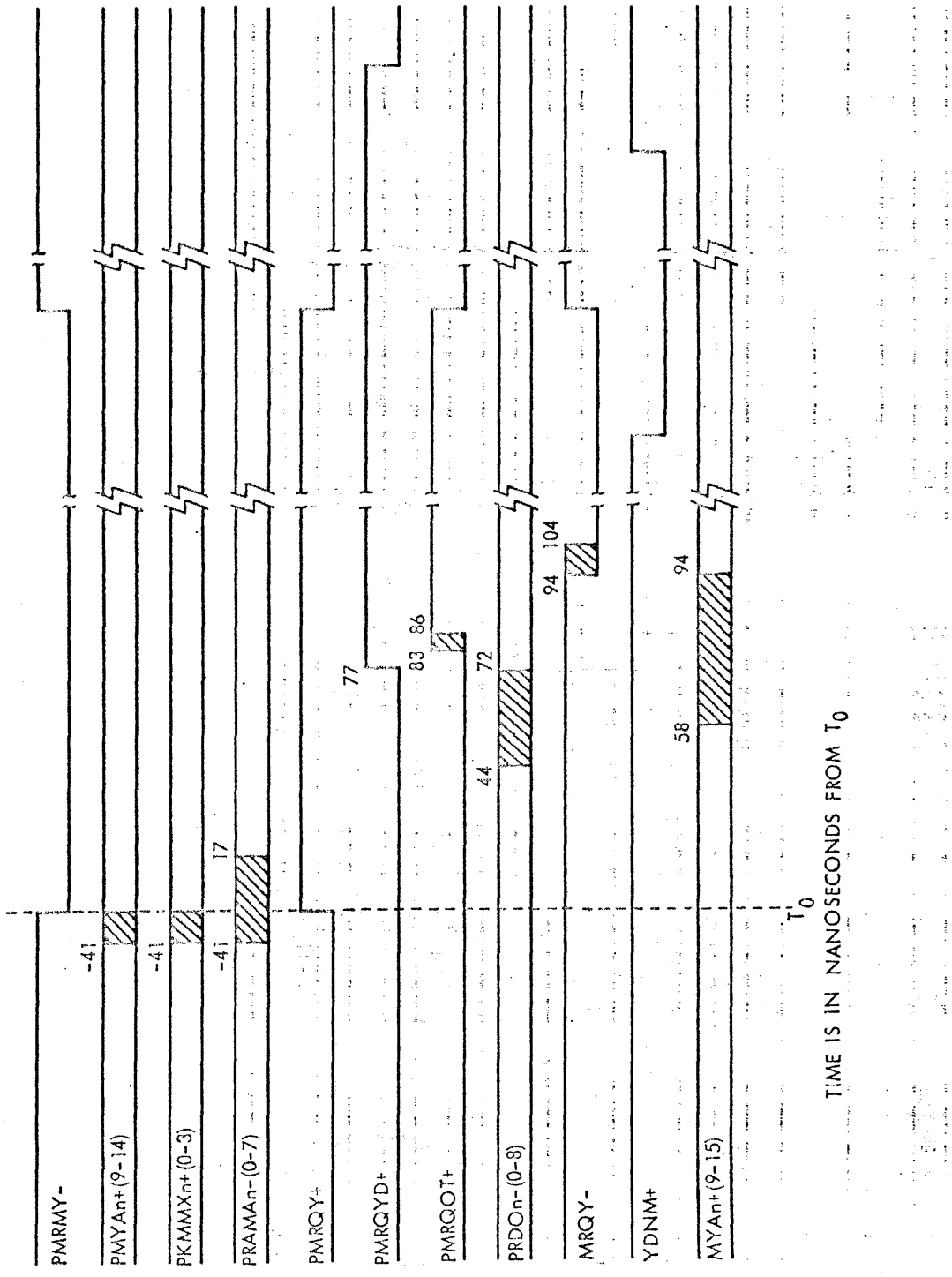

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Figure 4-17. Memory Mapping

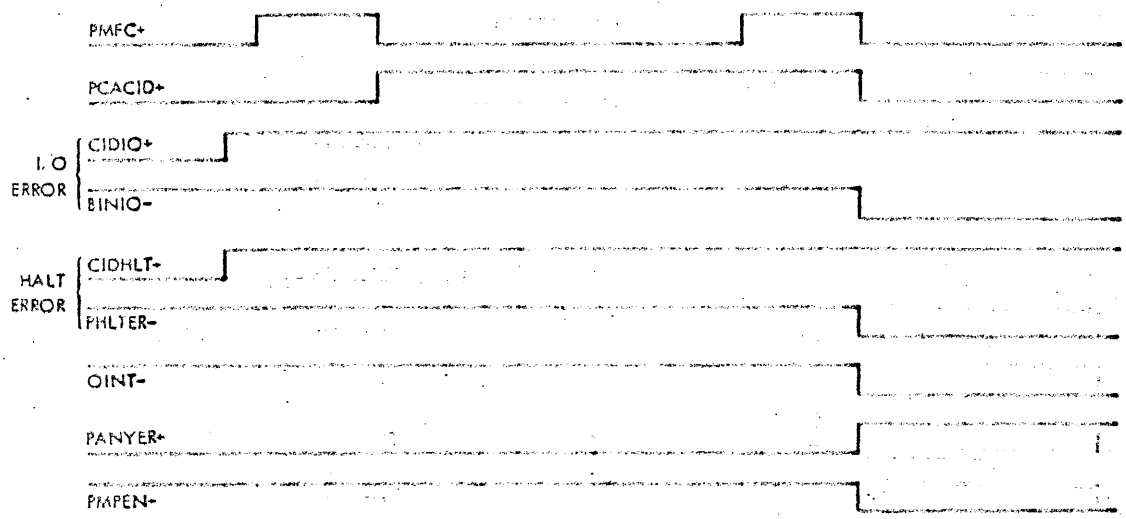

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Figure 4-18. I/O and Halt Error Detection

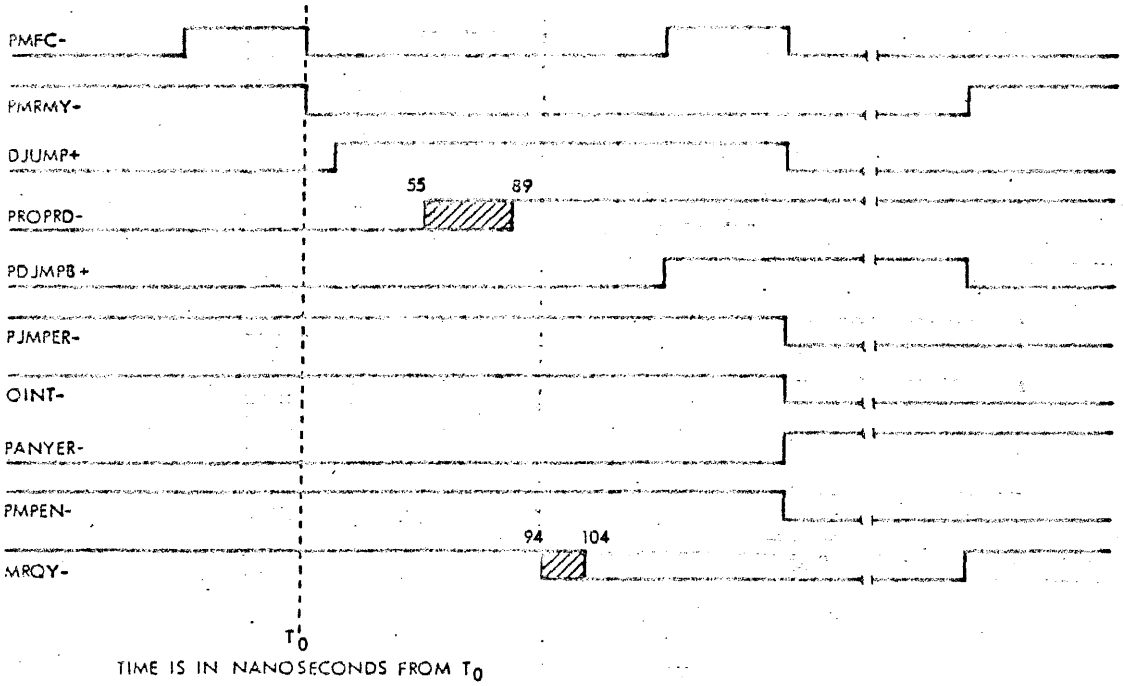

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Figure 4-19. Jump-Error Detection

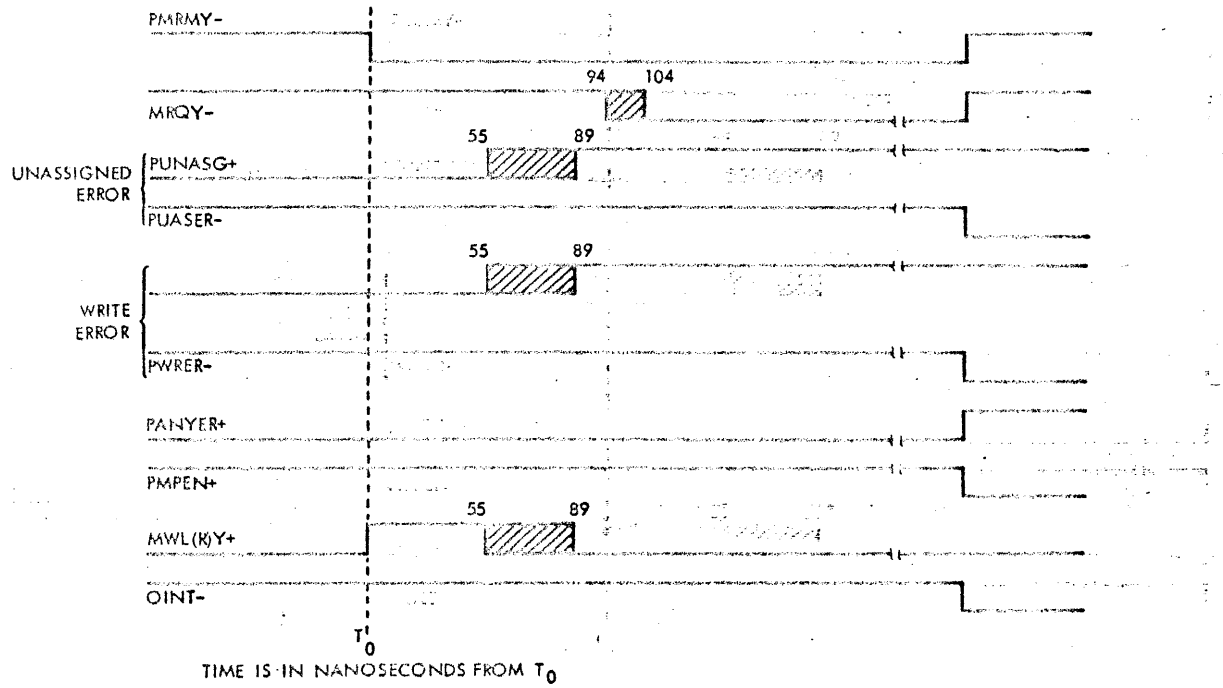

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Figure 4-20. Unassigned and Writing Error Detection

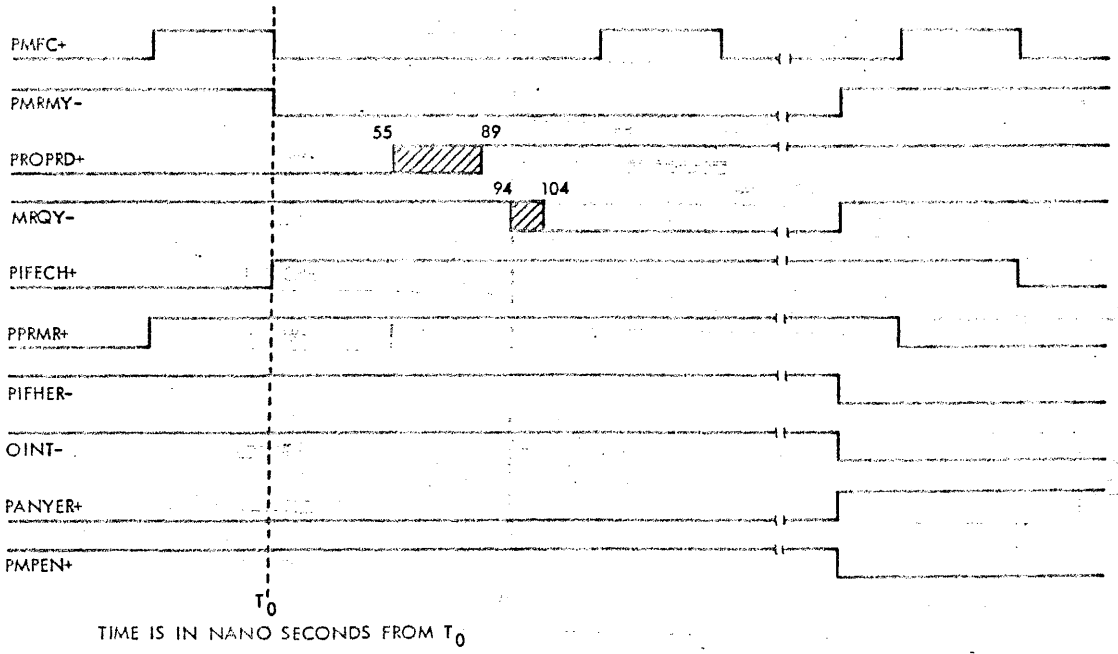

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Figure 4-21. Instruction-Fetch Error Detection

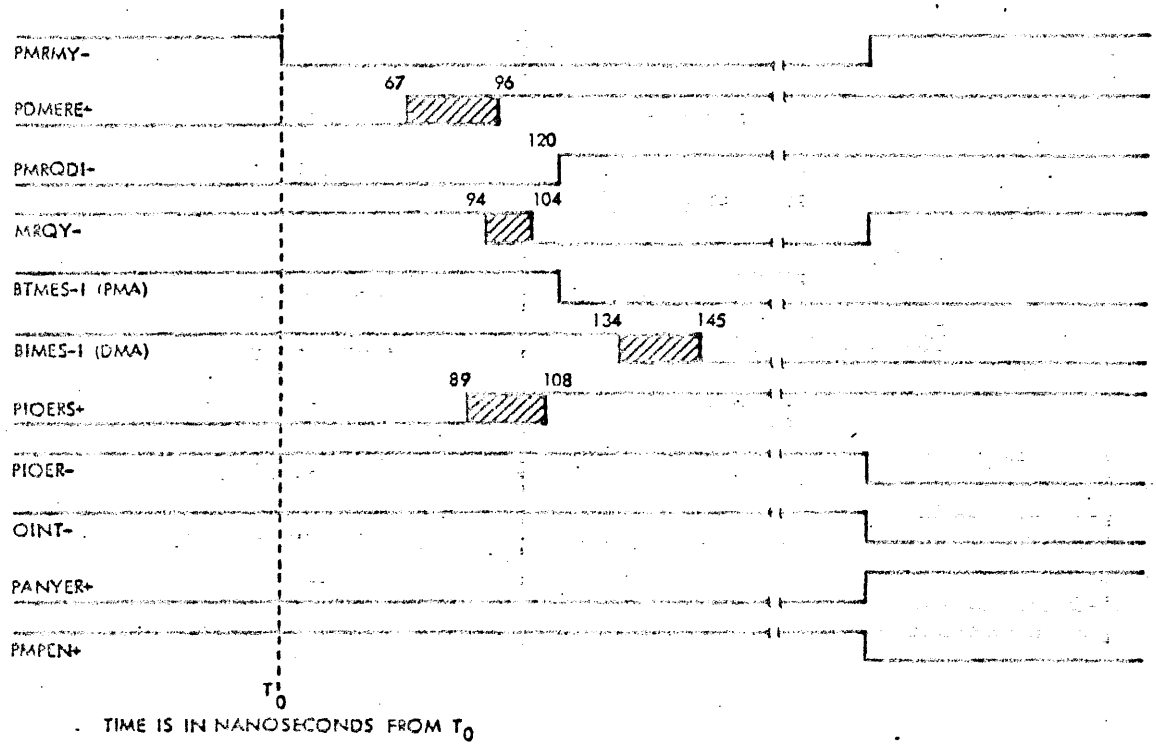

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Figure 4-22. I/O Data-Transfer Error Detection

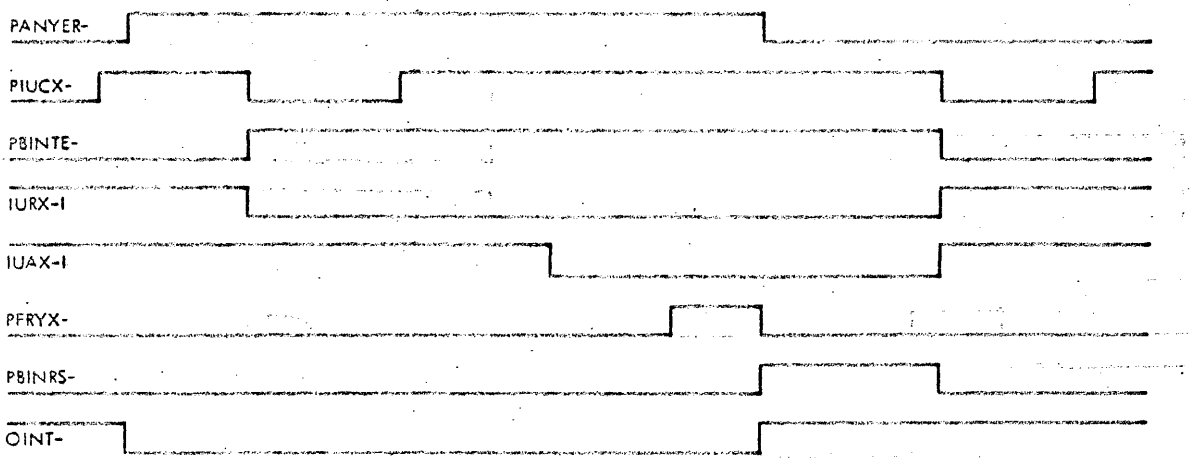

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Figure 4-23. Memory Protection Interrupt

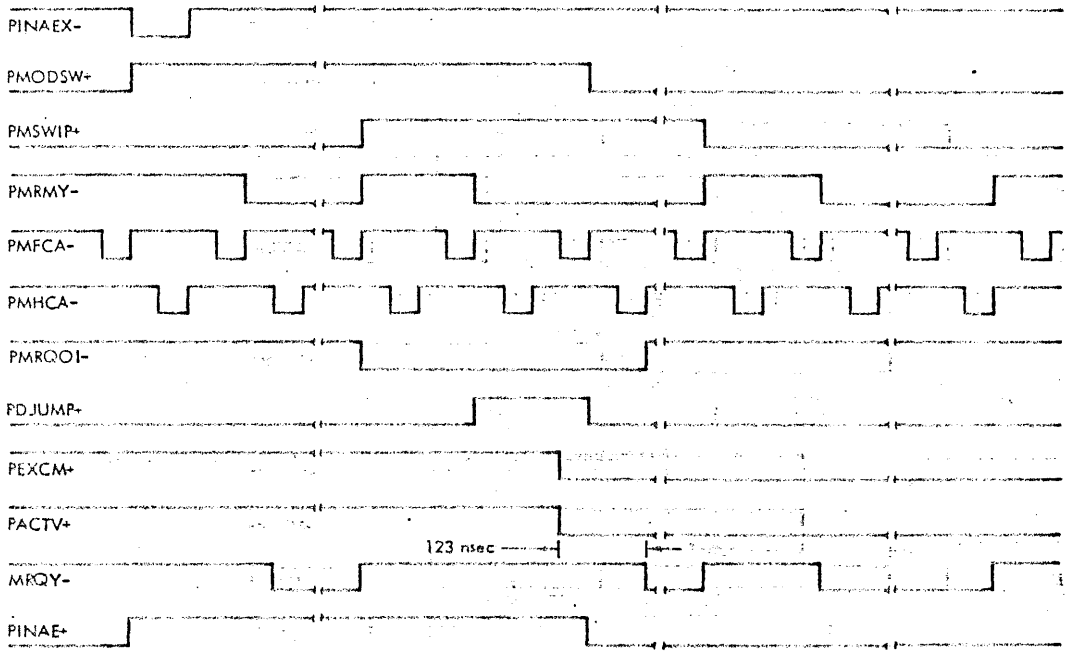

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Figure 4-24. Executive-Mode to Inactive-Mode Switching

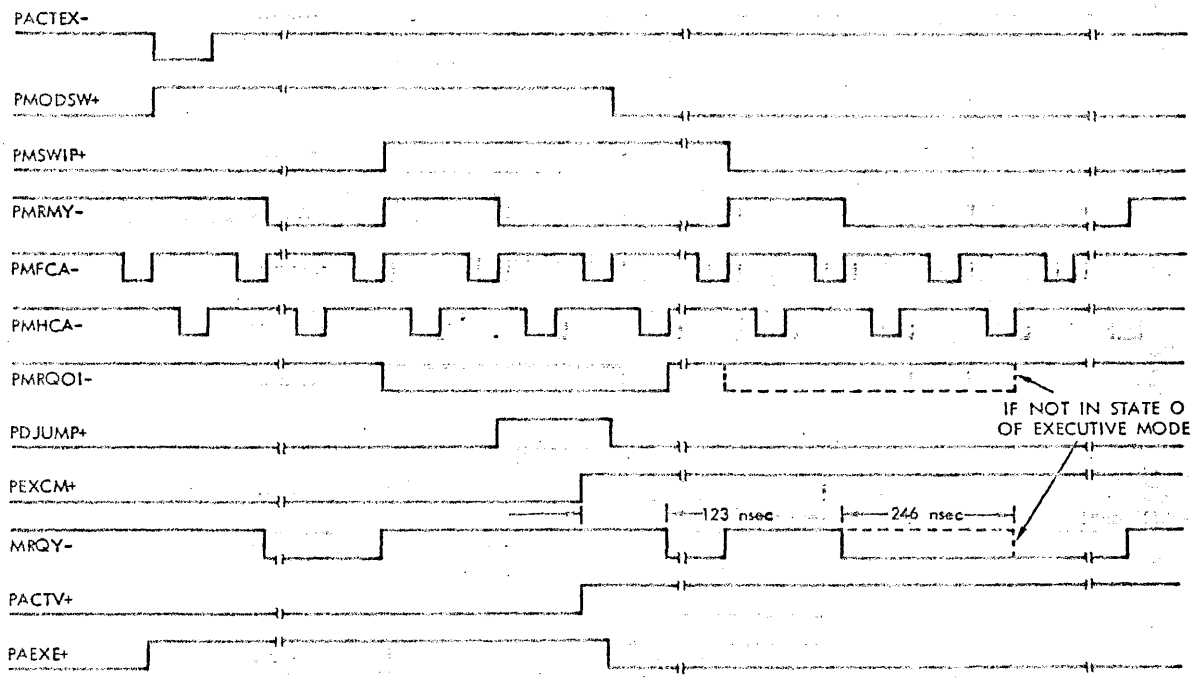

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Figure 4-25. Inactive-Mode to Executive-Mode Switching

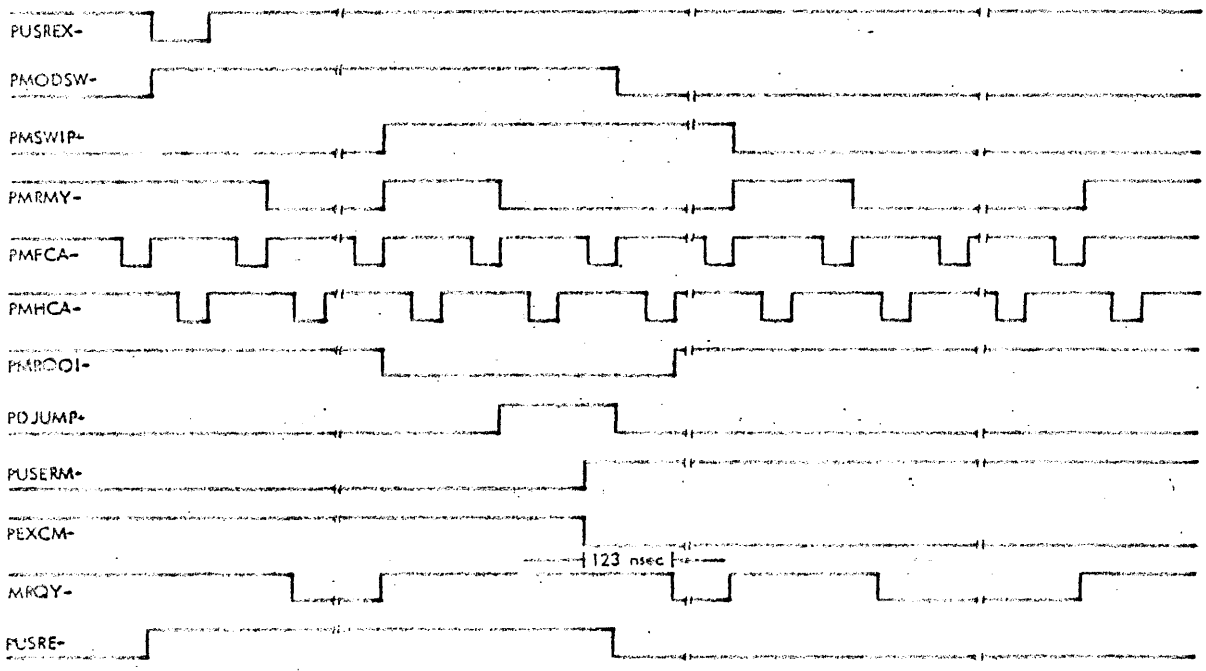

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Figure 4-26. Executive-Mode to User-Mode Switching

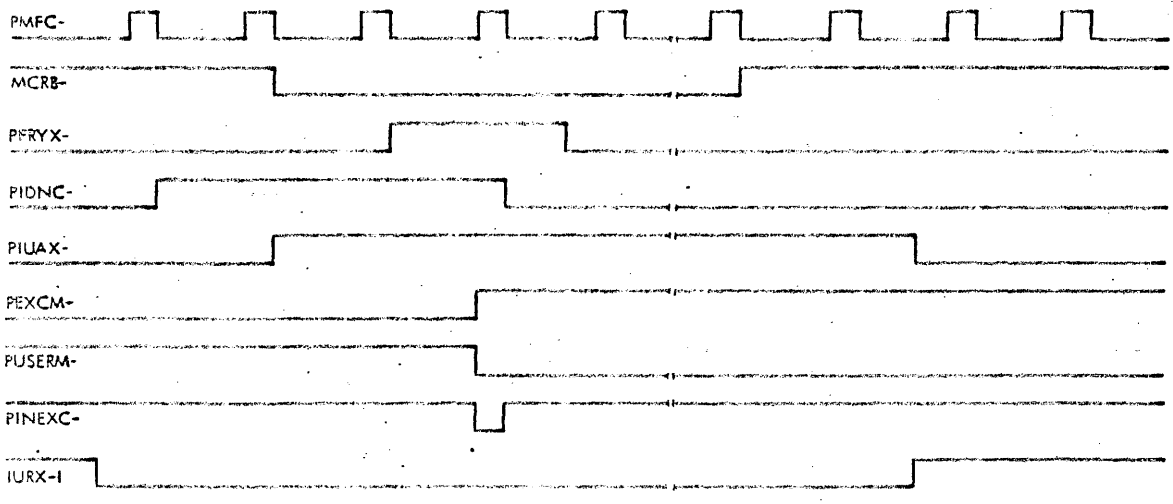

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Figure 4-27. User-Mode to Executive-Mode Switching

SECTION 5
MAINTENANCE

Maintenance personnel should refer to the discussion of the Megamap Test Program included in the MAINTAIN III Reference Manual. This test program verifies correct operation and isolates malfunctions of the SPERRY UNIVAC memory map and megamap options for V70 series computers.

5.1 TEST EQUIPMENT

The following test equipment and tools are recommended for memory map maintenance:

a. Oscilloscope, Tektronix type 547 with dual-trace plug-in unit or equivalent.

b. Multimeter, Triplett type 630 or equivalent.

c. Soldering iron, 15-watt pencil type.

5.2 CIRCUIT BOARD REPAIR

The memory map board is a four-layer PC board. The two outer layers provide signal interconnections for the circuit components. The two inner layers provide low-impedance ground and power voltage distribution, and 90-ohm microstrip transmission lines for all signals. The ICs contained on the board consist of LSI memories; MSI multiplexors, decoders, and registers; and SSI gates and flip-flops.

If it has been determined that circuit board repair is required, it is recommended that the Sperry Univac customer service department be contacted so that a new circuit board can be installed in the user's system and the faulty one returned to the factory for repairs. However, if the user decides to perform his own repairs, extreme caution should be used so that the circuit board is not permanently damaged. Approved repair procedures should be followed such as the ones described in document IPC-R-700A prepared by the Institute of Printed Circuits.

5.3 CIRCUIT-COMPONENT IDENTIFICATION

For IC components, the memory map board has location coordinates that are used in the logic diagrams as reference designations. For example, a flip-flop designated C8 in the memory map logic diagram is in the IC package at location row C column 8 on the memory map board. For discrete components, the reference designations used in the logic diagrams appear on the circuit board adjacent to each component.

Parts lists in the system documentation package provide a cross reference between SPERRY UNIVAC and the manufacturers part numbers.

SECTION 6
MNEMONICS

This section presents an alphabetized list of memory map signal mnemonics with definitions.

Plus or minus signs are included at the end of each mnemonic. The plus sign indicates the signal is at a high logical level when its function is being performed. The minus sign indicates the signal is at a low logical level when its function is being performed. A signal that is the logical inversion of another uses the same mnemonic with an opposite sign; these signals are complements of each other.

I/O bus signal mnemonics end with – I.

Mnemonic	Description
AREAD–	Read/write signal from the PMA option. A low level indicates a PMA reading operation.
BIMES– I	Stops a DMA transfer due to an error during a memory-mapping operation.
BINIO–	Indicates an I/O instruction error has occurred.
BINTE–	Memory-protection interrupt priority.
BTMES– I	Stops a PMA transfer due to an error during a memory-mapping operation.
CACIDE +	Used by the processor to transfer instruction-decoder contents onto the control-store address bus.
CIDHLT +	Indicates that the processor has decoded a halt instruction.
CIDIO +	Indicates that the processor has decoded an I/O instruction.
CIDJMK +	Indicates that the processor has decoded a jump-and-mark instruction.
DJUMP +	Indicates that the program has been directed to the effective jump address of a jump instruction.
DRYF– I	Data ready for high-speed DMA operation.
DRYX– I	Data ready for normal DMA operation.
EBnn– I(0-15)	I/O-bus data.
FRYF– I	Function ready for high-speed DMA operation.
FRYX– I	Function ready for normal DMA operation.
IDNC–	I/O done signal from option board.
IOKn– I(1-4)	I/O key bits from BIC.
IUAF– I	Interrupt acknowledgment for high-speed DMA operation.
IUAX– I	Interrupt acknowledgment for normal DMA operation.
IUCF– I	Interrupt clock for high-speed DMA operations.
IUCX– I	Interrupt clock for normal DMA operation.
IURX– I	I/O-bus interrupt request.
IWLMC–	I/O-write left byte.
IWRMC–	I/O-write right byte.
MAKO +	From processor, indicating the PMA memory request has been acknowledged.
MFC–	Processor full clock.
MHC–	Processor half clock.
MHGY–	Inhibits all memory access on port A of the mainframe memory.
MHGYn– (1-3)	Inhibits all memory access on port A of the expansion memories.
MHMY–	Inhibits all memory access on port B of the mainframe memory.

Mnemonic	Description
MHMYn-(1-3)	Inhibits all memory access on port B of the expansion memories.
MIMCn+(0,1)	Contains bits 0 and 1 of the IM field to specify a reading or writing operation.
MIRAB+	I/O memory request.
MRMYA-	Memory-map memory request of port A.
MRMYB-	Memory-map memory request of port B.
MRQY-	Mainframe memory request.
MRQYn-(1-3)	Expansion memory requests.
MRSZA-	Memory sequencing flip-flop in processor.
MWLY+	Mainframe-memory write, left byte.
MWLYn+(1-3)	Expansion-memory write, left byte.
MWRY+	Mainframe-memory write, right byte.
MWRYn+(1-3)	Expansion-memory write, right byte.
MYAn+(0-15)	Mainframe memory address bits.
MYA1n+(0-15)	Address bits for expansion memory 1.
MYA2n+(0-15)	Address bits for expansion memory 2.
MYA3n+(0-15)	Address bits for expansion memory 3.
MYDAn-(0-17)	Mainframe memory data, port A.
MYDBn-(0-17)	Mainframe memory data, port B.
MYKAn+(16-19)	PMA key bits, port A.
MYKBn+(16-19)	PMA key bits, port B.
MYMAn+(9-15)	Map memory address bits, port A.
MYMBn+(9-15)	Map memory address bits, port B.
MY1Dn-(0-17)	Memory data for expansion memory 1.
MY2Dn-(0-17)	Memory data for expansion memory 2.
MY3Dn-(0-17)	Memory data for expansion memory 3.
OINT-	Memory protection internal interrupt.
P64KEN+	Enables the 64K mode of operation.
PACTEX-	Results from the decoding of instruction EXC2 0146.
PACTV+	Indicates that the memory map is active.
PADR46+	Indicates that device address 46 is decoded.
PADSEL+	Device address selector.
PANYER+	Indicates that the memory map has detected an error.
PBINTE+	Interrupt priority output.
PBEMES+	Enabling signal to stop a DMA transfer due to an error.
PBICKn+(0-3)	BIC key bits.
PBINIO+	Memory-map I/O-instruction error flag.
PBINRS+	Memory-map interrupt response flag.
PBINTA+	Enables the interrupt address.
PBUFE-	Enables buffer data PDIBN+(0-12) to be transferred onto the I/O bus.
PBUFF+	Buffer-full flag.
PCLMEX-	Removes the executive-mode mask.
PDIBn+(0-12)	Output of buffer in the I/O bus data multiplexor.

Mnemonic	Description
PDMAn + (0-15)	Outputs of DMA memory-address counter.
PDMAER +	DMA error flag.
PDMAIN +	Indicates that a read-back operation is in progress.
PDMAOE +	Enabling signal for memory-map loading operation.
PDMAOT +	Indicates that a memory-map loading operation is in progress.
PDMARQ +	Memory-map loading or read-back request.
PDMCMP +	Indicates that a memory-map loading or read-back operation has been completed.
PDMERE +	Enabling signal for an error stop.
PDMIAE +	Enables an interrupt address at the completion of a memory-map loading or read-back operation.
PDMIEN +	Enables an interrupt at the completion of a memory-map loading or read-back operation.
PDMIUR–	Interrupt request at the completion of a memory-map loading or read-back operation.
PDMODP +	Indicates the data-phase of a memory-map loading operation.
PDMPEX–	Disables the memory protection function of the memory map.
PDMRCn– (1-3)	Internal (ripple) clock for the DMA memory address counter.
PDMRQP +	Indicates that a request for a memory-map loading or read-back operation has received I/O priority.
PDMTRM +	Terminates a memory-map loading or read-back operation due to an error.
PDTIX +	Indicates the data phase of an input data transfer.
PDTOX +	Indicates the data phase of an output data transfer.
PDTPF +	Indicates the data phase of a memory map loading or read-back operation.
PDTPFE +	Enabling signal for the data phase of the memory map loading or read-back operation.
PDTXn + (0-15)	Output of the first multiplexor of the I/O-bus data multiplexor.
PDWIOC +	Delayed write I/O control.
PEBn + (0-15)	Received I/O bus data.
PEBDn + (0-15)	Output of the I/O bus data multiplexor.
PEBEN +	Enabling signal for I/O bus drivers.
PEMPEX–	Results from the decoding of instruction EXC2 0646.
PEMSnE + (1-3)	Enabling signals for the executive-mode states.
PEMSMK–	Executive-mode mask.
PERRR–	Reset for an error condition.
PEXCM +	Executive mode.
PEXDEN–	Enables the decoding of an EXC2 instruction.
PEXMPB +	Buffered signal resulting from the decoding of the EXC2 0646 instruction.
PEXMSn + (1-3)	Executive-mode states.
PFRY46 +	Decoded address 46 for function ready.

Mnemonic	Description
PFRYAR +	Indicates that a function ready condition has occurred when IUAX-I is true.
PFULAC +	Full-access mode.
PFUNDE–	Enabling signal for output function decoding.
PHLTER–	Halt-instruction error flag.
PIADn + (0-15)	Output of instruction address register.
PIFECH +	Instruction fetch.
PIFERE +	Instruction-fetch error enabler.
PIFHER +	Instruction fetch error.
PIFJMK–	Jump-and-mark instruction fetch.
PIHMRQ +	Inhibits memory requests.
PIMAE–	Memory address enabler for loading and read-back operation.
PINAn + (1-3)	Interrupt-address data.
PINADM +	Interrupt address strobe.
PINAE +	Inactive-mode enabler.
PINAEX–	Results from the decoding of instruction EXC2 046.
PINEXC–	Indicates the memory map has entered the executive mode by an interrupt.
PINRF +	Interrupt response flag indicating the loading/ read-back operation is complete.
PINRXE +	Interrupt enabler.
PIOEKn + (0-3)	I/O-error key bits.
PIOER +	I/O data-transfer error.
PIOERE +	I/O-instruction error set enabler.
PIOUER +	I/O unassigned error.

Mnemonic	Description
PIOWR–	I/O memory write request.
PIURF +	Interrupt request for the completion of loading/ read-back operation.
PIWLRM +	I/O writing operation.
PJMPER–	Jump error.
PKB1EN–	Enabling signal for key bit 1.
PKBEME +	Clock for PBEMES +.
PKBICK +	Clock for BIC key bits.
PKBUFF–	Clock for PBUFF.
PKDTIX–	Clock for PDTIX +.
PKDTOX–	Clock for PDTOX +.
PKDTPF–	Clock for PDTPF +.
PKEYBn– (0,1)	Key bits.
PKIHMR–	Clock for PIHMRQ +.
PKLPMA +	Clock for PLPMAK +.
PKMMXn + (0-3)	Output of key multiplexor.
PKWC–	Clock for word-transfer counter.
PKWIOC–	Clock for PDIOC +.
PKYMXE–	Enabling signal in key multiplexor.
PKYMXn + (0-3)	Processor or PMA key bits.
PKYNZ +	Key is not equal to zero.
PLDBF–	Loading signal for the buffer in I/O-bus data multiplexor.
PLDIA +	Loading signal for the instruction address register.
PLPMAK +	Loads PMA key bits.
PMAKIR +	PMA or I/O memory cycle.
PMAKYn– (0-3)	PMA key bits.
PMARn + (0-9)	Output of map-address counter.

Mnemonic	Description
PMARCn-(1,2)	Internal clock for map-address register.
PMDXn-(0-17)	Expansion-memory data.
PMDXEN-	Enabling signal for PMDXn-(0-17).
PMFCMP+	Clock for error testing of halt, jump, and I/O instructions.
PMHGnE+(1-3)	Enabling signals for MHGYn-(1-3).
PMHMnE+	Enabling signals for MHMYn-(1-3).
PMIRBF+	Buffered MIRAB+.
PMODSW+	Memory-map mode switching.
PMPEN+	Enabling signal for the memory protection function.
PMRBPE+	Enables the memory request to by-pass the inactive memory map.
PMRQnE+(0-3)	Enabling signals for MRQY-, MRQY1+, MRQY2+, and MRQY3+.
PMRQD1+	Delayed memory request output 2.
PMRQOI-	Memory request output inhibitor.
PMRQOT+	Memory request output.
PMRQPA+	Clock for testing unassigned address, instruction fetch, and writing and I/O data-transfer errors.
PMRQYD+	Delayed memory request output 1.
PMRYDN+	Goes true when memory acknowledgment and memory request are true.
PMSWIP+	Indicates the memory map is in the process of switching from one operating mode to another.
POINTE+	Enabling signal for memory-protection internal interrupt.

Mnemonic	Description
PPMAWR-	PMA writing request.
PPRnF+(1-4)	High-speed DMA priority lines.
PPRKYn+(0-3)	Output bits from the memory map's key register.
PPRMF+	Priority input signal for high-speed DMA.
PPRMR+	Indicates processor is requesting memory.
PPRMX+	System interrupt priority input.
PPRMXB+	Buffered PPRMX+.
PPRNX-	System interrupt priority output.
PPROWR-	Processor writing request.
PRnX-I(1-9)	I/O-bus priority lines. PR1X-I is the highest priority and PR9X-I is the lowest.
PRAMAn-(0-7)	Output bits from the RAM address multiplexor.
PRAMSn-(0-3)	Row selectors for the RAM array.
PRAMW+	When high, loads data into the RAM array. When low, enables addressed data to be read out of the RAM array.
PRDIn-(11-12)	Swapping control bits.
PRDMEX-	Resets the memory map's DMA-transfer logic.
PRDOn(0-12)	Output data from RAM array.
PRIVLG+	Enabling signal for privileged instructions.
PRMAKn+(0-3)	Input for key multiplexor from either the PMA option or the memory map's key register.
PRMWEN+	Enabling signal for PRAMW+.

Mnemonic	Description
PROTRD +	Indicates that only operand fetches are permitted.
PRWRn- (11,12)	Read/write control signals for bits 11 and 12 of the RAM array.
PSDMEX-	Starts a memory-map DMA transfer.
PSEDMA +	Senses if the memory map is performing a DMA operation.
PSEN'n + (0,1)	Decoding bits for a SEN instruction.
PSENEN +	Enabling signal for SEN instruction.
PSIn + (0,1)	Selector signals for the I/O bus data multiplexor.
PUADn + (0-15)	Output bits from unassigned address register.
PUASER +	Indicates an unassigned address error.
PUNASG +	Indicates an unassigned page.
PUSAGW +	Writing strobe for usage bit.
PUSERM +	User mode.
PUSRE +	Enabling signal for user mode.
PUSREX-	Switches memory map from executive mode to user mode.
PWCRCn- (1,2)	Internal (ripple) clock for word-transfer counter.
PWCZ-	Output of word-transfer counter.
PWIMA-	Loads the initial memory address into the DMA memory-address counter.
PWIOC-	Loads the initial map address into the map-address counter.
PWRER-	Indicates a writing error.
PWRFUA-	Writing into a full-access page.
PWRKC-	Write-key control signal. Loads data into key register, 64K-memory register, and executive-state register.
PWRT-	Writing request.
PXFRW-	Loads data into the word-transfer counter.
PYD123 +	Memory acknowledgment from expansion memory 1, 2, or 3.
PYDNMD +	Delayed memory acknowledgment from expansion memory 1, 2, or 3.
SERX- I	I/O-bus sense response.
SPFA-	System power failure alarm.
SRST-	System reset.
SYRT- I	I/O bus system reset.
TPIF- I	High-speed trap-in request of I/O bus.
TPOF- I	High-speed trap-out request of I/O bus.
YDNMA +	Memory acknowlegment from port A of mainframe memory.
YDNMB +	Memory acknowlegment from port B of mainframe memory.
YDNMn + (1-3)	Memory acknowledgments from expansion memories.

DWG NO. 01A1541

REVISIONS

REV	EN	CHG CODE	DESCRIPTION	DR	APPD
A	82693	—	PRODUCTION RELEASE		
B	82782	1	ADDED PAR. D TO NOTE 10.1		5-3-74
—	82976	—	ADDED NOTE 10.2 ON PAGE 4		5-29-74
C	82997	1	ADDED NOTE 11.3 ON PAGE 4		5-29-74
—	83042	—	ADDED TO TAB BLK & NOTE 5 & ADDED NOTE 5.1 & PG 13		6/26/74
D	83718	1	ADDED NOTE 10.3	SJ	4/11/75
E	83780	2	REVISED & REDRAWN SH 12. SH 13, REMOVED "I/O PORT" & ADDED NOTE AT BOTTOM. ADDED SH. 14. ADDED -003 & LAST COLUMN TO TAB BLOCK	SJ	4/14/75
F	83786	2	SH.2 PARA. 4.0 a. 53P0872 WAS 53D0703. SH.3 PARA 4.0 b. 53P0873 WAS 53P0704	SJ	5/6/75
G	84097	1	NOTE 10.3 WAS TO CONN J6-13	SJ	9/30/75

TABULATION

PART NUMBER	MODEL NO.	REMARKS	OTHER OPTIONS IN SYSTEM
01P1541-000	7X-3300		
01P1541-001		With DC Pwr Cable, 7" Chassis	
01P1541-002		With DC Pwr Cable, 14" Chassis	WCS or FPP
01P1541-003		With DC Pwr Cable, 14" Chassis	None

FOR PARTS LIST SEE 01P1541

NEXT ASSEMBLY: END ITEM	MODEL NO.: V73	varian data machines / a varian subsidiary, 2722 michelson drive / irvine / california / 92664
DR		
CHK	for W.B	1-23-74
DSGN		
ENGR	for A.L	1/23/74
APPD		1/23/74
APPD		
CODE IDENT NO. 21101	TITLE: MEMORY MAP OPTION	
SIZE A	DWG NO. 01A1541	REV K
SHEET 1 OF 16		

8A10188 000C

REVISIONS

REV	EN	CHG CODE	DESCRIPTION	DR	APPD
H	84226	2	SH. 7, ADDED SEC. 18.0, RENUMBERED SHEETS	LKC	12/15/76
J	84233	3	REVISED NOTE 2 & ADDED FIGURE 5	LKC	12/15/76
K	84762	3	SH. 10, 11, & 12 - CONFIGURATION STD WAS PORT A	LKC	12-15-76

NOTES: UNLESS OTHERWISE SPECIFIED

1.0 This drawing provides for a Memory Map Board (DM 399) to be used in the V.D.M. V70 series computers.

2. Identify per specification 98A1163 (Reference Figure 5)

3.0 Table I lists all of the discretionary wiring features of the Memory Map Board along with the standard configuration as manufactured and tested by VDM. In the Table, the column headings are defined as follows:

3.1 CONFIGURATION

STD. - The standard test configuration as assembled prior to discretionary system wiring. "X" is the standard. "N/C" means no connection.

SYS. ENGNG. - An "X" should be placed in the appropriate column and line to indicate the module version and the actual module configuration as specified by the system engineer.

FUNCTION - The name of the feature under consideration.

LOCATION - Name of the discretionary wiring location as specified on the board assembly drawing 44E0685.

ALT. CONFIG'S. - The way the feature may be wired on completion of system test. This wiring is specified by the VDM systems engineer.

4.0 Power for the map may be provided in one of three ways as follows:

a. Use 01P1280-004 (115 VAC) or
01P1280-005 (230 VAC)
power supply and cable 53P0872.

b. Use 53P0873 cable as second cable from a V73 main power supply (01P1320) if sufficient excess +5V logic power is available.

c. Use specially designed power supply arrangement.

5.0 Examples of module interconnection in V73 system with memory map are shown in Test Cable Set Option, P/N 01A1450. (For -000 and -001) (Ref. Fig. 2)

5.1 Examples of module interconnection in reconfigured V73 systems and V72, V74 systems with memory map are shown in test cable option P/N 01A1665 (For -002). (Ref. Fig. 3)

6.0 Mapping for dual port memory requires one map per port.

7.0 System Memory Lockout Configurations.

7.1 The map allows extension of one of the port lockout function (MHGY- or MHMY-) to MHGY- or MHMY- on any expansion bus. Figure 1 illustrates a typical memory lockout configuration in which PMA Hog requests drive the MHGY- signal received by the map and drives out to the appropriate expansion memory busses as MHGYX- or MHMYX- (X=1, 2, 3).

8.0 Power Failed and Memory Reset

8.1 The map allows extension of power failed and memory reset (SPFA- and SRST- on any expansion bus. SPFA- or SRST- on each expansion bus can be eithee terminated or passed on to next expansion bus.

9.0 Memory Expansion

9.1 The map uses three memory expansion cables to drive three memory buses. Each cable can be an A port (pass A terminate B port) or a B port (pass B terminate A port) cable. Details of memory expansion can be referred to documents #01P1582-000, #01P1582-001, and #01P1582-002.

10.0 Processor Board Requirements

10.1 A. BINS - (Memory Protect Present) must be wired to ground.

B. The following modifications to the V73 Processor Board (44P0614), using DM 353 Rev. B and Rev. D printed wiring boards, are required:

1) Install EN 81749. This EN supplies needed control terms to the memory map.

2) Cut etch near connector pin J06-04 on the circuit side of the board.

C. The following modifications to V73 processor boards (44P0614), using DM 353 Rev. B through Rev. AA printed wiring boards, are required:

1) Add a jumper on circuit side of the board from connector pin J06-04 to I.C. pin T4-2.

2) Add a jumper on circuit side of the board from connector pin J06-42 to I.C. pin L4-3.

D. For processor boards using DM 353 Rev. AG and lower printed wiring boards install EN 82650-01 rework.

10.2 Configure jumpers at locations 23, 24, 25 and 26 per Note 5 and the Chart on Sheet 6 of 01A1331.

10.3 For Processor Boards using DM353 Rev AS and lower remove jumper wire from F15-4 to F15-7 and add jumper wire from F15-4 to Conn J6-12; using DM353 Rev AT and above remove jumper clip L1-L2 and add jumper clip L2-L3.

11.0 Option Board Requirements

11.1 The following modifications to the V73 Option Board (44P0619), using DM 357 Revision B and Revision D printed wiring boards, are required:

a. Install EN 81690. This change replaces the memory protect of the option board with the memory protect of the memory map.

b. Install EN 81872. This EN eliminates connector conflicts between the option board and the memory map on J3.

c. If memory map is installed on "Memory Port A" rework as follows:

Lift IC F14-9 and K6-11
Jumper F14-9 to K6-11 (Lifted Pins)
Jumper F14-9 (Lifted Pin) to wire wrap pin B50

d. If memory map is installed on "Memory Port B" rework as follows:

Lift IC F14-1 and K6-13
Jumper F14-1 to K6-13 (Lifted Pins)
Jumper F14-9 (Lifted Pin) to wire wrap post A25

11.2 The following modifications to the V73 Option Boards (44P0619), using DM 357 Revision B through Revision AC Printed Wiring Boards, are required:

a. Cut the etch near the connector pin J06-42 on the circuit side of the board.

11.3 The following modifications to the V73 Option Boards (44P0619), using DM 357 Revision T through Revision AC Printed Wiring Boards are required:

a. Cut etch on circuit side at connector pin J3-30, 32, 34 and 36.

12.0 BTC Requirements

12.1 BTC #44P0629-001 is used for a system with PMA and Memory Map. The following wires should be added to the I/O expansion chassis to accommodate the map error stop signal (BTMES-I):

a. JX-94 to JY-96 and JZ-94

b. JX-95 to JY-98 and JZ-95

where JX is the I/O cable slot,
JY is the BRC slot and
JZ is the terminator slot.

13.0 BIC Requirements

13.1 BIC #44P0689-003 is used for a system with map. The following wires should be added to the I/O expansion chassis to accomodate the map error stop signal (BIMES-1) and I/O key bits (IOK1-4-1):

a. JX-93 to JU-93 and JZ-93

b. JX-95 to JU-95 and JZ-95

c. JX-109 to JU-109 and JZ-109

d. JX-110 to JU-110 and JZ-110

e. JX-111 to JU-111 and JZ-111

f. JX-112 to JU-112 and JZ-112

g. JX-113 to JU-113 and JZ-113

h. JX-114 to JU-114 and JZ-114

where JX is the I/O cable slot,
JU is the BIC slot and
JZ is the terminator slot.

14.0 DCA Requirements

14.1 The following wire changes should be made to DCA for a system with map:

a. Delete: J03-30, J03-32, J03-34, J03-36, From RT 30.

b. Add: J03-29 to J01-109 (IOK1-1)
J03-30 to J01-110 (IOK2-1)
J03-31 to J01-112 (IOK3-1)
J03-32 to J01-113 (IOK4-1)
J03-27 to J01-94 (BTMES-1)
J03-34 to J01-93 (BTMES-1)
J03-33 to J01-95 (RETURN)
J03-35 to J01-111 (RETURN)
J03-35 to J01-114 (RETURN)
J01-32 to J03-28 (RT 30)
J01-34 to J02-34 (RT 34)

15.0 I/O Terminator Requirement

15.1 Terminator shoe #44P0630-000 should be replaced by #44P0664-000 on the I/O expansion chassis in a system with map installed.

16.0 For additional information, refer to the following documents:

a. V73 Processor Board
Option Drawing #01P1331

b. V73 Option Board
Option Drawing #01P1332

c. V73 WCS Board
Option Drawing #01P1444

17.0 For cable connections on front edge of boards see sheet 12 of this drawing.

18.0 On all assemblies with DM399 Rev "L" and above priority out is provided as a jumperable item on J3 Pin 21. This is provided for special non-standard system configurations. Normally, the priority line would end at the map. To use this feature, jumper E14 to E86.

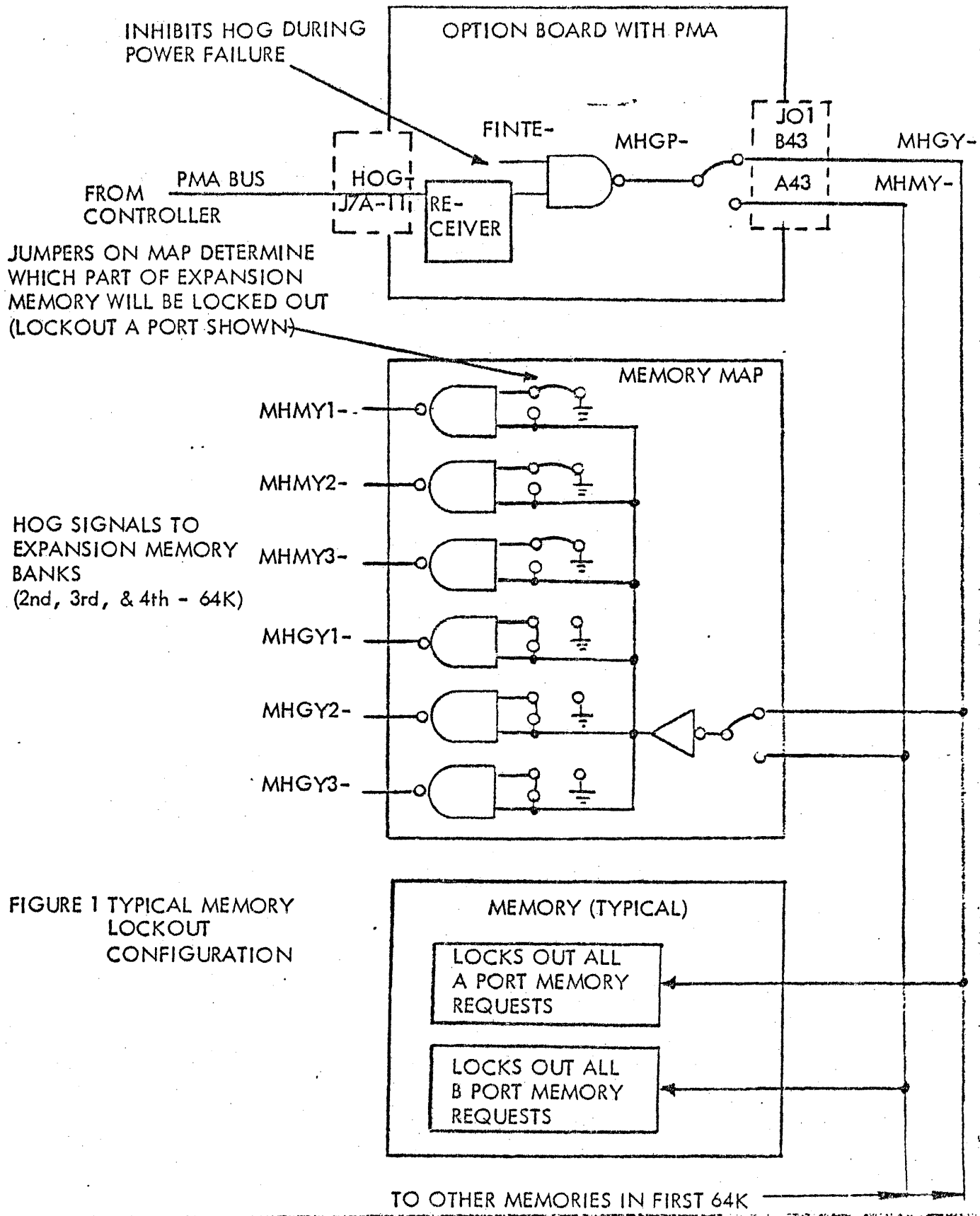

FIGURE 1 TYPICAL MEMORY LOCKOUT CONFIGURATION

SPECIFICATION FOR MEMORY MAP MODULE

CONFIGURATION STD.	CONFIGURATION SYS ENGNG 000			FUNCTION	JUMPER CLIP LOCATIONS (F/N 4) *INDICATES LOCATIONS WHERE WIRE WRAP IS REQUIRED IN PLACE OF (F/N4)	ALTERNATE CONFIGURATIONS
X N/C				I/O Device 46 Address 56	E3-E2 E3-E4	I/O Device Address = 56
X				Map Loading/Reading High Speed DMA Priority	*E7, E10, E13 should be wired to the High Speed DMA Chain such that the Map Loading/Reading has the Lowest Priority of all high speed DMA users.	
X				Normal DMA Priority to enable Map Loading/ Reading and Complete Interrupt	*E18 and E19 can be wired to any normal DMA Priority Chain. E18 is the Priority in and E19 is the Priority out.	If Map Loading/Reading Complete Interrupt is not desired, only E18 should be connected to Normal DMA Chain for Priority Input and output
X N/C				Map Loading/Reading Complete Interrupt Enable	E22-E20 Interrupt Enabled (Standard) E22-E21 Interrupt Disabled	This interrupt is disabled for a Vortex II System.
X X X X				Key Select From Processor Key Bus or Map Key Register	E23-E25 Select Map E26-E28 Key Register E29-E31 (Standard) E32-E34	E24-E25 Select E27-E28 Processor E30-E31 Key Bus E33-E34
X				Privileged Instruction Enable	E35-E36 Privileged Instruction Enabled (Standard)	E35-E37 Privileged Instructions Disabled
X				Executive Mode Enable	E39-E40 Executive Mode Enabled (Standard)	E38-E40 Executive Mode Disabled

SPECIFICATION FOR MEMORY MAP MODULE

CONFIGURATION STD	CONFIGURATION SYS ENGNG 000			FUNCTION	JUMPER CLIP LOCATIONS (F/N4) *INDICATES LOCATIONS WHERE WIRE WRAP IS REQUIRED IN PLACE OF (F/N4)	ALTERNATE CONFIGURATIONS
X X X X X X				Memory Lockout On Memory Bus 1, 2, and 3	E42-E41 E44-E45 E48-E49 E51-E52 E54-E55 E57-E58 Memory Lockout Disabled (Standard)	Bus 1 Memory Lockout Enabled Port A: E42-E43 Port B: E50-E52 Bus 2 Memory Lockout Enabled Port A: E45-E46 Port B: E53-E55 Bus 3 Memory Lockout Enabled Port A: E47-E49 Port B: E56-E58
X				Memory Request Delay #1	*E72 should be wired to either E60, E61, E62, E63, E64, E65, E66, E67, E68, E69, E70, to give a Total Delay of 80 Ns between PMRMY+ (B15-4) and PMRQYD+ (E72)	
X				Memory Request Delay #2	*E73 should be wired to either E60, E61, E62, E63, E64, E65, E66, E67, E68, E69, E70 to give a Total Delay of 120 Ns Between PMRMY+ (B15-4) and PMRQYD1+ (E72)	
N/C				Memory Lockout on Bus 0	Port A: C31-B31 Port B: B31-A31	C31-B31 A Port Lockout B Port B31-A31 B Port Lockout A Port
PORT B				Memory Port Connection	Port A / Port B: B1-C1 / A1-B1 B2-C2 / A2-B2 B3-C3 / A3-B3 B4-C4 / A4-B4 B5-C5 / A5-B5 B6-C6 / A6-B6 B7-C7 / A7-B7 B8-C8 / A8-B8	If PMA is used and mapping of only one port is required, then map, option board, and processor should be put on B Port. Mapping two ports requires one map board on each port.

SPECIFICATION FOR MEMORY MAP MODULE

CONFIGURATION				FUNCTION	JUMPER CLIP LOCATIONS (F/N 4) *INDICATES LOCATIONS WHERE WIRE WRAP IS REQUIRED IN PLACE OF (F/N4)		ALTERNATE CONFIGURATIONS
STD	SYS ENGNG 000				Port A	Port B	
PORT B				Memory Port Connection (Continued)	B9-C9	A9-B9	
					B10-C10	A10-B10	
					B11-C11	A11-B11	
					B12-C12	A12-B12	
					B13-C13	A13-B13	
					B14-C14	A14-B14	
					B15-C15	A15-B15	
					B16-C16	A16-B16	
					B17-C17	A17-B17	
					B18-C18	A18-B18	
					B19-C19	A19-B19	
					B20-C20	A20-B20	
					B21-C21	A21-B21	
					B22-C22	A22-B22	
					B23-C23	A23-B23	
					B24-C24	A24-B24	
					B25-C25	A25-B25	
					B26-C26	A26-B26	
					B27-C27	A27-B27	
					B28-C28	A28-B28	
					B29-C29	A29-B29	
					B30-C30	A30-B30	
					B32-C32	A32-B32	
					B33-C33	A33-B33	
					B34-C34	A34-B34	
					B35-C35	A35-B35	
					B36-C36	A36-B36	
					B37-C37	A37-B37	
					B38-C38	A38-B38	
					B39-C39	A39-B39	

varian data machines
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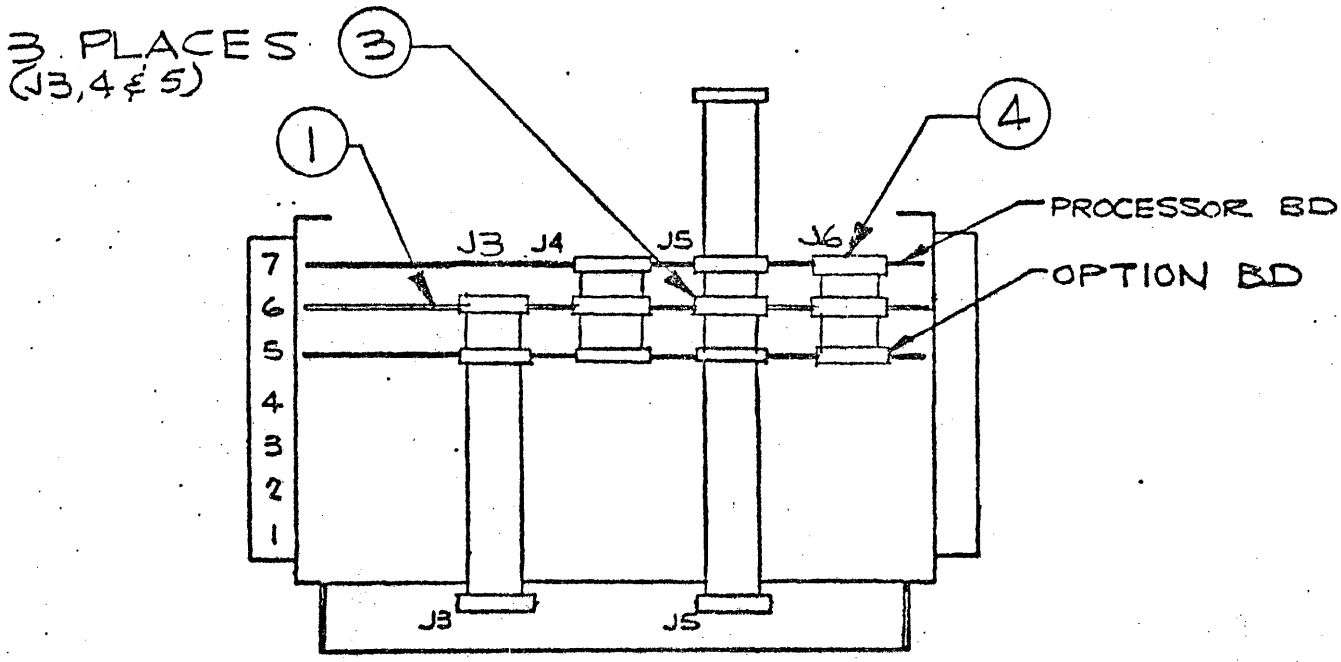
CODE IDENT NO. 21101

SPECIFICATION FOR MEMORY MAP MODULE

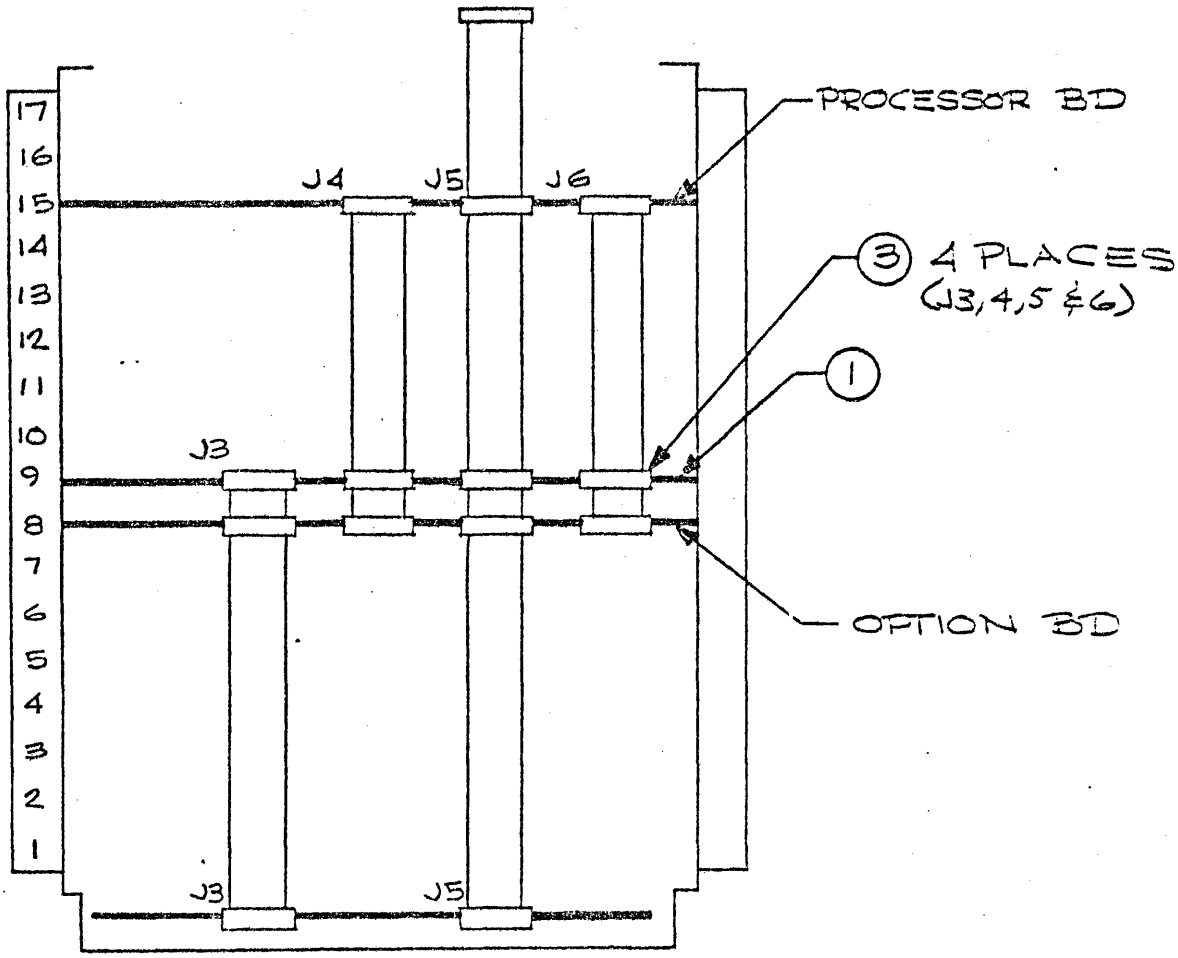
CONFIGURATION STD	CONFIGURATION SYS ENGNG 000	CONFIGURATION SYS ENGNG	CONFIGURATION SYS ENGNG	FUNCTION	JUMPER CLIP LOCATIONS (F/N4) *INDICATES LOCATIONS WHERE WIRE WRAP IS REQUIRED IN PLACE OF (F/N4		ALTERNATE CONFIGURATIONS
PORT B				Memory Port Connection (Continued)	Port A	Port B	
					B40-C40	A40-B40	
					B41-C41	A41-B41	
					B42-C42	A42-B42	
					B43-C43	A43-B43	
					B44-C44	A44-B44	
					B45-C45	A45-B45	
					B46-C46	A46-B46	
					B47-C47	A47-B47	
					B48-C48	A48-B48	
					B49-C49	A49-B49	
					B50-C50	A50-B50	
					B51-C51	A51-B51	
N/C				Memory Expansion Connection	J8, J9 to J12, J13 to J10, J11 to	Memory Bus 1 Memory Bus 2 Memory Bus 3	Connected if Memory Expansion is used.
X N/C				Map Read Back Enable	E76-E74 E76-E75	Enabled Disabled	(If the map is used to map the stand alone PMA)
X X N/C N/C				Key MUX Select Control	E77-E78 E81-E80 E77-E79 E81-E82		(If the map is used to map the stand alone PMA)
X N/C				Memory Protect	E85-E83 E85-E84	Enabled Disabled	(If the map is used to map the stand alone PMA)

01A1541
SH 12 OF 16
REV K



FOR -000 & -001

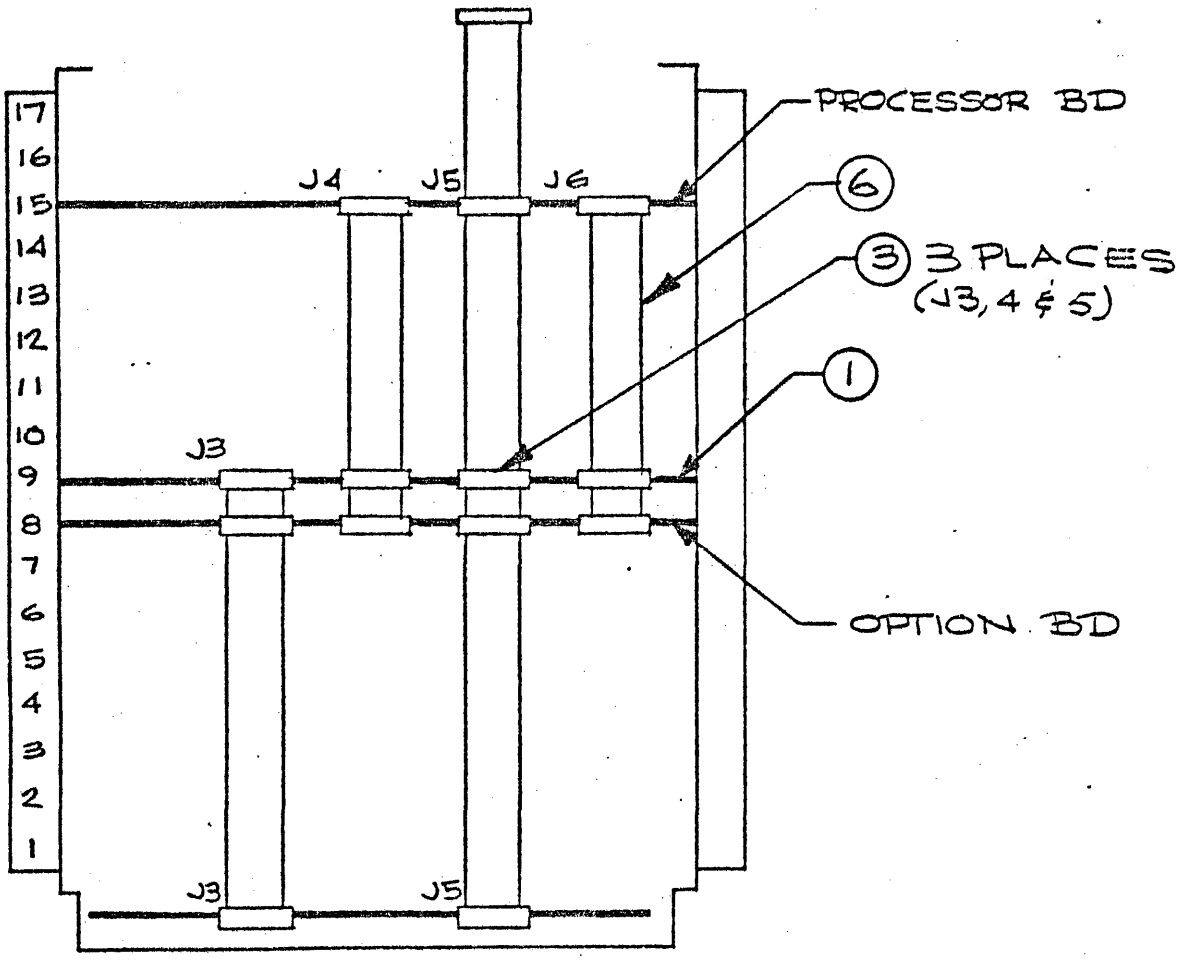
FIGURE 2



FOR-002

(APPLICABLE TO V72 & V73 WITH WCS OR FPP)

FIGURE 3



FOR -003

(APPLICABLE TO V72 & V73 WITH NO OTHER OPTIONS)

FIGURE 4

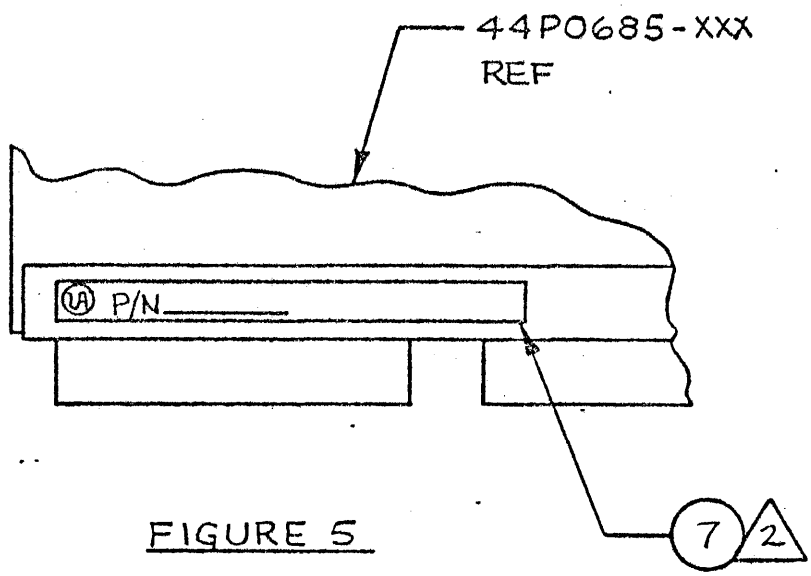


FIGURE 5

varian data machines	CODE IDENT NO. 21101		01A1541	K
			SH 16 OF 16	REV

SPERRY UNIVAC

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PARTS LIST

MFG. CODE	ISSUE DAT	NTROL	CA	TYPE	COMM. CODE	ST.	DOC. NO.	L. REV.
W	10/24/79	W777		M		A	PL W 0101541	L

TLE
MEMORY MAP OPTION

CL	U/M		AC	DOC. SIZE	RANGE	THRU	ISSUE	PIC REV.
A	EA		16	A				K

FIND NO.	QUANTITY REQUIRED	U/M	SIZE	PART OR IDENT. NO. DOCUMENT NO.	DASH	NOMENCLATURE OR DESCRIPTION		SP	CHG
[11				W-87844	-14	PL REV L, PIC REV K, RANGE 00 - 03 EIR RELEASED	10/24/79		
**********						********** COMMON DATA **********			
1	1	EA		W 4400685	-00	PC ASSEMBLY - MEMORY MAP DM399		A	*
2	AR	IN		W 5300333	-90	WIRE, WIRE-WRAP, SOLID	WHITE 30AWG	A	*
7	1	EA		W 8600015	-00	LABEL, IDENTIFICATION		A	*
$01		X		8W01163	-00	MARKING SPEC	PART IDENTIFICATION	A	*
**********						********** VARIABLE DATA - 00 **********			
3	3	EA		W 5700272	-03	CONNECTOR	50 CONTACT WITH OUT MTG EARS	A	*
4	1	EA		W 5300674	-10	CABLE ASSEMBLY	2 POSITION	A	*
**********						********** VARIABLE DATA - 01 **********			
3	3	EA		W 5700272	-03	CONNECTOR	50 CONTACT WITH OUT MTG EARS	A	*
4	1	EA		W 5300674	-10	CABLE ASSEMBLY	2 POSITION	A	*
5	1	EA		W 5300873	-60	CABLE ASSEMBLY - DC OUTPUT		A	*
**********						********** VARIABLE DATA - 02 **********			
3	4	EA		W 5700272	-03	CONNECTOR	50 CONTACT WITH OUT MTG EARS	A	*
5	1	EA		W 5300873	-60	CABLE ASSEMBLY - DC OUTPUT		A	*
**********						********** VARIABLE DATA - 03 **********			
3	3	EA		W 5700272	-03	CONNECTOR	50 CONTACT WITH OUT MTG EARS	A	*
5	1	EA		W 5300873	-60	CABLE ASSEMBLY - DC OUTPUT		A	*
6	1	EA		W 5300674	-25	CABLE ASSEMBLY	2 POSITION	A	*

DUPLICATE

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PARTS LIST

MFG CODE	ISSUE DATE	CONTROL	CA	TYPE	COMM CODE	ST	DOC NO	SHEET	PL REV
J W	10/13/80	W777		M		A	PL W 4400914	1	L

TITLE: PC ASSY - MEMORY SEMICONDUCTOR

CL	U/M	AC	DOC SIZE	RANGE	THRU	ISSUE	PIC REV
A	EA	3	C				C

FIND NO	QUANTITY REQUIRED	U/M	SIZE	PART OR IDENT NO DOCUMENT NO	DASH	NOMENCLATURE OR DESCRIPTION	SP	CHG
Z11				W-94457	-02	PL REV L, PIC REV C, RANGE 00 - 05 EIR RELEASED 10/13/80		
Z11 1				FCW2806-0	16	FCO HISTORY; FCO REV -		
Z11 2				FCW2832-0	21	FCO HISTORY; FCO REV -		
Z11 3				FCW2833-0	21	FCO HISTORY; FCO REV -		
Z11 4				FCW2834-0	21	FCO HISTORY; FCO REV -		
Z11 5				FCW2835-0	21	FCO HISTORY; FCO REV -		
Z10				W-94421	-01	PL REV K, PIC REV C, RANGE 00 - 05 EIR RELEASED 08/26/80		
**********						********** COMMON DATA **********		
1	1	EA		W 4000748	-00	PC BOARD SEMICONDUCTOR MEMORY (OM559)	A	
				NOTE		USE REV D		
2	1	EA		3008194	-00	INTEGRATED CIRCUIT TTL 7474 * FF D DUAL	I	
				REF DES	1	IC85,		*
3	3	EA		3007755	-00	INTEGRATED CIRCUIT TTLH 74H04 * GT HEX INVERT	I	
				REF DES	1	IC32-IC34,		*
4	1	EA		3008183	-00	INTEGRATED CIRCUIT TTL 7404 * GT HEX INVERT	I	
				REF DES	1	IC92,		*
5	1	EA		3008181	-00	INTEGRATED CIRCUIT TTL 7400 * GT NAND 2IN	I	
				REF DES	1	IC79,		*
6	3	EA		2899571	-00	INTEGRATED CIRCUIT DIGITAL TTLS 74S00 * GT NAND 2IN	A	*
				REF DES	1	IC47,IC50,IC68,		*
7	2	EA		W 4900127	-00	INTEGRATED CIRCUIT, DIGITAL TTL 74161 CNTR 4BT BIN	A	
				REF DES	1	IC43,IC44,		*
8	10	EA		W 4900128	-01	INTEGRATED CIRCUIT, DIGITAL TTL 7438 QUAD 2IN NAND	I	
				REF DES	1	IC6,IC8,IC10,IC12, IC14,IC20,IC22,IC24, IC26,IC28,		*
9	1	EA		3008089	-00	INTEGRATED CIRCUIT TTL 7413 * GT NAND 4IN	I	
				REF DES	1	IC91,		*

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PARTS LIST

MFG CODE	ISSUE DATE	CONTROL	CA	TYPE	COMM CODE	ST	DOC NO	SHEET	PL REV
J W	10/13/80	W777		M		A	PL W 4400914	2	L

TITLE: PC ASSY - MEMORY SEMICONDUCTOR

CL	U/M	AC	DOC SIZE	RANGE THRU	ISSUE	PIC REV
A	EA	3	C			C

FIND NO	QUANTITY REQUIRED	U/M	SIZE	PART OR IDENT NO DOCUMENT NO	DASH	NOMENCLATURE OR DESCRIPTION	SP	CHG
10	2	EA		5036524	-00	INTEGRATED CIRCUIT DIGITAL TTL 3404 * FF LATCH 6BT	I	
				REF DES	1	IC4,IC5,		*
11	1	EA		3008031	-00	INTEGRATED CIRCUIT TTL 74122 * MVB RG1 W/C	I	
				REF DES	1	IC80,		*
13	12	EA		5036504	-00	INTEGRATED CIRCUIT DIGITAL TTLS 74S04 * GT HEX INVERT	A	
				REF DES	1	IC47,5,IC49,IC52, IC57,IC60,IC64,IC71, IC78,IC81,5,IC83,		*
					4	IC89,IC95,		*
14	2	EA		5036506	-00	INTEGRATED CIRCUIT TTLS 74S11 * GT AND 3IN	A	*
				REF DES	1	IC74,IC75,		*
15	1	EA		5036518	-00	INTEGRATED CIRCUIT TTLS 74S40 * GT NAND BUFF	I	
				REF DES	1	IC59,		*
16	5	EA		2899528	-00	INTEGRATED CIRCUIT DIGITAL TTL 555 * TIMER	A	
				REF DES	1	IC81,IC87,IC90,IC93, IC96,		*
17	4	EA		2892053	-00	INTEGRATED CIRCUIT DIGITAL TTLS 74S175 * FF QUAD D	A	
				REF DES	1	IC65,IC66,IC72,IC73,		*
18	3	EA		2892082	-00	INTEGRATED CIRCUIT DIGITAL TTLS 74S153 * MUX 4 INPUT	A	
				REF DES	1	IC35-IC37,		*
19	2	EA		3013476	-00	INTEGRATED CIRCUIT TTLS 74S51 * GT AOI	A	
				REF DES	1	IC18,IC19,		*
20	1	EA		2899868	-00	INTEGRATED CIRCUIT DIGITAL TTLS 74S124 * OSC DUAL	A	
				REF DES	1	IC58,		*
21	6	EA		3013355	-00	INTEGRATED CIRCUIT-IC192 TTLH 74H21 * GT AND 4IN	I	
				REF DES	1	IC53,IC54,IC61,IC62, IC67,IC69,		*
22	16	EA		3013515	-00	INTEGRATED CIRCUIT TTLLS 74LS51 * GT AOI	A	
				REF DES	1	IC1-IC3,IC7,IC9,IC11, IC13,IC15,IC16,IC17, IC21,IC23,IC25,IC27,		*
					4	IC40,IC42		*

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PARTS LIST

MFG CODE	ISSUE DATE	CONTROL	CA	TYPE	COMM CODE	ST	PL	DOC NO	SHEET	PL REV
J N	10/13/80	M777		M		A	PL	W 4400914	3	L

TITLE: PC ASSY - MEMORY SEMICONDUCTOR

CL	U/M	AC	DOC SIZE	RANGE THRU	ISSUE	PIC REV
A	EA	3	C			C

FIND NO	QUANTITY REQUIRED	U/M	SIZE	PART OR IDENT NO DOCUMENT NO.	DASH	NOMENCLATURE OR DESCRIPTION	SP	CHG
23	4	EA		3013503	-00	INTEGRATED CIRCUIT TTLLS 74LS04 * GT HEX INVERT	A	
				REF DES	1	IC29-IC31,IC41,		*
24	1	EA		3013500	-00	INTEGRATED CIRCUIT TTLLS 74LS00 * GT NAND 2IN	A	
				REF DES	1	IC86,		*
25	11	EA		3013472	-00	INTEGRATED CIRCUIT - IC208 TTLS 74S140 * GT DRV 4IN	I	
				REF DES	1	IC48,IC55,IC56,IC63, IC70,IC76,IC77,IC82, IC84,IC88,IC94,		*
28	1	EA		8000034	-10	INTEGRATED CIRCUIT-1.5 AMP POSTTL DS340 VOLT REG 12V	A	
				REF DES	1	Q8,		*
30	1	EA	W	7600026	-00	TRANSISTOR PNP VCBO 60V 120MW BETA40	A	
				REF DES	1	Q7,		*
31	4	EA	W	7601046	-00	TRANSISTOR R097A CASE	A	
				REF DES	1	Q1,Q2,Q9,Q10		*
32	3	EA		2899749	-00	TSTR PNP VCBO 60V 400MW BETA50	A	
				REF DES	1	Q3,Q5,Q6		*
33	1	EA	W	7600020	-00	TRANSISTOR PNP VEBO 5V 400MW BETA35	A	
				REF DES	1	Q4,		*
34	2	EA	W	0400803	-00	BOARD STIFFENER	A	
35	1	EA		2899785	-12	CAP VAR CER DIEL PL 250V 25 PF= 5 PF	A	
				REF DES	1	C114,		*
36	1	EA	W	6901500	101	CAPACITOR, FIXED, MICA DIEL 100 PF 5% 500VDC	A	
				REF DES	1	C113,		*
37	3	EA	W	6901500	201	CAPACITOR, FIXED, MICA DIEL 200 PF 5% 500VDC	A	
				REF DES	1	C105,C108,C109,		*
38	1	EA	W	6901500	241	CAPACITOR, FIXED, MICA DIEL 240 PF 5% 500VDC	A	
				REF DES	1	C110,		*
39	1	EA	W	6901500	270	CAPACITOR, FIXED, MICA DIEL 27 PF 5% 500VDC	A	

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PARTS LIST

MFG CODE	ISSUE DATE	CONTROL	CA	TYPE	COMM. CODE	ST	DOC NO	SHT	PL REV
J W	10/13/80	W777		M		A	PL W 4400914	4	L

TITLE: PC ASSY - MEMORY SEMICONDUCTOR

CL	U/M	AC	DOC SIZE	RANGE	THRU	ISSUE	PIC REV
A	EA	3	C				C

FIND NO	QUANTITY REQUIRED	U/M	SIZE	PART OR IDENT NO		NOMENCLATURE OR DESCRIPTION	SP	CHG
				DOCUMENT NO	DASH			
				REF DES	1	C111,		*
40	1	EA	W	6901500	301	CAPACITOR, FIXED, MICA DIEL 300 PF 5% 500VDC	A	
				REF DES	1	C112,		*
42	80	EA	W	7100004	101	CAPACITOR, FIXED, CERAMIC DIEL1.0 UF +80%, -20%	A	*
				REF DES	1	C1,C2,C26-C73,C78, C80,C81,C83-C104, C106,C115,C120,C123,		*
					4	C133,		*
43	2	EA	W	7100004	151	CAPACITOR, FIXED, CERAMIC DIEL1.5 UF +80%, -20%	A	
				REF DES	1	C117,C131,		*
44	6	EA	W	7100200	107	CAPACITOR, FXD, TANTALUM DIEL 100 UF 10% 20V	A	
				REF DES	1	C116,C126-C130,		*
45	3	EA	W	7100200	476	CAPACITOR, FXD, TANTALUM DIEL 47 UF 10% 20V	A	
				REF DES	1	C119,C122,C132,		*
46	19	EA	W	7701017	-00	DIODE, 200MA	A	
				REF DES	1	CR1-CR4,CR6,CR7,CR9- CR16,CR18,CR19,		*
47	2	EA		4915496	-08	SEMICONDUCTOR DEV,DIODE, ZENER 5.10V NOM 5% 400MW PWR DIS	A	
				REF DES	1	CR8,CR17,		*
48	1	EA	W	7800104	-03	SWITCH, TOGGLE, ROCKER SPST ON NONE OFF 1A 40VDC	A	
				REF DES	1	A1,		*
49	3	EA	W	6502500	102	RES,FXD,COMPOSITION,1/4W,5% 1000 OHMS	A	
				REF DES	1	R127,R130,R144,		*
50	2	EA	W	6502500	820	RES,FXD,COMPOSITION,1/4W,5% 82 OHMS	A	
				REF DES	1	R126,R138,		*
51	1	EA	W	6502500	391	RES,FXD,COMPOSITION,1/4W,5% 390 OHMS	A	
				REF DES	1	R123,		*
52	1	EA	W	6502500	512	RES,FXD,COMPOSITION,1/4W,5% 5100 OHMS	A	
				REF DES	1	R15,		*

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PARTS LIST

MFG CODE	ISSUE DATE	CONTROL	CA	TYPE	COMM. CODE	ST	DOC NO	SHEET	PL REV
J M	10/13/80	M777		M		A	PL W 4400914	5	L

TITLE: PC ASSY - MEMORY SEMICONDUCTOR

CL	U/M	AC	DOC SIZE	RANGE THRU	ISSUE	PIC REV
A	EA	3	C			C

FIND NO	QUANTITY REQUIRED	U/M	SIZE	PART OR IDENT NO DOCUMENT NO	DASH	NOMENCLATURE OR DESCRIPTION	SP	CHG
53	1	EA		W 6502500	750	RES,FXD,COMPOSITION,1/4W,5% 75 OHMS	A	
				REF DES	1	R133,		*
54	1	EA		W 6000011	-47	RESISTOR, FIXED, WIRE WOUND 2W 5% 22	A	
				REF DES	1	R128,		*
55	1	EA		W 5700353	-08	CONN, PRINTED CIRCUIT, ELEC 9 PINS	A	
				REF DES	1	J1,		*
56	1	EA		W 6400017	502	RESISTOR, ADJBL, CERAMIC-PLSTC5K	A	
				REF DES	1	R16,		*
57	64	EA		W 6600042	-00	RESISTOR, FIXED, COMPOSITION .12W 5% 33	A	
				REF DES	1	R29-R31,R33,R35,R37, R39,R41,R75-R122, R145-R152		*
58	34	EA		W 6600042	-01	RESISTOR, FIXED, COMPOSITION .12W 5% 47	A	
				REF DES	1	R44,R46,R48,R50,R52, R54,R56,R58,R60,R62, R64,R66,R68,R70,R72,		*
					4	R74,R158-R175,		*
59	2	EA		W 6600042	-03	RESISTOR, FIXED, COMPOSITION .12W 5% 200	A	*
				REF DES	1	R20,R22,		*
60	4	EA		W 6600042	-04	RESISTOR, FIXED, COMPOSITION .12W 5% 300	A	
				REF DES	1	R19,R21,R23,R143,		*
61	4	EA		W 6600042	-05	RESISTOR, FIXED, COMPOSITION .12W 5% 1K	A	
				REF DES	1	R3,R125,R137,R141,		*
62	2	EA		W 6600042	-06	RESISTOR, FIXED, COMPOSITION .12W 5% 1.2K	A	
				REF DES	1	R24,R25,		*
63	3	EA		W 6600042	-07	RESISTOR, FIXED, COMPOSITION .12W 5% 1.8K	A	
				REF DES	1	R13,R124,R136,		*
64	1	EA		W 6600042	-08	RESISTOR, FIXED, COMPOSITION .12W 5% 2.0K	A	
				REF DES	1	R132,		*
65	1	EA		W 6600042	-09	RESISTOR, FIXED, COMPOSITION .12W 5% 2.4K	A	

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PARTS LIST

MFG CODE	ISSUE DATE	CONTROL	CA	TYPE	COMM CODE	ST	PL	DOC NO	SHEET	PL REV
J W	10/13/80	W777		M		A	PL	W 4400914	6	L

TITLE	CL	U/M		AC	DOC SIZE	RANGE THRU	ISSUE	PIC REV
PC ASSY - MEMORY SEMICONDUCTOR	A	EA		3	C			C

FIND NO	QUANTITY REQUIRED	U/M	SIZE	PART OR IDENT NO DOCUMENT NO	DASH	NOMENCLATURE OR DESCRIPTION	SP	CHG
				REF DES	1	R5,		*
66	1	EA	W	6600042	-10	RESISTOR, FIXED, COMPOSITION .12W 5% 3.6K	A	
				REF DES	1	R131,		*
67	2	EA	W	6600042	-11	RESISTOR, FIXED, COMPOSITION .12W 5% 4.7K	A	
				REF DES	1	R4,R10		*
68	30	EA	W	6600042	-12	RESISTOR, FIXED, COMPOSITION .12W 5% 5.1K	A	
				REF DES	1	R1,R2,R7,R11,R28,R32, R34,R36,R38,R40,R43, R45,R47,R49,R51,R53,		*
					4	R55,R57,R59,R61,R63, R65,R67,R69,R71,R73, R129,R139,R140,R142,		*
69	1	EA	W	6600042	-13	RESISTOR, FIXED, COMPOSITION .12W 5% 5.6K	A	
				REF DES	1	R9,		*
70	1	EA	W	6600042	-14	RESISTOR, FIXED, COMPOSITION .12W 5% 20K	A	
				REF DES	1	R6,		*
71	3	EA	W	6600042	-15	RESISTOR, FIXED, COMPOSITION .12W 5% 75K	A	
				REF DES	1	R8,R12,R17,		*
72	18	EA		4916657	-06	CAP FXD CER DIEL 50V +80 - 20% 100K PF	A	
				REF DES	1	C10,C11,C13-C24,C74- C77,		*
73	1	EA	W	7001000	183	CAPACITOR FXD METZD PLSTC DIEL.018 UF	A	
				REF DES	1	C107,		*
75	15	EA	W	5800066	-02	TERMINAL, STUD .063 DIA .084 LG .062 HD THK	A	
				REF DES	1	TP1-TP15,		*
76	1	EA	W	6200000	-07	FUSE LINK, THERMAL 2AMP	A	
				REF DES	1	F1,		*
77	1	EA	W	6502500	622	RES,FXD,COMPOSITION,1/4W,5% 6200 OHMS	A	
				REF DES	1	R14,		*
78	1	EA	W	7602222	-00	TRANSISTOR,NPN NPN VCBO 30V 500MW BETA50	A	
				REF DES	1	Q11,		*

SPERRY UNIVAC — SPERRY UNIVAC IS A DIVISION OF SPERRY RAND CORP.

PARTS LIST

MFG CODE	ISSUE DATE	CONTROL	CA	TYPE	COMM CODE	ST	DOC NO	SHEET	PL REV
J W	10/13/80	W777		M		A	PL W 4400914	7	L

TITLE: PC ASSY - MEMORY SEMICONDUCTOR

CL	U/M	AC	DOC SIZE	RANGE THRU	ISSUE	PIC REV
A	EA	3	C			C

FIND NO	QUANTITY REQUIRED	U/M	SIZE	PART OR IDENT NO DOCUMENT NO	DASH	NOMENCLATURE OR DESCRIPTION	SP	CHG
79	1	EA		9800216	-00	SEMICONDUCTOR DEVICE DIODE SILICON RECTIFIER 100PRV 1AMP	A	
				REF DES	1	CR20,		*
80	1	EA		4915496	-21	SEMICONDUCTOR DEV,DIODE, ZENER 16.00V NOM 5% 400MW PWR DIS	A	
				REF DES	1	CR21,		*
81	2	EA		3012137	-11	SEMICONDUCTOR DEV,DIODE,ZENER 8.20V NOM 5% 5W PL DSPN	2A	
				REF DES	1	CS22,CS23,		*
82	1	EA	W	7900017	-00	INSULATOR, MICA .002 THK FOR TO-3	A	
83	1	EA	W	6600042	-16	RESISTOR, FIXED, COMPOSITION .12W 5% 510	A	
				REF DES	1	R176,		*
84	1	EA		6601254	-00	PC ASSY-PIGGYBACK SEMICOND MEM	A	*
F01		X	W	9100661	-02	LOGIC MEMORY SEMICONDUCTER	A	*
S01		X		SW01163	-00	MARKING,MECHANICAL SPECS DSGN-F/GENERAL IDENTIFICATION	A	*
S02		X		SW00536	-00	THREADED FASTENERS SPECS DSGN-SELECTION-INSTALLATION	A	*
S03		X		SW01159	-00	PRINTED CIRCUIT BOARD SPECS PRCS- JUMPER INSTALLATION	A	*
**********						64K WITHOUT PARITY * VARIABLE DATA - 00**********		
29	256	EA	W	4900491	-00	INTEGRATED CIRCUIT, MEMORY MOS 4027 *RAM 4096X1	A	
				REF DES	1	IC100-IC115,IC200- IC215,IC300-IC315, IC400-IC415,IC500-		*
					4	IC515,IC600-IC615, IC700-IC715,IC800- IC815,IC900-IC915,		*
					7	IC1000-IC1015,IC1100- IC1115,IC1200-IC1215, IC1300-IC1315,IC1400-		*
					10	IC1415,IC1500-IC1515, IC1600-IC1615,		*
41	279	EA		6630012	-05	CAPACITOR, FIXED, CERAMIC DIEL .010 UF,50VDC,+80%,-20%	A	*
				REF DES	1	C3,C4,C7,C8,C9,C118, C121,C124,C125,C135- C404,		*
74	288	EA	W	5800195	-10	IC SOCKET 16 PIN	A	
**********						64K WITH PARITY * VARIABLE DATA - 01**********		
29	288	EA	W	4900491	-00	INTEGRATED CIRCUIT, MEMORY MOS 4027 *RAM 4096X1	A	
				REF DES	1	IC100-IC115,IC200- IC215,IC300-IC315, IC400-IC415,IC500-		*

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PARTS LIST

MFG CODE	ISSUE DATE	CONTROL	CA	TYPE	COMM. CODE	ST	DOC NO	SHEET	PL REV
J W	10/13/80	W777		M		A	PL W 4400914	8	L

TITLE: PC ASSY - MEMORY SEMICONDUCTOR

CL	U/M	AC	DOC SIZE	RANGE THRU	ISSUE	PIC REV
A	EA	3	C			C

FIND NO	QUANTITY REQUIRED	U/M	SIZE	PART OR IDENT NO DOCUMENT NO	DASH	NOMENCLATURE OR DESCRIPTION	SP	CHG
					4	IC515,IC600-IC615, IC700-IC715,IC800- IC815,IC900-IC915,		*
					7	IC1000-IC1015,IC1100- IC1115,IC1200-IC1215, IC1300-IC1315,IC1400-		*
					10	IC1415,IC1500-IC1515, IC1600-IC1615,IC116, IC117,IC216,IC217,		*
					13	IC316,IC317,IC416, IC417,IC516,IC517, IC616,IC617,IC716,		*
					16	IC717,IC816,IC817, IC916,IC917,IC1016, IC1017,IC1116,IC1117,		*
					19	IC1216,IC1217,IC1316, IC1317,IC1416,IC1417, IC1516,IC1517,IC1616,		*
					22	IC1617,		*
41	279	EA		6630012	-05	CAPACITOR, FIXED, CERAMIC DIEL ,010 UF,50VDC,+80%,-20%	A	*
				REF DES	1	C3,C4,C7,C8,C9,C118, C112,C124,C125,C135- C404,		*
74	288	EA		W 5800195	-10	IC SOCKET 16 PIN	A	
**********						*32K WITHOUT PARITY * VARIABLE DATA - 02**********		
29	128	EA		W 4900491	-00	INTEGRATED CIRCUIT, MEMORY MOS 4027 *RAM 4096X1	A	
				REF DES	1	IC100-IC115,IC200- IC215,IC300-IC315, IC400-IC415,IC500-		*
					4	IC515,IC600-IC615, IC700-IC715,IC800- IC815		*
41	153	EA		6630012	-05	CAPACITOR, FIXED, CERAMIC DIEL ,010 UF,50VDC,+80%,-20%	A	*
				REF DES	1	C3,C4,C7,C8,C9,C118, C121,C124,C125,C135- C198,C255,C334		*
74	144	EA		W 5800195	-10	IC SOCKET 16 PIN	A	
**********						*32K WITH PARITY * VARIABLE DATA - 03**********		
29	144	EA		W 4900491	-00	INTEGRATED CIRCUIT, MEMORY MOS 4027 *RAM 4096X1	A	
				REF DES	1	IC100-IC115,IC200- IC215,IC300-IC315, IC400-IC415,IC500-		*
					4	IC515,IC600-IC615, IC700-IC715,IC800- IC815,IC116,IC117,		*
					7	IC216,IC217,IC316, IC317,IC416,IC417, IC516,IC517,IC616,		*
					10	IC617,IC716,IC717, IC816,IC817,		*
41	153	EA		6630012	-05	CAPACITOR, FIXED, CERAMIC DIEL ,010 UF,50VDC,+80%,-20%	A	*
				REF DES	1	C3,C4,C7,C8,C9,C118, C121,C124,C125,C135- C198,C255-C334		*
74	144	EA		W 5800195	-10	IC SOCKET 16 PIN	A	

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PARTS LIST

MFG CODE	ISSUE DATE	CONTROL	CA	TYPE	COMM CODE	ST	PL	DOC NO	SHT	PL REV
J W	10/13/80	W777		M		A	PL	W 4400914	9	L

TITLE: PC ASSY - MEMORY SEMICONDUCTOR

CL	U/M		AC	DOC SIZE	RANGE	THRU	ISSUE	PIC REV
A	EA		3	C				C

FIND NO	QUANTITY REQUIRED	U/M	SIZE	PART OR IDENT NO DOCUMENT NO	DASH	NOMENCLATURE OR DESCRIPTION	SP	CHG
**********	**********	**********	**********	**********	**********	*16K WITHOUT PARITY * VARIABLE DATA = 04**********	***	
29	64	EA		W 4900491	-00	INTEGRATED CIRCUIT, MEMORY MOS 4027 *RAM 4096X1	A	
				REF DES	1	IC100-IC115,IC200- IC215,IC300-IC315, IC400-IC415,		*
41	81	EA		6630012	-05	CAPACITOR, FIXED, CERAMIC DIEL ,010 UF,50VDC,+80%,-20%	A	*
				REF DES	1	C3,C4,C7,C8,C9,C118, C121,C124,C125,C135- C166,C255-C294,		*
74	72	EA		W 5800195	-10	IC SOCKET 16 PIN	A	
**********	**********	**********	**********	**********	**********	*16K WITH PARITY * VARIABLE DATA = 05**********	***	
29	72	EA		W 4900491	-00	INTEGRATED CIRCUIT, MEMORY MOS 4027 *RAM 4096X1	A	
				REF DES	1	IC100-IC115,IC200- IC215,IC300-IC315, IC400-IC415,IC116,		*
					4	IC117,IC216,IC217, IC316,IC317,IC416, IC417,		*
41	81	EA		6630012	-05	CAPACITOR, FIXED, CERAMIC DIEL ,010 UF,50VDC,+80%,-20%	A	*
				REF DES	1	C3,C4,C7,C8,C9,C118, C121,C124,C125,C135- C166,C255-C294		*
74	72	EA		W 5800195	-10	IC SOCKET 16 PIN	A	

SPERRY UNIVAC

SPERRY UNIVAC IS A DIVISION OF SPERRY RAND CORP.

PARTS LIST

MFG. CODE	ISSUE D	CONTROL	CA	TYPE	COMM. CODE	ST	DOC NO	T	PL REV
J W	10/15/79	W777		M		A	PL W 0101095	1	F

TITLE I/O EXPANDER OPTION

CL	U/M	AC	DOC SIZE	RANGE	THRU	ISSUE	PIC REV
A	EA	6	A				D

FIND NO	QUANTITY REQUIRED	U/M	SIZE	PART OR IDENT. NO. DOCUMENT NO.	DASH	NOMENCLATURE OR DESCRIPTION		SP	CHG
Z06				W-87474	-27	PL REV F, PIC REV D, RANGE 00 - 03 EIR RELEASED 10/15/79			
**********						********** COMMON DATA **********			
1	1	EA		W 4400670	-00	PC ASSEMBLY - SERIES I/O EXPANDER		A	*
7	AR	IN		W 5300453	-50	WIRE,STR,TWISTED PAIR,I.P,V.C,30 AWG BLACK & GREEN		A	*
8	AR	EA		W 9000007	-00	POTTING COMPOUND		A	*
F01		X		W 9100435	-00	LOGIC DIAGRAM - SERIES I/O EXPANDER		A	*
S01		X		SW01163	-00	MARKING SPEC	PART IDENTIFICATION	A	*
S02		X		SW00830	-00	TEST SPECIFICATION	I/O EXPANDER OPTION	A	*
S03		X		SW01169	-00	HARDWARE PERFORMANCE SPEC	SERIES I/O EXPANDER (DM394)	A	*
**********						*SEE TABULATION ON DRAWING	* VARIABLE DATA - 00**********		
2	1	EA		W 5300537	-60	CABLE ASSY, I/O EXPANDER		A	*
**********						*SEE TABULATION ON DRAWING	* VARIABLE DATA - 01**********		
3	1	EA		W 5300650	-60	CABLE ASSY, I/O EXPANDER		A	*
**********				F3036-00	*****	*SEE TABULATION ON DRAWING	* VARIABLE DATA - 02**********		
4	1	EA		W 5300665	-00	I/O EXPANDER OPTION CABLE		A	*
5	1	EA		W 4400664	-02	PC ASSEMBLY - TERM SHOE DM389	NORMAL I/O AND HIGH SPEED DMA	A	*
**********				F3036-01	*****	*SEE TABULATION ON DRAWING	* VARIABLE DATA - 03**********		
4	1	EA		W 5300665	-00	I/O EXPANDER OPTION CABLE		A	*
6	1	EA		W 0101954	-00	TERMINATOR OPTION	1 TERMINATOR	A	*

REVISIONS					
REV	PN	CHG NOTE	DESCRIPTION	APPROVED	DATE
X1	—	—	PROTOTYPE RELEASE		9/3/74
A	81342	—	PRODUCTION RELEASE		10/3/74

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. THIS DRAWING CONSISTS OF THE FOLLOWING SHEETS: 1.0, 2.0, 3.0, 4.0, 5.0, 6.0, 7.0

2. ALL RESISTOR VALUES ARE IN OHMS 1/4W ± 5%

TABLE OF CONTENTS

DESCRIPTION	SHEET NO.
POWER AND GROUND DISTRIBUTION AND DECOUPLING	3.0
CONNECTOR FUNCTION	4.0
I/O BUS TERMINATION & PRIORITY LOOKAHEAD LOGIC	5.0
RTC/PIM INTERRUPT ENABLE SENSE LOGIC	6.0, 7.0

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
R13	
E19	
C11	
IC14	
A8	

REFERENCE DRAWINGS	
44D0718	ASSEMBLY
44P0718	PARTS LIST
40D0580	P.W. BOARD
97D0714	ARTWORK
97D0715	SOLDERMASK

DR	Mancanelli	8-8-74
CHK		9/27/74
DSGN		
ENGR		9/30/74
APPD		9/30/74
APPD		

varian data machines /a varian subsidiary
2722 michelson drive / irvine / california / 92664

TITLE
LOGIC DIAGRAM
TERMINATOR SHOE, DM389-1

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0491	A

SCALE | SHEET 1.0

4 3 2 1

D C B A

CONNECTOR P1

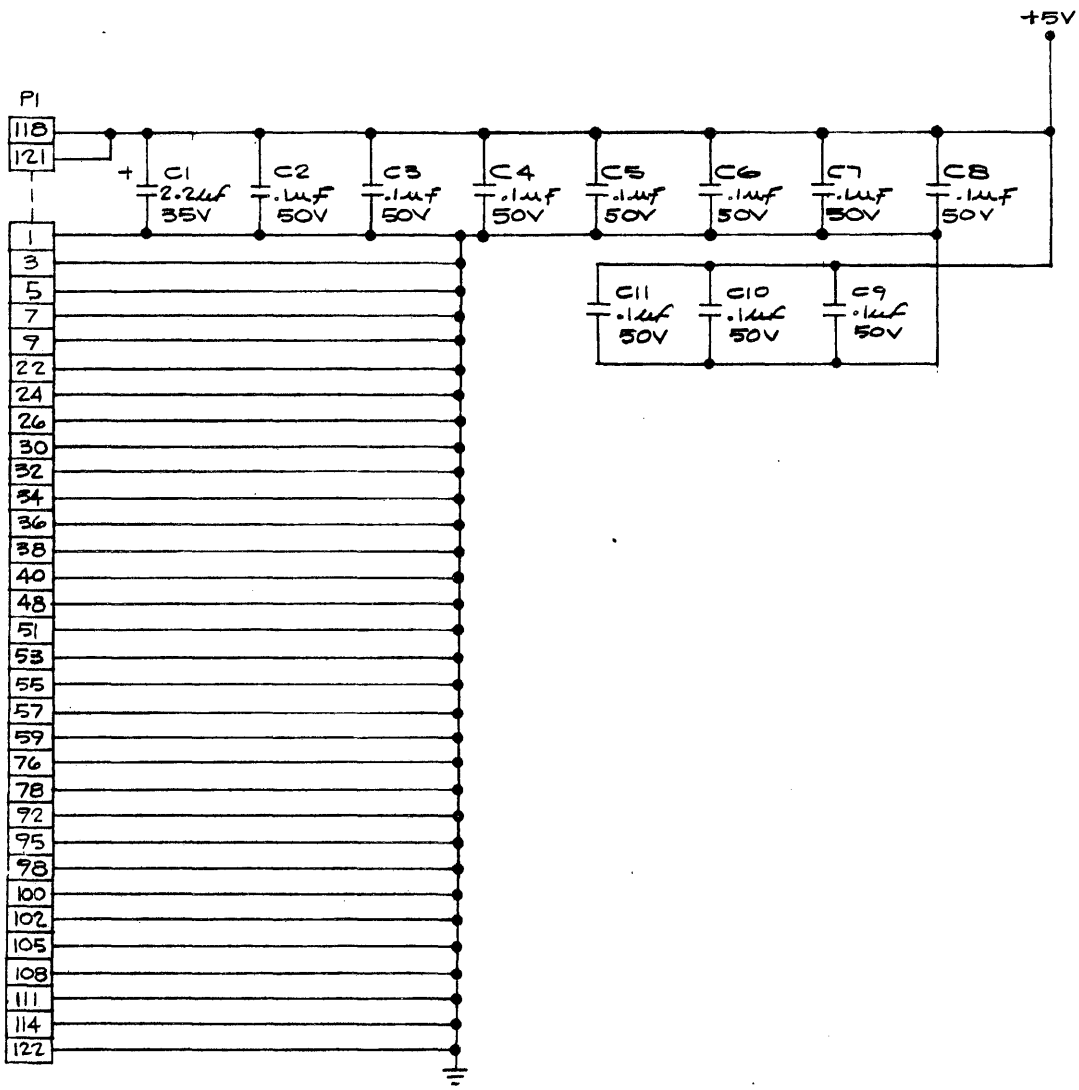
PIN	FUNCTION	SHEET
1	GND	3.0
2	EB00-I	4.0
3	GND	3.0
4	EB01-I	4.0
5	GND	3.0
6	EB02-I	4.0
7	GND	3.0
8	EB03-I	4.0
9	GND	3.0
10	EB04-I	4.0
11	EB05-I	4.0
12	EB06-I	4.0
13	EB07-I	4.0
14	EB08-I	4.0
15	EB09-I	4.0
16	EB10-I	4.0
17	EB11-I	4.0
18	EB12-I	4.0
19	EB13-I	4.0
20	EB14-I	4.0
21	EB15-I	4.0
22	GND	3.0
23		
24	GND	3.0
25		
26	GND	3.0
27	FRYX-I	4.0
28		
29	DRYX-I	4.0
30	GND	3.0
31	SERX-I	4.0
32	GND	3.0
33	TPIX-I	4.0
34	GND	3.0
35	TPØX-I	4.0
36	GND	3.0
37		
38	GND	3.0
39		
40	GND	3.0
41		
42		
43	SYRT-I	4.0
44	IUAX-I	4.0
45	IUCX-I	4.0
46	IURX-I	4.0
47	IUJX-I	4.0
48	GND	3.0
49		
50		
51	GND	3.0
52		
53	GND	3.0
54		
55	GND	3.0
56		
57	GND	3.0
58		
59	GND	3.0
60		
61		

CONNECTOR P1

PIN	FUNCTION	SHEET
62		
63		
64		
65		
66		
67		
68		
69		
70		
71		
72		
73		
74		
75		
76	GND	3.0
77		
78	GND	3.0
79		
80		
81		
82		
83		
84		
85		
86		
87		
88		
89		
90	TPIF-I	5.0
91	TPØF-I	5.0
92	GND	3.0
93	BIMES-I	5.0
94	BTMES-I	5.0
95	GND	3.0
96	N/U	5.0
97	N/U	5.0
98	GND	3.0
99	N/U	5.0
100	GND	3.0
101	N/U	5.0
102	GND	3.0
103	IUCF-I	5.0
104	IUAF-I	5.0
105	GND	3.0
106	FRYF-I	5.0
107	DRYF-I	5.0
108	GND	3.0
109	IØK1-I	5.0
110	IØK2-I	5.0
111	GND	3.0
112	IØK3-I	5.0
113	IØK4-I	5.0
114	GND	3.0
115	DAGS	4.0
116		
117		
118	+5V	3.0
119		
120		
121	+5V	3.0
122	GND	3.0

CONNECTOR FUNCTION

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9IC0491	A
SCALE		SHEET 2.0	

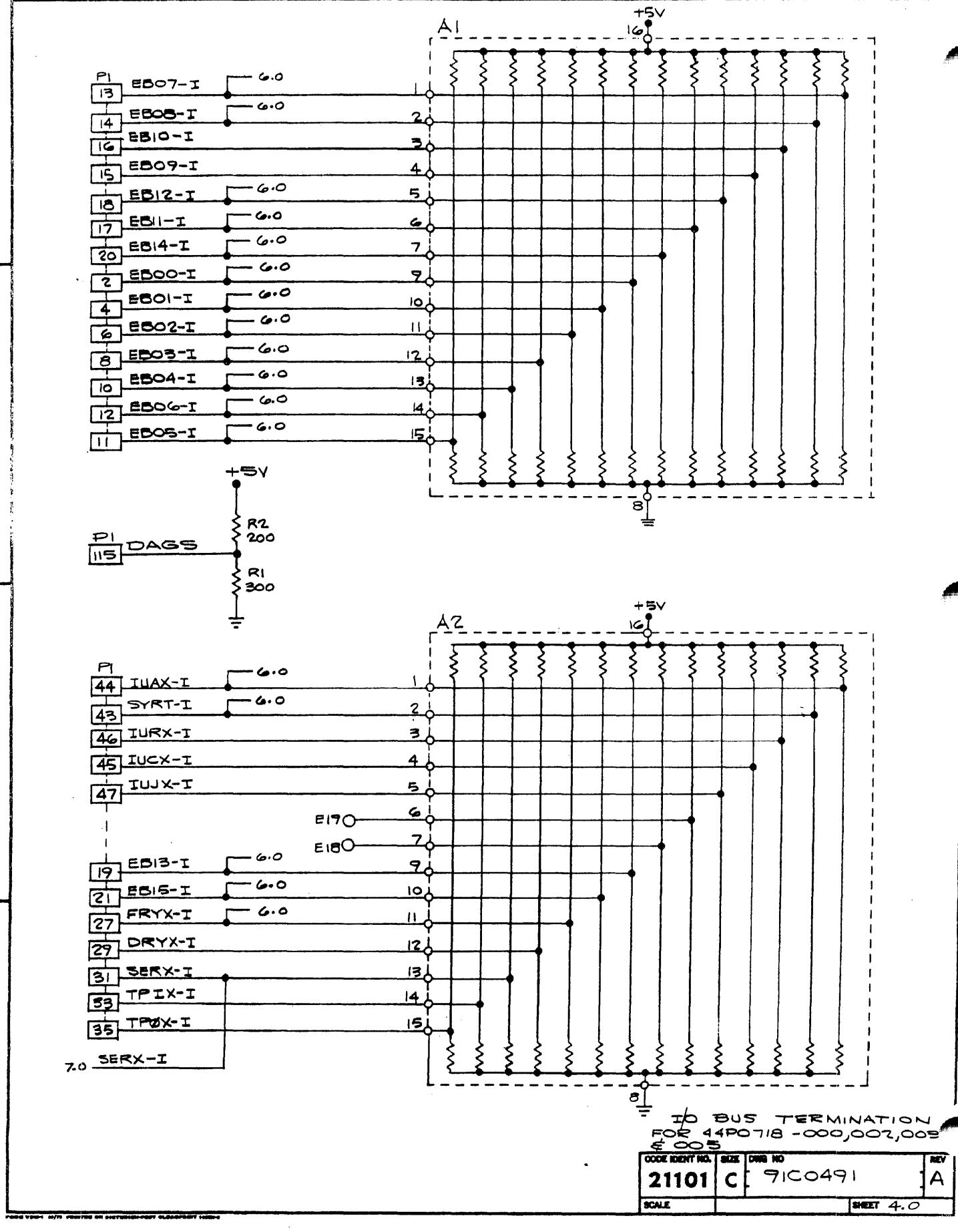


1. FOR ALL 14 PIN IC'S, PWR & GRD DISTRIBUTION IS; PIN 7 = GRD, PIN 14 = PWR

2. FOR ALL 16 PIN ICS, PWR & GRD DISTRIBUTION IS; PIN 8 = GRD, PIN 16 = PWR

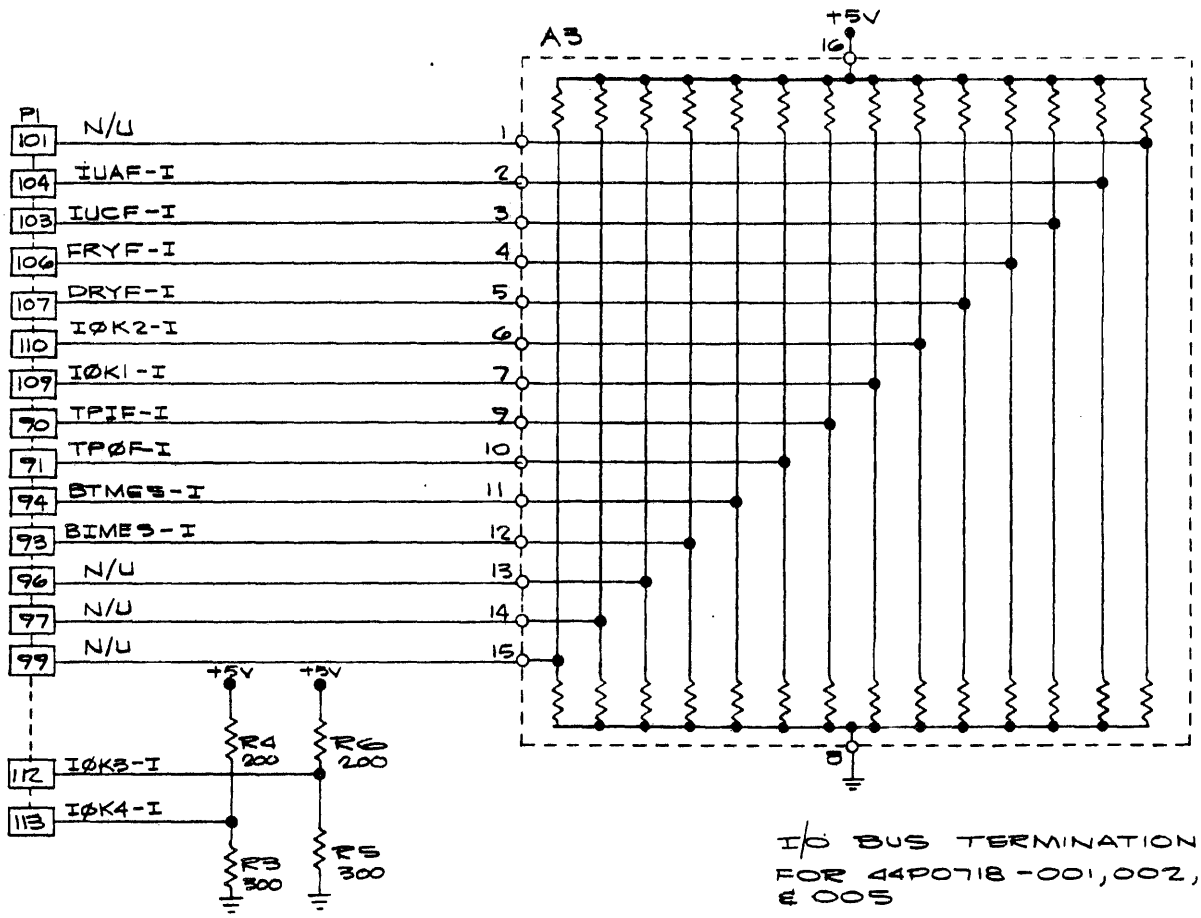
POWER AND GROUND DISTRIBUTION DECOUPLING

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0491	A
SCALE			SHEET 3.0

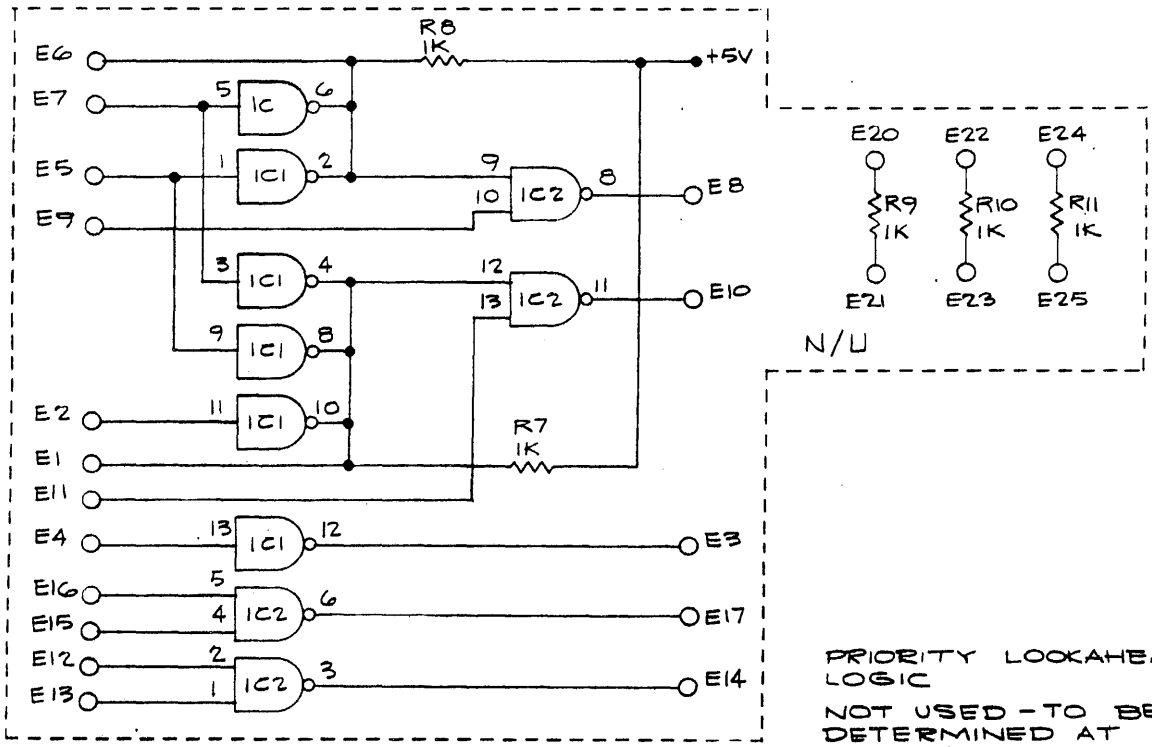


I/O BUS TERMINATION
FOR 44P0718-000,002,005
& 005

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0491	A
SCALE		SHEET 4.0	



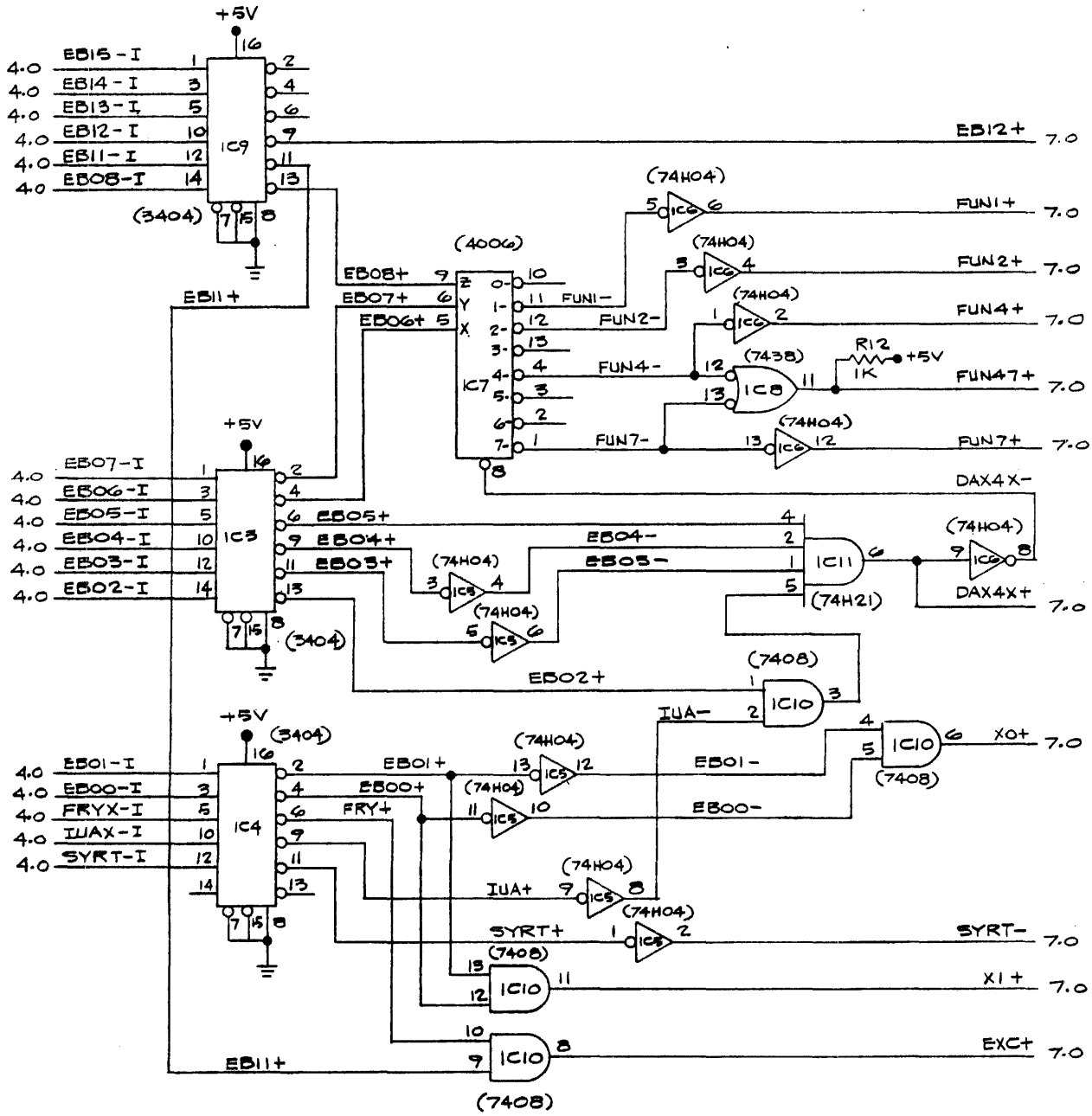
I/O BUS TERMINATION
FOR 44P0718-001,002,004 & 005



PRIORITY LOOKAHEAD LOGIC

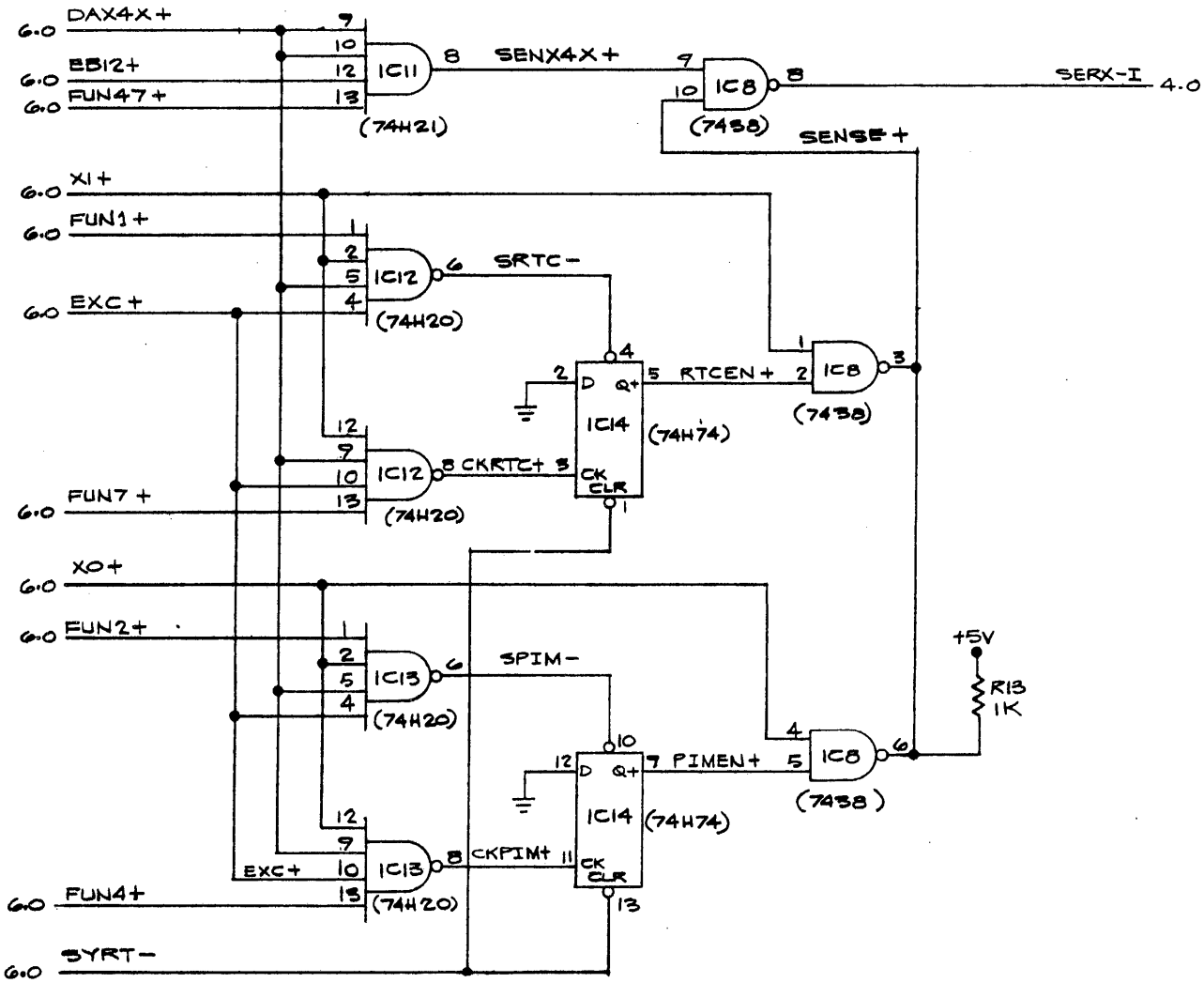
NOT USED - TO BE DETERMINED AT SYSTEM LEVEL

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100491	A
SCALE		SHEET 5.0	



RTC/PIM INTERRUPT ENABLE SENSE LOGIC FOR 44P0718-003,004 & 005

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0491	A
SCALE		SHEET 6.0	



RTC/PIM INTERRUPT ENABLE SENSE LOGIC

FOR 44P0718-003,004 & 005

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0491	A
SCALE		SHEET 7.0	