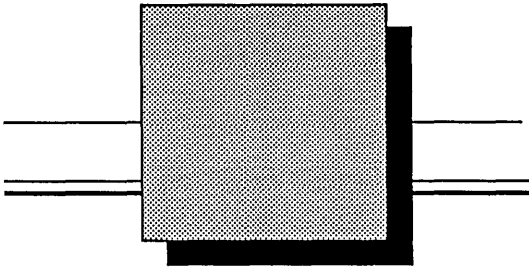

Library Reference Manual

Volume II

October 1, 1989

P/N: 900-00734

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MANUAL REVISION HISTORY

Rev	Date	Software Release	Reason for Change
A	3–10–86	Library Release 7.3	Initial release.
B	6–30–86	Library Release 7.6	Updated libraries to include releases 7.4 and 7.6; added VAXstation II support.
C	10–10–86	Library Release 7.8	Updated libraries to include release 7.8.
D	4–6–87	Library Release 8.4	Updated libraries to include releases 8.0, 8.2, and 8.4; updated PIN_NUMBER property and added platform–specific information for the Sun Workstation.
E	10–1–89	Library Release 9.0	Updated all libraries to include releases 8.6, and 9.0; updated logic array libraries to include release 9.3; added ECL 10KH, ECL ANSI 10KH, FACT, and RCACMOS libraries; added DECstation support.

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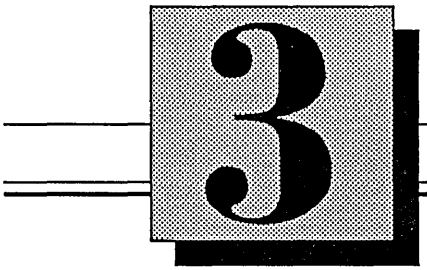
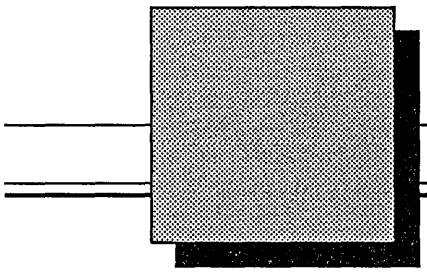
Volume II



54 Series Libraries

This section describes the individual libraries that make up the 54 series libraries. Note that both standard and ANSI body styles are available for all libraries and that the same components are available in each library. The body style selected is determined by the first library name encountered in the library search path or by the last **library** command.

Contents



The 54LSTTL and ANSI 54LSTTL Libraries

The 54LSTTL Library requires approximately 5694 Kbytes of disk storage, and the ANSI 54LSTTL Library requires approximately 5675 Kbytes of disk storage. The physical, timing, and simulation models for each library are identical and differ only in their body drawings. The part name for a component in either library is the same; the body drawing used is determined by the first library name encountered in the library search path (*54lsttl.lib* or *a54lsttl.lib*).

The specifications used to construct the models in these libraries were taken from the Texas Instruments data books or from Mil Spec MIL-M-38510. Parts indicated with an asterisk (*) are from MIL-M-38510; the descriptions for these components include the military device type in parentheses.

The release level of the 54LSTTL and ANSI 54LSTTL Libraries is 9.0.

Each library contains body drawings and physical, timing, and simulation models for the following 155 components:

* **54LS00**	Quad 2-input NAND (30001)
* **54LS02**	Quad 2-input NOR (30301)
* **54LS03**	Quad 2-input open-collector NAND (30002)
* **54LS04**	Hex inverter (30003)
* **54LS05**	Hex open-collector inverter (30004)
* **54LS08**	Quad 2-input AND (31004)
* **54LS09**	Quad 2-input open-collector AND (31005)
* **54LS10**	Triple 3-input NAND (30005)
* **54LS11**	Triple 3-input AND (31001)
* **54LS12**	Triple 3-input open-collector NAND (30006)
* **54LS13**	Dual 4-input NAND Schmitt trigger (31301)
* **54LS14**	Hex Schmitt-trigger inverter (31302)
* **54LS15**	Triple 3-input open-collector AND (31002)
* **54LS20**	Dual 4-input NAND (30007)
* **54LS21**	Dual 4-input AND (31003)
* **54LS22**	Dual 4-input open-collector NAND (30008)
54LS24	Quad 2-input Schmitt-trigger NAND
* **54LS26**	Quad 2-input NAND (32102)
* **54LS27**	Triple 3-input NOR (30302)
* **54LS28**	Quad 2-input NOR (30204)
* **54LS30**	8-input NAND (30009)
* **54LS32**	Quad 2-input OR (30501)
54LS33	Quad 2-input NOR
* **54LS37**	Quad 2-input NAND buffer (30202)
* **54LS38**	Quad 2-input open-collector NAND buffer (30203)

* **54LS40**	Dual 4-input NAND (30201)
* **54LS42**	4-to-10-line decoder (30703)
54LS48	BCD-to-7-segment decoder/driver
* **54LS51**	2-wide 3-input, 2-wide 2-input AND-OR-invert (30401)
* **54LS54**	4-wide AND-OR-invert (30402)
54LS55	2-wide 4-input AND-OR-invert
* **54LS73**	Dual JK flip-flops with clear (30101)
* **54LS74**	Dual positive-edge-triggered D flip-flop (30102)
* **54LS75**	4-bit bistable latch (31601)
* **54LS76**	Dual JK flip-flop with preset and clear (30110
54LS78	Dual JK flip-flop with common clock and clear
* **54LS83**	4-bit binary full adders with fast carry (31201)
* **54LS85**	4-bit magnitude comparator (31101)
* **54LS86**	Quad 2-input exclusive-OR (30502)
* **54LS90**	Decade counter (31501)
54LS91	8-bit shift register
* **54LS92**	4-bit divide-by-12 counter (31510)
* **54LS93**	4-bit binary counter (31502)
* **54LS95**	4-bit shift register (30603)
* **54LS96**	5-bit shift register (30604)
* **54LS107**	Dual JK flip-flops with clear (30108)
* **54LS109**	Dual JKbar positive-edge-triggered flip-flop (30109)
* **54LS112**	Dual JK negative-edge-triggered flip-flop (30103)
* **54LS113**	Dual JK negative-edge-triggered flip-flop with preset (30104)
* **54LS114**	Dual JK negative-edge-triggered flip-flop with preset, common clear and clock (30105)

* **54LS122**	Retriggerable monostable multivibrator with clear (31403)
* **54LS123**	Dual retriggerable monostable multivibrators with clear (31401)
* **54LS125**	Quad bus buffers with three-state outputs (32301)
* **54LS126**	Quad bus buffers with three-state outputs (30104)
* **54LS132**	Quad 2-input positive-NAND Schmitt triggers (30105)
54LS133	13-input positive-NAND gate
54LS136	Quad 2-input exclusive-OR
54LS137	3-to-8 line decoders/multiplexers with address latch
* **54LS138**	3-to-8 line decoders/multiplexers (30701)
* **54LS139**	Dual 2-to-4 line decoders/multiplexers (30702)
54LS145	BCD-to-decimal decoders/drivers
54LS147	10-line decimal to 4-line BCD priority encoder
* **54LS148**	8-line to 3-line octal priority encoder (36001)
* **54LS151**	1-of-8 data selectors/multiplexers (30901)
54LS152	1-of-8 data selectors/multiplexers
* **54LS153**	Dual 4-line-to-1-line data multiplexer (30902)
54LS154	4-to-16 line decoders/demultiplexers
* **54LS155**	Decoders/demultiplexers (32601)
* **54LS157**	Quad 2-to-1-line non-inverting multiplexer (30903)
* **54LS158**	Quad 2-to-1-line inverting data multiplexer (30904)

* **54LS160**	4-bit synchronous decade counters with direct clear (31503)
* **54LS161**	4-bit synchronous binary counters with direct clear (31504)
* **54LS162**	4-bit synchronous decade counters with synchronous clear (31511)
* **54LS163**	4-bit synchronous binary counters with synchronous clear (31512)
* **54LS164**	8-bit parallel output serial shift register (30605)
* **54LS165**	Parallel-load 8-bit shift registers (30608)
* **54LS166**	8-bit shift registers (30609)
* **54LS169**	4-bit synchronous binary up/down counters (31506)
* **54LS170**	4 by 4 register files (31902)
* **54LS173**	4-bit D-type registers with 3-state outputs (36101)
* **54LS174**	Hex D-type flip-flops (30106)
* **54LS175**	Quad D-type flip-flops (30107)
* **54LS181**	Arithmetic logic units/function generators (30801)
54LS182	Look-ahead carry generators
54LS183	Dual carry-save full adders
* **54LS190**	Synchronous BCD up/down counter (31513)
* **54LS191**	Synchronous binary up/down counter (31509)
* **54LS192**	Synchronous BCD up/down dual clock counters (31507)
* **54LS193**	Synchronous binary up/down dual clock counters (31508)
* **54LS194A**	4-bit bidirectional shift register (30601)

* **54LS195**	4-bit parallel-access shift registers (30602)
* **54LS196**	Presettable decade/bi-quinary counters/latches (32001)
* **54LS197**	Presettable binary counters/latches (32002)
54LS219	64-bit random access memory
* **54LS221**	Dual monostable multivibrators (31402)
54LS222	16 x 4 asynchronous first-in first-out memories
* **54LS240**	Octal inverting 3-state bus transceiver (32401)
* **54LS241**	Octal non-inverting 3-state bus transceiver (32402)
* **54LS242**	Quad inverting 3-state bus transceiver (32801)
* **54LS243**	Quad non-inverting 3-state bus transceiver (32802)
* **54LS244**	Octal non-inverting 3-state bus transceiver (32403)
* **54LS245**	Octal non-inverting 3-state bus transceiver (32803)
* **54LS251**	3-state data multiplexer (30905)
* **54LS253**	Dual data selectors/multiplexers (30908)
* **54LS257**	Quad 3-state non-inverting data multiplexer (30906)
* **54LS258**	Quad 3-state inverting data multiplexer (30907)
* **54LS259**	8-bit addressable latches (31603)
54LS260	Dual 5-input NOR
* **54LS266**	Quad 2-input exclusive-NOR gates with open collector (30303)
* **54LS273**	Octal D-type flip-flops (32501)
* **54LS279**	Quad SR latches (31602)
* **54LS280**	9-bit odd/even parity generators/checkers (32901)
* **54LS283**	4-bit binary full adders (31202)
* **54LS290**	Decade counter (32003)
* **54LS293**	4-bit binary counter (32004)

* **54LS295**	4-bit bidirectional universal shift register (30606)
* **54LS298**	Quad 2-input multiplexers with storage (30909)
54LS299	8-bit bidirectional 3-state shift/storage register
54LS322	8-bit shift register with sign extend
54LS323	8-bit bidirectional universal shift/storage registers with 3-state outputs
* **54LS348**	8-line to 3-line priority encoder (36002)
54LS353	Dual 4-line to 1-line data selectors/multiplexers
54LS363	Hex bus drivers
54LS364	Hex bus drivers
* **54LS365**	Hex noninverted 3-state bus drivers (32201)
* **54LS366**	Hex inverted 3-state bus drivers (32202)
* **54LS367**	Hex bus drivers (32203)
* **54LS368**	Hex bus drivers (32204)
* **54LS373**	Octal 3-state D-latch with common enable (32502)
* **54LS374**	Octal 3-state positive-edge-triggered D register (32503)
* **54LS377**	Octal D-type flip-flops with enable (32504)
54LS378	Hex D-type flip-flops
54LS379	Quad D-type flip-flops with enable
54LS381	Arithmetic logic unit/function generator
* **54LS390**	Dual decade counters (32701)
* **54LS393**	Dual 4-bit binary counters (32702)
54LS533	8-bit latch with inverting outputs
* **54LS540**	Octal buffers and line drivers with 3-state outputs (32404
* **54LS541**	Octal buffers and line drivers with 3-state outputs (32405)
54LS590	8-bit binary counters with output registers

54LS592	8-bit binary counter with input registers
54LS593	8-bit binary counter with input registers
54LS640	Octal 3-state inverting bus transceiver
54LS641	Octal open-collector non-inverting bus transceiver
54LS642	Octal open collector inverting bus transceiver
54LS645	Octal 3-state non-inverting bus transceiver
54LS668	Synchronous 4-bit up/down counters
54LS669	Synchronous 4-bit up/down counters
* **54LS670**	4 x 4 register files with 3-state outputs (31901)
54LS671	4-bit 3-state universal shift register/latch
54LS672	4-bit 3-state universal shift register/latch
54LS674	16-bit shift registers
54LS684	8-bit magnitude comparators
54LS693	Synchronous counters with output registers and multiplexed 3-state outputs
54LS699	Synchronous up/down counters with output registers and multiplexed 3-state outputs

Application Notes

Monostable Multivibrators

The 54LS122, 54LS123, and 54LS221 models fully support the simulation and timing behavior of a retrigerrable multivibrator – infinite retriggering edges and external resettability at any time.

To use the simulation model, logic initialization or initial depositing of the same value (either 0 or 1) to internal signals D0 and D1 must be performed.

To use the timing verification model, the following must be observed:

- The Timing Verifier's directives file *(verifier.cmd)* must include the directive:

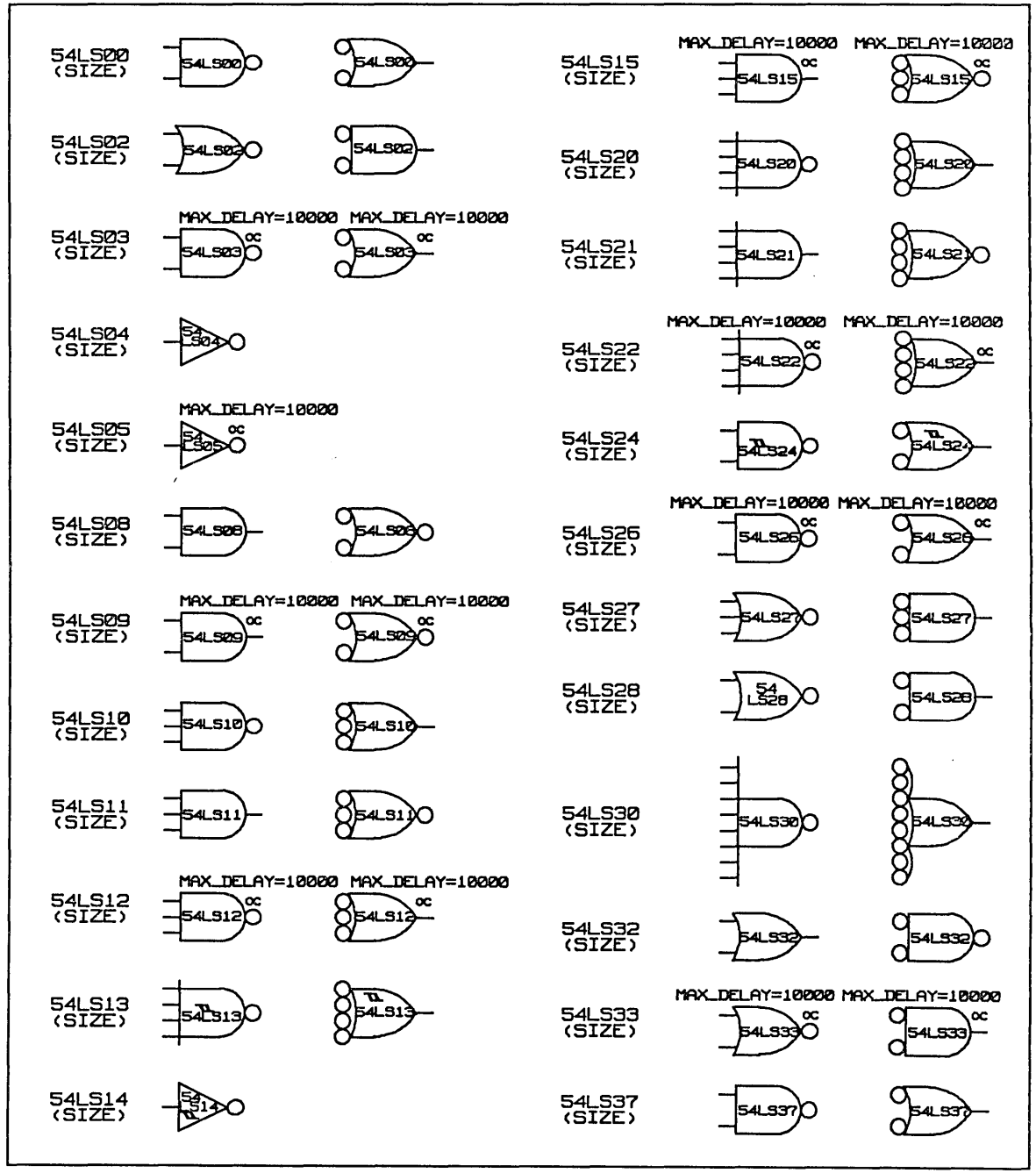
  ```
  LATCH_ERR_MODEL CLOSED;
  ```

- The first trigger edge must occur after 'PULSE_WIDTH' ns.

- The maximum trigger frequency is

  ```
  2 * RETRIG_DIV2 -1
  ```

  edges per 'PULSE_WIDTH' ns. Since RETRIG_DIV2 is defined to be 6 in the model, 2*6–1=11 clock edges are permitted in any 'PULSE_WIDTH' ns interval. If an application requires a greater trigger frequency, RETRIG_DIV2 must be redefined in the model.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54LS02 (SIZE)
MAX_DELAY=10000 MAX_DELAY=10000
54LS03 (SIZE)
54LS04 (SIZE)
MAX_DELAY=10000
54LS05 (SIZE)
54LS08 (SIZE)
MAX_DELAY=10000 MAX_DELAY=10000
54LS09 (SIZE)
54LS10 (SIZE)
54LS11 (SIZE)
MAX_DELAY=10000 MAX_DELAY=10000
54LS12 (SIZE)
54LS13 (SIZE)
54LS14 (SIZE)
MAX_DELAY=10000 MAX_DELAY=10000
54LS15 (SIZE)
54LS20 (SIZE)
54LS21 (SIZE)
MAX_DELAY=10000 MAX_DELAY=10000
54LS22 (SIZE)
54LS24 (SIZE)
MAX_DELAY=10000 MAX_DELAY=10000
54LS26 (SIZE)
54LS27 (SIZE)
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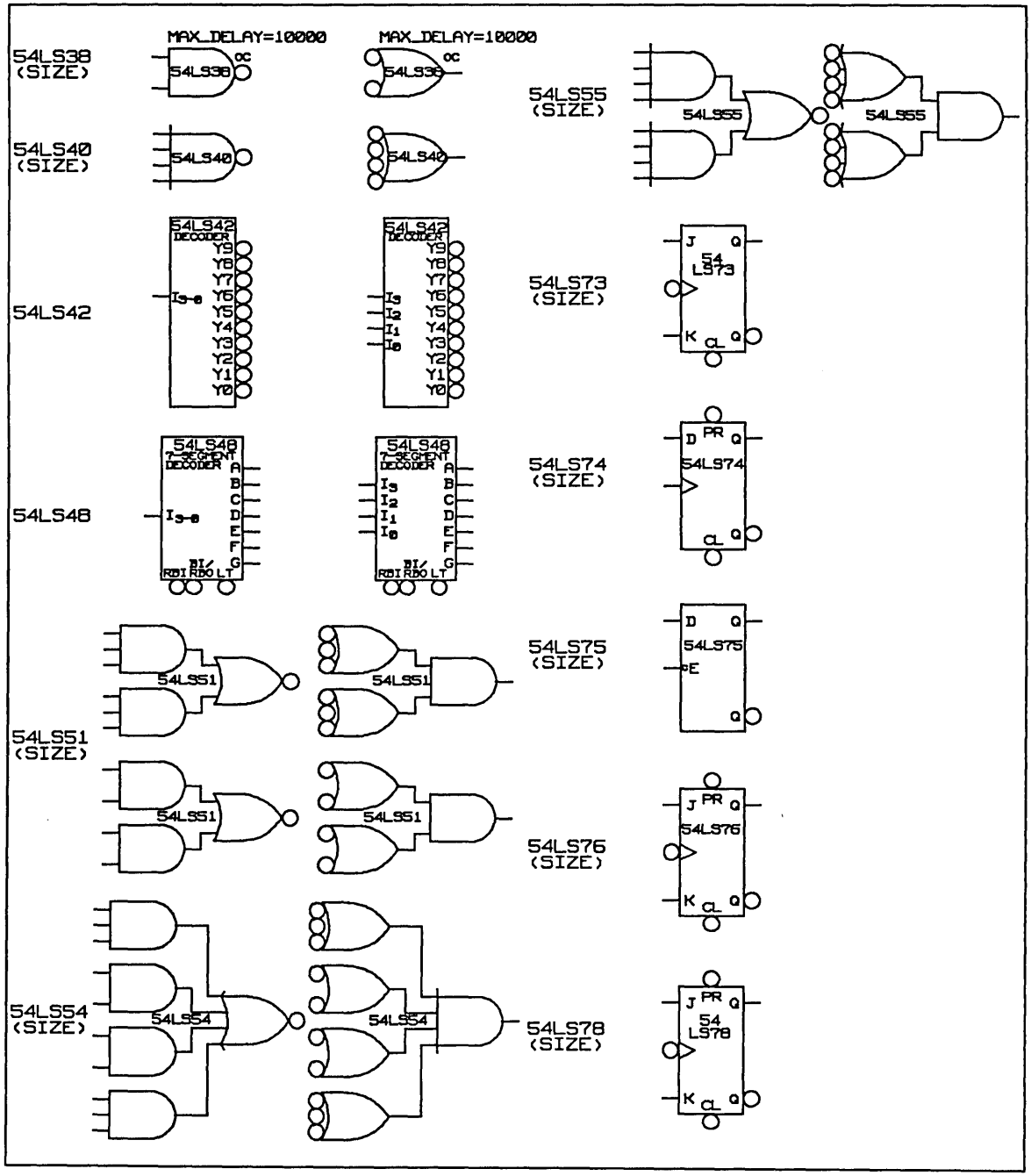
MAX_DELAY=10000 MAX_DELAY=10000
54LS33 (SIZE)
54LS37 (SIZE)


MAX_DELAY=10000
MAX_DELAY=10000
54LS38
(SIZE)
54LS38
54LS38
54LS40
(SIZE)
54LS40
54LS40
54LS42
54LS42
DECODER
Y9
Y8
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
I3-0
I3
I2
I1
I0
54LS48
54LS48
7-SEGMENT
DECODER
A
B
C
D
E
F
G
BI/
RBO
RBI
LT
I3-0
54LS51
(SIZE)
54LS51
54LS51
54LS51
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(SIZE)
54LS54
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54LS55
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54LS55
54LS55
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(SIZE)
J
Q
54
LS73
K
Q
54LS74
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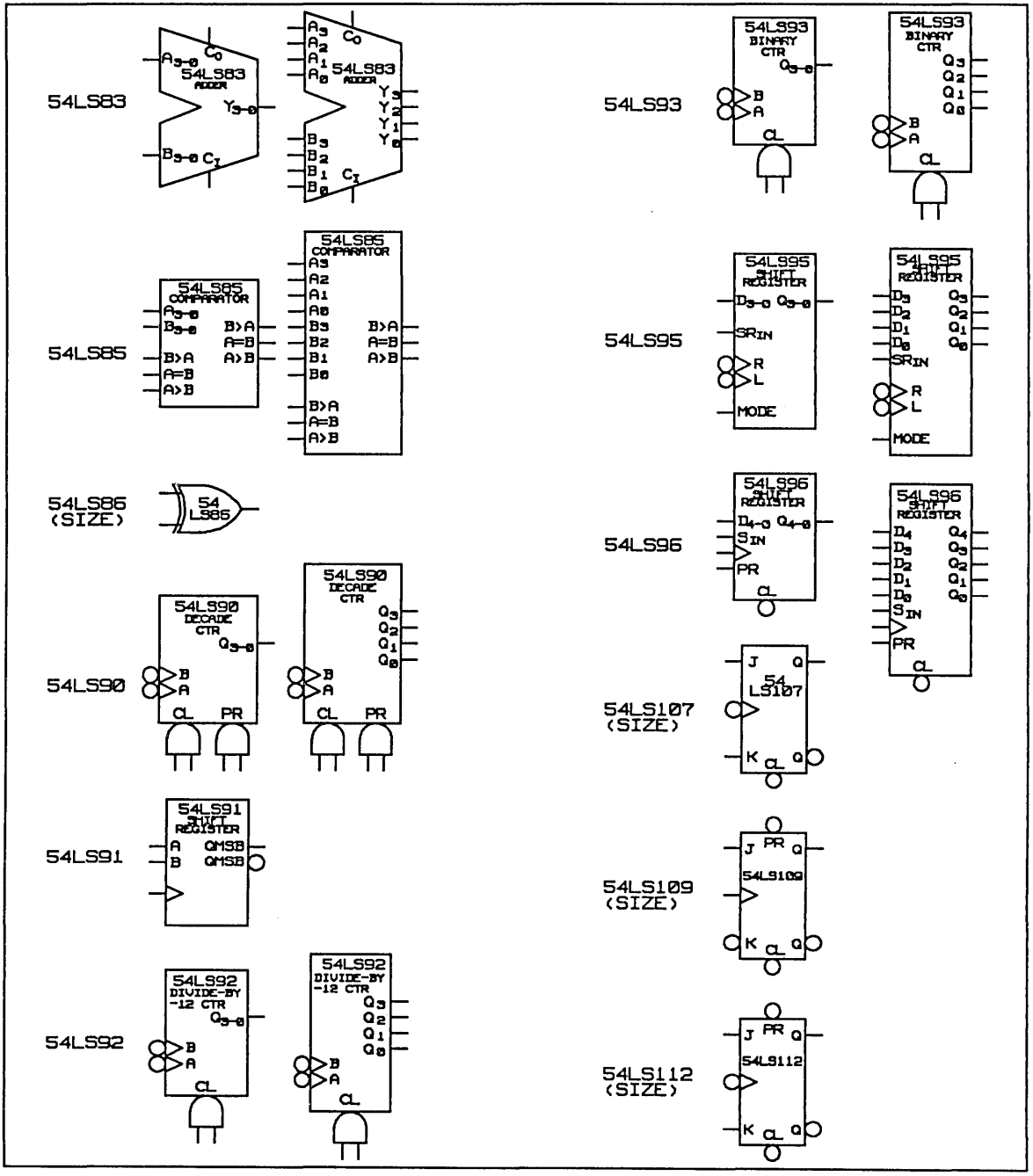
LS78
K
Q


54LS83
54LS85
54LS86 (SIZE)
54LS90
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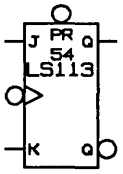
54LS93
54LS95
54LS96
54LS107 (SIZE)
54LS109 (SIZE)
54LS112 (SIZE)

54LS113
(SIZE)



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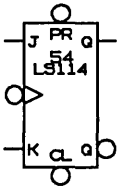

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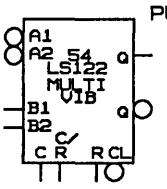

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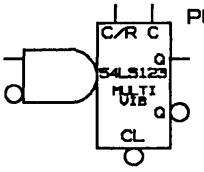

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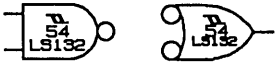
54LS126
(SIZE)

54LS132
(SIZE)



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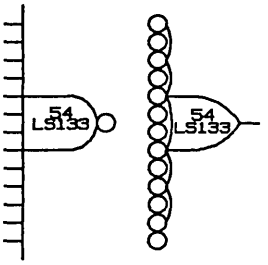

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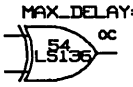

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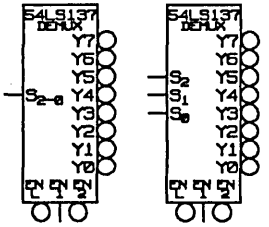

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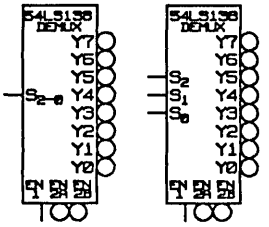

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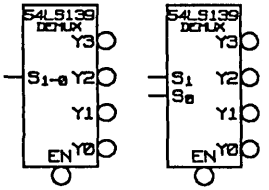

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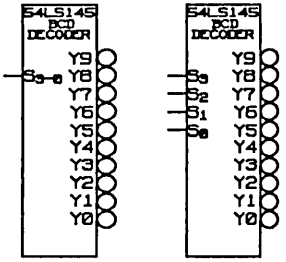

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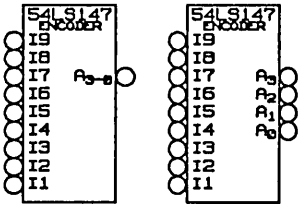

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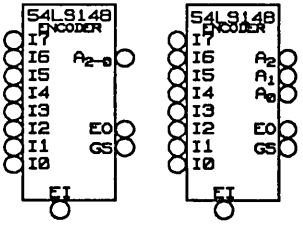

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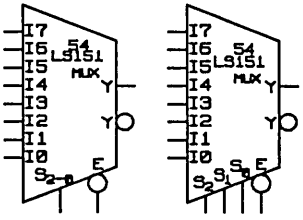

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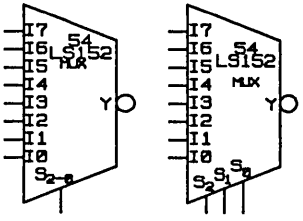

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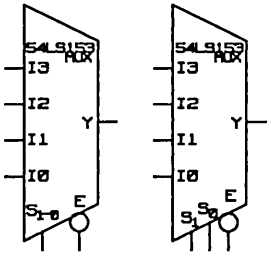

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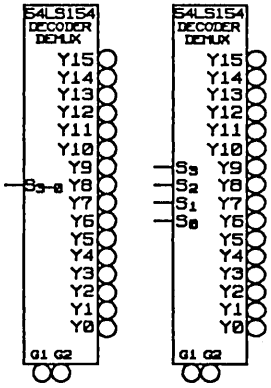

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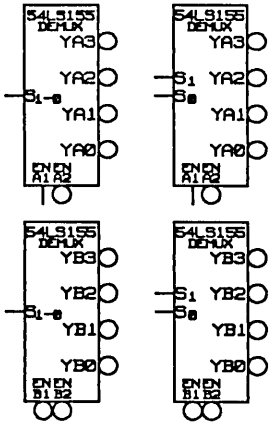

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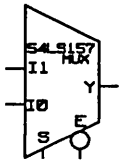

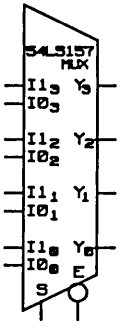

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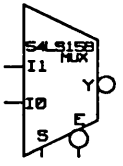

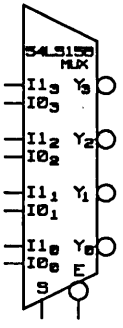

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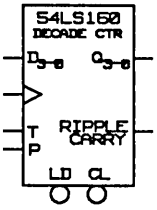

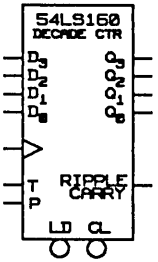

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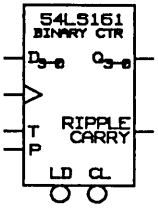

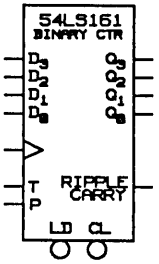

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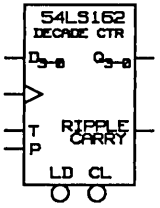

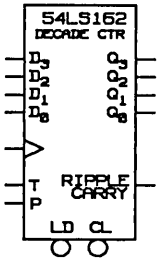

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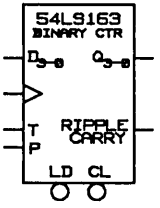

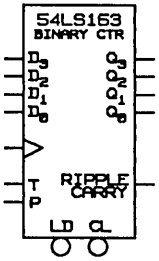

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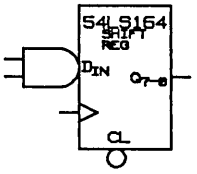

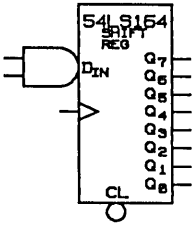

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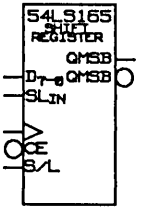

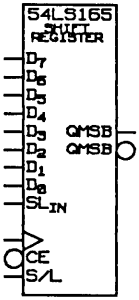

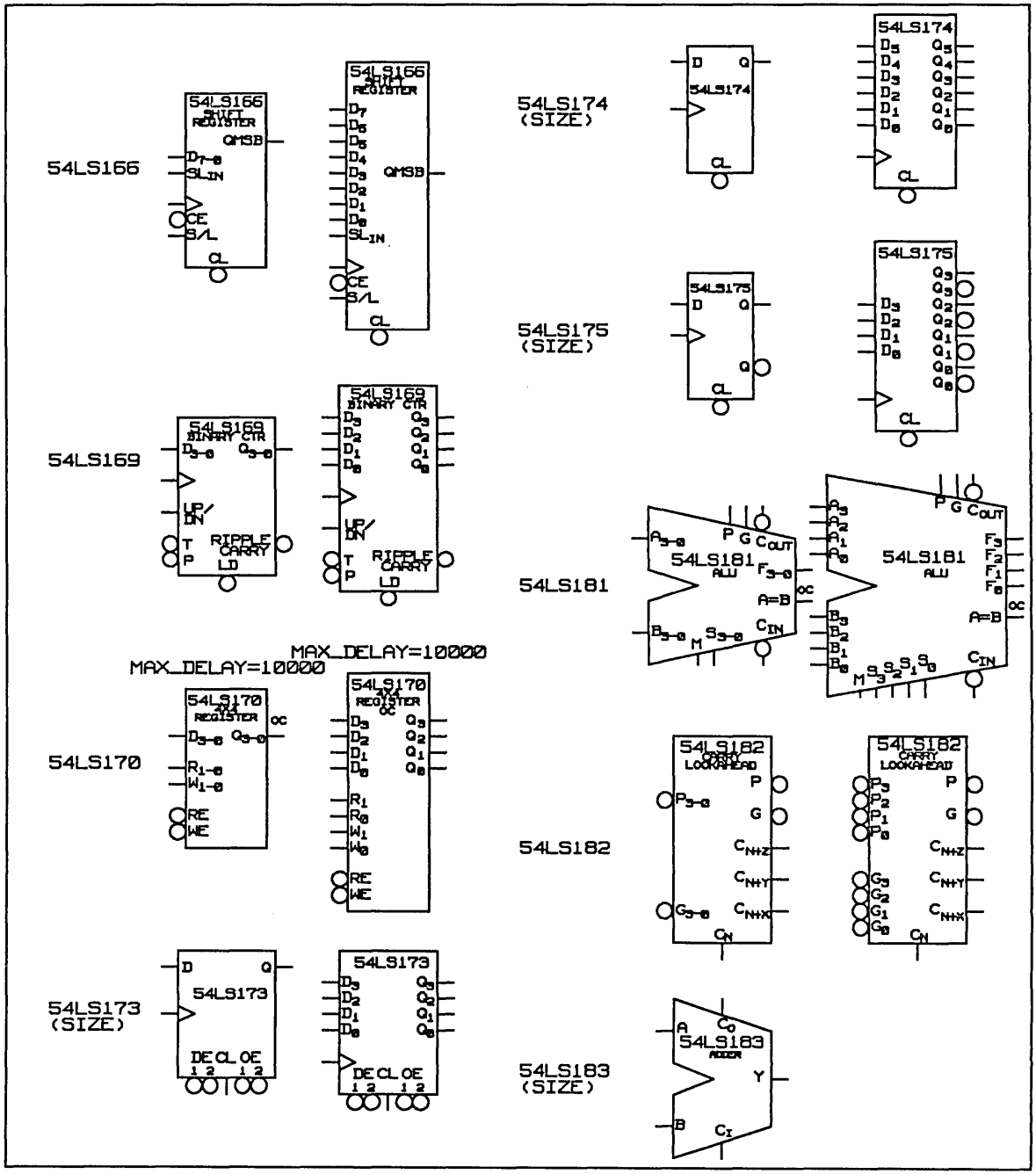
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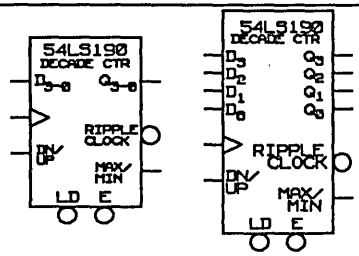

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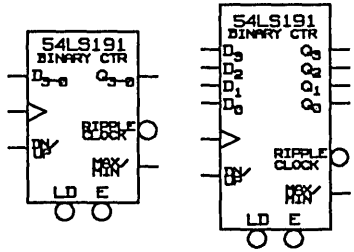

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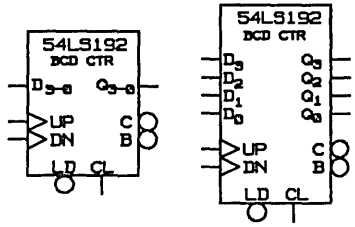

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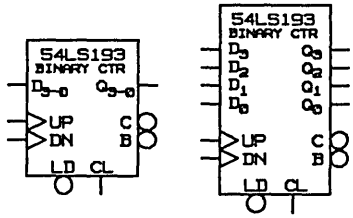

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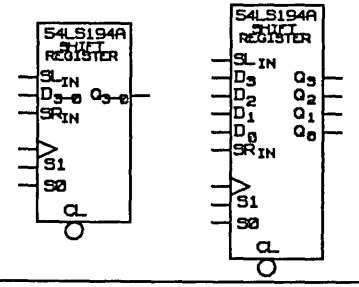

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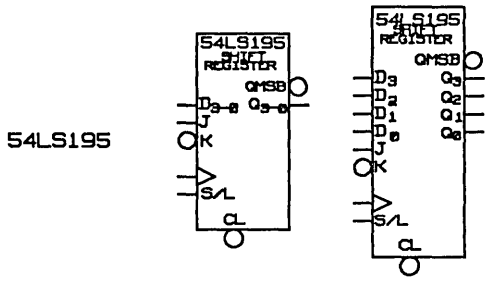

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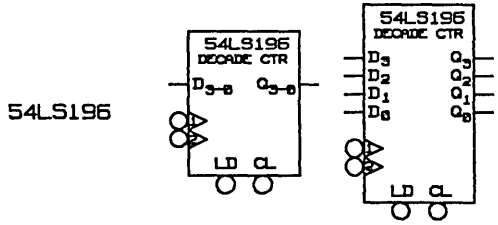

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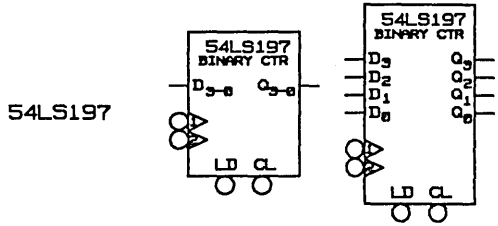

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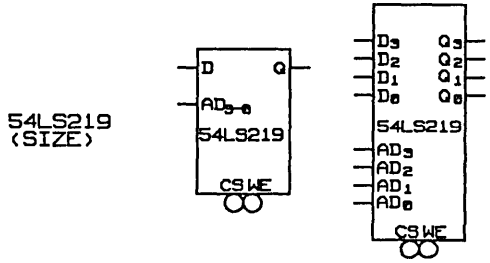

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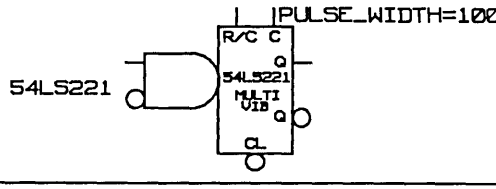

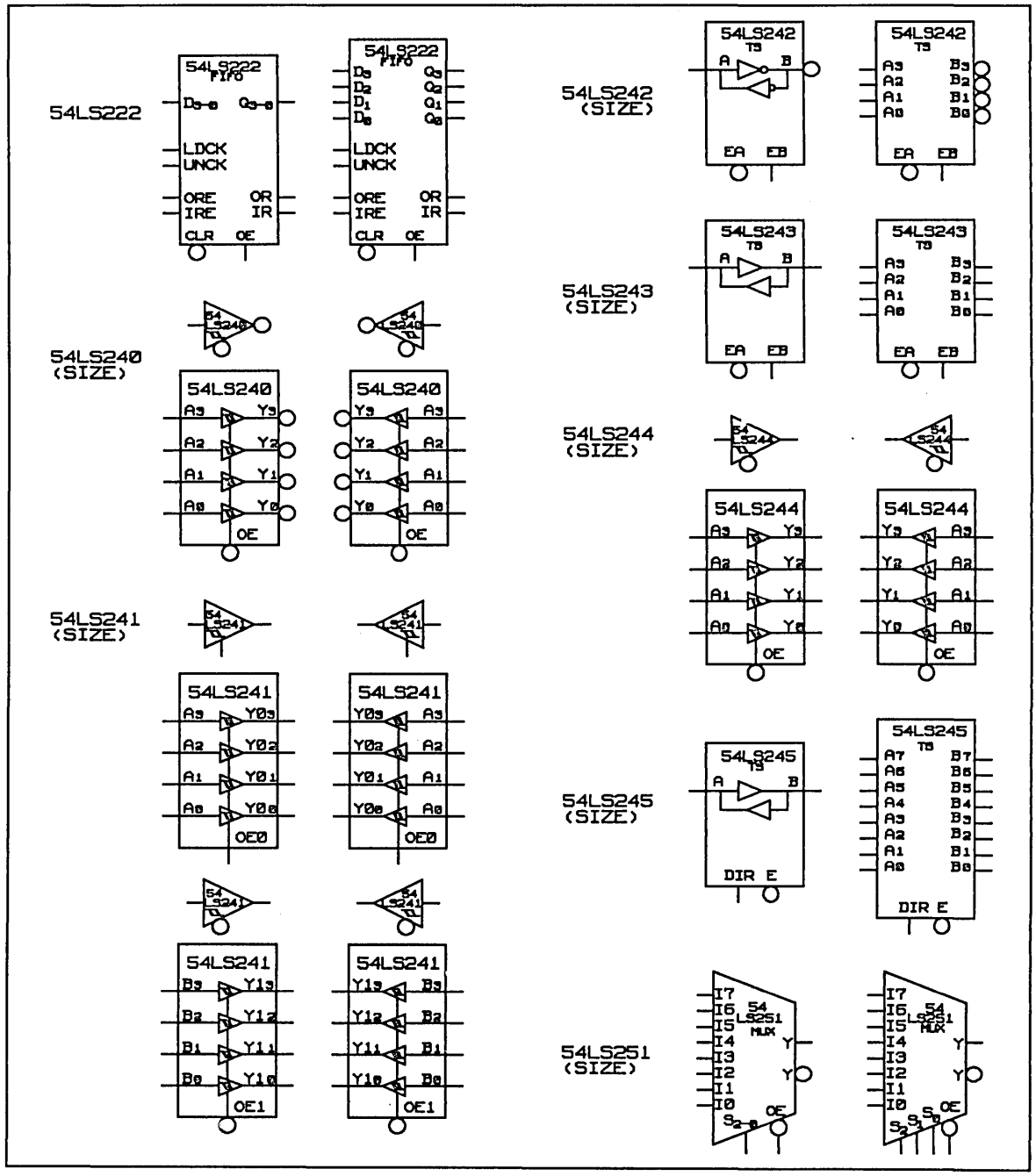
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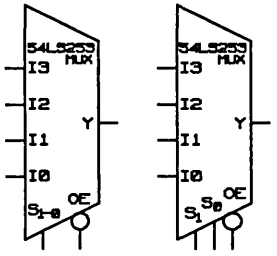

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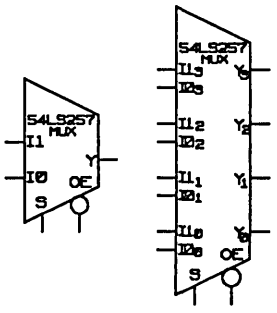

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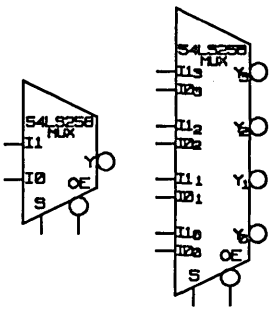

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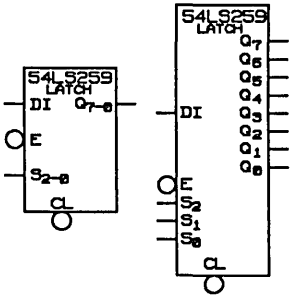

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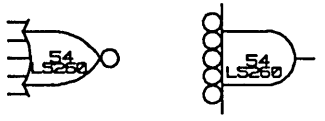

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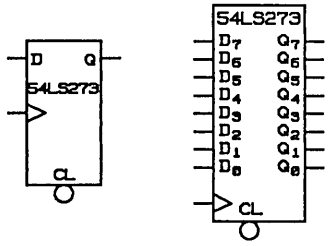

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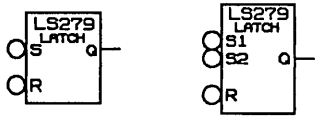

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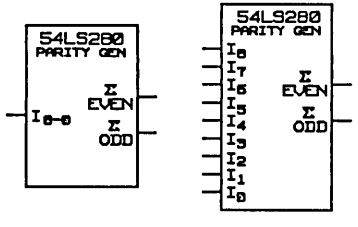

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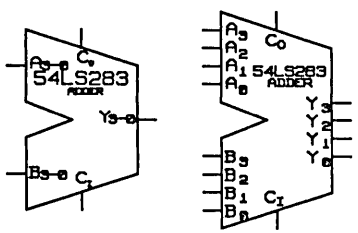

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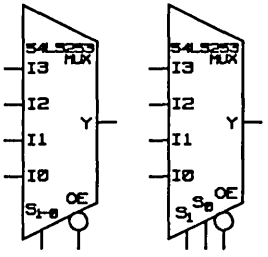

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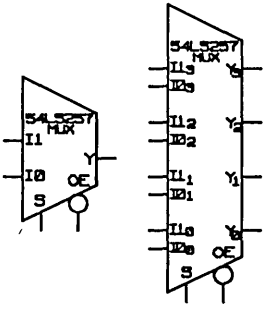

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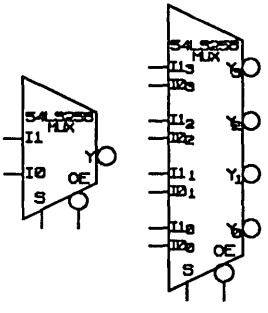

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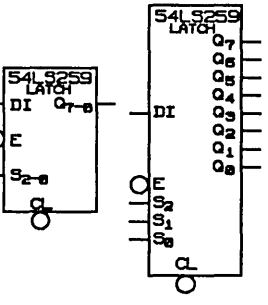

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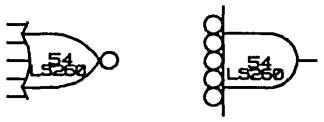

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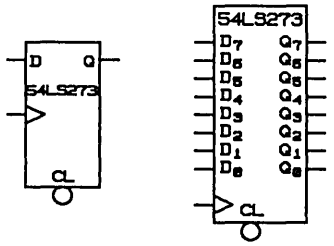

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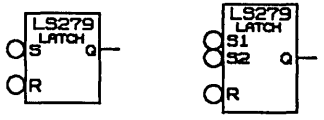

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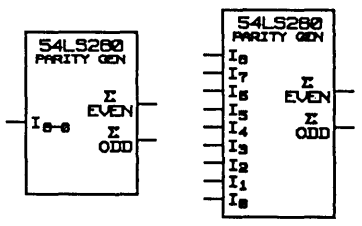

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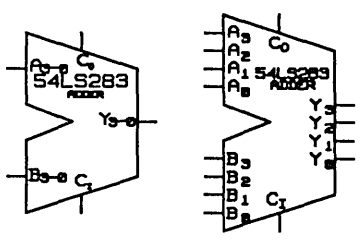

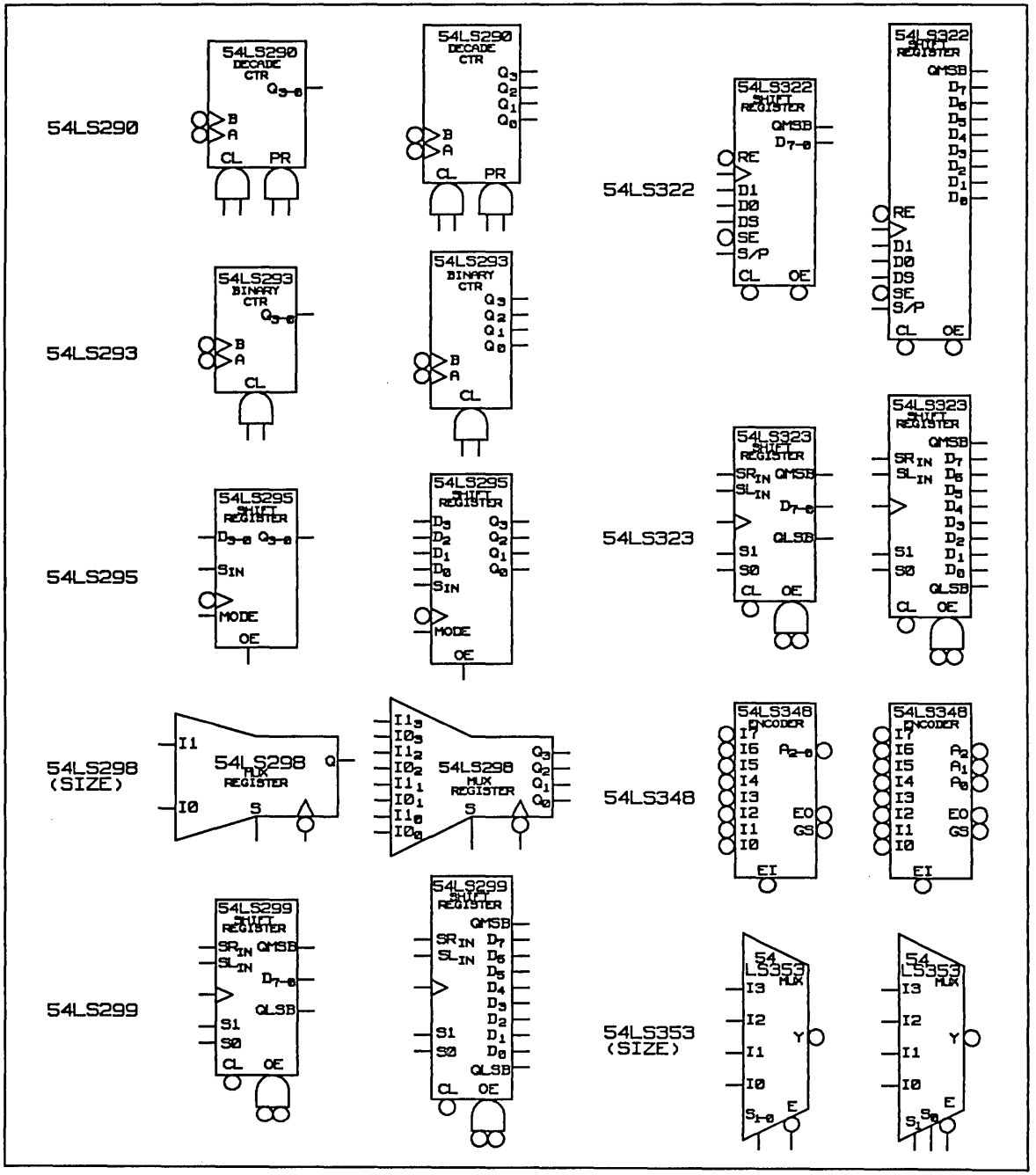
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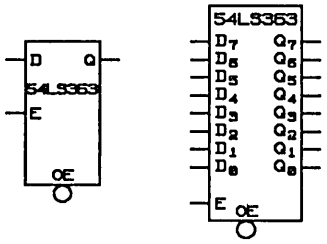
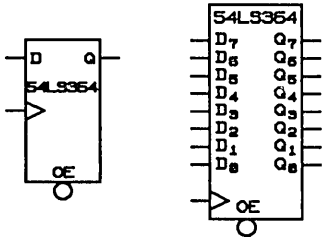
BINARY CTR
CL
54LS293
BINARY CTR
54LS295
54LS295
SHIFT REGISTER
MODE
OE
54LS295
SHIFT REGISTER
54LS298
(SIZE)
54LS298
MUX REGISTER
S
54LS298
MUX REGISTER
54LS299
54LS299
SHIFT REGISTER
SR IN
SL IN
QMSB
QLSB
S1
S0
54LS299
SHIFT REGISTER
54LS322
54LS322
SHIFT REGISTER
RE
D1
D0
DS
SE
S/P
54LS322
SHIFT REGISTER
54LS323
54LS323
SHIFT REGISTER
54LS323
SHIFT REGISTER
54LS348
54LS348
ENCODER
EI
EO
GS
54LS348
ENCODER
54LS353
(SIZE)
54
LS353
MUX
54
LS353
MUX

54LS363
(SIZE)



54LS364
(SIZE)



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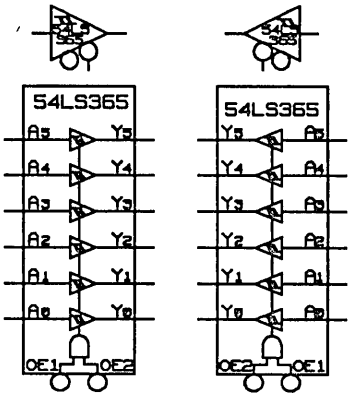
(SIZE)



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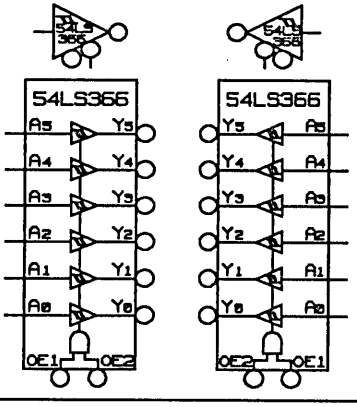
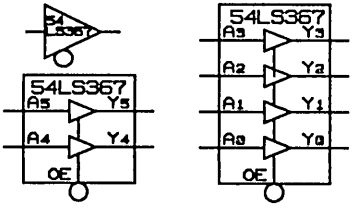


54LS367
(SIZE)



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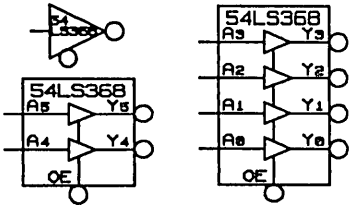
(SIZE)



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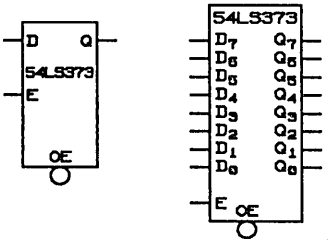
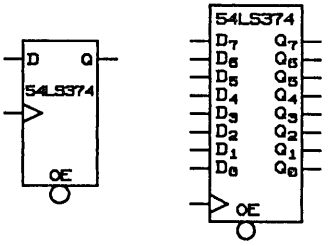
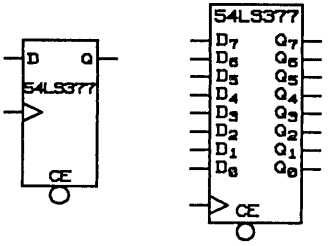
(SIZE)

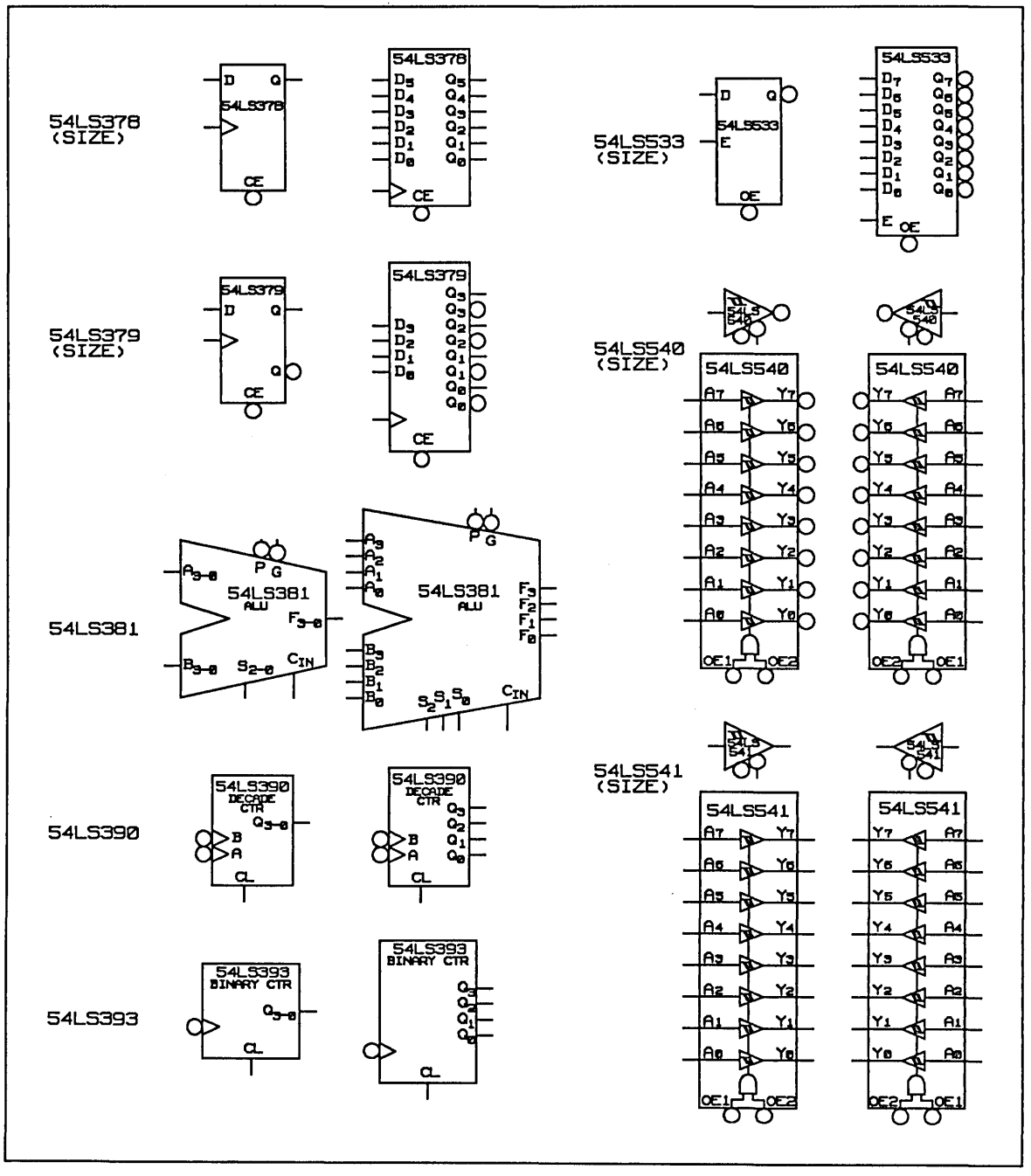


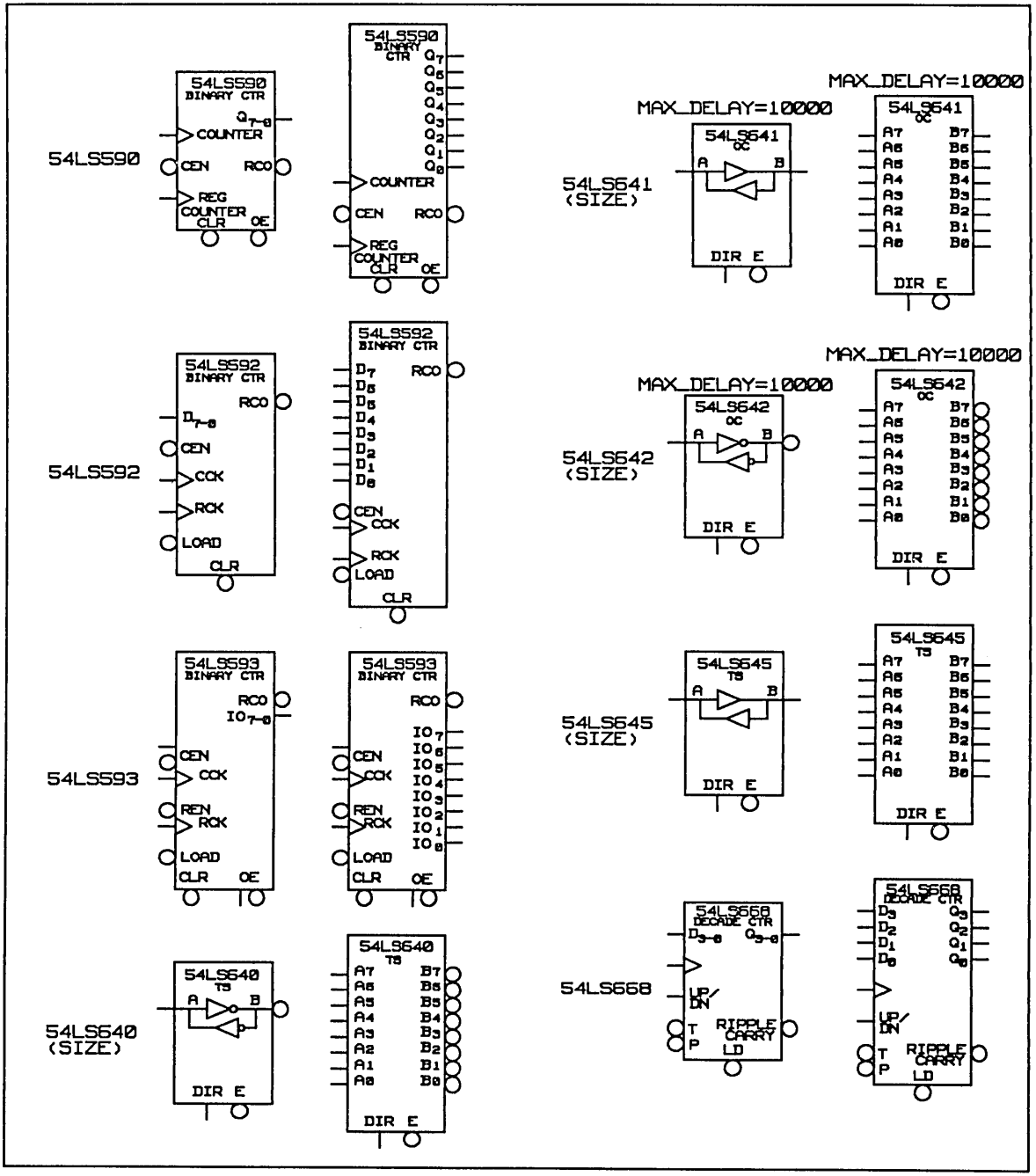
54LS374
(SIZE)

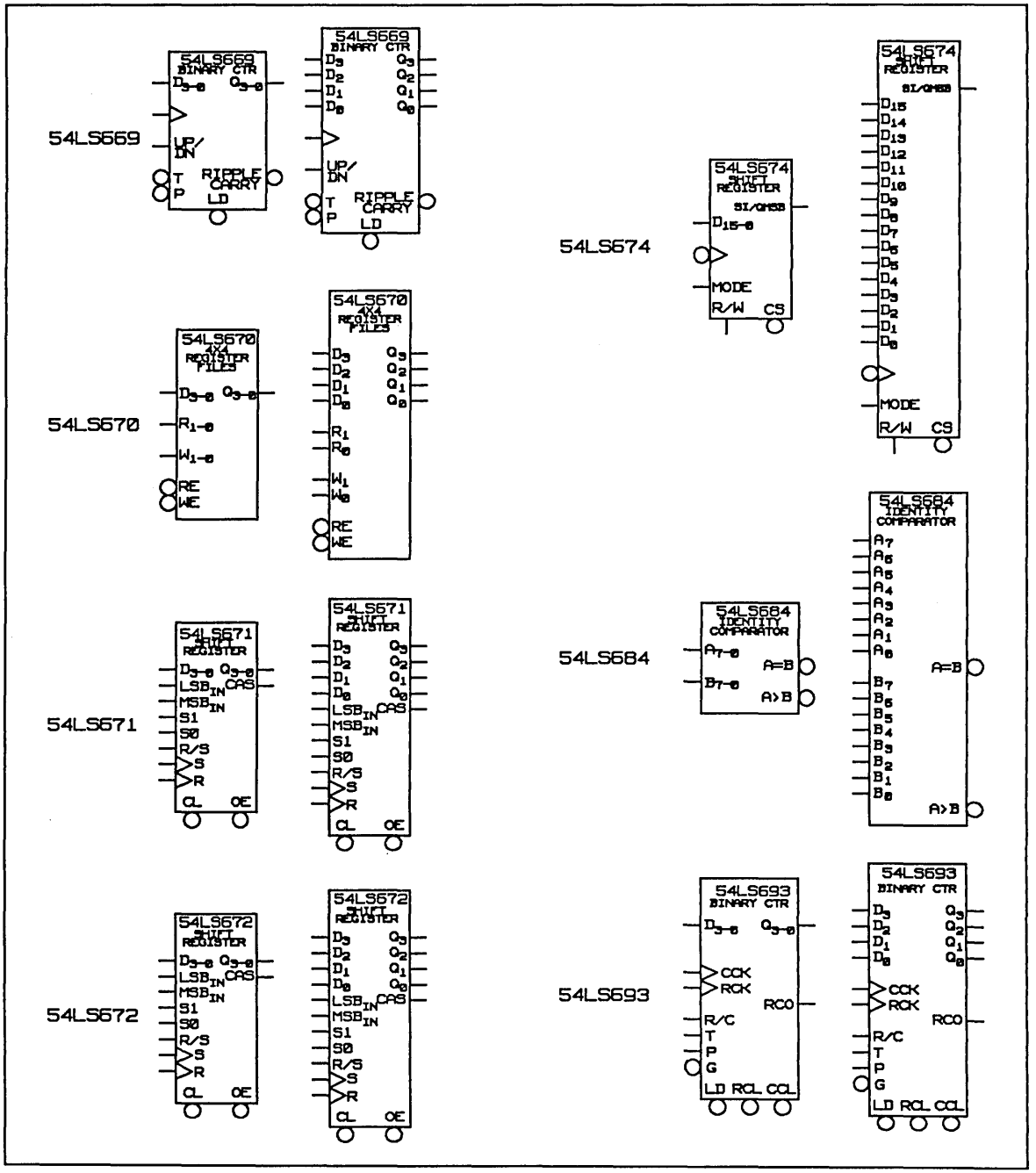


54LS377
(SIZE)

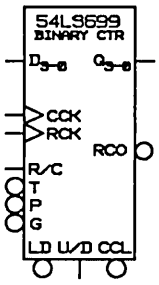


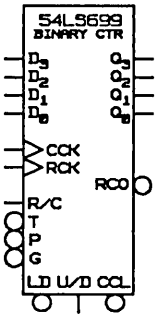

54LS378
(SIZE)
54LS533
(SIZE)
54LS379
(SIZE)
54LS540
(SIZE)
54LS381
54LS390
54LS393
54LS541
(SIZE)

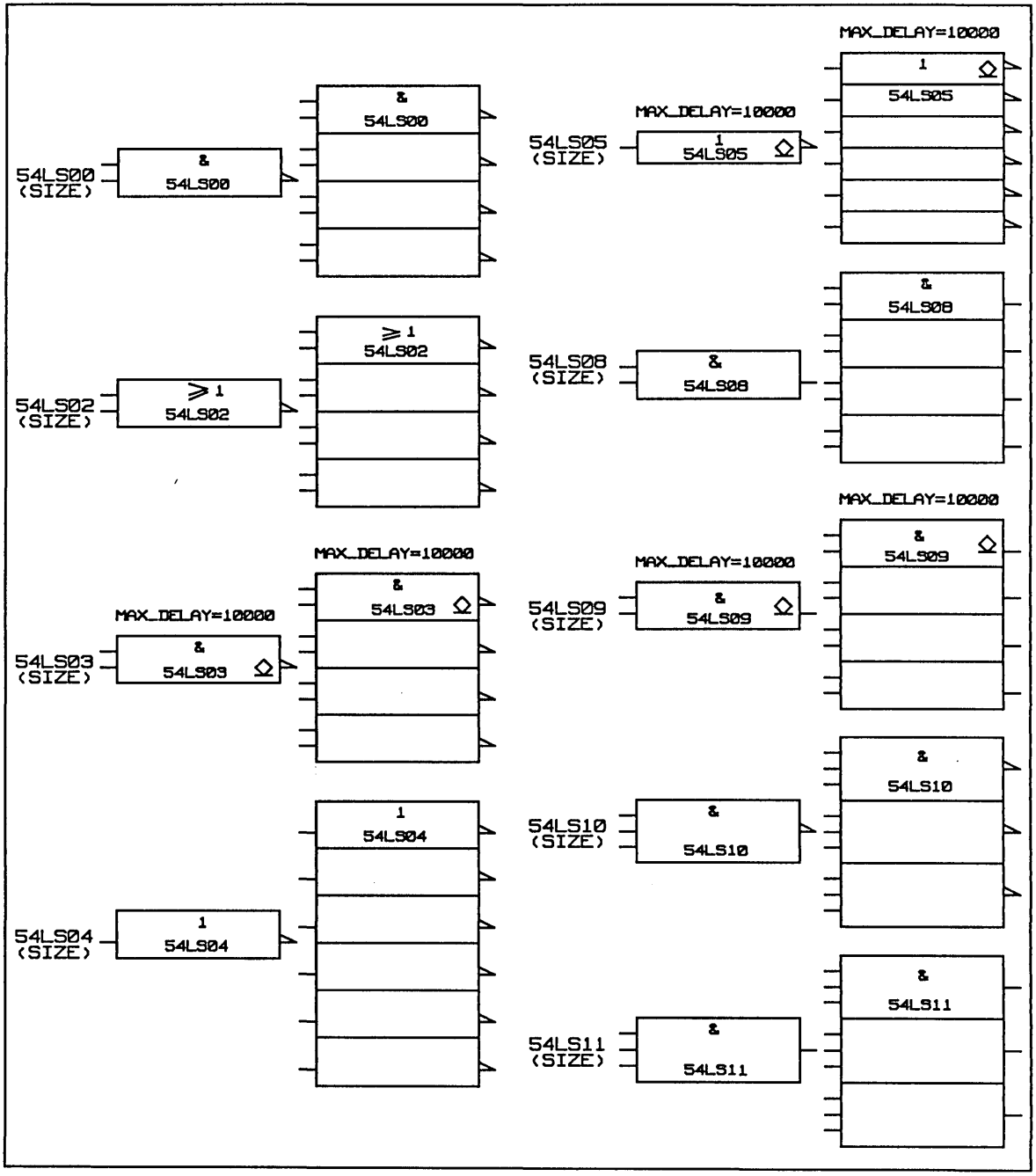

54LS590
54LS590
BINARY CTR
COUNTER
CEN
RCO
REG COUNTER CLR
OE
54LS592
BINARY CTR
CCK
RCK
LOAD
CLR
54LS593
BINARY CTR
REN
54LS640
TS
DIR E
MAX_DELAY=10000
54LS641
OC
54LS642
54LS645

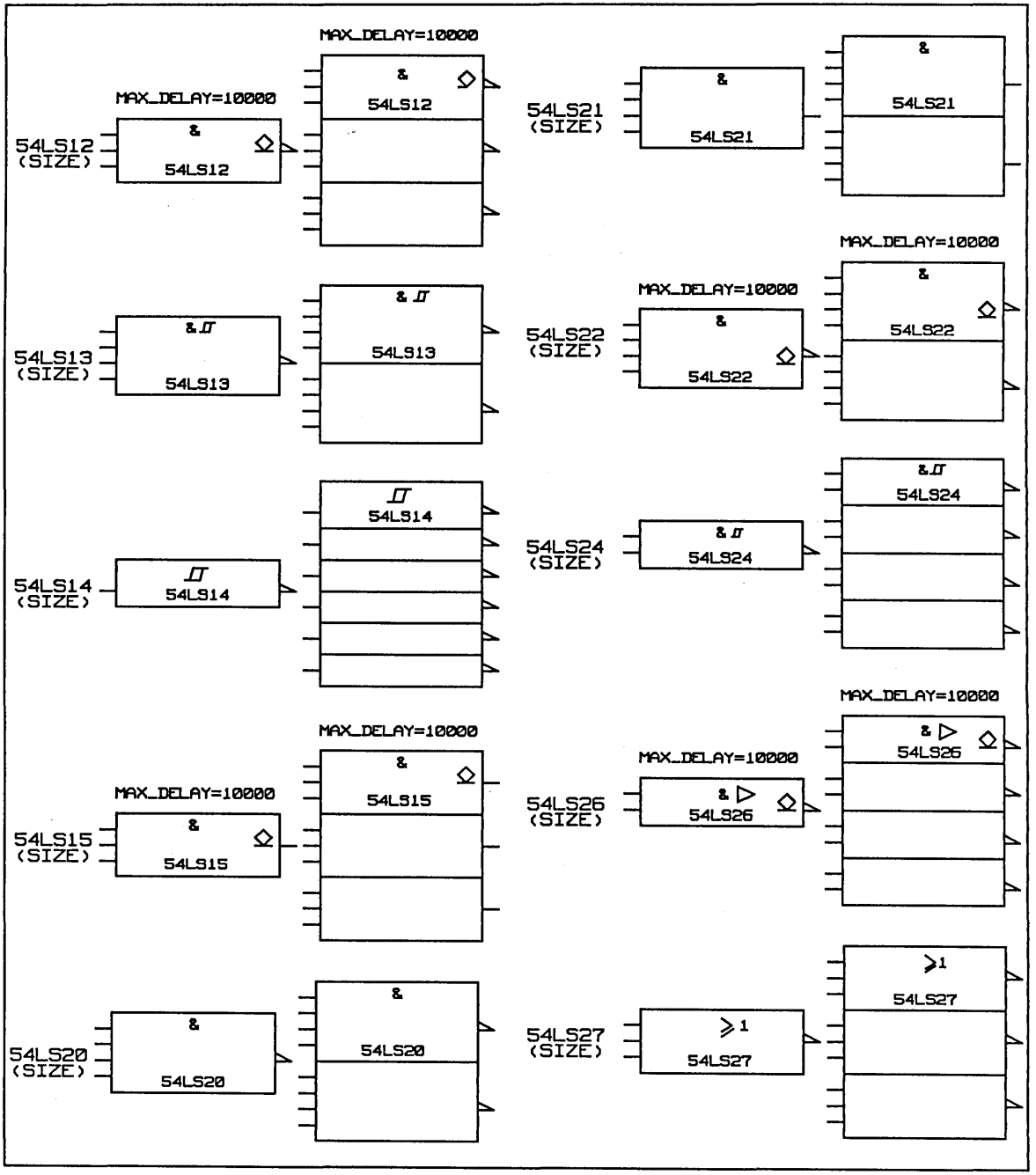

54LS669
54LS669
BINARY CTR
UP/DN
RIPPLE CARRY
LD
54LS670
4X4 REGISTER FILES
RE
WE
54LS671
SHIFT REGISTER
LSB
MSB
S1
S0
R/S
CAS
CL
OE
54LS672
SHIFT REGISTER
54LS674
SHIFT REGISTER
SI/OMSB
MODE
R/W
CS
54LS684
IDENTITY COMPARATOR
A=B
A>B
54LS693
BINARY CTR
CCK
RCK
RCO
R/C
LD RCL CCL

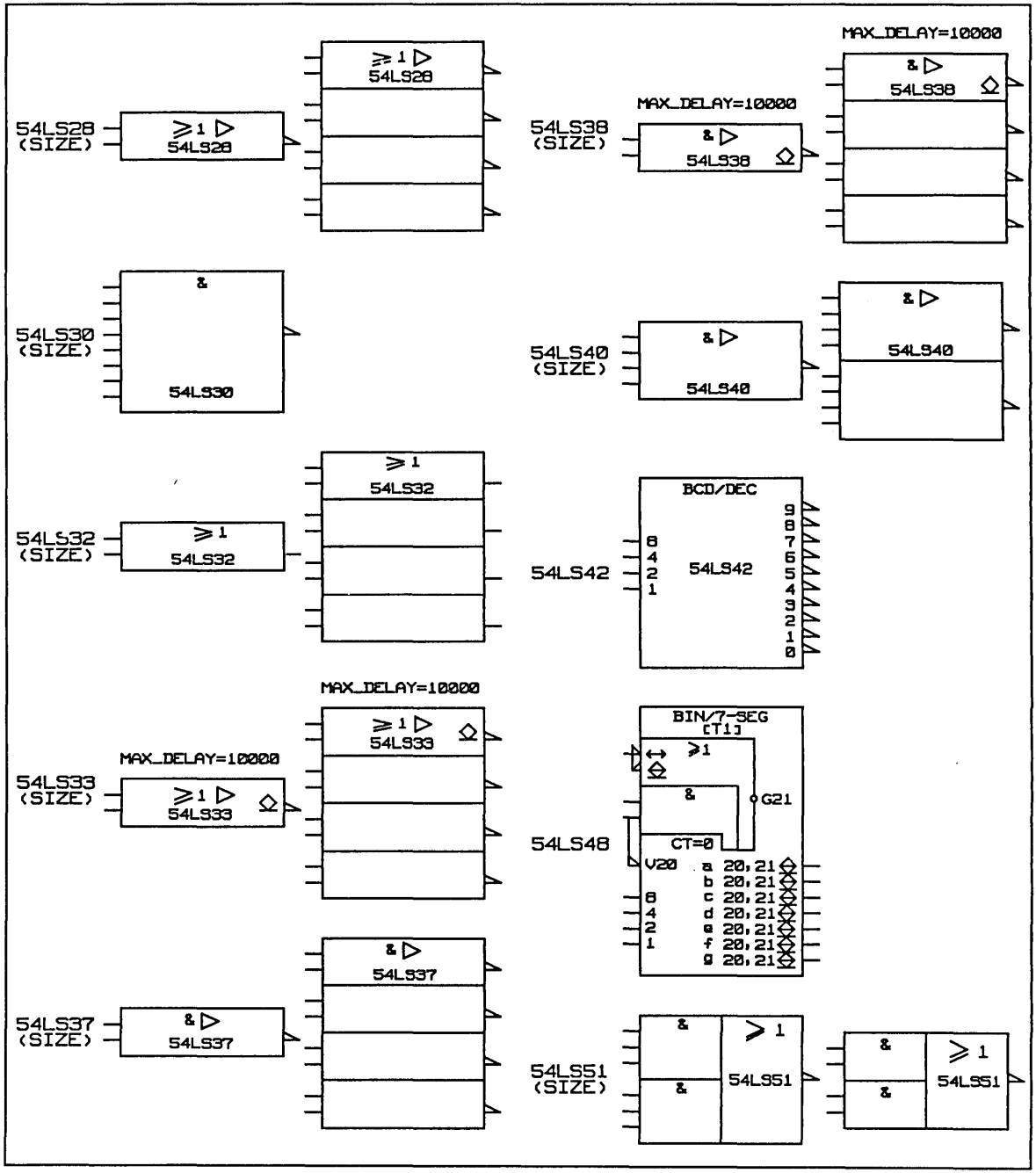
54LS699

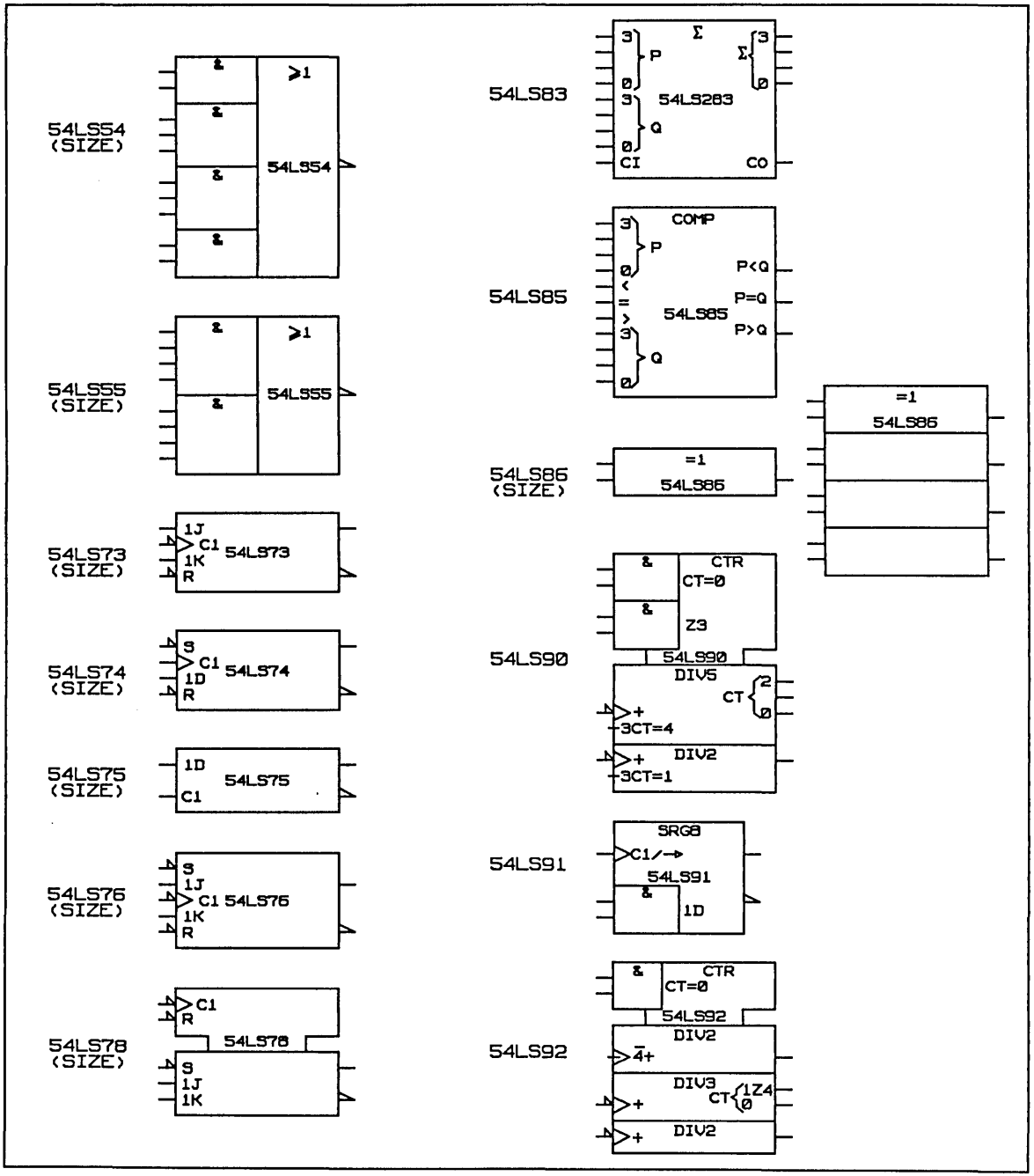

54LS699
BINARY CTR
D3-0
Q3-0
CCK
RCK
RCO
R/C
T
P
G
LD U/D CCL

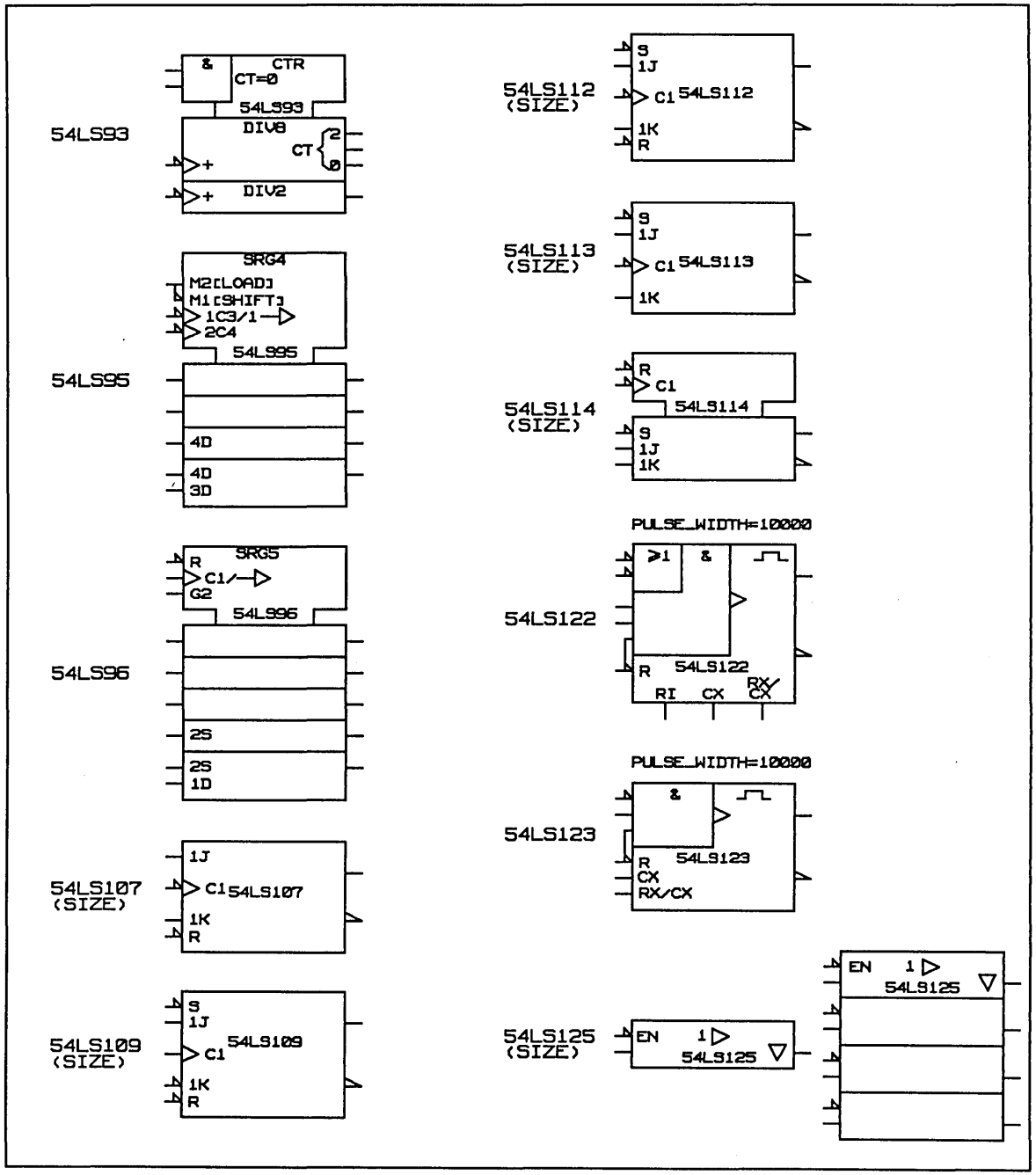

54LS699
BINARY CTR
D3
D2
D1
D0
Q3
Q2
Q1
Q0
CCK
RCK
RCO
R/C
T
P
G
LD U/D CCL

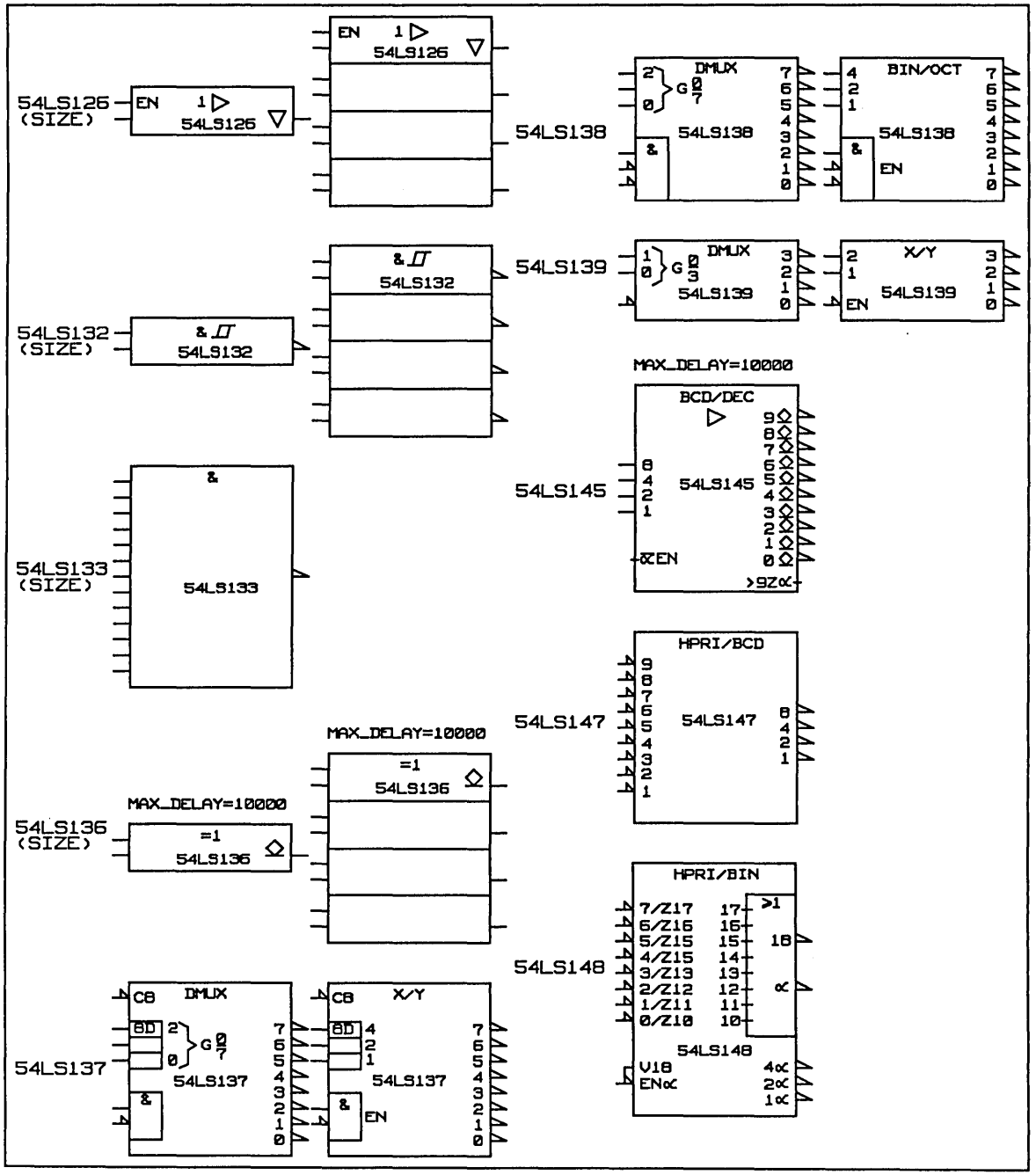

54LS00
(SIZE)
&
54LS00
54LS02
(SIZE)
≥1
54LS02
54LS03
(SIZE)
MAX_DELAY=10000
&
54LS03
54LS04
(SIZE)
1
54LS04
54LS05
(SIZE)
MAX_DELAY=10000
1
54LS05
54LS08
(SIZE)
&
54LS08
54LS09
(SIZE)
MAX_DELAY=10000
&
54LS09
54LS10
(SIZE)
&
54LS10
54LS11
(SIZE)
&
54LS11

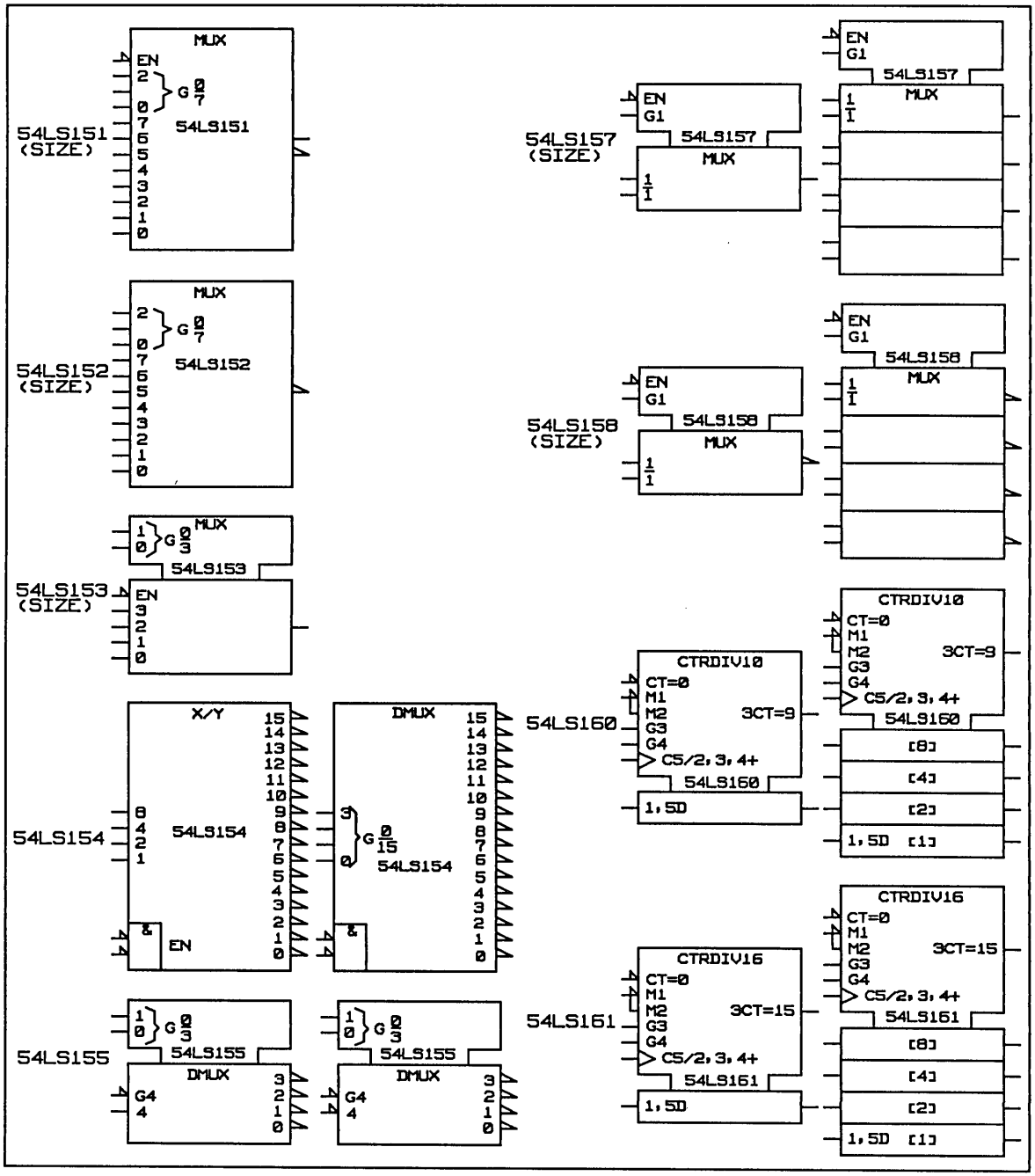

MAX_DELAY=10000
&
54LS12
MAX_DELAY=10000
&
54LS12
54LS12
(SIZE)
54LS12
54LS21
(SIZE)
&
54LS21
&
54LS21
&Π
54LS13
54LS13
(SIZE)
&Π
54LS13
MAX_DELAY=10000
&
54LS22
MAX_DELAY=10000
&
54LS22
54LS22
(SIZE)
&
54LS22
Π
54LS14
54LS14
(SIZE)
Π
54LS14
&Π
54LS24
&Π
54LS24
54LS24
(SIZE)
MAX_DELAY=10000
&
54LS15
MAX_DELAY=10000
&
54LS15
54LS15
(SIZE)
&
54LS15
MAX_DELAY=10000
&▷
54LS26
MAX_DELAY=10000
&▷
54LS26
54LS26
(SIZE)
&▷
54LS26
&
54LS20
&
54LS20
54LS20
(SIZE)
&
54LS20
≥1
54LS27
≥1
54LS27
54LS27
(SIZE)
≥1
54LS27

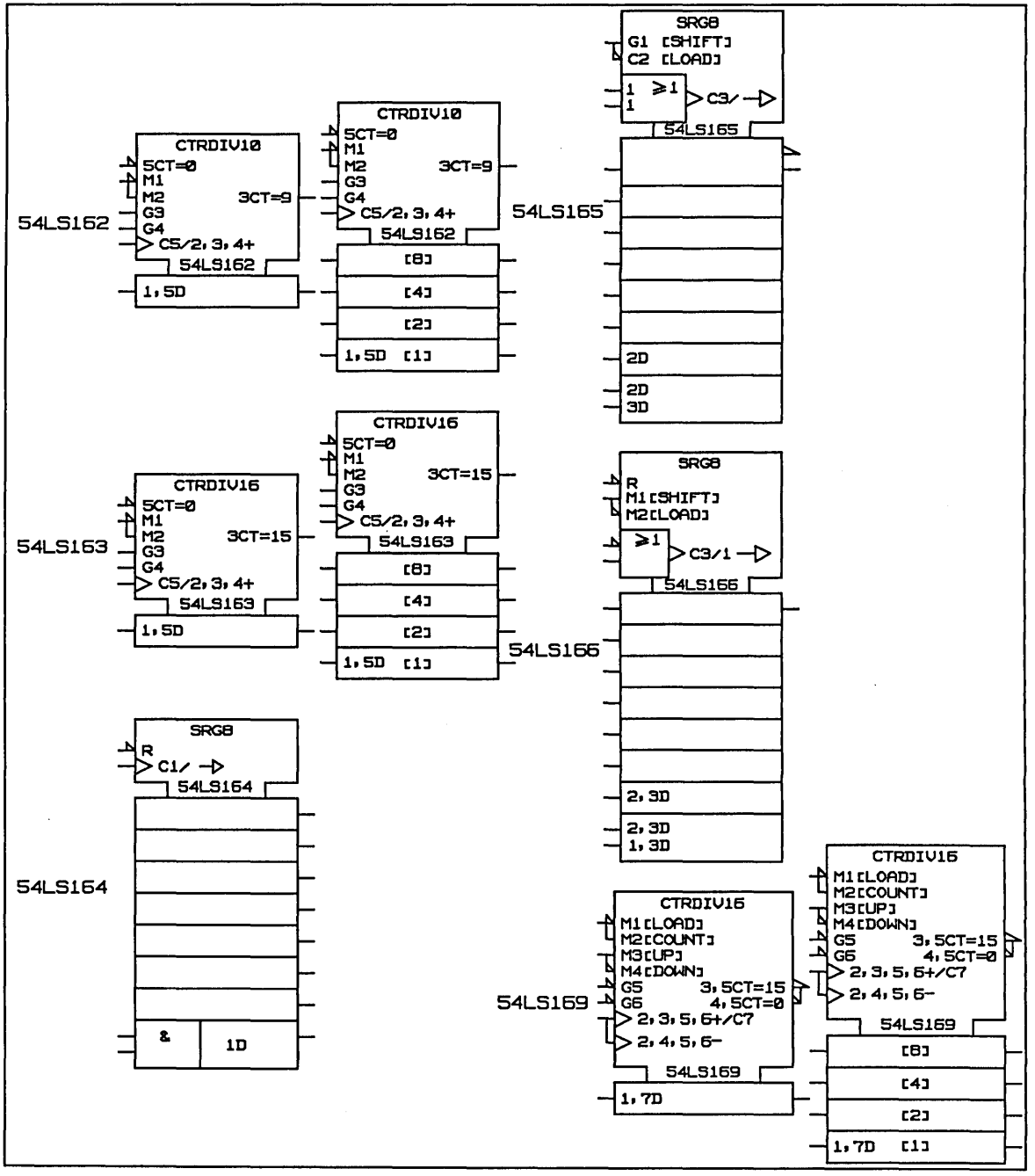

54LS28
(SIZE)
54LS28
54LS28
54LS30
(SIZE)
54LS30
54LS30
54LS32
(SIZE)
54LS32
54LS32
MAX_DELAY=10000
MAX_DELAY=10000
54LS33
(SIZE)
54LS33
54LS33
54LS37
(SIZE)
54LS37
54LS37
MAX_DELAY=10000
MAX_DELAY=10000
54LS38
(SIZE)
54LS38
54LS38
54LS40
(SIZE)
54LS40
54LS40
BCD/DEC
54LS42
54LS42
BIN/7-SEG
[T1]
G21
CT=0
V20
54LS48
54LS51
(SIZE)
54LS51
54LS51

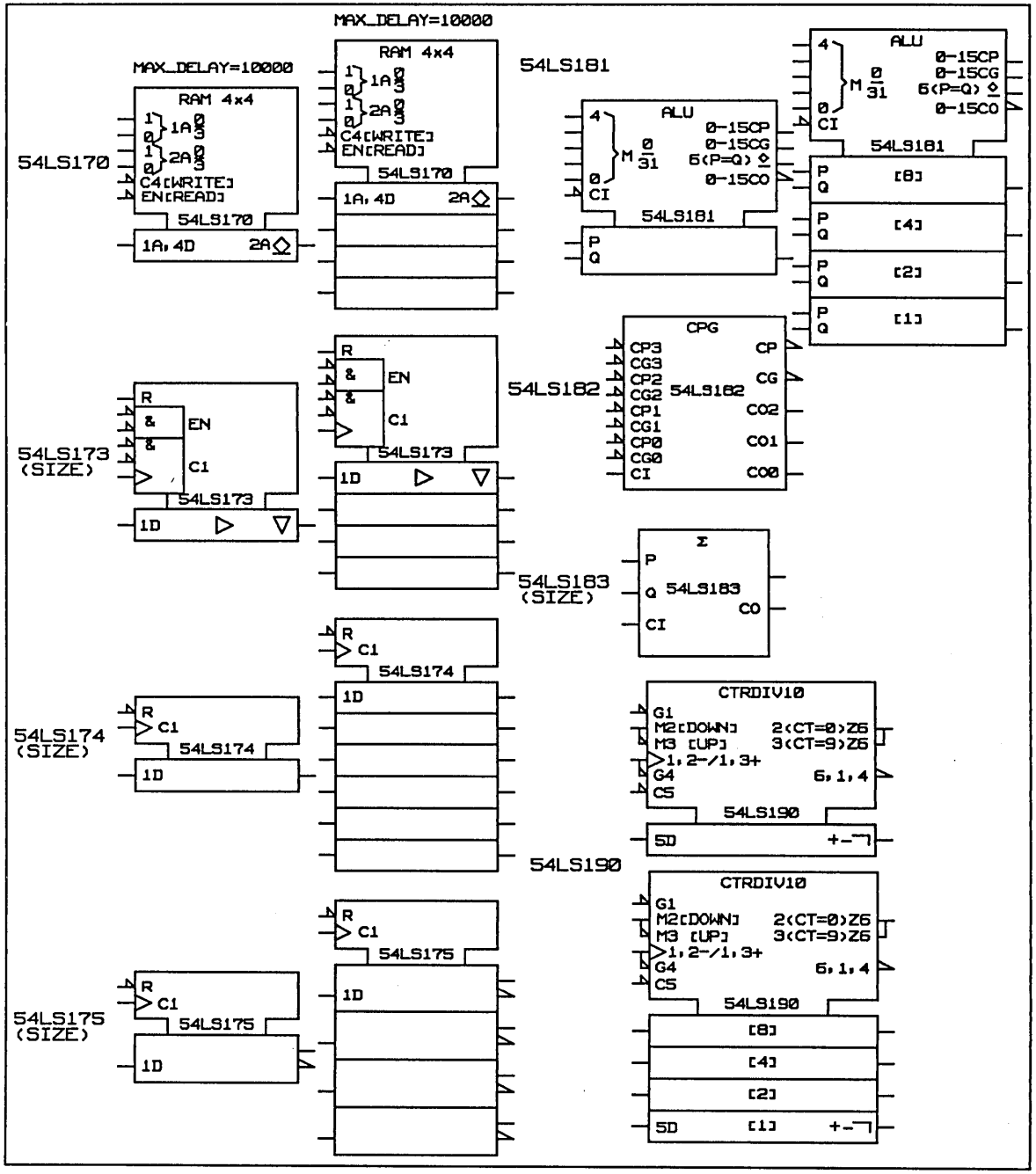

54LS54
(SIZE)
&
≥1
54LS54
54LS55
(SIZE)
54LS55
54LS73
(SIZE)
1J
C1
1K
R
54LS73
54LS74
(SIZE)
S
C1
1D
R
54LS74
54LS75
(SIZE)
1D
C1
54LS75
54LS76
(SIZE)
S
1J
C1
1K
R
54LS76
54LS78
(SIZE)
C1
R
54LS78
S
1J
1K
54LS83
Σ
P
Q
54LS283
CI
CO
54LS85
COMP
P<Q
P=Q
P>Q
54LS85
54LS86
(SIZE)
=1
54LS86
54LS90
CTR
CT=0
Z3
54LS90
DIV5
CT
+
3CT=4
DIV2
3CT=1
54LS91
SRG8
C1/→
54LS91
1D
54LS92
CT=0
54LS92
DIV2
DIV3
1Z4
DIV2

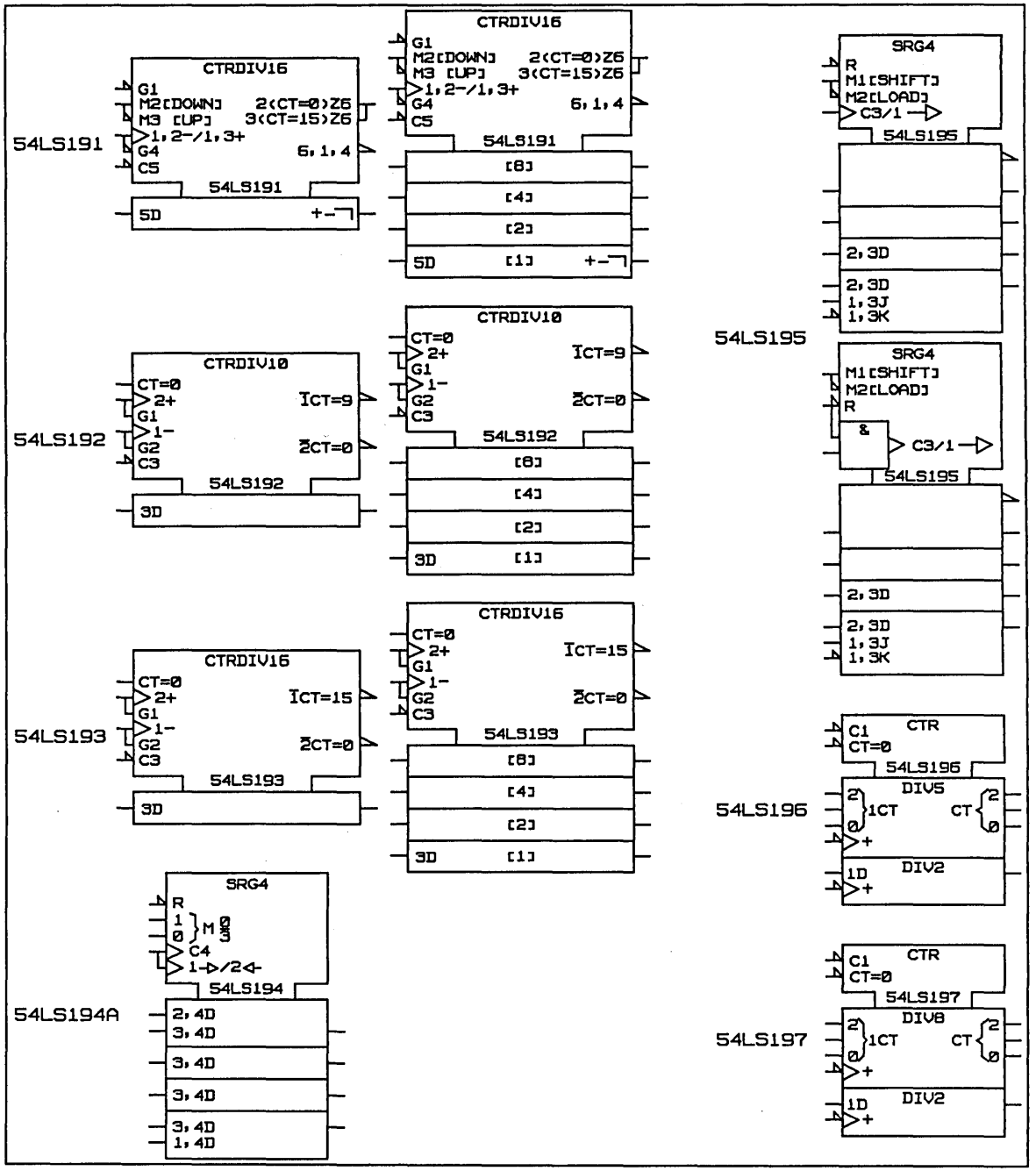

54LS93
&
CTR
CT=0
54LS93
DIV8
CT
2
0
+
+
DIV2
54LS95
SRG4
M2[LOAD]
M1[SHIFT]
1C3/1
2C4
54LS95
4D
4D
3D
54LS96
SRG5
R
C1/
G2
54LS96
2S
2S
1D
54LS107
(SIZE)
1J
C1
54LS107
1K
R
54LS109
(SIZE)
S
1J
C1
54LS109
1K
R
54LS112
(SIZE)
S
1J
C1
54LS112
1K
R
54LS113
(SIZE)
S
1J
C1
54LS113
1K
54LS114
(SIZE)
R
C1
54LS114
S
1J
1K
54LS122
PULSE_WIDTH=10000
≥1
&
R
54LS122
RI
CX
RX
CX
54LS123
PULSE_WIDTH=10000
&
54LS123
R
CX
RX/CX
54LS125
(SIZE)
EN
1
54LS125
EN
1
54LS125

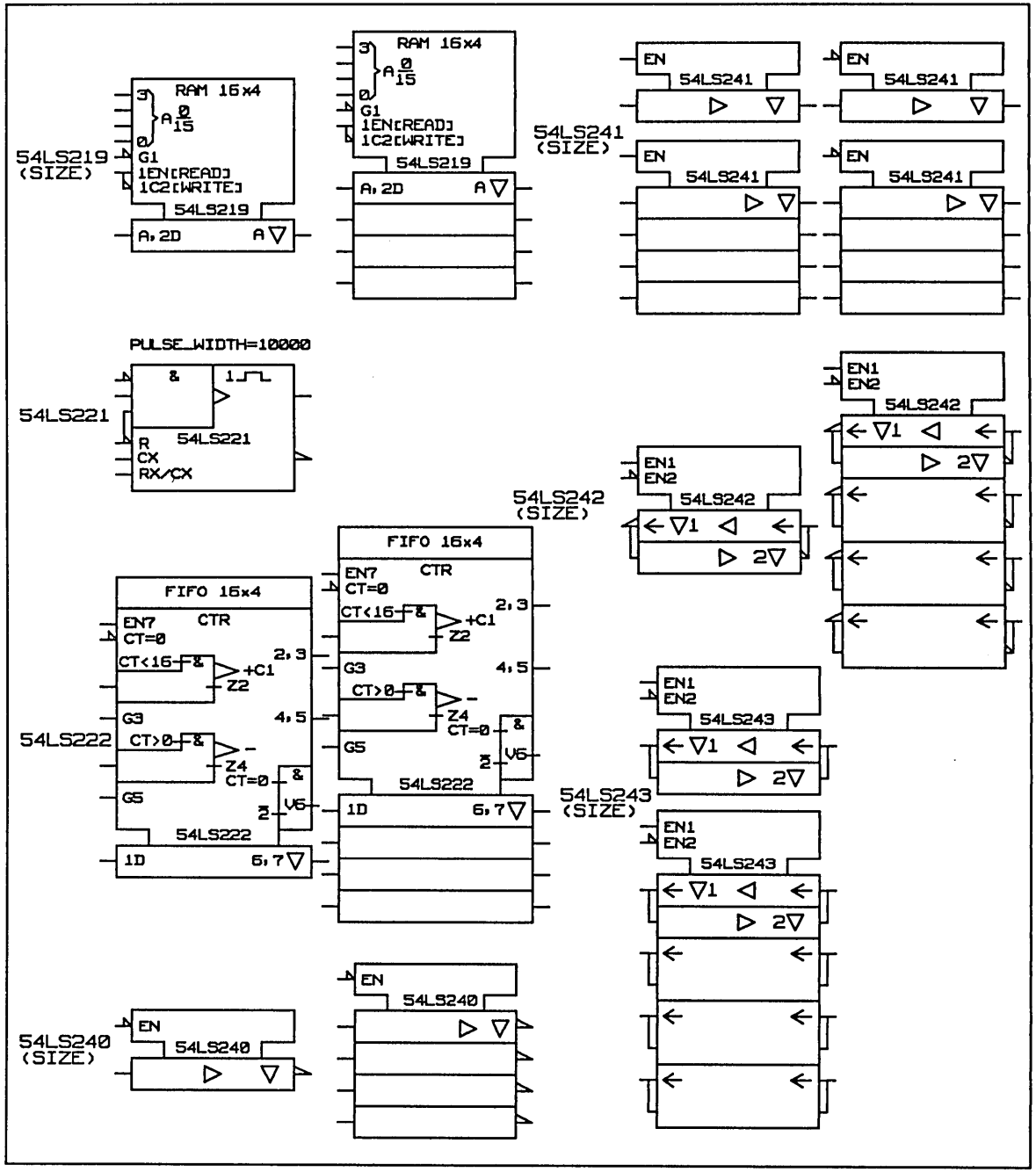

54LS126
(SIZE)
EN
1
54LS126
54LS138
DMUX
BIN/OCT
54LS138
54LS139
X/Y
54LS132
(SIZE)
&
54LS132
MAX_DELAY=10000
BCD/DEC
54LS145
54LS133
(SIZE)
54LS133
HPRI/BCD
54LS147
=1
54LS136
54LS136
(SIZE)
HPRI/BIN
54LS148
C8
54LS137
EN

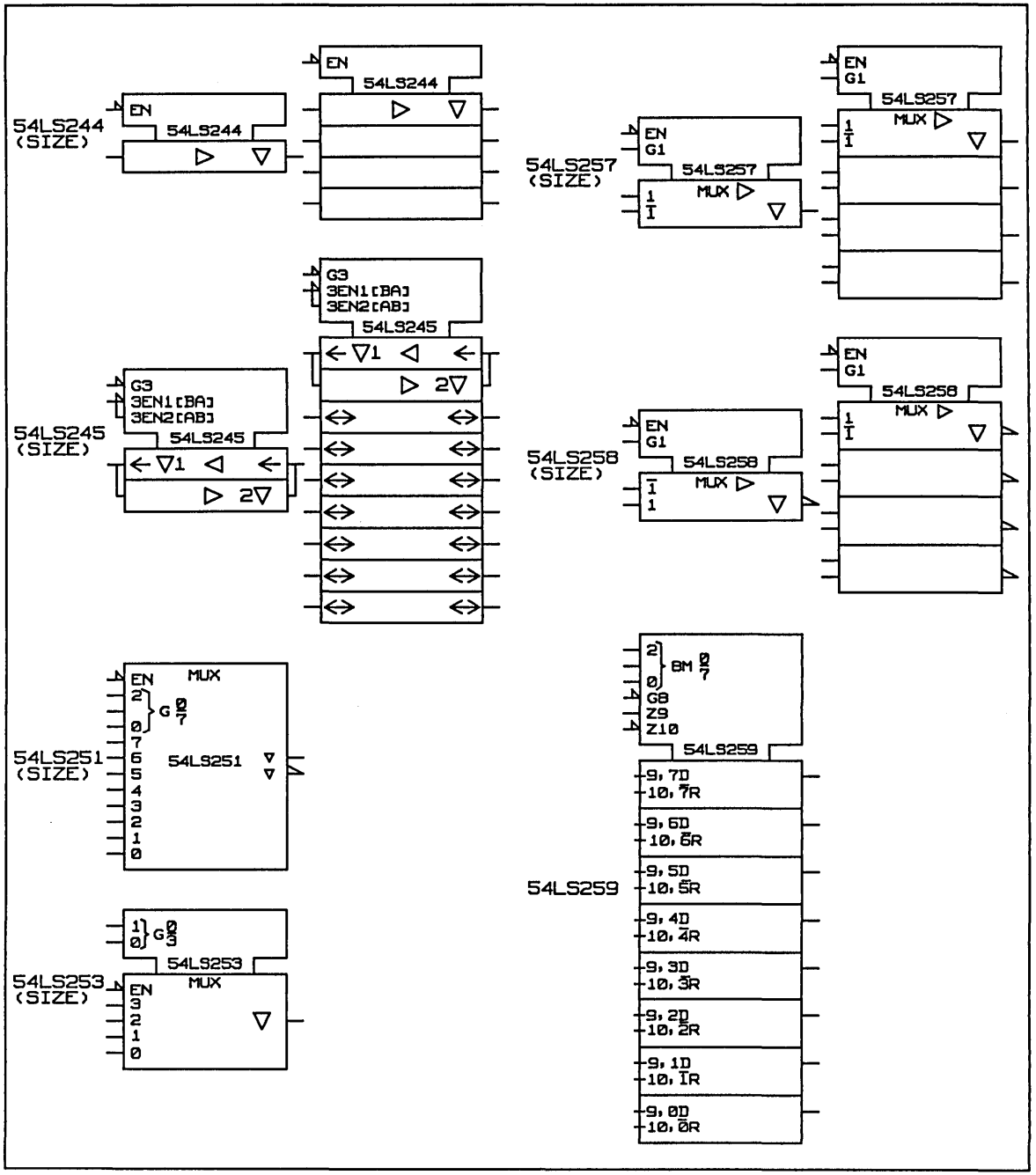

MUX
EN
G 0 7
54LS151
54LS151
(SIZE)
MUX
G 0 7
54LS152
54LS152
(SIZE)
MUX
G 0 3
54LS153
54LS153
(SIZE)
EN
X/Y
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
8 4 2 1
54LS154
EN
DMUX
G 0 15
54LS154
54LS155
DMUX
G4
54LS157
(SIZE)
54LS158
(SIZE)
54LS160
CTRDIV10
CT=0
M1
M2
G3
G4
C5/2, 3, 4+
3CT=9
[8]
[4]
[2]
[1]
1, 5D
54LS161
CTRDIV16
3CT=15

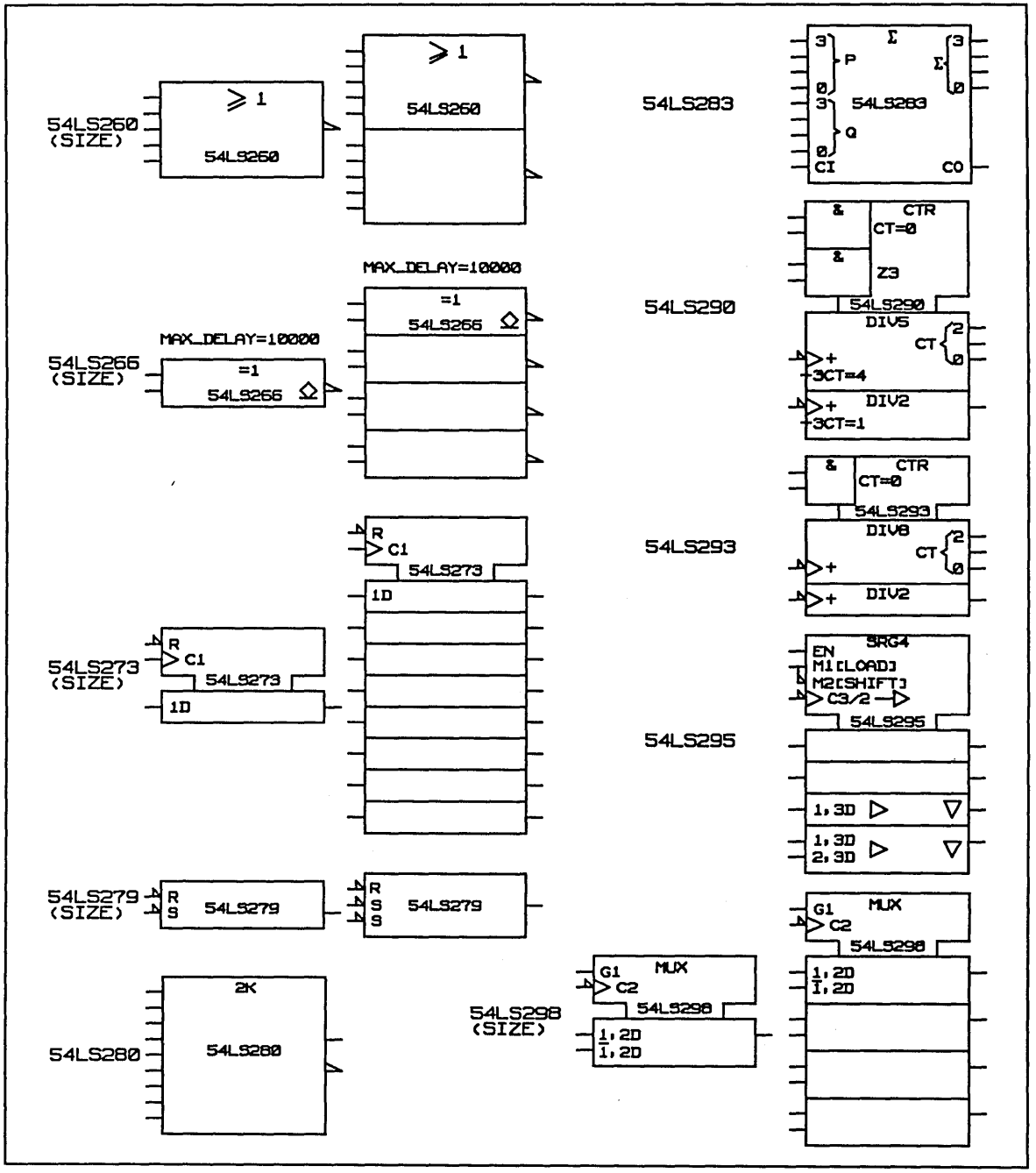

CTRDIV10
5CT=0
M1
M2
G3
G4
C5/2,3,4+
3CT=9
54LS162
1,5D
[8]
[4]
[2]
[1]
SRG8
G1 [SHIFT]
C2 [LOAD]
1
1
≥1
C3/
54LS165
2D
2D
3D
CTRDIV16
3CT=15
54LS163
SRG8
R
M1 [SHIFT]
M2 [LOAD]
≥1
C3/1
54LS166
2,3D
2,3D
1,3D
SRG8
R
C1/
54LS164
&
1D
CTRDIV16
M1 [LOAD]
M2 [COUNT]
M3 [UP]
M4 [DOWN]
G5
G6
3,5CT=15
4,5CT=0
2,3,5,6+/C7
2,4,5,6-
54LS169
1,7D


MAX_DELAY=10000
RAM 4x4
54LS170
54LS181
ALU
54LS182
CPG
54LS173
(SIZE)
54LS183
Σ
54LS174
CTRDIV10
54LS190
54LS175

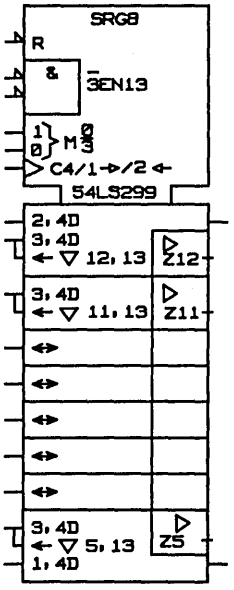

54LS191
CTRDIV16
G1
M2[DOWN] 2<CT=0>Z6
M3 [UP] 3<CT=15>Z6
1,2-/1,3+
G4 6,1,4
C5
54LS191
5D +-
54LS192
CTRDIV10
CT=0
2+
G1
1-
G2
C3
ICT=9
2CT=0
3D
54LS193
CTRDIV16
ICT=15
54LS194
SRG4
R
M
C4
1->/2<-
2,4D
3,4D
54LS195
SRG4
R
M1[SHIFT]
M2[LOAD]
C3/1
2,3D
1,3J
1,3K
&
54LS196
CTR
C1
CT=0
DIV5
1CT
CT
DIV2
1D
54LS197


54LS219
(SIZE)
RAM 16x4
A 0 15
G1
1EN[READ]
1C2[WRITE]
54LS219
A,2D
A
54LS241
(SIZE)
EN
54LS241
PULSE_WIDTH=10000
54LS221
&
1
R
CX
RX/CX
54LS221
54LS242
(SIZE)
EN1
EN2
54LS242
1
2
54LS222
FIFO 16x4
EN7
CTR
CT=0
CT<16
+C1
Z2
2,3
G3
CT>0
Z4
4,5
G5
V6
54LS222
1D
6,7
54LS243
(SIZE)
54LS243
54LS240
(SIZE)
EN
54LS240

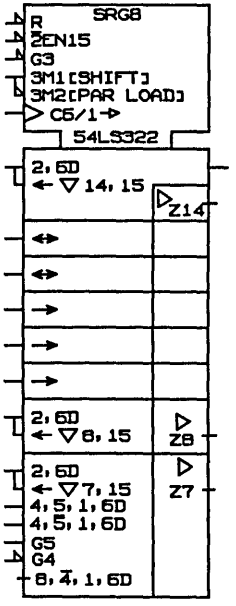

54LS244
(SIZE)
EN
54LS244
54LS257
(SIZE)
EN
G1
54LS257
MUX
54LS245
(SIZE)
G3
3EN1[BA]
3EN2[AB]
54LS245
54LS258
(SIZE)
EN
G1
54LS258
MUX
54LS251
(SIZE)
MUX
54LS251
54LS253
(SIZE)
54LS253
MUX
54LS259
BM
54LS259
9,7D
10,7R
9,6D
10,6R
9,5D
10,5R
9,4D
10,4R
9,3D
10,3R
9,2D
10,2R
9,1D
10,1R
9,0D
10,0R


54LS260
(SIZE)
≥ 1
54LS260
≥ 1
54LS260
54LS283
Σ
3
P
0
3
Q
0
CI
54LS283
Σ
3
0
CO
MAX_DELAY=10000
54LS266
(SIZE)
MAX_DELAY=10000
=1
54LS266
=1
54LS266
54LS290
&
CTR
CT=0
&
Z3
54LS290
DIV5
CT
2
0
+
3CT=4
DIV2
+
3CT=1
54LS293
&
CTR
CT=0
54LS293
DIV8
CT
2
0
+
DIV2
+
54LS273
(SIZE)
R
C1
54LS273
1D
R
C1
54LS273
1D
54LS295
EN
SRG4
M1[LOAD]
M2[SHIFT]
C3/2
54LS295
1,3D
1,3D
2,3D
54LS279
(SIZE)
R
S
54LS279
R
S
S
54LS279
54LS298
(SIZE)
G1
MUX
C2
54LS298
1,2D
1,2D
G1
MUX
C2
54LS298
1,2D
1,2D
54LS280
2K
54LS280

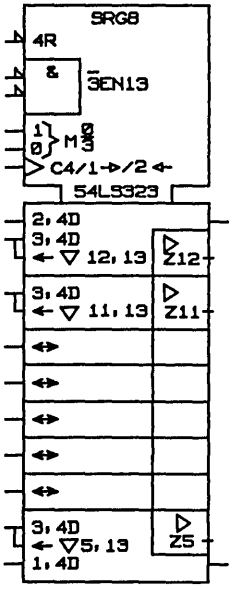
54LS299



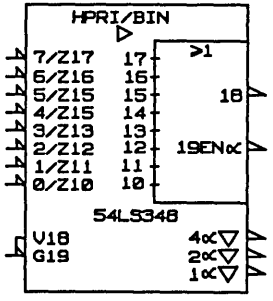
54LS322



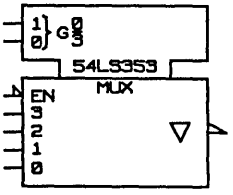
54LS323

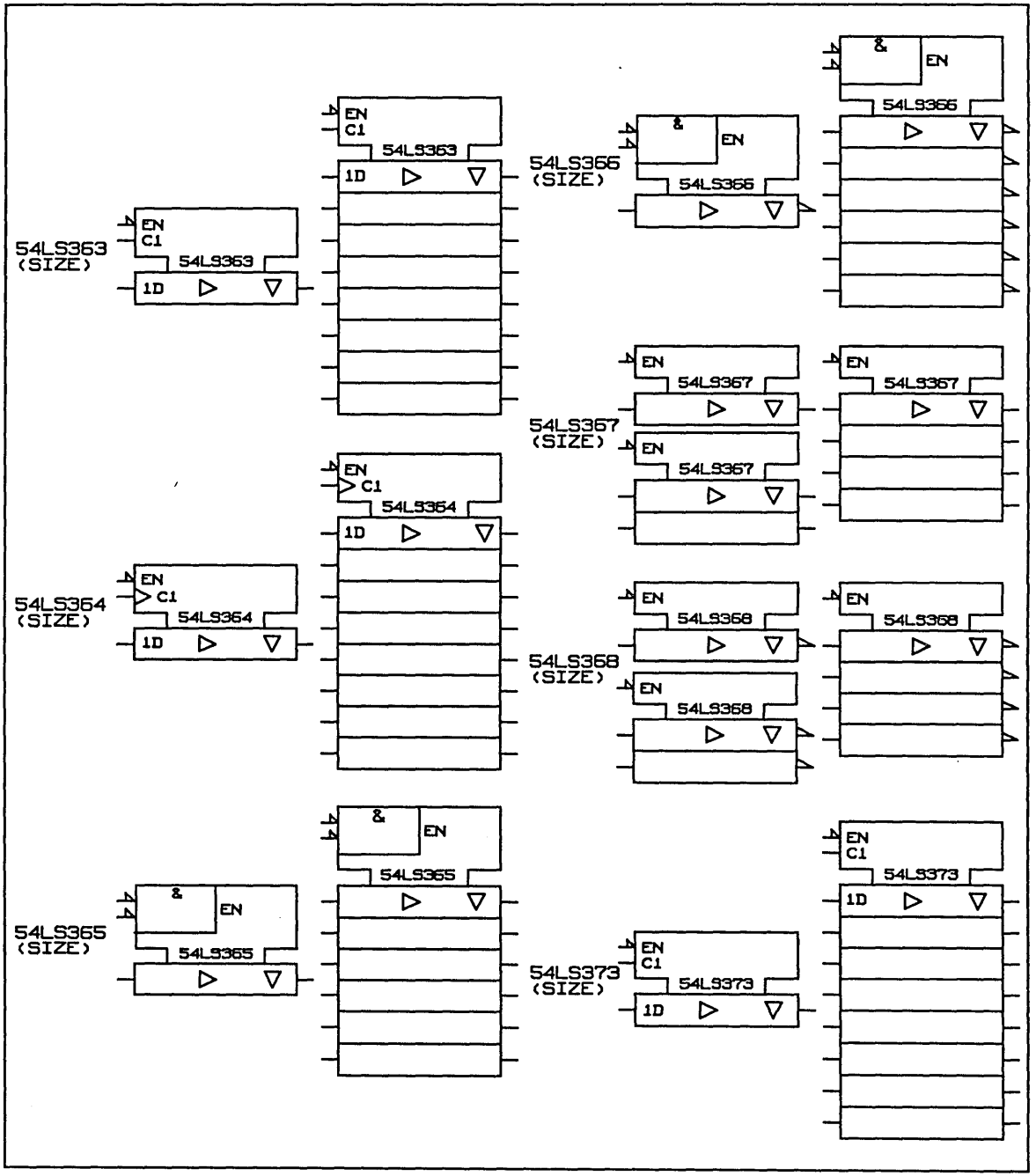


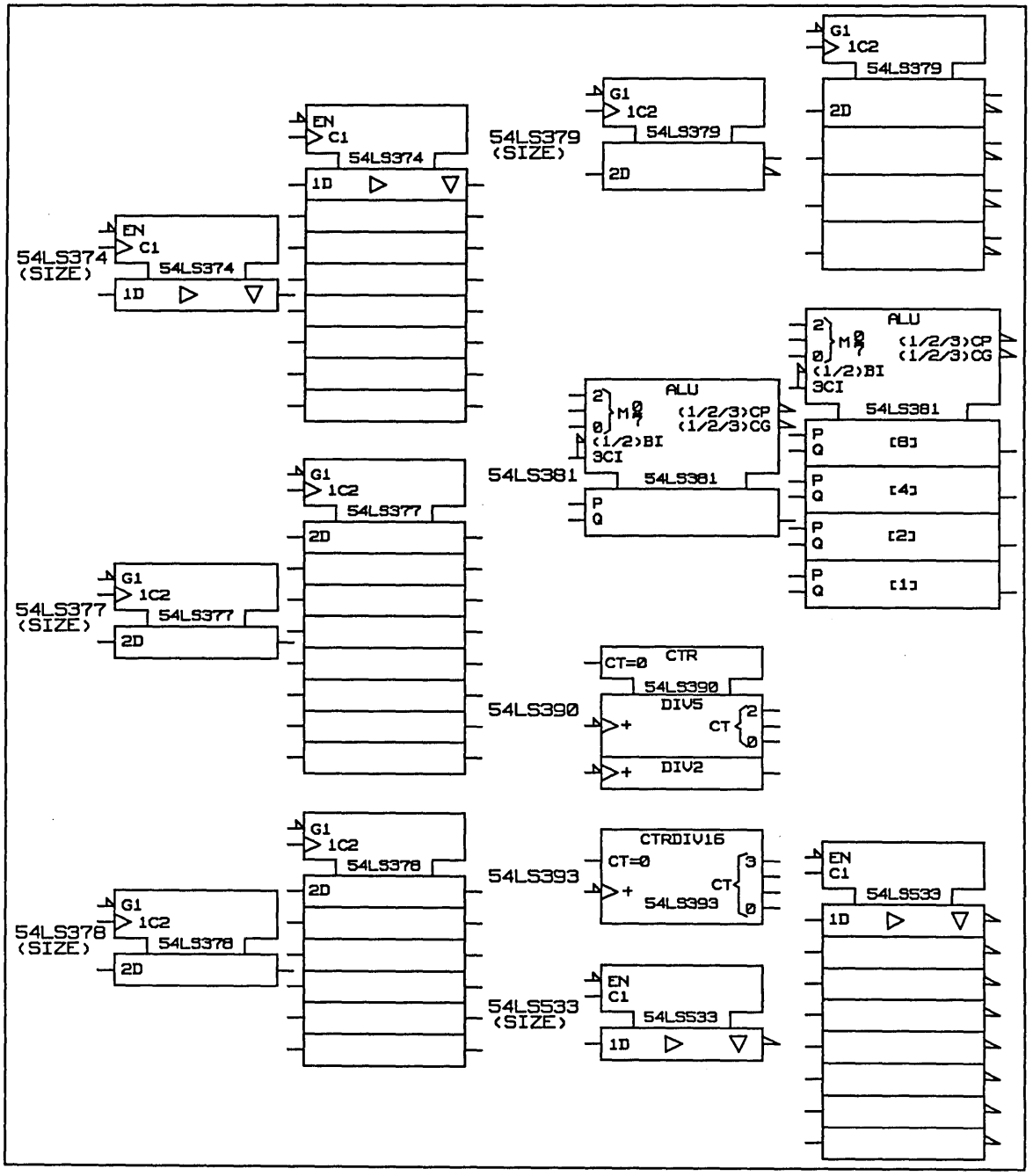
54LS348

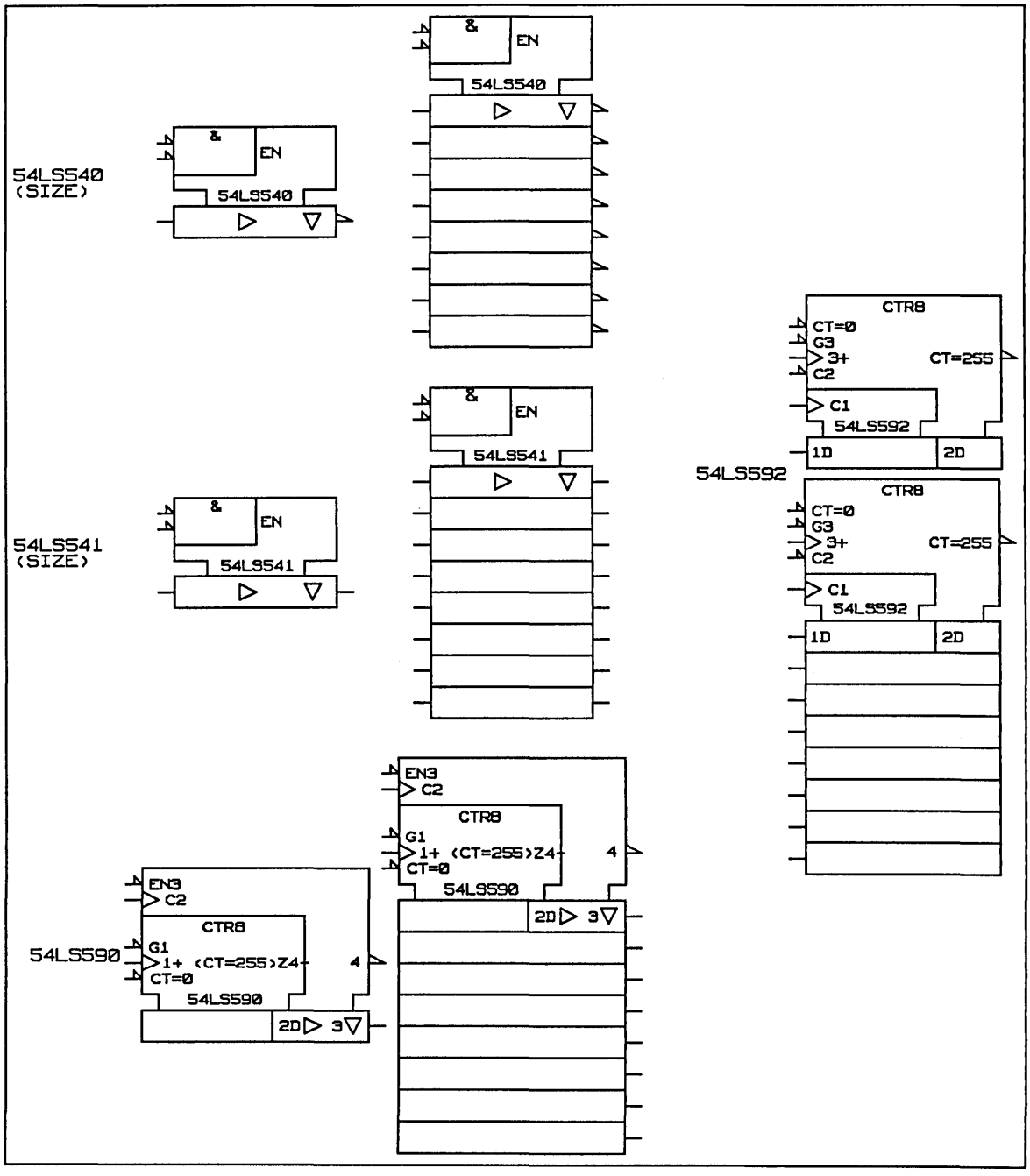


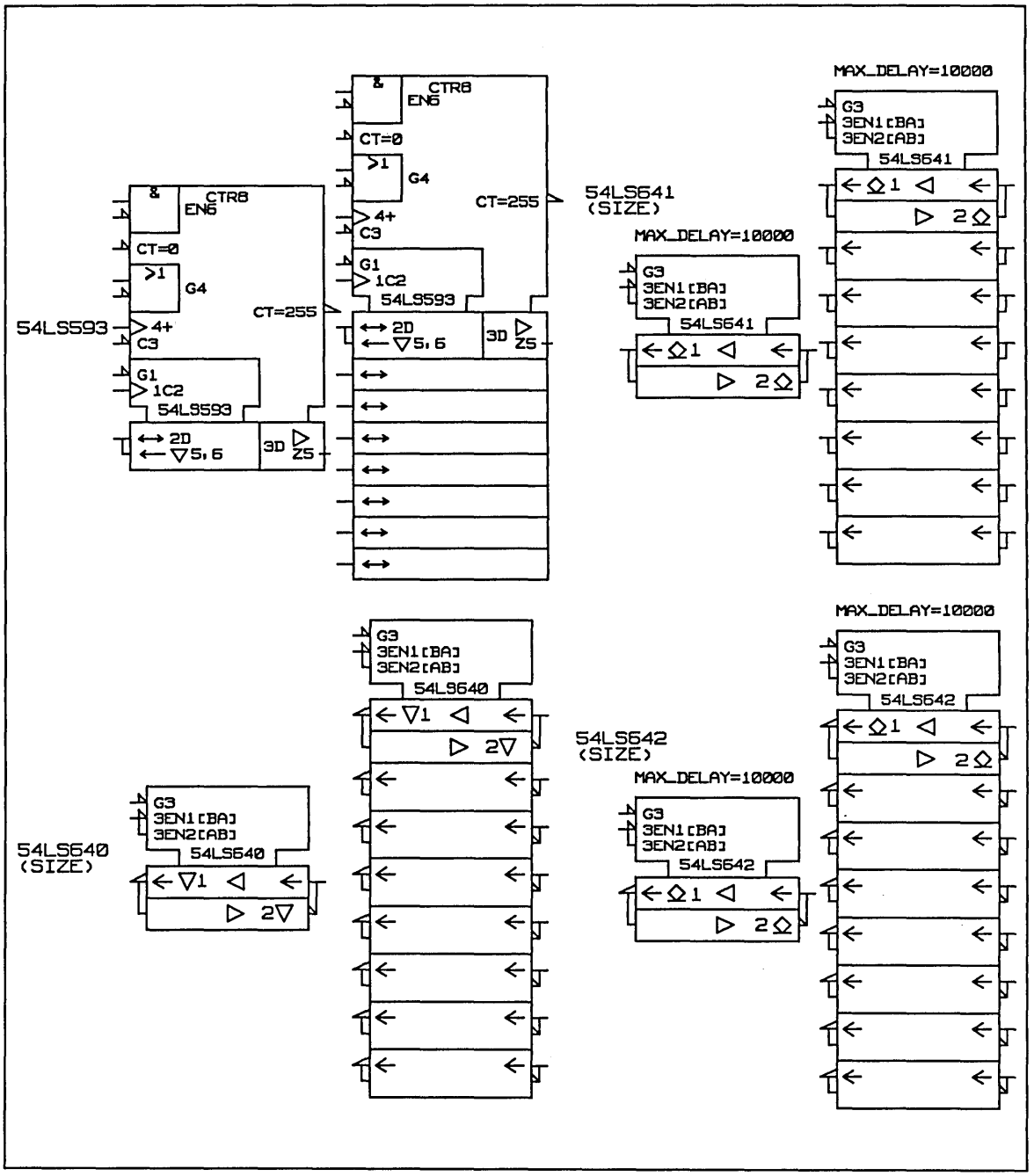
54LS353
(SIZE)

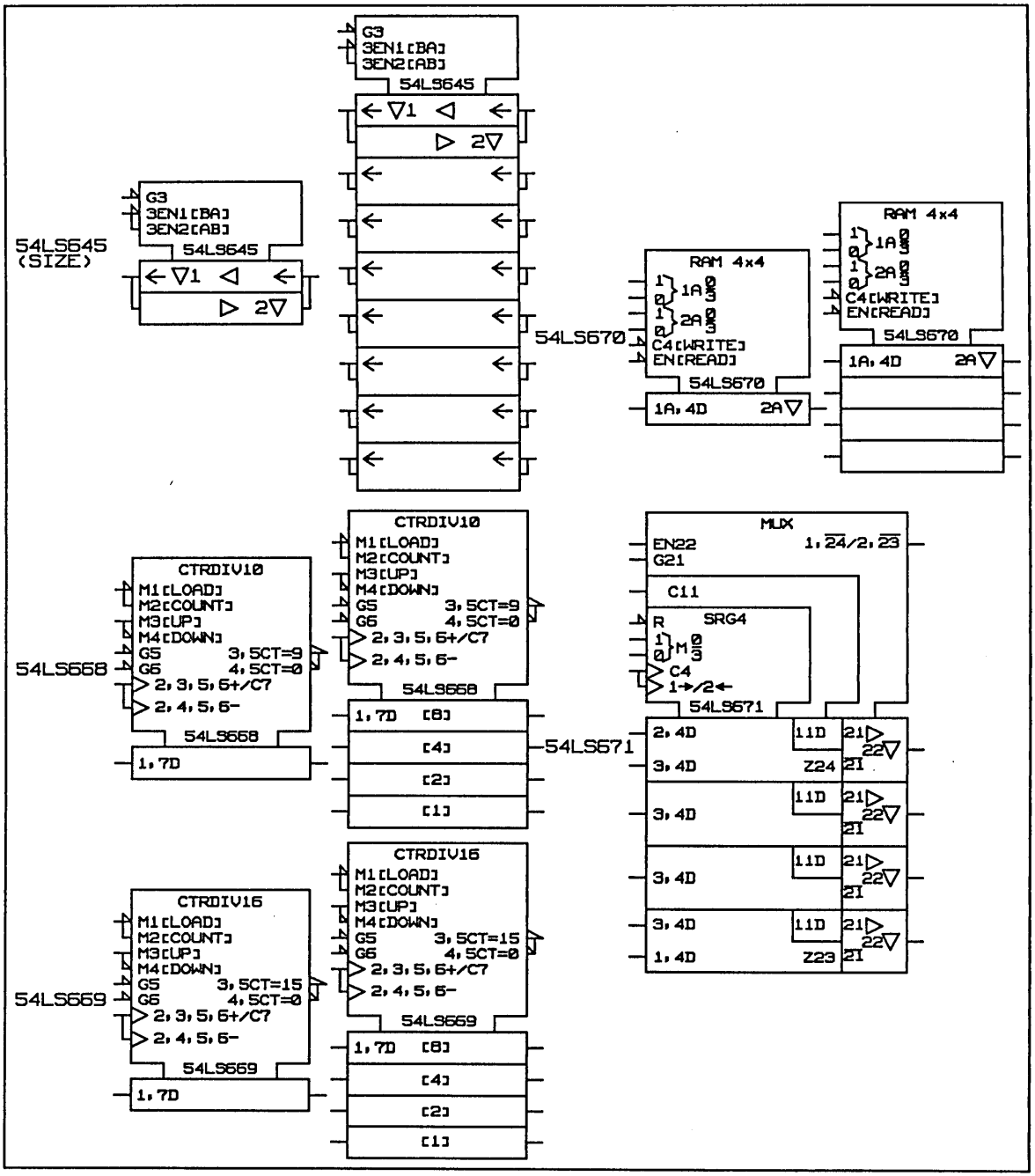


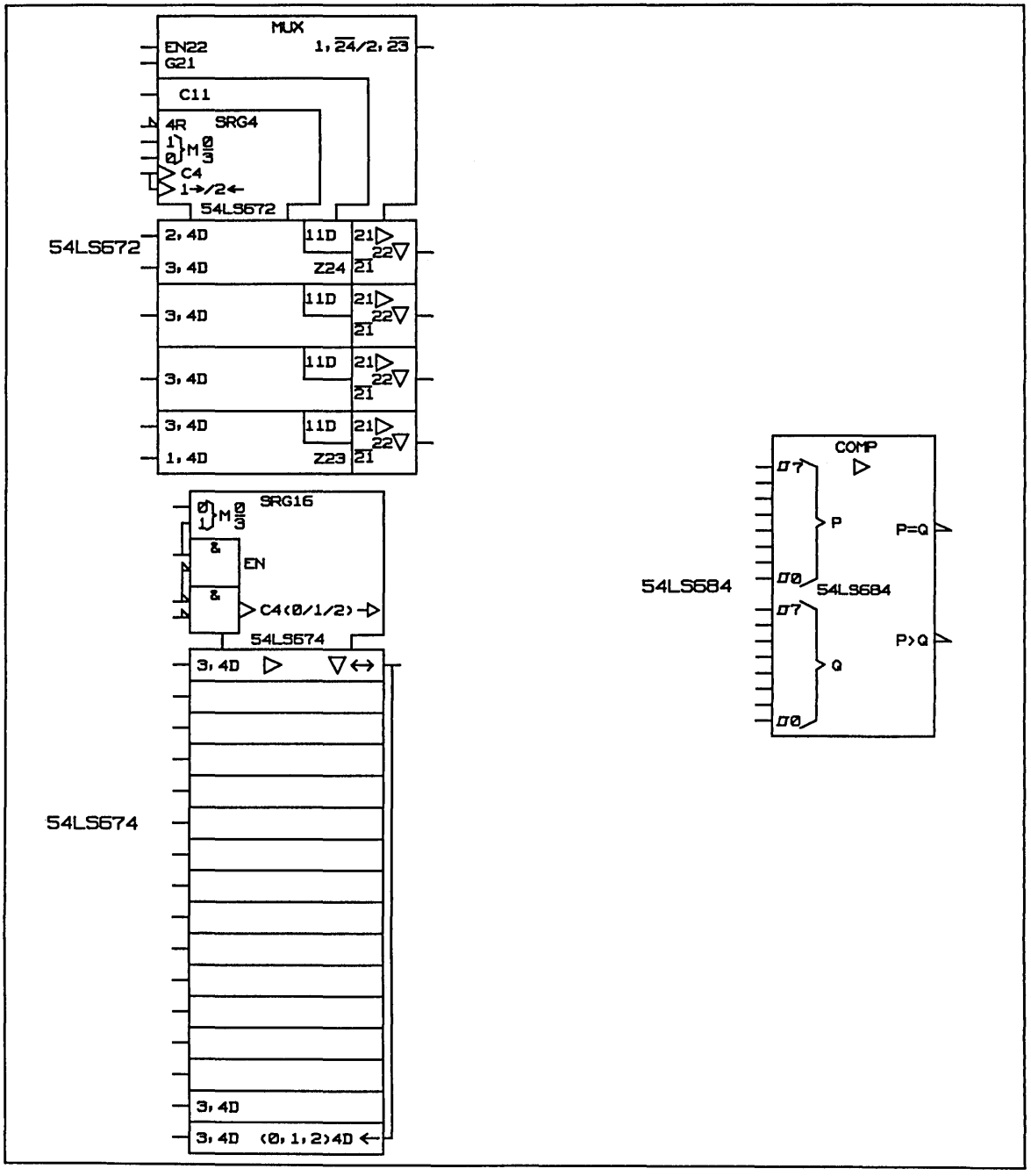

54LS363
(SIZE)
EN
C1
54LS363
1D
54LS364
(SIZE)
EN
C1
54LS364
1D
54LS365
(SIZE)
&
EN
54LS365
54LS366
(SIZE)
&
EN
54LS366
54LS367
(SIZE)
EN
54LS367
54LS368
(SIZE)
EN
54LS368
54LS373
(SIZE)
EN
C1
54LS373
1D


54LS374
(SIZE)
EN
C1
1D
54LS374
54LS379
(SIZE)
G1
1C2
2D
54LS379
54LS377
(SIZE)
54LS377
54LS381
ALU
2
M
0
(1/2/3)CP
(1/2/3)CG
(1/2)BI
3CI
P
Q
[8]
[4]
[2]
[1]
54LS381
54LS390
CT=0
CTR
DIV5
DIV2
CT
54LS390
54LS378
(SIZE)
54LS378
54LS393
CTRDIV16
54LS393
54LS533
(SIZE)
54LS533

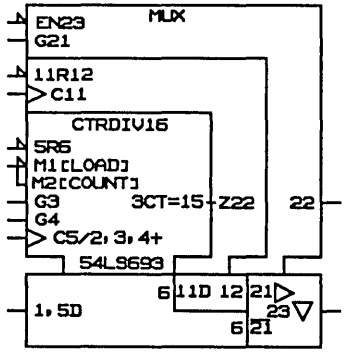

54LS540
(SIZE)
&
EN
54LS540
54LS541
(SIZE)
54LS541
54LS590
EN3
C2
CTR8
G1
1+ (CT=255)Z4
CT=0
4
2D
3
54LS592
CT=0
G3
3+
C2
C1
CT=255
1D
2D

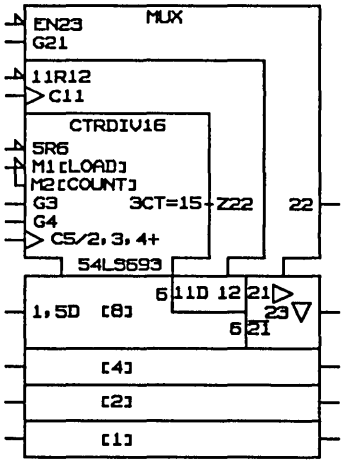

54LS593
54LS641
(SIZE)
54LS640
(SIZE)
54LS642
(SIZE)
MAX_DELAY=10000
CTR8
EN6
CT=0
G4
CT=255
4+
C3
G1
1C2
2D
5,6
3D
Z5
G3
3EN1[BA]
3EN2[AB]


54LS645
(SIZE)
G3
3EN1[BA]
3EN2[AB]
54LS645
54LS670
RAM 4x4
C4[WRITE]
EN[READ]
1A,4D
2A
54LS668
CTRDIV10
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5 3,5CT=9
G6 4,5CT=0
2,3,5,6+/C7
2,4,5,6-
1,7D
[8]
[4]
[2]
[1]
54LS669
CTRDIV16
G5 3,5CT=15
G6 4,5CT=0
54LS671
MUX
EN22
G21
1,2̄4/2,2̄3
C11
R
SRG4
C4
1→/2←
2,4D
3,4D
1,4D
11D
Z24
Z23

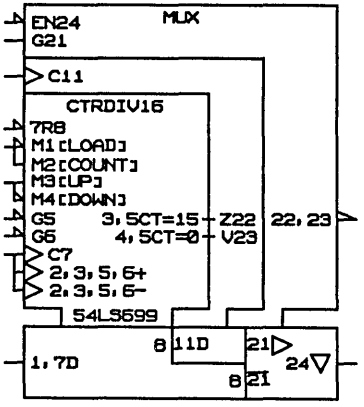

MUX
EN22
G21
1, 2/2, 3
C11
4R
SRG4
M
C4
1→/2←
54LS672
54LS672
2, 4D
3, 4D
11D
21
22
Z24
Z23
SRG16
EN
C4(0/1/2)→
54LS674
54LS674
3, 4D
(0, 1, 2)4D ←
54LS684
COMP
P
Q
P=Q
P>Q
54LS684

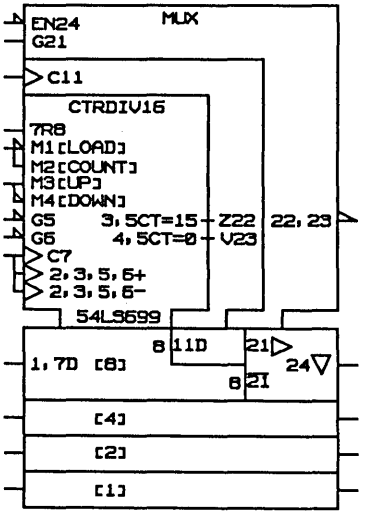
54LS693

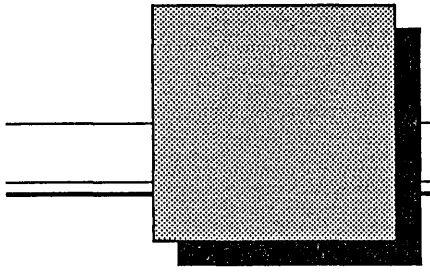




54LS699







The 54STTL and ANSI 54STTL Libraries

The 54STTL Library requires approximately 1891 Kbytes of disk storage, and the ANSI 54STTL Library requires approximately 1878 Kbytes of disk storage. The physical, timing, and simulation models for each library are identical and differ only in their body drawings. The part name for a component in either library is the same; the body drawing used is determined by the first library name encountered in the library search path (*54sttl.lib* or *a54sttl.lib*).

The specifications used to construct the models in these libraries were taken from the Texas Instruments data books or from Mil Spec MIL-M-38510. Parts indicated with an asterisk (*) are from MIL-M-38510; the descriptions for these components include the military device type in parentheses.

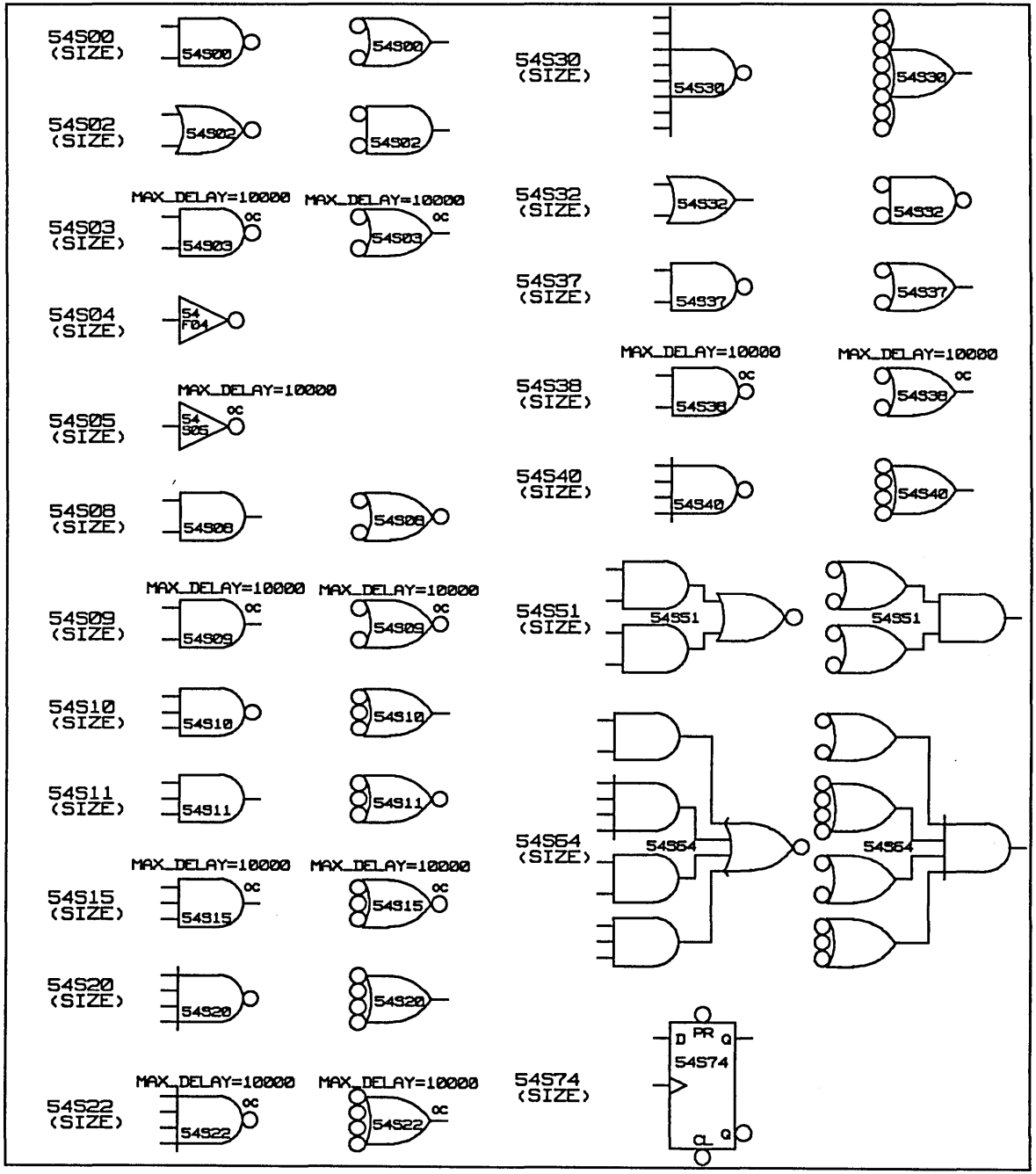
The release level of the 54STTL and ANSI 54STTL Libraries is 9.0.

Each library contains body drawings and physical, timing, and simulation models for the following 59 components:

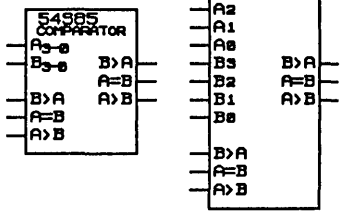
* **54S00**	Quad 2-input NAND (07001)
* **54S02**	Quad 2-input NOR (07301)
* **54S03**	Quad 2-input open-collector NAND (07002)
* **54S04**	Hex inverter (07003)
* **54S05**	Hex open-collector inverter (07004)
* **54S08**	Quad 2-input AND (08003)
* **54S09**	Quad 2-input open-collector AND (08004)
* **54S10**	Triple 3-input NAND (07005)
* **54S11**	Triple 3-input AND (08001)
* **54S15**	Triple 3-input open-collector AND (08002)
* **54S20**	Dual 4-input NAND (07006)
* **54S22**	Dual 4-input open-collector NAND (07007)
* **54S30**	8-input NAND
54S32	Quad 2-input OR
54S37	Quad 2-input NAND buffer
54S38	Quad 2-input open-collector NAND buffer
* **54S40**	Dual 4-input positive NAND buffer (07201)
* **54S51**	2-wide 3-input, 2-wide 2-input AND-OR-invert (07401)
* **54S64**	4-2-3-2 input AND-OR-invert gates (07402)
* **54S74**	Dual positive-edge-triggered D flip-flop (07101)

* **54S85**	4-bit magnitude comparator (08201)
* **54S86**	Quad 2-input exclusive-OR (07501)
54S109	Dual JKbar positive-edge-triggered flip-flop
* **54S112**	Dual JK negative-edge-triggered flip-flop (07102)
54S132	Quad 2-input positive NAND Schmitt triggers
* **54S133**	13-input positive NAND gates
* **54S138**	3-to-8 line decoders/multiplexers (07701)
* **54S139**	Dual 2-to-4 line decoders/multiplexers (07702)
* **54S140**	Dual 4-input positive NAND 50-ohm line drivers (08101)
* **54S151**	1-of-8 data selectors/multiplexers (07901)
* **54S153**	Dual 4-line to 1-line data multiplexer (07902)
* **54S157**	Quad 2-to-1-line non-inverting multiplexer (07903)
* **54S158**	Quad 2-to-1-line inverting data multiplexer (07904)
54S162	4-bit synchronous decade counters with synchronous clear
54S163	4-bit synchronous binary counters with synchronous clear
54S169	4-bit synchronous binary up/down counters
* **54S174**	Hex D-type flip-flops (07105)
* **54S175**	Quad D-type flip-flops (07106)
* **54S181**	Arithmetic logic units/function generators (07801)
* **54S182**	Look-ahead carry generators (07802)

54S189	64-bit random access memories
* **54S194**	4-bit bidirectional shift register (07601)
54S201	256-bit random memories
54S225	Asynchronous first-in first-out memories
54S240	Octal inverting 3-state bus transceiver
54S241	Octal non-inverting 3-state bus transceiver
54S244	Octal non-inverting 3-state bus transceiver
* **54S251**	3-state data multiplexer (07905)
* **54S253**	Dual data selectors/multiplexers (07908)
* **54S257**	Quad 3-state non-inverting data multiplexer (07906)
* **54S258**	Quad 3-state inverting data multiplexer (07907)
54S260	Dual 5-input positive NOR gates
54S280	9-bit odd/even parity generators/checkers
54S283	4-bit binary full adders
54S299	8-bit bidirectional 3-state shift/storage register
54S373	Octal 3-state D-latch with common enable
54S374	Octal 3-state positive-edge-triggered D register
54S381	Arithmetic logic unit/function generator
54S471	Programmable read-only memories

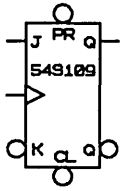

54S00
(SIZE)
54S00
54S00
54S02
(SIZE)
54S02
54S02
MAX_DELAY=10000
MAX_DELAY=10000
54S03
(SIZE)
54S03
54S03
54S04
(SIZE)
54
F04
MAX_DELAY=10000
54S05
(SIZE)
54
S05
54S08
(SIZE)
54S08
54S08
MAX_DELAY=10000
MAX_DELAY=10000
54S09
(SIZE)
54S09
54S09
54S10
(SIZE)
54S10
54S10
54S11
(SIZE)
54S11
54S11
MAX_DELAY=10000
MAX_DELAY=10000
54S15
(SIZE)
54S15
54S15
54S20
(SIZE)
54S20
54S20
MAX_DELAY=10000
MAX_DELAY=10000
54S22
(SIZE)
54S22
54S22
54S30
(SIZE)
54S30
54S30
54S32
(SIZE)
54S32
54S32
54S37
(SIZE)
54S37
54S37
MAX_DELAY=10000
MAX_DELAY=10000
54S38
(SIZE)
54S38
54S38
54S40
(SIZE)
54S40
54S40
54S51
(SIZE)
54S51
54S51
54S64
(SIZE)
54S64
54S64
54S74
(SIZE)
D
PR
Q
54S74
CL
Q

54S85

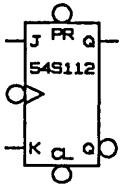


54S86
(SIZE)

54S109
(SIZE)

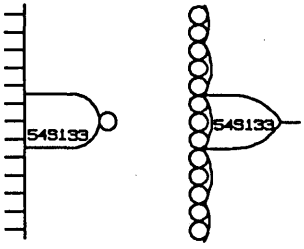


54S112
(SIZE)

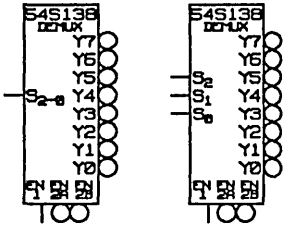


54S132
(SIZE)

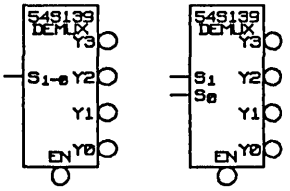
54S133
(SIZE)



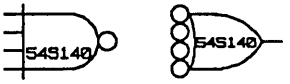
54S138



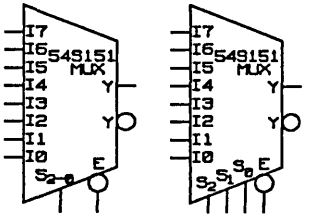
54S139



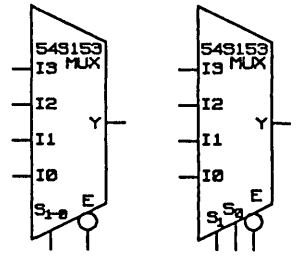
54S140
(SIZE)

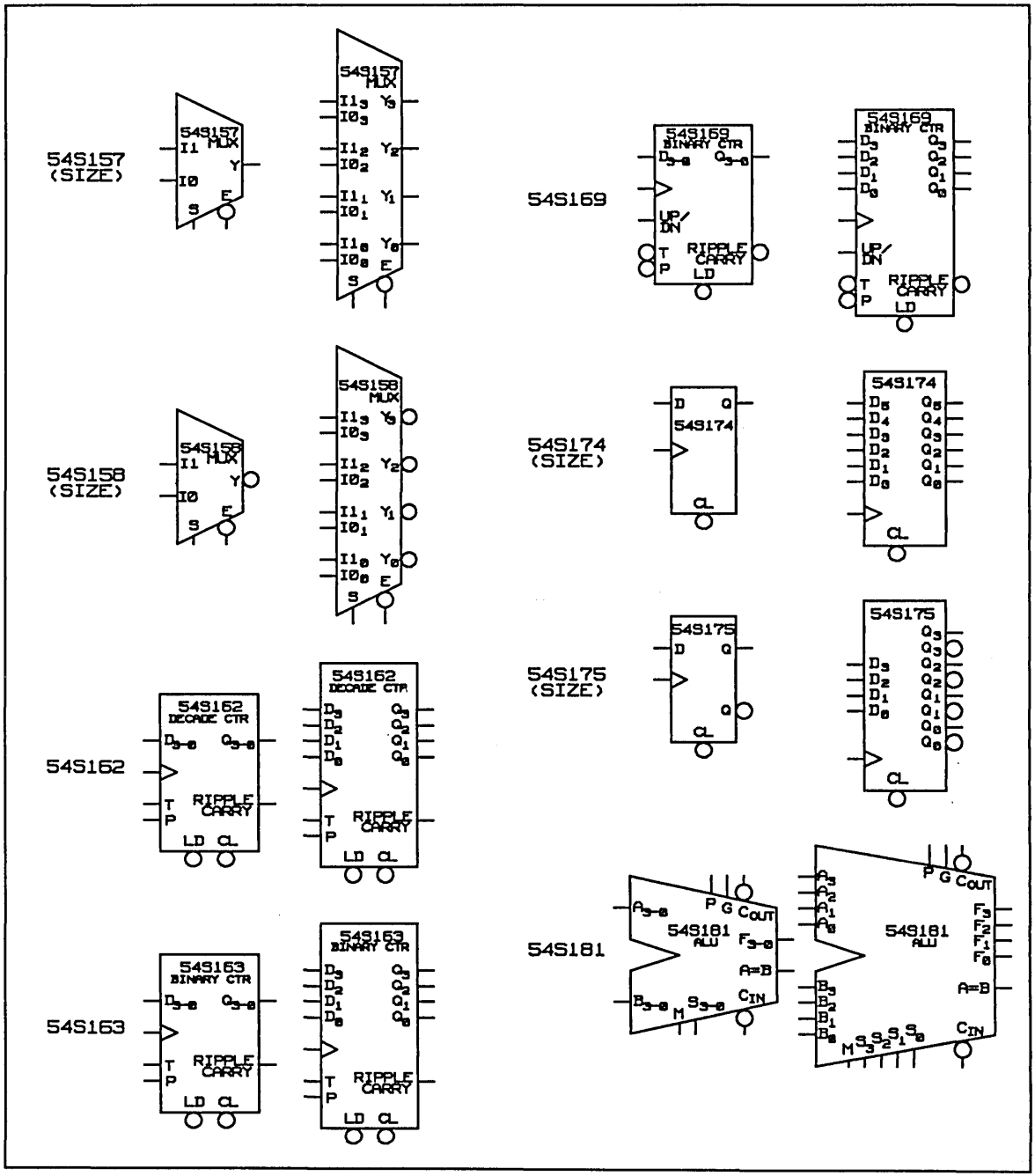


54S151
(SIZE)

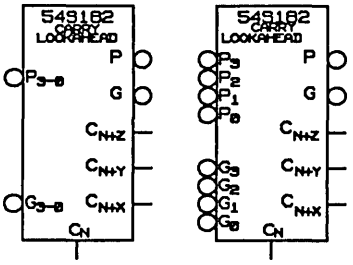


54S153
(SIZE)

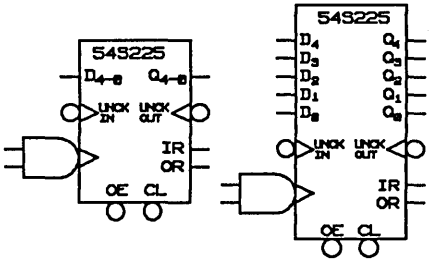



54S157
(SIZE)
54S157
MUX
54S158
(SIZE)
54S158
MUX
54S162
54S162
DECADE CTR
54S163
54S163
BINARY CTR
54S169
54S169
BINARY CTR
54S174
(SIZE)
54S174
54S175
(SIZE)
54S175
54S181
54S181
ALU
RIPPLE CARRY
LD
CL
UP/DN
A=B

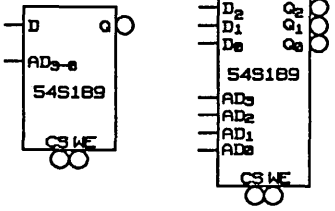
54S182



54S225



54S189 (SIZE)



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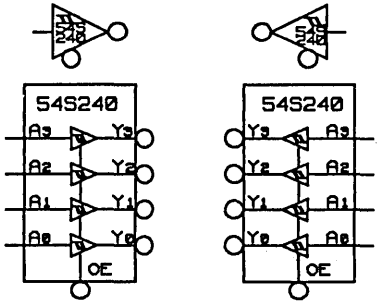
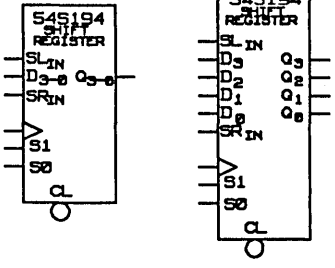


54S194



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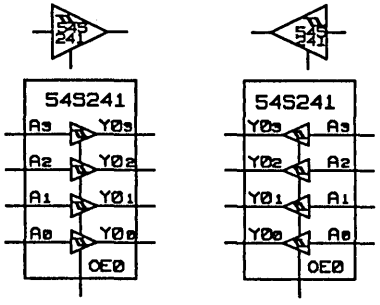

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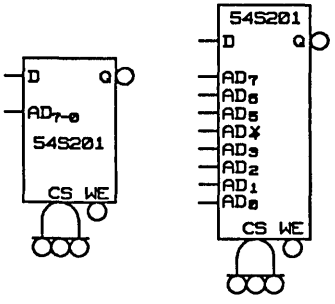

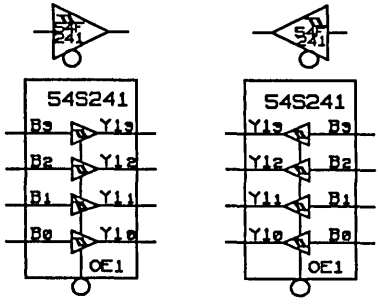

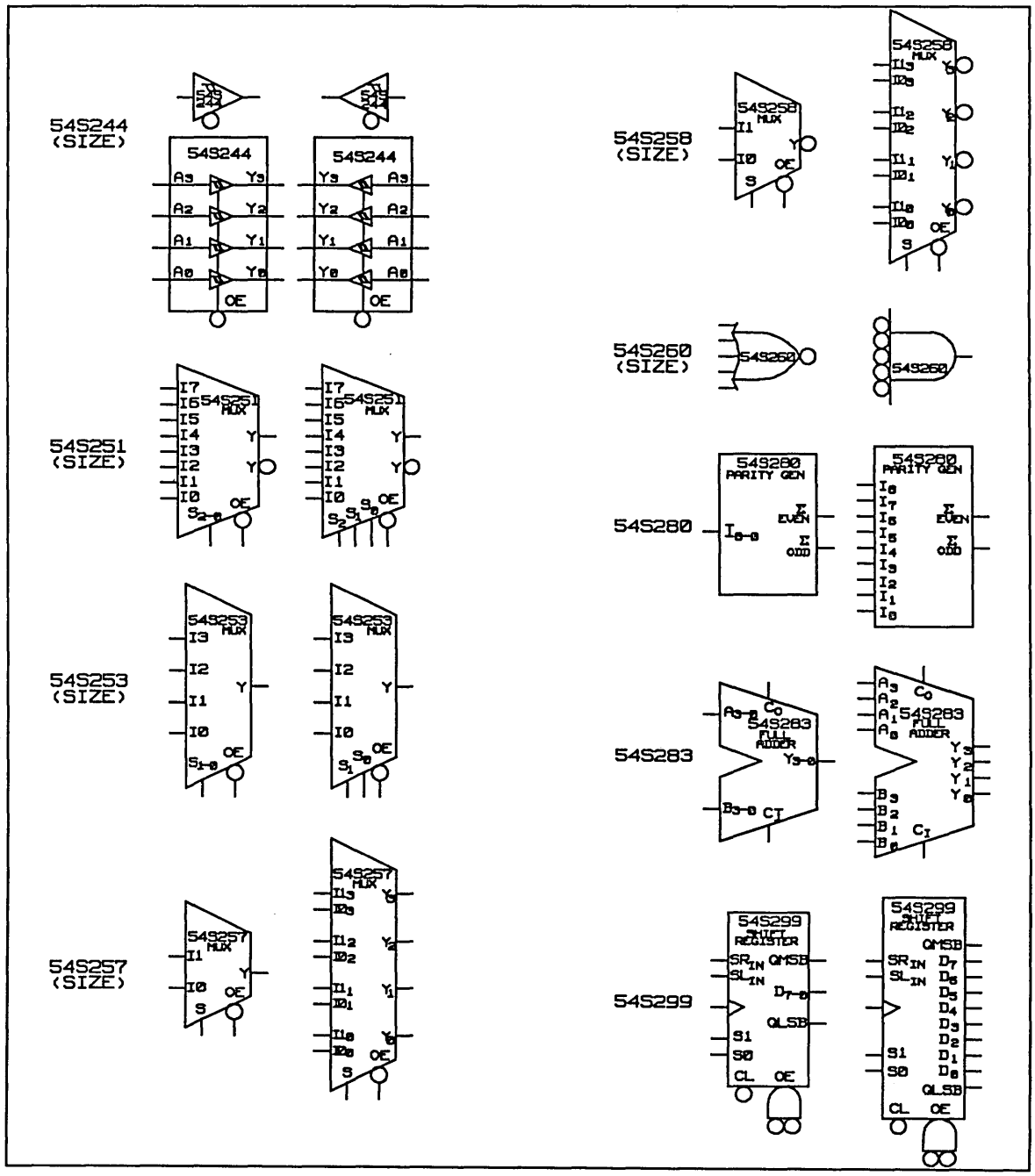
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54S244
54S244
54S251
(SIZE)
54S251
54S251
54S253
(SIZE)
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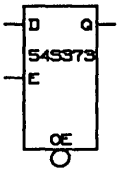
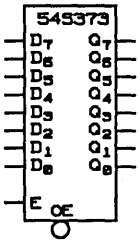
54S253
54S257
(SIZE)
54S257
54S257
54S258
(SIZE)
54S258
54S258
54S260
(SIZE)
54S260
54S260
54S280
54S280
PARITY GEN
54S280
PARITY GEN
54S283
54S283
FULL ADDER
54S283
FULL ADDER
54S299
54S299
SHIFT REGISTER
54S299
SHIFT REGISTER

54S373
(SIZE)





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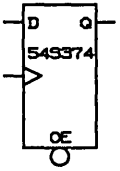
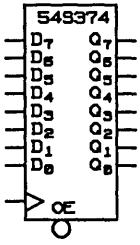
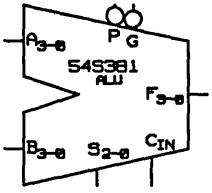
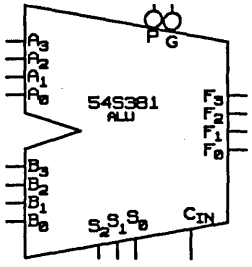


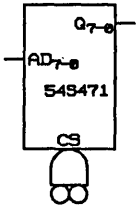


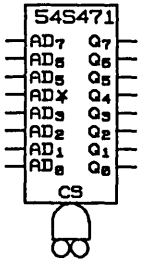
54S381

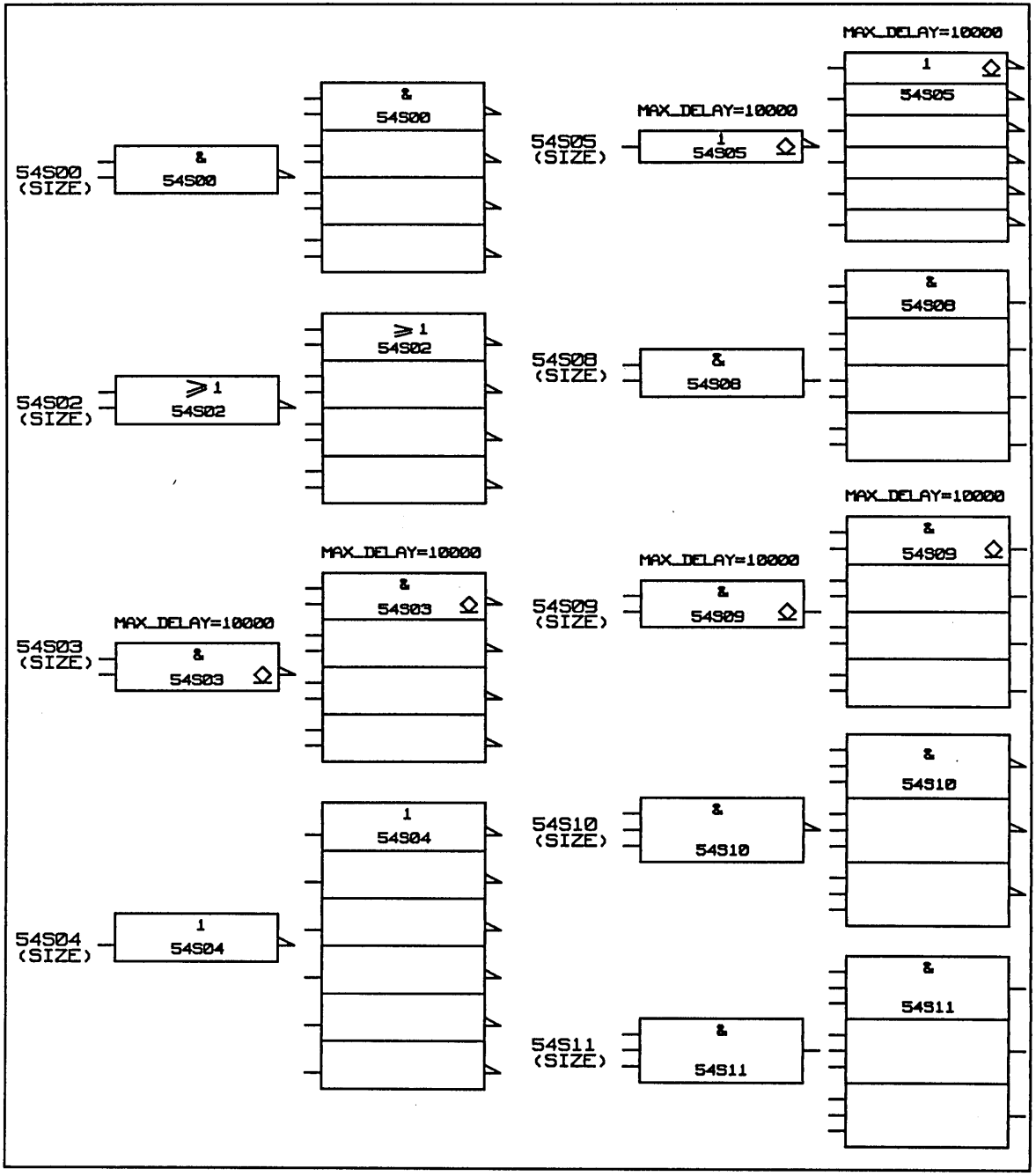


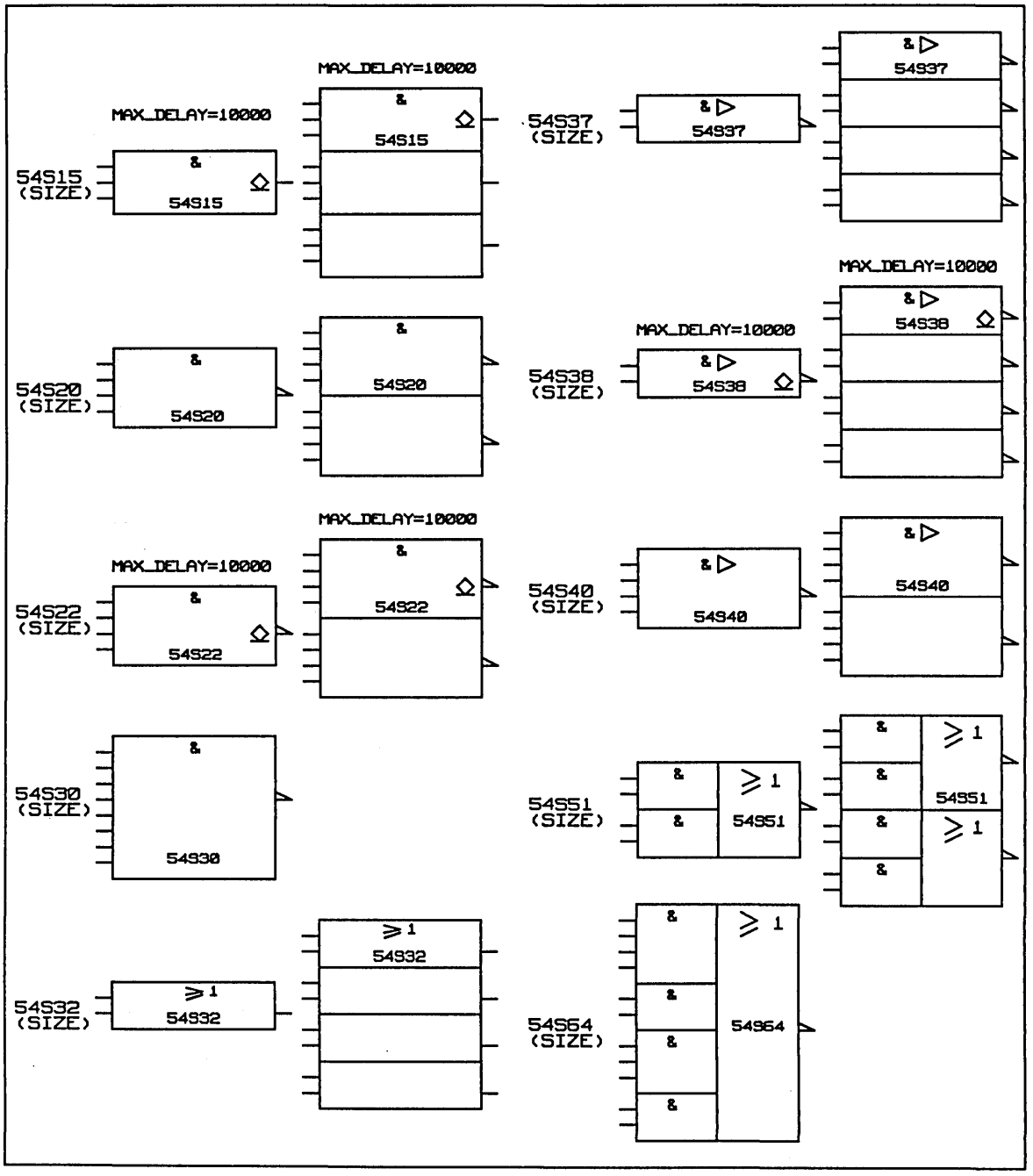


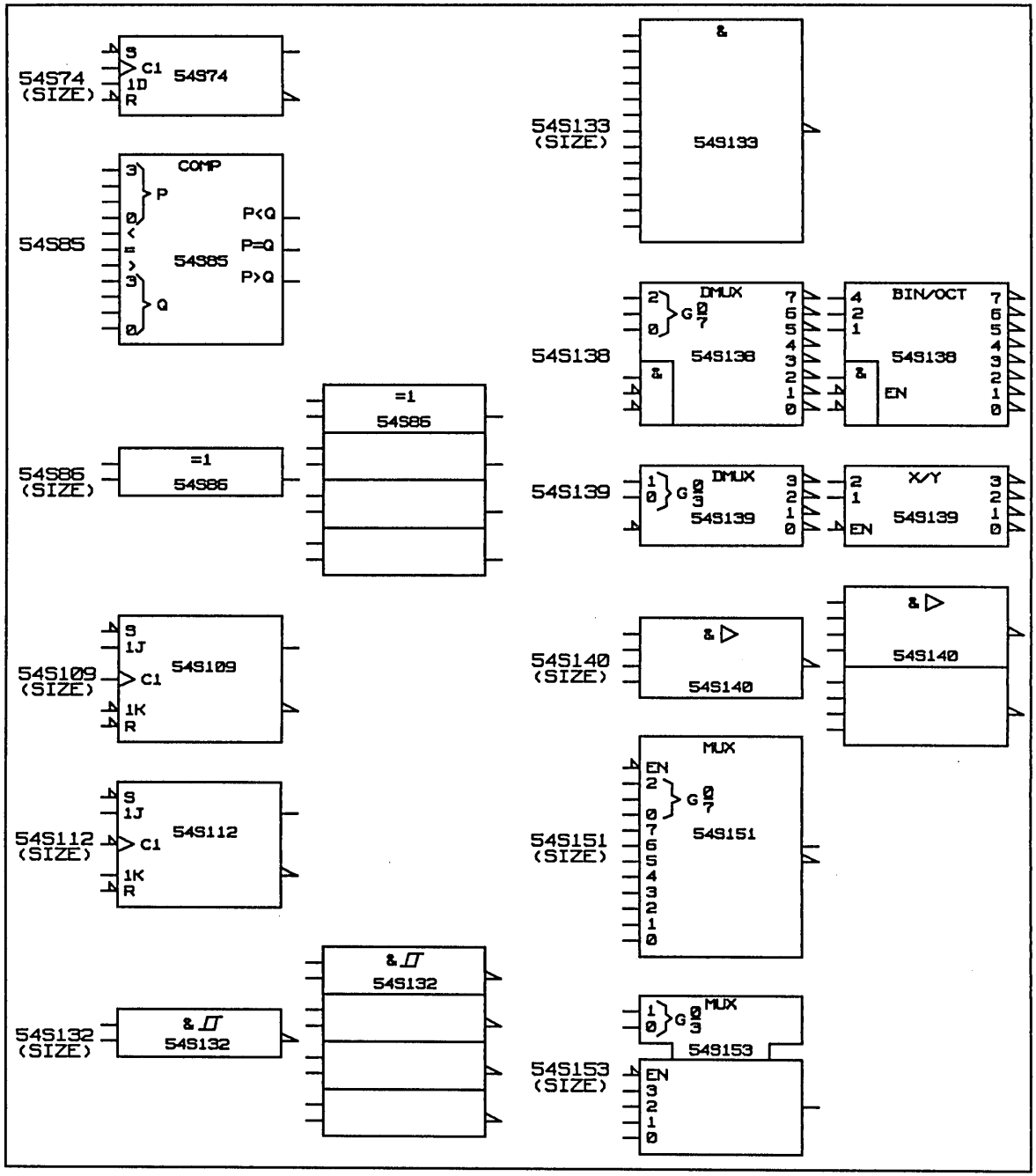
54S471

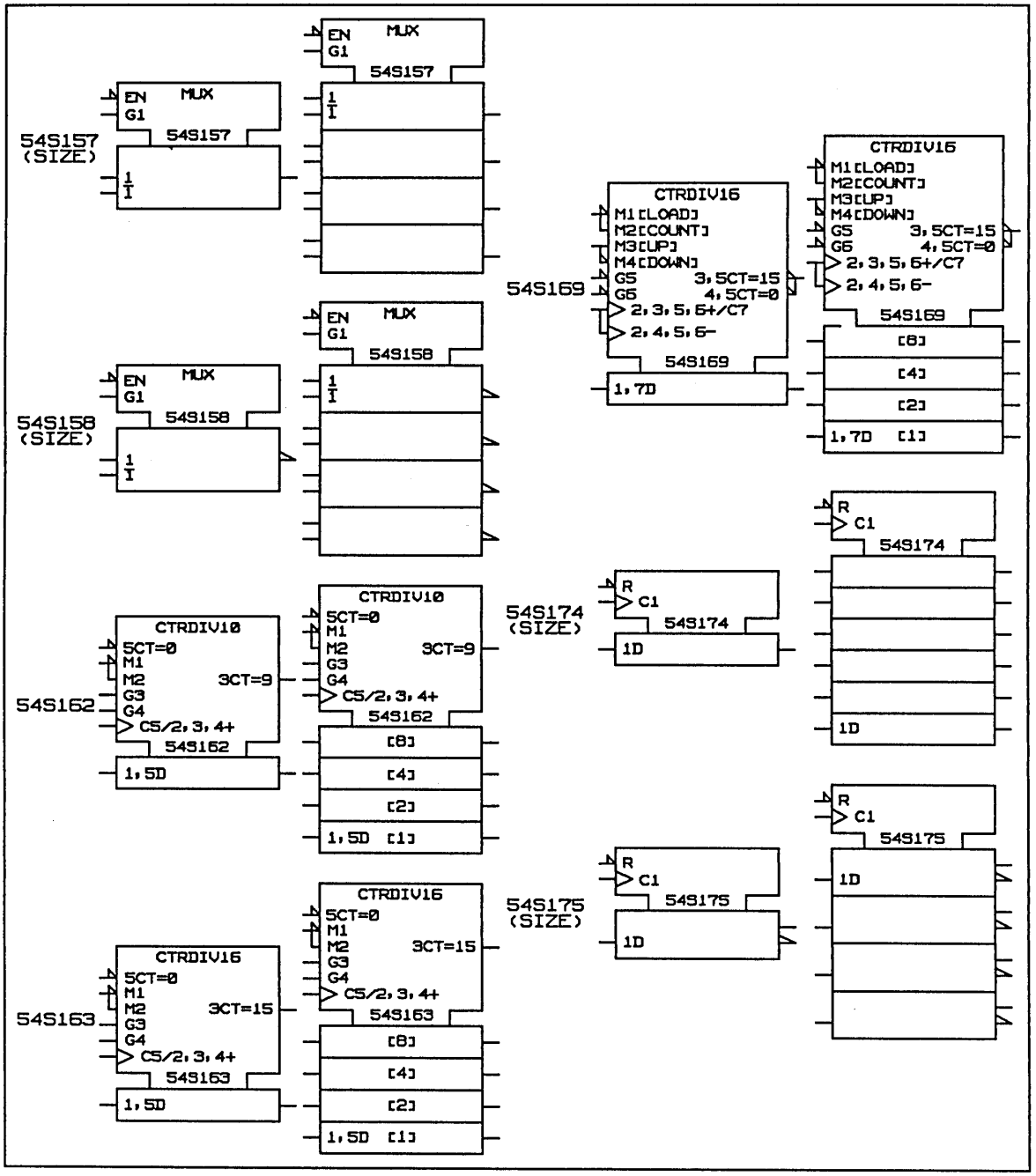


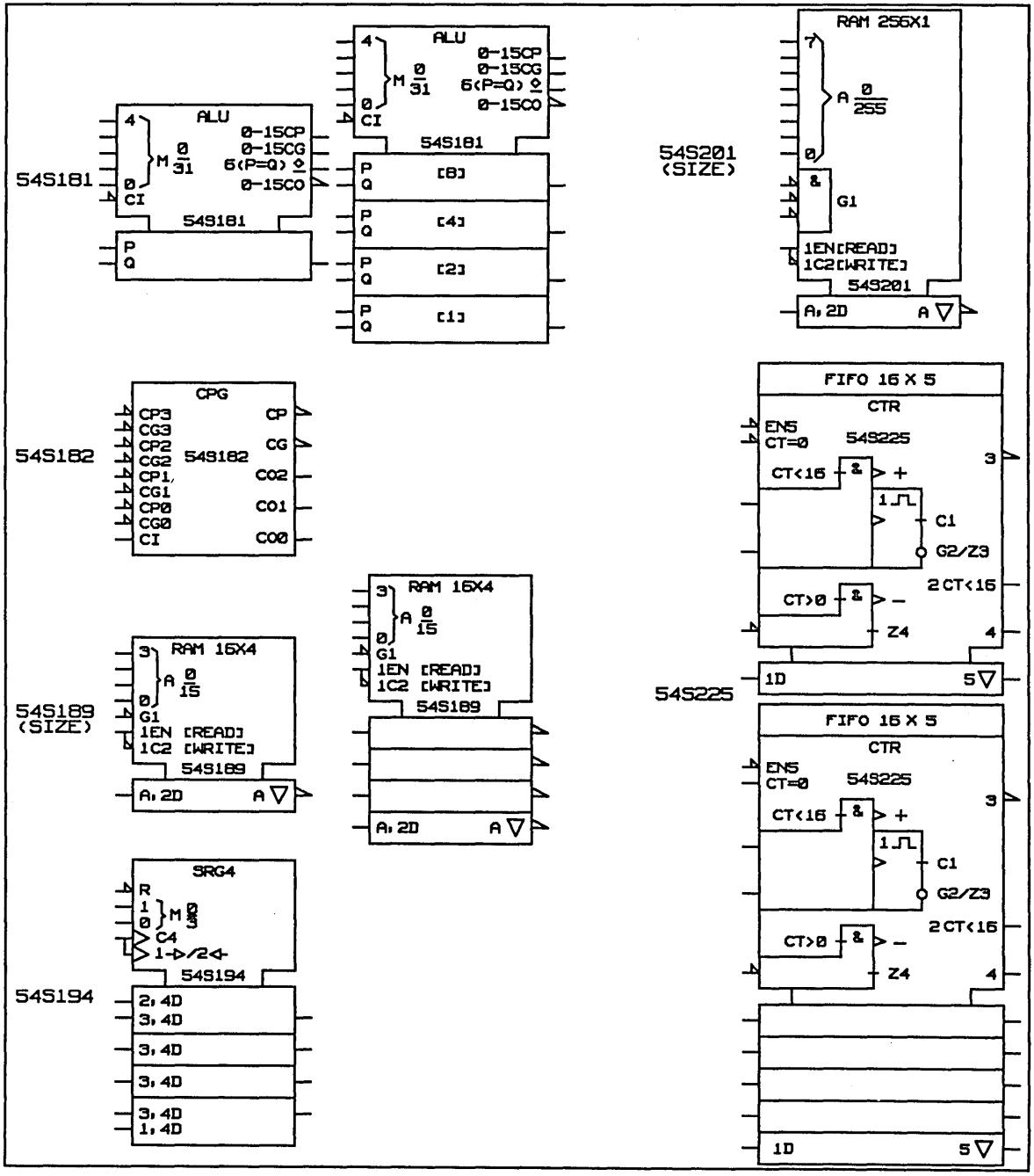


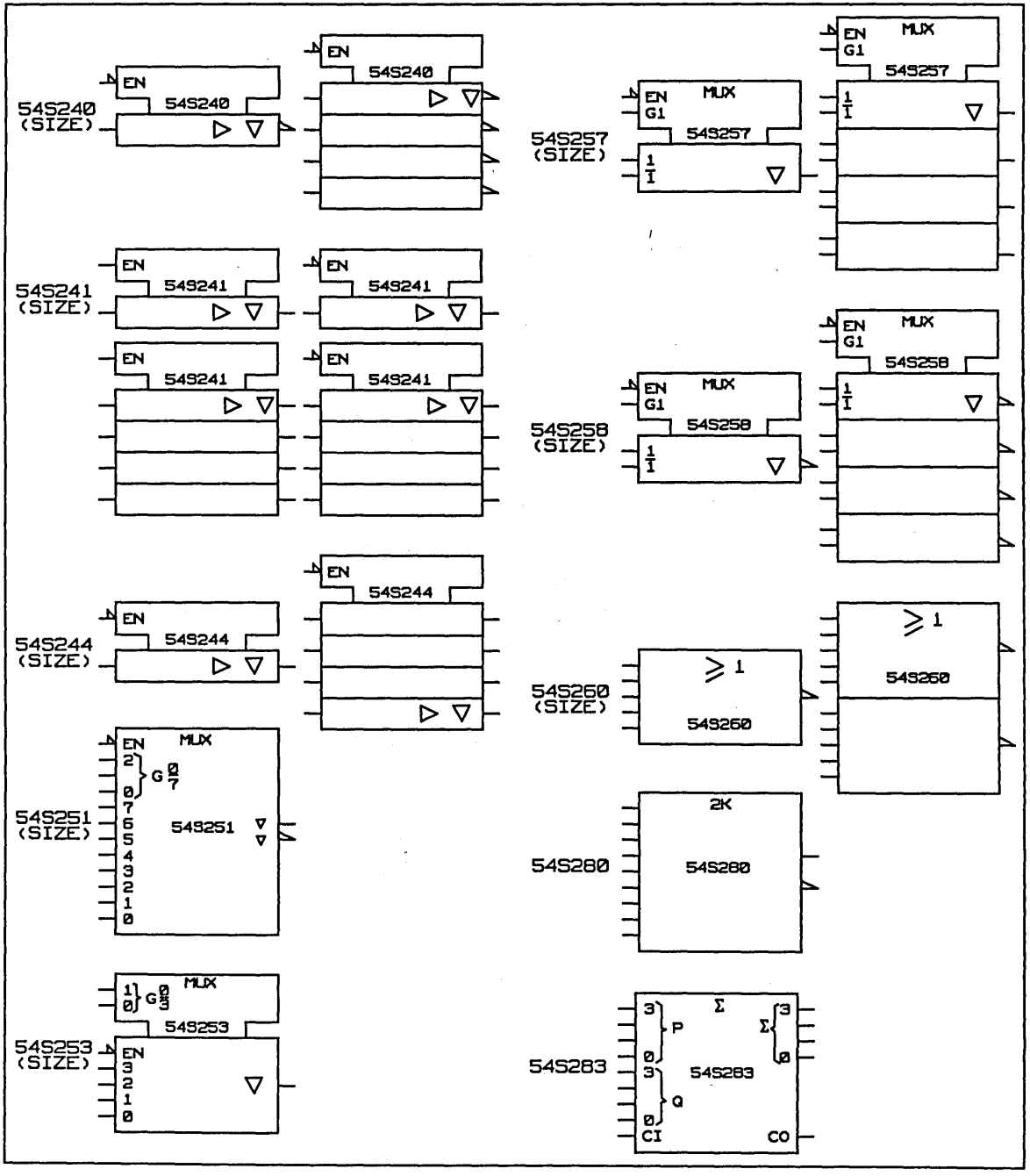

54S00
(SIZE)
&
54S00
&
54S00
54S02
(SIZE)
≥1
54S02
≥1
54S02
MAX_DELAY=10000
54S03
(SIZE)
&
54S03
MAX_DELAY=10000
&
54S03
54S04
(SIZE)
1
54S04
1
54S04
54S05
(SIZE)
MAX_DELAY=10000
1
54S05
MAX_DELAY=10000
1
54S05
54S08
(SIZE)
&
54S08
&
54S08
54S09
(SIZE)
MAX_DELAY=10000
&
54S09
MAX_DELAY=10000
&
54S09
54S10
(SIZE)
&
54S10
&
54S10
54S11
(SIZE)
&
54S11
&
54S11

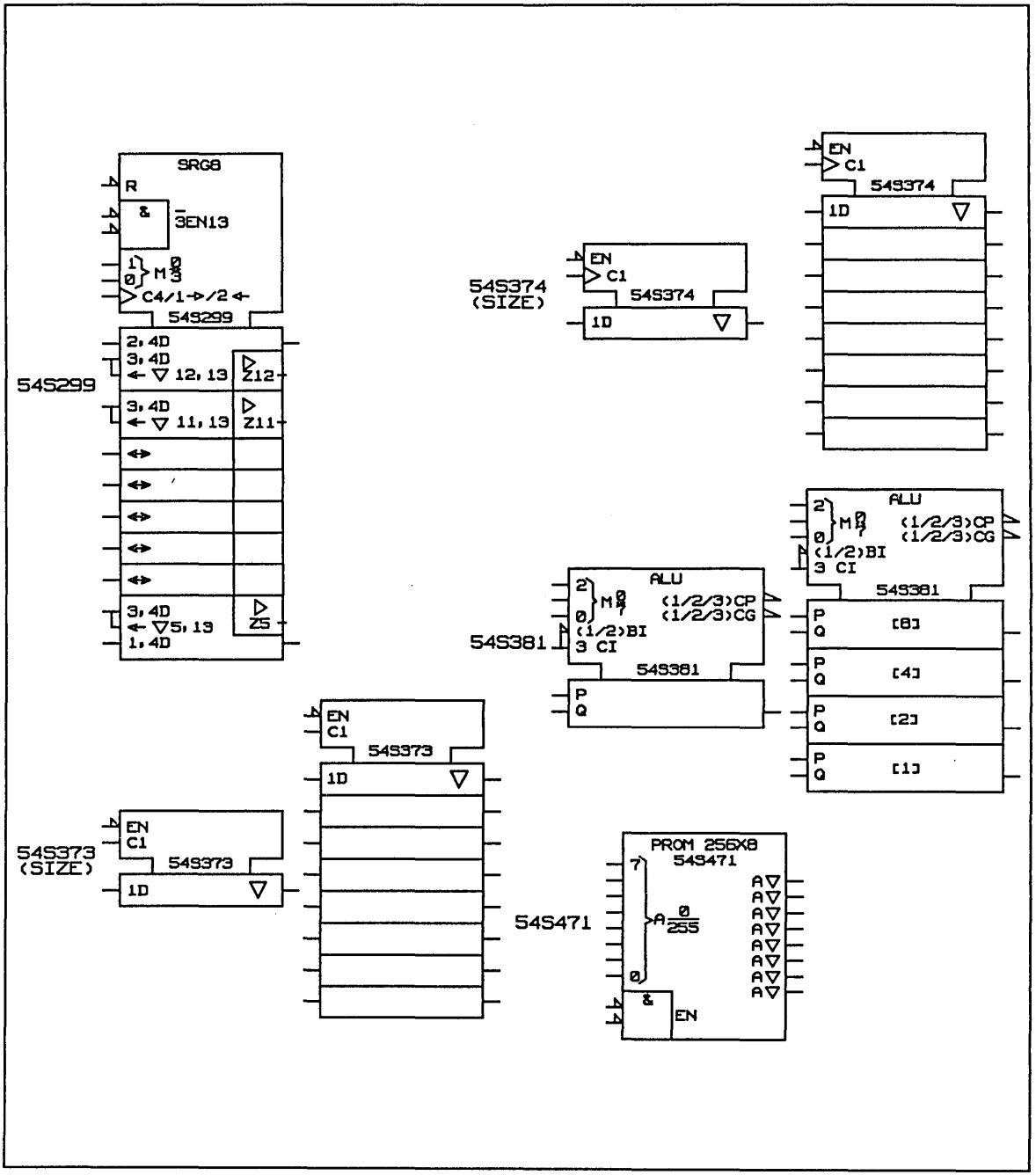

MAX_DELAY=10000
MAX_DELAY=10000
54S15
(SIZE)
54S15
54S15
54S20
(SIZE)
54S20
54S20
MAX_DELAY=10000
MAX_DELAY=10000
54S22
(SIZE)
54S22
54S22
54S30
(SIZE)
54S30
54S32
(SIZE)
54S32
54S32
54S37
(SIZE)
54S37
54S37
MAX_DELAY=10000
MAX_DELAY=10000
54S38
(SIZE)
54S38
54S38
54S40
(SIZE)
54S40
54S40
54S51
(SIZE)
54S51
54S51
54S64
(SIZE)
54S64

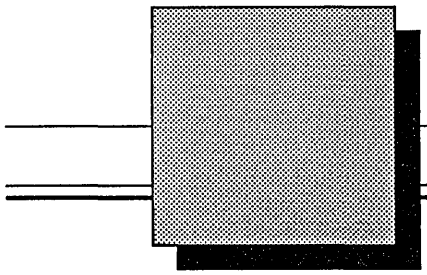

54S74
(SIZE)
S
C1
1D
R
54S74
54S85
COMP
P
P<Q
P=Q
P>Q
Q
54S86
(SIZE)
=1
54S86
54S109
(SIZE)
1J
1K
54S109
54S112
(SIZE)
54S112
54S132
(SIZE)
&
54S132
54S133
(SIZE)
54S133
54S138
DMUX
G
54S138
BIN/OCT
EN
54S139
X/Y
54S139
54S140
(SIZE)
54S140
54S151
(SIZE)
MUX
54S151
54S153
(SIZE)
54S153


MUX
EN
G1
54S157
54S157
(SIZE)
1
I
54S158
(SIZE)
CTRDIV10
5CT=0
M1
M2
3CT=9
G3
G4
C5/2,3,4+
54S162
1,5D
[8]
[4]
[2]
[1]
CTRDIV16
5CT=0
3CT=15
54S163
CTRDIV16
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5
3,5CT=15
G6
4,5CT=0
2,3,5,6+/C7
2,4,5,6-
54S169
1,7D
R
C1
54S174
1D
54S175


54S181
ALU
4
M 0 31
0
CI
0-15CP
0-15CG
6(P=Q)
0-15CO
54S181
P
Q
[8]
[4]
[2]
[1]
54S201
(SIZE)
RAM 256X1
7
A 0 255
&
G1
1EN[READ]
1C2[WRITE]
54S201
A, 2D
A
54S182
CPG
CP3
CG3
CP2
CG2
CP1,
CG1
CP0
CG0
CI
54S182
CP
CG
C02
C01
C00
54S189
(SIZE)
RAM 16X4
3
A 0 15
G1
1EN [READ]
1C2 [WRITE]
54S189
A, 2D
A
54S225
FIFO 16 X 5
CTR
ENS
CT=0
54S225
CT<15
+
1
C1
G2/Z3
2 CT<16
CT>0
–
Z4
4
1D
5
54S194
SRG4
R
1
0
M 0 3
C4
1->/2<-
54S194
2, 4D
3, 4D
3, 4D
3, 4D
3, 4D
1, 4D


54S240
(SIZE)
EN
54S240
54S241
(SIZE)
EN
54S241
54S244
(SIZE)
EN
54S244
54S251
(SIZE)
MUX
EN
G
54S251
54S253
(SIZE)
MUX
54S253
EN
54S257
(SIZE)
MUX
EN
G1
54S257
54S258
(SIZE)
MUX
EN
G1
54S258
54S260
(SIZE)
≥1
54S260
54S280
2K
54S280
54S283
Σ
P
Q
CI
CO
54S283


SRG8
R
&
3EN13
M
C4/1→/2←
54S299
2, 4D
3, 4D
12, 13
Z12
11, 13
Z11
5, 13
Z5
1, 4D
54S299
EN
C1
54S374
1D
54S374
(SIZE)
ALU
(1/2/3)CP
(1/2/3)CG
(1/2)BI
3 CI
54S381
P
Q
[8]
[4]
[2]
[1]
54S373
54S373
(SIZE)
PROM 256X8
54S471
A
0
255
EN



The 54ASTTL and ANSI 54ASTTL Libraries

The 54ASTTL Library requires approximately 2019 Kbytes of disk storage, and the ANSI 54ASTTL Library requires approximately 2043 Kbytes of disk storage. The physical, timing, and simulation models for each library are identical and differ only in their body drawings. The part name for a component in either library is the same; the body drawing used is determined by the first library name encountered in the library search path (*54asttl.lib* or *a54asttl.lib*).

The specifications used to construct the models in these libraries were taken from the Texas Instruments data books.

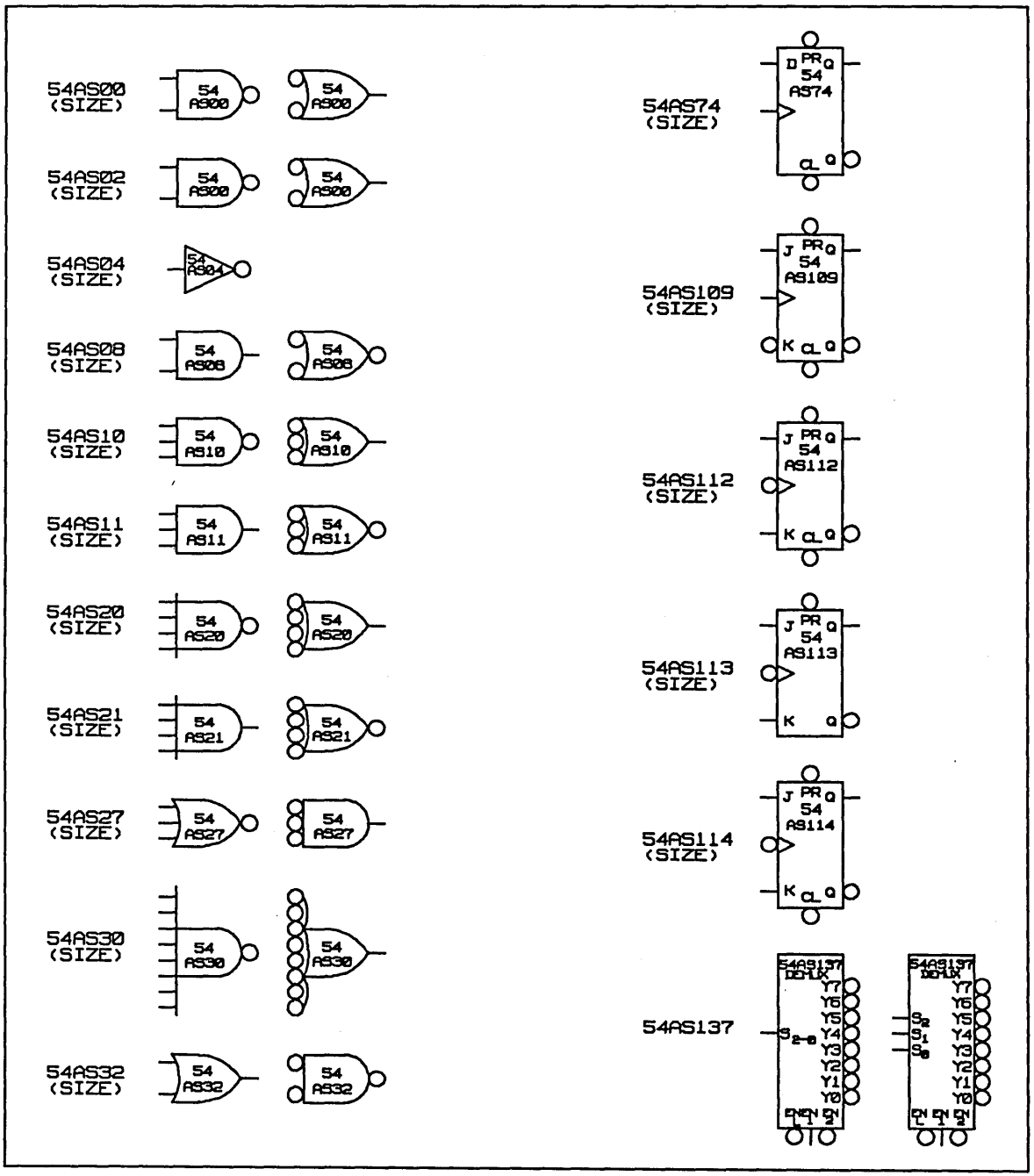
The release level of the 54ASTTL and ANSI 54ASTTL Libraries is 9.0.

Each library contains body drawings and physical, timing, and simulation models for the following 59 components:

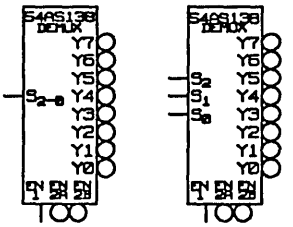
54AS00	Quad 2-input NAND
54AS02	Quad 2-input NOR
54AS04	Hex inverter
54AS08	Quad 2-input AND
54AS10	Triple 3-input NAND
54AS11	Triple 3-input AND
54AS20	Dual 4-input NAND
54AS21	Dual 4-input AND
54AS27	Triple 3-input NOR
54AS30	8-input NAND
54AS32	Quad 2-input OR
54AS74	Dual positive-edge-triggered D flip-flop
54AS109	Dual JKbar positive-edge-triggered flip-flop with clear and preset
54AS112	Dual JK negative-edge-triggered flip-flop with clear and preset
54AS113	Dual JK negative-edge-triggered flip-flop with preset
54AS114	Dual JK negative-edge-triggered flip-flop with preset common clear and clock
54AS137	3-to-8 line decoders/multiplexer with address latch
54AS138	3-to-8 line decoders/multiplexer
54AS139	Dual 2-to-4 line decoders/multiplexer
54AS151	1 of 8 data selectors/multiplexer

54AS153	Dual 1 of 4 data selectors/multiplexer
54AS157	Quad 1 of 2 data selector/multiplexer
54AS158	Quad 1 of 2 data selector/multiplexer
54AS161	4-bit synchronous binary counters with direct clear
54AS163	Synchronous 4-bit binary counter
54AS169	4-bit synchronous binary up/down counter
54AS174	Hex D-type flip-flops with clear
54AS175	Quad D-type flip-flops with clear
54AS181	Arithmetic logic unit/function generator
54AS182	Look-ahead carry generator
54AS195	4-bit bidirectional shift registers
54AS240	Octal buffer and line driver with 3-state output
54AS241	Octal buffer and line driver with 3-state output
54AS243	Quad noninverted 3-state bus transceiver
54AS244	Octal buffer and line driver with 3-state output
54AS251	1 of 8 3-state data selectors/multiplexer
54AS253	Dual 1 of 4 data selector/multiplexer with 3-state output
54AS257	Quad 1 of 2 data selector/multiplexer with 3-state output
54AS258	Quad 1 of 2 data selector/multiplexer with 3-state output
54AS373	Octal D-type 3-state transparent latch

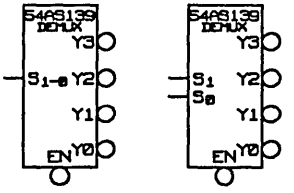
54AS374	Octal D-type edge-triggered flip-flop
54AS533	Octal D-type 3-state transparent latch
54AS534	Octal D-type edge-triggered flip-flop with 3-state output
54AS573	Octal D-type 3-state transparent latch
54AS574	Octal D-type edge-triggered flip-flop with 3-state output
54AS580	Octal D-type 3-state transparent latch
54AS623	Octal bus transceivers
54AS645	Octal bus transceivers
54AS648	Octal bus transceivers and registers
54AS821	10-bit bus interface flip-flops with 3-state outputs
54AS823	9-bit bus interface flip-flops with 3-state outputs
54AS843	9-bit bus interface D-type latches with 3-state outputs
54AS867	Synchronous 8-bit up/down counter
54AS869	Synchronous 8-bit up/down counter
54AS873	Dual 4-bit D-type latches with 3-state outputs
54AS877	8-bit universal transceiver port controllers
54AS881	Arithmetic logic/unit function generator
54AS882	32-bit look-ahead carry generator
54AS1034	Hex drivers


54AS00 (SIZE)
54AS02 (SIZE)
54AS04 (SIZE)
54AS08 (SIZE)
54AS10 (SIZE)
54AS11 (SIZE)
54AS20 (SIZE)
54AS21 (SIZE)
54AS27 (SIZE)
54AS30 (SIZE)
54AS32 (SIZE)
54AS74 (SIZE)
54AS109 (SIZE)
54AS112 (SIZE)
54AS113 (SIZE)
54AS114 (SIZE)
54AS137

54AS138



54AS139



54AS151
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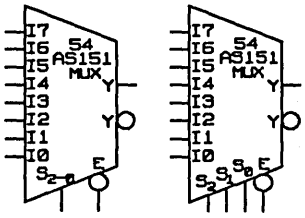
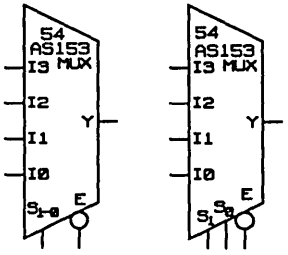


54AS153
(SIZE)



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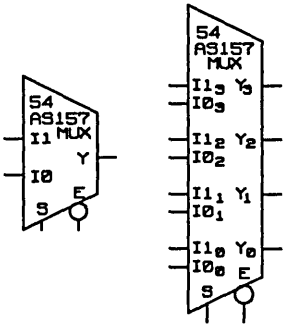

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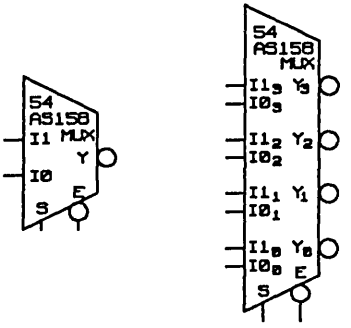
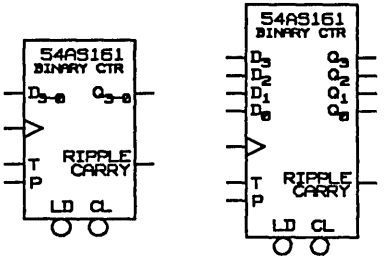
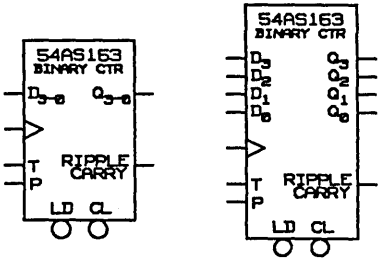


54AS161



54AS163



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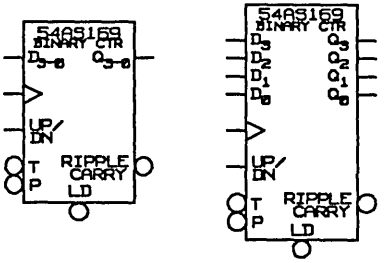

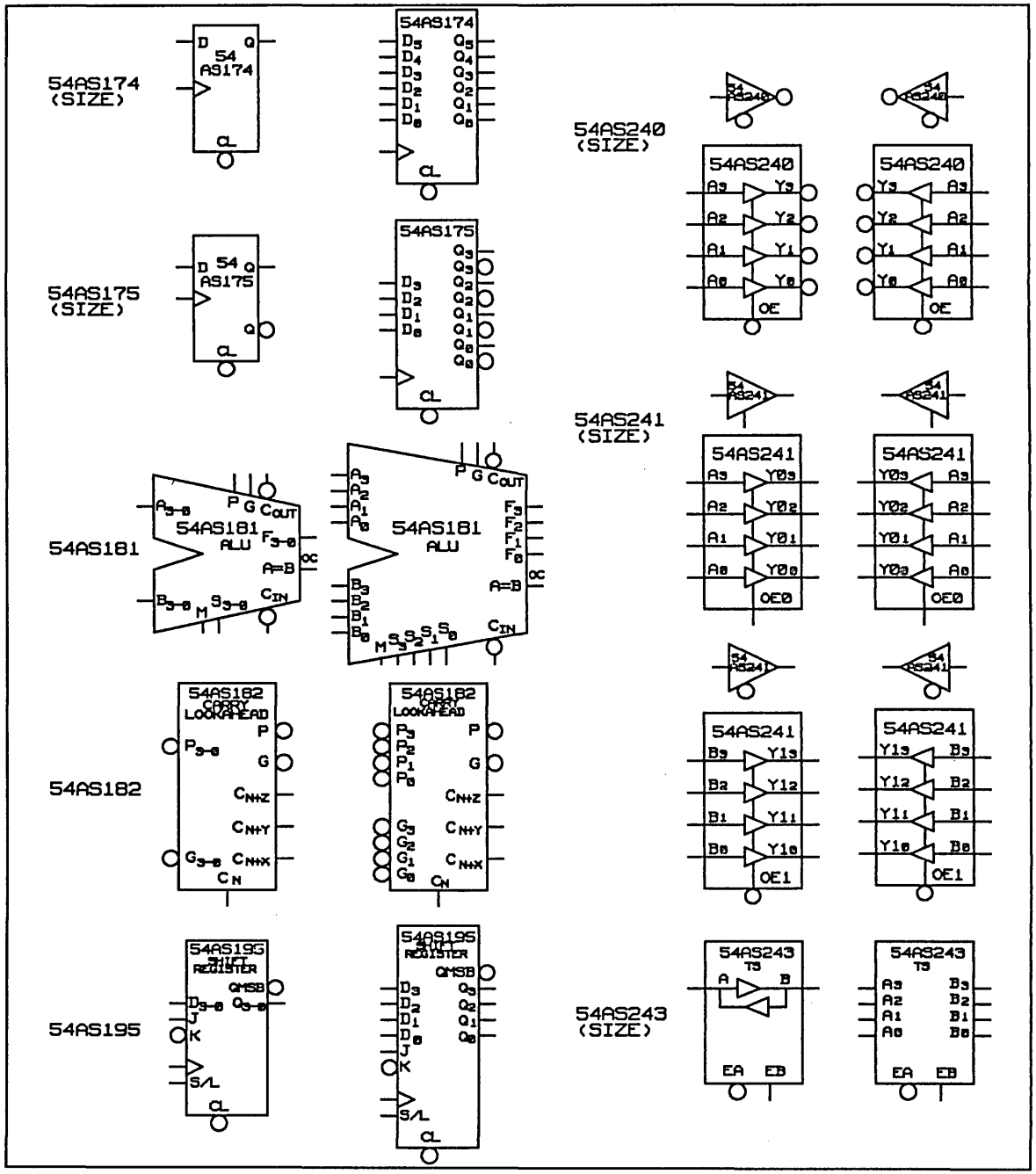
54AS174
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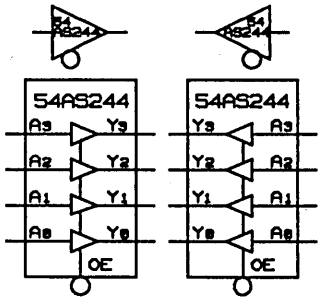
54AS174
54AS175
(SIZE)
54AS175
54AS181
54AS181
ALU
54AS182
54AS182
CARRY
LOOKAHEAD
54AS195
54AS195
4BIT
REGISTER
54AS240
(SIZE)
54AS240
54AS241
(SIZE)
54AS241
54AS243
(SIZE)
54AS243
T3

54AS244
(SIZE)



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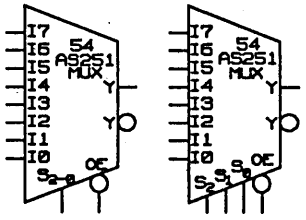

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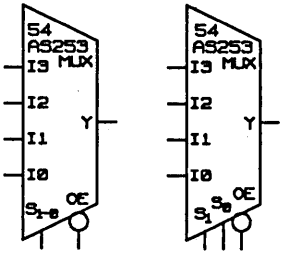

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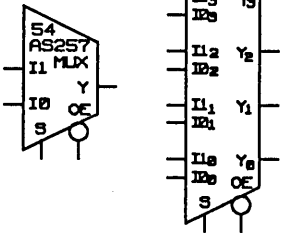

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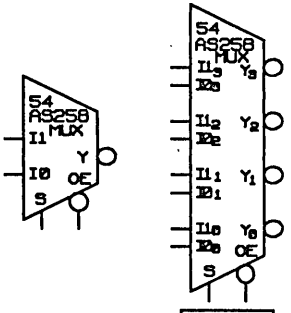

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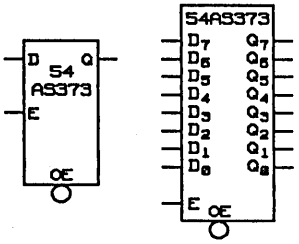

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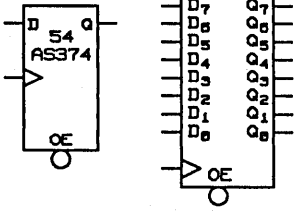

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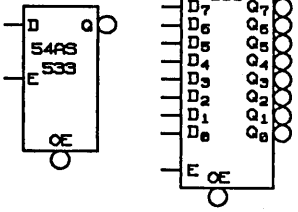

54AS534
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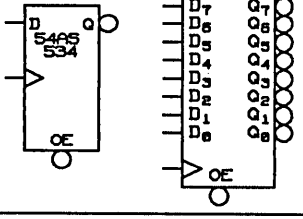
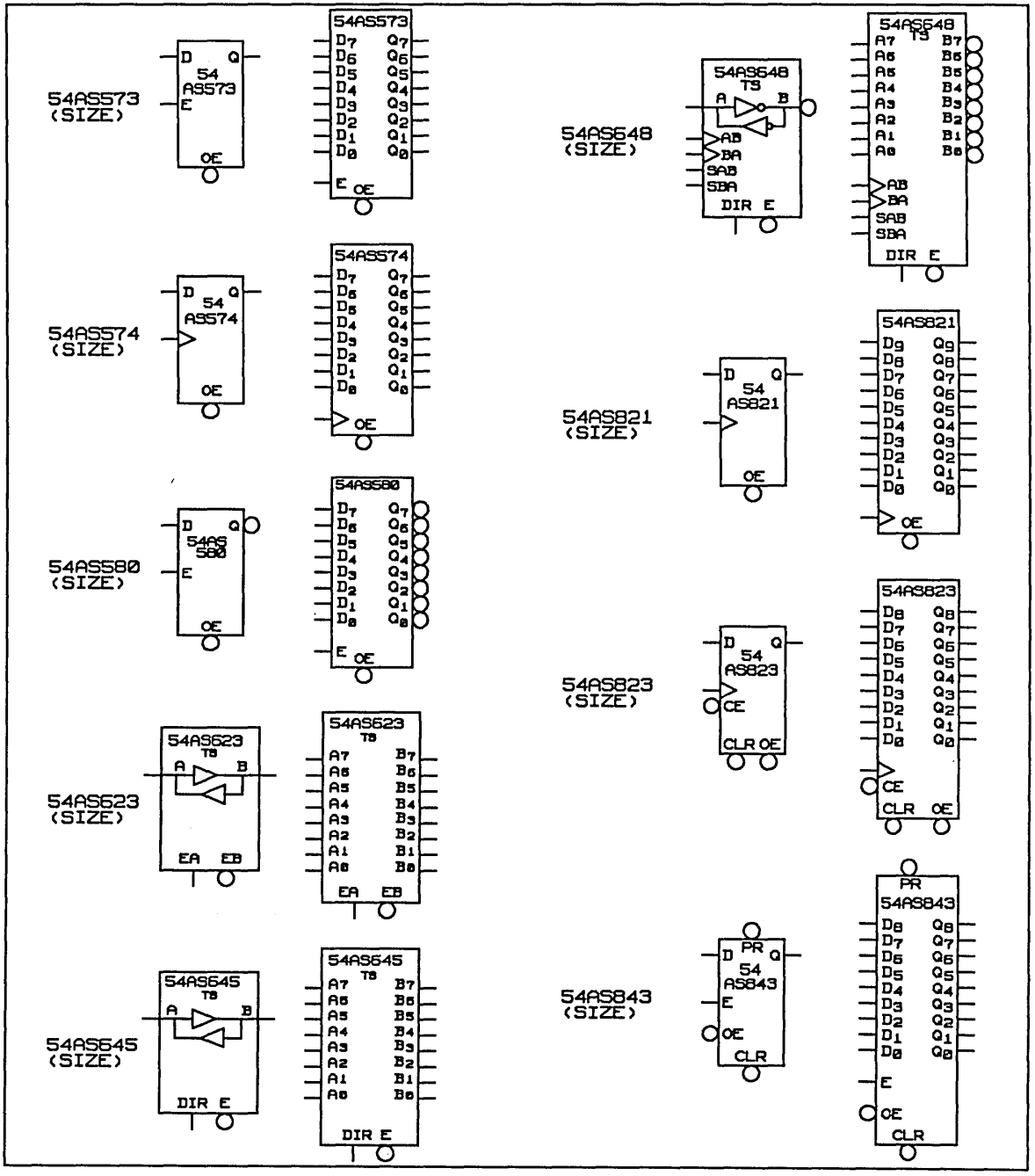
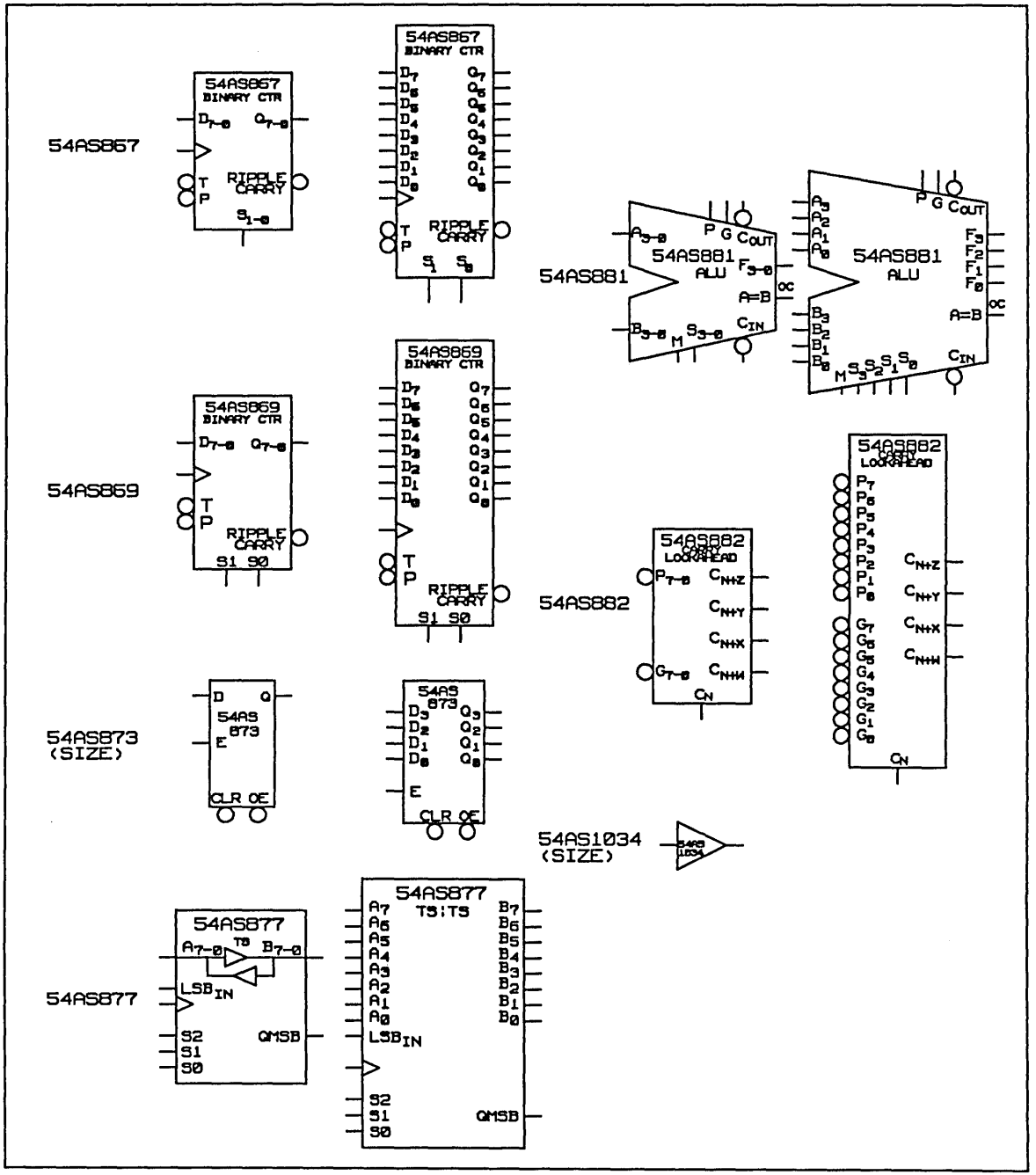
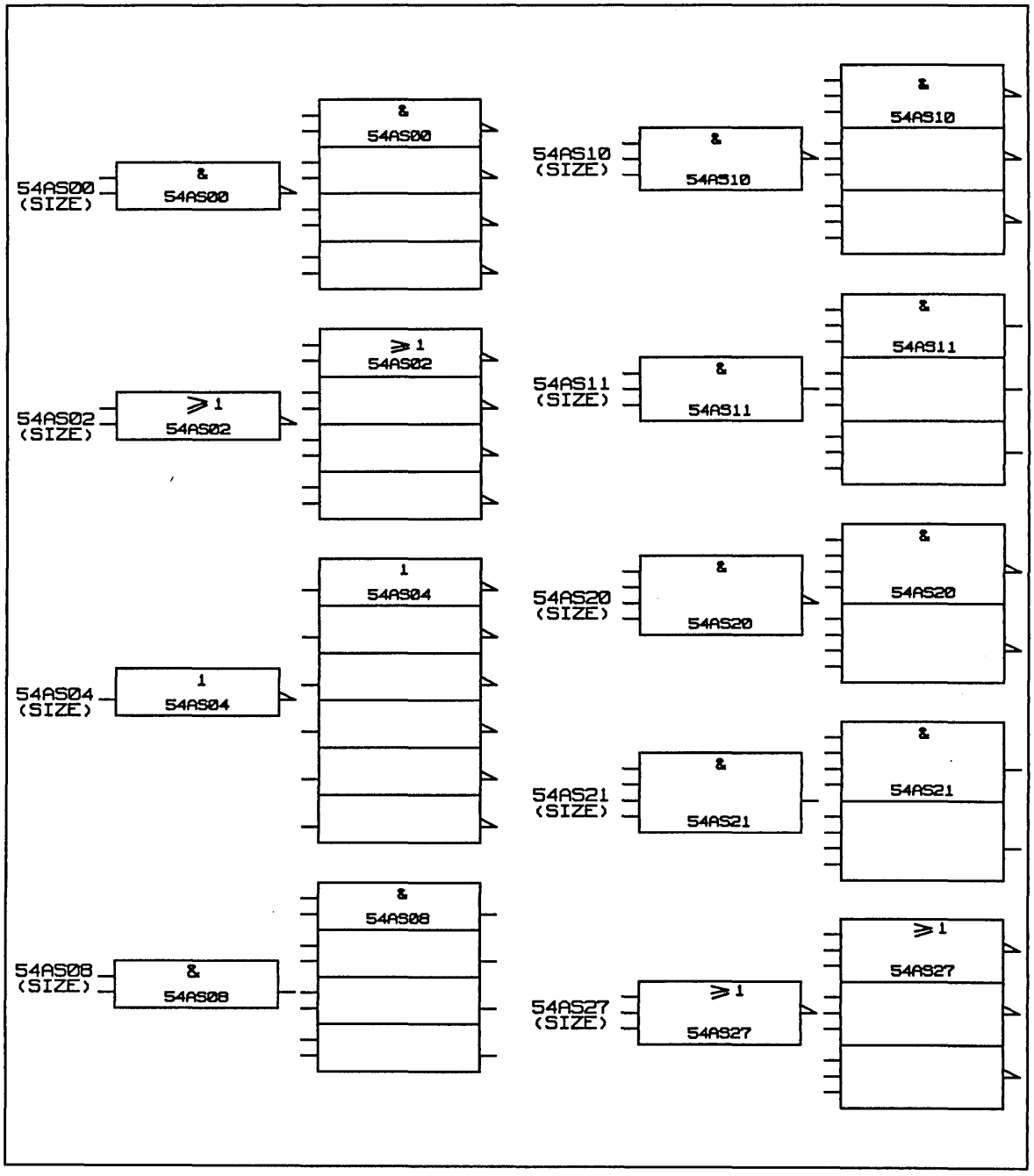
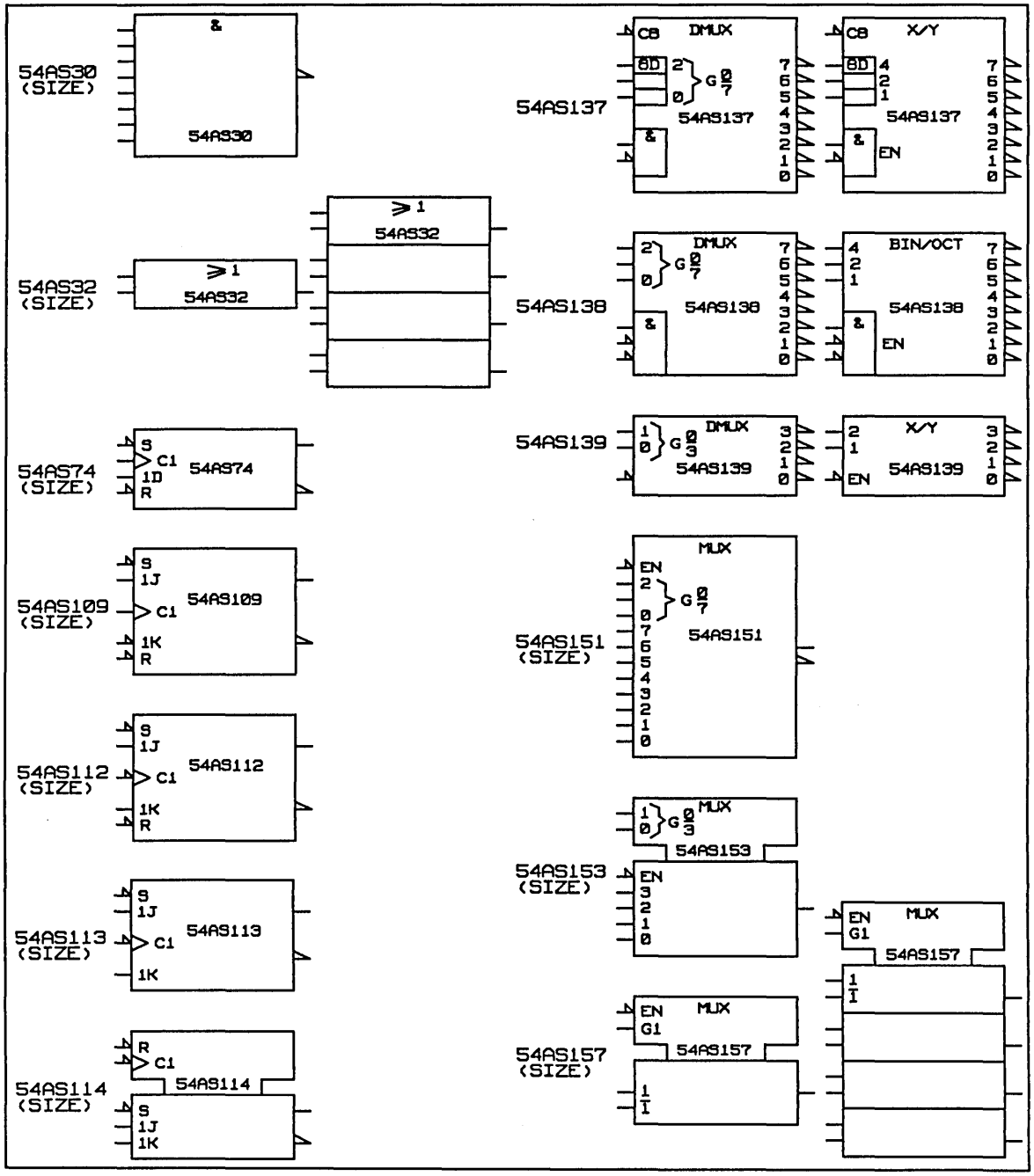
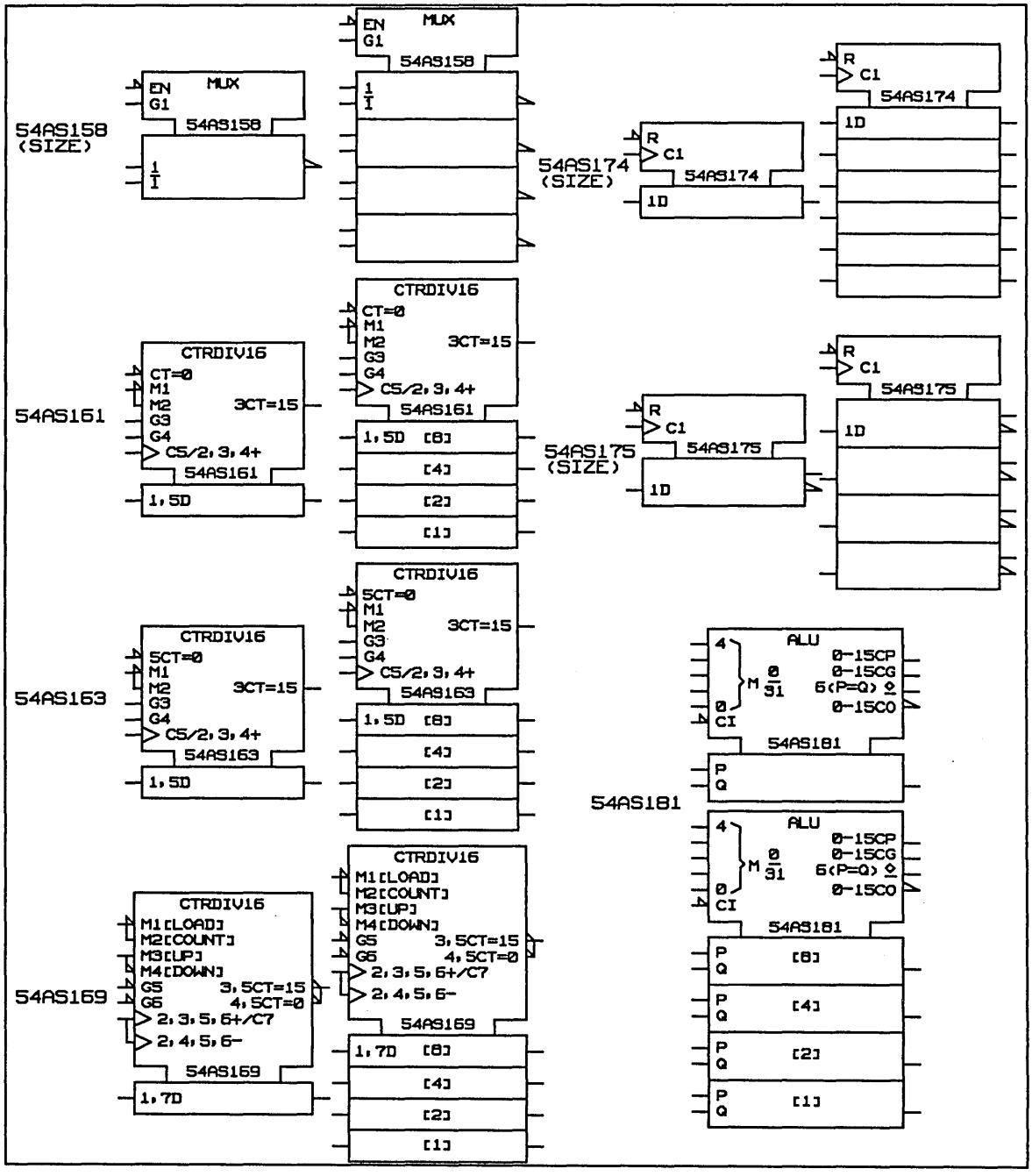


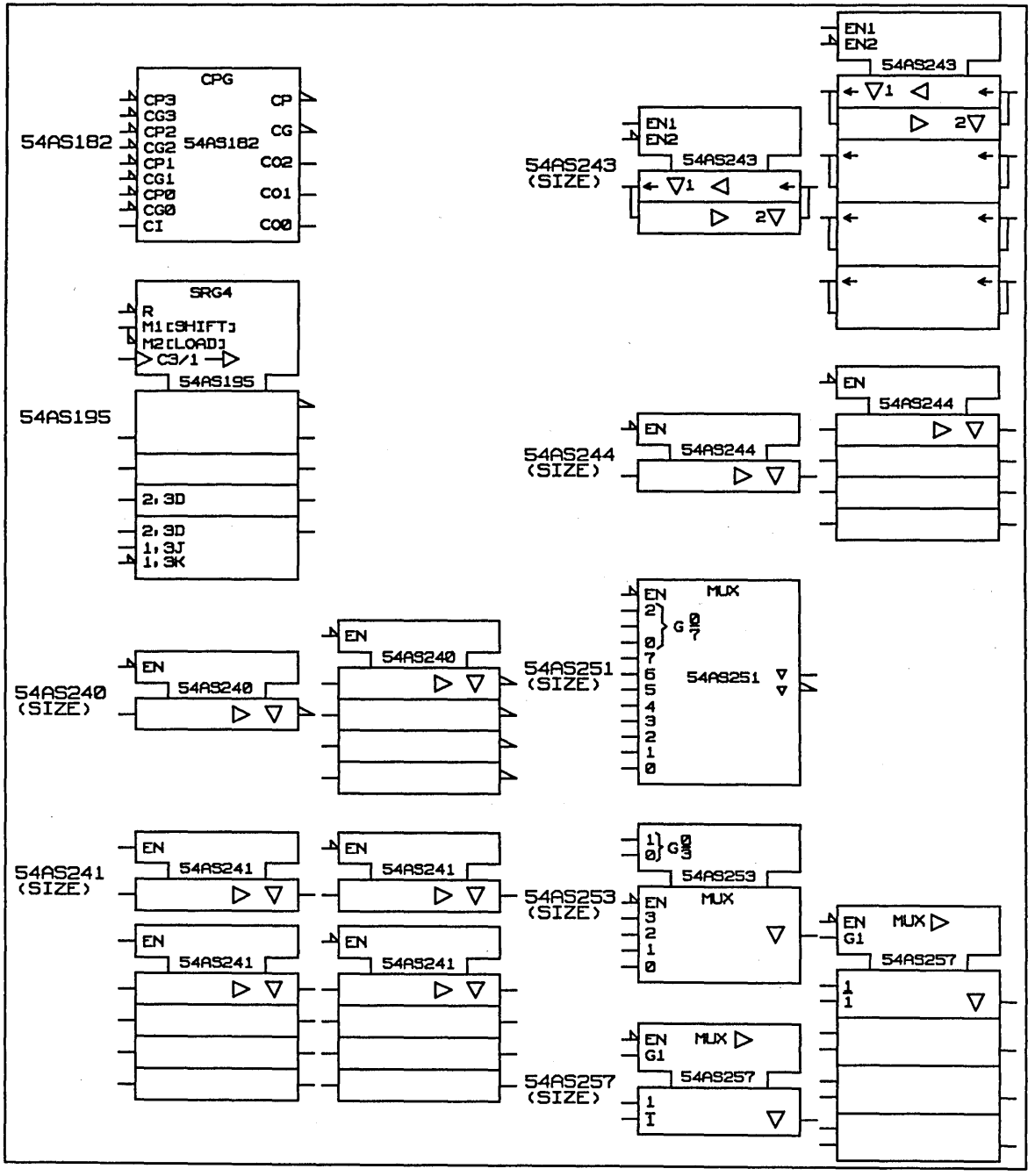

54AS573
(SIZE)
54AS573
54AS574
(SIZE)
54AS574
54AS580
(SIZE)
54AS580
54AS623
(SIZE)
54AS623
54AS645
(SIZE)
54AS645
54AS648
(SIZE)
54AS648
54AS821
(SIZE)
54AS821
54AS823
(SIZE)
54AS823
54AS843
(SIZE)
54AS843

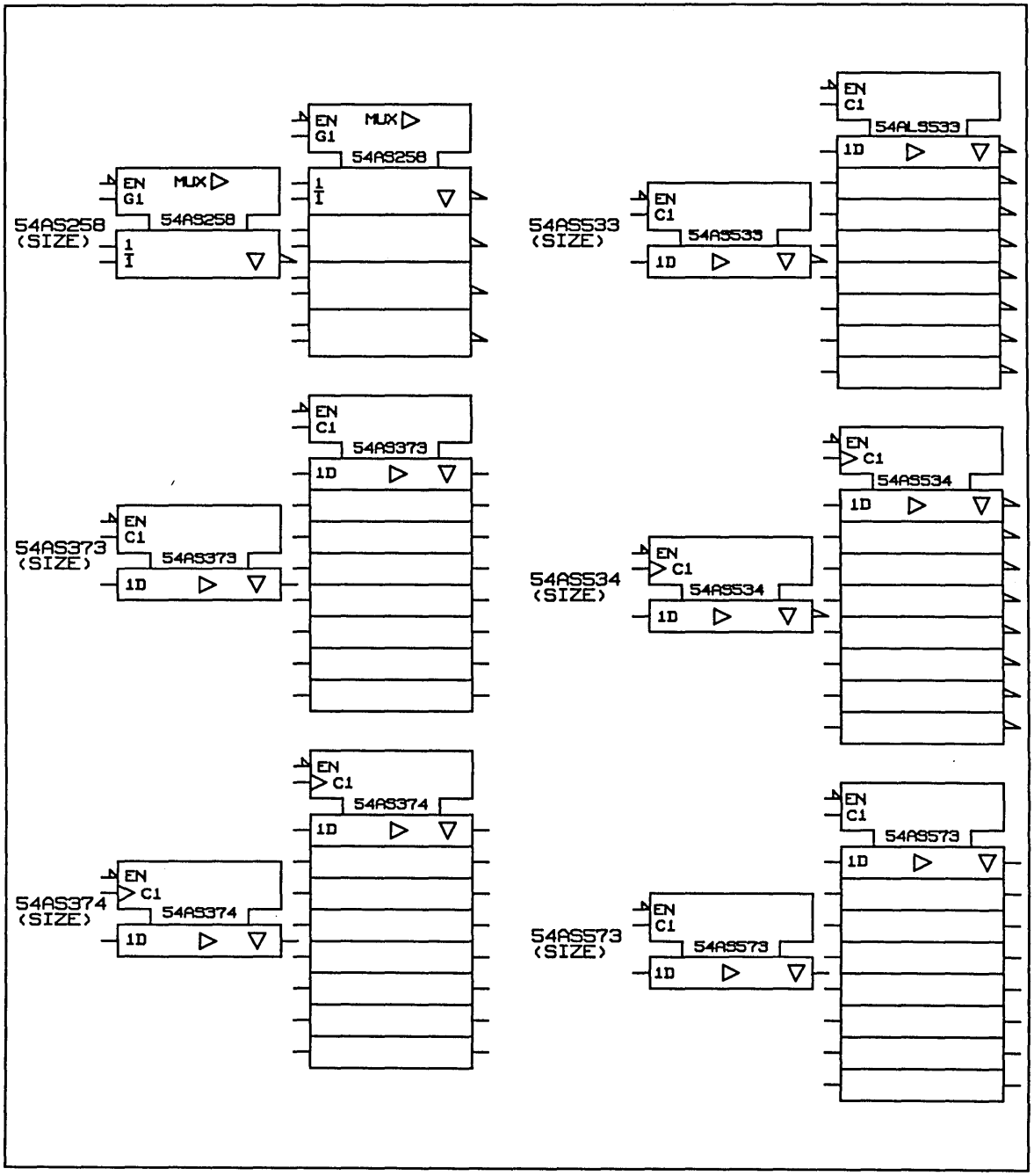

54AS867
54AS867
BINARY CTR
RIPPLE CARRY
54AS869
54AS869
BINARY CTR
RIPPLE CARRY
54AS881
54AS881
ALU
54AS882
54AS882
CARRY LOOKAHEAD
54AS873
(SIZE)
54AS873
54AS1034
(SIZE)
54AS877
54AS877
T:T

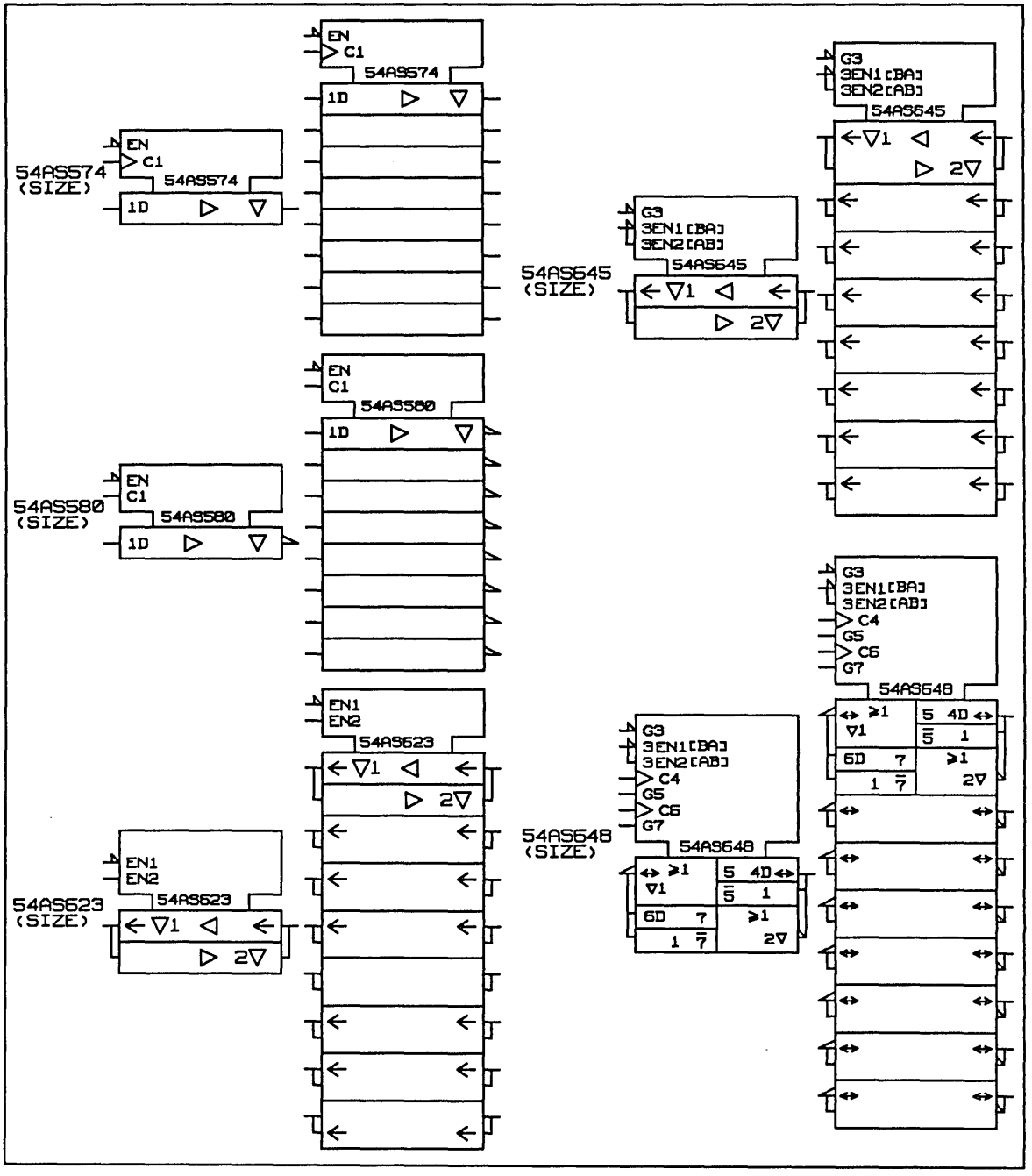

54AS00
(SIZE)
&
54AS00
54AS02
(SIZE)
≥1
54AS02
54AS04
(SIZE)
1
54AS04
54AS08
(SIZE)
&
54AS08
54AS10
(SIZE)
&
54AS10
54AS11
(SIZE)
&
54AS11
54AS20
(SIZE)
&
54AS20
54AS21
(SIZE)
&
54AS21
54AS27
(SIZE)
≥1
54AS27

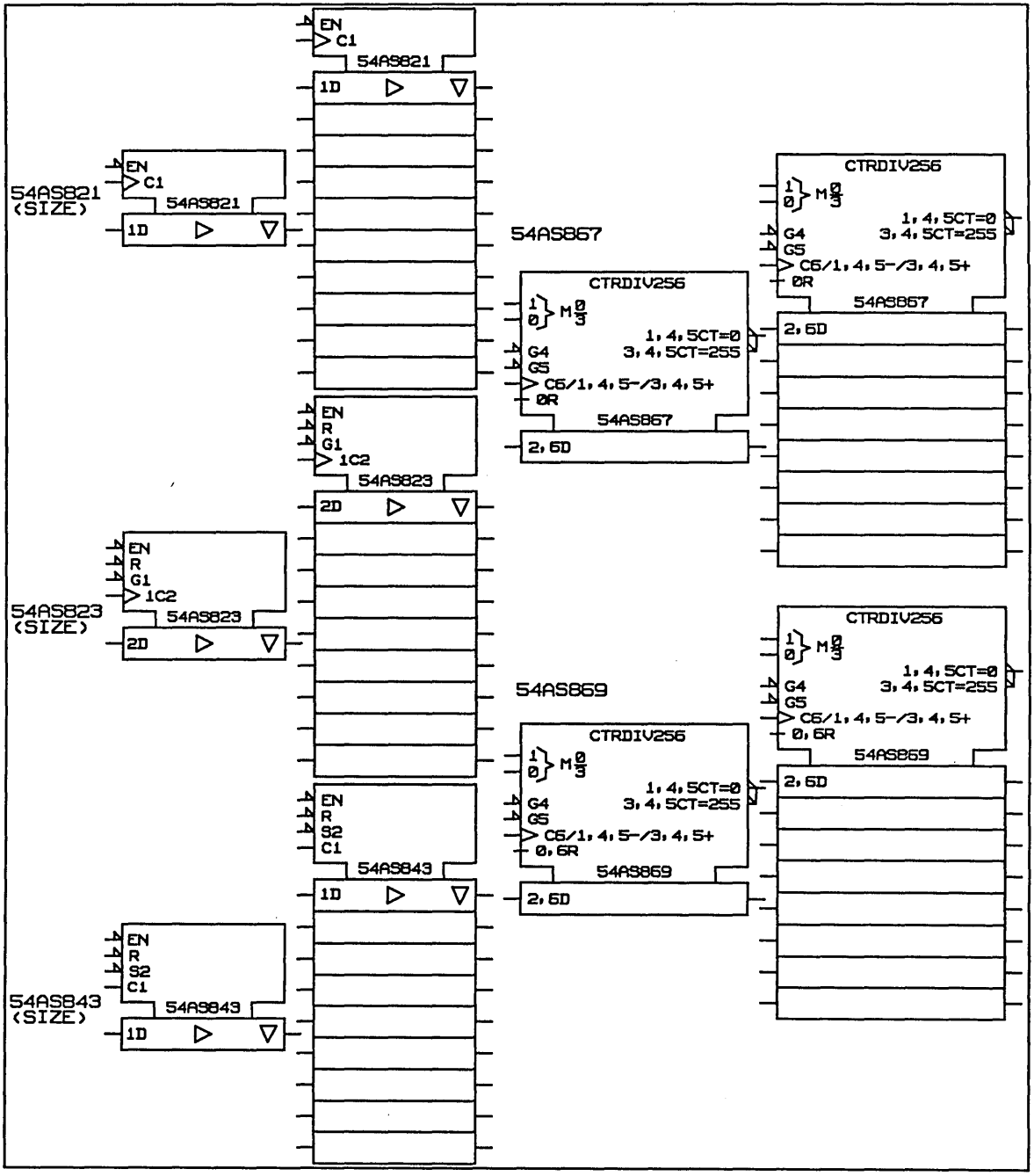

54AS30
(SIZE)
&
54AS30
54AS32
(SIZE)
≥1
54AS32
54AS74
(SIZE)
S
C1
1D
R
54AS74
54AS109
(SIZE)
S
1J
C1
1K
R
54AS109
54AS112
(SIZE)
S
1J
C1
1K
R
54AS112
54AS113
(SIZE)
S
1J
C1
1K
54AS113
54AS114
(SIZE)
R
C1
54AS114
S
1J
1K
54AS137
CB
DMUX
6D
2
0
G Ø 7
54AS137
&
7 6 5 4 3 2 1 0
CB
X/Y
6D
4
2
1
54AS137
&
EN
7 6 5 4 3 2 1 0
54AS138
2
0
G Ø 7
DMUX
54AS138
&
7 6 5 4 3 2 1 0
4
2
1
BIN/OCT
54AS138
&
EN
7 6 5 4 3 2 1 0
54AS139
1
0
G Ø 3
DMUX
54AS139
3 2 1 0
2
1
X/Y
54AS139
EN
3 2 1 0
54AS151
(SIZE)
MUX
EN
2
G Ø 7
0 7 6 5 4 3 2 1 0
54AS151
54AS153
(SIZE)
1
0
G Ø 3
MUX
54AS153
EN
3 2 1 0
EN
G1
MUX
54AS157
1
I
54AS157
(SIZE)
EN
G1
MUX
54AS157
1
I

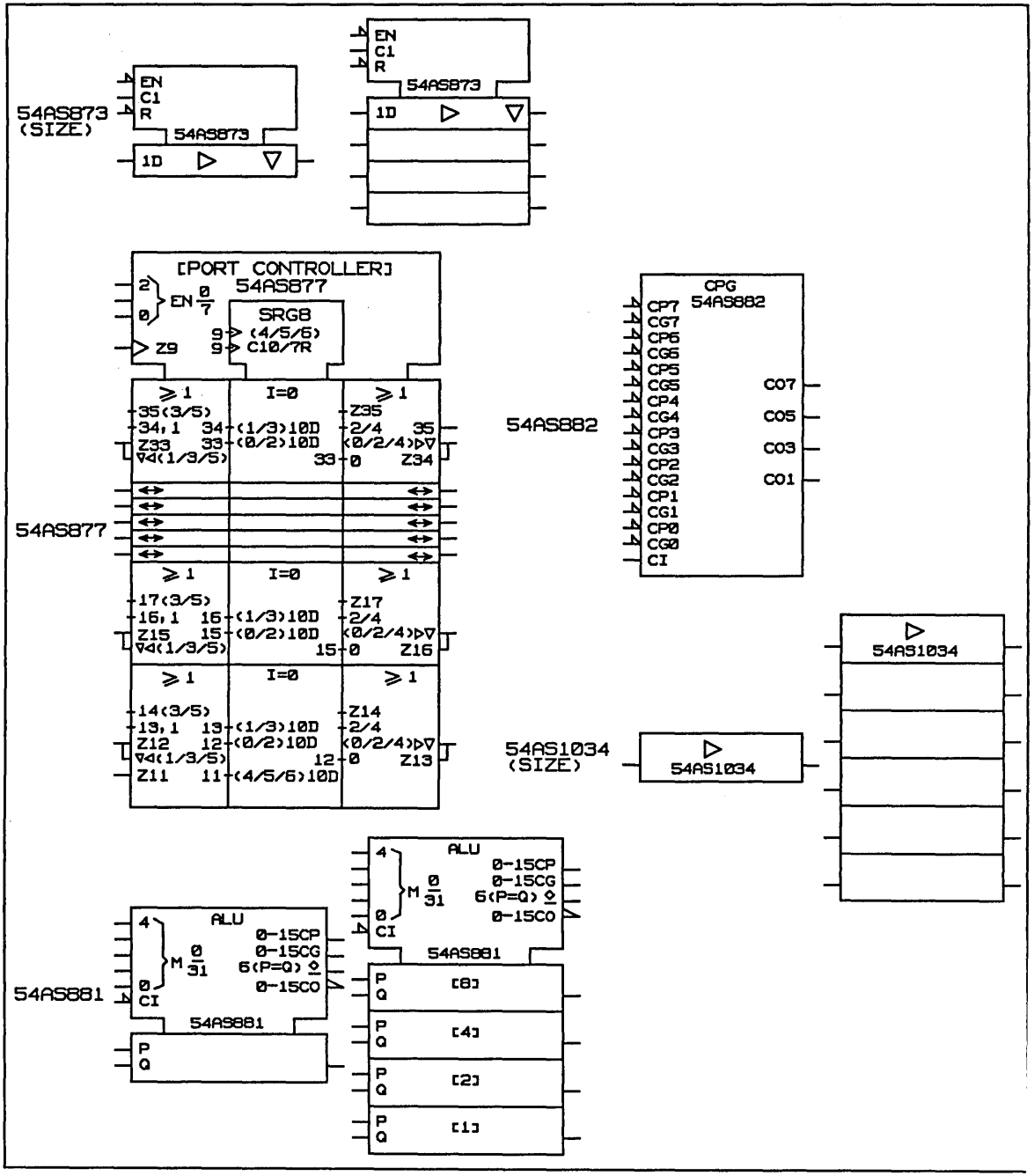

54AS158
(SIZE)
MUX
EN
G1
54AS158
1
1
54AS174
(SIZE)
R
C1
54AS174
1D
54AS161
CTRDIV16
CT=0
M1
M2
G3
G4
C5/2,3,4+
3CT=15
54AS161
1,5D
[8]
[4]
[2]
[1]
54AS175
(SIZE)
54AS175
54AS163
54AS163
54AS181
ALU
4
M
0
31
0
CI
0-15CP
0-15CG
6(P=Q)
0-15CO
P
Q
54AS169
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5
G6
3,5CT=15
4,5CT=0
2,3,5,6+/C7
2,4,5,6-
1,7D

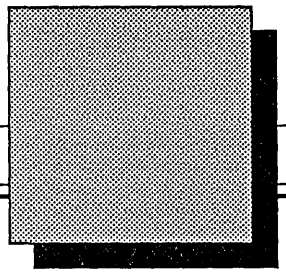

54AS182
CPG
CP3
CG3
CP2
CG2
CP1
CG1
CP0
CG0
CI
54AS182
CP
CG
CO2
CO1
CO0
54AS195
SRG4
R
M1[SHIFT]
M2[LOAD]
C3/1
54AS195
2,3D
2,3D
1,3J
1,3K
54AS240
(SIZE)
EN
54AS240
54AS241
(SIZE)
EN
54AS241
54AS243
(SIZE)
EN1
EN2
54AS243
1
2
54AS244
(SIZE)
EN
54AS244
54AS251
(SIZE)
MUX
G
54AS251
54AS253
(SIZE)
54AS253
MUX
54AS257
(SIZE)
54AS257
MUX
G1


EN
G1
MUX
54AS258
1
I
54AS258
(SIZE)
EN
C1
54ALS533
1D
54AS533
(SIZE)
54AS373
54AS534
54AS374
54AS573


EN
C1
54AS574
1D
54AS574
(SIZE)
EN1
EN2
54AS623
2∇
54AS623
(SIZE)
54AS580
54AS580
(SIZE)
G3
3EN1[BA]
3EN2[AB]
54AS645
54AS645
(SIZE)
C4
G5
C6
G7
54AS648
54AS648
(SIZE)


EN
C1
54AS821
1D
54AS821
(SIZE)
54AS823
(SIZE)
54AS843
(SIZE)
R
G1
1C2
S2
2D
54AS867
CTRDIV256
M 0 3
1, 4, 5CT=0
3, 4, 5CT=255
G4
G5
C6/1, 4, 5-/3, 4, 5+
0R
2, 6D
54AS869
0, 6R


54AS873
(SIZE)
EN
C1
R
54AS873
1D
[PORT CONTROLLER]
54AS877
SRGB
(4/5/6)
C10/7R
54AS877
I=0
54AS882
CPG
54AS882
CP7
CG7
CP6
CG6
CP5
CG5
CP4
CG4
CP3
CG3
CP2
CG2
CP1
CG1
CP0
CG0
CI
CO7
CO5
CO3
CO1
54AS1034
(SIZE)
54AS1034
ALU
54AS881
0-15CP
0-15CG
0-15CO
[8]
[4]
[2]
[1]
P
Q



The 54ALSTTL and ANSI 54ALSTTL Libraries

The 54ALSTTL Library requires approximately 3363 Kbytes of disk storage, and the ANSI 54ALSTTL Library requires approximately 3423 Kbytes of disk storage. The physical, timing, and simulation models for each library are identical and differ only in their body drawings. The part name for a component in either library is the same; the body drawing used is determined by the first library name encountered in the library search path (*54alsttl.lib* or *a54alsttl.lib*).

The specifications used to construct the models in these libraries were taken from either the Texas Instruments data books or from Mil Spec MIL-M-38510. Parts indicated with an asterisk (*) are from MIL-M-38510; the descriptions for these components include the military device type in parentheses.

The release level of the 54ALSTTL and ANSI 54ALSTTL Libraries is 9.0.

Each library contains body drawings and physical, timing, and simulation models for the following 108 components:

* **54ALS00**	Quad 2-input NAND (37001)
54ALS01	Quad 2-input open-collector NAND
* **54ALS02**	Quad 2-input NOR (37301)
54ALS03	Quad 2-input positive-NAND with open-collector input
* **54ALS04**	Hex inverter (37006)
54ALS05	Hex open-collector inverter
* **54ALS08**	Quad 2-input AND (37401)
54ALS09	Quad 2-input positive-AND with open-collector output
* **54ALS10**	Triple 3-input NAND (37002)
* **54ALS11**	Triple 3-input AND (37402)
54ALS12	Triple 3-input positive-AND with open-collector output
54ALS15	Triple 3-input positive-AND with open-collector output
* **54ALS20**	Dual 4-input NAND (37003)
54ALS21	Dual 4-input AND
54ALS22	Dual 4-input positive-NAND with open-collector output
* **54ALS27**	Triple 3-input NOR (37302)
* **54ALS28**	Quad 2-input positive-NOR buffer (38402)
* **54ALS30**	8-input NAND (37004)
* **54ALS32**	Quad 2-input OR (37501)
54ALS33	Quad 2-input positive-NOR buffer with open-collector output

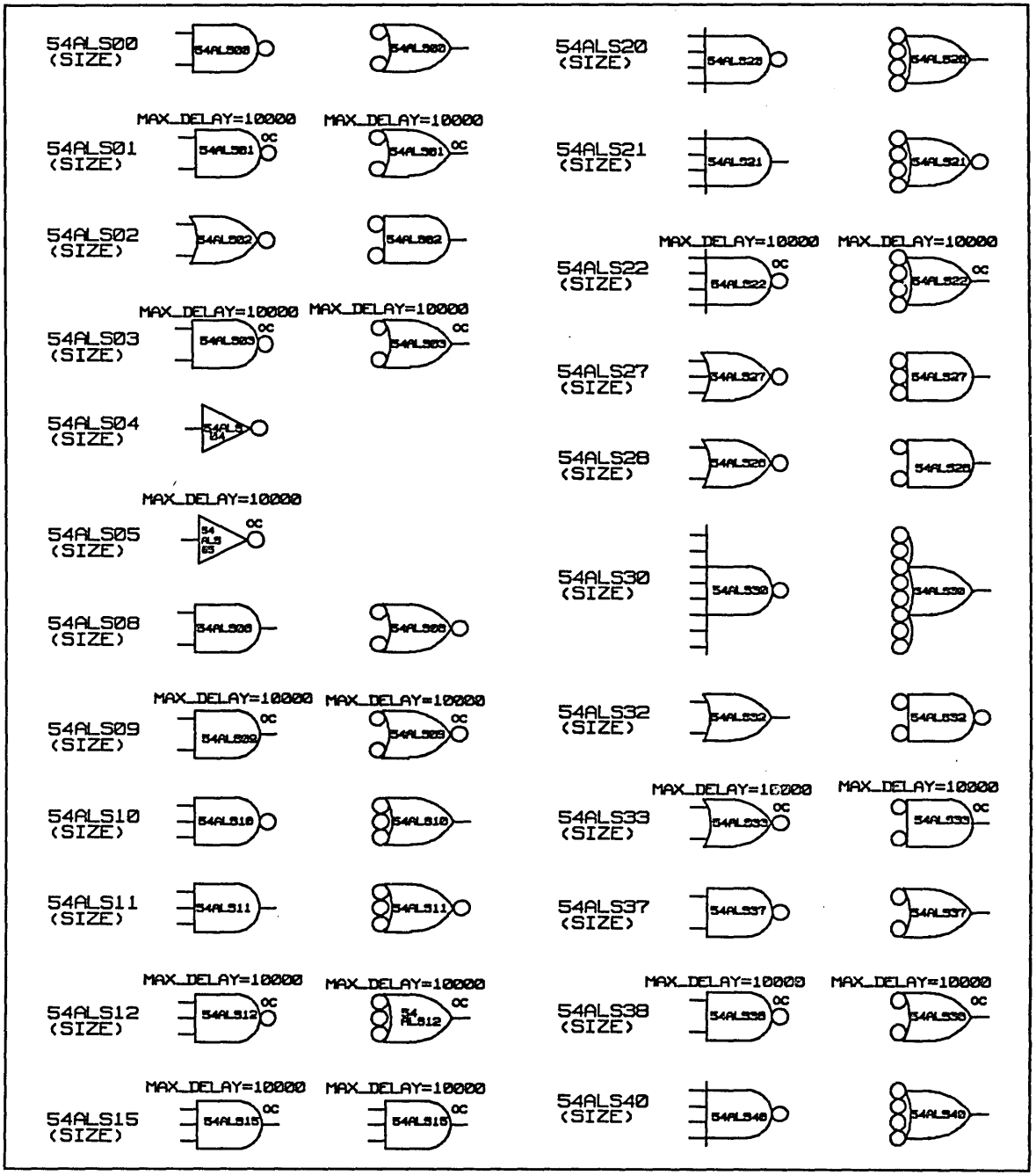
* **54ALS37**	Quad 2-input NAND buffer (38401)
54ALS38	Quad 2-input open-collector NAND buffer
* **54ALS40**	Dual 4-input positive-NAND buffer (38407)
* **54ALS74**	Dual positive-edge-triggered D flip-flop (37101)
54ALS86	Quad 2-input exclusive-OR
* **54ALS109**	Dual JKbar positive-edge-triggered flip-flop (37102)
* **54ALS112**	Dual JK negative-edge-triggered flip-flop with clear and preset (37103)
54ALS113	Dual JK negative-edge-triggered flip-flop with preset
54ALS114	Dual JK negative-edge-triggered flip-flop with preset, common clear, and clock
* **54ALS133**	13-input positive-NAND (37005)
54ALS137	3-to-8 line decoder/multiplexer with address latches
* **54ALS138**	3-to-8 line decoders/multiplexers (37701)
54ALS139	Dual 2-to-4 line decoders/multiplexers
54ALS151	1-of-8 data selectors/multiplexers
54ALS153	Dual 1-of-4 data selector/multiplexer
54ALS157	Quad 1-of-2 data selector/multiplexer
54ALS158	Quad 1-of-2 data selector/multiplexer
* **54ALS160**	4-bit synchronous decade counters with direct clear (38101)
* **54ALS161**	4-bit synchronous binary counters with direct clear (38001)
* **54ALS162**	4-bit synchronous decade counters with synchronous clear (38102)

* **54ALS163**	4-bit synchronous binary counters with synchronous clear (38002)
54ALS164	8-bit parallel output serial shift register
54ALS165	Parallel-load 8-bit shift register
54ALS166	8-bit shift registers
* **54ALS168**	4-bit synchronous decade up/down counters (38103)
* **54ALS169**	4-bit synchronous binary up/down counters (38003)
* **54ALS174**	Hex D-type flip-flops (37201)
* **54ALS175**	Quad D-type flip-flops (37202)
54ALS190	Synchronous BCD up/down counter
54ALS191	Synchronous binary up/down counter
54ALS192	Synchronous binary up/down dual clock counters
54ALS193	Synchronous binary up/down dual clock counters
* **54ALS240**	Octal buffer and line driver with 3-state output (38301)
* **54ALS241**	Octal buffer and line driver with 3-state output (38302)
* **54ALS242**	Quad inverting 3-state bus transceiver (38506)
* **54ALS243**	Quad 3-state bus transceiver (38507)
* **54ALS244**	Octal buffer and line driver with 3-state output (38303)
54ALS245	Octal non-inverting 3-state bus transceiver
54ALS251	3-state data multiplexer
54ALS253	Dual data selectors/multiplexers

54ALS257	Quad 3-state non-inverting data multiplexer
54ALS258	Quad 3-state inverting data multiplexer
54ALS273	Octal D-type flip-flop with clear
* **54ALS299**	8-bit universal shift/storage register with 3-state output (37601)
* **54ALS323**	8-bit universal shift/storage register with 3-state output (37602)
54ALS352	Dual 1 of 4 line inverting data selector/multiplexer
54ALS353	Dual 1 of 4 data selector/multiplexer with 3-state output
54ALS365	Hex non-inverted 3-state bus transceiver
54ALS366	Hex inverted 3-state output bus driver
54ALS367	Hex non-inverted 3-state output bus driver
54ALS368	Hex inverted 3-state output bus driver
* **54ALS373**	Octal 3-state D-latch with common enable (37203)
* **54ALS374**	Octal D-type edge-triggered flip-flop (37204)
54ALS520	8-bit identity comparator
54ALS521	8-bit identity comparator
54ALS533	Octal D-type transparent latches with 3-state output
54ALS534	Octal D-type edge-triggered flip-flop with 3-state output
54ALS538	3-line to 8-line decoder/demultiplexer with 3-state output
54ALS540	Octal buffer and line driver with 3-state output
54ALS541	Octal buffer and line driver with 3-state output

54ALS563	Octal D-type transparent latch with 3-state output
54ALS564	Octal D-type edge-triggered flip-flop with 3-state output
* **54ALS569**	Synchronous 4-bit up/down binary counter with 3-state output (38005)
* **54ALS573**	Octal D-type transparent latch with 3-state output (38201)
* **54ALS574**	Octal D-type edge-triggered flip-flop with 3-state output (37104)
54ALS575	Octal D-type edge-triggered flip-flop with 3-state output
* **54ALS576**	Octal D-type edge-triggered flip-flop with 3-state output (37105)
* **54ALS580**	Octal D-type transparent latch with 3-state output (38202)
54ALS623	Octal 3-state non-inverting bus transceiver
* **54ALS640**	Octal 3-state inverting bus transceiver (38501)
* **54ALS645**	Octal 3-state non-inverting bus transceiver (38505)
54ALS648	Octal bus transceiver and register
54ALS652	Octal bus transceiver and register
54ALS677	Address comparator
54ALS688	8-bit identity comparator
54ALS804	Hex 2-input NAND driver
54ALS805	Hex 2-input NOR driver
54ALS808	Hex 2-input AND driver
* **54ALS857**	Hex 2-to-1 universal multiplexer (37901)
* **54ALS873**	Dual 4-bit D-type 3-state latch (38203)

* **54ALS874**	Dual 4-bit D-type edge-triggered flip-flop (37106)
* **54ALS878**	Dual 4-bit D-type edge-triggered flip-flop with 3-state outputs
* **54ALS1000**	Quad 2-input positive-NAND buffer (38401)
* **54ALS1002**	Quad 2-input NOR buffer (38402)
* **54ALS1004**	Hex inverter (38409)
* **54ALS1005**	Hex 3-state inverter buffer (38410)
* **54ALS1008**	Quad 2-input positive-AND buffer/driver (38404)
* **54ALS1034**	Hex driver (38411)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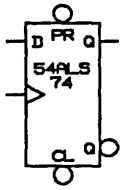

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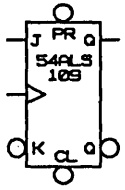

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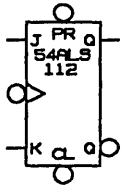

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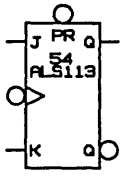

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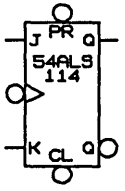

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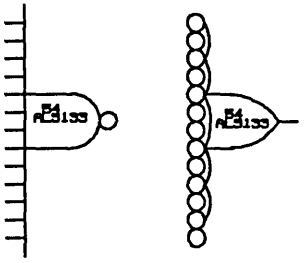

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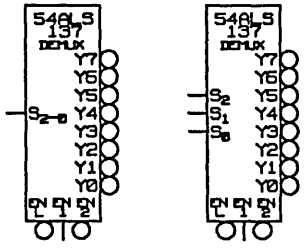

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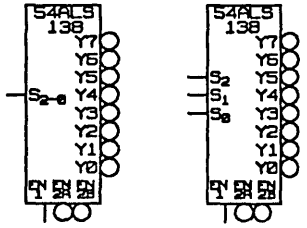

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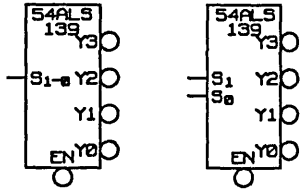

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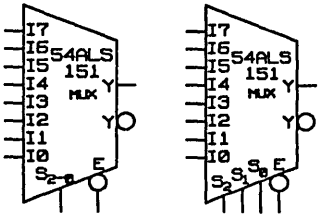

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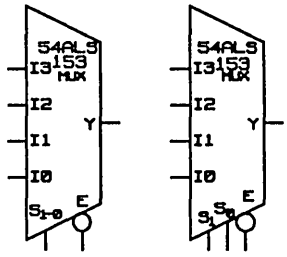

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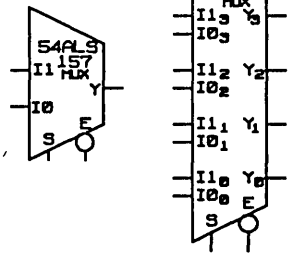

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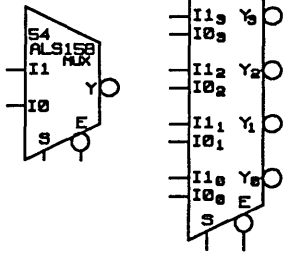

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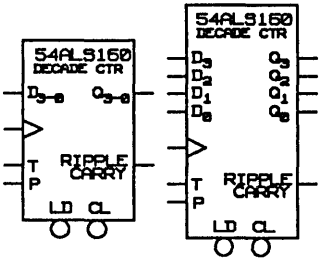

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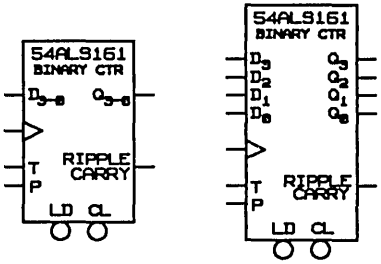

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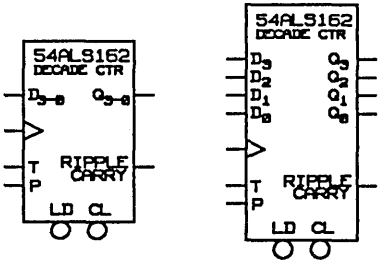

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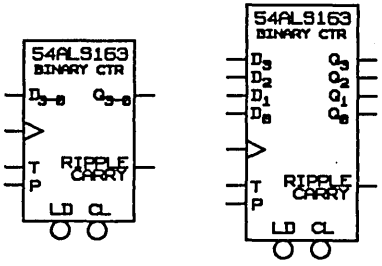

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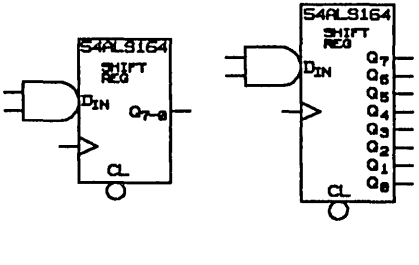

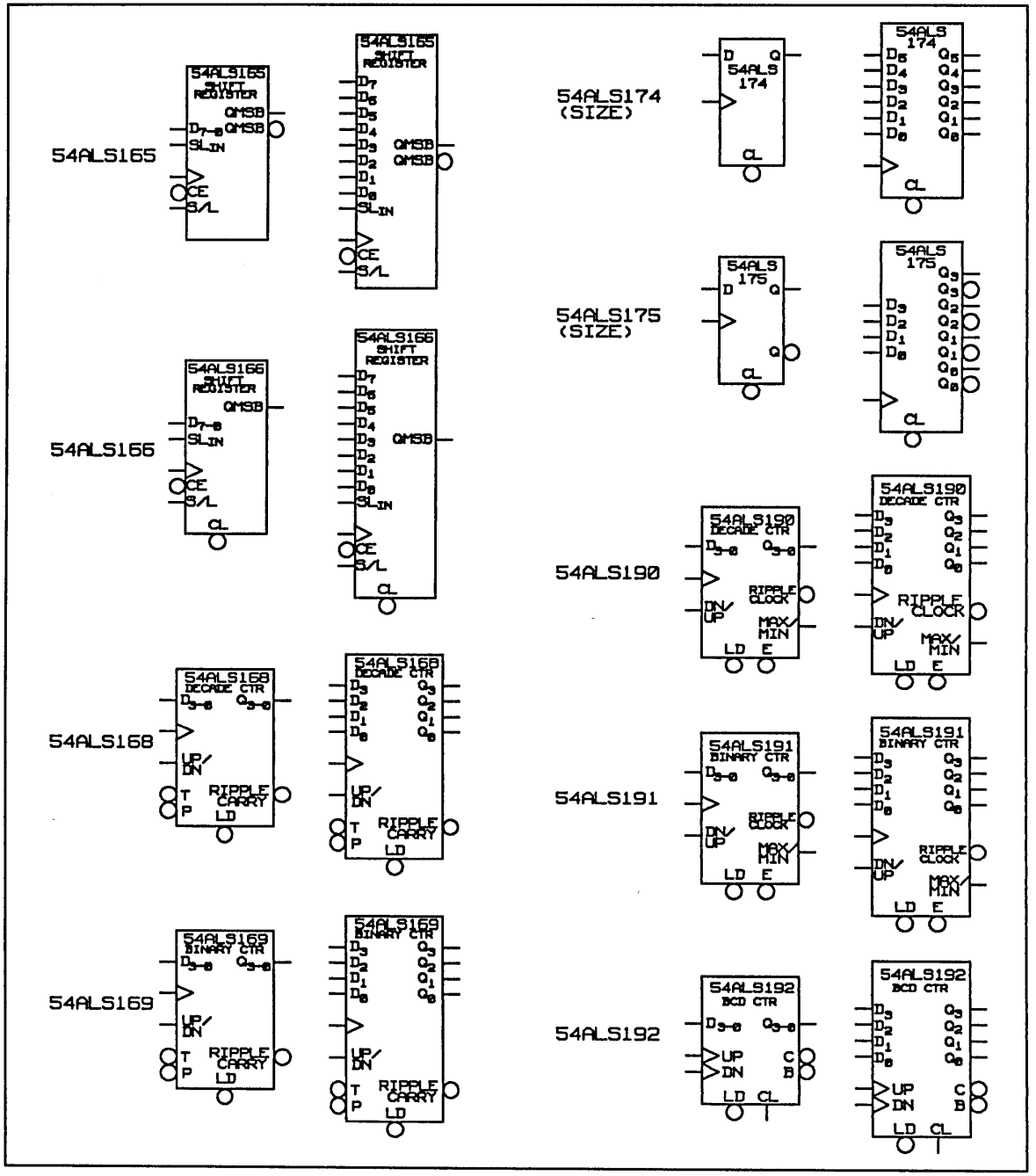
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BINARY CTR
BCD CTR
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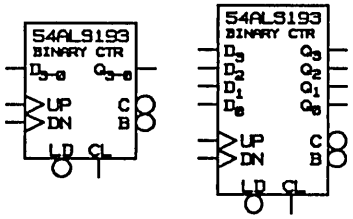

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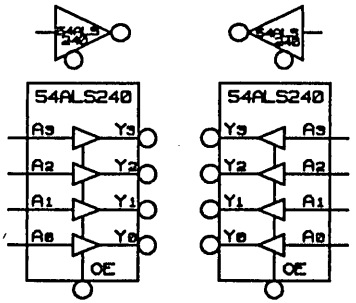

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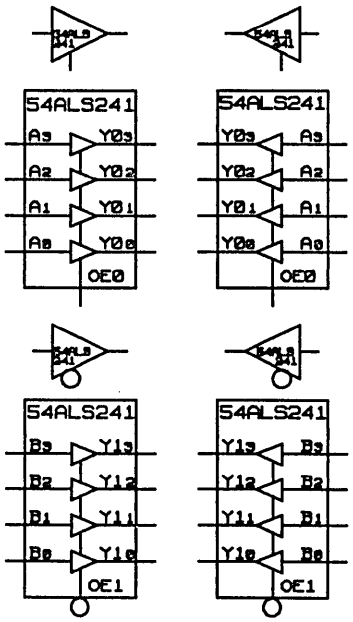

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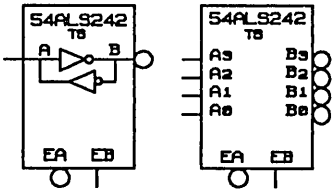

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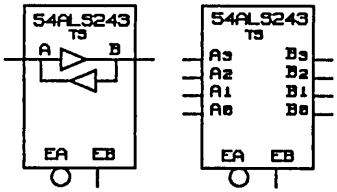

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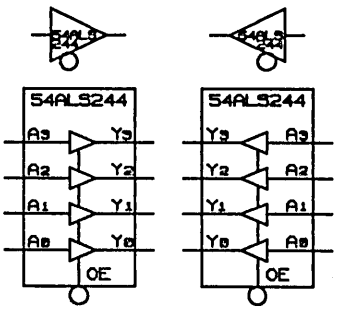

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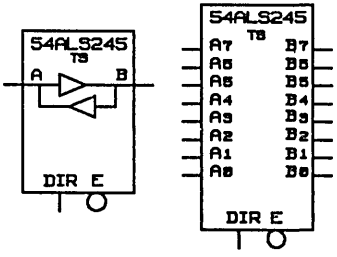

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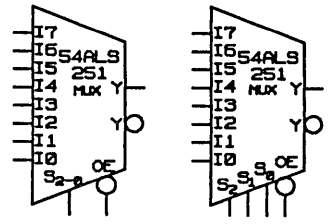

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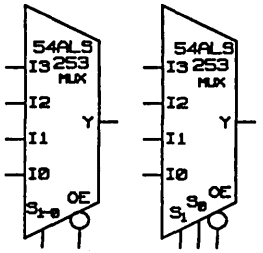

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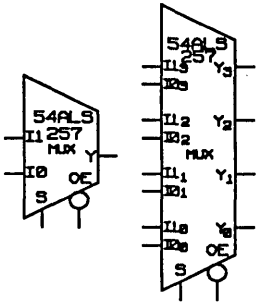

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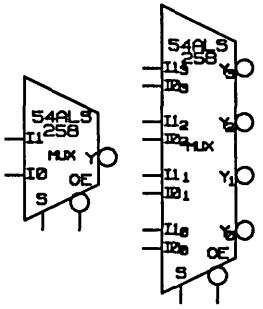

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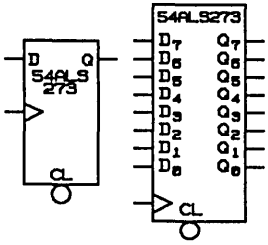

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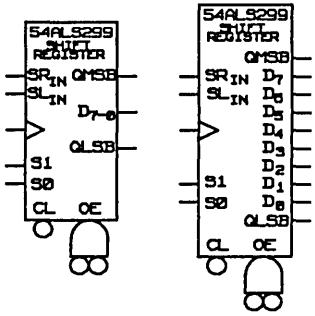

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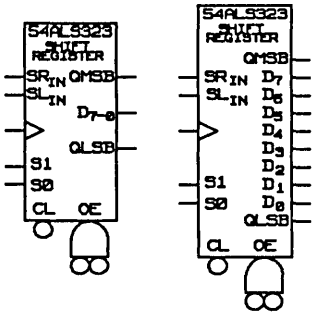

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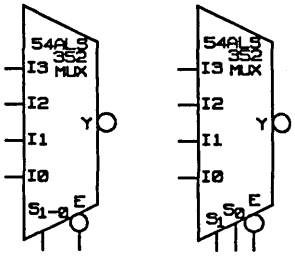

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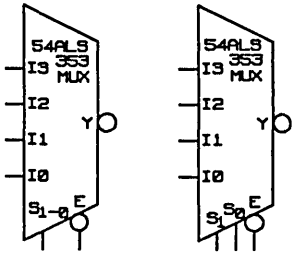

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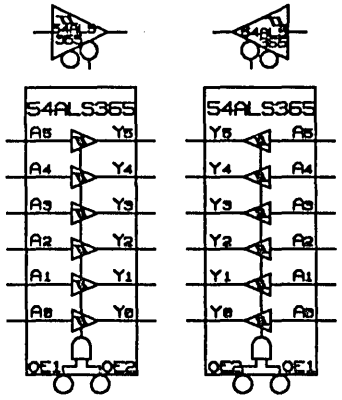

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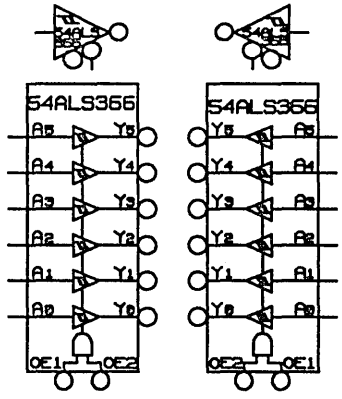

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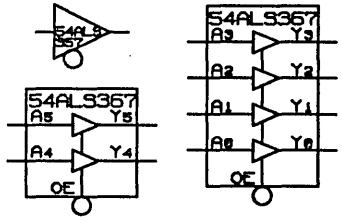

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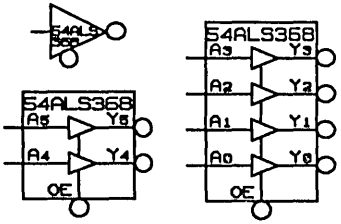

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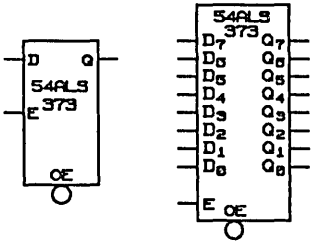

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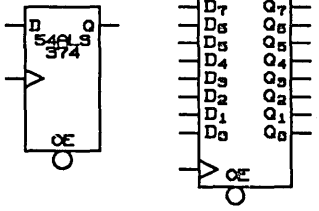

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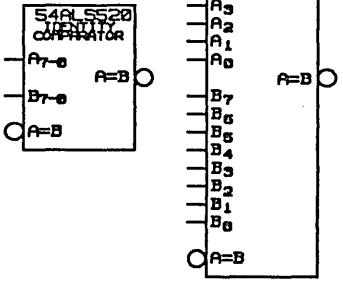

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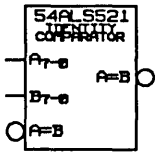

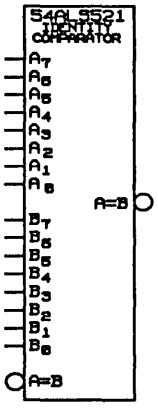

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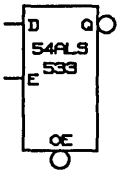

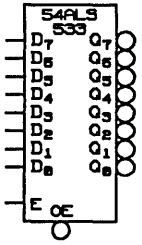

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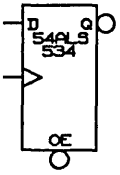

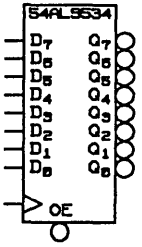

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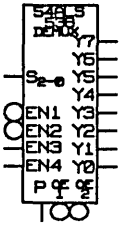

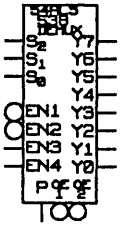

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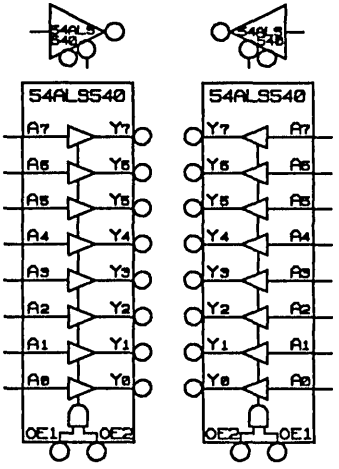

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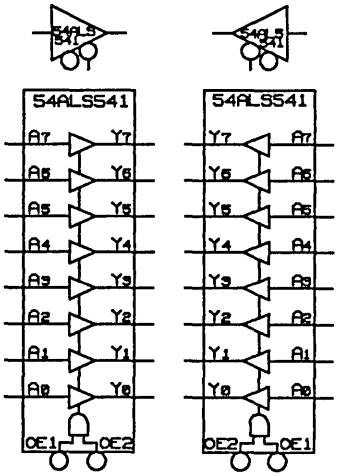

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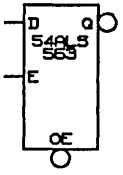

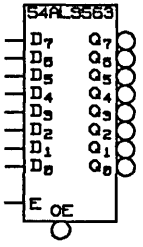

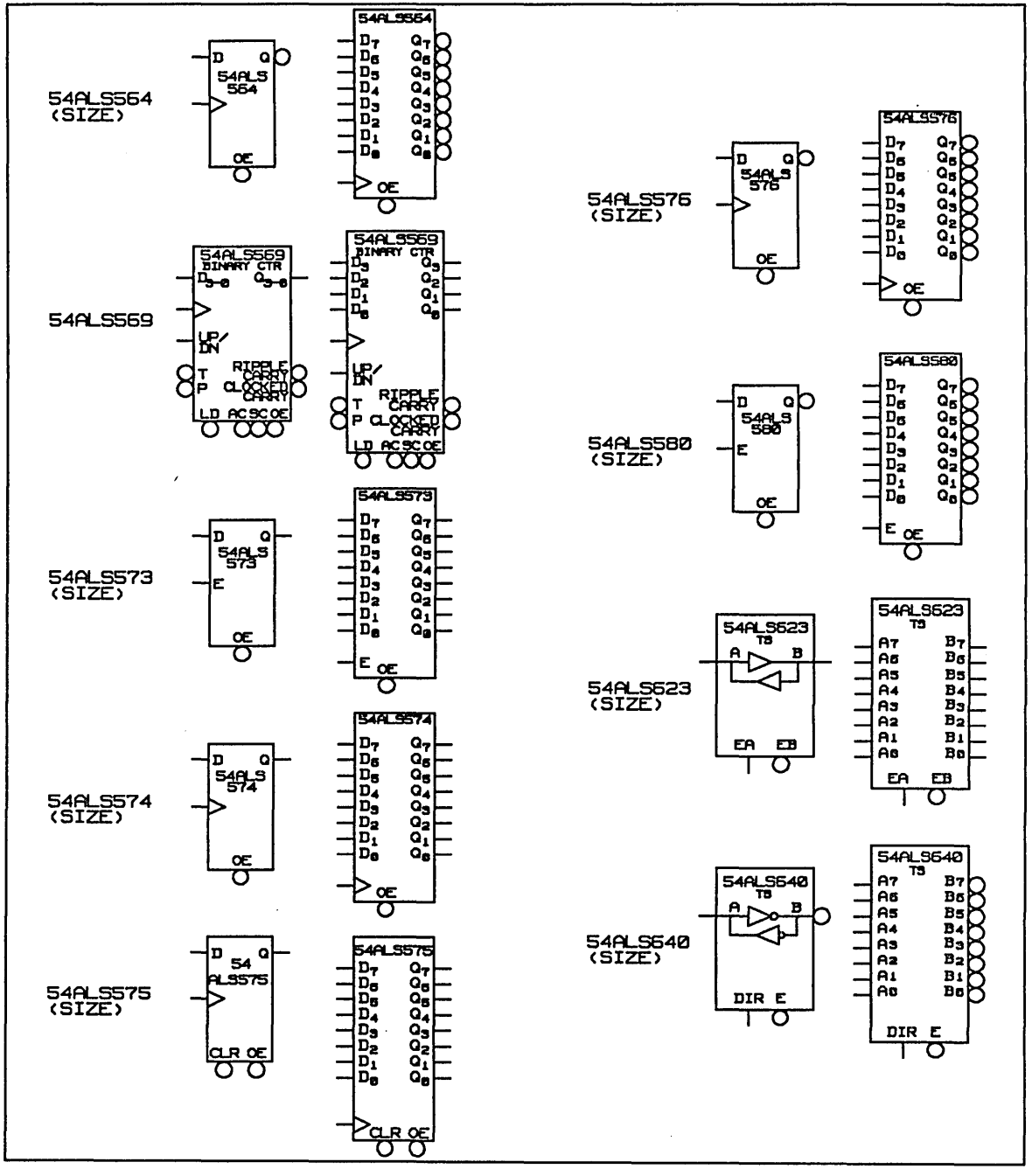
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54ALS576
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54ALS580
(SIZE)
54ALS623
(SIZE)
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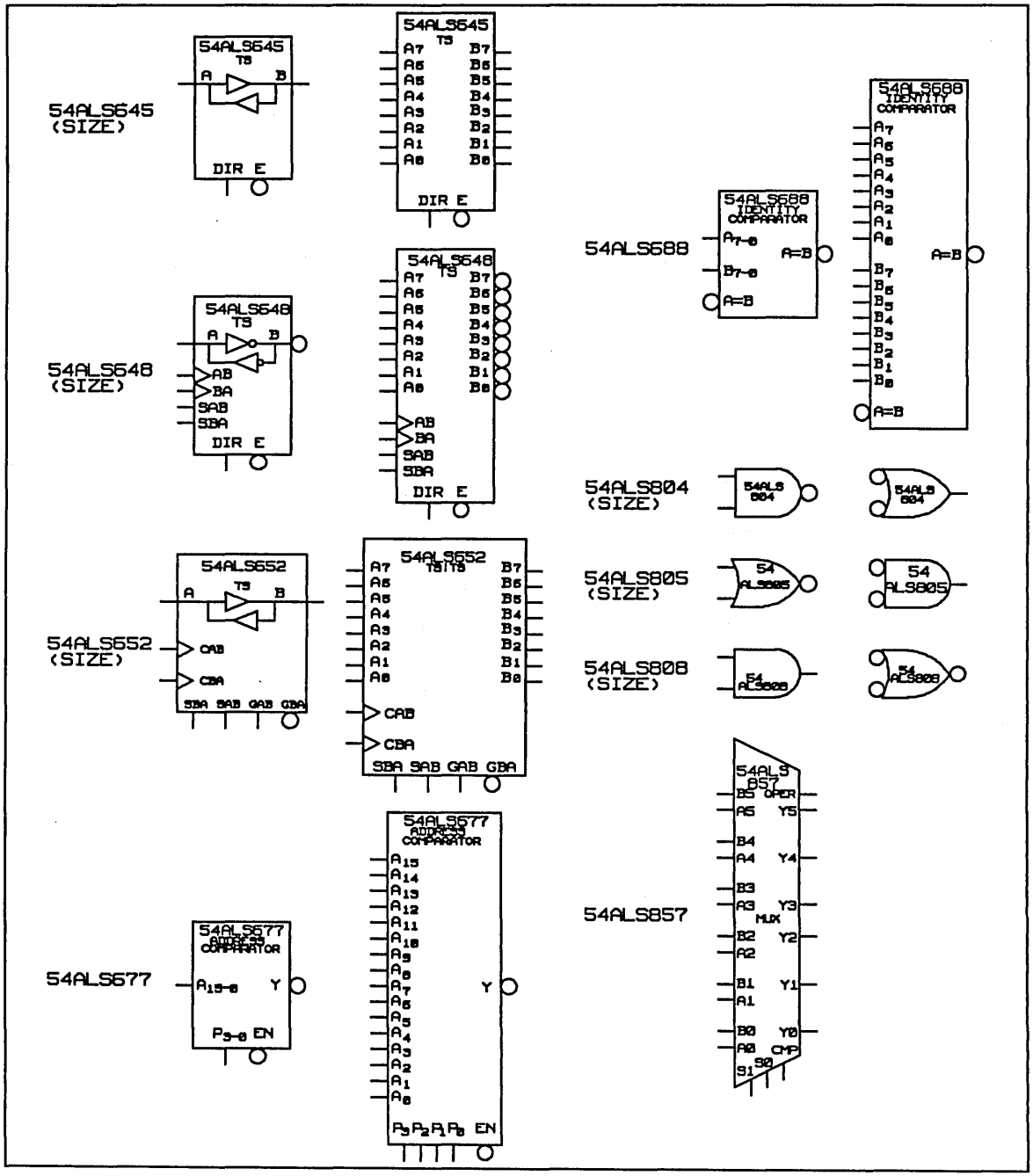
(SIZE)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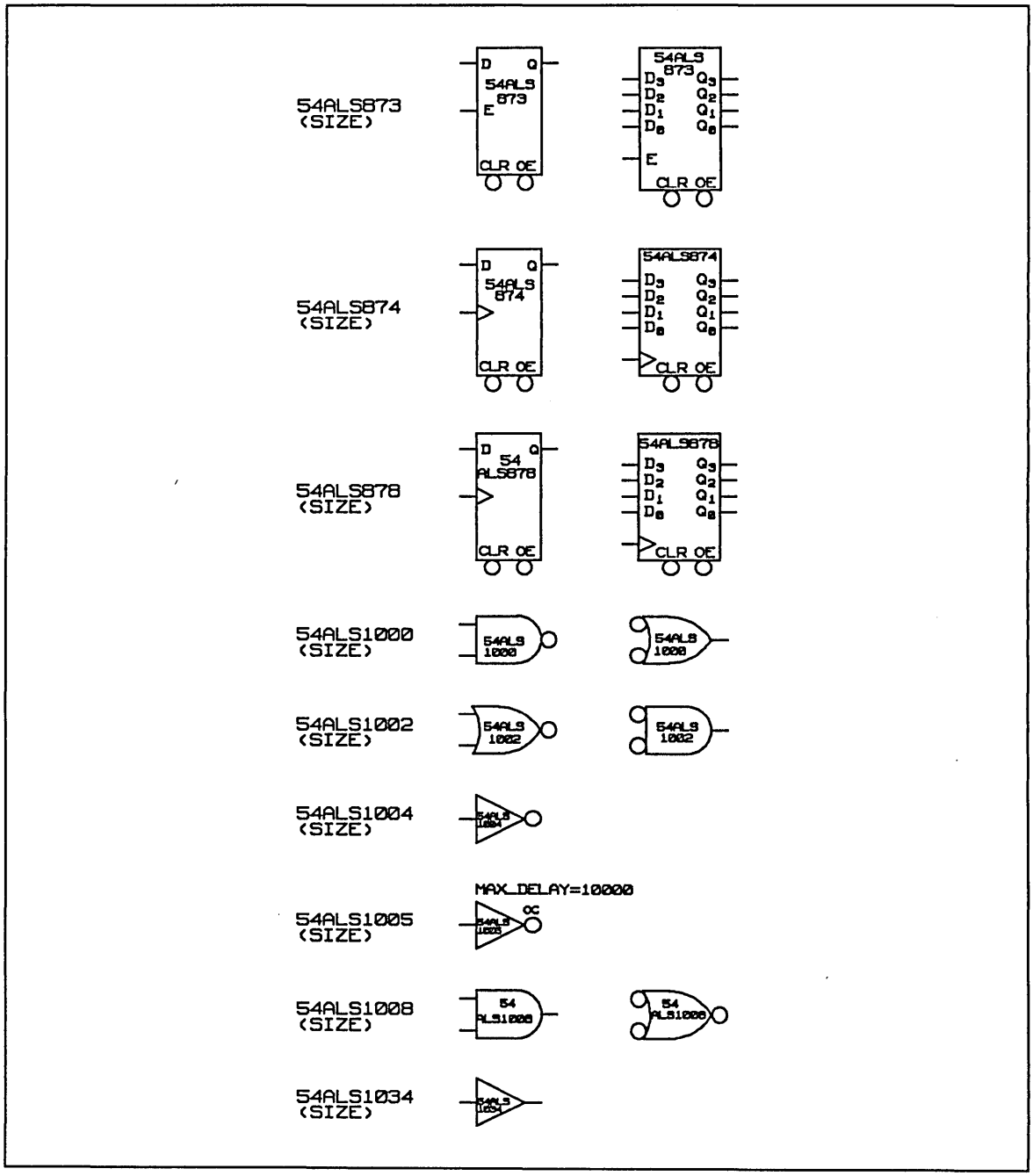
TS
A
B
DIR E
54ALS645
TS
A7 B7
A6 B6
A5 B5
A4 B4
A3 B3
A2 B2
A1 B1
A0 B0
DIR E
54ALS648
(SIZE)
54ALS648
TS
A
B
AB
BA
SAB
SBA
DIR E
54ALS648
TS
A7 B7
A6 B6
A5 B5
A4 B4
A3 B3
A2 B2
A1 B1
A0 B0
AB
BA
SAB
SBA
DIR E
54ALS652
(SIZE)
54ALS652
A
TS
B
CAB
CBA
SBA SAB GAB GBA
54ALS652
TS/TS
A7 B7
A6 B6
A5 B5
A4 B4
A3 B3
A2 B2
A1 B1
A0 B0
CAB
CBA
SBA SAB GAB GBA
54ALS677
54ALS677
ADDRESS
COMPARATOR
A15-0
Y
P3-0 EN
54ALS677
ADDRESS
COMPARATOR
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
Y
P3 P2 P1 P0 EN
54ALS688
(SIZE)
54ALS688
IDENTITY
COMPARATOR
A7-0
B7-0
A=B
A=B
54ALS688
IDENTITY
COMPARATOR
A7
A6
A5
A4
A3
A2
A1
A0
A=B
B7
B6
B5
B4
B3
B2
B1
B0
A=B
54ALS804
(SIZE)
54ALS
804
54ALS
804
54ALS805
(SIZE)
54
ALS805
54
ALS805
54ALS808
(SIZE)
54
ALS808
54
ALS808
54ALS857
54ALS
857
B5 OPER
A5 Y5
B4
A4 Y4
B3
A3 Y3
MUX
B2 Y2
A2
B1 Y1
A1
B0 Y0
A0 CMP
S0
S1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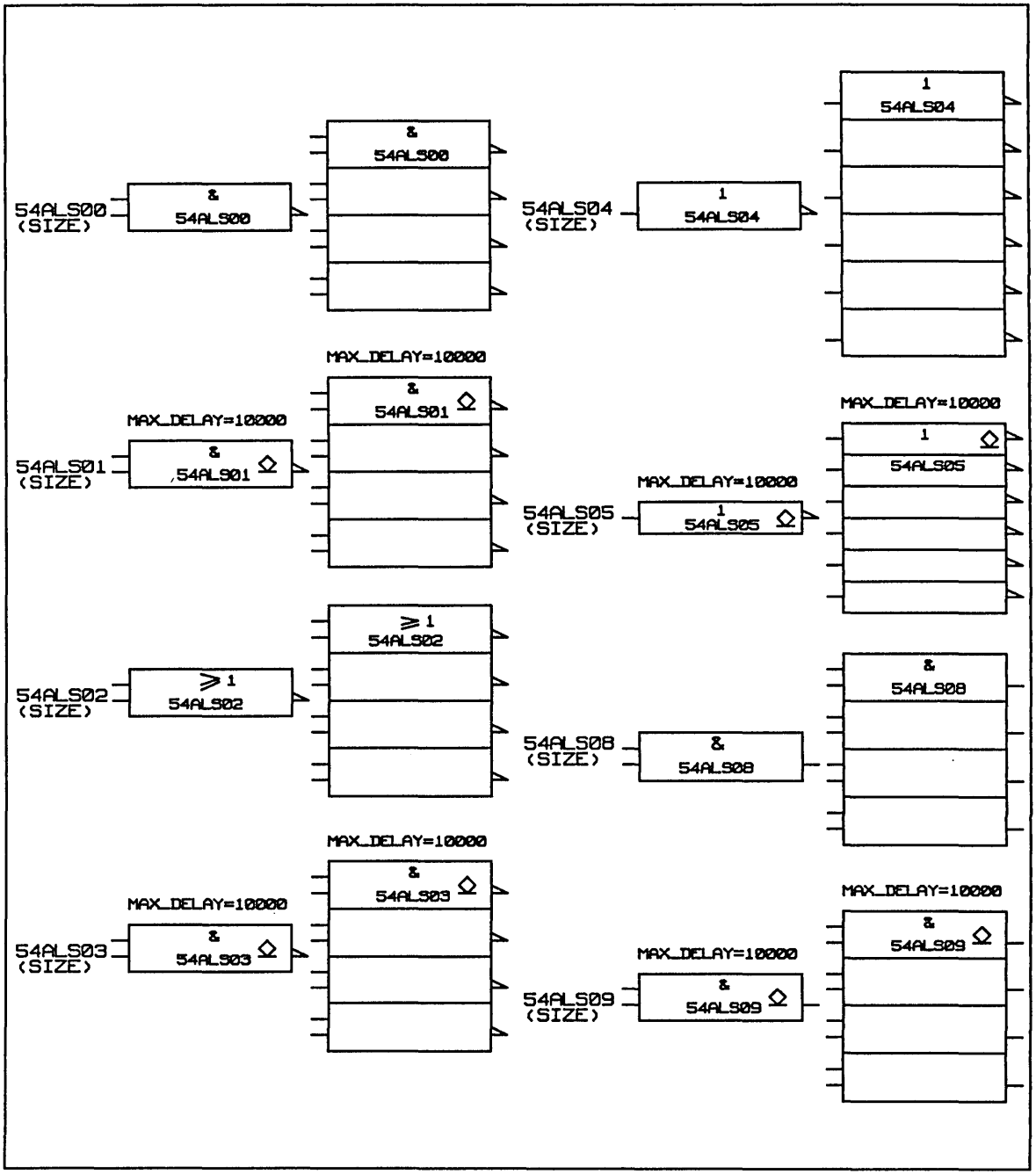
D
Q
54ALS
873
E
CLR OE
54ALS
873
D3
D2
D1
D0
Q3
Q2
Q1
Q0
E
CLR OE
54ALS874
(SIZE)
D
Q
54ALS
874
CLR OE
54ALS874
D3
D2
D1
D0
Q3
Q2
Q1
Q0
CLR OE
54ALS878
(SIZE)
D
Q
54
ALS878
CLR OE
54ALS878
D3
D2
D1
D0
Q3
Q2
Q1
Q0
CLR OE
54ALS1000
(SIZE)
54ALS
1000
54ALS
1000
54ALS1002
(SIZE)
54ALS
1002
54ALS
1002
54ALS1004
(SIZE)
MAX_DELAY=10000
54ALS1005
(SIZE)
OC
54ALS1008
(SIZE)
54
ALS1008
54
ALS1008
54ALS1034
(SIZE)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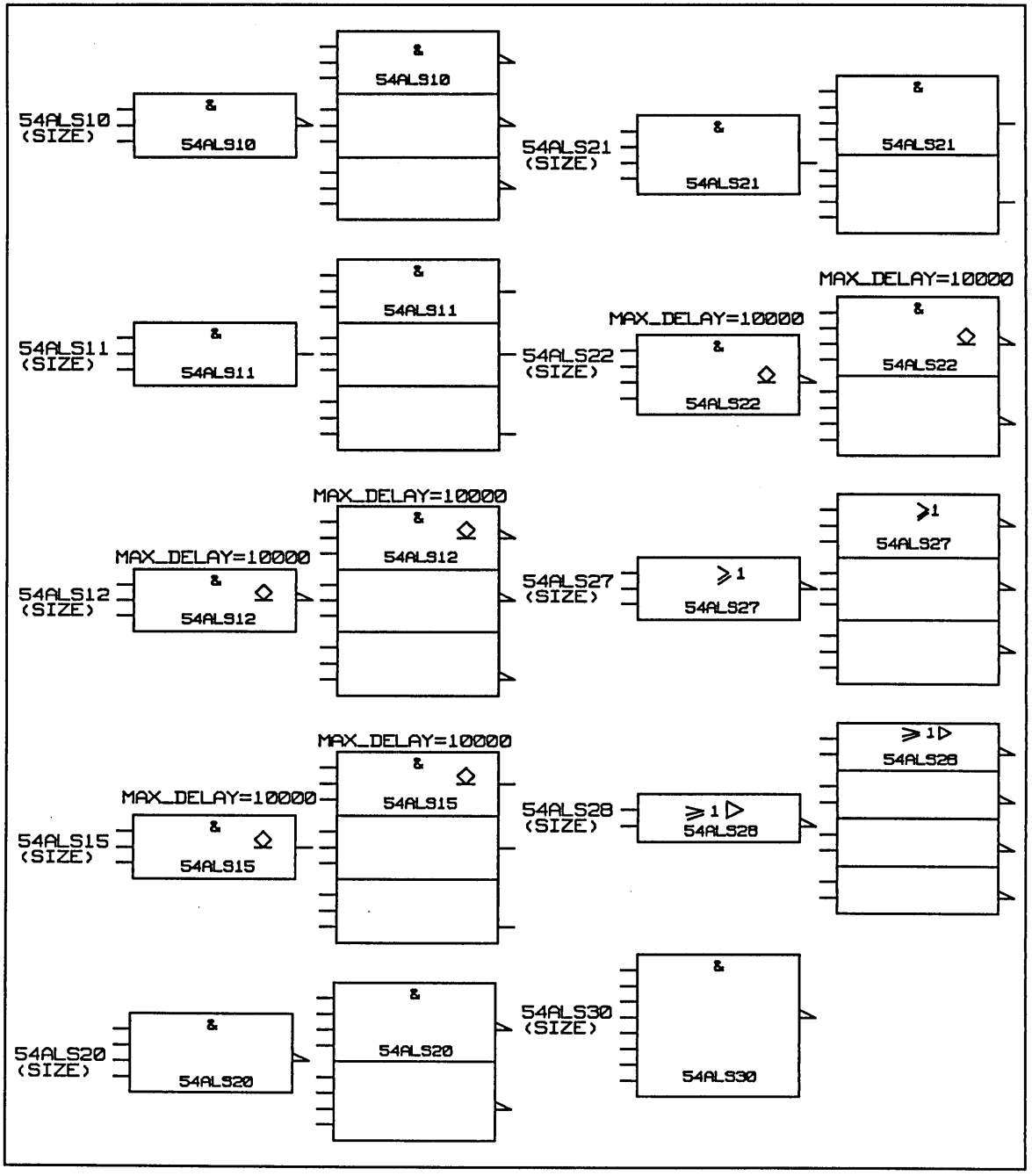
(SIZE)
&
54ALS00
&
54ALS00
54ALS04
(SIZE)
1
54ALS04
1
54ALS04
MAX_DELAY=10000
54ALS01
(SIZE)
MAX_DELAY=10000
&
54ALS01
&
54ALS01
MAX_DELAY=10000
54ALS05
(SIZE)
MAX_DELAY=10000
1
54ALS05
1
54ALS05
54ALS02
(SIZE)
≥1
54ALS02
≥1
54ALS02
54ALS08
(SIZE)
&
54ALS08
&
54ALS08
MAX_DELAY=10000
54ALS03
(SIZE)
MAX_DELAY=10000
&
54ALS03
&
54ALS03
54ALS09
(SIZE)
MAX_DELAY=10000
&
54ALS09
&
54ALS09
MAX_DELAY=10000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&
54ALS10
&
54ALS10
54ALS21
(SIZE)
&
54ALS21
&
54ALS21
54ALS11
(SIZE)
&
54ALS11
&
54ALS11
MAX_DELAY=10000
54ALS22
(SIZE)
&
54ALS22
MAX_DELAY=10000
&
54ALS22
MAX_DELAY=10000
54ALS12
(SIZE)
&
54ALS12
MAX_DELAY=10000
&
54ALS12
54ALS27
(SIZE)
≥1
54ALS27
≥1
54ALS27
MAX_DELAY=10000
54ALS15
(SIZE)
&
54ALS15
MAX_DELAY=10000
&
54ALS15
54ALS28
(SIZE)
≥1
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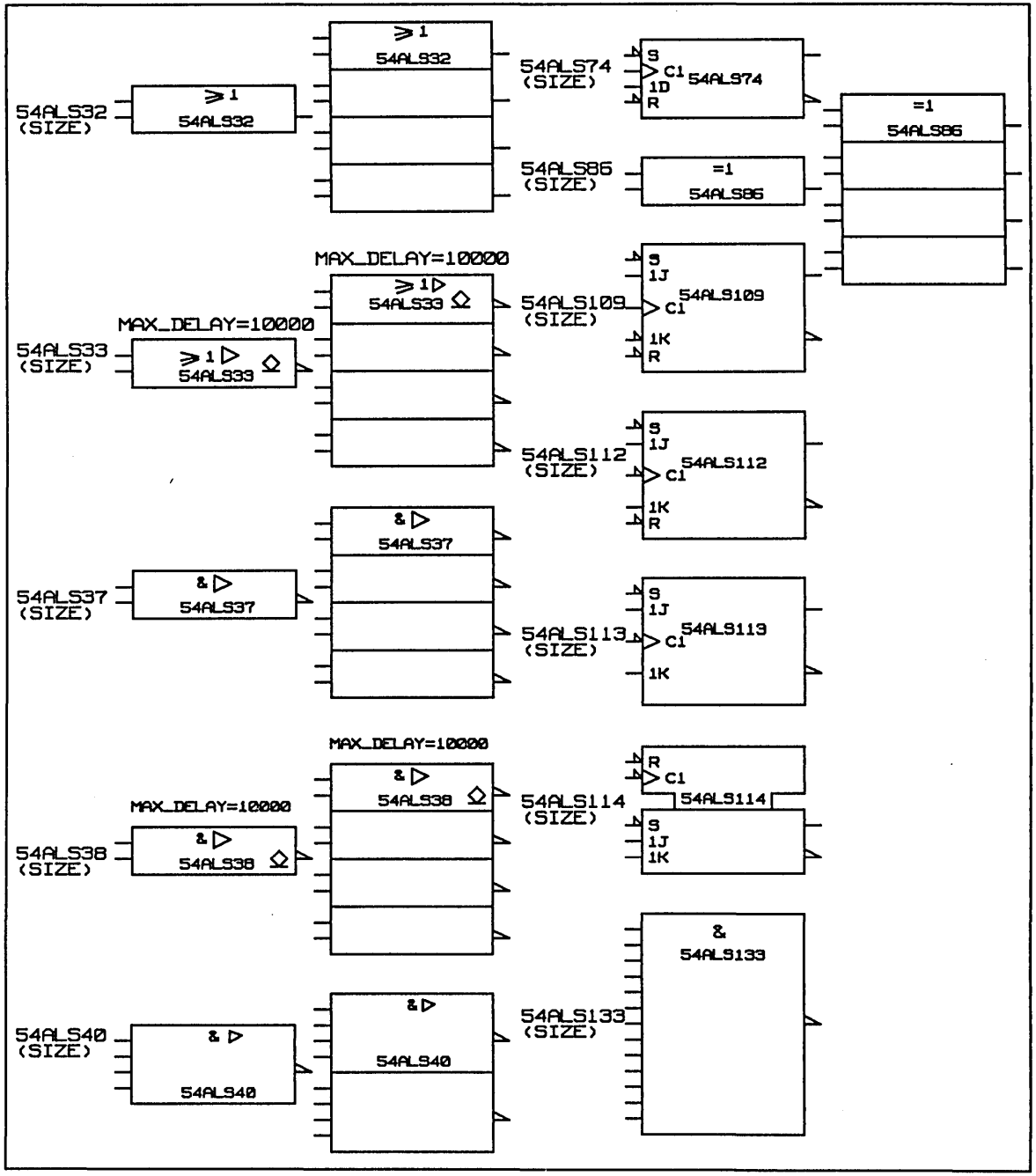
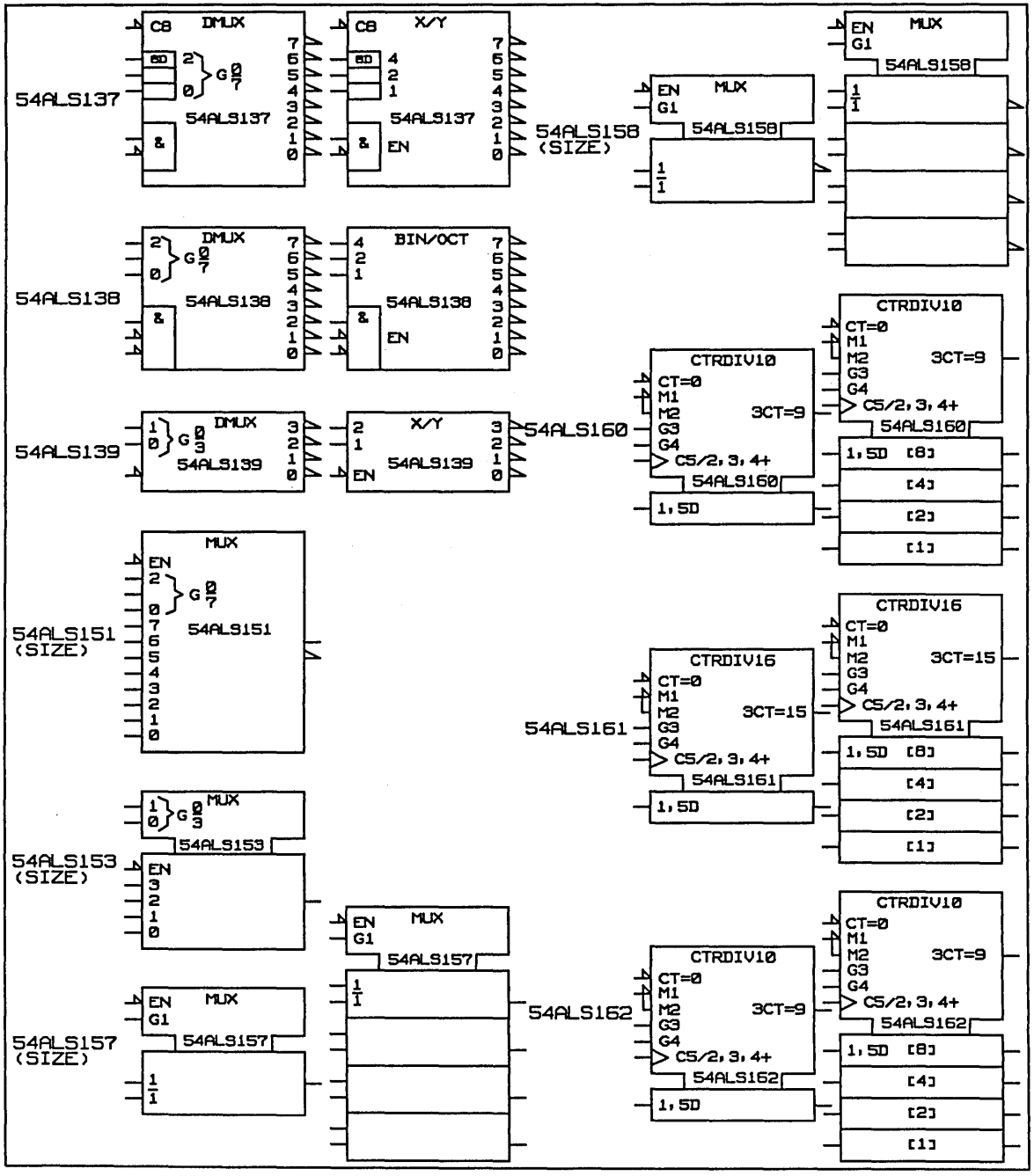
≥1
54ALS28
54ALS20
(SIZE)
&
54ALS20
&
54ALS20
54ALS30
(SIZE)
&
54ALS30


54ALS32
(SIZE)
≥1
54ALS32
≥1
54ALS32
54ALS74
(SIZE)
S
C1
1D
R
54ALS74
54ALS86
(SIZE)
=1
54ALS86
=1
54ALS86
MAX_DELAY=10000
54ALS33
(SIZE)
≥1
54ALS33
MAX_DELAY=10000
≥1
54ALS33
54ALS109
(SIZE)
S
1J
C1
1K
R
54ALS109
54ALS112
(SIZE)
S
1J
C1
1K
R
54ALS112
54ALS37
(SIZE)
&
54ALS37
&
54ALS37
54ALS113
(SIZE)
S
1J
C1
1K
54ALS113
MAX_DELAY=10000
54ALS38
(SIZE)
&
54ALS38
MAX_DELAY=10000
&
54ALS38
54ALS114
(SIZE)
R
C1
54ALS114
S
1J
1K
54ALS40
(SIZE)
&
54ALS40
&
54ALS40
54ALS133
(SIZE)
&
54ALS133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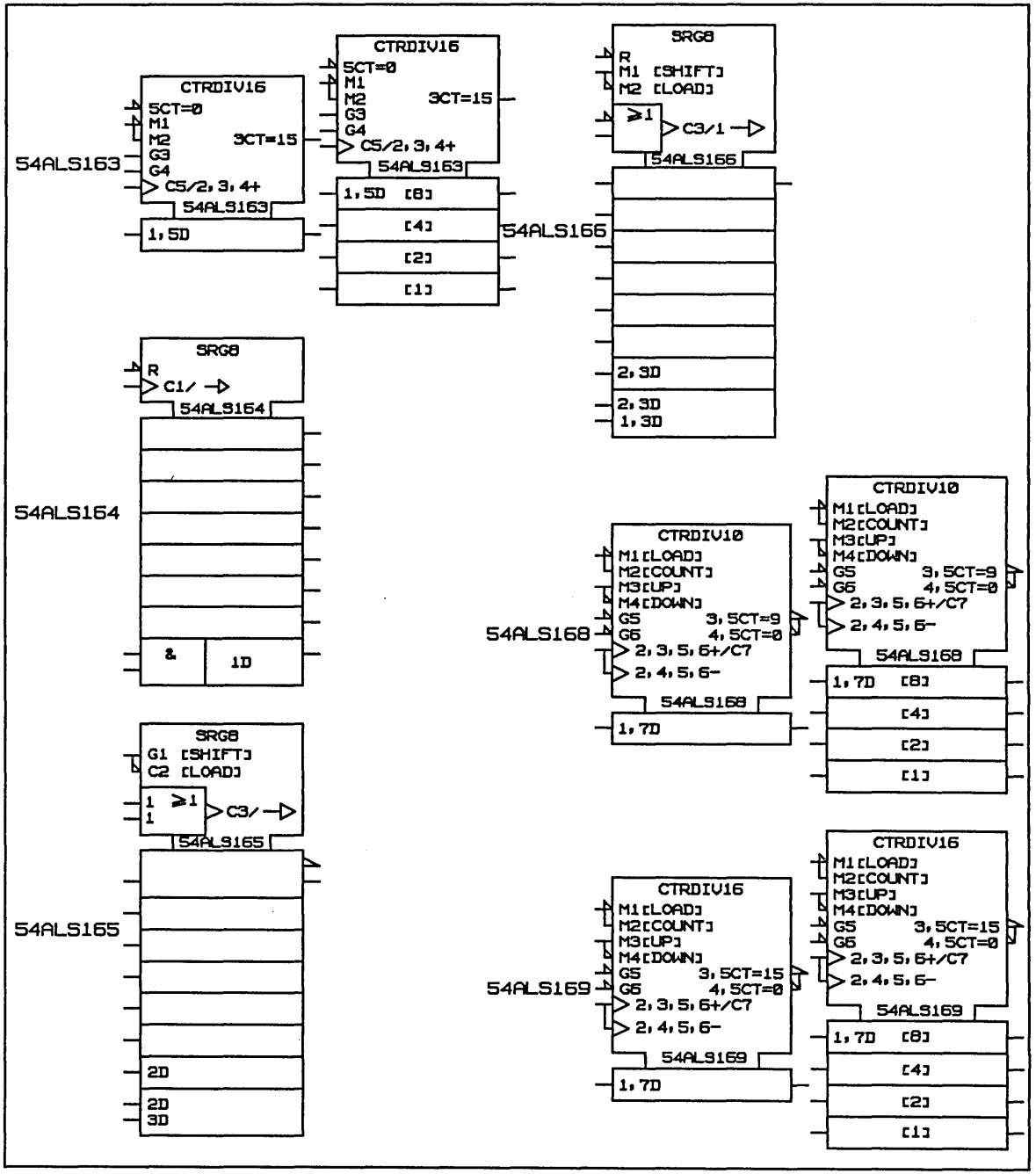
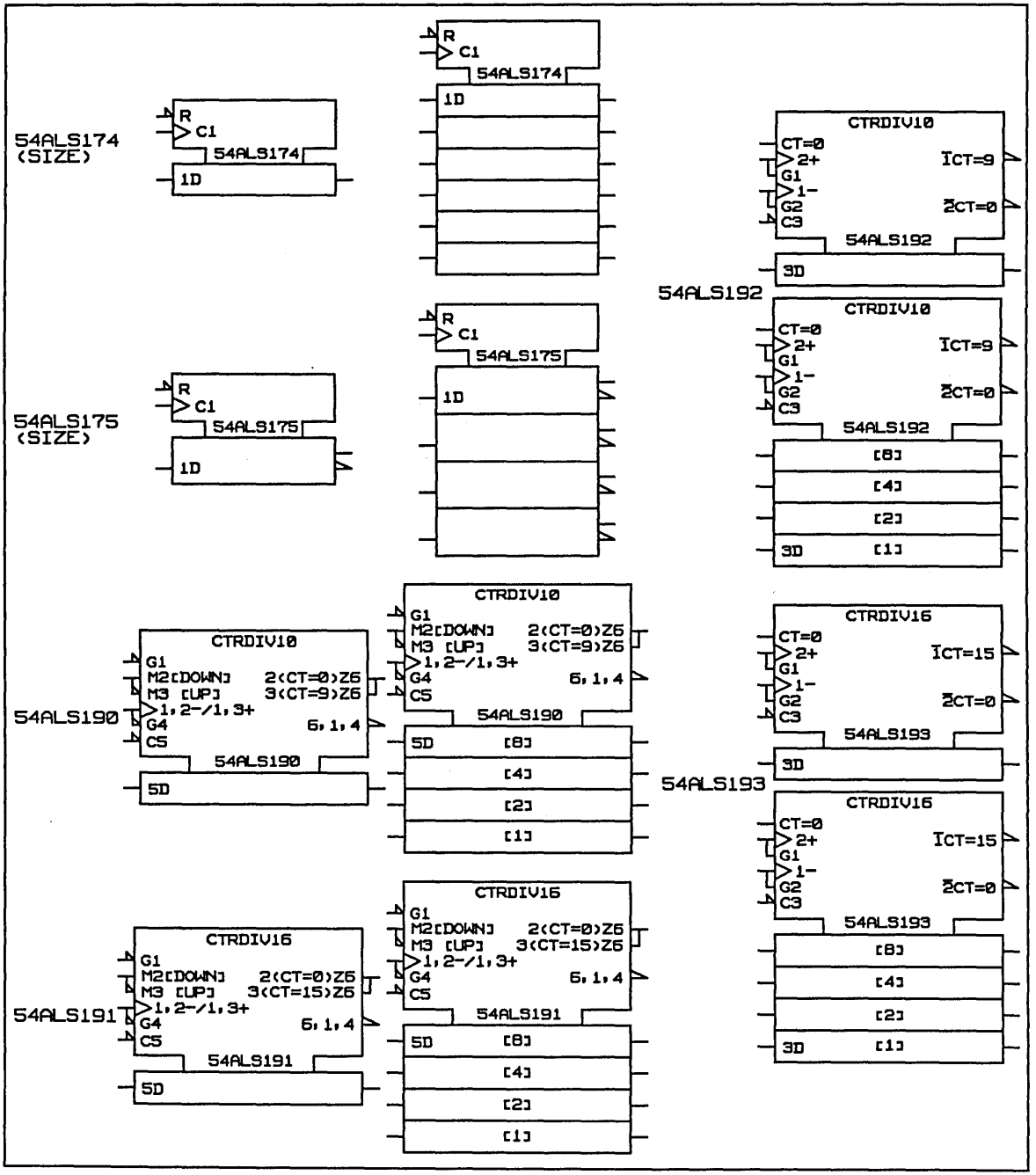
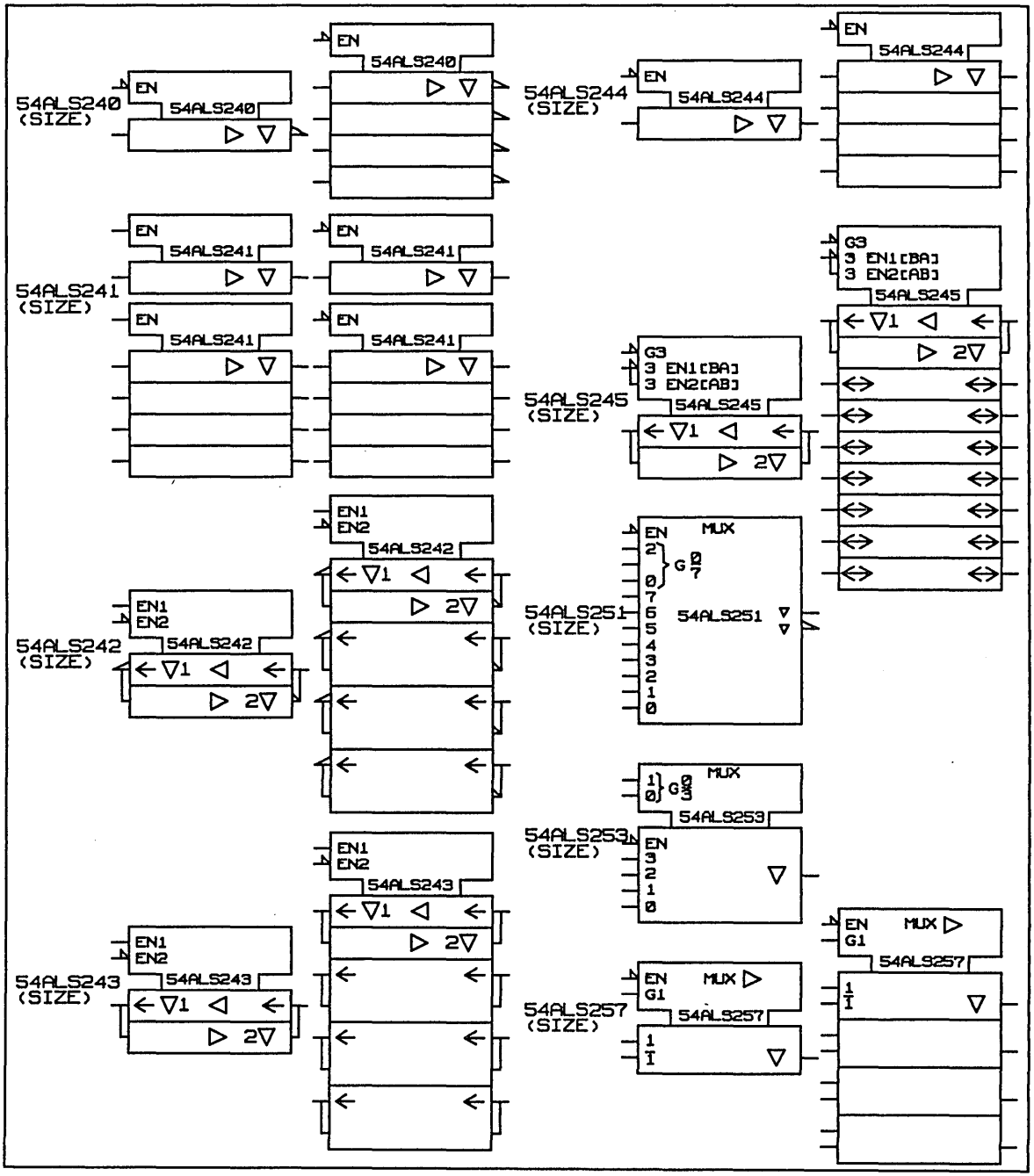
54ALS138
54ALS139
54ALS151
(SIZE)
54ALS153
(SIZE)
54ALS157
(SIZE)
54ALS158
(SIZE)
54ALS160
54ALS161
54ALS162
DMUX
X/Y
BIN/OCT
MUX
CTRDIV10
CTRDIV16
3CT=9
3CT=15
C5/2,3,4+
1,5D


CTRDIV16
5CT=0
M1
M2
G3
G4
C5/2, 3, 4+
3CT=15
54ALS163
1, 5D
[8]
[4]
[2]
[1]
SRG8
R
M1 [SHIFT]
M2 [LOAD]
≥1
C3/1
54ALS166
2, 3D
1, 3D
SRG8
R
C1/
54ALS164
&
1D
SRG8
G1 [SHIFT]
C2 [LOAD]
1
≥1
C3/
54ALS165
2D
3D
CTRDIV10
M1 [LOAD]
M2 [COUNT]
M3 [UP]
M4 [DOWN]
G5
G6
3, 5CT=9
4, 5CT=0
2, 3, 5, 6+/C7
2, 4, 5, 6-
54ALS168
1, 7D
CTRDIV16
3, 5CT=15
4, 5CT=0
54ALS169


54ALS174
(SIZE)
R
C1
54ALS174
1D
54ALS175
(SIZE)
54ALS175
54ALS190
CTRDIV10
G1
M2[DOWN]
M3 [UP]
1,2-/1,3+
G4
C5
2<CT=0>Z6
3<CT=9>Z6
6,1,4
5D
[8]
[4]
[2]
[1]
54ALS191
CTRDIV16
3<CT=15>Z6
54ALS192
CT=0
2+
G1
1-
G2
C3
ICT=9
ZCT=0
3D
54ALS193
ICT=15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EN
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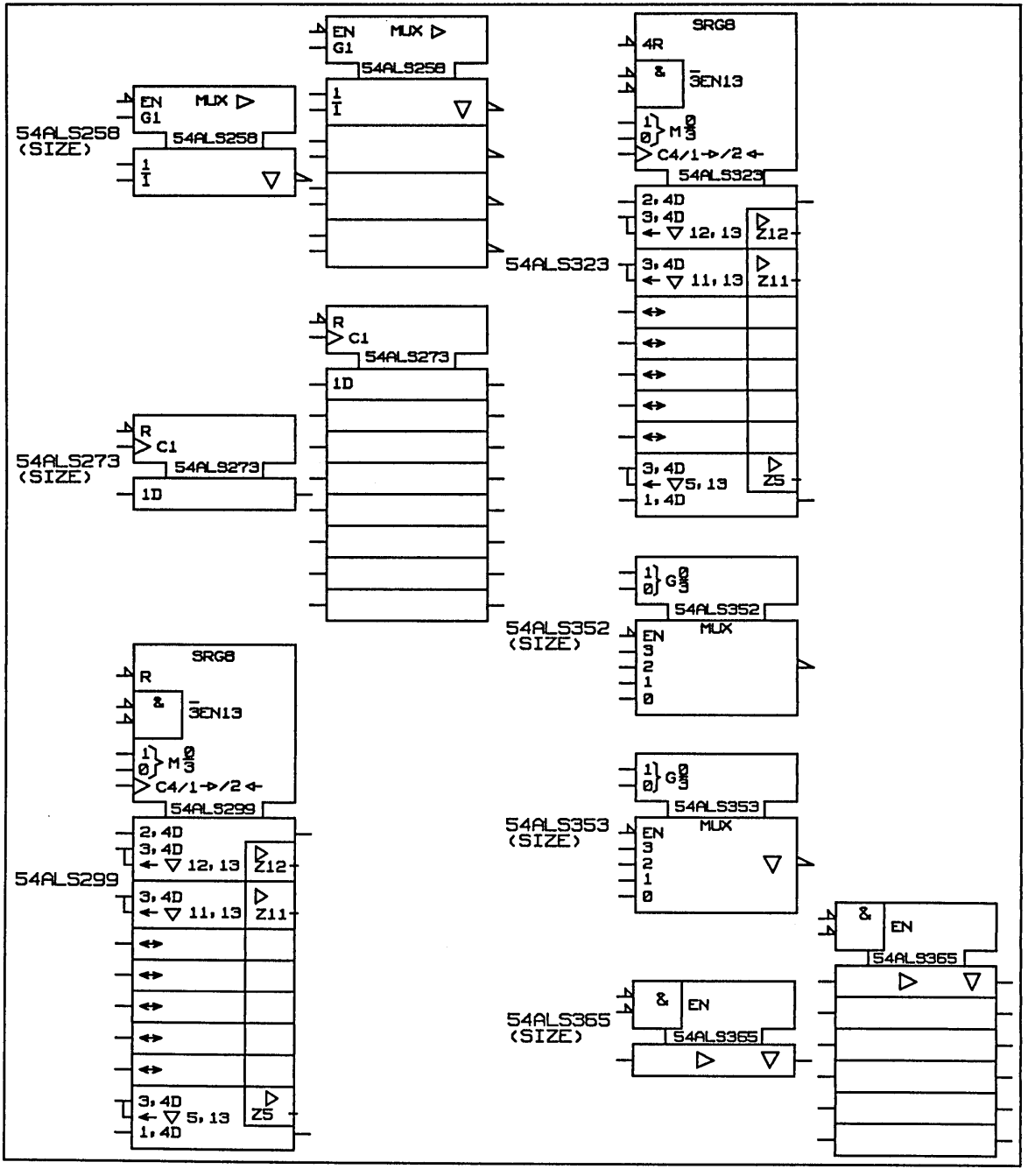
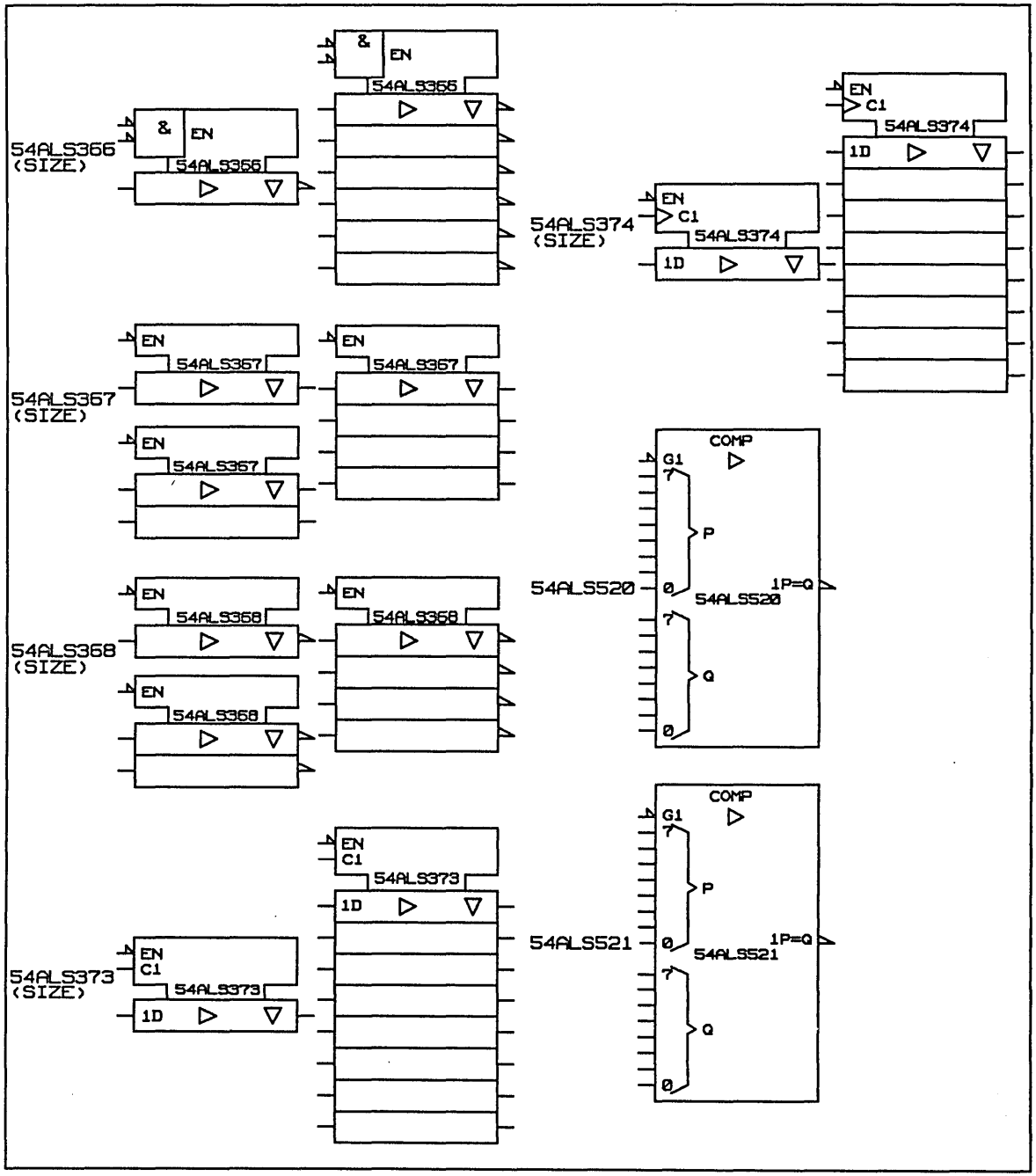
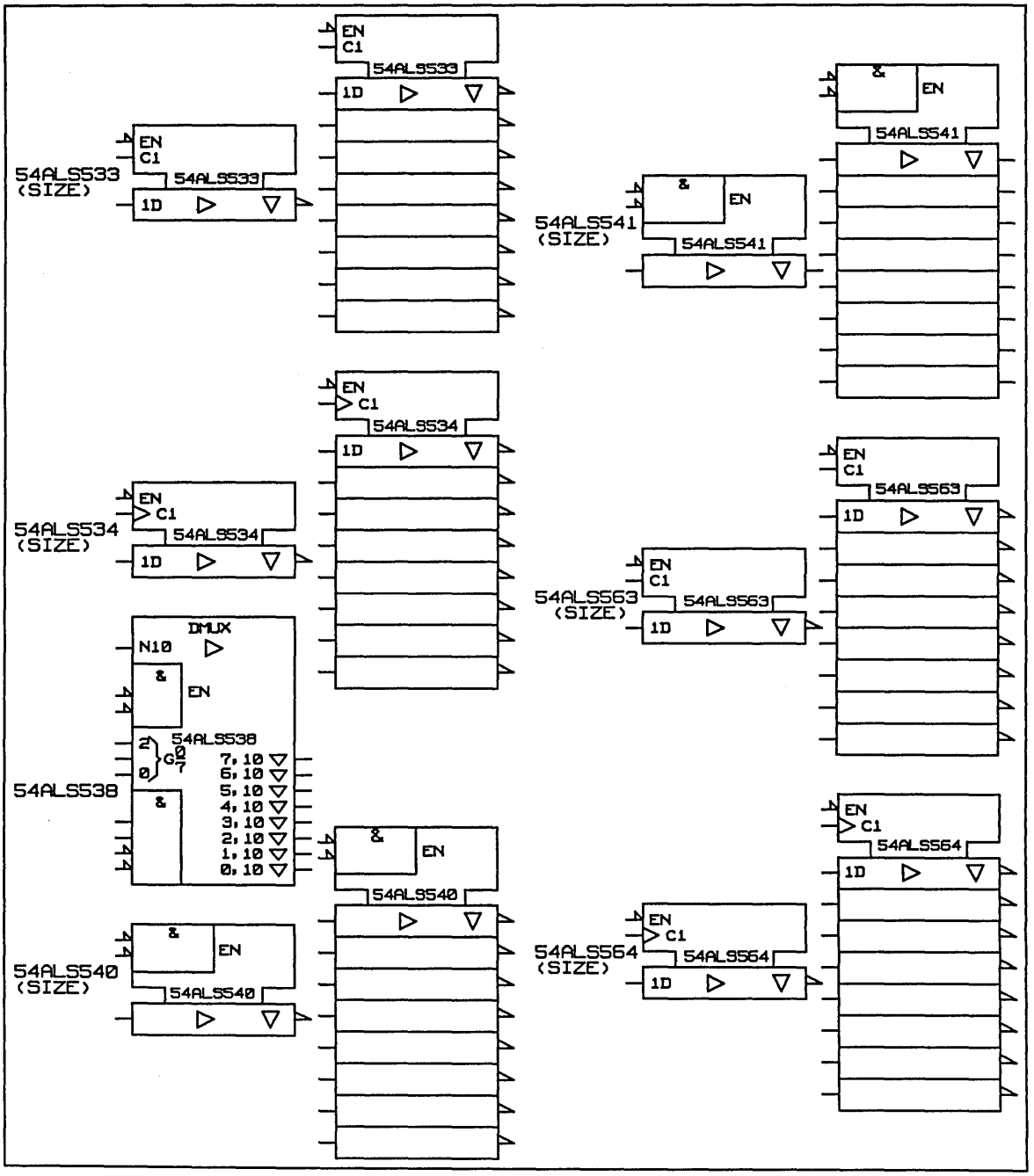
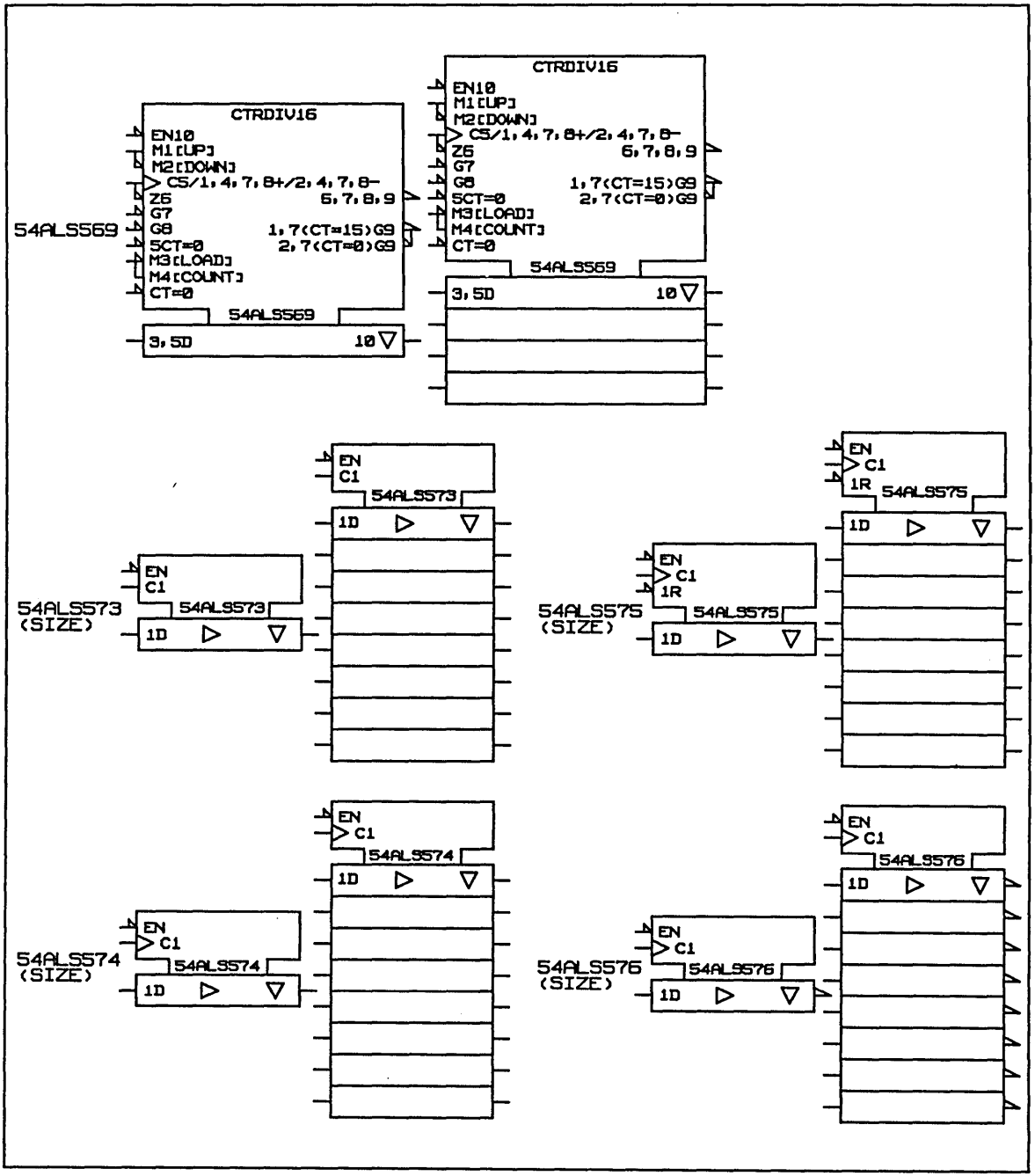
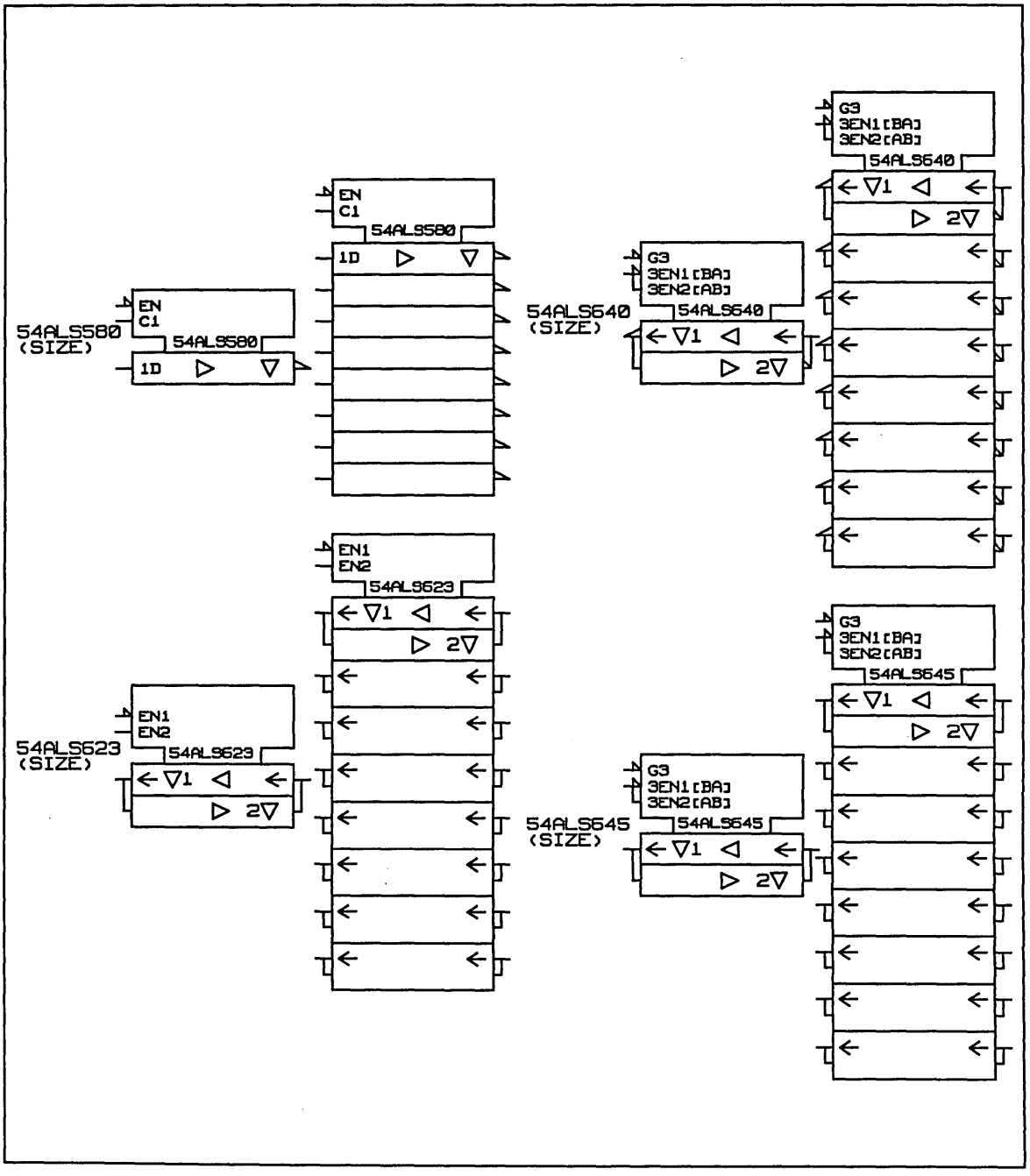
(SIZE)
54ALS241
54ALS242
(SIZE)
EN1
EN2
54ALS242
54ALS243
(SIZE)
54ALS243
54ALS244
(SIZE)
54ALS244
54ALS245
(SIZE)
G3
3 EN1[BA]
3 EN2[AB]
54ALS245
54ALS251
(SIZE)
MUX
54ALS251
54ALS253
(SIZE)
54ALS253
54ALS257
(SIZE)
G1
54ALS257

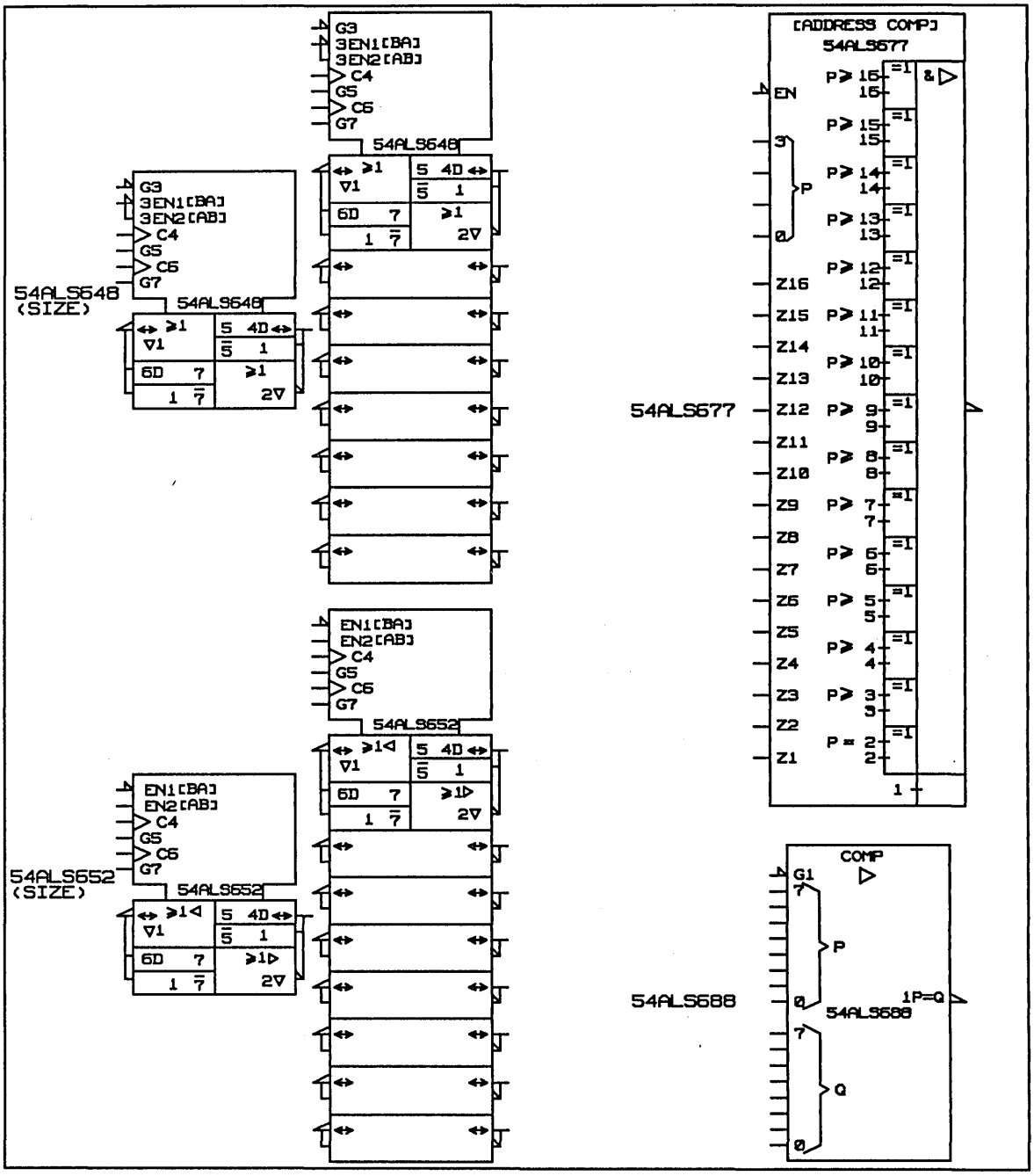

54ALS258
(SIZE)
EN
G1
MUX
54ALS258
1
I
54ALS323
SRG8
4R
&
3EN13
M
C4/1→/2←
54ALS323
2, 4D
3, 4D
12, 13
Z12
11, 13
Z11
5, 13
Z5
1, 4D
54ALS273
(SIZE)
R
C1
54ALS273
1D
54ALS352
(SIZE)
G
54ALS352
EN
MUX
54ALS299
54ALS353
(SIZE)
54ALS353
54ALS365
(SIZE)
54ALS365
EN


54ALS366
(SIZE)
&
EN
54ALS366
54ALS367
(SIZE)
EN
54ALS367
54ALS368
(SIZE)
54ALS368
54ALS373
(SIZE)
EN
C1
1D
54ALS373
54ALS374
(SIZE)
54ALS374
54ALS520
COMP
G1
P
Q
1P=Q
54ALS520
54ALS521
54ALS521


EN
C1
54ALS533
1D
54ALS533
(SIZE)
&
EN
54ALS541
54ALS541
(SIZE)
EN
C1
54ALS534
54ALS534
(SIZE)
EN
C1
54ALS563
54ALS563
(SIZE)
DMUX
N10
&
EN
54ALS538
G0
G7
7,10
6,10
5,10
4,10
3,10
2,10
1,10
0,10
54ALS538
54ALS540
54ALS540
(SIZE)
EN
C1
54ALS564
54ALS564
(SIZE)


CTRDIV16
EN10
M1[UP]
M2[DOWN]
C5/1,4,7,8+/2,4,7,8-
Z6
6,7,8,9
G7
G8
1,7(CT=15)G9
5CT=0
2,7(CT=0)G9
M3[LOAD]
M4[COUNT]
CT=0
54ALS569
3,5D
10
54ALS569
CTRDIV16
EN10
M1[UP]
M2[DOWN]
C5/1,4,7,8+/2,4,7,8-
Z6
6,7,8,9
G7
G8
1,7(CT=15)G9
5CT=0
2,7(CT=0)G9
M3[LOAD]
M4[COUNT]
CT=0
54ALS569
3,5D
10
EN
C1
54ALS573
1D
54ALS573
(SIZE)
EN
C1
54ALS573
1D
EN
C1
1R
54ALS575
1D
54ALS575
(SIZE)
EN
C1
1R
54ALS575
1D
EN
C1
54ALS574
1D
54ALS574
(SIZE)
EN
C1
54ALS574
1D
EN
C1
54ALS576
1D
54ALS576
(SIZE)
EN
C1
54ALS576
1D


EN
C1
54ALS580
1D
54ALS580
(SIZE)
EN1
EN2
54ALS623
54ALS623
(SIZE)
G3
3EN1[BA]
3EN2[AB]
54ALS640
54ALS640
(SIZE)
54ALS645
54ALS645
(SIZE)
▽1
2▽


54ALS648
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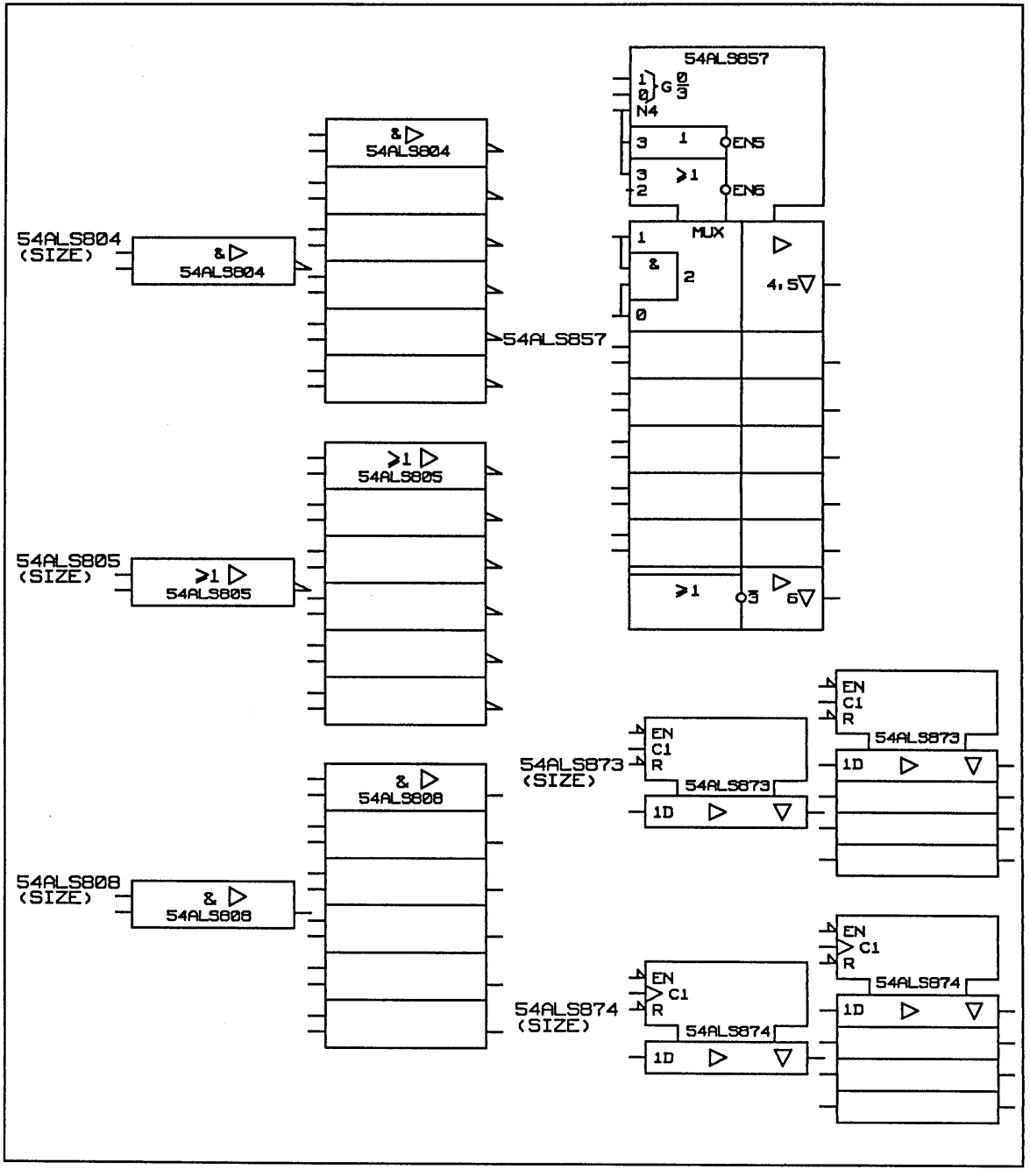
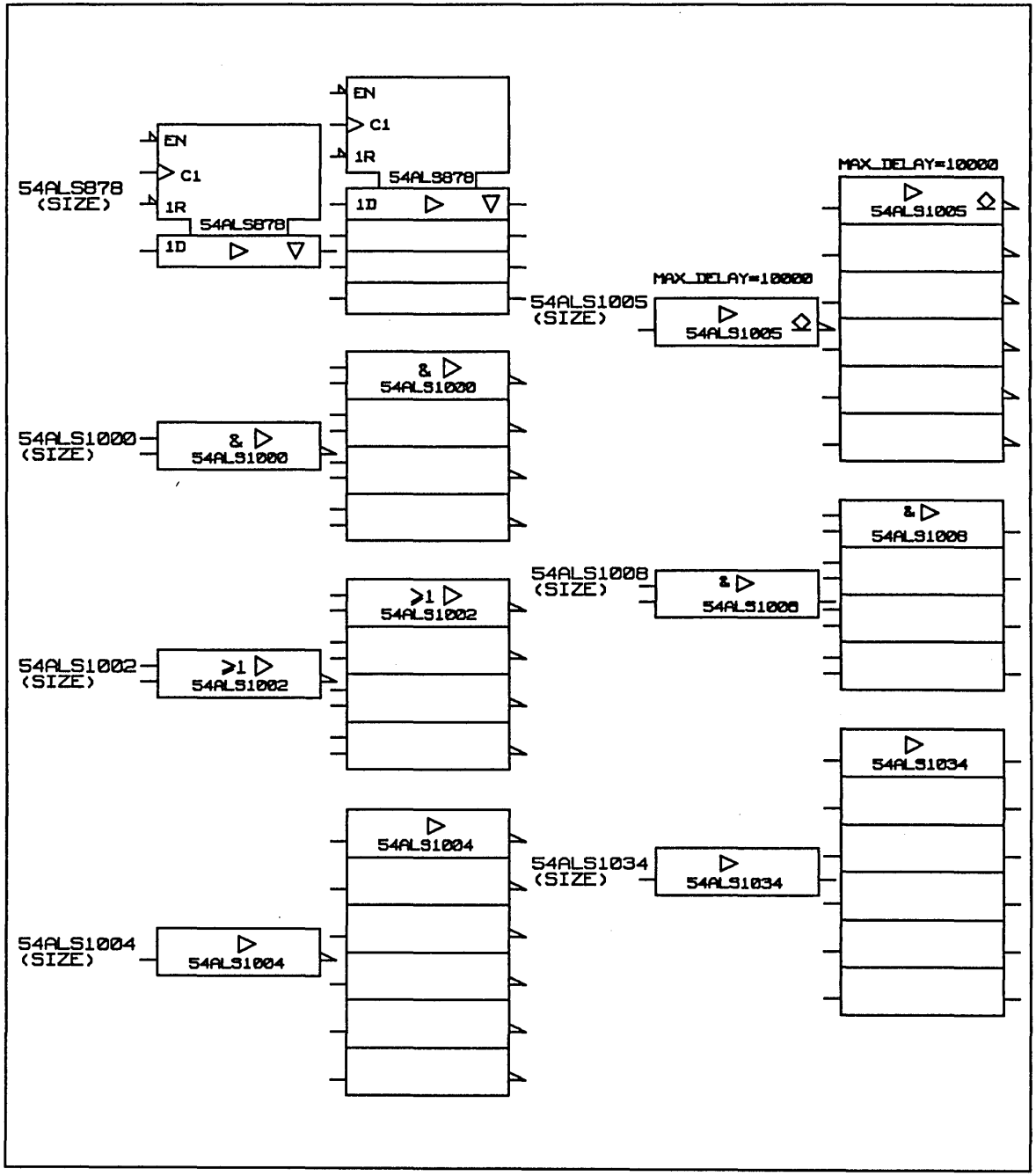
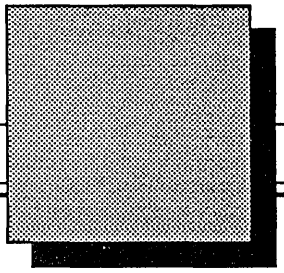
54ALS652
(SIZE)
54ALS677
54ALS688
54ALS677
54ALS688
COMP


54ALS857
G
N4
EN5
EN6
MUX
54ALS804
54ALS804
(SIZE)
54ALS857
54ALS805
54ALS805
(SIZE)
54ALS808
54ALS808
(SIZE)
54ALS873
(SIZE)
54ALS873
EN
C1
R
1D
54ALS874
(SIZE)
54ALS874


EN
C1
1R
54ALS878
1D
54ALS878 (SIZE)
MAX_DELAY=10000
54ALS1005
54ALS1005 (SIZE)
&
54ALS1000
54ALS1000 (SIZE)
54ALS1008
54ALS1008 (SIZE)
≥1
54ALS1002
54ALS1002 (SIZE)
54ALS1034
54ALS1034 (SIZE)
54ALS1004
54ALS1004 (SIZE)



The 54HCMOS and ANSI 54HCMOS Libraries

The 54HCMOS Library requires approximately 5373 Kbytes of disk storage, and the ANSI 54HCMOS Library requires approximately 5312 Kbytes of disk storage. The physical, timing, and simulation models for each library are identical and differ only in their body drawings. The part name for a component in either library is the same; the body drawing used is determined by the first library name encountered in the library search path (*54hcmos.lib* or *a54hcmos.lib*).

The release level of the 54HCMOS and ANSI 54HCMOS Libraries is 9.0.

Each library contains body drawings and physical, timing, and simulation models for the following 141 components:

54HC00	Quad 2-input NAND
54HC02	Quad 2-input NOR
54HC03	Quad 2-input open-collector NAND
54HC04	Hex inverter
54HC08	Quad 2-input AND
54HC10	Triple 3-input NAND
54HC11	Triple 3-input AND
54HC14	Hex Schmitt-trigger inverter
54HC20	Dual 4-input NAND
54HC27	Triple 3-input NOR
54HC30	8-input NAND
54HC32	Quad 2-input OR
54HC42	4-to-10-line decoder
54HC51	2-wide 3-input, 2-wide 2-input AND-OR-invert
54HC58	2-wide 3-input, 2-wide 2-input AND-OR
54HC73	Dual JK flip-flop with clear
54HC74	Dual positive-edge-triggered D flip-flop
54HC75	4-bit bistable latch
54HC76	Dual JK flip-flop with preset and clear
54HC85	4-bit magnitude comparator
54HC86	Quad 2-input exclusive-OR
54HC107	Dual JK negative-edge-triggered flip-flop
54HC109	Dual JKbar positive-edge-triggered flip-flop
54HC112	Dual JK negative-edge-triggered flip-flop
54HC113	Dual JK negative-edge-triggered flip-flop

54HC123	Dual retriggerable monostable multivibrators with clear
54HC125	Quad bus buffer with three-state output
54HC126	Quad bus buffer with three-state output
54HC132	Quad 2-input positive-NAND Schmitt triggers
54HC133	13-input NAND
54HC137	3-to-8 line decoder/demultiplexer with address latch
54HC138	3-to-8 line decoder/demultiplexer
54HC139	Dual 2-to-4 line decoder/multiplexer
54HC147	10-line decimal to 4-line BCD priority encoder
54HC151	1-of-8 data selector/multiplexer
54HC153	Dual 4-line to 1-line data multiplexer
54HC154	4-to-16 line decoder/demultiplexer
54HC157	Quad 2-to-1-line non-inverting multiplexer
54HC158	Quad 2-to-1-line inverting data multiplexer
54HC160	4-bit synchronous decade counters with direct clear
54HC161	4-bit synchronous binary counters with direct clear
54HC162	4-bit synchronous decade counters with synchronous clear
54HC163	4-bit synchronous binary counters with synchronous clear
54HC164	8-bit parallel output serial shift register
54HC165	8-bit serial output shift register

54HC166	8-bit shift register
54HC173	Quad D-type flip-flop
54HC174	Hex D-type flip-flop
54HC175	Quad D-type flip-flop
54HC180	9-bit parity generator/checker
54HC182	Look-ahead carry generators
54HC190	Synchronous BCD up/down counter
54HC191	Synchronous binary up/down counter
54HC192	Synchronous BCD up/down counter
54HC193	Synchronous binary up/down dual clock counters
54HC194	4-bit bidirectional shift register
54HC195	4-bit universal shift register
54HC221	Dual non-retriggerable monostable multivibrator
54HC237	3-to-8 line decoder/demultiplexer with address latch
54HC240	Octal inverting 3-state bus transceiver
54HC241	Octal non-inverting 3-state bus transceiver
54HC242	Quad inverting 3-state bus transceiver
54HC243	Quad non-inverting 3-state bus transceiver
54HC244	Octal non-inverting 3-state bus transceiver
54HC245	Octal non-inverting 3-state bus transceiver
54HC251	3-state data multiplexer
54HC253	Dual data selector/multiplexer
54HC259	8-bit addressable latches
54HC266	Quad 2-input exclusive-NOR gate
54HC257	Quad 3-state non-inverting data multiplexer

54HC273	Octal D-type flip-flop
54HC280	9-bit odd/even parity generators/checker
54HC283	4-bit binary full adders
54HC292	Programmable frequency divider/digital timer
54HC294	Programmable frequency divider/digital timer
54HC298	Quad 2-input multiplexers with storage
54HC299	8-bit bidirectional 3-state shift/storage register
54HC354	1-of-8 data selector/multiplexer with data and address latches and 3-state output
54HC356	1-of-8 data selector/multiplexer with data and address latches and 3-state output
54HC365	Hex non-inverted 3-state bus drivers
54HC366	Hex inverted 3-state bus drivers
54HC367	Hex bus driver
54HC368	Hex bus driver
54HC373	Octal 3-state D-latch with common enable
54HC374	Octal 3-state positive-edge-triggered D register
54HC390	Dual 4-stage binary ripple counter
54HC393	Dual 4-stage binary ripple counter
54HC423	Dual retriggerable monostable multivibrators
54HC533	8-bit latch with inverting outputs
54HC534	8-bit register with inverting outputs
54HC540	Octal buffers and line drivers with 3-state outputs
54HC541	Octal buffers and line drivers with 3-state outputs
54HC563	8-bit latch with inverting 3-state outputs
54HC564	8-bit register with inverting 3-state outputs
54HC573	Octal latch with three-state output

54HC574	Octal D-type flip-flop with three-state output
54HC590	8-bit binary counter/three state latch
54HC595	8-bit serial-input/serial- or parallel-output shift register with latched 3-state output
54HC597	8-bit serial- or parallel-input/serial-output shift register with input latch
54HC640	Octal 3-state inverting bus transceiver
54HC643	Octal 3-state inverting and non-inverting bus transceiver
54HC646	Octal 3-state non-inverting bus transceiver and D-type flip-flop
54HC648	Octal 3-state inverting bus transceiver and D-type flip-flop
54HC688	8-bit equality comparator
54HC4002	Dual 4-input NOR
54HC4016	Quad analog switch/multiplexer/demultiplexer
54HC4017	Decade counter/divider
54HC4020	14-bit binary counter
54HC4024	7-bit binary counter
54HC4040	12-bit binary counter
54HC4049	Hex inverting buffer/logic-level down converter
54HC4050	Hex non-inverting buffer/logic-level down converter
54HC4051	8-channel analog multiplexer/demultiplexer
54HC4052	Dual 4-channel analog multiplexer/demultiplexer
54HC4053	Triple 2-channel analog multiplexer/demultiplexer

54HC4066	Quad analog switch/multiplexer/demultiplexer with enhanced on-resistance linearity
54HC4075	Triple 3-input OR
54HC4078	8-input NOR/OR
54HC4316	Quad analog switch/multiplexer/demultiplexer with separate analog and digital power supplies
54HC4351	8-channel analog multiplexer/demultiplexer with address latch
54HC4352	Dual 4-channel analog multiplexer/demultiplexer with address latch
54HC4353	Triple 2-channel analog multiplexer/demultiplexer with address latch
54HC4514	4-to-16 line decoder/demultiplexer with address latch
54HC4538	Dual monostable multivibrator
54HCT00	Quad 2-input NAND gate
54HCT02	Quad 2-input NOR gate
54HCT04	Hex inverter
54HCT32	Quad 2-input OR gate
54HCT138	3-to-8 line decoder/demultiplexer
54HCT240	Octal inverting 3-state bus transceiver
54HCT241	Octal non-inverting 3-state bus transceiver
54HCT244	Octal non-inverting 3-state bus transceiver
54HCT245	Octal three state bus transceiver
54HCT280	9-bit odd/even parity generators/checker
54HCT373	Octal 3-state D-latch with common enable

54HCT374	Octal 3-state positive-edge-triggered D register
54HCT640	Octal 3-state inverting bus transceiver
54HCT643	Octal 3-state inverting and non-inverting
54HCT688	8-bit equality comparator
54HCT670	4x4 register file/3-state output
54HCU04	Hex inverter

Application Notes

Monostable Multivibrators

The 54HC123, 54HC423, 54HC221, and 54HC4538 models fully support the simulation and timing behavior of retrigerrable and non-retriggerable multivibrators which are resettable at any time.

To use the simulation model, logic initialization or initial depositing of the same value (either 0 or 1) to internal signals D0 and D1 must be performed.

To use the timing verification model, the following must be observed:

- The Timing Verifier's directives file *(verifier.cmd)* must include the directive:

```
LATCH_ERR_MODEL CLOSED;
```

- The first trigger edge must occur after 'PULSE_WIDTH' ns.

- The maximum trigger frequency is

```
2 * RETRIG_DIV2 -1
```

  edges per 'PULSE_WIDTH' ns. Since RETRIG_DIV2 is defined to be 6 in the model, 2*6-1=11 clock edges are permitted in any 'PULSE_WIDTH' ns interval. If an application requires a greater trigger frequency, RETRIG_DIV2 must be redefined in the model.

Capacitive Loading Effects

The delay calculations for the timing and simulation models are based on values from the *Motorola High-Speed CMOS Logic Data* book (1983). The delay times are calculated using the short circuit current method with a Vcc of 4.5 volts and a temperature of 25°C (see page 4-12 of the data book). The typical drive is therefore:

0.5 * 4.5 / 17.3 (mA) = 0.13

The typical and maximum delays for the individual components in the data book are given with a capacitive load of 50pF. Using these values, the typical no-load delay is calculated from the equation:

typ_delay (no load) = *typ_delay* (50pF) - 0.13 * 50

Assuming that the ratio of maximum no-load delay to maximum delay (50pF) is the same as typical no-load delay to typical delay (50pF), the maximum no-load delay is:

typ_delay (no load) * *max_delay* (50pF) / *typ_delay* (50p

The minimum delay for timing and simulation models is one-half of typical or one-third of maximum; the minimum drive is calculated from:

min_delay (50pF) - *min_delay* (no load) / 50

The following examples show the delay and drive calculations for a 54HC00 and an 54HC74.

54HC00 Data Book:

typical delay (50pF) = 9
maximum delay (50pF) = 18
typical drive = 0.13

54HC00 Calculation:

typical delay (no load) = 9 - 0.13 * 50 = 2.5
maximum delay (no load) = 2.5 * 18 / 9 = 5.0
minimum delay (50pF) = 9 / 2 = 4.5
minimum delay (no load) = 2.5 / 2 = 1.25
maximum drive = (18 - 5) / 50pF = 0.26
minimum drive = (4.5 - 1.25) / 50pF = 0.065

From these calculations, the min/max delay for the 54HC00 timing model is 1.25/5.0, and the min/max drive for the timing model is 0.065/0.26. The min/typ/max delay for the 54HC00 simulation model is 1.25/2.5/5.0, and the min/typ/max drive for the simulation model is 0.065/0.13/0.26.

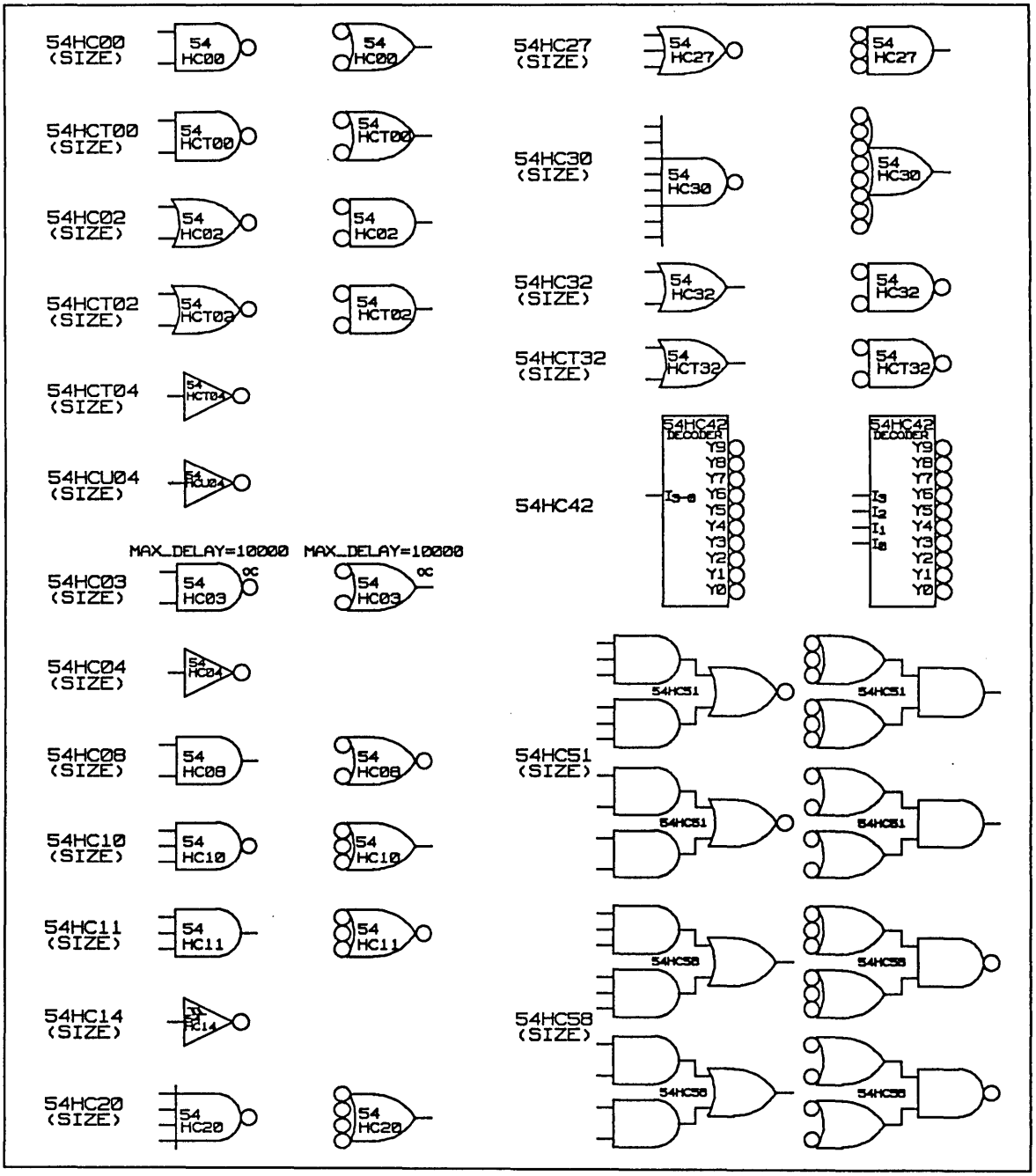
54HC74 Data Book (from CLK to Q or Q*):

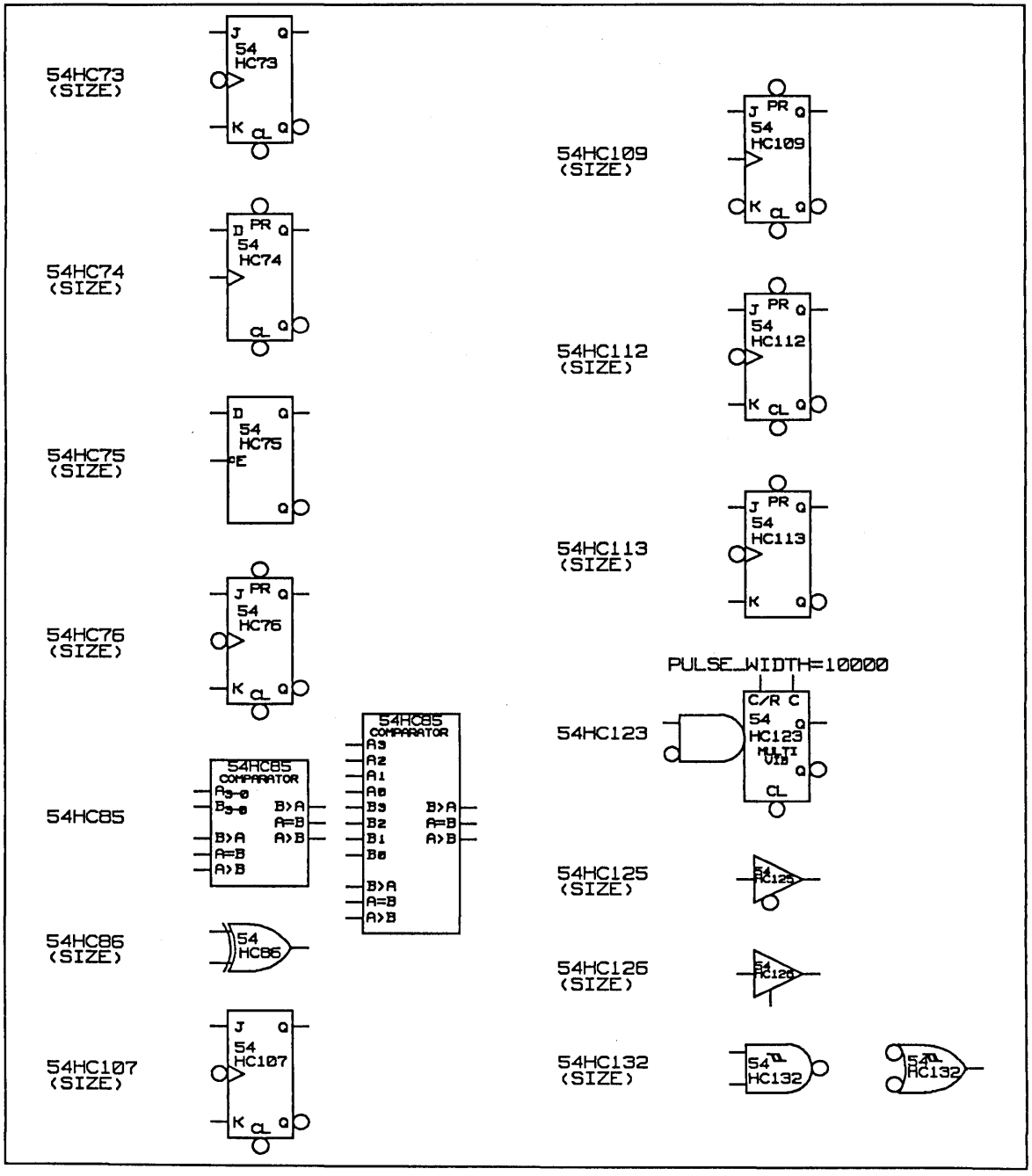
typical delay (50pF) = 18
maximum delay (50pF) = 35
typical drive = 0.13

54HC74 Calculation:

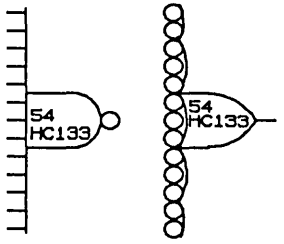
typical delay (no load) = 18 - 0.13 * 50 = 11.5
maximum delay (no load) = 11.5 * 35 / 18 = 22.36
minimum delay (50pF) = 18 / 2 = 9.0
minimum delay (no load) = 11.5 / 2 = 5.75
maximum drive = (35 - 22.36) / 50pF = 0.253
minimum drive = (9.0 - 5.75) / 50pF = 0.065

From these calculations, the min/max delay for the 54HC74 timing model is 5.75/22.36, and the min/max drive for the timing model is 0.065/0.253. The min/typ/max delay for the 54HC74 simulation model is 5.75/11.5/22.36, and the min/typ/max drive for the simulation model is 0.065/0.13/0.253.

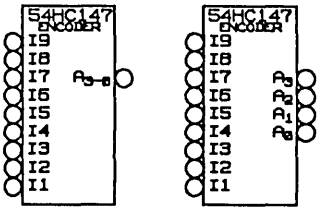

54HC00 (SIZE)
54HCT00 (SIZE)
54HC02 (SIZE)
54HCT02 (SIZE)
54HCT04 (SIZE)
54HCU04 (SIZE)
MAX_DELAY=10000
MAX_DELAY=10000
54HC03 (SIZE)
54HC04 (SIZE)
54HC08 (SIZE)
54HC10 (SIZE)
54HC11 (SIZE)
54HC14 (SIZE)
54HC20 (SIZE)
54HC27 (SIZE)
54HC30 (SIZE)
54HC32 (SIZE)
54HCT32 (SIZE)
54HC42
54HC51 (SIZE)
54HC58 (SIZE)


54HC73
(SIZE)
J
Q
54
HC73
K
CL
Q
54HC74
(SIZE)
D
PR
Q
54
HC74
CL
Q
54HC75
(SIZE)
D
Q
54
HC75
E
Q
54HC76
(SIZE)
J
PR
Q
54
HC76
K
CL
Q
54HC85
54HC85
COMPARATOR
A3-0
B3-0
B>A
A=B
A>B
B>A
A=B
A>B
54HC85
COMPARATOR
A3
A2
A1
A0
B3
B2
B1
B0
B>A
A=B
A>B
B>A
A=B
A>B
54HC86
(SIZE)
54
HC86
54HC107
(SIZE)
J
Q
54
HC107
K
CL
Q
54HC109
(SIZE)
J
PR
Q
54
HC109
K
CL
Q
54HC112
(SIZE)
J
PR
Q
54
HC112
K
CL
Q
54HC113
(SIZE)
J
PR
Q
54
HC113
K
Q
PULSE_WIDTH=10000
54HC123
C/R
C
54
HC123
MULTI
VIB
Q
CL
54HC125
(SIZE)
54
HC125
54HC126
(SIZE)
54
HC126
54HC132
(SIZE)
54
HC132
54
HC132

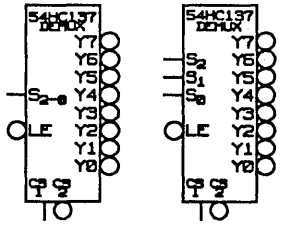
54HC133
(SIZE)



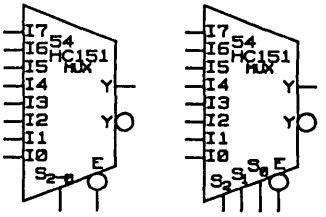
54HC147



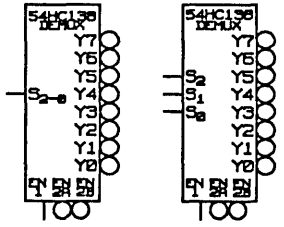
54HC137



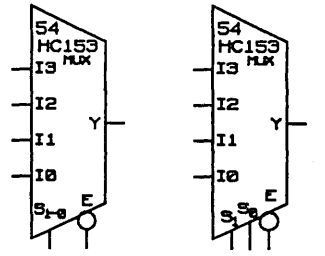
54HC151
(SIZE)



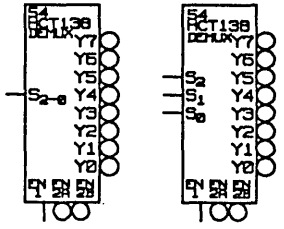
54HC138



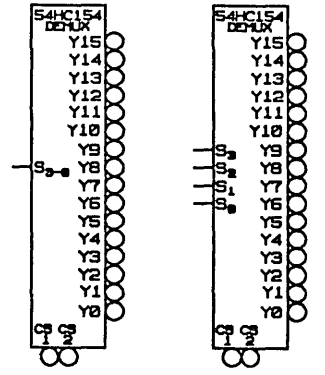
54HC153
(SIZE)



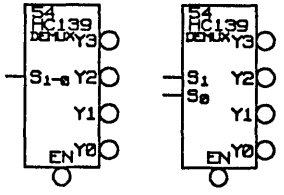
54HCT138

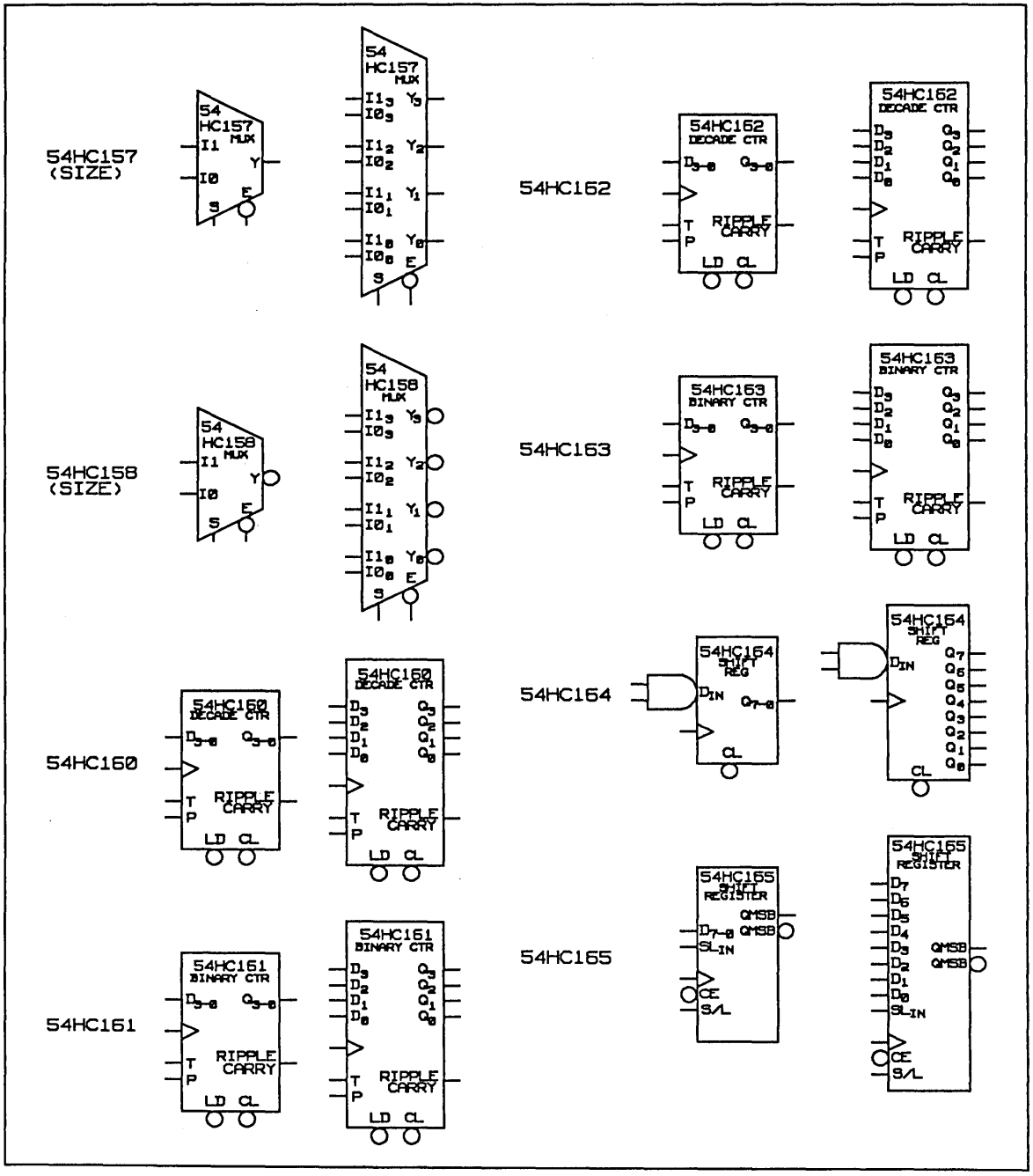


54HC154

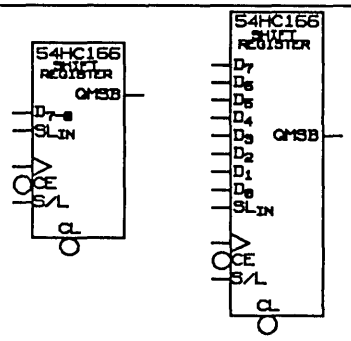


54HC139

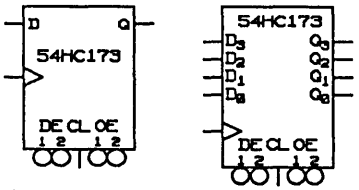



54HC157 (SIZE)
54HC158 (SIZE)
54HC160
54HC161
54HC162
54HC163
54HC164
54HC165
MUX
DECADE CTR
BINARY CTR
SHIFT REG
SHIFT REGISTER
RIPPLE CARRY
LD
CL

54HC166



54HC173 (SIZE)



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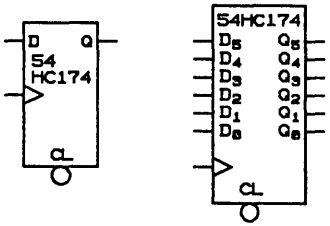
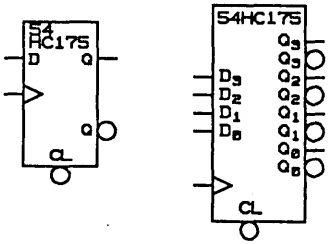
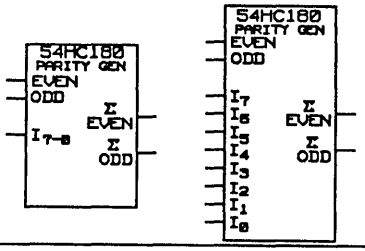


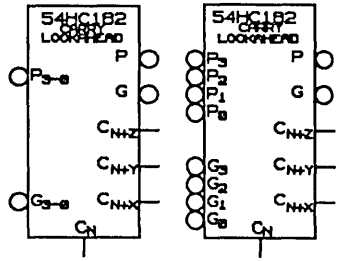
54HC175 (SIZE)



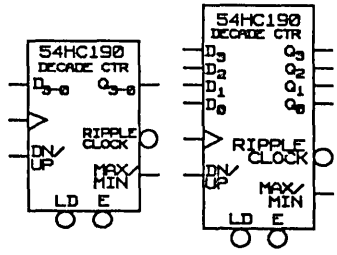
54HC180



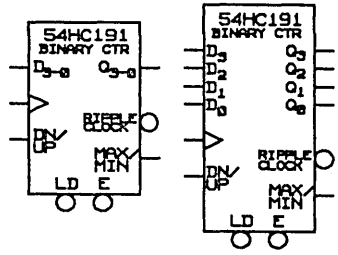
54HC182



54HC190



54HC191



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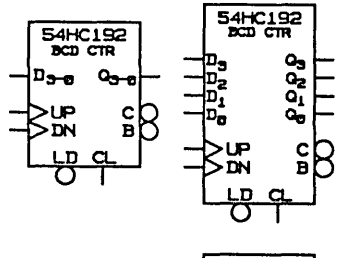

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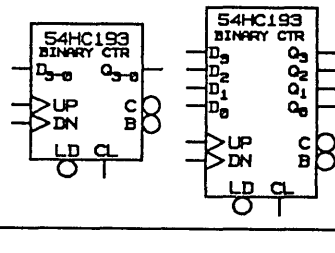

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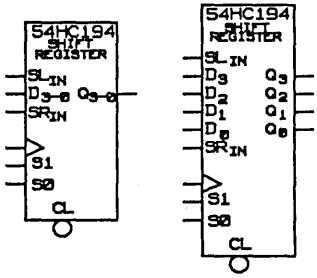

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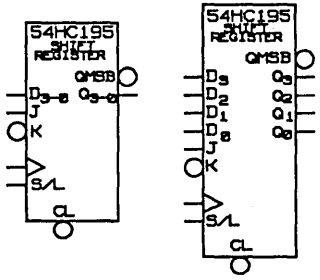

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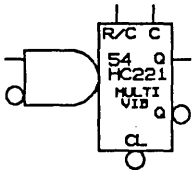

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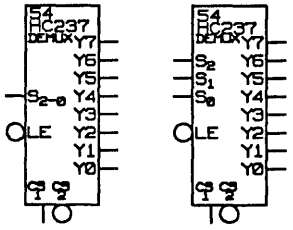

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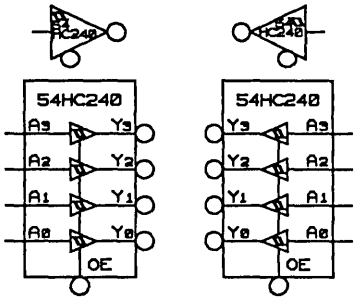

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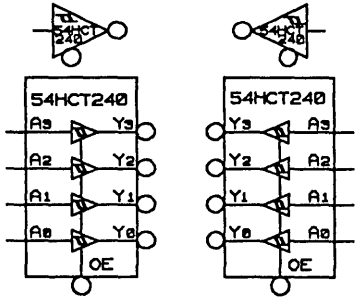

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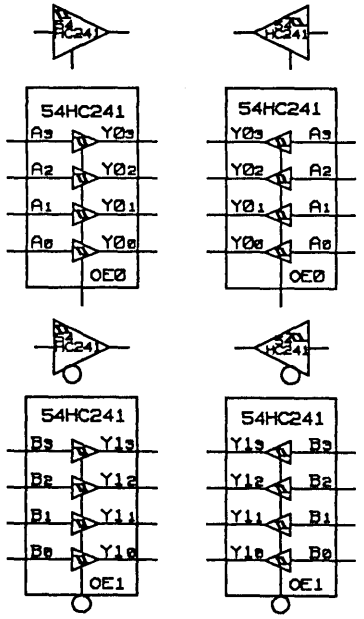

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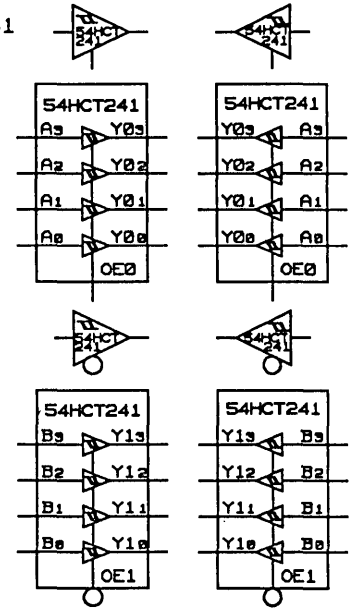

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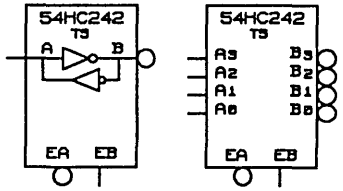

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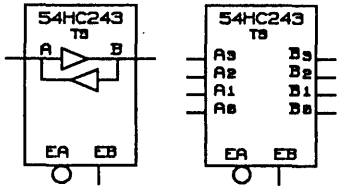

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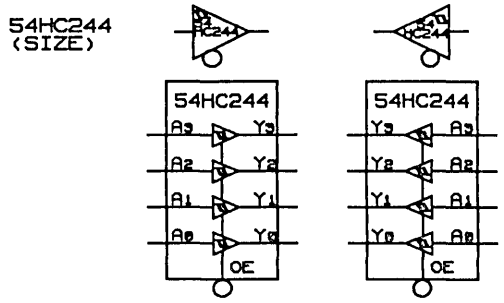

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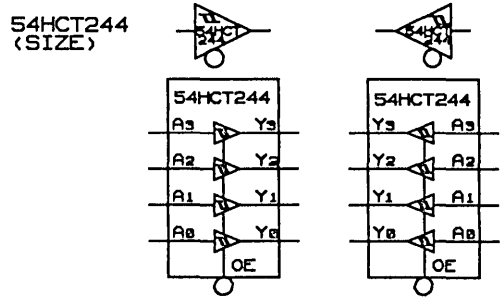

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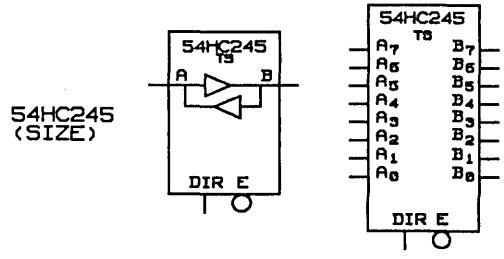

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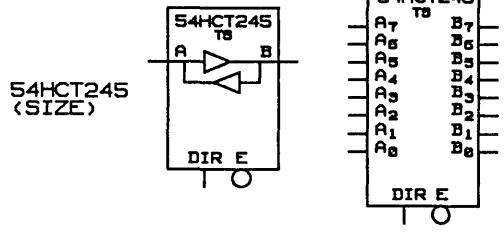

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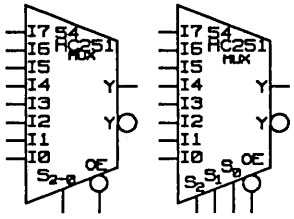

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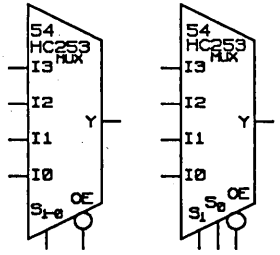

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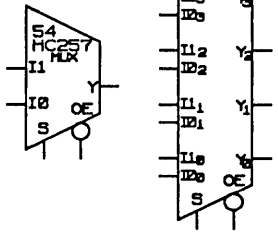

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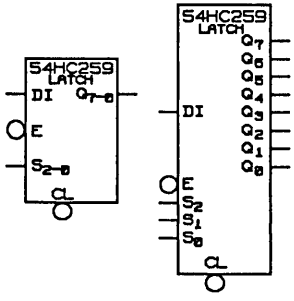

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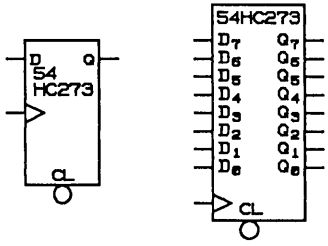

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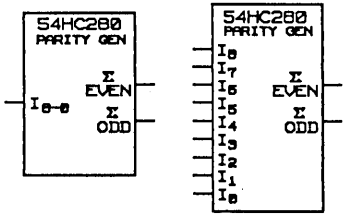

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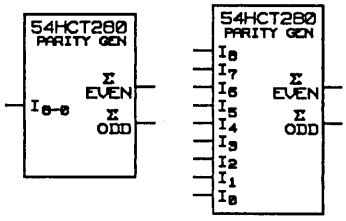

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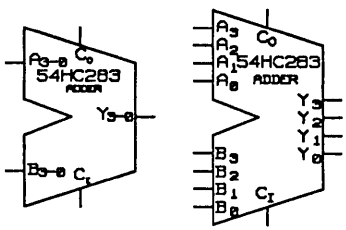

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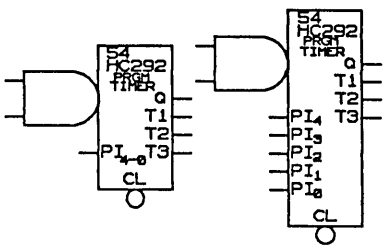

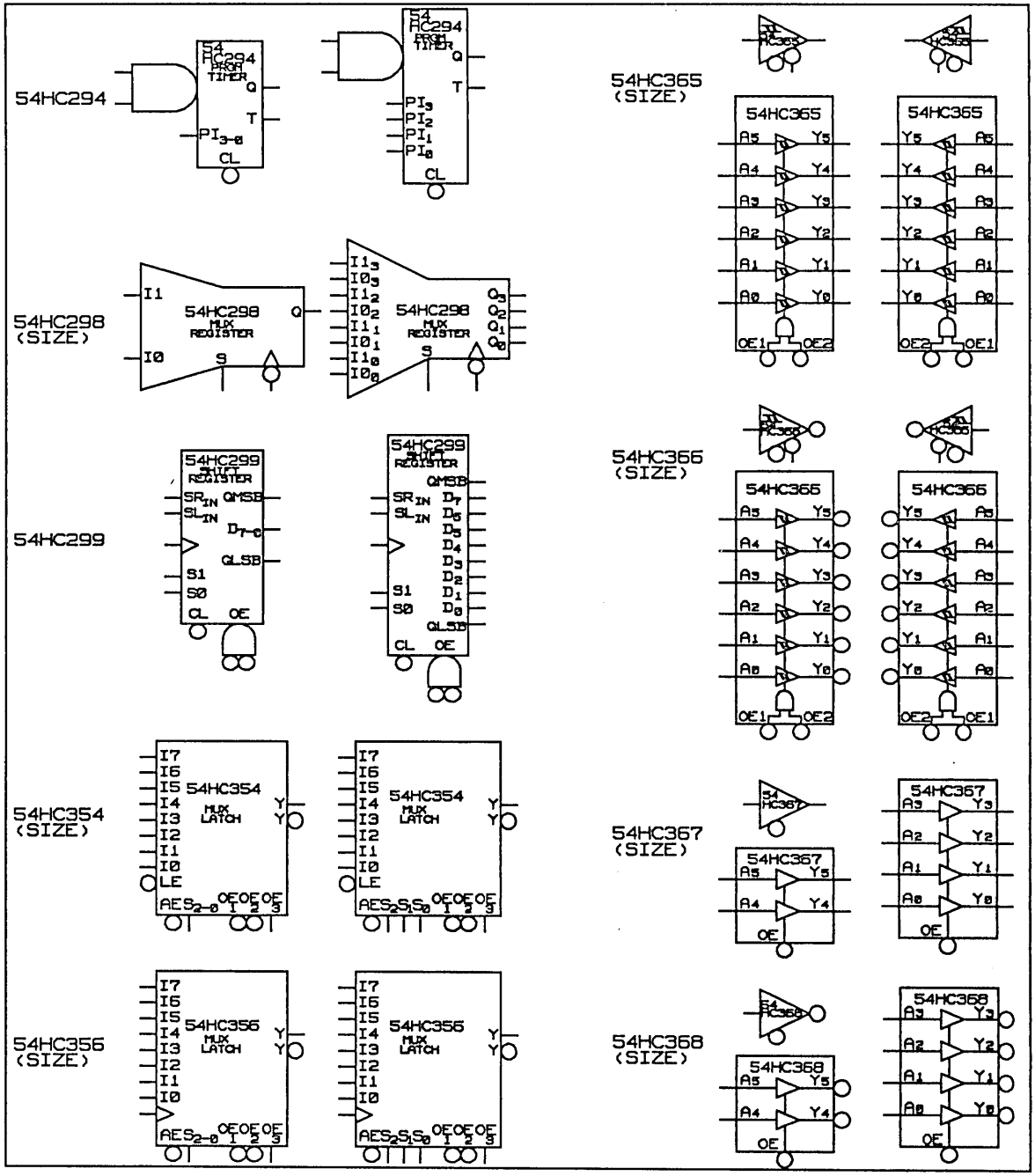
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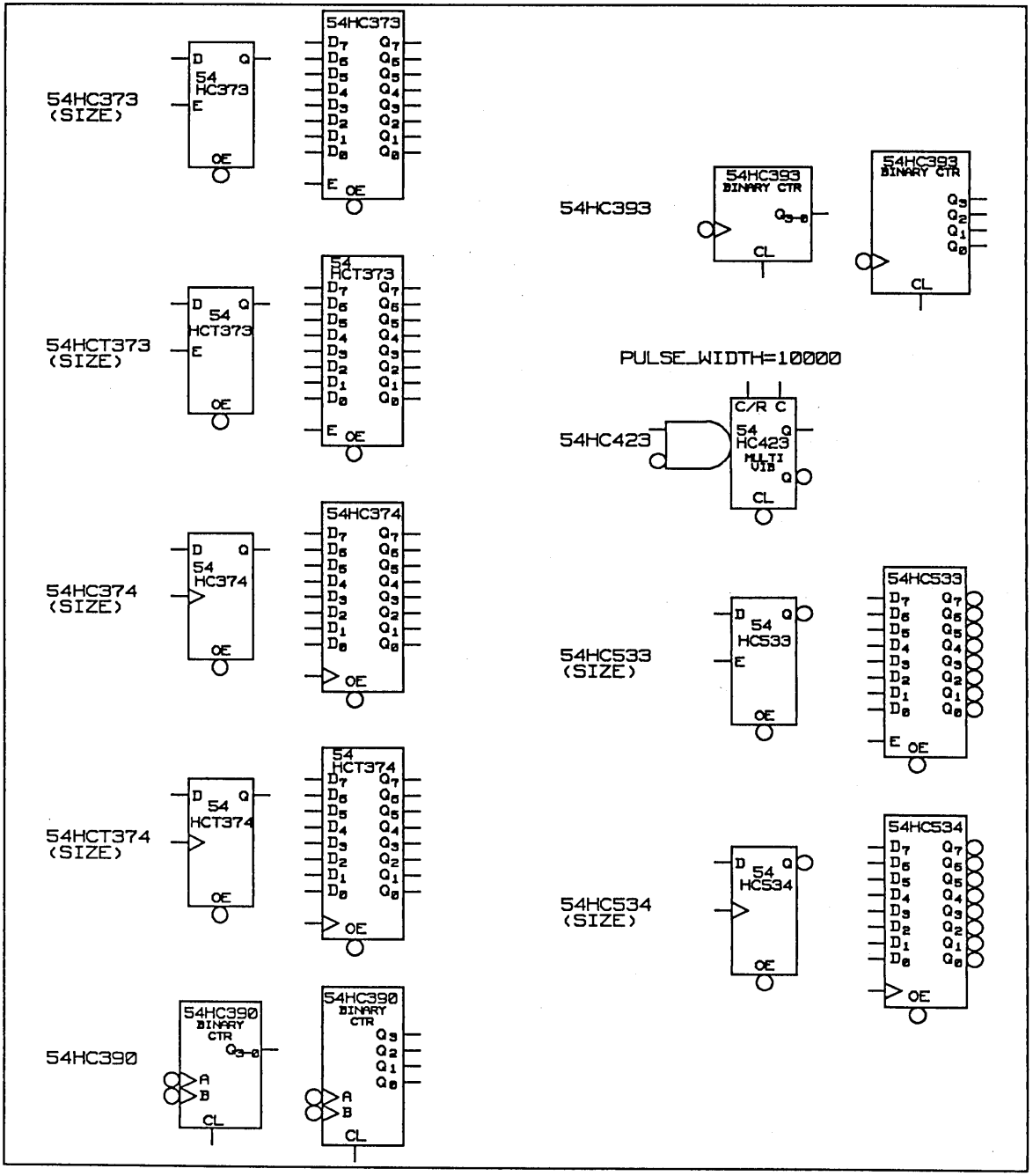
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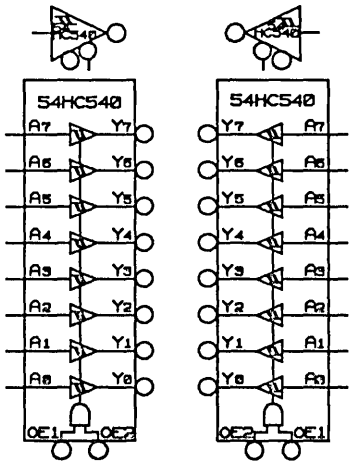

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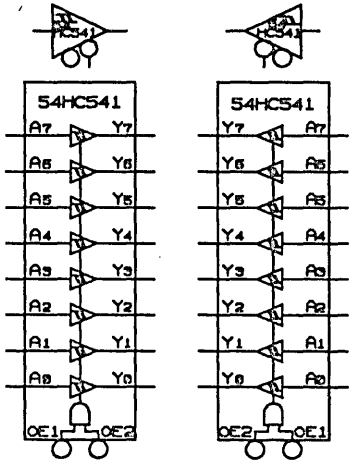

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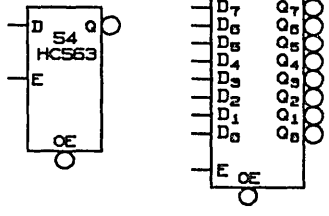

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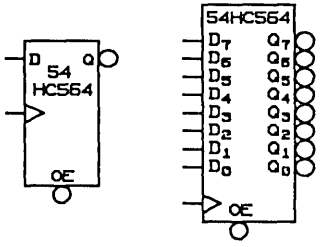

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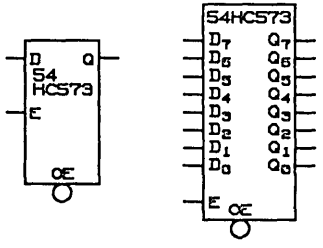

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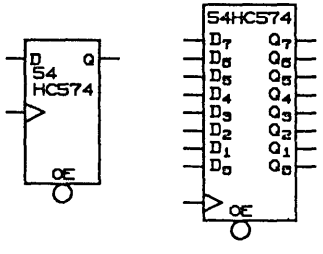

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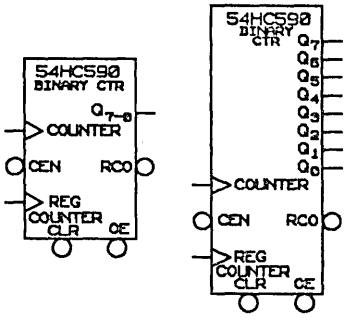

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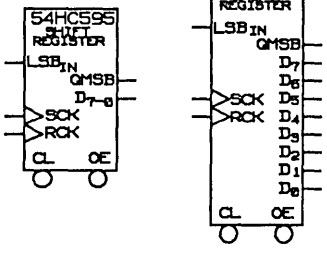

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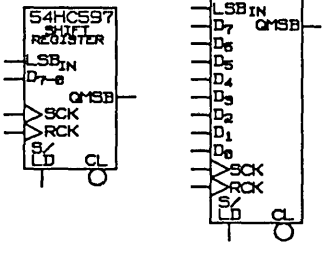

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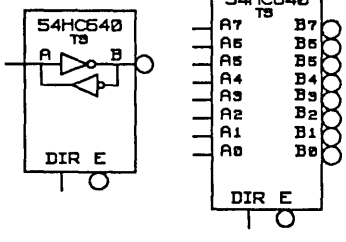

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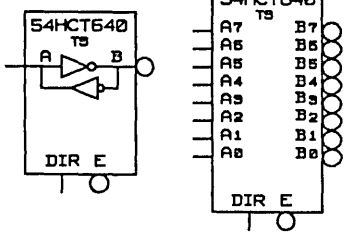

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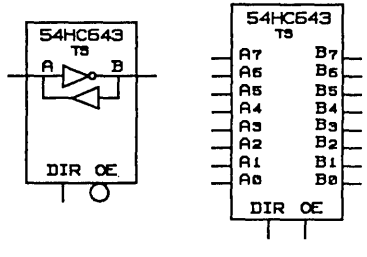

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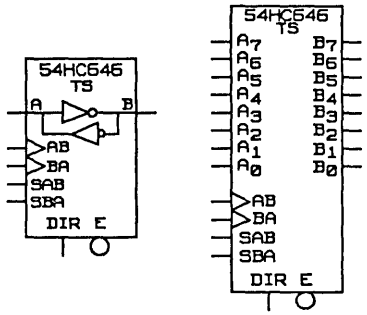

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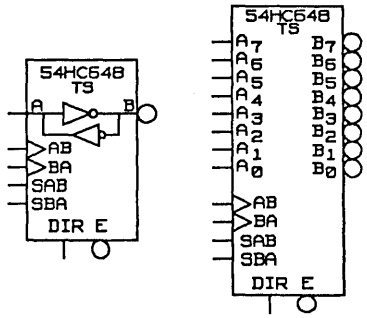

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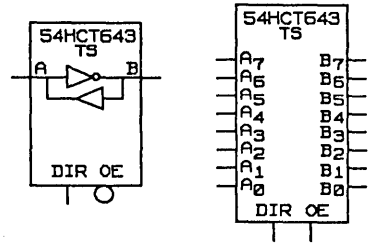

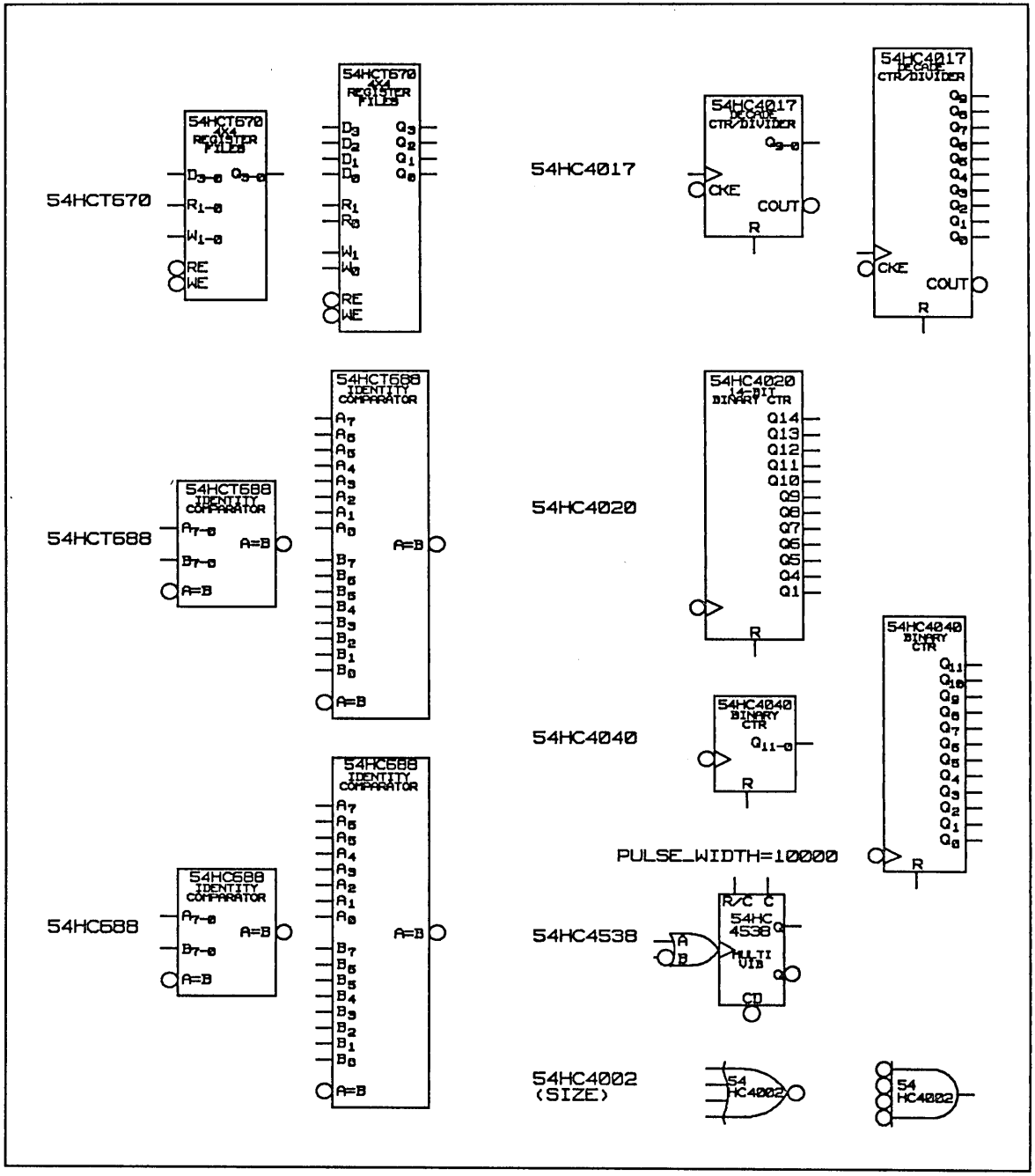
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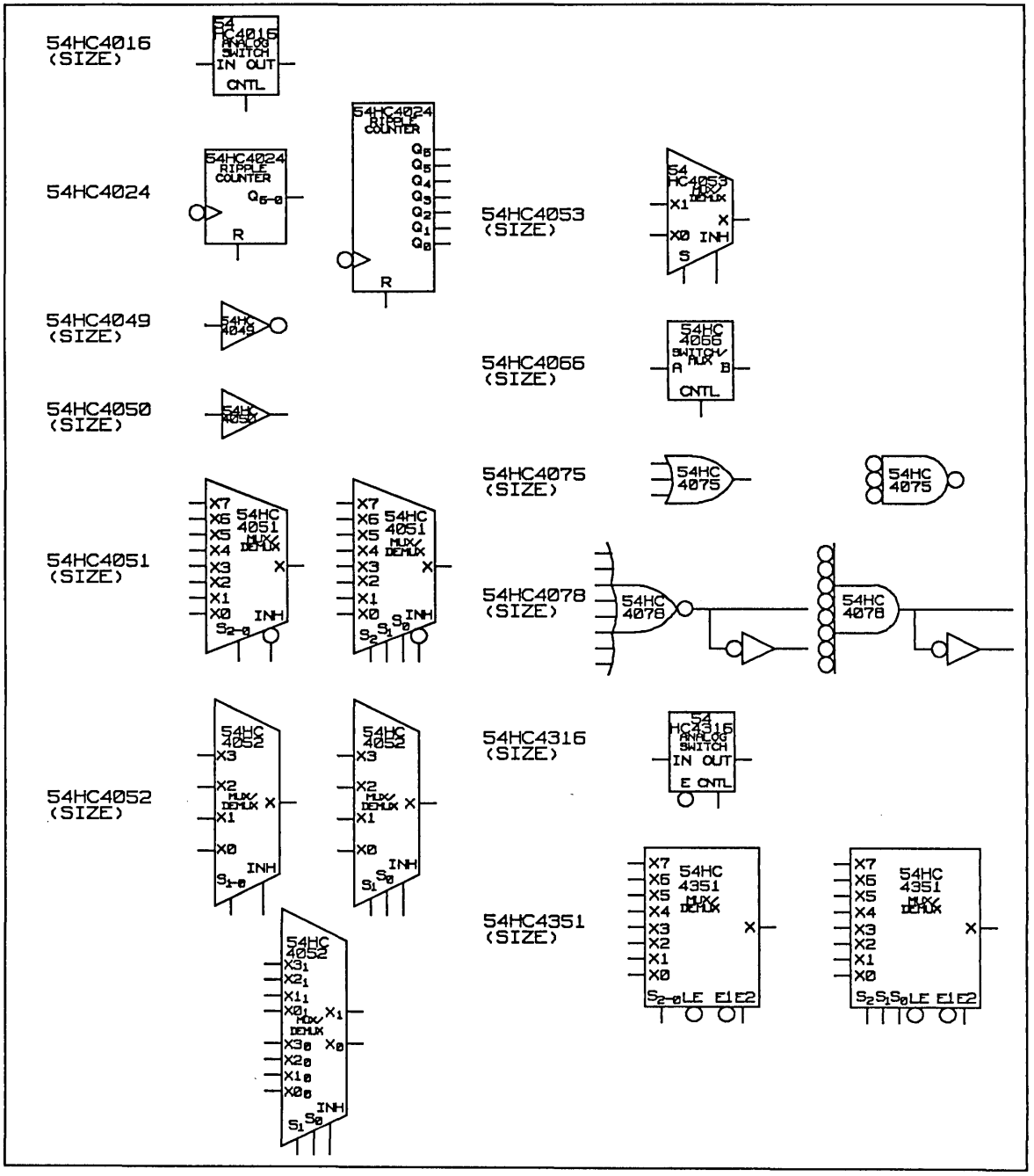
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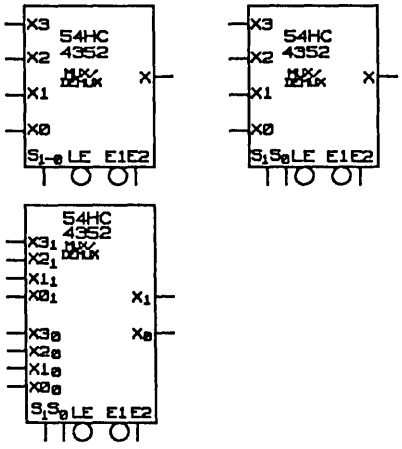

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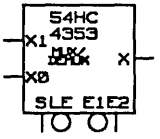
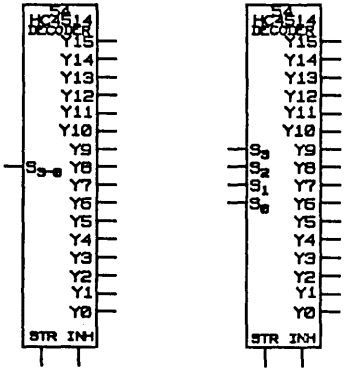
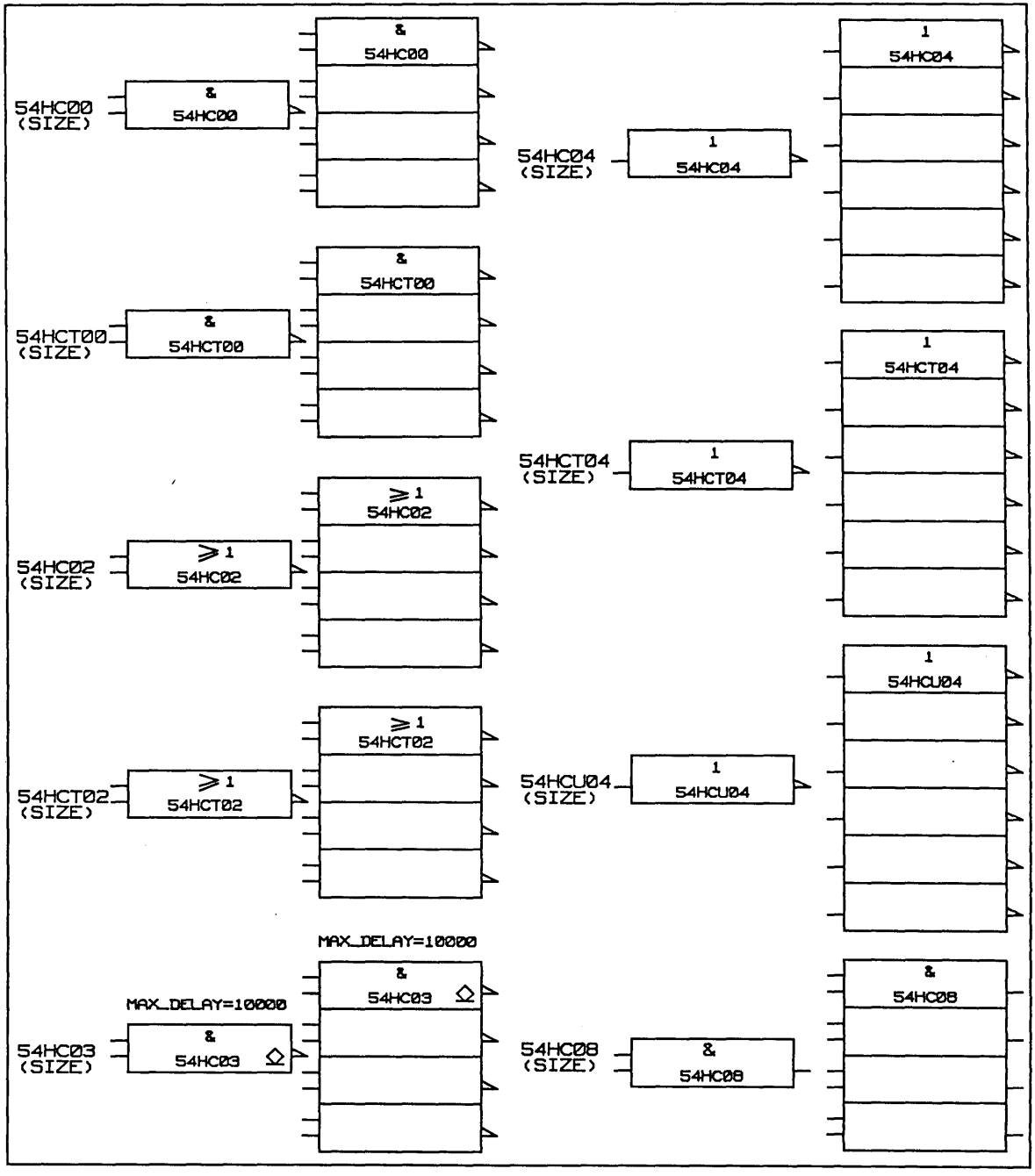
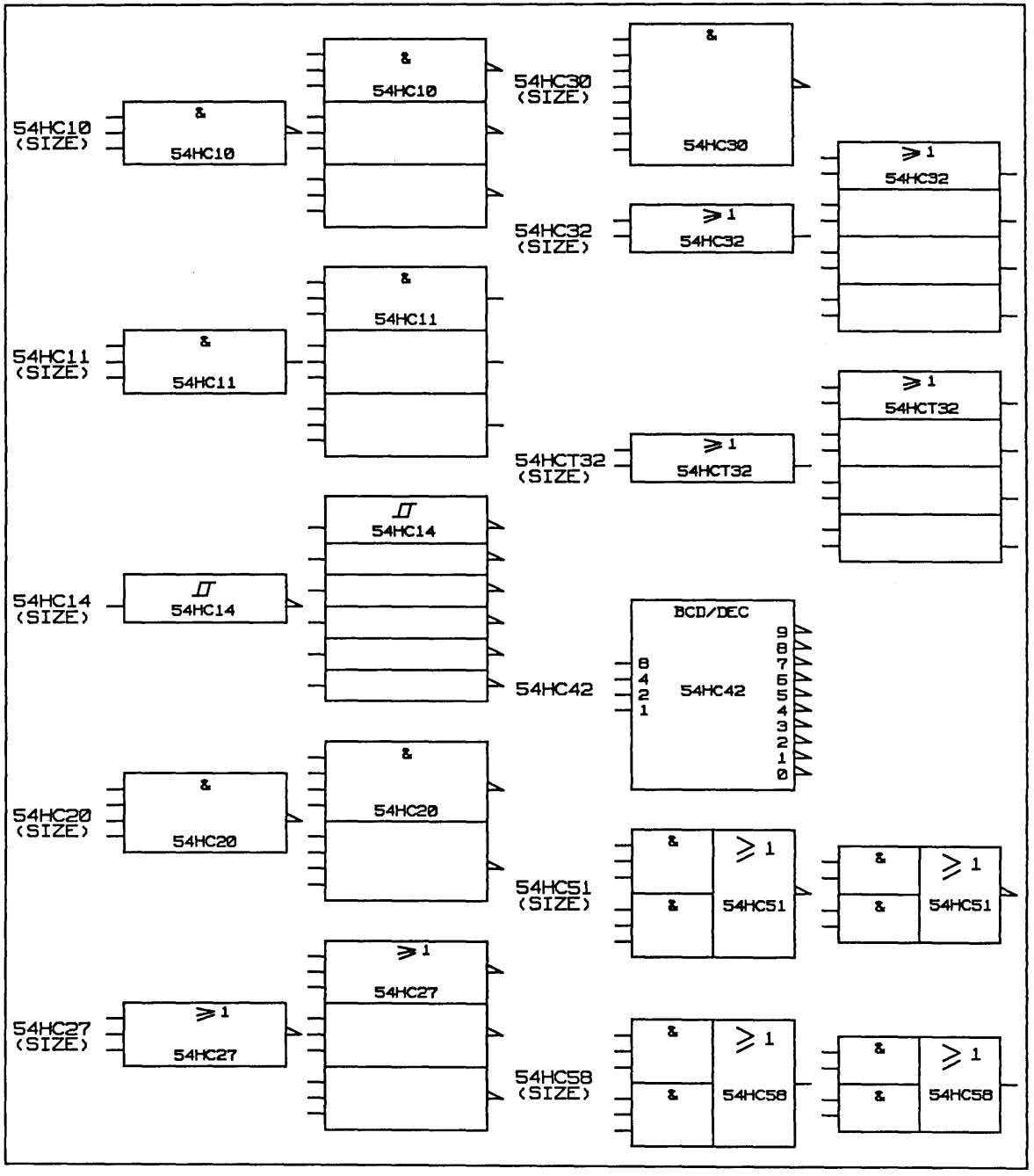
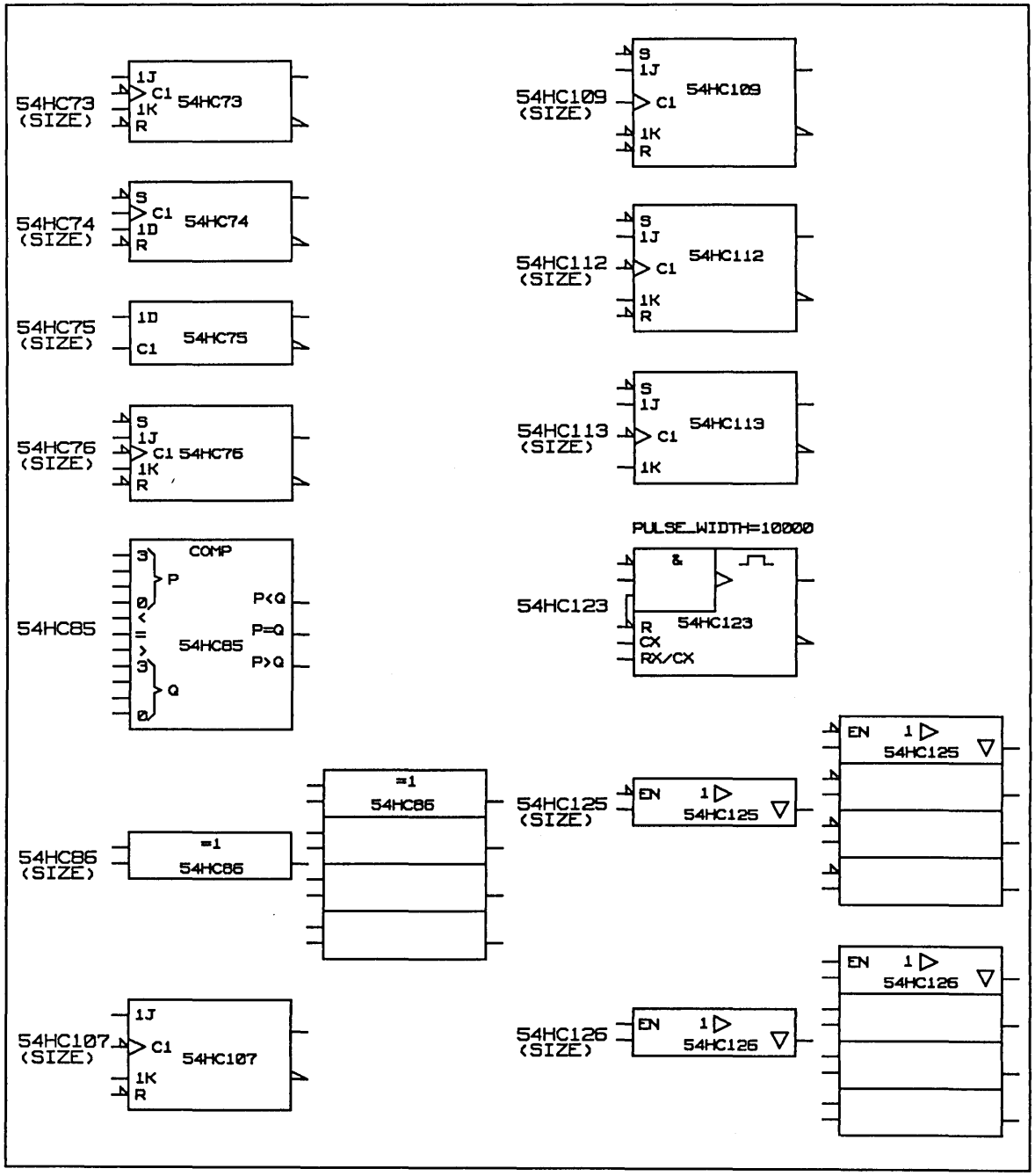


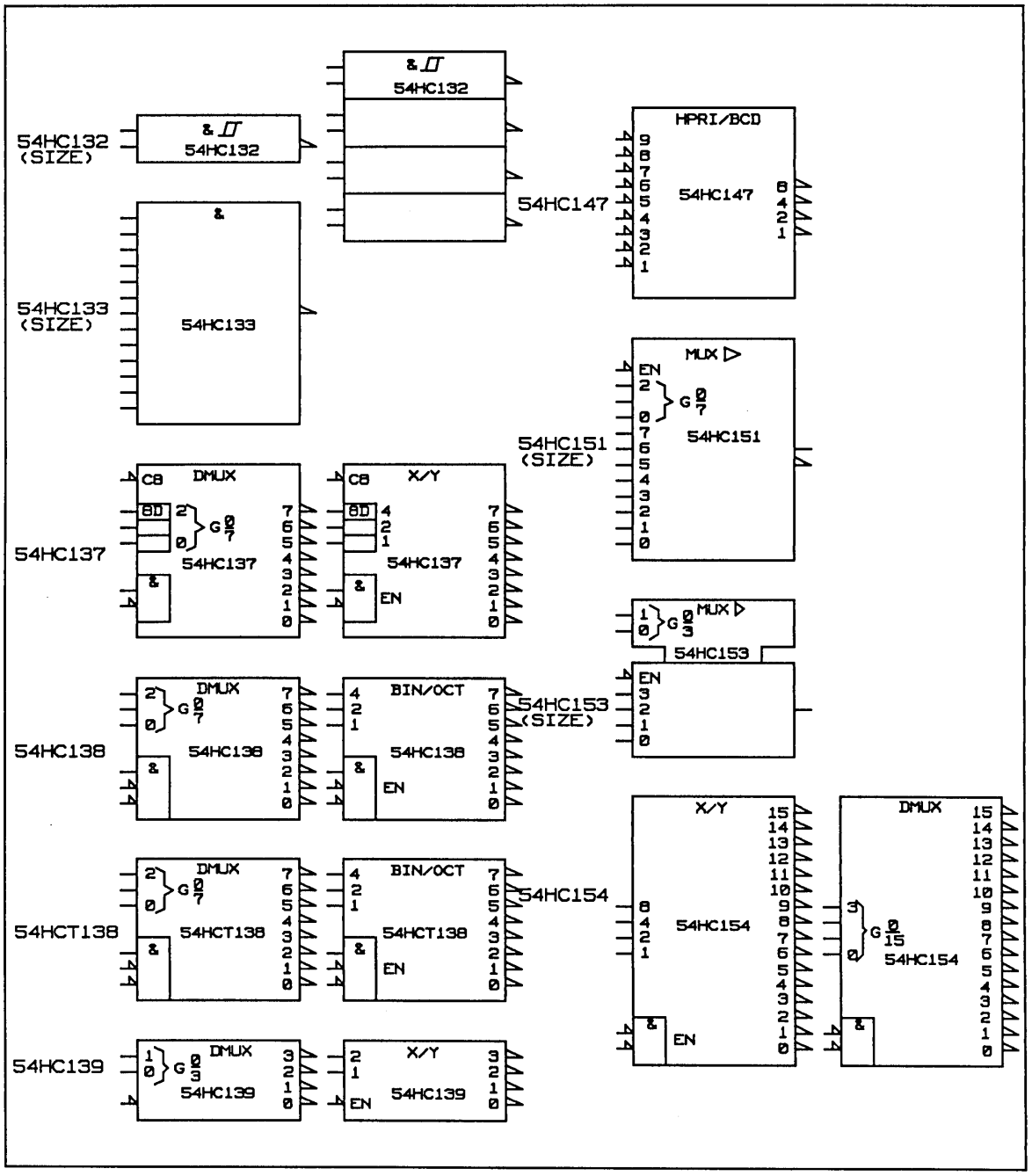
54HC4514

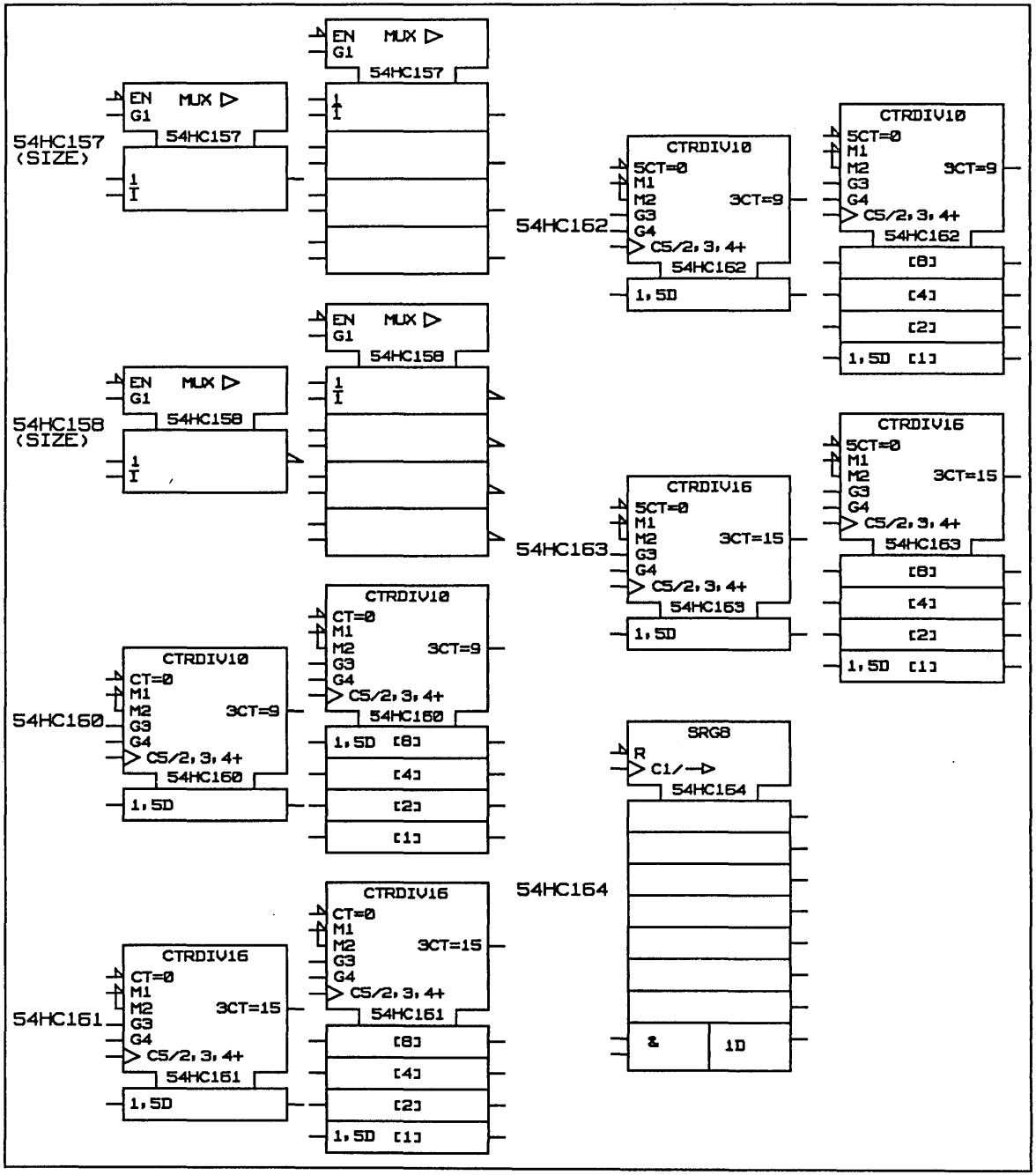


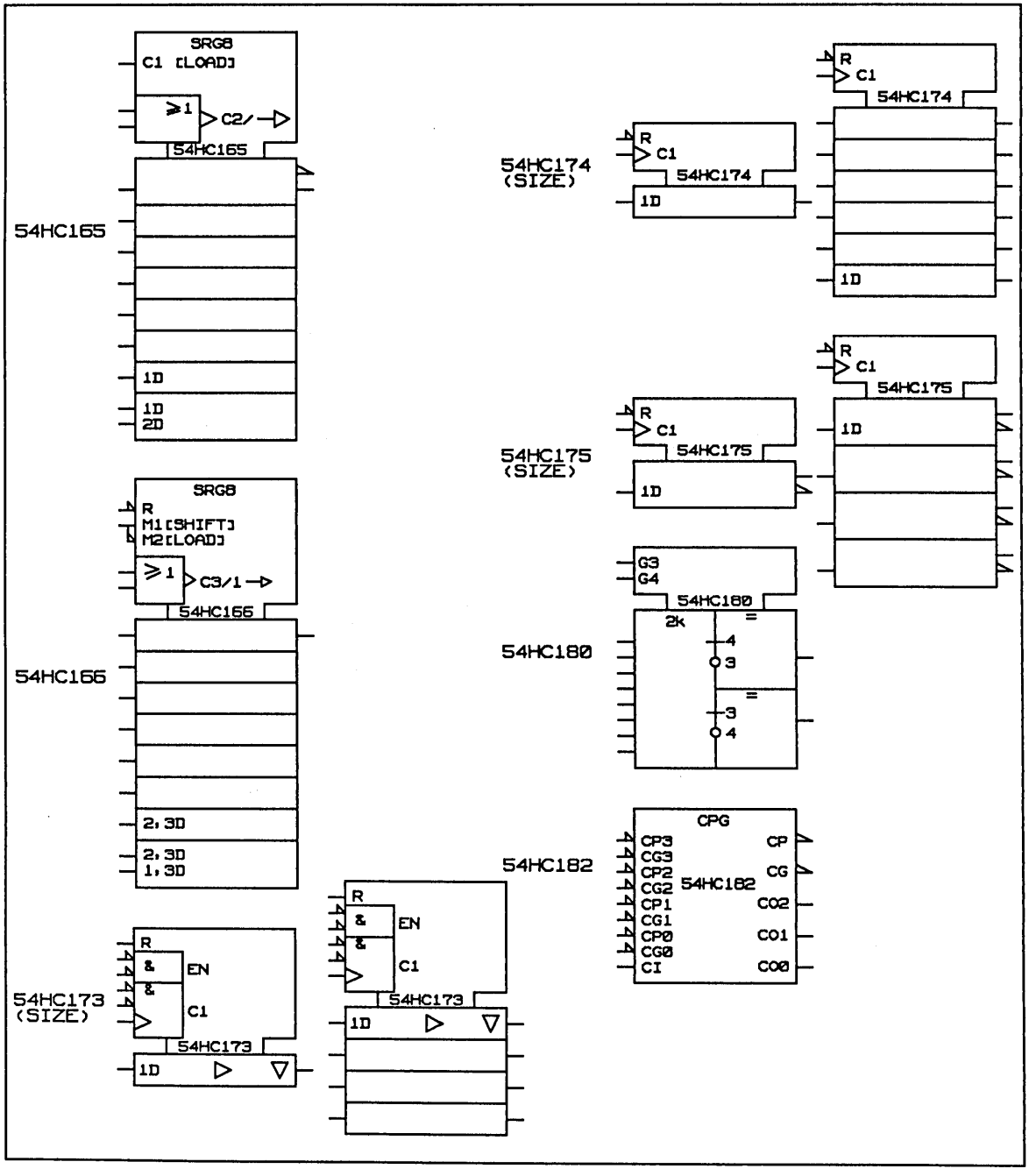

&
54HC00
54HC00
(SIZE)
&
54HC00
&
54HCT00
54HCT00
(SIZE)
&
54HCT00
≥1
54HC02
54HC02
(SIZE)
≥1
54HC02
≥1
54HCT02
54HCT02
(SIZE)
≥1
54HCT02
MAX_DELAY=10000
MAX_DELAY=10000
&
54HC03
54HC03
(SIZE)
&
54HC03
1
54HC04
54HC04
(SIZE)
1
54HC04
1
54HCT04
54HCT04
(SIZE)
1
54HCT04
1
54HCU04
54HCU04
(SIZE)
1
54HCU04
&
54HC08
54HC08
(SIZE)
&
54HC08

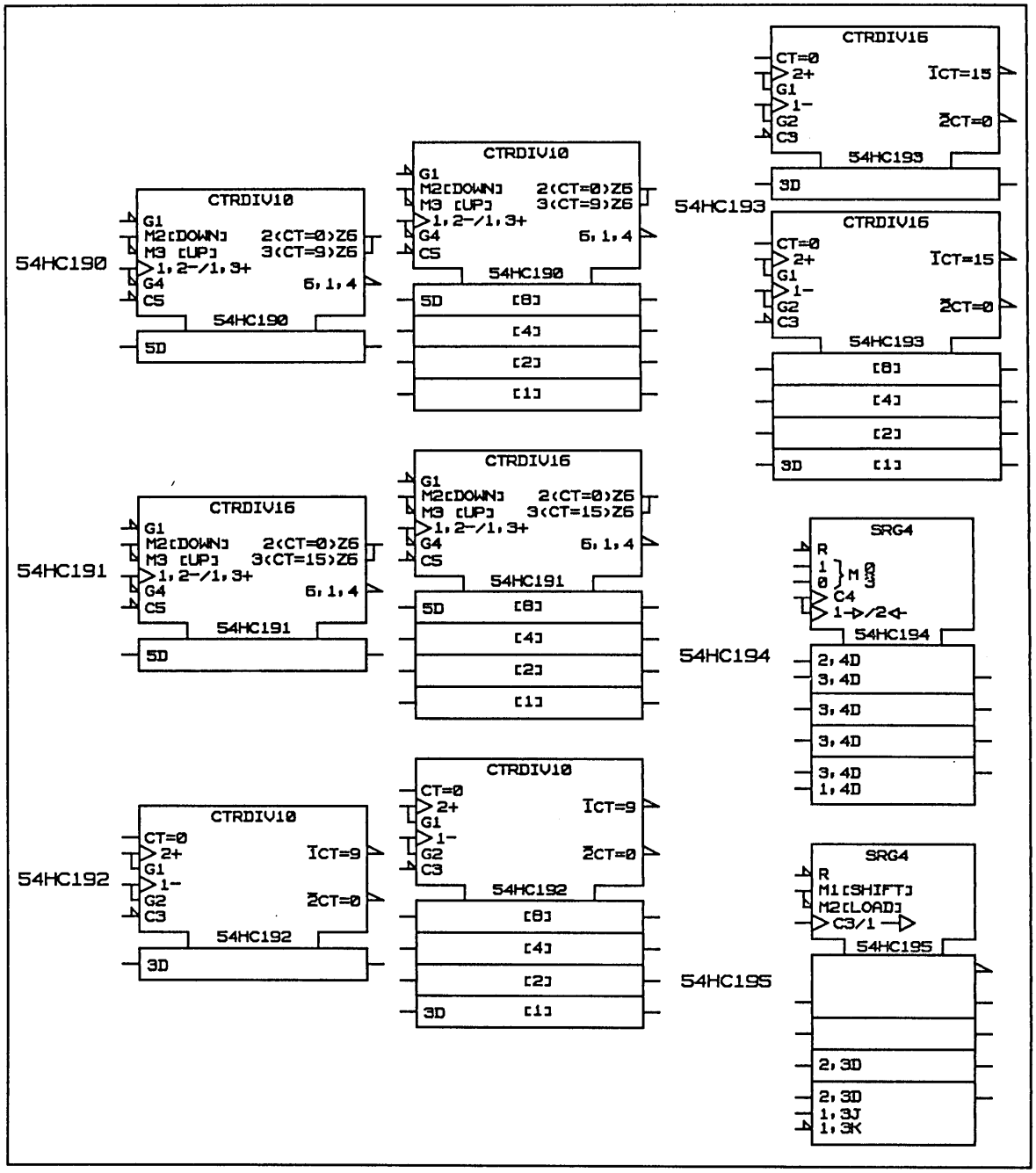

54HC10
(SIZE)
&
54HC10
54HC11
(SIZE)
&
54HC11
54HC14
(SIZE)
54HC14
54HC20
(SIZE)
&
54HC20
54HC27
(SIZE)
≥1
54HC27
54HC30
(SIZE)
&
54HC30
54HC32
(SIZE)
≥1
54HC32
54HCT32
(SIZE)
≥1
54HCT32
54HC42
BCD/DEC
8
4
2
1
54HC42
9
8
7
6
5
4
3
2
1
0
54HC51
(SIZE)
&
&
≥1
54HC51
54HC58
(SIZE)
&
&
≥1
54HC58

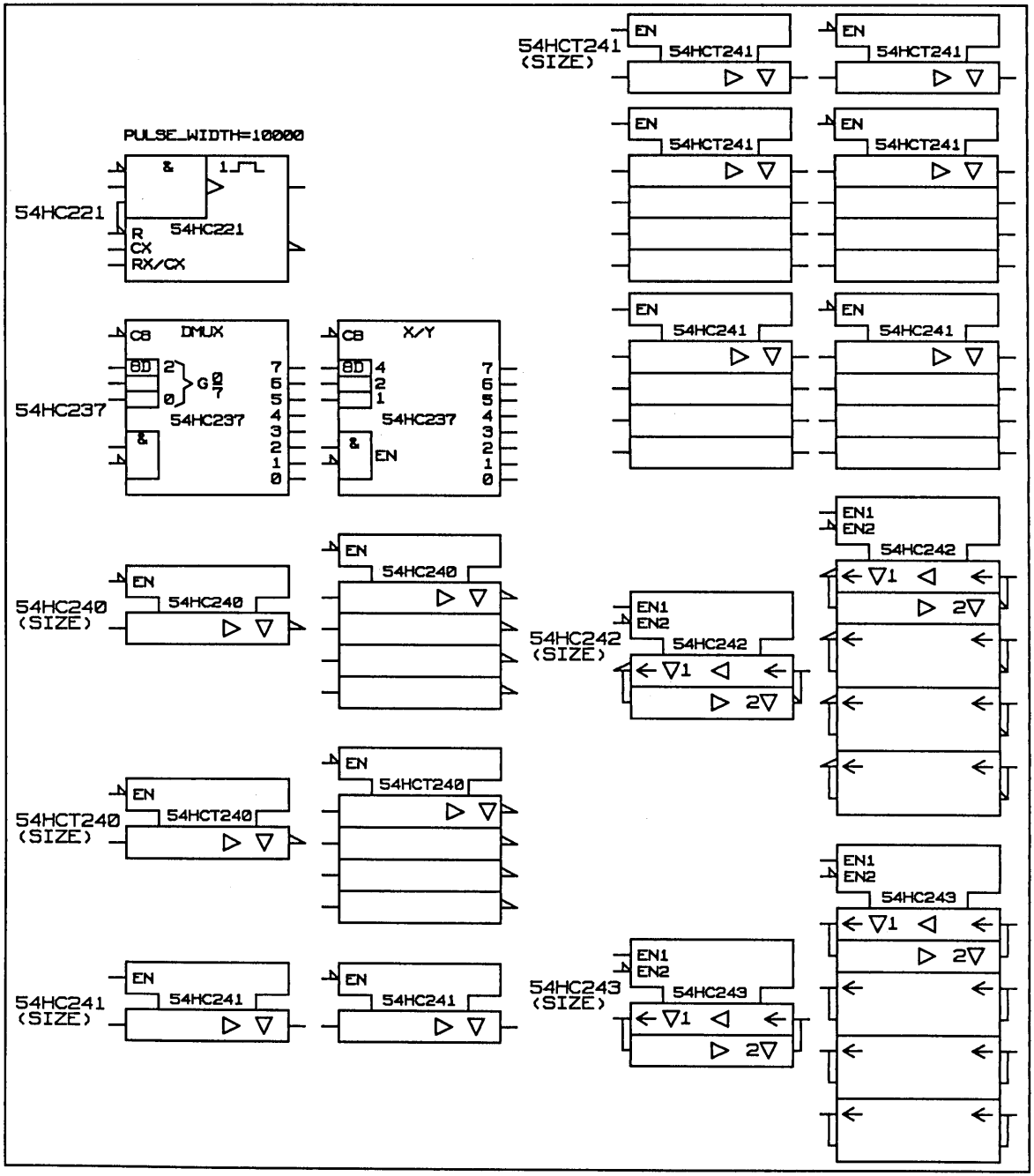

54HC73
(SIZE)
1J
C1
1K
R
54HC73
54HC74
(SIZE)
S
C1
1D
R
54HC74
54HC75
(SIZE)
1D
C1
54HC75
54HC76
(SIZE)
S
1J
C1
1K
R
54HC76
54HC85
COMP
P
P<Q
P=Q
P>Q
Q
54HC85
54HC86
(SIZE)
=1
54HC86
54HC107
(SIZE)
1J
C1
1K
R
54HC107
54HC109
(SIZE)
S
1J
C1
1K
R
54HC109
54HC112
(SIZE)
S
1J
C1
1K
R
54HC112
54HC113
(SIZE)
S
1J
C1
1K
54HC113
PULSE_WIDTH=10000
54HC123
&
R
CX
RX/CX
54HC123
54HC125
(SIZE)
EN
1
54HC125
54HC126
(SIZE)
EN
1
54HC126

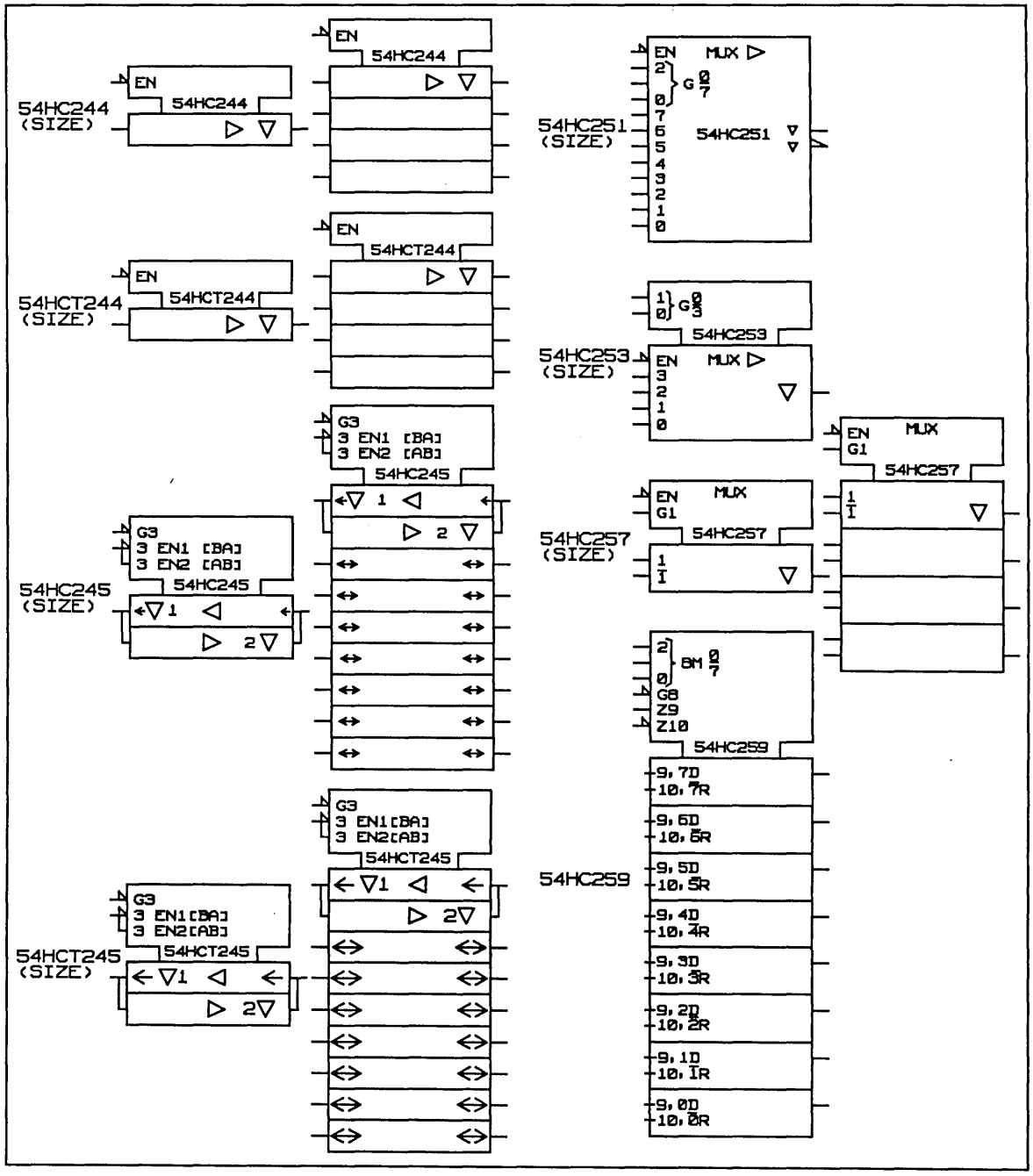

54HC132
(SIZE)
54HC132
54HC133
(SIZE)
54HC133
54HC137
54HC138
54HCT138
54HC139
54HC147
54HC151
(SIZE)
54HC153
(SIZE)
54HC154
HPRI/BCD
54HC147
MUX
54HC151
DMUX
54HC137
X/Y
54HC137
DMUX
54HC138
BIN/OCT
54HC138
DMUX
54HCT138
BIN/OCT
54HCT138
DMUX
54HC139
X/Y
54HC139
MUX
54HC153
X/Y
54HC154
DMUX
54HC154

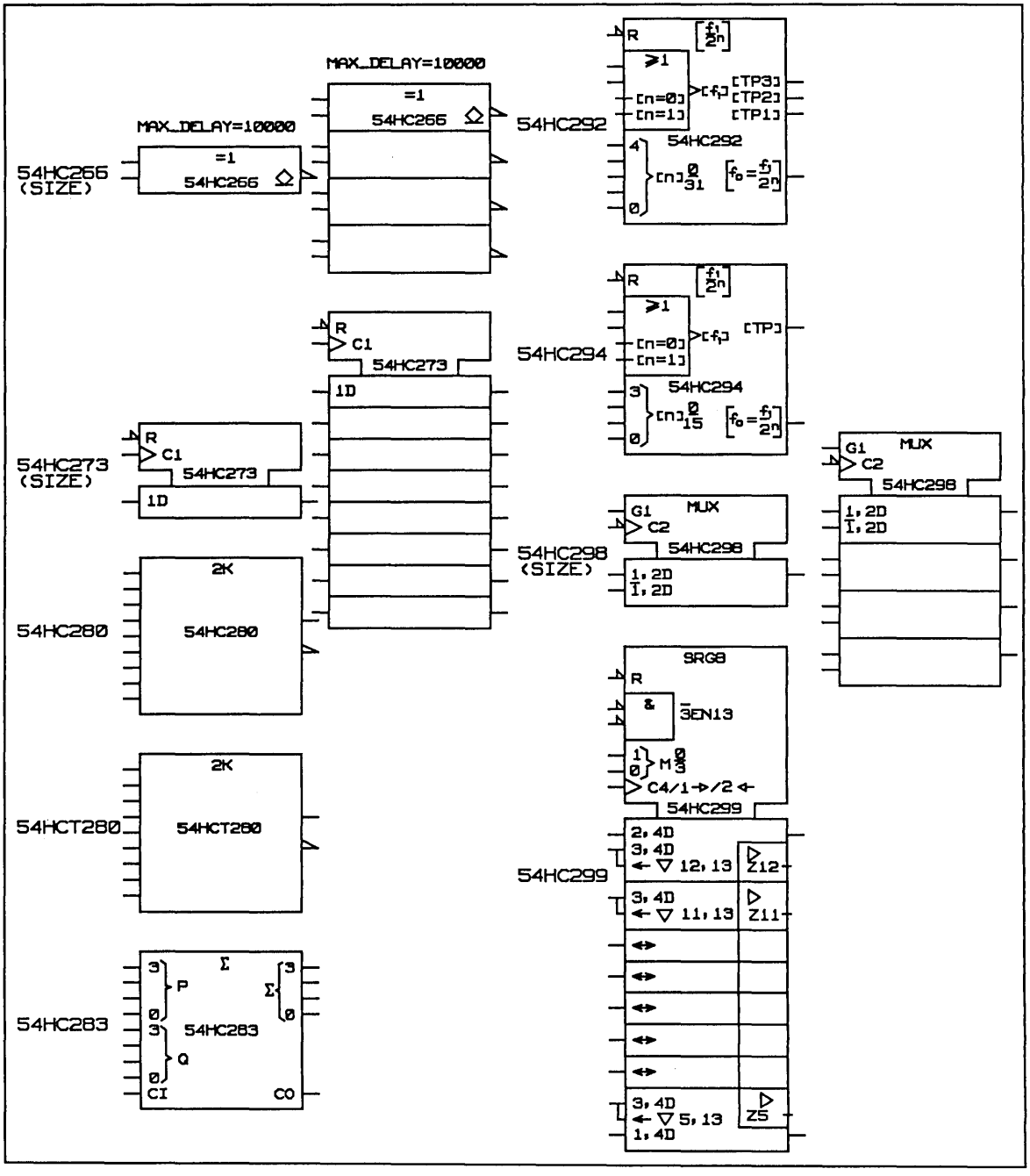

54HC157
(SIZE)
EN
G1
MUX
54HC157
1
I
54HC158
(SIZE)
54HC158
54HC160
CTRDIV10
CT=0
M1
M2
G3
G4
3CT=9
C5/2,3,4+
1,5D
[8]
[4]
[2]
[1]
54HC161
CTRDIV16
3CT=15
54HC162
5CT=0
54HC163
54HC164
SRG8
R
C1/→
&
1D

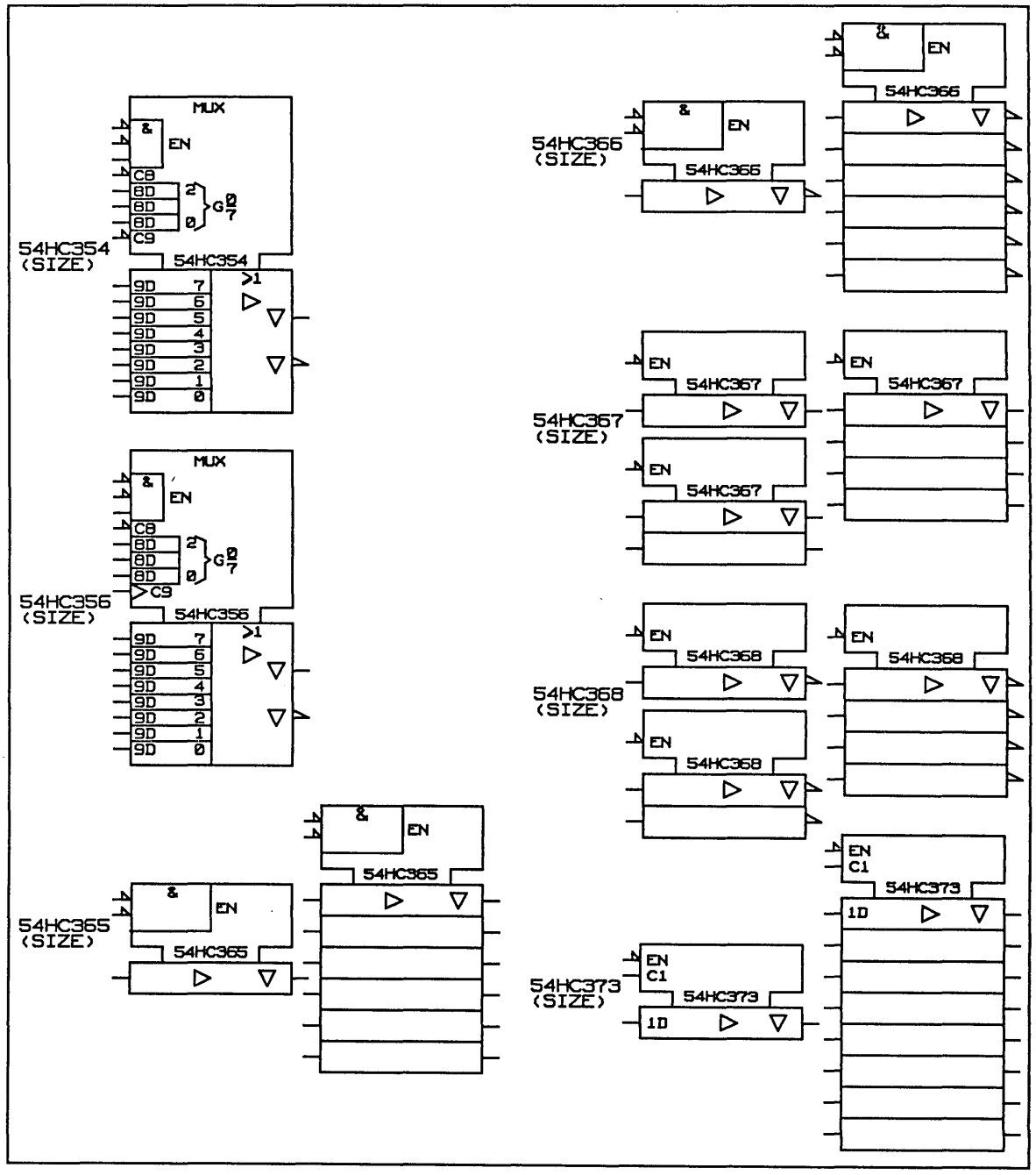

SRG8
C1 [LOAD]
≥1
C2/
54HC165
1D
1D
2D
54HC165
SRG8
R
M1 [SHIFT]
M2 [LOAD]
≥1
C3/1
54HC166
2,3D
2,3D
1,3D
54HC166
R
&
EN
C1
54HC173
1D
54HC173
(SIZE)
R
&
EN
C1
54HC173
1D
54HC182
R
C1
54HC174
1D
54HC174
(SIZE)
R
C1
54HC174
1D
R
C1
54HC175
1D
54HC175
(SIZE)
R
C1
54HC175
1D
G3
G4
54HC180
2k
=
4
3
=
3
4
54HC180
CPG
CP3
CG3
CP2
CG2
CP1
CG1
CP0
CG0
CI
54HC182
CP
CG
CO2
CO1
CO0

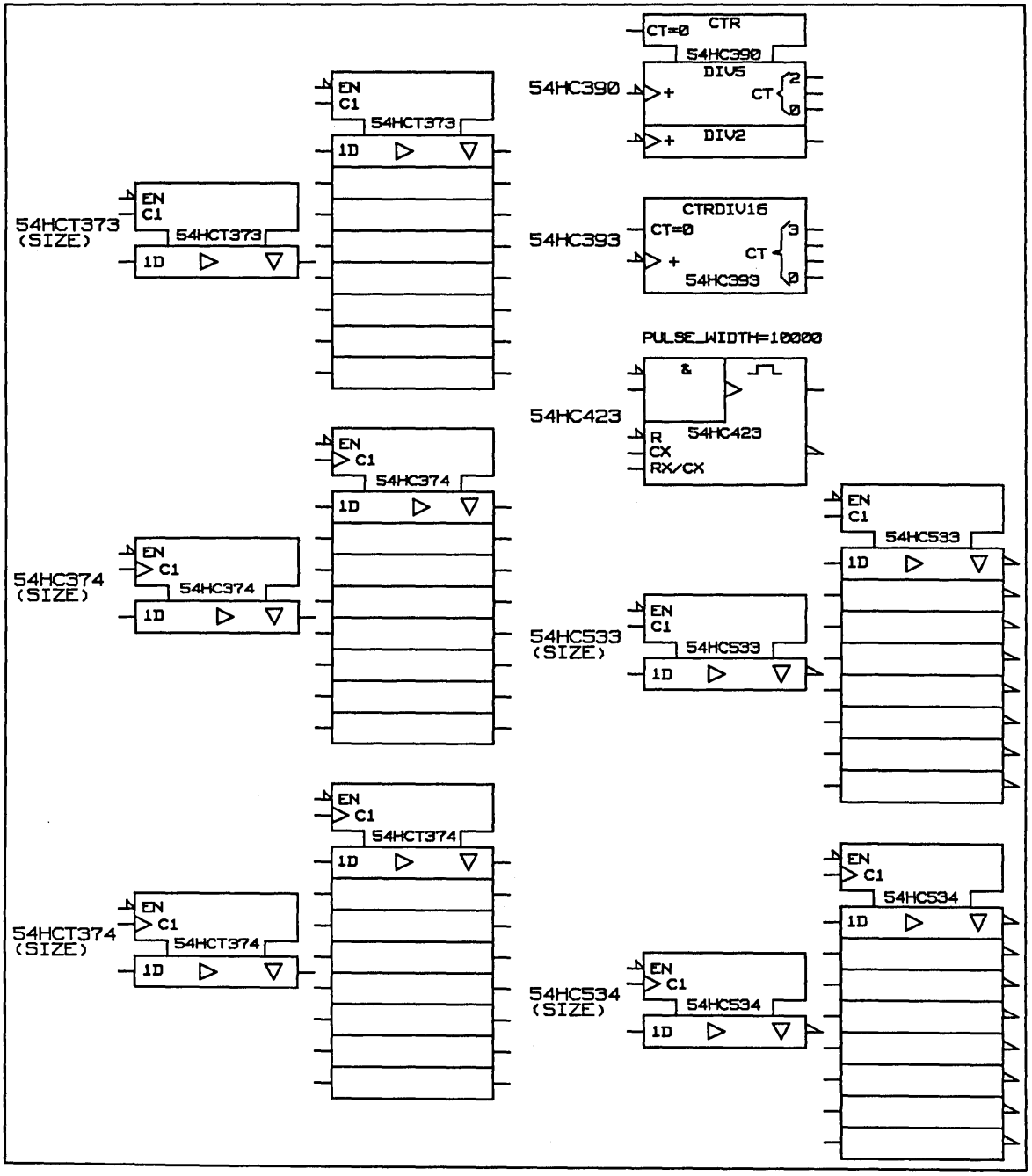

54HC190
CTRDIV10
G1
M2[DOWN] 2(CT=0)Z6
M3 [UP] 3(CT=9)Z6
1,2-/1,3+
G4 6,1,4
CS
54HC190
5D
CTRDIV10
G1
M2[DOWN] 2(CT=0)Z6
M3 [UP] 3(CT=9)Z6
1,2-/1,3+
G4 6,1,4
CS
54HC190
5D [8]
[4]
[2]
[1]
54HC193
CTRDIV16
CT=0
2+
G1
1-
G2
C3
ICT=15
ZCT=0
54HC193
3D
54HC193
CTRDIV16
CT=0
2+
G1
1-
G2
C3
ICT=15
ZCT=0
54HC193
[8]
[4]
[2]
3D [1]
54HC191
CTRDIV16
G1
M2[DOWN] 2(CT=0)Z6
M3 [UP] 3(CT=15)Z6
1,2-/1,3+
G4 6,1,4
CS
54HC191
5D
CTRDIV16
G1
M2[DOWN] 2(CT=0)Z6
M3 [UP] 3(CT=15)Z6
1,2-/1,3+
G4 6,1,4
CS
54HC191
5D [8]
[4]
[2]
[1]
54HC194
SRG4
R
1
0
M 0
3
C4
1->/2<-
54HC194
2,4D
3,4D
3,4D
3,4D
3,4D
1,4D
54HC192
CTRDIV10
CT=0
2+
G1
1-
G2
C3
ICT=9
ZCT=0
54HC192
3D
CTRDIV10
CT=0
2+
G1
1-
G2
C3
ICT=9
ZCT=0
54HC192
[8]
[4]
[2]
3D [1]
54HC195
SRG4
R
M1[SHIFT]
M2[LOAD]
C3/1->
54HC195
2,3D
2,3D
1,3J
1,3K

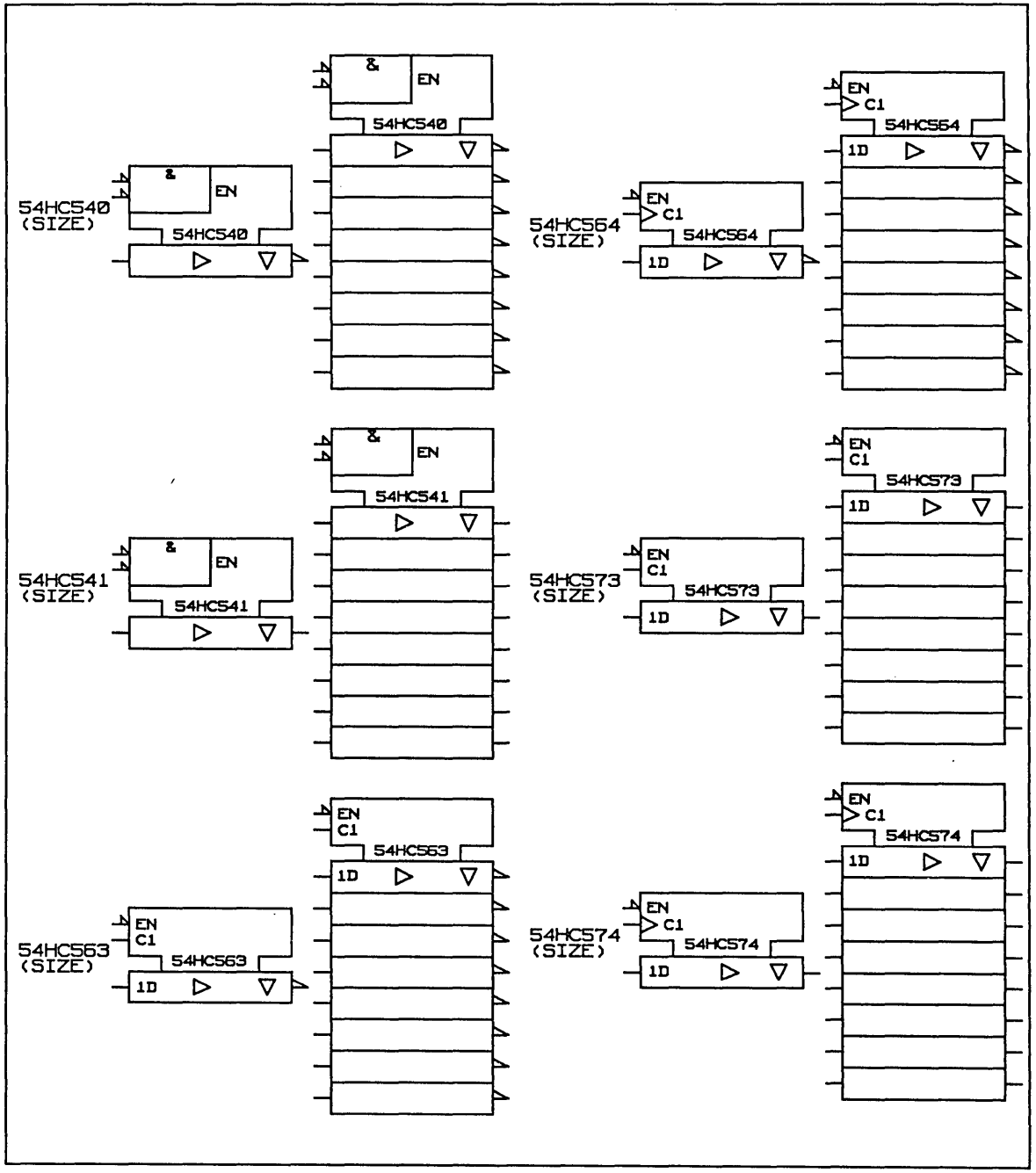

54HCT241
(SIZE)
EN
54HCT241
PULSE_WIDTH=10000
54HC221
&
1
R
CX
RX/CX
54HC237
CB
DMUX
BD
G
54HC237
X/Y
EN
54HC240
(SIZE)
54HC240
54HCT240
(SIZE)
54HCT240
54HC241
(SIZE)
54HC241
54HC242
(SIZE)
EN1
EN2
54HC242
54HC243
(SIZE)
54HC243

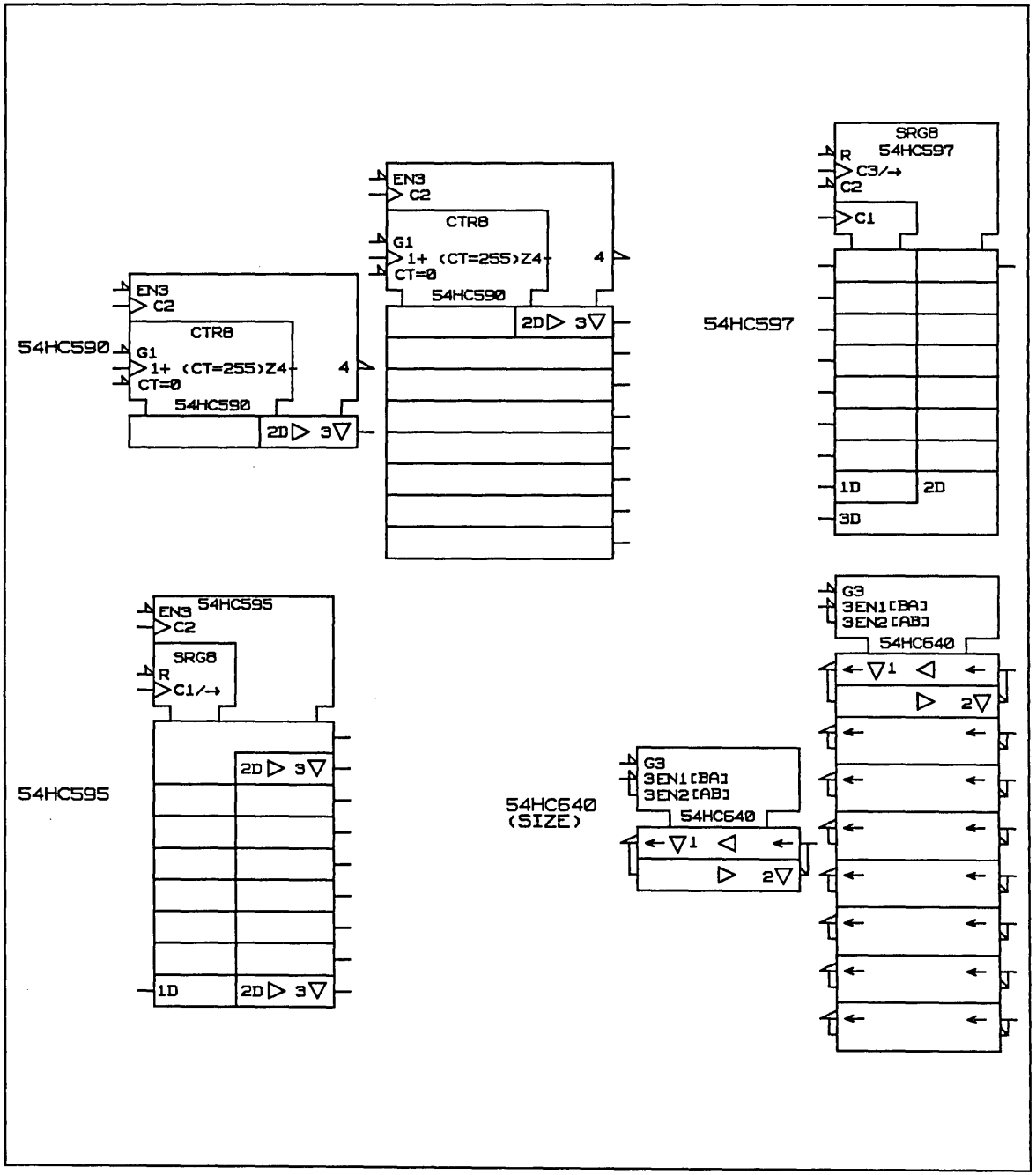

54HC244
(SIZE)
EN
54HC244
54HCT244
(SIZE)
54HCT244
54HC245
(SIZE)
G3
3 EN1 [BA]
3 EN2 [AB]
54HCT245
54HC251
(SIZE)
MUX
54HC251
54HC253
(SIZE)
54HC253
54HC257
(SIZE)
G1
54HC257
54HC259
BM
G8
Z9
Z10
9,7D
10,7R
9,6D
10,6R
9,5D
10,5R
9,4D
10,4R
9,3D
10,3R
9,2D
10,2R
9,1D
10,1R
9,0D
10,0R

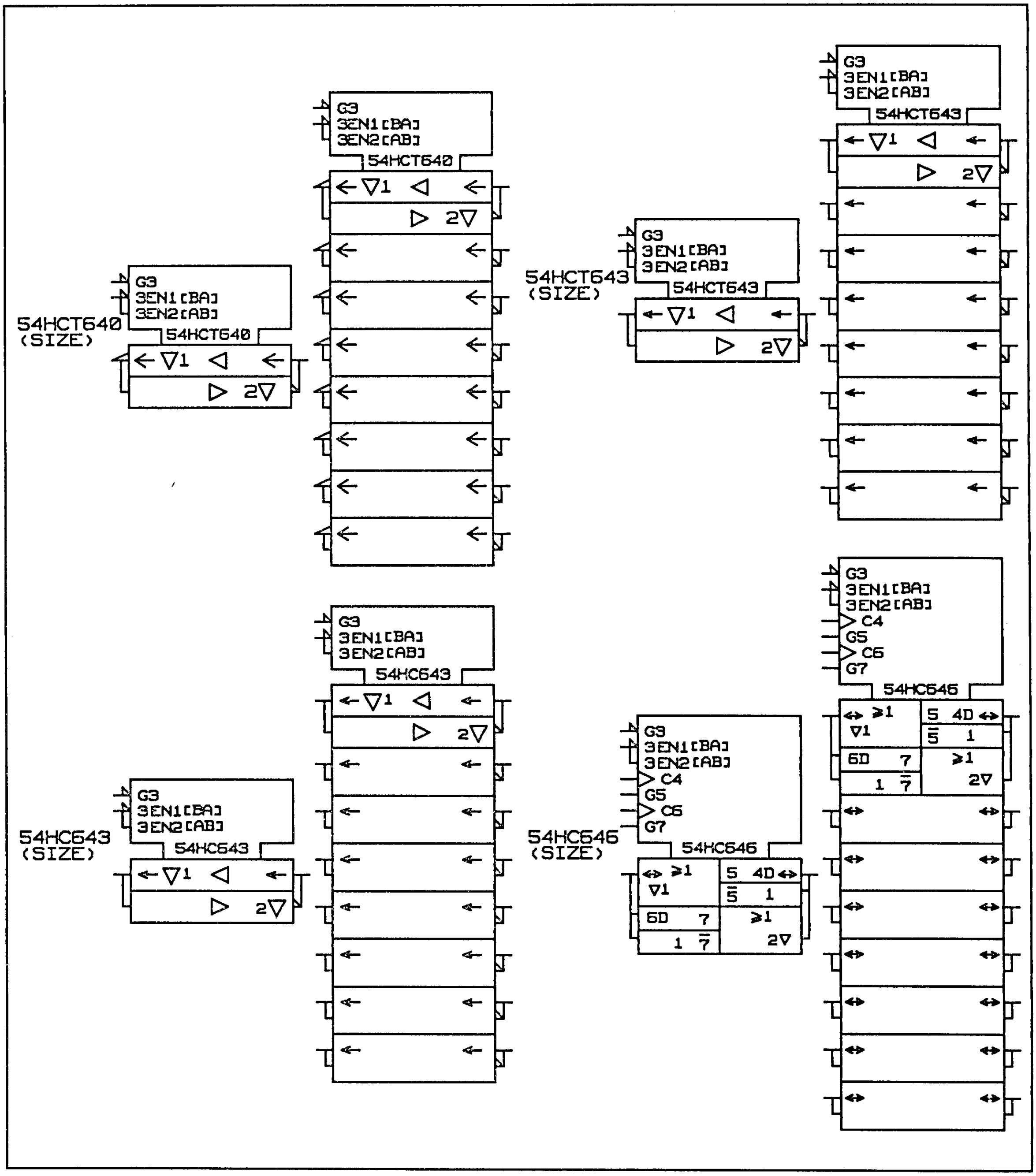

MAX_DELAY=10000
=1
54HC266
54HC266
(SIZE)
MAX_DELAY=10000
=1
54HC266
54HC292
R
≥1
[n=0]
[n=1]
[TP3]
[TP2]
[TP1]
54HC292
4
0
[n] 31 0
54HC294
R
≥1
[n=0]
[n=1]
[TP]
54HC294
3
0
[n] 15 0
R
C1
54HC273
1D
54HC273
(SIZE)
R
C1
54HC273
1D
54HC280
2K
54HC280
54HCT280
2K
54HCT280
54HC283
Σ
P
Q
CI
CO
54HC298
(SIZE)
G1
MUX
C2
54HC298
1,2D
1̄,2D
G1
MUX
C2
54HC298
1,2D
1̄,2D
SRG8
R
&
3EN13
M
C4/1→/2←
54HC299
54HC299
2,4D
3,4D
12,13
Z12
3,4D
11,13
Z11
3,4D
5,13
Z5
1,4D

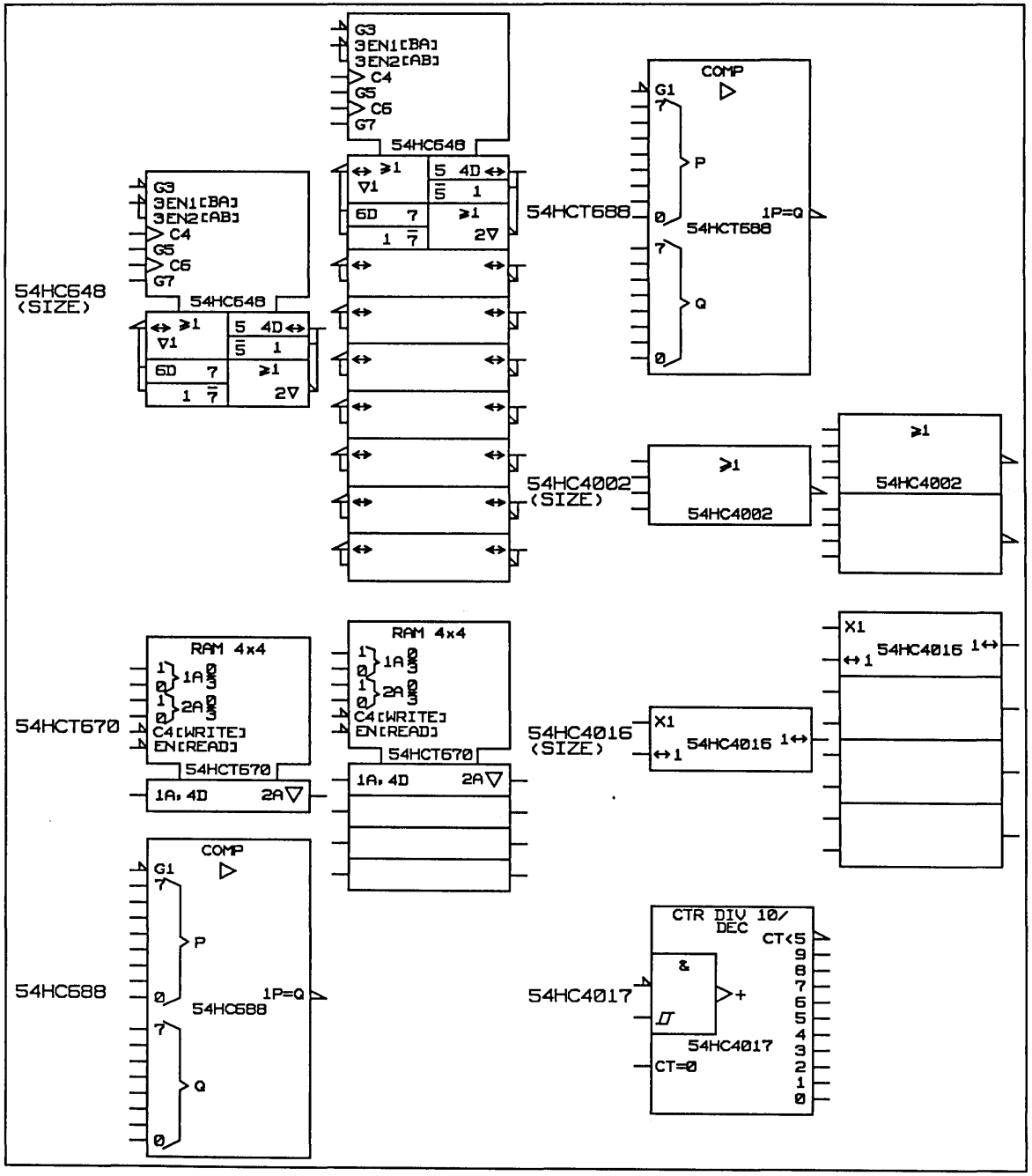

MUX
&
EN
C8
8D
8D
8D
C9
2
0
G0
7
54HC354
(SIZE)
54HC354
9D 7
9D 6
9D 5
9D 4
9D 3
9D 2
9D 1
9D 0
>1
MUX
&
EN
C8
8D
8D
8D
C9
2
0
G0
7
54HC356
(SIZE)
54HC356
9D 7
9D 6
9D 5
9D 4
9D 3
9D 2
9D 1
9D 0
>1
&
EN
54HC365
&
EN
54HC365
54HC365
(SIZE)
54HC365
&
EN
54HC366
&
EN
54HC366
54HC366
(SIZE)
54HC366
EN
54HC367
EN
54HC367
54HC367
(SIZE)
EN
54HC367
EN
54HC367
EN
54HC368
EN
54HC368
54HC368
(SIZE)
EN
54HC368
EN
54HC368
EN
C1
54HC373
1D
EN
C1
54HC373
(SIZE)
54HC373
1D

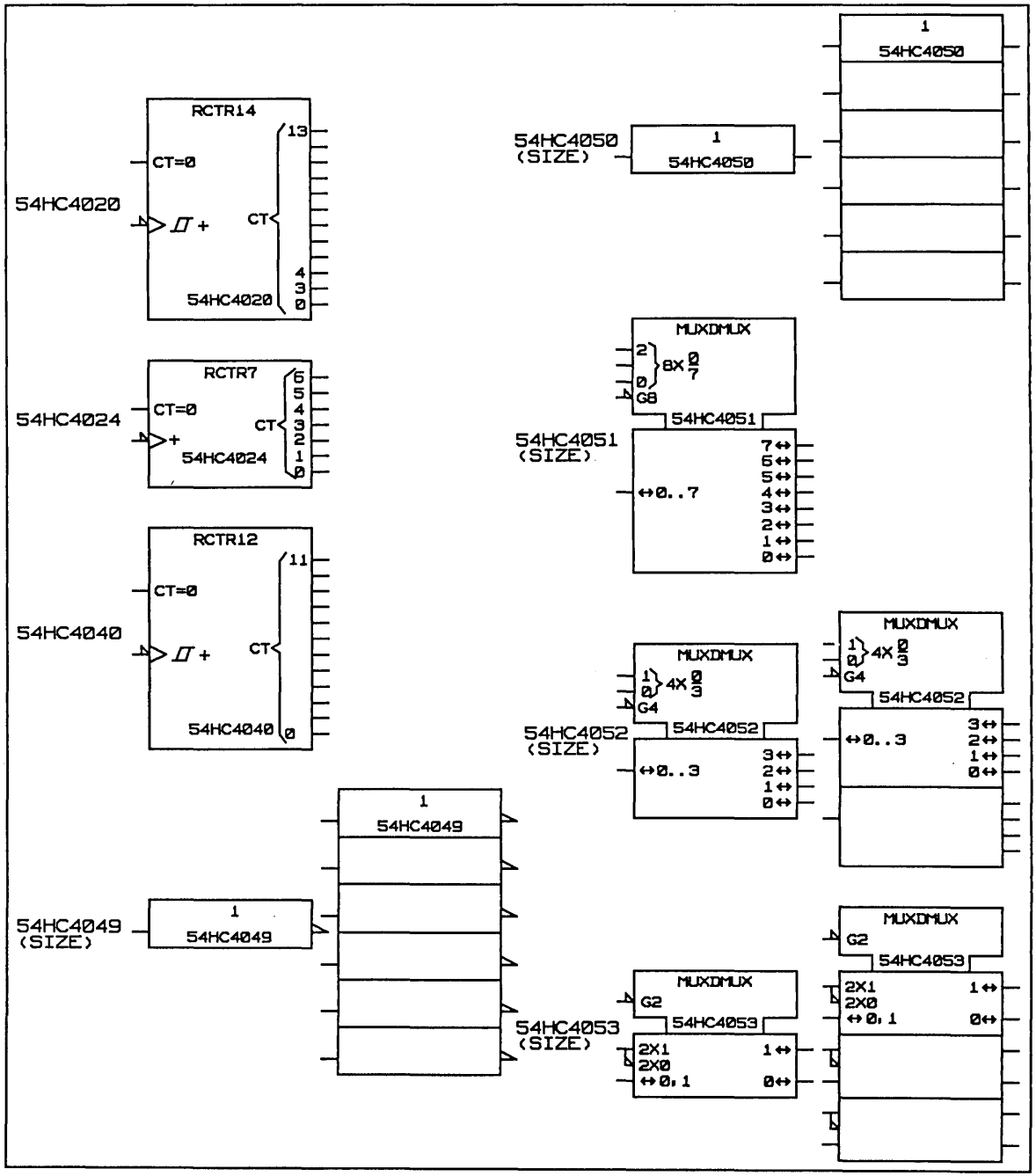

CTR
CT=0
54HC390
DIV5
CT
2
0
DIV2
54HC390
EN
C1
54HCT373
1D
54HCT373
(SIZE)
CTRDIV16
CT=0
CT
3
0
54HC393
54HC393
PULSE_WIDTH=10000
&
54HC423
R
CX
RX/CX
54HC423
54HC374
54HC374
(SIZE)
54HC533
54HC533
(SIZE)
54HCT374
54HCT374
(SIZE)
54HC534
54HC534
(SIZE)

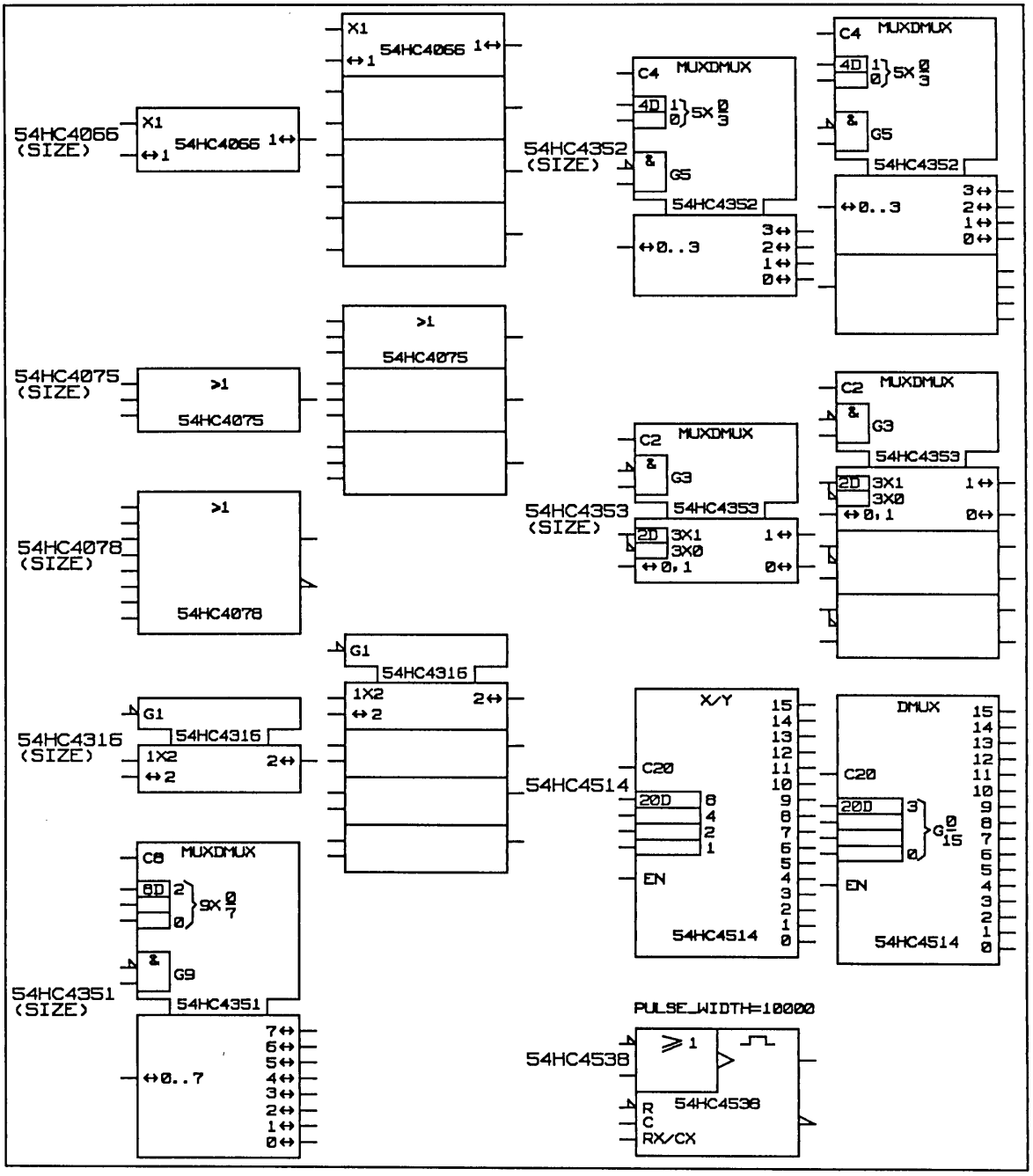

&
EN
54HC540
54HC540
(SIZE)
EN
C1
54HC564
1D
54HC564
(SIZE)
54HC541
54HC541
(SIZE)
54HC573
54HC573
(SIZE)
54HC563
54HC563
(SIZE)
54HC574
54HC574
(SIZE)

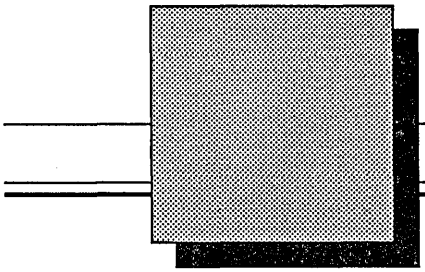

54HC590
EN3
C2
CTR8
G1
1+ (CT=255)Z4
CT=0
54HC590
2D
3
4
54HC597
SRG8
54HC597
R
C3/→
C2
C1
1D
2D
3D
54HC595
SRG8
C1/→
54HC640
(SIZE)
G3
3EN1 [BA]
3EN2 [AB]
54HC640
1
2


54HCT640
(SIZE)
54HCT640
54HCT643
(SIZE)
54HCT643
54HC643
(SIZE)
54HC643
54HC646
(SIZE)
54HC646
G3
3EN1[BA]
3EN2[AB]
C4
G5
C6
G7
∇1
2∇
5
4D
6D
7
≥1


54HC648
(SIZE)
54HC4002
(SIZE)
54HCT670
54HC4016
(SIZE)
54HC688
54HC4017
54HCT688
54HC4002
54HC4016
54HC4017
54HC648
54HCT670
54HC688
54HCT688
COMP
RAM 4x4
CTR DIV 10/DEC


RCTR14
CT=0
CT
13
4
3
0
54HC4020
54HC4020
RCTR7
CT=0
CT
6
5
4
3
2
1
0
54HC4024
54HC4024
RCTR12
CT=0
CT
11
0
54HC4040
54HC4040
1
54HC4049
54HC4049
(SIZE)
1
54HC4049
1
54HC4050
54HC4050
(SIZE)
1
54HC4050
MUXDMUX
2
0
8X 0 7
G8
54HC4051
54HC4051
(SIZE)
↔0..7
7↔
6↔
5↔
4↔
3↔
2↔
1↔
0↔
MUXDMUX
1
0
4X 0 3
G4
54HC4052
54HC4052
(SIZE)
↔0..3
3↔
2↔
1↔
0↔
MUXDMUX
G2
54HC4053
54HC4053
(SIZE)
2X1
2X0
↔0,1
1↔
0↔
MUXDMUX
G2
54HC4053
2X1
2X0
↔0,1
1↔
0↔


54HC4066
(SIZE)
X1
54HC4066
54HC4075
(SIZE)
>1
54HC4075
54HC4078
(SIZE)
54HC4078
54HC4316
(SIZE)
G1
54HC4316
1X2
2↔
54HC4351
(SIZE)
C8 MUXDMUX
54HC4352
(SIZE)
C4 MUXDMUX
54HC4352
54HC4353
(SIZE)
C2 MUXDMUX
54HC4353
54HC4514
X/Y
DMUX
C20
EN
54HC4514
PULSE_WIDTH=10000
54HC4538
R
C
RX/CX



The 54FAST and ANSI 54FAST Libraries

The 54FAST Library requires approximately 2271 Kbytes of disk storage, and the ANSI 54FAST Library requires approximately 2232 Kbytes of disk storage. The physical, timing, and simulation models for each library are identical and differ only in their body drawings. The part name for a component in either library is the same; the body drawing used is determined by the first library name encountered in the library search path (*fast.lib* or *a74fast.lib*).

The specifications used to construct the models in these libraries were taken from either the Fairchild FAST data books or from Mil Spec MIL-M-38510. Parts identified with an asterisk (*) are from MIL-M-38510; the descriptions for these components include the military device type in parentheses.

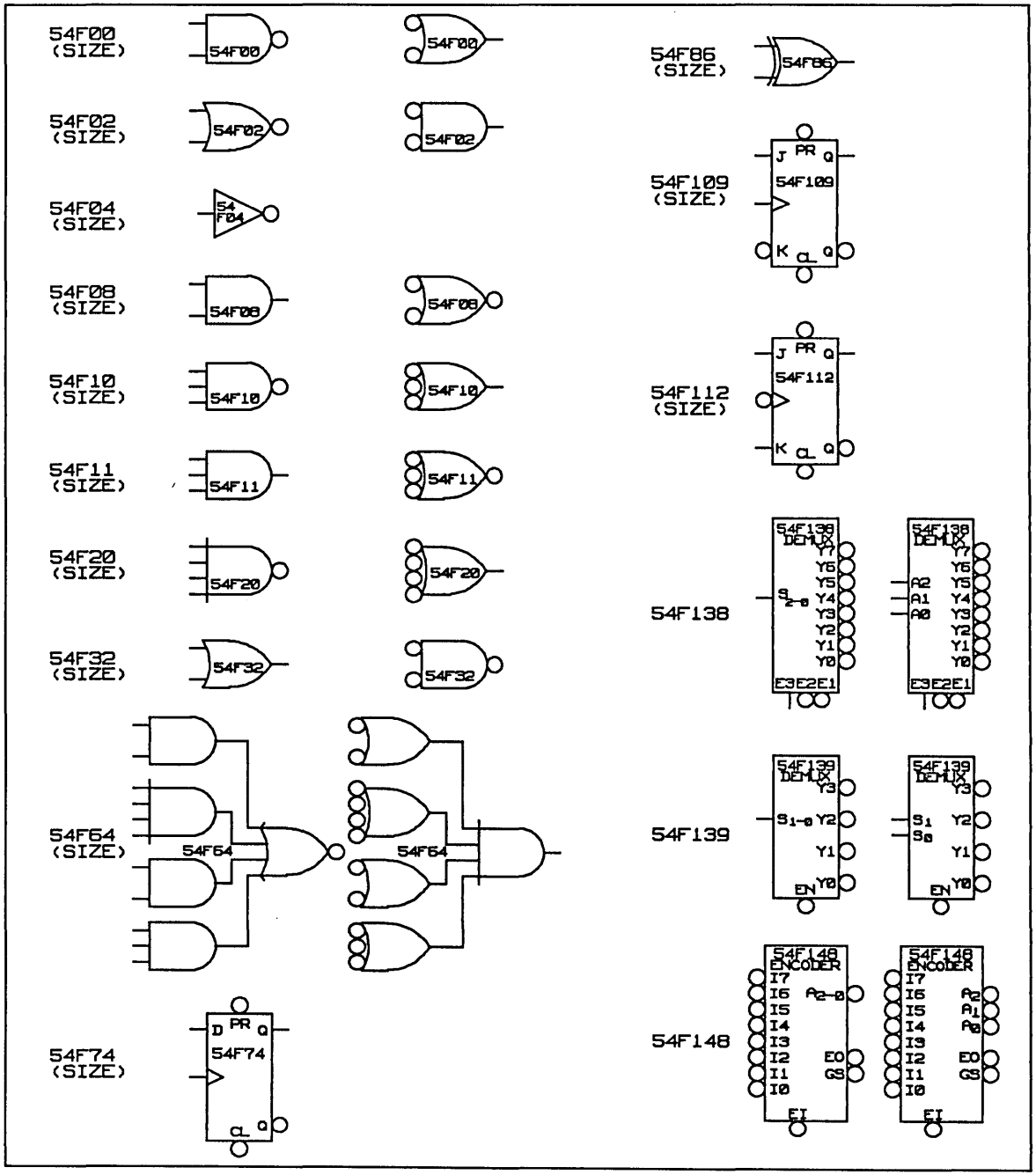
The release level of the 54FAST and ANSI 54FAST Libraries is 9.0.

Each library contains body drawings and physical, timing, and simulation models for the following 62 components:

* **54F00**	Quad 2-input NAND (33001)
* **54F02**	Quad 2-input NOR (33301)
* **54F04**	Hex inverter (33002)
* **54F08**	Quad 2-input AND (34001)
* **54F10**	Triple 3-input NAND (33003)
* **54F11**	Triple 3-input AND (34002)
* **54F20**	Dual 4-input NAND (33004)
* **54F32**	Quad 2-input OR (33501)
* **54F64**	4-2-3-2-input AND-OR-invert gate (33401)
* **54F74**	Dual positive-edge-triggered D flip-flop (34101)
* **54F86**	Quad 2-input exclusive-OR (34501)
* **54F109**	Dual JKbar positive-edge-triggered flip-flop (34102)
* **54F112**	Dual JK negative-edge-triggered flip-flop (34103)
* **54F138**	3-to-8-line decoders/multiplexers (33701)
* **54F139**	Dual 2-to-4-line decoders/multiplexers (33702)
54F148	8-line to 3-line priority encoder
* **54F151**	1-of-8 data selectors/multiplexers (33901)
* **54F153**	Dual 4-line to 1-line data multiplexer (33902)
* **54F157**	Quad 2-to-1-line non-inverting multiplexer (33903)
* **54F158**	Quad 2-to-1-line inverting data multiplexer (33904)

54F161	Synchronous presettable binary counter
54F163	4-bit synchronous binary counters with synchronous clear
54F164	Serial-in parallel-out shift register
54F169	4-stage synchronous bidirectional counter
* 54F174	Hex D-type flip-flops (34017)
* 54F175	Quad D-type flip-flops (34104)
54F181	Arithmetic logic units/function generators
54F182	Look-ahead carry generators
54F189	64-bit random access memory
54F190	Synchronous BCD up/down counter
54F191	Synchronous binary up/down counter
* 54F194	4-bit bidirectional shift register (33601)
54F219	64-bit random access memory
* 54F240	Octal inverting 3-state bus transceiver (33201)
* 54F241	Octal non-inverting 3-state bus transceiver (33202)
* 54F242	Octal bus transceiver with 3-state outputs (34801)
* 54F243	Quad non-inverting 3-state bus transceiver (34802)
* 54F244	Octal non-inverting 3-state bus transceiver (33203)
* 54F245	Octal non-inverting 3-state bus transceiver (34803)
* 54F251	3-state data multiplexer (33905)
* 54F253	Dual data selectors/multiplexers (33908)
* 54F257	Quad 3-state non-inverting data multiplexer (33906)
* 54F258	Quad 3-state inverting data multiplexer (33907)
54F273	Octal D-type flip-flops
* 54F280	9-bit odd/even parity generators/checkers (34901)

* **54F283**	4-bit binary full adders (34201)
54F323	8-bit universal shift/storage register
* **54F352**	Dual 4-input multiplexer (33909)
* **54F353**	Dual 4-input multiplexer with 3-state outputs (33910)
* **54F373**	Octal 3-state D-latch with common enable (34601)
* **54F374**	Octal 3-state positive-edge-triggered D register (34105)
54F377	Octal D-type flip-flops with clock enable
54F378	Parallel D-type register with enable
54F379	Quad D-type flip-flops with enable
54F381	Arithmetic logic unit/function generator
54F382	4-bit arithmetic logic unit
* **54F398**	Quad 2-port register (35001)
* **54F399**	Quad 2-port register (35002)
* **54F521**	8-bit identity comparator (34701)
* **54F533**	Octal transparent latch (34602)
* **54F534**	Octal D-type flip-flop (34106)
54F569	4-bit binary counter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54 F04
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54F20 (SIZE)
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54F32
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54F74 (SIZE)
D PR Q
54F74
Q
54F86 (SIZE)
54F86
54F109 (SIZE)
J PR Q
54F109
K Q
54F112 (SIZE)
J PR Q
54F112
K Q
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54F138 DEMUX
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S2-0
E3 E2 E1
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A2 A1 A0
54F139
54F139 DEMUX
Y3 Y2 Y1 Y0
S1-0
EN
54F139 DEMUX
S1 S0
54F148
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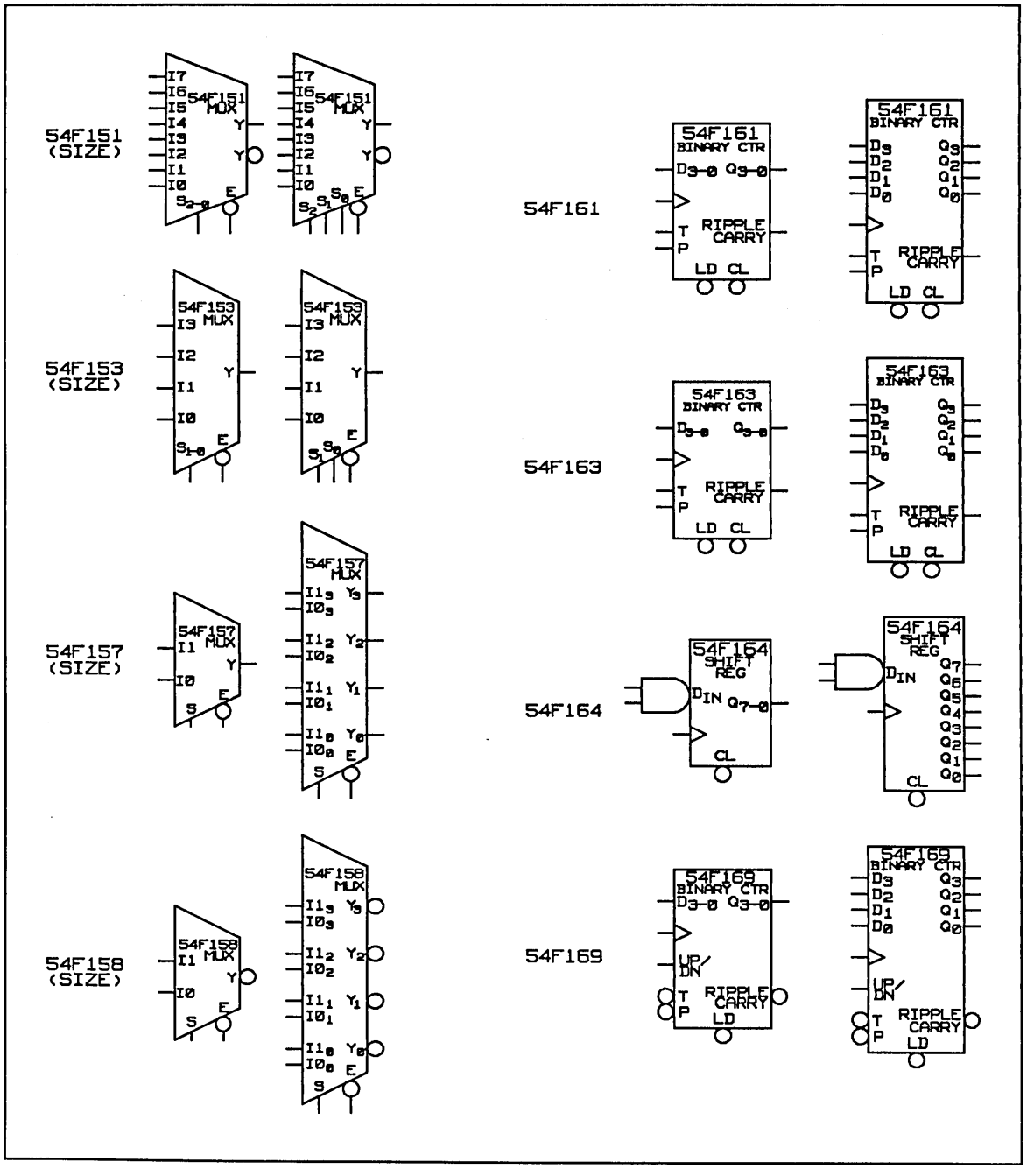
A2-0
EO GS
EI
54F148 ENCODER
A2 A1 A0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54F164
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54F153 MUX
54F157 MUX
54F158 MUX
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54F163 BINARY CTR
54F164 SHIFT REG
54F169 BINARY CTR
RIPPLE CARRY
LD CL

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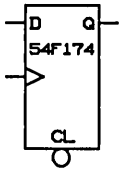

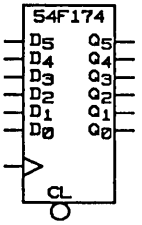

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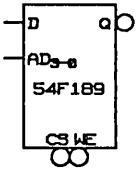

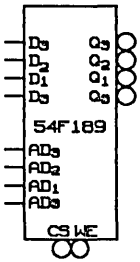

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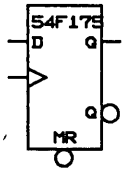

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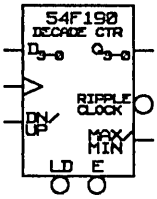

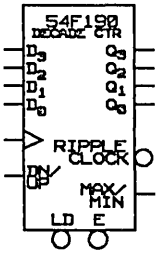

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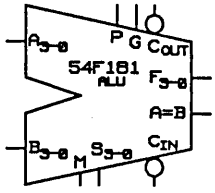

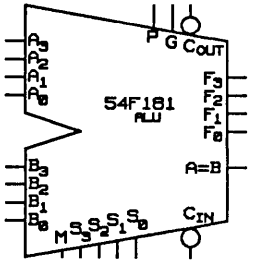

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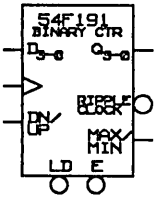

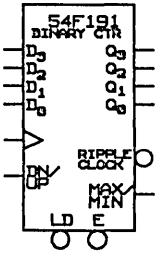

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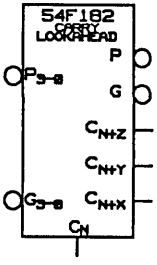

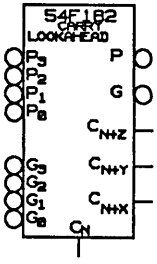

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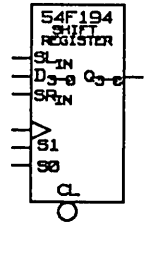

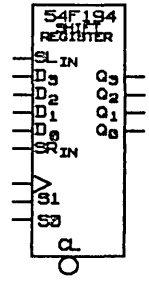

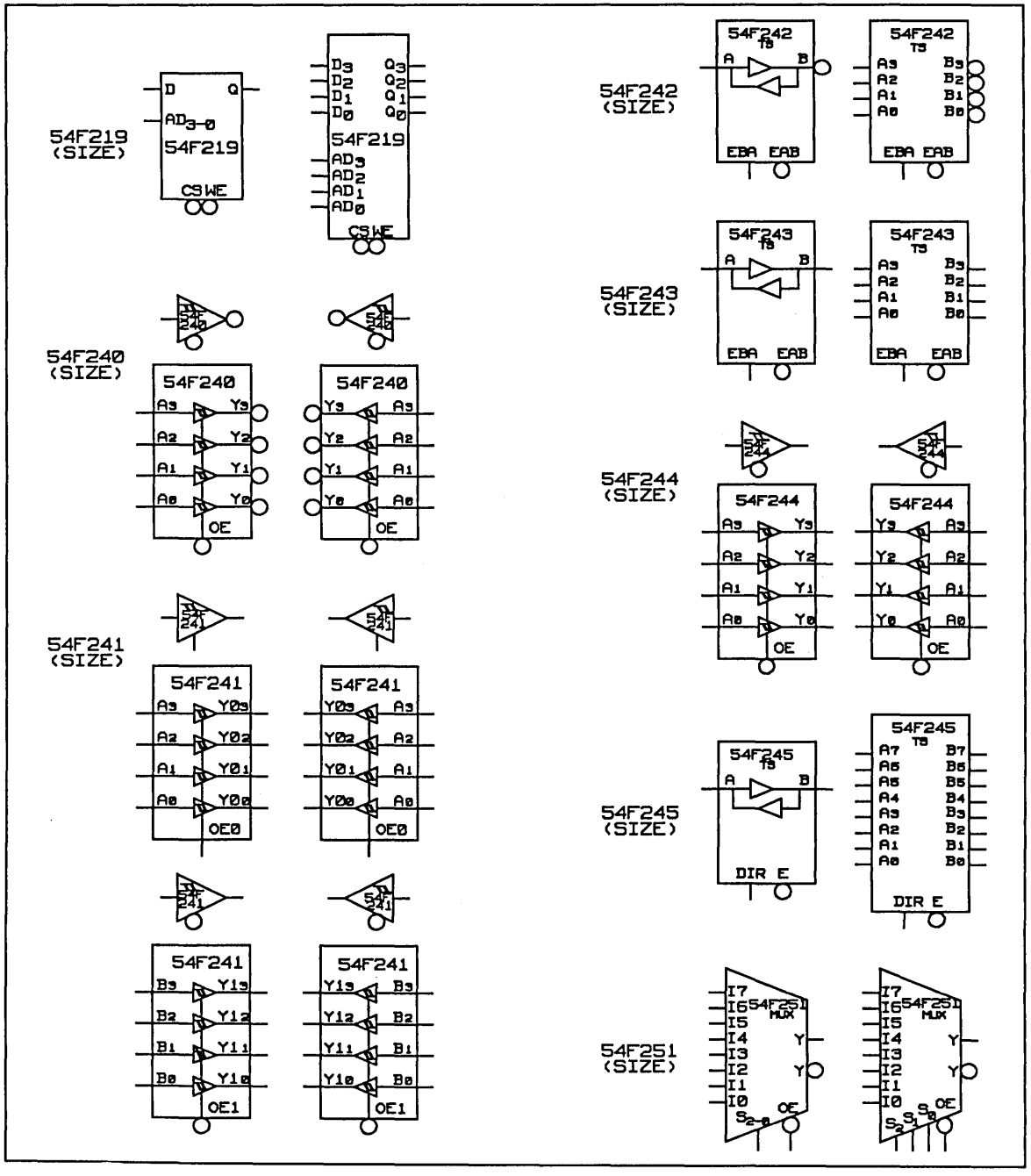
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D2
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D0
Q3
Q2
Q1
Q0
AD3
AD2
AD1
AD0
54F240
(SIZE)
54F240
A3
A2
A1
A0
Y3
Y2
Y1
Y0
OE
54F241
(SIZE)
54F241
Y03
Y02
Y01
Y00
OE0
B3
B2
B1
B0
Y13
Y12
Y11
Y10
OE1
54F242
(SIZE)
54F242
TS
A
B
EBA
EAB
54F243
(SIZE)
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(SIZE)
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(SIZE)
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DIR
E
A7
A6
A5
A4
B7
B6
B5
B4
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(SIZE)
54F251
MUX
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I6
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S1
S0

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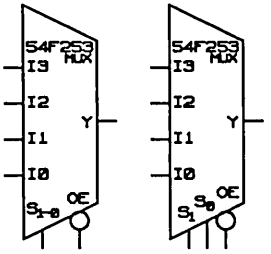

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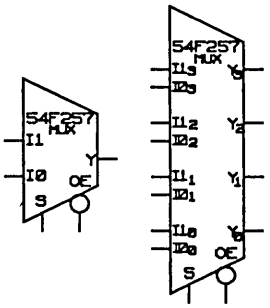

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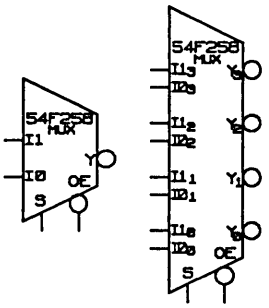

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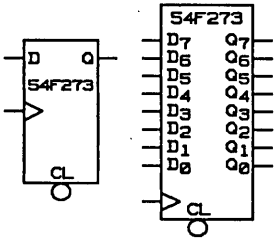

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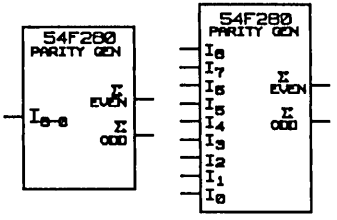

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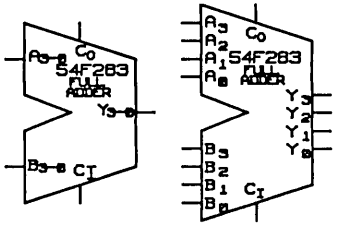

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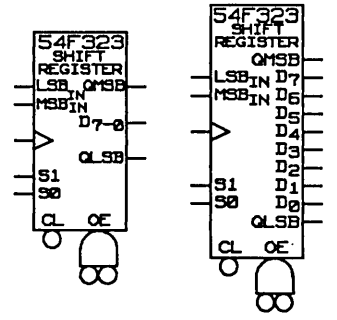

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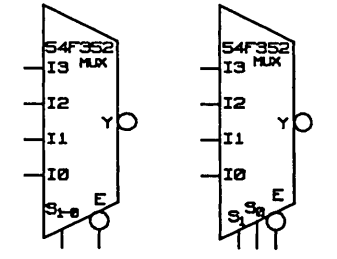

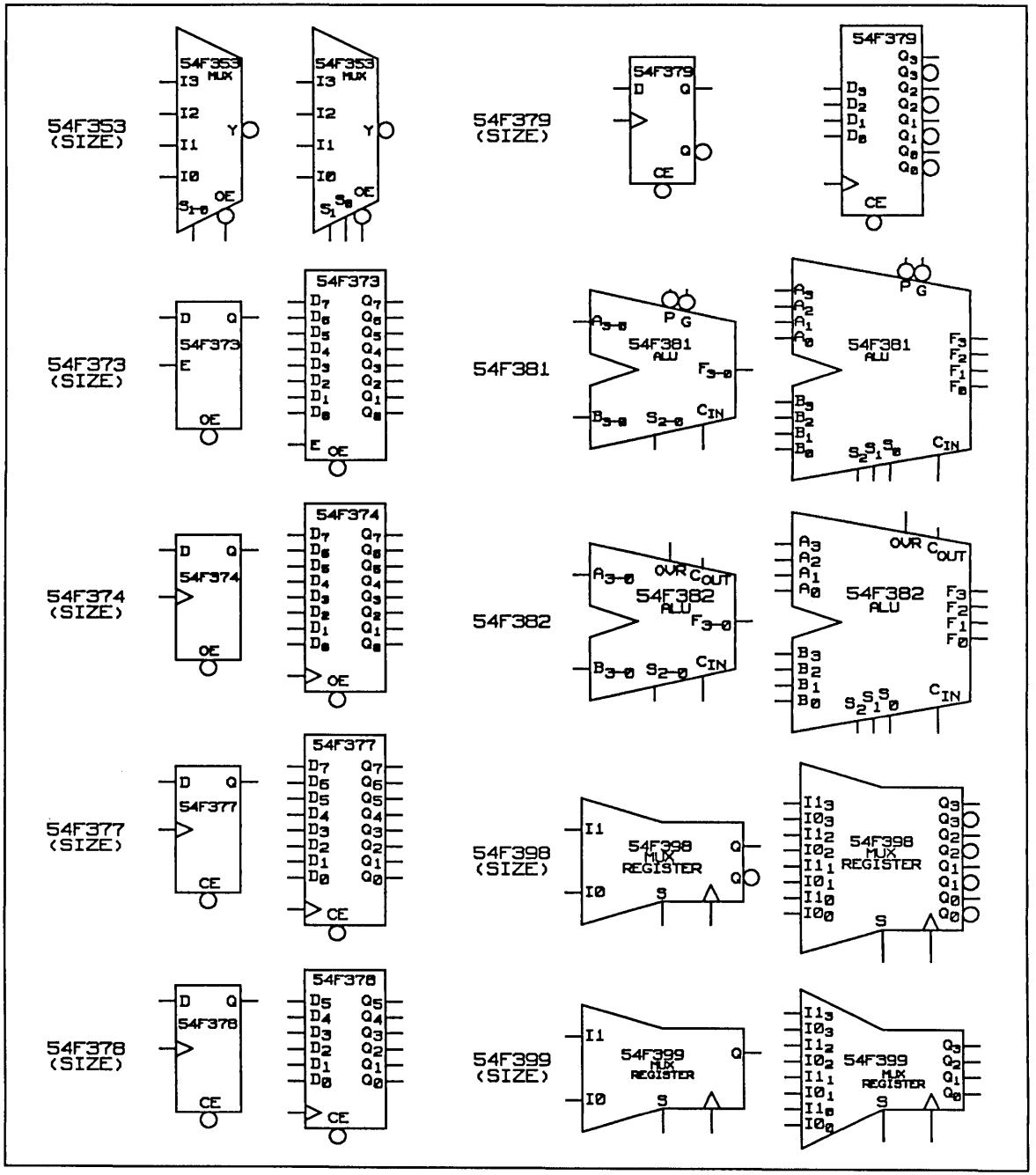
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Q
CE
Q3
Q2
Q1
Q0
D3
D2
D1
D0
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OE
D7
D6
D5
D4
D3
D2
D1
D0
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CIN
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G
ALU
A3
A2
A1
A0
B3
B2
B1
B0
S2 S1 S0
F3
F2
F1
F0
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COUT
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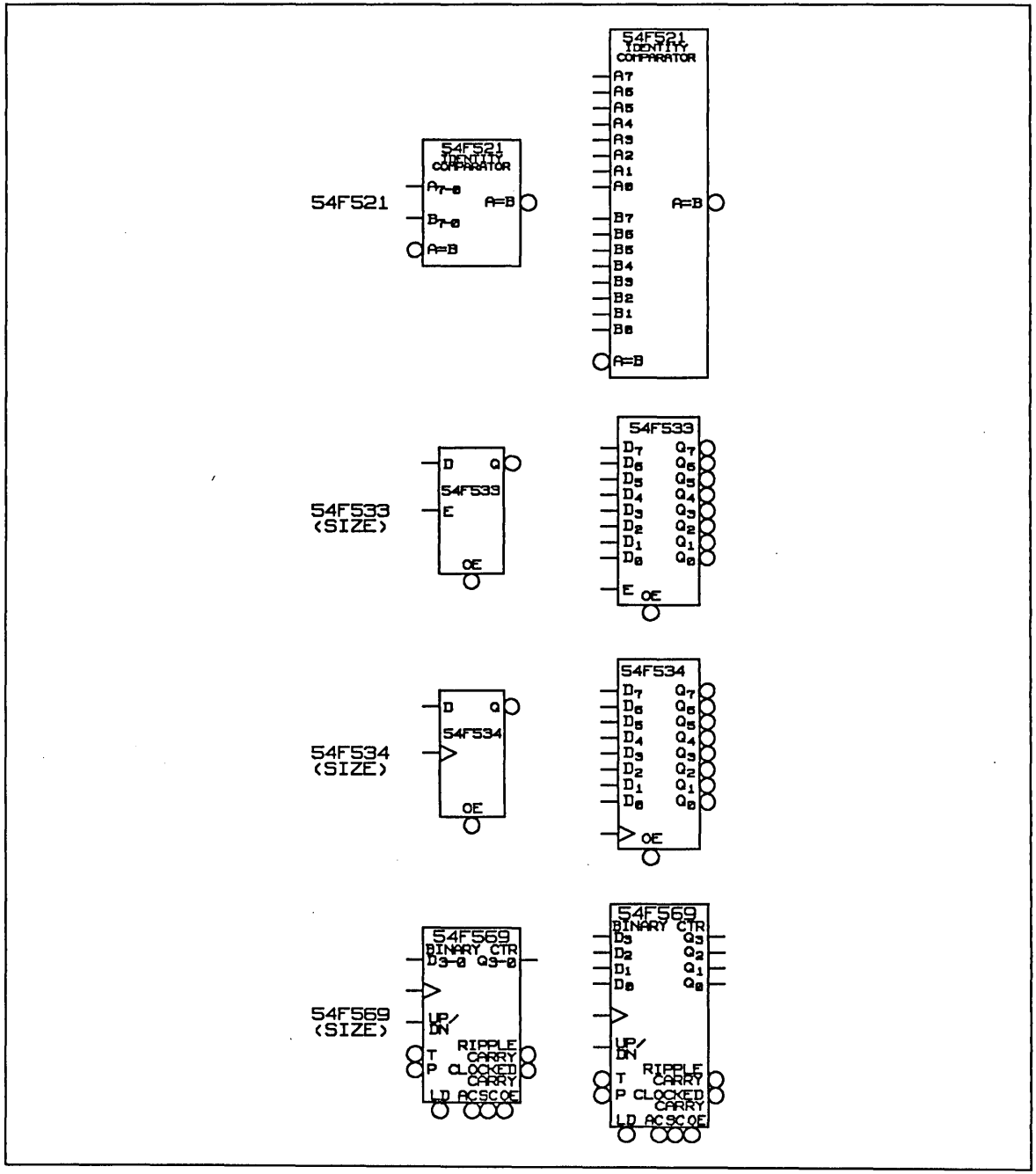
(SIZE)
54F399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IDENTITY
COMPARATOR
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B7-0
A=B
A=B
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IDENTITY
COMPARATOR
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A6
A5
A4
A3
A2
A1
A0
B7
B6
B5
B4
B3
B2
B1
B0
A=B
A=B
54F533
(SIZE)
D
Q
54F533
E
OE
54F533
D7
D6
D5
D4
D3
D2
D1
D0
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Q6
Q5
Q4
Q3
Q2
Q1
Q0
E
OE
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D
Q
54F534
OE
54F534
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D6
D5
D4
D3
D2
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D0
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Q5
Q4
Q3
Q2
Q1
Q0
OE
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BINARY CTR
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Q3-0
UP/
DN
T
P
RIPPLE
CARRY
CLOCKED
CARRY
LD
AC
SC
OE
54F569
BINARY CTR
D3
D2
D1
D0
Q3
Q2
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UP/
DN
T
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CLOCKED
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LD
AC
SC
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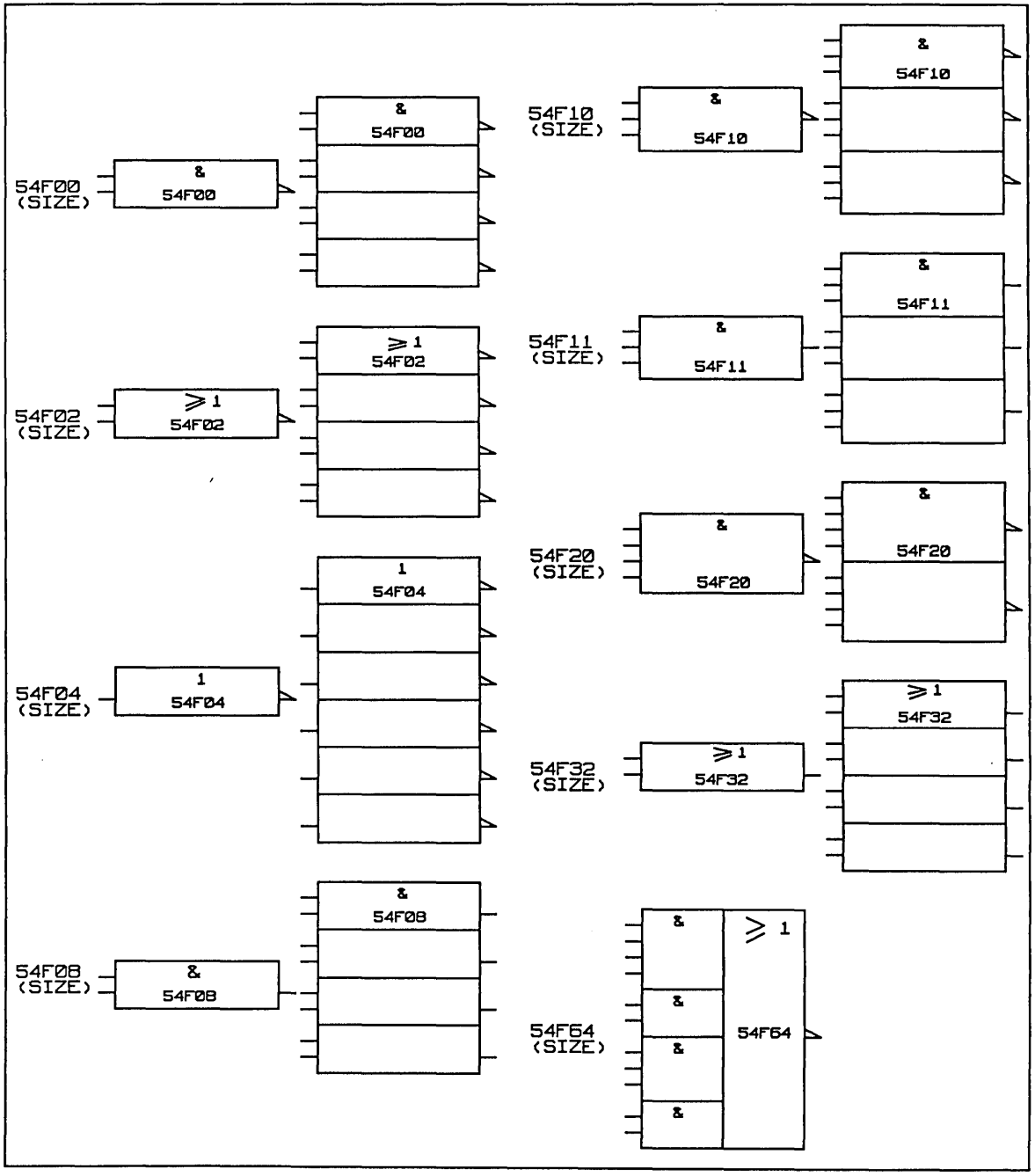
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(SIZE)
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(SIZE)
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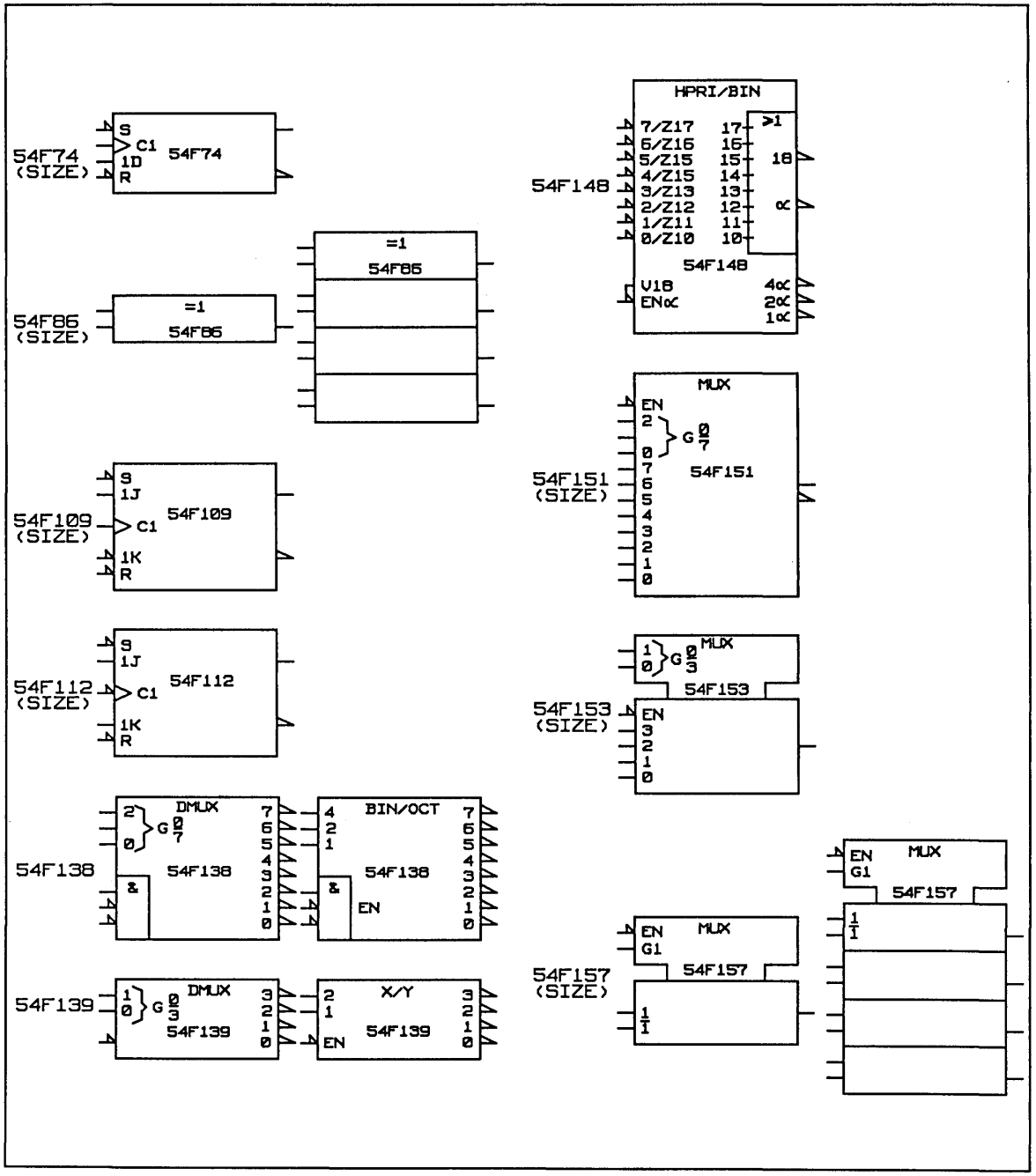
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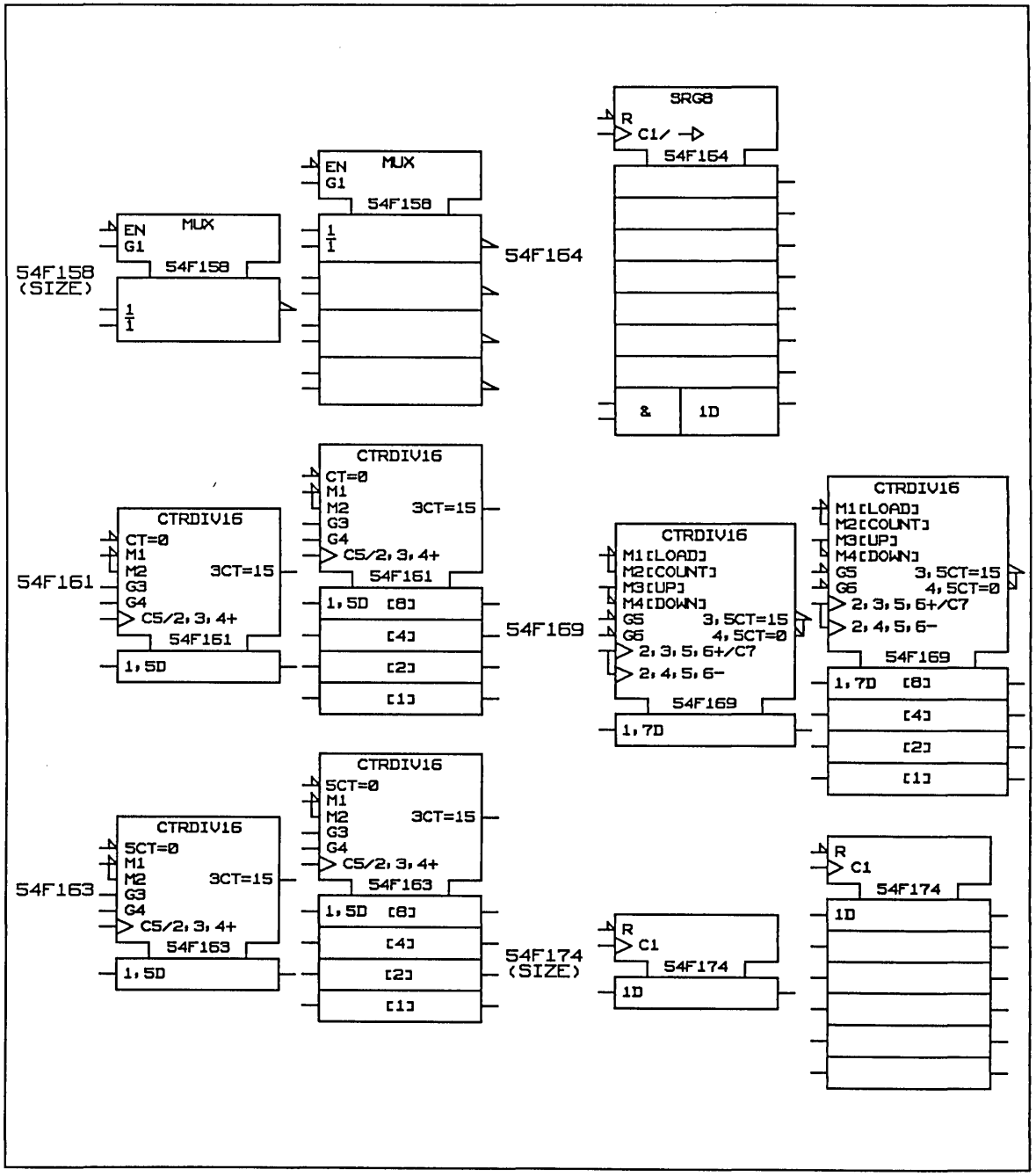
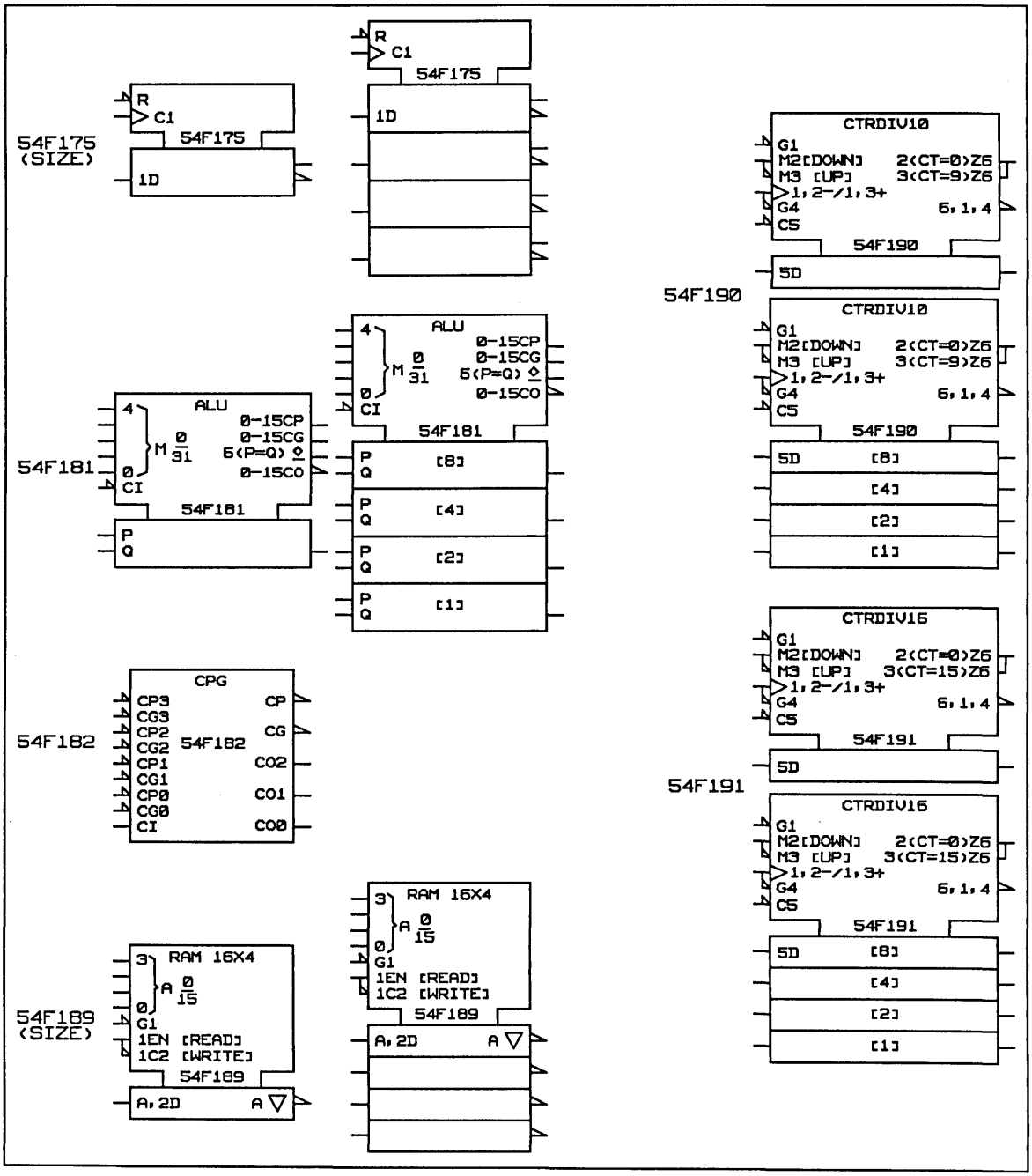
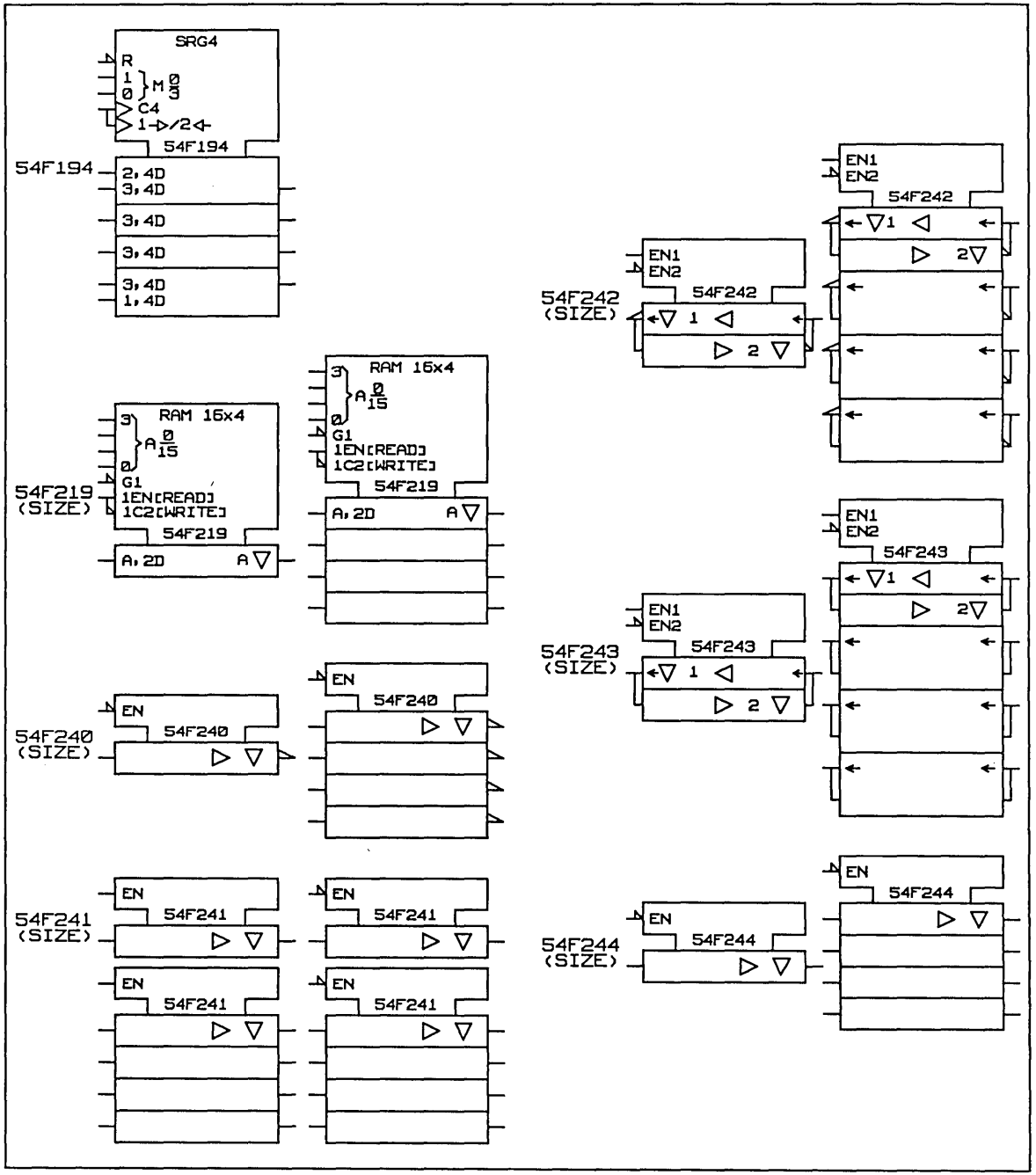
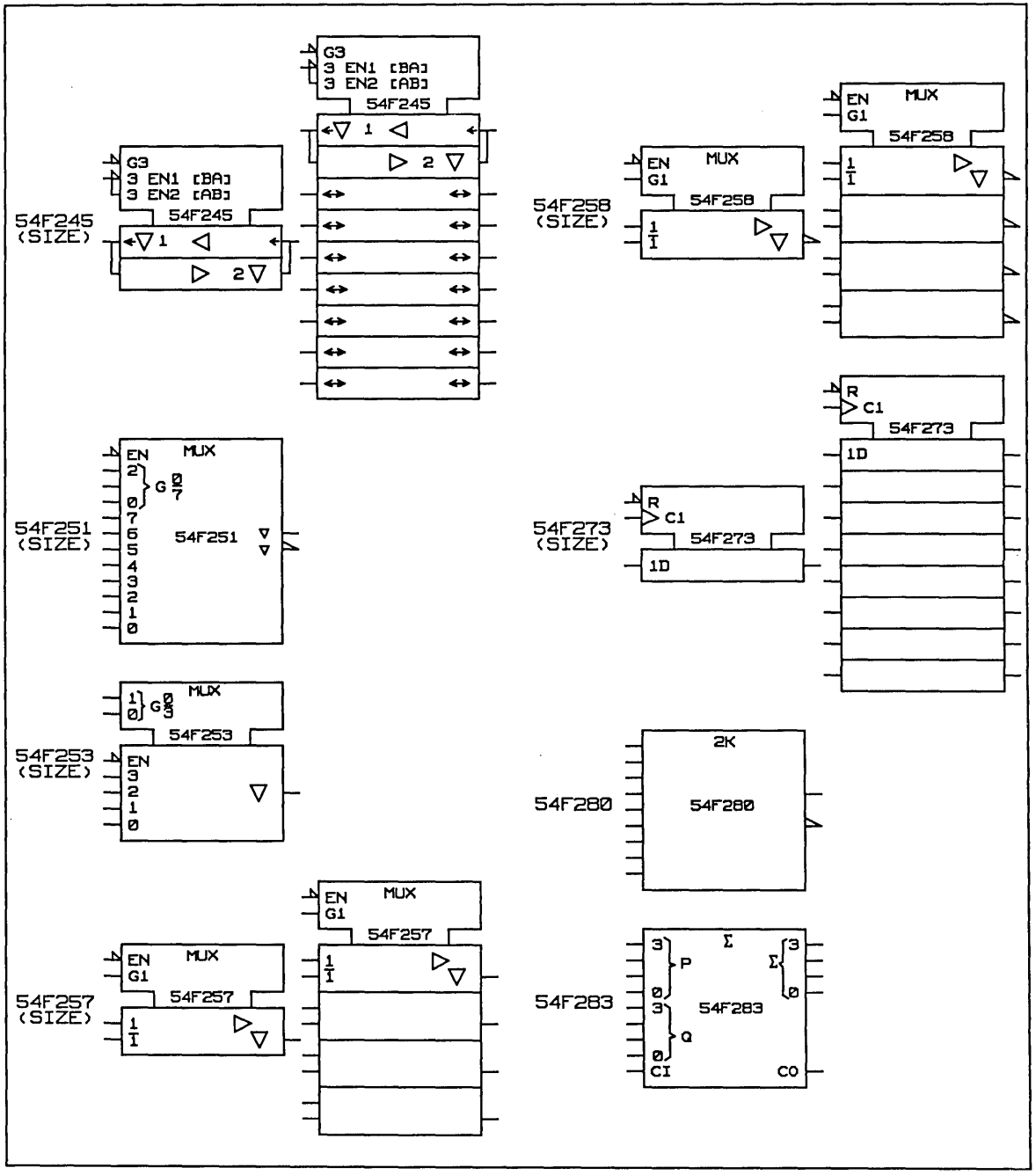
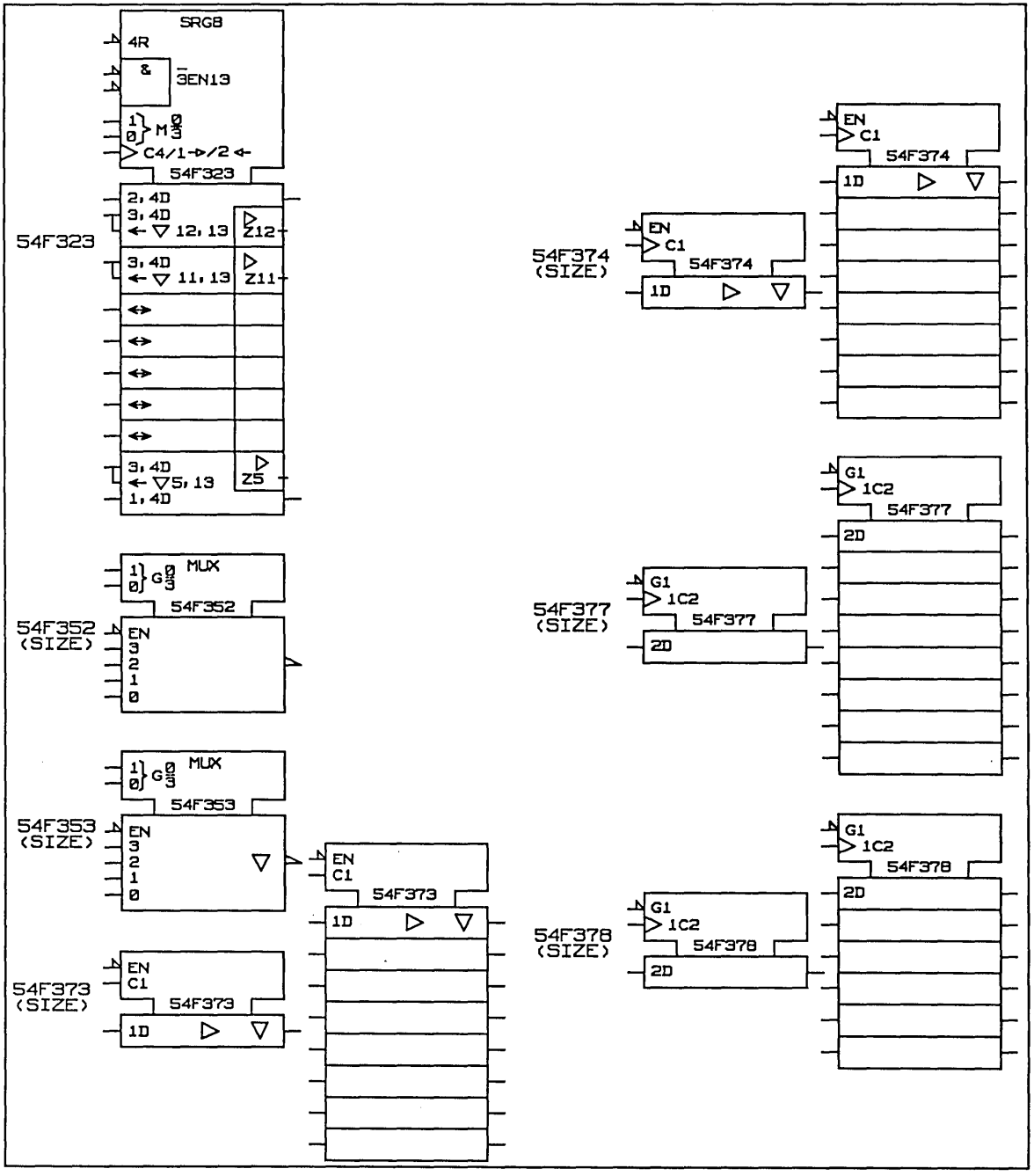
C1
1D
R
54F74
54F86
(SIZE)
=1
54F86
54F109
(SIZE)
S
1J
C1
1K
R
54F109
54F112
(SIZE)
S
1J
C1
1K
R
54F112
54F138
DMUX
G
54F138
&
BIN/OCT
54F138
EN
54F139
DMUX
G
54F139
X/Y
54F139
EN
HPRI/BIN
7/Z17
6/Z16
5/Z15
4/Z14
3/Z13
2/Z12
1/Z11
0/Z10
>1
18
54F148
V18
ENα
4α
2α
1α
54F148
54F151
(SIZE)
MUX
EN
G
54F151
54F153
(SIZE)
MUX
G
54F153
EN
54F157
(SIZE)
MUX
EN
G1
54F157
MUX
EN
G1
54F157

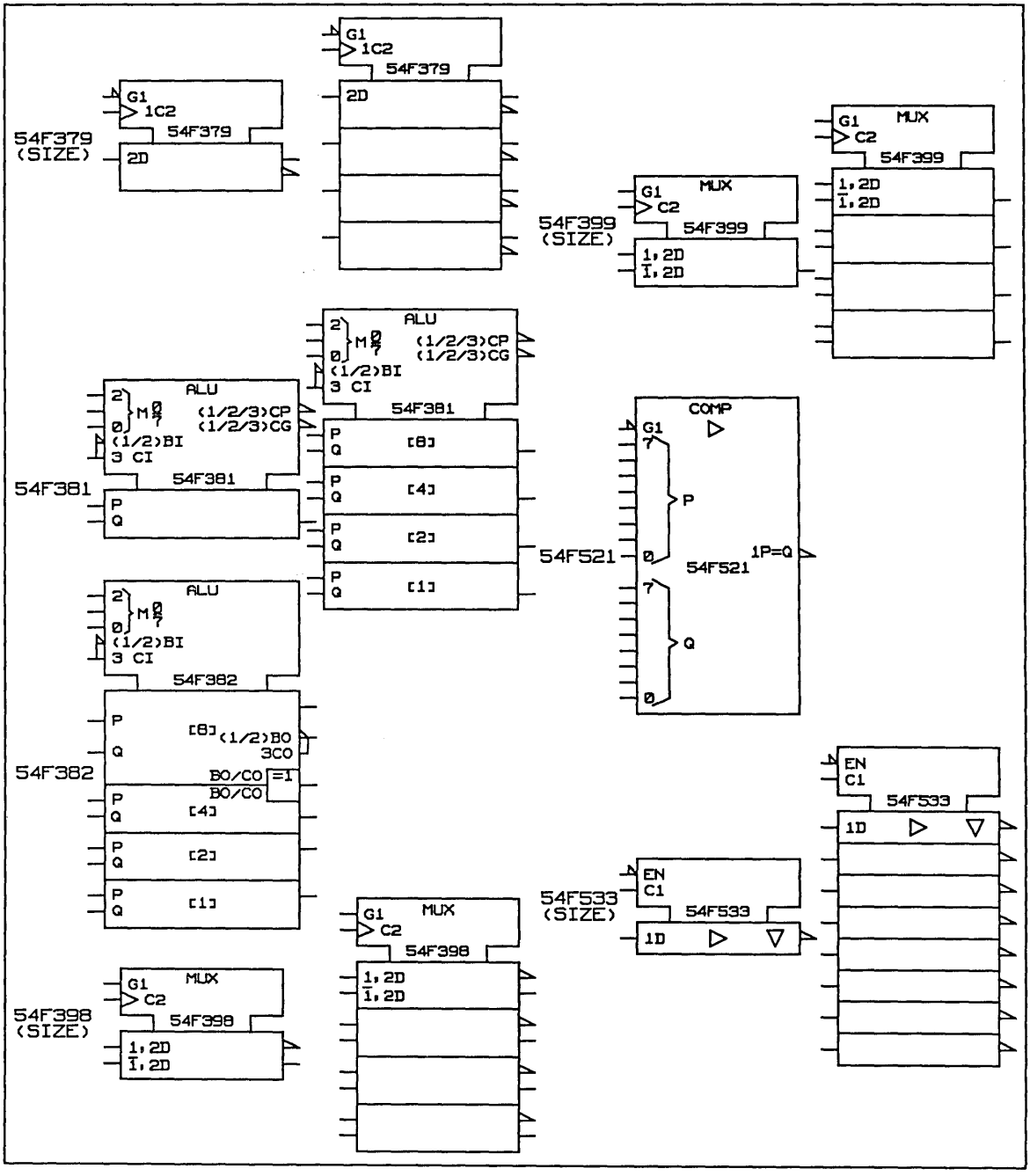

MUX
EN
G1
54F158
1
I
54F158
(SIZE)
54F164
SRG8
R
C1/
54F164
&
1D
CTRDIV16
CT=0
M1
M2
G3
G4
C5/2, 3, 4+
3CT=15
54F161
1, 5D
[8]
[4]
[2]
[1]
54F169
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5
G6
3, 5CT=15
4, 5CT=0
2, 3, 5, 6+/C7
2, 4, 5, 6-
1, 7D
5CT=0
54F163
54F174
(SIZE)
R
C1
1D
54F174

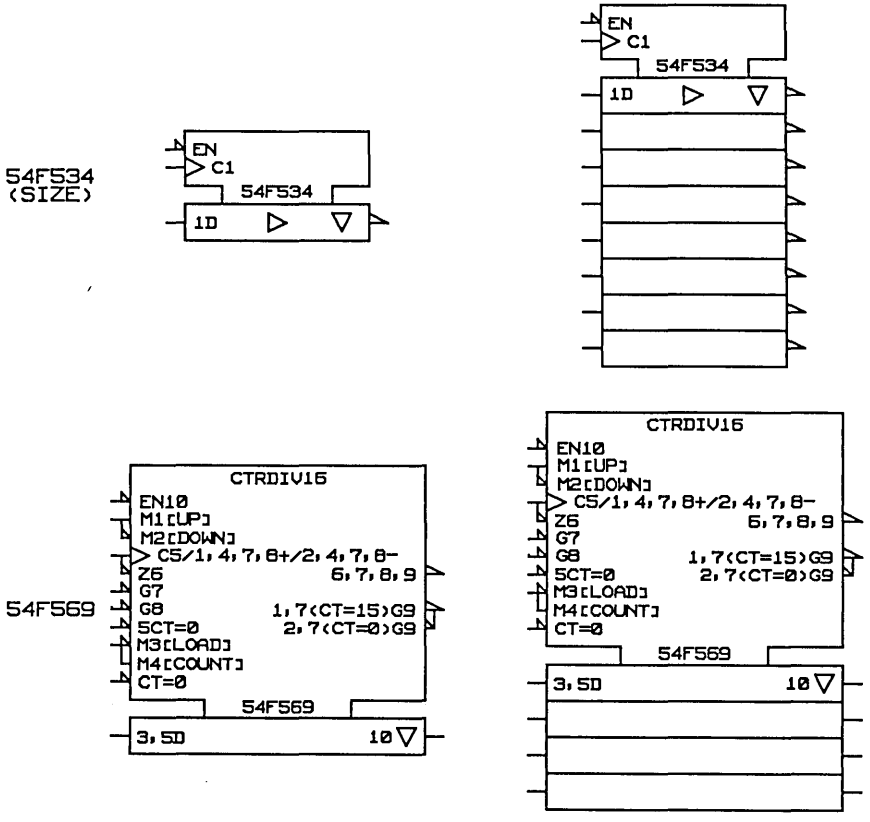

54F175
(SIZE)
R
C1
54F175
1D
54F181
ALU
0-15CP
0-15CG
6(P=Q)
0-15C0
CI
P
Q
54F182
CPG
CP3
CG3
CP2
CG2
CP1
CG1
CP0
CG0
CI
CP
CG
CO2
CO1
CO0
54F189
(SIZE)
RAM 16X4
A 0 15
G1
1EN [READ]
1C2 [WRITE]
A, 2D
A
54F190
CTRDIV10
G1
M2[DOWN]
M3 [UP]
2(CT=0)Z6
3(CT=9)Z6
1, 2-/1, 3+
G4
6, 1, 4
C5
5D
[8]
[4]
[2]
[1]
54F191
CTRDIV16
3(CT=15)Z6

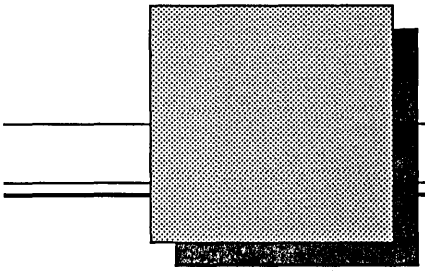

SRG4
R
1
0
M
C4
1→/2←
54F194
54F194
2, 4D
3, 4D
3, 4D
3, 4D
3, 4D
1, 4D
RAM 16x4
A
G1
1EN(READ)
1C2(WRITE)
54F219
54F219
(SIZE)
A, 2D
EN
54F240
54F240
(SIZE)
54F241
54F241
(SIZE)
EN1
EN2
54F242
54F242
(SIZE)
1
2
54F243
54F243
(SIZE)
54F244
54F244
(SIZE)


54F245
(SIZE)
G3
3 EN1 [BA]
3 EN2 [AB]
54F245
1
2
54F258
(SIZE)
EN
G1
MUX
54F258
1
I
54F251
(SIZE)
EN
MUX
G
54F251
54F273
(SIZE)
R
C1
54F273
1D
54F253
(SIZE)
MUX
54F253
EN
54F280
2K
54F280
54F257
(SIZE)
MUX
54F257
54F283
Σ
P
Q
CI
CO
54F283


SRG8
4R
&
3EN13
M
C4/1→/2←
54F323
2, 4D
3, 4D
12, 13
Z12
3, 4D
11, 13
Z11
3, 4D
5, 13
Z5
1, 4D
54F323
MUX
54F352
EN
54F352
(SIZE)
MUX
54F353
EN
54F353
(SIZE)
EN
C1
54F373
1D
EN
C1
54F373
54F373
(SIZE)
EN
C1
54F374
1D
EN
C1
54F374
54F374
(SIZE)
G1
1C2
54F377
2D
G1
1C2
54F377
54F377
(SIZE)
2D
G1
1C2
54F378
2D
G1
1C2
54F378
54F378
(SIZE)
2D


G1
1C2
54F379
2D
54F379
(SIZE)
MUX
C2
54F399
1,2D
1,2D
54F399
(SIZE)
ALU
M
(1/2/3)CP
(1/2/3)CG
(1/2)BI
3 CI
54F381
P
Q
[8]
[4]
[2]
[1]
COMP
7
0
P
Q
54F521
1P=Q
54F382
(1/2)BO
3CO
BO/CO
=1
EN
C1
54F533
1D
54F533
(SIZE)
54F398
(SIZE)


54F534
(SIZE)
EN
C1
54F534
1D
EN
C1
54F534
1D
54F569
CTRDIV16
EN10
M1[UP]
M2[DOWN]
C5/1,4,7,8+/2,4,7,8-
Z6
6,7,8,9
G7
G8
1,7(CT=15)G9
5CT=0
2,7(CT=0)G9
M3[LOAD]
M4[COUNT]
CT=0
54F569
3,5D
10
CTRDIV16
EN10
M1[UP]
M2[DOWN]
C5/1,4,7,8+/2,4,7,8-
Z6
6,7,8,9
G7
G8
1,7(CT=15)G9
5CT=0
2,7(CT=0)G9
M3[LOAD]
M4[COUNT]
CT=0
54F569
3,5D
10



The 54TTL and ANSI 54TTL Libraries

The 54TTL Library requires approximately 1171 Kbytes of disk storage, and the ANSI 54TTL Library requires approximately 1231 Kbytes of disk storage. The physical, timing, and simulation models for each library are identical and differ only in their body drawings. The part name for a component in either library is the same; the body drawing used is determined by the first library name encountered in the library search path (*54ttl.lib* or *a54ttl.lib*).

The specifications used to construct the models in these libraries were taken from either the Texas Instruments data books or from Mil Spec MIL-M-38510. Parts identified with an asterisk (*) are from MIL-M-38510; the descriptions for these components include the military device type in parentheses.

The release level of the 54TTL and ANSI 54TTL Libraries is 9.0.

Each library contains body drawings and physical, timing, and simulation models for the following 35 components:

* 5400	Quad 2-input positive NAND gate (00104)
* 5404	Hex inverter (00105)
* 5406	Hex inverter buffer/driver with open collector output (00801)
* 5407	Hex buffer/driver with open collector output (00803)
* 5408	Quad 2-input positive AND gate (01601)
* 5410	Triple 3-input positive NAND gate (00103)
* 5416	Hex inverter buffer/drivers with open collector high-voltage outputs (00802)
* 5417	Hex buffer/driver with open collector output (00804)
* 5425	Dual 4-input positive NOR gate with strobe (00403)
* 5428	Quad 2-input positive NOR gate (16201)
* 5432	Quad 2-input positive OR gate (16101)
5433	Quad 2-input NOR buffers with open collector output
* 5445	BCD to decimal decoder (01004)
* 5447	BCD to 7-segment decoder (01007)
* 5470	AND-gated JK positive edge triggered flip-flop with preset and clear (00206)

5480	Gated full adders
5481	Gated full adders
* 5482	2-bit binary full adders (00601)
5494	4-bit shift registers
* 54116	Dual 4-bit latches (01503)
54120	Dual pulse synchronizers/drivers
* 54121	Monostable multivibrators (01201)
* 54123	Dual retriggerable monostable multivibrators with clear (01203)
54128	50-ohm line driver
* 54150	1-of-16 data selector/multiplexer (01401)
* 54154	4-to-16 line decoder/demultiplexer (15201)
54159	4-to-16 line decoder/demultiplexer
54176	35-MHz presettable decade counters/latches
54177	35-MHz presettable binary counters/latches
54179	4-bit universal shift registers
54185	Binary-to-BCD converter
54198	8-bit bidirectional universal shift registers
54265	Quad complementary output elements
54273	Octal D-type flip-flop
54376	Quad JK flip-flops

Application Notes

Monostable Multivibrators

The 74121, 74122, and 74123 models fully support the simulation and timing behavior of a retrigerrable multivibrator – infinite retriggering edges and external resettability at any time.

To use the simulation model, logic initialization or initial depositing of the same value (either 0 or 1) to internal signals D0 and D1 must be performed.

To use the timing verification model, the following must be observed:

- The Timing Verifier's directives file *(verifier.cmd)* must include the directive:

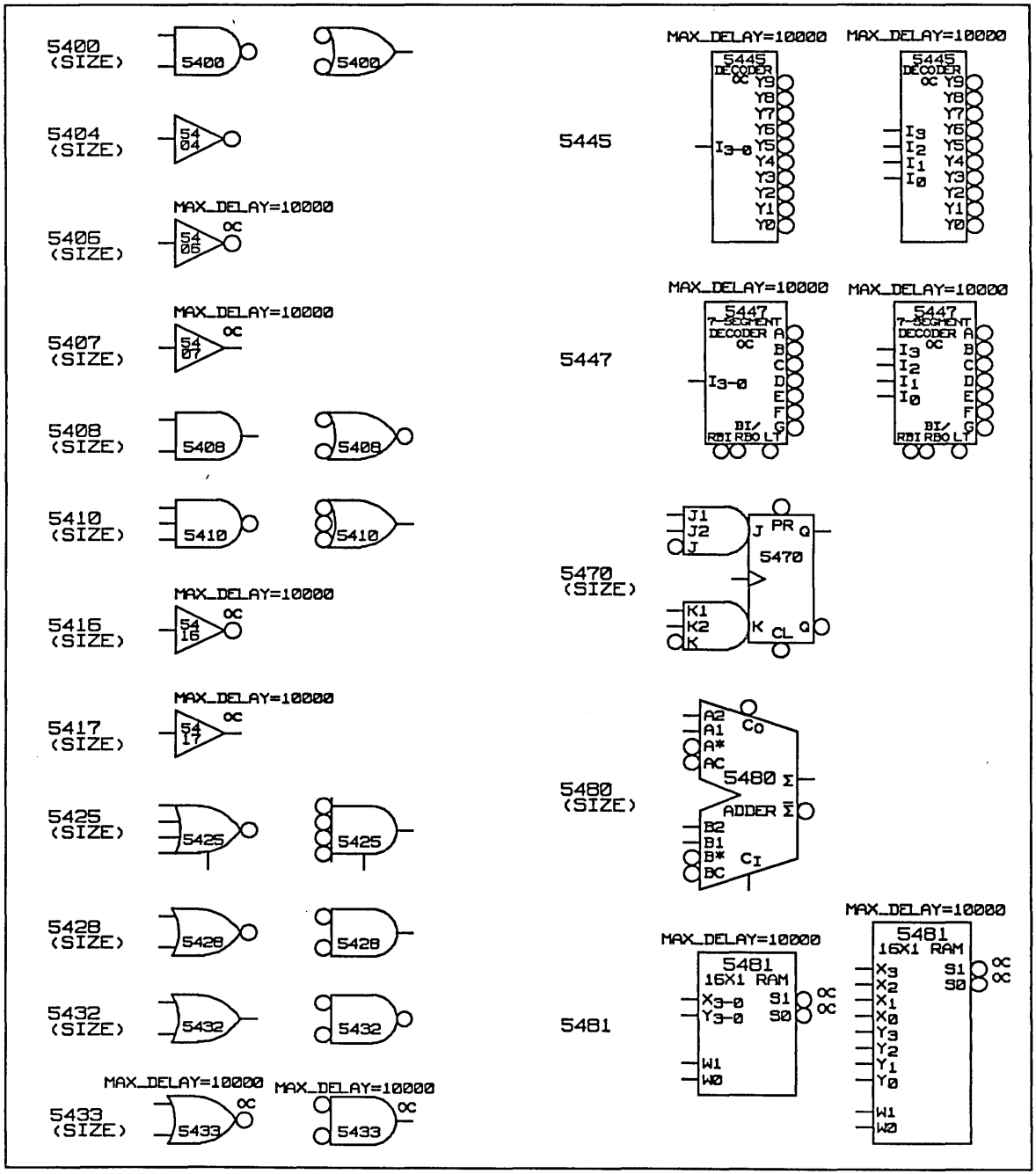
  ```
  LATCH_ERR_MODEL CLOSED;
  ```

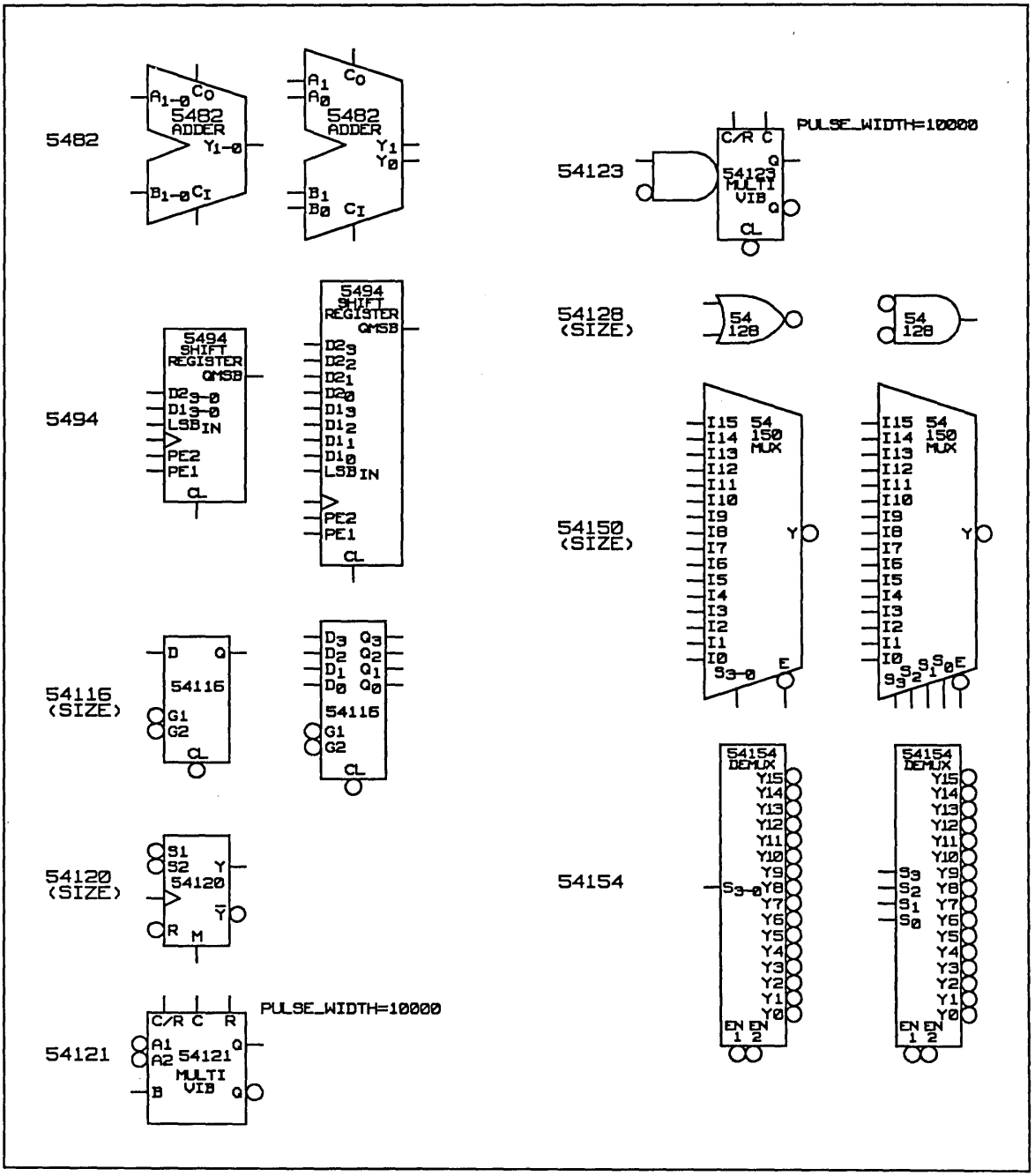
- The first trigger edge must occur after 'PULSE_WIDTH' ns.

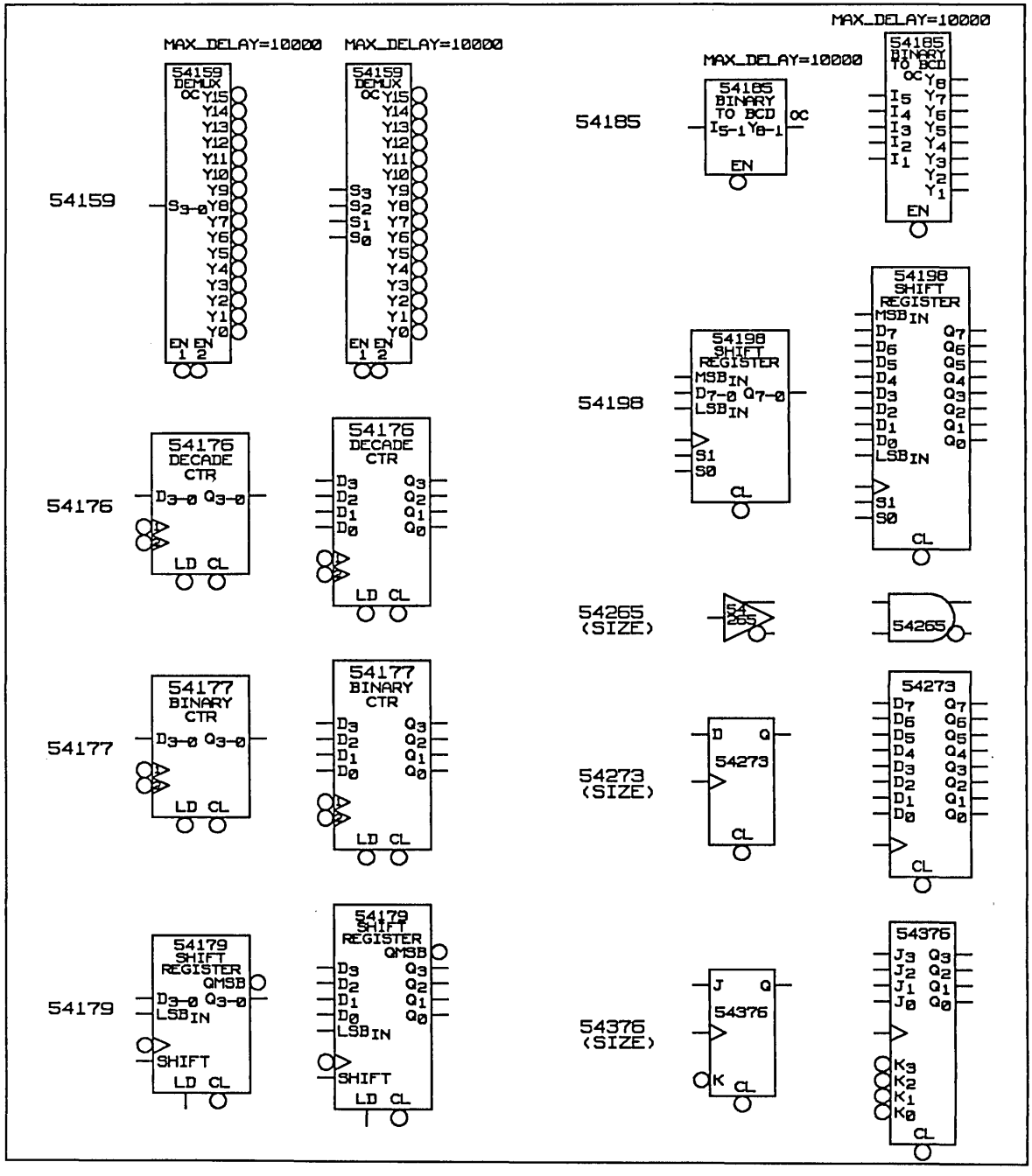
- The maximum trigger frequency is

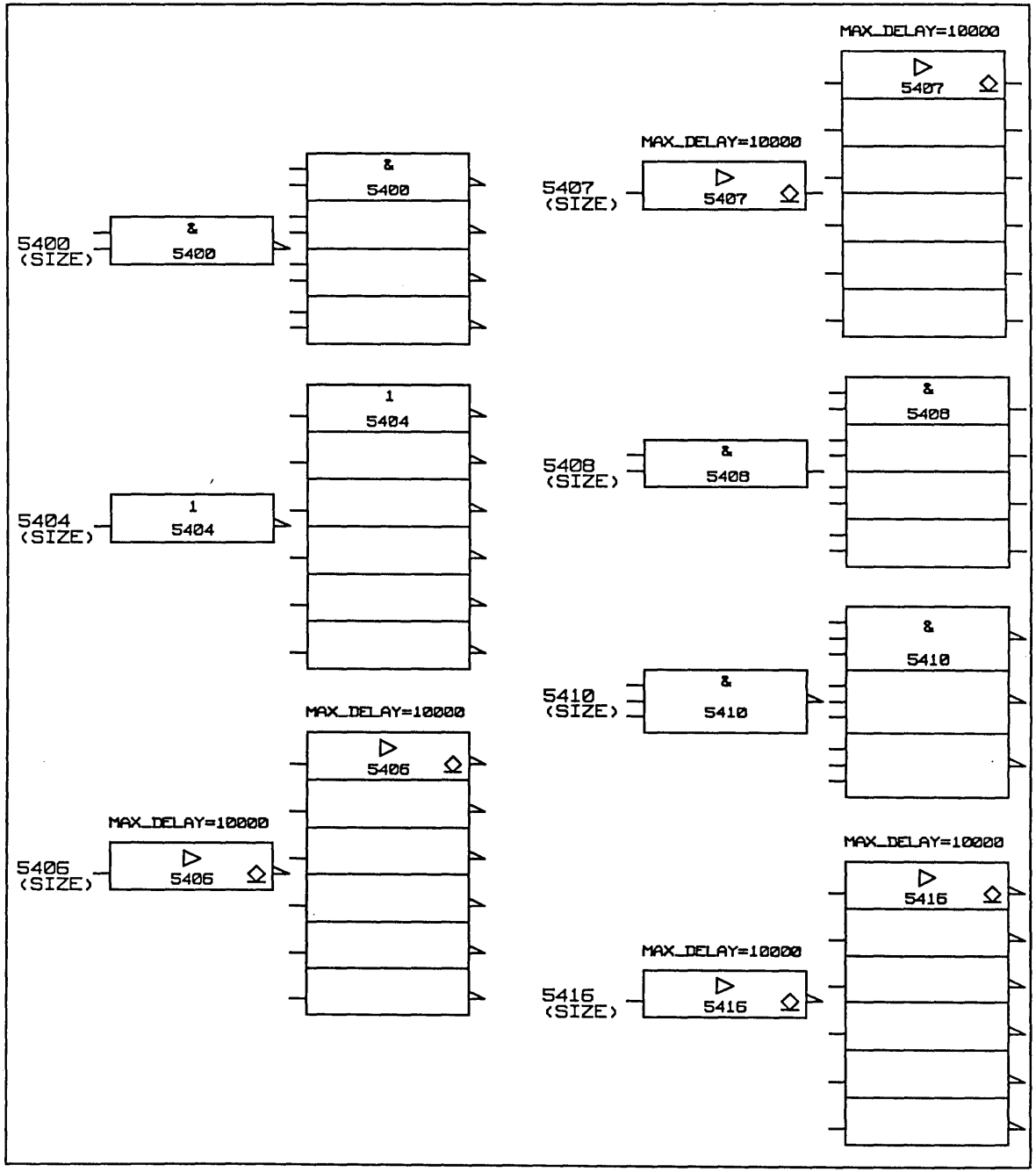
  ```
  2 * RETRIG_DIV2 -1
  ```

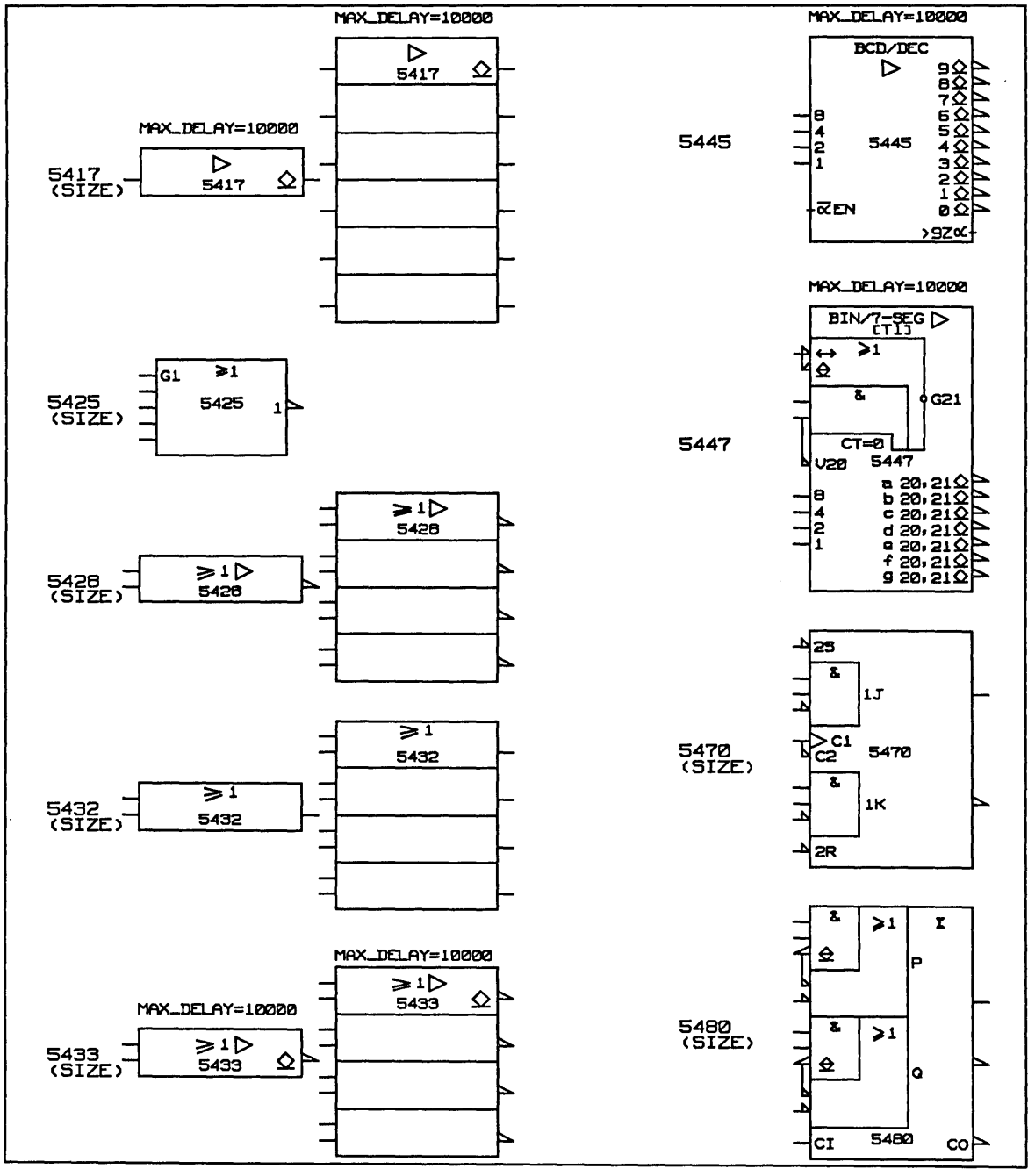
  edges per 'PULSE_WIDTH' ns. Since RETRIG_DIV2 is defined to be 6 in the model, 2*6-1=11 clock edges are permitted in any 'PULSE_WIDTH' ns interval. If an application requires a greater trigger frequency, RETRIG_DIV2 must be redefined in the model.

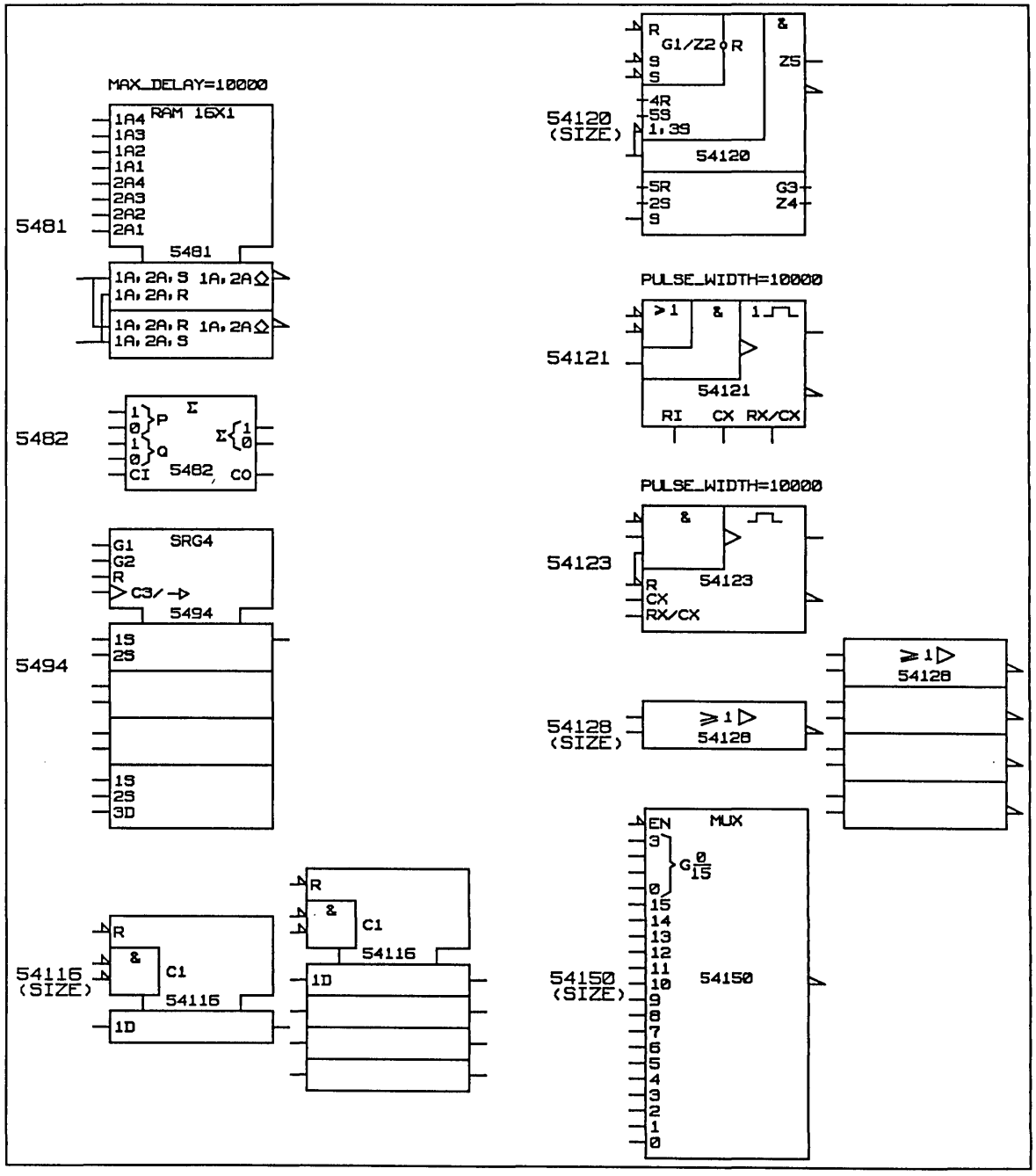

5400 (SIZE)
5400
5400
5404 (SIZE)
54 04
MAX_DELAY=10000
5406 (SIZE)
54 06
MAX_DELAY=10000
5407 (SIZE)
54 07
5408 (SIZE)
5408
5408
5410 (SIZE)
5410
5410
MAX_DELAY=10000
5416 (SIZE)
54 16
MAX_DELAY=10000
5417 (SIZE)
54 17
5425 (SIZE)
5425
5425
5428 (SIZE)
5428
5428
5432 (SIZE)
5432
5432
MAX_DELAY=10000
MAX_DELAY=10000
5433 (SIZE)
5433
5433
5445
MAX_DELAY=10000
5445 DECODER
I3-0
Y9 Y8 Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0
MAX_DELAY=10000
5445 DECODER
I3 I2 I1 I0
Y9 Y8 Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0
5447
MAX_DELAY=10000
5447 7-SEGMENT DECODER
I3-0
A B C D E F G
BI/RBI RBO LT
MAX_DELAY=10000
5447 7-SEGMENT DECODER
I3 I2 I1 I0
A B C D E F G
BI/RBI RBO LT
5470 (SIZE)
J1 J2 J
PR Q
5470
K1 K2 K
CL Q
5480 (SIZE)
A2 A1 A* AC
CO
5480 Σ
ADDER Σ̄
B2 B1 B* BC
CI
5481
MAX_DELAY=10000
5481 16X1 RAM
X3-0 Y3-0
S1 S0
W1 W0
MAX_DELAY=10000
5481 16X1 RAM
X3 X2 X1 X0 Y3 Y2 Y1 Y0
S1 S0
W1 W0

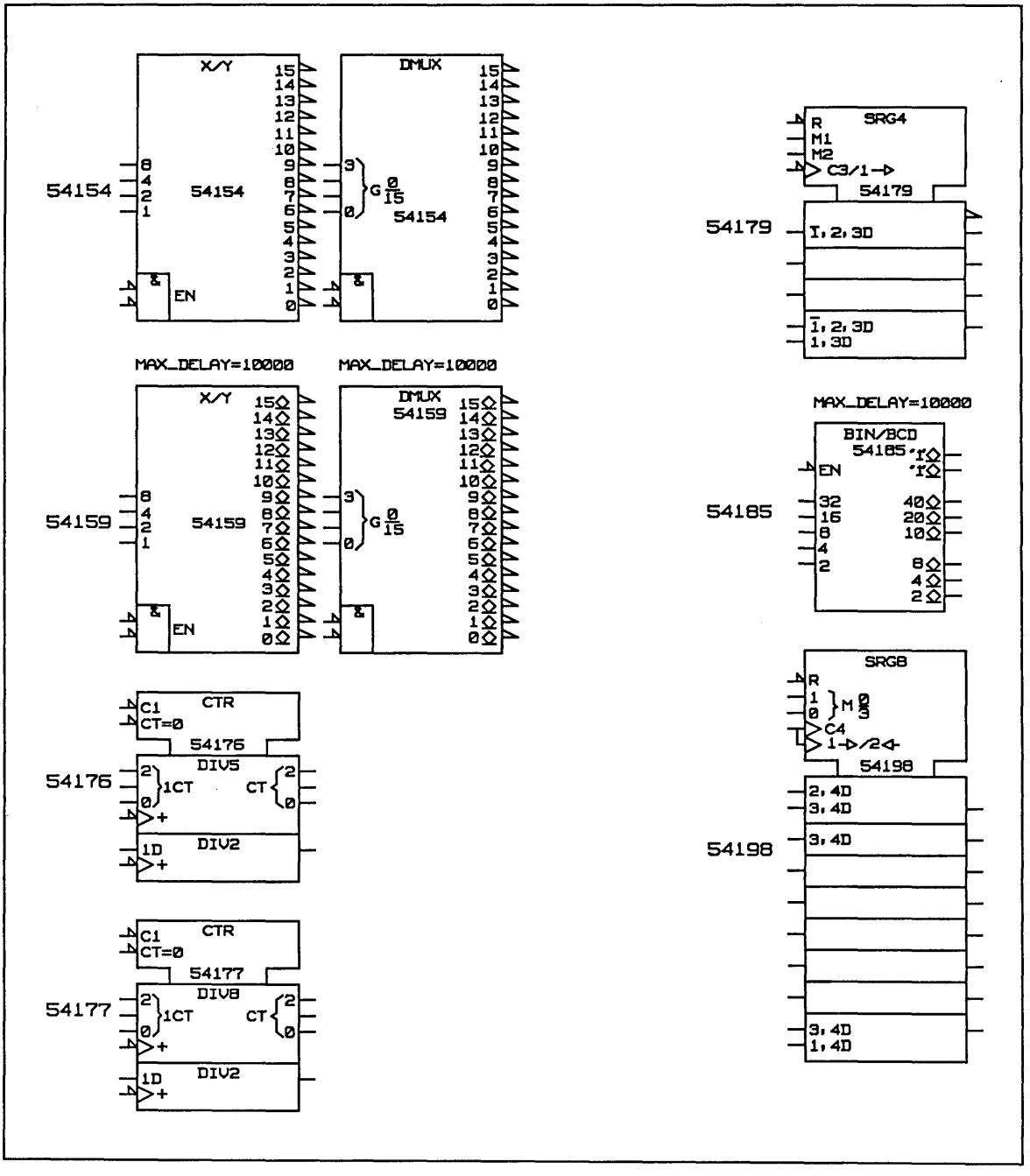

5482
5482 ADDER
5482 ADDER
5494
5494 SHIFT REGISTER
5494 SHIFT REGISTER
54116 (SIZE)
54116
54116
54120 (SIZE)
54120
54121
PULSE_WIDTH=10000
54123
PULSE_WIDTH=10000
54123 MULTI VIB
54128 (SIZE)
54 128
54 128
54150 (SIZE)
54 150 MUX
54 150 MUX
54154
54154 DEMUX
54154 DEMUX

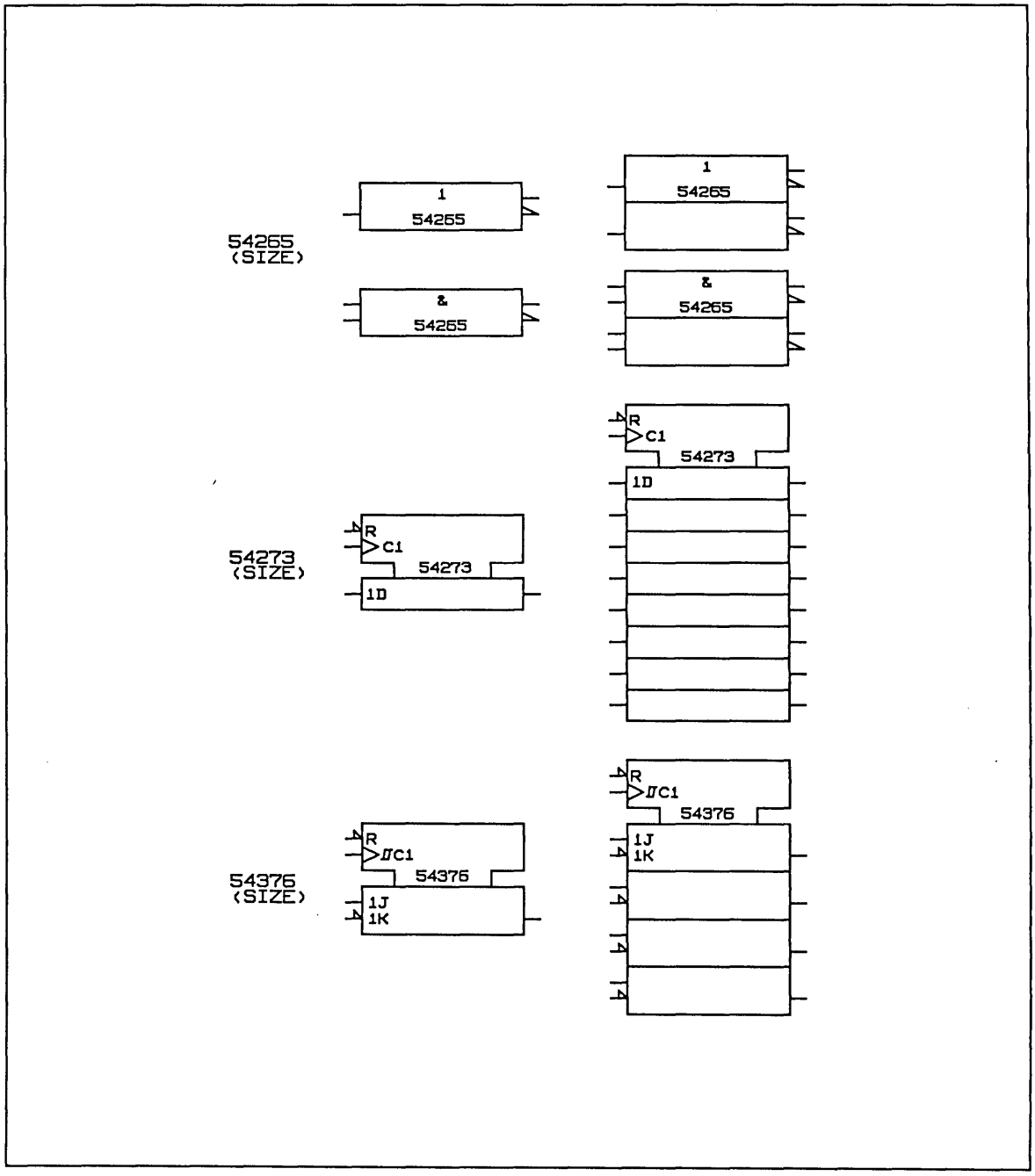

MAX_DELAY=10000
MAX_DELAY=10000
MAX_DELAY=10000
MAX_DELAY=10000
54159
54159
DEMUX
OC Y15
Y14
Y13
Y12
Y11
Y10
Y9
S3-0 Y8
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
EN EN
1 2
54159
DEMUX
OC Y15
Y14
Y13
Y12
Y11
Y10
Y9
S3
S2
S1
S0
Y8
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
EN EN
1 2
54185
54185
BINARY
TO BCD
OC
I5-1 Y8-1
EN
54185
BINARY
TO BCD
OC Y8
I5 Y7
I4 Y6
I3 Y5
I2 Y4
I1 Y3
Y2
Y1
EN
54176
54176
DECADE
CTR
D3-0 Q3-0
LD CL
54176
DECADE
CTR
D3 Q3
D2 Q2
D1 Q1
D0 Q0
LD CL
54198
54198
SHIFT
REGISTER
MSBIN
D7-0 Q7-0
LSBIN
S1
S0
CL
54198
SHIFT
REGISTER
MSBIN
D7 Q7
D6 Q6
D5 Q5
D4 Q4
D3 Q3
D2 Q2
D1 Q1
D0 Q0
LSBIN
S1
S0
CL
54265
(SIZE)
54265
54265
54177
54177
BINARY
CTR
D3-0 Q3-0
LD CL
54177
BINARY
CTR
D3 Q3
D2 Q2
D1 Q1
D0 Q0
LD CL
54273
(SIZE)
D Q
54273
CL
54273
D7 Q7
D6 Q6
D5 Q5
D4 Q4
D3 Q3
D2 Q2
D1 Q1
D0 Q0
CL
54179
54179
SHIFT
REGISTER
QMSB
D3-0 Q3-0
LSBIN
SHIFT
LD CL
54179
SHIFT
REGISTER
QMSB
D3 Q3
D2 Q2
D1 Q1
D0 Q0
LSBIN
SHIFT
LD CL
54376
(SIZE)
J Q
54376
K CL
54376
J3 Q3
J2 Q2
J1 Q1
J0 Q0
K3
K2
K1
K0
CL

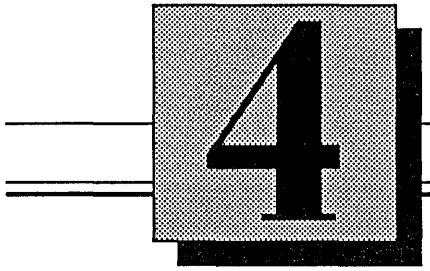

&
5400
5400
(SIZE)
&
5400
1
5404
5404
(SIZE)
1
5404
MAX_DELAY=10000
5406
MAX_DELAY=10000
5406
(SIZE)
5406
MAX_DELAY=10000
5407
5407
(SIZE)
MAX_DELAY=10000
5407
&
5408
5408
(SIZE)
&
5408
&
5410
5410
(SIZE)
&
5410
MAX_DELAY=10000
5415
MAX_DELAY=10000
5416
(SIZE)
5416


MAX_DELAY=10000
5417
MAX_DELAY=10000
5417
5417
(SIZE)
5425
(SIZE)
G1
≥1
5425
1
5428
(SIZE)
≥1
5428
5432
(SIZE)
≥1
5432
MAX_DELAY=10000
5433
(SIZE)
MAX_DELAY=10000
5445
BCD/DEC
5445
MAX_DELAY=10000
5447
BIN/7-SEG
[TTL]
G21
CT=0
V20
5447
a 20,21
b 20,21
c 20,21
d 20,21
e 20,21
f 20,21
g 20,21
5470
(SIZE)
2S
1J
C1
C2
5470
1K
2R
5480
(SIZE)
P
Q
CI
5480
CO


MAX_DELAY=10000
RAM 16X1
1A4
1A3
1A2
1A1
2A4
2A3
2A2
2A1
5481
1A, 2A, S
1A, 2A, R
1A, 2A, R
1A, 2A, S
5482
CI
CO
SRG4
G1
G2
R
C3/→
5494
1S
2S
3D
54116
(SIZE)
C1
1D
54120
(SIZE)
G1/Z2
Z5
4R
5S
1,3S
G3
Z4
5R
2S
PULSE_WIDTH=10000
54121
RI
CX
RX/CX
54123
54128
(SIZE)
MUX
54150
(SIZE)


54154
X/Y
54154
EN
DMUX
54154
MAX_DELAY=10000
54159
X/Y
54159
EN
DMUX
54159
MAX_DELAY=10000
54176
CTR
54176
DIV5
DIV2
54177
CTR
54177
DIV8
DIV2
54179
SRG4
54179
54185
MAX_DELAY=10000
BIN/BCD
54185
54198
SRG8
54198

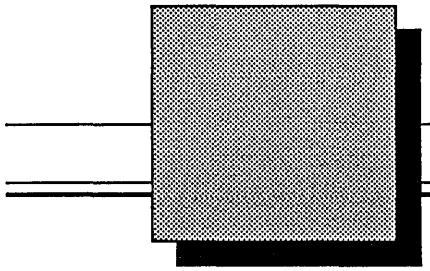

54265
(SIZE)
1
54265
&
54265
1
54265
&
54265
54273
(SIZE)
R
C1
54273
1D
R
C1
54273
1D
54376
(SIZE)
R
C1
54376
1J
1K
R
C1
54376
1J
1K



Miscellaneous Libraries

This section describes the miscellaneous libraries available from Valid. Note that both standard and ANSI body styles are available with the MEMORY Library; when both libraries are included, the body style selected is determined by the first library name encountered in the library search path or by the last **library** command.

Contents



The CMOS Library

The CMOS Library requires approximately 4327 Kbytes of disk storage. The specifications used to construct the models in this library were taken from the following data books:

- Motorola
- RCA
- National
- Fairchild

The data books were used in the order listed. If the part was not in Motorola, it was taken from RCA. If it was not in either Motorola or RCA, it was taken from National, and so on.

The release level of the CMOS Library is 9.0.

The library contains bodies and physical, simulation, and timing models for the following 106 components:

4000UB	Quad 2-input NAND
4001B	Quad 2-input NOR
4002B	Dual 4-input NOR
4006B	18-bit static shift register
4008B	4-bit full adder
4011B	Quad 2-input NAND
4012B	Dual 4-input NAND
4013B	Dual D flip-flop
4014B	8-bit static shift register
4015B	Dual 5-bit static shift register
4016B	Quad analog switch/quad multiplexer
4017B	Decade counter/divider
4018B	Presettable divide-by-N counter
4019B	Quad AND/OR select
4020B	14-bit binary counter
4021B	8-bit static shift register
4022B	Octal counter/divider
4023B	Triple 3-input NAND
4024B	7-stage ripple counter
4025B	Triple 3-input NOR
4027B	Dual JK flip-flop
4028B	BCD-to-decimal decoder
4029B	4-bit presettable up/down counter
4030B	Quad exclusive-OR
4032B	Triple serial adder

4034B	8-bit universal bus register
4035B	4-bit shift register
4038B	Triple serial adder
4040B	12-bit binary counter
4042B	Quad latch
4043B	Quad NOR R-S latch
4047B	Monostable/astable multivibrator
4049UB	Hex inverter/buffer
4050B	Hex buffer
4051B	8-channel analog multiplexer
4052B	Dual 4-channel analog multiplexer
4053B	Triple 2-channel analog multiplexer
4060B	14-stage ripple-carry binary counter/divider
4066B	Quad analog switch
4067B	Multiplexer/demultiplexer
4068B	8-input NAND
4069UB	Hex inverter
4070B	Quad exclusive-OR
4071B	Quad 2-input OR
4072B	Dual 4-input OR
4073B	Triple 3-input AND
4075B	Triple 3-input OR
4076B	Quad D-type register
4077B	Quad exclusive-NOR
4078B	8-input NOR

4081B	Quad 2-input AND
4082B	Dual 4-input AND
4093B	Quad 2-input NAND Schmitt trigger
4094B	8-bit bus compatible shift store latch
4098B	Dual monostable multivibrator
4099B	8-bit addressable latch
4160B	Decade counter with asynchronous clear
4161B	Binary counter with asynchronous clear
4162B	Decade counter with synchronous clear
4163B	Binary counter with synchronous clear
4174B	Hex D flip-flop
4175B	Quad D flip-flop
4502B	Strobed hex inverter/buffer
4503B	Hex 3-state buffer
4504B	Hex TTL or CMOS to CMOS level shifter
4508B	Dual 4-bit latch
4510B	BCD up/down counter
4511B	BCD to 7-segment latch/decoder/driver
4512B	8-channel data selector
4514B	4-bit latch/4-to-16 line decoder
4515B	4-bit latch/4-to-16 line decoder
4516B	Binary up/down counter
4517B	Dual 64-bit static shift register
4519B	4-bit AND/OR selector
4520B	Dual binary up counter

4526B	Programmable binary divide-by-N counter
4528B	Dual monostable multivibrator
4529B	Dual 4-channel analog data selector
4530B	Dual 5-input majority logic gate
4532B	8-bit priority encoder
4538B	Dual precision monostable multivibrator
4539B	Dual 4-channel data selector/multiplexer
4549B	Successive approximation register
4551B	Quad 2-input analog mux/demultiplexer
4552B	64 x 4 bit static RAM
4555B	Dual binary to 1-of-4 decoder
4556B	Dual binary to 1-of-4 decoder
4557B	1-to-64 bit variable length shift register
4559B	Successive approximation register
4562B	128-bit static shift register
4572UB	Hex gate
4584B	Hex Schmitt trigger
4585B	4-bit magnitude comparator
4599B	8-bit addressable latch
4724B	8-bit addressable latch
40085B	4-bit magnitude comparator
40103B	8-stage presettable synchronous down counter
40105B	FIFO register
40109B	Quad low-to-high voltage level shifter
40161B	Binary counter with asynchronous clear

40162B	Decade counter with synchronous clear
40163B	Binary counter with synchronous clear
40174B	Hex D flip-flop
40175B	Quad D flip-flop
40192B	BCD up/down counter
40193B	Binary up/down counter

Application Notes

Monostable Multivibrators

The 4098B and 4047B models fully support the simulation and timing behavior of a retrigerrable multivibrator – infinite retriggering edges and external resettability at any time.

To use the simulation model, logic initialization or initial depositing of the same value (either 0 or 1) to internal signals D0 and D1 must be performed.

To use the timing verification model, the following must be observed:

- The Timing Verifier's directives file *(verifier.cmd)* must include the directive:

  ```
  LATCH_ERR_MODEL CLOSED;
  ```

- The first trigger edge must occur after 'PULSE_WIDTH' ns.

- The maximum trigger frequency is

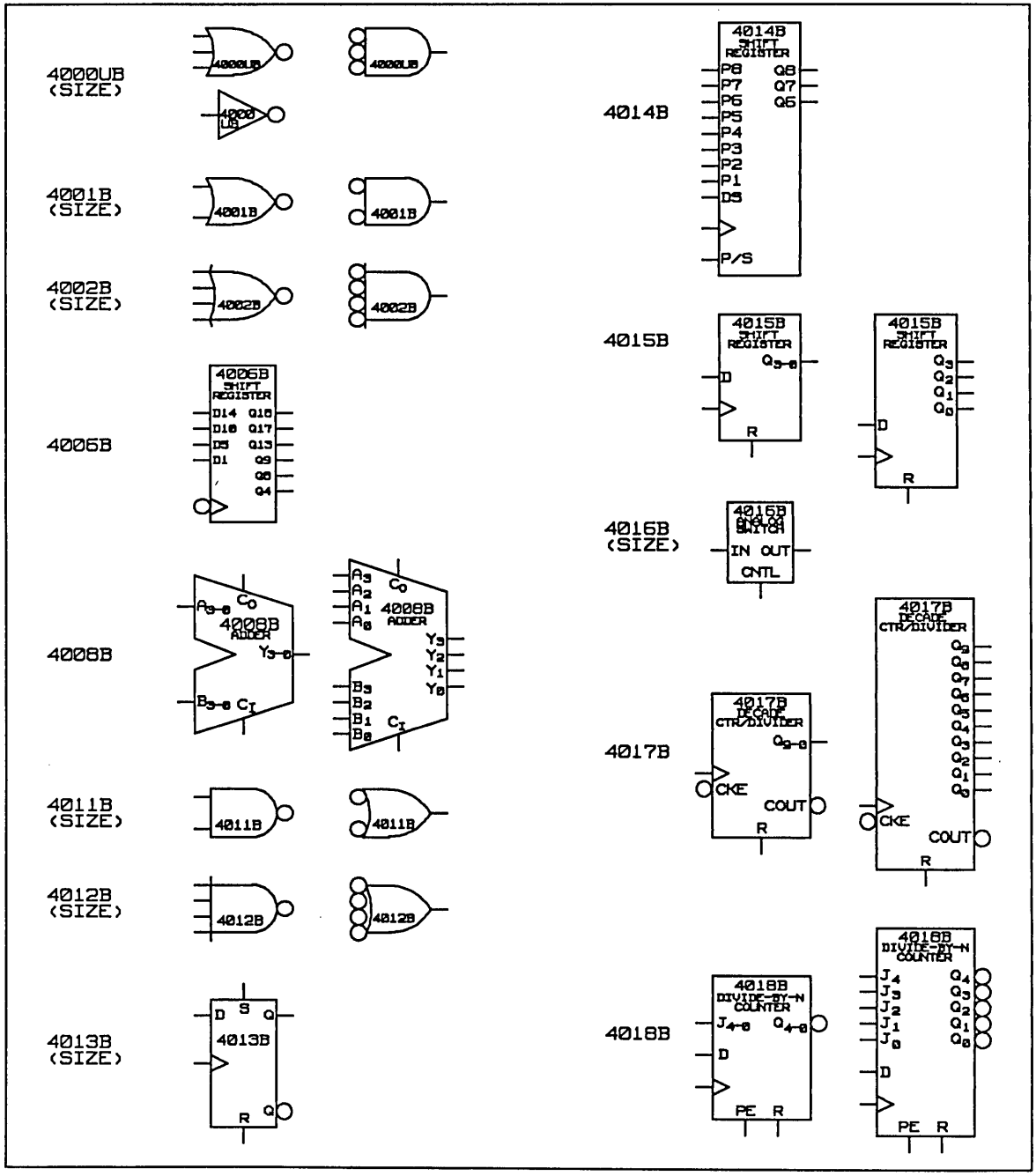
  ```
  2 * RETRIG_DIV2 -1
  ```

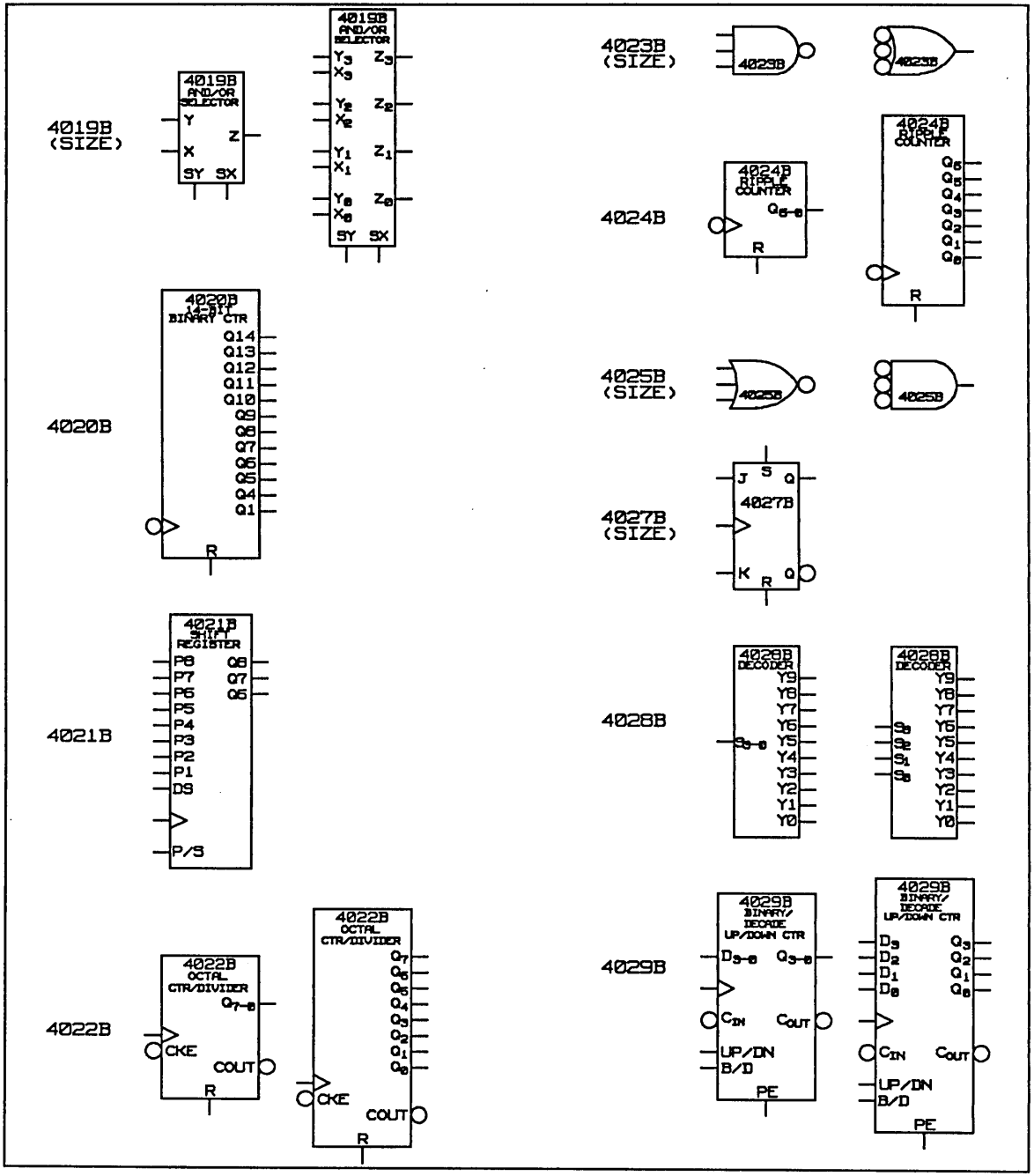
  edges per 'PULSE_WIDTH' ns. Since RETRIG_DIV2 is defined to be 6 in the model, 2*6–1=11 clock edges are permitted in any 'PULSE_WIDTH' ns interval. If an application requires a greater trigger frequency, RETRIG_DIV2 must be redefined in the model.

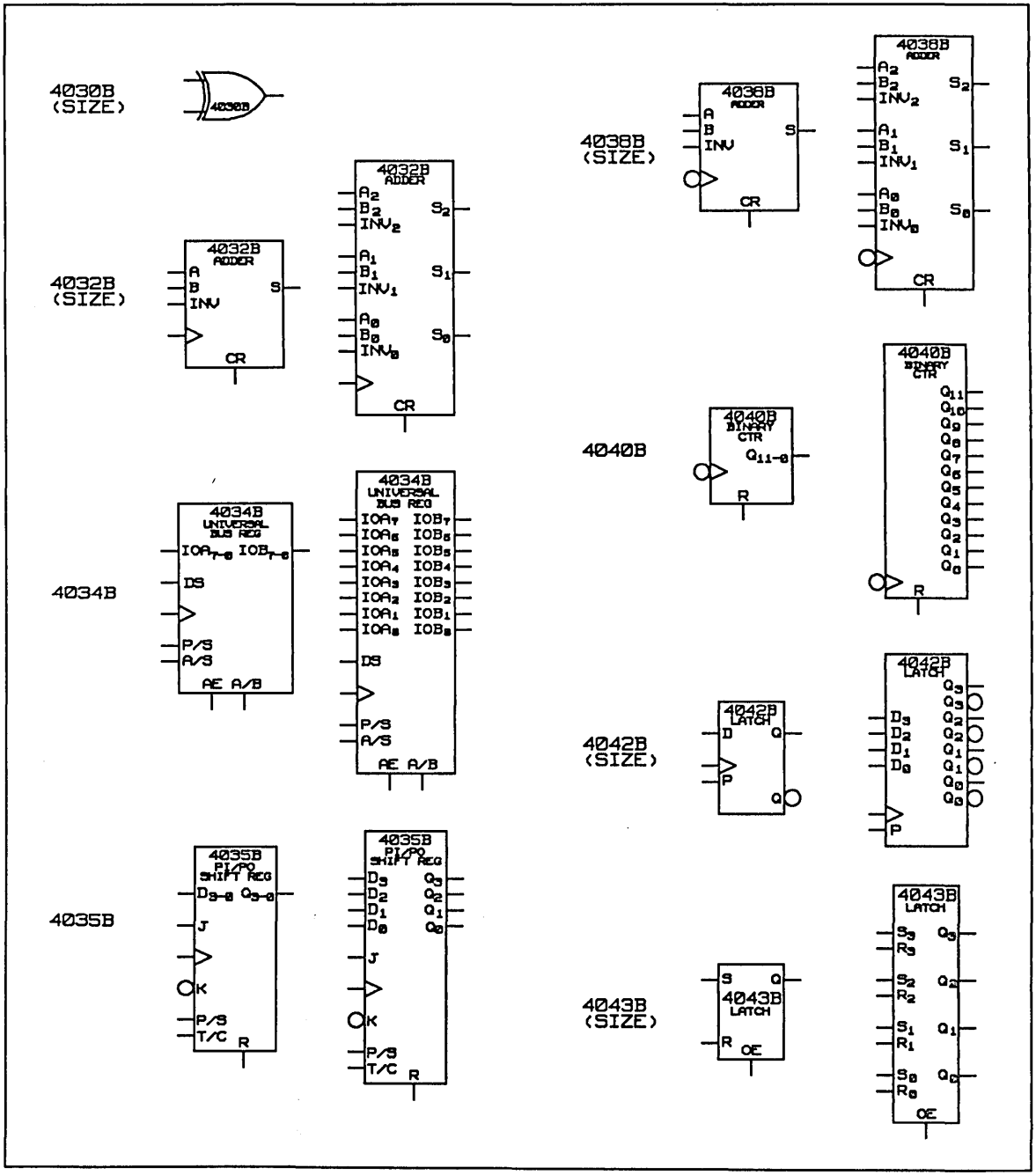
Successive Approximation Registers

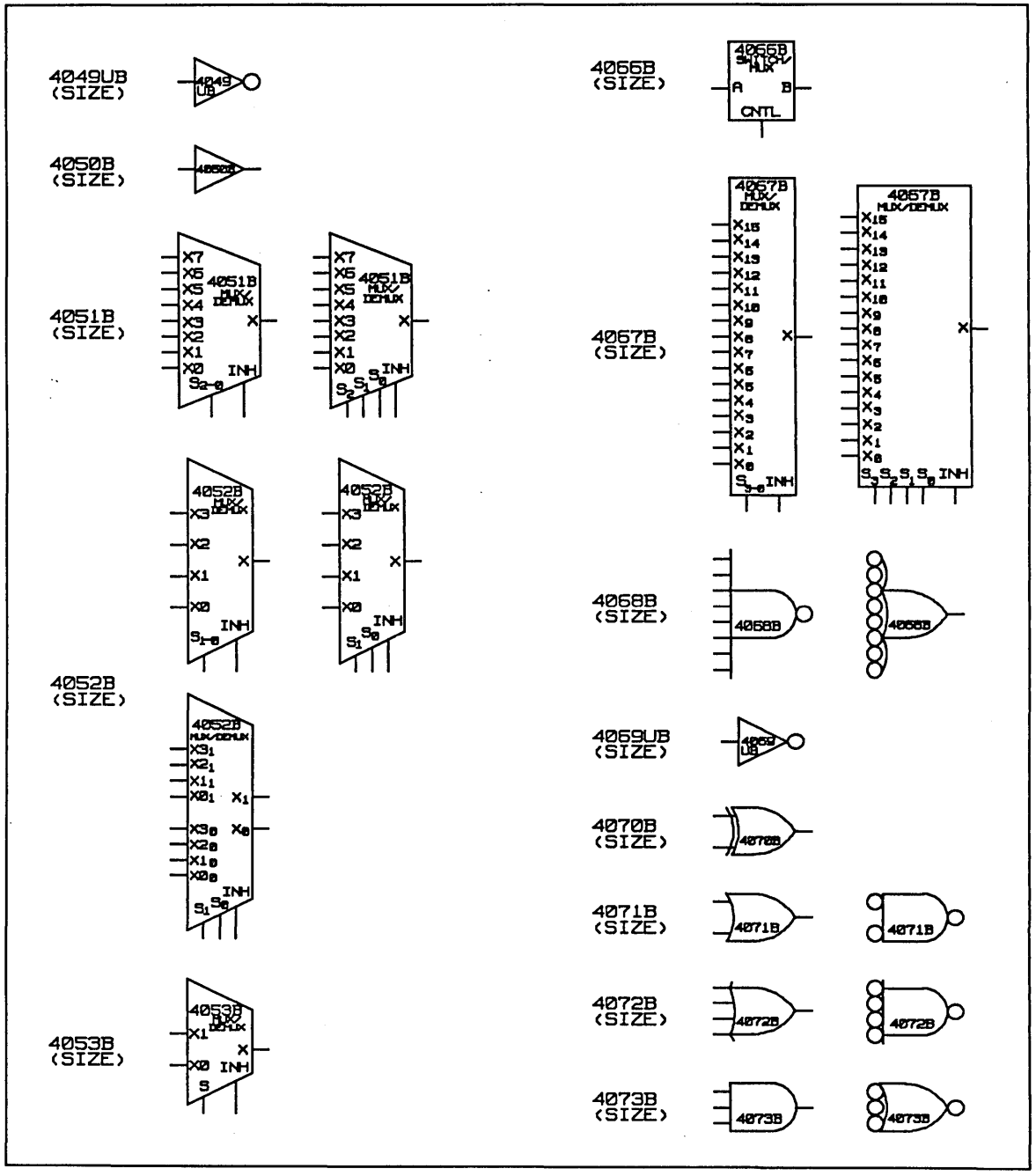
To use the timing verification model for the 4549B or 4559B successive approximation registers, the Timing Verifier's directive file *(verifier.cmd)* must include the directive:

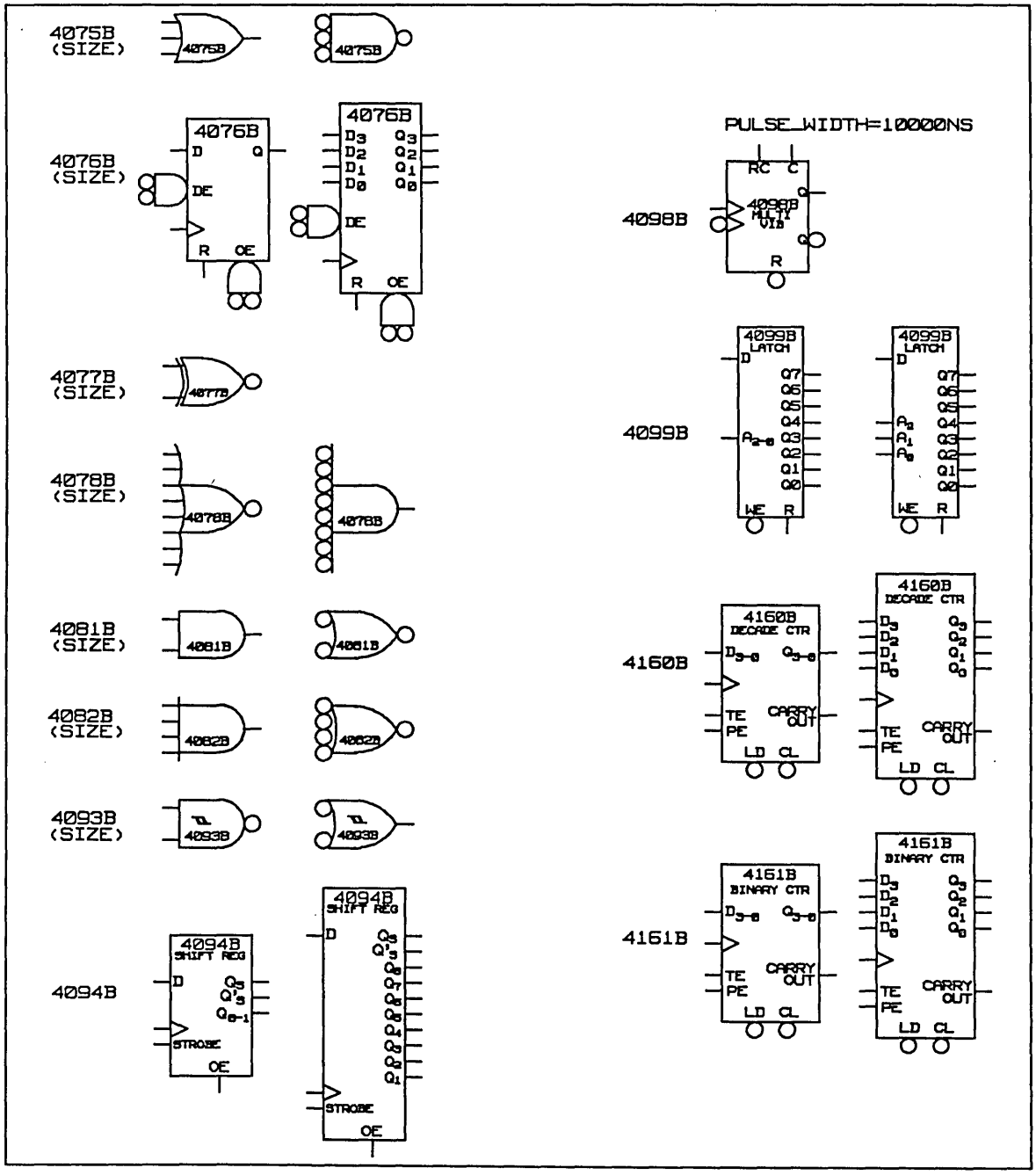
```
LATCH_ERR_MODEL CLOSED;
```

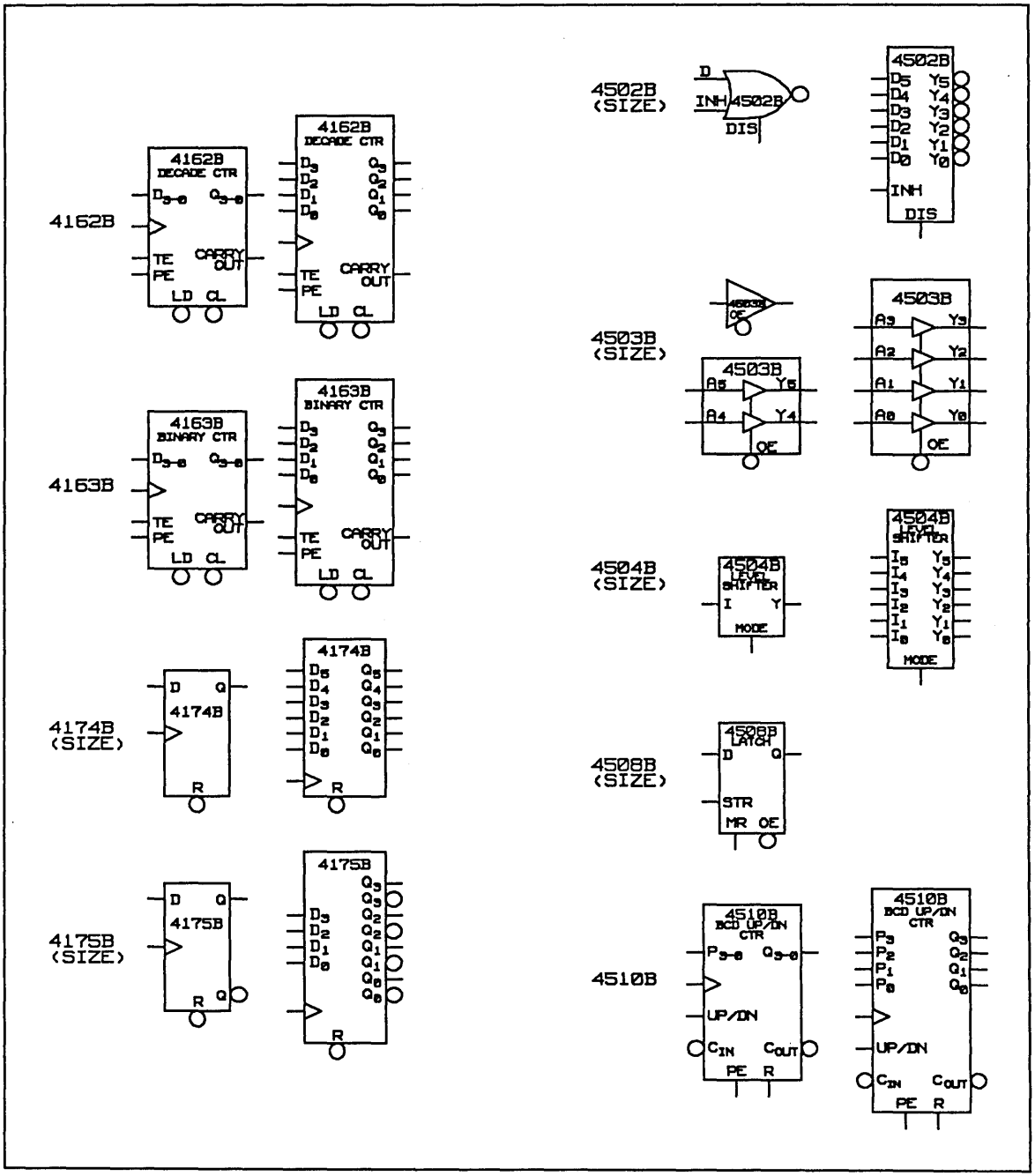

4000UB (SIZE)
4001B (SIZE)
4002B (SIZE)
4006B
4008B
4011B (SIZE)
4012B (SIZE)
4013B (SIZE)
4014B
4015B
4016B (SIZE)
4017B
4018B
4014B SHIFT REGISTER
P8 P7 P6 P5 P4 P3 P2 P1 DS P/S
Q8 Q7 Q6 Q5
4015B SHIFT REGISTER
D R
4016B ANALOG SWITCH
IN OUT CNTL
4017B DECADE CTR/DIVIDER
CKE COUT R
4018B DIVIDE-BY-N COUNTER
PE R
4006B SHIFT REGISTER
4008B ADDER
4013B

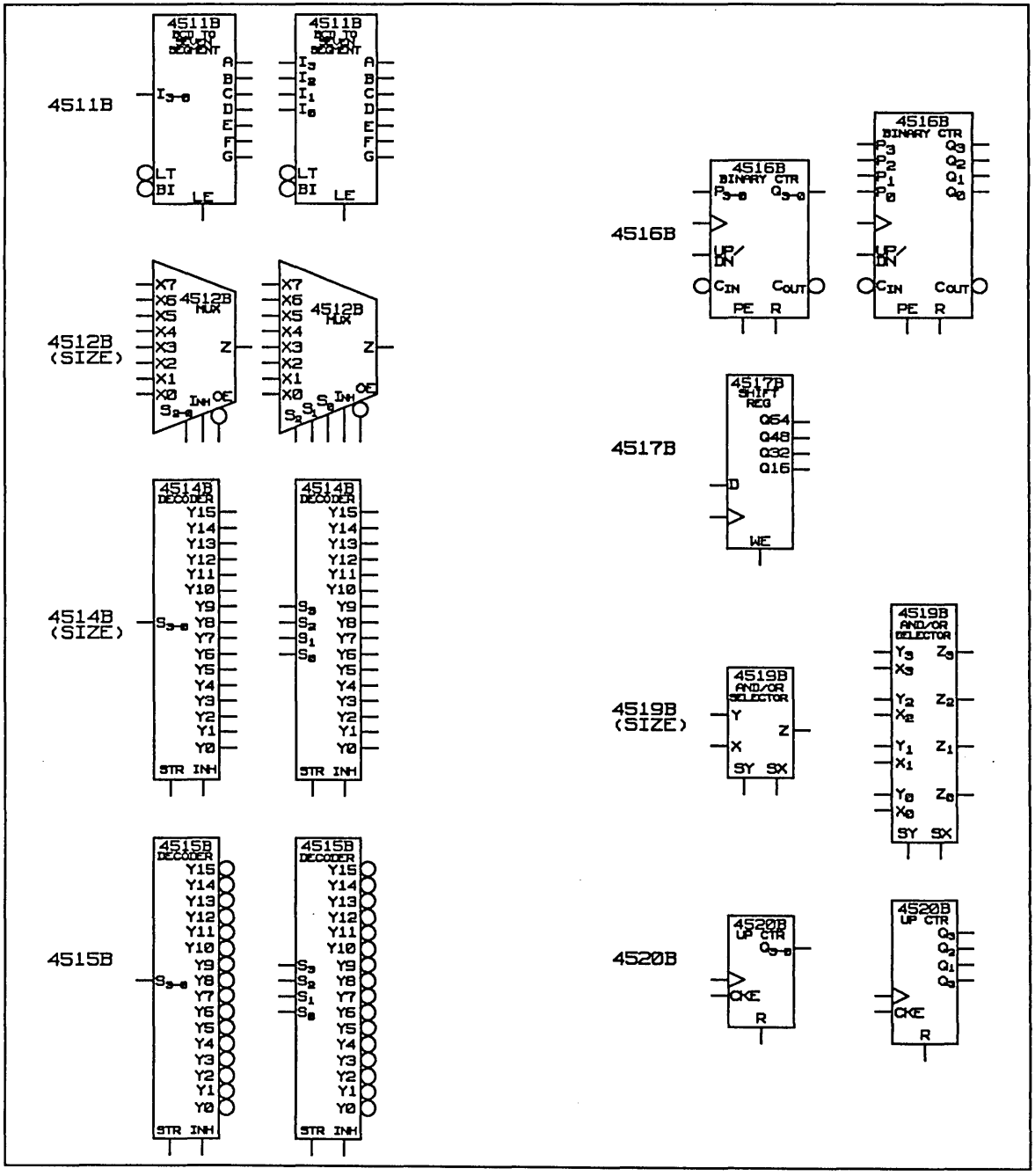

4019B (SIZE)
4019B AND/OR SELECTOR
Y Z X SY SX
4019B AND/OR SELECTOR
Y3 Z3 X3 Y2 Z2 X2 Y1 Z1 X1 Y0 Z0 X0 SY SX
4020B
4020B 14-BIT BINARY CTR
Q14 Q13 Q12 Q11 Q10 Q9 Q8 Q7 Q6 Q5 Q4 Q1 R
4021B
4021B SHIFT REGISTER
P8 P7 P6 P5 P4 P3 P2 P1 DS Q8 Q7 Q6 P/S
4022B
4022B OCTAL CTR/DIVIDER
Q7-0 CKE COUT R
4022B OCTAL CTR/DIVIDER
Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0 CKE COUT R
4023B (SIZE)
4023B
4024B
4024B RIPPLE COUNTER
Q5-0 R
4024B RIPPLE COUNTER
Q6 Q5 Q4 Q3 Q2 Q1 Q0 R
4025B (SIZE)
4025B
4027B (SIZE)
4027B
J S Q K R Q
4028B
4028B DECODER
D3-0 Y9 Y8 Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0
4029B
4029B BINARY/ DECADE UP/DOWN CTR
D3-0 Q3-0 CIN COUT UP/DN B/D PE
4029B BINARY/ DECADE UP/DOWN CTR
D3 D2 D1 D0 Q3 Q2 Q1 Q0 CIN COUT UP/DN B/D PE

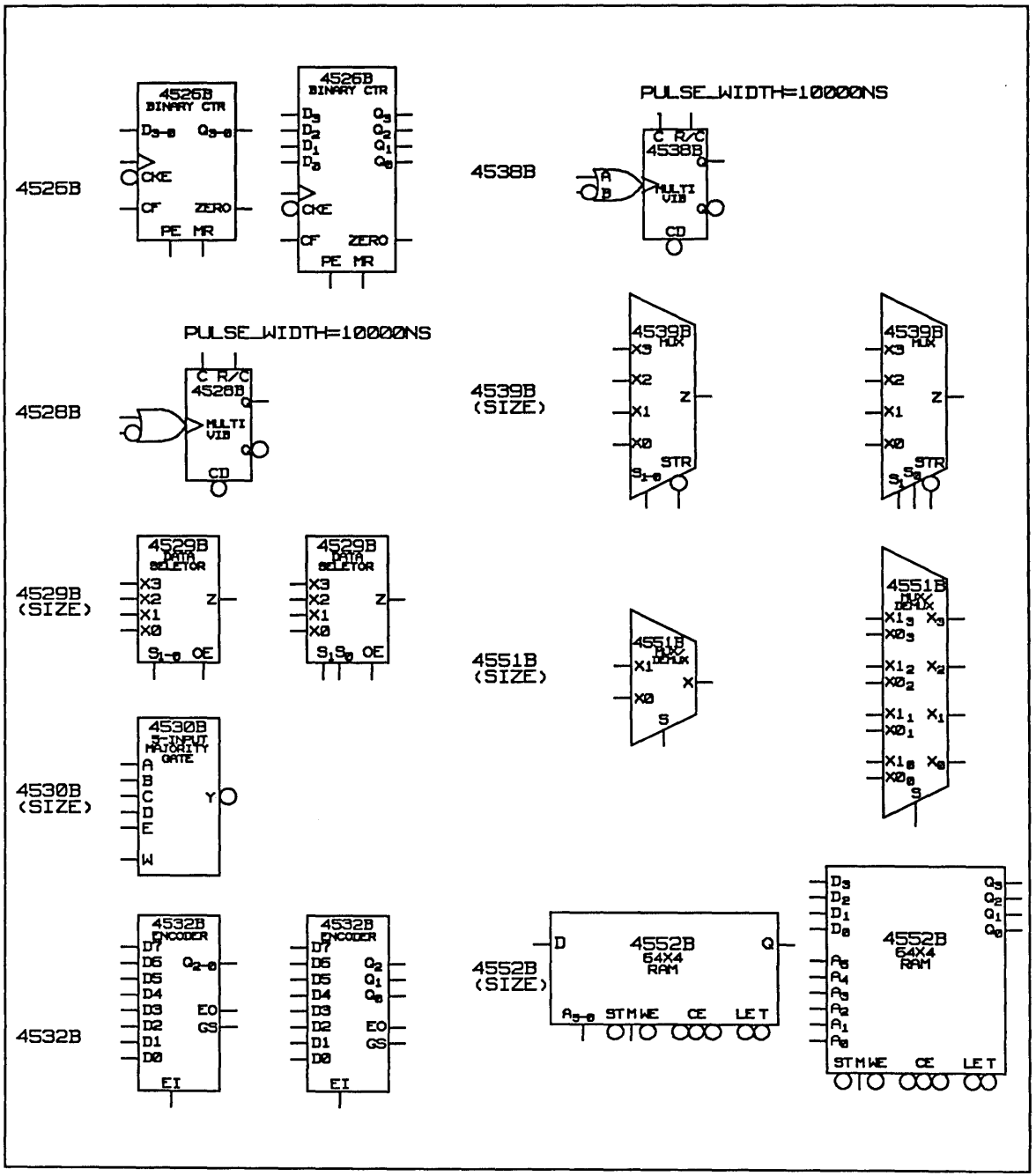

4030B
(SIZE)
4032B
(SIZE)
4034B
4035B
4038B
(SIZE)
4040B
4042B
(SIZE)
4043B
(SIZE)
ADDER
UNIVERSAL BUS REG
PIPO SHIFT REG
BINARY CTR
LATCH
CR
R
OE

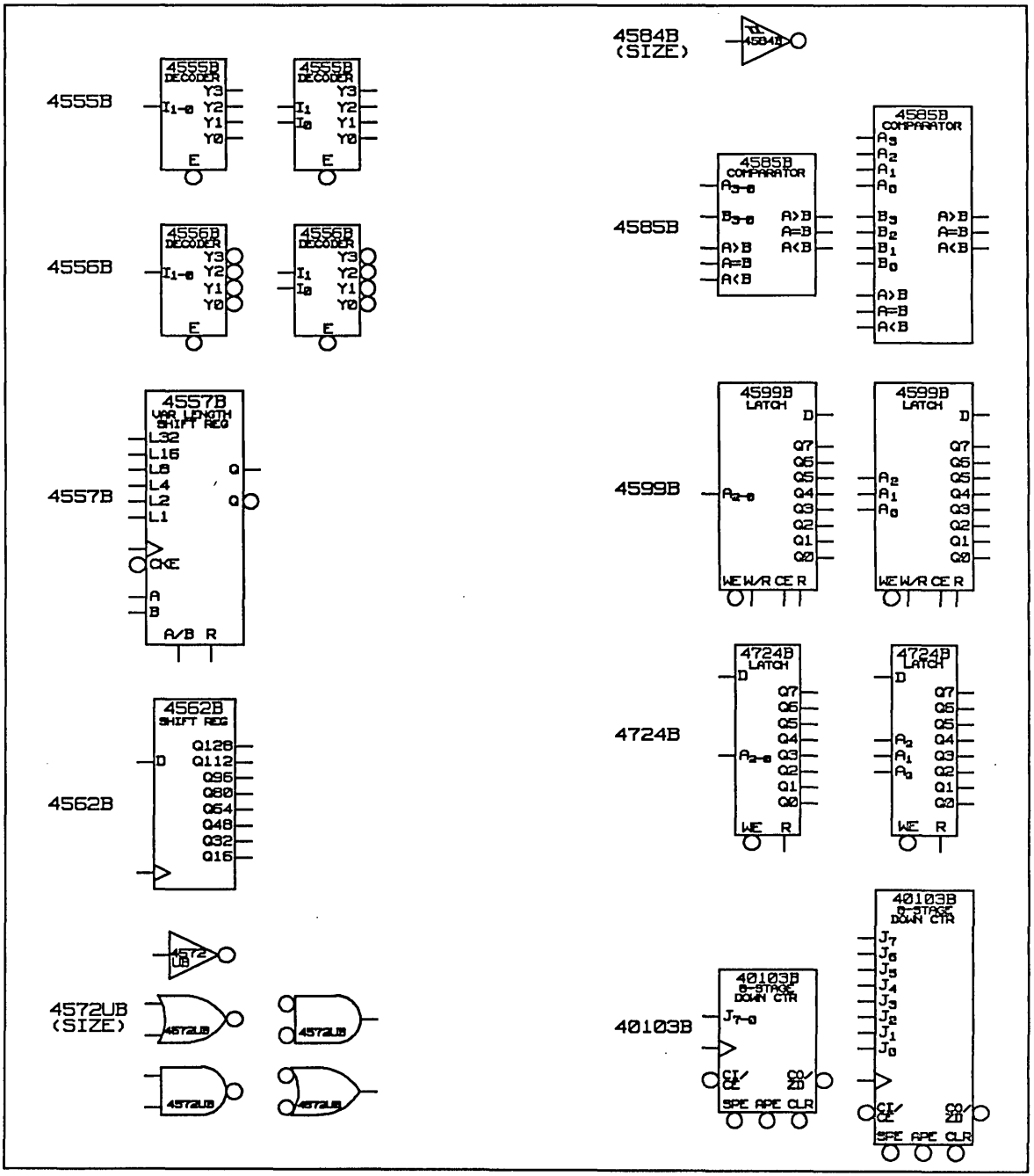

4049UB
(SIZE)
4049 UB
4050B
(SIZE)
4051B
(SIZE)
X7
X6
X5
X4
X3
X2
X1
X0
4051B
MUX/
DEMUX
X
INH
4052B
(SIZE)
4052B
MUX/DEMUX
4053B
(SIZE)
4053B
MUX/
DEMUX
S
4066B
(SIZE)
4066B
SWITCH/
MUX
A
B
CNTL
4067B
(SIZE)
4067B
MUX/
DEMUX
4068B
(SIZE)
4068B
4069UB
(SIZE)
4069 UB
4070B
(SIZE)
4070B
4071B
(SIZE)
4071B
4072B
(SIZE)
4072B
4073B
(SIZE)
4073B

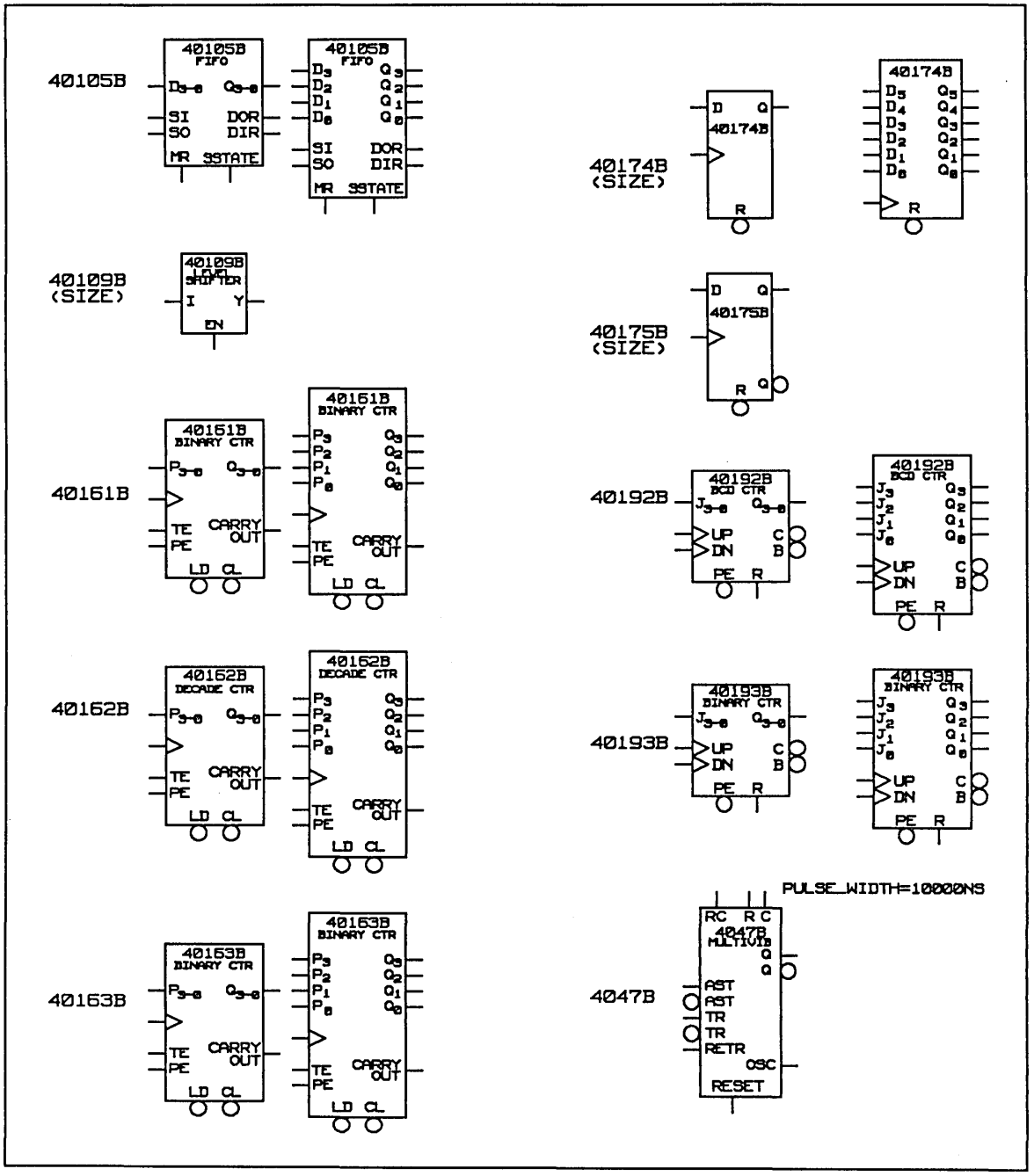

4075B (SIZE)
4076B (SIZE)
4077B (SIZE)
4078B (SIZE)
4081B (SIZE)
4082B (SIZE)
4093B (SIZE)
4094B
4098B
4099B
4160B
4161B
PULSE_WIDTH=10000NS
RC
C
R
D
Q
DE
OE
LATCH
WE
DECADE CTR
CARRY OUT
TE
PE
LD
CL
BINARY CTR
SHIFT REG
STROBE


4162B
4162B
DECADE CTR
4163B
4163B
BINARY CTR
4174B
4174B
(SIZE)
4175B
4175B
(SIZE)
4502B
4502B
(SIZE)
4503B
4503B
(SIZE)
4504B
4504B
(SIZE)
4508B
4508B
(SIZE)
4510B
4510B
BCD UP/DN CTR

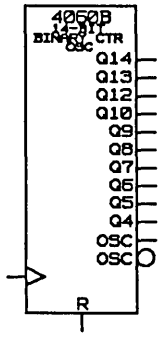

4511B
4511B
4511B
4512B
(SIZE)
4512B
4512B
4514B
(SIZE)
4514B
4514B
4515B
4515B
4515B
4516B
4516B
4516B
4517B
4517B
4519B
(SIZE)
4519B
4519B
4520B
4520B
4520B


4526B
4526B
BINARY CTR
D3-0
Q3-0
CKE
CF
ZERO
PE MR
4526B
BINARY CTR
D3
D2
D1
D0
Q3
Q2
Q1
Q0
CKE
CF
ZERO
PE MR
4538B
PULSE_WIDTH=10000NS
C R/C
4538B
A
B
MULTI VIB
CD
4528B
PULSE_WIDTH=10000NS
C R/C
4528B
MULTI VIB
CD
4539B
(SIZE)
4539B
MUX
X3
X2
X1
X0
Z
STR
S1-0
4539B
MUX
X3
X2
X1
X0
Z
STR
S1
S0
4529B
(SIZE)
4529B
DATA SELECTOR
X3
X2
X1
X0
Z
S1-0
OE
4529B
DATA SELECTOR
X3
X2
X1
X0
Z
S1
S0
OE
4551B
(SIZE)
4551B
MUX DEMUX
X1
X0
X
S
4551B
MUX DEMUX
X13
X03
X12
X02
X11
X01
X10
X00
X3
X2
X1
X0
S
4530B
(SIZE)
4530B
8-INPUT MAJORITY GATE
A
B
C
D
E
W
Y
4532B
4532B
ENCODER
D7
D6
D5
D4
D3
D2
D1
D0
Q2-0
EO
GS
EI
4532B
ENCODER
D7
D6
D5
D4
D3
D2
D1
D0
Q2
Q1
Q0
EO
GS
EI
4552B
(SIZE)
D
4552B
64X4
RAM
Q
A3-0
STM
WE
CE
LET
4552B
64X4
RAM
D3
D2
D1
D0
Q3
Q2
Q1
Q0
A5
A4
A3
A2
A1
A0
STM
WE
CE
LET

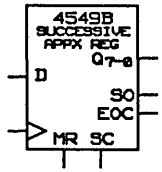

4555B
4555B
DECODER
Y3
Y2
Y1
Y0
E
4556B
4556B
4557B
4557B
VAR LENGTH
SHIFT REG
L32
L16
L8
L4
L2
L1
Q
CKE
A
B
A/B R
4562B
4562B
SHIFT REG
D
Q128
Q112
Q96
Q80
Q64
Q48
Q32
Q16
4572UB
(SIZE)
4572
UB
4572UB
4584B
(SIZE)
4584B
4585B
4585B
COMPARATOR
A>B
A=B
A<B
4599B
4599B
LATCH
WE W/R CE R
4724B
4724B
LATCH
WE R
40103B
40103B
8-STAGE
DOWN CTR
SPE APE CLR

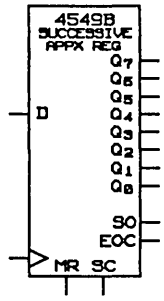

40105B
40105B FIFO
D3-0 Q3-0
SI DOR
SO DIR
MR 3STATE
40105B FIFO
D3 Q3
D2 Q2
D1 Q1
D0 Q0
SI DOR
SO DIR
MR 3STATE
40109B (SIZE)
40109B LEVEL SHIFTER
I Y
EN
40161B
40161B BINARY CTR
P3-0 Q3-0
TE CARRY OUT
PE
LD CL
40161B BINARY CTR
P3 Q3
P2 Q2
P1 Q1
P0 Q0
TE CARRY OUT
PE
LD CL
40162B
40162B DECADE CTR
P3-0 Q3-0
TE CARRY OUT
PE
LD CL
40162B DECADE CTR
P3 Q3
P2 Q2
P1 Q1
P0 Q0
TE CARRY OUT
PE
LD CL
40163B
40163B BINARY CTR
P3-0 Q3-0
TE CARRY OUT
PE
LD CL
40163B BINARY CTR
P3 Q3
P2 Q2
P1 Q1
P0 Q0
TE CARRY OUT
PE
LD CL
40174B (SIZE)
D Q
40174B
R
40174B
D5 Q5
D4 Q4
D3 Q3
D2 Q2
D1 Q1
D0 Q0
R
40175B (SIZE)
D Q
40175B
R Q
40192B
40192B BCD CTR
J3-0 Q3-0
UP C
DN B
PE R
40192B BCD CTR
J3 Q3
J2 Q2
J1 Q1
J0 Q0
UP C
DN B
PE R
40193B
40193B BINARY CTR
J3-0 Q3-0
UP C
DN B
PE R
40193B BINARY CTR
J3 Q3
J2 Q2
J1 Q1
J0 Q0
UP C
DN B
PE R
4047B
PULSE_WIDTH=10000NS
RC R C
4047B MULTIVIB
Q
Q
AST
AST
TR
TR
RETR
OSC
RESET

4060B

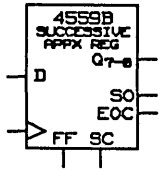


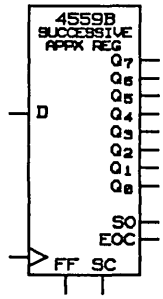
4549B



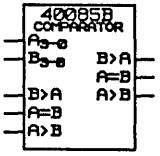


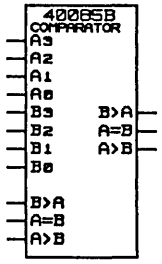
4559B

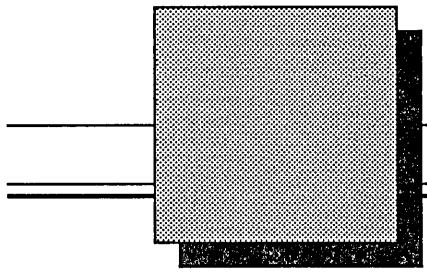




40085B







The DISCRETE Library

The DISCRETE Library requires approximately 415 Kbytes of disk storage.

The release level of the DISCRETE Library is 9.0.

The library contains body drawings and physical models for the following 31 components:

4BIT CONNECTOR
ANALOG GND
ANTENNA
ATTENUATOR
BATTERY

CAPACITOR
CHASSIS GND
CONNECTOR
DIODE
EARTH GND

FUSE
GND
INDUCTOR
INTERLOCK
LAMP

LED
LOOP ANTENNA
MULTITAP TRANSFORMER
N JFET
NPN

P JFET
PNP
RESISTOR
SWITCH
TAPPED INDUCTOR

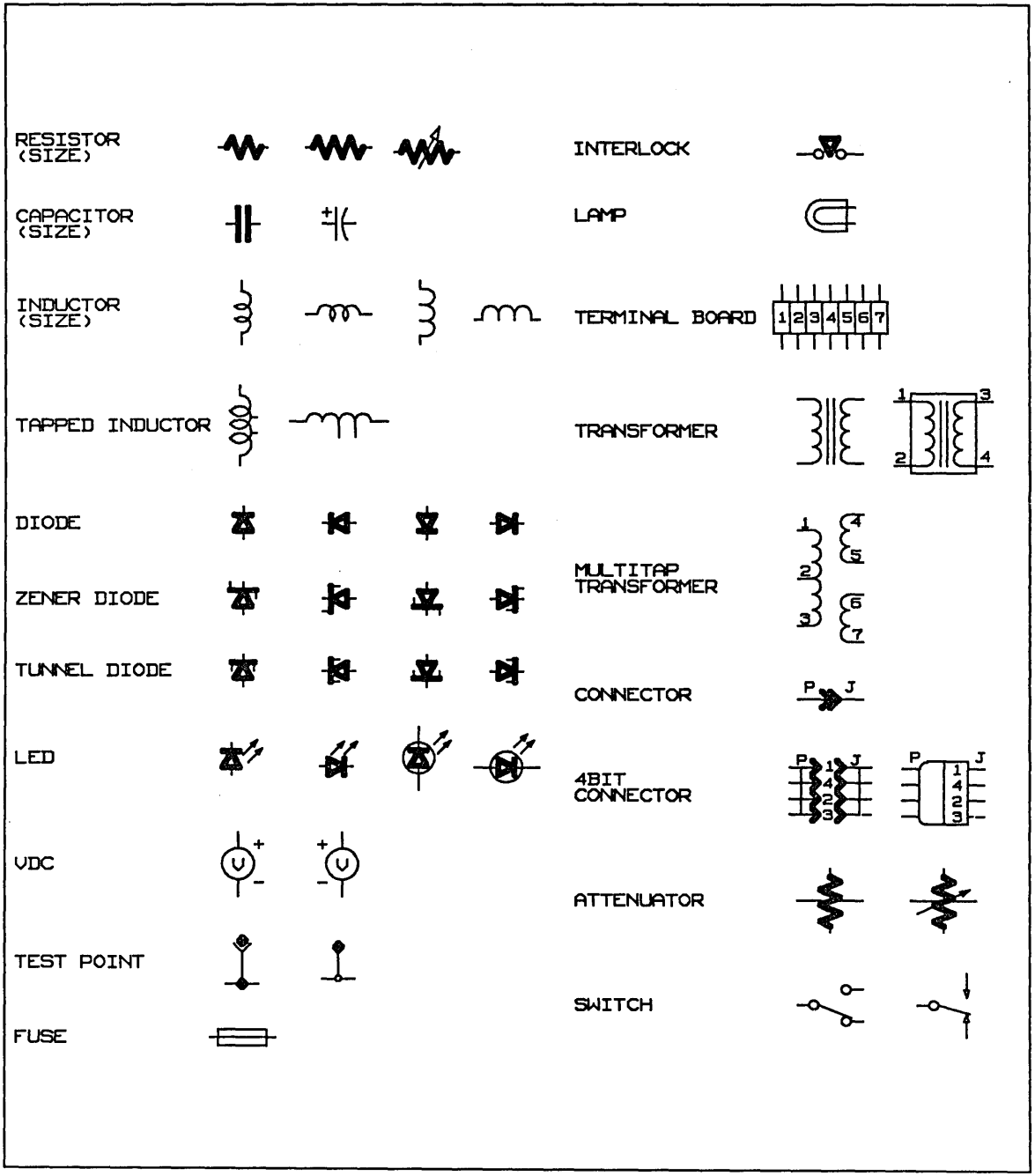
TERMINAL BOARD
TEST POINT
TRANSFORMER
TUNNEL DIODE
VDC

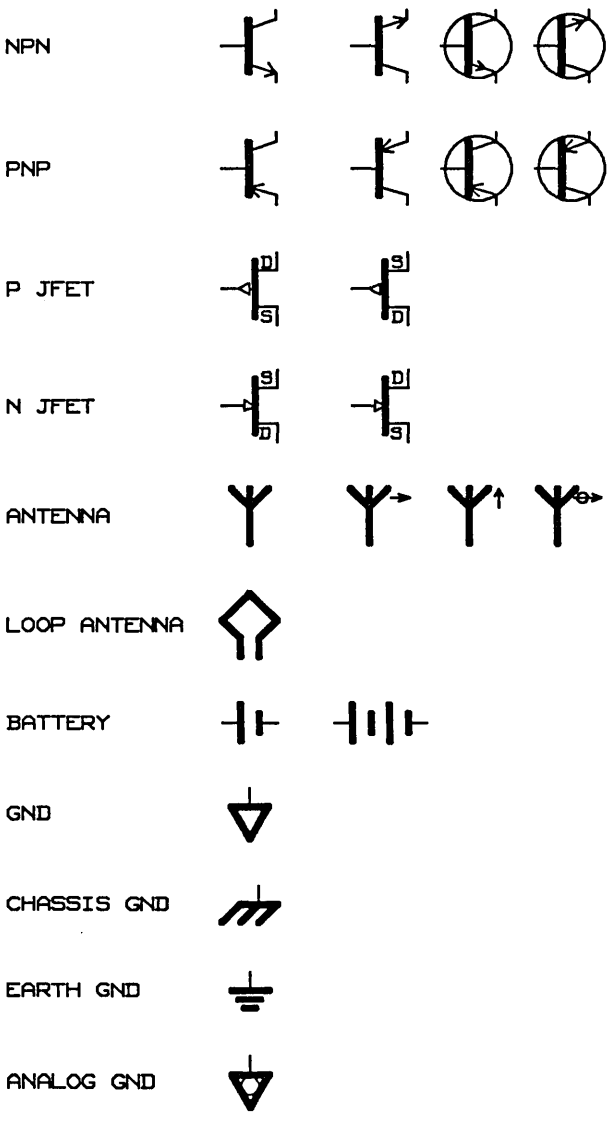
ZENER DIODE

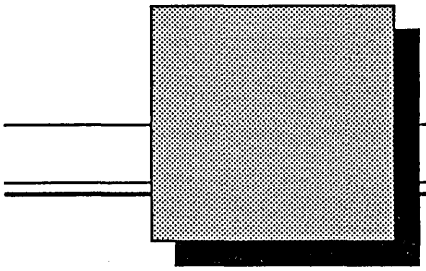
Application Notes

The Discrete Library is a generic library; users must diagram and customize parts to meet their requirements.

The RESISTOR, CAPACITOR, and INDUCTOR models also include simulation and timing models. These models function only as connection elements; the output signal always follows the input signal. Hence, the CAPACITOR can only be used as a coupling capacitor, not as a bypass capacitor. Likewise, the RESISTOR model cannot be used as a pullup or pulldown resistor.


RESISTOR (SIZE)
CAPACITOR (SIZE)
INDUCTOR (SIZE)
TAPPED INDUCTOR
DIODE
ZENER DIODE
TUNNEL DIODE
LED
VDC
TEST POINT
FUSE
INTERLOCK
LAMP
TERMINAL BOARD
1 2 3 4 5 6 7
TRANSFORMER
MULTITAP TRANSFORMER
CONNECTOR
P
J
4BIT CONNECTOR
ATTENUATOR
SWITCH


NPN
PNP
P JFET
D
S
N JFET
S
D
ANTENNA
LOOP ANTENNA
BATTERY
GND
CHASSIS GND
EARTH GND
ANALOG GND



The MEMORY and ANSI MEMORY Libraries

The MEMORY Library requires approximately 4623 Kbytes of disk storage, and the ANSI MEMORY Library requires approximately 4948 Kbytes of disk storage. The physical, timing, and simulation models for each library are identical and differ only in their body drawings. The part name for a component in either library is the same; the body drawing used is determined by the first library name encountered in the library search path (*memory.lib* or *amemory.lib*).

The release level of the MEMORY and ANSI MEMORY Libraries is 9.0.

Each library contains a body drawing and physical, timing, and simulation models for the following 98 components:

2114AL-1	1024 x 4 static RAM
2147H-1	4096 x 1 static RAM
2148H-3	1024 x 4 static RAM
2164A-15	65536 x 1 dynamic RAM
24S10	256 x 4 bipolar PROM
24S41	1024 x 4 bipolar PROM
24S81	2048 x 4 bipolar PROM
24SA10	256 x 4 bipolar PROM
27128	16384 x 8 EPROM
2716-1	2048 x 8 EPROM
27256	32K x 8 EPROM
2732A-2	4096 x 8 EPROM
27512	64K x 8 EPROM
2764-2	8192 x 8 EPROM
27C256	32K x 8 EPROM
27C64	8K x 8 EPROM
27LS18	32 x 8 bipolar PROM
27LS19	32 x 8 bipolar PROM
27S13	512 x 4 bipolar PROM
27S13A	512 x 4 bipolar PROM
27S181	1024 x 8 bipolar PROM
27S181A	1024 x 8 bipolar PROM
27S185	2048 x 4 bipolar PROM
27S185A	2048 x 4 bipolar PROM
27S19	32 x 8 bipolar PROM

27S191	2048 x 8 bipolar PROM
27S19A	32 x 8 bipolar PROM
27S21	256 x 4 bipolar PROM
27S21A	256 x 4 bipolar PROM
27S25	512 x 8 bipolar PROM
27S25A	512 x 8 bipolar PROM
27S27	512 x 8 bipolar PROM
27S28	512 x 8 bipolar PROM
27S28A	512 x 8 bipolar PROM
27S29	512 x 8 bipolar PROM
27S29A	512 x 8 bipolar PROM
27S291	2048 x 8 bipolar PROM
27S291A	2048 x 8 bipolar PROM
27S33	1024 x 4 bipolar PROM
27S33A	1024 x 4 bipolar PROM
27S41	4096 x 4 bipolar PROM
27S41A	4096 x 4 bipolar PROM
27S43	4096 x 8 bipolar PROM
27S43A	4096 x 8 bipolar PROM
28L22	256 x 8 low-power PROM
28L42	512 x 8 low-power PROM
28L86A	1024 x 8 low-power PROM
28LA22	256 X 8 low-power PROM
28R85	512 x 8 registered PROM
28S42	512 x 8 standard PROM

28S86A	1024 x 8 standard PROM
28S166	2048 x 8 standard PROM
51C256L-15	256K x 1 CHMOS dynamic RAM
51C64L-12	64K x 1 CHMOS dynamic RAM
74F410	16 x 4 RAM with register stack
74S188	32 x 8 PROM
74S288	32 x 8 PROM
74S387	256 x 4 PROM
AM9122-25	256 x 4 static R/W RAM
AM9128-70	2048 x 8 static R/W RAM
AM9150-20	1024 x 4 static R/W RAM
AM93L422	256 x 4 static RAM
AM9864-2	8192 x 8 EEPROM
CY7C122-15	256 x 4 static R/W RAM
CY7C150-15	1024 x 4 static R/W RAM
CY7C166-25	16384 x 4 static R/W RAM
CY7C167-25	16384 x 1 static R/W RAM
CY7C169-25	4096 x 4 static R/W RAM
CY7C185-35	8192 x 4 static R/W RAM
CY7C235-30	1K x 8 CMOS PROM
CY7C263-35	8192 x 8 PROM
CY8C166-25	16384 x 4 static R/W RAM
CY8C185-35	8192 x 4 static R/W RAM
F1600-55	65536 x 1 CMOS static RAM
HM4864-2	65536 x 1 NMOS RAM

HM6116-2	2048 x 8 CMOS RAM
HM6167	16384 x 1 CMOS RAM
HM6264P-15	8192 x 8 CMOS static RAM
HM6514-5	1024 x 4 CMOS static RAM
IDT7130L-90	1024 x 8 CMOS dual port RAM
IDT7130S-90	1024 x 8 CMOS dual port RAM
IMS1420-45	4096 x 4 static RAM
M5M44C256P-10	256K x 4 dynamic RAM
M5M4C1000P-10	1024K x 1 dynamic RAM
MCM10474-15	1024 x 4 static RAM
MCM10474-25	1024 x 4 static RAM
MCM6164-55	8192 x 8 HCMOS static RAM
MCM6664-15	65536 x 1 dynamic RAM
NMC2142A	1024 x 4 static RAM
TC511002-10	1024K dynamic RAM
TC5517B	2048 x 8 CMOS RAM
TC5564P-15	8192 x 8 CMOS static RAM
TMS2149-3	1024 x 4 static RAM
TMS2167-4	16384 x 1 static RAM
TMS4164-12	16384 x 1 dynamic RAM
TMS4256E9-15	256K x 9 dynamic RAM
UPD446-5	2048 x 8 static CMOS RAM
X2210	64 x 4 nonvolatile static RAM

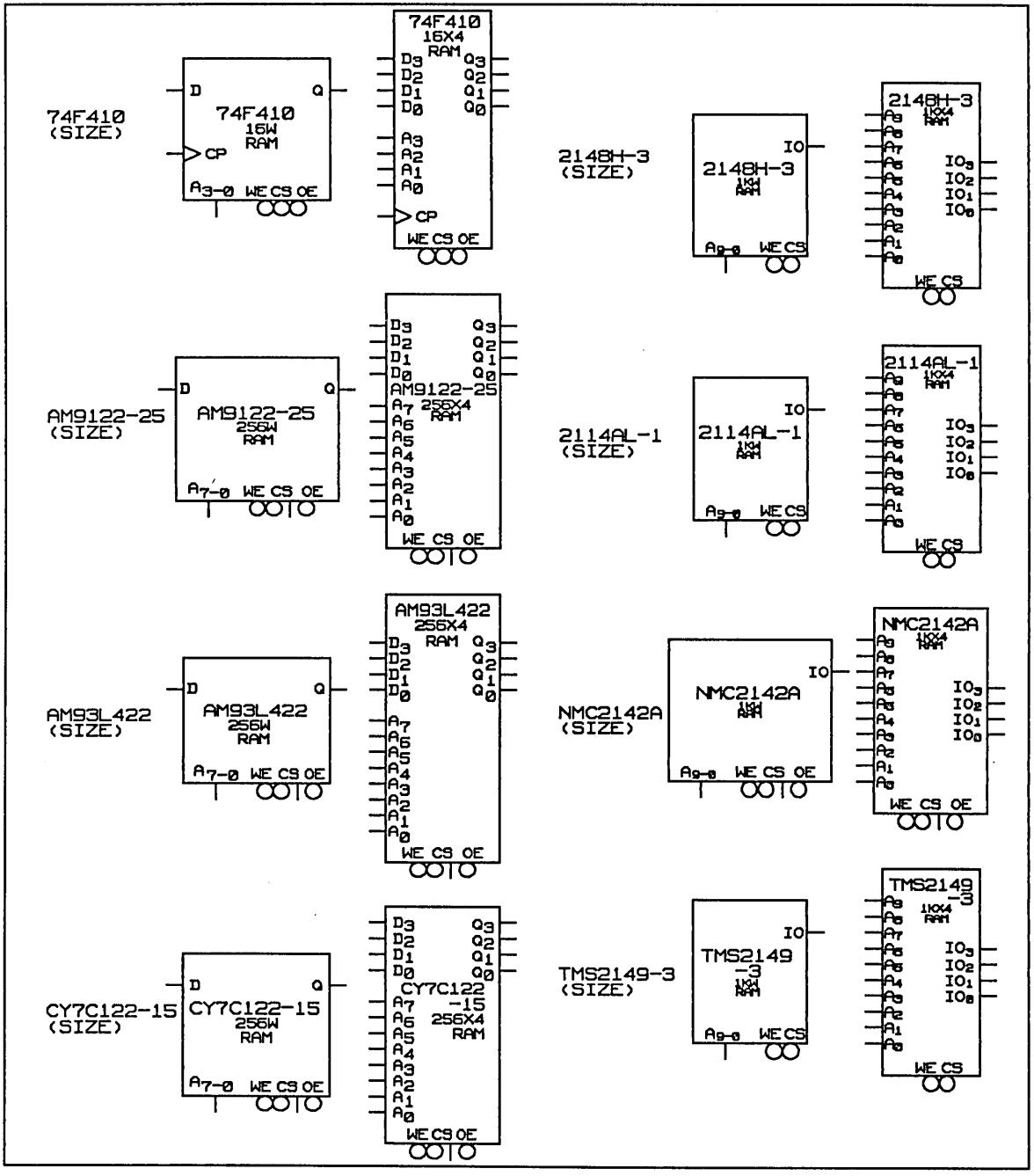
Application Notes

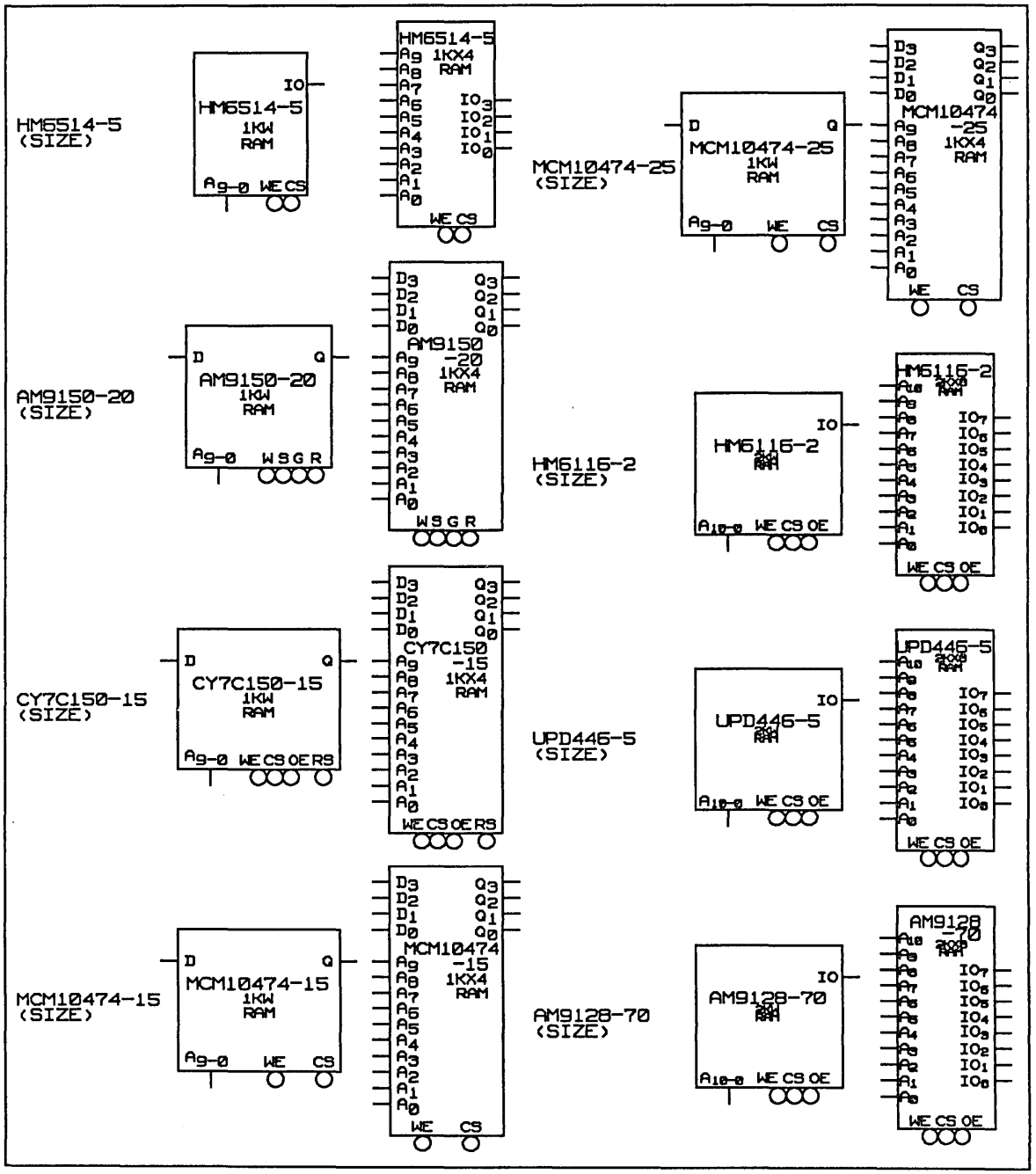
Static RAMs

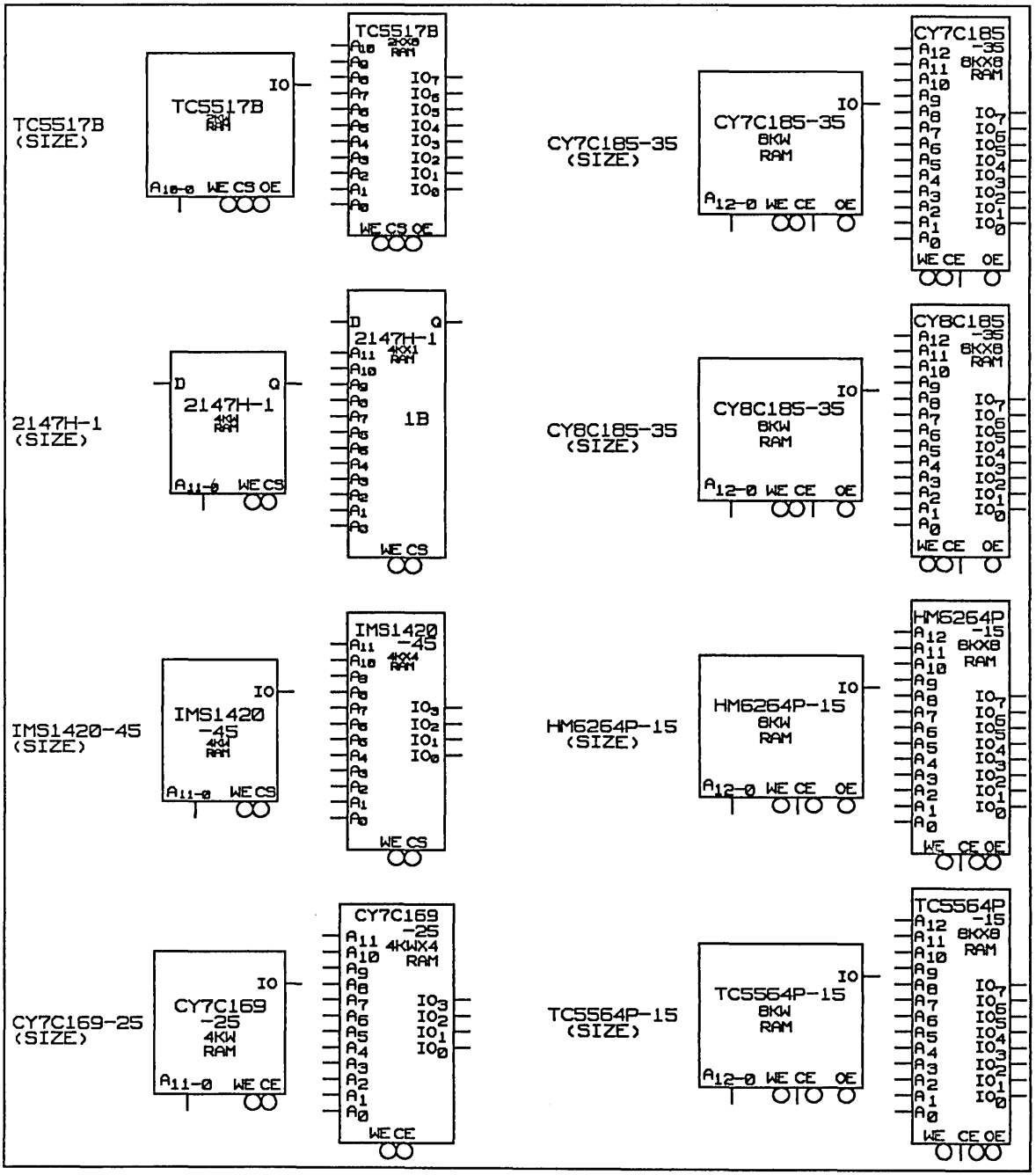
The static RAM models work for both a CS*-controlled write cycle and a WE*-controlled write cycle. To make the best use of the models, include the following directive in the Timing Verifier's directives file *(verifier.cmd)*:

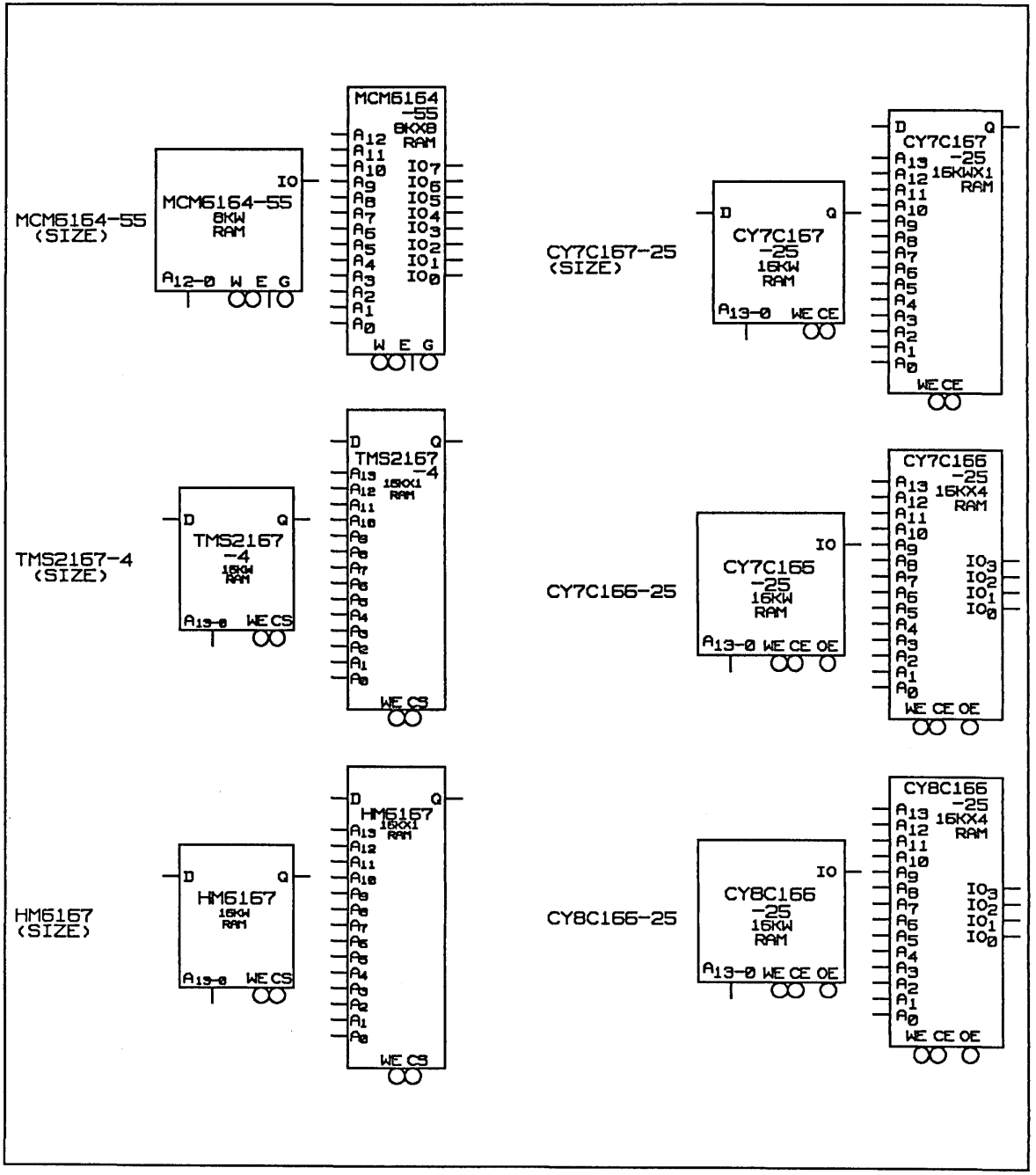
```
latch_err_model closed;
```

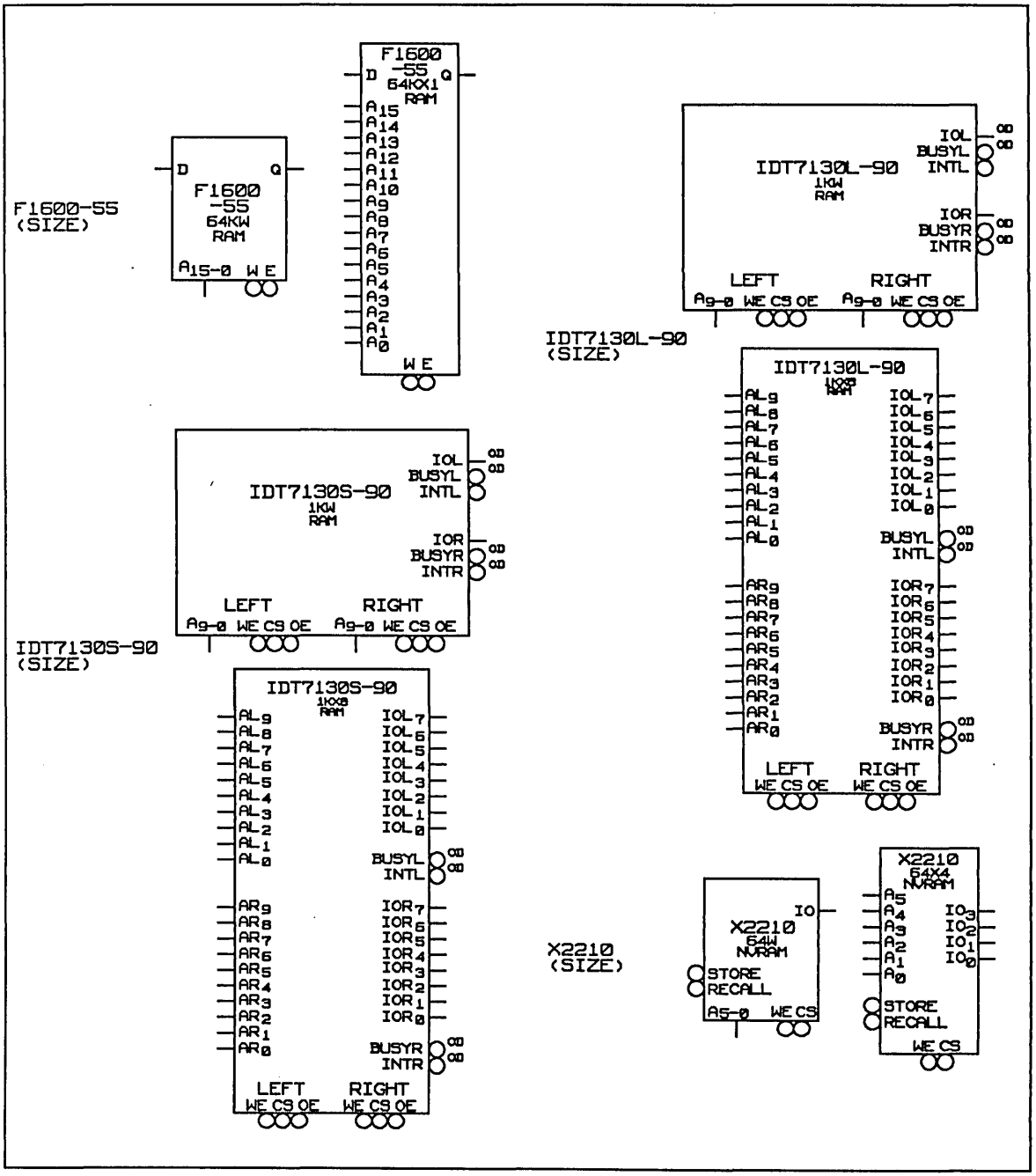
If this directive is omitted, the model still works correctly, but the Timing Verifier generates an erroneous hold time violation on the I/O pins.

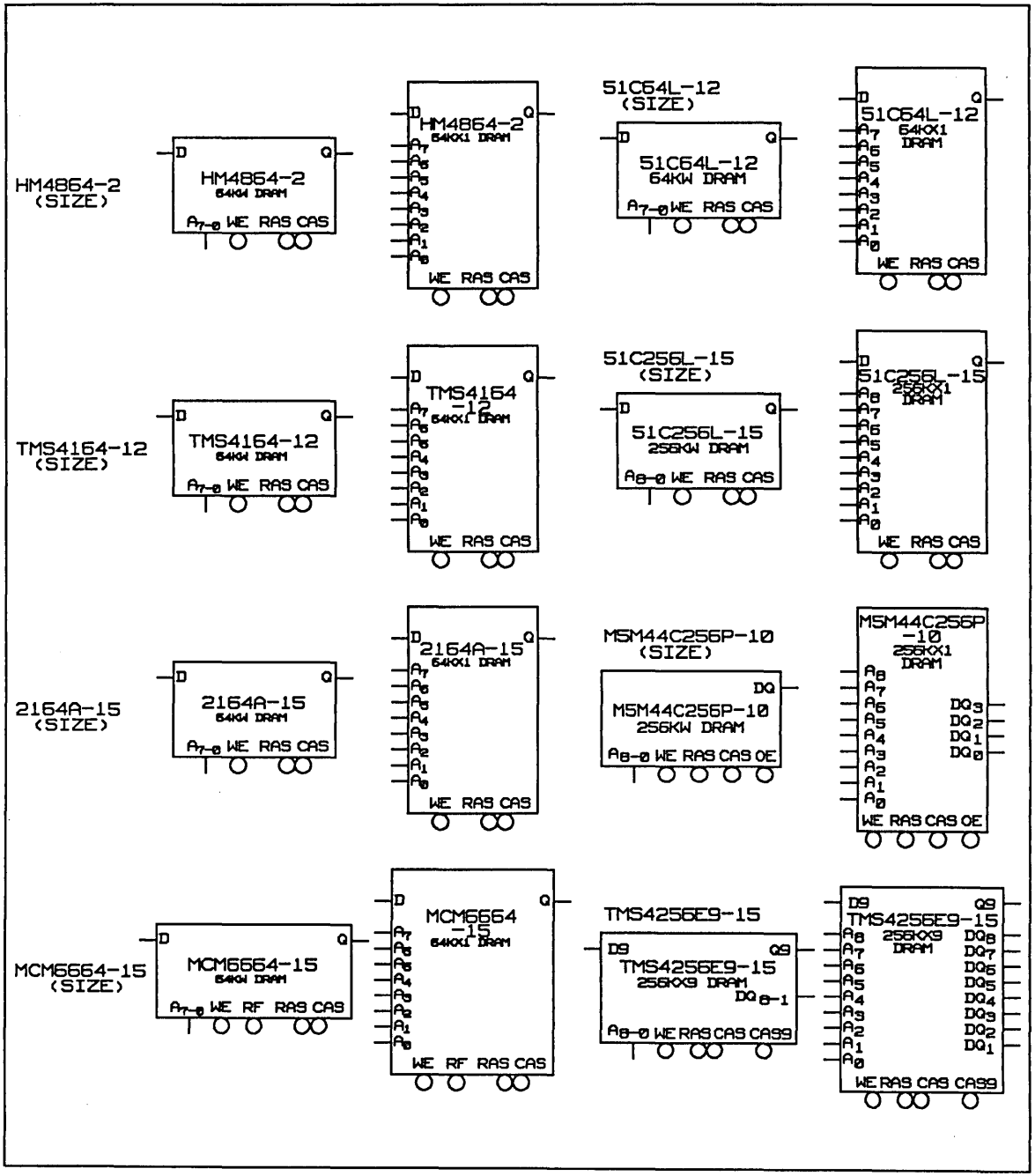

74F410
(SIZE)
D
Q
74F410
16W
RAM
CP
A3-0 WE CS OE
74F410
16X4
RAM
D3
D2
D1
D0
Q3
Q2
Q1
Q0
A3
A2
A1
A0
CP
WE CS OE
2148H-3
(SIZE)
IO
2148H-3
1KX4
RAM
A9-0 WE CS
2148H-3
IO3
IO2
IO1
IO0
WE CS
AM9122-25
(SIZE)
AM9122-25
256W
RAM
A7-0 WE CS OE
AM9122-25
256X4
RAM
A7
A6
A5
A4
2114AL-1
(SIZE)
2114AL-1
1KX4
RAM
2114AL-1
AM93L422
(SIZE)
AM93L422
256W
RAM
AM93L422
256X4
RAM
NMC2142A
(SIZE)
NMC2142A
1KX4
RAM
A9-0 WE CS OE
NMC2142A
CY7C122-15
(SIZE)
CY7C122-15
256W
RAM
CY7C122
-15
256X4
RAM
TMS2149-3
(SIZE)
TMS2149
-3
1KX4
RAM
A9-0 WE CS
TMS2149
-3

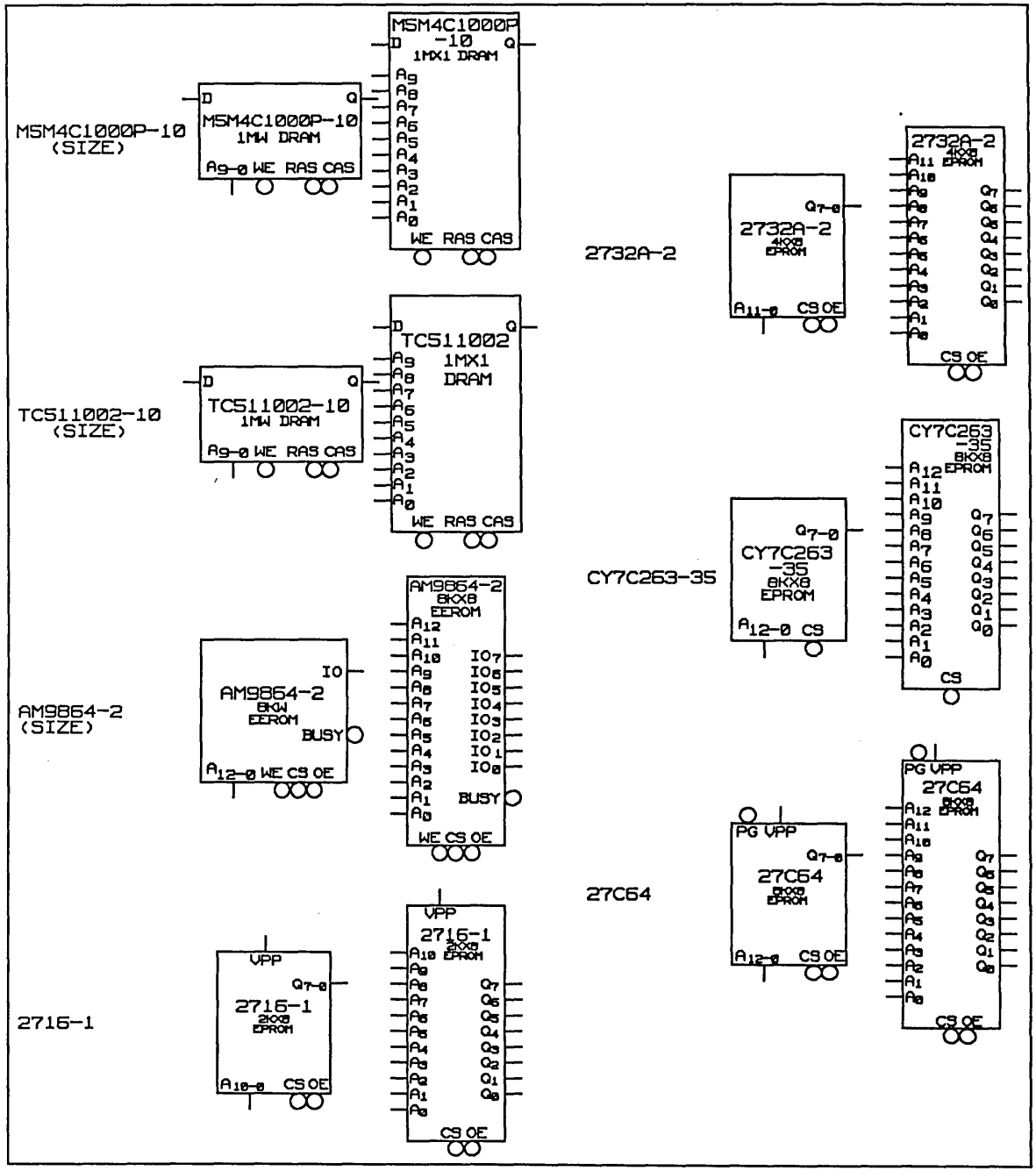

HM6514-5
(SIZE)
HM6514-5
1KW
RAM
IO
A9-0 WE CS
HM6514-5
1KX4
RAM
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
IO3
IO2
IO1
IO0
WE CS
MCM10474-25
(SIZE)
MCM10474-25
1KW
RAM
D
Q
A9-0 WE CS
MCM10474
-25
1KX4
RAM
D3
D2
D1
D0
Q3
Q2
Q1
Q0
WE CS
AM9150-20
(SIZE)
AM9150-20
1KW
RAM
D
Q
A9-0 WSG R
AM9150
-20
1KX4
RAM
WSG R
HM6116-2
(SIZE)
HM6116-2
2KX8
RAM
IO
A10-0 WE CS OE
HM6116-2
2KX8
RAM
IO7
IO6
IO5
IO4
IO3
IO2
IO1
IO0
WE CS OE
CY7C150-15
(SIZE)
CY7C150-15
1KW
RAM
D
Q
A9-0 WE CS OE RS
CY7C150
-15
1KX4
RAM
WE CS OE RS
UPD446-5
(SIZE)
UPD446-5
2KX8
RAM
IO
A10-0 WE CS OE
UPD446-5
2KX8
RAM
IO7
IO6
IO5
IO4
IO3
IO2
IO1
IO0
WE CS OE
MCM10474-15
(SIZE)
MCM10474-15
1KW
RAM
D
Q
A9-0 WE CS
MCM10474
-15
1KX4
RAM
WE CS
AM9128-70
(SIZE)
AM9128-70
2KX8
RAM
IO
A10-0 WE CS OE
AM9128
-70
2KX8
RAM
IO7
IO6
IO5
IO4
IO3
IO2
IO1
IO0
WE CS OE

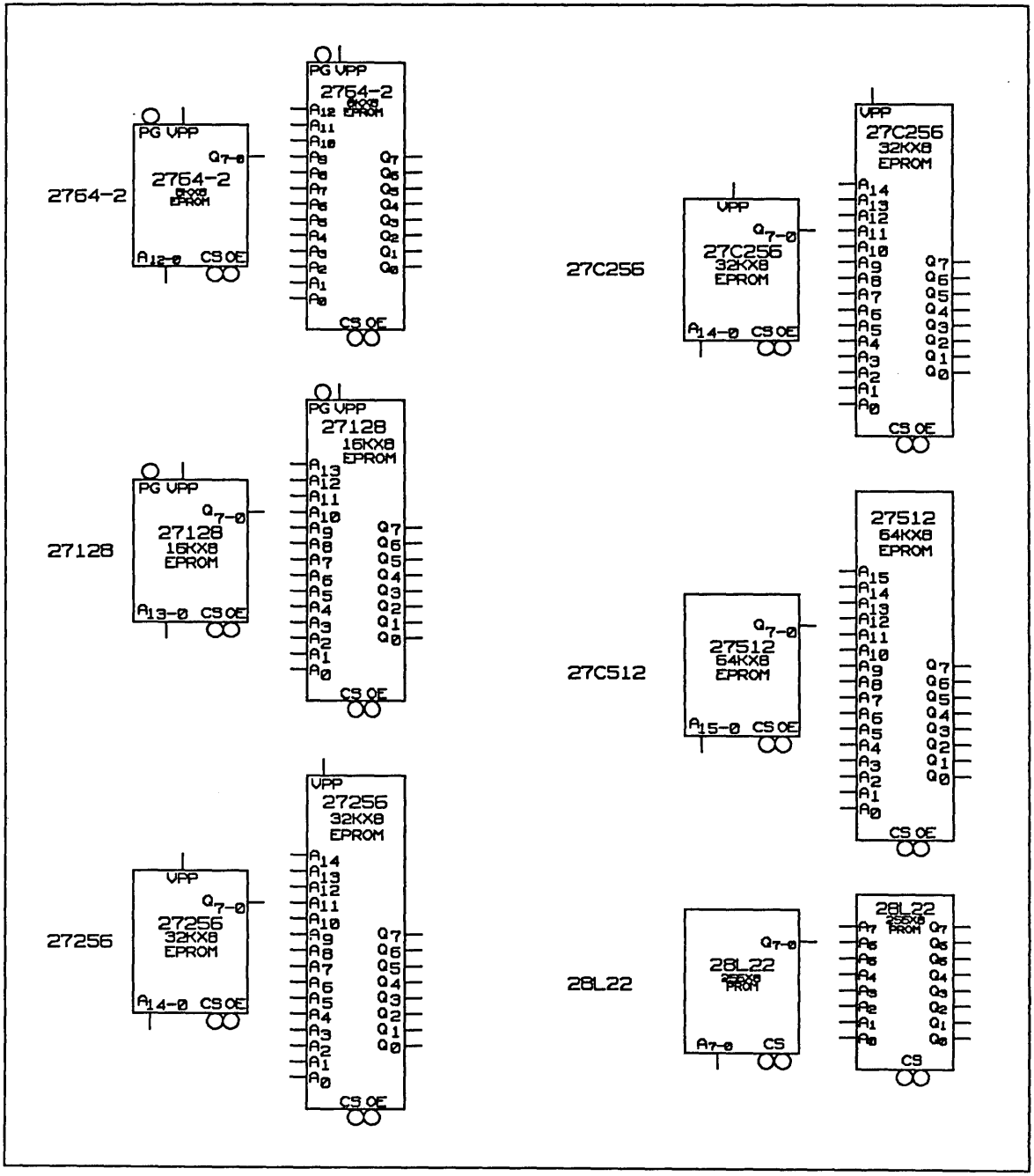

TC5517B
(SIZE)
TC5517B
1KX8
RAM
IO
A10-0 WE CS OE
TC5517B
1KX8
RAM
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
IO7
IO6
IO5
IO4
IO3
IO2
IO1
IO0
WE CS OE
CY7C185-35
(SIZE)
CY7C185-35
8KW
RAM
IO
A12-0 WE CE OE
CY7C185
-35
8KX8
RAM
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
IO7
IO6
IO5
IO4
IO3
IO2
IO1
IO0
WE CE OE
2147H-1
(SIZE)
2147H-1
4KX1
RAM
D
Q
A11-0 WE CS
2147H-1
4KX1
RAM
1B
D
Q
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
WE CS
CY8C185-35
(SIZE)
CY8C185-35
8KW
RAM
IO
A12-0 WE CE OE
CY8C185
-35
8KX8
RAM
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
IO7
IO6
IO5
IO4
IO3
IO2
IO1
IO0
WE CE OE
IMS1420-45
(SIZE)
IMS1420
-45
4KX4
RAM
IO
A11-0 WE CS
IMS1420
-45
4KX4
RAM
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
IO3
IO2
IO1
IO0
WE CS
HM6264P-15
(SIZE)
HM6264P-15
8KW
RAM
IO
A12-0 WE CE OE
HM6264P
-15
8KX8
RAM
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
IO7
IO6
IO5
IO4
IO3
IO2
IO1
IO0
WE CE OE
CY7C169-25
(SIZE)
CY7C169
-25
4KW
RAM
IO
A11-0 WE CE
CY7C169
-25
4KWX4
RAM
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
IO3
IO2
IO1
IO0
WE CE
TC5564P-15
(SIZE)
TC5564P-15
8KW
RAM
IO
A12-0 WE CE OE
TC5564P
-15
8KX8
RAM
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
IO7
IO6
IO5
IO4
IO3
IO2
IO1
IO0
WE CE OE

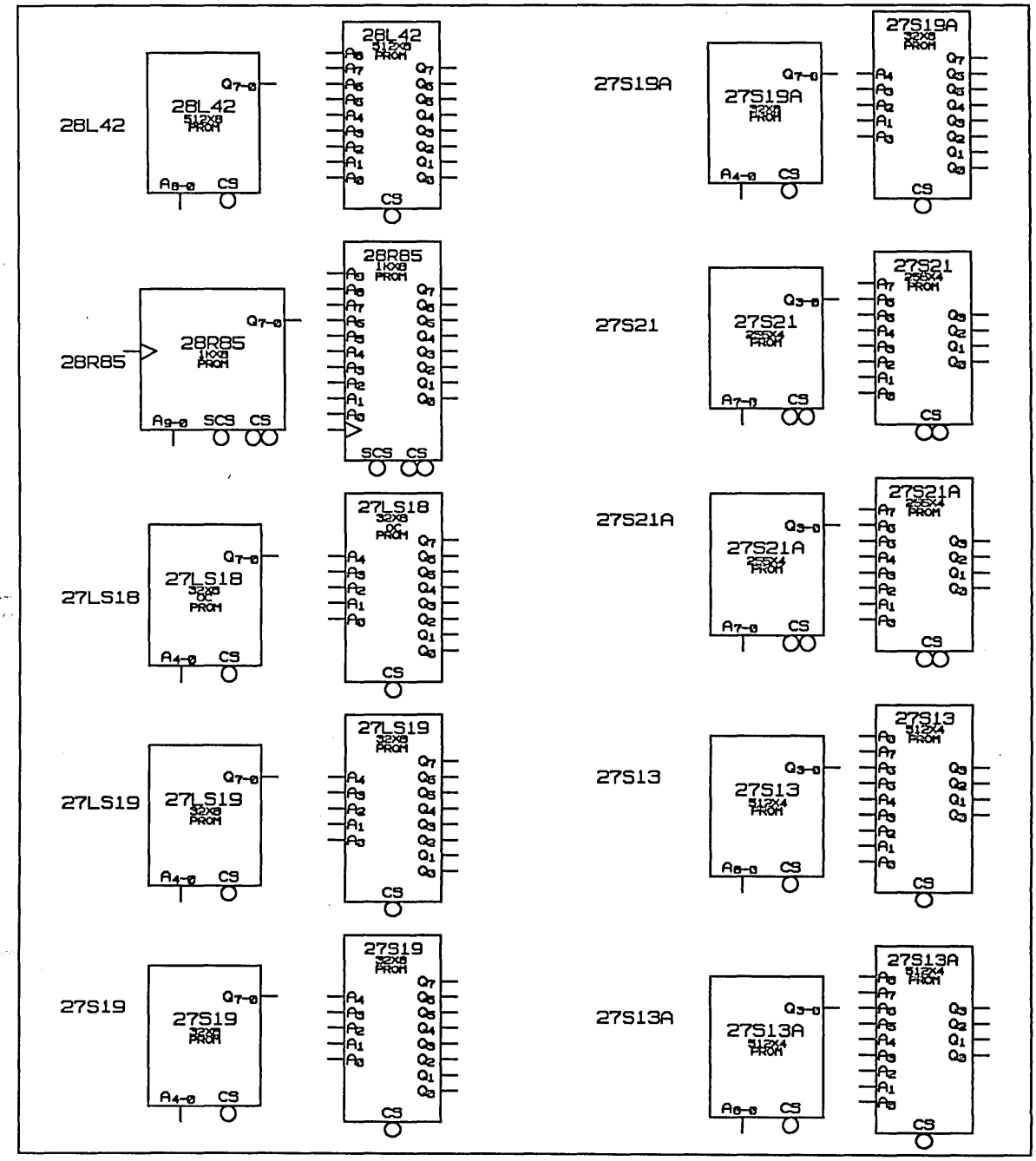

MCM6164-55
(SIZE)
MCM6164-55
8KW
RAM
IO
A12-0 W E G
MCM6164
-55
8KX8
RAM
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
IO7
IO6
IO5
IO4
IO3
IO2
IO1
IO0
W E G
CY7C167-25
(SIZE)
D
Q
CY7C167
-25
16KW
RAM
A13-0 WE CE
CY7C167
-25
16KWX1
RAM
WE CE
TMS2167-4
(SIZE)
TMS2167
-4
16KW
RAM
A13-0 WE CS
TMS2167
-4
16KX1
RAM
WE CS
CY7C166-25
CY7C166
-25
16KW
RAM
A13-0 WE CE OE
CY7C166
-25
16KX4
RAM
IO3
IO2
IO1
IO0
WE CE OE
HM6167
(SIZE)
HM6167
16KW
RAM
A13-0 WE CS
HM6167
16KX1
RAM
WE CS
CY8C166-25
CY8C166
-25
16KW
RAM
A13-0 WE CE OE
CY8C166
-25
16KX4
RAM
WE CE OE

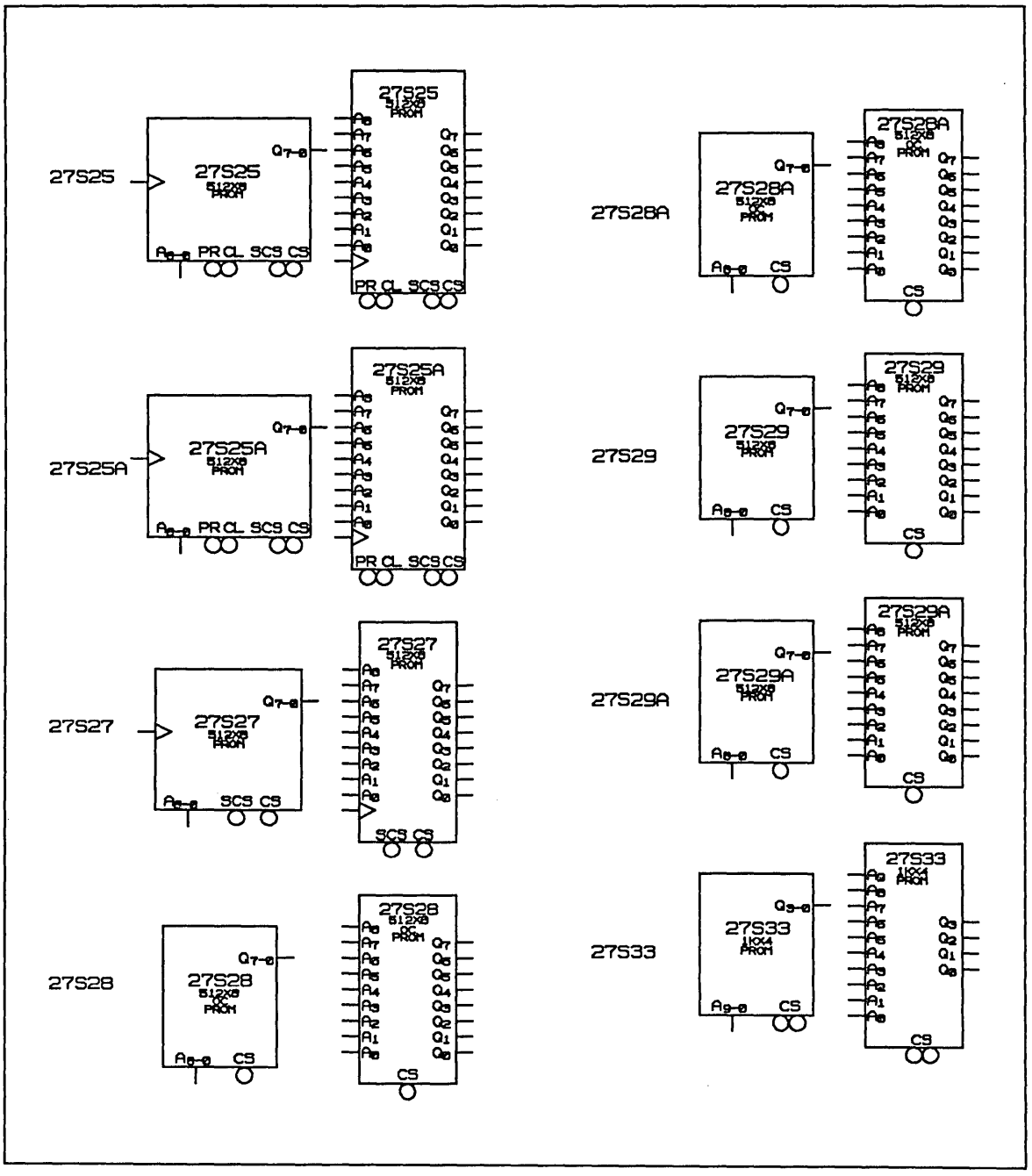

F1600-55
(SIZE)
D
Q
F1600
-55
64KW
RAM
A15-0 W E
F1600
-55
64KX1
RAM
D
Q
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
W E
IDT7130L-90
(SIZE)
IDT7130L-90
1KW
RAM
IOL
BUSYL
INTL
8
8
IOR
BUSYR
INTR
8
8
LEFT
A9-0 WE CS OE
RIGHT
A9-0 WE CS OE
IDT7130L-90
1KW8
RAM
AL9
AL8
AL7
AL6
AL5
AL4
AL3
AL2
AL1
AL0
IOL7
IOL6
IOL5
IOL4
IOL3
IOL2
IOL1
IOL0
BUSYL
INTL
AR9
AR8
AR7
AR6
AR5
AR4
AR3
AR2
AR1
AR0
IOR7
IOR6
IOR5
IOR4
IOR3
IOR2
IOR1
IOR0
BUSYR
INTR
LEFT
WE CS OE
RIGHT
WE CS OE
IDT7130S-90
(SIZE)
IDT7130S-90
1KW
RAM
IDT7130S-90
1KW8
RAM
X2210
(SIZE)
X2210
64W
NVRAM
IO
STORE
RECALL
A5-0 WE CS
X2210
64X4
NVRAM
A5
A4
A3
A2
A1
A0
IO3
IO2
IO1
IO0
STORE
RECALL
WE CS


HM4864-2
(SIZE)
HM4864-2
64KW DRAM
A7-0 WE RAS CAS
HM4864-2
64KX1 DRAM
WE RAS CAS
51C64L-12
(SIZE)
51C64L-12
64KW DRAM
A7-0 WE RAS CAS
51C64L-12
64KX1 DRAM
WE RAS CAS
TMS4164-12
(SIZE)
TMS4164-12
64KW DRAM
A7-0 WE RAS CAS
TMS4164 -12
64KX1 DRAM
WE RAS CAS
51C256L-15
(SIZE)
51C256L-15
256KW DRAM
A8-0 WE RAS CAS
51C256L-15
256KX1 DRAM
WE RAS CAS
2164A-15
(SIZE)
2164A-15
64KW DRAM
A7-0 WE RAS CAS
2164A-15
64KX1 DRAM
WE RAS CAS
M5M44C256P-10
(SIZE)
M5M44C256P-10
256KW DRAM
A8-0 WE RAS CAS OE
M5M44C256P -10
256KX1 DRAM
WE RAS CAS OE
MCM6664-15
(SIZE)
MCM6664-15
64KW DRAM
A7-0 WE RF RAS CAS
MCM6664 -15
64KX1 DRAM
WE RF RAS CAS
TMS4256E9-15
TMS4256E9-15
256KX9 DRAM
A8-0 WE RAS CAS CAS9
TMS4256E9-15
256KX9 DRAM
WE RAS CAS CAS9

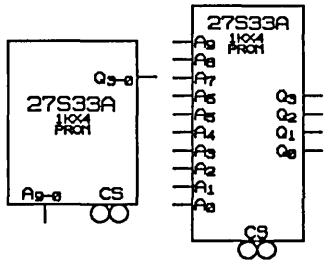

M5M4C1000P-10
(SIZE)
D
Q
M5M4C1000P-10
1MW DRAM
A9-0 WE RAS CAS
M5M4C1000P
-10
1MX1 DRAM
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
WE RAS CAS
2732A-2
Q7-0
2732A-2
4KX8
EPROM
A11-0 CS OE
A11
A10
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
CS OE
TC511002-10
(SIZE)
TC511002-10
1MW DRAM
A9-0 WE RAS CAS
TC511002
1MX1
DRAM
CY7C263-35
CY7C263
-35
8KX8
EPROM
A12-0 CS
A12
CS
AM9864-2
(SIZE)
AM9864-2
8KX8
EEROM
IO
BUSY
A12-0 WE CS OE
IO7
IO6
IO5
IO4
IO3
IO2
IO1
IO0
27C64
PG VPP
27C64
8KX8
EPROM
2716-1
VPP
2716-1
2KX8
EPROM
A10-0 CS OE
A10
CS OE


2764-2
PG VPP
2764-2
8KX8
EPROM
A12-0 CS OE
Q7-0
PG VPP
2764-2
8KX8
EPROM
A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
CS OE
27128
PG VPP
27128
16KX8
EPROM
A13-0 CS OE
Q7-0
PG VPP
27128
16KX8
EPROM
A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
CS OE
27256
VPP
27256
32KX8
EPROM
A14-0 CS OE
Q7-0
VPP
27256
32KX8
EPROM
A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
CS OE
27C256
VPP
27C256
32KX8
EPROM
A14-0 CS OE
Q7-0
VPP
27C256
32KX8
EPROM
A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
CS OE
27C512
27512
64KX8
EPROM
A15-0 CS OE
Q7-0
27512
64KX8
EPROM
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
CS OE
28L22
A7-0 CS
Q7-0
28L22
PROM
28L22
PROM
A7 A6 A5 A4 A3 A2 A1 A0
Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
CS

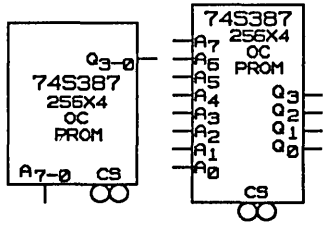

28L42
28L42
512X8
PROM
Q7-0
A8-0
CS
28R85
1KX8
PROM
Q7-0
A9-0
SCS
CS
27LS18
32X8
OC
PROM
Q7-0
A4-0
CS
27LS19
32X8
PROM
Q7-0
A4-0
CS
27S19
32X8
PROM
Q7-0
A4-0
CS
27S19A
32X8
PROM
Q7-0
A4-0
CS
27S21
256X4
PROM
Q3-0
A7-0
CS
27S21A
256X4
PROM
Q3-0
A7-0
CS
27S13
512X4
PROM
Q3-0
A8-0
CS
27S13A
512X4
PROM
Q3-0
A8-0
CS


27S25
27S25
512X8
PROM
Q7-0
A8-0
PR CL SCS CS
27S25A
27S25A
27S27
27S27
SCS CS
27S28
27S28
CS
27S28A
27S28A
27S29
27S29
27S29A
27S29A
27S33
27S33
1IX4
Q3-0
A9-0

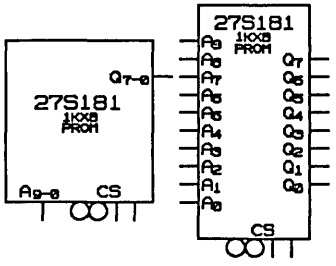
27S33A



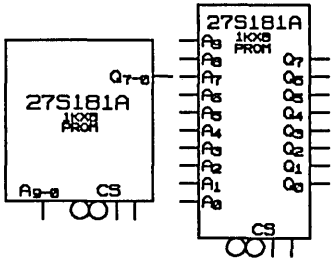
74S387



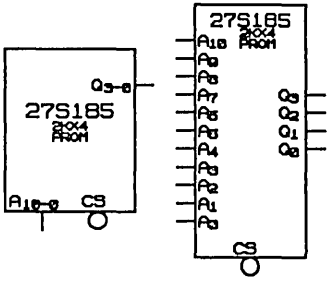
27S181



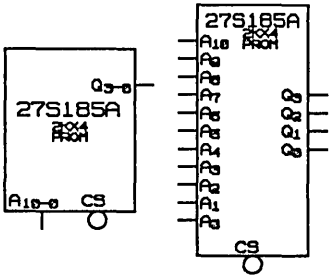
27S181A



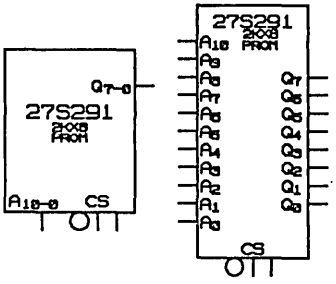
27S185



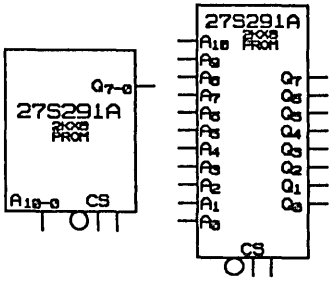
27S185A

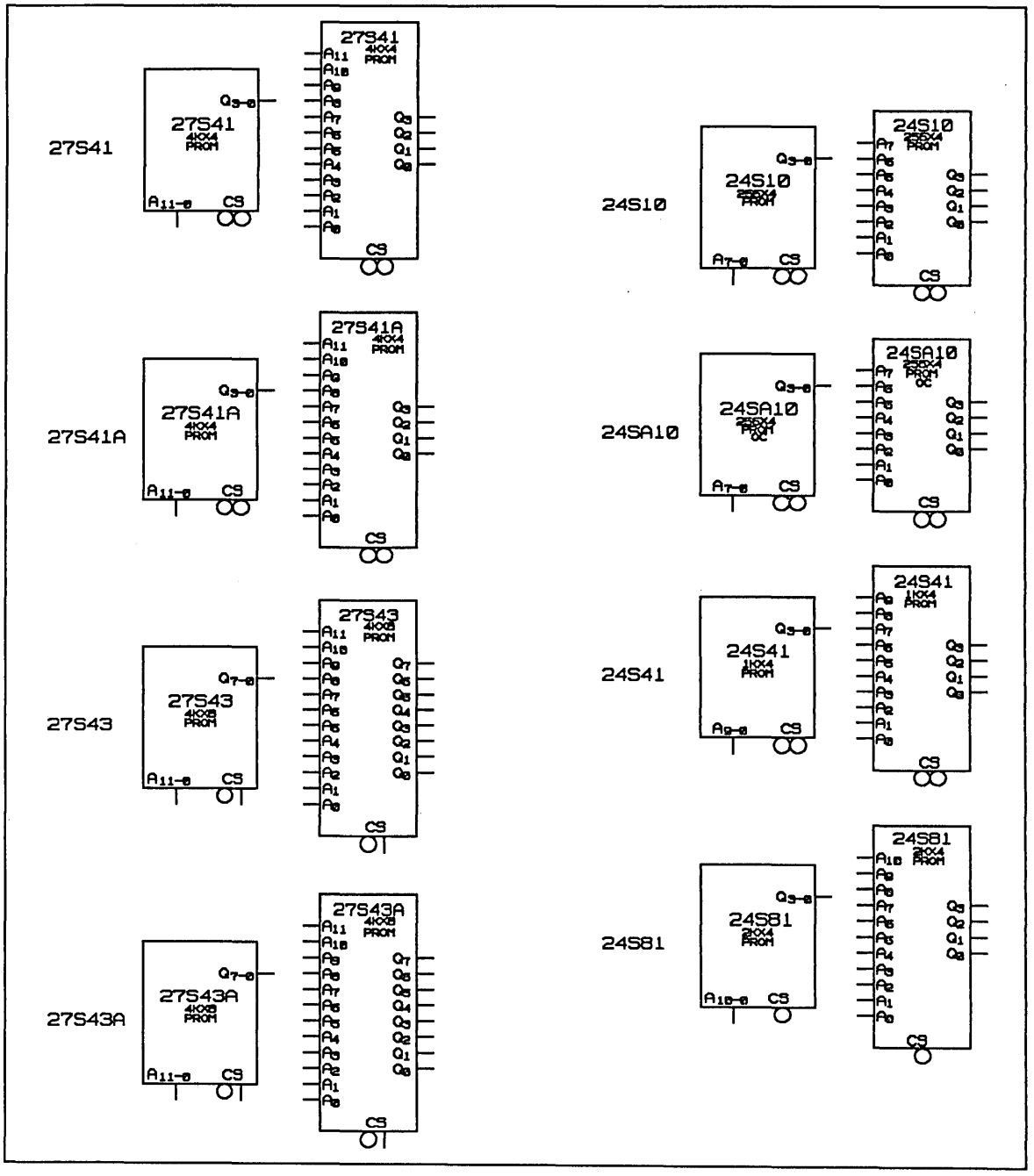


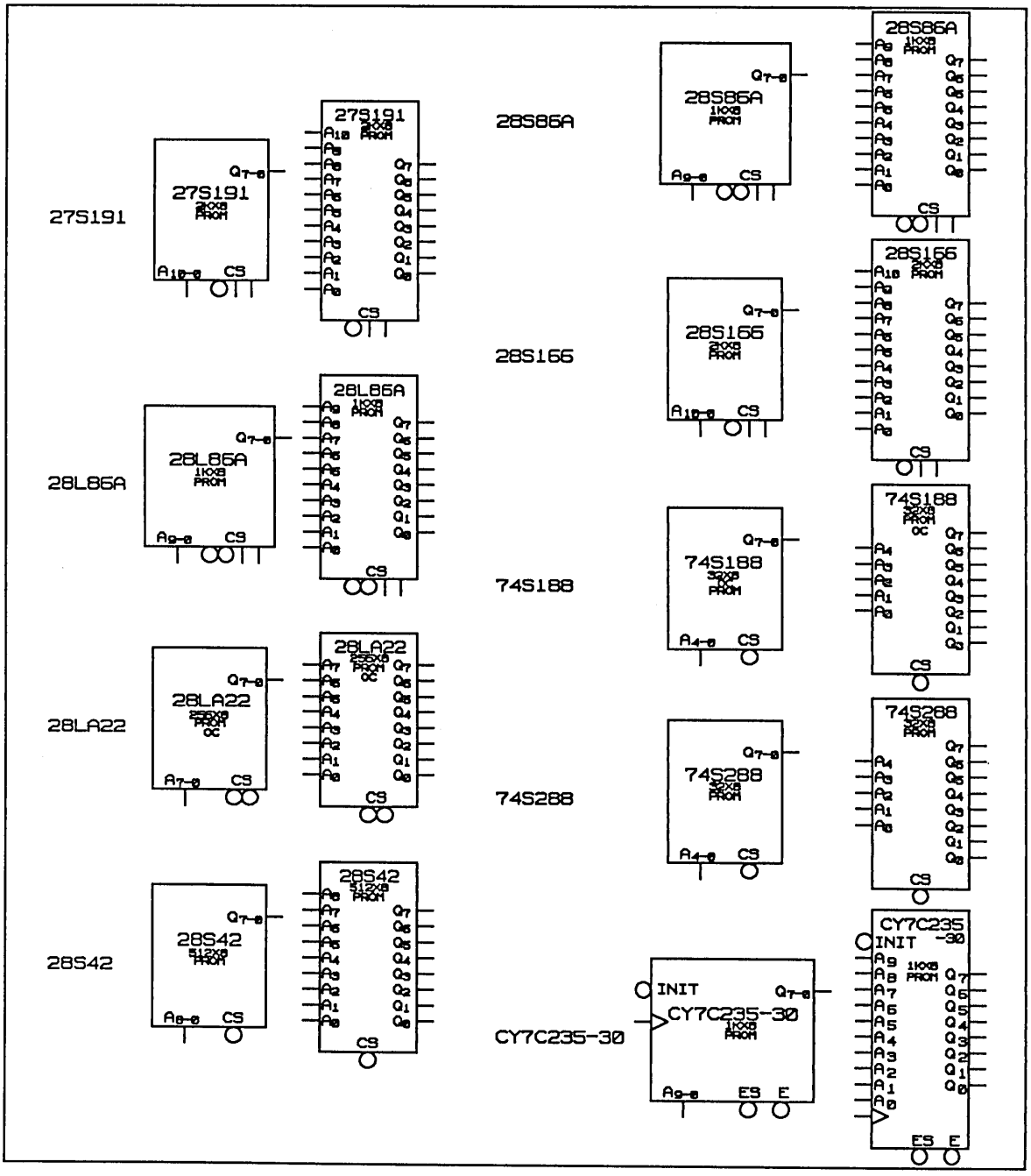
27S291

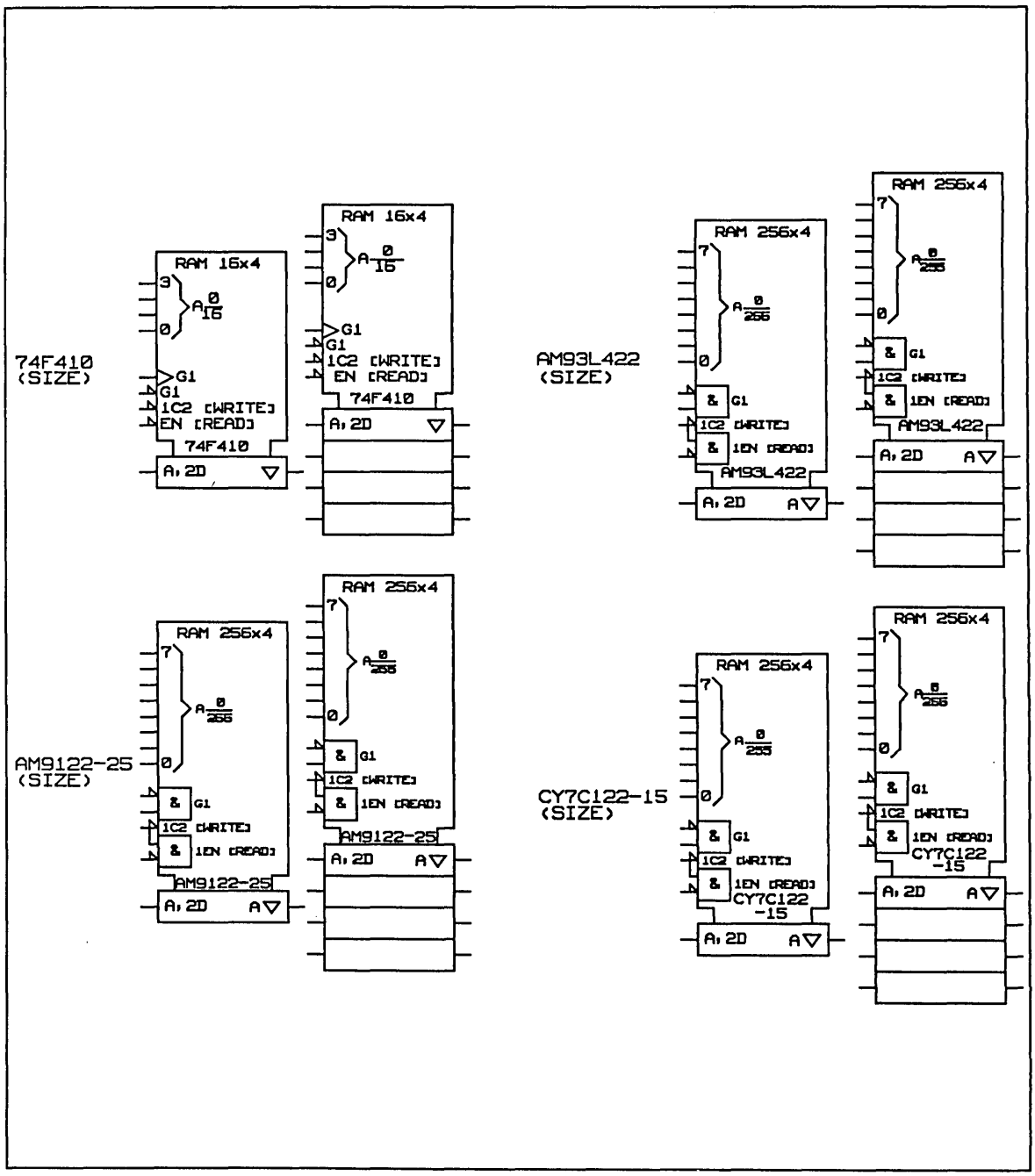


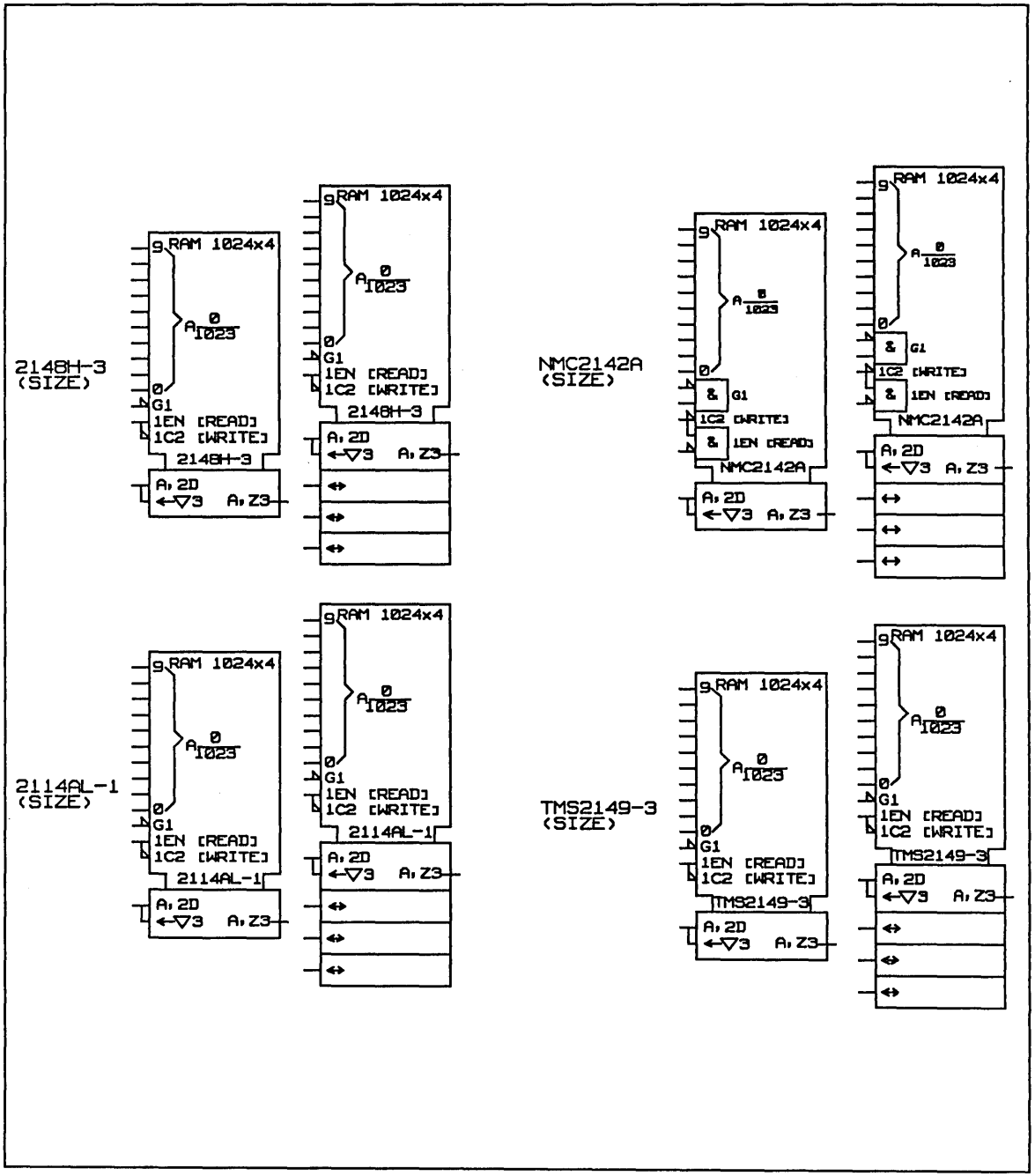
27S291A

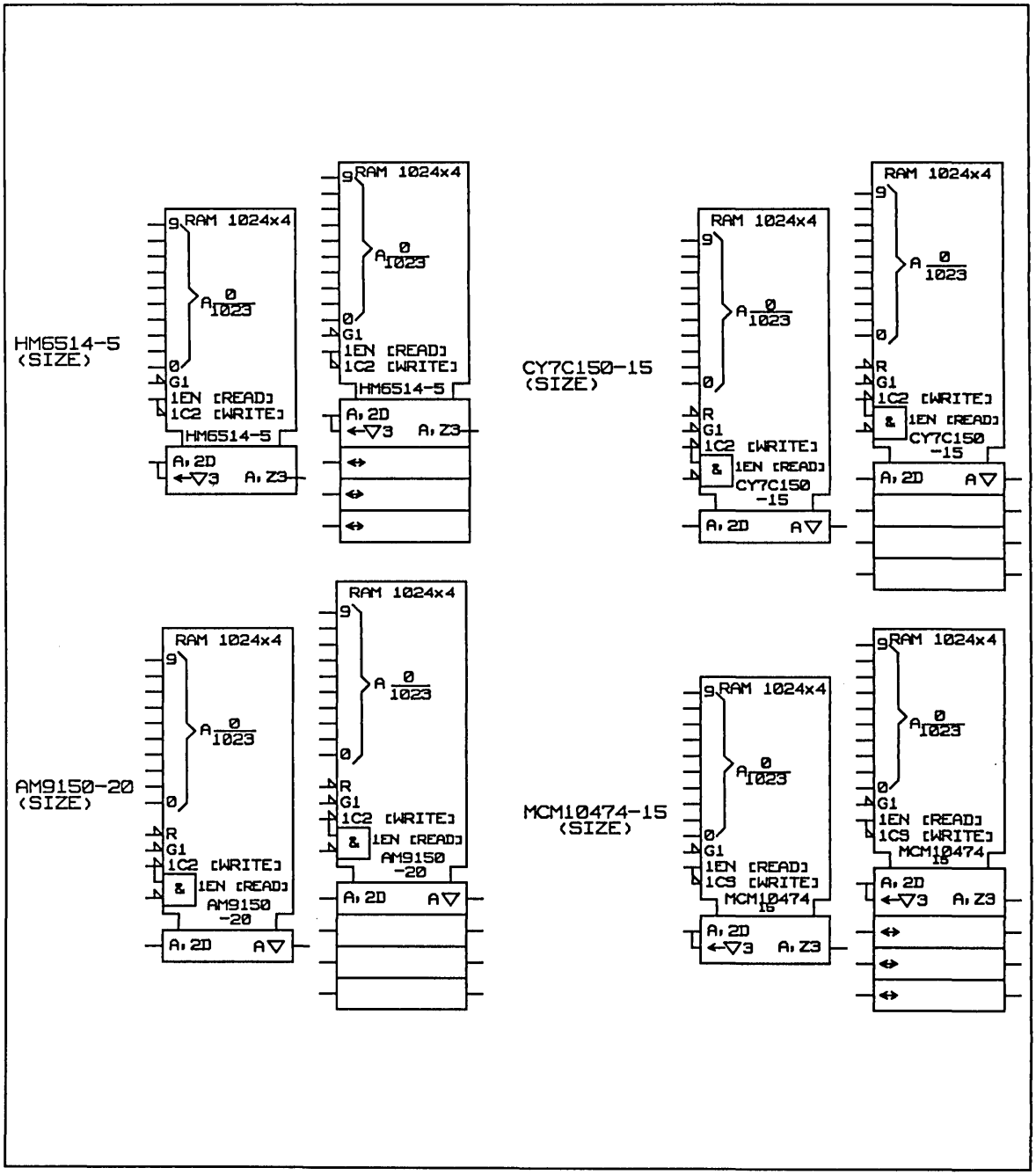


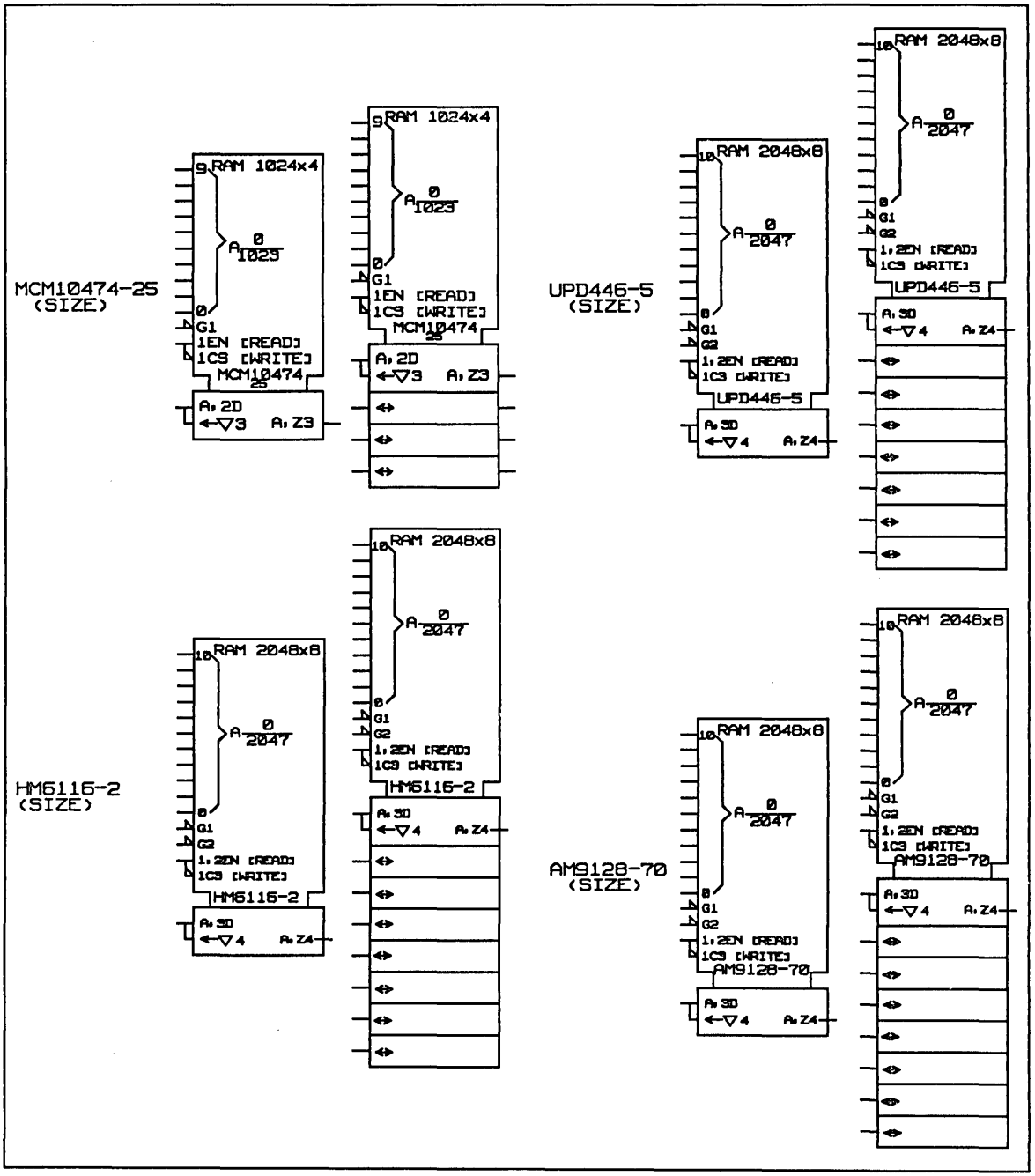

27S41
27S41A
27S43
27S43A
24S10
24SA10
24S41
24S81

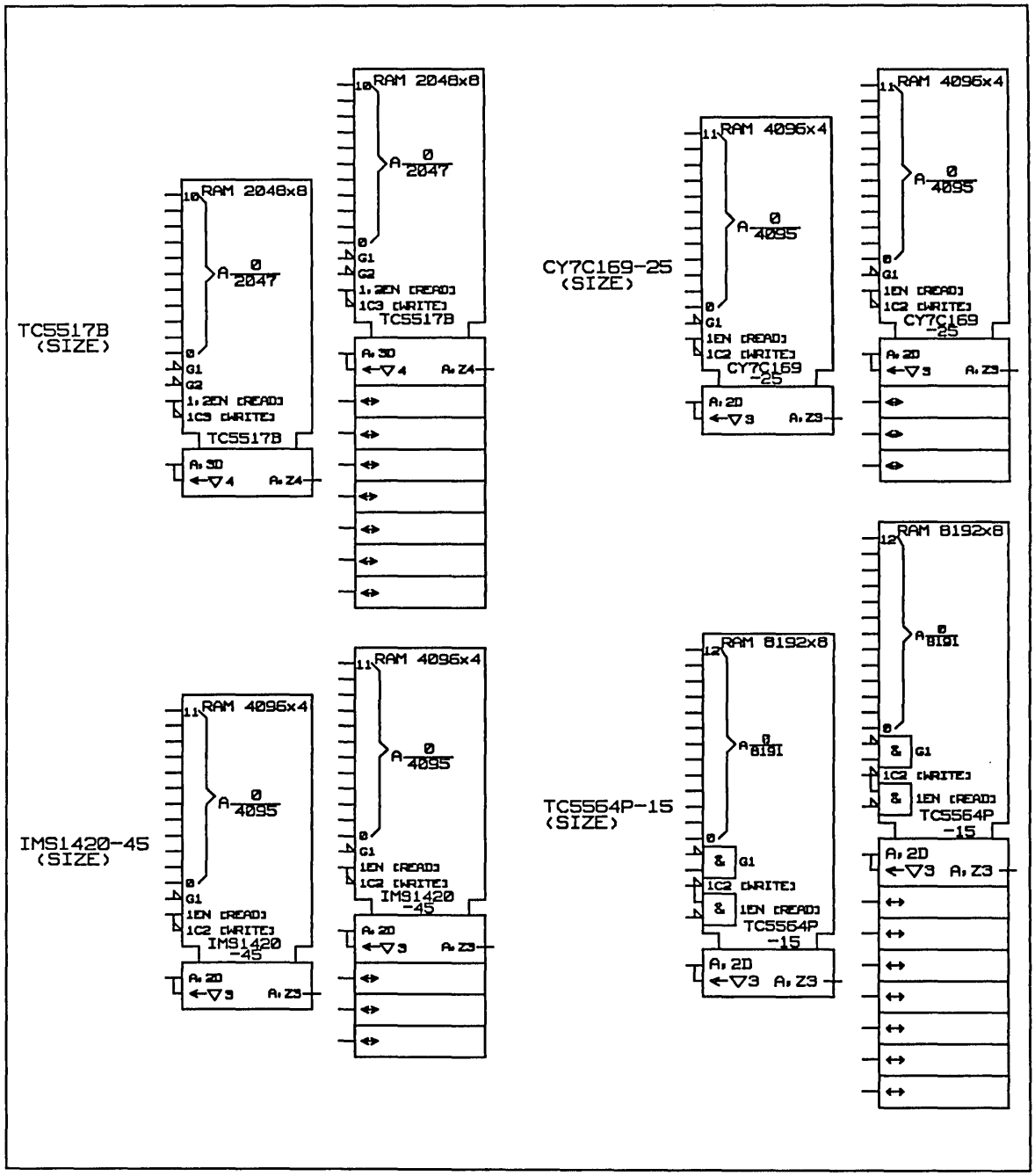

27S191
28S86A
28S166
28L86A
74S188
28LA22
74S288
28S42
CY7C235-30

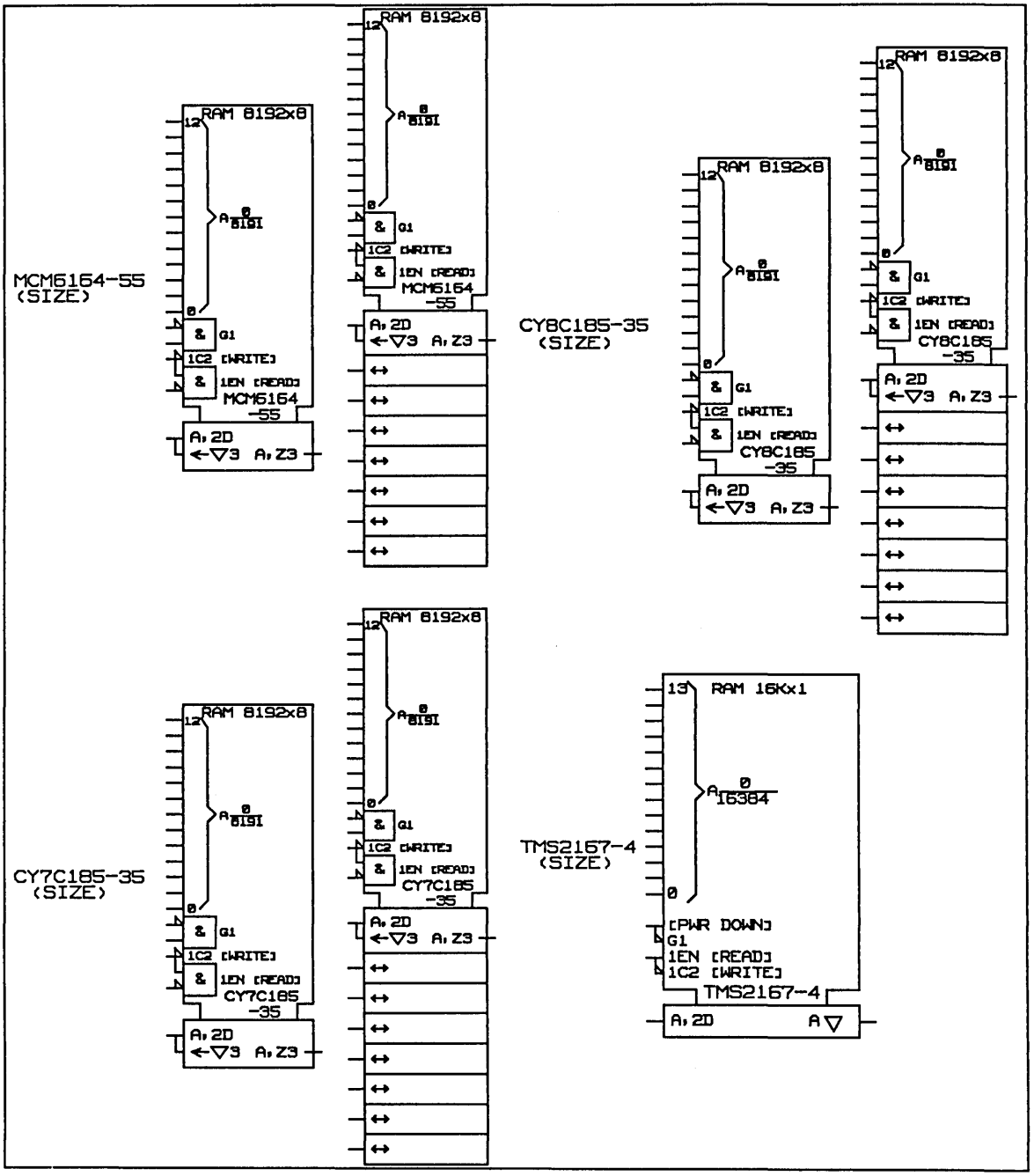

74F410
(SIZE)
RAM 16x4
3
0
A 0/15
G1
1C2 [WRITE]
EN [READ]
74F410
A, 2D
AM93L422
(SIZE)
RAM 256x4
7
0
A 0/255
&
G1
1C2 [WRITE]
1EN [READ]
AM93L422
A, 2D
A
AM9122-25
(SIZE)
AM9122-25
CY7C122-15
(SIZE)
CY7C122
-15

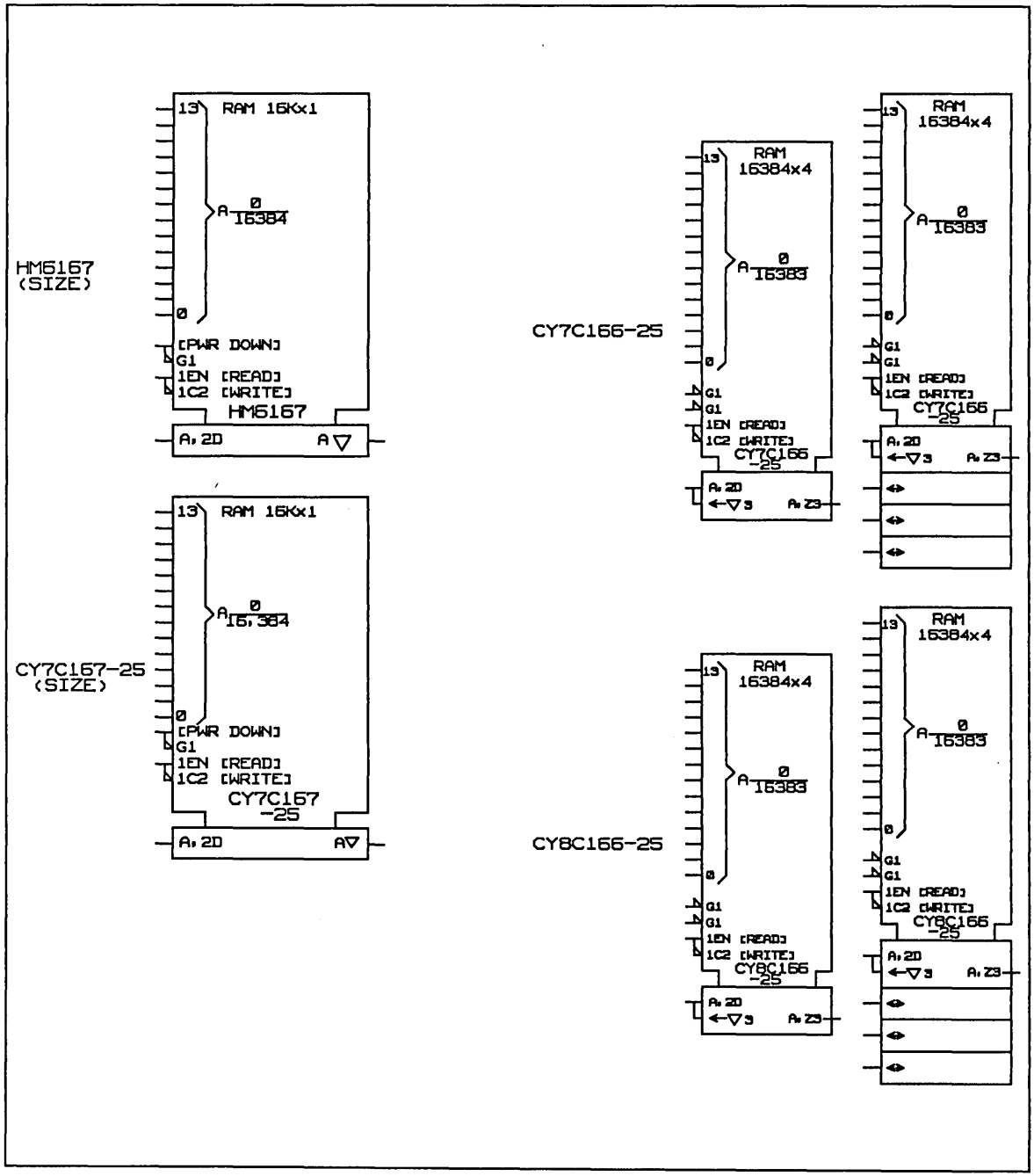

2148H-3
(SIZE)
RAM 1024x4
A 0/1023
G1
1EN [READ]
1C2 [WRITE]
2148H-3
A, 2D
←▽3
A, Z3
NMC2142A
(SIZE)
NMC2142A
2114AL-1
(SIZE)
2114AL-1
TMS2149-3
(SIZE)
TMS2149-3

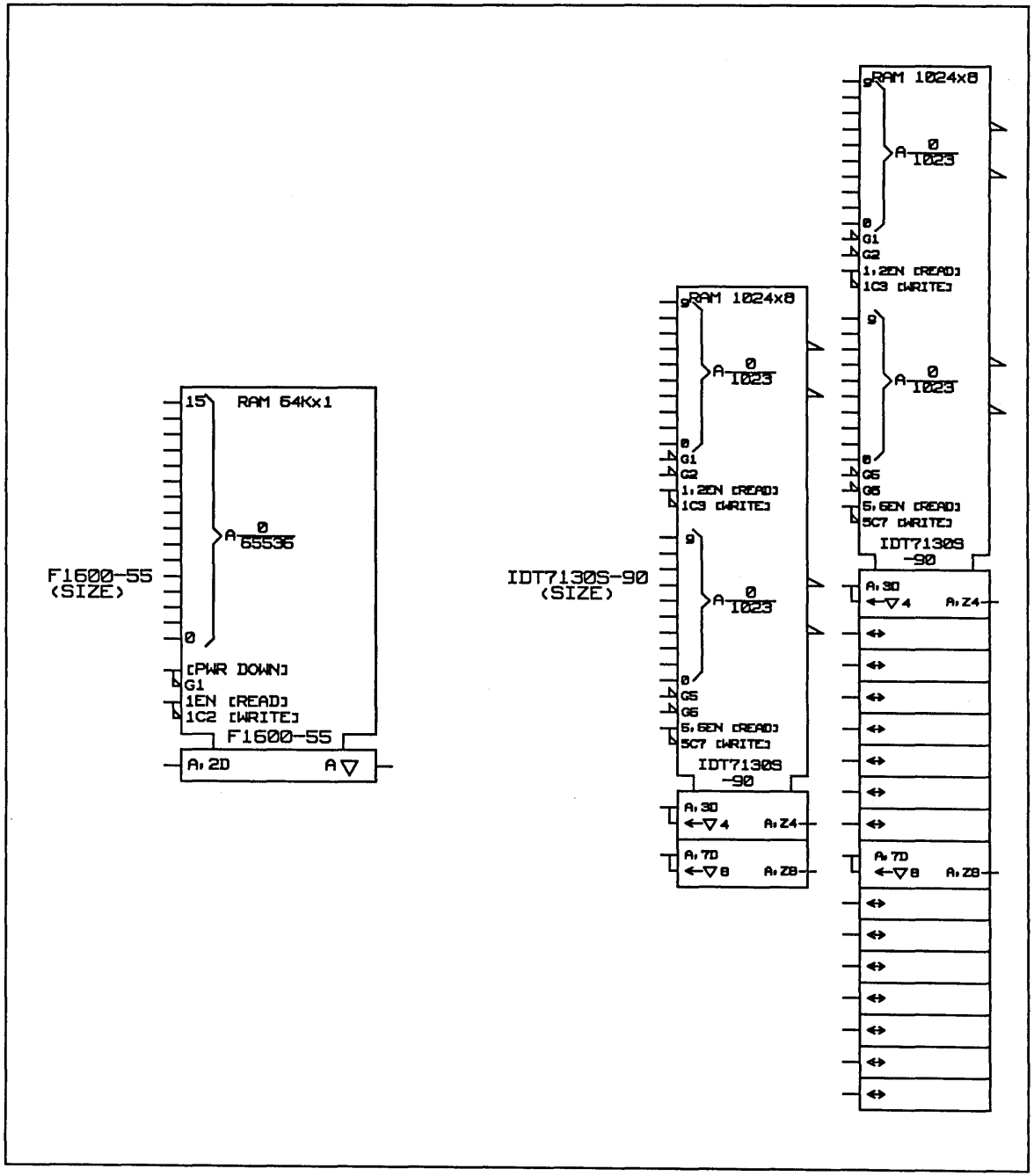

HM6514-5
(SIZE)
RAM 1024x4
A 0 1023
G1
1EN [READ]
1C2 [WRITE]
HM6514-5
A,2D
A,Z3
CY7C150-15
(SIZE)
CY7C150
-15
R
&
AM9150-20
(SIZE)
AM9150
-20
MCM10474-15
(SIZE)
MCM10474
15
1C3 [WRITE]

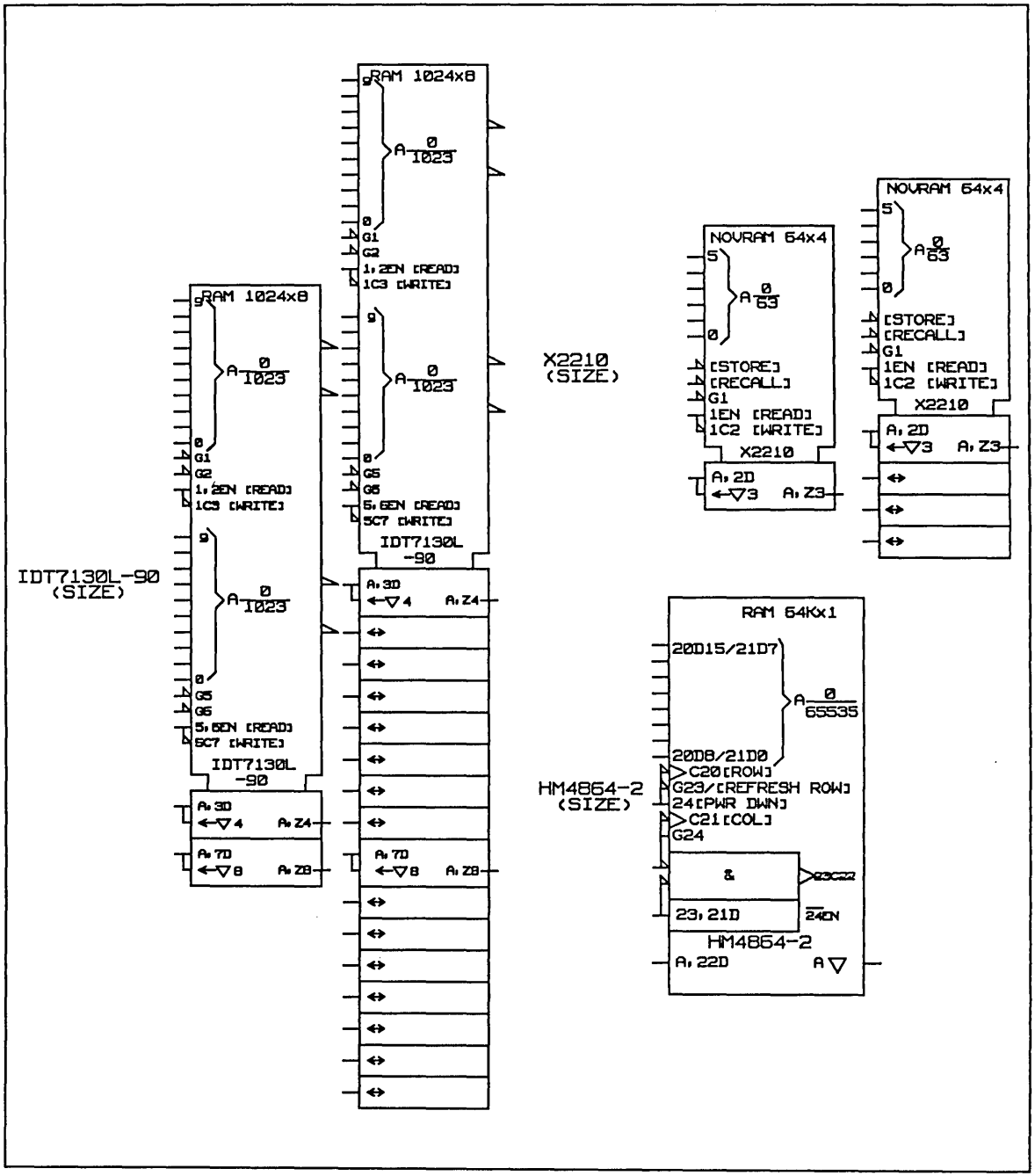

MCM10474-25
(SIZE)
RAM 1024x4
A 0 1023
G1
1EN [READ]
1CS [WRITE]
MCM10474-25
A,2D
A,Z3
UPD446-5
(SIZE)
RAM 2048x8
A 0 2047
G1
G2
1,2EN [READ]
1C9 [WRITE]
UPD446-5
A,3D
A,Z4
HM6116-2
(SIZE)
HM6116-2
AM9128-70
(SIZE)
AM9128-70


TC5517B
(SIZE)
RAM 2048x8
TC5517B
CY7C169-25
(SIZE)
RAM 4096x4
CY7C169
-25
IMS1420-45
(SIZE)
RAM 4096x4
IMS1420
-45
TC5564P-15
(SIZE)
RAM 8192x8
TC5564P
-15

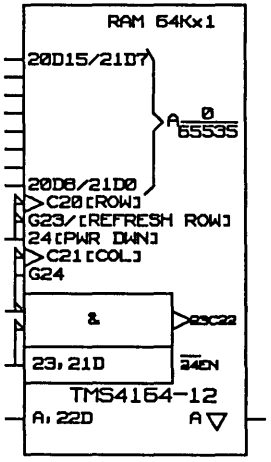

MCM6164-55
(SIZE)
RAM 8192x8
12
A 0 8191
0
& G1
1C2 [WRITE]
& 1EN [READ]
MCM6164
-55
A, 2D
←▽3 A, Z3
CY8C185-35
(SIZE)
CY8C185
-35
CY7C185-35
(SIZE)
CY7C185
-35
TMS2167-4
(SIZE)
13
RAM 16Kx1
A 0 16384
[PWR DOWN]
G1
1EN [READ]
1C2 [WRITE]
TMS2167-4
A, 2D
A▽


HM6167
(SIZE)
13
RAM 16Kx1
A 0 16384
0
[PWR DOWN]
G1
1EN [READ]
1C2 [WRITE]
HM6167
A,2D
A
CY7C167-25
(SIZE)
13
RAM 16Kx1
A 0 16,384
0
[PWR DOWN]
G1
1EN [READ]
1C2 [WRITE]
CY7C167
-25
A,2D
A
CY7C166-25
13
RAM
16384x4
A 0 16383
0
G1
G1
1EN [READ]
1C2 [WRITE]
CY7C166
-25
A,2D
3
A,Z3
CY8C166-25
13
RAM
16384x4
A 0 16383
0
G1
G1
1EN [READ]
1C2 [WRITE]
CY8C166
-25
A,2D
3
A,Z3

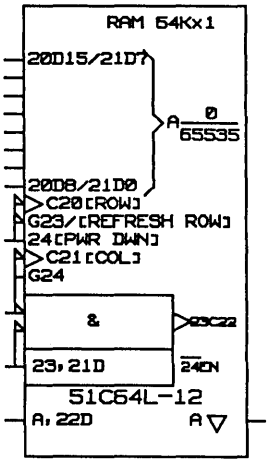

F1600-55
(SIZE)
15
RAM 64Kx1
A 0 65536
0
[PWR DOWN]
G1
1EN [READ]
1C2 [WRITE]
F1600-55
A,2D
A
IDT7130S-90
(SIZE)
RAM 1024x8
A 0 1023
0
G1
G2
1,2EN [READ]
1C3 [WRITE]
G5
G6
5,6EN [READ]
5C7 [WRITE]
IDT7130S
-90
A,3D
A,Z4
A,7D
A,Z8


IDT7130L-90
(SIZE)
RAM 1024x8
A 0 1023
G1
G2
1, 2EN [READ]
1C3 [WRITE]
G5
G6
5, 6EN [READ]
5C7 [WRITE]
IDT7130L
-90
A, 3D
4
A, Z4
A, 7D
8
A, Z8
X2210
(SIZE)
NOVRAM 64x4
A 0 63
[STORE]
[RECALL]
1EN [READ]
1C2 [WRITE]
X2210
A, 2D
3
A, Z3
HM4864-2
(SIZE)
RAM 64Kx1
20D15/21D7
A 0 65535
20D8/21D0
C20 [ROW]
G23/[REFRESH ROW]
24[PWR DWN]
C21 [COL]
G24
&
23, 21D
HM4864-2
A, 22D
A

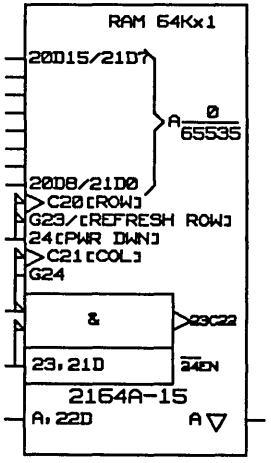
TMS4164-12
(SIZE)



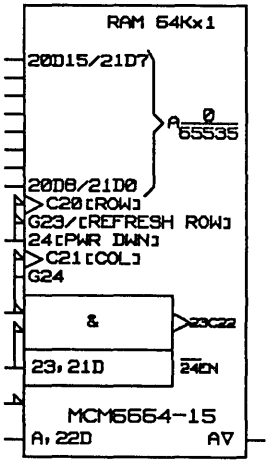
51C64L-12
(SIZE)

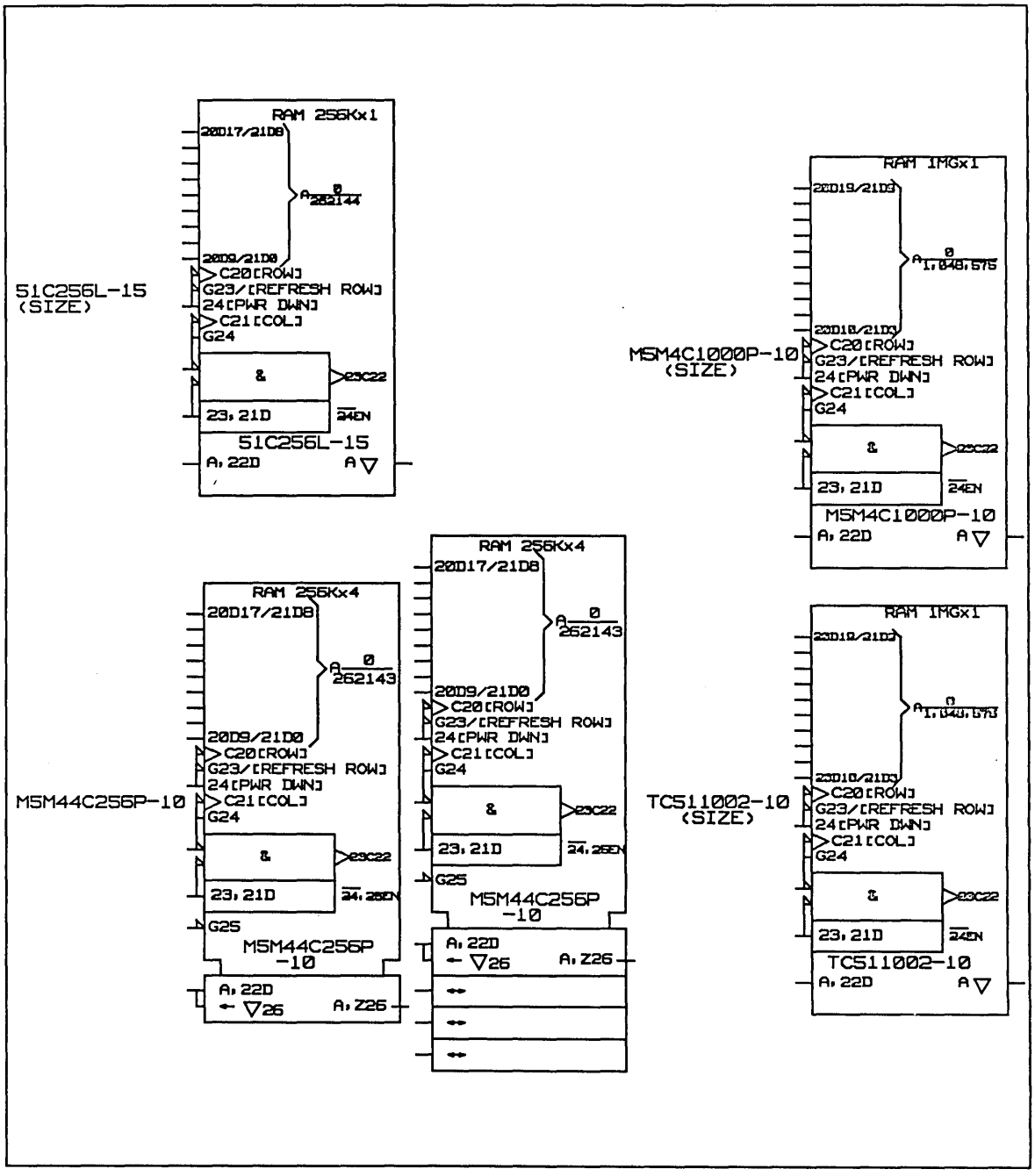


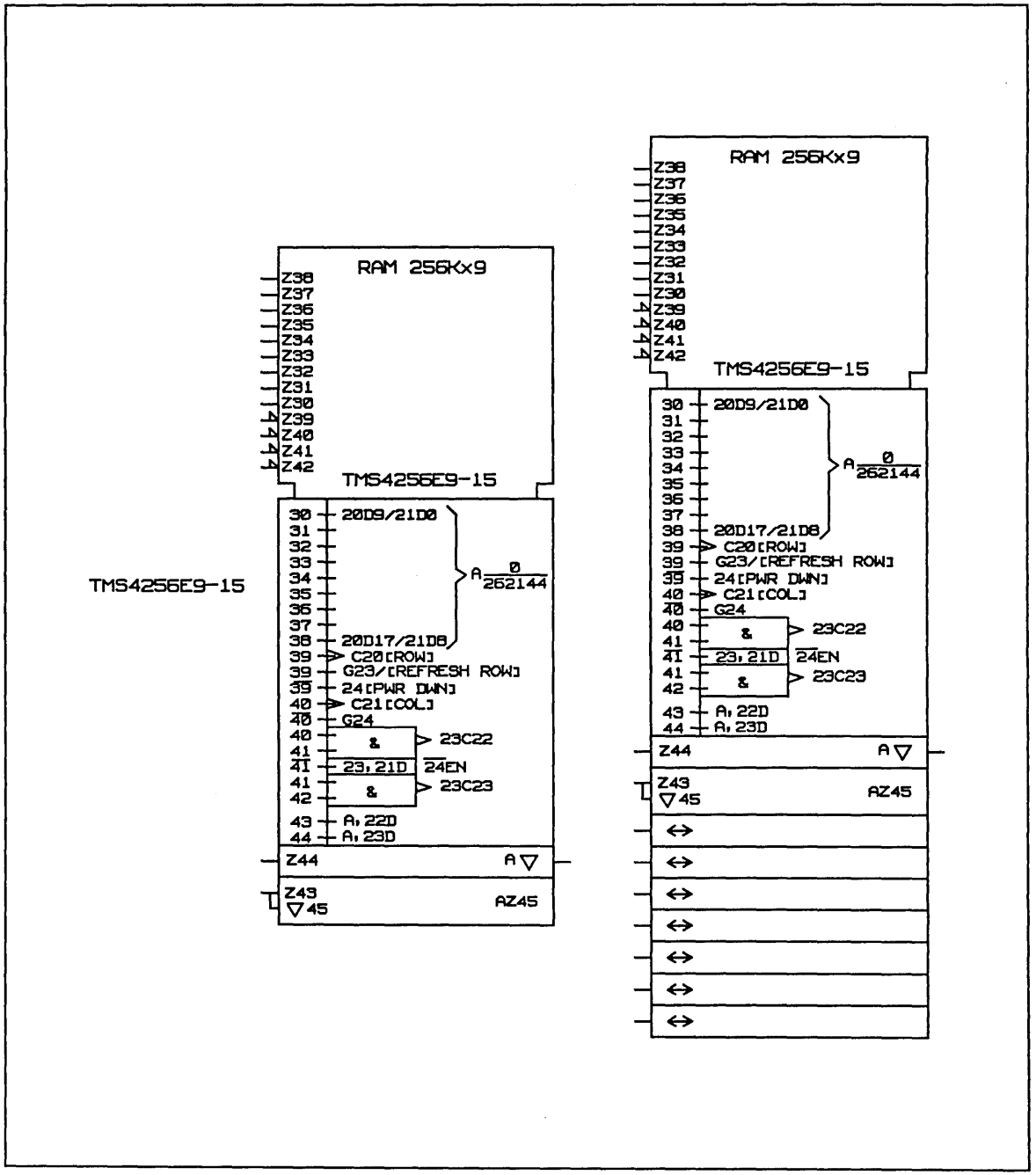
2164A-15
(SIZE)

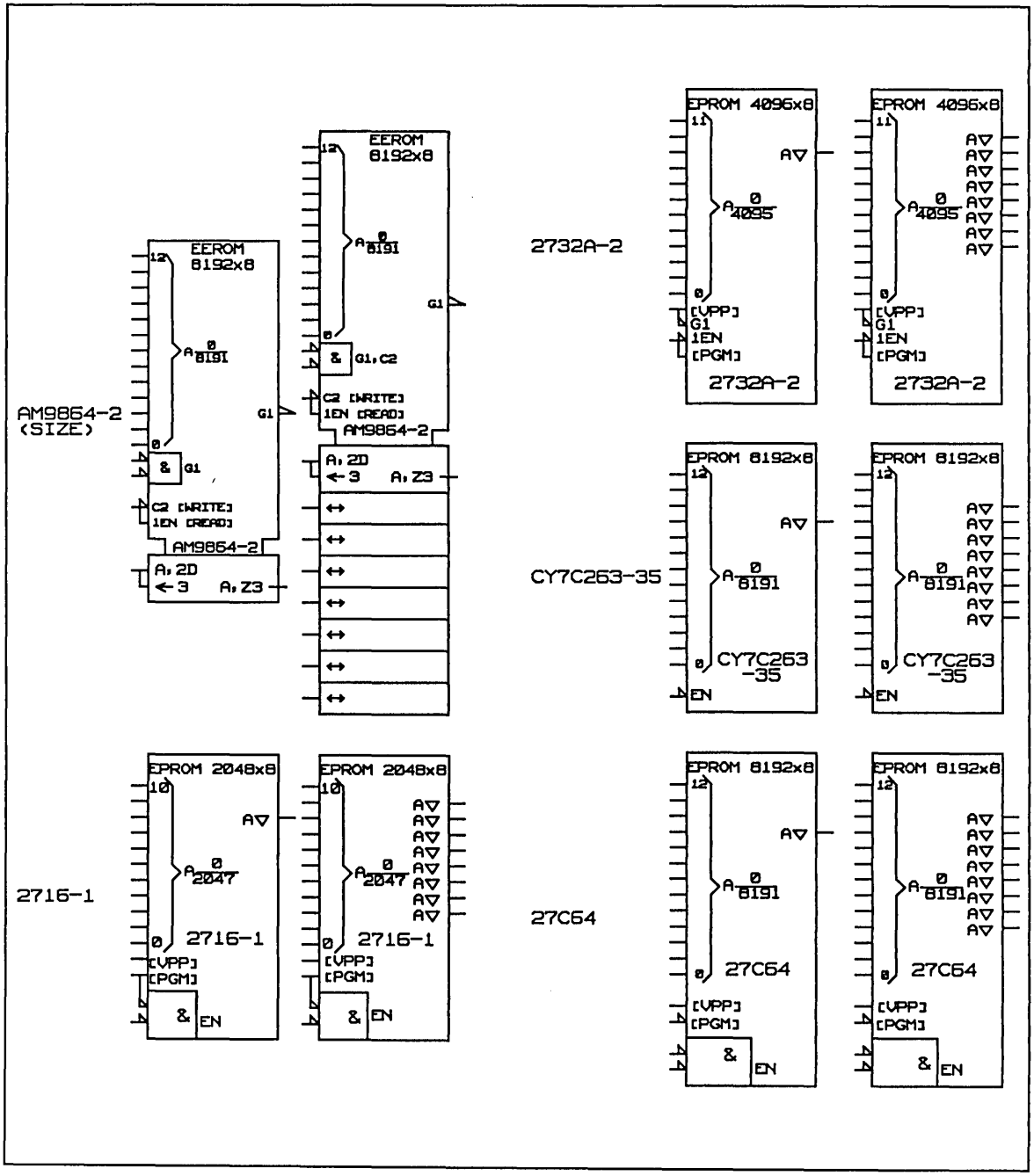


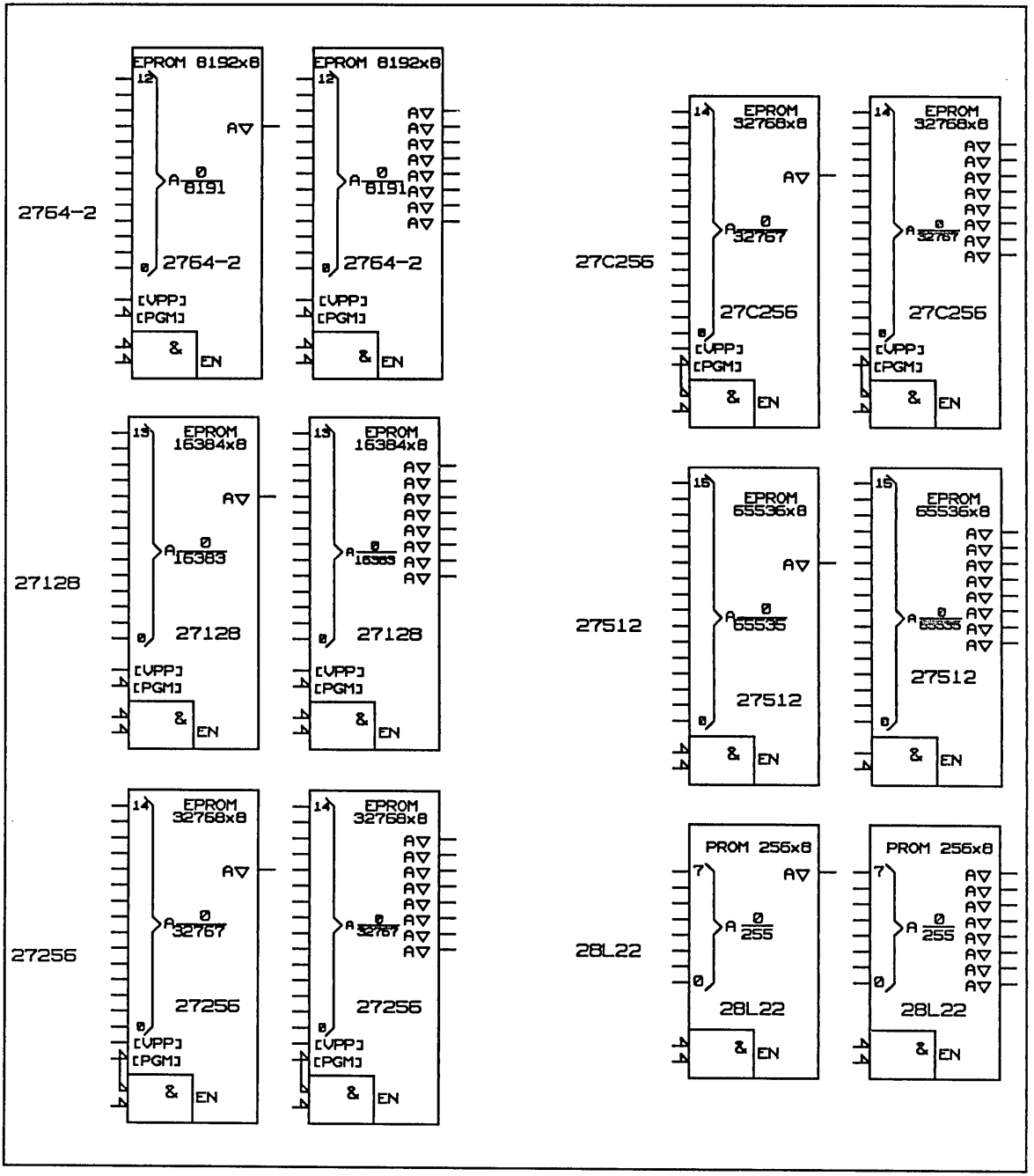
MCM6664-15
(SIZE)

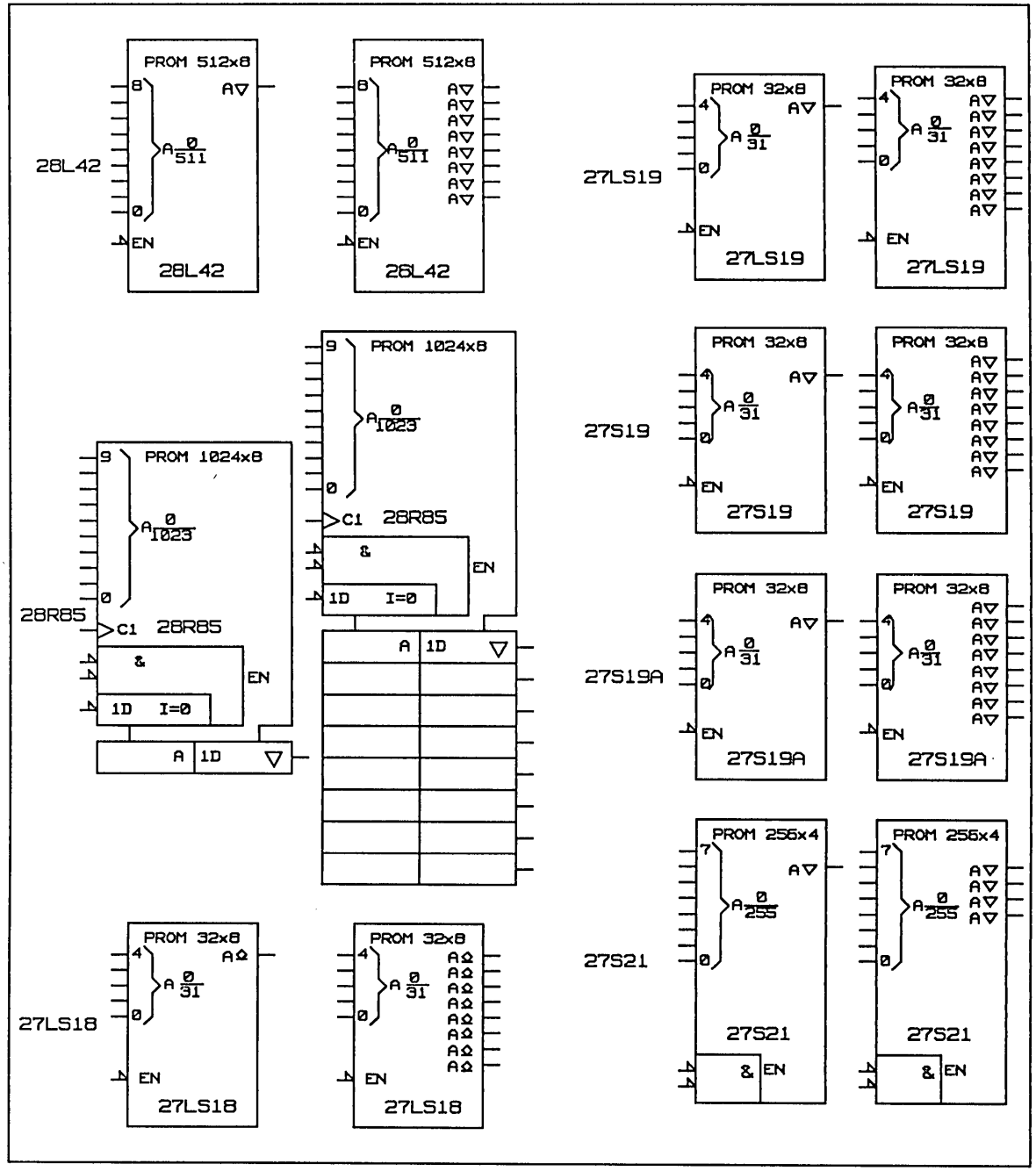


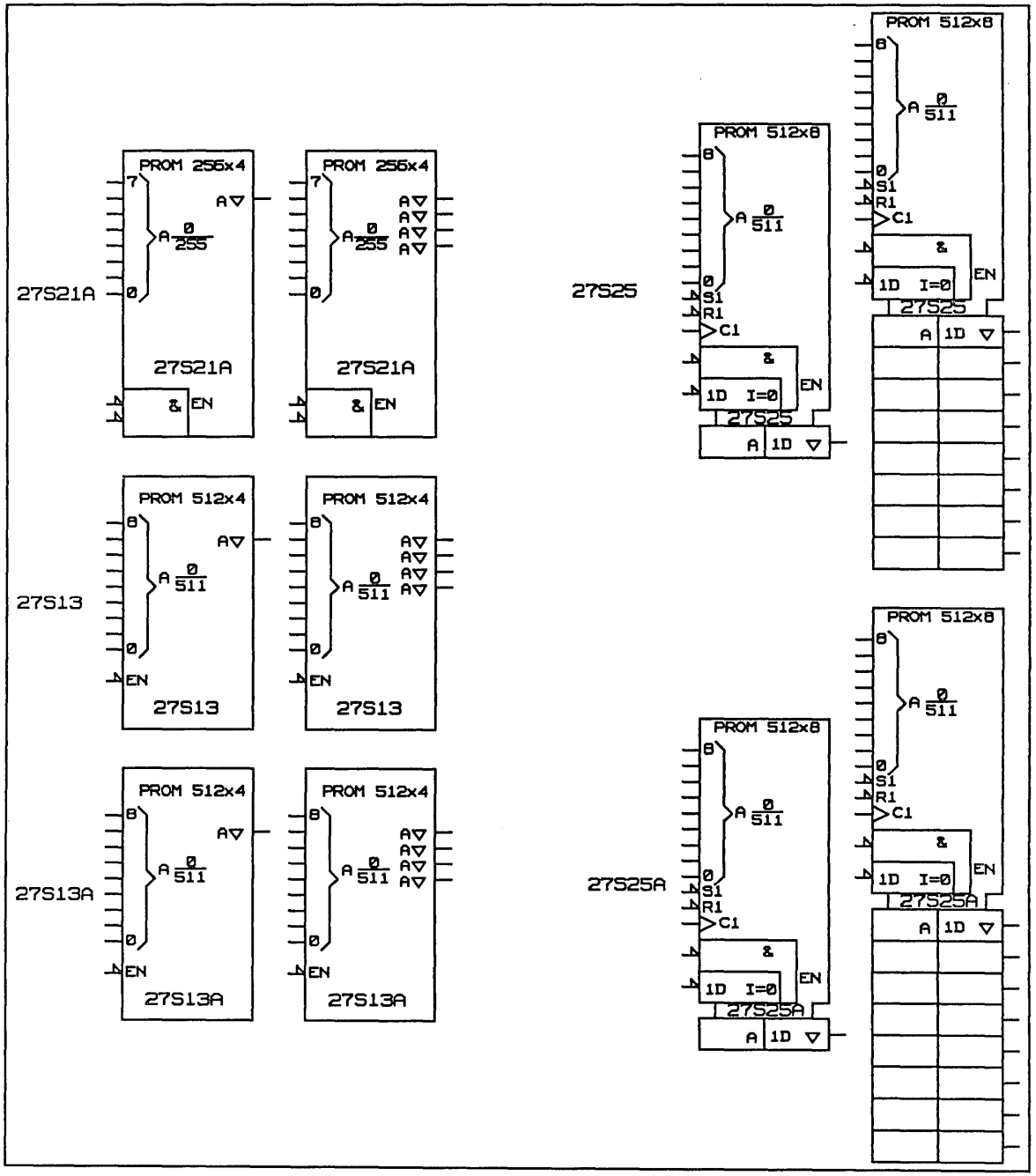

51C256L-15
(SIZE)
RAM 256Kx1
20D17/21D8
A 0 262144
20D9/21D0
C20[ROW]
G23/[REFRESH ROW]
24[PWR DWN]
C21[COL]
G24
&
23, 21D
23C22
24EN
51C256L-15
A, 22D
A
M5M4C1000P-10
(SIZE)
RAM 1MGx1
22D19/21D9
A 0 1,048,575
22D18/21D8
M5M4C1000P-10
M5M44C256P-10
RAM 256Kx4
20D17/21D8
A 0 262143
20D9/21D0
C20[ROW]
G23/[REFRESH ROW]
24[PWR DWN]
C21[COL]
G24
&
23, 21D
23C22
24, 25EN
G25
M5M44C256P
-10
A, 22D
26
A, Z26
TC511002-10
(SIZE)
RAM 1MGx1
22D19/21D9
A 0 1,048,575
22D18/21D8
TC511002-10

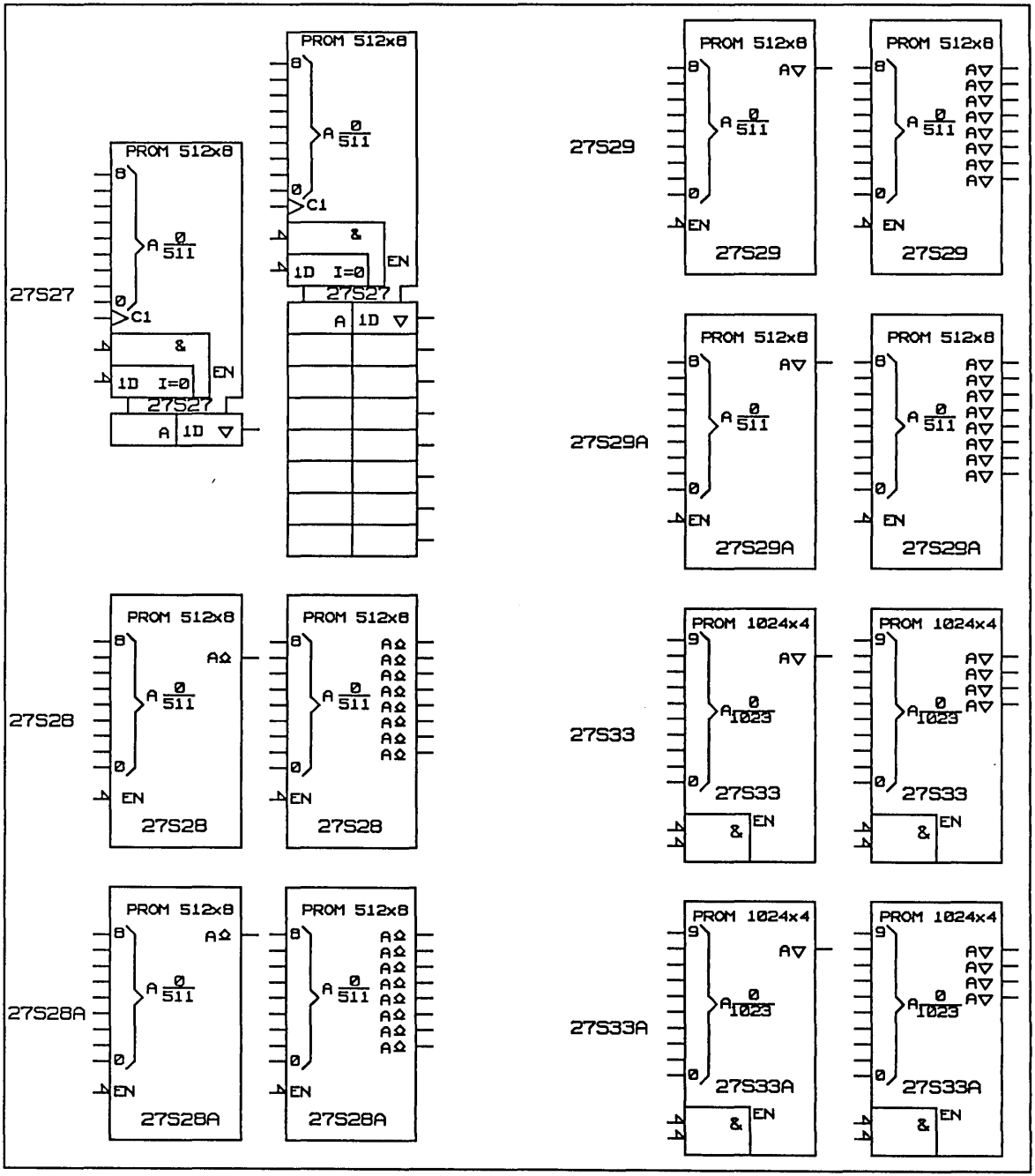

TMS4256E9-15
RAM 256Kx9
TMS4256E9-15
RAM 256Kx9
TMS4256E9-15

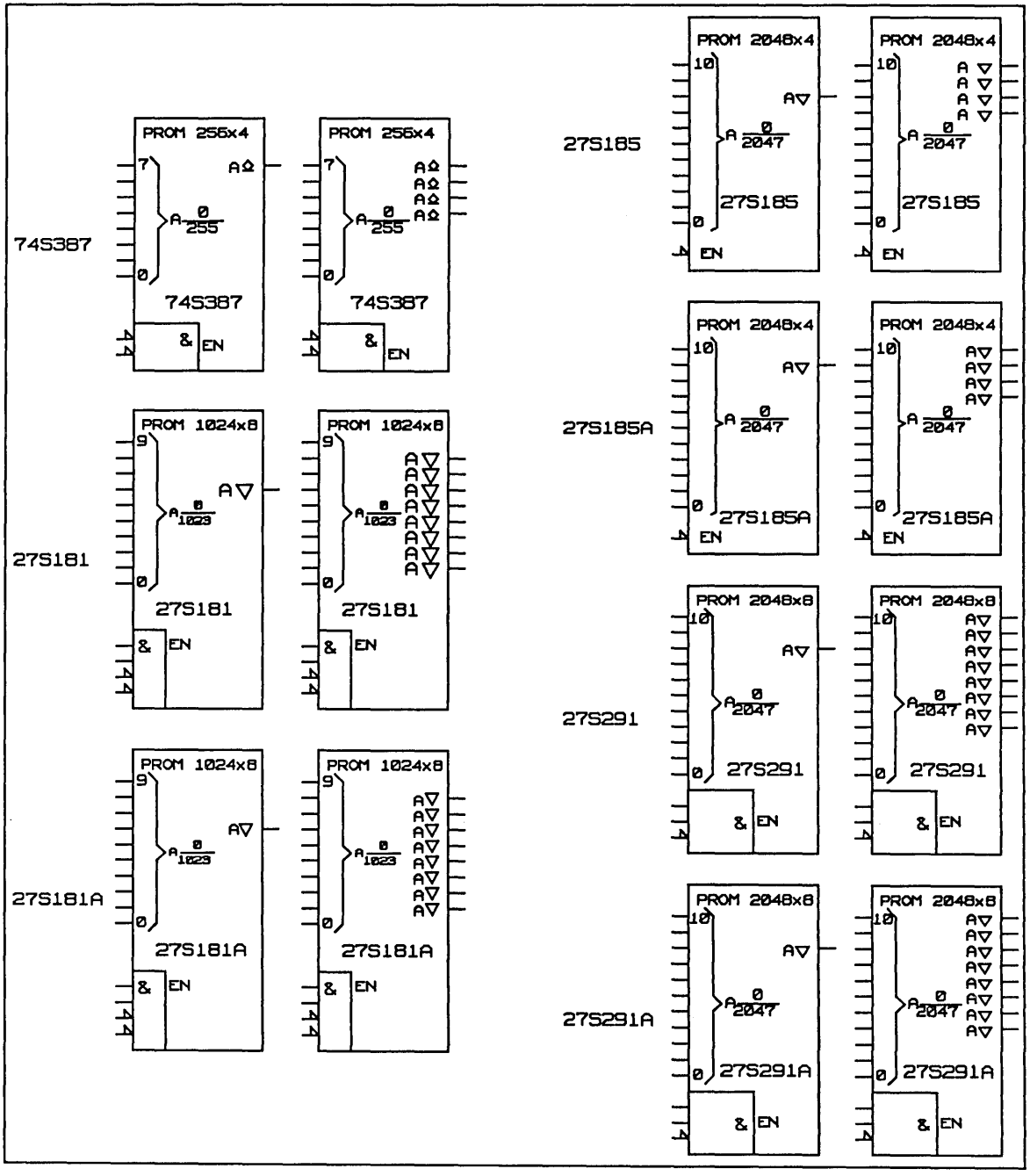

AM9864-2
(SIZE)
EEROM
8192x8
A 0 8191
G1
&
G1, C2
C2 [WRITE]
1EN [READ]
AM9864-2
A, 2D
←3
A, Z3
2732A-2
EPROM 4096x8
A 0 4095
[VPP]
G1
1EN
[PGM]
CY7C263-35
EPROM 8192x8
A 0 8191
CY7C263
-35
EN
2716-1
EPROM 2048x8
A 0 2047
2716-1
[VPP]
[PGM]
27C64
EPROM 8192x8
A 0 8191
27C64
[VPP]
[PGM]
EN

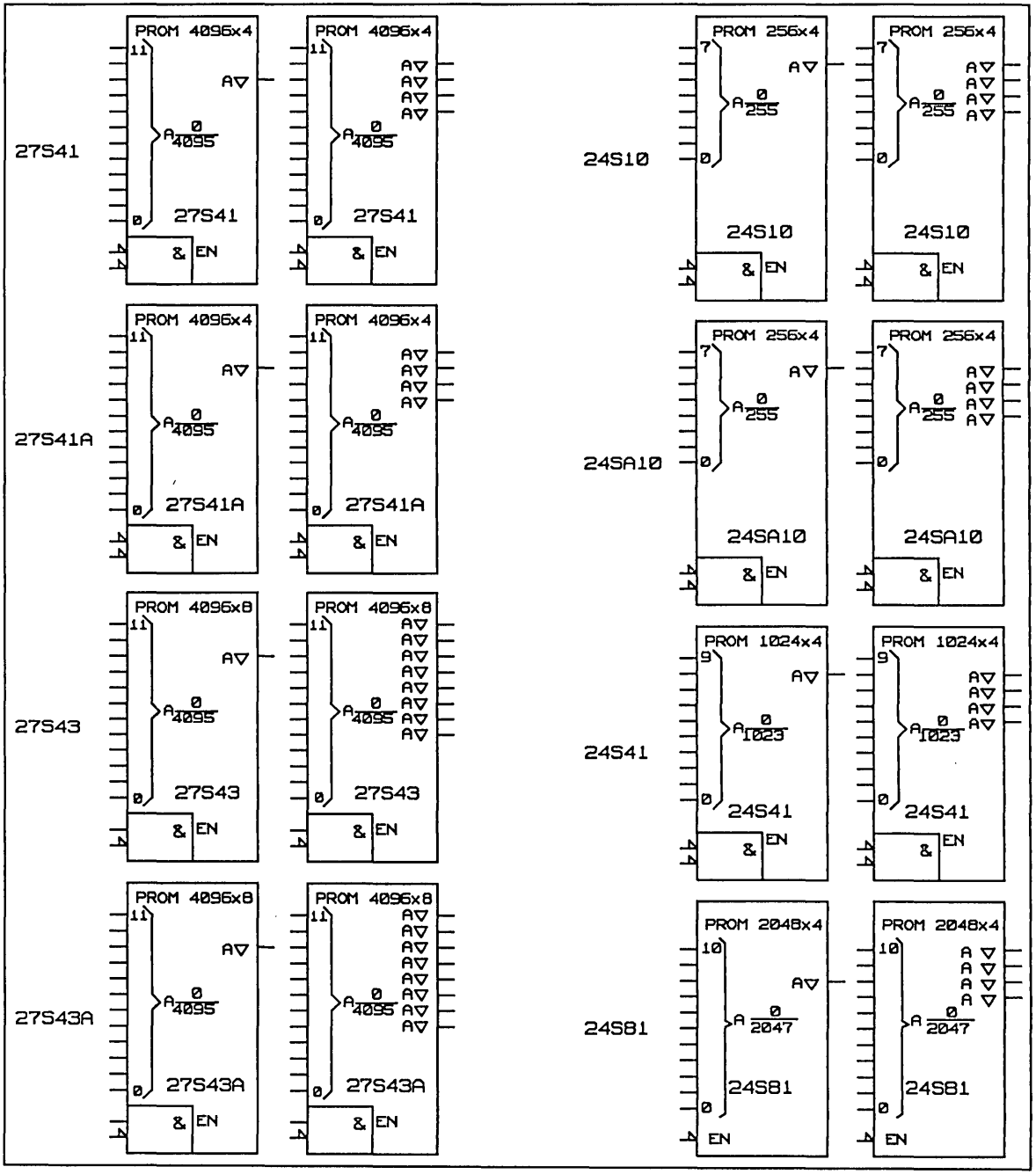

2764-2
EPROM 8192x8
12
A
0
8191
0
2764-2
[VPP]
[PGM]
&
EN
27128
EPROM 16384x8
13
16383
27128
27256
EPROM 32768x8
14
32767
27256
27C256
EPROM 32768x8
14
32767
27C256
27512
EPROM 65536x8
15
65535
27512
28L22
PROM 256x8
7
255
28L22

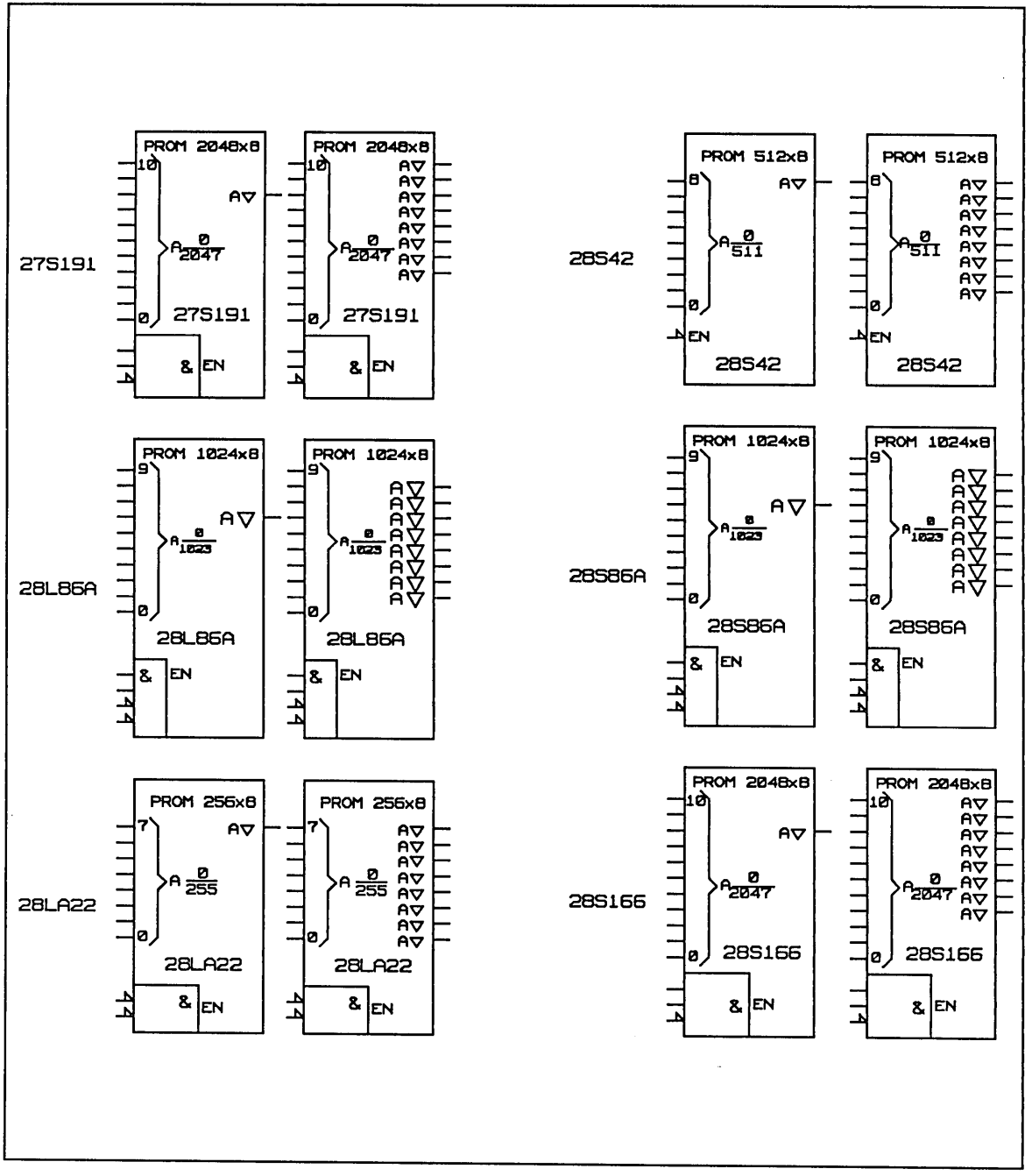

28L42
PROM 512x8
28L42
PROM 512x8
26L42
27LS19
PROM 32x8
27LS19
PROM 32x8
27LS19
27S19
PROM 32x8
27S19
PROM 32x8
27S19
28R85
PROM 1024x8
28R85
PROM 1024x8
28R85
27S19A
PROM 32x8
27S19A
PROM 32x8
27S19A
27LS18
PROM 32x8
27LS18
PROM 32x8
27LS18
27S21
PROM 256x4
27S21
PROM 256x4
27S21


27S21A
PROM 256x4
27S21A
27S13
PROM 512x4
27S13
27S13A
PROM 512x4
27S13A
27S25
PROM 512x8
27S25
27S25A
PROM 512x8
27S25A

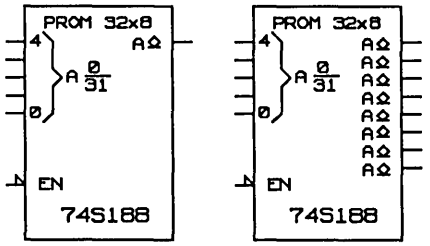

27S27
PROM 512x8
A 0 511
C1
&
1D I=0
EN
27S27
A 1D
27S29
PROM 512x8
A
EN
27S29
27S29A
PROM 512x8
27S29A
27S28
PROM 512x8
27S28
27S28A
PROM 512x8
27S28A
27S33
PROM 1024x4
A 0 1023
27S33
27S33A
PROM 1024x4
27S33A


74S387
PROM 256x4
74S387
27S181
PROM 1024x8
27S181
27S181A
PROM 1024x8
27S181A
27S185
PROM 2048x4
27S185
27S185A
PROM 2048x4
27S185A
27S291
PROM 2048x8
27S291
27S291A
PROM 2048x8
27S291A
EN

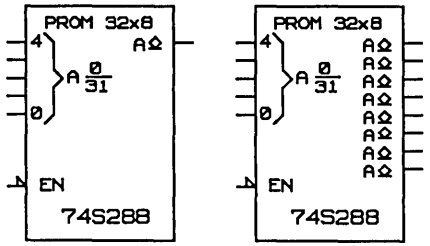

27S41
PROM 4096x4
11
A∇
0
A4095
0
27S41
&
EN
44
27S41A
27S43
PROM 4096x8
27S43A
24S10
PROM 256x4
7
A255
24S10
24SA10
24S41
PROM 1024x4
9
A1023
24S41
24S81
PROM 2048x4
10
A2047
24S81


27S191
PROM 2048x8
10
A
A2047
0
27S191
&
EN
4
PROM 2048x8
10
A
A2047
0
27S191
&
EN
4
28S42
PROM 512x8
8
A
A511
0
EN
28S42
PROM 512x8
8
A
A511
0
EN
28S42
28L86A
PROM 1024x8
9
A
A1023
0
28L86A
&
EN
4
PROM 1024x8
9
A
A1023
0
28L86A
&
EN
4
28S86A
PROM 1024x8
9
A
A1023
0
28S86A
&
EN
4
PROM 1024x8
9
A
A1023
0
28S86A
&
EN
4
28LA22
PROM 256x8
7
A
A255
0
28LA22
&
EN
4
PROM 256x8
7
A
A255
0
28LA22
&
EN
4
28S166
PROM 2048x8
10
A
A2047
0
28S166
&
EN
4
PROM 2048x8
10
A
A2047
0
28S166
&
EN
4

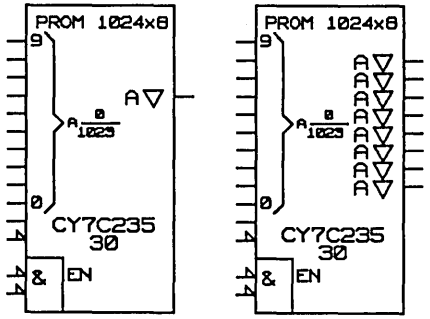
74S188

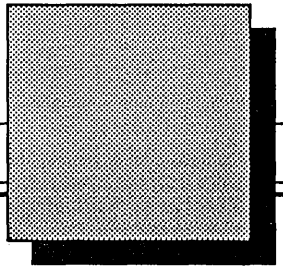


74S288



CY7C235-30





The MM74C Library

The MM74C Library requires approximately 359 Kbytes of disk storage.

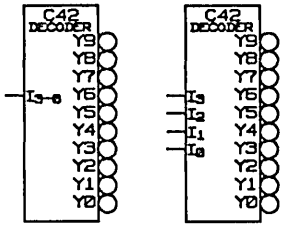
The specifications used to construct the models in this library were taken from the National Semiconductor Data Books.

The release level of the MM74C Library is 9.0.

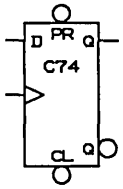
The library contains body drawings and physical, timing, and simulation models for the following 10 components:

C42	BCD-to-decimal decoder
C74	Dual D-type flip-flop
C154	4-line to 16-line decoder/demultiplexer
C157	Quad 2-input multiplexers
C192	Synchronous 4-bit up/down decade counter
C373	3-state octal D-type latch
C374	3-state octal D-type flip-flop
C902	Hex non-inverting TTL buffer
C910	256-bit 3-state random access read/write memory
C914	Hex Schmitt trigger with extended input voltage

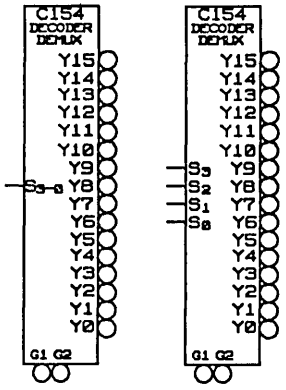
C42



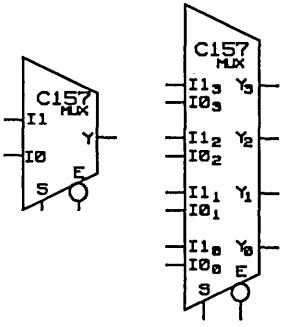
C74
(SIZE)



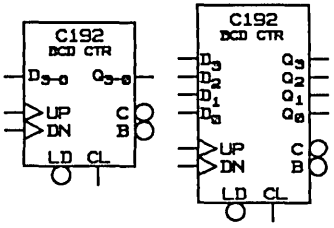
C154



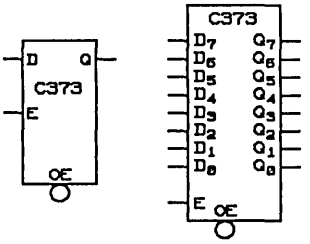
C157
(SIZE)



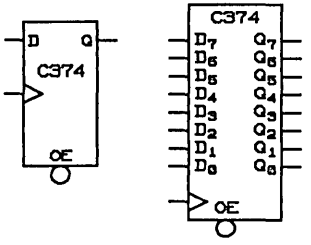
C192



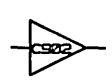
C373
(SIZE)



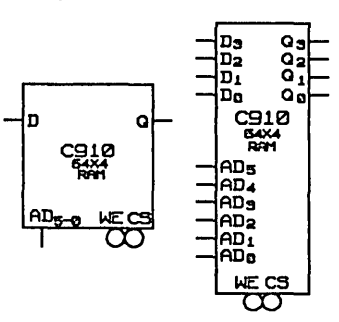
C374
(SIZE)



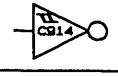
C902
(SIZE)

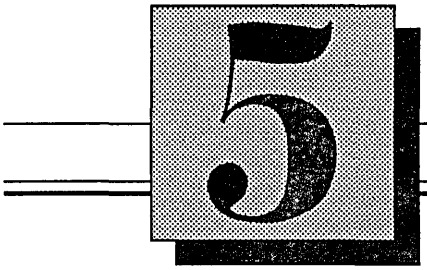


C910
(SIZE)



C914
(SIZE)

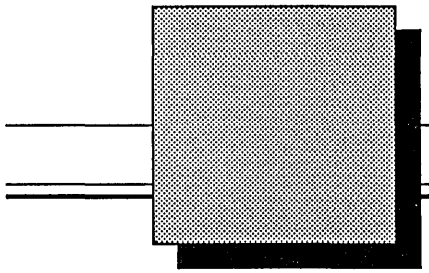




ECL Libraries

This section describes the individual libraries that make up the ECL libraries.

Contents



The 10K Library

The 10K Library requires approximately 2196 kbytes of disk storage.

The specifications used to construct the models in this library were taken from the Motorola Data Books.

The release level of the ECL 10K Library is 9.0.

The 10K library contains body drawings and physical, timing, and simulation models for the following 68 components:

10016	Counter
10100	Quad 2-input NOR with strobe
10101	Quad OR/NOR
10102	Quad 2-input NOR
10103	Quad 2-input OR
10104	Quad 2-input AND
10105	Triple 2-3-2-input OR/NOR
10106	Triple 4-3-3-input NOR
10107	Triple 2-input exclusive-OR/exclusive-NOR
10109	Dual 4-5-input OR/NOR
10110	Dual 3-input 3-output OR
10111	Dual 3-input 3-output NOR
10113	Quad exclusive-OR
10115	Quad line receiver
10116	Triple line receiver
10117	Dual 2-wide 2-3-input OR-AND/OR-AND-invert
10118	Dual 2-wide 3-input OR-AND
10119	4-wide 4-3-3-3-input OR-AND
10121	4-wide OR-AND/OR-AND-invert
10123	Triple 4-3-3 input bus driver
10124	Quad MTTL-to-MECL translator
10125	Quad MECL-to-MTTL translator
10130	Dual latch
10131	Dual D-type master-slave flip-flop
10132	Dual multiplexer with latch and common reset

10133	Quad latch
10134	Dual multiplexer with latch
10135	Dual JK master-slave flip-flop
10136	Universal hexadecimal counter
10137	Universal decade counter
10141	4-bit universal shift register
10145	16 X 4 register file
10153	Quad latch
10154	Binary Counter
10158	Quad 2-input multiplexer
10159	Quad 2-input inverting multiplexer
10160	12-bit parity generator/checker
10161	Binary to 1-of-8 decoder (low)
10162	Binary to 1-of-8 decoder (high)
10163	Error detection/correction circuit
10164	8-line multiplexer
10165	8-input priority encoder
10166	5-bit magnitude comparator
10168	Quad latch
10170	9 plus 2-bit parity generator/checker
10171	Dual binary to 1-of-4 decoder (low)
10172	Dual binary to 1-of-4 decoder (high)
10173	Quad 2-input multiplexer/latch
10174	Dual 4-to-1 multiplexer
10175	Quint latch

10176	Hex D-type master-slave flip-flop
10179	Look-ahead carry block
10180	Dual 2-bit adder/subtractor
10181	4-bit arithmetic logic unit and function generator
10186	Hex D-type master-slave flip-flop with reset
10188	Hex buffer with enable
10189	Hex inverter with enable
10192	Quad bus driver
10195	Hex inverter/buffer
10197	Hex AND
10210	High-speed dual 3-input 3-output OR gate
10211	High-speed dual 3-input 3-output NOR gate
10212	High-speed dual 3-input 3-output OR/NOR gate
10216	High-speed triple line receiver
10231	High-speed dual type-D master/slave flip-flop
10415	1K x 1 RAM
10804	4-bit ECL/TTL inverting bidirectional transceiver with latch
10805	5-bit ECL/TTL inverting bidirectional transceiver with latch

Application Notes

10115 Quad Line Receiver

The three body versions of the 10115 quad line receiver can be used in three different ways:

- As a differential line receiver (Version 1)
- As a non–inverting translator (Version 2)
- As an inverting translator (Version 3)

When the part is used as an inverting/non–inverting translator, one of the input pins must be tied to the bias pin (pin 'V'). If the part has the SIZE property, the user must place a REPLICATE body between the 'V' pin and the input pin since the 'V' pin is a scalar pin and the input pin is a vectored pin. There is a restriction in the current implementation of the model in that the user cannot put a SIZE greater than 4B to the part (there are four sections in a package); otherwise the Packager will not be able to package the part correctly.

Body version 2 is used as a non–inverting translator. The 'V' pin is connected to pin 'B<SIZE–1..0>*' (the pin directly opposite the 'V' pin) through a REPLICATE body. No REPLICATE body is needed for SIZE=1B.

Body version 3 is used as an inverting translator. The 'V' pin is connected to the input of a REPLICATE body (for SIZE > 1B) and the output of the REPLICATE body is connected to pin 'A<SIZE–1..0>' of the part (the pin directly opposite the 'V' pin). No REPLICATE body is needed for SIZE=1B.

10116 Triple Line Receiver

The 10116 triple line receiver has the same considerations as the 10115 quad line receiver except that the maximum size is 3B (SIZE=3B).

10125 Quad MECL-to-MTTL Translator

The 10125 quad MECL-to-MTTL translator has the same considerations as the 10115 quad line receiver.

10216 High-Speed Triple Line Receiver

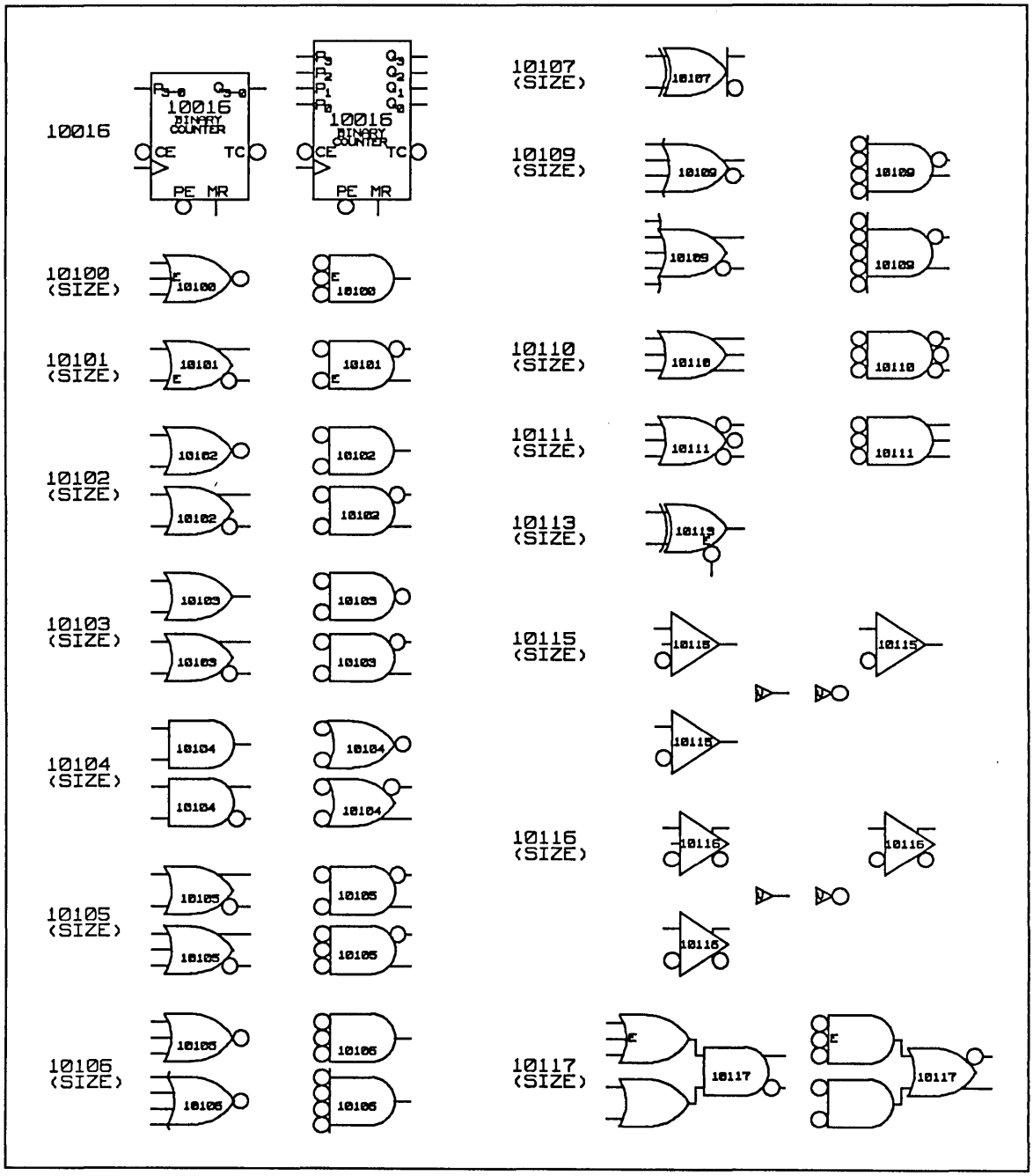
The 10216 high-speed triple line receiver has the same considerations as the 10115 quad line receiver except that the maximum size is 3B (SIZE=3B).

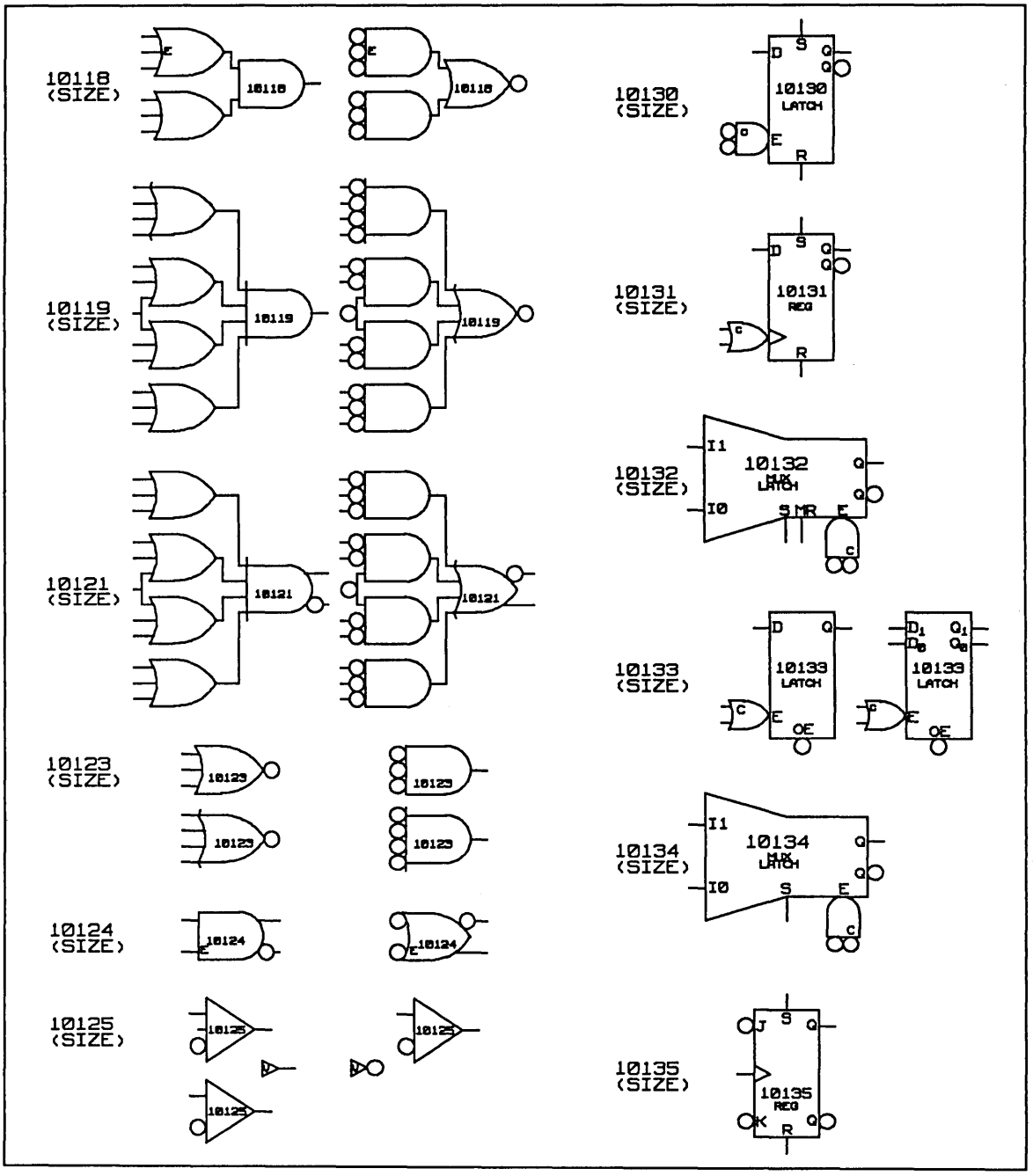
Receiver/Translator Modifications

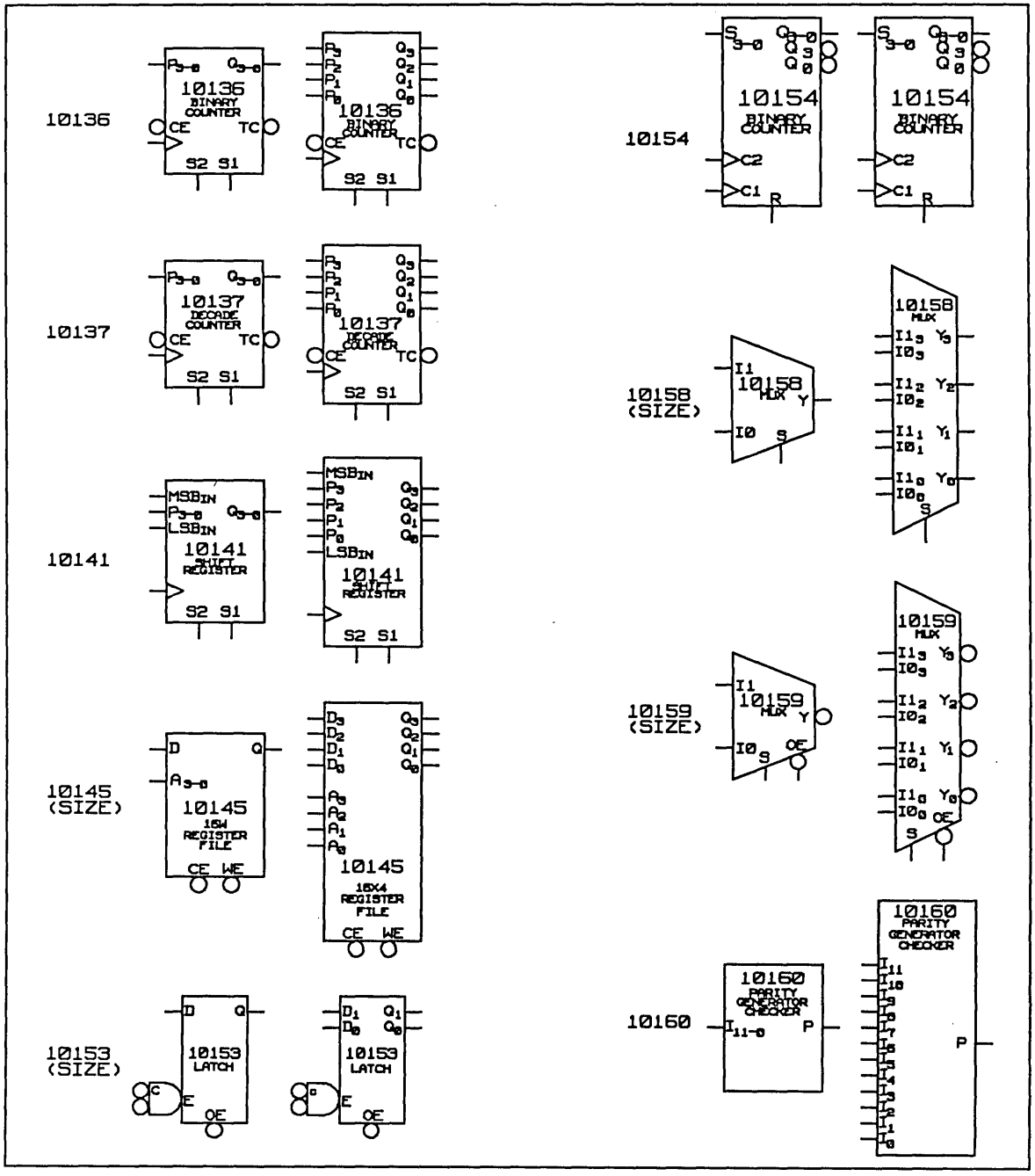
The following parts have been modified to allow proper packaging:

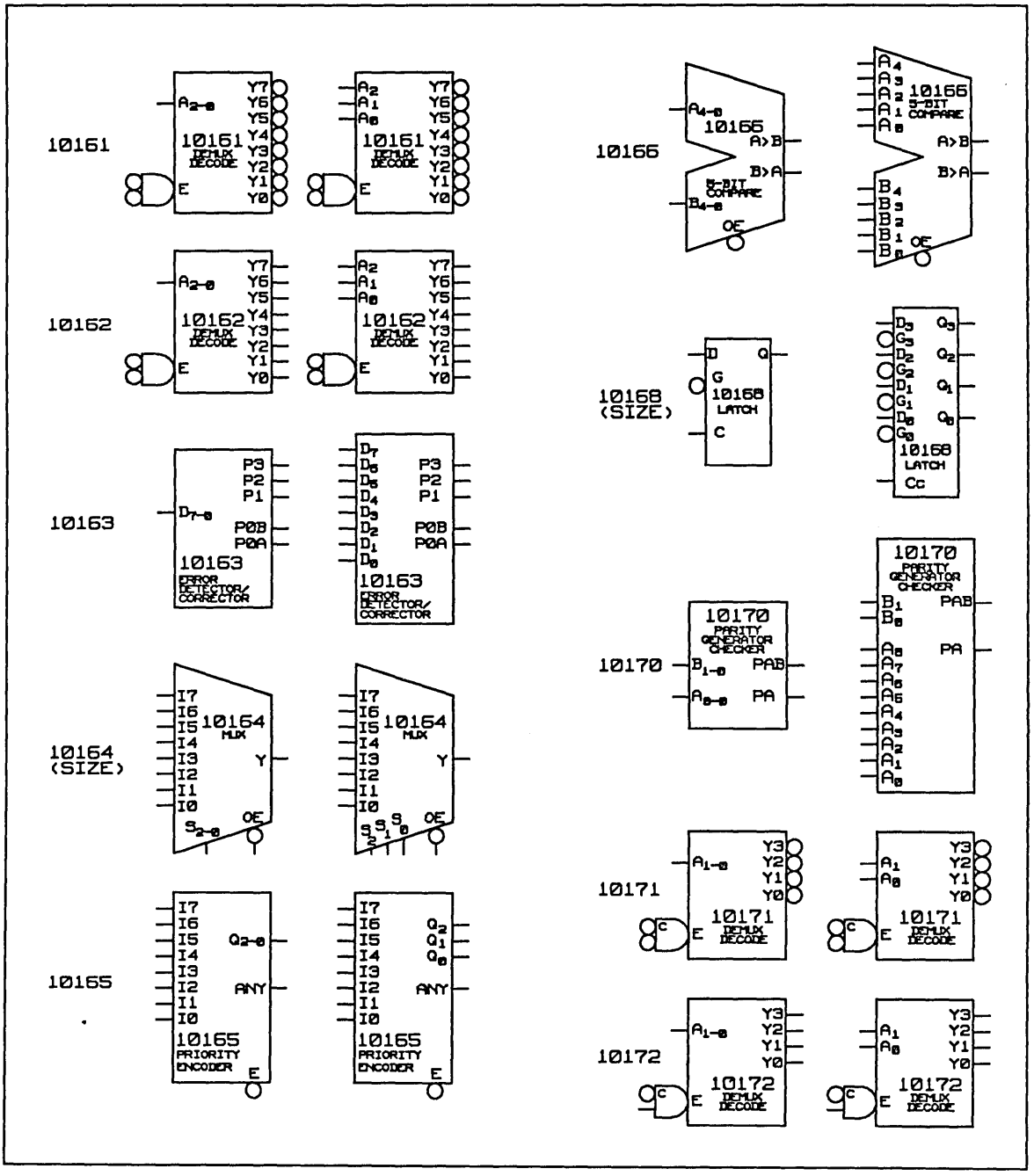
10115 Quad line receiver
10116 Triple line receiver
10125 Quad MECL-to-MTTL translator
10216 High-speed triple line receiver

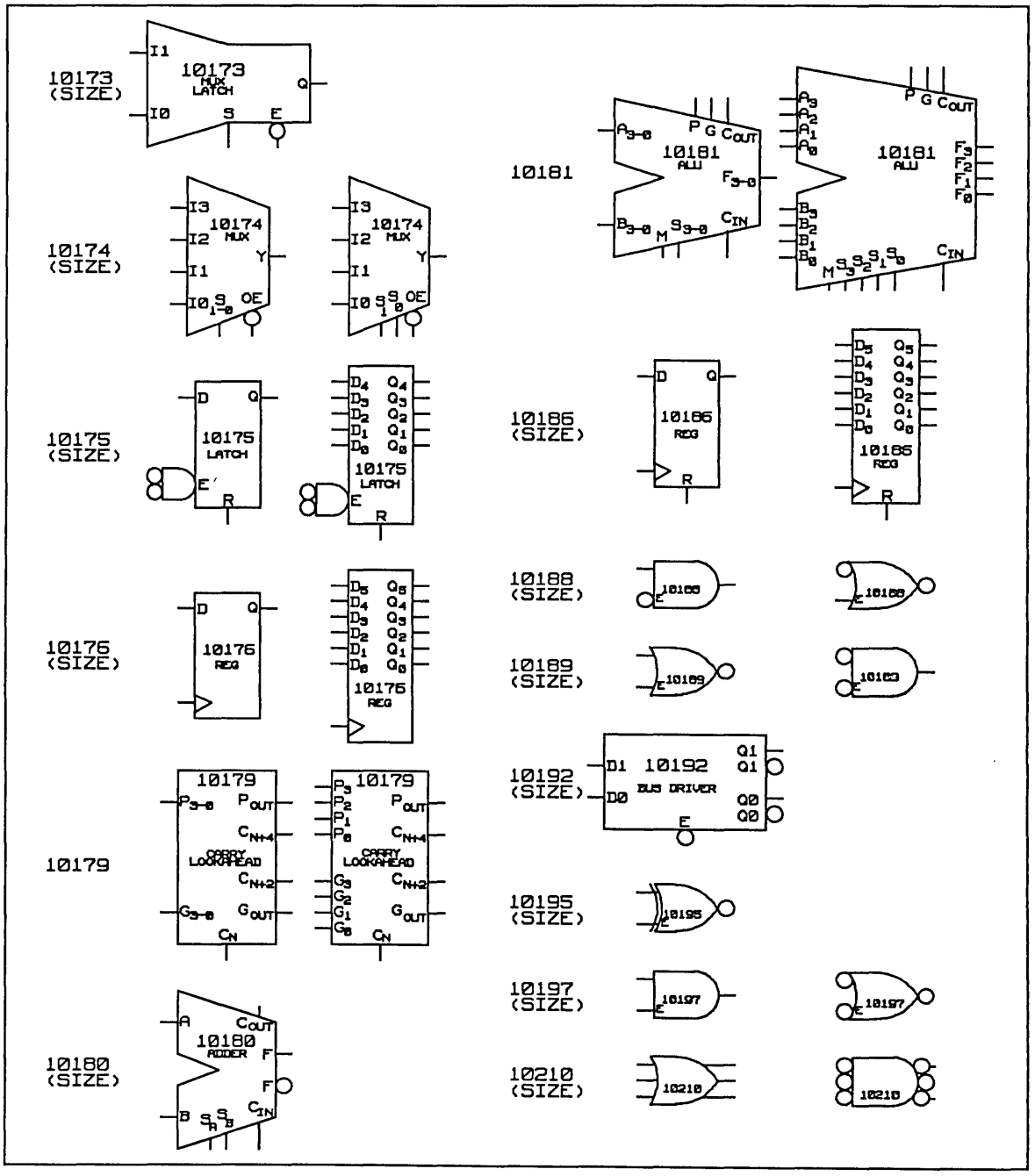
The bias pin (pin V) of body version 1 of the above components has been changed from an invisible pin to a visible, off-grid pin centered between the two input pins. When individual sections of one of these components are to be included in the same package, the bias pins from each section must be wired together (using the blue button).

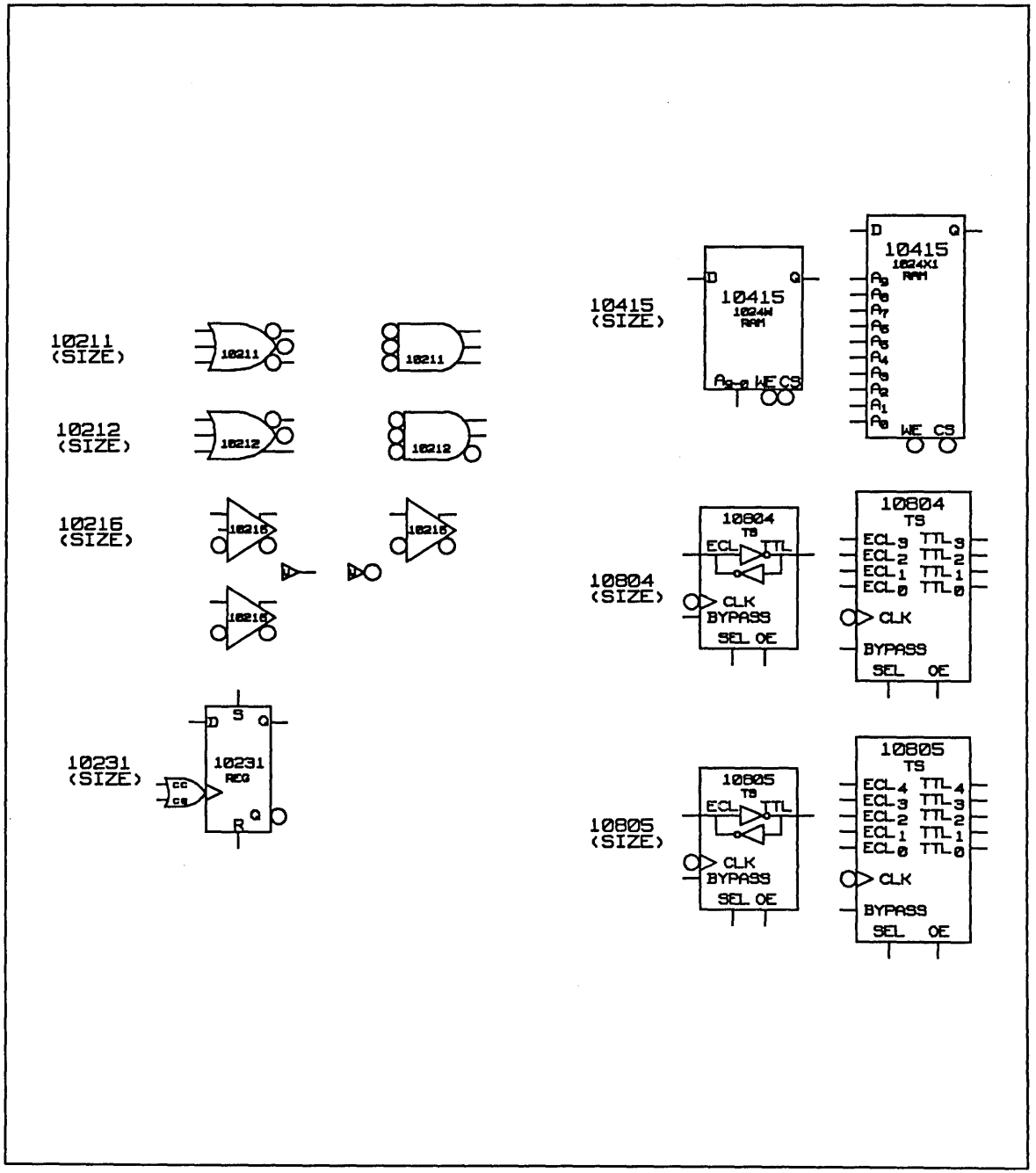

10016
10016
BINARY COUNTER
CE
TC
PE MR
10100 (SIZE)
10101 (SIZE)
10102 (SIZE)
10103 (SIZE)
10104 (SIZE)
10105 (SIZE)
10106 (SIZE)
10107 (SIZE)
10109 (SIZE)
10110 (SIZE)
10111 (SIZE)
10113 (SIZE)
10115 (SIZE)
10116 (SIZE)
10117 (SIZE)

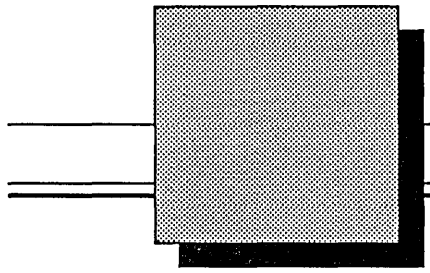

10118
(SIZE)
10118
10118
10119
(SIZE)
10119
10119
10121
(SIZE)
10121
10121
10123
(SIZE)
10123
10123
10123
10123
10124
(SIZE)
10124
10124
10125
(SIZE)
10125
10125
10125
10130
(SIZE)
10130
LATCH
D
S
Q
G
E
R
10131
(SIZE)
10131
REG
10132
(SIZE)
10132
LATCH
I1
I0
S
R
E
C
10133
(SIZE)
10133
LATCH
D
Q
C
E
OE
10134
(SIZE)
10134
LATCH
I1
I0
S
E
10135
(SIZE)
10135
REG
J
K


10136
10136
BINARY COUNTER
CE
TC
S2 S1
10137
10137
DECADE COUNTER
10141
10141
SHIFT REGISTER
MSBIN
LSBIN
10145
(SIZE)
10145
16W REGISTER FILE
CE WE
10145
16X4 REGISTER FILE
10153
(SIZE)
10153
LATCH
10154
10154
BINARY COUNTER
C2
C1
R
10158
(SIZE)
10158
MUX
10159
(SIZE)
10159
MUX
10160
10160
PARITY GENERATOR CHECKER


10161
10161
DEMUX DECODE
10162
10162
DEMUX DECODE
10163
10163
ERROR DETECTOR/ CORRECTOR
10164 (SIZE)
10164
MUX
10165
10165
PRIORITY ENCODER
10166
10165
5-BIT COMPARE
10166
5-BIT COMPARE
10168 (SIZE)
10168
LATCH
10170
10170
PARITY GENERATOR CHECKER
10171
10171
DEMUX DECODE
10172
10172
DEMUX DECODE


10173 (SIZE)
10173
MUX LATCH
I1
I0
S
E
Q
10174 (SIZE)
10174
MUX
I3
I2
I1
I0
Y
OE
10175 (SIZE)
10175
LATCH
D
Q
E
R
10176 (SIZE)
10176
REG
10179
10179
CARRY LOOKAHEAD
10180 (SIZE)
10180
ADDER
10181
10181
ALU
10186 (SIZE)
10186
REG
10188 (SIZE)
10189 (SIZE)
10192 (SIZE)
10192
BUS DRIVER
10195 (SIZE)
10197 (SIZE)
10210 (SIZE)


10211
(SIZE)
10211
10211
10212
(SIZE)
10212
10212
10216
(SIZE)
10216
10216
10216
10231
(SIZE)
D
S
Q
10231
REG
CC
CS
R
Q
10415
(SIZE)
D
Q
10415
1024W
RAM
WE
CS
D
Q
10415
1024X1
RAM
WE
CS
10804
(SIZE)
10804
TS
ECL
TTL
CLK
BYPASS
SEL
OE
10804
TS
CLK
BYPASS
SEL
OE
10805
(SIZE)
10805
TS
ECL
TTL
CLK
BYPASS
SEL
OE
10805
TS
CLK
BYPASS
SEL
OE



The 10KH and ANSI 10KH Libraries

The ECL 10KH Library and ANSI 10KH Libraries both require approximately 464 Kbytes of disk storage.

The specifications used to construct the models in these libraries were taken from the Motorola ECL data books.

The release level of the ECL 10KH and ANSI 10KH Libraries is 9.0.

The libraries contain body drawings and physical, timing, and simulation models for the following 12 components:

10H104	Quad 2-input AND
10H115	Quad line receiver
10H116	Triple line receiver
10H131	Dual D-type master-slave flip-flop
10H158	Quad 2-input multiplexer
10H174	Dual 4-to-1 multiplexer
10H175	Quint latch
10H176	Hex D-type master-slave flip-flop
10H179	Look-ahead carry block
10H180	Dual 2-bit adder/subtractor
10H181	4-bit arithmetic logic unit and function generator
10H186	Hex D-type master-slave flip-flop with reset

Application Notes

10115 Quad Line Receiver

The three body versions of the 10115 quad line receiver can be used in three different ways:

- As a differential line receiver (Version 1)
- As a non-inverting translator (Version 2)
- As an inverting translator (Version 3)

When the part is used as an inverting/non-inverting translator (Version 2 or Version 3), one of the input

pins must be tied to the bias pin (pin 'V'). If the part has the SIZE property, the user must place a REPLICATE body between the 'V' pin and the input pin since the 'V' pin is a scalar pin and the input pin is a vectored pin. There is a restriction in the current implementation of the model in that the user cannot put a SIZE greater than 4B to the part (there are four sections in a package); otherwise the Packager will not be able to package the part correctly.

Body version 2 is used as a non-inverting translator. The 'V' pin is connected to pin 'B<SIZE-1..0>*' (the pin directly opposite the 'V' pin) through a REPLICATE body. No REPLICATE body is needed for SIZE=1B.

Body version 3 is used as an inverting translator. The 'V' pin is connected to the input of a REPLICATE body (for SIZE > 1B) and the output of the REPLICATE body is connected to pin 'A<SIZE-1..0>' of the part (the pin directly opposite the 'V' pin). No REPLICATE body is needed for SIZE=1B.

10116 Triple Line Receiver

The 10116 triple line receiver has the same considerations as the 10115 quad line receiver except that the maximum size is 3B (SIZE=3B).

Receiver/Translator Modifications

The following components have been modified to allow proper packaging:

10115 Quad line receiver
10116 Triple line receiver

The bias pin (pin V) of body version 1 of the above components has been changed from an invisible pin to a visible, off-grid pin centered between the two input pins. When individual sections of one of these components are to be included in the same package, the bias pins from each section must be wired together (using the blue button).

DELAY_EQ Property

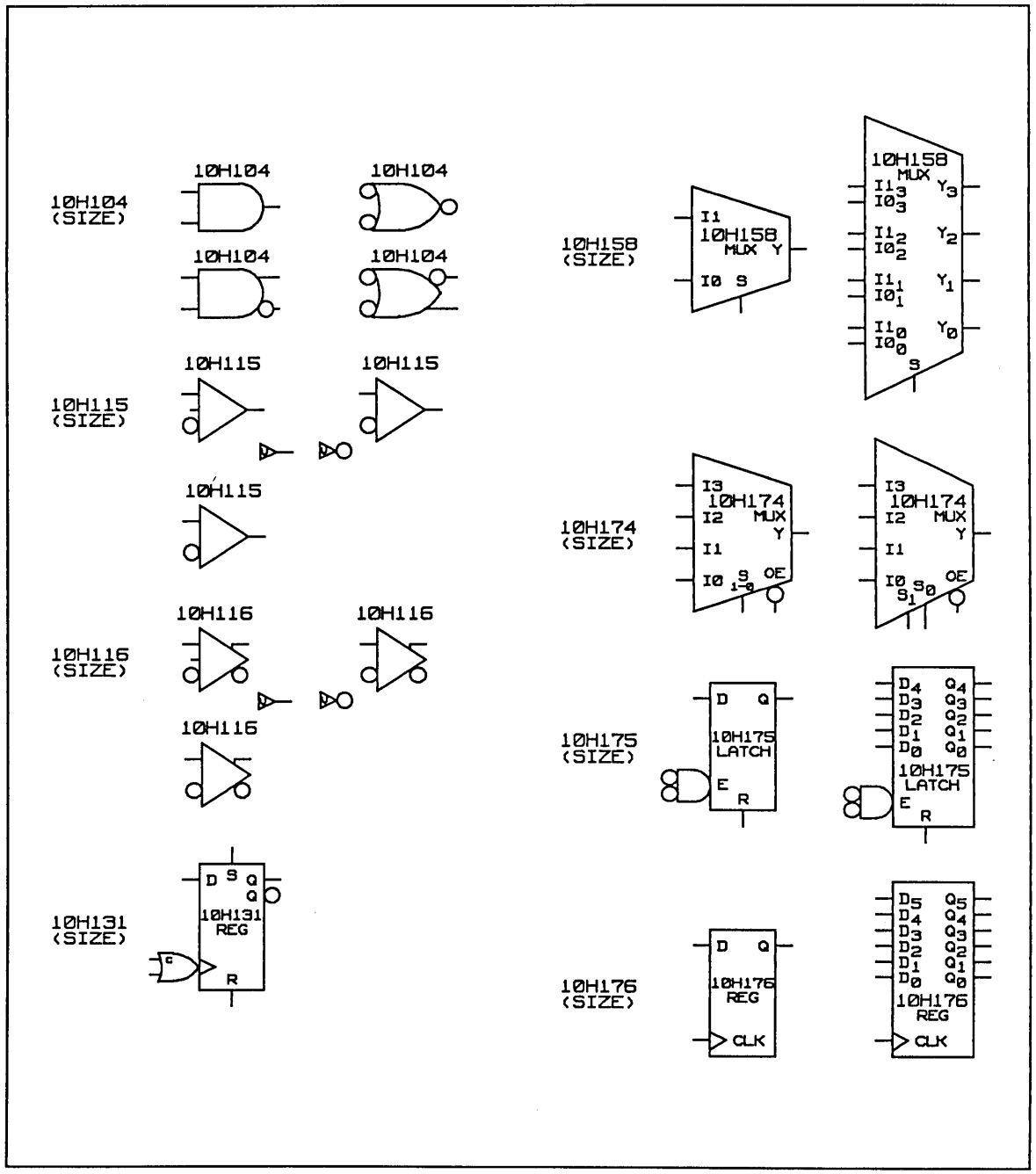
The ANSI 10KH library supports specification of a DELAY_EQ property on the simulation model primitives.

Use the DELAY_EQ property on the model along with the USER_EXPRESSION directive in the *simulate.cmd* file to adjust primitive delay times for various test conditions. By combining the property and the directive, you avoid changing the delay values directly on the SIM models in the library and eliminate the need to recompile the design each time the delay is changed.

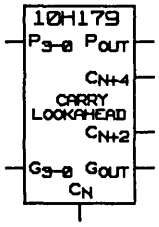
For example, to increase the delay on the simulation models for the library by a factor of two, include the following USER_EXPRESSION in the *simulator.cmd* file:

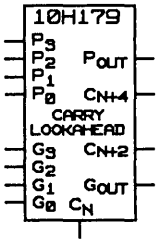
```
user_expression fast, rep='delay*2.0';
```

For additional information on the USER_EXPRESSION directive, refer to the "Expression Evaluator" section of the *ValidSIM Reference Manual*.

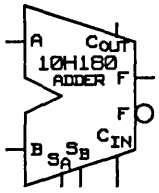

10H104
(SIZE)
10H104
10H104
10H104
10H104
10H115
(SIZE)
10H115
10H115
10H115
10H116
(SIZE)
10H116
10H116
10H116
10H131
(SIZE)
D S Q
Q
10H131
REG
C
R
10H158
(SIZE)
I1
10H158
MUX Y
I0 S
10H158
MUX
I1 3
I0 3
Y3
I1 2
I0 2
Y2
I1 1
I0 1
Y1
I1 0
I0 0
Y0
S
10H174
(SIZE)
I3
10H174
I2 MUX
Y
I1
I0 S1 S0 OE
10H175
(SIZE)
D Q
10H175
LATCH
E
R
D4 Q4
D3 Q3
D2 Q2
D1 Q1
D0 Q0
10H176
(SIZE)
D Q
10H176
REG
CLK
D5 Q5
D4 Q4
D3 Q3
D2 Q2
D1 Q1
D0 Q0

10H179

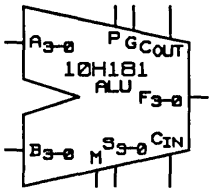


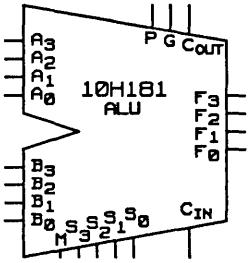


10H180
(SIZE)

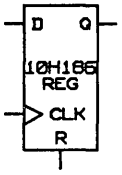


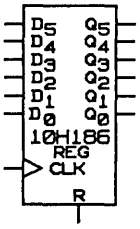
10H181

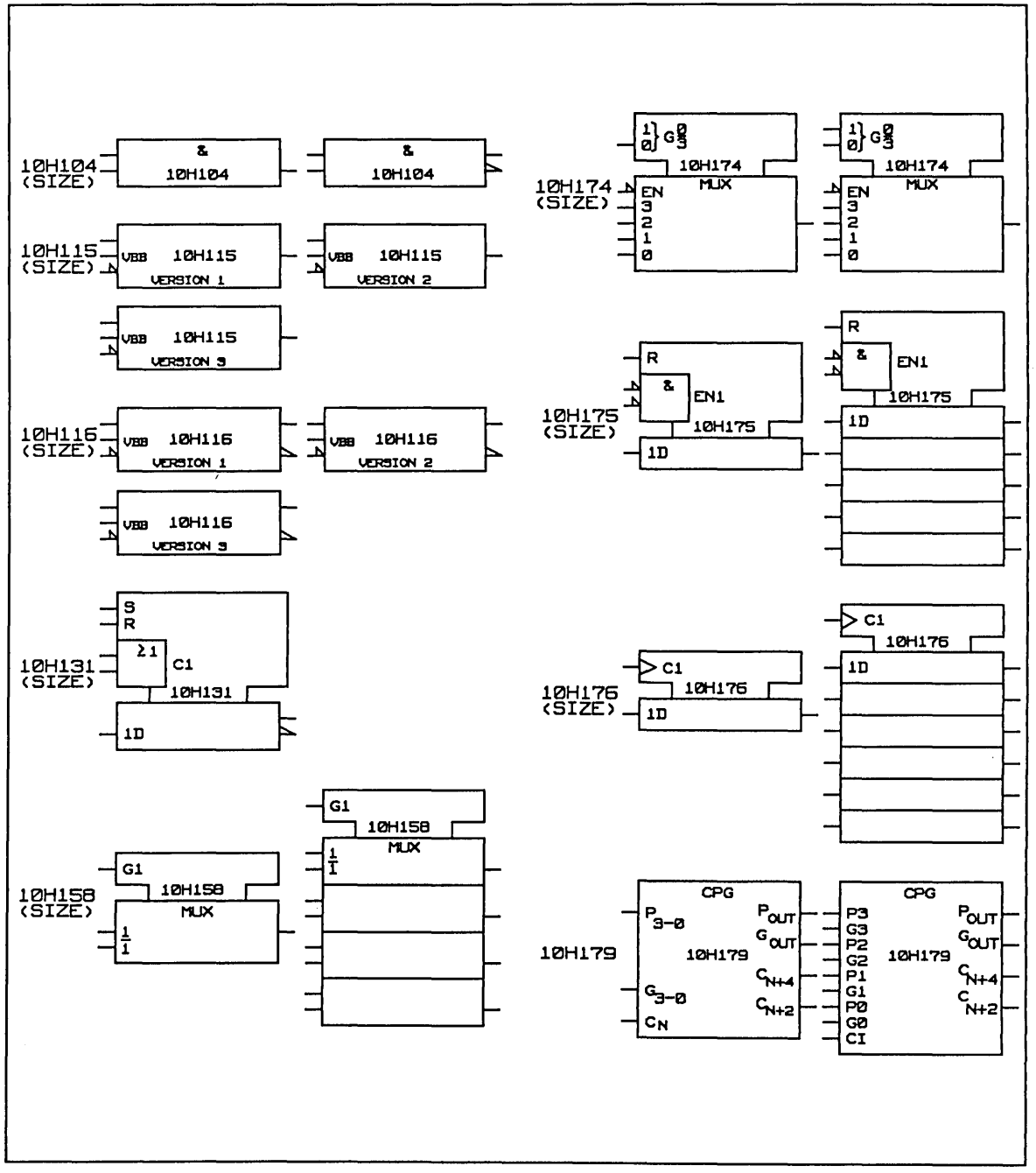


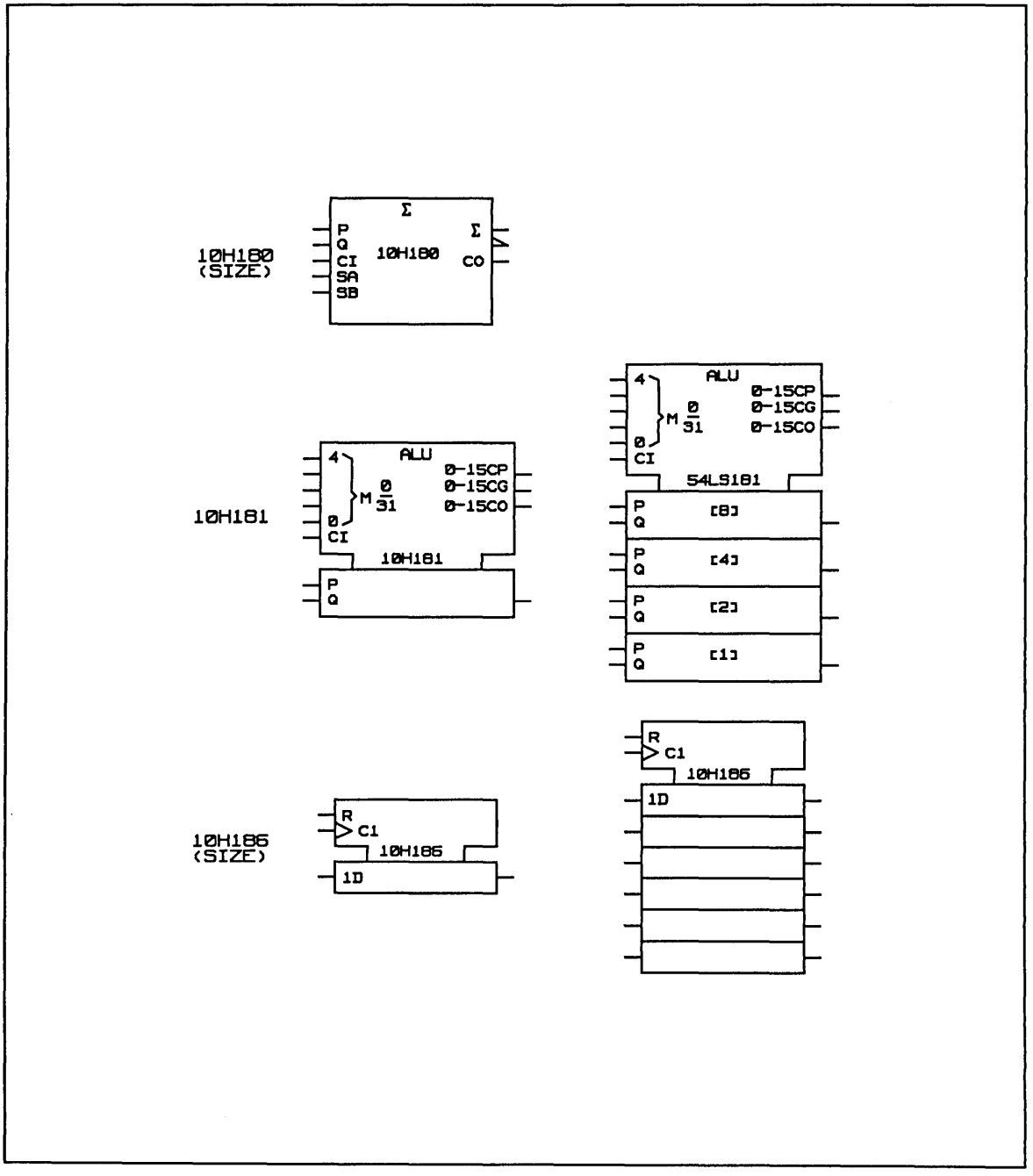


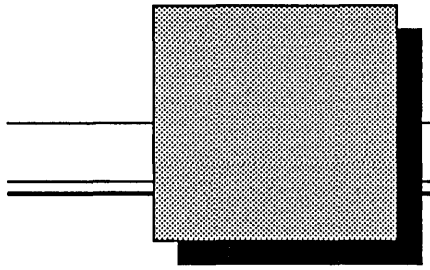
10H186
(SIZE)






10H104 (SIZE)
&
10H104
10H115 (SIZE)
VBB 10H115
VERSION 1
VERSION 2
VERSION 3
10H116 (SIZE)
VBB 10H116
10H131 (SIZE)
S
R
Σ1
C1
10H131
1D
10H158 (SIZE)
G1
10H158
MUX
10H174 (SIZE)
EN
10H174
10H175 (SIZE)
R
EN1
10H175
10H176 (SIZE)
C1
10H176
10H179
CPG
P3-0
G3-0
CN
POUT
GOUT
CN+4
CN+2
P3
G3
P2
G2
P1
G1
P0
G0
CI


10H180
(SIZE)
Σ
P
Q
CI
SA
SB
10H180
Σ
14
CO
10H181
4
M
0
31
0
CI
ALU
0-15CP
0-15CG
0-15CO
10H181
P
Q
54LS181
[8]
[4]
[2]
[1]
10H186
(SIZE)
R
C1
10H186
1D



The 100K Library

The 100K Library requires approximately 1537 Kbytes of disk storage.

The specifications used to construct the models in this library were taken from the Fairchild Data Books.

The release level of the ECL 100K Library is 9.0.

The library contains body drawings and physical, timing, and simulation models for the following 39 components:

100101	Triple 5-input OR/NOR
100102	Quint 2-input OR/NOR with enable
100107	Quint exclusive-OR/NOR
100112	Quad driver with enable
100113	Quad driver
100114	Differential line receiver
100117	Triple 2-wide OR-AND/OR-AND-invert
100118	5-wide 5-4-4-4-2 OR-AND/OR-AND-invert
100122	9-bit buffer
100123	Hex bus driver
100124	Hex TTL-to-ECL translator
100125	Hex ECL-to-TTL translator
100126	9-bit backplane driver
100130	Triple D-type latch
100131	Triple D-type flip-flop
100136	4-stage counter/shift register
100141	8-bit shift register
100142	4 x 4 content addressable memory
100145	16 x 4 read/write register file
100150	Hex D-type latch
100151	Hex D-type flip-flop
100155	Quad multiplexer/latch
100156	Mask-merge
100158	8-bit shift matrix
100160	Dual parity generator/checker

100163	Dual 8-input multiplexer
100164	16-input multiplexer
100165	Universal priority encoder
100166	9-bit comparator
100170	Universal demultiplexer/decoder
100171	Triple 4-input multiplexer with enable
100179	Carry look-ahead
100180	Fast 6-bit adder
100181	4-bit binary/BCD ALU
100182	9-bit Wallace tree adder
100183	2 x 8-bit recode multiplier
100255	ECL 100K-to-TTL converter
100422	256 x 4-bit static random access memory
100474	1024 x 4-bit static random access memory

Application Notes

100114 Hex TTL-to-ECL Translator

The three body versions of the 10114 hex TTL-to-ECL translator can be used in three ways:

- As a differential line receiver (Version 1)
- As a non-inverting translator (Version 2)
- As an inverting translator (Version 3)

When the part is used as an inverting/non-inverting translator (Version 2 or Version 3), one of the input pins must be tied to the bias pin (pin 'V'). If the part has the SIZE property, the user must place a REPLICATE body between the 'V' pin and the input pin since the 'V' pin is a scalar pin and the input pin is a vectored pin. There is a restriction in the current implementation of the model in that the user cannot put a SIZE greater than 5B to the part (there are five sections in a package); otherwise the Packager will not be able to package the part correctly.

Body version 2 is used as a non-inverting translator. The 'V' pin is connected to pin 'B<SIZE-1..0>*' (the pin directly opposite the 'V' pin) through a REPLICATE body. No REPLICATE body is needed for SIZE=1B.

Body version 3 is used as an inverting translator. The 'V' pin is connected to the input of a REPLICATE body (for SIZE > 1B) and the output of the REPLICATE body is connected to pin 'A<SIZE-1..0>' of the part (the pin directly opposite the 'V' pin). No REPLICATE body is needed for SIZE=1B.

100125 – Hex ECL–to–TTL Translator

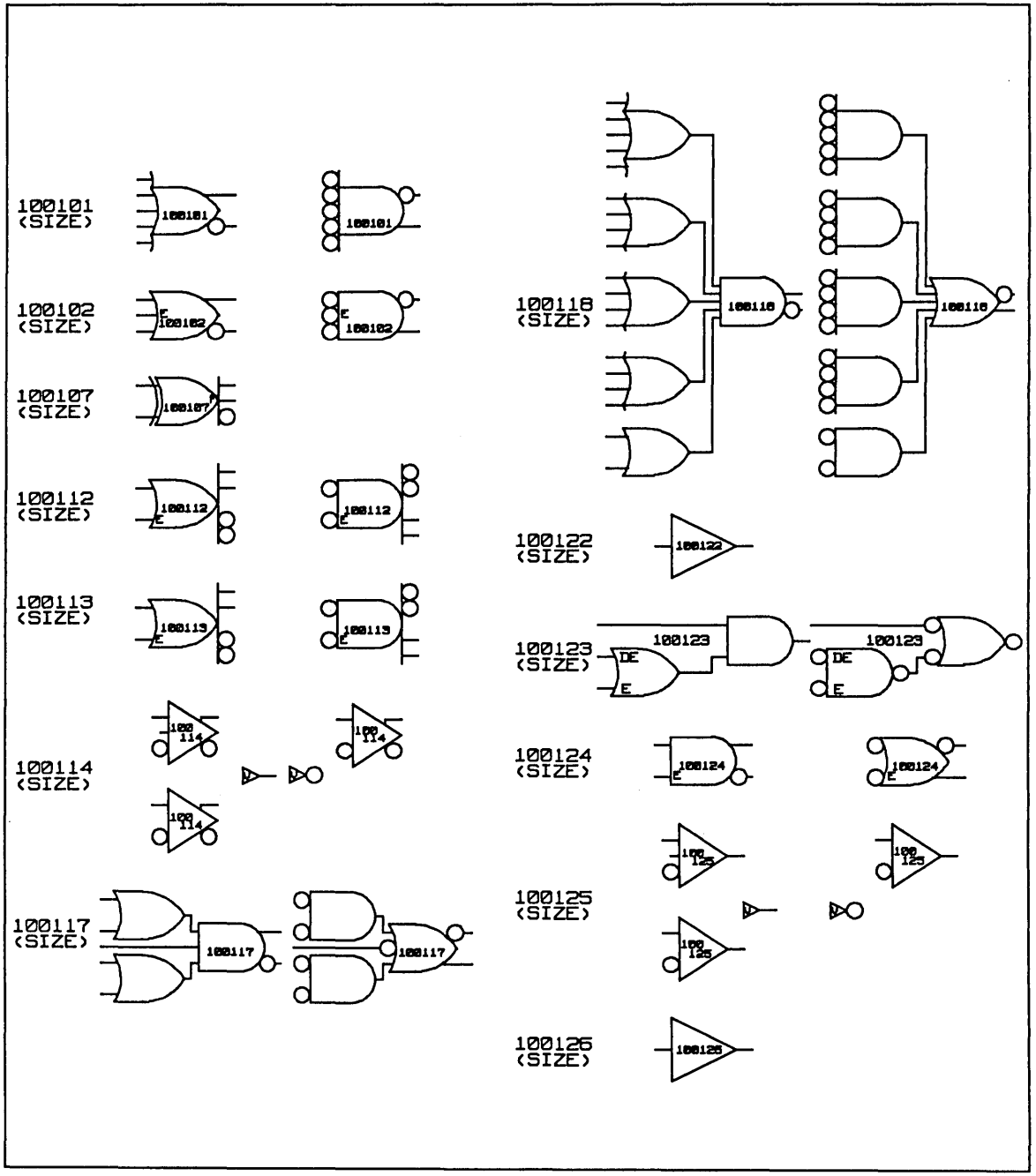
The 100125 hex ECL–to–TTL translator has the same considerations as the 100114 except that the maximum size is 6B.

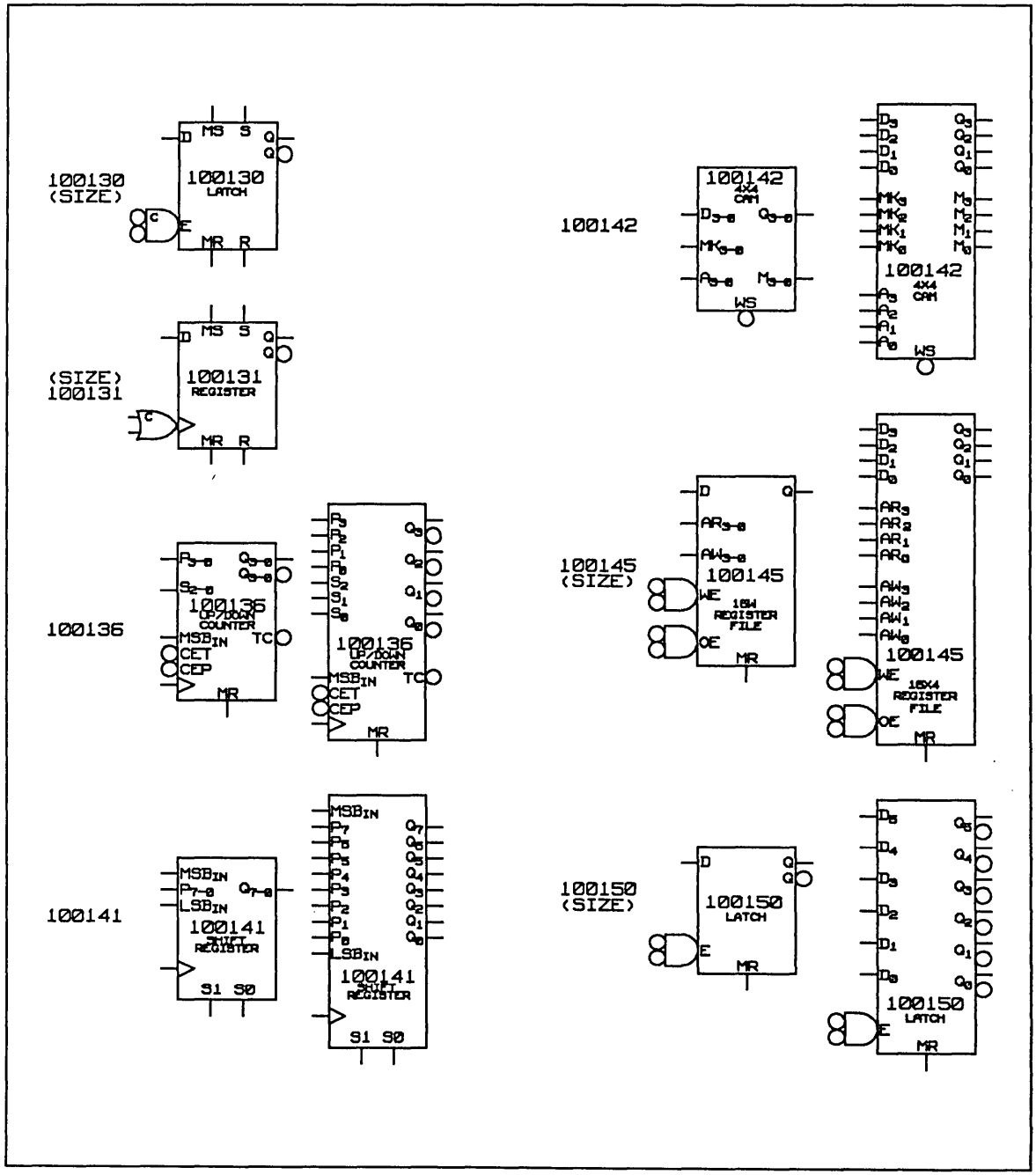
Receiver/Translator Modifications

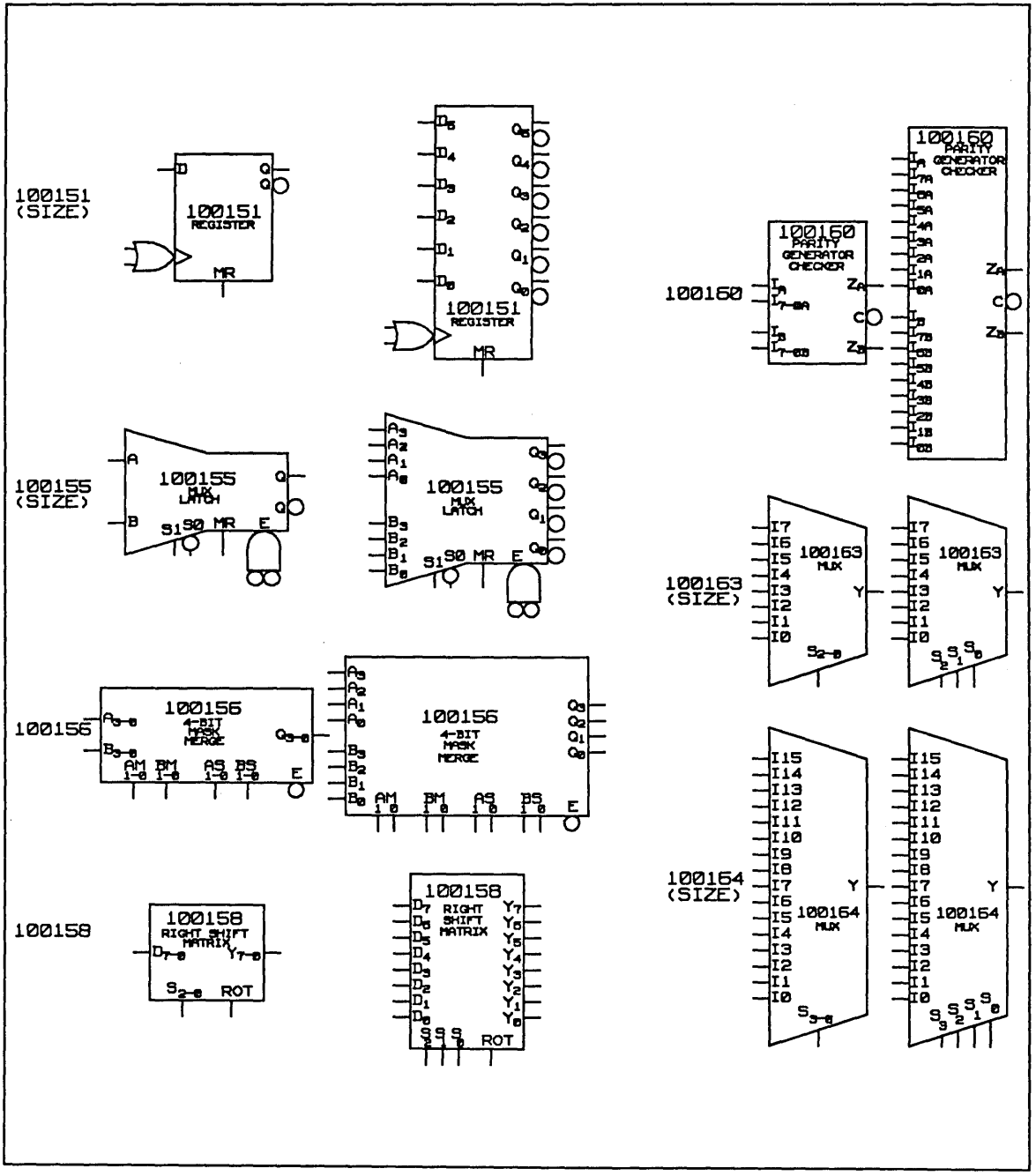
The following components have been modified to allow proper packaging:

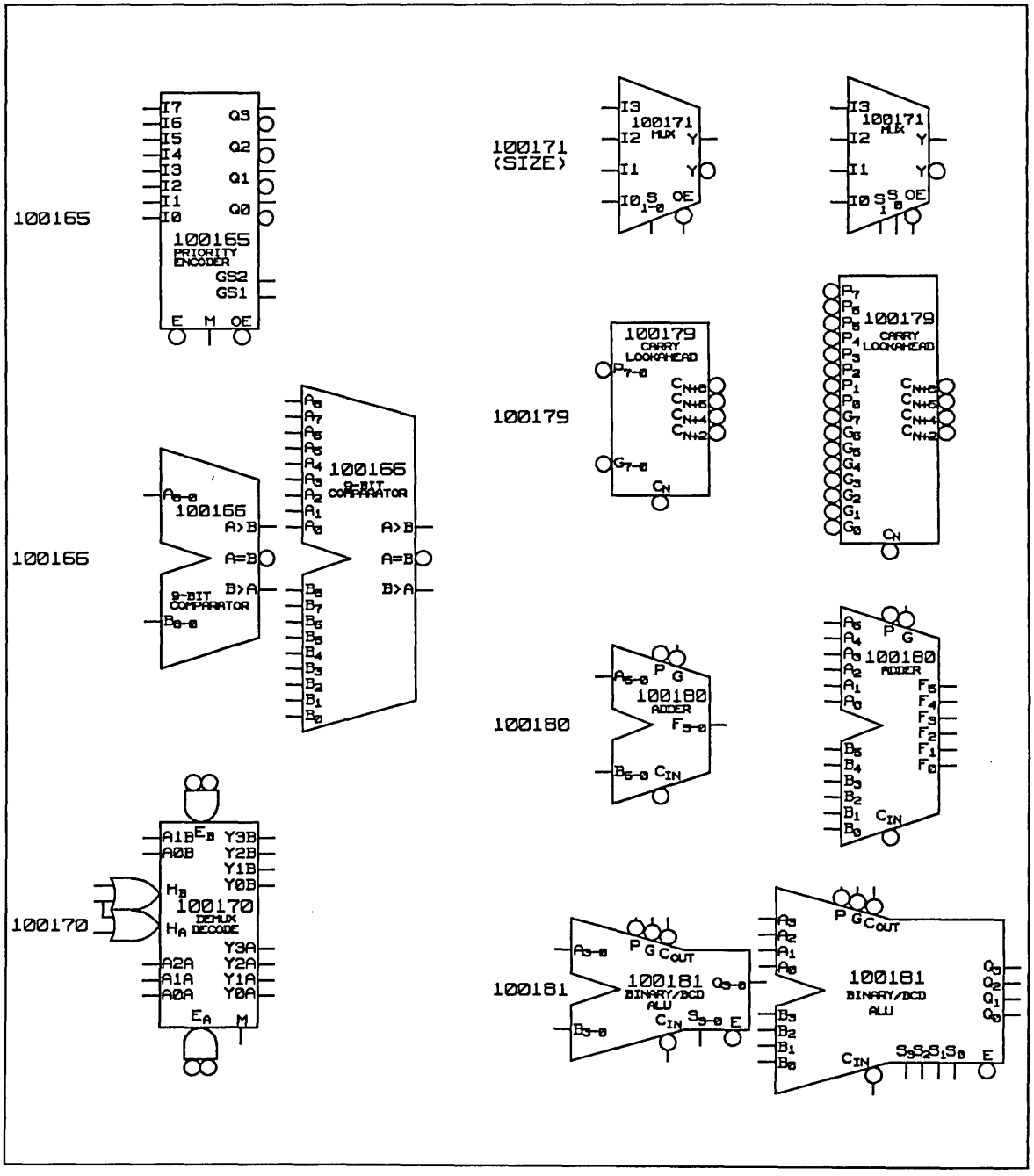
100114 Hex TTL–to–ECL Translator
100125 Hex ECL–toTTL Translator

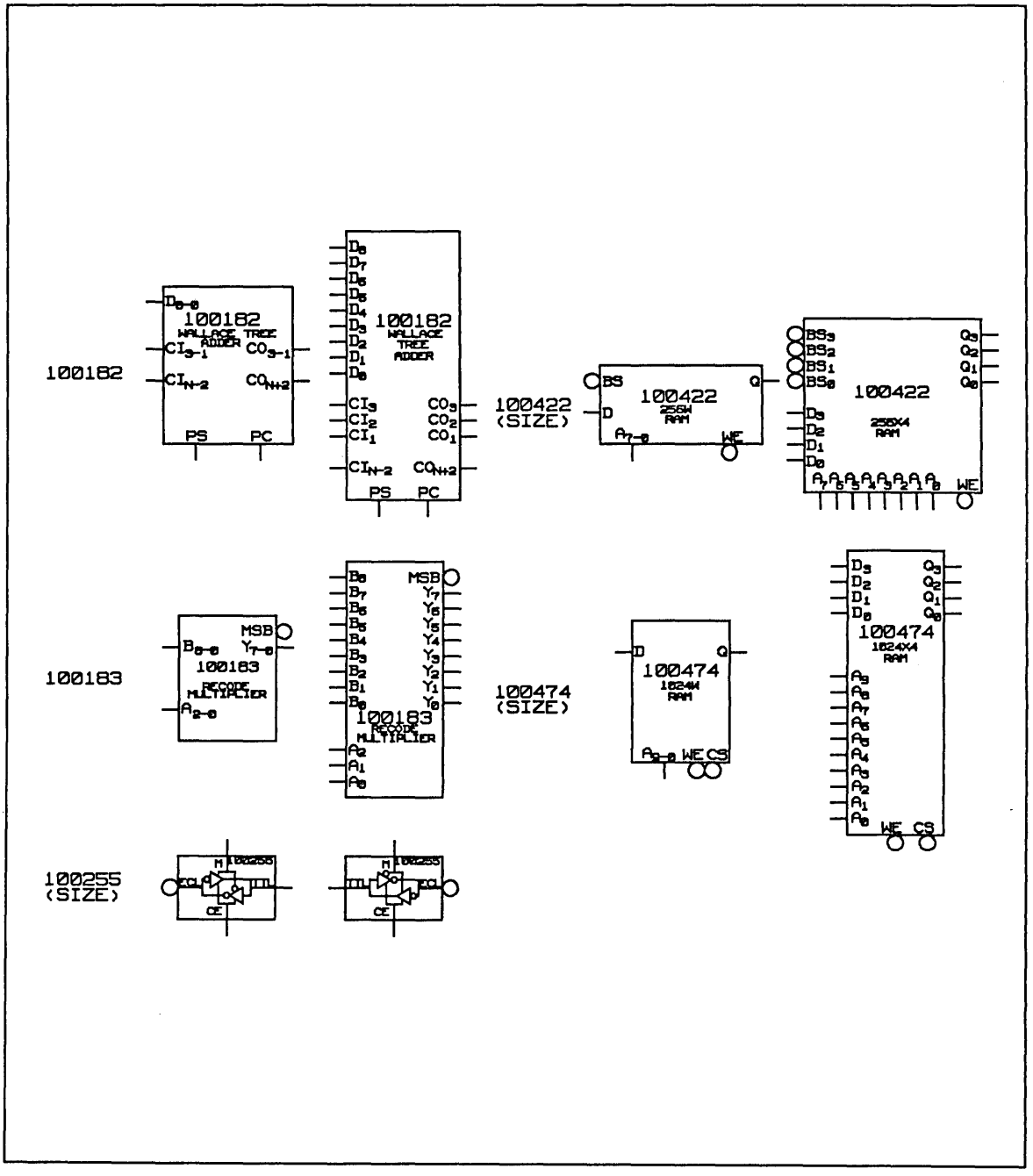
The bias pin (pin V) of body version 1 of the above components has been changed from an invisible pin to a visible, off–grid pin centered between the two input pins. When individual sections of one of these components are to be included in the same package, the bias pins from each section must be wired together (using the blue button).

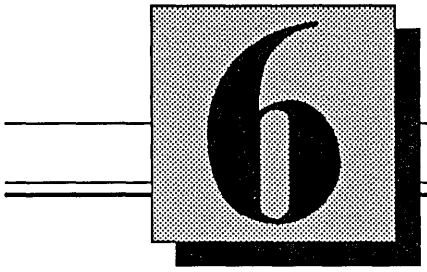

100101
(SIZE)
100102
(SIZE)
100107
(SIZE)
100112
(SIZE)
100113
(SIZE)
100114
(SIZE)
100117
(SIZE)
100118
(SIZE)
100122
(SIZE)
100123
(SIZE)
100124
(SIZE)
100125
(SIZE)
100126
(SIZE)


100130
(SIZE)
100130
LATCH
MS S
D Q
E
MR R
(SIZE)
100131
100131
REGISTER
MS S
D Q
MR R
100136
100136
UP/DOWN
COUNTER
MSBIN
CET
CEP
TC
MR
100141
100141
SHIFT
REGISTER
MSBIN
LSBIN
S1 S0
100142
100142
4X4
CAM
WS
100145
(SIZE)
100145
16W
REGISTER
FILE
WE
OE
MR
100150
(SIZE)
100150
LATCH


100151
(SIZE)
100151
REGISTER
MR
100155
(SIZE)
100155
MUX
LATCH
100156
4-BIT
MASK
MERGE
100158
RIGHT SHIFT
MATRIX
ROT
100160
PARITY
GENERATOR
CHECKER
100163
(SIZE)
MUX
100164
(SIZE)


100165
100165
PRIORITY ENCODER
I7
I6
I5
I4
I3
I2
I1
I0
Q3
Q2
Q1
Q0
GS2
GS1
E
M
OE
100166
8-BIT COMPARATOR
A>B
A=B
B>A
100170
DEMUX DECODE
100171
(SIZE)
100171
MUX
100179
CARRY LOOKAHEAD
100180
ADDER
100181
BINARY/BCD ALU

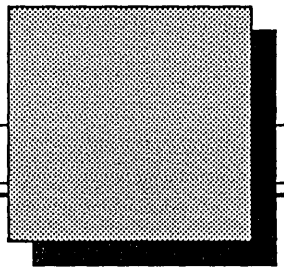

100182
100182
100422
(SIZE)
100183
100183
100474
(SIZE)
100255
(SIZE)



The LOGIC ARRAY Libraries

This section describes the individual libraries that make up the LOGIC ARRAY libraries.

Contents



Programmable Logic Devices User's Guide

This document details a technique for modeling Programmable Logic Devices (PLDs), including PAL, PROM, FPGA, FPLA, and FPLS devices. The technique provides a convenient and compact way of describing accurate gate–level models where precise simulation and timing analysis is required.

The technique modifies blank, or unprogrammed, base models for a particular PLD made up of standard SCALD primitives. A JEDEC format file is used to modify the device's database and to customize, or program, the part.

The release level of the Programmable Logic Devices User's Guide is 9.1.

Modeling Programmable Logic Devices

The major difference between PLD libraries and standard SCALD libraries is that the PLD library is not referenced during a Graphics Editor session. Rather, a device in the PLD library represents a "base" model that is brought into your account and customized, similar to the treatment of a physical device. Several programs and scripts are provided to develop a PLD model.

The basic PLD modeling scheme is that models are defined in two parts, or *pages*. One page represents the base, or logical, model of the PLD and is constructed using standard SCALD primitives (with the SIZE property) to reproduce the internal gate array structure of the PLD. This section of the model accurately represents a blank, unprogrammed device.

The other page represents reserved space for a connectivity file made up of the actual programmable AND/OR arrays. This file, when added to the base model, completes the programming for the device. A data conversion routine is provided to create this file from a JEDEC format file specification.

Implementing Programmable Logic Devices

A Pascal-based program, *genpld*, is provided to generate the programmable logic of the device. The function of this program is to provide a device-independent logic array generator complemented by a base model that provides buffers and registers to interface to the outside world. The base model is also used to attach the timing information. *Genpld* produces the second page of the model in GED connectivity file format.

Two major files are required by the *genpld* program:

Fusemap file

This file is in standard JEDEC format to provide the program with the necessary information about blown and intact fuses. This file is obtained by an independent front end running on either the workstation or some other host. Currently, three tools are supported on the SCALD system (ABEL, CUPL, and PALASM) to produce this JEDEC format file.

PLD description file

This file specifies the size and node names of a particular PLD. This file is used to generate the logic and to connect the base model with the corresponding programmable array. One description file is required for each device model, and additional parts may be added without changing the software. The intent is that Valid supplies all files, although experienced users can model parts themselves. An example of the file format is outlined on page 6-14.

Genpld actually generates AND and OR gates and connects them by building nodes. The logic is optimized for the actual number of terms used and also

makes extensive use of vectors in order to keep the number of primitives and signal names (synonyms) to a minimum. An optional text file that describes non-SCALD primitives may be specified. This feature adds the capability to interface to other simulators. The text file contains various AND and OR gate primitives that describe the formal form of the primitive and the naming of input and output pins. You must change the base model in the library to completely support this feature; the default is to use the SCALD primitives. *Genpld* also reads in the signal name syntax configuration file *(config.dat)* in order to determine the library format.

Genpld accepts the following command-line arguments:

-s *simulator_primitive_filename* (optional argument)

-p *PLD_description_filename* (required argument)

-j *jedec_file* (optional argument)

Genpld is completely embedded in shell scripts and is transparent to the user. These scripts manage the environment, including:

- Moving and deleting files
- Providing a user-friendly interface
- Performing extensive error checking

User Interface

Three shell programs are provided to create and manipulate PLDs:

- *makepld* Make PLD
- *genpld* Blow fuses (program device)
- *rempld* Remove PLD

The program functions are detailed below. A flowchart is provided on page 6–16.

Makepld

The basic function of the *makepld* program is to create a new, unique part in your work area (your account) by copying a part from an existing library. To run this program, type:

```
makepld
```

The program prompts for the following entries:

- *Device name (type) from library* (for example, 16R8, 16L8, etc.).
- *Device name for part in your account* (for example, pal_1, P7035A, decoder2). The program tests to be sure the name you enter is unique. The device name you enter must be compatible with the operating system's file name syntax. No spaces or special characters are permitted.
- *Your working SCALD directory.* The program tests for an existing Valid SCALD directory. The SCALD directory name you enter must be in the current directory.

When this information is correctly entered, *makepld* copies the requested device from the library into your account under the new device name. An entry is made in the specified SCALD directory, and a "chips" entry is made in the file *plds.prt*. *Plds.prt* is a local part file created by *makepld* that contains the chips information for all of your PLDs in your SCALD directory. This file is read by the Packager when schematics containing the PLDs are processed.

The *makepld* program changes the names of drawings in several files to avoid complaints from the Compiler.

The *makepld* program provides a basic body shape for use in drawings, the foundation for simulator and verifier models (unprogrammed), and the basic chips information for a device. You can modify the body shape with respect to shape, size, pin orientation, bubbles, and notes. You should not add or delete pins or change pin names (adding, deleting, and changing pin names is possible; a detailed knowledge of library modeling is required). The body has a default property "label" that is modified to reflect the name of the device. The property value appears as text that may be moved, scaled, or displayed invisibly by the Graphics Editor.

Genpld

The basic function of the *genpld* program is to read a fusemap file in JEDEC format and then to program your PLD. Before running this program, you must create the input JEDEC file by running the PALASM program (PALs only), CUPL, or ABEL (see associated user documentation).

You may also choose to generate a JEDEC file on another host with other tools such as AMAZE (Signetics); the JEDEC file then must be moved to the SCALD system via RS232, tape, or diskette. To run the program, type:

```
genpld
```

The program prompts for the following entries:

- *PLD name* (the name you gave the device)
- *PLD JEDEC file name*

Genpld checks the status of the PLD and reports if the device has been previously programmed. You may overwrite the previous PLD description or quit. The program displays the header from the specified file for your inspection before proceeding.

A data conversion routine reads the JEDEC file and generates a connectivity file that is added to the device model (the program also performs some file cleanup to keep the Compiler from complaining).

Unlike physical PLD devices, these models can be programmed and reprogrammed as required. It is not necessary to make a new PLD or to modify the schematic.

Note: *Genpld* uses several temporary files in the */tmp* directory. Files in this directory with the same names as those used by this program are deleted.

Caution The PALASM program does not accept tabs in the equations file. Check to be sure your screen editor does not insert tabs automatically (the UNIX/ULTRIX *expand* command can be used to remove tabs). Also, when using the equation section, be sure to include the "DESCRIPTION:" keyword at the end of the file.

Rempld

The basic function of the *rempld* program is to remove a PLD from your account. This program removes the subdirectory for the specified PLD, the corresponding SCALD directory entry, and the entry in the *plds.prt* file.

To run this program, type:

```
rempld
```

The program prompts for the following entries:

- *PLD name*
- *Your working SCALD directory*

Before removing the PLD, the program reports the status of the device. At this point, you may choose whether or not to continue the removal process.

Note: A PLD may be removed using the Graphics Editor; its entry, however, remains in *plds.prt* unless the entry is manually deleted from the file. In case the device is subsequently reentered without removing the physical information, the Packager issues Error 201.

Programmable Logic Devices and Scald Software

Graphics Editor

PLDs behave in a unique way since they are created outside of the Graphics Editor and are simply "plugged-in" to your SCALD directory.

PLDs behave in a unique way since they are created outside of the Graphics Editor and are simply "plugged-in" to your SCALD directory.

When a PLD is created prior to starting a session of the Graphics Editor, the PLD device appears in your directory and is ready for immediate use. If a Graphics Editor session is currently running when a PLD is made, the PLD does not automatically appear in your directory. Accordingly, the Graphics Editor must reread the working directory before the PLD can be used. The recommended procedure is to use the **ignore** and **use** directory commands from within the Graphics Editor; note that any bodies created in the working directory disappear from the current schematic with the **ignore** command and then reappear with the **use** command. Alternately, you can exit the current Graphics Editor session and restart the editor.

The output pins of devices that have programmable output pins are individually bubbleable. You should section the part in order to map the logical names to the physical pins.

Compiler

A special SCALD directory has been created in the library for "primitives" used in the modeling of PLDs. This directory *(pld.sdir)* is used only for device modeling purposes and should not be referenced by the user in the Compiler directives file. The name of the PLD library or libraries used must be referenced with the LIBRARY directive (for example, LIBRARY NEWPAL24;) and should be included in the master library file. All information required to compile locally is in your account. When compiling for logic (to package a PLD design), it is not necessary to first run *genpld*; when compiling for sim or time, *genpld* must run to "program" the PLD before compiling the design.

Simulator

I/O pins that are programmed as inputs must be driven by external gates for simulation purposes. I/O pins functioning as inputs have an internal three-state buffer on the node in a high-impedance state. This state is propagated on the pin and cannot be overridden by the Simulator; only a gate on the schematic can drive this node.

Timing Verifier

The Timing Verifier models are essentially duplicates of their corresponding Simulator models. You should be aware that when these complex models are verified on a schematic, the verifier outputs timing information for signals internal to the model (in addition to all other signals in the design). Although this additional information may be a nuisance, the Timing Verifier results are correct. Devices that have three state outputs must be enabled (for example, in a case file); otherwise high impedance may propagate back via feedback paths and thus result in an unknown state.

Packager

PLD chips files can be modified to accommodate the Packager. The Packager performs checks on nets to determine if any design rules have been violated (for example, outputs tied together of incompatible types; see the *ValidPACKAGER Reference Manual* for details). The chips information is created by the *makepld* program in the *plds.prt* file. This file must be referenced as a library file (with the LIBRARY directive) in the Packager directives file.

PLD Description File Format

```
device_name (* must be in lower case *)
:AND_TERMS
    SIZE_AND {size} (* number of and gates *)
    SIZE_INPUT {size}:{skip}(* input + feedback *)
    INPUT_NAME {signalname}(* input + feedback in fuseaddress order *)
    FUSE_STARTADDRESS {fuseaddresses}(* e.g., 1712 *)
    FIXED (* for proms *)
    OUTPUT_NAME {signalname}
:OR_TERMS
    SIZE_OR {size}
    SIZE_INPUT {size}:{skip}
    INPUT_NAME {signalname}
    FUSE_STARTADDRESS {fuseaddresses}
    FIXED (* for pals *)
    OUTPUT_NAME {signalname}
:CONTROL_TERMS
    SIZE_AND {size}
    SIZE_INPUT {size}:{skip}
    INPUT_NAME {signalname}
    FUSE_STARTADDRESS {fuseaddresses}
    NONE
    OUTPUT_NAME {signalname}
:SPECIAL_FUSES
    RANGE={fuseaddress..fuseaddress}:{skip}:
        {input_signame<bitsubscript> or constant}:
        {output_signame<bitsubscript>}:{floatvalue}:{O or A}
    SINGLE={fuseaddress}:{input_signame<bitsubscript> or constant}:
        {output_signame<bitsubscript>}:{floatvalue}
```

Figure 6-1. PLD Description File Format

Remarks

- All signal names must have a bit subscript.
- All signal names must be in upper case.
- No numeric characters are allowed in a signal name.
- The optional A or O parameter in the RANGE directive causes AND or OR gates to be built.
- All parameters to a directive are separated by colons.

Design Flow

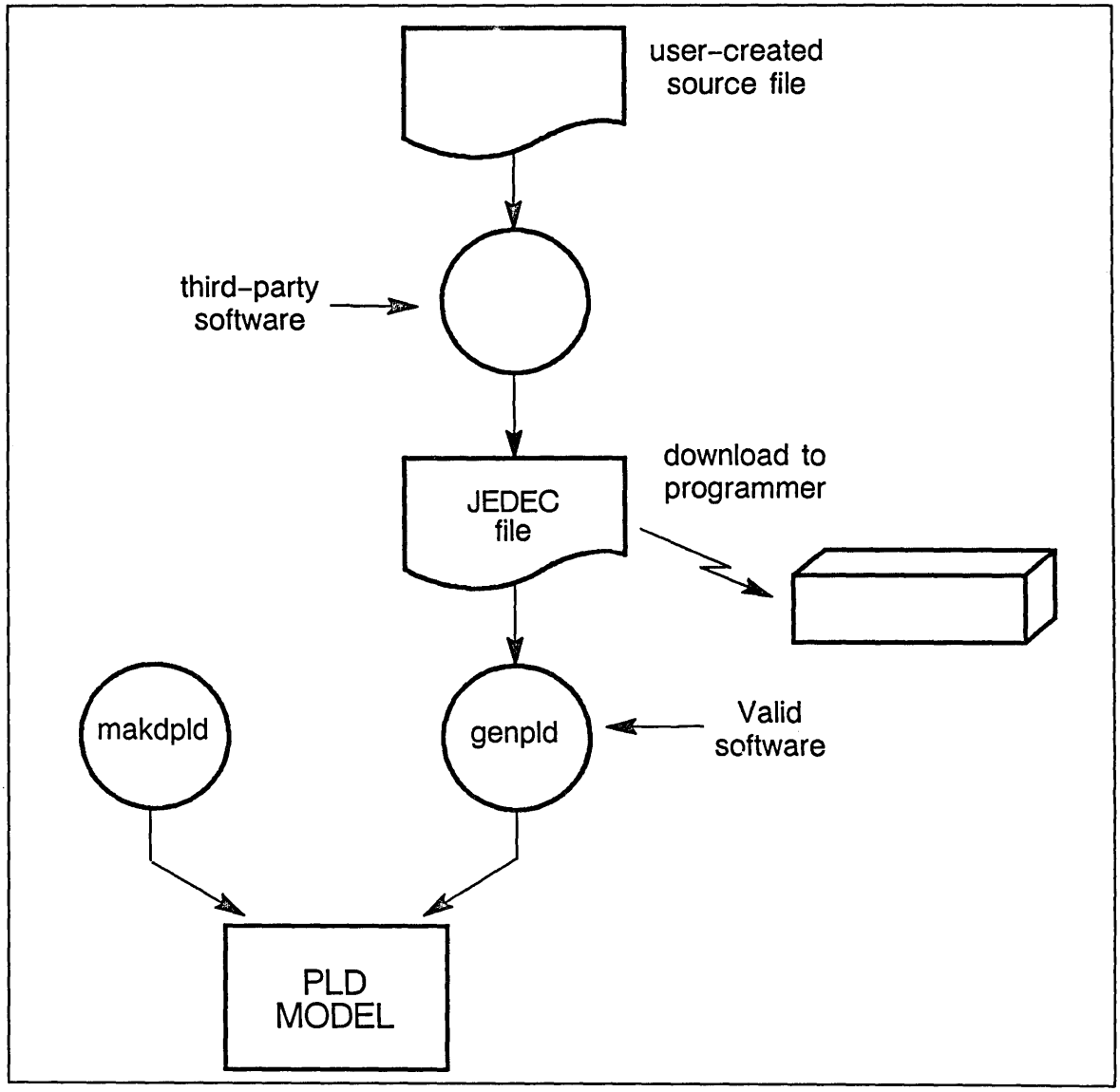
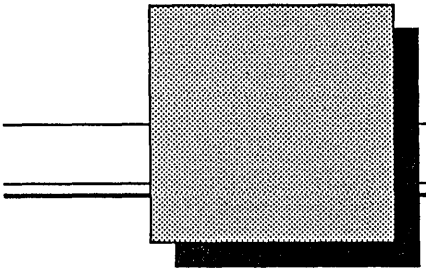


Figure 6-2. PLD Design Flow



The NEWPAL20 Library

The NEWPAL20 Library requires approximately 1703 Kbytes of disk storage.

The specifications used to construct the models in this library were taken from the Monolothic Memories data books.

The release level of the NEWPAL20 Library is 9.3.

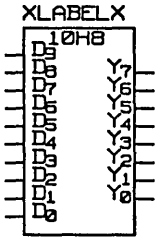
The library contains body drawings and physical, timing, and simulation models for the following 32 components:

10H8	16L8D
10L8	16LD8
10P8	16P2
12H6	16P8
12L6	16R4
12P6	16R4A
14H4	16R4B
14L4	16R4D
14P4	16R6
16C1	16R6B
16H2	16R8
16HD8	16R8A
16L2	16R8B
16L8	16RP4
16L8A	16RP6
16L8B	16RP8

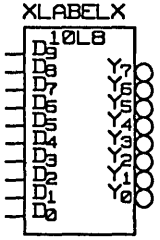
Application Notes

- The NEWPAL20 library requires the *libutil* software package; this package is installed in the */u0/tools* or */usr/valid/tools* directory.
- Please refer to the *Programmable Logic Devices User's Guide* at the front of this section.

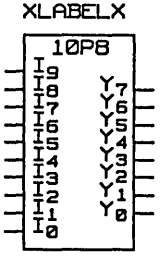
10H8



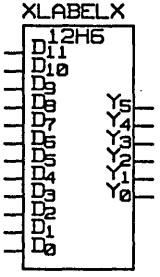
10L8



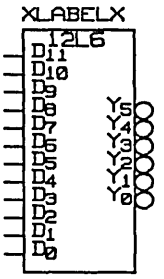
10P8



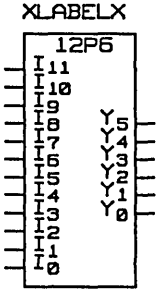
12H6



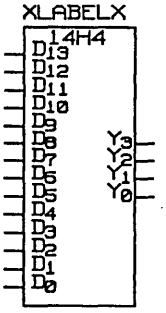
12L6



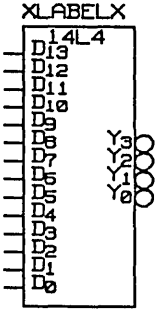
12P6



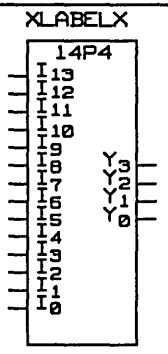
14H4



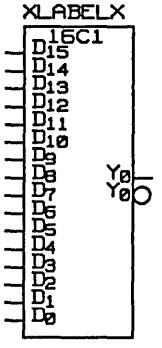
14L4



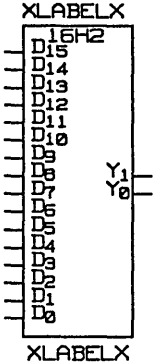
14P4



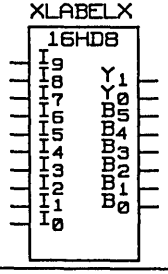
16C1



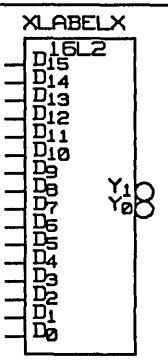
16H2



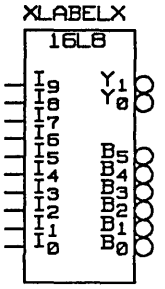
16HD8



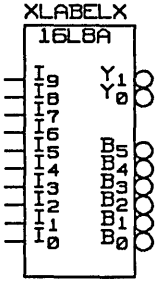
16L2



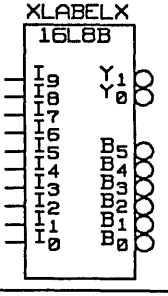
16L8



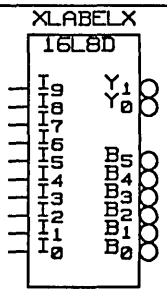
16L8A



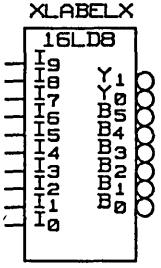
16L8B



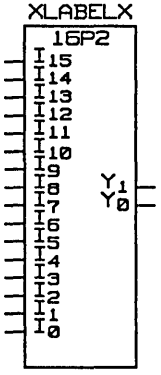
16L8D



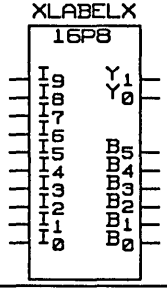
16LD8



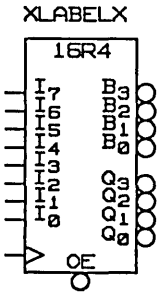
16P2



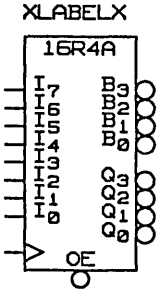
16P8



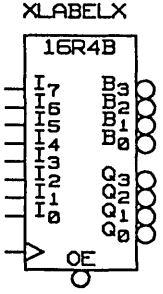
16R4



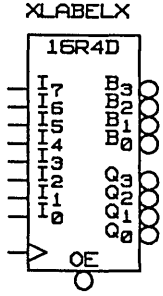
16R4A



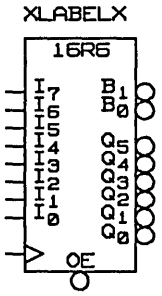
16R4B



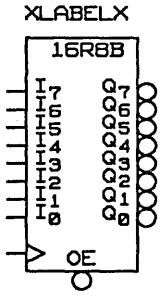
16R4D



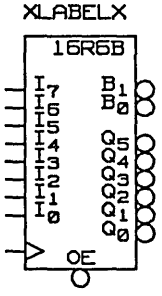
16R6



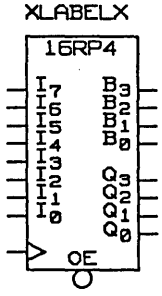
16R8B



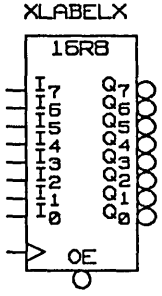
16R6B



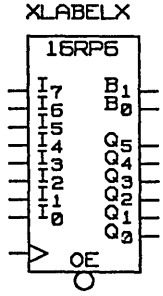
16RP4



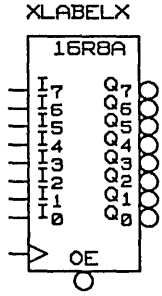
16R8



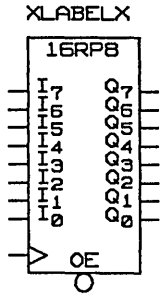
16RP6

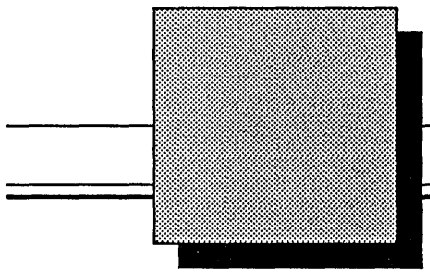


16R8A



16RP8





The NEWPAL24 Library

The NEWPAL24 Library requires approximately 1439 Kbytes of disk storage.

The specifications used to construct the models in this library were taken from the Monolothic Memories data books.

The release level of the NEWPAL24 Library is 9.3.

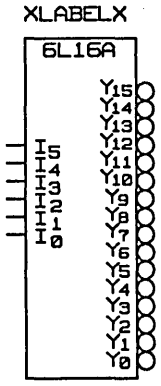
The library contains body drawings and physical, timing, and simulation models for the following 40 components:

6L16A	20L10
8L14A	20L10A
12H10	20L10B
12L10	20P2
12P10	20R4
14H8	20R4A
14L8	20R4B
14P8	20R6
16H6	20R6A
16L6	20R8
16P6	20R8A
18H4	20R8B
18L4	20RS4
18P4	20RS8
20C1	20RS10
20H2	20S10
20L2	20X4
20L8	20X8
20L8A	20X10
20L8B	22P10A

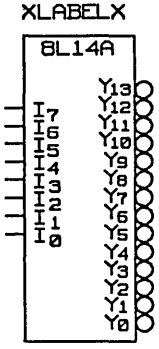
Application Notes

- The NEWPAL24 library requires the *libutil* software package; this package is installed in the */u0/tools* or */usr/valid/tools* directory.
- Please refer to the *Programmable Logic Devices User's Guide* at the front of this section.

6L16A



8L14A



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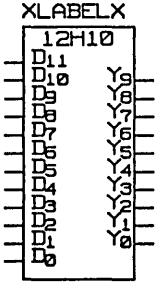

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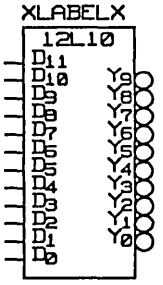

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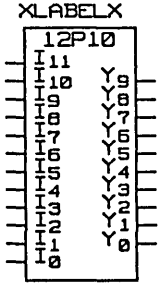

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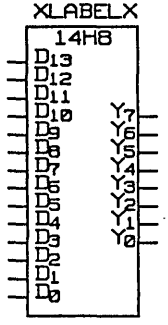

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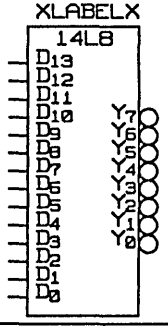

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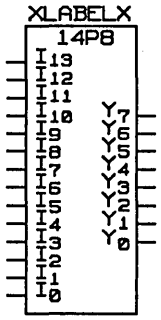

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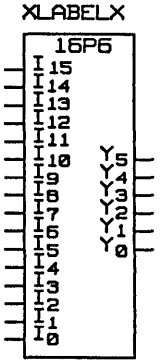

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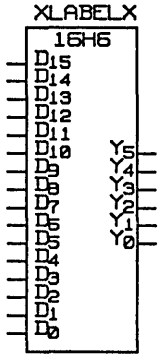

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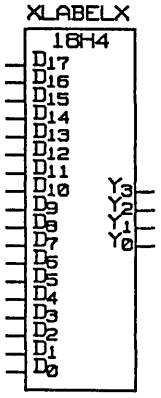

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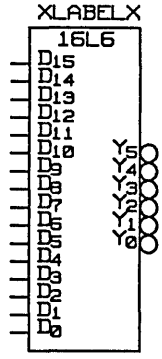

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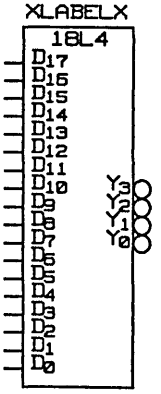

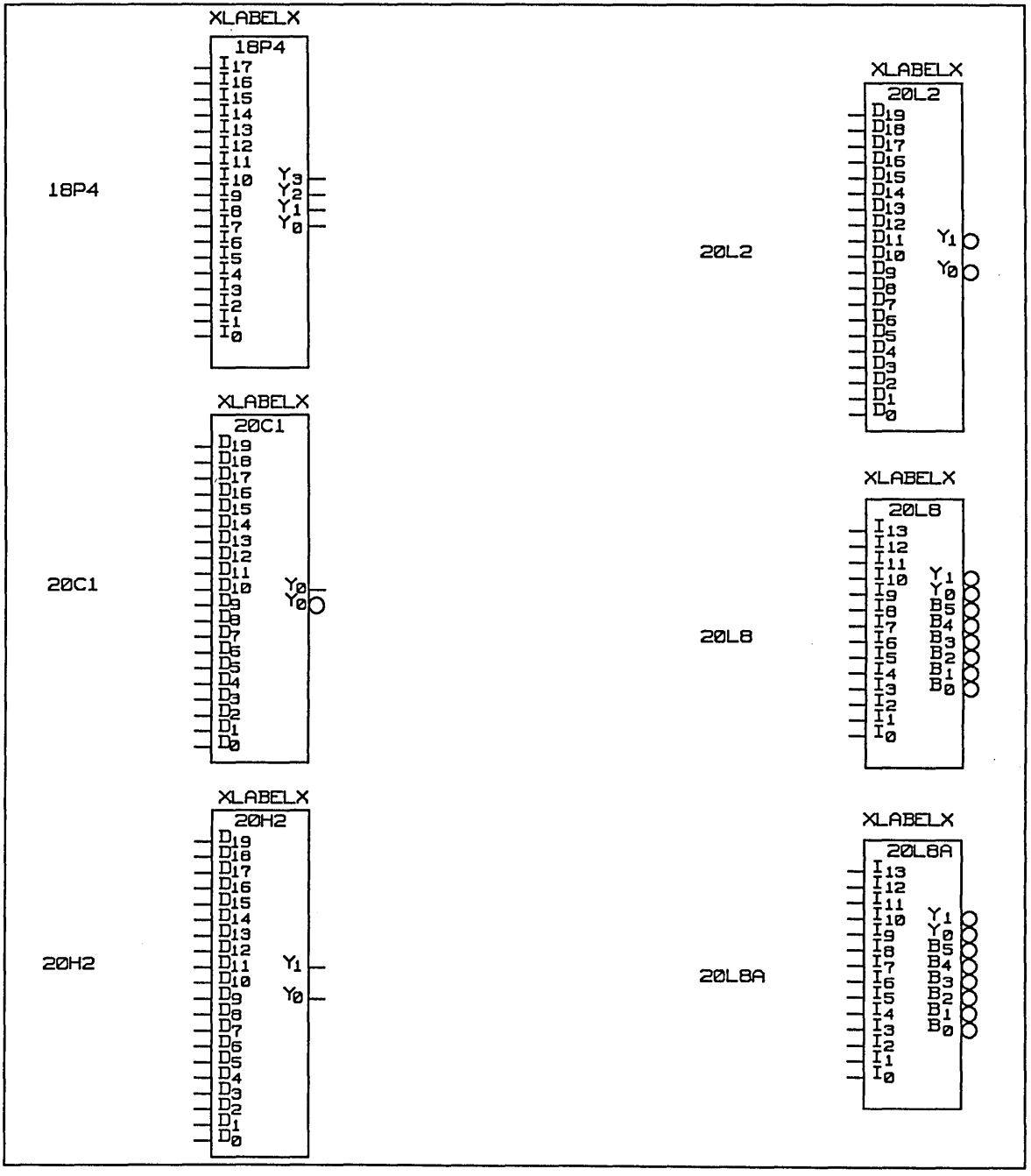
18P4
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18P4
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I5
I4
I3
I2
I1
I0
Y3
Y2
Y1
Y0
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XLABELX
20C1
D19
D18
D17
D16
D15
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D11
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D7
D6
D5
D4
D3
D2
D1
D0
Y0
Y0
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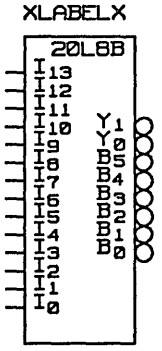
20L8B



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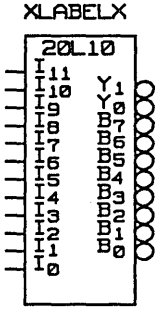

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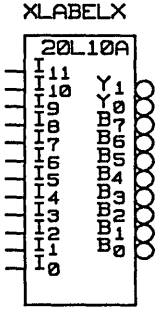

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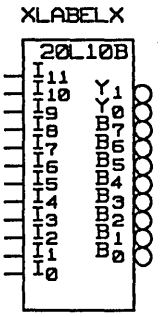

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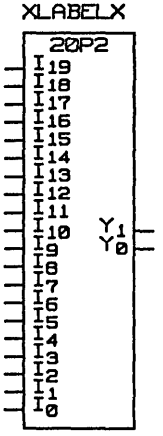

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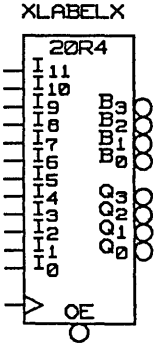

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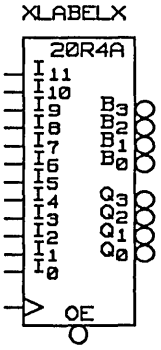

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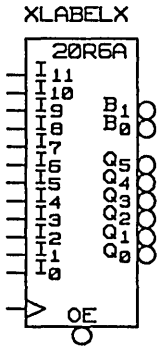

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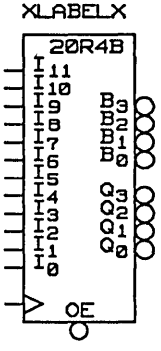

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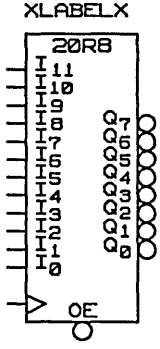

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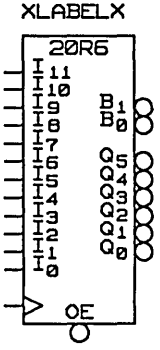

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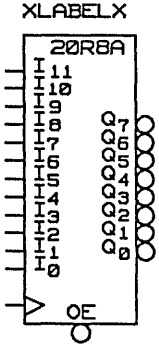

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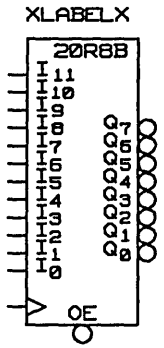

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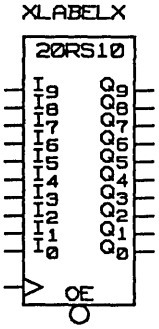

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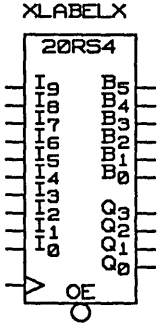

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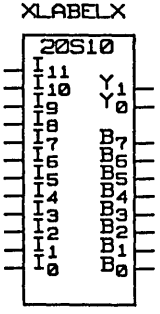

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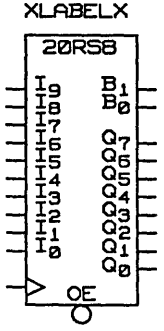

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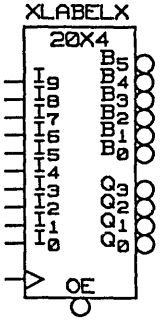

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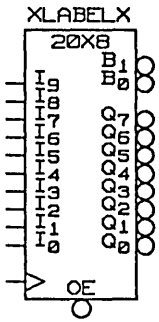

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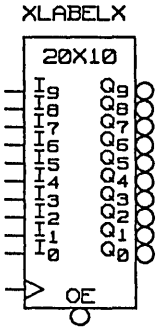

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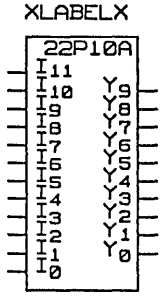
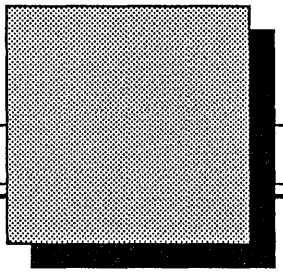




The ADVPAL Library

The ADVPAL Library requires approximately 1986 Kbytes of disk storage.

The specifications used to create the models in this library were taken from the following data books:

- Advanced Micro Devices
- Altera
- Lattice
- Monolothic Memories
- Texas Instruments

The appropriate data book is noted with each component.

The release level of the ADVPAL Library is 9.3.

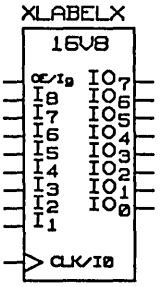
The library contains body drawings and physical, timing, and simulation models for the following 15 components:

16V8	Lattice GAL16V8A
18P8	AMD AMPAL18P8
18P8A	AMD AMPAL18P8A
18P8B	AMD AMPAL18P8B
20RA10	MMI 20RA10
20V8	Lattice GAL20V8A
22V10	AMD PAL22V10
22VP10	TI TIBPAL22VP10-25M
23S8	MMI AMPAL23S8
32R16	MMI PAL32R16
32VX10	MMI PAL32VX10
EP300	Altera EP300
EP600	Altera EP600
EP900	Altera EP900
T19L8	TI TIBPALR19L8

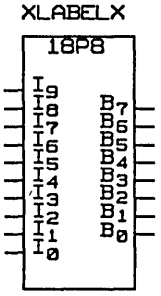
Application Notes

- The ADVPAL library requires the *libutil* software package; this package is installed in the */u0/tools* or */usr/valid/tools* directory.
- Please refer to the *Programmable Logic Devices User's Guide* at the front of this section.

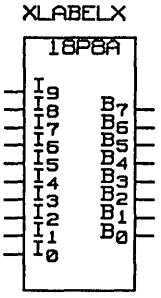
16V8



18P8



18P8A



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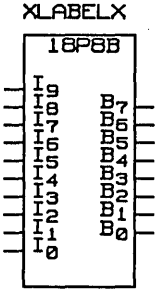

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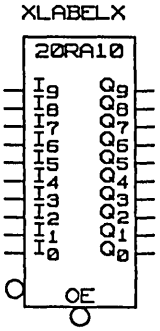

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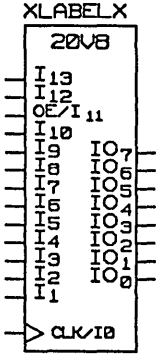

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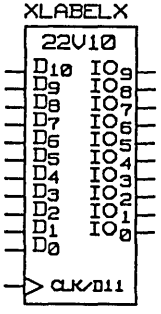

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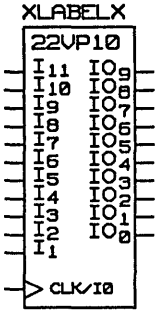
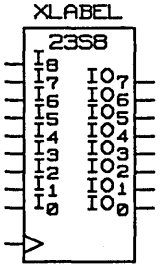


23S8



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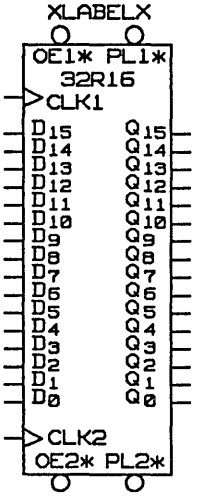

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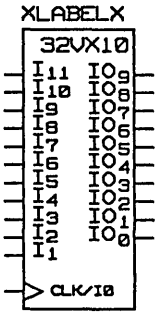

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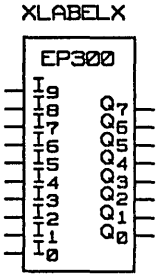

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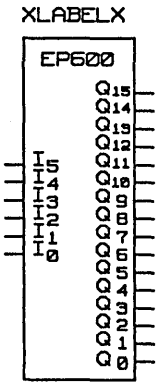

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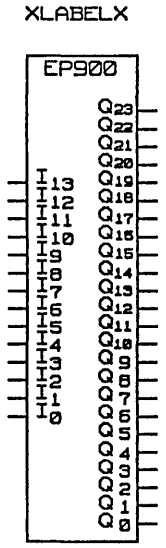
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Q22
Q21
Q20
Q19
Q18
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Q16
Q15
Q14
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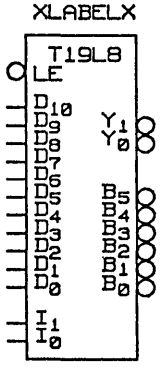
T19L8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D6
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Y1
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B5
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B1
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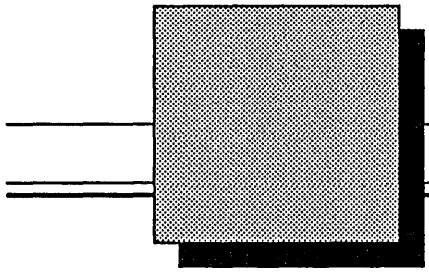


The IFL Library

The IFL Library requires approximately 711 Kbytes of disk storage.

The specifications used to construct the models in this library were taken from the Signetics data books.

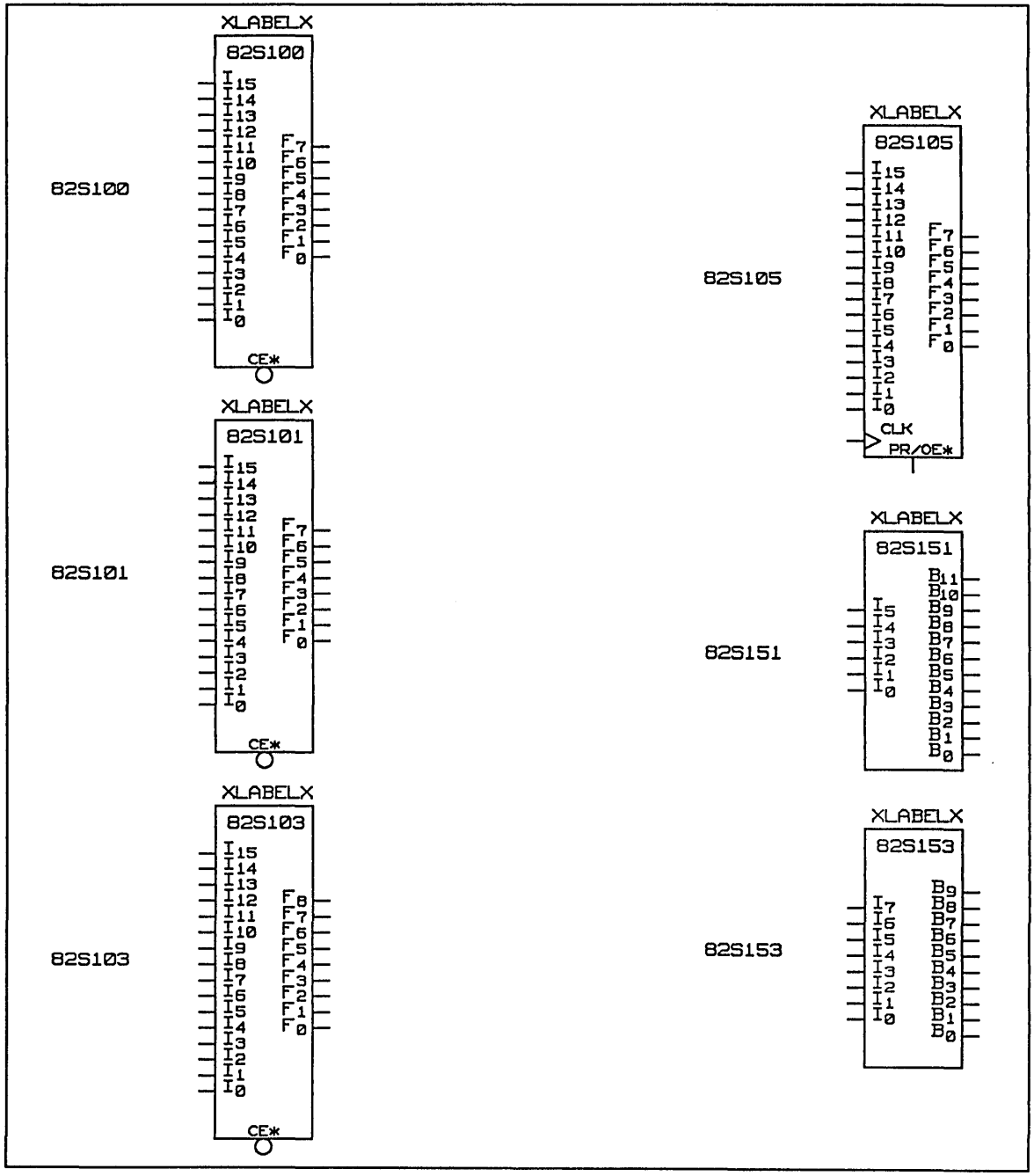
The release level of the IFL Library is 9.3.

The library contains body drawings and physical, timing, and simulation models for the following 12 components:

82S100	FPLA (Field Programmable Logic Array)
82S101	FPLA
82S103	FPGA (Field Programmable Gate Array)
82S105	FPLS (Field Programmable Logic Sequencer)
82S151	FPGA
82S153	FPLA
82S153A	FPLA
82S155	FPLS 4-Bit Register
82S157	FPLS 6-Bit Register
82S159	FPLS 8-Bit Register
82S161	FPLA
82S167	FPLS

Application Notes

- The IFL library requires the *libutil* software package; this package is installed in the */u0/tools* or */usr/valid/tools* directory.
- Please refer to the *Programmable Logic Devices User's Guide* at the front of this section.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XLABELX
82S100
I15
I14
I13
I12
I11
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I7
I6
I5
I4
I3
I2
I1
I0
F7
F6
F5
F4
F3
F2
F1
F0
CE*
82S101
XLABELX
82S101
CE*
82S103
XLABELX
82S103
CE*
82S105
XLABELX
82S105
CLK
PR/OE*
82S151
XLABELX
82S151
B11
B10
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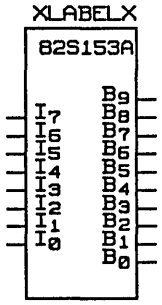
XLABELX
82S153

82S153A



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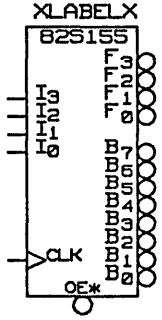

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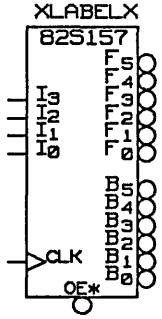

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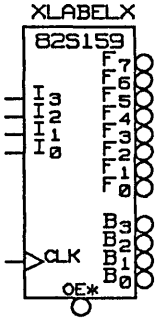

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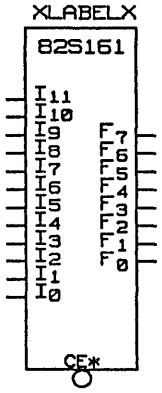
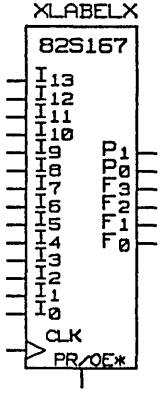
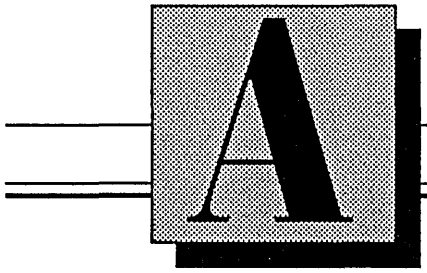


82S167





Additional Libraries

The following libraries are available for use on the SCALD system. These libraries are supplied directly by the manufacturer; for additional information, contact your Valid Sales Representative.

AMCCQ700	LMA 9K
C6000	MCA1200
CDC6000	MCA2500
FGC	MCA2800
HCA6300	MCA2900
LCA 10K	SCX3MU
LCB 15	TISC

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