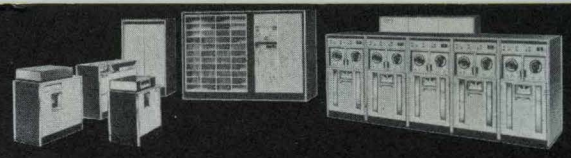


UNIVAC®
Solid-State Systems

GENERAL DESCRIPTION

UNIVAC
Solid-State II Systems

GENERAL DESCRIPTION

UNIVAC
Solid-State II Systems

Contents

1. Introduction

CONCEPT OF DESIGN

UNIVAC® Solid-State II Systems are general-purpose, digital computing systems designed to perform a wide range of business and scientific data-processing applications. They are characterized by a main memory composed of both magnetic drum and magnetic core. The practicality and economy of employing magnetic drums as main memory has been proved by the success of UNIVAC Solid-State Systems. The speed of magnetic core is apparent in such systems as UNIVAC III and UNIVAC 490 Real-Time Systems. By combining these storage elements in the UNIVAC Solid-State II System, Remington Rand UNIVAC designers make available in one computing system two extremely desirable data-processing features — storage speed and economy.

MAJOR FEATURES

- **Main memory composed of up to 96,800 digits of magnetic drum storage and 14,080 digits of magnetic core storage.**
- **Variable, expandable system configurations.**
- **Fast arithmetic and logic circuits. Transfer rate is 707,000 characters per second.**
- **High-speed magnetic tape and 80- or 90-column punched-card input-output.**
- **Up to 240 million digits of mass storage.**
- **9 index registers for programming ease and processing efficiency.**
- **Large instruction repertoire including multi-word transfers.**
- **Comprehensive software package including an assembly system and library routines for input-output handling, program loading, program testing, and mathematical functions.**
- **Extensive built-in checking. Provision for varied programmed accuracy checks.**
- **Bit manipulation facility allows use of varied input-output data codes and highly advanced programming techniques.**
- **Solid-state circuitry for increased speed and reliability, low operating costs, compact design.**
- **600 lines per minute high-speed output printing.**
- **Simultaneous read-write tape operations possible with dual synchronizers.**

AUTOMATIC PROGRAMMING

Programs for the UNIVAC Solid-State II System can be written in the language of the assembly system with mnemonic instruction codes and relative and symbolic addresses. Because the programmer is relieved of such tasks as the optimum placement of instructions, the use of the assembly system reduces coding time. This programming aid also allows large applications to be divided among several programmers and thus effects another reduction in coding time. Since sections of a problem may be individually coded and later assembled into a unified program, the assembler diminishes the chances for errors.

LIBRARY OF PROGRAMMED ROUTINES

For the UNIVAC Solid-State II System, a full complement of proven programming routines is available. This extensive library, which includes input-output routines, mathematical routines, and an assembly system, eliminates a considerable portion of the programming required to make a new system operative. Moreover, as the need for new routines emerges and programming refinements are developed, users can continue to obtain additions to their libraries.

APPLICATION VERSATILITY

Special capabilities suit the UNIVAC Solid-State II System to almost all applications. Because of its great storage capacity and the versatility of its on-line input-output units, the system can be programmed to perform, in one run, applications that demand several runs on other computers. Table look-up operations, for example, had formerly proved costly since the distribution of various types of information such as schedules, rate computations or sales-analysis figures required large amounts of storage and consumed long periods of expensive computer time. The new UNIVAC Solid-State II System makes such operations feasible by providing not only the necessary storage capacity but also rapid access time.

The capacity for bit manipulation, for instance, readily lends itself to statistical jobs. For such applications, punched-card capacity can be increased by using specialized codes in which each punch position is interpreted as a yes or no answer to a specific question. The system's microsecond calculating speeds greatly facilitate applications which entail lengthy or frequent mathematical operations such as the utilization of a rate table in payroll computations, for example. The UNIVAC Solid-State II System, then, outstandingly performs not only those applications mentioned but also an almost unlimited variety of data-processing tasks.

SOLID-STATE DESIGN

All control circuits for both the Processor and input-output units consist of solid-state circuit cards arranged in the Central Processor. Although there are over a thousand printed circuits in the system, almost all of them are mounted on only eight types of solid-state cards. As a result, production is standardized, and maintenance is reduced to a relatively simple operation. Malfunctioning circuits are easily located, and removed from the Processor, and a new circuit card is quickly slipped into place. In addition to ease of production and maintenance, these solid-state circuits impart a high degree of operating reliability to the Processor while reducing the power, cooling and space requirements of the system. As the superior reliability of solid-state circuitry eliminated the need for expensive duplicate self-checking circuits, in a similar fashion, the cost of duplicating off-line control circuits in the input-output units was also eliminated by combining them — that is, by making the same circuit do double or triple duty.

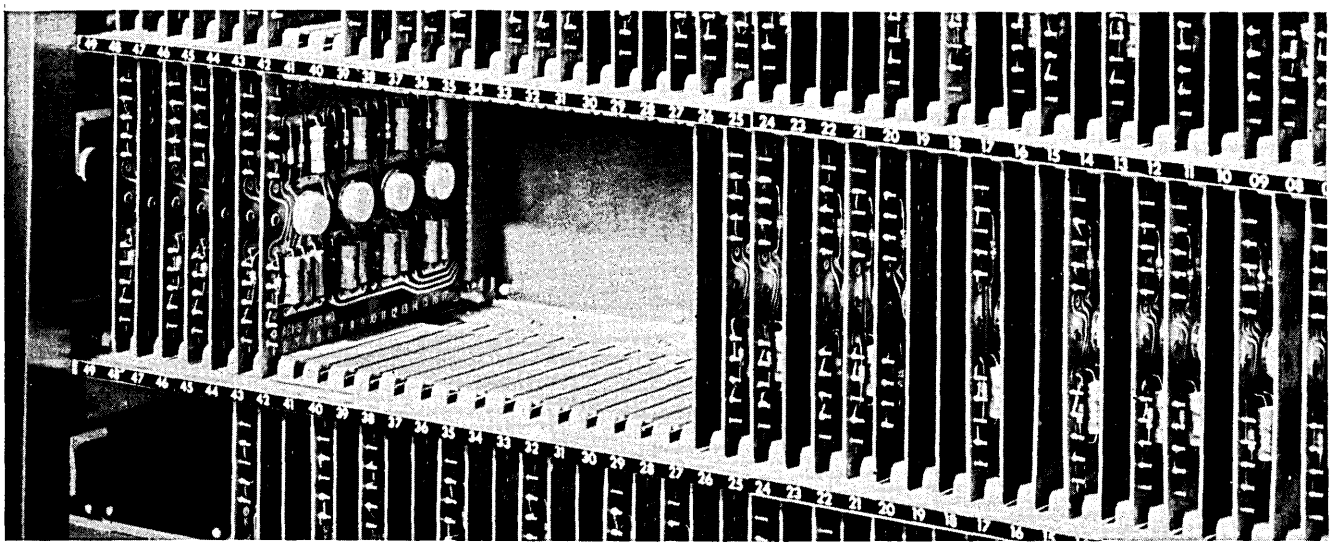


Figure 1-1. Solid-State Circuitry

2. Systems Configurations

In the UNIVAC Solid-State II System, large data storage and fast computing capabilities are combined with means to handle a variety of input-output media. Included are punched-cards, metallic or MYLAR* tape, and printed hard copies. With each medium, a variety of formats is possible to accommodate the specialized needs of almost all applications. The operating speeds of the input-output units which handle these media can be maintained at a consistently high level because the UNIVAC Solid-State II System is completely buffered for simultaneous operations. The reliable accuracy checks that have always been standard on all UNIVAC equipment are provided for all input-output devices.

A basic UNIVAC Solid-State II System is composed of a Central Processor, an input-output synchronizer, from one to ten UNISERVO** magnetic tape units, and a High-Speed Printer (Figure 2-1). This configuration provides high-volume magnetic tape input-output and output printing.

In all configurations the Central Processor includes 14,080 digits of magnetic core main memory and from 28,600 to 96,800 digits of magnetic drum main memory. Optional main memory capacity is only one of several optional features offered with Solid-State II Systems.

For applications requiring punched-card input-output, a High-Speed Card Reader and a Card Read-Punch Unit may be included (Figure 2-2). These units are optional components in any UNIVAC Solid-State II configuration. Models are available for handling 80-column or 90-column cards.

At the option of the user, magnetic tape handling capacity may be doubled. This is achieved by adding another synchronizer and from one to ten additional tape units.

From one to ten RANDEX**mass storage units may be included with any UNIVAC Solid-State II System. The data flow synchronizer for the RANDEX system is housed in the same cabinet with one of the tape synchronizers. Each RANDEX unit contains two storage drums with a combined capacity of 24 million digits of information. The 240 million digits of mass storage provided by a RANDEX system offers adequate capacity for the most demanding mass storage applications (Figure 2-3).

MYLAR is a registered trademark of the E. I. du Pont de Nemours & Co., Inc.

***Trademark of the Sperry Rand Corporation.*

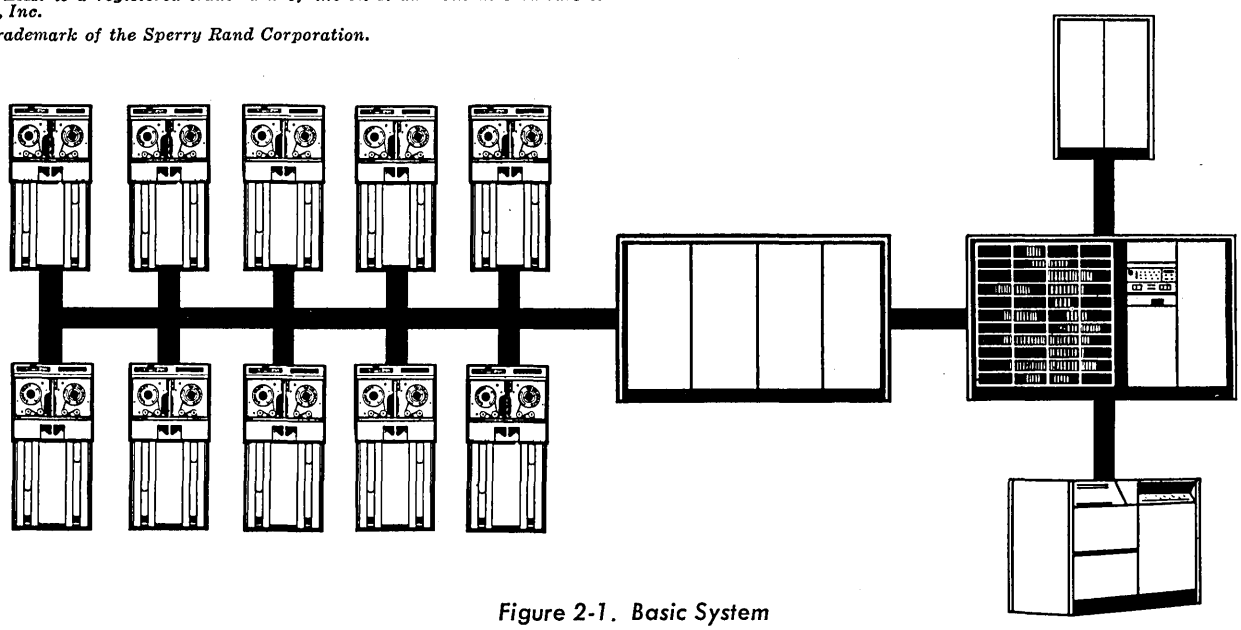


Figure 2-1. Basic System

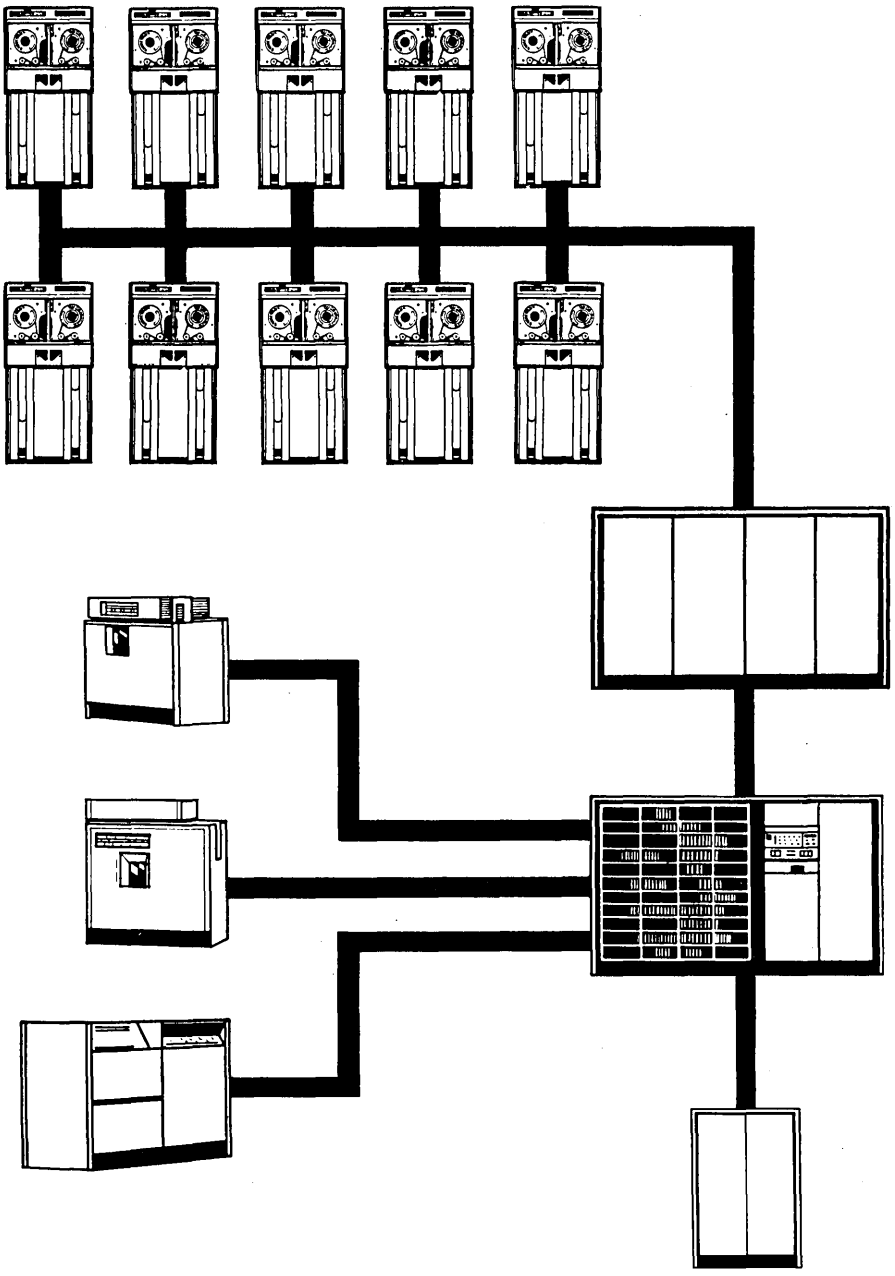


Figure 2-2. Basic System With Punched-Card Input-Output

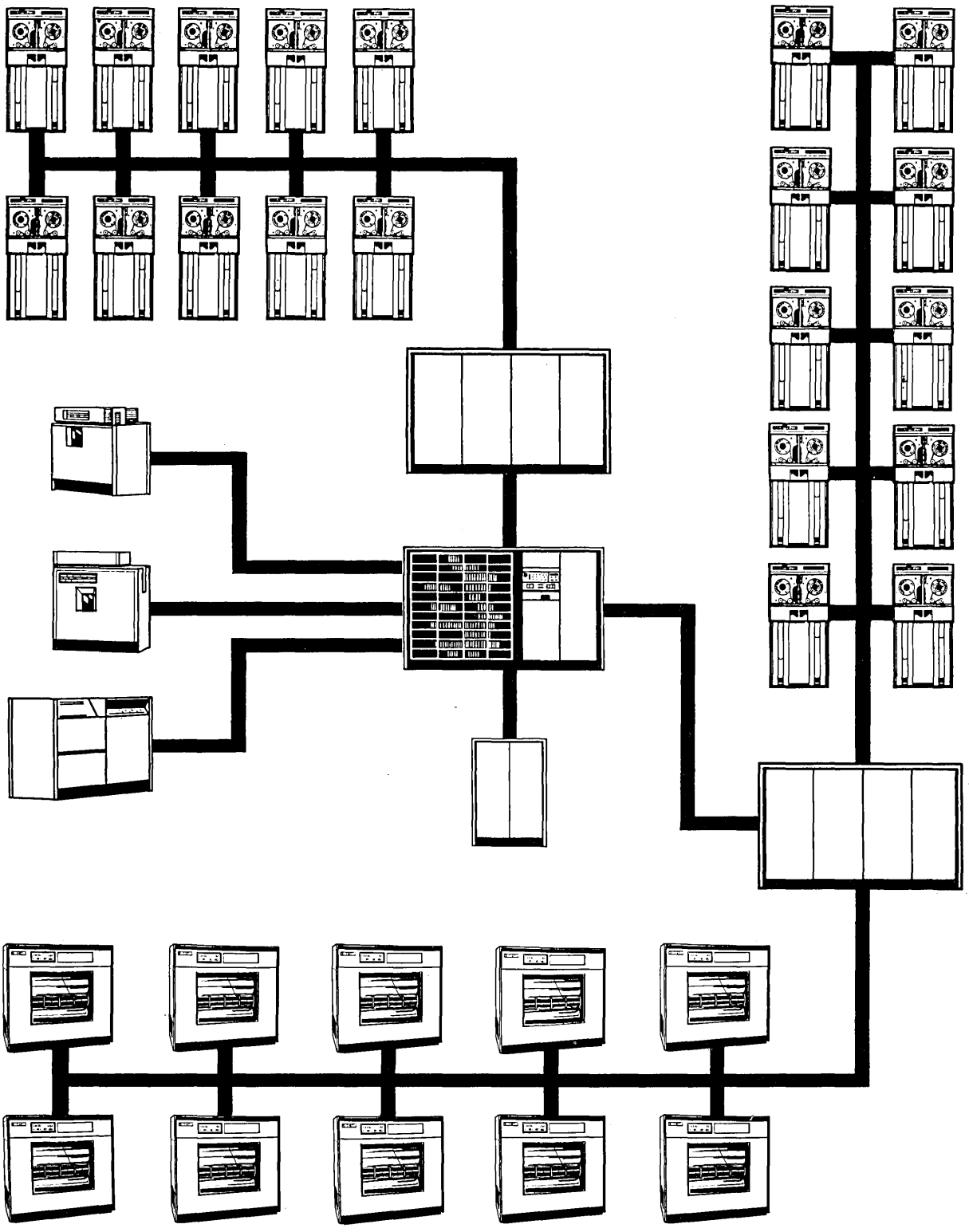


Figure 2-3. Schematic, Expanded Tape System With Mass Storage

3. Systems Components

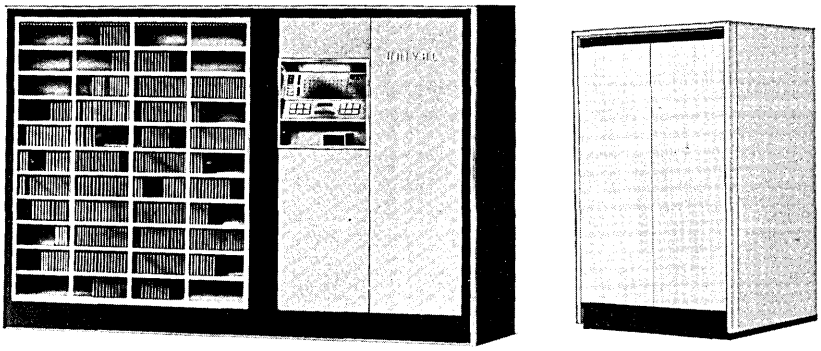


Figure 3-1. Central Processor and Core Storage Unit

Each component of the UNIVAC Solid-State II System is designed to impart the greatest data-processing capacity at the most economical cost.

CENTRAL PROCESSOR AND CORE STORAGE

Under guidance of an internally stored program, the Central Processor controls and coordinates the many interdependent activities of the UNIVAC Solid-State II System. It also houses the drum storage memory and the circuitry which performs arithmetic, data transfer, and logical operations such as data comparisons and translations. Functionally, the Central Processor is divided into three parts: arithmetic, control, storage.

Storage Characteristics

DATA REPRESENTATION:
Binary-coded decimal (biquinary)

WORD FORMAT:
11 decimal digits (including sign)

STORAGE METHOD:
Magnetic drum and magnetic core (separate cabinet)

DRUM CAPACITY:
2,600 to 8,800 words

CORE CAPACITY:
1,280 words

Control Characteristics

INSTRUCTION FORMAT:
2 address
2-digit operation code;
4-digit operand address;
4-digit address of next instruction

INSTRUCTION CYCLE:
1. Staticize instruction
2. Index register modification (if specified)
3. Access operand
4. Execute instruction
5. Access next instruction

INSTRUCTION REGISTERS:
rC, (holds instruction word); static register (holds operation code)

INDEX REGISTERS:
9

OPERATOR CONTROL:
Display panel and keyboard

Arithmetic Characteristics

REGISTERS:
rA, rL, rX (addressable)

TRANSFER RATE:
707,000 characters per second

TYPICAL TIMES:
1,176,470 additions or subtractions per minute

LOGIC:
Fixed-point

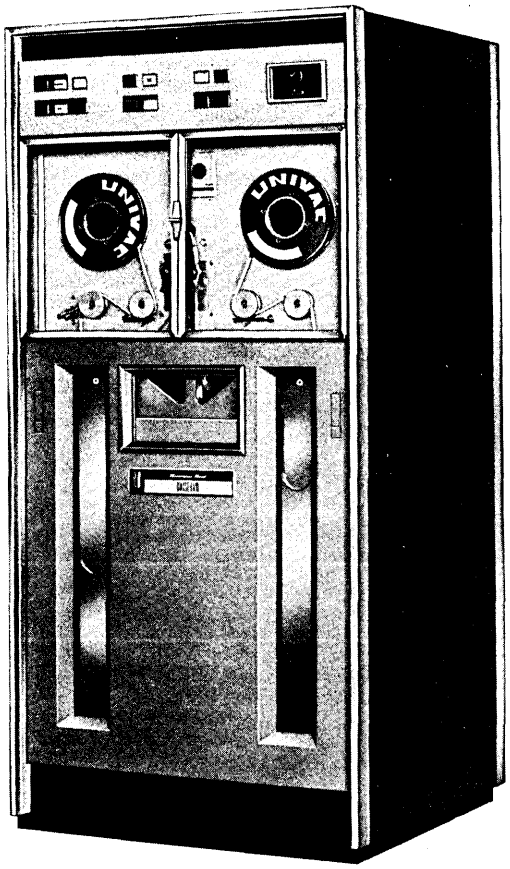


Figure 3-2. UNISERVO Tape Unit

UNISERVO MAGNETIC TAPE UNITS

Up to 20 UNISERVO magnetic tape units may be included in a UNIVAC Solid-State II System to provide extremely high-speed, accurate data input and output. In addition, they provide processing compatibility with almost all UNIVAC Computing Systems:

Characteristics

COMPATIBLE SYSTEMS:
- UNIVAC III SYSTEM
- UNIVAC 490 Real-Time System
- UNIVAC 1107 Thin-Film Memory System
- UNIVAC File-Computer
- UNIVAC Solid-State 80-90
- UNIVAC I and II

TAPE CODES:
- Any 6-bit plus odd check bit binary coded decimal (normally UNIVAC XS-3 or Solid-State II internal data code)

TAPE SPEED:
- 100 inches per second

RECORDING DENSITY:
- 125 cpi (low) or 250 cpi (high)

SIMULTANEOUS OPERATIONS:
- Simultaneous read and write operations possible with dual synchronizers

START TIME (ms):
- Read: 12.05 (250 cpi); 18.5 (125 cpi)
- Write: 12.0 (250 cpi); 18.8 (125 cpi)

STOP TIME (ms):
- Read: 9.15 (250 cpi); 16.25 (125 cpi)
- Write: 11.1 (250 cpi); 17.8 (125 cpi)

READING DIRECTION:
- Forward or backward

BLOCK SIZE:
- 120, 720, or 1100 characters

TAPES:
- Metallic or MYLAR

TAPE LENGTH:
- 1500 feet (maximum) or 2400 feet (maximum)

Operating Features

Each UNISERVO unit may read data into the system from tape moving in either a forward or backward direction, write on tape moving in a forward direction, and rewind its own tape. The units are essentially the same units that have proved so successful with other UNIVAC Systems. They are designed to permit fast tape mounting and ease of operation. A single switch on the front panel of each unit permits interchanging of metallic or MYLAR tape as required.

A number of checks is provided to maintain accuracy of information read or recorded in the various tape formats. Bad spots in the tape are detected photoelectrically.

Reading and writing are controlled by program instructions stored in main memory. These functions are coordinated by the synchronizer.

HIGH-SPEED CARD READER

The High-Speed Card Reader is a fast, accurate means of feeding information into the system. Two models of the Card Reader are available. The Card Reader 80 reads 80-column cards; the Card Reader 90 reads 90-column cards.

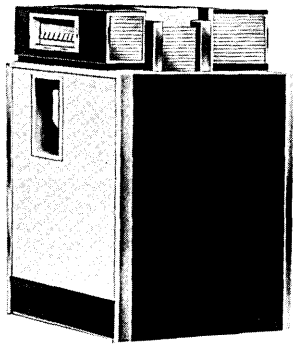


Figure 3-3. High-Speed Card Reader

Characteristics

BASIC SPEED:
600 cards per minute

BASIC CARD SIZE:
Standard 80-column or 90-column cards

OPTIONAL CARD SIZES:
22, 23+, 51, or 66 column short card forms (Card Reader 80)
16, 27, or 29 column short card forms (Card Reader 90)
Card feed mechanism can be easily adjusted to accept all card sizes. The use of short card sizes does not affect operating speed

STACKER SELECTION:
3 stackers

Operating Features

The card transport system consists of an input magazine, read station 1, read station 2, and three output stackers. Operation of the Card Reader is completely controlled by the program stored in the Central Processor. Cards stacked in the input magazine are fed into continuously revolving rollers that transport them through the two reading stations. Then they are sent to one of the output stackers. During its course through the transport system, a card conveys its contents to the Central Processor when it is brush-sensed at each read station in turn. The presence of two read stations permits the Processor to perform a complete verification and audit on all information entering the system.

CARD READ-PUNCH UNIT

The Card Read-Punch Unit is both an input and an output component of the Solid-State II System. It may be used to read input information from punched-cards into the system, and/or prepare processing results in punched-card form as output. Models are available for processing 80- or 90-column cards.

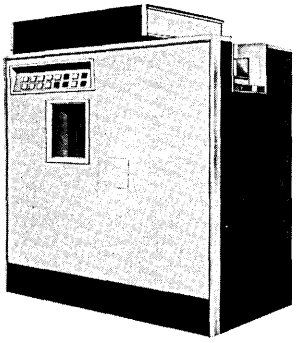


Figure 3-4. Card Read-Punch Unit

Characteristics

SPEED:
150 cards per minute

CARD SIZE:
Standard 80-column or 90-column cards

STACKER SELECTION:
2 stackers

Operating Features

The card transport system is composed primarily of an input magazine, read station 1, punch station, read station 2, and two output stackers. Movement of cards through the transport system is completely controlled by the program stored in the Central Processor. During its course through the transport system, the contents of a card are read at the first read station. After output information has been punched at the punch station, the card is read again at the second read station and deposited in an output stacker. The second read station permits the Processor to be programmed to compare the results of the second read with both the first read and punching results to assure accuracy of both reading and punching.

HIGH-SPEED PRINTER

The High-Speed Printer produces printed output information, intermediate processing results, distributed accumulations and balances, and final reports.

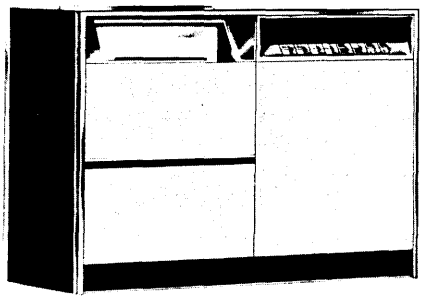


Figure 3-5. High-Speed Printer

Characteristics

SPEED:
600 lines per minute (maximum)

LINE CHARACTERS:
51 (26 alphabetic capitals; 10 numerals; 15 punctuation marks and special symbols)

VERTICAL LINE SPACING:
6 lines per inch (standard) 8 lines per inch (optional)

HORIZONTAL SPACING:
10 characters per inch

PAPER STOCK:
Any sprocket-fed paper, 4 to 21 inches wide, up to and including card stock, either blank or preprinted

COPIES:
An original and at least five carbon copies using paper between 11 and 13.5 pounds in weight

Operating Features

The design of the High-Speed Printer incorporates speed and accuracy with mechanical sturdiness and reliability. It is essentially a wheel printer equipped to produce clearly printed copy similar to that printed by a typewriter or conventional punched-card tabulating equipment.

The availability of 51 printable characters allows complete and final reports to be prepared on the High-Speed Printer in one operation. All operations of the High-Speed Printer are controlled by the program stored in the Central Processor.

RANDEX UNITS

A RANDEX System is composed of a synchronizer and one to ten RANDEX Drum File units which provide up to 24 million digits of mass data storage. Each unit contains two storage drums.

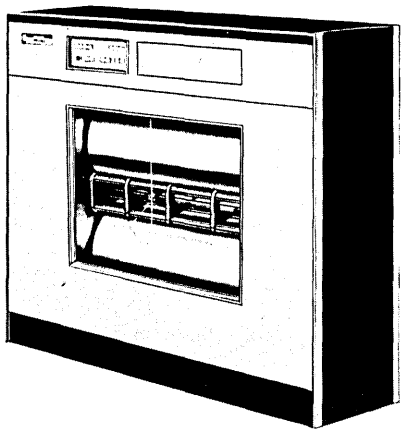


Figure 3-6. Randex Drum File

Characteristics

UNIT CAPACITY:
24 million digits

DATA CODE:
Any 4-bit code plus parity bit

TRACKS PER UNIT:
4,000

BLOCK SIZE:
48 11-digit words (including sign)

BLOCKS PER TRACK:
12

BIT DENSITY:
650 pulses per inch

ACCESS TIMES:
35 milliseconds read or write. No head movement
125 milliseconds minor head movement
550 milliseconds maxmium major head movement

Operating Features

RANDEX operates completely on-line under control of the program stored in main memory. However, RANDEX instructions are executed within the synchronizer. This leaves the Central Processor free to perform other operations. Information flowing to and from the drum units and main memory passes through the synchronizer and the input-output buffer.

4. Storage Features

DRUM-CORE MEMORY PHILOSOPHY

Memory size and speed of access are often major considerations in the selection of an electronic data-processing system. Perhaps more often the cost of the system is an even greater consideration. Today magnetic drums offer one of the most economical memory devices in terms of cost per unit stored. A possible disadvantage of drum storage, however, is that latency time may be consumed in accessing locations. Although instructions can usually be arranged in drum storage to eliminate a loss of time in accessing the next instruction, data is received in a random fashion and so complicates the problem of minimizing access time. The UNIVAC Solid-State II System, however, allows instructions to be stored in minimum latency on the drum and data to be stored in the "no latency" core. In this way, the UNIVAC Solid-State II System provides essentially the same speed as an all core system but at less cost.

From the standpoint of processing efficiency and programming simplicity, drum-core memory solves the latency problem intrinsic in drum memory computing systems. In this respect, latency may be described as the time that elapses until a particular required piece of information can be accessed for processing. For example, if drum storage word location 0010 is required for processing at a point in time when word location 0000 is under the drum read-write heads, there is a latency period before rotation of the drum brings location 0010 under the read-write heads.

On the memory drum of the UNIVAC Solid-State II, this latency period would amount to 170 microseconds. With the availability of core memory, however, there is no latency time required to access any word location in core memory. Minimum latency coding techniques can greatly reduce latency time in accessing data stored on the magnetic drum. However, the availability of 1280 words of core memory in addition to the drum memory virtually eliminates the need for intense minimum latency planning, increases program running efficiency, and simplifies the programming effort.

WORD FORMAT

Information is processed by the Central Processor and stored in memory in units known as "words." A word is composed of ten decimal digits, an algebraic sign, and a space between words (Figure 4-1). The digit positions are numbered 1 to 11, from left to right. Digit 1 is the most significant digit *(MSD)*; digit 10 is the least significant digit *(LSD)*.

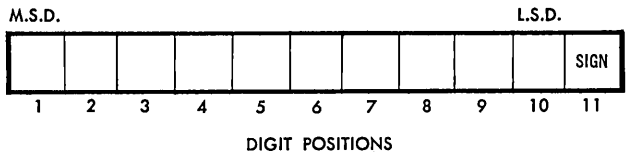


Figure 4-1. Word Format

Words are of two types, data words and instruction words. A data word contains information to be processed; an instruction word contains a processing command. Thus, instruction words control and direct the processing of data words.

COMPUTER CODE

The computer code for the UNIVAC Solid-State II System is a modified biquinary notation in which each digit is represented by four bits having the value 5-4-2-1. An odd parity bit is added to each of the ten digits of a word to ensure accuracy of transmission. That is, if an even number of bits is present in a digit, a bit is added in the parity (leftmost) position; if an odd number is present, no bit is placed in the parity position. During data transmission, the Processor checks every digit to see that an odd number of bits is still present.

The binary bit positions 5-4-2-1 denote the weight or value of a binary one when it appears in one of the positions. The value 9, for example, is represented by the combination of binary ones in binary bit positions 5 and 4 (5 + 4 = 9) and binary zeros in positions 2 and 1.

A data word containing the value 9,281,547,936 would be represented in storage as shown in Figure 4-2.

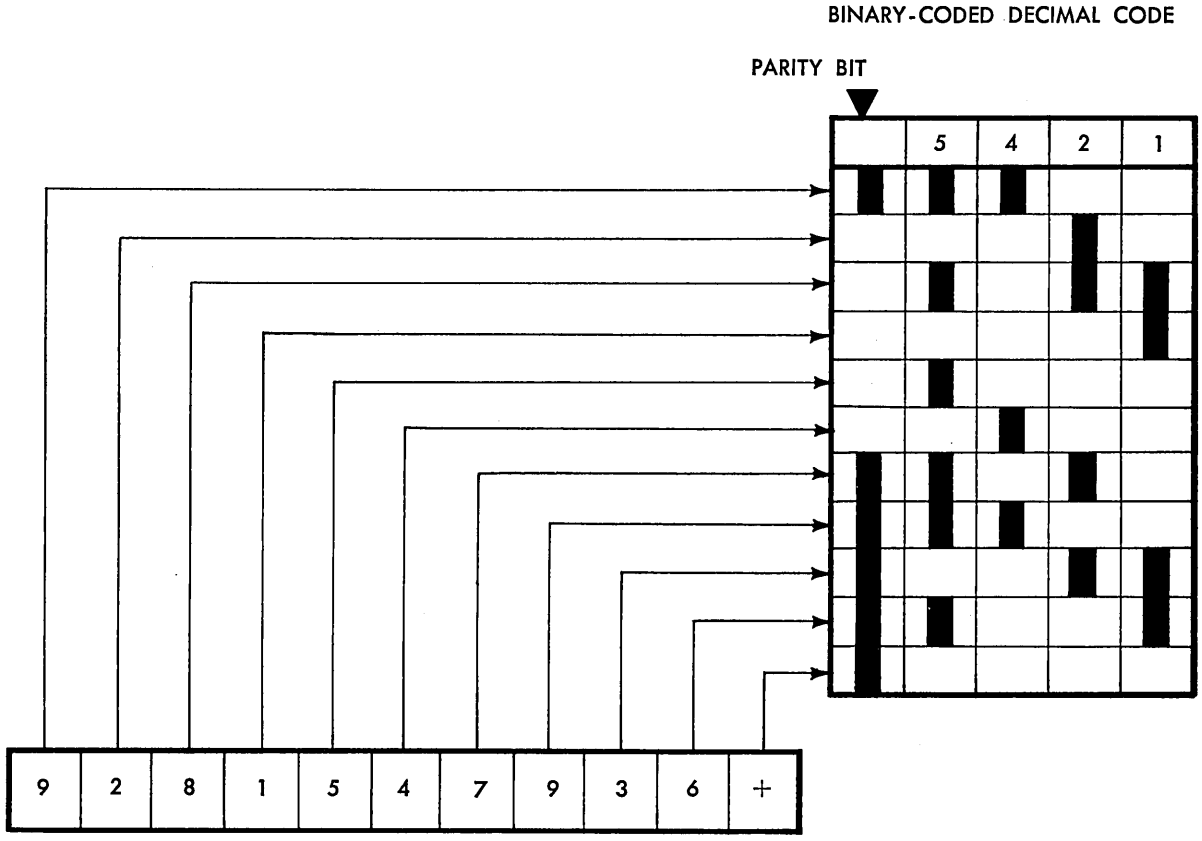


Figure 4-2. Binary Representation of Data Word

A ten-character group of information is represented in the Processor by two computer words: a numeric and a zone word. For the representation of numbers, only the numeric word has significance since the zone contains zeros only. The numbers 1 through 9 and 0 are represented in one computer word in computer code as:

	5421	5421	5421	5421	5421	5421	5421	5421	5421	5421
NUMERIC	0001	0010	0011	0100	1000	1001	1010	1011	1100	0000
	1	2	3	4	5	6	7	8	9	0

Alphabetic information in computer code requires the presence of bits in both the numeric and the zone words. The letters A through J of the alphabet appear in computer code as:

	5421	5421	5421	5421	5421	5421	5421	5421	5421	5421
NUMERIC	0001	0010	0011	0100	1000	1001	1010	1011	1100	0001

	5421	5421	5421	5421	5421	5421	5421	5421	5421	5421
ZONE	0001	0001	0001	0001	0001	0001	0001	0001	0001	0010
	A	B	C	D	E	F	G	H	I	J

Figure 4-3 contains the internal computer codes for the Solid-State II System. To be processed arithmetically or logically, information must be represented in computer code. Automatic translation instructions are available to convert UNIVAC XS-3 magnetic tape code, and 80- or 90-column punched-card codes to computer code. Information may be stored in the computer in any code.

DRUM STORAGE

The magnetic drum in the UNIVAC Solid-State II System is much like the one shown in Figure 4-4.

Located within the Central Processor, the drum measures approximately eight inches in diameter. It provides 2,600 to 8,800 words of main memory for the UNIVAC Solid-State II System.

Information is represented on the surface of the drum by magnetized spots arranged in binary codes where the presence of a spot represents a binary 1 and the absence of a spot represents a binary 0. Any spot recorded on the drum will remain there permanently, or until it is erased for the recording of another spot at the same location. Power to the system may be turned off completely without loss of information recorded on the drum.

(Zone) 5421	(Numeric) 5421	Printing Character
0000	0000	0
0000	0001	1
0000	0010	2
0000	0011	3
0000	0100	4
0000	1000	5
0000	1001	6
0000	1010	7
0000	1011	8
0000	1100	9
0001	0001	A
0001	0010	B
0001	0011	C
0001	0100	D
0001	1000	E
0001	1001	F
0001	1010	G
0001	1011	H
0001	1100	I
0010	0001	J
0010	0010	K
0010	0011	L
0010	0100	M
0010	1000	N
0010	1001	O
0010	1010	P
0010	0010	Q
0001	1100	R
0011	0010	S
0011	0011	T
0011	0100	U
0011	1000	V
0011	1001	W
0011	1011	Y
0011	1010	X
0011	1100	Z
0001	1111	#
0001	0101	.
0010	0101	$
0011	0101	, Comma
0000	0110	Space (N.P.)
0011	0000	+
0001	0110	:
0010	0110	*
0011	0110	%
0001	0111	&
0011	0001	/
0000	0111	)
0000	1111	' Apostrophe
0000	1110	;
0000	1101	(

Figure 4-3. Computer Codes

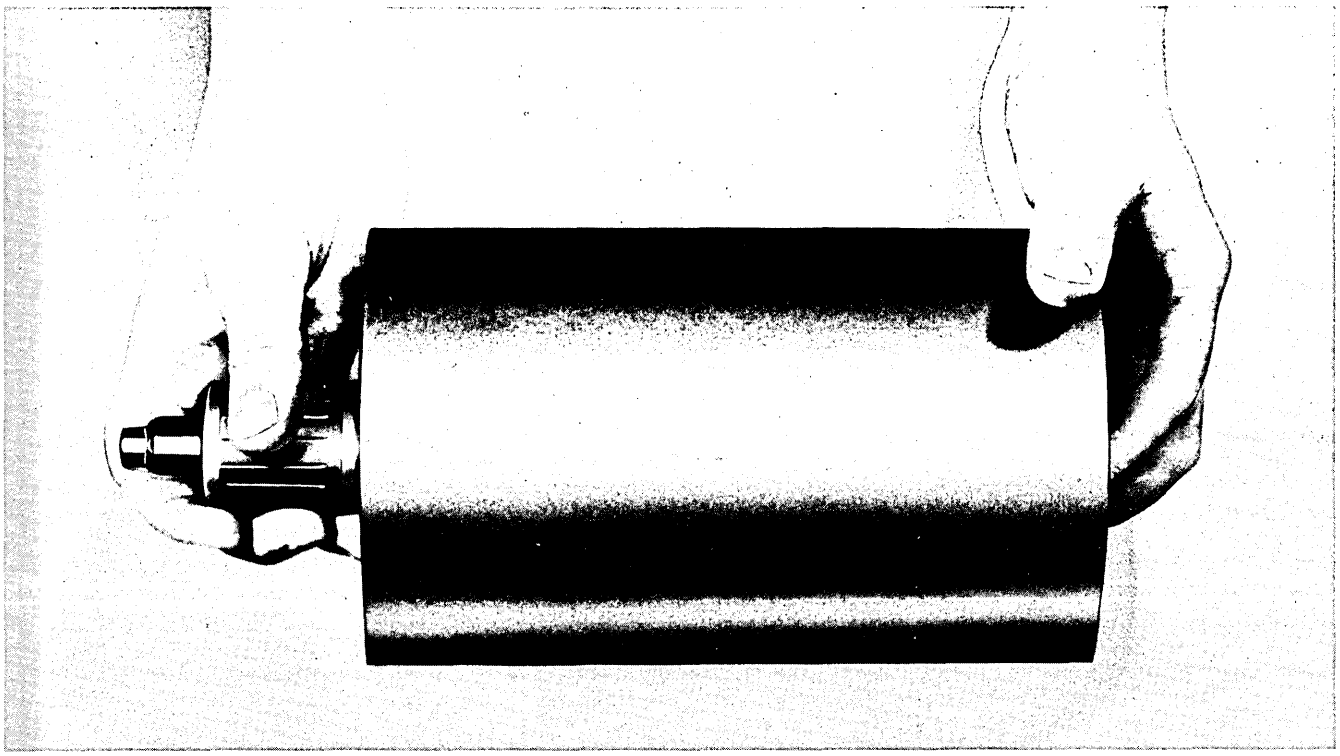


Figure 4-4. Storage Drum

The storage drum is divided into two major areas: main storage, and buffer storage.

Main Storage Area

The main storage area is composed of a number of storage bands which gird the periphery of the drum. Each band stores 200 words. The total number of bands on the drum is, of course, determined by the word-capacity of the drum selected by the user. A 2600-word drum is composed of 13 main storage bands; an 8800-word drum has 44 storage bands.

Starting with the most significant digit of a word, the pattern of bits representing each digit is recorded on the surface of the drum. At the instant of writing, the five bits of a digit are entered in parallel across a band. Each bit is deposited on a "track" which is merely a further vertical subdivision of a band. The remainder of the word is recorded on the drum in the same manner. Thus, words are recorded *serially,* digit-by-digit, five bits at a time.

Data Access

Information is recorded and removed from the drum by means of read-write heads positioned over each storage band near the drum surface. Data reading or writing occurs as the drum rotates at a speed of 17,670 revolutions per minute under the read-write heads.

Certain bands in main storage are serviced by one read-write head per band. These bands constitute the *standard-access area* of the drum. Maximum access time (time required to store or access information from the drum) for the standard access area is 3.4 milliseconds, or the time required for the drum to make one complete revolution under the read-write heads.

Other bands are called *high-speed access bands,* because they are serviced by four read-write heads, positioned 90 degrees apart around the drum. Maximum access time on the high-speed access bands is 0.85 milliseconds, or the time required for the drum to complete one-fourth of a revolution.

Access times are more readily measured in units of *word times.* A word time is the time required for one word location to pass beneath the read-write heads. Therefore, minimum access time on the high-speed and standard access bands is one word time. One word time is equivalent to .017

milliseconds. Maximum access time on the standard access bands is 200 word times; on the high-speed access bands it is 50 word times.

Addressing

Storage locations on the drum are identified by 4-digit addresses numbered consecutively beginning with 0000 and ranging to 8799.

As shown in Figure 4-5, words at the same horizontal position on all bands of the drum are considered to be on the same drum level. On each band, there are 200 levels, numbered 0000 to 0199. Each band on the drum is also numbered. The first band is the 00 band. The last band on a 5000-word drum is band 48; on an 8800-word drum, the last band is 86.

Therefore, any word location address is formed by adding the band number to the word level number. For example, location 4199 is obtained by adding level 199 to band 40.

2600-Word Drum Specifications

CAPACITY:
2,600
WORD ADDRESS RANGE:
0000 — 2599
BAND ADDRESS RANGE:
00 — 22 and 40
WORD TIME:
17 microseconds
STANDARD ACCESS AREA:
Capacity: 2,400 words
Word Address Range: 0000 — 2399
Band Address Range: 00 — 22
HIGH-SPEED ACCESS AREA:
Capacity: 200 words
Word Address Range: 4000 — 4199
Band Address: 40

5000-Word Drum Specifications

CAPACITY:
5,000 words
WORD ADDRESS RANGE:
0000 — 4999
BAND ADDRESS RANGE:
00 — 48
WORD TIME:
17 microseconds
STANDARD ACCESS AREA:
Capacity: 4,000 words
Word Address Range: 0000 — 3999
Band Address Range: 00 — 38
HIGH-SPEED ACCESS AREA:
Capacity: 1,000 words
Word Address Range: 4000 — 4999
Band Address Range: 40 — 48

8800-Word Drum Specifications

CAPACITY:
8,800-words
WORD ADDRESS RANGE:
0000 — 8799
BAND ADDRESS RANGE:
00 — 86
WORD TIME:
17 microseconds
STANDARD ACCESS AREA:
Capacity: 7,600 words
Word Address Range: 0000 — 3999;
5000 — 8599
Band Address Range: 00 — 38;
50 — 84

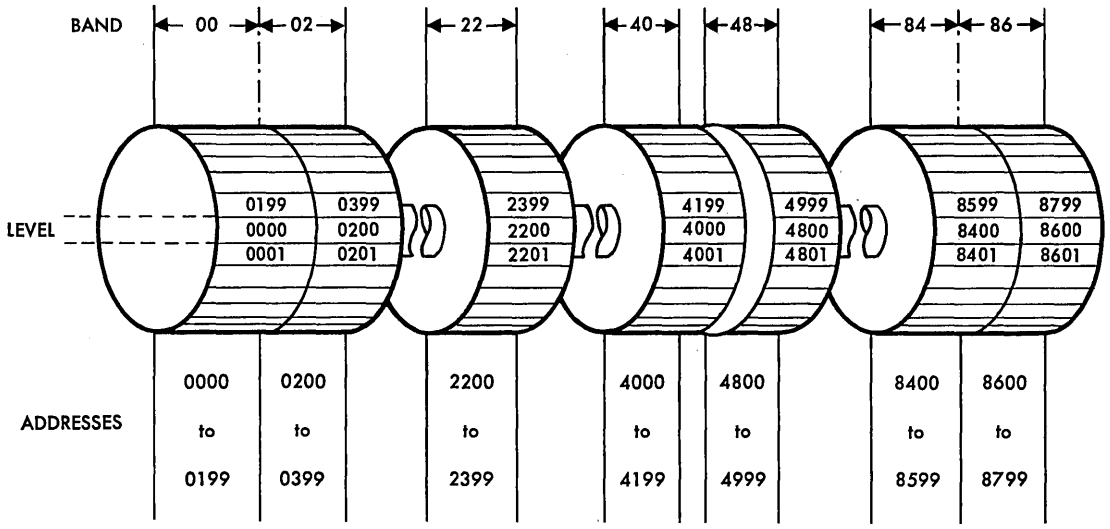


Figure 4-5. Schematic, Magnetic Storage Drum

HIGH-SPEED ACCESS AREA:
Capacity: 1,200 words
Word Address Range: 4000 — 4999;
8600 — 8799
Band Address Range: 40 — 48;
86

Buffer Storage Area

The buffer storage area on the drum permits data input, computing, and data output functions to overlap and occur simultaneously. The ability to effectively *combine* these operations, rather than have them occur end-on-end, allows the Solid-State II System to accomplish more work in a given period of time and achieve a greater overall operating efficiency.

Acting as an intermediary, the buffers compensate for the difference in operating speeds of the Central Processor and its external units. Moreover, they prevent relatively slow mechanical operations, such as printing, card punching, or card reading, from inhibiting much faster electronic operations such as arithmetic and internal data transfer functions within the Central Processor. This is achieved by relieving the Central Processor of the need to contact *directly* any input-output unit. Instead, it communicates only with the various input-output buffers.

All input and output information flowing from main storage to the external units, and vice versa, must pass through the buffer area. Buffers are provided on the drum for each input and output unit in a Solid-State II System. Further, there are available, in the repertoire of instructions, tests inquiring whether these buffers are loaded. In this way, the Central Processor can, in effect, handle the input-output devices on a program interrupt basis.

CORE STORAGE

In addition to its large magnetic drum memory, the UNIVAC Solid-State II System possesses 1,280 words of magnetic core memory. Core memory is composed of many tiny rings (cores) wired in a square plane such as the one shown in Figure 4-6.

Core planes are arranged in a stack large enough to contain 1,280 11-digit words. Each magnetic core stores one bit of information in the 5-4-2-1 binary code of the Processor. When magnetized in one direction, a core contains a binary 1; when magnetized in another direction a binary 0 is represented.

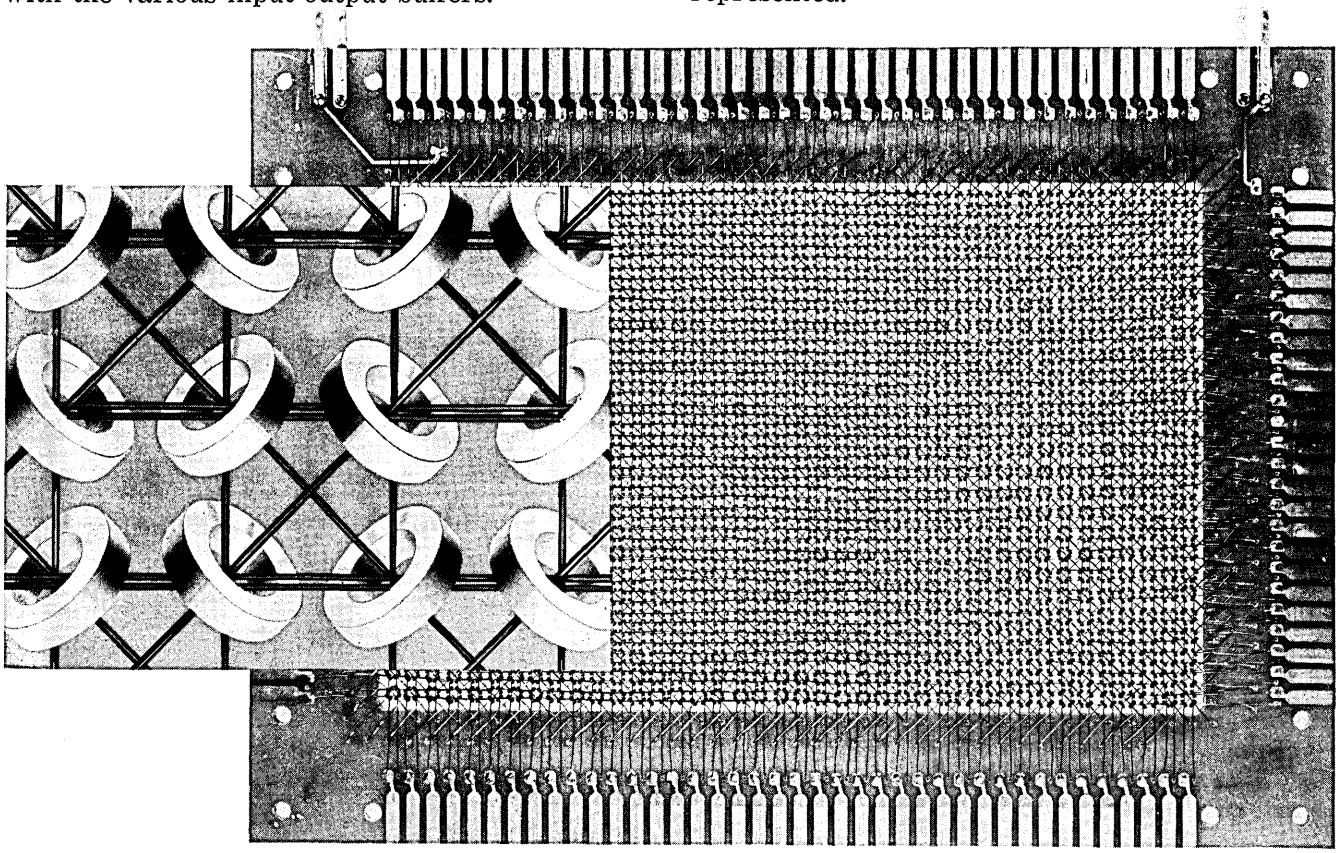


Figure 4-6. Core Memory Plane

Although core storage is housed separately, it functions as an integral part of the Central Processor. Information flows directly between core memory, drum memory, and the arithmetic and control units in the Processor. Therefore, the core memory may contain program instructions and data to be operated upon by the program.

Core memory cycle time for the 11-digit word is 17 microseconds. Information recorded in a word of core is always available until new data is transferred to that word or until power to the system is turned off.

Storage Areas

The first 1,000 words of core storage may be used for storing instructions or data without restriction. This area functions in the same manner as the main storage area on the magnetic drum.

The last 280 words of core memory may also contain instructions or data, but with the following restrictions: (1) instructions contained in this area can not be index register modified; (2) instructions which can cause a $c+1$ condition (arithmetic overflow and abnormal operation of peripherals) should not be placed in this area: (3) data contained in this area cannot be involved in multi-word transfer instructions.

Six of these 280 words of core storage are index registers (IR).

Addressing

Words in core storage are addressed by alphanumeric addresses. These addresses are listed below. Those memory locations marked IR_4 through IR_9 are completely available to the programmer at all times should he desire to use them for temporary storage.

WORDS	ADDRESSES
1–1000	B000–B999
1001–1100	B00A–B99A
1101–1200	B00F–B99F
1201–1210	B0AC–B9AC
1211–1220	B0AG–B9AG
1221–1230	B0AH–B9AH
1231–1240	B0FB–B9FB
1241–1250	B0FC–B9FC
1251–1260	B0FG–B9FG
1261–1270	B0FH–B9FH
1271	B0AB
1272	B1AB
1273	B2AB (IR_4)
1274	B3AB (IR_5)
1275	B4AB
1276	B5AB (IR_6)
1277	B6AB (IR_7)
1278	B7AB (IR_8)
1279	B8AB (IR_9)
1280	B9AB

5. Programming Features

STORED PROGRAM

The UNIVAC Solid-State II System is completely internally programmed. Program instructions and data to be processed are stored in either core or drum memory. The portion of the program stored on the drum is not normally stored in sequential memory locations. Since the instruction word format of the Solid-State II System allows both an operand and the next instruction address to be specified, instructions may be arranged in a pattern in memory which effectively minimizes execution time. Portions of the program stored in core are stored in any core location since there is no latency to core (each word is equally accessible).

DATA FLOW

The flow of information between the Central Processor and its on-line peripheral units is initiated and controlled by program instructions. Information entering the system from a peripheral unit is first placed in an input buffer on the magnetic drum. Data originating with the magnetic tape or RANDEX mass storage systems may be transferred from buffer storage to either drum or core memory where it is ready for processing. Punched-card input data is always transferred from the buffer to drum memory. It may be transferred from drum to core as required. Transfers between core and drum memory are greatly simplified by multi-word transfer instructions. Using these instructions, data groups of one to 200 words may be transferred. All input unit-to-buffer and buffer-to-memory data transfers are controlled by program instructions.

Information to be punched in cards as output by the Card Read-Punch Unit or printed by the High-Speed Printer is first placed in drum memory. From there it enters the buffer and is sent to the output unit. Output information to be placed on magnetic tape or a RANDEX drum file unit may enter the buffer from either drum or core memory before being recorded as output data. Individual program instructions initiate memory-to-buffer and buffer-to-output unit data flow.

The synchronizers for the RANDEX and tape systems regulate the flow of data between these systems and memory.

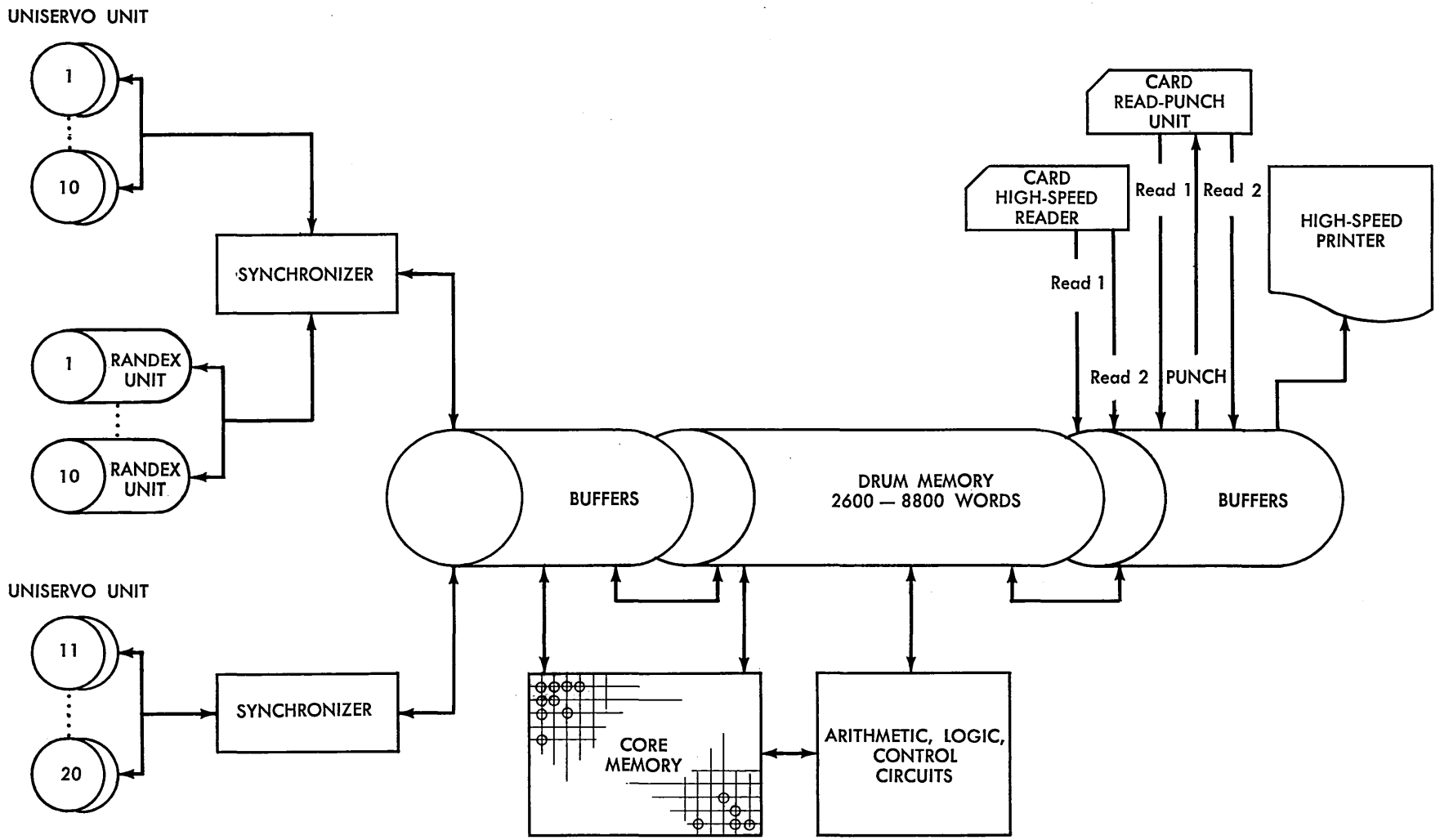


Figure 5-1. Schematic, Data Flow

INSTRUCTION WORD FORMAT

There are four distinct parts of Solid-State II instruction words:

1. The operation code (OP)
2. The m portion
3. The c portion
4. The sign

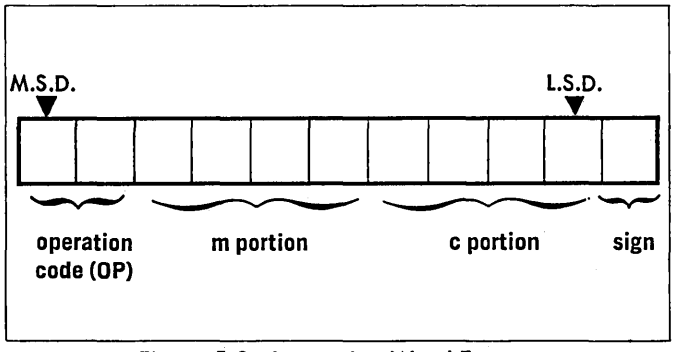


Figure 5-2. Instruction Word Format

The OP portion of the word specifies the *operation code,* or operator, and consists of two digits.

The *m* portion normally specifies the *memory location* (drum or core) of the data word to be operated upon. Four digits are used to indicate the *m* portion of the word.

The *c* portion normally specifies the *memory location* (drum or core) where the next instruction to be performed is to be found. Four digits make up the *c* portion.

The leftmost digit of the word is the most significant digit (*MSD*) and the rightmost digit — exclusive of the sign — is the least significant digit (*LSD*).

CONTROL REGISTERS

The control unit of the Processor contains two control registers: the static register and register *C*. These registers direct the execution of instructions and are not directly addressed.

Register C

Register *C*, the control register, receives each instruction to be executed and holds it during the period of execution. The instruction word is first sent to register *C*. The Processor then accesses the *m* and *c* locations indicated in the instruction word. When the next instruction is obtained from memory, it too is transferred to register *C*, and accessing the *m* and *c* addresses is repeated.

Static Register

The static register holds the two digits of the instruction operation code. Setting up the operation code in the static register, and the instruction word in register *C* is referred to as *staticizing the instruction.* After the instruction is staticized, it is sent to an instruction decoder, then through a function encoder, and emerges in the form of function signals which cause the instruction to be executed.

The static register and register *C* are thus directly tied in with the arithmetic and storage units of the Processor.

INSTRUCTION CYCLE

A three- or four-step cycle (with an additional step if index registers are used) is associated with each instruction depending upon whether an operand is required from memory. If setting-up the instruction is considered the starting point, the instruction cycle is:

(1)	(2)	(3)	(4)	(5)
Staticize the Instruction	Index Register Modification (if any)	Search for Operand	Execute the Instruction	Search for the Next Instruction

(1) STATICIZE THE INSTRUCTION

The instruction located by the previous search (5) is transferred from the memory to the static register and register *C*. This step requires one word time, which is 0.017 milliseconds.

(2) INDEX REGISTER MODIFICATION

When modification is indicated, the *m* address of the instruction is altered by the index register specified. The step requires one word time.

(3) SEARCH FOR THE OPERAND

If the operand specified is located in drum memory or in an arithmetic register (*A*, *X*, or *L*) a minimum of one word time is required to determine that location. If the next instruction is located in core memory, in most cases this cycle may be eliminated. (See Search Time Chart.)

(4) EXECUTE THE INSTRUCTION

The operation indicated in the instruction is performed. The time required depends upon the type of operation indicated.

(5) SEARCH FOR THE NEXT INSTRUCTION

If the next instruction is located in drum memory or in an arithmetic register (*A*, *X*, or *L*) a minimum of one word time is required to determine that location. In most cases, if the next instruction is located in core memory this cycle may be eliminated. (See Search Time Chart.)

INDEX REGISTERS

The UNIVAC Solid-State II System is equipped with nine index registers. The usual purpose of these index registers is to modify the operand address of an instruction, so that the same instruction can be used repetitively on different sets of data. Each of the nine index registers may contain four decimal digits, unsigned. The contents of an index register may be incremented or decremented through complementary addition and new values may be inserted at any time. Whenever an index register is incremented, the new sum present in that index register is automatically transferred to register *A* to facilitate testing. Any instruction (except 26 and 23) in which the *m* address is a discrete memory location may be modified with index registers (Figure 5-3). Since the modification takes place in register *C*, the original instruction in memory and the index register itself remains unchanged.

Index Register Addressing

Index registers 4 through 9 are addressed through the following bit configurations within the sign digit:

BITS	5	4	2	1	IR
	0	0	1	0	4
	0	0	1	1	5
	1	0	0	0	6
	1	0	0	1	7
	1	0	1	0	8
	1	0	1	1	9

Note: Designations for IR_1, IR_2, IR_3 have *not* changed.

The 4-bit of the sign digit is not used for indexing purposes.

Let contents of IR=B041*

In order to increment to level 046, the instruction should read:

07 B005* CCCC

In order to decrement to level 036 the instruction should read:

07 B995* CCCC

**Whenever a* B *appears as the most significant digit of the* m *portion of the 07 instruction, the computer will necessarily force a* B *into the most significant position of the index register.*

Figure 5-3. Examples of Modification with Index Registers

Modification Timing

Whenever an instruction is to be modified by any one of the index registers, an additional instruction phase is executed. This phase consists of adding the contents of the specified index register to the *m* address of the instruction before the instruction is executed.

When an instruction is to be executed it is transferred from memory and staticized. There it is examined to determine if modification is to take place. If modification is not indicated, the search for the operand located at the *m* address is begun. If modification is required, the contents of the specified index register are added to the *m* address in register *C* and the 4-digit result is replaced in the *m* portion of the instruction in register *C* before the search for the operand is begun. This step requires an additional word time. The additional instruction phase then, occurs after the instruction is staticized in register *C*, and before the search for the operand is begun.

Band Modification Feature (Drum)

A band modification feature enables modification with index register to be restricted, with drum storage addresses, to the same band in which it was initiated. If, during modification, the *m* address is altered to refer to another band, the computer will cause a return to the corresponding location in the original band. This band modification occurs when at least two of the following conditions are present:

1. The hundreds digit of the contents of the index register is odd.
2. The hundreds digit of the instruction's *m* address is odd.

3. During modification a carry occurs from the tens digit to the hundreds digit.

Band Modification Feature (Core)

The first 1,000 words of core memory, B000 through B999, may be considered a band of core, modulo 1000. That is, locations B998, B999, B000, and B001 are adjacent to the same extent that drum locations 1398, 1399, 1200, and 1201 are adjacent. All indexing operations performed upon base core addresses then are modulo 1000 within core. The additional 280 words of core memory may not be index register modified (nor may they be transferred as part of a multi-word group). When a core address is indexed, the index register should contain the non-numeric *B* in the most significant digit of the incrementation.

The figure below represents the condition which, in combination, cause band modification to be effected:

CONDITION

1	1	X	1	1	Index register
2	M	X	M	M	Instruction m address
3	S	S	S	S	Sum (modified m address)

KEY

X = odd digit
M = digit of the m portion
I = digit of the index register
S = digit of the sum of the index register and the m portion
⌣ = carry

Note: When the four digits of the *m* address are added to those of the index register, any carry from the most significant digit position is lost.

MSD

M	M	M	M	Digits of the m portion
1	1	1	1	Index register
⌣S	S	S	S	Sum (modified address)

This carry is lost.

ADDRESSABILITY OF REGISTERS

As a result of their addressability, register *A*, *X*, or *L* may be the *m* address of many, and the *c* address of all instructions.

The sole restriction is that they cannot be used in the *m* portion of the 50, 60, and 65 orders, nor in the *m* portion of the instructions which do not address a one-word storage location. The arithmetic registers are addressed by non-numeric digits in the least significant digit of *c* or *m*.

	LSD of m or c
BITS	DIGIT
rA = 0101	1/4
rX = 0111	3/4
rL = 0110	2/4

RANDEX ADDRESSING

Each block of information stored on a RANDEX drum has a unique seven-digit address. To access a block of information on one of the RANDEX units, a special format of the ten-digit instruction word is used. The seven least significant (rightmost) digits of the instruction word are used for the RANDEX address, and, as in the normal instruction word format, digit positions 1 and 2 (leftmost) hold the operation code. (The operation code is a coded command to read, write, or the like.) The extra digit position (position 3) in a RANDEX instruction word is disregarded by the computer. For convenience in programming, the position is normally filled in with a zero. The RANDEX instruction word format is described below:

RANDEX ADDRESS

1	2	3	4	5	6	7	8	9	10	
OP		0	0/9		0/3	00/99		00/19	0/5	ADDRESS CODE

DIGIT POSITION

DIGIT POSITIONS

1 and 2 — Operation Code
3 — Not used
4 — Number of RANDEX Unit
5 — Number of Drum Half
6 and 7 — Number of Sector
8 and 9 — Number of Track
10 — Number of Block

DUAL SYNCHRONIZERS

The use of dual synchronizers is optional with the Solid-State II System, providing for as many as twenty tape handling units. One synchronizer also governs RANDEX operations. If dual synchronizers are selected, the second will not accept RANDEX instructions. Selection between the two synchronizers is determined by a 0 or a 1 in the 4-bit position of the sign of the instruction word. A 0 in this position specifies the first synchronizer, and a 1 specifies the second. All RANDEX instruction words must have a 0 in the 4-bit position of the

sign. The use of dual synchronizers provides the ability to perform simultaneous read-write operations. A second tape input-output buffer is associated with the second synchronizer and all tape-handing instructions will use the 4-bit of their sign positions to specify whether they affect the first or second synchronizer, 4-bit off or on.

ALPHA-NUMERIC COMPARISONS

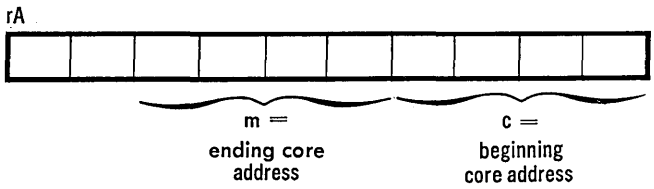
Added instructions allow the Solid-State II System to perform alpha-numeric comparisons. For this purpose, register *X* is divided into two halves, each half consisting of 2 subregisters. Bit positions 1 and 2 are the lower half of r*X* (subregisters 1 and 2), while bit positions 4 and 5 are the upper half (subregisters 3 and 4). In the comparison, the two numeric words are transferred to r*A* and r*L*. The zone word of r*A* goes to subregisters 1 and 2 of r*X*, while the zone word for r*L* goes to subregister 3 and 4 of r*X*.

CORE ADDRESSES

Any instruction except 11, 46, 96 and 81 may call for a core location in the *m* portion of the instruction. Core locations may be specified for any *c* address.

MULTI-WORD TRANSFERS

The UNIVAC Solid-State II System is capable of transferring from 1 to 200 consecutive words either from drum memory to core memory or vice versa in one instruction. The transfer instruction contains the first drum address in the *m* portion. The programmer would have previously loaded register *A* with the beginning and ending core memory addresses in the form:



The time required to effect this powerful transfer instruction is 4 word times (68 microseconds). plus 1 word time for each word transferred.

The last digit, the sign, is, in a data word, either plus or minus. The value of the sign digit is then either 0 (plus) or 1 (minus). In an instruction word, the sign serves other purposes, such as:

- **Identifying index registers.**
- **Identifying instructions dealing with alpha-numeric comparisons.**
- **Specifying the proper input-output device in a dual synchronizer system.**

INSTRUCTION LIST

ARITHMETIC

70	m	c	Add
75	m	c	Subtract
85	m	c	Multiply
55	m	c	Divide

TRANSFER

25	m	c	Memory to Register A.
60	m	c	Register A to Memory.
05	m	c	Memory to Register X.
65	m	c	Register X to Memory.
30	m	c	Memory to Register L.
50	m	c	Register L to Memory.
77	—	c	Register A to Register L.
26	m	c	Zeros to Register A.
31	m	c	Zeros to Register L.
06	m	c	Zeros to Register X.
36	m	—	Zeros to Register A, sign unchanged.
86	m	—	Zeros to Register A, Register X.
23	m	—	Register C to Register A.
90	m	c	MSD of Memory to Sign of Register L.
F0	m	c	Sign of Memory to MSD of Register A.
B8	m	c	1 — 200 words Core Memory to Drum Memory.
B0	m	c	1 — 200 words Drum Memory to Core Memory.
05*	m	c	Bits 1 and 2 of Memory to bits 3 and 4 of Register X.

TRANSLATE

12	—	c	Card Code to Computer Code.
17	—	c	Computer Code to Card Code.
C3	m	c	XS-3 Code to Computer Code.
C1	m	c	Computer Code to XS-3 Code.

COMPARE

82	=	≠	Register A with Register L for Equality.
87	>	≤	Register A with Register L for Magnitude.

ALPHA-NUMERIC COMPARE

82*	=	≠	Register A (plus register X 1-2 bits) with Register L (plus register X 4-5 bits) for Equality.
87*	>	≤	Register A (plus register X 1-2 bits) with Register L (plus register X 4-5 bits) for Magnitude.

EDIT

20	m	c	Superimpose Memory on Register A.
35	m	c	Erase m from Register A.
32	m	c	Shift Register A and X right.
37	m	c	Shift Register A left.
62	—	c	Zero suppress Register A.

*Bit in Sign bit position 4.

CONTROL

00	m	—	Skip to m address.
67	—	c	Stop.

INDEX REGISTER

02	m	c	Load Index Register.
07	m	c	Increment and Unload Index Register.

CARD READ-PUNCH UNIT

81	m	c	Memory to Buffer Transfer. Card Cycle.
46	m	c	Buffer to Memory Transfer.
22	m	c	Buffer-loaded Test.
57	m	c	Stacker Select.

HIGH-SPEED CARD READER

72	m	c	Card Cycle.
96	m	c	Buffer to Memory Transfer.
42	m	c	Buffer-loaded Test.
47	m	c	Stacker Select.

HIGH-SPEED PRINTER

11	m	c	Advance Paper and Print.
16	m	c	Advance Paper.
27	m	c	Printer-operating Test.

UNISERVO MAGNETIC TAPE SYSTEM

G2	m	c	Tape to Buffer Transfer (Read).
H2	m	c	Buffer to Tape Transfer (Write).
F6	m	c	Buffer to Memory Transfer.
C6	m	c	Memory to Buffer Transfer.
C7	m	c	Buffer-loaded Test.
C2	m	c	UNISERVO-busy Test.
F2	m	c	Rewind Tape.

RANDEX MASS STORAGE SYSTEM

40	m	c	Memory to Synchronizer Instruction Register Transfer.
18	m	c	Position Head.
92	m	c	Test Boom.
43	m	c	Head Position Sample.
28	m	c	Write.
38	m	c	Read.
48	m	c	Write and Check.
58	m	c	Search Write.
68	m	c	Search Read.
F6	m	c	Buffer to Memory Transfer.
C6	m	c	Memory to Buffer Transfer.
C7	m	c	Buffer-loaded Test.
C2	m	c	Synchronizer-busy Test.

SEARCH TIME CHART

Sign Digit	Op Code	m Address can be Core	Search for m Eliminated if in Core	Search for c Eliminated if in Core	Search for m Eliminated (if in Core) IR Modification is Performed
	70	YES	YES	YES	YES
	75	YES	YES	YES	YES
	85	YES	YES		YES
	55	YES	YES	YES	YES
	25	YES	YES	YES	YES
	60	YES			YES
	05	YES	YES	YES	YES
	65	YES			YES
4	65				
	30	YES	YES	YES	YES
	50	YES			YES
	77			YES	
	26			YES*	
	31			YES*	
	06			YES*	
4	06				
	36			YES*	
	86			YES*	
	23				
	12			YES	
	17			YES	
	C1			YES	
	C3			YES	
	82				
	87				
4	82				
4	87				
	20	YES	YES	YES	YES
	35	YES	YES	YES	YES
	32				
	37				
	62			YES	
	00			YES	
	67				
	02				
	07				
	81				
	46				
	22				
	57			YES	
	72				
	96				
	42				
	11				
	16				
	27				
	F2				
	G2				
	H2				
	90	YES	YES	YES	YES
	B0	YES			
	B8	YES			
	F0	YES	YES	YES	YES
	05	YES	YES	YES	YES
	40	YES	YES	YES	YES
	92				
	43			YES	
	18				
	28				
	38				
	48				
	58				
	68				
	F6	YES			
	C6	YES			
	C7				
	C2				

*Address of next instruction must be placed in *m* and *c* portions of instruction word.

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