SPERRY RAND

UNIVAC

TYPE 1219B DIGITAL DATA COMPUTER TECHNICAL MANUAL VOLUME I

TECHNICAL MANUAL

for

TYPE 1219B
DIGITAL DATA COMPUTER
VOLUME 1
SECTIONS 1-8

PX 4682-1-2

AUGUST 1968
July 1972 (Change 3)

UNIVAC
DEFENSE SYSTEMS DIVISION
St. Paul, Minnesota

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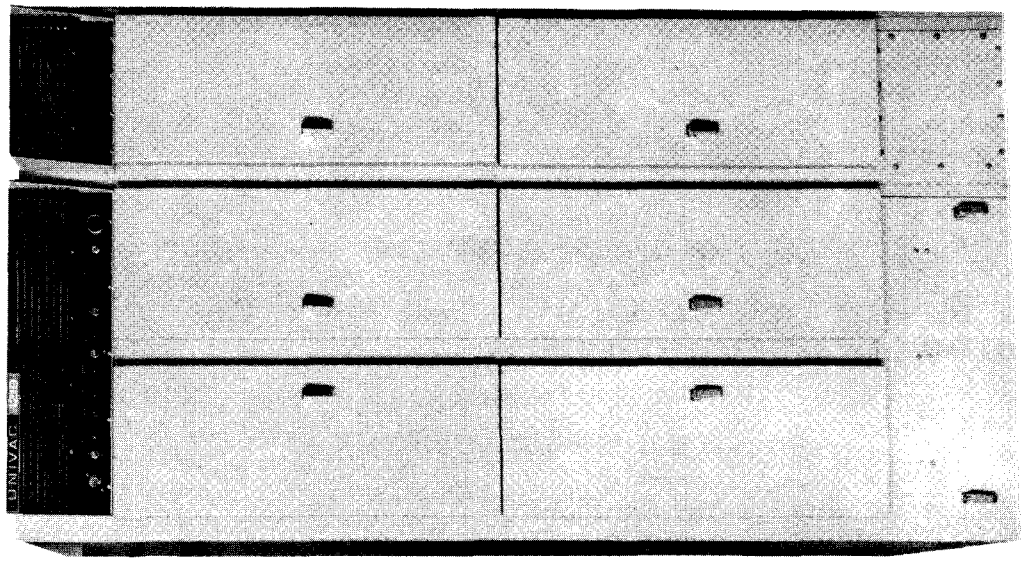

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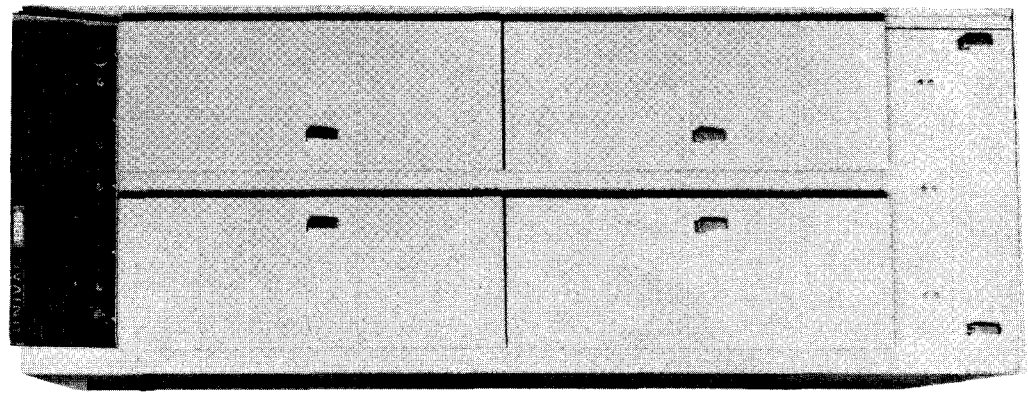


4-DRAWER UNIT

Figure 1-1. UNIVAC Type 1219B Digital Data Computer

SECTION 1

GENERAL DESCRIPTION

1-1. INTRODUCTION.

a. SCOPE AND PURPOSE. - This instruction manual describes the UNIVAC Type 1219B Digital Data Computer (figure 1-1), and provides information required for maintenance and operation.

b. ORGANIZATION. - The instruction manual is divided into nine sections to facilitate rapid reference to the information and provide a logical grouping of related facts.

(1) SECTION 1, GENERAL DESCRIPTION. - Section 1 contains an introduction to the manual, a brief description of the UNIVAC Type 1219B Digital Data Computer, and a basic explanation of functions it performs. Included in this section are illustrations to aid in mechanical and electrical identification of assemblies, subassemblies, and parts; also, several tabular listings of the characteristics of the unit.

(2) SECTION 2, INSTALLATION. - Section 2 contains information necessary for the preparation and installation of the equipment for normal operation. Included are outline drawings of the unit to illustrate space requirements and illustrations to aid in locating mechanical and electrical connections.

(3) SECTION 3, OPERATOR'S SECTION. - Section 3 contains a description of the unit operating controls and indicators. It also contains instructions required for manual operation of the unit including read, write, and load routines. A repertoire of instructions is included with a description of each operation performed by the coded instruction word.

(4) SECTION 4, THEORY OF OPERATION. - Section 4 contains a detailed description of the equipment operation with particular emphasis on logical rather than electrical functions. The description references the functional schematics contained in section 9 and, in some cases, in-text simplified illustrations. A description of each printed circuit card used for logic functions is contained at the end of this section.

(5) SECTION 5, TROUBLESHOOTING. - Section 5 contains the recommended procedures to isolate and correct equipment malfunctions. Included are suggested schedules for performing maintenance programming, such as, preventive maintenance routines, tests to be performed in conjunction with maintenance programming, and a logical explanation of the error conditions which may occur during performance of these tests.

(6) SECTION 6, SERVICE AND REPAIR. - Section 6 contains a tabular listing of the maintenance equipment recommended to aid and assist in the maintenance and repair of the unit, assemblies, subassemblies, and component replacement and repair; and adjustment procedures to insure optimum equipment operation.

(7) SECTION 7, PARTS LIST. - Section 7 contains a tabular listing of assemblies and repairable electronic parts contained in the unit. Included in this listing are part numbers, reference designations, and vendors' code numbers. The reference designations contained in the parts list coincide with designations marked on the equipment, drawings, and diagrams.

(8) SECTION 8, SYMBOLOGY. - Section 8 contains a description of circuit card symbology and operation which is intended to serve primarily as a troubleshooting and maintenance guide.

(9) SECTION 9, FUNCTIONAL SCHEMATICS. - Section 9 contains logic diagrams and other drawings necessary for the performance of required maintenance and for a complete comprehensive understanding of the equipment operation. This section also contains a symbology explanation, chassis maps for locating printed circuit cards, and power distribution drawings to facilitate power malfunction isolation.

1-2. EQUIPMENT ILLUSTRATION.

Figure 1-1 illustrates the UNIVAC Type 1219B Digital Data Computer with the protective covers or doors closed. The doors cover control panels with the exception of the power control panel at the top of the unit. Figures 1-2 and 1-3 illustrate the computer (with doors open to expose the control panels) with available options. The information contained within this manual refers to Univac part number 7049747.

1-3. FUNCTIONAL DESCRIPTION.

a. GENERAL. - The UNIVAC Type 1219B Digital Data Computer (hereinafter referred to as the computer) is a general purpose, stored program, real-time computer. The computer is capable of solving any problem normally solved by standard mathematical techniques and also performs most data processing functions. Options available with the computer are listed in table 1-1. Operational and functional characteristics are listed in tables 1-2 and 1-3, respectively. General characteristics are listed in table 1-4.

Computer logic is divided into four functionally definable sections: control, input/output, arithmetic, and memory (figure 1-4). These four sections are described in paragraphs 1-3h, i, j, and k.

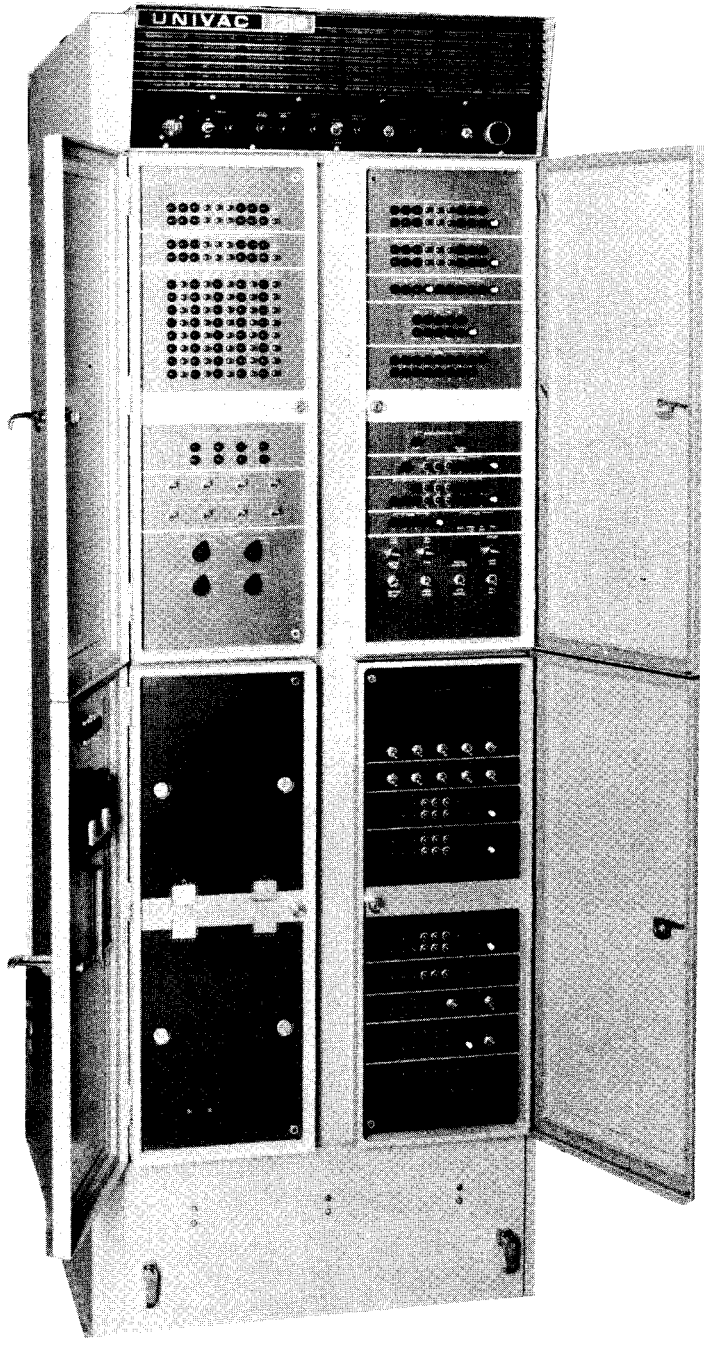
b. INSTRUCTION REPERTOIRE. - The computer has a repertoire of 102 flexible, single-address instructions with provisions for address or operand modification by eight index registers. A list of instructions is contained in table 1-5.

c. INSTRUCTION FORMAT. - The instructions are classified as either format I or format II instructions.

Format I instructions (figure 1-5a) contain a 6-bit function designator and a 12-bit operand. The operand specifies either a constant or part of a memory address to be used in the performance of the instructions.

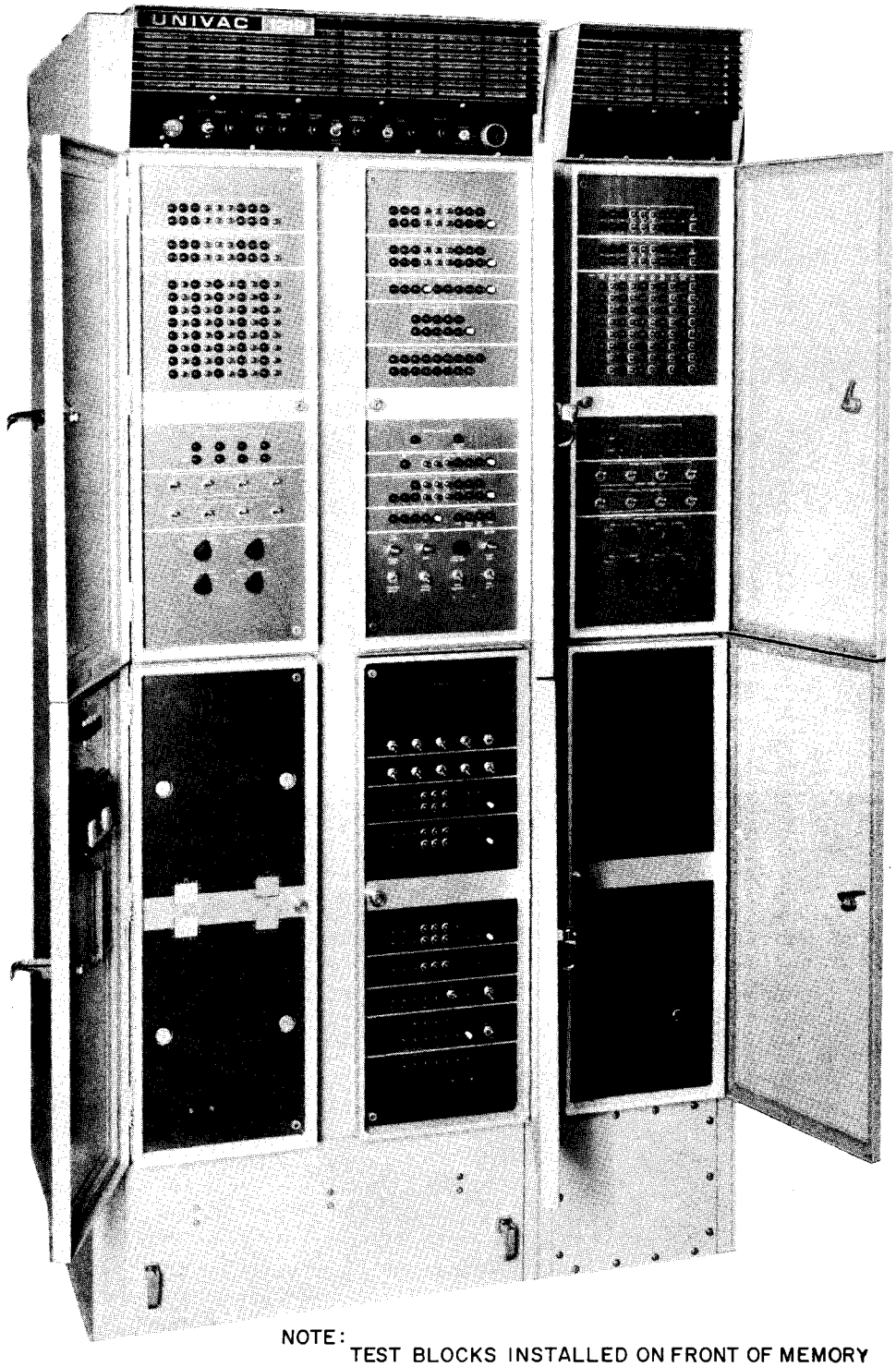
Format II instructions (figure 1-5b) contain a 6-bit function designator and a 6-bit minor function code. The function designator is always an octal 50 (to specify a format 2 instruction). The minor function code is used to identify the instruction to be performed. The low-order, 6-bit designator of the instruction word identifies a count during a shift operation, a channel number for input or output functions, or a switch setting for stop or skip instructions.

d. PROGRAM RECOVERY. - The computer has an automatic program recovery capability. In the event of a computer fault, a programmed instruction is referenced to automatically load a new program into the computer memory. Also, this procedure (utilizing a nondestructive read-out bootstrap memory) is used for loading initial programs.



NOTE: TEST BLOCKS INSTALLED ON FRONT OF MEMORY DRAWER ONLY ON SN 14-48.

Figure 1-2. Computer With Maximum of Eight Input/Output Channels



NOTE:
TEST BLOCKS INSTALLED ON FRONT OF MEMORY DRAWER ONLY ON SN 14-48.

Figure 1-3. Computer With Maximum of 16 Input/Output Channels

TABLE 1-1. COMPUTER OPTIONS AVAILABLE.

ITEM	OPTION
Input/Output Channels	4, 8, 12, or 16 channels
Memory Capacity	16, 384; 32, 768; 49, 152, or 65, 536 words
Control Memory Capacity	128 or 256 words
Interface Voltage Level	-3.0 or -15.0 vdc.
Data Transfer Rate	

INTERFACE TYPE (VDC)	CHANNEL CONFIGURATION	MAXIMUM DATA TRANSFER RATE (WORDS PER SECOND)
-3	Single	166,667 18-bit words
-3	Dual 1 odd and 1 even channel	333,334 18-bit words (166,667 36-bit words)
-3	Multi 1 or more odd and 1 or more even channel(s)	500,000 18-bit words (max. main memory rate)
-15	Single	41,667 18-bit words
-15	Dual 1 odd and 1 even channel	83,334 18-bit words (41,667 36-bit words)
-15	Multi 2 or more odd and 2 or more even channels	166,667 18-bit words (max. -15-volt interface rate)

e. REMOTE CONTROL. - The computer has provisions for remote control and monitoring. A remote control console (figure 1-6), can be connected to jack A12J17. A front panel indicator shows whether the computer is in local control or remote control. The indicators and alarm on the remote control console are functional when the computer is in local or remote mode. The switches on the remote control console are functional only when the computer is in remote mode.

f. REAL TIME CLOCK. - An internal real-time clock increments the contents of address 000015 at a rate of 1024 cycles (increments) per second. The computer is capable of accepting real-time clock interrupts at frequencies up to 20 kilocycles per second. The real-time clock enable is controlled by a front panel switch.

g. INTERRUPTS. - When the contents of address 000015 overflow (777777 to 000000), the program is interrupted by the overflow interrupt and the next instruction is taken from address 000013.

A real-time clock monitor interrupt is initiated by storing a desired time count in address 000014 (real-time clock monitor), and enabling the real-time clock monitor

via the 50:14 instruction. When the count in address 000015 equals the count stored in address 000014, the computer program is interrupted by the real-time clock, and the next monitor interrupt instruction is taken from address 000012 (monitor interrupt). Also, the real-time clock monitor is disabled.

The computer can accept an external synchronizing interrupt through jack A12J18. Whenever the external synchronizing signal occurs, the computer interrupts program operation and performs the instruction located at address 000016 (synchronizing interrupt entrance address). The external synchronizing interrupt is enabled and disabled by a front panel switch. This interrupt can occur at frequencies up to 20 kilocycles per second.

The computer is available with the options listed in table 1-1 and also is available with or without the top stabilization bracket.

h. CONTROL SECTION. - The control section provides the timing, instruction translation, and operational sequencing required for performance under either program control or manual operation.

Under program control, the computer performs the instructions of an entire program at a high rate of speed, stopping only where programmed.

For manual operation, two control panels contain the switches and indicators by which the computer may be sequenced through the functions of an instruction, allowing each operation and its results to be visually displayed and examined. These two are control panel 1 located on drawer A2, and control panel 2 located on drawer A4.

The control section of the computer (figure 1-9) consists of five logically definable areas: console control, timing, program translation and control, registers, and special circuits.

(1) CONSOLE CONTROL. - The console control area contains the controls, indicators, and logic circuitry required by an operator for program control. The switches and indicators used for other logic functions are not included in this section. Switches in the console control area are provided for master clearing the computer, starting and stopping operations, operational mode selection, and controlling programmed stops and skips.

The start-stop logic consists of the logic necessary to start, stop, and master clear the computer, and to control the application of phase pulses for the several modes of operation. This logic is dependent upon the switch settings as defined in tables 3-2 and 3-4, and various programmed stops.

The mode selection logic determines the individual mode of operation to be performed by the computer. The four modes are: Load, Phase Step, Operation Step, and Run. The mode of operation is selected by a switch on control panel 1 (A2).

The program skip logic functions during the execution of the several skip instructions to effect the skip procedure of the instruction if the necessary conditions have been met. A programmed skip is an instruction which allows the computer to omit the next sequential instruction, providing the conditions exist indicated by the skip instruction.

The program stop logic detects programmed stops and compares these instructions with the switch settings which effect the stops. A programmed stop is an instruction which causes the computer to cease operation until manual intervention again returns it to a Run status. There are five switch-controlled stops and one unconditional stop.

(2) TIMING CIRCUITS. - Timing commands within the computer are a function of the master clock circuit and the main timing cycle circuits. The master clock circuit produces four basic timing pulses used to establish the operation of the main timing cycle circuits and provides command enable pulses through gating by the main timing chain.

The master clock generates and distributes four basic timing pulses for each 500 nanoseconds of operation. These four pulses, called phases one through four, constitute one complete clock cycle. Four clock cycles represent one computer memory cycle. Figure 1-7 shows the relationship between the master clock phase pulse outputs and the outputs from the main timing chain flip-flops.

The main timing cycle circuits supply enables to the computer logic for operation of command timing sequences. Timing pulses developed by command timing sequences are numerically identified by the clock cycle and phase with which they are associated. The only exception to this rule is T52 used only during complement A and complement AL instructions. In the term T34, the 3 represents the third clock cycle, the 4 indicates that phase four is the last usable phase occurring during that timing pulse. Phase pulses are not ANDed with the first half (shaded area, figure 1-7) of the timing pulses because of the instability of the pulse during this time. The second half of the pulse is used to insure the proper voltage level and stability of the signal when used for gating purposes.

Each phase pulse duration time is approximately 100 nanoseconds; the clock cycle is 500 nanoseconds; and the computer memory cycle is 2 microseconds.

TABLE 1-2. OPERATIONAL CHARACTERISTICS

ITEM	INFORMATION	
WORD LENGTH	18 bits (36 bits optional for I/O)	
CORE MEMORY STORAGE	16K, 32K, 49K, or 65K words	
CONTROL MEMORY STORAGE	128 or 256 words	
BOOTSTRAP MEMORY STORAGE	32 nondestructible words	
CYCLE TIME		
Core Memory	2.0 usec	
Control Memory	0.5 usec	
Bootstrap Memory	2.0 usec	
SIGNAL LEVEL DATA		
Computer Signal Level	MAIN MEMORY LOW = 0.0 VDC "0" HIGH = +3 VDC "1" CONTROL ARITHMETIC LOW = -4.5 VDC "1" HIGH = 0.0 VDC "0"	
I/O Signal Level	FAST INTERFACE HIGH = 0.0 VDC = "1" LOW = -3.0 VDC = "0"	SLOW INTERFACE HIGH = 0.0 VDC = "1" LOW = -15.0 VDC = "0"

TABLE 1-3. FUNCTIONAL CHARACTERISTICS

ITEM	DESCRIPTION
WORD LENGTH	Normal word length is 18 bits. Dual channel capability allows 36-bit word transfers on any consecutive even-odd pair of I/O channels for compatability with larger systems.
ARITHMETIC	Parallel, subtractive, one's complement in either single length (18 bits) or double length (36 bits).
MEMORY SIZE	16, 384, 32, 768, 49, 152 or 65, 536 18-bit words.
CONTROL MEMORY SIZE	128 18-bit words, expandable to 256 words for control word storage
BOOTSTRAP MEMORY SIZE	32 permanently wired, nondestructible readout words for paper tape or magnetic tape program load and automatic program recovery. Teletypewriter load bootstrap available upon special request.
MEMORY ACCESS TIME	Main memory access time is a maximum of 750 nanoseconds. Control and bootstrap memory access time is a maximum of 300 nanoseconds.
MEMORY CYCLE TIME	Main and bootstrap memory cycle time is 2.0 microseconds. Control memory cycle time is 500 nanoseconds.
INSTRUCTION REPERTOIRE	102 single-address flexible instructions with provisions for address and operand modification by eight index registers.
I/O CHANNELS	Optional selection of 8, 12, or 16 input and output channels for bidirectional communication with peripheral devices. Choice of fast or slow interface.
TRANSFER MODE	All input and output transfers are parallel.
INPUT/OUTPUT CONTROL	Inputs and outputs are buffer controlled without program monitor. Control by ESI (externally specified index) or by ESA (externally specified address) from peripheral devices.
REAL-TIME OPERATION INTERNAL OR EXTERNAL SYNC	Internal real-time clock or external sync connection provides synchronizing interrupt and makes possible automatic inter-computer time-out fault detection.
REAL-TIME CLOCK	1024 cycles per second is standard. Other frequencies are available upon request.
MEMORY PROTECT	Automatic stop without loss of stored information when a voltage fault occurs.

TABLE 1-4. GENERAL CHARACTERISTICS

ITEM	4-DRAWER UNIT	6-DRAWER UNIT
WEIGHT (Maximum)	1050 pounds	1460 pounds
OVERALL DIMENSIONS (Maximum)		
Height	72 inches	72 inches
Width	26 inches	38 inches
Depth	29 inches	29 inches
CUBIC CONTENT	54,288 cubic inches	79,344 cubic inches
CLEARANCE REQUIREMENTS	Top: 12 inches Sides: 8 inches each Front: 39 inches Rear: 10 inches	
REQUIRED ENVIRONMENTAL CONDITIONS		
OPERATING TEMPERATURE RANGE	32°F (0°C) to 122°F (50°C)	
OVERTEMPERATURE WARNING	115°F (46°C)	
OVERTEMPERATURE SHUTDOWN	140°F (60°C)	
HUMIDITY, MAXIMUM RELATIVE	95%	
HEAT DISSIPATION	Approx. 5000 BTU/hours for 32K memory and 8 I/O channels	
AC POWER REQUIREMENTS		
LOGIC POWER	115 VAC ±1%, 400 CPS ±5%, 3-Phase, 3-wire	
BLOWER POWER	115 VAC ±10%, 400 CPS ±5%, 3-Phase, 3-wire	

AC POWER REQUIREMENTS PER OPTION

COMPUTER CONFIGURATIONS MEMORY SIZE	I/O CHANNELS	MAX. INPUT POWER REQUIRED AT 115 VOLTS (WATTS)
8K	4	1530
16K	8	1640
32K	8	1860
32K	16	2080
65K	16	2510

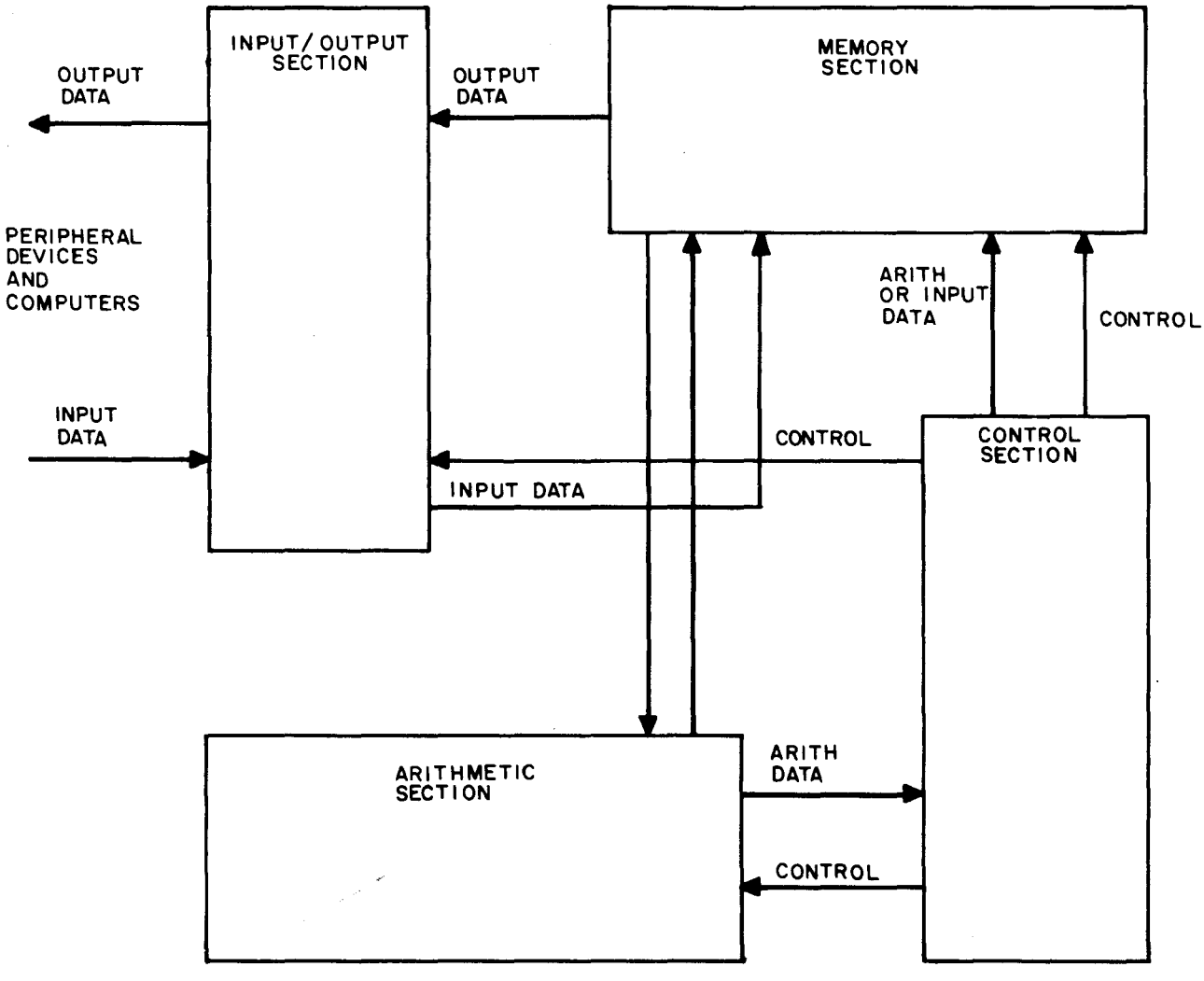


Figure 1-4. Computer Simplified Block Diagram

TABLE 1-5. LIST OF INSTRUCTIONS

FUNCTION CODE	OPERATION	EXECUTION TIME (MICROSECONDS)
00	Illegal code	2
01	Illegal code	2
02-03*	Compare AL	4
04-05*	Selective substitute	4
06-07*	Compare with mask	4
10-11*	Enter AU	4
12-13*	Enter AL	4
14-15*	Add AL	4
16-17*	Subtract AL	4
20-21*	Add A	6
22-23*	Subtract A	6
24-25*	Multiply AL	14
26-27*	Divide A	14
30-31*	Indirect return jump	6
32-33*	Enter B	4
34-35*	Direct jump	2
36-37*	Enter B with constant	2
40-41*	Store zero	4
42-43*	Store B	4
44-45*	Store AL	4
46-47*	Store AU	4
50	See format II instructions	
51	Selective set	4
52	Selective clear	4
53	Selective complement	4
54	Indirect jump and enable interrupts	4
55	Indirect jump	4
56	B skip	4
57	Index skip	6
60	Jump AU = 0	2
61	Jump AL = 0	2

*The odd octal code instructions are modified by the index register.

TABLE 1-5. LIST OF INSTRUCTIONS (CONT)

FUNCTION CODE	OPERATION	EXECUTION TIME (MICROSECONDS)
62	Jump AU ≠ 0	2
63	Jump AL ≠ 0	2
64	Jump AU positive	2
65	Jump AL positive	2
66	Jump AU negative	2
67	Jump AL negative	2
70	Enter AL with constant	2
71	Add constant to AL	2
72	Store ICR	4
73	B jump	2
74	Store address	4
75	Store SR	4
76	Return jump	4
77	Illegal code	2
	Format II Instructions	
50 00	Not used	-
50 01	Set input active	2
50 02	Set output active	2
50 03	Set external function active	2
50 04	Not used	-
50 05	Not used	-
50 06	Not used	-
50 07	Not used	-
50 10	Not used	-
50 11	Input transfer	6
50 12	Output transfer	6
50 13	External function transfer	6
50 14	Enable real-time clock monitor	2
50 15	Terminate input	2
50 16	Terminate output	2
50 17	Terminate external function	2

TABLE 1-5. LIST OF INSTRUCTIONS (CONT)

FUNCTION CODE	OPERATION	EXECUTION TIME (MICROSECONDS)
50 20	Set resume	2
50 21	Skip on input inactive	2
50 22	Skip on output inactive	2
50 23	Skip on external function inactive	2
50 24	Wait for interrupt	2
50 25	Wait for interrupt	2
50 26	Output override	2
50 27	External function override	2
50 30	Remove interrupt lockout	2
50 31	Remove interrupt lockout	2
50 32	Remove external interrupt lockout	2
50 33	Remove external interrupt lockout	2
50 34	Set interrupt lockout	2
50 35	Set interrupt lockout	2
50 36	Set external interrupt lockout	2
50 37	Set external interrupt lockout	2
50 40	Not used	-
50 41	Right shift AU	2+*
50 42	Right shift AL	2+*
50 43	Right shift A	2+*
50 44	Scale factor	4+*
50 45	Left shift AU	2+*
50 46	Left shift AL	2+*
50 47	Left shift A	2+*
50 50	Skip on key setting	2
50 51	Skip on no borrow	2
50 52	Skip on overflow	2
50 53	Skip on no overflow	2
50 54	Skip on odd parity	2
50 55	Skip on even parity	2
50 56	Stop on key setting	2

* If K=1-4, add 2; K=4-8, add 4; K=9-12, add 6; K=13-16, add 8; K=17-20, add 10; K=21-24, add 12; K=25-28, add 14; K=29-32, add 16; K=33-35, add 18

TABLE 1-5. LIST OF INSTRUCTIONS (CONT)

FUNCTION CODE	OPERATION	EXECUTION TIME (MICROSECONDS)
50 57	Skip on no resume	2
50 60	Round AU	2
50 61	Complement AL	2
50 62	Complement AU	2
50 63	Complement A	2
50 64	Not used	-
50 65	Not used	-
50 66	Not used	-
50 67	Not used	-
50 70	Not used	-
50 71	Not used	-
50 72	Enter ICR	2
50 73	Enter SR	2
50 74	Not used	-
50 75	Not used	-
50 76	Not used	-
50 77	Not used	-

(3) PROGRAM TRANSLATION AND CONTROL. - Each of the program instructions contains a coded command for specific computer sequencing. These commands must be decoded to perform the specific function indicated by the instruction. The program translation and control circuitry, consisting of five logically definable areas interprets the coded command, establishes the sequence of events to be performed, and supplies the command enables for the operation. The five areas of the circuitry are the F register, function code translator, format II translator, sequencer, and command enable circuit.

The F register is a seven-bit, flip-flop register which stores the function code during execution of an instruction. During a format I instruction, bits 2^0 through 2^5 contain the function code and bit 2^6 remains cleared. If the programmed instruction is a format II instruction, bit 2^6 is set and the minor function code is contained in bits 2^0 through 2^5. The function code will remain in the F register during the entire performance of the instruction.

The function translator interprets the function code contained in the F register into enable signals to initiate the necessary computer operation. Format I instructions explained in paragraph 1-5b are identified by a two-digit octal code (00 through 47 and 51 through 77).

The format II translator supplies the necessary enables to alter the normal sequence of events to perform specific instructions. Format II instructions are identified by

a four-digit octal code (50 00 through 50 77). The octal 50 of an instruction will set the 2^6 bit of the F register and thus identify the instruction as format II.

The sequencer influences the main timing sequence to insure the proper execution of each instruction. To perform this function, the sequencer selects individual major command sequences in the proper order to execute the instruction. By selectively gating the main timing chain enables, only the operations of the selected command sequence are performed.

Table 1-6 lists major command sequences available for selection by the sequencer. As indicated, they are divided into three general catagories; control, input/output, and wait, Not all major command sequences are required to perform an instruction. It is the function of the sequencer to select those which will fulfill the requirements of the instruction. In several instructions, only one sequence is required; others require several sequence combinations.

In addition to the major command sequences, two minor command sequences are initiated by the main timing chain under the influence of the appropriate major sequence. These sequences are advance P sequence and multiply/divide/shift sequence and operate independently from the major sequence enables.

The command enable circuitry provides the required enabling signals for transfer, shifting, scaling, and storage of words, instructions, or operands in, or between, the several registers within the computer functional logic. Command enables are generated by sequencer outputs or by individual instructions themselves, depending upon the operation to be performed.

(4) REGISTERS. - The control section of the computer contains several registers used for the performance of control functions. These are the index registers, ICR register, SR register, P register, two S registers, and K register. Each register has a specific logic function to perform during the manipulation of instructions and commands.

The index registers are eight memory locations, the contents of which may be used to modify either the address or operand in odd-numbered instructions from 03 to 47. The contents of the registers are one's complement numbers, which may be used to either decrement or increment. Only one of the eight registers may be used during a given operation and selection of the active index register is determined by the contents of the index control register.

The ICR register (index control register) contains the programmed address of the currently active index register to be used for instruction modification. Any one of the eight index registers may be selected by the numerical value entered into the ICR register through program control.

The five-bit SR register (special register), when active, is used to supply the four most-significant bits of memory address in the S register. The maximum bit content of a programmed address is 12 bits. The memory address consists of 16 bits. The additional four bits will be supplied by either the SR register or P register. When the SR register bit 2^3 contains a one, SR register is considered active and will supply the necessary four bits. These four bits will extend the u position of the programmed address to the required 16 bits.

The P register (program address register) is used to store the address of the instruction currently being entered for execution. The contents of the P register are incremented by one when instruction is transferred from its memory location and thus contains the next sequential address to be entered. The four most-significant bits of the address will be supplied by P register to the S register during those instructions when the SR register is not active.

The S registers (memory address registers) receive the address of a memory location at start of a memory cycle and retain this address throughout read/write cycle to control the translation circuitry. The S registers may receive the address from the I/O section (which generates certain assigned addresses), from control or arithmetic section, or from an I/O channel connected to a peripheral device capable of specifying an address. The S1 register is a 16-bit register associated with main memory. The 8-bit S_0 register is associated with control memory.

The K register is basically a six-bit, double-rank counter used for both storage and control. Its primary use is to store and record shift and scale factor counts during execution of multiply, divide, shift, and scale factor instructions. It is also used to store selective skip and stop instructions. During operation, a transfer of bits from the upper rank to the lower rank will decrement the contents by one. The return transfer from lower rank to upper rank prepares the register for the next sequence.

(5) SPECIAL CIRCUITS. - Included in the control section are several circuits which perform unique functions in operation of the computer. These special circuits are parity, B register and ± 1 network, compare, overflow, and stop/skip circuits.

The parity circuits complete operation of the parity check, which is originated by the arithmetic section of the computer. The parity of the contents of X register is checked in a pair-compare scheme to insure an odd parity content. If the resulting signal indicates an even parity, parity flip-flop is set to notify associated computer logic of the parity status.

The B register and the ± 1 network is used to increment or decrement contents of a memory address during input and output operations and to update currently active index register during either B skip or B jump instructions.

The compare circuitry is used to collate contents of the initial and terminal address control words during an input or output operation. If contents of these two words are identical, the compare circuit notifies computer logic of the termination of the buffer.

The overflow circuit performs a test to determine whether an overflow condition exists during an arithmetic operation and notifies computer control logic of results.

The stop/skip logic is used to test for various conditions under which a stop or skip instruction would be performed. Used in conjunction with STOP and SKIP switches on Control Panel 2 (A4), the stop/skip logic compares setting of these switches with the contents of the instruction to determine if this operation should be performed.

i. I/O SECTION. - The I/O section of the computer controls communications between the computer and connected peripheral devices. The computer can be obtained with 4, 8, 12, or 16 input/output channels (refer to table 1-7). Each group of four channels is available in either -3 volt (fast) or -15 volt (slow) interface. Data transfer rates are listed in table 1-1.

The I/O operations consist of three major functions: data transfers, interrupts, and special operations. During data transfer, one I/O operation transfers a single word between the computer and a peripheral device. A complete data transfer operation may consist of a number of I/O operations, which transfer a number of data words. Data transfer between the computer and two or more devices can be performed at the same time; individual I/O operations transferring words to the different devices are interlaced, or multiplexed. Interrupts provide a means to intervene in the main program; thus, giving the computer real-time, and fault detection and correction capabilities.

(1) CLASS OF OPERATION. - Two classes of operation are available for data transfers; normal or intercomputer. Any channel can be operated either as a normal channel (capable of communicating with peripheral equipment) or as an intercomputer channel (capable of communicating with another computer). The normal or intercomputer communication is selected by a switch on the front panel (one switch for each channel).

(2) I/O COMMUNICATION MODES. - Four different communication modes are available: single channel, dual channel, externally specified index (ESI), and externally specified address (ESA). Each even-odd pair of I/O channels may operate in any one of the different modes. The mode of operation is selected by four four-position switches located on the I/O drawer front panel.

The dual channel, ESI, and ESA modes require use of an even-odd channel pair; therefore, only those computers with eight or more channels can utilize those three modes. (A four-channel computer contains one I/O chassis with channels 0, 2, 4, and 6 only.)

(a) SINGLE CHANNEL. - In the single channel mode of operation, communication is with 18-bit data words. The main memory locations to be used for data transfer are internally selected by buffer control words, which are stored in control memory and selected automatically for the active channel.

(b) DUAL CHANNEL. - In dual channel mode of operation, an even-odd channel pair is combined to allow communication with 36-bit data words. Data transfer is by 36 parallel data lines contained in one cable. The 36-data-bit input and output cables must be connected to the odd channel of the channel pair. No external I/O cables can be connected to even channel while in the dual channel mode.

Control on dual channel is maintained by odd channel control lines. Separate parallel words of 18 bits or less are processed sequentially by the I/O section, and all data transfers are controlled in the same manner as for single mode.

(c) ESI MODE. - In ESI mode of operation, an even-odd channel pair is combined; however, only 18-bit data words are transferred.

The main memory locations to be used for data transfer are specified by an I/O buffer control word (index). The address of the controlling index is accepted from the external device on the odd-numbered channel. The location of index words is limited to control memory addresses.

For ESI input operation, the 18 bits on the even-numbered channel are stored at the address specified by the index word; address of the index is specified by 18 bits on the odd-numbered channel. For ESI output operation, the computer performs a normal output buffer with redundant 18-bit words being transferred.

(d) ESA MODE. - In ESA mode of operation, an even-odd channel pair is combined; however, only 18-bit data words are transferred. For ESA input operation, 18 bits on the even-numbered channel are stored at the address specified by 18 bits on the odd-numbered channel. For ESA output operation, the computer performs a normal output buffer with redundant 18-bit words being transferred.

(3) I/O BUFFER MODES. - Four methods for terminating a buffer are provided in the computer: continuous data mode, 1218 (normal) mode, 1218 (NTDS compatible) mode, and 1219 mode. Continuous data mode (CDM) is selected by a bit in the terminal buffer control word. One of the other three modes must be selected (for all chan-

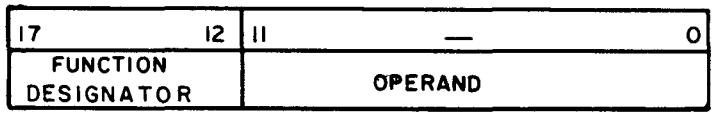
nels) by positioning a printed circuit module in one of three locations (see figure 9-186). The use of continuous data mode is contingent upon which of the other three modes is active.

(a) CONTINUOUS DATA MODE. - The continuous data mode provides the computer with a method of re-establishing a buffer for a given channel and I/O operation without repeating instructions 50:11 - 50:13. In continuous data mode, the computer automatically reinitiates a buffer when buffer termination occurs.

The continuous data mode is selected by setting bit 17 of the terminal buffer control word (TBCW). For channels 0 thru 7, the new buffer control words are contents of addresses 20 + 2K (TBCW) and 20 + 2K + 1 (current buffer control word). For channels 10 thru 17, new buffer control words for the odd numbered channel are contents of address 220 + 2(K-10) (TBCW) and 220 + 2(K-10) + 1 (current buffer control word). Note that K = four bits of channel numbers. The continuous data mode can be set only by bit 17 of the TBCW when the 1219 buffer mode is active.

(b) 1218 (NORMAL) MODE. - This mode disables continuous data mode. Output data and external function buffers are terminated only upon receiving the next output data request (ODR) or external function request (EFR) from peripheral equipment after the last word of the buffer has been sent.

a. FORMAT 1



b. FORMAT 2

Figure 1-5. Instruction Format

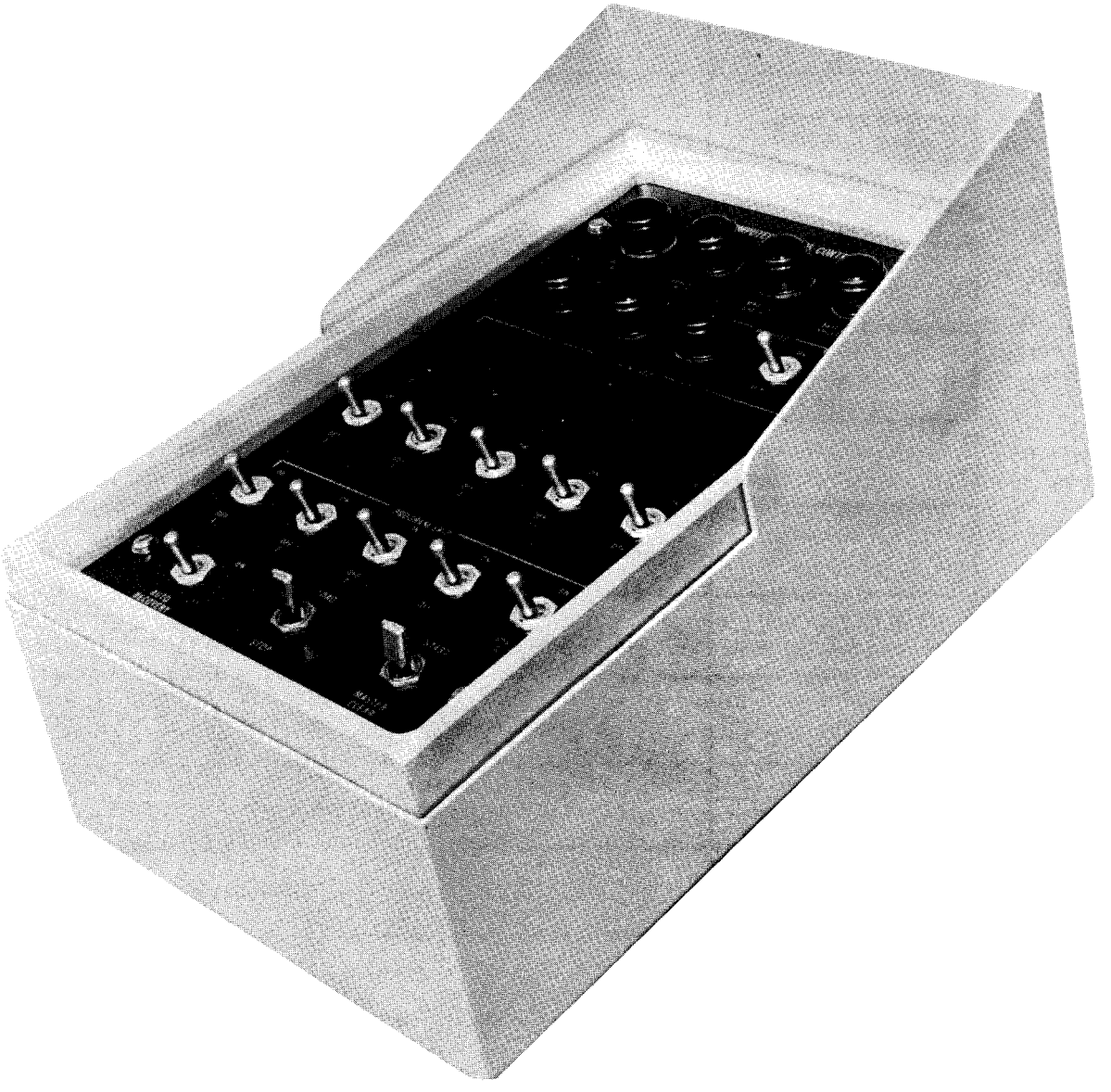


Figure 1-6. Computer Remote Control Console

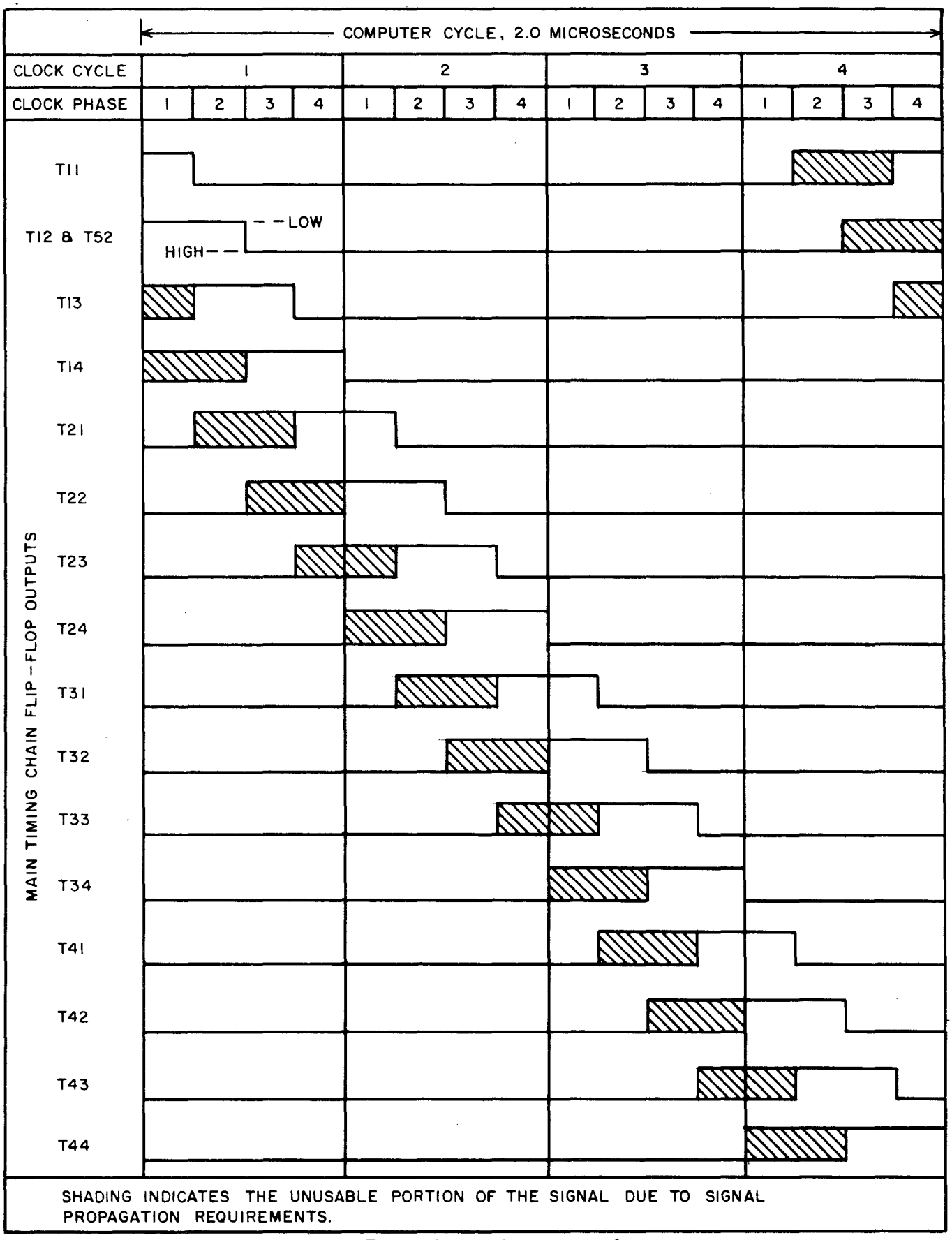


Figure 1-7. Main Timing Cycle Outputs

TABLE 1-6. MAJOR COMMAND SEQUENCES

TYPE	SEQUENCE	FUNCTION
CONTROL	I	Reads instruction word from memory.
	R1	Reads normal 18-bit operands from memory and performs the data manipulations as required.
	R2	Reads second 18 bits of a 36-bit operand and performs data manipulations as required.
	W	Writes an 18-bit word in memory and performs data manipulations as required.
INPUT/ OUTPUT	INTERRUPT	Reads contents of interrupt entrance registers from memory.
	B1	Reads terminal address control word and stores it in appropriate control memory address.
	B2	Reads initial address control word and stores it in appropriate control memory address.
	I/O 1	Reads from or writes into memory, either an 18-bit word or first 18 bits of a 36-bit word.
	I/O 2	Reads from or writes into memory, second 18 bits of a 36-bit word.
WAIT	WAIT	Inhibits performance of all control sequences but permits input/output operations to continue until an interrupt occurs.

TABLE 1-7. I/O CHANNEL GROUPING

NUMBER OF I/O CHANNELS	CHANNEL DESIGNATIONS (OCTAL)
4	0, 2, 4, 6
8	0 thru 7
12	0 thru 7 plus 10, 12, 14, 16
16	0 thru 7, 10 thru 17

(c) 1218 (NTDS COMPATIBLE) MODE. - This mode disables continuous data mode. Output data and external function buffers are terminated upon sending the last word of the buffer.

(d) 1219 MODE. - This mode enables continuous data mode. Output data and external function buffers are terminated upon sending the last word of the buffer.

(4) DATA FORMAT. - Three types of information transferred between the I/O section and peripheral units are data words, function words, and external interrupt codes.

Data words represent alphabetic and numeric data. Input data words are data entered into the computer from peripheral units. Output data words are data sent to peripheral units from the computer. Data words are 18 bits for single-channel, ESI, and ESA modes, and 36 bits for dual-channel mode.

Function words are control information sent from the computer to peripheral units to specify the type of operation a peripheral unit is to perform. Function words are 18 bits for single-channel ESI, and ESA modes, and 36 bits for dual-channel mode.

External interrupt codes are control information sent to the computer from a peripheral unit. The external interrupt code specifies an error or special condition that exists in a peripheral unit.

(5) I/O INSTRUCTION WORD FORMAT. - The input/output instruction word format, normally called format II, is as follows:

BIT	17 — 12	11 — 6	5 — 0
CODE	F	M	K

f - Always octal 50 for input/output instruction.

m - Specifies type of input/output instruction.

k - Specifies channel number.

All three codes are octal. The f and m codes are shown in text separated by a colon (f:m); since f is always 50 for an I/O instruction, the instruction word code appears as 50:m.

(6) I/O INSTRUCTIONS. - The I/O instructions are listed in table 1-8.

(a) INITIATE TRANSFER INSTRUCTIONS. - Six of the I/O instructions are used to initiate data transfer (including external function words) between the computer and peripheral unit.

If the I/O instruction word at address N is an input-transfer, output-transfer, or external-function instruction (50:11, 50:12, or 50:13), two buffer control words are read from addresses N + 1 and N + 2 and stored in the control memory. These two control words outline the size of the memory area (buffer) to be used. The instruction specified by m code of the instruction word is performed with the chan-

nel specified by k portion of the instruction word. Data words are loaded into or removed from the designated buffer. When the buffer is full (all words removed or all words loaded), operation is terminated.

If the I/O instruction word is a set-input-active, set-output-active, or set-external-function-active instruction (50:01, 50:02, or 50:03), it is assumed that buffer control words are already located in control memory and, addresses N + 1 and N + 2 are not read. The rest of data transfer operation is performed like the 50:11, 50:12, or 50:13 instructions.

(b) TERMINATE TRANSFER INSTRUCTIONS. - Three I/O instructions (50:15, 50:16, and 50:17) are used to end a data transfer prior to normal termination. Because external function and output transfer utilize some common circuitry, terminating either one terminates the other.

(c) STATUS TEST INSTRUCTIONS. - Four I/O instructions (50:21, 50:22, 50:23, and 50:57) provide a means for checking the status of I/O operation. If a 50:21, 50:22, or 50:23 instruction is executed, a skip occurs if the related data transfer operation is inactive. If a 50:57 instruction is executed, a skip occurs if resume status is inactive (clear).

(d) SPECIAL OPERATION INSTRUCTIONS. - Eight I/O instructions perform special operations in the I/O section. The use of these instructions is discussed in paragraphs 1-3i(10) and 1-3i(11).

(7) BUFFER CONTROL WORDS. - Buffer control words specify areas in memory where data or function words are stored. During input operations, input data words are received from the peripheral unit and stored at the location specified by buffer control words. During output operations, output-data or external-function words are removed from memory location specified by buffer control words and sent to the peripheral unit.

Two memory areas are assigned to each input/output channel: one area for input data words and one area for output-data or external-function words. Two buffer control words are required to specify a memory area: one specifies initial current address and one specifies the last address. Buffer control words are stored in locations as specified in table 1-13.

Memory area (buffer) to be used is established by I/O instructions 50:11, 50:12, or 50:13 (figure 1-8). If the I/O instruction word at address N (N can be any memory address) is either an input transfer, output transfer, or external function transfer (50:11, 50:12, or 50:13) instruction, address N + 1 must contain terminal address designator and address N + 2 must contain initial address designator.

The contents of address N + 1 and N + 2 are established by the program. When the computer decodes 50:11, 50:12, or 50:13 at address N, it automatically reads addresses N + 1 and N + 2 to obtain terminal and initial addresses of the buffer. The initial address designator is incremented or decremented for each data transfer; therefore, it also can be called the current address designator.

The two buffer control words read from addresses N + 1 and N + 2 are stored in specific locations of control memory during execution of the I/O operation. The terminal address is stored at address 60 + 2k or 260 + 2(k-10) for a 50:11 instruction; 40 + 2k or 240 + 2(k-10) for a 50:12 instruction; or 20 + 2k or 220 + 2(k-10) for a 50:13 instruction. (k refers to channel numbers specified by k portion of the I/O instruction word.) The current address of the buffer is stored at

TABLE 1-8. INPUT/OUTPUT INSTRUCTIONS

FUNCTION	OCTAL CODE	OPERATION
INITIATE TRANSFER	50:01	Set input active
	50:02	Set output active
	50:03	Set external function active
	50:11	Input transfer
	50:12	Output transfer
	50:13	External function
TERMINATE TRANSFER	50:15	Terminate input
	50:16	Terminate output (and external function)
	50:17	Terminate external function (and output)
STATUS TEST	50:21	Skip on input inactive
	50:22	Skip on output inactive
	50:23	Skip on external function inactive
SPECIAL OPERATION	50:20	Set resume
	50:14	Enable real-time clock monitor
	50:26	Output override
	50:27	External function override
	50:30 and 50:31	Remove interrupt lockout
	50:32 and 50:33	Remove external interrupt lockout
	50:34 and 50:35	Set interrupt lockout
	50:36 and 50:37	Set external interrupt lockout
	50:57	Skip on no resume

61 + 2k or 261 + 2(k-10) for a 50:11 instruction; 41 +2k or 241 + 2(k-10) for a 50:12 instruction; or 21 + 2k or 221 + 2(k-10) for a 50-13 instruction. For example, assume that the instruction word at address N specifies a 50:11 instruction for channel 3: terminal address at N + 1 is stored at control-memory address 66 (60 + 2·3 = 66); initial or current address is stored at control-memory address 67 (61 + 2·3 = 67). The buffer control words are shown in figure 1-8.

(a) MODIFIER DESIGNATOR. - The most significant bit (17) of current address word is the modifier designator. If bit 17 is set to one, the current address is decremented for each data transfer; if bit 17 is set to zero, the current address is incremented for each data transfer.

(b) MONITOR DESIGNATOR. - Bit 16 of the current address word is the monitor designator. If bit 16 is set to one, an internal interrupt occurs when buffer is full; if bit 16 is set to zero, no interrupt will occur when buffer is full.

(c) CONTINUOUS DATA MODE DESIGNATOR. - Bit 17 of the terminal address buffer control word is the continuous data mode designator. If the bit is set to one upon

termination of the buffer, and if computer buffer mode 1219 is active, the computer will enter continuous data mode. (Refer to paragraph 1-3i(3).) If bit 17 is set to zero, buffer termination will be as usual. Continuous data mode designator and monitor designator may be set to one in a pair of buffer control words; thus, notifying the program of completing one buffer while establishing another.

Output operations are performed to transfer data words and external function words from computer to peripheral device.

(8) DATA TRANSFER OPERATIONS. - Data transfer operations transfer words between the computer memory and a peripheral device. A buffer is a specific address in memory used for the data transfer operation. Location of the buffer is specified by buffer control words. A different pair of buffer control words is used for each channel and for each of the three transfer instructions (input transfer, output transfer, and external function).

(a) INPUT TRANSFER OPERATIONS. - Input transfer operations include input data and external interrupt operations. Both types are initiated either by set input active (50:01) or input transfer (50:11) instructions. The peripheral device used activates either an external-interrupt-request line or an input-data-through line to indicate the type of input operation to be performed.

For an input data operation, the computer accepts data words from the peripheral device and stores them in the designated buffer. Operation is terminated when the buffer is full. The data transfer could be as short as a single word.

For an external interrupt operation, the peripheral device sends coded words to the computer to indicate that an emergency condition has occurred. An emergency condition includes transmission of data with a parity error, magnetic tape breakage, card punch feed error, voltage faults, and several others. Each individual error generates a different external interrupt word. The code used for each error is a function of the peripheral device, and provisions must be made in the computer program to properly translate and react to each condition.

A channel does not need to be active to receive an external interrupt request. No buffer control words are used for an external interrupt operation.

(b) OUTPUT TRANSFER OPERATIONS. - Output transfer operations included output transfer and external-function operations. Output transfer is initiated either by set output active (50:02) or an output transfer (50:12) operation.

For an output data operation, the computer removes data words from the designated buffer and sends them to the peripheral device. The operation is terminated when the buffer is empty. The data transfer could be as short as a single word.

An external function operation allows the computer to control operations of the peripheral devices. For an external function operation, the computer removes external function words from the designated buffer and sends them to the peripheral device. External function words are translated by peripheral devices into commands, which initiate appropriate functions in the device in preparation for an input or output operation. Codes used and operations desired are a function of the peripheral device, its capabilities, and needs of the computer program.

(9) MONITOR INTERRUPT. - A monitor interrupt causes channel-oriented program intervention upon completion of a data transfer buffer. The program, through a subroutine, acknowledges that I/O operation has been completed and makes the necessary adjustments. A monitor interrupt is established by proper coding of buffer

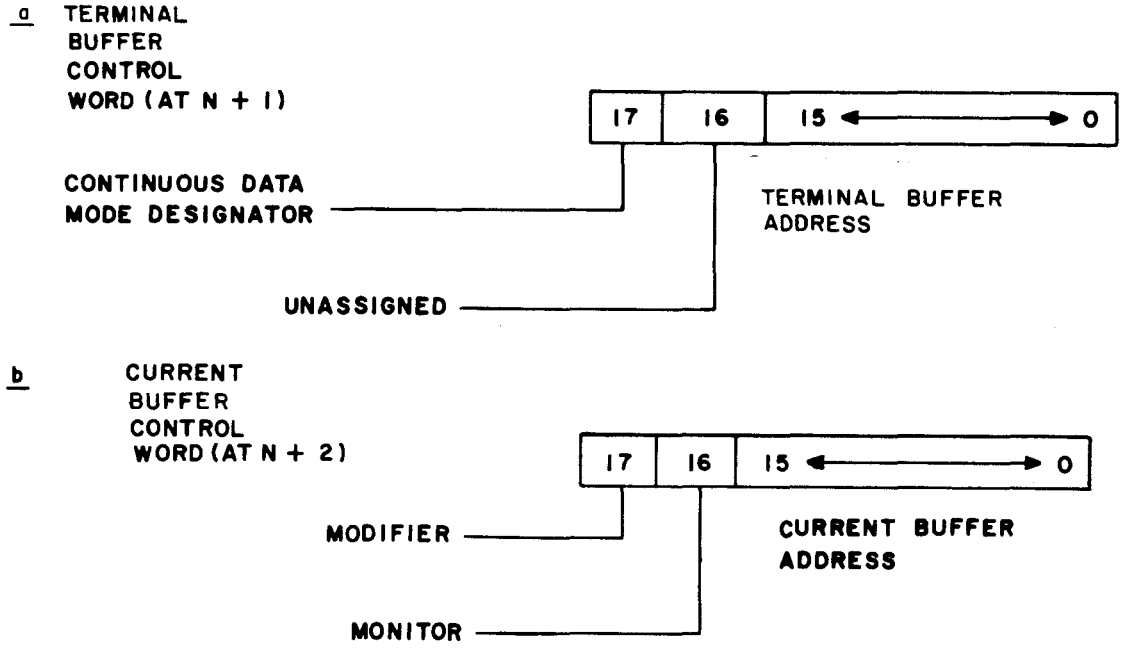


Figure 1-8. Control Word Formats

control words for the type of operation to be used (refer to paragraph 1-3i(7)). Monitor interrupts can be used during input-transfer, output-transfer, and external-function instructions.

With monitor interrupt set, the channel is made inactive at completion of the buffer. The computer is then forced, according to the channel and type of monitor, to a monitor interrupt register, which is an assigned control memory address.

In the ESA mode where several equipments are being multiplexed on the same channel, a channel remains active at completion of the buffer; this is necessary because other data transfers may still be in operation on that channel. The monitor interrupt stores the odd-channel input in the ESA output terminal word register before forcing the computer to the same address. The program can detect, through a subroutine, which of the equipments on the multiplexed channel has completed data transfer.

The external interrupt monitor, which is not subject to coding of buffer control words, is unconditionally set during I/O sequence, which stores the external function word.

(10) SPECIAL INTERRUPTS. - The I/O section provides logic for five special interrupts: program fault, resume fault, real-time clock monitor, external synchronizing interrupt, and RTC overflow; these interrupts have priorities as listed here. Special interrupts allow intervention during a program so that occurrences pertinent to the results of a program can be analyzed.

When an interrupt occurs, the computer begins interrupt I sequence immediately upon completion of instruction or I/O operation which is in process. During interrupt I sequence, the computer references a specific address, depending upon the type of interrupt. Usually a return jump is stored at that address so an interrupt-processing subroutine can be performed, and the computer can return to the interrupted position in the program.

(a) PROGRAM FAULT. - A program fault occurs when an illegal instruction (00, 01, or 77) is decoded. This interrupt forces the computer to either address 00000 or address 00500, depending upon the position of AUTO RECOVERY switch. If AUTO RECOVERY switch is in the up position, address 00500 is selected; this address is the initial address of the bootstrap program.

(b) RESUME FAULT. - When a channel is operating as an intercomputer channel (IC) and is performing an output data request or external function request, the channel ties up output channels for the entire group until the receiving computer sends a resume. If the receiving computer does not acknowledge receipt of the transmitted word, it would render the four channels of the chassis inoperative in the transmitting computer. If the IC channel were dual, all other channels of the odd and even chassis would be inoperative. To prevent this condition from continuing indefintely, the RTC (real-time clock) serves as a timing device on all intercomputer output data and external function transmission.

The RTC is monitored from time of transmission. If the clock reaches its maximum count (in a 0 to 1024-count cycle) before a resume is received, resume fault is set. Since the RTC may be at any point in the count cycle as transmission begins, the time varies when resume must be received. This time is from 1/1024th of a second to one second, since RTC rate is 1024 count per second. Once resume fault is set, the computer enters interrupt sequence and is forced to address 00011.

(c) REAL-TIME CLOCK MONITOR. - The real-time clock (RTC) monitor interrupt causes an intervention in the computer program when value of the RTC monitor word wtored at address 00014 equals the value of the RTC word stored at address 00015, provided instruction 50:14 (enable RTC monitor) has been performed. Once the interrupt occurs, the computer is forced to address 00012 where it can enter a subroutine for RTC processing.

(d) EXTERNAL SYNCHRONIZING INTERRUPT. - The external synchronizing interrupt (ext sync) provides the computer and associated peripheral device with the ability to maintain program synchronization between detection of physical occurrences and data processing related to the occurrence. Thus, real-time computation can be performed with the peripheral device connected to one external synchronizing jack.

At the receipt of an external synchronizing signal, the computer sets the external synchronizing condition and the computer program is interrupted. The computer is then forced to control-memory address 00016.

(e) REAL-TIME CLOCK OVERFLOW. - The RTC overflow interrupt occurs when the RTC word (in the BU register) changes from maximum to zero. The time interval to step the RTC word from zero to maximum is 256 seconds. If the RTC word has not been reset prior to reaching its maximum count (and is permitted to automatically change to zero), RTC overflow/interrupt is set. The computer is then forced to control-memory address 00016.

(11) SPECIAL OPERATIONS. - The I/O section supplies several special operations that give the computer added programming control of I/O operations. These include real-time clock, override, interrupt lockout, wait, and resume instructions.

(a) REAL-TIME CLOCK. - The real-time clock normally operates at a rate of 1024 cps. Different frequencies are available at customer request. RTC operation counts into the RTC word register located at address 00015 in control memory. The RTC operation is inhibited under the following conditions: RTC/DISC switch is in up position; the computer is in R1 sequence of instructions 20 - 23 or 57; the computer is handling the first I/O sequence of a 36-bit operation; the computer has a continuous data request.

(b) OVERRIDE. - The computer has the ability to force an external function word to be sent to a peripheral device regardless of the state of EF request line for that channel. This is accomplished by program use of the external-function-override instruction (50:27). This program option enables the computer to re-establish positive control by overriding whatever function the peripheral device is performing. This instruction is necessary during an intercomputer operation if the computer wishes to send an external function, since EF request line is not usable.

(c) INTERRUPT LOCKOUT. - The computer has two interrupt lockout instructions and two lockout removal instructions. The instructions are 50:30 and 50:31, remove interrupt lockout; 50:32 and 50:33, remove external interrupt lockout; 50:34 and 50:35, set interrupt lockout; and 50:36 and 50:37, set external interrupt lockout.

The set-interrupt-lockout instruction prevents any interrupt from being processed, except an instruction fault interrupt. Any interrupt received during lockout period will be recorded, and, when the lockout is removed, will be processed in order of priority. However, if two interrupts of the same type are received during the lockout period, the second will be ignored.

The set-external-interrupt-lockout instruction prevents processing of an EI monitor by making it impossible to scan the EI monitors. The EI request is processed as usual and monitor flip-flop is set, but the monitor cannot be processed until lockout is removed.

To remove lockout conditions, the proper remove-lockout instruction must be used. Instructions must be paired properly; that is, 50:30 and 50:31 with 50:34 and 50:35, and 50:32 and 50:33 with 50:36 and 50:37.

(d) WAIT. - Wait-for-interrupt instruction, 50:24 and 50:25, stops the computer from performing any operation until receipt of an interrupt. During this time, the clock and the timing chain run but the computer sequencer remains in wait sequence cycle after cycle. The only sequence the computer can advance to is interrupt sequence, and then only upon receipt of any interrupt, although I/O functions continue during this time.

(e) RESUME. - The set resume instruction, 50:20, provides programming means to overcome a resume fault. When the instruction is used, data in the output registers is lost.

(12) PRIORITY. - The computer performs an I/O priority scan concurrently with a program instruction sub-sequence. I/O priority scan sequentially scans priority A events listed in table 1-9. If no priority A even is detected, the scan sequentially scans the priority B events listed in table 1-10.

TABLE 1-9. SEQUENCE SCAN PRIORITY A

PRIORITY A	SCAN FOR DATA EVENTS
1	Real-Time Clock Update
2	External Interrupt
3	External Function Request
4*, 5*	Output Request or External Function
5*, 4*	Input Data Request

*Each time either 4 or 5 is detected, they shall reverse their priority rating.

TABLE 1-10. SEQUENCE SCAN PRIORITY B

PRIORITY B	SCAN FOR INTERRUPT EVENTS
1	Fault (Program)
2	Resume Fault
3	Real-Time Clock (Monitor)
4	Real-Time Clock (Overflow)
5	Synchronizing Interrupt
6	External Interrupt (Monitor)
7	External Function (Monitor)
8	Output (Monitor)
9	Input (Monitor)

The priority A events 2, 3, and 4 are channel dependent and are scanned for each channel, starting with the highest numbered channel and ending with channel 0. (A priority 4 event on channel 17_8 has a higher priority than a priority 2 or 3 event on channel 16_8.) If one or more priority A events are detected, the highest priority event is processed, and scan restarted at the beginning of the priority A scan.

Priority B events 6, 7, and 8 are channel dependent and are scanned for each channel starting with the highest numbered channel and ending with 0. If one or more priority B events are detected, the highest priority event is processed and scan restarted at the beginning of priority A scan. If no priority B event is detected, scan is restarted at the beginning of the priority A scan.

(13) I/O SECTION LOGIC. - The I/O section (figure 1-9) contains seven logically-definable areas: active, request, priority, input selectors, acknowledge, C registers, and I/O control.

(a) ACTIVE. - In normal class of operation, active circuitry functions as the on/off switch of the I/O section. Except for external interrupts, communications

can exist between computer and peripheral devices only when I/O channels are active. In the intercomputer class of operation, active circuitry is bypassed.

(b) REQUEST. - Request portion of the I/O section receives four types of request signals (external interrupt, input data, output data, and external function) from peripheral devices. The type of request is recorded and maintained until the request is honored by the computer. Only one request of each type is accepted by an I/O channel until that request is honored. The request portion of the I/O section also receives the same four types of monitor signals (an internal system whereby the computer is notified that an I/O operation has been completed). It records the type of monitor and maintains this information until the monitor is honored.

During operation, it is possible for each I/O channel to have one of the four types of requests and monitors present at the same time. Thus, priority circuitry is necessary to honor requests or monitors.

(c) PRIORITY. - Priority of I/O requests and monitors is established according to channel number and function. Once priority is established, channel number and function is encoded into a binary value, which is sent as an address to control memory. This address specifies which control words and type of I/O operation are to be used for each channel.

(d) INPUT SELECTORS. - Input selectors are gated input amplifiers. Each I/O channel has eighteen selectors, one for each bit of the data words. When a peripheral device sends a request to the computer, it also places a data word on the input lines. After priority is granted to the requesting channel, the data word of that channel is gated into the computer through input amplifiers.

(e) ACKNOWLEDGE. - Acknowledge circuitry informs peripheral devices of the status of I/O operations by sending three types of acknowledge signals: input data acknowledge, output data acknowledge, and external function acknowledge. The type of signal and channel number selected is influenced by priority circuit.

The acknowledge signal sent depends upon the type of function performed. Input acknowledge signal is sent for an external interrupt or input data transfer. Output data acknowledge signal is sent for an output data transfer. External function acknowledge is sent for an external function transfer.

j. ARITHMETIC SECTION. - The arithmetic section of the computer performs arithmetic and logic functions to present a solution to a given problem. Arithmetic functions include addition, subtraction, multiplication, division, shifting, and scaling. Logic functions include masking, selective substitution, comparisons, and word transfers between components of the arithmetic section or between the arithmetic section and computer core memory. Circuits contained within the arithmetic section include a 36-bit A register (subdivided into two 18-bit registers), X register, D register, W register, and subtractive-type adder.

The arithmetic section employs one's complement binary arithmetic and a subtractive type adder to perform arithmetic and logical operations. Arithmetic operations are addition, subtraction, multiplication, and division, as well as shifting and scaling. Logical operations include masking, selective substitution, and complementing.

The arithmetic section is divided into seven basic subsections as shown in figure 1-9. These subsections are arithmetic selector, adder, X register, D register, AU register, AL register, and W register. Control of the arithmetic section is maintained by command enable circuits of the control section.

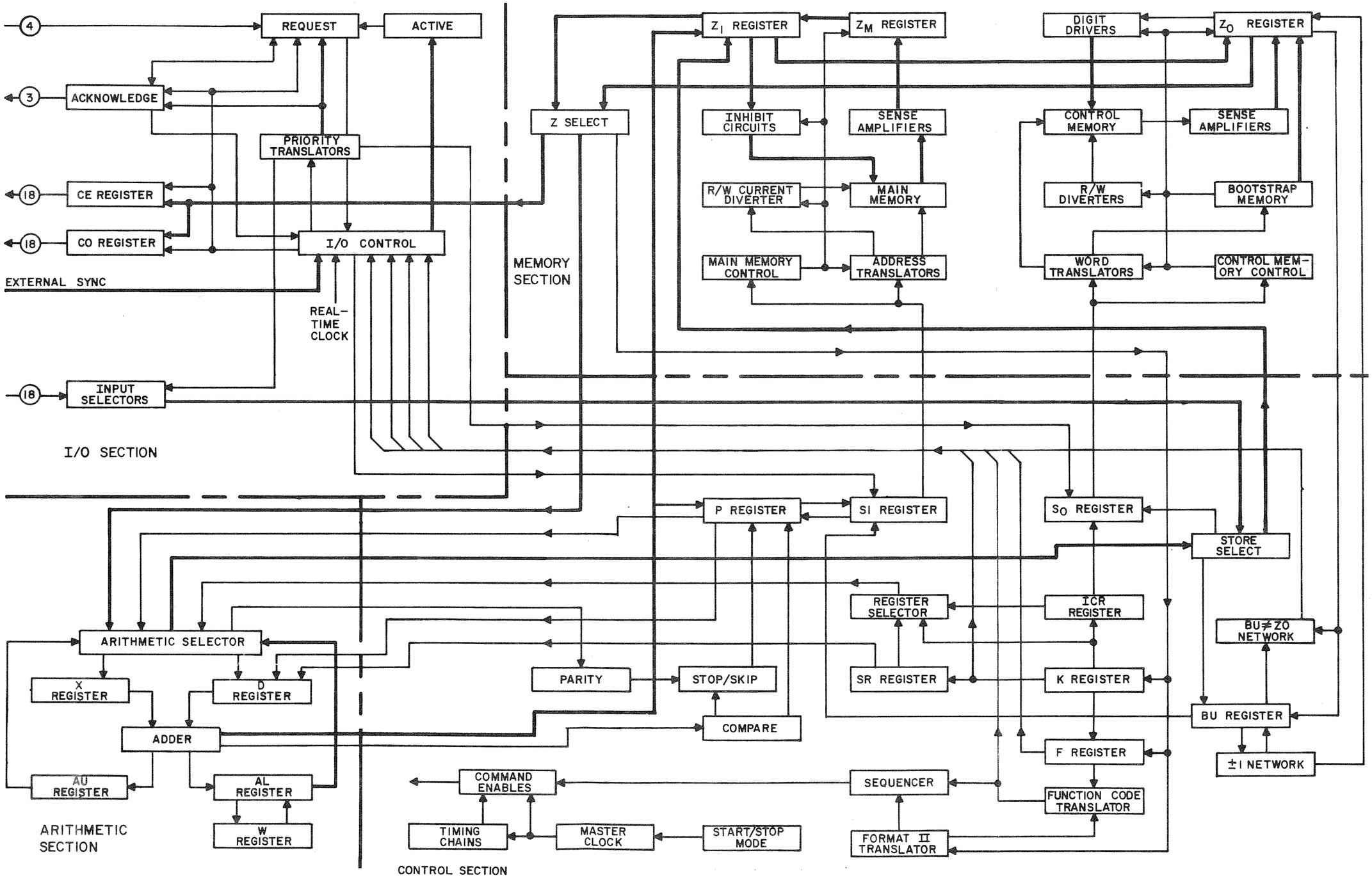


Figure 1-9. Computer Block Diagram

(1) ARITHMETIC SELECTOR. - The arithmetic selector acts as a distribution point for data entering and leaving the arithmetic section with the exception of data concerning P, S, and Z_1 registers. The selector receives data from the control section and A register; it sends data to X and D registers, control (parity), and memory (store selector) sections.

(2) ADDER. - The adder is an 18-stage, subtractive-type device. It provides, as an output, the solution of (X) - (D') (for example, the solution of the quantity held in X register minus the complement of the quantity held in D register). In a subtraction problem, it is sometimes necessary to borrow from a higher order digit; this is also true in the adder. To increase speed of the adder, section borrows are used for each of the three stages. Section borrows pass a known borrow across stages that cannot satisfy a borrow to a stage that can satisfy the needed borrow; it also starts complementing due to a borrow in the stages in between. Thus, time needed to propagate a borrow down eighteen stages of the adder is reduced by a factor of six.

(3) REGISTERS. - All registers in the arithmetic section are 18-bit, flip-flop registers. They are all controlled by command enables from the control section.

The X register is one of the input registers of the adder. It is also used with the AU register for left and right shifting. D register is the other input register of the adder.

AU register is the upper half of the A register and receives data from the adder. It is also used for shifting. AL register is the lower half of the A register and receives data from the adder. It is also used for left and right shifting with the W register. The only function of the W register is shifting.

The parts of A register are so connected that left or right shifting can be accomplished on a 36-bit word.

k. MEMORY SECTION. - The computer is available with 16,384, 32,768, 49,152, or 65,536 18-bit words of addressable memory. Computer storage is divided into main memory, control memory, and a nondestructive read-out bootstrap memory. Storage location for each word in all three memories is assigned a discrete address. Storage capacity of the three memory subsections is listed in table 1-11.

(1) MAIN MEMORY. - Main or core memory provides storage for programs, constants, and data. Main memory capacity is 16-, 32-, 49-, or 65-thousand 18-bit words. The number of usable addresses is either 160 or 288 less than the number of actual storage locations; control and bootstrap memory addresses overlap with main memory addresses (see table 1-11). Memory address assignments are listed in table 1-12.

Main memory is a random-access, coincident-current, bit-oriented core memory. Cycle time is 2 microseconds and maximum access time is 750 nanoseconds.

Main memory is divided into seven logically definable areas (figure 1-9): memory control, address translators, memory cores, inhibit circuits, sense amplifiers, Z_m register, and Z_1 register.

(a) MEMORY CONTROL. - Main memory control provides timing and enable signals to regulate memory circuit operation. When an input signal initiates a memory cycle, control circuits provide signals to perform a read cycle and a write cycle.

(b) ADDRESS TRANSLATORS. - Address translators decode the memory address stored in S1 register and enable the appropriate X-line and Y-line to select the decoded address. Memory control signals pulse selected X and Y lines through the address translator to read and write at the selected address.

(c) MEMORY CORES. - Main memory cores provide actual storage for the program and data words. Cores are located on memory stacks. Each stack consists of 18 planes with 4096 cores per plane. Each plane stores a single bit of an 18-bit word. The 18 planes together form the stack and store 4096 18-bit words.

One of 64 X-lines and one of 64 Y-lines is selected by address translators to select one of 4096 addresses on a stack. Address translators also select one of 4, 8, 12, or 16 stacks in the memory.

(d) INHIBIT CIRCUITS. - Inhibit circuits are used to inhibit writing a one at the bit positions that are to store a zero. At write time, X and Y lines are pulsed to write a one at all 18-bit positions of the selected address. If a zero is to be stored at any bit position in this word, an inhibit pulse must be generated for those positions.

(e) SENSE AMPLIFIERS. - Sense amplifiers monitor 18-output lines from each stack (one line for each bit of a word). When cores for a single word are pulsed at read time, the sense amplifiers detect the one (core switches) and zero (core does not switch) outputs and stores them in the Z_m register.

(f) Z_m REGISTER. - The Z_m register provides necessary storage for the information read from main memory. Each of the four stacks containing 16K-words in main memory has one Z_m register; however, only one is used at a time. Thus, the Z_m register is referenced singularly.

(g) Z_l REGISTER. - The Z_l register is used as a buffer for words being transferred between main memory and other sections of the computer.

TABLE 1-11. COMPUTER MEMORY SIZES

MEMORY DESIGNATION	TOTAL ADDRESSES AVAILABLE	BOOTSTRAP MEMORY ADDRESSES	CONTROL MEMORY ADDRESSES	MAIN MEMORY ADDRESSES
16K	16,384	32	128 256	16,224 16,096
32K	32,768	32	128 256	32,608 32,480
49K	49,152	32	128 256	48,992 48,864
65K	65,536	32	128 256	65,376 65,248

TABLE 1-12. MAIN MEMORY ADDRESS ASSIGNMENTS

MEMORY ADDRESS	ADDRESS ASSIGNMENT
000100 thru 000117	External interrupt (EI) entrance registers, I/O channels 0 thru 7.
000100	EI channel 0, entrance address
000101	EI channel 0, interrupt word
000102	EI channel 1, entrance address
↕	
000117	EI channel 7, interrupt word
000120 thru 000137	External function monitor interrupt (EFMI) registers and ESI external function terminate (ESI-EFT) control words, I/O channels 0 thru 7.
000120	EFMI for channel 0, entrance address
000121	ESI-EFT for channel 0, control word
000122	EFMI for channel 1, entrance address
↕	
000137	ESI-EFT for channel 7, control word
000140 thru 000157	Output monitor interrupt (OMI) registers and ESI output terminate (ESI-OT) control words for I/O channels 0 thru 7.
000140	OMI for channel 0, entrance address
000141	ESI-OT for channel 0, control word
000142	OMI for channel 1, entrance address
↕	
000157	ESI-OT for channel 7, control word
000160 thru 000177	Input monitor interrupt (IMI) entrance registers and ESI input terminate (ESI-IT) control words for I/O channels 0 thru 7.
000160	IMI for channel 0, entrance address
000161	ESI-IT for channel 0, control word
000162	IMI for channel 1, entrance address
↕	
000177	ESI-IT for channel 7, control word

TABLE 1-12. MAIN MEMORY ADDRESS ASSIGNMENTS (CONT.)

MEMORY ADDRESS	ADDRESS ASSIGNMENT
000300 thru 000317	External interrupt (EI) entrance registers, I/O channels 10 thru 17.
000300	EI for channel 10, entrance address
000301	EI for channel 10, interrupt word
000302	EI for channel 11, entrance address
↕	
000317	EI for channel 17, interrupt word
000320 thru 000337	External function monitor interrupt (EFMI) registers and ESI external function terminate (ESI-EFT) control words, I/O channels 10 thru 17.
000320	EFMI for channel 10, entrance address
000321	ESI-EFT for channel 10, control word
000322	EFMI for channel 11, entrance address
↕	
000337	ESI-EFT for channel 17, control word
000340 thru 000357	Output monitor interrupt (OMI) registers and ESI output terminate (ESI-OT) control words for I/O channels 10 thru 17.
000340	OMI for channel 10, entrance address
000341	ESI-OT for channel 10, control word
000342	OMI for channel 11, entrance address
↕	
000357	ESI-OT for channel 17, control word
000360 thru 000377	Input monitor interrupt (IMI) entrance registers and ESI input terminate (ESI-IT) control words for I/O channels 10 thru 17.
000360	IMI for channel 10, entrance address
000361	ESI-IT for channel 10, control word
000362	IMI for channel 11, entrance address
↕	
000377	ESI-IT for channel 17, control word
000400 thru 000477	Assigned to expanded ESI option when selected; otherwise instruction word and data storage.

TABLE 1-12. MAIN MEMORY ADDRESS ASSIGNMENTS (CONT.)

MEMORY ADDRESS	ADDRESS ASSIGNMENT
000540 thru 000577	Instruction word and data storage
000600 thru 000677	Assigned to expanded ESI option when selected; otherwise instruction word and data storage.
000700 thru 177777	Instruction word and data storage

(2) BOOTSTRAP MEMORY. - Bootstrap memory (figure 1-9) is a word-oriented, nondestructive readout-type of memory with a maximum access time of 300 nanoseconds and a cycle time of 2 microseconds. Bootstrap memory is a 32-word prewired program that loads a program of instructions via a peripheral device such as a paper tape reader or a magnetic tape transport and automatically reloads the program if the computer senses an invalid operation. Bootstrap memory utilizes logic circuitry assigned to control memory for the performance of its functions. Bootstrap memory addresses are from 00500 through 00537.

Bootstrap mode switch located on the front panel of drawer A4 provides a means of storing a second bootstrap program using main memory storage. In NDRO position, the switch allows the computer to reference nondestructive readout bootstrap memory where, for example, the paper tape load routine is stored. In MAIN MEMORY position, the computer references main memory addresses 00500 through 00537 where the magnetic tape load routine may be stored. The referenced main memory addresses are not the NDRO type and information stored at these addresses may be changed or altered while the switch is in MAIN MEMORY position.

(3) CONTROL MEMORY. - Control memory (figure 1-9) is a word-oriented core memory consisting of either 128 or 256 18-bit word storage locations. Access time of the control memory is a maximum of 300 nanoseconds; cycle time is 500 nanoseconds. Address assignments for the control memory are listed in table 1-13.

The entire control memory circuit provides fast access to control words and to modifying index registers which allows this section to operate independently from the other two memory sections of the computers. Thus, because information is more readily available for input and output operations, operand and address modification, and real-time clock functions, the speed of the main computer operations is increased.

(a) S_0 REGISTER. - The S_0 register is the address register for control memory. Reference to an address in control memory is entered in the S_0 register for translation. Any location in control memory may be addressed through program control and the constants may be entered in the desired registers. S register slaves are gates for the application of proper enables to succeeding circuits.

TABLE 1-13. CONTROL MEMORY ADDRESS ASSIGNMENTS

MEMORY ADDRESS	ADDRESS ASSIGNMENT
00000	Fault interrupt entrance register
00001 thru 00010	Index registers (8).
00011	Resume fault interrupt entrance register.
00012	RTC monitor interrupt entrance register.
00013	RTC overflow interrupt entrance register.
00014	RTC monitor word register.
00015	RTC word register.
00016	Synchronizing interrupt entrance register.
00017	Scale factor shift count word register.
00020 thru 00037	Continuous data mode (CDM) and external function (EF) buffer control registers for I/O channels 0 thru 7.
00020	CDM/EF for channel 0, terminal address
00021	CDM/EF for channel 0, current address
00022	CDM/EF for channel 1, terminal address
↕	
00037	CDM/EF for channel 7, current address
00040 thru 00057	Output buffer control (OBC) registers for I/O channels 0 thru 7
00040	OBC for channel 0, terminal address
00041	OBC for channel 0, current address
00042	OBC for channel 1, terminal address
↕	
00057	OBC for channel 7, current address
00060 thru 00077	Input buffer control (IBC) registers for I/O channels 0 thru 7
00060	IBC for channel 0, terminal address
00061	IBC for channel 0, current address
00062	IBC for channel 1, terminal address
↕	
00077	IBC for channel 7, current address

TABLE 1-13. CONTROL MEMORY ADDRESS ASSIGNMENTS (CONT.)

MEMORY ADDRESS	ADDRESS ASSIGNMENT
00220 thru 00237	Continuous data mode (CDM) and external function (EF) buffer control registers for I/O channels 10 thru 17.
00220	CDM/EF for channel 10, terminal address
00221	CDM/EF for channel 10, current address
00222	CDM/EF for channel 11, terminal address
↕	
00237	CDM/EF for channel 17, current address
00240 thru 00257	Output buffer control (OBC) registers for I/O channels 10 thru 17.
00240	OBC for channel 10, terminal address
00241	OBC for channel 10, current address
00242	OBC for channel 11, terminal address
↕	
00257	OBC for channel 17, current address
00260 thru 00277	Input buffer control (IBC) registers for I/O channels 10 thru 17.
00260	IBC for channel 10, terminal address
00261	IBC for channel 10, current address
00262	IBC for channel 11, terminal address
↕	
00277	IBC for channel 17, current address
00400 thru 00477 and 00600 thru 00677	Control memory assigned to expanded ESI option when selected, otherwise assigned to main memory for instruction word and data storage.

(b) WORD TRANSLATORS. - Word translators decode contents of the S register slaves to locate selected memory address.

(c) DIGIT DRIVER AND R/W DIVERTERS. - Digit drivers perform the same function as inhibit circuits in the main memory. R/W diverters provide necessary drive currents for reading from or writing into the control memory cores.

(d) SENSE AMPLIFIERS. - Sense amplifiers detect bit-content of the addressed memory location and amplify detected signals to a level usable by the associated logic circuits.

(e) Z_0 REGISTER. - The Z_0 register supplies required storage for the input and output information from control memory.

1-4. PHYSICAL DESCRIPTION.

a. GENERAL CABINET. - The computer is housed in a single cabinet and is self-sufficient except for required input power and data signal lines. The standard computer cabinet (figure 1-2) is subdivided into four drawers, a power supply, two fan assemblies, and various panels necessary for operator-maintenance, control, and input/output connections. All drawers, chassis, and assemblies mounted within the control unit frame assembly may be removed for maintenance or repair if required.

An alternate cabinet configuration is supplied when 12 or 16 I/O channel option is selected with drawers A1 and A8 identical (figure 1-3). The alternate cabinet has one additional fan assembly.

The computer also has a remote console available that duplicates several of the control switches (figure 1-6). The remote console is connected to the computer by a standard I/O cable plugged into the special remote console jack.

b. COMPUTER ASSEMBLIES. - Three drawer assemblies contain the necessary logic circuitry for control of various computer instructions and transfers. The fourth drawer assembly contains computer core memory and associated circuitry. The power supply produces ac and dc voltages used throughout the control unit cabinet. Fan assemblies provide forced air cooling for cabinet drawers. A power control panel is provided to allow complete control of the computer from a single panel during turn-on and turn-off sequence. Audible and visual warnings indicate abnormal conditions.

(1) LOGIC DRAWERS. - Three logic drawers contain required circuitry to perform control and logic functions designated by the computer program. Indicators and switches located on the front of each drawer provide a visual display and manual control of circuit conditions.

(a) MOUNTING. - Each drawer is slide-mounted to allow easy access to the cabinet interior and to facilitate inspection and maintenance of drawer assemblies. Figure 1-10 pictures a drawer fully extended from the cabinet.

(b) DRAWER LOCKING. - Each logic drawer is held in place by a locking screw which, when loosened, permits the drawer to be extended approximately 26 inches from the cabinet. When the drawer is extended from the cabinet the electrical connections to the drawer are broken because the interassembly cable connectors are disconnected from their mating receptacles located on the rear of the cabinet frame.

(c) LOGIC CHASSIS. - Each of the logic drawers contains two vertically-mounted logic chassis, a front panel, and twelve connectors for interassembly cables. One side of each chassis contains printed circuit modules and the reverse side contains intrachassis wiring. The indicators and manual controls associated with the circuits on the chassis are mounted on the front panel of the drawer. The front panel is hinged to open and expose circuit test blocks. Figure 1-11 shows a typical logic chassis.

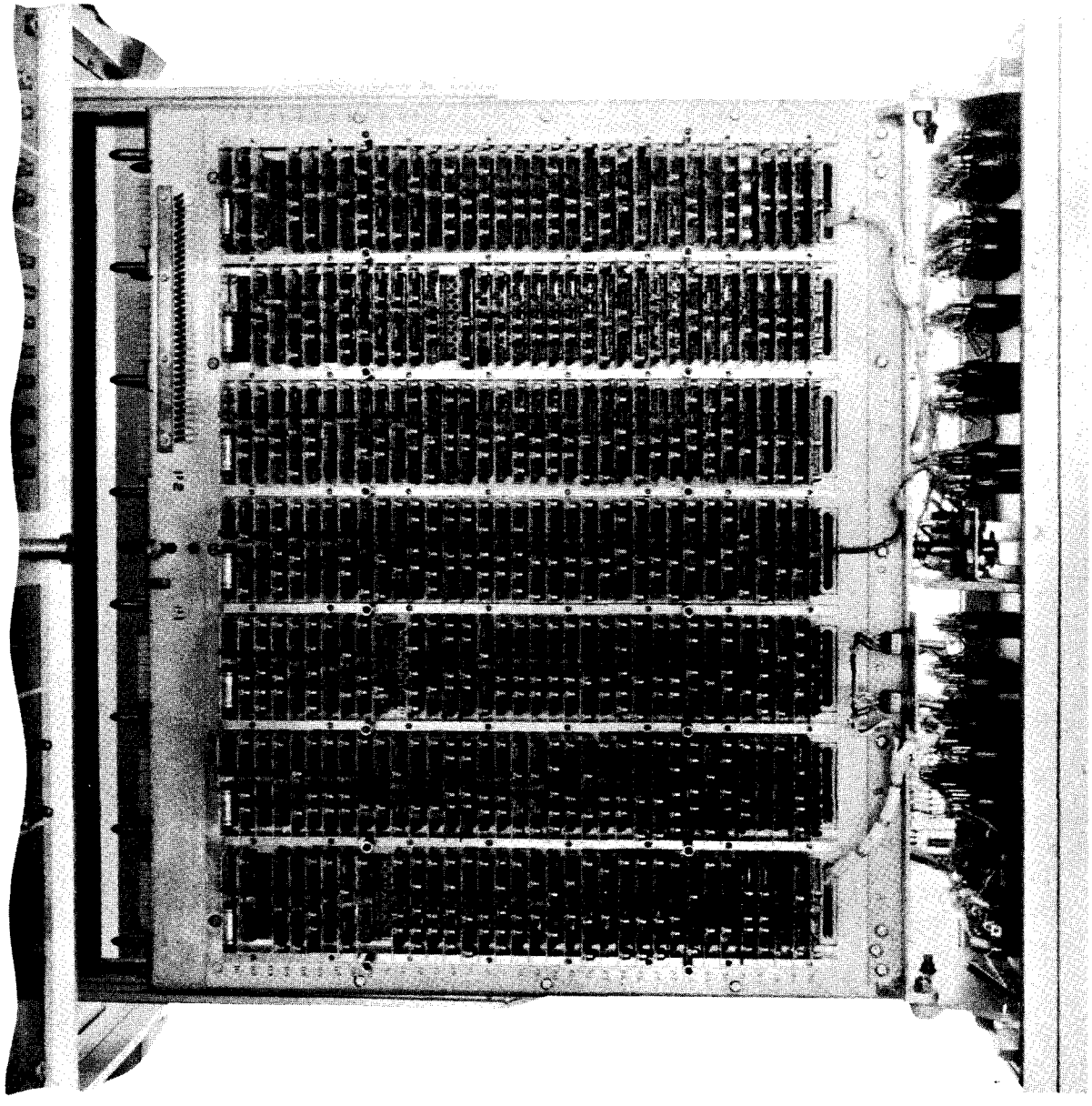


Figure 1-10. Logic Drawer (Extended)

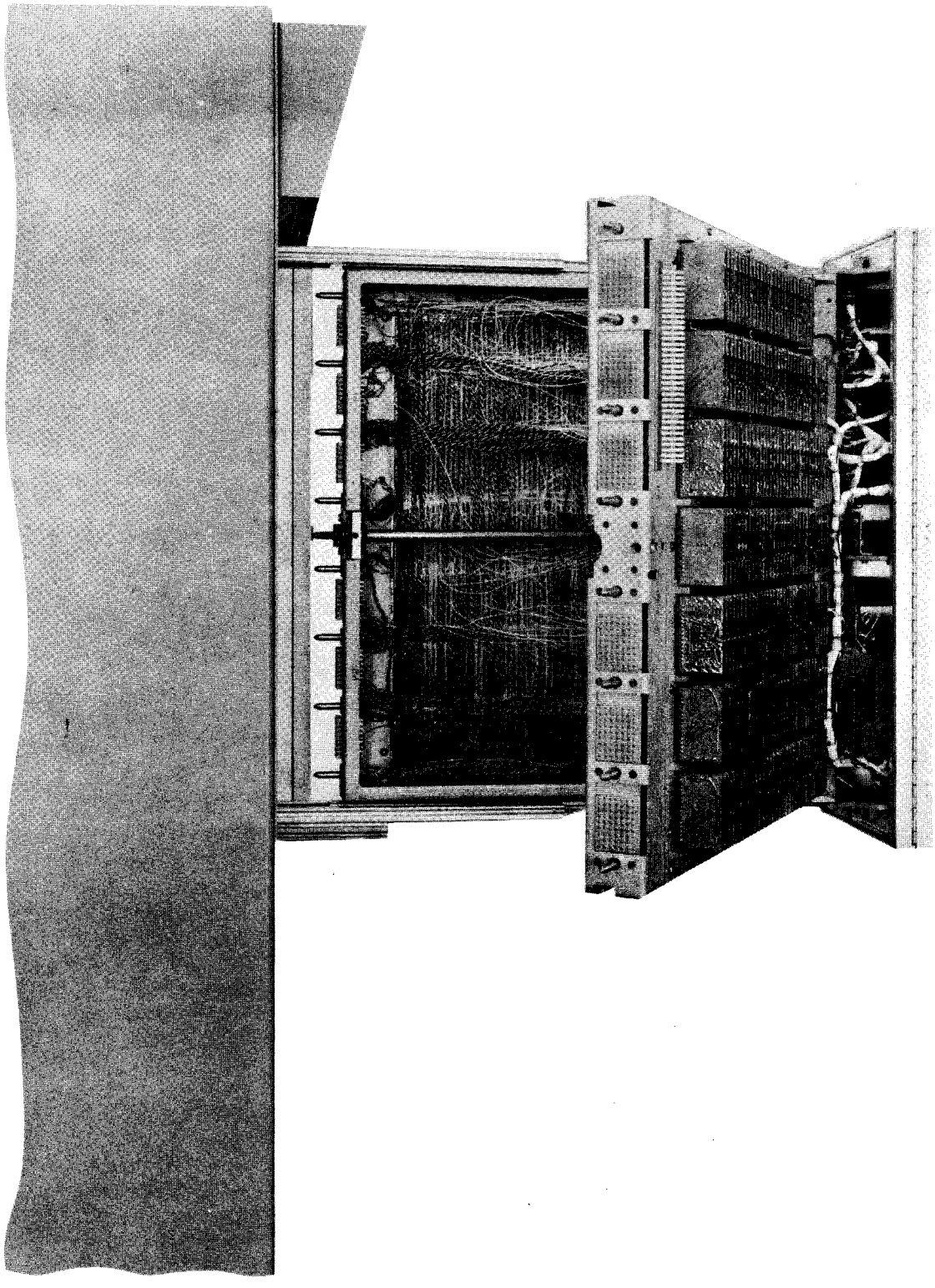


Figure 1-11. Typical Logic Chassis

(2) MEMORY DRAWER. - The memory drawer contains core memory stacks and associated circuitry to provide 18-bit word storage in the computer. A single memory drawer can house 16 core memory stacks for a maximum storage capacity of over 65 thousand 18-bit words. Figure 1-12 shows the location of memory stacks on the extended memory drawer. A main-memory stack is illustrated in figure 1-13.

(3) CONTROL AND BOOTSTRAP MEMORY LOCATION. - Control and bootstrap memories are located in drawer A4 and are identified in figure 1-14. Figure 1-15 illustrates the control memory stack; figure 1-16 illustrates the bootstrap memory assembly.

(4) POWER SUPPLY CHASSIS. - The power supply chassis contains main dc power supplies that provide the necessary dc voltage for computer logic functions. Figure 1-17 pictures the power supply chassis. Table 1-14 lists dc power supply outputs.

(5) MAIN MEMORY POWER SUPPLY. - An additional power supply is located on the main memory chassis and provides voltages required specifically for main memory operation. The voltages are listed in table 1-15.

(6) FAN ASSEMBLIES. - Three fan assemblies provide the required air circulation to cool the cabinet interior. Air is drawn in through the top of the cabinet and exhausted through the grill at the lower rear of the cabinet.

TABLE 1-14. DC POWER SUPPLY OUTPUTS

DC VOLTAGE	TOLERANCE	CURRENT (Max. Amp)
+15.0*	±10%	40.0
-15.0*	±10%	48.0
-4.50	±10%	29.0
±10.0 (Main Memory)	Adjustable from ±9.0 to ±11.0	0.2 for each 4K memory bank
±10.0 (Control Memory)	Adjustable from ±7.0 to ±11.0	6 amp peak
±15.0 (Control Memory)	Adjustable from ±13.5 to ±16.5	6 amp peak

* Absolute values of these two voltages may differ by not more than 6.0% of the lower voltage.

TABLE 1-15. MAIN MEMORY POWER SUPPLY OUTPUTS

DC VOLTAGE	TOLERANCE	CURRENT (Max. Amp)
+3.0	+2.9 to +3.1	8.0
-3.0	-2.9 to -3.1	0.5
-15.0	+13.5 to-16.5	20.0
+15.0	+13.5 to +16.5	20.0
+6.0	+5.7 to +6.3	15.0

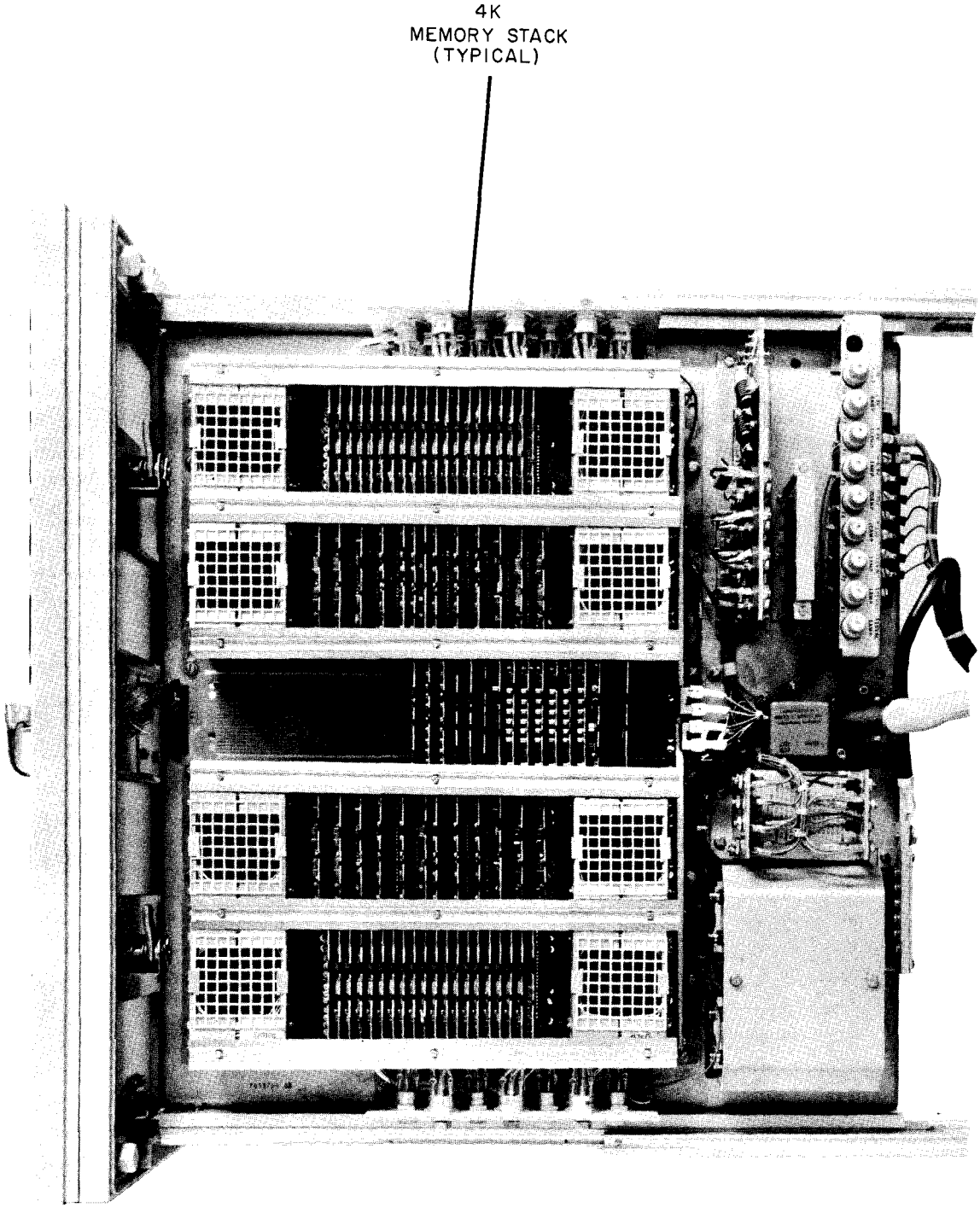


Figure 1-12. Main Memory Stack Locations (A3A2)

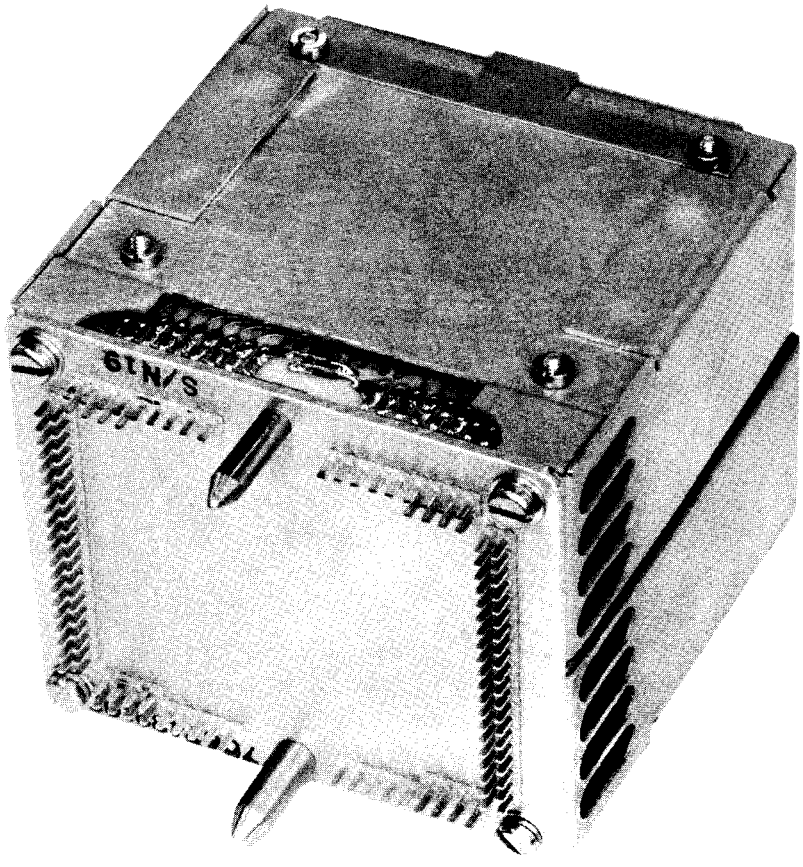


Figure 1-13. Typical Main Memory Stack

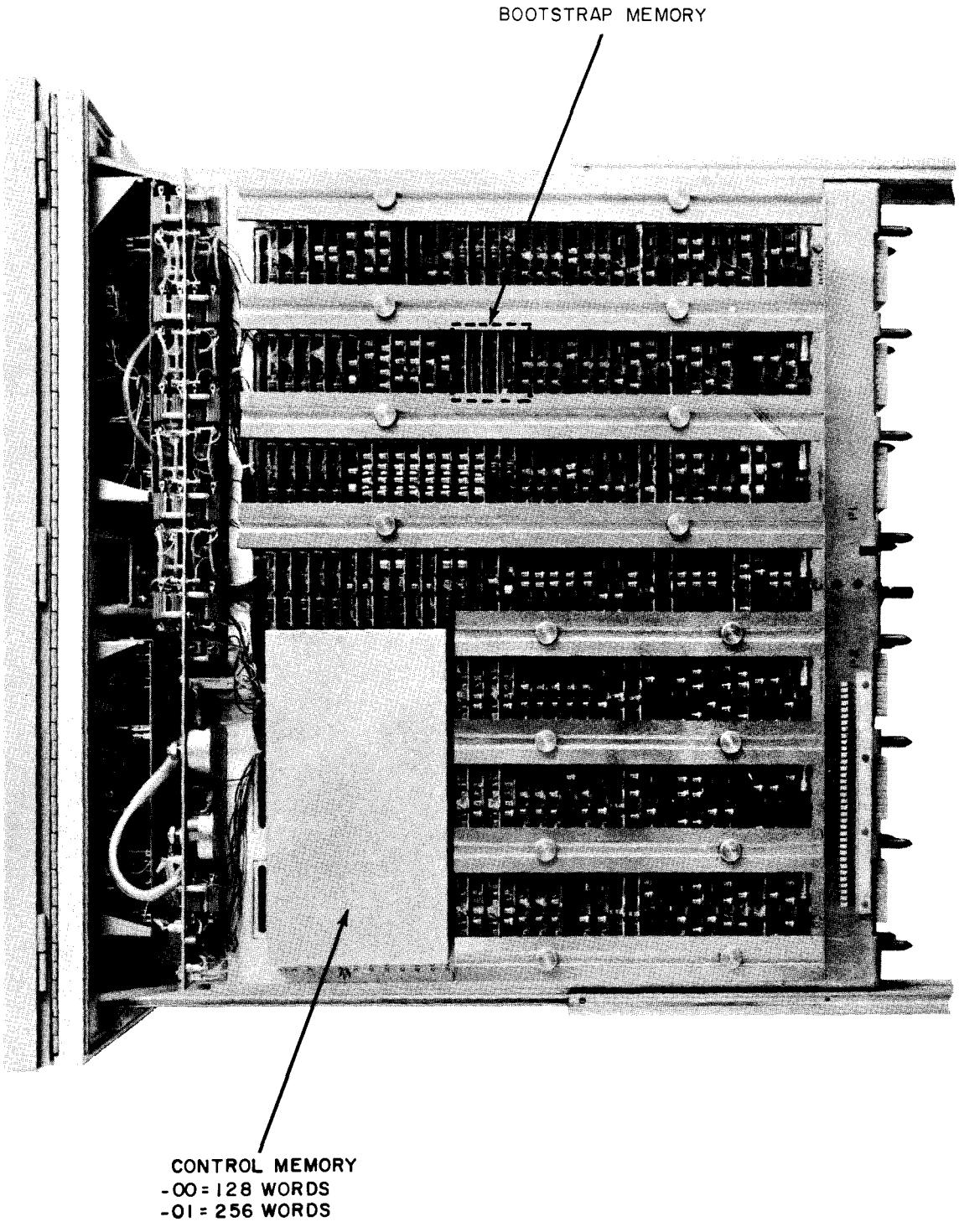
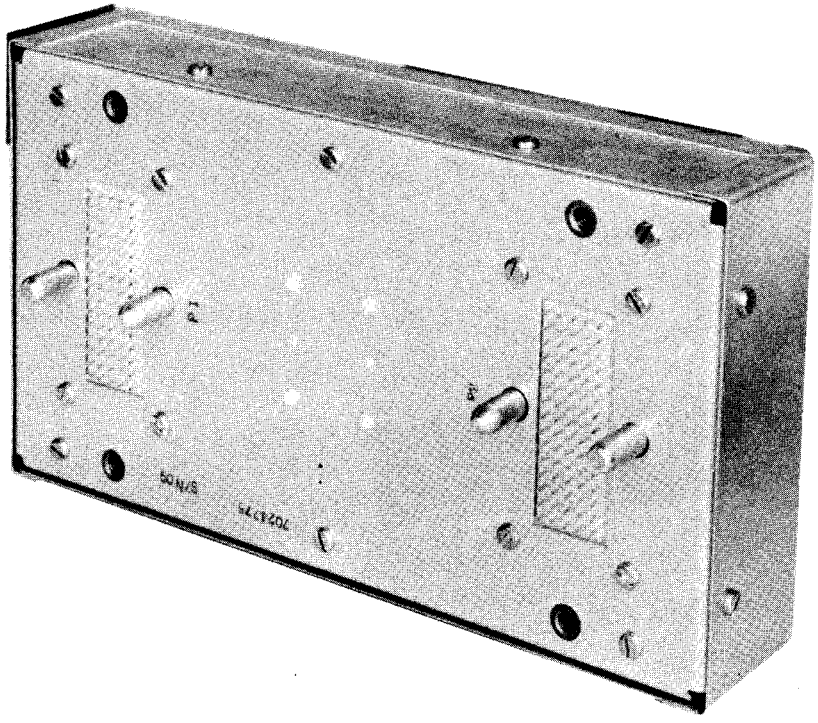
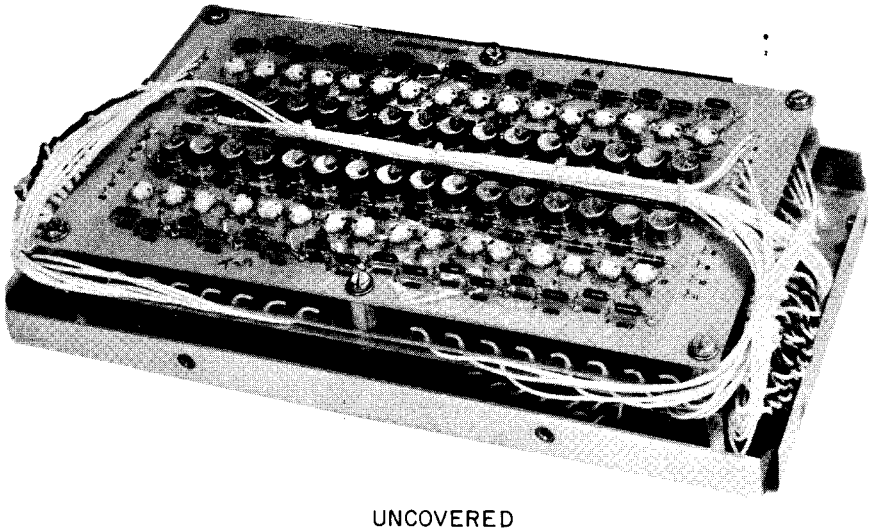


Figure 1-14. Bootstrap and Control Memory Drawer A4 Locations



COVERED



UNCOVERED

Figure 1-15. Control Memory Stack

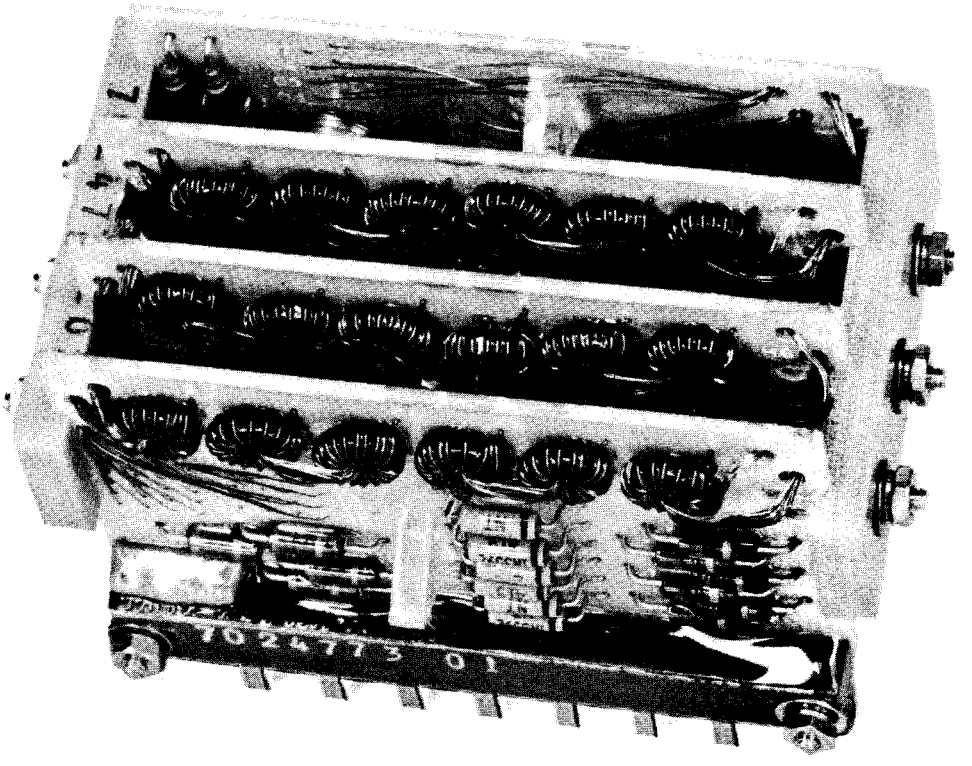


Figure 1-16. Bootstrap Memory Assembly

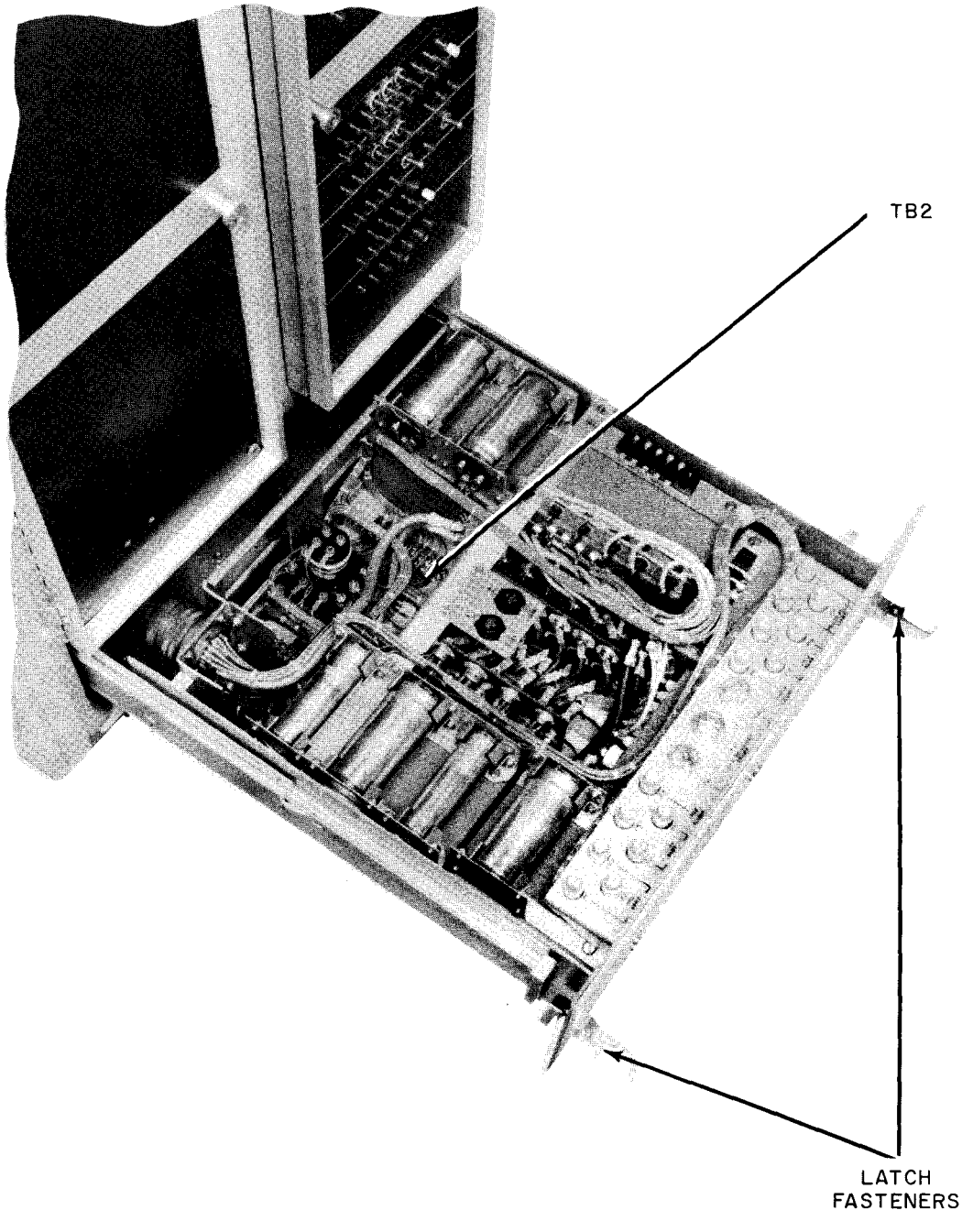


Figure 1-17. Power Supply Chassis

(7) PANELS. - The power control panel, (A5) in figure 1-18, provides electrical control of computer power, a visual display of computer operating conditions, and an audible alarm for signaling temperature irregularities. Switches and indicators for logic control are mounted on drawer front panels and provide manual control and allow proper sequencing during initial power application. The cable entry panel is located on the cabinet top and contains input and output connectors, remote control connector, and external synchronizing jack.

(8) ASSEMBLY DESIGNATIONS. - Figure 1-18 identifies various cabinet parts and computer assemblies.

(9) MODULE COMPLEMENT. - The printed circuit module is the basic replaceable unit of the computer and provides a mounting board for circuit components. The computer uses two basic types of modules. Type A, illustrated in figure 1-19, uses a 15-pin connector and contains from one to five circuits. Type B, figure 1-20, uses a 56-pin connector and contains from 1 to 16 circuits. For module types and quantities, refer to tables 1-16 and 1-17.

(10) FUSES, SWITCHES, AND RELAYS. - Fuses, power control switches and relays contained in the computer are listed in tables 1-18 and 1-19.

1-5. GLOSSARY OF TERMS.

Many terms which have an accepted meaning in the English language have a specific meaning when applied to computer operation and circuitry. This glossary is intended to delineate these terms and their specific meanings as they are written in this manual.

ABORT - A condition within the computer which results in the following sequential instruction being skipped or omitted.

ACCESS TIME - The time interval, characteristic of a memory or storage device, which exists between the instant information is requested and the instant this information is available to requesting circuitry.

ACCUMULATOR - A 36-bit addressable register, consisting of two 18-bit registers, AL and AU, used in arithmetic processes and commonly labeled the A register. A register is the principal arithmetic register and is used to hold sum, difference, product, or remainder during the final steps of arithmetic functions.

ACKNOWLEDGE - Indication of acceptance or issuance by the computer of signals on input or output lines to peripheral equipment. Abbreviated as ACK.

ADDER - A device which forms as an output the sum of two or more numbers presented as inputs. Related to the accumulator.

ADDRESS - A coded number specifically designating a computer register or a location within an internal storage device. Stored information is referenced by its address.

ADDRESSABLE - Capable of being referenced or entered by an address or instruction.

AND - A signal circuit with two or more input lines in which the output line supplies the desired signal only when all inputs are coincident signals. Synonomous with an AND gate and AND circuit.

ARITHMETIC - A section within the computer where arithmetic processes are performed and operands or results are temporarily stored.

AUXILIARY ROUTINE - A routine designed to assist in operation of the computer and in debugging other routines.

BINARY - A characteristic, property, or condition in which there are but two possible alternatives.

BINARY ARITHMETIC - A numbering system which uses two as its base and only the digits one and zero are recognized.

BINARY CELL - An information-storing element capable of two possible stable states.

BINARY NUMBER - A single digit or group of characters or symbols representing the total, aggregate, or amount of units by utilizing base two. Using the digits 1 and 0 to represent a quantity.

BINARY POINT - The radix point or root of the binary system.

BISTABLE - The capability of assuming either of two stable states; hence, capable of storing one bit of information.

BIT - An abbreviation of binary digit. A single character in a binary number representing the condition of a stage of storage within a computer. A unit of information capacity of a storage device.

BOOTSTRAP - A technique for loading the first group of instructions of a routine into storage; then using these instructions to load the remainder of the routine.

BOOTSTRAP MEMORY - A permanently wired, nondestructive readout memory containing the load routine for loading programs into storage. The program stored in nondestructive readout memory.

BORROW - An arithmetically negative carry; the additional subtraction of a one from the next partial difference. A borrow occurs in direct subtraction by raising the low order digit of the minuend by one unit of the next higher digit. A borrow occurs in binary subtraction when a digit of the minuend is a zero and the corresponding digit of the subtrahend is a one.

BUFFER - Transfer of data between the computer and peripheral equipments; intermediary storage between two data handling systems having different access times or formats.

BUFFER REGISTER - Final holding register for computer output to external devices or initial holding register for input to the computer; normally referred to as the C registers.

CAPACITY - Maximum size of a number that can be processed in the storage locations of a computer.

CARRY - A condition which arises in addition when the sum of two digits in the same digit place equals or exceeds the base of the number system in use; a digit to be added to the next digit column; the process of forwarding the carry digit.

CHASSIS - A divisional unit of the computer containing plug-in circuit cards and/or memory devices and the necessary wiring and test points for maintenance, assembly, and repair.

CHECKSUM - Sum used in a summation check.

CLEAR - To erase the contents of a storage device by replacing the contents with blanks or zeros. To reset a storage or memory device to the zero state. The signal used to perform the clear function such as master clear.

CLOCK - Basic timing or master timing device used to provide the basic sequencing pulses for the operation of the computer.

CODE - A system of symbols for meaningful communication; a machine language program.

CODED PROGRAM - Procedure for solving a given problem through use of computer logic. The coded program may vary in detail from a simple outline of the procedure to be followed to an explicit list of coded instructions.

COMPARE - To examine the representation of a quantity to discover its relationship to zero. To examine two quantities for the purpose of discovering identity or relative magnitude.

COMPILER LANGUAGE - A set of symbols used to abbreviate computer instructions and functions.

COMPLEMENT - A quantity expressed to the base N which is derived from a given quantity by a particular rule; frequently used to represent the negative of a given quantity. A complement on N, obtained by subtracting each digit of the given quantity from N-1, adding unity to the least-significant digit, and performing all resultant carrys. For example, the one's complement of 100011 is 011100; the nine's complement of 456 is 543.

CONTROL - Circuits within the computer which effect the completion of a function in the prepared sequence; the proper interpretation of an instruction and the issuance of proper commands to sequentially command computer logic to final completion of this interpretation.

CONTROL MEMORY - A storage device with assigned address locations used to hold information for control of computer logic operations.

COUNTER - A device capable of increasing or decreasing the value of its content upon receipt of coded input signals.

DEBUG - To isolate and remove all malfunctions from computer circuitry; to correct mistakes in a computer program or routine.

DIGIT - One of a set of numerical characters used as coefficients of powers of the radix in the positional notation of numbers.

ENABLE - (noun) A signal or pulse which allows other conditions to be acted upon; (verb) to apply the signal, to provide an enable signal.

EXECUTE - To perform indicated operations on specified operands.

FAULT - A condition which arises from the application of an illegal or improper signal; resulting from the detection of an improper or illegal condition.

FIXED POINT ARITHMETIC - A type of arithmetic in which operands and results of all arithmetic operations must be properly scaled so as to have a magnitude between certain fixed values. A method of calculation in which operations occur in an invariant manner and in which the computer does not consider the location of the radix point.

FLOW DIAGRAM - A graphical presentation of a sequence of events or operations; a flow chart.

FLOATING POINT ARITHMETIC - A form of number presentation in which quantities are represented by one number, the mantissa; multiplied by a power of the number base, the characteristic. A method of calculation which automatically accounts for location of the radix point.

FUNCTION CODE - That portion of the instruction word which specifies to the controlling logic the particular operation to be performed.

GATE - A circuit, which yields an output signal, that is dependent upon some function of its past or present input signals; AND gate or OR gate.

HALF-SUBTRACT - The bit-by-bit subtraction of two binary numbers with no regard for borrows, abbreviated HS. The complement for half-subtract is "half-subtract not" which is abbreviated $\overline{HS}$.

HARDWARE - The physical equipments or devices that comprise a computer and its associated peripheral units; contrasted with software.

HOLD - The function of retaining information in a storage device after this information has been transferred to another device; contrasted with clear.

INDEX REGISTER - A register which contains a quantity that may be used for address or operand modification; sometimes referred to as B register or B box. One of seven registers contained in control memory and used for operand and address modification during specific instructions.

INFORMATION - A collection of facts or other data as derived from the processing of data.

INPUT - Information or data transferred from, or to be transferred from, a peripheral device to internal storage of the computer. To transfer data or information into the computer.

INPUT/OUTPUT - A section within the computer which provides a method of communication with peripheral equipments, abbreviated I/O.

INPUT/OUTPUT REGISTERS - Registers within the computer that are used for the storage of information to be transferred from or transferred to the computer.

INSTRUCTION - A set of characters which defines an operation to be performed by the computer and contains the required addresses, operands, and other necessary information; same as instruction word.

INSTRUCTION DESIGNATORS - Those parts which constitute an instruction word and represented by the letters f, m, k, and y. The letter f designates format or function code; m, minor function code when applicable; k, modification designator; and y, operand address.

INSTRUCTION REPERTORY - The set of instructions which a computing system or data processing system is capable of performing.

INTERFACE - A common boundary between automatic data processing systems or between parts of a single system.

INTERNAL STORAGE - Storage facilities forming an integral physical part of the computer from which instructions and operands may be processed.

INTERRUPT - 1) Internal; an internally generated signal which indicates termination of an input or output buffer or acceptance of an external interrupt. 2) External; a signal from an external device which indicates an unusual condition which requires computer attention.

JUMP - An instruction or signal which, conditionally or unconditionally, specifies the location of the next sequential instruction and directs the computer to that instruction; used to alter the normal sequential control of the computer.

LEAST-SIGNIFICANT DIGIT - The first digit of a number counter from the right; the lowest-order digit of a number.

LOAD - To enter information into the storage area of a computer; to insert information into a register; to insert a program into a computer.

LOGIC - The systematic scheme which defines interactions of signals in the design of an automatic data processing system.

LOGICAL PRODUCT - Bit-by-bit multiplication of two binary numbers.

LOGICAL SUM - Bit-by-bit addition of two binary numbers with no regard for carrys; abbreviated LS. The complement of the logical sum is the "logical sum not", abbreviated $\overline{LS}$.

MAIN MEMORY - Core storage area of the computer used for normal word or program storage. That area of the computer used for instruction storage and for addressable operands.

MALFUNCTION - A failure in the operation of the hardware of a computer; failure or casualty in an equipment which degrades its operation or causes equipment to become inoperative.

MASK - A machine word that specifies which parts of another machine words are to be operated upon.

MASKING - The process of extracting a nonword group or a field of characters from a word or string of words.

MASTER CLEAR - To clear all normal storage locations of a computer prior to an operation. To set all major flip-flops to store a zero.

MASTER CLOCK - Primary timing signals within a computer. The source of primary timing signals.

MEMORY - A device into which information may be introduced, retained, and extracted for use at a later time.

MODE - A computer system of data presentation. A selected type of computer operation such as read or write mode.

MODIFY - To alter a portion of an instruction so its interpretation and execution will be other than normal. To alter a subroutine according to a defined parameter.

MODULE - An interchangeable plug-in item containing components. A printed circuit card upon which are mounted the electronic components.

MODULUS - The maximum quantity of permissible numbers that may be used in a process or system. The modulus for the group of numbers from -15 to +15 is 31.

MOST-SIGNIFICANT DIGIT - From left, the first digit of a number other than zero; the highest-order digit of a number.

NONADDRESSABLE - Pertaining to a storage location incapable of being referenced by an instruction word.

NONDESTRUCTIVE READOUT - A memory device that stores information which has been preset at manufacture and cannot be changed or altered; reading information from a memory device that does not destroy the contents of the device; a reading of information from a register without changing that information within the register.

NONVOLATILE STORAGE - Storage mediums such as magnetic tapes, drums, cores, and discs, which retain information in the absence of power, and may be made available upon restoration of that power.

NUMBER - The total, aggregate, or amount of units; a figure or word, or a group of figures or words used to graphically represent an arithmetic sum or total.

OCTAL NUMBERS - A numbering system using eight symbols, 0 through 7, as its base; numbers in which the base has been set at eight.

OPERAND - A quantity entering or arising in an instruction; an argument, result, parameter, or indication of the location of the next instruction; the address portion of an instruction.

OPERATION - A defined action; action specified by a single computer instruction or group of instructions.

OPERATOR - A mathematical symbol which represents an arithmetic process to be performed upon an operand. One who operates the computer.

OUTPUT - A transfer of information from the internal storage system of the computer to peripheral devices or external storage; the process of an information transfer from the computer.

OVERFLOW - The condition that arises when the result of an arithmetic operation exceeds the capacity of the allotted storage area; overcapacity; information contained in an item which is in excess of a given or stated amount.

PAPER TAPE READER - A device capable of sensing information punched on a paper tape in the form of a series of holes. A photoelectric readout device, abbreviated PT Reader.

PARALLEL - To handle simultaneously in separate facilities; to operate on two or more parts of a word or item simultaneously; contrasted with serial.

PARALLEL TRANSFER - To transfer characters of a word simultaneously over separate lines.

PARTIAL CARRY - Execution of the carry process in which carrys that arise as a result of a carry are not transmitted to the next higher stage.

PARITY BIT - A bit, normally a one, that may be added to a word to insure the total number of ones in that word is odd.

PARITY CHECK - The process of checking the number of ones contained in a given word or group of words or instructions.

PASS - A complete cycle of reading, processing, and writing. A complete machine operation or run.

PERIPHERAL EQUIPMENT - Auxiliary machines placed under control of the central computer. Equipments used by, and in conjunction with, the main computer system.

POSITIONAL NOTATION - A method of expressing a quantity, using two or more figures wherein the successive right to left figures are interpreted as coefficients of ascending integer powers of the radix.

PRECISION - The degree of exactness with which a quantity is stated; the degree of discrimination or detail.

PRESET - To set contents of a storage location to an initial value.

PROGRAM - A complete sequence of machine instructions, routines, and operands necessary to solve a problem.

RADIX - The number of individual characters used in a numbering system; radix for the decimal system is ten; radix for the octal system is eight; radix for the binary system is two.

RADIX POINT - The period that separates the integer digits from the fractional digits of a number of the digital position involving the zero exponent of the radix from the digital position involving the minus-one exponent of the radix. The decimal point for the decimal system; the octal point for the octal system; or the binary point for the binary system.

RANDOM ACCESS - Pertaining to the process of obtaining information from or placing information into storage where the time required for such access is independent of the location of the information most recently obtained or placed in storage.

READ - To sense information; to extract information, usually from a memory location.

READER, CARD - A device capable of recognizing information in the form of holes punched in a card.

READER, MAGNETIC TAPE - A device capable of reading information recorded on magnetic tape in the form of magnetized dots.

READER, PAPER TAPE - (See paper tape reader).

REAL TIME - A measurement of elapsed time relative to a specific time or event.

REAL-TIME CLOCK - An oscillator and the associated circuitry capable of recording elapsed time measured in minutes, seconds, milliseconds, or other fractions of actual time periods.

REGISTER - A number of bistable stages used for holding or storing information. The number of stages determines the modulus of the number system which may be represented by the computing system; an addressable storage location. (See definition of accumulator, buffer register, index register, input/output register).

REPERTOIRE - Instructions or functions capable of being executed by the computer; repertoire of instruction (See definition of instruction repertory).

RESET - To clear; to set to zero; to return a device to zero or to an initial or arbitrarily selected value.

RESUME - The input acknowledge signal generated by a receiving computer upon completion of sampling input information lines.

RISE TIME - Time required for the leading edge of a generated or transmitted pulse to rise from one-tenth to nine-tenths of its final or terminal value. Rise time is proportional to the time constant of the circuit.

ROUTINE - A set of coded instructions arranged in proper sequence to direct the computer to perform a desired operation or sequence of operations. Subdivision of a program consisting of two or more functionally related instructions.

SCALE - To shift a binary number either right or left in a register to retain the number for future computations or for later storage within the computer.

SCALE FACTOR - Coefficients used to multiply or divide quantities in a problem so they fall within a given range of magnitude such as from +1 to -1.

SCAN - A cycle or sequence which routinely interrogates all requests and interrupts; to determine priority for real-time clock; input and output on a basis of channel number and type of request.

SENSE - To examine relative to a criterion; to read information from magnetic cores.

SEQUENCE - An orderly progression of items of information or of operations in accordance with set rules.

SERIAL - One at a time; pertaining to time-sequential transmission.

SERIAL TRANSFER - To transfer words of information or bits of a word in a serial manner; to transmit bits of a word or elements of information in succession over a single line; contrasted with parallel transfer.

SET - To place a binary cell or flip-flop in the state of storing a one; to change the state of a storage device to output a value other than zero.

SHIFT - To move characters of a unit of information columnwise left or right; to multiply or divide a number by a power of the base of notation; to move information left or right in the arithmetic section of a computer.

SHIFT REGISTER - A computer register in which the contents may be shifted either left or right.

SIGN - A symbol that distinguishes negative quantities from positive quantities.

SIGN BIT - Sign digit; bit used to designate the algebraic sign of a number.

SIGNIFICANT DIGITS - A set of digits from consecutive columns beginning with the most-significant digit other than zero and ending with the least-significant digit whose value is known and considered relevant.

SINGLE ADDRESS CODE - Consisting of instructions containing a coded representation of the operation to be performed and a single address of a word in storage or an operand. The instructions of the single address code contain a maximum of one address for reference in storage.

SOFTWARE - The totality of programs and routines used to extend capabilities of computers; programs and routines such as compilers, assemblers, narrators, routines, and subroutines.

STORAGE - Pertaining to a device in which information may be placed and retained for future use; synonymous with memory.

SUBROUTINE - A set of instructions necessary to direct the computer to perform a well defined mathematical or logical operation; a subunit of a routine such as multiply or divide subroutine.

TAG - A unit of identification whose composition differs from that of the other members of a set so that it can be used as a marker or label.

TRANSFER - Conveyance of control from one mode to another by means of instructions or signals; conveyance of data from one place to another.

TRANSLATE - To change information from one form of representation to another without significantly affecting the meaning; to transform.

TROUBLESHOOT - To search for the cause of a malfunction or erroneous program behavior to isolate and correct the malfunction or error.

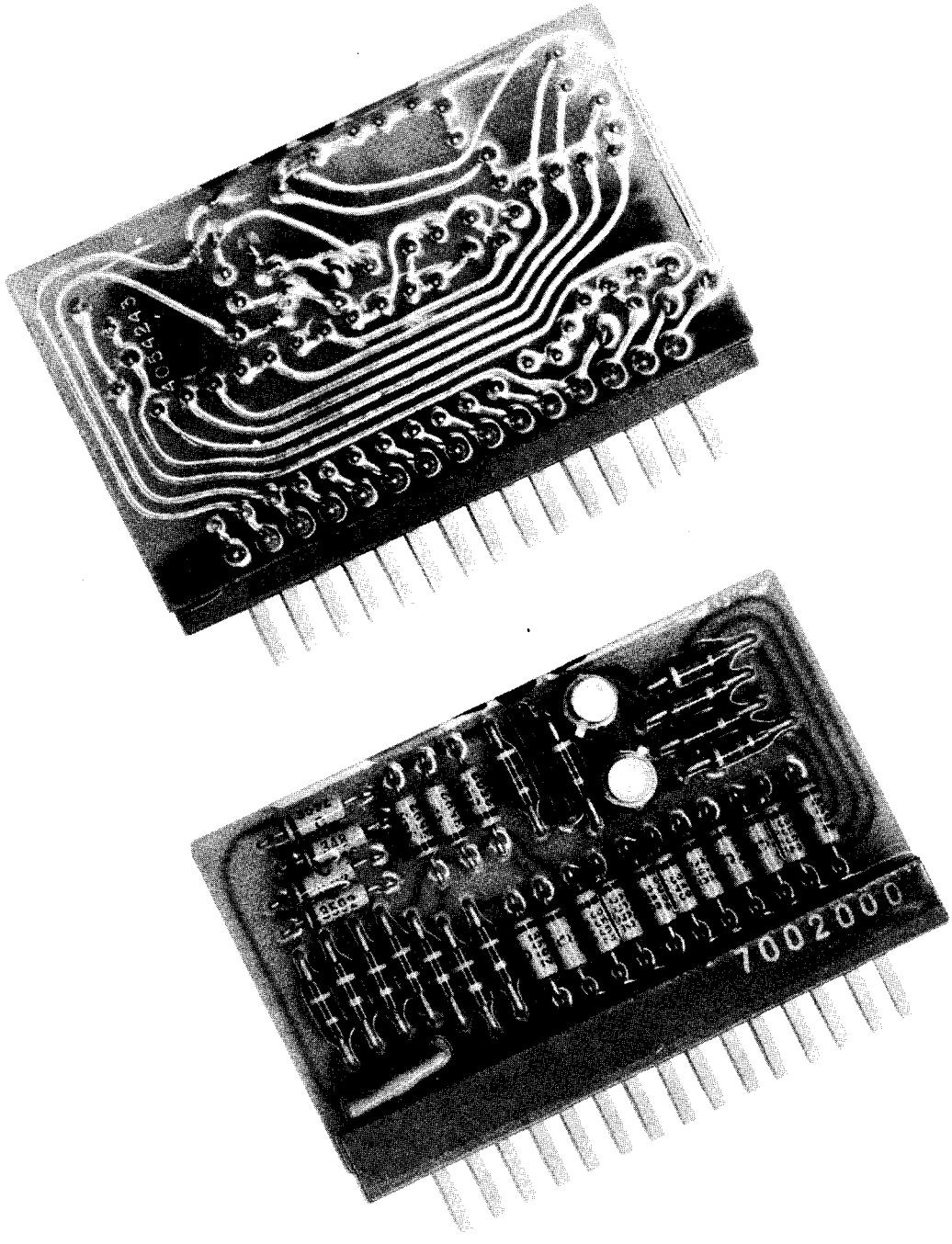


Figure 1-19. Printed Circuit Module, Type A

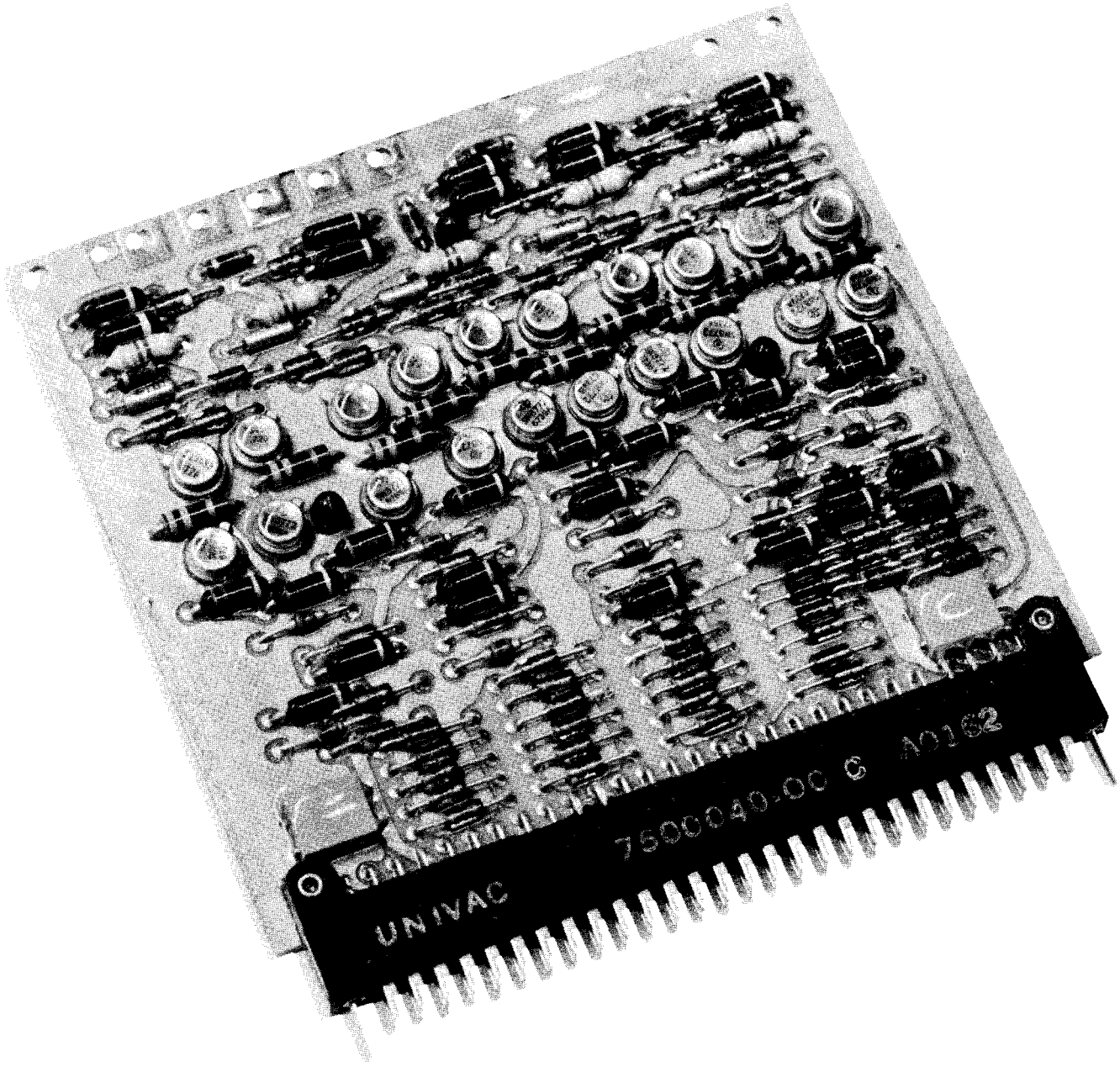


Figure 1-20. Printed Circuit Module, Type B

TABLE 1-16. PRINTED CIRCUIT MODULE COMPLEMENT, LOGIC CHASSIS

PART NO.	DESCRIPTION	CHASSIS						TOTAL
		A1	A2	A3	A4	A7	A8	
7000210	Pulse-Delay Oscillator	-	-	1	-	-	-	1
7002000	Flip-Flop	-	-	-	36	41	26	103
7002013	Driver-Amplifier	16	16	31	21	24	18	126
7002020	Flip-Flop	16	16	15	1	36	2	86
7002030	Inverter	26	25	9	8	8	10	85
7002040	Inverter	6	3	10	37	2	8	66
7002050	Inverter	10	10	19	35	16	24	114
7002060	Inverter	19	19	58	8	34	7	145
7002070	Inverter	15	14	27	16	14	10	96
7002080	Inverter	1	1	4	1	2	1	10
7002090	Input Amplifier	44*	44*	3	-	6***	-	97* 8*
7002100	Driver Amplifier	-	-	-	-	3	-	3
7002120	Driver Amplifier	-	-	1	-	-	1	2
7002130	Driver Amplifier	12*	12*	-	-	-	-	24*
7002140	Driver Amplifier	18*	18*	-	-	-	-	36*
7002160	Inverter	-	-	2	-	4	1	7
7002220	Inverter	-	-	-	2	1	1	4
7002321	Differential Amplifier	44*	44*	-	-	1*	-	89*
7002331	Control Line Amplifier	12*	12*	-	-	-	-	24*
7002341	Data Line Amplifier	18*	18*	-	-	-	-	36*
7002730	High Speed Selector	1**	1**	-	-	-	-	2**
7002861	Voltage Regulator	-	-	-	-	-	1	1
7002880	Voltage Regulator	-	-	-	-	1	-	1
7002900	Flip-Flop	16	17	15	41	10	9	108

TABLE 1-16. PRINTED CIRCUIT MODULE COMPLEMENT, LOGIC CHASSIS (CONT.)

PART NO.	DESCRIPTION	CHASSIS						TOTAL
		A1	A2	A3	A4	A7	A8	
7002920	Inverter	4	4	19	29	1	8	65
7002930	Flip-Flop	21***	21***	12	-	6	2	62
7003180	Capacitor Assembly	5	5	7	7	7	7	38
7003480	Time Delay	4**	4**	-	-	-	-	8
7003490	Driver Amplifier	-	-	1	-	-	2	3
7003600	Regulator Amplifier	-	-	-	-	-	1	1
7003621	Memory Driver	-	-	-	-	-	9	9
7003630	Pulse Delay Network	-	-	3	-	-	-	3
7003640	Emitter Follower	-	-	1	-	-	4	5
7003670	Driver Amplifier	-	-	-	-	-	4	4
7003680	Transformer Driver	-	-	-	-	-	4	4
7003710	Pulse Delay Network	-	-	-	-	-	2	2
7003720	Voltage Sensor	-	-	-	-	1	-	1
7003730	Regulator Amplifier	-	-	-	-	-	1	1
7003740	Control Amplifier	-	-	-	-	-	6	6
7003760	Current Diverter	-	-	-	-	-	2	2
7003771	Driver Amplifier	-	-	-	-	-	6	6
7003780	Driver Amplifier	-	-	-	-	-	18	18
7003850	Sense Amplifier	-	-	-	-	-	6	6
7104010	Selector Mode	-	-	-	-	1	-	1
7109000	Resistor Assembly	1	-	-	1	1	-	3
7109010	Resistor-Capacitor Assembly	-	1	-	1	1	-	3
						Total (See Note 1)		1368

TABLE 1-16. PRINTED CIRCUIT MODULE COMPLEMENT, LOGIC CHASSIS (CONT.)

(*) Used for Slow Interface

(**) Removed for Slow Interface

* Used for Fast Interface

** Removed for Fast Interface

*** One 2930 removed for Fast Interface, Chassis A1 and A2

(***) One 2090 replaced by 2321 on Chassis A7 for Fast Interface

NOTE 1 - Nominal Value Because of Customer Options

TABLE 1-17. MEMORY CHASSIS PRINTED CIRCUIT MODULE COMPLEMENT

PART NO.	DESCRIPTION	MEMORY CAPACITY			
		16K	32K	48K	65K
7500040	Driver Amplifier	3	4	7	8
7500260	Oscillator, Delay Line Amplifier	1	1	2	2
7500280	Emitter Follower	1	1	2	2
7500340	Voltage Sensor	1	1	2	2
7500400	Memory Switch, Bipolar	6	11	17	22
7500420	Drive Diverter	2	4	6	8
7500430	Transformer Assembly	4	8	12	16
7500650	Sense Amplifier	18	36	48	72
7500660	Capacitor-Diode Assembly	2	2	4	4
7500670	Capacitor Assembly	1	1	2	2
7500760	Level Changer - Amplifier	6	6	12	12
7500780	Voltage-Current Regulator	2	2	4	4
7500900	Driver Amplifier	2	2	4	4

TABLE 1-18. FUSE COMPLEMENT

DRAWER	FUSE	RATING (AMPS)
A1, A8 or (I/O drawer)	F1, F4	5
	F2, F5	12
	F3, F6	4
A2 (Control)	F1	8
	F2	10
	F3	5
	F4	6
	F5	12
	F6	4
A3 (Memory drawer)	First 16K / Second 16K	
	F1 / F4	3
	F2 / F5	6
	F3 / F6	15
A4 (Control)	F1, F4	6
	F2	12
	F3	3
	F5	8
	F6	5
PS1 (Power supply)	F1, F2, F3	5 (16K) +1 amp/additional 16K
	F4, F5, F6	1.5 (32K)
	F7, F11	6 (32K)
	F8, F9, F10	12 (16K) +3 amps/additional 16K
	F12, F13, F14	4 (16K) +1 amp/additional 16K
	F15, F16, F17	2 (8 I/O) +1 amp/additional 8 I/O

TABLE 1-19. POWER CONTROL SWITCHES AND RELAYS

RELAY OR SWITCH DESIGNATOR	NAME	FIGURE NO.
PSIK1	Power control relay	9-178
A5S1	Indicate-indicate/set switch	9-176
A5S2	Battle short switch	9-176
A5S3	Alarm disconnect-reset switch	9-176
A5S4	Power on-off switch	9-176
A12S1	Power supply interlock switch	9-177
A12S2	115° Temperature alarm switch	9-177
A12S3	140° Overtemperature switch	9-177
A12S4	115° Temperature alarm switch	9-177
A12S5	140° Overtemperature switch	9-177

SECTION 2

INSTALLATION

2-1. METHOD OF PACKING AND SHIPPING.

Normally, the computer is shipped by van line, in which case the computer will arrive at the site uncrated. When the computer is shipped by other means of transportation, or to an overseas installation, the computer will arrive at the site packed in a plywood shipping crate.

In either case, the computer is shipped with foam rubber pads taped to the corners of the cabinet to prevent damage to the equipment during loading, unloading, and transit. For additional protection, a vinyl bag is placed over the cabinet and sealed at the base to protect the equipment from dust, dirt, and moisture. A skid is bolted to the bottom of the cabinet for further protection and to permit the use of a forklift truck when handling or moving the computer.

2-2. UNPACKING INSTRUCTIONS.

The following unpacking instructions apply when the computer is received from the factory in a shipping crate. If the computer arrives uncrated, omit steps 1 through 4.

STEP 1. Remove all fasteners (screws, nails metal bands,) from top of shipping crate.

STEP 2. Lift off and remove top section of the crate.

STEP 3. Pry loose and pull away four sides of crate to expose equipment.

STEP 4. Remove all packing material (such as shredded paper) from around computer.

STEP 5. Remove vinyl bag covering computer; remove tape and protective padding from corners of cabinet.

STEP 6. Visually inspect equipment for scratches, dents, and other evidence of shipping damage. Make a note of all shipping damage and report it immediately.

STEP 7. Using a forklift truck move computer to general area where it is to be installed.

STEP 8. Remove bolts, which hold equipment to shipping skid; lift or slide computer from skid.

STEP 9. Check cables, test equipment, and spare parts received against shipping invoice for proper type and number; report all discrepancies.

STEP 10. Place computer in area specified on installation layout drawing.

2-3. PLACEMENT OF THE COMPUTER.

The computer is a self-contained unit measuring approximately 72 inches high, 31 inches deep, and 26 inches wide (38 inches wide if the computer includes the additional half cabinet). The exact placement of the computer at the site is largely at the discretion of the user with no unusual restrictions governing the choice of a location. However, there are certain factors to consider when

choosing a location. These factors are protection and drainage, clearance, cabling, power, cooling, and installation requirements.

a. PROTECTION AND DRAINAGE. - The computer requires no auxiliary structures. However, the selected location must provide protection against possible damage and excessive dust, moisture, and standing water. Also, the area must be large enough to ensure that heat generated by the equipment will be properly dissipated.

b. CLEARANCES. - The selected area must provide space for the computer with sufficient clearance around the cabinet to permit the unrestricted movement of personnel and test equipment. The minimum clearances required are: front - 39 inches, rear - 10 inches, sides (door clearance) - 8 inches each side, and top - 12 inches.

The 10-inch clearance at the rear of the cabinet is needed to ensure proper air circulation and heat dissipation. The 12-inch clearance above cabinet is required to facilitate signal cable connections. The 39-inch clearance at the front of the cabinet provides the space needed for chassis extension, inspection, testing, and parts removal and replacement. Figure 2-1 illustrates the clearance requirements.

c. CABLING RESTRICTIONS. - When selecting a location for the computer, consideration must be given to the location of the peripheral equipment with which the computer will operate. Generally, the computer should be located close to the peripheral equipment unless a given application requires otherwise.

The maximum distance between a peripheral device and a computer with the slow interface option is 300 feet when the signal cables used are balanced, twisted-pair, shielded cables having a maximum capacitance of 20 picofarads. The maximum distance between a peripheral device and a computer with the fast interface option is 50 feet when the signal cables used are balanced, twisted-pair, shielded cables having a minimum characteristic impedance of 120 ohms.

All I/O cables connect to the cable entry panel. This panel is located in the top interior of the cabinet directly below the cover (figure 2-2). The power cable connects to the power entry jack A14J1 on the top of the computer.

d. POWER REQUIREMENTS. - The air-cooled computer requires a 115-volt ($\pm$1%) line-to-line (line-to-neutral, optional), 3-phase, 400-cycle ($\pm$5%), 1800-watt, (4-drawer computer), 3200-watt (6-drawer computer), alternating current power source.

Power is cabled from the source through a junction box or control panel to the computer via a four-conductor cable. The cable consists of three phase wires and neutral wire. (The cable connects to jack A14J1, located on the top of the cabinet and shown in figure 2-2.)

e. COOLING REQUIREMENTS. - The computer system requires 400 cubic feet of cooling air per minute at 32°F (0°C) to 122°F (50°C) for a 4-drawer unit, or 610 cubic feet of air per minute at 32°F (0°C) to 122°F (50°C) for a 6-drawer unit.

f. INSTALLATION REQUIREMENTS. - The type of installation, mobile or stationary, determines the method of installing the computer. When used in a stationary

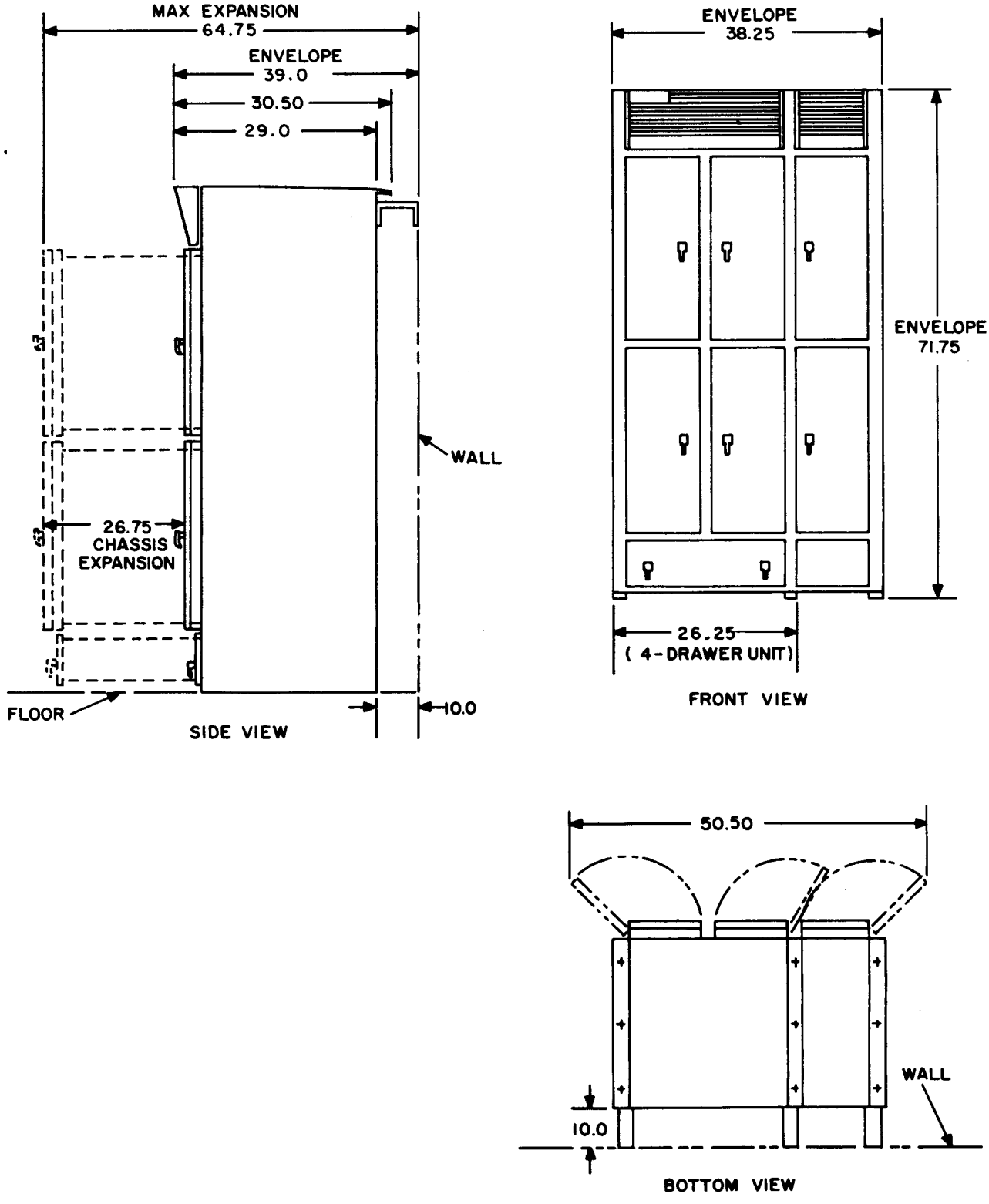


Figure 2-1. Computer Clearance Requirements

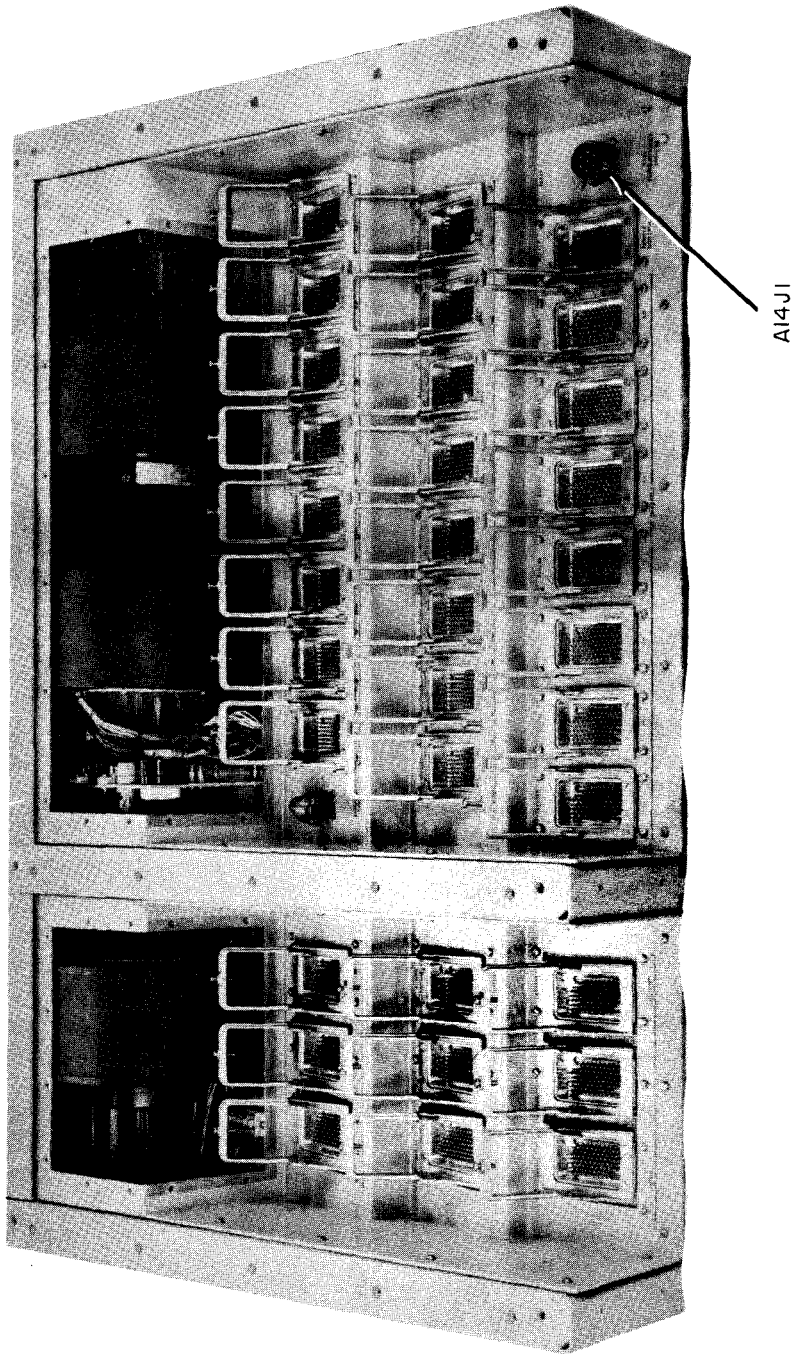


Figure 2-2. Location and Access to Cable Entry Panel

installation, the computer must be bolted to the floor to prevent the cabinet from tipping forward when the pull-out drawers are extended. When used in a mobile installation, the computer must be bolted to the floor and to a wall. The stabilizers needed to fasten the computer to the wall are provided at the rear of the cabinet.

Figure 2-3 is an outline dimensional drawing showing the location of the mounting holes in the base and at the rear of the cabinet.

2-4. CABLING INSTRUCTIONS.

a. POWER CABLE. - The power cable is a four-wire cable consisting of three phase wires and a neutral wire. Before connecting the power cable to either the power source or the computer, check all wires in the cable with an ohmmeter for continuity and short circuits. Then connect the cable as follows.

CAUTION

Before proceeding with step 1, check to ensure power is off and power supply to which the cable will be connected is dead.

STEP 1. Prepare the cable for fastening to the jack at the back of the computer. (For computer serial number 1, remove the top protective plate from the cabinet.)

STEP 2. Remove the plug from jack A14J1.

STEP 3. Open the jack and connect the neutral wire to pin D, then connect the three phase wires to pins A-Ø1, B-Ø2, and C-Ø3.

STEP 4. Connect the other end of the cable to the designated terminals at the control panel.

STEP 5. Verify all connections at A14J1 and at the power supply.

STEP 6. Perform the initial power checks according to paragraph 2-6b.

b. I/O SIGNAL CABLES. - The number of I/O signal cables that connect to the computer is dependent upon the I/O capability of the computer. Each I/O channel requires two 90-conductor (45 twisted-pair lines) cables; one is an input cable, the other an output cable. Thus, eight cables are required for a four-channel computer, sixteen cables for an eight-channel computer, twenty-four cables for a twelve-channel computer, and thirty-two cables for a sixteen-channel computer. An additional 90-pin jack at the top of all computers is supplied for remote control of the computer.

In addition to the I/O signal cables, a single three-conductor cable can be connected to the computer. This is a special cable used to connect the computer to an external synchronizing device.

The external synchronizing cable and all I/O signal cables connect to the computer at the cable entry panel. Cable connections are made as indicated in table 2-1.

Table 2-2 shows the pin assignments for the input/output cables connecting to the peripheral devices (connectors J1 through J16 and J21 through J36). Table 2-3 shows the pin assignments for the signal cable connecting to the remote console (connector J17) and external synchronizer (connector J18).

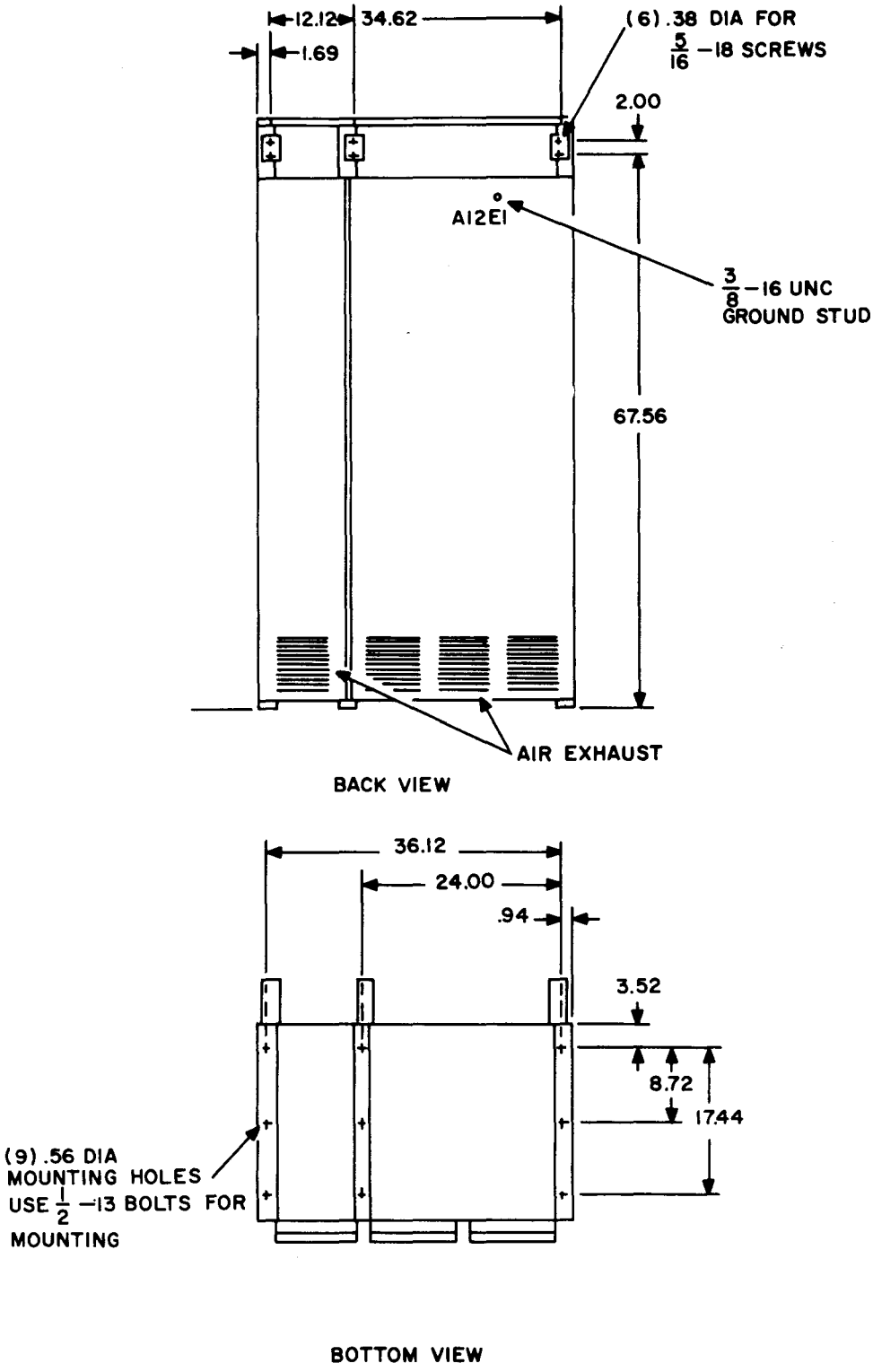


Figure 2-3. Location of Cabinet Mounting Holes

TABLE 2-1. I/O SIGNAL CABLE CONNECTIONS

COMPUTER CONNECTOR NO.	CABLE	COMPUTER CONNECTOR NO.	CABLE
J1	Channel 6-input	J18	External sync
J2	Channel 5-input	J21	Channel 12-input
J3	Channel 4-input	J22	Channel 11-input
J4	Channel 3-input	J23	Channel 10-input
J5	Channel 2-input	J24	Channel 15-input
J6	Channel 1-input	J25	Channel 14-input
J7	Channel 0-input	J26	Channel 13-input
J8	Channel 6-output	J27	Channel 17-input
J9	Channel 5-output	J28	Channel 16-input
J10	Channel 4-output	J29	Channel 17-output
J11	Channel 3-output	J30	Channel 16-output
J12	Channel 2-output	J31	Channel 15-output
J13	Channel 1-output	J32	Channel 14-output
J14	Channel 0-output	J33	Channel 13-output
J15	Channel 7-input	J34	Channel 12-output
J16	Channel 7-output	J35	Channel 11-output
J17	Remote console	J36	Channel 10-output

TABLE 2-2. CABLE CONNECTOR PIN ASSIGNMENTS (J1-J16, J21-J36)

PIN NO.	INPUT CONNECTOR PIN DESIGNATION	OUTPUT CONNECTOR PIN DESIGNATION
01	Input data request	Output acknowledge
02	Input data acknowledge	Output data request
03	External interrupt request	External function acknowledge
04	Spare	External function request
05	2^{32*}	2^{32*}
06	2^{33*}	2^{33*}
07	2^{34*}	2^{34*}
08	2^{35*}	2^{35*}
09	2^{0}	2^{0}
10	2^{1}	2^{1}
11	Input data request (R)	Output acknowledge (R)

TABLE 2-2. CABLE CONNECTOR PIN ASSIGNMENTS (J1-J16, J21-J36) (CONT)

PIN NO.	INPUT CONNECTOR PIN DESIGNATION	OUTPUT CONNECTOR PIN DESIGNATION
12	Input data acknowledge (R)	Output data request (R)
13	External interrupt (R)	External function acknowledge (R)
14	Spare (R)	External function request (R)
15	2^{32}(R)*	2^{32}(R)*
16	2^{33}(R)*	2^{33}(R)*
17	2^{34}(R)*	2^{34}(R)
18	2^{35}(R)*	2^{35}(R)*
19	2^{0}(R)	2^{0}(R)
20	2^{1}(R)	2^{1}(R)
21	Not used	Not used
22	2^{2}	2^{2}
23	2^{3}	2^{3}
24	2^{4}	2^{4}
25	2^{5}	2^{5}
26	2^{6}	2^{6}
27	2^{7}	2^{7}
28	2^{8}	2^{8}
29	2^{9}	2^{9}
30	2^{10}	2^{10}
31	2^{11}	2^{11}
32	2^{12}	2^{12}
33	2^{2}(R)	2^{2}(R)
34	2^{3}(R)	2^{3}(R)
35	2^{4}(R)	2^{4}(R)
36	2^{5}(R)	2^{5}(R)
37	2^{6}(R)	2^{6}(R)
38	2^{7}(R)	2^{7}(R)
39	2^{8}(R)	2^{8}(R)
40	2^{9}(R)	2^{9}(R)
41	2^{10}(R)	2^{10}(R)
42	2^{11}(R)	2^{11}(R)
43	2^{12}(R)	2^{12}(R)
44	Not used	Not used
45	Cable shield	Cable shield

TABLE 2-2. CABLE CONNECTOR PIN ASSIGNMENTS (J1-J16, J21-J36) (CONT)

PIN NO.	INPUT CONNECTOR PIN DESIGNATION	OUTPUT CONNECTOR PIN DESIGNATION
46	Not used	Not used
47	2^{13}	2^{13}
48	2^{14}	2^{14}
49	2^{15}	2^{15}
50	2^{16}	2^{16}
51	2^{17}	2^{17}
52	2^{18}*	2^{18}*
53	2^{19}*	2^{19}*
54	2^{20}*	2^{20}*
55	2^{21}*	2^{21}*
56	2^{22}*	2^{22}*
57	2^{23}*	2^{23}*
58	2^{13}(R)	2^{13}(R)
59	2^{14}(R)	2^{14}(R)
60	2^{15}(R)	2^{15}(R)
61	2^{16}(R)	2^{16}(R)
62	2^{17}(R)	2^{17}(R)
63	2^{18}(R)*	2^{18}(R)*
64	2^{19}(R)*	2^{19}(R)*
65	2^{20}(R)*	2^{20}(R)*
66	2^{21}(R)*	2^{21}(R)*
67	2^{22}(R)*	2^{22}(R)*
68	2^{23}(R)*	2^{23}(R)*
69	Cable shield	Cable shield
70	2^{24}*	2^{24}*
71	2^{25}*	2^{25}*
72	2^{26}*	2^{26}*
73	2^{27}*	2^{27}*
74	2^{28}*	2^{28}*
75	2^{29}*	2^{29}*
76	2^{30}*	2^{30}*
77	2^{31}*	2^{31}*
78	Not used	Not used

TABLE 2-2. CABLE CONNECTOR PIN ASSIGNMENTS (J1-J16, J21-J36) (CONT)

PIN NO.	INPUT CONNECTOR PIN DESIGNATION	OUTPUT CONNECTOR PIN DESIGNATION
79	Not used	Not used
80	2^{24}(R)*	2^{24}(R)*
81	2^{25}(R)*	2^{25}(R)*
82	2^{26}(R)*	2^{26}(R)*
83	2^{27}(R)*	2^{27}(R)*
84	2^{28}(R)*	2^{28}(R)*
85	2^{29}(R)	2^{29}(R)*
86	2^{30}(R)*	2^{30}(R)*
87	2^{31}(R)*	2^{31}(R)*
88	Not used	Not used
89	Not used	Not used
90	Not used	Not used

* When the computer is operating dual channel (for 36-bit word equipment), these pin designations apply. When the computer is operating single channel (for 18-bit word equipment), pin designations do not apply. Pins labeled with an asterisk are considered spares, but cannot be used as such.

The (R) implies either the ground return or signal return line of the twisted pair.

TABLE 2-3. PIN ASSIGNMENTS FOR REMOTE CONSOLE CABLE CONNECTOR (J17) AND EXTERNAL SYNC CONNECTOR (J18)

PIN NO.	CONNECTOR PIN DESIGNATION
01	Ground
02	Ground
03	-15V
04	-15V
05	Unassigned
06	Unassigned
07	Unassigned
08	Unassigned
09	Unassigned
10	Unassigned
11	Battle Short indicator

TABLE 2-3. PIN ASSIGNMENTS FOR REMOTE CONSOLE CABLE CONNECTOR (J17) AND EXTERNAL SYNC CONNECTOR (J18) (CONT)

PIN NO.	CONNECTOR PIN DESIGNATION
12	Marginal Check indicator
13	Horn Alarm
14	Stop 5 indicator
15	Unassigned
16	Unassigned
17	Unassigned
18	Unassigned
19	Unassigned
20	Unassigned
21	Unassigned
22	Stop 1 indicator
23	Run indicator
24	Remote indicator
25	Stop 4 indicator
26	Stop 3 indicator
27	Stop 2 indicator
28	Program Fault indicator
29	Stop 0 indicator
30	Unassigned
31	Unassigned
32	Unassigned
33	Unassigned
34	Unassigned
35	Unassigned
36	Unassigned
37	Unassigned
38	Unassigned
39	Unassinged
40	Unassigned
41	Unassigned
42	Unassigned
43	Unassigned
44	Unassigned
45	Ground
46	Unassigned

TABLE 2-3. PIN ASSIGNMENTS FOR REMOTE CONSOLE CABLE CONNECTOR (J17) AND EXTERNAL SYNC CONNECTOR (J18) (CONT)

PIN NO.	CONNECTOR PIN DESIGNATION
47	Stop 4 switch
48	Stop 3 switch
49	Stop 2 switch
50	Stop 1 switch
51	Stop 0 switch
52	Skip 4 switch
53	Skip 3 switch
54	Skip 2 switch
55	Skip 1 switch
56	Skip 0 switch
57	Master clear switch
58	Stop 4 switch (R)
59	Stop 3 switch (R)
60	Stop 2 switch (R)
61	Stop 1 switch (R)
62	Stop 0 switch (R)
63	Skip 4 switch (R)
64	Skip 3 switch (R)
65	Skip 3 switch (R)
66	Skip 1 switch (R)
67	Skip 0 switch (R)
68	Master clear switch (R)
69	Ground
70	Remote ON/OFF switch (ON)
71	Auto recovery switch
72	Load (Mode) switch
73	Stop switch
74	Start switch (NC)
75	Start switch (NO)
76	Unassigned
77	Abnormal condition indicator
78	Unassigned
79	Unassigned
80	Remote ON/OFF switch (ON) (R)
81	Auto recovery switch (R)

TABLE 2-3. PIN ASSINGMENTS FOR REMOTE CONSOLE CABLE CONNECTOR (J17) AND EXTERNAL SYNC CONNECTOR (J18) (CONT)

PIN NO.	CONNECTOR PIN DESIGNATION
82	Load (Mode) switch (R)
83	Stop switch (R)
84	Start switch (NC) (R)
85	Start switch (NO) (R)
86	Unassigned
87	Unassigned
88	Unassigned
89	Unassigned
90	Unassigned
PIN NO.	EXTERNAL SYNC CONNECTOR (J18)
A	External Sync (R)
B	Ground
C	External Sync Signal

2-5. COMPUTER GROUND REQUIREMENTS.

Grounding the computer is important for two reasons: 1) to ensure the safety of operating and maintenance personnel; 2) to maintain dc level system used for I/O communications.

The computer is grounded in two places; at pin D (A14E1) of the power entry jack, and at ground lug A12E1 located at the rear of the cabinet. The ac neutral wire connects to A14E1; system ground cables connect to ground lug A12E1 along with all internal circuit grounds.

Use a separate cable for grounding each peripheral device to the computer. These cables should not be junctioned at any point other than at the ground lug A12E1 on the rear of the computer. (See figure 2-4 for quasi-ground plane system.)

2-6. PREOPERATIONAL INSPECTION AND PRELIMINARY TESTING.

a. VISUAL INSPECTION. - The following procedure should be performed after installing the computer and connecting power and I/O signal cables, but before turning on power. The purpose of this inspection is to detect components and parts that may have been damaged when the computer was loaded, unloaded, or in transit. The types of damage to check for are loose circuit cards, loose card retainers, damaged fuses or indicators, and other forms of shipping damage not apparent or detected at the time of unpacking the equipment. For visual inspection, perform the following steps:

STEP 1. Open front cover on drawer A3 (figure 1-18) and remove combination tool from inside of the door.

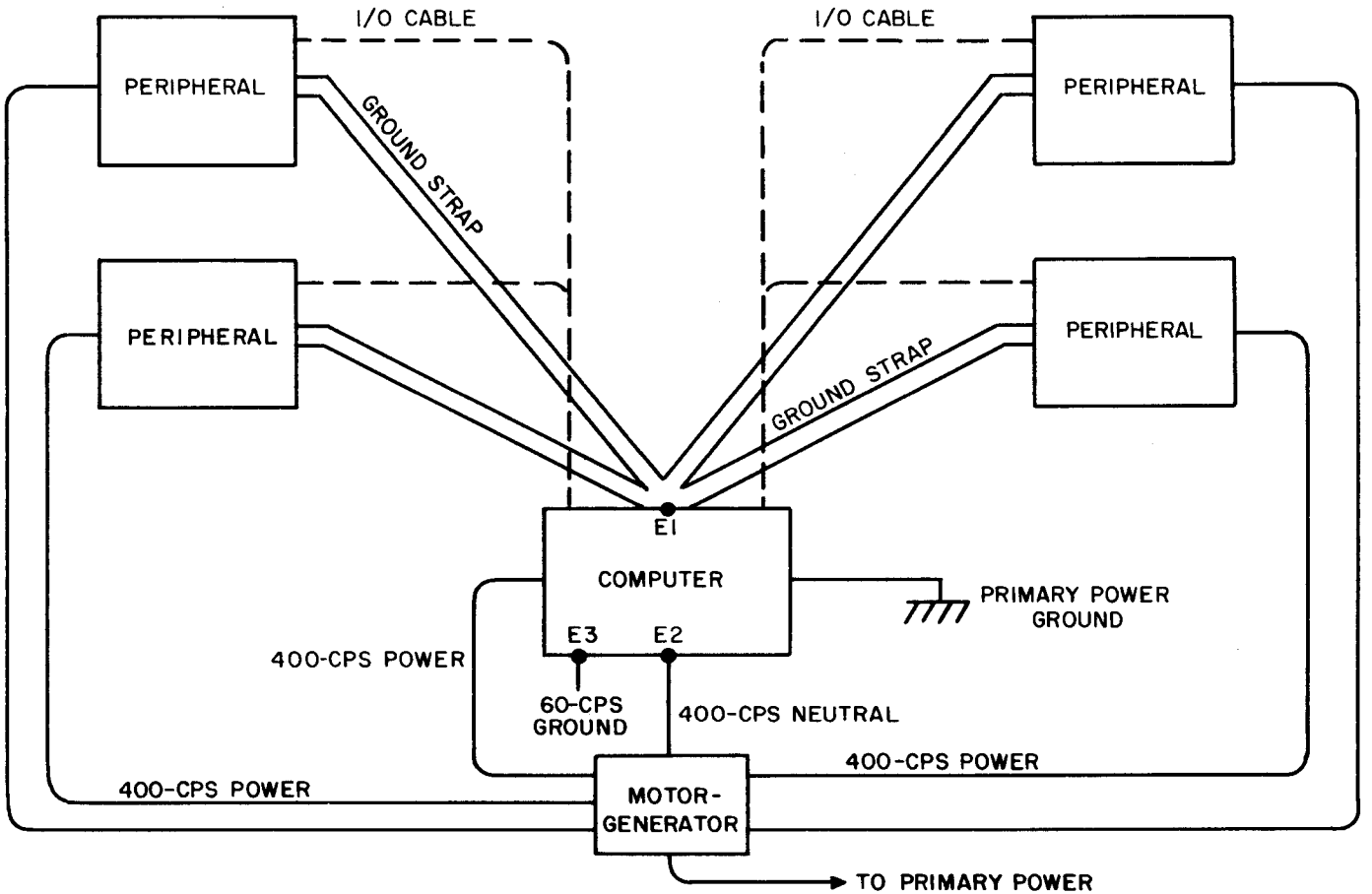


Figure 2-4. Quasi-Ground Plane System

STEP 2. Inspect components for loose connection or damage; replace as necessary.

STEP 3. Unscrew four locking bolts and extend drawer, ensuring that drawer locks securely in fully extended position.

STEP 4. Check drawer for loose retainers and circuit cards, reseating any cards that are loose and replacing damaged ones.

NOTE

Omit step 5 on drawer A3 if computer has a maximum memory capacity of 32K.

STEP 5. Unscrew bolt at back of hinged chassis and swing chassis open. Check for loose or broken wire wrap connections. Repair as necessary.

STEP 6. Ensure that no loose hardware (nuts, bolts, washers) is lying inside drawer. Also ensure that all terminal board mounting hardware and insulating materials are securely in place.

STEP 7. Check fuses mounted on inside of cabinet behind drawers; replace as necessary.

STEP 8. Close and bolt the hinged chassis; then close and lock pull-out drawer.

STEP 9. Repeat steps 1 through 8 for each of remaining drawers except that in step 3, use combination tool and loosen three retaining screws on front panel and open panel to expose test blocks and drawer-retaining bolt. Use combination tool and unscrew drawer-retaining bolt until plugs on rear of drawer are disengaged from cabinet receptacles. Slide drawer forward to fully extended position and ensure that drawer lock is engaged.

STEP 10. Check power supply drawer to ensure no fuses are cracked or broken. Ensure that all fuses are securely in place.

STEP 11. With a volt-ohmmeter, check power supply to ensure no short circuits exist between voltage lines, or between ground and any voltage lines.

b. INITIAL POWER CHECK. - For an initial power check, place switches in positions listed in table 2-4 and perform the following steps:

STEP 1. Turn on power at junction box or main control panel to apply ac power to computer as far as power supply, PS1.

STEP 2. Pull open power supply drawer.

STEP 3. At ac terminal board TB2 (figure 1-17), measure between terminals 1, 2, and 3 for proper voltage. There should be 115 volts (±1%) (steady state tolerance band) measured between terminals.

Transient voltages should not be less than 106.95 volts nor more than 123.05 volts, recoverable to the final value within the steady state tolerance band in 0.1 second maximum.

STEP 4. If all voltages check properly, close drawer. If not, recheck source; then, turn power OFF and check cable connections. When corrected, proceed to step 5.

TABLE 2-4. INITIAL SWITCH POSITIONS

SWITCH	POSITION
Power	Off
Disc alarm/reset alarm	Neutral
Battle Short	Off
Indicate-off-indicate/set	Indicate/set
Channel Inter. computer/channel normal	Channel Normal
Channel function (4)	Single
I/O clear-Master clear	Neutral
Seq step/stop	Neutral
Restart speed control	Approximate Center
Restart/start step	Neutral
Function repeat	Down
Phase repeat	Down
Auto recovery	Down
Disc Adv P	Down
Program stops	Down
Program skips	Down
Ext. sync. disc	Down
RTC disc	Down
Clock Narrow/normal (ODD)*	Normal
Clock Narrow/normal (EVEN)*	Normal
Bootstrap Mode	NDRO

* Located behind front panel on drawer A2.

STEP 5. On computer's power control panel, set POWER switch (S4) to ON position. Ensure POWER ON indicator lights and blowers operate.

STEP 5A. Remove four grill-retaining screws, swing grill upward and remove air filter.

STEP 5B. Set POWER switch (S4) to OFF position.

STEP 5C. Observe blower rotor and ensure that the rotor of each blower (B1 behind A5, and B2 behind A10) rotates so that the bottom of the rotor moves toward the front of the cabinet (counterclockwise) as shown in figure 2-4A. If either rotor is not running in a counterclockwise direction, check the associated wiring for correct connections.

NOTE

Switching the connections of any two blower wires will reverse direction of blower rotation.

STEP 5D. Replace air filter, ensuring that spring clips are against the grill and not the cabinet. Lower grill and replace four grill-retaining screws.

STEP 5E. Set POWER switch (S4) to ON position and proceed to step 6.

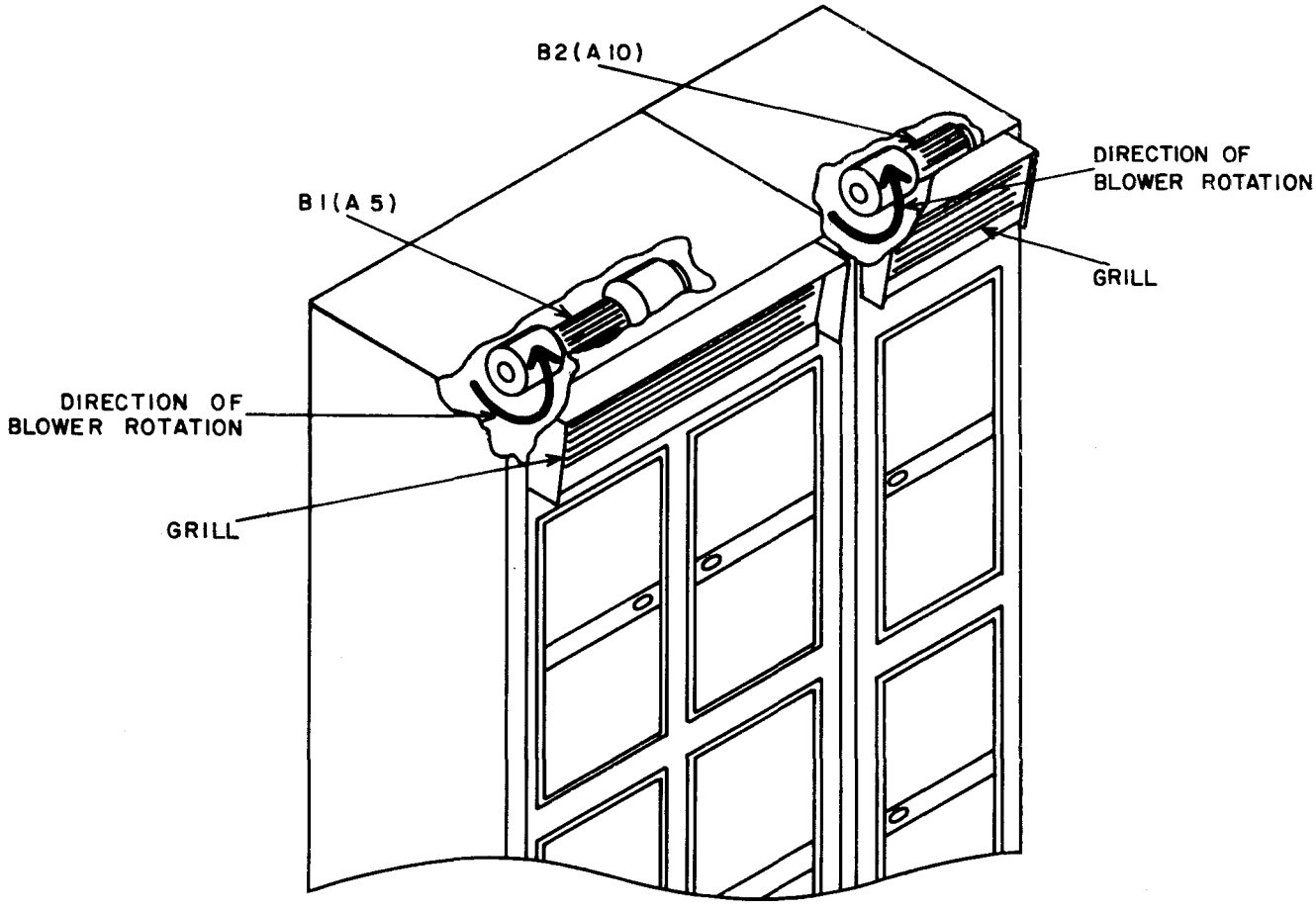


Figure 2-4A. Blower Rotation Check

STEP 6. Press MASTER CLEAR switch to clear computer logic circuitry.

STEP 7. Press PHASE STEP MODE switch to place computer in phase step mode of operation.

STEP 8. Use oscilloscope, preamplifier, and dc voltmeter and check power supply, PS1, voltages on each chassis at test points listed in table 2-5. Use a direct probe with oscilloscope and preamplifier to measure ripple voltages.

STEP 9. Use same equipment as in step 8 and meausre main memory power supply voltages on each chassis A3A1 and A3A2 at test points listed in table 2-6.

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NOTE

Chassis A3A1 is installed in Drawer 3 only if memory capacity is greater than 32K.

Figure 2-5 shows the printed circuit module at location 7C on which main memory voltage test points are located.

TABLE 2-5. DC POWER SUPPLY TEST DATA

VOLTAGE	TEST BLOCK (A1, A2 & A4)	TOLERANCE	DC RIPPLE ** (Peak to Peak)
+15V	TB1, TP D33	+13.5 to +16.5	0.20V
-15V	TB1, TP E33	-13.5 to -16.5	0.20V
-4.5V	TB1, TP F33	-4.05 to -4.95	0.20V
Ground	TB1, TP G33		
VOLTAGE	TEST BLOCK (DRAWER A4)	TOLERANCE	DC RIPPLE ** (Peak to Peak)
* -7V regulated	TB2, TP A33		
* -15V regulated	TB2, TP B33		
* +15V regulated	TB2, TP C33		
+15V	TB2, TP D33	+13.5 to +16.5	0.20V
-15V	TB2, TP E33	-13.5 to -16.5	0.20V
-4.5V	TB2, TP F33	-4.05 to -4.95	0.20V
Ground	TB2, TP G33		

* These factory-set voltages vary between machines and should not be changed unless a problem arises in the area.

** When the computer is Master Cleared and Phase Step mode is selected.

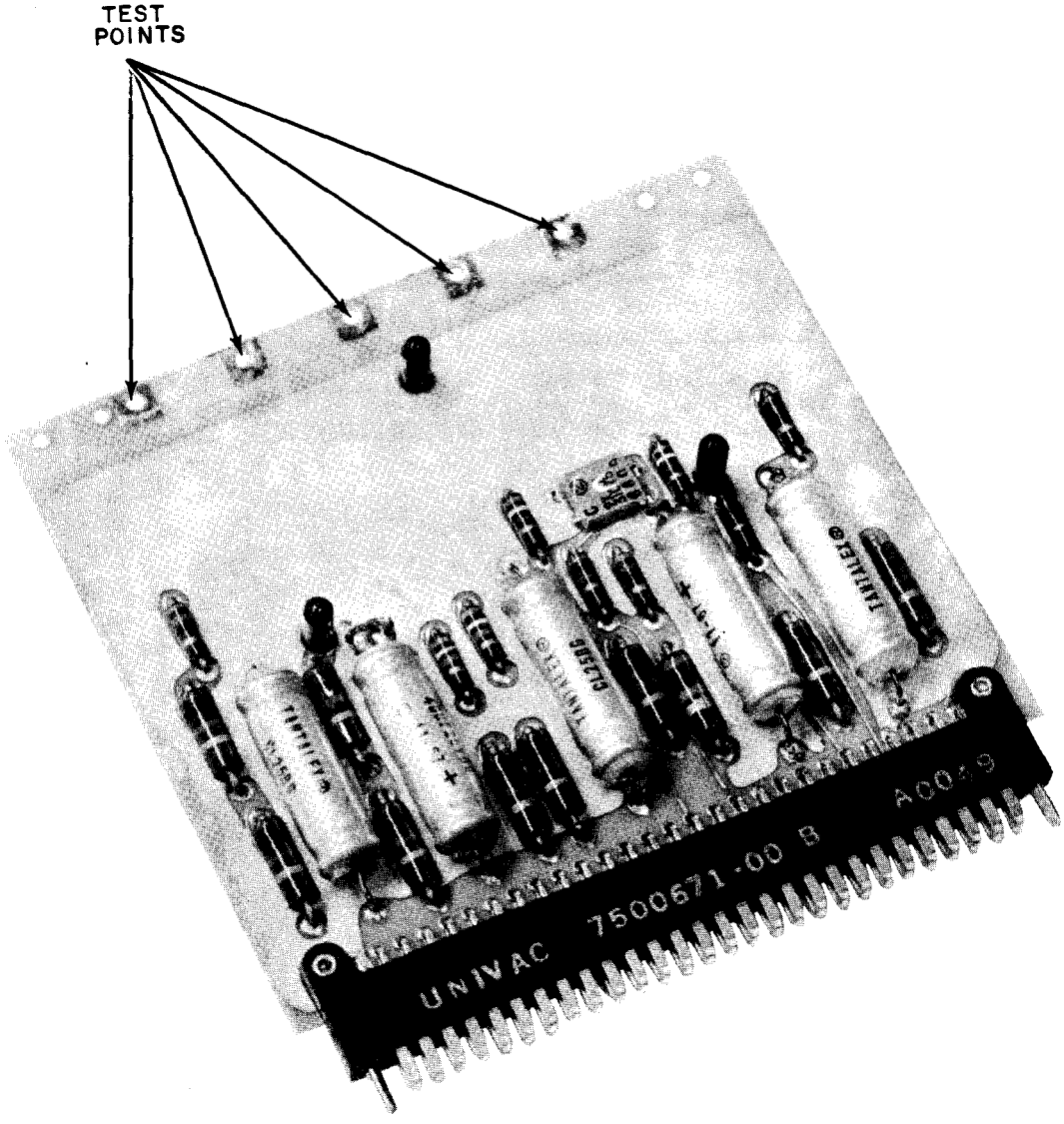


Figure 2-5. Test Point Card

TABLE 2-6. MAIN MEMORY POWER SUPPLY TEST POINTS

VOLTAGE	CHASSIS A3A1 & A3A2	TOLERANCE	DC RIPPLE ** (Peak to Peak)
+6V	gJ7C, TP 1	+5.7 to +6.3	0.10V
+15V	gJ7C, TP 3	+13.5 to +16.5	0.20V
-15V	gJ7C, TP 5	-13.5 to -16.5	0.20V
-3V	gJ7C, TP 7	-2.9 to -3.1	0.10V
+3V	gJ7C, TP 9	+2.9 to +3.1	0.10V
Ground	A3A2W2*		

* Use A3A2W2 for ground in each case.

** When the computer is Master Cleared and Phase Step mode is selected.

c. INITIAL OPERATIONAL CHECK. - The maintenance routines provide the most comprehensive method of testing the operational capabilities of the computer because they most closely simulate the actual operation of the computer. For a complete description of these routines, refer to Section 5 of this manual.

2-7. PACKAGING FOR RESHIPMENT. - To prepare for reshipment, perform the following steps:

CAUTION

Before proceeding with step 1, check to ensure power is OFF at the computer and the control panel or junction box.

STEP 1. Disconnect power cable from power source, external sync cable from external synchronizing device, and I/O signal cables from peripheral devices.

STEP 2. Remove cover from top of cabinet to provide access to cable entry panel.

STEP 3. Disconnect power cable, external sync cable and I/O signal cables at computer.

STEP 4. Replace and secure cover to top of cabinet.

STEP 5. If cables are to be shipped, form each cable in a coil (minimum diameter of 25 inches), use tape to hold the coil, and pack in a suitable container. Mark outside of the carton(s) CABLES INSIDE.

STEP 6. Lock all pull-out drawers and cabinet doors.

STEP 7. Cover corners and edges of cabinet with foam rubber pads or strips (or other suitable material) and tape in place.

STEP 8. Cover cabinet with a vinyl bag or a similar dust and moisture proof covering. Seal bag or covering at base of cabinet.

STEP 9. Place computer on a shipping skid and bolt cabinet securely in place on skid.

STEP 10. If computer is being prepared for overseas shipment, place computer in a plywood crate, filling airspace between crate and cabinet with shredded paper, foam rubber pads, or other suitable shock absorbing packing material.

STEP 11. Pack all applicable technical manuals in a box and mark box TECHNICAL MANUALS INSIDE.

SECTION 3

OPERATOR'S SECTION

3-1. GENERAL.

A computer is basically an automatic machine; however, there are certain controls that affect computer operation. The controls provide a means of setting and clearing the registers, selecting computer operating speeds, selecting optional program jumps or stops, and selecting input/output modes. On the computer, these controls are on the front panels of each drawer. The panels are designated: input/output panel (A1 or optional A8), control panel 1 (A2), memory panel (A3), control panel 2 (A4), and power control panel (A5). These panels are shown in figures 3-1 thru 3-5.

Indicator/switches on the operator panels are associated with the computer register and control flip-flops. These indicator/switches serve a dual function: the indicator lights when the associated flip-flop is in the set or one condition; pressing the indicator/switch places the associated flip-flop in the set or one condition. The indicators provide a visual indication of status and operation; they are intended primarily for maintenance personnel.

3-2. DESCRIPTION OF CONTROLS.

Tables 3-1 through 3-4 list the switches and indicator/switches of the computer with a functional description of each.

TABLE 3-1. INPUT/OUTPUT PANEL (A1 OR OPTIONAL A8)

TITLE	FUNCTION/USE
C_O 0-17	Displays contents and allows manual control of 18 bits of communications register common to all odd-numbered output channels. It contains upper 18 bits of word in dual channel mode.
C_E 0-17	Displays contents and allows manual control of 18 bits of communications register common to all even-numbered output channels. It contains lower 18 bits of word in dual channel mode.
I/O Channel and Status Grid	Indicator/switches indicate function and channel of that coordinate.
CHAN PRI	Indicated channel is requesting priority.
EI MON	An external interrupt monitor has been detected and is being processed.
EF MON	An external function has been detected and is being processed.
OD MON	An output data monitor has been detected and is being processed.
ID MON	An input data monitor has been detected and is being processed.

TABLE 3-1. INPUT/OUTPUT PANEL (A1 OR OPTIONAL A8) (CONT)

TITLE	FUNCTION/USE
EF ACT	External function mode has been made active (able to communicate).
OD ACT	Output data mode has been made active and is able to communicate.
ID ACT	Input data mode has been made active.
EF/OD ACK	An external function or output data acknowledge signal has been placed on an output control line.
ID ACK	An input data achnowledge signal has been placed on an output control line.
EF MODE	External function mode; when on, it indicates the EF mode for any EF/OD function; when off, it indicates the OD mode.
	NOTE Pressing above indicator/switches except CHAN PRI will set associated flip-flops.
FUNCTION PRIORITY Grid	Indicator/switches indicate function and channel group of that coordinate.
ODD	Odd-numbered I/O channels.
EVEN	Even-numbered I/O channels.
EXT INT	An external interrupt request for priority has been made or is being processed.
EF/OD	An external function or output data request has been made or is being processed.
ID	An input data request for priority has been made or is being processed. A request for priority cannot appear simultaneously on odd and even channel group.
	NOTE Pressing FUNCTION PRIORITY indicator/switches will set associated flip-flops.
CHANNEL INTER-COMPUTER/ CHANNEL NORMAL 0-7	Up position: Enables corresponding numbered input and output channels to be used as an intercomputer channel. Down position: Allows normal use of that numbered channel for other peripheral equipment.

TABLE 3-1. INPUT/OUTPUT PANEL (A1 OR OPTIONAL A8) (CONT)

TITLE		FUNCTION/USE
CHANNEL FUNCTION Switches 0-1 2-3 4-5 6-7	ESA	Allows the two channels selected to operate in the externally specified address mode (dual mode forced).
	DUAL	Connects adjacent input/output channels so they operate in double length (36-bit) mode; for example, switch 0-1 in DUAL position allows channels 0 and 1 to operate in dual mode.
	SINGLE	Allows I/O channels to operate in single (18-bit) mode.
	ESI	Allows two channels selected to operate in externally specified index mode (dual mode forced).

TABLE 3-2. CONTROL PANEL 1 (A2)

TITLE		FUNCTION/USE
A_U	0-17 and Clear	Displays contents and allows manual control of A_U register (upper 18 bits of A register). Each bit may be set by pressing appropriate indicator/switch. Clear button clears all 18-bit positions.
A_L	0-17 and Clear	Displays contents and allows manual control of A_L register (lower 18 bits of A register). Each bit may be set by pressing appropriate indicator/switch. Clear button clears all 18-bit positions.
ICR (Index Control Register)	0-2 and Clear	Indicates which of index registers is to be used as a modifier. Clear button clears entire register.
SR (Special Register)	Bits 0-3 and Clear	A four-bit register used to specify memory bank currently being used. Clear button clears the register.
	ACT	Comes on when SR is active. When cleared, SR is inactive.

TABLE 3-2. CONTROL PANEL 1 (A2) (CONT)

TITLE		FUNCTION/USE
SEQ DES (Sequence Designators)	I/O 1 (I/O I on front panel)	Indicates performance of first I/O sequence.
	I/O 2 (I/O II on front panel)	Indicates performance of second I/O sequence.
	I	Indicates performance of instruction sequence which is common to all instructions. Manually selecting I sequence clears all other sequences.
	INT	Indicates performance of interrupt sequence.
	R 1 (R I on front panel)	Indicates performance of first R (read) sequence.
	R2 (R II on front panel)	Indicates performance of second R (read) sequence.
	W	Indicates performance of W (write) sequence.
	WAIT	Indicates performance of WAIT sequence. (For example, computer waits for an interrupt.)
	B 1 (B I on front panel)	Indicates performance of first B sequence, which reads TACW and stores it in control memory.
	B 2 (B II on front panel)	Indicates performance of second B sequence, which reads IACW and stores it in control memory.
		NOTE All of sequence designator indicators can be manually set.
TIMING 11-14 21-24 31-34 41-44 and 52		Indicates setting of main timing cycle flip-flops, T11 through T52. Thus, as indicators come on and go off, progression of cycle time of computer is indicated. Indicator 52 comes on only during 50:61 and 50:63 instructions.
ABNORMAL CONDITION	TEMP	This indicator comes on when either low temperature thermostat detects an internal air temperature higher than 115°F (46°C).
	VOLTAGE FAULT	This indicator comes on when any of logic voltages (±5V, -3V) or memory voltage (±10V) fluctuates outside of preset limits.

TABLE 3-2. CONTROL PANEL 1 (A2) (CONT)

TITLE		FUNCTION/USE
F II (Format 2) 6		Bit 2^6 indicator of function code register indicates function code is of Format II type (for example, 50:XX). May be manually set or cleared.
FUNCTION CODE 0-5 and Clear		Bit 2^0-2^5 indicators of function code register octally display the function code in F register. All six bits may be manually set or cleared.
P 0-15 and Clear		Displays contents and allows manual control of 16 bits of program address register. Each bit may be set by pressing appropriate indicator/switch. Clear button clears all 16-bit positions.
MODE	LOAD	Indicates load mode. Pressing MODE LOAD button sets load mode, clears all other modes, and forces a jump to address 00500 for loading at high speed.
	PHASE STEP	Indicates phase step mode. Pressing MODE PHASE STEP button sets phase step mode, clears all other modes, and enables PHASE indicator/ switches and computer for clock phase operation. Inhibits memory.
	OP STEP	Indicates operation step mode. Pressing MODE OP STEP button sets operation step mode, clears all other modes, and enables computer for execution of one operation at a time. This will be one instruction or one sequence depending on position of SEQ STEP/STOP switch.
	RUN	Indicates run mode. Pressing MODE RUN button sets run mode, clears all other modes, and enables computer for normal high speed operation
PHASE	1-4 and Clear	Indicates phase selected. Selecting one phase by pressing indicator/switch enables computer to issue phase pulses in conjunction with phase step mode. Phase pulses are issued individually beginning with selected phase. Pressing Clear button clears all four phases.
I/O CLEAR/MASTER CLEAR Switch		Center position: Neutral. Momentary up position (I/O CLEAR): Clears I/O section of computer only and sets all stages of channel priority. Momentary down position (MASTER CLEAR): With computer not running, and not in phase step mode, clears all sections, registers and control flip-flops of central computer. With computer running, it clears VOLTAGE FAULT and/ or PROGRAM FAULT indicators only.

TABLE 3-2. CONTROL PANEL 1 (A2) (CONT)

TITLE	FUNCTION/USE
SEQ STEP/STOP Switch	Center position: Neutral. Momentary up position (SEQ STEP): Enables execution of a single sequence in conjunction with operation step mode. Momentary down position (STOP): Stops high speed operation of the computer; RUN indicator goes off.
RESTART SPEED CONT	Varies speed of low-speed oscillator.
RESTART/START STEP Switch	Center position: Neutral. Momentary up position (RESTART): Enables selected mode to be executed at restart speed control rate setting. Momentary down positon (START/STEP): Load mode selected - initiates high-speed start at address 00500. Run mode selected - initiates high-speed start at address designated in P. Phase step mode selected - initiates issuance of phase or phases indicated by PHASE indicators. Op step mode selected - initiates execution of one instruction or one sequence, depending upon position of SEQ STEP/STOP switch.
FUNCTION REPEAT Switch	Up position: Forces a repeat of instruction in F register at mode rate, and disables clearing of S register in any sequence other than I, except in W sequence of instruction 50:10-50:13.
PHASE REPEAT Switch	Up position: Forces repeat at high speed of phase or phases selected by PHASE indicators. (Phase step mode must be selected.)
AUTO RECOVERY Switch	Up position: Computer fault results in a jump to address 00500. Down position: Computer fault results in a jump to address 00000.
DISC ADV P Switch	Up position: Inhibits incrementing P register.

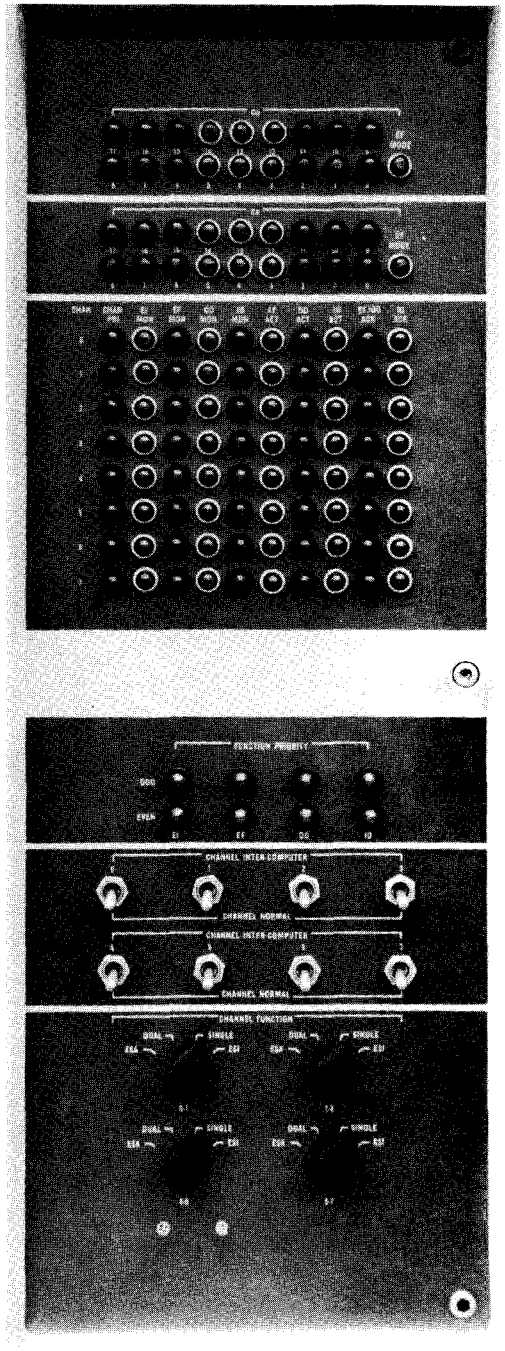


Figure 3-1. Input/Output Panel (A1 or optional A8)

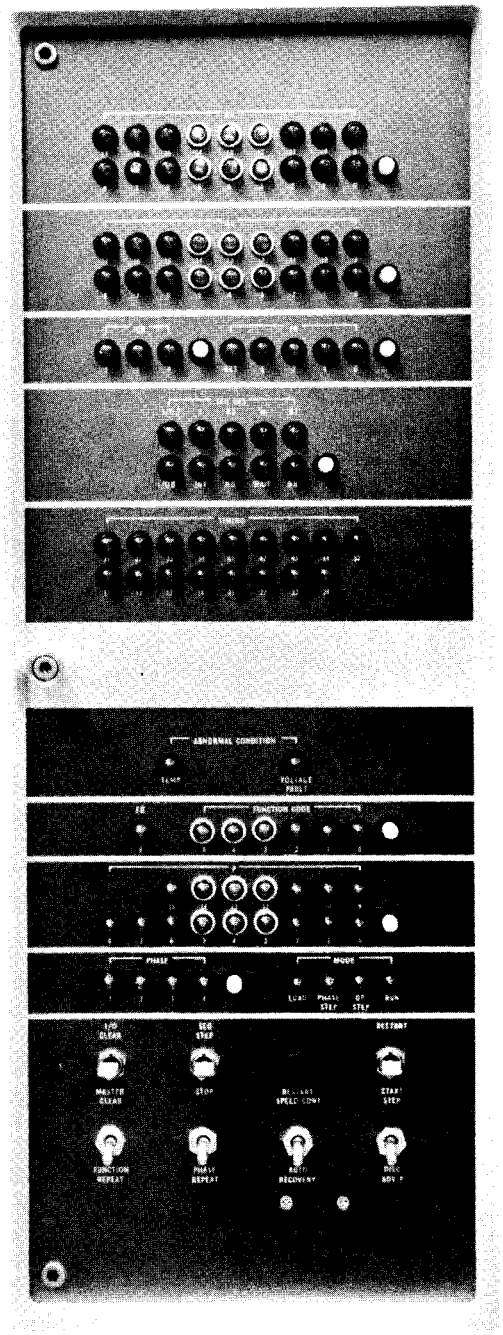


Figure 3-2. Control Panel 1 (A2)

TABLE 3-3. CONTROL PANEL 2 (A4)

TITLE		FUNCTION/USE
PROGRAM STOP Indicators 0-5		Comes on when a program stop occurs as a result of a 50:56 instruction. Indicator 5 lights for an unconditional stop; the rest are dependent upon stop switches.
PROGRAM STOP Switches 0-4		On position (up): Enables a program stop on switch setting for a 50:56 instruction if corresponding bit of instruction is a binary one.
PROGRAM SKIP Switches 0-4		On position (up): Enables a skip of next instruction on a 50:50 instruction if corresponding bit of instruction is a binary one.
S_1	0-15 and Clear	Displays contents and allows manual control of the 16 bits of memory address register. Each bit may be set by pressing appropriate indicator/switch. Clear button clears all bit positions simultaneously.
Z_1	0-17 and Clear	Displays contents and allows manual control of 18 bits of main memory exchange register. Each bit may be set by pressing appropriate indicator/switch. Pressing Clear button clears all 18-bit positions.
B	0-17 and Clear	Displays contents and allows manual control of 18 bits of buffer control register. Each bit may be set by pressing appropriate indicator/switch. Clear button clears all bit positions simultaneously.
K	0-5	Displays contents and allows manual control of six-bit register used for shift, multiply, divide, stop, and skip instructions. Must be cleared by MASTER CLEAR switch.
REG +10V/-10V		Manual adjustable potentiometers setting outputs of ±10V regulators.
ADV P SEQ 0-2		Indicates set condition of advance P sequence flip-flops and operation of sequence. Each flip-flop may be set by pressing appropriate indicator/switch.
INTERRUPT	INST FAULT	Indicates that an instruction fault (f=00, 01, 77) has been detected by fault circuitry, and a fault interrupt address is being generated to inform computer.
	RESUME FAULT	Indicates that resume signal was not received during a minimum period of 1 second and a maximum of 2 seconds after data was placed on an intercomputer channel.*

* Dependent upon RTC being operational (RTC DISC switch in down position).

TABLE 3-3. CONTROL PANEL 2 (A4) (CONT)

TITLE		FUNCTION/USE
	RTC MON	Indicates that memory address 15, RTC word, is equal to memory address 14, RTC monitor; and that an interrupt is being generated to inform computer.*
	RTC OVERFLOW	Indicates that 18 bits of RTC word have changed from all binary ones to all binary zeros; and that an interrupt is being generated to inform computer.*
	SYNC	Indicates that a synchronizing interrupt has been received from a peripheral device and is being processed.
EXT SYNC DISC Switch		Up position: External synchronizing input is disconnected. Down position: External synchronizing input may be received.
RTC	SEQ Indicator	Indicates that operation of updating real-time clock word is in process.
	DISC Switch	Up position: RTC interrupting signal is disconnected (disabled). Down position: RTC interrupting signal is operational (enabled).
I/O TRANSLATOR	ACTIVE	Indicates performance of any I/O operation or instruction (50:01 - 50:27).
	ESA	Indicates that current I/O operation is in externally specified address mode.
	DUAL	Indicates that current I/O operation is in dual (dual channel, 36-bit words) mode.
	ESI	Indicates that current I/O operation is in ESI (externally specified index) mode.
FUNCTION	0 and 1	These indicator/switches display binary value which represents I/O functions. Values are assigned as follows: 00 - Ext Interrupt 01 - Unassigned 10 - Output 11 - Input
CHANNEL	0-3 and Clear	These indicator switches display octal value of active I/O channel. Each bit may be set by pressing appropriate indicator/switch. Clear button clears all bits of CHANNEL and FUNCTION.

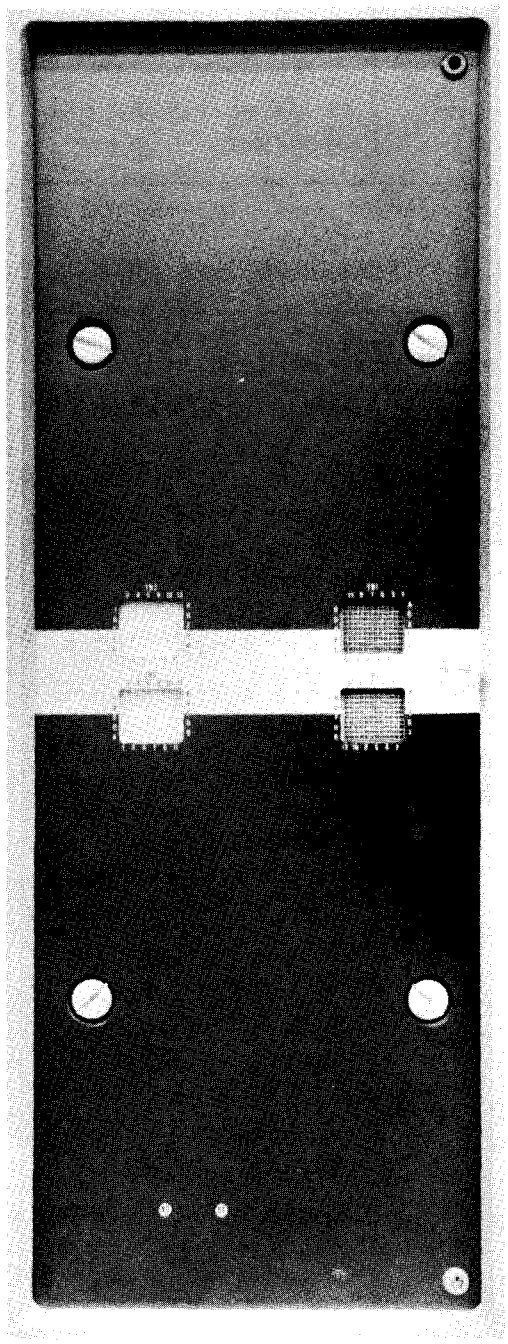
* Dependent upon RTC being operational (RTC DISC switch in down position).

TABLE 3-3. CONTROL PANEL 2 (A4) (CONT)

TITLE		FUNCTION/USE
MULT/DIV SEQ	0-6	Indicates set condition of multiply, divide, shift and scale sequence flip-flops and operation of sequence. Each flip-flop may be set by pressing appropriate indicator/ switch.
BOOTSTRAP MODE	NDRO	References NDRO bootstrap program at addresses 00500 through 00537.
	MAIN MEMORY	References main memory addresses 00500 through 00537 which may contain an alternate bootstrap program.

TABLE 3-4. POWER CONTROL PANEL (A5)

TITLE	FUNCTION/USE
RUNNING TIME METER	Cumulatively records time that power is supplied to computer. Range of meter is 0 to 9999.9 hours and cannot be reset.
POWER ON/OFF Switch	Under normal conditions*, when momentarily in ON position, power is applied to computer; in momentarily OFF position, power is removed. *Proper interlock and operating temperatures.
POWER Indicator	Comes on when power is being applied to computer.
LOCAL CONTROL Indicator	Comes on when computer may be controlled from control panels of computer (not remote control panel).
PROGRAM RUN Indicator	Comes on when computer is in any mode of operation other than stop. (For example, run flip-flop is set.)
DISC ALARM/RESET ALARM Switch	Center position: Allows horn to sound on program, voltage, or temperature fault. Momentary down position (RESET ALARM): Horn is silenced. Up position (DISC ALARM): Horn is disabled for all faults.
PROGRAM FAULT Indicator	Comes on when computer detects an illegal function code of 00, 01, 77 (Format I) in F register. Goes off by setting I/O CLEAR/ MASTER CLEAR switch to MASTER CLEAR position, regardless if computer is running or not.



NOTE: TEST BLOCKS INSTALLED ONLY ON SN 14-48.

Figure 3-3. Memory Panel (A3)

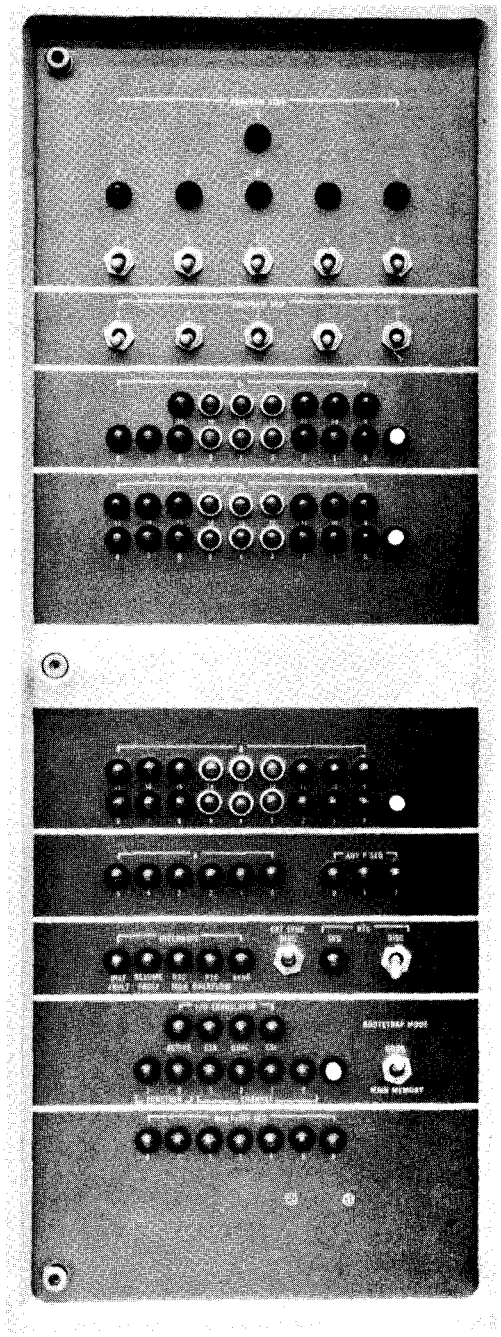


Figure 3-4. Control Panel 2 (A4)

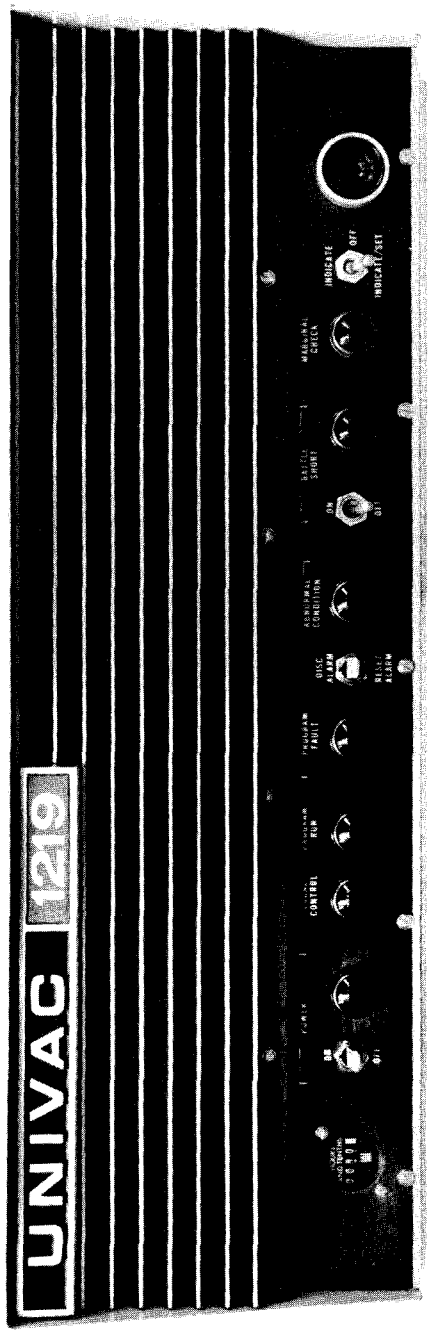


Figure 3-5. Power Control Panel (A5)

TABLE 3-4. POWER CONTROL PANEL (A5) (CONT)

TITLE	FUNCTION/USE
ABNORMAL CONDITION Indicator	Comes on when one of two abnormal condition indicators, TEMP or VOLTAGE FAULT on panel A2 is on.
BATTLE SHORT Switch	ON position: Disables memory protective circuitry, temperature and blower sensor circuitry thus removing all automatic computer shutdown.
BATTLE SHORT Indicator	Comes on when BATTLE SHORT switch is in ON position.
MARGINAL CHECK Indicator	Comes on when either CLOCK NARROW/NORMAL switch is in NARROW position.
INDICATE-OFF-INDICATE/SET Switch	Center position (OFF): Disconnects voltage to all incandescent lamps on all panels. Up position (INDICATE): Supplies voltage to all incandescent lamps on all panels. Down position (INDICATE/SET): Supplies voltage to all incandescent lamps and push-button switches on all panels.
Fault Horn	Horn sounds on program, voltage, or temperature fault.

3-3. EXPLANATION OF TERMS.

The following terms are used in the operating procedures (paragraphs 3-4 thru 3-5). When instructed to "press SWITCH A to XX", the momentary toggle switch marked "SWITCH A" is to be pressed to the position marked "XX" and released. When instructed to "press SWITCH A", the momentary pushbutton switch marked "SWITCH A" is to be pressed and released. A momentary switch is not to be held in one position unless specified. When instructed to "place switch A in XX", the switch marked "A" is to be set to the position marked "XX" and left in that position.

3-4. MANUAL READING AND WRITING.

The following procedures for manually reading and writing can be used to test and debug a program. Principally, the manual operations involve the correction and checking of the stored program being run. Although all of the procedures can be used, it is not intended that they should be rigidly followed for all cases of program correction and checking.

a. MANUAL READING FROM ADDRESSES. - Manual reading into the AL register involves the use of the ENTER AL instruction (f = 12). With this instruction, the contents of any memory address can be observed by using the following procedure:

STEP 1. Press SEQ STEP/STOP switch to STOP.

STEP 2. Press I/O CLEAR/MASTER CLEAR switch to MASTER CLEAR.

STEP 3. Set the P register equal to one less than the address of the word to be entered into the AL register.

STEP 4. Set the FUNCTION CODE register equal to 12_8.

STEP 5. Place FUNCTION REPEAT switch in the up position.

STEP 6. Press MODE OP STEP switch.

STEP 7. Press RESTART/START STEP switch to START STEP. (Repeat step 7 for first-time operation.)

With step 7 completed, the computer stops and the desired word is available for inspection in the AL register. To repeat the procedure, perform step 7 only.

b. MANUAL LOADING (WRITING) INTO ADDRESSES. - The procedure for manually entering a word into storage can be varied. One way is with a STORE AL (f = 44) instruction using the following procedure:

STEP 1. Press SEQ STEP/STOP switch to STOP.

STEP 2. Press I/O CLEAR/MASTER CLEAR switch to MASTER CLEAR.

STEP 3. Set the P register equal to one less than the address of the desired storage address.

STEP 4. Set the FUNCTION CODE register equal to 44_8.

STEP 5. Place FUNCTION REPEAT switch in the up position.

STEP 6. Set the word to be stored in the AL register.

STEP 7. Press MODE OP STEP switch.

STEP 8. Press RESTART/START STEP switch to START STEP. (Repeat step 8 for first-time operation.)

With step 8 completed, the computer stops and the word in the AL register is transferred to the desired memory location. To repeat the procedure, perform step 8 only.

c. MANUAL INSPECT AND CHANGE ROUTINE. - Often it is necessary to check the contents of consecutive addresses in storage. This can be done by manually loading a short program as follows:

ADDRESS	PROGRAMMED INSTRUCTION	EXPLANATION
010	507201	Select address 01 for index register (B1) modification.
011	440001	(AL) → B1
012	110000	B1 → AU
013	505640	STOP
014	470000	(AU) → (B1)
015	710001	Increment AL
016	340011	Jump

Load each instruction of the program, using the procedure outlined in paragraph 3-3b. When the program has been loaded, consecutive memory addresses are read by use of the following procedures:

STEP 1. Press SEQ STEP/STOP switch to STOP.

STEP 2. Press I/O CLEAR/MASTER CLEAR switch to MASTER CLEAR.

STEP 3. Set the P register equal to 00010_8.

STEP 4. Set the desired starting address in the AL register.

STEP 5. Press MODE RUN switch.

STEP 6. Press RESTART/START STEP switch to START STEP.

With step 6 completed, the computer stops and AU displays the contents of the address specified in AL. Each time the RESTART switch is pressed, AL is incremented and the computer stops with the contents of the next consecutive address displayed in AU. If, at any time, the operator decides to change the contents of an address as displayed in AU, he can make the change manually (set AU to the new value) and press the RESTART switch. This automatically changes the contents of that address (as specified in AL) and then displays the contents of the next consecutive address.

3-5. WIRE MEMORY (BOOTSTRAP).

a. GENERAL. - The computer has 32_{10} bootstrap memory address locations (00500_8 through 00537_8), which contain the wired memory bootstrap program for an initial load or bootstrap program. The computer can have a bootstrap written for paper tape, magnetic tape, or teletype input. The following paragraphs describe the paper tape bootstrap as a typical example.

The wired load program provides the ability to enter an initial package of utility routines, which may subsequently be used to enter and debug more sophisticated programs. These memory address locations have unique characteristics in that they operate in a special type of nondestructive read-out mode. They are not accessible to the programmer for store-type instructions.

The wired memory bootstrap program first locks out all interrupts, then loads in the utility package. The utility package is formulated so that only the basic load routine is read into the memory addresses immediately following the bootstrap program via wired memory load program. Control is then given to a temporary checksum verification routine of the utility package which verifies the basic load routine. A utility package routine then reads the balance of the utility package. If the checksum verification is incorrect, the computer comes to an unconditional stop with AU equal to the tape checksum and AL equal to the load checksum.

b. OPERATING INSTRUCTIONS. - Instructions for the load mode and automatic recovery mode are described below:

(1) LOAD MODE. - The load mode is used when the manual selection of the wired load program is desired and the computer is in the master clear state.

STEP 1. Place paper tape utility package in reader (assuming paper tape input).

STEP 2. Master clear the computer.

STEP 3. Press MODE LOAD switch.

STEP 4. Press RESTART/START STEP switch to RESTART. If tape and load checksums agree, the computer comes to an unconditional stop with AU and AL cleared.

(2) AUTOMATIC RECOVERY MODE. - If a fault condition occurs during the running of a program and the AUTO RECOVERY switch is in the up position, an interrupt addresses 00500_8 (starting address of the wired load program). This locks out all interrupts and initiates the wired load program, which loads in the utility package. For paper tape input, the paper tape utility package must have been placed in the reader (may be positioned on any leader frame) for the recovery to be completed.

NOTE

A fault condition occurring during the running of a program with the AUTO RECOVERY switch in the center position causes a jump to address 00000. Action continues as programmed.

3-6. STANDARD SOFTWARE.

Software packages, TRIM packages, and utility packages for use by the programmer and/or operator are available with the 1219B computer. These packages facilitate the writing and operation of programs. For a complete analysis of these packages and their uses, refer to the 1219B Programmer's Reference Manual, PX 3943-0-3.

3-7. REPERTOIRE OF INSTRUCTIONS.

The repertoire of instructions consists of 102 single-address, flexible instructions. Each instruction contains at least one 6-bit function code that designates which operations are to be performed, and a 12-bit number which may be a memory address or a constant.

a. SYMBOLS USED. - The following symbols are used throughout the description of instructions:

AU	Upper accumulator, 18-bit arithmetic register.
AL	Lower accumulator, 18-bit arithmetic register.
A	AU and AL linked together to form one 36-bit arithmetic register.
B	Contents of the B index register; 18-bit one's complement.
f	Function code, high-order 6 bits of all instruction words.
F	Function code register, 7 bits.
k	Designator contained in Format II instructions, 6 bits. May define shift count, I/O channel number, stop or skip condition, or the contents of the SR or ICR registers.
m	Minor function code contained in Format II instructions, 6 bits.

M	Memory word specified by (y), (y+BO, L(y)(AU) or L(y+B((AU) of compare instruction.
NI	Next instruction.
P	Program address register.
SR	Special register, 5-bit core memory bank designator.
u	Low-order 12 bits contained in Format I instruction words.
u_P	u prefaced with core memory bank designator bits of P.
u_{SR}	u prefaced with core memory bank designator bits of SR.
y	u extended, u_P, or u_{SR}.
Y	Address of constant formed by y or y+B with or without sign extension.
()	Contents of the address or register.
()i	Initial contents of the address or register.
$()_f$	Final contents of the address or register.
$()_n$	Designates any single nth bit of the contents of a register.
(Y+1, Y)	Designates the contents of two consecutive memory locations linked together to form a 36-bit word. Address Y+1 contains the most-significant half of the word while address Y contains the least-significant half.
:	The colon in a logical expression indicates comparison.
L( ) ( ) or ( )⊙( )	The bit-by-bit or logical product (logical AND) defined by the table:

	0	1
0	0	0
1	0	1

( ) v ( )	Logical sum, or inclusive OR defined by the table:

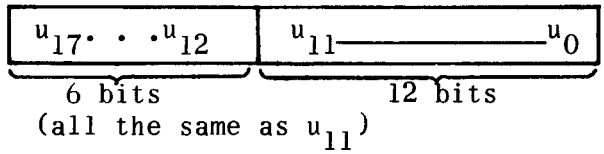
	0	1
0	0	1
1	1	1

( )⊕( )	Half add, half subtract, or exclusive OR defined by the table:

	0	1
0	0	1
1	1	0

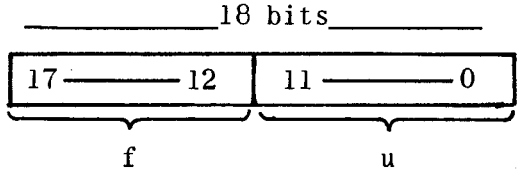
( )' or $\overline{(\ )}$	The one's complement of the contents of the address or register.
( ).( )	Algebraic product of the contents of two locations.
(Y)	When the contents of Y are used as an address, only the lower portion of the word that can be contained in S is transferred.
⟶	Transfer the quantity stated at the left of the symbol to the address or register stated at the right of the symbol.

xY x preceding some symbol indicates that the sign of the 12-bit constant has been extended to produce an 18-bit word, for example,

xY = 

b. INSTRUCTION WORD FORMATS. - Two basic word formats are used by the computer. The descriptions are as follows:

(1) FORMAT I.



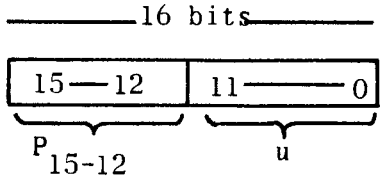
f : function code, six high-order bits

u : 12 low-order bits

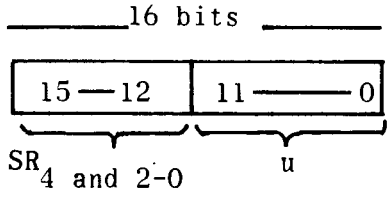
The definition and usage of a u is determined by the function code utilizing u in two distinct manners:

(a) u USED AS A CONSTANT. - For this case, u itself is the operand and requires no further memory reference; however, u is extended to 18 bits. (See list of instructions.)

(b) u USED AS AN ADDRESS. - For this case, u is used as the lower-order 12 bits of the base address referring to a memory location. The base address is 16 bits, designated as u_P or u_{SR}, and is described below.

u_p: 

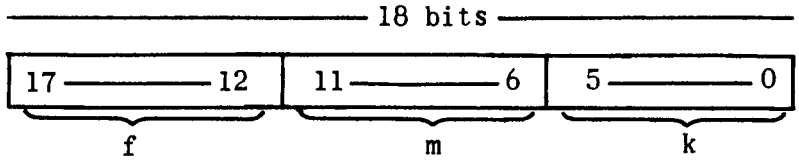
u_P is defined as a 16-bit address; the four high-order bits consist of the four high-order bits of P and the 12 low-order bits are u.

u_{SR}: 

u_{SR} is defined as a 16-bit address; the four high-order bits consist of the three low-order bits of SR and the highest-order bit of SR, and the 12 lower-order bits are u. The peculiar arrangement of bits in the SR register, bit 2^3 being the active bit, was done to insure program compatibility with the 1218 computer.

Certain Format I instructions allow the use of either u_P or u_{SR} as the operand address; for these instructions, u_{SR} is used if SR is active and u_P is used whenever SR is inactive. See list of instructions.

(2) FORMAT II.



f : six-bit function code (always equal to octal 50)

m : six-bit minor function code

k : six low-order bits (channel designator)

c. LIST OF INSTRUCTIONS. - The following pages list the repertoire of instructions for the computer. Common usage and examples are included with instructions where the meaning may not be obvious. No attempt has been made to indicate more sophisticated use. The instructions are listed and defined in the following format:

1) (Octal code) (Instruction name) (TRIM code) (Symbolic summary)

2) (Execution time)

3) (Definition of the y address or constant)

4) (Text defining the instruction in detail)

5) (Examples and/or notes if any)

The symbolic summary expression will use the symbol Y to include y or y+B, whichever is stated in the text for that instruction.

(1) FORMAT I INSTRUCTIONS.

00 ILLEGAL CODE - Jump to fault entrance register, address 0 or
01 address 500 (depending upon position of AUTO RECOVERY switch).

Execution time: 2 microseconds

02 COMPARE AL (CMAL) (AL):(Y)

Execution time: 4 microseconds

Y = u_P or u_{SR}

Compare algebraically (AL) with (y) and set the comparison designator as follows:

1) Set the compare stage

2) Set the greater stage if (AL) > (Y)

3) Set the equals stage if (AL) = (Y)

$(AL)_f = (AL)_i$

NOTE

The comparison designator is cleared by the execution of any subsequent instruction other than codes 60-67, and no interrupt is honored while the designator is set.

03 COMPARE AL (CMALB) (AL):(Y)

Execution time: 4 microseconds

Y = u_P or u_{SR}

Compare algebraically (AL) with (y+B) and set the comparison designator as follows:

1) Set the compare stage

2) Set the greater stage if (AL) > (y+B)

3) Set the equals stage if (AL) = (y+B)

$(AL)_f = (AL)_i$

NOTE

The comparison designator is cleared by the execution of any subsequent instruction other than codes 60-67, and no interrupt is honored while the designator is set.

04 SELECTIVE SUBSTITUTE (SLSU) L(AU)'(AL)+L(AU)(Y) AL or $(Y)_n \rightarrow AL_n$ for $(AU)_n = 1$

Execution time: 4 microseconds

y = u_P or u_{SR}

Replace the individual bits of (AL) with bits of (y) corresponding to ones in (AU), leaving the remaining bits of (AL) unaltered.

$(AU)_f = (AU)_i$

Example of selective substitute:

$(AU)_i$ = 007777 - Mask

(y) = 123451

$(AL)_i$ = 666666

$(AL)_f$ = 663451

05 SELECTIVE SUBSTITUTE (SLSUB) L(AU)'(AL)+L(AU)(Y) → AL

Execution time: 4 microseconds

y = u_P or u_{SR}

Replace the individual bits of (AL) with bits of (y+B) corresponding to ones in (AU), leaving the remaining bits of (AL) unaltered.

$(AU)_f = (AU)_i$

06 COMPARE WITH MASK (CMSK) L(AU)(AL):L(AU)(Y)

Execution time: 4 microseconds

$y = u_P$ or u_{SR}

Algebraically compare selected bits of (AL) with corresponding bits of (y) and set comparison designator as follows:

1) Set the compare stage

2) Set the greater stage if L(AL)(AU) > L(y)(AU)

3) Set the equals stage if L(AL)(AU) = L(y)(AU)

$(AL)_f = (AL)_i$: $(AU)_f = (AU)_i$

NOTE

The comparison designator is cleared by the execution of any subsequent instruction other than codes 60-67, and no interrupt is honored while the designator is set.

Example of compare with mask:

$(AU)_i$ = 007777 - Mask

(y) = 123451

$(AL)_i$ = 222351

Compare 2351 with 3451

$(AU)_f$ = 007777: $(AL)_f$ = 222351

07 COMPARE WITH MASK (CMSKB) L(AU)(AL):(AU)(Y)

Execution time: 4 microseconds

$y = u_P$ or u_{SR}

Algebraically compare selected bits of (AL) with corresponding bits of (y+B), and set the comparison designator as follows:

1) Set the compare stage

2) Set the greater stage if L(AL)(AU) > L(y+B)(AU)

3) Set the equals stage if L(AL)(AU) = L(y+B)(AU)

$(AL)_f = (AL)_i$: $(AU)_f = (AU)_i$

NOTE

The comparison designator is cleared by the execution of any subsequent instruction other than codes 60-67, and no interrupt is honored while the designator is set.

10 ENTER AU (ENTAU) (Y)→ AU

Execution time: 4 microseconds

$y = u_P$ or u_{SR}

Clear AU. Then transmit (y) to AU.

11 ENTER AU (ENTAUB) (Y) → AU

Execution time: 4 microseconds

$y = u_P$ or u_{SR}

Clear AU. Then transmit (y+B) to AU.

12 ENTER AL (ENTAL) (Y) ⟶ AL

Execution time: 4 microseconds

$y = u_P$ or u_{SR}

Clear AL. Then transmit (y) to AL.

13 ENTER AL (ENTALB) (Y) ⟶ AL

Execution time: 4 microseconds

$y = u_P$ or u_{SR}

Clear AL. Then transmit (y+B) to AL.

14 ADD AL (ADDAL) (AL)+(Y) ⟶ AL

Execution time: 4 microseconds

$y = u_P$ or u_{SR}

Add (y) to (AL) and leave the result in AL. Set overflow designator if overflow occurs.*

$(AL)_f$ are all ones if $(AL)_i$ and (y) are all ones.

15 ADD AL (ADDALB) (AL)+(Y) ⟶ AL

Execution time: 4 microseconds

$y = u_P$ or u_{SR}

Add (y+B) to (AL) and leave the result in AL. Set overflow designator if overflow occurs.*

$(AL)_f$ are all ones if $(AL)_i$ and (y+B) are all ones.

16 SUBTRACT AL (SUBAL) (AL)-(Y) ⟶ AL

Execution time: 4 microseconds

$y = u_P$ or u_{SR}

Subtract (y) from (AL) and leave the difference in AL. Set overflow designator if overflow occurs.*

$(AL)_f$ are all ones if $(AL)_i$ are all ones and (y) are all zeros.

17 SUBTRACT AL (SUBALB) (AL)-(Y) ⟶ AL

Execution time: 4 microseconds

$y = u_P$ or u_{SR}

Subtract (y+B) from (AL) and leave the difference in AL. Set overflow designator if overflow occurs.*

$(AL)_f$ are all ones if $(AL)_i$ are all ones and (y+B) are all zeros.

* The overflow designator is cleared only by the execution of instruction skip-on-overflow (f m = 50:52) or instruction skip-on-no overflow (f m = 50:53).

20 ADD A (ADDA) $(A)+(Y+1,Y) \rightarrow A$

Execution time: 6 microseconds

$y = u_P$ or u_{SR}

Add to (A) the double length (36-bit) number contained in storage cells y+1 and y, and leave the result in A. Set overflow designator if overflow occurs.* The least-significant half is in cell y and the most-significant half in y+1. The sign of the double length number is indicated by the most-significant bit of (y+1). Address y must be even; for example, the right-most octal digit must be 0, 2, 4, or 6.

NOTE

The instruction is executed in the following manner: The AU and AL registers are linked to form a continuous 36-bit A register. Any borrow required by AL comes from AU; any end-around-borrow required by AU is blocked and recorded in the borrow designator, leaving A uncorrected. The skip-on-no-borrow instruction (code 50:51) is used to test for required correction. Only add A or subtract A instructions set the designator.

Example of a double add with y = 07506:

$(A)_i$ = 201007430145

Address 07506 = 351123 (least-significant half)

Address 07507 = 077430 (most-significant half)

$(A)_f$ = 300440001271 - The result may be incorrect since the addition of some numbers results in an end-around-borrow. Since it is blocked, the result will be 1 larger than it should be (as in the example).

21 ADD A (ADDAB) $(A)+(Y+1,Y) \rightarrow A$

Execution time: 6 mircroseconds

$y = u_P$ or u_{SR}

Add to (A) the double length (36-bit) number contained in storage cells y+B+1 and y+B, leaving the result in A. Set overflow designator if overflow occurs.* The least-significant half is in cell y+B and the most-significant half in cell y+B+1. The sign of the double length number is the sign of (y+B+1). Address y+B must be even. (See note, instruction 20.)

22 SUBTRACT A (SUBA) $(A)-(Y+1,Y) \rightarrow A$

Execution time: 6 microseconds

$y = u_P$ or u_{SR}

* The overflow designator is cleared only by the execution of instruction skip-on-overflow (f m = 50:52) or instruction skip-on-no-overflow (f m = 50:53).

Subtract from (A) the double length (36-bit) number contained in storage cells y+1 and y, and leave the difference in A. Set overflow designator if overflow occurs.* The least-significant half is in cell y and the most-significant half in cell y+1. The sign of the double length number is the sign of (y+1). Address y must be even. The computer executes subtract A in a manner analogous to the add A instruction. (See note, instruction 20.)

23 SUBTRACT A (SUBAB) (A)-(Y+1,Y) ⟶ A

Execution time: 6 microseconds

$y = u_P$ or u_{SR}

Subtract from (A) the double length number contained in storage cells y+B+1 and y+B, and leave the difference in A. Set overflow designator if overflow occurs.* The least-significant half is in cell y+B and the most-significant half in cell y+B+1. The sign of the double length number is the sign of (y+B+1). Address y+B must be even. The computer executes subtract A in a manner analogous to the add A instruction. (See note, instruction 20.)

24 MULTIPLY AL (MULAL) (AL)x(Y) ⟶ A

Execution time: 14 microseconds

$y = u_P$ or u_{SR}

Multiply (AL) by (y) leaving the double length product in A. If the factors are considered integers, the product is an integer in A. The multiplication process is executed on the absolute value of the factors, then corrected for algebraic sign.

25 MULTIPLY AL (MULALB) (AL)x(Y) ⟶ A

Execution time: 14 microseconds

$y = u_P$ or u_{SR}

Multiply (AL) by (y+B) leaving the double length product in A. If the factors are considered integers, the product is an integer in A. The multiplication process is executed on the absolute value of the factors, then correct for algebraic sign.

26 DIVIDE A (DIVA) (A)÷(Y); Quot ⟶ AL, Rem ⟶ AU

Execution time: 14 microseconds

$y = u_P$ or u_{SR}

Divide (A) by (y) leaving the quotient in AL and the remainder in AU. The remainder always bears the sign of the dividend A_i with the results satisfying the relationship:

dividend = quotient x divisor + remainder

* The overflow designator is cleared only by the execution of instruction skip-on-overflow (f m = 50:52) or instruction skip-on-no-overflow (f m = 50:53).

Set overflow designator if overflow occurs.* Examples of the four possible sign combinations of the dividend/divisor and the results:

Dividend	Divisor	Quotient	Remainder
+5	+4	+1	+1
+5	-4	-1	+1
-5	+4	-1	-1
-5	-4	+1	-1

27 DIVIDE A (DIVAB) (A)÷(Y); Quot → AL, Rem → AU

Execution time: 14 microseconds

$y = u_P$ or u_{SR}

Divide (A) by (y+B), leaving the quotient in AL and the remainder in AU. The remainder bears the sign of the dividend A_i. (See instruction 26.)

30 INDIRECT RETURN JUMP (IRJP) (P)+1 → (Y); (Y)+1 → P

Execution time: 6 microseconds

Instruction executed from running program: $y = u_p$

Store (P)+1 at the address which is the low-order bits of (y), then increment that address by one (1) and enter it into the program address register.

Instruction executed from entrance register on interrupt: y = u

Store (P) at the address which is the low-order bits of (y), then increment that address by one (1) and enter it into the program address register.

Example of an indirect return jump executed from address 22000:

Address	Initial Contents	Final Contents	Explanation
22000	30 6500	Same	Execute subroutine from main program.
26500	71 7420	Same	Constant defining location of desired subroutine.
117420	37 2164	02 2001	Subroutine exit address.
117421	.. ....	Same	Subroutine entrance address (control is transferred here from indirect return jump).

The effect of the above sequence, upon execution of the indirect return jump at address 22000, is to transfer control to the subroutine starting at address 117421, but at the same time letting the subroutine know where to return control.

* The overflow designator is cleared only by the execution of instruction skip-on-overflow (f m = 50:52) or instruction skip-on-no-overflow (f m = 50:53).

31 INDIRECT RETURN JUMP (IRJPB) (P)+1 ⟶ (Y); (Y)+1 ⟶ P

Execution time: 6 microseconds

Instruction executed from running program: $y = u_p$

Store (P)+1 at the address which is the low-order bits of (y+B), then increment that address by one (1), and enter it into the program address register.

Instruction executed from entrance register on interrupt: $y = u$

Store (P) at the address which is the low-order bits of (y+B), then increment that address by one (1) and enter it into the program register.

32 ENTER B (ENTB) (Y) ⟶ B, Reg

Execution time: 4 microseconds

$y = u_P$ or u_{SR}

Transmit (y) to B_{ICR}

The full 18 bits of (y) are transmitted to the B register (a normally addressable memory location).

33 ENTER B (ENTBB) (Y) ⟶ B Reg

Execution time: 4 microseconds

$y = u_P$ or u_{SR}

Transmit (y+B) to B_{ICR}

The full 18 bits of (y+B) are transmitted to the B register (a normally addressable memory location).

34 DIRECT JUMP (JP) Y ⟶ P; NI = (Y)

Execution time: 2 microseconds

$y = u_P$

Unconditional jump to y. (Set P = y.)

35 DIRECT JUMP (JPB) Y ⟶ P; NI = (Y)

Execution time: 2 microseconds

$y = u_P$

Unconditional jump to y+B.

NOTE

Since B is an 18-bit, one's-complement number, care must be taken when using this instruction. In addition, it is possible that the address y+B may not be relative to the same core bank from which the (35) DIRECT JUMP was executed: consider a direct jump with y = 03560 and b = 010000. In this case y+B = 03560 + 010000 = 13560.

36 ENTER B WITH CONSTANT (ENTBK) xY ⟶ B Reg

Execution time: 2 microseconds

y = u (sign extended to 18 bits)

Clear B_{ICR} then transmit y to B_{ICR}

NOTE

u is a 12-bit, one's-complement number contained within the instruction; it does not refer to an address. Example of enter B with constant when u = 7701:

B_i = any value

B_f = 777701

37 MODIFY B WITH CONSTANT (ENTBKB) B_i + xY ⟶ B Reg

Execution time: 2 microseconds

y = u (sign extended to 18 bits)

Add y to B (add a constant to B). Note that u is a 12-bit, one's-complement number contained within the instruction and can be used to increment or decrement B.

40 CLEAR Y (STORE ZERO) (CL) 0 ⟶ Y

Execution time: 4 microseconds

y = u_P or u_{SR}

Store an 18-bit word of zeros at storage address y.

41 CLEAR Y (STORE ZERO) (CLB) 0 ⟶ Y

Execution time: 4 microseconds

y = u_P or u_{SR}

Store an 18-bit word of zeros at storage address y+B.

42 STORE B (STRB) B ⟶ Y

Execution time: 4 microseconds

y = u_P or u_{SR}

Store B at storage address y.

43 STORE B (STRBB) B ⟶ Y

Execution time: 4 microseconds

y = u_P or u_{SR}

Store B at storage address y+B.

44 STORE AL (STRAL) (AL) → Y

Execution time: 4 microseconds

$y = u_P$ or u_{SR}

Store (AL) at storage address y.

$(AL)_f = (AL)_i$

45 STORE AL (STRALB) (AL) → Y

Execution time: 4 microseconds

$y = u_P$ or u_{SR}

Store (AL) at storage address y+B.

$(AL)_f = (AL)_i$

46 STORE AU (STRAU) (AU) → Y

Execution time: 4 microseconds

$y = u_P$ or u_{SR}

Store (AU) at storage address y.

$(AU)_f = (AU)_i$

47 STORE AU (STRAUB) (AU) → Y

Execution time: 4 microseconds

$y = u_P$ or u_{SR}

Store (AU) at storage address y+B.

$(AU)_f = (AU)_i$

50 (See format II instructions immediately following function code 77.)

51 SELECTIVE SET (SLSET) (AL) v (Y) → AL or SET $(AL)_n$ for $(Y)_n = 1$

Execution time: 4 microseconds

$y = u_P$

Set the individual bits of (AL) to one corresponding to ones in (y), leaving the remaining bits of (AL) unaltered. This is a bit-by-bit inclusive OR.

Example of selective set:

$(AL)_i = 123456$

$(y) = 000077$

$(AL)_f = 123477$

52 SELECTIVE CLEAR (SLCL) L(AL)(Y) → AL or clear $(AL)_n$ for $(Y)_n = 0$

Execution time: 4 microseconds

$y = u_P$

Clear the individual bits of (AL) corresponding to zeros in (y), leaving the remaining bits of (AL) unaltered. The effect of this instruction is to compute the bit-by-bit (or logical) product of (AL) and (y) leaving the result in AL.

Example of selective clear:

$(AL)_i$ = 123456

(y) = 707070

$(AL)_f$ = 103050

53 SELECTIVE COMPLEMENT (SLCP) $(AL) \oplus (Y) \longrightarrow AL$ or complement $(AL)_n$ for $(Y)_n = 1$

Execution time: 4 microseconds

$y = u_P$

Complement the individual bits of (AL) corresponding to ones in (y), leaving the remaining bits of (AL) unaltered, for example, complement $(AL)_n$ for $(y)_n = 1$. This is a bit-by-bit exclusive OR.

Example of selective complement instruction:

$(AL)_i$ = 123456

(y) = 070007

$(AL)_f$ = 153451

54 INDIRECT JUMP AND ENABLE INTERRUPTS (IJPEI) $(Y) \longrightarrow P$; enable interrupts

Execution time: 4 microseconds

$y - u_P$ Address - $(y)_{15-0}$

Remove interrupt lockout (enable interrupts). Then jump to the address which is the low order bits of (y). An application of this instruction is the termination of a subroutine activated by an interrupt.

55 INDIRECT JUMP (IJP) $(Y) \longrightarrow P$

Execution time: 4 microseconds

$y = u_P$ Address = $(y)_{15-0}$

Jump to the address which is the low order bits of (y).

56 B SKIP (BSK) If B = (Y), skip NI
If B $\neq$ (Y), (B)+1 $\longrightarrow$ B, read NI

Execution time: 4 microseconds

$y = u_P$

Test B and (y) for equality. Skip next instruction if equal; otherwise increment B by one and read the next instruction.

57 INDEX SKIP (ISK)

If (Y) = 0, skip NI
If (Y) ≠ 0, (Y)-1 → Y, read NI

Execution time: 6 microseconds

$y = u_P$

If (y) ≠ 0, subtract one from (y) leaving the result in y, and take the next instruction; otherwise skip the next instruction leaving (y) unaltered.

60 JUMP AU ZERO (JPAUZ)

If [$\overline{\text{compare}}$ · (AU)=0] ⊕
[compare · (AL)=M ⊕
L(AL)(AU=M]: Y → P

Execution time: 2 microseconds

$y = u_P$

Jump to y; for example, set P = y, if:

1) Compare stage of the comparison designator is not set and (AU) = 0. (Negative zero acts as not zero.)

or

2) Compare stage of the comparison designator is set and the equals stage of the comparison designator is set.

Otherwise, execute next instruction.

61 JUMP AL ZERO (JPALZ)
(JPEQ)

If [$\overline{\text{compare}}$ · (AL)=0] ⊕
[compare · (AL)=M ⊕
L(AL)(AU)=M]: Y → P

Execution time: 2 microseconds

$y = u_P$

JUMP to y; for example, set P = y, if:

1) Compare stage of the comparison designator is not set and (AL) = 0. (Negative zero acts as not zero.)

2) Compare stage of the comparison designator is set, and the equals stage of the comparison designator is set.

Otherwise, execute next instruction.

62 JUMP AU NOT ZERO (JPAUNZ)

If [$\overline{\text{compare}}$ · (AU)≠0] ⊕
compare · (AU)≠M ⊕
L(AL)(AU)≠M]: Y → P

Execution time: 2 microseconds

$y = u_P$

Jump to y; for example, set P = y, if:

1) Compare stage of comparison designator is not set and (AU) ≠ 0.

or

2) Compare stage of comparison designator is set and the equals stage of the comparison designator is not set.

Otherwise, execute next instruction.

63 JUMP AL NOT ZERO (JPALNZ) (JPNOT)

If [$\overline{\text{compare}}$ · (AL)≠0] ⊕ [compare · (AL)≠M ⊕ L(AL)(AU)≠M] : Y → P

Execution time: 2 microseconds

$y = u_P$

Jump to y; for example, set P = y, if:

1) Compare stage of comparison designator is not set and (AL) ≠ 0.

or

2) Compare stage of comparison designator is set and the equals stage of the comparison designator is not set.

Otherwise, execute next instruction.

64 JUMP AU POSITIVE (JPAUP)

If [$\overline{\text{compare}}$ · (AU) Pos] ⊕ [compare · (AL) ≥ M ⊕ L(AL)(AU) ≥ M] : Y → P

Execution time: 2 microseconds

$y = u_P$

Jump to y; for example, set P = y, if:

1) Compare stage of comparison designator is not set and (AU) ≥ 0.

or

2) Compare stage of comparison designator is set and the greater stage of comparison designator is set.

Otherwise, execute next instruction.

65 JUMP AL POSITIVE (JPALP) (JPMLEQ)

If [$\overline{\text{compare}}$ · (AL) Pos] ⊕ compare · (AL) ≥ M ⊕ L(AL)(AU) ≥ M : Y → P

Execution time: 2 microseconds

$y = u_P$

Jump to y; for example, set P = y, if:

1) Compare stage of comparison designator is not set and (AL) ≥ 0.

or

2) Compare stage of comparison designator is set and the greater stage of comparison designator is set.

Otherwise, execute next instruction.

66 JUMP AU NEGATIVE (JPAUNG) If[$\overline{\text{compare}}$ • (AU) Neg]⊕ compare • (AL) < M⊕ L(AL)(AU) < M] : Y → P

Execution time: 2 microseconds

$y = u_P$

Jump to y; for example, set P = y, if:

1) Compare stage of comparison designator is not set and (AU) < 0.

or

2) Compare stage of comparison designator is set and the greater stage of comparison designator is not set.

Otherwise, execute next instruction.

67 JUMP AL NEGATIVE (JPALNG) (JPMGR) If[$\overline{\text{compare}}$ • (AL) Neg]⊕ compare • (AL) < M⊕ L(AL)(AU) < M] : Y → P

Execution time: 2 microseconds

$y = u_P$

Jump to y; for example, set P = y, if:

1) Compare stage of comparison designator is not set and (AL) < 0.

or

2) Compare stage of comparison designator is set and the greater stage of comparison designator is not set.

Otherwise, execute next instruction.

70 ENTER AL WITH CONSTANT (ENTALK) xY → AL

Execution time: 2 microseconds

y = u (with sign extended to 18 bits)

Clear AL. Then transmit y to AL.

Example of enter AL with constant when u = 0001

$(AL)_i$ = any value

$(AL)_f$ = 000001 (+1)

Example of enter AL with constant when u = 7776

$(AL)_i$ = any value

$(AL)_f$ = 777776 (-1)

NOTE

u is a 12-bit, one's complement number contained within the instruction; it does not refer to an address.

71 ADD CONSTANT TO AL (ADDALK) (AL) + xY ⟶ AL

Execution time: 2 microseconds

y = u (sign extended to 18 bits)

Add y to (AL) and leave the result in AL. The effect of this instruction is to increment/decrement (AL) with a constant contained within the instruction.

Example of add constant to AL when u = 0002 (+2)

$(AL)_i$ = 057777

$(AL)_f$ = 060001 (incremented)

Example of add constant to AL when u = 7775 (-2)

$(AL)_i$ = 067055

$(AL)_f$ = 067053 (decremented)

72 STORE INDEX CONTROL REGISTER (STRICR) (ICR) ⟶ Y_{5-0}

Execution time: 4 microseconds

$y = u_p$

Replace the low-order six bits of (y) with a six-bit value consisting of the four, lower-order bits equal to the contents of the index control register and the remaining two bits equal to zero. As this instruction affects a six-bit partial transfer, the upper 12 bits of (y) remain unchanged. $(ICR)_i = (ICR)_f$

NOTE

To clear the index control register see f = 50 72.

73 B JUMP (BJP) If B ≠ 0, B-1 ⟶ B Reg & Y ⟶ P
If B = 0, Execute NI

Execution time: 2 microseconds

$y = u_p$

If B ≠ 0, subtract one from B, then jump to y; otherwise, take the next instruction leaving B unaltered (neg zero ≠ 0).

NOTE

As B is a one's-complement number and can take values less than zero, the B jump will be effective only for program loops where B is initially positive.

74 STORE ADDRESS (STRADR) $(AL)_{11-0}$ ⟶ Y_{11-0}

Execution time: 4 microseconds

$y = u_p$

Replace the low-order 12 bits of (y) with the low-order 12 bits of (AL). As this instruction affects a partial transfer, the higher-order six bits of (y) remain undisturbed.

$(AL)_f = (AL)_i$

Examples of a store address instruction:

$(AL)_i = 762504$

$(y)_i = 567777$

$(y)_f = 562504$

75 STORE SPECIAL REGISTER (STRSR) $(SR) \longrightarrow Y_{5-0}$

Execution time: 4 microseconds

$y = u_P$

Replace the low-order six bits of (y) with a six-bit value of which the five low-order bits are equal to (special register) with the remaining bits equal to zero; store the result at y, then clear the active bit of the special register. As this instruction affects a six-bit partial transfer, the upper 12 bits of (y) remain undisturbed.

NOTE

This instruction deactivates the special register but does not clear the other 4 bits.

76 DIRECT RETURN JUMP (RJP) $(P)+1 \longrightarrow Y$; $Y+1 \longrightarrow P$

Execution time: 4 microseconds

$y = u_P$

Store (P)+1 at y, then jump to y+1. This instruction transfers to y a full 18-bit word, the lower bits being the address (P)+1 with the upper bits set to zero.

When this instruction is executed from an interrupt entrance register by an interrupt, store (P). Do not initiate the (P)+1 sequence.

77 ILLEGAL CODE - Jump to fault entrance register, address 0, or address 500 (depending on position of AUTO RECOVERY switch)

Execution time: 2 microseconds

(2) FORMAT II INSTRUCTIONS. - The following are Format II, type 3 instructions and require a combination of a 50 function code and a subfunction code that determines the operation to be performed. The 50 code is detected when read from memory and causes $1 \longrightarrow F_6$ and $Z_{11-6} \longrightarrow F_{5-0}$ for execution. The computer maintains its regular timing sequence, plus a Format II sequence.

50:00 Not used

50:01 SET INPUT ACTIVE (SIN)

Execution time: 2 microseconds

Set input channel k to the active state. The buffer control words stored in memory locations 60 + 2k and 61 +2k (channels 0-7) or 260 + 2(k-10) and 261 + 2(k-10) (channels 10-17) or as specified by the externally specified index or externally specified address will control the transfers.

50:02 SET OUTPUT ACTIVE (SOUT)

Execution time: 2 microseconds

Set output channel k to the active state. The buffer control words stored in memory locations 40 + 2k and 41 + 2k (channels 0-7) or 240 + 2(k-10) and 241 + 2(k-10) (channels 10-17) or as specified by the ESI or ESA will control the transfers.

50:03 SET EXTERNAL FUNCTION ACTIVE (SEXF)

Execution time: 2 microseconds

Set channel k external function mode active. The buffer control words stored in memory locations 20 + 2k and 21 + 2k (channels 0-7) or 220 + 2(k-10) and 221 + 2(k-10) (channels 10-17) will control the transfers.

50:04 Not used

50:05 Not used

50:06 Not used

50:07 Not used

50:10 Not used

50:11 INPUT TRANSFER (IN)

	Channels 0-7	Channels 10-17
	(P+1) → 60+2K	(P+1) → 260+2(K-10)
	(P+2) → 61+2k	(P+2) → 261+2(K-10)

Set input active on channel k.

Execution time: 6 microseconds

Initiate input transfer on channel k.

Transfer buffer limit address words (for input buffer) from the following two addresses to the input buffer control registers for the designated channel. (Other I/O channel and processer activity proceeds normally.)

50:12 OUTPUT TRANSFER (OUT)

	Channels 0-7	Channels 10-17
	(P+1) → 40+2k	(P+1) → 240+2(K-10)
	(P+2) → 41+2K	(P+2) → 241+2(K-10)

Set output active on channel k.

Execution time: 6 microseconds

Initiate output transfer on channel k.

Transfer buffer limit address words (for output buffer) from the following two instruction locations to the output buffer control registers for the designated channel. (Other I/O channel and processor activity proceeds normally.)

50:13 EXTERNAL FUNCTION (EXF)

Channels 0-7	Channels 10-17
(P+1) → 20+2k	(P+1) → 220+2(k-10)
(P+2) → 21+2k	(P+2) → 221+2(k-10)

Set external function active on channel k.

Execution time: 6 microseconds

Initiate external function transfer on channel k.

Transfer buffer limit addresses (for the function words to be used) from the following two instruction locations to the external function buffer control registers for the designated channel.

50:14 ENABLE REAL-TIME CLOCK MONITOR (RTC)

Execution time: 2 microseconds

Enable the real-time clock monitor interrupt; ignore k.

After execution of this instruction, equality between the RTC word register (location 15) and the RTC monitor word register (location 14) will interrupt the computer program. The next instruction is taken from the RTC monitor interrupt entrance register (location 12) and the RTC monitor is disabled.

50:15 TERMINATE INPUT (INSTP) Clear input active channel k.

Execution time: 2 microseconds

No monitor interrupt will occur as a result of the execution of this instruction.

50:16 TERMINATE OUTPUT (OUTSTP) Clear output active channel k.

Execution time: 2 microseconds

Terminate output on channel k.

No monitor interrupt will occur as a result of the execution of this instruction.

50:17 TERMINATE EXTERNAL FUNCTION (EXFSTP) Clear external function active channel k.

Execution time: 2 microseconds

Terminate external function on channel k.

No monitor interrupt will occur as a result of the execution of this instruction.

50:20 SET RESUME (SRSM) Set resume FF channel group K.

Execution time: 2 microseconds

Set the resume designator for the channel group specified by k to permit honoring the next requesting EF/OD function. Loss of any information currently held by the output register(s) for a peripheral device is allowed by this instruction.

50:21 SKIP ON INPUT INACTIVE (SKPIIN)

Execution time: 2 microseconds skip or no skip

Test for input buffer active on channel k. If inactive, skip the next instruction; otherwise, take next instruction.

50:22 SKIP ON OUTPUT INACTIVE (SKPOIN)

Execution time: 2 microseconds skip or no skip

Test for output buffer active on channel k. If inactive, skip the next instruction; otherwise, take the next instruction.

50:23 SKIP ON EXTERNAL FUNCTION INACTIVE (SKPEIN)

Execution time: 2 microseconds skip or no skip

Test for external function activity on channel k. If inactive, skip the next instruction; otherwise, take the next instruction.

50:24 WAIT FOR INTERRUPT (WTFI)
or
50:25 Execution time: 2 microseconds

Stop the computer until any interrupt occurs; ignore k, then execute the instruction located in the interrupt entrance register designated by the interrupt.

50:26 OUTPUT OVERRIDE (OUTOV)

Execution time: 2 microseconds

Wait for the output device to accept the word in the C register(s). Then simulate an output request on channel k and transfer the word designated by the address in the output buffer control register for that channel. Ignore the ESI or ESA mode if active. This instruction will transfer a word whether the buffer is active or not. Also, since the transfer takes place under control of the word in the buffer control register, the two buffer control words must not be equal. Equality terminates the action and no word will be transferred.

50:27 EXTERNAL FUNCTION OVERRIDE (EXFOV)

Execution time: 2 microseconds

Wait for the output device to accept the word in the C register(s). Then simulate an external function request on channel k and transfer the word designated by the address in the external function buffer control register for that channel. Ignore the ESI or ESA mode if active. This instruction transfers a word whether the buffer is active or not. Also, since the transfer takes place under control of the word in the buffer control register the two buffer control words must not be equal. Equality terminates the action and no word is transferred.

50:30 REMOVE INTERRUPT LOCKOUT (RIL)
or
50:31 Execution time: 2 microseconds

Remove the interrupt lockout - enable all interrupts, all channels; ignore k.

NOTE

A 50:30 or 50:31 instruction must be used in conjunction with a 50:34 or 50:35 instruction. It does not affect a 50:36 or 50:37 instruction.

50:32 REMOVE EXTERNAL INTERRUPT LOCKOUT (RXL)
or
50:33 Execution time: 2 microseconds

Remove the external interrupt lockout - enable external interrupts, all channels; ignore k.

NOTE

A 50:32 or 50:33 instruction must be used in conjunction with a 50:36 or 50:37 instruction. It does not affect a 50:34 or 50:35 instruction.

50:34 SET INTERRUPT LOCKOUT (SIL)
or
50:35 Execution time: 2 microseconds

Set the interrupt lockout - disable all interrupts, all channels; ignore k.

50:36 SET EXTERNAL INTERRUPT LOCKOUT (SXL)
or
50:37 Execution time: 2 microseconds

Set the external interrupt lockout - disable external interrupts, all channels; ignore k.

50:40 Not used

50:41 RIGHT SHIFT AU (RSHAU)

Execution time:

4 usec (k = 0-4)	14 usec (k = 21-24)
6 usec (k = 5-8)	16 usec (k = 25-28)
8 usec (k = 9-12)	18 usec (k = 29-32)
10 usec (k = 13-16)	20 usec (k = 33-35)
12 usec (k = 17-20)	

Shift (AU) to the right, k bit positions. The higher-order bits are replaced with the original sign bit, AU_{17}, as the value is shifted. This is an end-off shift; for example, the low-order bits are lost upon completion of the shift.

Example of right shift AU with k = 2.

$(AU)_i$ (positive)	=	370000
After first shift	=	174000
After second shift	=	076000
$(AU)_i$ (negative)	=	400000
After first shift	=	600000
After second shift	=	700000

50:42 RIGHT SHIFT AL (RSHAL)

Execution time: Same as instruction 50:41

Shift (AL) to the right, k-bit positions. The higher-order bits are replaced with the original sign bit (AL_{17}) as the value is shifted. This is an end-off shift; for example, the low-order bits are lost upon completion of the shift.

50:43 RIGHT SHIFT A (RSHA)

Execution time: Same as instruction 50:41

Shift (A) to the right, k-bit positions. The higher-order bits are replaced with the original sign bit (A_{35}) as the value is shifted. This is an end-off shift; for example, the low-order bits are lost upon completion of the shift.

Example of right shift A with k = 2.

		AU	AL
$(A)_i$ (positive)	=	370000	000000
After first shift	=	174000	000000
After second shift	=	076000	000000
$(A)_i$ (negative)	=	400000	000000
After first shift	=	600000	000000
After second shift	=	700000	000000

50:44 SCALE FACTOR (SF)

Execution time:

6 usec (k = 0-4)	16 usec (k = 21-24)
8 usec (k = 5-8)	18 usec (k = 25-28)
10 usec (k = 9-12)	20 usec (k = 29-32)
12 usec (k = 13-16)	22 usec (k = 33-35)
14 usec (k = 17-20)	

Shift (A) circularly to the left until either $A_{35} \neq A_{34}$ or k-minus-shift-count = 0; then store the positive quantity k minus shift count at memory address 00017. The effect of the instruction is to normalize (A) to the left subject to k. Scale factor is extremely useful when working with numerical values in floating point notation.

1) Example of scale factor with k = 7:

   $(A)_i$ = 170000 000000 (positive, not normalized)

   After first shift = 360000 000000 (positive, normalized)

   The computer, sensing (A) now normalized, stores k - shift count (7-1) = the 18-bit quantity 000006 ⟶ 00017.

2) Example of scale factor with k = 3:

   $(A)_i$ = 600000 000000 (negative, not normalized)

   After first shift = 400000 000000 (negative, normalized)

   The computer then stores the quantity 000002 ⟶ 00017.

3) Example of scale factor with k = 1:

   $(A)_i$ = 070000 000000 (positive, not normalized)

   After first shift = 160000 000000 (positive, not normalized)

   The computer, having exhausted k, stores the quantity 000000 ⟶ 00017 leaving (A) only partially normalized.

50:45 LEFT SHIFT AU (LSHAU)

Execution time: Same as instruction 50:41

Shift (AU) circularly to the left, k-bit positions. The lower-order bits are replaced with the higher-order bits as the word is shifted. No bits are lost with the execution of left shift instructions.

Example of left shift AU with k = 2.

$(AU)_i$ = 300000

After first shift = 600000

After second shift = 400001

50:46 LEFT SHIFT AL (LSHAL)

Execution time: Same as instruction 50:41

Shift (AL) circularly to the left, k-bit positions. The lower-order bits are replaced with the higher-order bits as the word is shifted. No bits are lost with the execution of left shift instructions.

50:47 LEFT SHIFT A (LSHA)

Execution time: Same as instruction 50:41

Shift (A) circularly to the left, k-bit positions. The lower-order bits are replaced with the higher-order bits as the word is shifted. No bits are lost with the execution of left shift instructions.

Example of left shift A with k = 2.

$(A)_i$	= 300000 000000
After first shift	= 600000 000000
After second shift	= 400000 000001

50:50 SKIP ON KEY SETTING (SKP)

Execution time: 2 microseconds skip or no skip

If bit 4, 3, 2, 1 or 0 of k is one and the corresponding skip key 4, 3, 2, 1, or 0 is set; or, if bit 5 of k is a one, skip the next instruction; otherwise, take the next instruction.

Examples of skip with:

k = 01 (bit 0)	Skip if skip key #0 is set.
k = 02 (bit 1)	Skip if skip key #1 is set.
k = 04 (bit 2)	Skip if skip key #2 is set.
k = 10 (bit 3)	Skip if skip key #3 is set.
k = 20 (bit 4)	Skip if skip key #4 is set.
k = 40 (bit 5)	Skip unconditionally.
k = 03 (bits 1,0)	Skip if either key #1 or #0 is set.

50:51 SKIP ON NO BORROW (SKPNBO)

Execution time: 2 microseconds skip or no skip

If the last previous add A or subtract A required a borrow, take the next instruction; otherwise, skip the next instruction; ignore k. The skip occurs if no correction to (A) is needed. This allows a correcting instruction to be inserted to save program steps. The correcting instruction will be subtract A where (Y+1,Y) = 000000000001.

50:52 SKIP ON OVERFLOW (SKPOV)

Execution time: 2 microseconds skip or no skip

If an overflow condition occurred on a previous arithmetic instruction, skip the next instruction; othrwise, take the next instruction. Ignore k and clear the overflow designator.

50:53 SKIP ON NO OVERFLOW (SKPNOV)

Execution time: 2 microseconds skip or no skip

If an overflow condition did not occur on any previous arithmetic instruction, skip the next instruction; otherwise, take the next instruction. Ignore k and clear the overflow designator.

50:54 SKIP ON ODD PARITY (SKPODD)

Execution time: 2 microseconds skip or no skip

If the sum of the bits resulting from the bit-by-bit product of (AL) and (AU) is odd, skip the next instruction; otherwise, take the next instruction. Ignore k.

$(AU)_f = (AU)_i$; $(AL)_f = (AL)_i$

Example of skip odd parity:

(AU)	= 000077 mask
(AL)	= 127723
bit-by-bit product	= 000023
bit sum	= 3

Since the bit sum is odd, the next instruction is skipped.

50:55 SKIP ON EVEN PARITY (SKPEVN)

Execution time: 2 microseconds skip or no skip

If the sum of the bits resulting from the bit-by-bit product of (AL) and (AU) is even, skip the next instruction; otherwise, take the next instruction. Ignore k.

$(AL)_f = (AL)_i$; $(AU)_f = (AU)_i$

50:56 STOP ON KEY SETTING (STOP)

Execution time: 2 microseconds

If bit 4, 3, 2, 1, or 0 of k is one and the corresponding console stop key 4, 3, 2, 1, or 0 is set; or, if bit 5 of k is one, stop the computer; otherwise, take the next instruction.

Examples of stop with:

k = 01 (bit 0)	Stop if stop key #0 is set.
k = 02 (bit 1)	Stop if stop key #1 is set.
k = 04 (bit 2)	Stop if stop key #2 is set.
k = 10 (bit 3)	Stop if stop key #3 is set.
k = 20 (bit 4)	Stop if stop key #4 is set.
k = 40 (bit 5)	Stop unconditionally.
k = 03 (bits 1,0)	Stop if either stop key #1 or #0 is set.

50:57 SKIP ON NO RESUME (SKPNR)

Execution time: 2 microseconds skip or no skip

If the resume designator specified by channel group k is not set (indicating unsuccessful transfer of a word to an output device), skip the next sequential instruction; otherwise, take the next instruction.

50:60 ROUND AU (RND) If (AU) positive, $(AU) + (AL)_{17} \rightarrow AL$

If (AU) negative, $(AU) - (AL)'_{17} \rightarrow AL$

Execution time: 2 microseconds

If (AU) is positive, add bit position 17 of AL to (AU); if (AU) is negative, subtract the complement of bit position 17 of AL from AU and leave the resultant rounded (AU) in AL. Ignore k. $(AU)_i = (AU)_f$.

An application of this instruction would be: a double length value in A is normalized as far as possible to the left; however, only a rounded, single-length number is required for the accuracy desired.

50:61 COMPLEMENT AL (CPAL) $(AL)' \longrightarrow AL$

Execution time: 2 microseconds

Complement (AL), leaving the result in AL; ignore k.

NOTE

This instruction affects a bit-by-bit complement with the following exception: all zeros (positive zero) will remain all zeros.

50:62 COMPLEMENT AU (CPAU) $(AU)' \longrightarrow AU$

Execution time: 2 microseconds

Complement (AU), leaving the result in AU; ignore k.

(See note: instruction 50:61.)

50:63 COMPLEMENT A (CPA) $(A)' \longrightarrow A$

Execution time: 2 microseconds

Complement (A), leaving the result in A; ignore k.

(See note: instruction 50:61.)

50:64 Not used

50:65 Not used

50:66 Not used

50:67 Not used

50:70 Not used

50:71 Not used

50:72 ENTER INDEX CONTROL REGISTER (ENTICR) $k_{2-0} \rightarrow$ ICR

Execution time: 2 microseconds

Clear the index control register. Then transmit the three, low order bits of k to the ICR.

50:73 ENTER SPECIAL REGISTER (ENTSR) $k_{4-0} \rightarrow$ SR

Execution time: 2 microseconds

Clear the special register. Then transmit the five low-order bits of k to the SR. (SR_3 = 1 activates the SR.)

50:74 Not used

50:75 Not used

50:76 Not used

50:77 Not used

SECTION 4

THEORY OF OPERATION

4-1. GENERAL.

a. SECTION CONTENT. - This section contains a logical analysis of computer operation including command timing, functional description, power distribution, power supply operation, and printed-circuit module symbology. Description of computer logic functions include references to the functional schematics contained in section 9, a logical interpretation of the operation of the circuits, reference tables, in-text illustrations, and simplified block diagrams. The information used to explain the printed-circuit module symbology is contained in section 8.

The logic analysis of the four sections of the computer, paragraphs 4-2 through 4-5, has been prepared assuming that the reader has acquainted himself with section 1, general description; and specifically, paragraph 1-3, functional description. If this is not the case, paragraph 1-3 should be read before reading paragraphs 4-2 through 4-4.

b. BLOCK DIAGRAM. - The computer block diagram, (figure 1-9) divides the computer into four functionally definable areas or sections: control, input/output (I/O), arithmetic, and memory. Each section is illustrated in a separate block diagram, and the individual blocks within these sections are described in detail in the succeeding paragraphs. Distribution of the timing pulses is not shown in the block diagrams because each block is included in this distribution.

4-2. FUNCTIONAL THEORY

a. CONTROL SECTION. - The control section, through the generation of specific sequencing and enables, allows computer operation under either manual or program control. During manual operation, circuit conditions are displayed on the front panels of the logic drawers. The conditions are controlled through the use of the pushbutton-indicator units and several control switches, which allow stepping slowly through the various functions performing an instruction. During this procedure, a study can be made of the lighted indicators to isolate possible logic malfunctions.

However, under program control, the computer performs instructions of an entire program at a high rate of speed, stopping only at programmed stops. During either manual or program control, the control section supplies timing, translation, and sequencing required for all computer functions.

The control section of the computer is divided into six logically definable blocks as shown in figure 4-1. These blocks are console control, timing circuits, translator circuits, register control, registers, and special circuits. The connecting lines show the functional relationship between the blocks, and between the control section and the remaining computer sections. The functions performed by each of these blocks are discussed in detail in the following paragraphs.

(1) CONSOLE CONTROL. - Five control circuits comprise the console control block of the computer. These five circuits are the power control panel, start/stop logic, master clear, remote control, and mode select logic. These circuits (located on figures 9-3, 9-7, 9-34, and 9-147) provide the basic control of computer operation from initial application of power to start of a computer program, and for termination of the execution of a program.

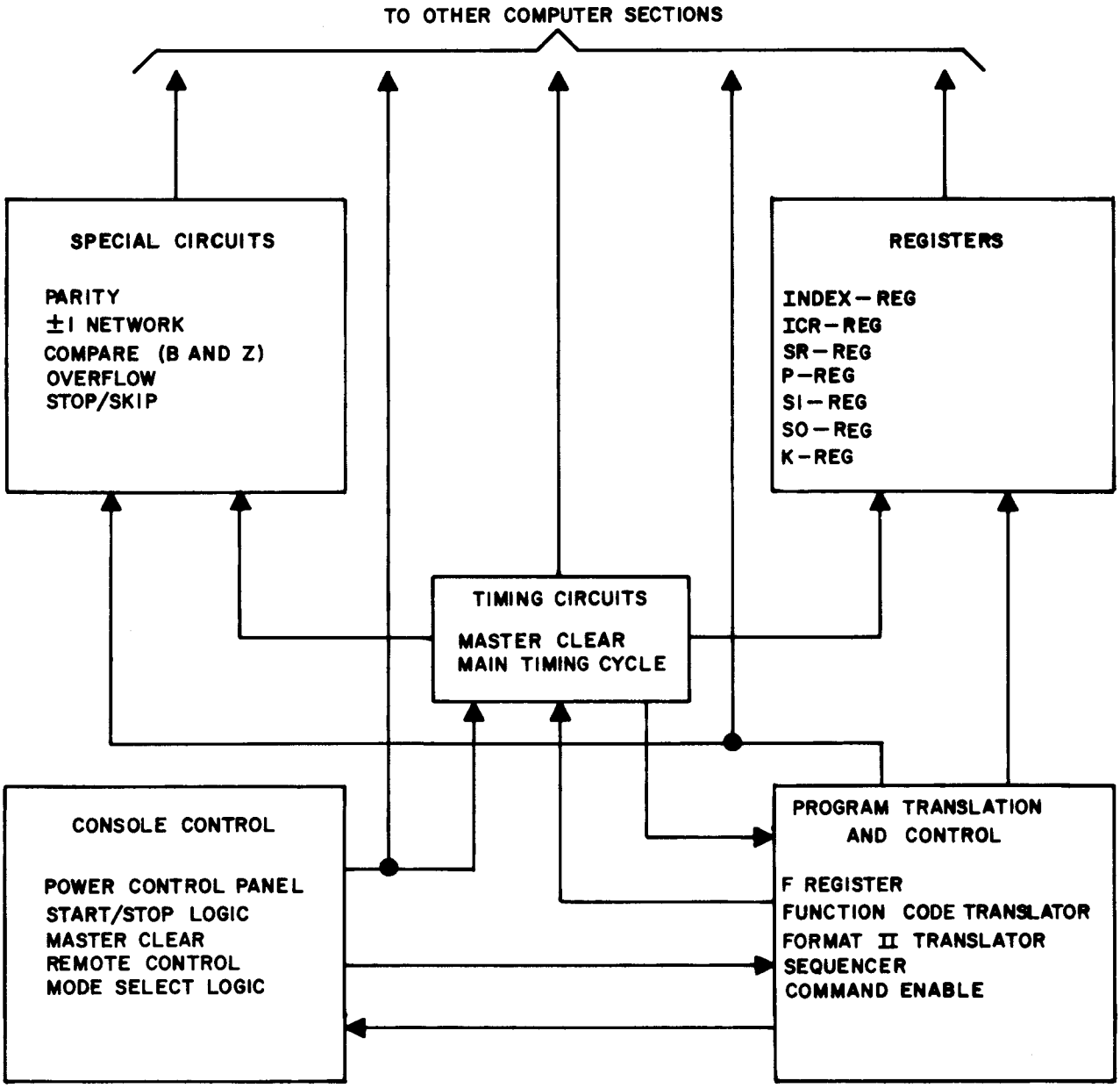


Figure 4-1. Control Section, Block Diagram

(a) POWER CONTROL PANEL. - Power control panel (figure 3-5) contains the switches and indicators used during the initial application of power, and for circuit control. The indicators provide a visual means of checking cabinet conditions and a running-time meter records total computer operating time. Circuit connections for the power control panel are shown in figure 9-176. The function of each switch, control, and indicator is listed in table 3-4.

(b) START/STOP LOGIC. Start/stop logic (figure 9-3) consists of the logic required to start the computer execution of a program, control the issuance of phase and timing pulses for the several modes of operation, and stop computer operation. The stopping function is dependent upon the switch settings listed in table 3-3 and any programmed computer stop instructions.

Start logic consists primarily of the start and run flip-flops, RESTART SPEED CONT potentiometer, and associated logic.

The computer enters the high-speed run process in one of two situations. If the RESTART/START STEP switch is placed momentarily in the START position, high-speed run occurs in all modes of operation except the phase step mode. If the switch is placed momentarily in the RESTART position, high-speed run occurs at the issuance of a pulse from the low-speed oscillator. The start flip-flop assures that only one start occurs for each operation of the switch or for each pulse from the oscillator. At initiation of the high-speed run condition, the run flip-flop is set and supplies enabling signals to various control logic circuits.

Stop logic is used to terminate computer operation by clearing the run flip-flop. In run mode, this is accomplished by programmed stops or by manually setting the SEQ STEP/STOP switch to STOP position.

In the op step mode, the run flip-flop is cleared and computer operation is stopped at termination of the I sequence during a Format I instruction providing SEQ STEP/STOP switch is in the center position. If this switch is in SEQ STEP position, the computer operation will terminate at the conclusion of each major sequence.

The RESTART SPEED CONT potentiometer controls the frequency of the low-speed oscillator and thus governs the application of pulses applied to set the start flip-flop during a restart operation.

Start/stop logic thus provides the signals that initiate computer operation in one of several modes and terminate this operation by either programmed stops or manual intervention through the SEQ STEP/STOP switch.

(c) MASTER CLEAR. - Master clear circuitry allows the operator to clear either certain selected flip-flops or all of the primary flip-flops in the computer. This option is provided by the three-position, spring-loaded I/O CLEAR/MASTER CLEAR switch (figure 9-7).

Placing the switch momentarily in the I/O CLEAR position clears the channel and function priority flip-flops (figures 9-65 and 9-66), the I/O translator circuits (figure 9-51), the EF/OD active flip-flops (figures 9-61 through 9-64), and the C register (figures 9-71 and 9-72). The resume flip-flop (figure 9-69) and request flip-flops (figures 9-61 through 9-64) are set.

Placing the switch momentarily in the MASTER CLEAR position when the computer is not in a run or phase step condition, clears all sections, registers, and control flip-flops in the control computer. If in a run condition, only the voltage fault and/or program fault flip-flops (figure 9-121) and the memory protection flip-flops (figure 9-134) are cleared.

The master clear signals are distributed to the logic circuitry through the gating circuits (figure 9-7).

(d) REMOTE CONTROL. - Control of computer operation can be maintained from a remote position through the use of the remote console (figure 1-6) supplied as a customer-selected option. Logic circuitry for operation of the remote console is provided within the standard computer and is shown in figures 9-3, 9-7, 9-31, 9-32, and 9-121.

Switches, controls, and indicators on the remote console duplicate the operating controls of the central computer. An interconnecting cable between the computer and the remote console is supplied with this option and limits the distance between the two units to a maximum of 300 feet.

(e) MODE SELECT. - The computer performs logic functions in one of four possible modes of operation. These four modes are run, phase step, op step (operation step), and load. The mode of operation must be manually selected on control panel 1 (A2) (figure 4-2) by pressing the specific pushbutton indicator corresponding to that mode. Because of the interconnecting logic circuitry, only one mode at a time can be selected.

Logically, mode selection is made by mode selection circuitry (figure 9-3). Pressing the desired pushbutton indicator supplies an enable for the selected mode and disables the three remaining modes. Enabling a given mode initiates sequencing the computer for that mode through generation of command outputs; that is, L $\Longrightarrow$ PROGRAM RUN, H $\Longrightarrow$ OP STEP, H $\Longrightarrow$ PHASE STEP, L $\Longrightarrow$ LOAD MODE. A simplified mode select circuit is shown in figure 4-3.

1. RUN MODE. - Run mode is the normal high-speed operating mode of the computer. All operations not pertaining to malfunction isolation and program debugging are performed in run mode. Although initial program loading is performed in the load mode, the computer reverts to run mode after approximately 2 microseconds of operation.

2. PHASE STEP MODE. - Phase step mode provides normal computer operation, including the memory circuitry, at a controlled rate of speed. Used primarily for logic malfunction isolation, phase step mode may be executed either by manually issuing each successive phase of the master clock through the START STEP position of the RESTART/START STEP switch, or by using the RESTART position of the switch and the low-speed oscillator. The RESTART SPEED CONT potentiometer controls speed of computer operation in the phase step mode. By placing the PHASE REPEAT switch in the up position and selecting a desired phase, the computer repeatedly issues the chosen pulse at a high rate of speed. If all four phases are selected, a cycle-step operation results.

3. OP STEP MODE. - In the op step mode, the computer operates at a high rate of speed but its operation is stopped at selected intervals throughout the performance of a program and must be manually restarted. During this mode, the operator examines the contents of the various registers for accuracy at specific times throughout the execution of a program. If a malfunction is detected, the operator can determine, from register content, the approximate point in the program at which the error occurred. Each operation of the RESTART/START STEP switch steps the computer through an instruction. If the SEQ STEP/STOP switch is off, the computer stops after the I sequence of each Format I instruction. If the switch is on, the computer stops after each major sequence of an instruction.

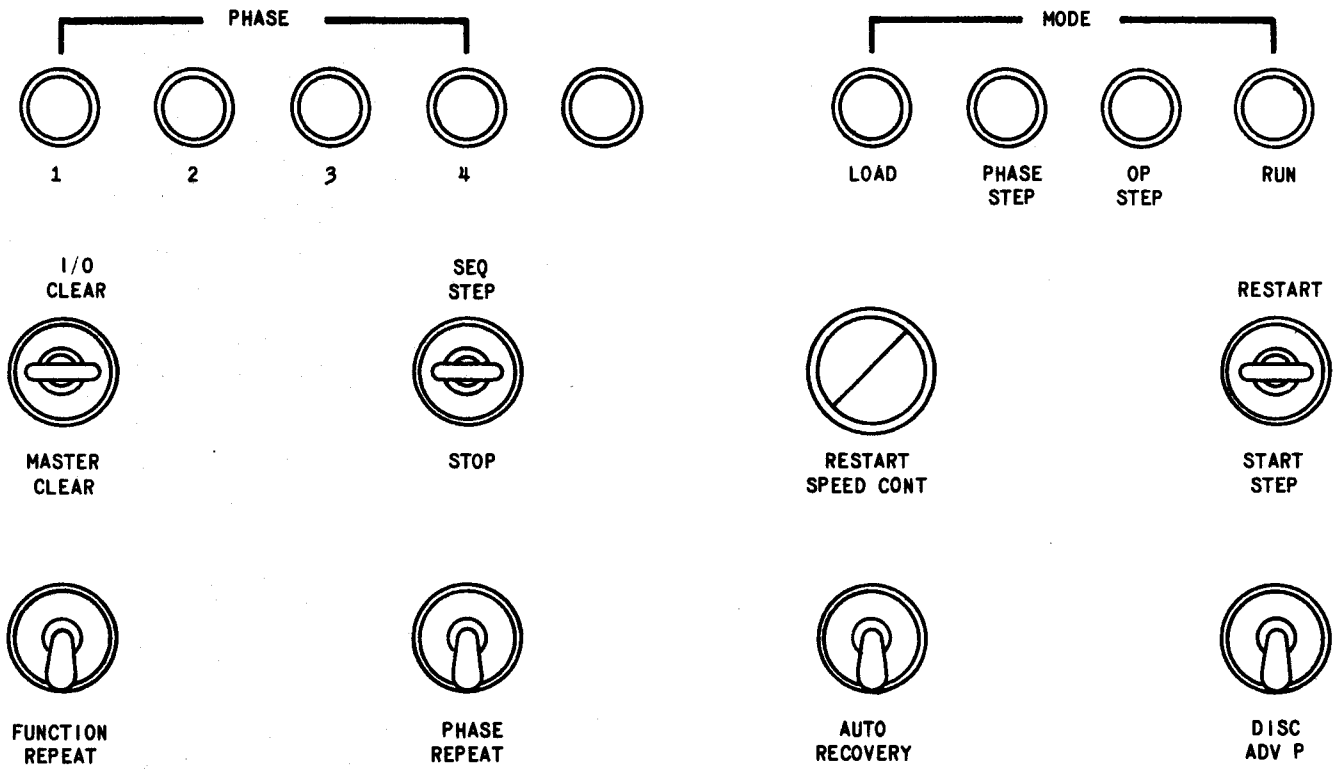


Figure 4-2. Operating Controls, Control Panel 1 (A2)

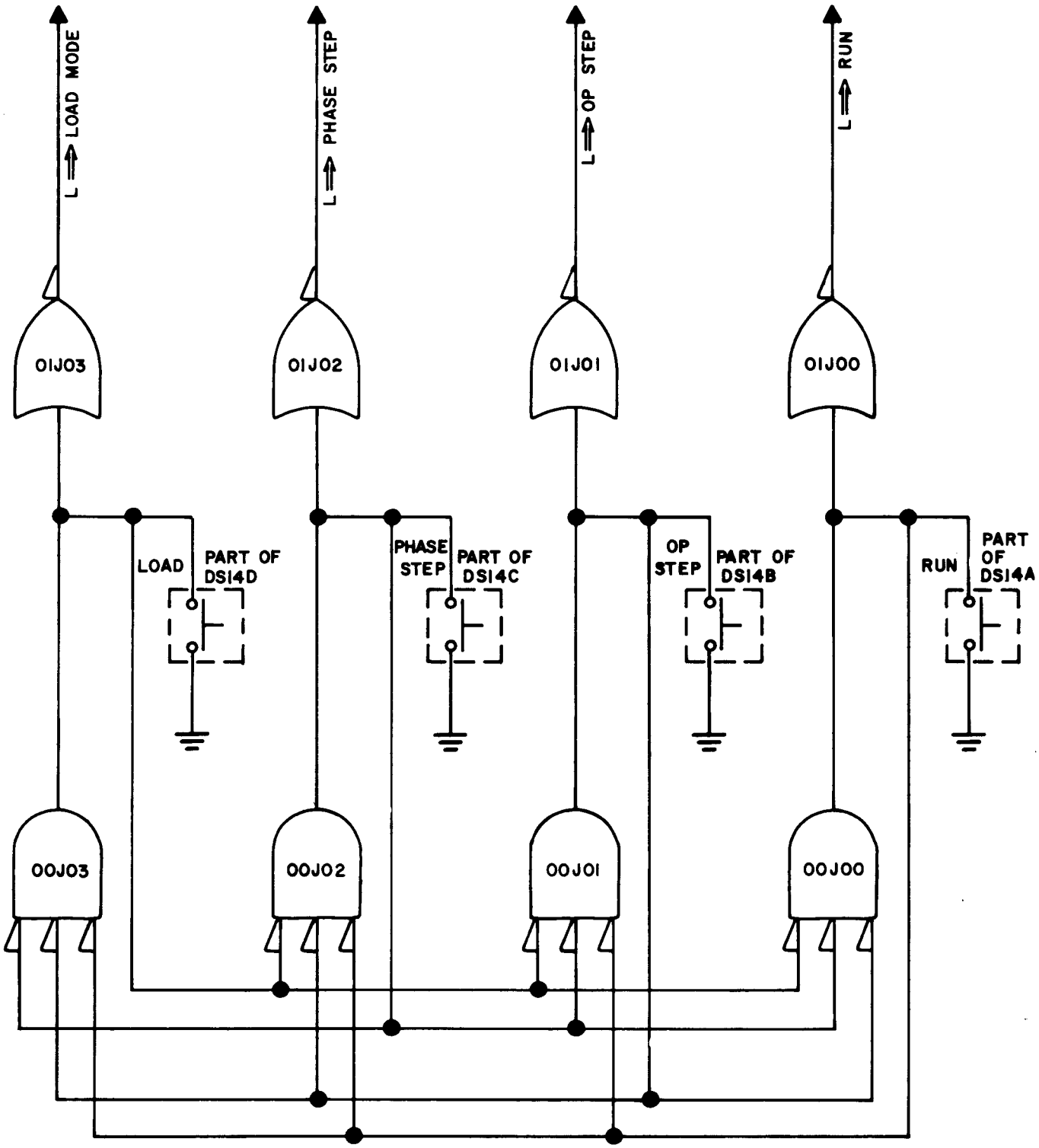


Figure 4-3. Typical Mode Selection Circuit, Simplified Diagram

4. LOAD MODE. - Load mode forces the computer logic to address the first instruction of the wired memory program at address 500_8. The computer performs at the high-speed rate and after the memory referencing has occurred, it performs in the normal run mode.

The switches and their functions are listed in table 4-1. Also included in this table are the positions of other control switches associated with computer functions.

TABLE 4-1. CONTROL SETTINGS AND FUNCTIONS

CONTROL PANEL SWITCHES					OPERATION
RESTART/ START STEP	SEQ STEP/ STOP	AUTO RECOVERY	PHASE REPEAT	FUNCTION REPEAT	
Settings With RUN Mode Indicator Lighted					
START STEP	Neutral	Down	Down	Down	Normal computer high-speed run.
START STEP	Neutral	Up	Down	Down	Normal high-speed run with bootstrap memory.
START STEP	Neutral	Down	Down	Up	Repeat instruction contained in F register for each momentary operation of RESTART/START STEP switch.
Neutral	STOP	Down	Down	Down	Stop computer high-speed operation after the execution of the I sequence of the next Format I instruction.
RESTART	Neutral	Down	Down	Down	Restart computer operation after a stop instruction or operation of the SEQ STEP/STOP switch.
Settings With PHASE STEP Mode Indicator Lighted					
START STEP	Neutral	Down	Down	Down	Send indicated phase pulse to computer logic, advance phase generator, and stop.
RESTART	Neutral	Down	Down	Down	Send next sequential phase pulse, as indicated, to computer logic and stop.
START STEP	Neutral	Down	Up	Down	Send a continuous pulse of phase indicated to computer logic at normal high-speed rate.
Settings With OP STEP Mode Indicator Lighted					
START STEP	Neutral	Down	Down	Down	Stop computer operation after execution of I sequence of each Format I instruction.
RESTART	Neutral	Down	Down	Down	Restart computer operation after above listed stop.

TABLE 4-1. CONTROL SETTINGS AND FUNCTIONS (CONT.)

CONTROL PANEL SWITCHES					OPERATION
RESTART/ START STEP	SEQ STEP/ STOP	AUTO RECOVERY	PHASE REPEAT	FUNCTION REPEAT	
Settings With OP STEP Mode Indicator Lighted (Cont.)					
START STEP	SEQ STEP	Down	Down	Down	Stop computer operation after each major sequence.
RESTART	SEQ STEP	Down	Down	Down	Restart computer operation after above listed stop.
Settings With LOAD Mode Indicator Lighted					
START STEP	Neutral	Down	Down	Down	Jump to address 00500. Clear Load Mode. Execute bootstrap program and subsequent programs in run mode.

(2) TIMING CIRCUITS. - Timing within the computer is initially provided by a master clock circuit. An additional clock circuit is used to govern functions of the main core memory and utilizes basic timing of the master clock.

Master clock, clock distribution, timing chains, and phase step logic are included in the timing circuitry.

(a) MASTER CLOCK. - The master clock, (figure 9-4) generates and distributes four clock pulses every 500 nanoseconds. The time duration of each clock pulse is approximately 120 nanoseconds. These four pulses, identified as phases 1, 2, 3, and 4, comprise one clock cycle. Four clock cycles comprise one computer cycle.

The relationship between the phases, clock cycles, and computer cycle is illustrated in figure 4-4. This illustration also includes the relationship of timing chain outputs to the master clock output.

The clock-generating circuit consists of a delay line, two phase generators, two phase flip-flops; and gates and inverters, which produce the proper enables. A simplified logic diagram of the master clock is shown in figure 4-5. The time relationship between various outputs and clock pulses is shown in figure 4-6. When not in use, all outputs of the delay line are 0.0 volt.

Applying an external enable to the clock-input inverter initiates the propagation of a -4.5-volt signal through the delay line circuit. After approximately 15 nanoseconds, this signal reaches pin eight of the delay line and is sent to gate EF 02. 125 nanoseconds after being applied to the delay-line chain, the signal reaches pin six and appears as a -4.5-volt signal at the input inverter. This signal disables the input inverter and a 0.0-volt signal is propagated through the delay-line. 120 nanoseconds later, the input inverter is re-enabled and the process is repeated. The application of delay-line output signals to the gating circuits and phase generators produces outputs shown in figure 4-6.

NOTE

Output pin numbers from the master clock delay lines may vary in individual computers because of inherent delays in logic modules.

In NARROW position, CLOCK NARROW-NORMAL switches allow the master clock circuit to generate pulses of a shorter time duration for marginal check procedures listed in section 5. Under ordinary operation, the switches will be in the NORMAL position.

(b) CLOCK DISTRIBUTION. - Clock distribution circuits (figures 9-5 and 9-6) supply the logic driving elements used to propagate clock phase pulses 1 through 4 throughout the computer. Each phase is applied through several non-inverting drivers to the associated computer logic. Figure 9-5 depicts this distribution to chassis three and four, located physically in drawer A2. Figure 9-6 depicts the distribution to the I/O chassis, and to chassis seven and eight. The I/O chassis are located in drawer A1, and, with the 12- or 16-I/O channel option, drawer A8. Chassis seven and eight are located in drawer A4.

Clock pulse distribution to the memory drawer A3 (and A9 with the 65K memory option) is shown in figure 9-6 where phases 1, 3, and 4 are routed to the main memory timing circuit on figure 9-122. Further memory timing is supplied from the main memory timing logic.

(c) TIMING CHAINS. - The computer contains two timing chains; the main timing chain (figures 9-8 through 9-11) and an auxiliary timing chain (figure 9-36). These timing chains are used to gate specific clock pulses in the generation of command sequence enables for execution of programmed instructions. Timing chains consist of flip-flops connected to produce sequential timing pulses when activated by the master clock.

Main timing chain outputs are shown in figure 4-4 which includes the relationship of these outputs to clock pulses. The auxiliary timing chain in figure 9-36 is discussed in paragraph 4-2b.

(d) PHASE STEP LOGIC. - Phase step logic (figures 9-3 and 9-4) enables the operator to apply either single sequential-phase pulses or a continual single-phase pulse to the remaining computer logic. Phase step logic is intended for use only during maintenance procedures, and assists in locating computer malfunctions and program errors.

For the application of single sequential-phase pulses, the PHASE REPEAT switch, located on control panel 1 (A2) and shown in figure 4-2, must be in the off (down) position. Prior to selection of the phase step mode of operation, one of the four phases must be selected as the initial applied phase. The phase is selected by pressing the appropriate PHASE pushbutton indicator on control panel 1. Pressing this indicator sets the associated lower-rank phase flip-flop in figure 9-4 and enables the corresponding upper-rank phase flip-flop. The upper-rank flip-flop is set with the pulse generated by pressing the RESTART/START STEP switch. If all four phase indicators are pressed, cycle-step operation is enabled.

To select the phase step mode, press the PHASE STEP pushbutton indicator. This disables the continuous application of the clock pulses through the circuitry on figure 9-3. Each operation of the RESTART/START STEP switch enables the next sequential clock pulse flip-flop to be set.

Placing the PHASE REPEAT switch in the on (up) position enables a single clock pulse of the selected phase to be continuously applied to the computer logic at the normal high-speed rate.

The phase step logic supplies an invaluable aid to maintenance and programming personnel by allowing the application of single phase or clock pulses and visually displaying the resulting computer operation performed by that pulse.

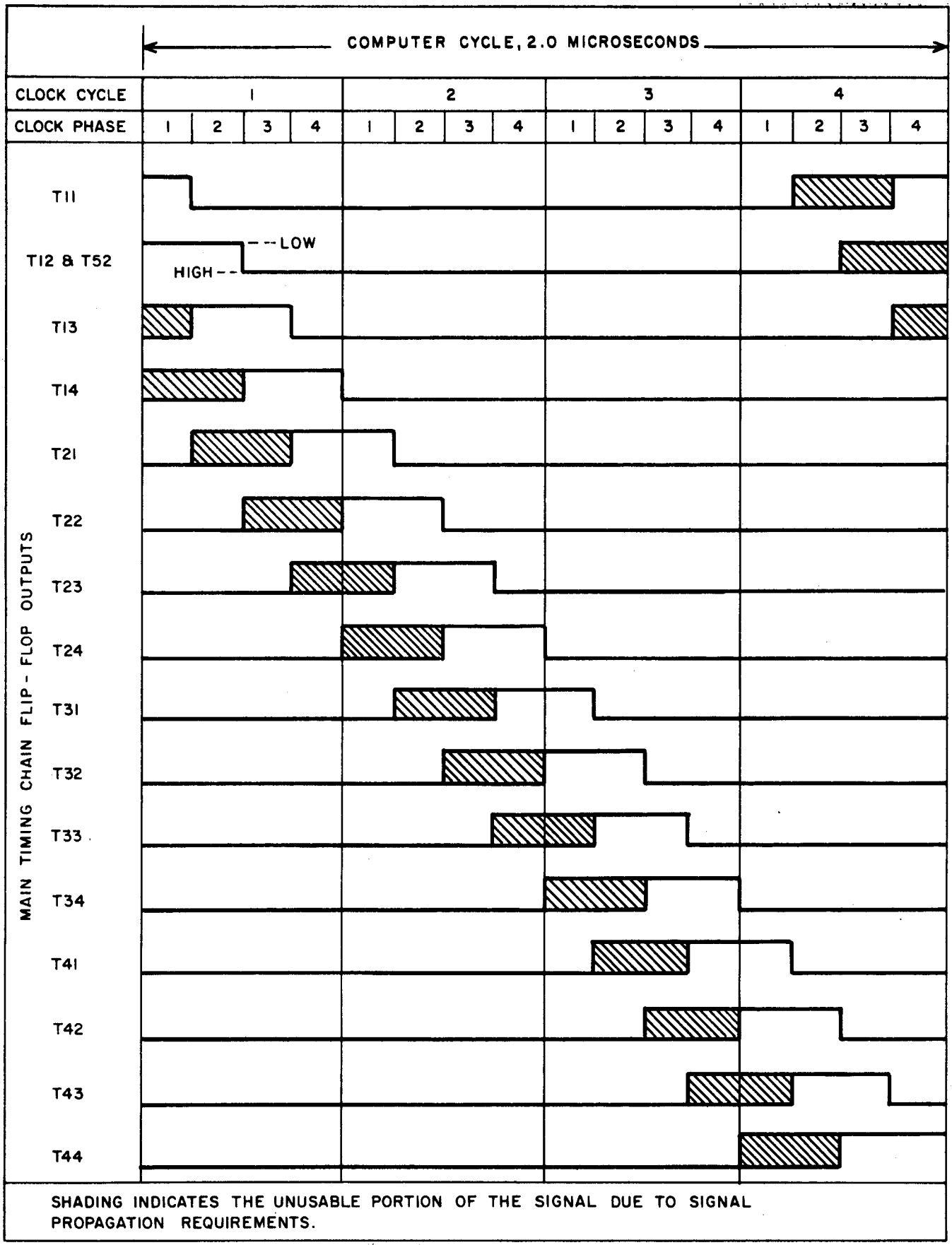


Figure 4-4. Main Timing Cycle Outputs

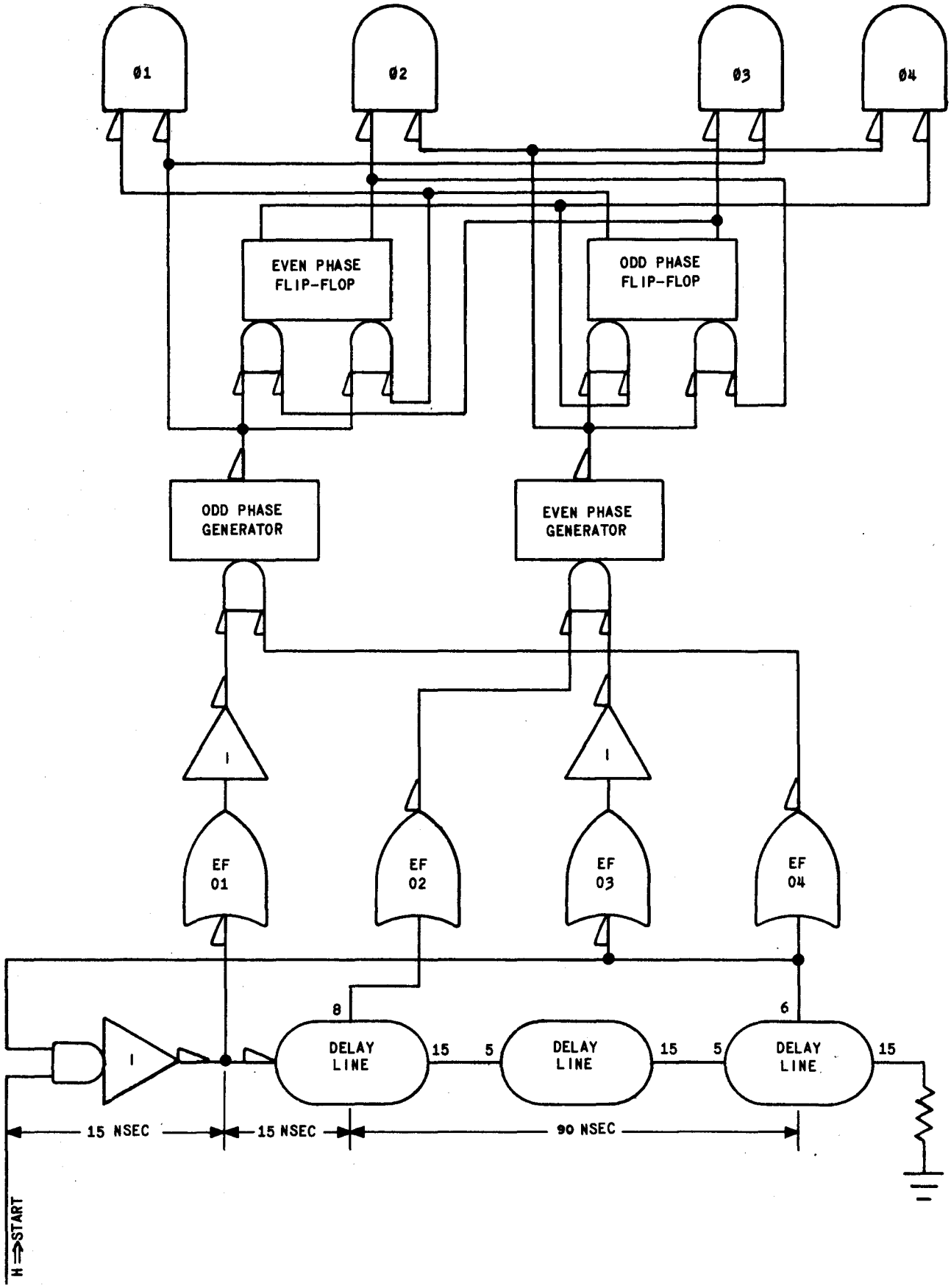


Figure 4-5. Master Clock Logic, Simplified Diagram

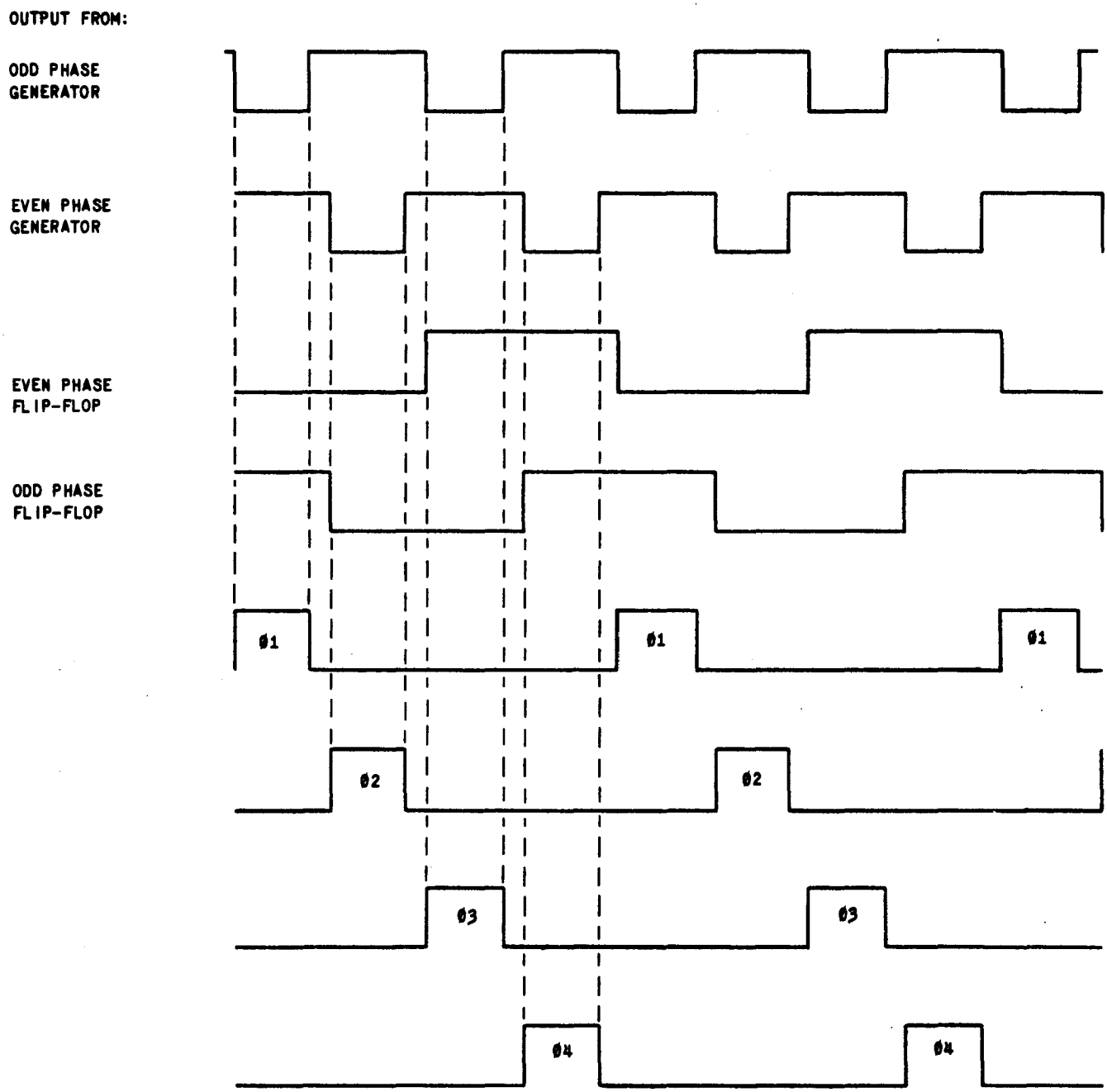


Figure 4-6. Master Clock Output Signals

(3) TRANSLATOR CIRCUITS. - The translator circuits decode the programmed instruction, designate from this information the sequences to be performed to accomplish the instruction, and provide the required outputs to enable execution of the designated operations. A typical translator circuit is shown in figure 4-8.

The translation circuitry includes function code (F) register, function code subtranslators, function translators, sequence designators, and sequence output circuits. These translation circuits are shown in figures 9-12 through 9-16, 9-35, 9-36, and 9-40 through 9-48.

(a) F REGISTER. - The F register (figure 9-40) stores the f portion of the instruction to be executed. Input to the F register is transferred from the Z select circuit. The bits to be transferred depend upon the contents of the Z select circuit and are translated into either Format II or Format I enables.

1. FORMAT II. - If bit 15 and bit 17 of the Z select circuit contain a one, and bits 12, 13, 14, and 16 contain zeros, the output from 16F50 (figure 9-40) enables setting OXF06 to indicate a Format II instruction. Bits 06 through 11 are then gated into the F register to be translated into the minor function code.

2. FORMAT I. - If the input translation circuit does not detect a Format II instruction, bits 12 through 17 of the Z select circuit are gated into the programmed instruction.

Output from the F register is routed to the function code translator circuits (figures 9-41 through 9-48) to be used for sequencing and control of computer logic.

By placing the FUNCTION REPEAT switch in the up position, both the clear enable and transfer enable of the F register are removed and the instruction contained in the F register is repeated continuously until manual intervention stops the computer or a fault condition occurs.

(b) FUNCTION CODE SUBTRANSLATORS. - Function code subtranslators (figures 9-41, 9-42, and 9-43) receive input from the F register and translate this data into the proper numeric value for sequencing the computer logic.

1. SUBTRANSLATOR 1. - Subtranslator 1 (figure 9-41) interprets the input to provide a general numeric value of the instruction, such as from 00 through 07, 10 through 17, or 00 through 47, odd. Output from this circuit is then used to enable further translation of the function code.

2. SUBTRANSLATOR 2. - Subtranslator 2 (figure 9-42) translates for the low-order octal numeral of the function code, that is, f - X0 or f - X2, X3. This output also is used to enable further function code translation.

3. SUBTRANSLATOR 3. - Subtranslator 3 (figure 9-43) identifies the low-order digit as being either even, as 0, 2, 4, or 6; or odd, as 1, 3, 5, or 7. It also supplies the Format I and Format II enables to allow further translation of the function code.

(c) FUNCTION TRANSLATORS. - The function translators (figures 9-44 through 9-48) comprise a network of AND, OR, and AND/OR gates and inverters which translate the contents of the F register into one of the octal function codes listed in section 1, table 1-4. Each of the function codes corresponds to one of the instructions, which may be programmed for execution by the computer.

The computer instructions are divided into two categories; Format I and Format II. Format I instructions are identified by a two-digit octal designator (00 through 47 and 51 through 77). Format II instructions are identified by a four-digit octal designator of which the first two digits are 50, indicating the major function code, followed by the second two digits (00 through 77) indicating the minor function code. The relationship between the F register and translation circuitry is shown in block form in figure 4-7; figure 4-8 shows a typical translation circuit.

(d) SEQUENCE DESIGNATORS. - Translation of the programmed instruction provides the information necessary to sequence computer operation. As shown in table 1-5, several major command sequences are available for manipulating data during the execution of an instruction. Although ten major command sequences and several minor subsequences exist, several instructions require only a single sequence for completion; others may require many of the sequences before final logic operation is completed. The selection of the required sequences and the order of their performance is determined by the translation data applied to the sequence designator circuitry (figures 9-12 and 9-13).

1. UPPER-RANK SEQUENCE DESIGNATOR. - The upper-rank sequence designator (figure 9-12) contains a series of flip-flops, each set to initiate a unique sequence of events within computer logic.

For example, one of several conditions required to initiate a W (write) sequence is if the function code is 40 through 47, Format I, and the present operation is an I sequence. The W flip-flop, G23, then is set by the proper clock phase and the W sequence is initiated. Each sequence flip-flop requires certain preceding sequence conditions, proper function code translations, and correct clock phase pulses for setting and initiating the associated sequence.

Outputs from the upper-rank sequence designator are routed to sequence output circuits which, when gated with the proper clock pulses, produce the computer logic sequencing.

For a detailed order of events occurring during a given instruction, see paragraph 4-7, command timing.

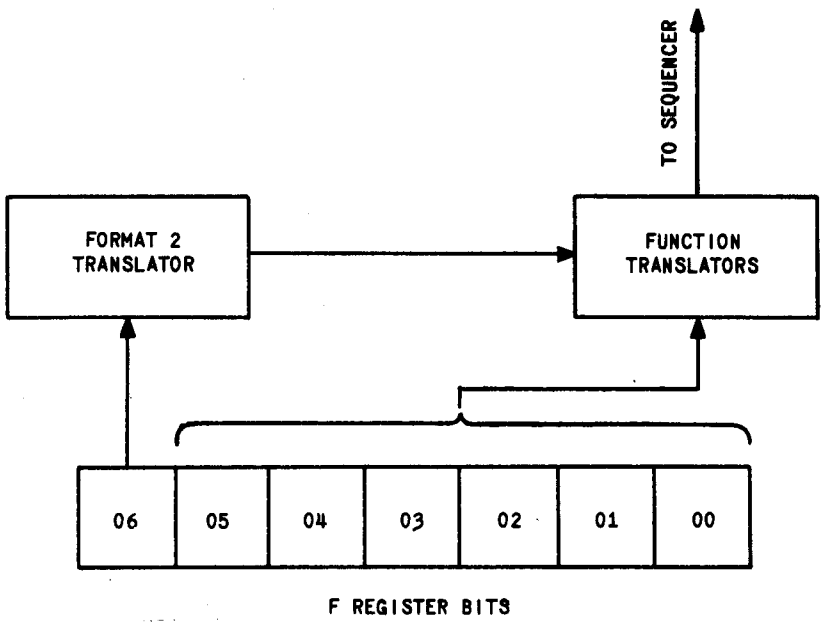


Figure 4-7. Relationship Between F Register and Translation Circuitry

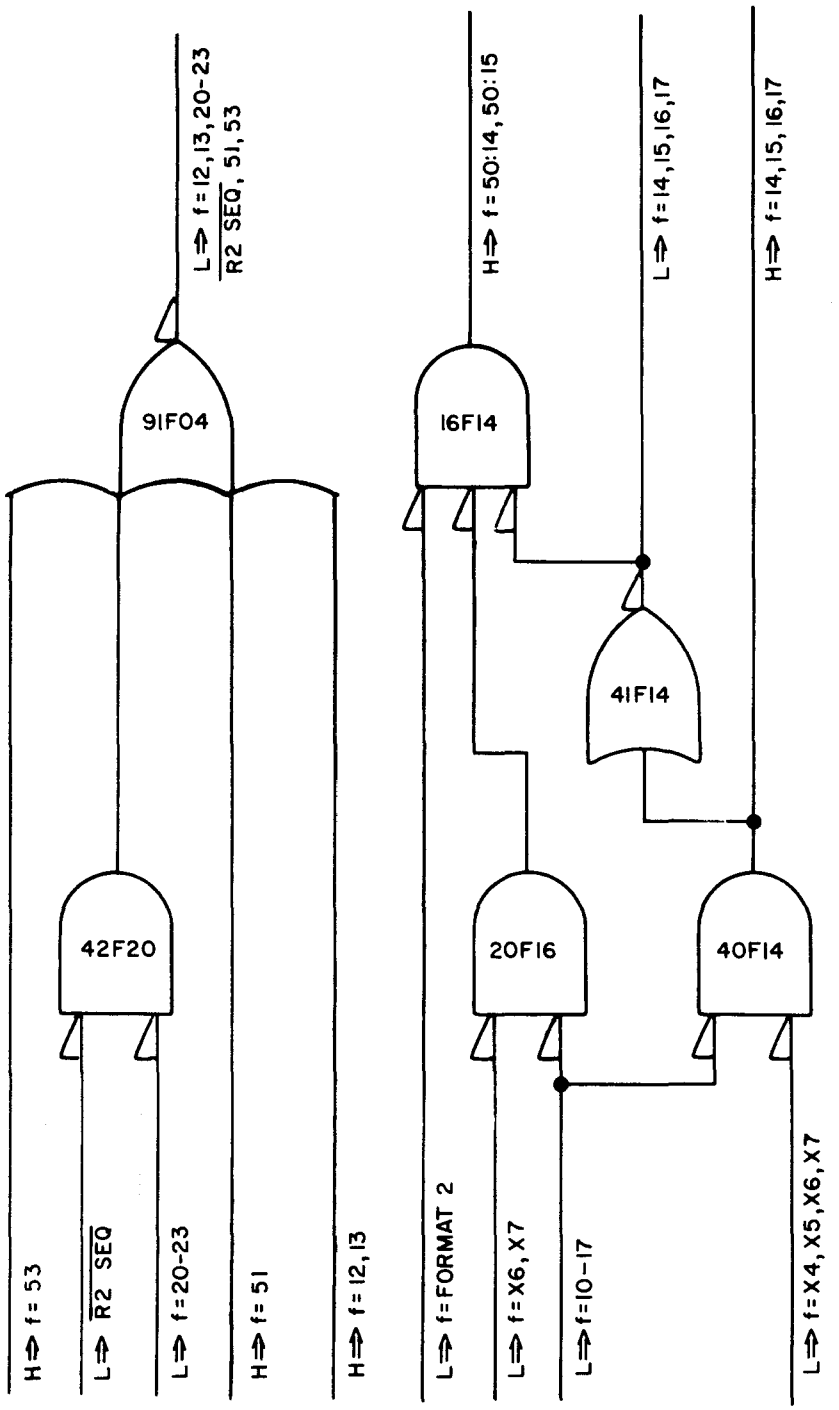


Figure 4-8. Typical Translation Circuit, Simplified Logic Diagram

2. LOWER-RANK SEQUENCE DESIGNATOR. - The lower-rank sequence designator (figure 9-13) is composed of several sequencing flip-flops and associated set and clear circuitry. Each flip-flop has, as one of its set conditions, an input from an associated flip-flop in the upper rank shown in figure 9-12. Output signals from the lower rank are then applied as enables to set the flip-flop in the upper rank, which designates the next series of operations.

(e) SEQUENCER. - The sequencer influences the main timing chain to ensure the proper execution of a programmed instruction. Individual main command sequences are selected in the proper order and gated with the main timing chain outputs to selectively gate timing pulses. Thus, only operations of the selected command sequence are performed.

Sequencer outputs are functionally segregated for ease of reference. The categories, as listed in table 1-5, are principally I/O, I, Interrupt, and R/W. Some of these have been divided into two parts to indicate either the first or second half of a 36-bit word operation.

Two minor command sequences are the multiply, divide, shift, and scale sequence; and the advance P subsequence. Each are initiated under the influence of the appropriate major sequence and operate independently from major sequence enables.

1. I/O SEQUENCE OUTPUTS. - The I/O sequence outputs (figure 9-14) provide command timing enables for the performance of I/O functions. The outputs are generated by the gating of several control signals, and are identified, as to their function by the signal description term.

2. I1, I2, and INTERRUPT SEQUENCE OUTPUTS. - The I1, I2, and interrupt sequence outputs (figure 9-15) provide the sequencing enables used during the identified sequence.

3. R/W SEQUENCE OUTPUTS. - R/W sequence outputs (figure 9-16) enable reading from memory or writing into memory and are required during the involvement of the computer memory in the execution of an instruction.

4. MULTIPLY, DIVIDE, SHIFT and SCALE SEQUENCE. - Shift logic (figure 9-36) is used during the execution of either a multiply, divide, shift, or scale factor instruction. The circuit contains a secondary timing chain which is dependent upon the master clock pulse output and produces command enables to perform the programmed instruction.

The scale factor flip-flop is set only during a 50:44 instruction and remains cleared during all other instructions.

Flip-flops 0XL00 through 0XL04 produce command enables during multiply, divide, and shift instructions. Flip-flops 0XL05 and 0XL06 are used only if one or the other of the operands is negative, indicated by an enable from 20G30.

The logic function of this circuit and its association with related circuitry is explained in the paragraph containing arithmetic processes.

5. ADVANCE P SUBSEQUENCE. - Advance P subsequence logic contains the circuitry required to increment or decrement the contents of the P register during execution of sequential instructions.

If a resume fault is detected by the computer logic while performing a force instruction, the contents of the P register are decremented.

During an I/O sequence, if an 18-bit word is sent under force to an interconnected computer and a resume is not received within an allotted period of time, a resume fault results. Immediately after this 18-bit word is forced, the contents of the P register are incremented by one. To repeat this instruction, the contents of the P register are decremented and the same 18-bit word is sent. The instruction is repeated until a resume signal is received from the associated computer. For this purpose, the decrement P flip-flop produces the H⟹DECREMENT P enable.

For a 30, 31, 57, or 76 instruction, the increment P flip-flop is set at Ø3.1 of the W sequence. During a 56 instruction, this flip-flop is set at Ø3.1 of the R1 sequence. For all other instructions, the flip-flop is set at Ø1.1 of the I sequence. The H⟹ADVANCE P enable is produced on the Ø3, following the setting of the increment P flip-flop.

The L⟹ADVANCE P enable clears the D register, transfers the contents of the P register to the D register, and sets the inhibit EAB flip-flop for incrementing P.

(4) REGISTER CONTROL. - The register control circuitry is composed of several control circuits used to generate transfer, clear, and gating enables for the control, arithmetic, and memory section registers. Control signals are also generated for several circuits not called registers, such as the adder, store select, and arithmetic selector.

(a) A REGISTER CONTROL. - A register control circuit (figure 9-20) provides enables required by the AU and AL registers to effect transfer of information either into, or from, these temporary storage locations. These enables are produced by gating function code translation, sequence commands, timing signals, and other selective signals in the necessary combinations. Resulting enables and their functions are listed below.

L ⟶ X ⟶ AU	Enables transfer of the contents of the X register to the AU register.
L ⟶ ADDER ⟶ AU	Enables transfer of the contents of the adder to the AU register and supplies one of the enables for setting the overflow flip-flop if this condition occurs.
H ⟶ CLEAR AU and H ⟶ CLEAR AL	Clears the contents of the designated register to contain all zeros.
L ⟹ ADDER ⟶ AL	Enables transfer of the contents of the adder to the AL register.
L ⟹ W ⟶ AL	Enables transfer of the contents of the W register to the AL register.

Both AU and AL registers may be cleared manually through the use of the CLEAR AU or AL switches located on the front panel of drawer A2.

(b) D REGISTER CONTROL. - D register control circuit (figure 9-18) functions to provide transfer and clear enables (generated from function code translation, sequencing commands, and timing pulses) to the D register.

Inputs to the D register control are provided from function code translation circuits to enable D register use during execution of specific instructions. Sequencing inputs enable use of the D register during execution of specific command sequences. Timing inputs provide the basic phasing of a D register operation. The D register control outputs and their functions are listed on the following page.

L ⟹ CLEAR D	Enables setting the contents of the D register to zero.
L ⟹ SELECT ⟶ D	Enables transfer of the contents of the arithmetic selector to the D register.
L ⟹ $\overline{\text{SELECT}}$ ⟶ D	Enables transfer of the complement of the contents of the arithmetic selector to the D register.
L ⟹ SET DU	Enables setting the upper six bits of the D register when executing certain instructions providing the lower 12 bits of the D register represent a negative number.
H ⟹ SET DU6	Applied in conjunction with the SET DU and the SR + SET ⟶ D signals.
L ⟹ SR + SET ⟶ D	Enables transfer of the contents of bits 0, 1, 2, and 4 of the SR register to bits 12 through 15 of the D register.
L ⟹ PU ⟶ DU	Enables transfer of the upper four bits of the P register to bits 12 through 15 of the D register.
H ⟹ ADVANCE P	Enables clearing the X and W registers prior to incrementing the contents of the P register.
L ⟹ PL ⟶ DL	Enables transfer of the lower 12 bits of the P register to the lower 12 bits of the D register.
L ⟹ SET INHIBIT EAB	Enables setting the inhibit EAB flip-flop, thus preventing an end-around-borrow during skip instructions and advancing the P register.

(c) P and B REGISTER CONTROL. - The P and B register control circuit (figure 9-21) supplies, through gating, transfer and clear enables for the P and B registers. The B register is represented on the block diagram of figure 9-2 as the BU register to distinguish it from the index registers, which are often referred to as B registers.

The enables (produced from function code translation, sequencing commands, and timing pulses) and their functions are listed below.

H ⟹ CLEAR P	Enables setting the contents of the P register to zero.
L ⟹ ADDER ⟶ P	Enables transfer of the contents of the lower 15 bits of the adder to the P register.
L ⟹ SI ⟶ P	Enables transfer of the contents of the SI register to the P register.
H ⟹ CLEAR B	Enables setting the contents of the B register to zero.
L ⟹ ZO ⟶ B	Enables transfer of the contents of the ZO register to the B register.
L ⟹ INPUT ⟶ B	Enables transfer of the 18 bit data word from a peripheral device to the B register.

(d) X and W REGISTER CONTROL. - The X and W register control circuit (figure 9-19) contains the logic which produces signals for clearing and transferring control of X and W registers. These signals are a resultant product of gating function code translation, sequencing commands, and timing pulses. Output signals and their functions are listed below:

L ⟹ CLEAR X or L ⟹ CLEAR W	Enables clearing the contents of the X or W register to zero.

L ⟹ SELECT ⟶ X	Enables transfer of the contents of the arithmetic selector to the X register.
L ⟹ $\overline{\text{SELECT}}$ ⟶ X	Enables transfer of the complement of the contents of the arithmetic selector to the X register.
L ⟹ AURI ⟶ X	*Enables transfer of bits 01 through 17 of the AU register to bits 00 through 16 of the X register.
L ⟹ ALRI ⟶ W	*Enables transfer of bits 01 through 17 of the AL register to bits 00 through 16 of the W register.
L ⟹ ALRI ⟶ X	*Enables transfer of bits 00 through 16 of the AU register to bits 01 through 17 of the X register; and bit 17 of the AU register to bit 00 of the X register.
L ⟹ ALLI ⟶ W	*Enables transfer of bits 00 through 16 of the AL register to bits 01 through 17 of the W register; and bit 17 of the AL register to bit 00 of the W register.

* These transfers are executed during single-register shift instructions. When A register shift instructions are executed, bit positions may vary. See paragraph 4-2a(4)(a), A register operation, for these instructions.

(e) ICR and SR CONTROL. - The ICR and SR control circuit (figure 9-38) contains the logic used to generate clear and transfer enables for the ICR and SR registers. These enables are the product of gating function code translation, sequencing commands, and timing signals. Circuit output signals and their functions are listed as follows:

H ⟹ CLEAR ICR	Enables clearing the contents of the ICR register to zero.
L ⟹ K00-K02 ⟶ ICR	Enables transfer of the contents of bits 00-02 of the K register to the ICR register.
H ⟹ CLEAR SR	Enables clearing the contents of the SR register to zero.
L ⟹ K00-K04 ⟶ SR	Enables transfer of the contents of bits 00-04 of the K register to the SR register.

These transfer and clear enables are generated during execution of f = 50:72, 50:73, and 75, as required by the instruction contents.

(f) S_1 REGISTER CONTROL. - The S_1 register control circuit (figure 9-22) supplies clear and transfer enables for entering information into the S_1 register for memory addressing. These enables are the resultant product of gating function code translation, sequence commands, I/O translations, and, timing pulses and control memory locations used during execution of an instruction. These enables and their functions are listed below:

L ⟹ CLEAR S_1	Enables clearing the contents of the S_1 register to zero.
L ⟹ TRANSLATOR ⟶ S_1	Enables transfer of translated interrupt signals to the S_1 register bits.
L ⟹ P ⟶ S_1	Enables transfer of the contents of the P register to the S_1 register.

L ⟹ ADDER ⟶ S_1	Enables transfer of the contents of the adder to the S_1 register.
L ⟹ SPECIAL INTERRUPT REQ ⟶ S_1	Enables transfer of the contents of the special interrupt translator to bits 01, 02, and 03 of the S_1 register.
L ⟹ B ⟶ S_1	Enables transfer of the contents of the B register to the S_1 register.
L ⟹ SET S_1 = 100	Enables setting S_1 register bit 06 to 1.
L ⟹ SET S_1 = 400	Enables setting S_1 register bit 08 to 1.
L ⟹ SET S_1 BIT 2^0	Enables setting the low-order bit of the S_1 register to 1.

(g) Z_1 REGISTER CONTROL. - The Z_1 register control circuit (figure 9-23) provides clear and transfer enables associated with the Z_1 register. These enables are a product of function code translation, sequencing commands, and timing pulses. The transfer enables govern the storage of information in the Z_1 register or preparatory transfer of data for eventual storage in the Z_1 register.

The clear and transfer enables and their functions are listed below:

L ⟹ MEMORY ⟶ Z_1	Enables transfer of the contents of a memory address, placed in the memory Z register, to the Z_1 register.
L ⟹ STORE SELECT ⟶ Z_1	Enables transfer of the contents of the store select circuit to the Z_1 register for eventual storage in memory.
L ⟹ ADDER ⟶ Z_1	Enables transfer of the contents of the adder to the Z_1 register for storage in memory.
H ⟹ Z1 ⟶ Z0	Enables transfer of the contents of the Z_1 register to the Z_0 register for storage in control memory.
L ⟹ XFER	Enables transfer of the contents of the control memory to the Z_0 register.

(h) SO REGISTER CONTROL. - The S_0 register control circuit (figure 9-24) generates and supplies clear and transfer enables for the S_0 register. Control and bootstrap memory addresses, to be used during execution of an instruction, are placed in the S_0 register for translation. The origin of these addresses is determined by the contents of the instruction.

For example, if the address is to be transferred from the S_1 register to the S_0 register, L ⟹ S_1=C OR B MEM ADD, L ⟹ I, R1, W or I/O, and T21 signals are ANDED with a phase 1 to produce the proper transfer enable. Other transfer enables are generated similarly. These enables and their functions are listed below:

L ⟹ ESI ⟶ S_0	Enables transfer of the ESI to the S_0 register.
L ⟹ I/O TRANSLATOR ⟶ S_0	Enables transfer of the translated storage address for I/O operations.
L ⟹ ICR ⟶ S_0	Enables addressing of the currently active index register.
L ⟹ S1 ⟶ S_0	Enables transfer of the contents of the S_1 register to the S_0 register.
L ⟹ CLEAR S_0	Enables clearing the contents of the S_0 register to zero.
L ⟹ STORE SELECT ⟶ S_0	Enables transfer of the contents of the store select circuit to the S_0 register during an ESA operation.

The L ⟹ SET S_0 BIT 2^0 signal is used during the B2 or CONT DATA sequence to update the S_0 register by one.

(i) Z_0 REGISTER CONTROL. - The Z_0 register control circuit, (figure 9-25) supplies transfer enables to the Z_0 register to effect a data transfer either to, or from, the Z_0 register. These enables (produced as a product of sequence commands, timing pulses, and function code translation) direct the proper operation. The enables and their meanings are listed below:

L ⟹ CLEAR ⟶ Z_0	A signal which causes the Z_0 register to be cleared to all zeros.
L ⟹ B $\pm$1 ⟶ Z_0	Enables transfer of the contents of the B $\pm$1 network to the Z_0 register.
L ⟹ Z1 ⟶ Z_0	Enables transfer of the contents of the Z_1 register to the Z_0 register.
L ⟹ CONT MEM ⟶ Z_0	Enables transfer of the control memory sense-amplifier outputs to the Z_0 register.
L ⟹ BOOTSTRAP ⟶ Z_0	Enables transfer of the contents of the selected bootstrap memory address to the Z_0 register.

(j) STORE SELECT CONTROL. - Store select control circuit (figure 9-26) provides control of the input to the store select circuit. The enables generated determine the source of this input. These enables and their functions are listed below:

L ⟹ I/O ODD UPPER	Enables transfer of the contents of the C register associated with I/O channels 11, 13, 15, and 17 to the store select circuit.
L ⟹ I/O EVEN UPPER	Enables transfer of the contents of the C register associated with I/O channels 10, 12, 14, and 16 to the store select circuit.
L ⟹ I/O ODD LOWER	Enables transfer of the contents of the C register associated with I/O channels 1, 3, 5, and 7 to the store select circuit.
L ⟹ I/O EVEN LOWER	Enables transfer of the contents of the C register associated with I/O channels 0, 2, 4, and 6 to the store select circuit.
L ⟹ $\overline{\text{I/O}}$	Enables Arithmetic Selector to the store select circuits.

At any time other than T21, upper and lower odd channels are partially enabled so that odd channel inputs may be gated into the computer during the I/O sequence.

(k) ARITHMETIC SELECTOR CONTROL. - The arithmetic selector control circuits (figure 9-17) provide control for the transfer of data into the arithmetic section. Enables generated transfer the source of the data to the selector. Simultaneously, other enables are generated, which complete the transfer from the selector to the destination. The source-selecting enables and their functions are listed below:

L ⟹ AU ⟶ SELECT	Enables transfer of the contents of the AU register to the arithmetic selector circuit.
L ⟹ AL ⟶ SELECT	Enables transfer of the contents of the AL register to the arithmetic selector circuit.

L ⟹ P ⟶ SELECT	Enables transfer of the contents of the P register to the arithmetic selector circuit.
L ⟹ Z ⟶ SELECT	Enables transfer of the contents of either the Z_0 or Z_1 register to the arithmetic selector circuit. The Z register selected is a function of the Z select circuit and the instruction being executed.
L ⟹ SR + ICR + K ⟶ SELECT	Enables transfer of the contents of either the SR, ICR, or K register to the lower six bits of the arithmetic selector circuit. Bits 06 through 11 are held to zero during this sequence.
L ⟹ 0's ⟶ SELECT	Enables holding bits 12 through 17 of the arithmetic selector to zero.
L ⟹ SCALE FACTOR COUNT ⟶ X	Enables transfer of the contents of the K register (the scale factor count) to the arithmetic selector during a 50:44 instruction.

(1) CONTROL DESIGNATORS. - The control designator circuits, (figure 9-27 and 9-28) supply control enables for execution of several jump, compare, and arithmetic functions. These enables are the product of function code translation, main timing sequences, and timing pulses. The enables and their functions are listed below:

L ⟹ FORWARD	Indicates to the I/O control circuitry that a forward buffer is in progress and B register is to be incremented.
L ⟹ +1 ⟶ B	Enables updating or incrementing B register by a count of one.
L ⟹ -1 ⟶ B	Enables decrementing contents of the B register by a count of one.
L ⟹ BACKWARD	Indicates to the I/O control circuit that a backward buffer is in progress and contents of the B register are to be decremented.
L ⟹ MULTIPLIER STORE	Enables partial product generation and storage.
L ⟹ INHIBIT EAB	Prohibits an end-around-borrow to the adder circuit.
L ⟹ INSERT EAB	Enables an end-around borrow.
L ⟹ ALL INTERRUPT LOCKOUT	Used to disable setting the INT flip-flop, thus preventing execution of the interrupt sequence. This signal results from a 50:34 or 50:35 instruction or if the interrupt sequence is being executed currently.
L ⟹ LOCKOUT EXT INT	Used in the I/O section of the computer to prevent computer recognition of an external interrupt from a peripheral device.
H ⟹ HOLD 1	Disables the main sequence outputs during the execution of instructions which require more than the amount of time allowed by normal sequencing; that is, multiply, divide, shift, scale factor, or force instructions.

L ⟹ FORCE	Simulates an output request during inter-computer operation.
H ⟹ HOLD 2	Disables the main sequence outputs until the Ø1.3 of the I sequence, to allow the computer to resume logic functions at the selected point in timing.

(m) COMPLEMENT AND SHIFT CONTROL. - The complement and shift control logic (figure 9-33) supplies enables to the arithmetic section to allow shifting the contents of the A register (AU and/or AL) either right or left, and complementing the contents of AU and AL during multiply and divide instructions, as necessary.

If a 24 or 25 instruction (multiply) is to be executed and the number in the AL register is negative, the A NEG flip-flop, OXG30, will be set. If a 26 or 27 instruction (divide) is to be executed and the number in the A register is negative, the A NEG flip-flop will be set. If the instruction is 24-27 and the number read from memory is negative, the Y NEG flip-flop, 1XG30, will be set. If both flip-flops are either cleared or set, an enable is not generated to the auxiliary timing chain to complement AL. The L ⟹ COMP AU enable is generated if either one flip-flop or the other is set during a multiply or if the A NEG flip-flop is set during a divide.

At the completion of the instruction, the negative sign (stored in either the Y NEG or A NEG flip-flop) will be restored to the result.

Right or left shift enables are generated during multiplication, division, or shift instruction execution, as appropriate.

(5) REGISTERS. - Several registers which perform control functions are included in the control section of the computer. Included in this category are the ICR register, SR register, K register, K1 and K0 counter register, and B register. Each of these registers perform a logic control function not necessarily dependent upon contained data.

(a) ICR REGISTER. - The ICR register (figure 9-39) consists of three flip-flop circuits. Set or cleared condition of these flip-flops indicates, to a programmed instruction, the index register which is currently active. The index registers, used for B modification in most odd-numbered instructions, are actually memory address storage locations 001 through 007 and 010. Setting the corresponding address in the ICR register indicates to program control the memory address of the active index register. If no bits are set in the ICR register, memory address 010 is used as the active index register; if bit 1 is set, memory address 001 will be used; etc.

It is important to note that memory address 000 is the fault entrance address and not an index register. As stated previously, index registers are located in addresses 001 through 007 and 010.

(b) SR REGISTER. - SR register (figure 9-39) provides the upper four bits of the memory address when activated through program direction. The expanded memory capability requires a maximum of 16 bits to specify a given memory address. Because only 12 of these bits may be included in the programmed instruction, the additional four bits are supplied by either the upper four bits of the current P register content or by the SR register.

Setting bit 2^3 activates the SR register and extends the programmed 12 bits into 16 bits by using bits 2^0, 2^1, 2^2, and 2^4 of the SR register. This scheme is used to assure compatibility of this computer with other UNIVAC computers and peripheral equipments.

When bit 2^3 is cleared, the SR register is deactivated and the four bits are supplied by the upper four bits of the current P register content. The bit content of the instruction to activate the SR register is shown in figure 4-9.

(c) KO and K1 COUNTER REGISTER. - The KO and K1 counter register (figure 9-37) is a two-rank register; each rank composed of six flip-flop circuits. The upper rank is designated as K1 and the lower rank is designated as KO. The primary purpose of the register is to function as a counter during multiply, divide, shift and scale factor operations. During these instructions, the contents of the K register designate the number of shift operations to be performed.

During the execution of a Format II instruction, the lower six bits (k portion) of the instruction word are placed in the K register. During a 50:72 instruction, the lower three bits of the K register are transferred to the ICR register (K00-K02 $\longrightarrow$ ICR). During a 50:73 instruction, the lower five bits of the K register are transferred to the SR register (L $\Longrightarrow$ K00-K04 $\longrightarrow$ SR).

The contents of the K register may also indicate the channel to be used during an I/O type instruction.

For a skip (50:50) or stop (50:56) instruction, the contents of the K register designate the active switch for execution of the programmed operation.

(d) B REGISTER and $\pm$1 NETWORK. - The B register (BU register in figure 9-2) and $\pm$1 network (figures 9-118, 9-119, and 9-120) is composed of 18 flip-flop circuits and associated gating elements to either add or subtract a logical one from the contents of the B register.

This network primarily increments or decrements the buffer control word, and also is used to specify the memory address to be used during an ESA operation.

Inputs to the B register are routed from either the Z_0 register or store select circuit. Command enables from the control designator circuit enable adding or subtracting a logical one from the contents of the B register and thus execute the increment or decrement function.

(6) SPECIAL CIRCUITS. - The control section of the computer contains several circuits classified as special, because they perform functions associated with only a few instructions. In this category are comparison designators, jump control, stop/skip logic, parity, and alarm logic.

(a) COMPARISON DESIGNATORS. - Comparison designators (figure 9-29) are represented by the compare block in the block diagram (figure 9-2) and consist of three flip-flop circuits and their associated input gating circuits. The three flip-flop circuits are compare, equal, and greater. Comparison designators are used during the execution of the four compare instructions, 02, 03, 06, and 07, to indicate the result of a comparison and store this result for further use. To use the result of a compare instruction, the next sequential instruction must be one of the 60 through 67 jump instructions. This is necessary because the comparison designators are cleared by the subsequent execution of any instruction other than 60 through 67. When the COMPARE flip-flop is set, all interrupts are disabled to prevent clearing the designators.

1. COMPARE. - The COMPARE flip-flop, OXG36, is set by the execution of any of the compare instructions to provide the H $\Longrightarrow$ COMPARE signal to disable possible interrupts. This flip-flop is cleared by Ø4.1 of the next sequential I sequence of any instruction other than 60 through 67.

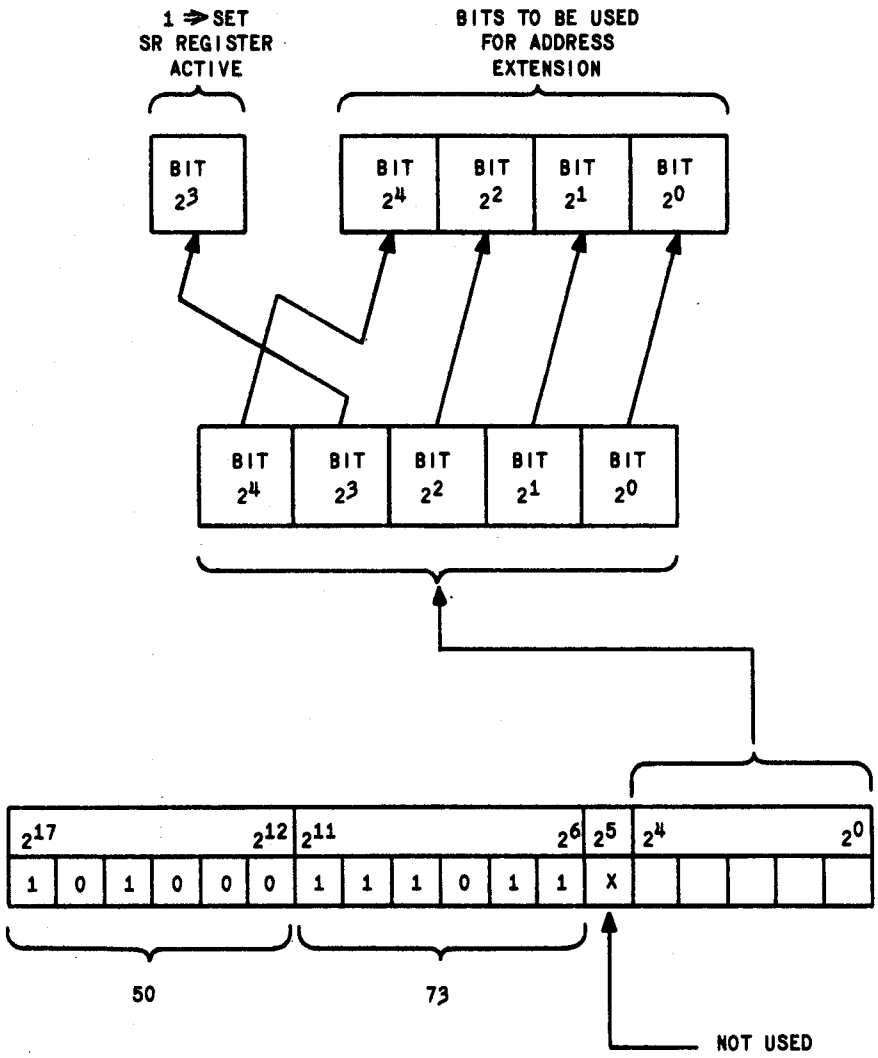


Figure 4-9. Bit Content, Activate SR Instruction

2. EQUAL. - The EQUAL flip-flop, OXG34, is set during an 02 or 03 instruction if the contents of the AL register equal the contents of the addressed memory location. It is set during an 06 or 07 instruction if the logical product of the contents of the AL and AU registers is equal to the logical product of the contents of the AU register and the addressed memory location. This flip-flop will be cleared coincident with the COMPARE flip-flop.

3. GREATER. - The GREATER flip-flop, OXG36, is set during an 02 or 03 instruction if the contents of the AL register are equal to, or greater than, the contents of the addressed memory location. It is set during an 06 or 07 instruction if the logical product of the AL and AU registers is equal to, or greater than, the logical product of the contents of AU register and addressed memory location. This flip-flop is cleared coincident with COMPARE flip-flop.

The greater check is performed by testing the sign bit of the X and D registers and looking for the presence or absence of an EAB. The value held in the X register is the contents from the arithmetic registers. The value in the D register is the complement of the contents of the memory location. The GREATER flip-flop is set when signs are unequal and there is no EAB, or when the signs are equal and there is an EAB.

If signs are unequal when checked, the two values to be compared have the same sign because D register contains the complement of one of the quantities. If signs are equal, conversely, one of the quantities is negative and the other positive. If there is no EAB when signs are unequal, the value in the X register must be equal, or greater than, the quantity from memory (A) $\geq$ (Y). If there is an EAB and signs are equal, then the value in the X register is positive and the other negative. Therefore, it follows that (A) > (Y).

(b) JUMP CONTROL. - Jump control logic (figure 9-29) is used during the execution of the 60 through 67 instructions to determine whether the conditions specified for the jump have been satisfied. Unlike skip instructions, which allow the omission of the next sequential instruction only, jump instructions may select any memory address for the next instruction providing that address is contained in the memory stack of the jump instruction word. If the conditions specified for the jump are satisfied, address of the next instruction to be performed is supplied by the (Y) portion of the jump instruction word, and bits 12 through 15 of the current P register contents.

If the following conditions are satisfied, a jump will occur. If these conditions are not satisfied, the next sequential instruction in the program will be executed.

60 Instruction - COMPARE flip-flop of the comparison designator is cleared and (AU) = + 0 or both the COMPARE and EQUAL flip-flops of the comparison designator are set.

61 Instruction - COMPARE flip-flop of the comparison designator is cleared and (AL) = + 0 or both the COMPARE and EQUAL flip-flops of the comparison designator are set.

62 Instruction - COMPARE flip-flop of the comparison designator is cleared and (AU) $\neq$ 0 or the COMPARE flip-flop of the comparison designator is set but the EQUAL flip-flop is cleared.

63 Instruction - COMPARE flip-flop of the comparison designator is cleared and (AL) $\neq$ 0 or the COMPARE flip-flop of the comparison designator is set but the EQUAL flip-flop is cleared.

64 Instruction - COMPARE flip-flop of the comparison designator is cleared and (AU) is positive or both the COMPARE and GREATER flip-flops of the comparison designator are set.

65 Instruction - COMPARE flip-flop of the comparison designator is cleared and (AL) is positive or both the COMPARE and GREATER flip-flops of the comparison designator are set.

66 Instruction - COMPARE flip-flop of the comparison designator is cleared and (AU) is negative or the COMPARE flip-flop of the comparison designator is set and the GREATER flip-flop is cleared.

67 Instruction - COMPARE flip-flop of the comparison designator is cleared and (AL) is negative or the COMPARE flip-flop of the comparison designator is set and the GREATER flip-flop is cleared.

(c) STOP/SKIP LOGIC. - Stop/skip logic (figures 9-30, 9-31, and 9-32) provides the programmed control of computer operation during any of the stop or skip instructions. The circuitry performs those operations which determine if the programmed conditions have been satisfied to effect a stop or skip. In addition to switch-controlled stops and skips, the circuitry tests for overflow, parity, borrows, I/O channel inactivity, and resume conditions. If skip conditions are satisfied, the computer initiates a second advance P subsequence and skips the next sequential instruction in the program. If these conditions are not satisfied, the computer executes the next sequential programmed instruction in the normal manner. Paragraph 3-6 includes stop and skip instructions and conditions required for compliance.

(d) PARITY. - Several instructions in the computer repertoire require a check of the number of one's contained in a binary 18-bit word. To perform this check, the parity circuit (figure 9-101) investigates the bit content of the arithmetic selector. If the resultant bit count is an even number, the output of the parity circuit is a high. If the count is odd, the output is a low. This output is then routed to the skip circuitry for evaluation during either a 50:54 or 50:55 instruction.

(e) ALARM LOGIC. - Alarm logic circuitry (figure 9-121) supplies signals to both local and remote indicators to present a visual display of fault and operational conditions.

Program fault signal is the result of an illegal function code (00, 01, or 77) being contained in an instruction.

The temperature warning signal is the result of an increase in cabinet temperature above the 115 degrees F (46 degrees C) limit.

A voltage fault signal is the result of an abnormal regulated voltage condition in the memory circuits.

The loss-of-air signal is the result of a loss of cooling air through the main memory core stacks.

b. INPUT/OUTPUT SECTION.

(1) I/O CHANNELS. - Each I/O channel is connected to a peripheral device (or another computer) with an input cable and an output cable. Normally, each cable

has 18 data lines and 4 control lines. For dual-channel operation, cables with 36 data lines are used. All data lines and control lines are twisted pair.

Any computer channel can operate as a normal channel or as an intercomputer channel. Switch selection for each channel is provided on the I/O panel. The switch circuitry is shown in logic figures 9-61 thru 9-64.

(a) NORMAL. - Normal class of operation for an I/O channel is used whenever the channel is connected to a peripheral device (figure 4-10). The normal class of operation subordinates the peripheral device to the computer for most I/O operations.

The output cable has the following control lines: external function request, output data request, external function acknowledge, and output data acknowledge. Request lines, which carry signals to the computer, inform the computer that the peripheral device is ready to accept a word of the type requested. Acknowledge lines, which carry signals from the computer, inform the peripheral device that a word of the type requested is on the data lines.

The input cable contains the following control lines: external interrupt request, input data request, and input acknowledge. Request lines, which carry signals to the computer, inform the computer that the peripheral device is ready to accept a word of the type requested. The acknowledge line, which carries signals to the peripheral device, informs the peripheral device that the computer has read the data lines.

(b) INTERCOMPUTER. - Intercomputer class of operation for an I/O channel is used whenever the channel is connected to another computer (figure 4-11). The intercomputer class of operation subordinates the sending computer to the receiving computer.

Cables used to connect two computers are identical to cables used when connecting a computer to peripheral devices. However, with the computers switched into the intercomputer class of operation, two control lines in each cable assume different meanings.

In the output cable of either computer, the output acknowledge line in normal interface becomes the ready line in intercomputer interface. The ready signal indicates to the receiving computer that the sending computer has placed a word on data lines. The output data request line in normal interface becomes the resume line in intercomputer interface. The resume signal indicates to the sending computer that the receiving computer has accepted the last data sent.

(c) DUAL. - An even-odd channel pair can be placed in dual mode by positioning a CHANNEL FUNCTION switch on the I/O panel. Cables with 36 data lines must be connected to the odd-numbered channel of the channel pair (figure 4-12). Cables cannot be connected to the even channel of the pair when in dual mode. Channel mode selector switches are shown in logic figure 9-67.

(2) I/O OPERATIONS. - Logical flow diagrams are provided for data transfer operations: input data transfer, external interrupt transfer, output data transfer, and external function transfer. Separate diagrams are provided for single-channel (18-bit) and dual channel (36-bit) operations.

Table 4-2 lists I/O flow diagrams. These diagrams should be used in conjunction with logic diagrams in section 9, volume II, to obtain detailed information on input/output section operation.

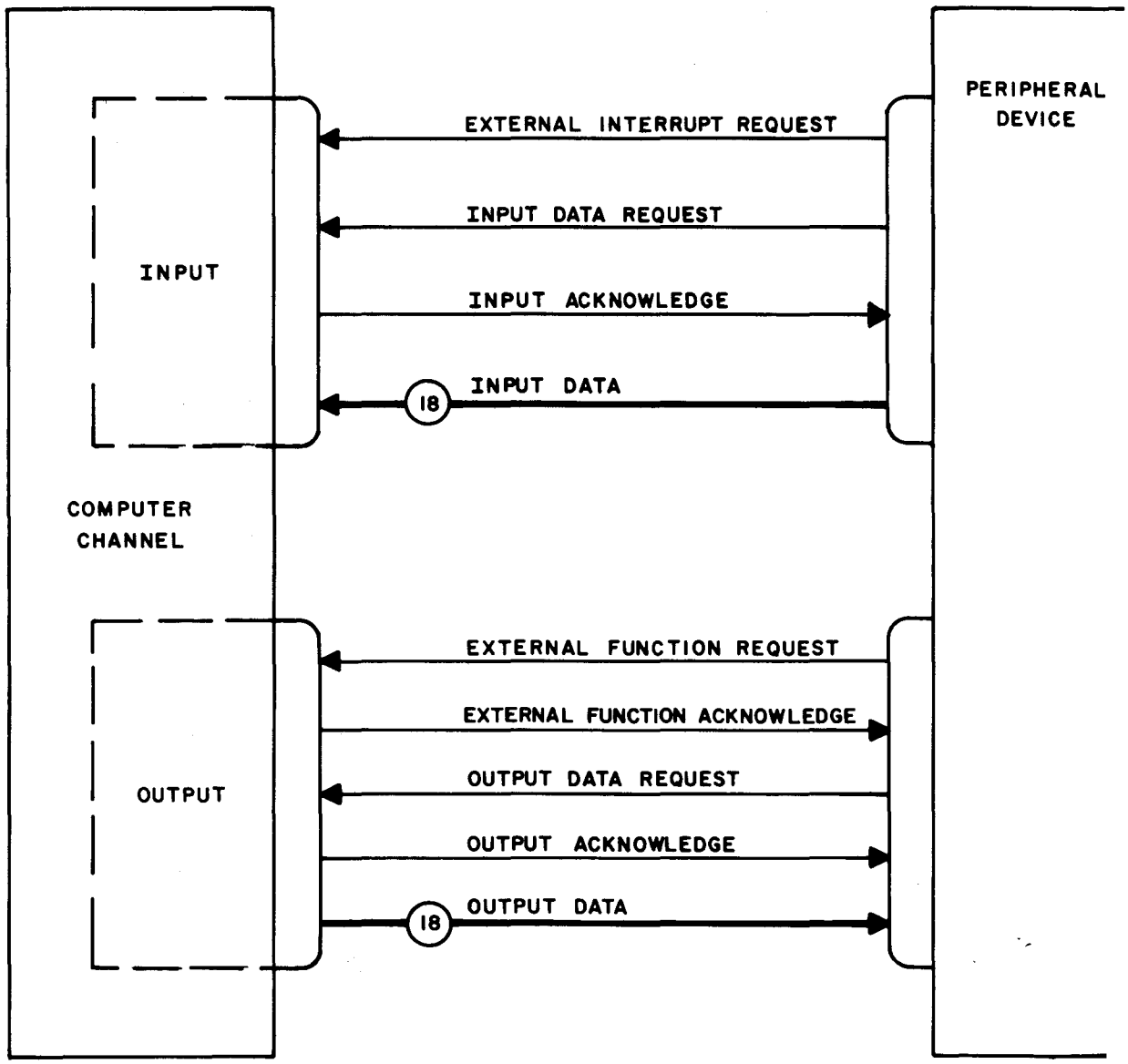


Figure 4-10. Normal I/O Interface

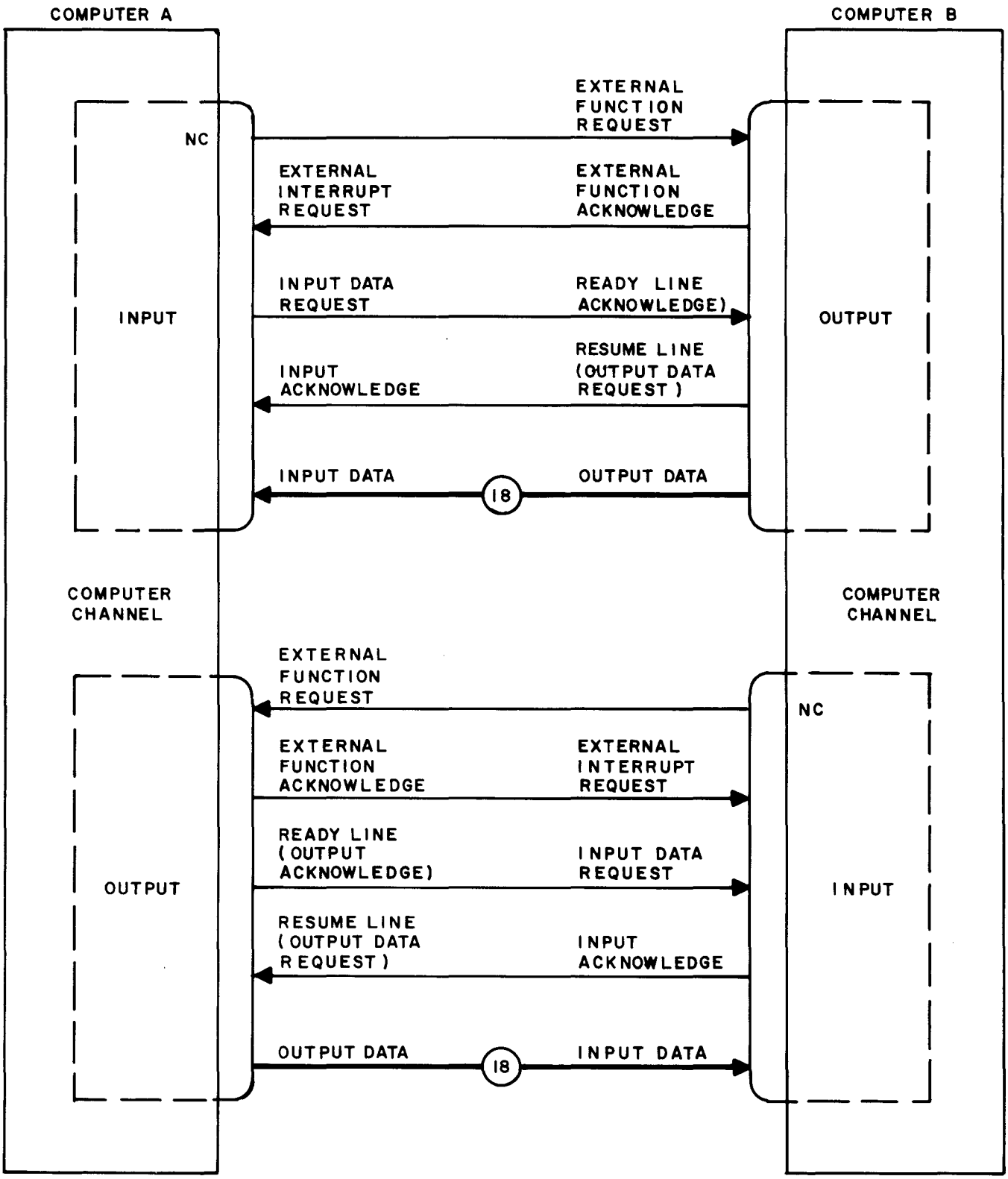


Figure 4-11. Intercomputer I/O Interface

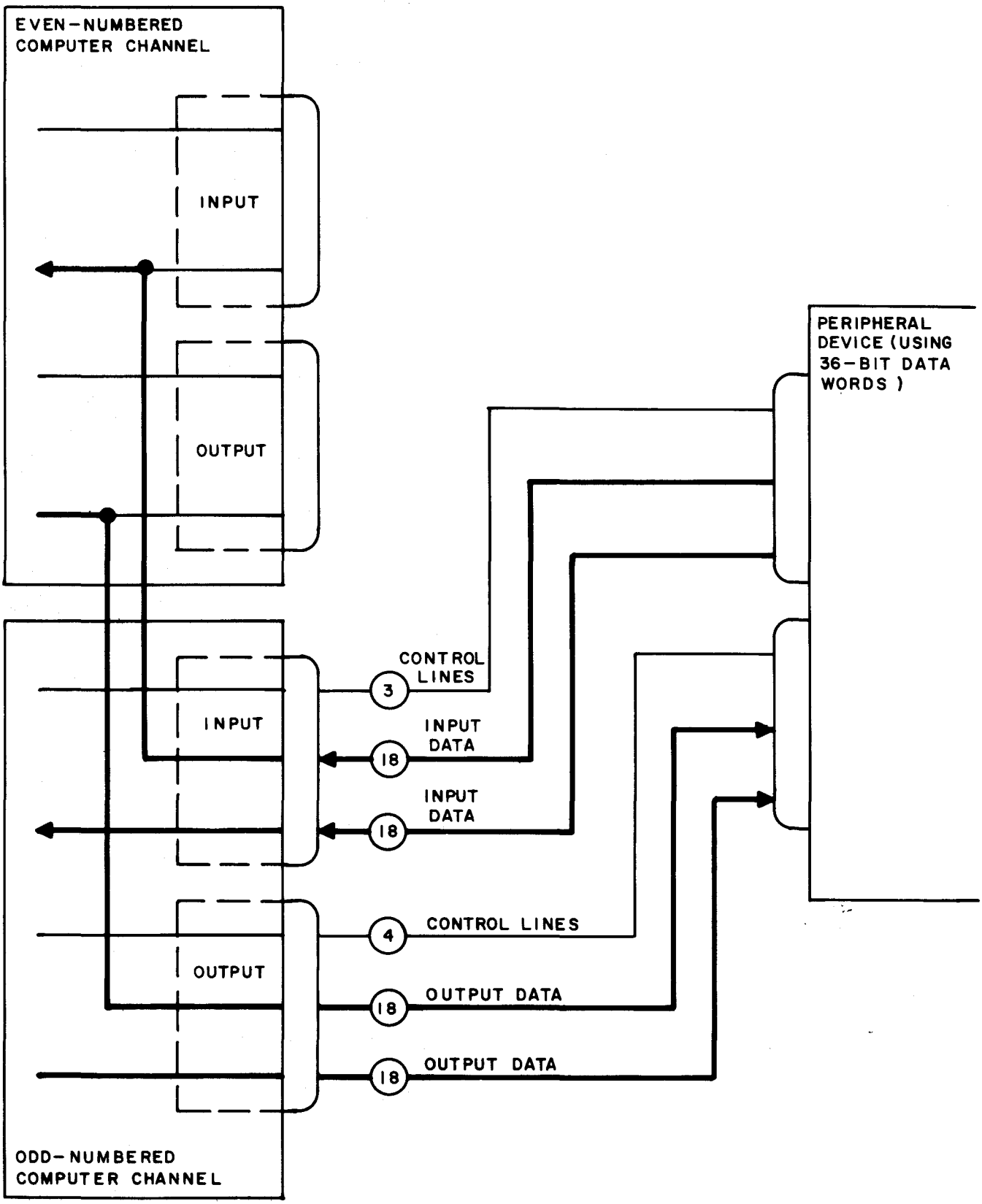


Figure 4-12. Dual Channel I/O Interface

TABLE 4-2. INDEX OF I/O FLOW DIAGRAMS

Figure	Flow Diagram
4-13	18-Bit Input Data Transfer
4-14	36-Bit Input Data Transfer
4-15	18-Bit External Interrupt Transfer
4-16	36-Bit External Interrupt Transfer
4-17	18-Bit Output Data Transfer
4-18	36-Bit Output Data Transfer
4-19	18-Bit External Function Transfer
4-20	36-Bit External Function Transfer

(3) I/O TIMING. - I/O timing consists of sequence timing and interface timing.

(a) SEQUENCE TIMING. - Sequence timing for the I/O section includes scan timing, and command timing for input/output sequences. Scan timing, listed in table 4-3, operates during all command sequences of all instructions except I/O instructions, which are listed in table 4-2. It is also inhibited during I/O 1 sequence, when in the dual mode or if in the ESI mode and about to terminate a buffer, or if a continuous data mode request is present. Scan timing runs during the R1 sequence of instructions 20-23 and 57, but I/O 1 flip-flop cannot be set. Scan timing is divided into two parts; during the first half it checks for data requests (either output or input types of operation), and in the second half for interrupt requests.

Sequence timing tables list the commands and conditions for each sequence and, in the case of the I/O sequences, the mode of operation is given. I/O sequences, I/O 1 and I/O 2, are listed in tables 4-4 and 4-5. The I/O 1 sequence is used to read the buffer control words, compare them, and then write the current address buffer control word back into control memory, as well as storing or transmitting a data word. I/O 2 sequence follows I/O 1 sequence when the computer is in the dual mode or in ESI mode, and terminating a buffer.

Table 4-6, continuous data mode sequence, lists the times and the commands for the CDM sequence. Table 4-7 gives the command timing for the real-time clock sequence.

Table 4-8 lists the interrupt sequence which runs parallel to the I sequence when a fault interrupt has been received or an I/O interrupt has been scanned-up. The interrupt sequence forces the computer to a specified address where the I sequence then takes over and controls the performance of the instruction which was stored at that address.

(b) INTERFACE TIMING. - Interface timing for both the slow and fast interfaces are shown in figures 4-21 and 4-22. Interface time shows the time duration for all the control signals generated by the computer and peripheral device during an input or output data transfer.

TABLE 4-3. SCAN TIMING

TIME	COMMAND	TYPE
T4.4	CLR Chan and Function Priority	Request Scan
T1.1	Reqs ⟶ Channel Priority	Request Scan
T1.4	Reqs ⟶ Function Priority	Request Scan
T2.1	CLR Xlator 1, and Channel and Function Xlator	Request Scan
T2.2	Enable Force Instruction Chan Prio Req ⟶ Xlator 1 Set I/O 1 Seq. Lower rank (if Request exists) Chan and Function Prio ⟶ Chan And Function Xlator Check for Dual Mode Initiate RTC Sequence	Resume Scan Request Scan Request Scan Request Scan Request Scan RTC Seq Scan
NOTE	The following commands are inhibited if a data request was scanned-up.	
T2.4	CLR Chan and Function Priority	Interrupt Scan
T3.1	Int Req ⟶ Chan Priority CLR Xlator 1, Channel and Function Xlator	Interrupt Scan I/O Type Inst. Scan
T3.2	f & k to Xlator 1, Channel and Function Xlator	I/O Type Inst. Scan
T3.4	Int Req ⟶ Function Priority	Interrupt Scan
T4.1	CLR Xlator 1, and Channel and Function Xlator	Interrupt Scan
T4.2	Chan Prio Req ⟶ Xlator 1 set Int 1, Upper rank (if monitor request exists) Chan and Function Prio ⟶ Chan and Function Xlator	Interrupt Scan Interrupt Scan

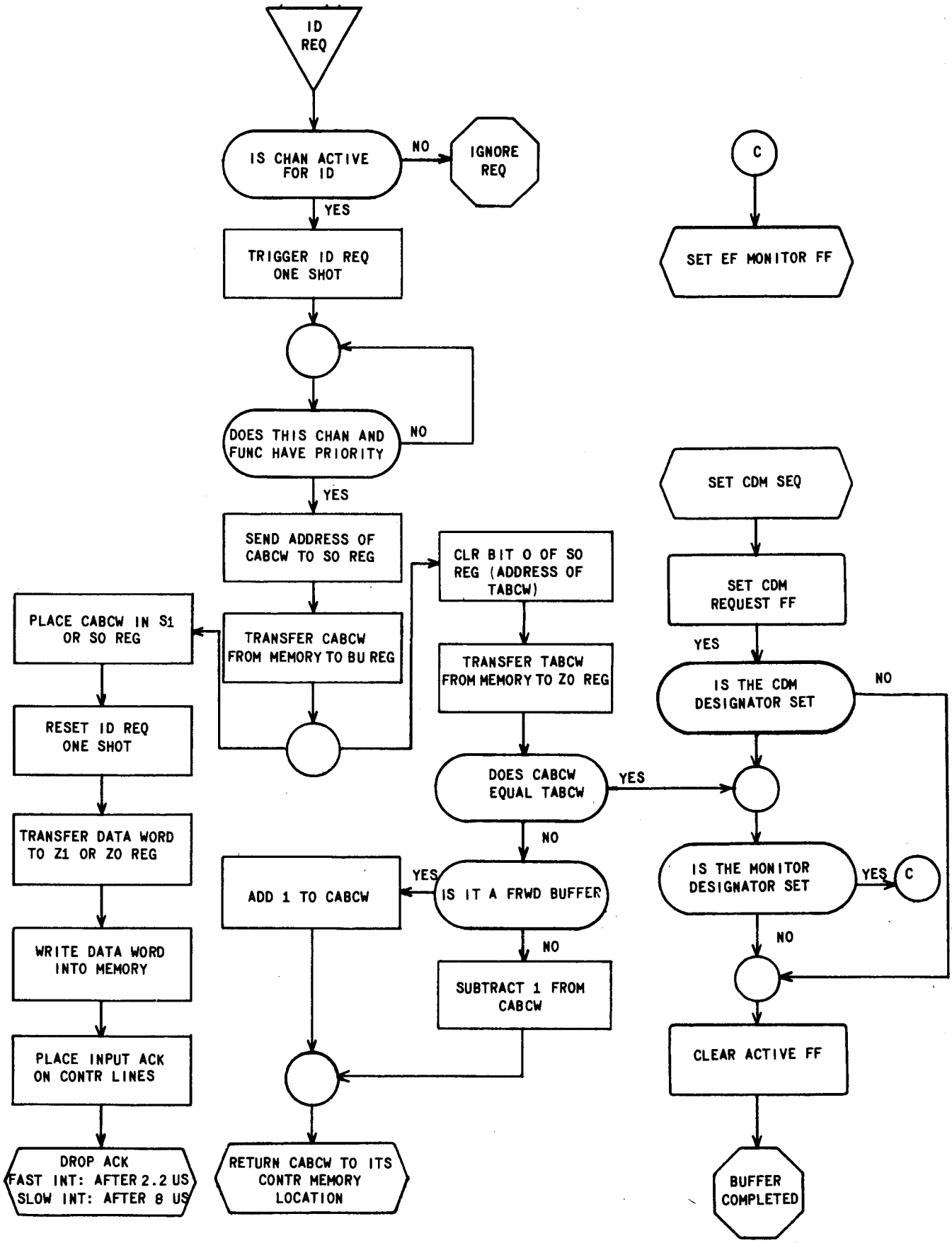


Figure 4-13. Simulation of Events for a Single (18-Bit) Input Data Transfer

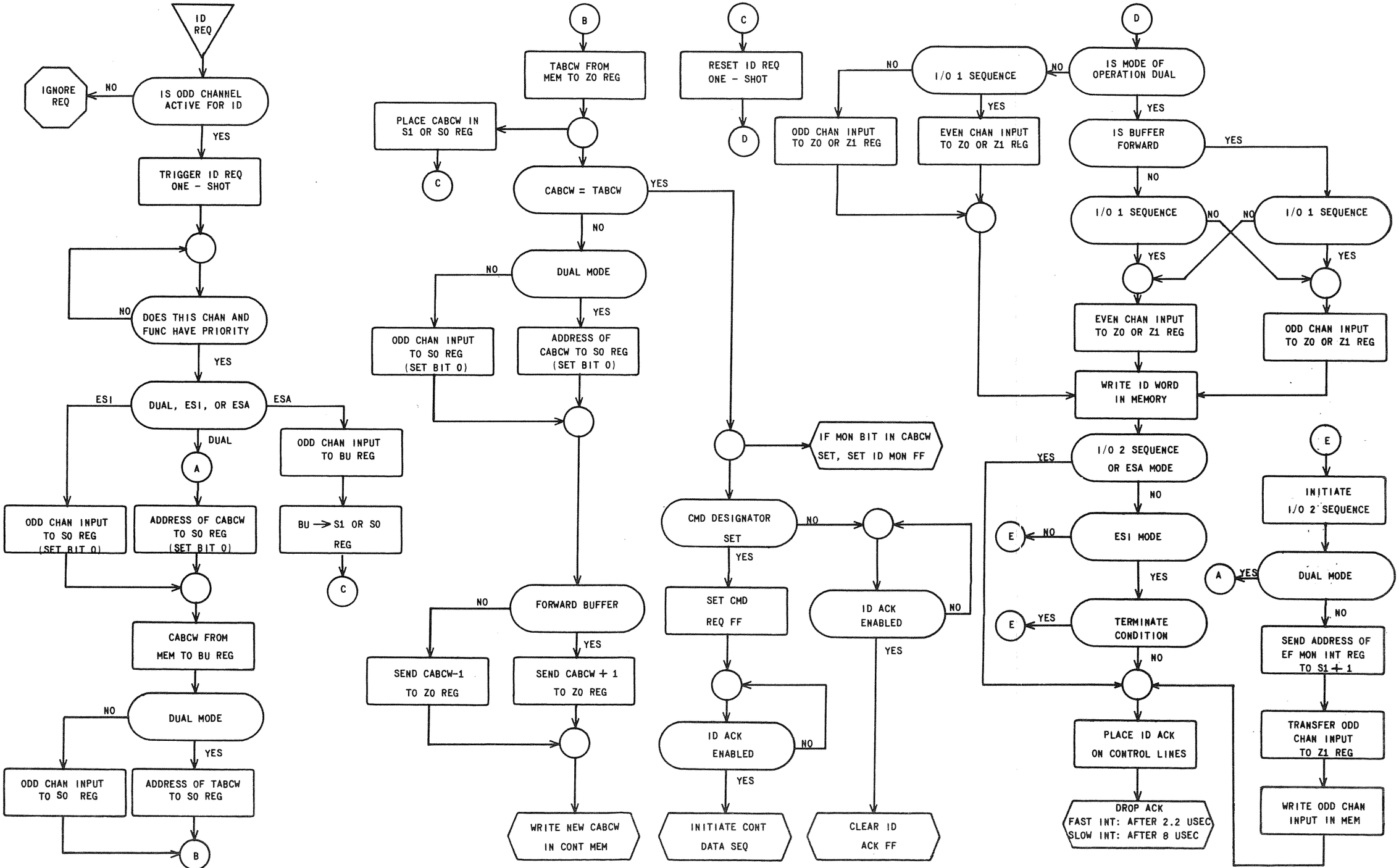


Figure 4-14. Simulation of Events for a 36-Bit Input Data Transfer

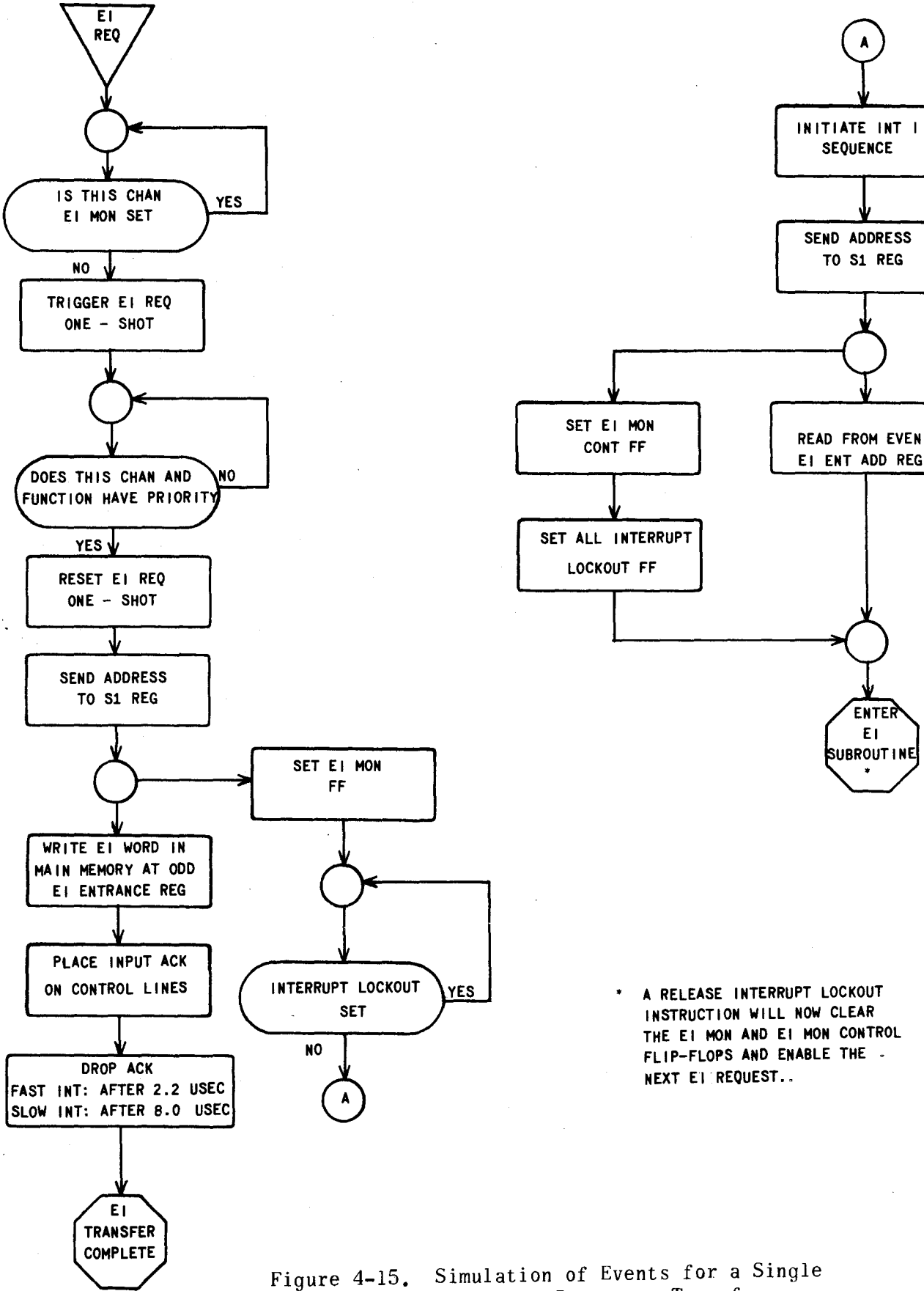


Figure 4-15. Simulation of Events for a Single (18-Bit) External Interrupt Transfer

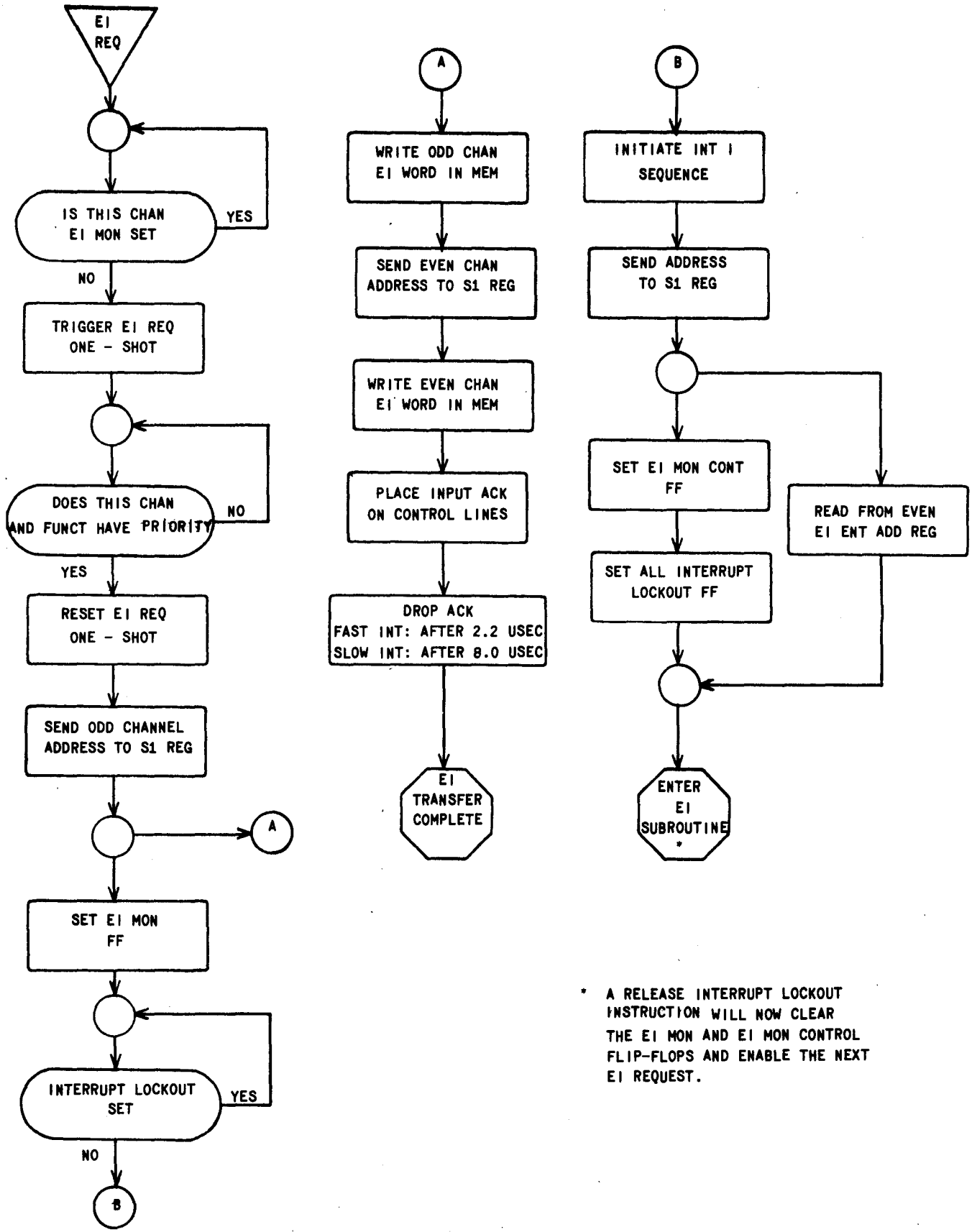


Figure 4-16. Simulation of Events for a Dual (36-Bit) External Interrupt Transfer

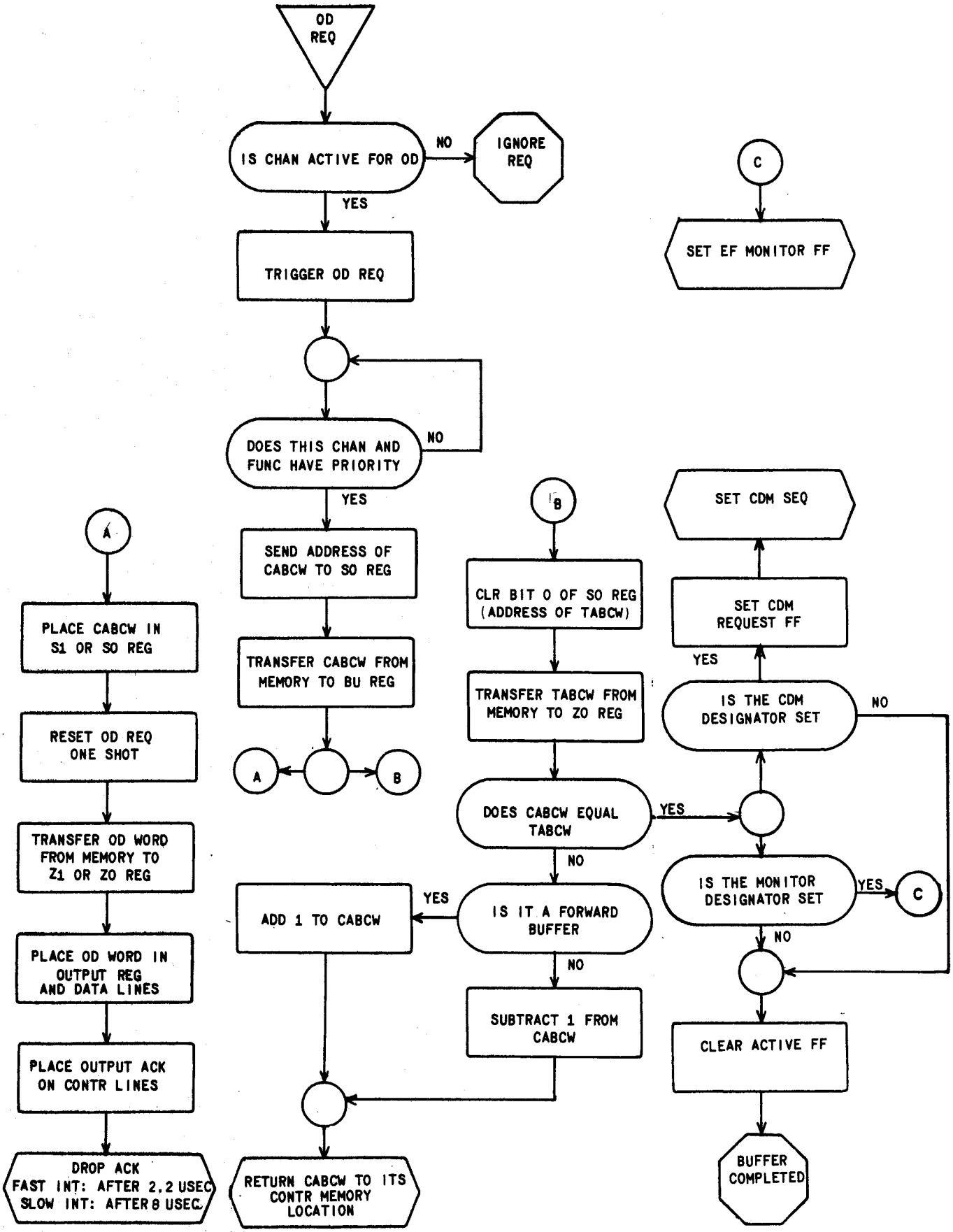


Figure 4-17. Simulation of Events for a Single Output Data Transfer

TABLE 4-4. I/O 1 SEQUENCE

TIME	COMMAND	CONDITION			
		SINGLE	DUAL	ESI	ESA
T3.1	I/O Xlator ⟶ S0	Not EI	Not EI	--	--
	ESI ⟶ S0	--	--	Not EI	--
	Initiate Control Memory	Not EI	Not EI	Not EI	--
	Set S0 ⟶ 2^0	x	x	x	--
	CLR Z0	x	x	x	x
T3.2	CLR Bu	x	x	x	x
T3.3	Control Memory ⟶ Z0	Not EI	Not EI	Not EI	--
T3.4	Z0 ⟶ Bu	x	x	x	--
	Odd Input Chan ⟶ Bu	--	--	--	Not EI
T4.1	I/O Xlator ⟶ S0	Not EI	Not EI	--	--
	ESI ⟶ S0	--	--	Not EI	--
	Initiate Control Memory	Not EI	Not EI	Not EI	--
	Set B ± Desig to + 1	x	x	x	x
	CLR ⟶ Z0	x	x	x	x
T4.2	Xlator I ⟶ Xlator II	x	x	x	x
	Set B ± 1 Desig to -1				
	If bkwd buffer bit set	Not EI	Not EI	Not EI	--
T4.3	CLR Resume FF	OD/EF	OD/EF	OD/EF	OD/EF
	Set Input Ack. Register	ID/EI	ID/EI	ID/EI	ID/EI
	CLR ID/EI Req FF	ID/EI	ID/EI	ID/EI	ID/EI
	Control Memory ⟶ Z0	Not EI	Not EI	Not EI	--
T4.4	Terminate	BU = Z0	BU = Z0	BU = Z0	
	Set CDM Req FF if CDM				
	bit set	BU = Z0	BU = Z0	BU = Z0	
T1.1	I/O Xlator ⟶ S0	Not EI	Not EI	--	--
	ESI ⟶ S0	--	--	Not EI	--
	Initiate Control Memory	Not EI	Not EI	Not EI	--
	CLR Z0	x	x	x	x
	Set S0 ⟶ 2^0	x	x	x	x
	Bu ⟶ S1	Not EI	Not EI	Not EI	Not EI
	I/O Xlator ⟶ S1	EI	EI	EI	EI
	Set S1 ⟶ 2^0 and 2^6	EI	EI	EI	EI
	Enable Main Memory	x	x	x	x
T1.2	B ±1 ⟶ Z0	Not EI	Not EI	Not EI	Not EI
T1.3	CLR Z1	x	x	x	x
	CLR ID Active FF	Terminate ID & CDM	Terminate ID & CDM	Terminate ID & CDM	
	Set EI Monitor	EI	EI	EI	EI
	Set Monitor FF if				
	Monitor bit set	Terminate	Terminate	Terminate	

TABLE 4-4. I/O 1 SEQUENCE (CONT.)

TIME	COMMAND	CONDITION			
		SINGLE	DUAL	ESI	ESA
T1.3 (Cont.)	Set Terminate OD/EF FF	OD/EF & Terminate & CDM	OD/EF & Terminate & CFM	OD/EF & Terminate & CDM	--
	Set OD/EF Ack. Reg.	OD/EF	OD/EF	OD/EF	OD/EF
	CLR OD/EF Req. FF	OD/EF	OD/EF	OD/EF	OD/EF
T1.4	Input Channel → Z1	ID/EI	ID/EI (even chan if bkwd, odd chan if fwrd)	ID EI (even chan) (even chan if bkwd, odd if fwrd)	ID EI (even chan) (odd chan)
	Start OD/EF Ack Timing	OD/EF		OD/EF & Terminate	
T2.1	Start ID/EI Ack Timing	ID/EI	--	ID/EI & Terminate	ID/EI
	S1 → S0 if S1=CM address	x	x	x	x
	Initiate CM if CM address	x	x	x	x
	CLR Z0 if CM address	x	x	x	x
T2.2	Main Memory → Z1	OD/EF	OD/EF	OD/EF	OD/EF
	Set I/O 2 SEQ (Lower Rank)	--	x	Terminate	--
	Set CDM SEQ	CDM REQ SET	--	CDM REQ SET & TERM	--
	Z1 → Z0 if CM address	ID	ID	ID	ID
T2.3	Control Memory → Z0	OD/EF and S0	OD/EF and S0	OD/EF and S0	OD/EF and S0
T2.4	Z1 or Z0 → Z SELECT	OD/EF	OD/EF	OD/EF	OD/EF
	Z SELECT → C	OD/EF	OD/EF (odd chan if fwrd or even chan if bkwd)	OD/EF (both chan)	OD/EF (both chan)

TABLE 4-5. I/O 2 SEQUENCE

TIME	COMMAND	CONDITION	
		DUAL	ESI
T3.1	I/O Xlator → S0	Not EI	--
	ESI → S0	--	--
	Initiate Control Memory	Not EI	--
	Set S0 → 2^0	x	--
	CLR Z0	x	x
T3.2	CLR Bu	x	x
T3.3	Control Memory → Z0	Not EI	--
T3.4	Z0 → Bu	x	--
	Input → Bu	--	--
T4.1	I/O Xlator → S0	Not EI	--
	ESI → S0	--	--
	Initiate Control Memory	Not EI	--
	Set B ±1 Desig to +1	x	x
	CLR Z0	x	x
T4.2	Xlator I → Xlator II	x	x
	Set B ±1 Desig -1 if bkwd buffer bit set	x	x
T4.3	Control Memory → Z0	Not EI	--
	CLR Resume FF	OD/EF	OD/EF
	Set Input Ack Register	ID/EI	ID/EI
	CLR ID/EI Req FF	ID/EI	ID/EI
T4.4	Terminate	BU = Z0	x
	Set CDM Req FF if CDM bit set	BU = Z0	x
T1.1	I/O Xlator → S0	Not EI	--
	ESI → S0	--	--
	Initiate CM	Not EI	--
	CLR Z0	x	--
	Set S0 → 2^0	x	--
	BU → S1	Not EI	--
	I/O Xlator → S1	EI	x
	Set S1 → 2^0 and 2^6	EI	x
	Initiate Main Memory	x	x
T1.2	B ±1 → Z0	Not EI	Not EI
T1.3	CLR Z1	x	x
	CLR ID Active FF	Terminate & CDM	Terminate & CDM
	Set EI Monitor	EI	EI
	Set Monitor FF if Monitor Bit set	Terminate	Terminate

TABLE 4-5. I/O 2 SEQUENCE (CONT.)

TIME	COMMAND	CONDITION	
		DUAL	ESI
T1.3 (Cont.)	Set Terminate OD/EF FF	OD/EF & Terminate & CDM	OD/EF & Terminate & CDM
	Set OD/EF Ack. Reg.	OD/EF	OD/EF
	CLR OD/EF Req. FF	OD/EF	OD/EF
T1.4	Input Chan ⟶ Z1	ID/E (odd chan if bkwd, even chan if frwd)	ID (odd chan) EI (even chan if fwrd, odd if bkwd)
	Start OD/EF Ack Timing	OD/EF	OD/EF
T2.1	Start ID/EI Ack Timing	ID/EF	ID/EF
	S1 ⟶ S0 if S1 = CM address	x	x
	Initiate CM if CM	x	x
	CLR Z0 if CM address	x	x
T2.2	Main Memory ⟶ Z1	OD/EF	OD/EF
	Set CDM Seq	CDM Req. FF Set	CDM Req. FF Set
	Z1 ⟶ Z0 if CM address	ID	ID
T2.3	Control Memory ⟶ Z0 if CM address	OD/EF	OD/EF
T2.4	Z1 ⟶ Z Select	OD/EF	--
	Z0 ⟶ Z Select if CM address	OD/EF	--
	Z Select ⟶ C	OD/EF (even chan if fwrd or odd chan if bkwd)	--

TABLE 4-6. CONTINUOUS DATA MODE SEQUENCE

TIME	COMMAND
T3.1	Xlator → S0 Set S0 → 2^0 Initiate Control Memory CLR Z0
T3.2	CLR Bu
T3.3	Control Memory → Z0
T3.4	
T4.1	Xlator → S0 Set S0 → 2^0 Initiate Control Memory Inhibit Clear Z0
T4.2	
T4.3	Inhibit Control Memory → Z0
T4.4	
T1.1	Xlator → S0 Initiate Control Memory Xlator → S1 CLR Z0
T1.2	
T1.3	Control Memory → Z0
T1.4	
T2.1	S1 → S0 Inhibit Clear Z0 Initiate Control Memory
T2.2	
T2.3	Inhibit Control Memory → Z0

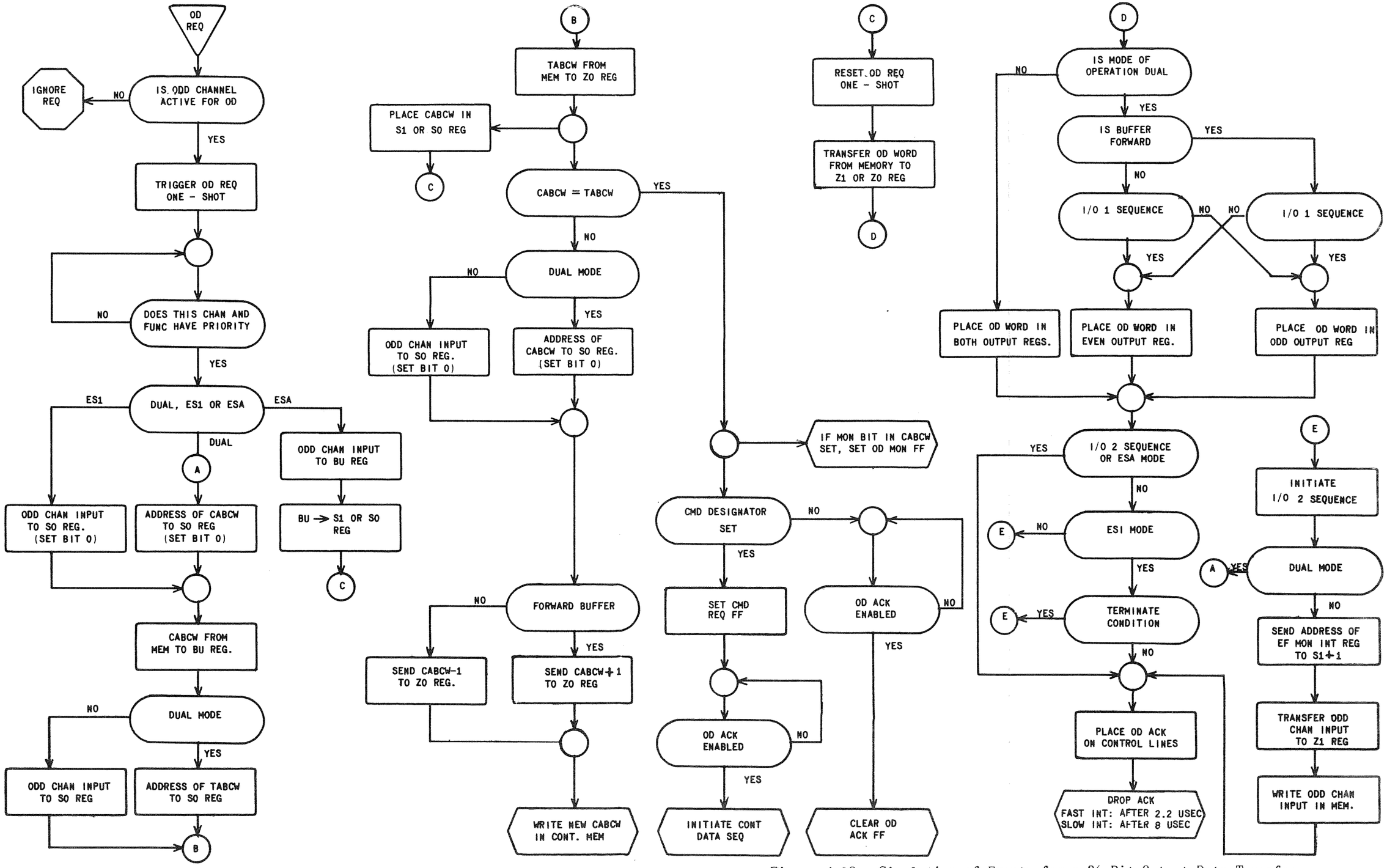


Figure 4-18. Simulation of Events for a 36-Bit Output Data Transfer

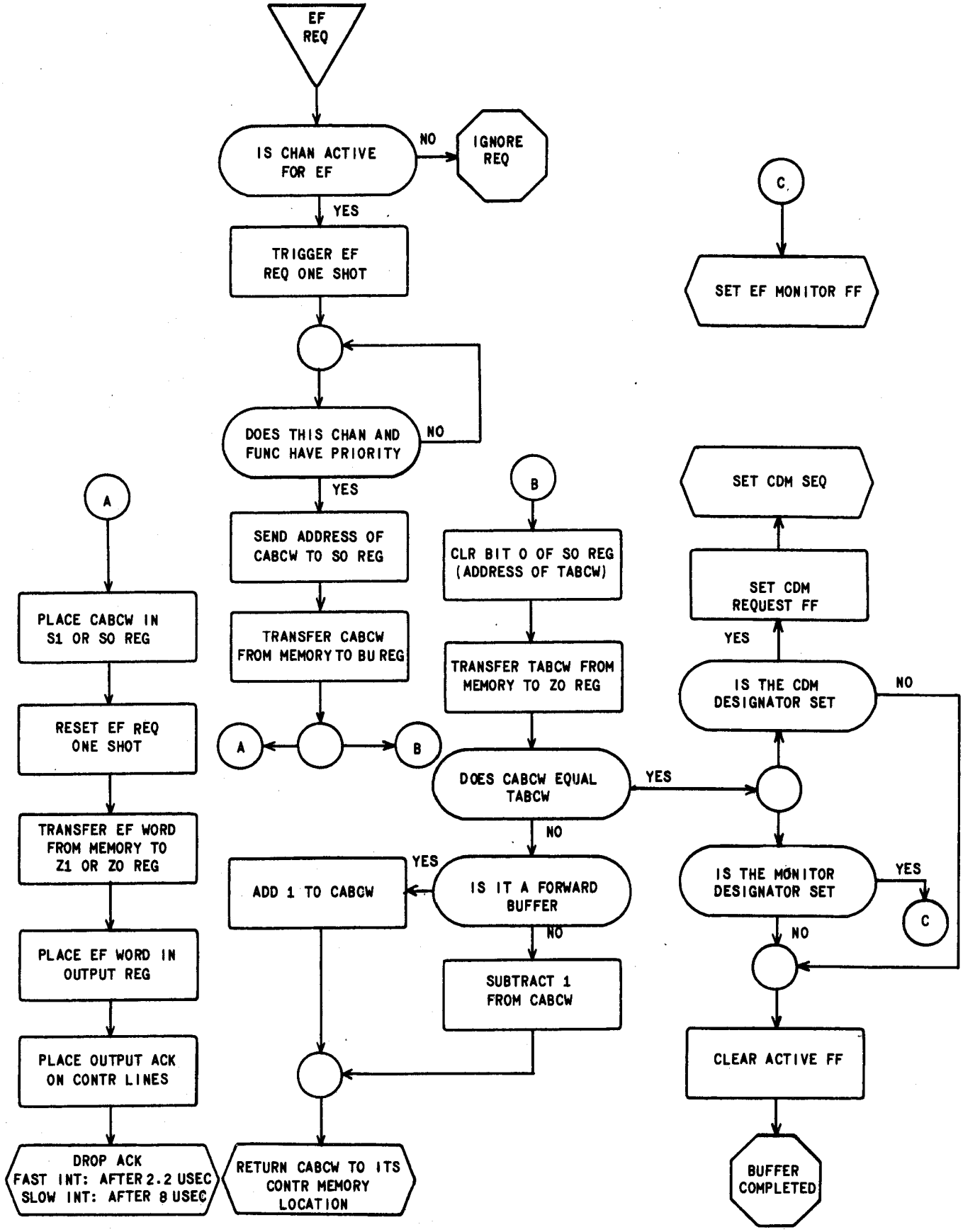


Figure 4-19. Simulation of Events for a Single (18-Bit) External Function Transfer

TABLE 4-7. REAL-TIME CLOCK SEQUENCE

TIME	COMMAND	CONDITION
T2.2	Initiate RTC Sequence Set Xlator to RTC Address Set I/O 1 FF (Lower Rank)	RTC request
T3.1	Xlator ⟶ S0 Set ⟶ S0 Bit 2^0 Initiate Control Memory	Read RTC Count
T3.2	CLR B, Z0	
T3.3	Control Memory ⟶ Z0	
T3.4	Z0 ⟶ B	
T4.1	Xlator ⟶ S0 Initiate Control Memory Set B ± Designator to +1 CLR $\overline{Z0}$	Read RTC Monitor Word
T4.2	Set I/O 1 FF (Upper Rank)	
T4.3	Control Memory ⟶ Z0	
T4.4	Set Terminate FF	B = Z0
T1.1	Xlator ⟶ S0 Set S0 2^0 Initiate Control Memory Set Resume fault CLR Z0	Store RTC Count (advanced) Resume not available & B 2^{10} changing
T1.2	B + 1 ⟶ Z0 Set RTC Monitor FF Set RTC Overflow FF CLR Resume Fault monitors	 RTC MON REQ FF set and terminate B = 777777 B 2^{10} changing
T1.3	CLR RTC Monitor Request FF Inhibit Control Memory ⟶ Z0	RTC MON FF set

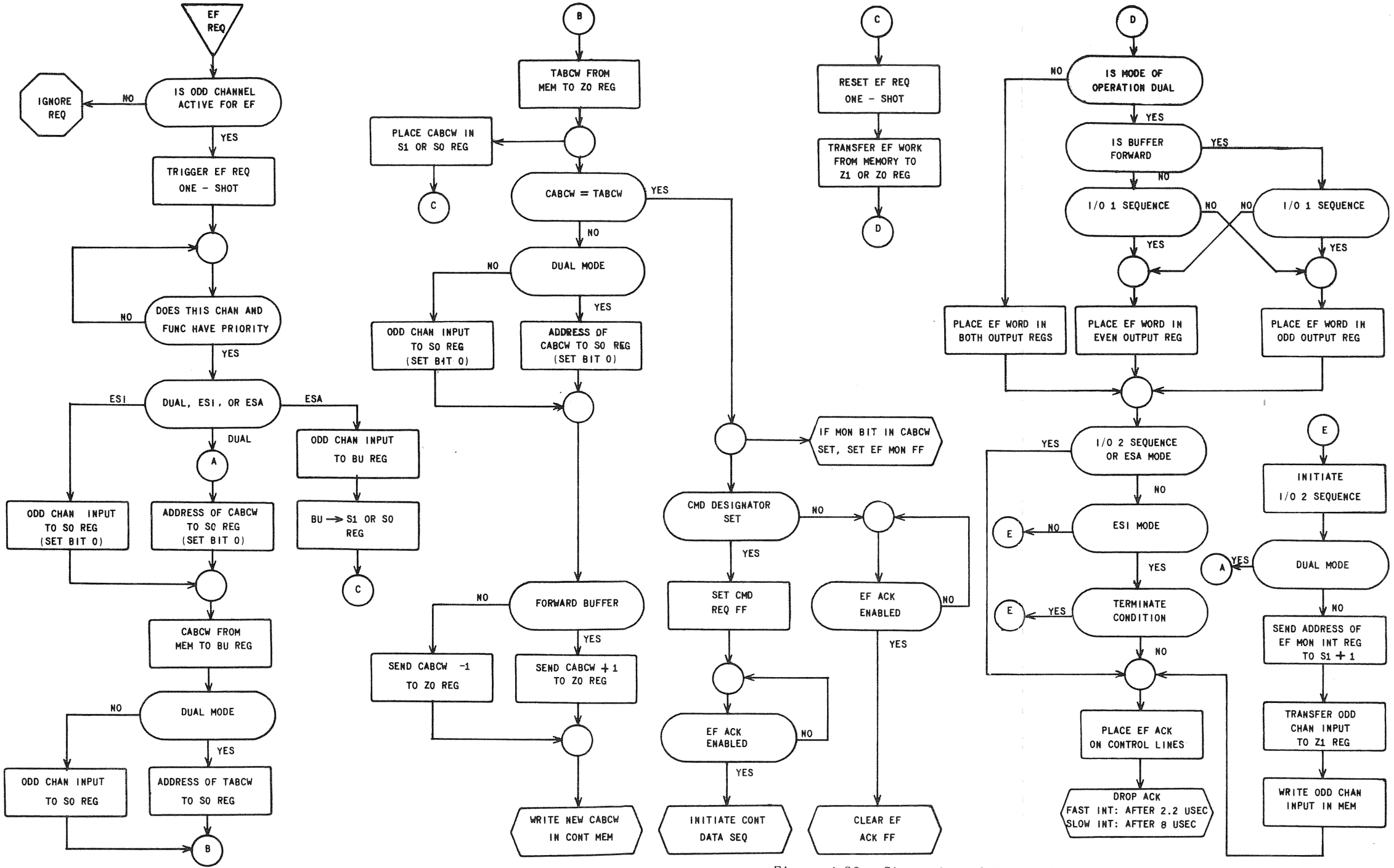
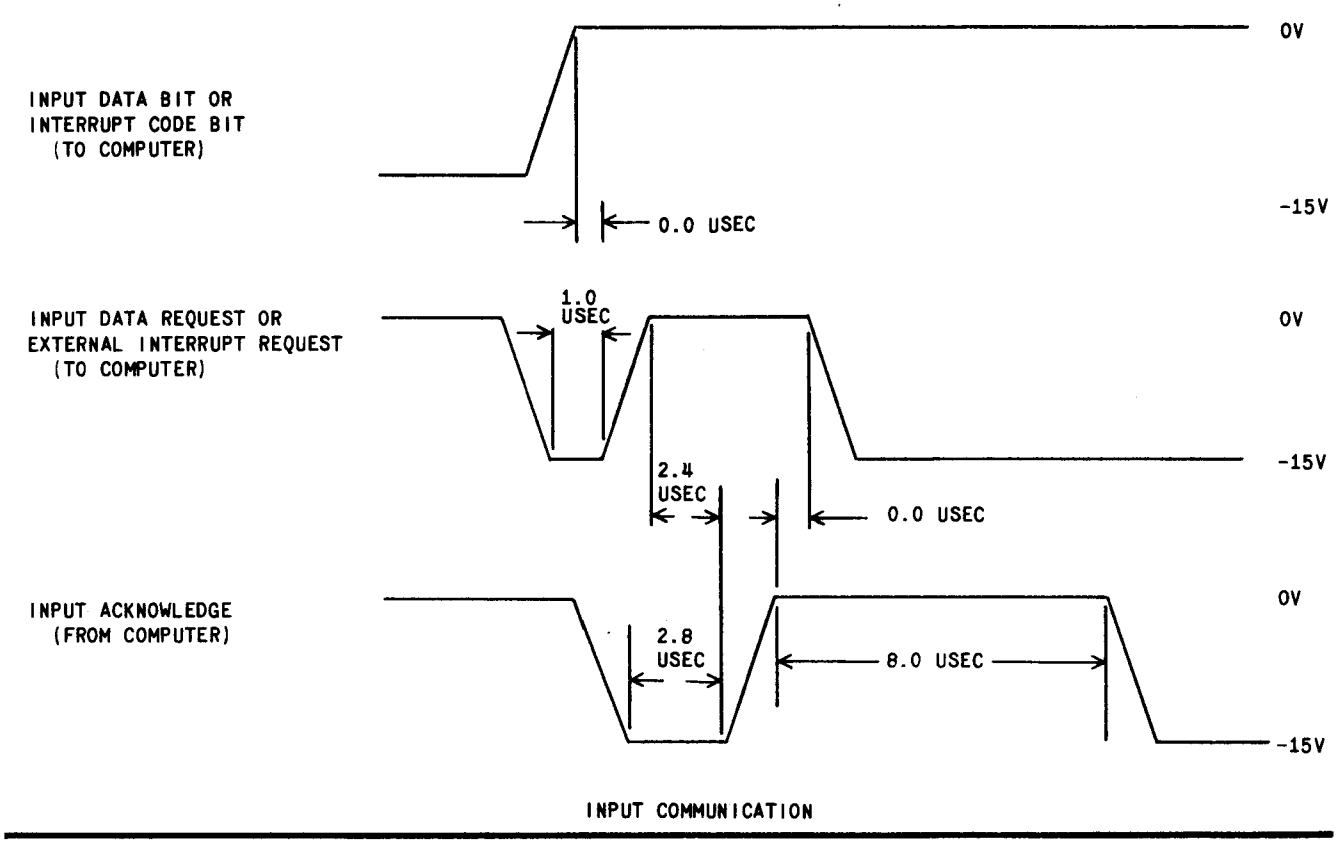
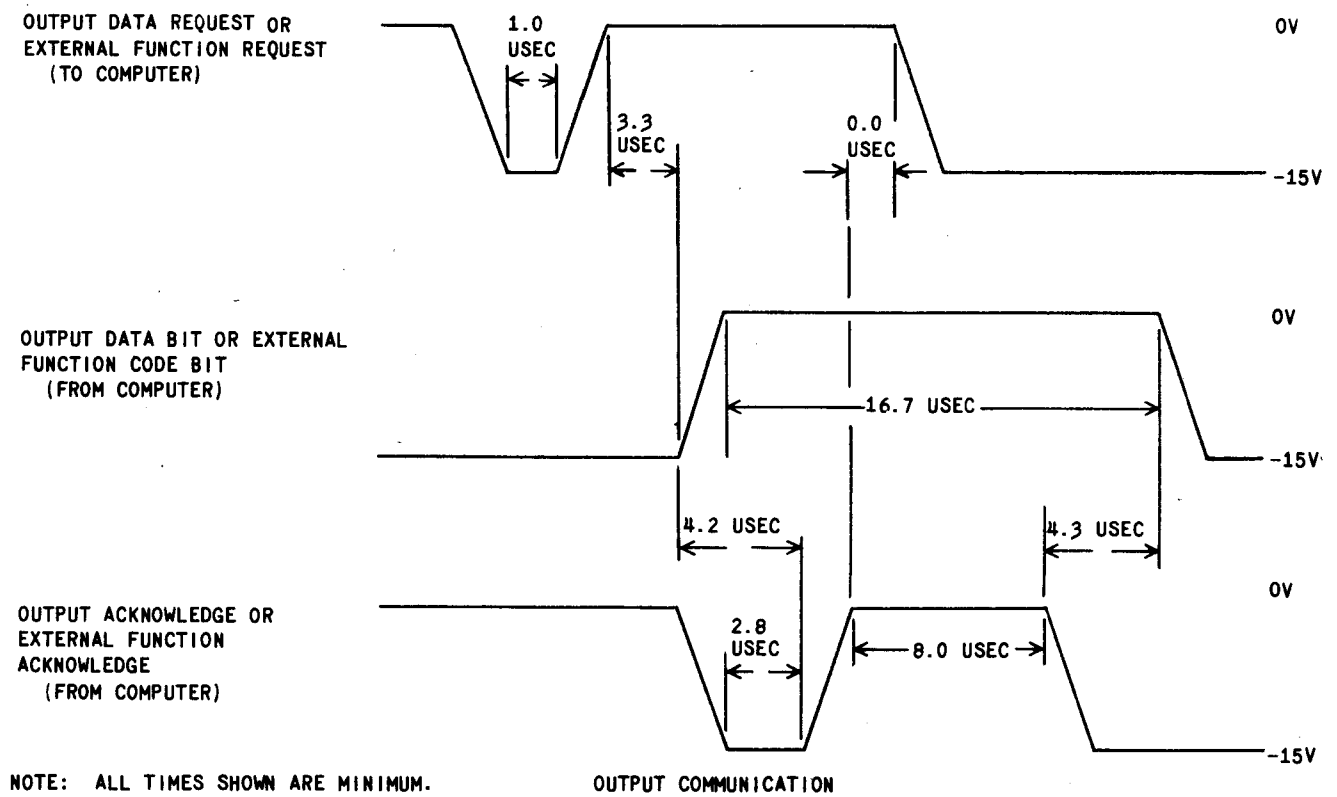


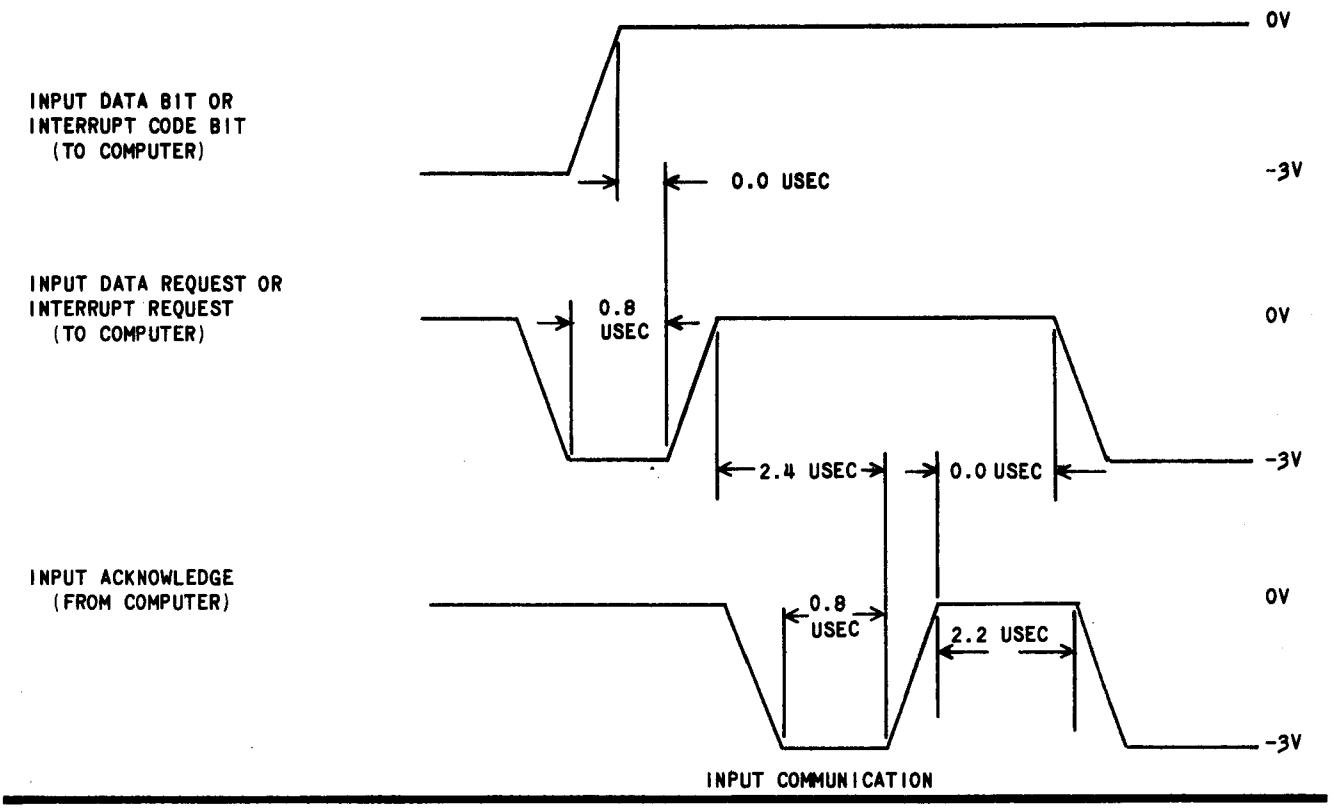
Figure 4-20. Simulation of Events for a 36-Bit External Function Transfer

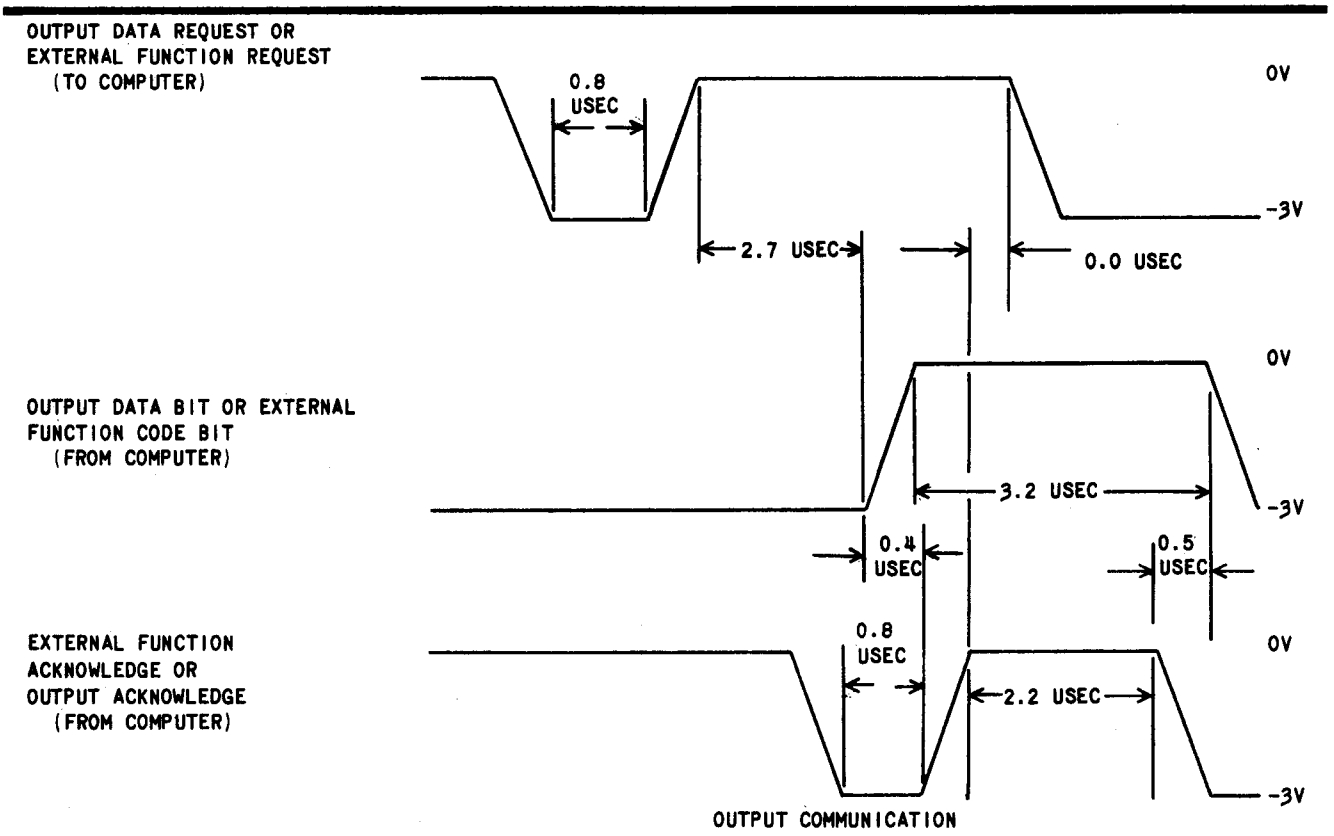




NOTE: ALL TIMES SHOWN ARE MINIMUM.

Figure 4-21. Slow Interface Timing





NOTE: ALL TIMES SHOWN ARE MINIMUMS.

Figure 4-22. Fast Interface Timing

TABLE 4-8. INTERRUPT SEQUENCE

TIME	COMMAND	CONDITION
T4.2	Set INT & I FF (Upper Rank)	I/O Int
T4.3	Spec Int Req ⟶ Spec Int Xlator	Not Instruction Fault
T1.1	Disable Adder ⟶ S1 of I SEQ Disable P ⟶ S1 of I SEQ SPECIAL INT REQ ⟶ S1 SET S1 Bit ⟶ 2^0 I/O Translator ⟶ S1 (Bits 4,5, & 7) S1 ⟶ S0 & Initiate CM Disable Set INCR, P FF of I SEQ CLR Z0 Initiate Main Memory	Int Seq & Spec Int Int Seq SPECIAL INT REQ Resume, EI, or RTC OVERFLOW Monitor INT and SP. INT REQ if S1 = Control Memory address
T1.3	Clear Processed interrupt Clear Inst Fault FF Clear processed monitor Control Memory ⟶ Z0	SP INT REQ $\overline{\text{SP INT REQ}}$ if S1 —— S0
T1.4	Lockout all interrupts	
T2.2	Set INT & I FF (Lower Rank)	
T3.4	Disable PU ⟶ DU of I SEQ Disable SR ⟶ D 12-15 of I SEQ Disable Reinitiation of WAIT SEQ	f ≠ 36, 37, 70, 71 and SR is not active or f = 30, 31, 34, 35 f = 00-27, 32, 33, 40-47 and SR is Active

c. ARITHMETIC SECTION.

(1) GENERAL. - The arithmetic section of the computer (figure 4-23) is composed of five flip-flop registers, a subtractive-type adder, and a logic-selecting circuit. The arithmetic section performs the following arithmetic operations: add, subtract, multiply, divide, shift, and scale factor. It also performs certain logical functions including masking, selective substitution, comparison, complement, and word transfers between elements of the arithmetic section, and between the arithmetic section and the control section and memory. These operations and logic functions are initiated and sequentially executed by command enables supplied from the control section.

The five flip-flop registers are the AU register, AL register, X register, W register, and the D register. The logic control circuit is the arithmetic selector and is commonly called select in the functional schematics of section 9. The subtractive type adder is the modifying circuit, which produces the arithmetic results used for numerical computations.

Although portions of the arithmetic section are used for the execution of several instructions, only those relating to arithmetic functions are discussed under the arithmetic section heading.

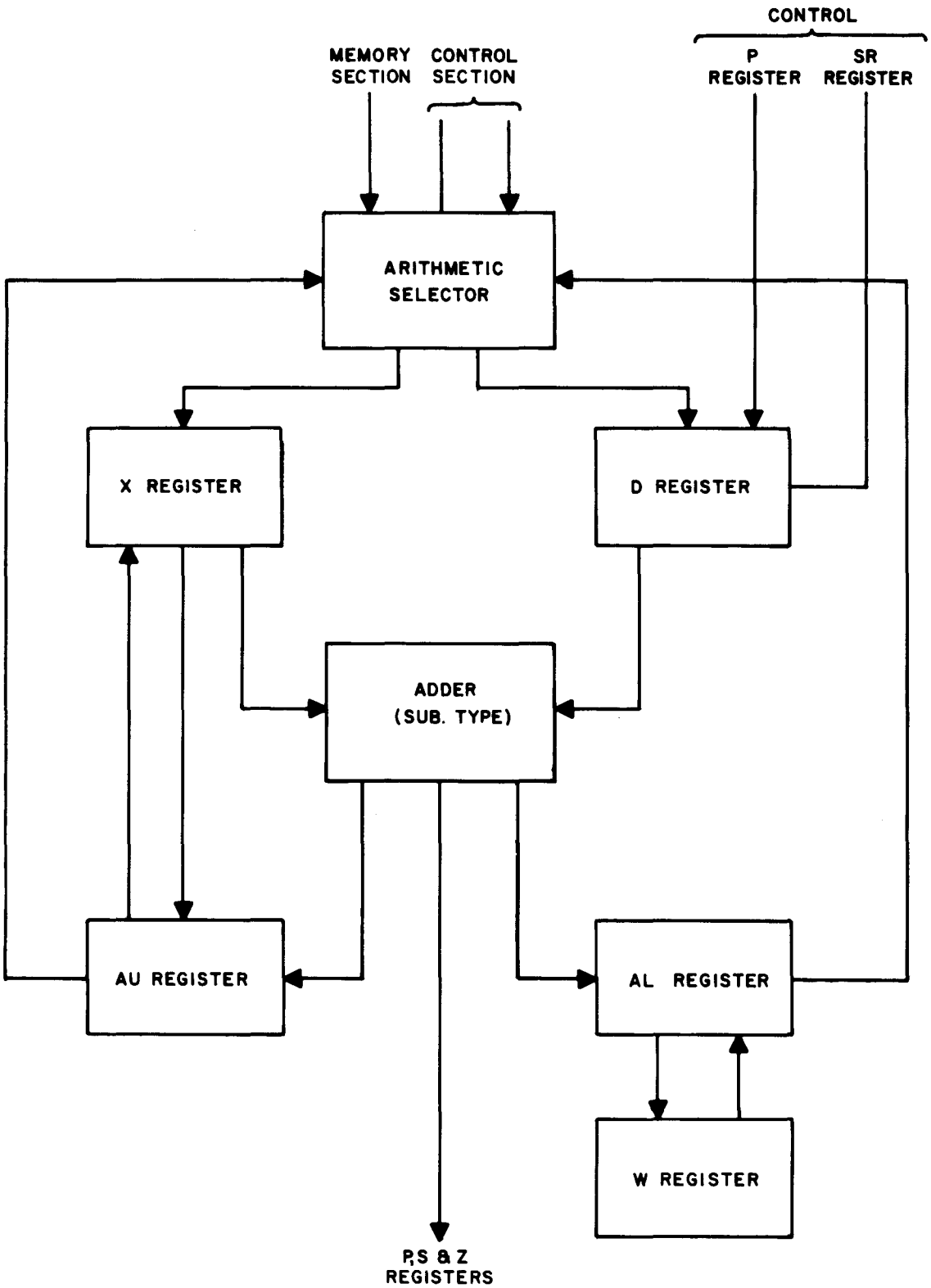


Figure 4-23. Arithmetic Section, Block Diagram

(2) FUNCTIONAL DESCRIPTION.

(a) REGISTERS. - The A register, consisting of AU (the upper 18 bits) and AL (the lower 18 bits); and the D, W, and X registers participate in arithmetic operations and provide temporary storage for results. Only the AU and AL registers are addressable through programmed instructions. The D, W, and X registers perform in conjunction with the AU and AL registers to produce the desired arithmetic functions.

1. AU REGISTER. - The AU register (figures 9-97 and 9-98) is composed of 18 flip-flop circuits and contains the upper 18 bits of the A register. The AU register performs the following functions:

1) Stores most significant 18 bits of augend prior to a 36-bit addition operation and the most significant 18 bits of the sum after addition.

2) Stores most significant 18 bits of minuend prior to a 36-bit subtract operation and the most significant 18 bits of the difference after subtraction.

3) Stores most significant bits of the product after multiplication.

4) Stores most significant bits of the dividend prior to a divide operation and the remainder after division.

5) Stores the most significant 18 bits of the information to be shifted during execution of double-length (36-bit) shift instructions.

6) Has shifting properties when used in conjunction with the X register.

7) Holds mask during certain logical operations.

Inputs to the AU register are from the X register and the adder and are direct bit-position transfers; that is, bit 2^0 of either the X register or the adder is transferred to bit 2^0 of the AU register. Input is controlled by the two command enables L $\Longrightarrow$ X $\longrightarrow$ AU and L $\Longrightarrow$ ADDER $\longrightarrow$ AU.

Outputs from the AU register are routed to the X register and the arithmetic selector. Output to the X register is routed to one of the two adjacent stages during shift operations. Figure 4-24 is a simplified diagram of these transfers and command enables under which they are executed. Output to the arithmetic selector is a direct transfer to bits from the AU register to corresponding bits in the arithmetic selector.

Additional outputs from the AU register are:

1) A18 (2^0) to the complement and shift control circuit during a right-shift A operation to shift the least significant bit of AU to the most significant bit position of AL.

2) A composite output from AU to the comparison designators to determine if the contents of AU are equal to zero.

3) A33, A34, and A35 to the auxiliary timing chain to indicate termination of a scale factor operation.

4) A35 to the control designators to indicate the presence or absence of an end-around-borrow.

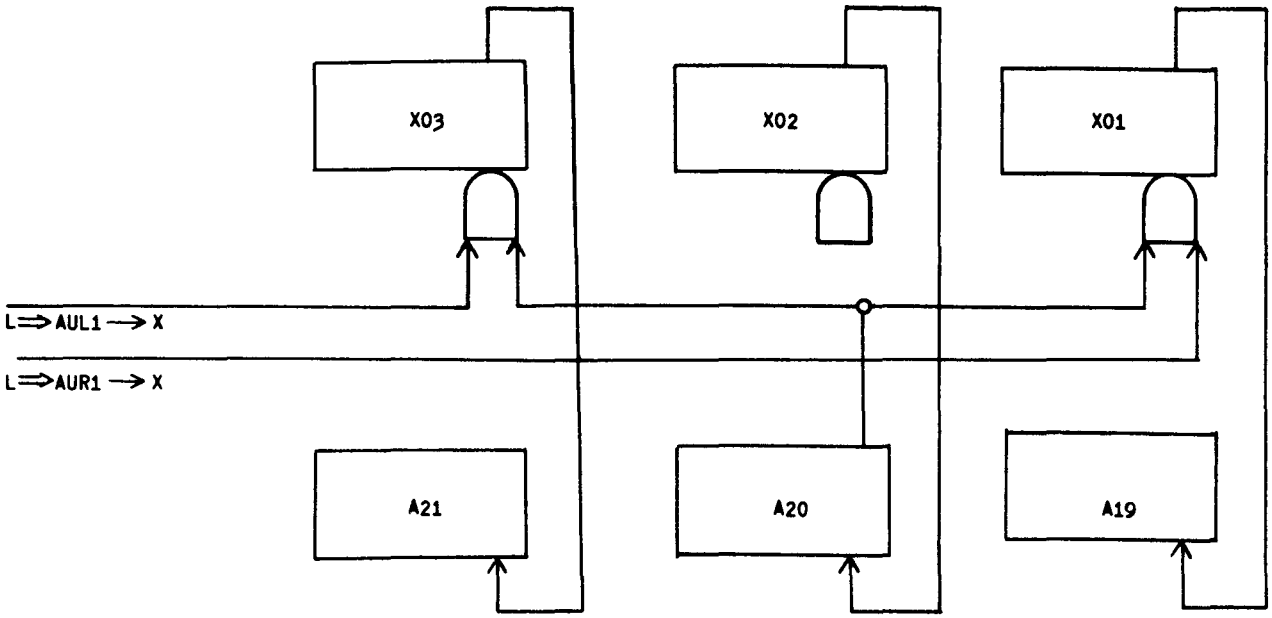


Figure 4-24. AU Register to X Register Shift Transfer

During maintenance and troubleshooting procedures, the operator may manually insert quantities into the AU register by pressing the pushbutton indicator associated with the corresponding bit position.

2. AL REGISTER. - The AL register (figures 9-99 and 9-100) is composed of 18 flip-flop circuits and contains the lower 18 bits of the A register. The AL register performs the following functions:

1) Stores augend prior to an 18-bit add operation and the sum after addition.

2) Stores minuend prior to an 18-bit subtract operation and the difference after subtraction.

3) Stores least significant 18 bits of the augend prior to a 36-bit add operation and the least significant 18 bits of the sum after addition.

4) Stores least significant 18 bits of the minuend prior to a 36-bit subtract operation and the least significant 18 bits of the difference after subtraction.

5) Stores multiplier prior to a multiply operation and the least significant 18 bits of the product after multiplication.

6) Stores least significant 18 bits of the dividend prior to a divide operation and the quotient after division.

7) Stores word to be modified during the execution of various logical instructions.

8) Stores word to be shifted during single-word (18-bit) shift instructions and the least significant 18 bits of the word to be shifted during double-word (36-bit) shift instructions.

9) Has shifting properties when used in conjunction with the W register.

Inputs to the AL register are from the W register during shift operations, and from the adder during other arithmetic operations. Both inputs are direct bit-position transfers, in that the input bits are transferred to the corresponding bit position in AL. Input is controlled by the two command enables L ⟹ W ⟶ AL and L ⟹ ADDER ⟶ AL. One additional input is supplied to bit position 2^0 to perform the end-around-borrow during those instructions requiring a subtraction operation.

Outputs from the AL register are routed to the W register and the arithmetic selector. Output to the W register is to one of the two adjacent bit positions during shift operations. Figure 4-25 is a simplified diagram of these transfers and command enables under which they are executed. Output to the arithmetic selector is a direct transfer of bits in the AL register to the corresponding bits in the arithmetic selector.

Additional outputs from the AL register are:

1) Bit 2^0 to the multiplier store flip-flop during a multiply instruction. If this bit is a logical one, the multiplier store flip-flop will be set to indicate that an addition operation is required.

2) Bit 2^{17} to the control designator circuit during a round AU instruction to establish the bit contents of AU bit 2^0.

3) The sign bit of AL to the jump control circuitry to establish validity of certain jump instructions such as jump if AL neg.

4) A composite output from the AL register to the comparison designators to determine if the contents of AL are equal to zero.

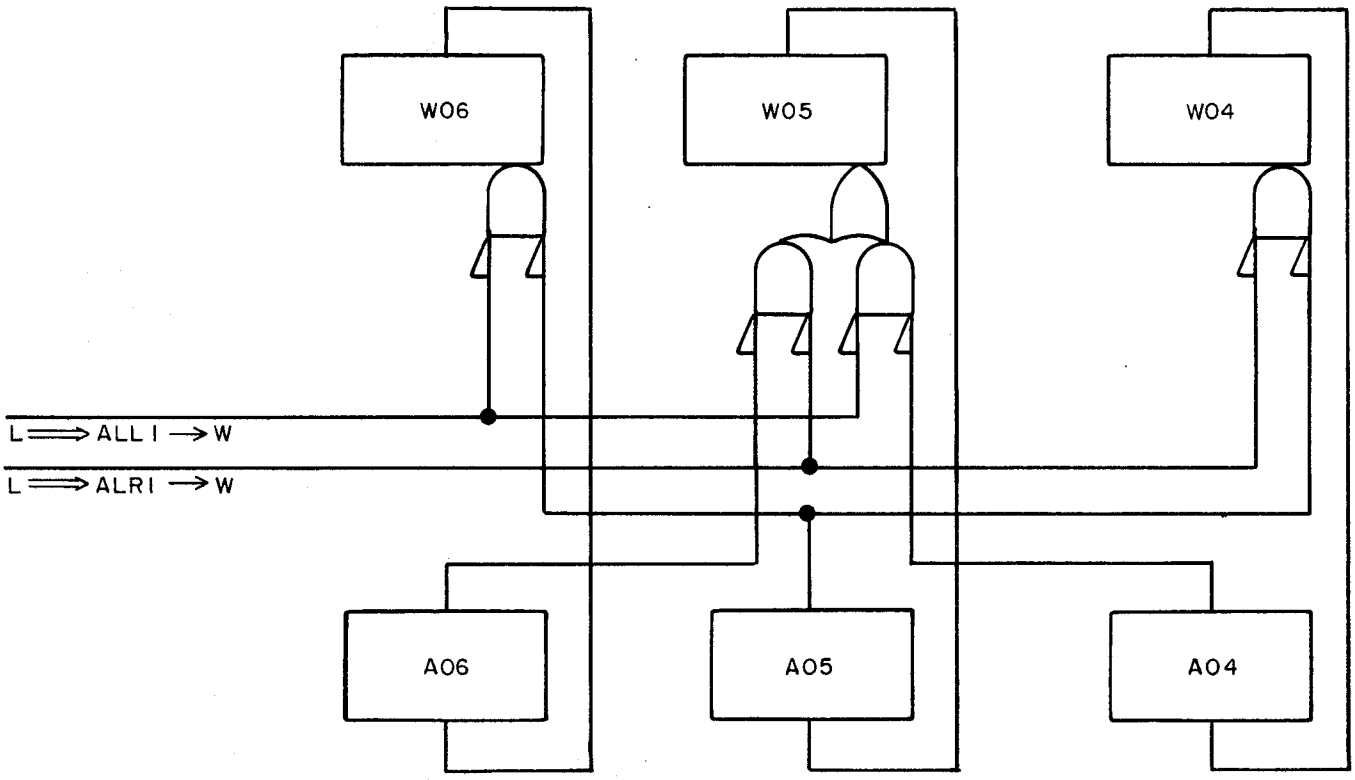


Figure 4-25. AL Register to W Register Shift Transfer

5) Bit 2^{17} to the shift control circuit during shifting operations.

The operator may manually insert quantities into the AL register during maintenance and troubleshooting procedures by pressing the pushbutton indicator associated with the corresponding bit position.

3. A REGISTER. - A register, composed of AU and AL registers, provides 36-bit word capabilities during the following operations:

1) Stores augend prior to a 36-bit add operation and the sum at the completion of the addition.

2) Stores minuend prior to a 36-bit subtract operation and the difference after subtraction.

3) Stores 36-bit dividend prior to a divide operation and the 18-bit quotient in AL and the 18-bit remainder in AU after division.

4) Stores product after a multiplication operation. AL stores the multiplier prior to the multiply.

5) Stores quantity to be shifted during shift operations in which more than 18 bits are involved.

6) Has shifting and complementing properties when used in conjunction with the other logic circuits in the arithmetic section.

Inputs to and outputs from the A register are a combination of inputs and outputs associated with AU and AL. All transfers either to or from the A register require two separate and distinct operations. One operation will either load or transfer the contents of AL; the other will either load or transfer the contents of AU.

4. D REGISTER. - D register (figures 9-85 and 9-86) is composed of 18 flip-flop circuits. Some of the functions performed by this register are as follows:

1) Stores multiplicand during a multiply operation.

2) Stores divisor during a divide operation.

3) Stores lower 12 bits of the P register in bit-positions 00 through 11 for incrementing to provide sequential addressing of memory locations.

4) Stores either the upper four bits of the P register or the contents of the SR register in bit-positions 12 through 15 depending upon the active status of the SR register.

Inputs to D register are from P register, SR register, and the arithmetic selector and are gated into D register by the command enables from D register control circuit.

If bit 2^3 of SR register is set, indicating that the SR register is active, the upper four bits of the addressed memory location are gated into the D register by the L $\Longrightarrow$ SR + SET $\longrightarrow$ D command enable. If the SR register is not active, the upper four bits are supplied by the current contents of the P register.

During certain arithmetic operations, either the contents or the complement of the contents of the arithmetic selector are gated into the D register.

Outputs from D register are applied to the adder to be compared with output from the X register.

5. W REGISTER. - W register (figures 9-89 and 9-90) is an 18-bit register used only with the AL register during shifting operations. The command enables L ⟹ ALR1 ⟶ W and L ⟹ ALL1 ⟶ W are shown in figure 4-25 and the transfer paths are from a given bit in AL to one of the adjacent bit positions in W.

Outputs from W register are routed directly to the corresponding bit in AL. One additional output, bit 2^0, is routed to the complement and shift control circuit to set $AL2^0$ during certain EAB operations.

The W register is nonaddressable and the contents of this register are not visually displayed on the front panel.

6. X REGISTER. - The X register (figures 9-87 and 9-88) is composed of 18 flip-flop circuits to receive and temporarily store information from either the AU register or the arithmetic selector.

When performing in conjunction with the AU register, the X register provides the shifting capabilities of AU. Figure 4-24 illustrates the transfer of data between the X register and the AU register. For example, during a right shift operation, a bit in A20 will be transferred to X01 by the L ⟹ AUR1 ⟶ X command enable and then to A19 by the L ⟹ X ⟶ AU.

Data transfer from the arithmetic selector to the X register, controlled by the L ⟹ SELECT ⟶ X and L ⟹ SELECT ⟶ X command enables, is a direct-bit transfer allowing either the contents or the complement of the contents of the arithmetic selector to be entered into X.

Outputs from the X register are applied to the AU register during shifting sequences as stated above, and to the adder and adder-borrow enable generation circuits. The outputs applied to the latter two circuits are both the contents and complement of the contents of the X register.

The X register is nonaddressable and contents of this register are not visually displayed on the front panel.

(b) ARITHMETIC SELECTOR. - The arithmetic selector (figures 9-82, 9-83, and 9-84) consists of 18 gating circuits corresponding to the normal 18-bit transfers within computer logic. The arithmetic selector provides the signal distribution network for the arithmetic section by using command enables to gate one of five inputs for distribution to four logic circuits.

1. INPUTS. - The AU register, AL register, P register, and Z register provide 18-bit word inputs to the arithmetic selector. Either the SR, ICR, or K register provides a six-bit word input to stages 00 through 05. When this input is used, zeros are applied to stages 06 through 17. The output is then determined by the application of one of five command enables from the arithmetic selector control.

2. OUTPUTS. - Each of the 18 stages has seven outputs which are applied to four circuits. Two outputs are applied to Z register, D register, and parity circuit. One output is identical in bit content to the gated input. The other output is the complement of the gated input word. These two outputs are commonly called select and $\overline{\text{select}}$ (not select). One select output is also applied to store select circuit in the control section.

The arithmetic selector performs the following functions:

1) Gates u portion of an instruction or operand to the D register following the read portion of a memory cycle.

2) Gates operand from the arithmetic section to the Z register for storage during the write portion of a memory cycle.

3) Gates contents of the P register to the arithmetic section to form the next memory address to be used.

4) Gates SR, ICR, or K register contents into the arithmetic section prior to storage in memory.

5) Gates addend from the AL register to the X register during an add AL or subtract AL instruction.

6) Gates augend from the Z register to the D register during an add AL or subtrace AL instruction.

7) Gates lower 18 bits of the addend from AL register to X register and the upper 18 bits of the addend from AU register to X register during an add or subtract A instruction.

8) Gates lower 18 bits of the augend from Z register to D register and then gates the upper 18 bits of the augend from Z register to D register during an add or subtract A instruction.

9) Produces the logical product of AL and (Y) by gating the contents of AL register and the contents of memory location Y, via the AU register, through the select circuitry simultaneously and sets the appropriate comparison designator.

The arithmetic selector contains no flip-flop circuits and its contents are not visually displayed on the front panel.

Figure 4-26 illustrates a typical stage of the arithmetic selector. Inputs to this stage are actually the complement of the bits in the AU, AL, Z select, and P registers. The appropriate output, select or $\overline{\text{select}}$, will then provide the necessary transfer of information to the other computer blocks. Throughout the text of this manual, inputs shall be referred to as direct bit transfers from the appropriate register.

(c) ADDER. - The adder in the block diagram (figure 4-23) consists of the adder-borrow enable generator, figures 9-91, 9-92, and 9-93; and the adder group, figures 9-94, 9-95, and 9-96. Composed primarily of AND gates, the adder performs the following functions:

1) During an increment P subsequence, the adder provides the updated address to P register. Initially, contents of the P register are transferred to the D register where a subtractive addition to the contents of the X register, cleared to zero, is made. The end-around-borrow is inhibited and the result, appearing as the output from the adder, is transferred to P register as the next sequential memory address.

2) During a decrement P subsequence, end-around-borrow is not inhibited and the resulting output from the adder is the same as the original contents of the P register. Thus, the same instruction, normally a 50:57 instruction, will be repeated until a resume is received from the peripheral device.

3) The adder contains the combination of the contents of the X and D registers during all computer operations.

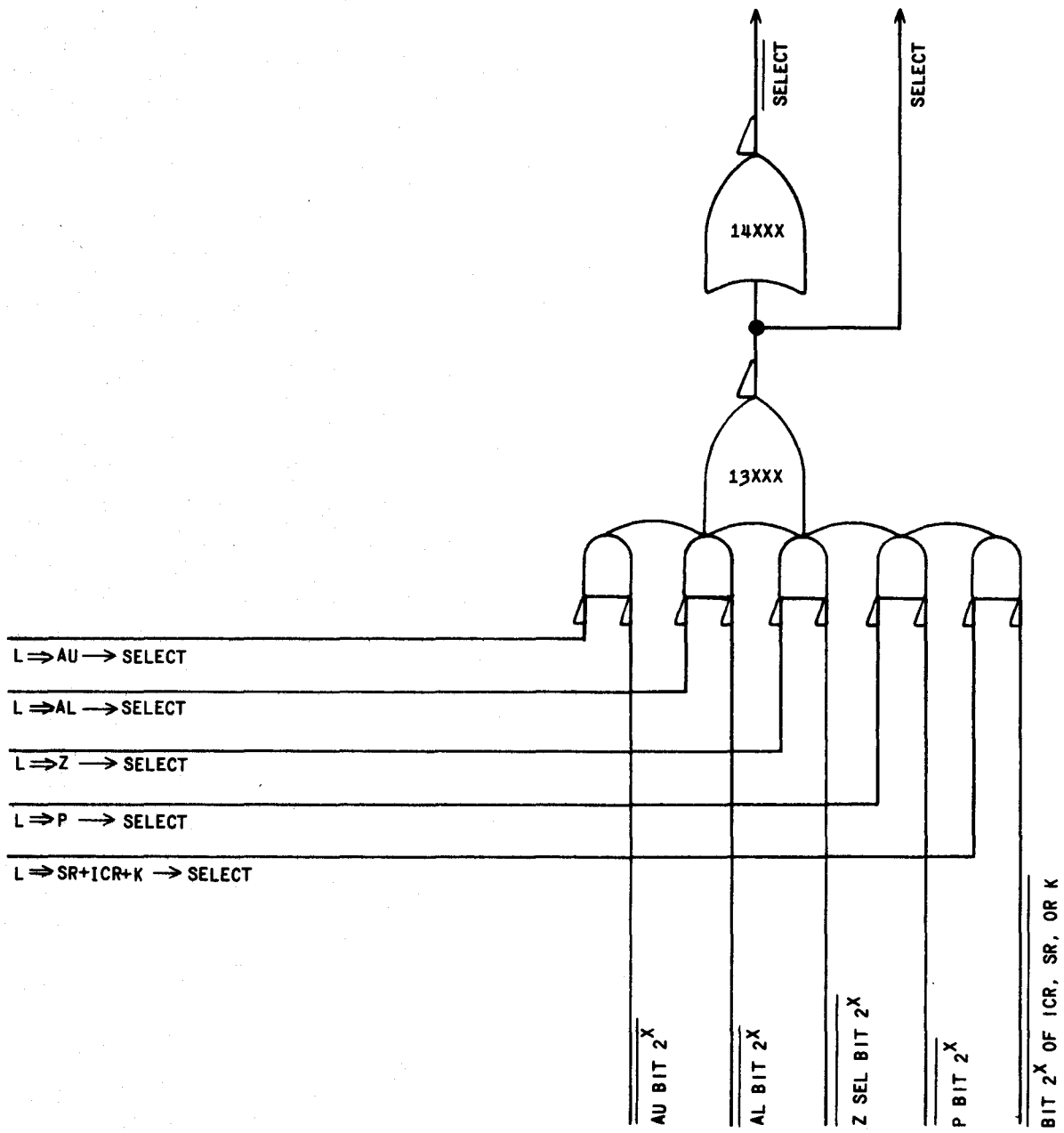


Figure 4-26. Typical Stage of Arithmetic Selector, Simplified Diagram

The adder contains no flip-flop circuits and its contents are not visually displayed on the front panel.

Because the adder in the 1219B computer translates for borrows rather than carries, it is considered to be a subtractive adder.

Operation of the adder is the same for both addition and subtraction. Because multiplication is a series of addition operations and division is a series of subtraction operations, the computer can perform all arithmetic functions in a single method.

The adder consists of three unique sections; the half-subtractor, the borrow generator, and the full-subtractor. Each section contains 18 stages to provide for 18-bit, word-handling capability.

The half-subtract section of the adder consists of the 10A-- and 11A-- adder stages.

The borrow generator consists of the 12A-- and 13A-- stages and the borrow enable generator (figures 9-91, 9-92, and 9-93).

The full-subtractor consists of the 14A-- stages.

1. HALF-SUBTRACTOR. - Figure 4-27 illustrates a single stage of the half-subtractor. Each stage compares contents of the X register to contents of the D register. This bit-by-bit comparison is accomplished in the 10A-- circuit. If the compared bits are the same, output of the 10A-- circuit will be a high (zero); if they are opposite, this output will be a low (one). Therefore, this output is a half-subtract result with no regard for borrows. Output of the 11A-- circuit is an inversion of the half-subtract result. In the half-subtract process, if a given stage of X and D both contain a zero, a borrow will be generated. This borrow may be satisfied only if a given stage of X and D both contain a one.

Example:

2^{17}				2^2	2^1	2^0	
0	0	-	-	1	0	1	X REGISTER CONTENTS
0	1	-	-	1	0	0	D REGISTER CONTENTS
0	1	-	-	0	0	1	HALF-SUBTRACT RESULT

2. BORROW GENERATOR. - Figure 4-28 illustrates, in simplified form, a single stage of the borrow generator. Conditions which require a borrow are when both X and D are equal to zero.

The computer adder has a propagation time of 200 nanoseconds. To achieve this speed, a network to increase the speed of the propagation of borrows is necessary. This network is the adder-borrow enable generator, hereinafter called the borrow generator.

Borrows are propagated through a maximum of two-bit positions within the adder. The borrow generator is divided into three sections, each of which contains two 3-bit subsections. If a borrow is generated in bit position 2^0, it is propagated through bit positions 2^1 and 2^2. If it is not satisfied in either of these two positions, it is then routed to the borrow generator to be gated into the first succeeding subsection which can satisfy the borrow.

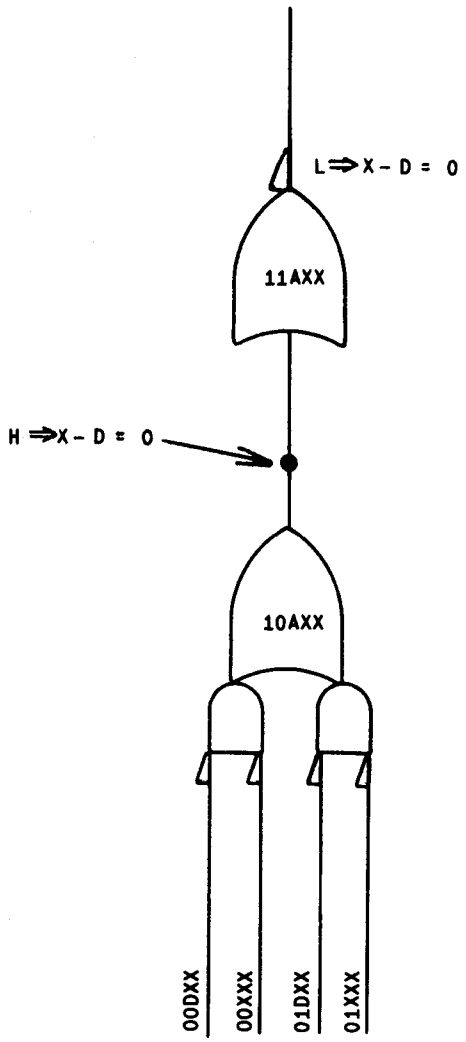
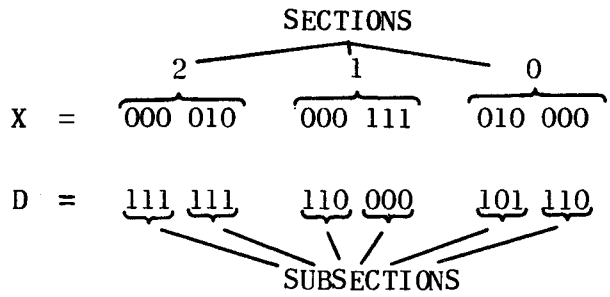


Figure 4-27. Single Stage of Half-Subtractor

Example:



As shown in the example, a borrow is generated in bit position 2^0. This borrow is propagated through bit positions 2^1 and 2^2 and cannot be satisfied. It is then reverted to the borrow generator which determines that the borrow cannot be satisfied in the subsection consisting of bits 2^3-2^5. Section one cannot satisfy the borrow; therefore, the borrow generator will insert the borrow in the subsection consisting of bits 2^{12}-2^{14} to be satisfied at bit position 2^{13}. The number of logic elements through which the borrow must be propagated is therefore reduced and the speed of the adder is increased.

3. FULL-SUBTRACTOR. - The borrow generator also gates the above generated borrow into all bit positions (to bit 2^{13}) to correct the outputs. This is accomplished in the 14A-- stages of the adder. At this point, the full-subtractor completes the operation of the adder. The 14A-- stages comprise the full-subtractor and produce the adder output.

(3) OPERATION.

(a) ARITHMETIC OPERATION. - All arithmetic operations are executed through the use of a one's complement, subtractive arithmetic system. Four arithmetic operations; addition, subtraction, multiplication, and division are performed following the rules of signed arithmetic. Multiply and divide operations have been reduced to a series of additions and subtractions and are executed as such through the computer logic.

The word format for the arithmetic operands consists of 17-word or data bits, bits 2^0 through 2^{16}, and one bit to indicate whether the quantity is positive or negative, bit 2^{17}. It is evident that the computer is capable of manipulating values within the range of $\pm 2^{16}$ or $\pm 131,071$.

Under certain conditions, the AL and AU registers may be combined into a single A register to provide increased number-handling capabilities. These conditions are encountered when performing double-length operations such as 36-bit additions and subtractions. In these cases, the numerical value of the numbers which may be handled is increased to $\pm 2^{34}$.

1. ADDITION. - The computer executes an addition by logically adding the contents of two flip-flop registers; one containing the addend and the other containing the augend. The sum after an 18-bit operation is stored in the AL register and, after a 36-bit operation in the A register.

In an 18-bit operation, the addend is initially placed in the AL register prior to add instruction. The augend is then read from addressed memory location and placed in the Z register. Contents of the AL register are then placed in the X register through the arithmetic selector. The augend is transferred through the arithmetic

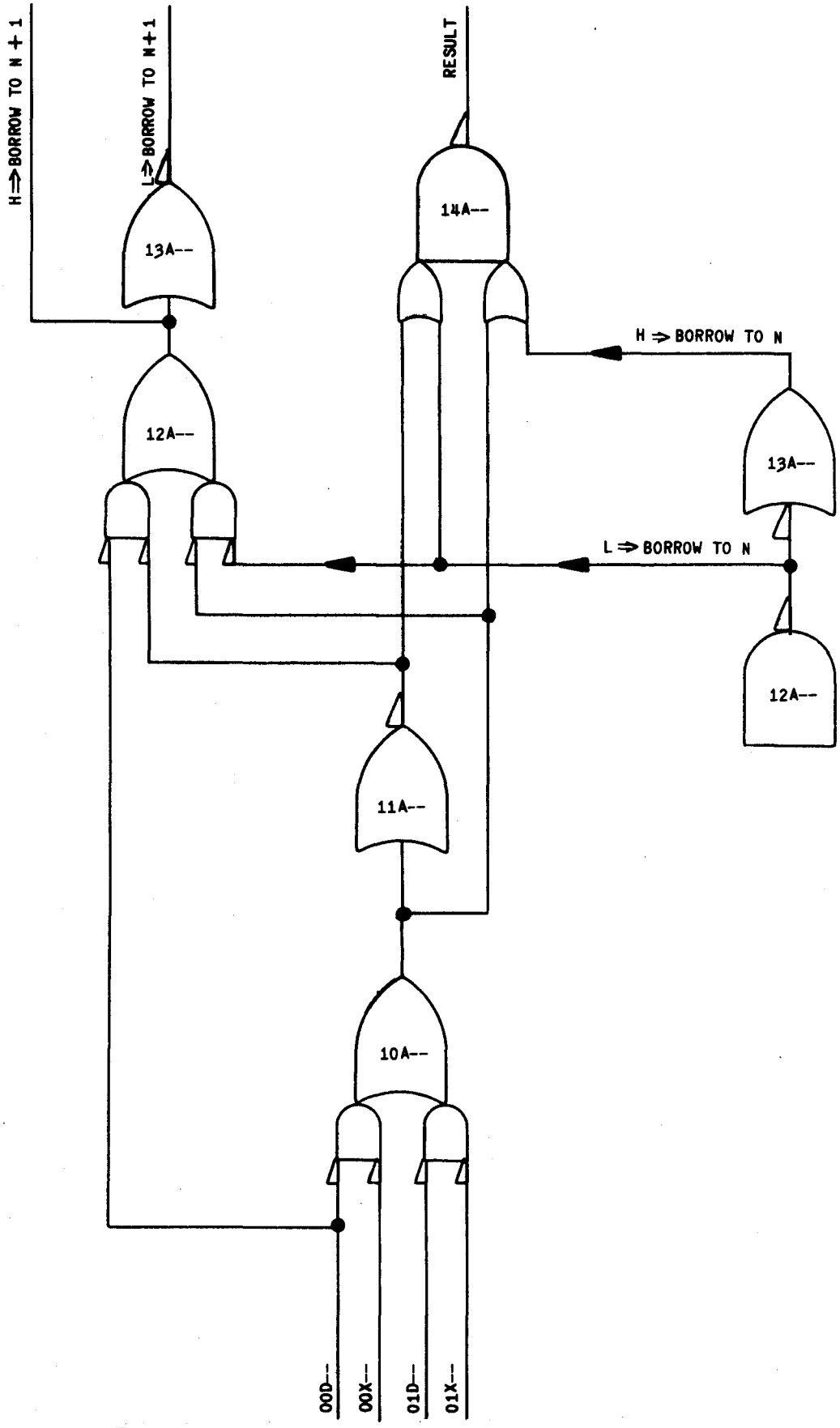


Figure 4-28. Single Stage of Borrow Generator

selector to the D register. The sum, appearing as the arithmetic result in the adder, is then transferred to the AL register for further operations. The ADD instruction, involving 18-bit operands, is executed in four microseconds with or without B modification.

In a 36-bit add operation (f=20,21) the 36-bit augend is initially placed in the A register. The addend, composed of two 18-bit words, is stored in two adjacent memory locations; the least significant 18-bits are stored in address Y and the most significant 18-bits are stored in address Y+1. Address Y must be an even numbered address.

During arithmetic operation, the contents of address Y are added to the 18-bits previously stored in the AL register with the result appearing in the AL register. A second R sequence (R2) is initiated to read the contents of Y+1 from memory and add these 18-bits to the 18-bits appearing in the AU register. The sum is then placed in the AU register and includes any carry that may have developed from the first add sequence. Add or subtract A instruction requires 6 microseconds for execution.

Single- and double-length add instructions are illustrated in figure 4-29 in flow chart format. During the single-length (18-bit) add instructions (f = 14, 15), the second pass is not required and the instruction is terminated after the ADDER $\longrightarrow$ AL operation. In the double-length (36-bit) add instructions (f = 20, 21), the second pass will read the contents of memory address Y+1 for the most significant 18 bits of the augend.

2. SUBTRACTION. - Subtraction sequence follows the same pattern as addition sequence with one exception. The 18-bits transferred to the arithmetic selector from Z register are complemented during transfer to the D register. Complement of the minuend is then added to the subtrahend to produce the arithmetic difference which is then stored in the AL register. The flow chart (figure 4-30) illustrates the execution of the 18-bit subtract instructions (f = 16, 17) and the 36-bit subtract instructions (f = 22, 23). The actual command sequencing is contained in the command timing tables in paragraph 4-7.

3. MULTIPLICATION. - During multiply instruction (f = 24, 25), the contents of an addressed memory location are multiplied by the contents of the AL register. Upon completion of the execution of the multiply instruction, the product is contained in A register with the least significant bits in AL register.

During the multiply operation, each bit of the multiplier is systematically examined by the computer. When a binary one is detected, the multiplicand is added to the partial product, raised to the appropriate power of two. As each bit is examined, the contents of the A register are right shifted one place and the contents of the K register are decremented by one. This operation is repeated for each of the 18 bits of the multiplier. Although there are just 18 bits in the multiplier, an additional shift is required to shift the entire final answer into the A register. Thus, the K register is set to contain 19_{10} and controls the number of shift operations.

Initially, the signs of the numbers to be multiplied are examined and stored and both quantities are converted to absolute positive values. The multiplier is placed in AL register, the multiplicand is placed in D register, AU and X registers are cleared to zero, and a count of 19_{10} is placed in K register. The decrement K, shift A, test AL bit 0, and conditional-add cycle is initiated and repeated until the contents of K register are equal to zero, thus examining each bit of the multiplier. At the completion of the operation, A register will contain the bits of the

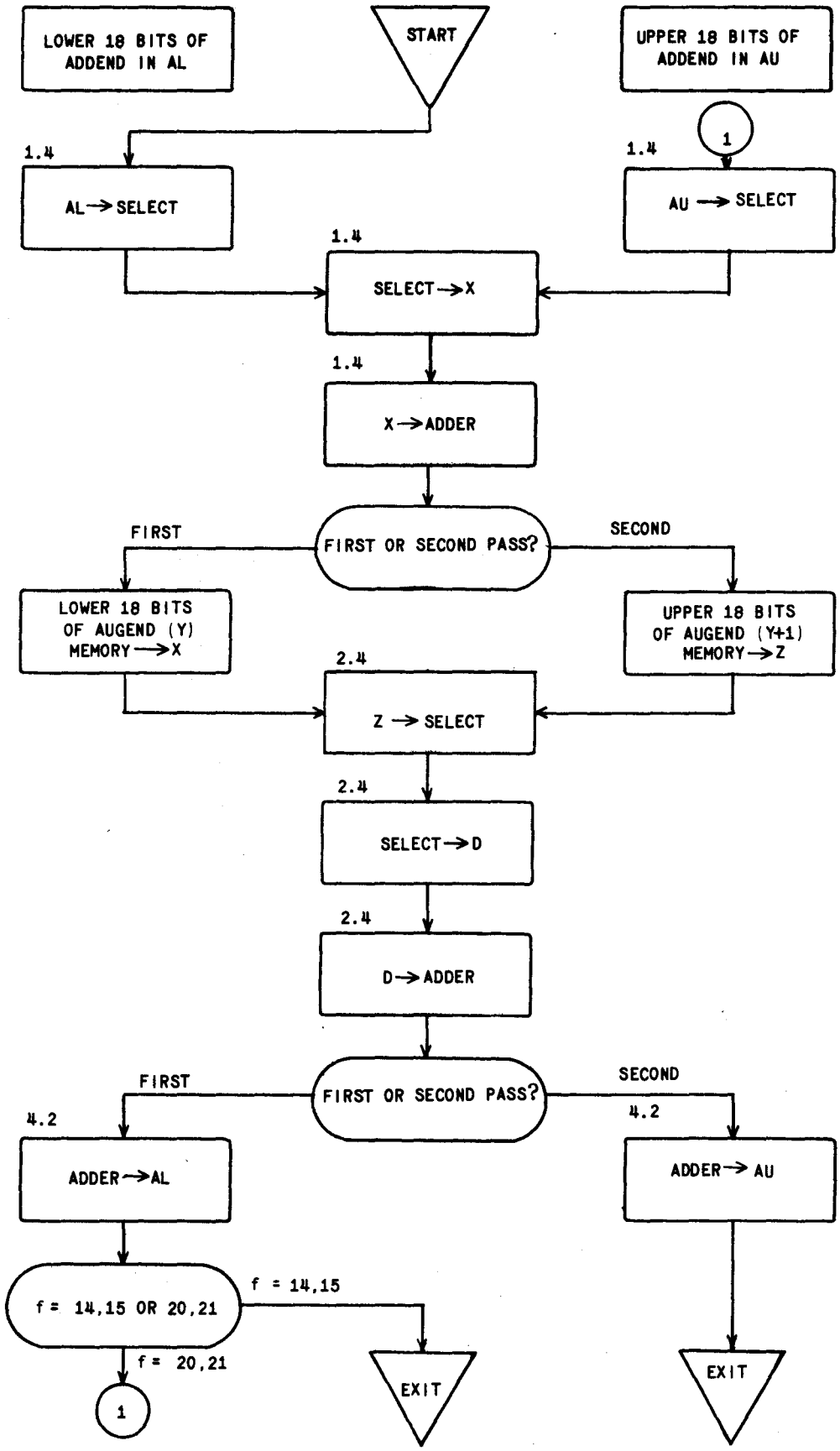


Figure 4-29. Add Instruction

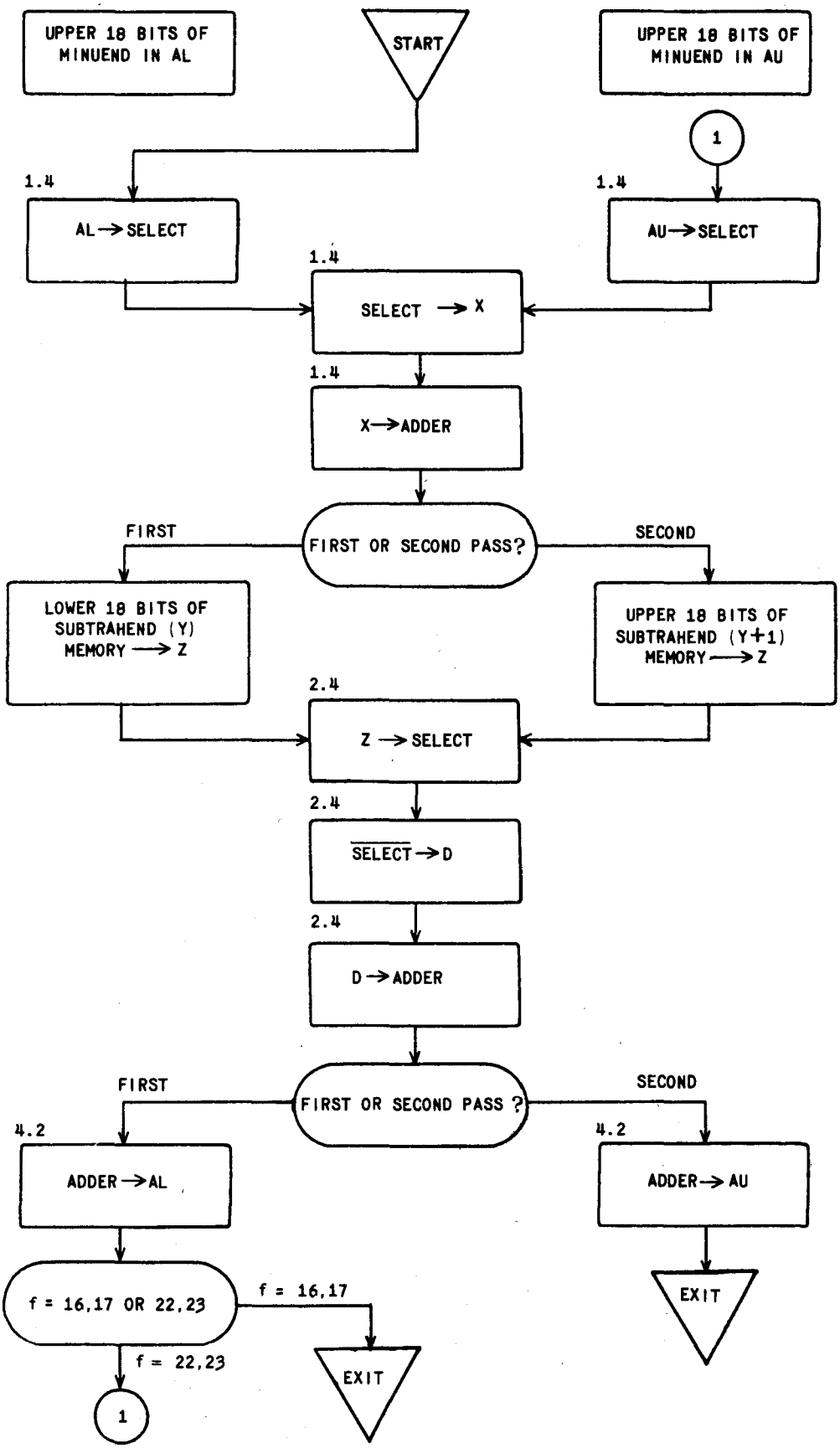


Figure 4-30. Subtract Instruction

product. If the product should be negative, as determined by stored signs of the quantities involved, the contents of A register are complemented and replaced in A register.

The significant portion of the multiply instruction begins with setting of the K register to 19_{10} at 2.1 time of R sequence. At 2.2 time, K1 register is cleared. Contents of K0 minus 1 are transferred to K1 register at 2.3 time; at the same time, X and W registers are cleared to zero. Contents of the AU register are right-shifted one place and routed to X register and contents of the AL register are right-shifted one place and routed to W register at 2.4 time. At 3.1 time, contents of the K1 register are transferred to the K0 register and the AU and AL registers are cleared to zero. At 3.2 time, contents of the X and W registers are transferred back to AU and AL registers. At 3.4 time, bit 2^0 of the AL register is examined to determine whether the conditional-add cycle is required. If the bit is a logical one, the multiplier store flip-flop is set to indicate that on the next pass through the sequence, contents of the adder will be transferred to the AU register at 3.2 time, replacing the transfer of the contents of the X to AU register.

This sequence is repeated until contents of the K1 register are equal to zero.

The multiply sequence (figure 4-31) is shown in flow chart format.

4. DIVISION. - During divide instruction (f = 26, 27) contents of the A register, the 36-bit dividend, are divided by contents of a specified memory address, the 18-bit divisor. Upon completion of the sequence, the 18-bit quotient is contained in AL register and the remainder, if any, is contained in AU register.

The computer performs the division process by systematically attempting to subtract the divisor from the dividend. Each subtraction attempt is followed by a one place left-shift of the contents of A register. K register contents are decremented by one and a test is performed to determine if an end-around-borrow resulted from the trial subtraction. If an end-around-borrow did occur, a logical zero is inserted in the least-significant bit position of AL register through the shift of the contents of the A register. If no end-around-borrow occurred, a logical one is placed in the least-significant bit position of the AL register, contents of the adder are gated into the AU register, and contents of the A register are left-shifted one place. This cycle is repeated 18 times; once for each bit in the divisor.

Initially, signs of the dividend and divisor are examined and stored in the Y neg and A neg flip-flops, the dividend is converted to an absolute positive value, and the divisor, placed in D register, is converted to an absolute negative value. Thus, the shift count of 18_{10} is held in K register, the dividend is held in A register, and the divisor is held in D register. Subtraction of D from A (left shift of A) decrement K, and test for an end-around-borrow cycle is then repeated for each of the 18 bits of the divisor. Upon completion, K register will be cleared, thereby terminating divide sequence. After the first subtract and check for end-around-borrow, providing no end-around borrow exists, OVERFLOW flip-flop is set. This indicates that the value of the quotient will exceed storage capabilities of AL register and the sign bit will be set. After the divide is completed, a test can be made for this condition by use of the 50:52 (skip on overflow) or 50:53 (skip on no overflow) instructions. If overflow does exist, final contents of the AL register will be $\pm$ 0.

At completion of the divide operation, the values of the dividend and the divisor are examined for sign content. The values of the quotient and remainder are then corrected as shown in table 4-9.

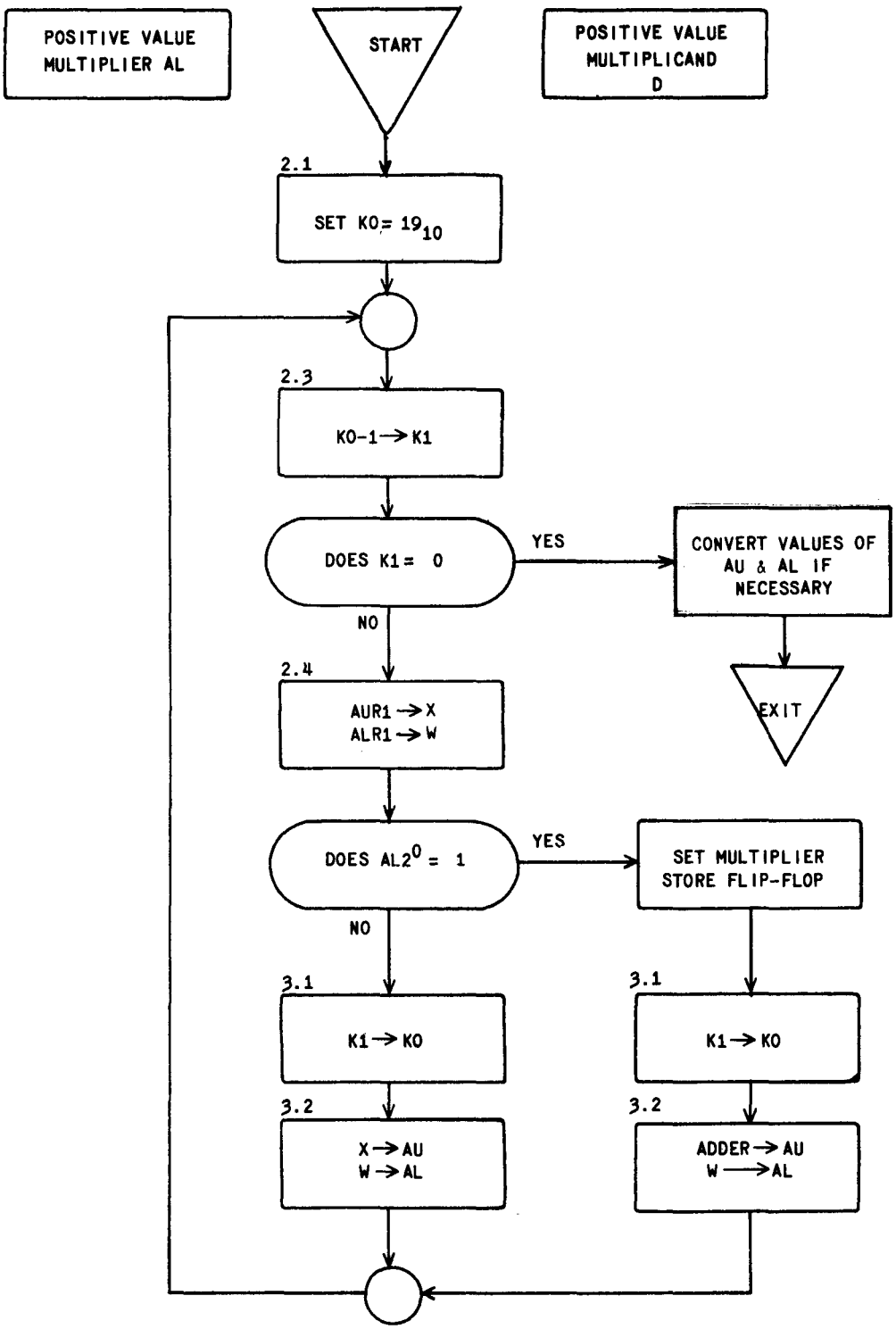


Figure 4-31. Multiply Sequence

TABLE 4-9. DIVIDE SEQUENCE SIGN CORRECTION

DIVIDEND	DIVISOR	QUOTIENT	REMAINDER
Positive	Positive	Positive	Positive
Positive	Negative	Negative	Positive
Negative	Positive	Negative	Negative
Negative	Negative	Positive	Negative

Three conditions affect the result of a divide operation. The first condition exists when the divisor is greater than the dividend. The quotient is then zero and the remainder is equal to the dividend. The second condition exists when the dividend is equal to the divisor. The quotient in this case is equal to one with a remainder of zero. The third condition exists when the dividend is greater than the divisor. In the latter case, the result is a normal quotient and remainder unless the value of the quotient is great enough to propagate a bit into the sign bit, thereby indicating overflow. Divide sequence (figure 4-32) is shown in flow chart format.

(b) SHIFT OPERATIONS. - The computer is capable of performing six shift instructions, which include right and left shifting of AU, AL, and A registers. Shift operations involve the use of both addressable and nonaddressable registers.

During all shift instructions, K register stores and records the number of shift operations, which are to be performed. One of the addressable registers, AU, AL, or A, contains the quantity to be shifted. The nonaddressable registers, X and W, provide addressable registers with the necessary shifting capabilities. The X register is used in conjunction with AU register; W register is used in conjunction with AL register. The X and W registers are combined when used with the A register.

1. SHIFT AU. - Right and left shift AU instructions (f = 50:41 and 50:45) use AU and X registers to accomplish the shift function. Contents of the AU register are transferred to adjacent bit positions in X register and then loaded in a direct bit-for-bit transfer in AU register. In the right-shift operation, the most significant bits in the register are replaced by the original sign bit as the quantity is shifted. In the left-shift operation, the most significant bit of the register contents is shifted in an end-around manner to the least significant bit position. Thus, bits shifted from the least significant bit position during a right shift are lost; whereas, the bits shifted during a left shift are end-around shifted to remain in the register. Figure 4-33 shows the shift pattern for AU register.

The number of shift operations must be specified in the lower six bits of the instruction word and will then be stored in K register. As each shift is performed, contents of K are decremented. When K register contains all zeros, the shift operation is terminated. Commands and functions which perform the shift operations (figure 4-34) are shown in flow chart format.

2. SHIFT AL. - Shift AL instruction (f = 50:42 and 50:46) are provided to shift the contents of AL register a given number of positions to either the right or left. These instructions involve the use of the addressable AL register and the nonaddressable W register. Figure 4-35 illustrates performance of the computer during these instructions. Figure 4-36 illustrates command sequence during a right and left shift of the AL register.

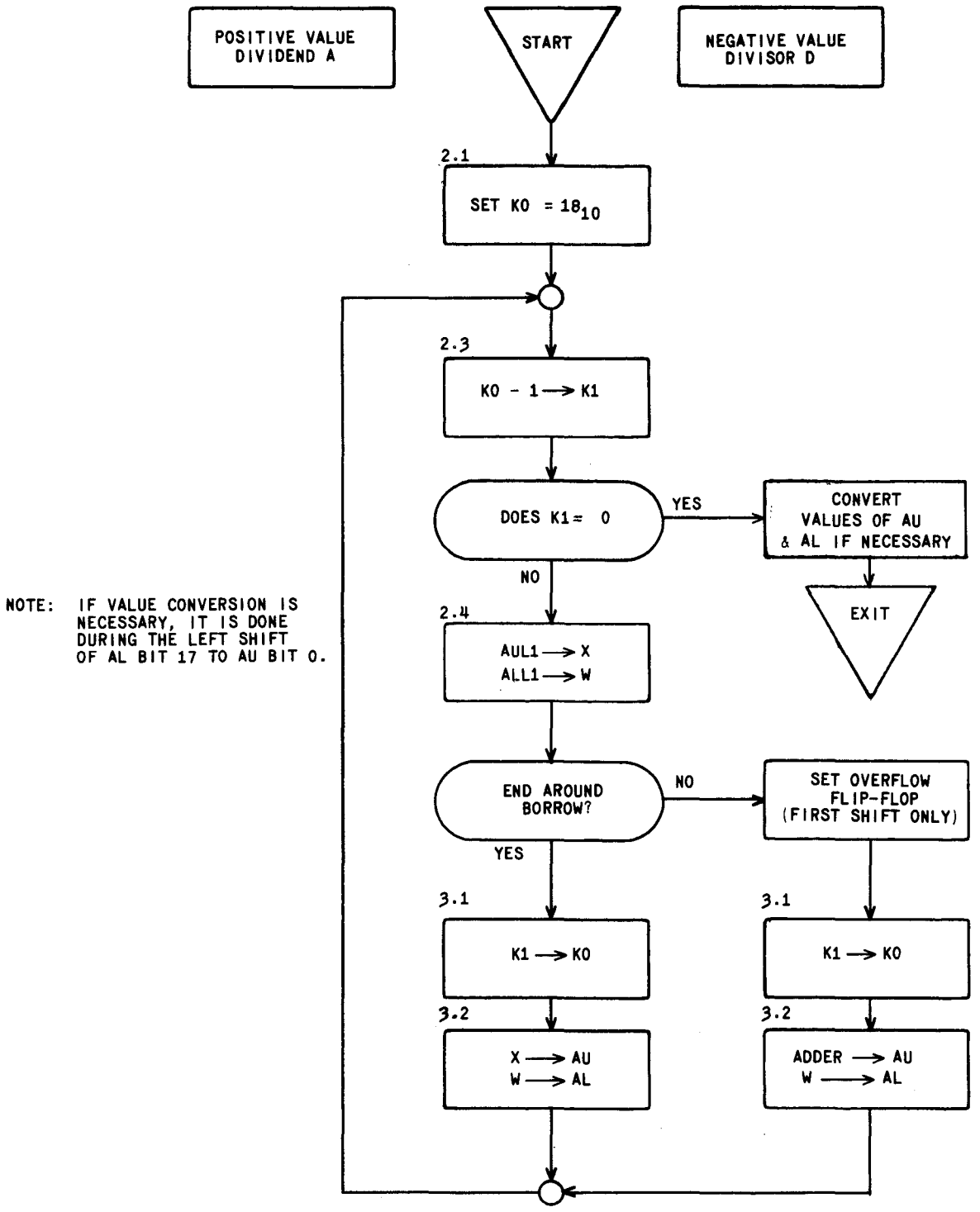


Figure 4-32. Divide Sequence

3. SHIFT A. - During execution of the right shift A or left shift A instruction (f = 50:43 and 50:47), the AU and AL registers are combined to form the 36-bit A register. In the execution of the right shift instruction, the high order bit is replaced by the sign bit and the low order bit is lost for each shift operation. In the execution of the left shift instruction, bits are end-around shifted so that the least-significant bit is replaced by the most-significant bit in each shift operation. Figure 4-37 illustrates the performance of the shift A instructions. The shift commands and their functions (figure 4-38) are shown in flow chart format.

(c) COMPLEMENT. - Complement instructions (f = 50:61, 50:62, and 50:63) involve the process of changing each bit of the given logical word to the opposite value. Each zero is replaced by a one and each one is replaced by a zero. The one exception to this rule is when the quantity to be complemented is a positive zero. In this case, complement operation is inhibited to prevent creating a negative zero. For example, the complement of 1101010 is 0010101; and the complement of 000001 is 111110. The computer has the capability of complementing the contents of AL register (f = 50:61), AU (f = 50:62), and contents of the entire A register (f = 50:63). The complement instructions are executed by setting the X register equal to a negative zero (X = 1's) and placing the quantity to be complemented in the D register. Thus, the resulting output from the adder appears as the complement of the original value.

One additional timing chain output (T52) is developed for complement instructions involving the AL register. The adder contents are transferred to the AL register without requiring the use of the normal timing chain outputs. T52 actually appears at the same time as T12.

Figure 4-39 illustrates the complement AL instruction in flow chart format. Figure 4-40 shows sequencing and function during the execution of the instruction.

Figure 4-41 shows sequencing of the complement AU instruction. Figure 4-42 shows the operation of complementing contents of the entire A register.

(d) SCALE FACTOR. - Scale factor instruction (f = 50:44) is used to normalize contents of the A register to the left, either fully or for a specified count contained in K register. The contents of the A register are shifted circularly to the left until bits A^{34} and A^{35} are not equal, or until the quantity has been shifted a number of places to the left specified by the count in K register. Upon completion of the scale factor operation, value remaining in the K register is stored at address 00017 for future use by the program.

(e) SELECTIVE ALTERATIONS. - The computer program is capable of altering the contents of the AL register in one of several selective methods. These are: selective set, selective clear, selective complement, and selective substitute. A word located at a given memory address, commonly referred to as the mask, must be specified in the selective instruction. Bits of the mask which contain ones indicate the bits of AL upon which the specified operation is to be performed. All other bits of AL remain unaltered.

1. SELECTIVE SET. - Selective set instruction (f = 51) places a one in each of the bit positions of the AL register specified by the position of set bits in the mask.

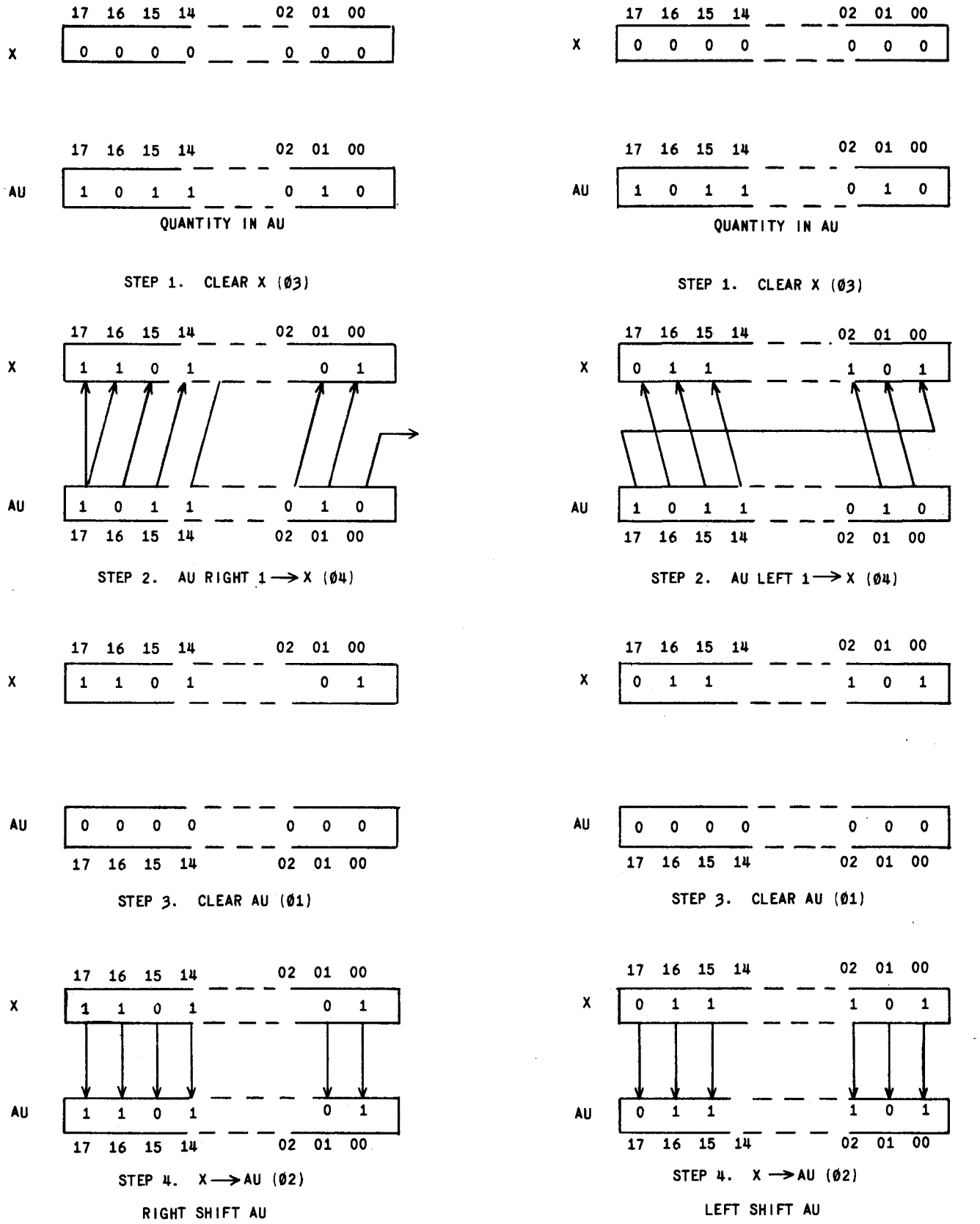


Figure 4-33. Shift Operation Involving the AU Register

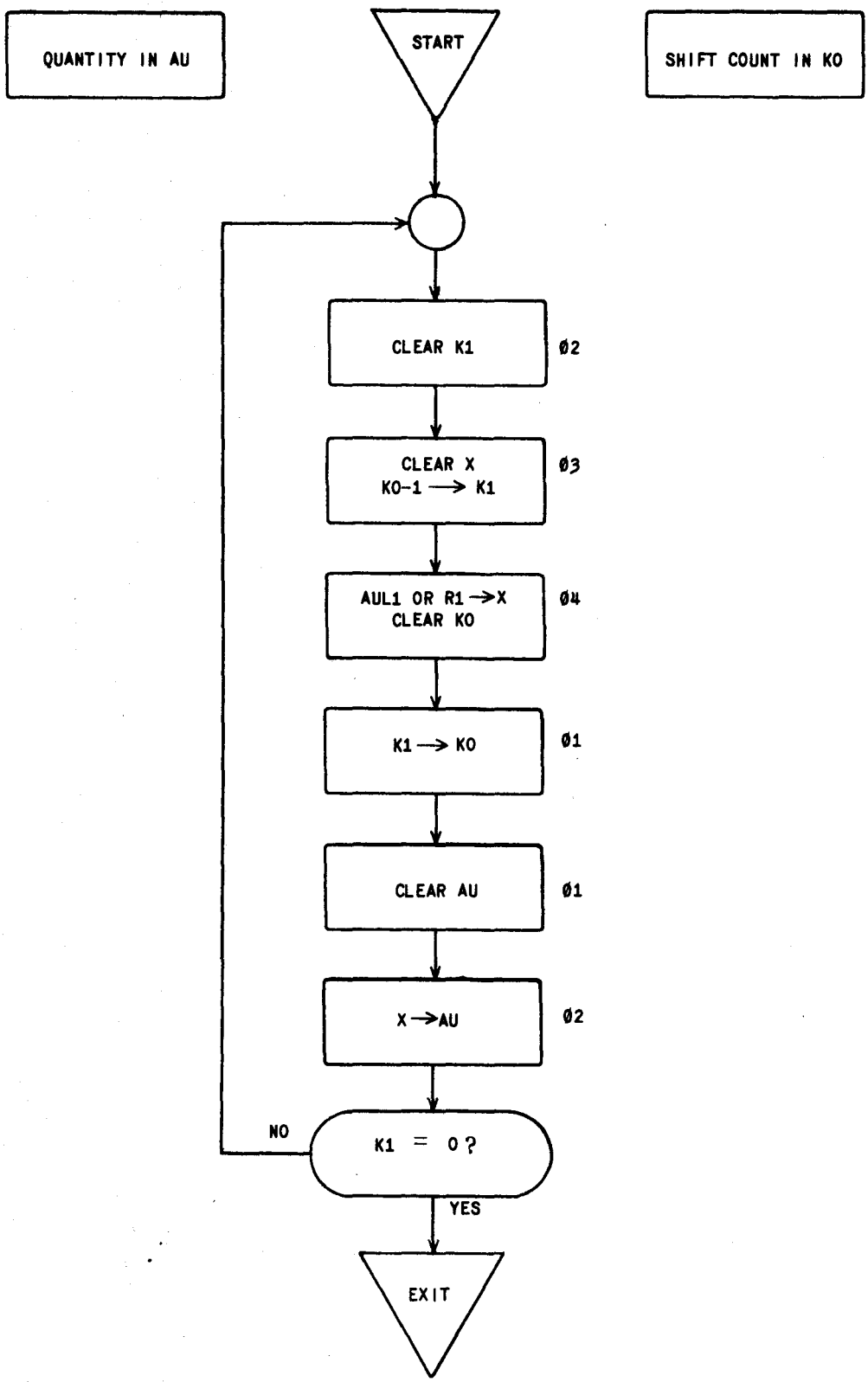


Figure 4-34. Shift Commands and Functions, AU Register

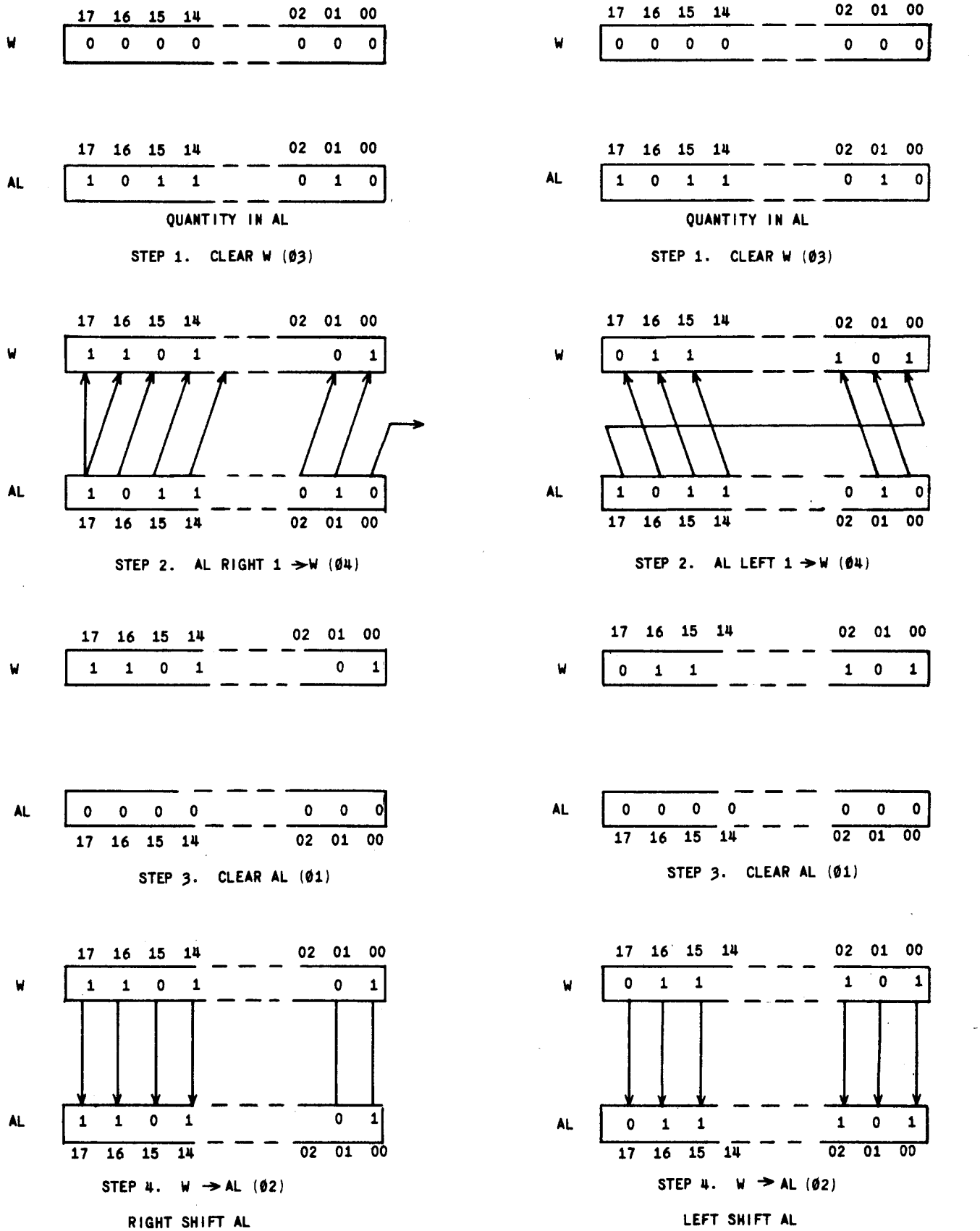


Figure 4-35. Shift Operations Involving the AL Register

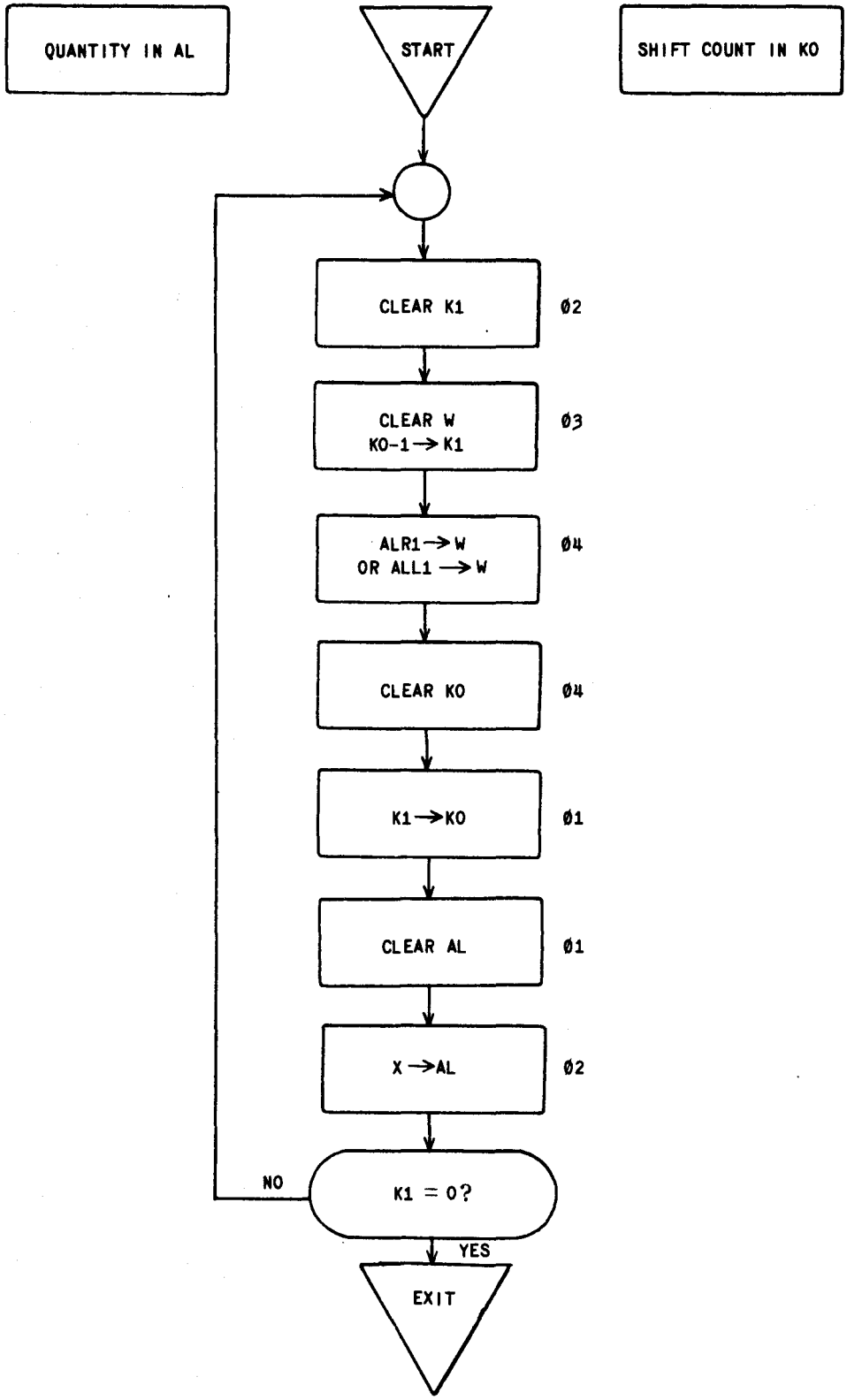
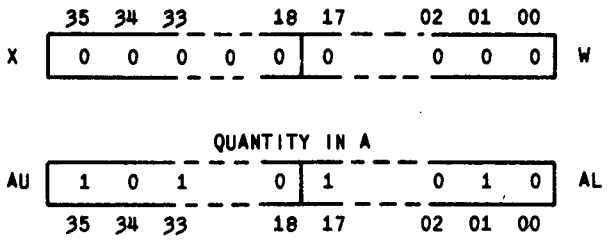
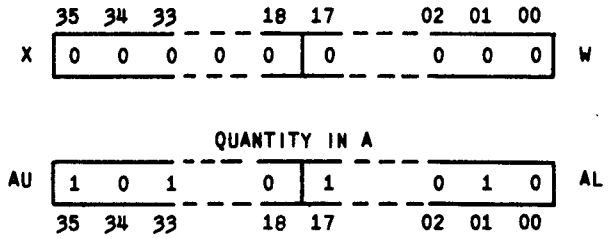


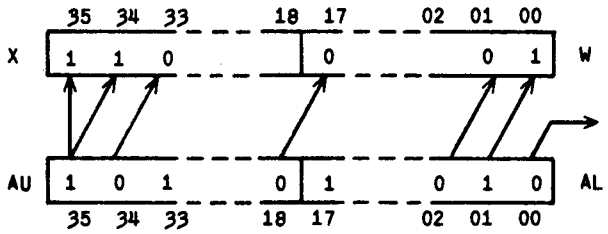
Figure 4-36. Shift Commands and Functions, AL Register



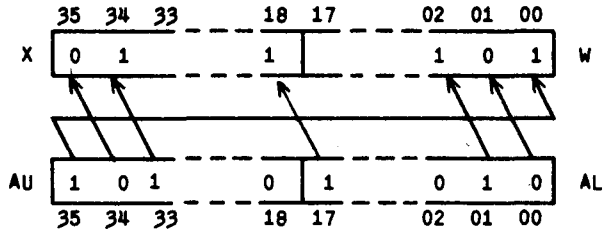
STEP 1. CLEAR X; CLEAR W



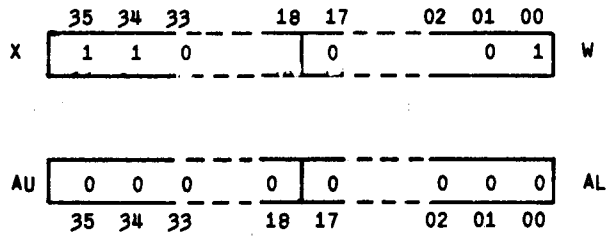
STEP 1. CLEAR X; CLEAR W



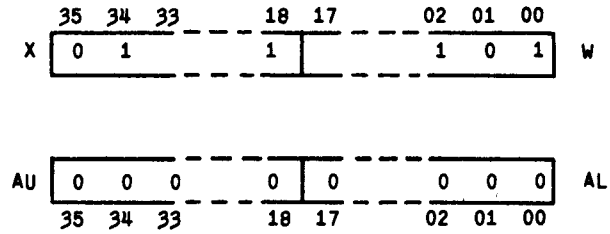
STEP 2. AUR1→X; ALR1→W



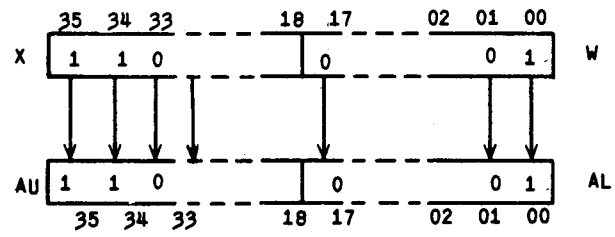
STEP 2. AUL1→X; ALL1→W



STEP 3. CLEAR AU; CLEAR AL

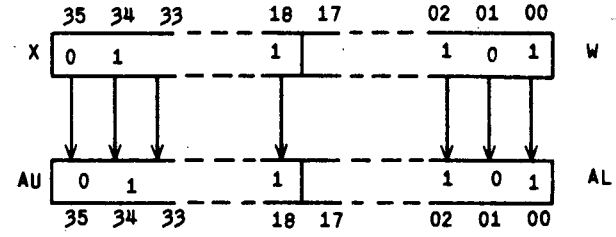


STEP 3. CLEAR AU; CLEAR AL



STEP 4. X→AU; W→X

a. RIGHT SHIFT A



STEP 4. X→AU; W→X

b. LEFT SHIFT A

Figure 4-37. Shift Operations Involving the A Register

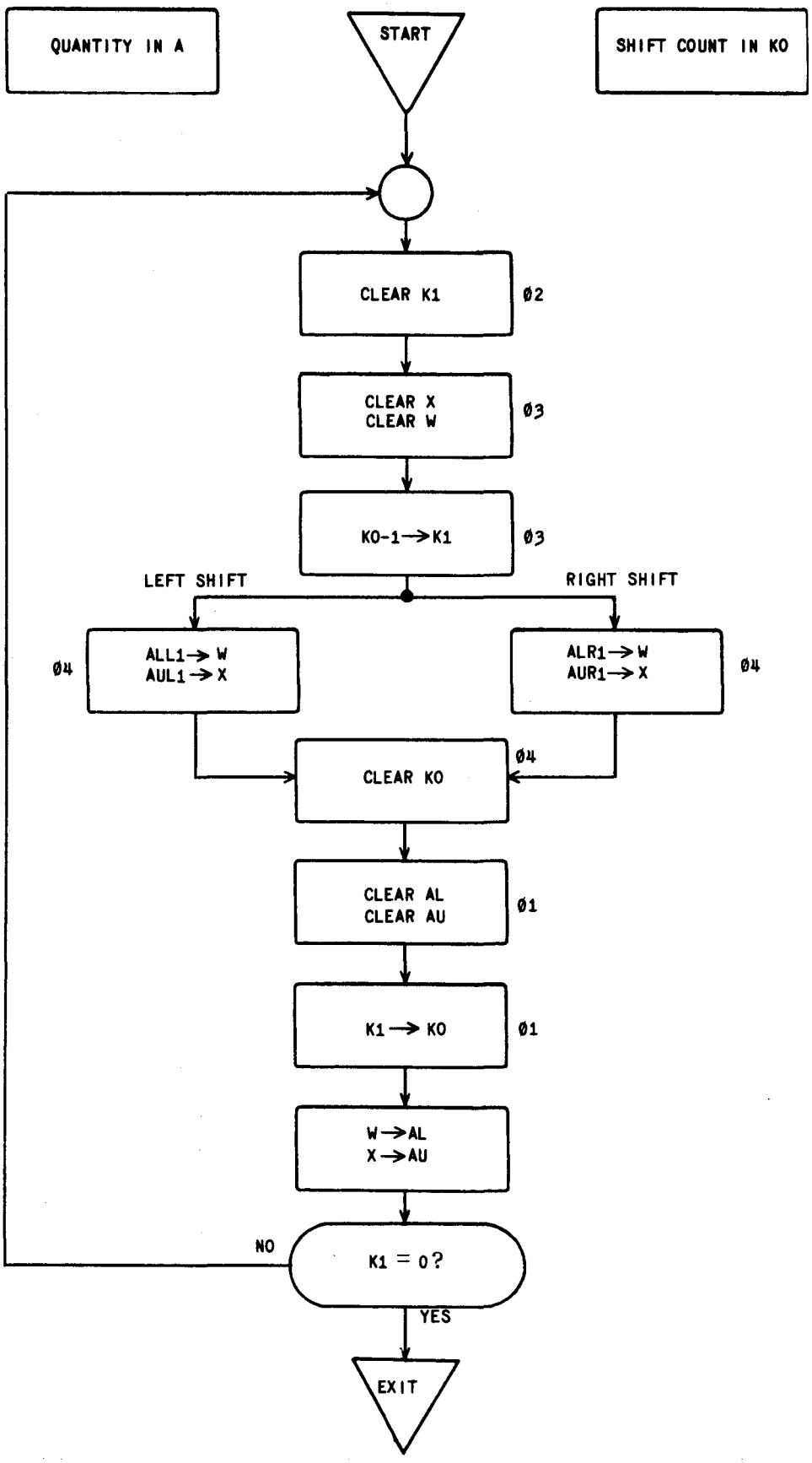


Figure 4-38. Shift Commands and Functions, A Register

2. SELECTIVE CLEAR. - Selective clear instruction (f = 57) places a zero in each of the bit positions of the AL register specified by contents of the mask and; thus, effectively clears these bits.

3. SELECTIVE COMPLEMENT. - Selective complement instruction (f = 53) complements the contents of those bit positions of the AL register as specified by the contents of a given memory location.

4. SELECTIVE SUBSTITUTE. - Selective substitute instruction (f = 04, 05) replaces selected bits of AL with corresponding bits of a memory location specified in the instruction. Location of set bits in AU, bits containing ones, specifies the bits to be substituted by memory. All other bits remain unchanged.

d. MEMORY SECTION

(1) GENERAL. - Memory section of the computer consists of three types: main memory, control memory, and bootstrap memory. The three memories differ in cycle time and storage capacity but all use magnetic cores as storage media. All three memories have random addressing; however, it serves no worthwhile purpose to address bootstrap memory in a program.

To operate a memory, three steps are performed: a discrete address is selected, a read cycle is performed to read the word stored at the selected address, and a write cycle is performed to store a word at the selected address. In the main and control memories, read cycle erases the addressed memory location to zero when the word is read; therefore, the word removed is restored again during the write cycle.

The bootstrap memory is a nondestructive readout memory; a word is not erased during the read cycle, and a word may not be written into this memory.

However, provisions have been incorporated to store two bootstrap programs; that is, load routine for paper tape and load routine for magnetic tape. Selection of the desired routine is controlled by the BOOTSTRAP MODE switch on the front panel of drawer A4. An example of the use of this switch follows:

The paper tape load routine is ordered as an option for bootstrap memory. The computer is then shipped with this pre-wired, non-destruct program in bootstrap memory at addresses 00500 through 00537. With the BOOTSTRAP MODE switch in the NDRO position, any reference to these addresses automatically references the prewired bootstrap program.

By placing the BOOTSTRAP MODE switch in the MAIN MEMORY position, the operator may manually load the magnetic tape load routine in the main memory addresses 00500 through 00537. Placing the switch in the NDRO position then prevents reference to the main memory addresses but rather, references bootstrap. If reference to the magnetic tape load routine is required, the operator may place the switch in the MAIN MEMORY position. Upon completion of the load routine, the switch is placed in the NDRO position and the main memory bootstrap program is protected from destruction even though the main program may order the entire main memory cleared to zero.

In effect, the computer contains the provisions for incorporating two bootstrap programs which may be selected by the BOOTSTRAP MODE switch.

The following description of core magnetization is provided as a prerequisite to the understanding of the magnetic core memories.

Figures 4-43 and 4-44 illustrate the physical location of the memories in the computer cabinet.

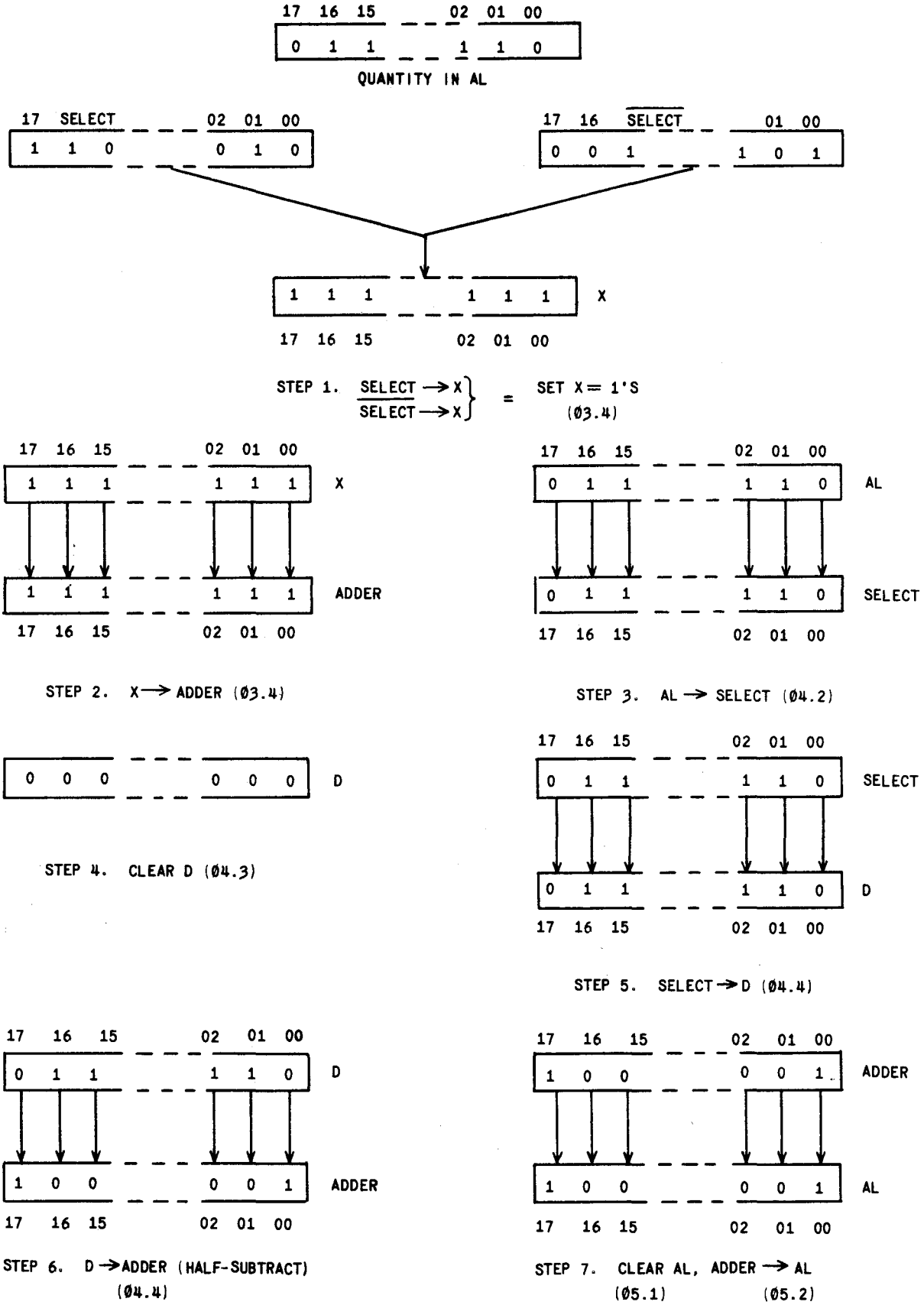


Figure 4-39. Complement AL Sequencing and Functions

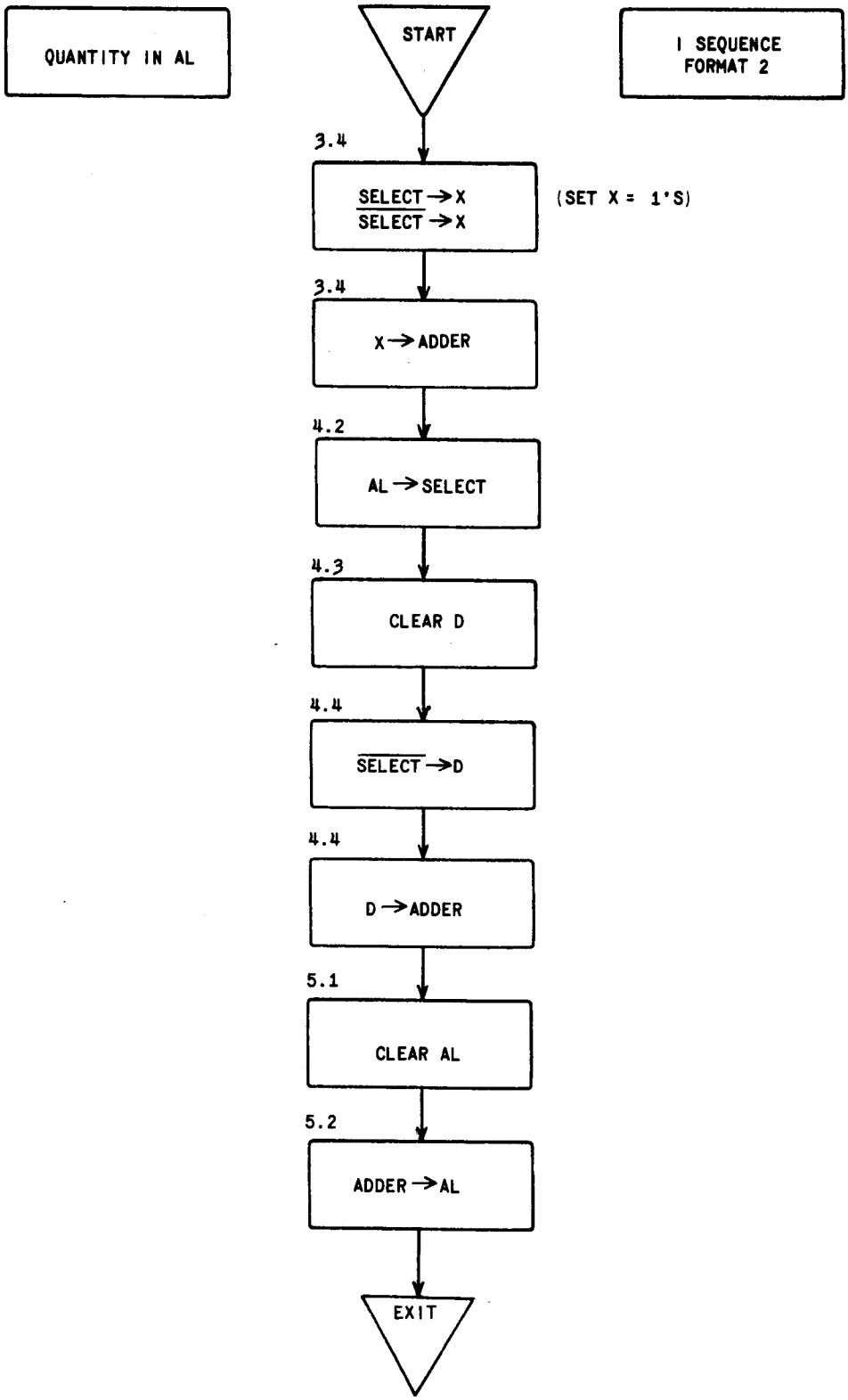


Figure 4-40. Complement AL Instruction Command Sequence

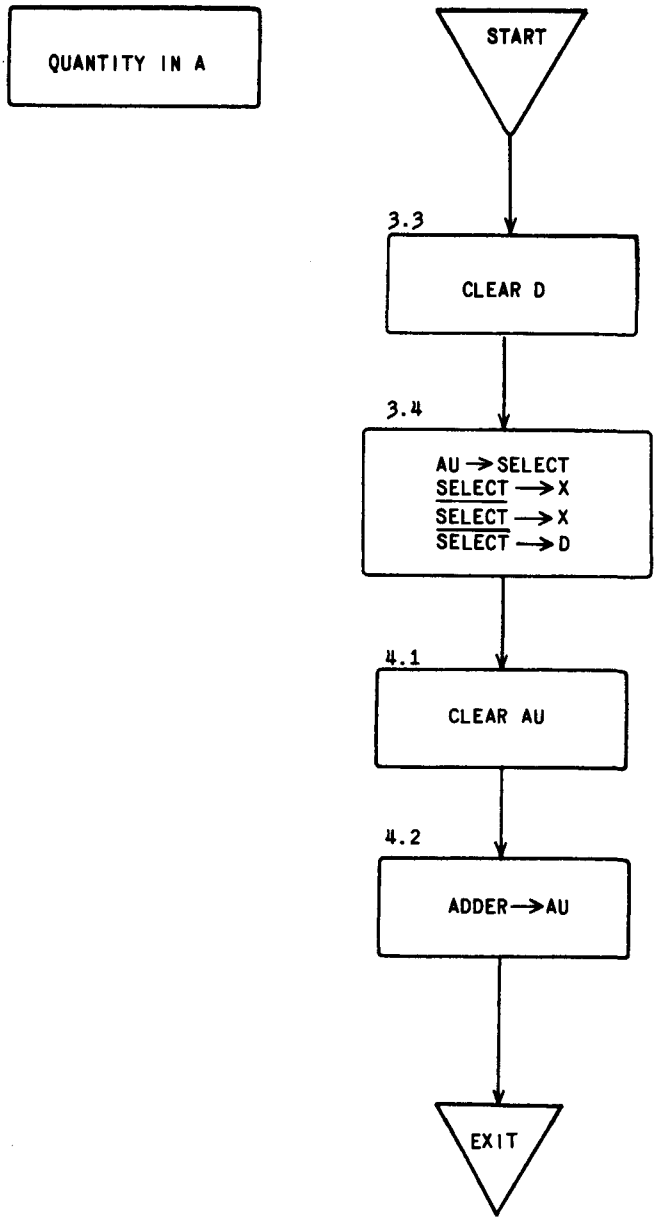


Figure 4-41. Sequencing of Complement AU Instruction 50:62

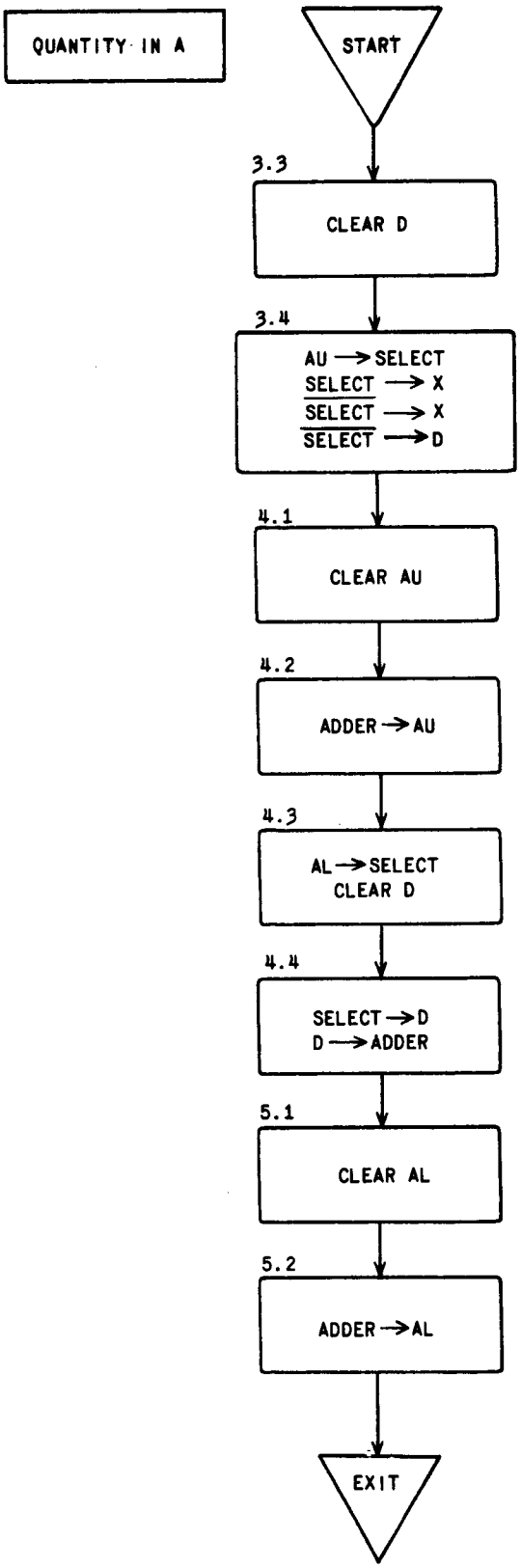


Figure 4-42. Sequencing of Complement A Instruction 50:63

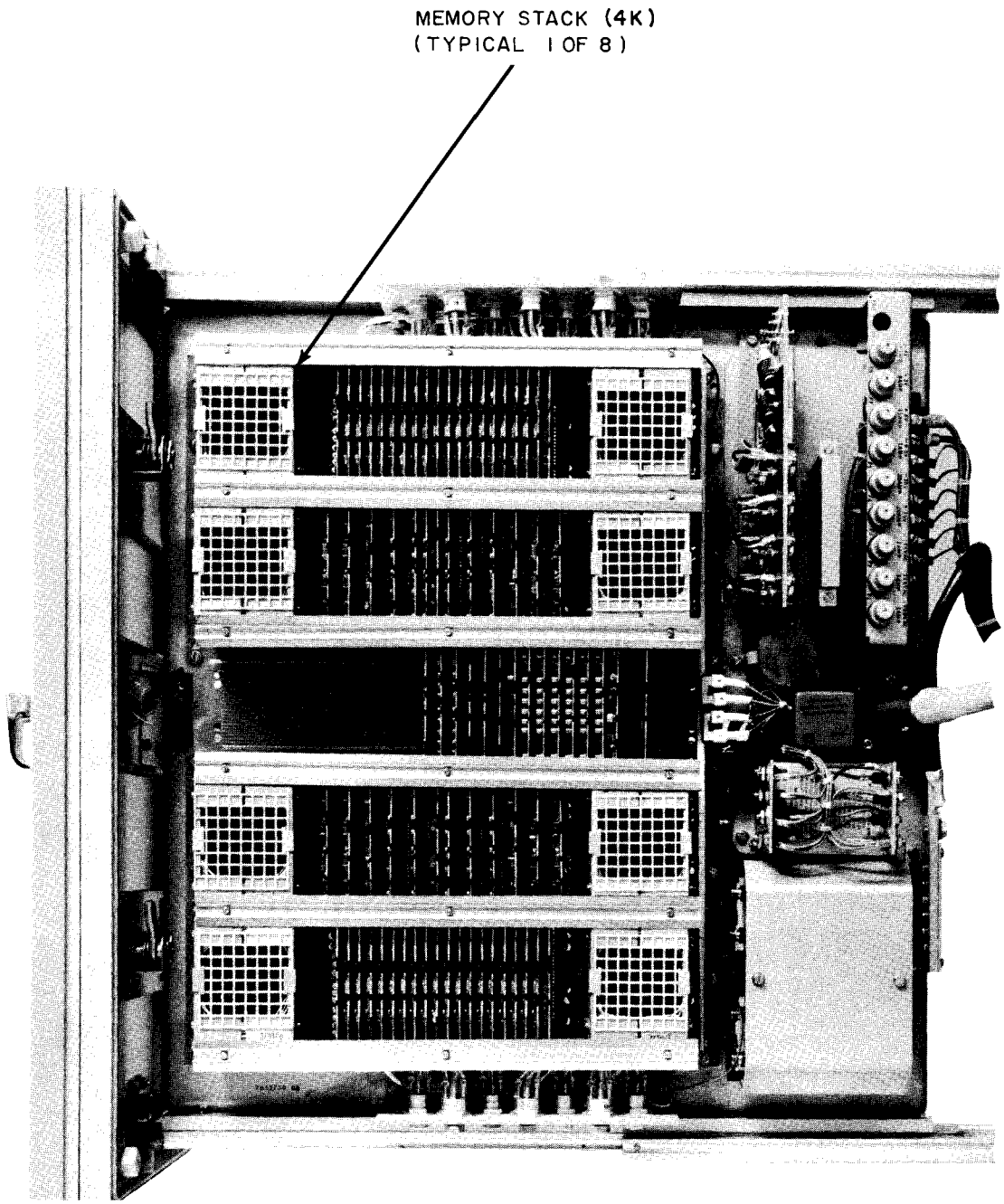


Figure 4-43. Main Memory Location, Drawer A3, (A2)

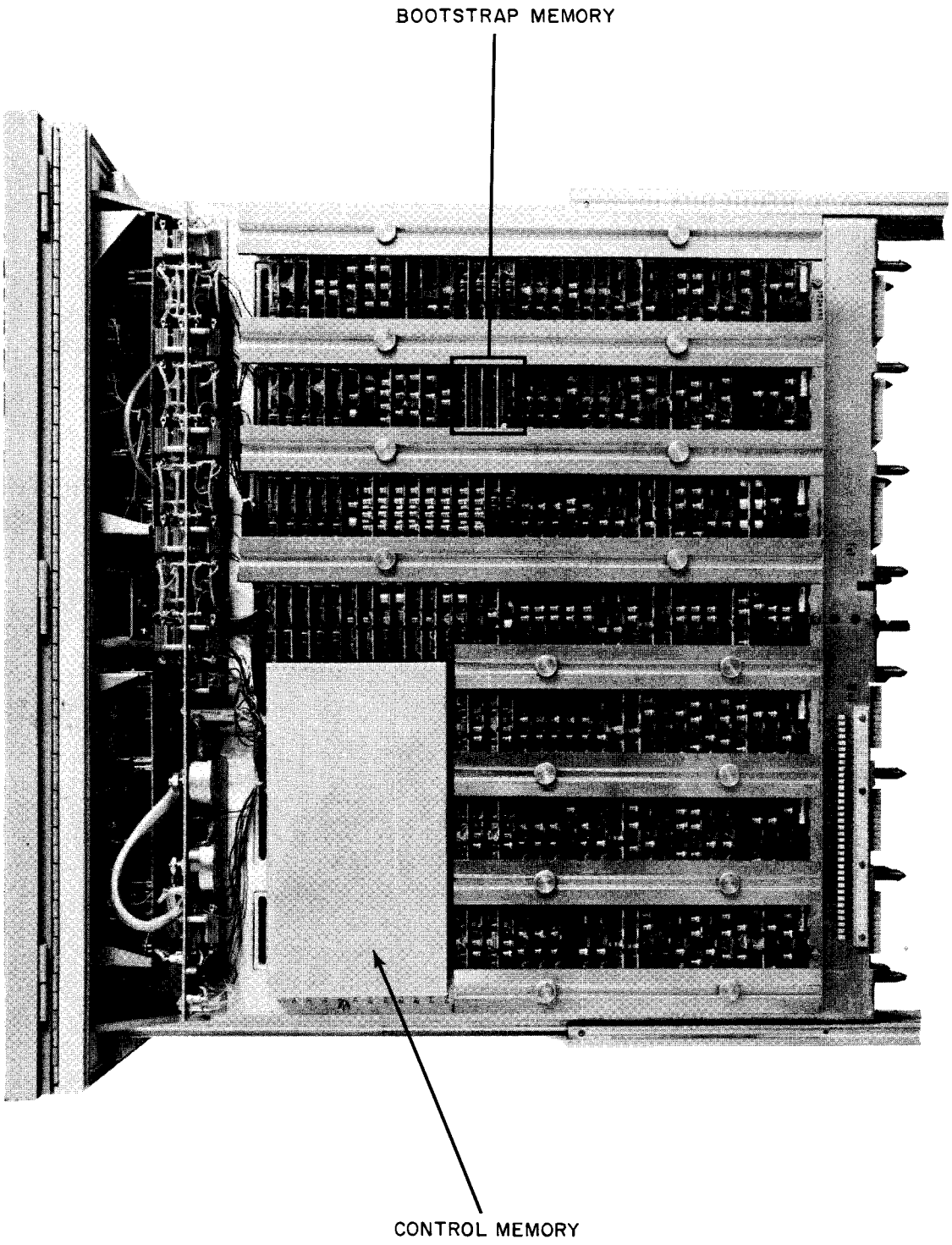


Figure 4-44. Drawer A4, Control And Bootstrap Memory Location

A magnetic core (figure 4-45a) is a ring-shaped ferrite device capable of being magnetized in either of two directions. The core is storing a one when magnetized in one direction, and storing a zero when magnetized in the opposite direction.

Two conductors (X and Y) threaded through the center of the core provide a means for magnetizing the core in either direction (figure 4-45b). The direction of the current pulses through these two conductors determines the magnetic polarity induced in the core. Pulses must be sent simultaneously through both conductors to magnetize the core; a pulse in just one conductor has no affect on the core.

A core is read (figure 4-45c) by magnetizing it to the zero state. If the core is storing a one, it is switched (magnetic polarity changed). The changing polarity induces a sense pulse in a third wire (sense-inhibit) through the core; this sense pulse, during read time, is a one. If the core is already storing a zero when the X and Y read pulses occur, no pulse is induced in the sense-inhibit line; the lack of a sense pulse at read time is a zero.

A read cycle places all cores in zero state prior to writing. A one is written (figure 4-45d) by coincident pulses on X and Y lines in the direction necessary for storing a one. Two coincident-current pulses switch the core to the one state. A zero is written by generating X and Y pulses (as when writing a one) and, at the same time, sending an inhibit pulse through the sense-inhibit line. Direction of the inhibit pulse induces magnetism that counteracts the effect of the X and Y pulses, and results in the core not being switched; the core retains the zero that was stored during the read cycle.

(2) MAIN MEMORY. - The main memory is a random-access, coincident-current, bit-oriented core memory with a 2-microsecond cycle time and 750-nanosecond (maximum) access time. The main memory is available with storage capacity for 16, 32, 49, or 65 thousand 18-bit words. The memory is arranged (functionally and physically) into banks of four stacks per bank; each stack stores 4,000 words. The memory size option is based on the number of 16-K banks selected by the customer.

This description of the main memory is arranged in the following order:

1) Operation of a basic memory stack (para 4-2d(2)(a).
2) Addressing (para 4-2d(2)(b).
3) X or Y line selection circuitry (para 4-2d(2)(c).
4) Sense-inhibit line selection (para 4-2d(2)(d).
5) Sense-inhibit line circuitry (para 4-2d(2)(e).
6) Main memory timing (para 4-2d(2)(f).

(a) MEMORY STACK OPERATION. - A memory stack contains a group of core planes. The number of planes in a stack is determined by the number of bits in the words to be stored. The 1219B computer uses 18-bit words and thus a memory stack in this computer contains 18 core planes.

The number of cores on each plane determines the number of words that can be stored in the stack. Figure 4-46 illustrates a five-bit stack of 6 X 6 planes (six rows of six cores per row); this stack has a capacity of 36 five-bit words.

Each X line passes through a single horizontal row of cores on each plane. Each Y line passes through a single vertical row of cores on each plane. Applying simultaneous current pulses to a single X line and a single Y line selects the one core (on every plane) at the junction of the two lines. The example in figure 4-44 illustrates the selection of the core at the junction of the X2 and Y3 lines (heavy lines).

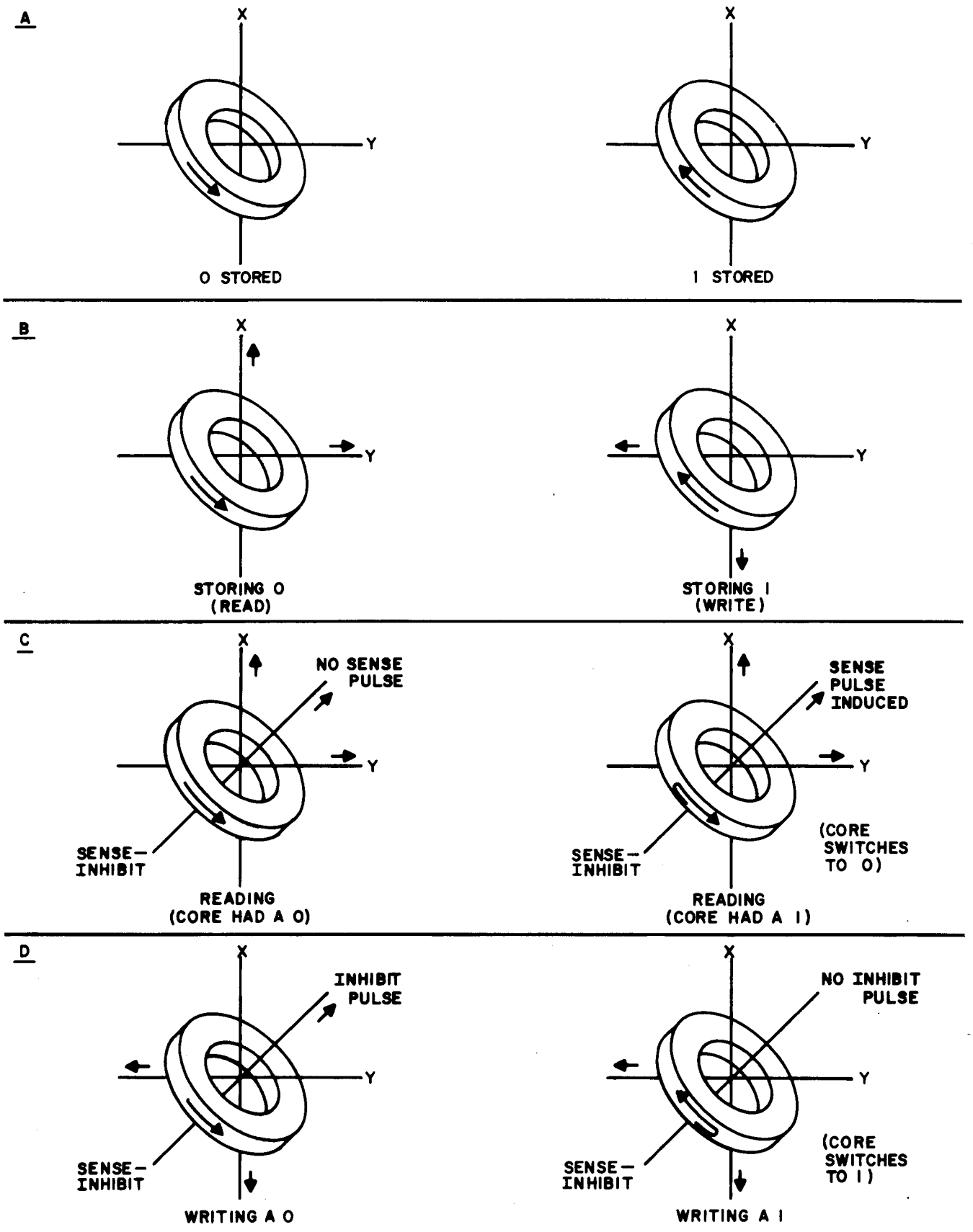


Figure 4-45. Core Magnetization

A separate sense-inhibit line for each plane passes through every core on the plane. The five-array stack in figure 4-46 has five sense-inhibit lines (one for each bit in a word). The 18-bit stacks used in the computer have 18 sense-inhibit lines per stack. During a read cycle, a sense pulse is induced on the sense-inhibit line if the selected core switches from one to zero. If the selected core already contains a zero, it does not switch and no sense pulse is induced on the sense-inhibit line. During a write step, an inhibit pulse is placed on the sense-inhibit line for each plane where a zero is to be written. The lack of an inhibit pulse on the other planes enables a one to be written.

In actual implementation, each plane is divided into two halves and a separate sense inhibit line is used for each half. An explanation of the sense-inhibit circuitry is provided in paragraph 4-2d(2)(e).

(b) ADDRESSING. - Figure 4-47 illustrates memory layout for the computer. The computer can be ordered with from one to four banks of memory stacks (for a total of 16K, 32K, 49K, or 65K word storage). A single memory address is selected by:

a) one of four banks;

b) one of four stacks in the selected bank;

c) one of 64 X-lines in the selected stack;

d) one of 64 Y-lines in the selected stack.

Once a single memory address is selected, a memory cycle (consisting of a read cycle and a write cycle) is performed to read the word stored at that address or store a new word at that address.

A 16-bit word stored in the S_1-register specifies the memory address to be used. Bits 15 and 14 of the S_1-register are used to select one of four banks (figure 4-47). Bits 13 and 12 are decoded to select one of four stacks. Bits 11 through 6 are decoded by the X-line selection circuit and bits 5 through 0 are decoded by the identical Y-line selection circuit.

Figure 4-48 is a block diagram of the circuit used to select one stack in a bank and one of 64 lines (either X or Y) in the stack. The decoded bank-select signal enables the AND gates for one X-selection and one Y-selection circuit. S_1- register bits 12 and 13 are decoded by one of the four AND gates in the primary circuit for the read-write pulse (heavy line in figure 4-48); thus, one of four primary windings is enabled for group selection.

Six S_1-register bits are used to select one of 64 X or Y lines in the stack; three bits select one of eight groups, and three bits select one of eight lines in each group. Group-select translators (figure 4-48) select one of eight secondary windings in the group select transformer. The word line translator selects one of eight secondary windings in the word select transformer. A secondary circuit is completed, then through one of eight word-select-transformer windings, one of 64 stack lines, and through one of eight group-select-transformer windings. During the memory cycle, a read pulse or a write pulse on the primary circuit is induced in one of 64 completed secondary circuits.

(c) X OR Y LINE SELECTION CIRCUIT. - Figure 4-49 illustrates an X-line or Y-line selection circuit for a single stack. The heavy line in the figure shows write current path for the selection of line one in group one. The word line translator decodes the three-bit input and turns on one of eight transistor switches

(Q1 in figure 4-49). The group selector decodes the other three-bit input and turns on one of eight transistor switches (Q2 in figure 4-49). A secondary write circuit is completed through CR4, Q2, CR6, one of eight T3 secondary windings, one line of cores in the stack, CR8, one of eight T2 secondary windings, Q1, CR1, and ground. A secondary read circuit is also selected through CR2, Q1, one of eight T1 secondary windings, CR7, one line of cores in the stack, one of eight T3 secondary windings, CR5, Q2, CR3, and ground.

Primary circuit for the stack is enabled by decoding stack select bits (12 and 13) and turning on transistor switch Q5. A write pulse turns on transistor Q4 and completes a primary circuit from -15 volts, through Q4, T2 primary, T3 primary pins 4, and 3, Q5, and L1 to +15 volts. A read pulse turns on transistor Q3 and completes a primary circuit from -15 volts, through Q3, T1 primary, T3 primary pins 1 and 2, Q5, and L1 to +15 volts. Transistor Q6 normally is on and clamps the collector of Q5 to -15 volts. The read pulse or write pulse turns off Q6, and thereby generates a pulse on the primary line.

A write current pulse is induced in the secondary circuit in one direction (from group selector to word line translator), and a read current pulse is induced in the opposite direction (word line translator to group selector). The difference in current direction is determined by the difference between the winding direction of T1 and T2 secondaries, and between the two halves of T3 primaries.

(d) SENSE-INHIBIT LINE SELECTION. - The sense-inhibit line circuitry for a single bit in one bank is illustrated in figure 4-50. Eighteen of these circuits are required for each bank. Heavy lines depict current path for an inhibit pulse to a plane in stack one and the current path for a sense pulse from a plane in stack two.

1. INHIBIT. Flip-flop Z17 (figure 4-50) is set by an input on pin 52 prior to receiving an inhibit pulse. An inhibit pulse at input pin 40 generates a negative pulse through the primary of transformer T3 (from Z4 pin 13 to Q10). The pulse induced in T3 secondary turns on transistor switch Q7, and completes a circuit through resistor R7, reactor T1, Q7, and transformer T7. The pulse induced in the secondary of T7 is the inhibit current pulse that passes through all cores on a single array of stack one.

Excessive current through T1 causes T1 to saturate and increase the voltage drop across R7. This voltage, inverted by transistor Q1, resets flip-flop Z17. Flip-flop Z17, through AND gate Z4, and T3, turns off Q7 and blocks any further inhibit current to stack one.

2. SENSE. The 4096 cores on a single plane of a memory stack are divided into two halves; one sense wire passes through half of the cores and a second sense wire passes through the other half of the cores. A read pulse on a single X-line and a single Y-line induces a noise pulse on both sense lines. If the addressed core (at the junction of X and Y lines) already contains a zero and does not switch, two noise pulses are identical. If the addressed core switches to zero (because it stored a one), the magnetic change induces a pulse on one of the sense lines. This pulse occurring with the noise pulses must be detected as a difference between the two noise pulses.

Transformer T16 (figure 4-50) is a common mode rejection transformer. Because the two windings are in the same direction (note the polarity dots on the same side for both windings), the transformer appears as a high impedance when both inputs are the same polarity. When the two inputs are different, the transformer appears

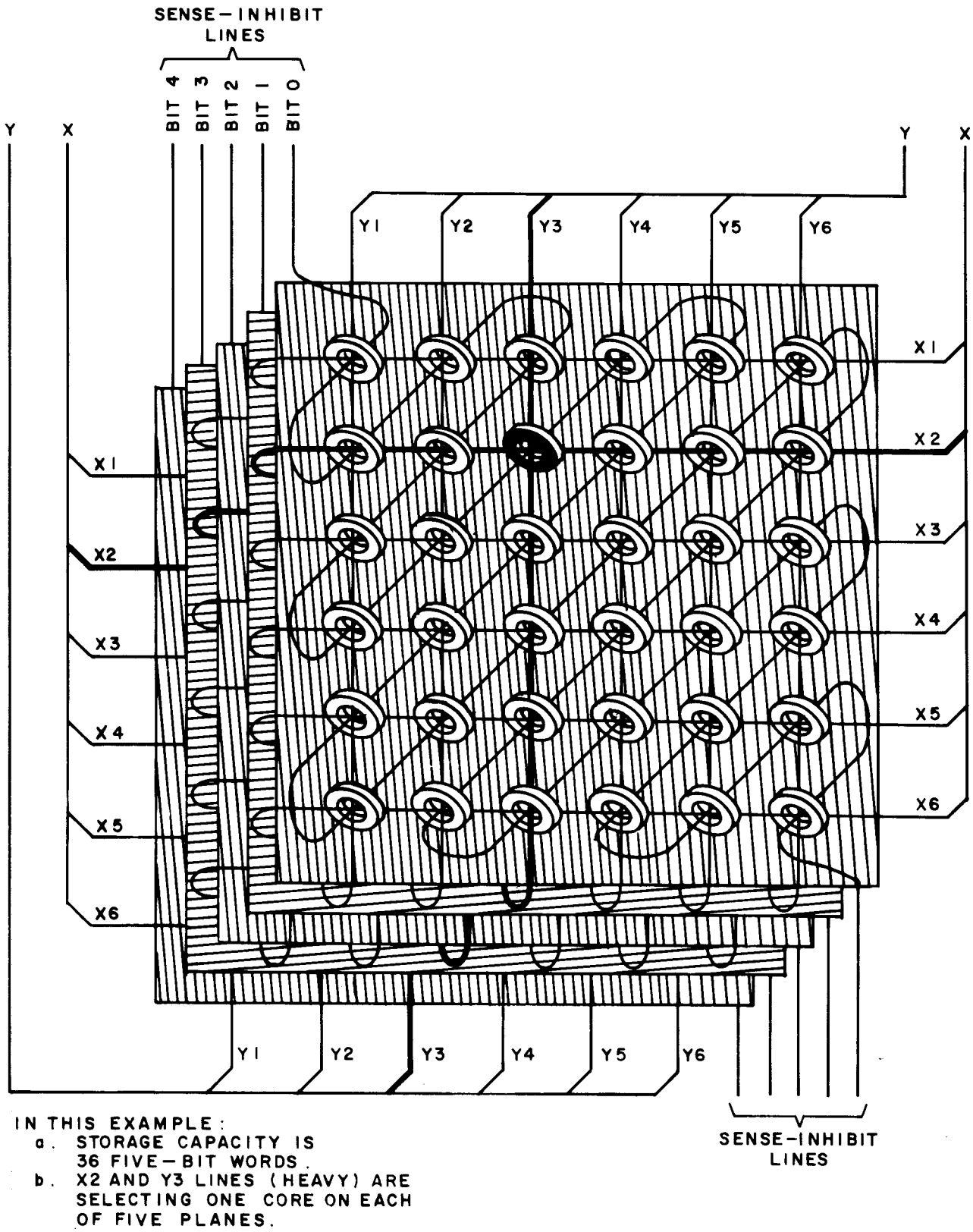


Figure 4-46. Memory Stack Operation

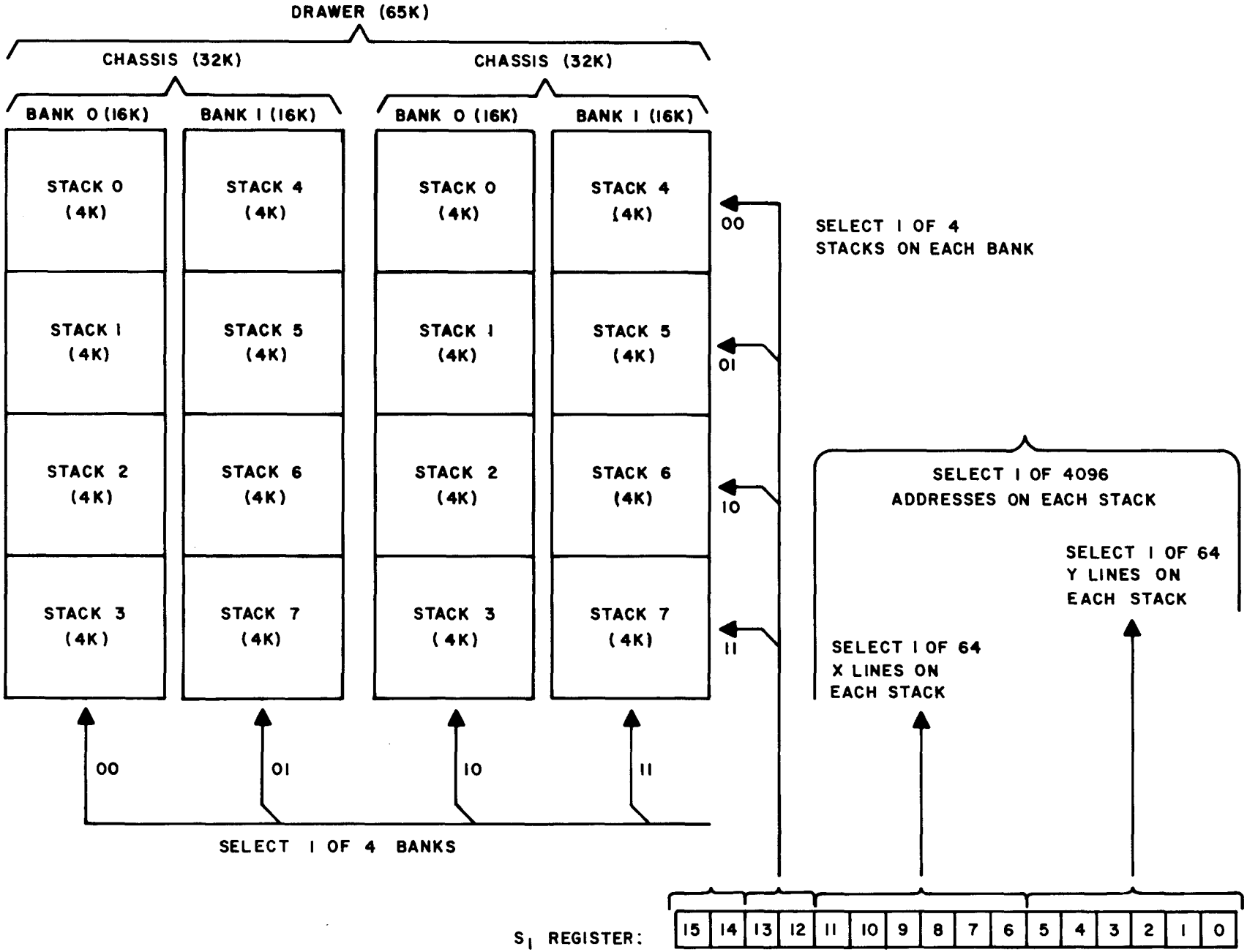


Figure 4-47. Main Memory Addressing

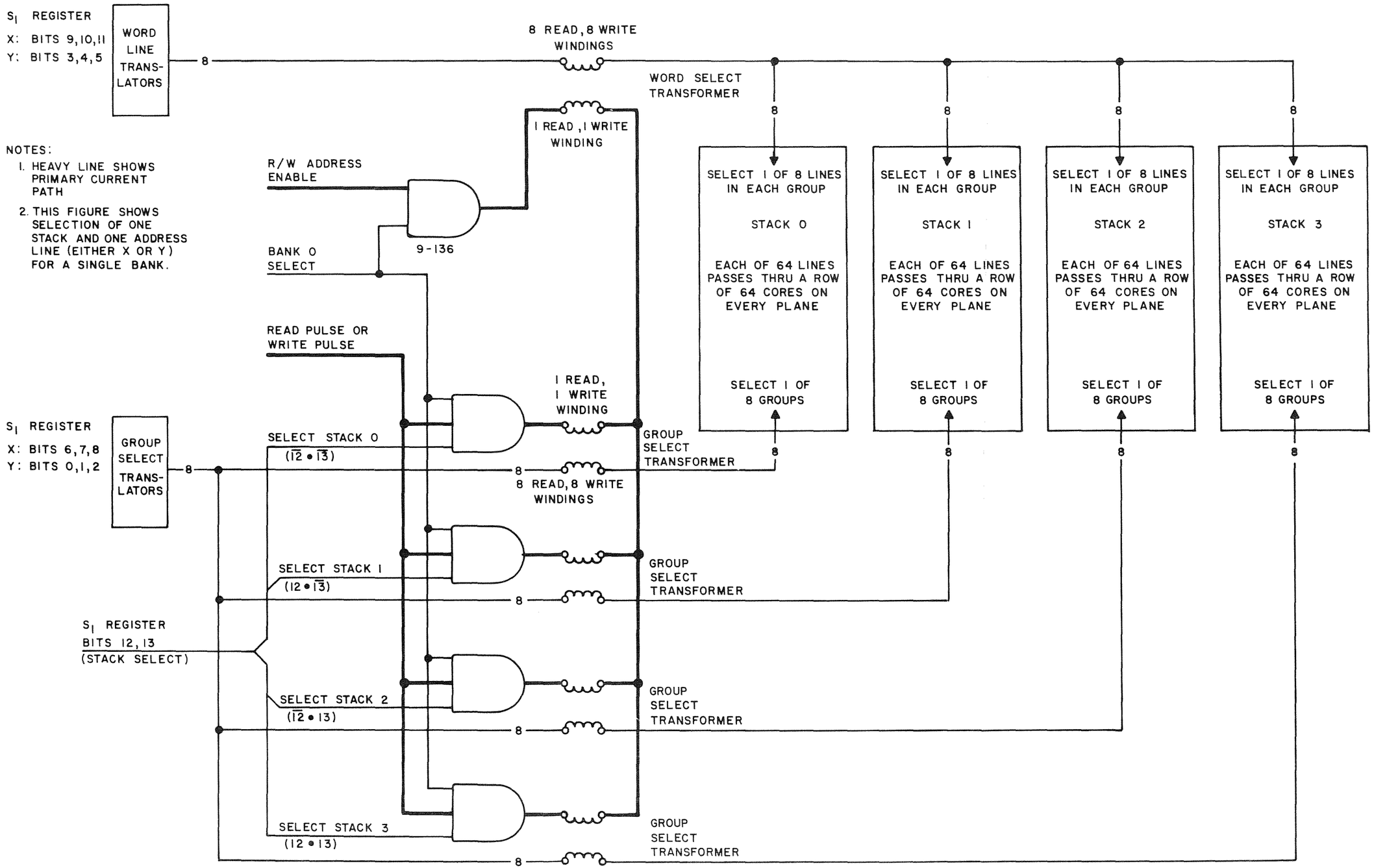
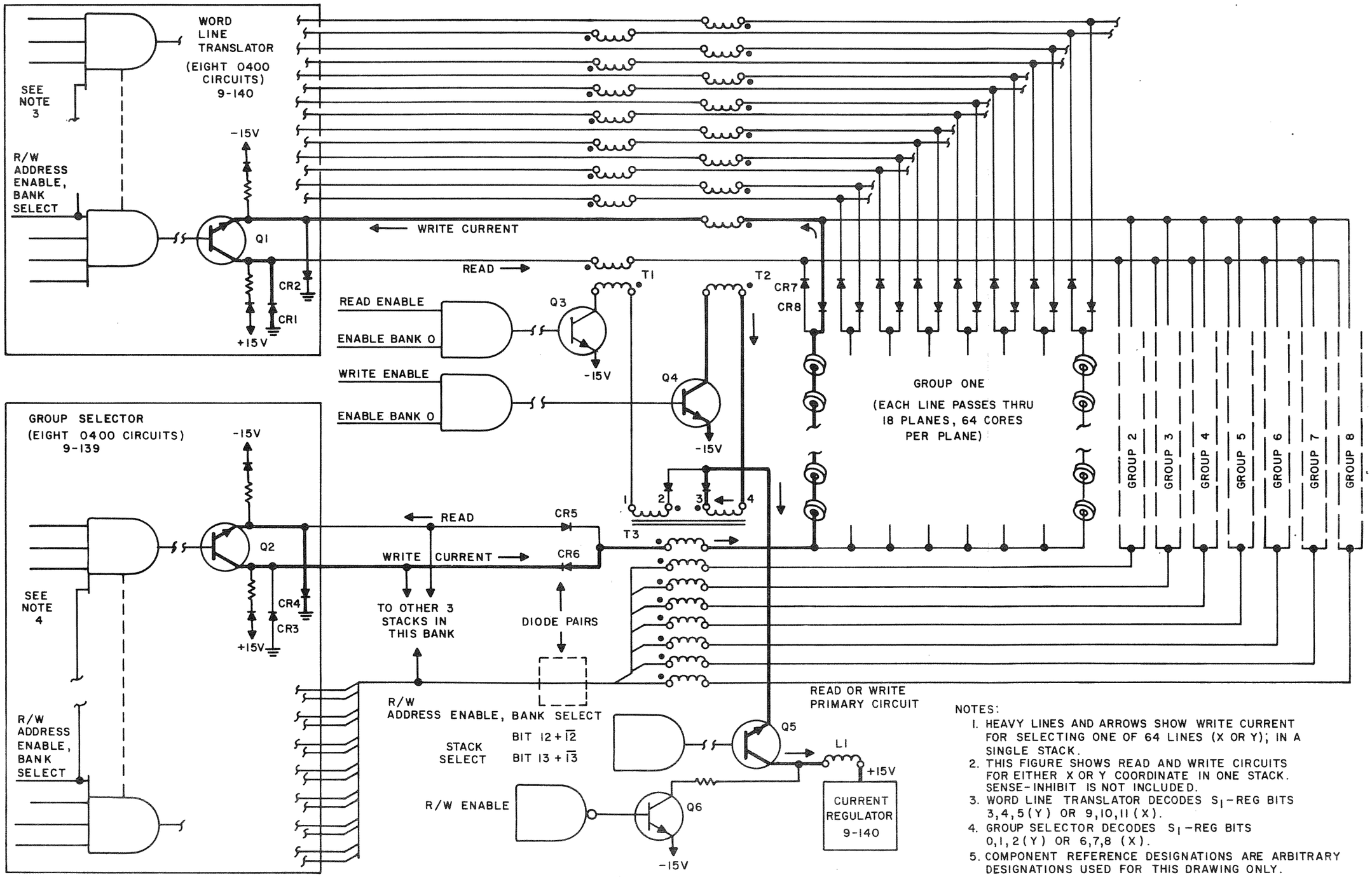


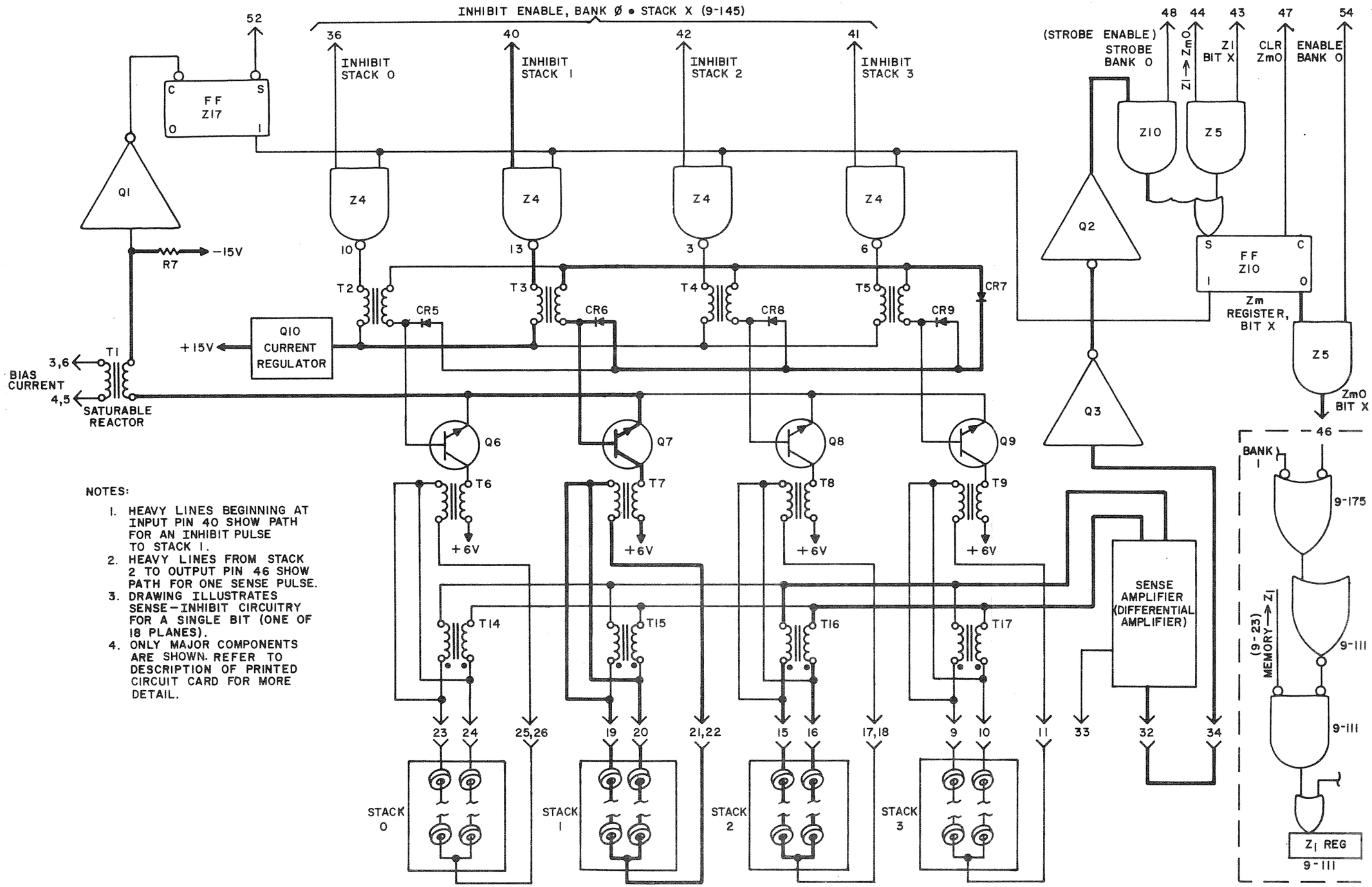
Figure 4-48. Stack Select And X Or Y Axis Select



NOTES:

1. HEAVY LINES AND ARROWS SHOW WRITE CURRENT FOR SELECTING ONE OF 64 LINES (X OR Y); IN A SINGLE STACK.
2. THIS FIGURE SHOWS READ AND WRITE CIRCUITS FOR EITHER X OR Y COORDINATE IN ONE STACK. SENSE-INHIBIT IS NOT INCLUDED.
3. WORD LINE TRANSLATOR DECODES S_1-REG BITS 3,4,5(Y) OR 9,10,11(X).
4. GROUP SELECTOR DECODES S_1-REG BITS 0,1,2(Y) OR 6,7,8 (X).
5. COMPONENT REFERENCE DESIGNATIONS ARE ARBITRARY DESIGNATIONS USED FOR THIS DRAWING ONLY.

Figure 4-49. X or Y Line Selection Circuit



NOTES:

1. HEAVY LINES BEGINNING AT INPUT PIN 40 SHOW PATH FOR AN INHIBIT PULSE TO STACK 1.
2. HEAVY LINES FROM STACK 2 TO OUTPUT PIN 46 SHOW PATH FOR ONE SENSE PULSE.
3. DRAWING ILLUSTRATES SENSE-INHIBIT CIRCUITRY FOR A SINGLE BIT (ONE OF 18 PLANES).
4. ONLY MAJOR COMPONENTS ARE SHOWN. REFER TO DESCRIPTION OF PRINTED CIRCUIT CARD FOR MORE DETAIL.

Figure 4-50. Sense-Inhibit Line Selection

as a very low impedance. The relative voltage difference between the two noise pulses at the moment the addressed core switches (X in figure 4-51) is passed through the transformer. This small voltage difference (of either polarity) is detected by the differential type sense amplifier as a stored one. The sense amplifier output is gated by the strobe-bank-0 signal to set flip-flop Z10. The flip-flop, representing a single bit of the Zm0-register, now stores the one that was read from memory.

(e) SENSE-INHIBIT LINE CIRCUITRY. - A single module contains all circuits necessary for generating an inhibit pulse, and for sensing and storing a sense pulse for a single bit for all four stacks of a memory bank. Figure 4-50 is a block diagram of the module and the related memory stacks. Heavy lines in figure 4-50 illustrate current path for an inhibit pulse to stack one and current path for a sense pulse from stack two; figure 4-52 is a more detailed diagram showing just these two circuits.

1. INHIBIT. - A negative input pulse at pin 52 sets flip-flop Z17. When this input again goes positive, flip-flop output is gated to AND gate Z4. An inhibit pulse for stack one then is enabled by Z4, and Z4 pin 13 goes negative. An inhibit pulse from Z4 pin 13 passes through transformer T3 primary, transistor Q10 to +15 volts. Q10 and its associated bias resistors form a base-drive, current-limiter circuit for T3 primary.

Transformer T3 provides a 1:3 current step-up for base drive to transistor Q7. Q7 is turned on and completes the circuit. The inhibit current pulse through transformer T7 primary is induced in T7 secondary circuit, which passes through all cores in a single plane of the memory stack.

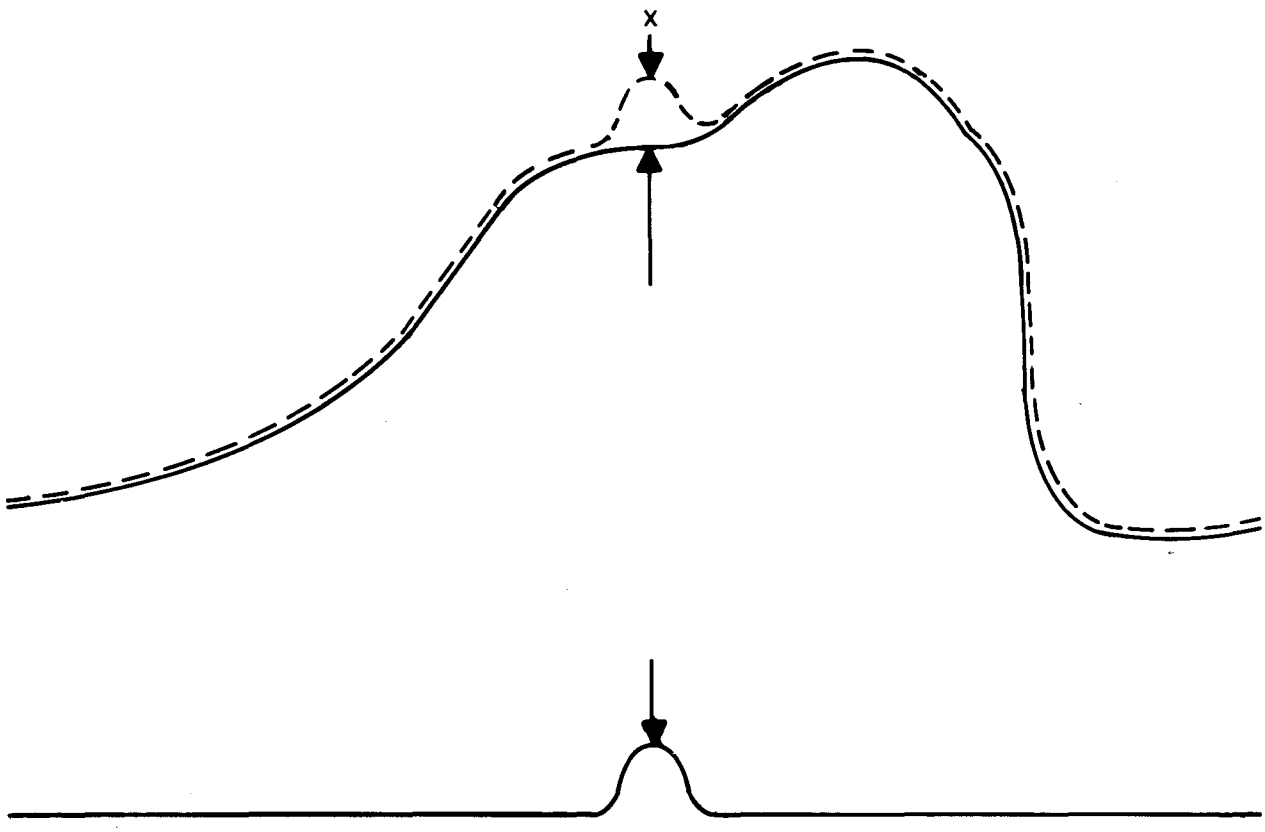


Figure 4-51. Signal Detection Through Rejection Transformer

T7 is a 2:1 current step-up transformer for the core circuit. Resistor R30 is a damping resistor for T7, and diode CR13 protects Q7 collector from excessive positive spikes at turn-off time.

Diodes CR18 and CR19 recover T7 so that secondary will not average the primary current after a series of inhibit pulses (secondary current returns to zero after each pulse). Transformer T11 compensates for possible differences in voltage drops across the two diodes.

Saturable reactor T1, transistor Q1, and flip-flop Z17 (figure 4-51) monitor the inhibit pulse current and block the pulse when excessive current is detected. T1 can saturate in either direction or it can be balanced between these two saturated conditions (see figure 4-53). The bias current through T1, pins A1 through A4, holds T1 biased in one direction (a, figure 4-53). The inhibit pulse current through R7, Q7, and T7 passes through T1, pins B7 through B10; this current is just enough to overcome bias current and hold T1 out of saturation (b, figure 4-53). If the inhibit pulse duration is too long, or excessive current occurs because of a defective component, T1 saturates in a direction opposite to the biased direction (c, figure 4-53). The voltage drop across R7 then increases enough to turn on Q1. The negative-going collector of Q1 resets flip-flop Z17. The output of Z17, through T3, turns off Q7 to block any further inhibit current to the cores.

2. SENSE. - An X-line read pulse and a Y-line read pulse in memory stack two (figure 4-52) induces a noise pulse on both sense lines from each plane in the stack (one line for each half of the plane). If the addressed core in the stack switches (from zero to one), the magnetic change induces a pulse on just one of the sense lines. This pulse is recognized as a difference between the two lines by common-mode-rejection transformer T16. Because the two halves of T16 are wound in the same direction, current applied from pins A1 to A2 attempts to induce current from pins B4 to B3, corresponding with negative voltage applied at pin A1 and positive applied at pin B3. Conversely, like voltages at pins A1 and B3 react against each other; the effect being a high impedance to alike inputs.

A voltage difference between the two halves of the core plane (generated by switching a core in only one half) is amplified by a two-stage differential amplifier consisting of Q4, a and b, and Q12, a and b. Resistors R15 and R18 are degenerative-feedback resistors for first stage of the differential amplifier; they lower differential input impedance so four quadrants can be terminated into one amplifier.

Transistor Q5 provides a high-impedance current source for Q4, and transistor Q11 provides a high-impedance current source for Q12. A high-impedance current source aids in common-mode rejection of the differential amplifier.

Transistors Q13 and Q14 comprise a rectifier for the final stage of the sense amplifier, enabling detection of differential signals of either polarity. A regulated threshold supply is connected to pin 33. The value of this threshold supply, and the value of R54 determines the point at which Q3 switches.

A switched core (stored one) detected by the sense amplifier turns on Q3, which then turns off Q2. The positive-going output of Q2 is strobed through AND gate Z10 to set flip-flop Z10. The flip-flop is one bit of an 18-bit Zm0 register.

(f) MAIN MEMORY TIMING. - A single main-memory timing cycle is performed to read a single word from memory or to write a single word into memory. First half of the memory timing cycle (read half-cycle) controls reading of a word from memory. Second half of the memory timing cycle (write half-cycle) controls writing of a word into memory.

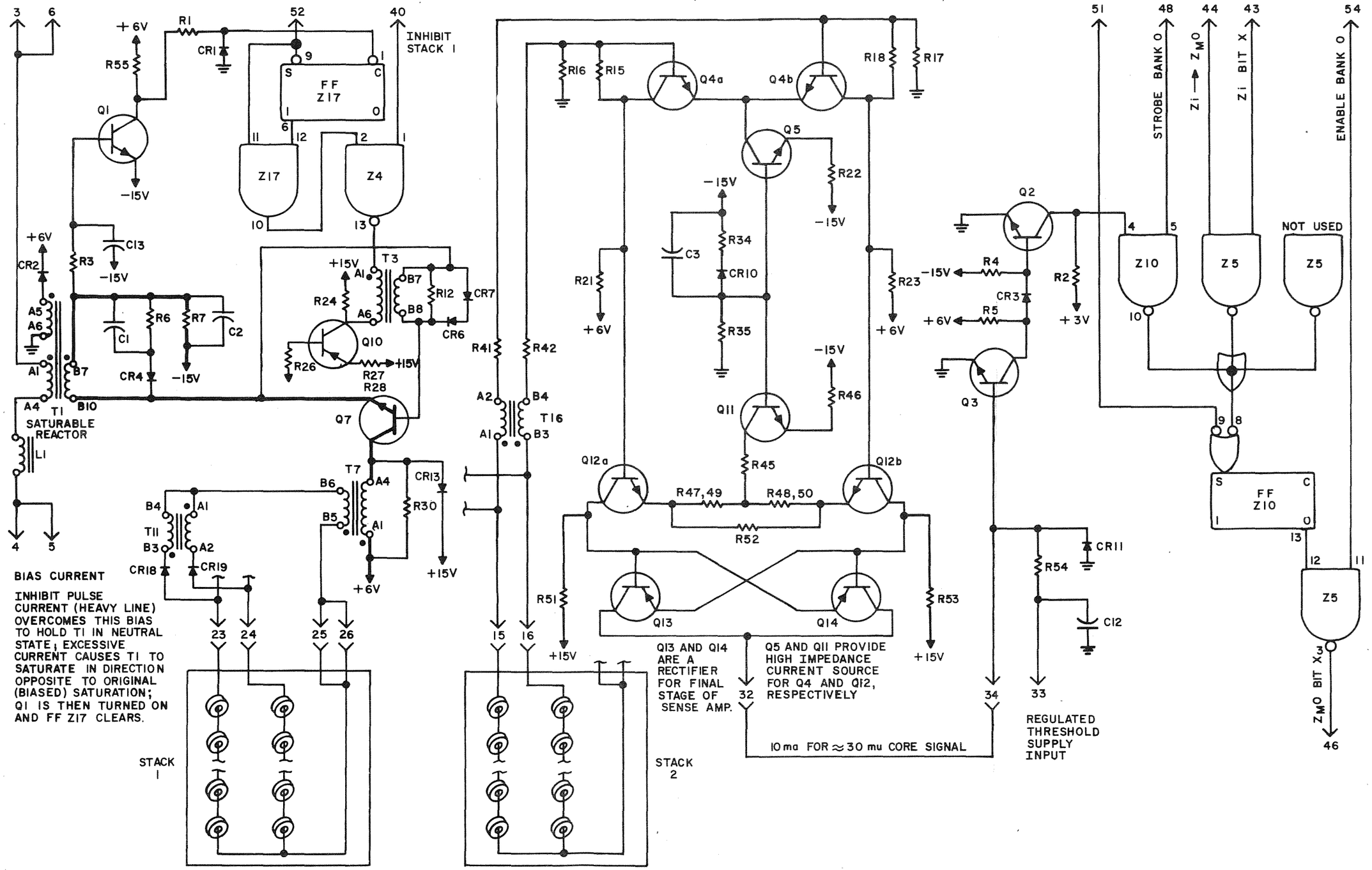
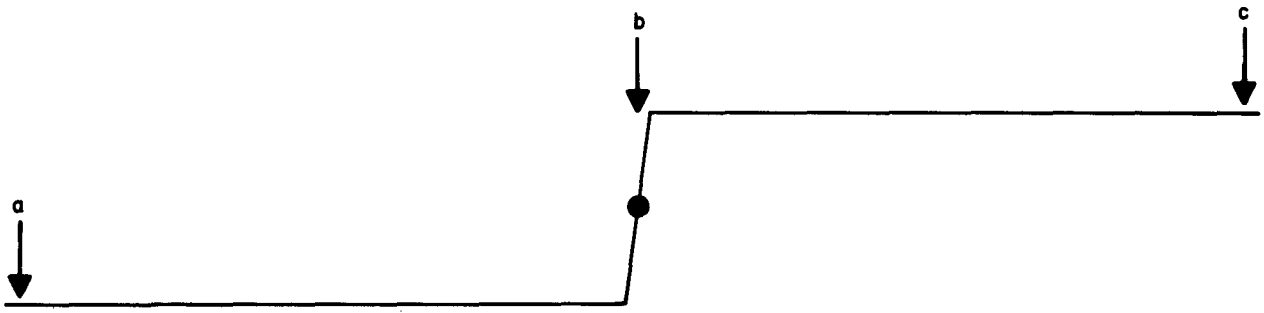
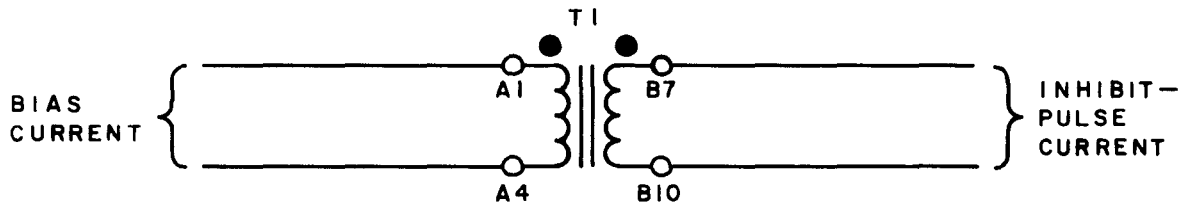


Figure 4-52. Sense-Inhibit Line Circuitry

Figure 4-53



BIAS CURRENT FROM PIN A1 TO A4 CAUSES T1 TO SATURATE IN ONE DIRECTION (POINT a ON CURVE). INHIBIT—PULSE CURRENT FROM PIN B7 TO B10 COUNTERACTS BIAS CURRENT AND HOLDS T1 OUT OF SATURATION (POINT b ON CURVE). EXCESSIVE CURRENT FROM PIN B7 TO B10 CAUSES T1 TO SATURATE IN A DIRECTION OPPOSITE TO BIASED DIRECTION (POINT c ON CURVE).



To read a word from memory, the word is taken out of memory and stored in Z_1 register during read half-cycle; during write half-cycle, the word is restored to its original locating in memory. To write a word in memory, read half-cycle is performed but the word is not stored in Z1 register; thus, the selected memory location is cleared. The word to be stored is placed in Z1 register and, during write half-cycle, loaded into memory.

The timing diagram (figure 4-54) should be used in conjunction with the figures referenced during the following discussion.

The initiate-memory signal applied to the 1-microsecond delay line (figure 9-135) starts memory timing cycle. The leading edge of initiate-memory starts read half-cycle, and the trailing edge starts write half-cycle. Initiate-memory signal is generated by flip-flop OXG80 (figure 9-134); this flip-flop is set during time T11 at clock-phase one and reset during time T24 at clock-phase four.

Outputs of the delay line on figure 9-135 are gated so as to provide a sequence of control signals for the memory operation. R/W-address-enable, read-enable, and R/W-enable signals are required to generate X and Y line read pulses through the selected address (see figure 4-49). R/W-address-enable signal (figure 9-136) is turned on by address-enable-(read) from figure 9-135. Bank-selection gating is provided by address decoding circuitry. Read-enable and R/W-enable signals are provided by the delay-line decoding circuitry on figure 9-135.

Read pulses induced in the sense lines are detected by the sense amplifiers and the resultant data bits are gated into the Zm register by the strobe-enable pulse (figure 4-50). The strobe-enable pulse generated by delay line decoding (figure 9-135) is gated by bank selection signals (figure 9-136) and sent to Zm register input gate as either strobe-bank-0 or strobe-bank-1.

If the memory operation being performed is a read operation, the data in the Zm register must be transferred to the Z_1 register. Zm register outputs from bank 0 and bank 1 are ORed together (figure 9-175) and sent to the Z_1 register (figure 9-111). The memory $\longrightarrow$ Z_1 signal necessary to transfer the read data is generated at time T22 (figure 9-23).

If memory operation being performed is a write operation, the memory $\longrightarrow$ Zm signal is blocked. Four specific conditions that block memory $\longrightarrow$ Z_1 are shown on figure 9-23: activating AND gate 13N13 degates (blocks) AND gate 17N13; activating any of the three three-input gates to 10N13 degates AND gate 11N13. Write data destined for memory storage is gated to the Z_1 register by the input gates on figure 9-111.

Clear-Zm pulse (figure 9-136) to either bank 0 or 1 occurs at the beginning of the write half-cycle to clear the Zm register. The Z1 $\longrightarrow$ Zm pulse originates from the same delay line outputs as the clear-Zm pulse, but Z_1 $\longrightarrow$ Zm is delayed approximately 10 nanoseconds by circuit delay; thus, Z_1 register contents are gated to Zm register immediately after Zm register is cleared.

X and Y line write pulses are generated by the R/W-address-enable, write-enable, and R/W-enable signals (figure 4-49). R/W-address-enable signal (figure 9-136) is turned on by address-enable (write) from figure 9-135. Bank-selection gating is provided by address decoding circuitry. Write-enable and R/W-enable signals are provided by delay-line decoding circuitry on figure 9-135.

Zm register contents are gated out by the inhibit-enable signal from figure 9-135. Inhibit-enable is gated by bank selection on figure 9-136. Each bit position of Zm register that contains a zero is gated to the sense-inhibit line as an inhibit pulse.

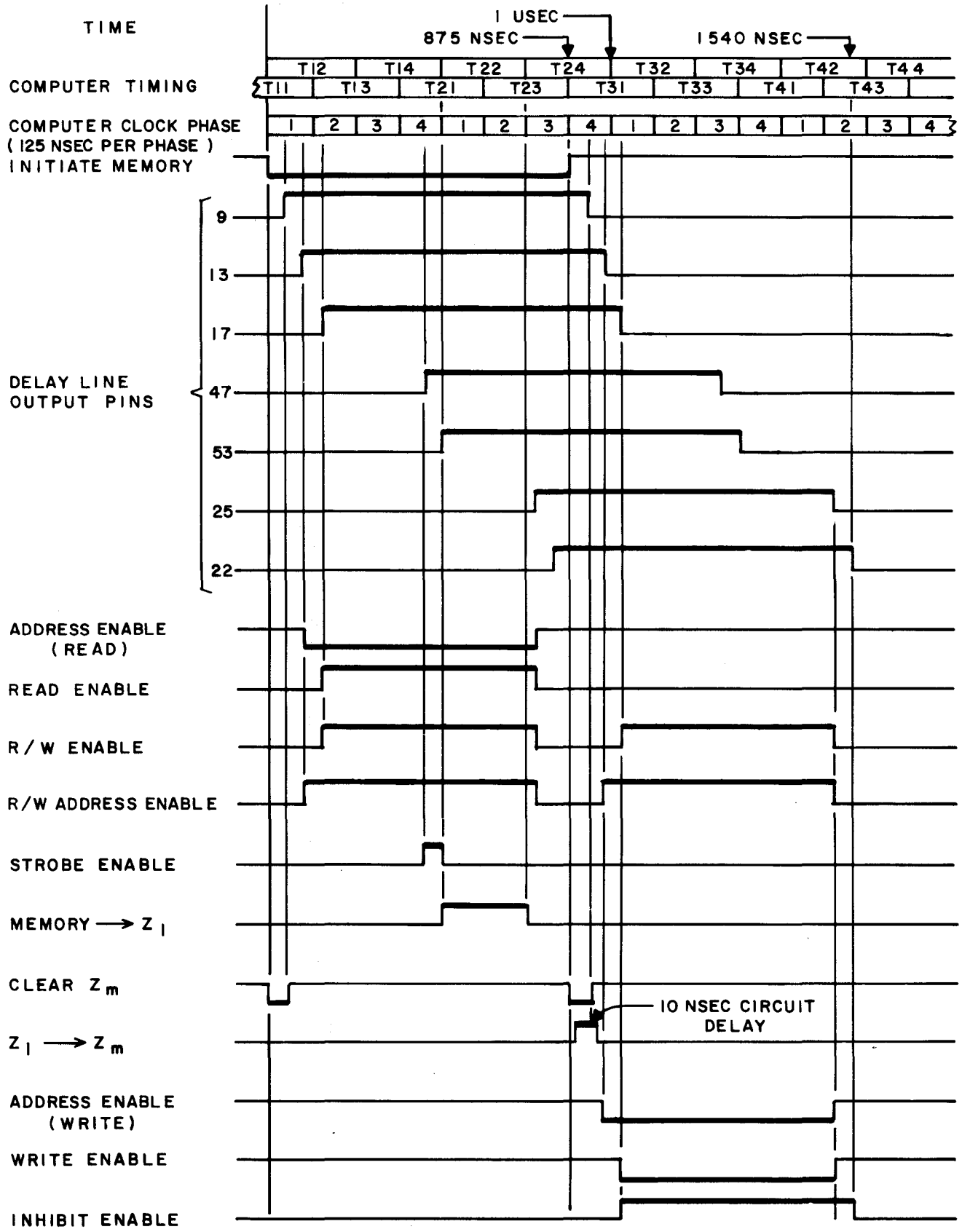


Figure 4-54. Main Memory Timing

(3) CONTROL MEMORY. - Control memory is a word-oriented, two-cores-per-bit memory with a 500-nanosecond cycle time. The control memory has a word length of 18 bits and is available in two sizes, 128 and 256 words.

The control memory is a random-access device and uses addresses 00000 through 00077 and 00200 through 00277 for the 128-word memory; and, in addition, addresses 00400 through 00477 and 00600 through 00677 for the 256-word memory. The control memory has a destructive readout; and therefore, requires a write operation as second half of the memory cycle.

The control memory (figure 4-55) functions when the control portion is enabled and has received inputs from the S_0 register, and the control and bootstrap memory timing. Enable for the control portion is present at all times except when bootstrap memory is in use. Inputs from the S_0 register and control memory timing are available whenever an address is gated into the S_0 register because the register gate is also the timing enable.

Outputs from the control portion are used to develop read, write, digit driver (which performs a similar function to a main memory inhibit), and strobe signals. The core stack consists of either one plane (128-word) containing the transformers, diode links and cores, or two identical planes (256-word). The 18 sense amplifiers and Z_0 register complete the control memory.

Control and bootstrap memory timing (figure 4-56) shows approximate times at which control signals are enabled and disabled by the clock. The timing shown is the suggested timing for control memory and may not correspond directly with timing achieved by the connections shown on figure 9-122, control memory timing functional schematic; however, because of inherent circuit card delays, clock connections may be changed to obtain the suggested timing. Moving connections in the directions indicated by the arrows above delay lines makes a corresponding change in timing shown at the similarly marked points on the time line.

(a) ADDRESSING. - Control memory addressing is similar to that of main memory except that addresses of control memory are not in complete numerical order and memory is word-oriented. Control memory addressing (figure 4-57) functionally depicts the operations necessary to use a memory location.

An address may be placed in the S_0 register under any one of three general conditions: if the S_1 register (main memory) contains a control memory address, contents of the S_1 register are gated into the S0 register; an address may be placed in the S0 register during any I/O sequence except ESA; or during an instruction in which B is involved for a reason other than B modification (Store B, B Skip, etc.). Because octal addresses in the 100's, 300's, 500's and 700's are included in main memory, binary bit number six has been omitted from the S0 register. A binary one in bit six would yield these main memory addresses and would not be addressed through the S_0 register.

The control memory (S_0 register) address translation scheme is shown in figure 4-58. All of the translating circuits are shown on figure 9-124. Half of the diode selectors (see the translation of bit 8) and the lower endboard selectors translate the lower three bits and select one of the eight diode links. Half of the group selectors (see translation of bit 7) and upper endboard selectors translate the third through fifth bits and select one of the eight line groups. The connections between eight diode links and eight line groups are made in the same manner as the connection between diode links and transformers of main memory. However, each of the eight diode links in the control memory have 16 diode pairs, eight for each 64 words; and to provide for the 128 word lines necessary per core plane, there are 16 line groups, each with eight lines (see figure 9-127).

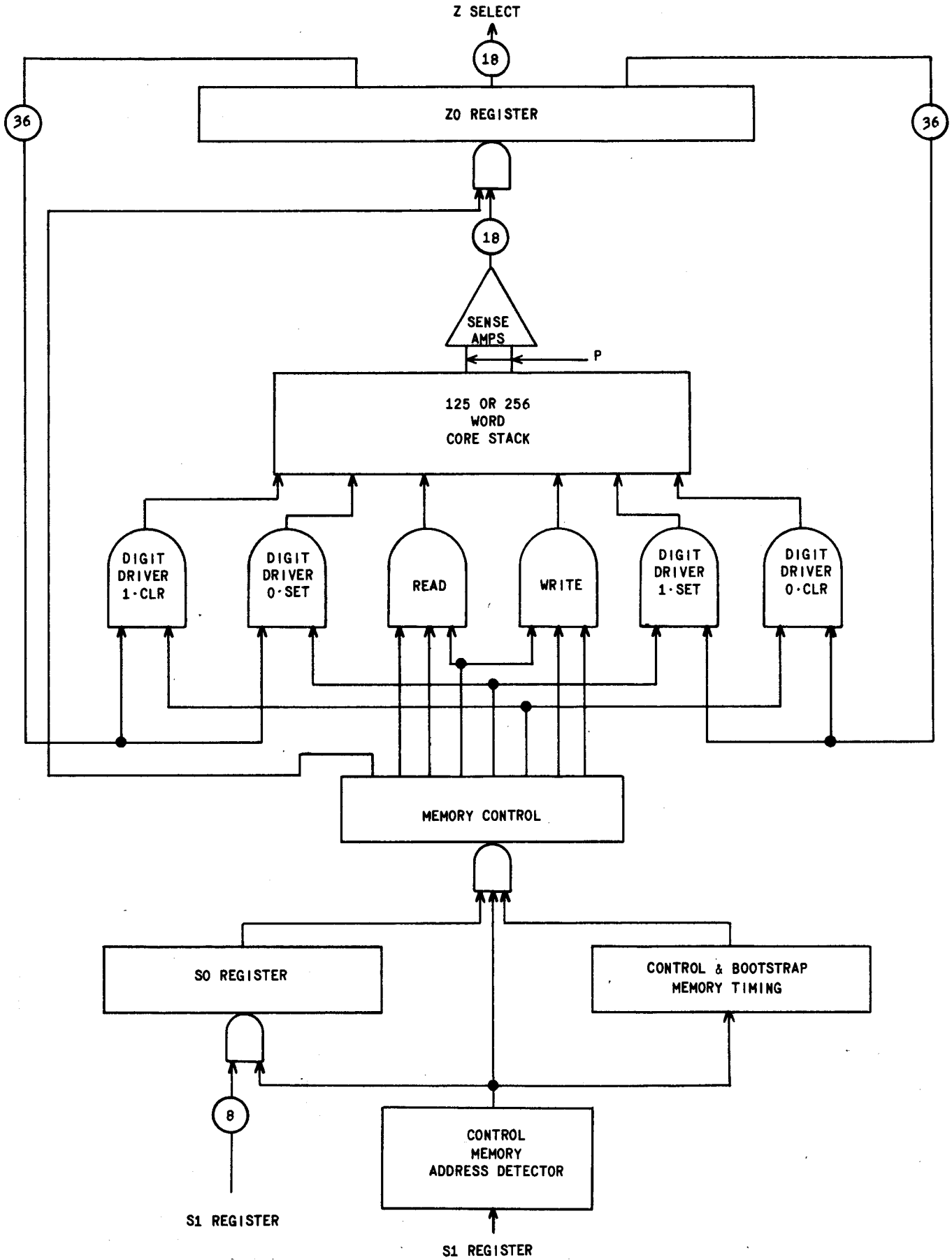


Figure 4-55. Control Memory, Functional Block Diagram

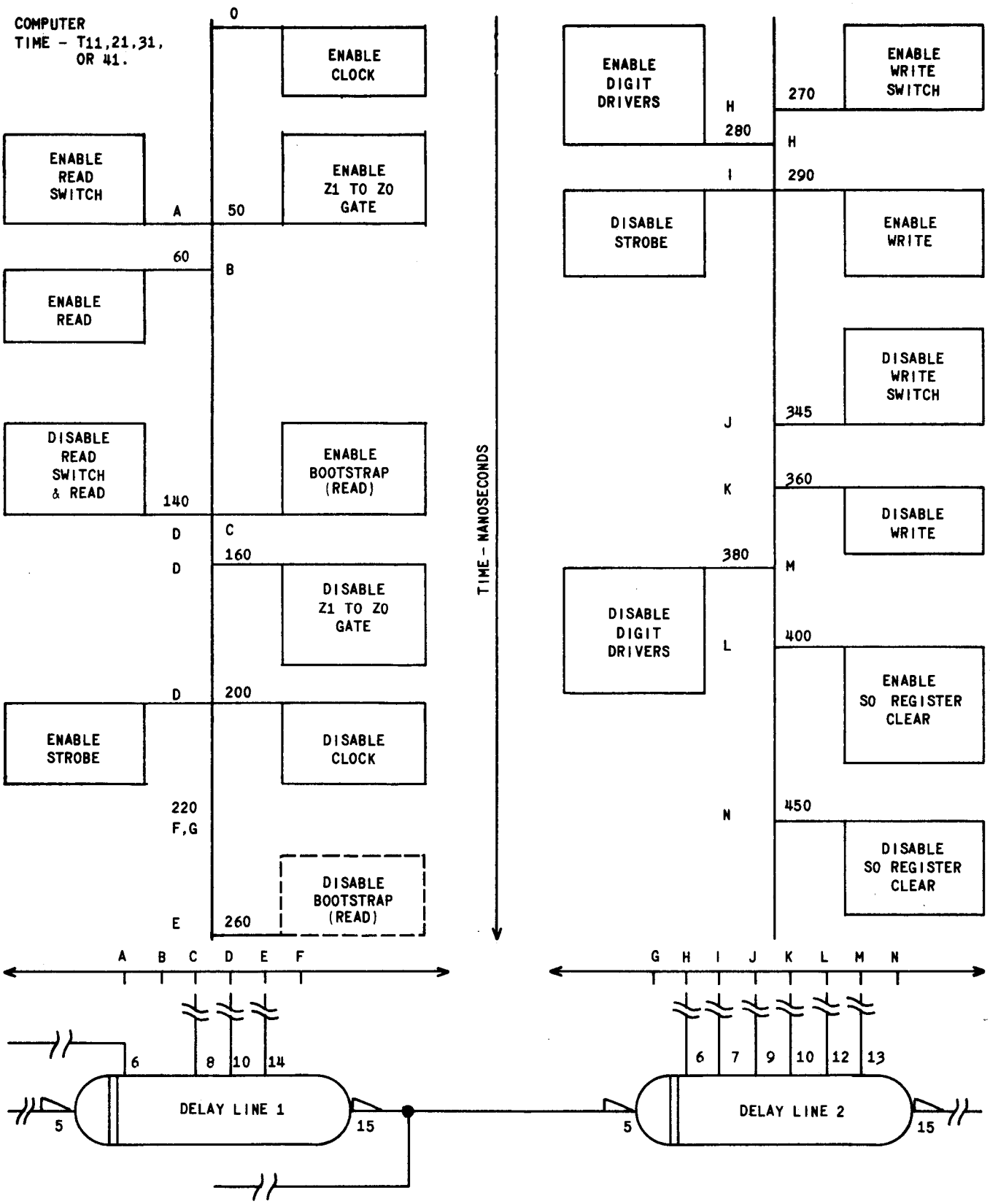


Figure 4-56. Control and Bootstrap Memory Timing - One Cycle

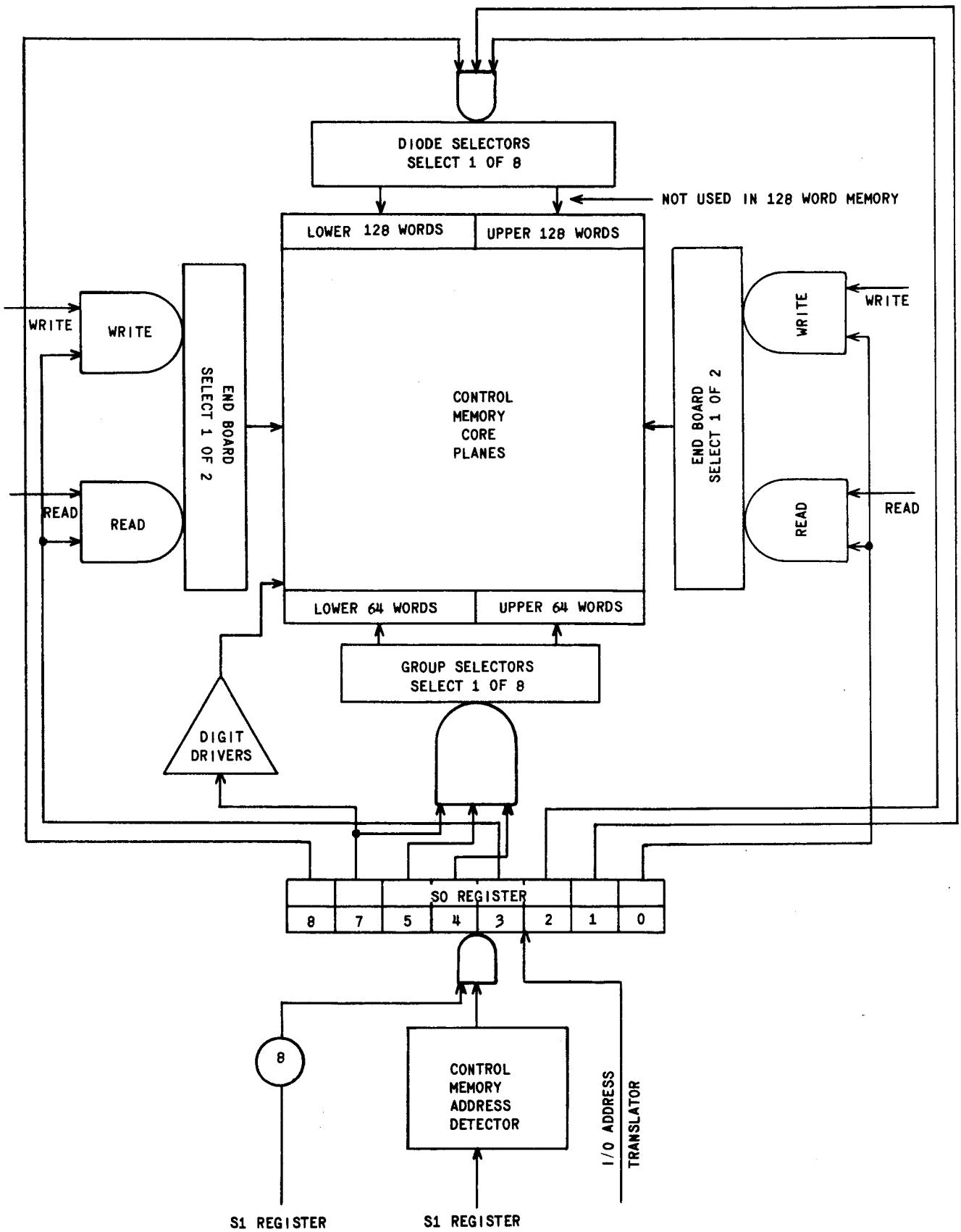


Figure 4-57. Control Memory Addressing

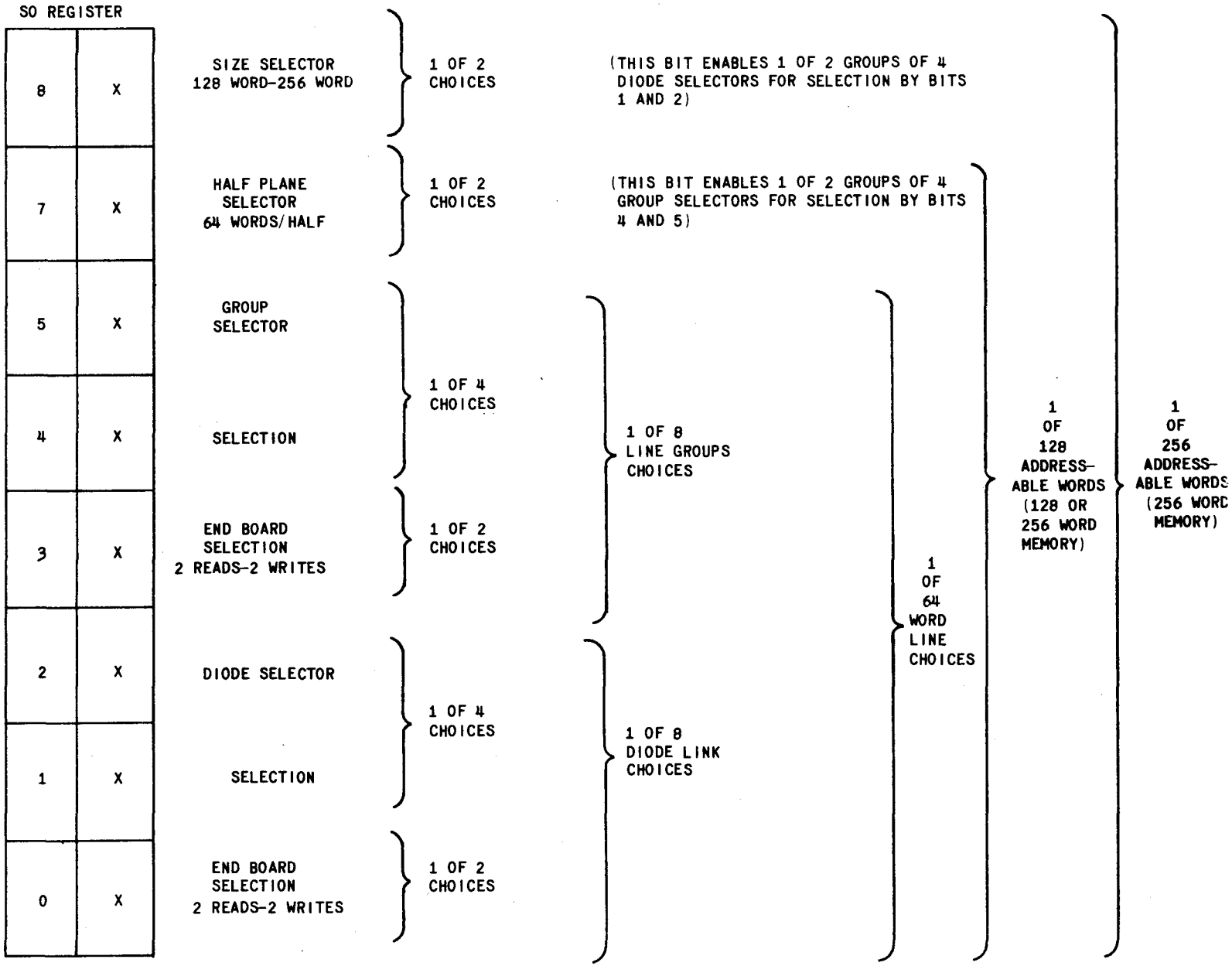


Figure 4-58. S0 Register Address Translation Scheme

In a half plane of 64 words, the translation is an eight-by-eight function. The necessary multiplication to achieve 64 possibilities is performed by the connecting word lines between translators. In control memory, eight word lines, one from each of the eight line groups, connect to a separate diode pair in one of the eight diode links, so that only one word line of a line group goes to a diode link. Thus, when the translators enable a line group and a diode link, only one of the 64 word lines is selected. By enabling only the translators for one of the two half planes, a choice of 128 words can be made; and by enabling only one of two possible core planes, a possible 256 different locations can be addressed.

(b) OPERATION. - Operation of control memory is conducted in two portions, read and write. Read operation takes the first half of memory cycle and write operation the second half. Unlike main memory, control memory is word-oriented; that is, only the magnetic cores of one memory location are strung on each word (read/write) line. Thus, during the read operation, only one line is pulsed. During write operation, the word line and all 18 digit lines are used, assuring proper combination of bits stored in the correct location.

The control memory uses the circuits shown in figure 4-59 to pulse word lines. When reading, the translating circuits enable a word driver in the opposite manner when writing, causing the direction of read current flow through the word lines to be opposite that of the write current.

1. BIT STORAGE. - Storage of information in the control memory is accomplished by using two magnetic cores for each word bit. One core is magnetized when storing a binary zero and the other is magnetized when storing a binary one. The control memory core plane, bit wiring (figure 4-60) shows the wiring configuration for a typical bit storage position for two words; one in the lower half plane and one in the upper half plane. A digit driver is connected to the digit line terminating at the top of the figure. A sense amplifier is connected to the sense line terminating at the bottom of the page. A word line passes twice, through 18 pairs of magnetic cores. Two passes through each core allows the use of one half the necessary current amplitude when switching the magnetic field of each core.

During a write operation, digit drivers are enabled according to binary value to be stored and the value of bit seven of the address to be used. For two such combinations, the digit lines carry current from terminal D00 to terminal D20; for the other two combinations, the current is reversed. Table 4-10 lists the combinations, current direction, enabled digit drivers, and cores which are magnetized.

Bit seven of the S_Q register specifies the difference between addresses 00000 through 00077 (bit seven clear) and 00200 through 00277 (bit seven set) for both size memories, and addresses 00400 through 00477 (bit seven clear) and 00600 through 00677 (bit seven set) in the large memory only.

2. READING. - Read operation is performed by passing the read current through all cores of the addressed word. The magnetizing force of the current causes all of the cores to be magnetized in the same direction. However, previous to the read operation, cores in each of the 18 core pairs were magnetized in opposite directions to each other. Therefore, one core was magnetized in the same direction as the read-current magnetizing force, and one core was magnetized in the opposite direction.

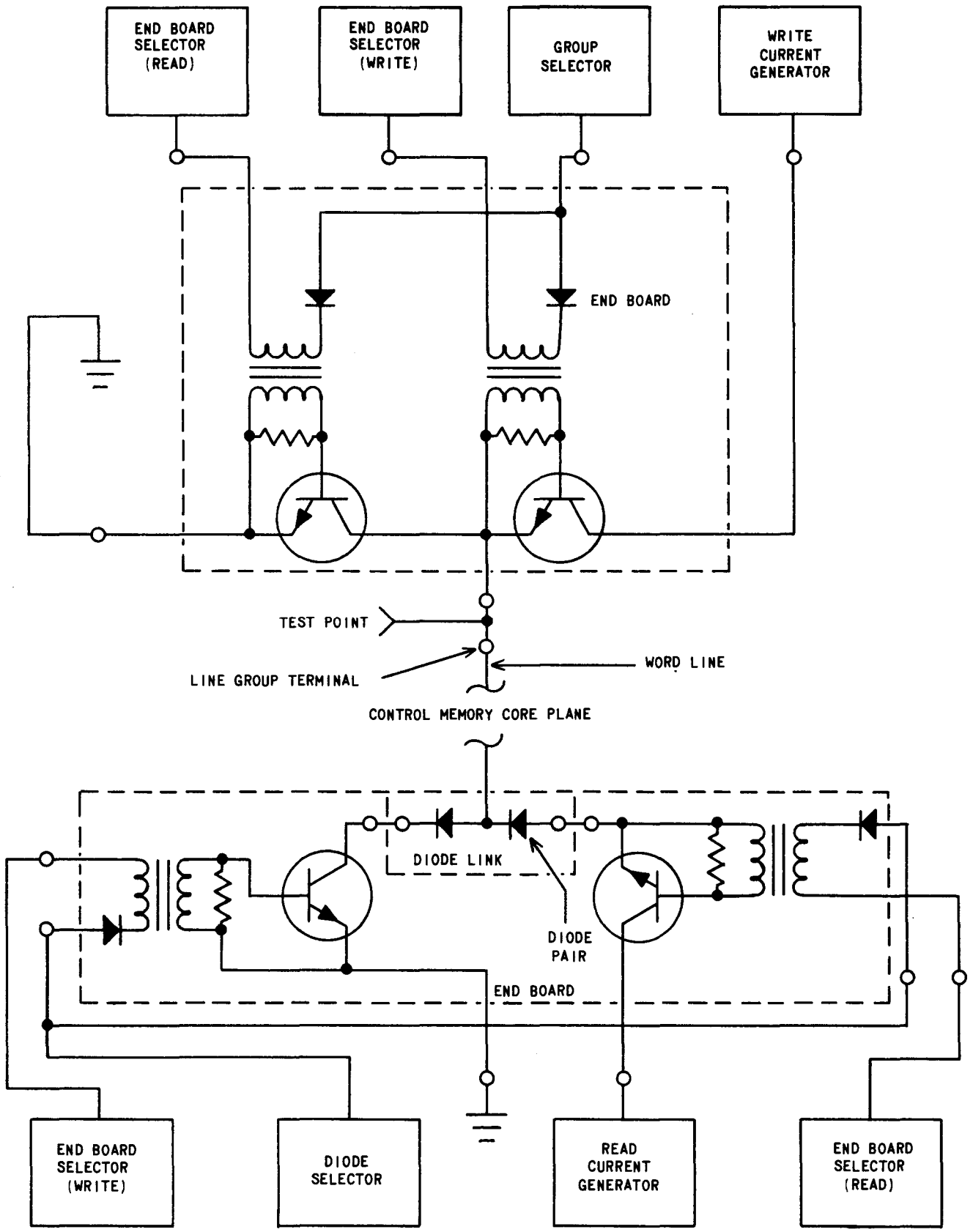


Figure 4-59. Typical Word Driver Circuit

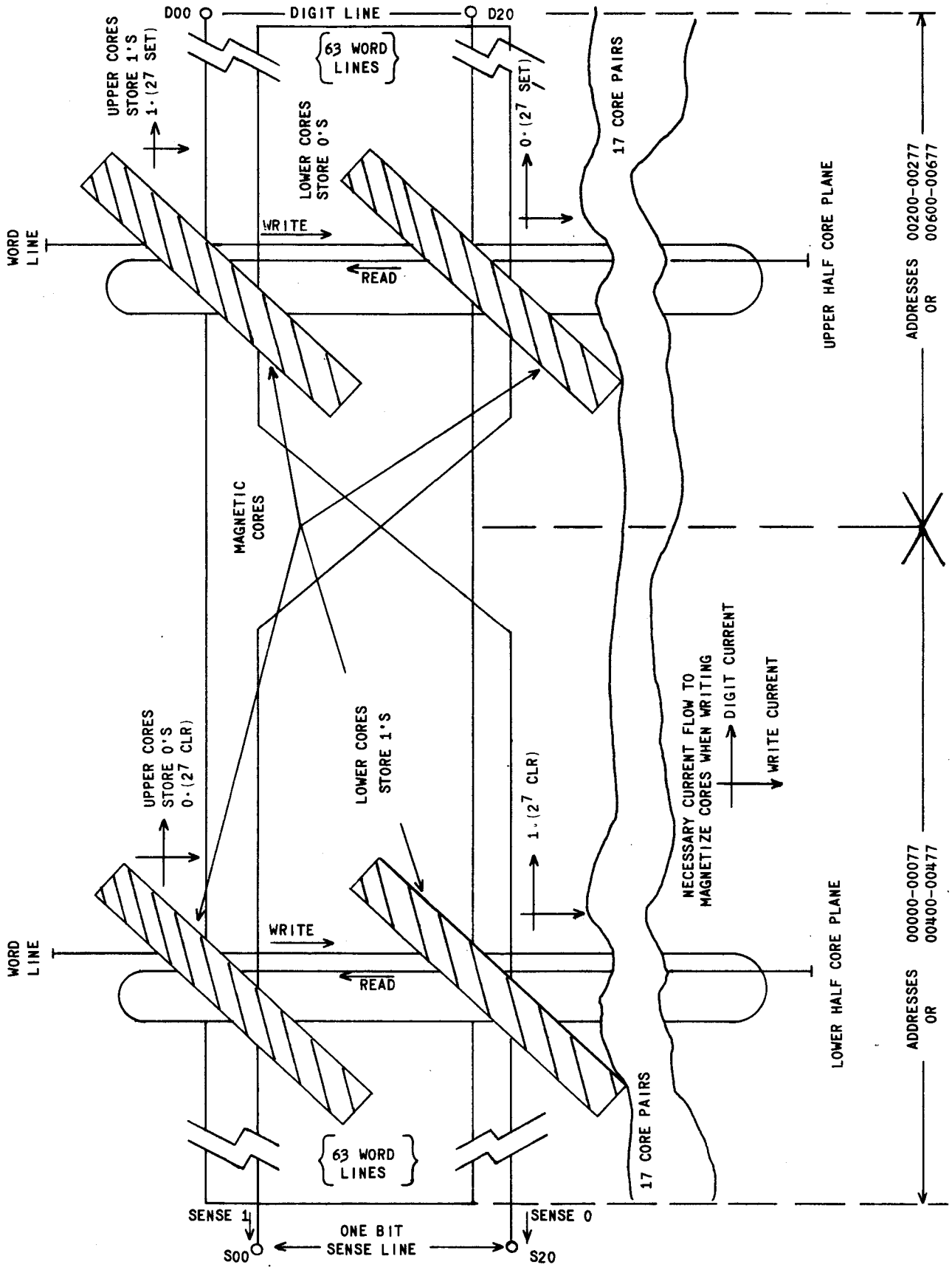


Figure 4-60. Control Memory Core Plane, Bit Wiring

TABLE 4-10. CONTROL MEMORY DIGIT OPERATION

TRANSLATION BINARY VALUE TO BE STORED	BIT 2^7 SO REGISTER	DIGIT DRIVERS ENABLED	CURRENT DIRECTION IN DIGIT LINES*		CORES AFFECTED
0	CLR	1ODDXX	D20	DOO	Lower half core Plane - Upper cores
	SET	OODDXX	DOO	D20	Upper half core Plane - Lower cores
1	CLR	OODDXX	DOO	D20	Lower half core Plane - Lower cores
	SET	1ODDXX	D20	DOO	Upper half core Plane - Upper cores

As read-current passes through a core pair, it enhances the magnetic field of one core, destroys the old magnetic field, and establishes a new magnetic field in the other core. Collapsing of one magnetic field and building of another induces a current in the sense line of that bit pair (figure 4-60). The sense line for each bit is strung through the 128-word core plane so that upper cores of the lower half plane and lower cores of the upper half plane, which store binary zeros, cause DOO through $D17_8$ terminals to go positive when switched by the read current. The other cores, which store binary ones, cause D20 through $D37_8$ sense-line terminals to go positive when read. When a binary one is sensed, the two-stage sense amplifier provides a low signal which is gated by the strobe and sets the corresponding flip-flop in the Z_0 register.

3. WRITING. - Write operation is performed by passing the write and digit current through all cores of the addressed word. However, direction of the digit current depends upon binary value to be stored at that bit position, (figure 4-60). It is easier to assume that two magnetizing forces of the write and digit current add at one core of a core pair to store the desired information; actually, they subtract at the other core to prevent its magnetic field from switching because the magnetizing force of the write current is sufficient to switch the cores by itself.

(4) BOOTSTRAP MEMORY. - The computer design incorporates provisions to effectively provide two 32-word (18 bits per word) bootstrap programs. The first of these two programs is a permanently wired, word-oriented core memory containing a non-destructive readout with a cycle time of 2 microseconds. The second of these programs is contained in main core memory and is identical to other main memory storage locations in capabilities and limitations. Either bootstrap is selected by the BOOTSTRAP MODE switch located on control panel two located on drawer A4. The two positions of this switch are NDRO and MAIN MEMORY.

(a) NDRO. - In the NDRO position, the permanently-wired bootstrap program, designed at the time of manufacture, contains a program consistent with the customer's requirements, and is referenced by the computer load routine.

(b) MAIN MEMORY. - In the MAIN MEMORY position, reference to the bootstrap program directs the program to the main memory, which is subject to the limitations of a normal core memory. Main memory addresses are identical to the NDRO memory. These addresses are 00500 through 00537.

The bootstrap mode switch (figure 9-107) in the NDRO position provides one enable to set the BOOTSTRAP flip-flop 0XS09. The output from this flip-flop, L → Enable Bootstrap, directs the address in the S_0 register to the permanently-wired bootstrap program at addresses 00500-00537. When the switch is in the MAIN MEMORY position, the flip-flop is not enabled and remains cleared. The resulting disables enable the $S_0 \longrightarrow S_1$ transfer and reference, through the S_1 register, addresses 00500 - 00537 in the main core memory.

By using this operation, 32 additional addresses are made available through the BOOTSTRAP MODE switch.

The main memory bootstrap program is identical to normal main memory operation, so refer to the main memory explanation for this operation. The following explanation for this operation. The following explanation covers only the NDRO bootstrap memory and is referred to as bootstrap memory.

The bootstrap program, is a short-load routine that transfers beginning instructions of a more complex load and operational program into the memory addresses specified by the bootstrap. Once the bootstrap program has been completed, the computer performs the functions of the newly loaded routine, which completes the transfer of all information and instructions for an operational program into the computer memory. The operation of the bootstrap program, since it involves I/O operations, is contingent upon preparation of the peripheral device for a load operation.

Bootstrap memory is addressed automatically during two operations of the computer: load mode and automatic recovery (if a fault is detected). The load mode forces the computer to address 500_8, which is the first address of the bootstrap memory, and is used for initial loading of operational programs. Whenever an instruction fault is detected, the fault logic forces the computer from the run mode into the load mode if the AUTO RECOVERY switch is in ON position.

Bootstrap memory operation is shown in figure 4-61. When bootstrap memory address detector finds any value in the S_1 register between 500 and 537, it enables the timing and control portions of the memory and gates the address in the S_1 register into the SO register. Translation of the address in the S_0 register by the eight line group selectors and four diode group selectors pulses the proper word line in permanent memory. Selecting the line causes the addressed word to be read and then gated by the strobe signal into the Z_0 register.

Since the NDRO memory does not require a write cycle, the timing is very simple. The strobe for the bootstrap memory is the same as for the control memory. The starting time for the bootstrap memory, referenced to computer time, is T21 when in the load mode and any phase one if a voltage fault is detected.

1. ADDRESSING. - The bootstrap memory uses a 4 X 8 selection scheme to find the addressed word out of the 32 possible words (see figures 9-132 and 9-133). There are four diode group selectors; each selector translates bits 03 and 04 in

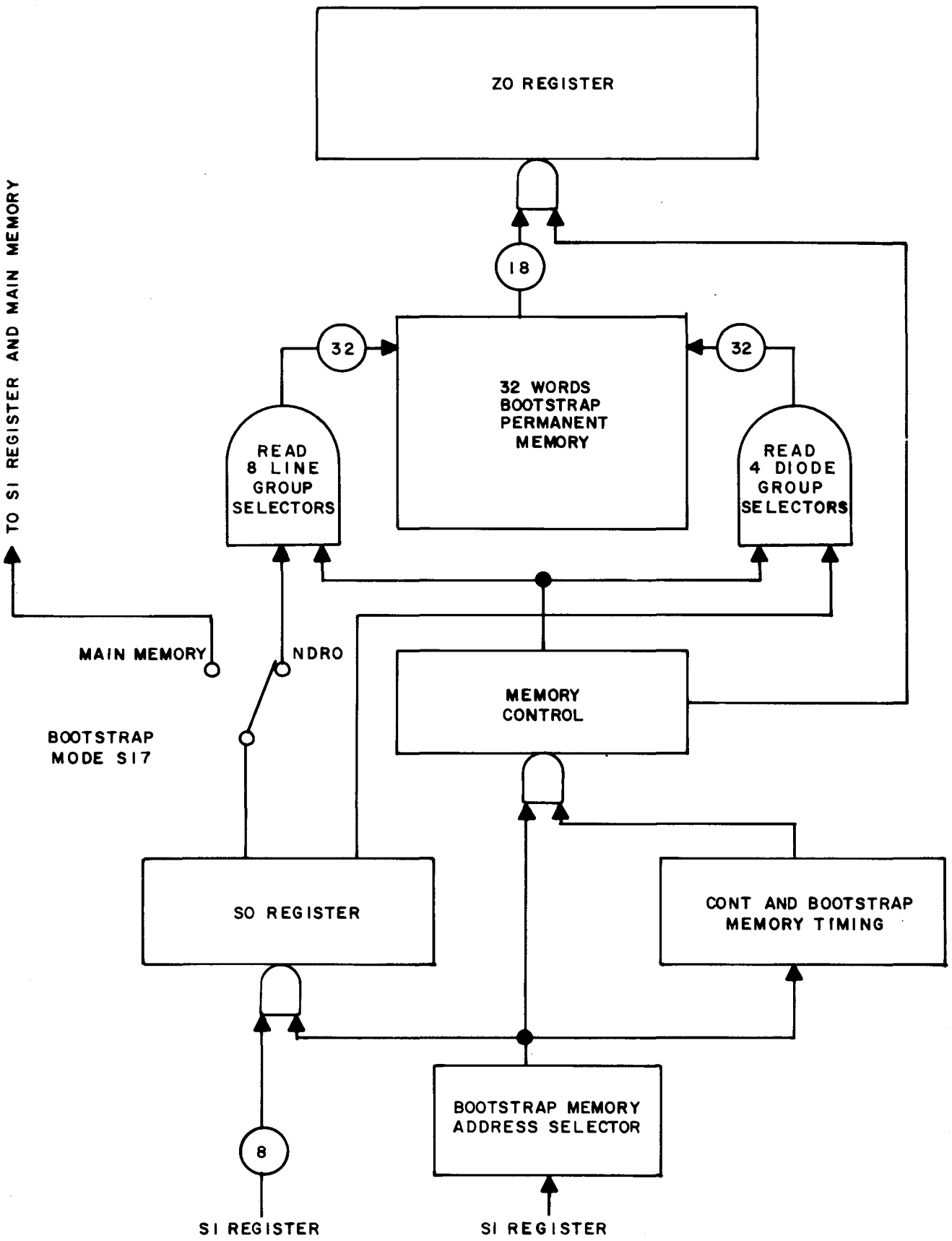


Figure 4-61. Bootstrap Memory, Functional Block Diagram

the S_0 register for one of the four possible combinations. There are eight line group selectors; each selector translates bits 00 through 02 in the S_0 register for one of the eight possible combinations. Each of the eight line group selectors have four separate word lines which are connected, one to each of the four diode group selectors. Therefore, only one of the 32-word lines connects a line group selector with a diode group selector. When the translations are performed, one line group selector and one diode group selector are enabled; thus, the word line between the selectors is pulsed.

2. OPERATION. - Unlike the operation of the other two memories, the bootstrap memory requires only a read operation to function because its construction establishes the contents of each memory location. The memory is designed as a word-oriented device with 32-word lines strung through 18 positions which establish the binary value of each of the 18 bits (see figure 9-133). The 18 positions each consist of two holes in a circuit board, one of which has a magnetic core around it. There are three circuit boards, each having six bit positions.

The 32-word lines are passed through one of the two holes for each of the 18 positions. If the binary value for that bit is a one, the line is passed through one hole of the magnetic core; if it is a zero, the line is passed through the other hole.

The word line passing through a magnetic core acts as the primary winding of a transformer. Windings around the magnetic core itself act as the secondary winding of a step-up transformer. When the word line is pulsed, the magnetic cores with the line passing through them transfer an amplified pulse to the associated bit sensing positions. These positions provide signals that are gated by the strobe into the Z_0 register by setting the corresponding flip-flops.

4-3. POWER SUPPLIES AND POWER DISTRIBUTION.

a. GENERAL. - Power for the computer logic is supplied primarily by the power supply located in the cabinet area designated as PS1. (See figure 1-18.) An additional power supply, located in memory drawer A3, supplies power for operation of the memory circuitry. Each supply provides several voltage outputs. Power control panel A5 contains major controlling switches and indicators, which provide a visual indication of computer power conditions. Schematic diagrams, which relate to the power supply, control, and distribution, are contained in figures 9-176 through 9-180.

b. POWER INPUT. - The computer requires an input power with characteristics as listed in table 1-4. Power is applied through a single four-conductor cable to the line filters FL1, FL2, and FL3 as shown in figure 9-177. Power is applied from these filters to fuses F8, F9, and F10 on figure 9-178 and from the fuses to the contacts of the power control relay K1. A simplified schematic diagram of the power control circuit is shown in figure 4-62. Interlock switch A12S1 is located on the rear of the power supply PS1 and breaks the input power circuit when the power supply drawer is extended. The temperature sensing switch (S3) is located on the cabinet interior (see figure 6-7) and opens the input power circuit if the temperature within the cabinet exceeds 140 degrees F (60 degrees C). The POWER switch (S4) is located on the power control panel. This switch is a spring-loaded, two-position toggle switch and is shown in figure 4-62 in the center position. Momentarily setting the switch to the ON position energizes K1. The holding circuit for K1 is supplied through one set of relay contacts and through the POWER switch. Setting the switch to OFF position interrupts the holding circuit to remove power from the power supply.

c. MAIN DC POWER SUPPLY. - The main dc power supply, located in PS1 and shown in figure 9-178, generates the dc power required for general logic operation. Circuitry is composed of three basic supplies and furnishes -4.5, -15.0, and +15.0 dc volts. Through transistor control, a regulated +25.0 and -25.0 volts are provided for control memory operation.

d. MAIN MEMORY POWER SUPPLY. - The main memory power supply, located on chassis A3A2 and shown in figure 9-179, produces voltages unique to memory operation. Output voltages from this supply are +3.0, -3.0, +6.0, -4.5, +15.0, and -15.0 dc volts. These voltages are regulated through CR9, CR10, CR11, and voltage regulator circuit 00VR03.

e. POWER DISTRIBUTION. - DC power from PS1 is distributed throughout computer logic through bus bars mounted on the main frame on the rear of the cabinet to pins 1 through 4 of the 15-pin printed circuit modules. Power from the main memory power supply is distributed through bus bars on the memory chassis to various pins as required on the 56-pin printed circuit modules.

f. MISCELLANEOUS CIRCUITS.

(1) RUNNING-TIME METER. - A running-time meter (M1 on figure 9-176) records total time that power is applied through relay K1 to the computer supplies.

(2) FAULT HORN. - The fault horn (LS1) provides an audible indication of a program, voltage, loss of air, or temperature fault. It is located on the power control panel.

4-4. COMMAND TIMING.

a. GENERAL. - This portion of the manual provides a detailed analysis of computer operation during execution of each instruction in the computer repertoire.

The information on command timing is divided into command sequences, and the timing for each instruction.

b. COMMAND SEQUENCES. - There are four types of command sequences employed by the computer. Command sequences are listed and defined as follows:

1) I - Instruction sequence: reads instruction from memory.

2) R1 & R2 - Read sequences: reads operand from memory.

3) W - Write sequence: writes operand into memory.

4) B1 & B2 - Buffer sequences: controls loading of buffer control words and activating of an I/O channel.

Command sequences are selected by the sequencer in a predetermined order necessary for proper instruction execution. The main timing chain, operating in conjunction with the sequence destination and the master clock, develops the 16 timing pulses

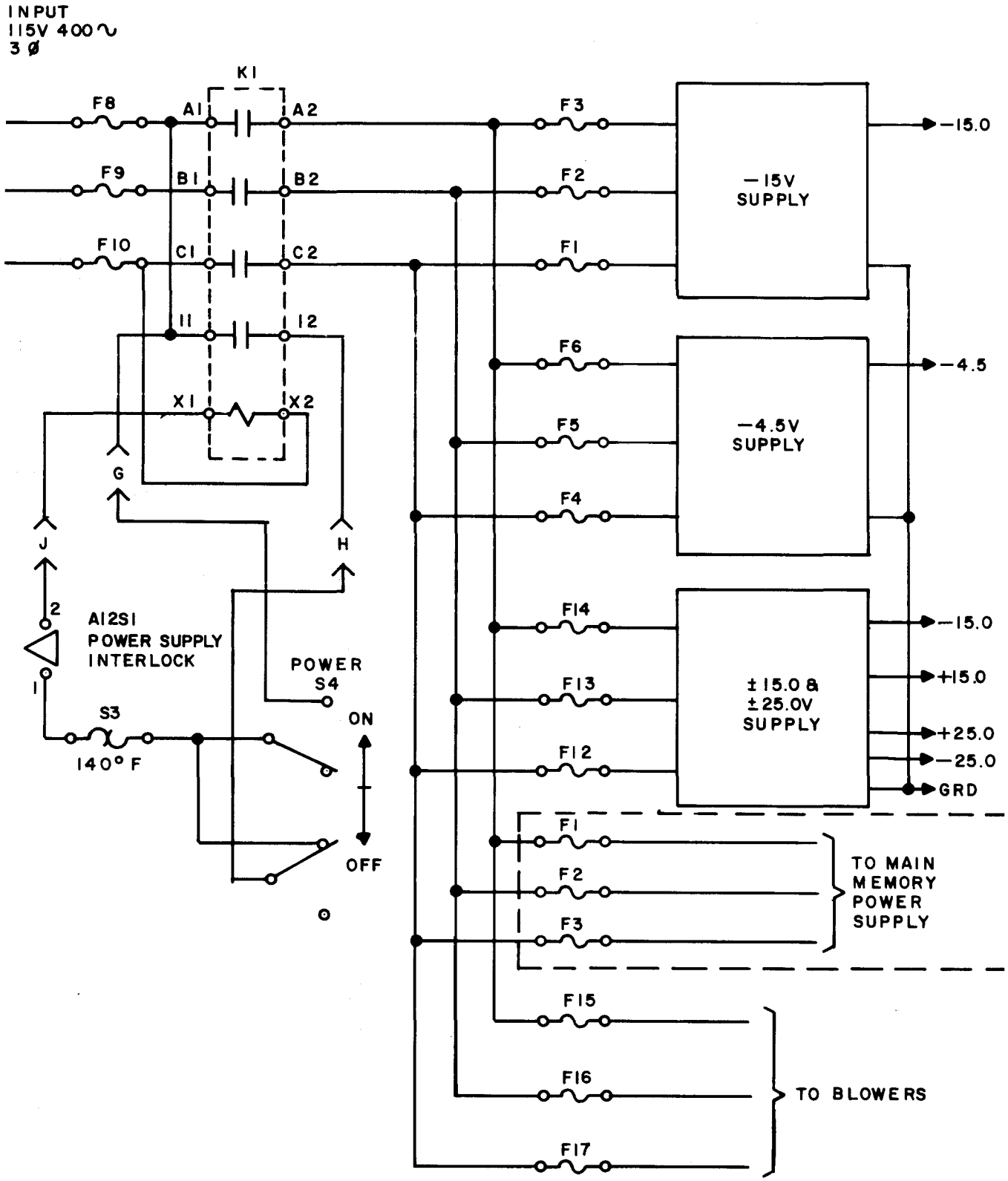


Figure 4-62. Power Control Circuit, Simplified Diagram

(4.4, 1.1, 1.2, 1.3, 1.4, 2.1, ..., 4.3) necessary to synchronize computer operation during the selected sequence. Not all command sequences are required to execute an instruction. In some cases, only one sequence (I) is necessary; in others, three sequences may be required for complete instruction execution. Refer to paragraph 4-4c, which lists each instruction with the applicable command sequences and the command sequence tables.

Command sequences of each instruction are listed in abbreviated form in table 4-11.

Command sequence tables contain a phase-by-phase analysis of functions performed during each command sequence. The notation along the left-hand margin of each sequence reflects internal computer timing in terms of cycle and phase time. Following each time notation is a list of commands performed at that time in the sequence. The expression in the third column following certain functions indicates a condition or conditions necessary to perform or not perform those functions.

Absence of an expression in the condition column indicates that the function is performed unconditionally.

For example, the entry T2.2 Memory $\longrightarrow$ Z1 in the I sequence is read: At 2.2 time, contents of the addressed memory location are unconditionally transferred into the Z1 register. The entry, T3.3 - AL $\longrightarrow$ Arithmetic Selector - f = 71, is read: At 3.3 time of instruction 71, the contents of the AL register are transferred to the arithmetic selector.

(1) I SEQUENCE. - I sequence (table 4-12) is the first sequence performed during the execution of every instruction. During the I sequence, the instruction word is addressed, read out of memory, and initially operated upon.

(2) R1 and R2 SEQUENCE. - R sequences (tables 4-13 and 4-14) are used in instructions where it is necessary to obtain contents of a given memory address to complete the instruction.

(3) W SEQUENCE. - W sequence (table 4-15) is used to write the results of an instruction into a specified memory location.

(4) B SEQUENCE. - B sequences (tables 4-16 and 4-17) are used to transfer the two words in memory locations immediately following the 50:11 through 50:13 instructions into the proper control memory location, and set the active flip-flop for the proper operation and channel.

c. INSTRUCTION TIMING. - This portion of command timing provides a detailed analysis of each instruction in the repertoire. Instructions are arranged in ascending numerical order by octal code starting with Format I instruction 00. The Format II instructions, 50:00 through 50:77, follow Format I instruction 77.

The description of each instruction contains the following:

1) Octal code of the instruction.

2) Name of the instruction.

3) Time required for execution.

4) A listing of the main command sequences employed in its execution and the order in which the sequences are performed.

5) Detailed analysis of the multiply, divide, shift, and scale sequences, where applicable.

TABLE 4-11. COMMAND SEQUENCES OF EACH INSTRUCTION

I SEQUENCES ONLY		
00	50:03	50:51
01	50:14	50:52
34	50:15	50:53
35	50:16	50:54
60	50:17	50:55
61	50:20	50:56
62	50:21	50:57
63	50:22	50:60
64	50:23	50:61
65	50:30	50:62
66	50:31	50:63
67	50:32	50:72
70	50:33	50:73
71	50:34	50:74
73	50:35	
77	50:36	
50:01	50:37	
50:02	50:50	

I AND R1 SEQUENCES		
02	12	33
03	13	51
04	14	52
05	15	53
06	16	54
07	17	55
10	32	56
11		

I, R1, AND R1R2 SEQUENCES
20
21
22
23

I AND EXTENDED SEQUENCES		
50:41	50:43	50:46
50:42	50:45	50:47

I, R1, AND EXTENDED SEQUENCES
24
25
26
27

I AND W SEQUENCES	
40	46
41	47
42	72
43	74
44	75
45	76

I, EXTENDED, AND W SEQUENCE
50:44

I AND WAIT SEQUENCES
50:24
50:25

I, R1, AND W SEQUENCES
30
31
57

I, IB1, AND IB2 SEQUENCES		
50:11	50:12	50:13
I, I/O 1, and (if Dual or ESI term) I/O 2		
50:26	50:27	

TABLE 4-12. I SEQUENCE

TIME	COMMAND	CONDITION
T4.4	Clear Channel and Function Priority Clear S1	
T1.1	Special Interrupt Register → S1 P → S1 Set RESUME flip-flop Clear AL 500_8 → S1 Enable Main Memory I/O Translator → S0 ICR → S0 Initiate Control Memory Set INCREMENT P flip-flop Clear P Register CLR Z0 Data Request → Chan Priority Translator → (S1 bits 4,5,and 7)	Int Sequence • Special Interrupt Normal Sequence f = 50:20 f = 50:61,63•T52 Load Mode f = 50:11-50:13 f = 32, 33, 36, 37, 56•$\overline{\text{Equal}}$, 73•B ≠ 0 f = 32, 33, 36, 37, 56•Equal, 73•B ≠ 0, 50:11-50:13 Not Int Sequence Load Mode Int Sequence•$\overline{\text{Spec Int}}$ or Cont Data Sequence
T1.2	Adder → AL B-1 → Z0 S1 → P Z1 → Z0 B+1 → Z0 Set RUN 1 flip-flop	f = 50:61, 63•T52 f = 73•B ≠ 0 Load Mode f = 50:11-50:13, 32, 33, 36, 37 f = 56•Equal RUN 1 flip-flop set
T1.3	Clear Z1 Clear D, Clear X, Clear W Clear HOLD-2 flip-flop Clear PARITY flip-flop Clear Select Stop flip-flops Inhibit Control Memory → Z0 Clear EF/OD ACK GEN flip-flop Clear F Register Clear MON and Special INT REG flip-flops	INCREMENT P flip-flop set HOLD 1 Cleared f = 73•B ≠ 0, 56•$\overline{\text{Equal}}$, 50:11-50:13, 32, 33, 36, 37 ACK DELAY flip-flop $\overline{\text{set}}$ Interrupt Sequence

TABLE 4-12. I SEQUENCE (CONT.)

TIME	COMMAND	CONDITION
T1.4	Set INHIBIT EAB flip-flop	INCREMENT P flip-flop set
	PL ⟶ DL	
	PU ⟶ DU	INCREMENT P flip-flop set
	Set PARITY flip-flop	Parity Odd
	Clear KO	
	Set DECREMENT P flip-flop	Force•Resume Fault
	Set INSERT EAB flip-flop	Decrement P flip-flop set
	Data Req ⟶ Function Priority	
	Set ALL INT LOCKOUT flip-flop	Interrupt Sequence
T2.1	CLR Translator	$\overline{\text{I/O}}$
	S1 ⟶ SO	S1 = Control or Bootstrap Mem Address
	Clear Sequence Designator, Lower Rank	RUN•I/O•HOLD 1
	Clear CONT DATA SEQ and RTC SEQ flip-flops	
	Clear P Register	
	Set BOOTSTRAP flip-flop	Load Mode
	Clear ZO	CONT DATA Seq
	Set RESUME flip-flop	EF/OD ACK
T2.2	CLR CLEAR HOLD flip-flop	Force•$\overline{\text{DECREMENT P}}$
	Sequence Designator Upper Rank ⟶ Lower Rank	RUN•I/O•HOLD 1
	Memory ⟶ Z1	
	Adder ⟶ P	
	Req ⟶ Translator	$\overline{\text{I/O + FORCE + RTC Seq.}}$
	Set RTC Seq flip-flop	RTC Advance
T2.3	Clear EAB flip-flops	
	O's ⟶ Arithmetic Selector Bits 12-17	$\overline{\text{Initiate Buffer}}$
	Z Select ⟶ Arithmetic Selector Bits 00-17	
	Clear D, Clear X, Clear W	
	Z ⟶ Z Select	
T2.4	Arithmetic Selector ⟶ D	
	Z Select Bits 00-05 ⟶ KO	$\overline{\text{I/O Sequence}}$
	Z Select Bits 12-17 ⟶ F	f = Format I
	Z Select Bits 06-11 ⟶ F	f = Format II
	Clear Main Memory Enable flip-flop	
	Arithmetic Selector ⟶ X	Initiate Buffer
	Arithmetic Selector ⟶ X	Initiate Buffer
T3.1	INT REG CHAN PRIO	I/O
	ICR ⟶ SO	
	Initiate Control Memory	
	Clear SKIP flip-flop	
	Clear I/O Translators	f = 50:00-23, 50:26-37
	CLR ZO	
	Set RESUME FAULT flip-flop	RTC Seq and B = 1024

TABLE 4-12. I SEQUENCE (CONT.)

TIME	COMMAND	CONDITION
T3.2	Set SKIP flip-flop	Skip to be executed
	F and K ⟶ I/O Translator	f = 50:00-23, 50:26-37
	CLR B	
T3.3	AU ⟶ Arithmetic Selector	f = 50:60, 62, 63
	AL ⟶ Arithmetic Selector	f = 71
	Z Select ⟶ Arithmetic Selector	f = 00-47 and Odd
	Clear D Register	f = 50:21-23, 50:55, 57, 60, 62, 63
	Clear ICR Register	f = 50:72
	Clear SR Register	f = 50:73
	Set RTC MON SEQ flip-flop	f = 50:14
T3.4	Arithmetic Selector ⟶ D	f = 50:60
	Arithmetic Selector ⟶ D	f = 50:62, 63
	P ⟶ D	f = 50:21-23, 50-55, 57
	Set INHIBIT EAB flip-flop	f = 50:21-23, 50-55, 57
	Set DU6 (sign Extension)	f = 36, 37, 70, 71 and -D Lower 12 are negative
	INT REG ⟶ Function Priority	$\overline{I/O}$
	ZO or input ⟶ B	
	Set HOLD 1 flip-flop	f = 50:26, 27, 40-47
	SR ⟶ D12-15	f = 00-27, 32, 33, 40-47 and SR is active
	PU ⟶ DU	f ≠ 36, 37, 70, 71 and SR is not active or f = 30, 31, 34, 35, 50:21-23, 50-55, 57, Int, I/O or Hold 2
	Set EXT INT LOCKOUT flip-flop	f = 50:36, 37
	CLR EXT INT LOCKOUT flip-flop	f = 50:32, 33
	Arithmetic Selector ⟶ X	
	AL ⟶ Arithmetic Selector	f = 71
	Arithmetic Selector ⟶ X	f = 50:60-63
	Set INHIBIT EAB flip-flop	f = 50:60 and AU17 ≠ AL17 or 50:21-23, 50-55, 57
	Set INSERT EAB flip-flop	f = 50:60 and AL is positive
	Set ALL INTERRUPT LOCKOUT flip-flop	f = 31, 54, 76 or 51:31
	Clear ALL INTERRUPT LOCKOUT flip-flop	f = 50:34, 35
	Sample Selective Stops	f = 50:56
	K00 - K02 ⟶ ICR	f = 50:72
	K00 - K02 ⟶ SR	f = 50:73
	Set INST FAULT flip-flop	f = 00, 01, 77
	Clear SCALE FACTOR flip-flop	f = 50:40-47

TABLE 4-12. I SEQUENCE (CONT.)

TIME	COMMAND	CONDITION
T4.1	Enable Shift Sequence	f = 50:40-47
	Clear RUN flip-flop	STOP exists
	Clear Sequence Designator, Upper Rank	
	Select RUN Mode	Load Mode
	Clear AU Register	f = 50:62, 63
	Clear AL Register	f = 70, 71, 50:60
	Clear P Register	f = 50:21-23, 50-55, 57 and SKIP or f = 34, 35, 60-67, 73 and JUMP
	Clear ZO Register	Cont Data Sequence
	Clear B±1 flip-flop	
	Clear I/O Translator	f ≠ I/O INSTRUCTIONS
	Clear COMPARISON DESIGNATORS	f ≠ 60-67
T4.2	Set RUN flip-flop	Start or Op Step
	Set WAIT flip-flop	f = 50:24, 25
	Set B1 Seq flip-flop	f = 50:10-13
	Set W Seq flip-flop	f = 50:40-47, 72, 74-76
	Set R1 Seq flip-flop	f = 50:02-33, 50-57
	Set I Seq flip-flop	f = Format I, Spec Int. Fault
	Adder ⟶ AU Register	f = 50:62, 63
	Adder ⟶ A1 Register	f = 70, 71, 50:60
	Adder ⟶ P Register	f = 50:21-23, 50-55, 57 and SKIP or f = 34, 35, 60-67, 73 and JUMP
	Translator 1 ⟶ Translator 2	I/O Sequence
	Set B±1 flip-flop	f = 73 or I/O Sequence·Backward Buffer
	CLR A NEG and Y NEG flip-flops	
	Clear HOLD 1 flip-flop	CLEAR HOLD flip-flop is set
	Set OVERFLOW flip-flop	f = 71, X and D are positive, and no borrow from 17 or f = 71, X and D are negative, and borrow from 17
	Requests-Translator	I/O Sequence
	Enable ID or EF/OD Ack Req.	I/O Sequence
T4.3	Set HOLD 2 flip-flop	HOLD 1 flip-flop set
	Clear INHIBIT AND INSERT EAB flip-flops	
	Set SPEC INT TRANS flip-flops	Inst. Fault
	Enable Memory Protect	Voltage Fault and no Battle Short
	Clear D Register	f = 50:61, 63
	Clear Z1 Register	f = 36, 37
	Clear TERMINATE flip-flop	
T4.4	CLR ACTIVE flip-flop	f = 50:15-50:17
	AL ⟶ Arithmetic Selector	f = 50:61, 63
	Arithmetic Selector ⟶ D	f = 50:61, 63
	Adder ⟶ Z1	f = 36, 37
	Clear OVERFLOW flip-flop	f = 50:52, 53
	Set TERMINATE flip-flop	B ≠ Z0 or B16 and B17 ≠ Z016 and Z017

TABLE 4-12. I SEQUENCE (CONT.)

TIME	COMMAND	CONDITION
T4.4 (Cont.)	Clear S1 Register	
	Set ACTIVE flip-flops	f = 50:01 - 50:03
	Set CONT DATA SEQ flip-flop	I/O Sequence·TERM·CDM Bit Set

TABLE 4-13. R1 SEQUENCE

TIME	COMMAND	CONDITION
T4.4	CLR S1	
T1.1	Adder → S1	
	ICR → S0	f = 56
	Initiate Control Memory	f = 56
	Enable Main Memory	
	CLR Z0	
T1.2		
T1.3	CLR X, W	f ≠ 57
	Control Memory → Z0	f = 56
	CLR D	f = 04, 05, 24-27, 53
	Set A NEG flip-flop	f = (24,25) and AL NEG or (26,27) and AU NEG
T1.4	AL → Arithmetic Selector	f ≠ 02, 03, 06, 07, 14-17, 20-23·$\overline{R2}$, 24, 25, 44, 45, 53, 74
	AU → Arithmetic Selector	f = 04, 05, 06, 07, 26, 27, 46, 47
	Z → Arithmetic Selector	f = 56
	Arithmetic Selector → X	f ≠ 24-27
	Arithmetic Selector → D	f = 04, 05, 24-27, 53
	CLR K0	
	Scale Factor Count → X	f = 50:44
	0's → Arithmetic Selector Bits 12-17	f = 40, 41, 72, 75 · 74
T2.1	CLR AU	f = 24, 25 or A NEG
	CLR AL	f = (24,25) and AL NEG
	Set K0 to 18	f ≠ X4, X5
	Set K0 to 19	f = X4, X5
T2.2	Adder → AL	f = (24,25) and A NEG
		f = ($\overline{24,25}$) and A NEG
T2.3	CLR D	f ≠ 04, 05, 53
	CLR INHIBIT and Insert EAB	
T2.4	Set Inhibit EAB	f = 20-23
	AL → Arithmetic Selector	f = 52
	AU → Arithmetic Selector	f = 06, 07
	Z1 → Arithmetic Selector	

TABLE 4-13. R1 SEQUENCE (CONT.)

TIME	COMMAND	CONDITION
T2.4 (Cont.)	Set Y NEG flip-flop	f = (24-27) and Y NEG
	Arithmetic Selector ⟶ D	f ≠ 02, 03, 06, 07, 16, 17, 22, 23, 53, 56 or f = (24,25) and Y POS for f = (26,27) and Y NEG
	$\overline{\text{Arithmetic Selector}}$ ⟶ D	f = 02, 03, 06, 07, 16, 17, 22-27, 53, 56 or (24,25) and Y NEG or f = (26,27) and Y POS
	Arithmetic Selector ⟶ X	f = 53
T3.1	ICR ⟶ SO	f = 56
	Initiate Control Memory	f = 56
	CLR ZO	f = 56
	Set INCREMENT P flip-flop	f = 56
T3.2	Enable COMPARE, GREATER, and EQUAL flip-flops	
	CLR INCREMENT P flip-flop	f = 56, X ≠ D[1]
	Set OVERFLOW flip-flop	f = 26, 27·Adder ⟶ AU
	CLR B	
T3.3	CLR X, D, W	f = 56, INCR P flip-flop set
	Control Memory ⟶ ZO	f = 56
T3.4	ZO ⟶ B	
	AU ⟶ Arithmetic Selector	f = 04, 05
	Arithmetic Selector ⟶ X	f = 04, 05
	P ⟶ D	f = 56, INCR P flip-flop set
	Set Inhibit EAB	f = 56, INCR P flip-flop set
T4.1	CLR AL	f = 04, 05, 12-17, 20-23, 52, 53
	CLR AU	f = 10, 11
	CLR P	f = 54, 55, or 56 and INCR P flip-flop set
	CLR Borrow Test (flip-flop)	f = 20-23
T4.2	Adder ⟶ AL	f = 04, 05, 12-17, 20-23, 51-53
	Adder ⟶ AU	f = 10, 11
	Adder ⟶ P	f = 54, 55, or 56 and INCR P flip-flop set
	Set Borrow Test (flip-flop)	if EAB and f = 20-23
T4.3	CLR Z1	f = 32, 33
T4.4	Adder ⟶ Z1	f = 32, 33

TABLE 4-14. R1R2 SEQUENCE

(Identical to R1 Sequence for f = 20-27 except as follows)

TIME	COMMAND	CONDITION
T4.4	Inhibit CLR S1	
T1.1	Set S1 bit 0	
T1.2		
T1.3		
T1.4	AU ⟶ Arithmetic Selector	f = 20-23
T2.1		
T2.2		
T2.3		
T2.4	Set Insert EAB	If Borrow Test FF Set·f = 20-23
T3.1		
T3.2		
T3.3		
T3.4		
T4.1	CLR AU CLR Borrow Test flip-flop	f = 20-23 f = 20-23
T4.2	Adder ⟶ AU Set Borrow Test flip-flop	f = 20-23 If EAB·f = 20-23
T4.3		

TABLE 4-15. W SEQUENCE

TIME	COMMAND	CONDITION
T4.3	Set Spec Int Xlator = 17	f = 50:44
T4.4	CLR S1 Set Insert EAB	f ≠ 57 f = 57 and Y ≠ 0 (X ≠ D^1)
T1.1	Adder ⟶ S1 SPECIAL INT. XLATOR ⟶ S1 ICR ⟶ S0 CLR Z0 Initiate Control Memory	f = 57 f = 50:44 f = 42, 43 f = 42, 43

TABLE 4-15. W SEQUENCE (CONT.)

TIME	COMMAND	CONDITION
T1.2	Z1 → Z0	f = 57
T1.3	CLR Z1	f ≠ 30, 31, 72, 75
	CLR X, W	f ≠ 57
T1.4	P → Arithmetic Selector	f = 30, 31, 76
	0's → Arithmetic Selector	f = 40, 41
	Z → Arithmetic Selector	f = 42, 43
	AU → Arithmetic Selector	f = 46, 47
	AL → Arithmetic Selector	f = 44, 45
	ICR → Arithmetic Selector	f = 72
	SR → Arithmetic Selector	f = 75
	K0 → Arithmetic Selector	f = 50:44
	Arithmetic Selector → X	f ≠ 24-27
	Store Selector → Z1	f ≠ 57
	Adder → Z1	f = 57
	0's → Arithmetic Selector Bits 12-17	f = 74
T2.1	CLR → P	f = 30, 31, 76
	S1 → S0 CLR Z0	S1 = Control or Bootstrap Mem Address
	Initiate Control Memory	S1 = Control or Bootstrap Mem Address
T2.2	S1 → P	f = 30, 31, 76
	Z1 → Z0	f = 30, 31, 40-47, 57, 76
	Inhibit Strobe, Main and Control Memory	f ≠ 30, 31, 40-47, 57, 76
	Inhibit Strobe lower 6 bits Z0·Z1	f = 72, 74, 75, 76
	Inhibit Strobe lower 12 bits Z0·Z1	f = 74
T2.3	CLR Insert EAB	f = 57
	CLR SR	f = 75
T2.4		
T3.1	Set INCREMENT P flip-flop	f = 30, 31, 76, 57·$\overline{\text{SKIP}}$
T3.2		
T3.3	CLR X, W	f = 30, 31, 76, 57·$\overline{\text{SKIP}}$
	CLR D	f = 30, 31, 76, 57·$\overline{\text{SKIP}}$
T3.4	P → D	f = 30, 31, 76, 57·$\overline{\text{SKIP}}$
	Set Inhibit EAB flip-flop	f = 30, 31, 76, 57·$\overline{\text{SKIP}}$
T4.1	CLR P	f = 30, 31, 76, 57·$\overline{\text{SKIP}}$
T4.2	Adder → P	f = 30, 31, 76, 57·$\overline{\text{SKIP}}$

TABLE 4-16. IB1 SEQUENCE

TIME	COMMAND
T4.4	CLR S1
T1.1	P ⟶ S1 Enable Main Memory Set INCREMENT P flip-flop CLR Z0
T1.2	
T1.3	Inhibit CLR F CLR D, X, W, Z1
T1.4	Set INHIBIT EAB flip-flop PL ⟶ DL PU ⟶ DU Inhibit Clear K0
T2.1	CLR Sequence Designator, lower rank CLR P CLR Z0
T2.2	Sequence Designator, Upper Rank ⟶ Lower Rank (Set I and B1 flip-flops) Memory ⟶ Z1 Adder ⟶ P
T2.3	CLR EAB flip-flops Z1 ⟶ Z Select Z Select ⟶ Arithmetic Selector CLR D, X, W
T2.4	Arithmetic Selector ⟶ D Arithmetic Selector ⟶ X, Arithmetic Selector ⟶ X Arithmetic Selector ⟶ W Inhibit Z select Bits 00-05 ⟶ K0 Inhibit Z select ⟶ F CLR Main Memory Enable flip-flop Inhibit 0's ⟶ Arithmetic Selector Bits 12-17
T3.1	ICR ⟶ S0 Initiate Control Memory Clear I/O Translators (Xlator 1, Chan and Funct and Special Int Xlator) CLR Z0
T3.2	F and K ⟶ I/O Translator
T3.3	
T3.4	

TABLE 4-16. IB1 SEQUENCE (CONT.)

TIME	COMMAND
T4.1	Inhibit Clear Run 1 flip-flop CLR Z0 CLR Sequence Designator, Upper Rank CLR B±1 flip-flop
T4.2	Sequence Designator, Lower Rank ⟶ Upper Rank (Set I and B2 flip-flops)
T4.3	CLR Z1

TABLE 17. IB2 SEQUENCE

TIME	COMMAND
T4.4	Adder ⟶ Z1 CLR S1
T1.1	P ⟶ S1 I/O Translator ⟶ S0 Enable Main Memory Initiate Control Memory Set INCREMENT P flip-flop CLR Z0
T1.2	Z1 ⟶ Z0
T1.3	Inhibit CLR F CLR D, X, W, Z1 Inhibit Control Memory ⟶ Z0
T1.4	Set INHIBIT EAB flip-flop PL ⟶ DL PU ⟶ DU Inhibit Clear K0
T2.1	CLR Sequence Designator, Lower Rank CLR P CLR Z0
T2.2	Sequence Designator, Upper Rank ⟶ Lower Rank (Set I flip-flop) Memory ⟶ Z1 Adder ⟶ P
T2.3	CLR EAB flip-flops Z1 ⟶ Z Select Z Select ⟶ Arithmetic Selector CLR D, X, W

TABLE 4-17. IB2 SEQUENCE (CONT.)

TIME	COMMAND
T2.4	Arithmetic Selector ⟶ D Arithmetic Selector ⟶ X, $\overline{\text{Arithmetic Selector}}$ ⟶ X Arithmetic Selector ⟶ W Inhibit Z select Bits 00-05 ⟶ K0 Inhibit Z select ⟶ F CLR Main Memory Enable flip-flop Inhibit 0's ⟶ Arithmetic Selector Bits 12-17
T3.1	ICR ⟶ S0 Initiate Control Memory Clear I/O Translators (Xlator 1, Chan and Funct and Special Int Xlator) CLR Z0
T3.2	F and K ⟶ I/O Translator
T3.3	
T3.4	
T4.1	Inhibit Clear Run 1 flip-flop CLR Z0 CLR Sequence Designator, Upper Rank CLR B±1 flip-flop
T4.2	Sequence Designator, Lower Rank ⟶ Upper Rank (Set I and B2 flip-flops)
T4.3	CLR Z1 Set Active FF (as designated by F and K)
T4.4	Adder ⟶ Z1 At this point, computer enters I Sequence of next instruction.
T1.1	P ⟶ S1 I/O Translator ⟶ S0 Set S0 20 Enable Main Memory Initiate Control Memory Set INCREMENT P flip-flop CLR P
T1.2	Z1 ⟶ Z0
T1.3	CLR F, D, W, Z1 Inhibit Control Memory ⟶ Z0

FORMAT I INSTRUCTIONS

00	ILLEGAL CODE I	Execution time: 2 usec
01	ILLEGAL CODE I	Execution time: 2 usec
02	COMPARE (AL) WITH (Y) I R1	Execution time: 4 usec
03	COMPARE (AL) WITH (Y) I (B modified)	Execution time: 4 usec
04	SELECTIVE SUBSTITUTE I R1	Execution time: 4 usec
05	SELECTIVE SUBSTITUTE I (B modified) R1	Execution time: 4 usec
06	COMPARE WITH MASK I R1	Execution time: 4 usec
07	COMPARE WITH MASK I (B modified) R1	Execution time: 4 usec
10	ENTER AU I R1	Execution time: 4 usec
11	ENTER AU I (B modified) R1	Execution time: 4 usec
12	ENTER AL I R1	Execution time: 4 usec
13	ENTER AL I (B modified) R1	Execution time: 4 usec
14	ADD AL I R1	Execution time: 4 usec
15	ADD AL I (B modified) R1	Execution time: 4 usec

16 SUBTRACT AL Execution time: 4 usec
I
R1

17 SUBTRACT AL Execution time: 4 usec
I (B modified)
R1

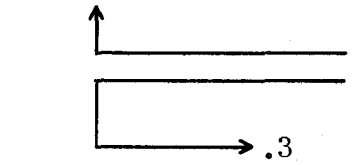
20 ADD A Execution time: 6 usec
I
R1
R1R2

21 ADD A Execution time: 6 usec
I (B modified)
R1
R1R2

22 SUBTRACT A Exeuction time: 6 usec
I
R1
R1R2

23 SUBTRACT A Execution time: 6 usec
I
R1
R1R2

24 MULTIPLY AL Execution time: 14 usec
I
R1T1.3 Set A NEG FF if AL neg, CLR D, X, W Reg.
.4 AL ⟶ Selector, $\overline{\text{Selector}}$ ⟶ D
R1T2.1 Set MULT/DIV SEQ (OXL01), Set KO=19_{10}, CLR AL if AL=neg
.2 CLR K1, Adder ⟶ AL if AL = neg
.3 CLR X, CLR W, CLR D (Pass 1 only)
⟶ KO-1 ⟶ K1
CLR MULT. STORE FF
Set OXL00 (First pass and KO ≠ 0)
Set Hold II FF (HOLD I FF set and first pass only)
.4 CLR KO, Selector ⟶ D (Y pos) Selector ⟶ D (Y neg)
(Pass 1 only)
Set MULT. STORE FF (AL Bit 0 = 1)
AUR1 ⟶ X, ALR1 ⟶ W
Set Y NEG FF if X = neg (Pass 1 only)
.1 K1 ⟶ KO
CLR AL
CLR AU



```
                .2    CLR    K1
                      SET HOLD 1 FF          (First pass only)
                      W ⟶ AL
(R1T2.3)              X ⟶ AU                 (AL Bit 0 = 0)
                      Adder ⟶ AU             (AL Bit 0 = 1)
                      KO ≠ 0
                      KO = 0

                .3    CLR  OXL00
                      Set  OXL02
                      KO-1 ⟶ K1
                      CLR  MULT. STORE FF
                      CLR X, CLR W

                .4    AUR1 ⟶ X, ALR1 ⟶ W

                .1    Set CLEAR HOLD FF
                      Set OXL03
                      CLR OXL01

                .3    CLR X, W, D
                      Set OXL04
                      CLR OXL02

                .4    AU ⟶ Arithmetic Selector
                      Arithmetic Selector ⟶ X      (AU  or AL ≠ 0)
                      Arithmetic Selector ⟶ X      (AU  or AL ≠ 0)
                      Arithmetic Selector ⟶ D

                .1    CLR  AU                      (Comp AU)
                      Set OXL05                    (Signs Unlike)
                      CLR OXL03

              R1T1.2  Resume R1 Sequence here
                      Adder ⟶ AU                   (Comp AU, Signs Unlike)
                      CLR HOLD I FF

                .3    CLR    D                     (Signs Unlike)
                      Set OXL06                    (Signs Unlike)
                      CLR OXL04

                .4    AL ⟶ Arithmetic Selector     (Signs Unlike)
                      Arithmetic Selector ⟶ D      (Signs Unlike)
```

NOTE

At this point, this instruction enters I sequence of the next instruction to complete its operation.

```
I    .1    CLR  AL                          (Signs Unlike)
           CLR  OXL05
      .2    Adder ⟶ AL
      .3    CLR  HOLD II FF                  (Signs Unlike)

25    MULTIPLY  AL                           Execution time:  14 usec
      I  (B modified)
      R1T2.1     Set MULT/DIV SEQ
                 (Same as instruction 24)
        T4.2     Resume R1 SEQ
                 (Same as instruction 24)
      I          (Same as instruction 24)

26    DIVIDE A                               Execution time:  14 usec
      I
      R1T1.3     Set A NEG FF if AU negative, CLR D, X, W
          .4     AU ⟶ Arithmetic Selector, (Arithmetic Selector) ⟶ D
      R1T2.1     Set MULT/DIV SEQ    (OXL01), Set KO = 18(10), CLR AU if AU neg
          .2     CLR K1, Adder ⟶ AU if AU neg
      ⟶   .3     CLR X, CLR W, CLR D (first pass only)
                 KO-1 ⟶ K1
                 Set OXL00                          (First pass and KO ≠ 0)
                 Set Hold II FF                     (HOLD I FF set and first
                                                    pass only)
          .4     CLR KO, (Arithmetic Selector) ⟶ D if Y pos (Pass 1 only)
                 AUL1 ⟶ X, ALL1 ⟶ W, Set Y NEG FF if X neg (Pass 1 only)
                 Arithmetic Selector ⟶ D if Y neg (First pass only)
          .1     K1 ⟶ KO
                 CLR  AL
                 CLR  AU
          .2     CLR  K1
                 SET HOLD 1 FF                      (First pass only)
                 W ⟶ AL
                 X ⟶ AU                             (EAB)
                 Adder ⟶ AU                         (No EAB)
                 If Adder ⟶ AU, set OVERFLOW FF (Pass 1 only)
      ⟵          KO ≠ 0
      ⟵          KO = 0
      ⟶   .3     CLR OXL00
                 Set OXL02
                 KO-1 ⟶ K1
                 CLR X, CLR W
          .4     AUL1 ⟶ X, ALL1 ⟶ W
          .1     Set CLEAR HOLD FF
                 Set OXL03
                 CLR OXL01
          .2
```

	.3	CLR X, W, D Set OXL04 CLR OXL02	
	.4	AU ⟶ Arithmetic Selector Arithmetic Selector ⟶ D	
	.1	CLR AU Set OXL05 CLR OXL03	(Comp AU) (Comp AU) (Signs Unlike)
R1T4.2		Resume R1 Sequence here Adder ⟶ AU CLR HOLD I FF	Comp AU
	.3	CLR D Set OXL06 CLR OXL04	(Signs Unlike) (Signs Unlike)
	.4	AL ⟶ Arithmetic Selector Arithmetic Selector ⟶ D	(Signs Unlike) (Signs Unlike)

NOTE

At this point, this instruction enters I sequence of the next instruction to complete its operation.

I	.1	CLR AL CLR OXL05	(Signs Unlike)
	.2	Adder ⟶ AL	(Signs Unlike)
	.3	CLR HOLD II FF	

27 DIVIDE A — Execution time: 14 usec

I (B modified)		
R1T2.1	Set MULT/DIV SEQ (Same as instruction 26)	
T4.2	Resume R1 SEQ (Same as instruction 26)	
I	(Same as instruction 26)	

30 INDIRECT RETURN JUMP — Execution time: 6 usec

I
R1
W

31 INDIRECT RETURN JUMP — Execution time: 16 usec

I (B modified)
R1
W

32 ENTER B — Execution time: 4 usec

I
R1

NOTE

At this point, this instruction enters I sequence of the next instruction to complete its operation.

I 1.1 ICR ⟶ SO
Initiate Control Memory

1.2 Z1 ⟶ Z0

1.3 Inhibit Control Memory ⟶ Z0

33 ENTER B — Execution time: 4 usec
I (B modified)
R1
I (Same as 32)

34 DIRECT JUMP — Execution time: 2 usec
I

35 DIRECT JUMP — Execution time: 2 usec
I (B modified)

36 ENTER B WITH CONSTANT — Execution time: 2 usec
I

NOTE

At this point, this instruction enters I sequence of the next instruction to complete its operation.

I 1.1 ICR ⟶ SO
Initiate Control Memory

1.2 Z1 ⟶ Z0

1.3 Inhibit Control Memory ⟶ Z0

37 MODIFY B WITH CONSTANT — Execution time: 2 usec
I (B modified)
I (Same as 36)

40 CLEAR Y — Execution time: 4 usec
I
W

41 CLEAR Y — Execution time: 4 usec
I (B modified)
W

42 STORE (B) — Execution time: 4 usec
I
W

43 STORE (B) Execution time: 4 usec
I (B modified)
W

44 STORE AL Execution time: 4 usec
I
W

45 STORE AL Execution time: 4 usec
I (B modified)
W

46 STORE AU Execution time: 4 usec
I
W

47 STORE AU Execution time: 4 usec
I (B modified)
W

50 See Format II instructions following instruction 77.

51 SELECTIVE SET Execution time: 4 usec
I
R1

52 SELECTIVE CLEAR Execution time: 4 usec
I
R1

53 SELECTIVE COMPLEMENT Execution time: 4 usec
I
R1

54 INDIRECT JUMP AND ENABLE INTERRUPTS Execution time: 4 usec
I
R1

55 INDIRECT JUMP Execution time: 4 usec
I
R1

56 B SKIP Execution time: 4 usec
I
R1

NOTE

At this point, this instruction enters I sequence of the next instruction to complete its operation.

I 1.1 ICR → SO if B ≠ (Y)
Initiate Control Memory

1.2 B+1 → ZØ

1.3 Inhibit Control Memory → ZO

57 INDEX SKIP Execution time: 6 usec
I
R1
W

60 JUMP AU ZERO Execution time: 2 usec
I

61 JUMP AL ZERO Execution time: 2 usec
I

62 JUMP AU NOT ZERO Execution time: 2 usec
I

63 JUMP AL NOT ZERO Execution time: 2 usec
I

64 JUMP AU POSITIVE Execution time: 2 usec
I

65 JUMP AL POSITIVE Execution time: 2 usec
I

66 JUMP AU NEGATIVE Execution time: 2 usec
I

67 JUMP AL NEGATIVE Execution time: 2 usec
I

70 ENTER AL WITH CONSTANT Execution time: 2 usec
I

71 ADD CONSTANT TO (AL) Execution time: 2 usec
I

72 STORE INDEX CONTROL REGISTER Execution time: 4 usec
I
W

73 B JUMP Execution time: 2 usec
I

NOTE

At this point, this instruction enters I sequence of the next instruction to complete its operation.

I 1.1 ICR ⟶ S0 if B ≠ 0
Initiate Control Memory

1.2 B-1 ⟶ Z0

1.3 Inhibit Control Memory ⟶ Z0

74 STORE ADDRESS Execution time: 4 usec
I
W

75 STORE SPECIAL REGISTER Execution time: 4 usec
I
W

76 DIRECT RETURN JUMP Execution time: 4 usec
I
W

77 ILLEGAL CODE Execution time: 2 usec
I

FORMAT II INSTRUCTIONS

50:00 Not Used

50:01 SET INPUT ACTIVE Execution time: 2 usec
I

50:02 SET OUTPUT ACTIVE Execution time: 2 usec
I

50:03 SET EXTERNAL FUNCTION ACTIVE Execution time: 2 usec
I

50:04 Not Used

50:05 Not Used

50:06 Not Used

50:07 Not Used

50:10 Not Used

50:11 INPUT TRANSFER Execution time: 6 usec
I
IB1
IB2

NOTE

At this point, this instruction enters I sequence of the next instruction to complete its operation.

I 1.1
1.2
1.3

50:12 OUTPUT TRANSFER Execution time: 6 usec
I
IB1
IB2

NOTE

At this point, this instruction enters I sequence of the next instruction to complete its operation.

50:13 EXTERNAL FUNCTION Execution time: 6 usec
I
IB1
IB2

NOTE

At this point, this instruction enters I sequence of the next instruction to complete its operation.

I

50:14 ENABLE REAL-TIME CLOCK MONITOR Execution time: 2 usec

50:15 TERMINATE INPUT Execution time: 2 usec
I

50:16 TERMINATE OUTPUT Execution time: 2 usec
I

50:17 TERMINATE EXTERNAL FUNCTION Execution time: 2 usec
I

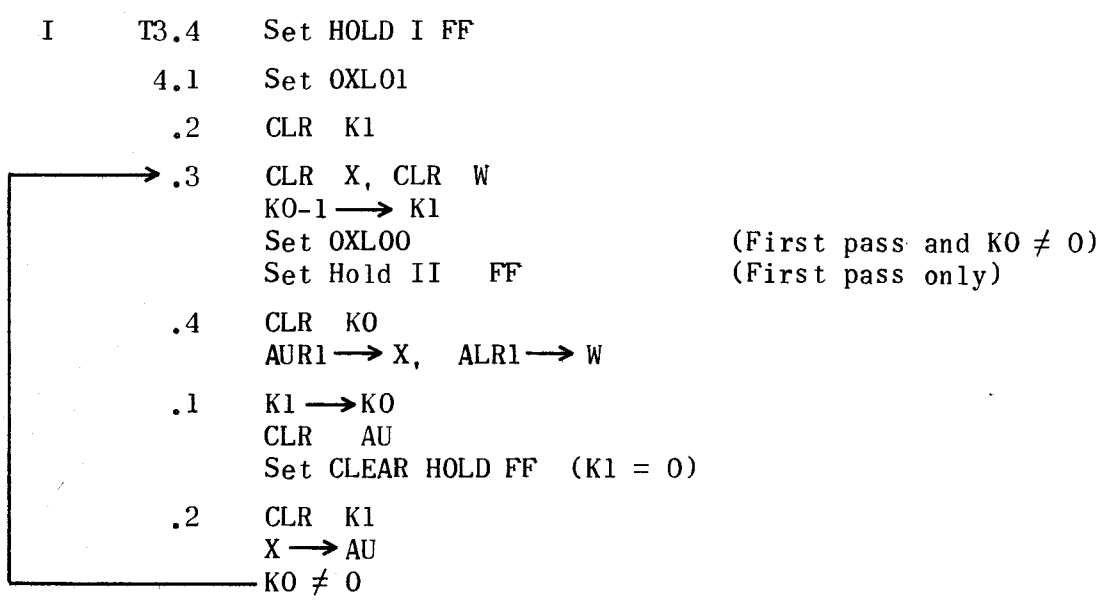
50:20 SET RESUME Execution time: 2 usec
I

50:21 SKIP ON INPUT CHANNEL INACTIVE Execution time: 2 usec
I

50:22 SKIP ON OUTPUT CHANNEL INACTIVE Execution time: 2 usec
I

50:23 SKIP ON FUNCTION MODE INACTIVE Execution time: 2 usec
I

50:24 and 50:25	WAIT FOR INTERRUPT I WAIT	Execution time: Indeterminate
50:26	OUTPUT OVERRIDE I	Execution time: 6 or 8 usec
50:27	EXTERNAL FUNCTION OVERRIDE I	Execution time: 6 or 8 usec
50:30 and 50:31	REMOVE INTERRUPT LOCKOUT I	Execution time: 2 usec
50:32 and 50:33	REMOVE EXTERNAL INTERRUPT I	Execution time: 2 usec
50:34 and 50:35	SET INTERRUPT LOCKOUT I	Execution time: 2 usec
50:36 and 50:37	SET EXTERNAL INTERRUPT LOCKOUT I	Execution time: 2 usec
50:40	Not Used	
50:41	RIGHT SHIFT AU	Execution time: 4 usec (KO = 0-4) 6 usec (KO = 5-8) 8 usec (KO = 9-12) 10 usec (KO = 13-16)



```
                    KO = 0
                .3  CLR  OXL00
                    Set  OXL02
                    KO-1 ──► K1
                    CLR  X, CLR  W
                .4  AUR1 ──► X, ALR1 ──► W
                .1  CLR  OXL01
                    Set CLEAR HOLD FF (Shift count = 0)
```

50:42 RIGHT SHIFT AL — Execution time: 4 usec (KO = 0-4); 6 usec (KO = 5-8); 8 usec (KO = 9-12); 10 usec (KO = 13-16)
I

```
            T3.4    Set HOLD I FF
             4.1    Set OXL01
              .2    CLR  K1
              .3    CLR  X, CLR  W
                    KO-1 ──► K1
                    Set OXL00              (First pass and KO ≠ 0)
                    Set Hold II FF         (First pass only)
              .4    CLR  KO
                    AUR1 ──► X, ALR1 ──► W
              .1    K1 ──► KO
                    CLR   AL
                    Set CLEAR HOLD FF (K1 = 0)
              .2    CLR  K1
                    W ──► AL
                    KO ≠ 0
                    KO = 0
                .3  CLR  OXL00
                    Set  OXL02
                    KO-1 ──► K1
                    CLR X,  CLR W
                .4  AUR1 ──► X, ALR1 ──► W
                .1  CLR  OXL01
                    Set CLEAR HOLD FF (Shift count ≠ 0)
```

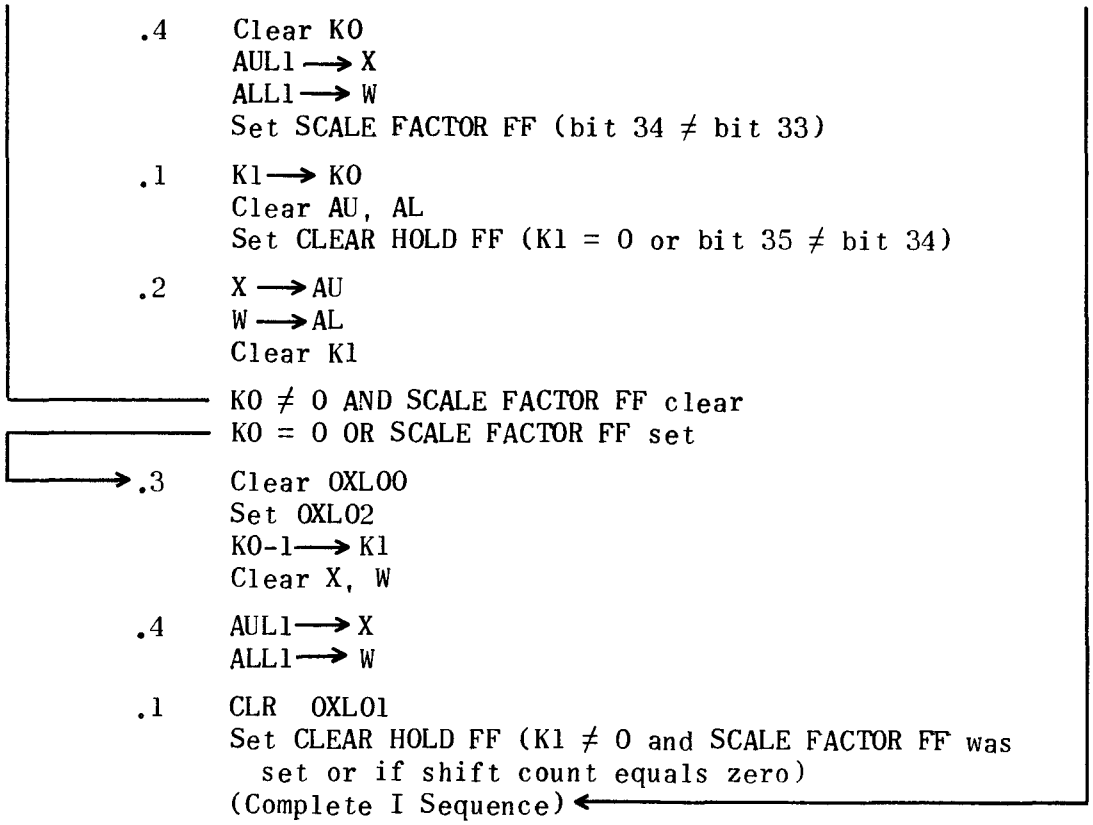
50:43 RIGHT SHIFT A — Execution time: 4 usec (K = 0-4); 6 usec (K = 5-8); 8 usec (K = 9-12); 10 usec (K = 13-16); 12 usec (K = 17-20); 14 usec (K = 21-24); 16 usec (K = 25-28); 18 usec (K = 29-32); 20 usec (K = 33-35)
I

```
        T3.4    Set HOLD I FF
         4.1    Set OXL01
          .2    CLR  K1
          .3    CLR X, CLR W
                KO-1 ⟶ K1
                Set OXL00                    (First pass and KO = 0)
                Set HOLD II FF               (First pass only)
          .4    CLR  KO
                AUR1 ⟶ X,  ALR1 ⟶ W
                LOWER BIT OF AU ⟶ UPPER BIT OF W
          .1    K1 ⟶ KO
                CLR  AL
                CLR  AU
                Set CLEAR HOLD FF (K1 = 0)
          .2    CLR  K1
                W ⟶ AL
                X ⟶ AU
                KO ≠ 0
                KO = 0
          .3    CLR  OXL00
                Set OXL02
                KO-1 ⟶ K1
                CLR X,  CLR W
          .4    AUR1 ⟶ X,  ALR1 ⟶ W
                LOWER BIT OF AU ⟶ UPPER BIT OF W
          .1    CLR  OXL01
                Set CLEAR HOLD FF (if shift count = 0)
```

50:44 SCALE FACTOR I

Execution time:
- 4 usec (K = 0-4)
- 6 usec (K = 5-8)
- 8 usec (K = 9-12)
- 10 usec (K = 13-16)
- 12 usec (K = 17-20)
- 14 usec (K = 21-24)
- 16 usec (K = 25-28)
- 18 usec (K = 29-32)
- 20 usec (K = 33-35)

```
        T3.1    Set CLEAR HOLD FF (bit 35 ≠ bit 34)
        T3.4    Set HOLD 1 FF
                Clear SCALE FACTOR FF
                Bit 35 ≠ bit 34
                Bit 35 = bit 34
         4.1    Set OXL01
          .2    Clear K1, clear HOLD I FF (bit 35 ≠ bit 34)
          .3    KO-1 ⟶ K1
                Clear X, W
                Set OXL00                    (First pass and KO ≠ 0)
                Set HOLD II FF (Pass 1 and HOLD I FF set)
```

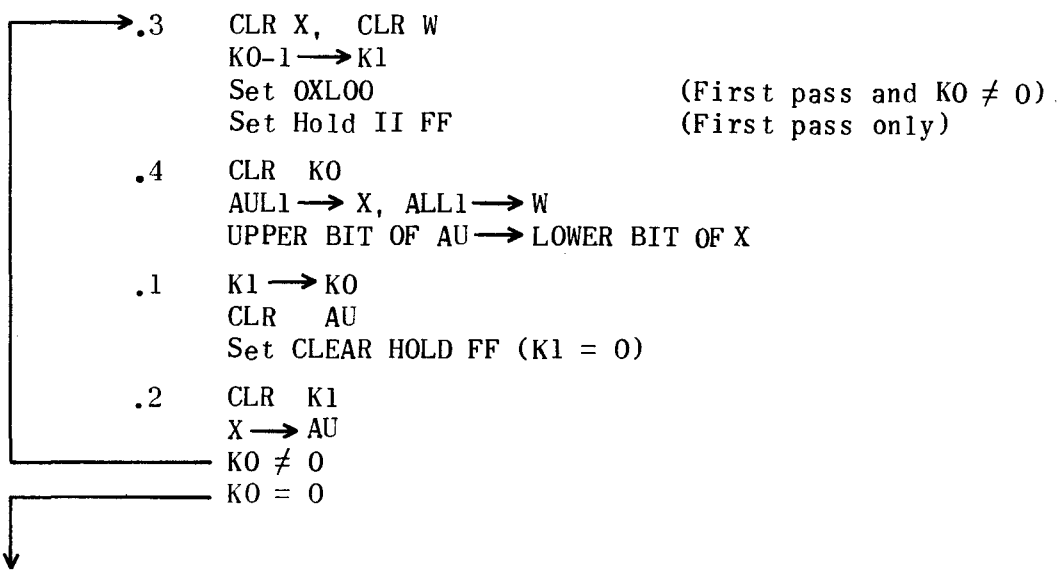


W

50:45 LEFT SHIFT AU

I

Execution time: 4 usec (KO = 0-4)
6 usec (KO = 5-8)
8 usec (KO = 9-12)
10 usec (KO = 13-16)



```
                .3   CLR  OXL00
                     Set  OXL02
                     K0-1 ──→ K1
                     CLR X, CLR W

                .4   AUL1 ──→ X, ALL1 ──→ W
                     UPPER BIT OF AU ──→  LOWER BIT OF X

                .1   CLR  OXL01
                     Set CLEAR HOLD FF (if shift count equals zero)
```

50:46 LEFT SHIFT AL I

Execution time: 4 usec (K0 = 0-4)
6 usec (K0 = 5-8)
8 usec (K0 = 9-12)
10 usec (K0 = 13-16)

```
          T3.4   Set HOLD I FF

           4.1   Set OXL01

            .2   CLR  K1

            .3   CLR  X, CLR W
                 K0-1 ──→ K1
                 Set OXL00                  (First pass and K0 ≠ 0)
                 Set Hold II FF             (First pass only)

            .4   CLR  K0
                 AUL1 ──→ X, ALL1 ──→ W
                 UPPER BIT OF AL ──→ LOWER BIT OF W

            .1   K1 ──→ K0
                 CLR   AL
                 Set CLEAR HOLD FF (K1 = 0)

            .2   CLR   K1
                 W ──→ AL
                 K0 ≠ 0
                 K0 = 0

            .3   CLR  OXL00
                 Set OXL02
                 K0-1 ──→ K1
                 CLR X, CLR W

            .4   AUL1 ──→ X, ALL1 ──→ W
                 UPPER BIT OF AL ──→ LOWER BIT OF X

            .1   CLR OXL01
                 Set CLEAR HOLD FF (if shift count equals zero).
```

50:47 RIGHT SHIFT A
I

Execution time:
4 usec (K = 0-4)
6 usec (K = 5-8)
8 usec (K = 9-12)
10 usec (K = 13-16)
12 usec (K = 17-20)
14 usec (K = 21-24)
16 usec (K = 25-28)
18 usec (K = 29-32)
20 usec (K = 33-35)

T3.4 Set HOLD I FF

4.1 Set OXL01

.2 CLR K1

.3 CLR X, CLR W
KO-1 → K1
Set OXL00 (First pass and KO ≠ 0)

.4 CLR KO
AUL1 → X, ALL1 → W
UPPER BIT OF AL → LOWER BIT OF X
UPPER BIT OF AU → LOWER BIT OF W

.1 K1 → KO
CLR AL
CLR AU
Set CLEAR HOLD FF (K1 = 0)

.2 CLR K1
W → AL
X → AU
KO ≠ 0
KO = 0

.3 CLR OXL00
Set OXL02
KO-1 → K1
CLR X, CLR W

.4 AUL1 → X, ALL1 → W
UPPER BIT OF AL → LOWER BIT OF X
UPPER BIT OF AU → LOWER BIT OF W

.1 CLR OXL01
Set CLEAR HOLD FF (if shift count equals zero)

50:50	SKIP OF KEY SETTING I	Execution time: 2 usec
50:51	SKIP ON NO BORROW I	Execution time: 2 usec
50:52	SKIP ON OVERFLOW I	Execution time: 2 usec
50:53	SKIP ON NO OVERFLOW I	Execution time: 2 usec
50:54	SKIP ON ODD PARITY I	Execution time: 2 usec
50:55	SKIP ON EVEN PARITY I	Execution time: 2 usec
50:56	STOP ON KEY SETTING I	Execution time: 2 usec
50:57	SKIP ON NO RESUME I	
50:60	ROUND AU I	Execution time: 2 usec
50:61	COMPLEMENT AL I	Execution time: 2 usec
50:62	COMPLEMENT AU I	Execution time: 2 usec
50:63	COMPLEMENT A I	Execution time: 2 usec
50:64	Not Used	
50:65	Not Used	
50:66	Not Used	
50:67	Not Used	
50:70	Not Used	
50:71	Not Used	
50:72	ENTER INDEX CONTROL REGISTER I	Execution time: 2 usec
50:73	ENTER SPECIAL REGISTER I	Execution time: 2 usec
50:74	Not Used	

50:75 Not Used

50:76 Not Used

50:77 Not Used

SECTION 5

TROUBLESHOOTING

5-1. GENERAL.

This section contains the recommended procedures to isolate and correct equipment malfunctions. Included are suggested schedules for performing maintenance programming, such as preventive maintenance routines, tests to be performed in conjunction with maintenance programming, and a logical explanation of the error conditions which may result during the performance of these tests.

Performance testing and functional checks are the two basic maintenance procedures for the computer. Performance tests involve the use of maintenance programs included in this section to indicate the performance level either prior to system operation or during maintenance procedures. The functional checks are included to assist in detecting the nature of a computer malfunction. The command-timing tables in section 4 list the sequence of events occurring during the execution of an instruction and may be used as a reference during the performance of the functional checks.

5-2. TEST EQUIPMENT AND SPECIAL TOOLS.

Table 6-1 lists the recommended test equipment and special tools to be used as aids in malfunction isolation and computer repair.

5-3. PRIMARY TROUBLESHOOTING.

Troubleshooting the computer is primarily a logical analysis of the symptoms peculiar to the malfunction. The printed-circuit module concept simplifies the task of troubleshooting because module replacement eliminates the need for component malfunction isolation. No circuit module repair procedures are included in this manual; defective modules are replaced.

a. INITIAL INSPECTION. - Following detection of a malfunction, visually inspect the panel indicators, switches, and fuses. If this inspection reveals a trouble area, a logical process of elimination will, in many instances, reveal the source of the trouble. Since this logical approach varies with the individual maintenance technician, no definite rules are included in this text. However, the step-by-step power check can be used to supplement the analysis. Use of the timing sequence charts in section 4 provides an advance indication of the events to be executed as the timing is manually advanced through the use of the phase-step sequence.

b. TEST POINT NOMENCLATURE. - The logic drawers each contain four test blocks; the memory drawer contains two test blocks.* Individual points within a test block are identified by the coordinate system; lettered from left to right and numbered from top to bottom. The first designator represents the particular test block on a given drawer; for example, TB2-B2 indicates test block 2, coordinates B and 2.

c. POWER CHECK. - The following procedure is used to check primary power and the dc voltages in the power logic, and memory drawers. The physical location of the drawers is shown in figure 8-5. The main power supply contains an interlock switch which must be secured in the cabinet during the voltage measurements. Fuse replacement is listed in table 1-18.

* Test blocks have been removed from memory drawer on serial numbers 49 and higher, and on serial numbers 14 - 48 if memory is larger than 32K. Memory test points for these machines are on circuit cards.

NOTE

The computer is sensitive to scope probes. Therefore, an unattenuated probe should be used only for sync input to the scope and for making power checks. All other checks should be made with an attenuated probe.

Ground connection for either oscilloscope or voltohmmeter connections is available at test point G33 on TB1 on logic chassis and at A32W2 on memory chassis or at any convenient ground inside the memory drawer. Using the cabinet as the ground connection for any measurement may result in an erroneous reading.

Use either an oscilloscope or voltohmmeter and measure the voltages by following the procedures of paragraph 2-6b.

Voltages which fail to meet the requirements listed in the table can then be traced to isolate the trouble to the power supply or the dc voltage bus network.

5-4. MEMORY TROUBLESHOOTING PROCEDURES.

Memory errors that occur in a logical pattern are generally caused by component failure, either in the memory proper or in the associated logic circuitry. The source of the error can be most easily isolated by use of the memory test program and by logical analysis. Random memory errors may indicate improperly adjusted memory-drive currents or read-strobe timing.

NOTE

Do not attempt to adjust memory regulated voltages, drive currents, or strobe timing until all other possible sources of malfunction have been investigated and corrected. See paragraph 6-4 for adjustment procedures.

5-5. MAINTENANCE PROGRAMS.

The maintenance programs consist of computer-controlled tests which may be performed to determine the functional capabilities of the system. These programs are included in PX 3520, 1219B Diagnostics.

5-6. PREVENTIVE MAINTENANCE SCHEDULES.

To maintain the computer in the best operating condition possible, perform the procedures listed in table 5-1.

TABLE 5-1. PREVENTIVE MAINTENANCE SCHEDULE

PROCEDURE	SCHEDULE	MANUAL REFERENCE
Indicator Inspection	Daily	None (for general information see section 3)
Vacuum Clean Filters	Weekly	Paragraph 5-6a(1)
Check System Ground	Weekly	Paragraphs 2-5, 5-6a(2)
Perform Confidence Check	Weekly	Paragraph 5-6a(3)
Clean Cabinet Interior	Monthly	Paragraph 5-6b(1)
Check Power	Monthly	Paragraph 5-6b(2)
Wash and Oil Filter	Semiannually	Paragraph 5-6c(1)
Test Memory Protect	Semiannually	Paragraph 5-6c(2)

Preventive maintenance (P.M.) is a term encompassing the procedures which the computer operator/maintenance personnel perform to keep the equipment in optimal operating condition, and prevent the decline of productive use. These P.M. procedures must be performed at regularly scheduled intervals. The period of time between P.M. checks will depend on the operating schedule necessary to meet productive requirements.

In a system where continuous operation is necessary, computer operation will have to be interrupted weekly for P.M. The time of this interruption is selected at the user's discretion. In a system of on-off (daily) operation, the computer confidence checks, paragraph 5-6a(4), should be performed before initiating a new productive period. In this on-off type of operation all other P.M. checks must be performed as scheduled.

A check off sheet (table 5-2) for the P.M. procedures is provided for use with table 5-1.

a. WEEKLY MAINTENANCE.

(1) VACUUM CLEAN AIR FILTER(S). - The air filter, located behind the grill on the power control panel (figure 6-9) must be vacuum-cleaned once each week. To remove the filter, perform the steps listed in paragraph 6-3j.

(2) CHECK SYSTEM GROUND. - Grounding the computer is important for two reasons; to ensure the safety of operating and maintenance personnel, and to maintain the dc level system used for I/O communications.

The computer is grounded in two places; at pin D (A14E1) of the power entry jack, and at ground lug E1 located at the rear of the cabinet. The ac neutral wire connects to A1E1; the system ground cables connect to ground lug A12E1 on the rear of the computer.

Use a separate cable for grounding each peripheral device to the computer. These cables should not be junctioned at any point other than at the ground lug A12E1 on the rear of the computer.

Ensure that ground is properly fastened to the computer.

(3) PERFORM CONFIDENCE CHECK. - The confidence programs consist of computer-controlled tests which may be performed to determine the functional capabilities of the computer. Either Maintenance routines or the Diagnostic routines may be used as confidence checks. The Maintenance routines are included in DS 4790. The Diagnostic routines are included in PX 3520.

b. MONTHLY MAINTENANCE.

(1) CLEAN CABINET INTERIOR. - Clean cabinet interior according to the following steps:

STEP 1. Extend and vacuum clean the exterior of all chassis. Remove as much dust as possible. There should be very little dust in the cabinet; if an excessive amount is present, the air filters or chassis are not seated properly or are not being cleaned thoroughly.

TABLE 5-2. PREVENTIVE MAINTENANCE CHECK-OFF SHEET

SCHEDULE	PROCEDURES	DATE	extra weeks 1	extra weeks 2
Weekly	Clean Air Filters			
	Check System Ground			
	Confidence Check			
Monthly	Power Check			
	Clean Cabinet Interior			
Semiannually	Wash and Oil Air Filters			
	Check Memory Protect			
	Record date and check-off P.M. procedures as you perform them. Take corrective action on abnormalities immediately.			

STEP 2. As each chassis is extended for cleaning, ensure that each card is seated properly. Loose or improperly seated cards cause intermittent failures. If there is excessive vibration, perform this maintenance procedure more frequently.

(2) CHECK POWER. - Check computer power by performing steps 1 through 9 of paragraph 2-6b.

c. SEMIANNUAL MAINTENANCE.

(1) WASH AND OIL FILTER. - Wash and oil the air filters semiannually. After removing the air filter (paragraph 6-3j), perform the following steps:

STEP 1. Vacuum filter.

STEP 2. Clean filter thoroughly in hot soapy water and dry with forced air.

STEP 3. Apply a thin coat of SAE #5 oil. Wipe off excess oil with a clean cloth.

(2) TEST MEMORY PROTECTION CIRCUITS. - Test the memory protection circuits semiannually by performing the following steps:

STEP 1. Load a program into the computer. A maintenance routine that can be cycled is ideal.

STEP 2. With the program cycling, drop computer power by pressing the computer ON/OFF switch to OFF.

STEP 3. Turn on computer power and restart program. If program does not operate properly, check the memory protect circuits. Repeat steps 2 and 3.

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SECTION 6

SERVICE AND REPAIR

6-1. SECTION CONTENT.

This section provides information required to correct isolated malfunctions, including parts replacement, adjustments, and overall troubleshooting instructions. Also included are memory troubleshooting procedures and waveforms to assist in the detection of errors due to memory component failure and the procedures for adjusting the clock cycle-time of the master timing circuits.

6-2. GENERAL.

Performance testing and functional checks are the two basic maintenance procedures for the computer. Performance tests involve the use of diagnostic programs (see paragraph 5-5) to indicate the performance level either prior to system operation or during maintenance procedures. Functional checks are included to assist in detecting the nature of a computer malfunction. The command-timing tables in section 4 list the sequence of events occurring during the execution of an instruction, and may be used as a reference during the performance of the functional checks.

a. SPECIAL TOOLS. - Table 6-1 lists the recommended special tools to be used as aids during computer maintenance and repair. These tools are not supplied with the computer at delivery.

The combination tool (figure 6-1) is supplied with the computer and is used during maintenance, service, and repair procedures.

A module extender (figure 6-2) can be fabricated by connecting a 15-pin male module connector to a female connector with 36-inch lengths of wire.

b. GENERAL PROCEDURES. - General procedures for wire-wrap or solder connections are contained in the following paragraphs.

(1) WIRE WRAP. - Most of the electrical connections in the computer are mechanical, solderless connections formed by wrapping a solid wire around a pin (figure 6-3). Each pin has a square cornered cross section. The wrapped connection forms a helical coil around the pin with points of contact at each of the four pin corners. Four points of contact are made for each turn of the connecting wire that encircles the pin.

Wire wrap connections are formed with a wire wrap gun (figure 6-4). This tool has a bit which rotates inside a stationary sleeve. The stationary sleeve holds the bit in place and has a slotted end that prevents the wire outside of the bit from rotating during the wrapping operation. The sleeve is held in the wire wrap gun by a chuck. The bit has a longitudinal groove that accommodates the end of the wire to be wrapped. A hole in the end of the bit (in the center) allows the bit to be slipped over the pin on which the wire wrap connection is to be made. The bit and sleeve used will depend on the gauge of the wire and size of the pin being wrapped.

All bits used in the field are of the modified type; that is, the bits are such that a portion of the insulation on the wire is also wrapped.

TABLE 6-1. TEST EQUIPMENT AND SPECIAL TOOLS

ITEM	NAME	VENDOR AND PART NUMBER	UNIVAC EQUIVALENT	FUNCTION
1	Oscilloscope	Tektronix 453	-	View waveforms
2	AC Current Probe	Tektronix 015-0140-02	-	View memory waveforms
3	Voltohmmeter	Triplett 630A	-	Measure AC/DC voltages, currents, and resistance
4	Crimping Tool, Single 24-26 gauge	Berg HT-14	8839-160	Crimp single taper pins to 24 gauge wire
5	Crimping Tool, Single 22 gauge, double 24 gauge	Berg HT-17	8839-161	Crimp double taper pins to 24 gauge wire
6	Insertion Tool	Amp No. 380306-2	8839-213	Insert taper pins in connectors
7	Insertion Tool	Amp No. 380310-3	8839-212	Insert taper pins in connectors
8	Insertion Tip	Amp No. 395042	8839-221	Insert double 24 gauge wire taper pins
9	Insertion Tip	Amp No. 395005	8839-227	Insert single 24 gauge wire taper pins
10	Wire Wrap Gun	Gardner-Denver No. 14R2	8130-132	Fasten wires to wire wrap pins
	The following bits and sleeves are used with item 10	Gardner-Denver		
	One 30 ga bit (*) One sleeve	501381 17611-2	8130-143 8130-129	
	One 30 ga bit One sleeve	504221 500350	8130-141 8130-142	
	One 28 ga bit (*) One sleeve	501389 502129	8130-155 8130-156	
	One 28 ga bit One sleeve	507387 502129	8130-154 8130-156	

(*) Indicates modified to wrap 1 1/4 more times than standard.

TABLE 6-1. TEST EQUIPMENT AND SPECIAL TOOLS (CONT)

ITEM	NAME	VENDOR AND PART NUMBER	UNIVAC EQUIVALENT	FUNCTION
		Gardner-Denver		
	One 24 ga bit	A17612-2	8130-123	
	One sleeve	17611-2	8130-129	
	One 24 ga bit (*)	26263	8130-121	
	One sleeve	18840	8130-128	
	One 24 ga bit	26589	8130-120	
	One 24/30 ga sleeve	17611-2	8130-129	
11	Unwrap Tool, 30 ga	Gardner-Denver No. 505244	8130-137	Unwraps wire wrap connections
12	Unwrap Tool 20 ga - 26 ga (inclusive)	Gardner-Denver No. 500130	8130-138	Unwraps wire wrap connections
13	Module Extender		7009452-00	Extend PC Module for test

(*) Indicates modified to wrap 1 1/4 more times than standard.

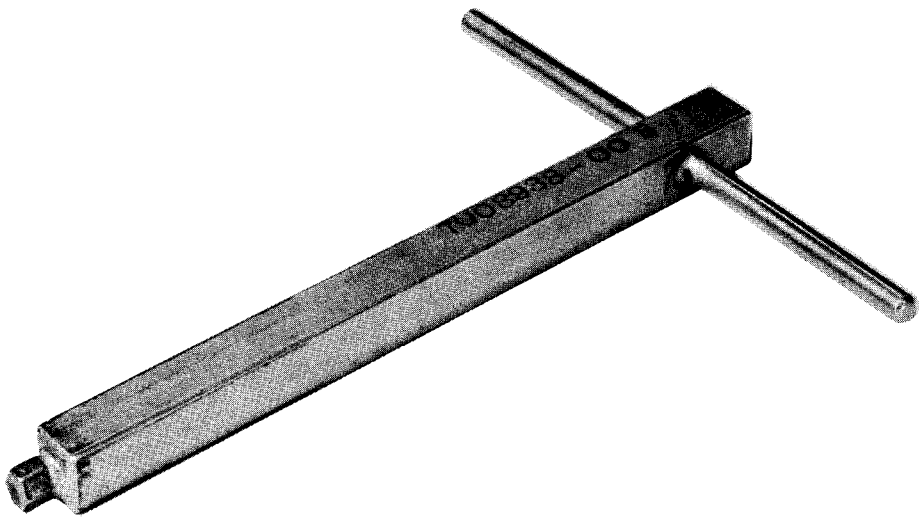


Figure 6-1. Combination Tool

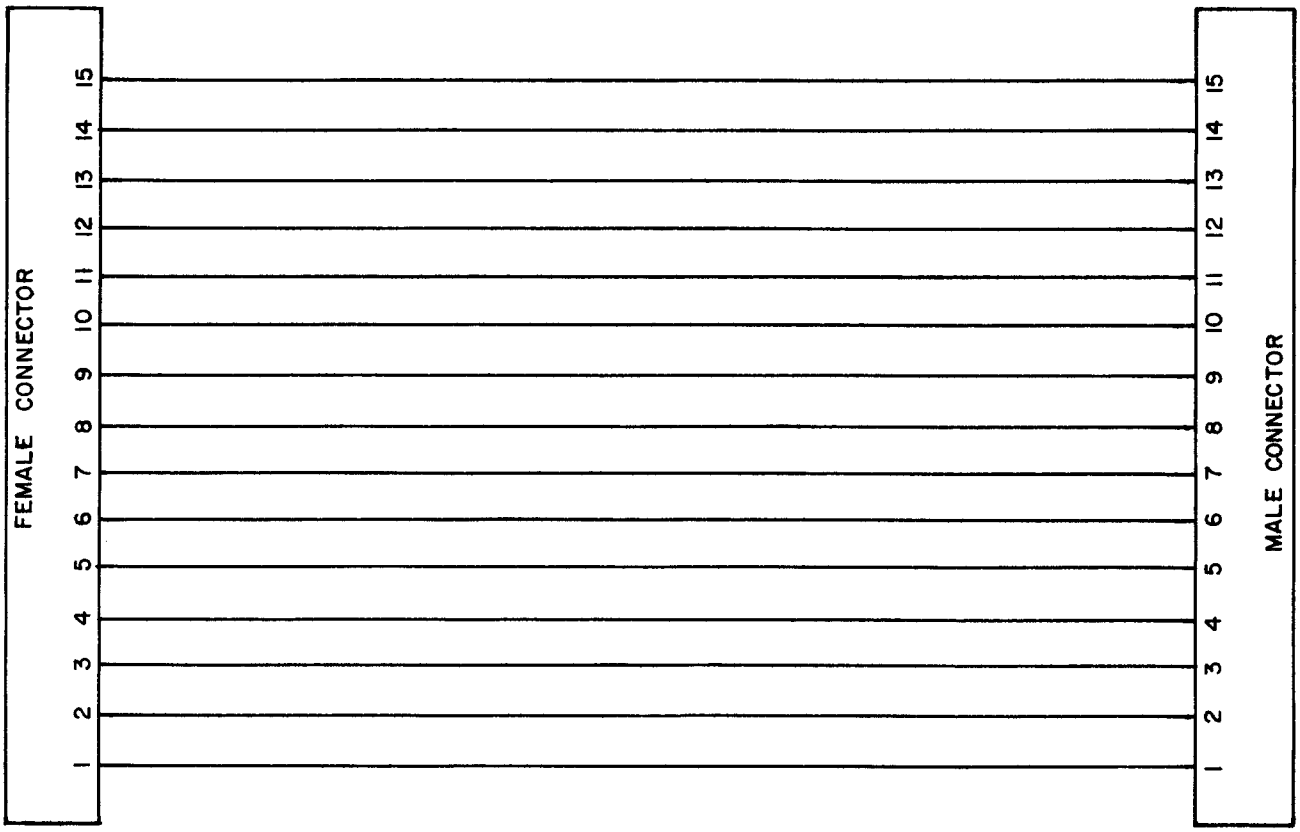


Figure 6-2. Module Extender Schematic

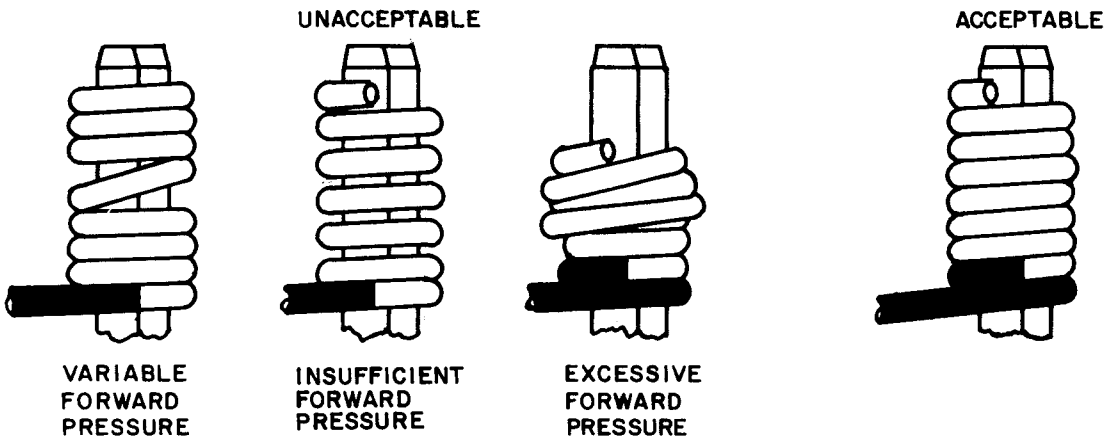
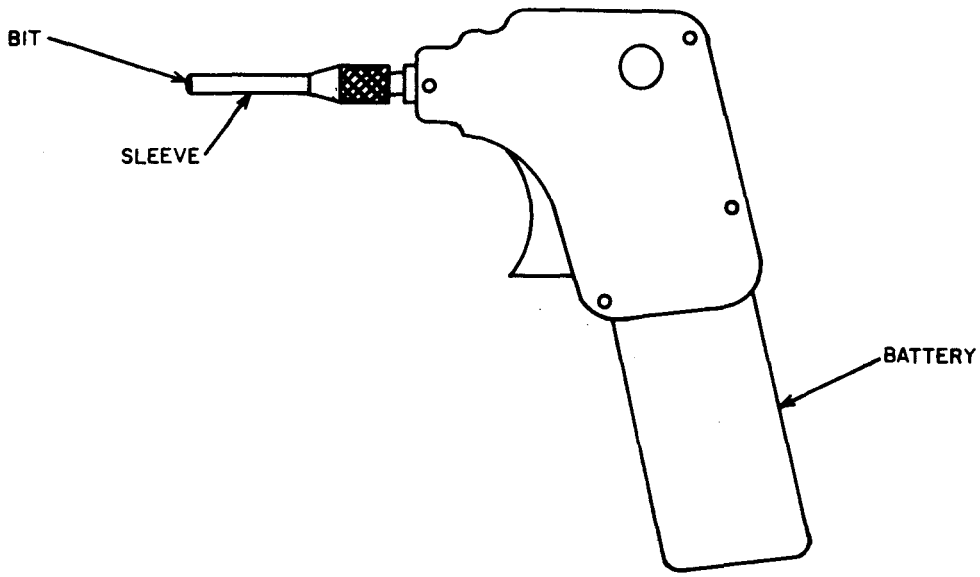
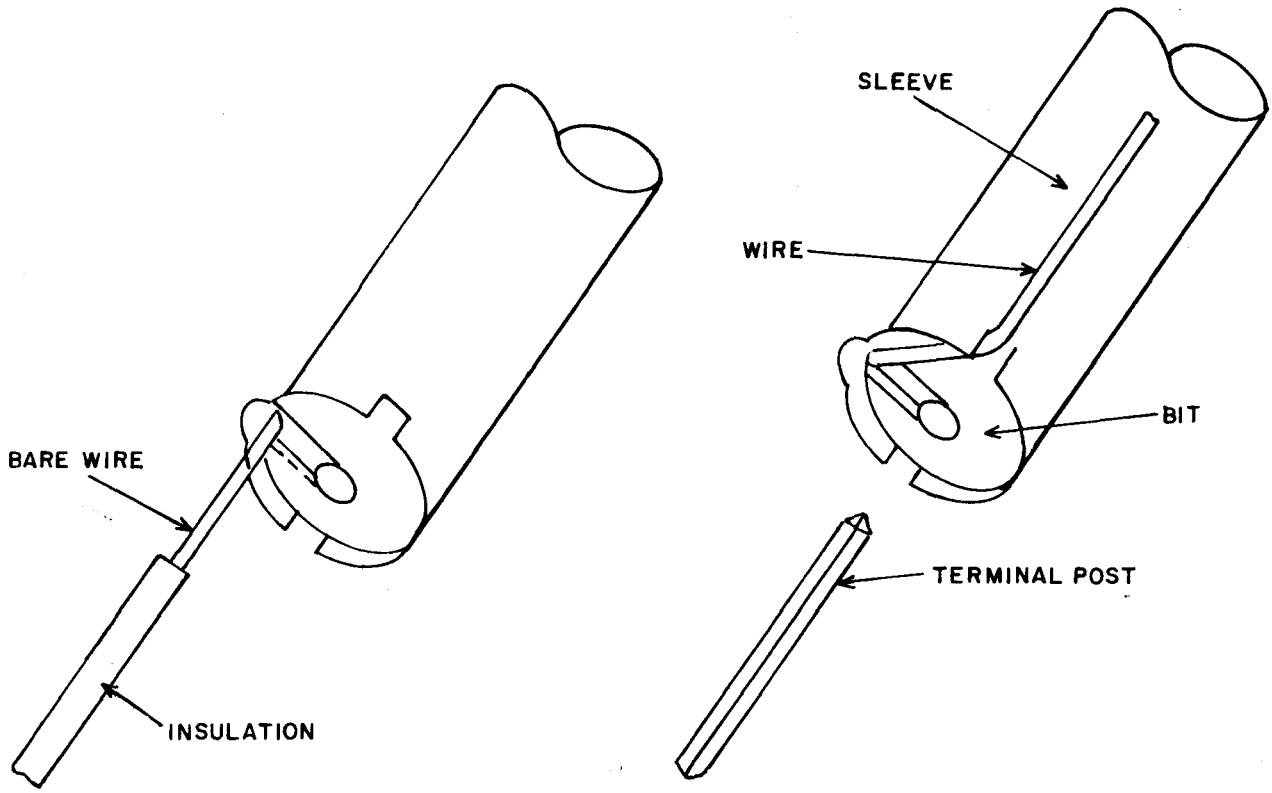


Figure 6-3. Wire Wrap Connections



A. WIRE WRAP GUN



B. INSERTION OF WIRE INTO LONGITUDINAL GROOVE.

C. POSITIONING OF GUN, WIRE, AND TERMINAL POST.

Figure 6-4. Wire Wrap Gun

The wire should be stripped of insulation as follows:

USE	IN. OF STRIPPED WIRE	IN. OF INSULATION INSERTED IN BIT
24 ga. (large pin)	1 1/2 ± 1/16	1/8
30 ga. (large pin)	1 1/2 ± 1/16	3/16
30 ga. (small pin)	1 1/8 ± 1/16	1/8

Insert the stripped end and insulation as far as it will go into the outer hole of the bit and bend the wire back along the side of the sleeve, making sure the wire passes through one of the two slots on the end of the sleeve (refer to table above for amount of insulation to be inserted). Slip the bit over the pin to the lowest level or to the designated tab level. It may be necessary to hold aside with a spring hook those wires adjacent to the pin. Wrap the wire by allowing the gun to come up on the pin while maintaining some forward pressure, so as to obtain an acceptable wrap (figure 6-3).

The wrap must have the following number of turns of bare wire and insulation:

24 ga.	Turns of bare wire-------	max. 6, min. 5
	Turns of insulation------	max. 2, min. 1/2
30 ga.	Turns of bare wire-------	max. 10, min. 7
	Turns of insulation------	max. 2, min. 1/2

The wrap must be tight on the pin. The battery in the gun must be sufficiently charged in order to deliver the proper torque required to make the wrap. The battery is of the detachable rechargeable type which is actually the handle of the gun. Removal of the battery is accomplished by twisting the handle 90° counterclockwise. On some models, a cap on the battery must first be unscrewed, then the battery can be inserted into a conventional 117 vac 60 cycle electrical outlet for a full charge of at least twelve hours of charging.

In routing the wire, there must be at least 1/32 of an inch of slack between the wire and any pin or obstruction that would cause shorting due to cold flow of the insulation, that is, when there is electrical conduction thru the insulation.

To remove a wrapped wire use the proper unwrap tool. This tool has a right and left handed end depending on which direction the wire is wrapped. The factory wire wrap machine wraps one end of the wire clockwise and the other end counterclockwise. All battery operated guns wrap clockwise. While unwrapping the ends of the wire, take care not to lose, in the chassis, any pieces of the wire that break off. Whenever removing a wire, try to verify the destination of both ends before removal to be sure it is the right one. After unwrapping each end, cut off one end and pull the wire out of the chassis via the other end. It may be necessary to use a spring hook to work the wire loose. When adding a new wire never rewrap that portion of an old wire which has been previously wrapped.

To prevent excess wear and ensure proper operation of the wire wrap bit and sleeve, clean both occasionally with chlorethene and a brush. When the wire wrap gun, bits, and sleeves are to be stored, coat them with a film of light oil to prevent any formation of rust.

(2) SOLDER CONNECTIONS. - Normal techniques employed for electronic component replacement and repair should be applied when removing and forming soldered connections.

6-3. COMPONENT REPLACEMENT AND REPAIR.

a. TEST BLOCK LOCATION. - To expose the test blocks for any chassis except the memory chassis, perform the following steps. Memory chassis test blocks are located on front panel except for machines over 32K in series serial numbers 14-48. No memory test blocks are provided on serial numbers 49 and over.

STEP 1. Use the combination tool (figure 6-1) to turn the three panel locking screws (figure 6-5) on the front of the drawer panel.

STEP 2. Swing the front panel out to expose the test blocks, connections to the switches, and indicators on the front panel (figure 6-6).

b. EXTENDING A DRAWER. - To extend a drawer from the computer, perform the following steps.

CAUTION

Remove power from the computer circuitry before extending a drawer to prevent possible damage to logic modules.

STEP 1. Swing open front panel (paragraph 6-3a).

STEP 2. Use the combination tool to turn the exposed drawer-locking screw (figure 6-6) counterclockwise until the plugs on the rear of the drawer are disengaged from the jacks on the rear panel.

CAUTION

If the computer is not securely fastened to the floor, do not extend more than one upper drawer or two lower drawers from the cabinet at any one time. Extending more than this number may upset the balance of the cabinet and tip the cabinet forward.

STEP 3. Slowly pull the drawer forward to its fully extended position. The slide catch (figure 6-7) engages when the drawer is fully extended. It may be necessary to lift the front of the drawer slightly to engage the slide catch.

STEP 4. Return the drawer into the cabinet by releasing the slide catch; push the drawer into the cabinet, and use the combination tool to turn the socket clockwise until the drawer is fully seated in the cabinet.

c. OPENING A CHASSIS. - To open the chassis and expose chassis wiring, perform the following steps:

STEP 1. Extend the drawer as listed in paragraph 6-3b, steps 1 through 4.

STEP 2. Remove the knurled, drawer locking screw from the rear chassis support (figure 6-7).

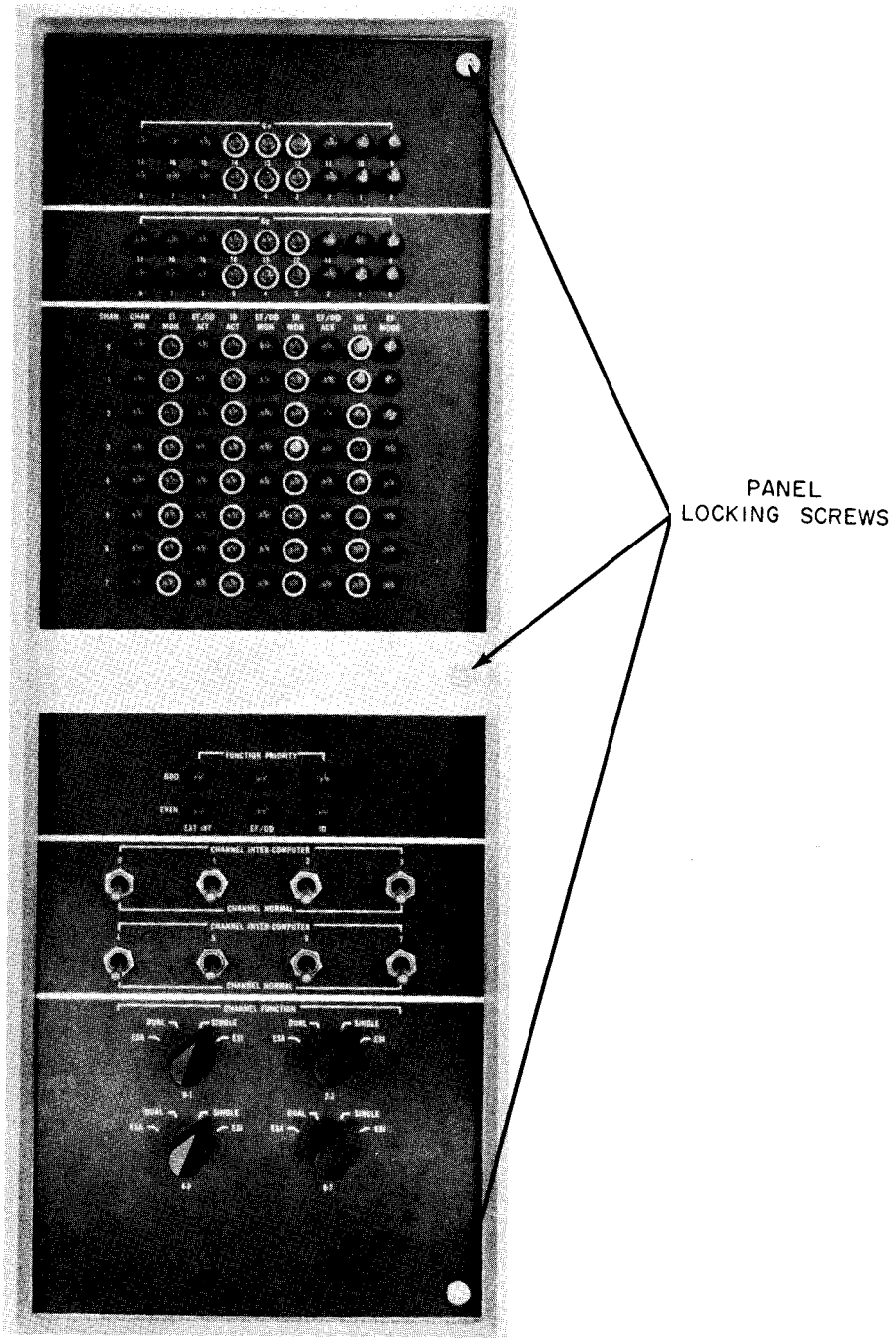


Figure 6-5. Drawer Front Panel

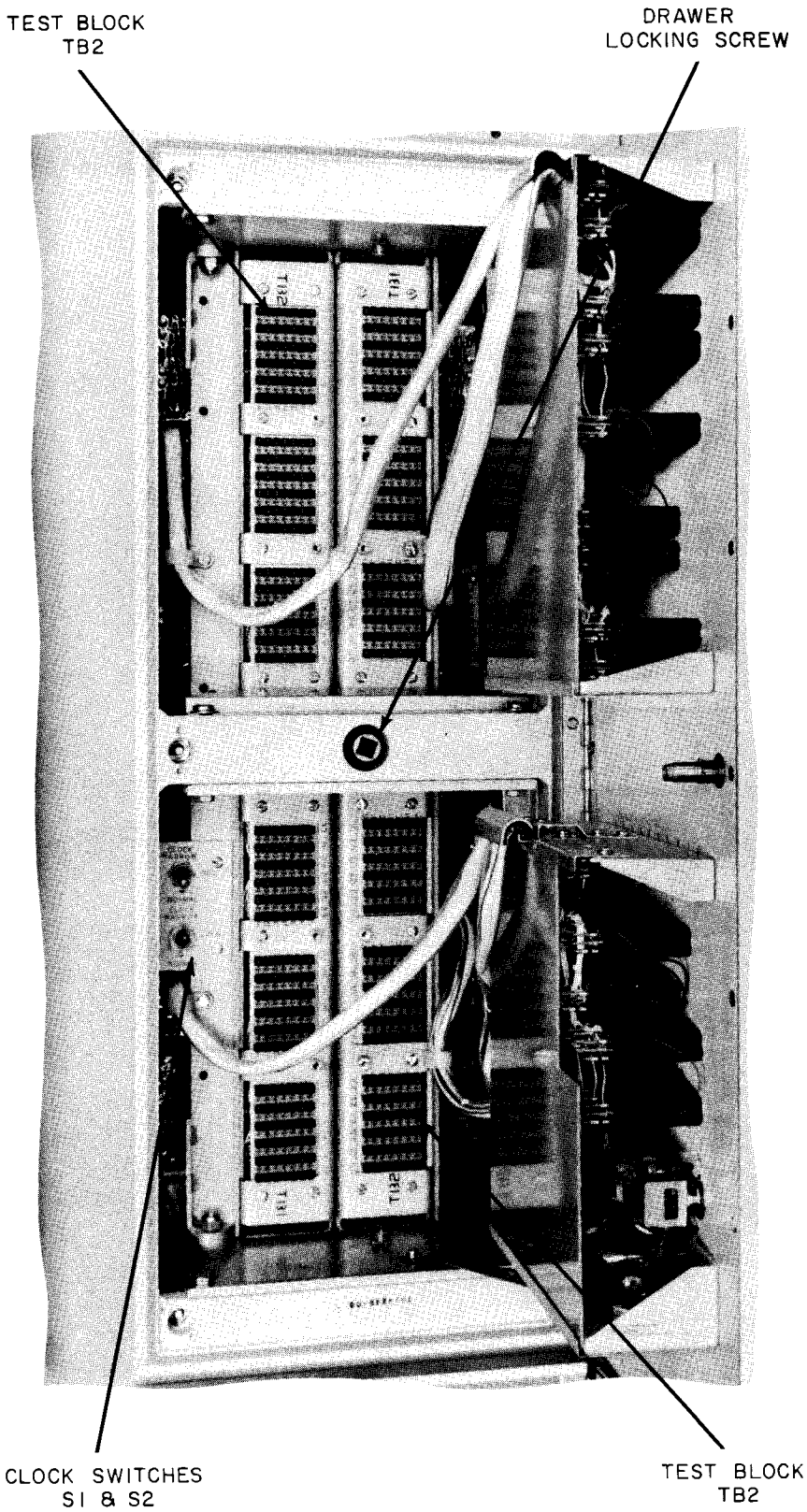


Figure 6-6. Parts Location, Panel Open

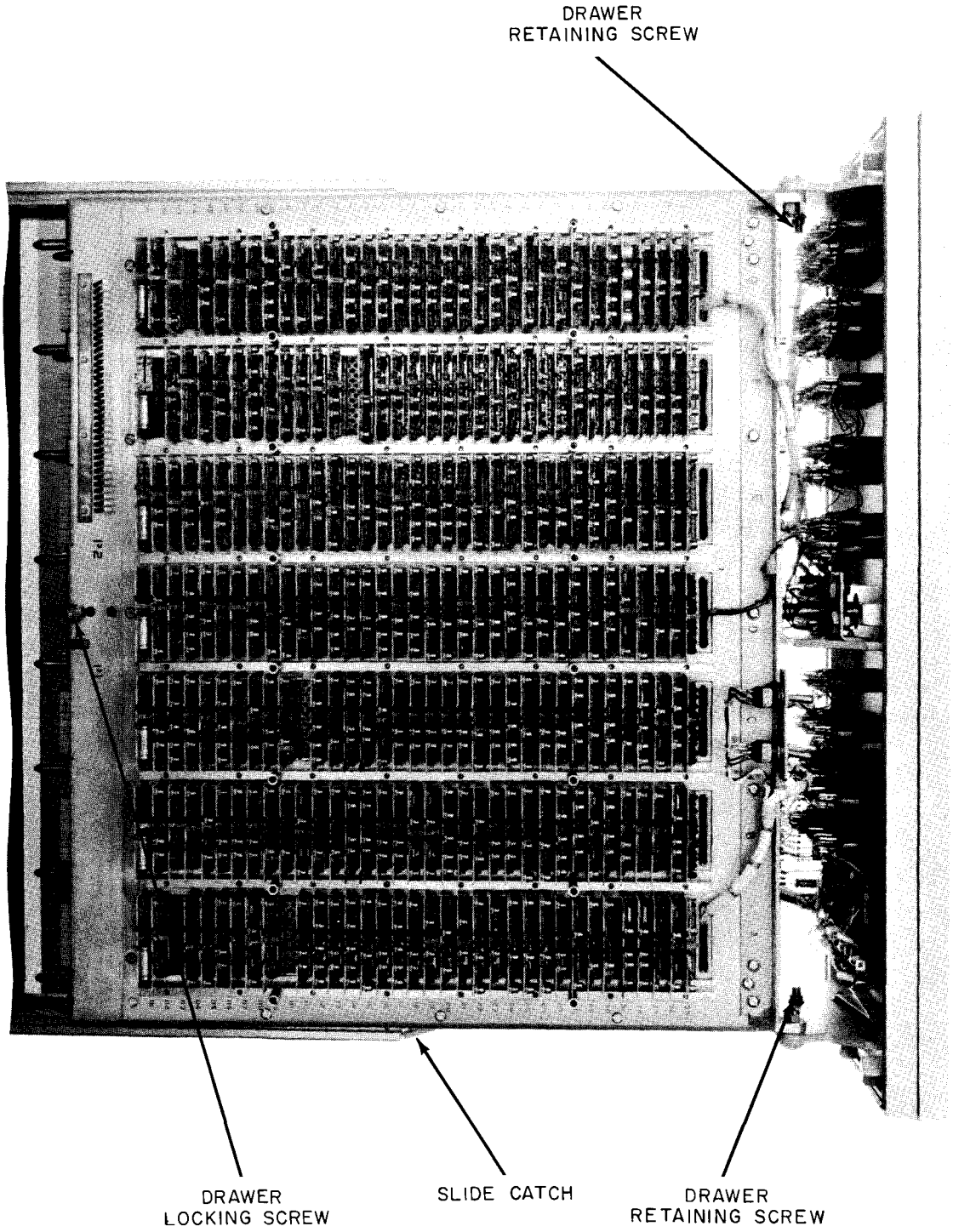


Figure 6-7. Chassis Fastener Location

STEP 3. Slowly swing the chassis on its hinges to expose the wiring (figure 6-8).

STEP 4. To secure the chassis to the drawer, follow a reverse procedure of steps 1, 2, and 3.

d. REMOVING A DRAWER. - To remove a drawer from the cabinet, perform the following steps:

STEP 1. Extend the drawer as listed in paragraph 6-3b, steps 1 through 4.

STEP 2. Remove the two flathead, drawer-retaining screws from top and bottom of the front of the drawer slide (figure 6-7).

STEP 3. Slowly withdraw the drawer from the cabinet.

e. FUSE REPLACEMENT. - Fuses control the application of operating voltage to each chassis. These fuses are located inside the cabinet directly behind the drawer with which they are associated (figure 6-9). To replace these fuses, extend the appropriate drawer and open the chassis; the fuses are now accessible.

f. TEMPERATURE-SENSING SWITCH LOCATION. - The temperature-sensing switches are located on the bottom plate of the main cabinet (figure 6-9). Access to these switches may be obtained by removing drawer A3 from the cabinet.

g. VOLTAGE-PROTECTION NETWORK LOCATION. - A voltage-protection network is provided for the input voltages to each chassis. These networks (figure 6-6) may be reached by opening the front panel.

h. EXTENDING THE POWER SUPPLY. - To extend the power supply, perform the following steps:

STEP 1. Lift the latch fasteners (figure 6-10) and turn 90 degrees.

STEP 2. Slowly slide the power supply from the cabinet until the slide catch engages.

i. REMOVING THE POWER SUPPLY. - To remove the power supply from the cabinet, perform the following steps:

STEP 1. Extend the power supply as listed in paragraph 6-3h.

STEP 2. Disconnect the two plugs from the rear of the power supply (figure 6-10).

STEP 3. Remove the four flathead screws that fasten each of the slides to the power supply chassis.

STEP 4. Use care and slowly pull the power supply from the cabinet.

j. FILTER REMOVAL. - The air filter, located behind the grill on the power control panel (figure 6-11) must be vacuum cleaned once each week. To remove the filter, perform the following steps:

STEP 1. Remove the four grill-retaining screws (figure 6-11) on the power control panel.

STEP 2. Remove the grill and filter.

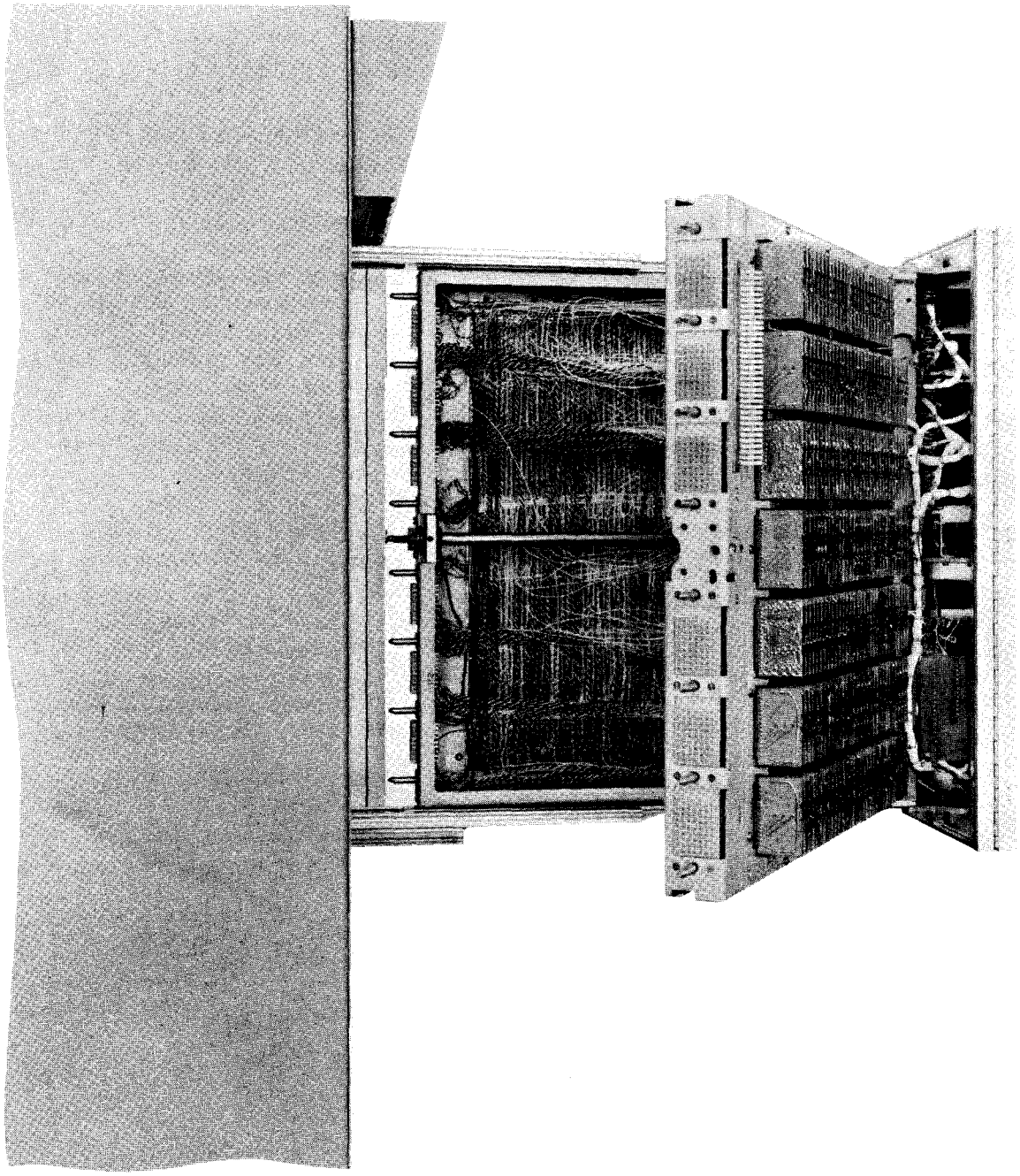


Figure 6-8. Logic Chassis Open

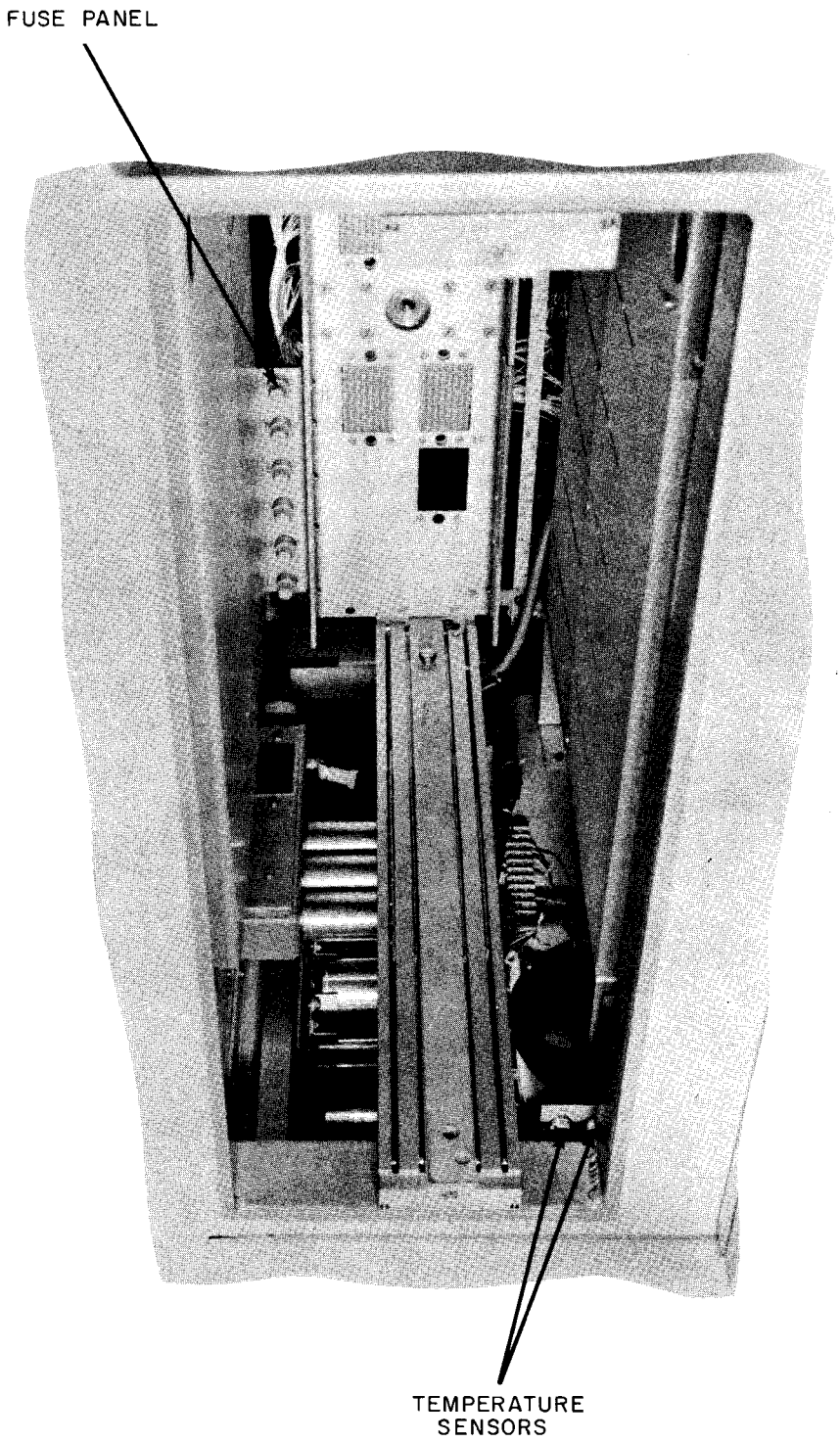


Figure 6-9. Fuse and Temperature Sensing Switch Location

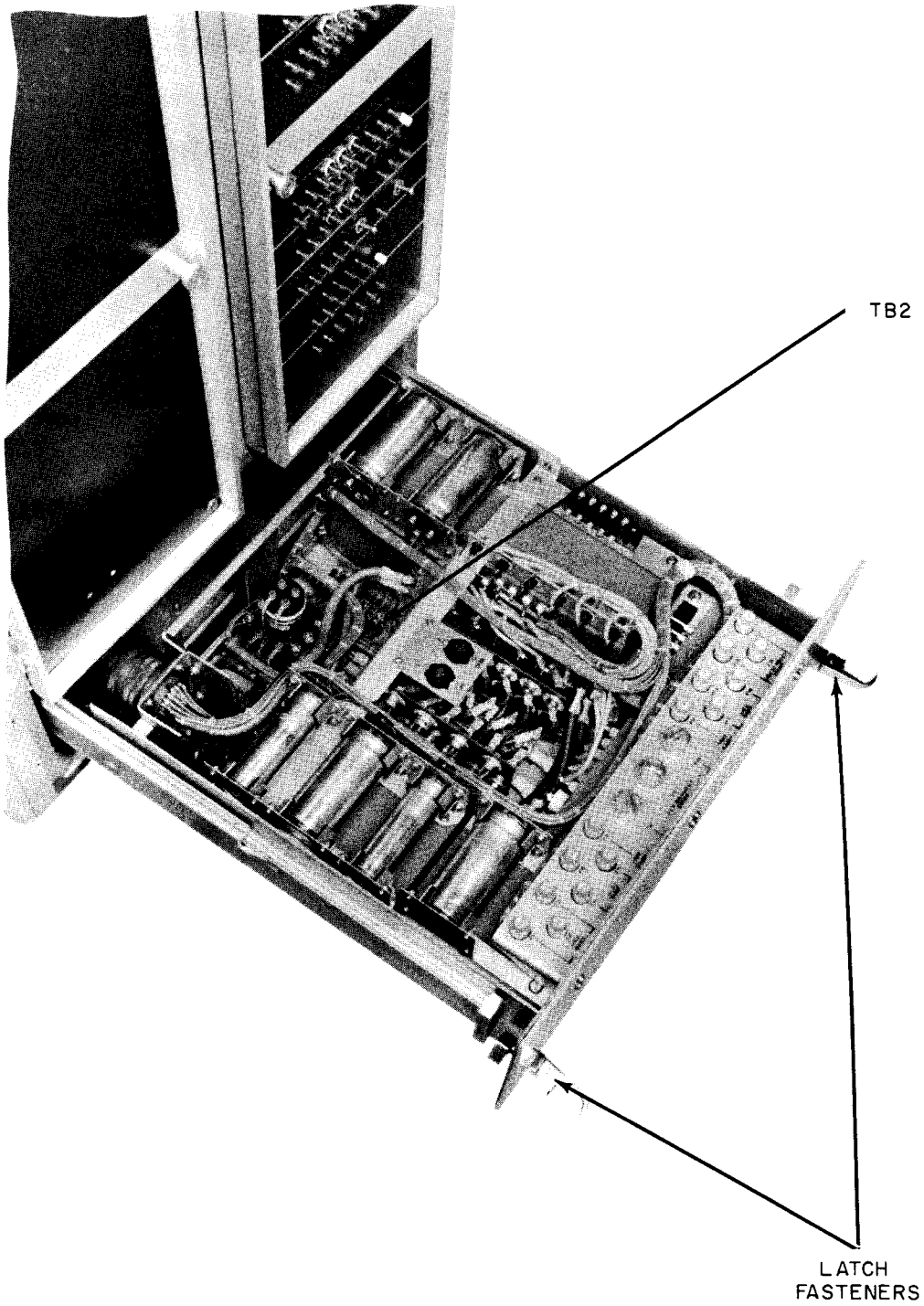


Figure 6-10. Power Supply Extended

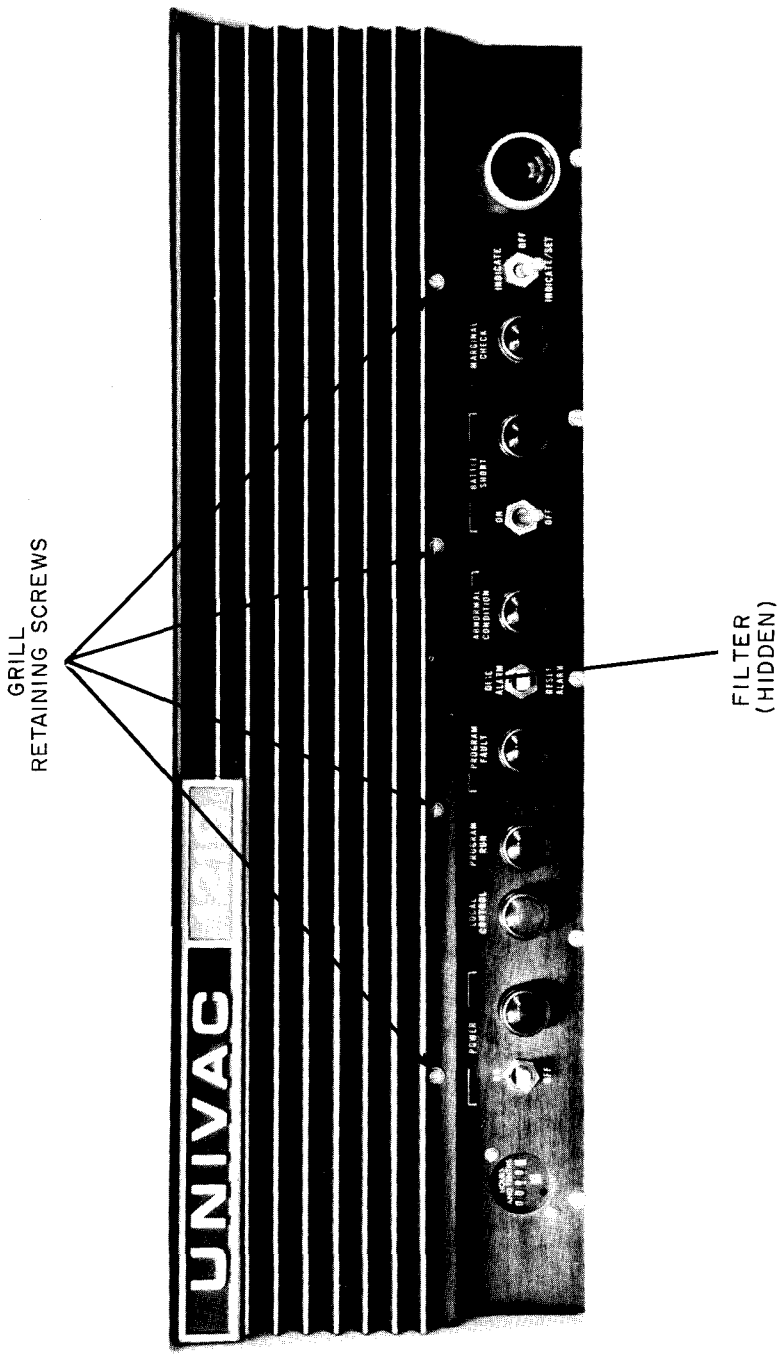


Figure 6-11. Filter Location

Every six months the filter should be removed as above and cleaned as follows:

STEP 1. Clean filter thoroughly in hot soapy water and dry with forced air.

STEP 2. Apply a thin coat of SAE #5 oil. Wipe off excess oil with a clean cloth.

STEP 3. Replace filter, ensuring that spring clips are against the grill and not the cabinet. Fasten the three grill-retaining screws.

k. CIRCUIT CARD REPLACEMENT. - When a malfunction is isolated to a particular circuit card or module, the card is replaced. This card replacement concept of troubleshooting is the lowest level of repair to be performed and simplifies repair procedures. Card replacement procedures are listed in the following steps:

STEP 1. Extend the appropriate drawer following the steps listed in paragraph 6-3b.

STEP 2. Locate the physical position of the module on the appropriate chassis. Chassis maps on figures 9-181 through 9-187 may be used for this purpose.

STEP 3. Remove the necessary hold-down strap or straps and slowly but firmly remove the module from the chassis jack.

STEP 4. Replace the module, fasten the hold-down straps and, disengaging the upper and lower drawer slide locks, slide the drawer into the cabinet.

STEP 5. Carefully tighten the screw fastener.

STEP 6. The computer is now ready for operation.

l. MEMORY STACK REPLACEMENT. - When a malfunction is isolated to a memory stack, the memory stack is replaced. It is suggested that the defective memory stack be packaged and returned to UNIVAC, Division of Sperry Rand Corp., St. Paul, Minnesota for repair.

The following paragraphs describe the procedures for replacing a main memory stack, a control memory stack, or the bootstrap assembly.

(1) MAIN MEMORY STACK REPLACEMENT. - To replace a main memory stack, perform the following steps:

STEP 1. Open the memory drawer front panel (A3).

STEP 2. To locate a faulty memory stack, refer to figure 6-12.

STEP 3. Remove the card hold-down straps.

STEP 4. Pull stack straight out.

(2) CONTROL MEMORY STACK REPLACEMENT. - To replace a control memory stack, perform the following steps:

STEP 1. Open drawer A4 according to paragraph 6-3b.

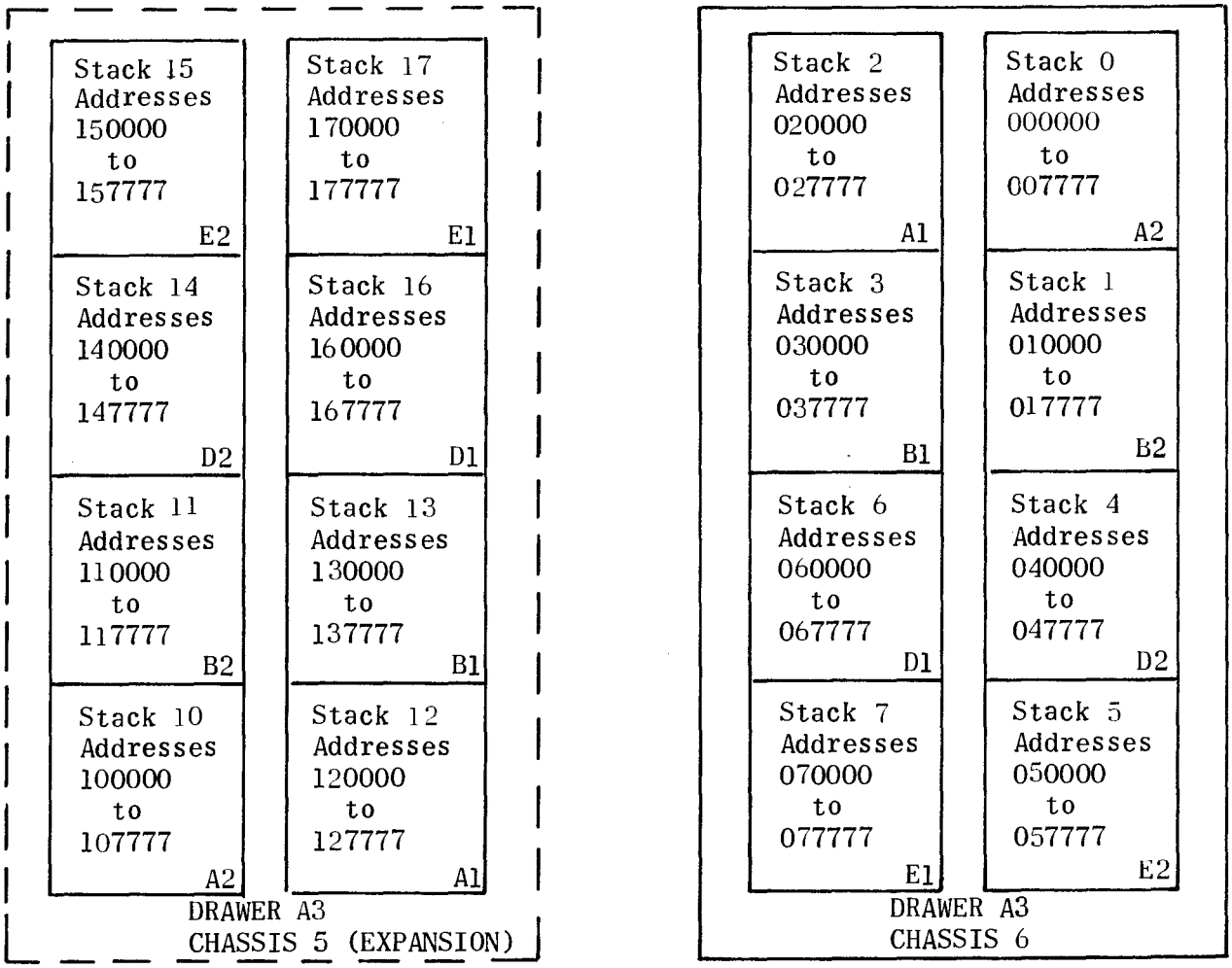


Figure 6-12. Memory Stack Location

STEP 2. Open the chassis according to paragraph 6-3c.

STEP 3. Locate and remove the four screws holding the control memory stack on the wired side of chassis A4A2. With the screws removed, the stack will not fall out.

STEP 4. Grasp the stack and pull straight out. The chassis can be closed to facilitate handling.

STEP 5. Replace with new or repaired stack; secure the four holding screws finger tight; close and fasten chassis; and secure the drawer.

(3) BOOTSTRAP ASSEMBLY REPLACEMENT. - To replace the bootstrap assembly, perform the following steps:

STEP 1. Open drawer A4 according to paragraph 6-3b.

STEP 2. Remove card hold-downs for the bootstrap row (B) and the adjacent rows (A and C).

STEP 3. Remove at least one card directly above and below the bootstrap assembly (from rows A and C).

STEP 4. Grasp bootstrap with fingers in spaces provided and pull straight out.

STEP 5. Replace with new or repaired boostrap assembly; replace cards in rows A and C.

STEP 6. Refasten card hold-downs, and secure the drawer.

6-4. MAIN MEMORY CURRENT ADJUSTMENTS.

The read and write-drive currents switch polarity of the ferrite cores in the memory stacks. The inhibit currents prevent the switching in those cores which are to contain zeros. If the read or write currents are too high, random ones are developed. If these currents are too low, a random dropping of ones usually results.

Before attempting memory current adjustments, ensure that failures, intermittent conditions, or marginal conditions do not exist in the computer logic and memory circuitry.

a. COMPUTER SETTINGS. - Make the following computer settings:

MASTER CLEAR

FUNCTION REPEAT

DISC ADV P

Set F Register to 44_8

Set P Register to 01000_8 (If checking BANK 0 on chassis 6)

Set P Register to 10000_8 (If checking BANK 0 on chassis 5)

Set P Register to 40000_8 (If checking BANK 1 on chassis 6)

Set P Register to 14000_8 (If checking BANK 1 on chassis 5)

Depress START switch

CAUTION

Do not operate the computer for any length of time without a cooling air flow. Direct an electric fan toward the chassis to prevent excessive heat build-up.

b. PROCEDURES. - Perform the following procedures:

To check the currents in BANK 0 on chassis 6, place the current probe as listed below. Values should be as shown in figure 6-13.

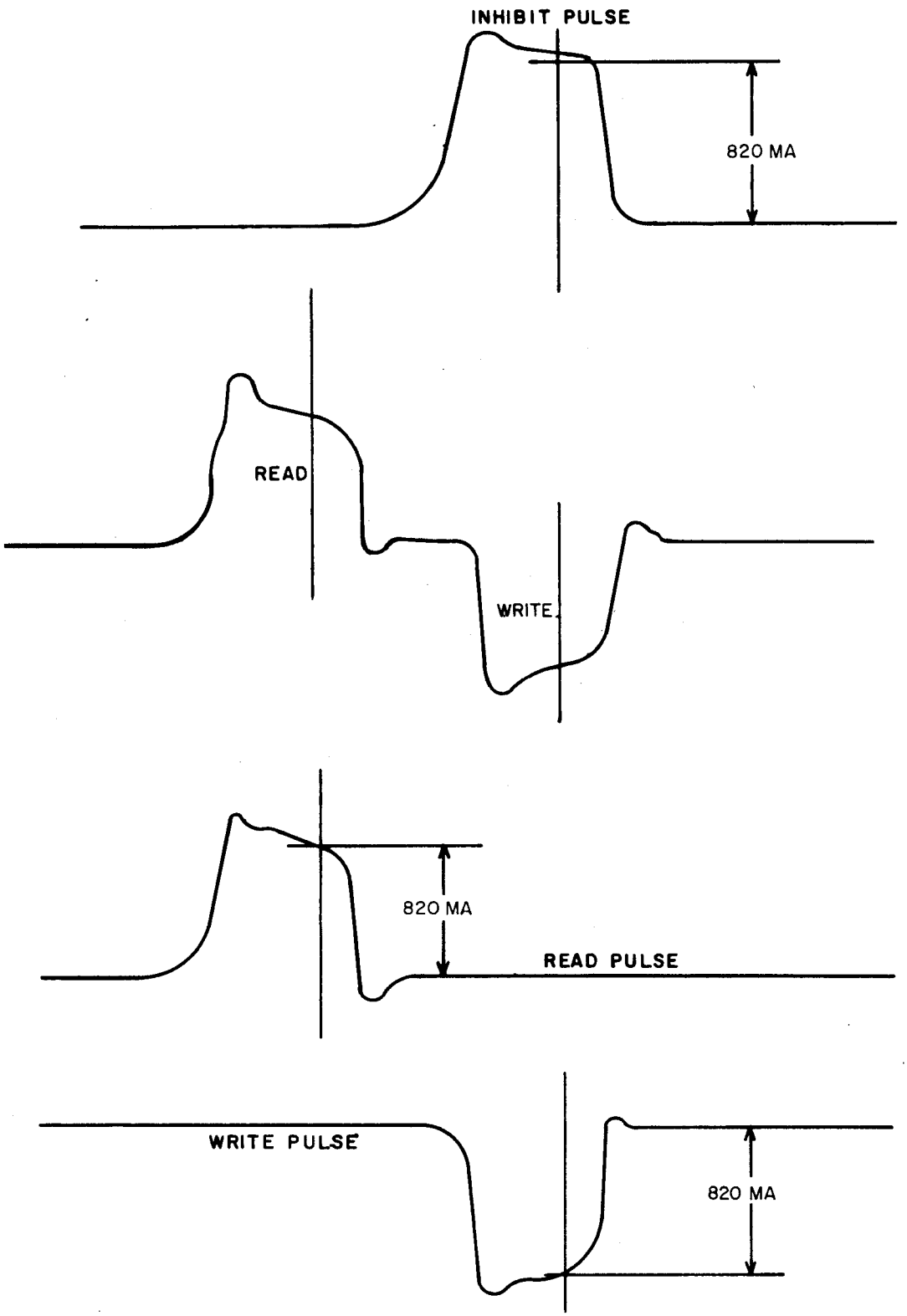


Figure 6-13. Memory Waveforms

X READ/WRITE	A1 F23	Figure 9-141	(Located behind Stack 0) (Loop)
Y READ/WRITE	A1 W2	Figure 9-144	(Located behind Stack 0) (Loop)
INHIBIT	A1 A4 and B4	Figure 9-147	(Black and white twisted pair behind Stack 0)

Set currents and voltages on the 7500780 regulator card for BANK 0 as listed below.

X READ/WRITE	820 ma P-P	(Adjust gJ30B-R9) (Top pot.)
Y READ/WRITE	820 ma P-P	(Adjust gJ30B-R10) (Second pot. down)
INHIBIT	820 ma	(Adjust gJ30B-R11) (Third pot. down)
SENSE BIAS	-6 volts at TP-5gJ30B	(Adjust gJ30B-R12) (Bottom pot.)

To check the currents in BANK 1 on chassis 6, place the current probe as listed below.

X READ/WRITE	D1 F23	Figure 9-149	(Located behind Stack 4)
Y READ/WRITE	D1 W2	Figure 9-152	(Located behind Stack 4)
INHIBIT	D1 A4 and B4	Figure 9-166	(Black and white twisted pair located behind Stack 4)

Set the currents and voltages in BANK 1 the same as for BANK 0, except use the 7500780 regulator card in location gJ30D.

To check the currents on chassis 5, follow the same procedure as for chassis 6. Pin locations for BANK 0 are located behind Stack 10 and those for BANK 1 behind Stack 14. Note that the relative positions of the adjustable pots are reversed. Pot gJ30B-R9 is the bottom pot and gJ30B-R12 is the top pot.

6-5. MAIN MEMORY STROBE TIMING CHECKS AND ADJUSTMENT.

The memory strobe gates information from the sense amplifiers to the Zm register flip-flops on the type 7500650 cards. Misadjustment of the strobe timing may cause erroneous information in the form of lost or added bits. Before a strobe adjustment is made, ensure that no failures, marginal conditions, or intermittent conditions exist in the computer circuitry.

To check memory strobe timing, perform the following:

a. COMPUTER SETTINGS. - Make the following computer settings:

RUN Mode

DISC ADV P

FUNCTION REPEAT

(F) = 010_8 (ENTAU)

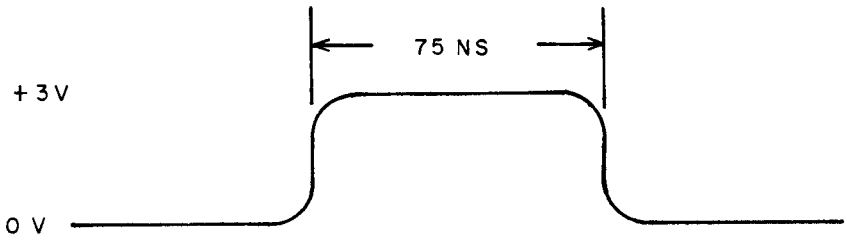
(P) = 01000_8

b. OSCILLOSCOPE SETTINGS. - Make the following oscilloscope settings:

Time	0.1 usec/cm
Trigger	EXT +, AC LF REJECT
SYNC	6TB1-F2

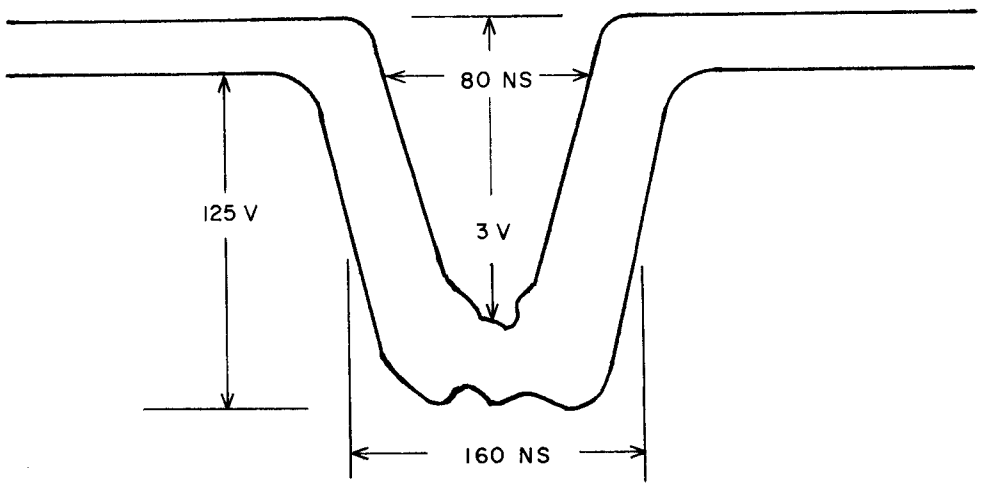
STEP 1. Press the START STEP switch and set Z1 = 777777_8.

STEP 2. Insert the Channel A probe of the dual trace preamplifier at TP3 (Strobe BANK 0). See figure 9-135. The pulse should be approximately 75 nanoseconds wide.



STEP 3. Connect the Channel B probe to TP5 of the 7500650 card at 6J38A (Bit 0 sense amplifier output). See figure 9-157.

STEP 4. Using the chopped mode on the oscilloscope preamplifier, compare the strobe timing with the output of the sense amplifier. The strobe pulse should start at about the midpoint of the sense amplifier output as shown.



STEP 5. To adjust strobe timing, move the initiating and terminating signal points on 50MT21 (7500260 card at 6J25C) to produce the pulse timing required. See figures 8-58 and 9-135. Maintain a 75 nanosecond spacing between the taps selected.

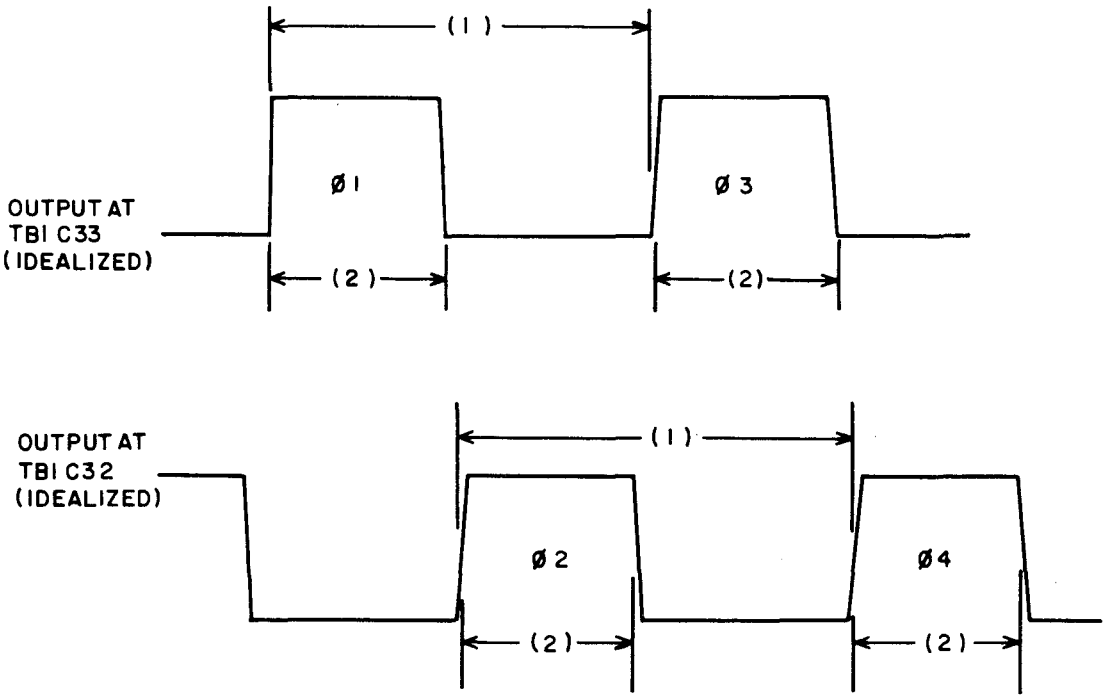
STEP 6. For memories greater than 32K, repeat the adjustments at corresponding points in chassis 5. Select address 100000_8 in P to enable the chassis 5 memory circuitry.

STEP 7. Perform the diagnostic memory test after any adjustments have been made. If errors occur, check the failing bits and readjust the strobe timing as above.

c. TESTING MEMORY. - Perform the diagnostic memory test after the memory strobe adjustments have been made. If an error occurs in the normal, high, or low margins, perform the adjustment procedures as stated in paragraph 6-5a, b. Check the sense amplifier output corresponding to the failing bits to ascertain the direction of the strobe adjustment.

6-6. CLOCK TIMING.

The frequency and duration of the clock-timing pulses are adjustable by changing the delay line tap connections shown in figure 9-4. The master clock should be adjusted only if the timing fails to meet the standards shown in figure 6-14.



(1) 250 NS
(2) 120 NS NORMAL, 80 NS NARROW.

Figure 6-14. Clock Pulse Timing

a. CYCLE-TIME ADJUSTMENT. - If the period (1) is greater than 250 nanoseconds, move the lead used for feedback c (figure 6-15) from 03DY01 to 01DD01 to a lower tap on 03DY01. If the period is less than 250 nanoseconds, move the lead to a higher tap.

b. PHASE PULSE ADJUSTMENT. - With the ODD CLOCK switch S1 (figure 6-15) in the NORMAL position, measure the pulse length (2) at TB1C33. If this length exceeds 120 nanoseconds, move lead a to a lower tap on 03DY01 or 02DY01 as required. If the pulse length is less than 80 nanoseconds, move this lead to a higher tap.

With the ODD CLOCK switch S1 in the NARROW position, measure pulse length at TB1C33. If this pulse length exceeds 70 nanoseconds, move lead d to a lower tap on 02DY01. If the pulse length is less than 50 nanoseconds, move the lead to a higher tap.

Follow the same procedure for the even phase pulses (S2), using leads b and e.

6-7. CONTROL MEMORY ADJUSTMENTS.

To adjust the control memory voltages and currents, perform the following procedures.

a. INITIAL SETTINGS. - Make the following settings:

+ VOLTAGE REGULATED SUPPLY

Measure the voltage at TB2-C33 on chassis 8 (figure 9-134). Using the pot marked +, located on the chassis next to the test points, adjust for +16 vdc.

- VOLTAGE REGULATED SUPPLY

Measure the voltage at TB2-B33 on chassis 8 (figure 9-134). Using the pot marked -, located on the chassis next to the test points, adjust for -16 vdc.

SENSE BIAS VOLTAGE SUPPLY

Extend drawer A4 and place the printed circuit card located in jack 8J20D on a card extender. Close the drawer and measure the voltage at TB2-A33. Adjust the pot on the card for -7 vdc. Perform the following steps:

STEP 1. Place FUNCTION REPEAT switch in the up position.

STEP 2. Place DISC ADV P switch in the up position.

STEP 3. Set the FUNCTION CODE pushbutton switch/indicators to 44_8.

STEP 4. Set the AL register to all "ones".

STEP 5. Press the RUN MODE pushbutton switch indicator and press the RESTART/START STEP switch to the START STEP position.

STEP 6. Connect the external trigger on the oscilloscope to TB2-C10 on chassis 8. Compare the strobe pulse observed at TB1-G25 on chassis 8 with the sense readout for bit 0 observed at TB2-A31. Note that the strobe pulse is wider than, and completely brackets, the sense readout for bit 0.

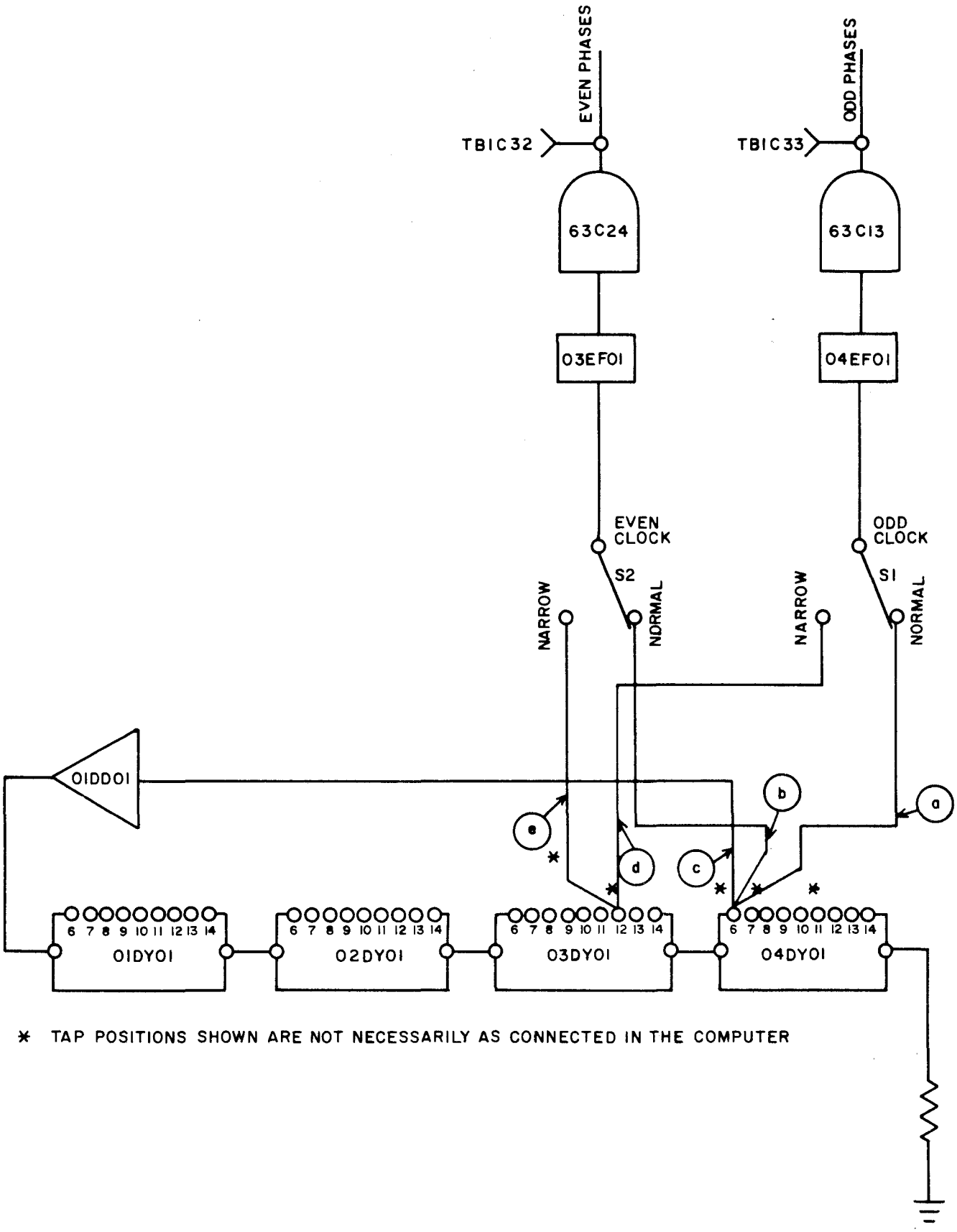


Figure 6-15. Phase Generator, Simplified

STEP 7. If the strobe pulse width exceeds 80 nanoseconds (±5 nanoseconds), adjust the Strobe Initiation (input to 30EF04) and Strobe Termination (input to 30EF05) taps to provide an 80-nanosecond (±5 nanoseconds) pulse that brackets the sense readout pulse as shown in figure 6-16.

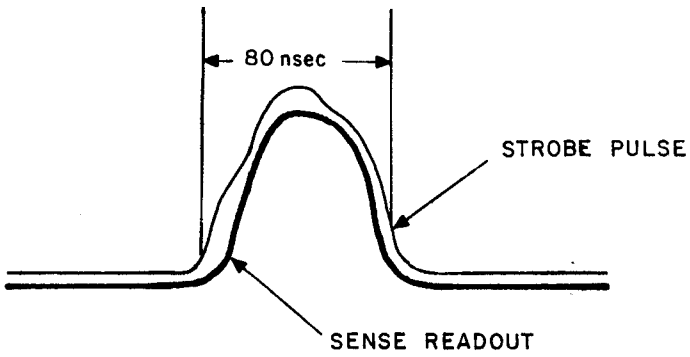


Figure 6-16. Strobe Pulse-Sense Readout Comparison

STEP 8. Place the DISC ADV P switch in the down position and ground bit 6 of the P register (test point TB1-A31 on chassis A4). Cycle the computer through the lower 100_8 addresses of control memory.

Observe all sense outputs (figure 9-131) and insure that the strobe pulse completely brackets each output.

It may be necessary to readjust the sense bias voltage to widen or narrow the readout for the weakest pulse.

STEP 9. Load and run the FACT Control Memory test to insure that a recheck and/or readjustment of the timing is not necessary.

STEP 10. With the FACT Control Memory test cycling properly, check the voltage at TB2-C33 on chassis 8 and raise the +V voltage until the test fails. Record this voltage.

STEP 11. Lower the voltage slightly and restart the test. Lower the voltage until the test again fails. Record this voltage.

STEP 12. Set the +V voltage at the midpoint between the two recorded values.

STEP 13. Adjust the -V voltage in the same manner, using test point TB2-B33 to monitor this voltage.

READ/WRITE CURRENTS

It is unlikely that it will be necessary to change the settings made in paragraph 6-7a on previous page. In most cases, with the control memory test running, the pots can be turned through their full range without error. If an error should occur at the far end of the pots, a bad memory is not indicated.

b. READ/WRITE CURRENT MEASUREMENTS. - The read/write current pots should be variable from minimum to maximum without causing an error in the test, if the voltage adjustments are properly made. However, an error occurring at the extreme ends of these pots does not necessarily mean that the control memory is bad. Some computers just will not have as good margins as others. Failures of the same bits would indicate marginal sense amplifiers or digit driver cards. Sense bias voltage may have to be touched up while observing "worst-case" sense outputs to ensure proper operation.

The read/write current pots should be returned to approximately their midpoint range. By reading continuously out of a control memory address, measure the current pulses with a current probe. The read current should be between 400-500 ma. and the write current between 300-400 ma.

If the S/N is 1 through 9, wires M1 and M2 going into J41 on the control memory allow checking of both currents at the same time. Wire M1 is for checking the read current and the upper pot is the adjustment. Wire M2 is for checking the write current and the lower pot is the adjustment.

On S/N 10 and above, the two jumper wires between two studs located by the read/write pots allow checking of the currents without removing the chassis. The upper wire TP-1 is for checking the read current and the upper pot is the adjustment.

While observing the memory currents, if you vary the pots from one limit to the other, the read current should vary approximately 150 ma. and the write current approximately 100 ma. If the currents fail to vary while changing the pots, the indication would be a failing part in the associated circuitry. It is also possible that the control memory timing is misadjusted; however, if it hasn't been touched it should be correct.

If the control memory is operating satisfactorily, the following adjustments can be made without error while cycling the control memory test.

VOLTAGE	FROM	TO
+VDC	+12 vdc	+19 vdc
-VDC	-10 vdc	-20 vdc

6-8. VOLTAGE FAULT ADJUSTMENT.

There are two detection circuits which must be adjusted for 104 and 101 vac input logic power respectively. These circuits enable the computer's memory to retain data during a power loss or line transient.

At 104 volts the voltage fault and abnormal condition indicators light and the alarm sounds. If battle short is on, the computer continues to run; if not, the memory cycle in process is allowed to finish and the program run indicator is then extinguished.

At 101 volts the detection circuit in each 32K section of the memory drawer disables the inhibit drivers regardless of the position of the battle short switch. After a power failure condition, the computer must be turned off and power reapplied to enable the inhibit drivers.

a. 104 VOLT CIRCUIT ADJUSTMENT. - To adjust the 104 volt circuit, perform the following steps:

STEP 1. Remove power from the equipment.

STEP 2. Connect a variac to the 400 cycle input line.

STEP 3. Open chassis A4A1 and remove the 2880 and 3720 cards at locations J34E and J34F respectively.

STEP 4. Insert card extender in J34E and close the chassis.

STEP 5. Put the 2880 card in the extender and connect a scope probe to test point A7TB2-D25 (12G81 on figure 9-134).

STEP 6. Bring up power and adjust the variac to 104 volts.

STEP 7. Adjust one of the potentiometers on the 2880 card until the signal on the scope has just gone negative and then back it off so that it is just positive again. Then adjust the other potentiometer on the card until it goes negative and back it off so that is is just positive again.

STEP 8. Adjust the variac to about 110 volts, then master clear the computer.

STEP 9. Reduce the variac until the computer voltage fault indicator lights. This is the voltage fault voltage.

STEP 10. Re-adjust the variac to 104 volts.

STEP 11. De-energize the equipment and move the card extender to J34F of the same chassis.

STEP 12. Remove the 2880 card from the card extender and insert the 3720 card.

STEP 13. Energize the equipment.

STEP 14. Adjust the potentiometer on the 3720 card until the signal on the scope has just gone negative and back it off so that it just goes positive again.

STEP 15. Repeat steps 8 and 9.

STEP 16. De-energize the equipment.

STEP 17. Remove the card extender and re-insert the 2880 and 3720 cards in 34E and 34F respectively.

STEP 18. Energize the computer and repeat steps 8 and 9 with the same results. If not, re-adjust the cards and compensate for any variance due to the use of the card extender.

b. 101 VOLT CIRCUIT ADJUSTMENT. - To adjust the 101 volt circuit, perform the following steps:

STEP 1. Connect a scope probe to test point TP1 on the 0340 card at J11C of chassis A3A2 (the first 32K of memory) (00V500 on figure 9-145).

STEP 2. Adjust the variac to 101 volts.

STEP 3. Adjust the potentiometer on the 0340 card at J11C of chassis A3A2 until the signal on the scope has just gone negative and then back it off so that it is just positive again.

STEP 4. Repeat steps 1 thru 3 for chassis A3A1 if the computer has more than 32K of memory.

STEP 5. Remove the variac and reconnect the 400 cycle input line.

The memory protection circuits can be checked by running any maintenance program and dropping input power. When the computer is turned on and the program is restarted it should run without any instruction loss. Note that memory tests must be restarted at their proper starting address.

SECTION 7

PARTS LIST

7-1. INTRODUCTION

The Maintenance Parts List identifies assemblies and detail parts contained in the computer. The parts list should not be used for disassembly or assembly procedures.

7-2. GROUP ASSEMBLY PARTS LIST

The group assembly parts list consists of illustrations and listings of assemblies and detail parts. The accompanying illustration precedes the parts breakdown listing for each assembly. Each assembly listed is followed by a breakdown of the component parts.

a. FIGURE AND INDEX COLUMN. This column shows the section number, a figure number of the assembly and all index numbers assigned to its component parts.

b. REFERENCE DESIGNATION COLUMN. This column lists the reference designator assigned to the assembly or detail part. These designators coincide with the designations marked on the equipment, drawings, and diagrams.

c. PART NUMBER COLUMN. This column lists the Univac part numbers except when government or vendor part numbers are listed.

A Coml entry indicates that the part may be procured commercially.

d. INDENT COLUMN. This column is coded alphabetically to show relationship to the next higher assembly.

e. DESCRIPTION. This column lists the item name of a part or assembly, followed by an identifying description. Whenever parts are procured from a vendor, the vendor's part number is listed in the Part Number column and the vendor's code "(00000)" is placed after the description of the item. These codes are listed in numerical sequence in table 7-1. The vendor code is followed by the contractor's specification control drawing number in parenthesis. Attaching parts are listed immediately following the assembly or part, which they secure.

Two abbreviations appear in the description column NHA and (AP). NHA indicates next higher assembly. The (AP) indicates attaching parts.

f. UNITS PER ASSEMBLY. This column lists the quantity of parts per assembly. When equipment contains two or more identical assemblies, or if similar assemblies have been combined in one illustration, the column will indicate the quantity of parts for one assembly only.

Two abbreviations are used in this column, Ref and Ar. Ref indicates that the quantity of an assembly has been previously considered. AR indicates a quantity as required.

g. USABLE ON CODE COLUMN. Letter codes in this column indicate variations of parts and assemblies which because of their physical similarity have been combined on one illustration. The absence of a code signifies the part is used on all assemblies.

TABLE 7-1. VENDOR CODES

Code	Name and Address
00736	Air-Maze, Division of North American Rockwell Corp., Air-Maze Plant 25000 Miles Road Cleveland, Ohio 44128
01021	Aldrich Co. E. Williams Road Wyoming, Illinois 61491
03508	General Electric Co. Semiconductor Products Dept. Electronics Park, Syracuse, N.Y. 13201
04713	Motorola Semiconductor Products Inc. 5005 E. McDowell Rd. Phoenix, Arizona 85008
05236	Jonathan Mfg. Co. 720 E. Walnut Fullerton, California 92632
07137	TEC Inc. 6700 Washington Ave South Eden Prairie, Minn. 55433
08524	Deutsch Fastener Corp. Los Angeles, Calif.
09922	Burndy Corp. Richards Ave. Norwalk, Conn. 06852
13327	Solitron Devices Inc. 256 Oak Tree Rd. Tappen, N.Y. 10983
15605	Cutler-Hammer Inc. Speciality Products Division 4201 N. 27th Street Milwaukee, Wisc. 53216
16512	National Connector Corp. 9210 Science Center Minneapolis, Minn. 55429
17771	Singer Co., The Diehl Division, Finderne Plant Finderne Ave. Somerville, N.J. 08876
37942	Mallory, P. R. and Co. 3029 E. Washington St. Indianapolis, Ind. 46206
43766	Nice Ball Bearing Co. 30th and Huntington Park Ave. Philadelphia, Pa. 19140
56289	Sprague Electric Co. Marshall St. N. Adams, Mass. 01247
71468	ITT Cannon Electric Inc. 3208 Humbolt St. Los Angeles, Calif. 90031
71744	Chicago Miniature Lamp Works 4433 Ravenswood Ave. Chicago, Ill. 60640
72619	Dialight Corp. 60 Stewart Ave. Brooklyn, N.Y. 11237
75382	Kulka Electric Co. 520 So. Fulton Ave. Mt. Vernon, N.Y. 10550
80023	Schott, Oscar A. Co. 500 11th Ave. So. Minneapolis, Minn. 55415
80183	Sprague Products Co. 99 Marshall St. N. Adams, Mass.
80294	Bourns Inc. 1200 Columbus Ave. Riverside, Calif. 92507
81312	Winchester Electronics Division, Litton Industries Inc. Main St. and Hillside Ave. Oakville, Conn.
81349	Military Specifications Promulgated by Standardization Division of Logistic Services DSA

TABLE 7-1. VENDOR CODES (CONT.)

Code	Name and Address
82647	Metals and Controls Inc., Control Products Group 34 Forest St. Attleboro, Mass. 02703
82805	Metal Textile Co. 647 E. 1st Ave. Roselle, N.J. 07203
82877	Rotron Inc. 7-9 Hasbrouck Lane Woodstock, N.Y. 12498
84613	Fuse Indicator Corp. 5900 Fishers Lane Rockville, Md. 20850
84830	Lee Spring Co., Inc. 30 Main St. Brooklyn, N.Y. 11201
90536	UNIVAC, Division of Sperry Rand Corp., Federal Systems Division Univac Park P.O. Box 3525 St. Paul, Minn. 55101
91506	Augat Inc. 33 Perry Ave. Attleboro, Mass. 02703
91637	Dale Electronics Inc. P.O. Box 609 Columbus, Nebr. 60601
91885	Major Plastic Products Co. 2515 S.E. Mail-Well Dr. Portland, Oreg. 97222
91886	Malco Mfg. Co. Inc. 5150 W. Roosevelt Rd. Chicago, Ill. 60650
91929	Honeywell, Inc. Microswitch Division, Chicago and Spring Streets Freeport, Ill. 61032
95267	Philamon Laboratories Inc. 90 Hopper St. Westbury, L.I., N.Y. 11590
96881	Thomson Industries Inc. 1029 Plandome Rd. Manhasset, N.Y. 11030
96906	Military Specifications Promulgated By Standardization Division of Logistic Services DSA

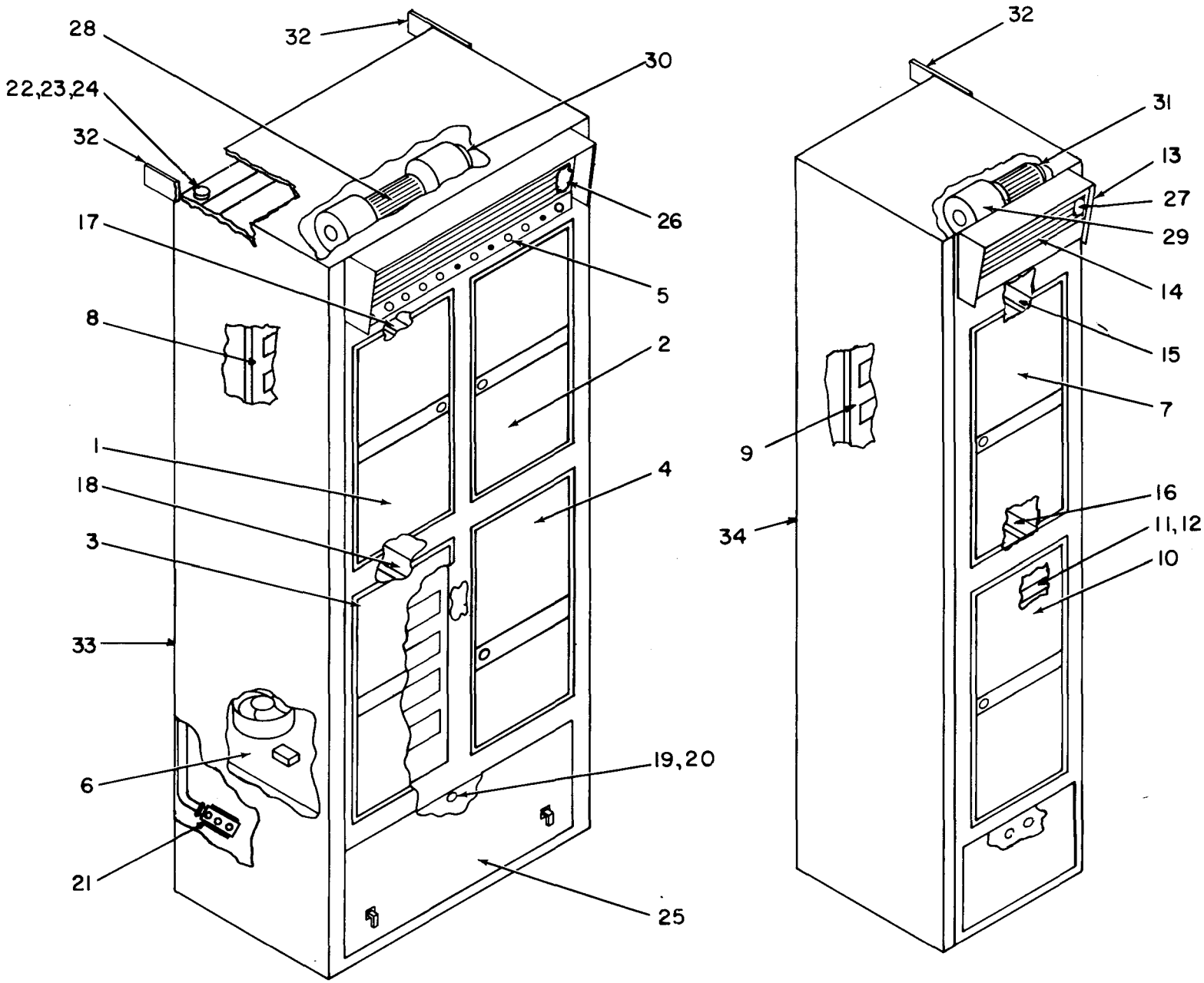


Figure 7-1. Digital Data Computer, (front view)

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
7- 1		A	COMPUTER, DIGITAL DATA	90536	7049747-00	REF	A
		A	COMPUTER, DIGITAL DATA	90536	7049747-01	REF	B
		A	COMPUTER, DIGITAL DATA	90536	7049747-02	REF	C
		A	COMPUTER, DIGITAL DATA	90536	7049747-03	REF	D
		A	COMPUTER, DIGITAL DATA	90536	7049747-04	REF	E
		A	COMPUTER, DIGITAL DATA	90536	7049747-05	REF	F
		A	COMPUTER, DIGITAL DATA	90536	7049747-06	REF	G
		A	COMPUTER, DIGITAL DATA	90536	7049747-07	REF	H
		A	COMPUTER, DIGITAL DATA	90536	7049747-08	REF	I
		A	COMPUTER, DIGITAL DATA	90536	7049747-09	REF	J
		A	COMPUTER, DIGITAL DATA	90536	7049747-10	REF	K
		A	COMPUTER, DIGITAL DATA	90536	7049747-11	REF	L
		B	ACCESSORY, INTEGRAL, I/O AND MEMORY	90536	7051213-00	1	A,D, I
		B	ACCESSORY, INTEGRAL, I/O AND MEMORY	90536	7051213-01	1	G
		B	ACCESSORY, INTEGRAL, I/O AND MEMORY	90536	7051213-02	1	J
		B	ACCESSORY, INTEGRAL, I/O AND MEMORY	90536	7051213-03	1	L
		B	ACCESSORY, INTEGRAL, I/O AND MEMORY	90536	7051229-00	1	H
		B	ACCESSORY, INTEGRAL, I/O AND MEMORY	90536	7051229-01	1	B,C
		B	ACCESSORY, INTEGRAL, I/O AND MEMORY	90536	7051229-02	1	E,F, K
		B	ACCESSORY, INTEGRAL, BASIC GROUP	90536	7045233-01	1	
		B	ACCESSORY, INTEGRAL, COMPUTER, AIR COOLED	90536	7053785-00	1	A,D, G,I, L
		B	ACCESSORY, INTEGRAL, COMPUTER, AIR COOLED	90536	7053785-01		J
		B	ACCESSORY, INTEGRAL, COMPUTER, AIR COOLED	90536	7051228-00		B,C, E,F, H,K

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
1-1	A1	C	CONVERTER, DIGITAL TO DIGITAL /FOR BREAKDOWN SEE FIG 7-2/	90536	7053795-01	1	A THRU G, I THRU L
	A1	C	CONVERTER, DIGITAL TO DIGITAL /FOR BREAKDOWN SEE FIG 7-2/	90536	7053795-05	1	H
-2	A2	C	CONVERTER, DIGITAL TO DIGITAL /FOR BREAKDOWN SEE FIG 7-2/	90536	7053795-02	1	
-3	A3	C	MEMORY DRAWER ASSEMBLY /FOR BREAKDOWN SEE FIG 7-3/	90536	7053750-00	1	A, D, E, F, G, I, K
	A3	C	MEMORY DRAWER ASSEMBLY /FOR BREAKDOWN SEE FIG 7-3/	90536	7053750-01	1	J
	A3	C	MEMORY DRAWER ASSEMBLY /FOR BREAKDOWN SEE FIG 7-3/	90536	7053750-02	1	H
	A3	C	MEMORY DRAWER ASSEMBLY /FOR BREAKDOWN SEE FIG 7-3/	90536	7053750-03	1	B, C
	A3	C	MEMORY DRAWER ASSEMBLY /FOR BREAKDOWN SEE FIG 7-3/	90536	7053750-04	1	L
-4	A4	C	CONVERTER, DIGITAL TO DIGITAL /FOR BREAKDOWN SEE FIG 7-2/	90536	7053795-03	1	
-5	A5	C	HOOD ASSEMBLY, CONTROL-INDICATOR /FOR BREAKDOWN SEE FIG 7-4/	90536	7050307-01	1	
-6	A6	C	FAN ASSEMBLY, AXIAL /FOR BREAKDOWN SEE FIG 7-16/	90536	7033221-01		
-7	A8	C	CONVERTER, DIGITAL TO DIGITAL /FOR BREAKDOWN SEE FIG 7-2/	90536	7053795-00	1	A, D, I, J, L
		C	CONVERTER, DIGITAL TO DIGITAL /FOR BREAKDOWN SEE FIG 7-2/	90536	7053795-04	1	G
-8	A12	C	CONNECTOR ASSEMBLY, ELECTRICAL /FOR BREAKDOWN SEE FIG 7-5/	90536	7053799-00	1	
-9	A13	C	CONNECTOR ASSEMBLY, ELECTRICAL /FOR BREAKDOWN SEE FIG 7-6/	90536	7025669-06	1	A, D, G, I, J, L
-10		C	DOOR AND PANEL ASSEMBLY /FOR BREAKDOWN SEE FIG 7-12/	90536	7019284-32		A, D, G, I, J, L

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
1		C	SCREW, PAN HD, 0.25-20UNC-2A BY 0.875 IN. LG /AP/		4912509-03 COML	4	A,D, G,I, J,L
		C	WASHER, FLAT, 0.25 IN. ID /AP/	96906	MS15795-810	4	A,D, G,I, J,L
-11		C	RETAINER, PANEL	90536	7033262-00	2	A,D, G,I, J,L
-12		C	BRACKET, PANEL	90536	7025732-00	2	A,D, G,I, J,L
		C	SCREW, PAN HD, 0.25-20-2A BY 0.625 IN. LG /AP/		4912528-03 COML	4	A,D, G,I, J,L
		C	WASHER, FLAT, 0.25 IN. ID /AP/	96906	MS15795-810	4	A,D, G,I, J,L
-13		C	HOOD, CABINET	90536	7050305-00	1	A,D, G,I, J,L
		C	SCREW, PAN HD, 6-32UNC-2A BY 1.75 IN. LG /AP/		4912524-13 COML	4	A,D, G,I, J,L
		C	SCREW, PAN HD, 6-32UNC-2A BY 0.375 IN. LG /AP/		4912524-02 COML	4	A,D, G,I, J,L
		C	WASHER, FLAT, NO. 6 /AP/	96906	MS15795-805	8	A,D, G,I, J,L
-14		C	GRILLE, HOOD	90536	7050304-00	1	A,D, G,I, J,L
		C	SCREW, PAN, HD, 6-32UNC-2A BY 1.0 IN. LG /AP/		4912524-10 COML	3	A,D, G,I, J,L
		C	WASHER, FLAT, NO. 6 /AP/	96906	MS15795-805	3	A,D, G,I, J,L
		C	SCREW, PAN HD, 8-32UNC-2A BY 0.375 IN. LG /AP/		4912525-02 COML	2	A,D, G,I, J,L
		C	WASHER, FLAT, NO. 8 /AP/	96906	MS15795-807	2	A,D, G,I,

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
1							J,L
		C	WASHER, LOCK, NO. 8 /AP/	96906	MS35338-137	2	A,D, G,I, J,L
		C	STOP, GRILLE /AP/	90536	7050302-00	2	A,D, G,I, J,L
		C	SLIDE, PACKAGE	90536	7024737-00	1	A,D, G,I, J,L
-15		D	SLIDE, TELESCOPING	05236	7900790-00 3502358	1	A,D, G,I, J,L
-16		D	SLIDE, TELESCOPING	05236	7900790-01 3502357	1	A,D, G,I, J,L
		D	SPACER, SLEEVE /AP FOR INDEXES 15 AND 16/	90536	7019272-00	2	A,D, G,I, J,L
		D	SCREW, PAN HD, 0.312-18UNC-2A BY 0.5 IN. LG /AP FOR INDEXES 15 AND 16/		4912530-00 COML	2	A,D, G,I, J,L
		D	SCREW, FLAT HD, 0.312-24UNF-2A BY 0.875 IN. LG /AP FOR INDEXES 15 AND 16/		908542-05 COML	2	A,D, G,I, J,L
		D	SCREW, PAN HD, 10-32UNF-2A BY 1.25 IN. LG /AP FOR INDEXES 15 AND 16/		4912527-07 COML	8	A,D, G,I, J,L
		D	SCREW, FLAT HD, 0.25-28UNF-2A BY 0.875 IN. LG /AP FOR INDEXES 15 AND 16/		4912509-03 COML	6	A,D, G,I, J,L
		D	WASHER, FLAT, NO. 10 /AP FOR INDEXES 15 AND 16/	96906	MS15795-808	8	A,D, G,I, J,L
		D	WASHER, LOCK, NO. 10 /AP FOR INDEXES 15 AND 16/	96906	MS35338-138	8	A,D, G,I, J,L
		D	SHIM, .3 IN. LG /AP FOR INDEXES 15 AND 16/	90536	254269-00	AR	A,D, G,I J,L
		D	SHIM, .3 IN. LG /AP FOR INDEXES 15 AND 16/	90536	254269-01	AR	A,D, G,I, J,L

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
1		D	SHIM, 3 IN. LG /AP FOR INDEXES 15 AND 16/	90536	254269-02	AR	A,D, G,I, J,L
		D	SHIM, 3.5 IN. LG /AP FOR INDEXES 15 AND 16/	90536	254270-00	AR	A,D, G,I, J,L
		D	SHIM, 3.5 IN. LG /AP FOR INDEXES 15 AND 16/	90536	254270-01	AR	A,D, G,I, J,L
		D	SHIM, 3.5 IN. LG /AP FOR INDEXES 15 AND 16/	90536	254270-02	AR	A,D, G,I, J,L
-17		C	SLIDE, TELESCOPING	05236	7900790-00 350235B	4	
-18		C	SLIDE, TELESCOPING	05236	7900790-01 350235T	4	
		C	SPACER, SLEEVE /AP FOR INDEXES 17 AND 18/	90536	7019272-00	8	
		C	SCREW, PAN HD, 0.312-18UNC-2A BY 0.5 IN. LG /AP FOR INDEXES 17 AND 18/		4912530-00 COML	8	
		C	SCREW, FLAT HD, 0.312-24UNF-2A BY 0.875 IN. LG /AP FOR INDEXES 17 AND 18/		908542-05 COML	8	
		C	SCREW, PAN HD, 10-32UNF-2A BY 1.25 IN. LG /AP FOR INDEXES 17 AND 18/		4912527-07 COML	32	
		C	SCREW, FLAT HD, 0.25-28UNF-2A BY 0.875 IN. LG /AP FOR INDEXES 17 AND 18/		4912509-03 COML	24	
		C	WASHER, FLAT, NO. 10 /AP FOR INDEXES 17 AND 18/	96906	MS15795-808	32	
		C	WASHER, LOCK, NO. 10 /AP FOR INDEXES 17 AND 18/	96906	MS35338-138	32	
		C	SHIM, 3 IN. LG /AP FOR INDEXES 17 AND 18/	90536	254269-00	AR	
		C	SHIM, 3 IN. LG /AP FOR INDEXES 17 AND 18/	90536	254269-01	AR	
		C	SHIM, 3 IN. LG /AP FOR INDEXES 17 AND 18/	90536	254269-02	AR	
		C	SHIM, 3.5 IN. LG /AP FOR INDEXES 17 AND 18/	90536	254270-00	AR	

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
1		C	SHIM, 3.5 IN. LG /AP FOR INDEXES 17 AND 18/	90536	254270-01	AR	
		C	SHIM, 3.5 IN. LG /AP FOR INDEXES 17 AND 18/	90536	254270-02	AR	
-19		C	SCREW, SELF-LOCKING, PAN HD, 6-32UNC-2A BY 0.437 IN. LG	85312	905320-03 NKS35216-26	1	
-20	S1	C	SWITCH, PUSH, SPDT CONTACT, 125/250 V 10 AMP	91929	900139-00 2AC6	1	
		C	SCREW, FLAT HD, 6-32UNC-2A BY 0.312 IN. LG /AP/		4912504-00 COML	2	
-21		C	FILTER ASSEMBLY, RADIO INTERFERENCE /FOR BREAKDOWN SEE FIG 7/ 7-7	90536	7033257-00	1	
		C	SCREW, PAN HD, 10-32UNF-2A BY 0.75 IN. LG /AP/		4912527-04 COML	6	
		C	WASHER, FLAT, NO. 10 /AP/	96906	MS15795-808	6	
-22		C	ADAPTER, CABLE TO CONNECTOR	96906	MS3057-12B	1	
-23		C	GASKET, FLAT, SQUARE	82801	907211-07 04-0402-0020	1	
-24		C	CONNECTOR, PLUG, ELECTRICAL, FEMALE, 7 CONTACT	96906	MS3108B20-15S	1	
		C	SCREW, PAN HD, 4-40UNC-2A BY 0.625 IN. LG /AP/		4912523-08 COML	4	
		C	WASHER, FLAT, NO. 4 /AP/	96906	MS15795-803	4	
		C	NUT, SELF-LOCKING, 4-40UNC-3B /AP/	96906	MS21044C04	4	
-25	PS1	C	POWER SUPPLY /FOR BREAKDOWN SEE FIG 7-16/	90536	7038864-02	1	
-26		C	FILTER, AIR-CONDITIONING	79405	7902716-02 122-203-101	1	
-27		C	FILTER, AIR-CONDITIONING	00736	7902716-03 125800-001	1	A,D, G,I, J,L
-28	B1	C	FAN, CENTRIFUGAL, 470 CFM, 115 V, 400 HZ, 3 PHASE	82877	7901279-00 DRFP,PD3504, 277WS	1	
-29	B2	C	FAN, CENTRIFUGAL, 240 CFM, 115 V, 400 HZ, 3 PHASE	82877	7901311-00 DRFP,PS3504, 277WS	1	A,D, G,I,

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
1							J,L
-30	A12TB1	C	TERMINAL BOARD	81349	8TB6	1	
-31	A13TB1	C	TERMINAL BOARD	81349	8TB6	1	A,D G,I, J,L
-32		C	STABILIZER ASSEMBLY /FOR BREAK-DOWN SEE FIG 7-20/	90536	7050267-00	1	A,D, G,I,
		C	STABILIZER ASSEMBLY /FOR BREAK-DOWN SEE FIG 7-21/	90536	7050265-00	1	B,C, E,F
		C	STABILIZER ASSEMBLY/FOR BREAK-DOWN SEE FIG 7-22/	90536	7050264-00	1	H,K
-33		C	CABINET, ELECTRICAL EQUIPMENT	90536	7034821-01	1	A,D, G,I, J,L
-34		C	CABINET, ELECTRICAL EQUIPMENT	90536	7034820-01	1	B,C, E,F, H,K

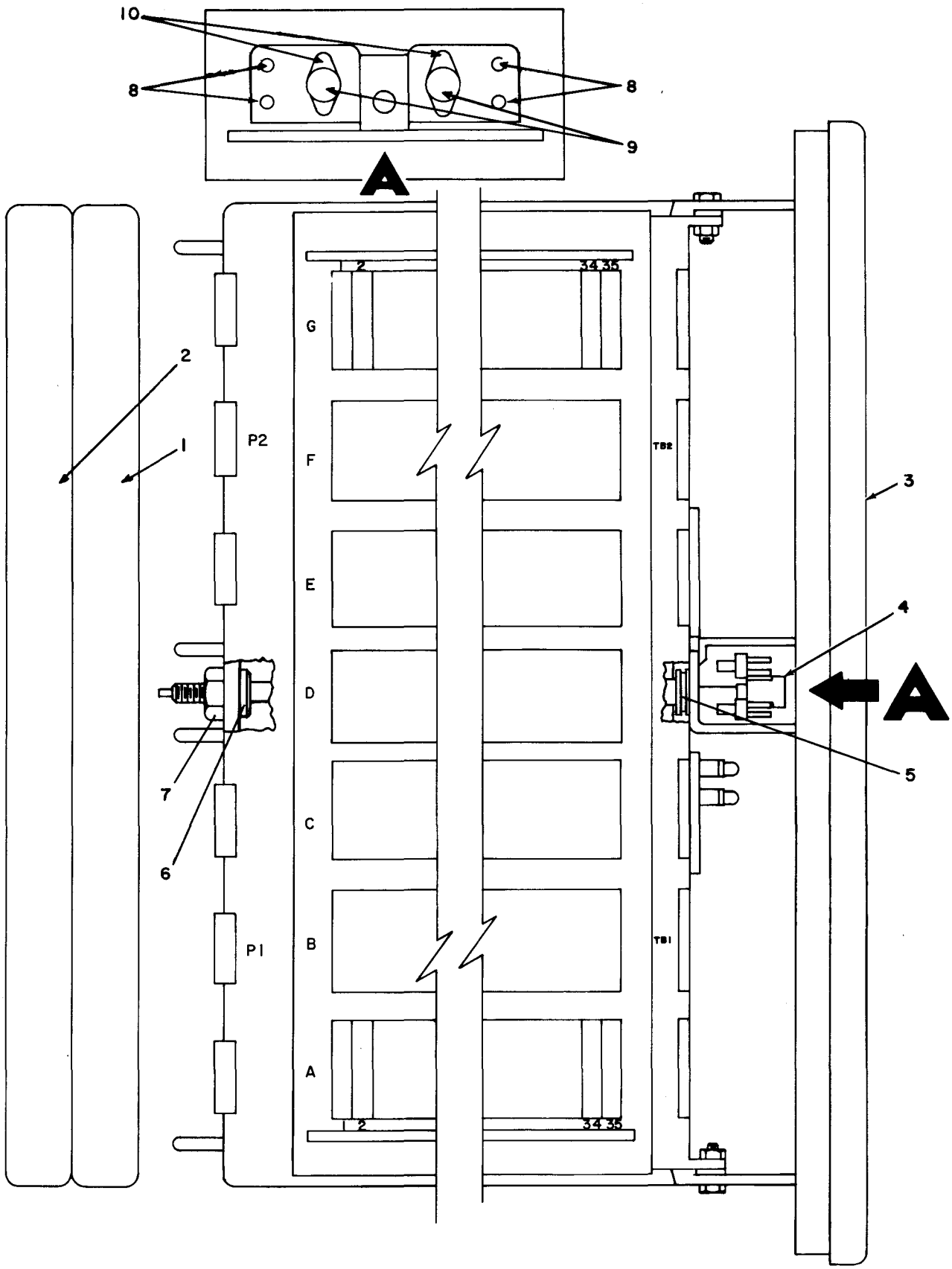
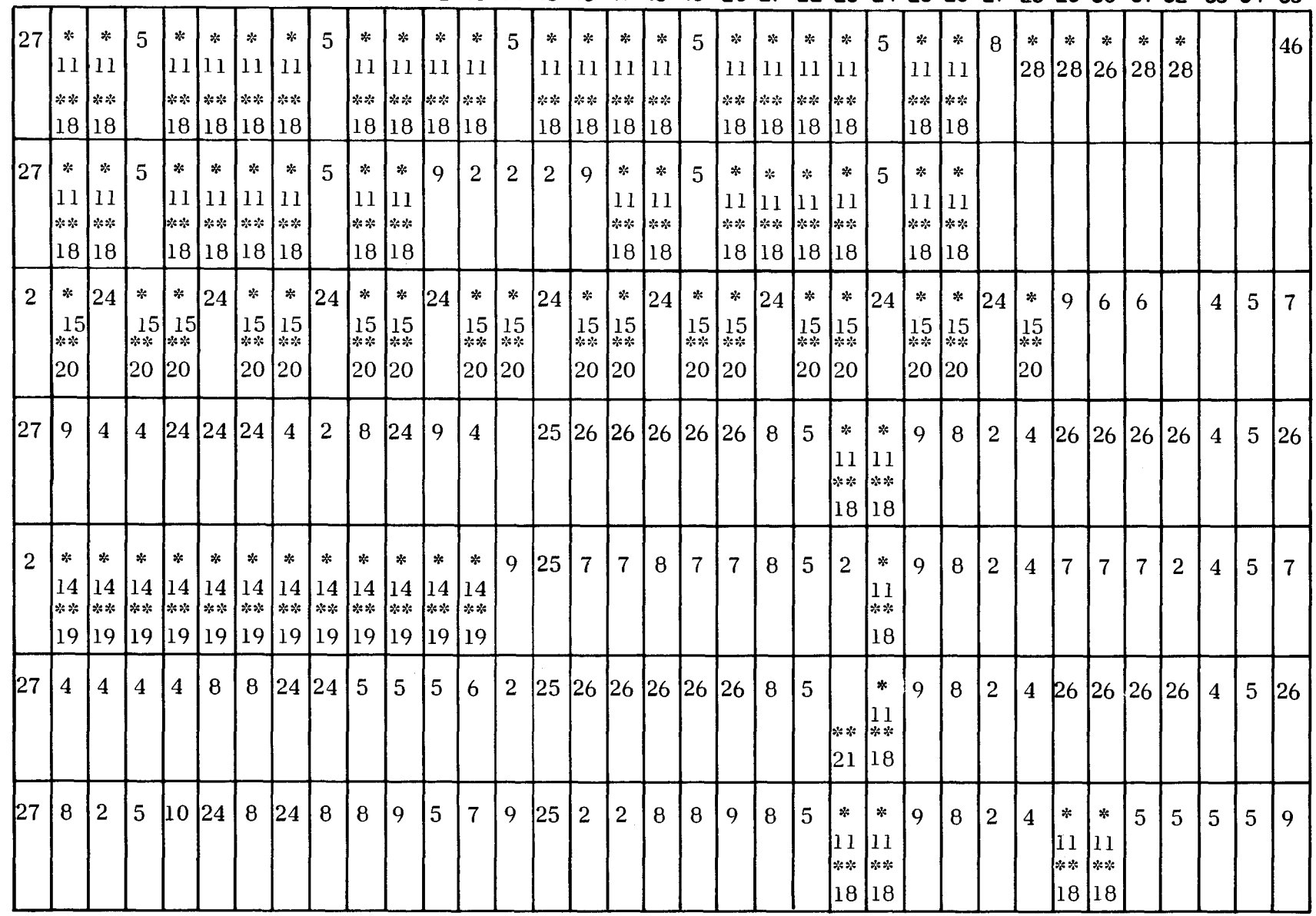


Figure 7-2. Digital to Digital Converter, A1,A2,A4,A8 - (Sheet 1 of 7)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
G	27	** 18 * 11	** 18 * 11	5	** 18 * 11	** 18 * 11	** 18 * 11	** 18 * 11	5	** 18 * 11	** 18 * 11	** 18 * 11	** 18 * 11	5	** 18 * 11	** 18 * 11	** 18 * 11	** 18 * 11	5	** 18 * 11	** 18 * 11	** 18 * 11	** 18 * 11	5	** 18 * 11	** 18 * 11	8	* 28	* 28	* 28	* 28	* 28			
F	27	** 18 * 11	** 18 * 11	5	** 18 * 11	** 18 * 11	** 18 * 11	** 18 * 11	5	** 18 * 11	** 18 * 11	9	2	2	2	9	** 18 * 11	** 18 * 11	5	** 18 * 11	** 18 * 11	** 18 * 11	** 18 * 11	5	** 18 * 11	** 18 * 11		6	6	6	9				45
E	2	** 20	24	** 20	** 20	24	** 20	** 20	24	** 20	** 20	24	** 20	** 20	24	** 20	** 20	24	** 20	** 20	24	** 20	** 20	24	** 20	** 20	24	** 20	9	6	6		4	5	7
D	27	9	4	4	24	24	24	4	2	8	24	9	4		25	26	26	26	26	26	8	5	** 18 * 11	** 18 * 11	9	8	2	4	26	26	26	26	4	5	26
C	2	** 19 * 14	** 19 * 14	** 19 * 14	** 19 * 14	** 19 * 14	** 19 * 14	** 19 * 14	** 19 * 14	** 19 * 14	** 19 * 14	** 19 * 14	** 19 * 14	9	25	7	7	8	7	7	8	5	2	** 18 * 11	9	8	2	4	7	7	7	2	4	5	7
B	27	4	4	4	4	8	8	24	24	5	5	5	6	2	25	26	26	26	26	26	8	5	** 21	** 18 * 11	9	8	2	4	26	26	26	26	4	5	26
A	27	8	2	5	10	24	8	24	8	8	9	5	7	9	25	2	2	8	8	9	8	5	** 18 * 11	** 18 * 11	9	8	2	4	** 18 * 11	** 18 * 11	5	5	5	5	9

** Fast Interface
* Slow Interface

Figure 7-2. Digital to Digital Converter, A1A1 - Module Location (Sheet 2 of 7)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
G	27	* 11 ** 18	* 11 ** 18	5	* 11 ** 18	* 11 ** 18	* 11 ** 18	* 11 ** 18	5	* 11 ** 18	* 11 ** 18	* 11 ** 18	* 11 ** 18	5	* 11 ** 18	* 11 ** 18	* 11 ** 18	* 11 ** 18	5	* 11 ** 18	* 11 ** 18	* 11 ** 18	* 11 ** 18	5	* 11 ** 18	* 11 ** 18	8	* 28	* 28	* 26	* 28	* 28			46
F	27	* 11 ** 18	* 11 ** 18	5	* 11 ** 18	* 11 ** 18	* 11 ** 18	* 11 ** 18	5	* 11 ** 18	* 11 ** 18	9	2	2	2	9	* 11 ** 18	* 11 ** 18	5	* 11 ** 18	* 11 ** 18	* 11 ** 18	* 11 ** 18	5	* 11 ** 18	* 11 ** 18									
E	2	* 15 ** 20	24	* 15 ** 20	* 15 ** 20	24	* 15 ** 20	* 15 ** 20	24	* 15 ** 20	* 15 ** 20	24	* 15 ** 20	* 15 ** 20	24	* 15 ** 20	* 15 ** 20	24	* 15 ** 20	* 15 ** 20	24	* 15 ** 20	* 15 ** 20	24	* 15 ** 20	* 15 ** 20	24	* 15 ** 20	9	6	6		4	5	7
D	27	9	4	4	24	24	24	4	2	8	24	9	4		25	26	26	26	26	26	8	5	* 11 ** 18	* 11 ** 18	9	8	2	4	26	26	26	26	4	5	26
C	2	* 14 ** 19	* 14 ** 19	* 14 ** 19	* 14 ** 19	* 14 ** 19	* 14 ** 19	* 14 ** 19	* 14 ** 19	* 14 ** 19	* 14 ** 19	* 14 ** 19	* 14 ** 19	9	25	7	7	8	7	7	8	5	2	* 11 ** 18	9	8	2	4	7	7	7	2	4	5	7
B	27	4	4	4	4	8	8	24	24	5	5	5	6	2	25	26	26	26	26	26	8	5	** 21	* 11 ** 18	9	8	2	4	26	26	26	26	4	5	26
A	27	8	2	5	10	24	8	24	8	8	9	5	7	9	25	2	2	8	8	9	8	5	* 11 ** 18	* 11 ** 18	9	8	2	4	* 11 ** 18	* 11 ** 18	5	5	5	5	9

* Slow Interface
** Fast Interface

Figure 7-2. Digital to Digital Converter, A1A2 - Module Location (sheet 3 of 7)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
G	27	7	6		8	6	25	5	9	7	6	7	25	9	8	9	8	8	8	9	8	2	9	24	2	6	7	8	6	9	29	26	26	26	26
F	27		5	25	6	8	25	9	4	7	7	7	8		2	5	5	8	8	8	8	9	2	24	2	7	9	24	5	5	4	8	8	8	9
E	27	8	5	8	6	8	25	25	4	8	25	24	2	26	26	8	5	9	8	9	8	2	2	24	2	8	8	24	9	24	4	2	2	2	2
D	27	7	25	9	8	25	25	8	6	2	4	24	9	26	26	9	8	9	2	2	8	2	8	24	2	8	2	24	2	24	7	2	4	4	32
C	27	8	9	8	25	9	25	10	8	4		9	4	26	26	7	8	8	8	8	8	2	8	9	2	8	8	24	2	24	4	9	7	33	32
B	27	8	25	25	10	8	8	8	4		7	4	4	26	26	8	8	7	7	9	8	10	8	8	2	2	9	24	7	24	8	25	25	11	32
A	27	25		6	6	8	25	7	25	7	8	9	8	9	2	8	9	8	16	10	16	2	5	2	2	2	8	7	4	4	11	11	1	7	13

Figure 7-2. Digital to Digital Converter, A2A1 - Module Location (Sheet 4 of 7)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
G	27 27	24	25	7	6	6	6	6	6	6	10	8	7	3	3	3	3	3	3	7	7	7	7	7	7	7	7	24	24	24	8	24	24	7	46
F	27	24	8	25	6	6	6	6	6	6	25	7	7	3	3	3	3	3	3	25	9	25	25	9	25	9	25	24	24	24	5	24	24	24	45
E	27	24	25	25	6	6	6	6	6	6	9	5	7	3	3	3	3	3	3	25	25	25	25	25	7	25	25	24	24	24	5	24	24	24	5
D	27	2	2	2	2	2	2	2	2	9	9	9	9	2	2	2	2	2	2	7	7	7	7	7	7	7	7	2	2	2	8	2	2	2	5
C	27	24	8	8	6	6	6	6	6	6	9	5	7	3	3	3	3	3	3	25	9	25	25	9	25	9	25	24	24	24	5	24	24	24	17
B	27	24	2	24	6	6	6	6	6	6	25	7	8	3	3	3	3	3	3	7	7	7	7	7	7	7	7	24	24	24	5	24	24	24	17
A	27	4	7	9	6	6	6	6	6	6	25	8	25	3	3	3	3	3	3	25	9	25	25	9	6	9	25	24	24	24	7	24	24	24	

Figure 7-2. Digital to Digital Converter, A2A2 - Module Location (Sheet 5 of 7)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
G	27	7	9	44		3	3	3	9	3	3	3	7	3	8	10	7	5	7	4	4	4	4	* 11 ** 18	26	7	7	24							46
F	27	8	8	8		3	3	3		3	3	3	7	3	8	8	5	5	8	4	4	26	8	4	17	4	7	24	9	8	4	4	4	37	45
E	27	16	8	8	4	3	3	3	2	3	3	3	7	3	8	9	8	25	9	26	4	4	8	26	4	4	8	8	9	8	9	7		23	
D	27	2	2	2		2	2	2	8	2	2	2	2	2	2	8	8	2	2	2	2	8	26	2	2	2	2	5	4		2	12	12	12	
C	27	5	9	4	4	3	3	3	2	3	3	3	7	3	2	9	24	5	8	3	3	8	9	4	4	24	24	16	8	4	4	4	6		
B	27	8	9		9	3	3	3		3	3	16	7	24	8	8	24	5	8	4	4	9	7	4	4	26	7	9	8	8	4	4	10		
A	27	16	4		3	3	3	3	7	3	3	24	7	24	8	8	24	6	5	3	4	8	8	4	4	11	11	11	11	11	4	4	11		

* Slow Interface

** Fast Interface

Figure 7-2. Digital to Digital Converter, A4A1 - Module Location (Sheet 6 of 7)

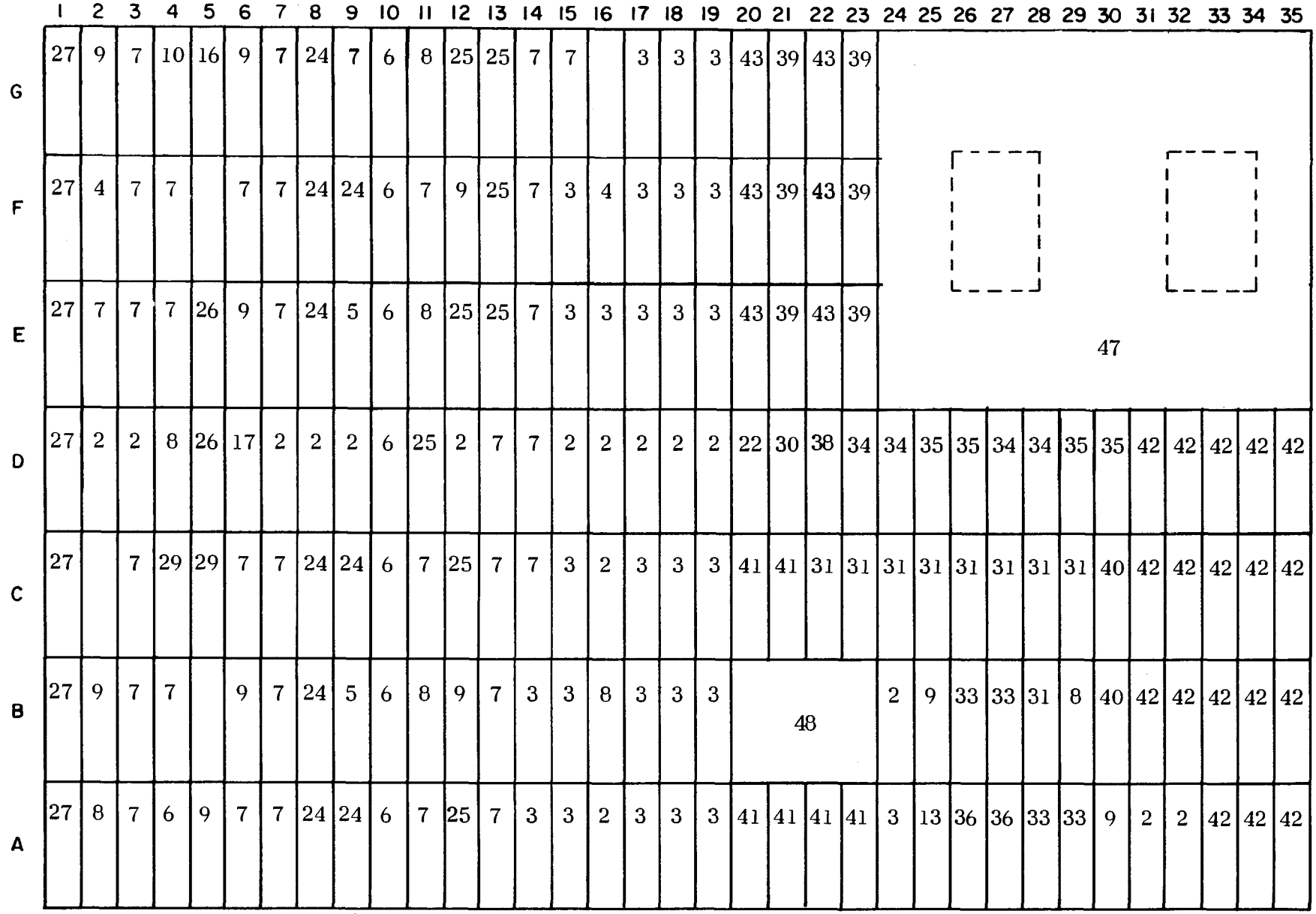


Figure 7-2. Digital to Digital Converter, A4A2 - Module Location (Sheet 7 of 7)

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
7- 2		C	CONVERTER, DIGITAL TO DIGITAL /FOR NHA SEE FIG 7-1/	90536	7053795-01	REF	A
	A1	C	CONVERTER, DIGITAL TO DIGITAL /FOR NHA SEE FIG 7-1/	90536	7053795-05	REF	B
	A2	C	CONVERTER, DIGITAL TO DIGITAL /FOR NHA SEE FIG 7-1/	90536	7053795-02	REF	C
	A4	C	CONVERTER, DIGITAL TO DIGITAL /FOR NHA SEE FIG 7-1/	90536	7053795-03	REF	D
	A8	C	CONVERTER, DIGITAL TO DIGITAL /FOR NHA SEE FIG 7-1/	90536	7053795-00	REF	E
	A8	C	CONVERTER, DIGITAL TO DIGITAL /FOR NHA SEE FIG 7-1/	90536	7053795-04	REF	F
-1	A1	D	CHASSIS ASSEMBLY, ELECTRICAL EQUIPMENT /FOR BREAKDOWN SEE FIG 7-8/	90536	7053794-00	1	A,E
	A1	D	CHASSIS ASSEMBLY, ELECTRICAL EQUIPMENT /FOR BREAKDOWN SEE FIG 7-8/	90536	7053794-02	1	C
	A1	D	CHASSIS ASSEMBLY, ELECTRICAL EQUIPMENT /FOR BREAKDOWN SEE FIG 7-8/	90536	7053794-04	1	D
	A1	D	CHASSIS ASSEMBLY, ELECTRICAL EQUIPMENT, BLANK	90536	7019292-01	1	B,F
-2	A2	D	CHASSIS ASSEMBLY, ELECTRICAL EQUIPMENT /FOR BREAKDOWN SEE FIG 7-8/	90536	7053794-01	1	A,B,
	A2	D	CHASSIS ASSEMBLY, ELECTRICAL EQUIPMENT /FOR BREAKDOWN SEE FIG 7-8/	90536	7053794-03	1	C
	A2	D	CONNECTOR ASSEMBLY, ELECTRICAL /FOR BREAKDOWN SEE FIG 7-9/	90536	7024793-02	1	D
-3	A3	D	DOOR-PANEL ASSEMBLY /FOR BREAK-DOWN SEE FIG 7-11/	90536	7053793-03	1	E,F
	A3	D	DOOR-PANEL ASSEMBLY /FOR BREAK-DOWN SEE FIG 7-11/	90536	7053793-02	1	A,B
	A3	D	DOOR-PANEL ASSEMBLY /FOR BREAK-DOWN SEE FIG 7-11/	90536	7053793-04	1	C
	A3	D	DOOR-PANEL ASSEMBLY /FOR BREAK-DOWN SEE FIG 7-12/	90536	7019284-26	1	D

FIG. & INDEX NO.	REF. DESIG.	INDEN	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
-4	MP1	D	LOCK ROD ASSEMBLY	90536	7007943-03	1	
-5		D	BEARING, SLEEVE, DOUBLE FLANGED, SPLIT, NYLON	96881	7900082-01 812FF	1	
-6		D	BEARING, BALL, THRUST, BANDED TYPE	43766	7902032-01 602SPECIAL	2	
-7		D	NUT, PLAIN, HEX	90536	7007865-00	1	
		D	SETSCREW, HEX SOCKET HD, 10-32 UNF-3A BY 0.375 IN. LG /AP/	96906	MS51023-51	1	
-8	CR1 CR2 CR4 CR5	D	SEMICONDUCTOR DEVICE, DIODE,	81349	1N1186	4	
-9	CR3 CR6	D	SEMICONDUCTOR DEVICE, DIODE,	81349	1N2804RB	2	
-10	XCR3 XCR6	D	SOCKET, SEMICONDUCTOR DEVICE	91506	7900149-00 8038-1G3	2	
-11		D	OSCILLATOR, PULSE DELAY	90536	7000210-00	3	B
		D	OSCILLATOR, PULSE DELAY	90536	7000210-00	1	C
-12		D	AMPLIFIER, DRIVER	90536	7002013-00	32	A,D,E
		D	AMPLIFIER, DRIVER	90536	7002013-00	52	C
		D	AMPLIFIER, DRIVER	90536	7002013-00	40	D
		D	AMPLIFIER, DRIVER	90536	7002013-00	16	B,F
-13		D	FLIP-FLOP, AND OR 2222-1	90536	7002000-00	36	B,C
		D	FLIP-FLOP, AND OR 2222-1	90536	7002000-00	68	D
-14		D	FLIP-FLOP, AND OR 33-3	90536	7002020-00	32	A,E
		D	FLIP-FLOP, AND OR 33-3	90536	7002020-00	16	B,C,F
		D	FLIP-FLOP, AND OR 33-3	90536	7002020-00	38	D
-15		D	INVERTER, AND OR 5-4	90536	7002030-00	52	A,E
		D	INVERTER, AND OR 5-4	90536	7002030-00	17	C
		D	INVERTER, AND OR 5-4	90536	7002030-00	9	D
		D	INVERTER, AND OR 5-4	90536	7002030-00	26	B,F
-16		D	INVERTER, AND OR 22222	90536	7002040-00	9	A,E

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
2		D	INVERTER, AND OR 22222	90536	7002040-00	47	C
		D	INVERTER, AND OR 22222	90536	7002040-00	10	D
		D	INVERTER, AND OR 22222	90536	7002040-00	3	B,F
-17		D	INVERTER, AND OR 22-23	90536	7002050-00	20	A,E
		D	INVERTER, AND OR 22-23	90536	7002050-00	55	C
		D	INVERTER, AND OR 22-23	90536	7002050-00	49	D
		D	INVERTER, AND OR 22-23	90536	7002050-00	10	B,F
-18		D	INVERTER, AND 3-3-2	90536	7002060-00	38	A,E
		D	INVERTER, AND 3-3-2	90536	7002060-00	66	C
		D	INVERTER, AND 3-3-2	90536	7002060-00	41	D
		D	INVERTER, AND 3-3-2	90536	7002060-00	19	B,F
-19		D	INVERTER, 1-1-1-1-1	90536	7002070-00	29	A,E
		D	INVERTER, 1-1-1-1-1	90536	7002070-00	43	C
		D	INVERTER, 1-1-1-1-1	90536	7002070-00	24	D
		D	INVERTER, 1-1-1-1-1	90536	7002070-00	14	B,F
-20		D	INVERTER, AND 3-6	90536	7002080-00	2	A,E
		D	INVERTER, AND 3-6	90536	7002080-00	5	C
		D	INVERTER, AND 3-6	90536	7002080-00	3	D
		D	INVERTER, AND 3-6	90536	7002080-00	1	B,F
-21		D	INVERTER, INPUT AMPLIFIER	90536	7002090-00	3	C
		D	INVERTER, INPUT AMPLIFIER	90536	7002090-00	6	D
		D	INVERTER, INPUT AMPLIFIER	90536	7002090-00 *	45	A,B
		D	INVERTER, INPUT AMPLIFIER	90536	7002090-00 *	44	A,E
-22		D	INVERTER, AND 1-8	90536	7002100-00	3	D
-23		D	AMPLIFIER, DRIVER	90536	7002120-00	1	C,D
-24		D	AMPLIFIER, DRIVER	90536	7002130-00 *	12	A,B,E
-25		D	AMPLIFIER, DRIVER	90536	7002141-00 *	18	A,B,E
-26		D	INVERTER, AND 1-8	90536	7002160-00	2	C

* SLOW INTERFACE

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
2		D	INVERTER, AND 1-8	90536	7002160-00	5	D
-27		D	INVERTER, OR L-4	90536	7002220-00	2	C,D
-28		D	AMPLIFIER, DIFFERENTIAL	90536	7002321-00 **	45	A,B
		D	AMPLIFIER, DIFFERENTIAL	90536	7002321-00	44	A,E
-29		D	AMPLIFIER, CONTROL LINE	90536	7002332-00 **	12	A,B,E
-30		D	AMPLIFIER, DATA LINE	90536	7002342-00 **	18	A,B,E
-31		D	SELECTOR, HIGH SPEED	90536	7002730-00 **	1	A,B,E
-32		D	REGULATOR, VOLTAGE	90536	7002861-00	1	D
-33		D	SENSOR, VOLTAGE /P15, M15/	90536	7002880-00	1	D
-34		D	FLIP-FLOP, 2/221C/	90536	7002900-00	34	A,E
		D	FLIP-FLOP, 2/221C/	90536	7002900-00	56	C
		D	FLIP-FLOP, 2/221C/	90536	7002900-00	19	D
		D	FLIP-FLOP, 2/221C/	90536	7002900-00	17	B,F
-35		D	INVERTER, AND OR 334	90536	7002920-00	8	A,E
		D	INVERTER, AND OR 334	90536	7002920-00	48	C
		D	INVERTER, AND OR 334	90536	7002920-00	9	D
		D	INVERTER, AND OR 334	90536	7002920-00	4	B,F
-36		D	FLIP-FLOP, 2/2C/21C/	90536	7002930-00	12	C
		D	FLIP-FLOP, 2/2C/21C/	90536	7002930-00	8	D
		D	FLIP-FLOP, 2/2C/21C/	90536	7002930-00	20	B,F
		D	FLIP-FLOP, 2/2C/21C/	90536	7002930-00 *	1	A,B,E
-37		D	CAPACITOR ASSEMBLY, NO. 3	90536	7003180-00	10	A,E
		D	CAPACITOR ASSEMBLY, NO. 3	90536	7003180-00	14	C,D
		D	CAPACITOR ASSEMBLY, NO. 3	90536	7003180-00	5	B,F
-38		D	TIME DELAY, 2 TO 15 USEC	90536	7003480-00 *	4	A,B,E
		D	TIME DELAY, 2 TO 15 USEC	90536	7003480-00	2	A,E

* SLOW INTERFACE

** FAST INTERFACE

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
2-39		D	AMPLIFIER, DRIVER	90536	7003490-00	1	C
		D	AMPLIFIER, DRIVER	90536	7003490-00	2	D
-40		D	AMPLIFIER, REGULATOR /-10 VOLT/	90536	7003600-00	1	D
-41		D	DRIVER, MEMORY /-17.5 VOLT/	90536	7003621-00	9	D
-42		D	NETWORK, PULSE DELAY	90536	7003630-00	3	C
-43		D	DRIVER, EMITTER FOLLOWER	90536	7003640-00	1	C
		D	DRIVER, EMITTER FOLLOWER	90536	7003640-00	4	D
-44		D	AMPLIFIER, DRIVER /115 VOLT SWITCH/	90536	7003670-00	4	D
-45		D	DRIVER, TRANSFORMER	90536	7003680-00	4	D
-46		D	NETWORK, PULSE DELAY /200 NSEC/	90536	7003710-00	2	D
-47		D	SENSOR, VOLTAGE /-14.5 VOLT/	90536	7003720-00	1	D
-48		D	AMPLIFIER, REGULATOR /P10 VOLT/	90536	7003730-00	1	D
-49		D	AMPLIFIER, SENSOR CONTROL	90536	7003740-00	6	D
-50		D	DIVERTER, CURRENT CONTROL	90536	7003760-00	2	D
-51		D	AMPLIFIER, DRIVER /POS & NEG/	90536	7003771-00	6	D
-52		D	AMPLIFIER DRIVER /DIGIT/	90536	7003780-00	18	D
-53		D	AMPLIFIER, SENSE /OUTPUT/	90536	7003850-00	6	D
-54		D	SELECTOR, JUMPER SWITCH	90536	7004010-00	1	D
-55		D	RESISTOR ASSEMBLY	90536	7009000-00	1	A,C, D,E
-56		D	CAPACITOR-RESISTOR ASSEMBLY	90536	7009010-00	1	A THRU F
-57		D	CONTROL MEMORY	90536	7024798-00	1	D
-58		D	BOOTSTRAP ASSEMBLY /DASH NUMBER INDICATES VARIABLE SELECTED BY CUSTOMER/	90536	7024774-XX	1	D

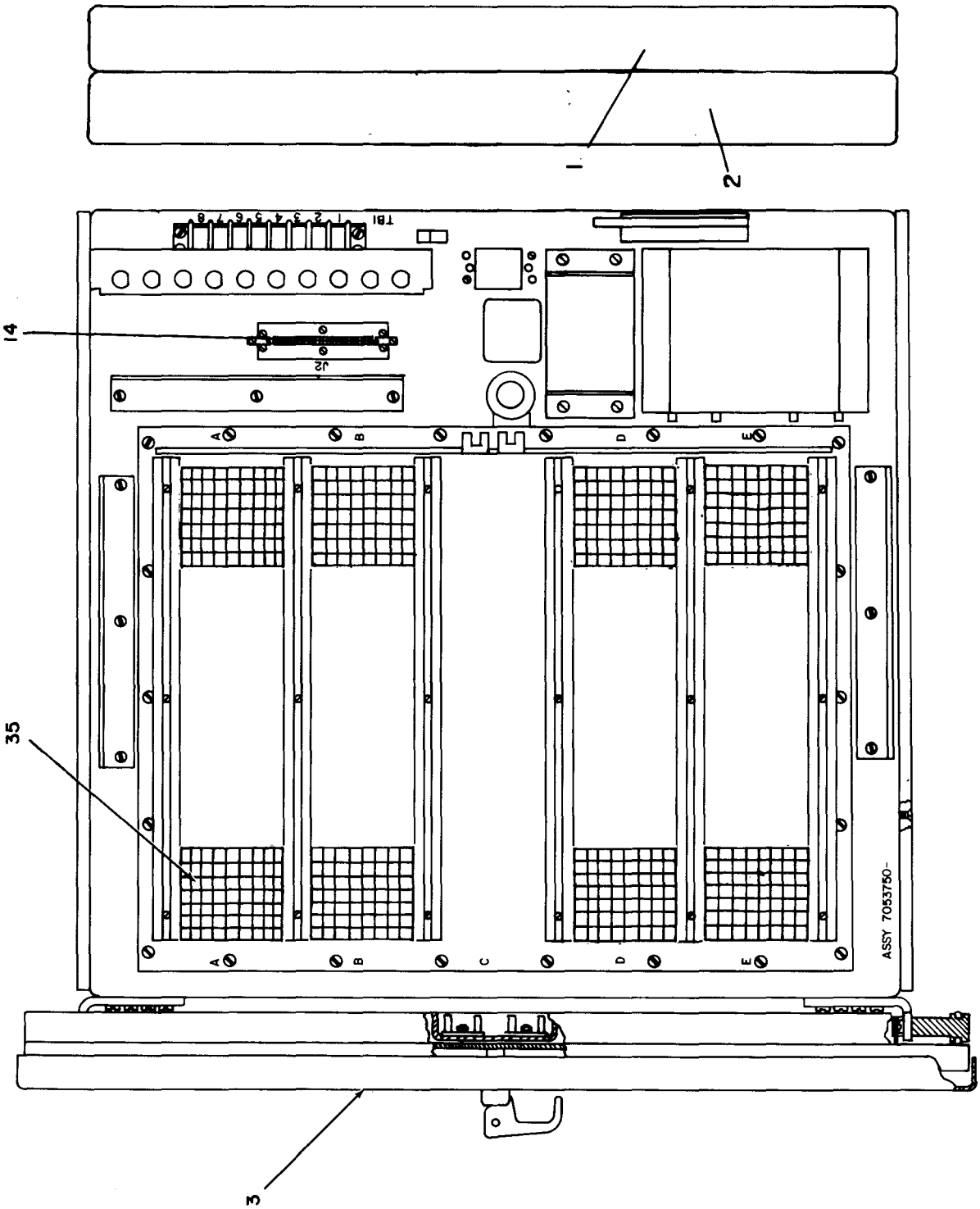


Figure 7-3. Memory Assembly (A3) (Sheet 1 of 3)

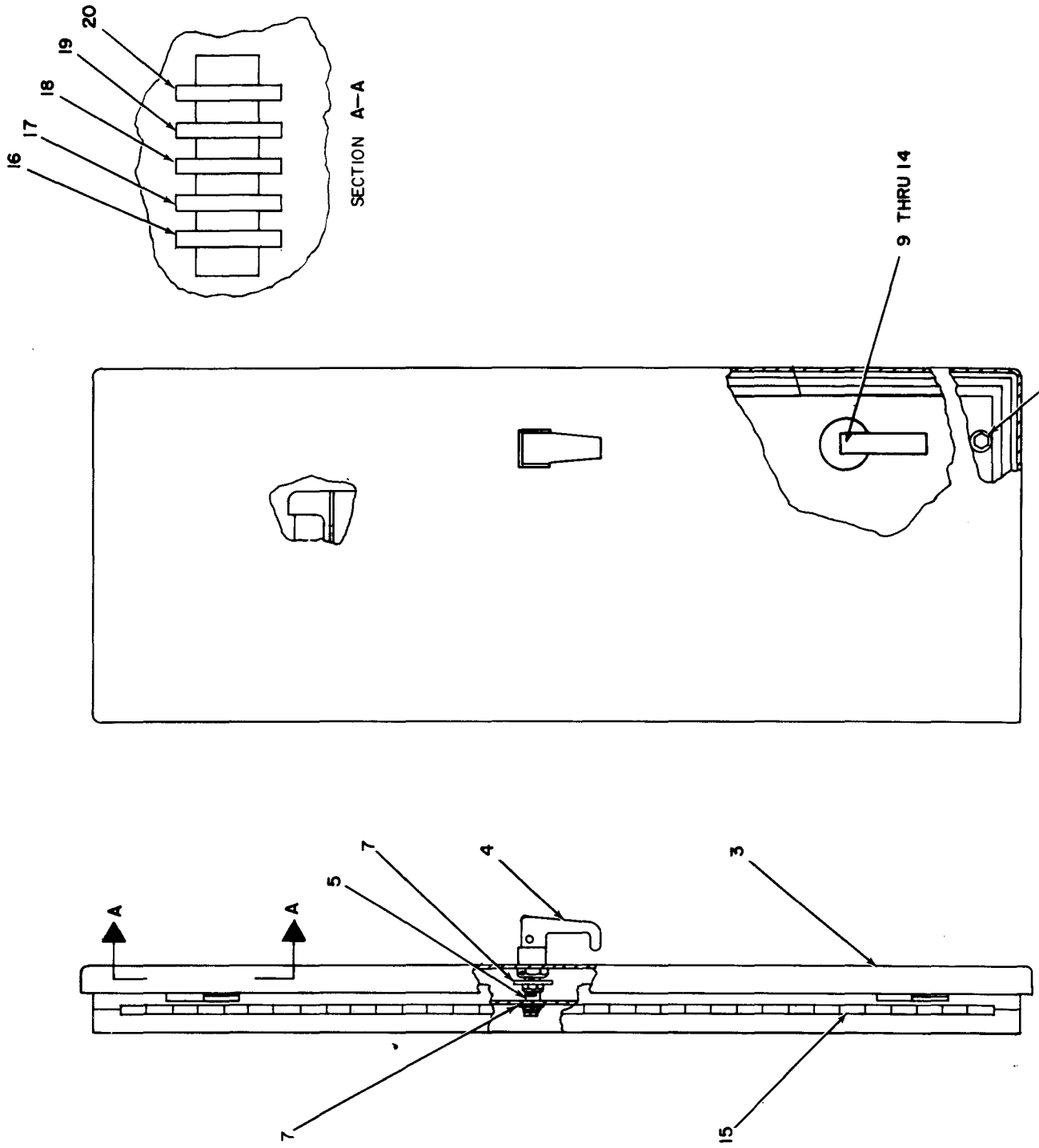


Figure 7-3. Memory Assembly (A3) (Sheet 2 of 3)

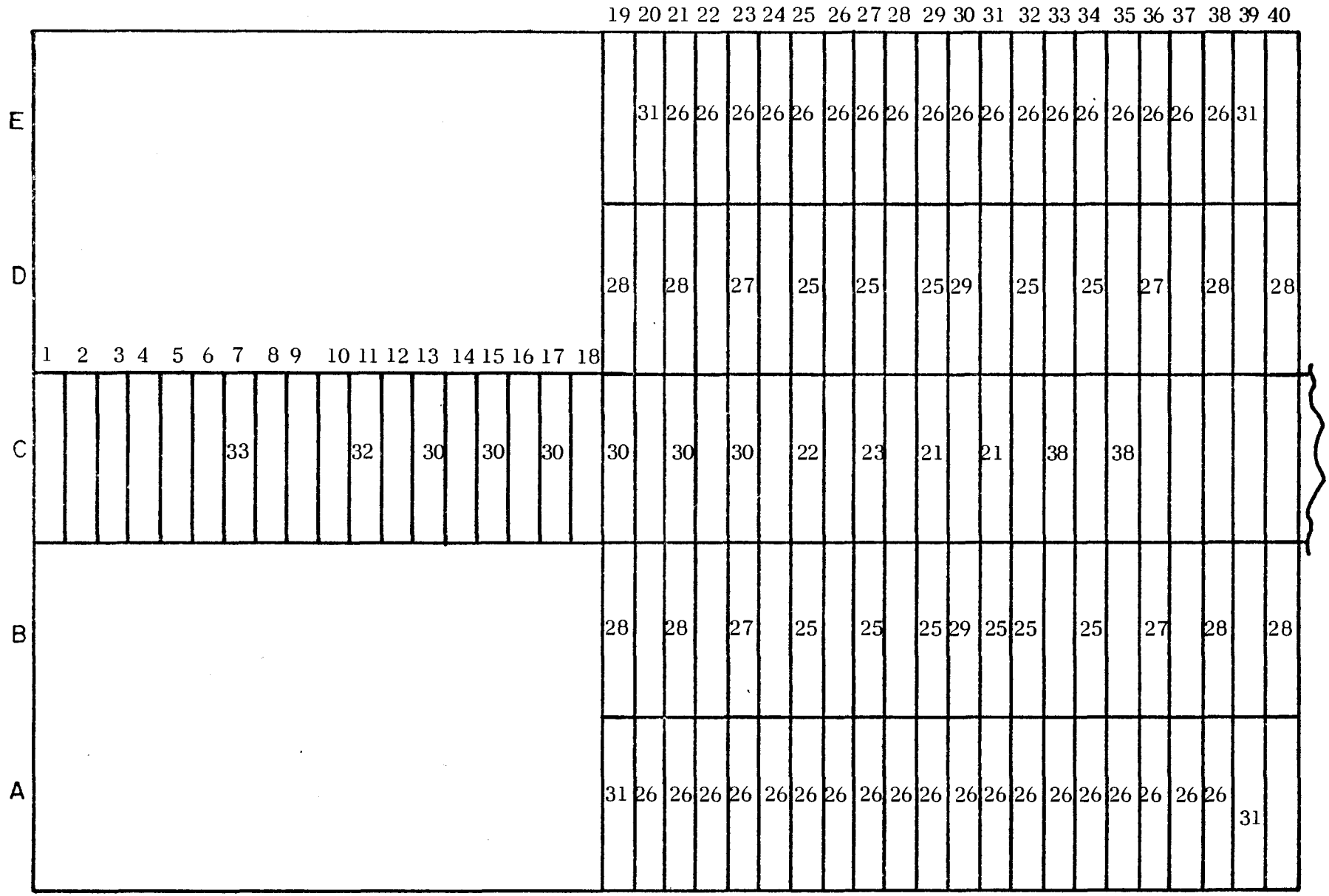


Figure 7-3. Memory Assembly (A3) (Sheet 3 of 3)

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
7- 3	A3	C	MEMORY ASSEMBLY /FOR NHA SEE FIG 7-1/	90536	7053750-00	REF	A
	A3	C	MEMORY ASSEMBLY /FOR NHA SEE FIG 7-1/	90536	7053750-03	REF	B
	A3	C	MEMORY ASSEMBLY /FOR NHA SEE FIG 7-1/	90536	7053750-01	REF	C
	A3	C	MEMORY ASSEMBLY /FOR NHA SEE FIG 7-1/	90536	7053750-02	REF	D
-1	A1	D	CHASSIS ASSEMBLY, ELECTRICAL EQUIPMENT /FOR BREAKDOWN SEE FIG 7-18/	90536	7085700-00	1	C
-2	A2	D	CHASSIS ASSEMBLY, ELECTRICAL EQUIPMENT /FOR BREAKDOWN SEE FIG 7-18/	90536	7053752-00	1	
-3		D	DOOR ASSEMBLY	90536	7085701-00	1	
-4		E	LATCH, RIM CLINCHING	90536	7008890-00	1	
-5		E	SPACER, SLEEVE	90536	7033086-00	1	
-6		E	STUD, TURNLOCK FASTENER	90536	7025359-00	2	
		E	RING, RETAINING, TURNLOCK FASTNER /AP/	08524	7900836-00 D1021A1	2	
		E	SPRING, HELICAL, COMPRESION /AP/	84830	7900906-01 LC042F7SS	2	
-7		E	PAWL, 1.68 IN. LG	90536	7019285-00	1	
-8		E	WASHER, SHOULDERED	90536	7050303-00	1	
-9		E	HANDLE	90536	7084898-00	4	
		E	PIN, SPRING 0.156 IN. DIA BY 0.5 IN. LG /AP/	96906	MS171556	4	
-10		E	RETAINER, SPRING	90536	7085705-00	4	
-11		E	SPRING, HELICAL, COMPRESSION	84830	7900906-01 LC042F7SS	4	
-12		E	PAWL, LATCH	90536	7085708-00	4	
		E	NUT, PLAIN, HEX, 0.312-24UNF-2B /AP/		907660-02 COML	4	
-13		E	SHAFT, LATCH	90536	7085706-00	4	
-14		E	BLOCK, MOUNTING, LATCH	90536	7085707-00	4	

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
3		E	SCREW, FLAT HD, 0.25-28UNF-2A BY 0.75 IN. LG /AP/		4912509-02 COML	8	
		E	WASHER, LOCK, 0.25 IN. ID /AP/	96906	MS35338-139	8	
		E	NUT, PLAIN, HEX, 0.25-28UNF-2B /AP/		907660-01 COML	8	
-15		E	HINGE, BUTT	90536	7019286-00	1	
-16	F1	E	FUSE	81349	F02A250V1/2AS	1	
-17	F2	E	FUSE	81349	F02A250V1AS	1	
-18	F3	E	FUSE	81349	F03A250V8AS	1	
-19	F4	E	FUSE	81349	F03A250V15AS	1	
-20	F5	E	FUSE	81349	F03A125V20AS	1	
-21		D	AMPLIFIER, DRIVER	90536	7500040-00	3	A
		D	AMPLIFIER, DRIVER	90536	7500040-00	2	B,D
		D	AMPLIFIER, DRIVER	90536	7500040-00	6	C
-22		D	OSCILLATOR, CLOCK	90536	7500260-00	1	A,B, D
		D	OSCILLATOR, CLOCK	90536	7500260-00	2	C
-23		D	AMPLIFIER, DRIVER	90536	7500280-00	1	A,B, D
		D	AMPLIFIER, DRIVER	90536	7500280-00	2	C
-24		D	REGULATOR, VOLTAGE	90536	7500320-00	1	A,B, D
		D	REGULATOR, VOLTAGE	90536	7500320-00	2	C
-25		D	SWITCH, MEMORY	90536	7500400-00	11	A
		D	SWITCH, MEMORY	90536	7500400-00	6	B,D
		D	SWITCH, MEMORY	90536	7500400-00	22	C
-26		D	AMPLIFIER, SENSE	90536	7500650-00	36	A
		D	AMPLIFIER, SENSE	90536	7500650-00	18	B,D
		D	AMPLIFIER, SENSE	90536	7500650-00	72	C
-27		D	DIVERTER, DRIVER	90536	7500421-00	4	A
		D	DIVERTER, DRIVER	90536	7500421-00	2	B,D

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
3		D	DIVERTER, DRIVER	90536	7500421-00	8	C
-28		D	TRANSFORMER ASSEMBLY	90536	7500431-00	8	A
		D	TRANSFORMER ASSEMBLY	90536	7500431-00	4	B
		D	TRANSFORMER ASSEMBLY	90536	7500431-00	16	C
		D	TRANSFORMER ASSEMBLY	90536	7500431-00	2	D
-29		D	REGULATOR, VOLTAGE	90536	7500781-00	2	A
		D	REGULATOR, VOLTAGE	90536	7500781-00	1	B,D
		D	REGULATOR, VOLTAGE	90536	7500781-00	4	C
-30		D	AMPLIFIER, LEVEL CHANGE	90536	7500761-00	6	A,B,D
		D	AMPLIFIER, LEVEL CHANGE	90536	7500761-00	12	C
-31		D	CAPACITOR-DIODE ASSEMBLY	90536	7500660-00	4	A
		D	CAPACITOR-DIODE ASSEMBLY	90536	7500660-00	2	B,D
		D	CAPACITOR-DIODE ASSEMBLY	90536	7500660-00	8	C
-32		D	SENSE, VOLTAGE	90536	7500340-00	1	A,B,D
		D	SENSE, VOLTAGE	90536	7500340-00	2	C
-33		D	CAPACITOR ASSEMBLY	90536	7500671-00	1	A,B,D
		D	CAPACITOR ASSEMBLY	90536	7500671-00	2	C
-34		D	AMPLIFIER, DRIVER	90536	7500900-00	2	A,B,D
		D	AMPLIFIER, DRIVER	90536	7500900-00	4	C
-35		C	MEMORY STACK ASSEMBLY	90536	7067439-05	8	A
		C	MEMORY STACK ASSEMBLY	90536	7067439-05	2	B
		C	MEMORY STACK ASSEMBLY	90536	7067439-05	16	C
		C	MEMORY STACK ASSEMBLY	90536	7067439-05	4	D

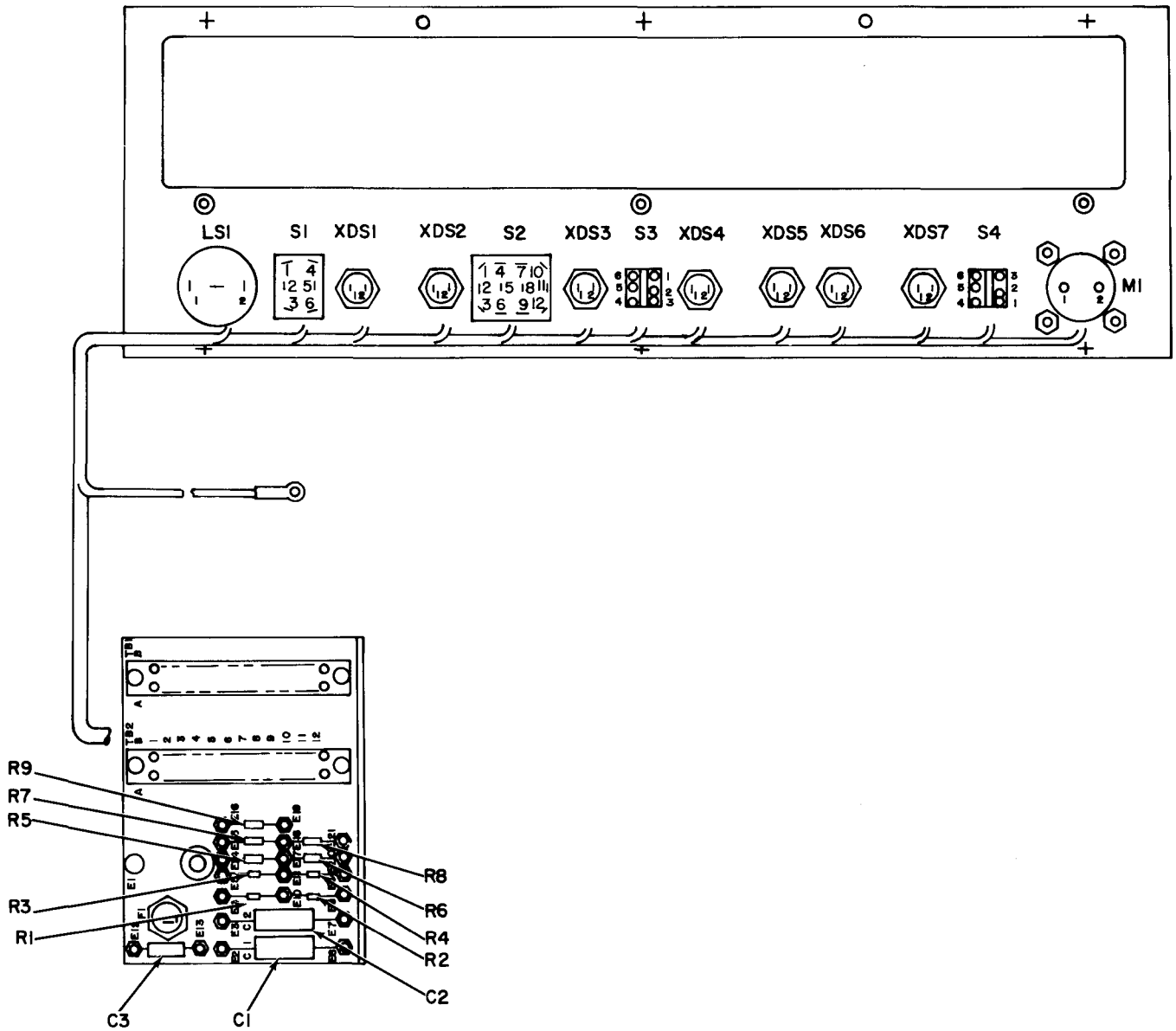


Figure 7-4. Hood Assembly (A5)

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
7- 4	A5	C	HOOD ASSEMBLY /FOR NHA SEE FIG 7-1/	90536	7050307-01	REF	
	C1 C2	D	CAPACITOR	81349	CP09A1KC104K3	2	
	C3	D	CAPACITOR, FIXED, ELECTROLYTIC, 6 VDC, 150 UF, PORM 20 %, M80 DEG C /M112 DEG F/ TO 85 DEG C /185 DEG F/ OPERATING TEMP RANGE	56289	908404-16 150D157X0006R2	1	
	DS1 THRU DS7	D	LAMP, INCANDESCENT, 0.15 AMP, 18 VDC, SINGLE CONTACT	71744	7900677-00 1826	7	
	F1	D	FUSE	81349	F03A250V12AS	1	
	LS1	D	HORN, ELECTRICAL, SOLID STATE, OSCILLATOR, FREQ 2.5 KC, 6 TO 28 VDC, 65 TO 86 DB AT 2 FT	37942	7900874-00 SC628S	1	
	M1	D	METER	96906	MS17325-1	1	
	R1 THRU R4	D	RESISTOR	81349	RC07GF471J	5	
	R5 THRU R9	D	RESISTOR	81349	RC20GF150J	1	
	S1	D	SWITCH	96906	MS35059-21	1	
	S2	D	SWITCH	96906	MS25068-23	1	
	S3	D	SWITCH, TOGGLE, 2 SPDT CONTACT, 2 POLE, 3 POSITION, 5 AMP AT 250 VAC	91929	7900635-01 13AT418T2	1	
	S4	D	SWITCH, TOGGLE, 2 SPDT CONTACT, 2 POLE, 3 POSITION, 5 AMP AT 250 VAC	91929	7900635-02 13AT416T2	1	
	TB1 TB2	D	TERMINAL BOARD	81349	26TB12	2	
	XDS1 XDS2	D	LIGHT, INDICATOR, THD LENS HOLDER, CONVEXED, YELLOW LENS	72619	7900678-02 85-0410-0113-203	2	
	XDS3 XDS4	D	LIGHT, INDICATOR, THD LENS HOLDER, CONVEXED, RED LENS	72619	7900678-00 85-0410-0111-203	2	
	XDS5 XDS7	D	LIGHT, INDICATOR, THD MTD LENS HOLDER, CONVEXED, GREEN LENS	72619	7900678-01 85-0410-0112-203	2	
	XDS6	D	LIGHT, INDICATOR, THD MTD LENS HOLDER, CONVEXED, BLUE LENS	72619	7900678-03 85-0410-0114-203	1	
	XF1	D	FUSEHOLDER	81349	FHN26G2	1	

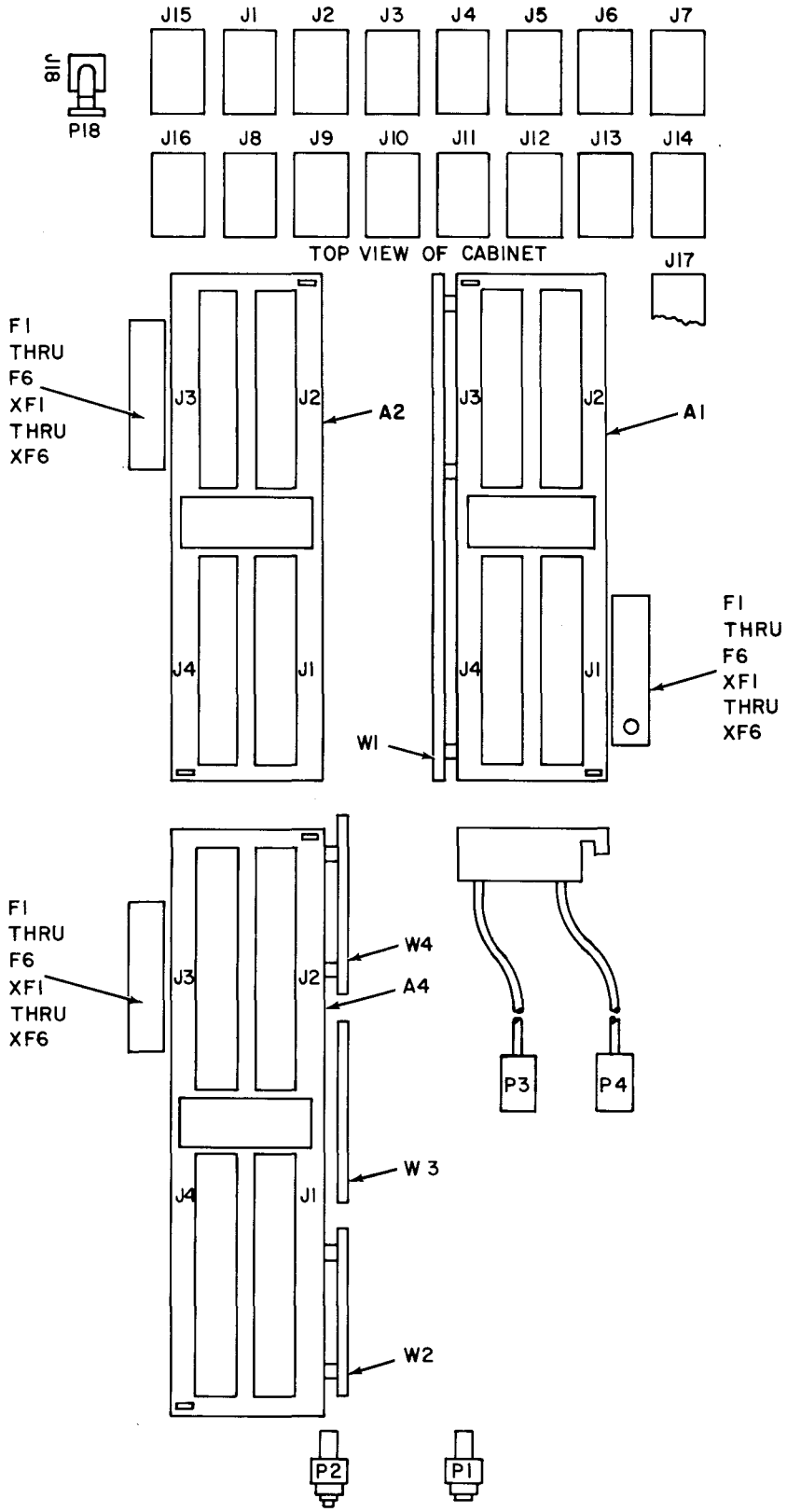


Figure 7-5. Connector Assembly (A12)

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
7- 5	A12	C	CONNECTOR ASSEMBLY, ELECTRICAL /FOR NHA SEE FIG 7-1/	90536	7053799-00	REF	
	A1	D	CONNECTOR SUBASSEMBLY, ELECTRICAL	90536	7019245-02	1	
	A1F1 A1F4	C	FUSE	81349	F02A250V5AS	2	
	A1F2 A1F5	C	FUSE	81349	F02A250V12AS	2	
	A1F3 A1F6	C	FUSE	81349	F02A250V4AS	2	
	A1J1 THRU A1J4	D	CONNECTOR, RECEPTACLE, ELECTRICAL, MALE, 189 CONTACTS	91886	7900842-00 3614875	4	
	A1XF1 THRU A1XF6	C	FUSEHOLDER	81349	FNH26G2	6	
	A2	D	CONNECTOR SUBASSEMBLY, ELECTRICAL	90536	7019245-02	1	
	A2F1	C	FUSE	81349	F03A250V8AS	1	
	A2F2	C	FUSE	81349	F03A250V10AS	1	
	A2F3	C	FUSE	81349	F02A250V5AS	1	
	A2F4	C	FUSE	81349	F02A250V6AS	1	
	A2F5	C	FUSE	81349	F03A250V12AS	1	
	A2F6	C	FUSE	81349	F02A250V4AS	1	
	A2J1 THRU A2J4	D	CONNECTOR, RECEPTACLE, ELECTRICAL, MALE, 189 CONTACTS, WIRE WRAP	91886	7900842-00 3614875	4	
	A2XF1 THRU A2XF6	C	FUSEHOLDER	81349	FNH26G2	6	
	A4	D	CONNECTOR SUBASSEMBLY, ELECTRICAL	90536	7050279-00	1	

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
5	A4F1 A4F4	C	FUSE	81349	F02A250V6AS	2	
	A4F2	C	FUSE	81349	F03A250V12AS	1	
	A4F5	C	FUSE	81349	F03A250V8AS	1	
	A4F6	C	FUSE	81349	F02A250V5AS	1	
	A4J1 THRU A4J4	E	CONNECTOR, RECEPTACLE, ELEC-TRICAL, MALE, 189 CONTACTS, WIRE WRAP	91885	7900842-00 3614875	4	
	A4W1 THRU A4W4	D	BUS BAR, GROUND	90536	7050281-00	4	
	A4XF1 THRU A4XF6	C	FUSEHOLDER	81349	FHN26G	6	
	J1 THRU J17	C	CONNECTOR, RECEPTACLE, ELEC-TRICAL, MALE, 90 CONTACT	71468	906489-00 DPD4500-1388	17	
	J18	C	CONNECTOR	96906	MS3108B10SL3S	1	
	P1	C	CONNECTOR	96906	MS3106A32-6S	1	
	P2	C	CONNECTOR	96906	MS3106A32-6SW	1	
	P3 P4	C	CONNECTOR, PLUG, ELECTRICAL /FOR BREAKDOWN SEE FIG 7-22/	90536	7078161-00	2	
	P18	C	CONNECTOR	96906	MS3102A10SL3P	1	
	W1	C	BUS BAR, GROUND	90536	7033264-00	1	
	W2 W3 W4	C	BUS BAR, POWER	90536	7033263-00	3	

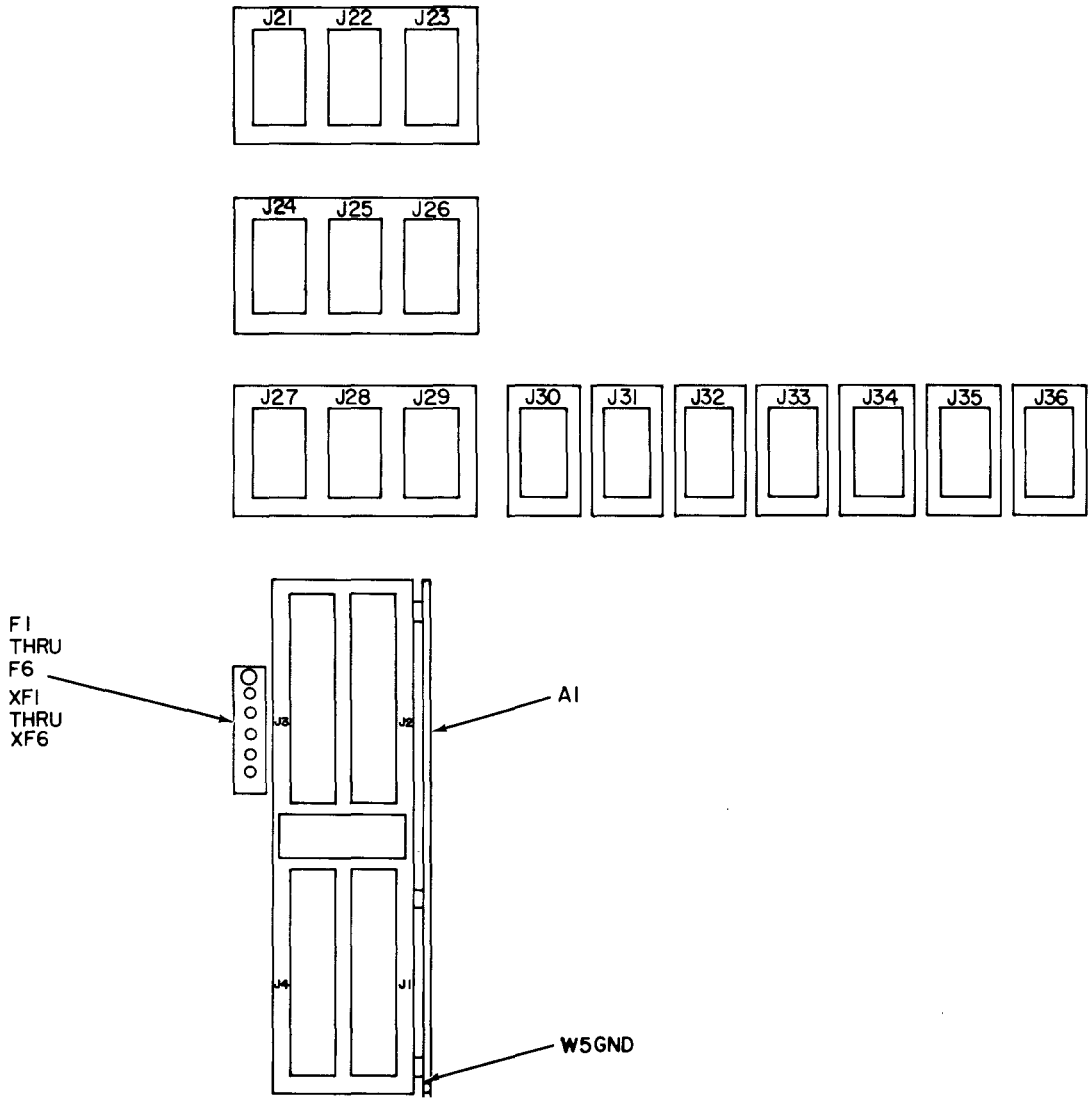


Figure 7-6. Connector Assembly (A13)

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
7- 6	A13	C	CONNECTOR ASSEMBLY /FOR NHA SEE FIG 7-1//	90536	7025669-06	1	
	A1	D	CONNECTOR SUBASSEMBLY, ELECTRICAL	90536	7019245-02	1	
	A1F1 A1F4	C	FUSE	81349	F02A250V5AS	2	
	A1F2 A1F5	C	FUSE	81349	F02A250V12AS	2	
	A1F3 A1F6	C	FUSE	81349	F02A250V4AS	2	
	A1J1 THRU A1J4	D	CONNECTOR, RECEPTACLE, ELECTRICAL, MALE, 189 CONTACTS	91886	7900842-00 3614875	4	
	A1XF1 THRU A1XF6	C	FUSEHOLDER	81349	FNH26G2	6	
	J21 THRU J36	D	CONNECTOR, RECEPTACLE, ELECTRICAL, MALE, 90 CONTACTS	71468	906689-00 DPD4500-1388	16	
	W5	D	BUS BAR	90536	7033264-00	1	

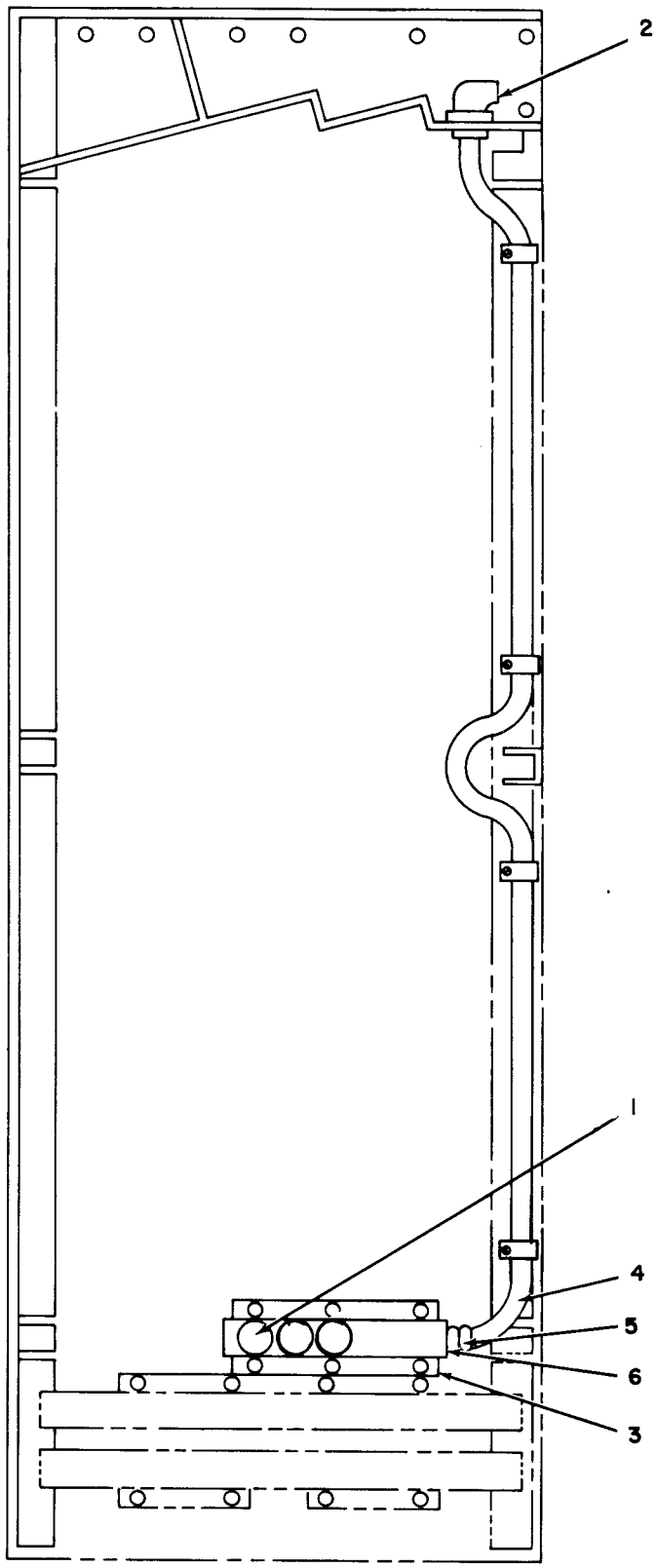


Figure 7-7. Filter Assembly, Radio Interference (A14)

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
7- 7		C	FILTER ASSEMBLE, RADIO INTER-FERENCE /FOR NHA SEE FIG 7-1/	90536	7033257-00	1	
-1	FL1 FL2 FL3	D	FILTER RADIO FREQUENCY, 400 VDC 20 AMP	56289	7900608-00 20JX31	3	
-2	P1	D	CONNECTOR	96906	MS3100A20-15P	1	
-3		D	BOX, ELECTRICAL FILTER	90536	7033255-00	1	
-4		D	CONDUIT ASSEMBLY, METAL, FLEXIBLE	01021	7900912-13 C175-0500-5800-A299	1	
-5		D	DUMMY CONNECTOR SHELL, ROUND	71468	908173-08 2182-5	1	
-6		D	GASKET, FLAT, SQUARE, ALUMINUM AND NEOPREME 0.020 IN. THK	82805	907211-05 40-016	1	
		D	NUT, SELF-LOCKING, HEX 4-40UNC-3B	96906	MS21044C04	4	
		D	SCREW, PAN HD, 4-40UNC-2A 0.438 IN. LG /AP FOR INDEXES 3 AND 4/		4912523-05 COML	4	
		D	WASHER, FLAT, NO. 4 /AP FOR INDEXES 3 AND 4/	96906	MS15795-803	4	

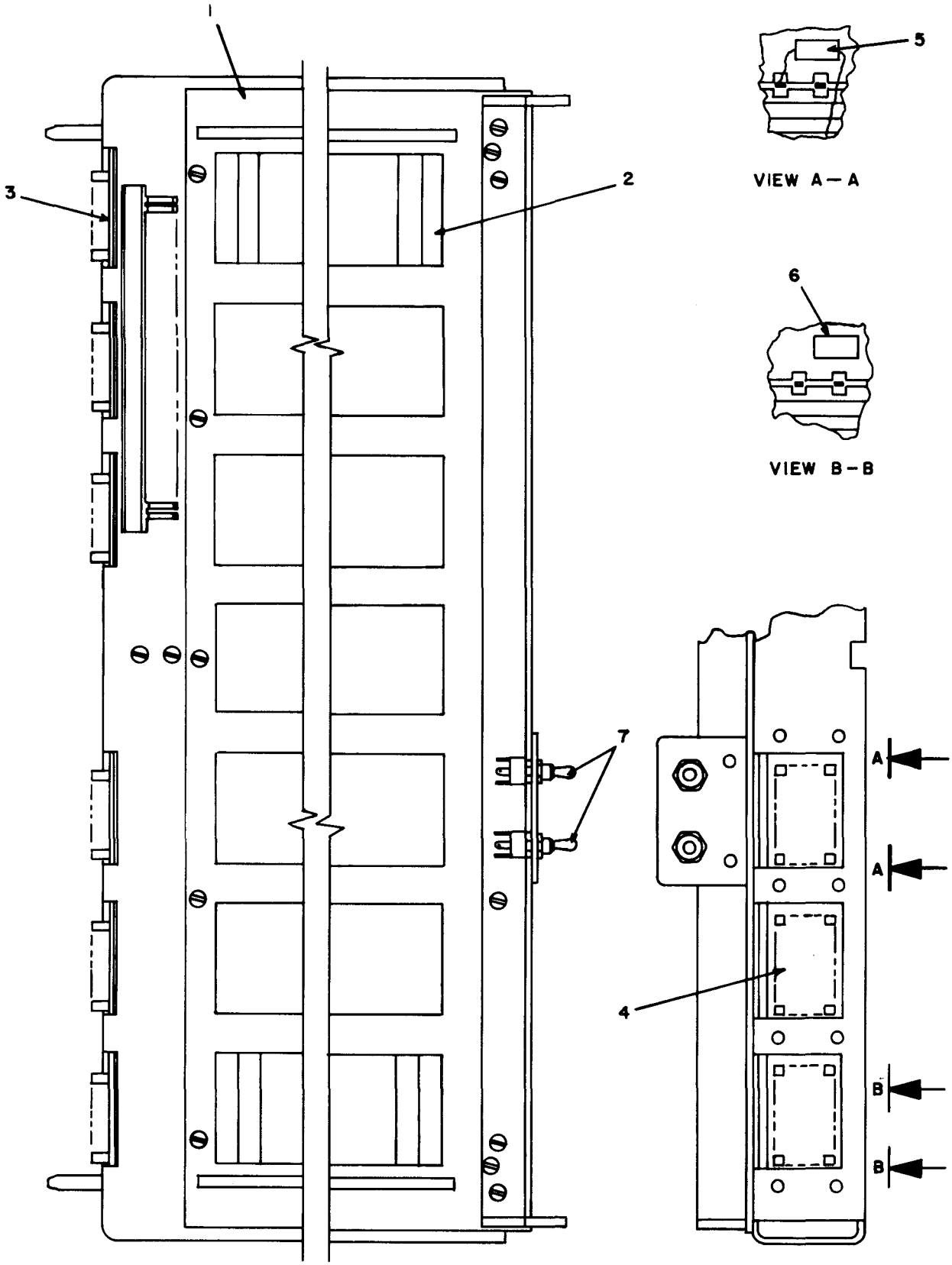


Figure 7-8. Chassis Assembly Electrical

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
7- 8	A1	D	CHASSIS ASSEMBLY, ELECTRICAL /FOR NHA SEE FIG 7-2/	90536	7053794-00	REF	A
	A1	D	CHASSIS ASSEMBLY, ELECTRICAL /FOR NHA SEE FIG 7-2/	90536	7053794-02	REF	B
	A1	D	CHASSIS ASSEMBLY, ELECTRICAL /FOR NHA SEE FIG 7-2/	90536	7053794-04	REF	C
	A2	D	CHASSIS ASSEMBLY, ELECTRICAL /FOR NHA SEE FIG 7-2/	90536	7053794-01	REF	D
	A2	D	CHASSIS ASSEMBLY, ELECTRICAL	90536	7053794-03	REF	E
-1		E	CONNECTOR ASSEMBLY, ELECTRICAL	90536	7019232-00	1	
-2	J1A THRU J35A, J1B THRU J35B, J1C THRU J35C, J1D THRU J35D, J1E THRU J35E, J1F THRU J35F, J1G THRU J35G	F	CONNECTOR, RECEPTACLE, ELECTRICAL, FEMALE, 15 CONTACT	16512	7900251-01 A2345-10	245	
-3	P1, P2	F	CONNECTOR, RECEPTACLE, ELECTRICAL, 189 CONTACT		7900843-00	2	
-4	TB1, TB2	F	TEST POINT ASSEMBLY, 231 CONTACT		7900841-00	2	
-5	C1 THRU C21	E	CAPACITOR, FIXED, CERAMIC DIELECTRIC, 0.47UF, P80 , M20 , 25 V	56289	7900092-04 5C11A9		
-6	R1 THRU R4	E	RESISTOR	81349	RC07GF221J	4	D
-7	S1, S2	E	SWITCH, TOGGLE, DPDT	15605	7900241-01 8869K4	2	B
-8		E	CHASSIS FRAME, ELECTRICAL EQUIPMENT	90536	7019230-00	1	D,E
		E	CHASSIS FRAME, ELECTRICAL EQUIPMENT	90536	7019230-01	1	A,B, C

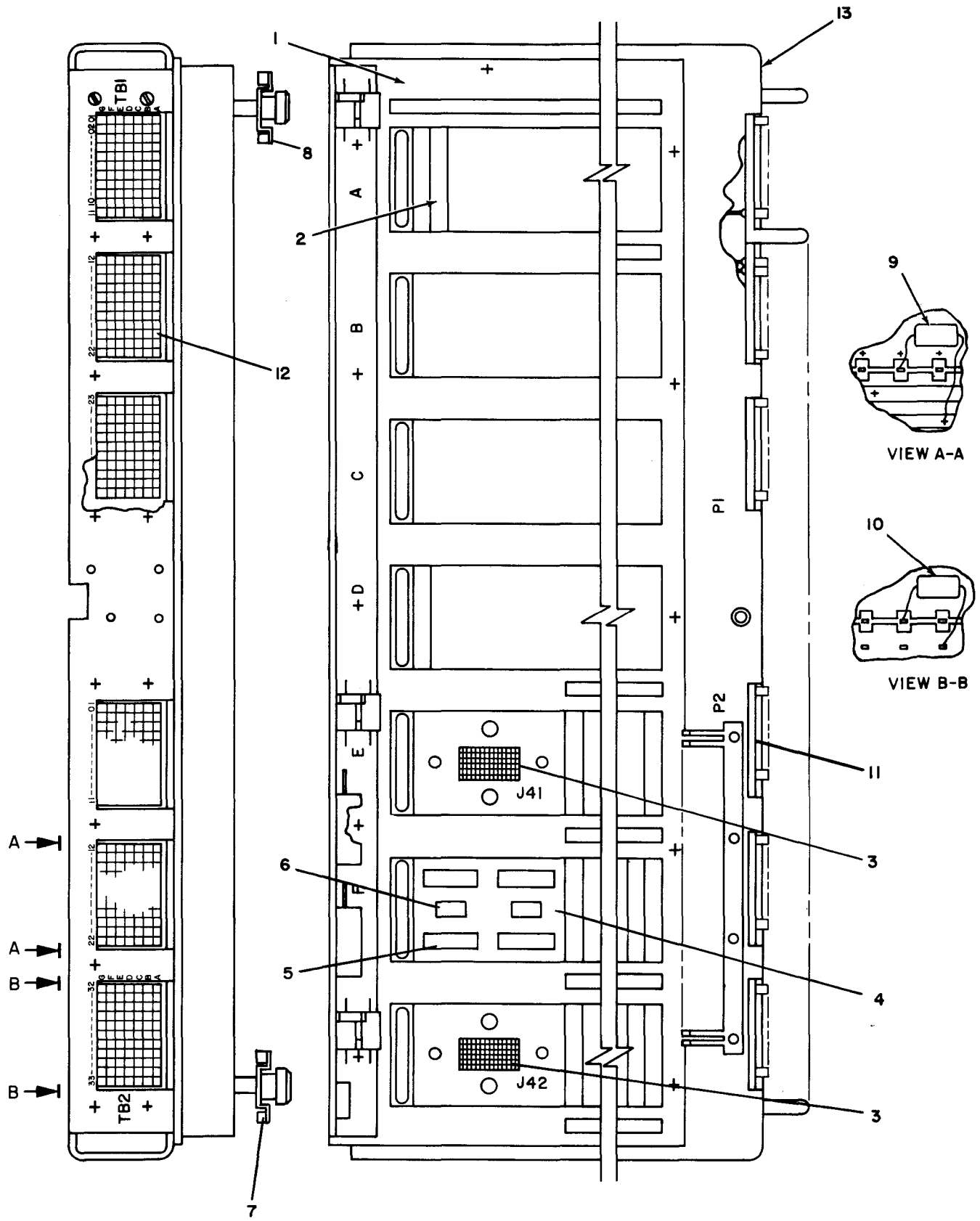


Figure 7-9. Connector Assembly (A4A2)

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
7- 9	A2	D	CONNECTOR ASSEMBLY /FOR NHA SEE FIG 7-2/	90536	7024793-02	REF	
-1	A1	E	CONNECTOR ASSEMBLY, ELECTRICAL	90536	7024790-00	1	
-2	A1J1A THRU A1J35A A1J1B THRU A1J35B A1J1C THRU A1J35C A1J1D THRU A1J35D A1J1E THRU A1J23E A1J1F THRU A1J23F A1J1G THRU A1J23G	F	CONNECTOR, RECEPTACLE, ELECTRICAL, FEMALE, 15 CONTACTS, WIRE WRAP, BLACK BODY	16512	7900251-01 A2345-11	209	
-3	A1J41 A1J42	F	CONNECTOR ASSEMBLY, ELECTRICAL	90536	7024786-00	2	
-4	A1A3	F	CAPACITOR-RESISTOR	90536	7024791-00	1	
-5	A3C1 THRU A3C4	F	CAPACITOR	81349	CL25BG251UP3	4	
-6	A3R1 A3R2	F	RESISTOR	81349	RE65N43R2	2	
-7		E	RETAINER, ELEXTRONIC CIRCUIT PLUG-IN UNIT	90536	7019281-00	4	
-8		E	RETAINER, ELECTRONIC CIRCUIT PLUG-IN UNIT	90536	7019281-03	4	
		E	THUMBSCREW /AP FOR INDEXES AND 8/	90536	7019283-00	16	
-9	C1 THRU C21	E	CAPACITOR, FIXED, CERAMIC DIELECTRIC, 25 VDC, 0.47 MF, M20 PCT P80 PCT	80183	7900092-04 5C11A9	21	
-10	R1 THRU R36	E	RESISTOR	81349	RC07GF151J	36	
-11	P1 P2	E	CONNECTOR, RECEPTACLE, ELECTRICAL, FEMALE, 189 CONTACT	91886	7900843-00 3614676	2	
-12	TB1 TB2	E	TEST POINT ASSEMBLY, 231 CONTACTS WIRE WRAP	91886	7900841-00 3614873	2	
-13	A2	E	RESISTOR ASSEMBLY /FOR BREAKDOWN SEE FIG 7-9/	90536	7034859-00	1	

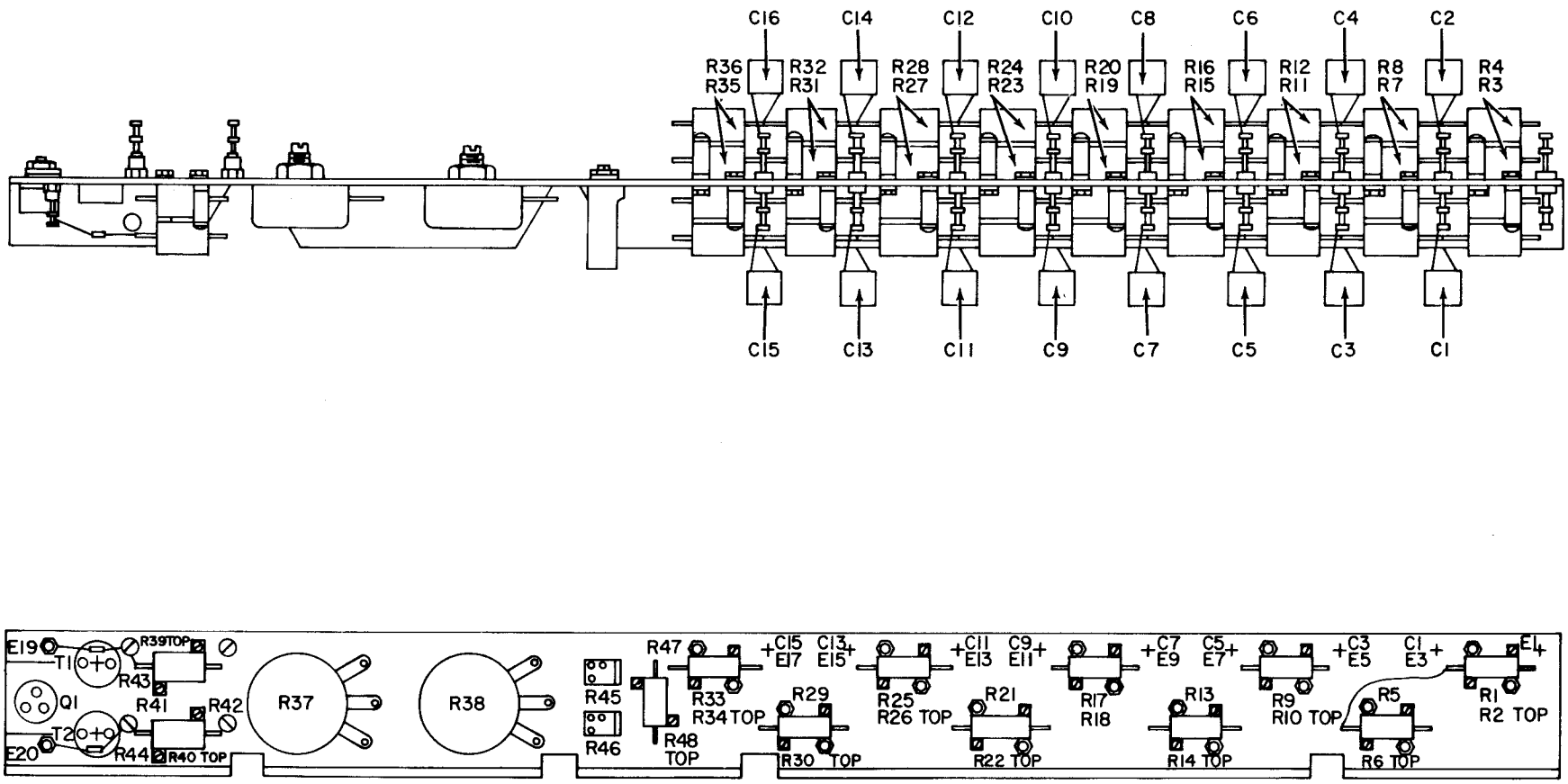


Figure 7-10. Resistor Assembly (A4A2A2)

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
7-10	A2	E	RESISTOR ASSEMBLY /FOR NHA SEE FIG 7-9/	90536	7034859-00	REF	
	C1 THRU C16	E	CAPACITOR, FIXED, CERAMIC DIELECTRIC, 25 VDC, 1 UF, M20 %, P80 %	56289	7900092-00 5C13C2	16	
	Q1	E	TRANSISTOR	81349	2N539	1	
	R1 THRU R36	E	RESISTOR	81349	RE65N46R4	36	
	R37 R38	E	RESISTOR	81349	RA30LASB100A	2	
	R39 THRU R42	E	RESISTOR	81349	RE65N40R2	4	
	R43 R44	E	RESISTOR	81349	RC07GF391J	2	
	R45 R46	E	RESISTOR, VARIABLE, 2000 OHM, PORM 5 PCT, 1 W, 70 DEG C /158 DEG F/ LINEAR TAPER, SINGLE SHAFT	80294	4912695-11 224S-1-202	2	
	R47	E	RESISTOR, FIXED, WIREWOUND, 5.5 OHM, PORM 1 %, 10 W	91637	7902306-04 NH10,5R5,1	1	
	R48	E	RESISTOR	81349	RE65N15R0	1	
	T1 T2	E	REACTOR, 1 MH, 250 MA	90536	4057445-00	2	

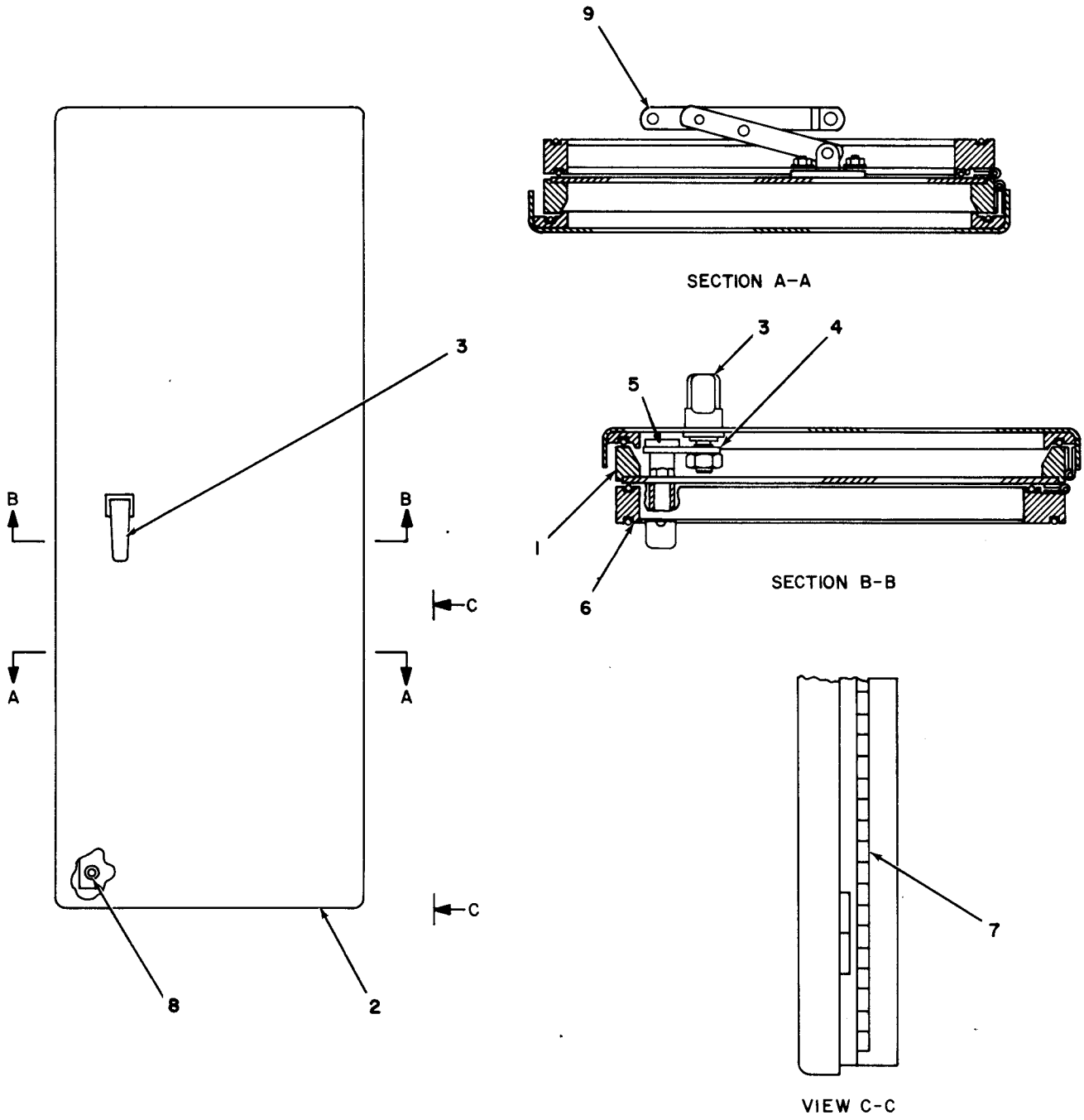


Figure 7-11. Electrical Equipment Door Panel Assembly (A3)

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
7-11	A3	D	DOOR PANEL ASSEMBLY, ELECTRICAL EQUIPMENT /FOR NHA SEE FIG 7-2/	90536	7053793-03	REF	A
	A3	D	DOOR PANEL ASSEMBLY, ELECTRICAL EQUIPMENT /FOR NHA SEE FIG 7-2/	90536	7053793-02	REF	B
	A3	D	DOOR PANEL ASSEMBLY, ELECTRICAL EQUIPMENT /FOR NHA SEE FIG 7-2/	90536	7053793-04	REF	C
-1	A1	E	CONTROL-INDICATOR /FOR BREAKDOWN SEE FIG 7-12/	90536	7053783-03	1	A
	A1	E	CONTROL-INDICATOR /FOR BREAKDOWN SEE FIG 7-12/	90536	7053783-02	1	B
	A1	E	CONTROL-INDICATOR /FOR BREAKDOWN SEE FIG 7-12/	90536	7053798-01	1	C
-2		E	DOOR, ELECTRICAL EQUIPMENT, CABINET	90536	7033949-00	1	B
		E	DOOR, ELECTRICAL EQUIPMENT, CABINET	90536	7033949-01	1	A,C
-3		E	LATCH, RIM CLINCHING	90536	7008890-00	1	
-4		E	PAWL, 1-68 IN. LG	90536	7019285-00	1	
-5		E	SPACER, SLEEVE	90536	7019290-00	1	
-6		E	STUD, TURNLOCK FASTENER, 1.887 IN. LG	90536	7025360-00	1	
		E	RING, RETAINING, TURNLOCK FASTENER *AP*	08524	7900836-00 D1021A1	1	
		E	SPRING, HELICAL, COMPRESSION /AP/	90536	7025366-00	1	
-7		E	HINGE, BUTT	90536	7019286-00	1	
		E	WASHER, FLAT, NO. 6 /AP/	96906	MS15795-805	6	
		E	SCREW, MACH, PAN HD, 6-32UNC2A BY 0.312 IN. LG /AP/		4912524-01 COML	6	
-8		E	STUD, TURNLOCK FASTENER, 1.137 IN. LG /AP/	90536	7025359-00	2	
		E	RING, RETAINING, TURNLOCK FASTENER /AP/	08524	7900836-00 D1021A1	2	
		E	SPRING, HELICAL, COMPRESSION /AP/	90536	7025366-00	2	
-9		E	STAY, FOLDING	90536	7019297-00	1	

FIG. & INDEX NO.	REF. DESIG.	NOTE	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
11		E	STAY, FOLDING BY 0.428 IN. LG /AP/	90536	7019296-00	1	
		E	SCREW, MACH, FLAT HD, 6-32UNC-2A	96906	MS51959-201	2	
		E	WASHER, FLAT, NO. 6 /AP/	96906	MS315795-805	2	
		E	NUT, SELF-LOCKING, HEX, 6-32UNC-3B /AP/	96906	MS20144C06	2	

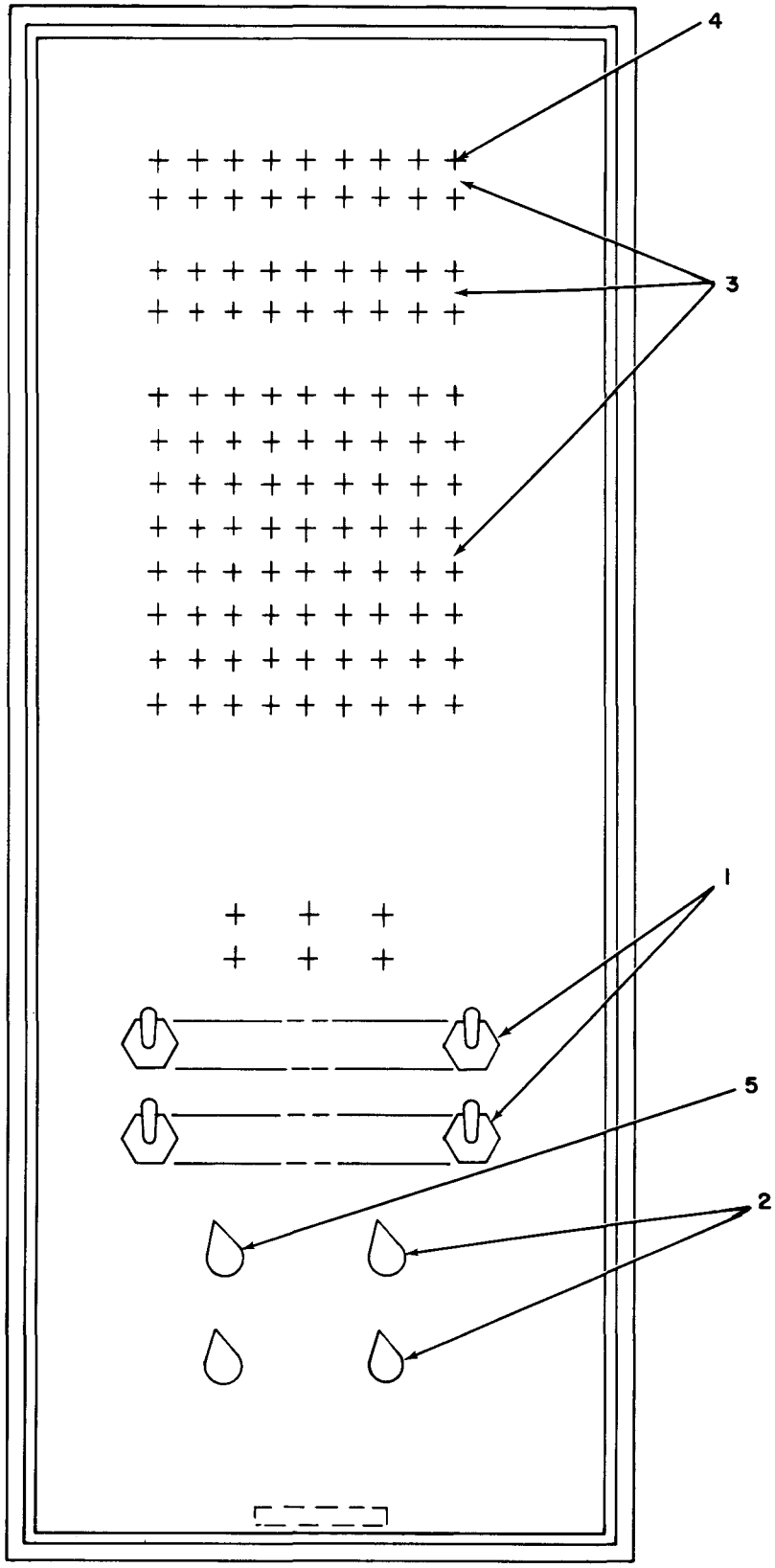


Figure 7-12. Control-Indicator Assembly (A1A3)

FIG. & INDEX NO.	REF. DESIG.	INDEX	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
7-12	A1	E	CONTROL-INDICATOR /FOR NHA SEE FIG 7-11/	90536	7053783-02	REF	A
	A1	E	CONTROL-INDICATOR /FOR NHA SEE FIG 7-11/	90536	7053783-03	REF	B
-1	S1 THRU S8	F	SWITCH	96906	MS25086-23	8	
-2	S9 THRU S12	F	SWITCH	81349	SR04B36C3MPC2-4N	4	
-3	XDS2A XDS4A THRU XDS12A XDS1B THRU XDS14B XDS1C THRU XDS12C XDS1D THRU XDS14D XDS1E THRU XDS12E XDS1F THRU XDS14F XDS1G THRU XDS12G XDS1H THRU XDS14H XDS1I THRU XDS12I XDS1J THRU XDS12J	F	SWITCH, PUSH, INDICATOR TYPE, WITH LAMP, TRANSISTORIZED	72619	7900496-23 908-1166-1633-526	126	
-4		F	NUT, PLAIN, ROUND, AL, CLEAR COLOR, 0.375-32NEF-2	07137	7900880-00 1112-2	54	
-5		F	KNOB	96906	MS91528-1K2B	4	

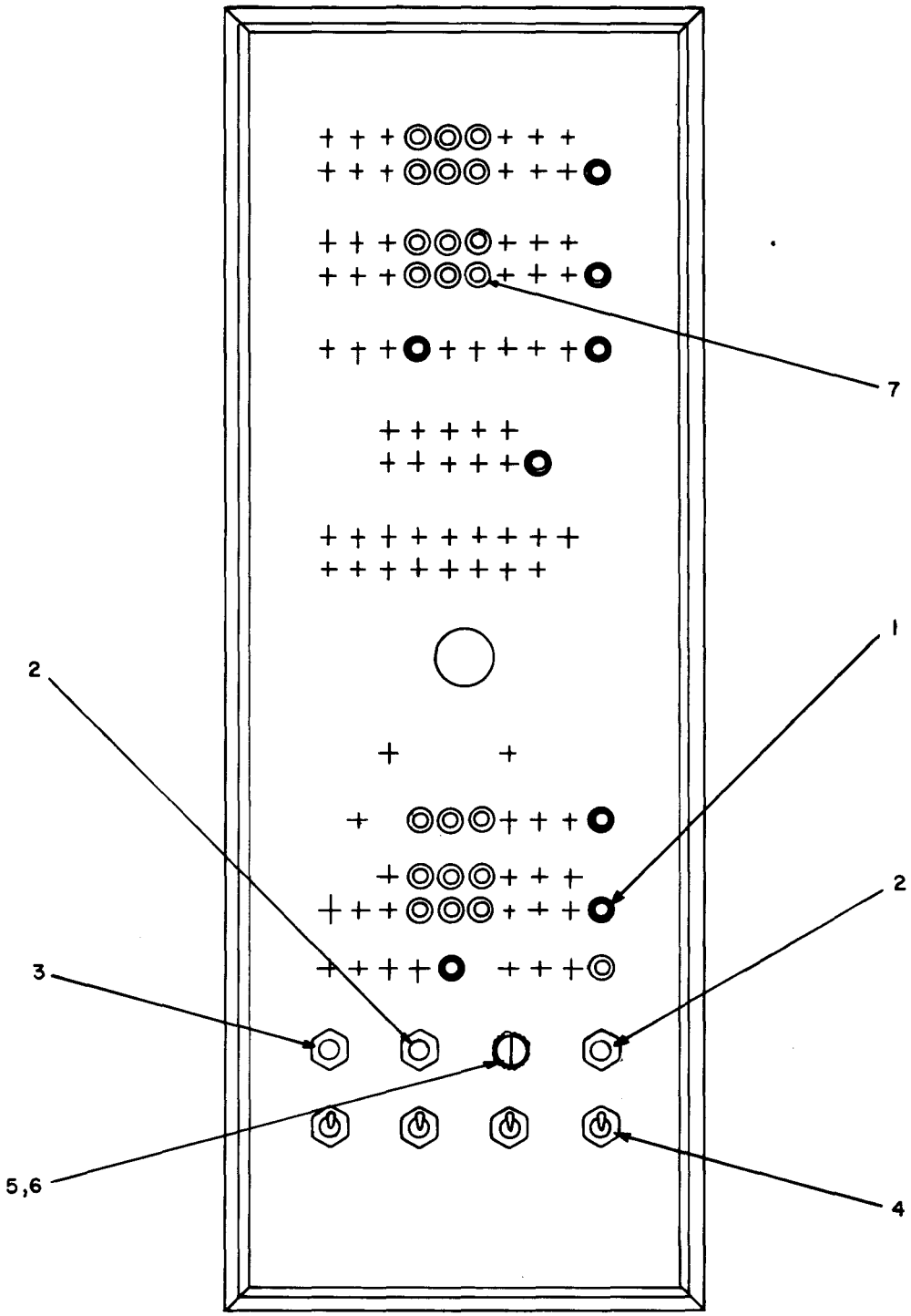


Figure 7-13. Control-Indicator

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
7-13		E	CONTROL-INDICATOR /FOR NHA SEE FIG 7-11/	90536	7053798-01	REF	
-1	S1 THRU S8	F	SWITCH, PUSH, SPST CONTACT	07137	7900987-00 MBS-S1838A9	8	
-2	S9 S10	F	SWITCH, TOGGLE, 2 POLE, 3 POSITION	91929	7900635-01 13AT418T2	2	
-3	S11	F	SWITCH, TOGGLE, 2 POLE, 3 POSITION	91929	7900635-02 13AT416T2	1	
-4	S12 THRU S15	F	SWITCH	96906	MS35059-23	4	
-5	R1	F	RESISTOR	81349	RV4NYSD105A	1	
-6		F	KNOB	96906	MS91528-1N28	1	
-7	XDS14A XDS1B THRU XDS5B XDS8B XDS11B THRU XDS14B XDS1C THRU XDS5C XDS8C XDS9C XDS11C THRU XDS14C XDS1E THRU XDS9E XDS11E XDS12E XDS13E XDS1F THRU XDS9F XDS11F XDS12F XDS1G THRU XDS4G XDS6G THRU XDS9G XDS11G	F	SWITCH, PUSH, INDICATOR TYPE, WITH LAMP, TRANSISTORIZED	72619	7900496-23 908-1166-1633-526	104	

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
13	THRU XDS14G XDS1H THRU XDS10H XDS12H XDS13H XDS14H XDS1I THRU XDS5I XDS8I XDS9I XDS11I XDS13I XDS14I XDS1J THRU XDS5J XDS8J XDS9J XDS13J XDS14J						

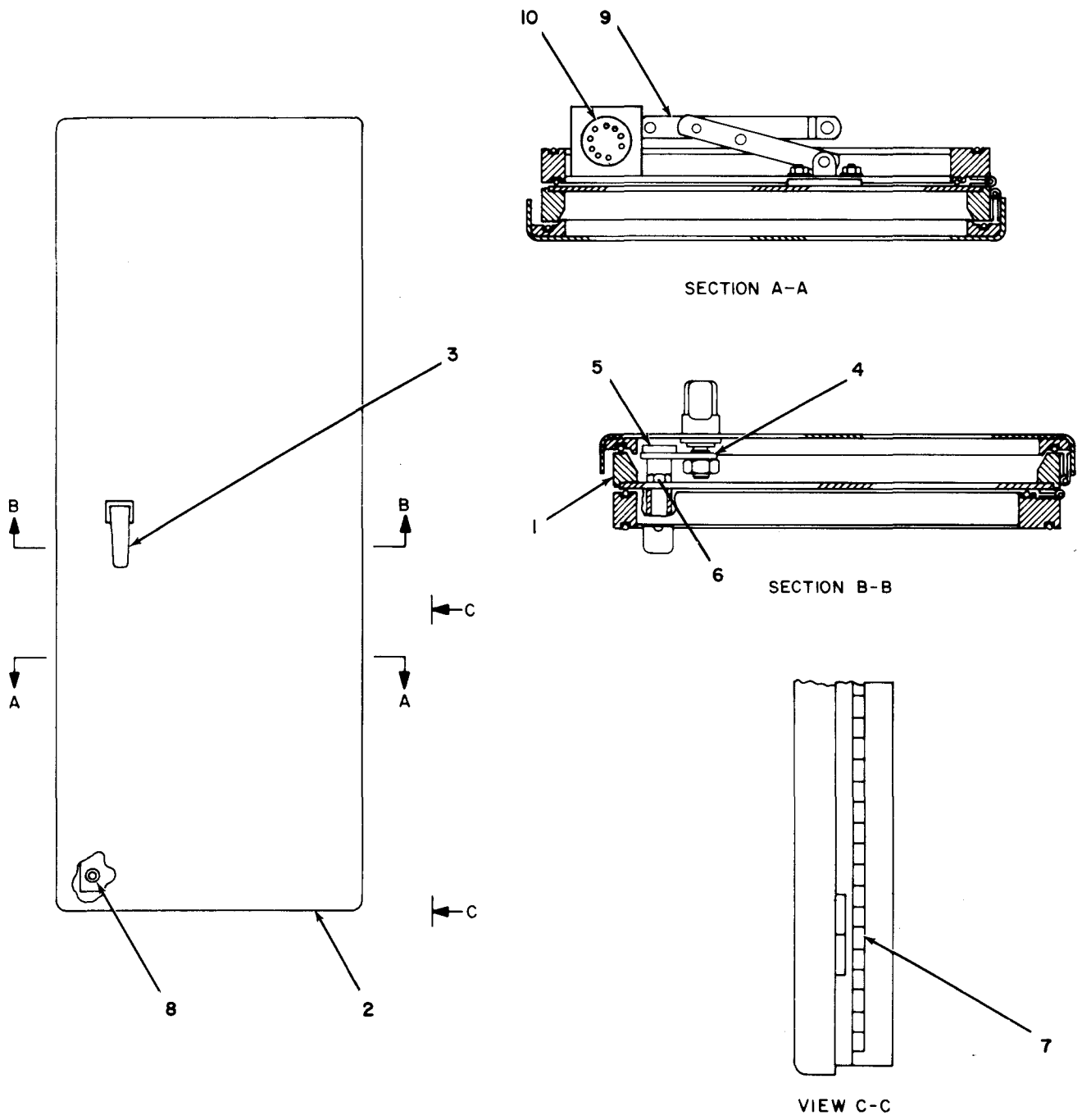


Figure 7-14. Door Panel Assembly (A3)

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
7-14	A3	D	DOOR AND PANEL ASSEMBLY /FOR NHA SEE FIG 7-2/	90536	7019284-26	REF	A
		D	DOOR AND PANEL ASSEMBLY /FOR NHA SEE FIG 7-2/	90536	7019284-32	REF	B
-1	A1	E	CONTROL-INDICATOR ASSEMBLY /FOR BREAKDOWN SEE FIG 7-15/	90536	7024767-02	1	A
	A1	E	PANEL, BLANK, ELECTRICAL EQUIPMENT	90536	7025725-03	1	B
-2		E	DOOR, ELECTRICAL EQUIPMENT	90536	7033949-01	1	
-3		E	LATCH, RIM CLINCHING	90536	7008890-00	1	
-4		E	PAWL, 1.68 IN. LG	90536	7019285-00	1	
-5		E	SPACER, SLEEVE	90536	7019290-00	1	
-6		E	STUD, TURNLOCK FASTENER	90536	7025360-00	1	
		E	RING, RETAINING, TURNLOCK FASTENER /AP/	08524	7900836-00 D1021A1	1	
		E	SPRING, HELICAL, COMPRESSION /AP/	90536	7025366-00	1	
-7		E	HINGE, BUTT	90536	7019286-00	1	
		E	SCREW, PAN HD, 6-32UNC-2A BY 0.312 IN. LG /AP/		4912524-01 COML	6	
		E	WASHER, FLAT, NO. 6 /AP/	88044	MS15795-805	6	
-8		E	STUD, TURNLOCK FASTENER	90536	7025359-00	2	
		E	RING, RETAINING, TURNLOCK FASTENER /AP/	08524	7900836-00 D1021A1	2	
		E	SPRING, HELICAL, COMPRESSION /AP/	90536	7025366-00	2	
-9		E	STAY, FOLDING	90536	7019297-00	1	A
		E	SCREW, FLAT HD, 6-32UNC-2A BY 0.438 IN. LG /AP/	88044 88044	MS51959-29 MS15795-805	2	A
		E	NUT, SELF-LOCKING, 6-32UNC-3B /AP/	88044	MS21044C06	2	A
-10	Y1	E	OSCILLATOR, AUDIO FREQUENCY, 15 VDC, 1024 HZ	95267	7901046-00 TFG5345-00	1	A

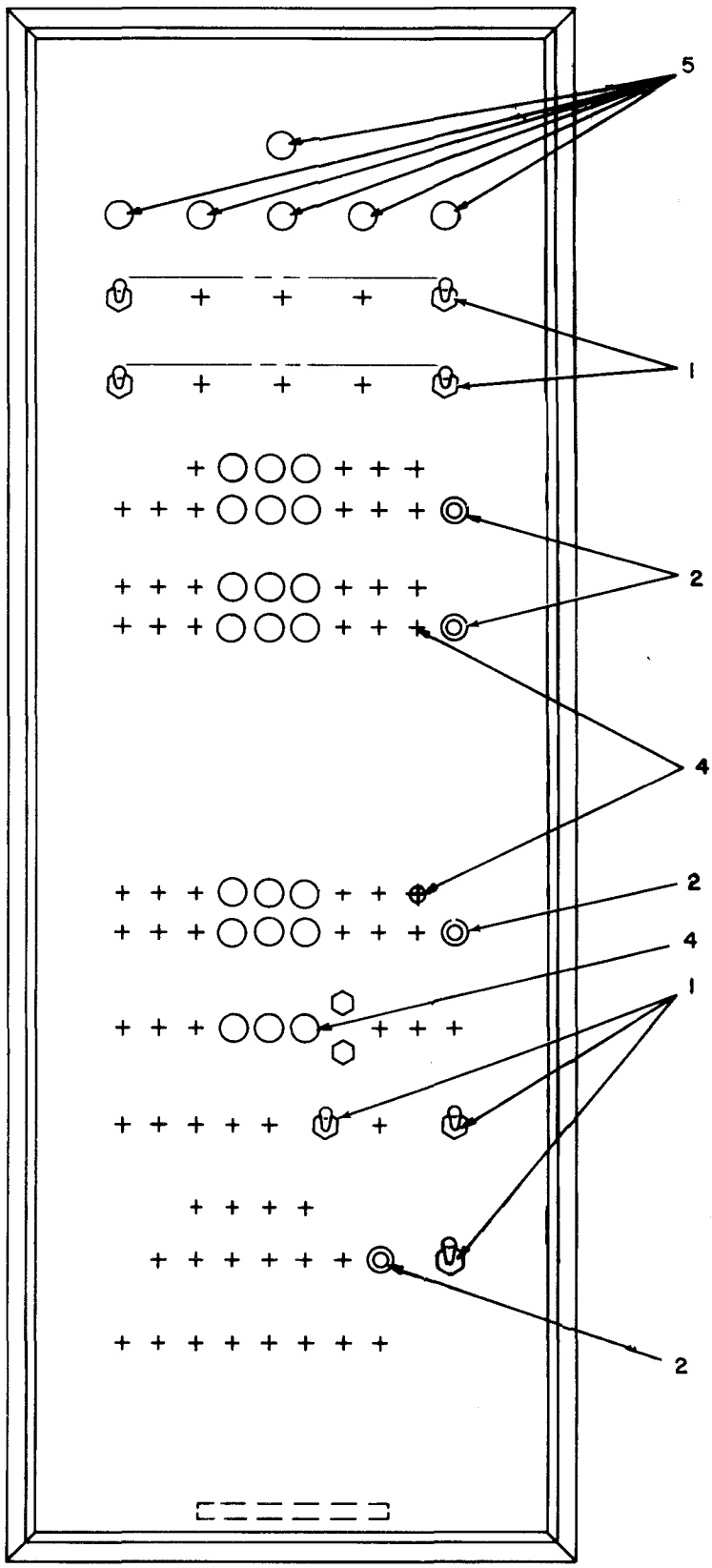


Figure 7-15. Control-Indicator Assembly (A4A3)

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
7-15	A1	E	CONTROL-INDICATOR ASSEMBLY /FOR NHA SEE FIG 7-14/	90536	7024767-02	REF	
-1	S1 THRU S10 S14 S15 S17	F	SWITCH	96906	MS35059-23	13	
-2	S11 S12 S13 S16	F	SWITCH, PUSH, SPST, MOMENTARY, WHITE, PUSHBUTTON, 100 MA, 110 VAC	07137	7900987-00 MBS-S1838A9	4	
-3	XDS7A XDS1B THRU XDS7B XDS1C THRU XDS8C XDS11C XDS2D THRU XDS6D XDS10D XDS11D XDS1E THRU XDS7E XDS9E XDS10E XDS11E XDS1F THRU XDS11F XDS1G THRU XDS11G XDS1H THRU XDS11H XDS2I THRU XDS8I XDS10I XDS11I XDS2J THRU XDS8J	F	SWITCH, PUSH, INDICATOR TYPE WITH LAMP, TRANSISTORIZED	72619	7900496-23 908-1166-1633-526	84	
-4		F	NUT, PLAIN, ROUND, AL, CLEAR COLOR, 0.375-32NEF-2	07137	7900880-00 1112-1	21	
-5		F	SWITCH, PUSH, INDICATOR TYPE WITH LAMP, TRANSISTORIZED	72619	7900215-00 920-1113-1631-522	6	

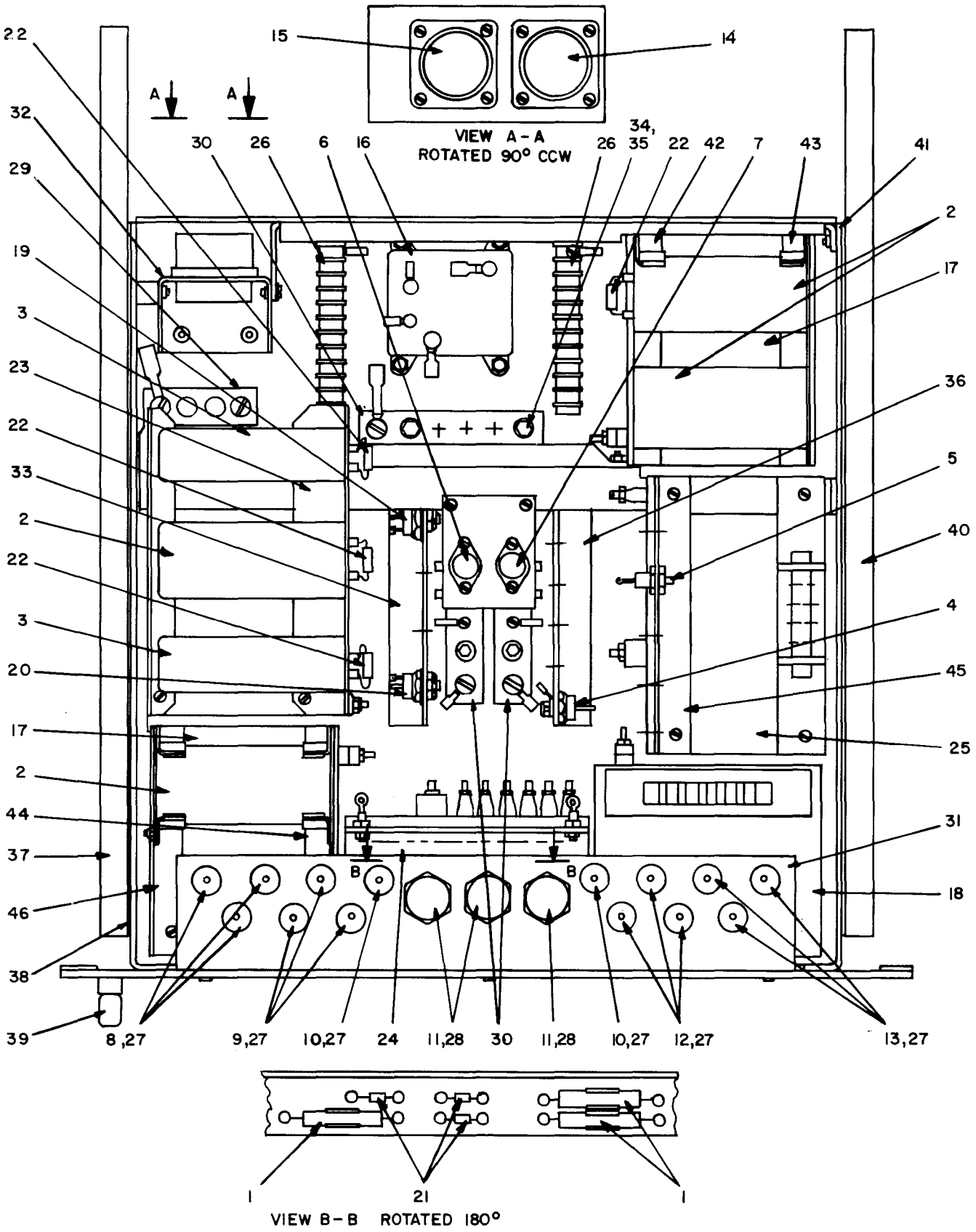


Figure 7-16. Power Supply (PS1)

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
7-16	PS1	B	POWER SUPPLY /FOR NHA SEE FIG 7-1/	90536	7038864-02	REF	
-1	C1 C2 C3	C	CAPACITOR	81349	CL25BH221UP3	3	
-2	C4 C6 C8 C9	C	CAPACITOR	81349	CE71C332G	4	
-3	C5 C7	C	CAPACITOR	81349	CE71C152G	2	
-4	CR1 THRU CR18	C	SEMICONDUCTOR DEVICE, DIODE	81349	1N1186	18	
-5	CR9 THRU CR24 CR27 THRU CR32	C	SEMICONDUCTOR DEVICE, DIODE	81349	1N1202	12	
-6	CR25	C	SEMICONDUCTOR DEVICE, DIODE	81349	1N2807B	1	
-7	CR26	C	SEMICONDUCTOR DEVICE, DIODE	81349	1N2808B	1	
-8	F1 F2 F3	C	FUSE	81349	F03A250V8AS	3	
-9	F4 F5 F6	C	FUSE	81349	F02A250V2AS	3	
-10	F7 F11	C	FUSE	81349	F02A250V6AS	2	
-11	F8 F9 F10	C	FUSE	81349	F03A125V20AS	3	
-12	F12 F13 F14	C	FUSE	81349	F02A250V5AS	3	
-13	F15 F16 F17	C	FUSE	81349	F03A250V12AS	3	
-14	J1	C	CONNECTOR	96906	MS3102A32-6P	1	
-15	J2	C	CONNECTOR	96906	MS3102A32-6PW	1	

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
16-16	K1	C	RELAY	96906	MS24143A2	1	
-17	L1 L3	C	REACTOR, FILTER CHOKE, 50 V, 450 UH, 80 AMP, 5 MILLIOHMS, METAL CASE	80023	4913131-00 S3804	2	
-18	L2	C	REACTOR, 50 V, 0.1 MH, 70 AMP, 0.0025 OHM, METAL CASE	80023	4913130-00 S3810	1	
-19	Q1 Q2	C	TRANSISTOR, SILICON, POWER	13327	7900755-00 MHT8034	2	
-20	Q3 Q4	C	TRANSISTOR, NPN, SILICON POWER	13327	7900756-00 MHT7038	2	
-21	R1 R2 R3	C	RESISTOR	81349	RC07GF104J	3	
-22	R4 THRU R7	C	RESISTOR	81349	RC42GF222J	4	
-23	T1	C	TRANSFORMER, POWER, STEP-DOWN PRIMARY 115 V, 400 HZ, 0-PHASE DELTA TO 3-PHASE DOUBLE WYE, SECONDARY 24.3 V AT 23 AMP	80023	4913127-00 S3802B	1	
-24	T2	C	TRANSFORMER, POWER, STEP-DOWN, PRIMARY 115 V, 400 HZ, 3-PHASE DELTA TO 3-PHASE DOUBLE WYE, SECONDARY 7.5 V AT 20 AMP	80023	4913126-00 S3808A	1	
-25	T3	C	REACTOR-TRANSFORMER, 115 VAC, 400 HZ EACH LEG OF 3-PHASE DELTA, 22.6 VRMS EACH LEG OF 3-PHASE DOUBLE WYE, WITH BALANCE COIL AND TWO 1 MH INDICATORS	80023	7901103-00 S4788	1	
-26	TB1 TB2	C	TERMINAL BOARD, BARRIER TYPE, 11 SCREW TYPE TERM	75382	4912675-10 20011	2	
-27	XF1 THRU XF7 XF11 THRU XF17	C	FUSEHOLDER	81349	FHN26G2	14	
-28	XF8 XF9 XF10	C	FUSEHOLDER, INDICATOR-TYPE, 125 V, 30 AMP	84613	908672-09 IND300-9	3	
-29	W1	C	BUS BAR	90536	7005432-00	1	
-30	W2 W3	C	BUS BAR	90536	7005427-00	3	

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
16	W4						
-31		C	BRACKET, FUSEHOLDER	90536	7019267-00	1	
-32		C	BRACKET, ELECTRICAL CONNECTOR	90536	7038852-00	1	
-33		C	BRACKET, ANGLE, DIODE-TRANSISTOR	90536	7019269-00	1	
-34		C	INSULATOR PLATE, 4.88 IN. LG /FOR W1, W3, AND W4/	90536	7005428-00	3	
-35		C	INSULATOR, BUSHING, BUS BAR	90536	7005429-00	14	
-36		C	BRACKET, ANGLE, DIODE	90536	7008587-02	1	
-37		C	SLIDE, TELESCOPING, 22 IN. LG	05236	7901056-01 350266-R	1	
-38		C	SHIM, TELESCOPING SLIDE	90536	7025682-00	3	
		C	SCREW, FLAT HD, 10-32UNF-2A BY 0.625 IN. LG /AP FOR INDEXES 41 AND 42/		4912507-03 COML	4	
-39		C	LATCH, RIM CLINCHING	90536	7009074-00	2	
-40		C	SLIDE, TELESCOPING, 22 IN. LG	05236	7901056-00 350266-L	1	
-41		C	SHIM, TELESCOPING SLIDE	90536	7025682-00	3	
		C	SCREW, FLAT HD, 10-32UNF-2A, 0.625 IN. LG /AP FOR 10/		4912507-03 COML	4	
-42		C	BRACKET, ANGLE, CAPACITOR	90536	7030413-00	1	
-43		C	BRACKET, ANGLE, CAPACITOR	90536	7030413-01	1	
-44		C	BRACKET, ANGLE, CAPACITOR, RH	90536	7030414-00	1	
-45		C	BRACKET, ANGLE, DIODE	90536	7030416-00	1	
-46		C	BRACKET, CAPACITOR, LH	90536	7030417-00	1	
-47							

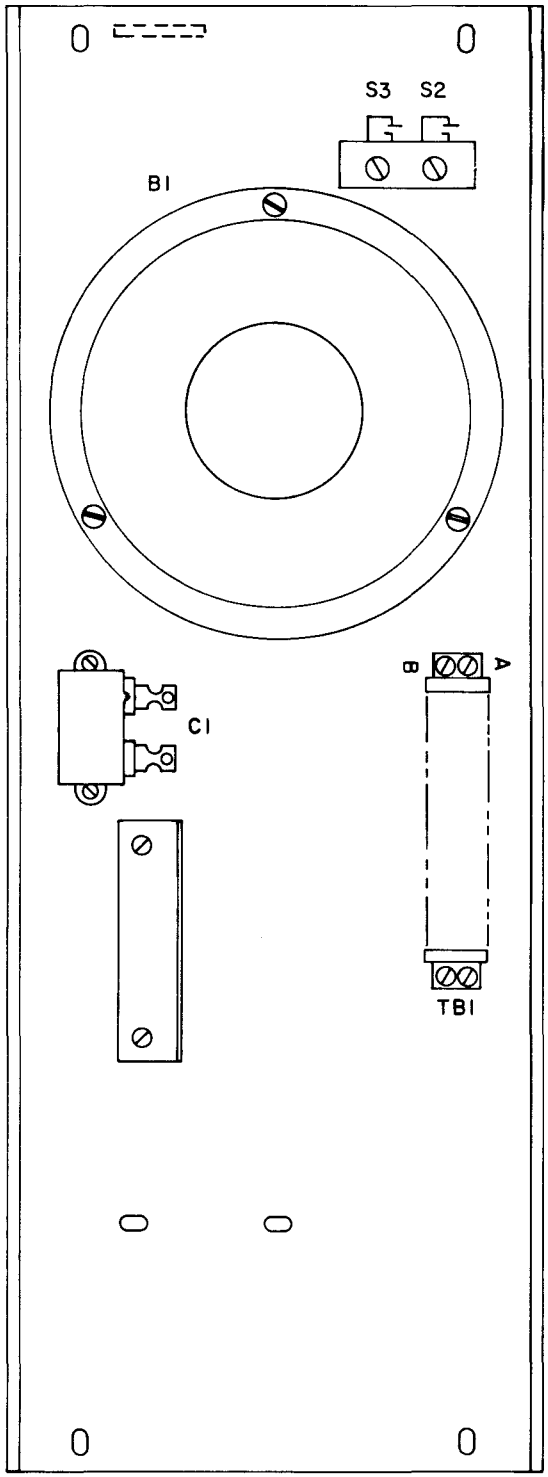


Figure 7-17. Fan Assembly (A6)

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
7-17	A6	B	FAN ASSEMBLY /FOR NHA SEE FIG 7-1/	90536	7033221-01	REF	
	B1	C	FAN, CENTRIFUGAL, 115 V, 400 HZ, SINGLE PHASE	17771	7901287-00 E2231-1	1	
		C	SCREW, MACHINE, PAN HD, 8-32-UNC-2A, 0.5 IN. LG /AP/		4912525-08 COML	3	
		C	WASHER, FLAT, NO. 8 /AP/	96906	MS15795-807	3	
	C1	C	CAPACITOR	81349	CH53B1MF504K	1	
		C	SCREW, MACHINE, PAN HD, 6-32-UNC-2A, 0.5 IN. LG /AP/		4912524-04 COML	2	
	S2	C	SWITCH, THERMOSTATIC, SPST, SEALED, CONTACTS CLOSE ON TEMP INCREASE, 111 DEG F /44 DEG C/ TO 115 DEG F %46 DEG C=	82647	4912495-10 4286A2-184	1	
	S3	C	SWITCH, THERMOSTATIC, SPST, SEALED, CONTACTS OPEN ON TEMP INCREASE, 136 DEG F /58 DEG C/ TO 140 DEG F /60 DEG C/	82647	4912495-09 4286A2-68	1	
	TB1	C	TERMINAL BOARD, BARRIER TYPE, 12 SCREW TYPE TERM	75382	4912675-11 20012	1	
		C	SCREW, MACHINE, PAN HD, 4-40UNC-2A, 0.562 IN. LG /AP/		4912523-07 COML	4	
		C	WASHER, LOCK, SPRING, NO. 4 /AP/	96906	MS35338-135	4	
		C	WASHER, FLAT, NO. 4 /AP/	96906	MS15795-803	4	

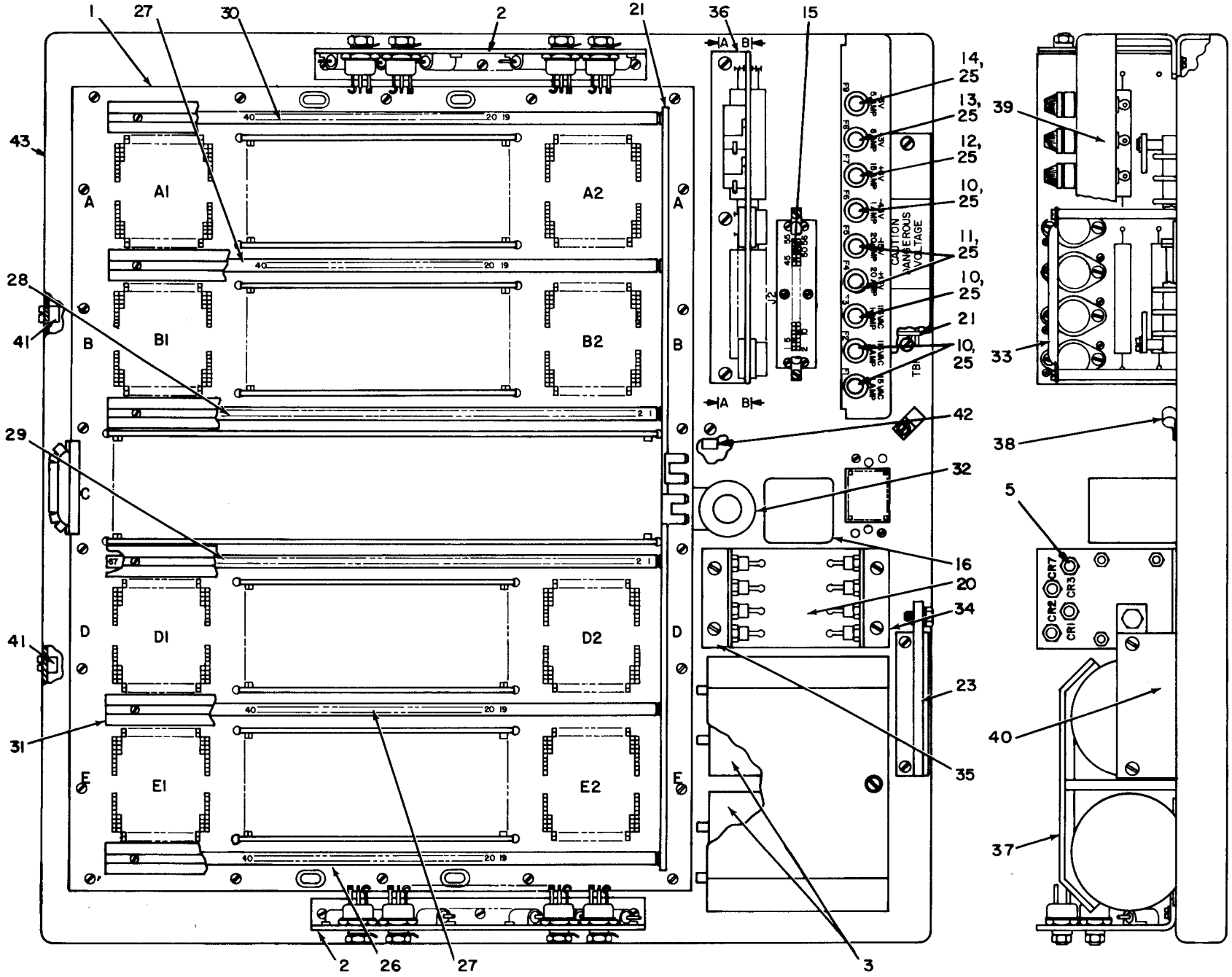


Figure 7-18. Electrical Equipment Chassis Assembly (A2) (Sheet 1 of 2)

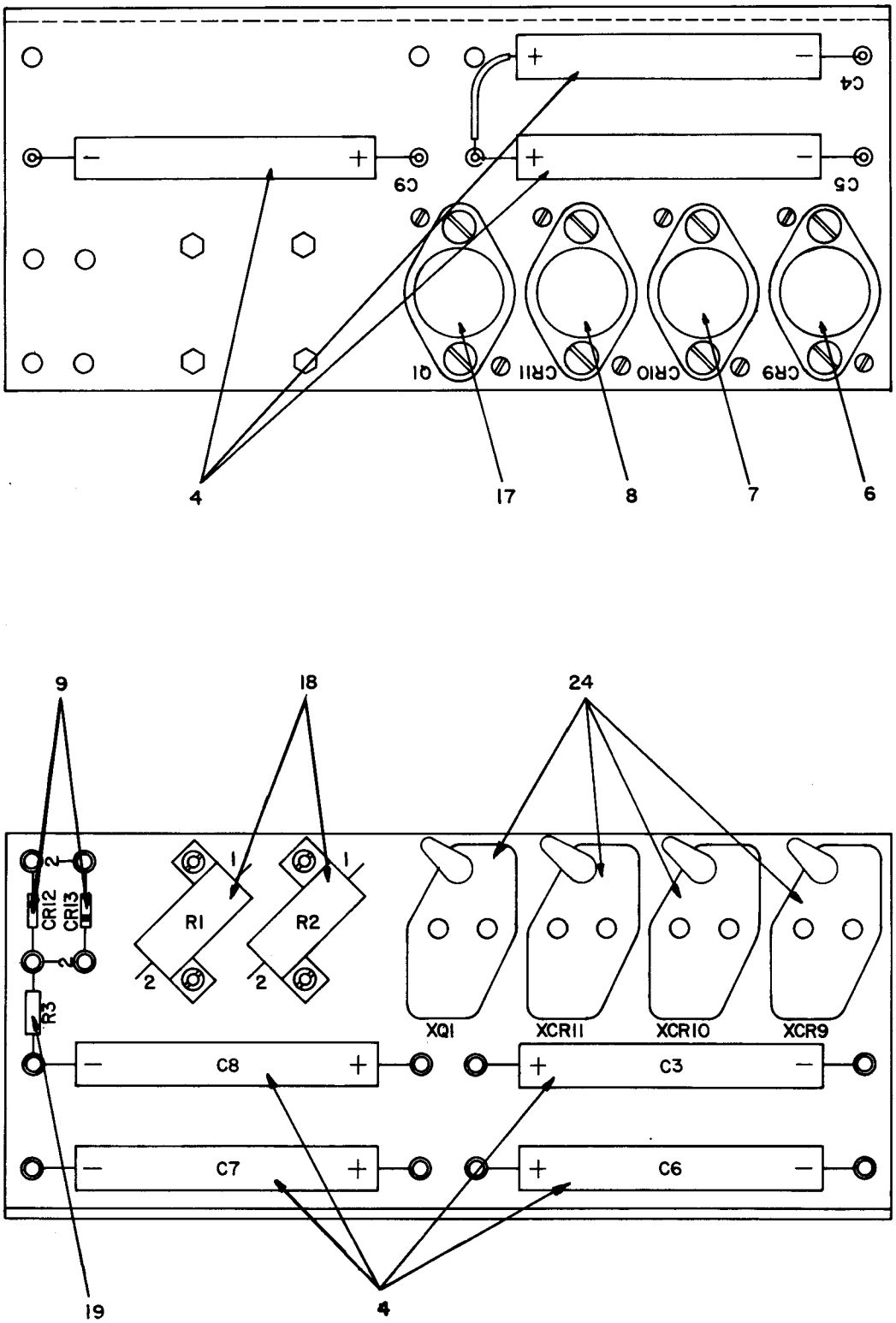


Figure 7-18. Electrical Equipment Chassis Assembly (A2) (Sheet 2 of 2)

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
7-18	A2	D	CHASSIS ASSEMBLY, ELECTRICAL EQUIPMENT /FOR NHA SEE FIG 7-3/	90536	7053752-00	REF	A
	A2	D	CHASSIS ASSEMBLY, ELECTRICAL EQUIPMENT /FOR NHA SEE FIG 7-3/	90536	7085700-00	REF	B
-1	A1	E	PANEL ASSEMBLY, ELECTRICAL CONNECTOR /FOR BREAKDOWN SEE FIG 7-19/	90536	7053755-00	1	
-2	A2 A3	E	COMPONENT ASSEMBLY, ELECTRICAL /FOR BREAKDOWN SEE FIG 7-20/	90536	7078176-00	2	
-3	C1 C2	E	CAPACITOR	81349	CE71C223F	2	
-4	C3 THRU C9	E	CAPACITOR	81349	CL25BH301UP3	7	
-5	CR1 THRU CR8	E	SEMICONDUCTOR DEVICE, DIODE	81349	1N1202	8	
-6	CR9	E	SEMICONDUCTOR DEVICE, DIODE	81349	1N2806B	1	
-7	CR10	E	SEMICONDUCTOR DEVICE, DIODE	81349	1N2804B	1	
-8	CR11	E	SEMICONDUCTOR DEVICE, DIODE	81349	1N2805B	1	
-9	CR12 CR13	E	SEMICONDUCTOR DEVICE, DIODE, SILICON, SWITCHING	03508	7901126-00 DHD894	2	
-10	F1 F2 F3 F6	E	FUSE	81349	F02A250V1AS	4	
-11	F4 F5	E	FUSE	81349	F03A125V20AS	2	
-12	F7	E	FUSE	81349	F03A250V15AS	1	
-13	F8	E	FUSE	81349	F03A250V8AS	1	
-14	F9	E	FUSE	81349	F02A250V102AS	1	
-15	J2	E	CONNECTOR, RECEPTACLE, ELECTRICAL, PLATE, FEMALE, 56 CONTACT	91886	7902206-00 5893517	1	
-16	L1	E	REACTOR, MH, AT 6.5 AMP, 2.5 VEMS, 120 HZ	80023	7900382-00 S4310	1	
-Q1		E	TRANSISTOR, NPN, SILICON, POWER	04713	7902045-00 SJ1245	1 1	

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
18-18	R1 R2	E	RESISTOR	81349	RE70GR402	2	
-19	R3	E	RESISTOR	81349	RC07GF102J	1	
-20	T1	E	TRANSFORMER, POWER, STEP-DOWN, 115 VOLTS, 400 HZ, 3-PHASE DELTA TO 6-PHASE STAR	80023	7902557-00 S5407	1	
-21	TB1	E	TERMINAL BOARD, BARRIER TYPE, 8 SCREW TYPE TERM	75382	900126-02 602-8	1	
-22	W1	E	BUS BAR	90536	7053758-00	1	
-23	W2	E	BUS BAR	90536	7074820-00	1	
-24	XCR9 THRU XCR11 XQ1	E	SOCKET, SEMICONDUCTOR DEVICE, TO-3	91506	7900149-00 8038-1G3	4	
-25	XF1 THRU XF9	E	FUSEHOLDER	81349	FHN26G2	9	
-26		E	GUIDE, CARD	90536	7053763-00	1	
-27		E	GUIDE, CARD	90536	7053764-00	2	
-28		E	GUIDE, CARD	90536	7053765-00	1	
-29		E	GUIDE, CARD	90536	7053766-00	1	
-30		E	GUIDE, CARD	90536	7053767-00	1	
-31		E	RETAINER, CARD	90536	7053769-00	6	
-32		E	GROMMET	96906	MS35489-49	1	
-33		E	BRACKET, HOLD DOWN, PRINTED CIRCUIT CARD	90536	7078245-00	1	
-34		E	BRACKET, TRANSFORMER-DIODE	90536	7053772-00	1	
-35		E	BRACKET, TRANSFORMER-DIODE	90536	7053772-01	1	
-36		E	BRACKET, MOUNTING, ELECTRICAL COMPONENT	90536	7078177-00	1	
-37		E	CLAMP, CAPACITOR	90536	7053777-00	1	
-38		E	CLAMP, LOOP, NYLON, P-STYLE		900129-04	1	
-39		E	BRACKET, FUSEHOLDER	09922 90536	HP5N 7074821-00	1	
-40		E	BRACKET, BUS BAR	90536	7074822-00	1	A

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
18-41		E	CLAMP, LOOP, NYLON, P-STYLE	09922	900129-03 HP4N	2	
-42		E	CLAMP, LOOP, NYLON, P-STYLE	09922	900129-05 HP6N	1	
-43		E	FRAME, CHASSIS, ELECTRICAL EQUIPMENT	90536	7053753-00	1	A
		E	FRAME, CHASSIS, ELECTRICAL EQUIPMENT	90536	7085702-00	1	B

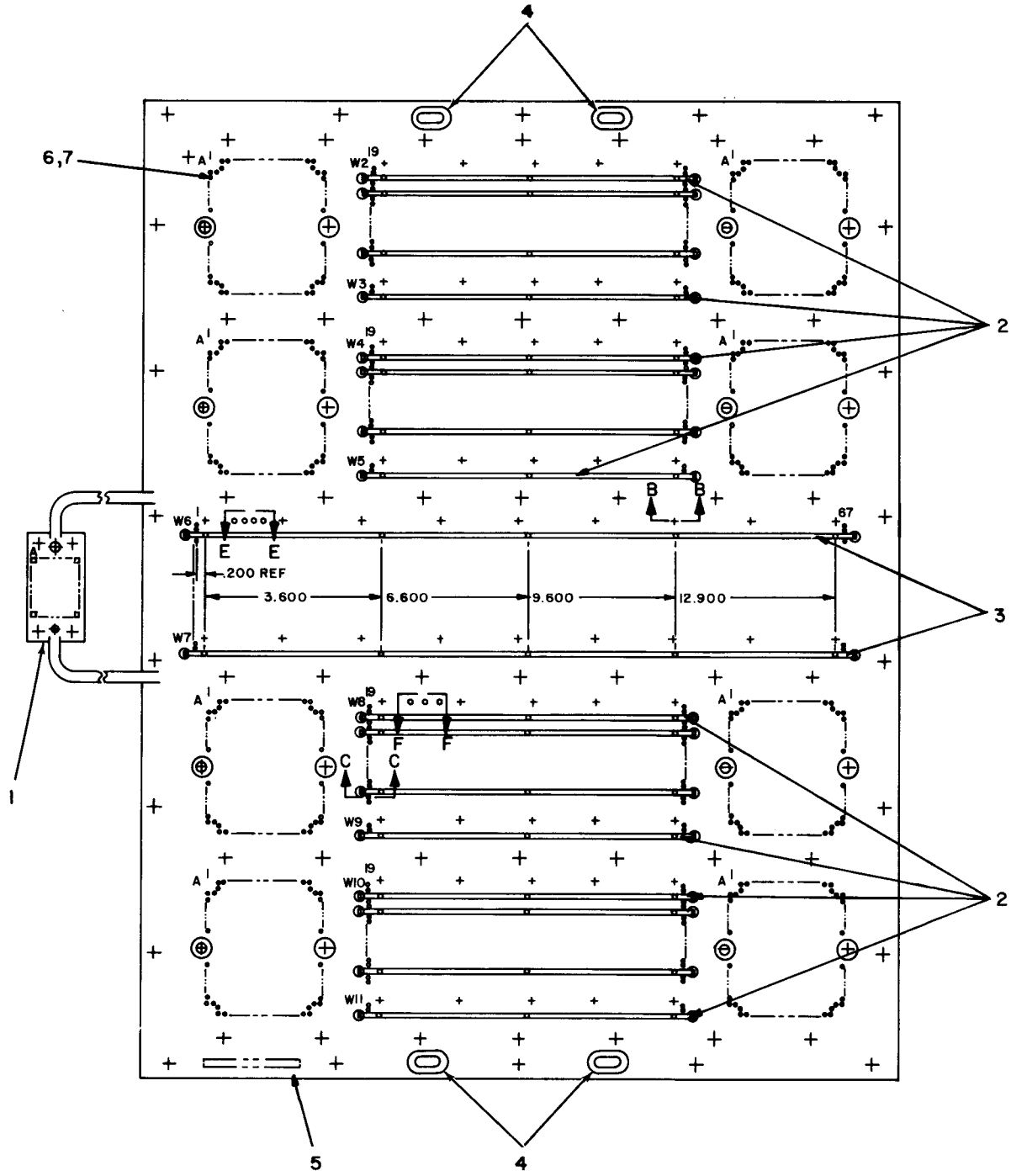


Figure 7-19. Electrical Connector Panel Assembly (A1)

FIG. & INDEX NO.	REF. DESIG.	INDEX	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
7-19	A1	E	PANEL ASSEMBLY, ELECTRICAL CONNECTOR /FOR NHA SEE FIG 7-18/	90536	7053755-00	REF	
-1	J1	F	CONNECTOR, RECEPTACLE, ELECTRICAL, MALE, WIRE WRAP, 120 CONTACTS	91886	7902239-01 5593566	1	
-2	W1 THRU W5 W8 THRU W11	F	BUS BAR, GROUND	90536	7078035-04	8	
-3	W6 W7	F	BUS BAR, GROUND	90536	7078035-05	2	
-4		F	GROMMET, RUBBER, 0.094 GROOVE, 0.375 ID, 0.5 MD, 0.641 OD, 0.25 W		4913271-02 COML	4	
-5		F	PANEL, ELECTRICAL CONNECTOR	90536	7067427-00	1	
-6		G	CONTACT, WIRE WRAP, FEMALE	90536	7050014-01	8144	
-7		G	BUSHING, WIRE WRAP, FEMALE	90536	7050015-00	8144	

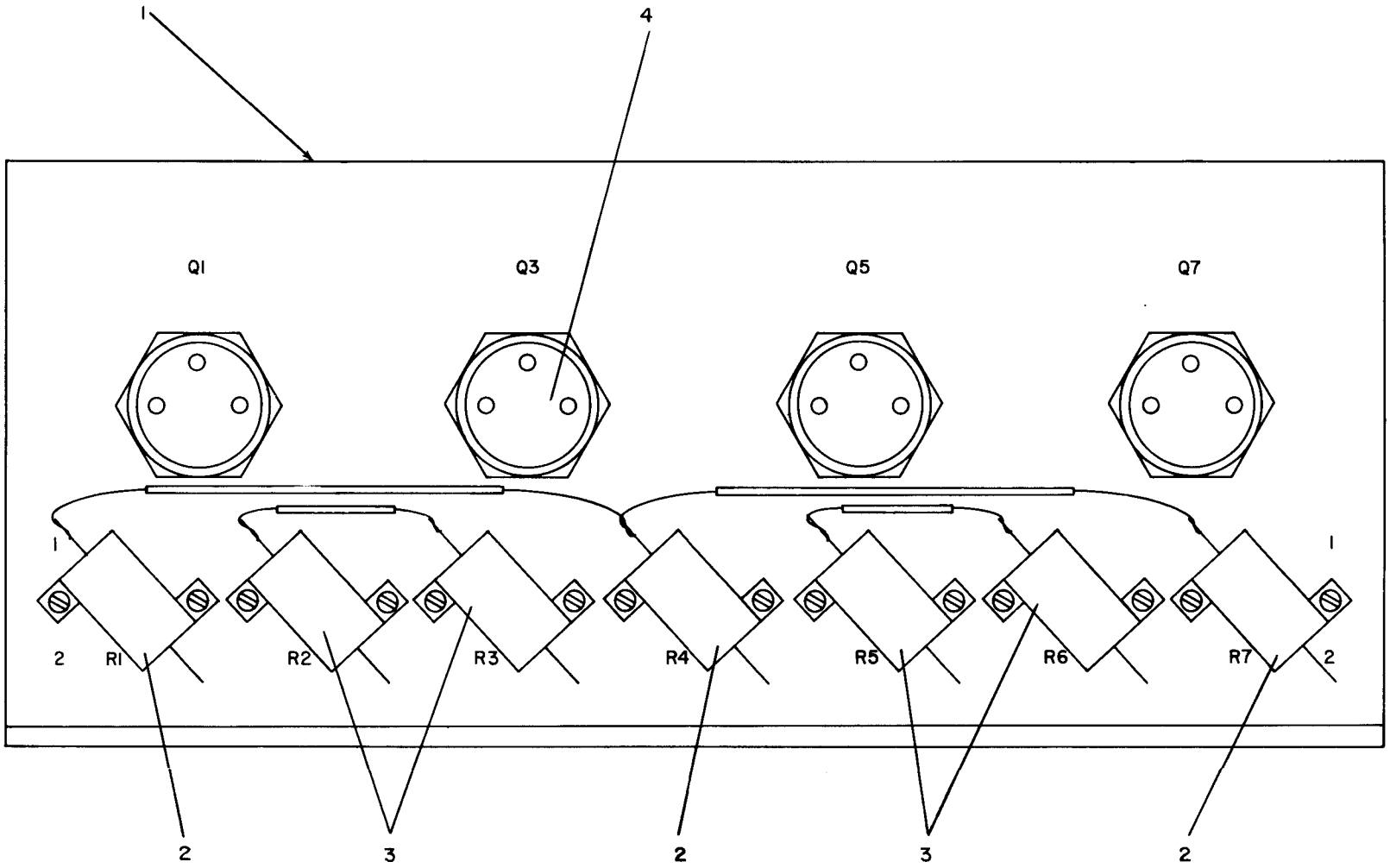


Figure 7-20. Electrical Component Assembly (A2 and A3)

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
7-20	A2 A3	E	COMPONENT ASSEMBLY, ELECTRICAL /FOR NHA SEE FIG 7-18/	90536	7078176-00	REF	
-1	Q1 Q3 Q5 Q7	F	TRANSISTOR, NPN, SILICON, POWER	13327	7900755-00 MHT8034	4	
-2	R1 R4 R7	F	RESISTOR, FIXED, WIRE WOUND, NON-INDUCTIVE, 7.5 OHM, PORM 1 %, 10 W	91637	7900497-99 NH10,7.5,1PCT	3	
-3	R2 R3 R5 R6	F	RESISTOR, FIXED, WIRE WOUND, NON-INDUCTIVE, 15 OHM, PORM 1 %, 10 W	91637	7900497-17 NH10,15.0,1PCT	4	
		F	SCREW, MACHINE, PAN HD, 2-56UNC-2A BY 0.395 IN. LG /AP FOR INDEXES 2 AND 3/		3157139-04 COML	14	
		F	WASHER, FLAT NO. 2 /AP FOR INDEXES 2 AND 3/	96906	MS15795-802	14	
		F	WASHER, LOCK, SPRING, NO. 2 /AP FOR INDEXES 2 AND 3/	96906	MS35338-134	14	
		F	NUT, PLAIN, HEX, NO. 2 /AP FOR INDEXES 2 AND 3/	96906	MS35649-224	14	
-4		F	BRACKET, MOUNTING, RESISTOR-TRANSISTOR	90536	7078175-00	1	

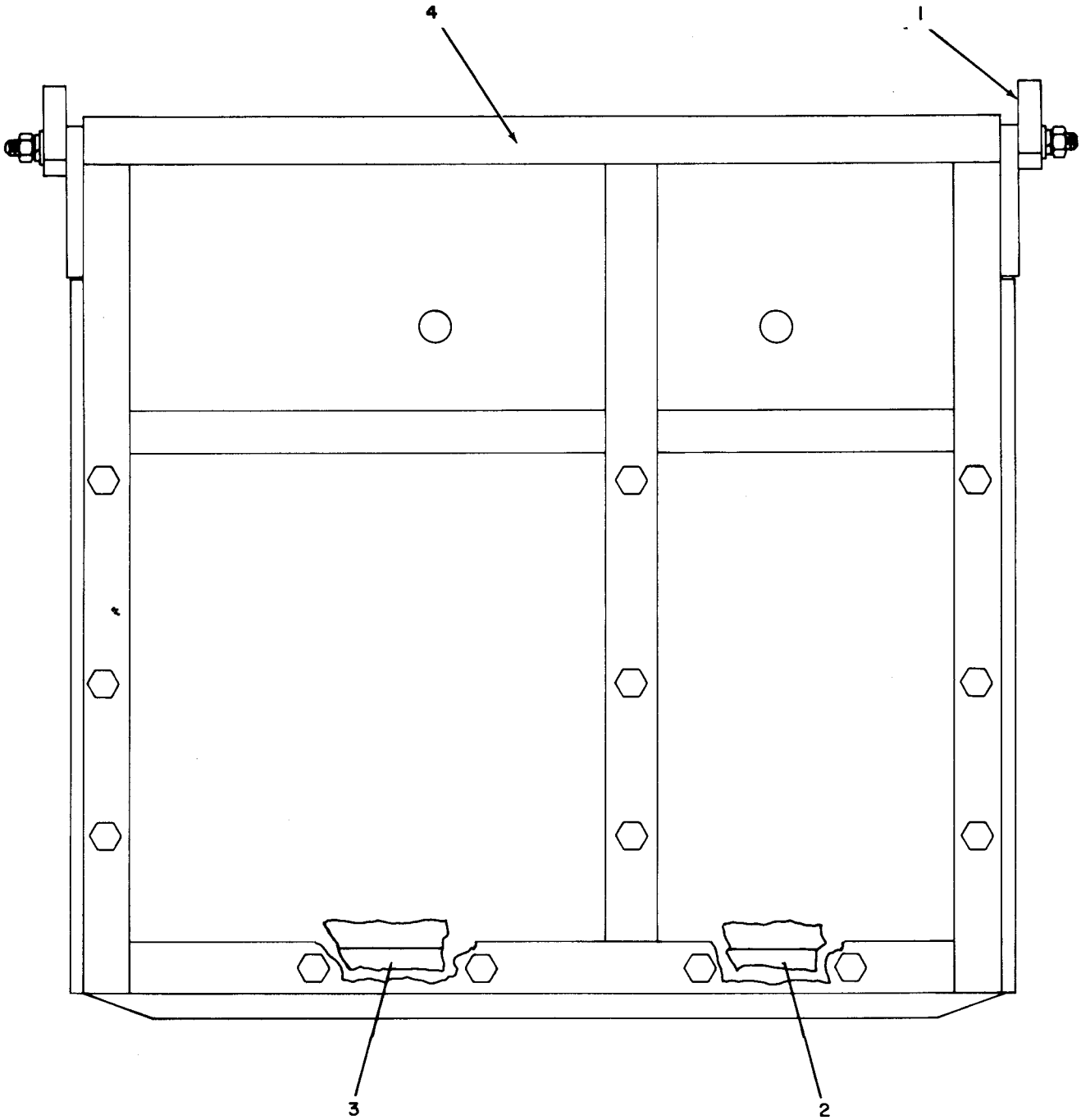


Figure 7-21. Stabilizer Assembly

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
7-21		B	STABILIZER ASSEMBLY /FOR NHA SEE FIG 7-1/	90536	7050267-00	REF	
-1		C	PLATE, STABILIZER	90536	7030450-01	2	
		C	SCREW, CAP, HEX HD, CAD PLATE STEEL, 3/8-16UNC-2A, 2 IN. LG		903090-16 COML	2	
		C	WASHER, LOCK, SPRING, 0.375 IN. /AP/ ID /AP/	96906	MS35332-141	2	
		C	NUT, PLAIN, HEX, FINISHED, 0.375-16UNC-2B /AP/	96906	MS51971-3	2	
-2		C	NUT STRIP	90536	7045244-00	1	
-3		C	NUT STRIP	90536	7045243-00	1	
		C	WASHER, FLAT, 0.375 IN. ID /AP/	96906	MS15795-814	6	
		C	WASHER, LOCK, 0.375 IN. ID /AP/	96906	MS35338-141	6	
		C	SCREW, HEX HD, 3/8-16UNC-2A BY 1.25 IN. LG /AP/	96906	MS35307-362	6	
-4		C	SUPPORT-COVER, CABINET	90536	7034846-00	1	

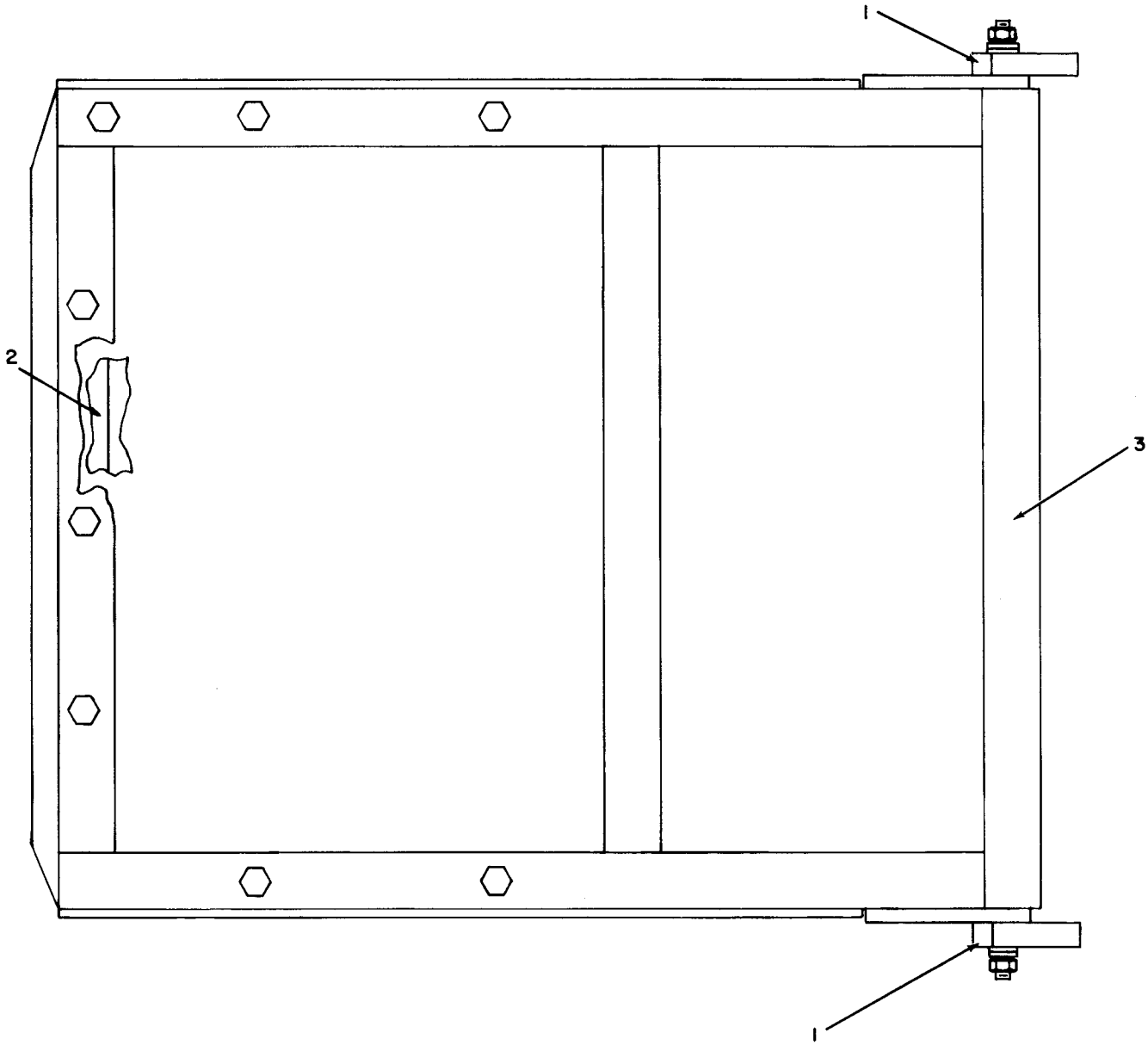


Figure 7-22. Stabilizer Assembly

FIG. & INDEX NO.	REF. DESIG.	INDENT	DESCRIPTION	MFR. CODE	UNIVAC PART NO. MFR. PART NO.	UNITS PER ASSY	USE ON CODE
7-22		B	STABILIZER ASSEMBLY /FOR NHA SEE FIG 7-1/	90536	7050265-00	REF	
-1		C	PLATE STABILIZER	90536	7030450-00	2	
		C	SCREW, CAP, HEX HD, CAD PLATE STEEL, 3/8-16UNC-2A, 2 IN. LG /AP/		903090-16 COML	2	
		C	WASHER, LOCK, SPRING, 0.375 IN. ID /AP/	96906	MS35338-141	2	
		C	NUT, PLAIN, HEX, FINISHED, 0.375-16UNC-2B /AP/	96906	4912541-02	2	
-2		C	NUT STRIP	90536	7045243-00	1	
-3		C	SUPPORT-COVER, CABINET	90536	7034845-00	1	
		C	SCREW, CAP, HEX HD, 3/8-16UNC-2A 1.25 IN. LG /AP/	96906	MS35307-362	4	
		C	WASHER, FLAT, 0.375 IN. ID /AP/	96906	MS15795-814	4	
		C	WASHER, LOCK, SPRING, 0.375 IN. ID /AP/	96906	MS35338-141	4	

PART NUMBER	FIG. & INDEX NO.
A2345-10	8-
A2345-11	9-
C175-0500-5800-A299	7-
CE71C152G	16-3
CE71C223F	18-3
CE71C332G	16-2
CH53B1MF504K	17-
CL25BG251UP3	9-5
CL25BH221UP3	16-1
CL25BH301UP3	18-4
CP09A1KC104K3	4-
D1021A1	3-
D1021A1	11-
D1021A1	14-
DHD894	18-
DPD4500-1388	5-
DPD4500-1388	6-
DRFP,PD3504,277WS	1-
DRFP,PS3504,277WS	1-
E2231-1	17-
F02A250V102AS	18-14
F02A250V12AS	5-
F02A250V12AS	6-
F02A250V1AS	3-17
F02A250V1AS	18-10
F02A250V1/2AS	3-16
F02A250V2AS	16-9
F02A250V4AS	5-
F02A250V4AS	6-
F02A250V5AS	5-
F02A250V5AS	6-
F02A250V5AS	16-12
F02A250V6AS	5-
F02A250V6AS	16-10
F03A125V20AS	3-20
F03A125V20AS	16-11
F03A125V20AS	18-11
F03A250V10AS	5-
F03A250V12AS	4-
F03A250V12AS	5-
F03A250V12AS	16-13
F03A250V15AS	3-19
F03A250V15AS	18-12
F03A250V8AS	3-18
F03A250V8AS	5-
F03A250V8AS	16-8
F03A250V8AS	18-13
FHN26G2	4-
FNH26G2	5-
FNH26G2	6-
FHN26G2	16-27
FHN26G2	18-25
HP4N	18-
HP5N	18-39

PART NUMBER	FIG. & INDEX NO.
HP6N	18-
IND300-9	16-
LC042F7SS	3-
MBS-S1838A9	13-
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MHT7038	16-
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MS3057-12B	1-22
MS3100A20-15P	7-2
MS3102A10SL3P	5-
MS3102A32-6P	16-14
MS3102A32-6PW	16-15
MS3106A32-6S	5-
MS3106A32-6SW	5-
MS3108B10SL3S	5-
MS3108B20-15S	1-24
MS315795-805	11-
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MS35338-141	22-
MS35489-49	18-32
MS35649-224	20-
MS51023-51	2-
MS51959-201	11-
MS51959-29	14-
MS51971-3	21-

PART NUMBER	FIG. & INDEX NO.
MS91528-1K2B	12-5
MS91528-1N2B	13-6
NH10,15.0,1PCT	20-
NH10,5R5,1	10-
NH10,7.5,1PCT	20-
NKS35216-26	1-
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RC07GF102J	18-19
RC07GF104J	16-21
RC07GF151J	9-10
RC07GF221J	8-6
RC07GF471J	4-
RC20GF150J	4-
RC42GF222J	16-22
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RE65N40R2	10-
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1N2806B	18-6
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1N2808B	16-7
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350266-R	16-
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7003760-00	2-50
7003771-00	2-51
7003780-00	2-52
7003850-00	2-53
7004010-00	2-54
7005427-00	16-30
7005428-00	16-34
7005429-00	16-35
7005432-00	16-29
7007865-00	2-7
7007943-03	2-4
7008587-02	16-36
7008890-00	3-4
7008890-00	11-3
7008890-00	14-3
7009000-00	2-55
7009010-00	2-56
7009074-00	16-39
7019230-00	8-8
7019230-01	8-
7019232-00	8-1
7019245-02	5-
7019245-02	6-
7019267-00	16-31
7019269-00	16-33
7019272-00	1-
7019281-00	9-7
7019281-03	9-8
7019283-00	9-
7019284-26	2-
7019284-26	14-
7019284-32	1-10
7019284-32	14-
7019285-00	3-7
7019285-00	11-4
7019285-00	14-4
7019286-00	3-15
7019286-00	11-7
7019286-00	14-7
7019290-00	11-5
7019290-00	14-5
7019292-01	2-
7019296-00	11-
7019297-00	11-9
7019297-00	14-9
7024737-00	1-
7024767-02	14-1
7024767-02	15-
7024774-XX	2-58
7024786-00	9-3
7024790-00	9-1
7024791-00	9-4
7024793-02	2-
7024793-02	9-
7024798-00	2-57
7025359-00	3-6
7025359-00	11-8
7025359-00	14-8
7025360-00	11-6
7025360-00	14-6
7025366-00	11-
7025366-00	14-
7025669-06	1-9
7025669-06	6-
7025682-00	16-38
7025682-00	16-41
7025725-03	14-
7025732-00	1-12
7030413-00	16-42
7030413-01	16-43
7030414-00	16-44
7030416-00	16-45
7030417-00	16-46
7030450-00	22-1
7030450-01	21-1
7033086-00	3-5
7033221-01	1-6
7033221-01	17-

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7033255-00	7-3
7033257-00	1-21
7033257-00	7-
7033262-00	1-11
7033263-00	5-
7033264-00	5-
7033264-00	6-
7033949-00	11-2
7033949-01	11-
7033949-01	14-2
7034820-01	1-
7034821-01	1-3
7034845-00	22-3
7034846-00	21-4
7034859-00	9-13
7034859-00	10-
7038852-00	16-32
7038864-02	1-25
7038864-02	16-
7045233-01	1-
7045243-00	21-3
7045243-00	22-2
7045244-00	21-2
7049747-00	1-
7049747-01	1-
7049747-02	1-
7049747-03	1-
7049747-04	1-
7049747-05	1-
7049747-06	1-
7049747-07	1-
7049747-08	1-
7049747-09	1-
7049747-10	1-
7049747-11	1-
7050014-01	19-6
7050015-00	19-7
7050264-00	1-
7050265-00	1-
7050265-00	22-
7050267-00	1-31
7050267-00	21-
7050279-00	5-
7050281-00	5-
7050302-00	1-
7050303-00	3-8
7050304-00	1-14
7050305-00	1-13
7050307-01	1-5
7050307-01	4-
7051213-00	1-
7051213-01	1-
7051213-02	1-
7051213-03	1-
7051228-00	1-
7051229-00	1-
7051229-01	1-
7051229-02	1-

PART NUMBER	FIG. & INDEX NO.
7053750-00	1-3
7053750-00	3-
7053750-01	1-
7053750-01	3-
7053750-02	1-
7053750-02	3-
7053750-03	1-
7053750-03	3-
7053750-04	1-
7053752-00	3-2
7053752-00	18-
7053753-00	18-43
7053755-00	18-1
7053755-00	19-
7053758-00	18-22
7053763-00	18-26
7053764-00	18-27
7053765-00	18-28
7053766-00	18-29
7053767-00	18-30
7053769-00	18-31
7053772-00	18-34
7053772-01	18-35
7053777-00	18-37
7053783-02	11-
7053783-02	12-
7053783-03	11-1
7053783-03	12-
7053785-00	1-
7053785-01	1-
7053793-02	2-
7053793-02	11-
7053793-03	2-3
7053793-03	11-
7053793-04	2-
7053793-04	11-
7053794-00	2-1
7053794-00	8-
7053794-01	2-2
7053794-01	8-
7053794-02	2-
7053794-02	8-
7053794-03	2-
7053794-03	8-
7053794-04	2-
7053794-04	8-
7053795-00	1-7
7053795-00	2-
7053795-01	1-1
7053795-01	2-
7053795-02	1-2
7053795-02	2-
7053795-03	1-4
7053795-03	2-
7053795-04	1-
7053795-04	2-
7053795-05	1-
7053795-05	2-

PART NUMBER	FIG. & INDEX NO.
7053798-01	11-
7053798-01	13-
7053799-00	1-8
7053799-00	5-
7067427-00	19-5
7067439-05	3-
7067439-05	3-35
7074820-00	18-23
7074821-00	18-
7074822-00	18-40
7078035-04	19-2
7078035-05	19-3
7078161-00	5-
7078175-00	20-4
7078176-00	18-2
7078176-00	20-
7078177-00	18-36
7078245-00	18-33
7084898-00	3-9
7085700-00	3-1
7085700-00	18-
7085701-00	3-3
7085702-00	18-
7085705-00	3-10
7085706-00	3-13
7085707-00	3-14
7085708-00	3-12
7500040-00	3-21
7500260-00	3-22
7500280-00	3-23
7500320-00	3-24
7500340-00	3-32
7500400-00	3-25
7500421-00	3-27
7500431-00	3-28
7500650-00	3-26
7500660-00	3-31
7500671-00	3-33
7500761-00	3-30
7500781-00	3-29
7500900-00	3-34
7900082-01	2-5
7900092-00	10-
7900092-04	8-5
7900092-04	9-9
7900149-00	2-10
7900149-00	18-24
7900215-00	15-5
7900241-01	8-7
7900251-01	8-2
7900251-01	9-2
7900382-00	18-16
7900496-23	12-3
7900496-23	13-7
7900496-23	15-3
7900497-17	20-3
7900497-99	20-2
7900608-00	7-1

PART NUMBER	FIG. & INDEX NO.
7900635-01	4-
7900635-01	13-2
7900635-02	4-
7900635-02	13-3
7900677-00	4-
7900678-00	4-
7900678-01	4-
7900678-02	4-
7900678-03	4-
7900755-00	20-1
7900755-00	16-19
7900756-00	16-20
7900790-00	1-15
7900790-00	1-17
7900790-01	1-16
7900790-01	1-18
7900836-00	3-
7900836-00	11-
7900836-00	14-
7900841-00	8-4
7900841-00	9-12
7900842-00	5-
7900842-00	6-
7900843-00	8-3
7900843-00	9-11
7900874-00	4-
7900880-00	12-4
7900880-00	15-4
7900906-01	3-
7900906-01	3-11
7900912-13	7-4
7900987-00	13-1
7900987-00	15-2
7901046-00	14-10
7901056-00	16-40
7901056-01	16-37
7901103-00	16-25
7901126-00	18-9
7901279-00	1-28
7901287-00	17-
7901311-00	1-29
7902032-01	2-6
7902045-00	18-Q1
7902206-00	18-15
7902239-01	19-1
7902306-04	10-
7902557-00	18-20
7902716-02	1-26
7902716-03	1-27
8038-163	2-
8038-163	18-
812FF	2-
85-0410-0111-203	4-
908542-05	1-
908672-09	16-28
908-1166-1633-526	12-
908-1166-1633-526	13-
908-1166-1633-526	15-
920-1113-1631-522	15-

PART NUMBER	FIG. & INDEX NO.

PART NUMBER	FIG. & INDEX NO.

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SECTION 8

SYMBOLOGY

8-1. GENERAL.

The information provided in the following paragraphs is a guide to the functional schematic diagrams supplied with the computer. Major areas covered in this portion of the manual are fundamental logical design ground rules, standard symbology used to represent logic elements in the diagrams and computer, reference designators that appear on the drawings and in the text material, special symbology, and physical and functional descriptions of the printed-circuit cards used in the computer.

The design of the computer is based on the negative logic concept. By convention, 0.0 volts represents a high and -4.5 volts represents a low.

8-2. CIRCUIT SYMBOLOGY.

The main symbols used on the functional schematic diagrams to represent the electrical circuits and logic elements that constitute the computer's internal hardware are shown in figures 8-1 through 8-3.

The following paragraphs provide a brief description of the more common logic elements used in the computer and the symbols used to represent them on the functional schematics. The symbology used parallels that of MIL STD 806B. Detailed functional descriptions of all the circuits are provided in paragraph 8-7. Examples of the logic cards are shown in parantheses.

a. INVERTER. - The basic inverter (2070) is a single-input inverting amplifier. It operates with nominal static voltages of 0.0 volts and -4.5 volts. The circuit provides a low output for a high input, and a high output for a low input. The inverter is represented symbolically as shown in figure 8-1a.

b. AND INVERTERS. - The AND inverters (2030) are inverting amplifiers with internal diode AND inputs. The number of inputs to each circuit is dependent upon the card type. The AND inverters operate with nominal static voltages of 0.0 volts and -4.5 volts. Each circuit provides a high output when all its inputs are low, and a low output when any one or all its inputs are highs.

c. AND-OR INVERTERS. - The AND-OR inverters (2040) are variations of the AND inverters and, like their counterparts, operate with nominal static voltages of 0.0 volts and -4.5 volts. The AND-OR inverter produces a high output when all inputs to any one of the AND circuit (squares) are lows. Conversely, the circuit produces a low output when a high is present on one or more inputs to each AND circuit.

d. OR INVERTER. - The OR inverter (2220) is similar to the AND-OR inverters in that it is an inverting amplifier that performs an OR function and operates with nominal static voltages of 0.0 volts and -4.5 volts. The circuit produces a low output only when all its inputs are highs, and a high output when any one input is a low.

e. FLIP-FLOPS. - The flip-flops (2000) are combinations of two internally-interconnected inverters. The circuit may consist of either two AND-OR inverters, or one inverter and one AND inverter.

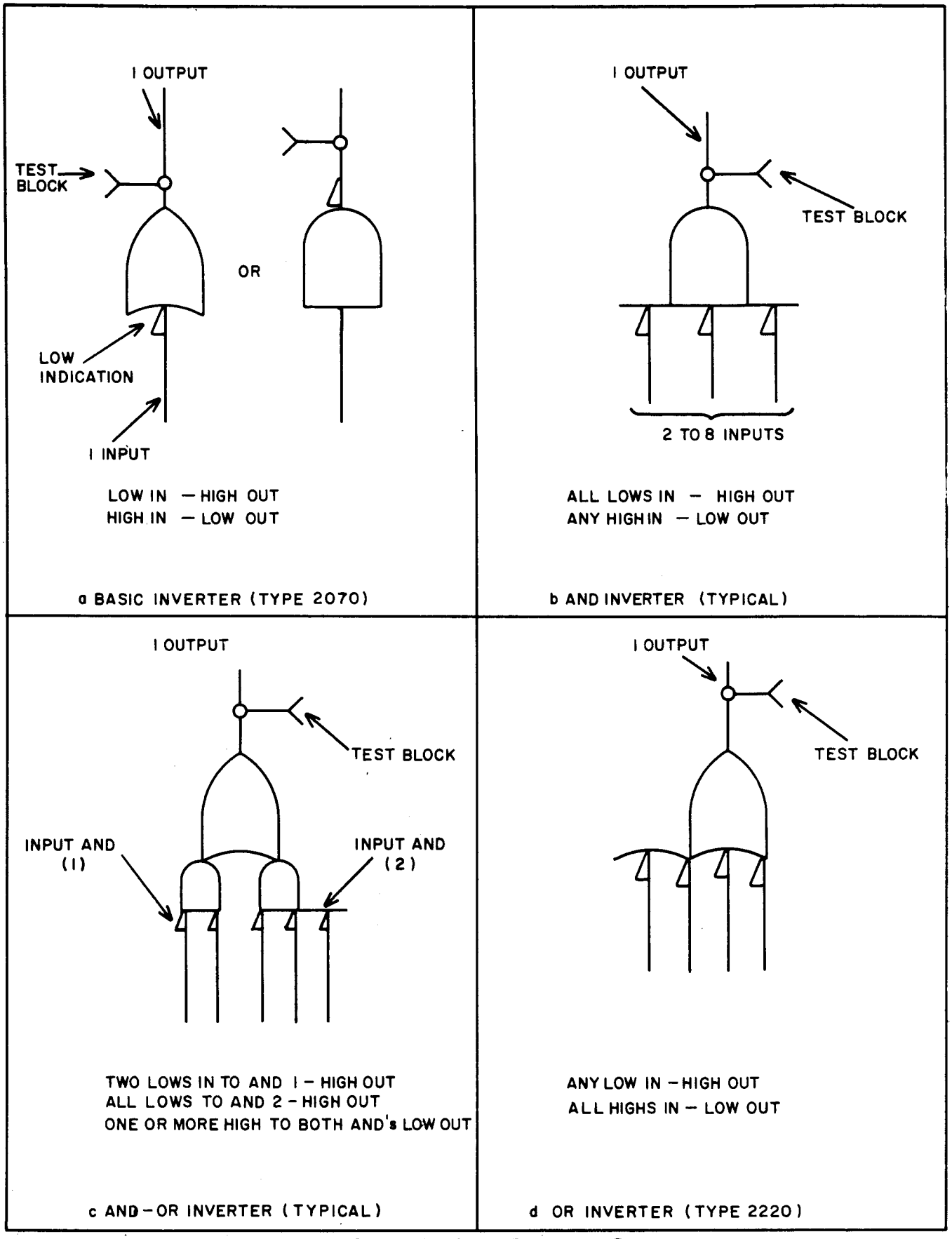


Figure 8-1. Typical Inverter Symbols

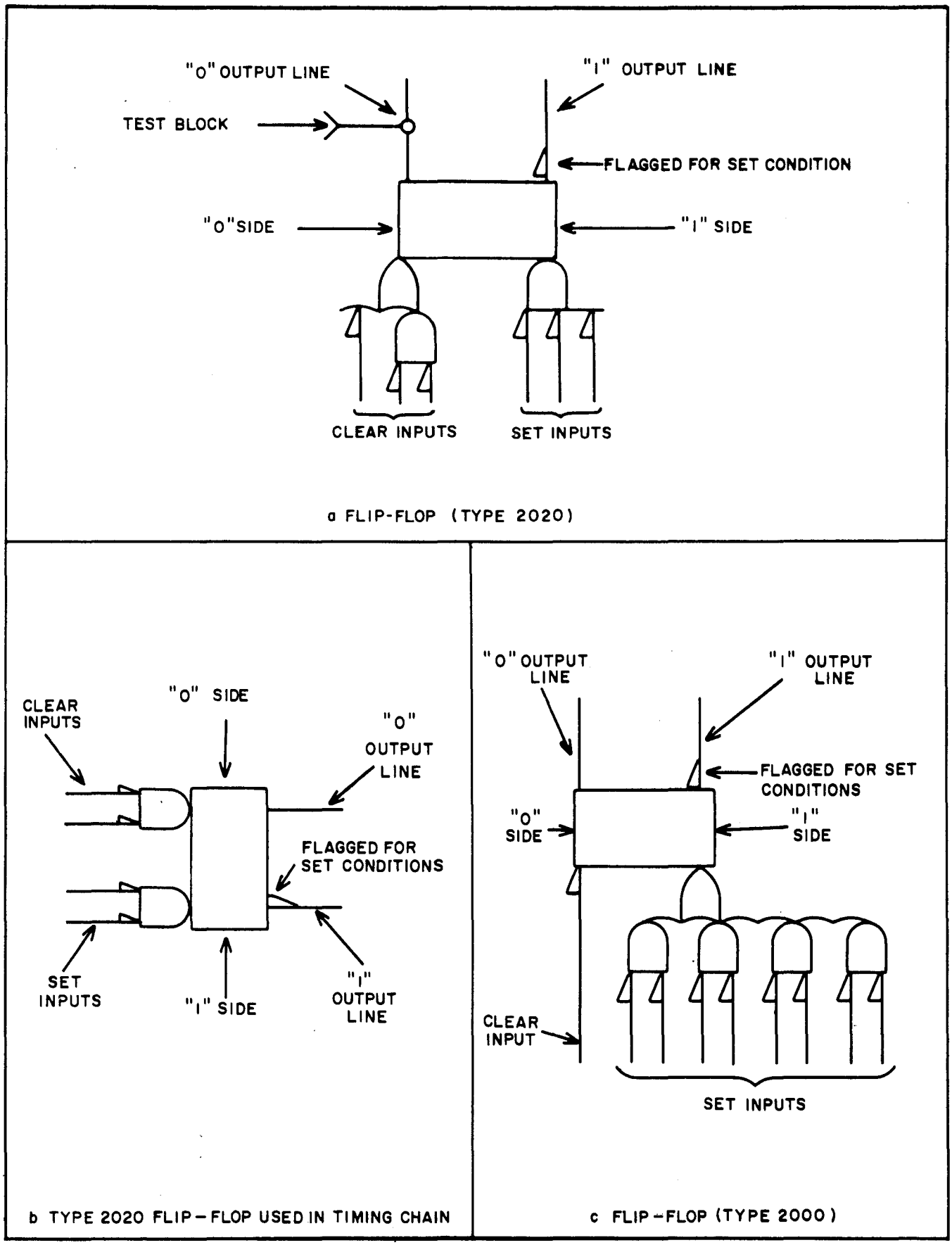


Figure 8-2. Typical Flip-Flop Symbols

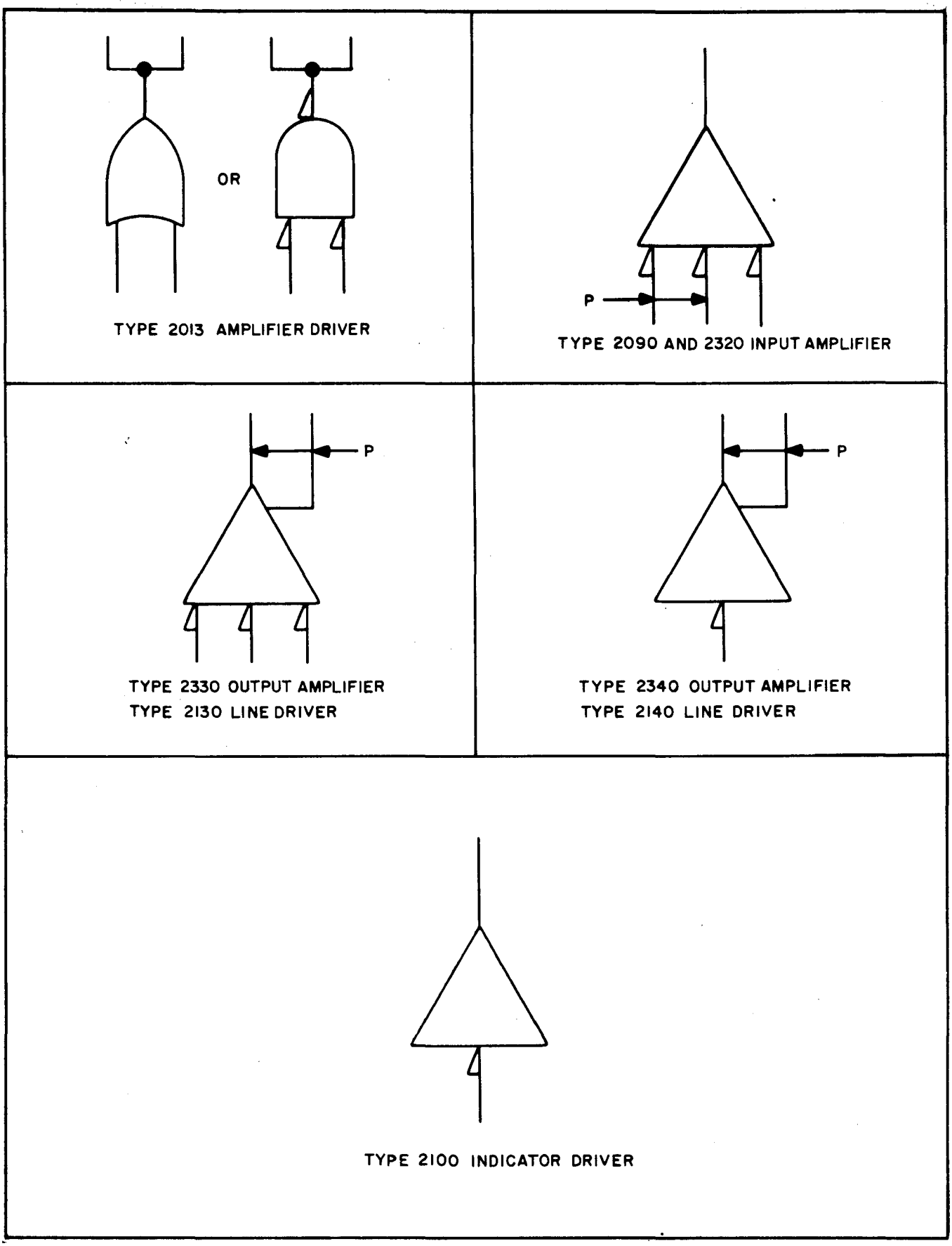


Figure 8-3. Typical Amplifier and Driver Symbols

The flip-flops are represented on the functional schematics by a rectangle as shown in figure 8-2. The rectangle may be drawn on either a horizontal or vertical plane, depending upon the function performed by the particular flip-flop.

A flip-flop has two stable states; the set state and the cleared state. The circuit is in the clear state when the output from the "1" side is a high and the output from the "0" side is a low. The circuit is in the set state when the output from the "1" side is a low and the output from the "0" side is a high. The flip-flop shown in figure 8-2a is set by simultaneously applying lows to all AND circuit inputs on the "1" side, and cleared by simultaneously applying lows to all AND circuit inputs on the "0" side. The outputs of all flip-flops are flagged showing the set condition.

In addition to setting and clearing a flip-flop by means of its input lines, a flip-flop can be set and cleared by applying the proper logic level to its set or clear output line. For example, a flip-flop can be forced to the set state by applying a low to the "1" output line. Conversely, a flip-flop can be forced to the cleared state by applying a low to the "0" output line.

f. AMPLIFIER DRIVER. - The amplifier driver (2013) is a double-inversion power amplifier used primarily for distributing clock and logic signals. The circuit operates with nominal static voltages of 0.0 volts and -4.5 volts and provides a low output only when all inputs to the circuit are lows. At all other times, the circuit provides a high output. Where it is applicable and practical, the amplifier driver circuits are assigned a unique logic notation to identify the cycle and phase of the signal being transmitted.

The amplifier driver is represented symbolically as shown in figure 8-3. Three common output pins each are capable of driving a number of logic circuits.

g. INPUT AMPLIFIERS. - The input amplifiers (2090) are used to amplify and invert the voltage levels of data and control signals received from externally located peripheral devices. Essentially, the circuits convert the externally generated signals to logic levels (0.0 and -4.5 volts) that are intelligible to the computer's internal circuits.

The input amplifiers are represented symbolically on the functional schematics by a triangle with three inputs and one output as shown in figure 8-3.

h. OUTPUT AMPLIFIERS AND LINE DRIVERS. - The output amplifiers and line drivers (2140) are inverting amplifiers used for the interface between the computer and input-output equipment. Essentially, the circuits convert computer-generated data and control signals to voltage levels (-3 and -15 volts) that are intelligible to the external peripheral devices.

The output amplifiers and line drivers are represented symbolically by triangles as shown in figure 8-3. For a description of these circuits, refer to paragraph 8-6.

i. INDICATOR DRIVER. - The indicator driver (2100) is a dual-purpose inverting amplifier driver. It is used as a relay puller to control certain relays on the power control panel and as a driver for the PROGRAM STOP indicators on control panel number 2. The driver produces a zero-volt output for a low input, and presents an apparent open circuit to the relay or indicator for a high input.

The circuit is represented symbolically on the functional schematics by a triangle with one input and one output as shown in figure 8-3.

8-3. REFERENCE DESIGNATORS.

Reference designators used on the functional schematic diagrams include unique designators, connector and jack location information, circuit card type identification, and special symbology. In addition, each schematic diagram contains such information as signal source and destination information, signal names, and page references.

a. UNIQUE DESIGNATORS. - Unique designators are combinations of alphabetic characters and numerical superscripts used to identify uniquely each logic element and associated circuit in the computer system.

The alphanumeric representation is in the form of "abXcd" as shown in figure 8-4. In the notation, "X" (a letter) generally identifies a specific logic section, designator, or register. The "abcd" (numbers) indicates the level or rank of a circuit and/or its usage; for example, the state of a register, the rank of a particular logic element, the "0" and "1" sides of a flip-flop, and in some cases, clock cycle and phase times.

(1) ALPHA ASSIGNMENTS. - The alphabetic portion of the logic notation X is generally derived from the following alpha assignment list.

A - Arithmetic Register (Accumulator) and Adder
B - BU Register
C - Input/Output (Communications) Registers
D - Arithmetic Register
E - Control
F - Function Register and Translator
G - Control
I - Input Logic and Registers
J - Manual Control
K - Counters, K Register
L - Secondary Timing Chains
M - Memory
N - Command Enables
P - Program Address Register
Q - Unassigned
R - Unassigned
S - Memory Address Register
T - Main Timing Chain
V - Input/Output Logic
W - Input/Output Control
X - Exchange Register
Y - Non-Standard Circuits
Z - Memory Data Register

(2) NUMERIC ASSIGNMENTS. - When the logic element is a flip-flop, the "b" portion of the logic notation "abXcd" may be either a 0 or 1 (figure 8-4) depending upon the side of the flip-flop to be referenced and is written on the schematic as an X. The 01 designates the set or "1" side of the flip-flop; the 00 designates the clear or "0" side of the flip-flop. In the case of a register or counter, the "cd" portion of the logic notation identifies individual bit positions or stages of the register or counter. For example, a register or counter normally has its stages numbered from right to left in descending order (2^n . . . 2^{03}, 2^{02}, 2^{01}, 2^{00}) with individual bit positions specified as a power of two. The "cd" portion,

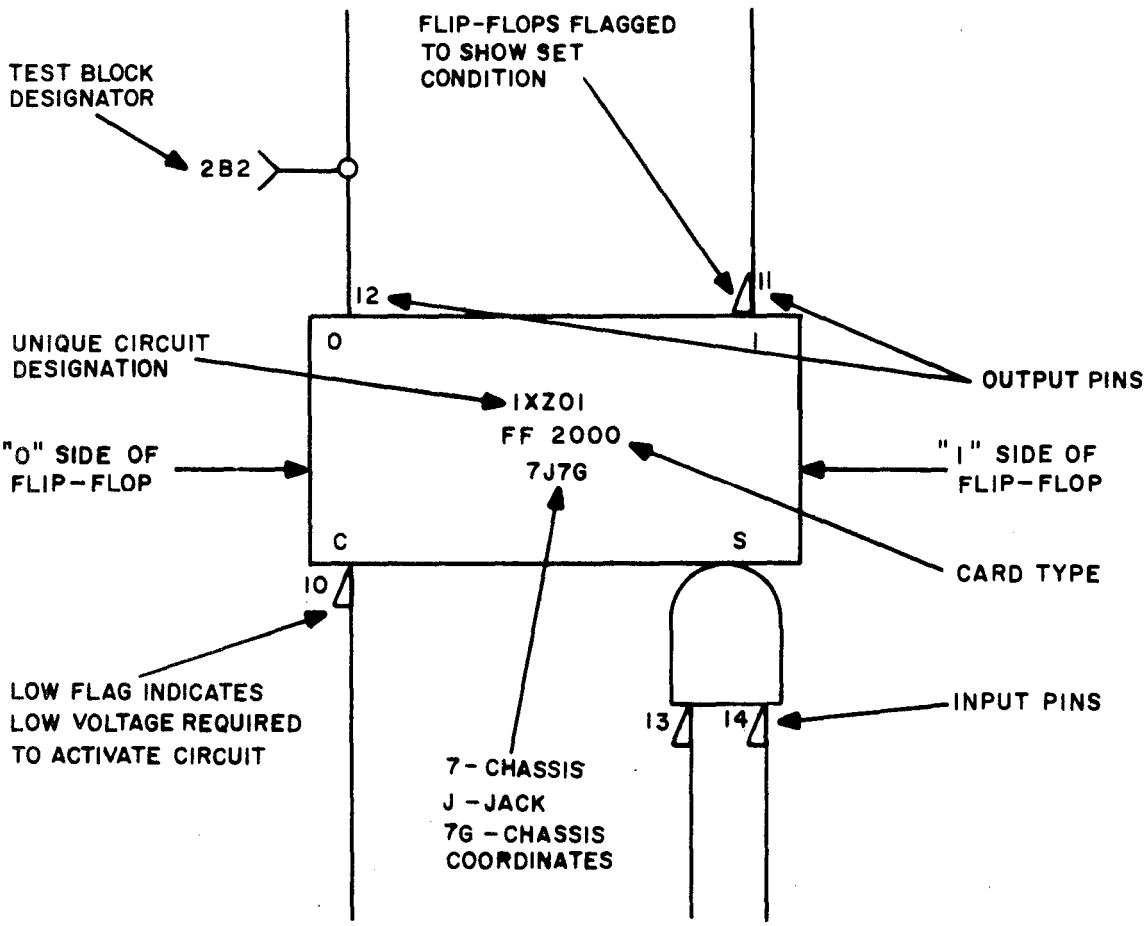


Figure 8-4. Examples of Logic Notations

therefore, would be .....03, 02, 01, 00. In the case of a double ranked register or counter, the "c" digit in the second rank is assigned arbitrarily (6, 7, or 8, for example), leaving a sufficient gap between the "c" numbers of the two ranks to allow for notating intermediate logic elements. If the numerics assigned the primary rank are as follows (considering only the 01 side of each flip-flop in the register):

$$01_X0n \ldots 01_X03,\ 01_X02,\ 01_X01,\ 01_X00,$$

the numeric assignments for the second rank would be:

$$01_X4n \ldots 01_X43,\ 01_X42,\ 01_X41,\ 01_X40.$$

The arbitrary assignment of 4 as the value for "c" in the secondary rank allows a sufficient gap between the two ranks for designating associated logic elements.

On functional schematics depicting more than one circuit, a "g" is used in place of a number in either the "ab" or "cd" position of the unique term. This "g" represents a different numerical value for each of the duplicated circuits and is usually defined in a note on the drawing.

b. CARD LOCATION DESIGNATORS. - A card location designator specifies the location of a card in the computer by chassis number and chassis coordinates. As shown below, the first digit in the designator identifies the chassis number. For duplicate circuits, the chassis number may be shown as "g". The "J" identifies the connector as a circuit card jack. The remainder of the designator identifies the coordinate location of the card connector on the specified chassis.

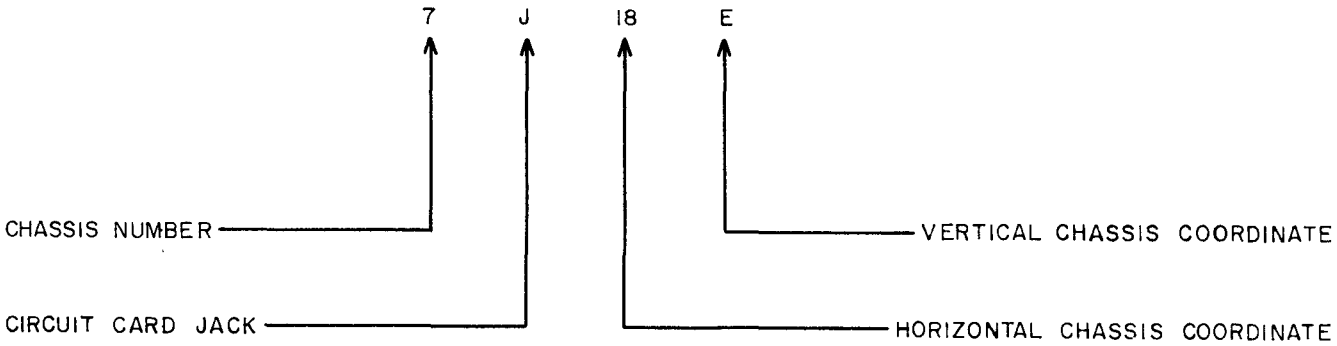


Figure 8-5 identifies the various chassis by chassis number in the computer. Figures 9-181 through 9-187 are illustrations showing the arrangement of the circuit card connectors on the various chassis (refer to Volume II).

c. TEST BLOCK DESIGNATORS. - A test block designator specifies a test block terminal by test block number and pin number (in terms of its coordinates on the test block) as shown. However, the designator does not specify the panel or chassis number of the test block. To determine on which chassis the test block is located, refer to the first digit of the card location designator of the circuit associated with the test block in question.

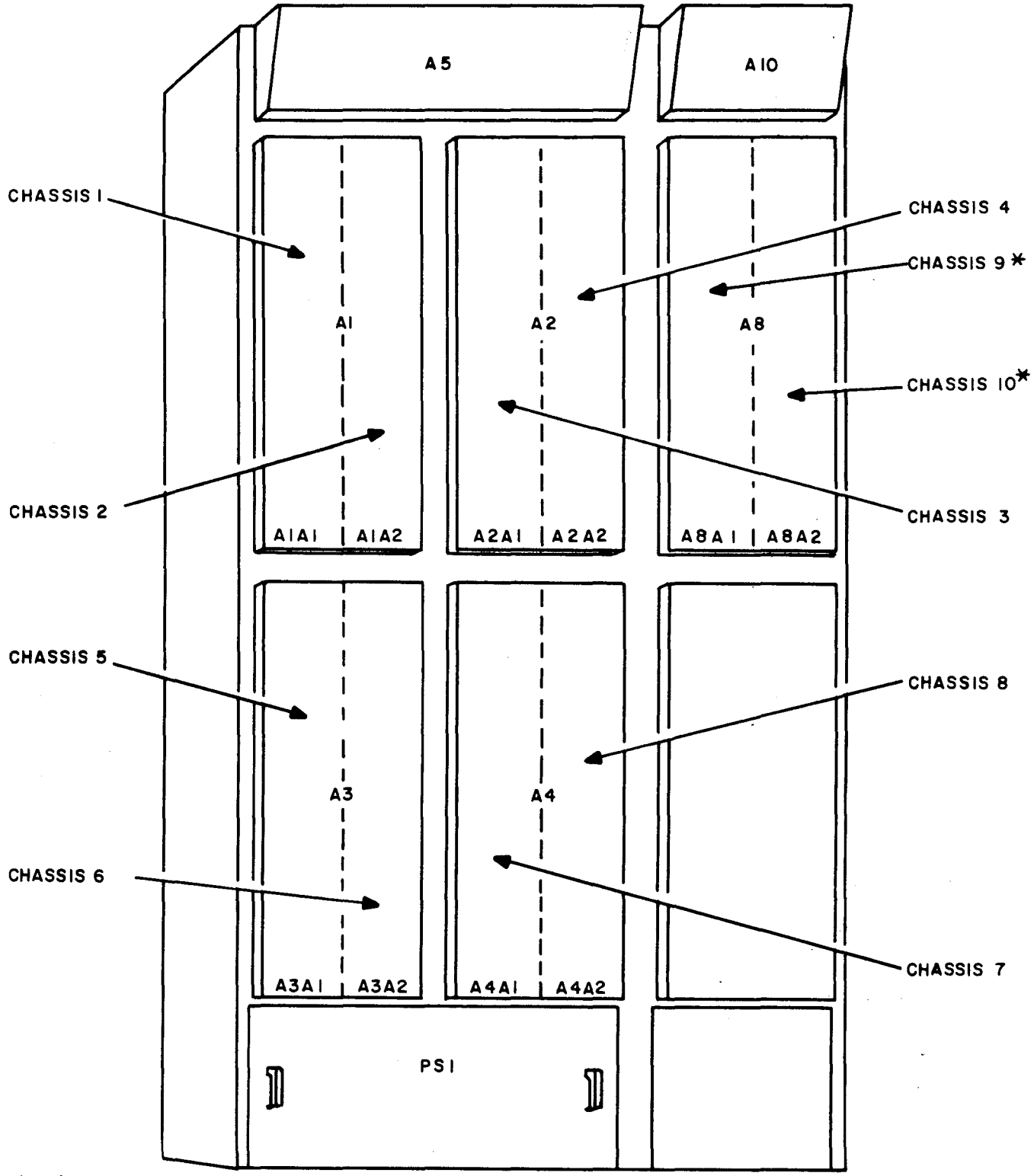
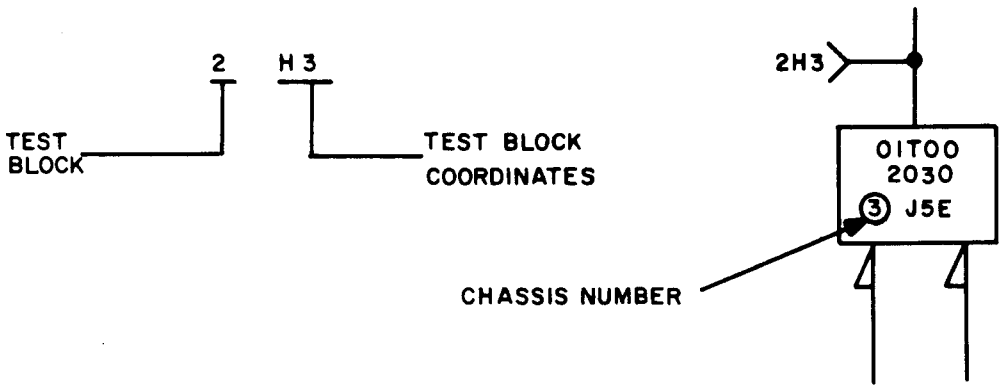
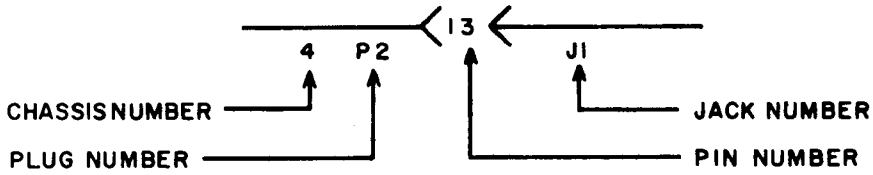


Figure 8-5. Drawer and Chassis Locations



d. CONNECTOR DESIGNATORS. - Each connector in the computer is assigned a unique reference designation consisting of a chassis identifier, plug and jack identifier, and pin number as shown in the following illustration.

The permanent part of the connector is referred to as the jack and is identified by a "J". The movable part of the connector is referred to as the plug and is identified by a "P". Note in the following illustration that no chassis number is assigned to the jack; it is always the same as the plug.



8-4. SPECIAL SYMBOLOGY.

When practical, input and output lines to and from logic elements are identified by signal names or special symbology to name the signal transmitted and/or to define a logical event. In addition to the signal or special symbol that appears above the signal line, the following information is provided to aid in signal tracing and maintenance.

1) Logic designation of the circuit generating the signal (source of input signals) or the circuit receiving the signal (destination of output signals).

2) Figure number of the source or destination circuit.

Figures 8-6 and 8-7 show examples of these designators as well as other special symbols.

8-5. CHASSIS MAPS.

The chassis maps show the physical layout of the card chassis, the location and type number of each circuit card used on the chassis, the number of circuits available on each card, logic notations for those circuits that are used, spare circuits on each card, and spare connectors on the chassis. Chassis maps for the computer

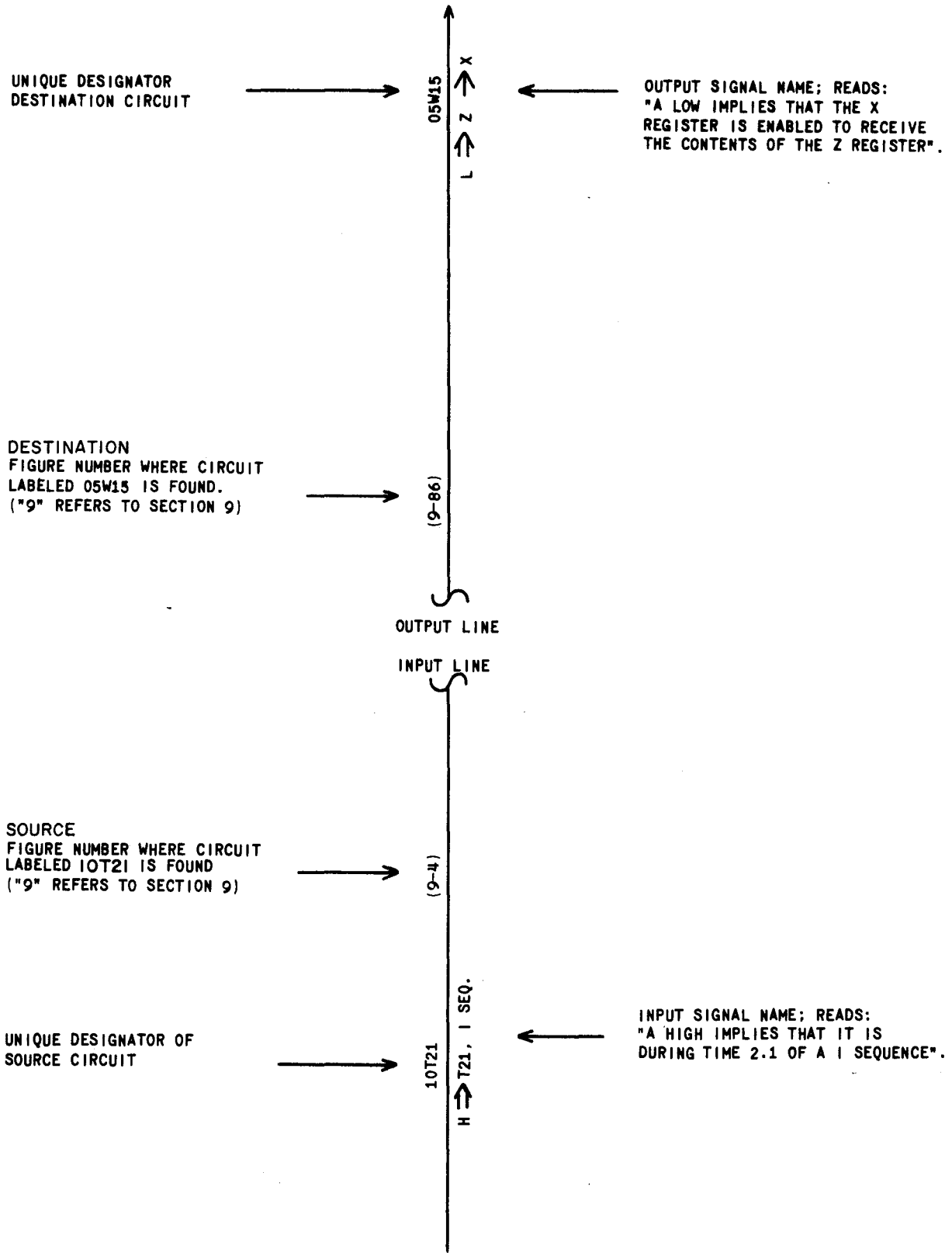


Figure 8-6. Signal Line Symbology

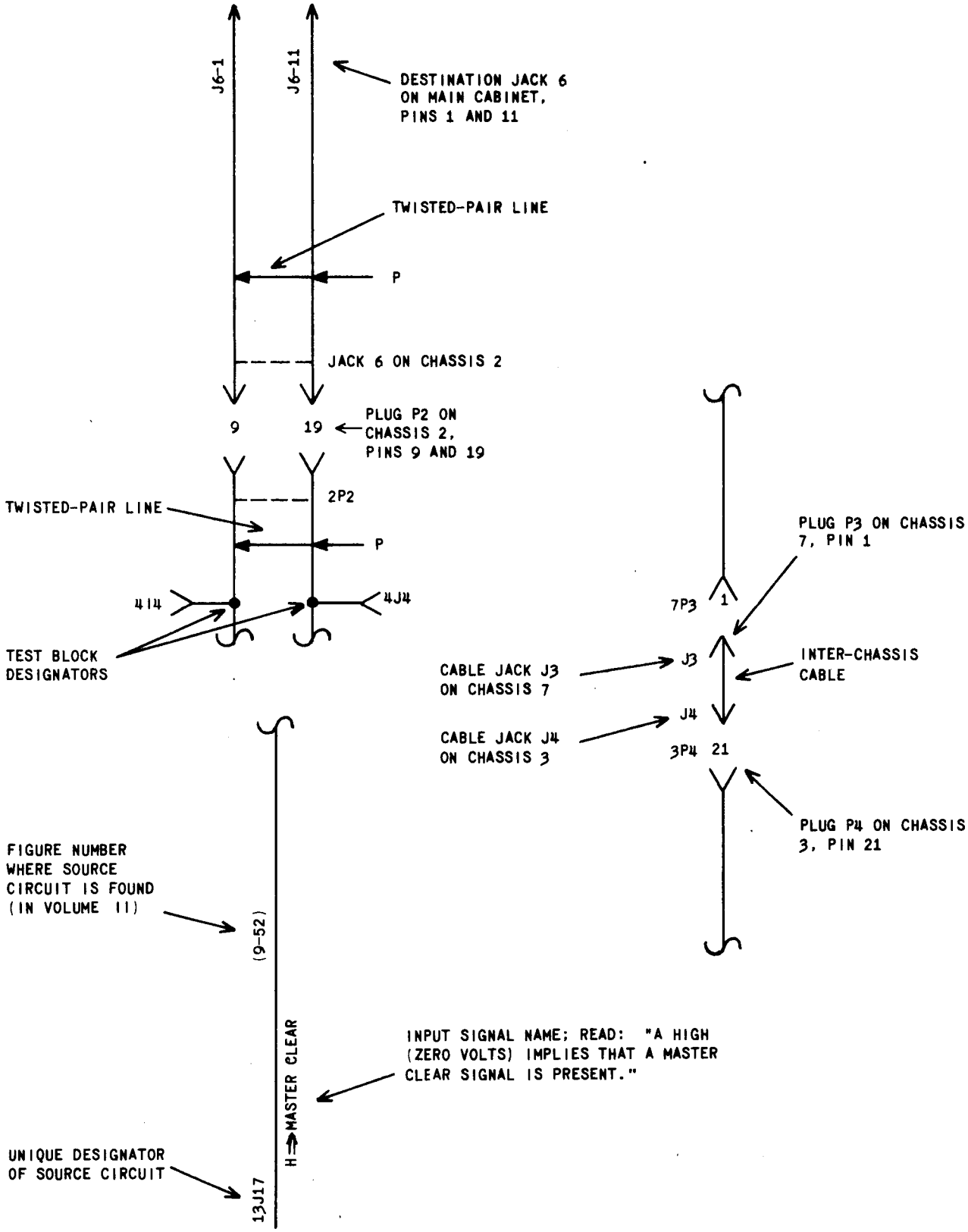


Figure 8-7. Special Symbology

are included with the functional schematic diagrams in Volume II (refer to figures 9-181 through 9-187). A simplified chassis map is shown on figure 8-8. As can be seen on the illustration, each chassis (except the memory chassis) contains 210 card connectors. Individual connectors are arranged on the chassis in seven rows; columns are numbered from left to right, 1 through 35.

The following discussion pertains to individual cards on the sample chassis map shown in figure 8-8.

Location A1 — Contains type 2070 card. The card contains five circuits. Only the first four circuits are used. The first circuit is labeled 02S10 on the functional schematics; the fourth circuit, 03S11. The dashes shown in the area reserved for the fifth logic notation indicate this circuit is a spare. The numbers 6 and 8 indicate that the circuits identified are found in figures 9-6 and 9-8. The 1-1-1-1-1 shows that each circuit has one input.

Location G35 — Contains type 2930 card. The card contains two flip-flop (FF) circuits.

Location F35 — A usable spare location.

Location F34 — A nonusuable spare location.

8-6. PHYSICAL DESCRIPTION OF PRINTED-CIRCUIT CARDS.

Generally, two types of printed circuit cards are used to supply the logic circuitry within the computer. The two types differ in the number of contact connections and circuit content. Type A contains from one to five circuits, with few exceptions, and terminates in a 15-pin connector. Type B contains from 1 to 16 circuits and terminates in a 56-pin connector. The type B cards are used in memory logic and control to minimize space and provide maximum memory storage capability.

Card-type numbers listed in the functional schematics are the last four digits of the actual part number. For the complete number, refer to tables 1-1 and 1-17.

Each card is color coded, using the standard resistor color coding scheme according to the last four digits as shown in the functional schematics of section 9. The 2013 card (7002013) is color coded red, black, brown, and orange and is an example of the coding system.

The least significant digit in the card type number indicates the revision of the basic card. As an example, card type 7002013 indicates the third revision of the basic 7002010 card. Any card with a higher revision number can replace a card with a lower revision number; however, the lower revision card cannot be used as a substitue for the higher revision card. The card type numbers, functional schematics of section 9 and card descriptions which follow will not be updated if a new revision of a card is released; since the new revision will replace the older card.

8-7. FUNCTIONAL DESCRIPTION OF PRINTED-CIRCUIT CARDS.

a. TYPE A PRINTED CIRCUIT MODULES. - Figures 8-9 through 8-55 describe the type A printed-circuit cards used in the computer. The descriptions are functional because they describe each circuit in terms of inputs and outputs rather than internal electronic operation.

Whenever possible, inputs and outputs are defined as lows or highs. In the computer, a low always implies a potential of -4.5 volts, and high always implies ground potential of 0.0 volts.

The following information is contained in the card descriptions:

1) Card name and card type number.

2) Symbol used to represent the card on the functional schematics.

3) A logic description and a design description when applicable.

b. TYPE B PRINTED CIRCUIT MODULES. - Figures 8-56 through 8-79 describe the type B printed-circuit cards.

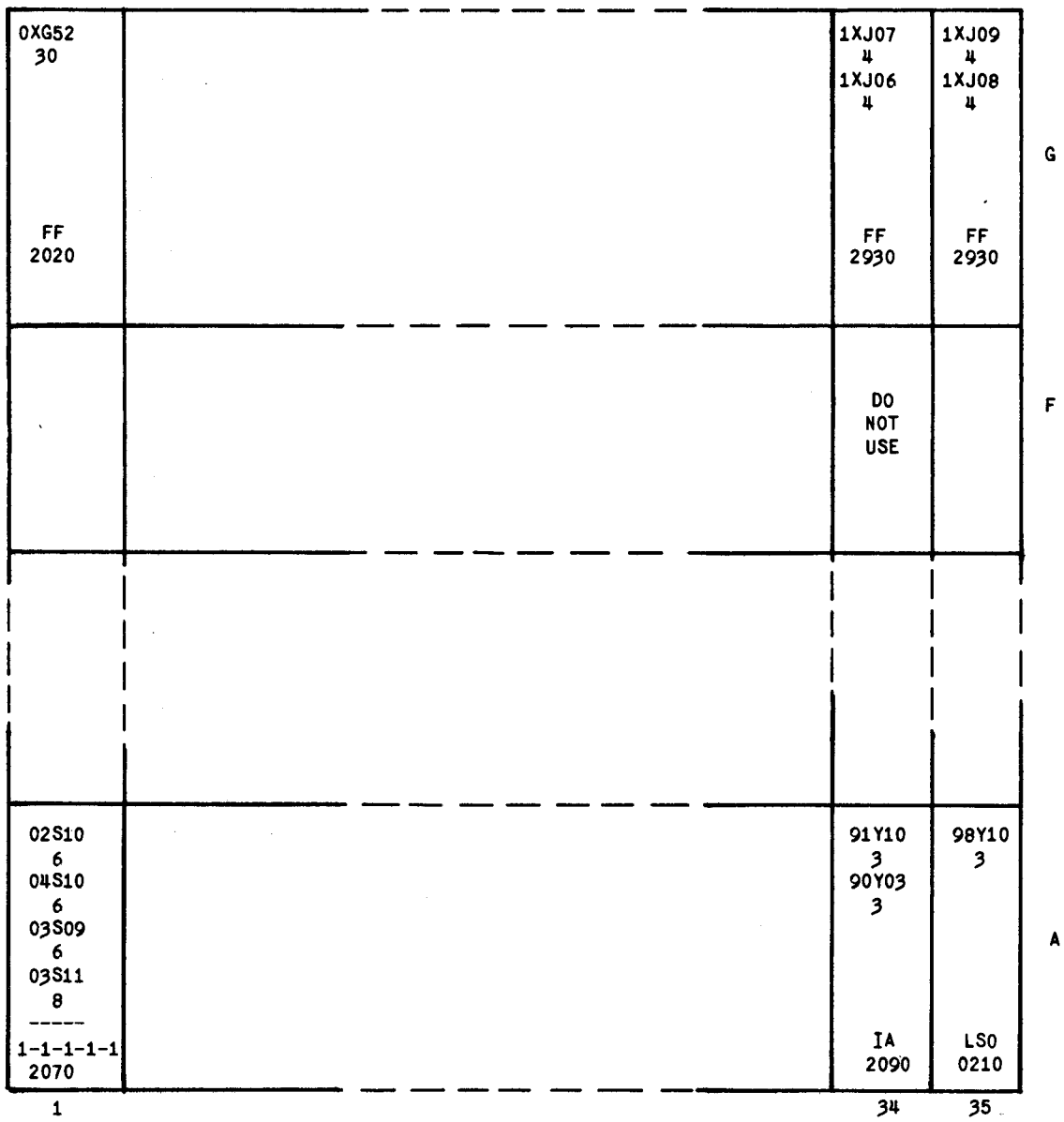
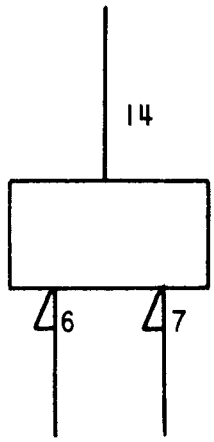


Figure 8-8. Sample Chassis Map



LOGIC SYMBOL

LOGIC DESCRIPTION

The output from this oscillator circuit is a square wave. The frequency of this output is normally controlled by the addition of an external potentiometer between pins 6 and 7. With this addition, the pulse rate may be varied between 2 and 200 cycles per second.

The amplitude of the output signal is from 0.0 volts to -15.0 volts.

This circuit is used to supply substitute timing pulses for maintenance and test purposes.

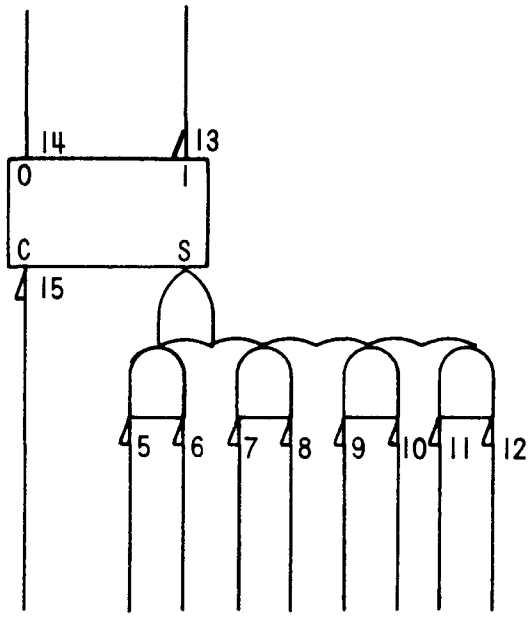
ELECTRICAL DESCRIPTION

The output from pin 14 is connected to the input of a 7002090 module with the ground return connected to pin 1.

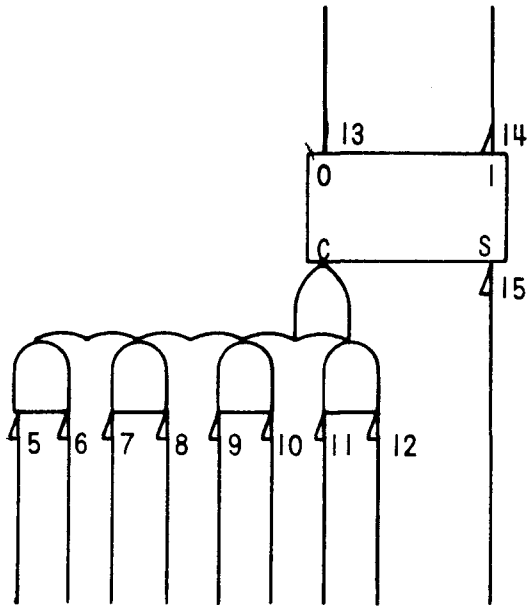
LOGIC			
INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-15.0 Volts	LOW	-15.0 Volts

POWER REQUIREMENTS				
PIN	1	2	3	4
VOLTAGE	Grd	-	-15.0	-
MW	-	-	200	-

Figure 8-9. Pulse-Delay Oscillator, Card Type 7000210



(a)



(b)

LOGIC SYMBOLS

LOGIC DESCRIPTION

A low input signal to pin 15, drawing (a), will clear the flip-flop with a resultant low signal at pin 14 and a high at pin 13.

When both inputs to any one AND circuit on the set side of the flip-flop are low, the flip-flop will be set to produce a low signal output at pin 13 and a high at pin 14.

Drawing (b) shows a reversal of drawing (a) with a multiple clear function and a single set function.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive voltage excursions of -0.3 volt and nominal negative voltage excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

The maximum input current required is 7.1 milliamperes.

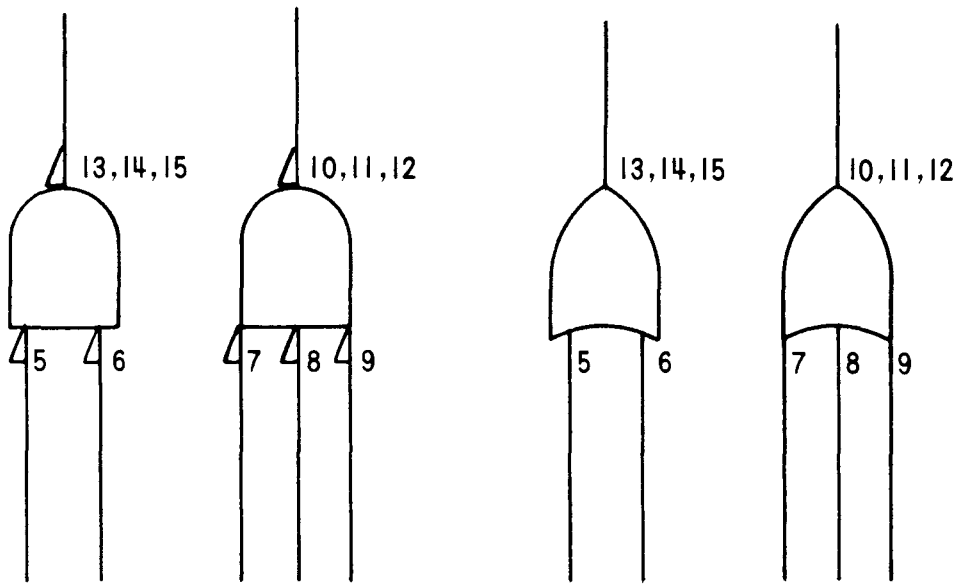
The circuit can drive one indicator driver plus either four AND/OR or AND gates.

The speed of the circuit is such that the second stage of two series-connected circuits will produce a usable output before the termination of a clock-phase input signal to the first stage. The duration of the normal clock-phase pulse is 125 nanoseconds.

LOGIC			
INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS				
PIN	1	2	3	4
VOLTAGE	Grd	+15.0	-15.0	-4.5
MW	-	64	656	43

Figure 8-10. Flip-Flop, Card Type 7002000



LOGIC SYMBOLS

LOGIC DESCRIPTION

If the input signal to any one pin of a logic element is high, the output from that element will be high.

If all of the inputs to a logic element are low, the output from that element will be low.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive voltage excursions of -0.0 volts and nominal negative voltage excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

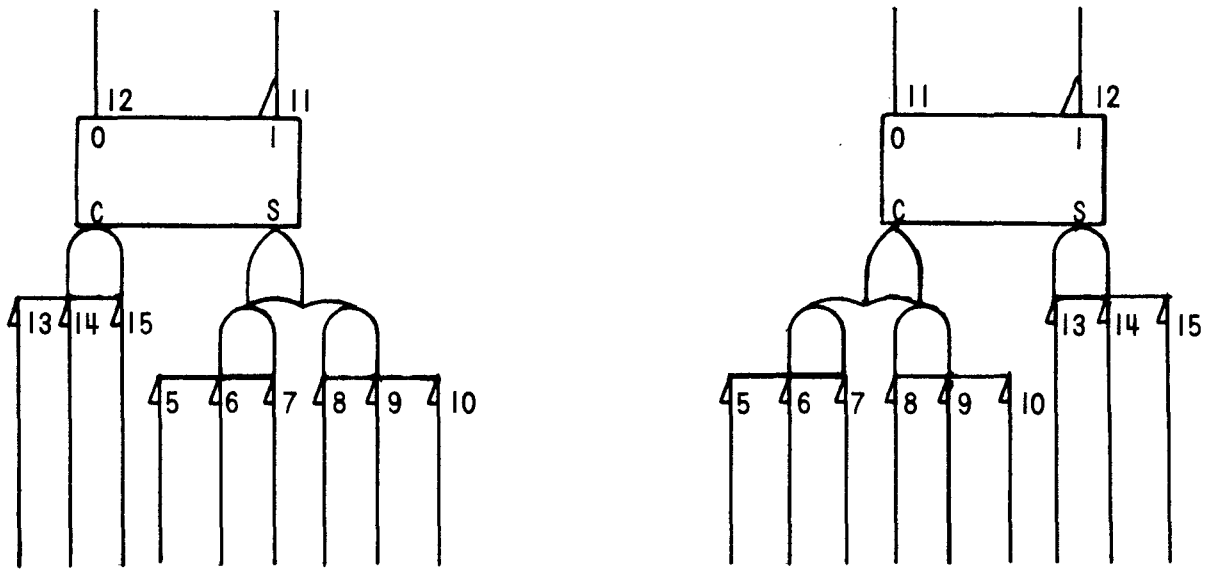
The maximum input current required is 5.8 milliamperes with 0.0 volts input.

This circuit is capable of driving six AND or AND/OR gates from each output pin for a total of 18 gates per logic element.

The speed of the circuit is such that the second of two series-connected stages will produce a usable output before the termination of a clock-phase input pulse to the first stage. The duration of a normal clock-phase pulse is 125 nanoseconds.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volts	HIGH	0.0 Volts	VOLTAGE	Grd	+15.0	-15.0	-4.5
LOW	-4.5 Volts	LOW	-4.5 Volts	MW	-	194	200	196

Figure 8-11. Driver Amplifier, Card Type 7002013



LOGIC SYMBOLS

LOGIC DESCRIPTION

This circuit may function in either of the two configurations shown above. In either case, all three inputs to any one AND gate must be low to perform the clear or set function.

The right side of the flip-flop is called the Set side, the left side is called the Clear side. When the flip-flop is cleared, the output from the Clear side is low. When the flip-flop is set, this output is high. The opposite is true for the Set side.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive voltage excursions of -0.0 volts and nominal negative voltage excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

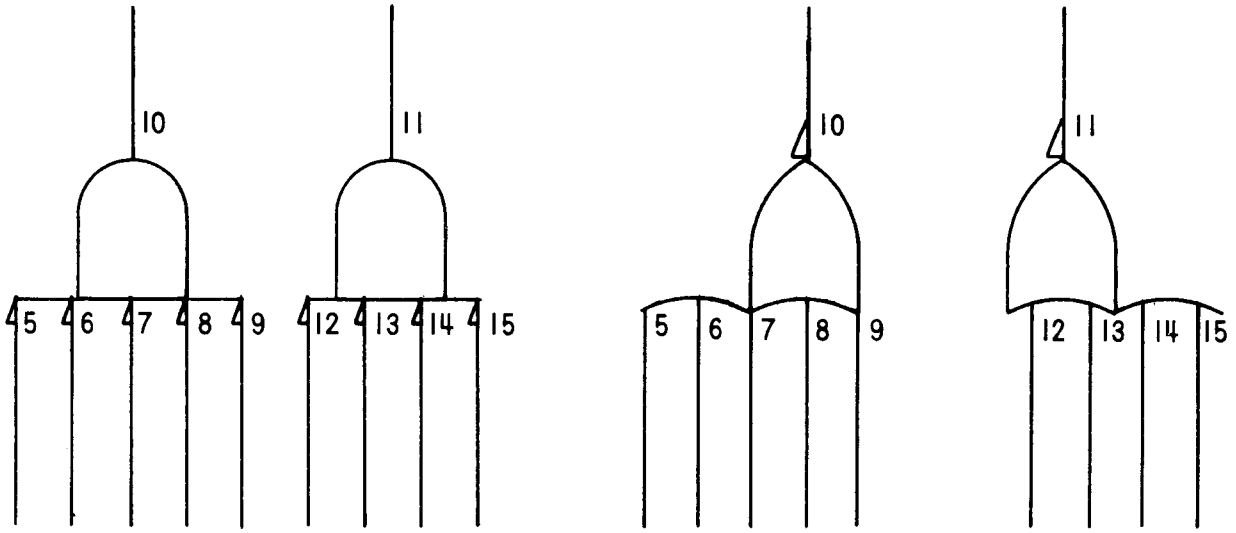
The maximum input current required is 7.1 milliamperes.

This logic element is capable of driving four AND gates and an indicator driver.

The speed of the circuit is such that the second of two series-connected circuits will produce a usable output before the termination of the clock-phase input signal to the first stage. The duration of the normal clock-phase pulse is 125 nanoseconds.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volts	HIGH	0.0 Volts	VOLTAGE	Grd	+15.0	-15.0	-4.5
LOW	-4.5 Volts	LOW	-4.5 Volts	MW	-	64	470	43

Figure 8-12. Flip-Flop, Card Type 7002020



LOGIC SYMBOLS

LOGIC DESCRIPTION

When all used inputs to a circuit are low, the output from that circuit will be high. If any one or more inputs to a circuit is high, the output will be low.

The module may be used either to AND low input signals or to OR high input signals.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive voltage excursions of -0.0 volts and nominal negative voltage excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

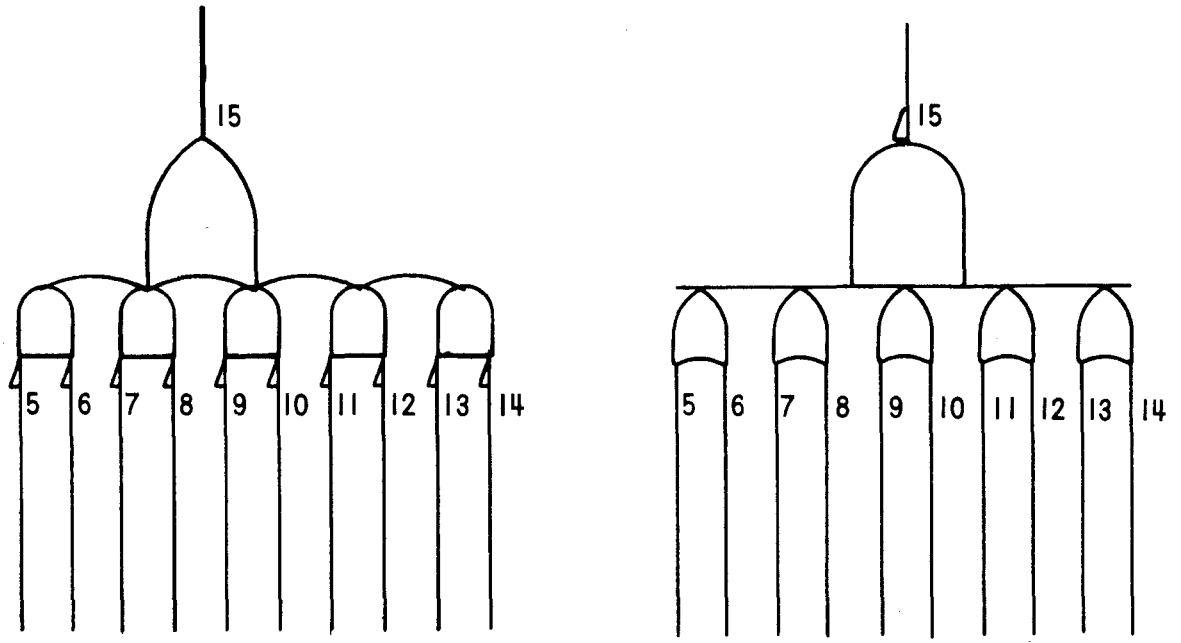
This logic element is capable of driving five AND/OR gates or six AND gates.

The maximum speed of this circuit is such that the second of two series-connected circuits will produce a usable output before the termination of the clock-phase input signal to the first circuit. The duration of the normal clock-phase pulse is 125 nanoseconds.

LOGIC			
INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS				
PIN	1	2	3	4
VOLTAGE	Grd	+15.0	-15.0	-4.5
MW	-	80	200	86

Figure 8-13. Inverter, Card Type 7002030



LOGIC SYMBOLS

LOGIC DESCRIPTION

When both inputs to any one AND circuit are low, the output of the module will be high. If at least one input to each OR circuit is high, the module output will be low.

The module may be used to either OR low input signals or to AND high input signals.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive voltage excursions of -0.0 volts and nominal negative voltage excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

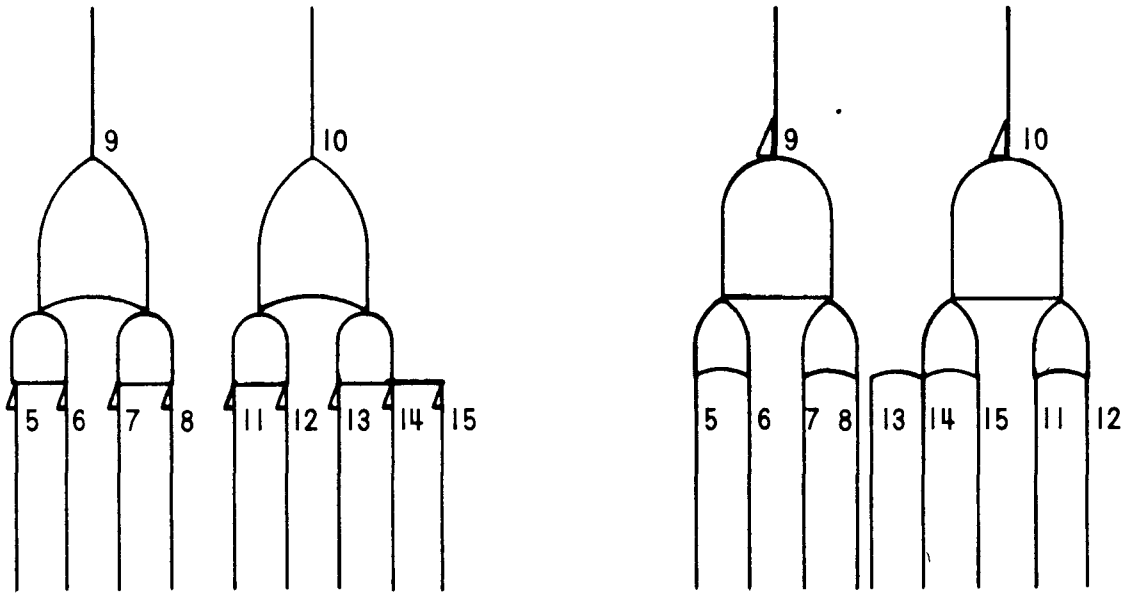
This logic element is capable of driving five AND/OR gates or six AND gates.

The maximum speed of this circuit is such that the second of two series-connected circuits will produce a usable output before the termination of the clock-phase input signal to the first circuit. The duration of the normal clock-phase pulse is 125 nanoseconds.

LOGIC			
INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS				
PIN	1	2	3	4
VOLTAGE	Grd	+15.0	-15.0	-4.5
MW	-	33	430	43

Figure 8-14. Inverter, Card Type 7002040



LOGIC SYMBOLS

LOGIC DESCRIPTION

When all input signals to any one AND input circuit are low, the output from the logic element will be high. If at least one input to each AND input circuit is high, the logic element output signal will be low.

The module may be used to either AND low signal inputs or to OR high signal inputs.

ELECTRICAL DESCRIPTION

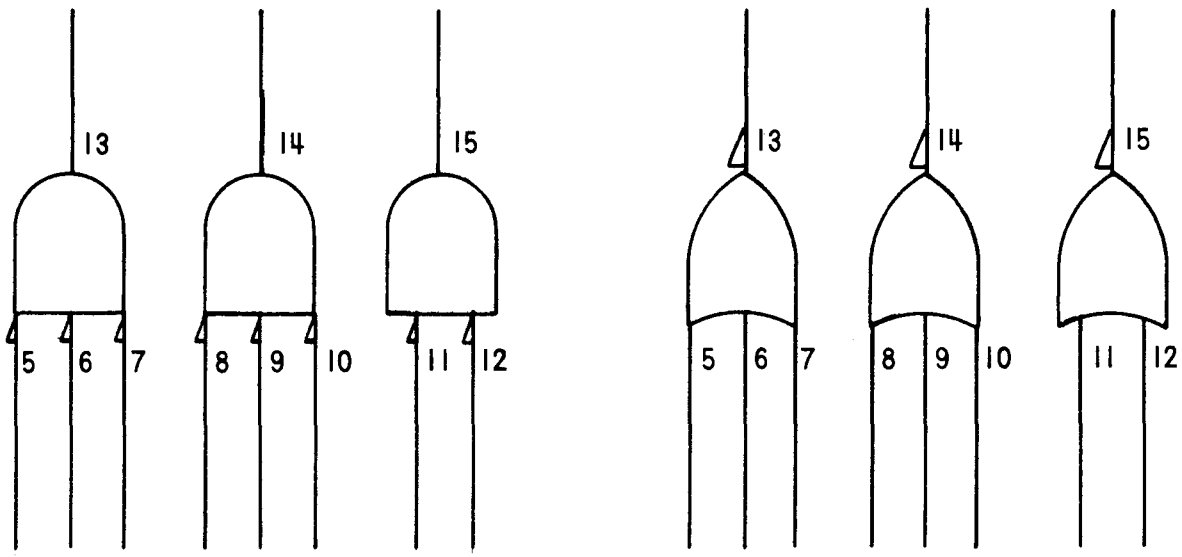
Input signals to this circuit must have nominal positive voltage excursions of -0.0 volts and nominal negative voltage excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

This logic element is capable of driving five AND/OR gates or six AND gates.

The maximum speed of this circuit is such that the second of two series-connected circuits will produce a usable output before the termination of the clock-phase input signal to the first circuit. The duration of the normal clock-phase pulse is 125 nanoseconds.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volts	HIGH	0.0 Volts	VOLTAGE	Grd	+15.0	-15.0	-4.5
LOW	-4.5 Volts	LOW	-4.5 Volts	MW	-	66	375	86

Figure 8-15. Inverter, Card Type 7002050



LOGIC SYMBOLS

LOGIC DESCRIPTION

When all inputs to a logic element are low, the output from that element will be high. When any input to an element is high, the output from that element will be low.

The module may be used to either AND low input signals or to OR high input signals.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive voltage excursions of -0.0 volts and nominal negative voltage excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

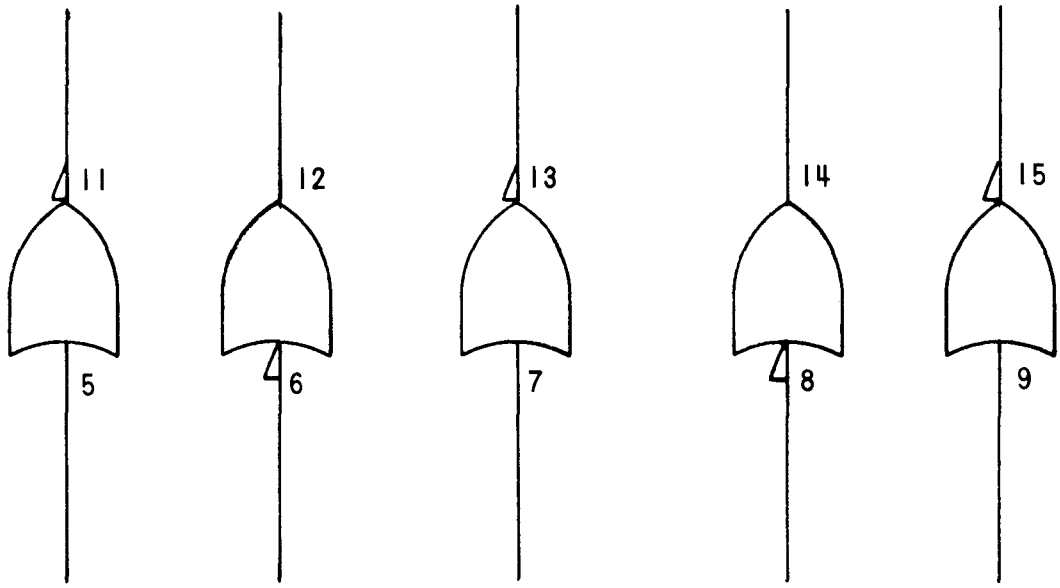
The maximum input current required is 5.8 milliamperes with 0.0 volts input.

The elements are capable of driving five AND/OR gates or six AND gates.

The speed of the circuit is such that the second of two series-connected circuits will produce a usable output before the termination of the clock-phase input signal to the first stage. The duration of the normal clock-phase pulse is 125 nanoseconds.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volts	HIGH	0.0 Volts	VOLTAGE	Grd	+15.0	-15.0	-4.5
LOW	-4.5 Volts	LOW	-4.5 Volts	MW	-	120	300	129

Figure 8-16. Inverter, Card Type 7002060



LOGIC SYMBOLS

LOGIC DESCRIPTION

The logic elements on this module are used to invert the input signal. If the input signal to any element is a low, the output of that element will be a high. Conversely, if the input to an element is a high, the output of that element will be a low.

Either of the two logic symbols shown above may be used to represent the logic elements and may be used interchangeably.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive voltage excursions of -0.0 volts and nominal negative voltage excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

The maximum input current required is 5.8 milliamperes with 0.0 volts input.

The elements can drive five AND/OR gates or six AND gates.

The speed of the circuit is such that the second of two series-connected circuits will produce a usable output before the termination of the clock-phase input signal to the first stage. The duration of the normal clock-phase pulse is 125 nanoseconds.

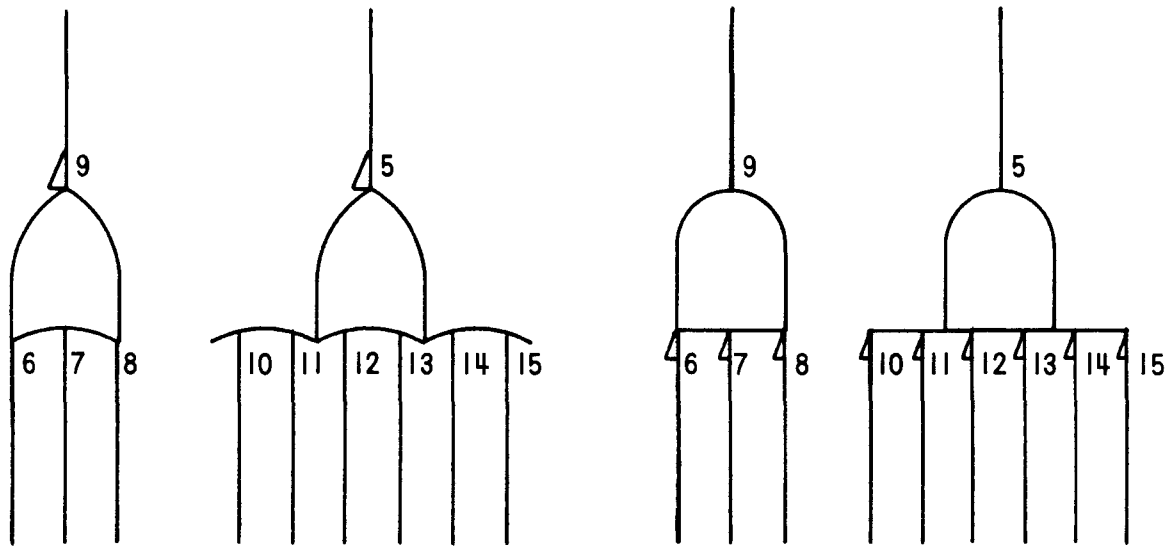
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Grd	+15.0	-15.0	-4.5
MW	-	200	500	215

Figure 8-17. Inverter, Card Type 7002070



LOGIC SYMBOLS

LOGIC DESCRIPTION

When all inputs to any one element are low, the output from that element is high.

When any one input to an element is high, the output from that element is a low.

The elements on this module are used to either AND low input signals or to OR high input signals.

One element on this module has three usable input pins, the other has six.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive voltage excursions of -0.0 volts and nominal negative voltage excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

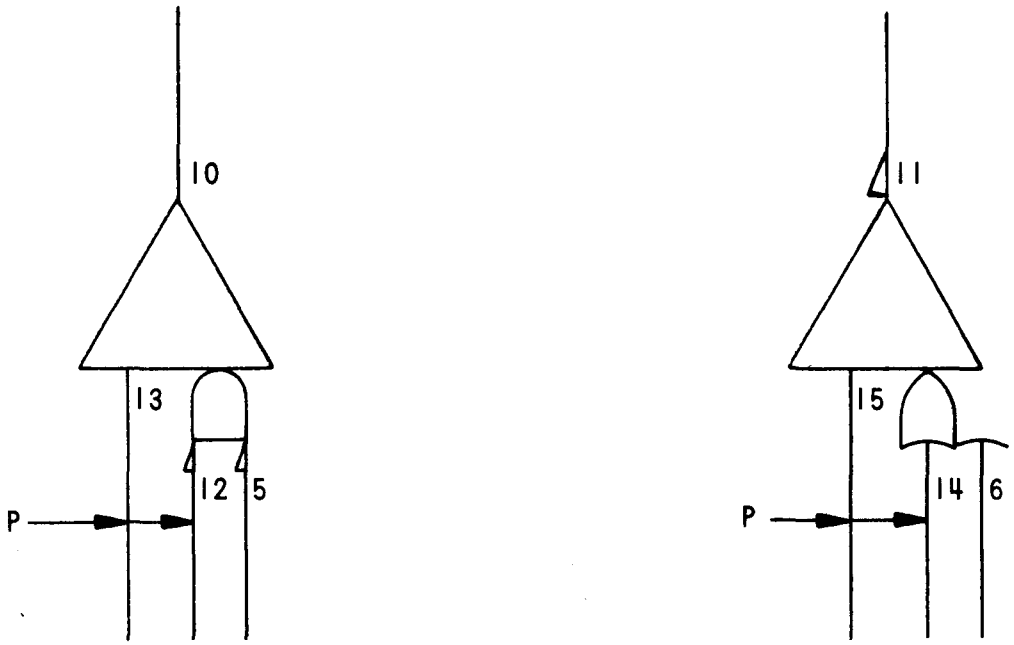
The maximum input current required is 5.8 milliamperes.

Each element can drive five AND/OR circuits or six AND circuits.

The maximum speed of each element is such that the second of two series-connected stages will produce a usable output before the termination of the clock-phase input signal to the first stage. The duration of the normal clock-phase signal is 125 nanoseconds.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volts	HIGH	0.0 Volts	VOLTAGE	Grd	+15.0	-15.0	-4.5
LOW	-4.5 Volts	LOW	-4.5 Volts	MW	-	80	200	86

Figure 8-18. Inverter, Card Type 7002080



LOGIC SYMBOLS

LOGIC DESCRIPTION

This module provides a gated input of signals from peripheral devices working in conjunction with the computer.

If the input to pin 5 is high, the output at pin 10 will be low.

If the input to pin 5 is low and the input to pin 12 is 0.0 volts, the output will be low.

If the input to pin 5 is low and the input to pin 12 is -15.0 volts, the output will be 0.0 volts.

Pins 13 and 15 are the ground return for the twisted pair.

ELECTRICAL DESCRIPTION

Input signals must have positive voltage excursions to a level between 0.0 and 0.5 volts and negative voltage excursions between -13.5 and -16.5 volts. Input signals are applied to either pin 12 or 14.

The gating signals applied to either pin 5 or 6 have positive excursions to a level between 0.0 and -0.5 volts, and negative voltage excursions to a level between -3.6 and -5.4 volts.

Output voltage excursions are the same as those given for the gating signals.

The maximum input current required is 3.7 milliamperes.

The elements on this module are capable of driving two AND/OR gates or two AND gates.

The circuit delay is between 1.0 and 2.2 microseconds.

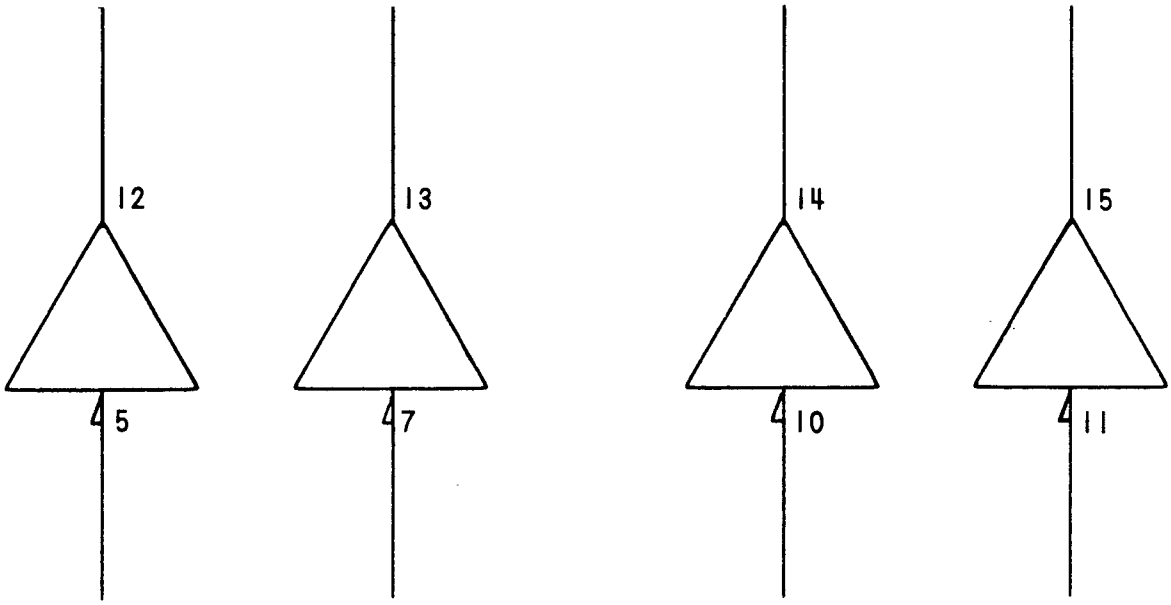
LOGIC

INPUT		OUTPUT	
LOW	-15.0 Volts	HIGH	0.0 Volts
HIGH	0.0 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Grd	+15.0	-15.0	-4.5
MW	-	24	96	126

Figure 8-19. Input Amplifier-Inverter, Card Type 7002090



LOGIC SYMBOLS

LOGIC DESCRIPTION

Each element on this module is used to supply the current to light an incandescent indicator.

When the input to an element is low, current will be supplied to light the indicator.

When the input to the element is high, no current is supplied to light the indicator.

ELECTRICAL DESCRIPTION

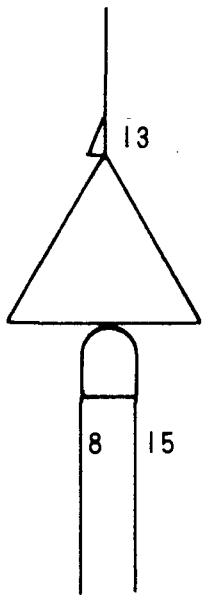
Input signals to these elements must have positive voltage excursions between 0.0 and -0.5 volts and negative voltage excursions between -3.6 and 5.4 volts.

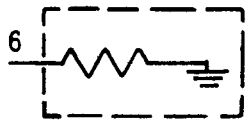
Output voltage excursions are to a level between -13.5 and -15.0 volts.

The output load for this circuit is an incandescent lamp and a limiting resistor which limits the output current to a maximum of 50 milliamperes.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volts	HIGH	0.0 volts	VOLTAGE	Grd	+15.0	-15.0	-4.5
LOW	-4.5 Volts	LOW	-15.0 volts	MW	-	120	-	300

Figure 8-20. Driver Amplifier, Card Type 7002100





LOGIC SYMBOL

LOGIC DESCRIPTION

If either a low is present on pin 15 or pin 15 is disconnected, the output from the module will be high.

If pin 15 is high, the output from the module will be the complement of the input to pin 8.

Pin 6 is connected to a resistor which is normally used to terminate delay line circuits.

This module is normally used in the clock circuits.

ELECTRICAL DESCRIPTION

Input pulses to this circuit must have nominal positive voltage excursions of 0.0 volts and nominal negative voltage excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

The maximum input current required is 7.65 milliamperes.

The maximum circuit delay is 40 nanoseconds.

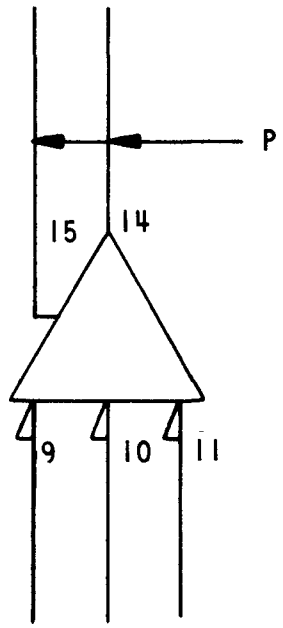
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Grd	+15.0	-15.0	-4.5
MW	-	80	125	325

Figure 8-21. Driver Amplifier, Card Type 7002120



LOGIC SYMBOL

LOGIC DESCRIPTION

When the input signals to pins 9, 10, and 11 are low, the output signal at pin 14 will be 0.0 volts.

If any one input signal is high, the output at pin 14 will be -13.5 volts.

Pin 15 is used to provide the ground return for the twisted-pair conductors.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive and negative voltages of 0.0 volts and -4.5 volts, respectively.

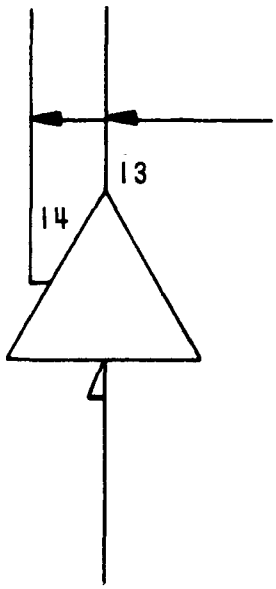
Output signals from this circuit have nominal positive and negative static voltages of 0.0 volts and -13.5 volts , respectively.

The maximum input current required is 2.0 milliamperes.

The rise and fall times of this module are controlled to provide a maximum change of 5.0volts per microsecond.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volts	LOW	-13.5 Volts	VOLTAGE	Grd	+15.0	-15.0	-4.5
LOW	-4.5 Volts	HIGH	0.0 Volts	MW	-	15	630	-

Figure 8-22. Driver Amplifier, Card Type 7002130



LOGIC SYMBOL

LOGIC DESCRIPTION

When the input signal is low, the output between pins 13 and 14 is 0.0 volts. When the input signal is high, the output is -13.5 volts.

Pin 14 is the ground return for the twisted-pair conductors.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive and negative voltage excursions of 0.0 and -4.5 volts, respectively.

Output signals from this circuit have nominal positive and negative static voltage excursions of 0.0 and -13.5 volts, respectively.

The maximum input current required is 2.25 milliamperes.

The output is capable of driving four twisted-pair conductors for a maximum length of 300 feet.

The rise and fall times of this module are controlled to provide a maximum change of 5.0 volts per microsecond.

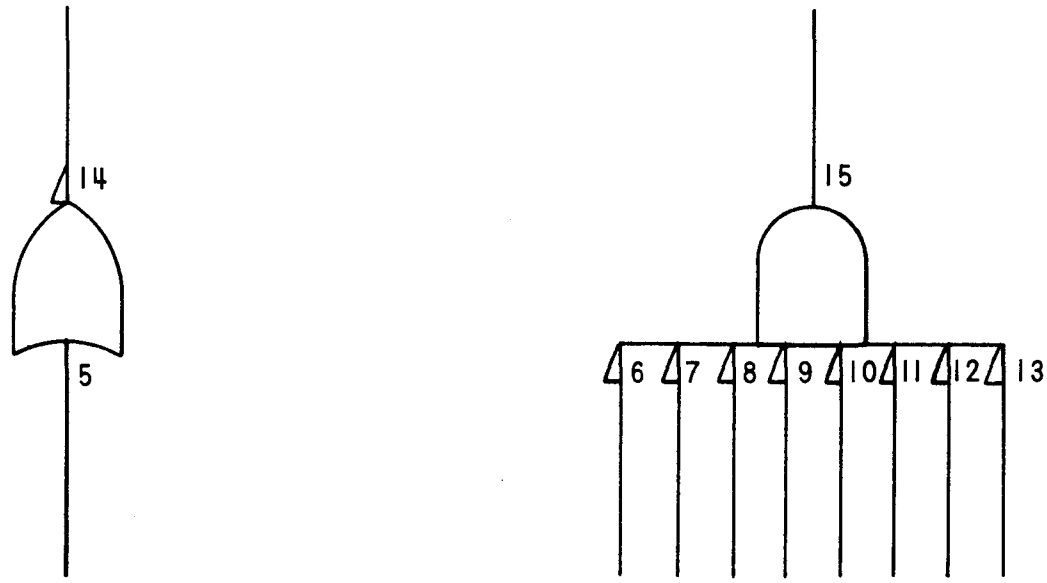
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	-13.5 Volts
LOW	-4.5 Volts	LOW	0.0 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Grd	+15.0	-15.0	-4.5
MW	-	15	450	-

Figure 8-23. Driver Amplifier, Card Type 7002140



LOGIC SYMBOL

LOGIC DESCRIPTION

Any one high-signal input to the AND gate will produce a low signal as an output. When all used inputs are low, the output will be high.

This module may also be used in the OR configuration. In this case, the OR symbol is used and the input of any high will cause a low output.

ELECTRICAL DESCRIPTION

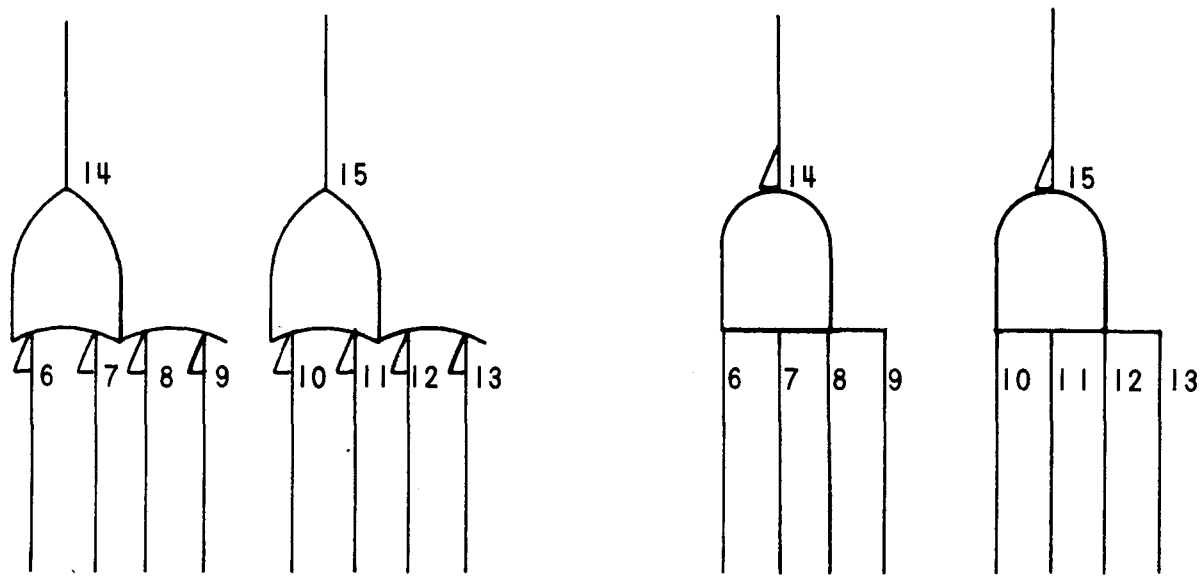
Input signals to this circuit must have nominal positive and negative voltage excursions of 0.0 volts and -4.5 volts, respectively. The output voltage levels are identical to the input voltage levels.

The maximum input current required is 5.8 milliamperes.

The speed of this module is such that the second of two series-connected stages will produce a usable output before the termination of a clock-phase pulse applied to the first stage. The duration of the normal clock-phase pulse is 125 nanoseconds.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volts	HIGH	0.0 Volts	VOLTAGE	Grd	+15.0	-15.0	-4.5
LOW	-4.5 Volts	LOW	-4.5 Volts	MW	-	80	200	86

Figure 8-24. Inverter, Card Type 7002160



LOGIC SYMBOLS

LOGIC DESCRIPTION

When all inputs to any one element are high, the output from that element will be low.

If any one input to an element is low, the output from that element will be high.

The circuit is considered to AND highs or to OR lows.

ELECTRICAL DESCRIPTION

Input signals to the elements must have nominal positive excursions between 0.0 and -0.3 volts and nominal negative excursions between -3.6 and -5.4 volts. The output voltage levels are identical to the input voltage levels.

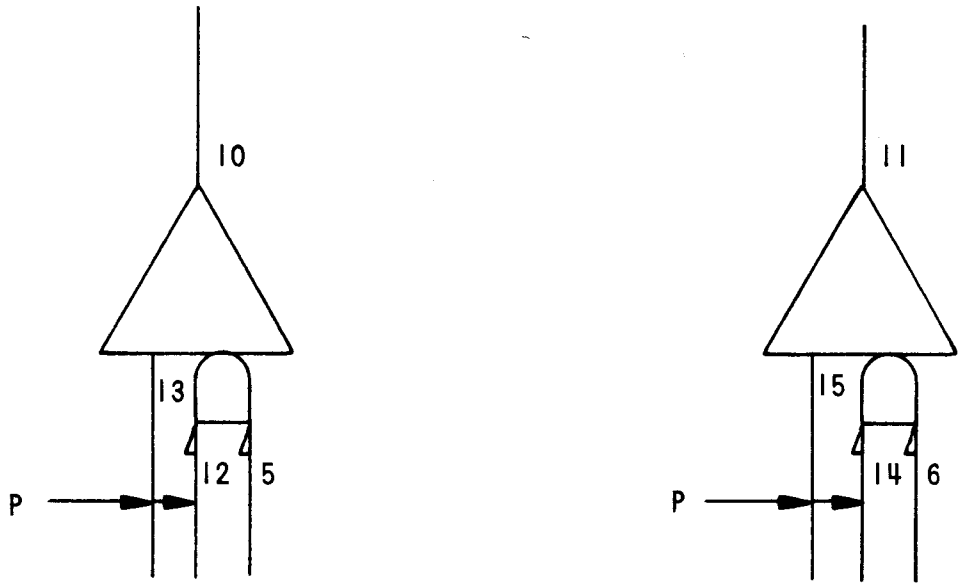
The maximum input current required is 7.0 milliamperes.

Each element is capable of driving six AND gates or five AND/OR gates.

The speed of each element is such that the second of two series-connected stages will produce a usable output before the termination of a clock-phase input signal to the first stage. The duration of the normal clock-phase pulse is 125 nanoseconds.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volts	HIGH	0.0 Volts	VOLTAGE	Grd	+15.0	-15.0	-4.5
LOW	-4.5 Volts	LOW	-4.5 Volts	MW	-	66	680	86

Figure 8-25. Inverter, Card Type 7002220



LOGIC SYMBOLS

LOGIC DESCRIPTION

To produce a high output from pin 10, the input to both pin 12 and 5 must be low. Pin 13 is the ground return for the twisted-pair input.

If either pin 12 or pin 5 are high, the output from pin 10 will be low.

The circuit has a high common-noise rejection when used with the twisted-pair input. The input impedance is balanced so that noise coupled into one conductor is also coupled into the other conductor and balanced out.

ELECTRICAL DESCRIPTION

Input signals to pin 12 must have nominal positive voltage excursions of -0.3 volts and nominal negative voltage excursions of -3.3 volts. Input voltages to the gate, pin 5, must have nominal positive voltage excursions of -0.3 volts and nominal negative voltage excursions of -4.5 volts.

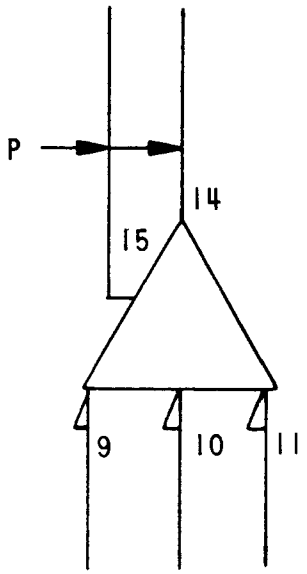
Output voltage levels are the same as those listed for the gate voltage levels.

The maximum input current required is 1.3 milliamperes. The maximum current turn-on and turn-off time is 200 nanoseconds.

This circuit is capable of driving two AND/OR gates or two AND gates.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volts	HIGH	0.0 Volts	VOLTAGE	Grd	+15.0	-15.0	-4.5
LOW	-3.0 Volts	LOW	-4.5 Volts	MW	-	180	255	40

Figure 8-26. Differential Amplifier, Card Type 7002321



LOGIC SYMBOL

LOGIC DESCRIPTION

To produce a high output, all inputs must receive a low signal. If any one input has a high applied, the resulting output will be low.

Pin 15 is used as the ground return for the output twisted pair.

The circuit contains high impedance features. With power off and a negative voltage applied from a remote source, the input impedance is not less than 0.1 megohm.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have positive static voltage excursions of between 0.0 and -0.5 volts and negative static voltage excursions of between -3.8 and -5.2 volts.

The output shall have positive static excursions of between 0.0 and -0.5 volts and negative static excursions of between -3.0 and -4.5 volts.

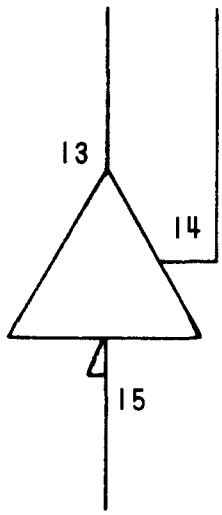
The maximum circuit delay and storage is 200 nanoseconds.

The maximum input current required is 4.6 milliamperes.

This module is capable of driving four input-amplifier modules of the 7002320 type through 150 feet of cable.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volts	LOW	-3.0 Volts	Voltage	Grd	+15.0	-15.0	-4.5
LOW	-4.5 Volts	HIGH	0.0 Volts	MW	-	130	500	80

Figure 8-27. Control Line Amplifier, Card Type 7002331



LOGIC SYMBOL

LOGIC DESCRIPTION

When the input signal to pin 15 is a low, the output at pin 13 is high. When the input is high, the output is low. Pin 14 is the ground connection for the twisted-pair output line.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive voltage excursions of -0.3 volts and nominal negative voltage excursions of -4.5 volts.

Output signals from this circuit will have nominal positive voltage excursions of -0.3 volts and a nominal static negative voltage excursion between -3.0 and -4.5 volts.

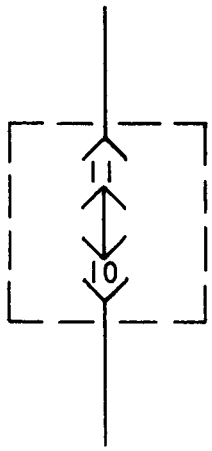
The maximum circuit delay and storage is 200 nanoseconds.

Maximum input current required is 4.6 milliamperes.

This module is capable of driving four input-amplifier modules of the 7002320 type through 150 feet of cable.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volts	LOW	-3.0 Volts	VOLTAGE	Grd	+15.0	-15.0	-4.5
LOW	-4.5 Volts	HIGH	0.0 Volts	MW	-	108	561	40

Figure 8-28. Data Line Amplifier, Card Type 7002341

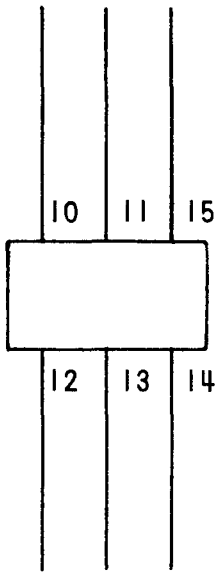


ELECTRICAL CONNECTIONS

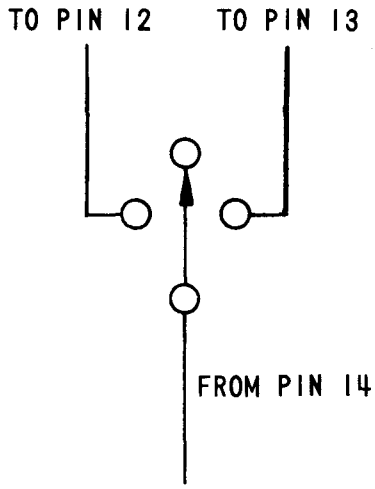
LOGIC DESCRIPTION	ELECTRICAL DESCRIPTION
(Not Applicable)	This module consists of a series of jumper wires used primarily for the transition from fast to slow interface in the input/output section of the computer.

				POWER REQUIREMENTS				
				PIN	1	2	3	4
				VOLTAGE	-	-	-	-
				MW	-	-	-	-

Figure 8-29 High-Speed Selector, Card Type 7002730



LOGIC SYMBOL



EXTERNAL CONNECTIONS

LOGIC DESCRIPTION

This module is used to provide a regulated voltage output for use by certain memory circuits.

Normal voltage output is a regulated -10 volts. Connecting pins 13 and 14 through the marginal check switch, as shown above, will provide an output at pin 15 of -11.0 volts. Connecting pins 12 and 14 will provide -9.0 volts.

The marginal check switch is used to determine the operating characteristics of the memory circuits under tolerable limit.

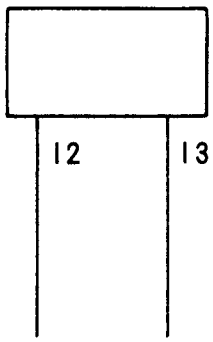
ELECTRICAL DESCRIPTION

The base of an externally-mounted, voltage-control transistor is connected to pin 11 of this module. The emitter of the transistor connects to pin 15. The collector of the transistor is connected to a -15.0 volt supply. The variable resistor is then adjusted to approximately -10.0 volts (clipping voltage) applied to the transistor. The resulting -10.0 volts are available as a regulated output at pin 15. This output voltage is adjustable between -5.0 and -12.0 volts.

The circuit is capable of supplying 500 milliamperes of current.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	N/A	HIGH	N/A	VOLTAGE	Grd	-	-15.0	-
LOW	N/A	LOW	N/A	MW	-	-	750	-

Figure 8-30. Marginal Check Voltage Regulator, Card Type 7002861



LOGIC SYMBOL

LOGIC DESCRIPTION

For the logic description of this module, refer to the logic description of the 7003720 module.

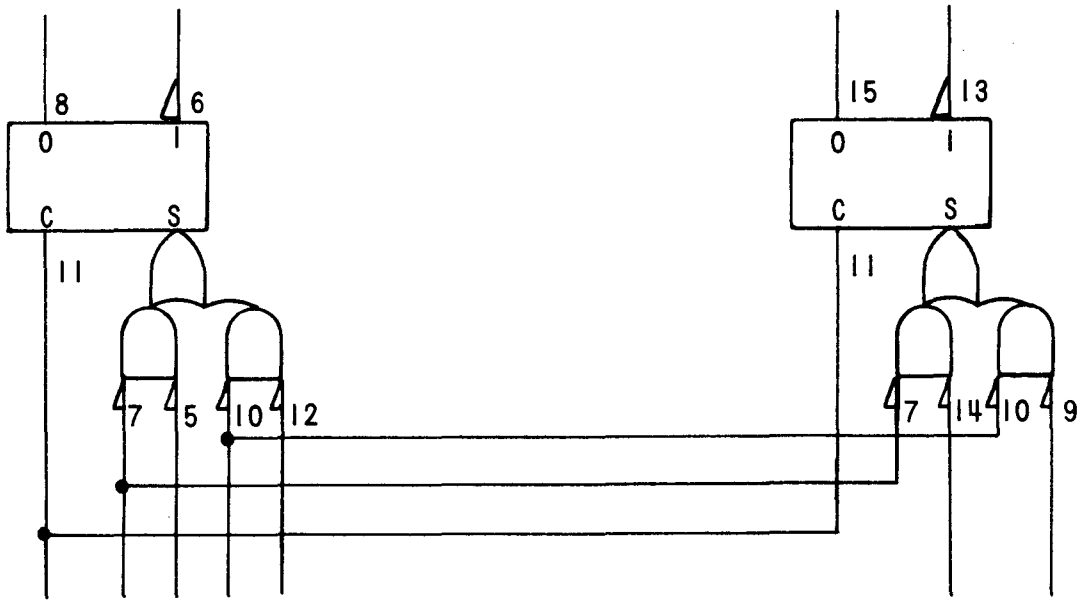
ELECTRICAL DESCRIPTION

This module functions as a detection device to sense voltage failures and fluctuations greater than 10 percent in the positive and negative 15-volt supplies. The level of detection may be adjusted to any level between 12.5 and 13.5 volts.

This module is designed to be used in conjunction with the 7003720 module. Either pin 12 or 13 of this module is connected to pin 13, 14, or 15 of the 7003720 module for voltage protection.

				POWER REQUIREMENTS				
				PIN	1	2	3	4
				VOLTAGE	Grd	+15.0	-15.0	-4.5
				MW	-	175	500	40

Figure 8-31. +15 and -15 Voltage Regulator, Card Type 7002880



LOGIC SYMBOLS

LOGIC DESCRIPTION

When both input signals to either of the two input AND gates are low, the flip-flop is set, resulting in a high output at either pin 8 or 15 and a low output at either pin 6 or 13.

When the input signal to pin 11 is high, the flip-flop is cleared with a reversal in the output levels.

Each of the two AND gates for each flip-flop have two common inputs with a single unique input for each gate.

The clear input is common for both flip-flop circuits.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive voltage excursions of 0.0 volts and nominal negative excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

The maximum current required at pins 5, 9, 12, and 14 is 6.85 milliamperes. The maximum current required at pins 7, 10, and 11 is 13.7 milliamperes.

Each output pin is capable of driving five AND circuits or four AND/OR circuits.

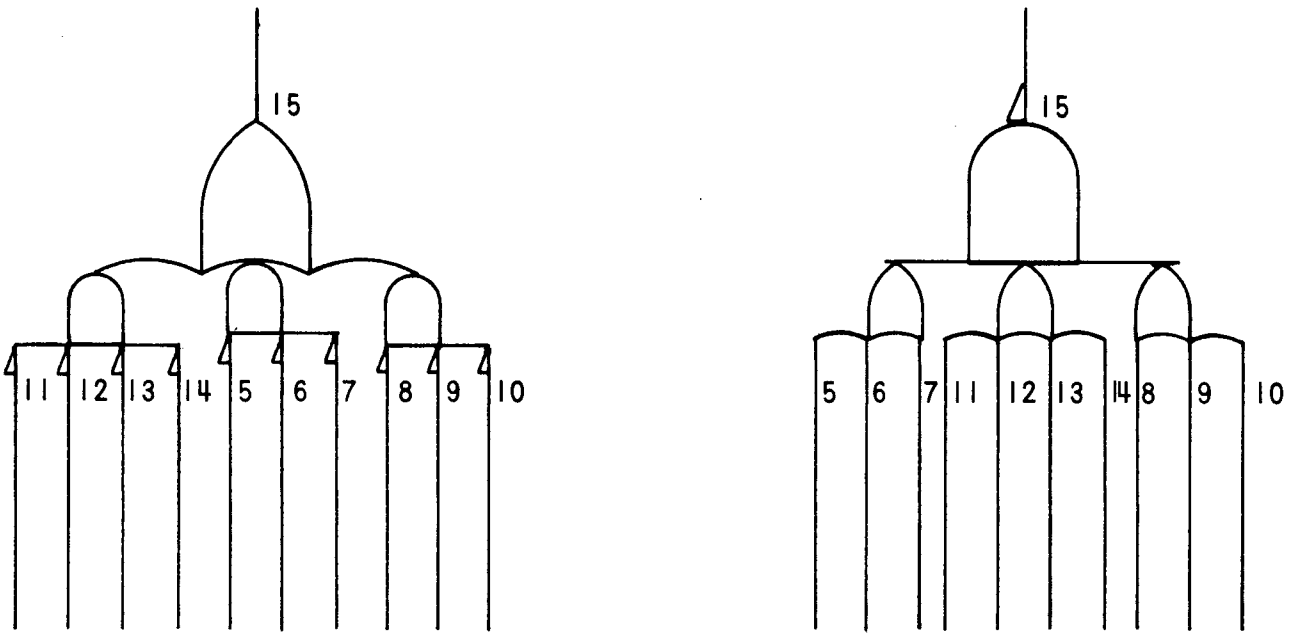
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Grd	+15.0	-15.0	-4.5
MW	-	125	727	86

Figure 8-32. Flip-Flop, Card Type 7002900



LOGIC SYMBOLS

LOGIC DESCRIPTION

When all inputs to any one AND circuit of an element are low, the output from that element will be high.

When at least one input to each OR circuit of an element is high, the output from that element will be low.

ELECTRICAL DESCRIPTION

Input signal to this circuit must have nominal positive excursions of -0.0 volts and nominal negative excursions of -4.5 volts.

The output voltage levels are identical to the input voltage levels.

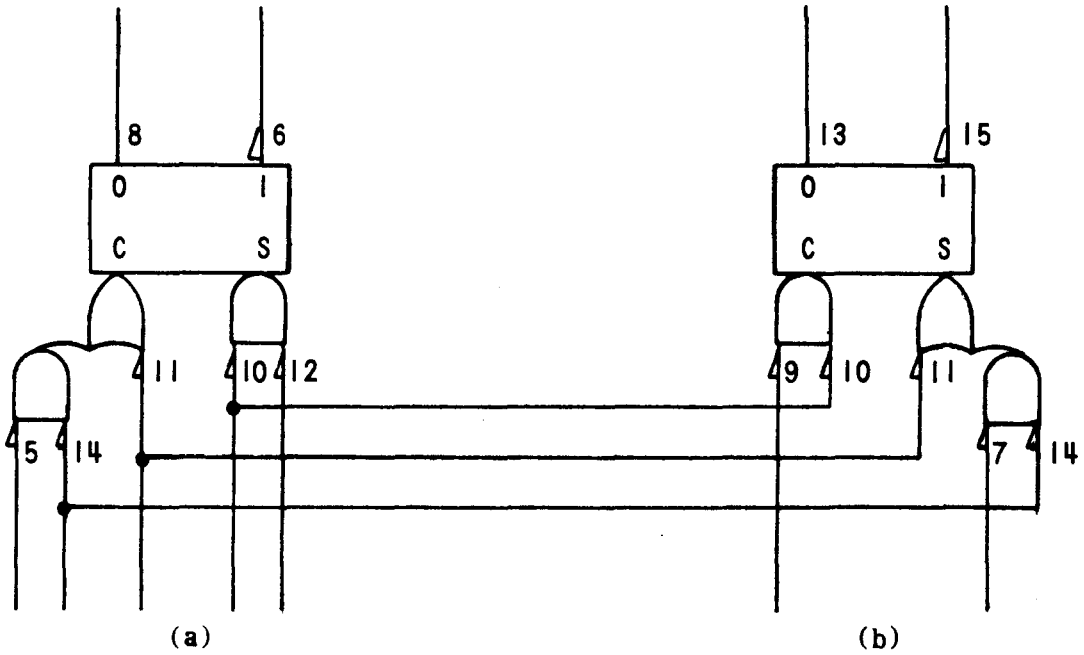
The maximum input current required is 7.1 milliamperes at 0.0 volts input.

The element is capable of driving five AND/OR gates or six AND gates.

The maximum turn-on time is 50 nanoseconds. The maximum turn-off time is 60 nanoseconds.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volts	HIGH	0.0 Volts	VOLTAGE	Grd	+15.0	-15.0	-4.5
LOW	-4.5 Volts	LOW	-4.5 Volts	MW	-	34.2	93.75	43.1

Figure 8-33. Inverter, Card Type 7002920



LOGIC SYMBOLS

LOGIC DESCRIPTION

A low to pin 11 will clear flip-flop (a) and set flip-flop (b). A low to pins 14 and 5 will also clear flip-flop (a) and low to pins 14 and 7 will also set flip-flop (b).

Each AND-gate input to the flip-flop requires two low signals to perform the logic function of clearing or setting.

When the flip-flop is set, the output from the "1" side will be low and the output from the "0" side will be high.

Either of the above configurations may be used to represent the logic function being performed by the flip-flop. Pins 10, 11, and 14 are common to both of the flip-flop circuits with pins 5, 7, 9, and 12 providing the unique input signals.

ELECTRICAL DESCRIPTION

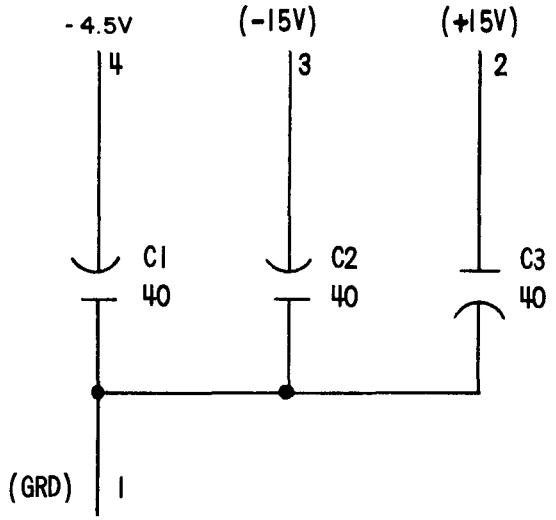
Input signals to this circuit must have nominal positive voltage excursions of 0.0 volts and nominal negative voltage excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

The maximum input current required for a single input pin is 7.1 ma. The current required for a common input pin is 14.2 ma.

The maximum turn-on and turn-off time for each element is 50 and 60 nanoseconds, respectively.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volts	HIGH	0.0 Volts	VOLTAGE	Grd	+15.0	-15.0	-4.5
LOW	-4.5 Volts	LOW	-4.5 Volts	MW	-	132	375	96

Figure 8-34. Flip-Flop, Card Type 7002930

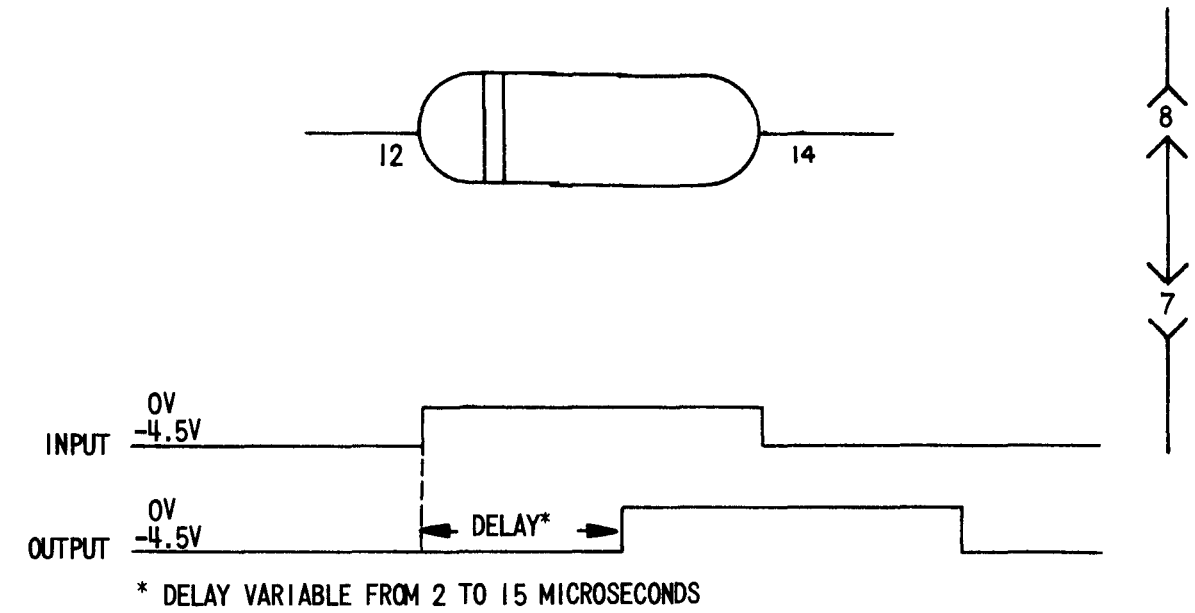


ELECTRICAL CONNECTIONS

LOGIC DESCRIPTION	ELECTRICAL DESCRIPTION
(Not Applicable)	The capacitors mounted on this module provide filter action for the voltages shown in parentheses. Chassis maps indicate the location of the cards in the computer.

	POWER REQUIREMENTS			
PIN	1	2	3	4
VOLTAGE	Grd	+15.0	-15.0	-4.5
MW	-	-	-	-

Figure 8-35. Capacity Assembly - #3, Card Type 7003180



LOGIC SYMBOL

LOGIC DESCRIPTION

The transition from a logic low to a logic high at the input sets the delay. After a set interval, the output changes to a logic high. The input and output pulse widths are the same and exceed the length of the delay.

Pins 7 and 8 supply a jumper network for external circuitry.

ELECTRICAL DESCRIPTION

The time delay operates with input and output pulses that have nominal positive excursions of -0.3 volts and nominal negative excursions of -4.5 volts.

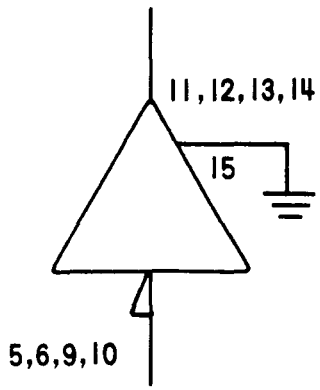
The maximum input current is 5.8 ma at 0.0 volts.

The output can drive three AND or AND/OR circuits.

R7 is adjusted to provide the required delay.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volts	HIGH	0.0 Volts	VOLTAGE	Grd	+15.0	-15.0	-4.5
LOW	-4.5 Volts	LOW	-4.5 Volts	MW	-	-	-	-

Figure 8-36. Time Delay - 2 to 15 usec, Card Type 7003480



LOGIC SYMBOL

LOGIC DESCRIPTION

With a low at the input, the output will be high. With a high at the input, the output will reflect an open circuit.

ELECTRICAL DESCRIPTION

This card contains four identical circuits each of which acts as a switch in the ground lead of a panel lamp. Pin 15 is common to all four output transistors and is grounded.

When a -4.5 volts is applied to any of the four driver inputs, the respective output transistor will conduct, allowing a potential of -15 volts to be applied to the respective panel lamp, illuminating it. When the inputs have a ground applied to them, the respective output transistor will not conduct, thereby opening the circuit to the lamp.

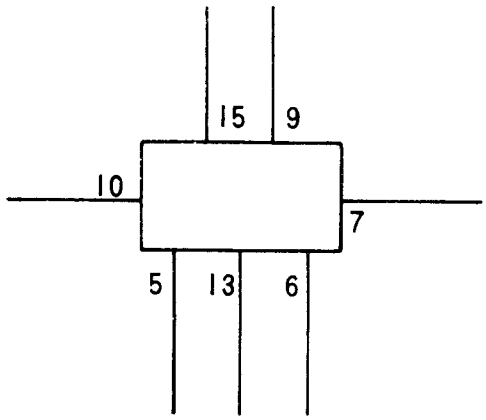
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	N/A

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Grd	15.0	N/A	-4.5
MW	-	-	-	-

Figure 8-37. Driver Amplifier, Card Type 7003490



ELECTRICAL CONNECTIONS

LOGIC DESCRIPTION	ELECTRICAL DESCRIPTION
(Not Applicable)	Pins 6 and 7 are connected to an externally mounted sensistor located in a core stack, which senses and compensates for temperature variations from 0°C (32°F) to 50°C (122°F). Pin 9 is connected to a variable resistor which is part of a voltage-divider network. It is normally adjusted for a steady state current of 4 amperes and will adjust for load changes from 1/3 to 6 amperes. The sensing of temperature and/or load variations affects a change in the forward biasing of the input transistor and results in maintaining an output of -10 volts to within 1 percent. The circuit is capable of steady state current of 4 amperes, and 7 amperes under pulsed conditions for periods up to 4 usec. Recovery time from full load to no load is approximately 40 usec.

	POWER REQUIREMENTS				
	PIN	1	2	3	4
	VOLTAGE	Grd	+15.0	-15.0	-
	MW	-	-	-	-

Figure 8-38. Regulator Amplifier (-10 volt), Card Type 7003600

LOGIC SYMBOLS

LOGIC DESCRIPTION

The elements on this module are used to drive the memory currents during read and write operations involving the core memories.

To produce a low signal output, all inputs must be low. If any one input to an element is high, the output from that element will be high.

ELECTRICAL DESCRIPTION

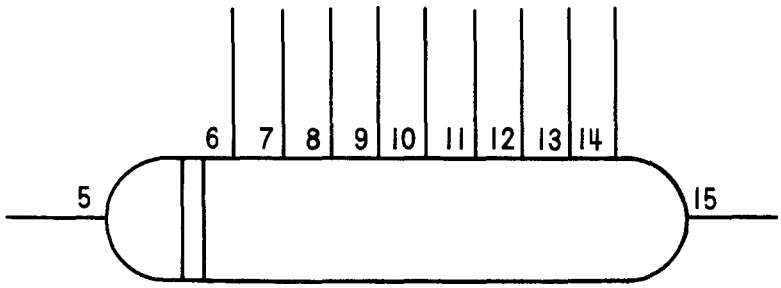
Input signals to this module must have nominal positive and negative voltage excursions of 0.0 and -4.5 volts, respectively.

Output signals from this module have nominal positive excursions of 0.0 volts and nominal negative voltage excursions of -7.5 volts for use in reading and writing operations in the core memory.

LOGIC			
INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-7.5 Volts

POWER REQUIREMENTS				
PIN	1	2	3	4
VOLTAGE	Grd	+15.0	-15.0	-4.5
MW	-	-	-	-

Figure 8-39. -7.5 Volt Memory Driver, Card Type 7003621



LOGIC SYMBOL

LOGICAL DESCRIPTION

This module provides a delay for input signals, either high or low, for a minimum of 5 nanoseconds and a maximum of 50 nanoseconds in increments of 5 nanoseconds. The minimum delay is available at pin 6 and each successive pin provides an additional 5-nanosecond delay.

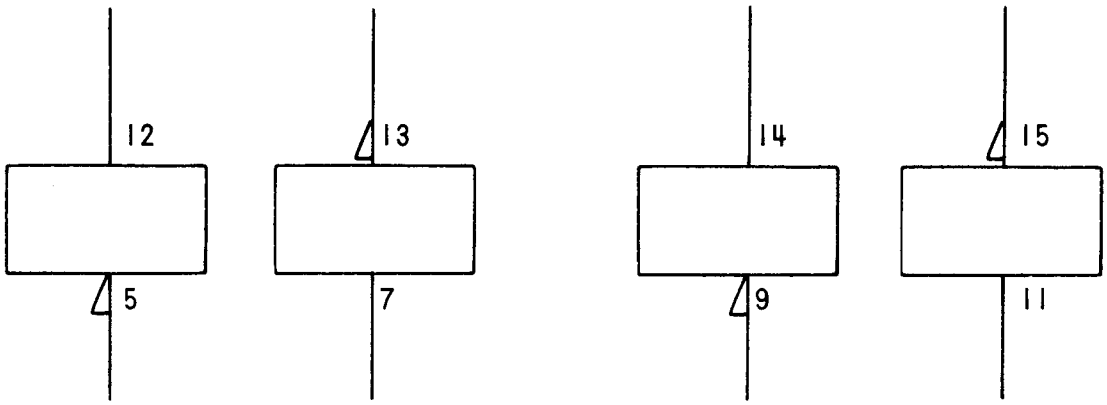
ELECTRICAL DESCRIPTION

This module, composed of coils and capacitors, operates in conjunction with the 7003640 module to produce timing and clock pulses for use throughout the computer logic.

A 200-ohm resistor is required to terminate the output of this module. This resistor is normally provided by the 7002120 module.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volts	HIGH	0.0 Volts	VOLTAGE	-	-	-	-
LOW	-4.5 Volts	LOW	-4.5 Volts	MW	-	-	-	-

Figure 8-40. Pulse-Delay Network, Card Type 7003630



LOGIC SYMBOLS

LOGIC DESCRIPTION

The logic elements on this module are used in conjunction with the 7003630 module to produce clock pulses for use throughout the computer for timing purposes.

Input pulses to each element are inverted through the element. The output from each element is capable of driving five AND/OR circuits or six AND circuits.

ELECTRICAL DESCRIPTION

Input signals to this module must have nominal positive voltage excursions of 0.0 volts and nominal negative voltage excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

When used with the delay line module, the high-impedance input circuit of this module provides a minimum load to the delay line circuit to prevent reflected signals.

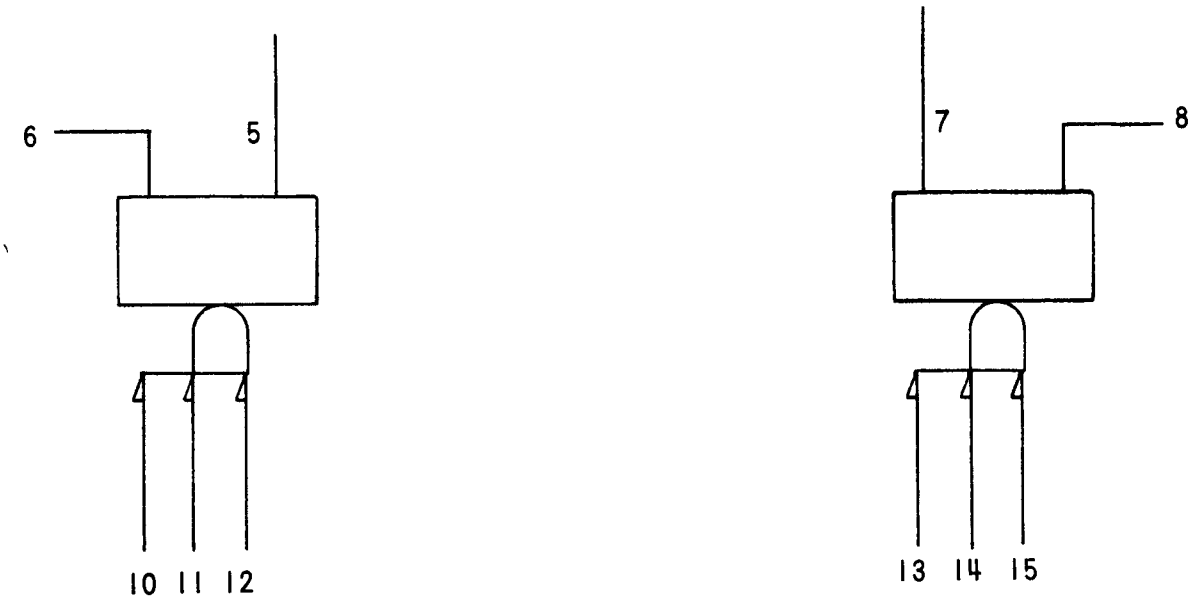
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Grd	+15.0	-15.0	-4.5
MW	-	-	-	-

Figure 8-41. Emitter-Follower Driver, Card Type 7003640



LOGIC SYMBOL

LOGIC DESCRIPTION

When all inputs to the AND gate are low, the output is high. When at least one input is high, the output will be a low.

ELECTRICAL DESCRIPTION

Pins 5 and 6 (7 and 8) are shorted together internally.

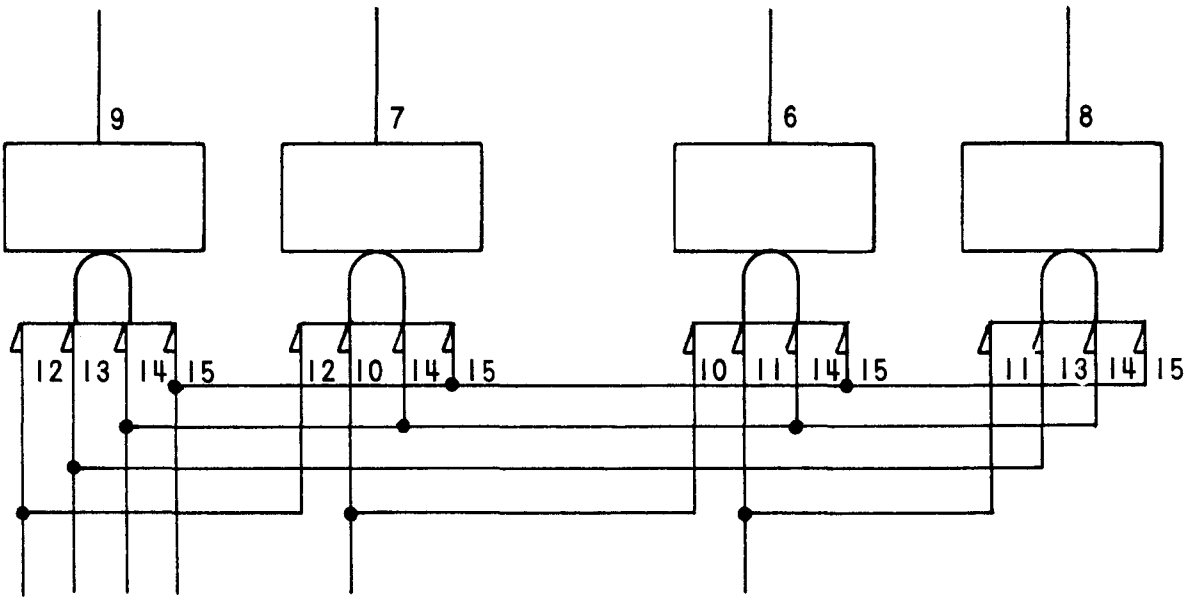
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-15.0 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Grd	+15.0	-15.0	-4.5
MW	-	-	-	-

Figure 8-42. Driver Amplifier, Card Type 7003670



LOGIC SYMBOL

LOGIC DESCRIPTION

Each of the elements on this module will produce a high-signal output when all inputs to that element have a low-signal input. Any one high input to an element will result in a low output from that element.

ELECTRICAL DESCRIPTION

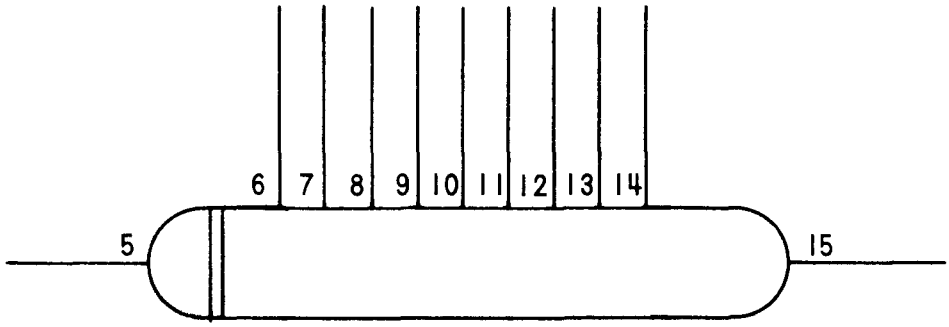
Several common inputs to the elements on the module provide common gating of the output.

Input signals must have nominal positive and negative voltage excursions of 0.0 and -4.5 volts, respectively. Output voltage levels are identical to the input voltage levels.

LOGIC			
INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS				
PIN	1	2	3	4
VOLTAGE	Grd	+15.0	-15.0	-4.5
MW	-	-	-	-

Figure 8-43. Transformer Driver, Card Type 7003680



LOGIC SYMBOL

LOGIC DESCRIPTION

This module provides a minimum delay of 20 nanoseconds and a maximum of 200 nanoseconds to an input pulse of either high or low signal characteristics.

A minimum delay of 20 nanoseconds is provided at pin 6; a maximum delay of 200 nanoseconds is provided at pin 15. Additional delays are provided at taps in increments of 20 nanoseconds.

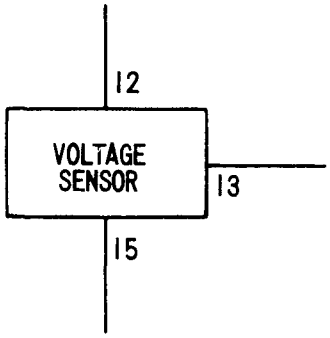
ELECTRICAL DESCRIPTION

This module, composed of coils and capacitors, operates in conjunction with the 7003640 module to produce timing pulses for the computer logic.

A 200-ohm termination resistor is required and is normally supplied as a part of a 7002120 module through pin 6 of that module.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volts	HIGH	0.0 Volts	VOLTAGE	Grd	-	-	-
LOW	-4.5 Volts	LOW	-4.5 Volts	MW	-	-	-	-

Figure 8-44. Pulse-Delay Network, Card Type 7003710



LOGIC SYMBOL

LOGIC DESCRIPTION

This circuit is used in conjunction with assembly 7002880. Pin 12 of 7002880 is connected to pin 12 of this assembly. Pin 15 is connected in the reference voltage line to the memory regulator. One logic circuit is driven off pin 13. A fault in any one of the three voltages will cause the voltage at pin 13 to switch from -4.5 volts to 0.0 volts. This circuit detects the voltage levels high enough to properly operate the logic when the memory is shut down.

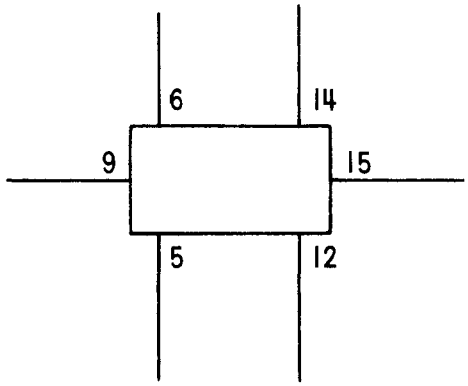
ELECTRICAL DESCRIPTION

This circuit is a detection device designed to sense voltage failures and tolerance decreases greater than 10 percent on the -4.5 volt supply. The level of detection may be adjusted by means of a potentiometer to any level between -3.2 volts and -4.0 volts. The circuit is designed to operate with 18 $\pm$1.8 volts on pin 9 and is grounded through a 1K resistor on pin 8. This results in a voltage of -4.5 volts nominal on pins 13, 14, and 15 under normal operating conditions, and results in ground when the circuit detects a voltage failure.

LOGIC			
INPUT		OUTPUT	
HIGH	N/A	HIGH	N/A
LOW	N/A	LOW	N/A

POWER REQUIREMENTS				
PIN	1	2	3	4
VOLTAGE	Grd	+15.0	-15.0	-4.5
MW	-	-	-	-

Figure 8-45. Voltage Sensor and Positive Switch, Card Type 7003720



LOGIC SYMBOL

LOGIC DESCRIPTION

An unregulated +15.0 volts is applied as a reference voltage to pins 5 and 6. This voltage, supplied through two transistors, is regulated through the use of a sensistor connected to pins 14 and 15.

Any change in temperature in the memory stack is detected and compensating voltages are developed through the transistors. The output voltage level is adjustable through a variable resistor connected between pins 5 and 12.

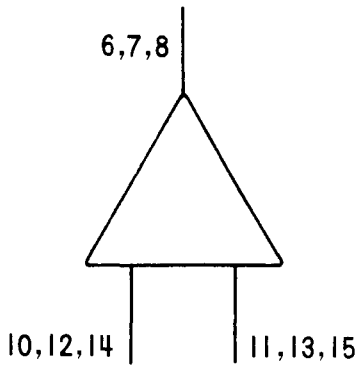
ELECTRICAL DESCRIPTION

The sensistor, mounted on a memory stack, controls the output voltage to give temperature compensation to the drive circuitry to ensure proper core operation through a 0°C (32°F) to 50°C (122°F) ambient temperature range.

The output voltage is regulated to within 1 percent when the input is within 10 percent. The regulator in the output stage is capable of supplying 7 amperes under pulsed conditions for periods up to 4 microseconds and steady state current of 4 amperes. The recovery time from full load to no load is about 40 microseconds.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	N/A	HIGH	N/A	VOLTAGE	Grd	+15.0	-15.0	-
LOW	N/A	LOW	N/A	MW	-	-	-	-

Figure 8-46. Regulator Amplifier (+10 volt), Card Type 7003730

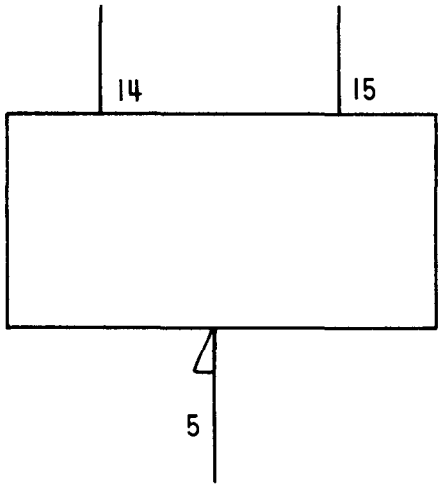


LOGIC SYMBOL

LOGIC DESCRIPTION	ELECTRICAL DESCRIPTION
(Not Applicable)	This card consists of three identical circuits. The input pins are connected to sense lines running through the cores in memory. The signal level applied to the inputs is approximately 50 to 70 millivolts. If the polarity on the sense lines is such that input pin 12 is negative, and input pin 13 is positive, the output at pin 7 will reflect a positive excursion of approximately 0.5 ma. If the polarity at the inputs is reversed or zero, the output at pin 7 will reflect an open circuit. To overcome any possibility of amplifying undesired noise that may be picked up by the sense lines, a common-mode choke is placed across the inputs offering an easy path to ground for the noise.

POWER REQUIREMENTS				
PIN	1	2	3	4
VOLTAGE	Grd	+15.0	-15.0	-
NW	-	-	-	-

Figure 8-47. Sense-Control Amplifier, Card Type 7003740



LOGIC SYMBOL

LOGIC DESCRIPTION

With a low input at pin 5, the output at pins 14 and 15 will be high. With a high input at pin 5, the output at pins 14 and 15 will be an open circuit.

ELECTRICAL DESCRIPTION

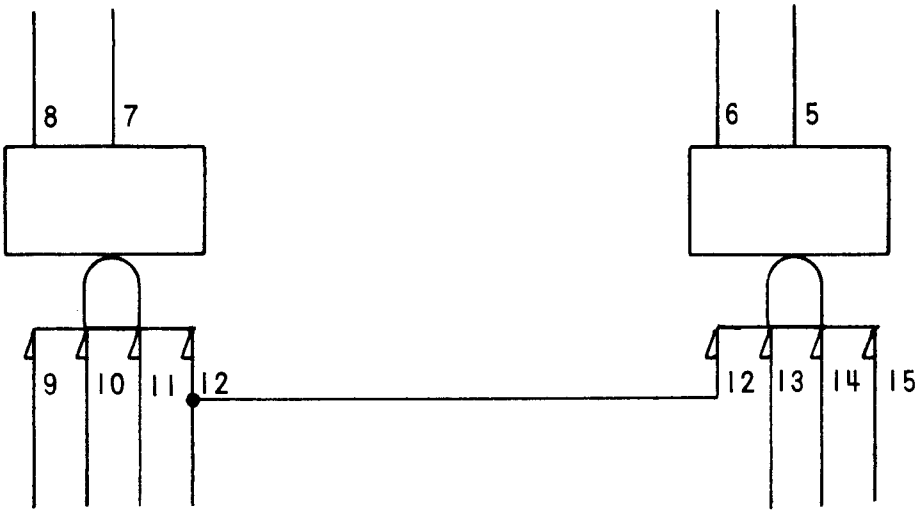
This card is normally used to divert current by passing it directly to ground or allowing it to pass on to another circuit.

With a -4.5 volts applied to input pin 5, the output transistors in this circuit are turned on and any positive potential applied to the output pins 14 and 15 is shunted directly to ground. With 0.0 volts applied at input pin 5, the output pins 14 and 15 will reflect an open circuit and infinite impedance to any applied voltage.

To protect against damage, the circuits to pins 14 and 15 are connected in parallel to divide the power dissipation.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volts	HIGH	0.0 Volts	VOLTAGE	Grd	+15.0	-15.0	-4.5
LOW	-4.5 Volts	LOW	Open	MW	-	-	-	-

Figure 8-48. Current-Control Diverter, Card Type 7003760



LOGIC SYMBOLS

LOGIC DESCRIPTION

When all inputs to one logic element are low, the output transistor, located between pins 7 and 8 (6 and 5) is turned on to allow current to flow between these pins.

If any one input is high, the transistor is cut off and current is inhibited.

ELECTRICAL DESCRIPTION

Input signals to this module must have nominal positive and negative voltage excursions of 0.0 and -4.5 volts, respectively.

The voltage applied to either pin 7 or 8 is considered the bias voltage to determine the output voltage level.

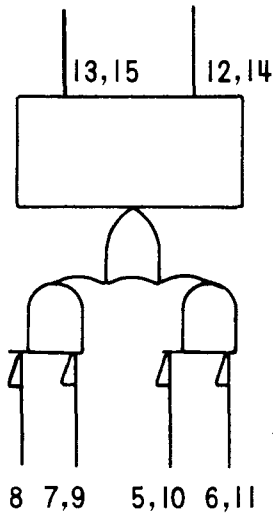
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	N/A
LOW	-4.5 Volts	LOW	N/A

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Grd	+15.0	-15.0	-4.5
MW	-	-	-	-

Figure 8-49. Driver Amplifier, Card Type 7003771



LOGIC SYMBOL

LOGIC DESCRIPTION

With a low at both input pins of either AND gate the output pins 14 and 15, or 12 and 13, will reflect a closed circuit. With one or more highs at both AND gate inputs, the output pins will reflect an open circuit.

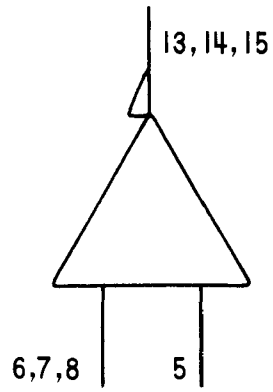
ELECTRICAL DESCRIPTION

The output pins of this card are connected to a transistor that is transformer-coupled to the input circuitry of the card. When -4.5 volts is applied to both inputs of either AND gates, the circuit will be enabled inducing a voltage in the transformer secondary so the base of the output transistor will become positive and the transistor will conduct. At this time the transistor acts as a switch to an external load and a potential of ±18 volts. The polarity of this 18 volts depends on which half of the card is operating.

The length of time the output transistor will conduct is determined by the time constant of the transformer secondary and the resistor connected across it.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volts	HIGH	N/A	VOLTAGE	Grd	+15.0	-15.0	-4.5
LOW	-4.5 Volts	LOW	N/A	MW	-	-	-	-

Figure 8-50. Driver-Digit Amplifier, Card Type 7003780



LOGIC SYMBOL

LOGIC DESCRIPTION

This circuit receives nonlogic voltages at its inputs. However, if a sufficiently positive voltage is applied at its input (pin 6,7, or 8), the respective output (pin 13,14, or 15) will be a logical low. Without a sufficiently high positive voltage at the input, the respective output pin will be a logical high.

Input pin 5 has a constant non-logic bias voltage applied to it.

ELECTRICAL DESCRIPTION

This circuit is a three-stage amplifier normally used for amplifying small pulses from a core memory and contains three identical circuits and a common bias supply (pin 5). The bias voltage applied at pin 5 is -10 volts. With a positive voltage applied to one of the input pins, the forward bias to the input transistor is sufficiently reduced, cutting it off. This results in an output at the respective output pin of -4.5 volts. With an open at the input pins, the bias will be sufficient enough to allow the input transistor to conduct and, consequently, the output transistor. With the output transistor conducting, the output of the circuit is placed at 0.0 volts or ground potential.

LOGIC

INPUT		OUTPUT	
HIGH	N/A	HIGH	0.0 Volts
LOW	N/A	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Grd	+15.0	N/A	-4.5
MW	-	-	-	-

Figure 8-51. Output-Sense Amplifier, Card Type 7003850

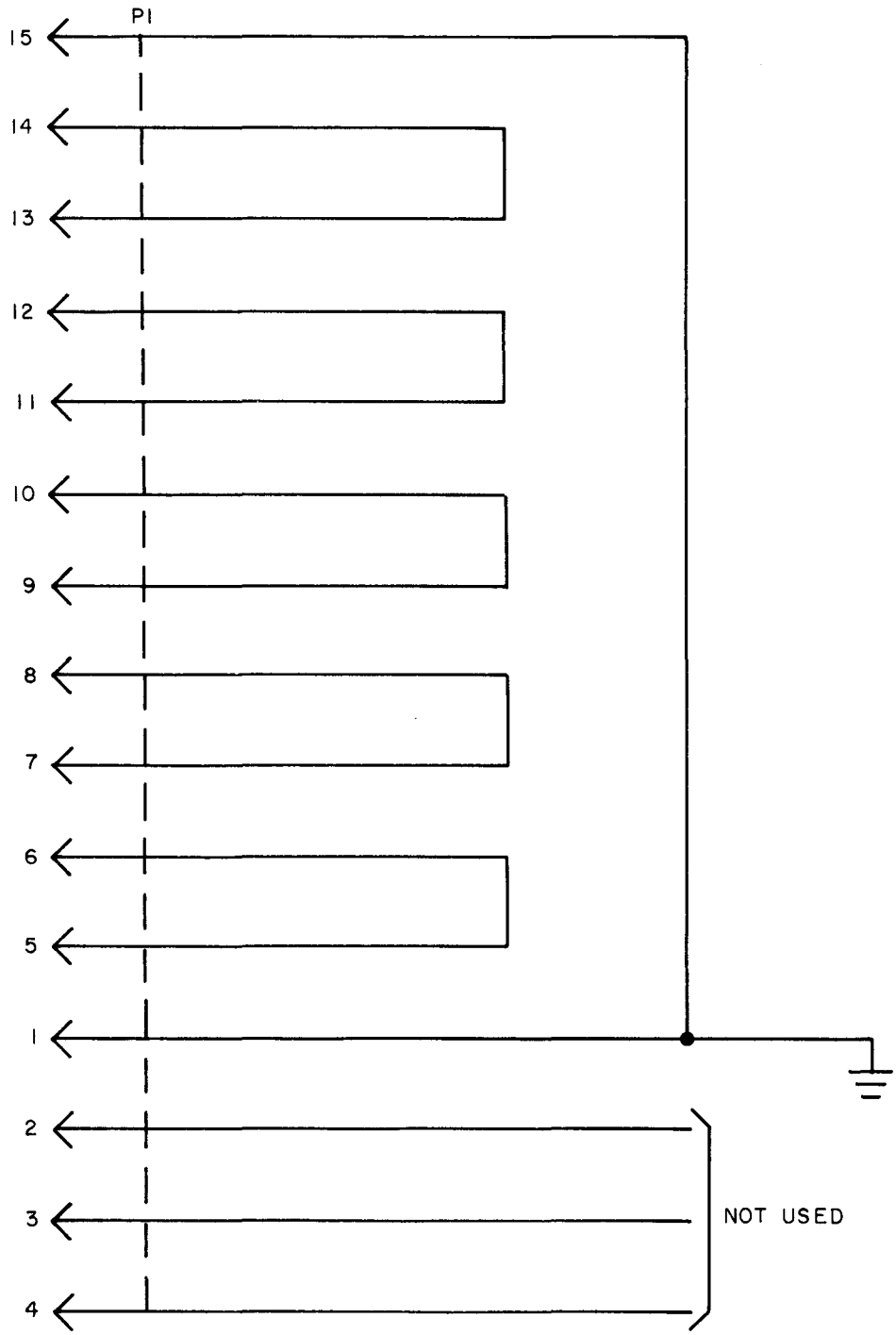


Figure 8-52. Jumper Switch Selector, Module 7104010 Schematic Diagram

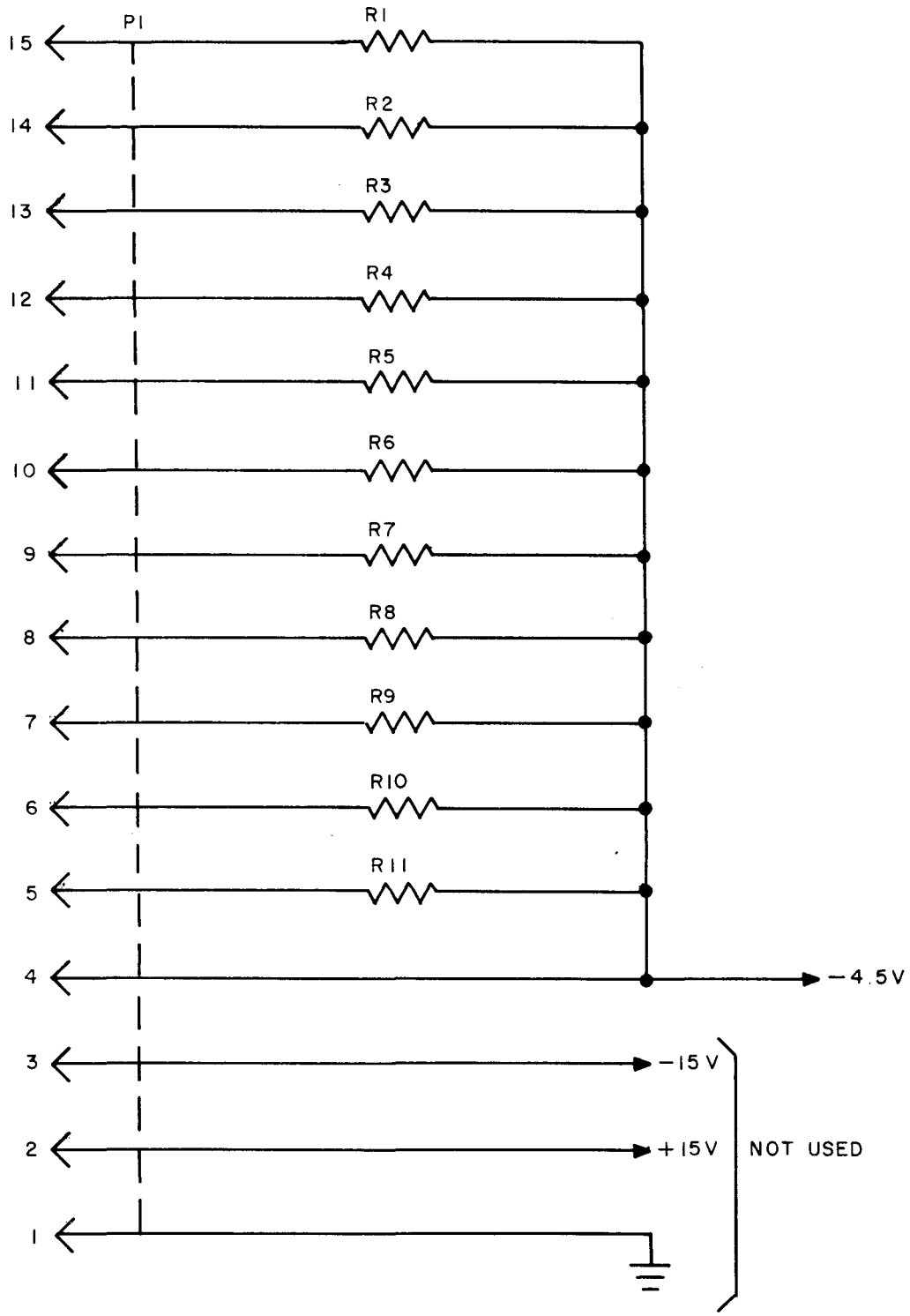
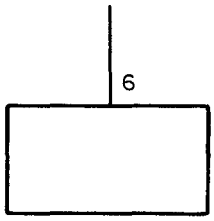


Figure 8-53. Resistor Assembly, Module 7109000 Schematic Diagram



LOGIC SYMBOL

LOGIC DESCRIPTION

When power is applied to the unit, the output, pin 6, will be high and after the R-C time constant of resistor R2 and capacitor C2, the output will become low. The low will be maintained while power is applied to the unit.

ELECTRICAL DESCRIPTION

This module contains a resistor-capacitor network made up of two resistors and two capacitors. The module is used to filter the voltages used for indicators.

LOGIC			
INPUT		OUTPUT	
HIGH	-	HIGH	-
LOW	-	LOW	-

POWER REQUIREMENTS				
PIN	1	2	3	4
VOLTAGE	G	+15v	-15v	-4.5v

Figure 8-54. Capacitor - Resistor Assembly, Module 7109010

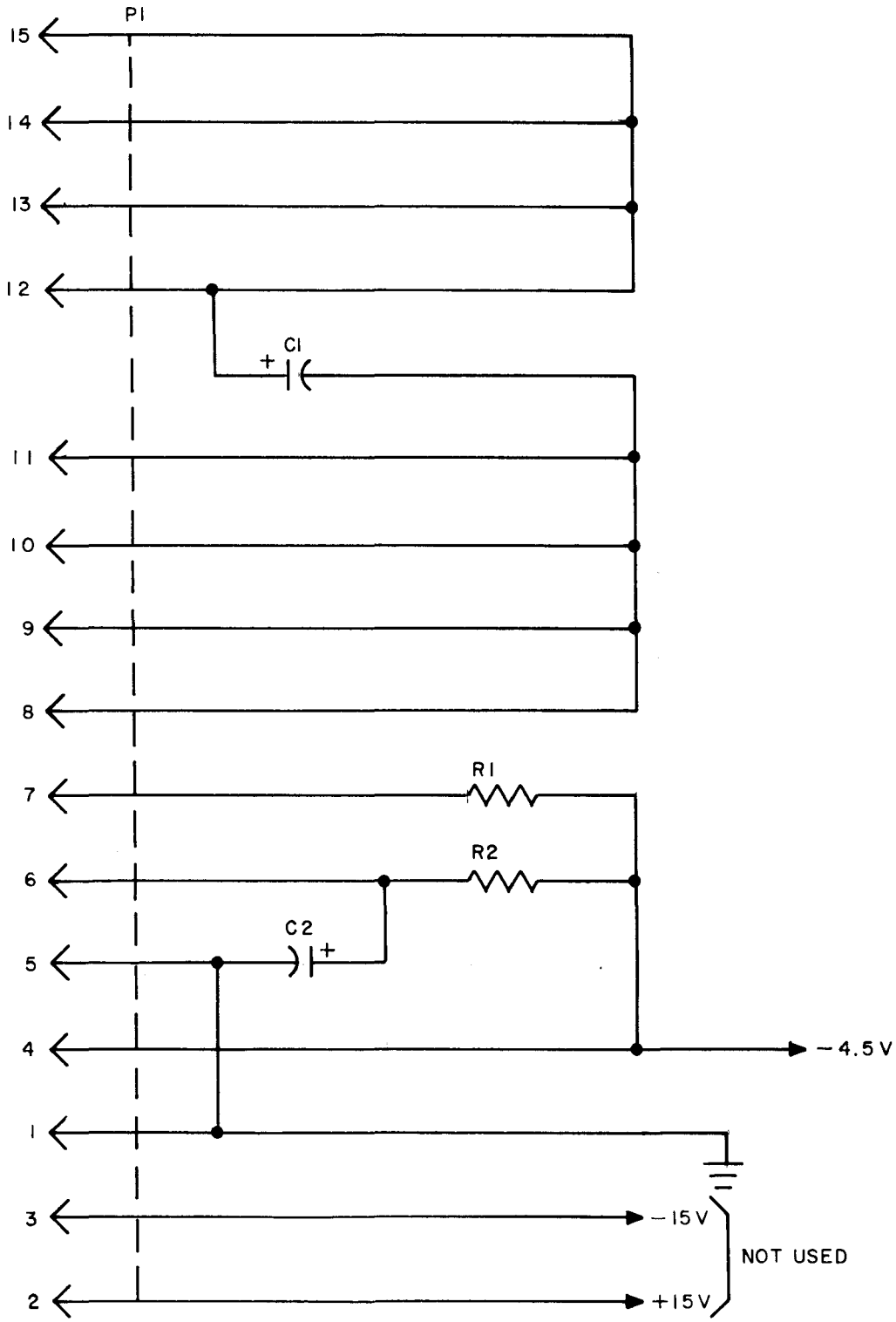


Figure 8-55. Capacitor - Resistor Assembly, Module 7109010 Schematic Diagram

(1) MODULE 7500040; INVERTER, AMPLIFIER, DRIVER. - This module contains five identical circuits that are used for AND, OR, INVERTER AND/OR, or OR/AND functions. The module contains discrete components such as: transistors, diodes, resistors, and capacitors. These components are required, rather than flat packs, in order for each circuit to provide the necessary power to drive a large number of circuits at a propagation time unchanged by the load. Figure 8-57 shows the logic symbols and figure 8-57 shows the schematic diagram.

Two types of AND and OR functions can be performed by the 0040 module. The module functions as a high input AND or low input OR when either pin 43, 44, or 46 is grounded. When the inputs on pins 51 and 52 are high, the output is low. When either input on pins 51 and 52 is low, the output is high. When only one input is used, this circuit performs an INVERTER function. Unused pins are left open. The module functions as a low input AND or high input OR by using either pin 43, 44, or 46 for one input and either pin 51, 52, or 54 for the other input. When both inputs to this circuit are low, the output is high. When one of the inputs is high, the output is low. Unused pins are left open.

The 0040 module also performs an OR/AND or AND/OR function. When one of the inputs to pins 43, 44, and 46 is low and one of the inputs to pins 51, 52, and 54 is low, the output is high. When all the inputs to pins 43, 44, and 46 are high or all the inputs to pins 51, 52, and 54 are high, the output is low.

(2) MODULE 7500260; OSCILLATOR, CLOCK DELAY LINE AND AMPLIFIER. - This module contains an amplifier and delay line interconnected as shown in figure 8-58 to form an oscillator. The external connections between the delay line and the ampli-

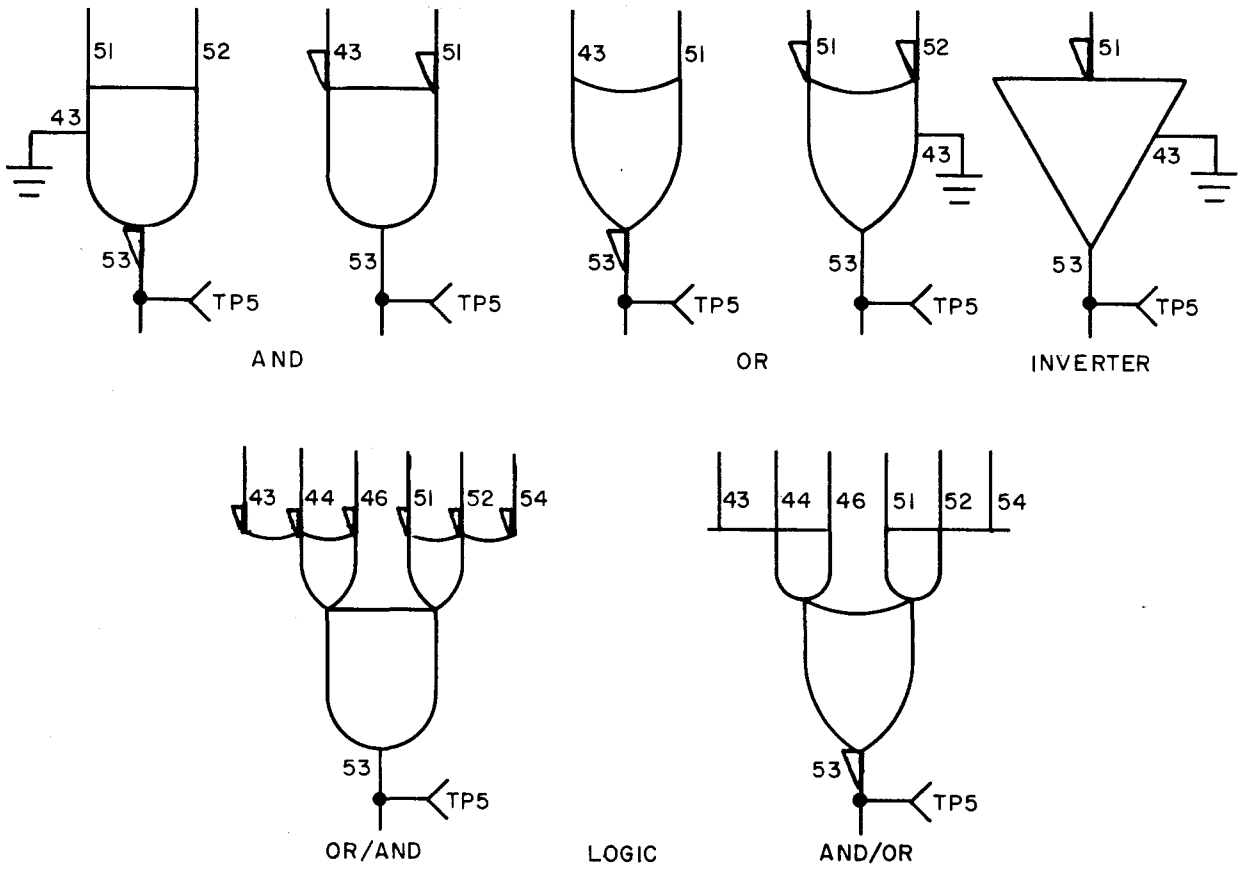


Figure 8-56. Amplifier Driver, Inverter, for Module 7500040

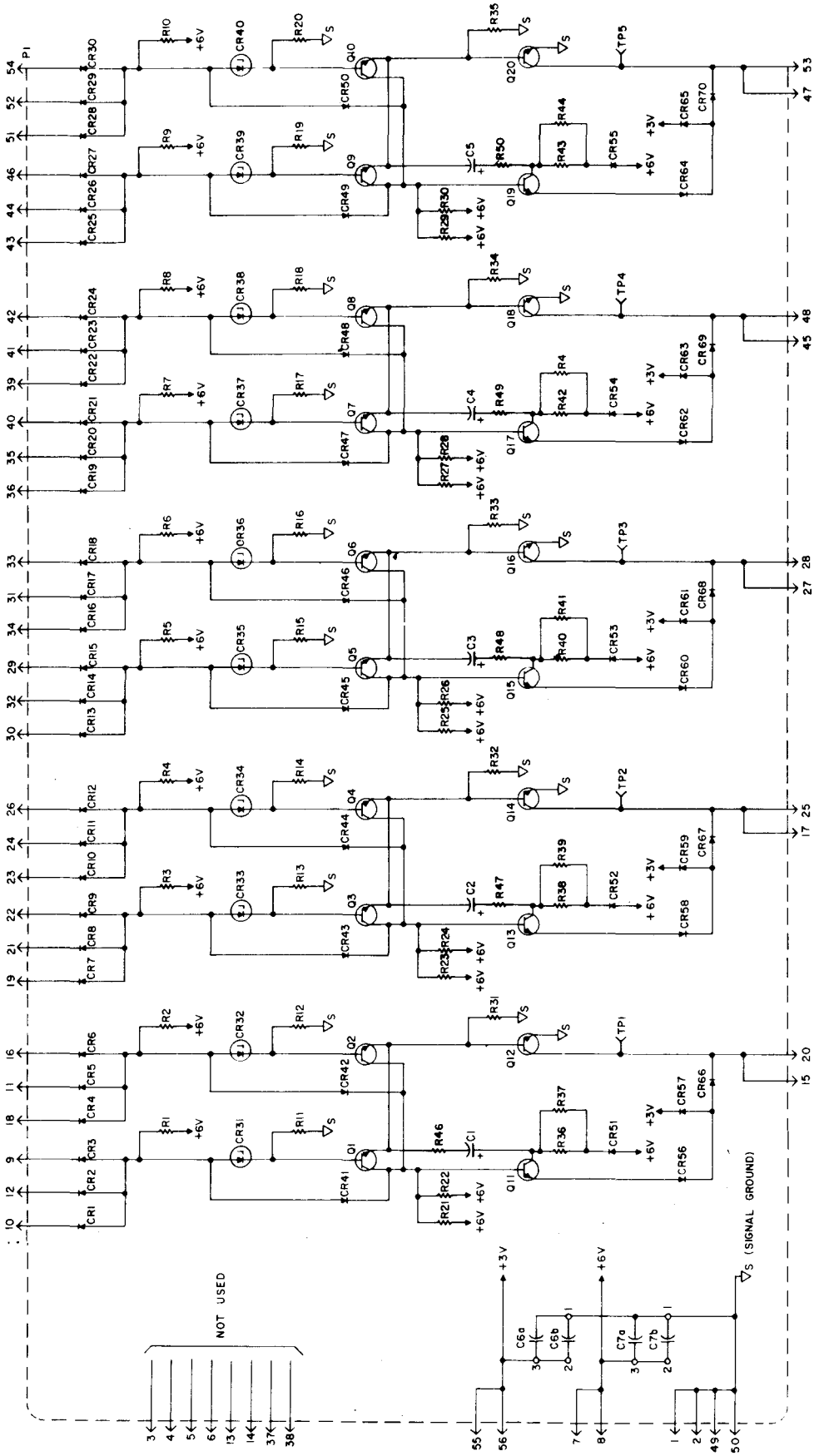


Figure 8-57. Module 7500040 Schematic Diagram

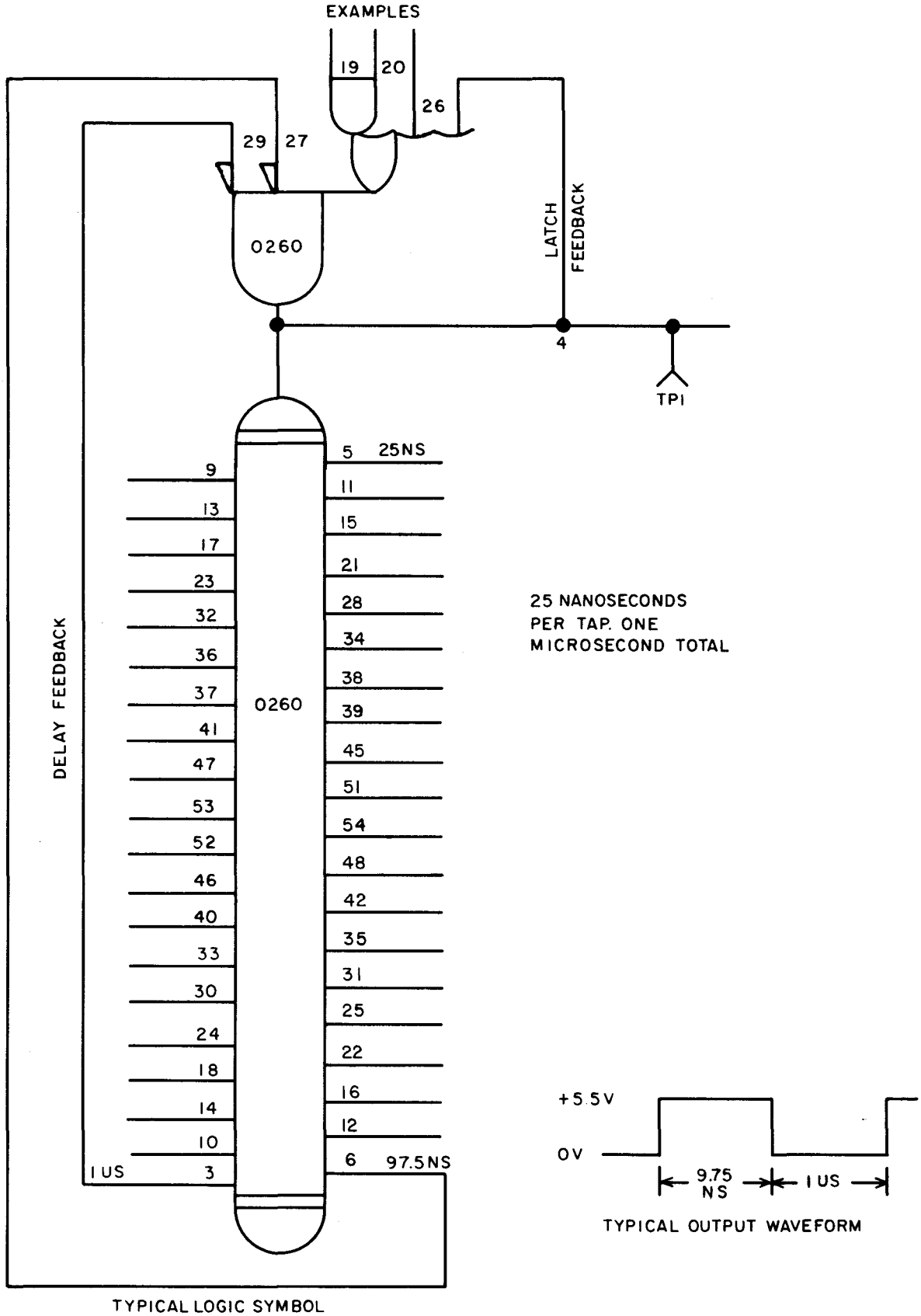


Figure 8-58. Oscillator, Clock Delay Line and Amplifier, Module 7500260

fier (pins 27 and 29) determine the cycle of the oscillator. The gate inputs (pins 19 and 20) and the individual input (pin 26) control the oscillator.

Figure 8-59 shows a schematic diagram for the 0260 module. In the quiescent state, the amplifier circuit is disabled (low input to pin 19 or 20 and pin 26). The oscillator is disabled by the low output of the amplifier and all delay line taps are low. The circuits remain in this state until a high input is applied to pins 19 and 20 or pin 26 of the amplifier. Then the output of the amplifier goes high (+5.5 volts) and this high begins propagating down the 1-microsecond delay line. The high output from the amplifier is also coupled back to the input. This enables the oscillator to complete a cycle even if the enabling signals (high input to pins 19 and 20 or pin 26) that started the oscillator are removed. When the high signal propagating down the delay line reaches pin 6 (975 nanoseconds later), the amplifier is disabled. The output from the amplifier goes low and a low begins to propagate down the delay line. When this low signal reaches pin 3 (1 microsecond later), the amplifier is again enabled provided the high input is still present at pins 19 and 20 or pin 26. Another oscillator cycle begins.

The waveform in figure 8-58 is dependent upon the interconnections between the amplifier and delay line. For example, the duration of the high level of the waveform is determined by the first delay line tap that connects to the amplifier. The duration of the low level is determined by the other delay line tap that connects to the amplifier. If the oscillator is disabled any time during the high level of the cycle, the oscillator completes the high level and then drops to the low level.

When the input to pin 26 is high or the inputs to pins 19 and 20 are high, the +5.5 volt level propagates through the delay line reaching an output pin every 25 nanoseconds.

The oscillator will continue to produce pulses until the enable inputs are removed. If the enable inputs are removed when the amplifier output is at the +5.5 volt level, feedback will hold the output until the +5.5 volt level of the cycle is complete.

(3) MODULE 7500280; EMITTER FOLLOWER, DRIVER AMPLIFIER. - This module contains three distinct circuit configurations: Four circuit groups consisting of a combination of regular discrete components comprising emitter-follower input driving a gated integrated inverter-output circuit (one part of a type 1001 flat-pack); four circuit groups consisting only of discrete components comprising emitter-follower inputs; and two type 1001 flat-packs. The logic descriptions are based on the logic symbols shown in figure 8-60. Figure 8-61 shows the schematic diagram.

For the emitter follower with gated output, a low input on the emitter-follower input pin 17 produces a high input to the associated AND inverter; a coincident high gating signal produces a low output from the circuit. By applying a constant high to the gated input pin (pin 27) the circuit can be used as a non-inverting amplifier. For example, a high input to pin 17 produces a high output from pin 30.

A high input on the emitter-follower pin 9 produces a low output (approximately 0 volts) on pin 10, and a low input produces a high output.

The integrated logic circuits perform AND or OR functions. If both inputs to the circuits are high, the output is low. If one input is low, the output is high.

(4) MODULE 7500340; VOLTAGE SENSOR. - This module contains two voltage detecting networks. Figure 8-62 shows logic symbols and figure 8-63 shows a schematic diagram of the voltage sensor circuits.

(5) MODULE 7500320; VOLTAGE REGULATOR, 3 TO 35 VOLTS. - The +15 volt power supply consists of a three-phase fullwave rectifier and a series regulator. The output of the rectifier is sampled by an error amplifier and compared to a reference voltage. Any difference between the reference and regulator output is amplified by four stages and used to drive the series regulator. An increase in the output of the +15v power supply results in less conduction of the series regulator to lower the output. A decrease in the output of the +15v power supply results in increased conduction of the series regulator to raise the output. The regulator circuits are on a 56-pin printed circuit module and the main power supply chassis.

Transistor Q1 is a constant current source. An increase in collector current causes a larger voltage drop across resistor R15, decreasing the forward bias and opposing the change in collector current. A decrease in the output voltage decreases the forward bias of transistor Q2b, the error amplifier. The collector current of transistor Q2b can decrease only if the collector current of transistor Q2a, the reference amplifier, increases. This causes a larger voltage drop across resistor R17, increasing the forward bias of transistor Q3. The increased voltage drop across transistor Q18 increases the forward bias of transistor Q4. The larger voltage drop across resistor R16 increases the forward bias of transistor Q5. The voltage drop across resistor R24 causes transistors Q6, Q7, Q8, Q9 and Q10 to conduct more. Consequently, transistor Q1, the series regulator, conducts more, raising the voltage. Potentiometer R6 adjusts the output of the regulator. Transistor Q1 is the series regulator. The reference voltage is obtained from a 6.2v Zener diode on the 0320 module. Zener diode CR37 provides overvoltage protection. Zener diode CR28 and resistor R14 are a preregulator for the reference voltage source. Zener diode CR30 and resistor R15 supply operating voltage for the final stages of the 0320 module.

A logic symbol and logic description are unnecessary and are not included. Figure 8-58A shows the schematic diagram for this module.

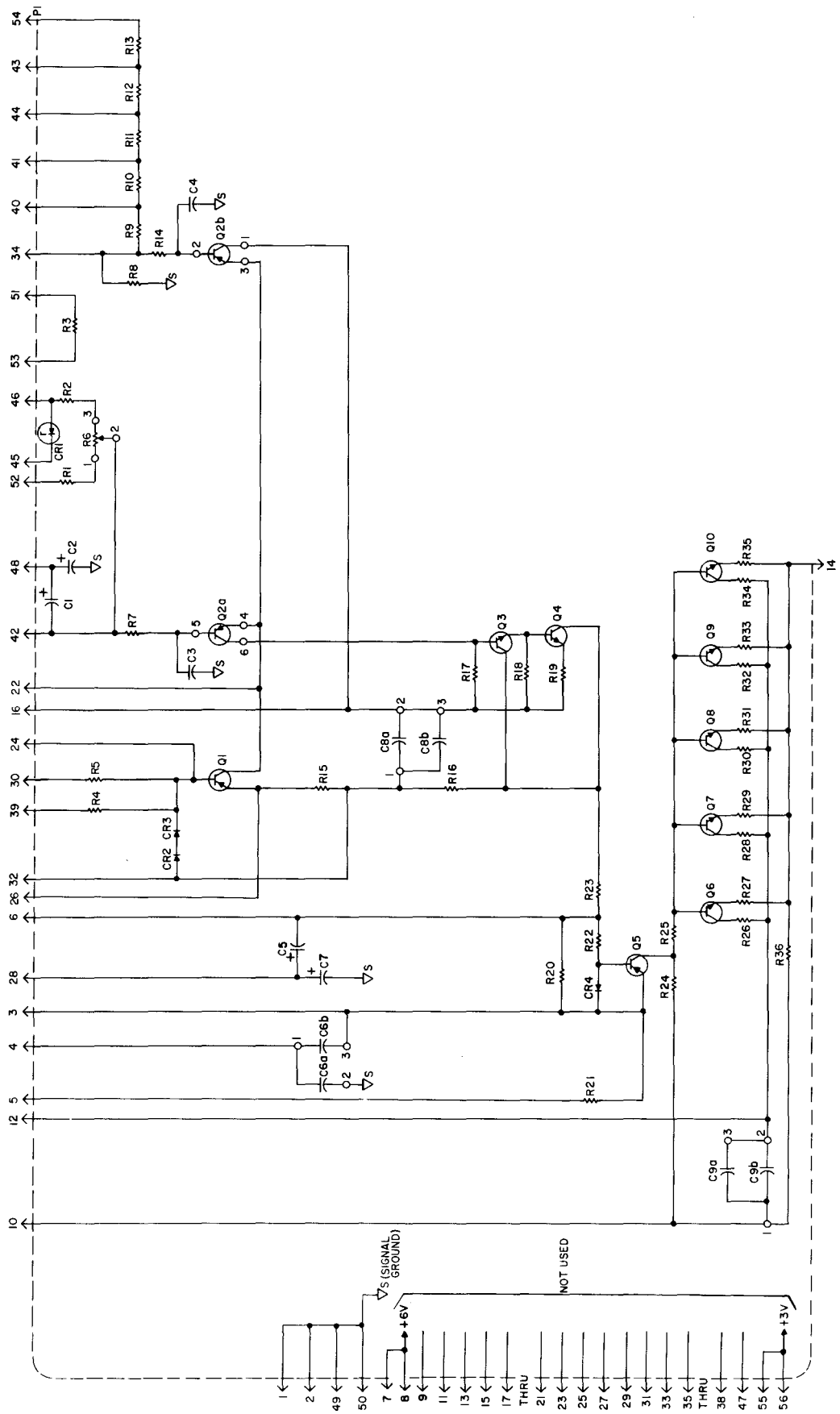


Figure 8-58A. Module 7500320 Schematic Diagram

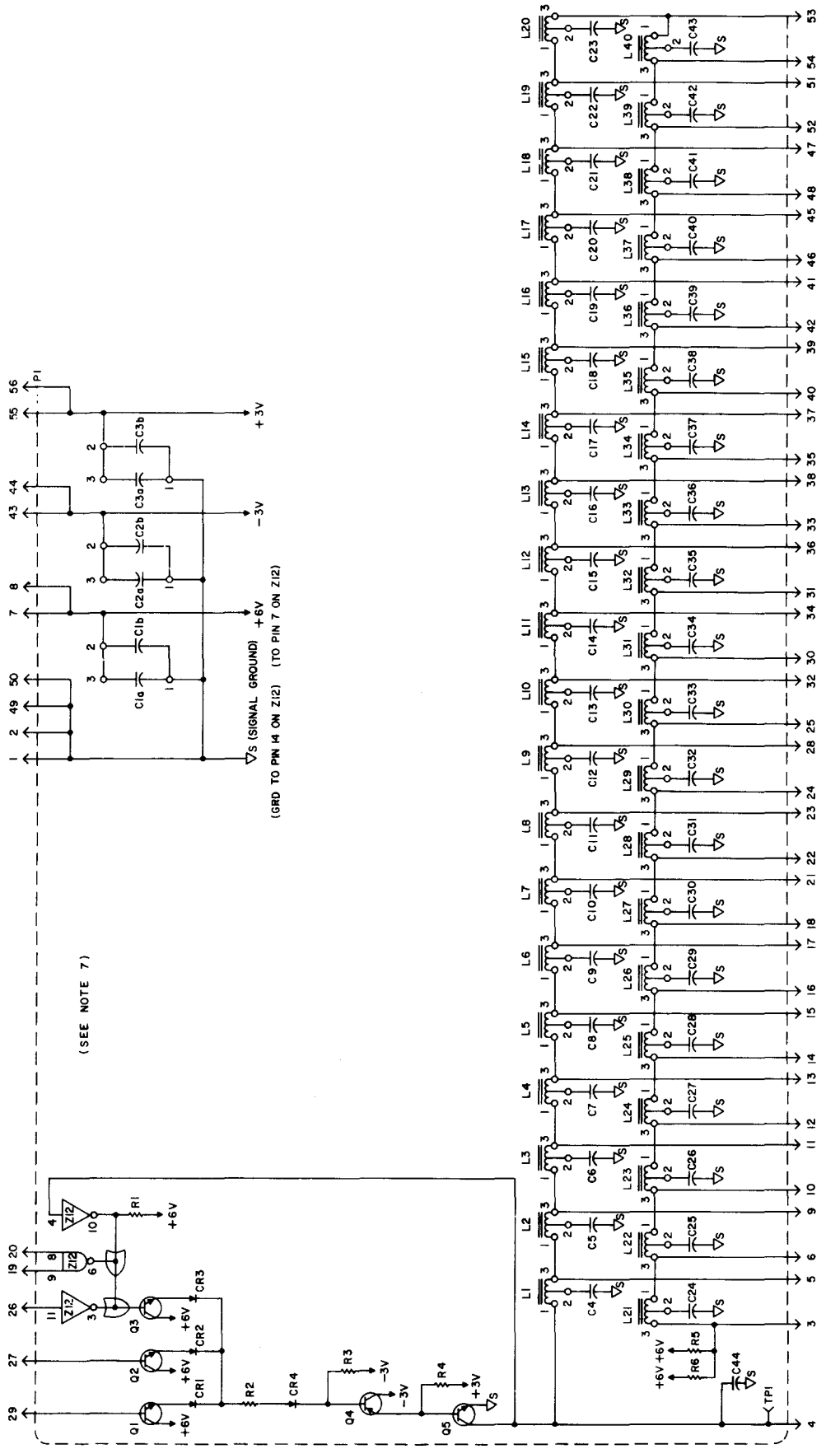


Figure 8-59. Module 7500260 Schematic Diagram

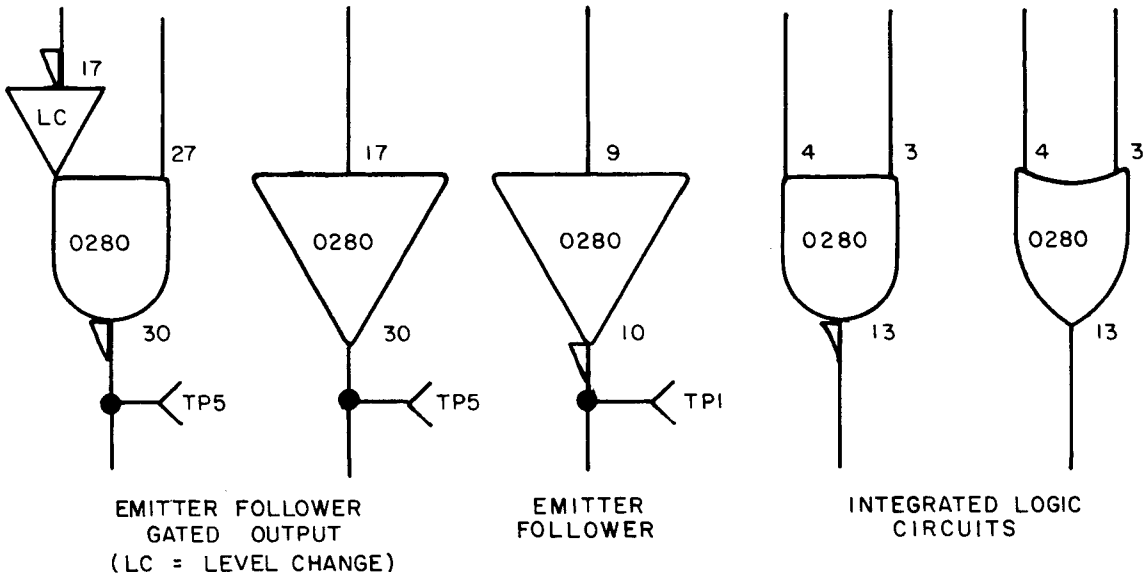


Figure 8-60. Emitter Follower, Driver Amplifier, Module 7500280

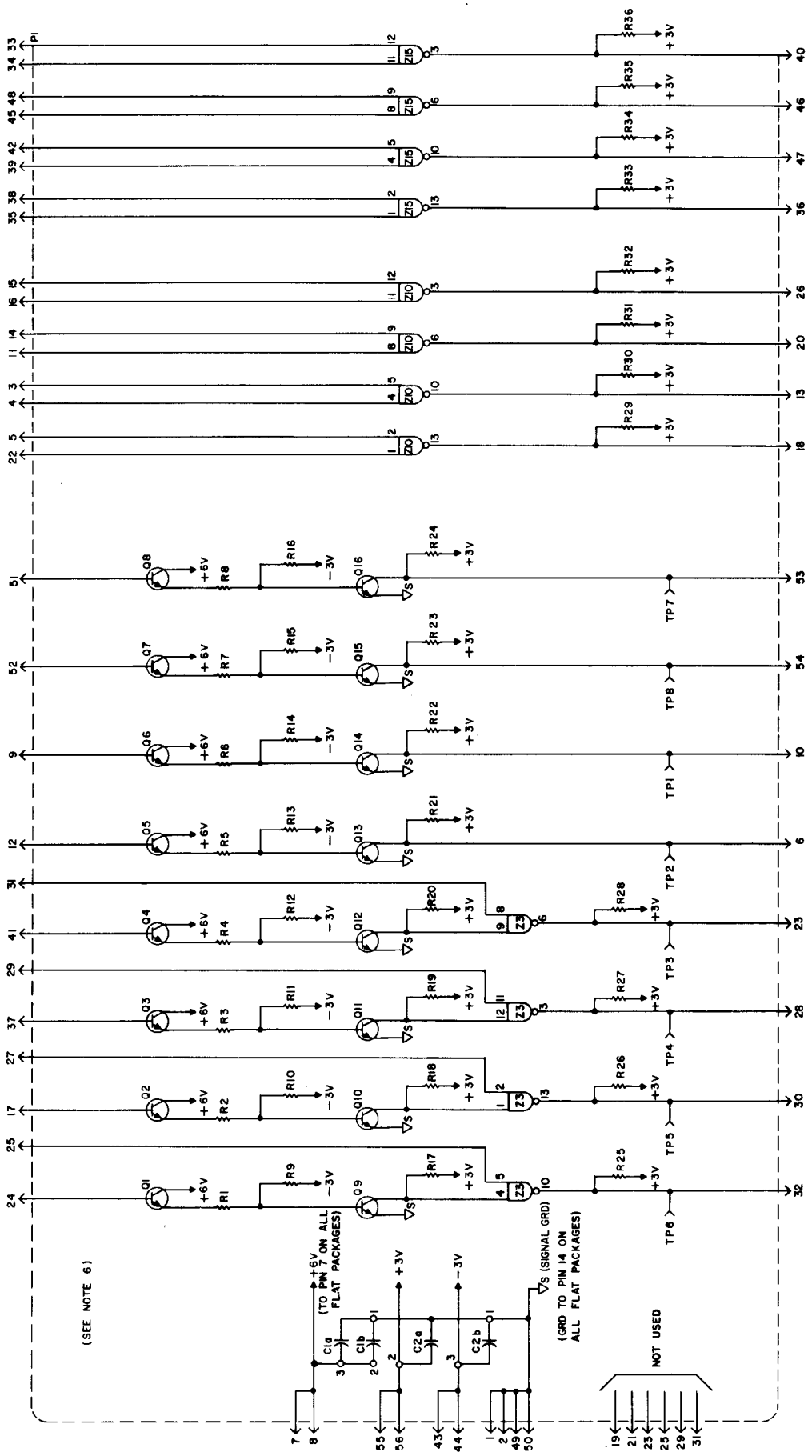
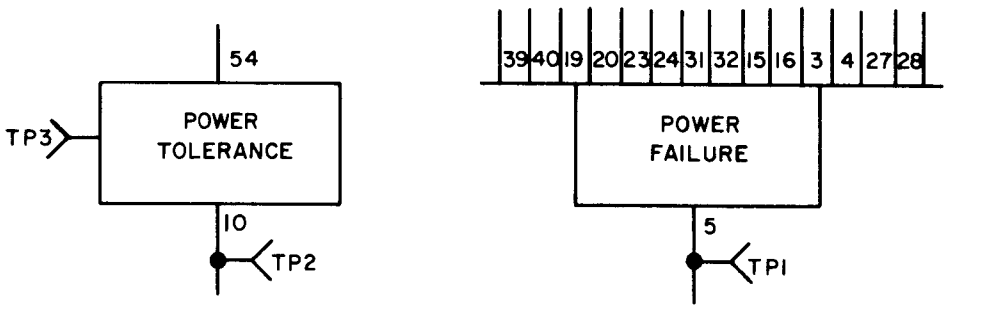
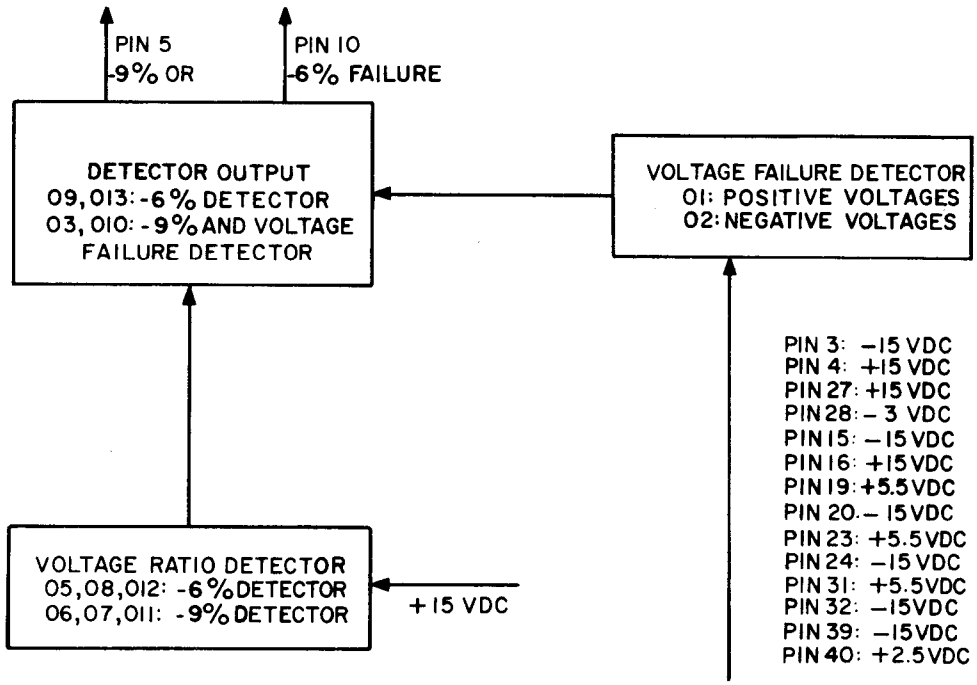


Figure 8-61. Module 7500280 Schematic Diagram



LOGIC SYMBOL



BLOCK
DIAGRAM

Figure 8-62. Voltage Sensor, Module 7500340

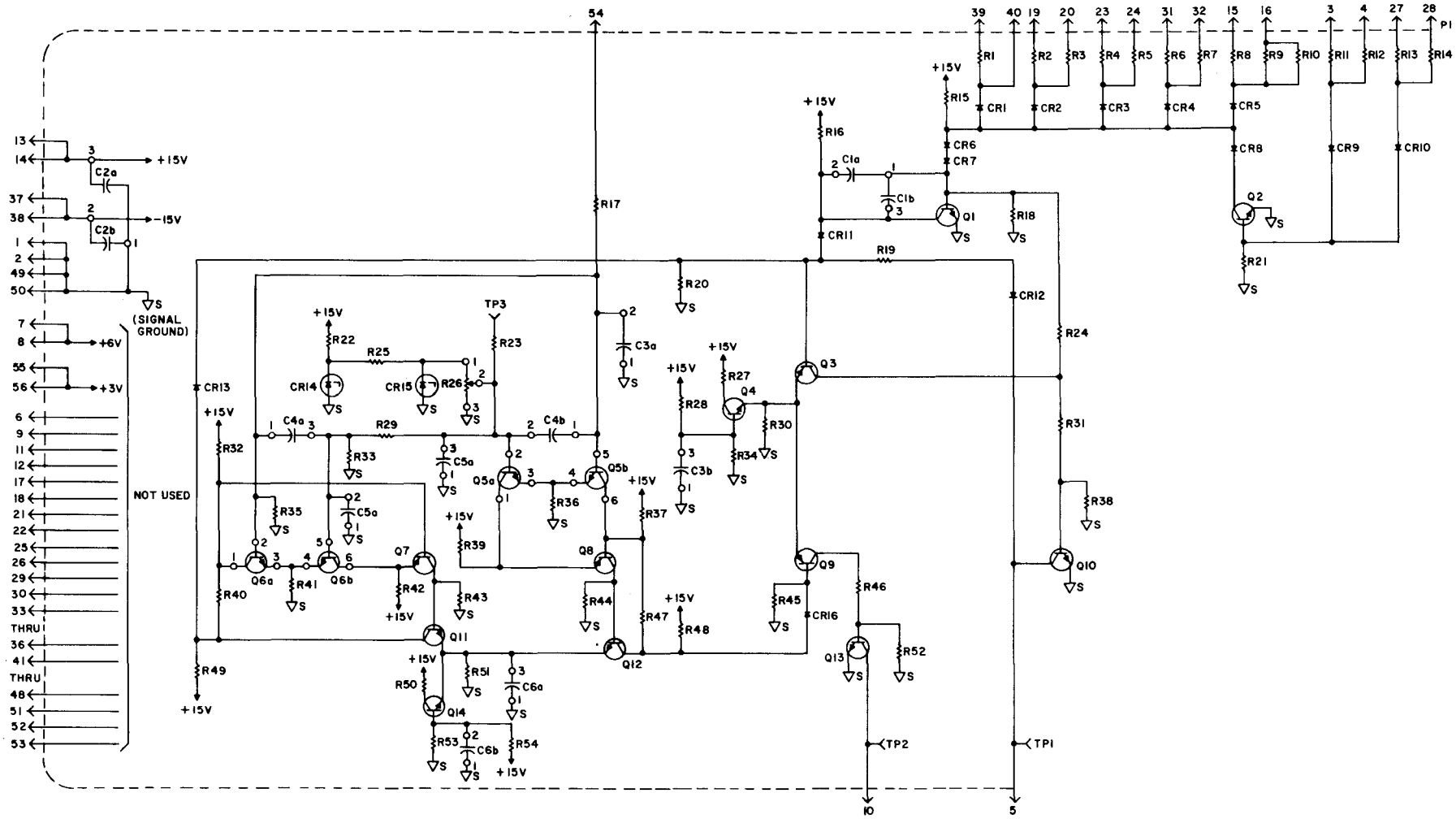


Figure 8-63. Module 7500340 Schematic Diagram

When the power tolerance circuit detects a loss of -6 percent in the +15 volt supply, the output goes high (pin 10). When the power failure sensor detects a failure in one of the -3, -15, +2.5, +5.5, +15 or -15 volt supplies or a loss of 9 percent in the +15 volt supply, the output goes high (pin 5).

(a) DETECTOR OUTPUT CIRCUIT GROUP. - Transistors Q9 and Q13 comprise the -6 percent detector output; transistors Q3 and Q10 comprise the -9 percent detector output. In both cases, normal operation occurs with transistors Q13 (-6 percent) and Q10 (-9 percent) conducting and supplying 100 ma control currents to the computer circuits connected to pins 10 and 5, respectively. The Q4 transistor stage is independent of -6 percent and -9 percent changes in the monitored +15 volt supply; the stage serves as a constant current source providing approximately +7.5 volts to the Q3 and Q9 emitters.

When a -6 percent decrease in the monitored +15 volt supply is detected, Q9 becomes biased to cutoff, turning off Q13 and removing the 100 ma control current from pin 10.

The -9 percent detector circuit is controlled from the diode OR configuration of diodes CR11 and CR13. When either a voltage failure is detected (CR11), or a failure of a -9 percent decrease in the monitored +15 volt supply is detected (CR13), transistor Q3 will be biased to cutoff, turning off Q10 and removing the 100 ma control current from pin 5.

(b) VOLTAGE FAILURE DETECTION GROUP. - Transistors Q1 and Q2 comprise voltage failure detectors, which monitor all power supply voltages with the exception of the +15 volt supply monitored by the voltage ratio detectors.

During normal operation, transistor Q1 is conducting and Q2 is biased to cutoff. If a failure occurs in the -3 or -15 volt supply, Q2 will become forward-biased, driving Q1 to cutoff and removing the forward bias from Q3. Transistors Q3 and Q10 will be turned off, thereby removing the 100 ma control current from pin 5. A voltage failure of any of the +2.5, +5.5 or -15-volt supplies will result in transistor Q1 being biased to cutoff; the resulting circuit operation is the same as just described.

(c) VOLTAGE RATIO DETECTOR GROUP. - Two similar voltage ratio detector circuits are used. Transistors Q5, Q8, and Q12 comprise the -6 percent ratio detector and Q6, Q7, and Q11 comprise the -9 percent ratio detector. Transistor Q14 is independent of -6 or -9 percent changes in the monitored +15 volt supply and serves as a constant current source for transistors Q11 and Q12.

For their respective circuit groups, the dual transistors, Q5 and Q6 comprise the differential circuits; Q8 and Q7 comprise the ratio detector stages, and Q12 and Q11 comprise the output amplifiers. Transistor Q12 drives the -6 percent detector output circuits and Q11 via OR diode CR13 drives the -9 percent detector output circuits.

A constant reference voltage is derived from the monitored +15 volt supply via resistors R22 and R25 and zener diodes CR14 and CR15; potentiometer R26 permits selecting the correct reference voltage. The reference voltage is applied to one side of the differential stages (Q5a, Q6b) in each ratio detector with transistor Q6b supplied from voltage divider R29, R33.

A voltage representative of the monitored +15 volt supply is applied to the other side of the differential stages from the junction of the voltage divider network or R17 and R35.

Assuming a -6 percent ratio change occurs, the Q5a-b conduction will bias Q8 to cutoff, removing the bias from Q12. With Q12 off, its positive collector voltage biases Q1 to cutoff, which in turn biases Q13 to cutoff, removing the 100 ma control current from pin 10.

Assuming a -9 percent ratio change occurs, the Q6a-b conduction will bias Q7 to cutoff, removing the bias from Q11. With Q11 off, its positive collector voltage via CR13 biases Q3 to cutoff, which in turn biases Q10 to cutoff, removing the 100 ma control current from pin 5.

A complete failure of the monitored +15 volt supply will result in both Q10 and Q13 being biased to cutoff, removing the control current from both pins 5 and 10.

(6) MODULE 7500400, BIPOLAR MEMORY SWITCH. - This module contains six bipolar memory switches. Each circuit is enabled by four inputs. Some of the input pins are common to several bipolar switches. Figure 8-64 shows the logic symbol of one bipolar switch, and figure 8-65 shows the schematic diagram.

When the four inputs (pins 17, 18, 20 and 28) are all high, the bipolar switch is turned on. Current flows from pin 6 to pin 9 or from pin 11 to pin 54. When one of the four inputs is low, the bipolar switch is turned off.

As used in the computer, two bipolar memory switches are selected for each read or write operation and together enable one drive line. Pins 6 and 54 are grounded. Each drive line is connected in series with two transformer secondaries, a read or write diode and each end is grounded by a bipolar memory switch. The transformers induce current in the drive lines. Read current flows in the opposite direction of write current.

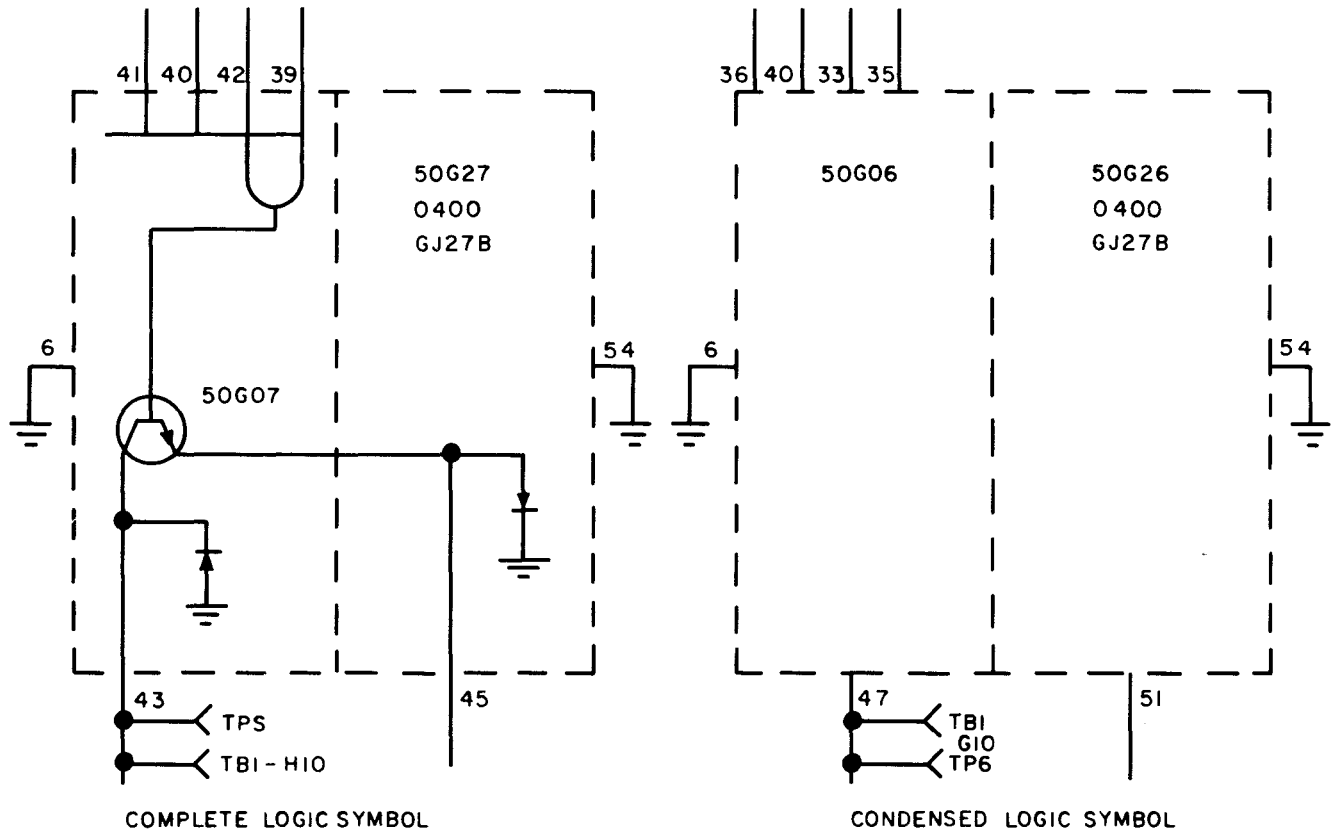


Figure 8-64. Logic Symbol of One Circuit on 7500400 Module

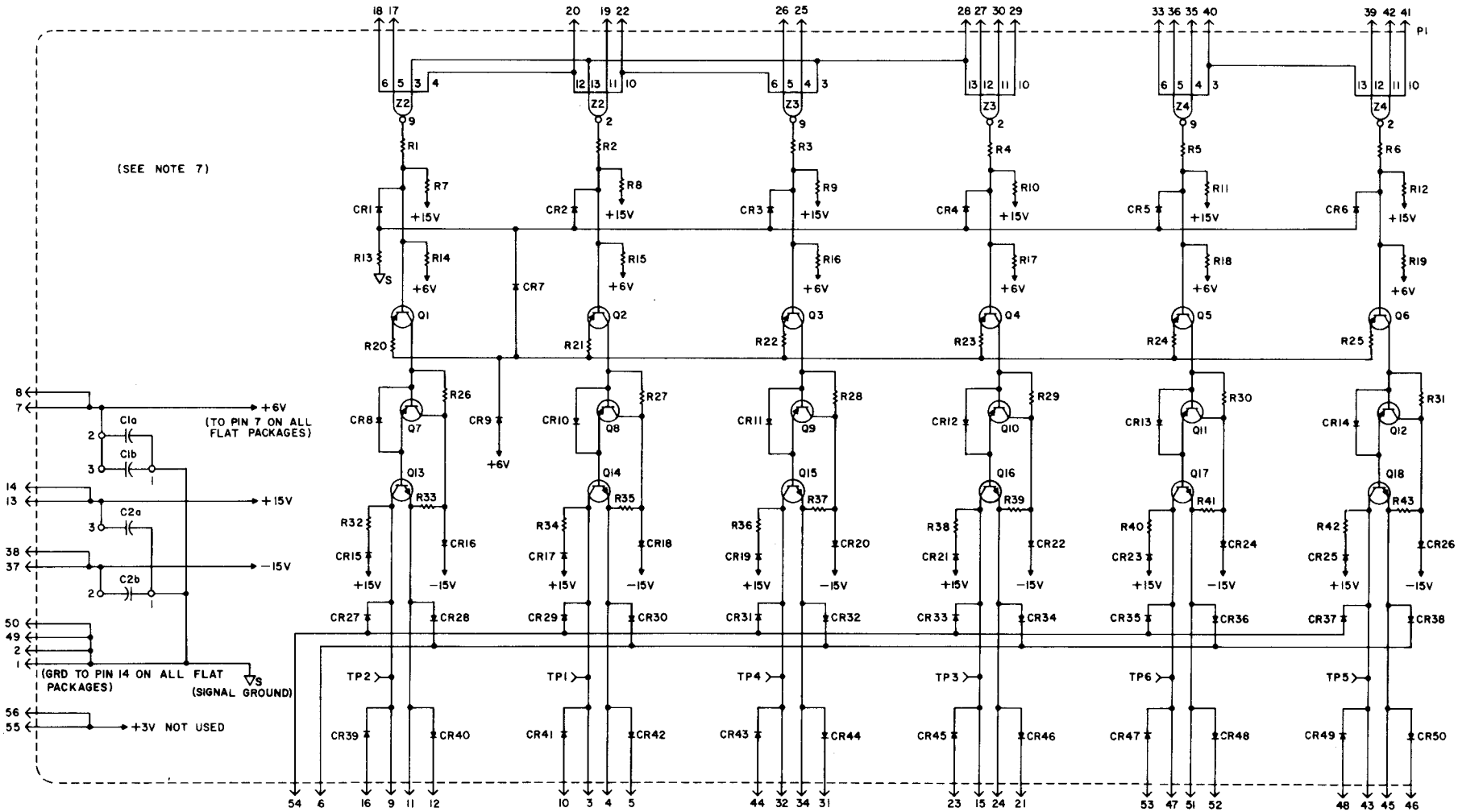


Figure 8-65. Module 7500400 Schematic Diagram

Current can flow from ground through pin 6, to pin 9 or from pin 11, and pin 54 to ground, depending upon the polarity of the voltage induced by the transformers.

(7) MODULE 7500420, READ/WRITE DIVERTER DRIVER. - This module contains one read/write diverter, a read diverter driver, and a write diverter driver. Read and write diverter drivers are identical. All three circuits are enabled by a common inverter.

(a) READ/WRITE DIVERTER. - Figure 8-66 shows the logic symbol and 8-67 shows the read/write diverter schematic. When input to pin 44 is low and input to pin 52 is high, the read/write diverter is enabled and no current flows through X or Y drive lines. When input to pin 44 is high or input to pin 52 is low, the read/write diverter is disabled and current flows through selected X or Y drive line.

(b) READ AND WRITE DIVERTER DRIVERS. - See figure 8-68 for the read and write diverter drivers logic symbol. When the input to pin 44 is low and the input to pin 48 is high, half of the drive current required by an X or Y drive line is induced in one of the secondary windings of the output transformer. The selected secondary is part of a complete circuit at this time, while the other seven secondaries are open-circuited by bipolar switches.

When the input to pin 44 is high or the input to pin 48 is low, no drive current is induced in one of the secondaries.

No current flows in the seven secondaries which are not enabled by the bipolar switches. Half of the current required by a drive line flows in the enabled secondary.

(8) MODULE 7500430, READ/WRITE SELECTION MATRIX TRANSFORMER ASSEMBLY. - This module contains two identical circuits. Each circuit has three enable inputs. The output is half of the current required by an X or Y drive line and is taken from one of the eight secondaries on the output transformer. External circuits are wired so that only one of the secondaries draws current at a time.

Pairs of secondaries from the two identical circuits are connected through isolation diodes to shared pins on the connector. This conserves output pins so that two circuits can be built on one 56-pin module.

Figure 8-69 shows the logic symbol of one of the circuits, and figure 8-70 shows the schematic diagram.

When the inputs to pins 47, 48, and 52 are high, half of the drive current required by an X or Y drive line is induced in one of the secondaries of the output transformer. When any of the three inputs is low, no drive current is induced in any of the secondaries.

When pins 47, 48, and 52 are high, pin 9 of Z10 is low. Transistor Q3 is forward biased and turns on, causing current to flow through the primary of transformer T1. Current flows in the secondary of T1 and turns on Q1.

As wired in the computer, pins 25 and 36 are connected to the read and write diverter driver transformer primary circuits and pin 3 is connected to a regulator.

When pins 47, 48, and 52 are high, a read or write diverter driver is enabled, and the read/write diverter is disabled.

Only one of the eight secondaries is enabled by the combined action of two bipolar switches. The other seven secondaries are disabled and open circuited by fourteen other bipolar switches. Half of the current required by an X or Y drive line is

induced in the selected secondary, which is connected in series with read or write diverter driver transformer secondary, a read or write diode, two bipolar switches, and an X or Y drive line.

(9) MODULE 7500650, SENSE AND INHIBIT AMPLIFIER. - This module contains inhibit drivers, sense amplifiers, one bit of the Z register and current overload detection circuits. Figure 8-71 shows a condensed logic symbol, and figure 8-72 shows a schematic diagram.

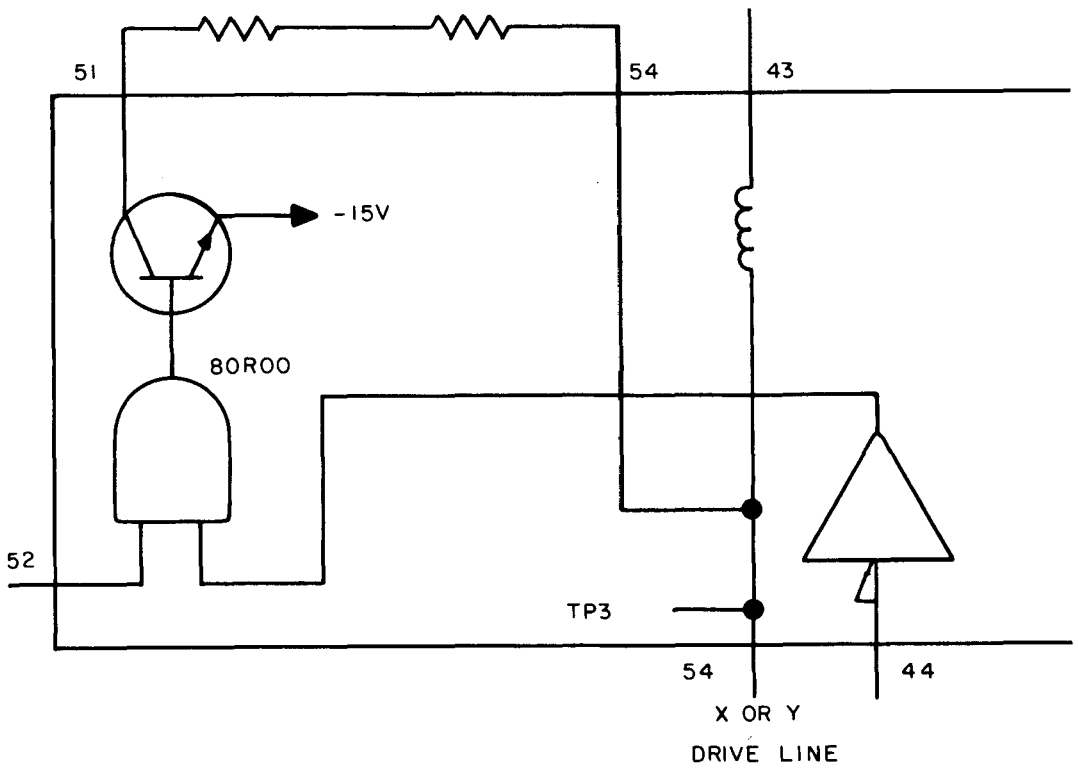
(a) INHIBIT DRIVER. - This module contains four inhibit drivers, each of which supplies inhibit current to one of 32 planes in one of four stacks. Each inhibit circuit is enabled by one AND gate. Only one AND gate is enabled at a time. This occurs when a high is applied to one of the stack select inputs (pins 36, 40, 41, or 42), if the overload flip-flop is set, no power failure (pin 52 high), corresponding bit of Z register is not set, and input 35 is high.

All inhibit drivers are disabled when input pin 35 is low, overload flip-flop is clear, a power failure exists, or corresponding bit of Z register is set.

A sense/inhibit line from pin 23 passes through half of the 4096 cores on one memory plane and returns to pins 25 and 26. A second sense/inhibit line from pin 24 passes through the other half of the cores and also returns to pins 25 and 26.

Pin 52 is high whenever all power supply voltages are normal. When pin 52 goes low, four inhibit drivers are disabled. After a power failure condition, computer power must be turned off and reapplied to enable the four AND gates comprising Z4.

(b) SENSE AMPLIFIER. - When the coincidence current switches one core in a plane of one of four stacks during a read cycle (as sensed by input pins 23 and 24, 19 and 20, 15 and 16; or 9 and 10), the output pin 32 will be positive. When no core is switched, the output pin 32 will be less positive.



LOGIC SYMBOL

Figure 8-66. Logic Symbol of Read/Write Diverter on Module 7500420

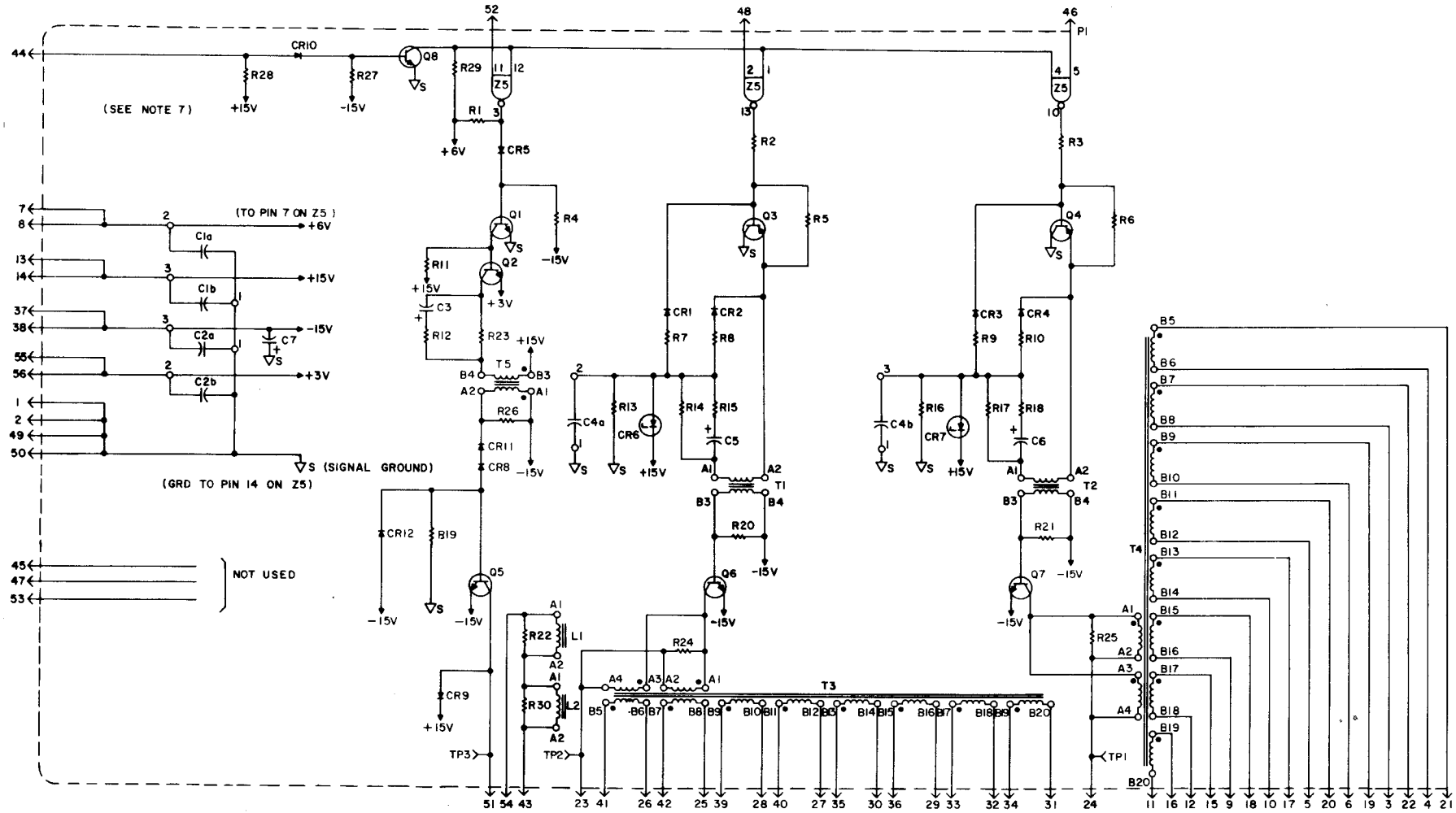
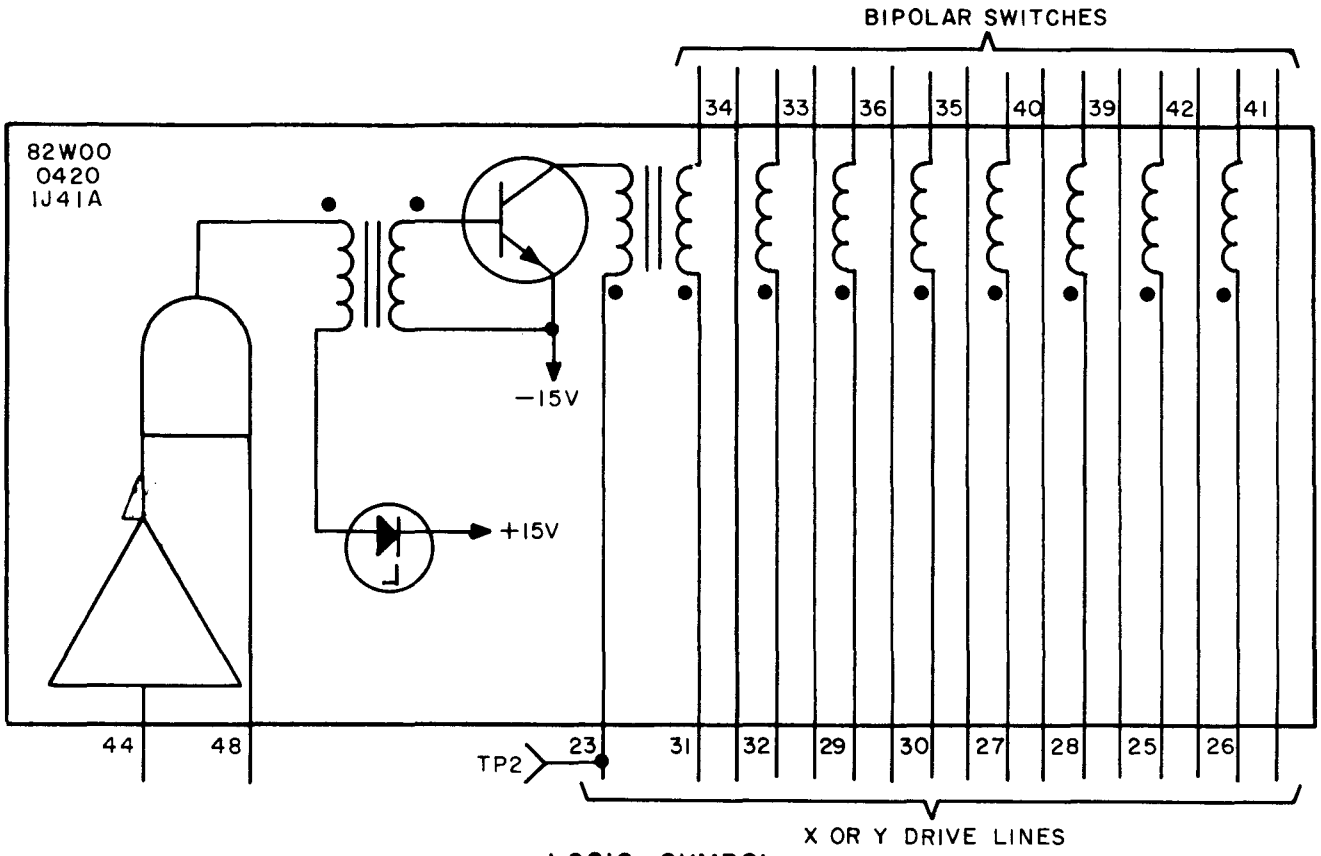


Figure 8-67. Module 7500420 Schematic Diagram



LOGIC SYMBOL

Figure 8-68. Logic Symbol of One Diverter Driver Module 7500420

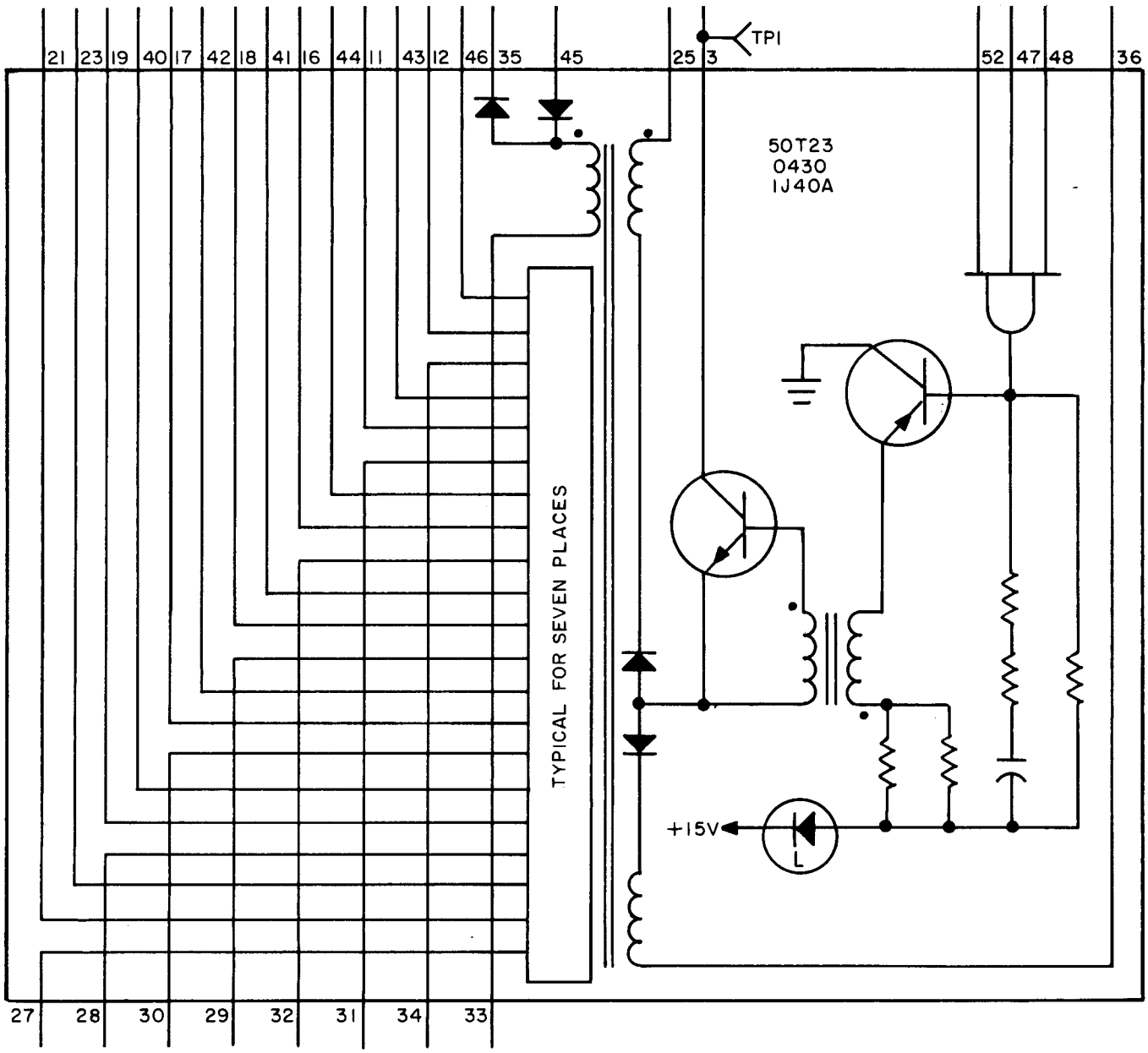
Input pins 23 and 24 are connected to one end of a sense/inhibit line, which passes through the 4096 memory cores on a single plane. Each of the other three pairs of input pins 19 and 20, 15 and 16, and 9 and 10 are similarly connected to a single plane in a different stack. Other circuits in the memory select one of the four stacks and pulse one X line and one Y line when data is read from the memory. The content of the single core at the junction of the selected X and Y lines of the selected stack is applied across one of the pairs of input pins. If the selected core does not switch, no difference in voltage is developed across the two input pins. The noise in each sense/inhibit line is equal and cancels. If the selected core is switched, a difference in voltage (approximately 30 millivolts) is developed across the two input pins. One sense/inhibit line carries only noise and the other carries a pulse generated by the switched core.

One flip-flop is associated with four sense amplifiers and four inhibit drivers.

The Z register flip-flop sets when the sense amplifier detects a core has switched during a read cycle (pin 34 and pin 48 high) or during the first portion of a write cycle when a bit is to be stored (pin 43 and pin 44 high). It clears when pin 47 goes low.

When the flip-flop is clear and pin 53 is high, output pin 43 will be low.

When the flip-flop is set, the inhibit drivers are disabled so that during the write cycle the selected core is allowed to switch.



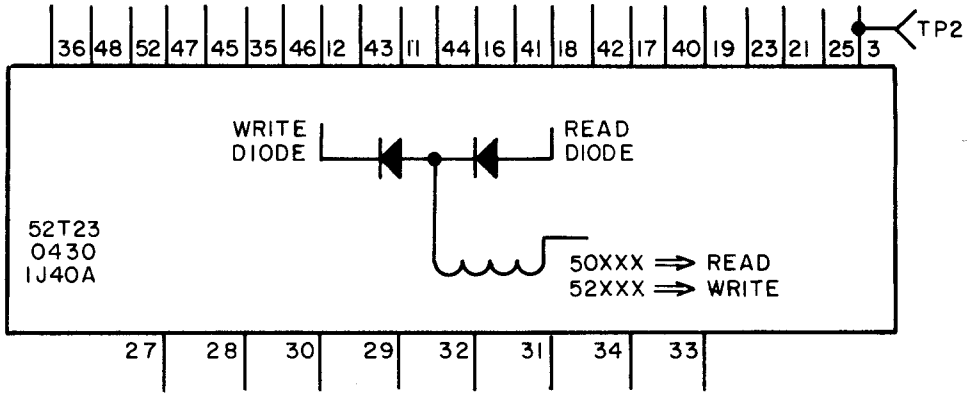


Figure 8-69. Logic Symbol of One Circuit on 7500430 Module

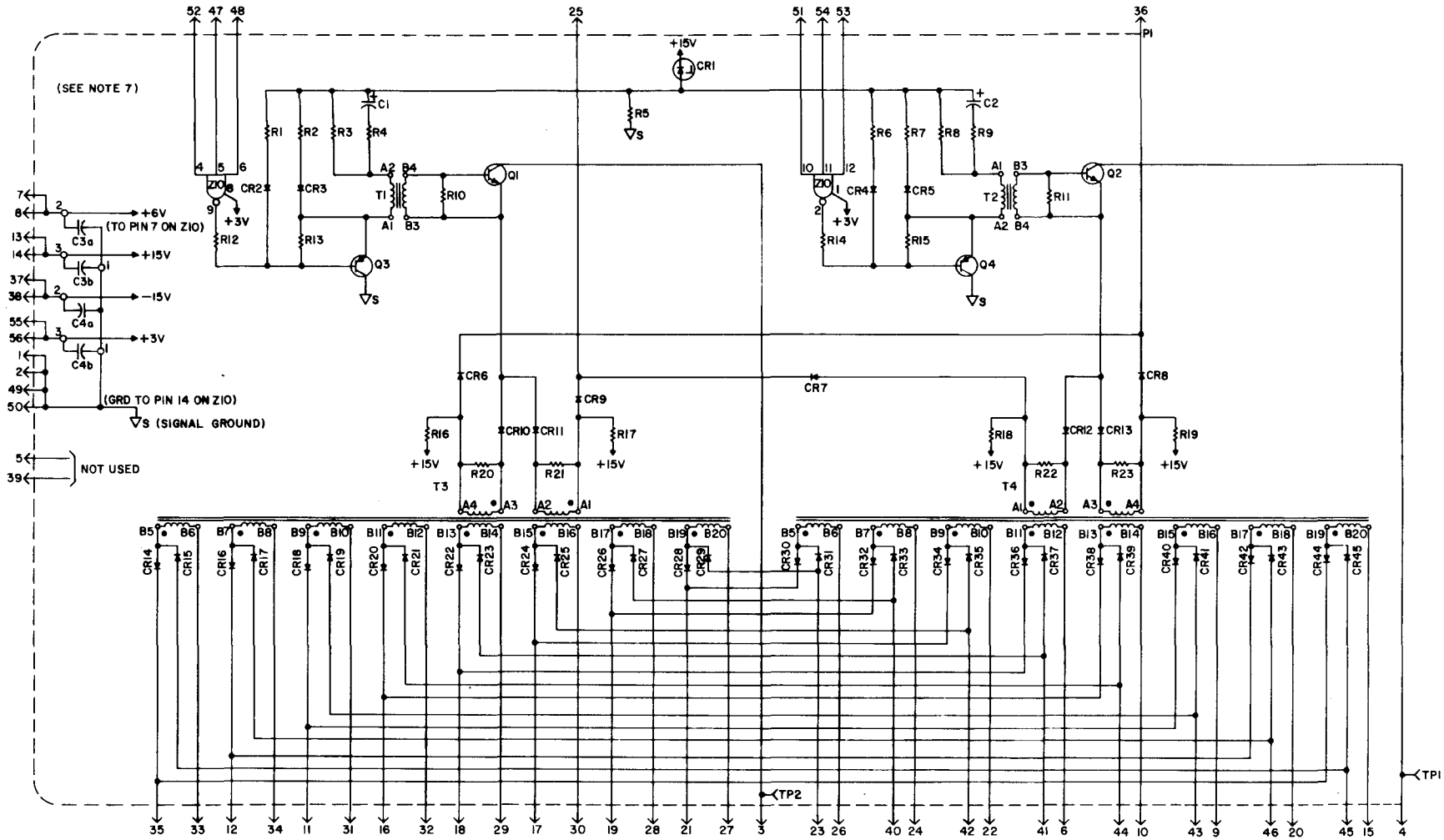
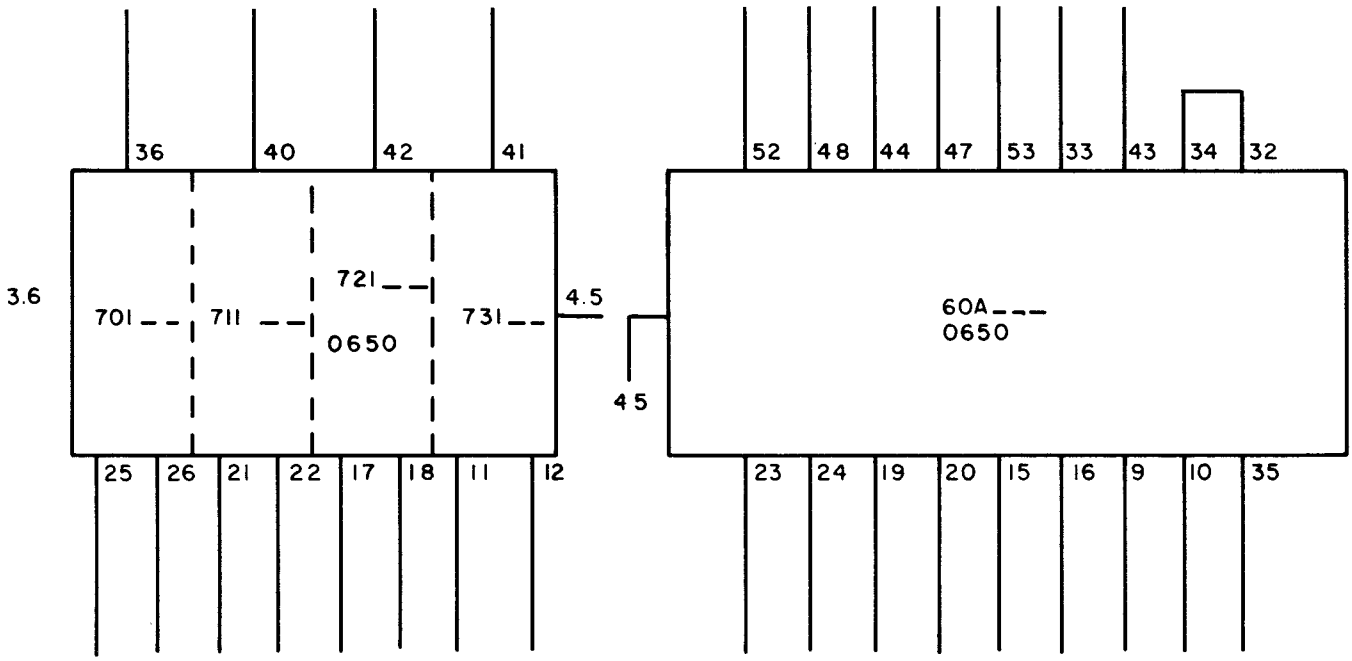


Figure 8-70. Module 7500430 Schematic Diagram



CONDENSED LOGIC DIAGRAM

Figure 8-71. Logic Symbol of Sense and Inhibit Amplifier on 7500650 Module

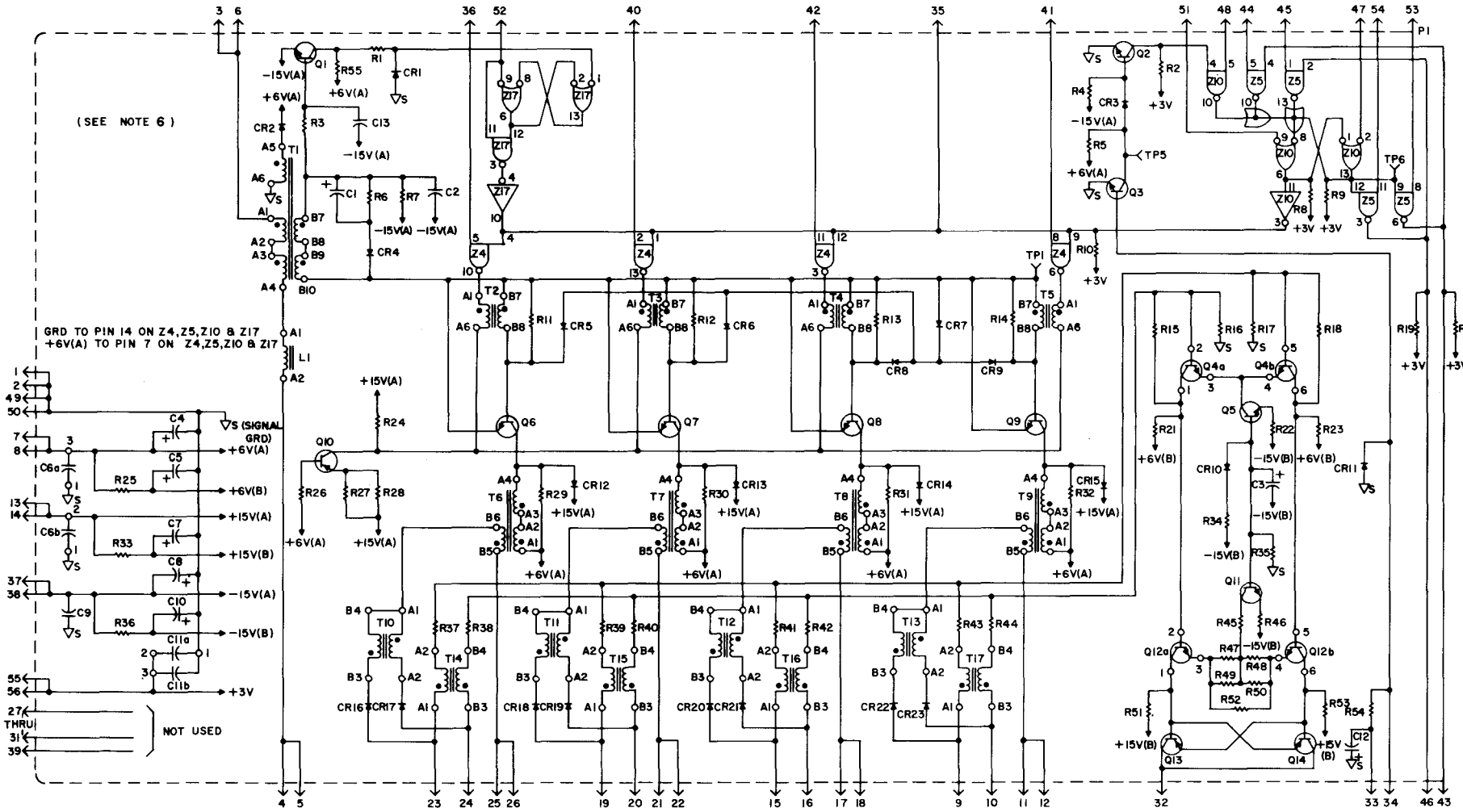


Figure 8-72. Module 7500650 Schematic Diagram

(10) MODULE 7500660; CAPACITOR-DIODE ASSEMBLY. - This module contains a series of capacitors and diodes which are required by other modules in the computer logic. No logic symbol is required for these components. Figure 8-73 shows the schematic diagram of this module.

(11) MODULE 7500670; CAPACITOR ASSEMBLY. - This module contains five capacitive filters. Figure 8-74 shows the schematic diagram of one of the networks. Each capacitor is coupled to two voltage pins and to three resistors. Pins 7 and 8 are standard -5.5V pins, pins 13 and 14 - +15V, pins 37 and 38 - -15V, pins 43 and 44 - -3V, and pins 55 and 56 - +2.5V. When the module is in place on a chassis, the capacitors provide additional filtering; inhibiting spurious signals from being received and transmitted by the voltage pins of the other modules on the chassis. The resistors isolate the test points and output pins from the voltage source for short circuit protection. The output pins are normally used for voltage supply to voltage sensor circuits such as the 0340 module.

(12) MODULE 7500760; AMPLIFIER, LEVEL CHANGER. - This module contains four inverters, two OR circuits, and eight amplifiers. Figure 8-76 shows the schematic diagram for this module.

A high input on either pin 5, 11, 20 or 22, will produce a low output on either pin 18, 24, 10 or 12. A high input on either pin 33 or 34 or on pin 51 or 54 will produce a low output on either pin 26 or 46.

A high input of +3.0 volts on either pin 27 or 30 will produce an output of 0.0 volt on pin 41. A low input of 0.0 volt on both pins 27 and 30 will produce an output of -4.5 volts. This is typical of the eight amplifier circuits. Figure 8-75 shows the logic symbol for these circuits.

(13) MODULE 7500780; VOLTAGE AND CURRENT REGULATOR. - This module contains three identical current regulators and one voltage regulator. Logic descriptions of these circuits are unnecessary and not included. Figure 8-75 shows the logic symbol for one of the three current regulators and also includes the external circuits wired to the regulator.

(14) MODULE 7500900; AMPLIFIER, DRIVER-LOGIC, NONINVERTING. - This module contains ten identical circuits which are represented by the logic symbols shown in figure 8-78. If a high input of +2.5 volts is applied to either pin 31 or 32, a high output of +2.5 volts will appear on both pins 21 and 22. If a low input of 0.0 volt appears on both 31 and 32, a low output will appear on both pins 21 and 22.

This circuit is normally used to drive nine logic elements as a noninverting logic driver. Figure 8-79 shows the schematic diagram for this module.

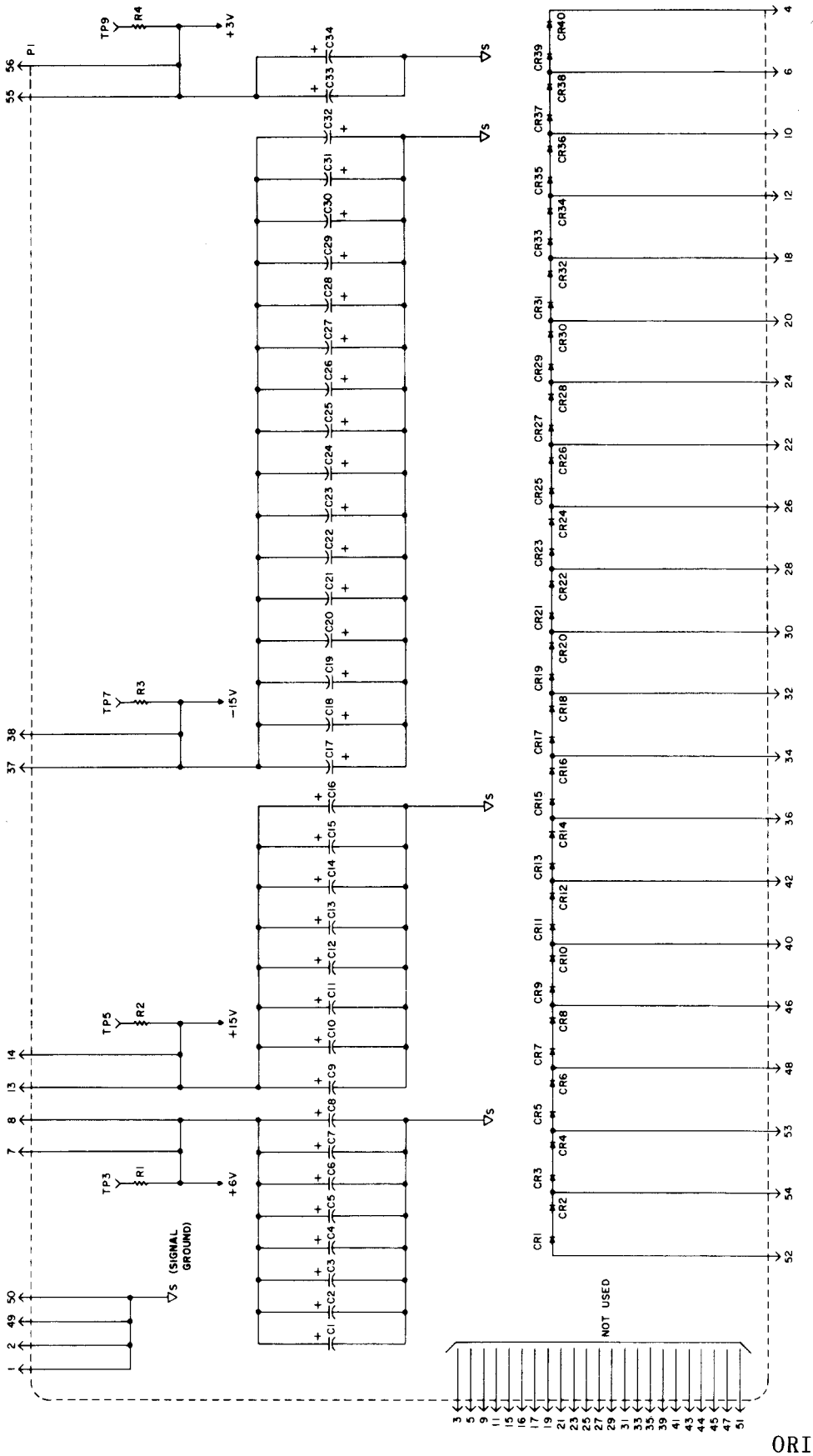


Figure 8-73. Capacitor-Diode Assembly, 7500660

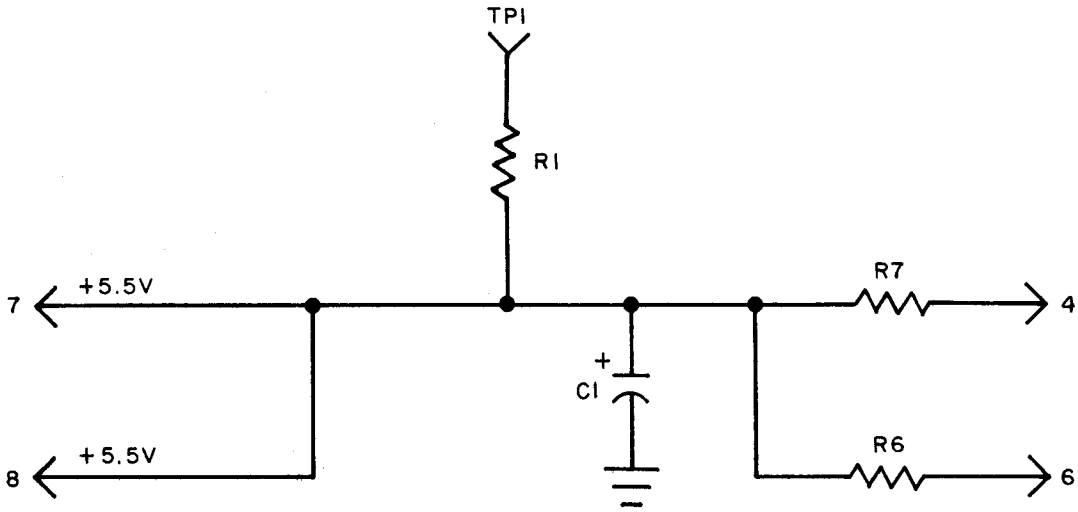


Figure 8-74. Module 7500670 Schematic Diagram

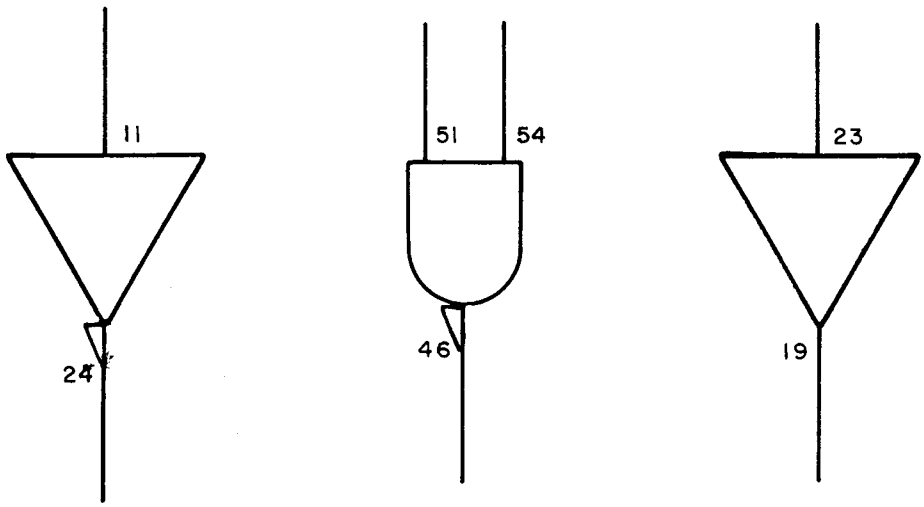


Figure 8-75. Logic Symbol of Level Changer Amplifier, Module 7500760

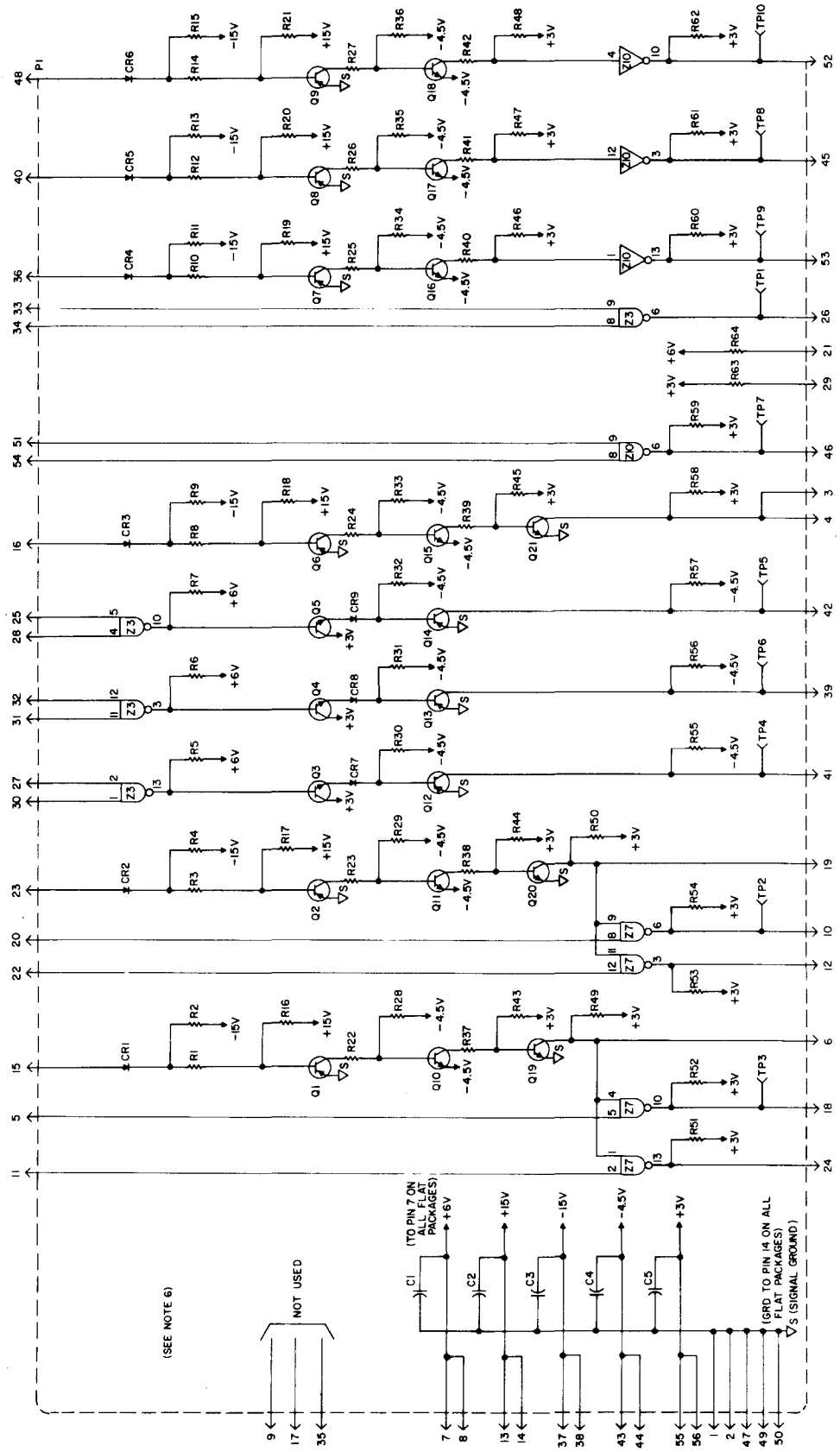


Figure 8-76. Module 7500760 Schematic Diagram

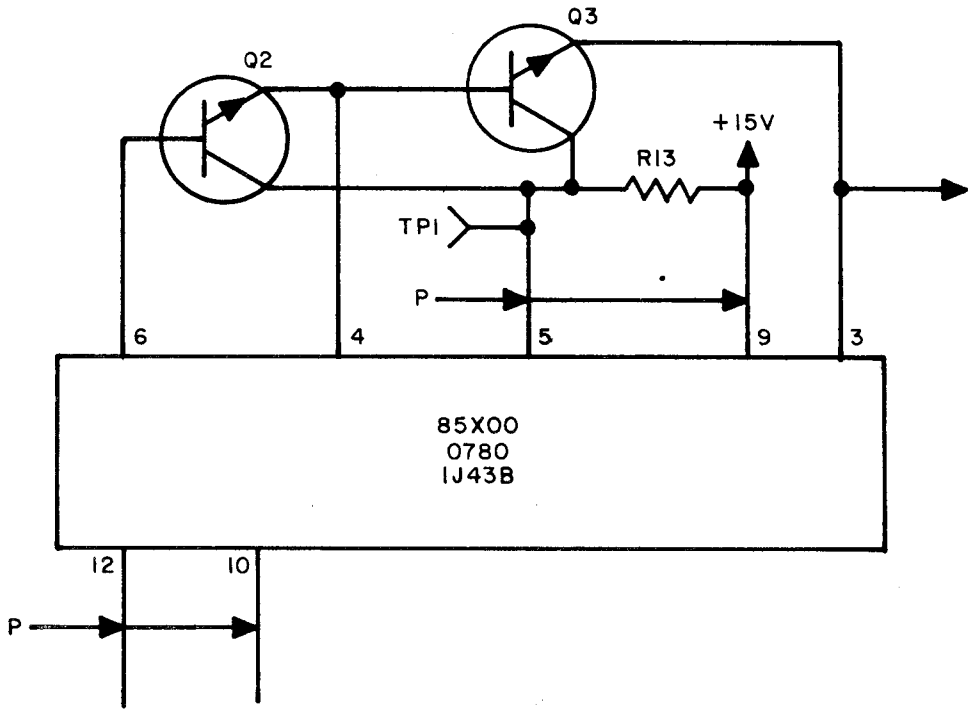


Figure 8-77. Logic Symbol of Current Regulator Circuit on 7500780 Module

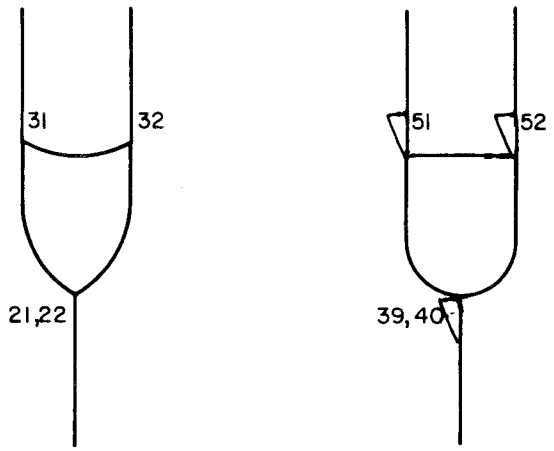


Figure 8-78. Logic Symbol of Noninverting Amplifier Driver, Module 7500900

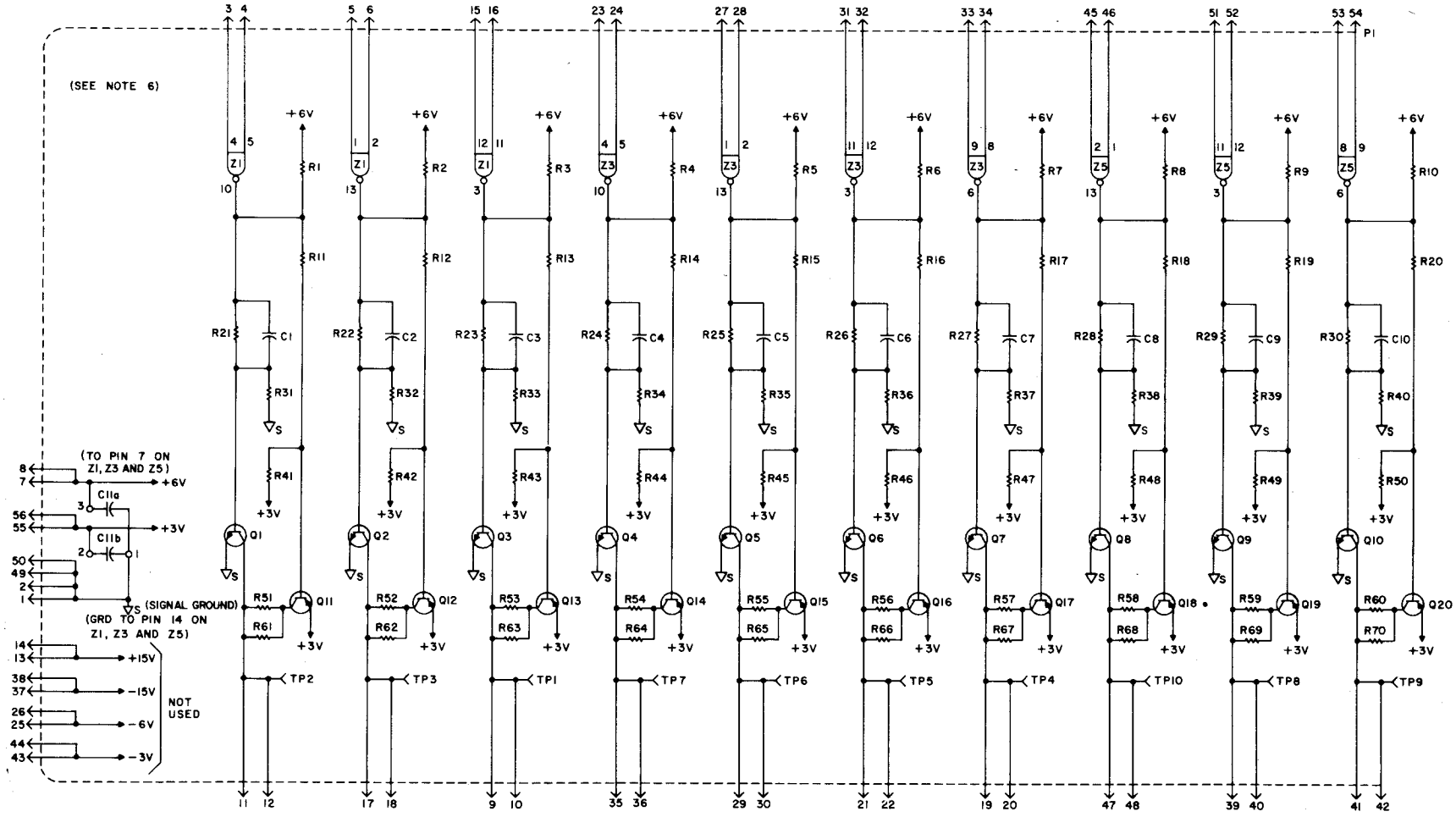


Figure 8-79. Amplifier, Driver-Logic, Noninverting, Module 7500900