SECTION 7 - MEMORY SECTION

7.1. GENERAL DESCRIPTION OF MAIN MEMORY

7.1-1. OBJECTIVES

To present the general description of main memory.

7.1-2. INTRODUCTION

Main memory has $65,536_{10}$ locations for storage of 18-bit words. The storage element is ferrite cores. Cycle time is 2 microseconds. The control and bootstrap memory addresses are not usable.

7.1-3. REFERENCES

a. UNIVAC 1219 Technical Manual, Volume I, Paragraph 1-5f (1).

b. UNIVAC 1219 Technical Manual, Volume II, Section 9 (logic diagrams).

7.1-4. INFORMATION

a. Storage Element.

1. Core Description. As storage elements, the main memory uses magnetic cores. These cores are made of ferrite material and can be magnetized. The direction of magnetization represents the information stored, a binary 1 or 0. There is one core for each bit position of each word location in memory. Refer to figure 7.1-1 for an illustration of one core.

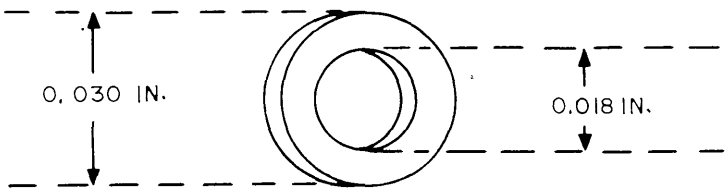


Figure 7.1-1. One Magenetic Core

2. Core Theory. The core is magnetized by passing approximately 500 ma through a wire which is threaded through the core. The direction of the current flow determines the direction of magnetization. This current is referred to as drive current and is carried by a drive line.

In the 1219 Computer, the drive current is produced from the resultant of currents carried by two drive lines which pass through the core. Refer to figure 7.1-2 for an illustration.

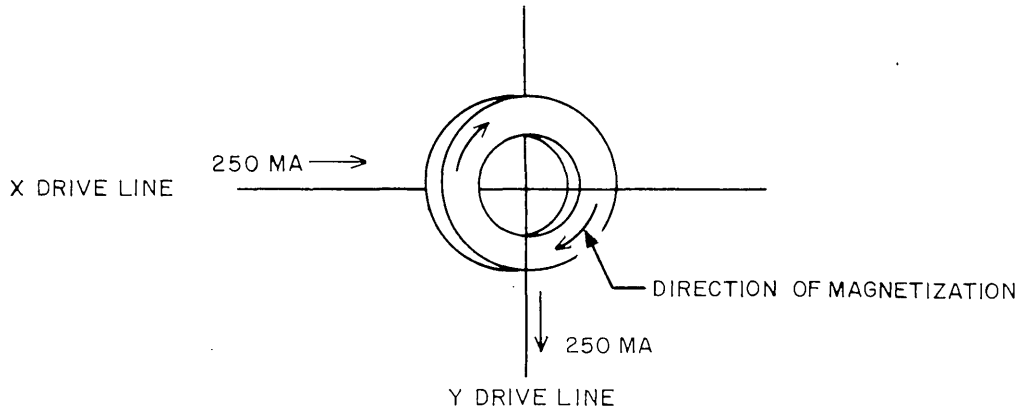


Figure 7.1-2. Core With X And Y Drive Lines

The currents aid each other so as to magnetize the core in the direction shown. This direction represents either a binary 1 or 0. If both currents are reversed, the direction of magnetization is switched.

If only one drive line is activated with current, the state of the core is not appreciably affected because the amount of current is not enough to switch the direction of magnetization.

Using the X and Y drive line principle, a matrix of cores is used with several X and Y lines. One X and one Y line are activated. The core which is located at their intersection is the only core affected. This core is referred to as the selected core. Refer to figure 7.1-3 for an illustration.

Figure 7.1-3 shows one core being selected or magnetized by the drive currents. So as to store complete 18-bit words, there are 18 separate core matrices referred to as bit planes. During a memory operation, one core on each of the bit planes is selected to formulate the 18-bit word.

b. Write Operation. The operation which stores information in memory is referred to as the write operation. This operation is such that the X and Y drive currents attempt to write all of the 18 cores involved to binary 1's.

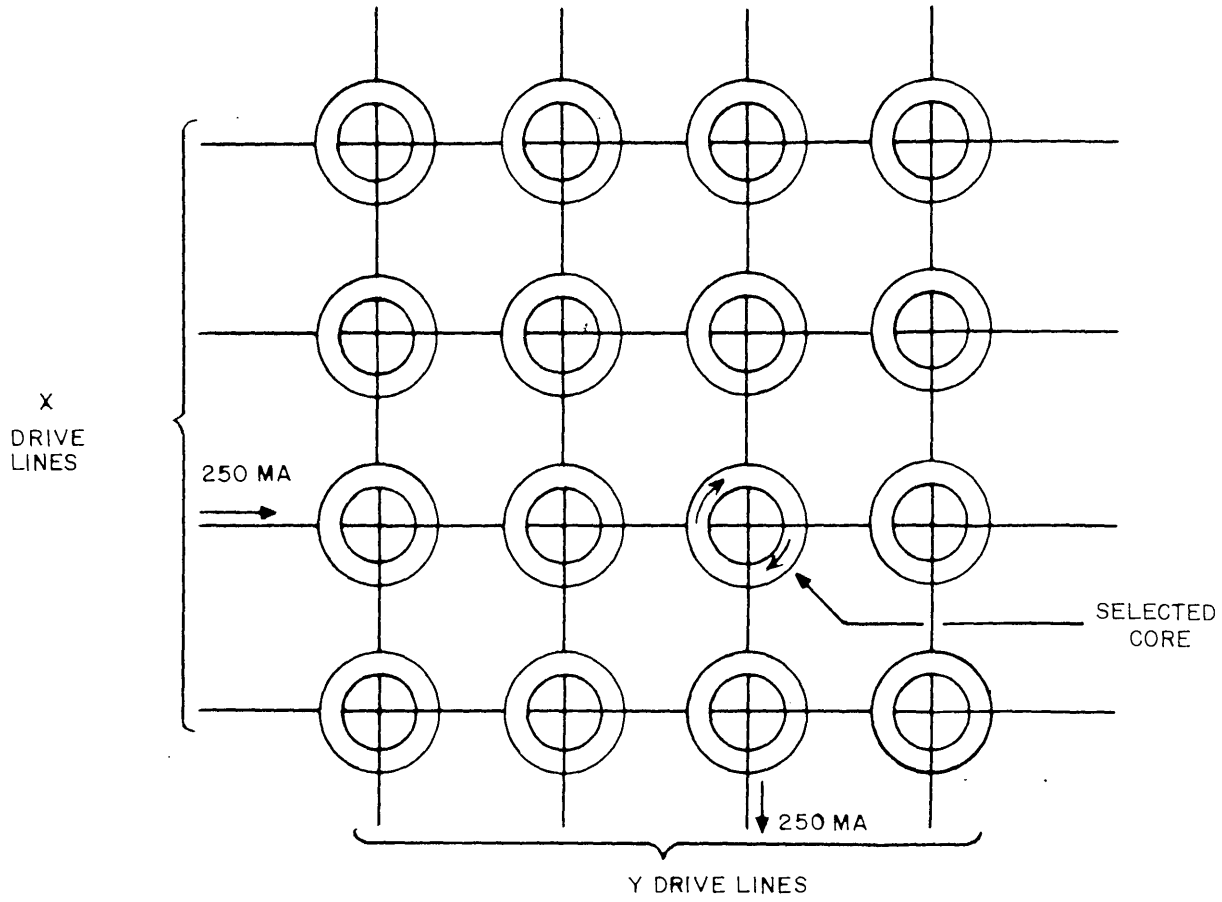


Figure 7.1-3. Core Matrix With X and Y Drive Lines

There is a third line, referred to as the inhibit line, which is activated with current of approximately 270 ma when it is desired to write a binary 0. When activated, its current negates from the X and Y currents to prevent the particular core from being switched. Refer to figure 7.1-4 for an illustration.

Prior to the write operation, all of the 18 cores are put in the binary 0 state. To write a binary 1, X and Y drive currents flow without inhibit current. The resultant current is enough to switch the particular core to the binary 1 state. A binary 0 is written by simply preventing the switching of the core to a 1_2 and leaving it in the 0_2 state. X and Y currents flow with inhibit current. The resultant current of approximately 250 ma is not enough to switch the core. Thus, it remains in its previous state of 0_2.

Since information written into memory comes from Z1, the inhibit lines for the particular 18 cores are controlled by the bit configuration of Z1. If $Z1_{XX}$ is a 1_2, no inhibit current flows for that bit position.

The inhibit line may be parallel to either of the drive lines. The effect is the same.

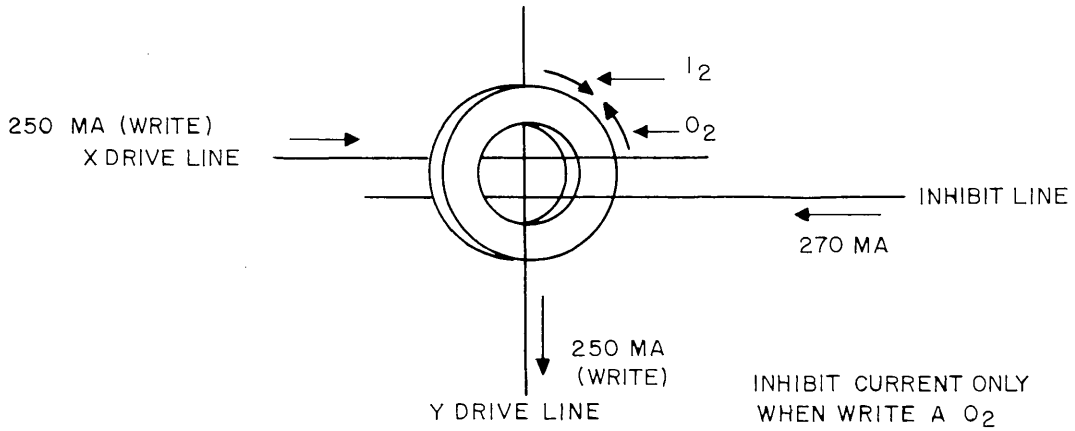


Figure 7.1-4. Core With X, Y, And Inhibit Lines

c. Read Operation. The operation which extracts information from memory is referred to as the read operation. This operation is such that the X and Y drive currents flow in the direction opposite to that for write and cause all 18 cores to be put in the 0_2 state. The information is destroyed and must be rewritten in the 18 cores to retain it.

The reading of information is accomplished by sensing the state of the 18 cores which existed prior to the X and Y current flow. A fourth line, referred to as the sense line, passes through the cores. There is one for each of the 18 bits. Refer to figure 7.1-5 for an illustration.

A binary 1 is indicated by a voltage induced in the sense line, regardless of polarity. If the core held a 0_2 prior to the read operation, the X and Y currents have negligible effect upon the magnetization of the core. There is little or no voltage induced in the sense line which is interpreted as a 0_2. If the core held a 1_2, the X and Y currents have great effect upon the core. The core is switched to 0_2. The corresponding change in magnetic flux causes an induced voltage in the sense line which is interpreted as a 1_2.

If the core had previously held a 0_2, there is noise voltage of small magnitude induced in the sense line. This voltage occurs sooner in response to the X and Y drive currents than does the voltage for a 1_2 stored in the core. To achieve the greatest differentiation between a 0_2 output and 1_2 output, a strobe pulse is used to enable the testing of the sense line for voltage. The strobe occurs when the difference between the noise voltage and the 1_2 voltage is maximum. Refer to figure 7.1-6 for the relationship of the strobe to the sense line voltage output.

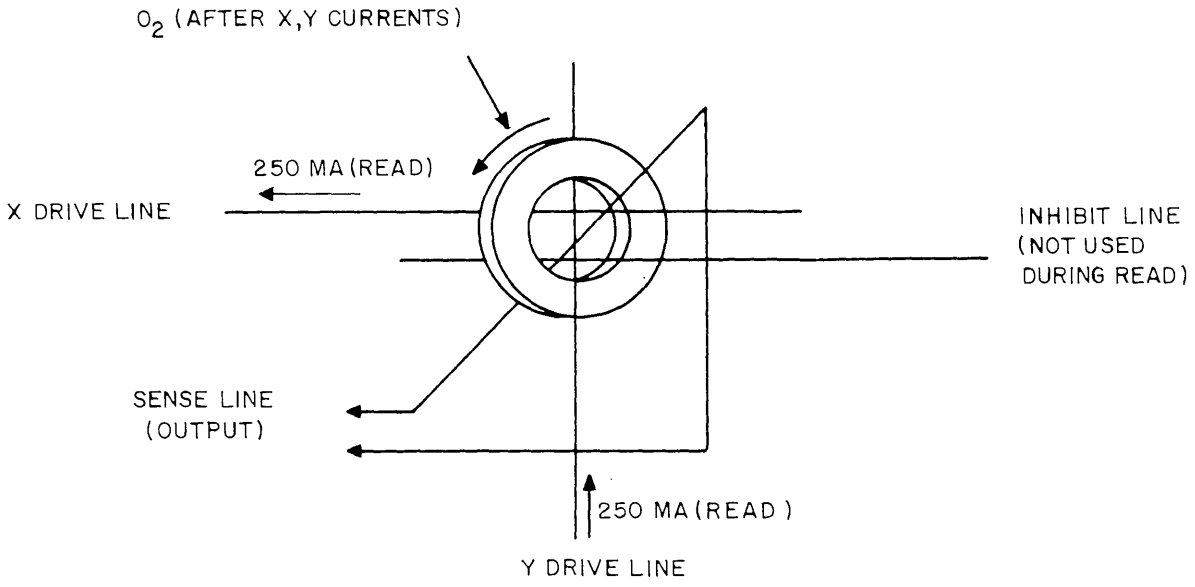


Figure 7.1-5. Core With X, Y, Inhibit, And Sense Lines

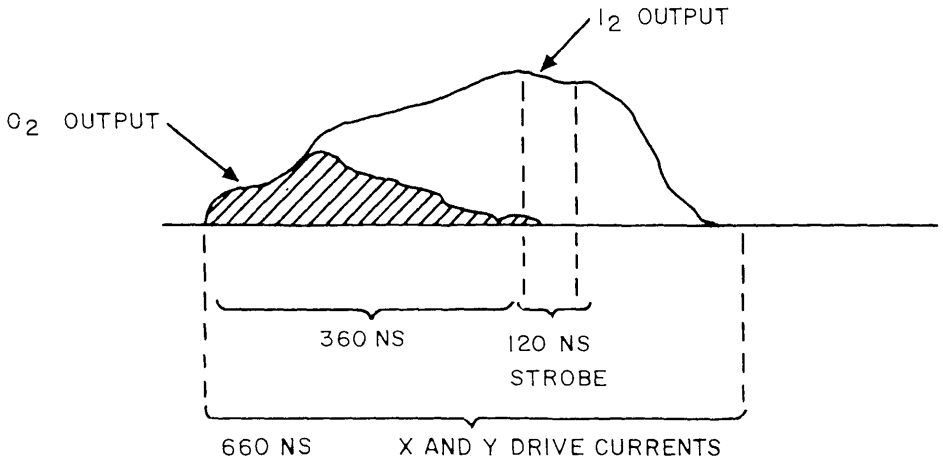


Figure 7.1-6. Magnetic Core Output On Sense Line

The sense line feeds an amplifier which responds to voltages of either polarity. During the strobe time, the output of the amplifier is used to set the information in the Z register. Actually, the data is strobed into a buffer register (ZM) before it is sent to Z1. Refer to figure 7.1-7 for an illustration.

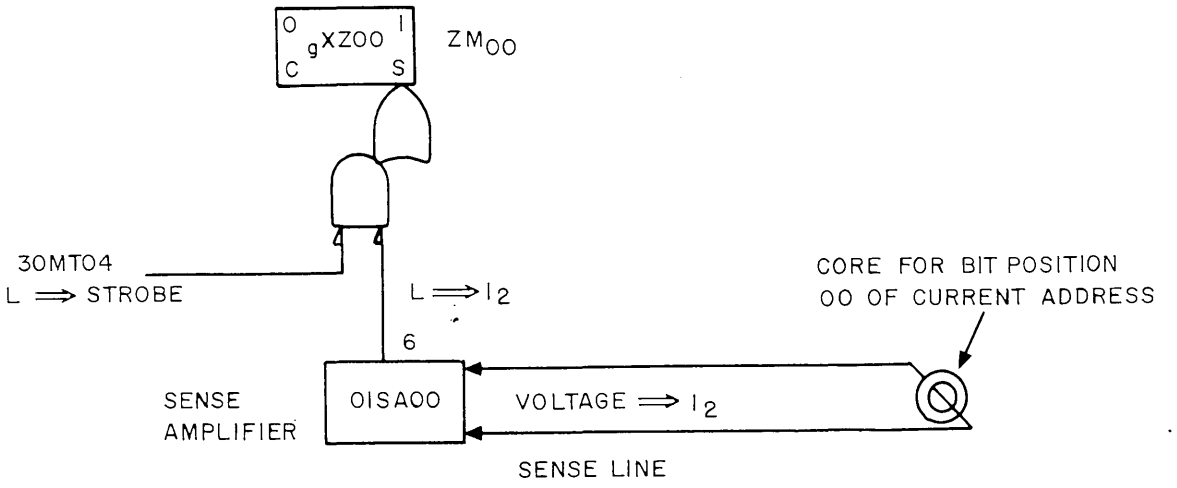


Figure 7.1-7. Main Memory Sense Line Output to ZM

d. Core Matrix. The cores are arranged in matrices. Each matrix contains cores for only one bit position of 4,096 locations. For example, a particular matrix contains bit position 00 for addresses 00000 through 07777_8. Refer to figure 7.1-8 for a typical smaller matrix.

In this example, one of 16 cores may be selected for a write or read operation. Only one sense and one inhibit line are necessary for the matrix because all cores in the matrix are for the same bit position.

When a particular core is selected by the intersection of X and Y currents in this example, three other cores receive 250 ma by a Y line and three more receive 250 ma by an X line. These cores do not switch to the opposite state because of the insufficient current; however, they do induce noise voltages in the sense line. Notice that the sense line is threaded through these cores in such a manner that the noise voltages oppose and tend to cancel one another. The sense line is threaded diagonally. Being perpendicular to the cores, maximum voltage is induced in the sense line from the switching core.

The inhibit line is threaded in such a manner that its current opposes any X or Y current with which it may intersect within a core. It is insured then that another core cannot be selected by the inhibit and either X or Y current aiding it to produce a resultant switching current.

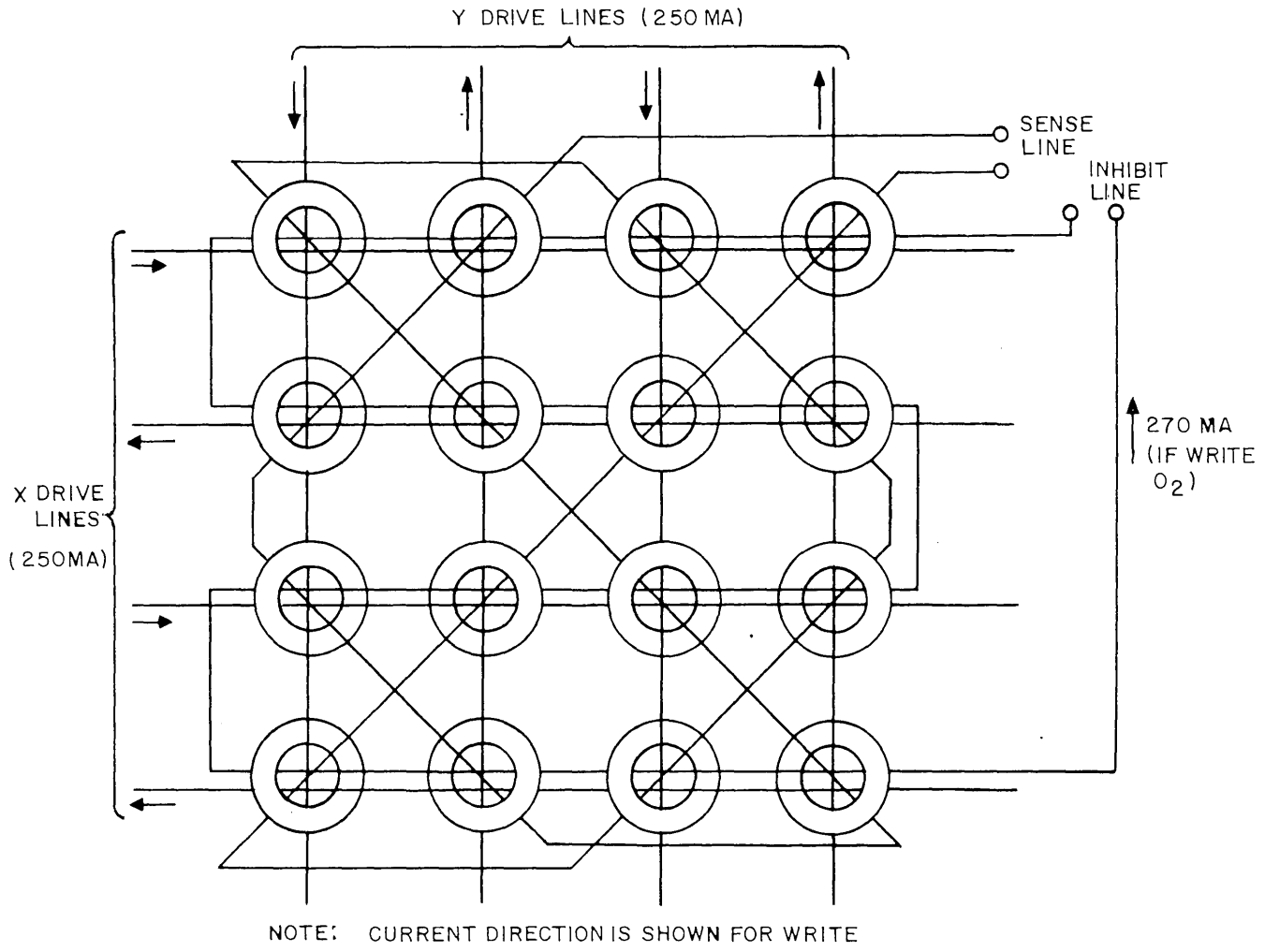


Figure 7.1-8. Typical Core Matrix

e. Physical Arrangement.

1. Memory Boards. Each matrix is referred to as a memory board. Each board contins 4,096 cores in a 64 X 64 array. Each board is driven by 64 X and 64 Y drive lines and has one inhibit and one sense line.

2. Stack. The memory boards are in stacks. The stacks are located on the four memory chassis. Each stack contains 18 bit positions for 4,096 memory locations. Refer to figure 7.1-9 and 7.1-10 for illustrations. The stack components described in figure 7.1-9 are discussed in a later sheet.

In each stack, the X and Y drive lines are threaded from one board to the next; such that one core on each board is selected when drive currents flow. The selected core on each board is at the intersections of the X and Y line. Refer to figure 7.1-11 for an illustration.

Sense lines from two stacks feed the same sense amplifier. The X and Y drive lines of just one stack are activated with current, such that only the selected stack will cause outputs from the sense amplifiers. Refer to figure 7.1-12 for an illustration.

The term bank is synonymous with the term stack. Refer to UNIVAC Technical Manual, Volume I, Section 1, figure 1-17 for a picture of one stack.

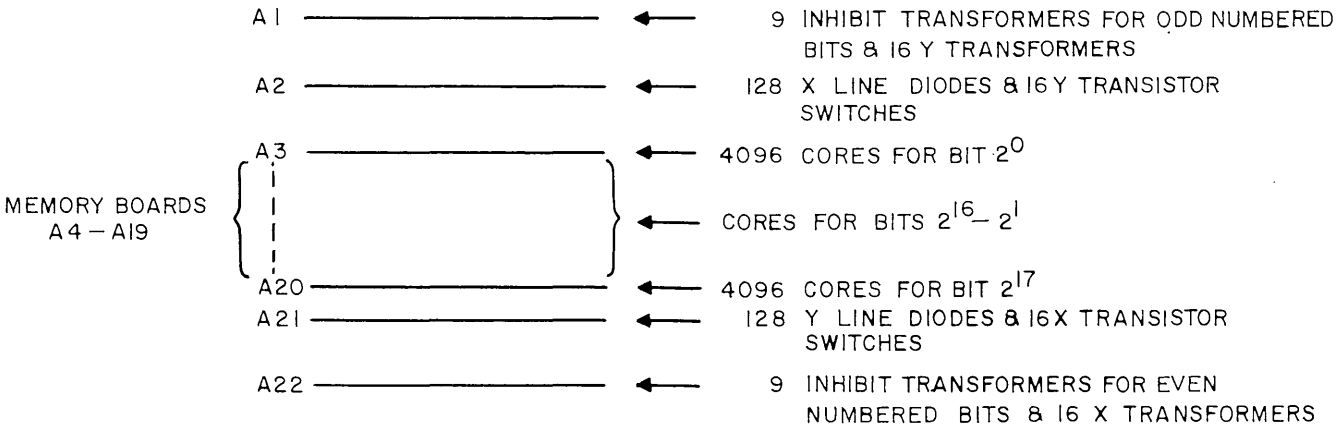
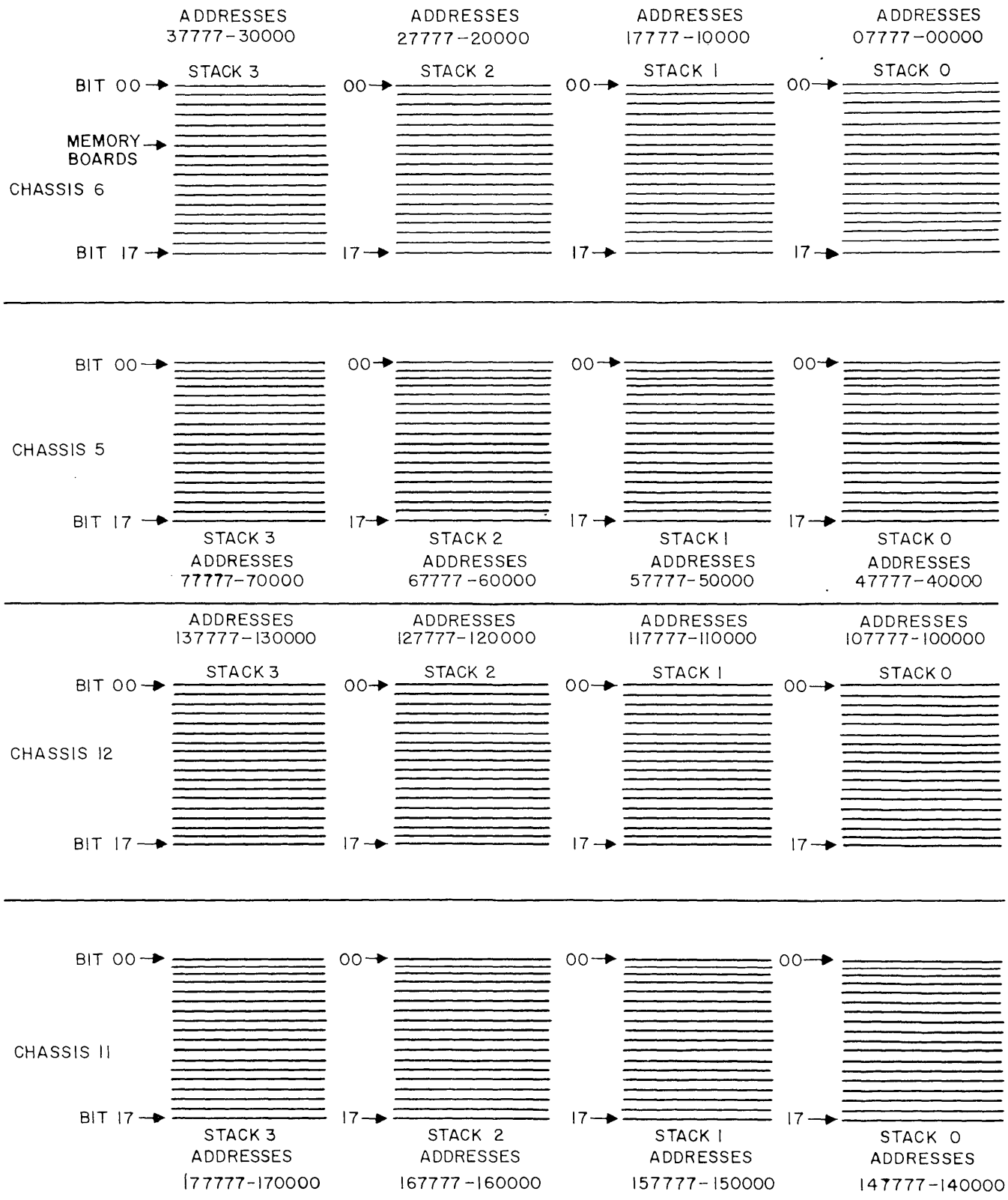


Figure 7.1-9. Physical Arrangement of One Stack (4096 Addresses)

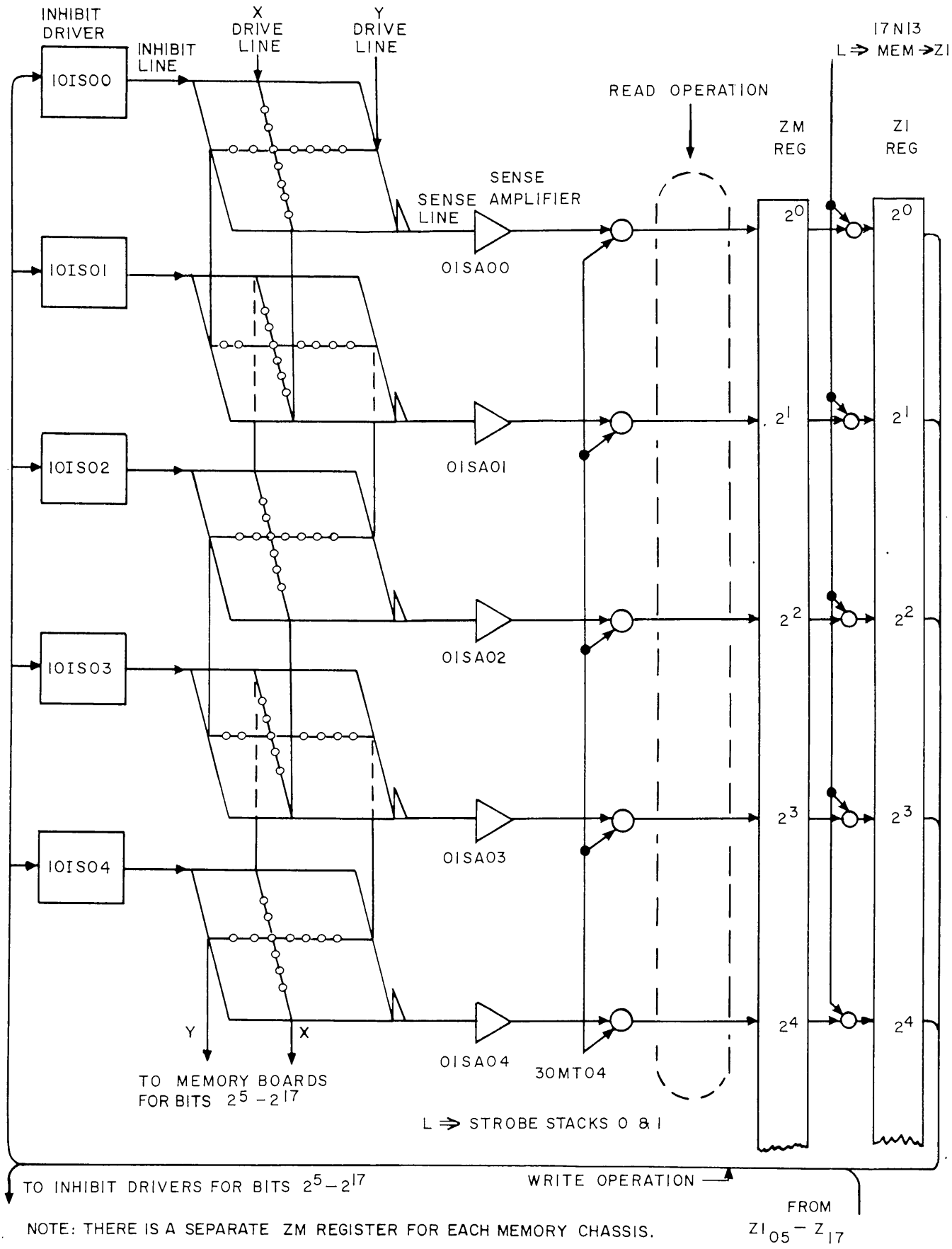
7.1-5. SUMMARY

Main memory has $65,536_{10}$ locations for storage of 18-bit words. The core storage element has destructive read-out which requires a read/write cycle. Cycle time is approximately 2 microseconds. The cores are distributed into stacks of 1,096 locations each. There are four memory chassis with four stacks per chassis. Each chassis, therefore, holds cores for all 18 bits of 16,384 locations plus the associated electronics.



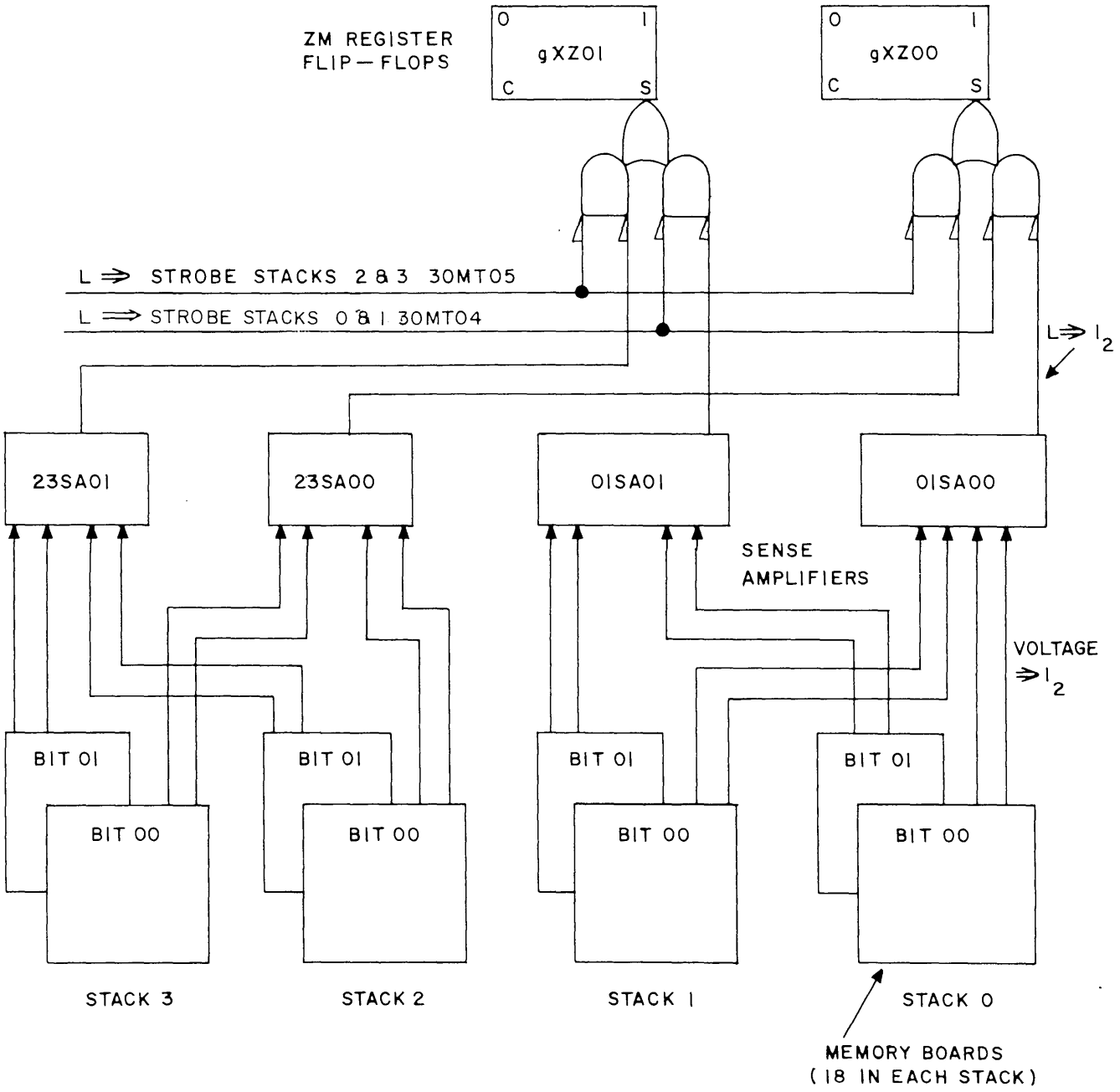
NOTE: THE TERM "STACK" AND "BANK" HAVE THE SAME MEANING.

Figure 7.1-10. Physical Arrangement Of Main Memory



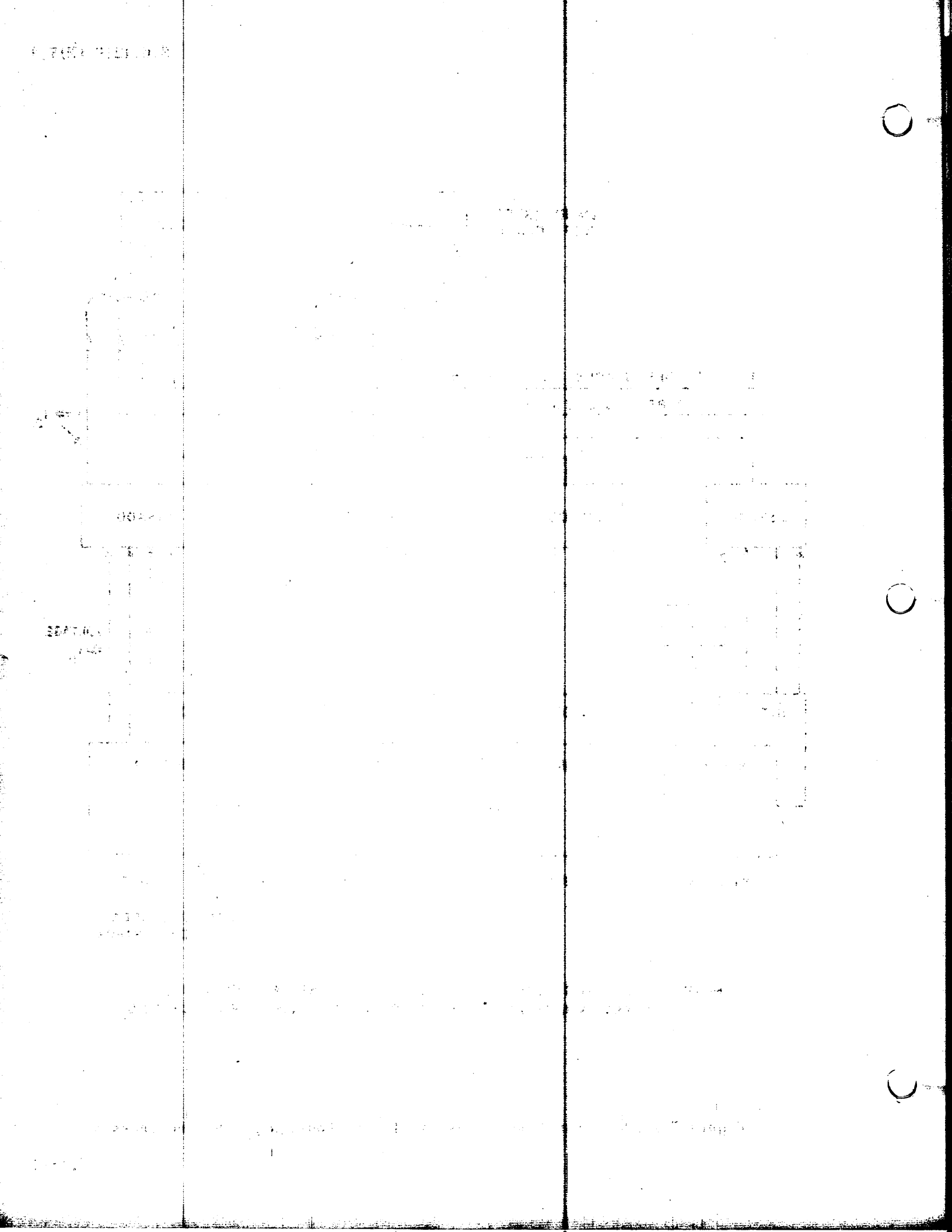
NOTE: THERE IS A SEPARATE ZM REGISTER FOR EACH MEMORY CHASSIS.

Figure 7.1-11. Block Diagram of Main Memory, Stack 0



NOTES: THE TERMS "STACK" AND "BANK" HAVE THE SAME MEANING.
THERE IS A SEPARATE ZM REGISTER FOR EACH MEMORY CHASSIS.

Figure 7.1-12. Main Memory Sense Amplifier Configuration, One Chassis



NAME:_____

7.1-6. STUDY QUESTIONS

a. How many cores are there in a stack? _____

b. How many memory addresses are involved in each stack?_____

c. Briefly describe the purpose of the inhibit line.

d. List some of the factors which assist in the differentiation of a 1_2 from a 0_2 read from a particular core.

SECTION 7 - MEMORY SECTION

7.2. MAIN MEMORY INTERNAL OPERATION

7.2-1. OBJECTIVES

To present the detailed theory of operation involved in the internal operation of main memory.

7.2-2. INTRODUCTION

Main memory is controlled by circuitry to select a particular set of 18 cores during a memory reference. Read and write operations are performed on these 18 cores.

7.2-3. REFERENCES

a. UNIVAC 1219 Technical Manual, Volume I, Paragraph 4-5b.

b. UNIVAC 1219 Technical Manual, Volume II, Section 9 (logic diagrams).

7.2-4. INFORMATION

a. General Description.

1. X and Y Drive Line Connections. The selection of a particular 18-bit location during a memory reference is accomplished with the use of X and Y drive lines carrying approximately 250 ma each. There are 64 of each per stack. Each stack on a chassis contains 18-bit positions for 4,096 locations. For a given address, one X line and one Y line is activated with current.

The address held in S1 selects one chassis, one stack on that chassis, and one pair of X and Y lines in that stack.

The 64 X and 64 Y lines in each stack are divided into groups. There are eight groups with each containing eight lines. Selection of a particular line is accomplished by the address specifying one of the eight groups and one of the eight lines within that group.

2. Translation of S1. The bit configuration of the address in S1 must specify the chassis, stack, X group of lines, X line, Y group of lines, and Y line. Refer to figure 7.2-1 for the interpretation of S.

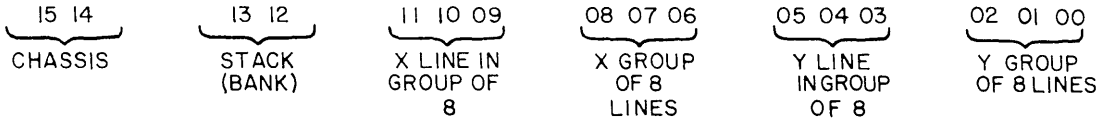


Figure 7.2-1. Translation of Address in S1

Refer to tables 7.2-1 and 7.2-2 for chassis and stack translation.

TABLE 7.2-1. CHASSIS TRANSLATION OF S1

$S1_{15}$	$S1_{14}$	CHASSIS
0	0	6 (addresses 37777-00000)
0	1	5 (addresses 77777-40000)
1	0	12 (addresses 137777-100000)
1	1	11 (addresses 177777-140000)

TABLE 7.2-2. STACK TRANSLATION OF S1

$S1_{13}$	$S1_{12}$	STACK
0	0	0
0	1	1
1	0	2
1	1	3

3. Drive Line Selection Technique. As an example, the X drive line selection for read operation is discussed for stack 0 of bank 0. Refer to figure 7.2-2 simplified diagram.

During the read operation the current diverter 10XR00 outputs a positive voltage level, the duration of which determines the width of the 240 ma X current pulse. As discussed later in this sheet, this time period is approximately 700 nanoseconds.

The output of 10XR00 is applied to eight transistor switches. One of these switches is closed when forward biased by the associated transformer secondary. A negative voltage is applied to the right-hand side of each primary by the driver-amplifier 10XS00 if S1 bits 13 and 12 specify stack 0. According to $S1_{08-06}$, one of the transformer primaries conducts due to a high level applied to its left-hand side.

One of the eight groups of eight X lines is selected by a positive voltage from the conducting transistor switch. One of the eight lines of the group is selected by a low level applied at the other according to $S1_{11-09}$. Current flows in the direction shown through the selected line. This line is threaded through all 18 memory boards in stack 0 and selects one core on each board at each intersection with the selected, current-carrying Y line in the stack.

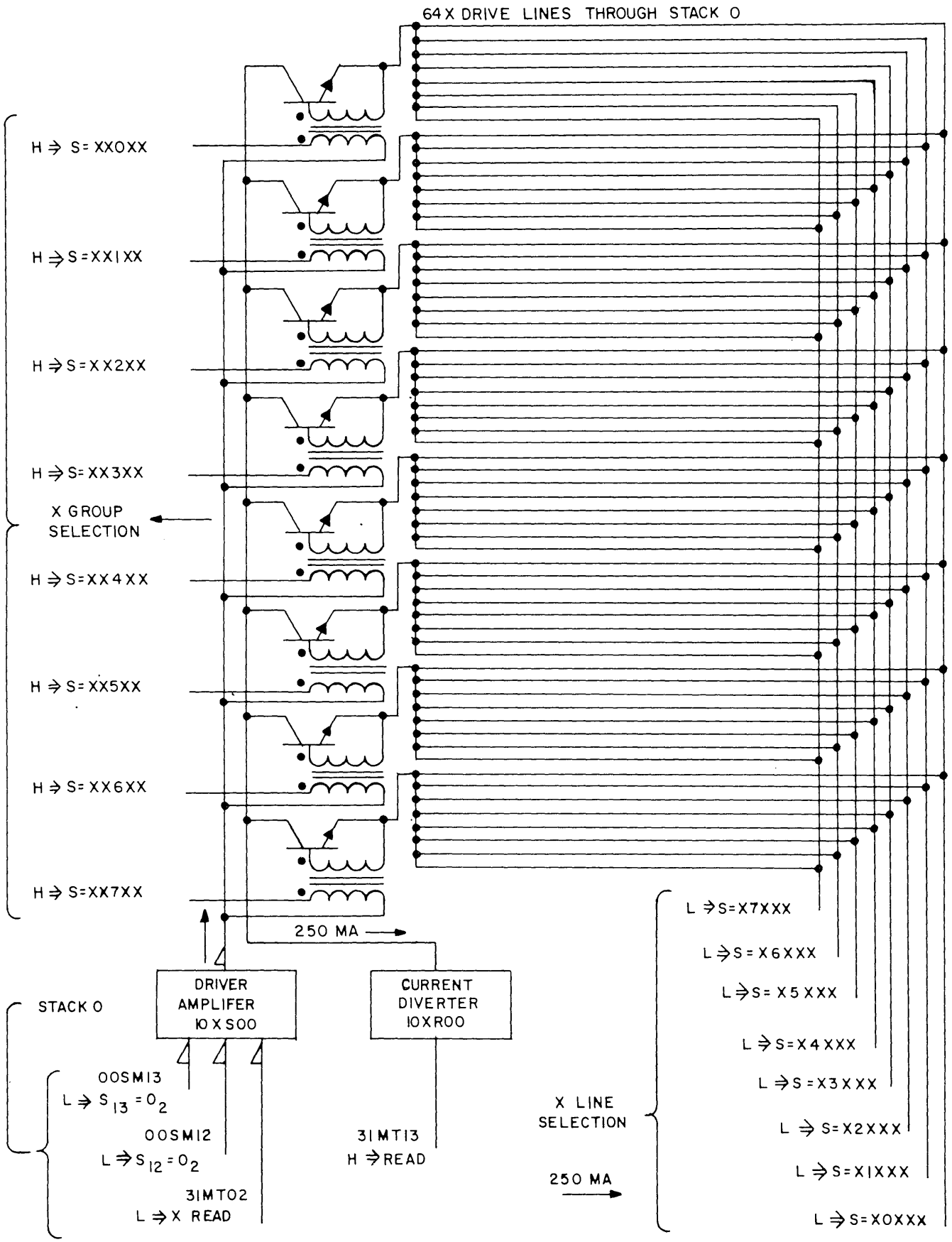


Figure 7.2-2. Simplified Diagram of Stack 0, X-Drive Line Connections for Read Operation

4. Example of Complete Operation for One Core.

a) Read Operation. So as to illustrate the interconnection of the various memory circuits, the operation involving one core is discussed. Refer to figure 7.2-3 for the following analysis.

The circuits shown below the core are concerned with the read operation. 10XR00 applies a positive voltage to the transistor switch. Assuming that X group 0 and stack 0 are selected, current flows from 10XS00 through the transistor switch primary to 10XG00. The transistor switch is forward biased by the transformer secondary voltage and applies the positive voltage from 10XR00 to the X drive line.

10XR00 also applies a negative voltage to pin 10 of 10XD00; and assuming the X line 0 is selected, this negative voltage is applied from pin 11 of 10XD00 to the other end of the X drive line. Current of 240 ma then flows through the X line in the direction shown with 10XR00 being the source and return of the current.

Y drive current is developed in the same manner to aid the X current in switching the state of the core to a 0_2.

If a 1_2 has been stored in the core, a voltage is induced in the sense line and is applied to 01SA00 causing a low level output. ZM_{00} is set during the strobe signal. If the Mem $\rightarrow$ Z1 enable is present, $Z1_{00}$ is also set.

The same X and Y lines shown are threaded through all 18 boards in stack 0 so as to read the 18 cores at their intersections.

There is a separate sense line for each memory board.

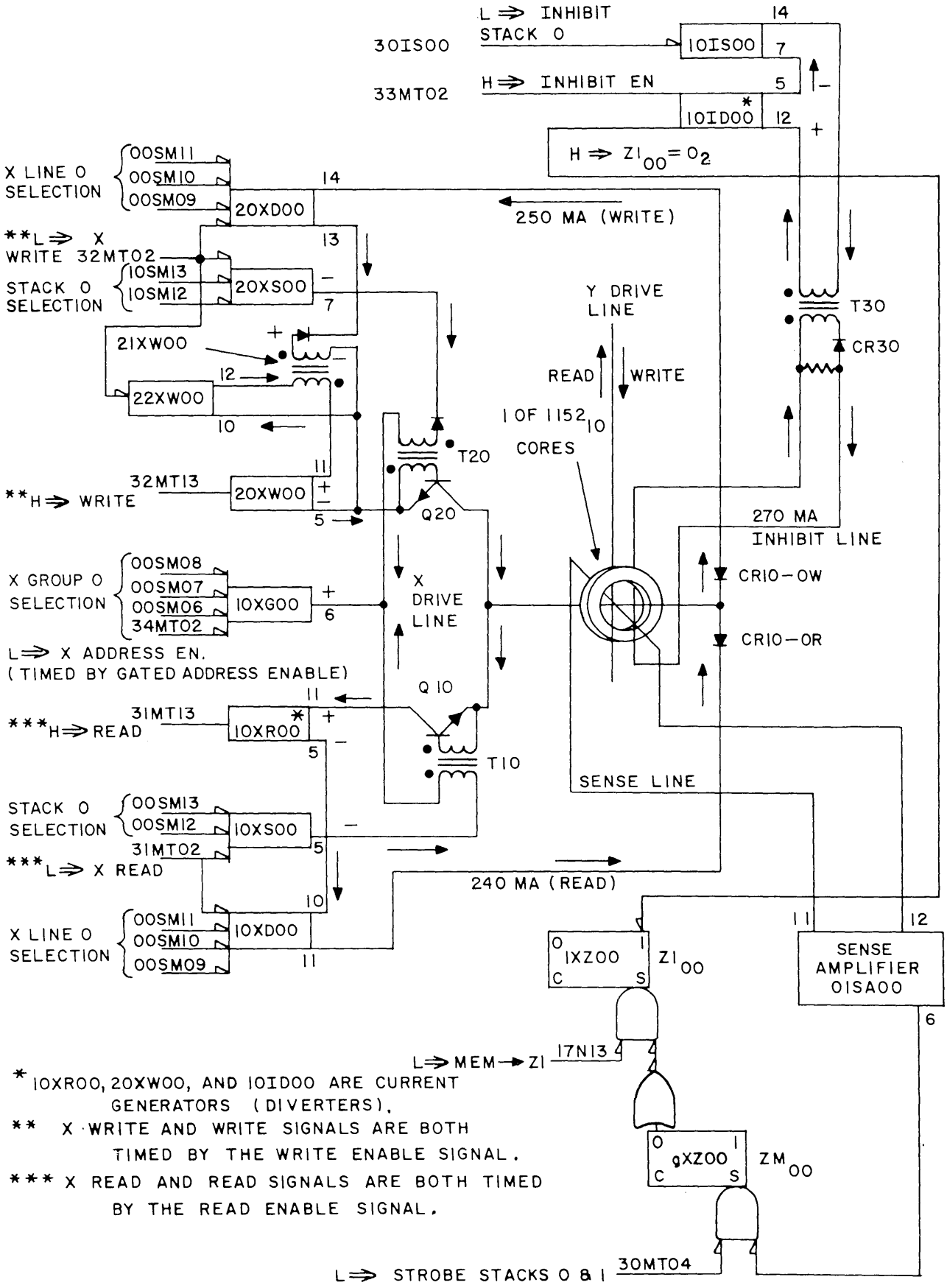
b) Write Operation. Refer to figure 7.2-3 for the following analysis.

X and Y current generation is similar to that for the read operation. The current circuits are connected so as to cause current flow through the same X and Y lines but in the opposite direction. 20XW00 applies a negative voltage to pin 10 of 22XW00. 22XW00 applies this voltage to one side of the transformer primary in 21XW00. The other side of the primary is connected to the positive voltage on pin 11 of 20XW00. The resulting primary current induces a voltage in the secondary. Assuming that X line 0 is selected, the positive voltage from the secondary is connected to one end of the X drive line through 20XD00.

Assuming that X group 0 and stack 0 are selected, current flows from 20XS00 through the write transistor switch primary to 10XG00. The transistor switch is forward biased by the transformer secondary voltage and applies the negative voltage to the other end of the X drive line. Current of 250 ma then flows through the X line in the direction shown.

Y drive current is developed in the same manner to aid the X current in attempting to switch the state of the core to a 1_2.

The X and Y currents will switch the core to a 1_2 only if there is no inhibit current. Inhibit current is dependent upon the content of Z1. The particular core shown is for bit position 00 and corresponds to $Z1_{00}$.



* 10XROO, 20XWOO, AND 10IDOO ARE CURRENT GENERATORS (DIVERTERS).

** X WRITE AND WRITE SIGNALS ARE BOTH TIMED BY THE WRITE ENABLE SIGNAL.

*** X READ AND READ SIGNALS ARE BOTH TIMED BY THE READ ENABLE SIGNAL.

Figure 7.2-3. Simplified Logic Diagram of X, Y, Inhibit, and Sense Line Connections

If $Z1_{00}$ is a 0_2, 10ID00 outputs positive and negative voltages. Assuming that the write operation is involved with stack 0, 10IS00 completes the current flow path from 10ID00 through the current transformer primary. Primary current flows in the direction shown with 10ID00 being the source and return of the current.

The resulting secondary current of approximately 270 ma flows through the inhibit line in the direction shown. This current is opposite to the X and Y currents so as to cause the resultant current through the core to be insufficient to switch the core to a 1_2. Thus, the core will remain in the 0_2 state if $Z1_{00} = 0_2$ and will be switched to a 1_2 if $Z1_{00} = 1_2$.

The same X and Y lines shown write into the 18 other cores in stack 0.

There is a separate inhibit line for each memory board.

b. Detailed Analysis.

1. Memory Timing. Memory has a timing source separate from other computer timing. Timing is developed from a series of delay lines which is initially activated from the computer main timing chain.

The delay line outputs time the memory operations so as to perform the read function followed by the write function. The inhibit current is timed such that it continues to flow after the X and Y write currents so as to insure that X and Y currents could not switch a core destined to remain in the 0_2 state.

Refer to logic diagrams, figure 9-122 for the memory timing circuitry. When flip-flop 0XG80 is set, the memory cycle is initiated. 0XG80 is set at T1.1 time and is cleared at T2.4 time which results in a set time of 875 ns.

The memory reference can be phased stepped. Notice that the set state of flip-flop 0XG80 produces the read operation signals, and the clear state produces the write operation signals. Since the setting and clearing of this flip-flop can be controlled by the operator in the phase-step mode, the time between the read and write portions of the memory cycle can also be determined by the operator. However, the read and write signals will have their normal durations. Because of this feature, a store instruction can be phase stepped completely.

Refer to figure 7.2-4 for a waveform diagram of the timing signals developed from the delay lines. The strobe signal timing is developed later in this sheet.

Refer to logic diagrams, figure 9-123 for the strobe logic circuitry. The strobe is generated from delay line 30MT02 and is timed so as to differentiate between a 1_2 sense line voltage and a noise voltage. There is a 20 ns time delay between consecutive pins on the type 3710 delay line card. The strobe signal should occur about 60 ns after the beginning of strobe-enable and last for approximately 120 ns.

The particular chassis selected by the address in S1 receives the timing signals. Refer to logic diagrams, figure 9-123 for the associated logic circuitry.

The logic circuitry shown in this figure is duplicated on the four memory chassis. Gates g1MT04, g4MT03, g3MT11, 30MT04, and 30MT05 receive the delay line timing signals. They are not used unless enabled by chassis selection.

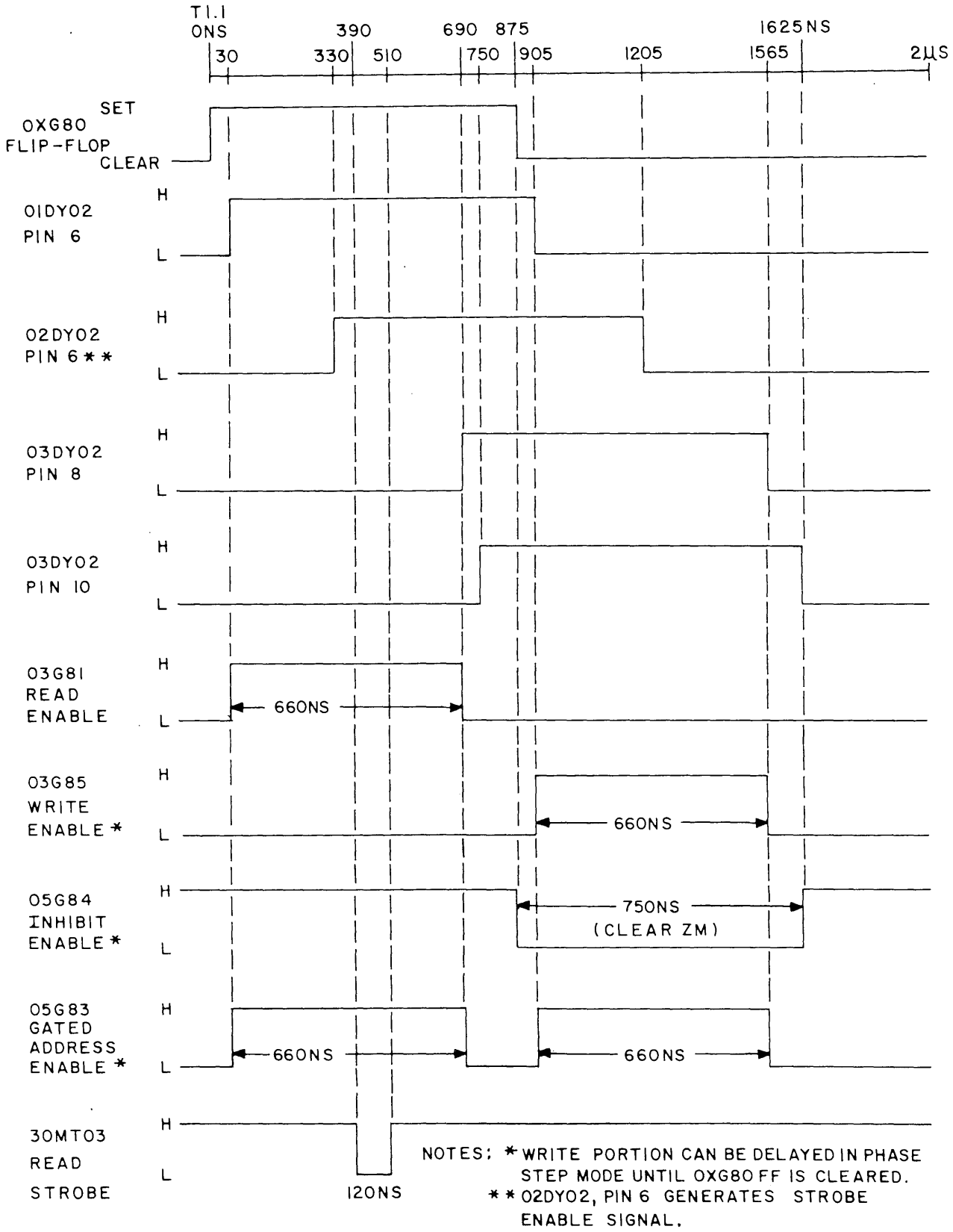


Figure 7.2-4. Theoretical Main Memory Timing

Also shown on this figure is the stack translation of S1 for the strobe signal and inhibit current. Bit positions $S1_{13,12}$ are sensed to determine the selected stack.

2. X Drive Current.

a) Read/Write Current Generators and Stack Selection. Refer to logic diagrams, figure 9-129 for the associated logic.

10XR00 and 20XW00 are the read and write X current generators, respectively. During the read operation, 10XR00 outputs a positive voltage on pins 11 and 12 and a negative voltage on pin 5. 10XM00 and 20XM00 are transformer current probes for the purpose of monitoring the X read and write currents through a transformer coupling network.

The driver-amplifiers, 10XS00 through 10XS03 and 20XS00 through 20XS03, select one of the four stacks. These circuits translate S1 bits 13 and 12 from S1 register slaves. The 10XS0- type is used for read and the 20XS0- for write.

b) X Group and Line Selection. There are eight groups of eight X lines each. One group and one line in that group are selected. Refer to logic diagrams, figure 9-128 for the associated logic circuitry.

The transformer drivers, 10XG00 through 10XG07, select one of the eight groups of X lines. These circuits translate S1 bits 08, 07, and 06 from S1 register slaves.

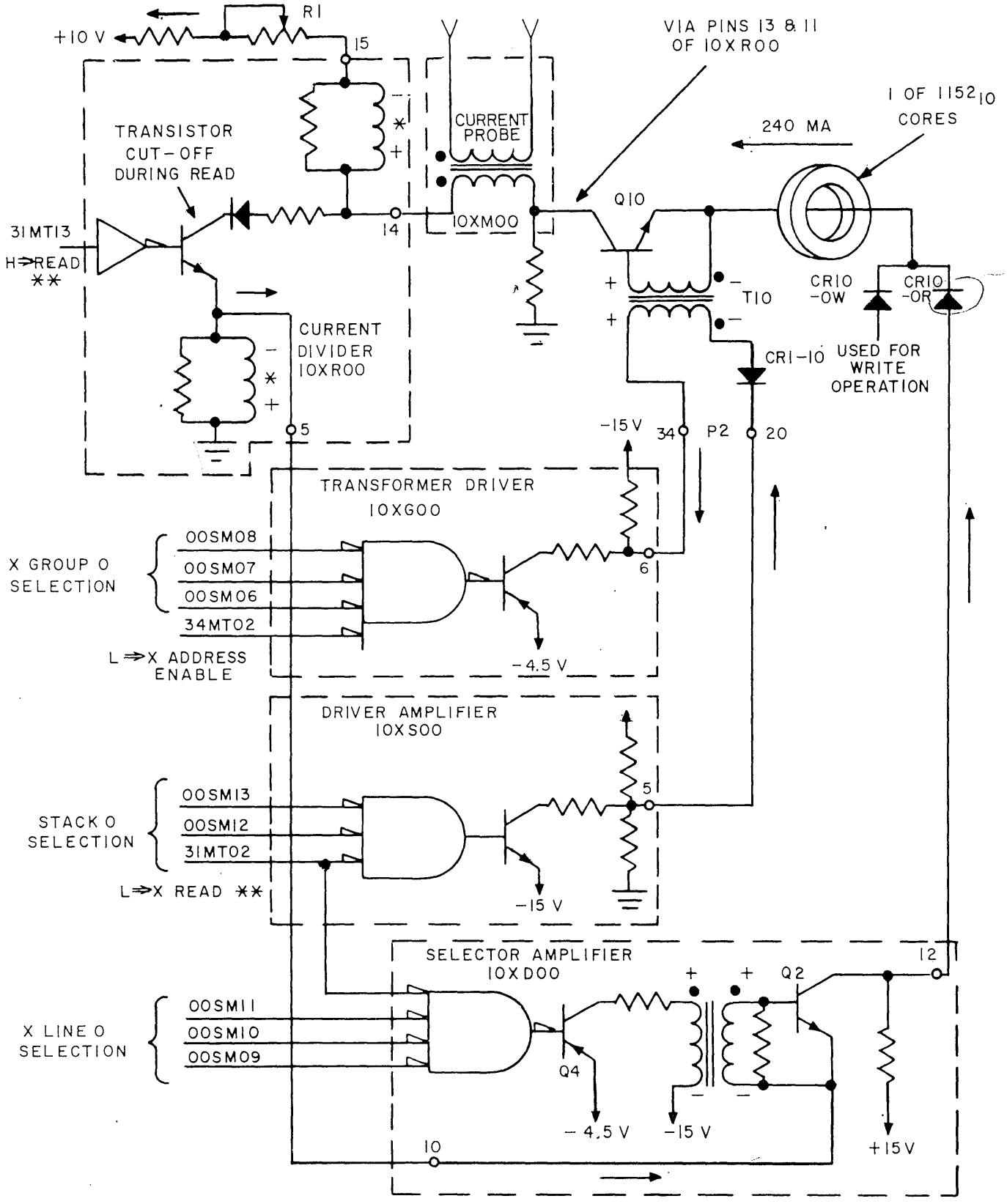
The selector-amplifiers, 10XD00 through 10XD07 and 20XD00 through 20XD07, select one of the eight X lines of the enabled group. These circuits translate S1 bits 11, 10, and 09 from S1 register slaves. The 10XD0- type is used for read and the 20XD0- for write.

c) Combined Circuits Interconnection. So as to illustrate the complete X drive current operation, the read current flow is analyzed. Refer to figure 7.2-5 for a simplified logic/schematic diagram illustrating the interconnection of the X line selection circuits as analyzed below.

Only the output stages of these circuits are shown for simplicity. Assuming stack 0 to be selected, the NAND gate located in 10XS00 applies a high level to its transistor so as to forward bias it. Assuming X line group 0 to be selected, the AND function in 10XG00 applies a low level to its transistor to forward bias it. Current flows from the -15v supply of 10XS00 through the transistor switch primary (P2-20) to the -4.5v supply of 10XG00.

The resulting secondary voltage forward biases the transistor switch to allow it to conduct X drive current. The source of current is 10XR00. Prior to the read operation, its transistor is conducting which causes small voltages to be developed across the R/L networks in the collector and emitter leads of polarity opposite to those shown. During the read operation, the transistor is cut off resulting in the development of voltages across these R/L networks of the polarity shown. A positive voltage then is applied to one side of the X drive line via the transistor switch and a negative voltage is applied to pin 10 of 10XD00.

Assuming X line 0 to be selected, the AND function in 10CD00 applies a low level to transistor Q4 to forward bias it. Current flows through its transformer primary resulting in a secondary voltage which forward biases transistor Q2. X drive line



NOTES * THE VOLTAGE POLARITIES SHOWN FOR THE R/L NETWORKS OF 10XR00 EXIST WITH ITS OUTPUT TRANSISTOR CUT OFF TO PROVIDE X LINE CURRENT.

** X READ AND READ SIGNALS ARE TIMED BY THE READ ENABLE SIGNAL.

Figure 7.2-5. Simplified Logic/Schematic Diagram of X Drive Line Connection for Read Operation

current flows from the negative voltage supplied by the emitter R/L network of 10XR00 through Q2 of 10XD00, the X line, and the transistor switch to the positive voltage supplied by the collector R/L network and +10v supply of 10XR00.

The X drive line current is approximately 240 ma and can be adjusted by R1 which is in series with the +10v supply to 10XR00.

The generation and flow of write current is similar. It involves current flow of approximately 250 ma through the same X drive line in the opposite direction.

3. Y Drive Current. The circuits which generate Y current and select a particular Y line are similar to those of the X drive current operation. Refer to logic diagrams, figure 9-126 and 9-127 for the logic circuitry concerned with the generation of read/write current, stack selection, Y line group selection, and Y line selection.

The drive line current is approximately 240 ma for read and 250 ma for write. Current can be adjusted by the potentiometers connected to 10YR00 and 20YW00 for read and write current, respectively. Refer to logic diagrams, figure 9-127 for 10YR00 and 20YW00.

4. Inhibit Current. Inhibit current is used only during the write operation. If no inhibit current flows, the X and Y write currents aid each other so as to switch the particular core to a 1_2. If a 0_2 is to be written, inhibit current flows opposite to the X and Y currents so as to prevent the switching action and retain a 0_2 in the core.

There is a separate inhibit line for each memory board of each stack. Inhibit current for each line is dependent upon the corresponding bit in the Z1 register from where the 18-bit word is to be written into memory.

Refer to figure 7.2-3 for a review of the circuits involved with the inhibit current. The example shown is for bit position 00. The current source is 10ID00 which operates in the same manner as the X and Y drive current generators. If $Z1_{00} = 0_2$, which means that inhibit current is desired, 10ID00 supplies positive and negative voltages. 10IS00 acts as a switch to pass current if stack 0 is selected. Current flow through the inhibit transformer causes secondary current flow of approximately 270 ma through the inhibit line which is the inhibit current.

Refer to logic diagrams, figures 9-130 through 9-131 for the logic circuitry associated with inhibit current.

5. Sense Line Output. The information is extracted from memory during the read operation by sense lines. There is a separate sense line for each memory board. Cores which are switched from 1_2's to 0_2's by the X and Y read currents induce voltages in the sense lines passing through them. Other cores which have a current-carrying X or Y line through them induce noise voltages in the sense lines. The strobe signal is used to differentiate between these voltages.

Refer to figure 7.2-3 for a review of the circuits involved with the sense line. The example shown is for bit position 00. 01SA00 outputs a low level when a voltage of either polarity is applied to it from the sense line. ZM_{00} is set during the strobe if the core contained a 1_2 prior to the X and Y read currents. $Z1_{00}$ is set if ZM_{00} is set.

Refer to logic diagrams, figures 9-133 through 9-135 for the logic circuitry associated with the sense line outputs for bit positions 17 through 00.

7.2-5. SUMMARY

The main memory cycle time is approximately 2 microseconds in duration. The first portion of the cycle performs the read operation and last portion performs the write operation. The address translation logic enables one X line and one Y line by performing chassis, stack, X line and group, and Y line and group selections. Transistor switches are used to route the current to the proper line.

NAME: _____

7.2-6. STUDY QUESTIONS

a. How many current generators (diverters, card 3690) are there on a memory chassis? _____

b. Given:

Address	Instruction
17776	101000
17777	121000
20000	717777

Assume each of the following malfunctions to occur individually. The given instructions are executed as a part of a program, and no malfunctions are noticed in their executions. Which of these conditions would cause the first two instructions to be destroyed from memory after they are read-out to be executed and yet not affect the last instruction as it appears in memory after it is read-out? Each of the following is on chassis 6. Indicate your answers by writing "yes" or "no" beside each malfunction condition.

1. 10YM00, open pin 7 (logic diagrams, figure 9-127) _____

2. 21XW00, open pin 8 (logic diagrams, figure 9-129) _____

3. 20XS02, open pin 7 (logic diagrams, figure 9-129) _____

4. 10XS01, open pin 5 (logic diagrams, figure 9-129) _____

5. 10XG07, open pin 9 (logic diagrams, figure 9-128) _____

6. 20XD00, open pin 13 (logic diagrams, figure 9-128) _____

7. 30MT03, grounded output (logic diagrams, figure 9-123) _____

8. Transistor Q10, open collector to emitter (logic diagrams, figure 9-136B) _____

9. Transistor Q20, open collector to emitter (logic diagrams, figure 9-136B) _____

c. Given: instruction = 440001
SR = 01111_2
AL = 000000

Assume each of the following malfunctions to occur individually. The given instruction is executed. Which of these conditions would cause the final content of address 70001 to be 000001_8? Indicate your answers by writing "yes" or "no" beside each malfunction condition.

1. 2XZ00 ff, grounded pin 8 (logic diagrams, figure 9-133) _____

2. 23SA00, pin 6 constant low level output, chassis 5 (logic diagrams, figure 9-133) _____

3. 3XZ00 ff, grounded pin 8 (logic diagrams, figure 9-133) _____

4. Open inhibit line, stack 3, chassis 5 _____

5. 1XZ00 ff, grounded pin 13 (logic diagrams, figure 9-111) _____

6. 3XZ00 ff, pin 8 constant low level output (logic diagrams, figure 9-133) _____

7. 03G85, constant low level output (logic diagrams, figure 9-122) _____

8. 05G85, grounded output (logic diagrams, figure 9-122) _____

SECTION 7 - MEMORY SECTION

7.3. GENERAL DESCRIPTION OF CONTROL MEMORY

7.3-1. OBJECTIVES

To present the general description of control memory.

7.3-2. INTRODUCTION

The basic control memory has 128 locations for storage of 18-bit words. Additional memory can be installed to provide 256 locations. The storage element is ferrite cores. Cycle time is 500 nanoseconds. Most of the control memory locations are assigned as special purpose such as real time clock, index registers, and input/output address control words. If the control memory locations are referenced directly by the program, their use will not result in time saving.

7.3-3. REFERENCES

UNIVAC 1219 Technical Manual, Volume I, Paragraph 4-5c

7.3-4. INFORMATION

a. Core Description. As storage elements, control memory uses magnetic cores. These cores are made of ferrite material and can be magnetized. The direction of magnetization represents the information stored. There are two cores for each bit position of each word location. One core is magnetized in a particular direction to store a 1_2. The other core is magnetized in the same direction to store a 0_2. Refer to figure 7.3-1 for an illustration of one core.

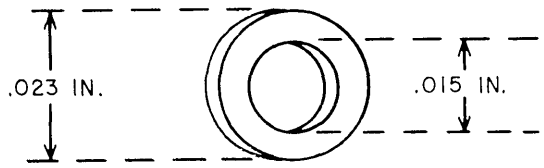


Figure 7.3-1. One Magnetic Core

The core is magnetized by passing current through a wire which is threaded through the core. This wire is referred to as the word line. The direction of current flow determines the direction of magnetization. Refer to figure 7.3-2 for an illustration.

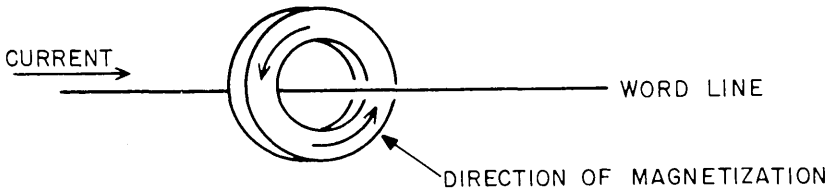


Figure 7.3-2. Core with Word Line

The operation to extract a word from memory (read) is destructive. That is, the word information is no longer retained. Thus, a write operation necessarily follows the read operation to restore the 18-bit word. The word line current to effect the read operation is opposite to that for writing.

b. Core Pair Operation. Refer to figure 7.3-3 for the following discussion.

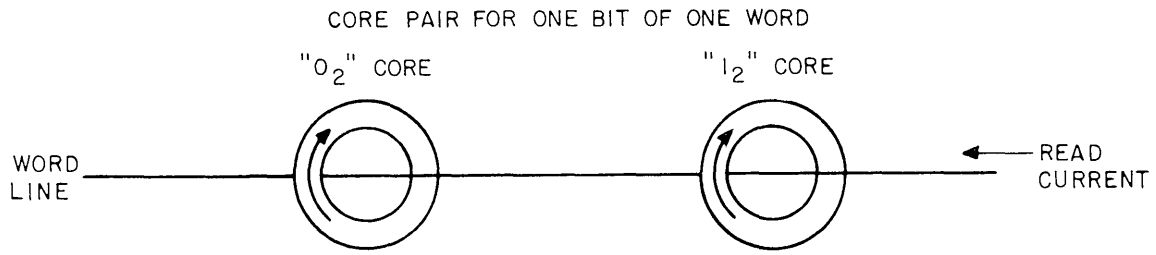
All of the drawings of figure 7.3-3 involve one core pair for one particular bit position. The first drawing illustrates the effect of the read operation upon the cores. Notice that both cores are magnetized in the same direction by the word line read current. This condition will always exist prior to the write operation, since writing is performed after the read operation. The read operation is shown at this time only to show the cores being set to a common state. Information is extracted from the cores by this operation, but this process is analyzed later in this sheet.

The second drawing shows the effect of word line current on the same core pair. Notice that the word line current direction is opposite that for reading. A second current-carrying line is introduced in this drawing. The digit line is only used (carries current) during the write operation. In this case, a 0_2 is being written into the core pair. The digit line current direction determines the binary value written.

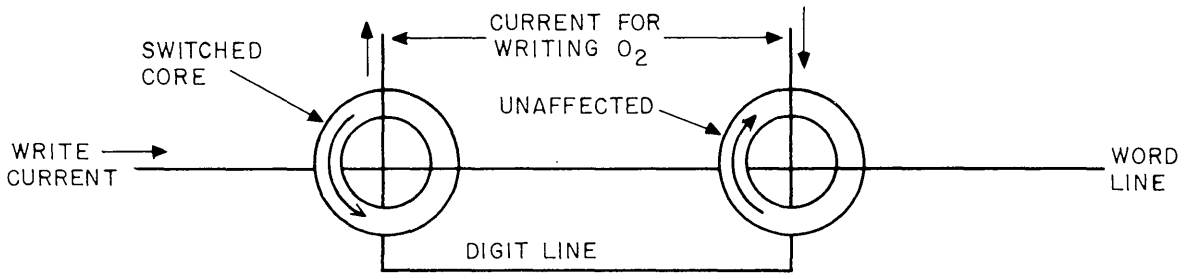
The effect of the digit line current with word line current is to cause a switch in the magnetization of the "0_2" core and not to affect the "1_2" core. It is not necessary for the digit line current to aid the word line current in the "0_2" core to switch, because the word line current amplitude alone is sufficient to cause the switching. Rather the function of the digit line current in this case is to negate the effect of word line current in the "1_2" core to prevent it from switching. This core retains its magnetization direction instated by the previous read operation.

The third drawing shows the effect of writing a 1_2 on the core pair. Notice that digit line current for writing a 1_2 is opposite to that for writing a 0_2. In this case, word line current is able to switch the "1_2" core. The digit line current subtracts from word line current to prevent the switching of the "0_2" core. This core retains its magnetization direction instated by the previous read operation.

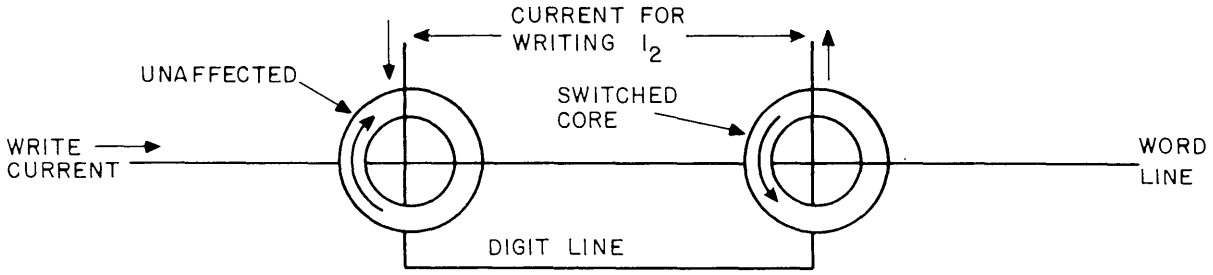
The last drawing again shows the read operation. The digit line is not used. The word line current direction is opposite to that for writing and causes both cores to be magnetized in the common direction as shown in the first drawing. One of the cores will already be magnetized in this direction. The other core will be switched to this direction. During the switching, the corresponding change in the magnetic lines of force induces a voltage in the third line shown, the sense line. This line



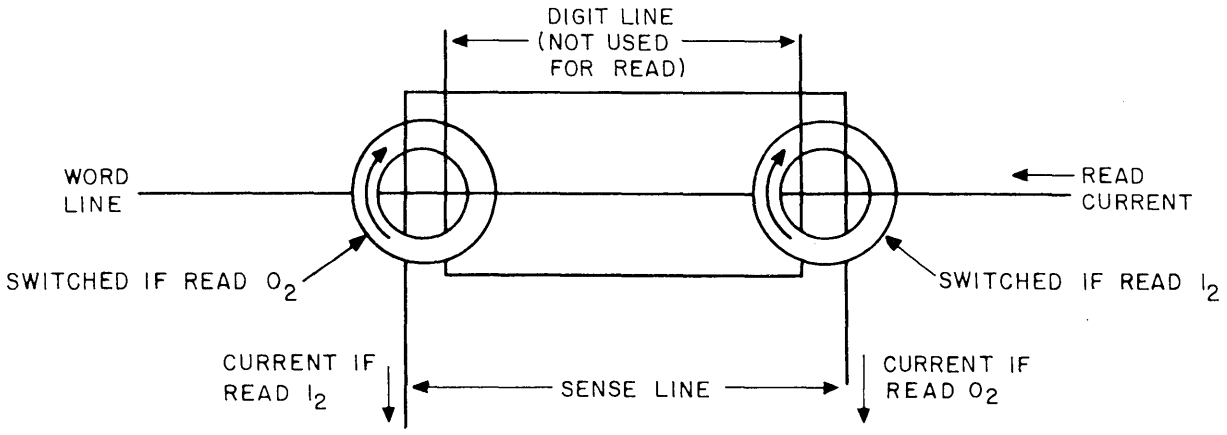
a. FIRST READ OPERATION



b. WRITE OPERATION FOR O_2



c. WRITE OPERATION FOR I_2



d. READ OPERATION

Figure 7.3-3. Control Memory Core Pair Operation

is only used during the read operation. The polarity of the sense line voltage, and thus the direction of current flow through the sense line, depends upon which core is switched. Therefore, one direction of sense line current indicates a 0_2 was stored in the core pair and the opposite direction indicates a 1_2 was stored. The sense line feeds an amplifier which is sensitive to the voltage polarity applied to it and which can discriminate between a 0_2 read-out and a 1_2.

Notice that after the read operation, both cores are magnetized in the same direction. A write operation always follows to restore the information read-out or to store new information.

c. Physical Arrangement. Each word location has its own word line which passes through all of its 18 core pairs. When a word line is activated with current, the associated 18-bit word location is selected and no other cores are affected. Refer to figure 7.3-4 for an illustration showing the memory arrangement.

There is a separate word line for each of the 128 locations. Each of these lines actually is threaded twice through its core pairs. Thus, a greater effect upon the cores is achieved from the word line current. Notice that each of the sense and digit lines passes through all core pairs of a particular bit position.

The word locations are separated into two sections of 64 locations each. Between these sections, the sense lines are crossed to minimize noise voltages induced in the sense line. The left-most core of any core pair in the lower section (addresses 00000 - 00077 or 00400 - 00477) is considered to be the "0_2" core. Because of the sense line reversal, the left-most core of any upper section core pair is considered to be the "1_2" core.

Since the position of the "1_2" and "0_2" cores is reversed in the two sections, the direction of digit line current is not only dependent on the binary value to be written but also the address. That is, the writting of 1_2 in the upper section requires digit line current flow in the direction opposite to that for writing 1_2 in the lower section.

For the 256-word memory, there are two separate configurations like that shown in figure 7.3-4.

7.3-5. SUMMARY

Control memory can have 128 or 256 18-bit word locations. The memory cycle time is approximately 500 nanoseconds. During this cycle, a read operation is performed followed by a write operation. The storage device for each bit is a core pair. Depending on the binary value stored, one core of the pair or the other is used to hold the bit.

The read operation uses word line current to switch the core magnetization. Only one core of each pair of the word is affected by the current, depending on the bit value. The core that switches causes sense line current, the direction of which indicates the bit value.

The write operation uses word line current of opposite direction to that used for reading. Digit line current is also used to determine which core of each pair will be affected by the word line current. The direction of digit line current is dependent upon the binary bit value as well as the address involved.

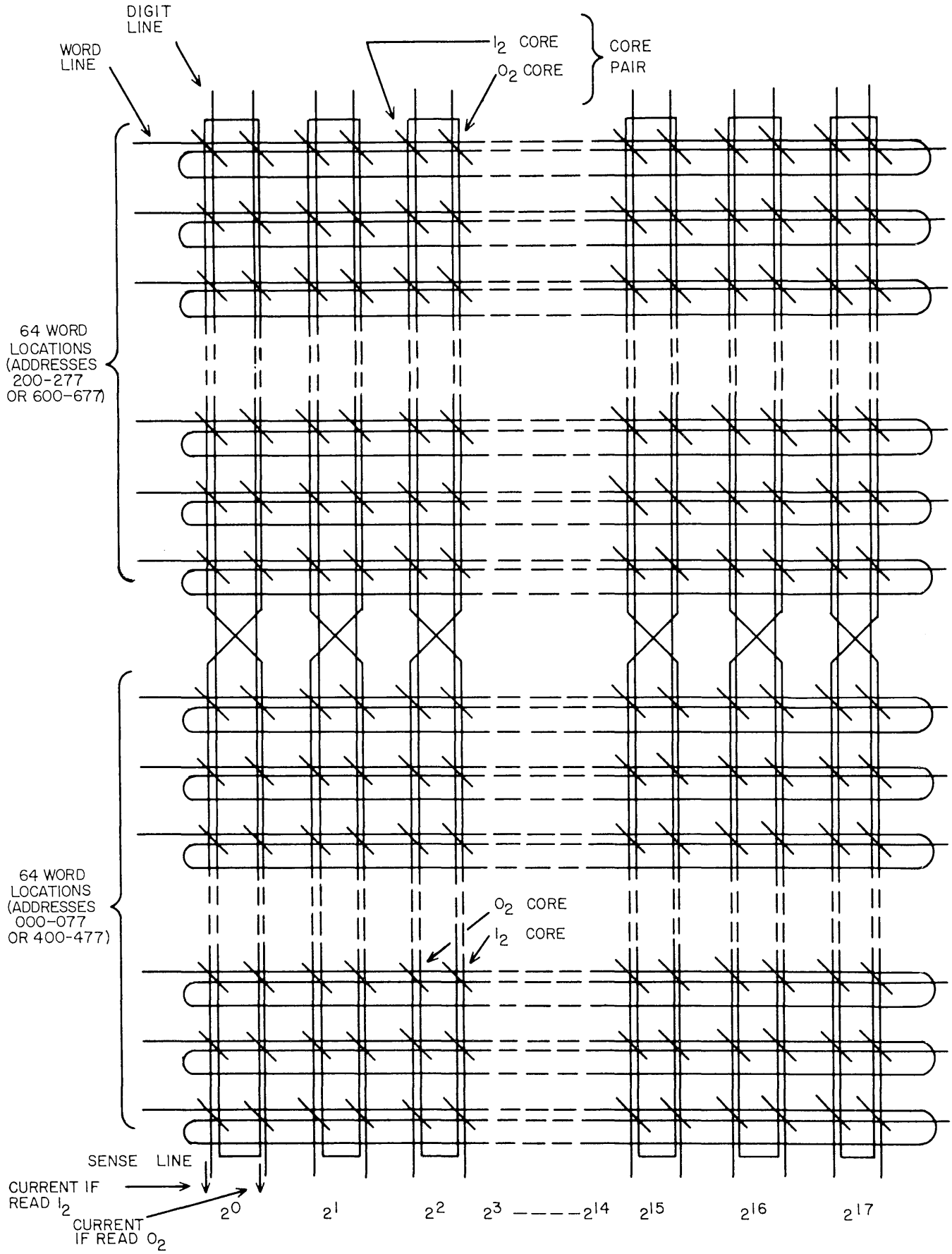


Figure 7.3-4. Control Memory Arrangement for 128_{10} Word Locations

SECTION 7 - MEMORY SECTION

7.4. CONTROL MEMORY INTERNAL OPERATION

7.4-1. OBJECTIVES

To present the detailed theory of operation involved in the internal operation of control memory.

7.4-2. INTRODUCTION

Control memory has circuitry to select one of 128 or 256 word drive lines. Read and write current flows through the selected line in opposite directions. There is one digit line for each bit position common to every address. It is activated during the write operation only. Current direction is dependent upon the binary value to be stored as well as the address.

7.4-3. REFERENCES

a. UNIVAC 1219 Technical Manual, Volume I, Paragraph 4-5c.

b. UNIVAC 1219 Technical Manual, Volume II, Section 9 (logic diagrams).

7.4-4. INFORMATION

a. General Description. Of the 128 or 256 word drive lines, one is selected during each control memory reference. This line carries current in one direction for approximately 80 nanoseconds during the read operation and in the opposite direction for approximately 60 nanoseconds during the write operation. Each of the 18 core pairs, through which the word line passes, is affected by the current.

For the 128-word memory, the word lines are considered to be in 16 groups of eight lines each. For the 256-word memory, the word lines are considered to be in 16 groups of 16 lines. Word line selection is made by enabling one group and one line of that group. The control memory address is placed in SO. The bit configuration of SO is translated into group and line. Line selection is also referred to as diode section.

Group selection is actually subdivided into what is termed group and board selection and group pair selection. Line (diode) selection is actually subdivided into what is termed diode end board selection and diode pair selection. Refer to figure 7.4-1 for the translation of SO.

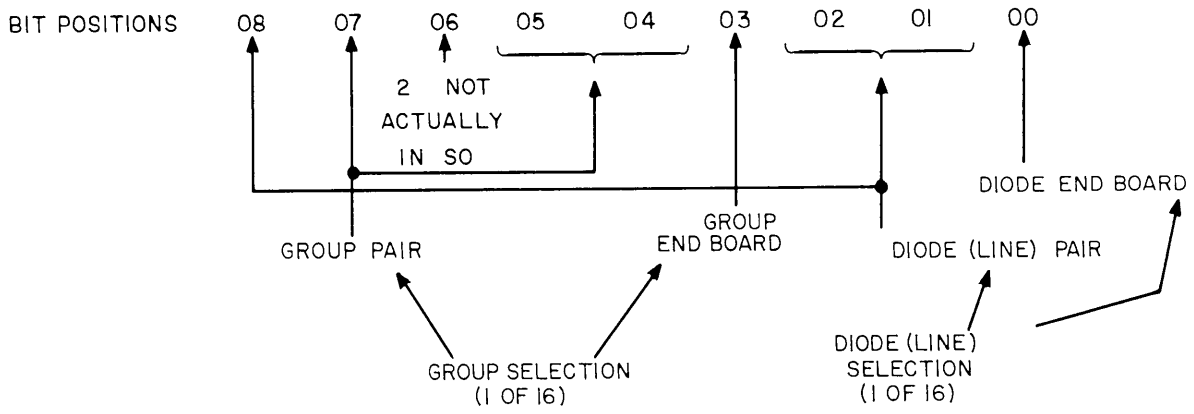


Figure 7.4-1. Control Memory Address Translation From SO

Refer to figure 7.4-2 for the complete 256 word line array.

The word line current flow direction and SO translation levels indicated are for the read operation. The lines are connected at one side to form 16 groups. Line selection is performed at the other end. The write operation performs the same selection except that the SO selection levels shown are reversed. The resulting current through the selected word line is in the direction opposite to that for read. Each line is diode-coupled to the line selection termination which prevents any current other than that through the selected line.

The bottom section shown does not exist for the 128-word memory. In this configuration, there are 16 groups with eight lines per group. Refer to figure 7.4-3 for a detailed connection diagram of a portion of the word lines.

Only 64 lines (eight groups) of the possible 256 word lines are shown. This diagram shows only the read circuits. Group selection is made by the 20WGO- and 10WGO- series gates. The enabling of a group is done by forward biasing the corresponding transistor switch (Q16 through Q2). This applies a ground level to the group. Selection of the transistor switch is made by current flow from the group end board circuit through the associated transformer primary to the group pair circuit.

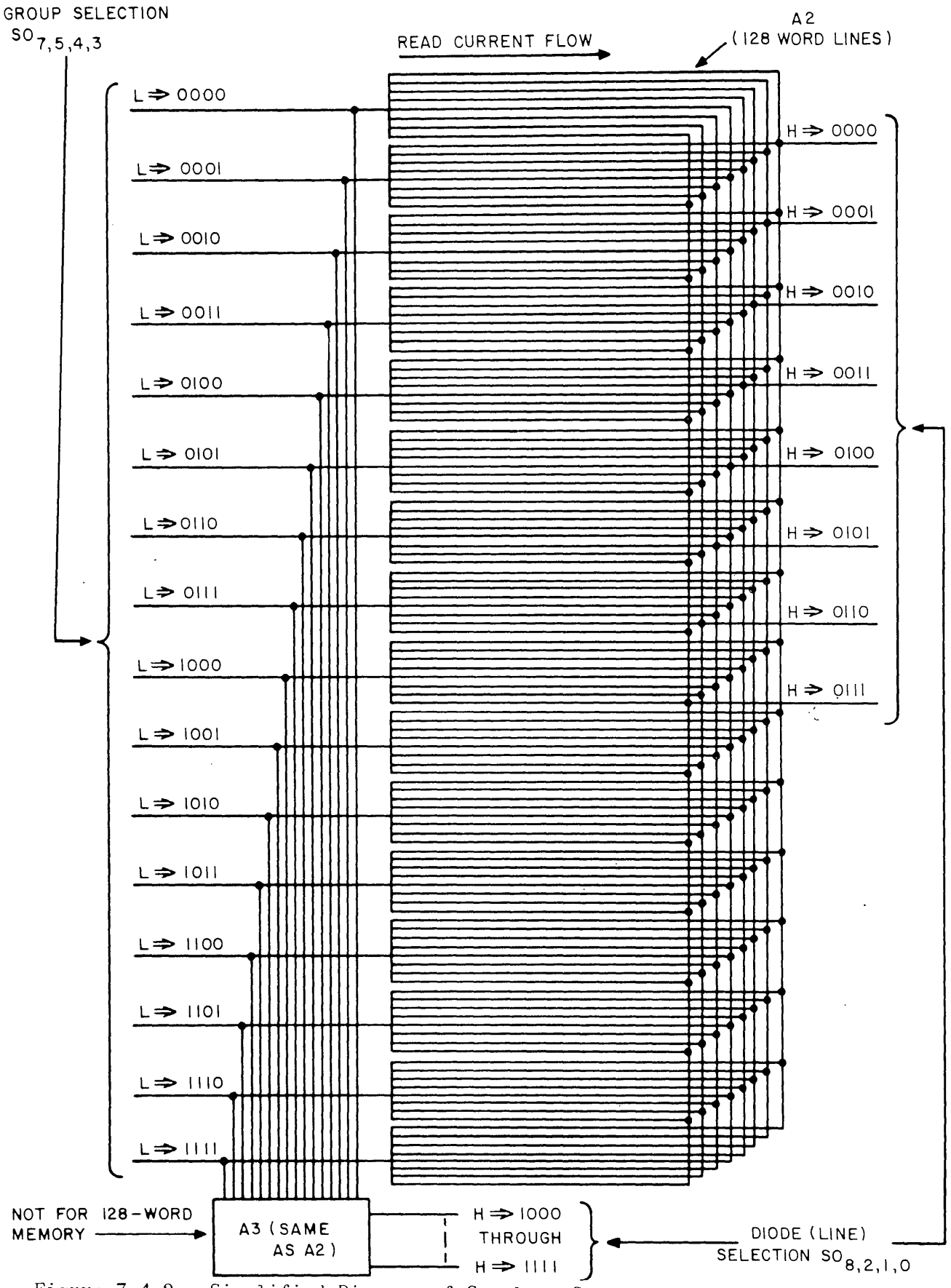


Figure 7.4-2. Simplified Diagram of Complete Control Memory Word Line Array (Read Operation)

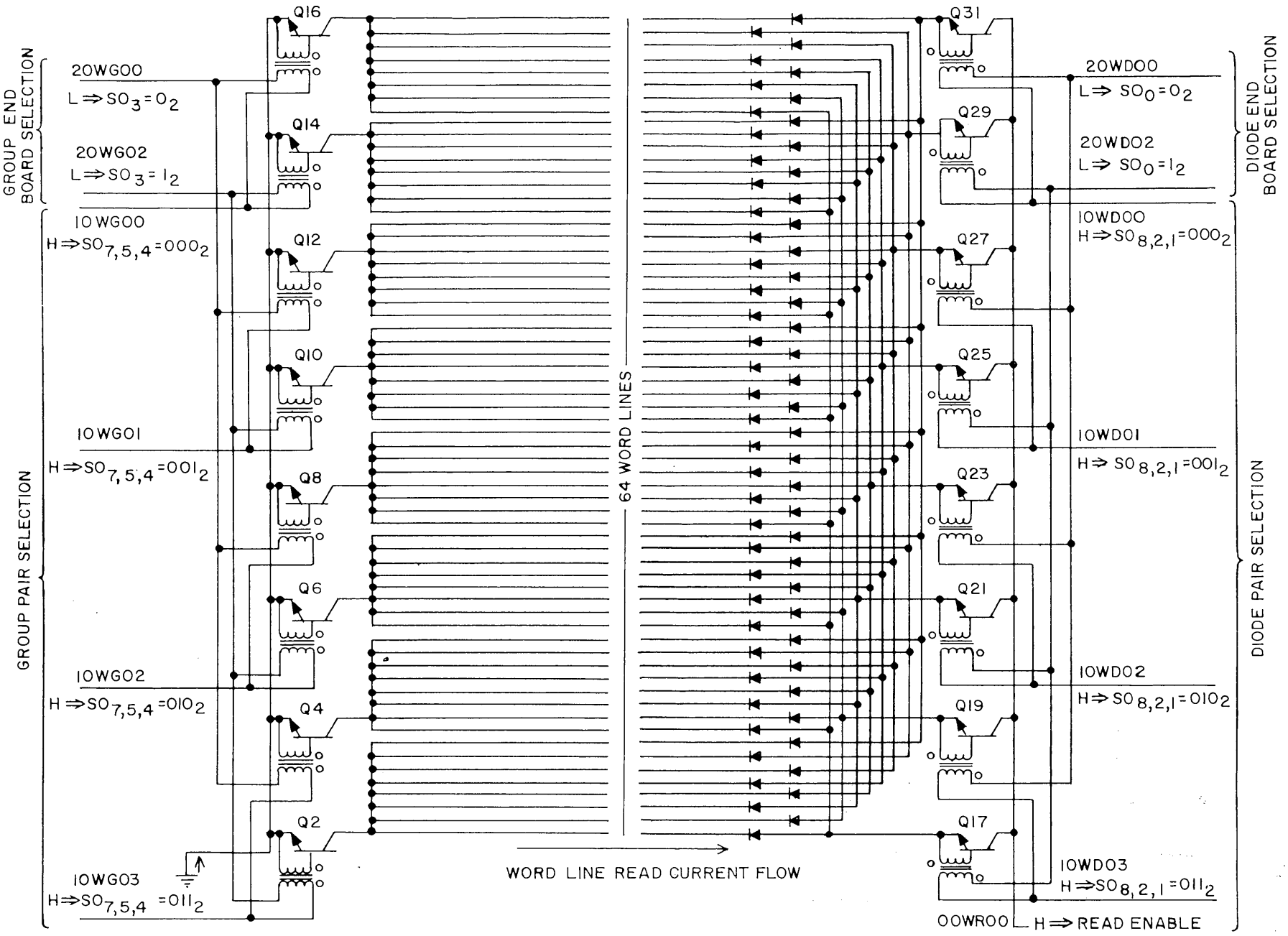


Figure 7.4-3. Detailed Diagram of Partial Control Memory Word Line Connection (Read Operation)

Diode (line) selection is performed in a similar manner with the 20WD0- and 10WD0- series gates. The selected transistor switch (Q31 through Q17) is forward biased and applies a positive voltage to the line from the 00WR00 read current diverter. Word line current flow, therefore, is from group selection to line selection for the read operation. The write circuits are not shown. There are separate transistor switches and transformers for the write operation to cause word line current flow in the opposite direction.

b. Detailed Analysis.

1. Word Line Current.

a) Group Selection. Refer to logic diagrams, figure 9-139 for the group selection logic.

20WG00 through 20WG03 and 10WG00 through 10WG07 perform the selection of group end board and group pair, respectively. 20WG00 and 20WG02 are used for read. 20WG01 and 20WG03 are used for write. The selected 20WG0- gate applies a negative voltage to one side of the group transformer. The selected 10WG0- gate applies a relatively positive voltage to the other side of the group transformer.

b) Line (Diode) Selection. Refer to logic diagrams, figure 9-139 for the line selection logic.

20WD00 through 20WD03 and 10WD00 through 10WD07 perform the selection of diode end board and diode pair, respectively. 20WD00 and 20WD02 are used for read. 20WD01 and 20WD03 are used for write. The selected 20WD0- gate applies a negative voltage to one side of the diode (line) transformer. The selected 10WD0- gate applies a relatively positive voltage to the other side of the diode transformer.

c) Read and Write Current Source. Refer to logic diagrams, figure 9-139 for the read and write current generation circuits.

The source of word line current is the positive regulated voltage supply (+15v) shown. The two current diverters (00WR00 and 00W00) act as switches which are normally closed. That is, they apply a ground level to the two output registers. During the read or write enable signal, the switch is open and the selected word line represents the major load for the regulated voltage supply. The two potentiometers shown are for read and write word current adjustments.

d) Combined Circuits Interconnection. The complete path of read current flow for the address 000_8 word line is analyzed. Refer to figure 7.4-4 for a simplified logic/schematic diagram.

Assuming group end board 0 ($SO_3 = 0_2$) and group pair 0 ($SO_{7,5,4} = 000_2$) to be selected, 20WG00 and 10WG00 cause current flow through the group transformer primary in the direction shown. The resulting secondary voltage forward biases transistor Q16 which applies a ground level to one end of the selected word line. Assuming diode end board 0 and diode pair 0 to be selected, 10WD00 and 20WD00 cause current flow through the diode transformer primary in the direction shown. The resulting

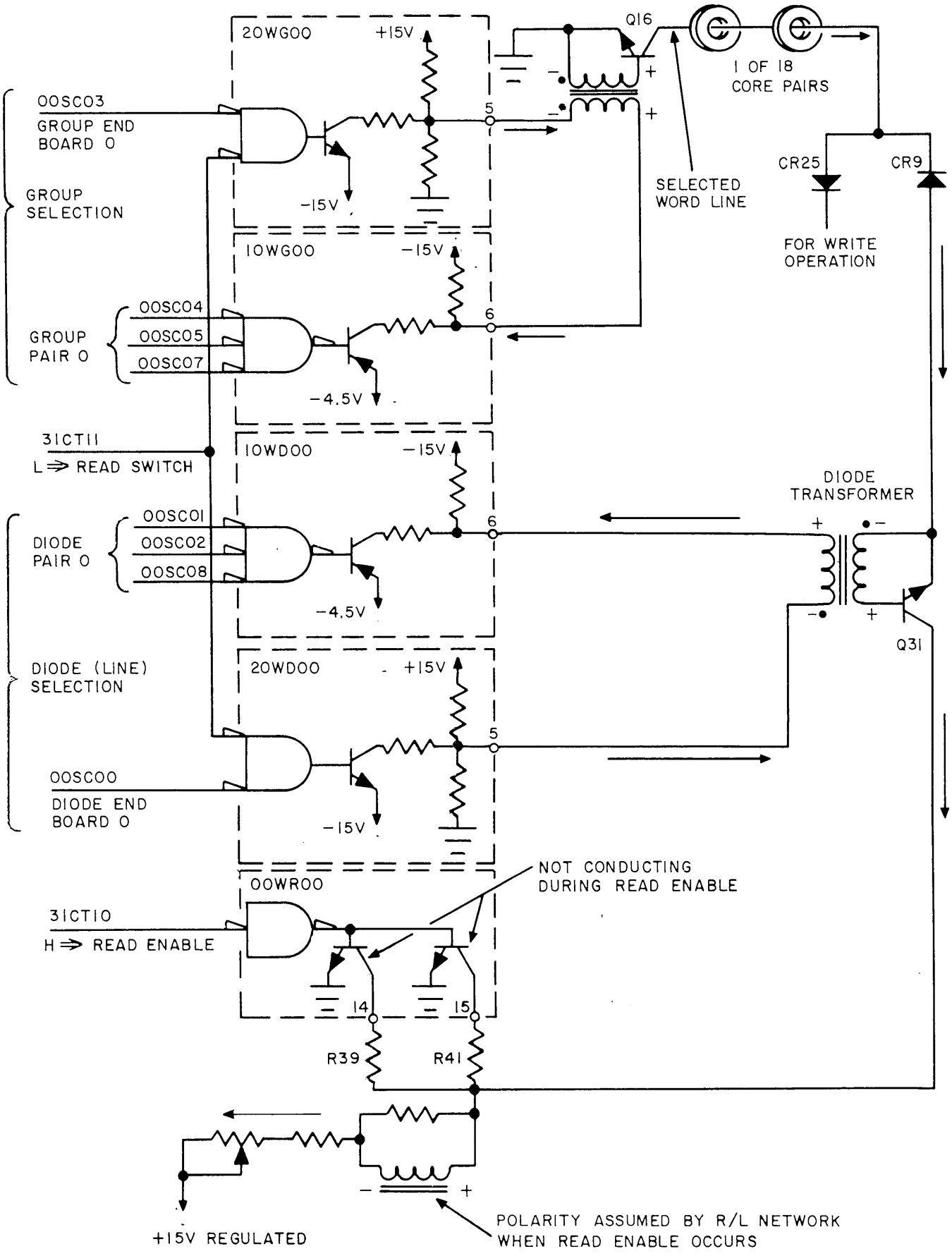


Figure 7.4-4. Simplified Logic/Schematic Diagram of Control Word Drive Circuitry for Read Operation (S0 = 0008)

secondary voltage forward biases transistor Q31 which completes the connection of the word line to the current diverter 00WR00 and the +15 volt supply.

In the absence of the read-enable signal, the two output transistors of 00WR00 are conducting to cause current flow through R39 and R40 to the +15 volt supply. The resulting voltage drop across the R/L network is opposite to that shown. The occurrence of the read-enable cuts off the output transistors of 00WR00. The resulting current change causes the R/L network to develop the voltage polarity shown in an attempt to maintain current flow. Current flow to the +15 volt supply at this time is through the selected word line in the direction shown.

2. Digit Line Current. Digit line current flows only during the write operation. The 18 digit lines intersect the 128 or 256 word lines through the core pairs. Only the 18 core pairs which are threaded by the selected, current-carrying word line are affected (written into).

The direction of digit line current for writing 1_2 is opposite to that for writing 0_2. Thus, the digit line drivers are controlled by Z0. Since each digit line is crossed between each 64 word line section, control is also effected by the address (bit 2^7). Refer to logic diagrams, figures 9-141 and 9-142 for the digit line drivers.

There are two drivers associated with each digit line. The 00DD-- series circuits cause digit line current flow out of pin 13. The 10DD-- series circuits cause current flow into pin 14. Refer to figure 7.4-5 for a simplified logic/schematic diagram.

This diagram concerns only bit 2^0. Depending upon the bit value of $Z0_{00}$ and the address ($S0_7$), one of the two circuits shown will be activated during the digit enable signal. Current flows of both 00DD00 and 10DD00 are shown only for illustration. The digit line passes through all 128 or 256 core pairs for bit 2^0.

3. Sense Line Output. Refer to logic diagrams, figure 9-143 for the sense amplifiers.

The sense lines feed directly into the sense amplifiers 20SA00 through 20SA17. Considering 20SA00 for an example, a positive voltage applied to it on pin 15 with respect to pin 14 indicates a 1_2 has been read from memory. The output will be a positive voltage level in this case. A 0_2 read, indicated by an input voltage of the opposite polarity, causes an open (relatively low level) output. 21SA00 inverts to output a low level for a 1_2. 20SA00 performs a holding function. For some short period of time, 20SA00 will continue to output the indication of the bit value read. This function allows the dropping of the read word line current before the occurrence of the read strobe signal which gates the output of the 21SA-- series circuits to Z0.

4. Initiation of Memory Reference. Refer to logic diagrams, figures 9-24 and 9-107.

91S00 (9-107) outputs a low level if S1 holds a control memory or bootstrap address. At T2.1 time of the proper sequence, 39N10 (9-24), fully enabled, causes S1 $\longrightarrow$ S0 and Initiate CM/Bootstrap (output to 01DT10). The bootstrap flip-flop (9-107) would not be set because of S1 not holding the value $500\text{-}537_8$. This flip-flop being clear causes the control memory/bootstrap timing to reference control memory instead of bootstrap.

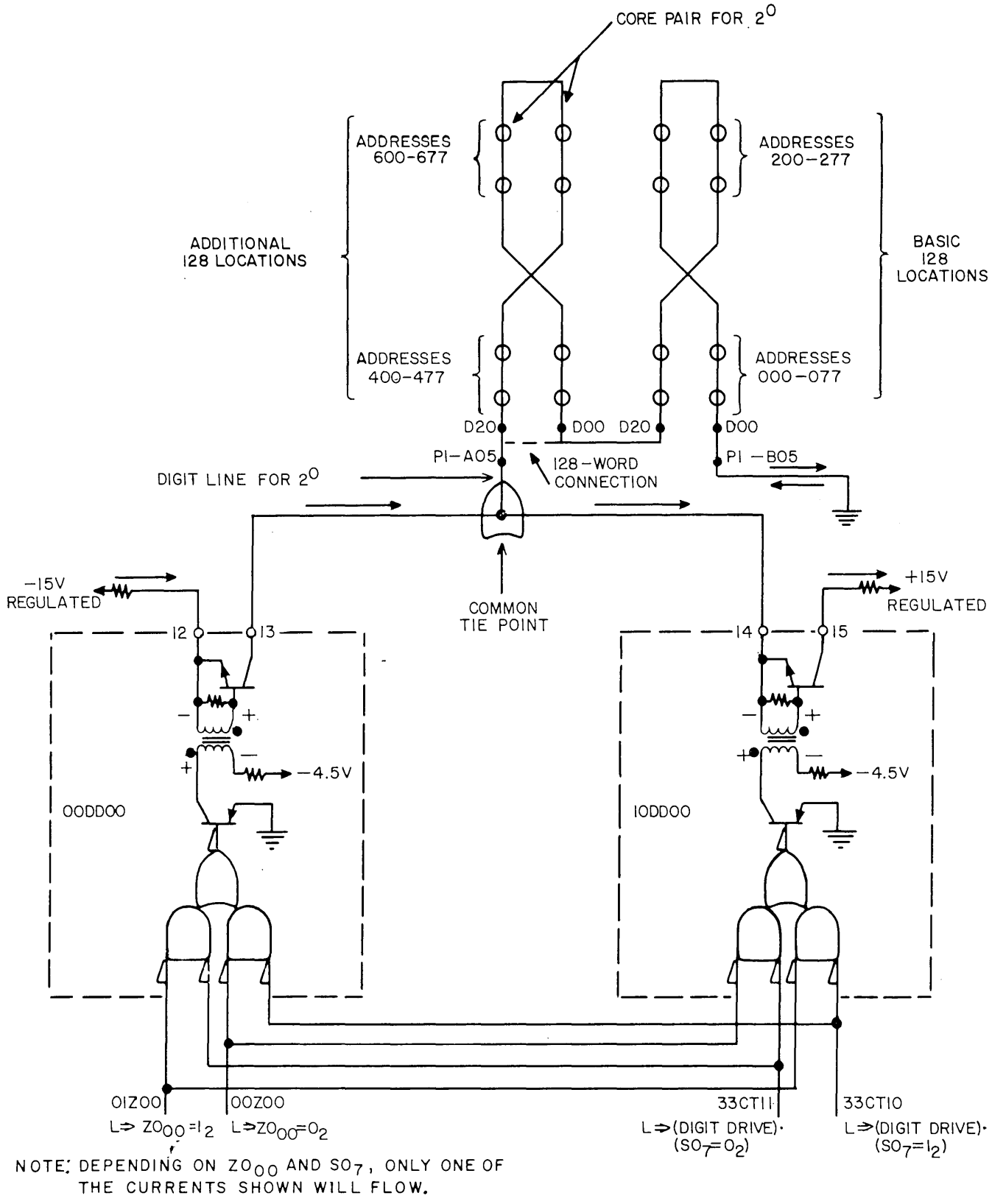


Figure 7.4-5. Simplified Logic/Schematic Diagram of Control Memory Digit Line Circuitry (Bit 2^0)

Also, 10N00 (9-107) is disabled to allow Z0 → Z Select and prevent Z1 → Z Select. Refer to figure 7.4-6 for a block diagram description of the I-sequence operations to obtain an instruction from control memory.

If a store instruction should use a control memory address, the control memory cycle is used in place of main memory. Refer to figure 7.4-7 for a block diagram description of the W-sequence operations to store AL (f = 46, 47) into control memory.

The control memory reference can also be initiated by 19N10, 29N10, and 49N10 (9-24). These gates place the address directly in S0 and initiate the memory timing by their outputs to 01DT10.

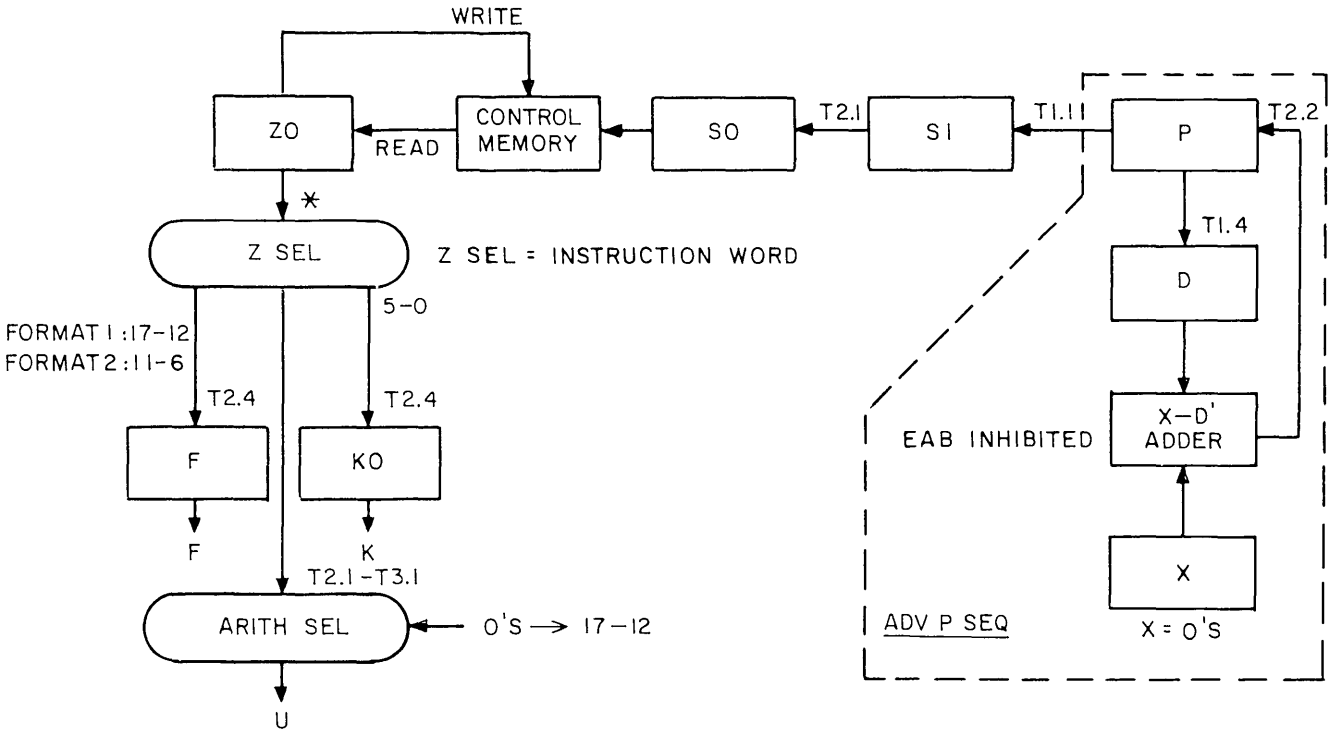
5. Memory Timing. Refer to logic diagrams, figure 9-137 for the timing logic.

Control memory used the same timing source as used by bootstrap. Memory access time is approximately 250 nanoseconds. Timing is initiated at the setting of the 0XDT10 flip-flop. Refer to figure 7.4-8 for the timing waveforms. This analysis is theoretical in that transient times through the gates are not considered.

7.4-5. SUMMARY

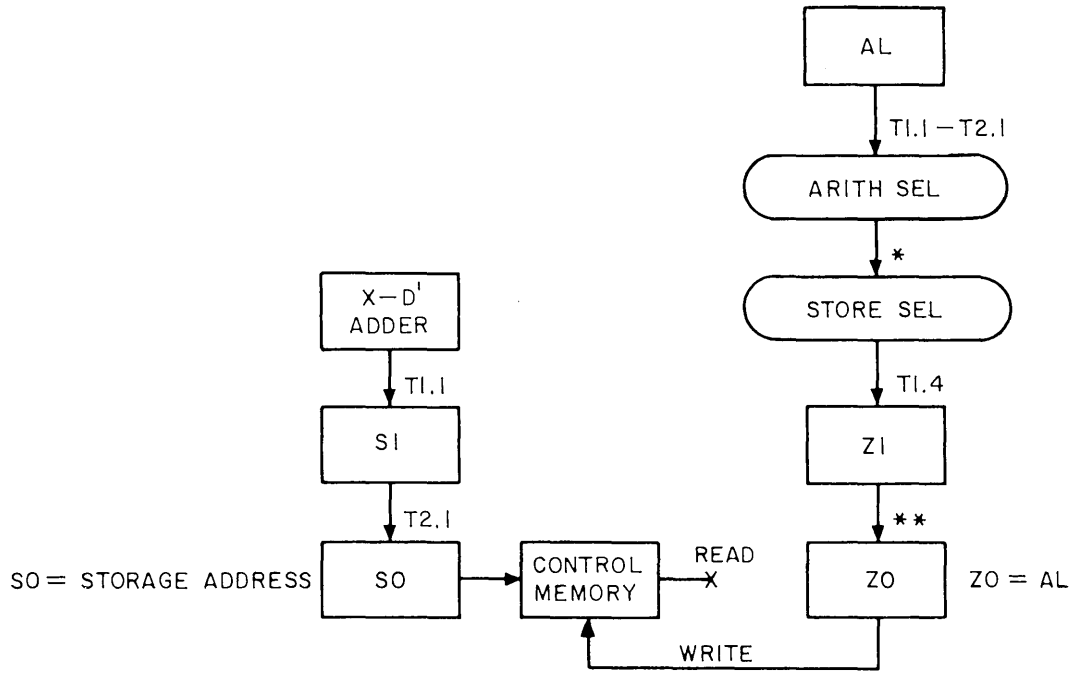
The enabling of one word line is made by group and line (diode) selections. Word line current flow has a duration of approximately 80 nanoseconds. Memory access time is approximately 250 nanoseconds. Word line current flows for both read and write, but in opposite directions. Digit line current flows during the write operation only. Its direction is dependent upon the binary value to be written and the address. The sense line outputs are applied to Z0 and are gated by the strobe signal.

The control memory reference is initiated on a Ø1 and its cycle is complete before the next Ø1.



NOTE: * ZO → Z SEL OCCURS AS LONG AS SI = CM ADDRESS.

Figure 7.4-6. I Sequence Data Flow Referencing Control Memory



NOTES: *ARITH SEL → STORE SEL OCCURS FOR ENTIRE W SEQUENCE.

**ZI → ZO IS TIMED BY CM TIMING.

Figure 7.4-7. W Sequence Data Flow for f = 46, 47 With Storage Address in Control Memory

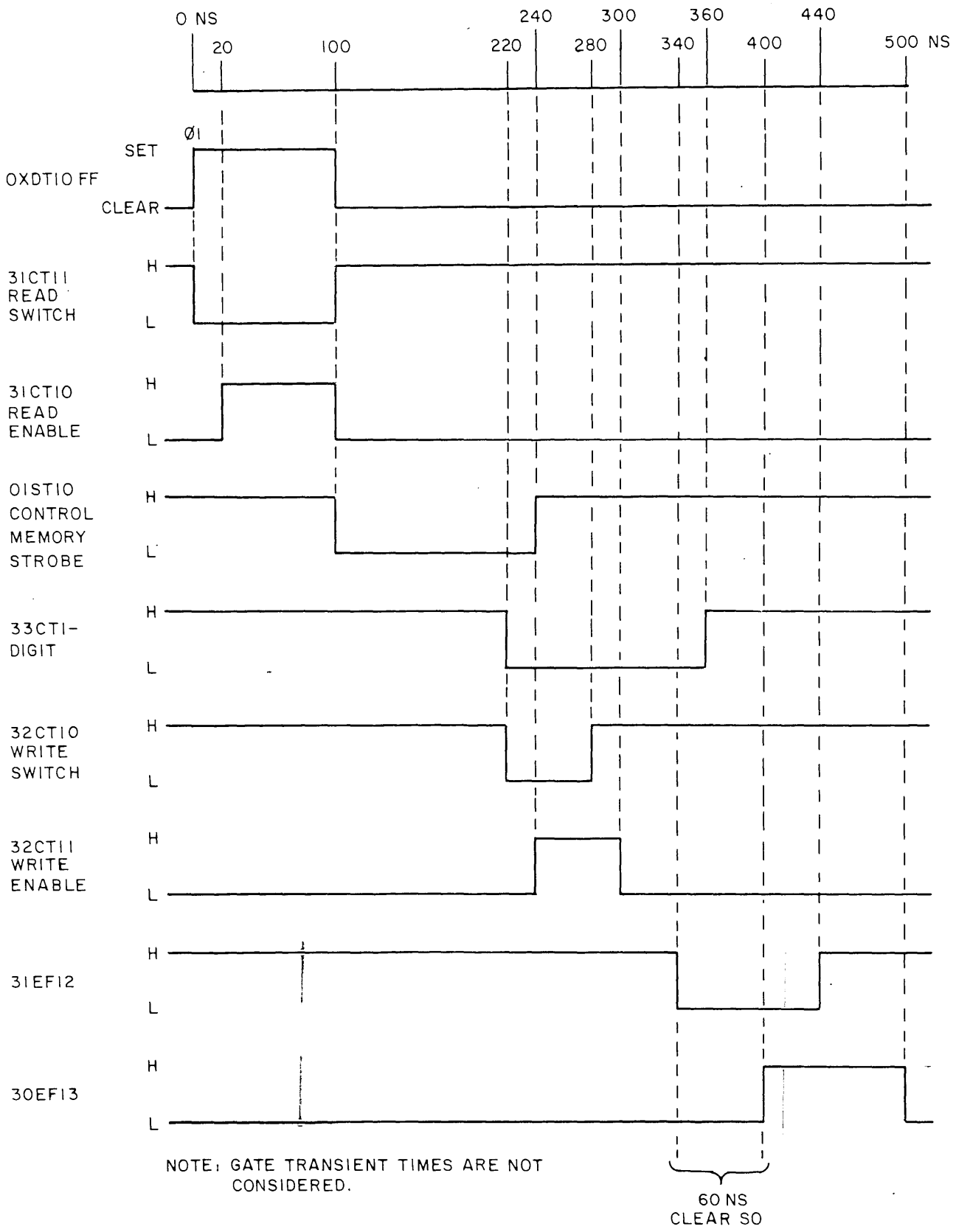


Figure 7.4-8. Control Memory Theoretical Timing

SECTION 7 - MEMORY SECTION

7.5. GENERAL DESCRIPTION OF BOOTSTRAP MEMORY

7.5-1. OBJECTIVES

To present the general description of bootstrap memory.

7.5-2. INTRODUCTION

Bootstrap memory has 32_{10} locations for storage of 18-bit words. The program contained therein is hard-wired and consists of a short load routine for some particular peripheral input device. Cycle time is 500 nanoseconds. However, when bootstrap is referenced, its rapid cycle time is not utilized. The effective cycle time is 2 microseconds.

7.5-3. REFERENCES

UNIVAC 1219 Technical Manual, Volume I, Paragraph 4-5d.

7.5-4. INFORMATION

a. Storage Element. As storage elements, bootstrap memory uses ferromagnetic core transformers. There is one transformer for each bit position which is shared by all 32 addresses. The transformer secondary winding is the sense line. The primary winding is simply a current-carrying drive line. If a 1_2 is desired in a particular bit position, the drive line is threaded through the associated core to produce secondary current. If a 0_2 is desired, the drive line bypasses the core. The sense line (secondary winding), therefore, carries no current for the 0_2 configuration. Refer to figure 7.5-1 for an illustration of one core transformer showing both the 1_2 and 0_2 configurations.

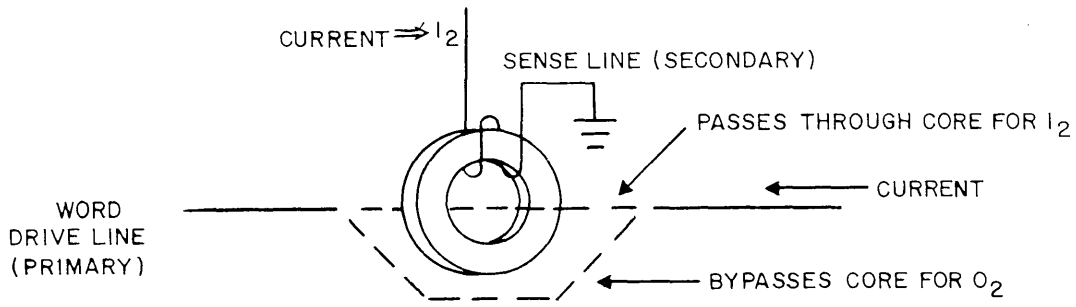


Figure 7.5-1. Core Transformer

b. Read-out Operation. The bootstrap addresses are 00500_8 through 00537_8.

There is one word drive line for each address. For a particular memory reference, only the one word line corresponding to the address is activated with current. Each word line determines the binary content of its address by the pattern in which it is threaded through and around the cores. Refer to figure 7.5-2 for an example showing the configuration for the first two bootstrap addresses.

Only two of the 32 word drive lines are shown. Notice that the sense lines are gated directly to the Z0 register. The magnitude of the sense line voltage is sufficient to set the Z0 flip-flop without amplification. The -4.5 voltage and diodes are used to prevent the sense line voltage from rising more negative than -4.5 volts.

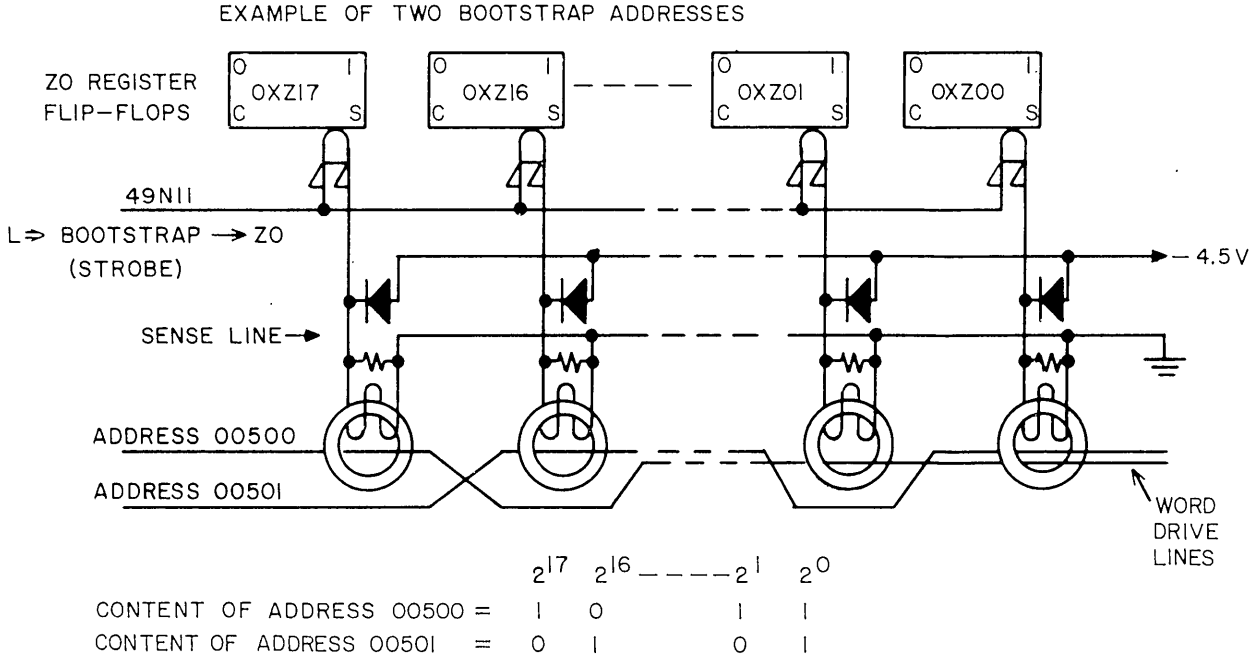


Figure 7.5-2. Example of Two Bootstrap Addresses

Since the read operation is not destructive to the information contained in bootstrap memory, no write operation is necessary.

c. Physical Arrangement. The entire memory is contained in one plug-in module comprised of four cards. The module is located in chassis 8. The transformer cores are attached to three of these cards and are threaded serially by the 32 word drive lines according to the binary content. The bootstrap load routine can be changed by inserting a different module. Refer to the UNIVAC 1219 Technical Manual, Volume I, Section 4, figure 4-58 for a picture of the bootstrap module.

7.5-5. SUMMARY

Bootstrap memory has 32 locations for 18-bit words. The storage device is a core transformer. The secondary winding is the sense line which inputs to the Z0 register. There are 32 primary windings (word drive lines). Only one of these

lines carries current during a bootstrap memory reference. The binary content is hard-wired by the pattern in which the word drive lines are threaded through or around the core transformers.

The content of bootstrap is a short load routine. Different bootstrap modules can be inserted to change the load routine.

SECTION 7 - MEMORY SECTION

7.6. BOOTSTRAP MEMORY INTERNAL OPERATION

7.6-1. OBJECTIVES

To present the detailed theory of operation involved in the internal operation of bootstrap memory.

7.6-2. INTRODUCTION

Bootstrap memory has circuitry which selects one of 32 word drive lines. The threading pattern of the selected line causes the desired binary output from the sense lines of the 18 core transformers.

7.6-3. REFERENCES

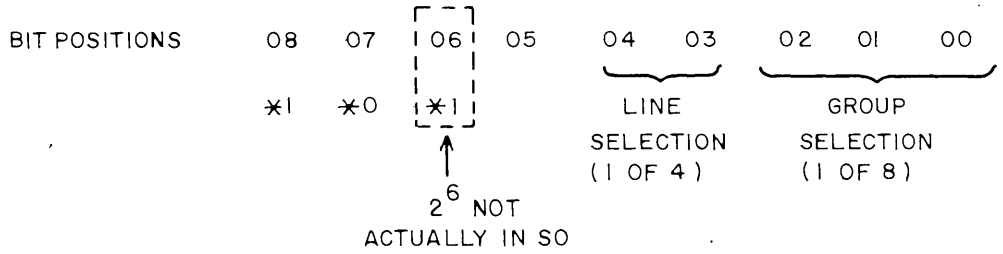
a. UNIVAC 1219 Technical Manual, Volume I, Paragraph 4-5d.

b. UNIVAC 1219 Technical Manual, Volume II, Section 9 (logic diagrams).

7.6-4. INFORMATION

a. General Description. Of the 32 word drive lines, one is selected during each bootstrap memory reference. This line carries current for approximately 120 nanoseconds. Each core transformer, through which the line passes, develops a secondary voltage in the sense line. This voltage represents a 1_2 read out of bootstrap.

The drive lines are considered to be in eight groups of eight lines each. Drive line selection is made by enabling one group and one line of that group. The bootstrap address is placed in S0. The bit configuration of S0 is translated into group and line. Refer to figure 7.6-1 for the translation of S0.



NOTE: * THESE DIGITS ARE "CONSTANTS" OF THE BOOTSTRAP ADDRESSES ($500_8 - 537_8$)

Figure 7.6-1. Bootstrap Address Translation From S0

Refer to figure 7.6-2 for a simplified diagram of the drive line array.

As shown, the lines are connected at one side to form eight groups of four lines per group. Group selection is made by the 00BG0-series gates. The selected group of lines has a positive voltage applied from the 00BG0- gate.

The connection at the other end forms line selection. One of the 10BD-0 series gates is enabled to select one of the four lines by applying a negative voltage. The resulting current flow is from the line selection gate, through the diode, through the selected word drive line which passes through or around the 18 core transformers, and into the group selection gate. The diodes prevent more than one word line carrying current.

b. Detailed Analysis.

1. Drive Line Current.

a) Group Selection. Refer to logic diagrams, figure 9-144 for the group selection logic.

00BG00 through 00BG07 perform the selection. The common input to these circuits labeled "Enable Bootstrap" is the timing signal. Its duration is approximately 120 nanoseconds. The other inputs are from SO_{02-00}. The fully enabled 00BG0- circuit acts as a switch between its two output pins. This applies a positive voltage to the group from the +15 volt supply shown.

b) Line Selection. Refer to logic diagrams, figure 9-144 for the line selection logic.

10BD00 through 10BD30 perform the selection. These circuits are timed by the same "Enable Bootstrap" signal used for group selection. The other inputs are from $SO_{04,03}$. The fully enabled 10BD-0 circuit acts as a switch between its two output pins. This applies a negative voltage to the lines from the -15 volt supply shown.

c) Combined Circuits Interconnection. The complete path of current flow for the address 500_8 word drive line is analyzed. Refer to figure 7.6-3 for a simplifed logic/schematic diagram.

Assuming group 0 to be selected, 00BG00 applies a positive voltage to the drive line. The AND gate is actually part of the 00BG00 circuit. When fully enabled, the output transistor conducts. Assuming line 0 to be selected, 10BD00 applies a negative voltage to the other end of the drive line. Current flows in the direction shown, either through or around each of the 18 core transformers depending upon the desired binary content of this address.

2. Sense Line Output. Refer to study guide sheet number 7.5, figure 7.5-2 for the sense line arrangement.

Each core transformer has a sense line as its secondary winding. A voltage is induced in the sense line only if the current-carrying word drive line is threaded through the core (1_2). The sense line voltage polarity is such that it applies a negative voltage, which is limited to - 4.5 volts by the diode, to the associated

Z0 flip-flop setting AND gate. The strobe signal from 49N11 allows the 18-bit word read-out to set Z0. The strobe occurs during the word drive line current flow.

Refer to logic diagrams, figure 9-145 for all 18 core transformers and their outputs.

The eight inputs from the left side perform group selection. The four inputs from the right side perform line selection. The 18 sense line outputs are directly connected to the set side of the corresponding Z0 flip-flops. From left to right, the sense line output destinations are 01Z17 through 01Z00. The common connection made directly to each sense line is grounded (via card pin 15).

3. Initiation of Memory Reference. Refer to logic diagrams, figures 9-24 and 9-107.

91S00 (9-107) outputs a low level if S1 holds a bootstrap or control memory address. At T2.1 time of the proper sequence, 39N10 (9-24), fully enabled, causes S1 → S0 and Initiate CM/Bootstrap (output to 01DT10). Also the output to 01S09 (9-107) sets the Bootstrap flip-flop if S1 = $500\text{-}537_8$. This flip-flop being set causes the control memory/bootstrap timing to reference bootstrap instead of control memory.

Also, 10N00 (9-107) is disabled to allow Z0 → Z Select and prevent Z1 → Z Select. Refer to figure 7.6-4 for a block diagram description of the I-sequence operations to obtain an instruction from bootstrap memory.

4. Memory Timing. Refer to logic diagrams, figure 9-137 for the timing logic.

Bootstrap memory uses the same timing source as used by control memory; however, bootstrap does not have a write (restore) operation. Memory access time is approximately 250 nanoseconds. Timing is initiated at the setting of the 0XDT10 flip-flop. Refer to figure 7.6-5 for the timing waveforms. This analysis is theoretical in that transient times through the gates are not considered.

7.6-5. SUMMARY

The enabling of one word drive line is made by group and line selections. The selection circuitry also supplies the drive line current. Drive current flow has a duration of approximately 120 nanoseconds. Memory access time is approximately 250 nanoseconds. The sense line outputs are applied directly to the Z0 flip-flops. Gating is accomplished with the strobe signal.

The bootstrap memory reference is initiated at T2.1 time if S1 holds $00500\text{-}00537_8$.

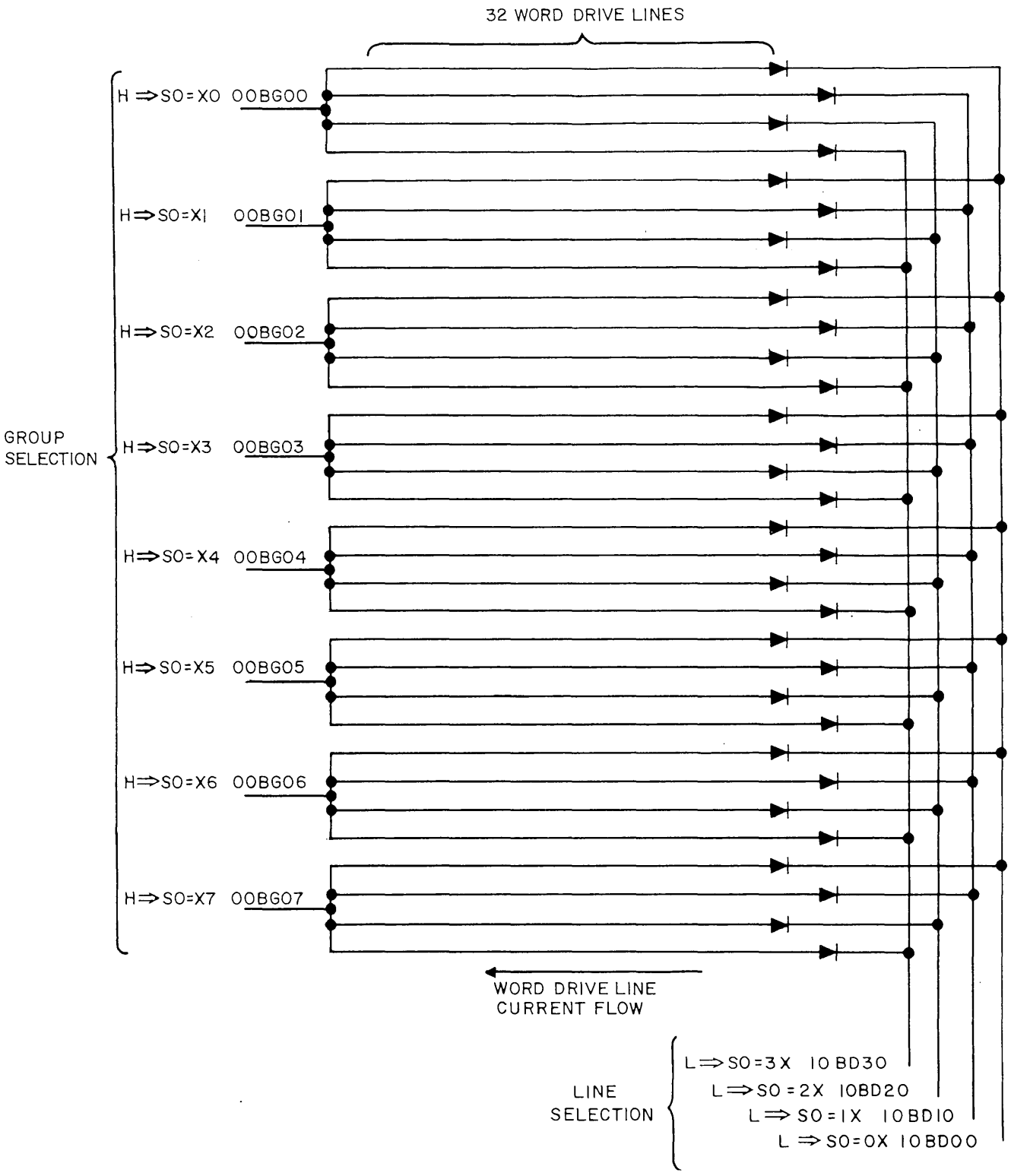


Figure 7.6-2. Simplified Diagram of Bootstrap Drive Lines

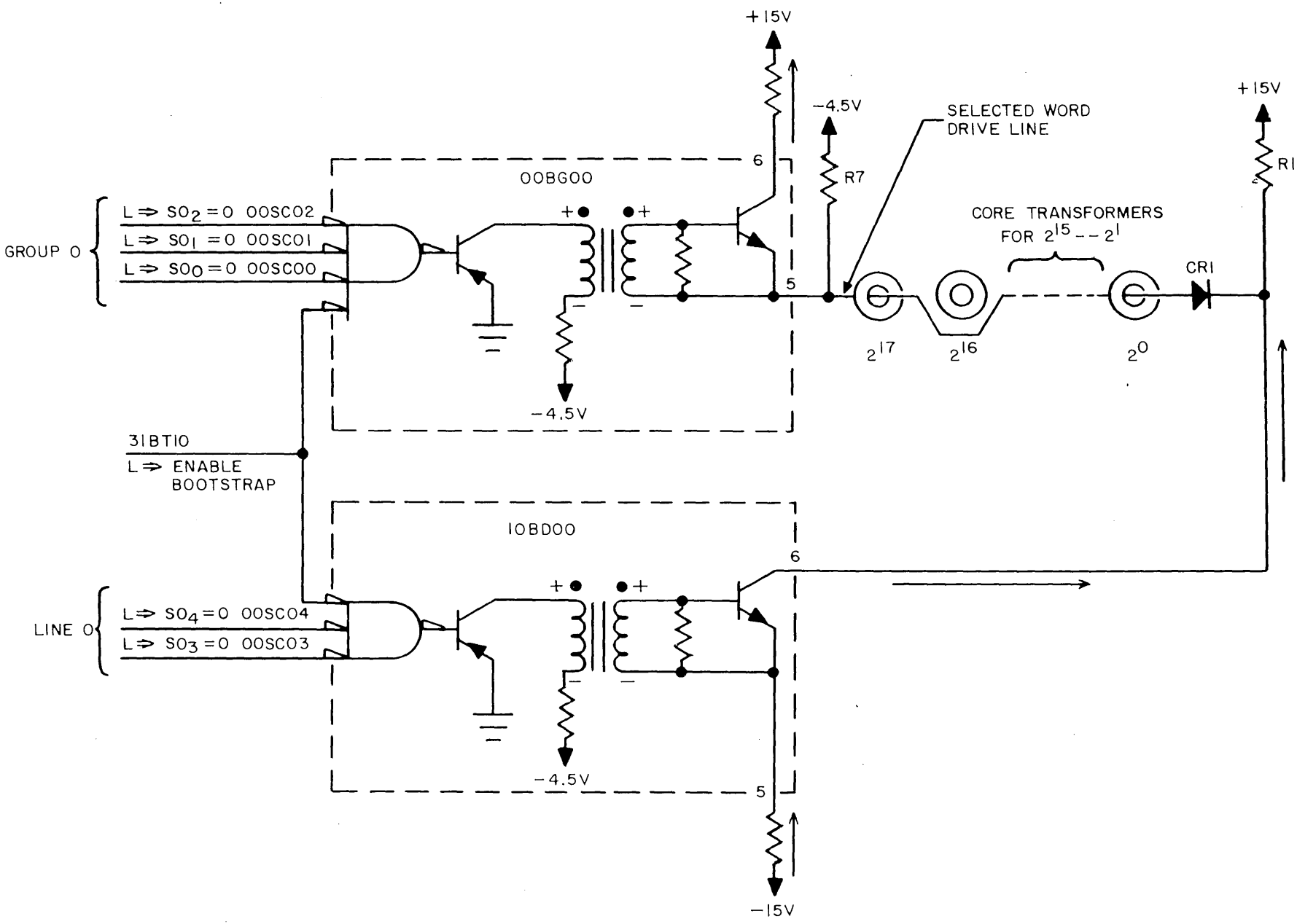
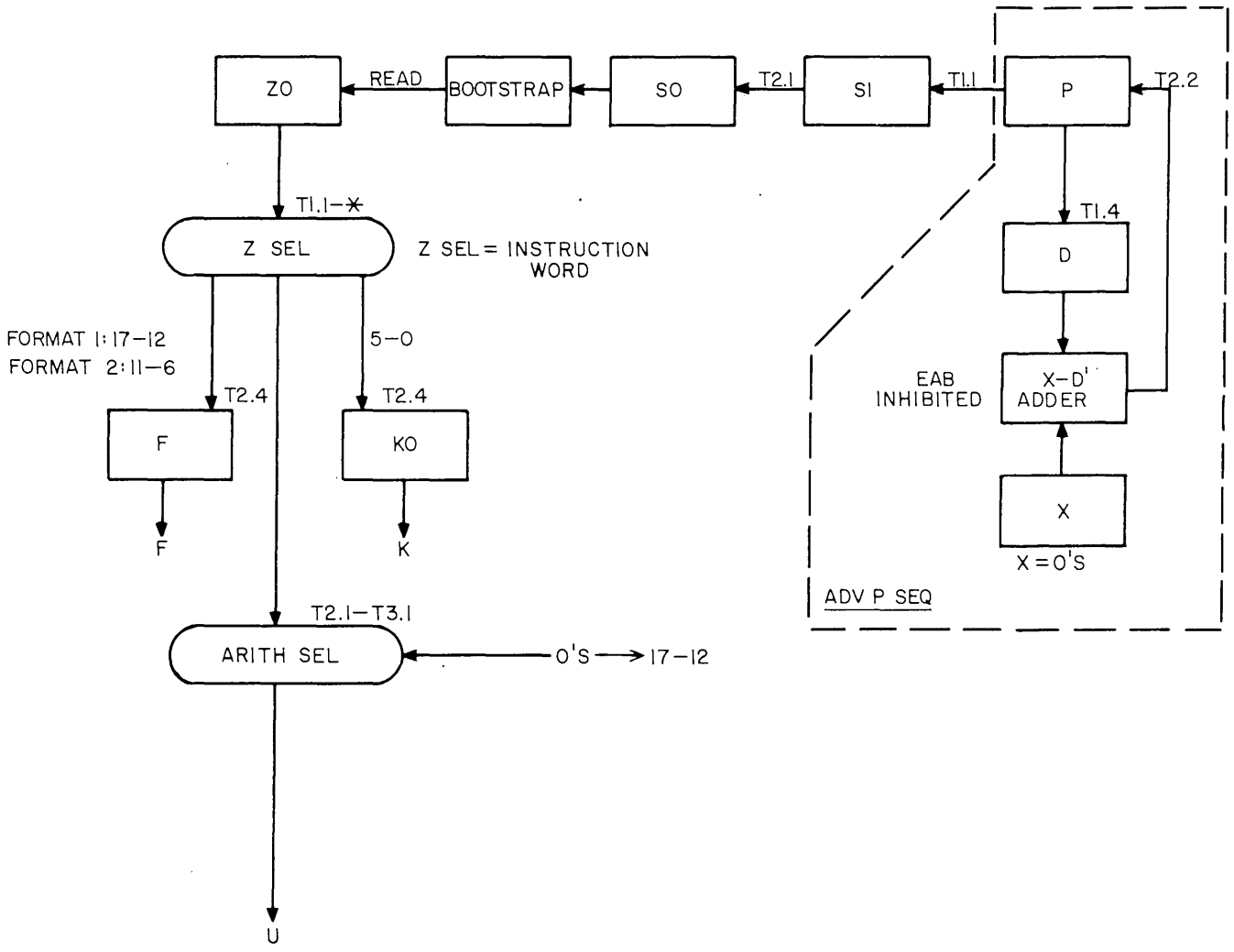
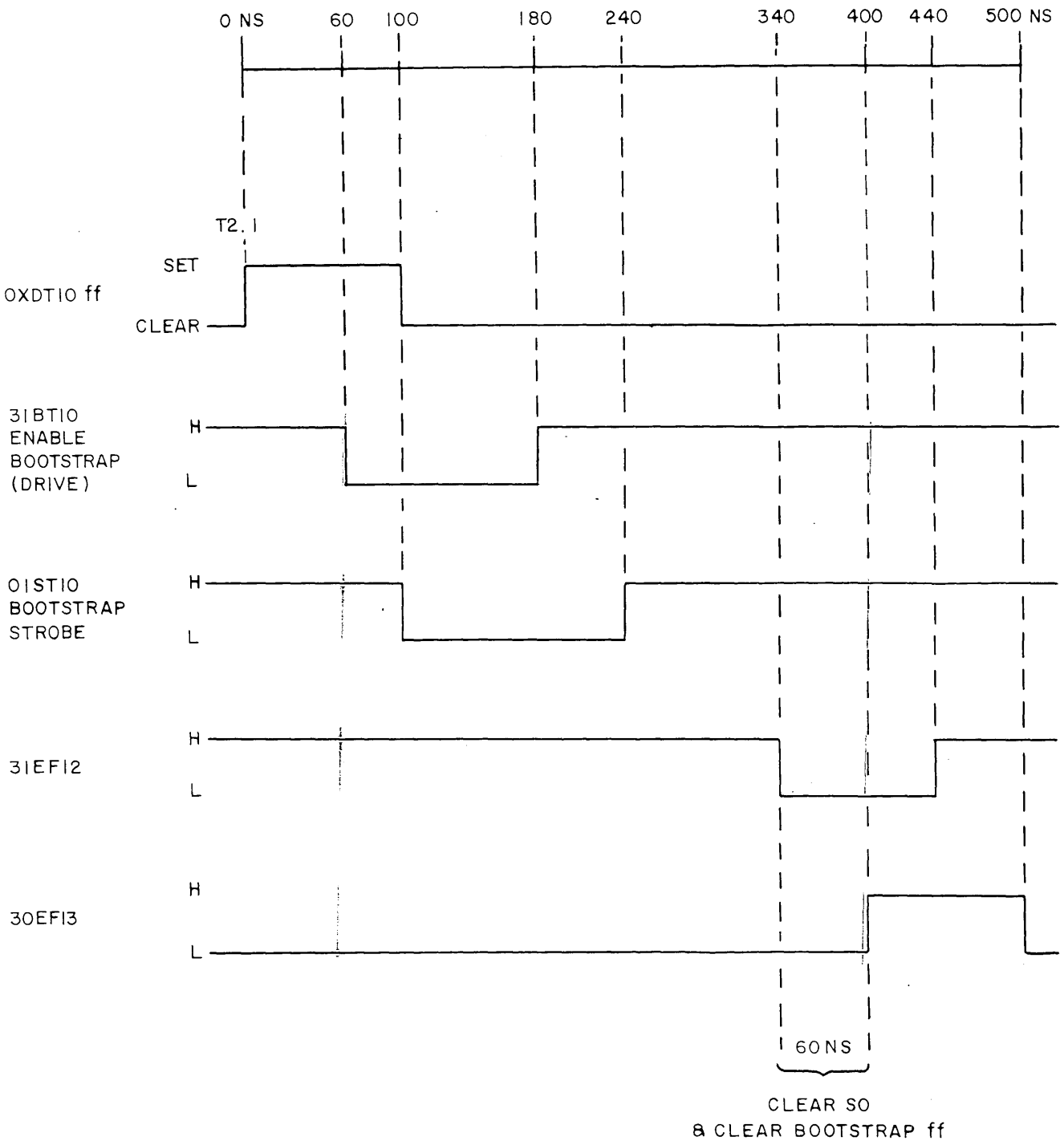


Figure 7.6-3. Simplified Logic/Schematic Diagram of Bootstrap Drive Circuitry (Group 0 & Line 0)



NOTES: ONLY THE INSTRUCTION READ-OUT AND P ADVANCEMENT OPERATIONS ARE SHOWN.
OTHER I SEQUENCE EVENTS ARE AS NORMAL.
*Z0 ⟶ Z SEL OCCURS AS LONG AS S1 = BOOTSTRAP ADDRESS.

Figure 7.6-4. I-Sequence Data Flow Referencing Bootstrap



NOTE: GATE TRANSIENT TIMES ARE NOT CONSIDERED.

Figure 7.6-5. Bootstrap Memory Theoretical Timing