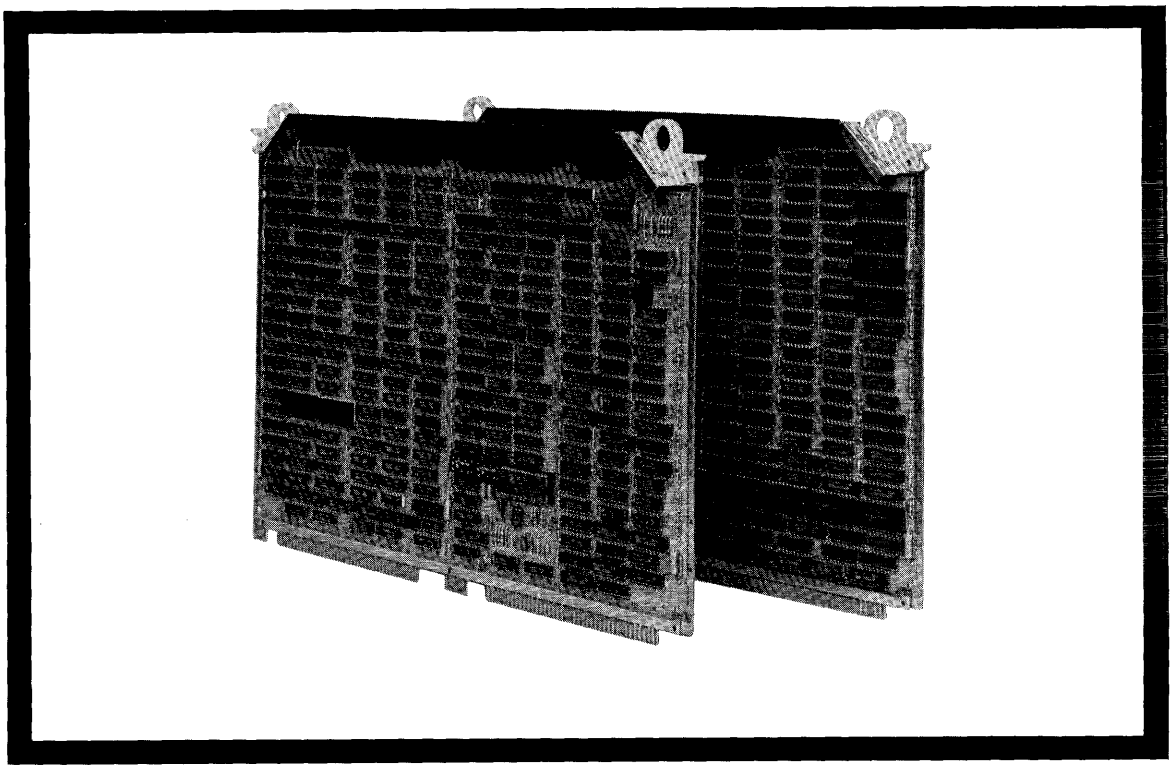
DEPOT THEORY AND MAINTENANCE

Model 990/12 LR Computer



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The computers offered in this agreement, as well as the programs that TI has created to use with them, are tools that can help people better manage the information used in their business; but tools—including TI computers—cannot replace sound judgment nor make the manager's business decisions.

Consequently, TI cannot warrant that its systems are suitable for any specific customer application. The manager must rely on personal judgment of what is best for his or her business.

Preface

The *990/12 LR Computer, Depot Theory and Maintenance*, when combined with the *990/12 LR Computer, General Description*, provides depot level maintenance information required to service the Model 990/12 Low Radiation (LR) Arithmetic Unit (AU) and System Memory Interface (SMI) boards.

These manuals are specifically limited to information on the 990/12 LR AU and SMI boards, and do not describe the many Texas Instruments 990-family computers and computing systems that include the 990/12 LR AU and SMI boards.

Section

1 Detailed Functional Description — Provides a detailed functional description of the two boards that comprise the Central Processing Unit (CPU).

2 Maintenance — Provides depot-level maintenance procedures using a special test system, the 990/12 LR Functional Verification System, to test the CPU boards.

3 Drawings — Provides CPU board assembly drawings and logic diagrams.

The following manuals also describe the 990/12 LR Central Processing Unit:

Title	Part Number
Model 990/12 LR Computer, General Description (available as part of manual kit 2268237-0001)	2268239-9701
Model 990/12 LR Computer, Field Theory and Maintenance (available as part of manual kit 2268237-0001)	2268240-9701

Contents

Illustrations

Tables

1

Detailed Functional Description

1.1 INTRODUCTION

Your depot maintenance manual kit is not complete without *Model 990/12 LR Computer, General Description*, part number 2268239-9701. A general description manual serves as an introduction to a field or depot manual kit. General introductory information, specifications, installation data, operator instructions, and operator preventative maintenance appear in the general description manual.

Model 990/12 LR Computer, Depot Theory and Maintenance starts where the general description ends. This manual contains depot-level operation and maintenance information for the 990/12 LR CPU, manufactured by Texas Instruments Incorporated.

This section describes the arithmetic unit (AU) to system memory interface (SMI) board interface and provides a detailed functional description of the 990/12 LR AU and SMI boards.

1.2 AU to SMI BOARD INTERFACE

The interface between the AU and SMI boards is made by two short ribbon cables connected to connectors P3 and P4 on the top edge of each board. Pin assignments are the same for each board. Table 1-1 describes pin assignments and interface signal functions.

Table 1-1. AU board to SMI Board Interface Pin Assignments and Functions

Signature	Pin	I/O*	Description
ADDR(15)— (LSB)	P3-2	OUT	ADDR(0)— through ADDR(15)— comprise the address bus.
ADDR(14)—	P3-3	OUT	
ADDR(13)—	P3-4	OUT	
ADDR(12)—	P3-5	OUT	
ADDR(11)—	P3-6	OUT	
ADDR(10)—	P3-7	OUT	
ADDR(9)—	P3-8	OUT	
ADDR(8)—	P3-9	OUT	
ADDR(7)—	P3-10	OUT	
ADDR(6)—	P3-11	OUT	
ADDR(5)—	P3-12	OUT	
ADDR(4)—	P3-13	OUT	
ADDR(3)—	P3-14	OUT	
ADDR(2)—	P3-15	OUT	
ADDR(1)—	P3-16	OUT	
ADDR(0)— (MSB)	P3-17	OUT	
INTPRES—	P3-19	IN	Interrupt present. When active (low), it indicates that an interrupt is requested. If active, the processor selects the data on the interrupt code input lines, ILEV(0)— through ILEV(3)—, for comparison to the interrupt bits of the status register (ST). If an equal or higher priority than the enabled interrupt level is determined (interrupt code equal to or less than ST bits 12 through 15), the processor interrupt sequence is initiated. If the comparison fails, the processor ignores the request. INTPRES— remains active and the processor continues to sample the interrupt-code input lines until the program enables a priority low enough to accept the request interrupt.
ILEV(0)—	P3-21	IN	Interrupt-code input lines that are sampled when INTPRES— active.
ILEV(1)—	P3-22	IN	
ILEV(2)—	P3-23	IN	
ILEV(3)—	P3-24	IN	
ENCREG—	P3-26	OUT	Becomes active (low) during overlap conditions to ensure proper loading of the map file.
FPINT—	P3-27	IN	Permits front panel interrupts even though the Disable Interrupt instruction (DINT) has been invoked.
IERRINT	P3-28	IN	Signals to the AU that the level 2 interrupt pending is an actual error condition.

Note:

* I/O refers to the AU board.

Table 1-1. AU board to SMI Board Interface Pin Assignments and Functions (Continued)

Signature	Pin	I/O*	Description
ST7—	P3-30	OUT	ST bit 7. Privileged instructions execute only when register bit 7 equals 0 (ST7— equals 1).
ST8	P3-31	OUT	ST8 is the map file select. When ST bit 8 equals 0, map file 0 is selected; when ST bit 8 equals 1, map file 1 is selected.
ST9—	P3-32	OUT	Memory management and protection flag. The flag is enabled when ST9— equals 1 (ST9 equals 0).
CLKON—	P3-34	OUT	Active (low) in response to the CKON instruction to enable the real-time clock.
CLKOFF—	P3-35	OUT	Active (low) in response to the CKOF instruction to disable the real-time clock.
PRIVOP—	P3-36	OUT	Signal generated by processor to indicate a privileged instruction fetch attempt when the processor is not in the privileged mode (ST bit 7 equals 1).
ILLOPST—	P3-37	OUT	Signal generated by processor to indicate that an illegal operation code has been decoded.
MPFILE(0)— MPFILE(1)—	P3-38 P3-39	OUT OUT	Control code signals generated by the processor as map file select signals and applied to a map select register on the SMI board to select map file 0, 1, 2, or 3.
LMF—	P3-40	OUT	An active (low) signal from the processor indicating that a map file load is in progress.
IDLE—	P3-42	OUT	A signal from the processor to the SMI board indicating that the processor is in the idle mode.
SMILED—	P3-43	OUT	A signal from the processor to the SMI board that lights the FAULT indicator on the SMI board indicating an SMI board failure.
INVADDR—	P3-45	OUT	A control signal from the processor that, when low, enables inverted address bus data to the SMI board; when high, it enables noninverted address bus data to the SMI board.

Note:

* I/O refers to the AU board.

Table 1-1. AU board to SMI Board Interface Pin Assignments and Functions (Continued)

Signature	Pin	I/O*	Description
SYSCLKA—	P3-47	IN	Clock signal generated on the SMI board, used to drive the AU board main clock.
SYSCLKB—	P3-49	IN	Clock signal generated on the SMI board used to drive the AU board. This clock is the control store clock, and its shape is modified during the long 482 cycles to clock the control store in the middle of the cycle.
OVERFLOW—	P4-1	OUT	A signal from the processor indicating arithmetic overflow.
OVERLAP—	P4-3	IN	Signal generated by the SMI whenever the address being mapped is greater than or equal to the WP and less than the WP plus 32. Any address mapped outside the current map file is not overlapped.
CRA(0)— CRA(1)— CRA(2)— CRA(3)—	P4-4 P4-5 P4-6 P4-7	IN IN IN IN	The AU board is the source for this bus during workspace cache demand fill microcycles, and the SMI board is the source at all other times. In each case, this bus contains the workspace register number.
MEMCYC—	P4-9	OUT	When active (low), indicates that the next clock period is for a memory cycle.
READ	P4-10	OUT	When high, indicates that the memory cycle request is for a read cycle. READ is latched on the SMI board.
LDMAP—	P4-12	OUT	When low, requests a map cycle during the present state. Enables clocks for memory mapping base selection and mapped address latch logic.
CACHINHB—	P4-13	IN	CACHINHB— becomes active when certain level 2 interrupts are set. It inhibits any writes to memory and workspace cache until the next time the instruction register is loaded.
INSTEX—	P4-15	OUT	INSTEX— is active during instruction stream read cycles.
ENDINSTR—	P4-17	OUT	Indicates that the previous instruction is finished and a new instruction is starting.

Note:

* I/O refers to the AU board.

Table 1-1. AU board to SMI Board Interface Pin Assignments and Functions (Continued)

Signature	Pin	I/O*	Description
INHIBIT—	P4-19	OUT	INHIBIT— is active during the demand fill microcycles and overlap microcycles, to inhibit the clock.
WRTDEN—	P4-21	IN	WRTDEN— enables the TILINE data drivers on the AU board.
MPERINH—	P4-22	OUT	Inhibits the map errors generated by prefetching instructions across map boundaries.
CLKDLY—	P4-23	OUT	CLKDLY— delays the clock during memory cycles where data is being transferred back onto the A bus. This allows extra setup time for data being read into the workspace cache or register file.
RESET—	P4-24	OUT	Signal generated during the execution of the RSET instruction.
STACKOV—	P4-25	OUT	Stack overflow/underflow condition reported as system error interrupt (level 2).
LOADIR—	P4-27	OUT	LOADIR— is active when the instruction register is being loaded.
LOADWS—	P4-28	OUT	LOADWS— is active during writes to the workspace cache.
WRTRCMEM—	P4-29	OUT	WRTRCMEM— forces a write into the error trace memory. It is used by microdiagnostics.
HOLDACC—	P4-30	OUT	A normally high signal that forces the TILINE signal THOLD— to go low, thus preventing interference from another processor until the first processor releases TLHOLD—.
WSPACC—	P4-33	OUT	WSPACC— is active when a workspace is read from or written into.
LDIST—	P4-35	OUT	LDIST— is used during LDS or LDD target instructions to force the use of map file 2.
NPRES	P4-37	OUT	NPRES becomes active when a demand fill is being forced.

Note:

* I/O refers to the AU Board.

Table 1-1. AU board to SMI Board Interface Pin Assignments and Functions (Continued)

Signature	Pin	I/O*	Description
LONG482	P4-39	OUT	LONG482 forces a slower clock to allow data to propagate in the SN74S482 devices on the AU board.
CRU—	P4-40	OUT	CRU— is active during CRU cycles to force a 250 ns clock.
FAST—	P4-41	OUT	FAST— forces a fast clock on the current cycle.
UPC(0)—	P4-42	OUT	UPC(0)— is active during microcycles from WCS. UPC(0)— forces a slower clock.
ABMAP—	P4-43	OUT	ABMAP— forces a slower clock to allow for ALU add time whenever data is being mapped from the A bus.
STCEN—	P4-45	OUT	STCEN— generates STORECLK, a CRU backplane clock used during CRU write cycles.
INTCRU—	P4-47	IN	When low, indicates to processor that CRU address is in the main chassis and that CRU input data can be processed at a faster rate.
DIAGCRU—	P4-48	IN	Serial data from the diagnostic registers on the SMI board to the AU board.
CRUOUT—	P4-50	OUT	CRU data out. Serial data appears on the CRUOUT— line when an LDCR, SBZ, or SBO instruction is executed. The data is sampled by external I/O interface logic at the CRU interface.

Note:

* I/O refers to the AU board.

1.3 AU BOARD FUNCTIONAL DESCRIPTION

This paragraph provides a functional description of the AU board, shown in Figure 1-1. The description is keyed to Figure 1-2, a functional block diagram of the AU board, and to Figure 3-1, the logic diagram for the AU board.

1.3.1 Arithmetic Logic Unit (ALU)

The ALU function of the 990/12 LR is implemented on the AU board with four SN74S481 4-bit, binary micro/macroprogrammable processor elements connected in cascade. The ALU performs arithmetic and logic operations on a 16-bit word. As shown in Figure 1-2, data input to the ALU is from the A bus at the AI data input port or from the B bus at the BI/O data I/O port. Data out from the ALU is from the data out port that is connected to the A bus or from the BI/O data I/O port to the B bus. In the following description, refer to the functional block diagram of the ALU (Figure 1-3).

Data on the A bus during phase 1 of the clock is stored in the A latch during phase 2 of the clock and can also be placed in the workspace register, also called the accumulator (AC). Data on the B bus during phase 1 of the clock cycle is stored in the B latch during phase 2 of the clock cycle. The result of the operations on the data in the A latch and the B latch is placed either directly on the sum bus (internal to the processor) or shifted to the left or right. The data on the sum bus can be output on the B bus or on the data out port, which is an input to the A bus. Internally, data on the sum bus can be placed in the memory counter (MC), program counter (PC), the (AC), or the extended accumulator (XAC). On each clock cycle, the MC and PC can hold, or increment by one or two counts. The content of either the MC or PC can be an output of the address out port and, if selected by an address multiplexer, is applied to the address bus. Also, the contents of the PC may be an operand of the ALU operation. The AC can be used to store the result from the sum bus, or can be used for shift operations. The XAC receives data shifted from the AC in double-precision shift operations or receives data from the sum bus. The XAC is used to hold the most significant word of double-precision operations and is used in double-precision shift operations. The data in the AC and in the XAC can be placed on the data out port, which is the input of the A bus.

The operations performed by the ALU include addition, subtraction, multiplication, division, and bit-by-bit logic operations between two operands. A cyclic redundancy character (CRC) can also be generated, as well as arithmetic and logical shifts to the left, to the right, and circular. An operation code from the microcode word, applied to the operation select inputs, specifies the operation to be performed. This code also specifies the internal source of each operand, and the internal destination of the result. The states of the control lines, derived from the fields of the microcode word, select the following:

- The destination of input from the A bus (to the A latch only or to the A latch and the AC)
- The B bus as an input to the B latch, or as an output from the sum bus
- The data on the data out port (from the sum bus, the AC, or the XAC)
- The data on the address out port from the PC or MC
- The operation of the PC (hold or increment)
- The operation of the MC (hold or increment)
- The value of the increment (either one or two counts)

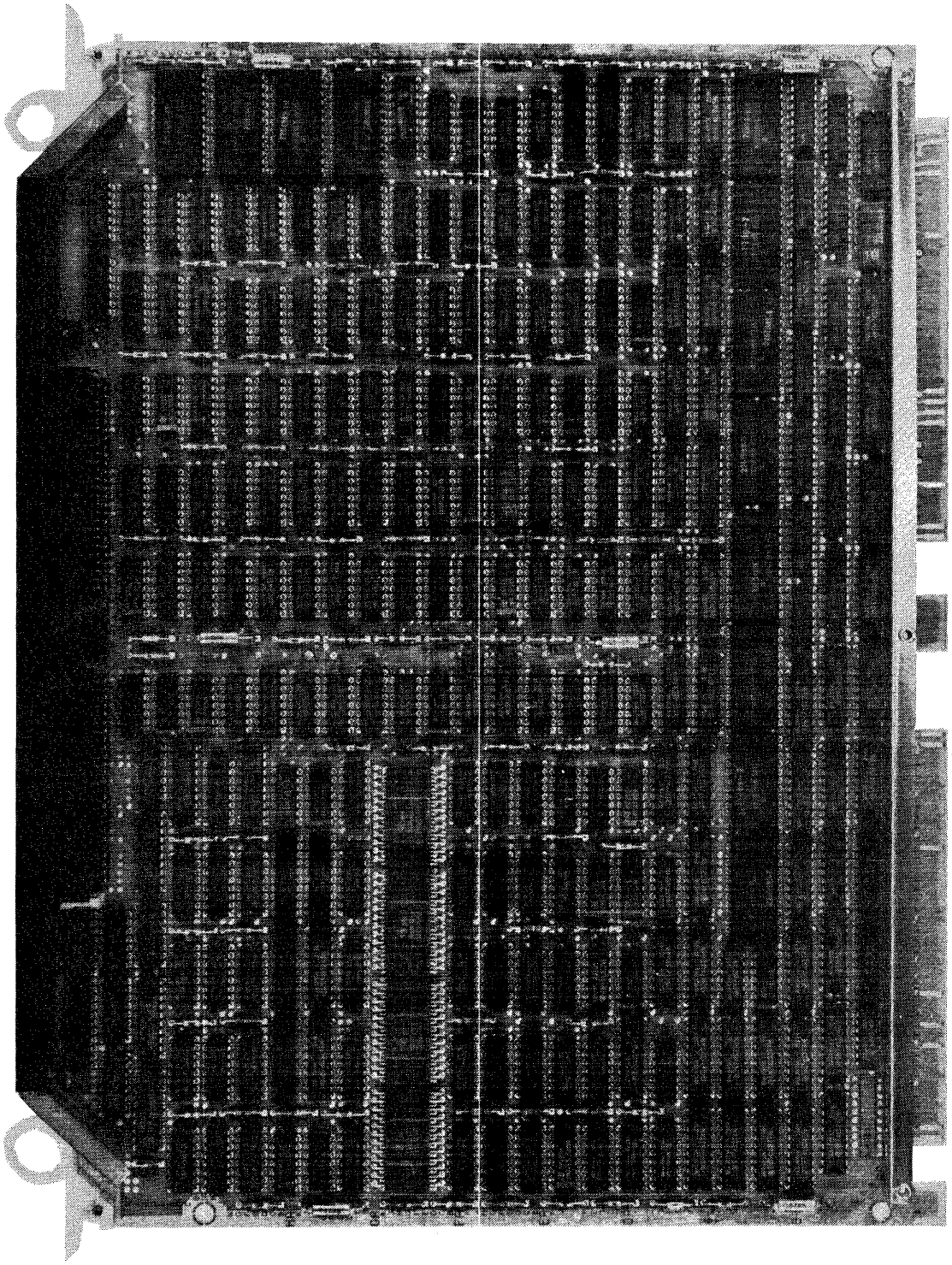

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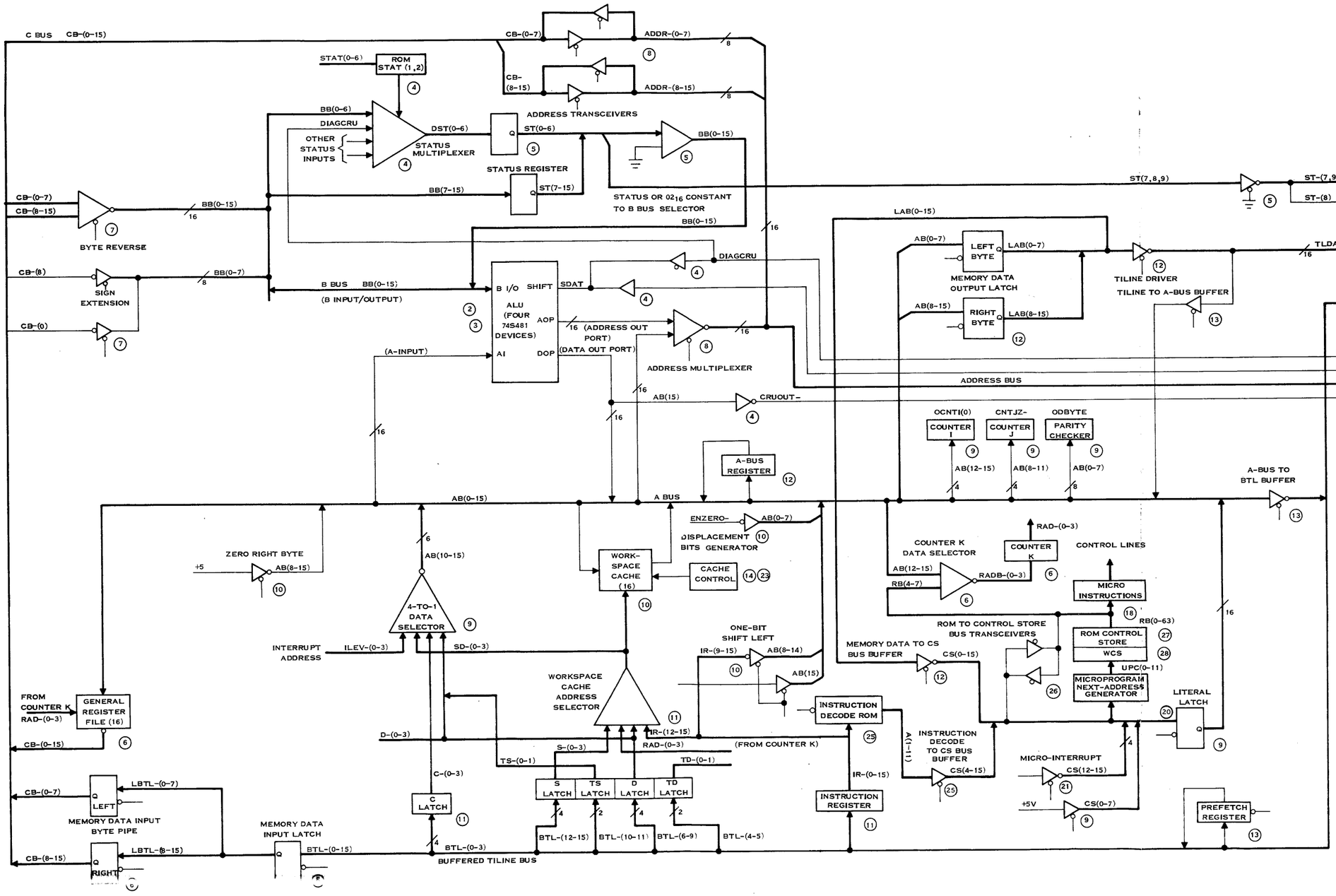
Figure 1-1. The Arithmetic Unit (AU) Board



NOTE: NUMERALS IN CIRCLES INDICATE PAGE NUMBERS OF AU BOARD LOGIC DIAGRAMS.

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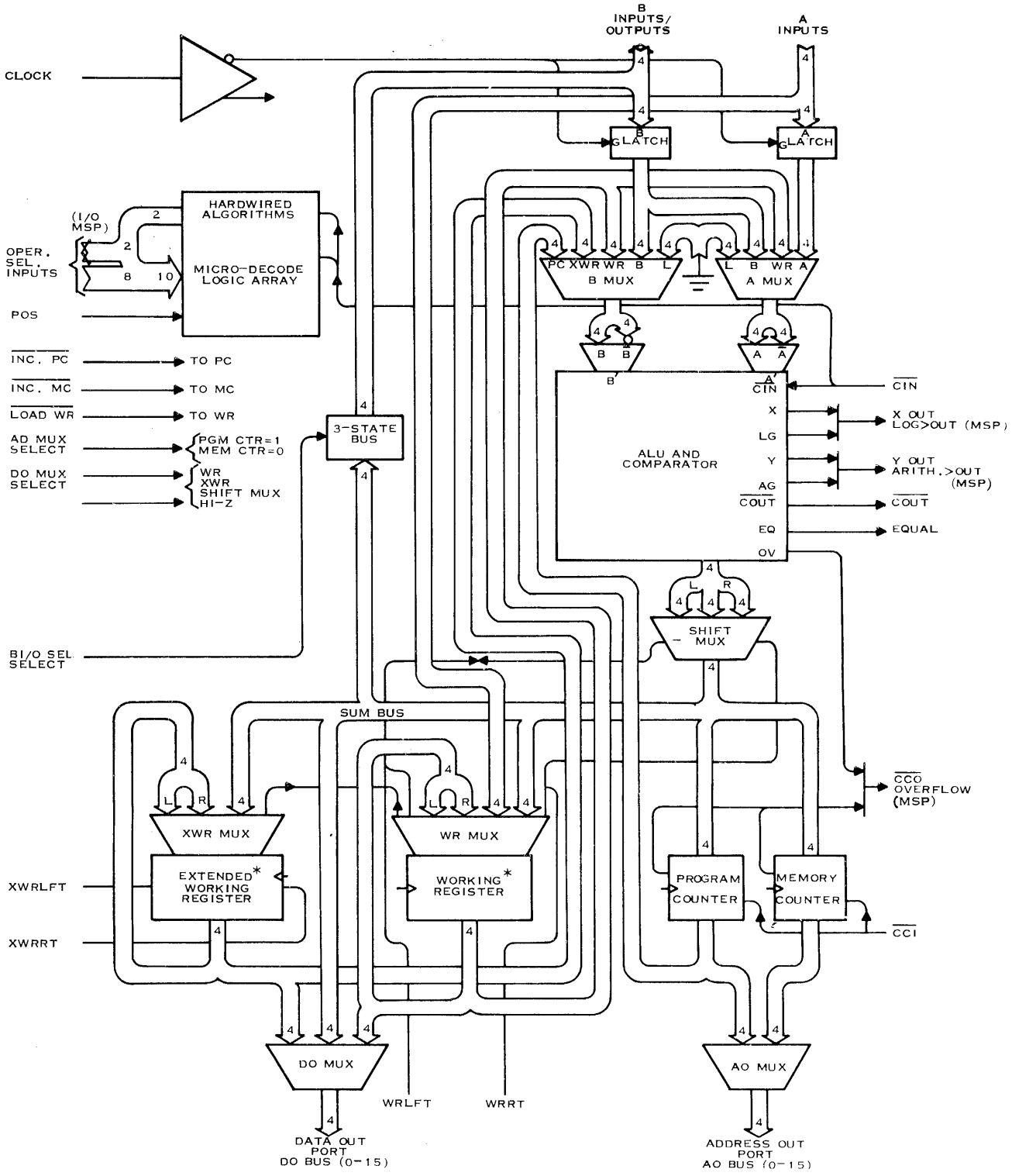
Figure 1-2. Functional Block Diagram of the AU Board



*THE WORKING REGISTER (WR) AND THE EXTENDED WORKING REGISTER (XWR) ARE ALSO REFERRED TO AS THE ACCUMULATOR (AC) AND THE EXTENDED ACCUMULATOR (XAC), RESPECTIVELY.

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Figure 1-3. Functional Diagram of the SN74S481

Table 1-2 provides the pin numbers and the pin functions of the processor element.

Table 1-2. Processor Element SN74S481 Pin Functions

Pin Number	Pin Name	Pin Function	Input, Output or Input/Output
46 47 1 2	BI/O0 BI/O1 BI/O2 BI/O3	4-bit parallel data input port to the B latch, or 4-bit parallel data output for the sum bus when not being used as an input.	I/O
6 5 4 3	AI0 AI1 AI2 AI3	4-bit parallel data input port to the A latch and workspace register (WR).	Inputs
7 8 9 10 17 14 13 11 15 16	OP0 OP1 OP2 OP3 OP4 OP5 OP6 OP7 OP8 OP9	OP0 through OP9 serve as a 10-bit parallel operation-select input to the microdecode logic array. In the most significant position, OP8 and OP9 serve as open-collector outputs during multiply and divide algorithms. In the least significant position, OP9 serves as the open-collector output during the CRC algorithm.	Inputs
12	Vcc	Single five-volt power supply terminal.	Supply Voltage Pin
18	CIN—	Receives low (active) ripple carry input data.	Input
19	POS	Directs internal and I/O end-conditions required to define the relative position of each bit-slice when N-SN74S481s are cascaded to implement Nx4-bit word lengths. When biased at 2.4 volts, the package operates as the least significant slice. When grounded, it functions as an intermediate slice. When high (5 volts), it functions as the most significant slice.	Input
20	Y/AG	In least significant and intermediate positions, outputs arithmetic carry generate (Y), for use with look-ahead. In the most significant position, outputs are true arithmetically-greater-than signals.	Output
21	X/LG	In least significant and intermediate positions, outputs arithmetic carry propagate (X), for use with look-ahead. In most significant positions outputs are true, logically-greater-than signals.	Output

Table 1-2. Processor Element SN74S481 Pin Functions (Continued)

Pin Number	Pin Name	Pin Function	Input, Output or Input/Output
22	COUT—	Outputs are low (active) ripple carry data.	Output
23	EQ	Outputs true (active-high) equality of sum bus equals zero for each 4-bit slice. The open-collector output permits wired-AND to achieve Nx4-bit equality outputs.	Open-Collector-Output
24	LDWR—	When low, data applied at the AI port, coincident with the ↑ clock transition, is loaded into the WR.	Input
26 25	WRRT WRLFT	Working register and sum bus shift interconnectivity pins. WRRT receives left-shift, and outputs right-shift (true) data. WRLFT receives right-shift and outputs left-shift (true) data. Shift can be single-precision, double-precision, signed, or unsigned.	Bidirectional I/O
28 27	XWRRT XWRLFT	Extended working register shift interconnectivity pins. XWRRT receives left-shift, and outputs right-shift data. XWRLFT receives right-shift and outputs left-shift data. Shift can be single-precision, double-precision, signed, or unsigned.	Bidirectional I/O
29 30	D0 D1	Selects one of three DOP sources (WR, XWR, or sum bus) or places the DOP outputs in a high-impedance state.	Inputs
34 33 32 31	DOP0 DOP1 DOP2 DOP3	4-bit parallel, data-out port. DOP0 is the least significant bit.	3-state outputs
35	INCMC—	When low, enables the MC to increment, as directed by CCI— on the next ↑ clock transition. When high, inhibits MC to the hold mode. As CCO— is common to MC and PC, the MC should be inhibited when PC is enabled.	Input
36	GND	Common or ground terminal for the supply voltage.	

Table 1-2. Processor Element SN74S481 Pin Functions (Continued)

Pin Number	Pin Name	Pin Function	Input, Output or Input/Output
37	CCO—/OV	In the least significant and intermediate positions, a low-level output indicates that either the PC or MC is at the maximum count. CCO— is common to both PC and MC, so the ambiguous carry can be avoided if one or both counters is/are disabled by the INCPC— and/or INCMC— inputs. In the most significant position, a high-level output (depending on the operation selected) indicates that the WR, XWR, or ALU will overflow (OV) on the next clock.	Output
38 39 40 41	AOP0 AOP1 AOP2 AOP3	4-bit parallel address out port.	Output
42	A0	Selects one of two AOP sources (PC or MC).	Input
43	INCPC—	When low, it enables the PC to increment as directed by CCI— on the next ↑ clock transition. When high, it inhibits the PC to the hold mode. As CCO— is common to PC and MC, the PC should be inhibited when the MC is enabled.	Input
44	CCI—	In the least significant position, a low input directs the enabled PC or enabled MC to increment by one on the next ↑ clock transition. In the least significant position a high directs the enabled PC or enabled MC to increment by two. In other positions, a low is a carry input and a high inhibits the counter.	Input
45	CK	When high, enables the transparency of A and B input latches. When low, it latches A and B input data. It clocks synchronous registers and counters on the positive transition.	Input
48	BI/O SEL	When low, it enables BI/O to output sum bus data. When high, the BI/O output drivers are placed in a high-impedance state, permitting BI/O to be used as data inputs.	Input

A clock cycle is supplied to the ALU at a maximum frequency of 4.5 megahertz. Clocking of the ALU circuits occurs on the rising edge (negative to positive transition) of the clock. The A bus and B bus both supply input signals to the ALU and must be clocked at the same frequency. The C bus also must be clocked at the same frequency since the C bus can be gated into the B bus. Two phases are defined for these clocks. During phase 1, the ALU inputs, to be used in the operation that occurs at the rise of the ALU clock, are placed on the A bus or B bus. During phase 2, the result of the operation is available to be placed on the A bus or B bus.

1.3.2 Microcode Instructions

The instructions of the 990/12 LR are implemented as sets of microcode instructions accessed from either a ROM control store or a writable control store (WCS). Figure 1-4 shows that each word of microcode contains 64 bits organized into 15 fields. Microcode instructions are written symbolically using the microcode assembly language. A microcode assembler translates the source statements of the assembly language into binary object code that can be loaded into the WCS. It is important to note that the bit order of the microcode instruction generated by the microcode assembler is not the same as the bit order of the microcode instruction stored in the ROM control store or WCS. Figure 1-4 shows these bit order differences. A utility program reformats the object code for loading into the WCS. Each field controls a portion of the computer logic. For example, an 11-bit field controls the microprocessor, a single bit controls the byte mode, and a 17-bit field determines the location of the next microcode instruction to be executed. The WCS microcode instructions are in the same format as those of the ROM control store and are stored in the WCS using a load control store (LCS) instruction. In order to execute instructions contained in the WCS, the computer accesses an XOP instruction with the WCS enable bit of the ST set to logic one. The first 32 locations in the WCS are dedicated entry points for 16 sets of microcode instructions. The C field of the XOP instruction specifies 1 of 16 hardware XOPs, each implemented by microcode in the WCS. The content of the C field passes control to the appropriate location in the dedicated area of the WCS. Typically, control passes to the following microcode instruction that branches to the remainder of the microcode routine after execution.

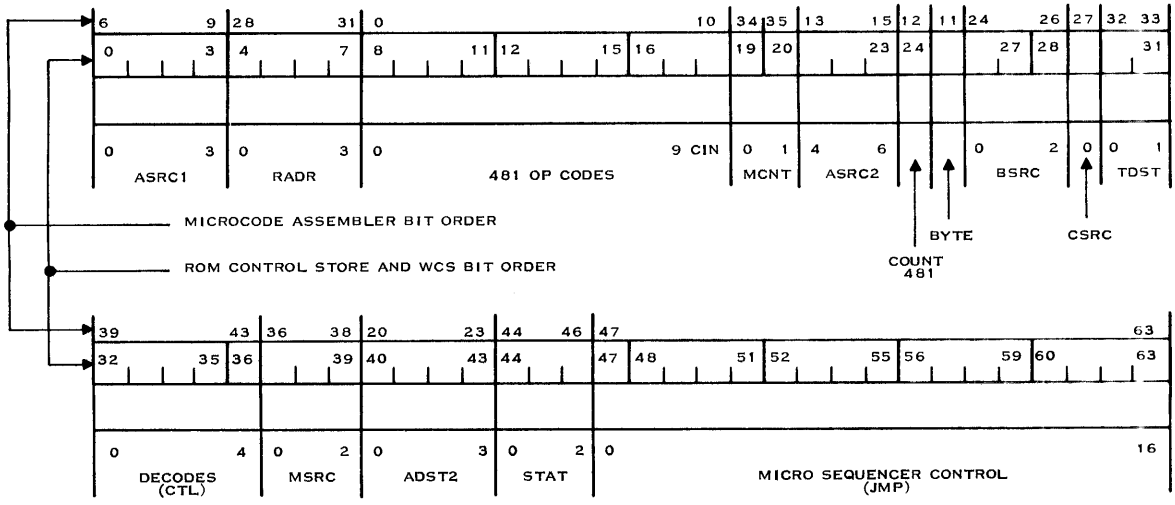

Figure 1-4. Fields of the ROM Control Store or WCS Microcode Word

1.3.3 A Bus

As shown in Figure 1-2, the A bus is a 16-bit data bus with signal signatures AB (0 through 15). The A bus interconnects the following:

- The ALU (AI data in port and data out port)
- An address multiplexer
- The A bus register
- Counter I
- Counter J
- Counter K data selector and counter K
- A four-to-one data selector
- The A bus buffer
- The A bus to BTL buffer
- The memory data output latch
- The general register file
- Displacement bits generator
- A one-bit shift-left generator
- A zero right byte generator
- The parity generator
- A literal latch
- The workspace cache

Three fields of the microcode word control the A bus, allowing the microcode to select the A bus source during phase 1, and the A bus source and destination during phase 2. Figure 1-4 identifies these fields as ASRC1, ASRC2, and ADST2, respectively. Field ASRC1 is a 4-bit field that selects 1 of 16 sources that can be connected as the source for the A bus during phase 1. The A bus destination during phase 1 is the A latch in the ALU, the memory interface circuits, or both. Field ASRC2 is a 3-bit field that selects 1 of 8 sources for the A bus during phase 2. One of these sources is the source selected during phase 1 to provide a total of 17 A bus sources (when redundancy is considered) during phase 2. Field ADST2 is a 4-bit field that selects 1 of 16 destinations for the A bus during phase 2. Refer to the logic diagram for the AU board, found in section 3 of this manual, and to Figure 1-2 for the following detailed description of the operation of the A bus.

1.3.3.1 Address Multiplexer. The address multiplexer selects from its inputs either the address out port from the ALU (program counter or memory counter content) or the A bus for output to the address bus. When neither the address out port nor the A bus is selected for output to the A bus, the C bus is the source for the address bus, or the address bus is the source for the C bus through address transceivers as shown in Figure 1-2.

1.3.3.2 A Bus Register. The A bus register serves as a destination for the A bus when the clock signal CLAREG applied to the register is active and output control signal ENAREG— is high. CLAREG is a function of clock signal CLK2— and the ADST2 field of the microcode word (refer to Figure 1-4). CLAREG clocks the present value of the A bus into the D inputs of the register and the Q outputs of the register are held at high impedance. When ENAREG— is brought low, the A bus register serves as a source to the A bus. ENAREG— is a function of clock signal CL8A and the ASRC1 field of the microcode word.

1.3.3.3 Counters I and J. Counters I and J are each 4-bit down-counters that are loaded from bits 12 through 15 and bits 8 through 11 of the A bus, respectively. When used separately, each counter can be loaded to provide decrementing counts 15 through 0. When the counters are used together, the counters can be loaded to provide decrementing counts 255 through 0. The counters are used by the processor in the control of conditional jumps. Loading of counters I and J occurs when signals LDCNTI— and LDCNTJ—, respectively, are low. Both signals are a function of the ADST2 field of the microcode word. Both of the signals that enable the counters for counting are a function of the DECODES field of the microcode word.

1.3.3.4 Counter K Data Selector and Counter K. Bits 12 through 15 of the A bus constitute one input to the quadruple 2-line to 1-line data selector; the register address field of the microcode word (ROM bits 4 through 7) is the other input to the data selector. When the select signal LDCNTK— that is applied to the selector is low, the A bus input is selected for output from the data selector; when LDCNTK— is high, the input from the ROM bit is selected for output. In either case, the output of the data selector (RADB— bits 0 through 3) is applied as the load input to counter K.

The select signal, LDCNTK—, is an output of an A destination decode programmable read-only memory (PROM). The state of LDCNTK— (high or low) is determined as the PROM is addressed by A destination address lines ADST (0 through 3), and signal A1A0N. Lines ADST (0 through 3) are developed at the output of a flip-flop as a function of ROM bits 40 through 43, and signal A1A0N is a function of ROM bits 0 and 1.

Counter K counts either up or down under control of signal K(3), a function of ROM bit 7. When the load signal LDRAD— goes low, counter K is loaded to count from that value contained at the output of the counter K data input selector on lines RADB— (0 through 3). The low LDCNTK— signal, which selects the A bus input to the counter K data input selector for output, causes LDRAD— to go low: the result is that whenever LDCNTK— is low; the value contained in bits 12 through 15 of the A bus is loaded into counter K.

When LDCNTK— is high, the ROM-bit input to the counter K data input selector is selected for output. The high LDCNTK— no longer causes LDRAD— to go low to load the counter. A low ENLD— developed from ANDed high signals CNTK— and CMODE— now causes the counter to load.

The high CNTK— at the output of a ROM is a function of control code decoding of ROM bits 32 through 36. The high CMODE— at the Q output of a flip-flop is generated when both LDCNTK— and CNTK— are high.

Counter K counts when enabling signals ENK— and KENT— are both low. ENK— is low when signal K(2) (a function of ROM bit 6) is high and CMODE is toggled high. KENT— is low if either BYTE or K(3)TAG is low. BYTE is a function of ROM bit 25. K(3)TAG is low if signal K(3) and TAG— are the same; both high or both low. K(3) is a function of ROM bit 7. TAG— is the inverted function of either the MDI tag or the register file tag as selected by the C-source ROM bit 29 and CSRC(0), which is a function of ROM bit 29.

The counter K output, RAD— (0 through 3), is used to address the general register file and is one of four inputs to the workspace cache address selector. When the A source signals ASRC(2) and ASRC(3) are both low, the counter K input to the workspace cache address selector is selected for output as signals SD— (0 through 3). SD— (0 through 3) addresses the workspace cache and also addresses the dirty control RAM. The dirty control RAM performs as the 17th bit of the workspace cache.

1.3.3.5 A Bus Four-to-One Data Selector. The four-to-one data selector serves as a source for bits 10 through 15 of the A bus for one of four input signals to the data selector. The enabling signal and the select signals applied to the data selector are a function of the ASRC1 field of the microcode word. The input signals to the data selector that can be selected for output to the A bus are as follows:

- The workspace cache address signals SD— (0 through 3)
- The interrupt-code input lines ILEV— (0 through 3) from the SMI board
- The C-latch output signals C— (0 through 3) and K(4) (a function of the ASRC1 field of the microcode word and a register file and memory data input latch TAG signal)
- The TS latch signals TS— (0 and 1) along with two D-latch signals D— (2 and 3)

The enabling signal for the data selector is applied to the displacement bits generator and to two AND gates to cause bits 0 through 9 of the A bus to go low when the four-to-one data selector is enabled.

1.3.3.6 A Bus Buffer. The A bus buffer is a phase 2 A bus source to enable TILINE* data to the A bus when enabling signal ENTAB— is low. The low ENTAB— signal is a function of the ASRC2 field of the microcode word. The low ENTAB— signal can also be generated as a function of a high STEP2WSR signal. A high STEP2WSR is generated to indicate the second step of the demand and fill sequence.

1.3.3.7 A Bus to BTL Buffer. The A bus to BTL buffer enables A bus data to the buffered TILINE bus when the enabling signal ENTABL— is low. ENTABL—, a function of the MCNT field of the microcode word, is inhibited during the time when the output of the prefetch register is applied to the buffered TILINE bus.

* TILINE is a trademark of Texas Instruments Incorporated.

1.3.3.8 Memory Data Output Latch. The memory data output latch can be enabled for left byte, right byte, or full word transfer of input A bus data to the output of the latch. The latch output is applied to the TILINE driver and memory data to the CS bus buffer. When enabling signal LDMD0— is low, the A bus data is clocked through the selected part of the latch and applied to inputs of the TILINE driver and the memory data to the CS bus buffer. The select signals TAB, BYTE, and MA15 permit either the right half, left half, or both half-sections of the latch to be selected for byte or full-word data transfer.

TAB is a function of the ASRC2 field of the microcode word, BYTE is a function of the BYTE field of the microcode word, and MA15 is a function of the MSRC field of the microcode word and bit 15 of the address bus. Enabling signal LDMD0— is a function of the ADST2 field of the microcode word.

1.3.3.9 General Register File. The general register file consists of sixteen, 16-bit registers that are addressed by the output of counter K. When enabled for a write operation, the general register file serves as a destination for the A bus. The general register file is a source for the C bus. The file can be written into or read from in either 16-bit word or right or left byte operations. The operation of the general register file in read operations is discussed in the description of the C bus, paragraph 1.3.5. The general register file is selected for either a read or write operation when signal ENREG— is low. The right half and the left half of the registers are enabled for a write operation when signals CLRFR and CLRFL, respectively, are clocked low. ENREG—, CLRFR, and CLRFL are all products of the ADST2 and BYTE fields of the microcode word at the output of an A destination decode ROM. The signals are clocked into the register file by clock signal CLK3—.

1.3.3.10 Displacement Bits Generator. As previously described, at the time the A bus four-to-one data selector is enabled for output of bits 10 through 15 on to the A bus, the same enabling signal (ENCSD—) applied to the displacement bits generator, and to two AND gates, causes bits 0 through 9 of the A bus to go low. The displacement bits generator also is enabled when the one-bit shift-left generator is active. The one-bit shift-left generator shifts instruction register bits 9 through 15 one bit to the left and places them on the A bus as bits 8 through 14 and at the same time, sets bit 15 of the A bus low. The enabled displacement bits generator sets A bus bits 0 through 7 high or low in coincidence with the high or low state of instruction register bit 8.

1.3.3.11 A Bus Zero Right Byte Generator. A ZERORB— signal generated as a function of the DECODES field of the microcode word enables the zero right byte generator to set bits 8 through 15 of the A bus to zero. The ZERORB— signal is also applied to the status or >02 constant to B bus selector to zero the right byte of the B bus.

NOTE

The right angle bracket symbol (>) denotes hexadecimal.

1.3.3.12 Parity Generator. The parity generator checks the parity of the A bus bits 0 through 7 to generate a high ODBYTE signal when an odd number of the bits are high. ODBYTE is applied to a four-line to one-line status multiplexer and when selected for output, is clocked through the status register as the status register parity bit, bit 5.

1.3.3.13 Literal Latch. The output control of the literal latch is enabled for transfer of CS bus data to the A bus during phase 1 of the clock as a function of the ASRC1 field of the microcode word. The latch is enabled for output during phase 2 of the clock as a function of the ASRC2 field of the microcode word.

1.3.3.14 Workspace Cache. The workspace cache consists of four 64-bit random-access read/write bipolar memory devices, each organized as 16 words of 4 bits to provide storage for one 16-bit word for each of 16 registers. Data accessed as workspace registers is stored as it is fetched from memory. Subsequent accesses to the same data are taken from the workspace cache. When the workspace pointer is changed, all workspace registers that were written into are copied into TILINE memory. When the processor performs a memory write to physical memory locations that correspond to current workspace, both memory and workspace are updated.

Registers of the workspace cache can be addressed as a phase 1 source, a phase 2 source, and a phase 2 destination of the A bus. When the workspace cache is enabled during phase 1 of the clock, the workspace register addressed by signals SD— (0 through 3) at the output of the workspace cache address selector serves as the source for the A bus. This output signal is selected from one of four inputs to the workspace cache address selector. The result is that the A bus source during phase 1 of the clock is the workspace register addressed by either counter K, by instruction register bits 12 through 15, by the D latch, or by the S latch. With the workspace cache enabled during phase 2 of the clock, the register addressed during phase 1 can remain as the A bus source, or the register addressed by counter K or by the D latch can be substituted for the phase 1 A bus source. During phase 2 of the clock, the workspace register addressed as the A bus source in phase 1 serves as the A bus destination in either the word mode, or left- or right-byte mode.

1.3.4 B Bus

As shown in Figure 1-2, the B bus like the A bus, is a 16-bit data bus. Signal signatures for the bus are BB (0 through 15). The B bus interconnects the following:

- The ALU (BI/O I/O port)
- The status multiplexer
- The status register or >02 constant to B bus selector
- The C bus

The BSRC field of the microcode word selects one of eight sources for the B bus. Two of the eight sources are different during phase 1 and phase 2. The microcode word bit configuration that selects either the status register or the >02 constant as the phase 1 source for the B bus, selects the ALU sum bus as the source during phase 2. The destination for the B bus during phase 1 is the B latch of the ALU. During phase 2, the destination of the B bus is the status multiplexer and/or the ST controlled by the status field (ROM bits 44 through 46) and the extended status field (ROM bits 60 through 63). The interface to the C bus is highly flexible in that the C bus can be copied to the B bus in its present form, with bytes reversed, left byte only with sign extended, right byte only with sign extended, left byte copied to right byte, or right byte copied to left byte.

1.3.4.1 Status Multiplexer. The status multiplexer consists of two dual four-line to one-line selectors and three eight-line to one-line selectors and serves as a destination for B bus bits 0 through 6. The B bus bits are among numerous other inputs to the status multiplexer. The selected inputs to the status multiplexer become signals DST0 through DST6 at the output of the status multiplexer. DST0 through DST6 are applied as inputs to the status register. The select signals applied to the status multiplexer are a function of the STAT field of the microcode word and of the four least significant bits of the JMP field of the microcode word. The four least significant bits of the JMP field are interpreted as the extended status field when a conditional jump on true condition is specified. The STAT field and extended status field signals address STAT1 and STAT2 ROMs to generate the status multiplexer select signals.

1.3.4.2 Status Register. The status register consists of an octal D-type flip-flop with a common clock, a hexadecimal D-type flip-flop with a common clock and a common enable, and a quad D-type flip-flop with rail outputs with a common clock and common enable. The octal flip-flop input signals DST0 through DST6, are selected from various inputs to the status multiplexer, as described in the previous paragraph, are clocked through the register as status bits 0 through 6. Input signals to the hexadecimal D-type flip-flop consist of bits 7 through 11 of the B bus. When the enabling signal, LD8, is low, the input bits are clocked through the flip-flop as status bits 7 through 11. LD8 is generated at the output of STAT2 ROM as a function of the STAT field and the extended status field of the microcode word. Input signals to the quad D-type flip-flop consist of B bus signals 12 through 15; and when the enabling signal LD12 is low, the input bits are clocked through the flip-flop as status bits 12 through 15. The complements to status bits 12 through 15 (ST12— through ST15—) are also supplied at the output of the flip-flop. LD12, like LD8, is generated at the output of STAT2 ROM as a function of the STAT and extended status fields of the microcode word.

The status bits (ST0 through ST15) are applied as an input to the status or >02 constant to B bus selector. Additionally, status bits 0 through 5 are applied to an instruction decode ROM, status bits 4 through 10 are ANDed to provide an arithmetic overflow signal to the SMI board, status bits 7 through 9 are buffered for application to the AU board to SMI board interface, status bits 7 through 11 are applied to logic that sets conditions for controlling the microprogram next-address generator, status bit 8 is applied to a control code decoding ROM that generates map control signals for the SMI board, and signals ST12— through ST15— are applied to a 4-bit magnitude comparator on the AU board to set the interrupt mask.

1.3.4.3 Status or >02 Constant to B Bus Selector. The status or >02 constant to B bus selector consists of four quadruple two-line to one-line data selectors. The select and output control enable signals applied to the data selectors are a function of the BSRC field of the microcode word. With the output control signal enabled and with the A inputs to the data selectors selected for output (select signal BSRC2 is low), the status register bits are the phase 1 source to the B bus. When the select signal applied to the data selectors is high, the B inputs to the data selector are selected for output and one of these two conditions prevails;

- When the signal ZERORB— (which is an input to the next to the least significant bit (LSB) position of the B inputs) is high, the output to the B bus is a >02 logic level signal;
- When the signal ZERORB— is high, only the right byte section of the data selector output control is enabled, and the effect is to zero the right byte of the B bus.

The ZERORB— signal is a function of control code decoding of the DECODES field of the microcode word.

1.3.4.4 The B Bus to C Bus Interconnect. The B bus to C bus interconnect consists of byte reverse and sign extension logic. The byte reverse logic consists of four quadruple 2-line to 1-line data selectors. The sign extension logic consists of two octal three-state output line drivers. One of the octal drivers extends the sign of the most significant bit (MSB) of the right byte of the C bus to the left byte of the B bus. The other octal driver extends the sign of the MSB of the left byte of the C bus to the left byte of the B bus.

Opposite bytes of the C bus are connected to the A and B inputs of the byte reverse data selectors. With applied selection and output control signals, and the use of the sign extension logic, the C bus can be copied to the B bus:

- In its present form
- With bytes reversed
- Left byte only with sign extended
- Right byte only with sign extended
- Left byte copied to the right byte
- Right byte copied to the left byte

1.3.5 C Bus

The C bus is a 16-bit data bus with signatures CB— (0 through 15). The C bus interconnects the memory data input latch via the memory data input byte pipe, the general register file, the address bus, and the B bus. The CSRC field (bit 29 of the microcode word) in conjunction with the DECODES field of the microcode word, selects the C bus source. The selected C bus source can be either the memory data input latch, the general register file as addressed by counter K, or the address bus. The destination of the C bus is the B bus as selected by the BSRC field of the microcode word and/or the address bus when selected by the MSRC field of the microcode word.

When enabled for a write operation, the general register file is a destination of the A bus. When enabled for a read operation, this file is a source for the C bus. The general register file (as addressed by counter K) is enabled for a read operation by the CSRC field of the microcode word and a decode of the DECODES field of the microcode word.

Address transceivers are the bidirectional interface between the C bus and the address bus. A low derived from a decode of the DECODES field of the microcode word enables the transceivers in the direction of address bus to C bus. A high derived from the decode along with an enabling signal from the map source (MSRC) field of the microcode word enables the transceivers in the direction of the C bus to the address bus.

The C bus to B bus interface is effected by the sign extension and the byte reverse logic.

The memory data input latch holds buffered TILINE data stored under control of the TDST field of the microcode word. The stored data is available for transfer to the C bus either in byte or word length under control of the CSRC and DECODES field of the microcode word.

1.3.5.1 General Register File as a C Bus Source. The general register file is a destination of the A bus as well as a source for the C bus. The operation of the general register file as a destination for the A bus is described in paragraph 1.3.3.9.

The contents of the register file as addressed by the output of counter K is enabled for a read to the C bus when chip select signal ENREG— is low. For a read operation, the low ENREG— is a function of the CSRC field of the microcode word and the signal ENADCB— that is derived from a decode of the DECODES field of the microcode word.

1.3.5.2 Address Transceivers. The address transceivers consist of two octal bus transceivers with three-state outputs. The devices permit transmission from the C bus to the address bus or from the address bus to the C bus depending upon the logic level of the directional control signal, ENADCB—. When the enable input signal (ENA—) to the transceivers is high, the two buses are isolated effectively from each other. The operation of the address transceivers is described in paragraph 1.3.5.

1.3.5.3 Byte Reverse and Sign Extension Logic. The byte reverse and sign extension logic interconnects the B bus and the C bus. The operation of the byte reverse and sign extension logic is described in paragraph 1.3.4.4.

1.3.6 Address Bus

The address bus is a 16-bit bus with signal signatures ADDR— (0 through 15). The address bus interconnects the address out port of the ALU, the A bus, and the C bus on the AU board. Additionally, the address bus is brought to the pins of connector P3 at the top edge of the AU board where a ribbon cable completes the interface to the SMI board. On the SMI board, the address bus is applied through buffers to mapping logic, to the WP, to workspace cache control logic, and to the CRU address latch.

On the AU board, the address multiplexer selects either the address out port from the ALU or the A bus for output to the address bus. The address transceivers are the bidirectional interface between the C bus and the address bus.

1.3.7 Buffered TILINE Bus

The buffered TILINE bus is a 16-bit data bus with signatures BTL— (0 through 15). The buffered TILINE bus interconnects the TILINE data bus, the A bus, the instruction register, the CDS latch, the prefetch register, and the C bus (the latter via the memory data input latch and memory data input byte pipe).

The TDST field of the microcode word selects the destination of the buffered TILINE bus. Depending on the value of the TDST field, the buffered TILINE data bus is loaded into the instruction register and the CDS latch in one configuration, into the prefetch register and the memory data input latch in a second configuration, and into the memory data input latch (only) in a third configuration.

The memory control field of the microcode word, MCNT, and a decode of the DECODES field of the microcode word select the source for the buffered TILINE bus. The A bus to BTL buffer is the A bus to buffered TILINE bus interface, and the TILINE buffer is the TILINE data bus to buffered TILINE bus interface. A third source for the buffered TILINE bus is the stored data in the prefetch register. The enabling signal for the output control of the prefetch register also enables the clock for the CDS latch to cause the contents of the prefetch register to be loaded into the CDS latch.

1.4 SMI BOARD FUNCTIONAL DESCRIPTION

This paragraph provides a functional description of the SMI board, shown in Figure 1-5. The description is keyed to Figure 1-6, a functional block diagram of the SMI board, and to the logic diagram for the SMI board.

1.4.1 Loader and Self-Test ROM

The loader and self-test ROM on the SMI board is implemented with two Texas Instruments TMS 4732 devices that are 32,768-bit, read-only memories (ROMs). The two mask devices are each organized as 4K by 8-bits and provide 4K 16-bit words of loader and self-test ROM.

Figure 1-7 shows the functional block diagram of the loader and self-test ROM. A low PDATEN— signal enables data output from the ROM to the TILINE data bus. For the enabling signal PDATEN— to be developed, address bus signals ABUSB0 through ABUSB5 must be developed, and status register bit 8 must be cleared by software (ST8A— equals 1), and map file 0 must be implemented (MAPFLE0— equals 1). With PDATEN— low, the content of the ROM, addressed by address lines TLAD11 through TLAD19, is enabled on the TILINE data bus.

In the power-up sequence, the reset signal TLRESB— clears a CRU-addressable latch, signals EPROMADR0 through EPROMADR2 are reset, and one 512-word section of the EPROM is addressed. CRU output instructions that address CRU output bits 10, 11, and 12 at CRU base address >1FA0 (EPROMADR0 through EPROMADR2) are required to enable other 512-word sections of the EPROM. For more information, refer to the *Model 990/12 LR Computer, General Description*.

1.4.2 Breakpoint System

The 990/12 LR breakpoint system is implemented using a CRU-addressable 16-bit breakpoint register, the error interrupt status register, and the error trace memory. The breakpoint register address is CRU base address >1F80. A CRU output instruction loads the desired breakpoint word address into the breakpoint register. CRU output bits 1 through 15 of the breakpoint register (corresponding to register output signals BRKRG14 through BRKRG0, respectively) are used for the breakpoint word address and CRU output bit 0, BRKRG15, is used as a breakpoint enable signal (logic 1 equals breakpoint enabled). When the breakpoint system is enabled and a memory reference is made to the unmapped address that corresponds to the value placed in the breakpoint register, the error interrupt trap (level 2) is taken and the breakpoint flag is set in the error interrupt status register (bit 6, CRU base address >1FC0). When an error interrupt or breakpoint interrupt occurs, the error interrupt trace memory contains a trace of the 15 memory cycles that occurred prior to and including the fetch of the error interrupt trap vector. The trace memory does not stop immediately upon setting of the interrupt but stores one more workspace access or memory cycle to make the 16th word. The breakpoint address and breakpoint enable bits are cleared by hardware when:

- The breakpoint occurs
- A RSET is generated
- A power-up occurs

By disabling the breakpoint system and enabling the diagnostic interrupt logic, the breakpoint register is addressed in diagnostic testing of interrupt levels 3 through 15. This feature is discussed in the description of the interrupt logic (paragraph 1.4.4).

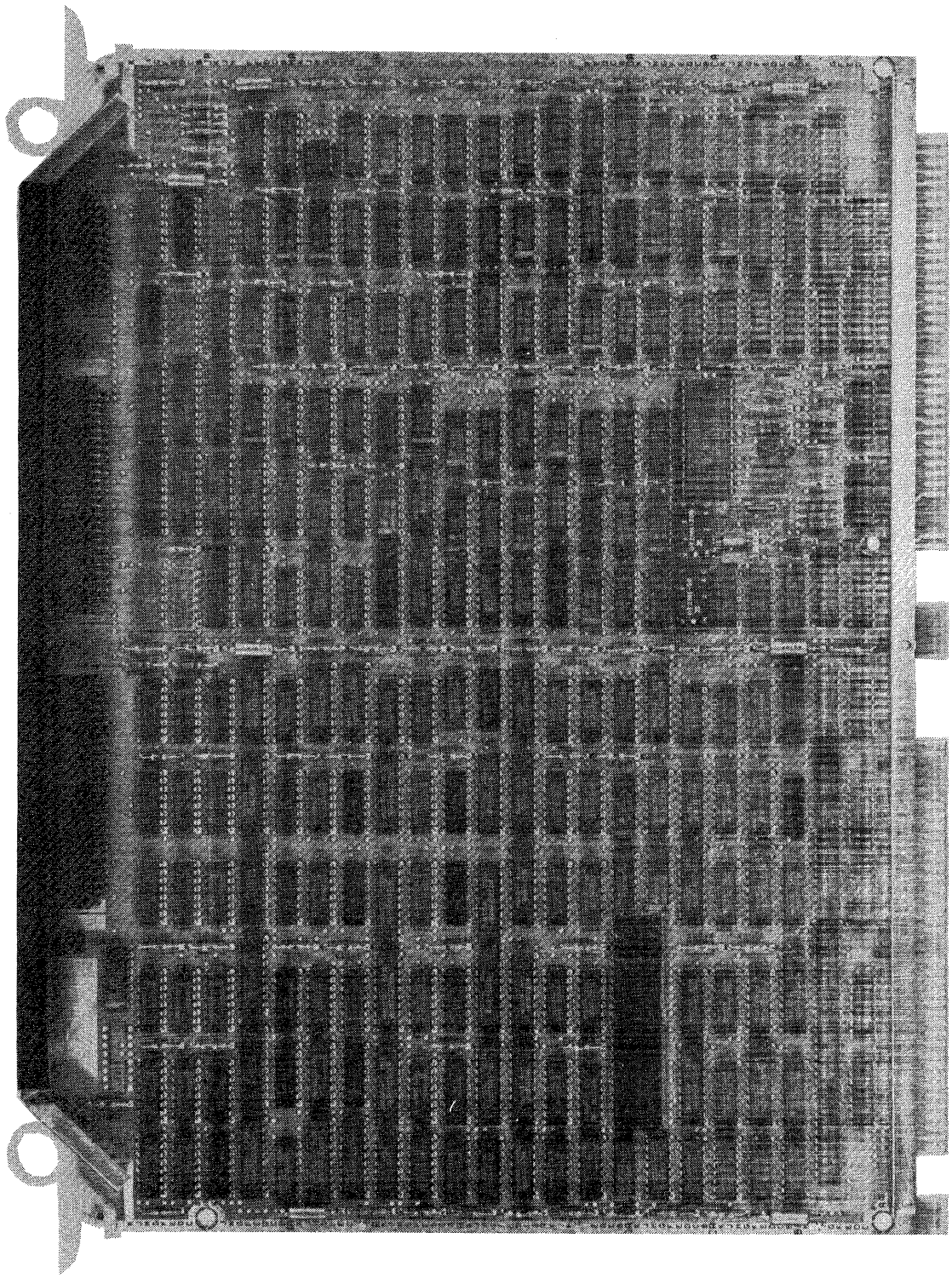

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Figure 1-5. System Mapping Interface (SMI) Board

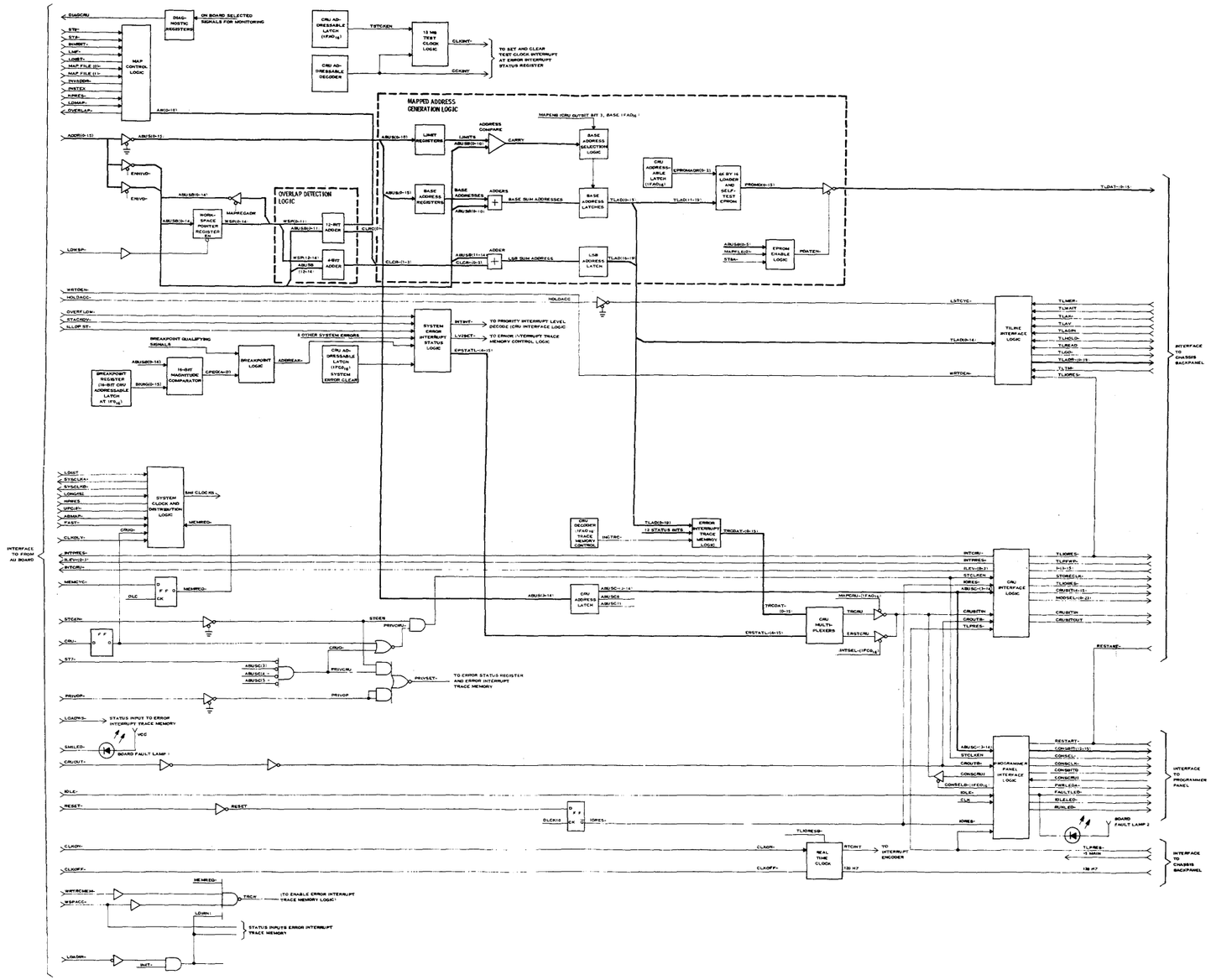

Figure 1-6. Functional Block Diagram of the SMI Board

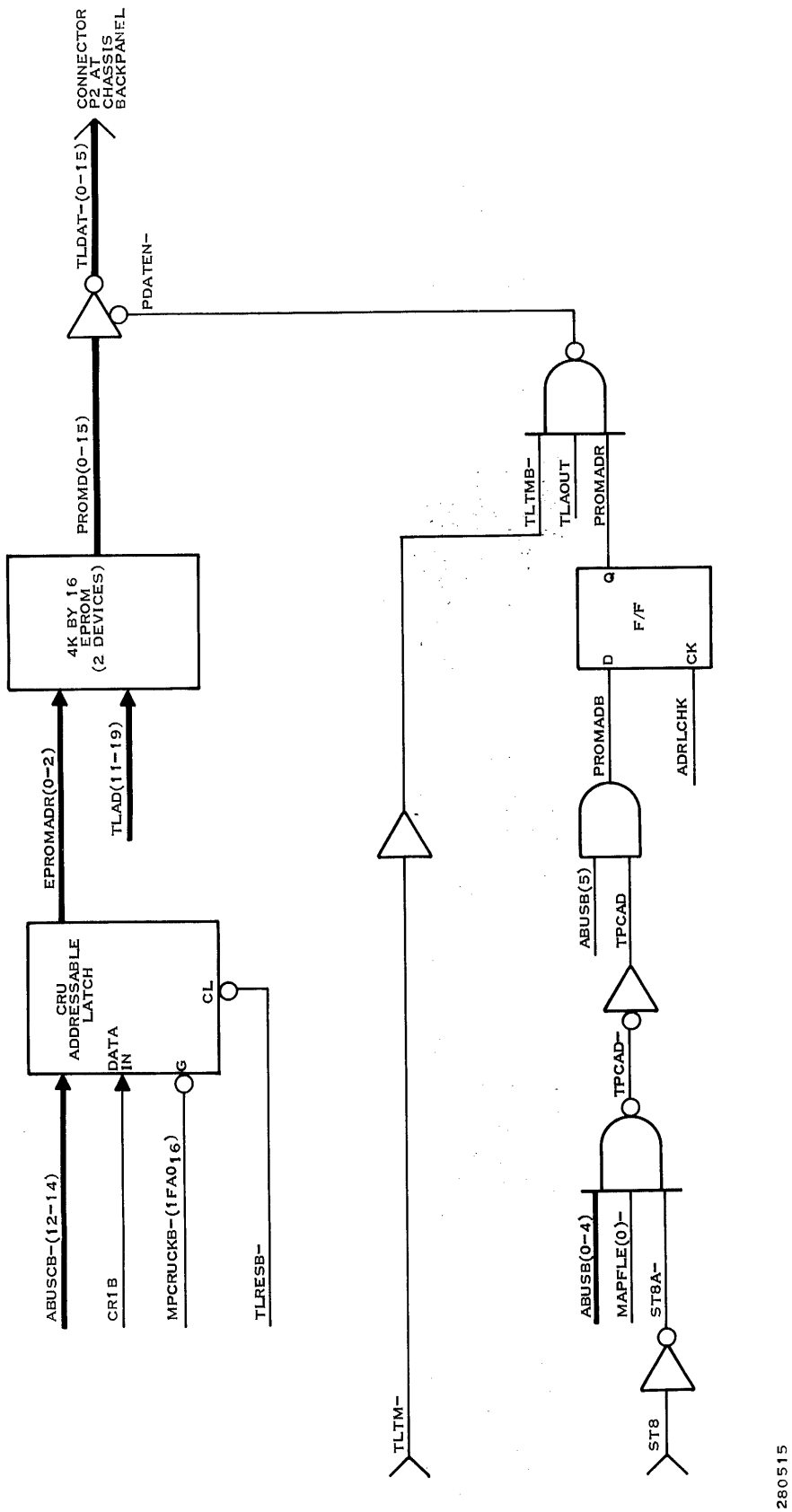

Figure 1-7. Simplified Functional Diagram of Loader and Self-Test ROM

The simplified functional diagram of the breakpoint system in Figure 1-8 should be used in the following description of the operation of the breakpoint system.

A CRU output instruction loads the breakpoint register (shown on the diagram as two 8-bit latches) with the desired breakpoint address and with the breakpoint enable signal. The output of the breakpoint register is applied as an input to a 16-bit magnitude comparator. With breakpoint enabled, when the unmapped address applied to the comparator as ABUSB (0 through 14) corresponds to the breakpoint address, the comparator output signals (CPEQA through CPEQD) go high. The signals are applied as inputs to a NAND gate along with breakpoint qualifying signals MAPREQ, PRVBKEN, and BKENA. If a long distance mapping instruction is being executed by the processor, LDMAP— goes high sending MAPREQ low, to disable the breakpoint system. The breakpoint can be enabled or disabled with the processor in the privileged mode by addressing CRU output bit 13 at CRU base address >1FA0 (refer to *990/12 LR Computer, General Description* for the CRU output bit assignments for error interrupt trace control and map control).

The enabling signal BKENA, further qualifies the breakpoint system. Output bit 3 at CRU base address >1FA0 is the memory map enable signal MAPENB. A low MAPENB enables the breakpoint system in the absence of memory mapping. When memory mapping is in use, output bit 5, at CRU base address >1FA0 (MAPF), enables the breakpoint system for either map 0 or map 1. When MAPF equals 0, map 0 is enabled; and when MAPF equals 1, map 1 is enabled.

When qualifying conditions as described are met, the low STBK— at the output of the NAND gate generates a high BKD signal that is clocked through a flip-flop as ADBK. As shown in Figure 1-8, the ADBK signal and the breakpoint select signals, BKSL6 and BKSL7, are applied to logic to generate the breakpoint signal ADBREAK— under certain stipulated conditions. Signals BKSL6 and BKSL7 are CRU output signals 6 and 7 at CRU base address >1FA0. Functions of the CRU output bits permit breakpoint to occur under four conditions:

1. When an instruction fetch is made to the breakpoint address
2. When memory is read from the address
3. When memory is written to the address
4. When the breakpoint is addressed for any condition

ADBREAK— is applied as one input to the error interrupt status register to generate a low ERSTATL6— error status signal. The error status signal causes the level 2 interrupt to be taken and the error trace memory to be activated. Additionally, ERSTATL6— is applied to a CRU multiplexer where it is available as a status signal and can be polled as CRU input bit 6 at CRU address >1FC0. The low ERSTATL6— also clears the breakpoint register.

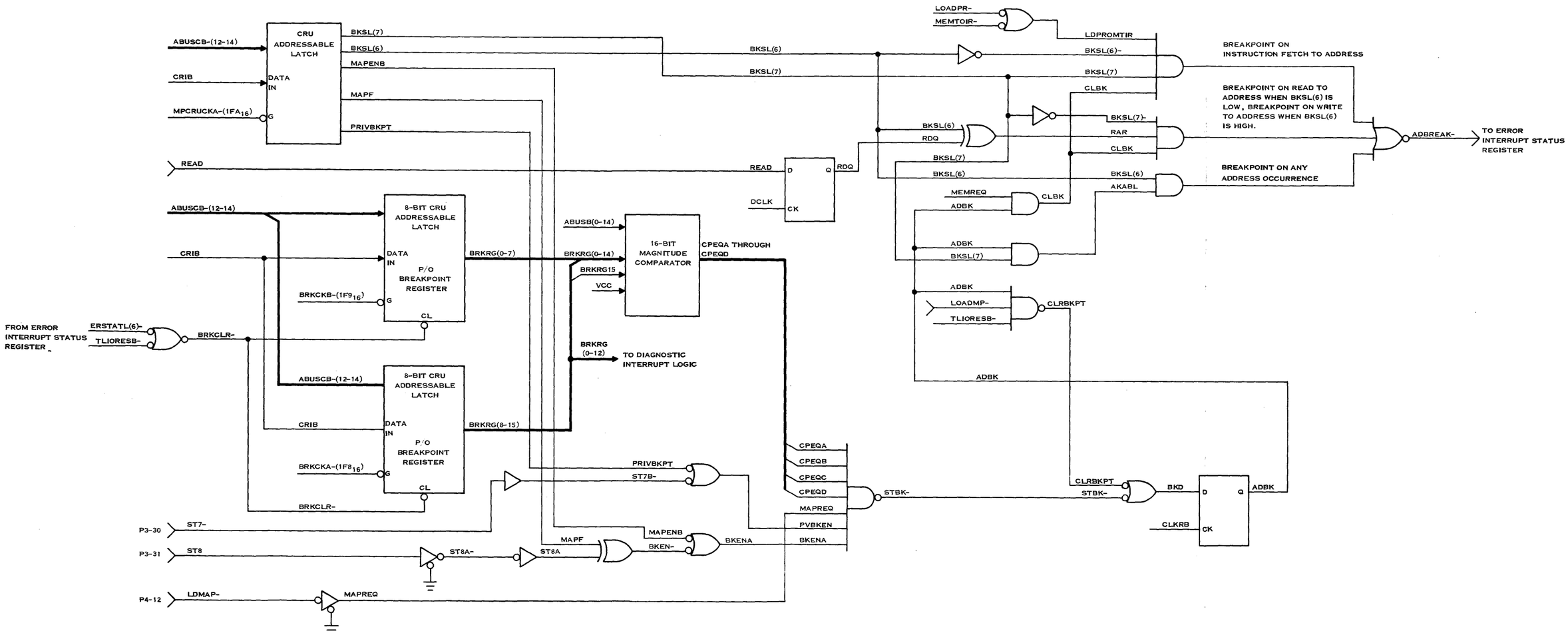

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Figure 1-8. Simplified Functional Diagram of Breakpoint System

1.4.3 System Error Interrupt Level 2

The system error interrupt is a merging of all system errors, plus breakpoint and test clock inputs in an error interrupt status register, implemented as a 12-bit CRU register at CRU base address >1FC0. Each error is stored in the error interrupt status register and is read and/or cleared through the CRU interface, and is also cleared by either an I/O reset or a master clear. Table 1-3 lists the CRU input and output bit assignments that address the system error interrupt logic.

As shown in the functional diagram for the system error interrupt, Figure 1-9, system errors plus breakpoint and test clock are applied as inputs to the system error interrupt status register to provide error status signals ERSTATL4— through ERSTATL15— at the output of the register. The error status signals are applied to a data selector/multiplexer where they can be read with a CRU input instruction addressed to CRU base address >1FC0. The error status signals are also applied to interrupt logic and to error interrupt trace memory logic. A level 2 interrupt is activated and an error interrupt trace memory cycle is generated. The error status signals can be cleared with a set bit to zero instruction to a CRU latch addressable at CRU base address >1FC0. A set bit to one instruction addressed to any of bits 0 through 7 at CRU base address >1FC0 sets all bits in the error interrupt status register for diagnostic purposes.

1.4.4 Interrupt Logic Description

The 990/12 LR minicomputer uses 16 priority-vectored levels. A priority ranking system assigns numbers from 0 (the highest priority) to 15 (the lowest priority) to the level so that interrupt conflicts can be resolved. Interrupt inputs are synchronized with the system clock on the SMI board, encoded, and presented to the processor along with an interrupt request, INTPRES—. The interrupt levels are vectored for rapid reaction to recognized interrupts. That is, corresponding to each interrupt level is a two-word vector located in low-order memory (addresses >00 through >3E). When the processor recognizes an interrupt, it loads the vector for that level into the WP (first vector word) and the PC (second vector word) to define the new WP and program starting point for the interrupt service routine. The old values of PC, WP, and ST are saved in the new workspace. When the interrupt routine is complete, the processor returns to the program that was executing when the interrupt occurred by restoring the original values to the PC, WP, and ST. Should a higher priority interrupt occur while an interrupt service subroutine is executing, the processor honors the interrupt after completing the current instruction. The processor enters the higher-priority interrupt subroutine and preserves the linkage to the earlier interrupt in the same manner described for the first interrupt. Thus, many interrupts can occur simultaneously with the processor maintaining an orderly linkage between the interrupt programs. Table 1-4 lists the interrupt levels, assignments, vector location, and mask information. The level 0 interrupt is reserved for the power-up interrupt and for the single instruction execute (SIE) function. Eleven other interrupt conditions implemented by the 990/12 LR minicomputer are internal to the operation of the computer. These 11 conditions merge as level 2 system error interrupts and are described in Table 1-3. A power failure warning pulse (TLPFWP—) generated by the power supply, is brought into the SMI board at pin 16 of P1 and is applied to the input of a priority interrupt encoder, to generate a level 1 interrupt. Interrupt levels 3 through 15 are available for assignment to external devices. The 990 family system software supports peripherals at specified interrupt levels, as shown in Table 1-4.

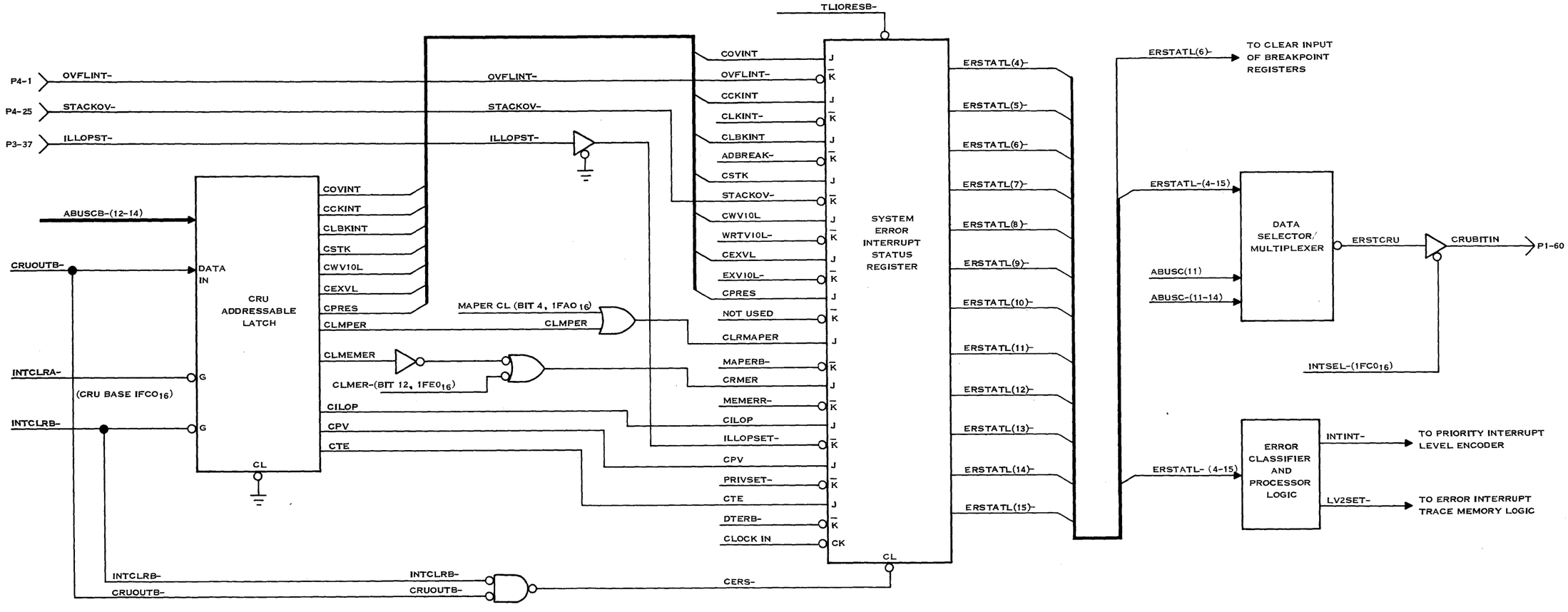

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Figure 1-9. System Error Interrupt Level 2, Functional Diagram

Table 1-3. System Error Interrupt CRU Bit Assignments (CRU Base Address >1FC0)

Input Bit	Output Bit[1]	Error Condition
4	4	Arithmetic overflow
5	5	12 ms test clock
6	6	Breakpoint address encountered
7	7	Stack overflow/underflow
8	8	Write attempt in protected memory
9	9	Execution violation. Indicates an attempt to execute from a mapped memory segment that was flagged as nonexecutable.
10	10	Not used
11	11[2]	Mapping error. Indicates an attempt to address memory beyond the limits set in the active map file limit register.
12	12[3]	Memory data error
13	13	Illegal operation
14	14	Privileged instruction fetch with privileged mode off.
15	15	TILINE time-out. Indicates an attempt to address unimplemented TILINE address (memory).

Notes:

[1] Individually cleared by SBZ instruction. An SBO instruction to bits 0 through 7 of this register sets all bits for diagnostic purposes.

[2] Can be cleared by SBZ instruction to mapping feature bit 4 (CRU base address > 1FA0) for 990/10 compatibility.

[3] Can be cleared by SBO or SBZ instruction to programmer panel bit 12 (CRU base address > 1FE0) for 990/4 compatibility.

Table 1-4. Interrupt Level Data

Interrupt Level	Vector Location*	Device Assignments	Enabling Mask Values
0	00	Power-up	0 through F
1	04	Power Failure	1 through F
2	08	Error	2 through F
3	0C	Open	3 through F
4	10	Card Reader	4 through F
5	14	Real-time clock	5 through F
6	18	733 ASR/KSR	6 through F
7	1C	Open	7 through F
8	20	Open	8 through F
9	24	MT1600 Tape Controller	9 through F
10	28	911 CRT No. 1 and No. 2	A through F
11	2C	Open	B through F
12	30	Open	C through F
13	34	System Disk	D through F
14	38	Line Printer	E and F
15	3C	Open	F only

Note:

* Trap address

1.4.4.1 Masking. The processor uses a 4-bit field in the ST to determine the lowest-priority interrupt that will be recognized during a program operation and also to ensure that an interrupt service routine will not be halted due to another interrupt of equal or lower priority.

At the start of a program, the mask field in the ST is loaded with the mask value. The processor compares this value with any interrupts that occur. If the level of the interrupt is equal to or less than the mask value (of equal or greater priority), the processor recognizes the interrupt and calls the service routine for that interrupt level. When the processor sets up for the service routine, it loads a value into the mask field that is one less than the interrupt level being serviced, thereby disabling interrupts from devices of equal or lower priority. The enabling mask values for the different interrupt levels are shown in Table 1-4.

1.4.4.2 Priority Interrupt Level Encoder. The logic for implementing interrupt levels 0 through 15 is located on the SMI board and consists primarily of an interrupt input register and a priority encoder. Figure 1-10 is a functional diagram of the priority interrupt level encoder. The interrupt input register consists of two SN74LS374s, each containing eight D-type flip-flops. The 14 interrupts, TLPFWP— and I(3)— through I(15)—, are applied as D inputs to the flip-flops and are transferred to the Q outputs on the positive transition of the CLKM clock signal. The Q outputs are applied as inputs to the priority encoder that consists of two cascaded 8-line-to-3-line priority encoders. Also applied to the priority encoder are the single instruction execute (SIE) signal, FPINTR—, and the system error interrupt level 2 signal, INTINT—. The SIE signal is encoded as a level 0 interrupt. Signals LEV0— through LEV3— at the output of the priority encoder provide a binary-coded interrupt level that corresponds to the highest-priority interrupt level input. An interrupt, at any level, causes a low interrupt INTPRES— signal to be generated and applied to the AU board along with signals ILEV0— through ILEV3— (the binary-coded interrupt level signals). Note that in addition to being applied to the priority encoder, the level 0 interrupt is applied directly to the AU board as signal FPINT—. This permits front panel interrupts even though the disable interrupts instruction has been invoked.

As shown in Figure 1-10, 13 bits of the breakpoint register can be used as a diagnostic tool to set or reset interrupt levels 3 through 15. The breakpoint register is addressed at CRU base address >1F80. CRU output bits 3 through 15 (corresponding to register output signals BRKRG12 through BRKRG0, respectively) are used to set or reset interrupt levels 3 through 15.

The interrupt diagnostic mode is enabled with an SBO instruction addressed to CRU output bit 8 at CRU base address >1FA0, to set DITEN high. The breakpoint register is then addressed at CRU base address >1F80, setting output bit 0 to logic 0 (to disable the breakpoint system) and setting output bits 3 through 15 with appropriate interrupt information.

Power Failure Interrupt. When ac power begins to fail, a sensor in the power supply generates a low TILINE power failure warning pulse (TLPFWP—) that is applied to the SMI board. TLPFWP— is applied as an input to the interrupt input register and is encoded as a level 1 interrupt. At this point, the computer has two milliseconds of program time before a power supply reset (TLPRES—) halts operation. This interrupt sets the interrupt mask in the ST to 0.

Real-Time Clock Interrupt. The power supply contains a line-frequency synchronized clock that generates the 100- or 120-hertz signal. The real-time clock interrupt logic is implemented on the SMI board. A signal is generated every 8.33 or 10 milliseconds to provide a level 5 interrupt request. The interrupt is enabled by a low CLKON— signal from the AU board in response to the control instruction CKON. The interrupt is cleared by either a low CLKOFF— signal from the AU board in response to the CKOF instruction or a low TLIORESB— signal generated by a RSET instruction. TLIORESB— is also generated by the TLPRES— power-up sequence from the power supply. Though the real-time clock is normally wired for level 5 interrupt, it can be wired for level 15 interrupt. When the level 5 interrupt occurs, the processor sets the interrupt mask to 4.

1.4.5 Error Interrupt Trace Memory

When an error interrupt or breakpoint occurs, the error interrupt trace memory contains a trace of the 15 memory cycles prior to and including the fetch of the error interrupt trap vector. The trace memory does not stop immediately upon setting of the interrupt, but stores one more workspace access or memory cycle to make the sixteenth word.

The error interrupt trace memory consists of eight 64-bit RAM devices, each organized as sixteen 4-bit words, that provides read/write capability for sixteen 32-bit trace words. Each 32-bit word consists of a 20-bit address field and a 12-bit status code. Figure 1-11 provides a functional diagram of the error interrupt trace memory. Additional information on the function of the bits of the trace words can be found in the *Model 990/12 LR Computer, General Description.*

1.4.6 12-Millisecond Test Clock

The 12-millisecond test clock resides on the SMI board. When enabled, the 12-millisecond test clock generates an interrupt from which a service routine determines the percentage of time used by various system routines and the percentage of time available to users.

As shown in Figure 1-12 an SBO instruction addressed to CRU output bit 1 at CRU base address >1FA0, generates a high test clock enable TSTCKEN. TSTCKEN, clocked through a flip-flop by an output of the test clock, provides a 12-millisecond test clock interrupt input to the error interrupt status register. When the clock interrupt occurs, the system error interrupt (level 2) is taken and the 12-millisecond test clock flag is set in the error interrupt status register (CRU input bit 5 of CRU base address >1FC0). The interrupt is cleared by addressing an SBZ instruction to CRU output bit 5 at CRU base address >1FC0. A power-up or RSET instruction clears and disables the clock interrupt.

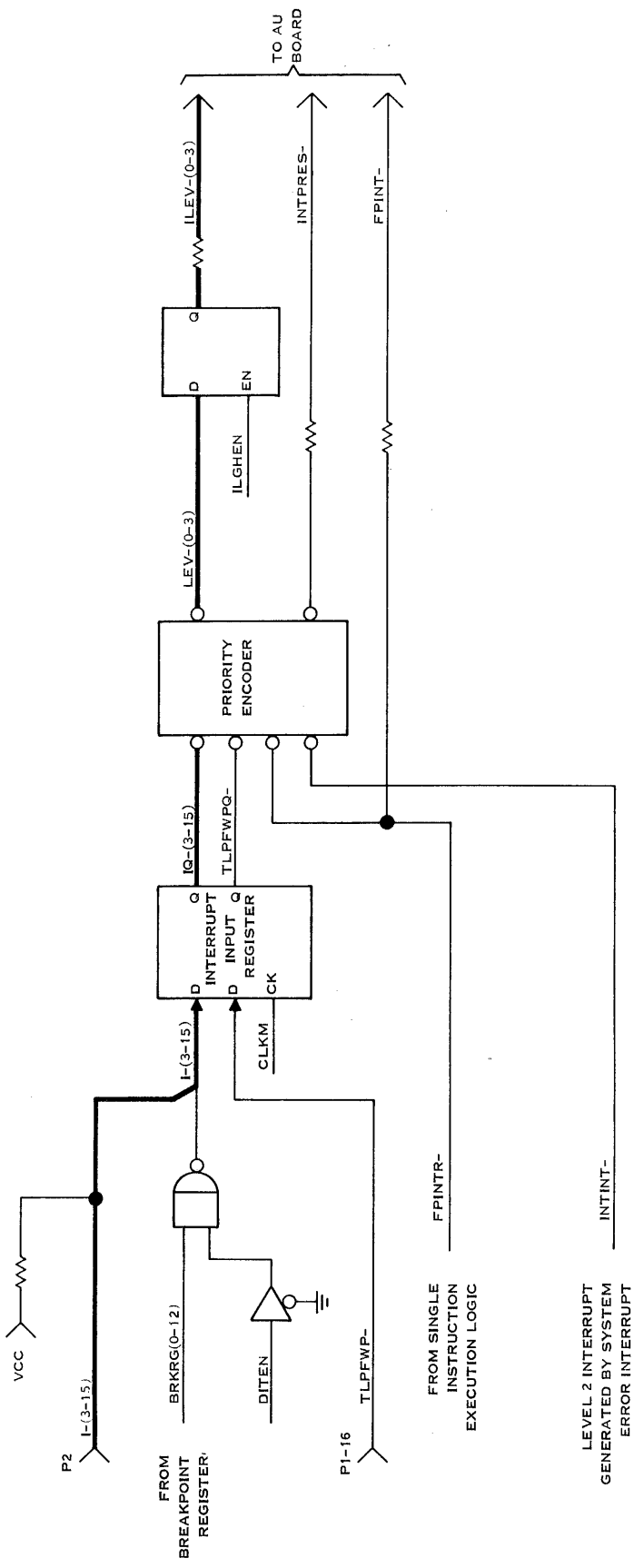

Figure 1-10. Priority Interrupt Level Encoder

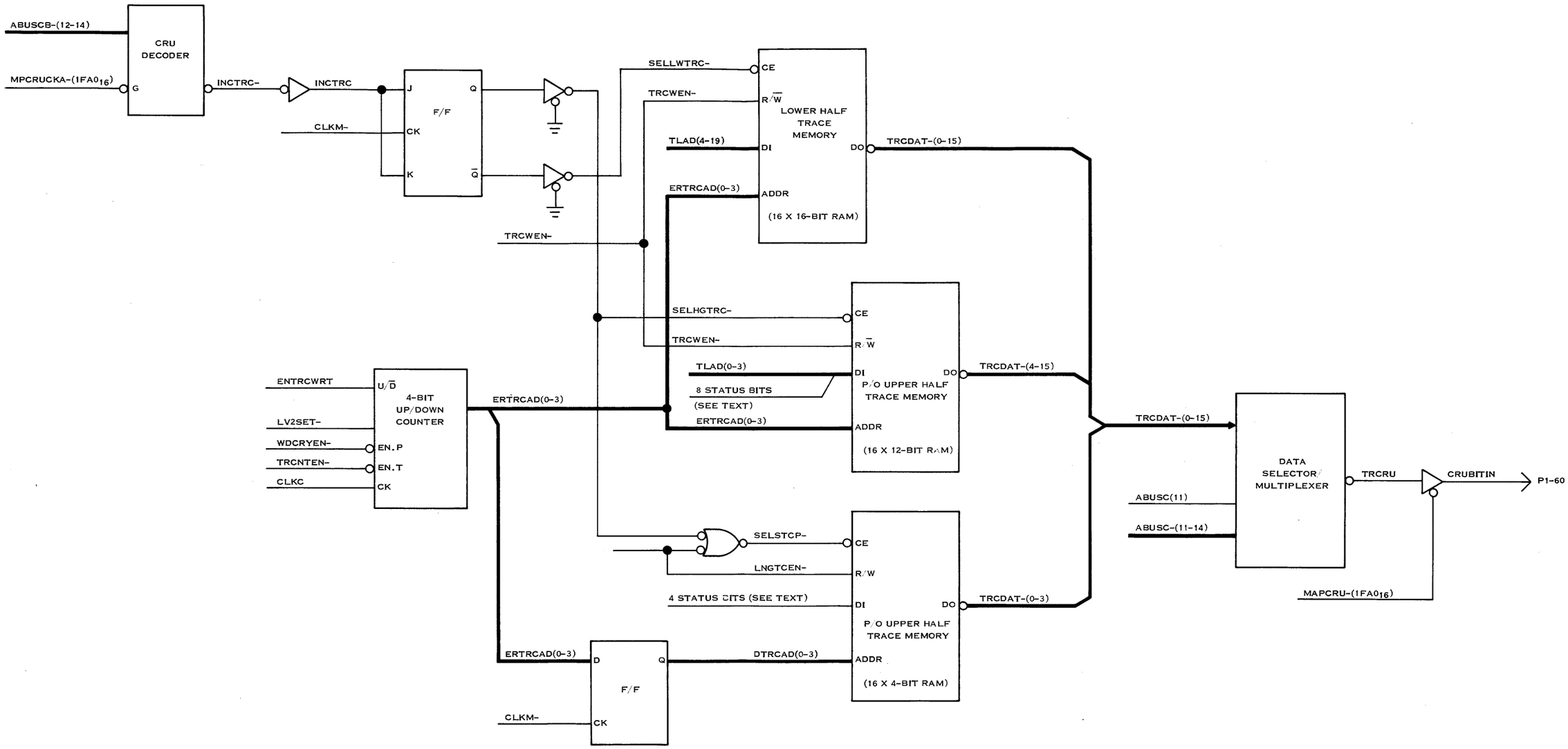

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Figure 1-11. Error Interrupt Trace Memory Functional Diagram

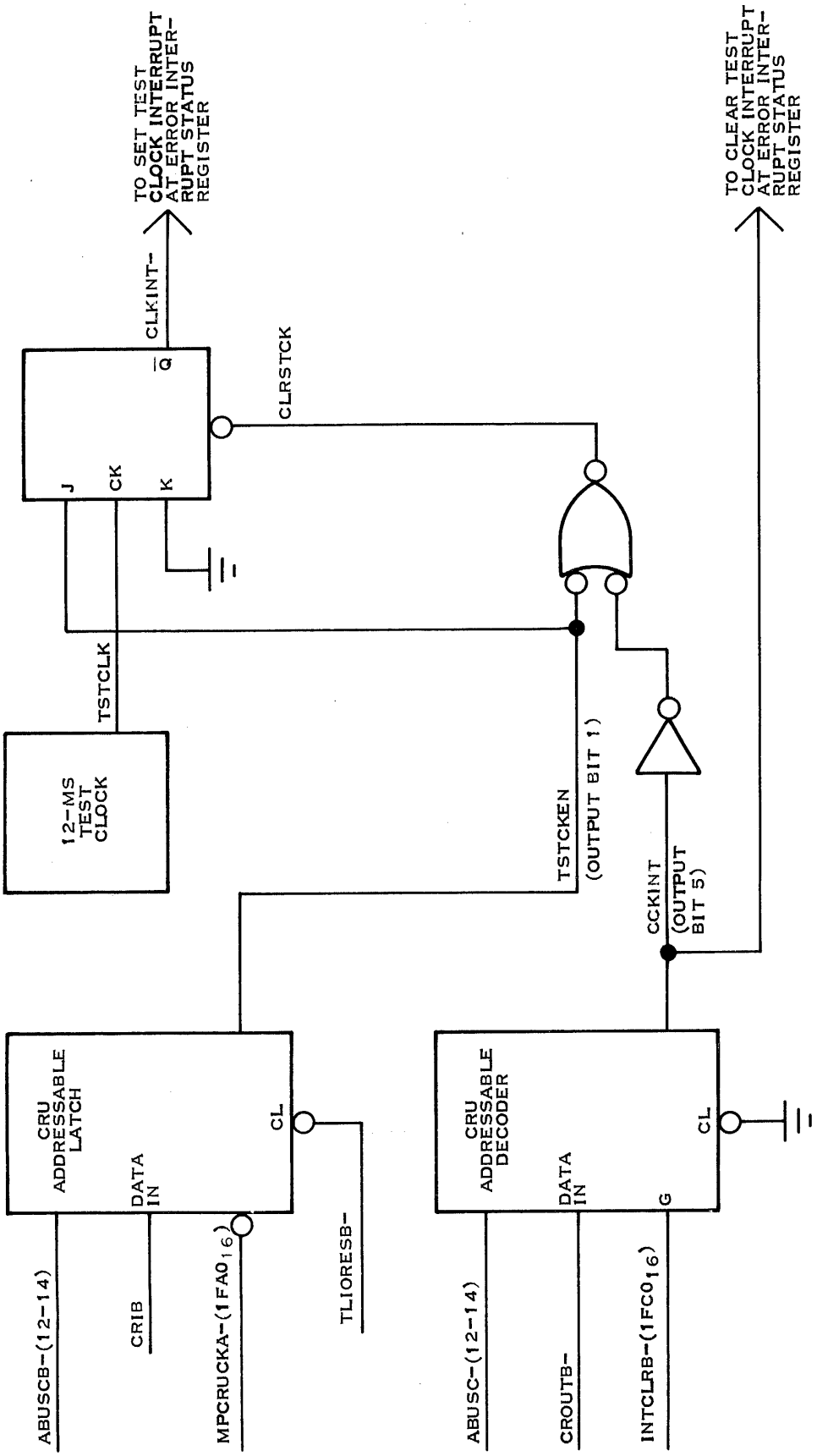

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Figure 1-12. 12-Millisecond Test Clock Interrupt Functional Diagram

1.4.7 Diagnostic Registers

Figure 1-13 shows that the diagnostic registers logic contains five shift/storage registers and a data selector/multiplexer. Each shift/storage register is loaded parallel with the signals to be monitored by that register. These signals are serially clocked out of the shift/storage register as an input to a data selector/multiplexer. Additional information can be found in the *990/12 LR Computer, General Description*.

1.4.8 Programmer Panel Interface

The programmer panel interface is comprised of TTL devices mounted on the SMI board that serve as the interface between the processor on the AU board and the programmer panel. Thirteen signal lines plus 5 volts of main power and ground are brought to a 20-pin male connector, plug P5, mounted at the top edge of the SMI board. The interface to the programmer panel is completed through a 20-conductor ribbon cable. The interface signals are as shown in Figure 1-14. The description that follows for the signals and how they are implemented is keyed to the simplified logic diagram of Figure 1-15.

1.4.8.1 Communications Register Unit (CRU) Bit Select Bits. The CRU bit select bits (CONSBIT12 through CONSBIT15) are developed from bits of the processor address bus as follows. Address bus signals ADDR3— through ADDR14— are brought into the SMI board at connector P3, applied to bus drivers, and clocked through a register to provide signals ABUSC3— through ABUSC14—. CONSBIT12 through CONSBIT15 are the bit select field of the CRU 12-bit address word and as shown in Figure 1-15, are developed from signals ABUSC11— through ABUSC14—. During a read operation, the bit select field bits applied to the programmer panel select a particular bit for input to the processor; during a write operation, the bits are used to generate control strobes in the programmer panel.

1.4.8.2 CONSCLK— Signal. The CONSCLK— signal is active when low to generate control strobe enable or write enable logic in the programmer panel. When a CRU device such as the programmer panel is being addressed in an output operation, the processor and logic on the AU board provide a low STCEN— signal to the SMI board. The inverted STCEN— signal is ANDed with the PRIVCRU— signal on the SMI board. PRIVCRU— is also high if the processor is not in the privileged instruction mode (status bit ST7 equals 1) and a high STCLKEN signal is generated. STCLKEN is ANDed with delayed clock signals to provide the CRU clock, CRCK. When CRCK goes high, a low CONSCLK— signal is provided at the programmer panel interface.

1.4.8.3 CONSEL— Signal. A low CONSEL— signal at the programmer panel interface signifies to the programmer panel that it has been selected as the addressed module. Address bits ADDR3— through ADDR10— received from the processor address bus are inverted and clocked through a register to provide a high ABUSC(8) signal, low ABUSC(3)— through ABUSC(7)— signals, and low ABUSC(9)— and ABUSC(10)— signals when the programmer panel is to be addressed. These signals applied to the module select decoder generate the low CONSEL— signal.

1.4.8.4 Serial Data Lines CONSBITD and CONSCRUI. CRUOUT— serial data from the central processor is brought into the SMI board at the P4 connector and is applied through a series of inverter-buffers and a resistor to the programmer panel interface as the CONSBITD signal. CONSBITD is sampled by the programmer panel when the CONSCLK— input to the programmer panel goes low. CONSCRUI serial input data from the programmer panel is applied to a three-state driver that is enabled by the low CONSELB— signal when the programmer panel is the addressed module. The output of the driver is applied to the AU board as CRUBITIN.

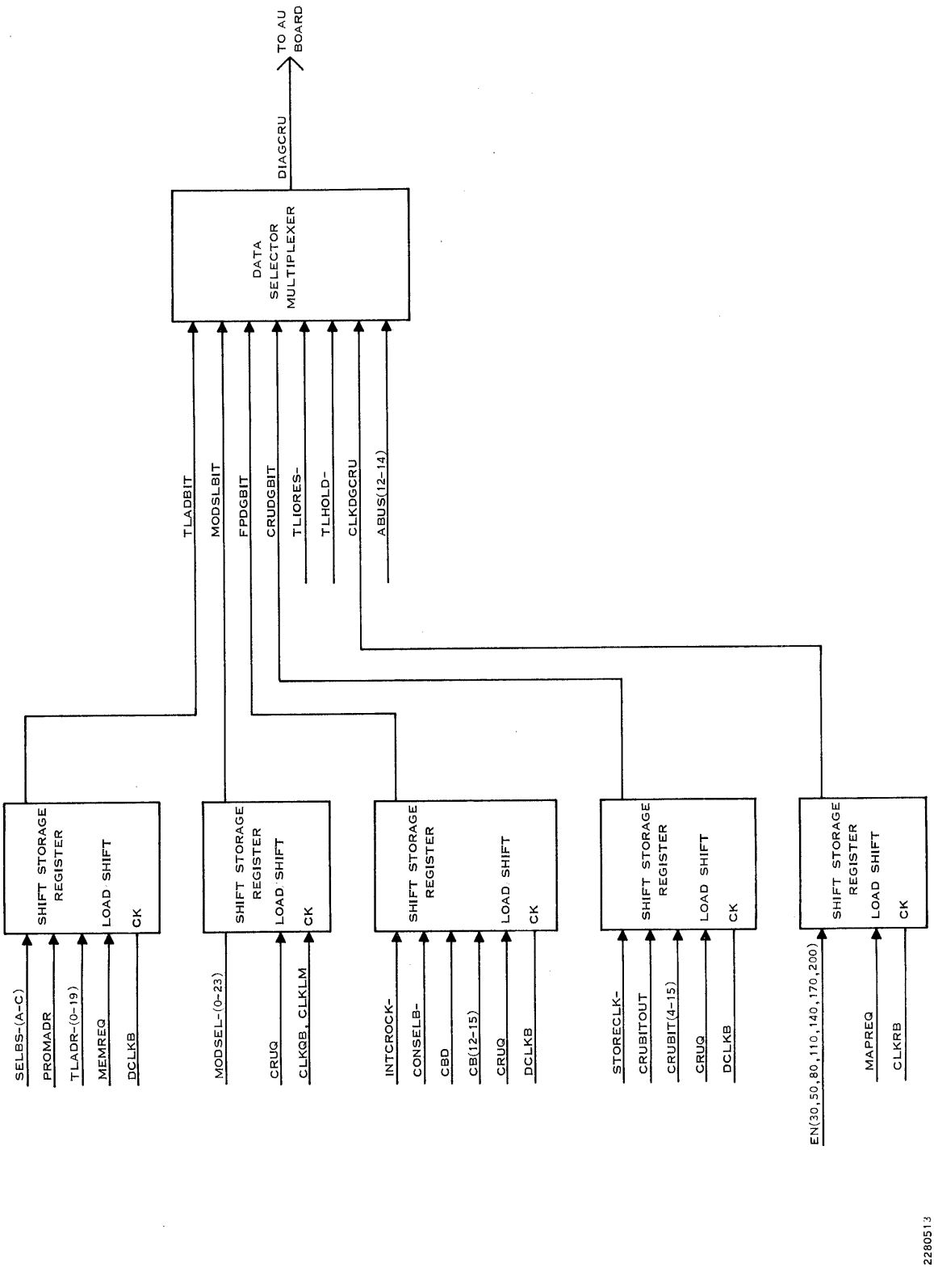

Figure 1-13. Diagnostic Registers

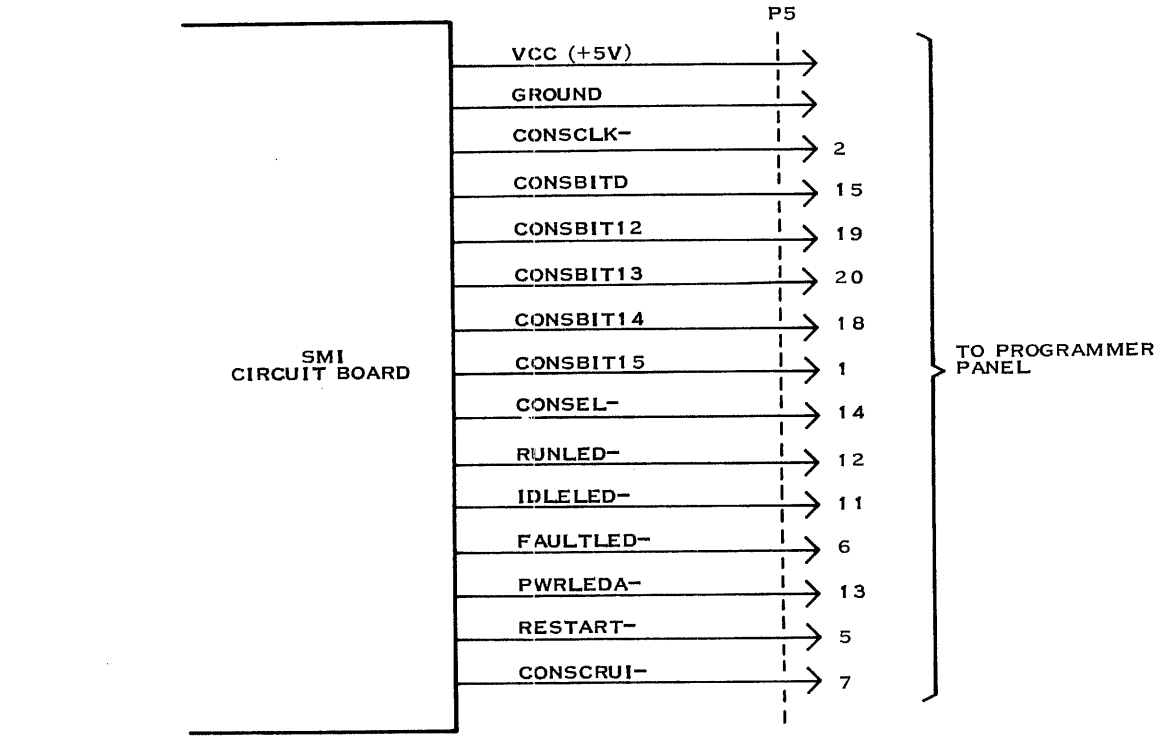

Figure 1-14. Programmer Panel Interface Signals

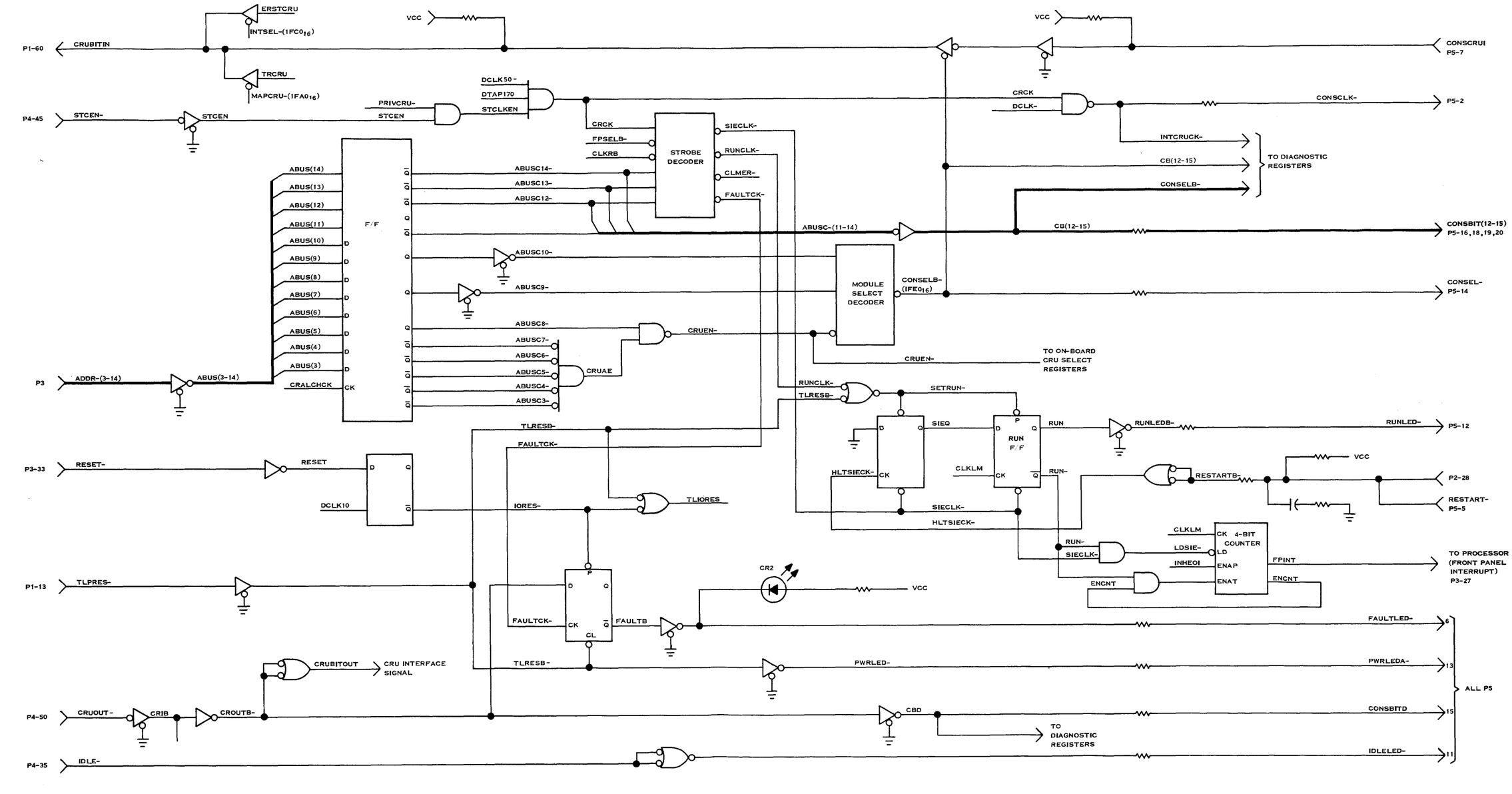

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Figure 1-15. Programmer Panel Interface

1.4.8.5 PWRLEDA— Signal. A normally high TLPRES— supplied by the computer power supply to the SMI board at the computer back panel is inverted on the SMI board and applied through a resistor to the programmer panel interface as the normally low PWRLEDA— signal. The low PWRLEDA— signal illuminates the POWER LED on the front panel to indicate that the system power supply is on.

1.4.8.6 FAULTLED— Signal. The FAULTLED— signal is a programmable low output signal generated by the central processor to illuminate the FAULT LED on the front panel as well as a fault lamp on the SMI board to indicate the result of a processor test. A logic one on the central processor CRUOUT data line addressed to the programmer panel CRU output bit 11 lights the panel and board lamps. As shown in Figure 1-15, a logic one on the CRUOUT data line provides a low at the CRUOUT— input to the SMI board and at the D input to the fault flip-flop. This low is clocked out of the flip-flop as a high FAULTB signal by the FAULTCK— strobe. FAULTB is inverted and is provided to the programmer panel interface as the FAULTLED— signal. The low output of the inverter also lights the fault lamp on the SMI board. FAULTCK— is generated at the output of a strobe decoder when CRU output bit 11 of the programmer panel is addressed. Both fault lamps are illuminated following a power-up and are turned off by the user's software or by the self-test option. An SBZ instruction addressed to programmer panel CRU output bit 11 or a RSET instruction extinguishes both lamps. An SBO instruction can turn on the fault lamps.

1.4.8.7 RUNLED— Signal. The RUNLED— signal is an active-when-low signal at the programmer panel interface that is generated by the computer while in the RUN mode. The low illuminates the RUN LED on the front panel. As shown in Figure 1-15, either a low TLPRES— or a low RUNCLK— signal sets a flip-flop to provide a high RUN signal that is inverted and applied to the programmer panel interface through a series resistor as RUNLED— signal. Since TLPRES— is initially low during a power-up, the RUNLED— signal is always generated when power is applied. The low RUNCLK— signal is programmable and is generated with an SBO or SBZ instruction addressed to CRU output bit 10 of the programmer panel.

1.4.8.8 RESTART— Signal. RESTART— is a low signal generated at the programmer panel interface by pressing the HALT/SIE switch on the programmer panel. On the SMI board, RESTART— is inverted and clocks a low SIEQ signal out of a flip-flop. SIEQ, in turn, is clocked through the RUN flip-flop to generate a low RUN signal. The RUNLED— signal goes high and the programmer panel moves into the active (HALT) mode of operation.

As the Q— output of the RUN flip-flop goes high in response to the RESTART— signal, RUN— enables and presets a four-bit counter to a count of 13. After two additional assembly language instructions, the counter generates a high FPINT pulse that in turn generates a low FPINT— signal causing the processor to trap to memory address >FFFC. This front panel pulse occurs even though disable interrupt instruction DINT has been invoked. The high ENDINSTR— returned from the AU board provides the low INHEOI signal to the counter to prevent the generation of a new FPINT pulse.

1.4.8.9 IDLELED— Signal. A low IDLELED— signal at the programmer panel interface illuminates the IDLE LED on the panel as an indication of processor inactivity. When the processor executes an IDLE instruction, it causes a low IDLE— signal to be applied to the SMI board. On the SMI board, IDLE— applied to a driver generates a low IDLEDLED— signal that is applied to the programmer panel interface through a series resistor. The low IDLE— signal from the processor changes state when program execution resumes due to an interrupt, load, or reset.

1.4.9 Communications Register Unit (CRU) Interface

The direct-command-driven I/O interface for the processor is called the CRU. The CRU provides for up to 4096 directly addressable output bits. Input and output operations can address each of the bits individually or in fields from 1 to 16 bits. The processor instructions that drive the CRU can set, reset, or test any bit in the CRU array, and the processor instructions can move data between memory and the CRU data fields.

Logic for the CRU interface is mounted on the SMI board, and exerts control over the interface data and control lines. Except for module select signals and the slot location used for the SMI board, these lines are available to all main chassis locations. Twenty-four module select signals which CRU interface logic decodes, are made available to chassis slot locations 2 through 13.

1.4.9.1 CRU Applications. Because of its extremely flexible data format, the CRU can be used effectively for a wide range of control and data operations. These operations can be divided into two broad categories; those involving a single control bit transfer, and those requiring input or output of a word of several data or status bits.

Single-Bit Operations. Single-bit operations typically involve the computer sampling a status bit. When the status bit sets, the computer responds by setting a control bit or by transferring to a different set of instructions. For example, a communications interface unit can generate a single interrupt for one of several reasons such as output complete, input complete, or line status change. An output or input complete requires a transfer to instructions that perform another output or input operation. A line status change might require setting a control output or transferring to instructions that handle the change in other ways.

Multiple-Bit Operations. Multiple-bit operations typically involve a data input device such as a keyboard or card reader, or an output device such as a display or card punch. An interrupt from the device causes the processor to perform an STCR instruction to read data from the CRU device and store it in memory. Similarly, to send data to the device the processor executes an LDCR instruction to fetch data from memory and transfer it to the CRU device.

1.4.9.2 CRU Interface Signals. Logic on the SMI board implements a dedicated CRU interface for the programmer panel, and also implements a standard CRU interface for the main chassis. The CRU interface signals to the main chassis are brought to the bottom edge connectors, P1 and P2, of the SMI board. Table 1-5 provides the function for each of the CRU interface signals, the pin numbers of the signals on the SMI board, and the pin numbers of the signals as they appear on the backpanel chassis slots of the main chassis. Both connectors in each chassis slot are furnished with the CRU bit select bits (CRUBIT 12-15) and other CRU interface signals that permit each connector to address 16 bits of the CRU. Connector P1 in a chassis slot receives one module select signal corresponding to one 16-bit register, whereas connector P2 receives two module select signals and thus can address up to 32 bits of the CRU. Connector P1 also receives the 8 most significant bits of the CRU address, thereby permitting the chassis slot to be used for a CRU expansion driver or for modules that ignore module select signals to directly decode their own CRU address.

1.4.10 TILINE Logic

The 990/12 LR computer uses a high-speed, bidirectional 16-bit data bus called the TILINE, which, along with associated control lines, serves to transfer data between all high-speed system elements. The following discusses implementation and logic for the TILINE bus.

Table 1-5. CRU Interface Signals

Signature	SMI Board* Pin Number	Slot 2-13 Pin Number	Function
CRUBIT4	P1-56	P1-56	Address bits generated by the processor to select a particular chassis (bits 4 through 6), a 16-bit module within that chassis (bits 7 through 11), and a particular bit from that module (bits 12 through 15). CRUBITS 4 through 11 are capable of driving at least 12 normalized TTL loads; CRUBITS 12 through 15 are capable of driving 30 normalized TTL loads.
CRUBIT5	P1-54	P1-54	
CRUBIT6	P1-52	P1-52	
CRUBIT7	P1-50	P1-50	
CRUBIT8	P1-62	P1-62	
CRUBIT9	P1-64	P1-64	
CRUBIT10	P1-68	P1-68	
CRUBIT11	P1-70	P1-70	
CRUBIT12	P1-36	P1-36, P2-36	
CRUBIT13	P1-32	P1-32, P2-32	
CRUBIT14	P1-38	P1-38, P2-38	
CRUBIT15	P1-34	P1-34, P2-34	
CRUBITOUT	P1-18	P1-18, P2-18	Serial data line for transfer of data from the processor to the addressed CRU bit(s). This line is active only when STORECLK— goes low. (Will drive 30 normalized TTL loads.)
CRUBITIN	P1-60	P1-60, P2-60	Serial data line for transfer of data from the addressed CRU bit to the processor. This line must be driven by an open collector gate and only when the module is selected. A 470-ohm pullup resistor is mounted on the SMI circuit board for this line.
STORECLK—	P1-22	P1-22, P2-22	An active-when-low pulse that indicates to the selected CRU module that the operation is a write (set bit or LDCR) operation. This pulse transfers the data on the CRUBITOUT line into a holding flip-flop that is the CRU bit. (Will drive 30 normalized loads.)
TLIORES—	P1-14	P1-14, P2-14	I/O Reset: A normally high signal that, when low, resets all connected devices. This signal is a minimum 250 ns pulse that is generated by a RSET instruction in the processor. This signal is also low until dc power is up and stable. Will drive 30 TTL loads.

Note:

* Pin numbers shown are valid for the SMI board except for signals MODSEL24— through MODSEL31— and INT16— through INT31—. These signals are not implemented on the SMI board, and these pin numbers are assigned to TILINE data signals 4 through 11 and TILINE address signals 0 through 15 on that board. If these signals are implemented in CRU expansion, TILINE expansion cannot be used in the same chassis.

Table 1-5. CRU Interface Signals (Continued)

Signature	SMI Board* Pin Number	Slot 2-13 Pin Number	Function
TLPFWP—	P1-16	P1-16, P2-16	Power Failure Warning Pulse: A pulse that precedes TLPRES— by 2 ms and indicates that a power failure is imminent. Will drive 30 TTL loads.
TLPRES	P1-13	P1-13, P2-13	Power Reset: A normally high signal that goes low to reset connected devices at least 10 μs before dc voltages begin to fail during power-down. During power-up, this signal is low until all voltages are stable.
MODSEL0—	P1-23	Slot 13, P2-48	Module select signals generated by the processor from address bits 6 through 10 (CRUBITS 7 through 11). Note that P1 in each slot of the backpanel receives one module select signal, whereas P2 receives two module select signals. This configuration permits P2 to use 32 bits of the CRU. Note that pins 48 of successive P2 connectors in the chassis slots are connected to even-numbered module select signals and, at the CRU circuit board level, carry a MODSELA— signature. Pins 46 of successive P2 connectors in the chassis slots are connected to pin 48 of P1 of that slot and then to an odd-numbered module select signal and carry a signature of MODSELB—. Pin P1-48 is not used when a full-sized CRU circuit board is installed in a chassis slot.
MODSEL1—	P1-35	Slot 13, P1-48 and P2-46	
MODSEL2—	P1-37	Slot 12, P2-48	
MODSEL3—	P1-43	Slot 12, P1-48 and P2-46	
MODSEL4—	P1-44	Slot 11, P2-48	
MODSEL5—	P1-45	Slot 11, P1-48 and P2-46	
MODSEL6—	P1-46	Slot 10, P2-48	
MODSEL7—	P1-47	Slot 10, P1-48 and P2-46	
MODSEL8—	P1-48	Slot 9, P2-48	
MODSEL9—	P1-49	Slot 9, P1-48 and P2-46	
MODSEL10—	P1-51	Slot 8, P2-48	
MODSEL11—	P1-53	Slot 8, P1-48 and P2-46	
MODSEL12—	P1-61	Slot 7, P2-48	
MODSEL13—	P1-67	Slot 7, P1-48 and P2-46	

Note:

* Pin numbers shown are valid for the SMI board except for signals MODSEL24— through MODSEL31— and INT16— through INT31—. These signals are not implemented on the SMI board, and these pin numbers are assigned to TILINE data signals 4 through 11 and TILINE address signals 0 through 15 on that board. If these signals are implemented in CRU expansion, TILINE expansion cannot be used in the same chassis.

Table 1-5. CRU Interface Signals (Continued)

Signature	SMI Board* Pin Number	Slot 2-13 Pin Number	Function
MODSEL14—	P1-69	Slot 6, P2-48	
MODSEL15—	P1-71	Slot 6, P1-48 and P2-46	
MODSEL16—	P2-38	Slot 5, P2-48	
MODSEL17—	P2-36	Slot 5, P2-48 and P2-46	
MODSEL18—	P2-34	Slot 4, P2-48	
MODSEL19—	P2-32	Slot 4, P1-48 and P2-46	
MODSEL20—	P2-22	Slot 3, P2-48	
MODSEL21—	P2-18	Slot 3, P1-48 and P2-46	
MODSEL22—	P2-16	Slot 2, P2-48	
MODSEL23—	P2-13	Slot 2, P1-48 and P2-46	
MODSEL24—	P2-61		
MODSEL25—	P2-63		
MODSEL26—	P2-43		
MODSEL27—	P2-45		
MODSEL28—	P2-21		
MODSEL29—	P2-33		
MODSEL30—	P2-23		
MODSEL31—	P2-20		

Note:

* Pin numbers shown are valid for the SMI board except for signals MODSEL24— through MODSEL31— and INT16— through INT31—. These signals are not implemented on the SMI board, and these pin numbers are assigned to TILINE data signals 4 through 11 and TILINE address signals 0 through 15 on that board. If these signals are implemented in CRU expansion, TILINE expansion cannot be used in the same chassis.

Table 1-5. CRU Interface Signals (Continued)

Signature	SMI Board* Pin Number	Slot 2-13 Pin Number	Function
INT3—	P2-24		Each side of each full-sized chassis slot is furnished with a pin (P1-66 and P2-66) through which a CRU circuit board can interrupt the processor. These pins are connected to interrupt levels in accordance with assigned priorities.
INT4—	P2-46		
INT5—	P2-48		
INT6—	P2-50		
INT7—	P2-52		
INT8—	P2-54		
INT9—	P2-56		
INT10—	P2-58		
INT11—	P2-62		
INT12—	P2-64		
INT13—	P2-65		
INT14—	P2-66		
INT15—	P2-68		
INT16—	P2-55		
INT17—	P2-44		
INT18—	P2-51		
INT19—	P2-53		
INT20—	P2-57		
INT21—	P2-59		
INT22—	P2-47		
INT23—	P2-49		
INT24—	P2-17		
INT25—	P2-19		
INT26—	P2-10		
INT27—	P2-12		
INT28—	P2-11		
INT29—	P2-15		
INT30—	P2-8		
INT31—	P2-9		

Note:

* Pin numbers shown are valid for the SMI board except for signals MODSEL24— through MODSEL31— and INT16— through INT31—. These signals are not implemented on the SMI board, and these pin numbers are assigned to TILINE data signals 4 through 11 and TILINE address signals 0 through 15 on that board. If these signals are implemented in CRU expansion, TILINE expansion cannot be used in the same chassis.

1.4.10.1 TILINE Applications. The TILINE bus is fully implemented on high-capability 990 computers, including the 990/12 LR minicomputer. It is used as the path of data communication between all high-speed system elements. The CPU, main memory, and all high-speed peripheral devices, such as disk files and magnetic tape transports, are directly connected to the TILINE bus. Slower peripheral devices, such as EIA-compatible devices, are connected to the 990/12 LR through the CRU. The interface to the minicomputer system of either a CRU or a TILINE device is made through installing either device into a slot of the chassis backpanel since the CRU and TILINE share the same backpanel but use different pin positions.

1.4.10.2 Master-Slave Concept. There are two classes of devices that connect to the TILINE bus: TILINE master devices that control data transfers, and TILINE slave devices that generate or accept data in response to a master device. Data transfers in either direction always occur between one master and one slave. The CPU is an example of a master device, and a memory module is an example of a slave device. All slave devices recognize a specific address and are activated only when addressed. For example, a memory module is activated when some master device performs a read operation from an address within the bounds of its address. The configuration of the system must be such that only one slave device recognizes any particular address. Pencil switches on the memory modules are set to provide the starting address and size of the module.

Peripheral controllers are both master and slave devices. Special registers addressed as specific memory addresses near the high end of memory constitute the slave part of the peripheral controller. The registers are loaded by the CPU with memory-to-memory move instructions. The registers specify the parameters of a peripheral data transfer. In the case of a disk, they specify a disk address, the number of sectors of data to be transferred, the new memory address of the data, and whether the data is to be read or written. One register in each peripheral controller is a status register for that controller. The bits in the register indicate information such as operation complete, read error, rewind complete, and illegal command. Other bits in the peripheral controller status register are set by the CPU to command the peripheral to start, stop, clear its interrupt, or reset. All of these registers are addressed by the CPU as consecutive words of memory at some specific address. Pencil switches are used to set the address of the registers for each peripheral controller. When a peripheral controller is started by the CPU, it transfers data between memory and the peripheral device by cycle-stealing with the CPU and any other master devices that may be active. When a peripheral controller needs to transfer a word of data over the TILINE bus, the master device part of the peripheral controller must gain access to the TILINE and then can address a slave (such as a memory module) and read from or write to it.

1.4.10.3 TILINE Interface Signals. There are 48 TILINE interface signals that perform the addressing, data transfer, and control functions of the TILINE bus. Figure 1-16 illustrates and Table 1-6 defines the TILINE interface signals and gives their connector pin numbers assigned at the chassis backpanel. The signals are functionally grouped and are described in the three subparagraphs that follow.

Data Transfer Operations. There are 40 TILINE interface signals that are used exclusively for data transfer operations on the TILINE bus. As shown in Figure 1-16, 36 of these signals consist of the 20 address bits and 16 data bits with the remaining four signals used primarily for control of the actual data transfer operation. These four signals are TLGO—, TLREAD, TLTM—, and TLMER—. All signals are transmitted and received between a TILINE master device and a TILINE slave device during a data transfer. A description of both a read and write data transfer follows.

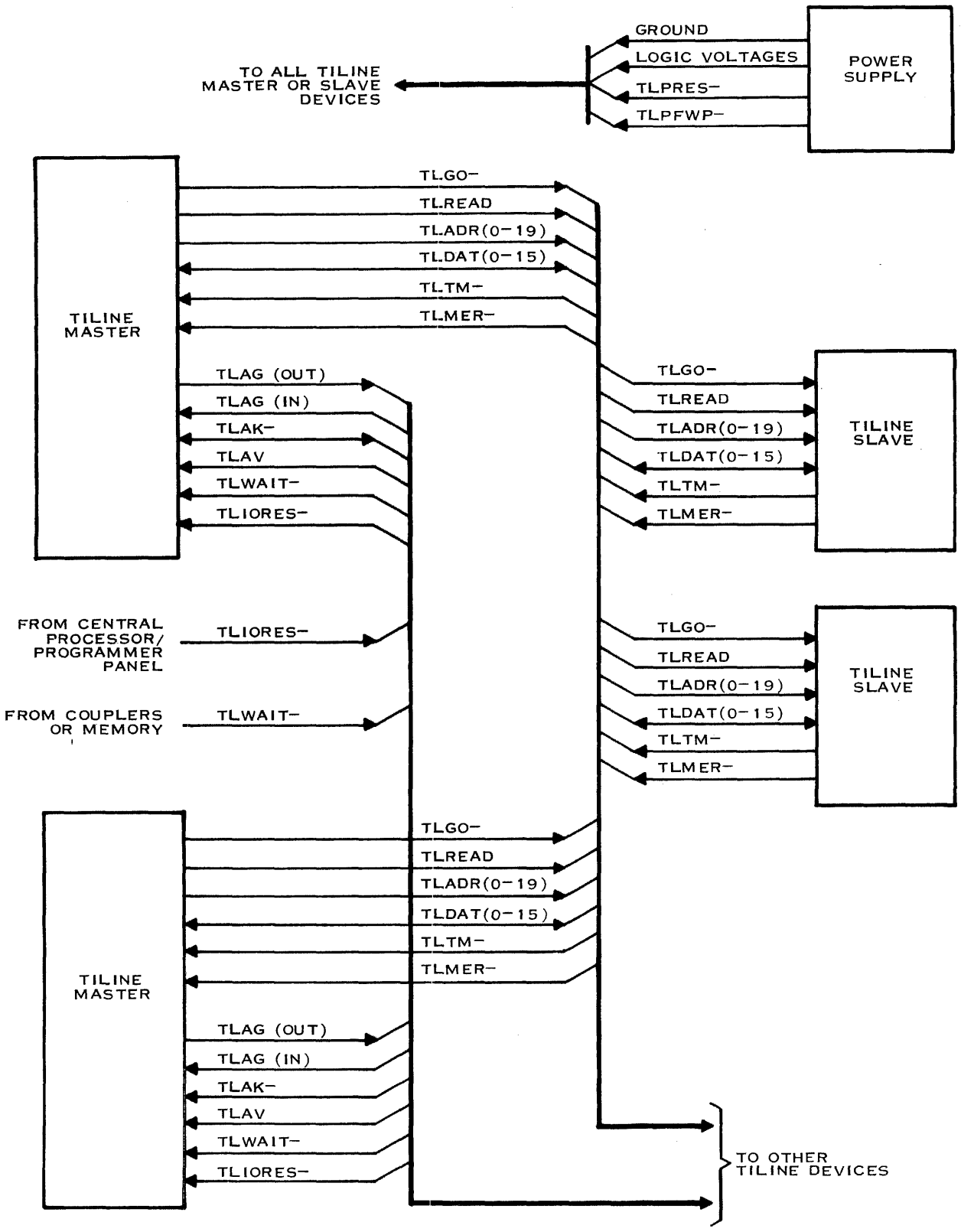

Figure 1-16. TILINE Interface Signals

Table 1-6. TILINE Signal Definitions

Signature	Pin Number	Definition
TLGO—	P1-25	TILINE Go: Initiates all data transfers when transition from high (3V) to low (1V) occurs.
TLREAD	P1-11	TILINE Read: When high (3V) it designates a read from slave operation; when low (1V) it designates a write to slave operation.
TLADR00—	P2-55	TILINE Address to define the location of data during a fetch or store operation. When high (≥2V), the corresponding address bit is 0; when low (≤0.8V), the corresponding address bit is 1.
01—	P2-44	
02—	P2-51	
03—	P2-53	
04—	P2-57	
05—	P2-59	
06—	P2-47	
07—	P2-49	
08—	P2-17	
09—	P2-19	
10—	P2-10	
11—	P2-12	
12—	P2-11	
13—	P2-15	
14—	P2-8	
15—	P2-9	
16—	P2-29	
17—	P2-27	
18—	P2-25	
TLADR19—	P2-31	
TLDAT00—	P2-67	TILINE Data: Bidirectional data lines that, when high (≥2V) represent zero data bits, and, when low (≤0.8V) represent one data bits.
01—	P2-69	
02—	P2-35	
03—	P2-37	
04—	P2-61	
05—	P2-63	
06—	P2-43	
07—	P2-45	
08—	P2-21	
09—	P2-33	
10—	P2-23	
11—	P2-20	
12—	P1-27	
13—	P1-28	
14—	P1-30	
TLDAT15—	P1-31	
TLTM—	P1-20	TILINE Terminate: When low (1V) indicates that the slave device has completed the requested operation.

Table 1-6. TILINE Signal Definitions (Continued)

Signature	Pin Number	Definition
TLMER—	P1-55	TILINE Memory Error: When low (≤0.8V), indicates that a nonrecoverable error has occurred during a memory read operation.
TLAG(in)	P2-6	TILINE Access Granted: When high (≥2V), indicates that no higher-priority device has requested use of the TILINE. When low (≤0.8V), prevents the receiving device from gaining access to the TILINE bus.
TLAG(out)	P2-5	TILINE Access Granted: When high (≥2V), indicates that neither the sending device nor any higher-priority device is requesting use of the TILINE bus. When low (≤0.8V), indicates that either the sending device or some higher-priority device is requesting use of the TILINE bus and prevents all lower-priority devices from gaining access to the bus.
TLAK—	P1-71	TILINE Acknowledge: When high (3V), indicates that no TILINE device was recognized as the next device to use the TILINE bus. When low (1V), indicates that some TILINE device has requested access, was recognized, and is waiting for the bus to become available.
TLAV	P1-58	TILINE Available: When high (3V), indicates that no TILINE device is using the bus. When low (1V), indicates that the TILINE bus is busy.
TLWAIT—	P1-63	TILINE Wait: A normally high (3V) signal that, when low (1V), temporarily suspends all TILINE master devices from using the TILINE bus. This signal is generated by bus couplers to allow them to use the bus as the highest-priority user.
TLIORES—	P1-14 P2-14	TILINE I/O Reset. A normally high (≥2V) signal that, when low (≤0.8V), halts and resets all TILINE I/O devices. This signal is a 100 to 500 ns pulse generated by the RESET switch on the programmer panel or by the execution of a RSET instruction in the AU.
TLPRES—	P1-13 P2-13	TILINE Power Reset: A normally high (≥2V) signal that goes low(≤0.8V) to reset all TILINE devices and inhibit critical lines to external equipment. The signal is generated by the power supply at least 10 μs before dc voltages begin to fail during power-down and until dc voltages are stable during power-up.

Table 1-6. TILINE Signal Definitions (Continued)

Signature	Pin Number	Definition
TLPFWP—	P1-16 P2-16	TILINE Power Failure Warning Pulse: A pulse that precedes TLRES— by 2 ms. When low (≤0.8V), indicates that a power-down sequence is in progress, allowing the AU to perform its power failure interrupt subroutine.
TLHOLD—	P2-26	TILINE Hold Signal: A normally high (3V) signal that goes low (1V) to assert that a CPU is executing an Absolute Value (ABS) instruction. TILINE Hold prevents interference from another processor on the TILINE bus while the first processor is performing the ABS instruction. This signal is used and propagated by TILINE COUPLERS in multiprocessor systems.
TLCACHEN	P1-73	TILINE Cache Enable Signal: The cache controller is enabled when this signal is high.

When a TILINE master device has access to the TILINE bus, it can accomplish a memory (slave) write cycle as follows:

1. The master asserts TILINE Go (TLGO—) and at the same time asserts the write command TILINE Read (TLREAD) by setting both signals low. The master simultaneously generates valid write data on the data bus (TLDAT—) and a valid 20-bit address (TLADR—) on the address lines.

2. All slave devices on the TILINE receive the TILINE Go transmitted by the master.

3. The slave devices decode the address to determine which slave is addressed.

4. The slave generates a delayed GO signal (using a timer circuit) and uses that signal to strobe for a valid address decode. In the case of a memory module, a delayed GO and a valid address decode generate a memory start signal. It is the responsibility of the slave device to delay GO for a time sufficient to accommodate the worst case address decode time and the worst case TILINE skew, with TILINE skew defined as 20 nanoseconds maximum.

5. When the slave device has delayed GO and decoded the address as valid, it performs the write cycle and then asserts the TILINE Terminate (TLTM—). At the time the slave device asserts TLTM—, it must be finished with the TLDAT—, TLADR, and TLREAD signals from the TILINE bus.

6. When the TILINE master receives the asserted TLTM—, it must release TLGO—, TLREAD, TLADR—, and TLDAT—. At this time, the master device can release the TILINE to another master device.

7. When the slave receives the release of TLGO—, it must release TLTM—.

8. When the master device receives the release of TLTM—, it can begin a new cycle if it has not relinquished the TILINE to another master device.

When a TILINE master device has access to the TILINE, it can accomplish a memory (slave) read cycle as follows:

1. The master asserts TLGO— and at the same time generates a valid address signal (TLADR—) and TLREAD signal. All slave devices on the TILINE bus receive the TILINE GO transmitted by the master.

2. The slave devices delay the GO signal and decode the address as is done for a write cycle. As in the write cycle, it is the responsibility of the slave device to delay GO for a time sufficient to accommodate the worst case TILINE skew (20 nanoseconds maximum) and the worst case address decode time.

3. When the address is decoded as valid, the slave device then generates read data. In the case of a memory module, this means starting a read cycle.

4. When read data is valid, and the slave device has finished using TLADR— and TLREAD, the slave device then applies TLTM—.

5. If a read error is detected during a read cycle, the READ ERROR (TLMER—) signal is asserted by the slave.

6. When the master device receives the asserted TLTM—, it must delay for at least worst case TILINE skew and then release TLGO— and TLADR— signal lines.

7. When the master device releases TLGO—, it must have finished using the TLDAT— and TLMER— signals. The TILINE master device can now relinquish the TILINE bus to another master device.

8. The slave device receives the released TLGO—, and must release the TLTM— and TLDAT— signals.

9. The master device receives the released TLTM— and can now begin a new cycle if it has not relinquished the TILINE to another master device.

Master Device TILINE Acquisition. The following three TILINE signals are used by master devices to schedule the next TILINE master during the last data transfer operation of the present TILINE master:

- TILINE Access Granted (TLAG)
- TILINE Acknowledge (TLAK—)
- TILINE Available (TLAV)

All TILINE master devices connect to the TILINE bus in a positional priority system; the TILINE device installed in the highest numbered chassis slot receives the highest priority. Priority ranking decreases with each chassis slot location towards the CPU, which has the priority. Figure 1-17 illustrates the connections between TILINE master devices that establish the priority system.

TILINE Special Purpose Functions. In addition to the TILINE signals associated with data transfers and those that establish priority for TILINE access, there are five special function signals. These signals are:

- TILINE I/O Reset (TLIORES—)
- TILINE Power Failure Warning Pulse (TLPFWP—)
- TILINE Power Reset (TLPRES—)
- TILINE Wait (TLWAIT—)
- TILINE Hold (TLHOLD—)

TLIORES— is generated by the CPU during execution of its I/O Reset instruction or in response to the programmer panel RESET switch. TLIORES— is a 100 to 500 nanosecond negative pulse on a normally high line. TLIORES— is also asserted whenever TLPRES— is asserted. TLPRES— is available to all devices connected to the TILINE bus. TLIORES— halts and resets all TILINE I/O devices. The devices should reset in an orderly fashion in response to TLIORES—, and any memory cycle in progress should be completed normally. For example, if a tape write is in progress, an end-of-record sequence should occur. When a device is reset while active, it must report abnormal completion status.

TLPFWP— is generated by the power supply to indicate that a power shutdown is imminent. The signal is a low pulse that occurs at least 2 milliseconds before TLPRES— occurs. The negative-going edge of this pulse causes the CPU to trap to the power failure trap location and the effect of the negative-going edge of TLPFWP— on connected TILINE I/O devices is the same as TLIORES—. TLPFWP— remains low until TLPRES— is asserted.

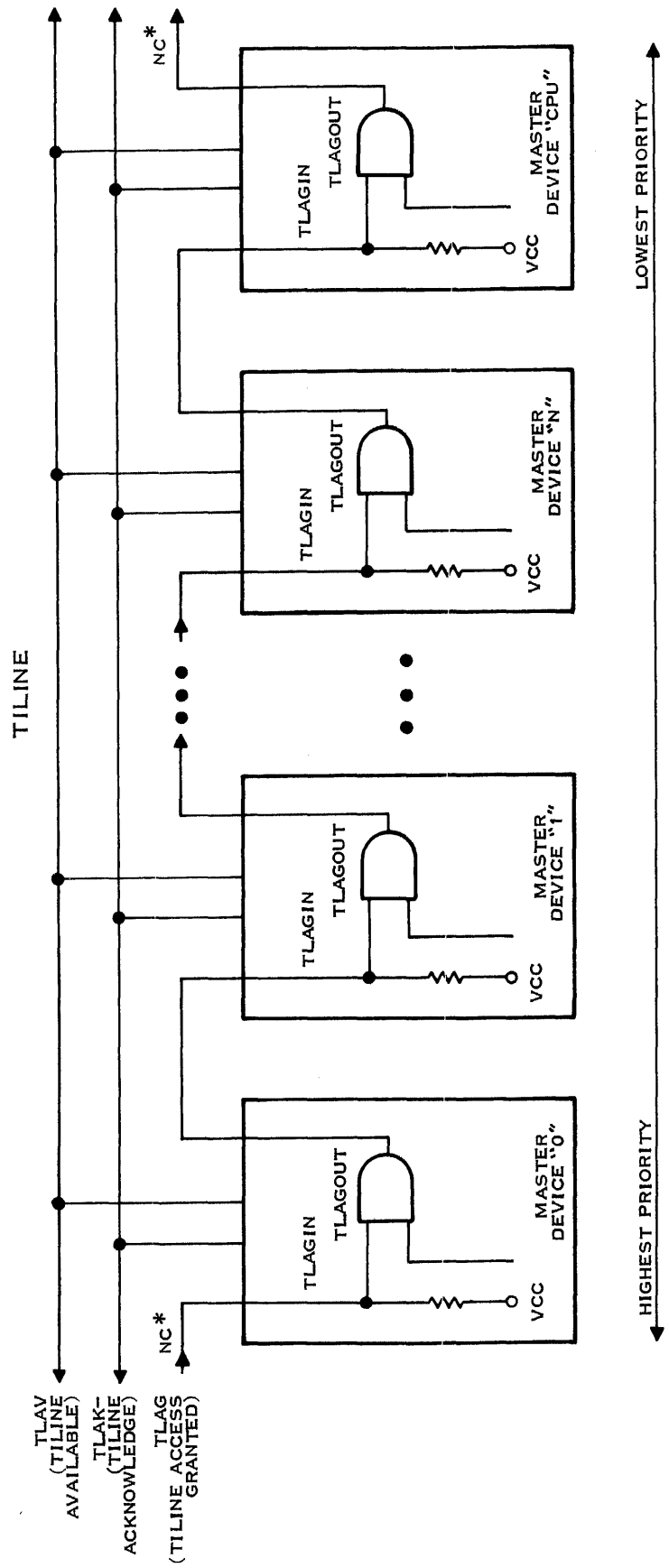

Figure 1-17. TILINE Master Devices Priority Interconnection

TLPRES— is a normally high signal that goes low at least 10 microseconds before any dc voltage level from the power supply begins to fail due to normal shutdown or ac power failure. TLPRES— is generated by the power supply. It remains low during and after a power failure. During ac power turn-on, TLPRES—remains at a low level until all dc voltages from the power supply are up and stable. The purpose of TLPRES— is to reset all device controllers and the CPU during power failure and to directly inhibit all critical lines to external equipment that are powered by a separate power supply. For example, it is TLPRES— that prevents a tape deck from getting a rewind pulse when the CPU is powered up and down. During the power-up sequence, the TLPRES— resets all I/O controllers to their idle state and clears any device status information. The CPU performs the power-up interrupt trap as the TLPRES— goes high (indicating that power is up and stable).

TLWAIT— is a normally high signal, generated by TILINE Couplers, that is used to resolve certain conflicts that can arise in computer-to-computer communication over the TILINE bus. The purpose of TLWAIT— is to directly disable (inhibit) the following signals from all TILINE master devices (including CPUs):

- TLGO
- TLREAD
- TLADR—
- TLDAT

Note that these signals are not inhibited in slave devices. The foregoing signals are disabled within 40 nanoseconds from the time TLWAIT— is asserted and remain disabled as long as TLWAIT— stays low. This action should not cause any state change in master devices and, except for its TILINE interface drivers, the master device should not be aware that TLWAIT— has been asserted. TLWAIT— prevents the master device from noticing any TLTM— or TLMER— signals that occur, and also holds the TILINE timeout timer reset of the master device. TLWAIT— allows the TILINE couplers to exercise a higher-than-any priority on the TILINE bus.

TLHOLD— is a normally high signal that is brought low by a CPU prior to the operand fetch of an ABS instruction. TLHOLD— remains low until the operand store cycle is complete or until the processor determines that the operand store is not needed. ABS is intended to be used as a software interlock. ABS reads a memory word, tests it, and then, if it is negative, subtracts it from zero and restores it to memory in its original location. In the use of ABS as a software interlock in the multiprocessor system, it is possible for one processor to modify a memory word while another processor is performing an ABS instruction on that word. This interference ruins the usefulness of ABS as a software interlock. TLHOLD— prevents this interference by holding TILINE access for the processor performing ABS. TLHOLD— is used and propagated by TILINE couplers in multiprocessor systems.

1.4.10.4 TILINE Access Controller. The TILINE access controller (TAC), a Texas Instruments SN58220, is a single-chip, bipolar integrated circuit device that is the interface between the SMI board and the TILINE bus for all TILINE signals used in bus acquisition and data transfer control. Each TILINE I/O signal can be connected from the TAC directly to the TILINE bus since the chip provides compatible driver/receiver circuits.

The TAC clock generator logic provides the capability for generation of n-phase clocks with an almost unlimited number of cycle times and duty cycles. The cycle time and duty cycle can be selected via two or more RC timing components connected externally to the chip. Additional phases of the clock can be achieved by providing external RC time delay logic in addition to the timer logic provided on the TAC chip. Generally, TILINE master devices operate as synchronous systems with a variable speed clock. During nonmemory cycles, the clock remains free-running and the master device operates as a fixed-frequency, synchronous system. During a memory cycle (MS2 going high), the clock is stopped until the addressed memory responds with a completion signal. The clock is then restarted and processing continues. Thus, the system operates synchronously with a variable speed clock. The TAC provides the capability of executing multiple memory cycles during a single bus acquisition cycle. This is useful for test and set operations necessary either for multiprocessor systems that share resources, or for peripheral controllers that require burst data transfers to achieve a high throughput rate. Table 1-7 shows the pin-out and signal definitions for the 28-pin TAC.

Table 1-7. TILINE Access Controller Signal Definitions

Signature	Pin Number	Input/ Output*	Definition
TLAK—	2	I/O	These signals are defined in Table 1-6.
TLAG (in)	4	I	
TLAG (out)	5	O	
TLPRES—	9	I	
TLAV	11	I/O	
TLREAD	17	O	
TLWAIT—	13	I	
TLTM—	15	I/O	
TLGO—	20	I/O	
RC4IN	1	I	The RC network connected to this input controls the deskewing time for TLAG signals.
RC4OUT	3	O	Permits additional circuits for deskewing of TLAG signals. Not used by the 990/12 LR.
CLK	7	I	Positive-edge triggered. Usually tied to MDTR or the last clock edge that completes a memory or device access cycle.
LCYC—	8	I	An active (low) signal that releases the TILINE on the rising edge of the CLK signal.
TOE—	10	O	An active (low) signal that occurs when the TILINE access controller does not receive a TLTM— signal after a fixed period of time from the start of a bus transfer. The time period is controlled by the RC network attached to the RC3 pin of the TILINE access controller (pin MS1 equals 1).

Note:

* I/O refers to the TILINE access controller.

Table 1-7. TILINE Access Controller Signal Definitions (Continued)

Signature	Pin Number	Input/ Output*	Definition
RC3	12	I	The RC network connected to RC3 controls the time between TILINE access and the generation of a TOE— signal.
READ	16	I	A high input for a read operation, a low input for a write operation. READ is buffered and enabled during TILINE access as TLREAD.
GND	14	I/O	Provides board ground to the TILINE access controller chip.
WDE—	19	O	An active (low) signal that enables data onto the TILINE data bus during a write operation.
ABE—	18	O	An active (low) signal that enables the address onto the TILINE bus.
MS1	21	I	An active (high) input that causes the assertion of TLGO— and ABE—, and enables, when applicable, TLREAD and WDE—, when bus access has been granted and when TLGO— and TLTM— are both high.
RC2	22	I	The RC network connected to this pin determines the length of time that signal MDTR remains low.
MDTR	25	O	System clock output. This signal can be stopped only when it is in the low state.
MS2	23	I	A high at MS2 enables MDTR to clock when MS1 is high and with signals TLGO— and TLTM— going to an inactive state followed by TLTM— return to an active state. At this point, the state of TLGO— is not important. A low MS2 input always allows MDTR to clock. The typical memory state is with both MS1 and MS2 high.
END—	24	I	For two-phase clock generation, END— is tied to pin 27, T1C. For multiple-phase generation, other RC timers can be inserted between END— and T1C.

Note:

* I/O refers to the TILINE access controller.

Table 1-7. TILINE Access Controller Signal Definitions (Continued)

Signature	Pin Number	Input/ Output*	Definition
RC1	26	I	The RC network connected to RC1 controls the high time of MDTR.
T1C	27	O	Controls the high time of MDTR when connected to END—.
Vcc	28	I	Applies board voltage to the TILINE access controller.

Note:

* I/O refers to the TILINE access controller.

1.4.11 Memory Mapping

Memory mapping expands the inherent addressing capability of the 990/12 LR processor from 64K bytes to 2048K bytes. The addressing expansion is accomplished by relocating the address generated by the processor within blocks of memory defined by preloaded displacement values. The mapping logic (or map file) consists of four sets of mapping registers, map 0, map 1, map 2, and map 3. Maps 0, 1, and 2 are for use by the operating system, user programs, and long-distance instructions, respectively. Map 3 is used in certain instructions as an alternative map file. It cannot be specified in the user's code and can only be selected by the microcode. Figure 1-18 illustrates the data, address and control paths within the mapping circuits. For more information, refer to the *990/12 LR Computer, General Description.*

1.4.11.1 Address Development. Figure 1-19 illustrates how a 20-bit mapped address is created from a 15-bit address. During a normal memory access, whether for a read or for a write operation, the four least significant bits of the incoming address are transferred without change as the least significant bits of the mapped address. The 11 most significant bits of the incoming address are added to the 11 least significant bits of the base address, with any resulting carry propagated up through the remaining bits of the base address register. The result of the addition is used as the 16 most significant bits of the mapped address to complete the 20-bit address.

An alternate method of mapping the least significant bits of the address is used during a workspace cache demand-fill microcycle. A workspace cache demand-fill microcycle occurs when a workspace register is addressed that has not previously had its contents loaded into the workspace cache on the AU board. During workspace cache demand-fill microcycles, the signal that contains the workspace register number and addresses the workspace cache on the AU board is enabled to the LSB adder on the SMI board to provide the least significant bits of the mapped address.

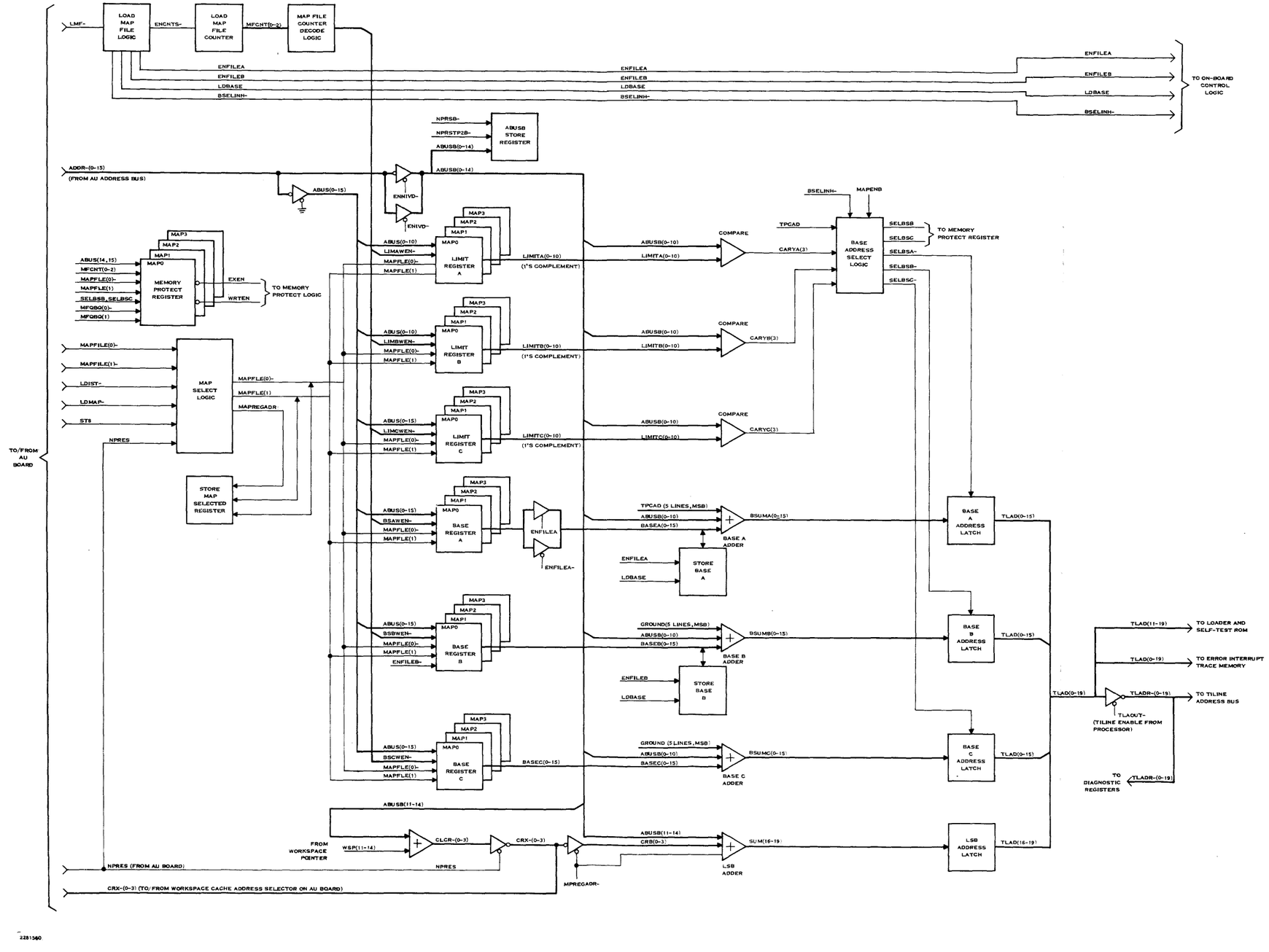

Figure 1-18. Memory Mapping Block Diagram

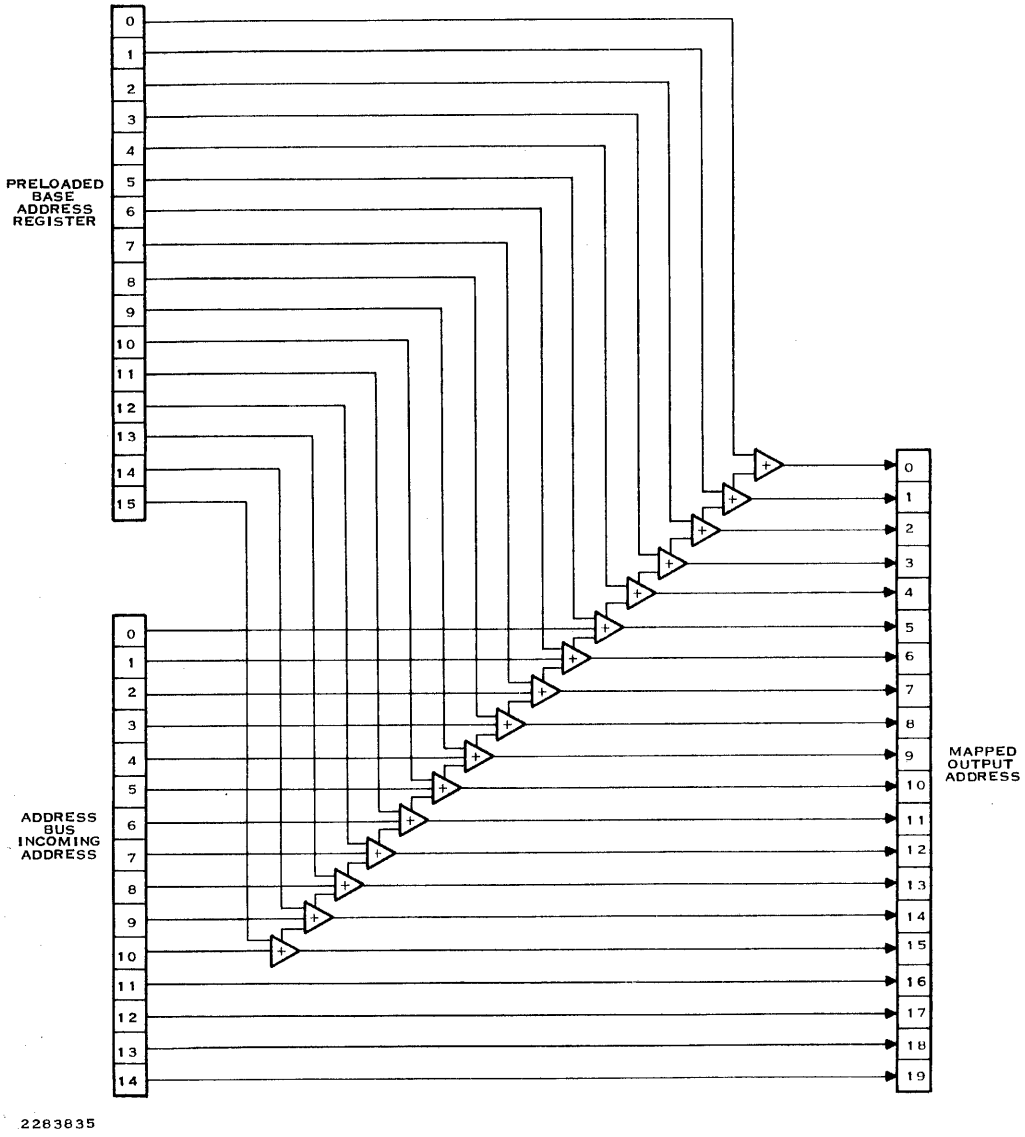

Figure 1-19. Mapped Address Development

1.4.11.2 Base Register Selection. The mapping circuits must decide which base register to use for a particular operation since there are three base registers that can be used for address development in each set of map registers. To make this selection, the incoming address is compared to the three separate values contained in limit registers A, B, and C for the selected map set. These limit registers contain the one's complement value of an upper-bound address for specified ranges of incoming addresses. Adding each of these complement values to the incoming address (binary subtraction of the true limit values) and then monitoring the carry-out bit from each addition determines the range that contains the incoming address value. If any of the additions do not produce a carry-out, the incoming address is less than the true value of the corresponding limit register. The three carry-out bits are examined by base register select logic to eliminate coincident conditions. For example, if the incoming address is less than the limit register A value, it will also be less than the values in limit registers B and C. The base register select logic recognizes only the lowest limit register and generates an enabling signal to select the base register addition process that corresponds to the recognized limit register.

The address development and the limit comparison processes occur simultaneously for each of the base registers and the limit registers. The output of the limit comparison selects the result of one of the address development processes, rather than enabling the process itself. This construction greatly increases the speed of the mapping process to provide a mapped address as soon as the comparison is complete.

1.4.11.3 Map Selection. The map file logic contains four sets of map registers that are used for the following functions:

- Map 0 — Reserved for use by the operating system so that its area of memory can be segregated from the area of memory used by programs running in the system.
- Map 1 — Used by programs running under the operating system.
- Map 2 — Used by the long-distance instructions exclusively and cannot be accessed with any other instructions.
- Map 3 — Used in certain new instructions as an alternative map file. Map 3 cannot be specified in the user's code but can be selected by the microcode.

During a map loading operation, two signals from the AU circuit board, MAPFILE(0)— and MAPFILE(1)—, select the map to be used. Applied to the map select logic, MAPFILE(0)— and MAPFILE(1)— generate map select signals MAPFLE(0)— and MAPFLE(1)—. MAPFLE(0)— and MAPFLE(1)— in turn generate binary signals 00 through 11 to address the four map files of each of the three limit registers and each of the three base registers. MAPFLE(0)— and MAPFLE(1)— also address the four map files of the memory protect register. The memory protect register is an extension of the limit registers and stores memory protect information contained in bits 14 and 15 of each of the three parameter words used to address the limit registers.

During regular use of the map file (when not loading), an active (low) LDMAP— signal is provided by the AU board and map files 0, 1, and 3 are selected by signals MAPFILE(0)— and MAPFILE(1)— in the manner used during a map loading operation. In response to either of the long-distance instructions (LDD and LDS), the AU board provides an active LDIST— signal that is applied to map select logic on the SMI board. LDIST— forces selection of map file 2.

A workspace cache is located on the AU board where data accessed as workspace registers is stored as it is fetched from memory. Subsequent accesses to the same data are from the on-board cache, eliminating the need for a memory cycle. However, when the workspace register has not been previously accessed, a demand-fill memory cycle is required. The AU board generates an active NPRES signal to indicate the demand-fill requirement.

1.4.11.4 Map File Loading. During a load map file operation, the AU board activates the LMF— interface signal to indicate that a load operation is in progress. Simultaneously, an address is placed on the address bus from the AU board. This address indicates the starting address of six contiguous words in memory that contain the map file parameters to be loaded. After passing through the mapping circuits, the address is directed to memory to fetch the first parameter word. The active LMF— signal applied to map select logic develops the base select inhibit signal BSELINH—. BSELINH— inhibits further clocking of the base address select register so that the presently selected base address latch remains selected for the remainder of the load map file operation. Also developed from map select logic, are signals that disable the outputs of base registers A and B to their respective adders while enabling the store base A and store base B registers which save the A and B base addresses for mapping during the load map file operation. Base register C is not disabled, and base C address is not saved since the value in base register C is not changed until after receipt of the sixth and final parameter word from memory, at which time the value is no longer required.

The load map file logic provides a counter enable signal to the load map file counter. The counter increments with each succeeding clock pulse. The initial output of the counter is decoded by the map file counter decode logic and generates an enabling signal to transfer the first parameter from memory into limit register A. Subsequent memory cycles increment the counter so that incoming data is distributed to registers in the selected map file in the following parameter word order:

1. Limit register A, enabling signal LIMAWEN—
2. Base register A, enabling signal BSAWEN—
3. Limit register B, enabling signal LIMBWEN—
4. Base register B, enabling signal BSBWEN—
5. Limit register C, enabling signal LIMCWEN—
6. Base register C, enabling signal BSCWEN—

Additionally, bits 14 and 15 of parameter words 1, 3, and 5 contain memory protect information that is stored in the memory protect register and retrieved when the appropriate base register and map file are selected. Because of the sequence used in accessing the mapping parameters and the manner in which the data is loaded into the map file registers, the data must be formatted correctly in memory before the load operation begins. Figure 1-20 illustrates the proper format for all of the parameters. All parameters must be in contiguous memory locations in the order in which they will be loaded. Also, the values must be left-justified within the memory word since bits 11, 12, and 13 are ignored when loading the limit registers and the memory protect register.

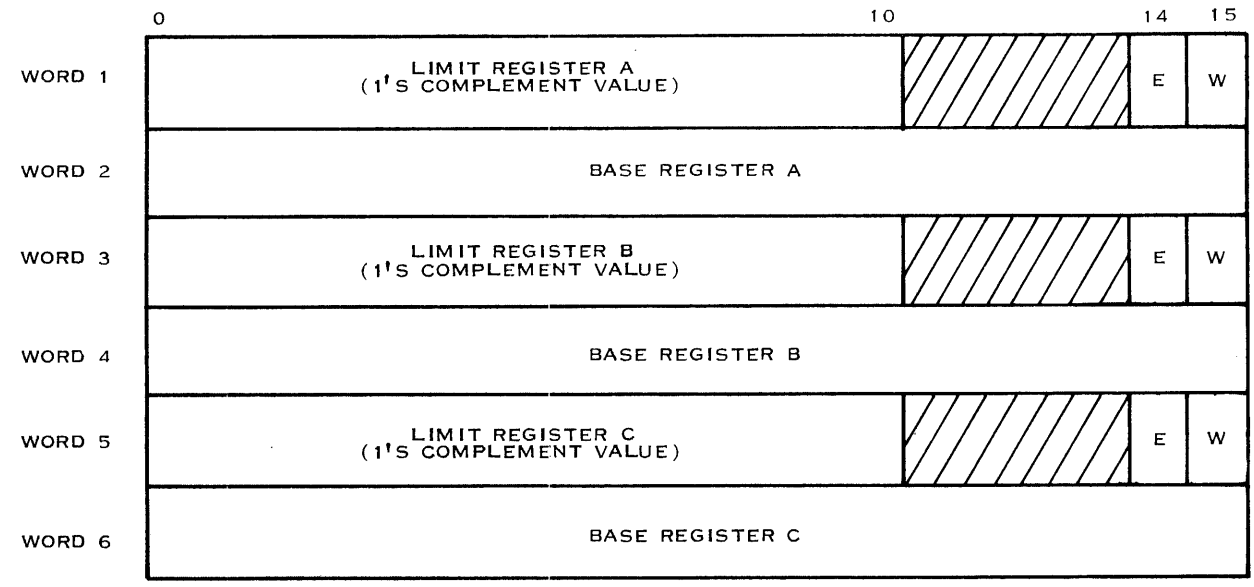

Figure 1-20. Memory Format of Mapping Parameters

1.4.11.5 Memory Management and Protection. Memory protect information contained in bits 14 and 15 of the three parameter words that address the limit registers during a map loading operation is stored in the addressed map file of the memory protect register. Signals EXEN and WRTEN are developed at the output of the memory protect register and correspond to the complement of bits 14 and 15 respectively, of the limit registers' parameter words. The decoded functions are shown in Table 1-8.

Table 1-8. Memory Protect Decode of Limit Register Parameter Words

Mapping Limit Register Bits		Memory Cycles Permitted in Segment
14 (E)	15 (W)	
0	0	Read, Write, Execute
0	1	Read, Execute
1	0	Read, Write
1	1	Read only

Memory management and protection is invoked for predetermined mapped memory addresses by setting bit 9 in the status register. Invoking memory protection and management provides an alternate means of generating the TILINE write enable signal to prohibit execute and write operations to segments of protected memory. Segments of memory protected from write operations and predetermined from the stored status of bits 14 and 15 of the three parameter words, are loaded into the limit registers during the map loading operations. When a level 2 error interrupt occurs, writes into memory and the workspace cache are inhibited until the interrupts are tested.

TILINE peripheral control space (TPCS) addresses are excluded from memory protection. Attempts to write to or execute in protected memory generate write violation signals. These signals provide inputs generated as level two interrupts to the error interrupt trace memory and to the system error interrupt status register.

1.4.11.6 TILINE Peripheral Control Space (TPCS) Mapping. The TPCS is a range of TILINE addresses reserved for assignment to peripheral device controllers. The address range is 512 words. This 512 word range of addresses extends from TILINE word addresses > FFC00 through > FFDFF. The processor maps CPU addresses > F800 through > FBFF to the TPCS. Map file 0 invokes this particular mapping when ST bit 8 equals 0, or when the CPU is in the unmapped mode.

The mapping circuits develop TPCS addresses by monitoring the six most significant bits of the incoming address. If the five most significant bits are set, and the sixth most significant bit is clear (CPU address is > F800 or greater but less than > FC00), ST bit 8 is clear (using map 0), and no long distance instruction is being executed (not using map 2), then the mapping circuits will pass the incoming address bits as the least significant 15 bits of the output TILINE address. To complete the TILINE address, the mapping circuits insert five ones as the five most significant bits of the TILINE word address. For more information, refer to the *990/12 LR Computer, General Description*.

2

Maintenance

2.1 INTRODUCTION

This section provides depot-level maintenance procedures for the 990/12 LR CPU. A special test system, the 990/12 LR Functional Verification System (FVS) is used in the testing of the CPU boards. Operating instructions are provided in this section for testing the boards using the FVS. The FVS is used for the following:

- To verify board failures
- To isolate failures to a replaceable component
- To verify that a board failure has been repaired thus assuring that a board is ready for return to service.

2.2 DESCRIPTION OF THE FVS

The FVS as shown in Figure 2-1 is housed in a double-bay equipment desk and a single-bay pedestal with some of the major units of the FVS positioned on the desk tabletop or pedestal tabletop. Major units of the FVS consist of the following:

- The desk assembly
- A Model 911 Video Display Terminal (VDT)
- A Model 990 Maintenance Unit Programmer Panel
- A Model 743 Keyboard Send-Receive (KSR) Data Terminal
- A Model 810 Printer
- A pedestal assembly

The desk assembly consists of the following:

- A DS10 disk drive
- A 13-slot chassis that contains a 990/10 host computer with 352K bytes of memory.
- The peripheral device controller boards to interface with the rest of the FVS.
- A modified 3-slot original equipment manufacturer (OEM) chassis that contains the device controllers for a DS10 disk drive and a 743 KSR data terminal.
- A 3-slot OEM chassis that contains the state controller board that is connected to the AU/SMI vacuum chamber assembly.

The AU/SMI vacuum chamber assembly, located on the desk assembly tabletop, is the interface to the CPU boards under test. Two Lambda power supplies are provided as part of the desk assembly. One powers the AU/SMI vacuum chamber assembly and the other provides power for the two OEM chassis. The pedestal assembly contains a DS10 disk drive and an FD800 floppy disk.

Figure 2-2 is a block diagram of the FVS that shows the host computer, other major units of the FVS, and the interface connections between them.

2.3 FVS OPERATIONAL CHARACTERISTICS

The following operational description of the FVS is keyed to Figure 2-2. A 990/10 host computer communicates with a 990/12 LR CPU through the state controller board (SCB). The board under test is one of the two boards of the 990/12 LR CPU. To facilitate testing, the 990/12 LR computer requires two types of communications:

- Downloads of object code or microcode
- Commands to control the 990/12 LR from the FVS

The 990/10 computer and the 990/12 LR computer share memory that is located in the 990/10 chassis. The 990/12 LR accesses memory through the TILINE coupler but cannot access the first 32K bytes since the diagnostic software is hardware-protected from the unit under test to prevent the control software from being destroyed as the diagnostic test proceeds. The SCB functions as a CRU device and is connected to the unit under test fixture with ribbon cables.

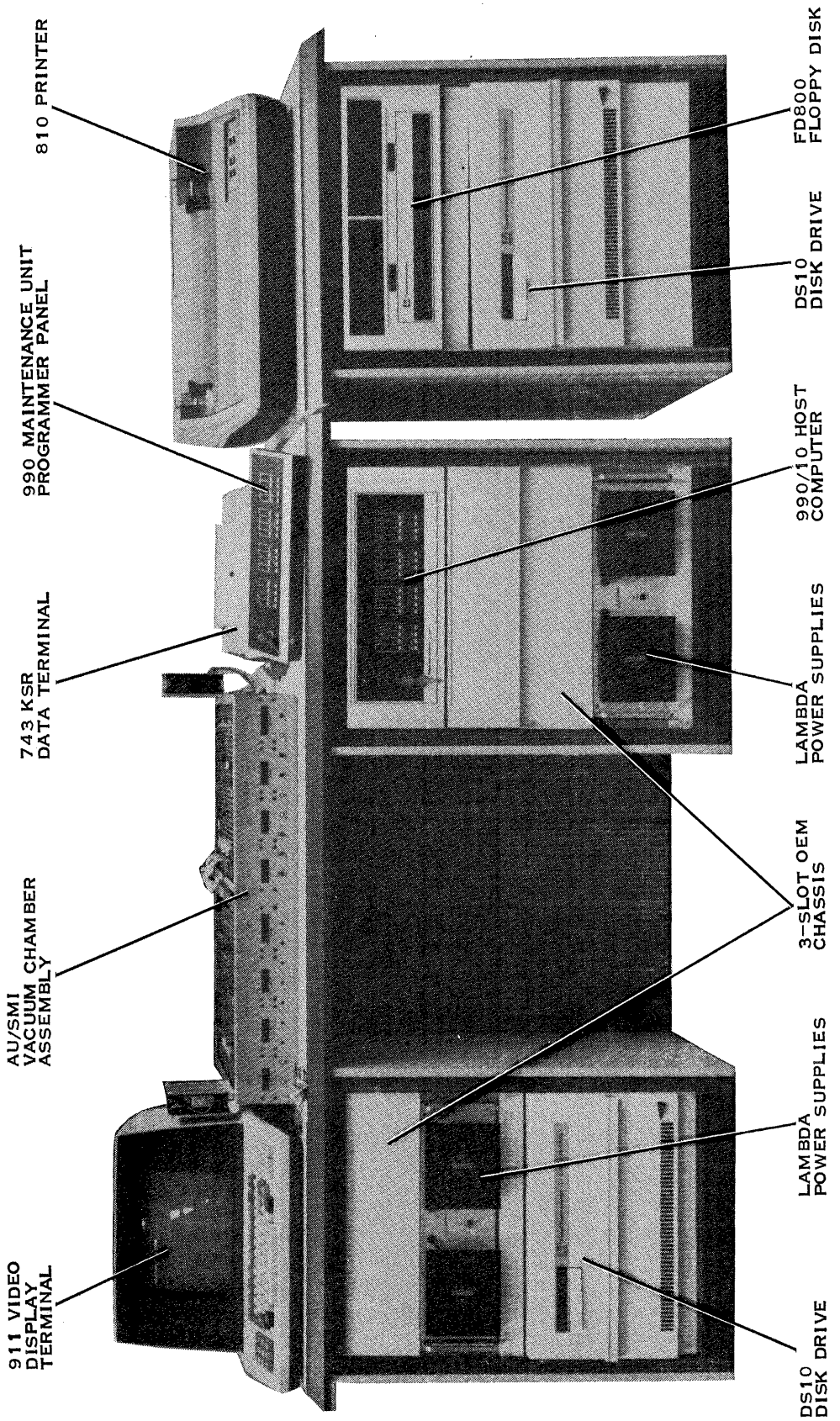

Figure 2-1. 990/12 LR Functional Verification System

Object code downloads cause assembly language programs to be loaded into the 990/12 LR computer's memory for execution by the 990/12 LR computer. Microcode downloads cause microcode to be loaded into 2K by 64-bit section of RAM on the SCB. The 990/12 LR can be forced to execute microcode either from its own microcode ROMs or from RAM on the SCB. Since the SCB RAM can hold the instruction set microcode, microcode diagnostics, or any other microcode for execution by the 990/12 LR; microcode changes are easily facilitated by the FVS. The SCB has several features in addition to the RAM just discussed. One feature is a breakpoint register that permits the FVS to breakpoint the 990/12 LR on a selected microcode instruction. Another feature is the trace memory that records results of the last 64 microcode instructions executed by the 990/12 LR. The FVS can also control the clock of the 990/12 LR through the SCB, permitting activation of a selected number of clocks including single instruction execution (SIE). The FVS communicates to the SCB and to the 990/12 LR through the various CRU bits of two control words. Some CRU bits are used to enable functions, some are used to select multiplexer inputs, and some must be toggled to perform certain functions. Each CRU bit corresponds to a signal path on the SCB. The CRU bits are listed and described in the program description for the *Diagnostic Overlay Guidance System*, part number 2268200-9901. Almost all of the CRU bits are looped back, that is, they can be read back from the SCB and can then be tested for a certain value. A map of the CRU bits is contained in the listing for the test module Driver and Interrupt Handler (DRVINT), part number 2268203-9901. The 990/12 LR is controlled by setting and resetting the proper CRU bits at the appropriate time. Examples of this are contained in the software routines, especially in the STMON subroutine calls, in the test module DRVINT. These subroutines perform the following functions:

- Starting and halting the unit under test clock
- Reading/writing to RAM
- Enabling interrupts
- Reading trace memory
- Reading microprogram counters
- Setting and clearing a breakpoint

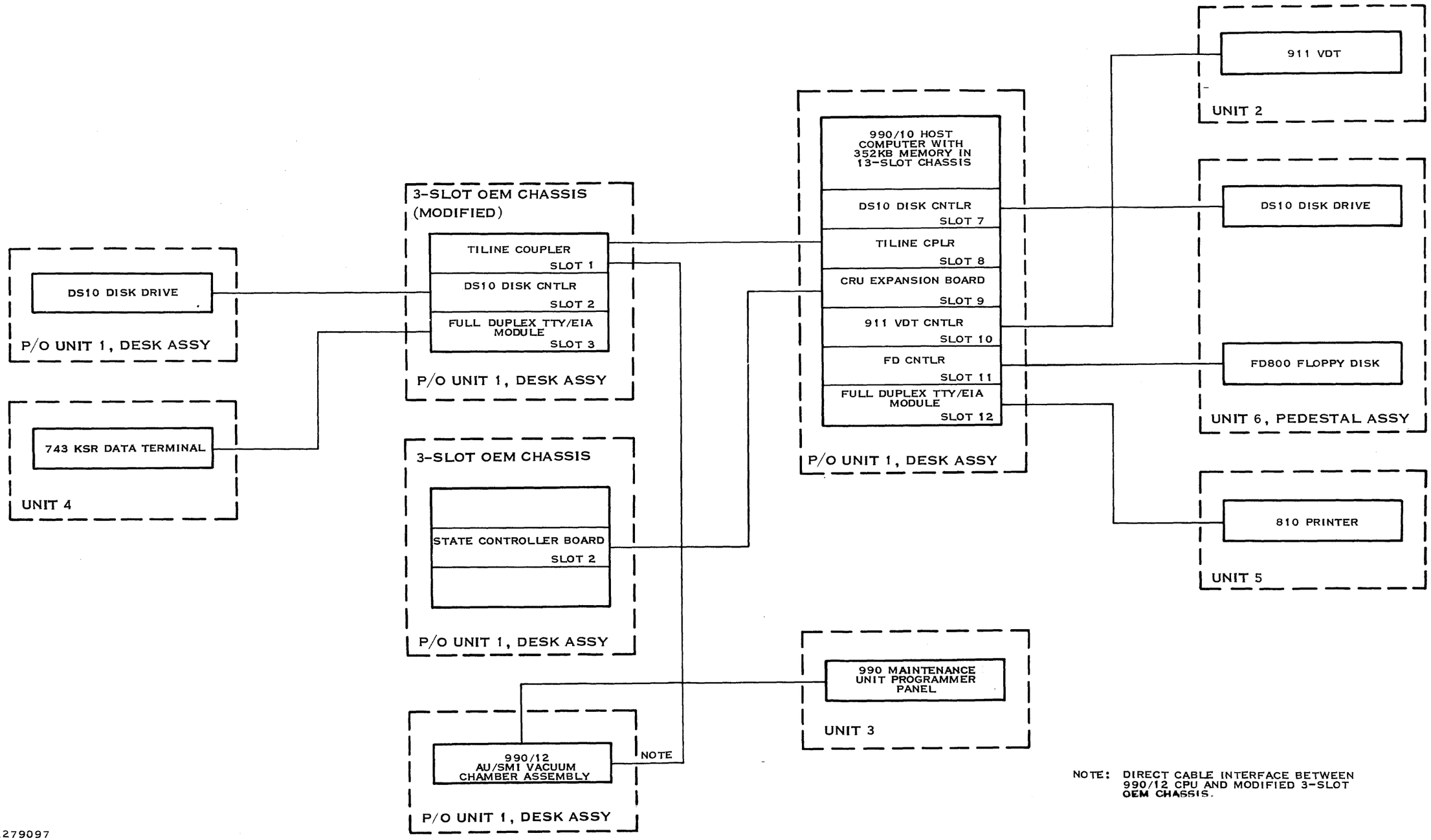

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Figure 2-2. Functional Verification System Block Diagram

2.4 DIAGNOSTIC OVERLAY GUIDANCE SYSTEM SOFTWARE DESCRIPTION

The Diagnostic Overlay Guidance System (DOGS) runs under the DOCS operating system and executes in the control central processor. DOCS is described in the *Model 990 Computer Diagnostics Handbook*, part number 945400-9701. The Batch Command Stream (BCS) feature of DOCS allows execution of a file of verbs that can be used to perform all functions needed to complete part of a 990/12 LR test. In addition to DOCS, DOGS contains the following modules:

- Display and Test Initialization (DISPLAY), which contains test initialization and the IDLE verb.
- Special Verbs Module (SPECVERB), which contains code for verbs to download to RAM, download to 990/12 LR memory, reset, clock control, and many other verbs peculiar to the 990/12 or the SCB.
- Driver and Interrupt Handler for SCB (DRVINT) which contains the driver for STMON subroutine calls. These calls are made by the verbs to perform certain functions such as:
  - — Start/stop/test unit under test clock
  - — Set/clear breakpoints
  - — Read/write RAM
  - — Read trace memory
- Each STMON subroutine is identified by a number between 1 and 23 that is included in the call list of parameters.
- PDT Monitor and Microcode Monitor (MONITORS), which contains Program Demonstration Test Monitor for use with burn-in DOCS and also has micromonitor for timing of microcode diagnostics (overlays).
- Modified Loaders (DLOADER 1, DLOADER 2), which contains disk loader used by both DOCS and DOGS for downloads.
- Trace and Modify Registers (TRCREG), which contains code to read/write the unit under test registers, code to trace microcode, and code to compare RAM with ROM.
- Microcode Module for TRCREG (refer to number 6) (RWMIC), which contains module of microcode generated by OBJ990 for read/write of 990/12 LR registers.

2.5 CPU CHECKOUT PROCEDURES

This paragraph contains procedures for initial turn-on and operation of the FVS. Figure 2-3 and Table 2-1 provide the locations and functions of the displays and indicators of the FVS vacuum chamber assembly. Figure 2-4 and Table 2-2 provide the locations and functions of the controls and test points on the right side panel of the vacuum chamber assembly. Figure 2-5 and Table 2-3 provide the locations and functions of the controls and test points on the left side panel of the vacuum chamber assembly. Procedures for diagnostic testing of the suspected faulty AU or SMI board using the FVS are also provided in this paragraph. The diagnostic tests will run to completion or until an error is encountered. When an error occurs in diagnostic testing, refer to the troubleshooting procedures of paragraph 2.6 as an aid in isolating a fault to a replaceable component.

Table 2-1. FVS Vacuum Chamber Displays and Indicators

Display/Indicator	Function
OVERLAY NO	Provides hexadecimal display of the overlay number presently active when running diagnostic overlays. This is a copy of microcode scratch register 0.
TEST NO	Provides hexadecimal display of the test number of the overlay presently active in diagnostic testing. This is valid as a test number only when running overlays; otherwise, it is a copy of microcode scratch register 1.
ABUS 1	Provides hexadecimal display of the data on AU board A bus during phase 1 of the clock.
ABUS 2	Provides hexadecimal display of the data on AU board A bus during phase 2 of the clock.
INT(Display)	Provides hexadecimal display of currently active interrupt level, 0 to 15. Default or no interrupt equals 7.
UPC	Provides hexadecimal display of the current microprogram counter.
IR	Provides hexadecimal display of the current assembly language instruction residing in the instruction register.
ADDR BUS	Provides hexadecimal display of value contained in address bus provided to the SMI board by the AU board.
MAP BUS	Provides hexadecimal display of value contained in the mapped address provided to the TILINE by the SMI board.
VACUUM	Applies vacuum to the vacuum chamber assembly

Table 2-1. FVS Vacuum Chamber Displays and Indicators (Continued)

Display/Indicator	Function
FAN	Applies power to cooling fan mounted on AU board side of vacuum chamber assembly. The two fans for the vacuum chamber assembly are electrically interlocked so that both fans cannot be turned off at the same time. Normal mode of operation is for both fans to be running to adequately cool the mounted boards. If a failure occurs whereby neither fan runs, the mounted boards will overheat and may be destroyed.
CLK	When lighted, this indicates that the 990/12 LR unit under test system clock is running; when not lighted, the clock is off.
ROM	When lighted, this indicates that the 990/12 LR unit under test is using on-board instruction ROM. When not lighted, it is using the state controller RAM for instructions or diagnostic overlay code.
Φ1, Φ2 TRACE switch	Used to select phase 1 or phase 2 of the clock.
Φ1	When lighted, this indicates that Φ1 was selected.
TILINE HOLD	When lighted, this indicates that the TILINE signal TLHOLD— is active.
TILINE WAIT	When lighted, this indicates that the TILINE signal TLWAIT— is active.
TILINE GO	When lighted, this indicates that the TILINE signal TLGO— is active.
MAPEN	When lighted, this indicates that the SMI board is enabled for mapping.
INT(Indicator)	Lights to indicate that an interrupt has occurred.
L2INT	Lights to indicate that a system error level two interrupt has occurred. The INT indicator will also light.
BRKPT	Lights to indicate that a breakpoint interrupt has occurred.
MAPFL1, MAPFL2	Indicates the status of the control code signals generated by the processor as binary map file select signals. This is a binary representation of the map file that is currently enabled (map 0, map 1, map 2, or map 3).
FAN	Applies power to the cooling fan mounted on SMI board side of vacuum chamber assembly.
POWER	Applies power to the vacuum chamber assembly.

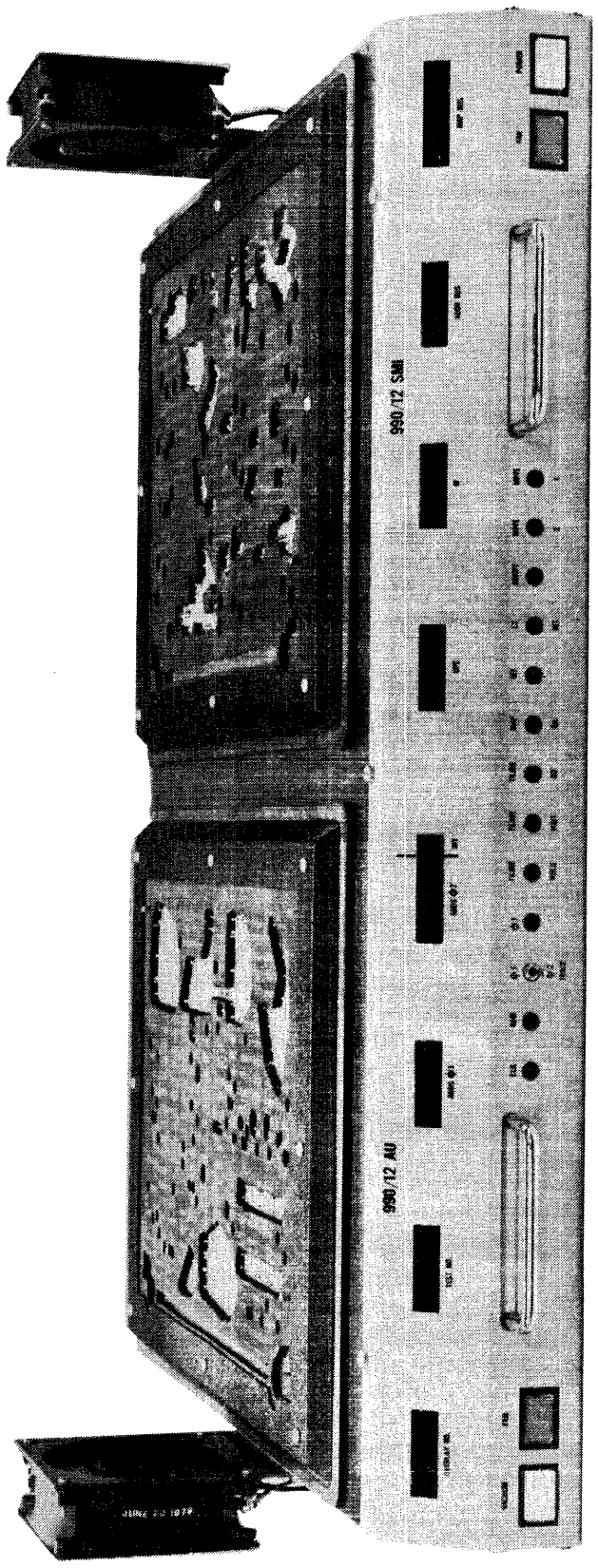

Figure 2-3. FVS Vacuum Chamber Assembly Displays and Indicators

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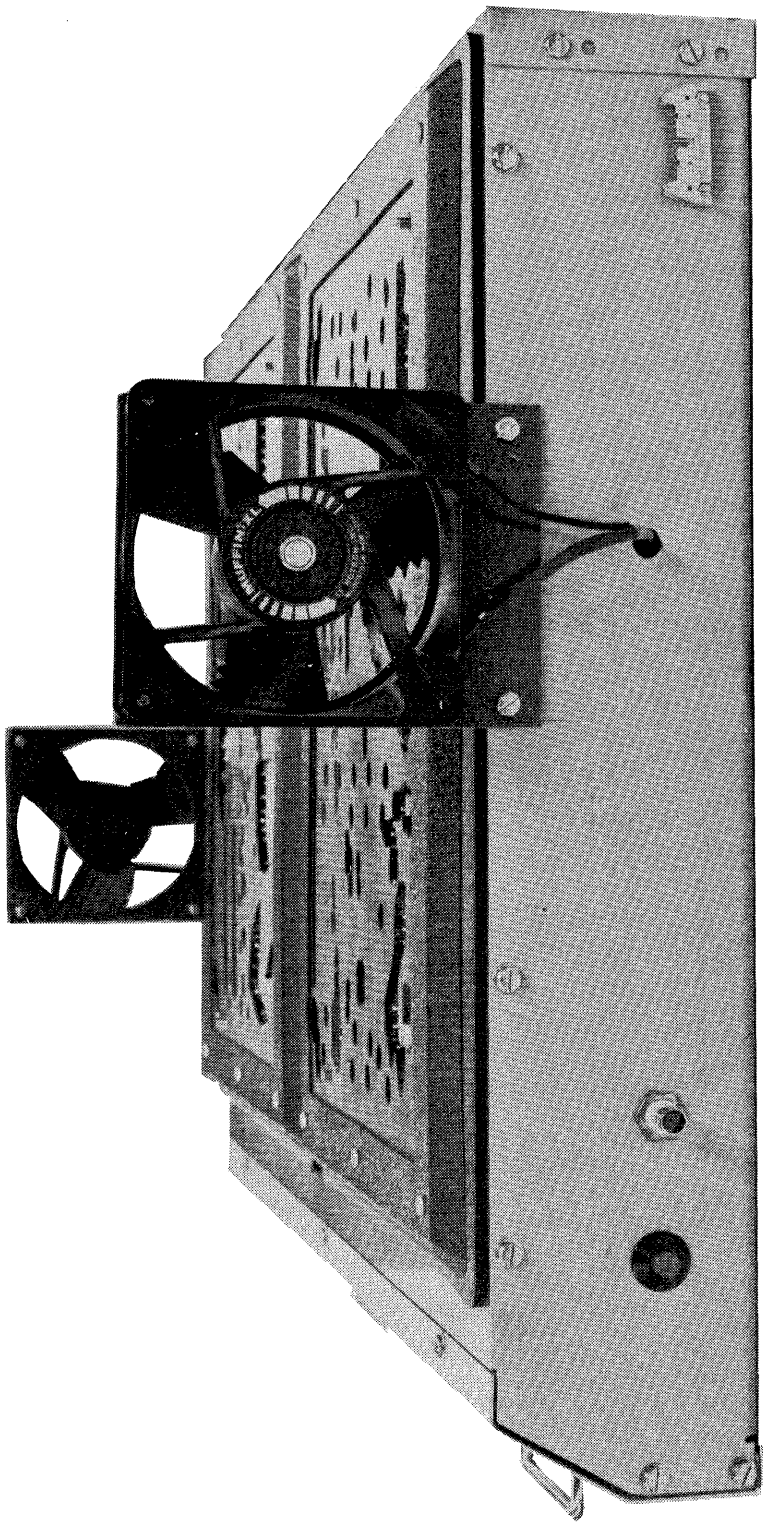

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Figure 2-4. FVS Vacuum Chamber Assembly Controls and Test Points, Right Side Panel

Table 2-2. FVS Vacuum Chamber Assembly Controls and Test Points, Right Side Panel

Control/Test Point	Function
TILINE RESET switch	Applies TILINE reset signal to CPU boards mounted on the vacuum chamber assembly.
SCOPE SYNC input jack	Provides the operator software-set soft breakpoint for use as oscilloscope synchronization signal.
FRONT PANEL connector	Provides connecting point for maintenance unit programmer panel to 990/12 LR CPU mounted in the vacuum chamber assembly.

Table 2-3. FVS Vacuum Chamber Assembly Controls and Test Points, Left Side Panel

Control/Test Point	Function
TRACE PROBE clip-on probes	Consists of 17 clip-on test probes that are connected by ribbon cable, as an input to the SCB board. The test probes permit the operator to select up to 16 test points on the board under test. The test points are monitored by software. The operator can use the DT verb to call these test points up for display on the video display terminal. The test points are listed as UNKNOWN on the display. The 17th test probe provides an optional hardware breakpoint enable. The breakpoint is active (stop) when low, and is enabled with the FE verb and disabled with the FD verb.

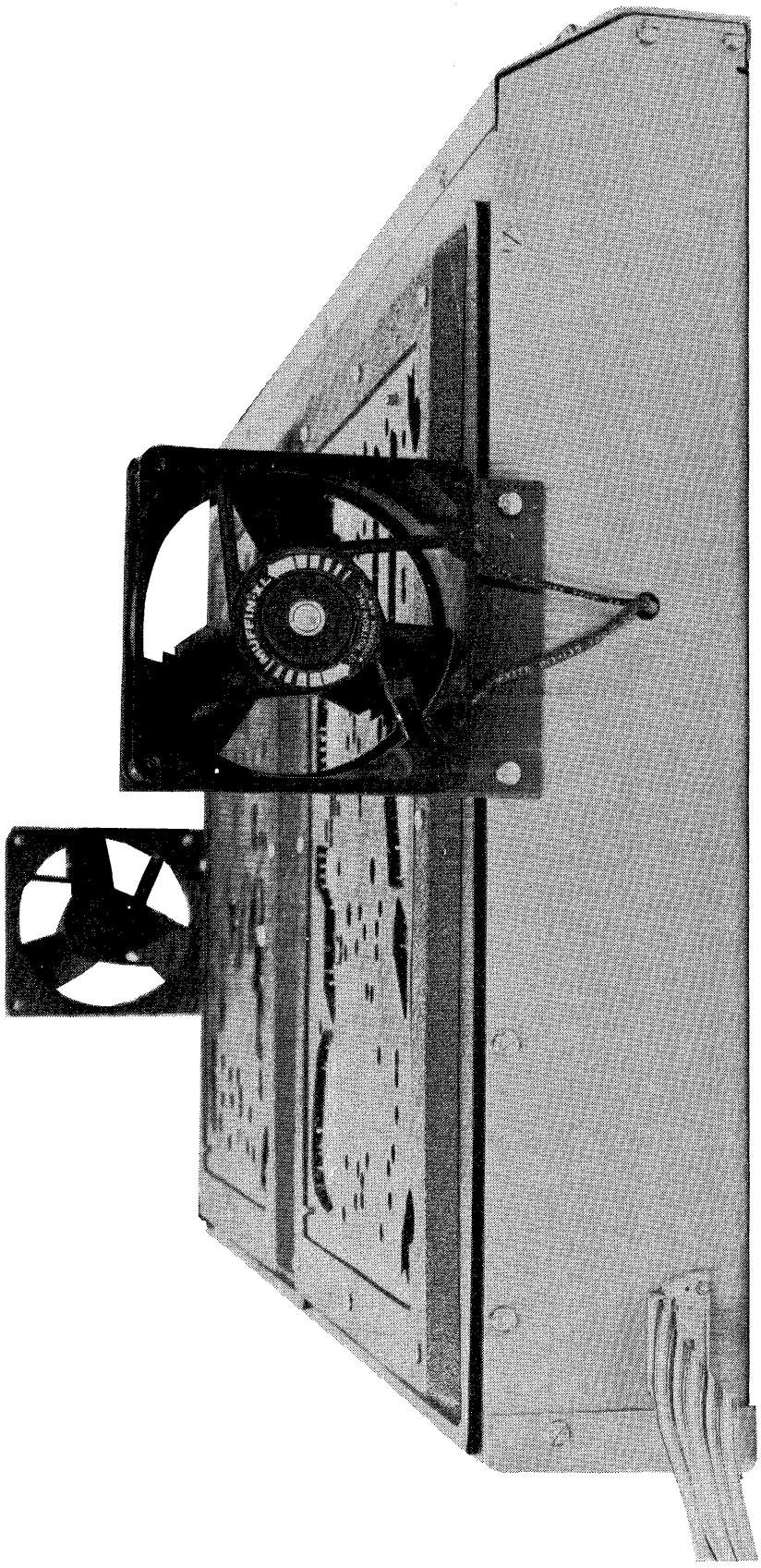

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Figure 2-5. FVS Vacuum Chamber Assembly Controls and Test Points, Left Side Panel

2.5.1 Initial Turn-On Procedures for the FVS

The FVS should be readied for diagnostic testing of the 990/12 LR AU and SMI boards as follows:

1. On both DS10 disk drive units (one in pedestal assembly and one in desk assembly), ensure that the START/STOP switch/indicator is in the STOP position (pushbutton raised and the indicator extinguished).

2. Close the ac (MAIN) circuit breaker at the rear of both disk drive units.

3. Turn the circuit breaker for the FVS on the desk assembly to ON.

4. Install the disk cartridge containing the DOGS operating software with overlays and diagnostics into the DS10 disk drive associated with the 990/10 computer (located in the pedestal assembly) as follows:

   a. Pull the disk drive out of the rack.

NOTE

Power must be on and the START/STOP lamp must be extinguished to release the lock on the hold-down arms.

   b. Pull back the hold-down arms.

   c. Set the disk cartridge upright on a firm supportive surface.

NOTE

Two types of disk cartridges are provided for the DS10. One type features a dust cover lock that releases when moved to the left. The other type releases the lock when the button is pushed to the center of the handle.

   d. Hold the disk cartridge cover release button in the unlocked position while lifting the cartridge handle to separate the dust cover and disk.

   e. Disengage the dust cover from the disk. Set the dust cover aside.

CAUTION

Do not make abusive contact between the disk and the spindle. Ensure that the read/write heads are fully retracted and the brushes are completely out of the disk area. Remove any dust from the magnetic chuck.

f. Position the head opening of the disk toward the rear of the disk drive and place the disk onto the spindle hub.

g. Rotate the cartridge slowly back and forth until the cartridge seats over the spindle.

h. Turn the handle down to seat the cartridge.

i. Place the dust cover (removed in step e) with the open end down over the cartridge.

j. Position the hold-down arms over the cartridge and dust cover.

k. Push the disk drive into the rack.

5. Select write protection for both the cartridge and the fixed disk for the 990/10 DS10 as follows:

   a. Observe that the disk drive front panel alternate-action switches, WRITE PROTECT CART and WRITE PROTECT DISK are not lighted.

   b. Depress the WRITE PROTECT CART and WRITE PROTECT DISK switches. Observe that the switch indicators light and that the switches remain in a partially depressed position.

6. Press the DS10 disk drive front panel START/STOP switch/indicator. Ensure that the pushbutton stays partially depressed and that the indicator lights. Verify that the FAULT switch/indicator remains extinguished.

7. The READY indicator lights, and the disk drive is ready for operation by the computer approximately 65 seconds after pressing the START/STOP switch/indicator.

8. Using the procedures of steps 4, 6, and 7, install the disk cartridge containing the operating system for the 990/12 LR CPU boards into the DS10 disk drive located in the desk assembly. Do not select write protection for the operating system disk.

9. Turn the Model 810 Printer power switch (located at the left rear of the printer as you face the printer) to the on position. Observe that the POWER indicator on the printer operator control panel is lit.

10. Turn the 743 KSR data terminal ac power switch to the on position. The ac power switch is a toggle switch on the top rear corner of the KSR. When the toggle switch is pushed to the rear of the unit, ac power is applied to the unit.

11. Turn the 990/10 programmer panel key switch to UNLOCK and then depress the HALT, RESET, and LOAD switches in that order.

12. Initialize the 990/10 system as follows:

    a. Set the 911 video display terminal (VDT) power switch located on the right side of the video display monitor housing to ON.

    b. On the 911 VDT, enter Y and RETURN.

    c. The video display responds:

        CRT 911 INT LEVEL? DEF = 0A-

    d. Enter B and RETURN. The video display responds:

        ERROR MSG DEVICE (0 = ASR/KSR 1 = 913 2 = 911 3 = LP)? DEF = 2-

    e. Enter 3 and RETURN. The video display responds:

        PRINTER CRU ADDR? DEF = 0060-

    f. Press RETURN. The video display responds:

        PRINTER INT LEVEL? DEF = 0E-

    g. Press RETURN. The video display responds:

        ENTER CONTROL OPTIONS SEPARATED BY COMMAS; (E = ERROR MSG'S, H = HDR MSG'S, N = ERR #'S, I = IDLE ON ERR'S)-

    h. After entry of control options as desired, press RETURN. The video display responds:

        LOAD TEST? (DEF = 0)-

    i. Press RETURN. The video display responds:

        VERB?-

    j. Enter IT and RETURN. The system is now initialized and ready to perform diagnostic testing of the 990/12 LR CPU boards.

2.5.2 Diagnostic Testing Procedures Using the FVS

To test the individual boards on the FVS use the following tests:

- AU test — Part number 2309323-9901
- SMI test — Part number 2309328-9901

These boards are tested as a set. The test concept relies on a standard known-to-be-good board to be used in conjunction with the board to be tested. That is, when the AU board is to be tested, a standard known-to-be-good SMI board is used as the other board of the set; when the SMI board is to be tested, a standard known-to-be-good AU board is used as the other board of the set. The steps noted in the aforementioned tests should be performed in order and any failure should be noted. Use the troubleshooting procedures of paragraph 2.6 to isolate failures to a replaceable component.

CAUTION

Ensure that the boards are properly seated when the VACUUM switch is depressed before applying power with the UUT POWER switch. Failure to do so can damage the boards.

2.5.3 FVS 990/12 LR Operating System Recovery

Each of the two previously described DS10 drives have one fixed disk and one removable cartridge disk. They are assigned separate logical unit numbers as though they were physically separate, independent devices. The DS10 pedestal type disk drive contains the software for the 990/10 operating system (optional) on the fixed disk and the removable cartridge disk contains the DOGS operating software and diagnostic overlays. The desk assembly DS10 disk drive, fixed disk, contains the software for the 990/12 LR operating system. The removable cartridge disk for this disk drive is a spare position not used in the operation of the FVS disk drive controller, or the standard set of 990/12 LR CPU boards.

In the normal operation of the FVS for testing, a bad CPU board can erratically overwrite on and can destroy the 990/12 LR operating software. The operating system can be restored by using the Disk Copy/Restore (DCOPY) utility of the DX10 operating system to copy the contents of the removable cartridge disk backup copy of the 990/12 LR operating system to the fixed disk of the desk assembly DS10 disk drive. If not already installed, use the procedures of paragraph 2.5.1 to install the removable cartridge backup copy of the 990/12 LR operating system into the desk assembly DS10 disk drive. Refer to Volume II of the *DX10 Operating System Release 3 Reference Manual* (use the most recent release) for a complete description of the DCOPY operating procedures. Procedures for restoring the 990/12 LR operating system follow.

CAUTION

Ensure that the boards are properly seated in the vacuum fixture when the VACUUM switch is pressed before applying power with the UUT POWER switch. Failure to do so can damage the boards.

1. Install standard known-to-be-good AU and SMI boards in the vacuum chamber assembly. The boards are placed on the vacuum chamber assembly with the component side up. The boards are properly oriented by placing the holes at two opposite corners of the boards over the guide pins that are part of each side of the vacuum chamber assembly. Press the white VACUUM switch on the left side of the vacuum chamber assembly and the UUT POWER switch on the right side of the vacuum chamber assembly. The displays at the front part of the vacuum chamber assembly should now be illuminated.

2. Press the CMD key on the 911 VDT keyboard. The system responds with:

   VERB?-

3. Enter RS and press RETURN on the 911 VDT keyboard. The system responds with:

   VERB?-

4. Enter RO and press RETURN on the 911 VDT keyboard.

5. Enter EC and press RETURN on the 911 VDT keyboard. The system responds with:

   Monitor? (0 = NO MONITOR, 1 = MDIAG, 2 = PDT) DEF = 0-

6. Press RETURN for the default response. The system responds with:

   VERB?-

7. On the maintenance unit programmer panel, press HALT, RESET, and CLEAR.

8. On the maintenance unit programmer panel data entry switches, select hexadecimal 0084, press MA ENTER and then MDD.

9. Select hexadecimal 0400 on the maintenance unit programmer panel data entry switches.

10. On the 990/12 LR DS10 desk assembly disk drive, press the alternate action WRITE PROTECT CART and WRITE PROTECT DISK switches to unprotect both disks. On the maintenance unit programmer panel, press the MDE switch and LOAD switch. After a few seconds the IDLE LED on the maintenance unit programmer panel lights, denoting that the 990/12 LR operating system from the removable disk in the spare position has been booted.

11. On the keyboard of the 743 KSR data terminal, enter ESC and !. The system responds on the 743 printer as follows:

    WARNING: SYSTEM IS NOT INITIALIZED

    [ ]

12. Enter ISA. and press RETURN from the 743 KSR keyboard. The system responds with:

    **** START LOG COMMAND PROCESSED ****
    WARMSTART PROCEDURE COMPLETE:

13. Press RETURN on the 743 KSR keyboard.

14. To execute the Disk Copy/Restore routine, enter DCOPY and press RETURN on the 911 VDT keyboard. DCOPY begins execution with the following statement:

    DISK COPY/RESTORE
    ANSWER (Y/N) QUESTIONS WITH Y FOR YES AND ANY OTHER
    CHARACTER EXCEPT $ FOR NO
    RESPOND ANY TIME WITH $ TO RESTART
    LISTING DEVICE NAME-

15. Press the alternate action WRITE PROTECT CART switch on the desk assembly DS10 disk drive to protect the disk cartridge. To the request for listing device, the operator should press RETURN.

16. The system begins a series of requests as follows:

    VERIFY ONLY? (Y/N)

17. Press N and RETURN.

    DEFAULT? (Y/N)

18. Press Y and RETURN.

19. The copy utility prompts for the following input:

    MASTER DEVICE

20. Enter DS01 and press RETURN. The system then prompts:

    VOLUME

21. Operator response should be DOGS12 COPY (or other name of backup disk) and press RETURN. The utility then prompts:

    COPY DEVICE

22. Operator response should be DS02 and RETURN. The utility then prompts:

    VOLUME

23. Operator response should be DOGS12 and RETURN. The system responds with the following message:

    MOUNT DESIRED VOLUMES-
    TYPE CR WHEN READY

24. Depress the alternate action WRITE PROTECT CART switch to protect the removable cartridge disk for the desk assembly DS10 disk drive. Press RETURN on the 911 VDT keyboard. At this time the copy operation is initiated.

25. The copy operation is complete when the following messages are displayed:

    COPY AND VERIFY COMPLETE
    QUIT? (Y/N)

26. The operator should respond with Y and RETURN.

27. The system responds to the QUIT affirmative response with:

    SYSTEM DISK READY?

28. Press the alternate action WRITE PROTECT CART switch on the desk assembly DS10 disk drive to unprotect the disk cartridge and enter Y and RETURN in response to the system disk ready query. At this time DCOPY terminates.

CAUTION

If it is necessary in the next step to run the DS10 diagnostics, remove the backup copy of the 990/12 LR operating system from the spare removable cartridge disk position and replace it with a scratch removable cartridge disk.

29. On the maintenance unit programmer panel, press HALT, RESET, and LOAD. The system will now boot from the fixed disk drive. If any errors are found, the DCOPY routine should be attempted again. If the 990/12 LR will not boot from the fixed disk drive after two tries, the DS10 diagnostics should be run on the fixed disk drive.

2.6 CENTRAL PROCESSOR TROUBLESHOOTING PROCEDURES

The troubleshooting procedures in this paragraph are performed when it has been determined that an AU board or an SMI board is faulty from the use of the checkout procedures of paragraph 2.5. Performance of the troubleshooting procedures requires that the test equipment and reference materials, as listed in Table 2-4, be available.

Table 2-4. Test Equipment and Reference Documents Required for Troubleshooting

Item	Part Number
Oscilloscope, Tektronix Model 465 (or equivalent)	
DOGS Program Description	2268200-9901
AU Overlay Listing	2268213-9001
SMI Overlay Listing	2268214-9001
Diagnostics Listing	2268215-9001

The FVS operator should be thoroughly familiar with the program description for the DOGS software. This document describes the software used to control the 990/12 LR FVS and describes the special verbs and the error messages used.

If a failure occurs to a board during the running of the AU or SMI diagnostic overlays, the FVS will halt at the end of the test in which the failure occurred. At this point, the overlay number and test number that caused the failure will be displayed by the FVS. The operator can then find the reason for failure by setting a breakpoint on error and running the failing overlay again. The diagnostic then breaks at the error. The operator then can use the dump trace verb to obtain a display (or printout) of the microcode instructions executed just prior to and including the microcode instruction that caused the failure. By examining the listing for the overlay and comparing it to the trace, the operator can determine which instruction that the board under test has failed to perform. Then through use of the logic diagram for the board and the oscilloscope, the fault can be isolated to the component that caused the failure. An example of the procedures leading to the fault isolation follows.

1. Enter DC and press RETURN on the 911 VDT keyboard.
2. Enter RS and press RETURN on the 911 VDT keyboard.
3. Enter LS and press RETURN on the 911 VDT keyboard. The system responds:

   EXECUTE? (1 = YES, 0 = NO) DEF = 0 -

4. Press RETURN on the keyboard. The system responds with:

   VERIFY ONLY (0 = NO, 1 = YES) DEF = 0 -

5. Press RETURN on the keyboard. A menu will appear on the 911 video monitor along with the response:

   TYPE DIAG. # OR FILE NAME? -

   The menu displays the diagnostic numbers of the overlays. For example assume hexadecimal 47 is displayed by the FVS. Overlay hexadecimal 47 corresponds to the diagnostic number 34, therefore the operator response to the request for the diagnostic number should be to enter 34 and then set the breakpoint address as shown in the next steps.

6. Enter DC and press RETURN on the 911 VDT keyboard.

7. Enter RS and press RETURN on the 911 VDT keyboard. The system responds with:

   VERB?

8. Enter SB and press RETURN on the 911 VDT keyboard. The system responds with:

   ENTER BREAKPOINT ADDRESS -

9. Enter 1 and press RETURN on the 911 VDT keyboard.

NOTE

The error routine always returns to microcode address 0001. At the breakpoint, the trace memory contains the last 32 microcode instructions executed, and this necessarily includes those instructions required to execute the error routine.

The system continues with the SB verb as follows:

SOFT BP ?(0 = NO, 1 = YES) DEF = 0 -
WAIT FOR BREAKPOINT? (1 = YES, 0 = NO) DEF = 1 -

10. The operator should default through these two queries by pressing RETURN on the 911 VDT keyboard. The system responds:

    WAITING FOR BREAKPOINT

    The SB verb automatically turns on the clock, executes the diagnostic, and breakpoints at microcode address 1. At this point the operator should execute the DT verb to dump the state controller board trace memory. Information on the format of the dumped trace memory is contained in the program description for the DOGS software. The dump of the trace memory provides the address of the microcode instruction that led to the error routine. By consulting the listing for the diagnostic at the instruction that failed, the operator can determine the nature of the failure. Use the logic diagram for the board under test and the oscilloscope to isolate the trouble to the failed component. After repairing the board, run the complete diagnostic to ascertain that the board is free from faults.

    Use similar troubleshooting procedures if a failure occurs to a board during the execution of the AU12 diagnostic portion of the test or (in the case of the AU board under test) the execution of the test of the instruction microcode. Instead of an FVS display of overlay and test failure, a message of error condition is printed on the Model 810 Printer. Selected AU diagnostics can be loaded into memory by using the DD verb and the microcode test overlay can be loaded by using the LS verb.

3

Drawings

This section contains the following assembly drawings and logic diagrams for the 990/12 LR CPU:

DWG NO 2303320

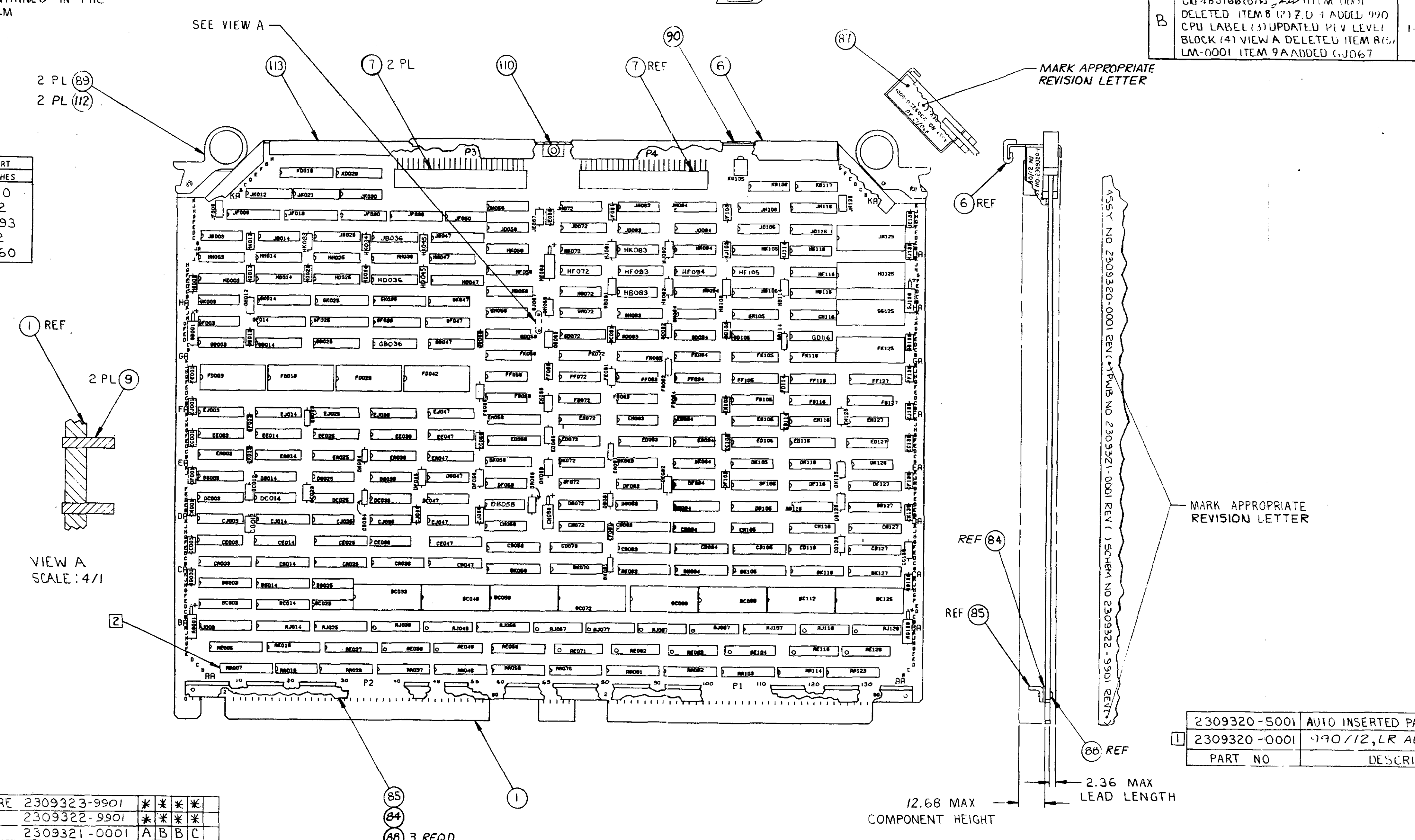
NOTES: UNLESS OTHERWISE SPECIFIED:

[1] ITEM 111 IN THE -0001 LM CONSISTS OF COMPONENTS WHICH ARE AUTO-INSERTED AND CONTAINED IN THE -5001 LM

[2] AA007 IS A SPARE LOCATION

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	CN 431214(D15) ITEM 0001 ADDED ITEM 115 (2) UPDATED REV LEVEL BLOCK	1-27-83	Haykes
B	CN 485166(B15) ITEM 0001 DELETED ITEM 8 (2) 7.D 4 ADDED 990 CPU LABEL (3) UPDATED REV LEVEL BLOCK (4) VIEW A DELETED ITEM 8 (5) LM-0001 ITEM 9A ADDED GJ067	1-27-83	Haykes

CONVERSION CHART	
mm	INCHES
0.25	.010
0.5	.02
2.36	.093
3.0	.12
12.68	.460



	2309320-5001	AUTO INSERTED PARTS LIST FOR -0001
[1]	2309320-0001	990/12, LR AU ASSEMBLY
	PART NO	DESCRIPTION

REVISION LEVEL					
TEST PROCEDURE	2309323-9901	*	*	*	*
LOGIC	2309322-9901	*	*	*	*
PWB	2309321-0001	A	B	B	C
ASSEMBLY	2309320	*	*	A	B

3	MARK	902-01	01	HGT 3.0, CLR BLK, (CAT 16)
2	SLDR	127-01	00	
1	SLDR	124-02	00	
SEQ		PROCESS		ADDITIONAL CLASSIFICATION

-3 QTY	-2 QTY	-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES: 2 PLACE DECIMALS ±0.25, 1 PLACE DECIMALS ±0.5, ANGLES ±1°
- INTERPRET DRAWING PER DOD-D-1000
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS 0.25 FIM
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

NEXT ASSY 2309332 — USED ON 7110

TEXAS INSTRUMENTS — SI-METRIC

990/12, LR AU ASSEMBLY

SIZE D — FSCM NO 06668 — DRAWING NO 2309320

REV STATUS OF SHEETS

LM

32

TEXAS INSTRUMENTS
INCORPORATED

DATE 01/26/83 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 1 of

PART NUMBER: LM2309320-0001 — REV: B

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	REF	EA		2309322-9901	LOGIC DIAG,990/12,LR AU	
0003	REF	EA		2309323-9901	TEST PROCEDURE,990/12,LR AU	
0004	REF	EA		2309324-9901	SPEC,990/12,LR AU	
0005	00001.000	EA		2220291-0001	LED,RED,5V=VF,15MA=IF,R.ANGLE,1-POS.	
0005A					KG105	
0006	00001.000	EA		2308640-0001	INSULATOR,SHIELD-STIFFENER,270.5MM	
0007	00002.000	EA		2210154-0015	HEADER,POLARIZED AND LATCHING, 50 PINS	000779-86476-7
0007A					P3 P4	
0009	00002.000	EA		0996864-0001	CONNECTOR,SOCKET PCB	022526-75060-007
0009A					GF067 GJ067	
0076	00004.000	EA		0996768-0001	IC,SN74S481,A 4-BIT MICROCOMPUTER	001295-SN74S481
0076A					FD003 FD016 FD029 FD042	
0084	00001.000	EA		2308655-0001	INSULATOR,PWB,346.96MM,EYELET MOUNT	
0085	00001.000	EA		2308653-0001	STIFFENER,PWB,346.96MM,EYELET MOUNT	
0087	00001.000	EA		2308630-0005	LABEL,ID,990 EMI/RFI BD-990/AU	
0088	00003.000	EA		0085936-0017	EYELET .121 BARREL OD X.187 LG FLANGE	USH - #SE-46
0089	00002.000	EA		2308622-0001	EJECTOR,PWB,SELF-LOCKING	
0090	00001.000	EA		2308652-0001	LABEL,LED,CPU,990 EMI/RFI-BOARD FAULT	

DRAFTSMAN — DATE — CKD DRAFTSMAN J. Robby 1-26-83 — DATE — DESIGN ENGINEER — DATE — TITLE: 990/12,LR AU ASSY

APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO 7110 — PART NUMBER LM2309320-0001 — REV B

T.I. 25789

TEXAS INSTRUMENTS
INCORPORATED

DATE 01/26/83 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 2 of

PART NUMBER: LM2309320-0001 — REV: B

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0110	00001.000	EA		0972831-0003	RIVET,1/8X.235,TUBULAR,STEEL,BLIND	019738-1821-0408
0111	00001.000	EA		2309320-5001	AUTO-INSERTED PARTS LIST FOR -0001	
0112	00002.000	EA		0085936-0067	EYELET.089 BARREL OD X.375 LG FLANGE	
0113	00001.000	EA		2308618-0001	SHIELD-STIFFENER,GROUP III,(CPU)	
0115	REF	EA		2262003-9901	TEST PROC, SYSTEM, 990/12 CPU W/MAPPING	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: 990/12,LR AU ASSY

APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2309320-0001 — REV B

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TEXAS INSTRUMENTS
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DATE 01/26/83 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 1 of

PART NUMBER: LM2309320-5001 — REV: B

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2309321-0001	PWB,990/12 AU,LR	
0010	00006.000	EA		0972924-0006	CAP FIX TANT SOLID 39 UFD 10% 10 VOLT	QPL -M39003/1-2259
0010A					AG001 AG138 CH069 GB001	
0010B					HE069 GJ138	
0011	00004.000	EA		0972900-7400	NETWORK SN74LS00N	TI -SM74LS00N
0011A					DB072 FK072 GD083 GD116	
0012	00001.000	EA		0972900-7402	NETWORK,SN74LS02N	
0012A					EH072	
0013	00003.000	EA		0972900-7404	NETWORK SN74LS04N	
0013A					DG025 DK083 FF072	
0014	00004.000	EA		0972749-0001	NETWORK, SN74LS08N	
0014A					GD058 GK003 HF058 JH094	
0015	00003.000	EA		0972900-7410	NETWORK SN74LS10N	
0015A					GD094 HK083 JD083	
0016	00001.000	EA		2261989-0001	PROM,990/12 AU,CROM 00	SEE TI- DRAWING
0016A					BC033	
0017	00001.000	EA		0972900-7112	NETWORK SN74LS112N	TI -SN74LS112N
0017A					GH083	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR -0001

APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2309320-5001 — REV B

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TEXAS INSTRUMENTS
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DATE 01/26/83 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 2 of

PART NUMBER: LM2309320-5001 — REV: B

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0018	00001.000	EA		0222222-7125	NETWORK SN74125N	
0018A					FF083	
0019	00001.000	EA		0972900-7138	NETWORK SN74LS138N	TI -SN74LS138N
0019A					FK058	
0020	00007.000	EA		0972946-0065	RES FIX 1.0K OHM 5% .25 W CARBON FILM	ROH - R-25
0020A					EA081 DK012 EF012 EG023	
0020B					FG092 GD092 GB114	
0021	00005.000	EA		0801383-0001	NETWORK SN74LS151N	
0021A					EA036 ED105 JB025 JK021	
0021B					KD029	
0022	00003.000	EA		0972900-7153	NETWORK SN74LS153N	TI -SN74LS153N
0022A					FK083 JB036 JF030	
0023	00001.000	EA		0219402-7175	NETWORK,SN74S175N	
0023A					DF083	
0024	00002.000	EA		0972900-7420	NETWORK SN74LS20N	
0024A					DC025 EH094	
0025	00001.000	EA		0972813-0001	NETWORK-SN74LS21N	
0025A					ED127	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR -0001

APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2309320-5001 — REV B

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DATE 01/26/83 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 3 of — PART NUMBER LM2309320-5001 — REV B

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0026	00004.000	EA		0996845-0001	IC,AM29701PC 16 X 4-BIT RAM	034335-AM29701PC
0026A					EE003 EE014 EE025 EE036	
0027	00008.000	EA		0996089-0001	IC,SN74LS240N,LINE DRIVERS	001295-SN74LS240N
0027A					AA048 AA070 AE005 AE016	
0027B					AE027 AJ003 CJ014 CH127	
0028	00001.000	EA		0996089-0002	IC,SN74LS241N,LINE DRIVERS	01295S-N74LS241N
0028A					EH058	
0029	00002.000	EA		0996089-0004	IC,SN74LS244N LINE DRIVER	-SN74LS244N
0029A					CA025 CE025	
0030	00010.000	EA		0996755-0001	IC,SN74LS245N BUS XCVR TRANSITION	001295-SN74LS245N
0030A					CA036 CA047 BK058 BK070	
0030B					BK105 BK116 BK127 GF014	
0030C					GF025 BK094	
0031	00004.000	EA		0996136-0001	IC,SN74LS257N,DATA SELECTORS/MULTIPLEXER TI -SN74LS257N	
0031A					HH003 HH014 HH025 HH036	
0032	00001.000	EA		0996136-0002	IC,SN74LS258N,DATA SELECTORS/MULTIPLEXER TI -SN74LS258N	
0032A					DG003	
0033	00002.000	EA		0972120-0001	NETWORK,SN74259 8-BIT ADDRESSABLE LATCH	001295-74259

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR -0001
APPD.MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2309320-5001 — REV B

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TEXAS INSTRUMENTS
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DATE 01/26/83 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 4 of — PART NUMBER LM2309320-5001 — REV B

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0033A					HH047 HF083	
0034	00001.000	EA		0996029-0001	IC,SN74LS273N OCTAL D-TYPE FLIP/FLOP	TI -SN74LS273N
0034A					JB047	
0035	00001.000	EA		0972811-0001	NETWORK-SN74LS280N	
0035A					DC014	
0036	00001.000	EA		0972900-7432	NETWORK SN74LS32N	TI -SN74LS32N
0036A					HF105	
0037	00001.000	EA		2261989-0002	PROM,990/12 AU,CROM 08	SEE TI- DRAWING
0037A					BC046	
0038	00003.000	EA		0996852-0001	IC,SN74LS353N DUAL 4/1 LINE DATA SEL	001295-SN74LS353N
0038A					CE003 CJ003 DC003	
0039	00002.000	EA		0996420-0001	IC, SN74LS373N	001295-SN74LS373N
0039A					GK014 GK025	
0040	00003.000	EA		0996420-0002	IC,SN74LS374N	001295-SN74LS374N
0040A					CD058 CD105 CD127	
0041	00002.000	EA		0996769-0001	IC,SN74LS377N,OCTAL,D-TYPE FLIP-FLOP	001295-SN74LS377N
0041A					BC003 BC014	
0042	00001.000	EA		0996770-0001	IC,SN74LS378N,D-TYPE FLIP-FLOP	001295-SN74LS378N

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR -0001
APPD.MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2309320-5001 — REV B

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DATE 01/26/83 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 5 of — PART NUMBER LM2309320-5001 — REV B

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0042A					JB014	
0043	00001.000	EA		0996770-0002	IC,SN74LS379N D-TYPE FLIP-FLOP	001295-SN74LS379N
0043A					JB003	
0044	00002.000	EA		0972900-7451	NETWORK SN74LS51N	TI -SN74LS51N
0044A					DC047 HK116	
0045	00001.000	EA		2261989-0003	PROM,990/12 AU,CROM 16	SEE TI- DRAWING
0045A					BC059	
0046	00002.000	EA		0972900-7474	NETWORK SN74LS74N	
0046A					HB083 HB094	
0047	00001.000	EA		0972785-0001	NETWORK SN74S85N	
0047A					JK012	
0048	00010.000	EA		0219402-7400	NETWORK SN74S00N	
0048A					BC025 CJ025 CH105 DF094	
0048B					EH116 FB058 GF003 GF047	
0048C					JD058 JK030	
0049	00003.000	EA		0219402-7402	NETWORK SN74S02N	TI -SN74S02N
0049A					ED094 HF072 JD106	
0050	00001.000	EA		0219402-7403	NETWORK SN74S03N	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR -0001
APPD.MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2309320-5001 — REV B

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DATE 01/26/83 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 6 of — PART NUMBER LM2309320-5001 — REV B

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0050A					EA025	
0051	00008.000	EA		0219402-7404	NETWORK SN74S04N	
0051A					CE014 DB083 FB094 FB116	
0051B					JH058 JH106 FB072 KB108	
0052	00008.000	EA		0219402-7408	NETWORK SN74S08N	TI- -SN74S08N
0052A					DC036 EH083 EH127 HK058	
0052B					JD094 JH072 CJ036 ED072	
0053	00005.000	EA		0219402-7410	IC, SN74S10N	
0053A					DG036 DG047 GH058 JF050	
0053B					DK128	
0054	00005.000	EA		0219402-7411	NETWORK SN74S11N	
0054A					CH094 DF072 FB083 HB072	
0054B					GK047	
0055	00001.000	EA		0219402-7133	NETWORK SN74S133N	
0055A					DB116	
0056	00004.000	EA		0219402-7138	NETWORK SN74S138N	
0056A					CH072 CH116 HK072 JD072	
0057	00005.000	EA		0219402-7153	NETWORK SN74S153N	TI -SN74S153N

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR -0001
APPD.MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2309320-5001 — REV B

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TEXAS INSTRUMENTS INCORPORATED — LIST OF MATERIAL — ORIGINAL COPY — PAGE 7 of — DATE 01/26/83 — PART NUMBER LM2309320-5001 REV B

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0057A					EE047 EJ047 EH105 HK105	
0057B					JH116	
0058	00003.000	EA		0219402-7157	NETWORK SN74S157N	
0058A					ED116 FB127 FF116	
0059	00003.000	EA		0996305-0001	IC,SN74S169 UP/DOWN COUNTER,4 BIT	001295-SN74S169
0059A					EA003 EA014 EA047	
0060	00001.000	EA		0219402-7182	NETWORK SN74S182N	TI -SN74S182N
0060A					GB047	
0061	00005.000	EA		0996795-0001	IC,SN74S189N 16 X 4-BIT STATIC RAM	01295S-N74S189N
0061A					DK058 EJ003 EJ014 EJ025	
0061B					EJ036	
0062	00002.000	EA		0219402-7194	NETWORK SN74S194N	
0062A					DB094 FK116	
0063	00001.000	EA		0219402-7420	NETWORK SN74S20N	
0063A					CJ047	
0064	00007.000	EA		0996046-0001	IC,OCTAL BUFFER/DRIVER SN74S240	TI -SN74S240
0064A					AA026 AA037 DB127 DF127	
0064B					GF036 GK036 KD018	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR -0001

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2309320-5001 REV B

T.I. 25788

TEXAS INSTRUMENTS INCORPORATED — LIST OF MATERIAL — ORIGINAL COPY — PAGE 8 of — DATE 01/26/83 — PART NUMBER LM2309320-5001 REV B

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0065	00002.000	EA		0996063-0001	IC,SN74S241N,LINE DRIVERS	001295-SN74S241N
0065A					AA059 AA081	
0066	00004.000	EA		0219402-7251	NETWORK SN74S251	
0066A					FF094 FF105 FK094 FK105	
0067	00001.000	EA		0219402-7257	NETWORK SN74S257N	
0067A					DB105	
0068	00008.000	EA		0219402-7258	NETWORK SN74S258N	
0068A					HD003 HD014 HD025 HD036	
0068B					GB003 GB014 GB025 GB036	
0069	00001.000	EA		2261989-0004	PROM,990/12 AU,CROM 24	SEE TI- DRAWING
0069A					BC072	
0070	00001.000	EA		2261989-0005	PROM,990/12 AU,CROM 32	SEE TI- DRAWING
0070A					BC086	
0071	00003.000	EA		0219402-7430	NETWORK SN74S30N	
0071A					CD116 FB105 HK094	
0072	00005.000	EA		0219402-7432	NETWORK SN74S32N	TI- -SN74S32N
0072A					DF058 DF116 DK116 HB105	
0072B					HF094	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR -0001

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2309320-5001 REV B

T.I. 25788

TEXAS INSTRUMENTS INCORPORATED — LIST OF MATERIAL — ORIGINAL COPY — PAGE 9 of — DATE 01/26/83 — PART NUMBER LM2309320-5001 REV B

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0073	00016.000	EA		0996201-0001	IC,SN74S374N,EDGE-TRIGGERED FLIP-FLOPS	TI -SN74S374N
0073A					AA092 AA103 AE059 AA123	
0073B					AJ014 AJ025 AJ056 AJ107	
0073C					BG003 BG014 CA003 CA014	
0073D					CE047 CD070 CD094 ED058	
0074	00001.000	EA		2261989-0006	PROM,990/12 AU,CROM 40	SEE TI- DRAWING
0074A					BC099	
0075	00001.000	EA		2261989-0007	PROM,990/12 AU,CROM 48	SEE TI- DRAWING
0075A					BC112	
0077	00003.000	EA		0996102-0001	IC,SN74S482N MICRO-ADDRESS GENERATOR	TI -SN74S482N
0077A					BK083 CD083 CH083	
0078	00004.000	EA		0219402-7451	NETWORK SN74S51N	
0078A					DB058 DG014 FF058 GH072	
0079	00004.000	EA		0219402-7464	NETWORK SN74S64N	
0079A					DK094 GD105 JD116 JH083	
0080	00006.000	EA		0219402-7474	NETWORK SN74S74N	
0080A					AA018 BG025 CE036 CH058	
0080B					DK105 KB117	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR -0001

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2309320-5001 REV B

T.I. 25788

TEXAS INSTRUMENTS INCORPORATED — LIST OF MATERIAL — ORIGINAL COPY — PAGE 10 of — DATE 01/26/83 — PART NUMBER LM2309320-5001 REV B

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0081	00001.000	EA		0219402-7486	NETWORK SN74S86N	
0081A					GH094	
0082	00003.000	EA		0972946-0055	RES FIX 390 OHM 5 % .25 W CARBON FILM	ROH - R-25
0082A					DB034 DK034 GB056	
0083	00034.000	EA		0972763-0013	CAP,FIXED .010UF 50 VOLTS	004222-MC105E103Z
0083A					BG001 DB125 CK001 BG138	
0083B					DC012 DH069 CK138 EC001	
0083C					EK069 EC138 FE001 GB069	
0083D					FF138 GH012 JE067 HJ138	
0083E					HD012 HB081 HD023 HB092	
0083F					HD034 HB103 HD045 HB114	
0083G					DF045 EC056 FE081 JF081	
0083H					GD103 CJ056 EC103 DE092	
0083I					EH125 FD114	
0086	00037.000	EA		0972763-0025	CAPACITOR,.10UF 50V FX,CERAMIC DIEL	COR CA-C03Z5U104Z050A
0086A					CC001 DH125 CG012 DA066	
0086B					CC138 DF001 ED069 DF138	
0086C					EJ001 FF069 EJ138 GB012	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR -0001

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2309320-5001 REV B

T.I. 25788

TEXAS INSTRUMENTS
INCORPORATED

DATE 01/26/83 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 11 of — PART NUMBER LM2309320-5001 — REV B

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0086D					GH069 GB138 JE069 JE138	
0086E					HK012 HJ081 HK023 HJ092	
0086F					HK034 HJ103 HK045 HJ114	
0086G					DC023 CJ044 DF056 FB056	
0086H					GC081 JF103 EK103 DF103	
0086I					CD125 EG114 HB001 JF006	
0086J					JH125	
0091	00002.000	EA		0219402-7139	NETWORK SN74S139N	
0091A					DF105 GH105	
0092	00001.000	EA		0219402-7151	NETWORK SN74S151N	
0092A					HF116	
0093	00002.000	EA		2210147-0001	IC,4/1 LINE DATA SELECTOR,MUX	012955-N74LS352N
0093A					HB116 HB058	
0094	00016.000	EA		0996464-0001	IC,2114-2 1024X4-BIT STATIC RAM	001295-TMS4045-20NL
0094A					AE038 AE048 AE082 AE093	
0094B					AE104 AE116 AE126 AE071	
0094C					AJ036 AJ046 AJ077 AJ087	
0094D					AJ097 AJ118 AJ128 AJ067	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR -0001
APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2309320-5001 — REV B

T.I. 25789

TEXAS INSTRUMENTS
INCORPORATED

DATE 01/26/83 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 12 of — PART NUMBER LM2309320-5001 — REV B

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0095	00001.000	EA		2261989-0008	PROM,990/12 AU,CROM 56	SEE TI- DRAWING
0095A					BC125	
0096	00001.000	EA		2261989-0009	PROM,990/12 AU,IROM 5	SEE TI- DRAWING
0096A					FK125	
0097	00001.000	EA		2261989-0010	PROM,990/12 AU,IROM 3	SEE TI- DRAWING
0097A					GG125	
0098	00001.000	EA		2261989-0011	PROM,990/12 AU,IROM 1	SEE TI- DRAWING
0098A					HD125	
0099	00001.000	EA		2261989-0012	PROM,990/12 AU,IROM 2	SEE TI- DRAWING
0099A					JA125	
0100	00001.000	EA		2262021-0001	PROM,990/12 AU,PREFETCH INHIBIT	
0100A					AA114	
0101	00001.000	EA		2262022-0001	PROM,990/12,A DESTINATION 1	
0101A					DK072	
0102	00001.000	EA		2262022-0002	PROM,990/12,A DESTINATION 2	
0102A					GD072	
0103	00001.000	EA		2262022-0010	PROM,990/12 AU,IR DECODE 6-3H	
0103A					GH116	

AUTO-INSERTED PARTS LIST FOR -0001
APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2309320-5001 — REV B

T.I. 25789

TEXAS INSTRUMENTS
INCORPORATED

DATE 01/26/83 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 13 of — PART NUMBER LM2309320-5001 — REV B

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0104	00001.000	EA		2262019-0001	PROM,990/12 AU,DECODE 1	
0104A					ED083	
0105	00001.000	EA		2262019-0005	PROM,990/12 AU,DECODE 2-A	
0105A					HD047	
0106	00001.000	EA		2262019-0003	PROM,990/12 AU,STATUS 1	
0106A					JF008	
0107	00001.000	EA		2262019-0004	PROM,990/12 AU,STATUS 2	
0107A					JF019	
0108	00001.000	EA		2262020-0004	PROM,990/12 AU,IR DECODE 4-3H	
0108A					FF127	
0109	00001.000	EA		2262020-0002	PROM,990/12 AU,DECODE 3	
0109A					JF039	
0114	00003.000	EA		0972946-0025	RES FIX 22.0 OHM 5 % .25 W.CARBON FILM	ROH - R-25
0114A					CF081 DB081 BK081	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR -0001
APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2309320-5001 — REV B

T.I. 25789

DWG NO 2309322 SH 1

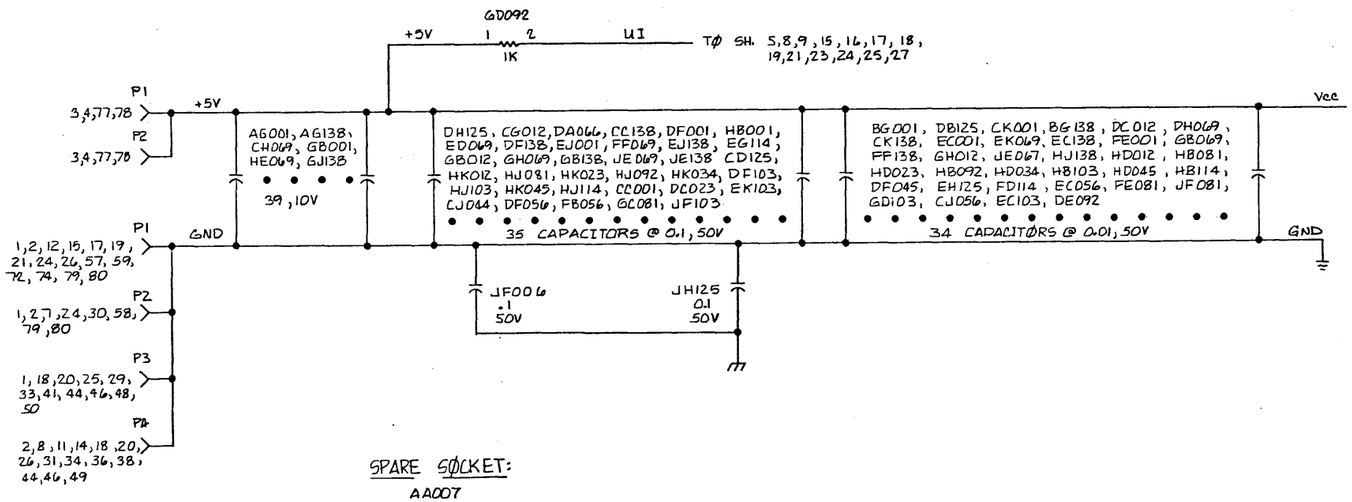
REV	DESCRIPTION	DATE	APPROVED
	REVISIONS		

NOTES: UNLESS OTHERWISE SPECIFIED:

1. ALL DEVICE TYPES ARE PREFIXED WITH SN74.
2. VCC IS APPLIED TØ PIN 8 ØF ALL 8-PIN IC'S, PIN 14 ØF ALL 14-PIN IC'S, PIN 16 ØF ALL 16-PIN IC'S, PIN 20 ØF ALL 20-PIN IC'S, ETC.
3. GRØUND IS APPLIED TØ PIN 4 ØF ALL 8-PIN IC'S, PIN 7 ØF ALL 14-PIN IC'S, PIN 8 ØF ALL 16-PIN IC'S, PIN 10 ØF ALL 20-PIN IC'S, ETC.
4. DEVICE TYPE, PIN NUMBERS, AND LØCATIØN ØF IC IS SHØWN AS FØLLØWS:

LS00 AND LS04 = DEVICE TYPE
1, 2, AND 3 = PIN NUMBERS
FK072 AND FB094 = LØCATIØN

5. RESISTANCE VALUES ARE IN ØHMS.
6. RESISTØRS ARE ¼ WATT, 5%.
7. CAPACITANCE VALUES ARE IN MICRØFARADS.



SPARE SØCKET:
AA007

.3 QTY	.2 QTY	.1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES
				PARTS LIST		

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES: 2 PLACE DECIMALS ±0.25; 1 PLACE DECIMALS ±0.5; ANGLES ±1°
- INTERPRET DRAWING PER DOD D 1000
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS 0.25 FIM
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE | THIRD ANGLE PROJECTION

0.33 THRU 3.18	±.C 10-0.03
3.20 THRU 8.35	±0.13-0.03
8.38 THRU 12.70	±0.15-0.03
12.73 THRU 19.05	±0.20-0.03

2309320 | 7110
NEXT ASSY | USED ON

DWN DATE
CHK K. KEELER 8-13-82
ENGR
APVD/ENGR
QA
APVD/MFG
KEY 9-13-82

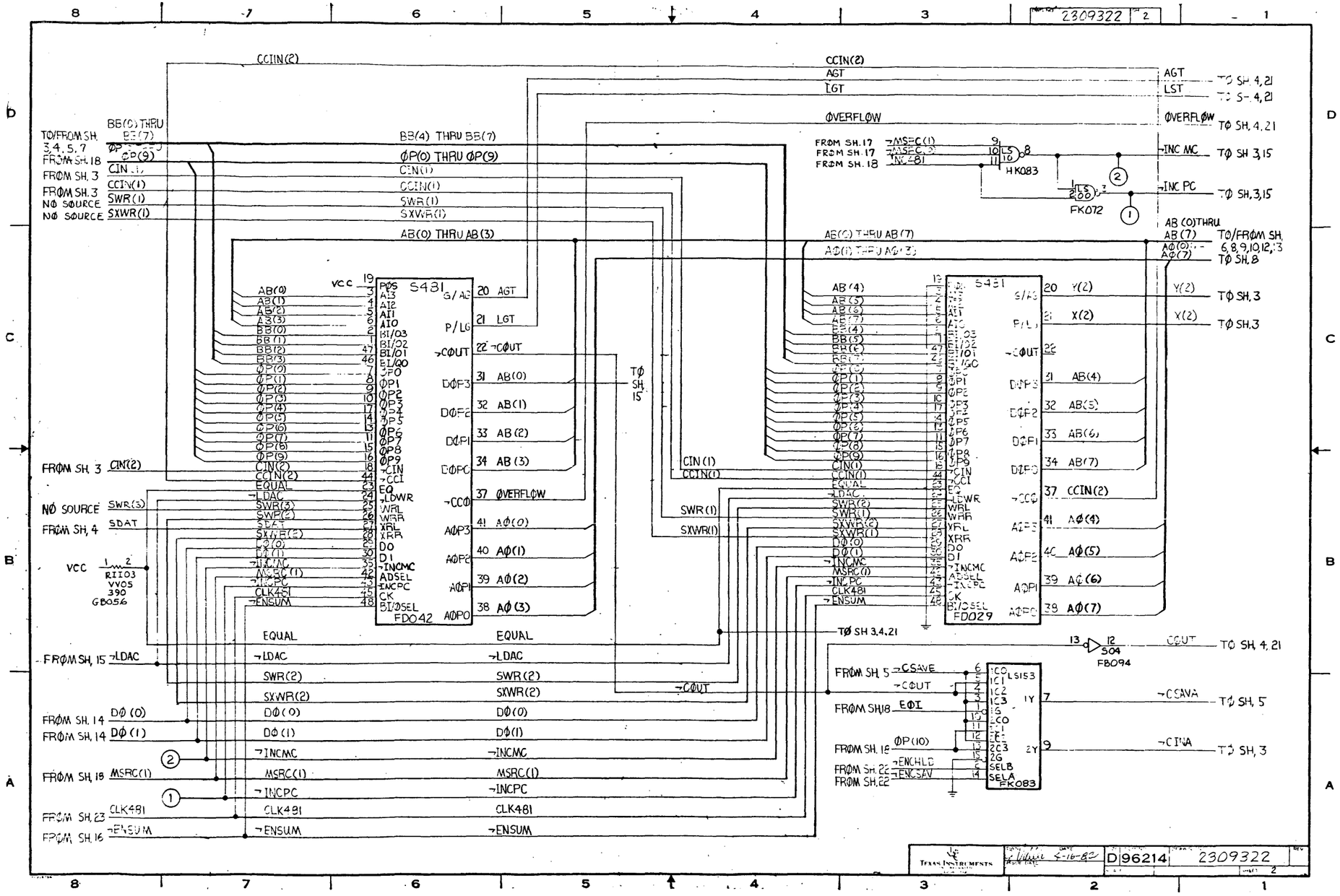
TEXAS INSTRUMENTS | SI-METRIC

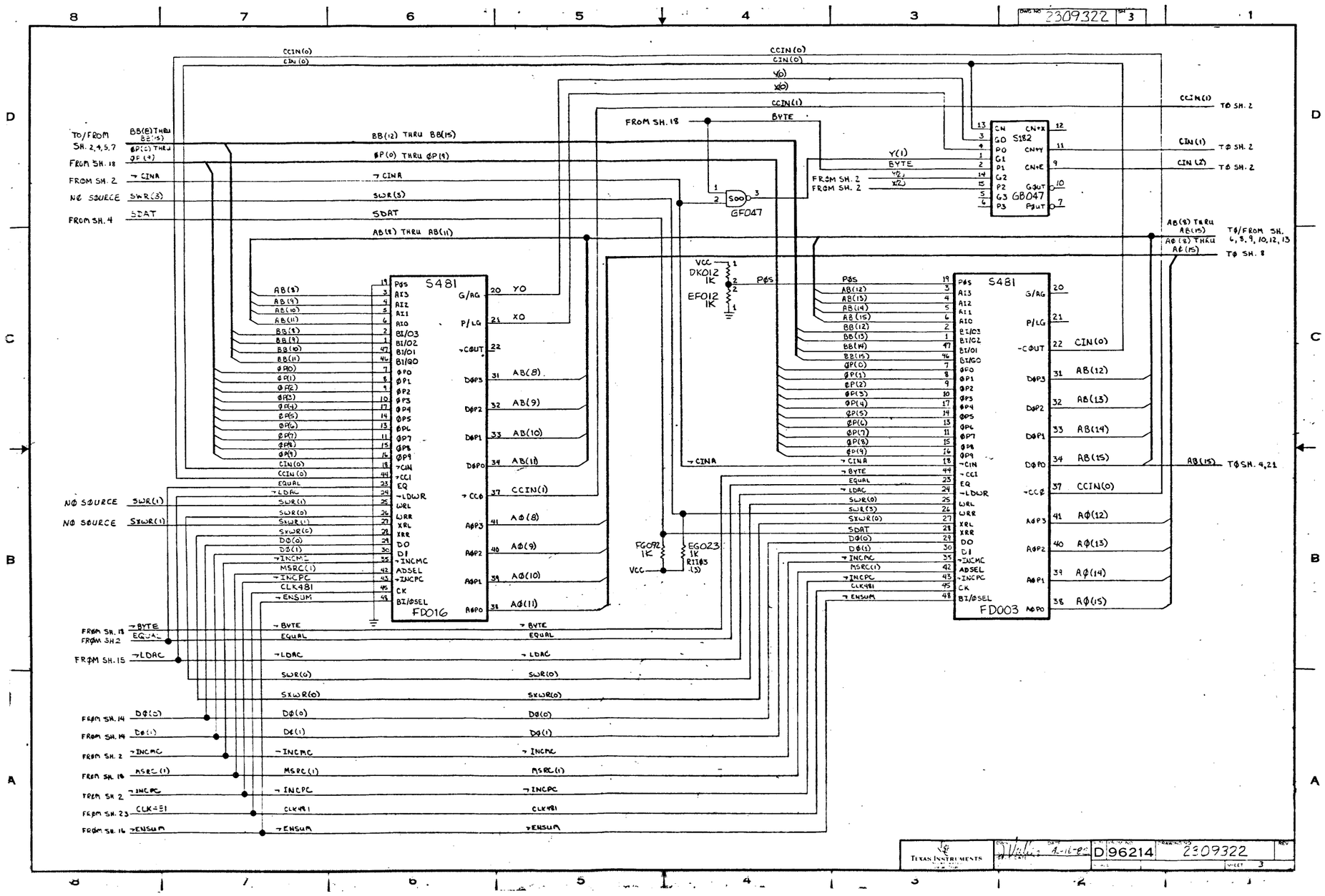
LØGIC DIAGRAM, 990/12, LR AU

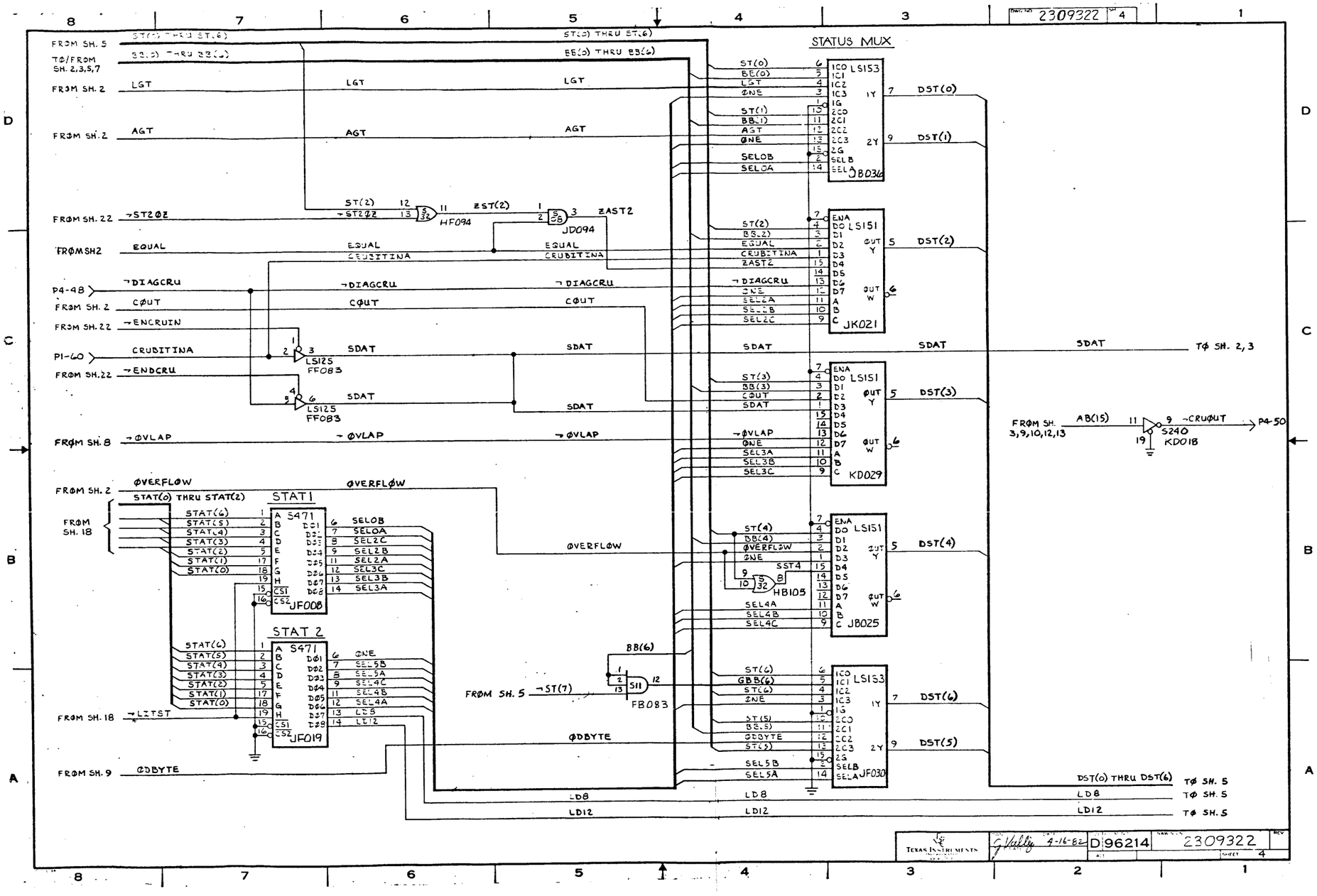
SIZE D | FSCM NO 06668 | DRAWING NO 2309322

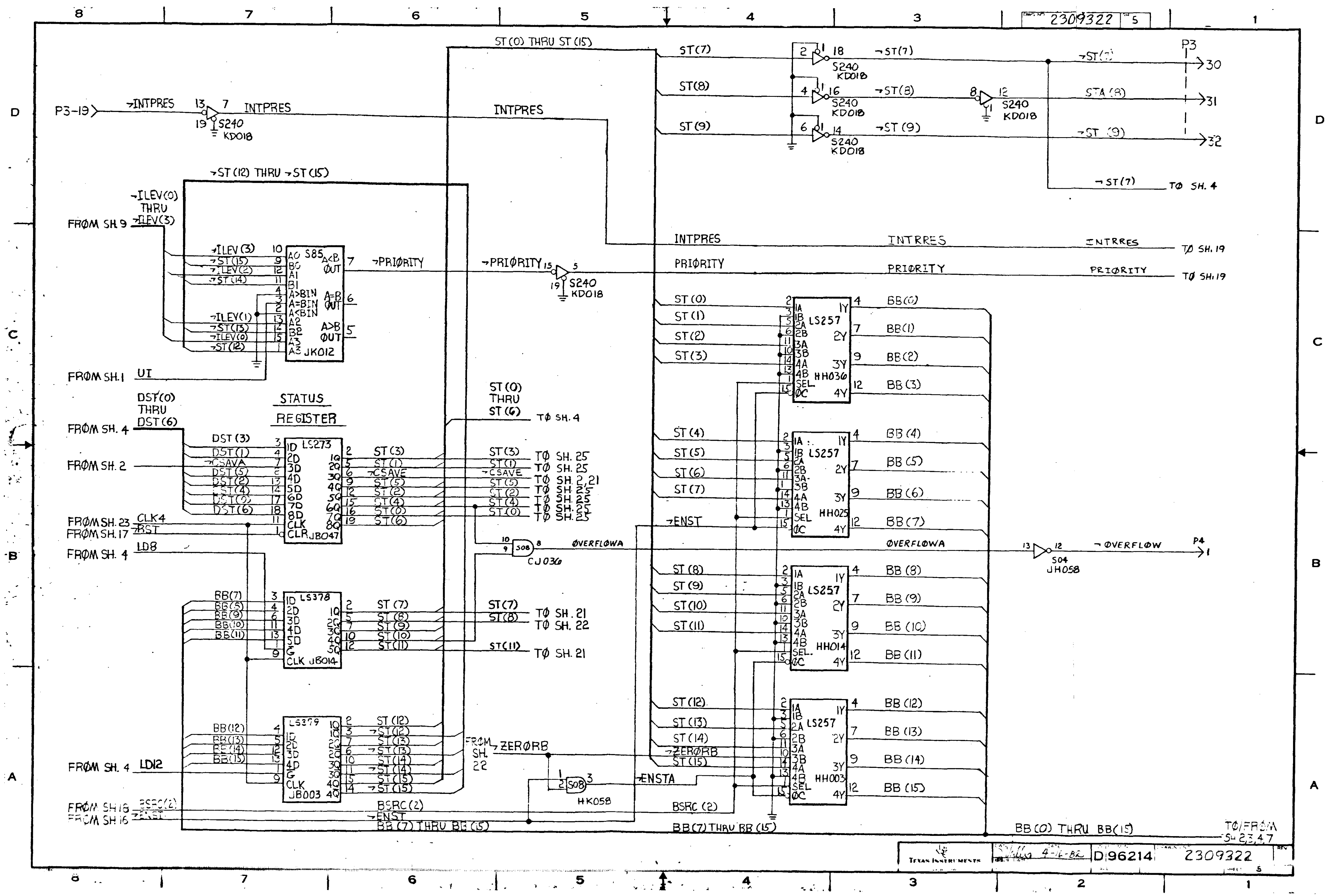
SEQ	IDENT	ADDITIONAL	NOTES	REV STATUS	REV
					17 18 19 20 21 22 23 24 25 26 27 28 29

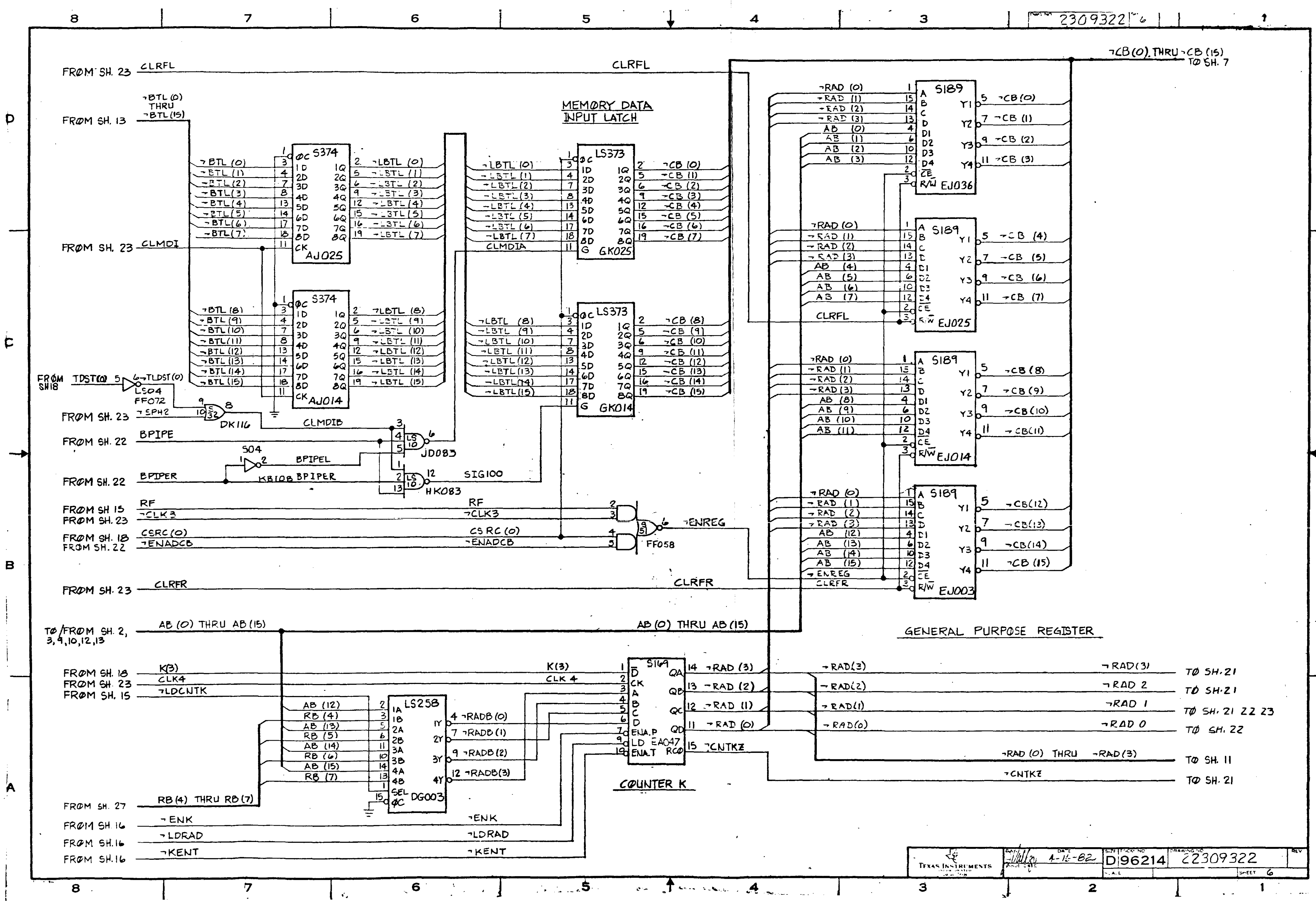
REFERENCE — FOR APPLICATION TO CONTROLLED SPECIFICATIONS SEE TI DRAWING 729467

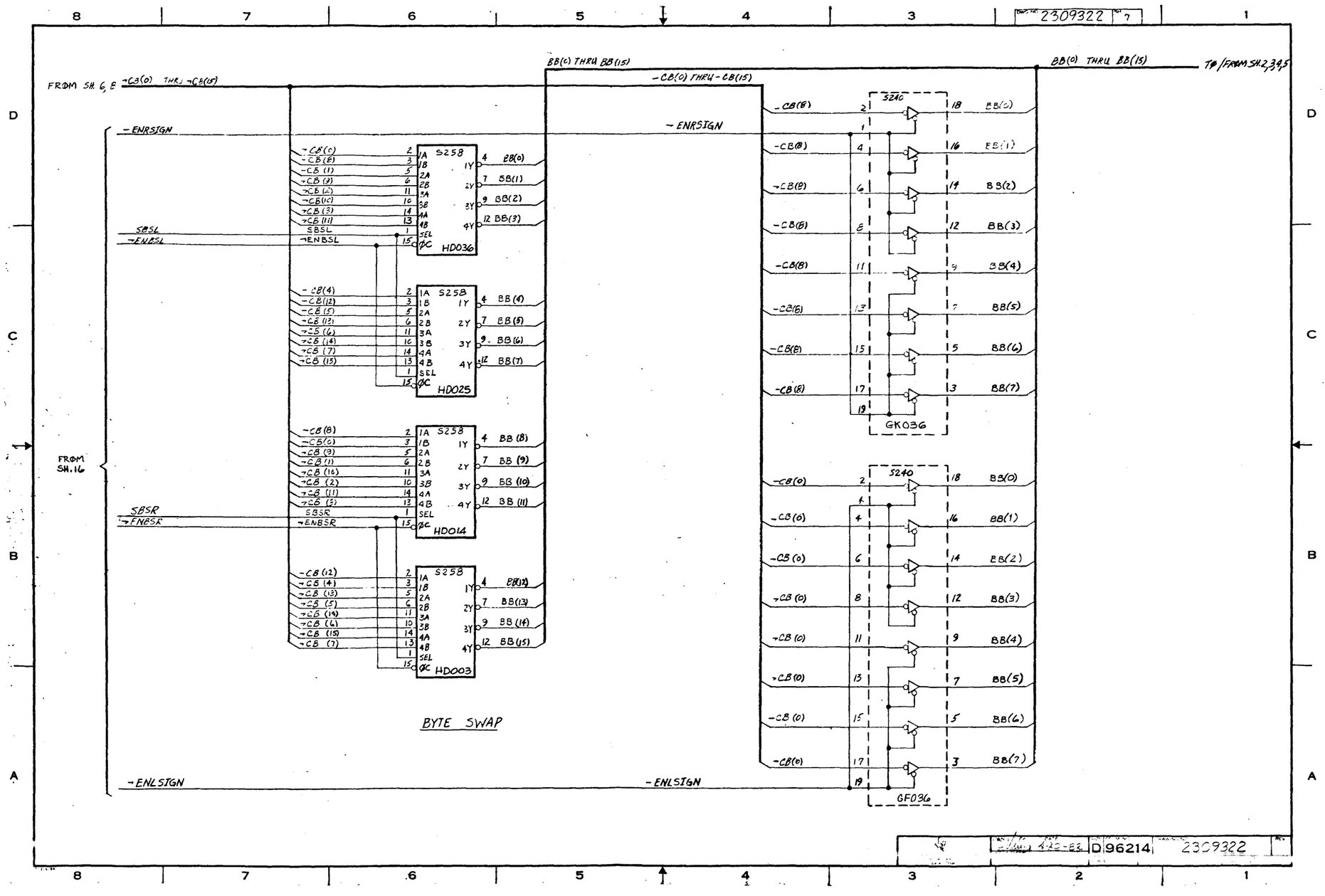

2309322
CCIN(2)
BB(0) THRU BB(7)
TO/FROM SH. 3,4,5,7
FROM SH. 18
FROM SH. 3
FROM SH. 3
NØ SOURCE
NØ SOURCE
ØP(9)
CIN(1)
CCIN(1)
SWR(1)
SXWR(1)
BB(4) THRU BB(7)
ØP(0) THRU ØP(9)
CIN(1)
CCIN(1)
SWR(1)
SXWR(1)
AB(0) THRU AB(3)
S481
FD042
S451
FD029
AGT
LGT
ØVERFLØW
AB(4) THRU AB(7)
AØ(1) THRU AØ(3)
AGT
LST
ØVERFLØW
TØ SH. 4, 21
TØ SH. 4, 21
TØ SH. 4, 21
FROM SH. 17 →MSEC(1)
FROM SH. 17 →MSEC(3)
FROM SH. 18 INC-281
HK083
→INC MC
→INC PC
TØ SH. 3, 15
TØ SH. 3, 15
FK072
AB(0) THRU AB(7)
AØ(0) THRU AØ(7)
TO/FROM SH. 6, 8, 9, 10, 12, 13
TØ SH. 8
Y(2)
X(2)
TØ SH. 3
TØ SH. 3
FROM SH. 3 CIN(2)
NØ SOURCE SWR(3)
FROM SH. 4 SDAT
VCC
RII03
VV05
390
GB056
EQUAL
→LDAC
SWR(2)
SXWR(2)
DØ(0)
DØ(1)
→INCMC
MSRC(1)
→INCPC
CLK481
→ENSUM
FROM SH. 15 →LDAC
FROM SH. 14 DØ(0)
FROM SH. 14 DØ(1)
FROM SH. 18 MSRC(1)
FROM SH. 23 CLK481
FROM SH. 16 →ENSUM
TØ SH 15
CIN(1)
CCIN(1)
SWR(1)
SXWR(1)
→CØUT
TØ SH 3,4,21
FROM SH. 5 →CSAVE
→CØUT
FROM SH. 18 EØI
FROM SH. 18 ØP(10)
FROM SH. 22 →ENCHLD
FROM SH. 22 →ENCSAV
FK083
504
FB094
CØUT
TO SH. 4, 21
→CSAVA
TØ SH. 5
→CINA
TØ SH. 3
TEXAS INSTRUMENTS
D 96214
2309322

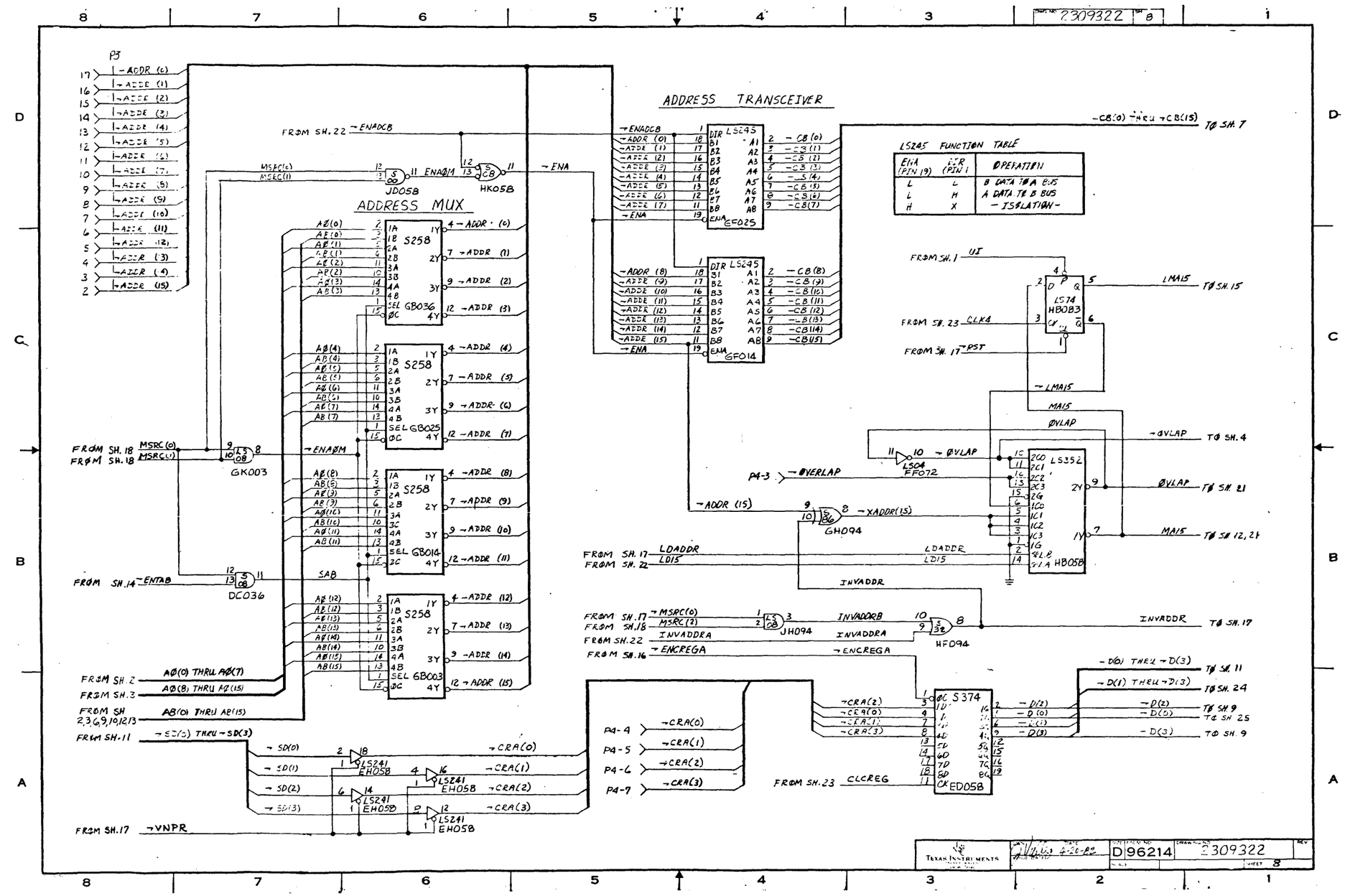

DWG NO 2309322 REV 3
CCIN(0)
CIN(0)
CCIN(1)
BYTE
FROM SH. 18
TO/FROM SH. 2,4,5,7
FROM SH. 18
FROM SH. 2
NO SOURCE
FROM SH. 4
BB(8) THRU BB(15)
ØP(0) THRU ØP(9)
→CINA
SWR(3)
SDAT
AB(8) THRU AB(11)
BB(12) THRU BB(15)
Y(1)
X(1)
FROM SH. 2
S182
GB047
CCIN(1) TO SH. 2
CIN(1) TO SH. 2
CIN(2) TO SH. 2
AB(8) THRU AB(15) TO/FROM SH. 4,8,9,10,12,13
AB(8) THRU AB(15) TO SH. 8
S481
FD016
FD003
G/RG
P/LG
→COUT
DØP3
DØP2
DØP1
DØP0
→CCØ
AØP3
AØP2
AØP1
AØP0
AB(8)
AB(9)
AB(10)
AB(11)
AB(12)
AB(13)
AB(14)
AB(15)
CIN(0)
CCIN(0)
CCIN(1)
AØ(8)
AØ(9)
AØ(10)
AØ(11)
AØ(12)
AØ(13)
AØ(14)
AØ(15)
VCC
DK012 1K
EF012 1K
FG092 1K
EG023 1K RII03 (3)
S00
GF047
AB(15) TO SH. 4,21
NO SOURCE SWR(1)
NO SOURCE SXWR(1)
FROM SH. 18 →BYTE
FROM SH. 2 EQUAL
FROM SH. 15 →LDAC
FROM SH. 14 DØ(0)
FROM SH. 14 DØ(1)
FROM SH. 2 →INCMC
FROM SH. 18 MSRC(1)
FROM SH. 2 →INCPC
FROM SH. 23 CLK481
FROM SH. 16 →ENSUM
TEXAS INSTRUMENTS
D96214
2309322
SHEET 3

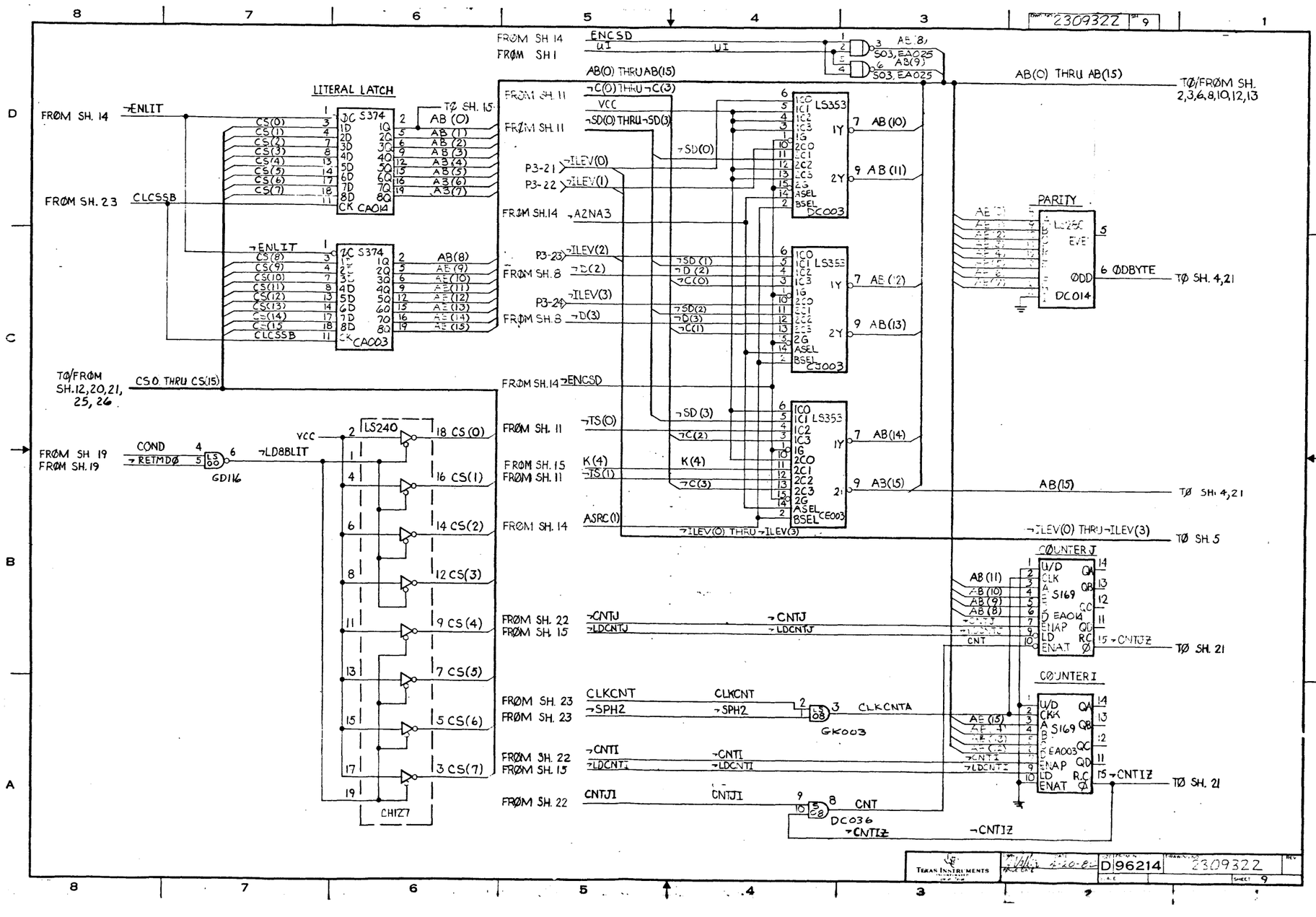

STATUS MUX
FROM SH. 5
T0/FROM SH. 2,3,5,7
FROM SH. 2
FROM SH. 22
FROMSH2
P4-48
P1-60
FROM SH. 8
FROM SH. 9
FROM SH. 18
ST(0) THRU ST(6)
BB(0) THRU BB(6)
LGT
AGT
EQUAL
CRUBITINA
→DIAGCRU
C0UT
→ENCRUIN
→ENDCRU
SDAT
→0VLAP
0VERFLOW
STAT(0) THRU STAT(2)
STAT1
STAT 2
SELOB
SELOA
SEL2C
SEL2B
SEL2A
SEL3C
SEL3B
SEL3A
SEL5B
SEL5A
SEL4C
SEL4B
SEL4A
→LITST
LD8
LDI2
0DBYTE
0NE
ZST(2)
ZAST2
BB(6)
→ST(7)
DST(0)
DST(1)
DST(2)
DST(3)
DST(4)
DST(5)
DST(6)
DST(0) THRU DST(6)
T0 SH. 5
T0 SH. 2, 3
FROM SH. 3,9,10,12,13
AB(15)
→CRU0UT
P4-50
LSI53
LSI51
JB036
JK021
JD094
HF094
LSI25
FF083
FB083
KD029
JB025
JF030
S471
JF008
JF019
S240
KD018
HB105
SST4
TEXAS INSTRUMENTS
D96214
2309322

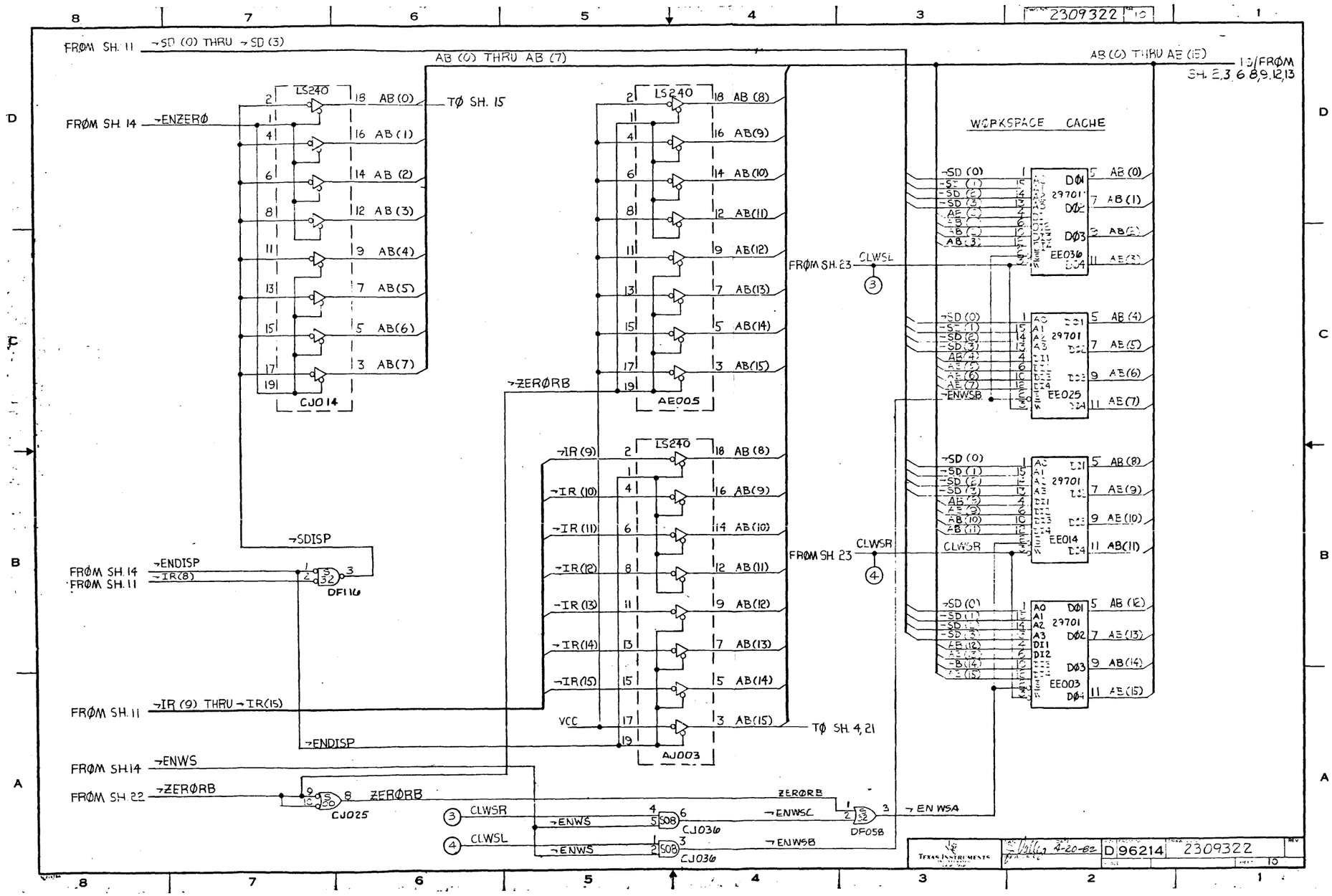

2309322
ST (0) THRU ST (15)
P3-19
¬INTPRES
INTPRES
S240
KD018
¬ST (12) THRU ¬ST (15)
¬ILEV(0) THRU ¬ILEV(3)
FROM SH. 9
S85
JK012
¬PRIORITY
PRIORITY
FROM SH. 1
UI
STATUS REGISTER
DST(0) THRU DST(6)
FROM SH. 4
FROM SH. 2
LS273
JB047
FROM SH. 23
FROM SH. 17
CLK4
LD8
LS378
JB014
LS379
JB003
LD12
BSRC(2)
¬ENST
BB (7) THRU BB (15)
ST (0) THRU ST (6) TO SH. 4
TO SH. 25
TO SH. 2,21
ST(7) TO SH. 21
ST(8) TO SH. 22
ST(11) TO SH. 21
S08
CJ036
OVERFLOWA
FROM SH. 22
¬ZERORB
HK058
¬ENSTA
LS257
HH036
HH025
HH014
HH003
BB (0) THRU BB (15)
TO/FROM SH. 2,3,4,7
S04
JH058
¬OVERFLOW
P4
P3
¬ST (7)
¬ST (8)
¬ST (9)
TO SH. 4
INTPRES
TO SH. 19
PRIORITY
TO SH. 19
TEXAS INSTRUMENTS
D 96214
2309322

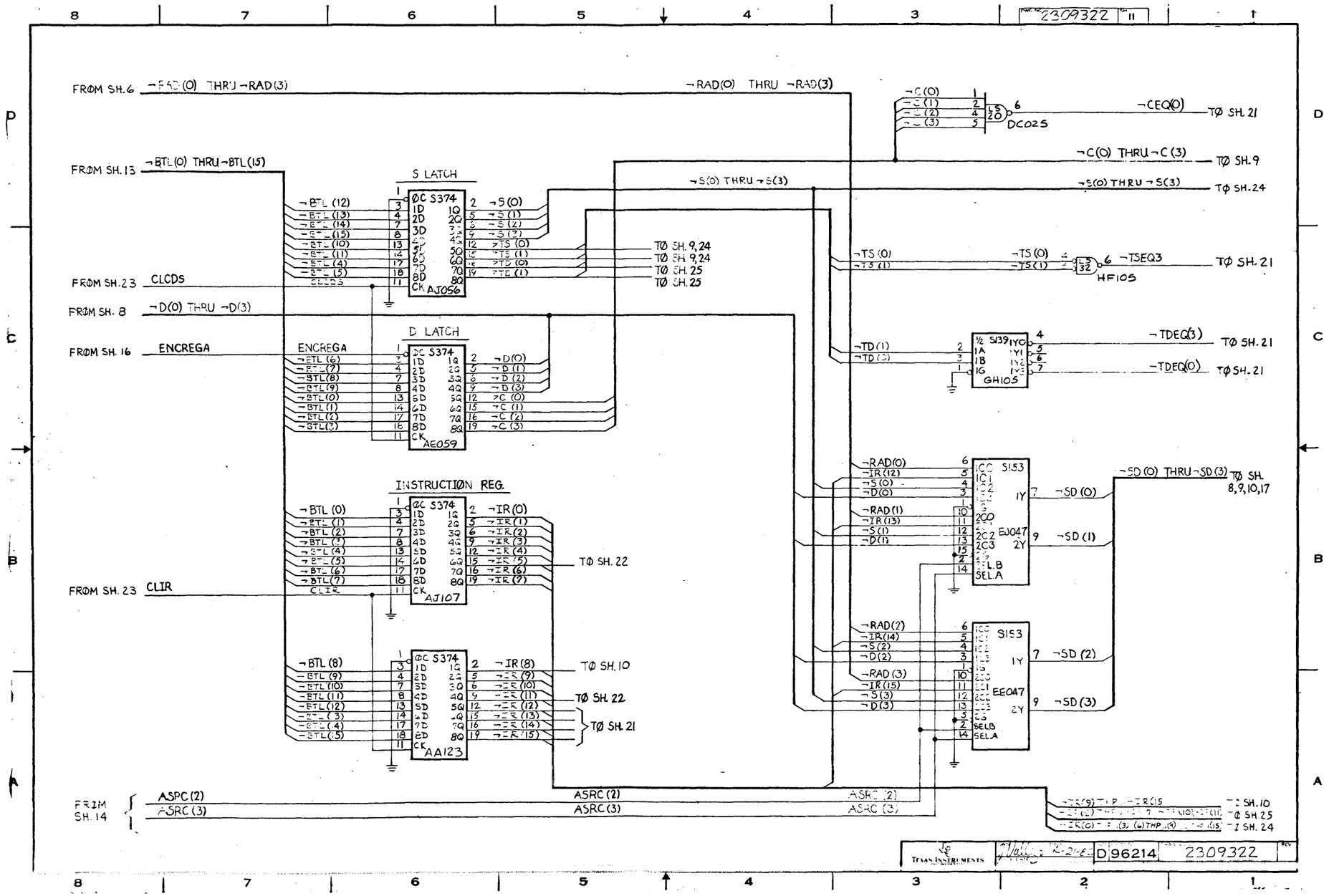

MEMORY DATA INPUT LATCH
GENERAL PURPOSE REGISTER
COUNTER K
D96214
22309322

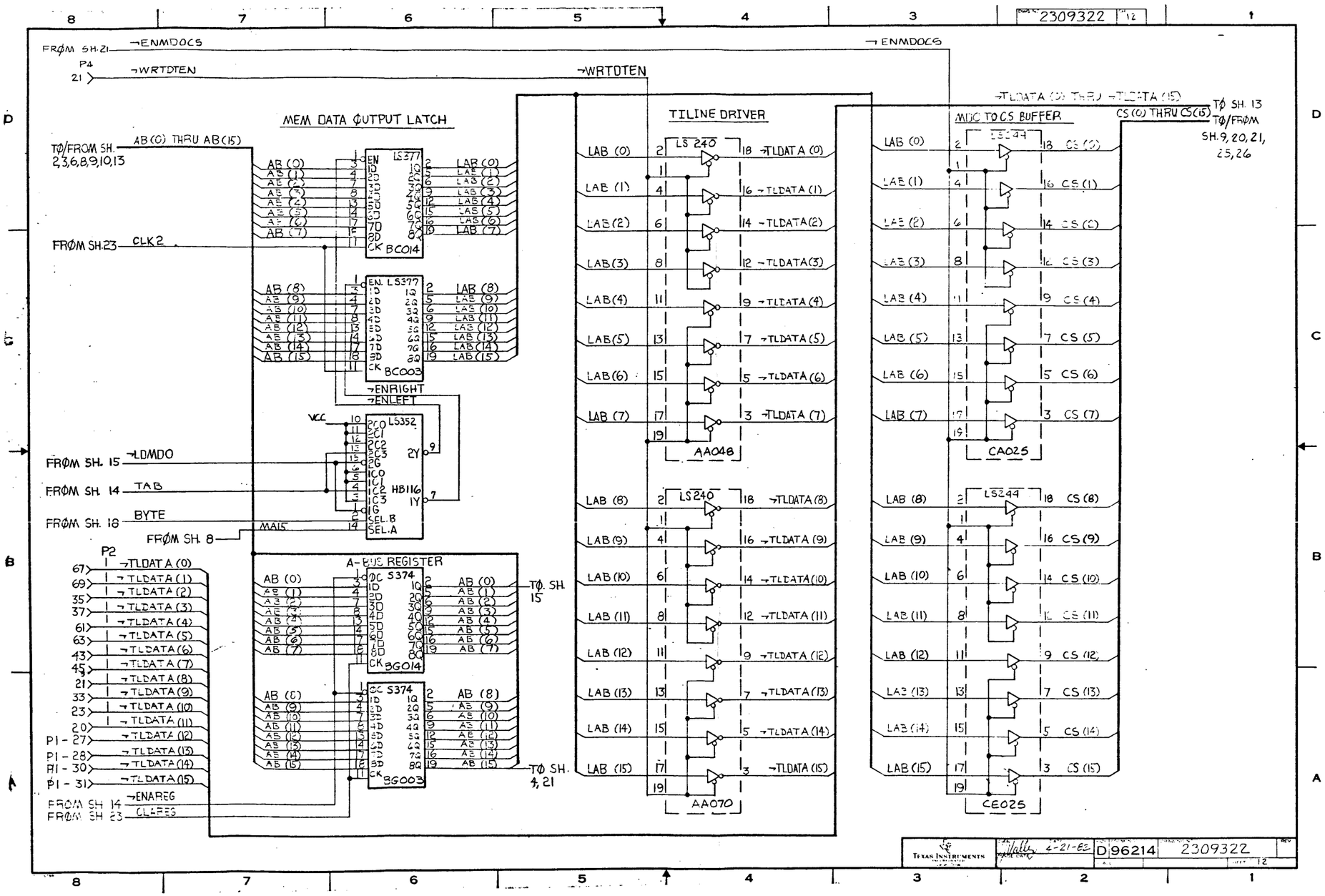

2309322
FROM SH. 6, 8
¬CB(0) THRU ¬CB(15)
BB(0) THRU BB(15)
TO/FROM SH.2,3,4,5
−CB(0) THRU −CB(15)
−ENRSIGN
SBSL
¬ENBSL
SBSR
¬ENBSR
FROM SH.16
−ENLSIGN
S258
HD036
HD025
HD014
HD003
S240
GK036
GF036
BYTE SWAP
4-23-82
D96214
2309322

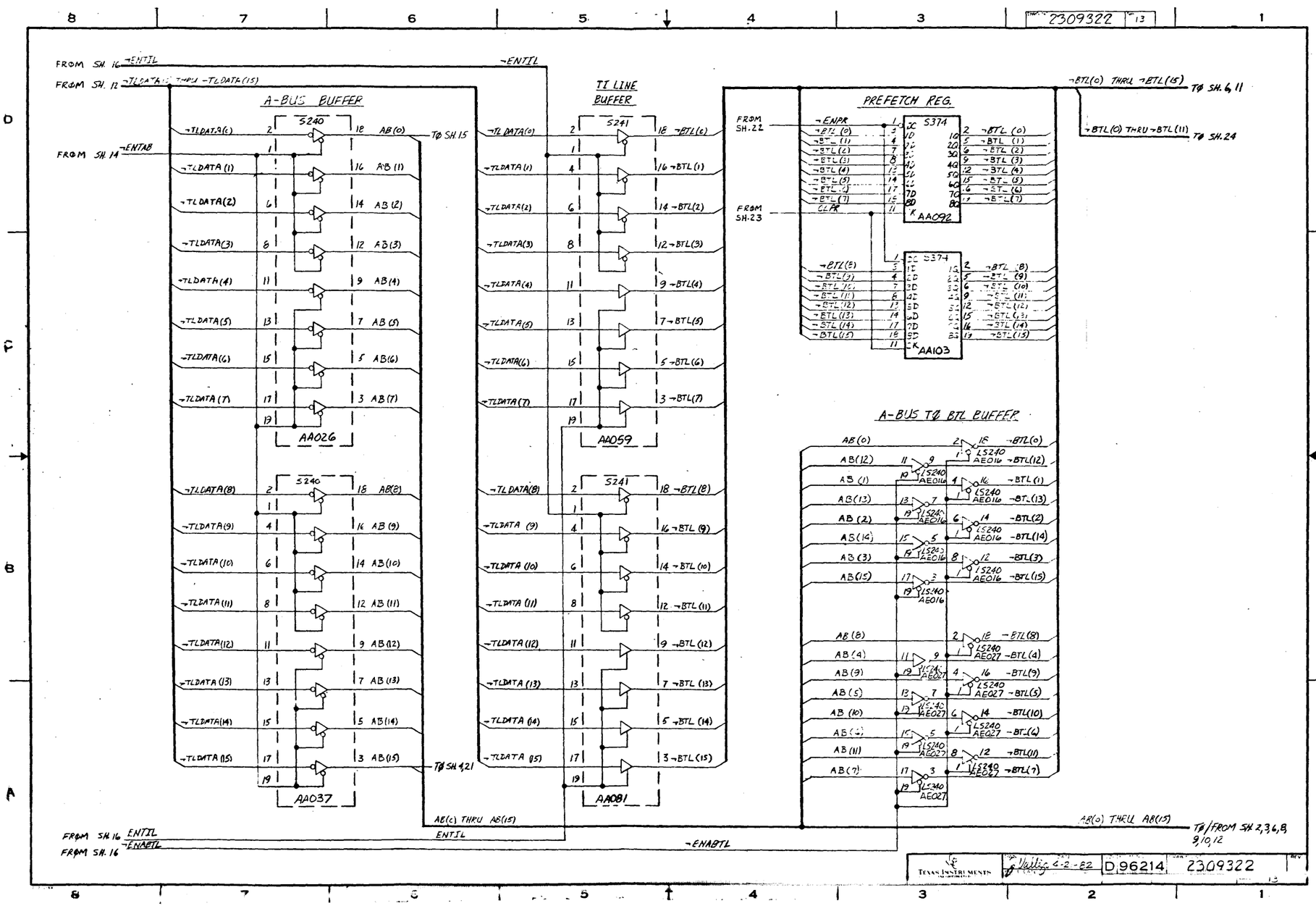

2309322
P3
ADDRESS TRANSCEIVER
ADDRESS MUX
FROM SH. 22 →ENADCB
JD058
HK058
→ENA
S258
GB036
GB025
GB014
GB003
GK003
DC036
FROM SH. 18 MSRC(0)
FROM SH. 18 MSRC(1)
FROM SH. 14 →ENTAB
SAB
FROM SH. 2
FROM SH. 3
FROM SH 2,3,6,9,10,12,13
FROM SH. 11
FROM SH. 17 →VNPR
LS245
GF025
GF014
LS245 FUNCTION TABLE
ENA (PIN 19)
DIR (PIN 1)
OPERATION
B DATA TO A BUS
A DATA TO B BUS
— ISOLATION —
TO SH. 7
FROM SH. 1 UI
LS74
HB083
LMAIS
TO SH. 15
FROM SH. 23 CLK4
FROM SH. 17 →RST
MAIS
ØVLAP
→ØVLAP
TO SH. 4
P4-3 →ØVERLAP
LS04
FF072
LS352
GH094
→XADDR(15)
FROM SH. 17 LDADDR
FROM SH. 22 LDI5
INVADDR
TO SH. 17
FROM SH. 17 →MSRC(0)
FROM SH. 18 MSRC(2)
FROM SH. 22 INVADDRA
FROM SH. 16 →ENCREGA
JH094
HF094
P4-4 →CRA(0)
P4-5 →CRA(1)
P4-6 →CRA(2)
P4-7 →CRA(3)
LS241
EH058
FROM SH. 23 CLCREG
S374
ED058
TO SH. 11
TO SH. 24
TO SH. 9
TO SH. 25
TEXAS INSTRUMENTS
D96214
2309322

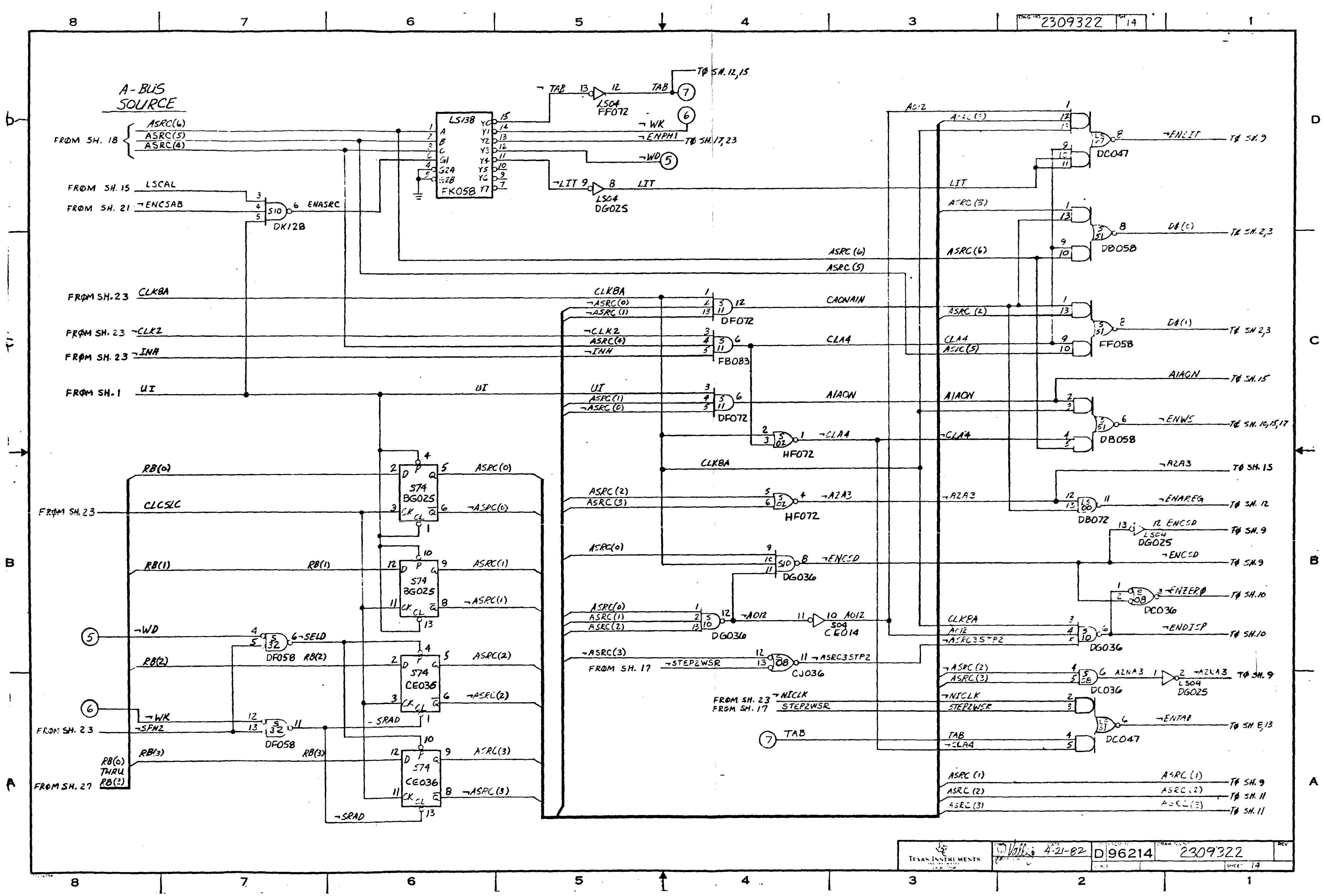

2309322
LITERAL LATCH
FROM SH. 14 ¬ENLIT
FROM SH. 23 CLCSSB
CS(0) THRU CS(15)
TO/FROM SH. 12,20,21, 25, 26
FROM SH 19 COND
FROM SH. 19 ¬RETMDØ
GD116
¬LDBBLIT
VCC
LS240
CHIZ7
FROM SH. 14 ENCSD
FROM SH 1 UI
AB(0) THRU AB(15)
FROM SH. 11 ¬C(0) THRU ¬C(3)
VCC
¬SD(0) THRU ¬SD(3)
P3-21 ¬ILEV(0)
P3-22 ¬ILEV(1)
FROM SH. 14 ¬A2NA3
P3-23 ¬ILEV(2)
FROM SH. 8 ¬D(2)
P3-24 ¬ILEV(3)
FROM SH. 8 ¬D(3)
FROM SH. 14 ¬ENCSD
FROM SH. 11 ¬TS(0)
FROM SH. 15 FROM SH. 11 K(4) ¬TS(1)
FROM SH. 14 ASRC(1)
FROM SH. 22 FROM SH. 15 ¬CNTJ ¬LDCNTJ
FROM SH. 23 FROM SH. 23 CLKCNT ¬SPH2
FROM SH. 22 FROM SH. 15 ¬CNTI ¬LDCNTI
FROM SH. 22 CNTJI
DC036
¬CNTIZ
AB(0) THRU AB(15)
TO/FROM SH. 2,3,6,8,10,12,13
PARITY
TO SH. 4,21
¬ILEV(0) THRU ¬ILEV(3)
TO SH. 5
COUNTER J
COUNTER I
TO SH. 21
TEXAS INSTRUMENTS
D 96214
2309322

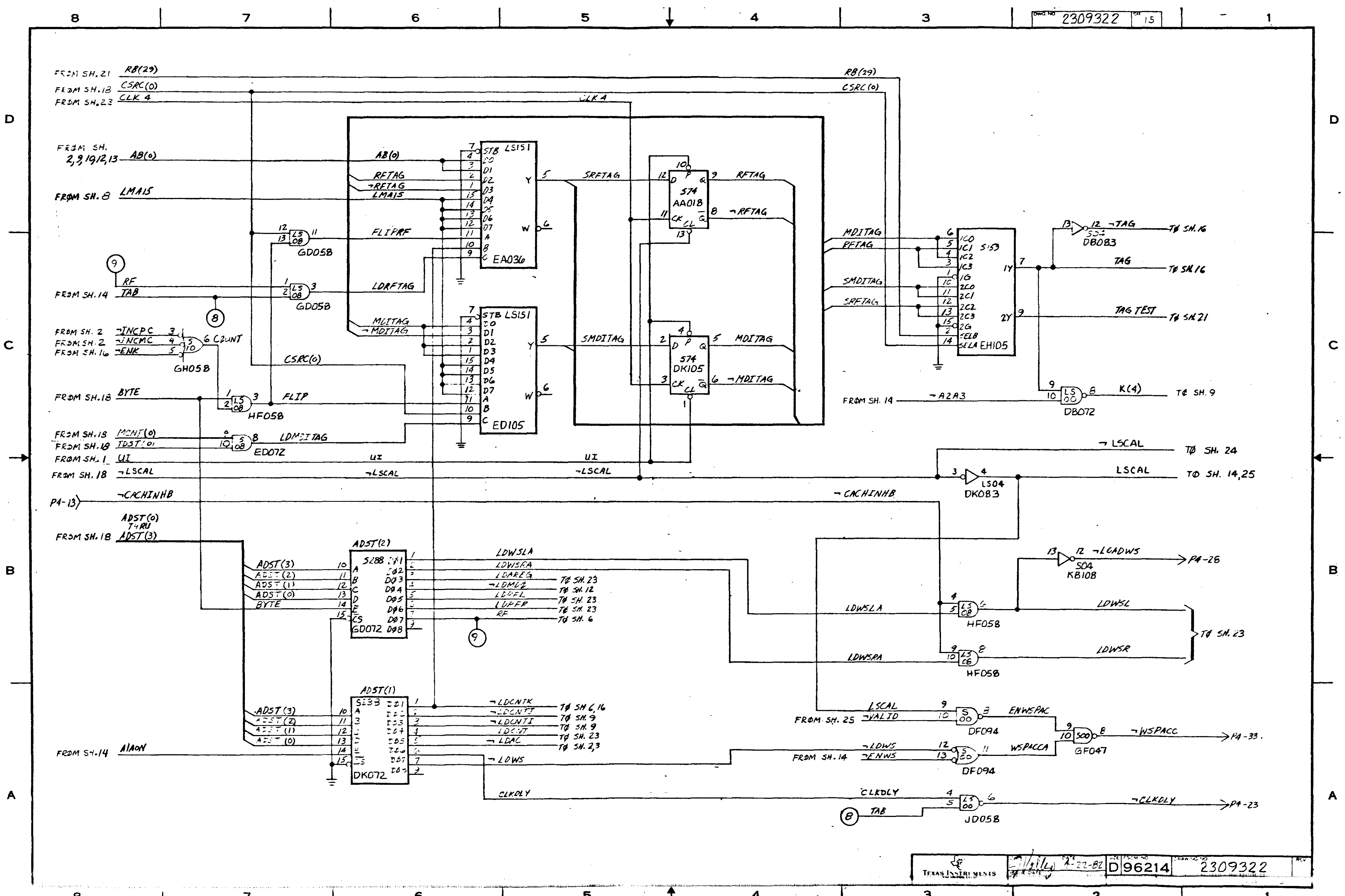

2309322
FROM SH. 11 →SD (0) THRU →SD (3)
AB (0) THRU AB (7)
AB (0) THRU AB (15)
13/FROM SH. 2,3,6,8,9,12,13
FROM SH. 14 →ENZERØ
TØ SH. 15
LS240
CJ014
AE005
AJ003
→ZERØRB
→IR (9)
→IR (10)
→IR (11)
→IR (12)
→IR (13)
→IR (14)
→IR (15)
VCC
TØ SH. 4, 21
WØRKSPACE CACHE
EE036
EE025
EE014
EE003
29701
FROM SH. 23 CLWSL
CLWSR
→ENWSB
→SDISP
FROM SH. 14 →ENDISP
FROM SH. 11 →IR(8)
DF116
FROM SH. 11 →IR (9) THRU →IR(15)
→ENDISP
FROM SH. 14 →ENWS
FROM SH. 22 →ZERØRB
CJ025
ZERØRB
CLWSR
CLWSL
→ENWS
CJ036
→ENWSC
→ENWSB
DF058
→ENWSA
Texas Instruments
D 96214
2309322
REV
SHEET 10

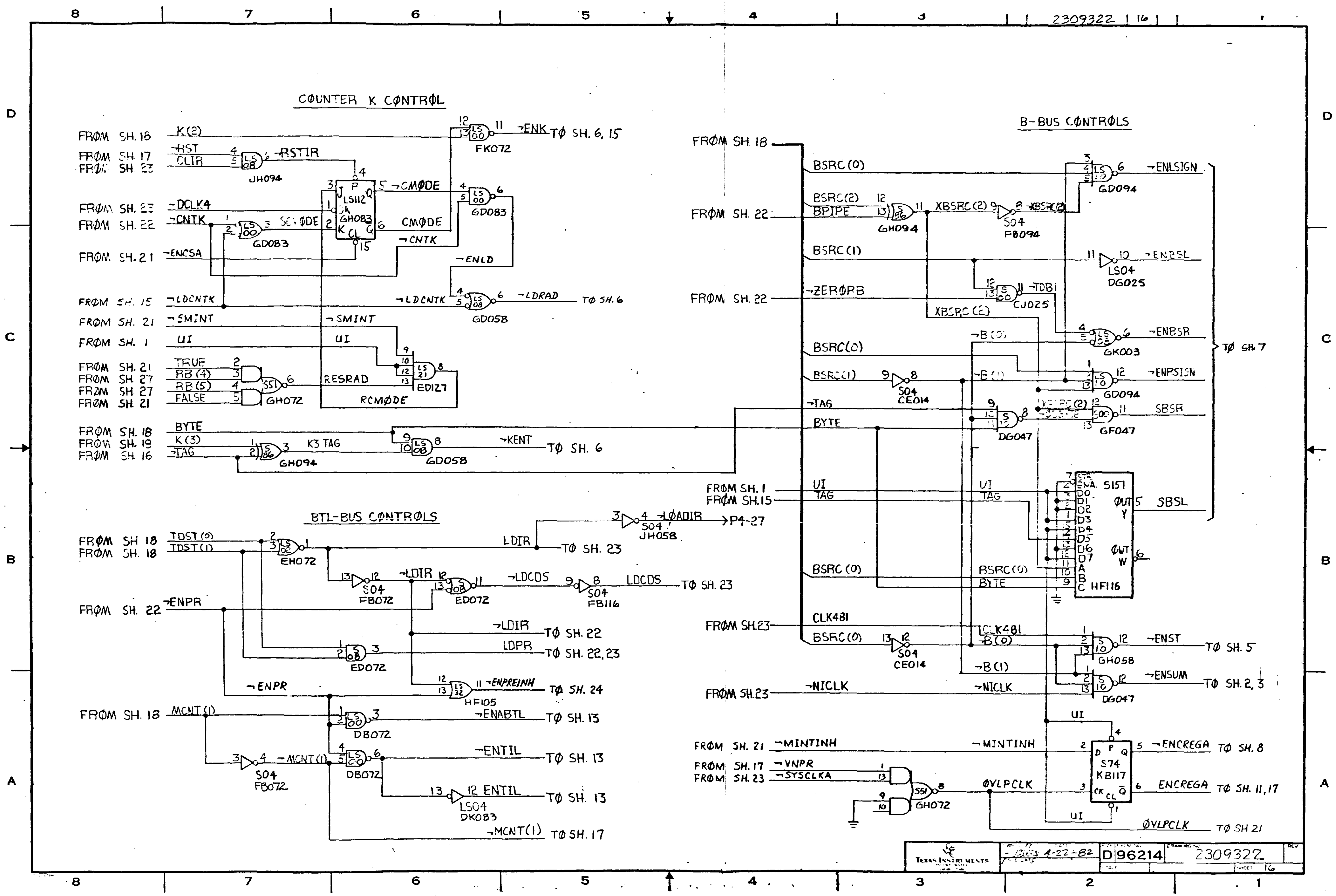

2309322 11
FROM SH.6 ¬RAD(0) THRU ¬RAD(3)
¬RAD(0) THRU ¬RAD(3)
FROM SH.13 ¬BTL(0) THRU ¬BTL(15)
S LATCH
¬BTL (12)
¬BTL (13)
¬BTL (14)
¬BTL (15)
¬BTL (10)
¬BTL (11)
¬BTL (4)
¬BTL (5)
CLCDS
¬S(0)
¬S(1)
¬S(2)
¬S(3)
TS (0)
TS (1)
AJ056
TØ SH. 9,24
TØ SH. 9,24
TØ SH. 25
TØ SH. 25
FROM SH.23 CLCDS
FROM SH. 8 ¬D(0) THRU ¬D(3)
FROM SH. 16 ENCREGA
D LATCH
ENCREGA
¬BTL (6)
¬BTL (7)
¬BTL(8)
¬BTL(9)
¬BTL(0)
¬BTL(1)
¬BTL(2)
¬BTL(3)
S374
¬D(0)
¬D(1)
¬D(2)
¬D(3)
¬C(0)
¬C(1)
¬C(2)
¬C(3)
AE059
INSTRUCTIØN REG.
¬BTL (0)
¬BTL (1)
¬BTL (2)
¬BTL (3)
¬BTL (4)
¬BTL (5)
¬BTL (6)
¬BTL(7)
CLIR
¬IR(0)
¬IR(1)
¬IR(2)
¬IR(3)
¬IR(4)
¬IR(5)
¬IR(6)
¬IR(7)
AJ107
TØ SH. 22
FROM SH. 23 CLIR
¬BTL (8)
¬BTL (9)
¬BTL(10)
¬BTL(11)
¬BTL(12)
¬BTL(3)
¬BTL(4)
¬BTL(5)
¬IR(8)
¬IR(9)
¬IR(10)
¬IR(11)
¬IR(12)
¬IR(13)
¬IR(14)
¬IR(15)
AA123
TØ SH. 10
TØ SH. 22
TØ SH. 21
¬C(0)
¬C(1)
¬C(2)
¬C(3)
LS20
DC025
¬CEQ(0)
TØ SH. 21
¬C(0) THRU ¬C(3)
TØ SH. 9
¬S(0) THRU ¬S(3)
TØ SH. 24
¬TS(0)
¬TS(1)
LS32
HF105
¬TSEQ3
TØ SH. 21
¬TD(1)
¬TD(2)
½ S139
GH105
¬TDEQ(3)
TØ SH. 21
¬TDEQ(0)
TØ SH. 21
¬RAD(0)
¬IR(12)
¬S(0)
¬D(0)
¬RAD(1)
¬IR(13)
¬S(1)
¬D(1)
¬RAD(2)
¬IR(14)
¬S(2)
¬D(2)
¬RAD(3)
¬IR(15)
¬S(3)
¬D(3)
S153
EJ047
EE047
SEL.B
SEL.A
¬SD(0)
¬SD(1)
¬SD(2)
¬SD(3)
¬SD(0) THRU ¬SD(3) TØ SH. 8,9,10,17
FROM SH. 14 ASRC(2) ASRC(3)
ASRC(2)
ASRC(3)
TEXAS INSTRUMENTS
D 96214
2309322

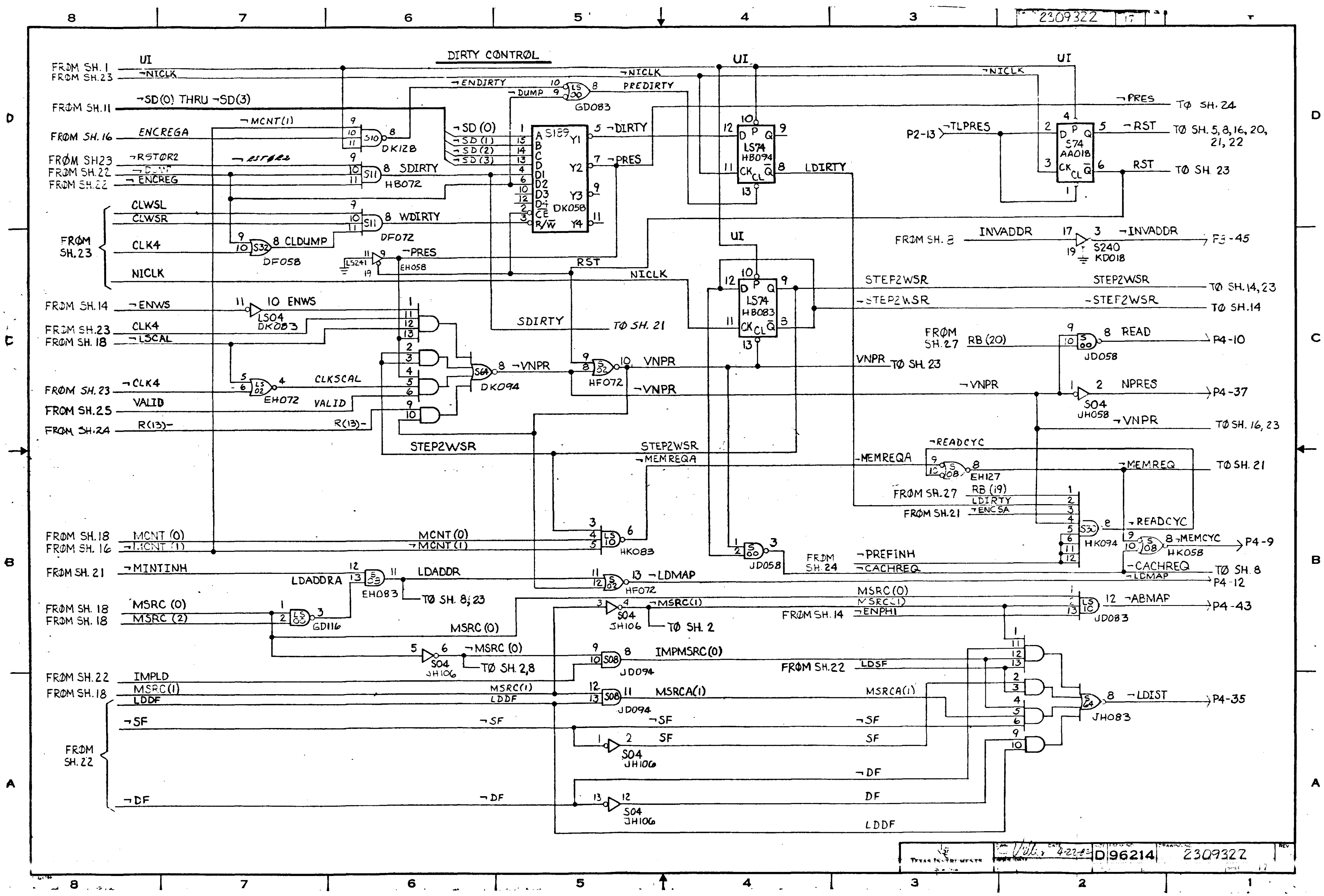

2309322
FROM SH.21 →ENMDOCS
P4 21 →WRTDTEN
→ENMDOCS
→WRTDTEN
MEM DATA OUTPUT LATCH
TILINE DRIVER
MDC TO CS BUFFER
→TLDATA (0) THRU →TLDATA (15)
CS(0) THRU CS(15)
TO SH. 13
TO/FROM SH. 9, 20, 21, 25, 26
TO/FROM SH. 2,3,6,8,9,10,13
AB(0) THRU AB(15)
FROM SH.23 CLK2
LS377
BC014
BC003
→ENRIGHT
→ENLEFT
LS352
HB116
FROM SH. 15 →LDMDO
FROM SH. 14 TAB
FROM SH. 18 BYTE
FROM SH. 8 MAIS
A-BUS REGISTER
LS374
BG014
BG003
TO SH. 15
TO SH. 4, 21
P2
P1-27 →TLDATA(12)
P1-28 →TLDATA(13)
P1-30 →TLDATA(14)
P1-31 →TLDATA(15)
FROM SH 14 →ENAREG
FROM SH 23 CLAREG
LS 240
AA048
AA070
LS244
CA025
CE025
TEXAS INSTRUMENTS
D 96214
2309322

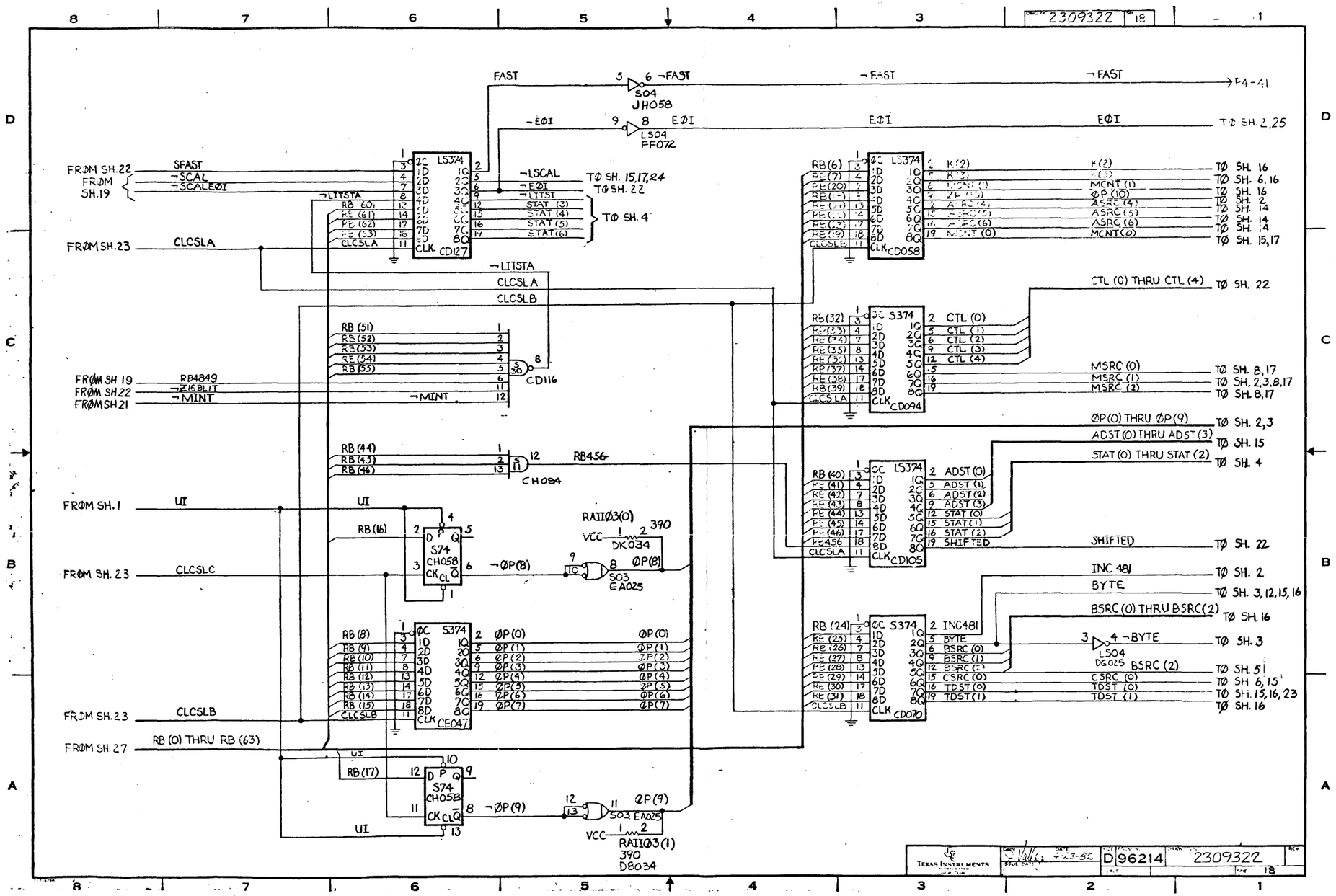

2309322 13
FROM SH. 16 ¬ENTIL
FROM SH. 12 ¬TLDATA(0) THRU ¬TLDATA(15)
A-BUS BUFFER
S240
¬TLDATA(0) 2 18 AB(0) TO SH.15
FROM SH. 14 ¬ENTAB 1
¬TLDATA(1) 16 AB(1)
¬TLDATA(2) 6 14 AB(2)
¬TLDATA(3) 8 12 AB(3)
¬TLDATA(4) 11 9 AB(4)
¬TLDATA(5) 13 7 AB(5)
¬TLDATA(6) 15 5 AB(6)
¬TLDATA(7) 17 3 AB(7)
19
AA026
¬TLDATA(8) 2 18 AB(8)
¬TLDATA(9) 4 16 AB(9)
¬TLDATA(10) 6 14 AB(10)
¬TLDATA(11) 8 12 AB(11)
¬TLDATA(12) 11 9 AB(12)
¬TLDATA(13) 13 7 AB(13)
¬TLDATA(14) 15 5 AB(14)
¬TLDATA(15) 17 3 AB(15)
TO SH.9,21
AA037
¬ENTIL
TI LINE BUFFER
S241
¬TLDATA(0) 2 18 ¬BTL(0)
¬TLDATA(1) 4 16 ¬BTL(1)
¬TLDATA(2) 6 14 ¬BTL(2)
¬TLDATA(3) 8 12 ¬BTL(3)
¬TLDATA(4) 11 9 ¬BTL(4)
¬TLDATA(5) 13 7 ¬BTL(5)
¬TLDATA(6) 15 5 ¬BTL(6)
¬TLDATA(7) 17 3 ¬BTL(7)
19
AA059
¬TLDATA(8) 2 18 ¬BTL(8)
¬TLDATA(9) 4 16 ¬BTL(9)
¬TLDATA(10) 6 14 ¬BTL(10)
¬TLDATA(11) 8 12 ¬BTL(11)
¬TLDATA(12) 11 9 ¬BTL(12)
¬TLDATA(13) 13 7 ¬BTL(13)
¬TLDATA(14) 15 5 ¬BTL(14)
¬TLDATA(15) 17 3 ¬BTL(15)
19
AA081
AB(0) THRU AB(15)
ENTIL
¬ENABTL
FROM SH.16 ENTIL
FROM SH.16 ¬ENABTL
PREFETCH REG.
FROM SH.22
¬ENPR 1
¬BTL(0) 3
¬BTL(1) 4
¬BTL(2) 7
¬BTL(3) 8
¬BTL(4) 13
¬BTL(5) 14
¬BTL(6) 17
¬BTL(7) 18
CLR 11
S374
1Q 2
2Q 5
3Q 6
4Q 9
5Q 12
6Q 15
7Q 16
8Q 19
AA092
FROM SH.23
¬BTL(8) 3
¬BTL(9) 4
¬BTL(10) 7
¬BTL(11) 8
¬BTL(12) 13
¬BTL(13) 14
¬BTL(14) 17
¬BTL(15) 18
AA103
¬BTL(0) THRU ¬BTL(15) TO SH.6,11
¬BTL(0) THRU ¬BTL(11) TO SH.24
A-BUS TO BTL BUFFER
AB(0) 2 18 ¬BTL(0)
AB(12) 11 9 ¬BTL(12)
AB(1) 4 16 ¬BTL(1)
AB(13) 7 13 ¬BTL(13)
AB(2) 6 14 ¬BTL(2)
AB(14) 5 15 ¬BTL(14)
AB(3) 8 12 ¬BTL(3)
AB(15) 3 17 ¬BTL(15)
LS240 AE016
AB(8) 2 18 ¬BTL(8)
AB(4) 11 9 ¬BTL(4)
AB(9) 4 16 ¬BTL(9)
AB(5) 7 13 ¬BTL(5)
AB(10) 6 14 ¬BTL(10)
AB(6) 5 15 ¬BTL(6)
AB(11) 8 12 ¬BTL(11)
AB(7) 3 17 ¬BTL(7)
LS240 AE027
AB(0) THRU AB(15) TO/FROM SH 2,3,6,8 9,10,12
TEXAS INSTRUMENTS
Whitig 4-2-82
D96214 2309322 REV
8 7 6 5 4 3 2 1

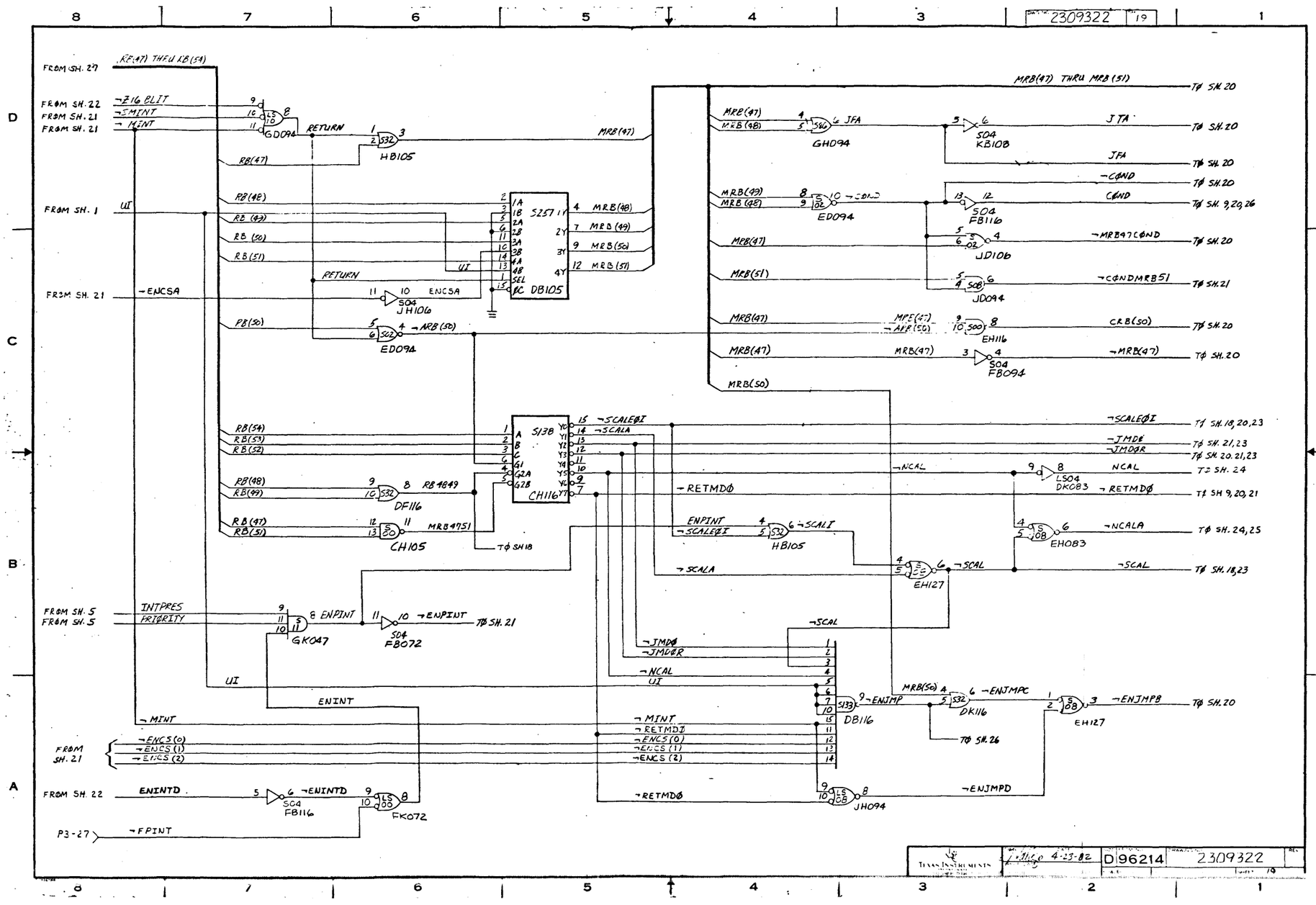

A-BUS SOURCE
2309322
14
TEXAS INSTRUMENTS
4-21-82
D 96214
2309322
LS138
FK058
DK128
DC047
DB058
FF058
DF072
FB083
HF072
DG036
CE014
CJ036
DC036
DC047
574
BG025
CE036
DF058
FROM SH. 18
FROM SH. 15
FROM SH. 21
FROM SH. 23
FROM SH. 1
FROM SH. 17
FROM SH. 27

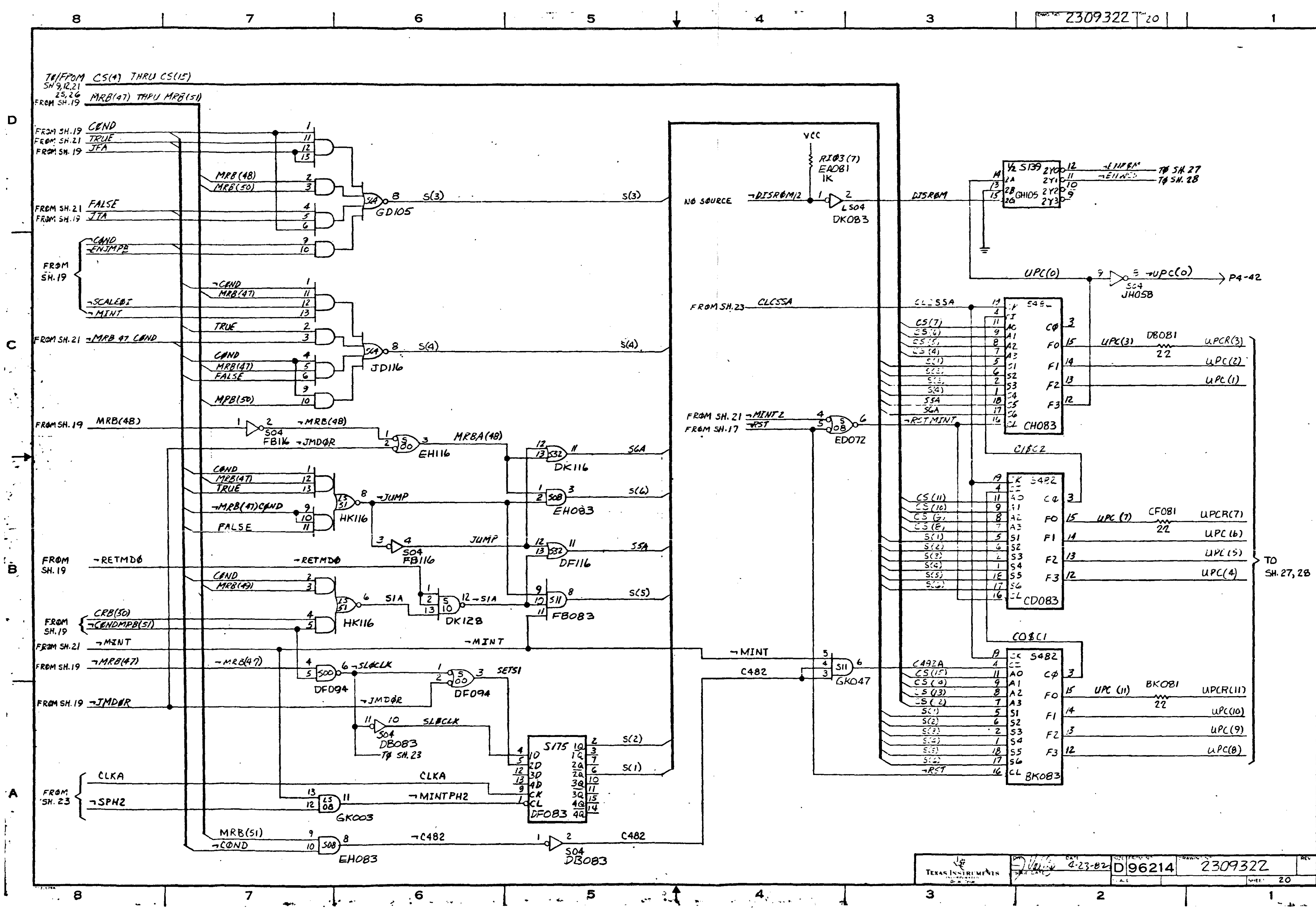

2309322
LS151
EA036
ED105
S74
AA018
DK105
S153
EH105
S288
GD072
S133
DK072
TEXAS INSTRUMENTS
D 96214
2309322

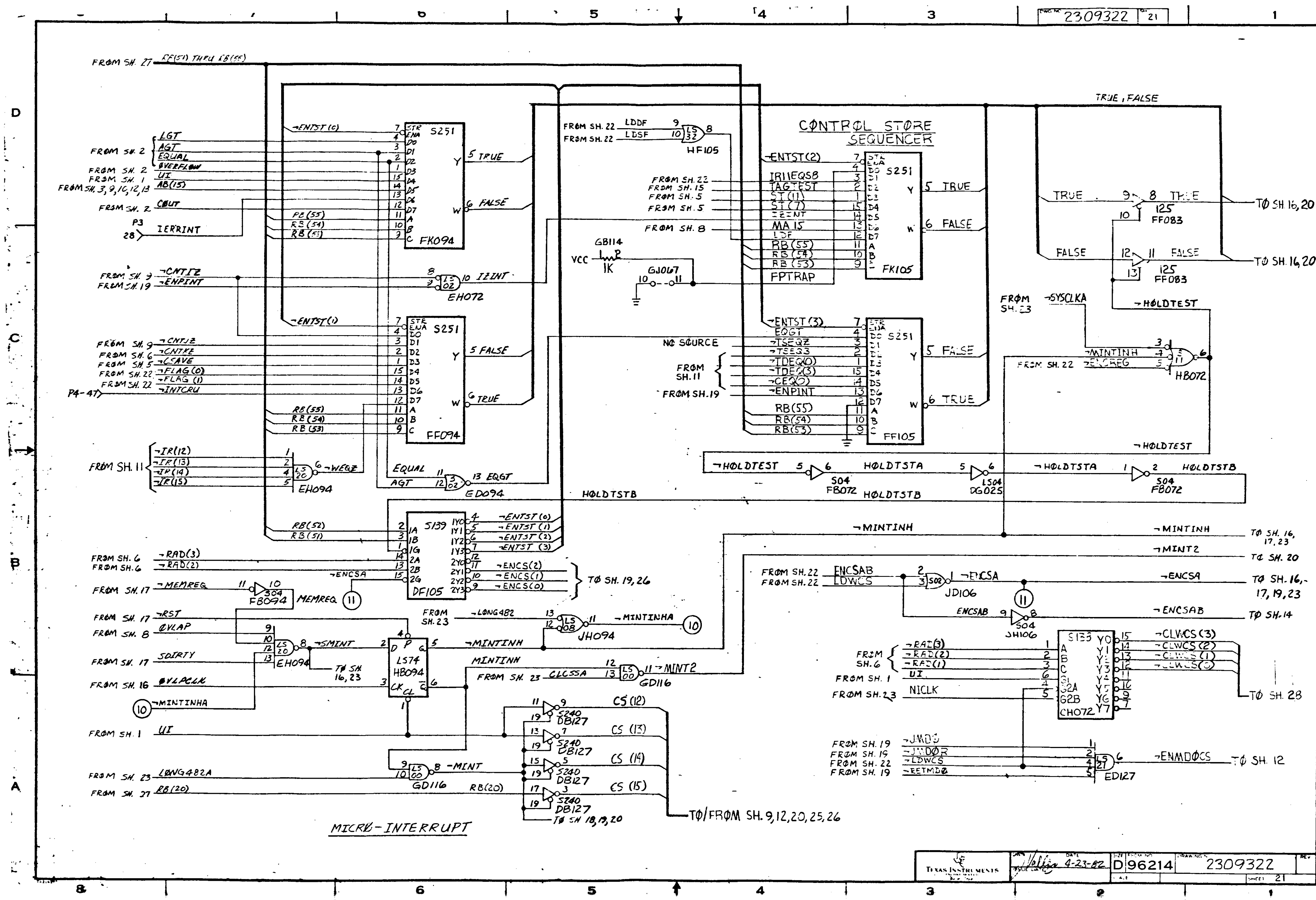

2309322 16
COUNTER K CONTROL
FROM SH. 18 K(2)
¬ENK TO SH. 6, 15
FK072
¬RSTIR
GH094
¬CMODE
GD083
CMODE
¬CNTK
GD083
¬ENLD
¬LDRAD TO SH. 6
GD058
FROM SH. 21 ¬SMINT
FROM SH. 1 UI
RESRAD
RCMODE
ED127
GH072
BYTE
K(3)
¬TAG
K3 TAG
¬KENT TO SH. 6
GH094
GD058
BTL-BUS CONTROLS
FROM SH 18 TDST(0)
FROM SH. 18 TDST(1)
EH072
LDIR TO SH. 23
¬LOADIR P4-27
JH058
¬LDIR
¬LDCDS
LDCDS TO SH. 23
FB072
ED072
FB116
FROM SH. 22 ¬ENPR
¬LDIR TO SH. 22
LDPR TO SH. 22, 23
ED072
¬ENPR
¬ENPREINH TO SH. 24
HF105
FROM SH. 18 MCNT(1)
¬ENABTL TO SH. 13
DB072
¬MCNT(1)
¬ENTIL TO SH. 13
FB072
DB072
12 ENTIL TO SH. 13
DK083
¬MCNT(1) TO SH. 17
B-BUS CONTROLS
FROM SH. 18
BSRC(0)
¬ENLSIGN
GD094
FROM SH. 22
BPIPE
XBSRC(2)
GH094
FB094
BSRC(1)
¬ENBSL
DG025
CJ025
FROM SH. 22 ¬ZEROPB
¬ENBSR
GK003
TO SH. 7
¬ENPSIGN
GD094
CE014
¬TAG
BYTE
SBSR
DG047
GF047
FROM SH. 1 UI
FROM SH. 15 TAG
S157
SBSL
HF116
BSRC(0)
BYTE
FROM SH. 23 CLK481
¬ENST TO SH. 5
GH058
CE014
¬B(1)
¬ENSUM TO SH. 2, 3
FROM SH. 23 ¬NICLK
DG047
UI
FROM SH. 21 ¬MINTINH
¬ENCREGA TO SH. 8
FROM SH. 17 ¬VNPR
FROM SH. 23 ¬SYSCLKA
S74
KB117
ENCREGA TO SH. 11, 17
OVLPCLK
GH072
OVLPCLK TO SH 21
TEXAS INSTRUMENTS
4-22-82
D 96214
2309322
16

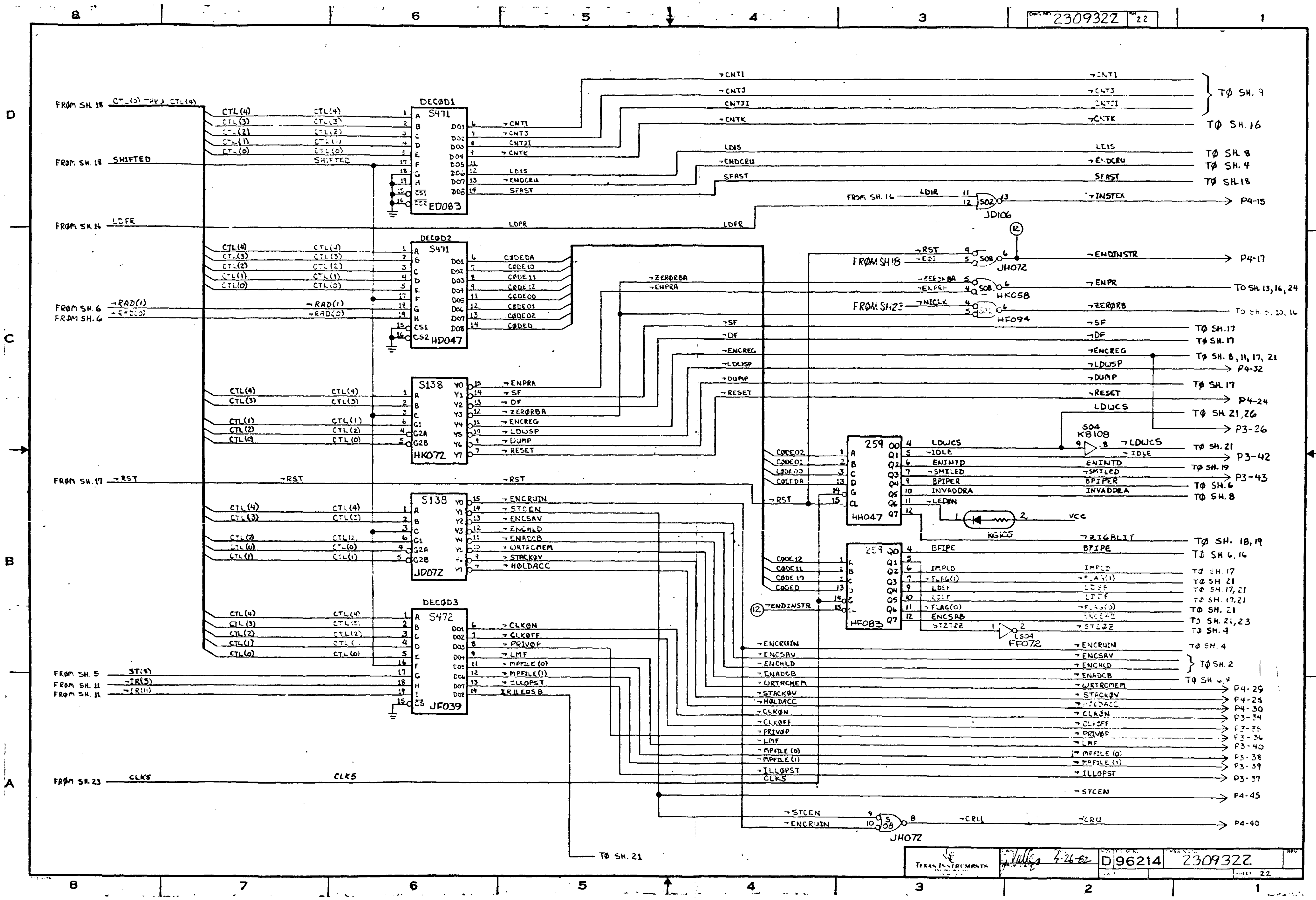

DIRTY CONTROL
D96214
2309322

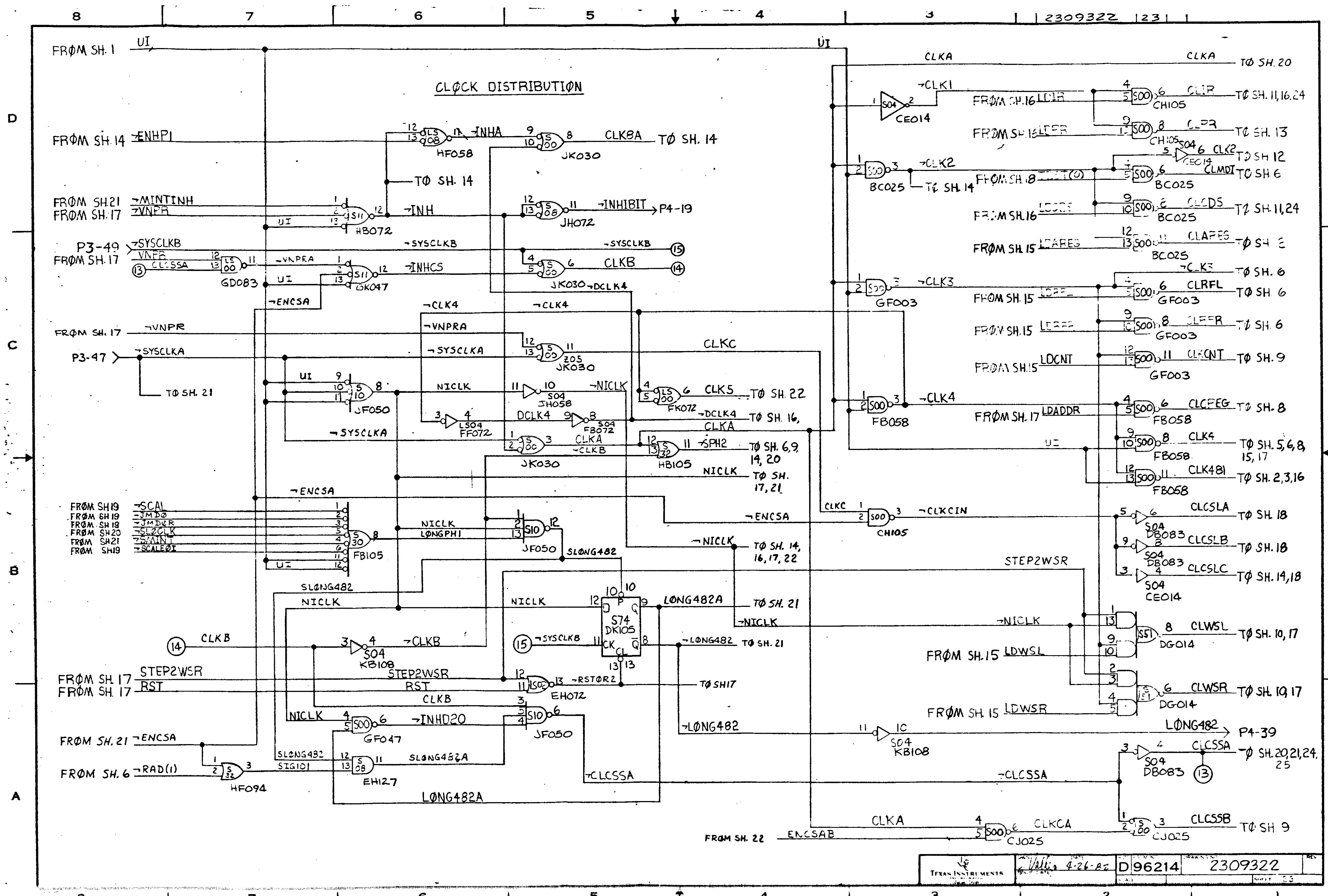

2309322 18
FAST
S04 JH058
¬FAST
→P4-41
¬EØI
LS04 FF072
EØI
TØ SH. 2,25
FROM SH.22
FROM SH.19
SFAST
¬SCAL
¬SCALEØI
¬LITSTA
CLCSLA
FROMSH.23
¬LSCAL
TØ SH. 15,17,24
TØ SH. 22
TØ SH. 4
LS374
CD127
RB(6)
TØ SH. 16
TØ SH. 6, 16
TØ SH. 16
TØ SH. 2
TØ SH. 14
TØ SH. 14
TØ SH. 14
TØ SH. 15,17
CD058
CLCSLB
CTL (0) THRU CTL (4)
TØ SH. 22
RB(32)
CD094
RB (51)
FRØM SH 19
FRØM SH.22
FRØMSH21
RB4849
¬16BLIT
¬MINT
CD116
MSRC (0)
MSRC (1)
MSRC (2)
TØ SH. 8,17
TØ SH. 2,3,8,17
TØ SH. 8,17
ØP(0) THRU ØP(9)
TØ SH. 2,3
ADST(0) THRU ADST(3)
TØ SH. 15
STAT(0) THRU STAT(2)
TØ SH. 4
RB (44)
RB (43)
RB (46)
RB456
CH094
RB(40)
CD105
SHIFTED
TØ SH. 22
FROM SH. 1
UI
RB(16)
RAIIØ3(0)
390
DK034
FROM SH. 23
CLCSLC
S74 CH058
¬ØP(8)
S03 EA025
ØP(8)
INC 481
TØ SH. 2
BYTE
TØ SH. 3, 12, 15, 16
BSRC(0) THRU BSRC(2)
TØ SH. 16
RB (24)
CD070
L504 DG025
¬BYTE
TØ SH. 3
BSRC (2)
TØ SH. 5
CSRC (0)
TDST (0)
TDST (1)
TØ SH 6, 15
TØ SH. 15, 16, 23
TØ SH. 16
RB (8)
ØP(0)
ØP(1)
ØP(2)
ØP(3)
ØP(4)
ØP(5)
ØP(6)
ØP(7)
CE047
FRØM SH.23
CLCSLB
FROM SH.27
RB (0) THRU RB (63)
RB(17)
¬ØP(9)
ØP(9)
S03 EA025
RAII03(1)
390
DB034
TEXAS INSTRUMENTS
D 96214
2309322
18

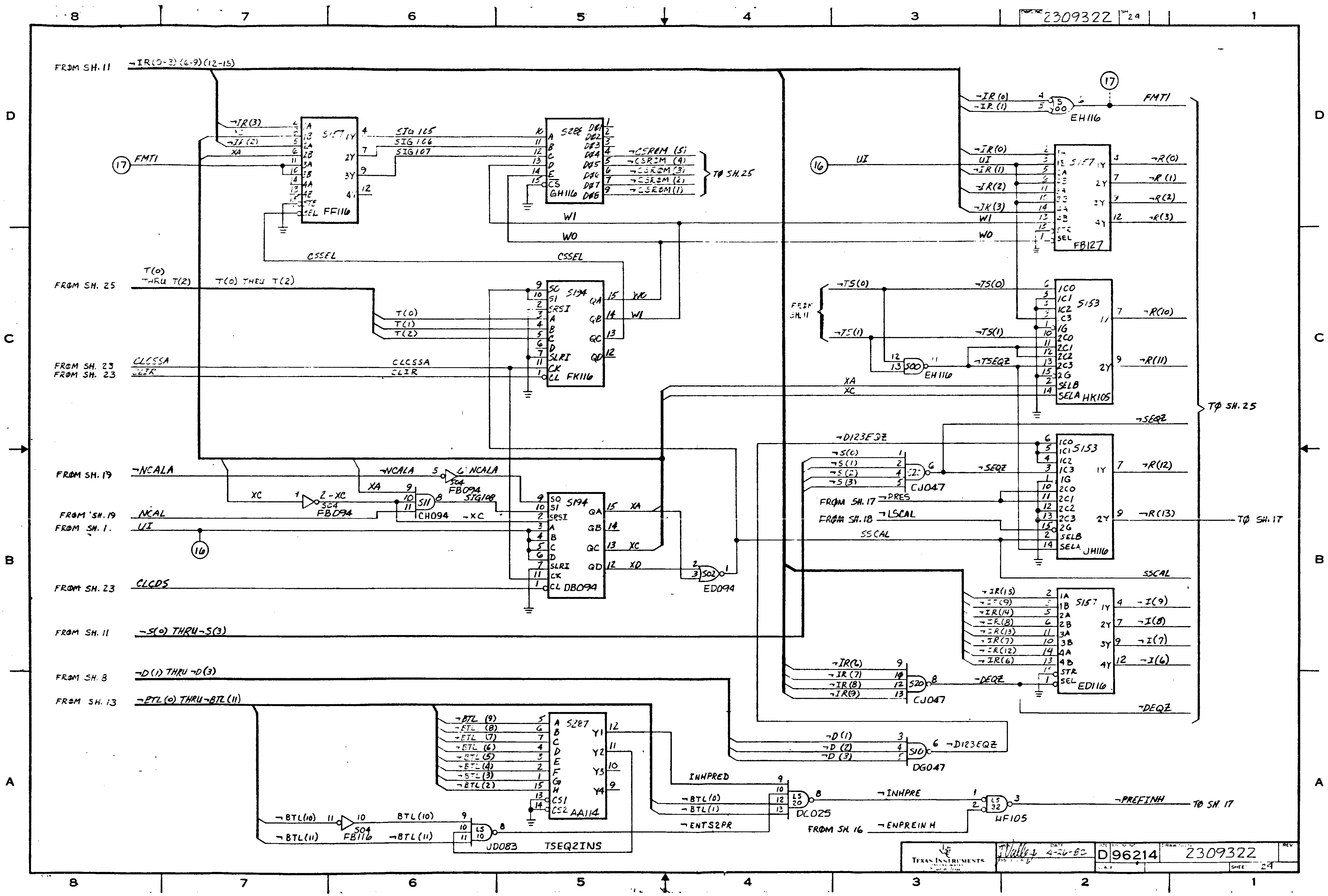

2309322 19
FROM SH. 27
RB(47) THRU RB(54)
FROM SH. 22
FROM SH. 21
FROM SH. 21
→Z16 BLIT
→SMINT
→MINT
GD094
RETURN
HB105
RB(47)
MRB(47)
MRB(47) THRU MRB(51)
T1 SH. 20
MRB(47)
MRB(48)
GH094
JFA
SD4 KB108
JTA
T1 SH. 20
T1 SH. 20
→COND
T1 SH. 20
MRB(49)
MRB(50)
ED094
SD4 FB116
COND
T1 SH. 9,20,26
FROM SH. 1
UI
RB(48)
RB(49)
RB(50)
RB(51)
S257
DB105
MRB(48)
MRB(49)
MRB(50)
MRB(51)
MRB(47)
JD106
→MRB47COND
T1 SH. 20
MRB(51)
JD094
→CONDMRB51
T1 SH. 21
FROM SH. 21
→ENCSA
RETURN
SD4 JH106
ENCSA
MRB(47)
MPE(47)
→APR(50)
EH116
CRB(50)
T1 SH. 20
PB(50)
→ARB(50)
ED094
MRB(47)
MRB(47)
SD4 FB094
→MRB(47)
T1 SH. 20
MRB(50)
RB(54)
RB(53)
RB(52)
S138
CH116
→SCALEØI
→SCALA
→SCALEØI
T1 SH. 18,20,23
→JMDØ
→JMDØR
T1 SH. 21,23
T1 SH. 20,21,23
RB(48)
RB(49)
DF116
RB4849
→NCAL
LS04 DK083
NCAL
T2 SH. 24
→RETMDØ
→RETMDØ
T1 SH 9,20,21
RB(47)
RB(51)
CH105
MRB4751
T1 SH 18
ENPINT
→SCALEØI
HB105
→SCALI
→NCALA
EH083
T1 SH. 24,25
→SCALA
→SCAL
EH127
→SCAL
T1 SH. 18,23
FROM SH. 5
FROM SH. 5
INTPRES
PRIORITY
GK047
& ENPINT
SD4 FB072
→ENPINT
T1 SH. 21
→SCAL
→JMDØ
→JMDØR
→NCAL
UI
UI
ENINT
MRB(50)
→ENJMPC
→ENJMP
DB116
DK116
→ENJMPB
T1 SH. 20
EH127
T1 SH. 26
→MINT
→RETMDØ
→ENCS(0)
→ENCS(1)
→ENCS(2)
FROM SH. 21
→ENCS(0)
→ENCS(1)
→ENCS(2)
FROM SH. 22
ENINTD
SD4 FB116
→ENINTD
FK072
→RETMDØ
JH094
→ENJMPD
P3-27
→FPINT
TEXAS INSTRUMENTS
4-23-82
D 96214
2309322
REV
SHEET 19

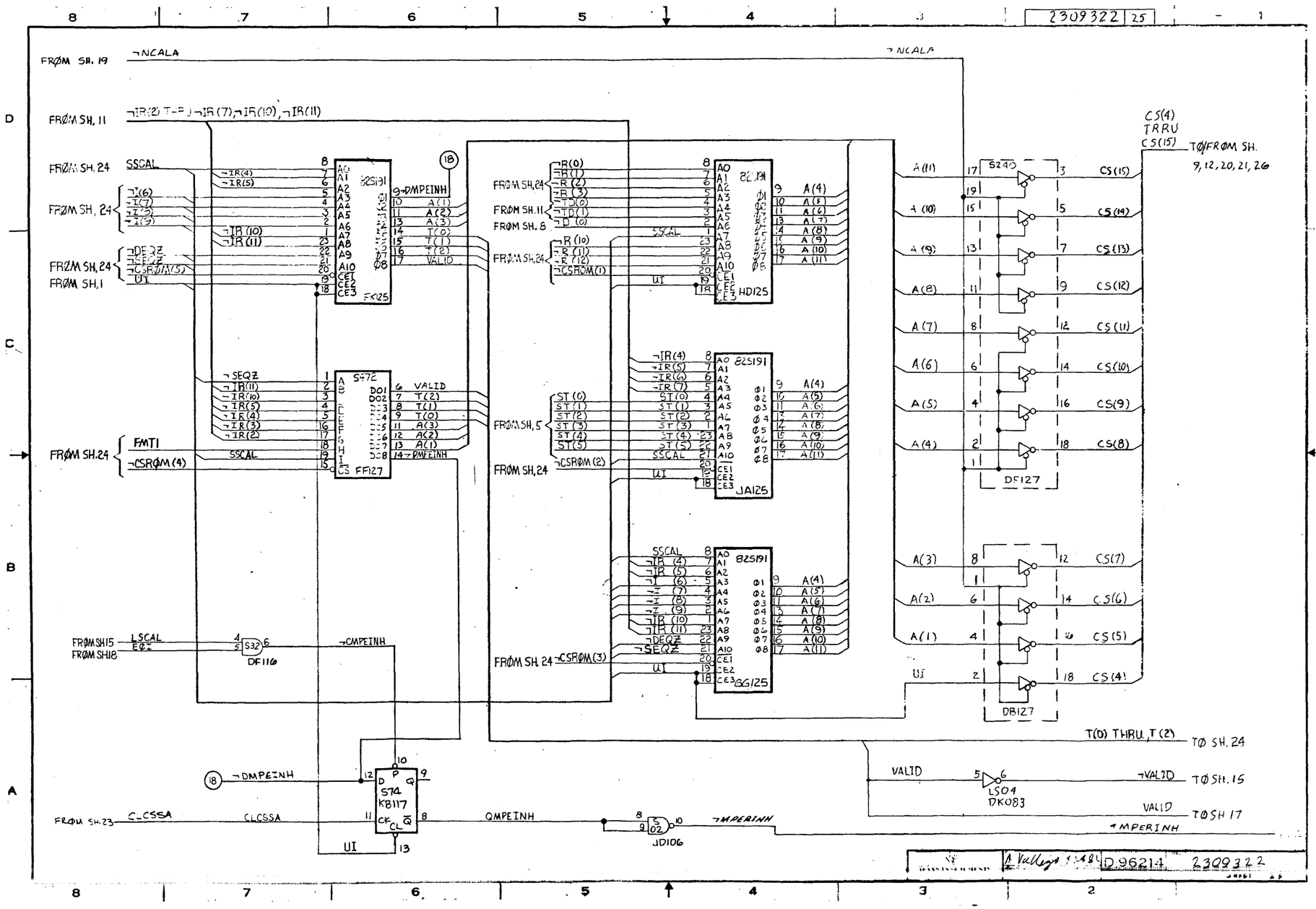

TO/FROM SH 9,12,21 25,26 CS(4) THRU CS(15)
FROM SH.19 MRB(47) THRU MRB(51)
GD105
JD116
S(3)
S(4)
NO SOURCE
¬DISRØM/2
DK083
DISRØM
GH105
TØ SH. 27
TØ SH. 28
UPC(0)
¬UPC(0)
P4-42
JH05B
FROM SH.23 CLCSSA
CH083
DB081
UPCR(3)
UPC(2)
UPC(1)
FROM SH. 21 ¬MINT2
FROM SH.17 ¬RST
ED072
FROM SH. 19 MRB(48)
FB116
EH116
MRBA(48)
DK116
S6A
S(6)
EH083
HK116
¬JUMP
JUMP
FB116
DF116
S5A
S(5)
FB083
DK128
S1A
CD083
CF081
UPCR(7)
UPC(6)
UPC(5)
UPC(4)
TO SH. 27, 28
FROM SH. 19 ¬RETMDØ
¬MINT
¬MRB(47)
DF094
SETS1
¬JMDØR
SLØCLK
DB083
TØ SH.23
C482
GK047
BK083
BK081
UPCR(11)
UPC(10)
UPC(9)
UPC(8)
DF083
S(2)
S(1)
FROM SH. 23 CLKA ¬SPH2
GK003
¬MINTPH2
MRB(51)
¬COND
EH083
¬C482
DB083
TEXAS INSTRUMENTS
4-23-82
D 96214
2309322
20

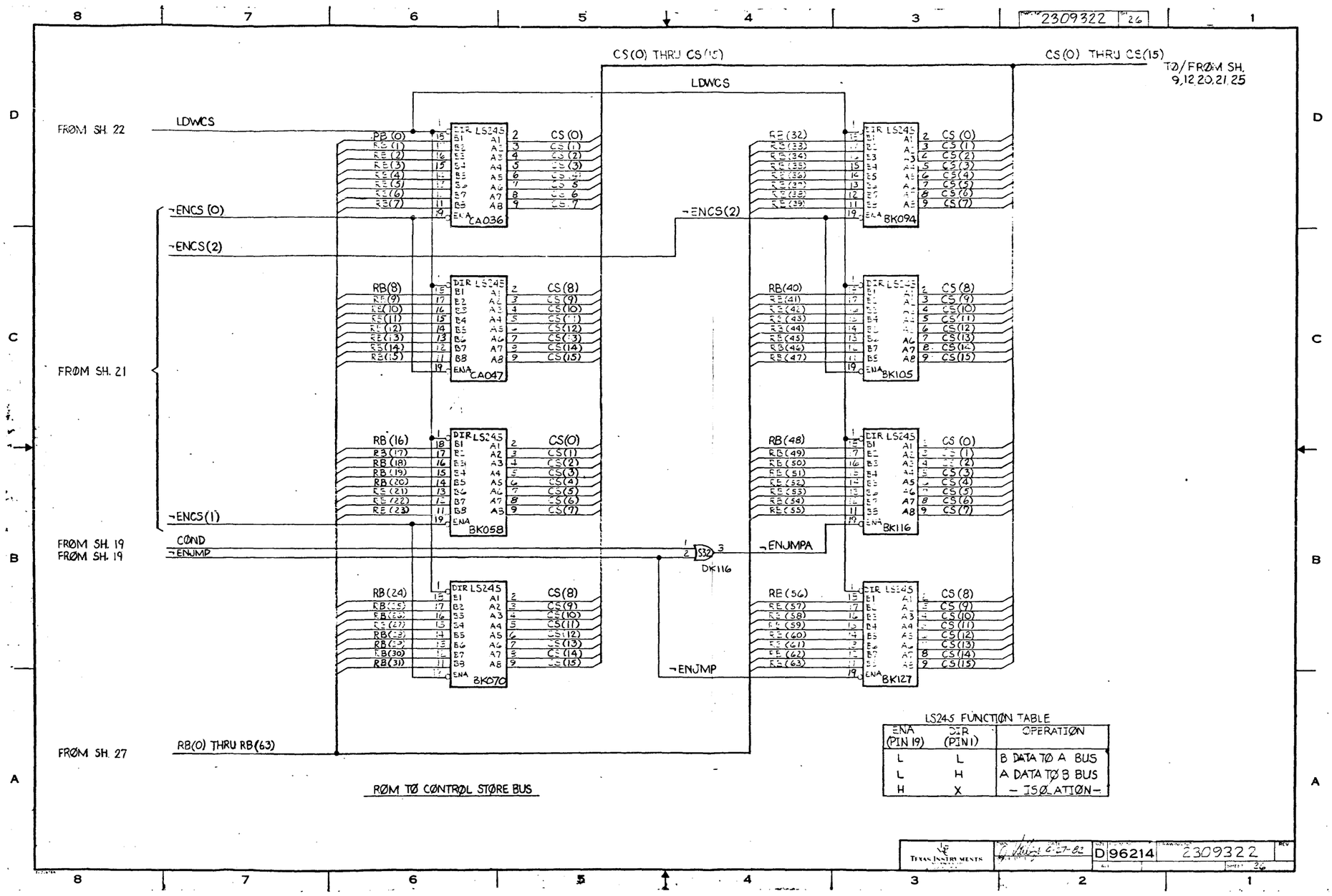

CONTROL STORE SEQUENCER
MICRO-INTERRUPT
2309322

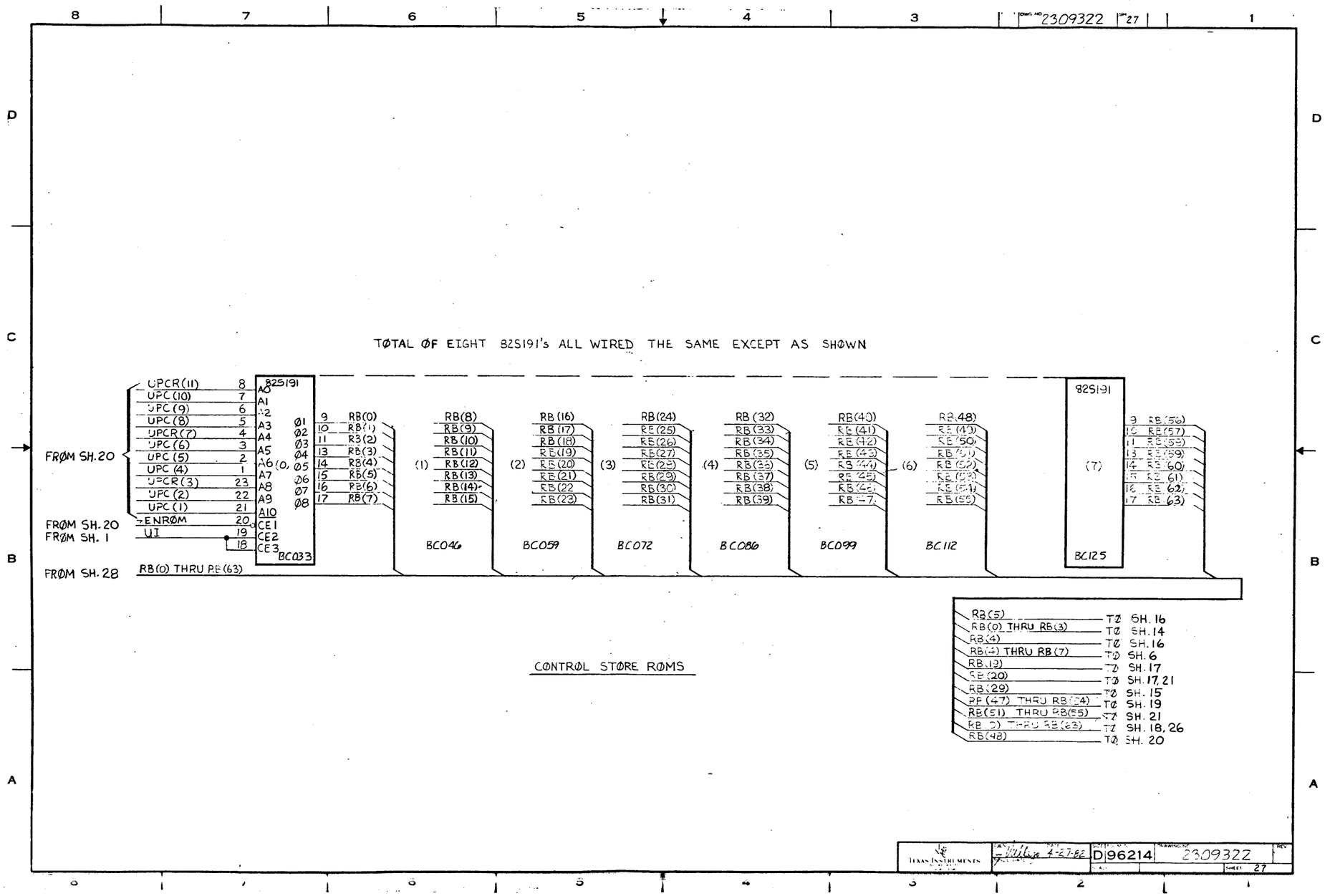

2309322
DECOD1
S471
ED083
DECOD2
HD047
S138
HK072
JD072
DECOD3
S472
JF039
HH047
HF083
TO SH. 9
TO SH. 16
TO SH. 8
TO SH. 4
TO SH. 18
P4-15
P4-17
FROM SH. 18
FROM SH. 23
FROM SH. 6
FROM SH. 17
FROM SH. 5
FROM SH. 11
FROM SH. 23
TO SH. 21
TEXAS INSTRUMENTS
D 96214
2309322

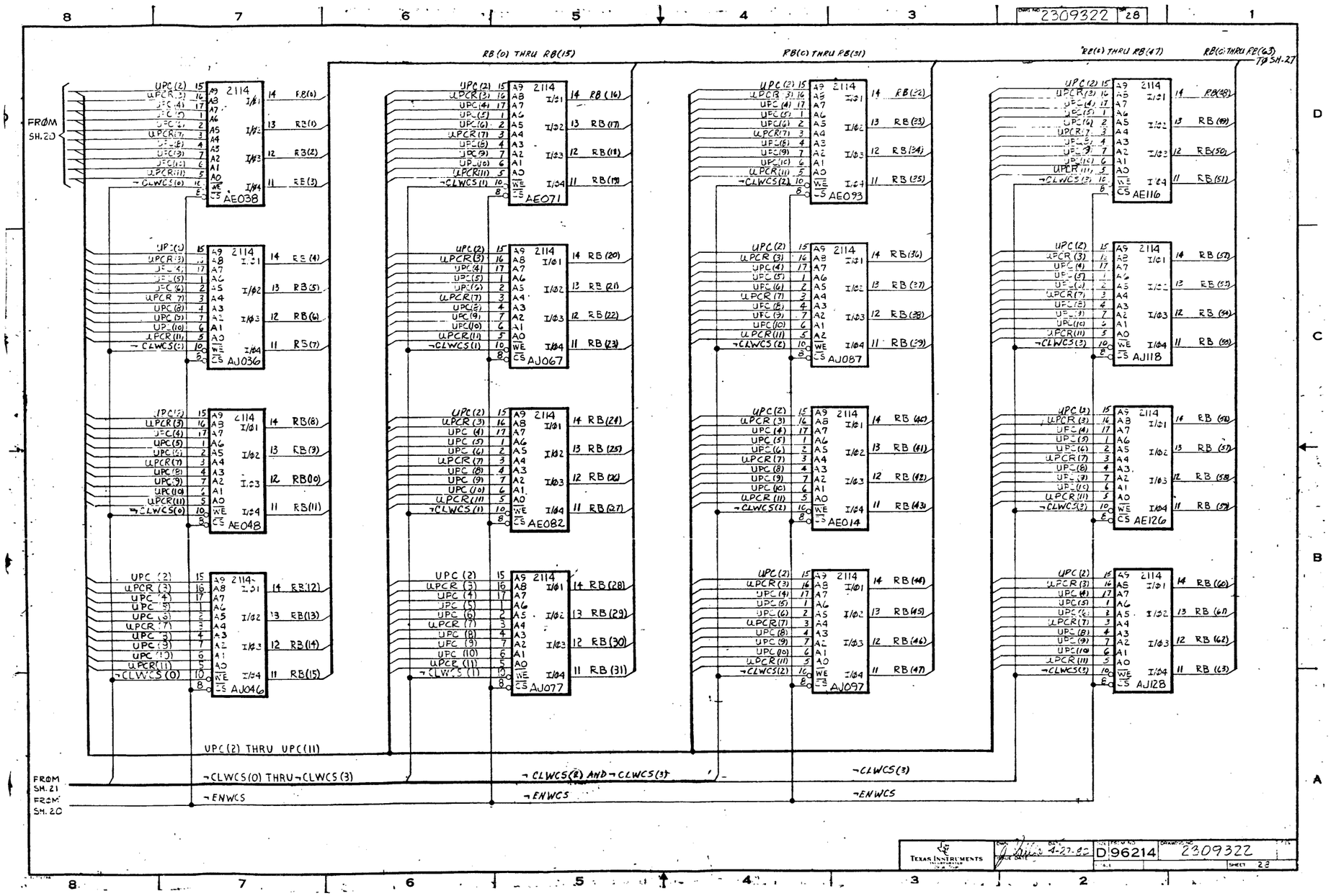

CLOCK DISTRIBUTION
FROM SH. 1
FROM SH. 14 ¬ENHPI
FROM SH21 ¬MINTINH
FROM SH. 17 ¬VNPR
P3-49 ¬SYSCLKB
FROM SH. 17
P3-47
TO SH. 21
TO SH. 14
CLK8A
¬INHIBIT
P4-19
CLKB
CLKC
CLK5
TO SH. 22
FROM SH. 17 STEP2WSR
FROM SH. 17 RST
FROM SH. 21 ¬ENCSA
FROM SH. 6 ¬RAD(1)
LONG482A
CLKA
TO SH. 20
CLCSLA
CLCSLB
CLCSLC
CLWSL
CLWSR
LONG482
P4-39
CLCSSA
CLCSSB
FROM SH. 22
D96214
2309322

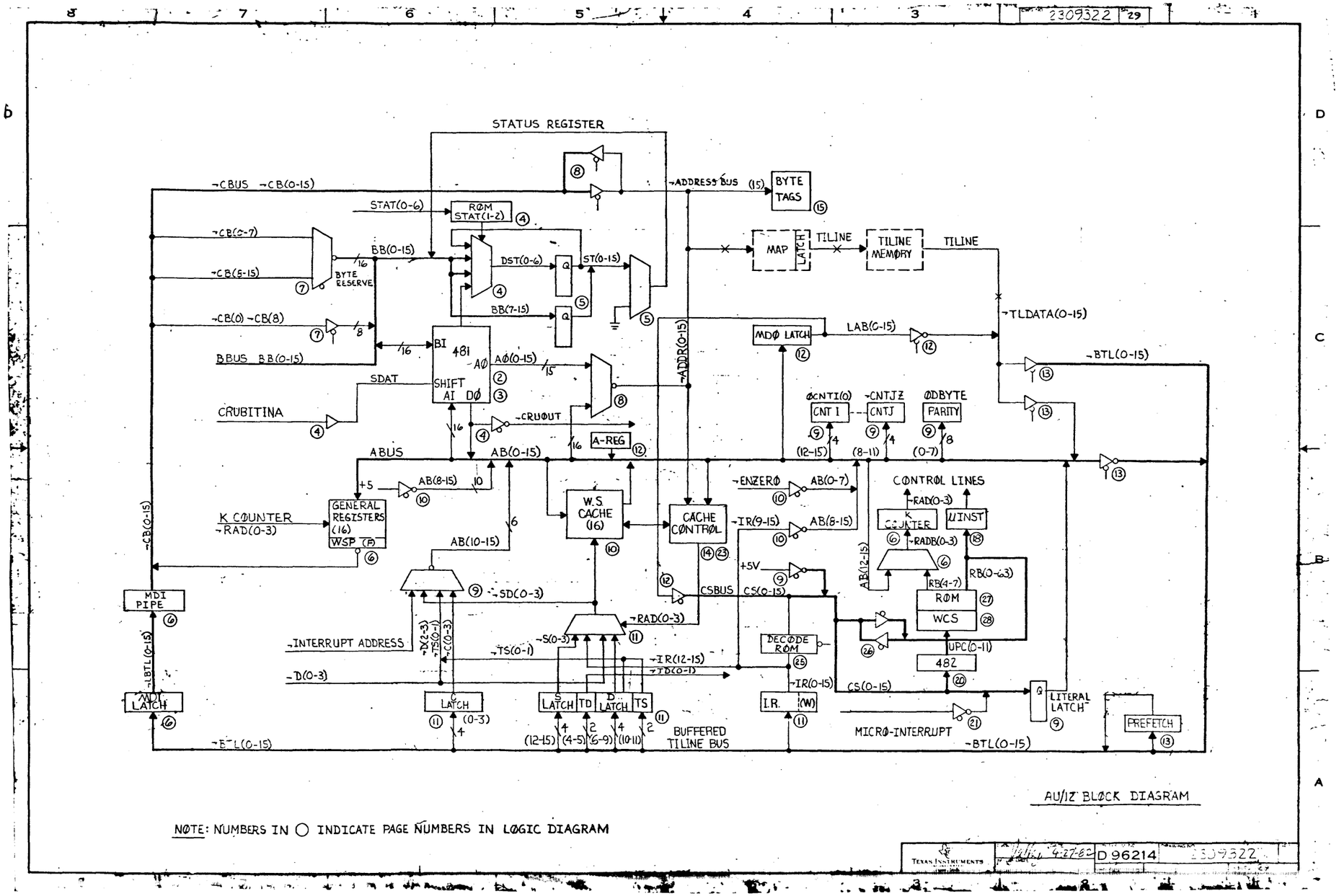

2309322
FROM SH. 11
FROM SH. 25
FROM SH. 23
FROM SH. 19
FROM SH. 1.
FROM SH. 8
FROM SH. 13
FROM SH. 17
FROM SH. 18
FROM SH. 16
TO SH. 25
TO SH. 17
FF116
GH116
FK116
DB094
FB094
CH094
ED094
AA114
JD083
TSEQ2INS
EH116
FB127
HK105
JH116
CJ047
ED116
DG047
DC025
HF105
FMT1
T(0) THRU T(2)
CSSEL
W1
W0
XA
XC
XD
-NCALA
NCAL
UI
CLCSSA
CLCDS
-S(0) THRU -S(3)
-D(1) THRU -D(3)
-BTL(0) THRU -BTL(11)
INHPRED
-INHPRE
-ENPREIN H
-PREFINH
-SEQZ
-DEQZ
-D123EQZ
SSCAL
-LSCAL
-PRES
TEXAS INSTRUMENTS
4-26-82
D 96214
2309322


2309322 25
FROM SH. 19
¬NCALA
FROM SH. 11
¬IR(2) THRU ¬IR(7), ¬IR(10), ¬IR(11)
FROM SH. 24
SSCAL
FROM SH. 24
FROM SH. 1
FROM SH.24
FMTI
¬CSRØM(9)
FROM SH15
FROM SH18
LSCAL
EQ
DF116
FROM SH.23
C_CSSA
CLCSSA
UI
¬DMPEINH
QMPEINH
JD106
¬MPERINH
FROM SH.11
FROM SH. 8
FROM SH.5
FROM SH. 24
¬CSRØM(3)
JA125
JH125
JG125
CS(4)
TRRU
CS(15)
TØ FROM SH.
9, 12, 20, 21, 26
DF127
DB127
T(0) THRU T(2)
TØ SH. 24
VALID
¬VALID
TØ SH. 15
TØ SH 17
LS04
DK083
A Vallejo
D.9621-1
2309322


2309322
CS(0) THRU CS(15)
CS(0) THRU CS(15)
TO/FROM SH. 9,12,20,21,25
LDWCS
FROM SH. 22
LDWCS
¬ENCS(0)
¬ENCS(2)
¬ENCS(2)
FROM SH. 21
¬ENCS(1)
FROM SH. 19
COND
FROM SH. 19
¬ENJMP
¬ENJMPA
¬ENJMP
FROM SH. 27
RB(0) THRU RB(63)
RØM TØ CØNTRØL STØRE BUS
DIR LS245
CA036
CA047
BK058
BK070
BK094
BK105
BK116
BK127
DK116
LS245 FUNCTION TABLE
ENA (PIN 19) | DIR (PIN 1) | OPERATIØN
L | L | B DATA TØ A BUS
L | H | A DATA TØ B BUS
H | X | – ISØLATIØN–
TEXAS INSTRUMENTS
D 96214
2309322


8
7
6
5
4
3
2
1
DWG NO 2309322
SH 27
D
C
B
A
TØTAL ØF EIGHT 82S191's ALL WIRED THE SAME EXCEPT AS SHØWN
82S191
UPCR(11) 8
UPC(10) 7
UPC(9) 6
UPC(8) 5
UPCR(7) 4
UPC(6) 3
UPC(5) 2
UPC(4) 1
UPCR(3) 23
UPC(2) 22
UPC(1) 21
ENRØM 20
UI 19
18
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
CE1
CE2
CE3
BC033
Ø1
Ø2
Ø3
Ø4
Ø5
Ø6
Ø7
Ø8
9 RB(0)
10 RB(1)
11 RB(2)
13 RB(3)
14 RB(4)
15 RB(5)
16 RB(6)
17 RB(7)
FRØM SH.20
FRØM SH.20
FRØM SH. 1
FRØM SH. 28
RB(0) THRU RB(63)
(1)
RB(8)
RB(9)
RB(10)
RB(11)
RB(12)
RB(13)
RB(14)
RB(15)
BC046
(2)
RB(16)
RB(17)
RB(18)
RB(19)
RB(20)
RB(21)
RB(22)
RB(23)
BC059
(3)
RB(24)
RB(25)
RB(26)
RB(27)
RB(28)
RB(29)
RB(30)
RB(31)
BC072
(4)
RB(32)
RB(33)
RB(34)
RB(35)
RB(36)
RB(37)
RB(38)
RB(39)
BC086
(5)
RB(40)
RB(41)
RB(42)
RB(43)
RB(44)
RB(45)
RB(46)
RB(47)
BC099
(6)
RB(48)
RB(49)
RB(50)
RB(51)
RB(52)
RB(53)
RB(54)
RB(55)
BC112
(7)
9 RB(56)
10 RB(57)
11 RB(58)
13 RB(59)
14 RB(60)
15 RB(61)
16 RB(62)
17 RB(63)
BC125
RB(5) TØ SH. 16
RB(0) THRU RB(3) TØ SH. 14
RB(4) TØ SH. 16
RB(4) THRU RB(7) TØ SH. 6
RB(13) TØ SH. 17
RB(20) TØ SH. 17, 21
RB(29) TØ SH. 15
RB(47) THRU RB(54) TØ SH. 19
RB(51) THRU RB(55) TØ SH. 21
RB(0) THRU RB(63) TØ SH. 18, 26
RB(48) TØ SH. 20
CONTRØL STØRE RØMS
TEXAS INSTRUMENTS
4-27-82
D 96214
2309322
SHEET 27


2309322 28
RB(0) THRU RB(15)
RB(16) THRU RB(31)
RB(32) THRU RB(47)
RB(48) THRU RB(63)
TO SH. 27
FROM SH. 20
AE038
AJ036
AE048
AJ046
AE071
AJ067
AE082
AJ077
AE093
AJ087
AE014
AJ097
AE116
AJ118
AE126
AJ128
UPC(2) THRU UPC(11)
¬CLWCS(0) THRU ¬CLWCS(3)
¬ENWCS
FROM SH. 21
FROM SH. 20
¬CLWCS(2) AND ¬CLWCS(3)
¬CLWCS(3)
TEXAS INSTRUMENTS
D 96214
2309322
SHEET 28



AU/12 BLOCK DIAGRAM

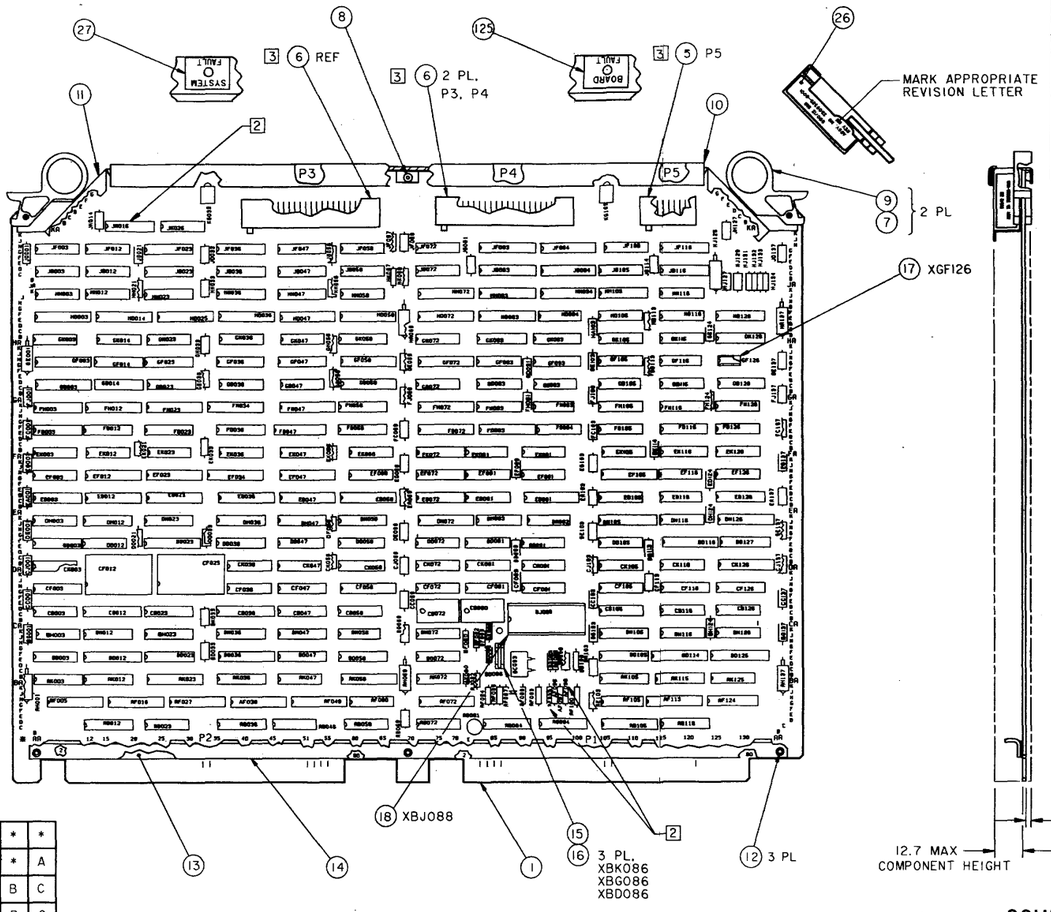
NØTE: NUMBERS IN ○ INDICATE PAGE NUMBERS IN LØGIC DIAGRAM

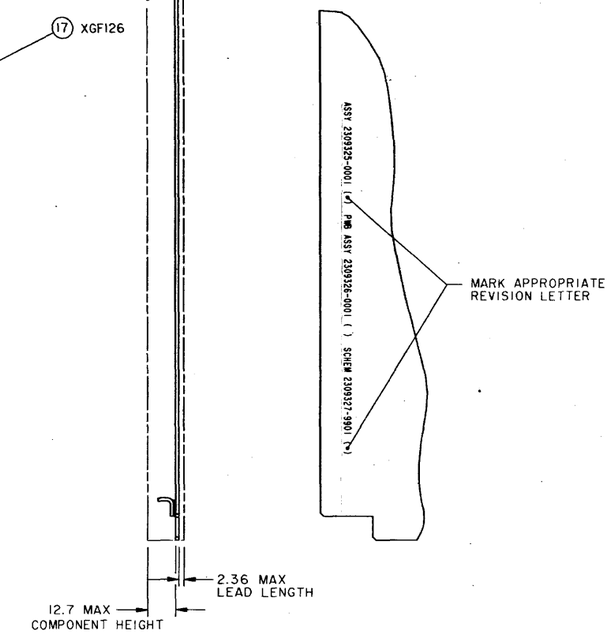
DWG NO 2309325 SH

NOTES: UNLESS OTHERWISE SPECIFIED:

1. ITEM 28 IN THE -0001 LM CONSISTS OF COMPONENTS WHICH ARE AUTO-INSERTED AND CONTAINED IN THE -5001 LM
2. REFERENCE DESIGNATORS JK016, AF096, AF098, AND BF081 ARE FOR SPARE COMPONENTS
3. SQUARE PAD INDICATES PIN 1 OF P3, P4, AND P5
4. REWORK PROCEDURE FOR REVISION A AND REVISION B PWB'S
   - A. CUT PIN 4 OF PACKAGE GB072.
   - B. ADD WIRE (30 AWG) FROM PIN 4 OF PACKAGE GB072 TO PIN 8 OF PACKAGE GB072.
   - C. ADD WIRE (30 AWG) FROM PIN 10 OF PACKAGE GB072 TO PIN 11 OF PACKAGE GB072.
   - D. ADD WIRE (30 AWG) FROM PIN 9 OF PACKAGE GB072 TO PIN 1 OF PACKAGE HH116.
   - E. ADD WIRE (30 AWG) FROM PIN 13 OF PACKAGE GB072 TO PIN 12 OF PACKAGE EF126.
   - F. ADD WIRE (30 AWG) FROM PIN 12 OF PACKAGE GB072 TO PIN 11 OF PACKAGE HH094.

CONVERSION CHART	
MM	INCHES
0.25	.010
0.5	.02
2.36	.093
3.0	.12
12.7	.50





REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	CN497644(E) D.PARR (1)LM-0001, ITEM 4 WAS 2309329-9901 SPEC. 990112. LR SMI (2)UPDATED REV LEVEL BLOCK	1-10-83	E. DIAZ
B	CN4981236(D) D.WHITE (1) ADDED SYSTEM TEST PROCEDURE, ITEM 126, TO -0001 LM (2) UPDATED REV LEVEL BLOCK	2-1-83	E. Diaz
C	CN4981195(B) D.WHITE (1) ADDED NOTE 4 (2) UPDATED REV LEVEL BLOCK	2-1-83	E. Diaz

REVISION LEVEL					
TEST PROC 2309328-9901	*	*	*	*
LOGIC 2309327-9901	*	*	*	A
PWB 2309326-0001	A	B	B	C
ASSY 2309325-0001	*	A	B	C

COMPUTER GENERATED DRAWING
DO NOT REVISE MANUALLY

[1]

2309325-5001 2309325-0001	AUTO-INSERTED PARTS LIST FOR -0001 990112, LR SMI ASSEMBLY
PART NUMBER	DESCRIPTION

SEQ NO	IDENT	F-SPEC	NO	ADDITIONAL CLASSIFICATION	NOTES	REV STATUS OF SHEETS	REV
	PROCESS						SH
3	MARK	902-01	01	HGT 3.0. COLOR BLACK (CAT 16)			
2	SLDR	127-01	00				
1	SLDR	124-02	00				

-3 QTY	-2 QTY	-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES
				2309332	7110	
				NEXT ASSY	USED ON	

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES: 2 PLACE DECIMALS ± 0.25, 1 PLACE DECIMALS ± 0.5, ANGLES ± 1°
- INTERPRET DRAWING PER 000-0-1000
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS 0.25 FIM
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE | THIRD ANGLE PROJECTION

0.33 THRU 3.18	+0.10/-0.03
3.20 THRU 6.35	+0.13/-0.03
6.38 THRU 12.70	+0.15/-0.03
12.73 THRU 19.05	+0.20/-0.03

DWN	D. WHITE	7-14-82
CHK	E. DIAZ	9-29-82
ENGR	RICHARD KINNAS	9-30-82
APVD-ENGR	ROBERT C. SISCO	10-6-82
QA	JOSEPH T. POOT	10-1-82
APVD-MFG	MIKE FISHBECK	10-1-82
RLSE	TONY BAILEY	10-7-82

TEXAS INSTRUMENTS INCORPORATED Digital Systems Group — SI-METRIC

990112. LR SMI ASSEMBLY

SIZE D | FSCM NO 06668 | DRAWING NO 2309325

TEXAS INSTRUMENTS INCORPORATED — DATE 01/26/83 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 1 of — PART NUMBER LM2309325-0001 — REV C

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	REF	EA		2309327-9901	LOGIC DIAGRAM,990/12,LR SMI	
0003	REF	EA		2309328-9901	TEST PROC,990/12,LR SMI	
0004	REF	EA		2309324-9901	SPEC,990/12,LR AU	
0005	00001.000	EA		2210154-0007	HEADER,PLZD AND LATCH, 20 POS	000779-SEE TI DWG
0005A					P5	
0006	00002.000	EA		2210154-0015	HEADER,POLARIZED AND LATCHING, 50 PINS	000779-86476-7
0006A					P3 P4	
0007	00002.000	EA		2308622-0001	EJECTOR,PWB,SELF-LOCKING	
0008	00001.000	EA		0972831-0003	RIVET,1/8X.235,TUBULAR,STEEL,BLIND	019738-1821-0408
0009	00002.000	EA		0085936-0067	EYELET.089 BARREL OD X.375 LG FLANGE	
0010	00001.000	EA		2308640-0001	INSULATOR,SHIELD-STIFFENER,270.5MM	
0011	00001.000	EA		2308618-0001	SHIELD-STIFFENER,GROUP III,(CPU)	
0012	00003.000	EA		0085936-0017	EYELET .121 BARREL OD X.187 LG FLANGE	USH - #SE-46
0013	00001.000	EA		2308655-0001	INSULATOR,PWB,346.96MM,EYELET MOUNT	
0014	00001.000	EA		2308653-0001	STIFFENER,PWB,346.96MM,EYELET MOUNT	
0015	00001.000	EA		0972713-0001	PLUG, JUMPER, I.C., 0.300 INCH	
0015A					BG086	
0016	00003.000	EA		0996864-0001	CONNECTOR,SOCKET PCB	022526-75060-007

DRAFTSMAN — DATE — CKD DRAFTSMAN L. Koenig 1-26-83 — DESIGN ENGINEER — TITLE 990/12,LR SMI ASSY

APPD MFG. — APPD PROJECT ENGINEER — RELEASED — PROJECT NO 7110 — PART NUMBER LM2309325-0001 — REV C

T.I. 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/26/83 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 2 of — PART NUMBER LM2309325-0001 — REV C

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0016A					XBG086 XBD086 XBK086	
0017	00001.000	EA		2210188-0010	DIP SOCKET,8-PIN,LOW PROFILE	SEE TI- DRAWING
0017A					XGF126	
0018	00001.000	EA		2210188-0017	SOCKET,DIP,28-PIN,LOW PROFILE	SEE T -I DRAWING
0018A					XBJ088	
0019	00001.000	EA		0972927-0048	CAP FIX MICA 300V 750 PF 5 %	QPL -CM05F751JDC
0019A					BC093	
0020	00001.000	EA		2210293-0005	DELAY MODULE, TAPPED, 40 4NS	019612-1213
0020A					CB080	
0021	00001.000	EA		2210293-0002	DELAY MODULE,TAPPED,50 +/- 3NS	001961-21198
0021A					CB072	
0022	00001.000	EA		0972188-0001	NETWORK,NE555V,MONOLITHIC TIMING,LINEAR	ST -NE555V
0022A					GF126	
0023	00001.000	EA		0236081-0000	X-XST 2N2894	TI -2N2894
0023A					AB081	
0024	00001.000	EA		0996896-0001	IC, CONTROLLER, SN58220N	001295-SN58220N
0024A					BJ088	
0025	00002.000	EA		2220291-0001	LED,RED,5V=VF,15MA=IF,R.ANGLE,1-POS.	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE 990/12,LR SMI ASSY

APPD MFG. — APPD PROJECT ENGINEER — RELEASED — PROJECT NO — PART NUMBER LM2309325-0001 — REV C

T.I. 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/26/83 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 3 of — PART NUMBER LM2309325-0001 — REV C

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0025A					KG033 KG105	
0026	00001.000	EA		2308630-0006	LABEL,ID,990 EMI/RFI BD-990/SMI	
0027	00001.000	EA		2308652-0002	LABEL,LED,CPU,990 EMI/RFI-SYSTEM FAULT	
0028	00001.000	EA		2309325-5001	AUTO-INSERTED PARTS LIST FOR -0001	
0029	00001.000	EA		2309348-0001	ROM,990/12,LR,LOADER/SELF TEST,LSB	
0029A					CF012	
0030	00001.000	EA		2309348-0002	ROM,990/12,LR,LOADER/SELF TEST,MSB	
0030A					CF025	
0038	00001.000	EA		0972757-0009	CAP FIX CER 470PF 10% 50V	
0038A					AJ082	
0122	00001.000	EA		0539370-0597	RES FIX FILM 162 K OHM 1% .25 WATT	COR - NA55
0122A					ALTERNATE PN 539370-0585	
0122B					THRU -0606	
0122C					HJ131	
0125	00001.000	EA		2308652-0001	LABEL,LED,CPU,990 EMI/RFI-BOARD FAULT	
0126	REF	EA		2262003-9901	TEST PROC, SYSTEM, 990/12 CPU W/MAPPING	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE 990/12,LR SMI ASSY

APPD MFG. — APPD PROJECT ENGINEER — RELEASED — PROJECT NO — PART NUMBER LM2309325-0001 — REV C

T.I. 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/26/83 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 1 of — PART NUMBER LM2309325-5001 — REV C

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2309326-0001	PWB,990/12 SMI,LR	
0031	00002.000	EA		0972757-0033	CAP,FIX,CERAMIC,.047MF,50V,+/-10% TOL.	
0031A					HJ127 HJ129	
0032	00001.000	EA		0972757-0001	CAP,FIXED CERAMIC 100 PF 10% 50V	UC -C51C101K
0032A					AF089	
0033	00007.000	EA		0972924-0006	CAP FIX TANT SOLID 39 UFD 10% 10 VOLT	QPL -M39003/1-2259
0033A					HJ125 AH001 GE001 AH069	
0033B					HA069 AH137 HA137	
0034	00041.000	EA		0972763-0025	CAPACITOR,.10UF 50V FX,CERAMIC DIEL	COR CA-C03Z5U104Z050A
0034A					BG001 CJ001 EA001 FC001	
0034B					GD091 HH021 BD033 DD033	
0034C					GB033 HH033 CK056 EK056	
0034D					GH056 JD056 AB069 CC069	
0034E					DE069 EG069 FJ069 HK069	
0034F					CF089 EF089 AE103 BG103	
0034G					CJ103 EA103 FC103 GE103	
0034H					CF113 EK114 HB113 BH124	
0034I					ED124 GK124 BG137 CJ137	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE AUTO-INSERTED PARTS LIST FOR -0001

APPD MFG. — APPD PROJECT ENGINEER — RELEASED — PROJECT NO — PART NUMBER LM2309325-5001 — REV C

T.I. 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/26/83 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 2 of — PART NUMBER LM2309325-5001 REV C

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0034J					EA137 FC137 GE137 JK014	
0034K					DD021	
0035	00040.000	EA		0972763-0013	CAP,FIXED .010UF 50 VOLTS	004222-MC105E103Z
0035A					CC001 DE001 EG001 FJ001	
0035B					JD001 EK021 JD021 BK033	
0035C					EK033 GH033 JD033 DF056	
0035D					GB056 HH056 BG069 CJ069	
0035E					EA069 FC069 GE069 JF069	
0035F					JB081 DB089 FH091 BA103	
0035G					CC103 DE103 EG103 FJ103	
0035H					HA103 DB113 GD113 JB114	
0035I					DH124 FH124 CC137 DE137	
0035J					EG137 FJ137 JD137 JH127	
0036	00001.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0036A					BB098	
0037	00003.000	EA		0972753-0012	CAP,FIXED 220PF 25 WVDC 2.0%	UC -C50D221G
0037A					AF100 AK080 BB100	
0039	00001.000	EA		0222222-7407	NETWORK-SN7407N	TI- -SN7407N

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR -0001

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM2309325-5001 REV C

T.I. 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/26/83 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 3 of — PART NUMBER LM2309325-5001 REV C

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0039A					CB105	
0040	00002.000	EA		0222222-7125	NETWORK SN74125N	
0040A					DD081 EK116	
0041	00002.000	EA		0222222-7148	NETWORK SN74148N	
0041A					BD047 BD058	
0042	00004.000	EA		0996017-0001	INTEGRATED CIRCUIT,QUAD J-K FLIP-FLOP	TI -SN74276N
0042A					CK126 DH126 HH094 JB094	
0043	00002.000	EA		0222222-7437	NETWORK SN7437N	
0043A					AB072 AF105	
0044	00003.000	EA		0222222-7442	NETWORK-SN7442N	
0044A					AB012 AB094 AB116	
0045	00003.000	EA		0972900-7400	NETWORK SN74LS00N	TI -SN74LS00N
0045A					CB126 FH105 GF083	
0046	00004.000	EA		0972900-7401	IC,SN74LS01N	TI -SN74LS01N
0046A					AB046 AB059 AF060 CB116	
0047	00001.000	EA		0972900-7402	NETWORK,SN74LS02N	
0047A					DH003	
0048	00005.000	EA		0972900-7404	NETWORK SN74LS04N	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR -0001

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM2309325-5001 REV C

T.I. 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/26/83 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 4 of — PART NUMBER LM2309325-5001 REV C

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0048A					AB023 CK105 EB105 FD126	
0048B					GB105	
0049	00004.000	EA		0972749-0001	NETWORK, SN74LS08N	
0049A					CB003 DH116 EF116 GB083	
0050	00002.000	EA		0972900-7410	NETWORK SN74LS10N	
0050A					CK116 FH116	
0051	00001.000	EA		0972900-7430	NETWORK SN74LS30N	TI -SN74LS30N
0051A					DD091	
0052	00002.000	EA		0972900-7474	NETWORK SN74LS74N	
0052A					BD003 CF105	
0053	00004.000	EA		0972815-0001	NETWORK-SN74LS85N	
0053A					DD023 DD036 DD047 DD058	
0054	00001.000	EA		0972751-0001	NETWORK, SN74LS86N	
0054A					EK003	
0055	00001.000	EA		0972900-7112	NETWORK SN74LS112N	TI -SN74LS112N
0055A					GK126	
0056	00002.000	EA		0972782-0001	NETWORK SN74LS132N	TI -SN74LS132N
0056A					CF091 EF003	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR -0001

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM2309325-5001 REV C

T.I. 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/26/83 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 5 of — PART NUMBER LM2309325-5001 REV C

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0057	00003.000	EA		0972900-7138	NETWORK SN74LS138N	TI -SN74LS138N
0057A					AB036 CF116 CF126	
0058	00001.000	EA		0801383-0001	NETWORK SN74LS151N	
0058A					AB084	
0059	00001.000	EA		0972669-0001	NETWORK,SN74LS163N	
0059A					AK003	
0060	00004.000	EA		0972900-7175	NETWORK SN74LS175N	
0060A					AK105 BD105 BH105 CF003	
0061	00014.000	EA		0996089-0001	IC,SN74LS240N,LINE DRIVERS	001295-SN74LS240N
0061A					AF027 AF072 AK023 BD012	
0061B					BD036 EF105 HD003 HD058	
0061C					HD072 HD083 JF094 GF003	
0061D					GF058 AF124	
0062	00002.000	EA		0996089-0002	IC,SN74LS241N,LINE DRIVERS	01295S-N74LS241N
0062A					GF072 HH083	
0063	00004.000	EA		0972668-0001	NETWORK SN74LS251N	
0063A					BD023 CF047 EB126 GB126	
0064	00006.000	EA		0996023-0001	IC,SN74LS259N	TI -SN74LS259N

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR -0001

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM2309325-5001 REV C

T.I. 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/26/83 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 6 of — PART NUMBER LM2309325-5001 REV C

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0064A					CK058 DD127 DH058 FD116	
0064B					HD126 HH105	
0065	00001.000	EA		0972667-0001	NETWORK,SN74LS279N	
0065A					EB003	
0066	00015.000	EA		0972652-0001	NETWORK SN74LS283N	
0066A					FD012 FD036 FD047 GF014	
0066B					GF036 GF047 HH023 HH036	
0066C					HH047 JB023 JB036 JB047	
0066D					JF023 JF036 JF047	
0067	00001.000	EA		2262022-0009	PROM,990/12,CLOCK CONTROL 1-B	
0067A					EF072	
0068	00001.000	EA		2262022-0008	PROM,990/12,CLOCK CNTL 2-A	
0068A					EB072	
0069	00011.000	EA		0996425-0001	IC,SN74LS299N	001295-SN74LS299N
0069A					AB105 AF005 AF016 AF038	
0069B					AF113 BD114 BD125 CF058	
0069C					DD116 FH023 FH047	
0070	00002.000	EA		0996420-0002	IC,SN74LS374N	001295-SN74LS374N

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR -0001

APPD MFG. — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2309325-5001 REV C

TI 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/26/83 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 7 of — PART NUMBER LM2309325-5001 REV C

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0070A					AF049 AK058	
0071	00003.000	EA		0996769-0001	IC,SN74LS377N,OCTAL,D-TYPE FLIP-FLOP	001295-SN74LS377N
0071A					FD072 GB003 GB058	
0072	00002.000	EA		0996765-0002	IC,SN74LS669AN,4-BIT UP/DOWN COUNTERS	001295-SN74LS669AN
0072A					BH003 GB093	
0073	00021.000	EA		0972654-0001	NETWORK,SN74LS670N	
0073A					EK012 EK023 EK036 EK047	
0073B					GB014 GB023 GB036 GB047	
0073C					GK014 GK023 GK036 GK047	
0073D					HH003 HH012 HH058 JB003	
0073E					JB058 JF003 JF012 JF058	
0073F					JB012	
0074	00010.000	EA		0219402-7400	NETWORK SN74S00N	
0074A					CK003 CK047 DD105 EK081	
0074B					FD094 GF116 GK116 HD094	
0074C					HD105 CF081	
0075	00002.000	EA		0219402-7402	NETWORK SN74S02N	TI -SN74S02N
0075A					EF060 GK105	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR -0001

APPD MFG. — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2309325-5001 REV C

TI 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/26/83 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 8 of — PART NUMBER LM2309325-5001 REV C

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0076	00002.000	EA		0219402-7404	NETWORK SN74S04N	
0076A					BH058 FH093	
0077	00005.000	EA		0219402-7408	NETWORK SN74S08N	TI -SN74S08N
0077A					BH116 DD072 DH092 EB081	
0077B					EK091	
0078	00003.000	EA		0219402-7410	IC, SN74S10N	
0078A					BH126 CK038 GF105	
0079	00002.000	EA		0219402-7411	NETWORK SN74S11N	
0079A					EB116 JK026	
0080	00001.000	EA		0219402-7415	NETWORK,SN74S15N SN74S SERIES	001295- SN74S15N
0080A					CF072	
0081	00003.000	EA		0219402-7420	NETWORK SN74S20N	
0081A					CF038 FH083 FH126	
0082	00002.000	EA		0219402-7430	NETWORK SN74S30N	
0082A					DD012 EF126	
0083	00002.000	EA		0219402-7432	NETWORK SN74S32N	TI -SN74S32N
0083A					CK072 CK091	
0084	00001.000	EA		0996851-0001	IC,QUAD POSITIVE-NAND, SN74S38N	-SN74S38N

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR -0001

APPD MFG. — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2309325-5001 REV C

TI 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/26/83 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 9 of — PART NUMBER LM2309325-5001 REV C

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0084A					AK072	
0085	00003.000	EA		0219402-7451	NETWORK SN74S51N	
0085A					EF081 GB116 GK072	
0086	00002.000	EA		0219402-7464	NETWORK SN74S64N	
0086A					DH083 EK126	
0087	00002.000	EA		0219402-7465	NETWORK SN74S65N	
0087A					BD072 BH072	
0088	00006.000	EA		0219402-7474	NETWORK SN74S74N	
0088A					CB058 CK081 EF091 EK060	
0088B					HD116 FD105	
0089	00001.000	EA		0219402-7112	NETWORK SN74S112N	TI -SN74S112N
0089A					DD003	
0090	00001.000	EA		0996849-0001	IC, POSITIVE-NAND GATE, SN74S134N	001295-SN74S134N
0090A					EK105	
0091	00001.000	EA		0219402-7138	NETWORK SN74S138N	
0091A					GK058	
0092	00001.000	EA		0219402-7139	NETWORK SN74S139N	
0092A					AK115	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR -0001

APPD MFG. — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2309325-5001 REV C

TI 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/26/83 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 10 of — PART NUMBER LM2309325-5001 REV C

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0093	00001.000	EA		0219402-7158	NETWORK SN74S158N	
0093A					JB116	
0094	00001.000	EA		0219402-7175	NETWORK,SN74S175N	
0094A					GK083	
0095	00009.000	EA		0996795-0001	IC,SN74S189N 16 X 4-BIT STATIC RAM	01295S-N74S189N
0095A					AK012 AK036 BH012 BH023	
0095B					BH036 BH047 CB023 CB047	
0095C					GK093	
0096	00006.000	EA		0996046-0001	IC,OCTAL BUFFER/DRIVER SN74S240	TI -SN74S240
0096A					DH072 HD014 HD036 HH072	
0096B					JF083 FH072	
0097	00004.000	EA		0996063-0001	IC,SN74S241N,LINE DRIVERS	001295-SN74S241N
0097A					EF023 EF047 HD025 HD047	
0098	00001.000	EA		0219402-7258	NETWORK SN74S258N	
0098A					GF093	
0099	00002.000	EA		0219402-7260	NETWORK SN74S260N	
0099A					AK125 GK003	
0100	00011.000	EA		0996848-0001	IC,SN74S283N 4-BIT FULL ADDER	001295-SN74S283

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR -0001

APPD. MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM2309325-5001 REV C

T.I. 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/26/83 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 11 of — PART NUMBER LM2309325-5001 REV C

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0100A					DH012 DH023 DH036 DH047	
0100B					EK072 FD003 FD023 FD058	
0100C					FH003 FH058 GF023	
0101	00005.000	EA		0972637-0001	NETWORK,74S299 SERIAL/PARALLEL CONVERTER	
0101A					EB012 EB023 EB036 EB047	
0101B					EB091	
0102	00002.000	EA		0996307-0001	IC,SN74S373,OCTAL D, FLIPFLOP	TI -SN74S373
0102A					FD083 JB083	
0103	00008.000	EA		0996201-0001	IC,SN74S374N,EDGE-TRIGGERED FLIP-FLOPS	TI -SN74S374N
0103A					CB012 CB036 DH105 EB058	
0103B					EF012 EF034 FH012 FH034	
0104	00002.000	EA		0972141-0041	NETWORK,RES. 1.0 K OHM 2 % 14 PIN DIP	BEC - 899-1-R1.0K
0104A					AK047 JF106	
0105	00001.000	EA		2210162-0301	NETWORK,RES LINE TERMINATION 5%,330/4700	073138-899-5-R330/470
0105A					JB072	
0106	00002.000	EA		0972007-1470	NETWORK,RES.,14 PIN,47 OHM,2%,7 ELEMENT	
0106A					JB105 JF072	
0107	00001.000	EA		0972037-2390	NETWORK,RES 390 OHM 2% 16PIN 8ELEMENT	SEE TI- DRAWING

AUTO-INSERTED PARTS LIST FOR -0001

APPD. MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM2309325-5001 REV C

T.I. 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/26/83 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 12 of — PART NUMBER LM2309325-5001 REV C

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0107A					JF116	
0108	00001.000	EA		0972141-0029	NETWORK,RES. 330 OHM 2 % 14 PIN DIP	BEC - 899-1-R330
0108A					HH116	
0109	00002.000	EA		0972946-0025	RES FIX 22.0 OHM 5 % .25 W.CARBON FILM	ROH - P-25
0109A					HK067 JF067	
0110	00002.000	EA		0972946-0065	RES FIX 1.0K OHM 5% .25 W CARBON FILM	ROH - R-25
0110A					BB095 BB096	
0111	00001.000	EA		2211400-0001	JUMPER,ZERO-OHM RESISTOR	SEE TI- DRAWING
0111A					BF083	
0112	00001.000	EA		0972946-0045	RES FIX 150 OHM 5 % .25 W CARBON FILM	SEE TI- DRAWING
0112A					HJ134	
0113	00001.000	EA		0972946-0081	RES FIX 4.7K OHM 5 % .25 W CARBON FILM	ROH - P-25
0113A					HJ133	
0114	00001.000	EA		0539370-0334	RES FIX FILM 294 OHM 1% .25 WATT	COR - NA55
0114A					AF095	
0115	00001.000	EA		0539370-0347	RES FIX FILM 402 OHM 1% .25 WATT	COR - NA55
0115A					AF097	
0116	00001.000	EA		0539374-0414	RES FIX FILM 2.00K OHM 1% .25 WATT	COR - NC5

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR -0001

APPD. MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM2309325-5001 REV C

T.I. 25789

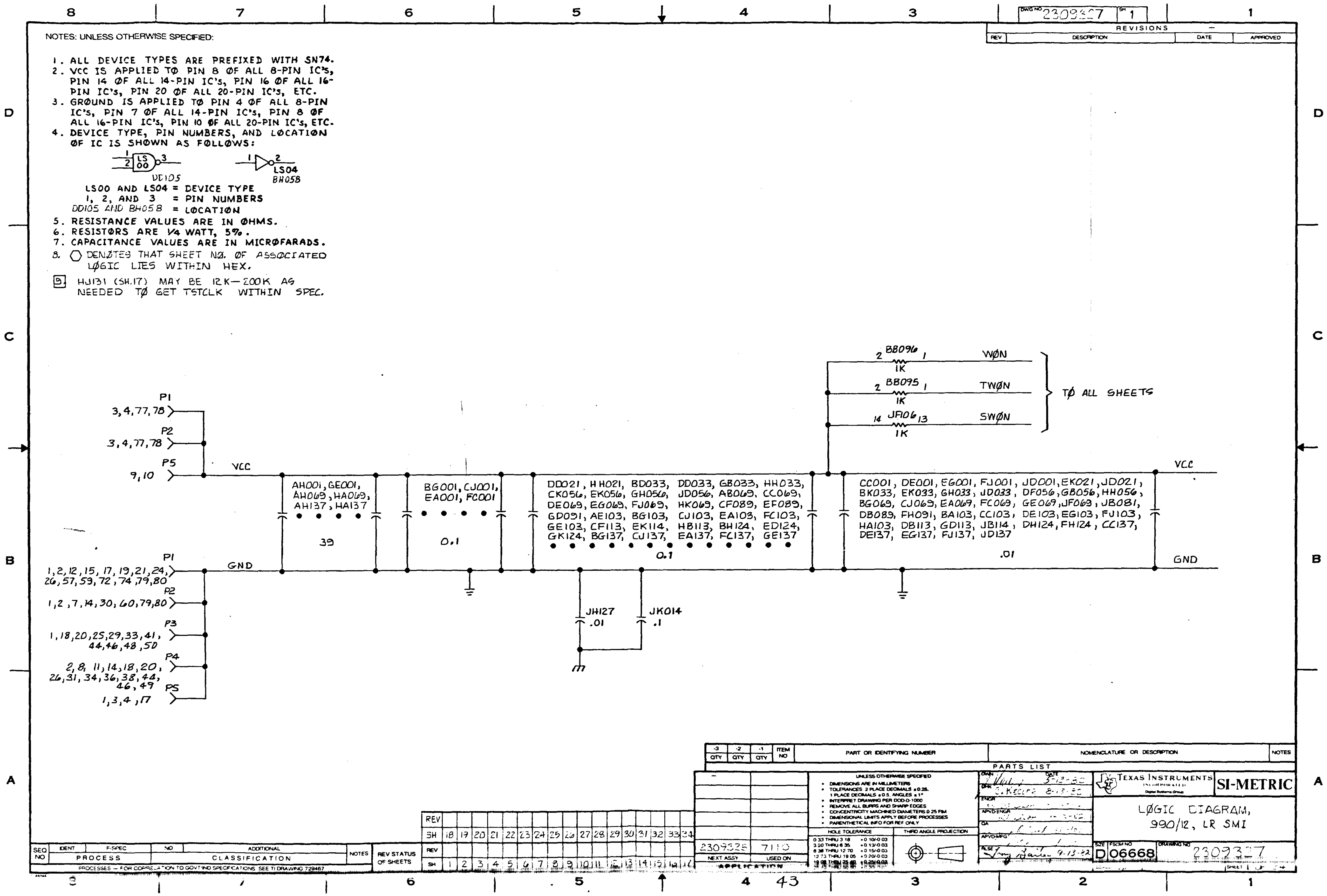
TEXAS INSTRUMENTS INCORPORATED — DATE 01/26/83 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 13 of — PART NUMBER LM2309325-5001 REV C

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0116A					AF093	
0117	00001.000	EA		0539374-0391	RESISTOR,FXD,FILM, 1.15 K OHMS,1/4W, 1%	024546-
0117A					BF080	
0118	00001.000	EA		0539370-0567	RES FIX FILM 78.7K OHM 1% .25 WATT	COR - NA55
0118A					BF082	
0119	00001.000	EA		0972946-0019	RES FIX 12.0 OHM 5 % .25 W.CARBON FILM	ROH - R-25
0119A					AF085	
0120	00001.000	EA		0972946-0109	RES FIX 68 K OHM 5 % .25 W CARBON FILM	ROH - R-25
0120A					HJ132	
0121	00002.000	EA		0972946-0054	RES FIX 360 OHM 5 % .25 W CARBON FILM	ROH - R-25
0121A					AF084 AF086	
0123	00001.000	EA		0972932-0001	DIODE 1N914B	SEE TI- DRAWING
0123A					AF087	
0124	00001.000	EA		0972655-0001	NETWORK,SN74S132N	
0124A					GB072	

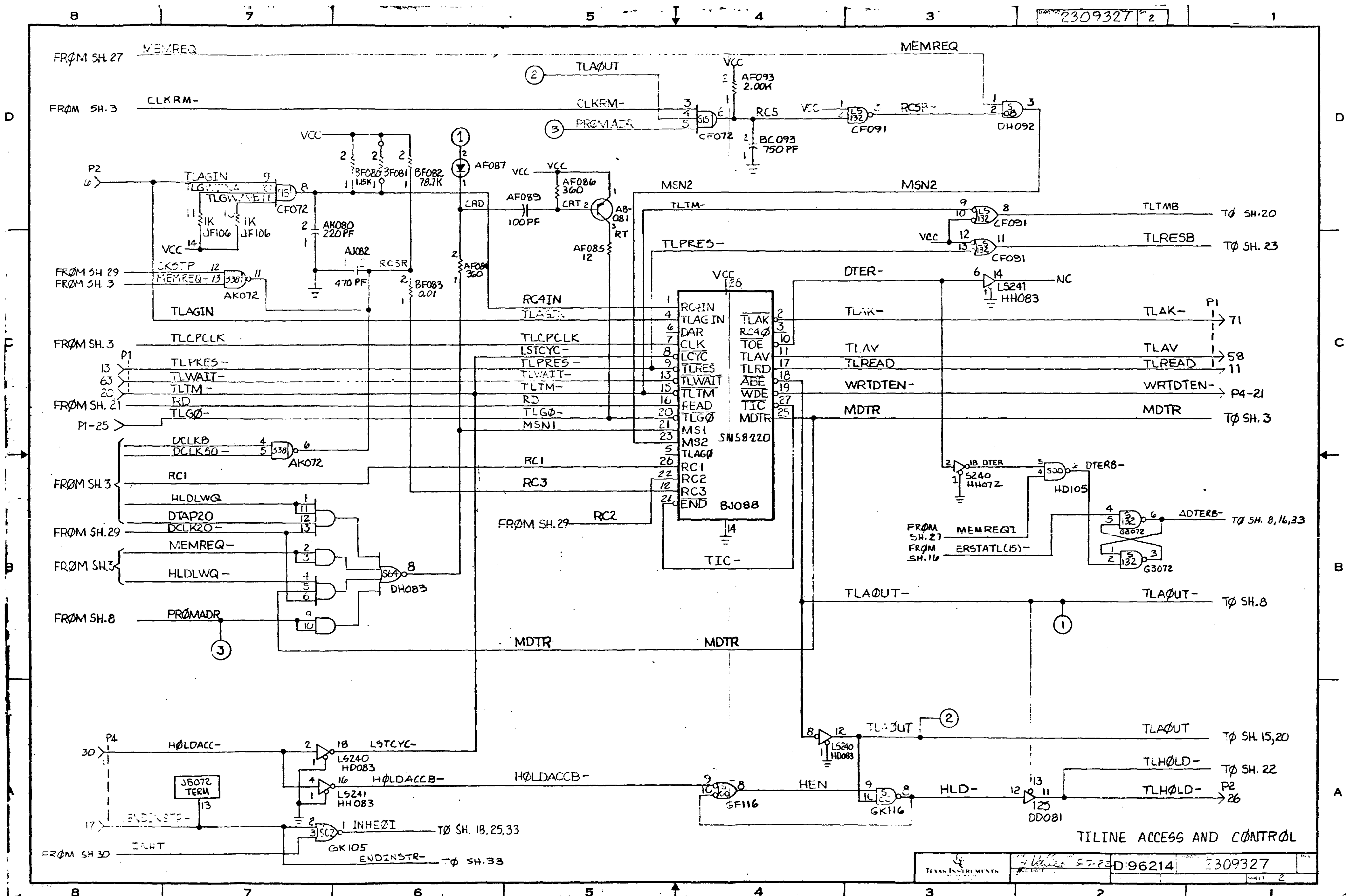
AUTO-INSERTED PARTS LIST FOR -0001

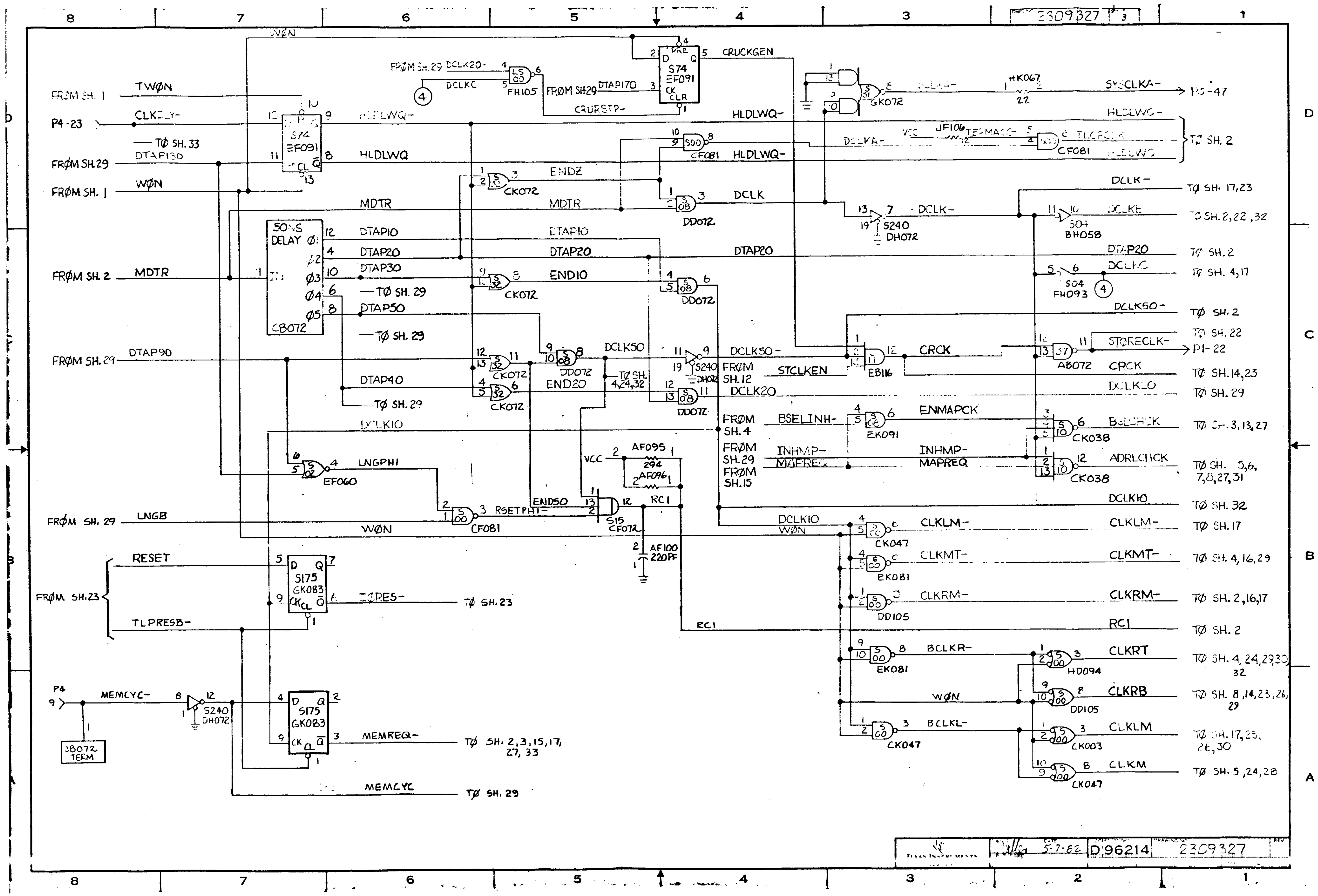
APPD. MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM2309325-5001 REV C

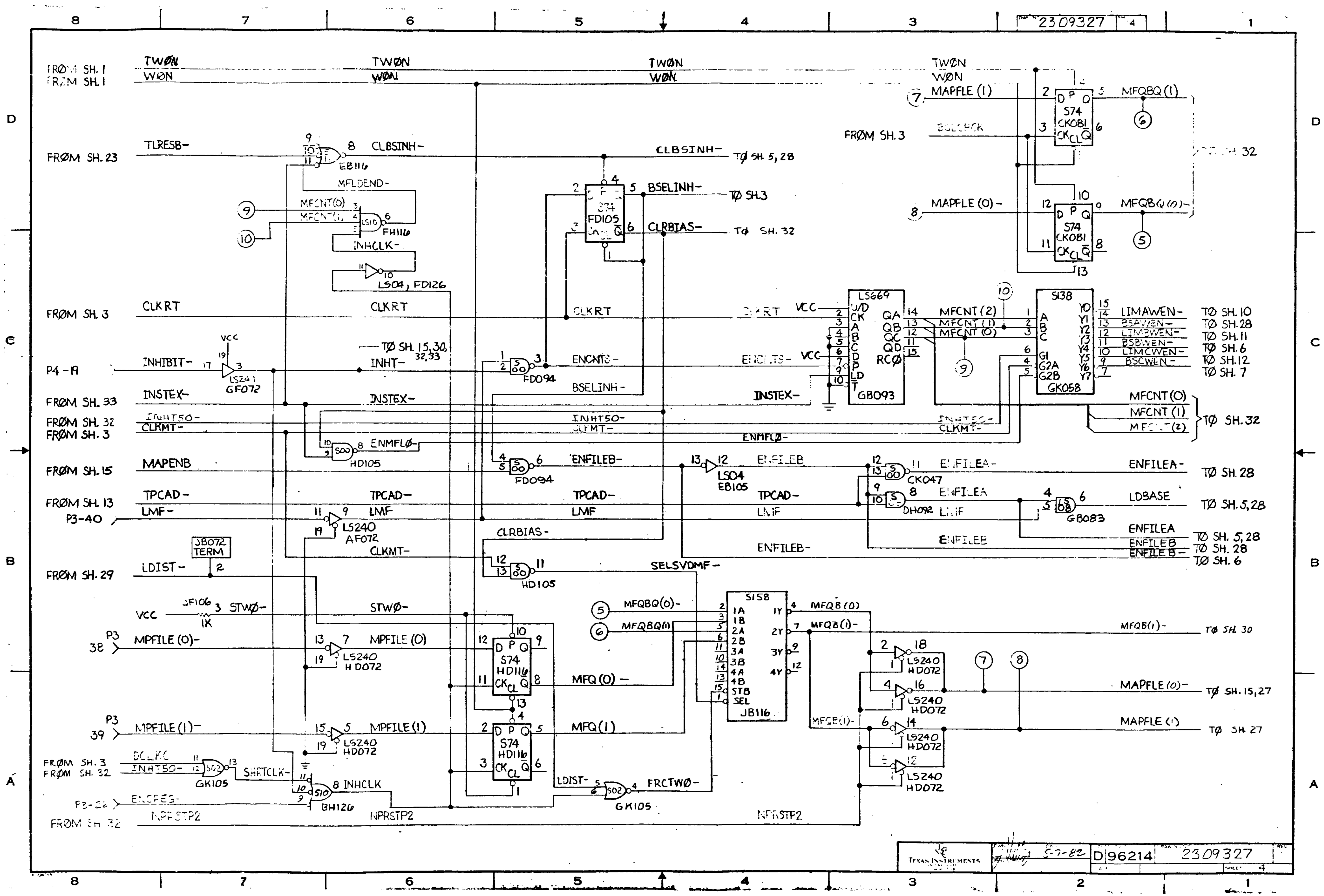
T.I. 25789

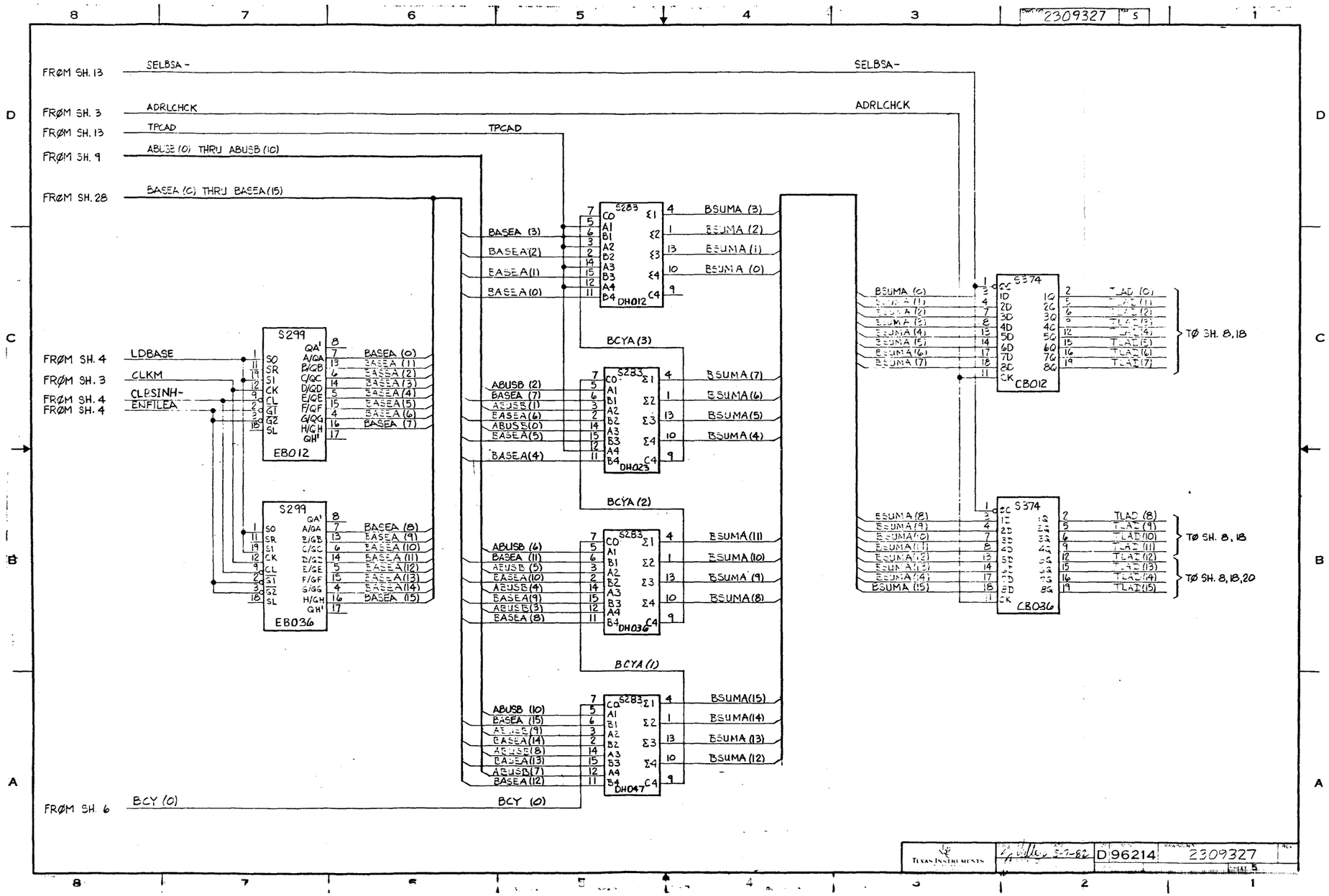


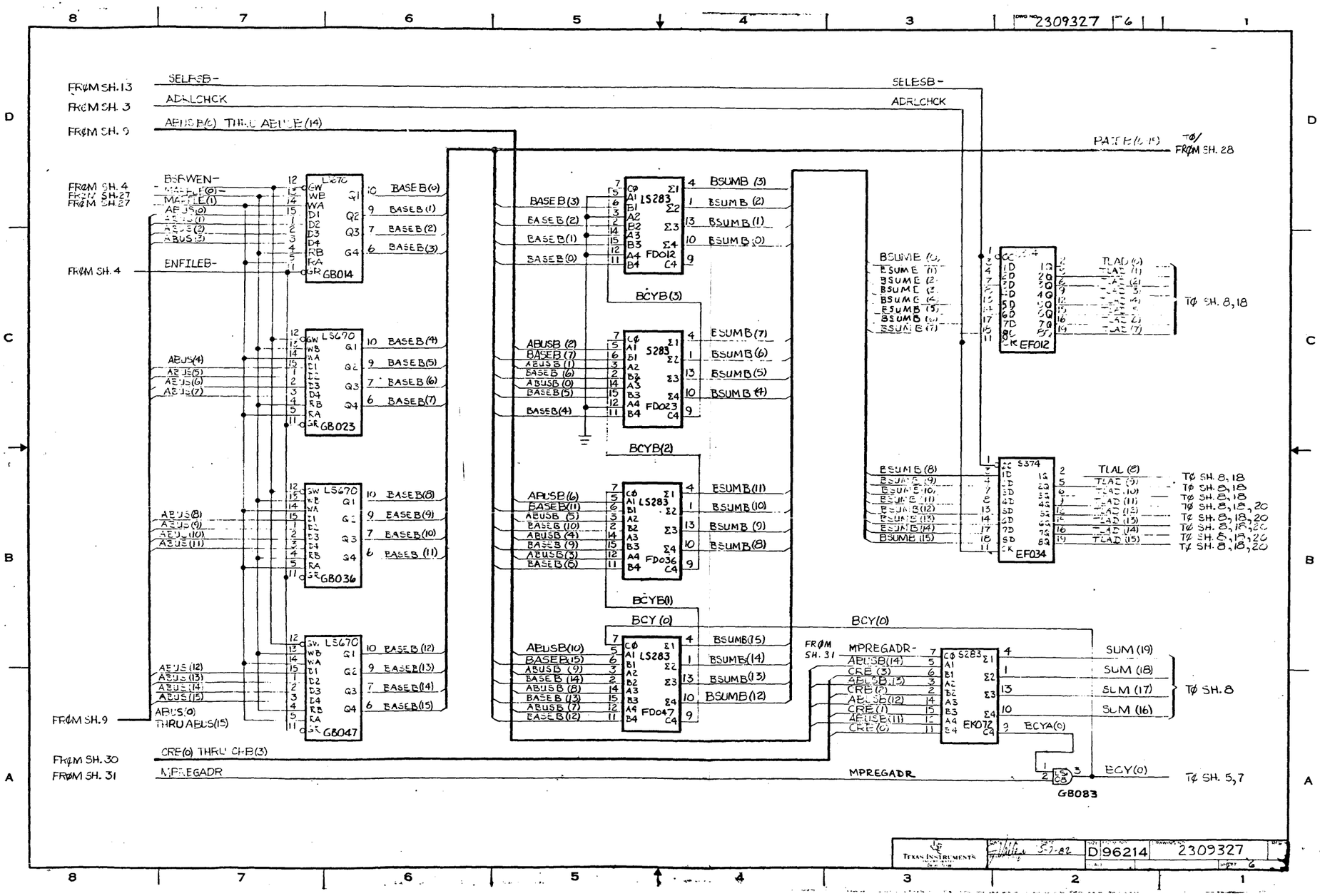
NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL DEVICE TYPES ARE PREFIXED WITH SN74.
2. VCC IS APPLIED TØ PIN 8 ØF ALL 8-PIN IC's, PIN 14 ØF ALL 14-PIN IC's, PIN 16 ØF ALL 16-PIN IC's, PIN 20 ØF ALL 20-PIN IC's, ETC.
3. GRØUND IS APPLIED TØ PIN 4 ØF ALL 8-PIN IC's, PIN 7 ØF ALL 14-PIN IC's, PIN 8 ØF ALL 16-PIN IC's, PIN 10 ØF ALL 20-PIN IC's, ETC.
4. DEVICE TYPE, PIN NUMBERS, AND LØCATIØN ØF IC IS SHØWN AS FØLLØWS:
LS00 AND LS04 = DEVICE TYPE
1, 2, AND 3 = PIN NUMBERS
DD105 AND BH058 = LØCATIØN
5. RESISTANCE VALUES ARE IN ØHMS.
6. RESISTØRS ARE 1/4 WATT, 5%.
7. CAPACITANCE VALUES ARE IN MICRØFARADS.
8. ◯ DENØTES THAT SHEET NØ. ØF ASSØCIATED LØGIC LIES WITHIN HEX.
9 HJ131 (SH.17) MAY BE 12K—200K AS NEEDED TØ GET TSTCLK WITHIN SPEC.
WØN
TWØN
SWØN
TØ ALL SHEETS
VCC
GND
AH001, GE001, AH069, HA069, AH137, HA137
39
BG001, CJ001, EA001, FC001
0.1
DD021, HH021, BD033, DD033, GB033, HH033, CK056, EK056, GH056, JD056, AB069, CC069, DE069, EG069, FJ069, HK069, CF089, EF089, GD091, AE103, BG103, CJ103, EA103, FC103, GE103, CF113, EK114, HB113, BH124, ED124, GK124, BG137, CJ137, EA137, FC137, GE137
CC001, DE001, EG001, FJ001, JD001, EK021, JD021, BK033, EK033, GH033, JD033, DF056, GB056, HH056, BG069, CJ069, EA069, FC069, GE069, JF069, JB081, DB089, FH091, BA103, CC103, DE103, EG103, FJ103, HA103, DB113, GD113, JB114, DH124, FH124, CC137, DE137, EG137, FJ137, JD137
.01
JH127 .01
JK014 .1
LØGIC DIAGRAM, 990/12, LR SMI
TEXAS INSTRUMENTS
SI-METRIC
D 06668
2309327

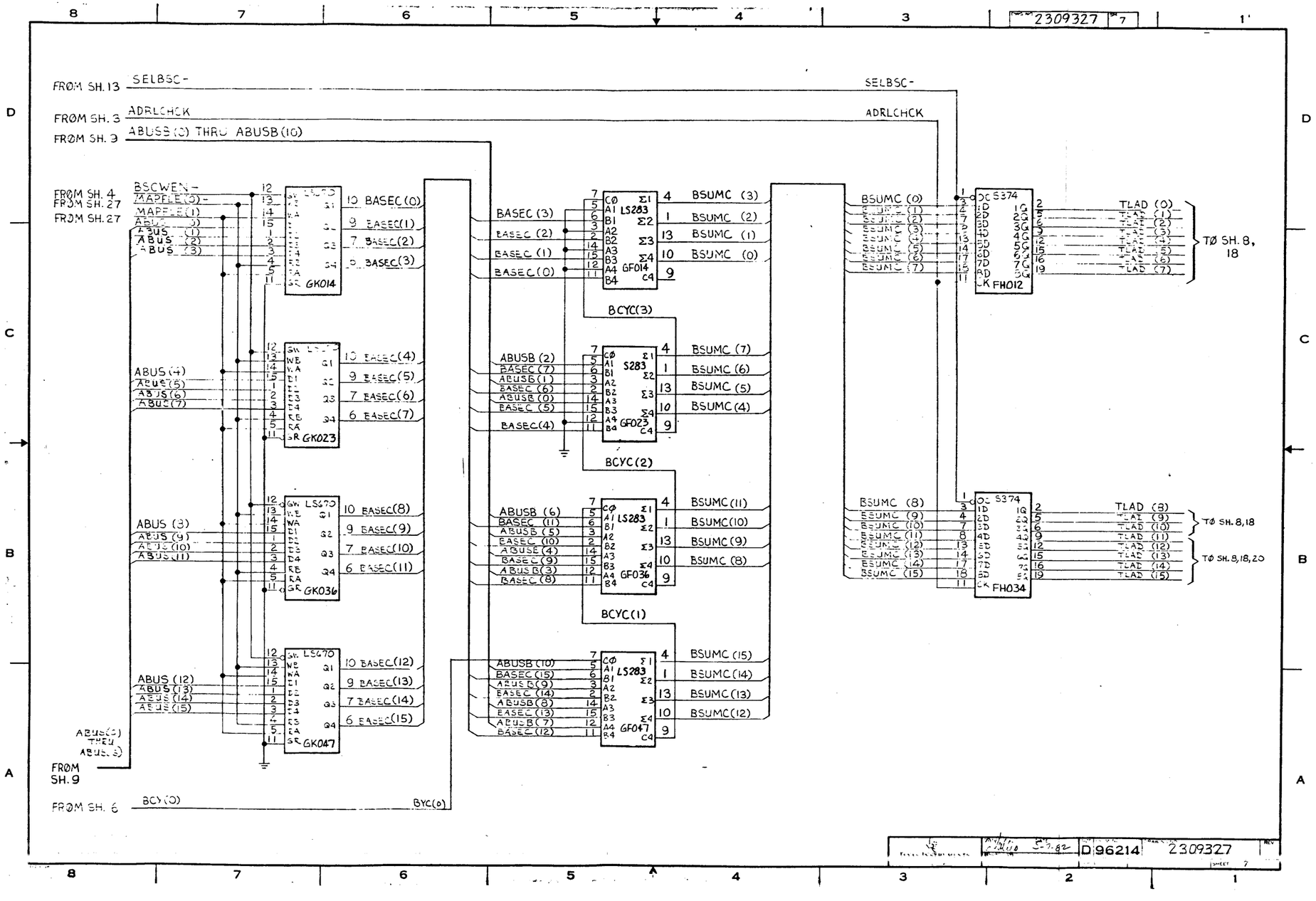

TILINE ACCESS AND CONTROL
D96214
2309327
SN58220
FROM SH. 27
FROM SH. 3
MEMREQ
CLKRM-
TLAOUT
PROMADR
MSN2
TLTMB
TO SH. 20
TLRESB
TO SH. 23
DTER-
TLAK-
TLAV
TLREAD
WRTDTEN-
MDTR
TO SH. 3
TLAOUT-
TO SH. 8
HOLDACC-
HOLDACCB-
HEN
HLD-
TLHOLD-
TO SH. 22
TO SH. 15,20
INHEOI
TO SH. 18,25,33
ENDINSTR-
TO SH. 33
ADTERB-
TO SH. 8,16,33

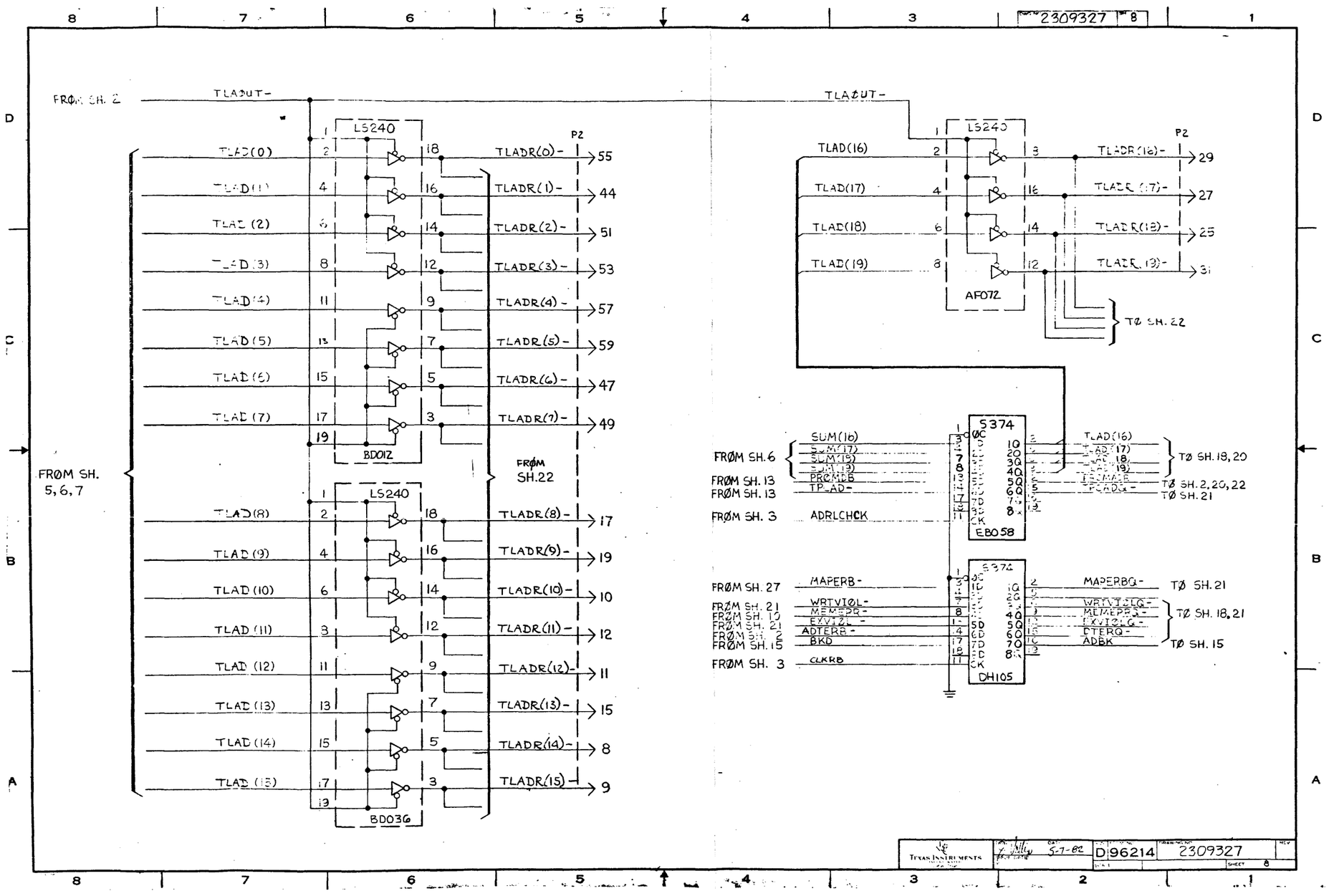

2309327
FROM SH. 1 TWØN
P4-23 CLK
FRØM SH.29 DTAP130
FRØM SH. 1 WØN
FRØM SH. 2 MDTR
FRØM SH. 29 DTAP90
FRØM SH. 29 LNGB
FRØM SH.23 RESET TLPRESB-
MEMCYC-
JB072 TERM
S74 EF091
HLDLWQ
50NS DELAY CB072
DTAP10 DTAP20 DTAP30 DTAP50 DTAP40
ENDZ END10 END20 END50
CK072 DD072 DD072 EF060 CF081 CF072
LNGPHI RSETPHI
AF095 294 AF096 AF100 220PF
RC1
S175 GK083
MEMREQ- TØ SH. 2,3,15,17, 27, 33
MEMCYC TØ SH. 29
CRUCKGEN CRURSTP-
FH105
SYSCLKA- P5-47
HLDLWQ- TØ SH. 2
DCLK- TØ SH. 17,23
TØ SH. 2,22,32
DTAP20 TØ SH. 2
DCLKC TØ SH. 4,17
DCLK50- TØ SH. 2
STØRECLK- P1-22
CRCK TØ SH. 14,23
DCLK20 TØ SH. 29
ENMAPCK
TØ SH. 3,13,27
ADRLCHCK TØ SH. 5,6, 7,8,27,31
DCLK10 TØ SH. 32
CLKLM- TØ SH. 17
CLKMT- TØ SH. 4,16,29
CLKRM- TØ SH. 2,16,17
RC1 TØ SH. 2
BCLKR- CLKRT TØ SH. 4,24,29,30, 32
CLKRB TØ SH. 8,14,23,26, 29
BCLKL- CLKLM TØ SH. 17,25, 26,30
CLKM TØ SH. 5,24,28
STCLKEN BSELINH- INHMP- MAPREQ
EB16 AB072 EK091 CK038 CK047 EK081 DD105 HD094 CK003 DH072 BH058 FH093
D 96214 2309327

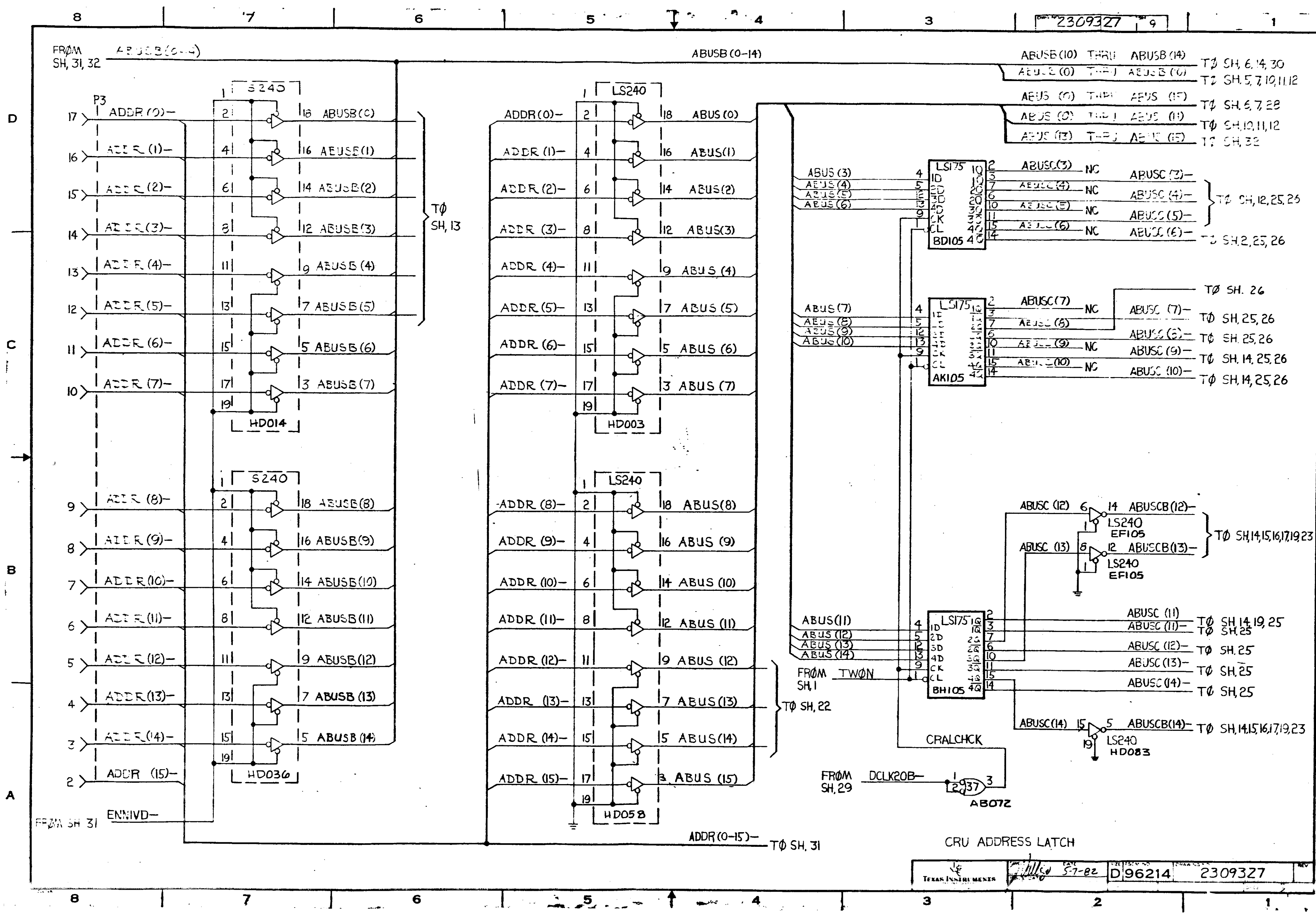

2309327
FROM SH. 1
TWON
WON
FROM SH. 23
TLRESB-
CLBSINH-
EB116
MFLDEND-
FH116
INHCLK-
LS04, FD126
S74
FD105
BSELINH-
TO SH.3
CLRBIAS-
TO SH. 32
TO SH 5,28
FROM SH. 3
CLKRT
P4-19
INHIBIT-
LS241
GF072
INHT-
TO SH. 15,30, 32,33
ENCNTS-
FD094
BSELINH-
FROM SH. 33
INSTEX-
FROM SH. 32
FROM SH. 3
INHTSO-
CLKMT-
ENMFLØ-
HD105
FROM SH. 15
MAPENB
ENFILEB-
LS04
EB105
FROM SH. 13
P3-40
TPCAD-
LMF-
LS240
AF072
CLKMT-
CLRBIAS-
SELSVDMF-
HD105
JB072
TERM
FROM SH. 29
LDIST-
VCC
STWØ-
MPFILE (0)-
MPFILE (1)-
LS240
HD072
S74
HD116
MFQ (0)-
MFQ (1)
FROM SH. 3
FROM SH. 32
DCLKC
INHTSO-
GK105
SHFTCLK-
INHCLK
BH126
ENCREG-
FROM SH 32
NPRSTP2
LDIST-
FRCTWØ-
GK105
MFQBQ(0)-
MFQBQ(1)
S158
JB116
MFQB(0)
MFQB(1)-
TO SH. 30
MAPFLE (0)-
TO SH. 15,27
MAPFLE (1)
TO SH. 27
LS669
GB093
MFCNT (2)
MFCNT (1)
MFCNT (0)
S138
GK058
LIMAWEN-
TO SH. 10
TO SH. 28
TO SH. 11
TO SH. 6
TO SH. 12
TO SH. 7
MFCNT (0)
MFCNT (1)
TO SH. 32
ENFILEA-
TO SH. 28
CK047
DH092
LDBASE
GB083
TO SH. 5,28
ENFILEA
ENFILEB
TO SH. 5,28
TO SH. 28
TO SH. 6
MAPFLE (1)
MAPFLE (0)-
MFQBQ (1)
MFQBQ (0)-
S74
CK081
TEXAS INSTRUMENTS
D 96214
2309327

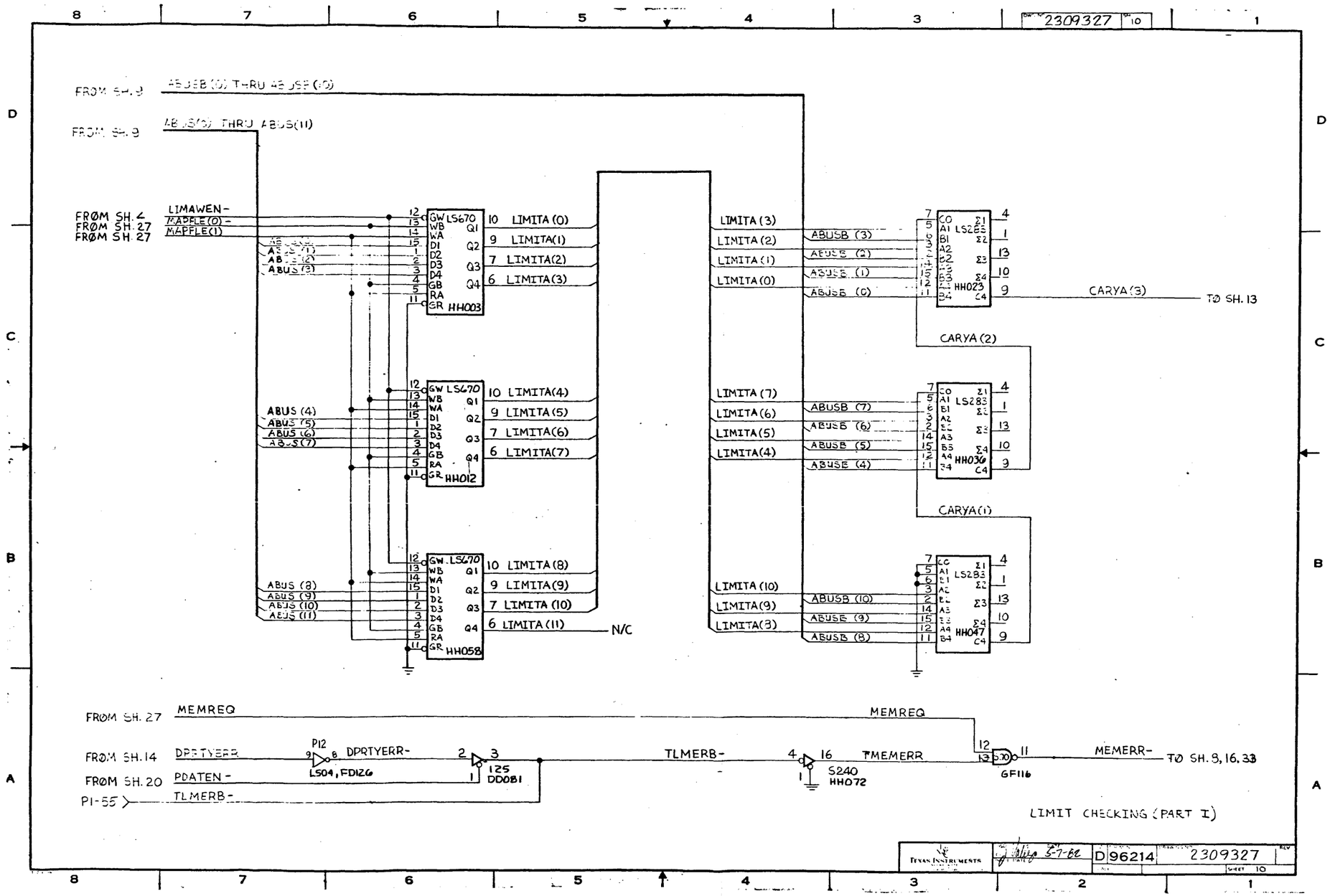

2309327
FRØM SH. 13 SELBSA-
SELBSA-
FRØM SH. 3 ADRLCHCK
ADRLCHCK
FRØM SH. 13 TPCAD
TPCAD
FRØM SH. 9 ABUSB (0) THRU ABUSB (10)
FRØM SH. 28 BASEA (0) THRU BASEA (15)
FRØM SH. 4 LDBASE
FRØM SH. 3 CLKM
FRØM SH. 4 CLRSINH-
FRØM SH. 4 ENFILEA
S299
EB012
S299
EB036
S283
DH012
S283
DH023
S283
DH036
S283
DH047
S374
CB012
S374
CB036
BCYA (3)
BCYA (2)
BCYA (1)
FRØM SH. 6 BCY (0)
BCY (0)
TØ SH. 8, 18
TØ SH. 8, 18
TØ SH. 8, 18, 20
TEXAS INSTRUMENTS
D96214
2309327

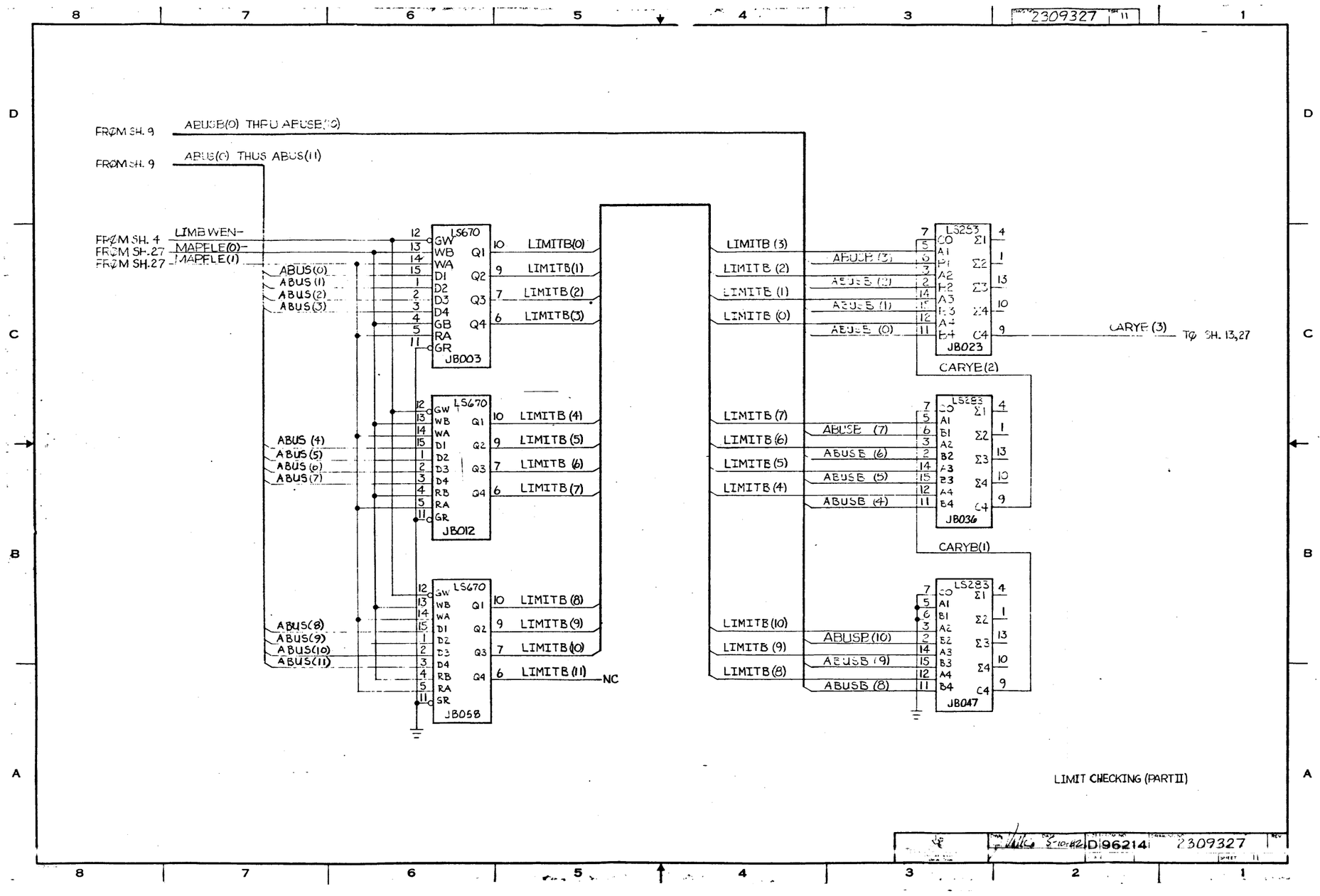

2309327
FROM SH. 13
SELESB-
FROM SH. 3
ADRLCHCK
FROM SH. 9
ABUSB(0) THRU ABUSB(14)
PARERR(0-15)
TO/FROM SH. 28
FROM SH. 4
FROM SH. 27
FROM SH. 27
BSRWEN-
ABUS(0)
ABUS(1)
ABUS(2)
ABUS(3)
ENFILEB-
FROM SH. 4
LS670
GB014
BASEB(0)
BASEB(1)
BASEB(2)
BASEB(3)
ABUS(4)
ABUS(5)
ABUS(6)
ABUS(7)
GB023
BASEB(4)
BASEB(5)
BASEB(6)
BASEB(7)
ABUS(8)
ABUS(9)
ABUS(10)
ABUS(11)
GB036
BASEB(8)
BASEB(9)
BASEB(10)
BASEB(11)
ABUS(12)
ABUS(13)
ABUS(14)
ABUS(15)
GB047
BASEB(12)
BASEB(13)
BASEB(14)
BASEB(15)
FROM SH. 9
ABUS(0) THRU ABUS(15)
LS283
FD012
BSUMB(0)
BSUMB(1)
BSUMB(2)
BSUMB(3)
BCYB(3)
FD023
BSUMB(4)
BSUMB(5)
BSUMB(6)
BSUMB(7)
BCYB(2)
FD036
BSUMB(8)
BSUMB(9)
BSUMB(10)
BSUMB(11)
BCYB(1)
FD047
BSUMB(12)
BSUMB(13)
BSUMB(14)
BSUMB(15)
BCY(0)
SELESB-
ADRLCHCK
BSUMB(0)
BSUMB(1)
BSUMB(2)
BSUMB(3)
BSUMB(4)
BSUMB(5)
BSUMB(6)
BSUMB(7)
EF012
TLAD(0)
TLAD(1)
TLAD(2)
TLAD(3)
TLAD(4)
TLAD(5)
TLAD(6)
TLAD(7)
TO SH. 8,18
BSUMB(8)
BSUMB(9)
BSUMB(10)
BSUMB(11)
BSUMB(12)
BSUMB(13)
BSUMB(14)
BSUMB(15)
S374
EF034
TLAD(8)
TLAD(9)
TLAD(10)
TLAD(11)
TLAD(12)
TLAD(13)
TLAD(14)
TLAD(15)
TO SH. 8,18
TO SH. 8,18
TO SH. 8,18
TO SH. 8,18,20
TO SH. 8,18,20
TO SH. 8,18,20
TO SH. 8,18,20
TO SH. 8,18,20
FROM SH. 31
MPREGADR-
ABUSB(14)
CRE(3)
ABUSB(13)
CRE(2)
ABUSB(12)
CRE(1)
ABUSB(11)
CRE(0)
EK012
SUM(19)
SUM(18)
SUM(17)
SUM(16)
TO SH. 8
ECYA(0)
BCY(0)
BCY(0)
GB083
TO SH. 5,7
FROM SH. 30
CRE(0) THRU CRB(3)
FROM SH. 31
MPREGADR
MPREGADR
TEXAS INSTRUMENTS
5-7-82
D96214
2309327

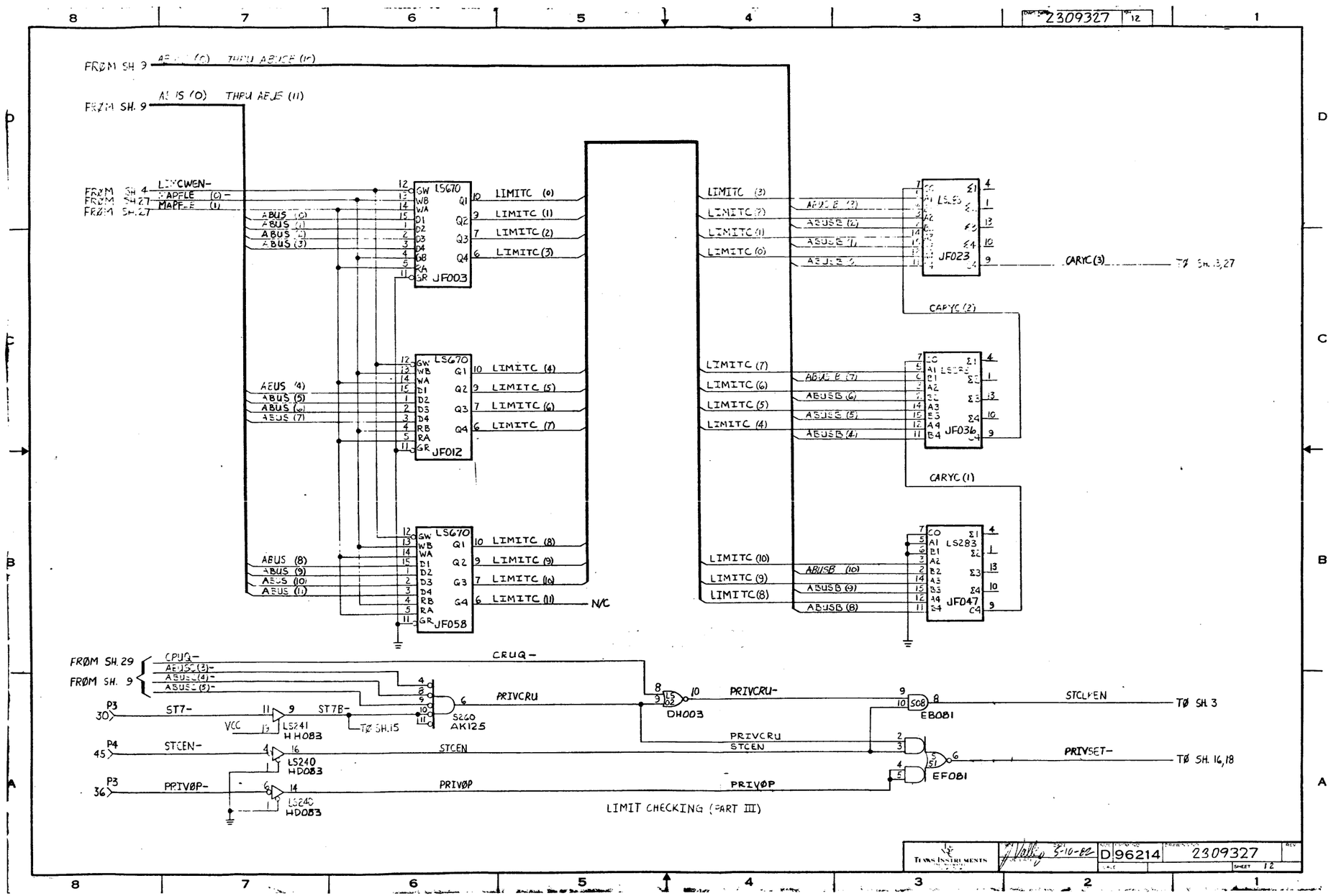

2309327
FROM SH. 13 SELBSC-
SELBSC-
FROM SH. 3 ADRLCHCK
ADRLCHCK
FROM SH. 3 ABUSB(0) THRU ABUSB(10)
FROM SH. 4 BSCWEN-
FROM SH. 27 MAPELE(3)-
FROM SH. 27 MAPELE(1)
ABUS (2)
ABUS (1)
ABUS (3)
GK014
BASEC(0)
BASEC(1)
BASEC(2)
BASEC(3)
ABUS(4)
ABUS(5)
ABUS(6)
ABUS(7)
GK023
BASEC(4)
BASEC(5)
BASEC(6)
BASEC(7)
ABUS (3)
ABUS (9)
ABUS (10)
ABUS (11)
GK036
BASEC(8)
BASEC(9)
BASEC(10)
BASEC(11)
ABUS (12)
ABUS (13)
ABUS (14)
ABUS (15)
GK047
BASEC(12)
BASEC(13)
BASEC(14)
BASEC(15)
ABUS(0) THRU ABUS(3)
FROM SH.9
FROM SH. 6 BCYC(0)
BYC(0)
BASEC (3)
BASEC (2)
BASEC (1)
BASEC (0)
LS283
GF014
BSUMC (3)
BSUMC (2)
BSUMC (1)
BSUMC (0)
BCYC(3)
ABUSB (2)
BASEC (7)
ABUSB (1)
BASEC (6)
ABUSB (0)
BASEC (5)
BASEC(4)
S283
GF023
BSUMC (7)
BSUMC (6)
BSUMC (5)
BSUMC(4)
BCYC(2)
ABUSB (6)
BASEC (11)
ABUSB (5)
BASEC (10)
ABUSE(4)
BASEC (9)
ABUSB(3)
BASEC (8)
GF036
BSUMC(11)
BSUMC(10)
BSUMC (9)
BSUMC (8)
BCYC(1)
ABUSB (10)
BASEC (15)
ABUSB(9)
BASEC (14)
ABUSB(8)
BASEC (13)
ABUSB(7)
BASEC (12)
GF047
BSUMC (15)
BSUMC (14)
BSUMC (13)
BSUMC (12)
BSUMC (0)
BSUMC (1)
BSUMC (2)
BSUMC (3)
BSUMC (4)
BSUMC (5)
BSUMC (6)
BSUMC (7)
S374
FH012
TLAD (0)
TLAD (1)
TLAD (2)
TLAD (3)
TLAD (4)
TLAD (5)
TLAD (6)
TLAD (7)
TØ SH. 8, 18
BSUMC (8)
BSUMC (9)
BSUMC (10)
BSUMC (11)
BSUMC (12)
BSUMC (13)
BSUMC (14)
BSUMC (15)
FH034
TLAD (8)
TLAD (9)
TLAD (10)
TLAD (11)
TLAD (12)
TLAD (13)
TLAD (14)
TLAD (15)
TØ SH. 8, 18
TØ SH. 8, 18, 20
D96214
2309327

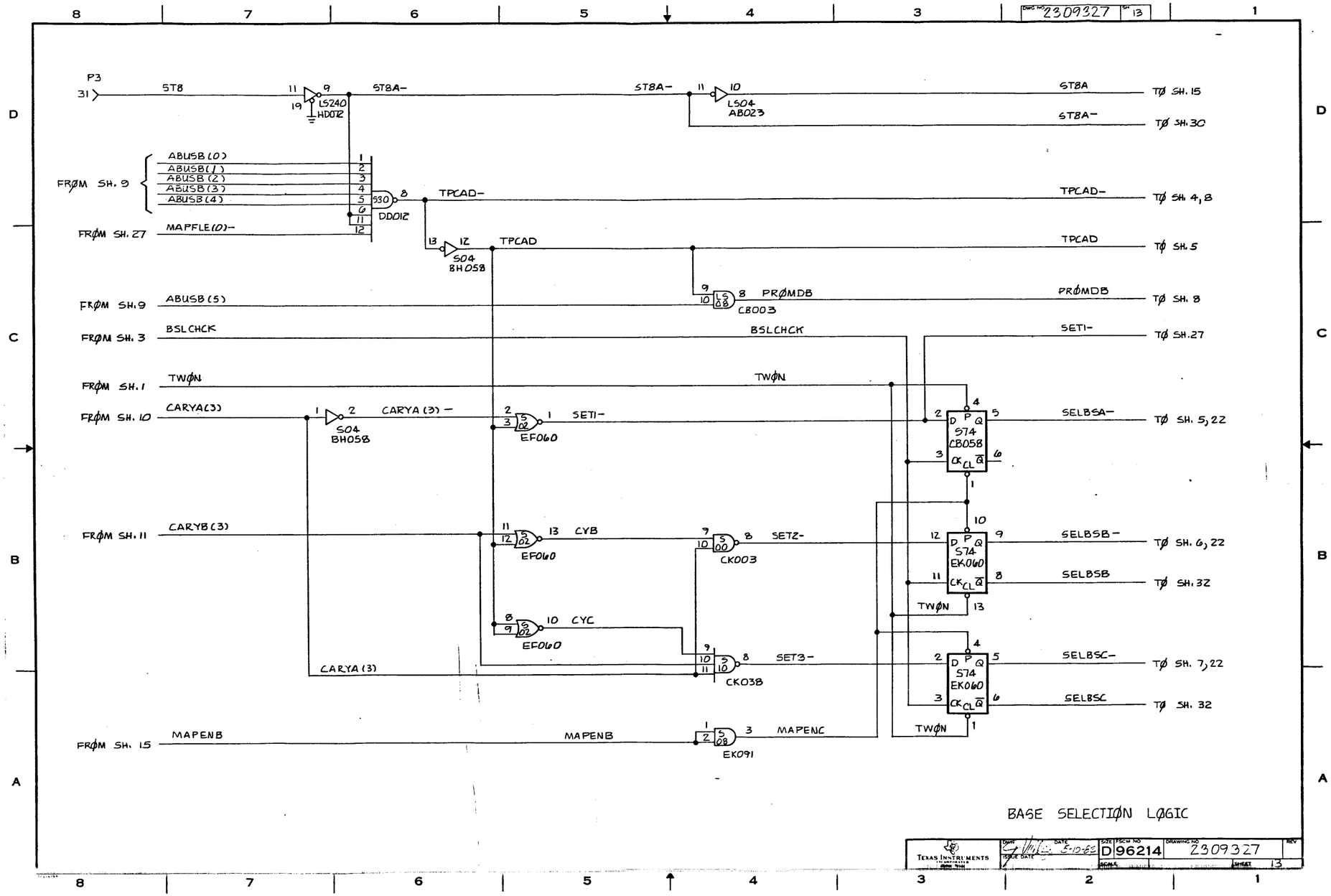

2309327
FROM SH. 2
TLADUT-
LS240
BDOIZ
TLAD(0)
TLAD(1)
TLAD(2)
TLAD(3)
TLAD(4)
TLAD(5)
TLAD(6)
TLAD(7)
TLADR(0)-
TLADR(1)-
TLADR(2)-
TLADR(3)-
TLADR(4)-
TLADR(5)-
TLADR(6)-
TLADR(7)-
55
44
51
53
57
59
47
49
FROM SH. 5, 6, 7
FROM SH. 22
LS240
BD036
TLAD(8)
TLAD(9)
TLAD(10)
TLAD(11)
TLAD(12)
TLAD(13)
TLAD(14)
TLAD(15)
TLADR(8)-
TLADR(9)-
TLADR(10)-
TLADR(11)-
TLADR(12)-
TLADR(13)-
TLADR(14)-
TLADR(15)-
17
19
10
12
11
15
8
9
TLADUT-
LS240
AF072
TLAD(16)
TLAD(17)
TLAD(18)
TLAD(19)
TLADR(16)-
TLADR(17)-
TLADR(18)-
TLADR(19)-
29
27
25
31
TO SH. 22
5374
EB058
FROM SH. 6
SUM(16)
SUM(17)
SUM(18)
SUM(19)
FROM SH. 13
PRCMEB
FROM SH. 13
TP-AD-
FROM SH. 3
ADRLCHCK
TLAD(16)
TLAD(17)
TLAD(18)
TLAD(19)
TO SH. 18, 20
TO SH. 2, 20, 22
TO SH. 21
5374
DH105
FROM SH. 27
MAPERB-
FROM SH. 21
WRTVIOL-
FROM SH. 10
MEMEPER-
FROM SH. 21
EXVIOL-
FROM SH. 2
ADTERR-
FROM SH. 15
BKD
FROM SH. 3
CLKRB
MAPERBQ-
WRTVIOLQ-
MEMEPERQ-
EXVIOLQ-
DTERQ-
ADBK
TO SH. 21
TO SH. 18, 21
TO SH. 15
TEXAS INSTRUMENTS
5-7-82
D96214
2309327
SHEET 8

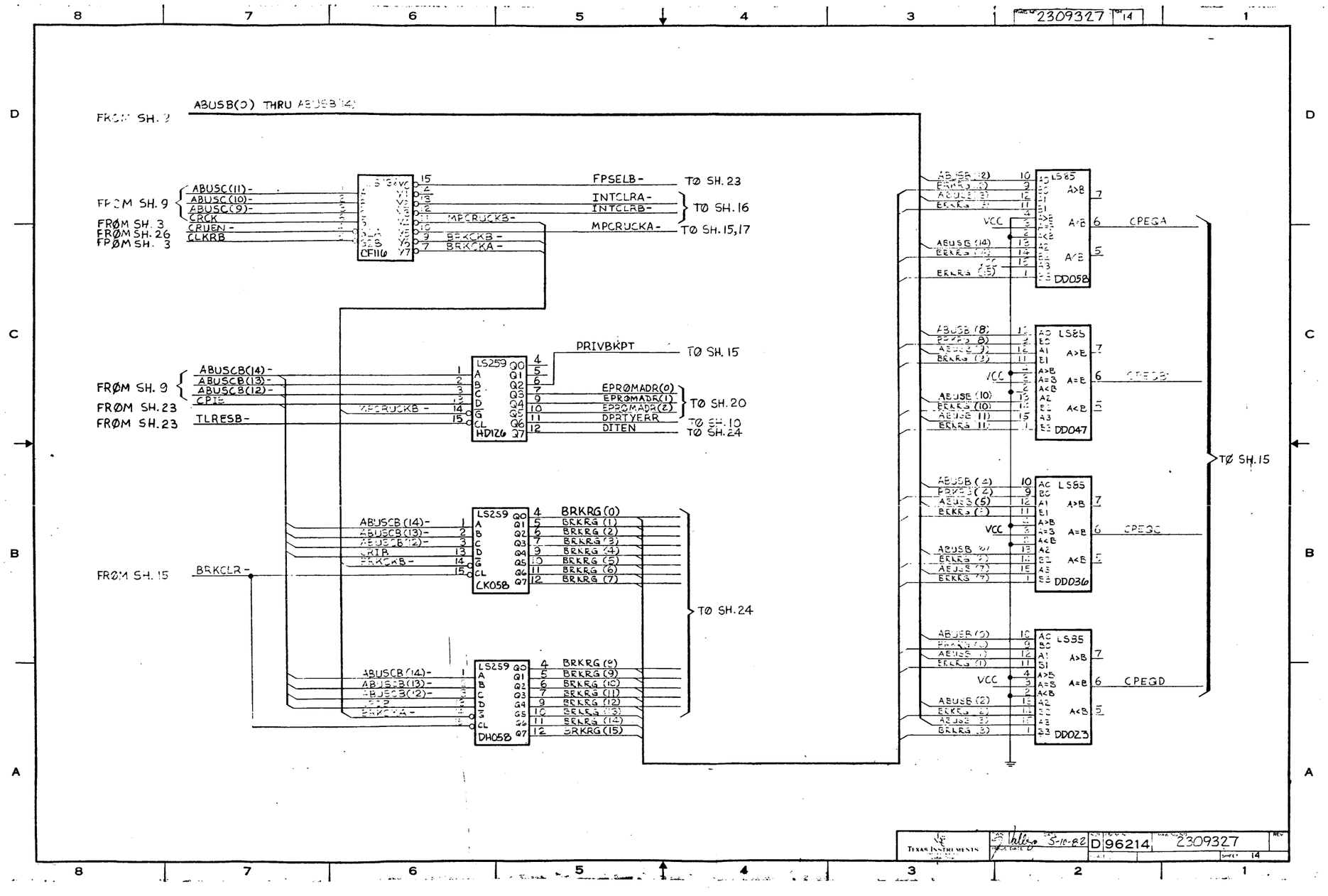

CRU ADDRESS LATCH
2309327
D 96214
ABUSB (0-14)
ADDR (0-15)– TØ SH, 31
LS240
LS175
HD014
HD036
HD003
HD058
BD105
AK105
BH105
EF105
HD083
AB072
CRALCHCK
FRØM DCLK20B
FRØM TWØN SH, 1
ENNIVD–
TØ SH, 13
TØ SH, 22

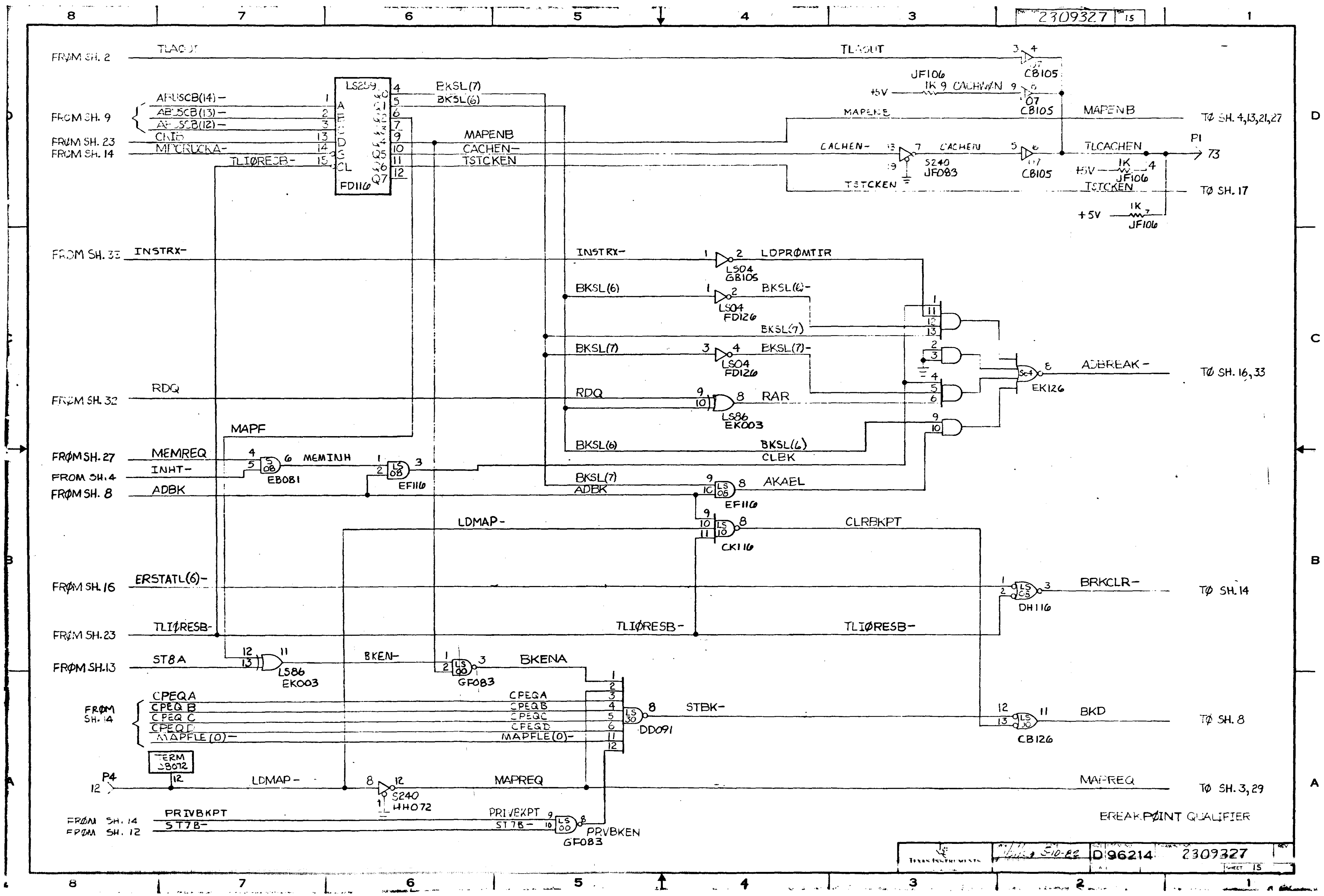

2309327
10
FROM SH. 9
ABUSB (0) THRU ABUSB (9)
FROM SH. 9
ABUS(0) THRU ABUS(11)
FROM SH. 4
FROM SH. 27
FROM SH. 27
LIMAWEN-
MAPPLE(0)-
MAPPLE(1)
GW LS670
WB
WA
D1
D2
D3
D4
GB
RA
GR
HH003
Q1
Q2
Q3
Q4
LIMITA(0)
LIMITA(1)
LIMITA(2)
LIMITA(3)
ABUS (1)
ABUS (2)
ABUS (3)
HH012
ABUS (4)
ABUS (5)
ABUS (6)
ABUS (7)
LIMITA(4)
LIMITA(5)
LIMITA(6)
LIMITA(7)
HH058
ABUS (8)
ABUS (9)
ABUS (10)
ABUS (11)
LIMITA(8)
LIMITA(9)
LIMITA(10)
LIMITA(11)
N/C
LIMITA (3)
LIMITA (2)
LIMITA (1)
LIMITA (0)
ABUSB (3)
ABUSB (2)
ABUSB (1)
ABUSB (0)
CO
A1
B1
A2
B2
A3
B3
A4
B4
LS283
HH023
C4
Σ1
Σ2
Σ3
Σ4
CARYA(3)
TØ SH. 13
CARYA(2)
LIMITA (7)
LIMITA (6)
LIMITA (5)
LIMITA (4)
ABUSB (7)
ABUSB (6)
ABUSB (5)
ABUSB (4)
HH030
CARYA(1)
LIMITA (10)
LIMITA (9)
LIMITA (8)
ABUSB (10)
ABUSB (9)
ABUSB (8)
HH047
FROM SH. 27
MEMREQ
MEMREQ
FROM SH. 14
DPRTYERR
P12
DPRTYERR-
LS04, FD126
FROM SH. 20
PDATEN-
P1-55
TLMERB-
TLMERB-
TMEMERR
S240
HH072
GF116
MEMERR-
TO SH. 8, 16, 33
LIMIT CHECKING (PART I)
TEXAS INSTRUMENTS
D 96214
2309327
SHEET 10

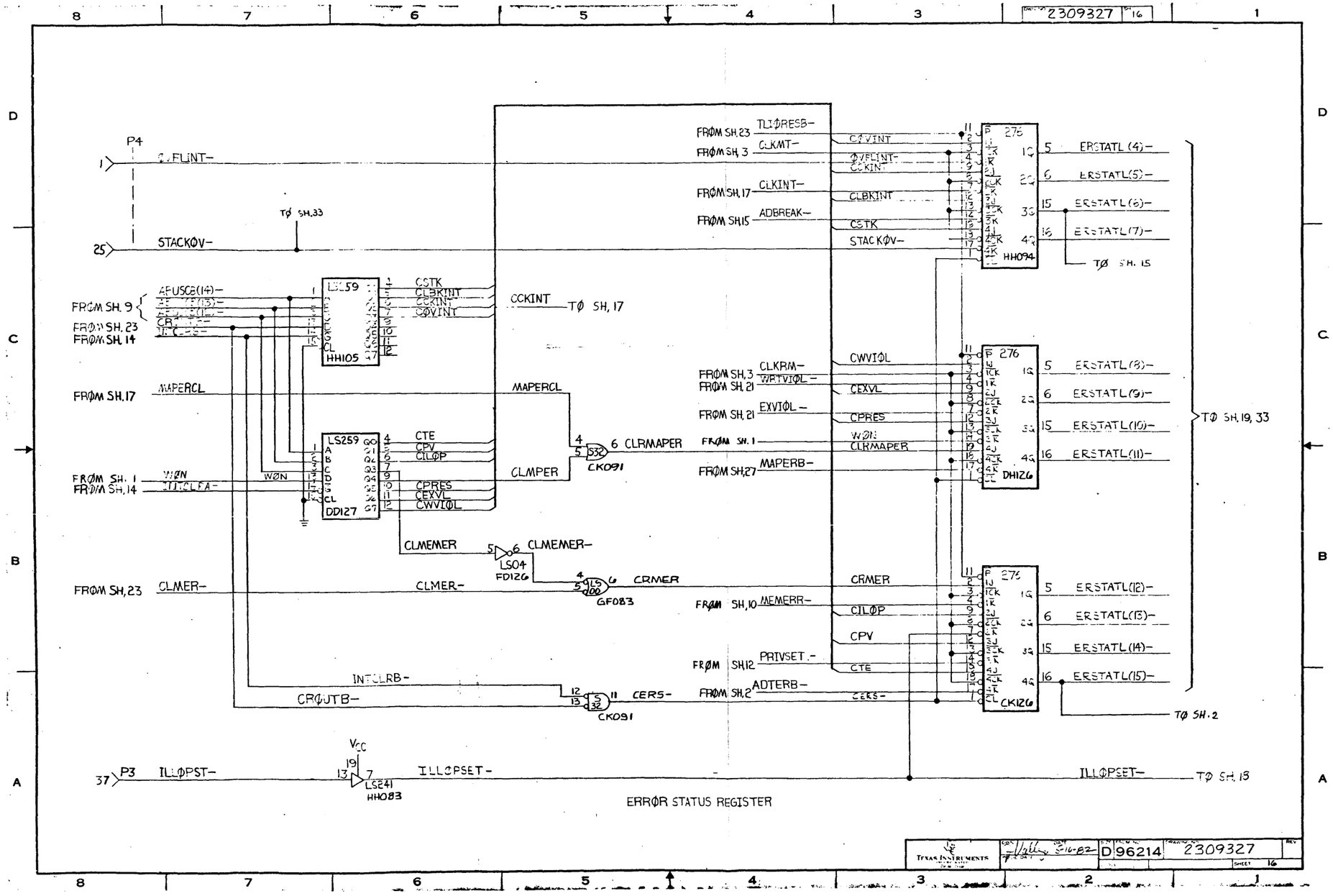

2309327
FROM SH. 9
ABUSB(0) THRU ABUSB(3)
FROM SH. 9
ABUS(0) THUS ABUS(11)
FROM SH. 4
FROM SH. 27
FROM SH. 27
LIMBWEN-
MAPELE(0)-
MAPELE(1)
ABUS(0)
ABUS(1)
ABUS(2)
ABUS(3)
ABUS (4)
ABUS(5)
ABUS(6)
ABUS(7)
ABUS(8)
ABUS(9)
ABUS(10)
ABUS(11)
LS670
JB003
JB012
JB058
LIMITB(0)
LIMITB(1)
LIMITB(2)
LIMITB(3)
LIMITB (4)
LIMITB (5)
LIMITB (6)
LIMITB (7)
LIMITB (8)
LIMITB (9)
LIMITB(10)
LIMITB (11)
NC
LIMITB (3)
LIMITB (2)
LIMITB (1)
LIMITB (0)
LIMITB (7)
LIMITB (6)
LIMITB (5)
LIMITB (4)
LIMITB (10)
LIMITB (9)
LIMITB (8)
ABUSB (3)
ABUSB (2)
ABUSB (1)
ABUSB (0)
ABUSB (7)
ABUSB (6)
ABUSB (5)
ABUSB (4)
ABUSP(10)
ABUSB (9)
ABUSB (8)
LS283
JB023
JB036
JB047
CARYB (3)
TO SH. 13,27
CARYB(2)
CARYB(1)
LIMIT CHECKING (PARTII)
D96214
2309327

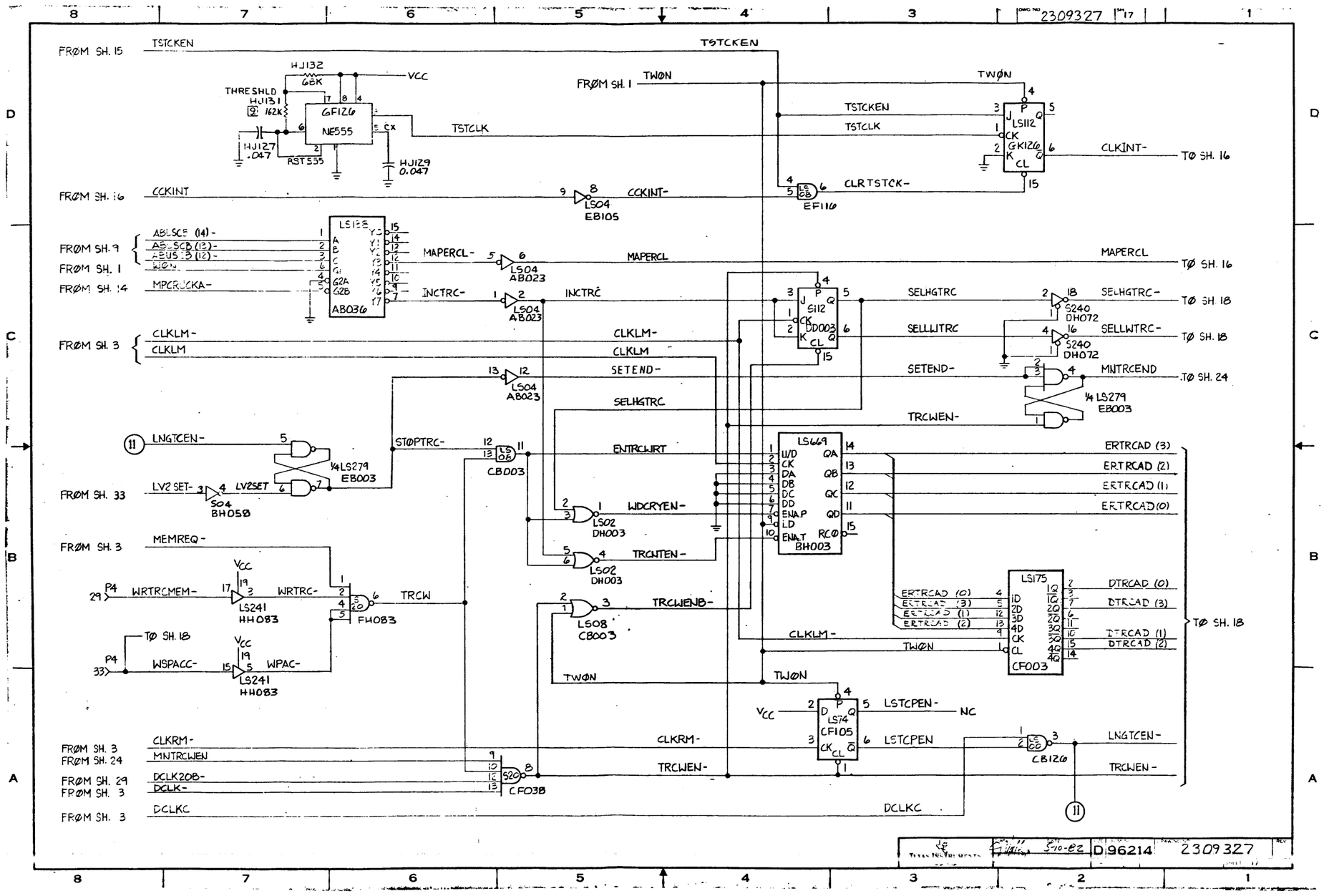

2309327 12
FROM SH 9 AB IS (0) THRU ABUSE (10)
FROM SH. 9 AB IS (0) THRU AEJE (11)
FROM SH 4 LIMCWEN-
FROM SH 27 MAPFLE (0)-
FROM SH.27 MAPFLE (1)
ABUS (0)
ABUS (1)
ABUS (2)
ABUS (3)
LS670 JF003
LIMITC (0)
LIMITC (1)
LIMITC (2)
LIMITC (3)
AEUS (4)
ABUS (5)
ABUS (6)
ABUS (7)
LS670 JF012
LIMITC (4)
LIMITC (5)
LIMITC (6)
LIMITC (7)
ABUS (8)
ABUS (9)
ABUS (10)
ABUS (11)
LS670 JF058
LIMITC (8)
LIMITC (9)
LIMITC (10)
LIMITC (11)
N/C
LIMITC (3)
LIMITC (2)
LIMITC (1)
LIMITC (0)
ABUSB (3)
ABUSB (2)
ABUSB (1)
AEJEB 0
LS283 JF023
CARYC (3)
TØ SH. 3,27
CARYC (2)
LIMITC (7)
LIMITC (6)
LIMITC (5)
LIMITC (4)
ABUSB (7)
ABUSB (6)
ABUSB (5)
ABUSB (4)
LS283 JF036
CARYC (1)
LIMITC (10)
LIMITC (9)
LIMITC (8)
ABUSB (10)
ABUSB (9)
ABUSB (8)
LS283 JF047
FROM SH. 29 CPUQ-
FROM SH. 9 ABUSB (3)-
ABUSB (4)-
ABUSB (5)-
CRUQ-
P3 30 ST7-
ST7B-
LS241 HH083
TØ SH.15
S260 AK125
PRIVCRU
DH003
PRIVCRU-
S08 EB081
STCLKEN
TØ SH. 3
P4 45 STCEN-
LS240 HD083
STCEN
PRIVCRU
STCEN
EF081
PRIVSET-
TØ SH. 16,18
P3 36 PRIVØP-
LS240 HD083
PRIVØP
PRIVØP
LIMIT CHECKING (PART III)
TEXAS INSTRUMENTS
D 96214
2309327
SHEET 12

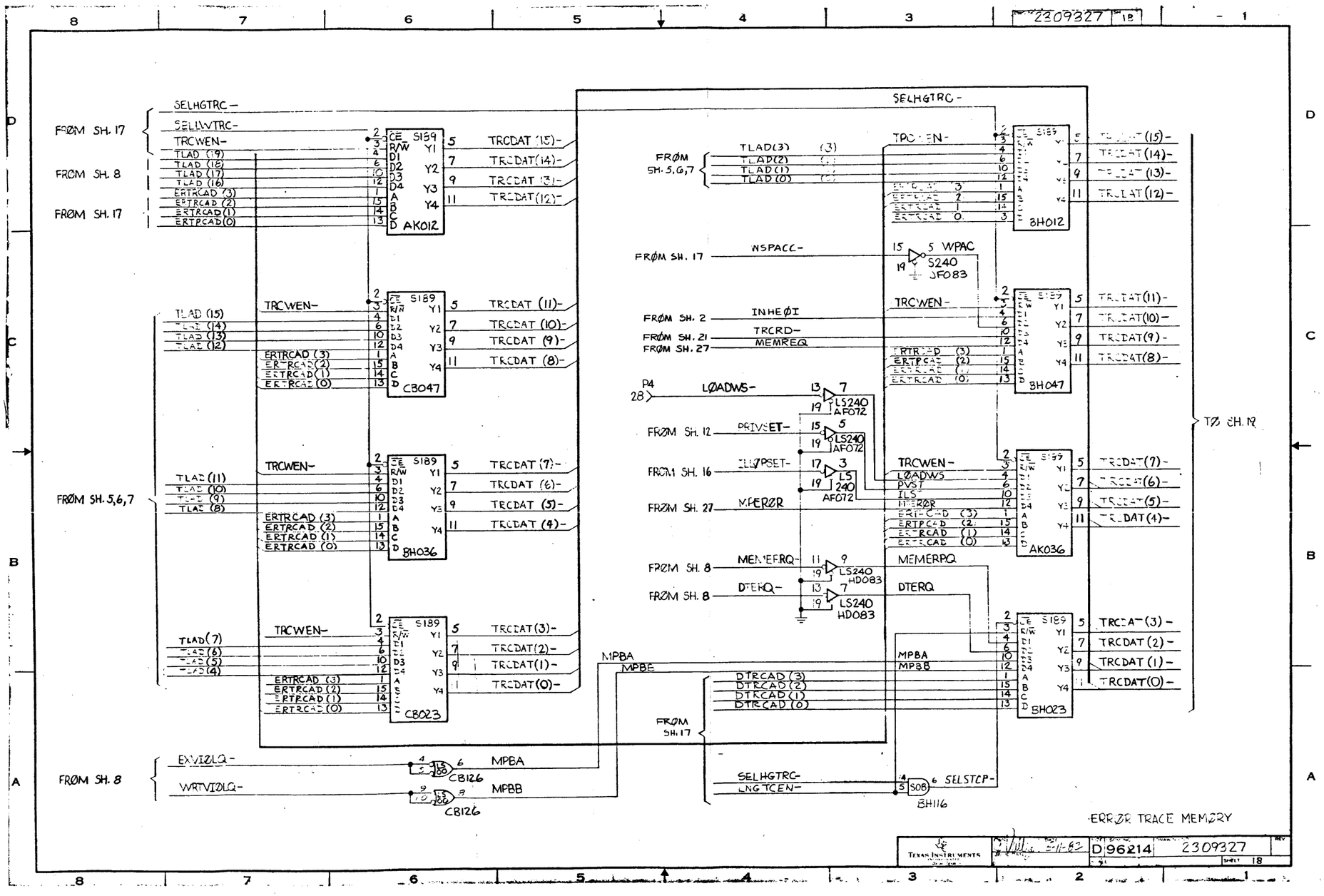

DWG NO 2309327 SH 13
P3
31
ST8
LS240 HD012
ST8A-
ST8A
TØ SH. 15
ST8A-
TØ SH. 30
FRØM SH. 9
ABUSB(0)
ABUSB(1)
ABUSB(2)
ABUSB(3)
ABUSB(4)
MAPFLE(0)-
FRØM SH. 27
DD012
TPCAD-
TPCAD-
TØ SH. 4, 8
S04 BH058
TPCAD
TPCAD
TØ SH. 5
FRØM SH. 9
ABUSB(5)
PRØMDB
PRØMDB
TØ SH. 8
CB003
FRØM SH. 3
BSLCHCK
BSLCHCK
SETI-
TØ SH. 27
FRØM SH. 1
TWØN
TWØN
FRØM SH. 10
CARYA(3)
CARYA(3)-
SETI-
SELBSA-
TØ SH. 5, 22
S04 BH058
EF060
S74 CB058
FRØM SH. 11
CARYB(3)
CYB
SETZ-
SELBSB-
TØ SH. 6, 22
EF060
CK003
S74 EK060
SELBSB
TØ SH. 32
TWØN
CYC
EF060
CARYA(3)
SET3-
SELBSC-
TØ SH. 7, 22
CK03B
S74 EK060
SELBSC
TØ SH. 32
TWØN
FRØM SH. 15
MAPENB
MAPENB
MAPENC
EK091
BASE SELECTIØN LØGIC
TEXAS INSTRUMENTS
DWN
DATE 5-12-83
ISSUE DATE
SIZE D
FSCM NO 96214
DRAWING NO 2309327
REV
SCALE
SHEET 13

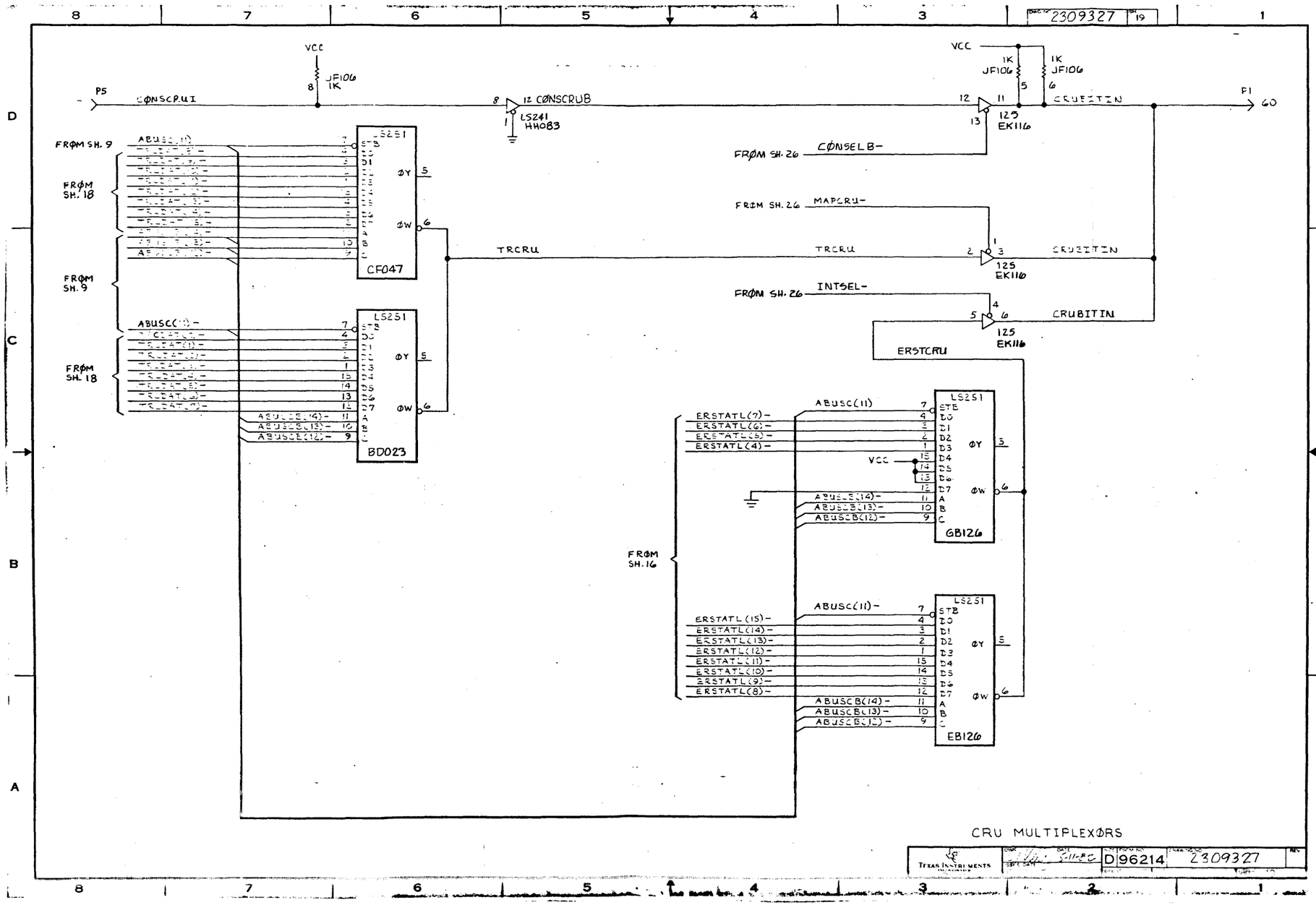

2309327 14
FROM SH. 2
ABUSB(0) THRU ABUSB(14)
FROM SH. 9
ABUSC(11)-
ABUSC(10)-
ABUSC(9)-
CRCK
FROM SH. 3
CRUEN-
FROM SH. 26
CLKRB
FROM SH. 3
CF1116
MPCRUCKB-
BRKCKB-
BRKCKA-
FPSELB-
TO SH. 23
INTCLRA-
INTCLRB-
TO SH. 16
MPCRUCKA-
TO SH. 15,17
PRIVBKPT
TO SH. 15
FROM SH. 9
ABUSCB(14)-
ABUSCB(13)-
ABUSCB(12)-
CPIE
FROM SH. 23
TLRESB-
FROM SH. 23
LS259
HD126
MPCRUCKB-
EPROMADR(0)
EPROMADR(1)
EPROMADR(2)
TO SH. 20
DPRTYERR
TO SH. 10
DITEN
TO SH. 24
FROM SH. 15
BRKCLR-
LK058
BRKRG(0)
BRKRG(1)
BRKRG(2)
BRKRG(3)
BRKRG(4)
BRKRG(5)
BRKRG(6)
BRKRG(7)
TO SH. 24
DH058
BRKRG(8)
BRKRG(9)
BRKRG(10)
BRKRG(11)
BRKRG(12)
BRKRG(13)
BRKRG(14)
BRKRG(15)
LS85
DD058
DD047
DD036
DD023
A>B
A=B
A<B
CPEGA
CPEGB
CPEGC
CPEGD
VCC
TO SH.15
TEXAS INSTRUMENTS
D96214
2309327
SHEET 14

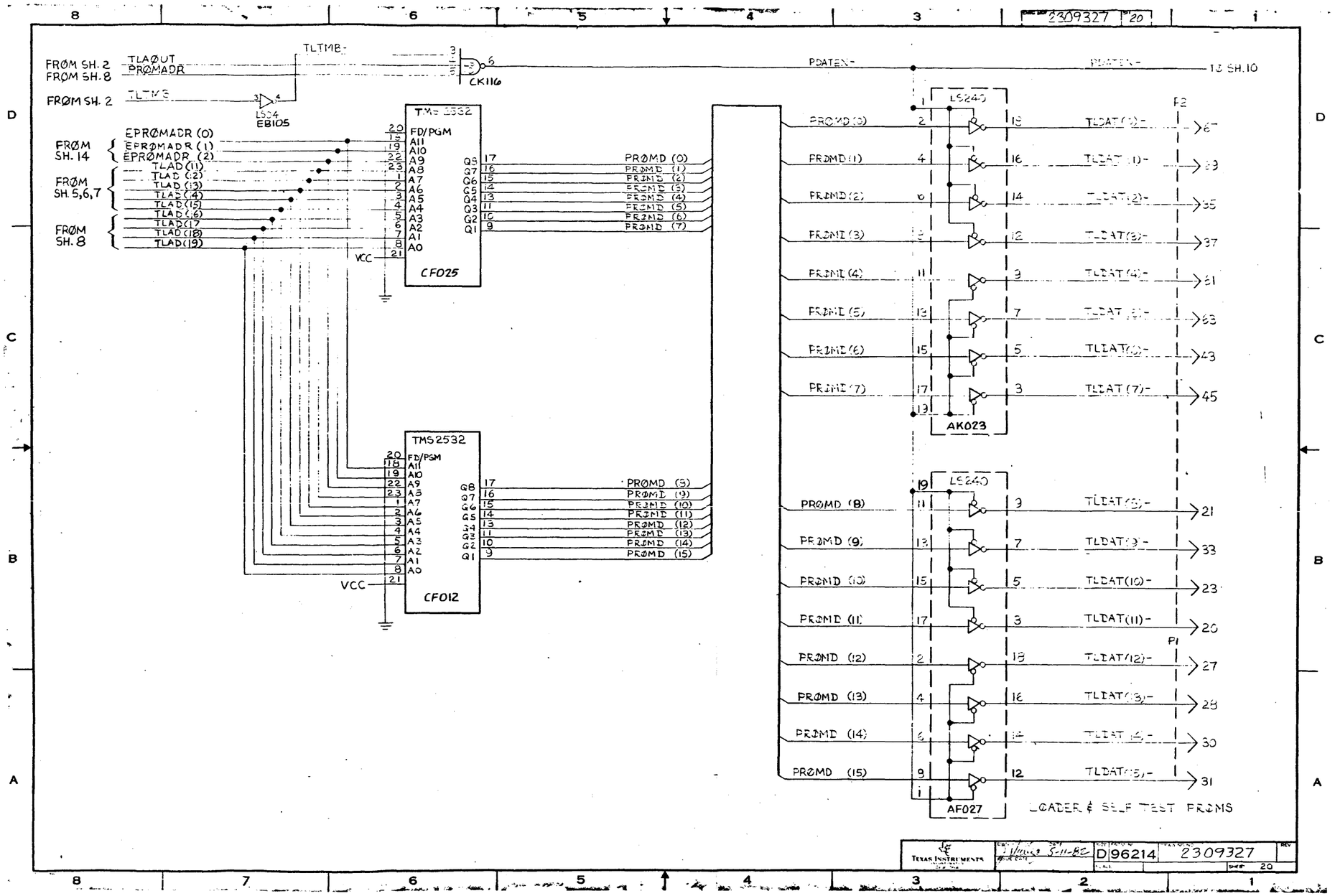

FRØM SH. 2
TLAOUT
FRØM SH. 9
ABUSCB(14)-
ABUSCB(13)-
ABUSCB(12)-
FRØM SH. 23
FRØM SH. 14
LS259
FD116
BKSL(7)
BKSL(6)
MAPENB
CACHEN-
TSTCKEN
JF106
CB105
MAPENB
TØ SH. 4,13,21,27
CACHEN-
S240
JF083
TLCACHEN
P1
73
TØ SH. 17
+5V
FRØM SH. 33
INSTRX-
LDPRØMTIR
LS04
GB105
BKSL(6)
FD126
BKSL(7)
ADBREAK-
TØ SH. 16,33
EK126
FRØM SH. 32
RDQ
RAR
LS86
EK003
MAPF
CLBK
FRØM SH. 27
MEMREQ
MEMINH
FROM SH. 4
INHT-
FRØM SH. 8
ADBK
EB081
EF116
AKAEL
LDMAP-
CLRBKPT
CK116
FRØM SH. 16
ERSTATL(6)-
BRKCLR-
TØ SH. 14
DH116
FRØM SH. 23
TLIØRESB-
FRØM SH. 13
ST8A
BKEN-
BKENA
GF083
FRØM SH. 14
CPEQA
CPEQ B
CPEQ C
CPEQ D
MAPFLE(0)-
STBK-
DD091
BKD
TØ SH. 8
CB126
TERM
P4
MAPREQ
HH072
TØ SH. 3,29
FRØM SH. 14
FRØM SH. 12
PRIVBKPT
ST7B-
PRVBKEN
BREAKPØINT QUALIFIER
D 96214
2309327
SHEET 15

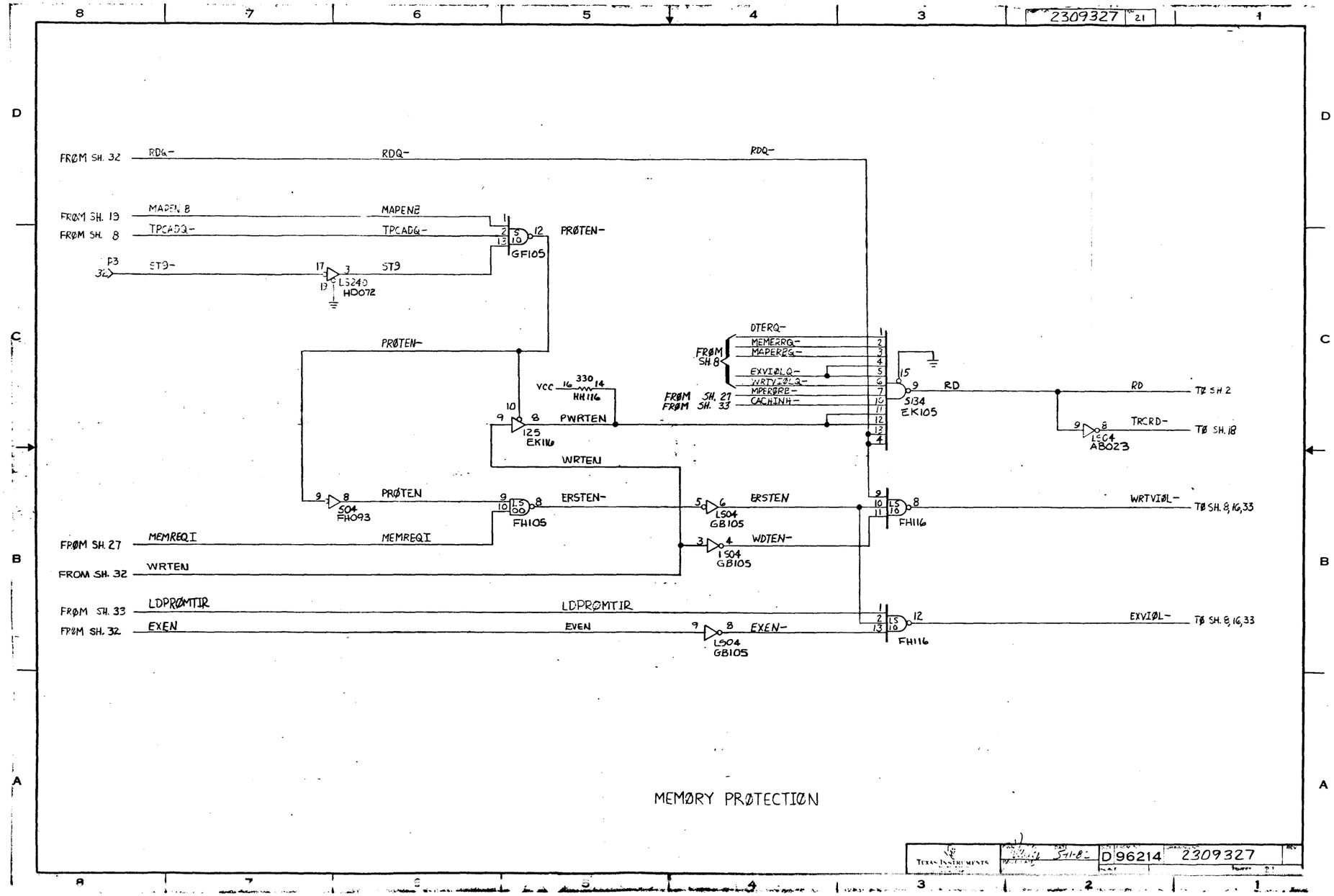

2309327
P4
C.FLINT–
TØ SH.33
STACKØV–
FROM SH. 9
FROM SH. 23
FROM SH. 14
LS259
HH105
CSTK
CLBKINT
CCKINT
C0VINT
CCKINT
TØ SH, 17
FROM SH.17
MAPERCL
MAPERCL
CTE
CPV
CLØP
CPRES
CEXVL
CWVIØL
DD127
FROM SH. 1
FROM SH, 14
WØN
CLMPER
6 CLRMAPER
LS32
CK091
CLMEMER
5 6 CLMEMER–
LS04
FD126
FROM SH, 23
CLMER–
CLMER–
4 5 6 CRMER
LS 00
GF083
INTCLRB–
CRØUTB–
12 13 11 CERS–
LS 32
CK091
Vcc
37 P3 ILLØPST–
19 13 7
LS241
HH083
ILLØPSET–
ILLØPSET–
TØ SH, 15
FROM SH, 23 TLIØRESB–
FROM SH, 3 CLKMT–
FROM SH, 17 CLKINT–
FROM SH, 15 ADBREAK–
C0VINT
C0VFLINT–
CCKINT
CLBKINT
CSTK
STACKØV–
P 276
HH094
ERSTATL (4)–
ERSTATL(5)–
ERSTATL(6)–
ERSTATL(7)–
TØ SH. 15
FROM SH, 3 CLKRM–
FROM SH, 21 WRTVIØL–
FROM SH, 21 EXVIØL–
FROM SH. 1 WØN
FROM SH, 27 MAPERB–
CWVIØL
CEXVL
CPRES
CLRMAPER
DH126
ERSTATL(8)–
ERSTATL(9)–
ERSTATL(10)–
ERSTATL(11)–
TØ SH. 19, 33
FROM SH, 10 MEMERR–
CILØP
CPV
CTE
CRMER
CK126
ERSTATL(12)–
ERSTATL(13)–
ERSTATL(14)–
ERSTATL(15)–
TØ SH. 2
FROM SH12 PRIVSET.–
FROM SH, 2 ADTERB–
CERS–
ERRØR STATUS REGISTER
TEXAS INSTRUMENTS
D 96214
2309327
SHEET 16

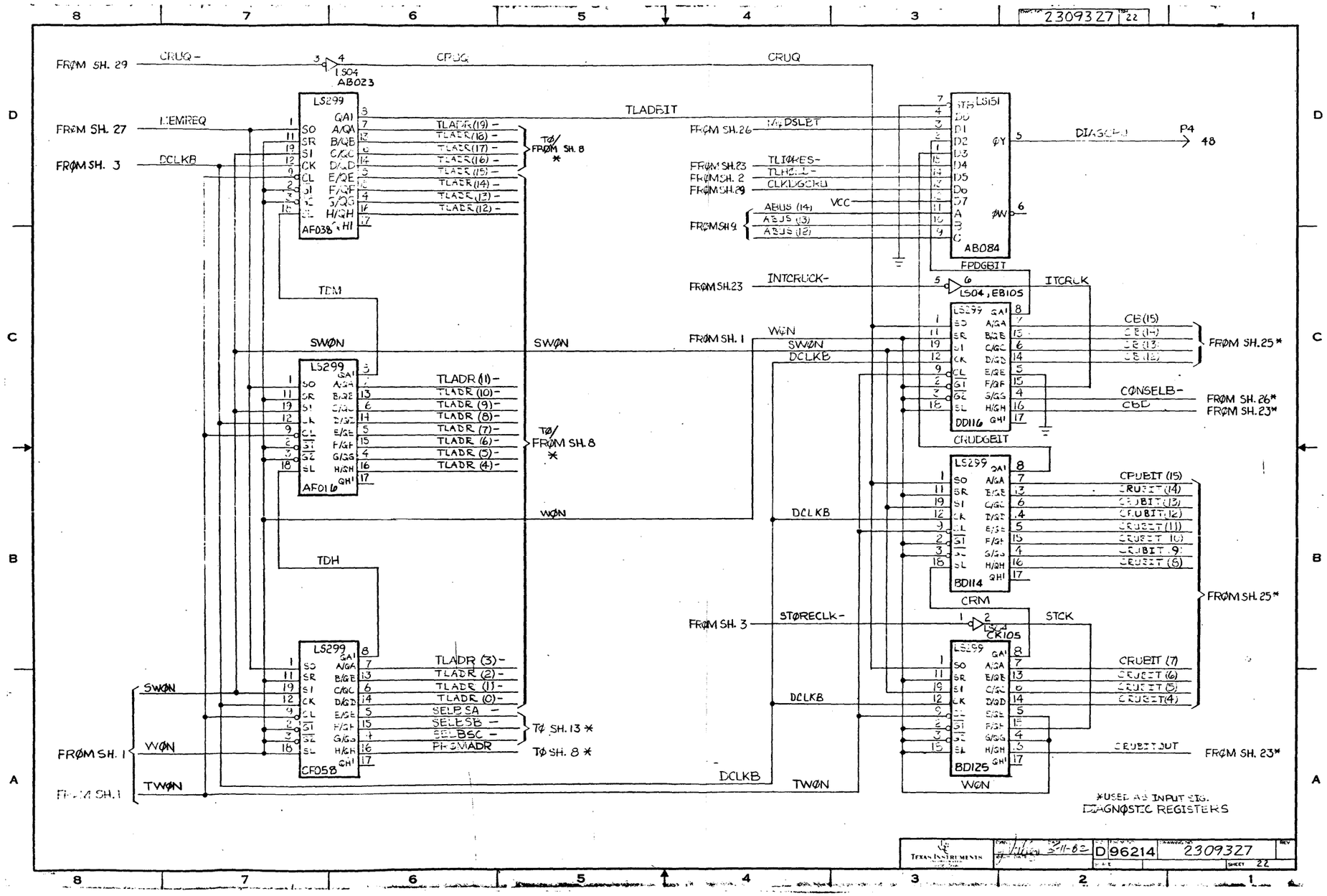

2309327
FRØM SH. 15
TSTCKEN
TSTCKEN
HJ132
68K
VCC
THRESHLD
HJ131
162K
GFIZ6
NE555
TSTCLK
HJ127
.047
RST555
HJ129
0.047
FRØM SH. 1
TWØN
TWØN
TSTCKEN
TSTCLK
LS112
GK1Z6
CLKINT-
TØ SH. 16
FRØM SH. 16
CCKINT
CCKINT-
LS04
EB105
CLR TSTCK-
EF116
FRØM SH. 9
FRØM SH. 1
FRØM SH. 14
ABUSCB (14)-
ABUSCB (12)-
ABUS 3 (12)-
WØN
MPCRUCKA-
LS138
AB036
MAPERCL-
LS04
AB023
MAPERCL
MAPERCL
TØ SH. 16
INCTRC-
INCTRC
LS04
AB023
SELHGTRC
SELHGTRC-
TØ SH. 18
S240
DH072
SELLWTRC
SELLWTRC-
TØ SH. 18
FRØM SH. 3
CLKLM-
CLKLM
CLKLM-
CLKLM
S112
DD003
SETEND-
SETEND-
MNTRCEND
TØ SH. 24
LS04
AB023
SELHGTRC
¼ LS279
EB003
TRCWEN-
LNGTCEN-
¼LS279
EB003
STØPTRC-
LS669
ENTRCWRT
ERTRCAD (3)
ERTRCAD (2)
ERTRCAD (1)
ERTRCAD (0)
FRØM SH. 33
LV2 SET-
LV2SET
S04
BH058
LS02
CB003
WDCRYEN-
LS02
DH003
TRCNTEN-
LS02
DH003
BH003
FRØM SH. 3
MEMREQ-
VCC
P4
29
WRTRCMEM-
LS241
HH083
WRTRC-
FH083
TRCW
TØ SH. 18
P4
33
WSPACC-
LS241
HH083
WPAC-
TRCWENB-
LS08
CB003
LS175
CF003
ERTRCAD (0)
ERTRCAD (3)
ERTRCAD (1)
ERTRCAD (2)
DTRCAD (0)
DTRCAD (3)
DTRCAD (1)
DTRCAD (2)
TØ SH. 18
CLKLM-
TWØN
TWØN
LS74
CF105
LSTCPEN-
NC
LSTCPEN
LS08
CB126
LNGTCEN-
TRCWEN-
FRØM SH. 3
FRØM SH. 24
CLKRM-
MNTRCWEN
CLKRM-
TRCWEN-
FRØM SH. 29
FRØM SH. 3
DCLK20B-
DCLK-
LS20
CF03B
FRØM SH. 3
DCLKC
DCLKC
5-10-82
D96214
2309327

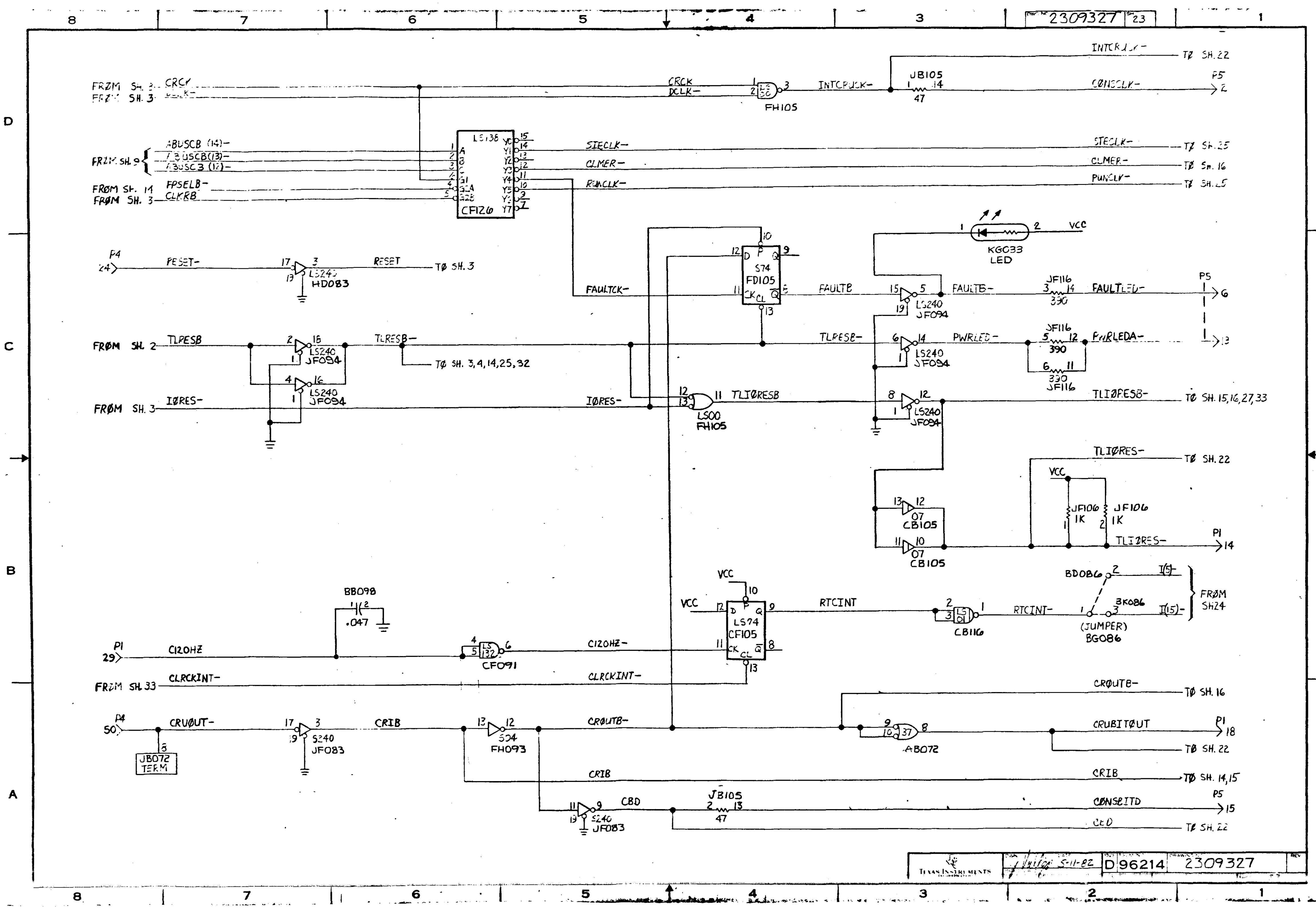

2309327 18
SELHGTRC-
SELLWTRC-
TRCWEN-
FRØM SH. 17
FRØM SH. 8
FRØM SH. 17
TLAD (19)
TLAD (18)
TLAD (17)
TLAD (16)
ERTRCAD (3)
ERTRCAD (2)
ERTRCAD (1)
ERTRCAD (0)
S189
AK012
TRCDAT (15)-
TRCDAT (14)-
TRCDAT (13)-
TRCDAT (12)-
TLAD (15)
TLAD (14)
TLAD (13)
TLAD (12)
CB047
TRCDAT (11)-
TRCDAT (10)-
TRCDAT (9)-
TRCDAT (8)-
TLAD (11)
TLAD (10)
TLAD (9)
TLAD (8)
FRØM SH. 5,6,7
BH036
TRCDAT (7)-
TRCDAT (6)-
TRCDAT (5)-
TRCDAT (4)-
TLAD (7)
TLAD (6)
TLAD (5)
TLAD (4)
CB023
TRCDAT (3)-
TRCDAT (2)-
TRCDAT (1)-
TRCDAT (0)-
FRØM SH. 8
EXVIDLQ-
WRTVIDLQ-
CB126
MPBA
MPBB
FRØM SH. 5,6,7
TLAD(3)
TLAD(2)
TLAD(1)
TLAD(0)
BH012
FRØM SH. 17
NSPACC-
S240
JF083
WPAC
FRØM SH. 2
INHEØI
FRØM SH. 21
FRØM SH. 27
TRCRD-
MEMREQ
BH047
P4
28
LØADWS-
LS240
AF072
FRØM SH. 12
DRIVSET-
FRØM SH. 16
ILLWPSET-
FRØM SH. 27
MPERØR
FRØM SH. 8
MEMERRQ-
LS240
HD083
FRØM SH. 8
DTERQ-
MEMERRQ
DTERQ
AK036
MPBA
MPBB
DTRCAD (3)
DTRCAD (2)
DTRCAD (1)
DTRCAD (0)
FRØM SH. 17
BH023
SELHGTRC-
LNGTCEN-
S08
SELSTCP-
BH116
TØ SH. 19
ERRØR TRACE MEMØRY
TEXAS INSTRUMENTS
D 96214
2309327
SHEET 18

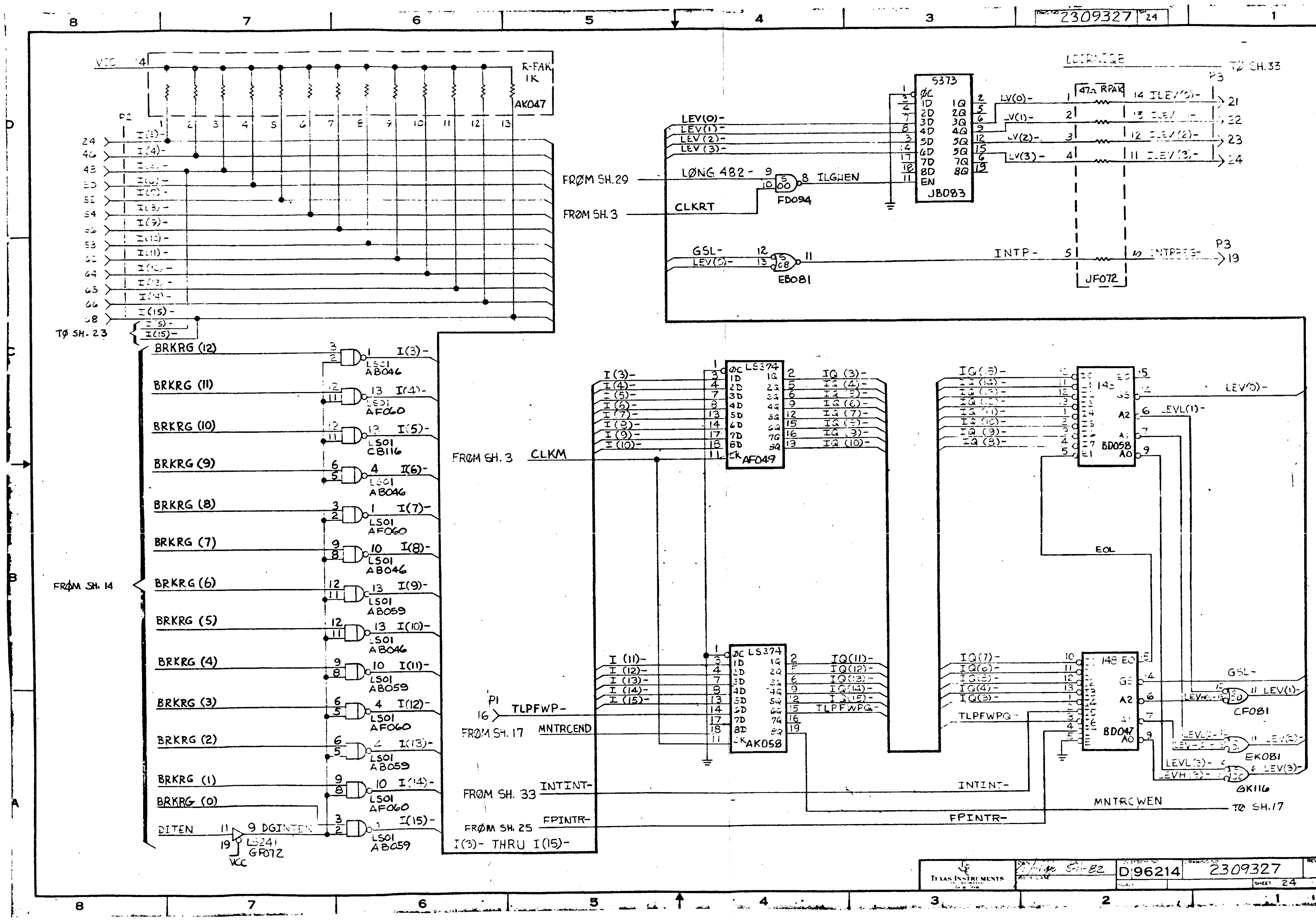

2309327
VCC
1K JF106
P5
CONSCRUI
12 CONSCRUB
LS241 HH083
P1 60
FROM SH. 9
FROM SH. 18
FROM SH. 9
FROM SH. 18
LS251
CF047
BD023
TRCRU
FROM SH. 26 CONSELB-
FROM SH. 26 MAPCRU-
FROM SH. 26 INTSEL-
125 EK116
CRUBITIN
ERSTCRU
ABUSC(11)
ERSTATL(7)-
ERSTATL(6)-
ERSTATL(5)-
ERSTATL(4)-
GB126
FROM SH. 16
ERSTATL(15)-
ERSTATL(14)-
ERSTATL(13)-
ERSTATL(12)-
ERSTATL(11)-
ERSTATL(10)-
ERSTATL(9)-
ERSTATL(8)-
EB126
CRU MULTIPLEXORS
TEXAS INSTRUMENTS
D 96214
2309327

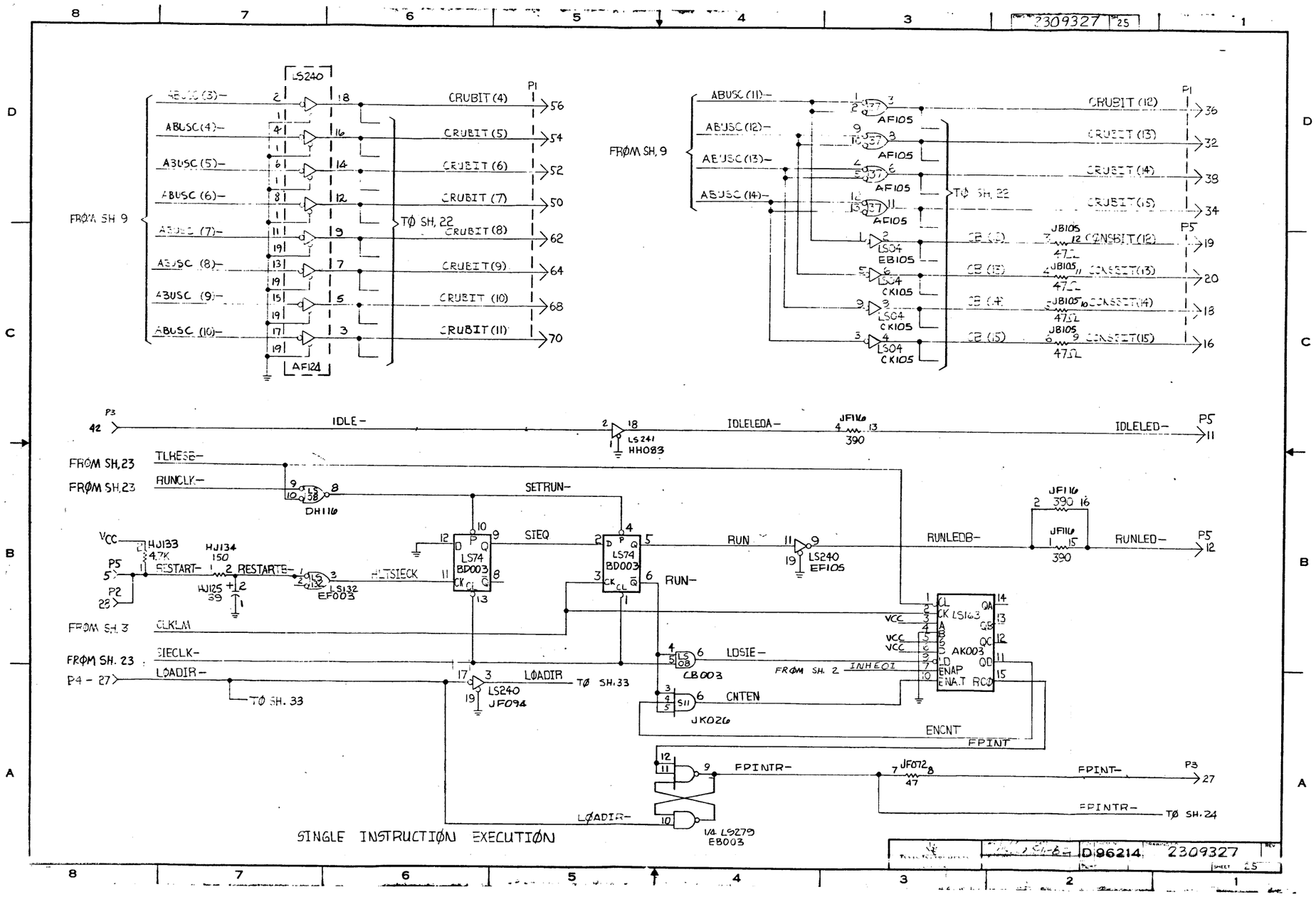

2309327
20
FROM SH. 2 TLAOUT
FROM SH. 8 PROMADR
TLTIMB-
CK116
FROM SH. 2 TLTIMS
LS04
EB105
PDATEN-
TO SH.10
EPROMADR (0)
FROM SH. 14 EPROMADR (1)
EPROMADR (2)
FROM SH. 5,6,7 TLAD(11)
TLAD(12)
TLAD(13)
TLAD(14)
TLAD(15)
TLAD(16)
FROM SH. 8 TLAD(17)
TLAD(18)
TLAD(19)
TMS2532
FD/PGM
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
VCC
CF025
PROMD (0)
PROMD (1)
PROMD (2)
PROMD (3)
PROMD (4)
PROMD (5)
PROMD (6)
PROMD (7)
TMS2532
CF012
PROMD (8)
PROMD (9)
PROMD (10)
PROMD (11)
PROMD (12)
PROMD (13)
PROMD (14)
PROMD (15)
LS245
AK023
AF027
P2
P1
TLDAT(0)-
TLDAT(1)-
TLDAT(2)-
TLDAT(3)-
TLDAT(4)-
TLDAT(5)-
TLDAT(6)-
TLDAT(7)-
TLDAT(8)-
TLDAT(9)-
TLDAT(10)-
TLDAT(11)-
TLDAT(12)-
TLDAT(13)-
TLDAT(14)-
TLDAT(15)-
LOADER & SELF TEST PROMS
TEXAS INSTRUMENTS
D 96214
2309327
SHEET 20

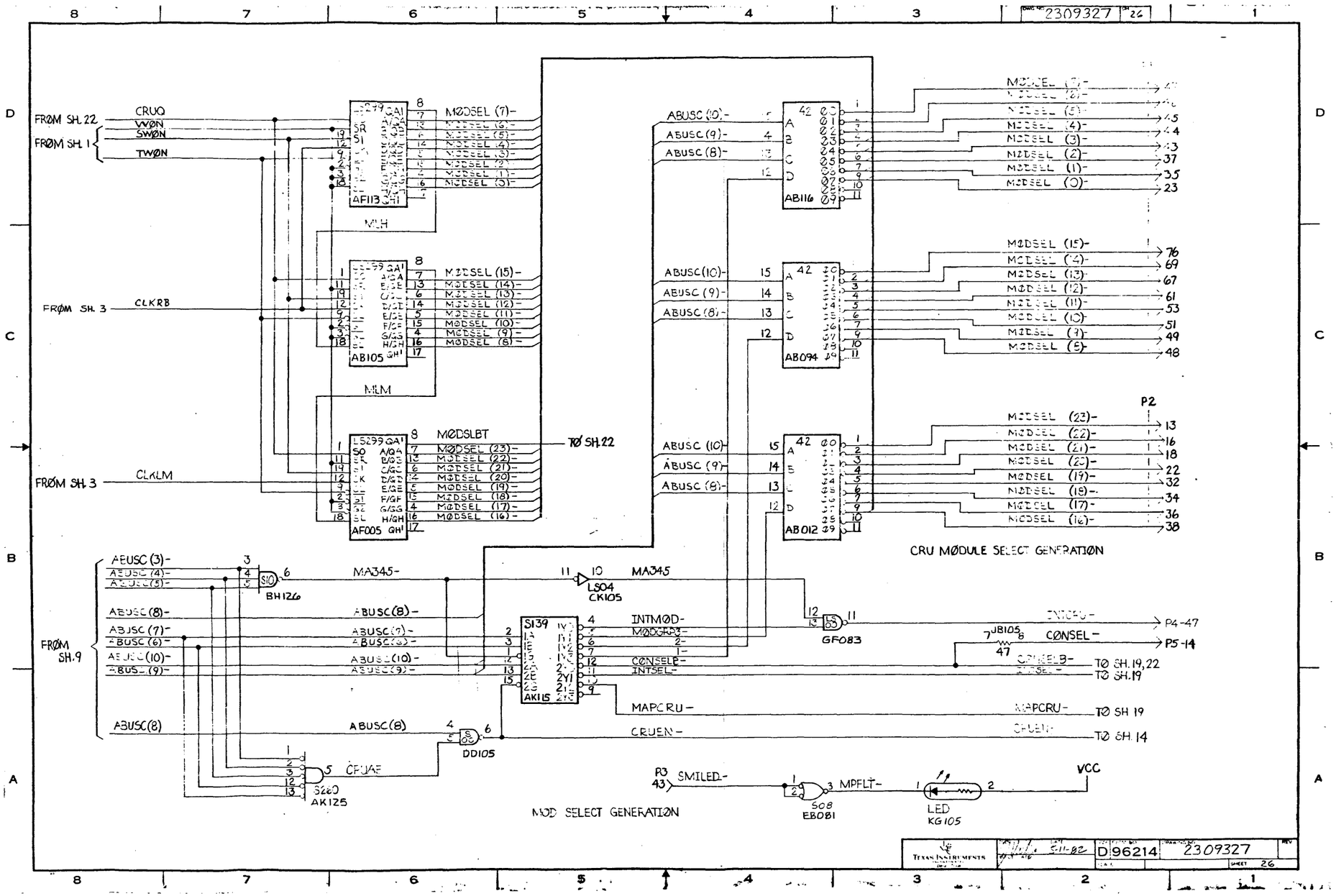

2309327
FRØM SH. 32
RDQ-
RDQ-
RDQ-
FRØM SH. 19
MAPEN. B
MAPENB
FRØM SH. 8
TPCADQ-
TPCADQ-
PRØTEN-
GF105
P3
32
ST9-
17
19
LS240
HD072
ST9
PRØTEN-
DTERQ-
MEMERRQ-
MAPERRQ-
FRØM SH. 8
EXVIØLQ-
WRTVIØLQ-
MPERØRE-
FRØM SH. 27
FRØM SH. 33
CACHINH-
S134
EK105
RD
RD
TØ SH. 2
VCC
330
RN116
PWRTEN
125
EK116
TRCRD-
LS04
AB023
TØ SH. 18
WRTEN
PRØTEN
504
FH093
ERSTEN-
FH105
ERSTEN
LS04
GB105
WRTVIØL-
FH116
TØ SH. 8, 16, 33
FRØM SH. 27
MEMREQI
MEMREQI
WDTEN-
LS04
GB105
FROM SH. 32
WRTEN
FRØM SH. 33
LDPRØMTIR
LDPRØMTIR
FRØM SH. 32
EXEN
EVEN
EXEN-
LS04
GB105
EXVIØL-
FH116
TØ SH. 8, 16, 33
MEMØRY PRØTECTIØN
TEXAS INSTRUMENTS
D96214
2309327

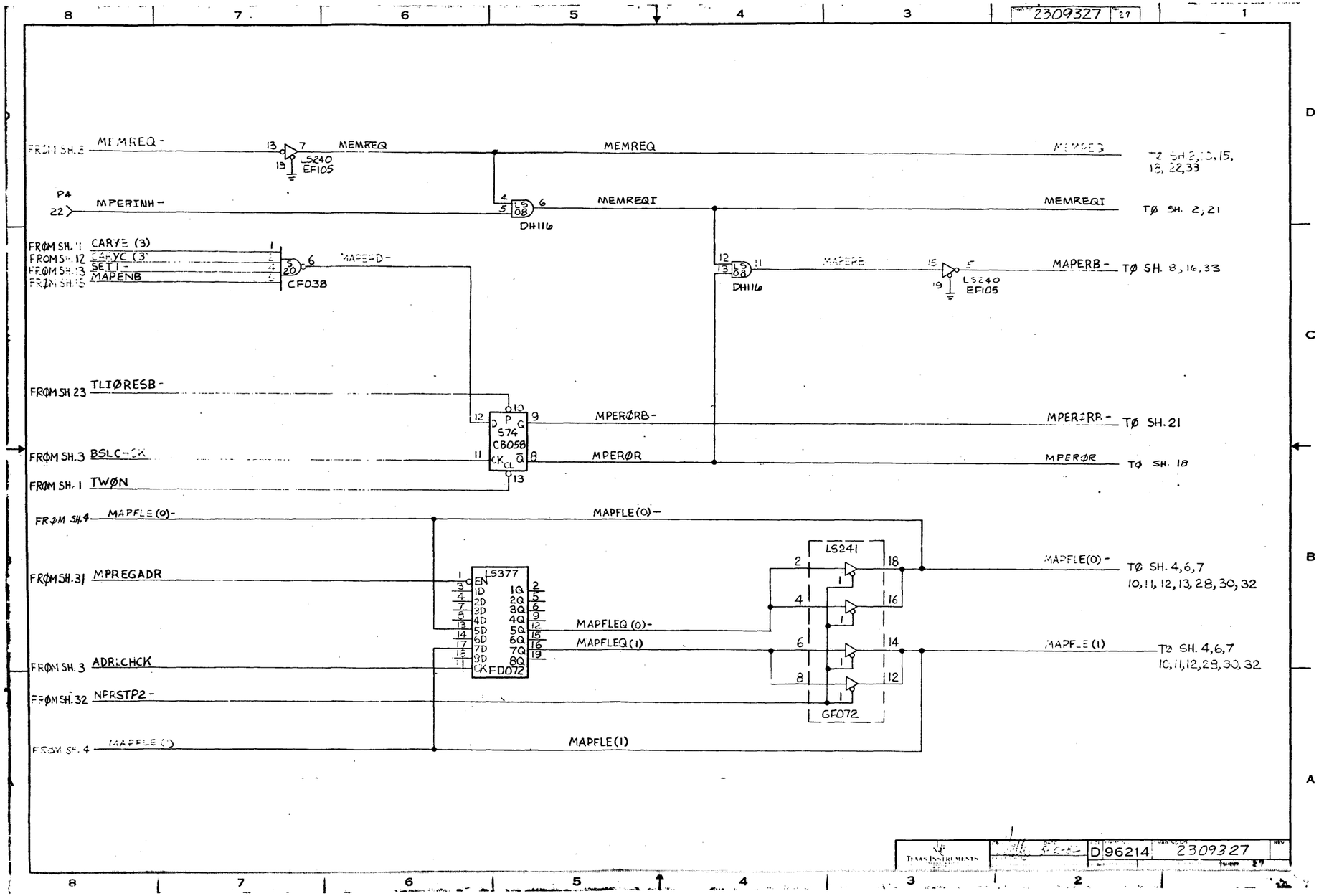

2309327 22
FROM SH. 29
CRUQ-
LS04 AB023
CRUQ
CRUQ
LS299
TLADBIT
FROM SH. 27
MEMREQ
FROM SH. 3
DCLKB
TLADR(19)-
TLADR(18)-
TLADR(17)-
TLADR(16)-
TLADR(15)-
TLADR(14)-
TLADR(13)-
TLADR(12)-
AF038
TØ FROM SH. 8 *
FROM SH.26
MA DSLBT
FROM SH.23
TLIOWES-
FROM SH. 2
CLKDGCKD
FROM SH.29
VCC
FROM SH 9
ABUS (14)
ABUS (13)
ABUS (12)
LS151
AB084
DIAGCPU
P4 48
FPDGBIT
FROM SH.23
INTCRUCK-
LS04, EB105
ITCRCK
TDM
SWØN
FROM SH. 1
WØN
SWØN
DCLKB
TLADR (11)-
TLADR (10)-
TLADR (9)-
TLADR (8)-
TLADR (7)-
TLADR (6)-
TLADR (5)-
TLADR (4)-
AF016
TØ FROM SH. 8 *
CE(15)
CE(14)
CE(13)
CE(12)
FROM SH. 25 *
CONSELB-
CRU
FROM SH. 26*
FROM SH. 23*
DD116
CRUDGBIT
WØN
DCLKB
CPUBIT (15)
CRUBIT (14)
CRUBIT (13)
CRUBIT (12)
CRUBIT (11)
CRUBIT (10)
CRUBIT (9)
CRUBIT (8)
BD114
FROM SH. 25*
TDH
CRM
FROM SH. 3
STØRECLK-
LS04 CR105
STCK
SWØN
FROM SH. 1
WØN
TWØN
SELPSA-
SELBSB-
SELBSC-
PERIPHADR
TØ SH. 13 *
TØ SH. 8 *
CF058
CRUBIT (7)
CRUBIT (6)
CRUBIT (5)
CRUBIT (4)
CRUBITOUT
FROM SH. 23*
BD125
DCLKB
TWØN
*USED AS INPUTS.
DIAGNOSTIC REGISTERS
TEXAS INSTRUMENTS
D 96214
2309327
SHEET 22

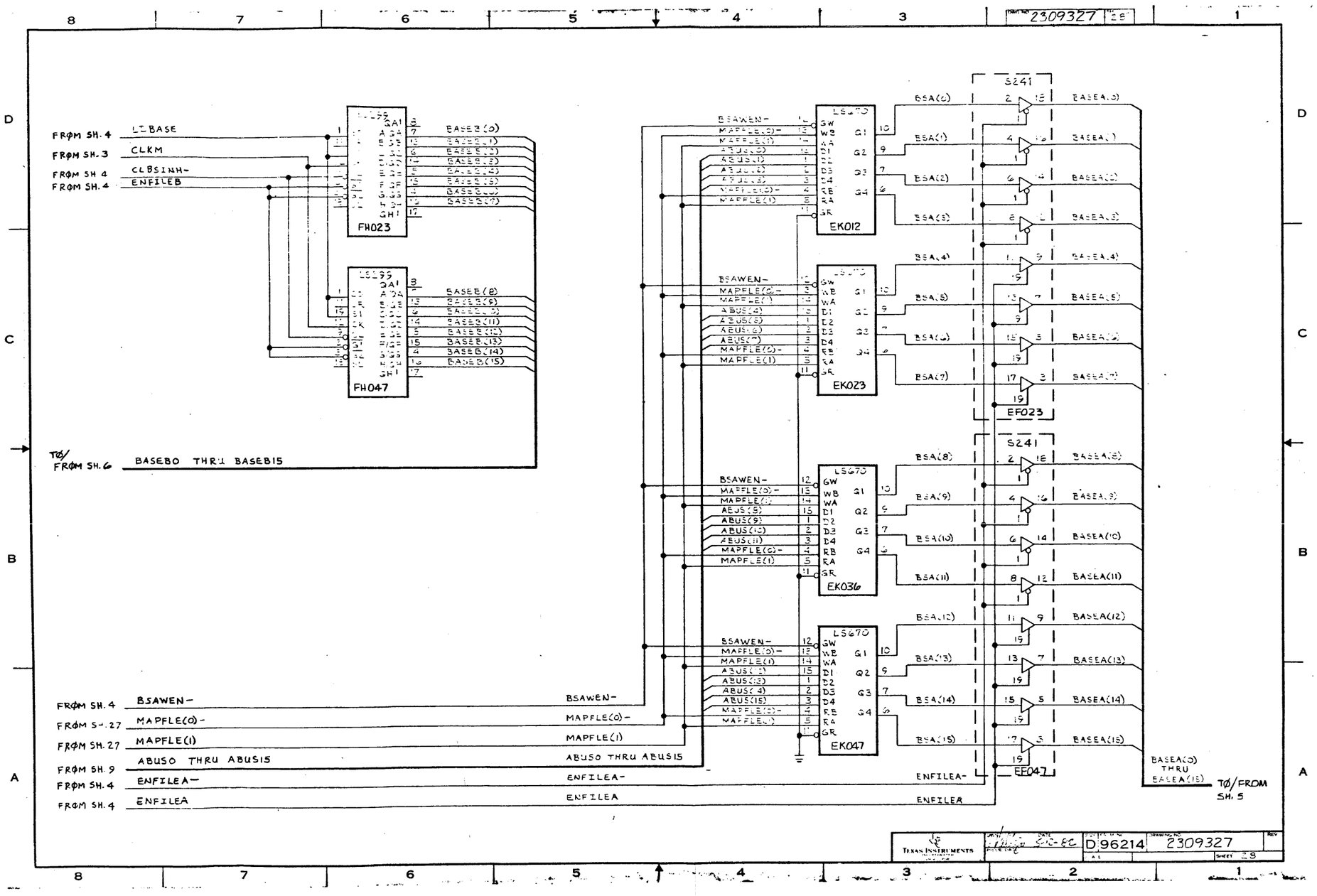

2309327
FRØM SH. 3 CRCK
FRØM SH. 9
ABUSCB (14)-
ABUSCB (13)-
ABUSCB (12)-
FRØM SH. 14 FPSELB-
FRØM SH. 3 CLKRB
LS138
CF126
CRCK
DCLK-
LS00
FH105
INTCPUCK-
JB105
47
INTCPUCK-
TØ SH. 22
CØNSCLK-
P5
STECLK-
TØ SH. 25
CLMER-
TØ SH. 16
PUNCLK-
TØ SH. 25
RUNCLK-
KG033
LED
VCC
P4
RESET-
RESET
TØ SH. 3
LS240
HD083
S74
FD105
FAULTCK-
FAULTB
FAULTB-
LS240
JF094
JF116
330
FAULTLED-
P5
FRØM SH. 2
TLRESB
TLRESB-
TØ SH. 3,4,14,25,32
TLRESB-
PWRLED-
390
PWRLEDA-
JF116
FRØM SH. 3
IØRES-
IØRES-
LS00
FH105
TLIØRESB
TLIØRESB-
TØ SH. 15,16,27,33
TLIØRES-
TØ SH. 22
VCC
JF106
1K
TLIØRES-
P1
07
CB105
BD086
FRØM SH24
BB098
.047
VCC
VCC
LS74
CF105
RTCINT
RTCINT-
CB116
(JUMPER)
BG086
BK086
P1
CI2OHZ
CF091
CI2OHZ-
FRØM SH 33
CLRCKINT-
CLRCKINT-
CRØUTB-
TØ SH. 16
P4
CRUØUT-
JB072
TERM
S240
JF083
CRIB
S04
FH093
CRØUTB-
AB072
CRUBITØUT
P1
TØ SH. 22
CRIB
CRIB
TØ SH. 14,15
S240
JF083
CBD
JB105
47
CØNSBITD
P5
CBD
TØ SH. 22
TEXAS INSTRUMENTS
5-11-82
D 96214
2309327

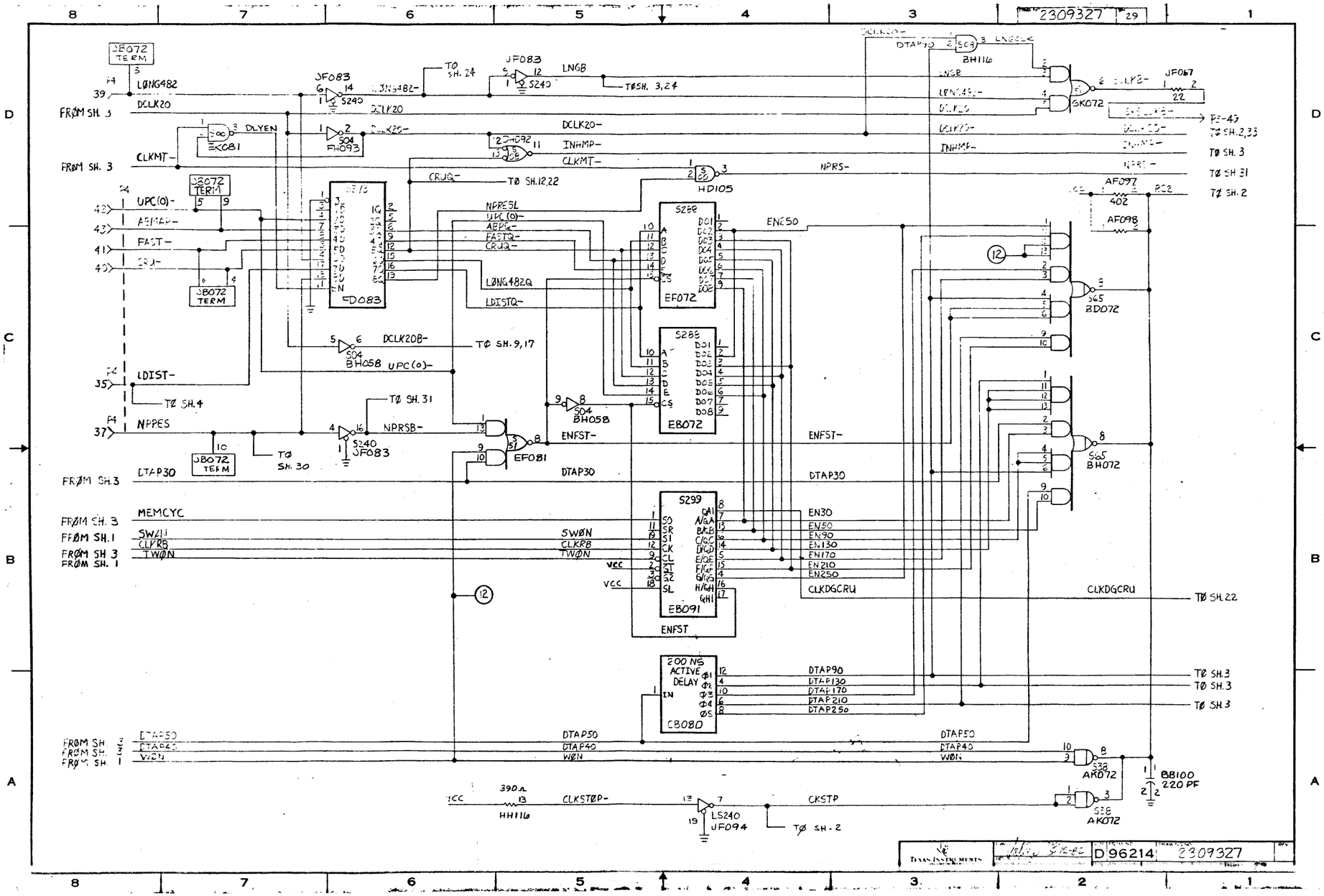

2309327
D 96214
2309327
SHEET 24
TEXAS INSTRUMENTS
BRKRG (12)
BRKRG (0)
DITEN
FROM SH. 14
TO SH. 23
FROM SH. 3 CLKM
FROM SH. 17 MNTRCEND
FROM SH. 33 INTINT-
FROM SH. 25 FPINTR-
I(3)- THRU I(15)-
FROM SH.29 LONG 482-
FROM SH. 3 CLKRT
TO SH.33
TO SH.17
MNTRCWEN
FPINTR-
INTINT-
GSL-
INTP-
EOL
LS374
AF049
AK058
JB083
FD094
EB081
JF072
BD058
BD047
CF081
EK081
GK116
LS241
GF072
AK047
R-PAK 1K

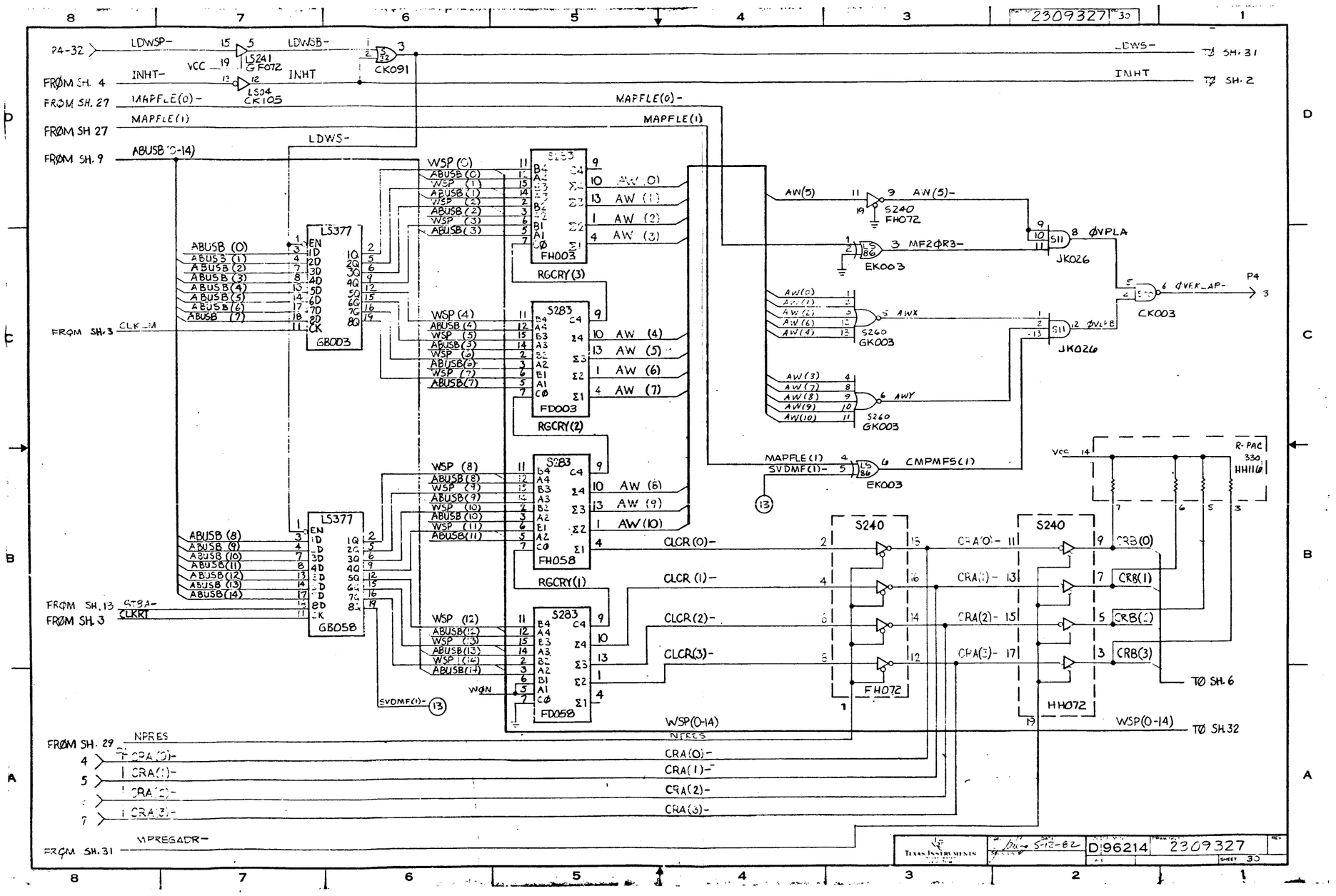

8
7
6
5
4
3
2
1
2309327
25
D
C
B
A
LS240
AF124
ABUSC (3)–
ABUSC(4)–
ABUSC(5)–
ABUSC (6)–
ABUSC (7)–
ABUSC (8)–
ABUSC (9)–
ABUSC (10)–
FRØM SH 9
TØ SH, 22
CRUBIT (4)
CRUBIT (5)
CRUBIT (6)
CRUBIT (7)
CRUBIT (8)
CRUBIT(9)
CRUBIT (10)
CRUBIT (11)
P1
56
54
52
50
62
64
68
70
ABUSC (11)–
ABUSC (12)–
ABUSC (13)–
ABUSC (14)–
FRØM SH, 9
AF105
EB105
CK105
LS04
CRUBIT (12)
CRUBIT (13)
CRUBIT (14)
CRUBIT (15)
CB (12)
CB (13)
CB (14)
CB (15)
JB105
47Ω
CONSBIT(12)
CONSBIT(13)
CONSBIT(14)
CONSBIT(15)
P5
36
32
38
34
19
20
18
16
P3
42
IDLE–
LS241
HH083
IDLELEDA–
JF116
390
IDLELED–
FROM SH,23
TLHESB–
RUNCLK–
LS
08
DH116
SETRUN–
VCC
HJ133
4.7K
HJ134
150
P5
5
RESTART–
RESTARTB–
P2
28
HJ125
39
LS132
EF003
HLTSIECK
LS74
BD003
SIEQ
RUN
RUN–
LS240
EF105
RUNLEDB–
RUNLED–
P5
12
FROM SH.3
CLKLM
FROM SH. 23
SIECLK–
P4 – 27
LOADIR–
TØ SH. 33
LOADIR
LS240
JF094
LDSIE–
CB003
FROM SH. 2
INHEQI
CNTEN
JK026
ENCNT
FPINT
LS163
AK003
ENAP
ENA.T
RCO
FPINTR–
JF072
47
FPINT–
P3
27
FPINTR–
TØ SH.24
LOADIR–
1/4 LS279
EB003
SINGLE INSTRUCTIØN EXECUTIØN
D96214
2309327
SHEET 25

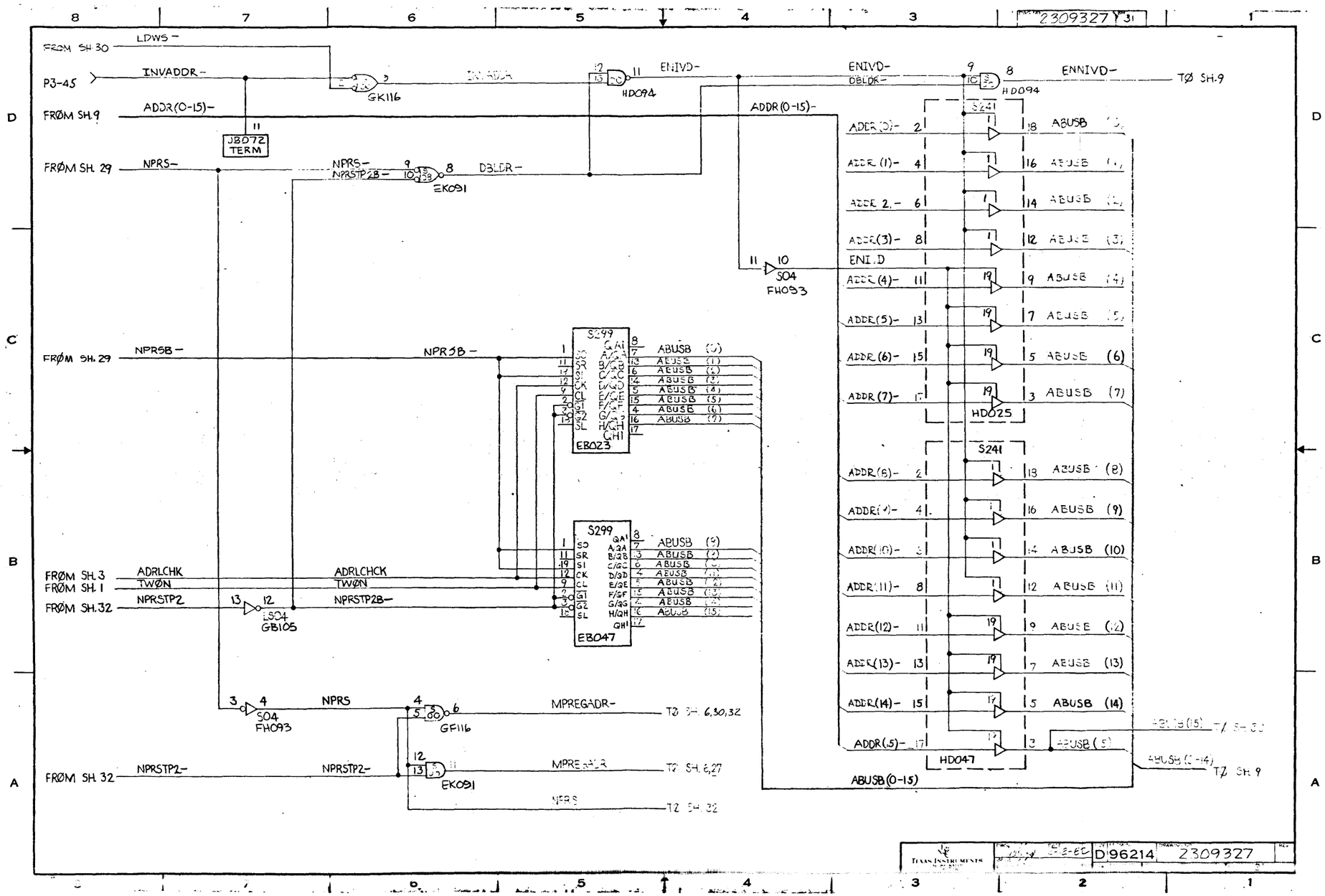

2309327
FROM SH. 22
CRUQ
WQN
SWQN
FROM SH. 1
TWQN
FROM SH. 3
CLKRB
CLKLM
FROM SH. 9
MQDSEL (7)-
MQDSEL (6)-
MQDSEL (5)-
MQDSEL (4)-
MQDSEL (3)-
MQDSEL (2)-
MQDSEL (1)-
MQDSEL (0)-
MQDSEL (15)-
MQDSEL (14)-
MQDSEL (13)-
MQDSEL (12)-
MQDSEL (11)-
MQDSEL (10)-
MQDSEL (9)-
MQDSEL (8)-
MQDSLBT
TQ SH.22
ABUSC (10)-
ABUSC (9)-
ABUSC (8)-
ABUSC (3)-
ABUSC (4)-
ABUSC (5)-
ABUSC (7)-
ABUSC (6)-
MA345-
INTMQD-
MQDGRP3-
CQNSELB-
INTSEL-
MAPCRU-
CRUEN-
CRUAE
SMILED-
MPFLT-
VCC
P2
P4-47
P5-14
TQ SH.19,22
TQ SH.19
TQ SH 19
TQ SH. 14
CRU MQDULE SELECT GENERATIQN
MQD SELECT GENERATIQN
LED
KG105
D96214
2309327
SHEET 26

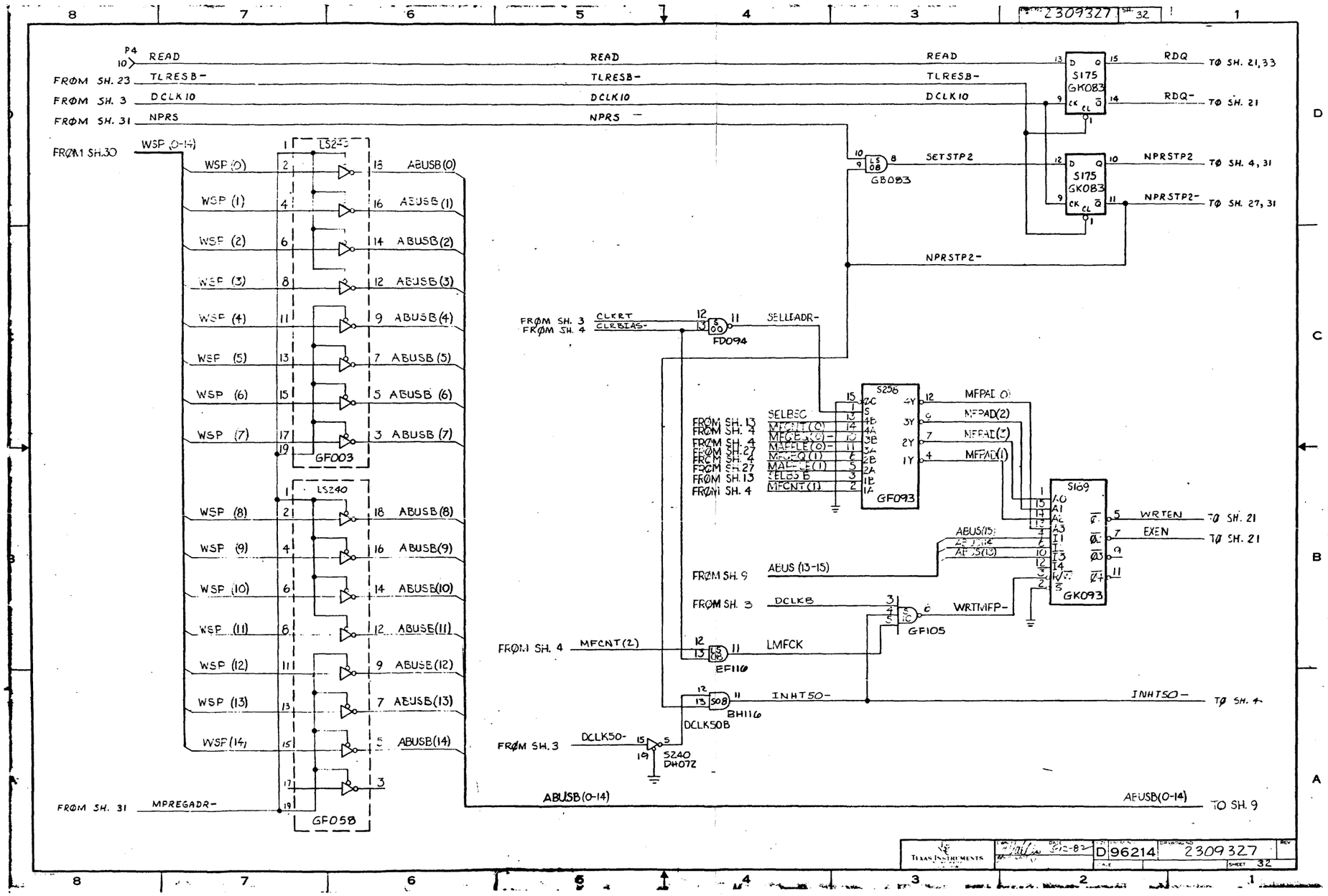

2309327
MEMREQ-
FROM SH.3
MEMREQ
S240
EF105
MEMREQ
MEMREQ
TØ SH. 2, 10, 15, 18, 22, 33
P4
22
MPERINH-
MEMREQI
DH116
MEMREQI
TØ SH. 2, 21
FROM SH. 1 CARVE (3)
FROM SH. 2 CARVC (3)
FROM SH. 3 SET1-
FROM SH. 5 MAPENB
CF038
MAPERD-
MAPERE
MAPERB-
TØ SH. 8, 16, 33
DH116
LS240
EF105
FROM SH.23 TLIØRESB-
S74
CB058
MPERØRB-
MPERØRB-
TØ SH. 21
FROM SH.3 BSLC-CK
MPERØR
MPERØR
TØ SH. 18
FROM SH. 1 TWØN
FROM SH. 4 MAPFLE(0)-
MAPFLE(0)-
FROM SH. 31 MPREGADR
LS377
EN
1D 2D 3D 4D 5D 6D 7D 8D
CK
1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q
FD072
MAPFLEQ(0)-
MAPFLEQ(1)
LS241
GF072
MAPFLE(0)-
TØ SH. 4, 6, 7 10, 11, 12, 13, 28, 30, 32
MAPFLE(1)
TØ SH. 4, 6, 7 10, 11, 12, 28, 30, 32
FROM SH. 3 ADRICHCK
FROM SH. 32 NPRSTP2-
FROM SH. 4 MAPFLE(1)
MAPFLE(1)
TEXAS INSTRUMENTS
D 96214 2309327

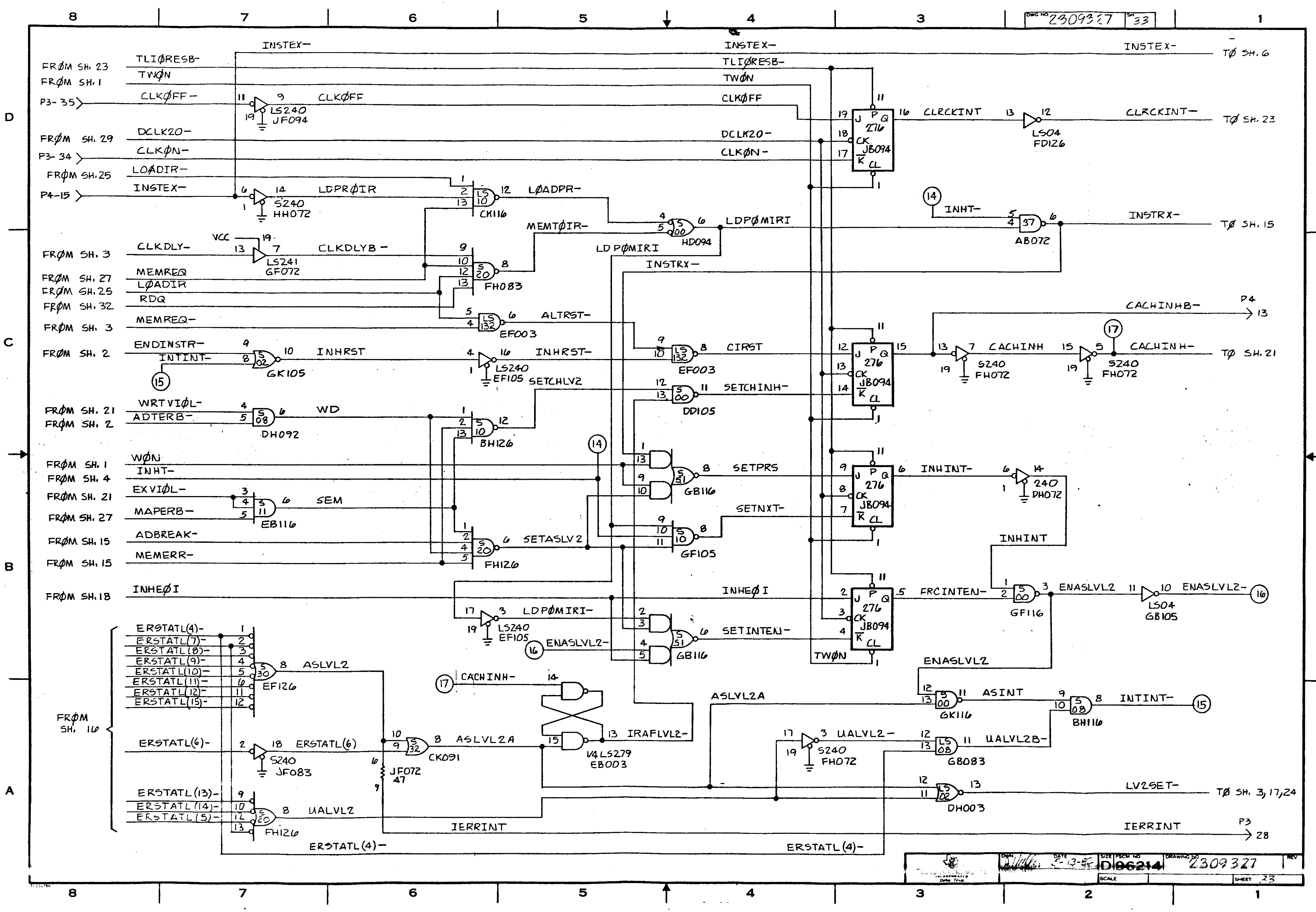

2309327
FROM SH. 4 LDBASE
FROM SH. 3 CLKM
FROM SH 4 CLBSINH-
FROM SH. 4 ENFILEB
FH023
FH047
TO/FROM SH. 6 BASEB0 THRU BASEB15
FROM SH. 4 BSAWEN-
FROM SH. 27 MAPFLE(0)-
FROM SH. 27 MAPFLE(1)
FROM SH. 9 ABUS0 THRU ABUS15
FROM SH. 4 ENFILEA-
FROM SH. 4 ENFILEA
BSAWEN-
MAPFLE(0)-
MAPFLE(1)
ABUS0 THRU ABUS15
ENFILEA-
ENFILEA
EK012
EK023
EK036
EK047
S241
EF023
EF047
BSA(0)
BSA(1)
BSA(2)
BSA(3)
BSA(4)
BSA(5)
BSA(6)
BSA(7)
BSA(8)
BSA(9)
BSA(10)
BSA(11)
BSA(12)
BSA(13)
BSA(14)
BSA(15)
BASEA(0)
BASEA(1)
BASEA(2)
BASEA(3)
BASEA(4)
BASEA(5)
BASEA(6)
BASEA(7)
BASEA(8)
BASEA(9)
BASEA(10)
BASEA(11)
BASEA(12)
BASEA(13)
BASEA(14)
BASEA(15)
BASEA(0) THRU BASEA(15) TO/FROM SH. 5
TEXAS INSTRUMENTS
D 96214
2309327
SHEET 39

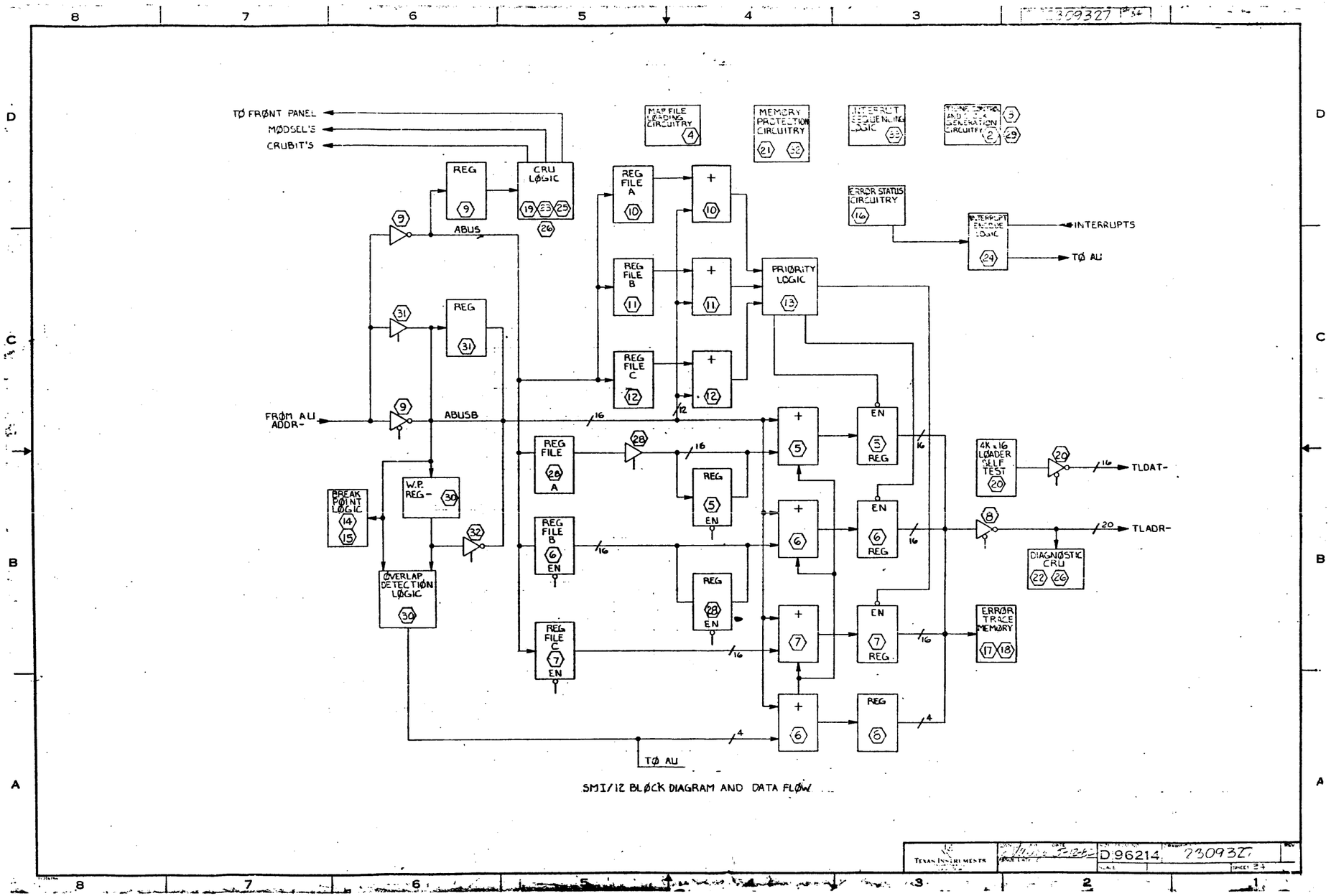

2309327
29
JB072 TERM
LØNG482
DCLK20
FRØM SH. 3
DLYEN
EXC81
CLKMT-
UPC(0)-
ABSMAP-
FAST-
CRU-
JF083
S240
FH093
TØ SH. 24
LNGB
TØSH. 3,24
INHMP-
CRUQ-
TØ SH.12,22
HD105
NPRS-
ED083
NPRESL
UPC(0)-
ABPG-
FASTQ-
CRUQ-
LØNG482Q
LDISTQ-
EF072
S288
EN50
DCLK20B-
TØ SH.9,17
BH058
LDIST-
TØ SH.4
NPPES
TØ SH. 31
NPRSB-
TØ SH. 30
EF081
ENFST-
DTAP30
EB072
S299
EB091
MEMCYC
SWØN
CLKRB
TWØN
EN30
EN90
EN130
EN170
EN210
EN250
CLKDGCRU
TØ SH.22
200 NS ACTIVE DELAY
CB080
DTAP90
DTAP130
DTAP170
DTAP210
DTAP250
TØ SH.3
DTAP50
DTAP40
WØN
AK072
BB100
220 PF
390Ω
HH116
CLKSTØP-
LS240
UF094
CKSTP
TØ SH-2
BH116
GK072
JF067
22
AF097
402
AF098
BD072
TØ SH.2,33
TØ SH. 3
TØ SH 31
TØ SH. 2
TEXAS INSTRUMENTS
D 96214
2309327


2309327
P4-32
LDWSP-
LS241 GF072
LDWSB-
CK091
FROM SH. 4
INHT-
INHT
LS04 CK105
FROM SH. 27
MAPFLE(0)-
FROM SH 27
MAPFLE(1)
FROM SH. 9
ABUSB (0-14)
LDWS-
TO SH. 31
TO SH. 2
L5377
GB003
GB058
FROM SH. 3
CLK_1M
FROM SH. 13
STBA-
CLKRT
S283
FH003
RGCRY(3)
FD003
RGCRY(2)
FH058
RGCRY(1)
FD058
AW (0)
AW (1)
AW (2)
AW (3)
AW (4)
AW (5)
AW (6)
AW (7)
AW (8)
AW (9)
AW (10)
S240
FH072
EK003
MF2ΦR3-
JK026
ΦVPLA
ΦVFB
ΦVFF_AP-
CK003
P4
AWX
AWY
GK003
CMPMFS(1)
SVDMF(1)-
R-PAC 330 HH110
CLCR(0)-
CLCR(1)-
CLCR(2)-
CLCR(3)-
CRA(0)-
CRA(1)-
CRA(2)-
CRA(3)-
CRB(0)
CRB(1)
CRB(2)
CRB(3)
HH072
TO SH. 6
WSP(0-14)
TO SH. 32
NPRES
FROM SH. 29
FROM SH. 31
NPREGADR-
TEXAS INSTRUMENTS
D96214
2309327
SHEET 30


2309327
FRØM SH 30
LDWS –
P3-45
INVADDR –
FRØM SH.9
ADDR(0-15)–
JB072
TERM
FRØM SH. 29
NPRS–
NPRSTP2B –
GK116
HD094
ENIVD–
DBLDR–
EK091
ENNIVD–
TØ SH.9
ADDR(0-15)–
S241
ADDR(0)–
ADDR (1)–
ADDR 2 –
ADDR(3)–
ENI.D
ADDR(4)–
ADDR(5)–
ADDR(6)–
ADDR(7)–
ABUSB (0)
ABUSB (1)
ABUSB (2)
ABUSB (3)
ABUSB (4)
ABUSB (5)
ABUSB (6)
ABUSB (7)
HD025
ADDR(8)–
ADDR(9)–
ADDR(10)–
ADDR(11)–
ADDR(12)–
ADDR(13)–
ADDR(14)–
ADDR(15)–
ABUSB (8)
ABUSB (9)
ABUSB (10)
ABUSB (11)
ABUSB (12)
ABUSB (13)
ABUSB (14)
ABUSB (15)
HD047
ABUSB(0-15)
ABUSB(0-14)
TØ SH. 9
S04
FH093
S299
EB023
EB047
FRØM SH. 29
NPR3B –
FRØM SH.3
FRØM SH.1
FRØM SH.32
ADRLCHK
TWØN
NPRSTP2
NPRSTP2B–
LS04
GB105
NPRS
MPREGADR–
TØ SH. 6,30,32
GF116
NPRSTP2–
MPRE
TØ SH. 6,27
TØ SH. 32
TEXAS INSTRUMENTS
D96214
2309327


2309327
SH. 32
P4
READ
TLRESB-
DCLK10
NPRS
FROM SH. 23
FROM SH. 3
FROM SH. 31
FROM SH.30
WSP (0-14)
LS245
WSP (0)
WSP (1)
WSP (2)
WSP (3)
WSP (4)
WSP (5)
WSP (6)
WSP (7)
ABUSB(0)
ABUSB(1)
ABUSB(2)
ABUSB(3)
ABUSB(4)
ABUSB(5)
ABUSB(6)
ABUSB(7)
GF003
LS240
WSP (8)
WSP (9)
WSP (10)
WSP (11)
WSP (12)
WSP (13)
WSP(14)
ABUSB(8)
ABUSB(9)
ABUSB(10)
ABUSB(11)
ABUSB(12)
ABUSB(13)
ABUSB(14)
FROM SH. 31
MPREGADR-
GF058
S175
GK083
RDQ
TO SH. 21,33
RDQ-
TO SH. 21
SETSTP2
NPRSTP2
TO SH. 4, 31
NPRSTP2-
TO SH. 27, 31
GB083
FROM SH. 3
FROM SH. 4
CLKRT
CLKBIAS-
SELLEADR-
FD094
S256
SELBSC
MFCNT(0)
MFCNT(1)
MFCNT(2)
MAPPLE(0)-
MAPPLE(1)
SELBSB
MFPAD(0)
MFPAD(2)
MFPAD(3)
MFPAD(1)
GF093
S169
GK093
WRTEN
EXEN
TO SH. 21
ABUS(15)
ABUS(13)
FROM SH. 9
ABUS (13-15)
FROM SH. 3
DCLKB
WRTMFP-
GF105
FROM SH. 4
MFCNT(2)
LMFCK
EF116
INHTSO-
TO SH. 4
BH116
DCLK50B
FROM SH. 3
DCLK50-
S240
DH072
ABUSB(0-14)
TO SH. 9
TEXAS INSTRUMENTS
D 96214
2309327
SHEET 32


2309327 SH 33
INSTEX-
TLIØRESB-
TWØN
CLKØFF-
CLKØFF
DCLK20-
CLKØN-
LØADIR-
LDPRØIR
LØADPR-
MEMTØIR-
LDPØMIRI
INSTRX-
CLKDLY-
CLKDLYB-
MEMREQ
RDQ
MEMREQ-
ALTRST-
ENDINSTR-
INTINT-
INHRST
INHRST-
CIRST
SETCHLVL2
SETCHINH-
WRTVIØL-
ADTERB-
WD
WØN
INHT-
EXVIØL-
MAPERB-
SEM
SETPRS
SETNXT-
ADBREAK-
MEMERR-
SETASLVZ
INHEØI
LDPØMIRI-
ENASLVL2-
SETINTEN-
CLRCKINT
CLRCKINT-
INSTRX-
CACHINHB-
CACHINH
CACHINH-
INHINT-
INHINT
FRCINTEN-
ENASLVL2
ASLVL2
ASLVL2A
ASINT
INTINT-
IRAFLVL2-
UALVL2-
UALVL2B-
LV2SET-
UALVL2
IERRINT
ERSTATL(4)-
ERSTATL(6)-
ERSTATL(13)-
ERSTATL(14)-
ERSTATL(5)-
FRØM SH. 23
FRØM SH. 1
FRØM SH. 29
FRØM SH. 25
FRØM SH. 3
FRØM SH. 27
FRØM SH. 32
FRØM SH. 2
FRØM SH. 21
FRØM SH. 4
FRØM SH. 15
FRØM SH. 18
FRØM SH. 16
TØ SH. 6
TØ SH. 23
TØ SH. 15
TØ SH. 21
TØ SH. 3, 17, 24
D96214
2309327
SHEET 23



SMJ/12 BLØCK DIAGRAM AND DATA FLØW

Alphabetical Index

Introduction

HOW TO USE INDEX

The index, table of contents, list of illustrations, and list of tables are used in conjunction to obtain the location of the desired subject. Once the subject or topic has been located in the index, use the appropriate paragraph number, figure number, or table number to obtain the corresponding page number from the table of contents, list of illustrations, or list of tables.

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The following index lists key words and concepts from the subject material of the manual together with the area(s) in the manual that supply major coverage of the listed concept. The numbers along the right side of the listing reference the following manual areas:

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  Tx-yy

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