Model 990/10 and 990/12 Computer Memories Depot Maintenance Manual

Part No. 2250690-9701 *A
15 December 1980

TEXAS INSTRUMENTS

LIST OF EFFECTIVE PAGES

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Model 990/10 and 990/12 Computer Memories Depot Maintenance Manual (2250690-9701)

Original Issue ..... 1 May 1980
Change 1 ..... 15 December 1980 (MCR 000911)

Total number of pages in this publication is 274 consisting of the following:

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Preface

This manual provides depot-level maintenance information for memory boards used with the Model 990/10 or Model 990/12 Minicomputer Systems. The manual is organized into the following four sections.

Section

1 General Description — Provides an introduction, overview, and specifications for the memory boards described in the manual.

2 Functional Description — Provides detailed theory of operation for the memory boards.

3 Maintenance — Describes the depot maintenance philosophy and provides the checkout and fault isolation procedures for the memory boards.

4 Drawings — Provides the assembly drawings and logic diagrams for the memory boards.

Additional information related to the use of the memory boards in the Model 990/10 and the Model 990/12 Minicomputer Systems may be found in the following documents.

Title	Part Number
Model 990 Computer 733 ASR/KSR Terminal Installation and Operation	945259-9701
Model 990/10 Computer System Hardware Reference Manual	945417-9701
Model 990/10 Computer System Field Maintenance Manual	945402-9701
Model 990/10 Computer System Depot Maintenance Manual	945404-9701
Model 990/12 Computer Hardware User's Manual	2264446-9701
Model 990/12 Computer System Field Maintenance Manual	2264447-9701

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1

General Description

1.1 GENERAL

This manual provides detailed theory and depot-level maintenance procedures for TILINE* memory boards that use a 16,384-bit dynamic random-access memory chip for primary memory storage. The memory boards described in this manual may be used with the Model 990/10 or Model 990/12 Minicomputer Systems and will be referred to as the TILINE memory. This section provides a brief general description of the TILINE memory boards.

1.2 TILINE MEMORY BOARDS

The TILINE memory boards described in this manual consist of the Memory Controller, 96KB, with Error Checking and Correction, 990/16KR, hereinafter referred to as the 96KB memory controller; the Cache Memory Controller, 64KB, with Error Checking and Correction, 990/16KR, hereinafter referred to as the cache controller; and the Memory Add-On Module, 256KB, with Error Checking and Correction, 990/16KR, hereinafter referred to as the 256KB add-on memory array. Configurations and parts numbers of the TILINE memory boards are as shown in table 1-1. Environmental specifications for the boards are as shown in table 1-2, power requirements are shown in table 1-3.

Table 1-1. TILINE Memory Boards

Logic Board	TI Part Number
96KB memory controller board (standard version)	
with 0 bytes RAM (controller only)	2261980-1
with 32K bytes RAM	2261980-2
with 64K bytes RAM	2261980-3
with 96K bytes RAM	2261980-4
96KB memory controller board (fine line version) 0 bytes RAM (controller only)	2261980-5
with 32K bytes RAM	2261980-6
with 64K bytes RAM	2261980-7
with 96K bytes RAM	2261980-8
Cache memory controller board (64K bytes RAM)	2261990-1
256KB add-on memory array board	
with 64K bytes RAM	948955-1
with 128K bytes RAM	948955-2
with 192K bytes RAM	948955-3
with 256K bytes RAM	948955-4

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Table 1-2. TILINE Memory Boards Environmental Specifications

Item	Specification
Operating	
Temperature[1]	0° to 65° C (32° to 149° F)
Humidity	0 to 95%, noncondensing
Storage	
Temperature	−40° to 70° C (−40° to 158° F)
Humidity	0 to 95%, noncondensing
Shock	Will sustain 2-foot vertical drop when installed in the chassis
Vibration	Will withstand 1G at 5 Hz to 80 Hz and 0.3G at 80 Hz to 500 Hz
Altitude	0 to 3.05 km (0 to 10,000 ft)

Note:

[1] Lower the upper operating temperature limit by 2°C (3.6°F) for every 762 meters (2500 feet) increase in altitude.

Table 1-3. Memory Board Current Requirements in Amperes

Voltage	Current, Maximum Cycle Rate[1]	Current, Idle Operation	Current, Standby Operation
96KB Memory Controller			
+5V Main	2	2	0
+5V Stby	0.550	0.550	0.170
+12V Stby	0.550	0.120	0.120
−5V Stby	0.0025	0.002	0.0025
256KB Add-On Memory Array			
+5V Main	0.200	0.200	0
+5V Stby	0.400	0.350	0.080
+12V Stby	1.10	0.350	0.350
−5V Stby	0.001	0.000020	0.000020
Cache Controller			
+5V Main	6	6	0
+5V Stby	0.600	0.600	0.200
+12V Stby	0.550	0.120	0.120
−5V Stby	0.002	0.002	0.002

Note:

[1] Current maximum cycle rate based on 1 cycle per microsecond for the 96KB memory controller and 256KB add-on memory array and 500-nanosecond average cycle rate for the cache controller. Current drain figures assume that each board is fully implemented with memory devices for maximum storage capacity.

2

Functional Description

2.1 GENERAL

This section provides a functional description of the TILINE memory. As shown in table 1-1, standard options of the 96KB memory controller board in standard and fine line versions provide memory capacity that ranges from 32K to 96K bytes on a single board in increments of 32K bytes. When system requirements are for greater than 96K bytes of memory, additional memory can be implemented by installing add-on memory array boards in full-sized slots of the chassis. Error checking and correcting (ECC) is a standard feature of TILINE memory.

The TILINE memory consists of two different memory controllers; the 96KB memory controller and the cache controller board. The cache controller uses a cache technique to improve the effective operating speed of primary memory. Expansion of memory is implemented by adding 256KB add-on memory array boards. Through the use of two memory controller boards, each with four add-on boards, total memory capacity can be expanded to 2M bytes when used in a 990/10 or 990/12 minicomputer system.

The paragraphs that follow provide a detailed description of each of the memory controllers and of the add-on memory array board.

2.2 96KB MEMORY CONTROLLER

The 96KB memory controller is a multilayered board that contains the memory control logic, storage logic, storage elements for up to 96K bytes of metal-oxide semiconductor (MOS) random-access memory (RAM) on the board, and the control logic for up to 1M bytes of additional memory on associated add-on memory expansion boards. The 96KB memory controller interface to the TILINE bus is made through the two 80-pin connectors at the bottom edge of the board that installs into the chassis slot. Two 50-pin connectors at the top edge of the board are used to interface with expanded memory. Table 2-1 describes these interface signals in detail. The interface signals to the TILINE at the bottom edge of the board are as described in table 2-2.

The 96KB memory controller functions as a TILINE SLAVE device. As such, it generates or accepts data only in response to a TILINE MASTER device. Logic on the 96KB memory controller consists of TILINE interface logic, timing and memory refresh control circuits, and error checking and correction circuits. The memory array on the memory controller consists of from zero to three banks (rows) of memory chips, with 22 memory chips in each bank. Each memory word consists of 16 data bits and six check bits. During normal operation, only the data bits are processed on the TILINE data bus.

The 96KB memory controller board may be placed in a diagnostic mode by addressing the memory controller logic at a specified TILINE Peripheral Control Space (TPCS) address. Cycle control and refresh control for the add-on memory boards are provided by the 96KB memory controller board, but the add-on memory expansion boards interface directly with the TILINE for address selection. The 96KB memory controller circuits, including the error checking and correcting circuits, are implemented in transistor-transistor logic (TTL) devices on the lower part of the board (figures 2-1 and 2-1A). The

Table 2-1. Memory Controller to 256KB Add-On Memory Array Board Interface Signals

Signature	Pin Number	Definition
MB00-	P4-1	22-bit bidirectional data bus that transfers read and write data between the two boards (includes six check bits: MB16- through MB21-).
MB01-	P4-3	
MB02-	P4-5	
MB03-	P4-7	
MB04-	P4-9	
MB05-	P4-11	
MB06-	P4-13	
MB07-	P4-15	
MB08-	P4-17	
MB09-	P4-19	
MB10-	P4-21	
MB11-	P4-23	
MB12-	P4-25	
MB13-	P4-27	
MB14-	P4-29	
MB15-	P4-31	
MB16-	P4-33	
MB17-	P4-35	
MB18-	P4-37	
MB19-	P4-39	
MB20-	P4-41	
MB21-	P4-43	
IBSEL-	P3-19	Board selected signal. The board selected signal is sent to the memory board controller when the 256KB add-on memory array board decodes a TILINE address that falls in the address space defined by the address switches and memory size jumpers.
IR/W-	P3-21	Read/write control. The read/write control line to the 256KB add-on memory array board specifies either a read or write memory operation.
ADODD	P3-29	Odd word address. The address odd line operates in conjunction with the read/write control line to enable both rows in a selected bank during a read operation or to enable only the required odd or even row during a write operation.
IRAS-	P3-13	Row address strobe. The row address strobe clocks seven row address bits into memory chips.
ICADSEL	P3-7	Column address select. The column address select line causes the second seven address bits to be applied to the memory chips.
ICAS-	P3-15	Column address strobe. Column address strobe clocks the seven column address bits into the memory chips.

Table 2-1. Memory Controller to 256KB Add-On Memory Array Board Interface Signals (Continued)

Signature	Pin Number	Definition
RFAD0- RFAD1- RFAD2- RFAD3- RFAD4- RFAD5- RFAD6-	P3-27 P3-33 P3-17 P3-35 P3-25 P3-23 P3-31	Refresh address lines. Refresh address lines provide the row address to the memory chips during a refresh operation.
REFRESH-	P3-5	Refresh cycle in progress. The refresh control line causes the refresh address lines to be applied to the memory chips that are then strobed into the memory chips by the IRAS- pulse.
+5 SWEN-	P3-1	5-volt switch enable. Turns on power (5 volts) to 256KB add-on memory array whenever main power is on or during a refresh operation in stand-by operation.
POWERON-	P3-11	Power on. Power on is true after 5 volts is stable. When false, this signal inhibits extraneous strobes to the memory chips.
IORES-	P3-37	I/O reset. The reset line resets the error indication lamps after initial power-up and in response to a front panel reset or execution of a RSET instruction.
IMERR-	P3-3	Memory error, multibit error. Memory error is generated by the control logic of the memory controller during a read cycle and sets the error indication lamp on the selected 256KB add-on memory array board.
ICERR-	P3-9	Correctable error, one-bit error detected. The correctable error signal is generated by the control logic of the memory controller during a read cycle. This indicates that a one-bit error has occurred and sets the error indication lamp on the selected 256KB add-on memory array board.

Table 2-2. TILINE Signal Definitions

Signature	Pin Number	Definition
TLGO-	P1-25	TILINE Go: Initiates all data transfers when transition from high (3 V) to low (1 V) occurs.
TLREAD	P1-11	TILINE Read: When high (3 V), designates a read from SLAVE operation; when low (1 V), designates a write to SLAVE operation.
TLADR00-	P2-55	TILINE address: To define the location of data during a fetch or store operation. When high (≥2 V), the corresponding address bit is a zero; when low (≤0.8 V), the corresponding address bit is a one.
01-	P2-44	
02-	P2-51	
03-	P2-53	
04-	P2-57	
05-	P2-59	
06-	P2-47	
07-	P2-49	
08-	P2-17	
09-	P2-19	
10-	P2-10	
11-	P2-12	
12-	P2-11	
13-	P2-15	
14-	P2-8	
15-	P2-9	
16-	P2-29	
17-	P2-27	
18-	P2-25	
TLADR19-	P2-31	
TLDAT00-	P2-67	TILINE Data: Bidirectional data lines that, when high (≥2 V), represent zero data bits and, when low (≤0.8 V), represent one data bits.
01-	P2-69	
02-	P2-35	
03-	P2-37	
04-	P2-61	
05-	P2-63	
06-	P2-43	
07-	P2-45	
08-	P2-21	
09-	P2-33	
10-	P2-23	
11-	P2-20	
12-	P1-27	
13-	P1-28	
14-	P1-30	
TLDAT15-	P1-31	
TLTM-	P1-20	TILINE Terminate: When low (1 V), indicates that the SLAVE device has completed the requested operation.
TLMER-	P1-55	TILINE Memory Error: When low (≤0.8 V), indicates that a nonrecoverable error has occurred during a memory read operation.

Table 2-2. TILINE Signal Definitions (Continued)

Signature	Pin Number	Definition
TLAG (in)	P2-6	TILINE Access Granted: When high (≥2 V), indicates that no higher-priority device has requested use of the TILINE. When low (≤0.8 V), prevents the receiving device from gaining access to the TILINE bus.
TLAG (out)	P2-5	TILINE Access Granted: When high (≥2 V), indicates that neither the sending device nor any higher-priority device is requesting use of the TILINE. When low (≤0.8 V), indicates that either the sending device or some higher-priority device is requesting use of the TILINE bus and prevents all lower-priority devices from gaining access to the bus.
TLAK-	P1-71	TILINE Acknowledge: When high (3 V), indicates that no TILINE device has been recognized as the next device to use the TILINE. When low (1 V), indicates that some TILINE device has requested access, has been recognized, and is waiting for the bus to become available.
TLAV	P1-58	TILINE Available: When high (3 V), indicates that no TILINE device is using the bus. When low (1 V), indicates that the TILINE bus is busy.
TLWAIT-	P1-63	TILINE Wait: A normally high (3 V) signal that, when low (1 V), temporarily suspends all TILINE MASTER devices from using the TILINE bus. This signal is generated by bus couplers to allow them to use the bus as the highest-priority user. The cache controller also generates TLWAIT- during initialization of the cache controller.
TLIORES-	P1-14 P2-14	TILINE I/O Reset. A normally high (≥2 V) signal that, when low (≤0.8V), halts and resets all TILINE I/O devices. This signal is a 100- to 500-nanosecond pulse generated by the RESET switch on the programmer panel or by the execution of a RSET instruction in the AU.
TLPRES-	P1-13 P2-13	TILINE Power Reset: A normally high (≥2 V) signal that goes low (≤0.8 V) to reset all TILINE devices and inhibit critical lines to external equipment. The signal is generated by the power supply at least 10 μs before dc voltages begin to fail during power-down and until dc voltages are stable during power-up.
TLPFWP-	P1-16 P2-16	TILINE Power Failure Warning Pulse: A pulse that precedes TLPRES- by 2 ms. When low (≤0.8 V), indicates that a power-down sequence is in progress, allowing the AU to perform its power failure interrupt subroutine.
TLHOLD-	P2-26	TILINE Hold Signal: A normally high (3 V) signal that goes low (1 V) to assert that a central processing unit (CPU) is executing an Absolute Value (ABS) instruction. TILINE Hold prevents interference from another processor on the TILINE while the first processor is performing the ABS instruction. This signal is used and propagated by TILINE COUPLERS in multiprocessor systems.
TLCACHEN	P1-73	TILINE Cache Enable Signal: The cache memory in the cache controller is enabled when this signal is high.

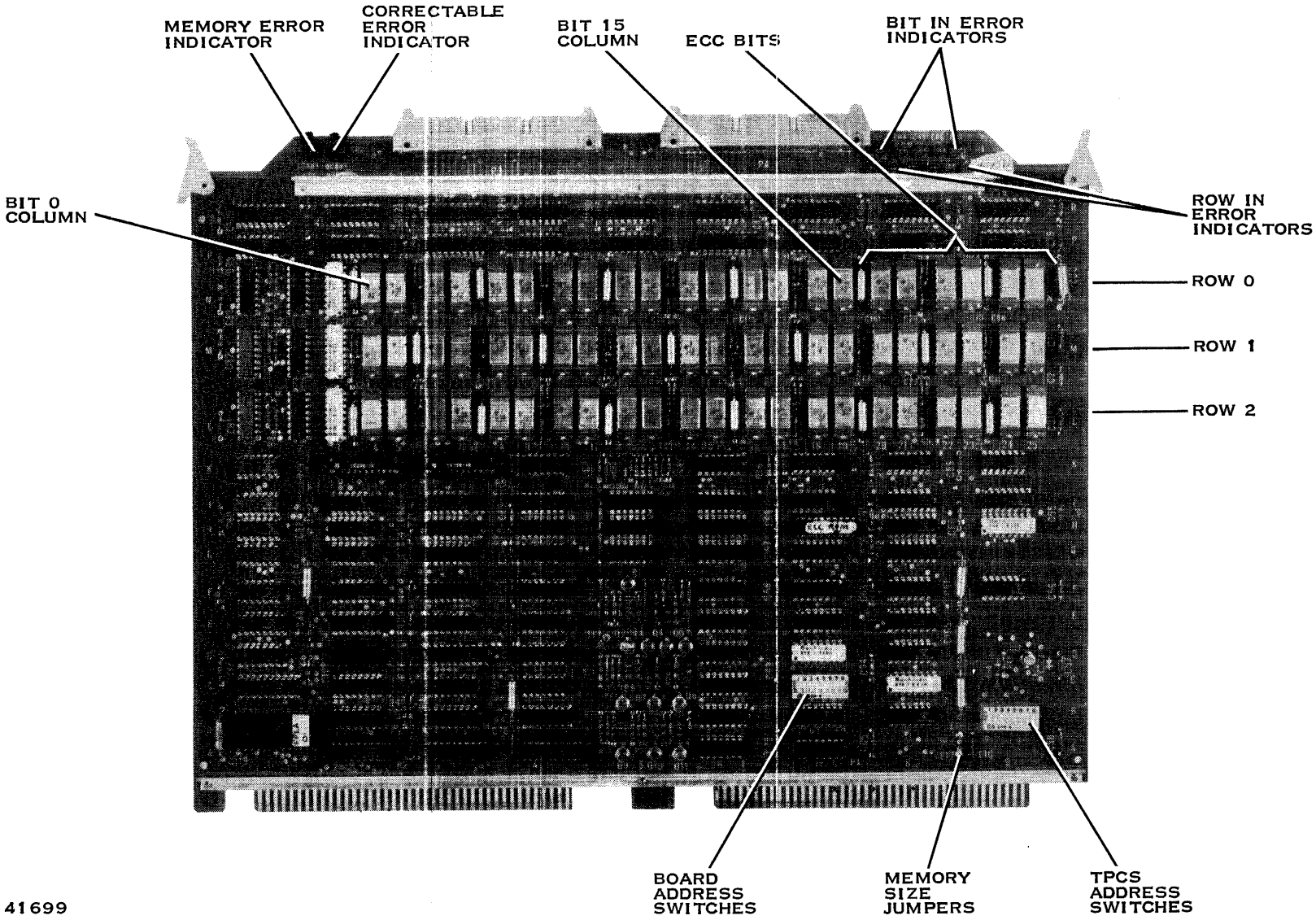


Figure 2-1. 96KB Memory Controller Board Component Locations, Standard Version

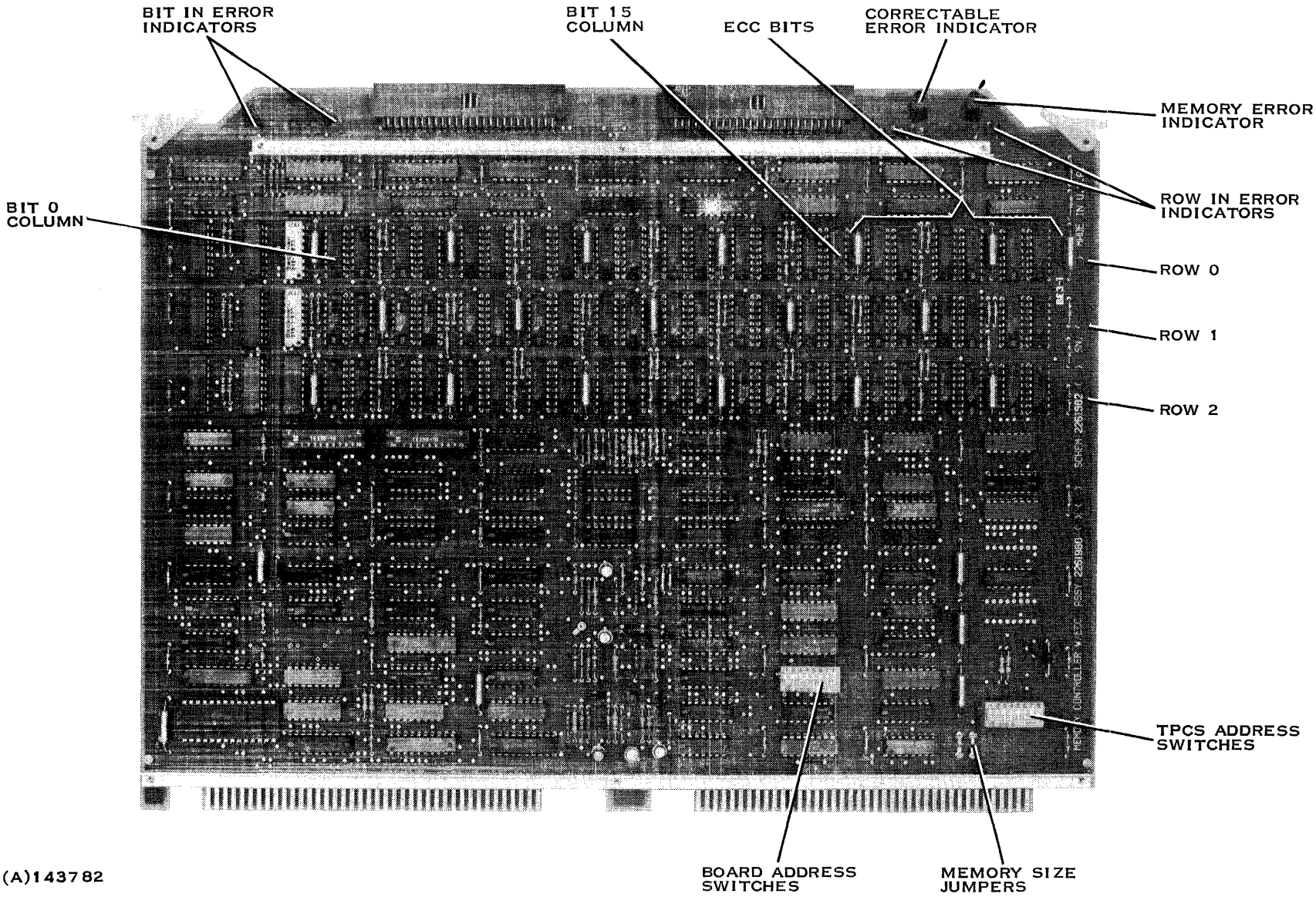


Figure 2-1A. 96KB Memory Controller Board Component Locations, Fine Line Version

96K bytes of on-board MOS memory consists of three rows of TMS 4116 devices across the top of the board. Each row includes the 22 devices required for the storage of 16 data bits and 6 ECC bits. The TMS 4116 chip is based on N-channel silicon gate technology, and the inputs and outputs are TTL compatible.

As shown in figure 2-1, the 96KB memory controller board includes, in addition to TTL control logic, 2 light-emitting diode (LED) error indicators, 11 LED chip failure indicators, and 2 dual-in-line switch packages. One of these switch packages is used to set the starting address of the on-board memory. The other switch package is used to select a TPCS address. The two error-indicating LEDs indicate that a one-bit (correctable) error or a multibit (uncorrectable) error has occurred on this board. The correctable error LED lights when the error-correcting logic detects and corrects an error in data read from memory. The memory error LED lights when the error-detecting logic senses a data error that cannot be corrected (two or more bits in error).

These indicators are set on the first occurrence of the respective error stimulant and remain set until the board is powered down or until an I/O RSET instruction is issued. The additional 11 chip failure LEDs pinpoint the memory chip that caused the first single-bit error. Any additional errors do not affect the chip failure LEDs. However, subsequent errors are recorded by the two error indicators located on the board where the error occurred. The 11 chip failure indicators are divided into 2 groups, as shown in figure 2-2. A group of five LEDs forms a binary code that identifies the bit that failed. The remaining six LEDs form a binary code that identifies the row that contains the failing chip. Table 2-3 summarizes the error indicators and their functions.

The dual-in-line base address switch consists of eight single-pole, single-throw address switches. The address switches correspond to the 8 most significant bits (MSB) of the 20-bit TILINE address and permit board starting address selection in 8K-byte increments. Switch 1 is the most significant bit

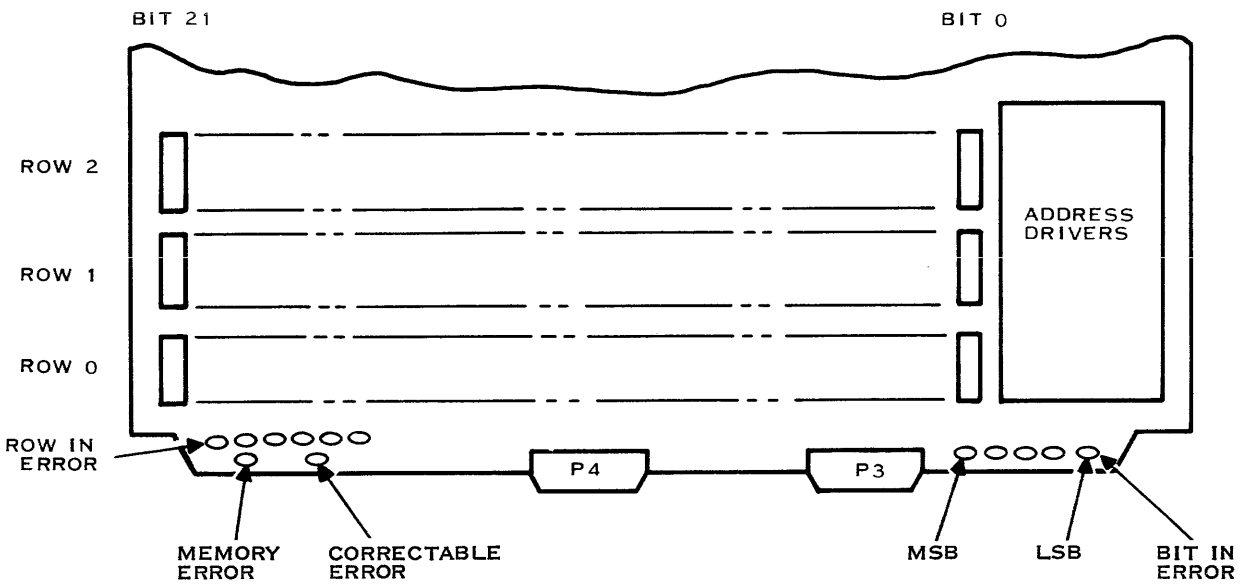
of the address and switch 8 is the least significant bit (LSB). The required switch settings for the 96KB memory controller are shown in table 2-4. Addresses other than those shown can be represented in a similar manner by using the eight switches to represent the binary number. Since each of the 3 rows of memory devices represents 32K bytes of memory, the memory capacity available is either 0, 32K, 64K, or 96K bytes. Memory size is set by connecting memory size jumpers as shown in table 2-5.

The diagnostic mode pencil switches correspond to address bits 11 through 18 of the 20-bit TILINE address bus and select the TPCS address used to operate the controller in the diagnostic mode. Switch 1 is the most significant bit, and switch 8 is the least significant bit. This permits the selection of 512 addresses that fall between $F800_{16}$, and $FBFE_{16}$, inclusive, in the 15-bit address form and between $FFC00_{16}$ and $FFDFF_{16}$ inclusive, in the 20-bit form. Table 2-6 shows some typical TPCS addresses and their corresponding switch settings. The recommended TPCS addresses for 96KB memory controllers are shown in table 2-7. Software provided by Texas Instruments expects these values to be used.

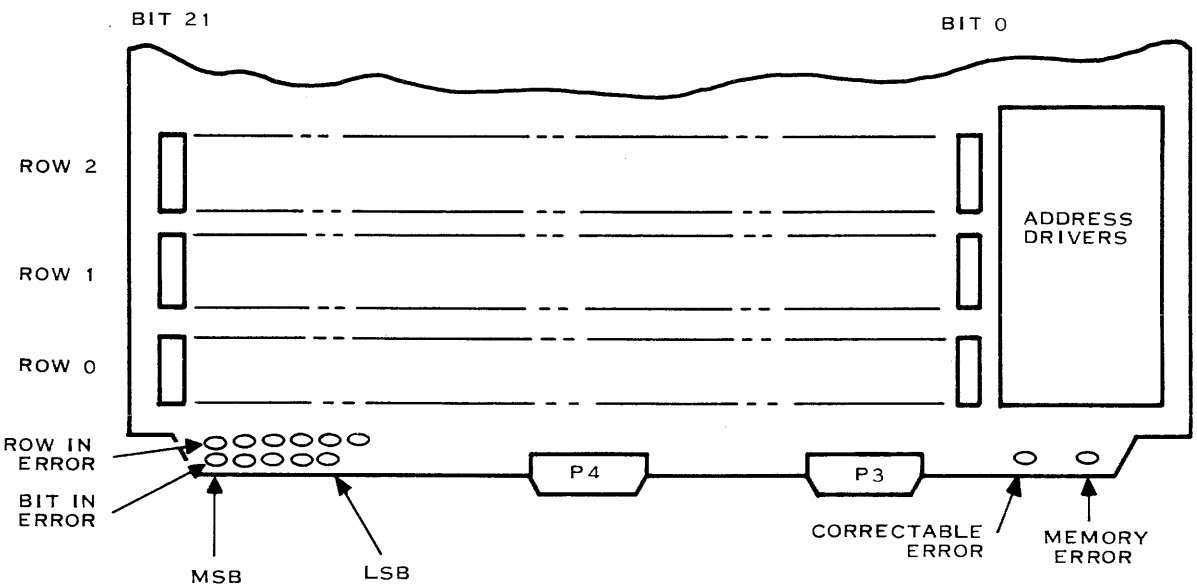
A host computer may place the 96KB memory controller in the diagnostic mode by addressing the controller with the correct TPCS address (see table 2-7) on the TILINE

Table 2-3. Description and Function of 96KB Memory Controller Error Indicators

Indicator	Description	Display Convention
Bit In Error	Hexadecimal Code 00 = Bit 0 . . 0F = Bit 15 . . 15 = Bit 21	LED On: Bit = 1
Row In Error	Hexadecimal Code 00 = Row 0 01 = Row 1 02 = Row 2 . . 22 = Row 34	LED On: Bit = 1
Memory Error	Multibit error on this board	LED On: Error
Correctable Error	Single-bit error on this board	LED On: Error



FINE LINE VERSION



STANDARD VERSION

(A)143783

Figure 2-2. 96KB Memory Controller Board Error Indicators

address lines while executing a write operation. When in the diagnostic mode, testing of all on-board memory banks and add-on expansion memory banks may be performed.

When the proper TPCS address is found to be present on the TILINE address lines, the controller examines the data bits present on the TILINE data bus for instructions on how to conduct the self-test. As shown in figure 2-3, bits 0 through 3 specify which of the four areas of memory on which to administer the test. The memory that is mounted on the 96KB memory controller board is divided into Bank A, Bank B, and Bank C. Additional memory boards are considered as expansion. Bank A addresses fall between the base address plus 16384_{16} (16K). Bank B addresses start at the end of Bank A and continue for another 16K. Bank C addresses fall similarly,

Table 2-4. 96KB Memory Controller Board, Starting Address Switch Settings

Beginning Word Address on Board ( )$_{16}$	Switch Setting								Number of Memory Words Below Board
	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	
00000	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0
01000	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	4,096
02000	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	8,192
03000	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	12,288
04000	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	16,384
05000	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	20,480
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0F000	OFF	OFF	OFF	OFF	ON	ON	ON	ON	61,440
10000	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	65,536
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
40000	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	262,144
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
F4000	ON	ON	ON	ON	OFF	ON	OFF	OFF	999,424

Table 2-5. 96KB Memory Controller Board Memory Size Jumper Schedule

Memory Size (Bytes)	Jumper E9	Jumper E10
0	OFF	OFF
32K	OFF	ON
64K	ON	OFF
96K	ON	ON

Table 2-6. TPCS Addresses and Corresponding Pencil Switch Settings

CPU Address	TPCS Address	Switch Setting SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
F800-02	FFC00-01	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
F804-06	FFC02-03	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
F81C-1E	FFC0E-0F	OFF	OFF	OFF	OFF	OFF	ON	ON	ON
F820-22	FFC10-11	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
F9FC-FE	FFCFE-FF	OFF	ON	ON	ON	ON	ON	ON	ON
FA00-02	FFD00-01	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
FBFC-FE	FFDFE-FF	ON	ON	ON	ON	ON	ON	ON	ON

Table 2-7. TPCS Locations for the 96KB Memory Controller

Typical Assignments for Memory Devices	Device
FB00	First 96KB memory controller (Switches 1 and 2 On)
FB04	Second 96KB memory controller (Switches 1,2, and 8 On)

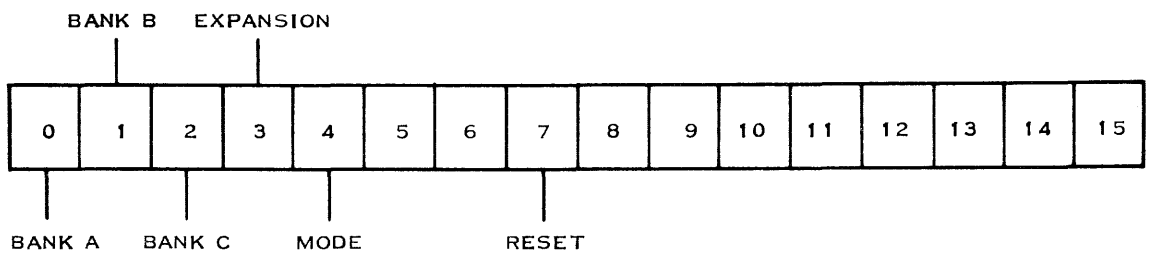


Figure 2-3. TPCS Data Word Bit Assignments

starting with the uppermost boundary for Bank B and continuing for another 16K.

Bit 4 controls the mode of the data placed on the TILINE data bus. When bit 4 is zero, the error correction logic on the controller is disabled and data is passed to the CPU unchanged. When bit 4 is set to one, the six check bits are exchanged for the most significant data bits. This allows the user to directly access the check bits generated by the ECC logic and to monitor their validity. Bit 7, when set to one, acts like an I/O reset to clear the controller error latches from the controller, restoring the memory controller board to normal operation.

When reading the TPCS word, the 96KB memory controller places data words on the TILINE data bus. The data words read are even and odd forms of the TPCS address as set in the TPCS pencil switches. The content and meaning of the two data words are as shown in figure 2-4.

After being placed in the diagnostic mode, data bits 0 through 7 of the TILINE data word are examined by the diagnostic logic when a TILINE write operation is peformed. The user can form this data word to control the following features:

- Selection of a portion of memory on which to perform the diagnostic test
- Selection of the diagnostic mode
- Clearing the error latches

Expansion memory cannot be modified into

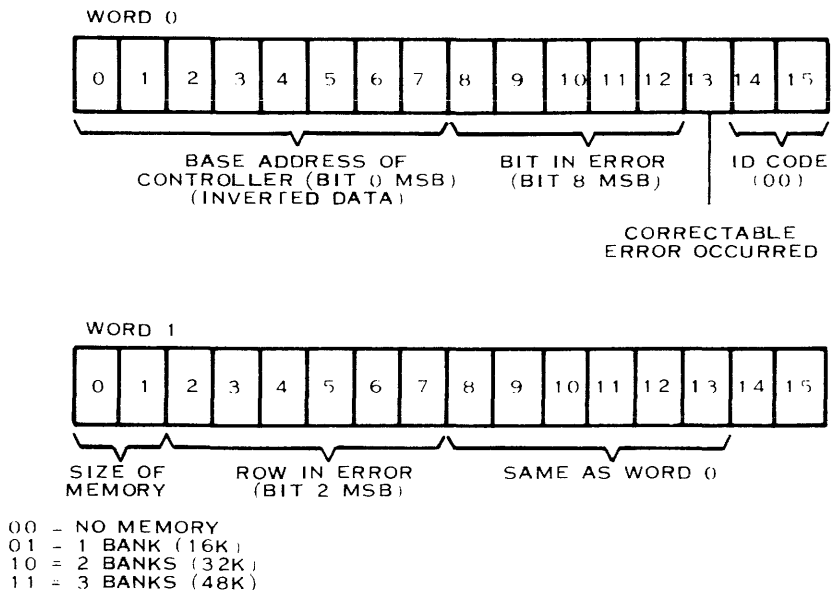


Figure 2-4. Word 0 and Word 1 Placed on the TILINE Data Bus by the 96KB Memory Controller When in the Diagnostic Mode During a Read Operation

banks. Data bits 0 through 3 select one or all of the banks and/or the expansion. Data bit 4 selects the mode under which the diagnostic should be run. When this bit is zero, the error detection and correction logic is disabled in the specified banks. When data bit 4 is one, the most significant data bits of the word are swapped through the multiplexer with the six error-checking bits in the banks or memory area specified. When bit 7 is one, a command is issued to clear all latches and disable all three-state TPCS devices to restore the controller to normal operation.

2.2.1 TMS 4116 Memory Chip

The TMS 4116 memory chip is a monolithic, high-speed, dynamic, 16,384-bit MOS RAM organized as 16,384 one-bit words. All inputs and outputs are compatible with TTL logic, including the clocks: Row Address Strobe (RAS-) and Column Address Strobe (CAS-). The seven address lines and the data-in (DI) lines are latched on the chip to simplify system design. The data out (DO) line is unlatched to allow greater system flexibility. To decode 1 of 16,384 storage cell locations, 14 address bits are required. To achieve this, seven row-address bits are set up on the seven address lines and latched onto the chip by RAS-. Then, in this system, a column address select (CADSEL-) signal applies the seven column address bits to the seven address lines. The CAS- strobe latches the column address bits onto the chip. A refresh operation must be performed at least every two milliseconds to retain data. Each of 128 row addresses is strobed with RAS- to cause all bits in each row to be refreshed. Since the output buffer is in the high-impedance state unless CAS- is applied, the "RAS- only" refresh sequence avoids any output during refresh. CAS- remains high (inactive) for this refresh sequence, thus conserving power.

2.2.2 Control and Operation

The 96KB memory controller monitors the TILINE, decodes addresses on the TILINE address bus, and directs the performance of read and write cycles to addressed memory under control of a TILINE MASTER device. This addressed memory can be on board or located on add-on expansion boards. The following functional description is keyed to the block diagram for the memory board (figure 2-5).

2.2.2.1 Memory Timer. Pulses used to control the timing and sequence of operation during memory read and write operations are provided by the memory timer. This includes timing for the memory refresh cycle that is a memory read operation. The memory timer consists of two resistance/capacitance (RC) timers and two 250-nanosecond delay lines along with associated TTL logic. Each 250-nanosecond delay line has 10 output taps that are separated from each other in time by 25 nanoseconds. An input signal to the delay line is propagated down the line and is reproduced at each output tap, with each progressive tap introducing an additional 25 nanoseconds of delay to the input signal. The delayed-by-250-nanoseconds output of the first delay line is the input to the second delay line, providing a total delay of 500 nanoseconds.

Reference is made to the simplified functional diagram for the memory timer in the following discussion of the operation of the timer (figure 2-6). When the 96KB memory controller is not busy with a previous memory operation nor a refresh operation, the asserted TLGO- from the MASTER device provides a high BTLGO to trigger the two RC timers. In turn, these generate the GO120 and GO170 pulses at approximately 120 and 170 nanoseconds after the asserted TLGO-. GO120 clocks a flip-flop to generate the row address strobes for both on-board use and for add-on memory expansion board use. With either the 96KB memory controller or add-on memory addressed, the low board selected signal (BSEL-) is clocked by GO170. A high BSEL- signal produces the low ENDCYC- signal to abort the cycle. Assuming a valid address is presented to the local memory or to an add-on memory expansion board, as BUSY goes high (at time T170 after TLGO- is asserted), a high pulse is clocked into the input of the first of the two delay lines. At the time T270, a pulse that is

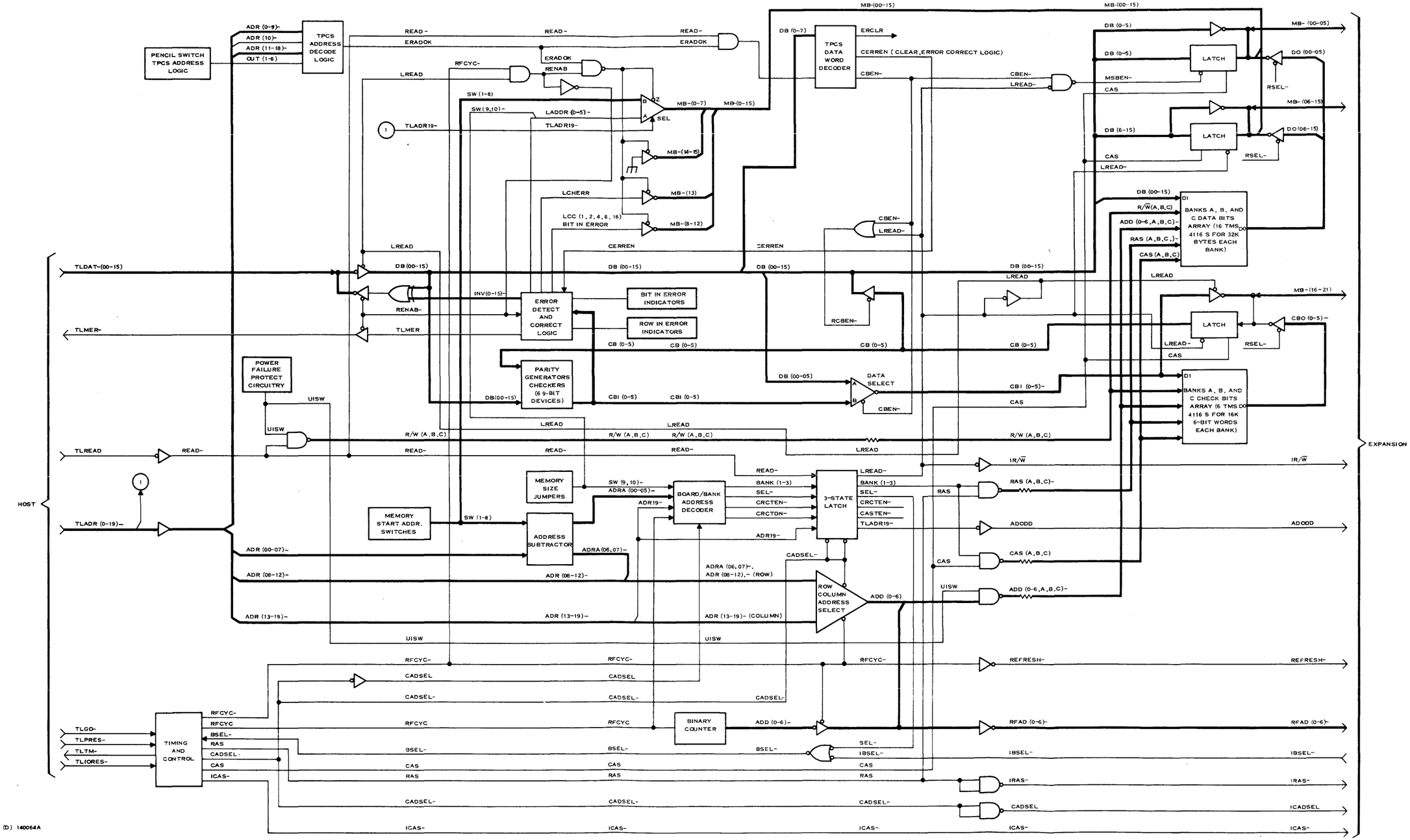


Figure 2-5. 96KB Memory Controller Block Diagram

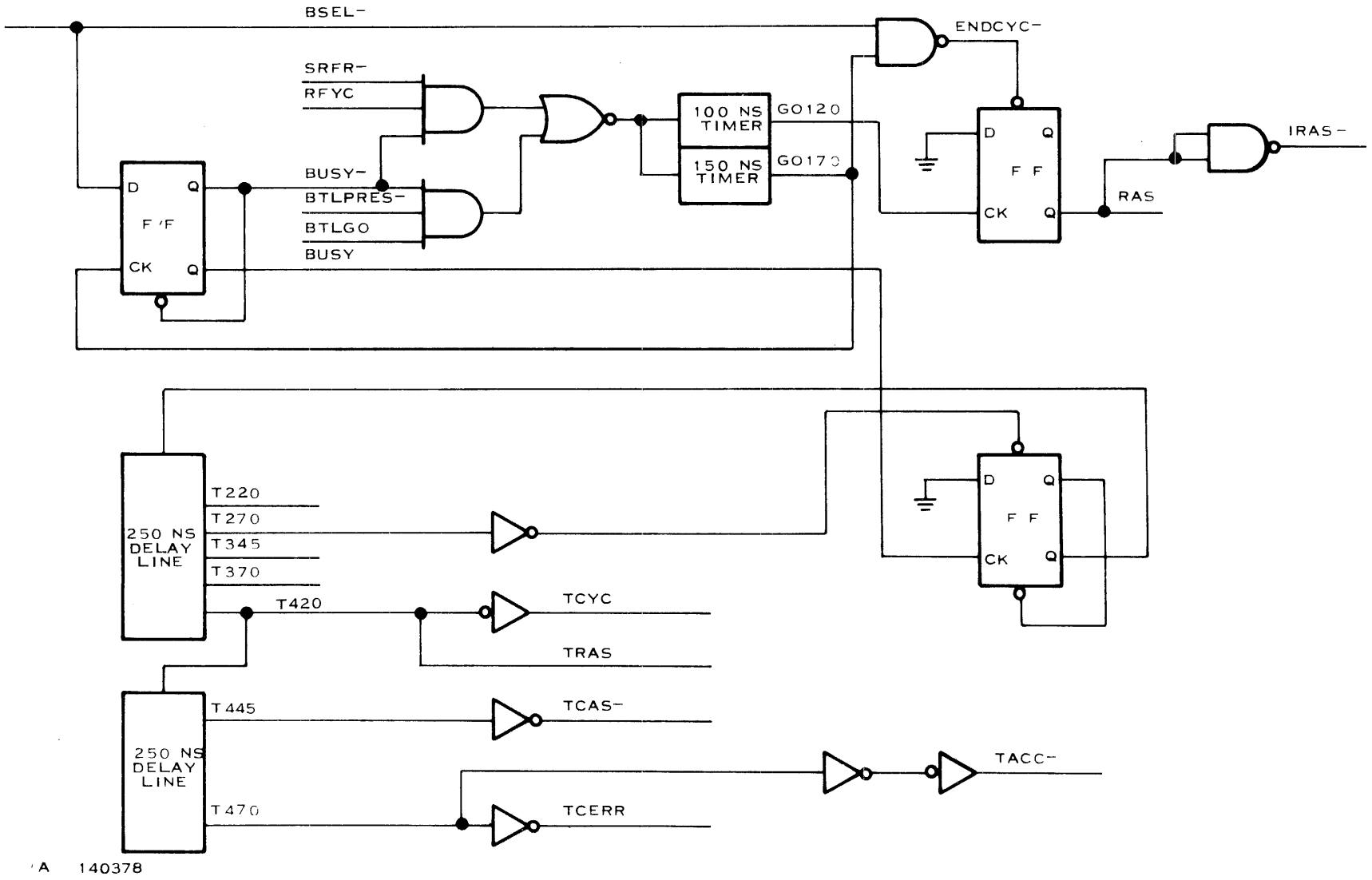


Figure 2-6. 96KB Memory Board Memory Timer Functional Diagram

delayed by 100 nanoseconds from GO170 is used to reset the flip-flop at the input to the delay line. This 100-nanosecond-wide pulse propagates down the delay lines, providing the various delayed pulses as shown in figure 2-6.

2.2.2.2 Address Examination. The TILINE address, consisting of address bits TLADR00- through TLADR19-, is presented to the 96KB memory controller at the time TILINE GO (TLGO-) is asserted by the TILINE MASTER device. The eight most significant bits, TLADR00- through TLADR07-, are applied to an adder circuit, where the starting address of the board as set by the start address switches on the board, is, in effect, subtracted, and the resultant output bits ADR00- through ADR07- are generated. With the board not busy (CADSEL- is high), address bits ADR00- through ADR05- and the output of two memory size jumpers are enabled as inputs to the board/bank address decoder. A valid address presented to the board/bank address decoder (that is a preprogrammed logic array) develops a low board selected signal, SEL-, and a high at one of the three BANK signals. At approximately 170 nanoseconds after TLGO- is asserted, and with the board selected, the GO170 output from the board timer clocks BUSY high and the memory read or write cycle operation is continued. If the address is not valid for the board or for any add-on memory board, BUSY remains low, and a high BSEL- signal ANDed with GO170 produces a low ENDCYC- to abort the cycle as previously described. Output bits of the address subtractor ADR06- and ADR07-, along with TILINE address bits TLADR08- through TLADR12- are applied as the row address inputs to the row/column address select circuit. Address bits TLADR13- through TLADR19- are the column address inputs to the row/column address select circuit. With no refresh operation in progress, the row address inputs are latched onto the memory chips in the addressed bank as the row address strobe, RAS, is clocked high by the GO120 output from the memory timer. The GO170 output from the memory timer clocks CADSEL- low, and the column address inputs to the row/column address select are selected for output to the memory chips. The T220 output from the timer clocks the column address strobe CAS high to latch the column address bits onto the memory chips in the address bank.

2.2.2.3 Memory Write Cycle. To execute a write to memory cycle, the TILINE master device asserts TLGO- and at the same time asserts the write command, TILINE READ (TLREAD), by setting both signals low. TLREAD causes the read/write input to the memory devices to go low, thereby placing the board in the write mode. The MASTER also generates valid write data on the data bus (TLDAT-) and a valid 20-bit address (TLADR-) on the address lines. The asserted TLGO- triggers the memory timer, and after 120 nanoseconds GO120 is generated to clock row address strobe (RAS) high and to also provide the row address strobe, IRAS-, for the add-on memory expansion boards. RAS is ANDed with the selected bank signal to provide a low row address strobe that latches the seven row address bits onto the selected bank of memory devices. A delayed strobe output from the memory timer GO170, is used to interrogate the results of address decoding on the 96KB memory controller and on the add-on expansion boards. With a valid address decoded, the low BSEL- clocked by GO170 generates a high BUSY signal. The high BUSY signal clocks a 100-nanoseconds wide pulse that is applied to the input of a 500-nanosecond delay line. The effect is that the delay line is activated at time T170 (nanoseconds) after TLGO- is asserted.

At time T170, the column address select signal CADSEL- is clocked low and the column address bits are selected for application to the addressed bank of memory devices. The column address strobe, CAS, is clocked high by T220 to strobe the column address bits, the 16 data bits, and the six check bits that are generated by check logic on the board into the selected memory bank. Also generated at this time is the column address strobe for add-on memory, ICAS-. For a

memory write cycle, the T345 output from the memory timer ANDed with a high READ- signal generates the TILINE terminate signal TLTM- for transmission to the TILINE interface. The time from receipt of the asserted TLGO- to the transmission of TLTM- is typically 370 nanoseconds. However, the time for a memory write cycle, the time from the beginning of a write cycle until a new memory cycle can begin, is typically 520 nanoseconds. TLGO- can be asserted by the master device before then but will be ignored until the memory busy signal is released. The positive transition of TCYC generated by the memory timer occurs at time T520 to signal the completion of the memory write cycle by changing the state of the flip-flop that generates the BUSY signal.

2.2.2.4 Memory Read Cycle. To execute a memory read cycle, the TILINE master device asserts TLGO- low and TLREAD high. TLREAD generates a high at the read/write input to the memory devices, thereby placing the memory board in the read mode.

The master also generates a valid address on the address lines. The address is decoded and interrogated, the row address strobe (RAS), column address select (CADSEL-), and the column address strobe (CAS) are generated and used in the same manner as was described for the memory write cycle. With the memory board addressed and in the read mode, the low RSEL- signal enables the 16 output data bits from the addressed memory through three-state buffers and latches. Each data bit is applied as one input to an exclusive-OR gate. Similarly, RSEL- enables six check bits to the error detect logic. RENAB-, clocked low by time T370 pulse output from the memory timer, enables the 16 data bits onto the data bus. However, data is not valid to the master device until TLTM- is asserted by the memory board. With no error detected, at time T445 the TACC output from the memory timer, ANDed with the high ERROR- signal, asserts TLTM- low. The master device accepts data as valid and releases TLGO-. A detected and correctable error generates an output from the error detect logic that is applied to the other input of the exclusive-OR gate for the data bit in error to change the sense of that data bit, thereby correcting the error. At the same time, the ERROR- signal driven low inhibits the assertion of the valid data signal, TLTM-, to the MASTER device. (After an appropriate delay to permit data correction, the positive transition of the TCERR output from the memory timer at time T520 asserts TLTM- to the master device.)

2.2.2.5 Memory Refresh Controller. A refresh of the memory cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses every two milliseconds to preserve data that is stored in the dynamic MOS memory storage cells. The refresh address lines at the output of the refresh controller replace the normal row and column address lines to refresh 1/128th of the memory during a refresh cycle. Refresh cycles are synchronized with memory requests and begin immediately following the first memory cycle that occurs after the refresh request is made. In the event that no memory requests are made before a second refresh request occurs, a refresh cycle is forced at the time of the second refresh request. When main power is removed from memory, the memory is said to be in the standby mode. While in this standby mode, only that circuitry required to maintain the integrity of the refresh controller is powered by the power supply battery. Refresh requests are generated at the same rate as when main power is on. When a refresh request occurs, the required address and control logic is switched on and the refresh cycle is executed. The address and control logic power is switched off at the completion of each single cycle. The refresh controller consists of a free-running oscillator, four flip-flops, and a binary counter. (Figure 2-7 is a simplified functional diagram of the refresh controller.) The output of the oscillator is ANDed with PWRON to generate 128 refresh clock pulses, labelled RFCLK, every two milliseconds. RFCLK clocks a high RFREQ to the inputs of refresh flip-flop 2 and the forced refresh flip-flop. If a memory cycle is

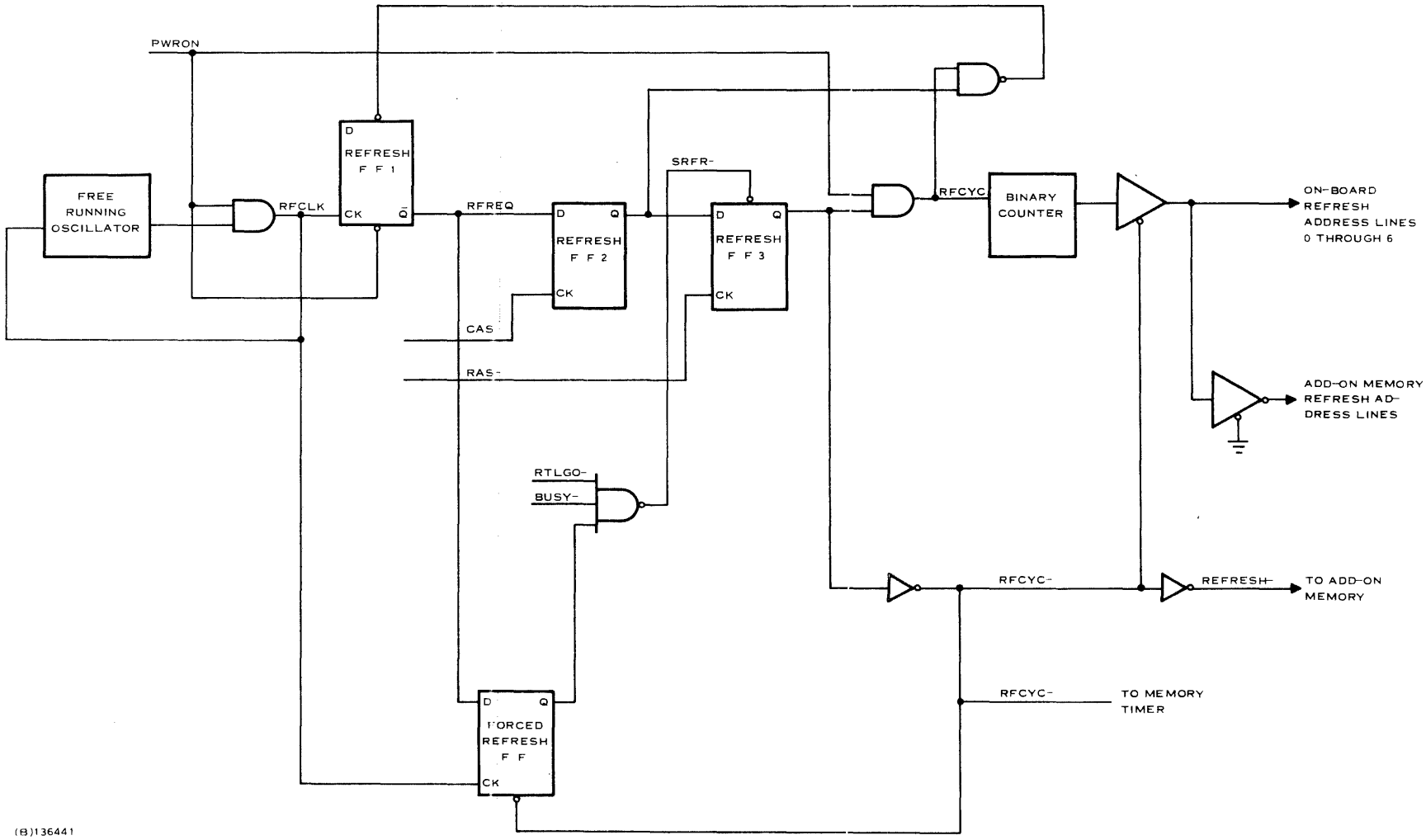


Figure 2-7. 96KB Memory Controller Refresh Logic Simplified Functional Diagram

in progress or if a memory cycle occurs before the next RFCLK pulse is issued, the column address strobe, CAS, clocks the high through to the input of refresh flip-flop 3. At the end of the memory cycle, the positive-going RAS- signal clocks the high through this flip-flop to generate the RFCYC and RFCYC- signals. RFCYC is used to increment the 128-count binary counter by one for each refresh cycle. The output of the counter is selected during a refresh cycle to address each of the 128 rows of the memory devices in turn, one row for each refresh cycle. The high RFCYC is applied at the input to the board/bank address decoder to enable all banks of memory during a refresh cycle. In the absence of normal memory cycles, CAS and RAS- are not available to clock the flip-flops in the method just described, and an alternate method of forcing refresh cycles is used. As before, the first RFCLK pulse clocks a high RFREQ to the inputs of two separate flip-flops. The flip-flop normally clocked by CAS remains static in the absence of a memory cycle, and the next RFCLK pulse generated clocks RFREQ through the forced refresh flip-flop as a high input to a NAND gate. With a memory cycle not in progress, the other two inputs to the NAND gate (RTLGO- and BUSY-) are high. The low SRFR- output of the NAND gate sets refresh flip-flop 3 to generate the RFCYC and RFCYC- signals. Since refresh flip-flop 1 is not reset by the ANDed outputs of refresh flip-flops 2 and 3, REFREQ at the input to the forced refresh flip-flop stays high, and all ensuing RFCLK pulses generate forced refresh cycles in the absence of normal memory cycles.

2.2.2.6. Error Checking and Correction. The error correction code is a modified Hamming code that allows for correction of any single-bit error and detection of any double-bit error that may occur when processing data to either on-board memory or to add-on memory array boards. A three-bit or greater number of errors causes erroneous operation of the checking logic. The gross error condition, wherein all 0s or all 1s are returned from memory, is detected as an error. During a write cycle, the 16 data bits are applied to a check bit generator that provides the six check bits, CB10 through CB15, at the same time that the data word is written into memory. The check bit generator consists of six 9-input odd/even parity generators/checkers. During a write cycle, eight data bits are applied as inputs to each of the six parity generators/checkers with the pattern shown in figure 2-8.

The six check bits generated are stored in memory along with the 16 data bits. During a read cycle, the six check bits are read out of memory as CB00- through CB05- along with

CHECK BIT \ DATA BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	X	X		X	X				X	X	X			X		
CB1	X		X	X		X	X		X			X			X	
CB2		X	X		X	X		X		X			X			X
CB3	X	X	X				X	X			X	X	X			
CB4				X	X	X	X	X						X	X	X
CB5									X	X	X	X	X	X	X	X

(A)142866

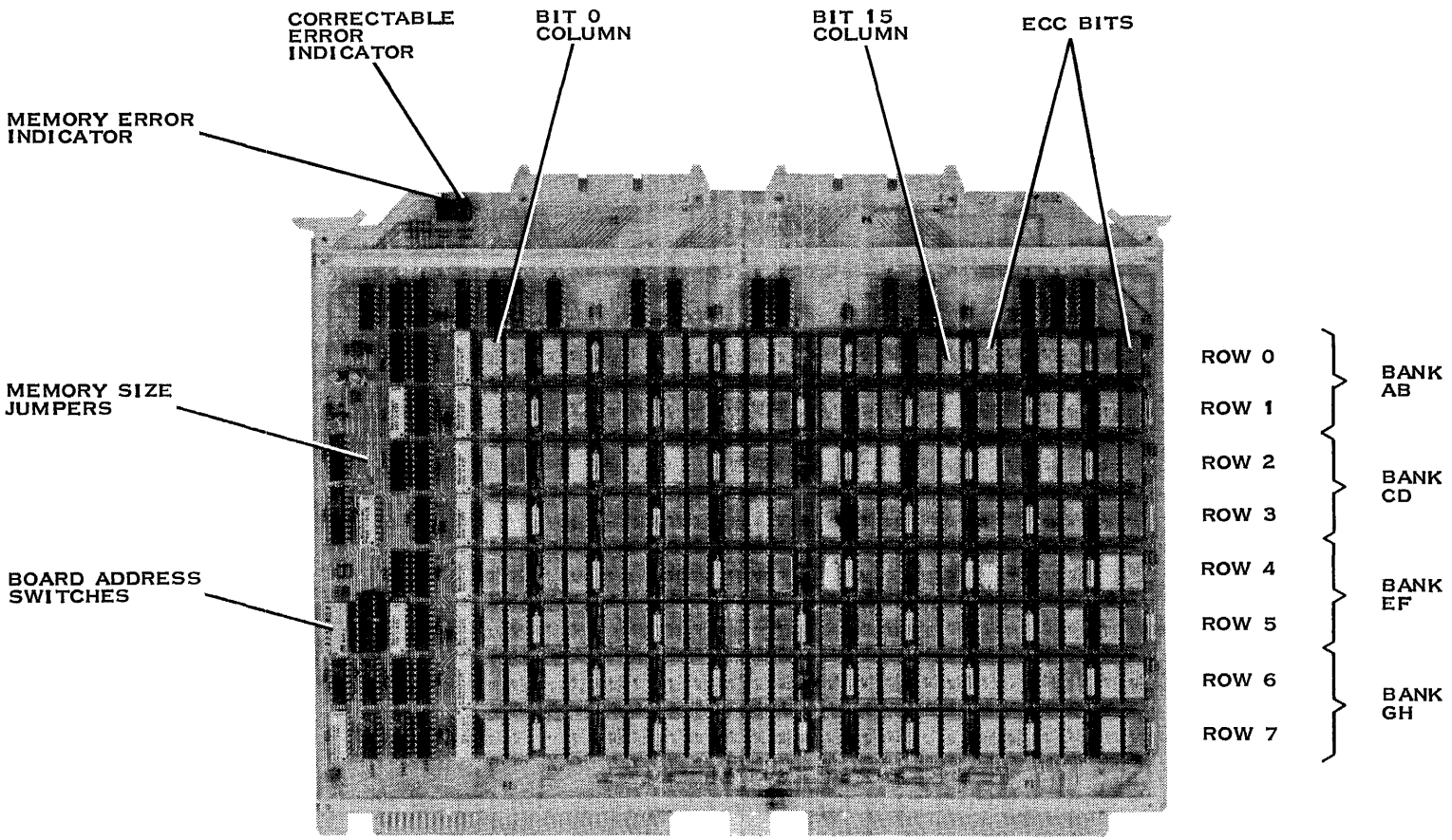
Figure 2-8. Error Correcting Code Bit Patterns

the data bits. The check bits, along with their corresponding data bits, are applied to the parity generators/checkers that are acting as 9-input devices. If the parity of all six groupings of data and check bits are correct, the assumption is made that no error has occurred. Note that the sense of two of the check bits (bits 0 and 1) is inverted to assure that the gross error condition of all 0s or all 1s is detected. If the parity of one or more of the check groups is incorrect, an error has occurred and the correction logic is enabled. The correction logic looks at the output of the six parity generators/checkers as a 6-bit code. Any single data bit error will change the sense of exactly three check bit lines and generate a code unique to that bit. The correction logic decodes this unique code, determines that the error is correctable, and inverts the specified data bit. Any single check bit error will change the sense of exactly one check bit line and generate a code unique to that bit. The correction logic will decode this unique code and pass the data with no modification. Any two data bits in error will change the sense of an even number of check bit lines and generate codes that are not unique to any given error combination. Therefore, a memory error is signaled and the data is not modified. Three or more bit errors generate codes that may indicate either no error, a correctable error, or an uncorrectable error, but in each instance an erroneous result is produced.

2.3 256KB ADD-ON MEMORY ARRAY

The 256KB add-on memory array board contains the storage elements, address decoding logic, and control and data buffers for up to 256K bytes of MOS RAM on the board. The board is used in conjunction with the 96KB memory controller (or the cache controller) to provide high-density main memory for the computer. Up to four of the 256KB add-on memory array boards may be under the control of one memory controller. The 256KB add-on memory array board interface to the TILINE consists of the TILINE address lines and power lines and is made through two 80-pin connectors at the bottom edge of the board that installs into the computer chassis. Two 50-pin connectors at the top edge of the board provide the data path and control signals interface to the 96KB memory controller. Memory on the 256KB add-on memory array board consists of from one to four banks of memory chips. Each bank consists of 2 rows of 22 memory chips (1 row for even and 1 row for odd word addresses). Double-word read and single-word write cycles are implemented for use with the cache controller.

As shown in figure 2-9, the address decoding logic and the control and data buffers for the 256KB add-on memory array board are implemented in TTL devices located on one side of the board. The eight rows (or four banks) of the TMS 4116 MOS memory devices extend across the rest of the board, with row and bank designations as shown in figure 2-9. Also installed on the board are two LED error indicators and the dual-in-line switch package used to set the starting address of the board. The two error-indicating LEDs indicate that a one-bit (correctable) error or a multibit (uncorrectable) error has occurred on this board. These indicators are set on the first occurrence of the respective error stimulant and remain set until the system is powered down or until an I/O Reset instruction is issued. The dual-in-line switch consists of eight single-pole, single-throw switches. The address switches correspond to the eight most significant bits of the 20-bit TILINE address and permit board starting address selection in 8K-byte increments. Switch 1 is the most significant bit of the address and switch 8 is the least significant bit. To set the starting address switch settings for the 256KB add-on board, use the switch settings provided for the 96KB memory controller (table 2-4). The memory capacity may be set in increments of from one to four banks of memory. Since each bank of memory represents 64K bytes of memory, the memory capacity available is either 64K, 128K, 192K, or 256K bytes. Memory size is set by connecting jumpers across the terminals of E9 and E10 as shown in table 2-8.



(A)141700

Figure 2-9. 256KB Add-On Memory Array Board Component Location

The description that follows is keyed to the functional block diagram for the 256KB add-on memory array board, figure 2-10.

2.3.1 Examination of Address

TILINE address bits TLADR00- through TLADR18- are presented to the 256KB add-on memory board at the same time that TLGO- is asserted to the memory controller. The eight most significant bits, TLADR00- through TLADR07-, are applied to an address adder circuit on the 256KB add-on memory board, where the starting address of the board as set by the starting address switches on the board is in effect subtracted. The resultant output address bits, ADR00- through ADR07-, are generated as the sum of this subtraction. With the board not busy, CADSEL- is high and address bits ADR00- through ADR04- are enabled as inputs to the board/bank address decoder. A valid address presented to the board/bank address decoder develops a low board selected signal, SEL-, and a high at one of four BANK signals.

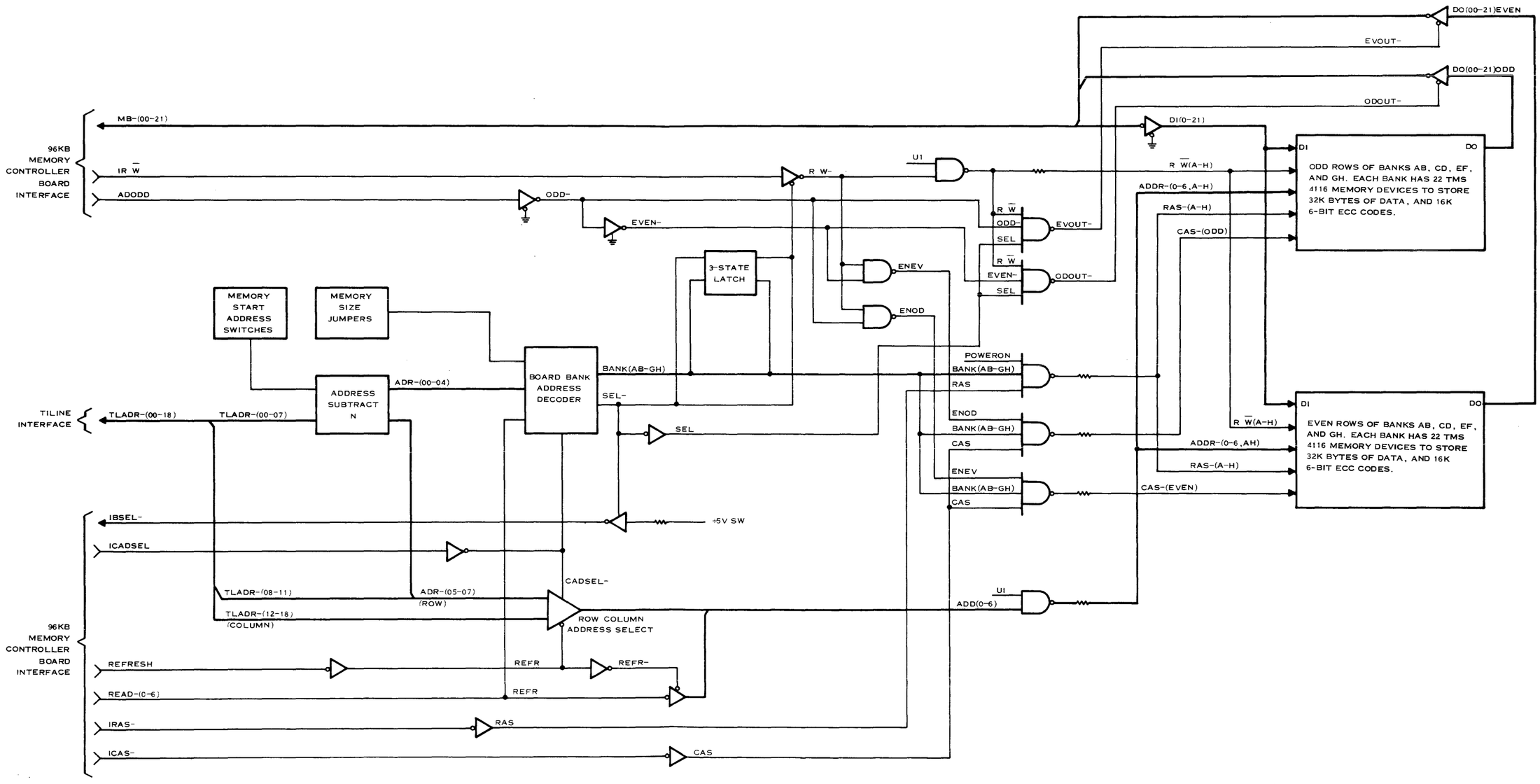
The SEL- enables a low IBSEL- interface signal to notify the memory controller that a valid address has been decoded and the memory read or write cycle is continued as described in the theory of operation for the memory controller. Output bits of the address subtractor ADR05- through ADR07- and TILINE address bits TLADR08- through TLADR11- are applied as the row address inputs to the row/column address select circuit. Address bits TLADR12- through TLADR18- are the column address inputs to the row/column address select circuit. With no refresh operation in progress, the row address strobe from the memory controller, IRAS-, is clocked low at time T120. At time T170, ICADSEL from the memory controller changes state, and the column address inputs to the row/column address select circuit are selected for output to the memory chips. Then at time T220, the column address strobe from the memory controller, ICAS-, changes state to latch the column address bits onto the memory chips in the addressed bank.

2.3.2 Write Cycle

To execute a write memory cycle, the TILINE master device asserts TLGO- and at the same time asserts the write command TILINE READ (TLREAD) by setting both signals low. The master also generates valid write data on the data bus (TLDAT-) and a valid 20-bit address (TLADR-) on the address lines. The memory interface circuits on the 96KB memory controller receive the TLGO- as the 256KB add-on-memory board decodes the address to determine if the address is valid for that board (as set on the memory start address switches and memory size jumpers). The asserted TLGO- triggers the memory timer on the memory controller that produces a delayed strobe to interrogate the results of the address decoder. If no valid ad-

Table 2-8. Memory Size Jumpers for 256KB Add-On Memory Array Board

Memory Size (Bytes)	Jumper E9	Jumper E10
64K	OFF	ON
128K	ON	OFF
192K	ON	ON
256K	OFF	OFF



(D)136442A

Figure 2-10. 256KB Add-On Memory Array Board Block Diagram

dress is decoded on the memory controller or on any 256KB add-on memory board, a cancel signal is produced that aborts the cycle. When a valid address is decoded on the 256KB add-on memory, the memory timer on the memory controller generates the following interface signals to the 256KB add-on memory board in this sequence:

- Row address strobe (IRAS-) to strobe seven address bits into the selected memory banks
- Column address select (ICADSEL) to select the second set of seven address bits
- Column address strobe (ICAS-) to strobe the second set of address bits, the 16 data bits, and the six check bits generated by the memory controller check logic in the selected memory bank. The memory timer also generates the TILINE terminate (TLTM-) to the TILINE bus.

The data word is steered to either the odd or even row of the selected bank by the ADODD signal that is generated by the memory controller from the least significant TILINE address bit, TLADR19-. The time from receipt of TLGO- to transmission of TLTM- is typically 370 nanoseconds.

2.3.3 Read Cycle

To execute a memory read cycle, the TILINE master device asserts TLGO- low and TLREAD high. The master also generates a valid address on the address lines. The address is decoded and interrogated. The row address strobe (RAS-), column address select (ICADSEL), and the column address strobe (ICAS-) are generated and used in the same manner described for the memory write cycle. Both the odd and even rows of the selected bank are accessed. The data word that is returned to the memory controller is specified by the ADODD control line as it generates either of two enabling signals, EVOUT- or ODOUT-. This line may be toggled after the first data word has been latched to provide the alternate word for cache storage. The odd-even words are contiguously addressed, with the odd word always being the next higher word addressed. The time from receipt of TLGO- to transmission of TLTM- is typically 520 nanoseconds if no error is detected in the data accessed from memory, and 620 nanoseconds if an error is detected and error correction logic is enabled. If the correction logic on the memory controller determines that the error is not correctable, the accessed data is not modified and TILINE memory error (TLMER-) is asserted in addition to TLTM-.

2.3.4 Refresh Cycle

Refresh timing for the 256KB add-on memory is controlled by the 96KB or cache memory controller that must produce 128 refresh cycles for each refresh period. For each refresh cycle, the memory controller provides the refresh address (RFAD0 through RFAD6), the REFRESH signal, and the row address strobe (IRAS-). The REFRESH signal applied to the board/bank address decoder on the 256KB add-on memory board, in turn generates the board-selected IBSEL- signal that is sent to the memory controller. All the memory banks on the memory array are refreshed simultaneously. While in standby mode, only the circuitry required to maintain the integrity of the refresh logic is powered by the power supply battery. Refresh requests are generated at the same rate as when main power is on. When a request occurs, the required address and control logic is switched on and the cycle is executed. The address and control logic is switched off at the completion of each single cycle.

2.4 CACHE CONTROLLER

The cache controller is a multilayered printed circuit board that contains all memory control logic as well as the storage elements for 64K bytes of primary memory and 2K bytes of cache memory, and the control logic for up to 1M bytes of additional memory on associated add-on memory expansion

boards. The cache controller uses a cache technique to improve the effective operating speed of primary memory. Under the cache concept, frequently used data is copied from the relatively slow primary memory into a small, fast cache memory. Subsequent calls to data residing in the cache can be honored many times faster than data from primary memory. The cache controller interface to the TILINE bus is made through the two 80-pin connectors at the bottom edge of the board that installs into the chassis slot. Two 50-pin connectors at the top edge of the board are used to interface with expanded memory.

As was true for the 96KB memory controller, up to four of the 256KB add-on memory array boards may be controlled by the cache controller. Cycle control and refresh control for the add-on array boards are provided by the cache controller but the add-on boards interface directly with the TILINE for address selection.

The cache controller circuits, including the ECC circuits, are implemented in TTL devices on the lower half of the board, as shown in figure 2-11. The 64K bytes of on-board MOS primary memory consist of two rows of TMS 4116 devices across the top of the board. Each row includes the 22 devices required for the storage of 16 data bits and the 6 error checking bits. The TMS 4116 chip is organized as 16,384 one-bit words housed in a 16-pin, dual-in-line package. The chip is based on N-channel silicon gate technology, and the inputs and outputs are TTL compatible. The 2K bytes of cache memory consist of two banks of memory devices grouped in the center of the board's lower edge. Each bank includes the 14 devices required for the storage of the 16 data bits, 2 data parity bits, a data error bit, 11 address bits, 2 address parity bits, and a validity bit. The memory device is organized as 256 4-bit words in an isoplanar TTL, 22-pin, dual-in-line package. The device has a typical read access time of 30 nanoseconds and has three-state outputs.

As shown in figure 2-12, the cache controller includes 3 LED error indicators, 11 LED chip failure indicators, and an LED HIT indicator. The 3 error-indicating LEDs are dedicated to the following functions:

- To indicate that a single-bit, correctable primary memory error has been detected and corrected (CERR).
- To indicate that a multibit, uncorrectable primary memory error has been detected and placed on the data bus unmodified (MERR).
- To indicate that a parity error has occurred in either the cache data or the cache data address. The requested word is provided from primary memory instead of cache (CAER).

The error-indicating LEDs are set on the first occurrence of an error stimulant and remain set until the board is powered down or until a RSET instruction is issued.

The additional eleven chip-failure indicators pinpoint the memory chip that caused the first single-bit error and are divided into two groups, as shown in figure 2-12. A group of five indicators form a binary code that identifies the bit that failed. The remaining six LEDs form a binary code that identifies the row that contains the failing chip. Additional errors do not affect these indicators but are recorded by the two error indicators located on the add-on memory expansion board where the error occurred.

The HIT indicator lights whenever the addressed word in a memory read or write operation resides in cache memory. Table 2-9 summarizes the indicators and their functions.

Each of the dual-in-line switches consists of eight single-pole, single-throw, push-type switches. As shown in figure 2-11, one switch package is used to set the cache controller's on-board memory starting address. The other package selects the TPCS address of the board.

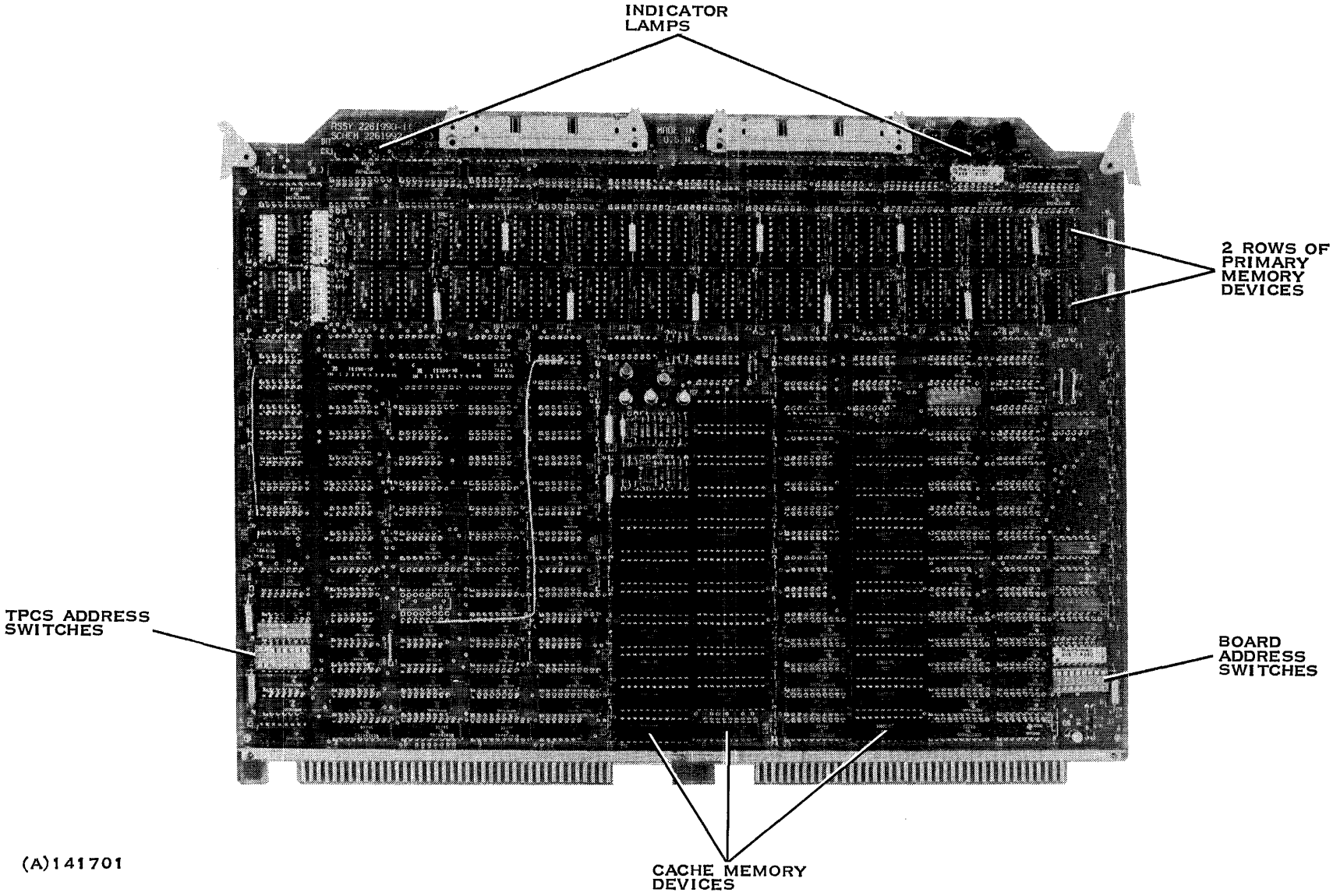
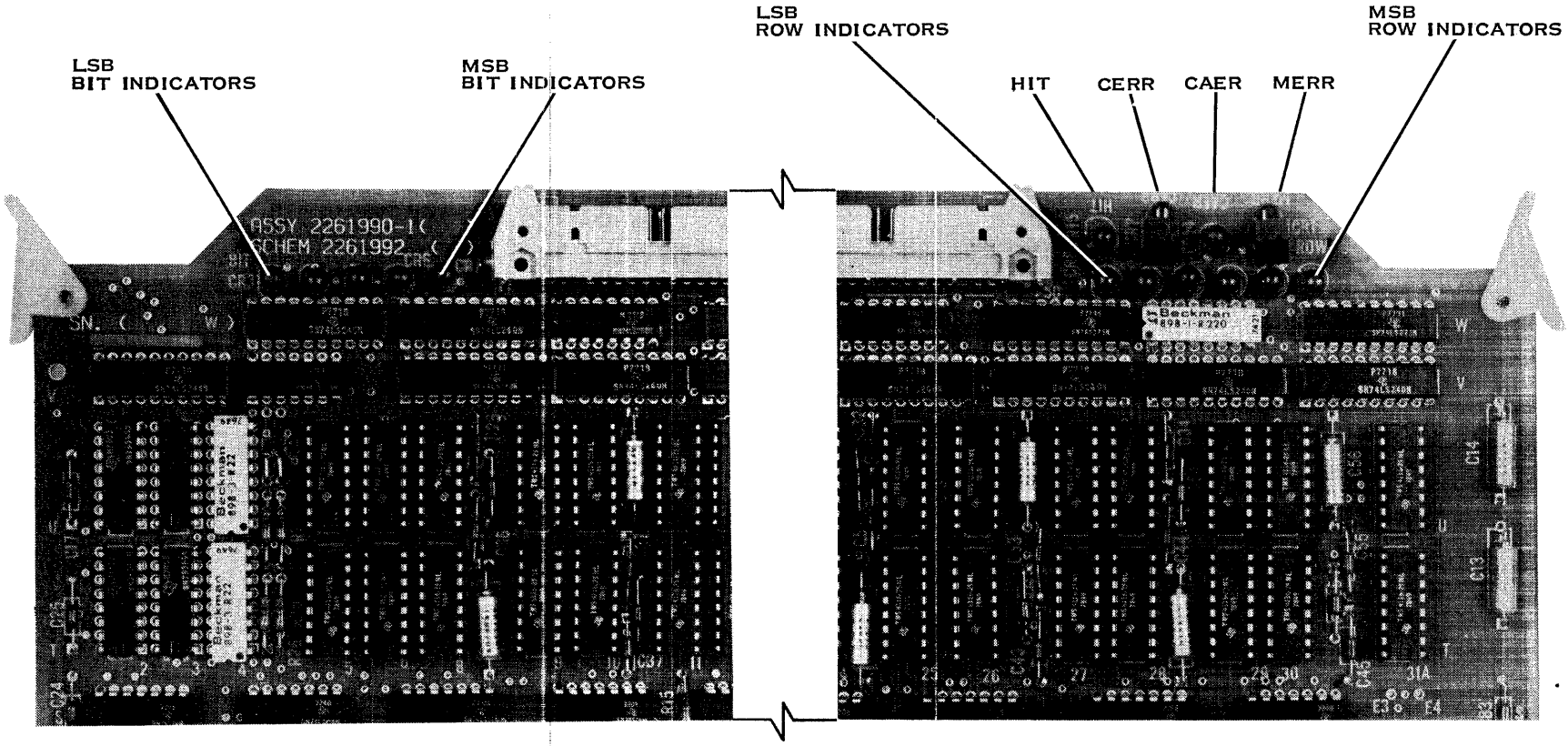


Figure 2-11. Cache Controller Memory Board Component Location



(A)141632

Figure 2-12. Cache Controller Indicators

The memory starting address switches correspond to the eight most significant bits of the 20-bit TILINE address and permit board starting address selection in 8K-byte increments. Switch 1 is the most significant bit of the address, and switch 8 is the least significant bit. Operation of these address switches is identical to those of the 96KB memory controller. The required switch settings for the cache controller are the same as those for the 96KB memory controller (see table 2-4). Addresses other than those shown can be represented in a similar manner by using the eight switches to establish the binary number.

The diagnostic mode pencil switches correspond to address bits 11 through 18 of the 20-bit TILINE address bus and select the TPCS address that is used to operate the controller in the diagnostic mode. Switch 1 is the most significant bit of the address, and switch 8 is the least significant bit. This permits the selection of 512 addresses that fall between $F800_{16}$ and $FBFE_{16}$, inclusive, in the 15-bit address form. The 20-bit address is generated in the address development process. Table 2-6 lists several examples of TPCS addresses and their corresponding switch settings. These settings are operated identically for the cache controller. The recommended TPCS addresses for cache controllers are shown in table 2-10. Software provided by Texas Instruments expects these values to be used.

2.4.1 Cache Operation

The cache controller makes the primary memory appear to operate faster by storing copies of often-used memory word pairs in a small, fast-access memory. The cache controller stores in cache the contents of the last 512 odd/even memory word pairs requested by a TILINE master device. An odd memory word is a word with an address in which the least significant bit is one. An even memory word is a word with an address in which the least significant bit is zero. A pair

Table 2-9. Description of Cache Controller Indicators

Indicator	Function
HIT	Indicates that the addressed word in a read or write operation resides in cache memory.
ROW	These six LEDs indicate in hexadecimal the row that sustained a data recovery error. Refer to table 2.3.
BIT	These five LEDs indicate in hexadecimal the bit determined to be in error. Refer to table 2-3.
CAER	An uncorrectable cache error has occurred.
CERR	A correctable primary memory data error has occurred.
MERR	An uncorrectable primary memory data error has occurred.

of data words whose addresses are identical except for the sense of the least significant bit is called an odd/even word pair. When a primary memory word is requested by the TILINE master device, the cache logic searches the collection of data words in the fast memory (cache memory) to see if the requested word is present. If the requested word is not present, the cache logic adds the new word to the cache memory along with the other member of the odd/even word pair. With the cache option enabled, any of the following possibilities may occur during a read or write operation.

- A valid memory address is decoded but is not present in the cache memory. If the memory operation is a read operation, the requested word and the other member of the odd/even pair are fetched from primary memory and copied to the cache memory. If the memory operation is a write operation, the specified word is updated in primary memory only and no action is taken by the cache controller to add this word to the cache memory.

- A valid memory address is decoded and is present in the cache memory. If the memory operation is a read operation, the requested word is copied from the cache memory to the TILINE data bus. If the memory operation is a write operation, both the cache memory and the primary memory are updated.

- A nonvalid memory address is found on the TILINE address bus. The cache controller takes no action and the TILINE is relinquished after a specified timeout period.

- The cache controller board is busy with either a memory refresh cycle or a memory cycle with another master device. The master device encountering the busy indication must wait for the cache controller board to become free.

The cache for the cache controller is enabled via the TPCS write word addressed to the cache controller. Addressing the cache controller's selected TPCS in a write operation with bit 9 of the word low, enables the cache. Similarly, setting this bit high disables the cache option and the board functions as a primary controller only.

The cache controller is equipped with error

Table 2-10. Recommended TPCS Settings for One or More Cache Controllers

CPU Address	TILINE Address	Module
FB10 (Switches 1, 2, and 6 ON)	FFD88	1st Cache Controller
FB14 (Switches 1, 2, 6, and 8 ON)	FFD8A	2nd Cache Controller
FB18	FFD8C	3rd Cache Controller*
.	.	.
.	.	.
.	.	.

Note:

*Additional controllers placed every four bytes (CPU address).

detection and correction circuits that generate error prevention data. The error prevention information is stored with other cache data as shown in figure 2-13. When the cache controller board is powered up or when an instruction is issued through the TPCS, an initialization sequence is executed on the cache controller. Initialization consists of setting all validity bits low and clearing all error logic. Validity bits are then generated and stored with all cached data word addresses. The sense of the validity bit is high when the cache is operating normally and low during intialization or when an error condition occurs. When a data word is fetched from the cache memory, the validity bit is checked along with the associated parity bits. If the validity bit is high, the fetched data word is treated normally. If the sense of the validity bit is low, the cache version of the requested word is discarded and the fetch is made from primary memory instead.

2.4.2 Cache Memory Control and Operation

The cache memory controller monitors the TILINE, decodes addresses on the TILINE address bus, and directs the performance of read and write cycles to addressed memory under control of a TILINE master device. This addressed memory can be on the cache memory controller board or located on add-on expansion boards. Figure 2-14 shows the data flow for the cache memory controller. The following functional description is keyed to the block diagram for the cache memory controller, figure 2-15, and to the logic diagram for the board, found in section 4.

2.4.2.1 Cache Memory Board Timer. Pulses used to control the timing and sequence of operations during memory read and write operations are provided by the memory timer. This includes timing for the memory refresh cycle that is in itself a memory read operation. The memory timer consists of two resistance/capacitance (R/C) timers, a 20-nanosecond delay line, a 30-nanosecond delay line, and two 250-nanosecond delay lines, along with associated TTL logic. Each 250-nanosecond delay line has 10 output taps that are separated from each other in time by 25 nanoseconds. An input signal to the delay line is propagated down the line and is reproduced at each output tap, with each progressive tap introducing an additional 25 nanoseconds of delay to the input signal. The delayed-by-250-nanoseconds output of the first delay line is the input to the second 250-nanoseconds delay line, providing a total delay of 500 nanoseconds.

Reference is made to the simplified functional diagram for the memory timer (figure 2-16) in the following description of the operation of the timer for a normal, primary memory cycle.

When the cache memory board is not busy with a previous memory operation or a refresh operation, the asserted TLGO- from the master device provides a high BTLGO to trigger one of the RC timers, which, in turn, generates a GO110 pulse at approximately 110 nanoseconds after the asserted TLGO-. GO110 clocks a flip-flop to generate the row address strobe for both on-board use and add-on memory expansion board use. The on-board row address strobe (RAS) is also applied to a 30-nanoseconds delay circuit that provides a GO150 signal at its output. With either the cache controller or an add-on memory board addressed, the low board selected signal, BSEL-, is clocked by GO150 to send the BUSY signal high. If neither local memory nor add-on memory is addressed, GO150 and the high BSEL- and BUSY- signals produce the low ENDCYC- to abort the cycle. Assuming a valid address is presented to the local memory or to an add-on memory expansion board, as BUSY goes high (at time T150 after TLGO- is asserted) a high pulse is clocked into the input of the first of two delay lines. At the time T250 output of the first delay line, the delayed-by-100-nanoseconds pulse is used to reset the flip-flop at the input to the delay line. This sets the width of the input pulse to the delay line at 100 nanoseconds. The 100-nanosecond pulse propagates down the delay lines, providing the various delayed pulses at outputs of the delay lines, as shown in figure 2-16.

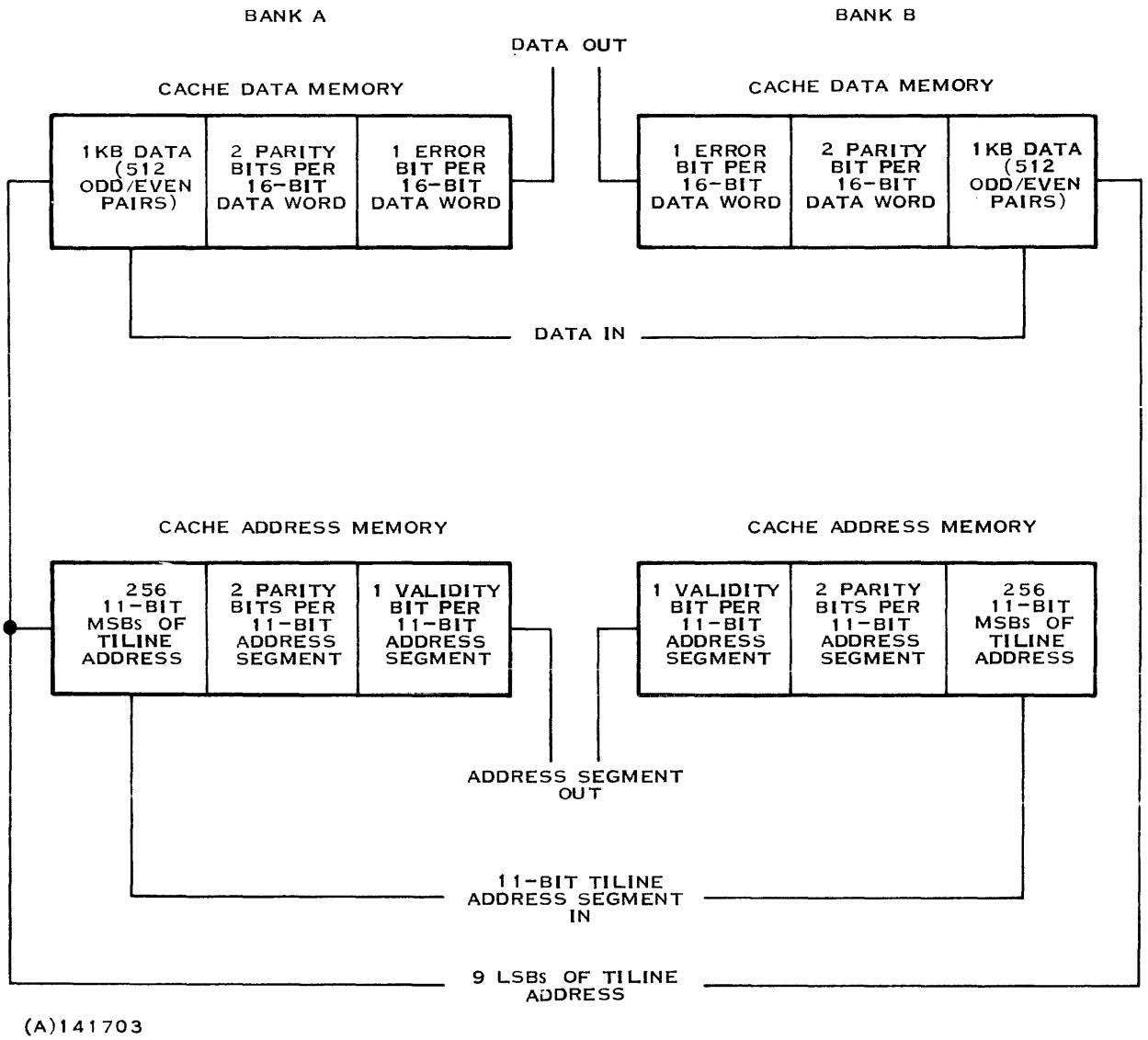
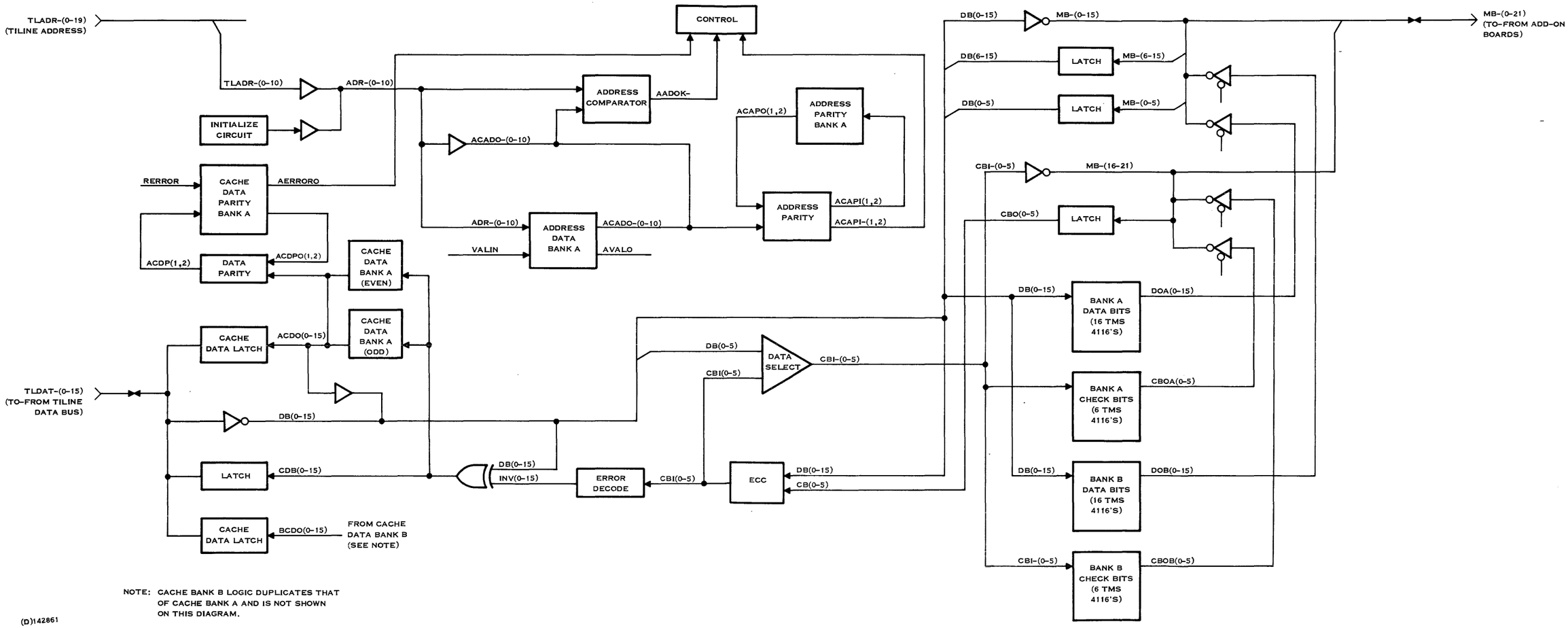


Figure 2-13. Organization of Cache Data



NOTE: CACHE BANK B LOGIC DUPLICATES THAT OF CACHE BANK A AND IS NOT SHOWN ON THIS DIAGRAM.

(D)142861

Figure 2-14. Cache Controller Data Flow Block Diagram

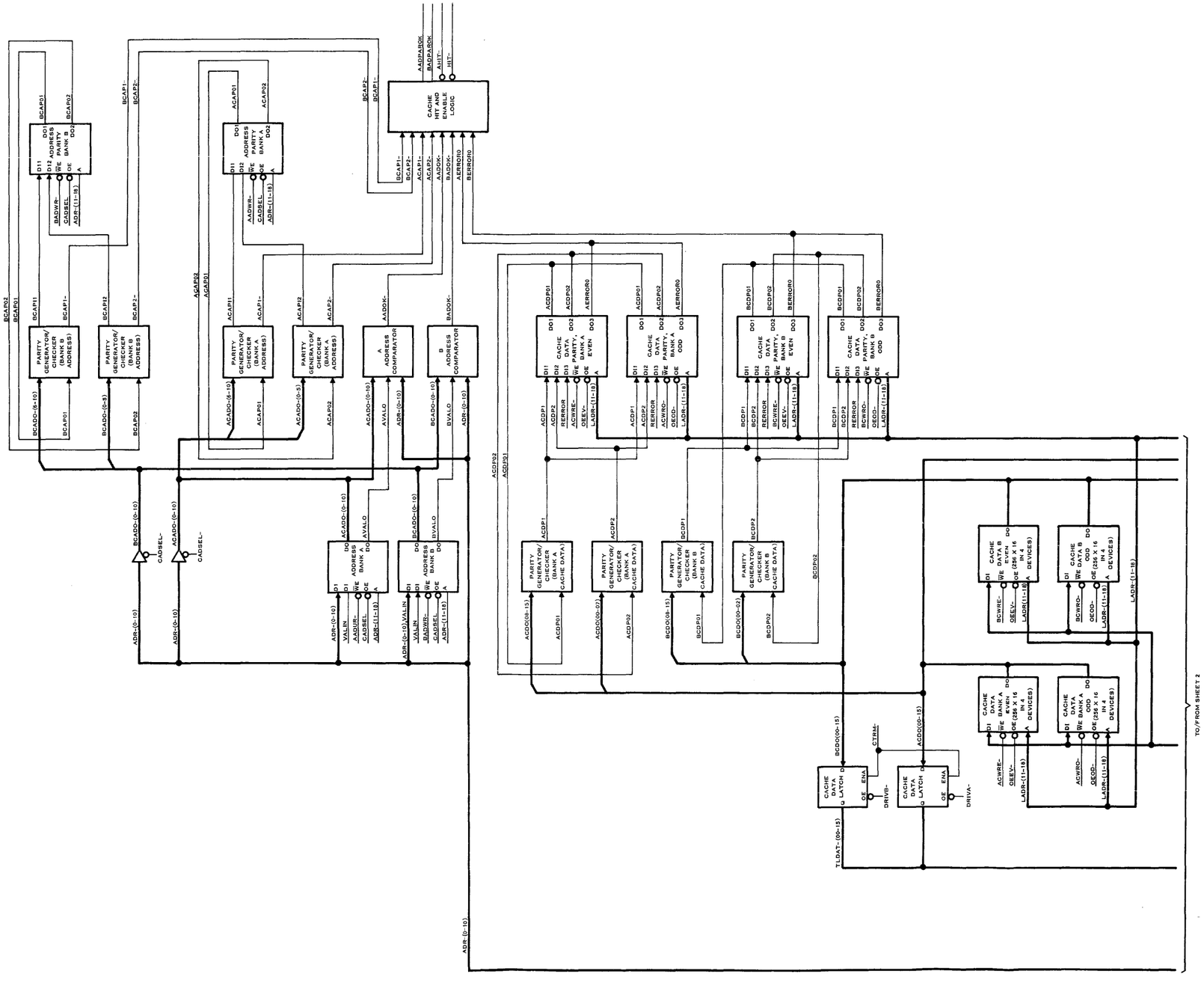


Figure 2-15. Cache Controller Block Diagram (Sheet 1 of 2)

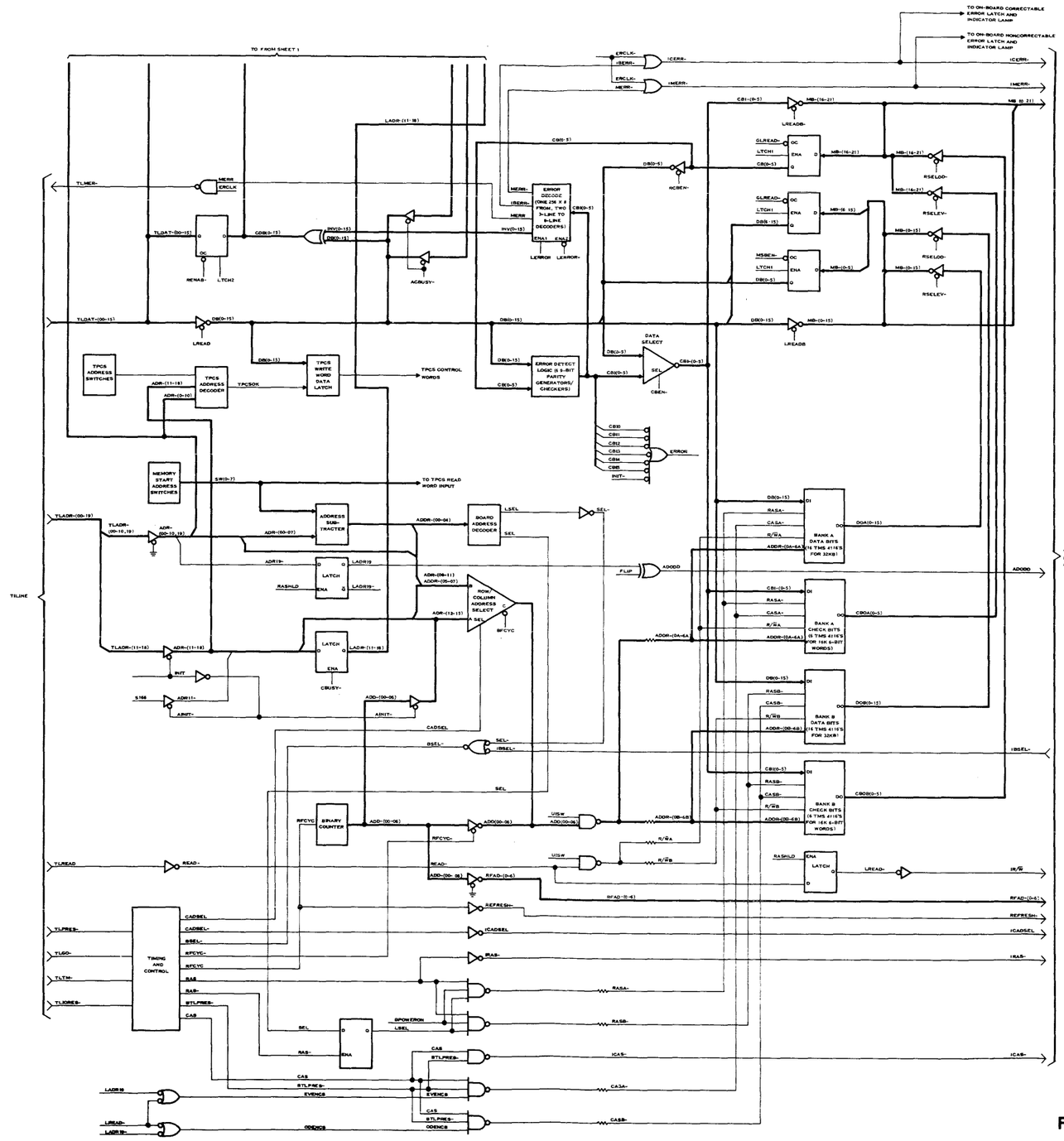
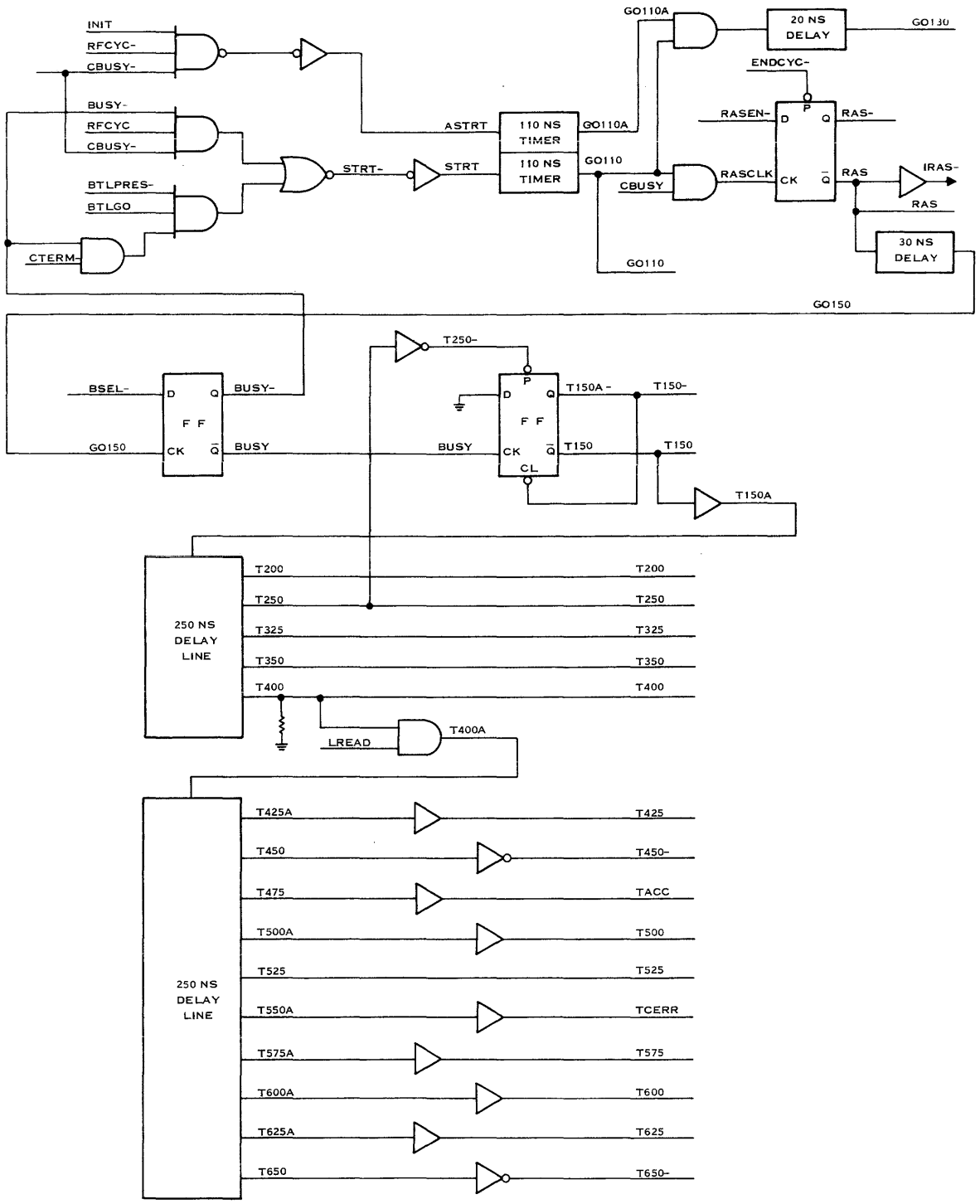


Figure 2-15. Cache Controller Block Diagram (Sheet 2 of 2)



(C)142862

Figure 2-16. Cache Controller Memory Timer Functional Diagram

An alternate 110-nanosecond timer is used to guarantee that the GO110 signal does not occur until 110 nanoseconds after TLGO- is asserted or 110 nanoseconds have elapsed since the board was busy with either a refresh cycle, an initialization cycle, or a cache storage operation.

The GO110A pulse is synchronized with the GO110 output of the other RC timer by applying the two signals to an AND gate. The output of the AND gate, delayed by 20 nanoseconds, provides the GO130 signal that is used in the timing of cache operations.

2.4.2.2 Primary Memory Address Examination. The TILINE address, consisting of address bits TLADR00- through TLADR19-, is presented to the cache memory controller board at the time TILINE GO (TLGO-) is asserted by the TILINE master device. As shown in figure 2-15, the eight most significant bits of the address, ADR00- through ADR07-, are applied to address comparison logic. In the address comparison logic, the board start address, as set by the start address switches, is subtracted from the eight most significant bits of the TILINE address to generate resultant output address bits ADDR00- through ADDR07-. When the cache controller is addressed, address bits ADDR-(00-04) provide an SEL signal that is latched at the output of a bistable latch as signals LSEL and LSEL-. The LSEL signal generates a low BSEL- signal that is applied as the D-input to a flip-flop (see figure 2-15). At approximately 150 nanoseconds after TLGO- is asserted, the GO150 output from the board memory timer clocks BUSY high and the memory read or write operation is continued. If the address is not valid for the board or for any add-on memory board, BUSY remains low and the high BSEL- signal, ANDed with high signals GO150 and BUSY-, produce a low ENDCYC- to abort the cycle.

Buffered TILINE address bits ADR12- through ADR18- are applied as the row address inputs to the row/column address select circuit. Output bits of the address subtracter, ADDR05- through ADDR07- along with buffered TILINE address bits ADR08- through ADR11- are applied as the column address inputs to the row/column adress select circuit. With no refresh operation in progress, the row address inputs are latched onto the primary memory chips as the row address strobe, RAS, is clocked high by the GO110 output from the memory timer. The time T150 output from the memory timer clocks CADSEL high and the column address inputs to the row/column address select circuit are selected for output to the memory chips address lines. The time T200 output from the memory timer clocks the column address strobe, CAS, high to latch the column address bits onto the memory chips.

2.4.2.3 Memory Write Cycle. To execute a write to memory cycle, the TILINE master device asserts TLGO- low and at the same time asserts the write command by setting TLREAD low. TLREAD causes the read/write input to the primary memory devices to go low, thereby placing the memory board in the write mode. The master also generates valid write data on the data bus (TLDAT-) along with a 20-bit TILINE address on the address lines. The memory board interface logic receives the TLGO- transmitted from the master device and decodes the address to determine if the cache memory controller board is addressed. The cache logic also begins to determine if the addressed word resides in the cache memory. A valid 20-bit address (TLADR-) on the address lines provides a high latched board selected signal (LSEL). If a valid address is not decoded, an ENDCYC- signal is generated that aborts the cycle. If a valid address is decoded and the address is also found to reside in cache, a cache present signal is generated at the output of the address comparator of the cache bank addressed. The cache address present signal generates a high cache busy signal that causes the TILINE data bits, 2 data parity bits, 1 data error bit, the 11 most significant address bits, a validity bit, and 2 address parity bits to be stored in cache memory. Cache memory storage occurs at time T250 of the memory cycle.

The TILINE data bits are also written into primary memory as follows. At approximately 110 nanoseconds after the asserted TLGO-, GO110 clocks the row address strobe (RAS) high and also provides the row address strobe (IRAS-) for add-on memory expansion boards. RAS is ANDed with the latched board selected signal (LSEL) to provide a low row address strobe that latches the seven row address bits onto the primary memory devices address lines. With signal CADSEL low at this time, the A-input to the row/column address select logic, address bits ADR12- through ADR18-, is selected to provide the seven row address bits for application to the memory device address lines.

At time T150, column address select signal CADSEL is clocked high and the column address bits are selected for application to the address lines of the memory devices. The column address strobe, CAS, is clocked high by T200 to strobe the column address bits, the 16 data bits, and the 6 check bits that are generated by check logic on the board into the memory devices. Also generated at this time is the column address strobe for add-on memory, ICAS-. For a memory write cycle, the T325 output from the memory timer, ANDed with a high READ- signal, generates the TILINE terminal signal TLTM- for transmission to the TILINE interface.

The time from the receipt of TLGO- to the transmission of TLTM- to the memory interface circuits is typically 350 nanoseconds. The write cycle time of the memory, which is the time from the beginning of a write cycle until the next memory cycle can begin, is typically 450 nanoseconds. When the TILINE master device receives the asserted TLTM- from the memory controller, it must release TLGO-, TLREAD, and the address and write data. When the memory receives the release of TLGO-, it must release TLTM-. The positive transition of the cycle complete signal, C/CMP, clocked high at T450, signals the completion of the memory write cycle by changing the state of the flip-flop that generates the BUSY signal.

If a valid address is decoded for the memory controller but that address does not also reside in cache, the memory write cycle to the primary memory devices occurs as just described, but no action occurs in the cache memory.

2.4.2.4 Memory Read Cycle. A memory read cycle occurs in the cache memory controller under different conditions. These conditions and the actions taken by the cache memory controller under the various conditions are summarized in example 1 that follows.

EXAMPLE 1

Condition	Action Taken
The cache is not enabled.	The requested word is provided to the master device from primary memory, whether or not the requested word resides in cache, and no cache action occurs.
The cache is enabled and the requested word resides in cache.	The requested word is provided to the master device from the cache.
The cache is enabled and the requested word does not reside in cache.	The requested word is provided to the master device from primary memory and a copy of the requested word is written into cache.

A memory read cycle with the cache not enabled is made from primary memory as follows. The TILINE master device asserts TLGO- low and TLREAD high. TLREAD generates a high at the read/write input to the primary memory devices, thereby placing the memory board in the read mode. The master device also generates a valid address on the address lines. The address is decoded and interrogated, and the row address strobe (RAS), column address select (CADSEL), and column address strobe (CAS) are generated in the manner that was described for the memory write cycle. With the memory board addressed and in the read mode, the low RSELEV- or RSELOD- signal enables the 16 output data bits from bank A (or row 0) or bank B (or row 1) through three-state buffers and latches. Each data bit is applied as one input to an exclusive-OR gate. Similarly, RSELEV- or RSELOD- enables six check bits to the error detect logic. RENAB-, clocked low by the time T350 pulse output from the memory timer, enables the 16 data bits onto the TILINE data bus. However, data is not valid to the master device until TLTM- is asserted by the memory board. With no error detected, at time T475 the TACC output from the memory timer, ANDed with the high ERROR- signal, asserts TLTM- low. The master device accepts data as valid and releases TLGO-. A detected and correctable error generates an output from the error detect logic. The output is applied to the other input of the exclusive-OR gate for the data bit in error, to change the sense of that data bit, thereby correcting the error. At the same time, the ERROR- signal driven low inhibits the assertion of the valid data signal, TLTM-, to the master device. After an appropriate delay to permit data correction, the time T600 pulse output from the memory timer clocks TERM high, and TLTM- is asserted to the master device.

A memory read cycle with the cache enabled and with the requested word residing in cache memory, occurs as follows. The master device asserts TLGO- and at the same time asserts TILINE READ high. A valid 20-bit address is presented on the TILINE address bus. The asserted TLGO- causes the board address to be decoded. It also causes the cache circuits to compare the TILINE address to the cached data addresses to determine if the requested word resides in cache. A delayed-by-110-nanoseconds strobe interrogates both the cache address search logic and the TILINE address decode logic. If the requested word is present in the cache, that is, if an address match occurs in one of the cache banks, an ADDRESS OK (AADOK- or BADOK-) signal is generated. These signals, AADOK- and BADOK-, are ORed together to stop the primary memory timing cycle (by not allowing RAS) and to enable data onto the TILINE via the drive signals, DRIVA- or DRIVB-.

If the cache address parity and the cache data parity are both good and the requested word in cache was stored without error, a low AHIT- signal is generated. At time T130, AHIT- is clocked through a flip-flop to generate a high CTERM signal. CTERM is used to continue to generate either a low DRIVA- (A bank addressed) or a low DRIVB- (B bank addressed) signal. At the same time, CTERM causes TLTM- to go low to indicate that valid data is on the data bus. The asserted TLTM- signals the end of the memory read cycle. The row address strobe logic is inhibited during a read from cache memory. Early completion of the cache memory cycle prevents the generation of the other signals that are applicable to a memory read from primary memory.

A memory read cycle with the cache enabled and with the requested word not residing in cache, occurs as follows. The read from the primary memory devices occurs in the same manner as was described for a memory read cycle with the cache not enabled. In addition to the read from the primary memory devices, the least recently used bank of cache is updated with the requested word and its odd/even pair. The cache storage of the primary memory words occurs in two phases. The first word of the odd/even pair is stored after the check bit comparison has been made on the requested primary word

(approximately coincident with the TLTM- signal). At time T500, output signals from the memory timer generate a 50-nanosecond pulse to enable cache storage of this first word of the odd/even pair. While the master device is retrieving the data presented to the TILINE data bus, the cache control logic causes the second word of the odd/even pair to enter the check bit and cache parity logic.

After the check bit comparison has been made on that word, it is also stored in cache. At time T625, output signals from the memory timer generate a 50-nanosecond pulse to enable cache storage of the second word of the odd/even pair. If on either of the cache write operations the cache logic detects an error from the check bit comparison, the cache operation is aborted and the error bit associated with the selected cache cell is enabled.

A cache cycle in which an error is detected in the cache proceeds as follows. At the assertion of TLGO-, both the primary memory and the cache address compare circuitry begin to look at the incoming address. At time GO110, the ADOK signal inhibits generation of the RAS signal and enables the drive signals to put data on the TILINE. At GO130 the results of the parity checks will reveal an error, thus inhibiting the generation of CTERM and causing the generation of an abort signal. The generation of the ABORT signal causes RAS to be generated to begin the start of a regular primary cycle. Twenty nanoseconds after RAS is generated, GO150 causes BUSY to go true to inhibit ENDR1 and disable the cache drive signals. The occurrence of ABORT also causes the cache error latch to go true. The CAER LED is lit and further cache memory cycles are prevented by inhibiting the enable cache terminate signal, ENCTRM. All subsequent read requests will be provided from primary memory.

2.4.3 TPCS Mode Operation

A master device uses the TPCS to gain access to the control logic of the cache controller for purposes of monitoring the operation or controlling the performance of the cache controller. The TPCS can be used to enable the cache option, to control error latches, and to operate the cache controller in the diagnostic mode.

The cache controller is placed in the diagnostic mode by placing the correct TPCS address on the TILINE address lines while executing a write operation. This address must fall between $FFC00_{16}$ and $FFE00_{16}$ (see table 2-10) and must match the address set in the TPCS pencil switches on the cache controller board. The operation of the cache controller while in the diagnostic mode is controlled by the data present on the TILINE data bus. Figure 2-17 illustrates the cache controller TPCS write word. Refer to table 2-11

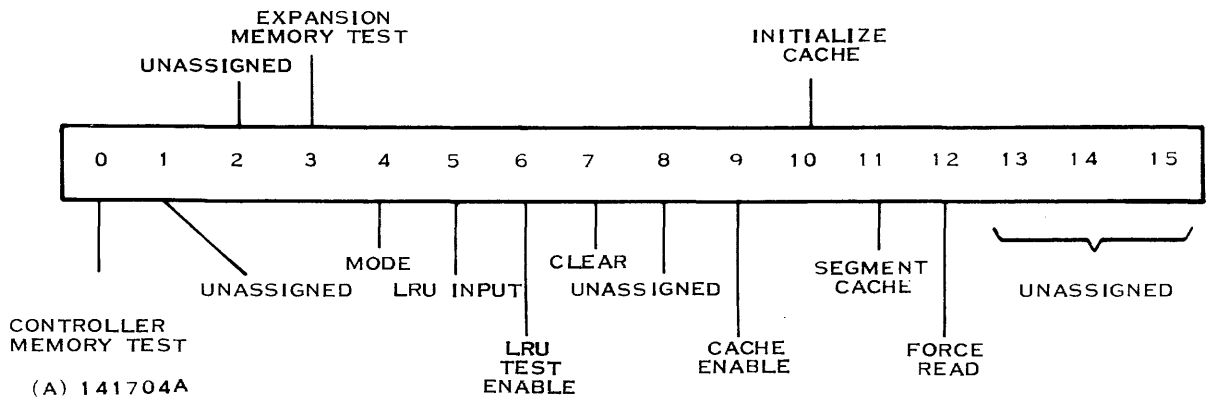


Figure 2-17. TPCS Write Word to Cache Controller

Table 2-11. Description of Bit Assignments for TPCS Write Word to Cache Controller

Bit	Description
0	When high, all read and write operations to the first 64K bytes of the primary memory on the cache board are modified as determined by bit 4.
1	Unassigned
2	Unassigned
3	When high, access to all expansion memory boards is modified as described for bit 0.
4	Mode bit. When low, error correction is disabled on banks in the areas of primary memory as specified by setting bits 0 and 3. When high, the six most significant data bits are swapped with the ECC field.
5	When enabled by bit 6, this bit controls the sense of the least-recently-used (LRU) bank flip-flop. When high, the LRU is forced high and the next word added to the cache memory is stored in bank B. When low, the LRU is forced low and the next word added to the cache memory is stored in bank A.
6	When high, the LRU bank flip-flop is forced to the sense of bit 5. This test allows a diagnostic check to control the bank of the cache memory to which new words are added.
7	When high, primary and cache memory error logic and the associated error indicator LEDs are cleared. This bit must be reset to reenable the primary memory error logic.
8	Unassigned
9	When set low, the cache logic is enabled (i.e., the cache controller begins processing primary memory references through the cache memory). When set high, the cache logic is completely disabled, and all primary memory references are made directly to primary memory.
10	When toggled (set to 1, then 0), the cache memory is initialized (i.e., all validity bits are set to false). All cache HITS will be disregarded unless the data was stored in the cache memory following the initialization.
11	When high, the controller stores data in the cache memory only from references made to the upper 32K bytes of primary memory. No data is stored in the cache memory if a MISS occurs with a primary memory address located in the lower 32K bytes of the on-board primary memory or located on any expansion board).

Tabel 2-11. Description of Bit Assignments for TPCS Write Word to Cache Controller (Continued)

Bit	Description
12	When high, this bit causes the cache to answer if an address match occurs. This bit is used to read cache addresses with parity errors.
13	Unassigned
14	Unassigned
15	Unassigned

for an explanation of the function of each write data bit while the cache controller is in the TPCS mode.

When the cache controller is placed in the diagnostic mode, tests may be performed either on primary memory or on the cache memory of the controller. The following diagnostic functions can be performed on primary memory:

- The 6 check bits generated on a write cycle and normally stored in the primary memory can be swapped with the 6 most significant data bits, 0 to 5.
- The 6 check bits returned from primary memory on a read cycle can be manipulated to replace data bits 0 to 5. Under this mode of operation, the error circuits detect and indicate any errors by using the appropriate indicator lamp, but error correction is inhibited and the data is not modified.
- The controller may be instructed to inhibit the data error detection and correction circuits so that uncorrected data may be read from memory.
- The error indication circuits can be reset by setting the primary memory reset bit (bit 7) in the TPCS write word.

The following diagnostic functions can be performed on the cache memory:

- The cache operation can be inhibited so that no cache operation will occur. Primary memory words residing in the cache will not be read during read cycles, and cache data will not be updated during write cycles.
- The cache operation can be restricted to the upper 32K bytes of the controller primary memory. This provides the capability to enter a diagnostic routine in the lower 32K bytes of the controller memory and prevent its execution from filling up the cache.
- The cache can be totally initialized by resetting all validity bits.
- The bank used by the cache to store new data can be preselected.

When reading the TPCS word, the cache controller places data words on the TILINE data bus. The data words read are even and odd forms of the TPCS address, as set in the TPCS pencil switches. Figure 2-18 shows the format of the two data words read from the cache controller. Table 2-12 explains the function of each read data word while the cache controller is in the TPCS mode.

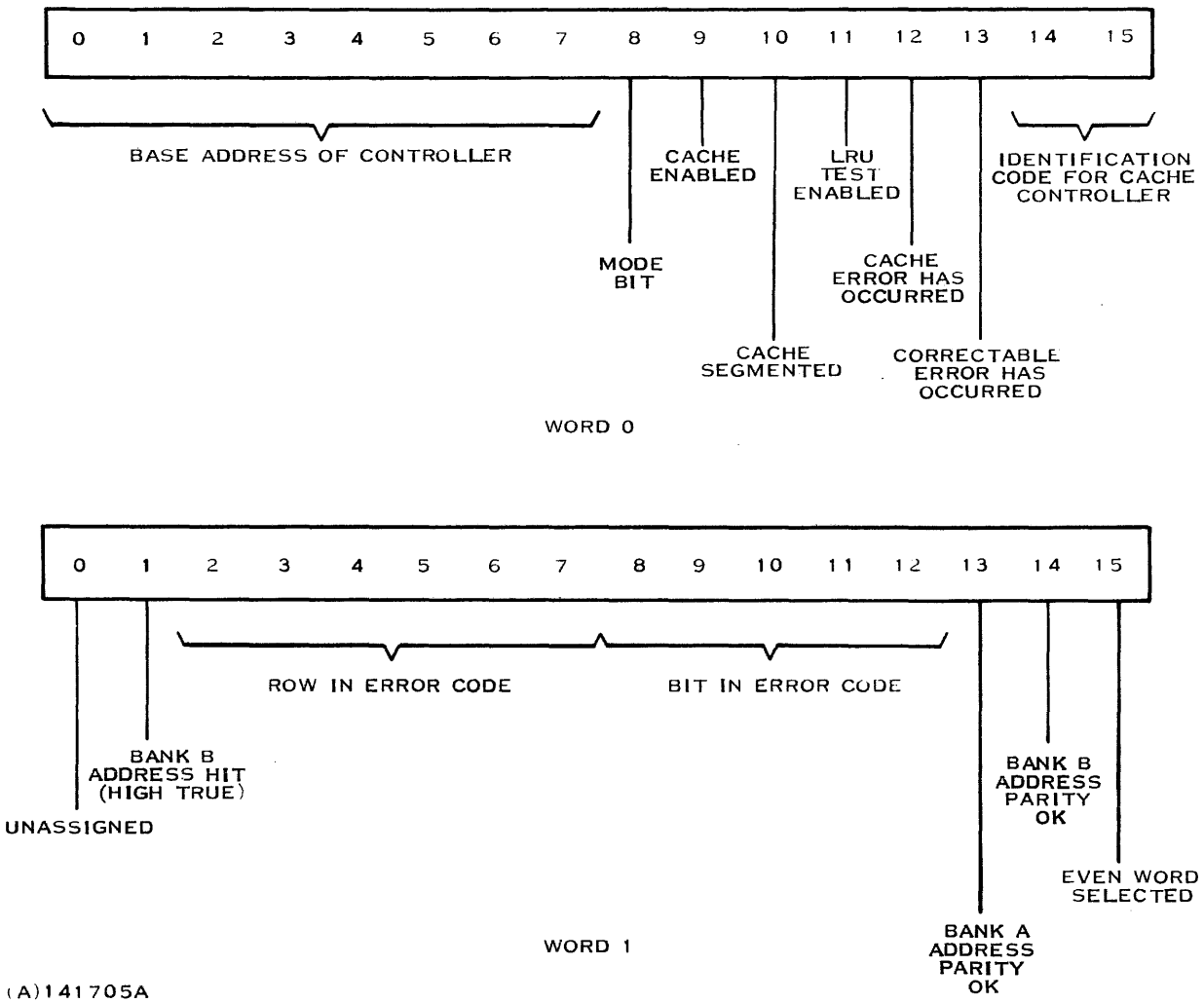


Figure 2-18. Data Words Output to TILINE During a Read Operation in TPCS Diagnostic Mode

Table 2-12. Bit Assignments for Read Words from Cache TPCS Diagnostic Mode

Bit	Description
WORD O:	
0-7	These eight bits indicate the setting found on the cache primary memory starting address pencil switches.
8-11	These bits echo the diagnostic state of the controller as follows; bit 8 = mode, bit 9 = cache enabled, bit 10 = cache segmented, and bit 11 = LRU enabled.
12	When high, a parity, validity, or error bit fault has occurred during a cache operation. An ECC error will also set this bit high.
13	When high, a single-bit ECC error has been detected and corrected in a fetch from primary memory.
14-15	These bits are permanently set to form the cache controller identify code, 01.
WORD 1:	
0	Unassigned; always set low.
1	When low, an address match has occurred in cache memory bank A.
2-7	The sense of these bits corresponds to the row-in-error information found on the error LEDs.
8-12	The sense of these bits corresponds to the bit-in-error information found on the error LEDs.
13	When high, the parity bits associated with the address fetch from cache memory bank A were good.
14	When high, the parity bits associated with the address fetch from cache memory bank B were good.
15	When high, an even word from cache memory has been selected. When low, an odd word has been selected.

3

Maintenance

3.1 GENERAL

This section describes the depot maintenance philosophy for the TILINE memories, provides operating procedures for the special test equipment required to perform depot maintenance, and provides checkout and fault isolation procedures for the TILINE memories. Depot maintenance for the memories may be performed in either one of two methods. In one method, a 990/10 hot mockup chassis is used to perform testing; in the other method, an Adar memory tester is used to perform testing. Procedures for both methods are provided in this section. Paragraphs 3.2 through 3.6 provide procedures and methods for use of the hot mockup; paragraphs 3.7 through 3.9 provide the procedures and methods for using the Adar memory tester.

3.2 MAINTENANCE PHILOSOPHY USING 990/10 HOT MOCKUP

Depot maintenance for the memory boards is based on the use of a 990/10 hot mockup, a logic analyzer, and a combination dual-trace oscilloscope/digital multimeter. Boards received from field maintenance repair facilities that are suspected to be faulty are serviced, one at a time, by placing the board on an extender board in the 990/10 hot mockup chassis. Initially, the board is tested under control of a diagnostic tape read into the 990/10 hot mockup memory from a cassette transport located in the 733 ASR/KSR Teleprinter. Any resulting error messages are then printed out on the 733 teleprinter.

Fault isolation down to the replaceable component level is performed using scoping loops (type determined by previous error message printout) entered from the programmers panel on the 990/10 hot mockup. Scoping loops are used in conjunction with the dual-trace scope/digital multimeter, the logic analyzer, the troubleshooting procedures provided in this section, and the diagrams provided in section 4. Scoping loops are also available in cassette form (verb package) for easy loading into memory. See the *Model 990 Computer Diagnostics Handbook,* part number 945400-9701, for details.

Once the faulty component has been identified, the board should be properly tagged (describing the corrective maintenance to be performed) and sent to the corrective maintenance workstation for repair. The repaired board is then returned to the troubleshooting workstation and tested for any further problems. If the diagnostic test runs to completion five consecutive times without an error message printout, the board is returned to normal use.

3.3 SPECIAL TEST EQUIPMENT

The 990/10 hot mockup system is used to perform depot maintenance on the TILINE memory boards. The operating controls and indicators and normal operating procedures for the 990/10 hot mockup system are provided in the *Model 990/10 Computer System Depot Maintenance Manual,* part number 945404-9701. An oscilloscope/digital voltmeter and logic analyzer are a part of the 990/10 hot mockup system. Refer to the manufacturer-supplied user manuals for operating procedures for these units.

3.4 990/10 HOT MOCKUP SYSTEM

The 990/10 hot mockup system consists of the following hardware units:

- 990/10 6-slot chassis with programmer panel and standby power supply options
- 990/10 AU1 and AU2 boards with loader and diagnostic ROM
- 990/10 ECC memory set of (2) boards with 64K bytes
- Extender ribbon cables for interconnection of boards on extender boards. Cable for memory addresses (AU1 to AU2) should have damping resistors in the lines.
- 733 ASR kit including TTY/EIA module, interface cable, and 733 ASR Data Terminal
- 990 CRU Expansion kit including 990 CRU expansion board, interface cable, and CRU buffer board
- 990 I/O expansion chassis with optional peripheral interface boards or associated peripherals, depending on subsystems serviced by the depot maintenance facility
- 16 I/O TTL Data Module.

3.4.1 733 ASR Data Terminal

The 733 ASR data terminal is used to load diagnostics from tape cassettes into the computer memory and to provide hardcopy printout of test results. The keyboard permits the operator to communicate with the diagnostic software when system parameters are required to execute the diagnostic or when calling up one of the loop programs available with some diagnostic systems (see Model 990 Computer Diagnostics Handbook for details).

For additional information on the 733 ASR, refer to the *Model 990 Computer, Model 733 ASR/KSR Data Terminal Installation and Operation*. Procedures for loading a diagnostic into the 990/10 hot mockup computer are contained in the *Model 990/10 Computer System Depot Maintenance Manual,* part number 945404-9701.

3.4.2 Programmer Panel

The use of the programmer panel with its controls and indicators are described in detail in the *Model 990/10 Computer System Hardware Reference Manual,* part number 945417-9701. Basically, the panel functions in one of the modes:

- Run mode
- Halt mode

Run Mode. When power is initially applied to the computer, the system comes up in the run mode, which locks out the programmer controls.

In this mode of operation, the RUN LED and all DATA DISPLAY LEDs on the panel are lighted and remain lit.

Halt Mode. In order to set the programmer panel to the halt mode, the key must be inserted in the key switch and the switch rotated to the UNLOCK position. At this time, pressing the HALT/SIE switch halts the computer and activates the controls on the programmer panel. The panel may be returned to the run mode by pressing the RUN switch.

3.5 DIAGNOSTIC TEST

The diagnostic test used to support depot maintenance of the 990/12 memory boards is RAMTST, Texas Instruments part number 2250586-9901.

3.6 MEMORY BOARD CHECKOUT AND FAULT ISOLATION PROCEDURES USING HOT MOCKUP SYSTEM

Memory board checkout procedures and fault isolation procedures are provided in tabular form in the paragraphs that follow. Once a malfunction has been discovered through the use of the tabular checkout procedures, a scoping loop may be entered into the computer via the programmer panel on the 990/10 hot mockup system. The scoping loop permits data to be continuously written into or read from a desired memory location or block of memory locations where a malfunction has been identified through use of the memory diagnostic test. Dynamic troubleshooting may then be performed on the board under test, using the tabular fault isolation procedures provided. The various types of scoping loops used in performing fault isolation are described in the subparagraphs that follow.

3.6.1 Repeated Write at Same Memory Location

Use the format shown in example program 1 to loop on a single specified address on the board under test.

The scoping loop program is entered into the computer from the programmer panel using the following procedure:

1. If the 990 Maintenance Unit is being used, set its POWER switch to the ON position and set the MODE switch to the PANEL position. If the programmer panel is part of the computer chassis, skip step 1 and proceed to step 2.
2. Set the key switch on the programmer panel to the UNLOCK position.
3. If the RUN LED is lighted, press the HALT/SIE switch to halt the processor and begin execution of the programmer panel code. When the panel is active, the RUN LED is extinguished.
4. Press the CLR switch to clear the panel's display register.
5. Press the ENTER ST (enter status) switch to clear the status register.
6. Set up 0900_{16} on the data display LEDs using the data entry switches. This is the address in memory where the first instruction of the scoping loop is to be stored.

NOTE

When a data display LED is lighted, it indicates a "1".

7. Press ENTER MA switch to load the

EXAMPLE 1

MEM Location	Machine Code	Comments
0900	02E0	LWPI, >100
0902	0100	
0904	0208	LI R8, (location)
0906	2000	Desired memory location upon which test will loop.
0908	0209	LI R9, (Data)
090A	0F0F	(Or any desired pattern)
090C	C609	Mov R9, *R8
090E	10FE	JMP $-1

memory address value 0900 into the memory address register.

8. Press CLR to clear the displays for the next entry.

9. Set up the instruction code ($02E0_{16}$) on the data LED displays using the data entry switches.

10. Press MDE switch, which causes 02E0 to be loaded into memory location 0900.

11. Press MAI, which increments the memory address value stored in the memory address register, and repeat steps 8-11 to enter the following program values into successive memory locations:

    - 0100
    - 0208
    - Address that the test will loop on (greater than 2000_{16} for memory expansion)
    - 0209
    - Data to be written into the looped memory location
    - C609
    - 10FE

12. Press CLR to clear the displays.

13. Enter 0900 into the displays (address of first instruction in the scoping loop).

14. Press ENTER PC to load the value into the program counter.

15. Press RUN to begin execution of the program. The RUN LED should light to indicate proper operation.

NOTE

If the RUN LED fails to light, return to step 1 and repeat the program setup procedure.

3.6.2 Continuous Read from Selected Memory Location

The basic scoping loop program described in 3.6.1 may be modified to perform a continuous read at a selected memory address. This is done by changing the instruction at memory location 090C in the previous program from C609 to C258, which is a MOV *R8, R9 instruction. This change to the basic program causes data to be read from a selected address and stored in memory location 0112 (workspace register 9). For maintenance purposes, the scoping loop may be interrupted at any time and the value stored in the workspace register may be examined using the following procedure:

1. Halt the processor by pressing HALT/SIE. The RUN LED should extinguish.

2. Press CLR to clear the displays.

3. Enter 0112 into the displays using the data entry switches.

4. Press ENTER MA to load 0112 into the memory address register.

5. Press MDD. The resulting value displayed on the panel LEDs should be the same value stored in memory location 090A of the scoping loop program.

3.6.3 Scoping Loop for Reading a Band of Memory Addresses

The basic scoping loop program may also be modified as shown in example program 2 to permit looping over a band of memory addresses in which the beginning and ending addresses are specified in the program.

NOTE

The procedures for entering this program are essentially the same as those described in paragraph 3.6.1.

3.6.4 96KB Memory Controller Checkout Procedure

On the 990/10 hot mockup chassis, set programmer panel key switch and battery switch to OFF. Install a known-to-be-good 96KB memory controller with at least 32K bytes of memory into slot 3 of the 990/10 hot mockup chassis. Mount the 96KB memory controller to be tested on a 990 extender board and install the extender into slot 5 of the 990/10 hot mockup chassis with the component side of the board facing up. Ensure that memory size jumpers E9 and E10 are installed to match the memory size of the board in accordance with the schedule of table 2-5.

Set starting address switches on board to be tested to select starting address of 8000_{16} bytes by setting switch number 6 to ON and all others to OFF. (This assumes that a 32K byte memory with start address set to 0000_{16} is used for storage of the diagnostic program.) Perform the checkout procedures described in table 3-1. If abnormal indications are obtained, refer to the fault isolation procedures of table 3-2.

3.6.5 The 96KB Memory Controller and 256KB Add-On Array Fault Isolation Procedure

Once a malfunction has been discovered through the use of the checkout procedure of table 3-1, a scoping loop may be set up to facilitate dynamic troubleshooting of the board under test. The scoping loop permits data to be written into or read from a desired memory location or block of memory locations where a malfunction was identified by the diagnostic procedures of table 3-1. Use the procedures in paragraphs 3.6.1 through 3.6.3 to establish the required scoping loop.

3.6.6 The 256K Memory Add-On Module with 960/16KR ECC Checkout Procedures

On the 990/10 hot mockup chassis, set programmer panel key switch and battery switch on OFF. Ensure that a known-to-be-good 96KB memory controller with at least 32K bytes of memory is installed into slot 3 of the 990/10 hot mockup chassis. Mount the 256KB add-on memory board to be tested on a 990 extender board and install the extender into slot 4 of the 990/10 hot mockup chassis with the component side of the board facing up. At the top edge of the two memory boards, use two 50-pin connector ribbon cables to connect P3 of the control memory

---

EXAMPLE 2

MEM Location	Machine Code	Comments
0900	02E0	LWPI>100
0902	0100	
0904	020A	LI R10, ENDLOC
0906	ENDLOC	Ending address +2
0908	0209	LI R9, DATA
090A	DATA	
090C	0208	LI R8, LOC
090E	LOC	
0910	CE09	MOV R9, *R8+
0912	820A	C R10, R8
0914	14FB	JHE
0916	10FC	JMP

Table 3-1. 96KB Memory Controller and 256KB Add-On Memory Checkout Procedures

Step	Procedure	Normal Indication	If Abnormal
1	On 990/10 hot mockup chassis, set programmer panel key switch and battery switch to ON.		
2	To verify correct operation of refresh timing circuits, connect oscilloscope probe to pin 4 of any TMS 4116 memory chip in row 0. The host CPU should be IDLE during this test so that the image on the scope will be uncluttered by front panel memory accesses. To enter IDLE mode, perform the following steps: 1. Halt the CPU 2. Enter a 0100_{16} on the front panel 3. Depress the PC button 4. Depress the MA button 5. Enter a 0340_{16} on the front panel 6. Depress the MDE button 7. Depress RUN 8. IDLE light should illuminate	See below.	See table 3-2, step 4.

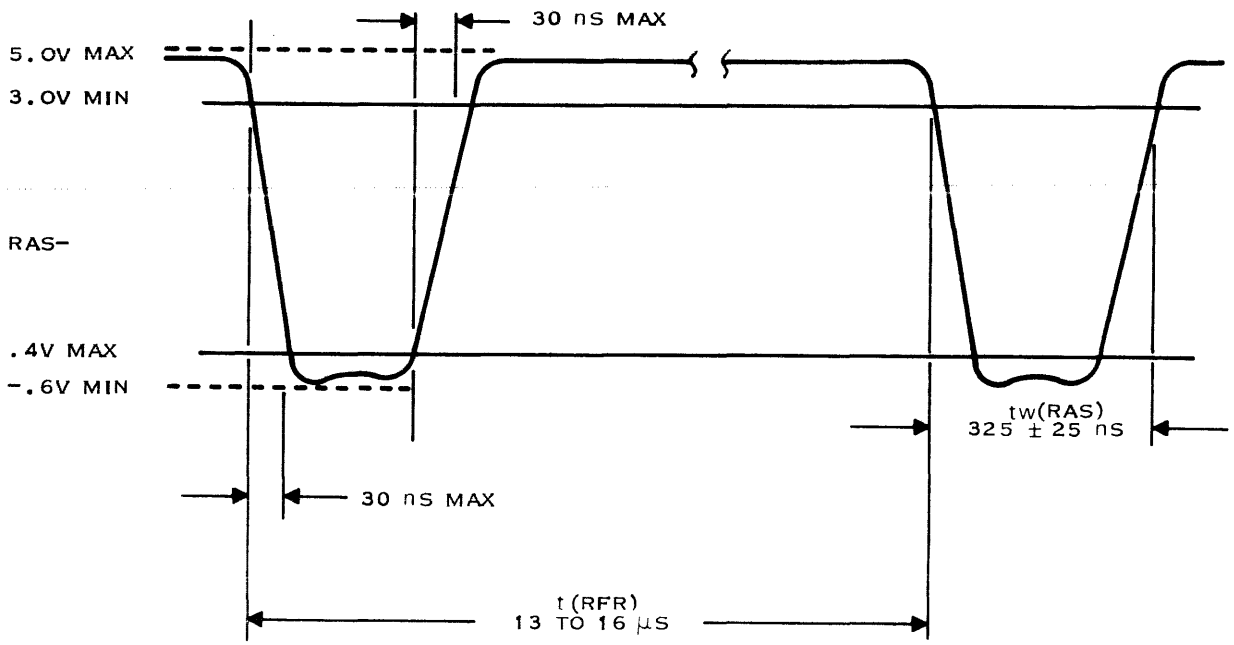


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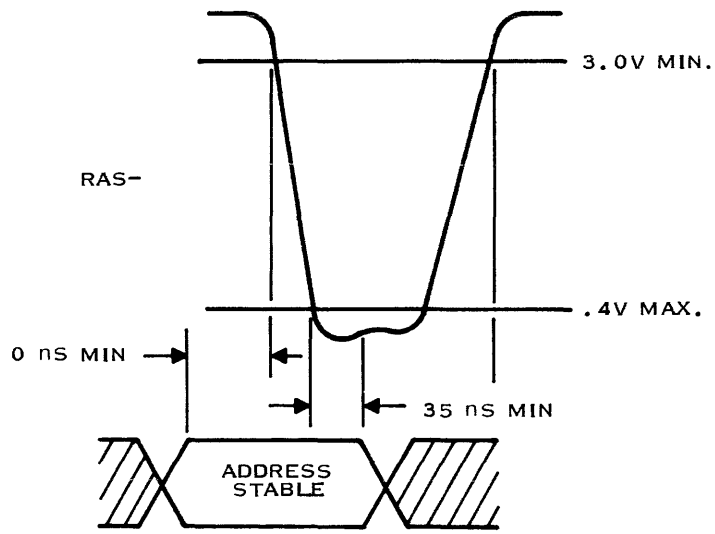
Table 3-1. 96KB Memory Controller and 256KB Add-On Memory Checkout Procedures (Continued)

Step	Procedure	Normal Indication	If Abnormal
3	Repeat step 2 for memory rows 1 and 2 by moving oscilloscope probe to pin 4 of any TMS 4116 memory chip in each of rows 1 and 2. Repeat step 2 for remaining memory rows if 256KB add-on memory is board under test.	Same as for step 2.	Same as for step 2.
4	Connect oscilloscope channel 1 probe to pin 4 of any TMS 4116 memory chip in row 0 and connect channel 2 probe in turn to each of the address lines, ADDR0A- through ADDR6A- (pins 5, 6, 7, 10, 11, 12, 13). Synchronize oscilloscope to channel 1 and note that each address line toggles.		See table 3-2, step 1, and check address path through B6, C6, E1, E2.



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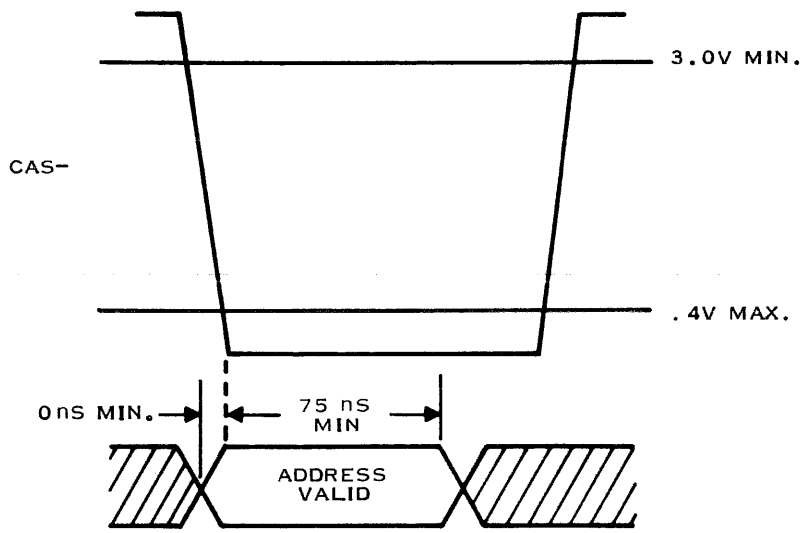
5	Connect oscilloscope channel 1 probe to pin 4 of any TMS 4116 memory chip in row 1 and connect channel 2 probe in turn to each of the address lines, ADDR0B- through ADDR6B-. Synchronize oscilloscope to channel 1.	Same as for step 4.	Same as for step 4.

Table 3-1. 96KB Memory Controller and 256KB Add-On Memory Checkout Procedures (Continued)

Step	Procedure	Normal Indication	If Abnormal
6	Connect oscilloscope channel 1 probe to pin 4 of any TMS 4116 memory chip in row 2 and connect channel 2 probe in turn to each of the address lines, ADDR0C- through ADDR6C-. Synchronize oscilloscope to channel 1. Repeat step 4 for remaining memory rows if 256KB add-on memory is board under test.	Same as for step 4.	Same as for step 4.
7	Repeat step 4, connecting channel 1 probe to pin 15 of any TMS 4116 chip in row 0 instead of to pin 4. Connect channel 2 probe in turn to each of the address lines, ADDR0A- through ADDR6A-. Synchronize oscilloscope to channel 1 and note that each address line toggles.	See below.	See table 3-2, step 4. If no abnormal result indication results from this step, check CADSEL- (J1-5), address multiplexer (E1, E2), and address drive.



(A)142841

8	Connect oscilloscope channel 1 probe to pin 15 of any TMS 4116 memory chip in row 1, and connect channel 2 probe in turn to each of the address lines ADDR0B- through ADDR6B-. Synchronize oscilloscope to channel 1.	Same as for step 7.	Same as for step 7.

Table 3-1. 96KB Memory Controller and 256KB Add-On Memory Checkout Procedures (Continued)

Step	Procedure	Normal Indication	If Abnormal
9	Connect oscilloscope channel 1 probe to pin 15 of any TMS 4116 memory chip in row 2, and connect channel 2 probe in turn to each of the address lines ADDR0C- through ADDR6C-. Synchronize oscilloscope to channel 1. Repeat step 7 for remaining memory rows if 256KB add-on memory is board under test.	Same as for step 7.	Same as for step 7.
10	Insert the cassette containing the diagnostic test RAMTST[1] (part number 2250586) into the 733 ASR cassette transport (see paragraph 3.4.1).		
11	Set 733 POWER switch to ON position. Set 733 ON LINE switch to ON LINE position. Set 733 CONT START/STOP switch to STOP position.	733 POWER in dicator lights. PLAYBACK CONTROL indicator extinguishes.	
12	Press REWIND switch for applicable cassette transport and wait for END indicator to light.	END indicator on 733 lights.	
13	Press LOAD/FF and wait for READY indicator to light.	READY indicator lights when tape is properly positioned. Playback light comes on.	
14	Set key switch on programmer panel to UNLOCK position, then press LOAD switch on panel.	Cassette begins moving under software control. When load is complete, the verb-package initialization sequence begins.	
15	In response to test query for beginning address, enter 8000.		

Note:

[1] RAMTST is a verb-package test and, as such, runs under control of a 990 verb package. The verb package executes the complete test or allows the operator to execute selected portions of the test by entering two-letter mnemonics called verbs. Refer to the *Model 990 Computer Diagnostics Handbook,* part number 945400, volumes 1 and 2, for instructions in the use of the verb package and for a description of RAMTST.

Table 3-1. 96KB Memory Controller and 256KB Add-On Memory Checkout Procedures (Continued)

Step	Procedure	Normal Indication	If Abnormal
16	In response to test query for ending address for memory board under test, enter 17FFE for 64K byte memory size		
17	Initialize the diagnostic and start the test by using the "EA" verb.	Printout indicates satisfactory completion of test.	Take corrective action as indicated by printout. Gross data errors indicate timing problems. Data errors on one or a few bits indicate data path problems. See table 3-2.

Table 3-2. The 96KB Memory Controller and 256KB Add-On Memory Board Fault Isolation Procedure

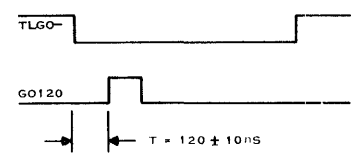
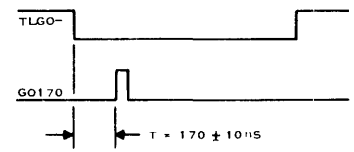
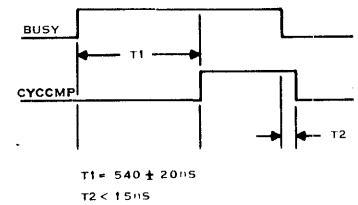
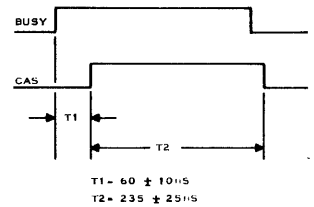
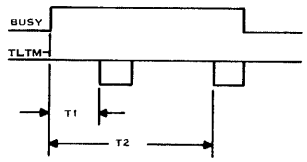
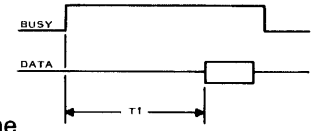
Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
			Memory Timing Problems		
1	Excessive number of data errors indicate board timing may be faulty.	Improper timing of GO120 pulse.	Use verb E4 to execute subtest 4 of RAM10 (or verb ET7 to execute subtest 7 of RAMTST) so that memory testing is not interrupted for header printing. Connect oscilloscope channel 1 probe to pin 7 of B07 and connect channel 2 probe to pin 10 of H03. Trigger the oscilloscope on negative transition of channel 1.		Replace resistor R11 or capacitor C96, first, to correct timing. If timing not brought into tolerance, replace the 74LS132 network, J05.
2	Same as step 1.	Improper timing of GO170 pulse.	Connect oscilloscope channel 1 probe to pin 7 of B07 and connect channel 2 probe to pin 12 of H03. Trigger the oscilloscope on negative transition of channel 1.		Replace resistor R12 or capacitor C86, first, to correct timing. If timing not brought into tolerance, replace the 74LS132 network, J05.
3	Same as step 1.	Time to clear CYCCMP signal is excessive.	Connect oscilloscope channel 1 probe to pin 8 of H02 and connect channel 2 probe to pin 6 of H02. Trigger the oscilloscope on positive transition of channel 1.		If T2 abnormal, replace H02. If T1 abnormal, delay line and associated networks.

Table 3-2. The 96KB Memory Controller and 256KB Add-On Memory Board Fault Isolation Procedure (Continued)

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
4	Same as step 1.	Improper timing of column address strobe, CAS.	Connect oscilloscope channel 1 probe to pin 8 of H02 and connect channel 2 probe to pin 9 of J02. Trigger the oscilloscope on positive transition of channel 1.	 T1 = 60 ± 10nS T2 = 235 ± 25nS	Adjust timing by replacing delay line, and/or associated networks.
5	Same as step 1.	Improper write access time (T1) or improper read access time (T2).	Connect oscilloscope channel 1 probe to pin 8 of H02 and connect channel 2 probe to pin 2 of B07. Trigger the oscilloscope on positive transition of channel 1.	 T1 = 185 ± 25nS T2 = 320 ± 25nS	Adjust timing by replacing delay line and/or associated networks.
6	Same as step 1.	Improper data access time (T1).	Connect oscilloscope channel 1 probe to pin 8 of H02 and connect channel 2 probe to pin 14 of any TMS 4116 memory chip. Trigger the oscilloscope on positive transition of channel 1.	 T1 = 225 nS, MAXIMUM	Adjust timing by replacing delay line and/or associated networks.

to P3 of the memory under test and to connect P4 of the control memory to P4 of the memory under test. Perform the checkout procedures described in table 3-1. If abnormal indications are obtained during a checkout procedure, refer to the fault isolation procedures of table 3-2.

3.6.7 Cache Memory Controller Checkout Procedure

On the 990/10 hot mockup chasis, set programmer panel key switch and battery switch to OFF. Install a known-to-be-good 96KB memory controller with at least 32K bytes of memory into slot 3 of the 990/10 hot mockup chassis. Mount the cache memory controller to be tested on a 990 extender board, and install the extender into slot 5 of the 990/10 hot mockup chassis with the component side of the board facing up.

Set starting address switch on the board to be tested to select starting address of 8000_{16} bytes by setting switch number 6 to ON and all others to OFF. (This assumes that a 32K byte memory with start address set to 0000 is used for storage of the diagnostic program.) Verify that the TPCS base address is set to FB10 (see table 2-6 and 2-10). Perform the checkout procedures described in table 3-3. If abnormal indications are noted during a checkout procedure, refer to the fault isolation procedures of paragraph 3.6.8.

3.6.8 Cache Memory Controller Fault Isolation and Troubleshooting Procedures

Once a malfunction has been discovered through the use of the checkout procedure of table 3-3, a scoping loop may be set up to facilitate dynamic troubleshooting of the board under test. The scoping loop permits data to be written into or read from a desired memory location or block of memory locations where a malfunction was identified by the diagnostic procedures of table 3-3. Use the procedures in paragraph 3.6.1 through 3.6.3 to establish the required scoping loop. Useful procedures and waveforms for isolating troubles in the cache memory controller are provided in the following subparagraphs.

3.6.8.1 Troubleshooting Cache for MISS Operation. The following program will cause the cache to have a MISS on each access. The waveforms shown in figure 3-1 are for a MISS operation.

1. Set starting address for cache controller to be tested to 0000 and set the TPCS address to $FB10_{16}$.

2. Apply power to the 990/10 hot mockup chassis.

3. At address $FB10_{16}$ enter 60, 50, 10 at the programmer panel as follows:

   Enter FB10, press MA

   Enter 60, press MDE

   Enter 50, press MDE

   Enter 10, press MDE

Table 3-3. Cache Memory Controller Checkout Procedures

Step	Procedure	Normal Indication	If Abnormal
1	On 990/10 hot mockup chassis, set programmer panel key switch and battery switch to ON.		
2	To verify correct operation of refresh timing circuits, connect oscilloscope probe to pin 4 of bank 0 TMS 4116 at location U5. The host CPU should be IDLE during this test so that the image on the scope will be uncluttered by front panel memory accesses. To enter IDLE mode, perform the following steps: 1. Halt the CPU 2. Enter a 0100_{16} on the front panel 3. Depress the PC button 4. Depress the MA button 5. Enter a 0340_{16} on the front panel 6. Depress the MDE button 7. Depress RUN 8. IDLE light should illuminate	See below.	See table 3-2, step 4.

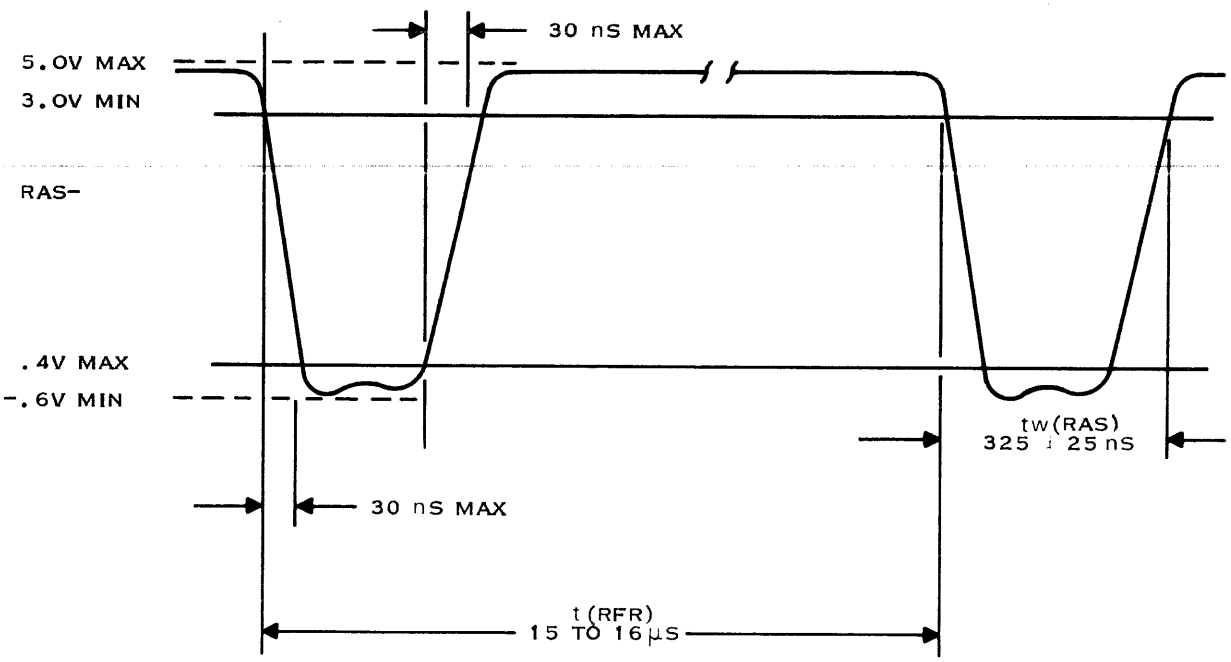


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Table 3-3. Cache Memory Controller Checkout Procedures (Continued)

Step	Procedure	Normal Indication	If abnormal
3	Repeat step 2 for memory bank 1 by moving oscilloscope probe to pin 4 of bank 1 TMS4116 at location T5.	Same as for step 2.	Same as for step 2.
4	Remove ac power by setting key switch on programmer panel to OFF but leave battery power on. Repeat steps 2 and 3.	Same as for step 2.	Same as for step 2.
5	Verify operation of the refresh address counter as follows. Connect channel 1 of oscilloscope to pin 4 of bank 0 TMS4116 at location U5. Synchronize oscilloscope channel 1 negative edge. Observe dynamic RAM address inputs by connecting, in turn, the channel 2 probe of the oscilloscope to pins 5, 6, 7, 10, 11, 12, and 13 of U5. Each address line should show both high and low states during RAS–.	See below.	

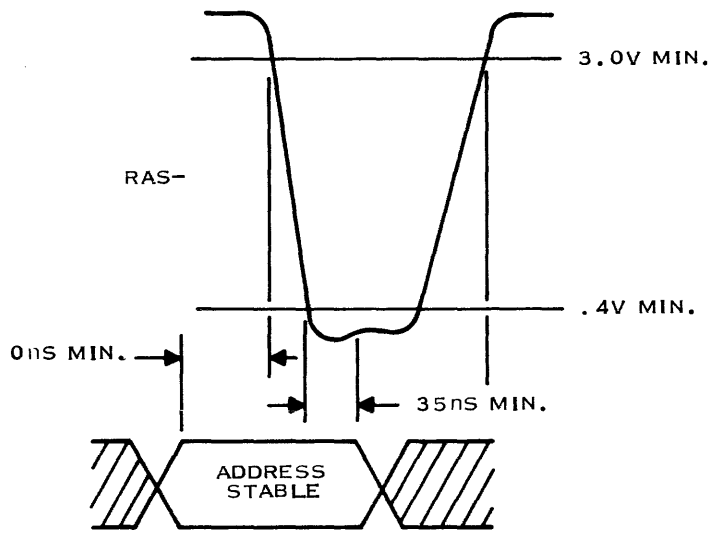

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Table 3-3. Cache Memory Controller Checkout Procedures (Continued)

Step	Procedure	Normal Indication	If Abnormal
6	Verify proper timing of the delayed timing signals GO110 and GO130. Use figure 3-9 to determine test points for oscilloscope.	See paragraph 3.2.7.3 and figure 3-9.	See paragraph 3.2.7.3 and figure 3-9.
7	Insert the cassette containing the diagnostic test RAMTST[1] (part number 2250586) into the 733 ASR cassette transport (see paragraph 3.4.1).		
8	Set 733 POWER switch to ON position. Set 733 ON LINE switch to ON LINE position. Set 733 CONT START/STOP switch to STOP position.	733 POWER indicator lights. PLAYBACK CONTROL indicator extinguishes.	
9	Press REWIND switch for applicable cassette transport and wait for END indicator to light.	END indicator on 733 lights.	
10	Press LOAD/FF and wait for READY indicator to light.	READY indicator lights when tape is properly positioned. Playback light comes on.	
11	Set key switch on programmer panel to UNLOCK position, then press LOAD switch on panel.	Cassette begins moving under software control. When load is complete, the verb-package initialization sequence begins.	
12	In response to test query for ending address for memory board under test, enter 17FFE for 64K byte memory size.		

Note:

[1] RAMTST is a verb-package test and as such runs under control of a 990 verb package. The verb package executes the complete test or allows the operator to execute selected portions of the test by entering two-letter mnemonics called verbs. Refer to the *Model 990 Computer Diagnostics Handbook,* part number 945400, volumes 1 and 2 for instructions in the use of the verb package and for a description of RAMTST.

Table 3-3. Cache Memory Controller Checkout Procedures (Continued)

Step	Procedure	Normal Indication	If Abnormal
13	Initialize the diagnostic and start the test by using the "EA" verb.	Printout indicates satisfactory completion of test.	Take corrective action as indicated by printout. Gross data errors indicate timing problems. Data errors on one or a few bits indicate data path problems.

NOTE

This process initializes the cache and causes it to segment (that is, only cache locations above address 8000_{16}). Pressing RESET clears this function.

4. From the programmer panel, enter the test loop shown in example program 3.

EXAMPLE 3

```
0100    C820    STRT MOV
                @TST2,@TST1
0102    8000
0104    0300
0106    0820    MOV
                @TST3,@TST1
0108    9000
010A    0300
010C    C820    MOV
                @TST4,@TST1
010E    A000
0110    0300
0112    10F6    JMP STRT

8000    AAAA
8002    5555
9000    1111
9002    2222

A000    4444
A002    8888

PC = 100
HALT
RESET
RUN
```

Observe waveforms of figure 3-1.

3.6.8.2 Troubleshooting Cache in Write-Through Operation. The following program will cause the cache to perform write-through operations. Figure 3-2 shows the waveforms that should be observed.

1. Perform steps 1, 2, and 3 of paragraph 3.6.8.1.
2. At the programmer panel, enter the program shown in example program 4.
3. Observe the waveforms of figure 3-2.

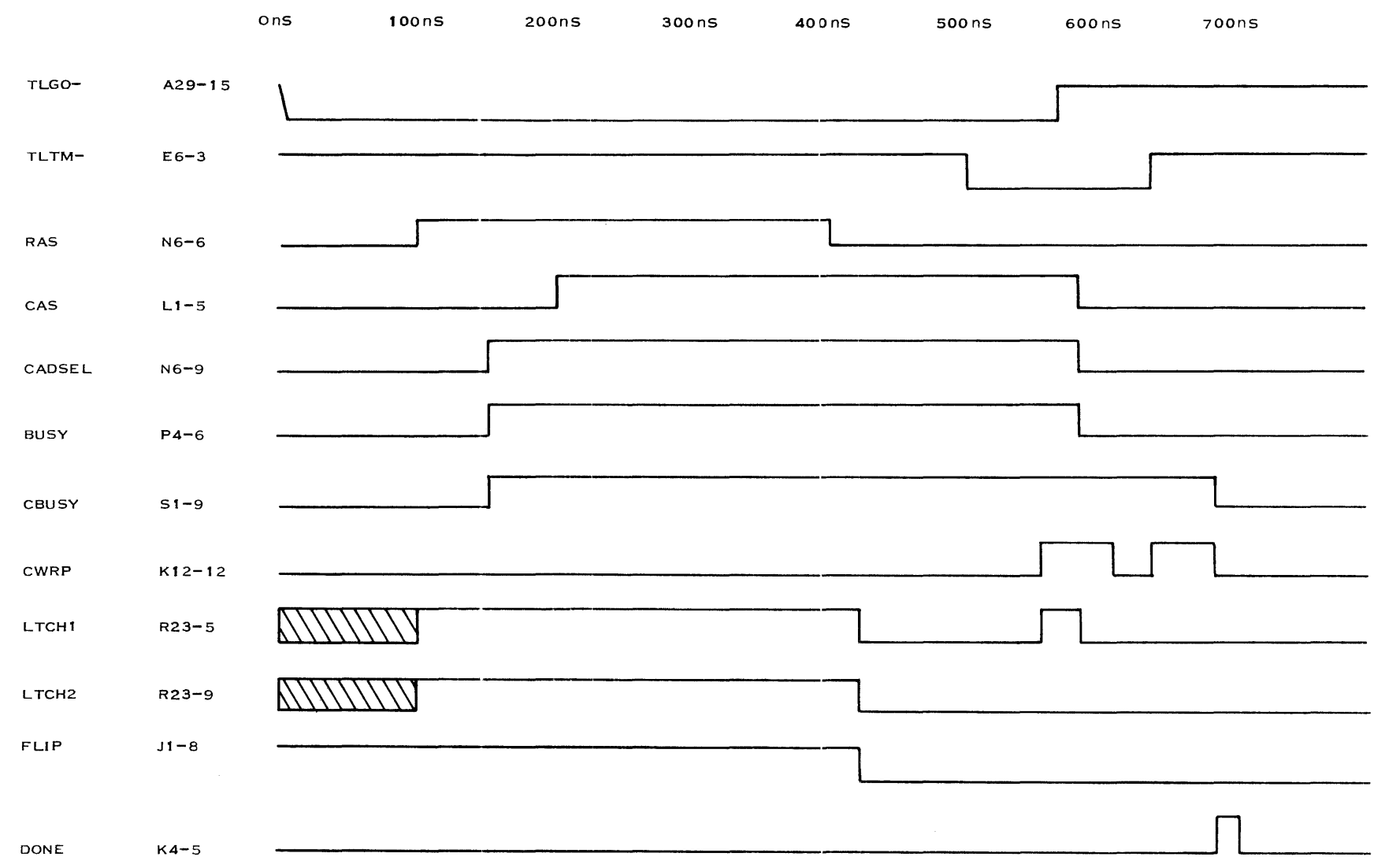


Figure 3-1. Cache Fill Operation

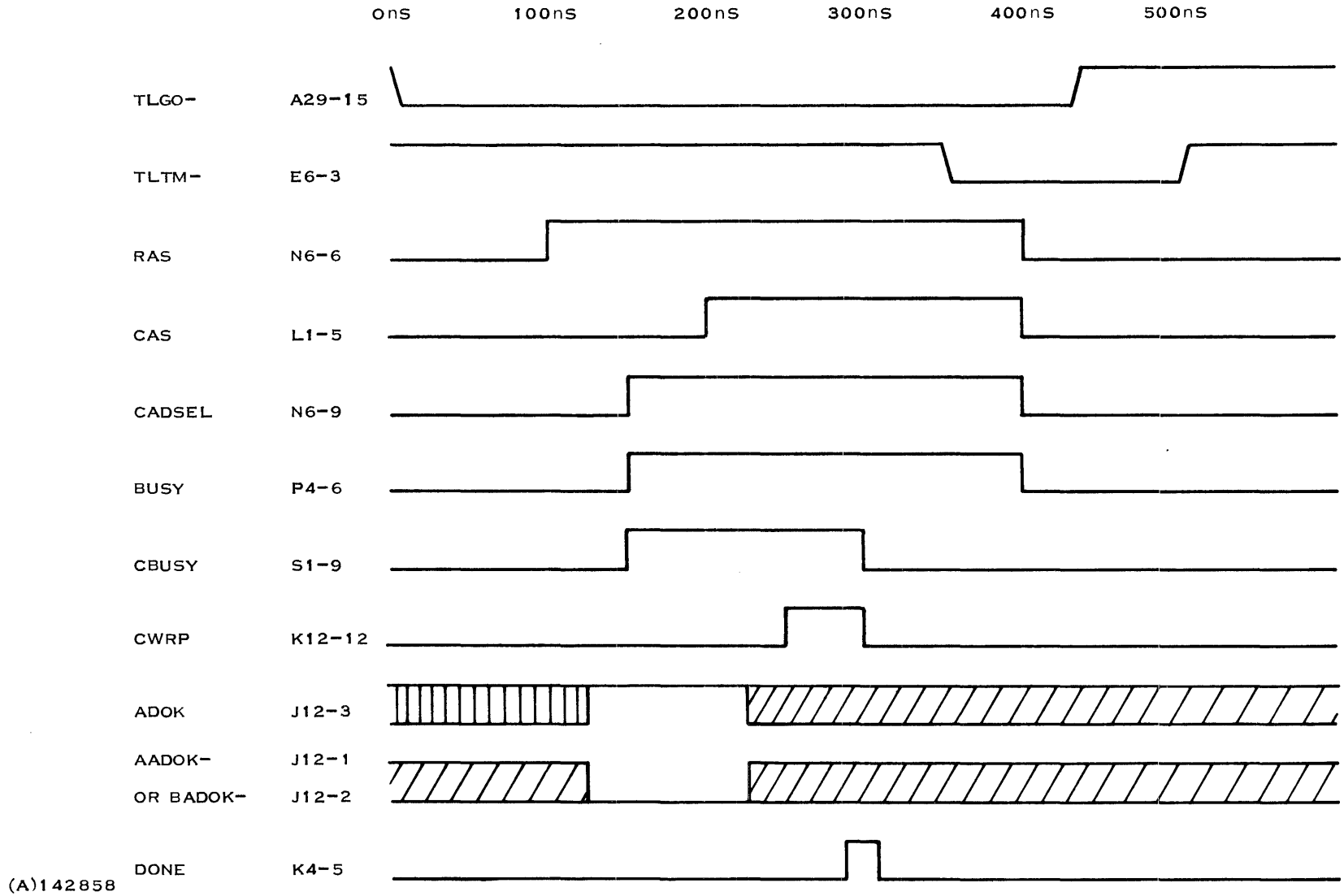


Figure 3-2. Cache Write-Through Operation

3.6.8.3 Troubleshooting Cache in HIT Operation. The following program will cause the cache to perform HIT operations. Figure 3-3 shows the waveforms that should be observed.

1. Perform steps 1, 2, and 3 of paragraph 3.6.8.1.
2. At the programmer panel enter the program shown in example program 5.
3. Observe the waveforms of figure 3-3.

3.6.8.4 Troubleshooting Primary Memory. To troubleshoot primary memory, enter the following program and observe the waveforms of figure 3-4.

1. Perform steps 1 and 2 of paragraph 3.6.8.1.
2. At address $FB10_{16}$ enter 60 and 40 at the programmer panel as follows:

   Enter FB10, press MA

   Enter 0060, press MDE

   Enter 0040, press MDE

   NOTE

   The above procedure initializes cache, then turns it off.

3. From the programmer panel, enter the program shown in example program 6.
4. Verify that the CBUSY signal does not come true.
5. Observe the waveforms of figure 3-4.

EXAMPLE 4

```
100   C280     STRT MOV @TST1,@ST2      READ FROM MEMORY
102   8000
104   010E
106   C280          MOV @TST3,@TST1     WRITE TO MEMORY
108   0110
10A   8000
10C   10FC          JMP STRT
10E   0000
10F   AAAA

PC    =100
RUN
```

EXAMPLE 5

```
100   C280     STRT MOV @TST1,@TST1
102   8000
104   8000
106   10FC          JMP STRT

PC    = 100
RUN
```

EXAMPLE 6

```
100     C280        MOV @TST1,@TST1        WRITE TO MEMORY
102     8000
104     8000
106     10F9        JMP STRT

PC      = 100
RUN
```

3.7 CACHE MEMORY BOARD CHECKOUT AND TROUBLESHOOTING PROCEDURES USING MEMORY TESTER

Instructions are provided in this paragraph for performing a checkout of the memory board using a memory tester. Additionally, useful troubleshooting procedures are provided along with waveform representations of the boards in various modes of operation.

Test equipment required to perform the memory board checkout procedures is listed in table 3-4.

3.7.1 Memory Test of Cache Memory Controller

Verify that the test equipment as listed in table 3-4 is currently certified and perform the test of the cache memory controller using the Adar memory tester as follows.

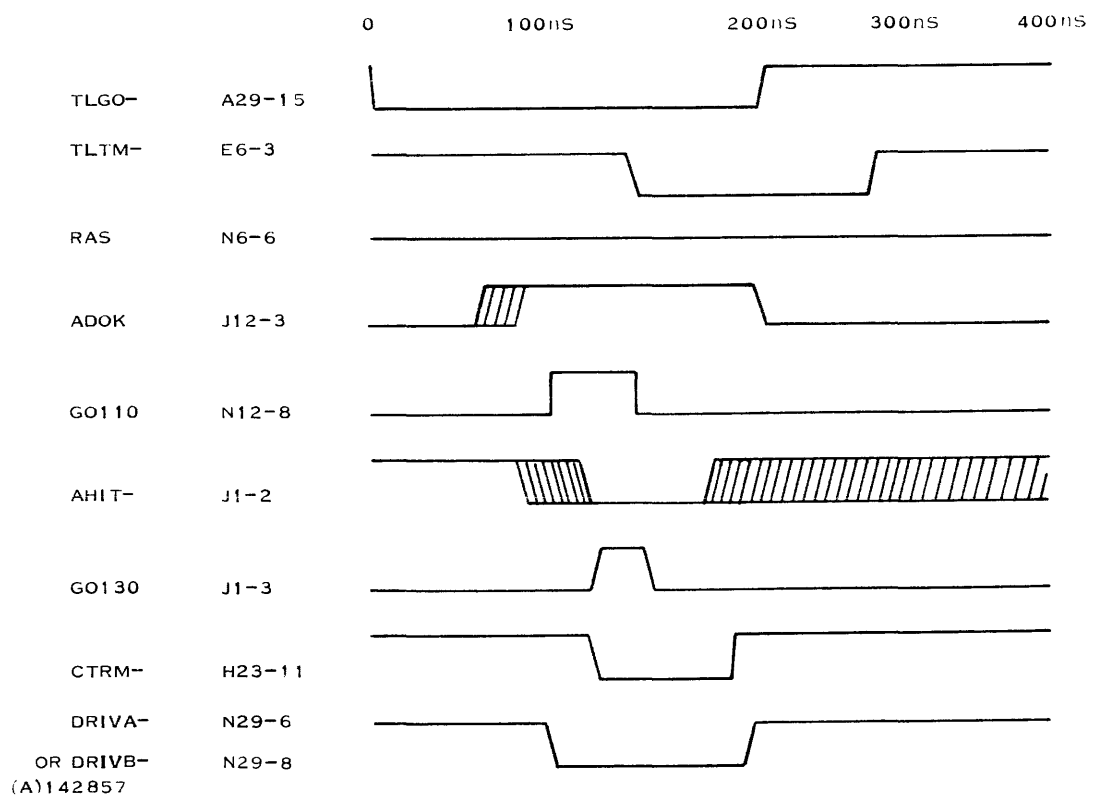


Figure 3-3. Cache HIT Operation

1. On the Adar memory tester, press the REM and RSI/RDS power switches, in that order (red switch lights should be off). Install the memory tester interface for the cache memory controller (part number 2264815-0005). Press the RSI/RDS and REM power switches, in that order (red switch lights should be on).

2. On the Adar memory tester, set RSI switches 1, 3, and 8 to the ON position and switches 4 through 7 to the OFF position.

3. Load the program tape, CACHET (TESTTS, ARRYTA). Enter "*RFI CACHET CAS" and press the XMIT key at the Adar memory tester data terminal.

4. Install the cache memory controller board to be tested into the memory tester interface with component side of the board facing the operator of the memory tester. Make connections as shown in table 3-5.

5. Peform visual check, ensuring that all DIP switches on the board under test are in the off position. Scan the board under test for solder shorts.

3.7.1.1 Primary Memory Test Execution. The primary memory test is started by entering "*R 0 0" and pressing the XMIT key at the Adar memory tester data terminal. The first test, a march pattern with nominal supplies, executed with error correction off, is performed, and results are displayed on a board error map (BEM) at the data terminal of the memory tester. See figure 3-5 for an interpretation of the BEM. Following the BEM, "J+ TO CONT OR J- TO END" is displayed allowing the operator to power down or to continue the test by using the joystick toggle switch at the memory test control panel. If the operator moves the joystick to "+", a march pattern with nominal supplies is exe-

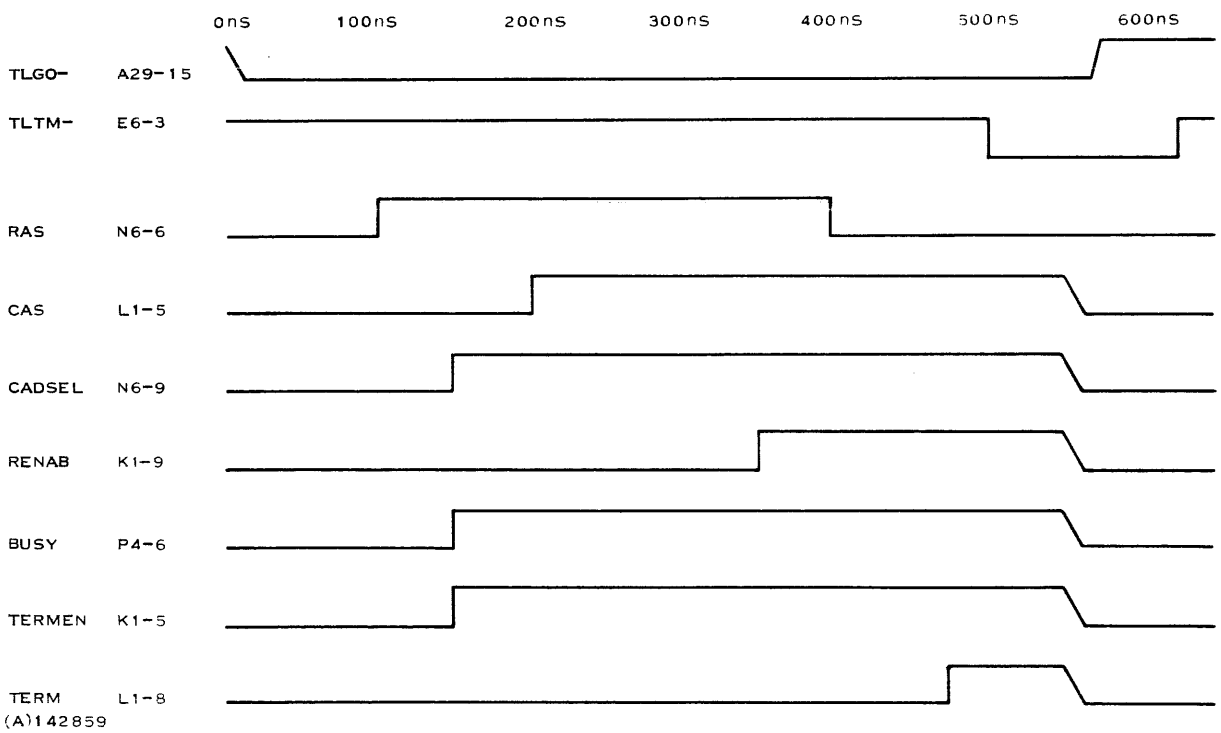


Figure 3-4. Memory Read, No Cache Operation

cuted on the error correction code storage RAMs. "J+ FOR DIAG OR TIMING; J- TO CONT" is displayed following the BEM, allowing the operator to branch to the diagnostic tests, to set timing, or to troubleshoot a problem; or to continue the test for primary memory if both march pattern tests are successfully completed. The diagnostic tests are described in paragraph 3.7.1.3, and those tests that are made when moving the joystick to "-" are described in paragraph 3.7.1.4.

3.7.1.2 Board Error Maps (BEM). The BEM is provided as a CRT display at the data terminal of the memory tester. As shown in figure 3-5, the BEM represents the memory array. Memory read errors are logged at speed during any given test, and at the end of each test the BEM displays any chip failures. The good chips are represented with asterisks, whereas failing memory chips are indicated by the reference designator of the failing chip. The BEM is interpreted as follows:

1. The first two rows of the BEM represent the 16K RAMs at reference designations, U5, U6, U8 through U11, U13, U14, U16, U17, U19, and U21 through U25 (first row); T5, T6, T8 through T11, T13, T14, T16, T17, T19, and T21 through T25 (second row). The asterisks are replaced by the corresponding reference designator as a failure occurs.

2. The second two rows of the BEM represent the 16K RAMs in the error correction code memory at reference designations U26 through U31 (first row) and T26 through T31 (second row).

3. The next two rows of the BEM represent the data channels at the expansion interface, MB00- through MB21- (odd numbered pins 1 through 43 of connector P4). As failures occur, MB00- is represented by B00, MB01- as B01, etc.

4. The last row of the BEM is enabled during the test for error correction (see paragraph 3.7.1.4). Each position represents one of the TILINE data channels TLDAT00- through TLDAT15-. As failures occur, the asterisks are replaced by B00 (TLDAT00-) through B15 (TLDAT15-).

3.7.1.3 Primary Memory Diagnostic Tests. The following is a description of primary memory diagnostic tests.

Table 3-4. Test Equipment Required for Memory Board Checkout Using Memory Tester

Item	Texas Instruments Part Number
Adar Model DR12/25 Memory Test System Tester	2264826-0001
Memory Tester Interface, Cache Memory Controller	2264815-0005
Oscilloscope, Tektronix Model 475 (or equivalent)	
Multimeter	
10X Probes with Grounding Clips	
Coaxial Cable with BNC to BNC Connectors	
Program Tape CACHET (TESTTS, ARRYTA)	

Existence Test. The existence test is run automatically after the joystick is toggled to "+" for the diagnostic tests. A BEM is displayed to indicate functioning memory chips. This test is run twice. During the first pass, the controller is set in a diagnostic mode such that error correction and detection is suspended and the 16 data bits are written and read without manipulation. During the second pass, the six ECC bits are written and read through the six most significant TILINE data channels, TLDAT00- through TLDAT05-.

Address Faults Test. If a functional data channel is found, the address faults plot will indicate faulty address lines in each row. Good addresses are denoted with periods, ".", failing addresses with "F".

Debug Routine. After the address faults plot, the operator is provided with three run commands for troubleshooting. The first is for the first or top row of 16K RAMs, the second for the second row of 16K RAMs, and the third for +5 Standby or Battery conditions. When transmitted, these commands result in a repetitive series of test cycles specifically for troubleshooting with an oscilloscope. At the top of the display, a write command is displayed for selecting the unit under test mode (data RAMs only with

Table 3-5. Cache Board to Tester Connections

Board Under Test	to	Memory Tester Interface
P1		J1
P2		J2
P3		[1]J3
P4		[1]J4

Note:

[1] J3 and J4 are ribbon cable connections. Arrows on mating connectors should be aligned with each other.

Figure 3-5. Board Error Map Representation for Cache Memory Controller Tests

ECC off, or ECC RAMs only in the bit swap mode).

3.7.1.4 Board Function Tests. Five board function tests are performed after the completion of the nominal march tests if the joystick is toggled "–" for performance. A description of the tests follows.

Expansion Interface Test. Data is supplied to add-on module memories via the expansion interface at MB00– through MB21–. A series of write data words are supplied to the TILINE interface while data at the expansion interface is tested. If a failure occurs, the BEM, TILINE data, and expected expansion interface data are displayed. A run continuous command is displayed for troubleshooting the failing condition. TILINE and expansion data displays should be interpreted as follows: TILINE = XXXX (where XXXX is hexadecimal representation, MSB to LSB, 16 binary bits); and EXPANSION I/F EXP DATA = OXXX OXXX (ignore zero positions and the two MSBs in leftmost X and interpret remaining Xs in hexadecimal, MSB to LSB, to provide 22 binary bits). For example, OCAA OFFF = OAA FFF or 00 1010 1010 1111 1111 1111.

Error Correction Test. A series of data words is supplied to the expansion interface with one bit (in varying position) in error. Data is measured at the TILINE interface and error correction must occur for each data and ECC bit for the test to pass. If a failure occurs, the BEM is displayed along with the expansion data word and TILINE expected data for the failing cycle. A run continuous command is provided for troubleshooting the failure.

Double Bit Error Detection. Two data words are supplied to the expansion interface, one with no error and one with two bits in error while TLMERR– at the TILINE interface is tested for false and true signal levels, respectively. If an error occurs, expansion interface data and the expected TLMERR– level is displayed. A run continuous command is provided for troubleshooting the failure.

Primary Memory Error LED Test. Errors are latched to light all primary memory error lamps (CR3 through CR13). The operator must verify that all LEDs are lighted and continue the test, power down, or use the oscilloscope if necessary. The test is looping continuously and may be observed with an osciloscope without a run command. Transmit the run command to continue the test or the command to power down after the operation of the LEDs has been verified.

+5 Standby Test. A checkerboard pattern is written to primary memory with error correction and cache on. A TLPRES– signal is issued and the +5 main supply is switched off. After several seconds, the +5 supply is switched back on, TLPRES– is set high, and the pattern is verified. To pass this test, the refresh circuit and the +5 switching circuit must function. This test can be observed with an oscilloscope using the run command on the debug display (see paragraph 3.7.1.3). Waveforms are provided in paragraph 3.7.2.6.

3.7.1.5 Primary Memory Performance Tests. Primary memory performance tests consists of march, checkerboard, refresh, GALROWCO-ROW, and GALROWCO-COL patterns. This series of tests is executed twice. Error correction is disabled during the first pass via the TILINE peripheral control space. The six correction bits are tested during the second pass (in the swap-bit mode). Each test is executed automatically, provided the previous test passes. If any test fails, the BEM, type of test, and power supply values are displayed followed by "J+ TO CONT; J– TO END". Joystick "+" will execute the next test; joystick "–" will result in a power-down.

CAUTION

Always power-down before attempting to remove memory chips from a board or when removing the board under test from the test interface fixture.

Each time a performance test passes, the type of test, "PASS", and the power supply values are displayed, and the next test is then executed.

Refresh Test. A checkerboard pattern is written to primary memory (with error correction and cache off). A wait period is then executed before the checkerboard pattern is verified. If the refresh circuits are not functioning, a failure will occur and the BEM will be displayed. The operator can continue or end the test with the joystick. The first half of the wait period has "no test" read cycles executed continuously, requiring the refresh controller to steal cycles at refresh intervals to perform refresh. For the second half of the wait period, no cycles (TLGO- is not activated) are issued and the refresh controller must latch refresh cycles without any cycles occurring simultaneously. The +5 main supply voltage is on during this test and the +5 switching circuit is not used.

3.7.1.6 Cache Memory Test Execution. Tests previously described are tests of the primary memory. Tests described in this paragraph are tests of the cache memory.

Cache Diagnostic. The cache diagnostic is a test to determine whether cache memory will hold data separate and different from primary memory. The diagnostic is executed six times, once on each of the four cache sections (bank A even, bank A odd, bank B even, and bank B odd) and twice on the full cache (1024 words). A pattern is written to memory with the cache on and then read to fill the cache. The cache is then turned off and primary memory is rewritten with a different (inverted) data pattern. The cache is then turned on again and the first pattern is verified. The pattern read should be the first one written, since all addresses should be stored in the cache (all cache HITs). Any address misses or parity errors and/or data parity errors will result in the inverted pattern being fetched from primary memory instead of the cache. The BEM and the results of the cache error latches will be displayed after each test is run.

Cache Error Information. If a failure occurs during any test of the cache, the operator is supplied with two types of error information: a BEM, as previously described, and a summary of cache error latch status. At this time, all primary memory tests should have passed. This means that any failures on the BEM do not refer to primary memory but to cache locations. In some cases, the BEM may show a failure while the error latches do not and vice versa. Careful interpretation of error information is important. If the caching sections determine an error, data will be returned from primary memory and the data may then be correct. The cache error latches then would be the only error indicator.

Cache Scoping Routine. After each of the six diagnostic tests have been executed, the operator has a choice of branching to the cache scoping routine or continuing the cache tests. If any errors were reported for any of the diagnostic tests, the operator may branch to the scoping routine to determine the nature of the failure. If no failures were reported, then the operator should use the joystick to continue the test. Waveforms for the scoping routines are provided in paragraph 3.7.2. Options are displayed for troubleshooting the cache data RAMs or the cache address storage RAMs. Options are also provided to restart the test, end the test, or restart the cache tests. Always end the test (power-down) before removing any memory chips from the board or before removing the board under test from the test interface fixture.

Cache March Performance Test. In the march performance test, a march pattern is executed on bank A and on bank B. Error information is provided on failures after each test.

Cache GALPAT Performance Test. A GALPAT pattern is executed twice on the full cache, once with low Vcc and once with high Vcc (that is, 4.75 and 5.25 volts, respectively).

Cache Address RAM March Performance Test. The cache address RAM march performance test results in a march pattern for the

cache address storage RAMs. The expansion interface is used repeatedly to store higher order addresses in the cache address storage RAMs. The test is executed first on bank A and then on bank B. The BEM and TPCS error latch status are displayed after each test.

Static Hold 1s Performance Test. In this test, a pattern is executed that stores logic 1s in cache bipolar static RAMs. A wait state is then executed (approximately 12 seconds) and the pattern is read to verify that the data has remained valid. The opposite data pattern is stored in primary memory so that if any MISS occurs because of address or data parity error or address inequality, an error will be logged on the BEM.

Static Hold 0s Performance Test. This test is the same as the static hold 1s performance test except that the data pattern stored is logic 0s.

3.7.2 Troubleshooting Primary Memory

The final diagnostic test for the primary section of the board under test, the debug routine, provides a run continuous command for each row. Each command results in a repetitive series of test cycles specifically designed for troubleshooting with an oscilloscope. Alternate 1s and 0s are applied to address and data for a write and a read cycle. The data and address words are then complemented, and a write is executed followed by a read as shown in the following example.

EXAMPLE 7

```
WRITE   DATA    WORD    ADDRESS
READ    DATA    WORD    ADDRESS

WRITE   DATA    WORD-   ADDRESS-
READ    DATA    WORD-   ADDRESS-
```

These four memory cycles are repeated continuously. A synchronizing signal occurring at the beginning of each series of four cycles is available at the memory tester control panel (CYCLE COUNT BNC). Refer to figure 3-6 for some specific waveforms and oscilloscope settings.

3.7.2.1 RAM Input/Output Timing. Refer to figure 3-7 for expanded timing waveforms at RAM inputs and outputs.

3.7.2.2 Refresh Timing. Refresh is performed asynchronously by the refresh oscillator and associated logic. See figure 3-8 for the expected waveform at the output of the oscillator (pin 6 of R12). External resistor R2, at pin 7 of S12, controls cycle time. To decrease cycle time, decrease the resistance of R2; to increase cycle time, increase the resistance of R2.

3.7.2.3 Delayed Timing Signals. The delayed timing signals, GO110 and GO130, should have the relationship to signal TLGO- as shown in figure 3-9. The RC delay network of R17, C3, and R12 (if installed) can be adjusted to obtain the expected time delay. If GO110 is less than the limits shown in figure 3-9, R12 can be removed from the circuit to increase the delay. If further adjustment is required, the value of R17 can be changed. Increasing resistance increases delay, decreasing resistance decreases delay. The RC delay network of R18, C4, and R13 (if installed) can be adjusted similarly to obtain the expected time delay for signal GO130.

3.7.2.4 Expansion Memory Signals. Signals IRAS-, ICAS-, and ICADSEL from the cache memory controller to the add-on expansion memory array board should have the relationship shown in figure 3-10. Proper adjustment of signals described in paragraph 3.7.2.3 will result in the required delay between signals IRAS- and ICADSEL.

3.7.2.5 Read Cycle, Write Cycle, Timing. Signals TLGO- and TLTM- should have the relationships shown in figure 3-11 for read cycles, read cycles with errors, and write cycles. After the memory tester has released TLGO-, the cache memory controller should release TLTM- within 60 nanoseconds as

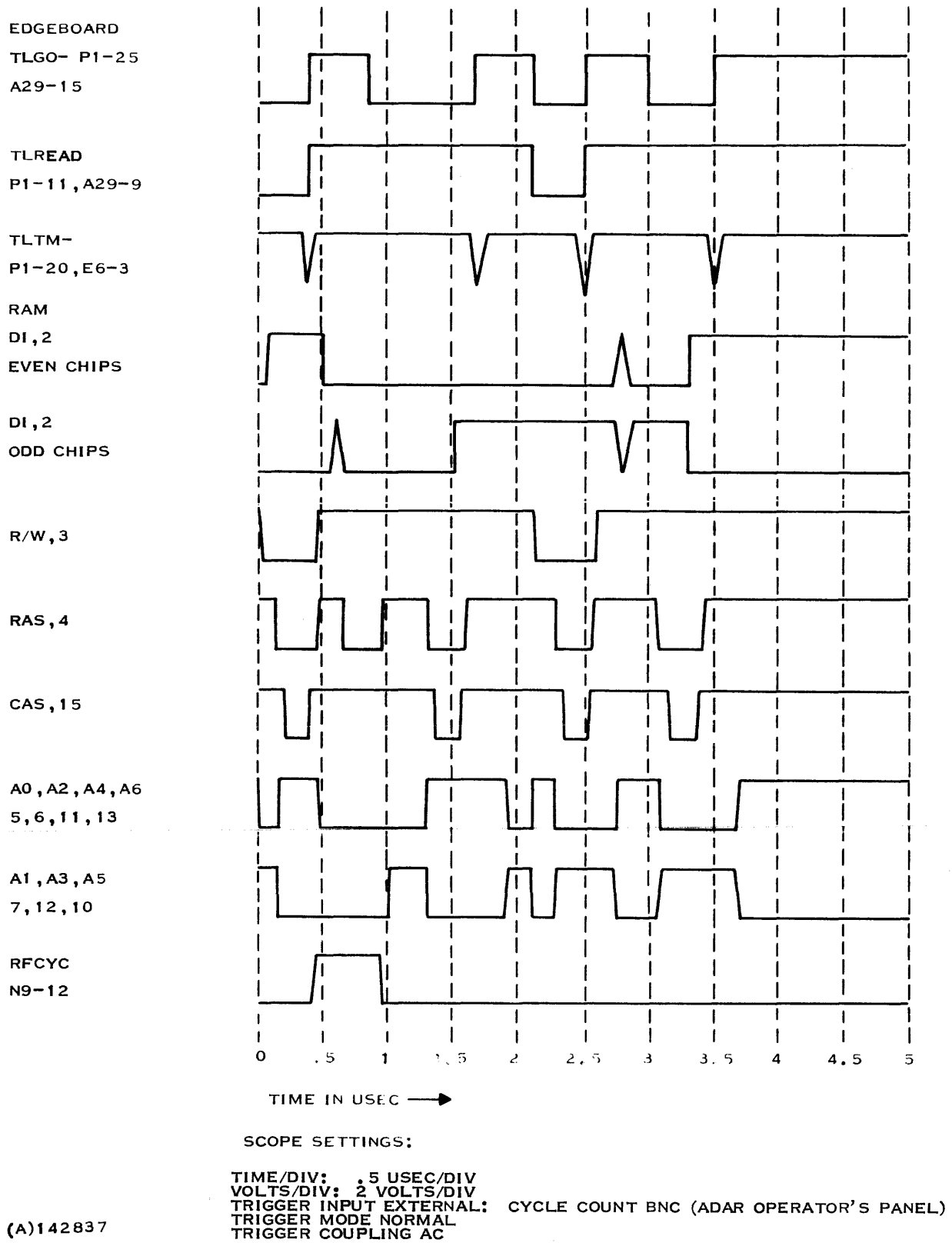
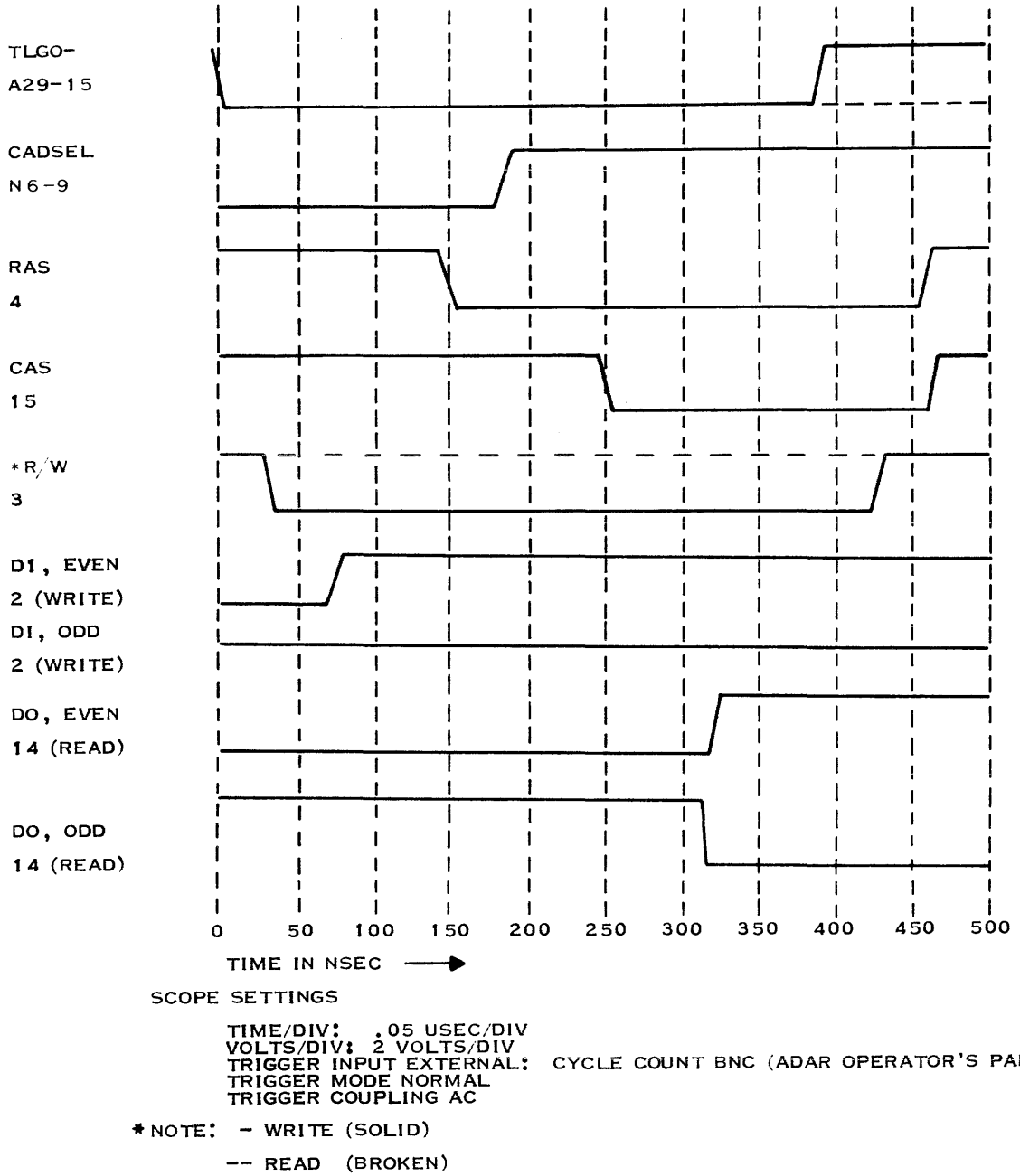
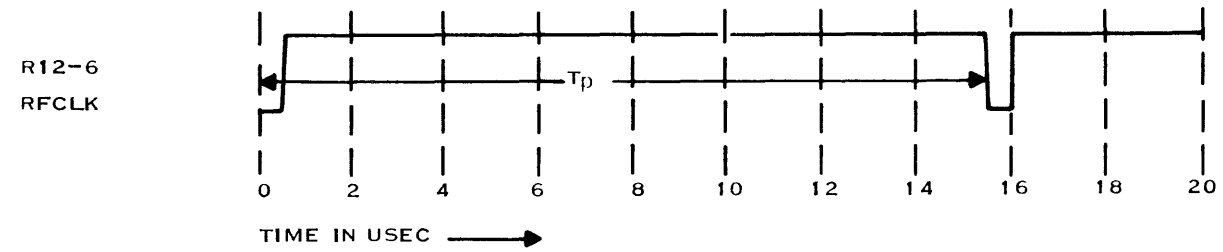


Figure 3-6. Debug Routine Waveforms



(A)142860

Figure 3-7. RAM Input/Output Waveforms



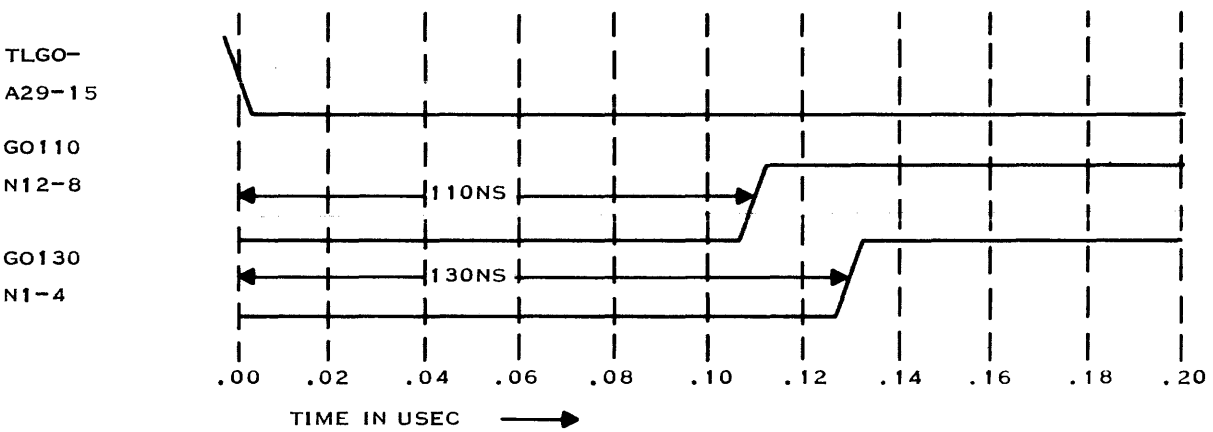
14.0 USEC < Tp < 15.5 USEC (AS A RESULT OF THIS SIGNAL RFCYC, N9-12, SHOULD OCCUR EVERY 15 USEC)

SCOPE SETTINGS

TIME/DIV: 2 USEC/DIV
VOLTS/DIV: 2 VOLTS/DIV
TRIGGER INPUT EXTERNAL: CYCLE COUNT BNC (ADAR OPERATOR'S PANEL)
TRIGGER MODE NORMAL
TRIGGER COUPLING AC
TRIGGER SOURCE: INPUT SIGNAL

(A)142865

Figure 3-8. Refresh Timing Waveform



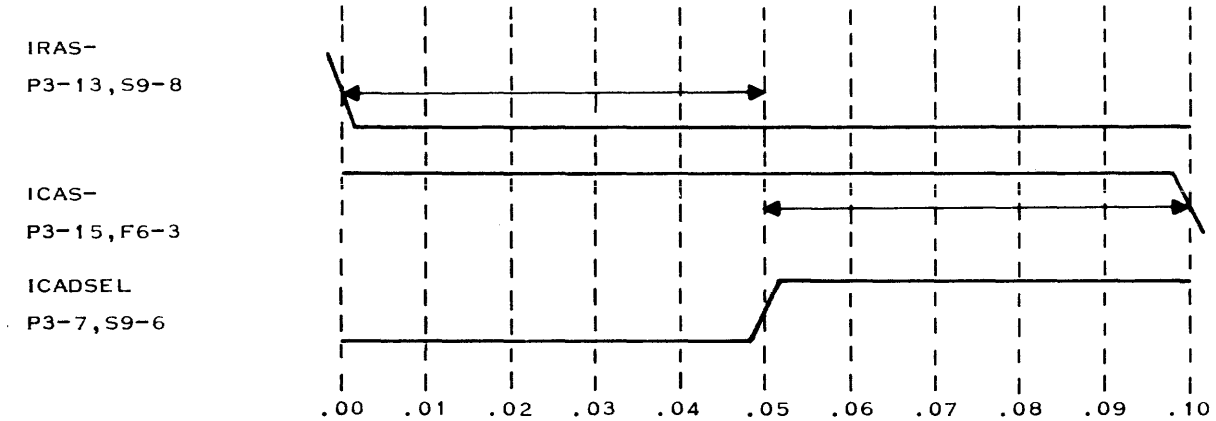
105NS < T(GO110) > 120NS
125NS < T(GO130) > 140NS
15NS < T(GO11C-GO130) > 25NS

SCOPE SETTINGS

TIME/DIV: .02 USEC/DIV
VOLTS/DIV: 2 VOLTS/DIV
TRIGGER INPUT EXTERNAL: CYCLE COUNT BNC (ADAR OPERATOR'S PANEL)
TRIGGER MODE NORMAL
TRIGGER COUPLING AC

(A)142864

Figure 3-9. Delayed Timing Signals Waveforms



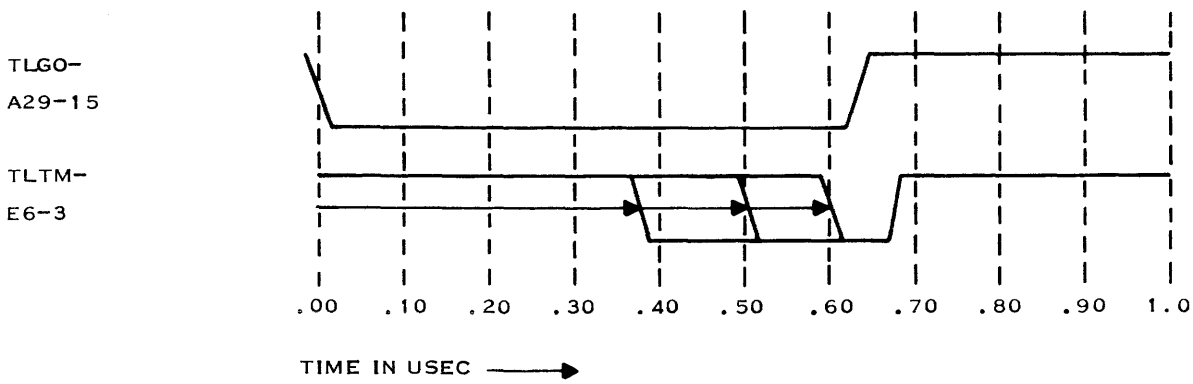
45NS < T(IRAS- TO ICADSEL) > 60NS
45NS < T(ICADSEL TO ICAS-) > 60NS

SCOPE SETTINGS

TIME/DIV: .01 USEC/DIV
VOLTS/DIV: 2 VOLTS/DIV
TRIGGER INPUT EXTERNAL: CYCLE COUNT BNC (ADAR OPERATOR'S PANEL)
TRIGGER MODE NORMAL
TRIGGER COUPLING AC

(A)142844

Figure 3-10. Expansion Memory Signals Waveforms



READ CYCLE 490NS < TP > 540NS*
READ CYCLE WITH ERROR 590NS < TP > 640NS*
WRITE CYCLES 365NS < TP > 400NS*

SCOPE SETTINGS

TIME/DIV: .10 USEC/DIV
VOLTS/DIV: 2 VOLTS/DIV
TRIGGER INPUT EXTERNAL: CYCLE COUNT BNC (ADAR OPERATOR'S PANEL)
TRIGGER MODE NORMAL
TRIGGER COUPLING AC

(A)142843

*NOTE: MINIMUM AND MAXIMUM VALUES BASED ON 110NS TLGO- TO GO110

Figure 3-11. Read and Write Cycles Timing Waveforms

shown in the expanded waveform of figure 3-12.

3.7.2.6 Main Power, Standby Power Signals. The waveforms of figure 3-13 show the relationships of signals to the main +5-volt supply, +5-volt standby or battery conditions. The relationships shown are for the initial loss of +5 main, duration of standby operation, and for reestablishment of +5 main.

3.7.3 Troubleshooting Cache Memory

Troubleshooting procedures and waveforms provided in paragraph 3.7.2 were for the memory controller with cache not enabled. This paragraph provides procedures for troubleshooting the board with the cache memory enabled. The debug routine for cache memory consists of a series of write and read cycles as shown in table 3-6.

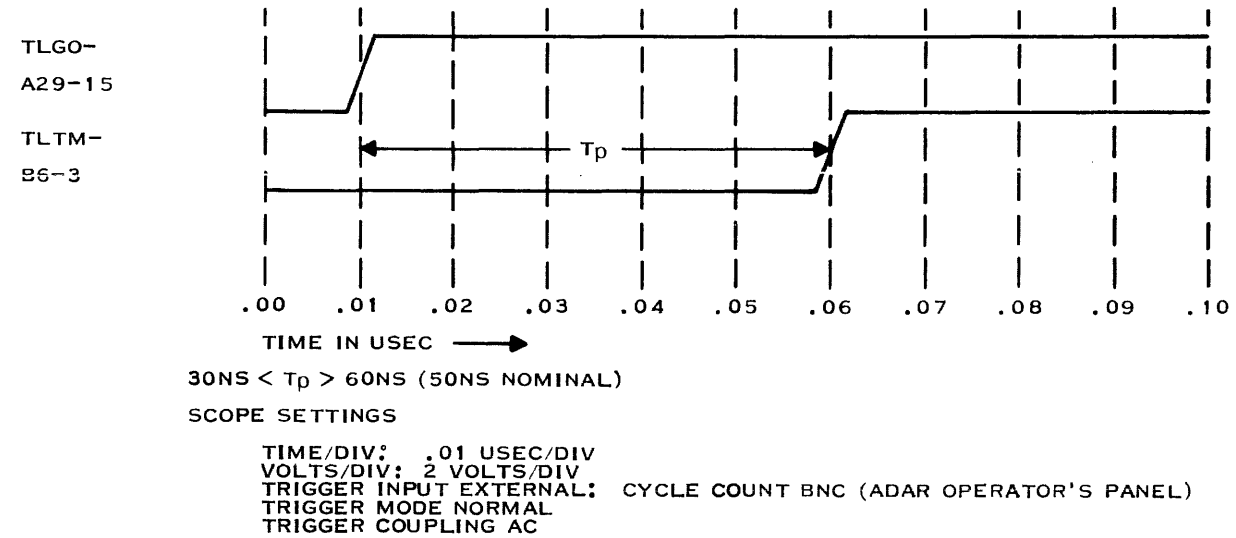


Figure 3-12. TLTM- Release, Expanded Waveform

Table 3-6. Algorithm Explanation for Cache Memory Debug Routine

1) CACHE MODE IS SET FROM TPCS FOR BANK A OR BANK B

2) TLADR19- IS SET
   A) HIGH—EVEN SECTION
   B) LOW—ODD SECTION
   NOTE: THIS ADDRESS WILL NOT CHANGE THROUGHOUT THE DEBUG ROUTINE.

3) ALGORITHM FOLLOWS

Cycle	OP	Stored Address	Index Address	Explanation of Cycle
1	WDW/	015	55	Write DW/ to primary memory 01 555.
2	RDW/	015	55	Read Primary DW/. This will store DW/ at cache index shown.
3	WDW	015	AA	Write DW to primary memory 01 5AA.
4	RDW	015	AA	Read primary DW. This will store DW at cache index shown.
5	RDW/	015	55	Read Cache DW/ from index shown. Fast access cache read.
6	RDW	015	AA	Read cache DW from index shown. Fast access cache read.
7	WDW	02A	55	Write primary DW to address shown.
8	RDW	02A	55	Read Primary DW. This will store DW at cache index shown, and change stored address at that index.
9	WDW/	02A	AA	Write primary DW/ to address shown.
10	RDW/	02A	AA	Read Primary DW/. This will store DW/ at cache index shown, and change stored address at that index.
11	RDW	02A	55	Read cache DW from index shown. Fast access cache read.
12	RDW/	02A	AA	Read cache DW/ from index shown. Fast access cache read.
13	WDW/	02A	55	Cache write-through.
14	WDW	02A	AA	Cache write-through.

Table 3-6. Algorithm Explanation for Cache Memory Debug Routine (Continued)

Cycle	OP	Stored Address	Index Address	Explanation of cycle

NOTES:
1) ALL ADDRESS WORDS GIVEN ARE POSITIVE TRUE VALUES (I.E. THE VALUE AT THE TILINE BUS IS THE INVERSE OF GIVEN ADDRESS.)

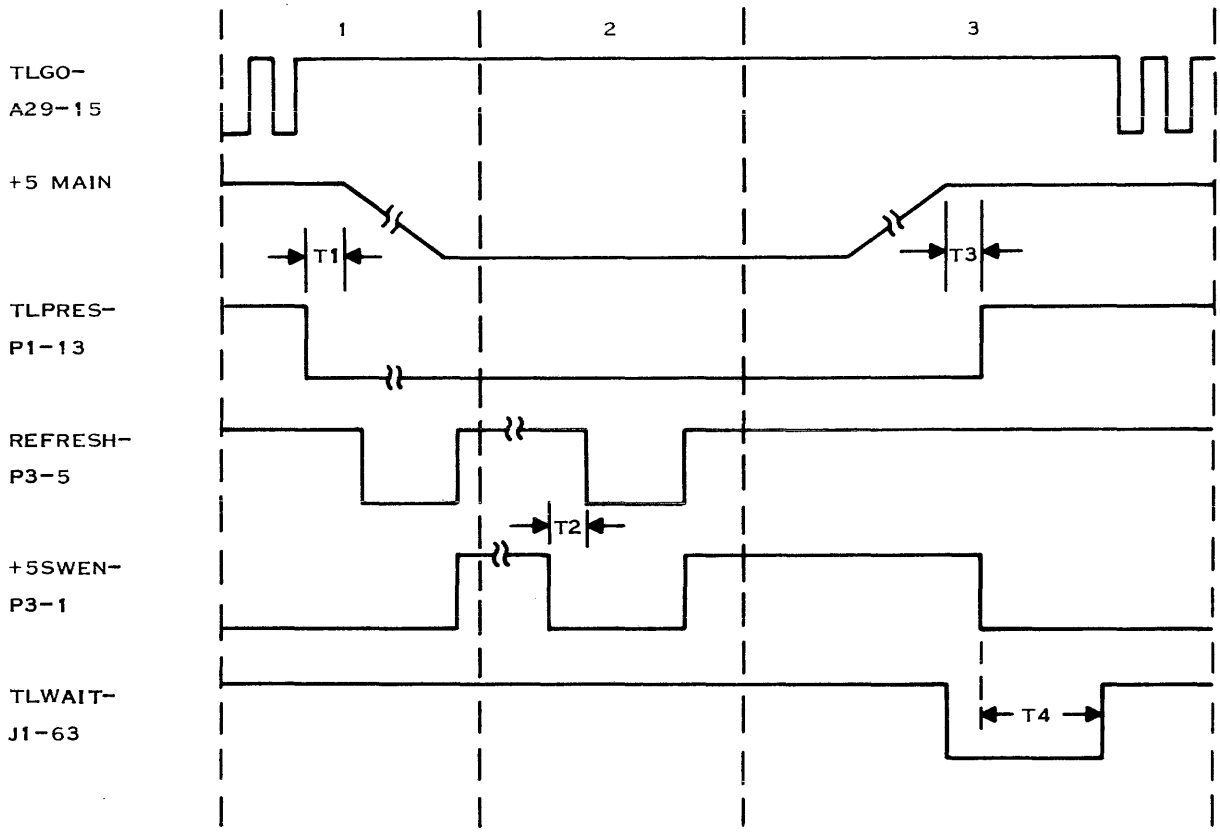
2) OP CODE EXPLANATION

WDW/—WRITE INVERTED DATA WORD	5555 (HEX)
WDW—WRITE DATA WORD	AAAA
RDW/—READ INVERTED DATA WORD	5555
RDW —READ DATA WORD	AAAA

3) INDEX ADDRESS IS TLADR11- (MSB) THRU TLADR18- (LSB)

4) STORED ADDRESS IS TLADR00- (MSB) THRU TLADR10- (LSB)

3.7.3.1 Cache Read Cycle with Cache Read Miss. The waveforms in figure 3-14 are for a cache read cycle with the accessed address not stored in the cache section (cache read miss). Data retrieved from primary memory is stored in cache memory along with the address and the word pair associated with the address. Waveforms shown in figure 3-14 are for bank A, even, only.

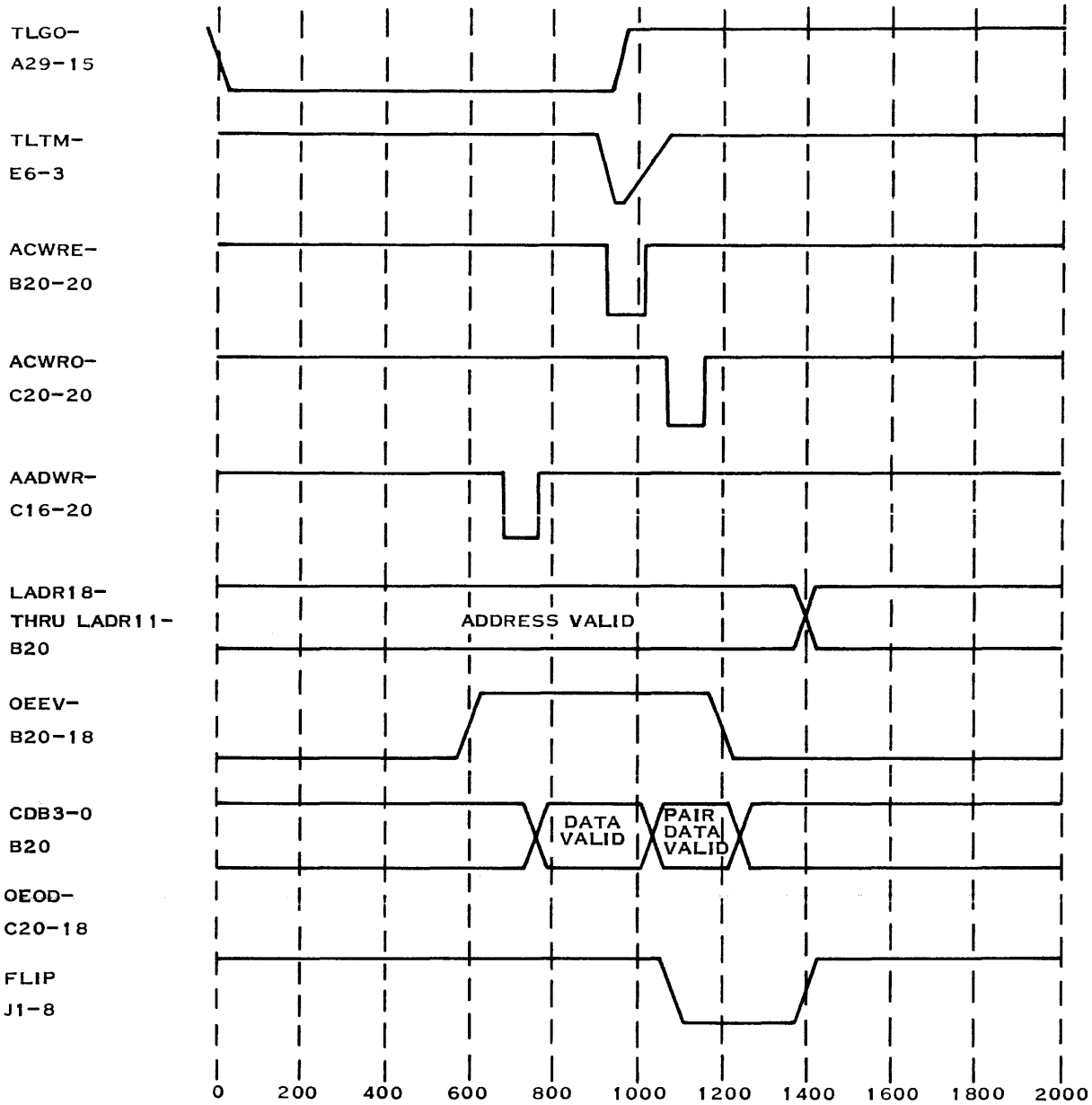


TI > 10US
490NS < T2 > 510NS
T3 > 0NS
7.8 MS < T4 > 8.0 MS

SECTION 1 - - END OF THE FIRST REFRESH CYCLE FOLLOWING TLPRES- TRUE, SWITCHES +5SWEN- OFF.
SECTION 2 - - FOR THE DURATION OF +5 MAIN POWER LOSS, REFRESH- AND +5SWEN- FOLLOW THE CYCLE SHOWN IN SECTION 2
SECTION 3 - - +5 MAIN IS RE-ESTABLISHED AS SHOWN IN SECTION 3

(A)142853

Figure 3-13. Waveforms for Standby Power Operation



SCOPE SETTINGS

CYCLE COUNT: 2,4,8, OR 10
TIME/DIV: .2 USEC/DIV
VOLTS/DIV: 2 VOLTS/DIV
TRIGGER INPUT EXTERNAL: CYCLE COUNT BNC (ADAR OPERATOR'S PANEL)
TRIGGER MODE NORMAL
TRIGGER COUPLING AC

(A)142856

Figure 3-14. Cache Read Cycle with Cache Miss, Waveforms

3.7.3.2 Cache Read Cycle with Cache Read Hit. The waveforms in figure 3-15 are for a cache read cycle with the accessed address stored in the cache section (cache read hit). Data is retrieved from the fast access cache data RAMs, and the primary memory read cycle is not initiated. This applies to cycles 5, 6, 11, and 12 in the debug routine (see table 3-6). Waveforms shown in figure 3-15 are for bank A, even, only.

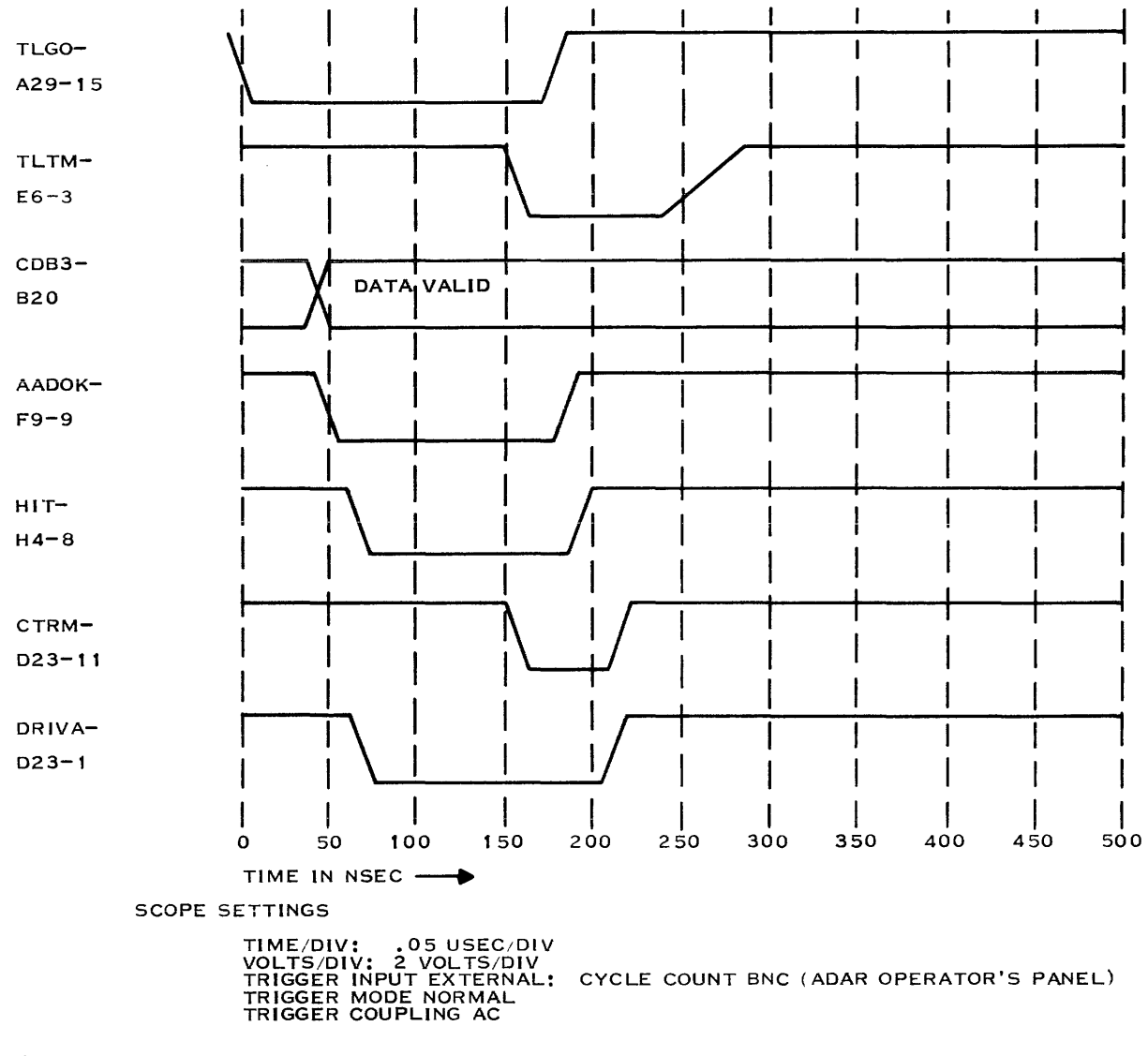


Figure 3-15. Cache Read Cycle with Cache Hit, Waveforms

3.7.3.3 Cache Write-Through cycle. Waveforms in figure 3-16 are for a write cycle with the accessed address stored in the cache section (cache write-through). Data is stored in both cache and primary data RAMs.

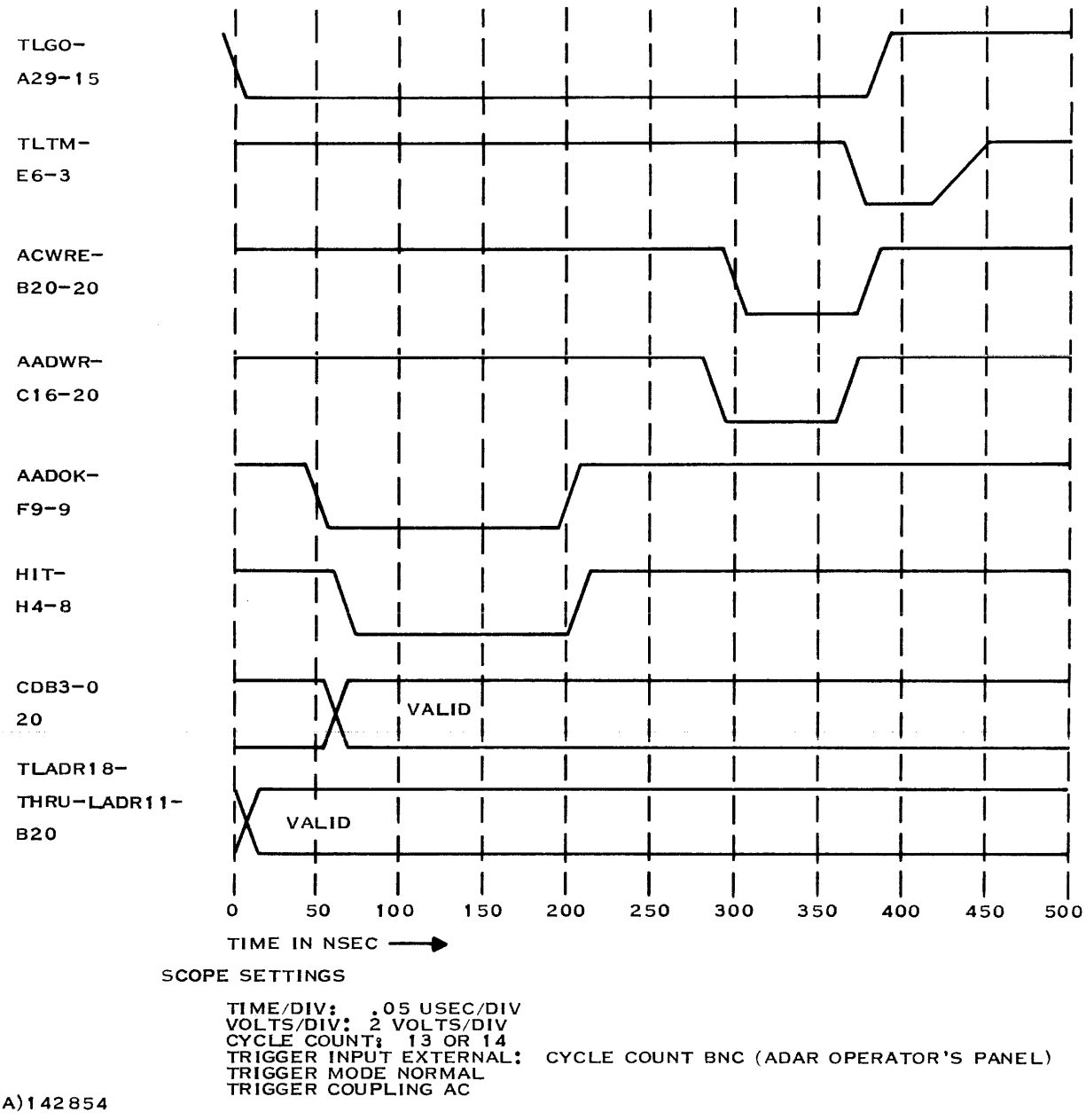


Figure 3-16. Cache Write-Through Cycle Waveforms

3.8 96KB MEMORY CONTROLLER CHECK-OUT AND TROUBLESHOOTING PROCEDURES USING MEMORY TESTOR

Instructions are provided in this paragraph for performing a checkout of the 96KB memory controller in standard and fine line versions, using a memory testor. Additionally, useful troublehsooting procedures are provided along with waveform representation of the board in various modes of operation. Test equipment required to perform the memory board checkout procedures is listed in table 3-7.

3.8.1 Memory Test of 96KB Memory Controller.

Verify that the test equipment as listed in table 3-7 is currently certified, and perform the test of the 96KB memory controller using the Adar memory tester as follows.

1. On the Adar memory tester, press the REM and RSI/RDS power switches in that order (red switch lights should be off). Install the memory tester interface for the 96KB memory controller (part number 2264815-0001). Press the RSI/RDS and REM power switches, in that order, (red switch lights should be on).
2. On the Adar memory tester, set RSI switches 1, 4, and 8 to the ON position and switches 2, 3, 5, 6, and 7 to the OFF position.
3. Load the program tape, 48CONT (TESTTS, ARRYTA). Enter "*RFI 48CONT CAS" and press the XMIT key at the Adar memory tester data terminal.
4. Install the 96KB memory controller board to be tested into the memory tester interface with component side of the board facing the operator of the memory tester. Make connections as shown in table 3-8.
5. Perform visual check. Ensure that all DIP switches on the board under test are in the off position. Scan the board under test for solder shorts.
6. Note the dash number of the board under test and ensure that the jumper configuration for jumpers J9 and J10 and the number of rows of memory chips agree with that shown in table 3-9.

Table 3-7. Test Equipment Required for 96KB Memory Controller Checkout Using Memory Tester

Item	Texas Instruments Part Number
Adar Model DR12/25 Memory Test System Tester	2264826-0001
Memory Tester Interface, 96KB Memory Controller	2264815-0001
Oscilloscope, Tektronix Model 475 (or equivalent)	
Multimeter	
10X Probes with Grounding Clips	
Coaxial Cable with BNC to BNC Connectors	
Program Tape 48CONT (TESTTS, ARRYTA)	

3.8.1.1 Memory Test Execution. The memory test is started by entering "*R 0 0" and pressing the XMIT key at the Adar memory tester data terminal. The memory tester will respond with "J+ TO START". After toggling the switch to the right (J+), the memory tester responds with "J+ FOR DIAG; J- FOR PERF" on the data terminal CRT. On the first pass, toggle the joystick to J- to start the performance tests. If the board under test fails the first test (a march test), the BEM will be displayed, followed by "J+ TO CONT; J- TO END". The operator should then end the test with J-, restart with J+, and run the diagnostic tests with J+ as directed by the CRT messages. If the board under test passes the first test, a pass condition will be indicated along with the type of test and the values of Vcc, Vbb, and Vdd. The remaining tests will be run automatically provided the preceding test passes. If any test fails, the BEM, type of test, and power supply values will be displayed, followed by "J+ TO CONT, J- TO EXIT". Setting the joystick to "J+" continues the next test; setting the joystick to "J-" will end the test. Always end the test before removing the board under test or before replacing memory chips.

3.8.1.2 96KB Memory Controller Board Error Maps (BEM). The BEM is provided as a CRT display at the data terminal of the memory tester. As shown in figure 3-17, the BEM represents the memory array. Memory read errors are logged at speed during any given test, and at the end of each test the BEM displays any chip failures. The good chips are represented with asterisks, whereas

Table 3-8. 96KB Board to Tester Connections

Board Under Test	to	Memory Tester Interface
P1		J1
P2		J2
P3		[1]J3
P4		[1]J4

Note:

[1] J3 and J4 are ribbon cable connections. Arrows on mating connectors should be aligned with each other.

Table 3-9. 96KB Memory Size Jumper Schedule

Part Number	Memory Size	J9	J10
2261980-0002	32KB	OFF	ON
2261980-0006	32KB	OFF	ON
2261980-0003	64KB	ON	OFF
2261980-0007	64KB	ON	OFF
2261980-0004	96KB	ON	ON
2261980-0008	96KB	ON	ON

failing memory chips are indicated by the reference designator of the failing chip. The BEM is interpreted as follows:

1. The first three rows of the BEM represent the 16K RAMs at reference designations N4 through N19 (first row), M4 through M19 (second row), and L4 through L19 (third row). The asterisks are replaced by the corresponding reference designator as a failure occurs.

2. The next three rows of the BEM represent the 16K RAMS in the error correction code memory at reference designations N20 through N25 (first row), M20 through M25 (second row), and L20 through L25 (third row).

3. The next two rows of the BEM represent the data channels at the expansion interface, MB00- through MB21- (odd-numbered pins 1 through 43 of connector P4). As failures occur, MB00- is represented by B00, MB01- as B01, etc.

4. The last row of the BEM is enabled during the test for error correction. Each position represents one of the TILINE data channels TLDAT00- through TLDAT15-. As failures occur, the asterisks are replaced by B00 (TLDAT00-) through B15 (TLDAT15-).

3.8.1.3 96KB Memory Controller Diagnostic Tests. The following is a description of memory controller diagnostic tests.

Existence Test. The existence test is run automatically after the joystick is toggled to "J+". A BEM will indicate any functioning memory chips. This test is run twice. During the first pass, the controller is set in a diagnostic mode such that error correction and detection is suspended and the sixteen data bits are written and read without manipulation. During the second pass, the six correction bits are written through the six most significant TILINE data channels, TLDAT00- through TLDAT05-.

Address Faults Test. If a functional data channel is found, the address faults plot will indicate faulty address lines in each row.

Debug Routine. After the address faults plot, the operator is provided with three commands for troubleshooting. The first is for the memory with error correction disabled; the second, for the error correction banks only. When transmitted, these commands result in a repetitive series of test cycles specifically for troubleshooting with an oscilloscope. Near the bottom of the display, a modification can be made to choose a given row in memory. Follow the CRT commands for setup. The last command provided

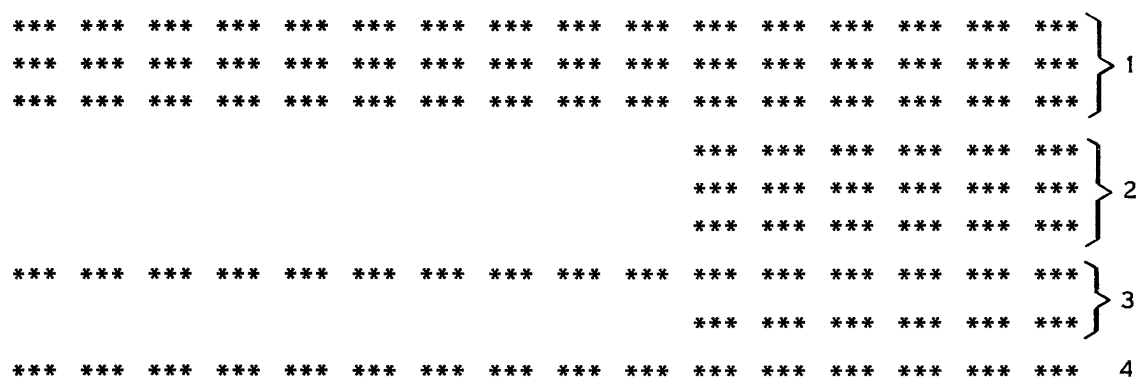


Figure 3-17. Board Error Map Representation for 96KB Memory Controller Tests

allows the operator to troubleshoot with the memory controller under standby conditions.

3.8.1.4 96KB Memory Performance Tests. Memory performance tests consist of march, checkerboard, rotate data word, increment data word, ping pong, GALROWCO-ROW, GALROWCO-COL, and diagonal patterns. This series of tests is executed twice. Error correction is disabled during the first pass via a diagnostic mode. The six correction bits are tested during the second pass.

3.8.1.5 96KB Memory Board Function Tests. Four board function tests are performed after the completion of the performance tests. First, data is written to the controller and tested at the expansion interface. Second, a series of data words with one bit in error is read through the expansion interface, expecting corrected data at the TILINE interface. Then the board under test is exercised in its normal operating mode (error correction enabled) with a march pattern. The last board function test, the +5 standby test, simulates operation under battery power (+5 MAIN supply at 0 volts).

3.8.2 Troubleshooting 96KB Memory Controller

The final diagnostic test for the memory controller, the debug routine, provides a run continuous command for each row. Each command results in a repetitive series of test cycles specifically designed for troubleshooting with an oscilloscope. Alternate 1s and 0s are applied to address and data for a write and a read cycle. The data word is then complemented and a write cycle is executed followed by a read cycle. The address is then complemented and the four cycles are repeated with the data word and its complement as shown in the following example.

EXAMPLE 7

WRITE	DATA	WORD	ADDRESS
READ	DATA	WORD	ADDRESS
WRITE	DATA	WORD-	ADDRESS
READ	DATA	WORD-	ADDRESS
WRITE	DATA	WORD	ADDRESS-
READ	DATA	WORD	ADDRESS-
WRITE	DATA	WORD-	ADDRESS-
READ	DATA	WORD-	ADDRESS-

The eight memory cycles are repeated continuously. A synchronizing signal occurring at the beginning of each series of eight cycles is available at the memory tester control panel (CYCLE COUNT BNC). Refer to figure 3-18 for some specific waveforms and oscilloscope settings.

3.8.2.1 96KB Memory Controller RAM Input/Output Timing. Refer to figure 3-19 for expanded timing waveforms at RAM inputs and outputs.

3.8.2.2 96KB Memory Controller Refresh Timing. Refresh is performed asynchronously by the refresh oscillator and associated logic. See figure 3-20 for the expected waveform at test point 1. Adjust the value of resistor R28 (15K ohms) or resistor R26 (47K ohms) if necessary. For a faster cycle time, subtract resistance from R28 or add resistance to R26. For a slower cycle time, add resistance to R28 or subtract resistance from R26.

3.8.2.3 96KB Memory Controller Delayed Timing Signals. The delayed timing signals, GO120 and GO170, should have the relationship to TLGO- as shown in figure 3-21. The RC delay networks of R11, R46, C96 and R12, R45, C86 can be adjusted to obtain the ex-

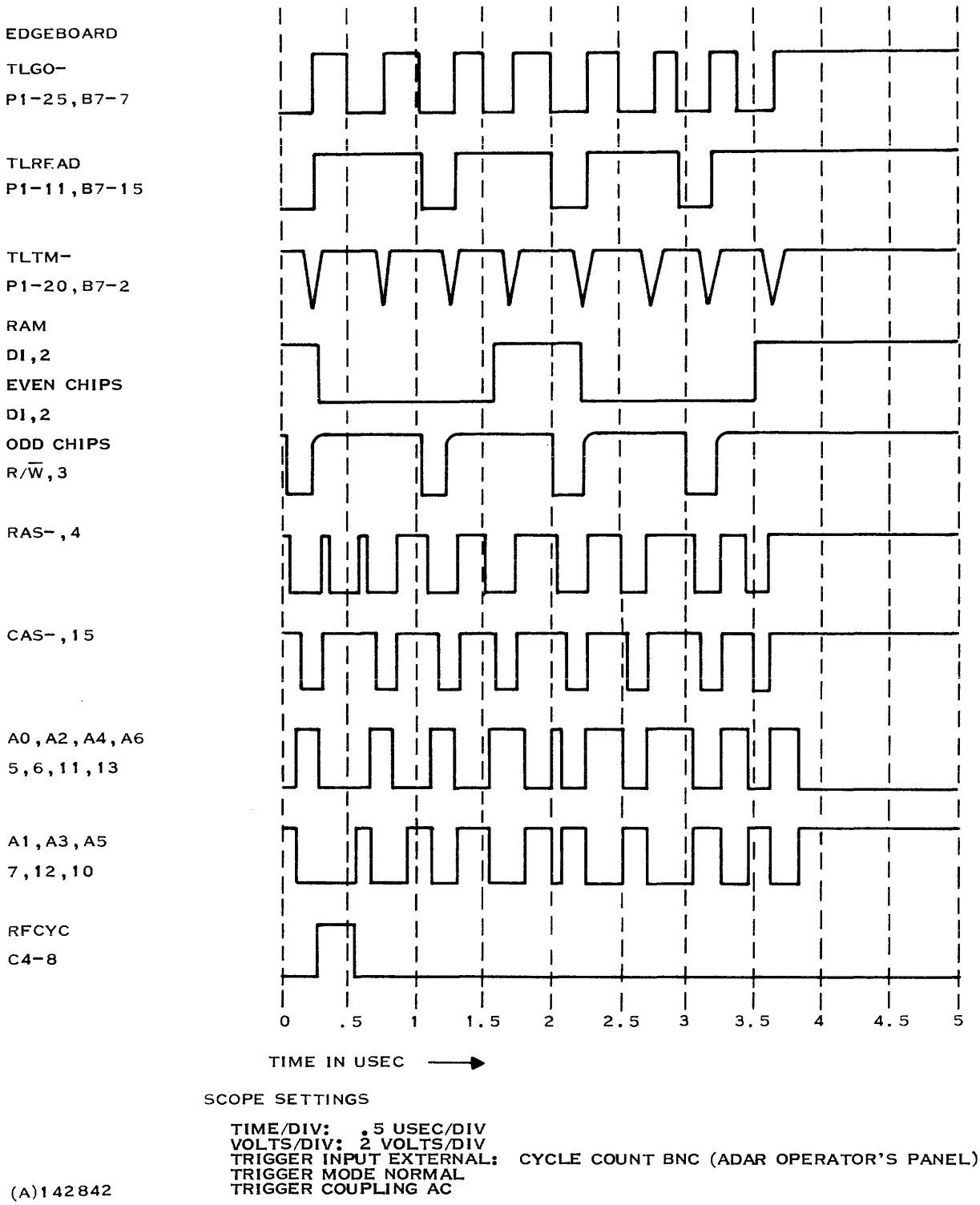


Figure 3-18. 96KB Memory Controller Debug Routine Waveforms

pected time delays. If GO120 delay is less than the limits, R46 can be removed from the circuit to increase the delay. Similarly, if GO170 delay is less than required, R45 can be removed from the circuit. If further adjustment is required, the values of R11 or R12 can be changed. Increasing resistance increases delay; decreasing resistance decreases delay.

3.8.2.4 96KB Memory Controller Expansion Memory Signals. Signals IRAS-, ICAS-, and ICADSEL from the 96KB memory controller to the add-on expansion memory array board should have the relationship shown in figure 3-22. In order to obtain the minimum delay of 45 nanoseconds between ICADSEL and ICAS-, selection of IC devices at locations J2, J4, or K2 may be required.

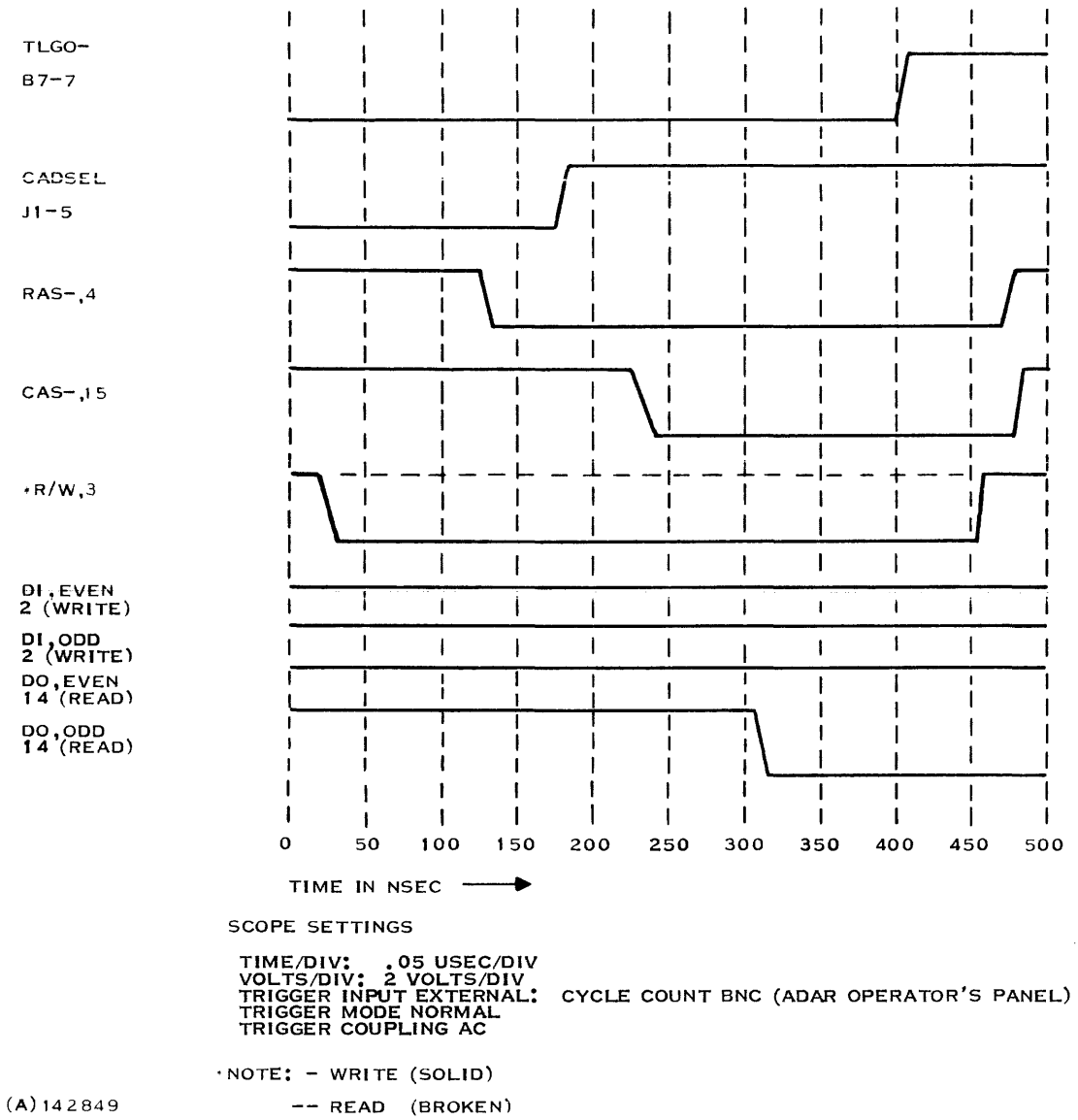
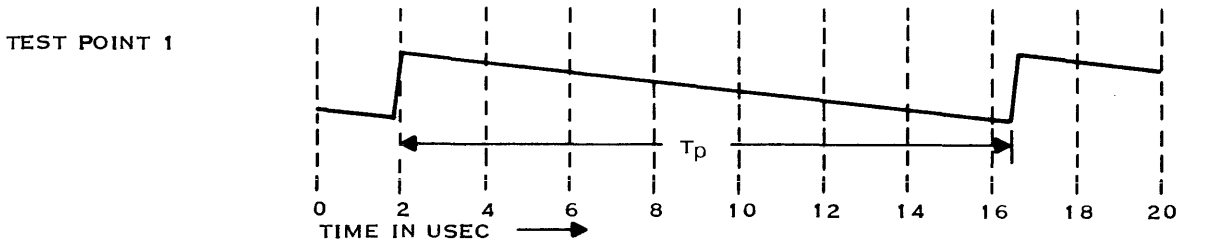


Figure 3-19. 96KB Memory Controller RAM Input/Output Timing Waveforms



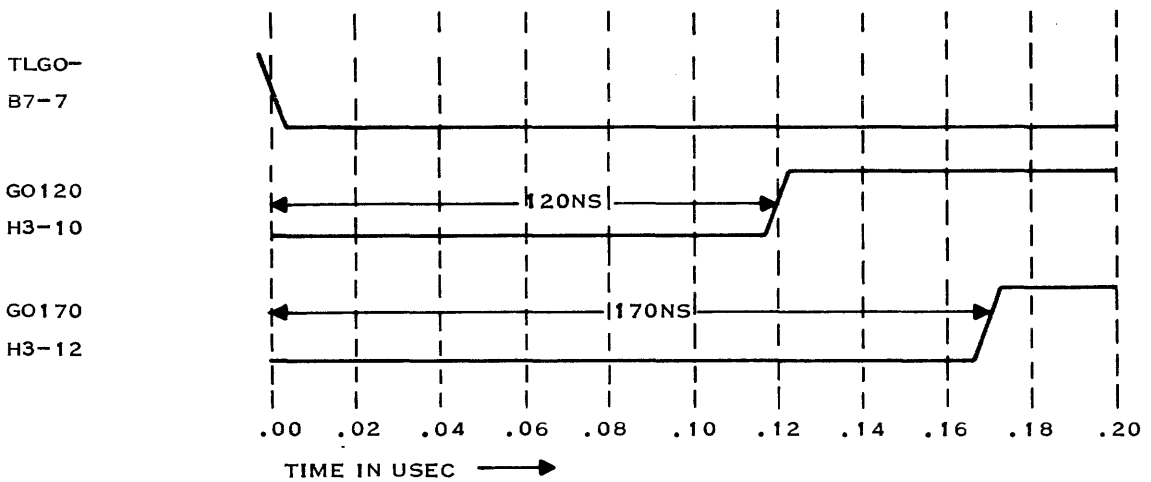
14.0 USEC < T_D > 15.5 USEC (AS A RESULT OF THIS SIGNAL RFCYC. A01-23, SHOULD OCCUR EVERY 15 USEC)

SCOPE SETTINGS

TIME/DIV: 2 USEC/DIV
VOLTS/DIV: 2 VOLTS/DIV
TRIGGER INPUT EXTERNAL: CYCLE COUNT BNC (ADAR OPERATOR'S PANEL)
TRIGGER MODE NORMAL
TRIGGER COUPLING AC

(A)142846

Figure 3-20. 96KB Memory Controller Refresh Timing Waveform



110NS < T(GO120) > 130NS
160NS < T(GO170) > 180NS
45NS < T(GO120-GO170) > 55NS

SCOPE SETTINGS

TIME/DIV: .02 USEC/DIV
VOLTS/DIV: 2 VOLTS/DIV
TRIGGER INPUT EXTERNAL: CYCLE COUNT BNC (ADAR OPERATOR'S PANEL)
TRIGGER MODE NORMAL
TRIGGER COUPLING AC

(A)142847

Figure 3-21. 96KB Memory Controller Delayed Timing Signals

3.8.2.5 Pulse Waveforms for 250-Nanosecond Delay. Pulse waveforms at the output of the 250-nanosecond delay devices are shown in figure 3-23.

3.8.2.6 Timing for Read/Write Cycles. Figure 3-24 shows the relationship between signals TLGO- and TLTM- for a read cycle free of errors, a read cycle with errors, and a write cycle.

3.8.2.7 TLGO- Release Time. After the memory tester has released TLGO-, the 96KB memory controller should release the signal TLTM- within 60 nanoseconds, as shown in figure 3-25.

3.8.2.8 96KB Main Power, Standby Power Signals. The relationship between main power and standby power for the 96KB memory controller is the same as that shown for the cache memory controller in figure 3-13. Signal TLGO- is at pin 7 of device B7 for the 96KB memory controller.

3.9 256KB ADD-ON MEMORY ARRAY CHECKOUT AND TROUBLESHOOTING PROCEDURES USING MEMORY TESTER

Instructions are provided in this paragraph for performing a checkout of the 256KB add-on memory array using a memory tester. Additionally, useful troubleshooting procedures are provided along with waveform representation of the board in various modes of operation. Test equipment required to perform the checkout procedures is listed in table 3-10.

3.9.1 Memory Test of 256KB Add-On Memory Array

Verify that the test equipment as listed in table 3-10 is currently certified and perform the test of the 256KB add-on memory array using the Adar memory tester as follows.

1. On the Adar memory tester, press the REM and RSI/RDS power switches, in that order (red switch lights should be

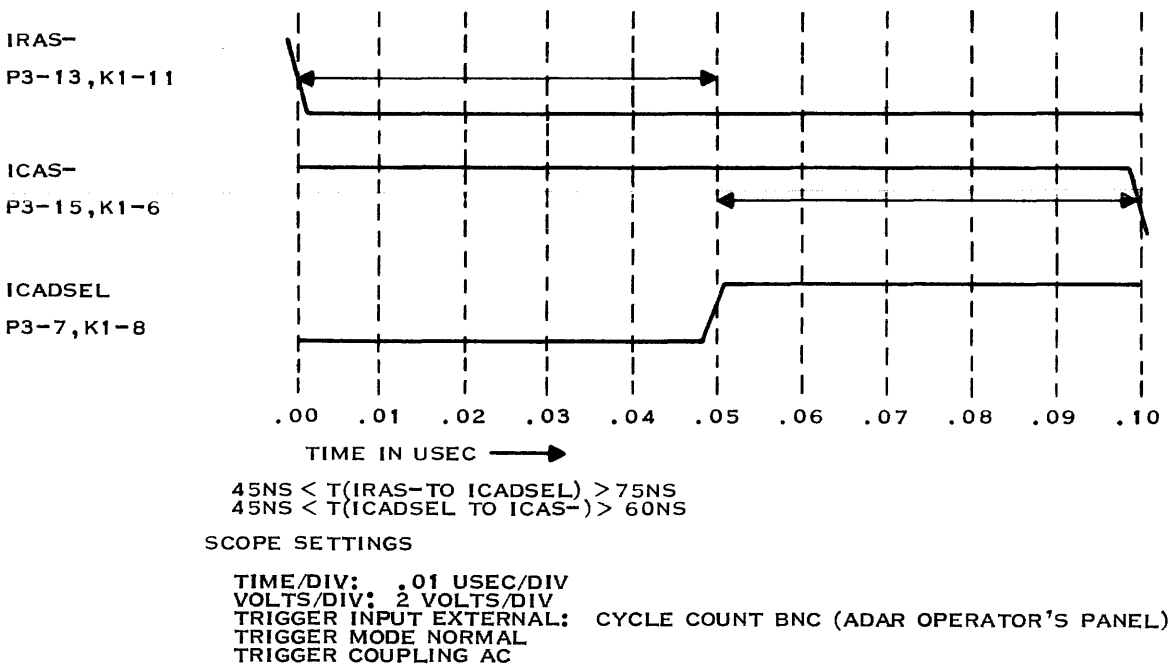


Figure 3-22. 96KB Memory Controller Expansion Memory Signals

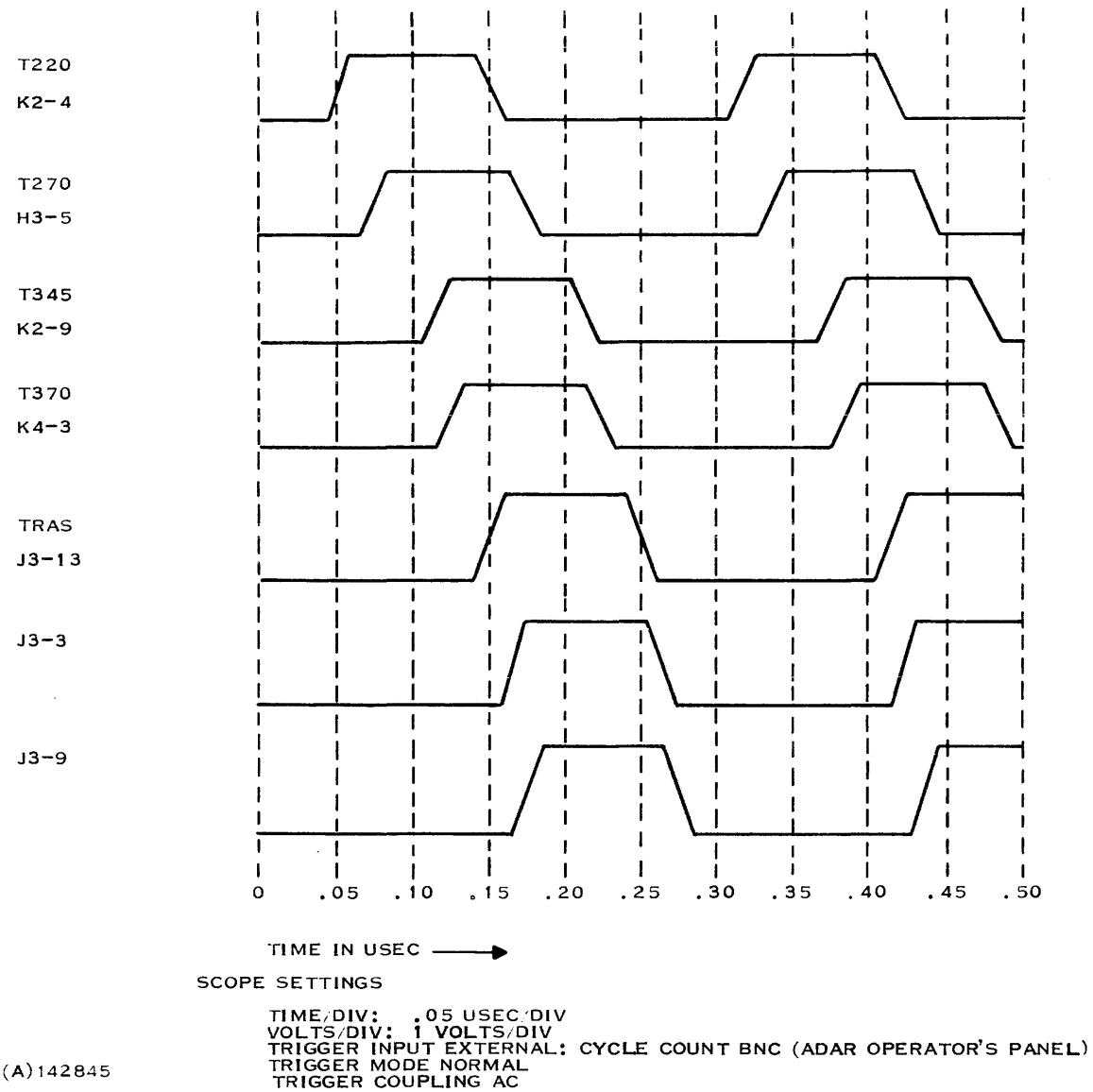
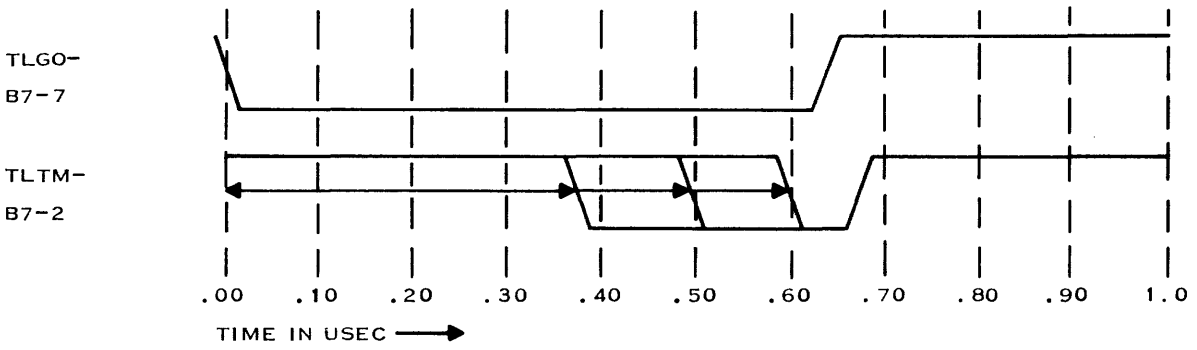


Figure 3-23. 250-Nanosecond Delay Devices Output Signals Waveforms



READ CYCLE 490NS < Tp > 540NS*
READ CYCLE WITH ERROR 590NS < Tp > 640NS*
WRITE CYCLES 365NS < Tp > 400NS*

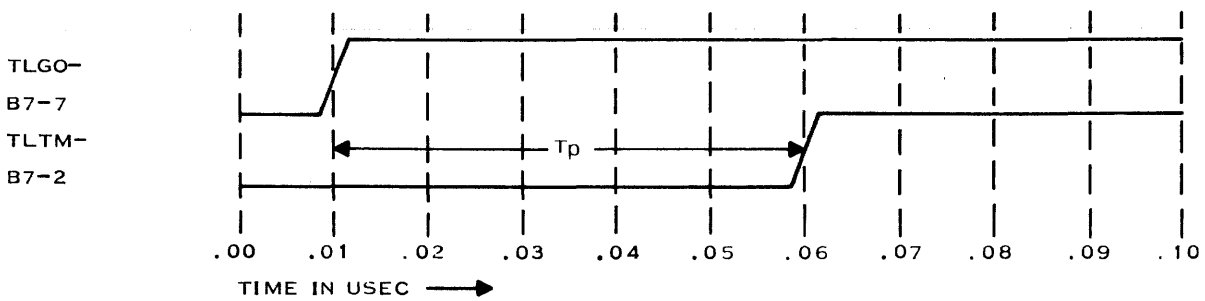
SCOPE SETTINGS

TIME/DIV: .10 USEC/DIV
VOLTS/DIV: 2 VOLTS/DIV
TRIGGER INPUT EXTERNAL: CYCLE COUNT BNC (ADAR OPERATOR'S PANEL)
TRIGGER MODE NORMAL
TRIGGER COUPLING AC

*NOTE: MINIMUM AND MAXIMUM VALUES BASED ON 170NS TLGO- TO GO170

(A)142852

Figure 3-24. Read/Write Cycle Timing



30NS < Tp > 60NS (50NS NOMINAL)

SCOPE SETTINGS

TIME/DIV: .01 USEC/DIV
VOLTS/DIV: 2 VOLTS/DIV
TRIGGER INPUT EXTERNAL: CYCLE COUNT BNC (ADAR OPERATOR'S PANEL)
TRIGGER MODE NORMAL
TRIGGER COUPLING AC

(A)142850

Figure 3-25. TLTM- Release Time

off). Install the memory tester interface for the 256KB add-on memory array (part number 2264815-0002). Press the RSI/RDS and REM power switches, in that order (red switch lights should be on).

2. On the Adar memory tester, set RSI switches 1, 2, and 8 to the ON position and switches 3 through 7 to the OFF position.

3. Load the program tape, 128EXP (TESTTS, ARRYTA). Enter "*RFI 128EXP CAS" and press the XMIT key at the Adar memory tester data terminal. Then load the calibration tape, CALRST. Enter "*RFI CALRST CAS" and press the XMIT key. The CRT will display "REQUEST COMPLETE" to indicate that calibration is complete.

4. Install the 256KB add-on memory array board to be tested into the memory tester interface with component side of the board facing the operator of the memory tester. Make connections as shown in table 3-11.

5. Perform visual check. Ensure that DIP switches on the board are all in the off position. Scan the board under test for solder shorts.

6. Note the dash number of the board under test and ensure that the jumper configuration for jumpers J9 and J10 and the number of rows of memory chips agree with that shown in table 3-12.

3.9.1.1 256KB Add-On Memory Array Memory Test Execution. The memory test is started by entering "*R 0 0" and pressing the XMIT key at the Adar memory tester data terminal. The operator should then follow the instructions on the data terminal CRT for program setup and use the toggle switch labeled JOYSTICK on the memory tester control panel to run the first board test. When the joystick is toggled, the nominal march test is run and the resulting board error map (BEM) is displayed. The operator then must use the joystick to choose between diagnostic or performance tests. The statement "J+ FOR DIAG ; J- FOR PERF" will appear on the CRT, and the operator must toggle the joystick to

Table 3-10. Test Equipment Required for 256KB Add-On Memory Array Checkout Using Memory Tester

Item	Texas Instruments Part Number
Adar Model DR12/25 Memory Test System Tester	2264826-0001
Memory Tester Interface, 256KB Add-On Memory Array Board	2264815-0002
Oscilloscope, Tektronix Model 475 (or equivalent)	
Multimeter	
10X Probes with Grounding Clips	
Coaxial Cable with BNC to BNC Connectors	
Program Tape 128EXP (TESTTS, ARRYTA)	

"+" or "-" as applicable. If the memory under test fails the nominal march test, the diagnostic tests should be run. The performance tests should be run if the board under test passes the nominal march test.

3.9.1.2 256KB Add-On Memory Array Board Error Maps (BEM). The BEM is provided as a CRT display at the data terminal of the memory tester. As shown in figure 3-26, the BEM represents the memory array. Memory read errors are logged at speed during any given test, and at the end of each test the BEM displays any chip failures. The good chips are represented with asterisks whereas failing memory chips are indicated by the reference designator for the failing chip. The BEM is interpreted as follows:

1. Each row of memory chips on the 256KB add-on memory array is represented by two rows in the BEM. Rows one through eight are ordered vertically, top to bottom, on the BEM just as they appear on the board under test. The first row of asterisks in figure 3-26 represents the 16K MOS RAMs in the top row of the memory board (data bits positions 0 through 15, left to right). The second row of the BEM represents the RAMs in data bit positions 16 through 21 (also in the top row of memory). This represen-

Table 3-11. 256KB Board to Tester Connections

Board Under Test	to	Memory Tester Interface
P1		J1
P2		J2
P3		[1]J3
P4		[1]J4

Note:

[1] J3 and J4 are ribbon cable connections. Arrows on mating connectors should be aligned with each other.

Table 3-12. 256KB Memory Size Jumper Schedule

Part Number	Memory Size (Bytes)	J9	J10
948955-0001	64K	OFF	ON
948955-0002	128K	ON	OFF
948955-0003	192K	ON	ON
948955-0004	256K	OFF	OFF

tation is implemented for each of the eight rows. For board assemblies with less than eight rows of memory implemented, the unused portion of the BEM can be ignored.

2. As failures occur in the first row of memory, the asterisks in the first row of the BEM are replaced by 100 (bit 0, first row) through 121 (bit 21, first row). The BEM as shown in figure 3-26 indicates that all of the memory chips in the fourth row have failed.

3.9.1.3 256KB Add-On Memory Array Diagnostic Tests. The following is a description of 256KB add-on memory array diagnostic tests.

Existence Test. The existence test is run automatically after the joystick is toggled to "J+" for the diagnostic tests. A BEM will indicate functioning memory chips. The operator should continue to toggle the joystick as directed by messages on the CRT.

Address Faults Test. If a functional data channel is found, the address faults plot will indicate faulty address lines in each row. As described in paragraph 2.2.1, the address inputs for the TMS4116 memory chip are multiplexed. The address faults display shows chip row addresses R0 through R6 and column addresses C0 through C6. These chip addresses correspond to the edgeboard addresses as follows:

R0 TLADR11 P2-12
R1 TLADR10 P2-10
R2 TLADR09 P2-19
R3 TLADR08 P2-17
R4 TLADR07 P2-49
R5 TLADR06 P2-47
R6 TLADR05 P2-59
C0 TLADR18 P2-25
C1 TLADR17 P2-27
C2 TLADR16 P2-29
C3 TLADR15 P2-9
C4 TLADR14 P2-8
C5 TLADR13 P2-15
C6 TLADR12 P2-11

Debug Routine. The debug routine provides a series of Run Continuous commands that may be executed, one for each of the eight

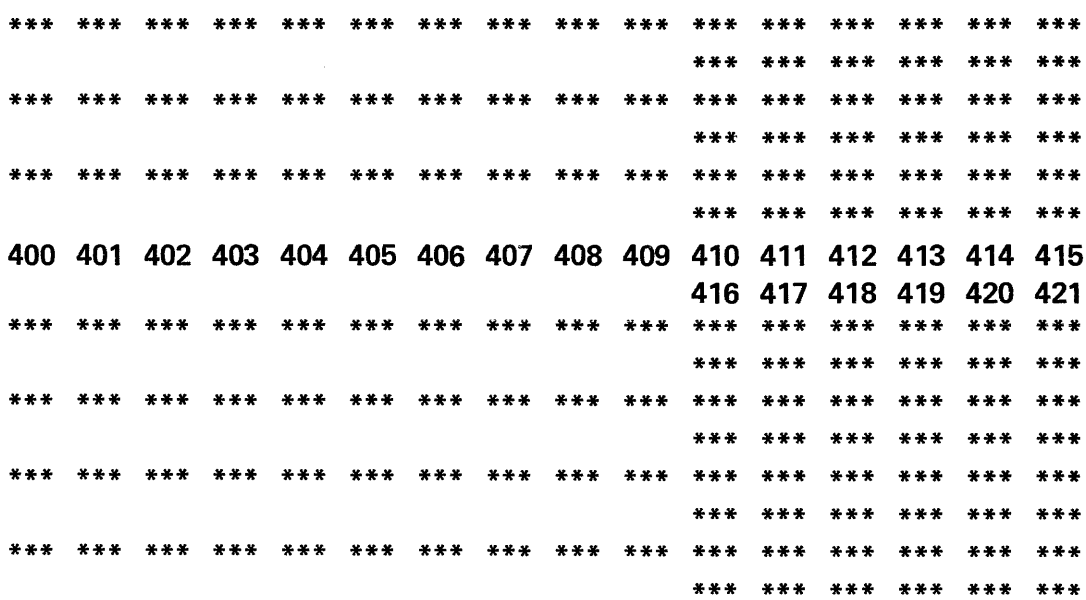


Figure 3-26. Board Error Map Representation for 256KB Add-On Memory Array Tests

rows of memory on the 256KB add-on memory array board. When entered, the run command in the form of "*RC X X" (where row is substituted for X X) results in a repetitive series of test cycles on the designated row. The test is specifically designed for troubleshooting with an oscilloscope.

3.9.1.4 256KB Add-On Memory Array Performance Tests. If the nominal march test passes, joystick J- will branch to the remaining board/chip performance and board function tests. Each test is run automatically after the joystick is toggled (J-) for the performance tests, provided the preceding test is successfully completed. If any test fails, the BEM, the type of test, and the values of Vcc, Vdd, and Vbb are displayed followed by "J + TO CONT; J- TO END". Always end the test before removing the board under test from the memory tester interface. For the performance tests, the majority of failures will be due to marginal memory chips, provided the march test passes.

3.9.1.5 256KB Add-On Memory Array Function Tests. Four board function tests are performed after the completion of the performance tests. Each of these tests is described as follows:

Refresh Operation. A data pattern is written to the board under test, and during a given time period only refresh cycles are performed. A read cycle is then performed to verify retention of data. The last two cycles of the debug routine (see paragraph 3.9.1.3) are refresh cycles for troubleshooting refresh circuit failures.

Board De-Select. To ensure that addresses that are not within the given address space for the board under test do not select the board, a series of invalid addresses are written to and read from the board, expecting that the attempt will fail. If an invalid address causes a pass condition to occur, the memory tester will stop and loop on that condition.

Error LED Test. Visual verification of the error LEDs is indicated by CRT messages. A Run Continuous command is provided for troubleshooting.

BSEL Test. The signal at edgeboard pin P3-19 is measured automatically for select and de-select levels. A Run Continuous command is provided for troubleshooting by CRT messages if the test fails.

3.9.1.6 Test Completed. If no error messages or failing board maps appear during the execution of the test, "TEST COMPLETE" will be displayed on the memory tester CRT to indicate that the board under test has successfully completed the test.

3.9.2 Troubleshooting the 256KB Add-On Memory Array

The final diagnostic test for the 256KB add-on memory array, the debug routine, provides a continuous command for each row. Each command results in a repetitive series of test cycles specifically designed for troubleshooting with an oscilloscope. Alternate 1s and 0s are applied to address and data for a write and a read cycle. Address and data are then complemented and a write cycle is performed followed by a read cycle. Two refresh cycles are performed with a refresh address and its complement. These six memory cycles are repeated continuously. A sync signal occurring at the beginning of each series of six cycles is available at the Adar memory tester control panel (CYCLE COUNT BNC). Refer to figure 3-27 for some specific waveforms and oscilloscope settings.

3.9.2.1 256KB Add-On Array RAM Input/Output Timing. Refer to figure 3-28 for expanded timing waveforms at RAM inputs and outputs.

3.9.2.2 256KB Add-On Array Error Circuit. A run continuous command is provided for troubleshooting the error LED circuits if the LEDs fail the visual test. See figure 3-29 for the expected waveforms.

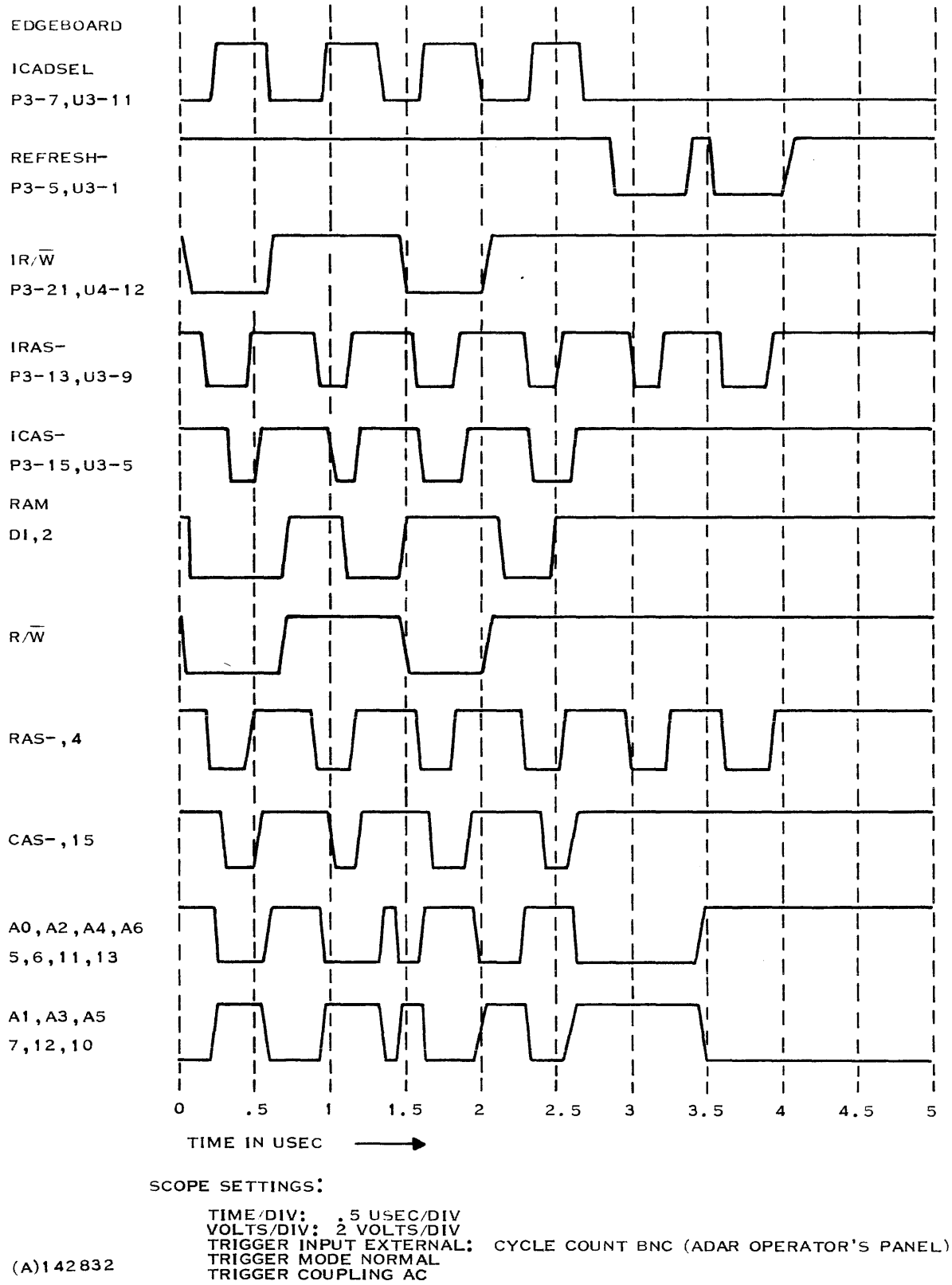


Figure 3-27. 256KB Add-On Memory Array Debug Routine Waveforms

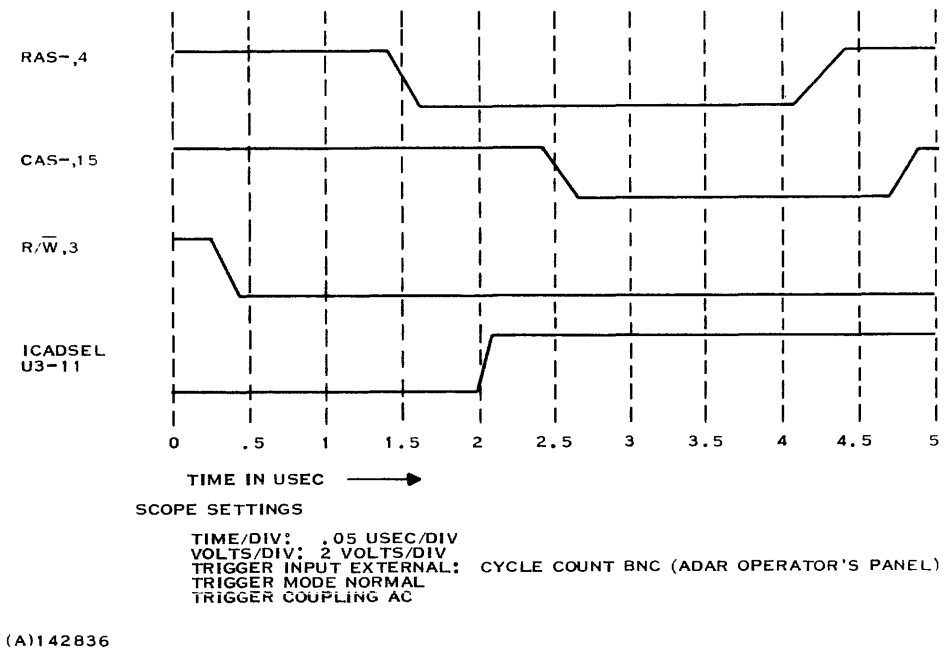


Figure 3-28. 256KB Add-On Array RAM Input/Output Timing Waveforms

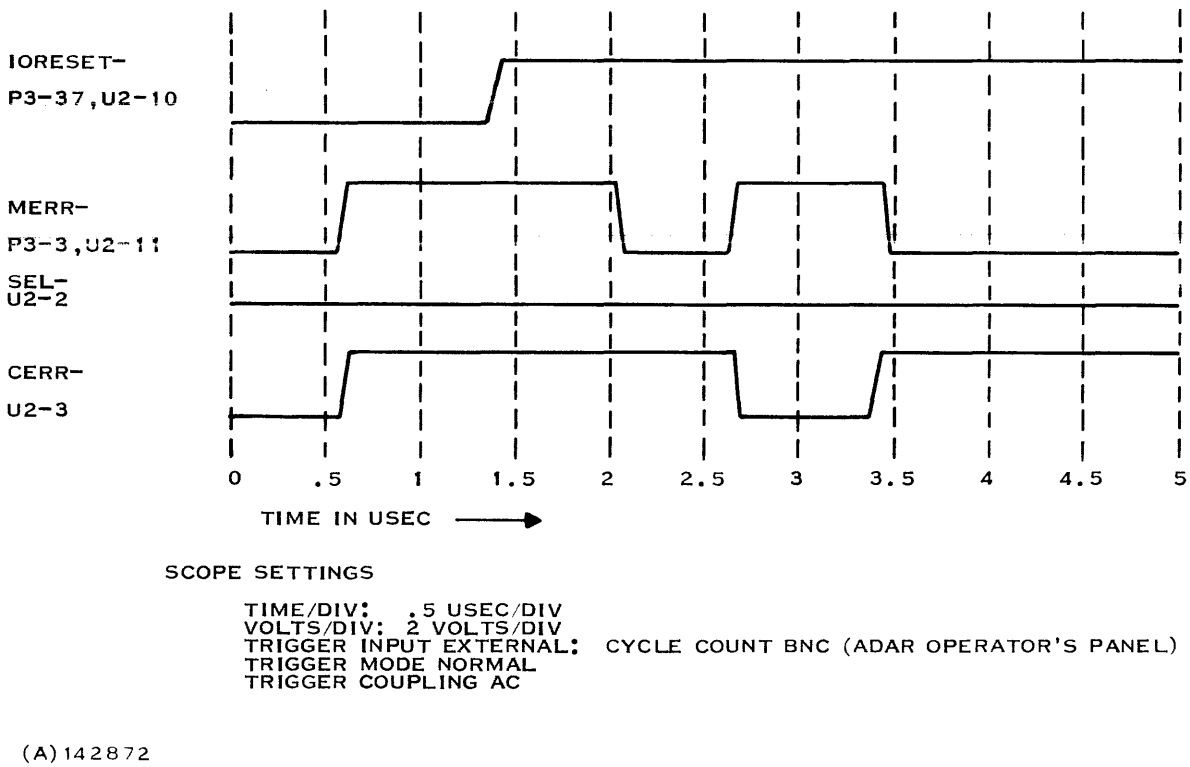


Figure 3-29. 256KB Add-On Array Error Circuits Waveforms

3.9.2.3 256KB Add-On Array Board Select Signal. A Run Continuous command is provided for troubleshooting the board select signal, IBSEL-, if the board select test fails. See figure 3-30 for the expected waveform.

3.9.2.4 Troubleshooting 256KB Add-On Array for Standby Power. A Run Continuous command is provided for troubleshooting the 256KB add-on array during standby power conditions. Waveforms are shown in figure 3-31 for the initial loss of +5 MAIN, for the duration of power loss (battery power), and for the resumption of +5 MAIN power.

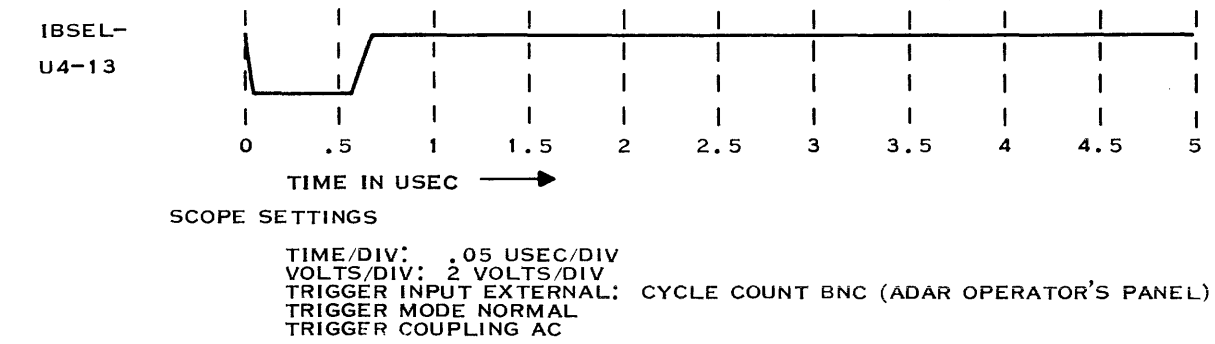


Figure 3-30. Board Select Waveform

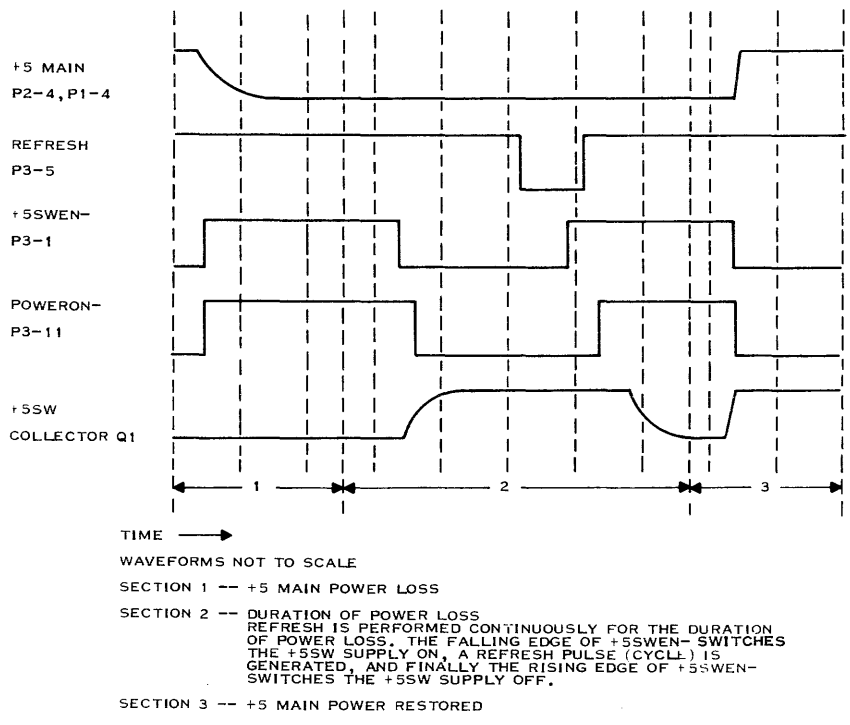


Figure 3-31. Waveforms for Power Loss and Restored Main Power

4

Drawings

This section contains the following assembly drawings and logic diagrams for TILINE memory.

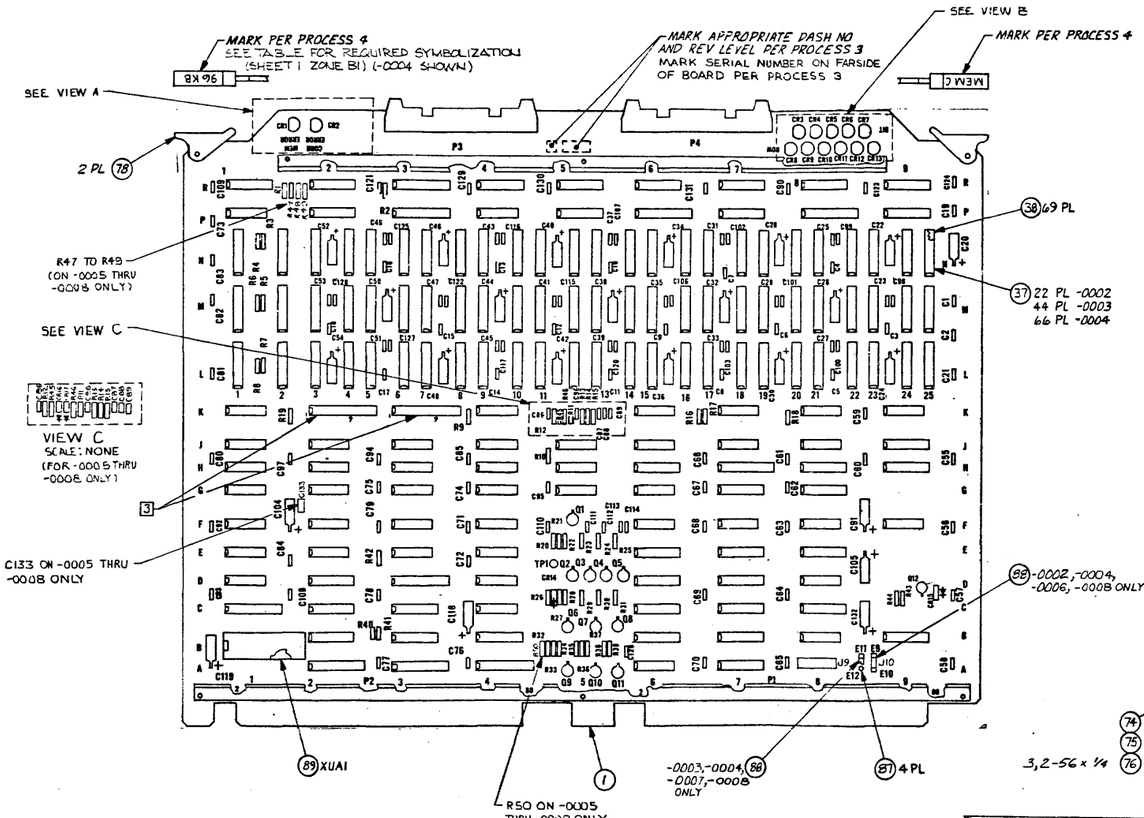
NOTES: UNLESS OTHERWISE SPECIFIED:

1. ITEM 36 IS INSTALLED AT TEST
2. R11, R12, R45 AND R46 MAY BE SELECTED OR DELETED AT TEST
3. INSTALL 16 PIN SOCKET (ITEM 35) PIN 1 AT PIN 1 OF PWB. INSTALL 8 PIN SOCKET (ITEM 79) PIN 1 AT PIN 9 OF PWB. UK2 AND UK3 ONLY

NOTES CONT ED:8 SH2

VIEW B
(FOR -0005 THRU -0008 PWB'S ONLY)

VIEW A
(FOR -0005 THRU -0008 PWB'S ONLY)



REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	CN436274 (B) & Mod (1) ADDED NOTES 5 & 6, AND JUMPER TABLE (2) ON LMS ITEM 53 WAS -0377, ITEM 54 WAS -0397, ITEM 62 WAS -0513, AND DELETED ITEM 77 (5) UPDATED REV LEVEL BLK	9-22-75	E Wong
B	CN437766 (B) & Mod (1) SH 2, NOTE 6 WAS "PWB REV A (2) UPDATED REV LEVEL BLK	11-14-78	J.K.
C	CN 437767 (B) & Mod (1) SH 2, ADDED NOTE 6D & E (2) UPDATED REV LEVEL BLOCK	11-14-78	J.K.
D	CN437771 (B) & Mod (1) SH 2: ADDED TO NOTE 6D & E (2) UPDATED REV LEVEL BLOCK	11-14-78	J.K.
E	CN437772 (E) & Mod (1) SH 1 ZN D7 NOTE WAS MARK...4" (2) SH1 ZN B1 ADDED SYMBOL COLUMN TO -1 TABLE (3) ON ALL LMS PN ITEM 68 WAS 972948-2, IT 64 WAS 972958-2, IT 68 WAS 539544-2, IT 79 WAS 539544-6, IT 89 WAS 539544-11 ALSO ADDED IT 96 TO ALL LMS (4) UPDATED REV LVL BLK	3-26-79	

(REVISIONS CONT SH 2)

5	2261980-5008	AUTO INSERTED PARTS LIST FOR 2261980-0008
5	2261980-5007	AUTO INSERTED PARTS LIST FOR 2261980-0007
5	2261980-5006	AUTO INSERTED PARTS LIST FOR 2261980-0006
5	2261980-5005	AUTO-INSERTED PARTS LIST FOR 2261980-0005

2261980-0004,8	J9 & J10	96 KB	96 KB
2261980-0003,7	J9	64 KB	64 KB
2261980-0002,6	J10	32 KB	32 KB
2261980-0001,5	—	0 KB	—
PART NUMBER	JUMPER	MEMORY SIZE	SYMBOLIZATION

2261980-0008	MEMORY CONTROLLER, 96KB W/ECC, 990/16KR, FL
2261980-0007	MEMORY CONTROLLER, 64KB W/ECC, 990/16KR, FL
2261980-0006	MEMORY CONTROLLER, 32 KB W/ECC, 990/16KR, FL
2261980-0005	MEMORY CONTROLLER W/ECC, 990/16KR FL
5 2261980-5004	AUTO-INSERTED PARTS LIST FOR 2261980-0004
2261980-5003	AUTO-INSERTED PARTS LIST FOR 2261980-0003
2261980-5002	AUTO-INSERTED PARTS LIST FOR 2261980-0002
5 2261980-5001	AUTO-INSERTED PARTS LIST FOR 2261980-0001
2261980-0004	MEMORY CONTROLLER, 96KB W/ECC, 990/16KR
2261980-0003	MEMORY CONTROLLER, 64KB W/ECC, 990/16KR
2261980-0002	MEMORY CONTROLLER, 32KB W/ECC, 990/16KR
2261980-0001	MEMORY CONTROLLER, W/ECC, 990/16KR
PART NO	DESCRIPTION

SEQ NO	IDENT	F SPEC	NO	ADDITIONAL
4	MARK	100-07	712	CLR BLK TYPE 6
3	MARK	100-02	21	HGT .12, CLR BLK
2	SLDR	124-02	00	
1	SLDR	127-01	00	

PROCESS / CLASSIFICATION — NOTES

PROCESSES — FOR CORRELATION TO GOVT/IND SPECIFICATIONS SEE TI DRAWING 725467

REV LEVEL CONT																
PWB 2262031-0001 (FL)	B	B	B	B	B	B	B	B	C	C	C	C	B	B	B	B
TEST PROC 2261983-9501	A	B	B	B	B	B	B	B	C	C	C	C	B	B	B	B
LOGIC 2261982-9901	E	E	E	E	E	F	F	F	F	F	F	F	F	F	F	F
PWB 2261981-0001	D	D	D	D	D	D	D	D	E	E	E	E	D	D	D	D
ASSY 2261980	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE			
TEST PROC 2261983-9501	*	*	*	*	*	*	*	*	A	A	A	A				
LOGIC 2261982-9901	*	/	A	B	B	B	D	D	D	D	D	D				
PWB 2261981-0001	5	5	C	C	C	C	C	C	C	C	D	D				
ASSY 2261980	*	A	B	C	D	E	F	G	H	K	L	M				

REV STATUS OF SHEETS: REV AE AE; SHEET 1 2

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION	NOTES
		PARTS LIST			

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES: ANGLES ±1°; 3 PLACE DECIMALS ± .010; 2 PLACE DECIMALS ± .02
- INTERPRET DRAWING PER MIL D 1000
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIM
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

.013 THRU .125 +.004 -.001	.126 THRU .250 +.005 -.001	.251 THRU .500 +.006 -.001
.501 THRU .750 +.008 -.001	.751 THRU 1.000 +.010 -.001	1.001 THRU 2.000 +.012 -.001

7047

NEXT ASSY / USED ON

APPLICATION

DRAWN 5-4-75; ENGR 5-12-75; APPR 6-6-75; CONTR 6-7-75; RELEASE 6/4/75

TEXAS INSTRUMENTS INCORPORATED Dallas, Texas

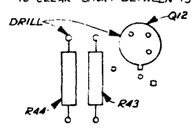
MEMORY CONTROLLER, W/ECC, 990/16KR

SIZE D; FSCM NO 96214; DRAWING NO 2261980

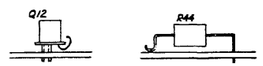
SCALE —; SHEET 1 OF 2

NOTES (CON'T)

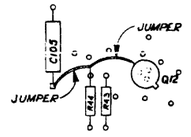
4. REWORK FOR PWB 2261981 REV'A' (APPLIES TO PWB 2261981 ONLY)
   (A) DRILL 2 HOLES AS SHOWN TO .055" (DRILL #54) TO CLEAR SHORT BETWEEN +5V AND -5V MEM (COLLECTOR OF Q12 AND TOP HOLE OF R44)



(B) FILL DRILLED HOLES WITH THERMOPLASTIC ADHESIVE
(C) MOUNT COMPONENTS Q12 AND R44 AS SHOWN. SOLDER LEADS TO PAD OF MODIFIED HOLES.



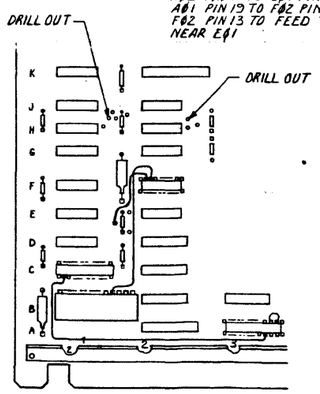
(D) SOLDER 24 AWG SOLID CONDUCTOR JUMPER WIRE ON COMPONENT SIDE AS SHOWN.



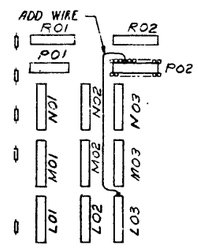
(E) SECURE Q12, R44, AND JUMPER WIRE WITH THERMOPLASTIC ADHESIVE

5. REWORK PROCEDURE FOR PWB REV A (APPLIES TO PWB 2261981 ONLY)
   A. REMOVE MARKING 'J9' AND 'J10' ON PWB
   B. MARK PER PROCESS POINTS E11 AND E12
      MARK PER PROCESS POINTS E9 AND E10
      'J10' NEAR TEST

6. REWORK PROCEDURE FOR PWB REV A THRU REV D (APPLIES TO PWB 2261981 ONLY)
   A. DRILL OUT FEED THROUGH HOLES
   B. ON COMPONENT SIDE ADD 24 AWG SOLID CONDUCTOR WIRE AS SHOWN BELOW
      ADD WIRE BETWEEN A83 PIN 12 TO A83 PIN 13
      A83 PIN 7 TO C81 PIN 2
      A81 PIN 13 TO F82 PIN 12
      F82 PIN 13 TO FEED THROUGH NEAR E81



C. ON COMPONENT SIDE 24 AWG SOLID CONDUCTOR WIRE AS SHOWN BELOW ADD WIRE FROM UP02 PIN 13 TO FEED THROUGH NEAR U L03



D. CUT PINS J7-12, H4-9, J1-1, AND J1-3
E. ON COMPONENT SIDE ADD THE FOLLOWING WIRES:

FROM	TO
J5-4	J7-12 (DEVICE)
H7-8	G6-9
K4-6	G6-10
G6-8	H4-9 (DEVICE)
H2-8	J1-3 (DEVICE)
H2-10	J1-1 (DEVICE)

7. REWORK PROCEDURE FOR PWB REV A THRU D: (APPLIES TO PWB 2261981 ONLY)
   A. REPLACE DEVICE IN LOCATIONS UE1 AND UE2 WITH ITEM 97 (745258)

8. REWORK PROCEDURE FOR PWB REV A THRU D: (APPLIES TO PWB 2261981 ONLY)
   A. CUT PIN F02-14
   B. ADD JUMPER FROM F02-14 TO G02-14

9. ITEM 98 IN -0001, -0002, -0003, -0004, -0005, -0006, -0007, AND -0008 LM 5 CONSISTS OF COMPONENTS WHICH ARE AUTO-INSERTED AND CONTAINED IN THE -5006-5002, -5003-5004, -5005, -5006, -5007, AND -5008 LM (APPLIES TO PWB 2261981 ONLY)

10. REWORK NOTE FOR PWB REV A THRU D: (APPLIES TO PWB 2261981 ONLY)
    A. CUT PIN GD4-13
    B. ADD JUMPER FROM G03-8 TO G04-13 (DEVICE)

REVISIONS					
ZONE	LTR	DESCRIPTION	DATE	APPROVED	
	LE	CN 472830 (D) Created (1) ITEM A WAS B AND VIEW B WAS A (2) UPDATED REV LEVEL BLOCK	9-23-80	E. Wing	

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	F	(C) [illegible] (1) ON -1, -2, -3, -4 LMS QTY ITEM 26 WAS 4 (2) ADDED ITEM 97 PN 2194628-7259 TO -1, -2, -3, & 4 (3) ADDED NOTE 7 (4) & (5) UPDATES REV LVL BLK	5-22-79	[illegible]
	G	CN 441710 (C) [illegible] (1) ON -1A CREATED -5001 -5002 -5003 & -5004 (2) ON -0001 -0002 -0003 & -0004 LMS ADDED ITEM 98 ITEM 53 WAS -385, ITEM 29 WAS -402 (4) DELETED REV LEVEL BLOCK (5) ADDED NOTE 9	5-22-79	[illegible]
	H	CN 448438 (B) [illegible] (1) ON SH2 ADDED NOTE 8 (2) UPDATED REV LEVEL BLOCK	3-23-79	[illegible]
	J	CN 442476 (C) [illegible] NOTE 6 S. "R4-6" WAS R4-8 (3) UPDATE REV LEVEL BLOCK.	5-25-79	E. Wing
	K	CN 436829 (C) [illegible] (1) SH 1 ZN D-5 UNDER "MARK APPROPRIATE ... PROCESS 3" ADDED "MARK SERIAL NO ... PROCESS 3" (2) ON LM -1, -2, -3, -4 ITEM 53 WAS P/N 5391370-381 & ADDED ITEMS 99 & 100 (3) ZN D-8 NOTE 2 READ "R45 & R46 VALUES ARE SELETED AT TEST (4) UPDATED REV LEVEL BLOCK	7-27-79	E. Wing
	L	CN 435041 (C) [illegible] (1) ON -1, -2, -3, -4 ON ITEM 99 P/N WAS 539370-414 & ITEM 100 WAS 537370-430 (2) UPDATED REV LEVEL BLOCK	7-27-79	E. Wing
	M	CN 435049 (C) [illegible] (1) ADDED R11 AND R12 TO NOTE 2 (2) UPDATED REV LEVEL BLOCK	7-27-79	E. Wing
	N	CN 449782 (B) [illegible] (1) ADDED NOTE 10 (C) UPDATED REV LEVEL BLOCK	10 DEC 79	[illegible]
	P	CN 472706 (C) [illegible] (1) ON SH 2 NOTE 6 FIRST LINE WAS "... PWB REV A & B" (2) NOTE 7 & 8 WAS "... REV A-C" (3) UPDATE REV LEVEL BLOCK	5-21-80	E. Wing
	R	CN 445221 (D) [illegible] (1) ADDED ITEM 101 TO -1, -2, -3 & -4 LM'S (2) UPDATED REV LEVEL BLOCK	5-21-80	E. Wing
	T	CN 472711 (B) [illegible] (1) ON SH 2 IN REV TABLE, ECN 449782 CLASS OF CHANGE WAS (C) (2) UPDATED REV LEVEL BLOCK	5-21-80	E. Wing
	U	CN 453424 (D) [illegible] (1) REVISED PER EXTENSIVE ENGINEERING CHANGES	5-21-80	E. Wing
	V	CN 473219 (D) [illegible] (1) DELETED NOTE 1 (2) UPDATED REV LEVEL BLOCK	5-21-80	E. Wing
	W	CN 461229 (D) [illegible] (1) DELETED ITEM 43 THRU 54, 56, 58, 60, 69, 85, 86, 90 FROM THE -1, -2, -3, AND -4 LM'S AND ADDED SAME ITEMS TO -5001, 2, 3, AND 4 LM'S (2) ON -0002, 3, AND 4 LM'S QTY OF ITEM 59 WAS 91, QTY OF ITEM 63 WAS 4 (3) ADDED ITEMS 59, 59A THRU 59H, 63 AND 63A (4) UPDATE REV LEV BLOCK	8-27-80	E. Wing
	Y	CN 459005 (D) [illegible] (1) REVISED PER EXTENSIVE ENGR CHANGES (2) UPDATED REV LEV BLOCK	8-27-80	E. Wing
	AA	CN 453322 (D) [illegible] (1) DELETED ITEM 38 FROM -1 THRU -8 LMS (2) MOVED ITEM 37 FROM -0002 THRU -0008 TO -5002 THRU -5008 (3) UPDATED REV LEV BLOCK	8-27-80	E. Wing
	AB	CN 454252 (D) [illegible] (1) ITEM 87 P/N WAS 097274Z-1 ON ALL LM'S (2) UPDATED REV LEV BLOCK	8-27-80	E. Wing
	AC	CN 465204 (D) [illegible] (1) ADDED ITEM 38 TO -0001 THRU -0008 LM (2) UPDATED REV LEV BLOCK	8-27-80	E. Wing
	AD	CN 474075 (C) [illegible] (1) DELETED ITEMS 35 AND 42 FROM -0002, 3, 4, 6, 7, 8 LM'S (2) ADDED ITEMS 35 AND 42 TO -5002, 3, 4, 6, 7, 8 LM'S (3) UPDATED REV LEV BLOCK	8-27-80	E. Wing

(REVISONS CONT IN ZONE D3)

TEXAS INSTRUMENTS	DRN J. Pumpian DATE 6/2/78 ISSUE DATE	SIZE / FSCM NO D 96214	DRAWING NO 226/980	REV AE
		SCALE	SHEET 2	

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM2261980-0001 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	REF	EA		2261982-9901	LOGIC,MEMORY CONTROLLER,W/ECC,990/12	
0003	REF	EA		2261983-9901	TEST PROCEDURE,MEMORY CONTROLLER,990/12	
0004	REF	EA		2261984-9901	SPECIFICATION,MEM CONT W/ECC,16KR	
0029	00002.000	EA		0996009-0002	IC,SN74LS241N,LINE DRIVERS	01295S-N74LS241N
0029A					UA2 UA4	
0027	00001.000	EA		0996029-0001	IC,SN74LS273N OCTAL D-TYPE FLIP/FLOP	TI -SN74LS273N
0027A					UD3	
0030	00001.000	EA		2261985-0001	FPLA,ADDRESS DECODE,16KR MEMORY CONT	
0030A					UA1	
0032	00003.000	EA		0996307-0001	IC,SN74S373,OCTAL D, FLIPFLOP	TI -SN74S373
0032A					UP3 UP6 UP8	
0033	00001.000	EA		0996420-0001	IC, SN74LS373N	001295-SN74LS373N
0033A					UC1	
0035	00006.000	EA		0972583-0001	NETWORK,SN75365	TI- -SN75365
0035A					UL1 UM1 UN1 UL2 UM2 UN2	
0036	00002.000	EA		0996462-0001	DELAY LINE,TAPPED	097722-FP-7111
0036A					UK2 UK3	
0038	00002.000	EA		2210188-0012	SOCKET,DIP,16-PINS,LOW PROFILE	SEE T -I DRAWING
0038A					XUK02 XUK03	
0042	00003.000	EA		0972037-1220	NETWORK,RES 22 OHM 2% 16PIN 8ELEMENT	073138-898-3-R22

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY CONTROLLER,W/ECC,990/16KR

APPD MFG. — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO 7047 — PART NUMBER LM2261980-0001 — REV ~~AE~~ AF

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM2261980-0001 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0042A					UL3 UM3 UN3	
0055	00002.000	EA		0972753-0012	CAP,FIXED 220PF 25 WVDC 2.0%	UC -C500221G
0055A					C86 C96	
0057	00001.000	EA		0972757-0016	CAP,FIXED CER 1000PF 50VRDC +10%	007119-CAC02XTR391K10
0057A					C110	
0059	00004.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0059A					C58 C111 C112 C113	
0063	00001.000	EA		0972924-0006	CAP FIX TANT SOLID 39 MFD 10 % 10 VOLT	QPL -M39003/1-2259
0063A					C119	
0064	00006.000	EA		0800523-0001	TRANSISTOR A5T2907 PNP SILICON	TI- -A5T2907
0064A					Q3 Q4 Q5 Q6 Q7 Q8	
0065	00001.000	EA		0972957-0001	TRANSISTOR,2N930A NPN LOW CUR AMP,TO-18	MOT - 2N930A
0065A					Q2	
0066	00001.000	EA		0972949-0001	TRANSISTOR 2N2605 LOW-LEVEL,LOW-NOISE	TI -2N2605
0066A					Q10	
0067	00002.000	EA		0972955-0001	XSTR 2N2369A,NPN,HIGH SPEED SW,TO-18	MOT - 2N2369A
0067A					Q1 Q11	
0068	00002.000	EA		0972057-0001	TRANSISTOR-A5T2222 NPN SILICON	TI- -A5T2222
0068A					Q9 Q12	
0070	00002.000	EA		0972537-0001	DIODE,LED 550-0103 50 MA 3 V	DIA --550-0103

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY CONTROLLER,W/ECC,990/16KR

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-0001 — REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 3 of — PART NUMBER LM2261980-0001 — REV AD AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0070A					CR1 CR2	
0071	00011.000	EA		0226609-0001	DIODE,VISIBLE LIGHT EMITTING	
0071A					CR3 THRU CR13	
0072	00002.000	EA		0972547-0008	SWITCH, SLIDE-SPST,DIP 8 SWITCHES	
0072A					UC7 U89	
0073	00002.000	EA		0972137-0005	CONNECTOR,PC 90 PIN	BEI - 65483-005
0073A					P3 P4	
0074	00001.000	EA		0945239-0001	BRACKET-STIFFENER, PWB, 14IN	
0075	00001.000	EA		0944954-0001	INSULATOR, PWB, 14IN	
0076	00006.000	EA		0972684-0002	SCREW,THD FRMG,HEX WSHR HD,2-56X1/4 LG	
0078	00002.000	EA		0533844-0001	EJECTOR, NYLON, NON-LOCKING, PWB	
0079	00002.000			2210188-0010	DIP SOCKET,8-PIN,LOW PROFILE	SEE TI- DRAWING
0080	00001.000	EA		0996089-0004	IC,SN74LS244N LINE DRIVER	-SN74LS244N
0080A					UA3	
0083	00001.000	EA		0996089-0001	IC,SN74LS240N,LINE DRIVERS	001295-SN74LS240N
0083A					UR3	
0084	00001.000	EA		0946693-0067	ROM #1,16K ECC DECODE,990/10	
0084A					UM7	
0087	00004.000	EA		0996864-0001	CONNECTOR,SOCKET PCB	022526-75060-007
0087A					E9 THRU E12	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY CONTROLLER,W/ECC,990/16KR

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-0001 — REV AD AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 4 of — PART NUMBER LM2261980-0001 — REV AD AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0089	00001.000	EA		2210188-0017	SOCKET,DIP,20-PIN,LOW PROFILE	SEE T -I DRAWING
0089A					XUA1	
0091	00001.000	EA		0411226-0002	TERMINAL,STUD	
0091A					TP1	
0092	00001.000	EA		0946707-0001	STIFFENER,PWB,11 INCH	
0093	00001.000	EA		0946708-0001	INSULATOR,STIFFENER,PWB,11 INCH	
0095	00001.000	EA		0539468-0002	DIODE,IN4002 1AMP 100PIV RECTIFIER	TI - IN4002
0095A					CR15	
0096	00001.000	EA		2210188-0014	SOCKET,DIP,20-PIN,LOW PROFILE	SEE T -I DRAWING
0096A					XUM7	
0098	00001.000	EA		2261980-5001	AUTO-INSERTED PARTS LIST FOR 2261980-1	
0099	00001.000	EA		0539370-0510	RES FIX FILM 20.0K OHM 1% .25 WATT	COR -NA55D-100PPM/C
0099A					R46	
0100	00001.000	EA		0539370-0525	RES FIX FILM 28.7K OHM 1% .25 WATT	COR - NA55
0100A					R45	
0101	00002.800	FT		2210083-0003	WIRE,ELEC,COND U/L STYLE 1213,24 AWG	090484-WTE24A

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY CONTROLLER,W/ECC,990/16KR

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-0001 — REV AD AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM2261980-0002 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	REF	EA		2261982-9901	LOGIC,MEMORY CONTROLLER,W/ECC,990/12	
0003	REF	EA		2261983-9901	TEST PROCEDURE,MEMORY CONTROLLER,990/12	
0004	REF	EA		2261984-9901	SPECIFICATION,MEM CONT W/ECC,16KR	
0025	00002.000	EA		0996089-0002	IC,SN74LS241N,LINE DRIVERS	01295S-N74LS241N
0025A					UA2 UA4	
0027	00001.000	EA		0996029-0001	IC,SN74LS273N OCTAL D-TYPE FLIP/FLOP	TI -SN74LS273N
0027A					UD3	
0030	00001.000	EA		2261985-0001	FPLA,ADDRESS DECODE,16KR MEMORY CONT	
0030A					UA1	
0032	00003.000	EA		0996307-0001	IC,SN74S373,OCTAL D, FLIPFLOP	TI -SN74S373
0032A					UP3 UP6 UP8	
0033	00001.000	EA		0996420-0001	IC, SN74LS373N	001295-SN74LS373N
0033A					UC1	
0036	00002.000	EA		0996462-0001	DELAY LINE,TAPPED	097722-EP-7111
0036A					UK2 UK3	
0038	00002.000	EA		2210188-0012	SOCKET,DIP,16-PINS,LOW PROFILE	SEE T -I DRAWING
0038A					XUK02 XUK03	
0055	00002.000	EA		0972753-0012	CAP,FIXED 220PF 25 WVDC 2.0%	UC -C500221G
0055A					C86 C96	
0057	00001.000	EA		0972757-0016	CAP,FIXED CER 1800PF 50WVDC +10%	007115-CAC02X7R391K10

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: MEMORY CONTROLLER,32KB W/ECC,16KR

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-0002 | REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM2261980-0002 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0057A					C110	
0059	00004.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0059A					C58 C111 C112 C113	
0063	00001.000	EA		0972924-0006	CAP FIX TANT SOLID 39 MFD 10 % 10 VOLT	QPL -M39003/1-2259
0063A					C119	
0064	00006.000	EA		0800523-0001	TRANSISTOR A5T2907 PNP SILICON	TI- -A5T2907
0064A					Q3 Q4 Q5 Q6 Q7 Q8	
0065	00001.000	EA		0972957-0001	TRANSISTOR,2N930A NPN LOW CUR AMP,TO-18	MOT - 2N930A
0065A					Q2	
0066	00001.000	EA		0972949-0001	TRANSISTOR 2N2605 LOW-LEVEL,LOW-NOISE	TI -2N2605
0066A					Q10	
0067	00002.000	EA		0972955-0001	XSTR 2N2369A,NPN,HIGH SPEED SW,TO-18	MOT - 2N2369A
0067A					Q1 Q11	
0068	00002.000	EA		0972057-0001	TRANSISTOR-A5T2222 NPN SILICON	TI- -A5T2222
0068A					Q9 Q12	
0070	00002.000	EA		0972937-0001	DIODE,LED 550-0103 50 MA 3 V	DIA --550-0103
0070A					CR1 CR2	
0071	00011.000	EA		0226609-0001	DIODE,VISIBLE LIGHT EMITTING	
0071A					CR3 THRU CR13	
0072	00002.000	EA		0972547-0008	SWITCH, SLIDE-SPST,DIP 8 SWITCHES	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: MEMORY CONTROLLER,32KB W/ECC,16KR

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-0002 | REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 3 of — PART NUMBER LM2261980-0002 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0072A					UC7 UB9	
0073	00002.000	EA		0972137-0005	CONNECTOR,PC 50 PIN	BEI - 65483-005
0073A					P3 P4	
0074	00001.000	EA		0945239-0001	BRACKET-STIFFENER, PWB, 14IN	
0075	00001.000	EA		0944954-0001	INSULATOR, PWB, 14IN	
0076	00006.000	EA		0972684-0002	SCREW,THD FRMG,HEX WSHR HD,2-56X1/4 LG	
0078	00002.000	EA		0533844-0001	EJECTOR, NYLON, NON-LOCKING, PWB	
0079	00002.000			2210188-0010	DIP SOCKET,8-PIN,LOW PROFILE	SEE TI- DRAWING
0080	00001.000	EA		0996089-0004	IC,SN74LS244N LINE DRIVER	-SN74LS244N
0080A					UA3	
0083	00001.000	EA		0996089-0001	IC,SN74LS240N,LINE DRIVERS	001295-SN74LS240N
0083A					UR3	
0084	00001.000	EA		0946693-0067	ROM #1,16K ECC DECODE,990/10	
0084A					UM7	
0087	00004.000	EA		0996864-0001	CONNECTOR,SOCKET PCB	022526-75060-007
0087A					E9 THRU E12	
0088	00001.000	EA		0972713-0001	PLUG, JUMPER, I.C., 0.300 INCH	
0088A					J10	
~~0089~~	~~00001.000~~	~~EA~~		~~2210188-0017~~	~~SOCKET,DIP,28-PIN,LOW PROFILE~~	~~SEE T -I DRAWING~~
0089A					XUA1	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY CONTROLLER,32KB W/ECC,16KR

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-0002 — REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 4 of — PART NUMBER LM2261980-0002 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
~~0091~~	00001.000	EA		0411226-0002	TERMINAL,STUD	
0091A					TP1	
0092	00001.000	EA		0946707-0001	STIFFENER,PWB,11 INCH	
0093	00001.000	EA		0946708-0001	INSULATOR,STIFFENER,PWB,11 INCH	
0095	00001.000	EA		0539468-0002	DIODE,1N4002 1AMP 100PIV RECTIFIER	TI - 1N4002
0095A					CR15	
0096	00001.000	EA		2210188-0014	SOCKET,DIP,20-PIN,LOW PROFILE	SEE T -I DRAWING
0096A					XUH7	
0098	00001.000	EA		2261980-5002	AUTO-INSERTED PARTS LIST FOR 2261980-2	
0099	00001.000	EA		0539370-0510	RES FIX FILM 20.0K OHM 1% .25 WATT	CDR -NA55D-100PPM/C
0099A					R46	
0100	00001.000	EA		0539370-0525	RES FIX FILM 28.7K OHM 1% .25 WATT	CDR - NA55
0100A					R45	
0101	00002.000	FT		2210083-0003	WIRE,ELEC,COND U/L STYLE 1213,24 AWG	090484-WTE24A

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY CONTROLLER,32KB W/ECC,16KR

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-0002 — REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM2261980-0003 REV AD AF

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	REF	EA		2261982-9901	LOGIC,MEMORY CONTROLLER,W/ECC,990/12	
0003	REF	EA		2261983-9901	TEST PROCEDURE,MEMORY CONTROLLER,990/12	
0004	REF	EA		2261984-9901	SPECIFICATION,MEM CONT W/ECC,16KR	
0025	00002.000	EA		0996609-0002	IC,SN74LS241N,LINE DRIVERS	01295S-N74LS241N
0025A					UA2 UA4	
0027	00001.000	EA		0996629-0001	IC,SN74LS273N OCTAL D-TYPE FLIP/FLOP	TI -SN74LS273N
0027A					U03	
0030	00001.000	EA		2261985-0001	PPLA,ADDRESS DECODE,16KR MEMORY CONT	
0030A					UA1	
0032	00003.000	EA		0996307-0001	IC,SN74S373,OCTAL D, FLIPFLOP	TI -SN74S373
0032A					UP3 UP6 UP8	
0033	00001.000	EA		0996420-0001	IC, SN74LS373N	001295-SN74LS373N
0033A					UC1	
0036	00002.000	EA		0996462-0001	DELAY LINE,TAPPED	097722-EP-7111
0036A					UK2 UK3	
0038	00002.000	EA		2219188-0012	SOCKET,DIP,16-PINS,LOW PROFILE	SEE T-I DRAWING
0038A					XUK02 XUK03	
0055	00002.000	EA		0972753-0012	CAP,FIXED 220PF 25 WVDC 2.0%	UC -C50D221G
0055A					C06 C96	
0057	00001.000	EA		0972757-0016	CAP,FIXED CER 1000PF 50WRDC +10%	007119-CAC02X7R391K10

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: MEMORY CONTROLLER,64KB W/ECC,16KR

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-0003 REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM2261980-0003 REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0057A					C110	
0059	00004.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0059A					C58 C111 C112 C113	
0063	00001.000	EA		0972924-0006	CAP FIX TANT SOLID 39 MFD 10 % 10 VOLT	QPL -M39003/1-2259
0063A					C119	
0064	00006.000	EA		0800523-0001	TRANSISTOR A5T2907 PNP SILICON	TI- -A5T2907
0064A					Q3 Q4 Q5 Q6 Q7 Q8	
0065	00001.000	EA		0972957-0001	TRANSISTOR,2N930A NPN LOW CUR AMP,TO-18	MOT - 2N930A
0065A					Q2	
0066	00001.000	EA		0972949-0001	TRANSISTOR 2N2605 LOW-LEVEL,LOW-NOISE	TI -2N2605
0066A					Q10	
0067	00002.000	EA		0972955-0001	XSTR 2N2369A,NPN,HIGH SPEED SW,TO-18	MOT - 2N2369A
0067A					Q1 Q11	
0068	00002.000	EA		0972057-0001	TRANSISTOR-A5T2222 NPN SILICON	TI- -A5T2222
0068A					Q9 Q12	
0070	00002.000	EA		0972537-0001	DIODE,LED 550-0103 50 MA 3 V	DIA --550-0103
0070A					CR1 CR2	
0071	00011.000	EA		0226609-0001	DIODE,VISIBLE LIGHT EMITTING	
0071A					CR3 THRU CR13	
0072	00002.000	EA		0972547-0008	SWITCH, SLIDE-SPST,DIP 8 SWITCHES	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: MEMORY CONTROLLER,64KB W/ECC,16KR

APPD. MFG DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-0003 REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 3 of — PART NUMBER LM2261980-0003 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0072A					UC7 UB9	
0073	00002.000	EA		0972137-0005	CONNECTOR,PC 50 PIN	BEI - 65483-005
0073A					P3 P4	
0074	00001.000	EA		0945239-0001	BRACKET-STIFFENER, PWB, 14IN	
0075	00001.000	EA		0944954-0001	INSULATOR, PWB, 14IN	
0076	00006.000	EA		0972684-0002	SCREW,THD FRMG,HEX WSHR HD,2-56X1/4 LG	
0078	00002.000	EA		0533844-0001	EJECTOR, NYLON, NON-LOCKING, PWB	
0079	00002.000			2210188-0010	DIP SOCKET,8-PIN,LOW PROFILE	SEE TI- DRAWING
0080	00001.000	EA		0996089-0004	IC,SN74LS244N LINE DRIVER	-SN74LS244N
0080A					UA3	
0083	00001.000	EA		0996089-0001	IC,SN74LS240N,LINE DRIVERS	001295-SN74LS240N
0083A					UR3	
0084	00001.000	EA		0946693-0067	ROM 81,16K ECC DECODE,990/10	
0084A					UH7	
0087	00004.000	EA		0996864-0001	CONNECTOR,SOCKET PCB	022526-75060-007
0087A					E9 THRU E12	
0088	00001.000	EA		0972713-0001	PLUG, JUMPER, I.C., 0.300 INCH	
0088A					J9	
~~0089~~	~~00001.000~~	~~EA~~		~~2210188-0017~~	~~SOCKET,DIP,28-PIN,LOW PROFILE~~	~~SEE T -I DRAWING~~
0089A					XUA1	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY CONTROLLER,64KB W/ECC,16KR

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-0003 — REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 4 of — PART NUMBER LM2261980-0003 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0091	00001.000	EA		0411226-0002	TERMINAL,STUD	
0091A					TP1	
0092	00001.000	EA		0946707-0001	STIFFENER,PWB,11 INCH	
0093	00001.000	EA		0946708-0001	INSULATOR,STIFFENER,PWB,11 INCH	
0095	00001.000	EA		0539468-0002	DIODE,1N4002 1AMP 100PIV RECTIFIER	TI - 1N4002
0095A					CR15	
0096	00001.000	EA		2210188-0014	SOCKET,DIP,20-PIN,LOW PROFILE	SEE T -I DRAWING
0096A					XUH7	
0098	00001.000	EA		2261980-5003	AUTO-INSERTED PARTS LIST FOR 2261980-3	
0099	00001.000	EA		0539370-0510	RES FIX FILM 20.0K OHM 1% .25 WATT	COR -NA55D-L00PPM/C
0099A					R46	
0100	00001.000	EA		0539370-0525	RES FIX FILM 28.7K OHM 1% .25 WATT	COR - NA55
0100A					R45	
0101	00002.800	FT		2210083-0003	WIRE,ELEC,COND U/L STYLE 1213,24 AWG	090484-WTF24A

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY CONTROLLER,64KB W/ECC,16KR

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-0003 — REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM2261980-0004 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	REF	EA		2261982-9901	LOGIC,MEMORY CONTROLLER,W/ECC,990/12	
0003	REF	EA		2261983-9901	TEST PROCEDURE,MEMORY CONTROLLER,990/12	
0004	REF	EA		2261984-9901	SPECIFICATION,MEM CONT W/ECC,16KR	
0025	00002.000	EA		0996089-0002	IC,SN74LS241N,LINE DRIVERS	01295S-N74LS241N
0025A					UA2 UA4	
0027	00001.000	EA		0996029-0001	IC,SN74LS273N OCTAL D-TYPE FLIP/FLOP	TI -SN74LS273N
0027A					U03	
0030	00001.000	EA		2261985-0001	FPLA,ADDRESS DECODE,16KR MEMORY CONT	
0030A					UA1	
0032	00003.000	EA		0996307-0001	IC,SN74S373,OCTAL D, FLIPFLOP	TI -SN74S373
0032A					UP3 UP6 UP8	
0033	00001.000	EA		0996420-0001	IC, SN74LS373N	001295-SN74LS373N
0033A					UC1	
0036	00002.000	EA		0996462-0001	DELAY LINE,TAPPED	097722-EP-7111
0036A					UK2 UK3	
0038	00002.000	EA		2210188-0012	SOCKET,DIP,16-PINS,LOW PROFILE	SEE T-I DRAWING
0038A					XUK02 XUK03	
0055	00002.000	EA		0972753-0012	CAP,FIXED 220PF 25 WVDC 2.0%	UC -C500221G
0055A					C86 C96	
0057	00001.000	EA		0972757-0016	CAP,FIXED CER 1800PF 50WRDC +10%	007115-CAC02X7R391K10

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY CONTROLLER,96KB W/ECC,16KR

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-0004 — REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM2261980-0004 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0097A					C110	
0099	00004.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0099A					C90 C111 C112 C113	
0063	00001.000	EA		0972924-0006	CAP FIX TANT SOLID 39 MFD 10 % 10 VOLT	QPL -M39003/1-2259
0063A					C119	
0064	00008.000	EA		0800523-0001	TRANSISTOR A5T2907 PNP SILICON	TI- -A5T2907
0064A					Q3 Q4 Q5 Q6 Q7 Q8	
0065	00001.000	EA		0972957-0001	TRANSISTOR,2N930A NPN LOW CUR AMP,TO-18	MOT - 2N930A
0065A					Q2	
0066	00001.000	EA		0972949-0001	TRANSISTOR 2N2605 LOW-LEVEL,LOW-NOISE	TI -2N2605
0066A					Q10	
0067	00002.000	EA		0972955-0001	XSTR 2N2369A,NPN,HIGH SPEED SW,TO-18	MOT - 2N2369A
0067A					Q1 Q11	
0068	00002.000	EA		0972057-0001	TRANSISTOR-A5T2222 NPN SILICON	TI- -A5T2222
0068A					Q9 Q12	
0070	00002.000	EA		0972937-0001	DIODE,LED 550-0103 50 MA 3 V	DIA --550-0103
0070A					CR1 CR2	
0071	00011.000	EA		0226609-0001	DIODE,VISIBLE LIGHT EMITTING	
0071A					CR3 THRU CR13	
0072	00002.000	EA		0972547-0006	SWITCH, SLIDE-SPST,DIP 8 SWITCHES	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY CONTROLLER,96KB W/ECC,16KR

APPD MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-0004 — REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 3 of — PART NUMBER LM2261980-0004 — REV XD AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0072A					UC7 UB9	
0073	00002.000	EA		0972137-0005	CONNECTOR,PC 50 PIN	BFI - 65483-005
0073A					P3 P4	
0074	00001.000	EA		0945239-0001	BRACKET-STIFFENER, PWB, 14IN	
0075	00001.000	EA		0944954-0001	INSULATOR, PWB, 14IN	
0076	00006.000	EA		0972684-0002	SCREW,THD FRMG,HEX WSHR HD,2-56X1/4 LG	
0078	00002.000	EA		0933844-0001	EJECTOR, NYLON, NON-LOCKING, PWB	
0079	00082.000			2210188-0010	DIP SOCKET,8-PIN,LOW PROFILE	SEE TI- DRAWING
0080	00001.000	EA		0996089-0004	IC,SN74LS244N LINE DRIVER	-SN74LS244N
0080A					UA3	
0083	00001.000	EA		0996089-0001	IC,SN74LS240N,LINE DRIVERS	001295-SN74LS240N
0083A					UR3	
0084	00001.000	EA		0946693-0067	ROM #1,16K ECC DECODE,990/10	
0084A					UH7	
0087	00004.000	EA		0996864-0001	CONNECTOR,SOCKET PCB	022526-75060-007
0087A					E9 THRU E12	
0088	00002.000	EA		0972713-0001	PLUG, JUMPER, I.C., 0.300 INCH	
0088A					J9 J10	
0089	00001.000	EA		2210188-0017	SOCKET,DIP,28-PIN,LOW PROFILE	SEE T -I DRAWING
0089A					XUA1	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY CONTROLLER,96KB W/ECC,16KR

APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-0004 — REV XD AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 4 of — PART NUMBER LM2261980-0004 — REV XD AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0091	00001.000	EA		0411226-0002	TERMINAL,STUD	
0091A					TP1	
0092	00001.000	EA		0946707-0001	STIFFENER,PWB,11 INCH	
0093	00001.000	EA		0946708-0001	INSULATOR,STIFFENER,PWB,11 INCH	
0095	00001.000	EA		0539468-0002	DIODE,1N4002 1AMP 100PIV RECTIFIER	TI - IN4002
0095A					CR15	
0096	00001.000	EA		2210188-0014	SOCKET,DIP,20-PIN,LOW PROFILE	SEE T -I DRAWING
0096A					XUH7	
0098	00001.000	EA		2261980-5004	AUTO-INSERTED PARTS LIST FOR 2261980-4	
0099	00001.000	EA		0539370-0510	RES FIX FILM 20.0K OHM 1% .25 WATT	COR -NA55D-10GPP4/C
0099A					R46	
0100	00001.000	EA		0539370-0525	RES FIX FILM 28.7K OHM 1% .25 WATT	COR - NA55
0100A					R45	
0101	00002.800	FT		2210083-0003	WIRE,ELEC,COND U/L STYLE 1213,24 AWG	090484-WTE24A

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY CONTROLLER,96KB W/ECC,16KR

APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-0004 — REV XD AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM2261980-0005 REV AD

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	REF	EA		2261982-9901	LOGIC,MEMORY CONTROLLER,W/ECC,990/12	
0003	REF	EA		2261983-9901	TEST PROCEDURE,MEMORY CONTROLLER,990/12	
0004	REF	EA		2261984-9901	SPECIFICATION,MEM CONT W/ECC,16KR	
0025	00002.000	EA		0996089-0002	IC,SN74LS241N,LINE DRIVERS	01295S-N74LS241N
0025A					UA2 UA4	
0027	00001.000	EA		0996029-0001	IC,SN74LS273N OCTAL D-TYPE FLIP/FLOP	TI -SN74LS273N
0027A					UD3	
0030	00001.000	EA		2261985-0001	FPLA,ADDRESS DECODE,16KR MEMORY CONT	
0030A					UA1	
0032	00003.000	EA		0996307-0001	IC,SN74S373,OCTAL D, FLIPFLOP	TI -SN74S373
0032A					UP3 UP6 UP8	
0033	00001.000	EA		0996420-0001	IC, SN74LS373N	001295-SN74LS373N
0033A					UC1	
0035	00006.000	EA		0972583-0001	NETWORK,SN75365	TI- -SN75365
0035A					UL1 UM1 UN1 UL2 UM2 UN2	
0036	00002.000	EA		0996462-0001	DELAY LINE,TAPPED	097722-EP-7111
0036A					UK2 UK3	
0038	00002.000	EA		2210188-0012	SOCKET,DIP,16-PINS,LOW PROFILE	SEE T -I DRAWING
0038A					XUK02 XUK03	
0042	00003.000	EA		0972037-1220	NETWORK,RES 22 OHM 2% 16PIN 8ELEMENT	073138-898-3-R22

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY CONTROLLER,W/ECC,990/16KR,FL

APPD MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-0005 REV AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM2261980-0005 REV AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0042A					UL3 UM3 UN3	
0046	00001.000	EA		0972946-0049	RES FIX 220 OHM 5 % .25 W CARBON FILM	ROH - R-25
0046A					R49	
0057	00001.000	EA		0972757-0016	CAP,FIXED CER 1000PF 50WRDC +10%	007119-CAC02X7R391K10
0057A					C110	
0059	00004.000	EA		0972763-0021	CAP,,FIXED,AXIAL LEAD,,.047 UF,+80%,-20%	
0059A					C90 C111 C112 C113	
0063	00001.000	EA		0972924-0006	CAP FIX TANT SOLID 39 MFD 10 % 10 VOLT	CPL -M39003/1-2259
0063A					C119	
0064	00006.000	EA		0800523-0001	TRANSISTOR A5T2907 PNP SILICON	TI- -A5T2907
0064A					Q3 Q4 Q5 Q6 Q7 Q8	
0065	00001.000	EA		0972957-0001	TRANSISTOR,2N930A NPN LOW CUR AMP,TO-18	MOT - 2N930A
0065A					Q2	
0066	00001.000	EA		0972949-0001	TRANSISTOR 2N2605 LOW-LEVEL,LOW-NOISE	TI -2N2605
0066A					Q10	
0067	00003.000	EA		0972955-0001	XSTR 2N2369A,NPN,HIGH SPEED SW,TO-18	MOT - 2N2369A
0067A					Q1 Q11 Q9	
0068	00001.000	EA		0972957-0001	TRANSISTOR-A5T2222 NPN SILICON	TI- -A5T2222
0068A					Q12	
0070	00002.000	EA		0972537-0001	DIODE,LED 550-0103 50 MA 3 V	DIA --550-0103

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY CONTROLLER,W/ECC,990/16KR,FL

APPD MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-0005 REV AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 3 of — PART NUMBER LM2261980-0005 — REV ~~AB~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0070A					CR8 CR11	
0071	00011.000	EA		0226609-0001	DIODE,VISIBLE LIGHT EMITTING	
0071A					CR1 THRU CR7,CR9,CR10	
0071B					CR12 CR13	
0072	00002.000	EA		0972547-0008	SWITCH, SLIDE-SPST,DIP 8 SWITCHES	
0072A					UC7 UB9	
0073	00002.000	EA		2210154-0015	HEADER,POLARIZED AND LATCHING, 50 PINS	000779-86476-7
0073A					P3 P4	
0074	00001.000	EA		0945239-0001	BRACKET-STIFFENER, PWB, 14IN	
0075	00001.000	EA		0944954-0001	INSULATOR, PWB, 14IN	
0076	00006.000	EA		0972684-0002	SCREW,THD FRMG,HEX WSHR HD,2-56X1/4 LG	
0078	00002.000	EA		0533844-0001	EJECTOR, NYLON, NON-LOCKING, PWB	
0079	00002.000			2210188-0010	DIP SOCKET,8-PIN,LOW PROFILE	SEE TI- DRAWING
0080	00001.000	EA		0996089-0004	IC,SN74LS244N LINE DRIVER	-SN74LS244N
0080A					UA3	
0083	00001.000	EA		0996089-0001	IC,SN74LS240N,LINE DRIVERS	001295-SN74LS240N
0083A					UR3	
0084	00001.000	EA		0946693-0067	ROM #1,16K ECC DECODE,990/10	
~~0084A~~					~~UH7~~	
0087	00004.000	EA		0996864-0001	CONNECTOR,SOCKET PCB	022526-75060-007

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY CONTROLLER,W/ECC,990/16KR,FL

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-0005 — REV ~~AB~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 4 of — PART NUMBER LM2261980-0005 — REV ~~AB~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0087A					E9 THRU E12	
0089	00001.000	EA		2210188-0017	SOCKET,DIP,28-PIN,LOW PROFILE	SEE T -I DRAWING
0089A					XUA1	
0091	00001.000	EA		0411226-0002	TERMINAL,STUD	
0091A					TP1	
0092	00001.000	EA		0946707-0001	STIFFENER,PWB,11 INCH	
0093	00001.000	EA		0946708-0001	INSULATOR,STIFFENER,PWB,11 INCH	
0095	00001.000	EA		0539468-0002	DIODE,1N4002 1AMP 100PIV RECTIFIER	TI - IN4002
0095A					CR15	
0096	00001.000	EA		2210188-0014	SOCKET,DIP,20-PIN,LOW PROFILE	SEE T -I DRAWING
0096A					XUM7	
0098	00001.000	EA		2261980-0005	AUTO-INSERTED PARTS LIST FOR 2261980-5	
0099	00001.000	EA		0539370-0510	RES FIX FILM 20.0K OHM 1% .25 WATT	COR -NA55D-100PPM/C
0099A					R46	
0100	00001.000	EA		0539370-0525	RES FIX FILM 28.7K OHM 1% .25 WATT	COR - NA55
0100A					R45	
0101	00002.000	FT		2210083-0003	WIRE,ELEC,COND U/L STYLE 1213,24 AWG	090484-WTE24A
0107	00001.000	EA		0972929-0373	CAP FIX CERAMIC 47.0 PF 10 % 200 V	QPL - M39014/1C-137
0107A					C133	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY CONTROLLER,W/ECC,990/16KR,FL

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-0005 — REV ~~AB~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM2261980-0006 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	REF	EA		2261982-9901	LOGIC,MEMORY CONTROLLER,W/ECC,990/12	
0003	REF	EA		2261983-9901	TEST PROCEDURE,MEMORY CONTROLLER,990/12	
0004	REF	EA		2261984-9901	SPECIFICATION,MEM CONT W/ECC,16KR	
0025	00002.000	EA		0996089-0002	IC,SN74LS241N,LINE DRIVERS	01295S-N74LS241N
0025A					UA2 UA4	
0027	00001.000	EA		0996029-0001	IC,SN74LS273N OCTAL D-TYPE FLIP/FLOP	TI -SN74LS273N
0027A					UD3	
0030	00001.000	EA		2261985-0001	FPLA,ADDRESS DECODE,16KR MEMORY CONT	
0030A					UA1	
0032	00003.000	EA		0996307-0001	IC,SN74S373,OCTAL D, FLIPFLOP	TI -SN74S373
0032A					UP3 UP6 UP8	
0033	00001.000	EA		0996420-0001	IC, SN74LS373N	001295-SN74LS373N
0033A					UC1	
0036	00002.000	EA		0996462-0001	DELAY LINE,TAPPED	097722-EP-7111
0036A					UK2 UK3	
0038	00002.000	EA		2210188-0012	SOCKET,DIP,16-PINS,LOW PROFILE	SEE T -I DRAWING
0038A					XUK02 XUK03	
0044	00001.000	EA		0972946-0049	RES FIX 220 OHM 5 % .25 W CARBON FILM	ROH - R-25
0044A					R49	
0057	00001.000	EA		0972757-0016	CAP,FIXED CER 1800PF 50WRDC +10%	007115-CAC02X7R391K10

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: MEMORY CONTROLLER,32KB,W/ECC,990/16KR,FL

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-0006 | REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM2261980-0006 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0057A					C110	
0059	00004.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0059A					C58 C111 C112 C113	
0063	00001.000	EA		0972924-0006	CAP FIX TANT SOLID 39 MFD 10 % 10 VOLT	QPL -M39003/1-2259
0063A					C119	
0064	00006.000	EA		0800523-0001	TRANSISTOR A5T2907 PNP SILICON	TI- -A5T2907
0064A					Q3 Q4 Q5 Q6 Q7 Q8	
0065	00001.000	EA		0972957-0001	TRANSISTOR,2N930A NPN LOW CUR AMP,TO-18	MOT - 2N930A
0065A					Q2	
0066	00001.000	EA		0972949-0001	TRANSISTOR 2N2605 LOW-LEVEL,LOW-NOISE	TI -2N2605
0066A					Q10	
0067	00003.000	EA		0972955-0001	XSTR 2N2369A,NPN,HIGH SPEED SW,TO-18	MOT - 2N2369A
0067A					Q1 Q11 Q9	
0068	00001.000	EA		0972057-0001	TRANSISTOR-A5T2222 NPN SILICON	TI- -A5T2222
0068A					Q12	
0070	00002.000	EA		0972537-0001	DIODE,LED 550-0103 50 MA 3 V	DIA --550-0103
0070A					CR8 CR11	
0071	00011.000	EA		0226609-0001	DIODE,VISIBLE LIGHT EMITTING	
0071A					CR1 THRU CR7,CR9,CR10	
0071B					CR12 CR13	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: MEMORY CONTROLLER,32KB,W/ECC,990/16KR,FL

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-0006 | REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 3 of — PART NUMBER LM2261980-0006 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0072	00002.000	EA		0972547-0008	SWITCH, SLIDE-SPST,DIP 8 SWITCHES	
0072A					UC7 U89	
0073	00002.000	EA		2210154-0015	HEADER,POLARIZED AND LATCHING, 50 PINS	000779-86476-7
0073A					P3 P4	
0074	00001.000	EA		0945239-0001	BRACKET-STIFFENER, PWB, 14IN	
0075	00001.000	EA		0944954-0001	INSULATOR, PWB, 14IN	
0076	00006.000	EA		0972684-0002	SCREW,THD FRMG,HEX WSHR HD,2-56X1/4 LG	
0078	00002.000	EA		0533844-0001	EJECTOR, NYLON, NON-LOCKING, PWB	
0079	00002.000			2210188-0010	DIP SOCKET,8-PIN,LOW PROFILE	SEE TI- DRAWING
0080	00001.000	EA		0996089-0004	IC,SN74LS244N LINE DRIVER	-SN74LS244N
0080A					UA3	
0083	00001.000	EA		0996089-0001	IC,SN74LS240N,LINE DRIVERS	001295-SN74LS240N
0083A					UR3	
0084	00001.000	EA		0946693-0067	ROM #1,16K ECC DECODE,990/10	
0084A					UM7	
0087	00004.000	EA		0996864-0001	CONNECTOR,SOCKET PCB	022526-75060-007
0087A					E9 THRU E12	
0088	00001.000	EA		0972713-0001	PLUG, JUMPER, I.C., 0.300 INCH	
0088A					J10	
0089	00001.000	EA		2210188-0017	SOCKET,DIP,28-PIN,LOW PROFILE	SEE T -I DRAWING

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY CONTROLLER,32KB,W/ECC,990/16KR,FL

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-0006 — REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 4 of — PART NUMBER LM2261980-0006 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0090A					XUA1	
0091	00001.000	EA		0411226-0002	TERMINAL,STUD	
0091A					TP1	
0092	00001.000	EA		0946707-0001	STIFFENER,PWB,11 INCH	
0093	00001.000	EA		0946708-0001	INSULATOR,STIFFENER,PWB,11 INCH	
0095	00001.000	EA		0539466-0002	DIODE,1N4002 1AMP 100PIV RECTIFIER	TI - 1N4002
0095A					CR15	
0096	00001.000	EA		2210188-0014	SOCKET,DIP,20-PIN,LOW PROFILE	SEE T -I DRAWING
0096A					XUM7	
0098	00001.000	EA		2261980-5006	AUTO-INSERTED PARTS LIST FOR 2261980-6	
0099	00001.000	EA		0539370-0510	RES FIX FILM 20.0K OHM 1% .25 WATT	COR -NA55D-100PPM/C
0099A					R46	
0100	00001.000	EA		0539370-0525	RES FIX FILM 28.7K OHM 1% .25 WATT	COR - NA55
0100A					R45	
0101	00002.000	FT		2210083-0003	WIRE,ELEC,COND U/L STYLE 1213,24 AWG	090484-WTF24A
0107	00001.000	EA		0972929-0373	CAP FIX CERAMIC 47.0 PF 10 % 200 V	QPL - M39014/1C-137
0107A					C133	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY CONTROLLER,32KB,W/ECC,990/16KR,FL

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-0006 — REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM2261980-0007 REV AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	REF	EA		2261982-9901	LOGIC,MEMORY CONTROLLER,W/ECC,990/12	
0003	REF	EA		2261983-9901	TEST PROCEDURE,MEMORY CONTROLLER,990/12	
0004	REF	EA		2261984-9901	SPECIFICATION,MEM CONT W/ECC,16KR	
0025	00002.000	EA		0996889-0002	IC,SN74LS241N,LINE DRIVERS	01295S-N74LS241N
0025A					UA2 UA4	
0027	00001.000	EA		0996829-0001	IC,SN74LS273N OCTAL D-TYPE FLIP/FLOP	TI -SN74LS273N
0027A					U03	
0030	00001.000	EA		2261985-0001	FPLA,ADDRESS DECODE,16KR MEMORY CONT	
0030A					UA1	
0032	00003.000	EA		0996307-0001	IC,SN74S373,OCTAL D, FLIPFLOP	TI -SN74S373
0032A					UP3 UP6 UP8	
0033	00001.000	EA		0996420-0001	IC, SN74LS373N	001295-SN74LS373N
0033A					UC1	
0036	00002.000	EA		0996462-0001	DELAY LINE,TAPPED	097722-EP-7111
0036A					UK2 UK3	
0038	00002.000	EA		2210188-0012	SOCKET,DIP,16-PINS,LOW PROFILE	SEE T-I DRAWING
0038A					XUK02 XUK03	
0044	00001.000	EA		0972946-0049	RES FIX 220 OHM 5 % .25 W CARBON FILM	ROH - R-25
0044A					R49	
0057	00001.000	EA		0972757-0016	CAP,FIXED CER 1800PF 50WRDC +10%	007115-CAC02X7R391K10

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: MEMORY CONTROLLER,64KB,W/ECC,990/16KR,FL

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-0007 REV AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM2261980-0007 REV AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0057A					C110	
0059	00004.000	EA		0972763-0021	CAP,,FIXED,AXIAL LEAD,,.047 UF,+80%,-20%	
0059A					C58 C111 C112 C113	
0063	00001.000	EA		0972924-0006	CAP FIX TANT SOLID 39 MFD 10 % 10 VOLT	QPL -M39003/1-2259
0063A					C119	
0064	00006.000	EA		0800523-0001	TRANSISTOR A5T2907 PNP SILICON	TI- -A5T2907
0064A					Q3 Q4 Q5 Q6 Q7 Q8	
0065	00001.000	EA		0972957-0001	TRANSISTOR,2N930A NPN LOW CUR AMP,TO-18	MOT - 2N930A
0065A					Q2	
0066	00001.000	EA		0972949-0001	TRANSISTOR 2N2605 LOW-LEVEL,LOW-NOISE	TI -2N2605
0066A					Q10	
0067	00003.000	EA		0972955-0001	XSTR 2N2369A,NPN,HIGH SPEED SW,TO-18	MOT - 2N2369A
0067A					Q1 Q11 Q9	
0068	00001.000	EA		0972057-0001	TRANSISTOR-A5T2222 NPN SILICON	TI- -A5T2222
0068A					Q12	
0070	00002.000	EA		0972537-0001	DIODE,LED 550-0103 50 MA 3 V	DIA --550-0103
0070A					CR8 CR11	
0071	00011.000	EA		0226609-0001	DIODE,VISIBLE LIGHT EMITTING	
0071A					CR1 THRU CR7,CR9,CR10	
0071B					CR12 CR13	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: MEMORY CONTROLLER,64KB,W/ECC,990/16KR,FL

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-0007 REV AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 3 of — PART NUMBER LM2261980-0007 — REV AD AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0072	00002.000	EA		0972547-0008	SWITCH, SLIDE-SPST,DIP 8 SWITCHES	
0072A					UC7 U89	
0073	00002.000	EA		2210154-0015	HEADER,POLARIZED AND LATCHING, 50 PINS	000779-86476-7
0073A					P3 P4	
0074	00001.000	EA		0945239-0001	BRACKET-STIFFENER, PWB, 14IN	
0075	00001.000	EA		0944954-0001	INSULATOR, PWB, 14IN	
0076	00004.000	EA		0972684-0002	SCREW,THD FRMG,HEX WSHR HD,2-56X1/4 LG	
0078	00002.000	EA		0533044-0001	EJECTOR, NYLON, NON-LOCKING, PWB	
0079	00002.000			2210188-0010	DIP SOCKET,8-PIN,LOW PROFILE	SEE TI- DRAWING
0080	00001.000	EA		0996089-0004	IC,SN74LS244N LINE DRIVER	-SN74LS244N
0080A					UA3	
0083	00001.000	EA		0996089-0001	IC,SN74LS240N,LINE DRIVERS	001295-SN74LS240N
0083A					UR3	
0084	00001.000	EA		0946693-0067	ROM #1,16K ECC DECODE,990/10	
0084A					UM7	
0087	00004.000	EA		0996064-0001	CONNECTOR,SOCKET PCB	022526-75068-007
0087A					E9 THRU E12	
0088	00001.000	EA		0972713-0001	PLUG, JUMPER, I.C., 0.300 INCH	
0088A					J9	
0089	00001.000	EA		2210188-0017	SOCKET,DIP,28-PIN,LOW PROFILE	SEE T -I DRAWING

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY CONTROLLER,64KB,W/ECC,990/16KR,FL

APPD-MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-0007 — REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 4 of — PART NUMBER LM2261980-0007 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0089A					XUA1	
0091	00001.000	EA		0411226-0002	TERMINAL,STUD	
0091A					TP1	
0092	00001.000	EA		0946707-0001	STIFFENER,PWB,11 INCH	
0093	00001.000	EA		0946708-0001	INSULATOR,STIFFENER,PWB,11 INCH	
0095	00001.000	EA		0539468-0002	DIODE,1N4002 1AMP 100PIV RECTIFIER	TI - IN4002
0095A					CR15	
0096	00001.000	EA		2210188-0014	SOCKET,DIP,28-PIN,LOW PROFILE	SEE T -I DRAWING
0096A					XUM7	
0098	00001.000	EA		2261980-5007	AUTO-INSERTED PARTS LIST FOR 2261980-7	
0099	00001.000	EA		0539378-0510	RES FIX FILM 20.0K OHM 1% .25 WATT	COR -NA55D-100PPM/C
0099A					R46	
0100	00001.000	EA		0539370-0525	RES FIX FILM 28.7K OHM 1% .25 WATT	COR - NA55
0100A					R45	
0101	00002.800	FT		2210083-0003	WIRE,ELEC,COND U/L STYLE 1213,24 AWG	090484-WTE24A
0107	00001.000	EA		0972929-0373	CAP FIX CERAMIC 47.0 PF 10 % 200 V	QPL - M39014/1C-137
0107A					C133	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY CONTROLLER,64KB,W/ECC,990/16KR,FL

APPD-MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-0007 — REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM2261980-0008 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	REF	EA		2261982-9901	LOGIC,MEMORY CONTROLLER,W/ECC,990/12	
0003	REF	EA		2261983-9901	TEST PROCEDURE,MEMORY CONTROLLER,990/12	
0004	REF	EA		2261984-9901	SPECIFICATION,MEM CONT W/ECC,16KR	
0025	00002.000	EA		0996089-0002	IC,SN74LS241N,LINE DRIVERS	01295S-N74LS241N
0025A					UA2 UA4	
0027	00001.000	EA		0996029-0001	IC,SN74LS273N OCTAL D-TYPE FLIP/FLOP	TI -SN74LS273N
0027A					UD3	
0030	00001.000	EA		2261985-0001	FPLA,ADDRESS DECODE,16KR MEMORY CONT	
0030A					UA1	
0032	00003.000	EA		0996307-0001	IC,SN74S373,OCTAL D, FLIPFLOP	TI -SN74S373
0032A					UP3 UP6 UP8	
0033	00001.000	EA		0996420-0001	IC, SN74LS373N	001295-SN74LS373N
0033A					UC1	
0036	00002.000	EA		0996462-0001	DELAY LINE,TAPPED	097722-EP-7111
0036A					UK2 UK3	
0038	00002.000	EA		2210188-0012	SOCKET,DIP,16-PINS,LOW PROFILE	SEE T -I DRAWING
0038A					XUK02 XUK03	
0044	00001.000	EA		0972946-0049	RES FIX 220 OHM 5 % .25 W CARBON FILM	ROH - R-25
0044A					R49	
0057	00001.000	EA		0972757-0016	CAP,FIXED CER 1800PF 50WRDC +10%	007115-CAC02X7R391K10

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: MEMORY CONTROLLER,96KB,W/ECC,990/16KR,FL

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-0008 | REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM2261980-0008 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0057A					C110	
0059	00004.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0059A					C58 C111 C112 C113	
0063	00001.000	EA		0972924-0006	CAP FIX TANT SOLID 39 MFD 10 % 10 VOLT	QPL -M39003/1-2259
0063A					C119	
0064	00006.000	EA		0800523-0001	TRANSISTOR A5T2907 PNP SILICON	TI- -A5T2907
0064A					Q3 Q4 Q5 Q6 Q7 Q8	
0065	00001.000	EA		0972957-0001	TRANSISTOR,2N930A NPN LOW CUR AMP,TO-18	MOT - 2N930A
0065A					Q2	
0066	00001.000	EA		0972949-0001	TRANSISTOR 2N2605 LOW-LEVEL,LOW-NOISE	TI -2N2605
0066A					Q10	
0067	00003.000	EA		0972955-0001	XSTR 2N2369A,NPN,HIGH SPEED SW,TO-18	MOT - 2N2369A
0067A					Q1 Q11 Q9	
0068	00001.000	EA		0972057-0001	TRANSISTOR-A5T2222 NPN SILICON	TI- -A5T2222
0068A					Q12	
0070	00002.000	EA		0972537-0001	DIODE,LED 550-0103 50 MA 3 V	DIA --550-0103
0070A					CR8 CR11	
0071	00011.000	EA		0226609-0001	DIODE,VISIBLE LIGHT EMITTING	
0071A					CR1 THRU CR7,CR9,CR10	
0071B					CR12 CR13	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: MEMORY CONTROLLER,96KB,W/ECC,990/16KR,FL

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-0008 | REV ~~AB~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 3 of — PART NUMBER LM2261980-0008 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0072	00002.000	EA		0972547-0008	SWITCH, SLIDE-SPST,DIP 8 SWITCHES	
0072A					UCT UB9	
0073	00002.000	EA		2210154-0015	HEADER,POLARIZED AND LATCHING, 50 PINS	000779-86476-7
0073A					P3 P4	
0074	00001.000	EA		0945239-0001	BRACKET-STIFFENER, PWB, 14IN	
0075	00001.000	EA		0944954-0001	INSULATOR, PWB, 14IN	
0076	00006.000	EA		0972684-0002	SCREW,THD FRMG,HEX WSHR HD,2-56X1/4 LG	
0078	00002.000	EA		0533844-0001	EJECTOR, NYLON, NON-LOCKING, PWB	
0079	00002.000			2210188-0010	DIP SOCKET,8-PIN,LOW PROFILE	SEE TI- DRAWING
0080	00001.000	EA		0996089-0004	IC,SN74LS244N LINE DRIVER	-SN74LS244N
0080A					UA3	
0083	00001.000	EA		0996089-0001	IC,SN74LS240N,LINE DRIVERS	001295-SN74LS240N
0083A					UR3	
0084	00001.000	EA		0946693-0067	ROM #1,16K ECC DECODE,990/10	
0084A					UH7	
0087	00004.000	EA		0996864-0001	CONNECTOR,SOCKET PCB	022526-75060-007
0087A					E9 THRU E12	
0088	00002.000	EA		0972713-0001	PLUG, JUMPER, I.C., 0.300 INCH	
~~0088A~~					~~J9 J10~~	
0089	00001.000	EA		2210188-0017	SOCKET,DIP,28-PIN,LOW PROFILE	SEE T -I DRAWING

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY CONTROLLER,96KB,W/ECC,990/16KR,FL

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-0008 — REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 4 of — PART NUMBER LM2261980-0008 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0089A					XUA1	
0091	00001.000	EA		0411226-0002	TERMINAL,STUD	
0091A					TP1	
0092	00001.000	EA		0946707-0001	STIFFENER,PWB,11 INCH	
0093	00001.000	EA		0946708-0001	INSULATOR,STIFFENER,PWB,11 INCH	
0095	00001.000	EA		0539468-0002	DIODE,1N4002 1AMP 100PIV RECTIFIER	TI - 1N4002
0095A					CR15	
0096	00001.000	EA		2210188-0014	SOCKET,DIP,20-PIN,LOW PROFILE	SEE T -I DRAWING
0096A					XUH7	
0098	00001.000	EA		2261980-5008	AUTO-INSERTED PARTS LIST FOR 2261980-8	
0099	00001.000	EA		0539370-0510	RES FIX FILM 20.0K OHM 1% .25 WATT	COR -NA55D-100PPM/C
0099A					R46	
0100	00001.000	EA		0539370-0525	RES FIX FILM 28.7K OHM 1% .25 WATT	COR - NA55
0100A					R45	
0101	00002.800	FT		2210083-0003	WIRE,ELEC,COND U/L STYLE 1213,24 AWG	090484-WTE24A
0107	00001.000	EA		0972929-0373	CAP FIX CERAMIC 47.0 PF 10 % 200 V	QPL - M39014/1C-137
0107A					C133	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY CONTROLLER,96KB,W/ECC,990/16KR,FL

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-0008 — REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM2261980-5001 — REV AD AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2261981-0001	PWB,MEMORY CONTROLLER,W/ECC,990/12	
0005	00001.000	EA		0219402-7400	NETWORK SN74S00N	
0005A					UK1	
0006	00002.000	EA		0972900-7400	NETWORK SN74LS00N	TI -SN74LS00N
0006A					UG2 UP4	
0007	00001.000	EA		0972900-7402	NETWORK,SN74LS02N	
0007A					UE4	
0008	00001.000	EA		0219402-7403	NETWORK SN74S03N	
0008A					UH5	
0009	00001.000	EA		0219402-7404	NETWORK SN74S04N	
0009A					UH3	
0010	00002.000	EA		0972900-7404	NETWORK SN74LS04N	
0010A					UJ3 UF2	
0011	00001.000	EA		0972749-0001	NETWORK, SN74LS08N	
0011A					UC4	
0012	00001.000	EA		0972900-7410	NETWORK SN74LS10N	
0012A					UD4	
0013	00001.000	EA		0219402-7430	NETWORK SN74S30N	
0013A					UJ7	
0014	00002.000	EA		0996136-0001	IC,SN74LS257N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS257N

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-1

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5001 | REV AD AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM2261980-5001 — REV AD AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0014A					UP9 UE6	
0015	00002.000	EA		0972900-7432	NETWORK SN74LS32N	TI -SN74LS32N
0015A					UG6 UH4	
0016	00001.000	EA		0972900-7451	NETWORK SN74LS51N	TI -SN74LS51N
0016A					UG3	
0017	00002.000	EA		0972900-7454	NETWORK SN74LS54N	TI -SN74LS54N
0017A					UH1 UD1	
0018	00005.000	EA		0219402-7474	NETWORK SN74S74N	
0018A					UJ1 UJ2 UK4 UH2 UJ4	
0019	00005.000	EA		0972900-7474	NETWORK SN74LS74N	
0019A					UG4 UF1 UF4 UG5 UE3	
0020	00004.000	EA		0219402-7486	NETWORK SN74S86N	
0020A					UF9 UF7 UF8 UF6	
0021	00001.000	EA		0972782-0001	NETWORK SN74LS132N	TI -SN74LS132N
0021A					UJ5	
0022	00002.000	EA		0219402-7138	NETWORK SN74S138N	
0022A					UG8 UG7	
0023	00002.000	EA		0996305-0001	IC,SN74S169 UP/DOWN COUNTER,4 BIT	001295-SN74S169
0023A					UD6 UC3	
0024	00001.000	EA		0972900-7175	NETWORK SN74LS175N	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-1

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5001 | REV AD AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 3 of — PART NUMBER LM2261980-5001 — REV AD

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0024A					UE8	
0026	00002.000	EA		0996136-0002	IC,SN74LS258N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS258N
0026A					UH8 UJ9	
0028	00006.000	EA		0219402-7280	NETWORK SN74S280N	TI -SN74S280N
0028A					UK6 UK7 UK8 UK9 UJ6 UJ8	
0029	00002.000	EA		0972652-0001	NETWORK SN74LS283N	
0029A					UB6 UC6	
0031	00018.000	EA		0972787-0004	NETWORK SN74LS368N	
0031A					UR1 UR2 UP2 UR6 UR7 UH6 UP7	
0031B					UR8 UR9 UC2 UB4 UA7 UR4 UR5	
0031C					UE7 UP5 UB3 UB2	
0034	00001.000	EA		0974674-0001	NETWORK SN75138N	
0034A					UB7	
0039	00002.000	EA		0996138-0001	IC,SN74LS266N 2-INPUT EXCLUSIVE-NOR GATE	TI -SN74LS266N
0039A					UD8 UB8	
0040	00001.000	EA		0972037-2680	NETWORK,RES 680 OHM 2% 16PIN BELENENT	073138-898-3-R680
0040A					UD7	
0041	00001.000	EA		0800118-0004	RESISTOR 220 OHMS DIL PULL UP 16 PINS	BEC -8981R220
0041A					UH9	
0043	00001.000	EA		0972946-0041	RES FIX 100 OHM 5 % .25 W CARBON FILM	ROH - R-25

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-1

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5001 | REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 4 of — PART NUMBER LM2261980-5001 — REV ~~AD~~ E

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0043A					R9	
0044	00005.000	EA		0972946-0049	RES FIX 220 OHM 5 % .25 W CARBON FILM	ROH - R-25
0044A					R1 R2 R29 R30 R31	
0045	00001.000	EA		0972946-0053	RES FIX 330 OHM 5 % .25 W CARBON FILM	ROH - R-25
0045A					R22	
0046	00001.000	EA		0972946-0061	RES FIX 680 OHM 5 % .25 W CARBON FILM	ROH - R-25
0046A					R21	
0047	00008.000	EA		0972946-0065	RES FIX 1.0K OHM 5% .25 W CARBON FILM	ROH - R-25
0047A					R10 R19 R20 R23 R24 R25 R37	
0047B					R38	
0048	00004.000	EA		0972946-0089	RES FIX 10K OHM 5% .25 W CARBON FILM	ROH - R-25
0048A					R32 R33 R34 R35	
0049	00001.000	EA		0972946-0095	RES FIX 18K OHM 5% .25 W CARBON FILM	ROH - R-25
0049A					R36	
0050	00001.000	EA		0972946-0105	RES FIX 47 K OHM 5 % .25 W CARBON FILM	ROH - R-25
0050A					R26	
0051	00001.000	EA		0972946-0121	RES FIX 220K OHM 5 % .25 W CARBON FILM	ROH - R-25
0051A					R39	
0052	00002.000	EA		0972946-0093	RES FIX 15K OHM 5% .25 W CARBON FILM	ROH - R-25
0052A					R27 R28	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-1

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5001 | REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 5 of — PART NUMBER LM2261980-5001 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0053	00001.000	EA		0539370-0385	RES FIX FILM 1.00K OHM 1% .25 WATT	COR - NA55
0053A					R11	
0054	00001.000	EA		0539370-0404	RES FIX FILM 1.58K OHM 1% .25 WATT	COR - NA55
0054A					R12	
0056	00001.000	EA		0972757-0025	CAP FIX CER .01MF 10% 50V	
0056A					~~C95~~	
0058	00012.000	EA		0972763-0009	CAP,FIXED .0047MF 50 VOLTS	004222-MC105F472Z
0058A					C74 C75 C80 C81 C82 C83 C85	
0058B					C94 C97 C108 C109 C121	
0059	00087.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0059A					C1 THRU C19 C21 C23 C25 C27	
0059B					C29 C31 C33 C35 C37 C39 C41	
0059C					C43 C45 C47 C49 C51 C53 C55	
0059D					C56 C57 C59 THRU C73 C76	
0059E					THRU C79 C84 C87 THRU C90	
0059F					C92 C93 C98 THRU C103 C106	
0059G					C107 C114 THRU C117 C120	
0059H					C122 THRU C125 C127 C128	
0059I					C129 C130 C131	
0060	00020.000	EA		0972924-0014	CAP FIX TANT SOLID 15 MFD 10 % 20 VOLT	QPL -M39003/1-2289

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-1

APPD -MFG — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-5001 — REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 6 of — PART NUMBER LM2261980-5001 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0060A					C20 C22 C24 C26 C28 C30 C32	
0060B					C34 C36 C38 C40 C42 C44 C46	
0060C					C48 C50 C52 C54 C91 C104	
0061	00001.000	EA		0222222-7470	NETWORK SN7470N	-SN7470N
0061A					UF3	
0062	00001.000	EA		0800118-0008	RESISTOR 1.0KOHMS DIL PULL UP 16 PINS	BEC -8981R1.0K
0062A					UC8	
0063	00003.000	EA		0972924-0006	CAP FIX TANT SOLID 39 MFD 10 % 10 VOLT	QPL -M39003/1-2259
0063A					C105 C118 C132	
0069	00001.000	EA		0972932-0081	DIODE 1N9148	SEE TI- DRAWING
0069A					CR14	
0081	00001.000	EA		0996508-0001	IC,74LS393N DUAL BINARY COUNTER	001295-74LS393N
0081A					UP1	
0082	00001.000	EA		0222222-7408	NETWORK-SN7408N	
0082A					UG1	
0085	00011.000	EA		0972946-0081	RES FIX 4.7K OHM 5 % .25 W CARBON FILM	ROH - R-25
0085A					R13 THRU R18 R40 R41 R42	
0085B					R43 R44	
0086	00006.000	EA		0972946-0025	RES FIX 22.0 OHM 5 % .25 W.CARBON FILM	ROH - R-25
0086A					R3 R4 R5 R6 R7 R8	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-1

APPD -MFG — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-5001 — REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED

DATE 08/01/80 — LIST OF MATERIAL — PAGE 7 of

PART NUMBER LM2261980-5001 REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0090	00001.000	EA		0972757-0021	CAP, FIX, CERAMIC, 4700PF, 50V 10%	
0090A					C126	
0094	00001.000	EA		0996780-0001	IC,SN74LS33N QUAD POSITIVE-NOR BUFFER	001295-SN74LS33N
0094A					UA6	
0097	00002.000	EA		0219402-7258	NETWORK SN74S258N	
0097A					UF1 UE2	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-1

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5001 REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM2261980-5002 REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2261981-0001	PWB,MEMORY CONTROLLER,W/ECC,990/12	
0005	00001.000	EA		0219402-7400	NETWORK SN74S00N	
0005A					UK1	
0006	00002.000	EA		0972900-7400	NETWORK SN74LS00N	TI -SN74LS00N
0006A					UG2 UP4	
0007	00001.000	EA		0972900-7402	NETWORK,SN74LS02N	
0007A					UE4	
0008	00001.000	EA		0219402-7403	NETWORK SN74S03N	
0008A					UH5	
0009	00001.000	EA		0219402-7404	NETWORK SN74S04N	
0009A					UH3	
0010	00002.000	EA		0972900-7404	NETWORK SN74LS04N	
0010A					UJ3 UF2	
0011	00001.000	EA		0972749-0001	NETWORK, SN74LS08N	
0011A					UC4	
0012	00001.000	EA		0972900-7410	NETWORK SN74LS10N	
0012A					UD4	
0013	00001.000	EA		0219402-7430	NETWORK SN74S30N	
0013A					UJ7	
0014	00002.000	EA		0996136-0001	IC,SN74LS257N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS257N

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-2

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5002 REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM2261980-5002 REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0014A					UP9 UE6	
0015	00002.000	EA		0972900-7432	NETWORK SN74LS32N	TI -SN74LS32N
0015A					UG6 UH4	
0016	00001.000	EA		0972900-7451	NETWORK SN74LS51N	TI -SN74LS51N
0016A					UG3	
0017	00002.000	EA		0972900-7454	NETWORK SN74LS54N	TI -SN74LS54N
0017A					UH1 UD1	
0018	00005.000	EA		0219402-7474	NETWORK SN74S74N	
0018A					UJ1 UJ2 UK4 UH2 UJ4	
0019	00005.000	EA		0972900-7474	NETWORK SN74LS74N	
0019A					UG4 UF1 UF4 UG5 UE3	
0020	00004.000	EA		0219402-7486	NETWORK SN74S86N	
0020A					UF9 UF7 UF8 UF6	
0021	00001.000	EA		0972782-0001	NETWORK SN74LS132N	TI -SN74LS132N
0021A					UJ5	
0022	00002.000	EA		0219402-7138	NETWORK SN74S138N	
0022A					UG8 UG7	
0023	00002.000	EA		0996305-0001	IC,SN74S169 UP/DOWN COUNTER,4 BIT	001295-SN74S169
0023A					UD6 UC3	
0024	00001.000	EA		0972900-7175	NETWORK SN74LS175N	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-2

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5002 REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 3 of — PART NUMBER LM2261980-5002 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0024A					UE8	
0026	00002.000	EA		0996136-0002	IC,SN74LS258N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS258N
0026A					UH8 UJ9	
0028	00006.000	EA		0219402-7280	NETWORK SN74S280N	TI -SN74S280N
0028A					UK6 UK7 UK8 UK9 UJ6 UJ8	
0029	00002.000	EA		0972692-0001	NETWORK SN74LS283N	
0029A					UB4 UC6	
0031	00018.000	EA		0972787-0004	NETWORK SN74LS368N	
0031A					UR1 UR2 UP2 UR6 UR7 UH6 UP7	
0031B					UR8 UR9 UC2 UB4 UA7 UR4 UR5	
0031C					UE7 UP5 UB3 UB2	
0034	00001.000	EA		0974674-0001	NETWORK SN75138N	
0034A					UB7	
0035	00004.000	EA		0972503-0001	NETWORK,SN75365	TI- -SN75365
0035A					UL1 UL2 UM1 UM2 UN1 UN2	
0037	00022.000	EA		0996680-0001	IC, 16K RAM, (SEL)	001295-TMS4116/ZA0727
0037A					UN4 THRU UN25	
0039	00002.000	EA		0996138-0001	IC,SN74LS266N 2-INPUT EXCLUSIVE-NOR GATE	TI -SN74LS266N
0039A					UD8 UB8	
0040	00001.000	EA		0972037-2680	NETWORK,RES 680 OHM 2% 16PIN 8ELEMENT	073138-898-3-R680

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-2

APPD.-MFG DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5002 | REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 4 of — PART NUMBER LM2261980-5002 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0040A					UD7	
0041	00001.000	EA		0800118-0004	RESISTOR 220 OHMS DIL PULL UP 16 PINS	BEC -8981R220
0041A					UH9	
0042	00003.000	EA		0972037-1220	NETWORK,RES 22 OHM 2% 16PIN 8ELEMENT	073138-898-3-R22
0042A					UL3 UM3 UN3	
0043	00001.000	EA		0972946-0041	RES FIX 100 OHM 5 % .25 W CARBON FILM	ROH - R-25
0043A					R9	
0044	00005.000	EA		0972946-0049	RES FIX 220 OHM 5 % .25 W CARBON FILM	ROH - R-25
0044A					R1 R2 R29 R30 R31	
0045	00001.000	EA		0972946-0053	RES FIX 330 OHM 5 % .25 W CARBON FILM	ROH - R-25
0045A					R22	
0046	00001.000	EA		0972946-0061	RES FIX 680 OHM 5 % .25 W CARBON FILM	ROH - R-25
0046A					R21	
0047	00008.000	EA		0972946-0065	RES FIX 1.0K OHM 5% .25 W CARBON FILM	ROH - R-25
0047A					R10 R19 R20 R23 R24 R25 R37	
0047B					R38	
0048	00004.000	EA		0972946-0089	RES FIX 10K OHM 5% .25 W CARBON FILM	ROH - R-25
0048A					R32 R33 R34 R35	
0049	00001.000	EA		0972946-0095	RES FIX 18K OHM 5% .25 W CARBON FILM	ROH - R-25
0049A					R36	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-2

APPD.-MFG DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5002 | REV ~~AD~~

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — **LIST OF MATERIAL** — PAGE 5 of — PART NUMBER LM2261980-5002 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0050	00001.000	EA		0972946-0105	RES FIX 47 K OHM 5 % .25 W CARBON FILM	ROH - R-25
0050A					R26	
0051	00001.000	EA		0972946-0121	RES FIX 220K OHM 5 % .25 W CARBON FILM	ROH - R-25
0051A					R39	
0052	00002.000	EA		0972946-0093	RES FIX 15K OHM 5% .25 W CARBON FILM	ROH - R-25
0052A					R27 R28	
0053	00001.000	EA		0539370-0385	RES FIX FILM 1.00K OHM 1% .25 WATT	COR - NA55
0053A					R11	
0054	00001.000	EA		0539370-0404	RES FIX FILM 1.58K OHM 1% .25 WATT	COR - NA55
0054A					R12	
0056	00001.000	EA		0972757-0025	CAP FIX CER .01MF 10% 50V	
0056A					C95	
0058	00012.000	EA		0972763-0009	CAP,FIXED .0047MF 50 VOLTS	004222-MC105E472Z
0058A					C74 C75 C80 C81 C82 C83 C85	
0058B					C94 C97 C108 C109 C121	
0059	00087.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0059A					C1 THRU C19 C21 C23 C25 C27	
0059B					C29 C31 C33 C35 C37 C39 C41	
0059C					C43 C45 C47 C49 C51 C53 C55	
0059D					C56 C57 C59 THRU C73 C76	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-2

APPD.-MFG DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5002 | REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — **LIST OF MATERIAL** — PAGE 6 of — PART NUMBER LM2261980-5002 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0059E					THRU C79 C84 C87 THRU C90	
0059F					C92 C93 C98 THRU C103 C106	
0059G					C107 C114 THRU C117 C120	
0059H					C122 THRU C125 C127 C128	
0059I					C129 C130 C131	
0060	00028.000	EA		0972924-0014	CAP FIX TANT SOLID 15 MFD 10 % 20 VOLT	QPL -M39003/1-2289
0060A					C20 C22 C24 C26 C28 C30 C32	
0060B					C34 C36 C38 C40 C42 C44 C46	
0060C					C48 C50 C52 C54 C91 C104	
0061	00001.000	EA		0222222-7470	NETWORK SN7470N	-SN7470N
0061A					UF3	
0062	00001.000	EA		0800118-0008	RESISTOR 1.0KOHMS DIL PULL UP 16 PINS	BEC -8981R1.0K
0062A					UC8	
0063	00003.000	EA		0972924-0006	CAP FIX TANT SOLID 39 MFD 10 % 10 VOLT	QPL -M39003/1-2259
0063A					C105 C118 C132	
0069	00001.000	EA		0972932-0001	DIODE 1N9148	SEE TI- DRAWING
0069A					CR14	
0081	00001.000	EA		0996508-0001	IC,74LS393N DUAL BINARY COUNTER	001295-74LS393N
0081A					UP1	
0082	00001.000	EA		0222222-7408	NETWORK-SN7408N	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-2

APPD.-MFG DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5002 | REV ~~AD~~ AE

TEXAS INSTRUMENTS
INCORPORATED

DATE 08/01/80 **LIST OF MATERIAL** PAGE 7 of

PART NUMBER LM2261980-5002 REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0082A					UG1	
0085	00011.000	EA		0972946-0081	RES FIX 4.7K OHM 5 % .25 W CARBON FILM	ROH - R-25
0085A					R13 THRU R18 R40 R41 R42	
0085B					R43 R44	
0086	00006.000	EA		0972946-0025	RES FIX 22.0 OHM 5 % .25 W.CARBON FILM	ROH - R-25
0086A					R3 R4 R5 R6 R7 R8	
0090	00001.000	EA		0972757-0021	CAP, FIX, CERAMIC, 4700PF, 50V 10%	
0090A					C126	
0094	00001.000	EA		0996780-0001	IC,SN74LS33N QUAD POSITIVE-NOR BUFFER	001295-SN74LS33N
0094A					UA6	
0097	00002.000	EA		0219402-7258	NETWORK SN74S258N	
0097A					UE1 UE2	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE AUTO-INSERTED PARTS LIST FOR 2261980-2

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5002 REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM2261980-5003 REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2261981-0001	PWB,MEMORY CONTROLLER,W/ECC,990/12	
0005	00001.000	EA		0219402-7400	NETWORK SN74S00N	
0005A					UK1	
0006	00002.000	EA		0972900-7400	NETWORK SN74LS00N	TI -SN74LS00N
0006A					UG2 UP4	
~~0007~~	~~00001.000~~	EA		~~0972900-7402~~	~~NETWORK,SN74LS02N~~	
0007A					UE4	
0008	00001.000	EA		0219402-7403	NETWORK SN74S03N	
0008A					UH5	
0009	00001.000	EA		0219402-7404	NETWORK SN74S04N	
0009A					UH3	
0010	00002.000	EA		0972900-7404	NETWORK SN74LS04N	
0010A					UJ3 UF2	
0011	00001.000	EA		0972749-0001	NETWORK, SN74LS08N	
0011A					UC4	
0012	00001.000	EA		0972900-7410	NETWORK SN74LS10N	
0012A					UD4	
0013	00001.000	EA		0219402-7430	NETWORK SN74S30N	
0013A					UJ7	
0014	00002.000	EA		0996136-0001	IC,SN74LS257N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS257N

DRAFTSMAN DATE — CKD. DRAFTSMAN DATE — DESIGN ENGINEER DATE — TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-3

APPD MFG DATE — APPD PROJECT ENGINEER DATE — RELEASED DATE — PROJECT NO — PART NUMBER LM2261980-5003 REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM2261980-5003 REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0014A					UP9 UE6	
0015	00002.000	EA		0972900-7432	NETWORK SN74LS32N	TI -SN74LS32N
0015A					UG6 UH4	
0016	00001.000	EA		0972900-7451	NETWORK SN74LS51N	TI -SN74LS51N
0016A					UG3	
0017	00002.000	EA		0972900-7454	NETWORK SN74LS54N	TI -SN74LS54N
0017A					UH1 UD1	
0018	00005.000	EA		0219402-7474	NETWORK SN74S74N	
0018A					UJ1 UJ2 UK4 UH2 UJ4	
0019	00005.000	EA		0972900-7474	NETWORK SN74LS74N	
0019A					UG4 UF1 UF4 UG5 UE3	
0020	00004.000	EA		0219402-7486	NETWORK SN74S86N	
0020A					UF9 UF7 UF8 UF6	
0021	00001.000	EA		0972782-0001	NETWORK SN74LS132N	TI -SN74LS132N
0021A					UJ5	
0022	00002.000	EA		0219402-7138	NETWORK SN74S138N	
0022A					UG8 UG7	
0023	00002.000	EA		0996305-0001	IC,SN74S169 UP/DOWN COUNTER,4 BIT	001295-SN74S169
0023A					UD6 UC3	
0024	00001.000	EA		0972900-7175	NETWORK SN74LS175N	

DRAFTSMAN DATE — CKD DRAFTSMAN DATE — DESIGN ENGINEER DATE — TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-3

APPD MFG DATE — APPD PROJECT ENGINEER DATE — RELEASED DATE — PROJECT NO — PART NUMBER LM2261980-5003 REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 3 of — PART NUMBER LM2261980-5003 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0024A					UE8	
0026	00002.000	EA		0996136-0002	IC,SN74LS258N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS258N
0026A					UH8 UJ9	
0028	00006.000	EA		0219402-7280	NETWORK SN74S280N	TI -SN74S280N
0028A					UK6 UK7 UK8 UK9 UJ6 UJ8	
0029	00002.000	EA		0972652-0001	NETWORK SN74LS283N	
0029A					UB6 UC6	
0031	00018.000	EA		0972787-0004	NETWORK SN74LS368N	
0031A					UR1 UR2 UP2 UR6 UR7 UH6 UP7	
0031B					UR8 UR9 UC2 UB4 UA7 UR4 UR5	
0031C					UE7 UP5 UB3 UB2	
0034	00001.000	EA		0974674-0001	NETWORK SN75138N	
0034A					UB7	
0035	00006.000	EA		0972583-0001	NETWORK,SN75365	TI- -SN75365
0035A					UL1 UL2 UM1 UM2 UN1 UN2	
0037	00044.000	EA		0996680-0001	IC, 16K RAM, (SEL)	001295-TMS4116/ZA072
0037A					UN4 THRU UN25 UM4 THRU UM25	
0039	00002.000	EA		0996138-0001	IC,SN74LS266N 2-INPUT EXCLUSIVE-NOR GATE	TI -SN74LS266N
0039A					UD8 UB8	
0040	00001.000	EA		0972037-2680	NETWORK,RES 680 OHM 2% 16PIN 8ELEMENT	073138-898-3-R680

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-3

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5003 | REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 4 of — PART NUMBER LM2261980-5003 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0040A					UD7	
0041	00001.000	EA		0800118-0004	RESISTOR 220 OHMS DIL PULL UP 16 PINS	BEC -8981R220
0041A					UH9	
0042	00003.000	EA		0972037-1220	NETWORK,RES 22 OHM 2% 16PIN 8ELEMENT	073138-898-3-R22
0042A					UL3 UM3 UN3	
0043	00001.000	EA		0972946-0041	RES FIX 100 OHM 5 % .25 W CARBON FILM	ROH - R-25
0043A					R9	
0044	00005.000	EA		0972946-0049	RES FIX 220 OHM 5 % .25 W CARBON FILM	ROH - R-25
0044A					R1 R2 R29 R30 R31	
0045	00001.000	EA		0972946-0053	RES FIX 330 OHM 5 % .25 W CARBON FILM	ROH - R-25
0045A					R22	
0046	00001.000	EA		0972946-0061	RES FIX 680 OHM 5 % .25 W CARBON FILM	ROH - R-25
0046A					R21	
0047	00008.000	EA		0972946-0065	RES FIX 1.0K OHM 5% .25 W CARBON FILM	ROH - R-25
0047A					R10 R19 R20 R23 R24 R25 R37	
0047B					R38	
0048	00004.000	EA		0972946-0089	RES FIX 10K OHM 5% .25 W CARBON FILM	ROH - R-25
0048A					R32 R33 R34 R35	
0049	00001.000	EA		0972946-0095	RES FIX 18K OHM 5% .25 W CARBON FILM	ROH - R-25
0049A					R36	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-3

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5003 | REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 5 of — PART NUMBER LM2261980-5003 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0050	00001.000	EA		0972946-0105	RES FIX 47 R OHM 5 % .25 W CARBON FILM	ROH - R-25
0050A					R26	
0051	00001.000	EA		0972946-0121	RES FIX 220K OHM 5 % .25 W CARBON FILM	ROH - R-25
0051A					R39	
0052	00002.000	EA		0972946-0093	RES FIX 15K OHM 5% .25 W CARBON FILM	ROH - R-25
0052A					R27 R28	
0053	00001.000	EA		0539370-0385	RES FIX FILM 1.00K OHM 1% .25 WATT	COR - NA55
0053A					R11	
0054	00001.000	EA		0539370-0404	RES FIX FILM 1.58K OHM 1% .25 WATT	COR - NA55
0054A					R12	
0056	00001.000	EA		0972757-0025	CAP FIX CER .01MF 10% 50V	
0056A					C95	
0058	00012.000	EA		0972763-0009	CAP,FIXED .0047MF 50 VOLTS	004222-MC105E472Z
0058A					C74 C75 C80 C81 C82 C83 C85	
0058B					C94 C97 C108 C109 C121	
0059	00087.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0059A					C1 THRU C19 C21 C23 C25 C27	
0059B					C29 C31 C33 C35 C37 C39 C41	
0059C					C43 C45 C47 C49 C51 C53 C55	
0059D					C56 C57 C59 THRU C73 C76	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-3

APPD. MFG — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-5003 — REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 6 of — PART NUMBER LM2261980-5003 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0059E					THRU C79 C84 C87 THRU C90	
0059F					C92 C93 C98 THRU C103 C106	
0059G					C107 C114 THRU C117 C120	
0059H					C122 THRU C125 C127 C128	
0059I					C129 C130 C131	
0060	00020.000	EA		0972924-0014	CAP FIX TANT SOLID 15 MFD 10 % 20 VOLT	QPL -M39003/1-2289
0060A					C20 C22 C24 C26 C28 C30 C32	
0060B					C34 C36 C38 C40 C42 C44 C46	
0060C					C48 C50 C52 C54 C91 C104	
0061	00001.000	EA		0222222-7470	NETWORK SN7470N	-SN7470N
0061A					UF3	
0062	00001.000	EA		0800118-0008	RESISTOR 1.0KOHMS DIL PULL UP 16 PINS	BEC -898IR1.0K
0062A					UC8	
0063	00003.000	EA		0972924-0004	CAP FIX TANT SOLID 39 MFD 10 % 10 VOLT	QPL -M39003/1-2259
0063A					C105 C118 C132	
0069	00001.000	EA		0972932-0001	DIODE IN9148	SEE TI- DRAWING
0069A					CR14	
0081	00001.000	EA		0996508-0001	IC,74LS393N DUAL BINARY COUNTER	001295-74LS393N
0081A					UP1	
0082	00001.000	EA		0222222-7408	NETWORK-SN7408N	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-3

APPD. MFG — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-5003 — REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED

DATE 08/01/80 **LIST OF MATERIAL** PAGE 7 of

PART NUMBER LM2261980-5003 REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0082A					UR1	
0085	00011.000	EA		0972946-0001	RES FIX 4.7K OHM 5 % .25 W CARBON FILM	ROH - R-25
0085A					R13 THRU R18 R40 R41 R42	
0085B					R43 R44	
0086	00006.000	EA		0972946-0025	RES FIX 22.0 OHM 5 % .25 W.CARBON FILM	ROH - R-25
0086A					R3 R4 R5 R6 R7 R8	
0090	00001.000	EA		0972757-0021	CAP, FIX, CERAMIC, 4700PF, 50V 10%	
0090A					C126	
0094	00001.000	EA		0996780-0001	IC,SN74LS33N QUAD POSITIVE-NOR BUFFER	001295-SN74LS33N
0094A					UA6	
0097	00002.000	EA		0219402-7258	NETWORK SN74S258N	
0097A					UE1 UE2	

DRAFTSMAN	DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE AUTO-INSERTED PARTS LIST FOR 2261980-3	
APPD-MFG	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO	PART NUMBER LM2261980-5003 REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — **LIST OF MATERIAL** — PAGE 1 of — PART NUMBER LM2261980-5004 REV AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2261981-0001	PWB,MEMORY CONTROLLER,W/ECC,990/12	
0005	00001.000	EA		0219402-7400	NETWORK SN74S00N	
0005A					UK1	
0006	00002.000	EA		0972900-7400	NETWORK SN74LS00N	TI -SN74LS00N
0006A					UG2 UP4	
0007	00001.000	EA		0972900-7402	NETWORK,SN74LS02N	
0007A					UE4	
0008	00001.000	EA		0219402-7403	NETWORK SN74S03N	
0008A					UH5	
0009	00001.000	EA		0219402-7404	NETWORK SN74S04N	
0009A					UH3	
0010	00002.000	EA		0972900-7404	NETWORK SN74LS04N	
0010A					UJ3 UF2	
0011	00001.000	EA		0972749-0001	NETWORK, SN74LS08N	
0011A					UC4	
0012	00001.000	EA		0972900-7410	NETWORK SN74LS10N	
0012A					UD4	
0013	00001.000	EA		0219402-7430	NETWORK SN74S30N	
0013A					UJ7	
0014	00002.000	EA		0996136-0001	IC,SN74LS257N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS257N

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-4

APPD-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5004 REV AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — **LIST OF MATERIAL** — PAGE 2 of — PART NUMBER LM2261980-5004 REV AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0014A					UP9 UE6	
0015	00002.000	EA		0972900-7432	NETWORK SN74LS32N	TI -SN74LS32N
0015A					UG6 UH4	
0016	00001.000	EA		0972900-7451	NETWORK SN74LS51N	TI -SN74LS51N
0016A					UG3	
0017	00002.000	EA		0972900-7454	NETWORK SN74LS54N	TI -SN74LS54N
0017A					UH1 UD1	
0018	00005.000	EA		0219402-7474	NETWORK SN74S74N	
0018A					UJ1 UJ2 UK4 UH2 UJ4	
0019	00005.000	EA		0972900-7474	NETWORK SN74LS74N	
0019A					UG4 UF1 UF4 UG5 UE3	
0020	00004.000	EA		0219402-7486	NETWORK SN74S86N	
0020A					UF9 UF7 UF8 UF6	
0021	00001.000	EA		0972782-0001	NETWORK SN74LS132N	TI -SN74LS132N
0021A					UJ5	
0022	00002.000	EA		0219402-7138	NETWORK SN74S138N	
0022A					UG8 UG7	
0023	00002.000	EA		0996305-0001	IC,SN74S169 UP/DOWN COUNTER,4 BIT	001295-SN74S169
0023A					UD6 UC3	
0024	00001.000	EA		0972900-7175	NETWORK SN74LS175N	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-4

APPD-MFG. DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5004 REV AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 3 of — PART NUMBER LM2261980-5004 REV AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0024A					UE8	
0026	00002.000	EA		0996136-0002	IC,SN74LS258N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS258N
0026A					UH8 UJ9	
0028	00006.000	EA		0219402-7280	NETWORK SN74S280N	TI -SN74S280N
0028A					UK6 UK7 UK8 UK9 UJ6 UJ8	
0029	00002.000	EA		0972652-0001	NETWORK SN74LS283N	
0029A					UB6 UC6	
0031	00018.000	EA		0972787-0004	NETWORK SN74LS368N	
0031A					UR1 UR2 UP2 UR6 UR7 UH6 UP7	
0031B					UR8 UR9 UC2 UB4 UA7 UR4 UR5	
0031C					UE7 UP5 UB3 UB2	
0034	00001.000	EA		0974674-0001	NETWORK SN75138N	
0034A					UB7	
0035	00006.000	EA		0972583-0001	NETWORK,SN75365	TI- -SN75365
0035A					UL1 UL2 UM1 UM2 UN1 UN2	
0037	00066.000	EA		0996680-0001	IC, 16K RAM, (SEL)	001295-TMS4116/ZA0727
0037A					UM4 THRU UN25 UM4 THRU UR25	
0037B					UL4 THRU UL25	
0039	00002.000	EA		0996138-0001	IC,SN74LS266N 2-INPUT EXCLUSIVE-NOR GATE	TI -SN74LS266N
0039A					UD8 UB8	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-4

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5004 REV AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 4 of — PART NUMBER LM2261980-5004 REV AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0040	00001.000	EA		0972037-2680	NETWORK,RES 680 OHM 2% 16PIN 8ELEMENT	073138-898-3-R680
0040A					UD7	
0041	00001.000	EA		0800118-0004	RESISTOR 220 OHMS DIL PULL UP 16 PINS	BEC -8981R220
0041A					UH9	
0042	00003.000	EA		0972037-L220	NETWORK,RES 22 OHM 2% 16PIN 8ELEMENT	073138-898-3-R22
0042A					UL3 UM3 UN3	
0043	00001.000	EA		0972946-0041	RES FIX 100 OHM 5 % .25 W CARBON FILM	ROH - R-25
0043A					R9	
0044	00005.000	EA		0972946-0049	RES FIX 220 OHM 5 % .25 W CARBON FILM	ROH - R-25
0044A					R1 R2 R29 R30 R31	
0045	00001.000	EA		0972946-0053	RES FIX 330 OHM 5 % .25 W CARBON FILM	ROH - R-25
0045A					R22	
0046	00001.000	EA		0972946-0061	RES FIX 680 OHM 5 % .25 W CARBON FILM	ROH - R-25
0046A					R21	
0047	00008.000	EA		0972946-0065	RES FIX 1.0K OHM 5% .25 W CARBON FILM	ROH - R-25
0047A					R10 R19 R20 R23 R24 R25 R37	
0047B					R38	
0048	00004.000	EA		0972946-0089	RES FIX 10K OHM 5% .25 W CARBON FILM	ROH - R-25
0048A					R32 R33 R34 R35	
0049	00001.000	EA		0972946-0095	RES FIX 18K OHM 5% .25 W CARBON FILM	ROH - R-25

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-4

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5004 REV AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 5 of — PART NUMBER LM2261980-5004 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0049A					R36	
0050	00001.000	EA		0972946-0105	RES FIX 47 K OHM 5 % .25 W CARBON FILM	ROH - R-25
0050A					R26	
0051	00001.000	EA		0972946-0121	RES FIX 220K OHM 5 % .25 W CARBON FILM	ROH - R-25
0051A					R39	
0052	00002.000	EA		0972946-0093	RES FIX 15K OHM 5% .25 W CARBON FILM	ROH - R-25
0052A					R27 R28	
0053	00001.000	EA		0539370-0385	RES FIX FILM 1.00K OHM 1% .25 WATT	COR - NA55
0053A					R11	
0054	00001.000	EA		0539370-0404	RES FIX FILM 1.58K OHM 1% .25 WATT	COR - NA55
0054A					R12	
0056	00001.000	EA		0972757-0025	CAP FIX CER .01MF 10% 50V	
0056A					C95	
0058	00012.000	EA		0972763-0009	CAP,FIXED .0047MF 50 VOLTS	004222-MC105E472Z
0058A					C74 C75 C80 C81 C82 C83 C85	
0058B					C94 C97 C108 C109 C121	
0059	00087.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0059A					C1 THRU C19 C21 C23 C25 C27	
0059B					C29 C31 C33 C35 C37 C39 C41	
0059C					C43 C45 C47 C49 C51 C53 C55	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-4

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5004 | REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 6 of — PART NUMBER LM2261980-5004 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0059D					C56 C57 C59 THRU C73 C76	
0059E					THRU C79 C84 C87 THRU C90	
0059F					C92 C93 C98 THRU C103 C106	
0059G					C107 C114 THRU C117 C120	
0059H					C122 THRU C125 C127 C128	
0059I					C129 C130 C131	
0060	00020.000	EA		0972924-0014	CAP FIX TANT SOLID 15 MFD 10 % 20 VOLT	QPL -M39003/1-2289
0060A					C20 C22 C24 C26 C28 C30 C32	
0060B					C34 C36 C38 C40 C42 C44 C46	
0060C					C48 C50 C52 C54 C91 C104	
0061	00001.000	EA		0222222-7470	NETWORK SN7470N	-SN7470N
0061A					UF3	
0062	00001.000	EA		0800118-0008	RESISTOR 1.0KOHMS DIL PULL UP 16 PINS	BEC -89R1R1.0K
0062A					UC8	
0063	00003.000	EA		0972924-0006	CAP FIX TANT SOLID 39 MFD 10 % 10 VOLT	QPL -M39003/1-2259
0063A					C105 C118 C132	
0069	00001.000	EA		0972932-0001	DIODE 1N914B	SEE TI- DRAWING
0069A					CR14	
0081	00001.000	EA		0996508-0001	IC,74LS393N DUAL BINARY COUNTER	001295-74LS393N
0081A					UP1	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-4

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5004 | REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED

DATE 08/01/80 **LIST OF MATERIAL** PAGE 7 of

PART NUMBER LM2261980-5004 REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	00001.000	EA		0222222-7408	NETWORK-SN7408N	
0002A					UG1	
0009	00011.000	EA		0972946-0081	RES FIX 4.7K OHM 5 % .25 W CARBON FILM	ROH - R-25
0009A					R13 THRU R18 R40 R41 R42	
0009B					R43 R44	
0006	00006.000	EA		0972946-0025	RES FIX 22.0 OHM 5 % .25 W.CARBON FILM	ROH - R-25
0006A					R3 R4 R5 R6 R7 R8	
0090	00001.000	EA		0972757-0021	CAP. FIX, CERAMIC, 4700PF, 50V 10%	
0090A					C126	
0094	00001.000	EA		0996780-0001	IC,SN74LS33N QUAD POSITIVE-NOR BUFFER	001295-SN74LS33N
0094A					UA6	
0097	00002.000	EA		0219402-7258	NETWORK SN74S258N	
0097A					UE1 UE2	

DRAFTSMAN	DATE	CKD DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						AUTO-INSERTED PARTS LIST FOR 2261980-4
APPD MFG	DATE	APPD PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO
						PART NUMBER LM2261980-5004 REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM2261980-5005 REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2262031-0001	PWB,MEMORY CONTROLLER W/FCC,990/12	
0005	00001.000	EA		0219402-7400	NETWORK SN74S00N	
0005A					UK1	
0006	00002.000	EA		0972900-7400	NETWORK SN74LS00N	TI -SN74LS00N
0006A					UG2 UP4	
0007	~~00001.000~~	EA		~~0972900-7402~~	~~NETWORK,SN74LS02N~~	
0007A					UE4	
0008	00001.000	EA		0219402-7405	NETWORK SN74S05N	
0008A					UH5	
0009	00001.000	EA		0219402-7404	NETWORK SN74S04N	
0009A					UH3	
0010	00001.000	EA		0972900-7404	NETWORK SN74LS04N	
0010A					UJ3	
0011	00001.000	EA		0972749-0001	NETWORK, SN74LS08N	
0011A					UC4	
0012	00001.000	EA		0972900-7410	NETWORK SN74LS10N	
0012A					UD4	
0013	00001.000	EA		0219402-7430	NETWORK SN74S30N	
0013A					UJ7	
0014	00002.000	EA		0996136-0001	IC,SN74LS257N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS257N

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-5

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5005 REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM2261980-5005 REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0014A					UP9 UE6	
0015	00002.000	EA		0972900-7432	NETWORK SN74LS32N	TI -SN74LS32N
0015A					UG6 UH4	
0016	00001.000	EA		0972900-7451	NETWORK SN74LS51N	TI -SN74LS51N
0016A					UG3	
0017	00002.000	EA		0972900-7454	NETWORK SN74LS54N	TI -SN74LS54N
0017A					UH1 UD1	
0018	00005.000	EA		0219402-7474	NETWORK SN74S74N	
0018A					UJ1 UJ2 UK4 UH2 UJ4	
0019	00005.000	EA		0972900-7474	NETWORK SN74LS74N	
0019A					UG4 UF1 UF4 UG5 UE3	
0020	00004.000	EA		0219402-7486	NETWORK SN74S86N	
0020A					UF9 UF7 UF8 UF6	
0021	00001.000	EA		0972782-0001	NETWORK SN74LS132N	TI -SN74LS132N
0021A					UJ5	
0022	00002.000	EA		0219402-7138	NETWORK SN74S138N	
0022A					UG8 UG7	
0023	00002.000	EA		0996305-0001	IC,SN74S169 UP/DOWN COUNTER,4 BIT	001295-SN74S169
0023A					UD6 UC3	
0024	00001.000	EA		0972900-7175	NETWORK SN74LS175N	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-5

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5005 REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — **LIST OF MATERIAL** — PAGE 3 of — PART NUMBER LM2261980-5005 — REV AD

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0024A					UE8	
0026	00002.000	EA		0996136-0002	IC,SN74LS258N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS258N
0026A					UH8 UJ9	
0028	00006.000	EA		0219402-7288	NETWORK SN74S280N	TI -SN74S280N
0028A					UK6 UK7 UK8 UK9 UJ6 UJ8	
0029	00002.000	EA		0972652-0001	NETWORK SN74LS283N	
0029A					UB6 UC6	
0031	00018.000	EA		0972787-0004	NETWORK SN74LS368N	
0031A					UR1 UR2 UP2 UR6 UR7 UH6 UP7	
0031B					UR8 UR9 UC2 UB4 UA7 UR4 UR5	
0031C					UE7 UP5 UB3 UB2	
0034	00001.000	EA		0974674-0001	NETWORK SN75138N	
0034A					UB7	
0039	00002.000	EA		0996138-0001	IC,SN74LS266N 2-INPUT EXCLUSIVE-NOR GATE	TI -SN74LS266N
0039A					UD8 UB8	
0040	00001.000	EA		0972037-2680	NETWORK,RES 680 OHM 2% 16PIN BELEMENT	073138-898-3-R680
0040A					UD7	
0041	00001.000	EA		0972037-2220	NETWORK,RES 220 OHM 2% 16PIN BELEMENT	
0041A					UH9	
0043	00001.000	EA		0972946-0041	RES FIX 100 OHM 5 % .25 W CARBON FILM	ROH - R-25

DRAFTSMAN DATE — CKD DRAFTSMAN DATE — DESIGN ENGINEER DATE — TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-5

APPD MFG. DATE — APPD PROJECT ENGINEER DATE — RELEASED DATE — PROJECT NO — PART NUMBER LM2261980-5005 — REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — **LIST OF MATERIAL** — PAGE 4 of — PART NUMBER LM2261980-5005 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0043A					R9	
0044	00007.000	EA		0972946-0049	RES FIX 220 OHM 5 % .25 W CARBON FILM	ROH - R-25
0044A					R1 R2 R29 R30 R31 R47 R48	
0045	00001.000	EA		0972946-0053	RES FIX 330 OHM 5 % .25 W CARBON FILM	ROH - R-25
0045A					R22	
0046	00002.000	EA		0972946-0061	RES FIX 680 OHM 5 % .25 W CARBON FILM	ROH - R-25
0046A					R21 R19	
0047	00007.000	EA		0972946-0065	RES FIX 1.0K OHM 5% .25 W CARBON FILM	ROH - R-25
0047A					R10 R20 R23 R24 R25 R37	
0047B					R38	
0048	00004.000	EA		0972946-0089	RES FIX 10K OHM 5% .25 W CARBON FILM	ROH - R-25
0048A					R33 R34 R35 R50	
0049	00001.000	EA		0972946-0115	RES FIX 120K OHM 5 % .25 W CARBON FILM	ROH - R-25
0049A					R36	
0050	00001.000	EA		0972946-0105	RES FIX 47 K OHM 5 % .25 W CARBON FILM	ROH - R-25
0050A					R26	
0051	00001.000	EA		0972946-0121	RES FIX 220K OHM 5 % .25 W CARBON FILM	ROH - R-25
0051A					R39	
0052	00001.000	EA		0972946-0093	RES FIX 15K OHM 5% .25 W CARBON FILM	ROH - R-25
0052A					R27	

DRAFTSMAN DATE — CKD DRAFTSMAN DATE — DESIGN ENGINEER DATE — TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-5

APPD MFG. DATE — APPD PROJECT ENGINEER DATE — RELEASED DATE — PROJECT NO — PART NUMBER LM2261980-5005 — REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 5 of — PART NUMBER LM2261980-5005 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0053	00001.000	EA		0539370-0385	RES FIX FILM 1.00K OHM 1% .25 WATT	COR - NA55
0053A					R11	
0054	00001.000	EA		0539370-0357	RES FIX FILM 511 OHM 1% .25 WATT	COR - NA55
0054A					R12	
0055	00002.000	EA		0972753-0012	CAP,FIXED 220PF 25 WVDC 2.0%	UC -C500221G
0055A					C86 C95	
0056	00001.000	EA		0972757-0025	CAP FIX CER .01MF 10% 50V	
0056A					C95	
0058	00012.000	EA		0972763-0009	CAP,FIXED .0047MF 50 VOLTS	004222-MC105E472Z
0058A					C74 C75 C80 C81 C82 C83 C85	
0058B					C96 C97 C108 C109 C121	
0059	00087.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0059A					C1 THRU C19 C21 C23 C25 C27	
0059B					C29 C31 C33 C35 C37 C39 C41	
0059C					C43 C45 C47 C49 C51 C53 C55	
0059D					C56 C57 C59 THRU C73 C76	
0059E					THRU C79 C84 C87 THRU C90	
0059F					C92 C93 C98 THRU C103 C106	
0059G					C107 C114 THRU C117 C120	
0059H					C122 THRU C125 C127 C128	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-5

APPD-MFG — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-5005 — REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 6 of — PART NUMBER LM2261980-5005 — REV ~~AE~~ AF

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0059I					C129 C130 C131	
0060	00020.000	EA		0972924-0014	CAP FIX TANT SOLID 15 MFD 10 % 20 VOLT	QPL -M39003/1-2289
0060A					C20 C22 C24 C26 C28 C30 C32	
0060B					C34 C36 C38 C40 C42 C44 C46	
0060C					C48 C50 C52 C54 C91 C104	
0061	00001.000	EA		0222222-7470	NETWORK SN7470N	-SN7470N
0061A					UF3	
0062	00001.000	EA		0800118-0008	RESISTOR 1.0KOHMS DIL PULL UP 16 PINS	BEC -8981R1.0K
0062A					UC8	
0063	00003.000	EA		0972924-0006	CAP FIX TANT SOLID 39 MFD 10 % 10 VOLT	QPL -M39003/1-2259
0063A					C105 C118 C132	
0064	00001.000	EA		0972932-0001	DIODE 1N9148	SEE TI- DRAWING
0064A					CR14	
0081	00001.000	EA		0996508-0001	IC,74LS393N DUAL BINARY COUNTER	001295-74LS393N
0081A					UP1	
0082	00001.000	EA		0222222-7408	NETWORK-SN7408N	
0082A					UG1	
0085	00011.000	EA		0972946-0081	RES FIX 4.7K OHM 5 % .25 W CARBON FILM	ROH - R-25
0085A					R13 THRU R18 R40 R41 R42	
0085B					R43 R44	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-5

APPD-MFG — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-5005 — REV ~~AE~~ AF

TEXAS INSTRUMENTS INCORPORATED

DATE 08/01/80 **LIST OF MATERIAL** PAGE 7 of

PART NUMBER LM2261980-5005 REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0086	00006.000	EA		0972946-0025	RES FIX 22.0 OHM 5 % .25 W.CARBON FILM	ROH - R-25
0086A					R3 R4 R5 R6 R7 R8	
0090	00001.000	EA		0972757-0021	CAP, FIX, CERAMIC, 4700PF, 50V 10%	
0090A					C126	
0094	00001.000	EA		0996780-0001	IC,SN74LS33N QUAD POSITIVE-NOR BUFFER	001295-SN74LS33N
0094A					UA6	
0097	00002.000	EA		0219402-7258	NETWORK SN74S258N	
0097A					UE1 UE2	
0102	00001.000	EA		0972946-0088	RES FIX 9.1K OHM 5 % .25 W CARBON FILM	ROH - R-25
0102A					R28	
0103	00001.000	EA		0996424-0001	IC,SN74LS375N 4 BIT BISTABLE LATCHES	001295-SN74LS375N
0103A					UA8	
0104	00002.000	EA		0231784-6002	DIODE- 4 PELLET, SILICON,MULTI	GE -HPD400
0104A					CR16 CR17	
0105	00001.000	EA		0972946-0075	RES FIX 2.7K OHM 5 % .25 W CARBON FILM	ROH - R-25
0105A					R32	
0106	00001.000	EA		0972784-0002	NETWORK SN74LS14N	
0106A					UF2	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE AUTO-INSERTED PARTS LIST FOR 2261980-5

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO

PART NUMBER LM2261980-5005 REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM2261980-5006 REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2262031-0001	PWB,MEMORY CONTROLLER W/ECC,990/12	
0005	00001.000	EA		0219402-7400	NETWORK SN74S00N	
0005A					UK1	
0006	00002.000	EA		0972900-7400	NETWORK SN74LS00N	TI -SN74LS00N
0006A					UG2 UP4	
0007	00001.000	EA		0972900-7402	NETWORK,SN74LS02N	
0007A					UE4	
0008	00001.000	EA		0219402-7405	NETWORK SN74S05N	
0008A					UH5	
0009	00001.000	EA		0219402-7404	NETWORK SN74S04N	
0009A					UH3	
0010	00001.000	EA		0972900-7404	NETWORK SN74LS04N	
0010A					UJ3	
0011	00001.000	EA		0972749-0001	NETWORK, SN74LS08N	
0011A					UC4	
0012	00001.000	EA		0972900-7410	NETWORK SN74LS10N	
0012A					UD4	
0013	00001.000	EA		0219402-7430	NETWORK SN74S30N	
0013A					UJ7	
0014	00002.000	EA		0996136-0001	IC,SN74LS257N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS257N

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-6

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5006 REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM2261980-5006 REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0014A					UP9 UE6	
0015	00002.000	EA		0972900-7432	NETWORK SN74LS32N	TI -SN74LS32N
0015A					UG6 UH4	
0016	00001.000	EA		0972900-7451	NETWORK SN74LS51N	TI -SN74LS51N
0016A					UG3	
0017	00002.000	EA		0972900-7454	NETWORK SN74LS54N	TI -SN74LS54N
0017A					UH1 UD1	
0018	00005.000	EA		0219402-7474	NETWORK SN74S74N	
0018A					UJ1 UJ2 UK4 UH2 UJ4	
0019	00005.000	EA		0972900-7474	NETWORK SN74LS74N	
0019A					UG4 UF1 UF4 UG5 UE3	
0020	00004.000	EA		0219402-7486	NETWORK SN74S86N	
0020A					UF9 UF7 UF8 UF6	
0021	00001.000	EA		0972782-0001	NETWORK SN74LS132N	TI -SN74LS132N
0021A					UJ5	
0022	00002.000	EA		0219402-7138	NETWORK SN74S138N	
0022A					UG8 UG7	
0023	00002.000	EA		0996305-0001	IC,SN74S169 UP/DOWN COUNTER,4 BIT	001295-SN74S169
0023A					UD6 UC3	
0024	00001.000	EA		0972900-7175	NETWORK SN74LS175N	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-6

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5006 REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 3 of — PART NUMBER LM2261980-5006 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0024A					UE8	
0026	00002.000	EA		0996136-0002	IC,SN74LS258N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS258N
0026A					UH8 UJ9	
0028	00006.000	EA		0219402-7280	NETWORK SN74S280N	TI -SN74S280N
0028A					UK6 UK7 UK8 UK9 UJ6 UJ8	
0029	00002.000	EA		0972652-0001	NETWORK SN74LS283N	
0029A					UR6 UC6	
0031	00018.000	EA		0972787-0004	NETWORK SN74LS368N	
0031A					UR1 UR2 UP2 UR6 UR7 UH6 UP7	
0031B					UR8 UR9 UC2 UB4 UA7 UR4 UR5	
0031C					UE7 UP5 UR3 UB2	
0034	00001.000	EA		0974674-0001	NETWORK SN75138N	
0034A					UB7	
0035	00006.000	EA		0972583-0001	NETWORK,SN75365	TI- -SN75365
0035A					UL1 UL2 UM1 UM2 UN1 UN2	
0037	00022.000	EA		0996680-0001	IC, 16K RAM, (SEL)	001295-TMS4116/7A0727
0037A					UN4 THRU UN25	
0039	00002.000	EA		0996138-0001	IC,SN74LS266N 2-INPUT EXCLUSIVE-NOR GATE	TI -SN74LS266N
0039A					UD8 UB8	
0040	00001.000	EA		0972037-2680	NETWORK,RES 680 OHM 2% 16PIN SELEMENT	073138-898-3-R680

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-6

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5006 | REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 4 of — PART NUMBER LM2261980-5006 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0040A					UD7	
0041	00001.000	EA		0972037-2220	NETWORK,RES 220 OHM 2% 16PIN SELEMENT	
0041A					UH9	
0042	00003.000	EA		0972037-1220	NETWORK,RES 22 OHM 2% 16PIN SELEMENT	073138-898-3-R22
0042A					UL9 UM3 UN3	
0043	00001.000	EA		0972946-0041	RES FIX 100 OHM 5 % .25 W CARBON FILM	ROH - R-25
0043A					R9	
0044	00007.000	EA		0972946-0049	RES FIX 220 OHM 5 % .25 W CARBON FILM	ROH - R-25
0044A					R1 R2 R29 R30 R31 R47 R48	
0045	00001.000	EA		0972946-0053	RES FIX 330 OHM 5 % .25 W CARBON FILM	ROH - R-25
0045A					R22	
0046	00002.000	EA		0972946-0061	RES FIX 680 OHM 5 % .25 W CARBON FILM	ROH - R-25
0046A					R21 R19	
0047	00007.000	EA		0972946-0065	RES FIX 1.0K OHM 5% .25 W CARBON FILM	ROH - R-25
0047A					R10 R20 R23 R24 R25 R37	
0047B					R38	
0048	00004.000	EA		0972946-0089	RES FIX 10K OHM 5% .25 W CARBON FILM	ROH - R-25
0048A					R33 R34 R35 R50	
0049	00001.000	EA		0972946-0115	RES FIX 120K OHM 5 % .25 W CARBON FILM	ROH - R-25
0049A					R36	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-6

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5006 | REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 5 of — PART NUMBER LM2261980-5006 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0050	00001.000	EA		0972946-0105	RES FIX 47 K OHM 5 % .25 W CARBON FILM	ROH - R-25
0050A					R26	
0051	00001.000	EA		0972946-0121	RES FIX 220K OHM 5 % .25 W CARBON FILM	ROH - R-25
0051A					R39	
0052	00001.000	EA		0972946-0093	RES FIX 15K OHM 5% .25 W CARBON FILM	ROH - R-25
~~0052A~~					R27	
0053	00001.000	EA		0539370-0385	RES FIX FILM 1.00K OHM 1% .25 WATT	COR - NA55
0053A					R11	
0054	00001.000	EA		0539370-0357	RES FIX FILM 511 OHM 1% .25 WATT	COR - NA55
0054A					R12	
0055	00002.000	EA		0972753-0012	CAP,FIXED 220PF 25 WVDC 2.0%	UC -C50D221G
0055A					C86 C96	
0056	00001.000	EA		0972757-0025	CAP FIX CER .01MF 10% 50V	
0056A					C99	
0058	00012.000	EA		0972763-0009	CAP,FIXED .0047MF 50 VOLTS	004222-MC105E472Z
0058A					C74 C75 C88 C81 C82 C83 C85	
0058B					C94 C97 C108 C109 C121	
0059	00067.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0059A					C1 THRU C19 C21 C23 C25 C27	
0059B					C29 C31 C33 C35 C37 C39 C41	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-6

APPD MFG. — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2261980-5006 — REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 6 of — PART NUMBER LM2261980-5006 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
~~0059C~~					C43 C45 C47 C49 C51 C53 C55	
0059D					C56 C57 C59 THRU C73 C76	
0059E					THRU C79 C84 C87 THRU C90	
0059F					C92 C93 C98 THRU C103 C106	
0059G					C107 C114 THRU C117 C120	
0059H					C122 THRU C125 C127 C128	
00591					C129 C130 C131	
0060	00020.000	EA		0972924-0014	CAP FIX TANT SOLID 15 MFD 10 % 20 VOLT	QPL -M39003/1-2289
0060A					C20 C22 C24 C26 C28 C30 C32	
0060B					C34 C36 C38 C40 C42 C44 C46	
0060C					C48 C50 C52 C54 C91 C104	
0061	00001.000	EA		0222222-7470	NETWORK SN7470N	-SN7470N
0061A					UF3	
0062	00001.000	EA		0800118-0008	RESISTOR 1.0KOHMS DIL PULL UP 16 PINS	BEC -8981R1.0K
0062A					UC8	
0063	00003.000	EA		0972924-0006	CAP FIX TANT SOLID 39 MFD 10 % 10 VOLT	QPL -M39003/1-2259
0063A					C105 C118 C132	
0069	00001.000	EA		0972932-0001	DIODE 1N9148	SEE TI- DRAWING
0069A					CR14	
0081	00001.000	EA		0996508-0001	IC,74LS393N DUAL BINARY COUNTER	001295-74LS393N

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-6

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-5006 — REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 7 of — PART NUMBER LM2261980-5006 — REV AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0081A					UP1	
0082	00001.000	EA		0222222-7408	NETWORK-SN7408N	
0082A					UG1	
0085	00011.000	EA		0972946-0081	RES FIX 4.7K OHM 5 % .25 W CARBON FILM	ROH - R-25
0085A					R13 THRU R18 R40 R41 R42	
0085B					R43 R44	
0086	00006.000	EA		0972946-0025	RES FIX 22.0 OHM 5 % .25 W.CARBON FILM	ROH - R-25
0086A					R3 R4 R5 R6 R7 R8	
0090	00001.000	EA		0972757-0021	CAP, FIX, CERAMIC, 4700PF, 50V 10%	
0090A					C126	
0094	00001.000	EA		0996780-0001	IC,SN74LS33N QUAD POSITIVE-NOR BUFFER	001295-SN74LS33N
0094A					UA6	
0097	00002.000	EA		0219402-7258	NETWORK SN74S258N	
0097A					UE1 UE2	
0102	00001.000	EA		0972946-0088	RES FIX 9.1K OHM 5 % .25 W CARBON FILM	ROH - R-25
0102A					R28	
0103	00001.000	EA		0996424-0001	IC,SN74LS375N 4 BIT BISTABLE LATCHES	001295-SN74LS375N
0103A					UA8	
0104	00002.000	EA		0231784-6002	DIODE- 4 PELLET, SILICON,MULTI	GE -HPD400
0104A					CR16 CR17	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-6

APPD MFG. DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5006 | REV AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 8 of — PART NUMBER LM2261980-5006 — REV AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0105	00001.000	EA		0972946-0075	RES FIX 2.7K OHM 5 % .25 W CARBON FILM	ROH - R-25
0105A					R32	
0106	00001.000	EA		0972784-0002	NETWORK SN74LS14N	
0106A					UF2	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-6

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5006 | REV AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM2261980-5007 REV ~~AB~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2262031-0001	PWB,MEMORY CONTROLLER W/ECC,990/12	
0005	00001.000	EA		0219402-7400	NETWORK SN74S00N	
0005A					UK1	
0006	00002.000	EA		0972900-7400	NETWORK SN74LS00N	TI -SN74LS00N
0006A					UG2 UP4	
0007	00001.000	EA		0972900-7402	NETWORK,SN74LS02N	
0007A					UE4	
0008	00001.000	EA		0219402-7405	NETWORK SN74S05N	
0008A					UH5	
0009	00001.000	EA		0219402-7404	NETWORK SN74S04N	
0009A					UH3	
0010	00001.000	EA		0972900-7404	NETWORK SN74LS04N	
0010A					UJ3	
0011	00001.000	EA		0972749-0001	NETWORK, SN74LS08N	
0011A					UC4	
0012	00001.000	EA		0972900-7410	NETWORK SN74LS10N	
0012A					UD4	
0013	00001.000	EA		0219402-7430	NETWORK SN74S30N	
0013A					UJ7	
0014	00002.000	EA		0996136-0001	IC,SN74LS257N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS257N

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-7

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5007 REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM2261980-5007 REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0014A					UP9 UE6	
0015	00002.000	EA		0972900-7432	NETWORK SN74LS32N	TI -SN74LS32N
0015A					UG6 UH4	
0016	00001.000	EA		0972900-7451	NETWORK SN74LS51N	TI -SN74LS51N
0016A					UG3	
0017	00002.000	EA		0972900-7454	NETWORK SN74LS54N	TI -SN74LS54N
0017A					UH1 UD1	
0018	00005.000	EA		0219402-7474	NETWORK SN74S74N	
0018A					UJ1 UJ2 UK4 UH2 UJ4	
0019	00005.000	EA		0972900-7474	NETWORK SN74LS74N	
0019A					UG4 UF1 UF4 UG5 UE3	
0020	00004.000	EA		0219402-7486	NETWORK SN74S86N	
0020A					UF9 UF7 UF8 UF6	
0021	00001.000	EA		0972782-0001	NETWORK SN74LS132N	TI -SN74LS132N
0021A					UJ5	
0022	00002.000	EA		0219402-7138	NETWORK SN74S138N	
0022A					UG8 UG7	
0023	00002.000	EA		0996305-0001	IC,SN74S169 UP/DOWN COUNTER,4 BIT	001295-SN74S169
0023A					UD6 UC3	
0024	00001.000	EA		0972900-7175	NETWORK SN74LS175N	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-7

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5007 REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 3 of — PART NUMBER LM2261980-5007 REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0024A					UE8	
0026	00002.000	EA		0996136-0002	IC,SN74LS258N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS258N
0026A					UH8 UJ9	
0028	00006.000	EA		0219402-7280	NETWORK SN74S280N	TI -SN74S280N
0028A					UK6 UK7 UK8 UK9 UJ6 UJ8	
0029	00002.000	EA		0972652-0001	NETWORK SN74LS283N	
0029A					UB6 UC6	
0031	00018.000	EA		0972787-0004	NETWORK SN74LS368N	
0031A					UR1 UR2 UP2 UR6 UR7 UH6 UP7	
0031B					UR8 UR9 UC2 UB4 UA7 UR4 UR5	
0031C					UE7 UP5 UB3 UB2	
0034	00001.000	EA		0974674-0001	NETWORK SN75138N	
0034A					UB7	
0035	00008.000	EA		0972983-0001	NETWORK,SN75365	TI- -SN75365
0035A					UL1 UL2 UM1 UM2 UN1 UN2	
0037	00044.000	EA		0996680-0001	IC, 16K RAM, (SEL)	001295-TMS4116/ZA0727
0037A					UN4 THRU UN25 UM4 THRU UM25	
0039	00002.000	EA		0996138-0001	IC,SN74LS266N 2-INPUT EXCLUSIVE-NOR GATE	TI -SN74LS266N
0039A					UD8 UB8	
0040	00001.000	EA		0972037-2680	NETWORK,RES 680 OHM 2% 16PIN 8ELEMENT	073138-898-3-R680

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-7

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5007 REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 4 of — PART NUMBER LM2261980-5007 REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0040A					UD7	
0041	00001.000	EA		0972037-2220	NETWORK,RES 220 OHM 2% 16PIN 8ELEMENT	
0041A					UH9	
0042	00003.000	EA		0972037-1220	NETWORK,RES 22 OHM 2% 16PIN 8ELEMENT	073138-898-3-R22
0042A					UL3 UM3 UN3	
0043	00001.000	EA		0972946-0041	RES FIX 100 OHM 5 % .25 W CARBON FILM	ROH - R-25
0043A					R9	
0044	00007.000	EA		0972946-0049	RES FIX 220 OHM 5 % .25 W CARBON FILM	ROH - R-25
0044A					R1 R2 R29 R30 R31 R47 R48	
0045	00001.000	EA		0972946-0053	RES FIX 330 OHM 5 % .25 W CARBON FILM	ROH - R-25
0045A					R22	
0046	00002.000	EA		0972946-0061	RES FIX 680 OHM 5 % .25 W CARBON FILM	ROH - R-25
0046A					R21 R19	
0047	00007.000	EA		0972946-0065	RES FIX 1.0K OHM 5% .25 W CARBON FILM	ROH - R-25
0047A					R10 R20 R23 R24 R25 R37	
0047B					R38	
0048	00004.000	EA		0972946-0089	RES FIX 10K OHM 5% .25 W CARBON FILM	ROH - R-25
0048A					R33 R34 R35 R50	
0049	00001.000	EA		0972946-0115	RES FIX 120K OHM 5 % .25 W CARBON FILM	ROH - R-25
0049A					R36	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-7

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5007 REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 5 of — PART NUMBER LM2261980-5007 REV AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0050	00001.000	EA		0972946-0105	RES FIX 47 K OHM 5 % .25 W CARBON FILM	ROH - R-25
0050A					R26	
0051	00001.000	EA		0972946-0121	RES FIX 220K OHM 5 % .25 W CARBON FILM	ROH - R-25
0051A					R39	
0052	00001.000	EA		0972946-0093	RES FIX 15K OHM 5% .25 W CARBON FILM	ROH - R-25
0052A					R27	
0053	00001.000	EA		0539370-0385	RES FIX FILM 1.00K OHM 1% .25 WATT	COR - NA55
0053A					R11	
0054	00001.000	EA		0539370-0357	RES FIX FILM 511 OHM 1% .25 WATT	COR - NA55
0054A					R12	
0055	00002.000	EA		0972753-0012	CAP,FIXED 220PF 25 WVDC 2.0%	UC -C500221G
0055A					C86 C96	
0056	00001.000	EA		0972757-0025	CAP FIX CER .01MF 10% 50V	
0056A					C95	
0058	00012.000	EA		0972763-0009	CAP,FIXED .0047MF 50 VOLTS	004222-MC105E472Z
0058A					C74 C75 C80 C81 C82 C83 C85	
0058B					C94 C97 C108 C109 C121	
0059	00087.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0059A					C1 THRU C19 C21 C23 C25 C27	
0059B					C29 C31 C33 C35 C37 C39 C41	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-7

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM2261980-5007 REV AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 6 of — PART NUMBER LM2261980-5007 REV AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0059C					C43 C45 C47 C49 C51 C53 C55	
0059D					C56 C57 C59 THRU C73 C76	
0059E					THRU C79 C84 C87 THRU C90	
0059F					C92 C93 C98 THRU C103 C106	
0059G					C107 C114 THRU C117 C120	
0059H					C122 THRU C125 C127 C128	
0059I					C129 C130 C131	
0060	00020.000	EA		0972924-0014	CAP FIX TANT SOLID 15 MFD 10 % 20 VOLT	OPL -M39003/1-2289
0060A					C20 C22 C24 C26 C28 C30 C32	
0060B					C34 C36 C38 C40 C42 C44 C46	
0060C					C48 C50 C52 C54 C91 C104	
0061	00001.000	EA		0222222-7470	NETWORK SN7470N	-SN7470N
0061A					UF9	
0062	00001.000	EA		0800118-0008	RESISTOR 1.0KOHMS DIL PULL UP 16 PINS	BEC -898IR1.0K
0062A					UC8	
0063	00003.000	EA		0972924-0006	CAP FIX TANT SOLID 39 MFD 10 % 10 VOLT	OPL -M39003/1-2259
0063A					C105 C118 C132	
0069	00001.000	EA		0972932-0001	DIODE 1N9148	SEE TI- DRAWING
0069A					CR14	
0081	00001.000	EA		0996508-0001	IC,74LS393N DUAL BINARY COUNTER	001295-74LS393N

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-7

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM2261980-5007 REV AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 7 of — PART NUMBER LM2261980-5007 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0081A					UP1	
0082	00001.000	EA		0222222-7408	NETWORK-SN7408N	
0082A					UG1	
0085	00011.000	EA		0972946-0081	RES FIX 4.7K OHM 5 % .25 W CARBON FILM	ROH - R-25
0085A					R13 THRU R18 R40 R41 R42	
0085B					R43 R44	
0086	00006.000	EA		0972946-0025	RES FIX 22.0 OHM 5 % .25 W.CARBON FILM	ROH - R-25
0086A					R3 R4 R5 R6 R7 R8	
0090	00001.000	EA		0972757-0021	CAP, FIX, CERAMIC, 4700PF, 50V 10%	
0090A					C126	
0094	00001.000	EA		0996780-0001	IC,SN74LS33N QUAD POSITIVE-NOR BUFFER	001295-SN74LS33N
0094A					UA6	
0097	00002.000	EA		0219402-7258	NETWORK SN74S258N	
0097A					UE1 UE2	
0102	00001.000	EA		0972946-0088	RES FIX 9.1K OHM 5 % .25 W CARBON FILM	ROH - R-25
0102A					R28	
0103	00001.000	EA		0996424-0001	IC,SN74LS375N 4 BIT BISTABLE LATCHES	001295-SN74LS375N
0103A					UA8	
0104	00002.000	EA		0231784-6002	DIODE- 4 PELLET, SILICON,MULTI	GE -HPD400
0104A					CR16 CR17	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-7

APPD MFG. DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5007 | REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 8 of — PART NUMBER LM2261980-5007 — REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0105	00001.000	EA		0972946-0075	RES FIX 2.7K OHM 5 % .25 W CARBON FILM	ROH - R-25
0105A					R32	
0106	00001.000	EA		0972784-0002	NETWORK SN74LS14N	
0106A					UF2	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-7

APPD MFG. DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5007 | REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM2261980-5008 — REV ~~AB~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2262031-0001	PWB,MEMORY CONTROLLER W/ECC,990/12	
0005	00001.000	EA		0219402-7400	NETWORK SN74S00N	
0005A					UK1	
0006	00002.000	EA		0972900-7400	NETWORK SN74LS00N	TI -SN74LS00N
0006A					UG2 UP4	
0007	00001.000	EA		0972900-7402	NETWORK,SN74LS02N	
0007A					UE4	
0008	00001.000	EA		0219402-7405	NETWORK SN74S05N	
0008A					UH5	
0009	00001.000	EA		0219402-7404	NETWORK SN74S04N	
0009A					UH3	
0010	00001.000	EA		0972900-7404	NETWORK SN74LS04N	
0010A					UJ3	
0011	00001.000	EA		0972749-0001	NETWORK, SN74LS08N	
0011A					UC4	
0012	00001.000	EA		0972900-7410	NETWORK SN74LS10N	
0012A					UD4	
0013	00001.000	EA		0219402-7430	NETWORK SN74S30N	
0013A					UJ7	
0014	00002.000	EA		0996136-0001	IC,SN74LS257N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS257N

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-8

APPD MFG. — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-5008 — REV ~~AB~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM2261980-5008 — REV ~~AB~~ AC

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0014A					UP9 UE6	
0015	00002.000	EA		0972900-7432	NETWORK SN74LS32N	TI -SN74LS32N
0015A					UG6 UH4	
0016	00001.000	EA		0972900-7451	NETWORK SN74LS51N	TI -SN74LS51N
0016A					UG3	
0017	00002.000	EA		0972900-7454	NETWORK SN74LS54N	TI -SN74LS54N
0017A					UH1 UN1	
0018	00005.000	EA		0219402-7474	NETWORK SN74S74N	
0018A					UJ1 UJ2 UK4 UH2 UJ4	
0019	00005.000	EA		0972900-7474	NETWORK SN74LS74N	
0019A					UG4 UF1 UF4 UG5 UE3	
0020	00004.000	EA		0219402-7486	NETWORK SN74S86N	
0020A					UF9 UF7 UF8 UF6	
0021	00001.000	EA		0972782-0001	NETWORK SN74LS132N	TI -SN74LS132N
0021A					UJ5	
0022	00002.000	EA		0219402-7138	NETWORK SN74S138N	
0022A					UG8 UG7	
0023	00002.000	EA		0996305-0001	IC,SN74S169 UP/DOWN COUNTER,4 BIT	001295-SN74S169
0023A					UD6 UC3	
0024	00001.000	EA		0972900-7175	NETWORK SN74LS175N	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-8

APPD MFG. — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-5008 — REV ~~AB~~ AC

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 3 of — PART NUMBER LM2261980-5008 — REV ~~AB~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0024A					UE8	
0026	00002.000	EA		0996136-0002	IC,SN74LS258N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS258N
0026A					UH8 UJ9	
0028	00006.000	EA		0219402-7280	NETWORK SN74S280N	TI -SN74S280N
0028A					UK6 UK7 UK8 UK9 UJ6 UJ8	
0029	00002.000	EA		0972652-0001	NETWORK SN74LS283N	
0029A					UB6 UC6	
0031	00018.000	EA		0972787-0004	NETWORK SN74LS368N	
0031A					UR1 UR2 UP2 UR6 UR7 UH6 UP7	
0031B					UR8 UR9 UC2 UB4 UA7 UR4 UR5	
0031C					UE7 UP5 UB3 UB2	
0034	00001.000	EA		0974674-0001	NETWORK SN75138N	
0034A					UB7	
0035	00006.000	EA		0972583-0001	NETWORK,SN75365	TI- -SN75365
0035A					UL1 UL2 UM1 UM2 UN1 UN2	
0037	00066.000	EA		0996680-0001	IC, 16K RAM, (SEL)	001295-TMS4116/ZA0727
0037A					UN4 THRU UN25 UM4 THRU UM25	
0037B					UL4 THRU UL25	
0039	00002.000	EA		0996138-0001	IC,SN74LS266N 2-INPUT EXCLUSIVE-NOR GATE	TI -SN74LS266N
0039A					UD8 UB8	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-8

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5008 | REV ~~AB~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 4 of — PART NUMBER LM2261980-5008 — REV ~~AB~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0040	00001.000	EA		0972037-2680	NETWORK,RES 680 OHM 2% 16PIN 8ELEMENT	073138-898-3-R680
0040A					UD7	
0041	00001.000	EA		0972037-2220	NETWORK,RES 220 OHM 2% 16PIN 8ELEMENT	
0041A					UM9	
0042	00003.000	EA		0972037-1220	NETWORK,RES 22 OHM 2% 16PIN 8ELEMENT	073138-898-3-R22
0042A					UL3 UM3 UN3	
0043	00001.000	EA		0972946-0041	RES FIX 100 OHM 5 % .25 W CARBON FILM	ROH - R-25
0043A					R9	
0044	00007.000	EA		0972946-0049	RES FIX 220 OHM 5 % .25 W CARBON FILM	ROH - R-25
0044A					R1 R2 R29 R30 R31 R47 R48	
0045	00001.000	EA		0972946-0053	RES FIX 330 OHM 5 % .25 W CARBON FILM	ROH - R-25
0045A					R22	
0046	00002.000	EA		0972946-0061	RES FIX 680 OHM 5 % .25 W CARBON FILM	ROH - R-25
0046A					R21 R19	
0047	00007.000	EA		0972946-0065	RES FIX 1.0K OHM 5% .25 W CARBON FILM	ROH - R-25
0047A					R10 R20 R23 R24 R25 R37	
0047B					R38	
0048	00004.000	EA		0972946-0089	RES FIX 10K OHM 5% .25 W CARBON FILM	ROH - R-25
0048A					R33 R34 R35 R50	
0049	00001.000	EA		0972946-0115	RES FIX 120K OHM 5 % .25 W CARBON FILM	ROH - R-25

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-8

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5008 | REV ~~AB~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 5 of — PART NUMBER LM2261980-5008 REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0049A					R36	
0050	00001.000	EA		0972946-0105	RES FIX 47 K OHM 5 % .25 W CARBON FILM	ROH - R-25
0050A					R26	
0051	00001.000	EA		0972946-0121	RES FIX 220K OHM 5 % .25 W CARBON FILM	ROH - R-25
0051A					R39	
0052	00001.000	EA		0972946-0093	RES FIX 15K OHM 5% .25 W CARBON FILM	ROH - R-25
0052A					R27	
0053	00001.000	EA		0539370-0385	RES FIX FILM 1.00K OHM 1% .25 WATT	COR - MA55
0053A					R11	
0054	00001.000	EA		0539370-0357	RES FIX FILM 511 OHM 1% .25 WATT	COR - MA55
0054A					R12	
0055	00002.000	EA		0972753-0012	CAP,FIXED 220PF 25 WVDC 2.0%	UC -CSBD221G
0055A					C86 C96	
0056	00001.000	EA		0972757-0025	CAP FIX CER .01MF 10% 50V	
0056A					C95	
0058	00012.000	EA		0972763-0009	CAP,FIXED .0047MF 50 VOLTS	004222-MC105E472Z
0058A					C74 C75 C80 C81 C82 C83 C85	
0058B					C94 C97 C108 C109 C121	
0059	00087.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0059A					C1 THRU C19 C21 C23 C25 C27	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-8

APPD-MFG — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-5008 REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED — DATE 08/01/80 — LIST OF MATERIAL — PAGE 6 of — PART NUMBER LM2261980-5008 REV ~~AD~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0059B					C29 C31 C33 C35 C37 C39 C41	
0059C					C43 C45 C47 C49 C51 C53 C55	
0059D					C56 C57 C59 THRU C73 C76	
0059E					THRU C79 C84 C87 THRU C90	
0059F					C92 C93 C98 THRU C103 C106	
0059G					C107 C114 THRU C117 C120	
0059H					C122 THRU C125 C127 C128	
0059I					C129 C130 C131	
0060	00020.000	EA		0972924-0014	CAP FIX TANT SOLID 15 MFD 10 % 20 VOLT	QPL -M39003/1-2289
0060A					C20 C22 C24 C26 C28 C30 C32	
0060B					C34 C36 C38 C40 C42 C44 C46	
0060C					C48 C50 C52 C54 C91 C104	
0061	00001.000	EA		0222222-7470	NETWORK SN7470N	-SN7470N
0061A					UF3	
0062	00001.000	EA		0800118-0008	RESISTOR 1.0KOHMS DIL PULL UP 16 PINS	BEC -8981R1.0K
0062A					UC8	
0063	00003.000	EA		0972924-0006	CAP FIX TANT SOLID 39 MFD 10 % 10 VOLT	QPL -M39003/1-2259
0063A					C105 C118 C132	
0069	00001.000	EA		0972932-0001	DIODE 1N914B	SEE TI- DRAWING
0069A					CR14	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-8

APPD-MFG — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2261980-5008 REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED

DATE 08/01/80 — LIST OF MATERIAL — PAGE 7 of — PART NUMBER LM2261980-5008 — REV ~~AB~~ AE

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0081	00001.000	EA		0996508-0001	IC,74LS393N DUAL BINARY COUNTER	001295-74LS393N
0081A					UP1	
0082	00001.000	EA		0222222-7408	NETWORK-SN7408N	
0082A					UG1	
0085	00011.000	EA		0972946-0081	RES FIX 4.7K OHM 5 % .25 W CARBON FILM	ROH - R-25
0085A					R13 THRU R18 R40 R41 R42	
0085B					R43 R44	
0086	00006.000	EA		0972946-0025	RES FIX 22.0 OHM 5 % .25 W.CARBON FILM	ROH - R-25
0086A					R3 R4 R5 R6 R7 R8	
0090	00001.000	EA		0972757-0021	CAP, FIX, CERAMIC, 4700PF, 50V 10%	
0090A					C126	
0094	00001.000	EA		0996780-0001	IC,SN74LS33N QUAD POSITIVE-NOR BUFFER	001295-SN74LS33N
0094A					UA6	
0097	00002.000	EA		0219402-7258	NETWORK SN74S258N	
0097A					UE1 UE2	
0102	00001.000	EA		0972946-0088	RES FIX 9.1K OHM 5 % .25 W CARBON FILM	ROH - R-25
0102A					R28	
0103	00001.000	EA		0996424-0001	IC,SN74LS375N 4 BIT BISTABLE LATCHES	001295-SN74LS375N
0103A					UA8	
0104	00002.000	EA		0231784-6002	DIODE- 4 PELLET, SILICON,MULTI	GE -HPD400

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-8

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5008 | REV ~~AD~~ AE

TEXAS INSTRUMENTS INCORPORATED

DATE 08/01/80 — LIST OF MATERIAL — PAGE 8 of — PART NUMBER LM2261980-5008 — REV ~~AE~~ AF

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
~~0104A~~					CR16 CR17	
0105	00001.000	EA		0972946-0075	RES FIX 2.7K OHM 5 % .25 W CARBON FILM	ROH - R-25
0105A					R32	
0106	00001.000	EA		0972784-0002	NETWORK SN74LS14N	
0106A					UF2	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 2261980-8

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2261980-5008 | REV ~~AE~~ AF

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DEVISE TYPES ARE PREFIXED WITH SN 74
2. GROUND IS APPLIED TO PIN 7 OF ALL 14-PIN IC'S AND PIN 8 OF ALL 16-PIN IC'S
3. VCC IS APPLIED TO PIN 14 OF ALL 14-PIN IC'S AND PIN 16 OF ALL 16-PIN IC'S
4. DEVICE TYPE, PIN NUMBERS, AND LOCATION OF IC IS SHOWN AS FOLLOWS:

00 AND 04 = DEVICE TYPE

4, 5, AND 6 = PIN NUMBERS

U17 AND U34 = REFERENCE DESIGNATOR

5. WHEN REQUIRED R45 AND R46 WILL BE SELECTED AT UNIT TEST.
6. UNLESS NOTED THIS SCHEMATIC APPLIES TO ALL DASH NUMBERED ASSEMBLIES. DASH 1 THRU DASH 4 ASSEMBLIES USE 2261981 PWBS. DASH 5 THRU DASH 8 ASSEMBLIES USE 2262031 PWBS.

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	CN451140(B) RCHAPA	8-31-78	
	B	CN447073(C) E. Cook	12-5-78	
	C	CN437778(C) E. Molina	3-26-79	
	D	CN449780(C) M. Wells	7-30-79	
	E	CN433600(C) B. Antonsen	11-26-79	
	F	CN453422(D) E. Linhart (I) ADDED SHEETS 2A, 3A, 4A, 12A AND 13A.	5-9-80	

REV STATUS OF SHEETS	REV	F	F	F	F	F
	SHEET	2A	3A	4A	12A	13A

REV STATUS OF SHEETS	REV	F	F	F	F	B	F	B	B	F	*	*	F	F	*
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PARTS LIST

-2 QTY REQD	-1 QTY REQD	ITEM NO	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION

UNLESS OTHERWISE SPECIFIED
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIR
- DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING
- IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY
- INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100

HOLE TOLERANCE

.013 THRU .138	+.004 -.001	.138 THRU .250	+.005 -.001	.250 THRU .500	+.006 -.001
.500 THRU .750	+.008 -.001	.750 THRU 1.000	+.010 -.001	1.001 THRU 2.000	+.012 -.001

2261980	7047
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES ANGLES ±1° 3 PLACE DECIMALS ±.010 2 PLACE DECIMALS ±.02

MATERIAL:

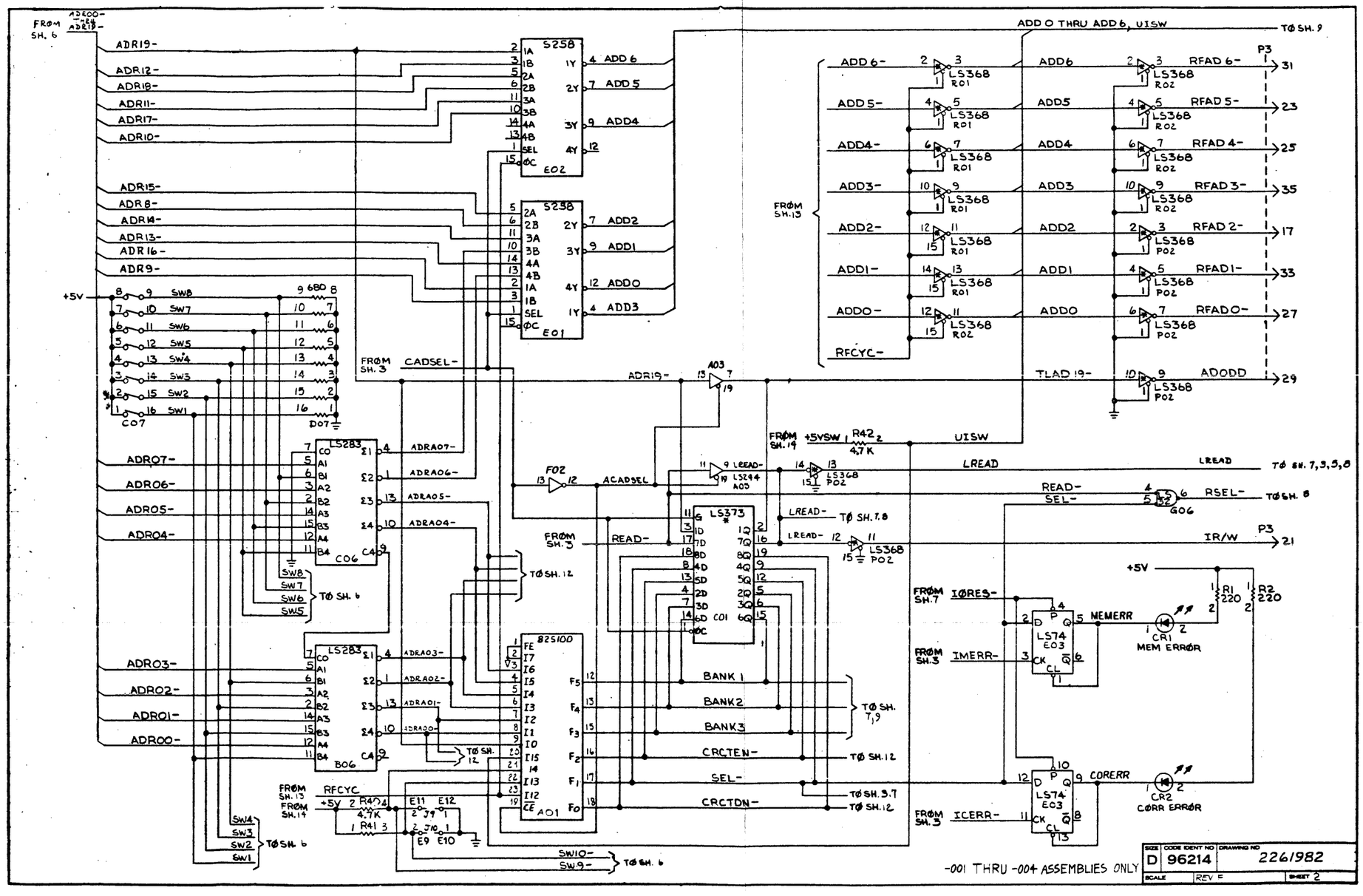
		DATE
DWN	Y. Lin	5-10-78
CHK	C. Keezer	6-8-78
ENGR	L. Myint	6-7-78
QA	[illegible]	6/7/78
APVD	[illegible]	6/15/78
CONTR NO		
DESIGN ACTIVITY APPROVAL	[illegible]	6/16/78

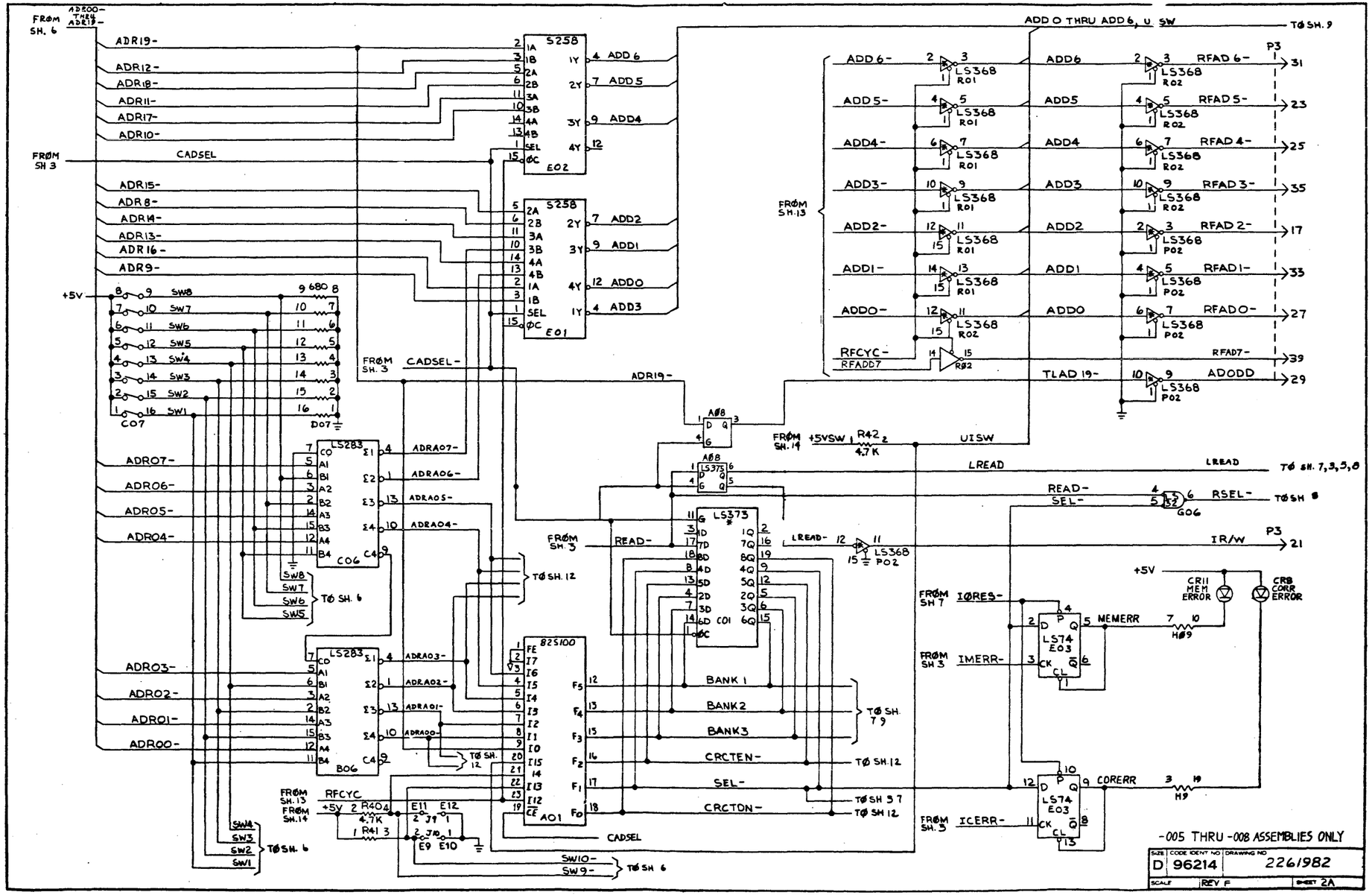
TEXAS INSTRUMENTS INCORPORATED Equipment Group Dallas, Texas

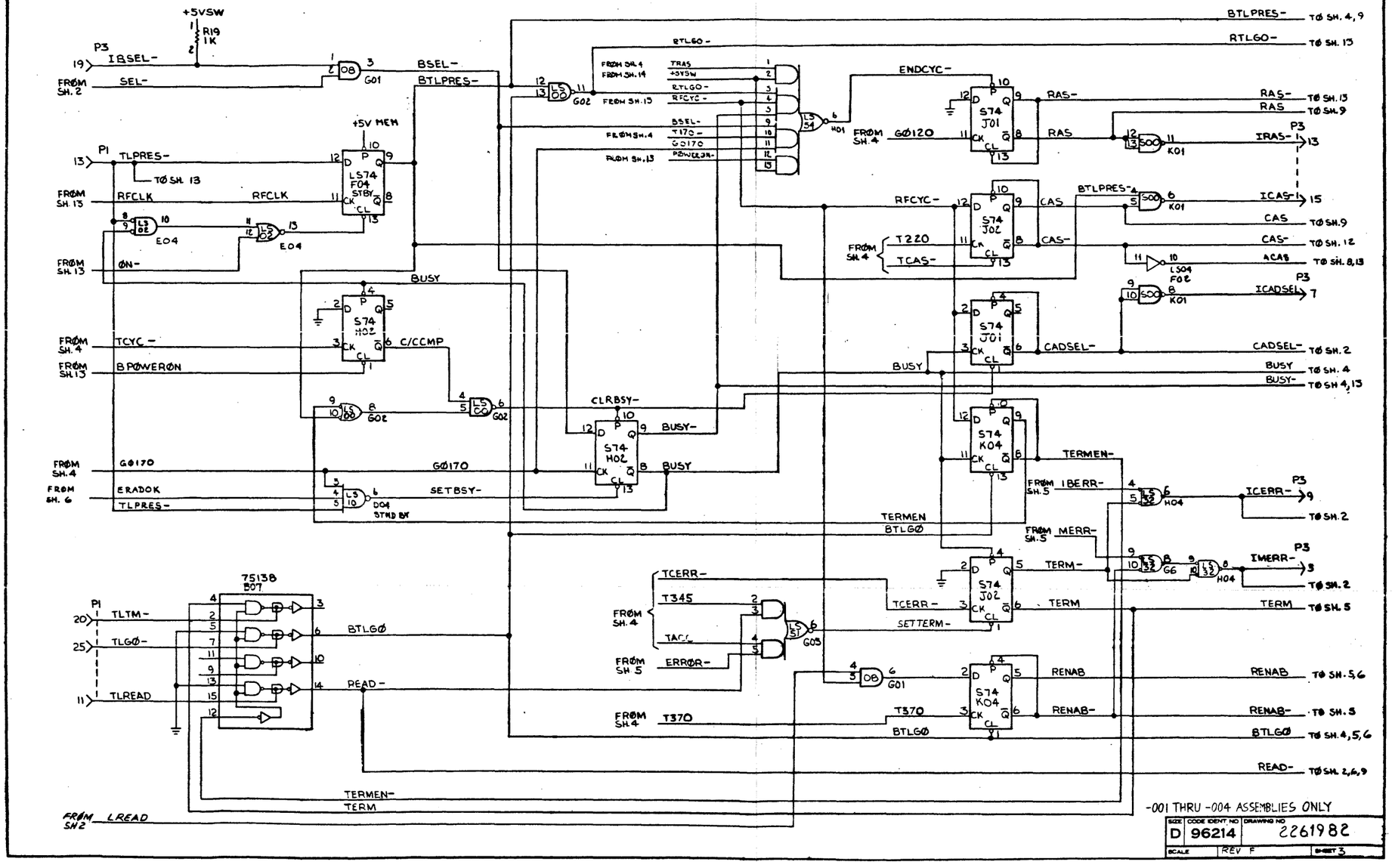
LOGIC DIAGRAM, MEMORY CONTROLLER, 990/16KR

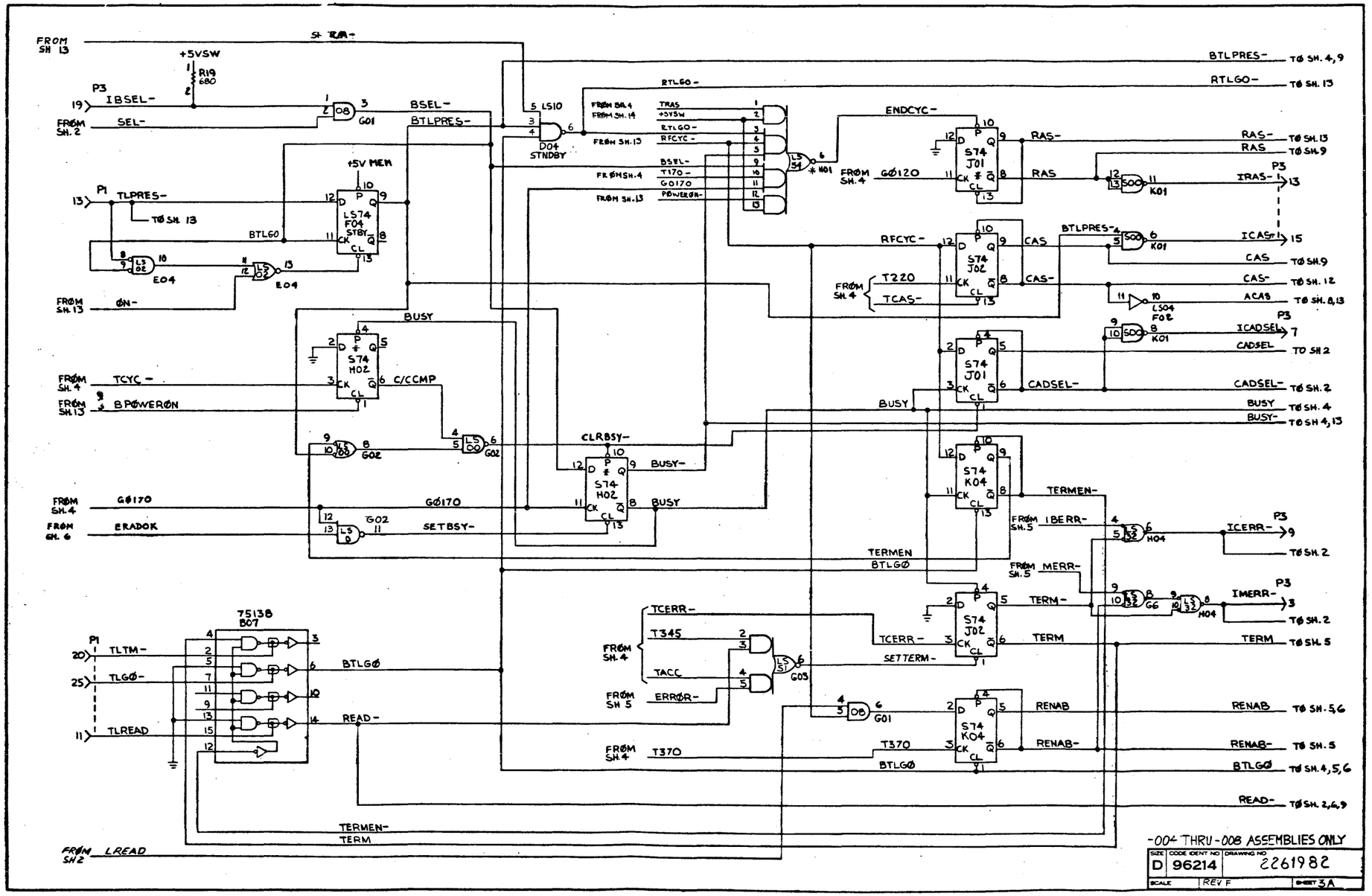
SIZE	CODE IDENT NO	DRAWING NO
D	96214	2261982

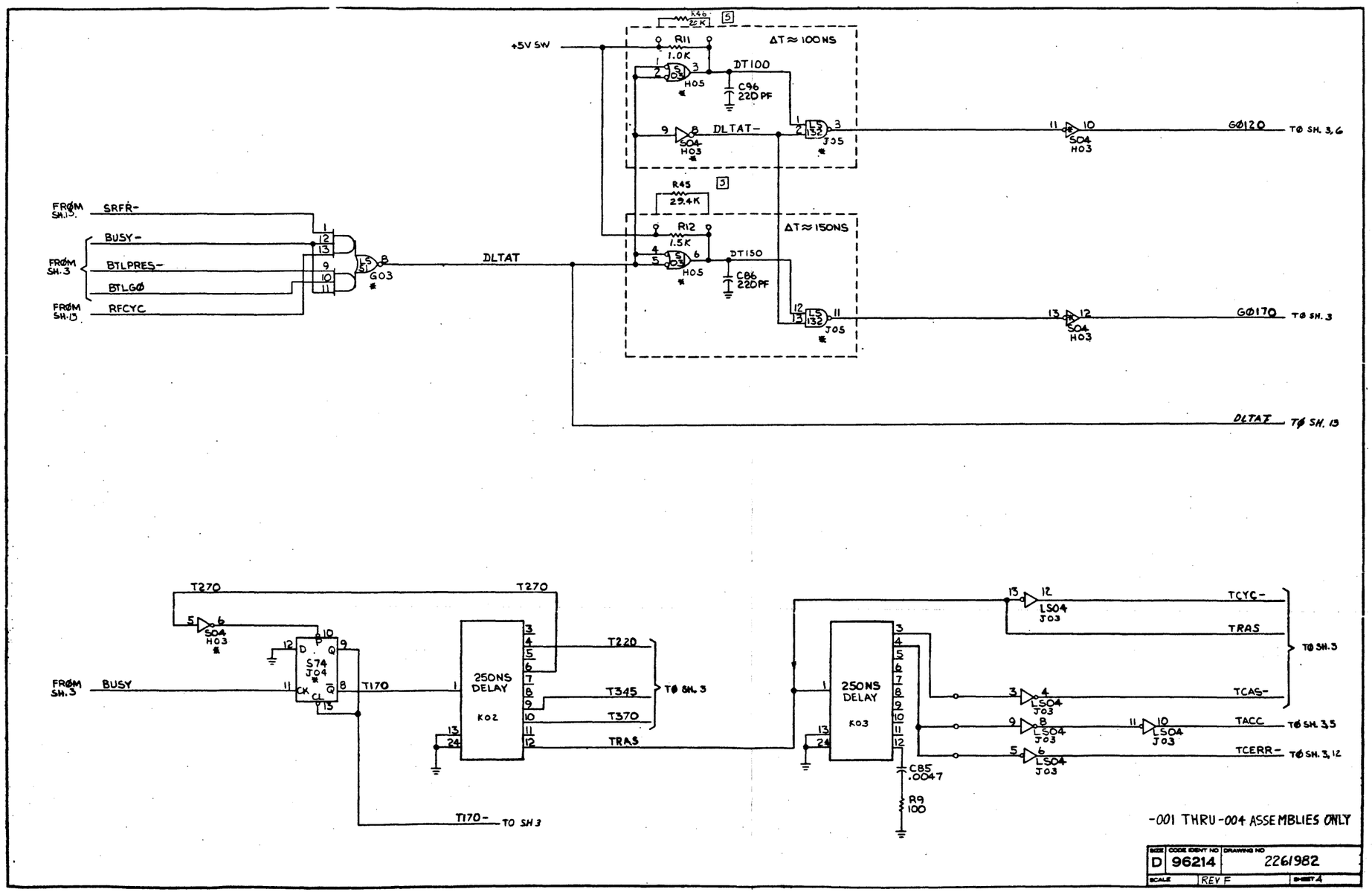
SCALE NONE | SHEET 1 OF 14

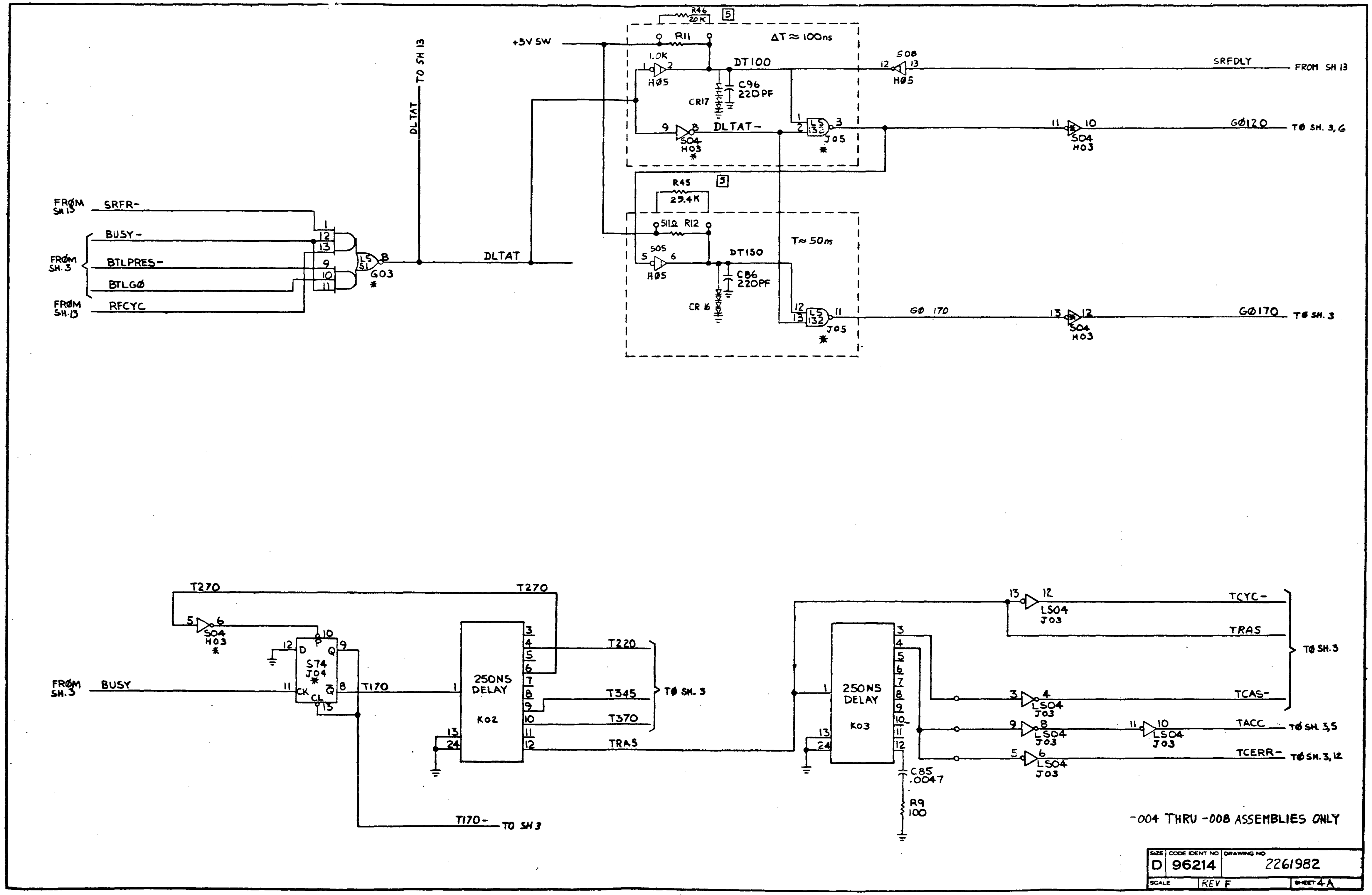

FROM SH. 6
ADR00- thru ADR19-
ADR19-
ADR12-
ADR18-
ADR11-
ADR17-
ADR10-
ADR15-
ADR8-
ADR14-
ADR13-
ADR16-
ADR9-
+5V
SW8
SW7
SW6
SW5
SW4
SW3
SW2
SW1
C07
D07
680
LS283
C06
B06
ADRA07-
ADRA06-
ADRA05-
ADRA04-
ADRA03-
ADRA02-
ADRA01-
ADRA00-
ADR07-
ADR06-
ADR05-
ADR04-
ADR03-
ADR02-
ADR01-
ADR00-
TØ SH. 6
TØ SH. 12
S258
E02
E01
ADD 6
ADD 5
ADD4
ADD2
ADD1
ADD0
ADD3
FROM SH. 3
CADSEL-
ADR19-
825100
A01
BANK 1
BANK2
BANK3
CRCTEN-
SEL-
CRCTDN-
TØ SH. 7,9
TØ SH. 3,7
FROM SH. 13
RFCYC
FROM SH. 14
+5V
R40 4.7K
R41 3
R42 4.7K
E11
E12
E9
E10
SW10-
SW9-
F02
ACADSEL
FROM SH. 3
READ-
LS373
LS244 A03
LS368 P02
LS368 R01
LS368 R02
LS368 P01
LREAD-
LREAD
TØ SH. 7,8
TØ SH. 7,3,5,8
FROM SH. 19
+5VSW
UISW
ADD 0 THRU ADD 6, UISW
TØ SH. 9
FROM SH. 13
ADD6-
ADD5-
ADD4-
ADD3-
ADD2-
ADD1-
ADDO-
RFCYC-
RFAD 6-
RFAD 5-
RFAD 4-
RFAD 3-
RFAD 2-
RFAD1-
RFADO-
TLAD 19-
ADODD
P3
31
23
25
35
17
33
27
29
READ-
SEL-
LS32 G06
RSEL-
TØ SH. 8
IR/W
21
FROM SH. 7
IØRES-
FROM SH. 3
IMERR-
LS74 E03
MEMERR
CR1
MEM ERROR
R1 220
R2 220
ICERR-
CORERR
CR2
CØRR ERRØR
-001 THRU -004 ASSEMBLIES ONLY
SIZE D
CODE IDENT NO 96214
DRAWING NO 2261982
SCALE
REV F
SHEET 2


FROM SH. 6
ADR00- THRU ADR19-
ADR19-
ADR12-
ADR18-
ADR11-
ADR17-
ADR10-
FROM SH 3
CADSEL
ADR15-
ADR8-
ADR14-
ADR13-
ADR16-
ADR9-
+5V
SW8
SW7
SW6
SW5
SW4
SW3
SW2
SW1
C07
D07
9 680 8
ADR07-
ADR06-
ADR05-
ADR04-
ADR03-
ADR02-
ADR01-
ADR00-
LS283
C06
B06
ADRA07-
ADRA06-
ADRA05-
ADRA04-
ADRA03-
ADRA02-
ADRA01-
ADRA00-
TØ SH. 6
TØ SH. 12
S258
E02
E01
ADD6
ADD5
ADD4
ADD3
ADD2
ADD1
ADD0
FROM SH. 3
CADSEL-
ADR19-
825100
A01
BANK 1
BANK2
BANK3
CRCTEN-
SEL-
CRCTON-
TØ SH 7 9
TØ SH. 12
TØ SH 5 7
FROM SH. 13
FROM SH. 14
RFCYC
+5V
R404
4.7K
R41
E11
E12
E9
E10
J9
J10
SW10-
SW9-
A08
FROM SH. 19
+5VSW
R42
4.7K
UISW
LS375
LREAD
TØ SH. 7,3,5,8
READ-
SEL-
G06
RSEL-
TØ SH 8
FROM SH. 3
READ-
LS373
C01
LREAD-
LS368
P02
IR/W
P3
21
ADD 0 THRU ADD 6, U SW
TØ SH. 9
FROM SH. 13
ADD6-
ADD5-
ADD4-
ADD3-
ADD2-
ADD1-
ADD0-
RFCYC-
RFADD7
LS368
R01
R02
R03
RFAD 6-
RFAD 5-
RFAD 4-
RFAD 3-
RFAD 2-
RFAD1-
RFAD0-
RFAD7-
TLAD 19-
ADODD
P3
31
23
25
35
17
33
27
39
29
+5V
CR11 MEM ERROR
CR8 CORR ERROR
FROM SH 7
IØRES-
FROM SH 3
IMERR-
LS74 E03
MEMERR
H09
COREERR
H9
FROM SH. 5
ICERR-
-005 THRU -008 ASSEMBLIES ONLY
SIZE D
CODE IDENT NO 96214
DRAWING NO 2261982
SCALE
REV F
SHEET 2A

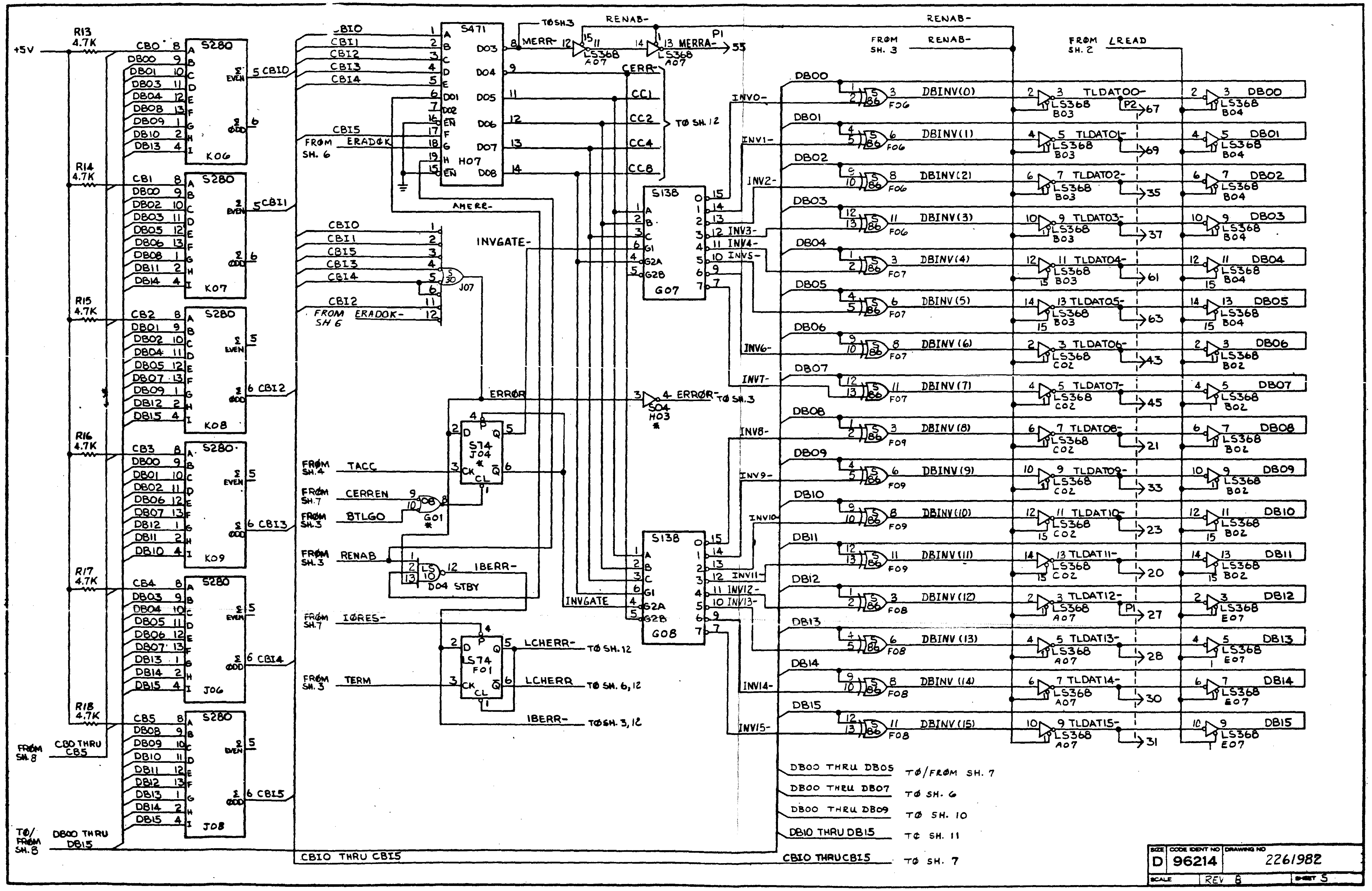

+5VSW
R19 1K
P3
IBSEL-
FROM SH. 2
SEL-
G01
BSEL-
BTLPRES-
P1
TLPRES-
TO SH. 13
FROM SH. 13
RFCLK
RFCLK
+5V MEM
LS74 F04 STBY
E04
E04
ØN-
BUSY
FROM SH. 4
TCYC-
FROM SH. 13
BPØWERØN
S74 H02
C/CCMP
G02
CLRBSY-
S74 H02
BUSY-
BUSY
FROM SH. 4
GØ170
FROM SH. 6
ERADOK
TLPRES-
SETBSY-
D04 STRD BY
RTLGO-
FROM SH. 4
TRAS
+5VSW
FROM SH. 14
RTLGO-
FROM SH. 13
RFCYC-
BSEL-
FROM SH. 4
T170-
GØ170
FROM SH. 13
PØWERØN-
LS51 H01
ENDCYC-
FROM SH. 4
GØ120
S74 J01
RAS-
RAS
TO SH. 13
TO SH. 9
P3
IRAS-
13
K01
RFCYC-
S74 J02
CAS
BTLPRES-
ICAS-
15
CAS
TO SH. 9
FROM SH. 4
T220
TCAS-
CAS-
TO SH. 12
ACAS
TO SH. 8, 13
LS04 F02
P3
ICADSEL
7
K01
S74 J01
CADSEL-
TO SH. 2
BUSY
TO SH. 4
BUSY-
TO SH 4, 13
S74 K04
TERMEN-
FROM SH. 5
IBERR-
P3
ICERR-
9
TO SH. 2
H04
TERMEN
BTLGØ
FROM SH. 5
MERR-
S74 J02
TERM-
IMERR-
P3
3
TO SH. 2
TERM
TO SH. 5
H04
75138 B07
P1
TLTM-
TLGØ-
TLREAD
BTLGØ
READ-
TCERR-
FROM SH. 4
T345
TACC
FROM SH. 5
ERRØR-
G03
SETTERM-
TCERR-
TERM
FROM SH. 4
T370
T370
BTLGØ
S74 K04
RENAB
RENAB
TO SH. 5, 6
RENAB-
RENAB-
TO SH. 5
BTLGØ
TO SH. 4, 5, 6
READ-
TO SH. 2, 6, 9
TERMEN-
TERM
FROM LREAD SH 2
-001 THRU -004 ASSEMBLIES ONLY
SIZE D
CODE IDENT NO 96214
DRAWING NO 2261982
SCALE
REV F
SHEET 3

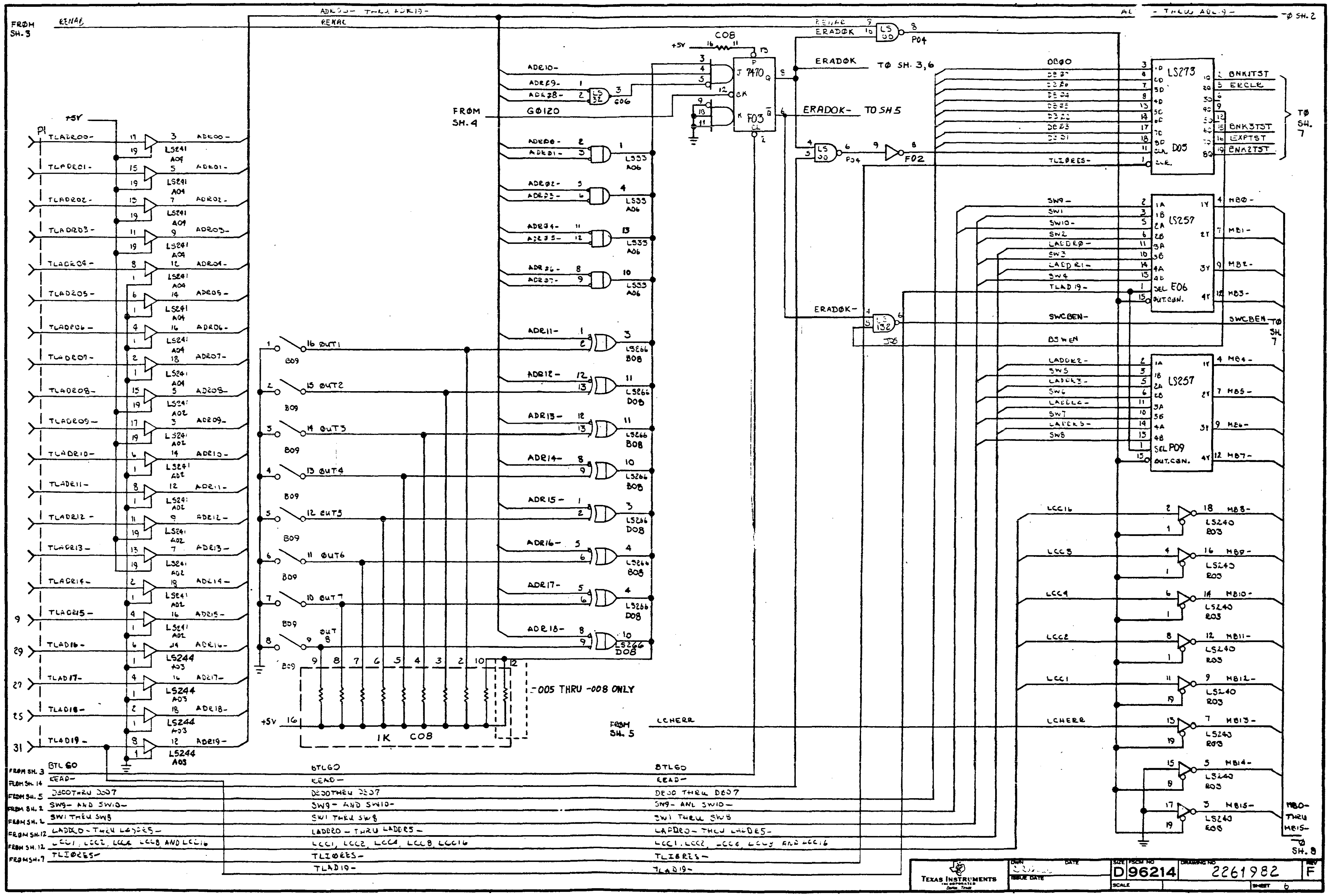

FROM SH 13
SH RA-
+5VSW
R19 680
P3
IBSEL-
FROM SH. 2
SEL-
G01
BSEL-
BTLPRES-
5 LS10
D04 STNDBY
RTLGO-
FROM SH.4
FROM SH.14
TRAS
+5VSW
RTLGO-
RFCYC-
FROM SH.13
BSEL-
T170-
FROM SH.4
G0170
FROM SH.13
POWERON-
LS 34
H01
ENDCYC-
FROM SH.4
G0120
S74 J01
RAS-
RAS
K01
P3
IRAS-
13
BTLPRES-
TO SH. 4,9
RTLGO-
TO SH. 13
RAS-
TO SH.13
RAS
TO SH.9
+5V MEM
P1
TLPRES-
TO SH. 13
LS74 F04 STBY
BTLGO
E04
E04
FROM SH.13
ØN-
RFCYC-
S74 J02
CAS
BTLPRES-
K01
ICAS-
15
CAS
TO SH.9
FROM SH.4
T220
TCAS-
CAS-
TO SH. 12
ACAS
TO SH. 8,13
LS04 F02
P3
ICADSEL
7
CADSEL
TO SH 2
BUSY
FROM SH.4
TCYC-
FROM SH.13
B POWERON
S74 H02
C/CCMP
S74 J01
CADSEL-
CADSEL-
TO SH. 2
BUSY
TO SH. 4
BUSY-
TO SH 4,13
CLRBSY-
S74 H02
BUSY-
BUSY
G02
G02
S74 K04
TERMEN-
FROM SH.4
G0170
FROM SH. 6
ERADOK
G02
SETBSY-
FROM SH.5
IBERR-
LS 32
H04
ICERR-
9
TO SH. 2
TERMEN
BTLGØ
FROM SH.5
MERR-
P3
IMERR-
3
TO SH. 2
TERM
TO SH. 5
S74 J02
TERM-
TERM
SETTERM-
75138 B07
P1
TLTM-
TLGØ-
TLREAD
BTLGØ
READ-
TCERR-
T345
TACC
FROM SH.4
FROM SH 5
ERRØR-
LS 51
G03
TCERR-
FROM SH.4
T370
T370
BTLGØ
S74 K04
RENAB
RENAB
TO SH. 5,6
RENAB-
TO SH. 5
BTLGØ
TO SH. 4,5,6
READ-
TO SH. 2,6,9
TERMEN-
TERM
FROM SH 2
LREAD
-004 THRU -008 ASSEMBLIES ONLY
SIZE D
CODE IDENT NO 96214
DRAWING NO 2261982
SCALE
REV F
SHEET 3A

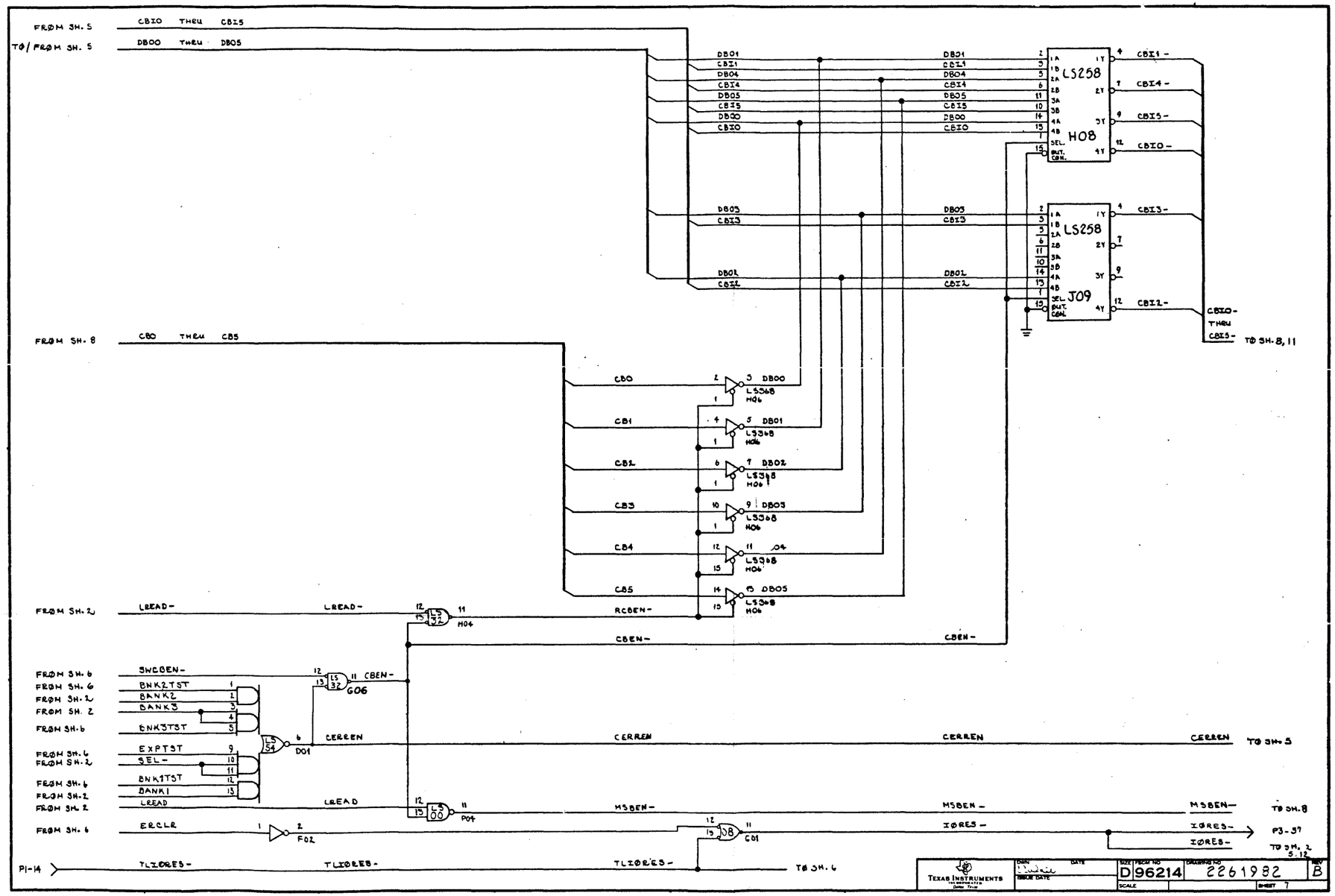

+5V SW
R11
1.0K
ΔT≈100NS
DT100
C96
22DPF
DLTAT-
G0120
TØ SH. 3,6
R45
29.4K
R12
1.5K
ΔT≈150NS
DT150
CB6
22DPF
G0170
TØ SH. 3
DLTAT
TØ SH. 13
FRØM SH.15
SRFR-
BUSY-
FRØM SH.3
BTLPRES-
BTLGØ
FRØM SH.13
RFCYC
G03
DLTAT
T270
T270
FROM SH.3
BUSY
S74 J04
T170
250NS DELAY
K02
T220
T345
T370
TRAS
TØ SH. 3
T170- TO SH 3
250NS DELAY
K03
TCYC-
TRAS
TCAS-
TØ SH.3
TACC
TØ SH. 3,5
TCERR-
TØ SH. 3, 12
C85 .0047
R9 100
-001 THRU -004 ASSEMBLIES ONLY
D
96214
2261982
REV F
SHEET 4

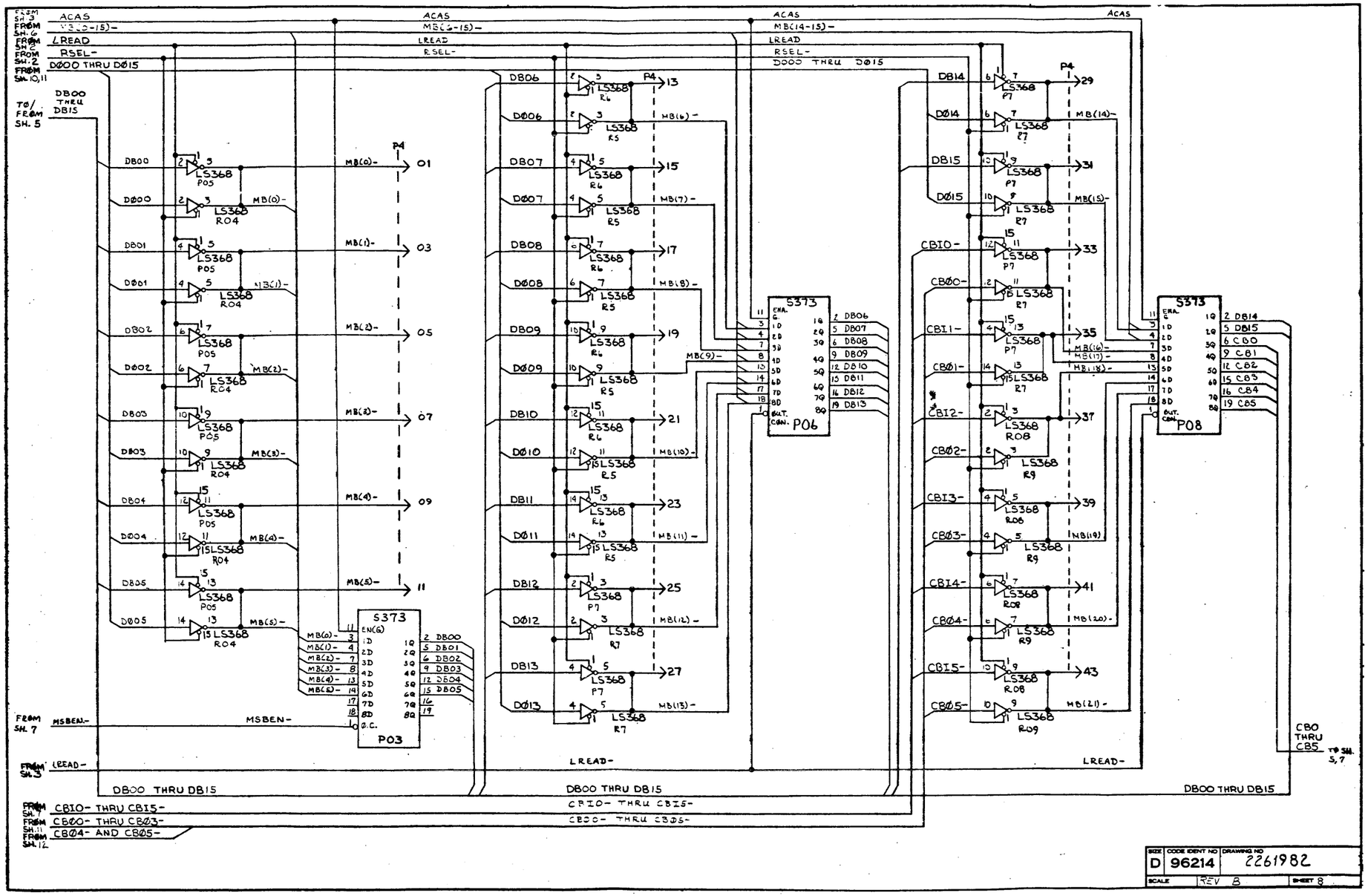


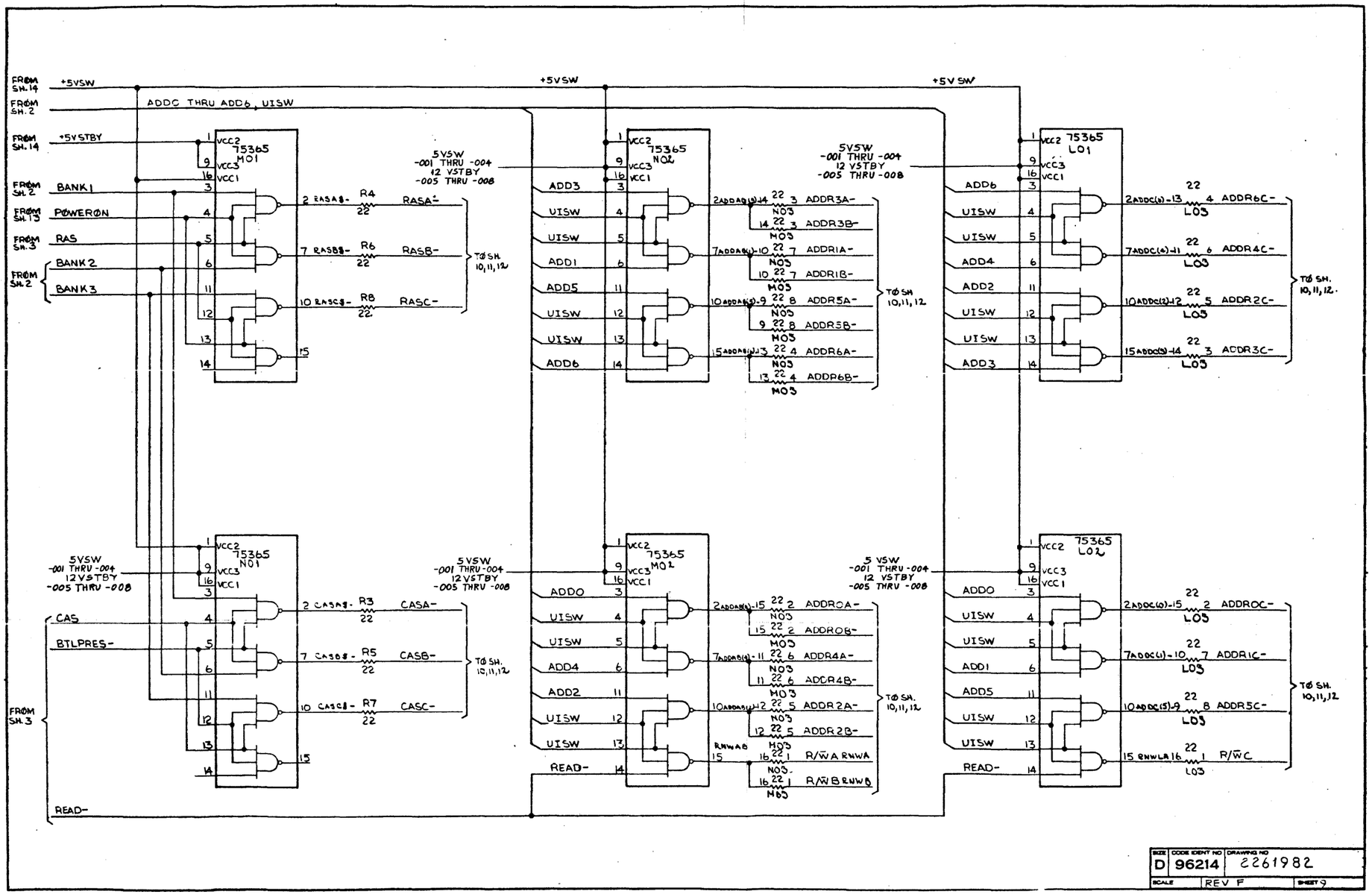
FROM SH 13 SRFR-
BUSY-
FROM SH.3 BTLPRES-
BTLGØ
FROM SH.13 RFCYC
G03
DLTAT TO SH 13
DLTAT
+5V SW
R46 20K
R11 1.0K
ΔT ≈ 100ns
DT100
C96 220 PF
CR17
DLTAT-
S04 H03
J05
S08 H05
SRFDLY FROM SH 13
GØ120 TO SH. 3, 6
R45 29.4K
511Ω R12
S05 H05
DT150
C86 220PF
CR16
T≈ 50ns
GØ 170
GØ170 TO SH. 3
T270
S04 H03
S74 J04
FROM SH.3 BUSY
T170
250NS DELAY K02
T220
T345 TO SH. 3
T370
TRAS
T170- TO SH 3
250NS DELAY K03
C85 .0047
R9 100
LS04 J03
TCYC-
TRAS
TO SH.3
TCAS-
TACC TO SH 3,5
TCERR- TO SH. 3,12
-004 THRU -008 ASSEMBLIES ONLY
D 96214 2261982
REV F
SHEET 4A

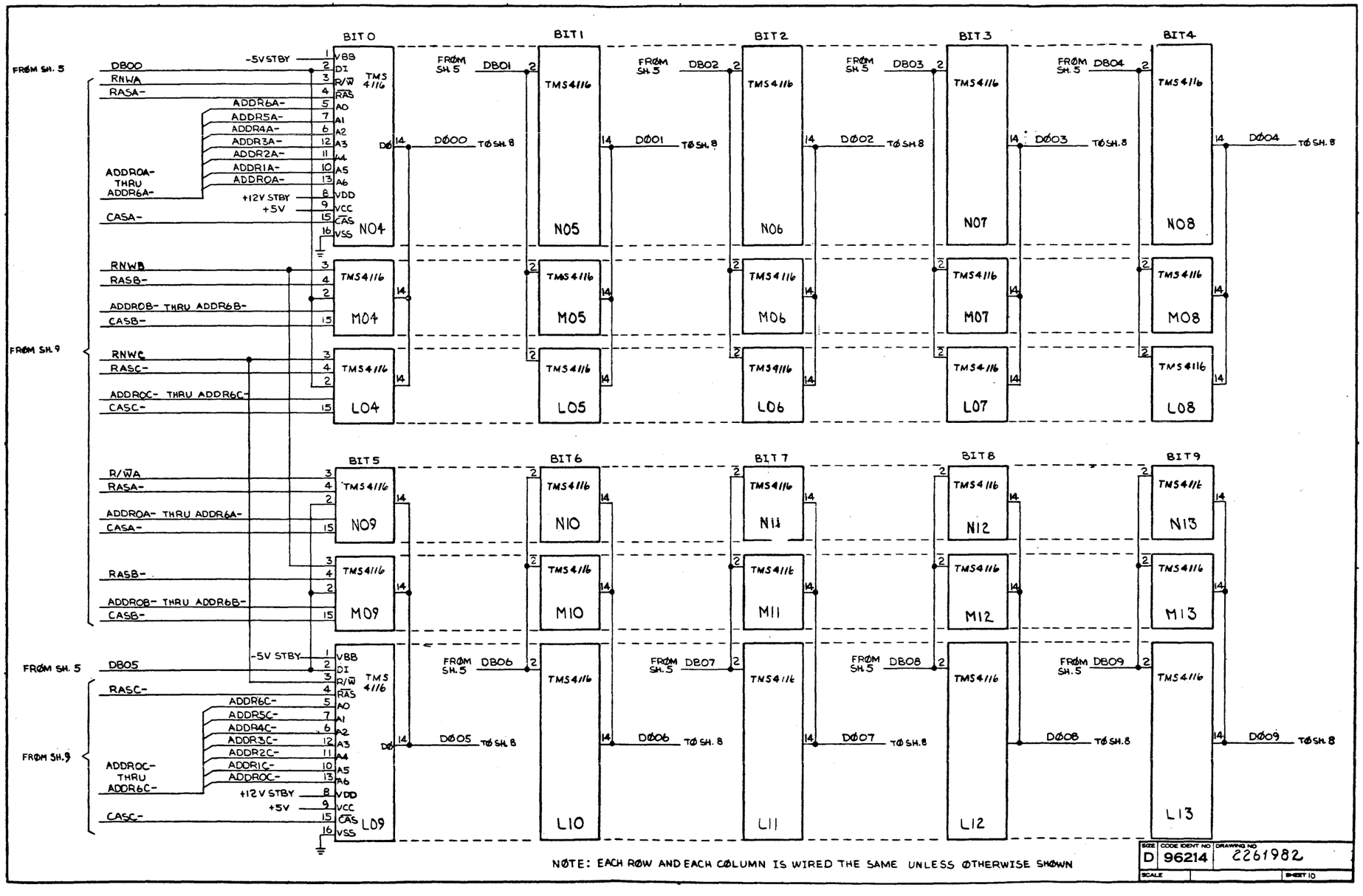

S280
K06
K07
K08
K09
J06
J08
S471
H07
S138
G07
G08
S74
J04
LS74
F01
LS368
A07
MERR-
MERRA-
RENAB-
ERROR
ERROR- TO SH.3
IBERR- TO SH. 3, 12
LCHERR- TO SH. 12
LCHERR TO SH. 6, 12
INVGATE-
CERR-
CC1
CC2
CC4
CC8
TO SH. 12
DB00 THRU DB05 TO/FROM SH. 7
DB00 THRU DB07 TO SH. 6
DB00 THRU DB09 TO SH. 10
DB10 THRU DB15 TO SH. 11
CB10 THRU CB15 TO SH. 7
FROM SH. 8 CB0 THRU CB5
TO/FROM SH. 8 DB00 THRU DB15
FROM LREAD SH. 2
FROM RENAB- SH. 3
D
96214
2261982
REV B
SHEET 5

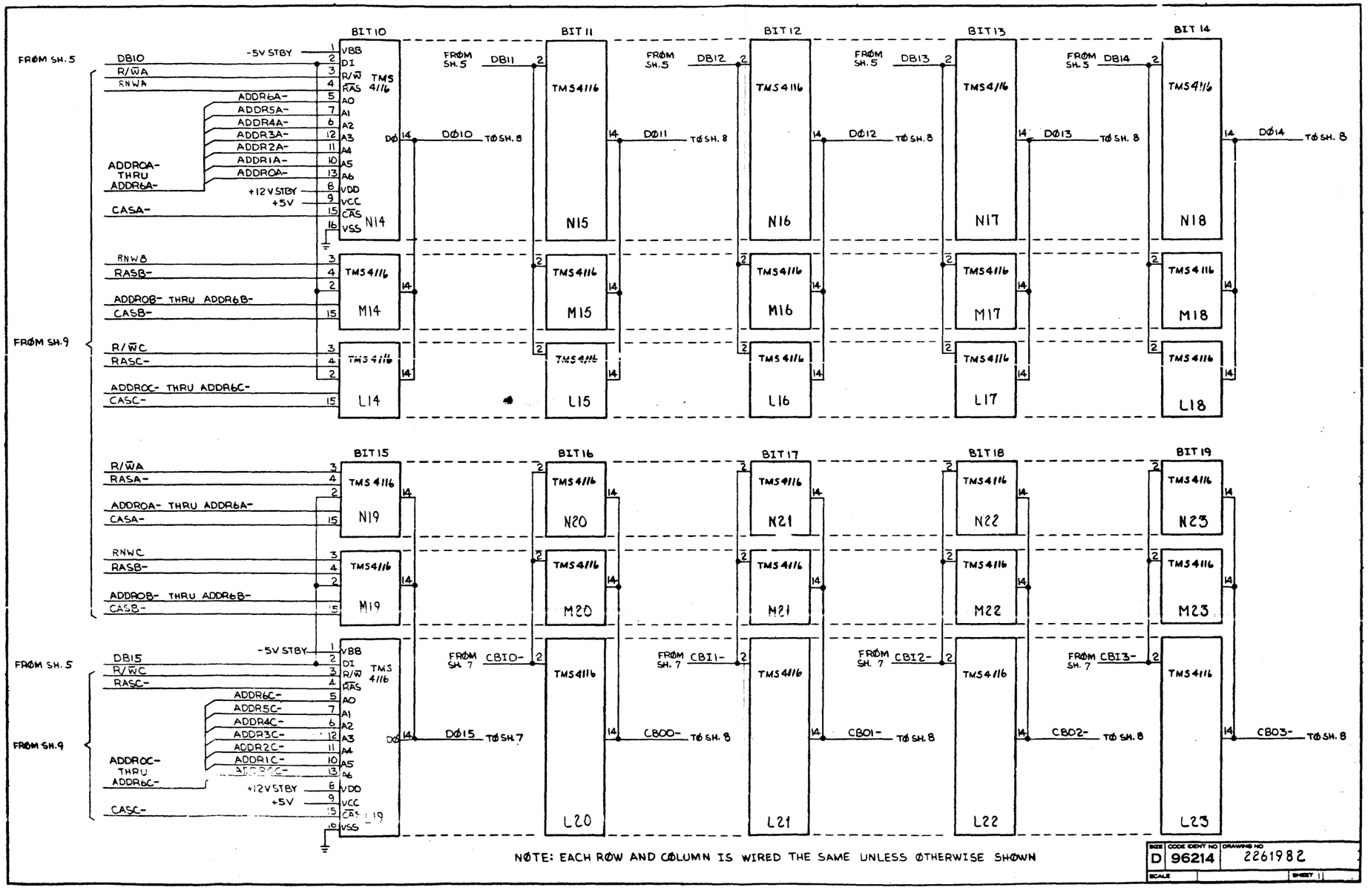

FROM SH. 3
TO SH. 2
ERADOK TO SH. 3, 6
ERADOK- TO SH 5
FROM SH. 4
LS273 D05
LS257 E06
LS257 P09
TO SH. 7
-005 THRU -008 ONLY
1K C08
FROM SH. 5
TO SH. 8
TEXAS INSTRUMENTS
D96214
2261982
F

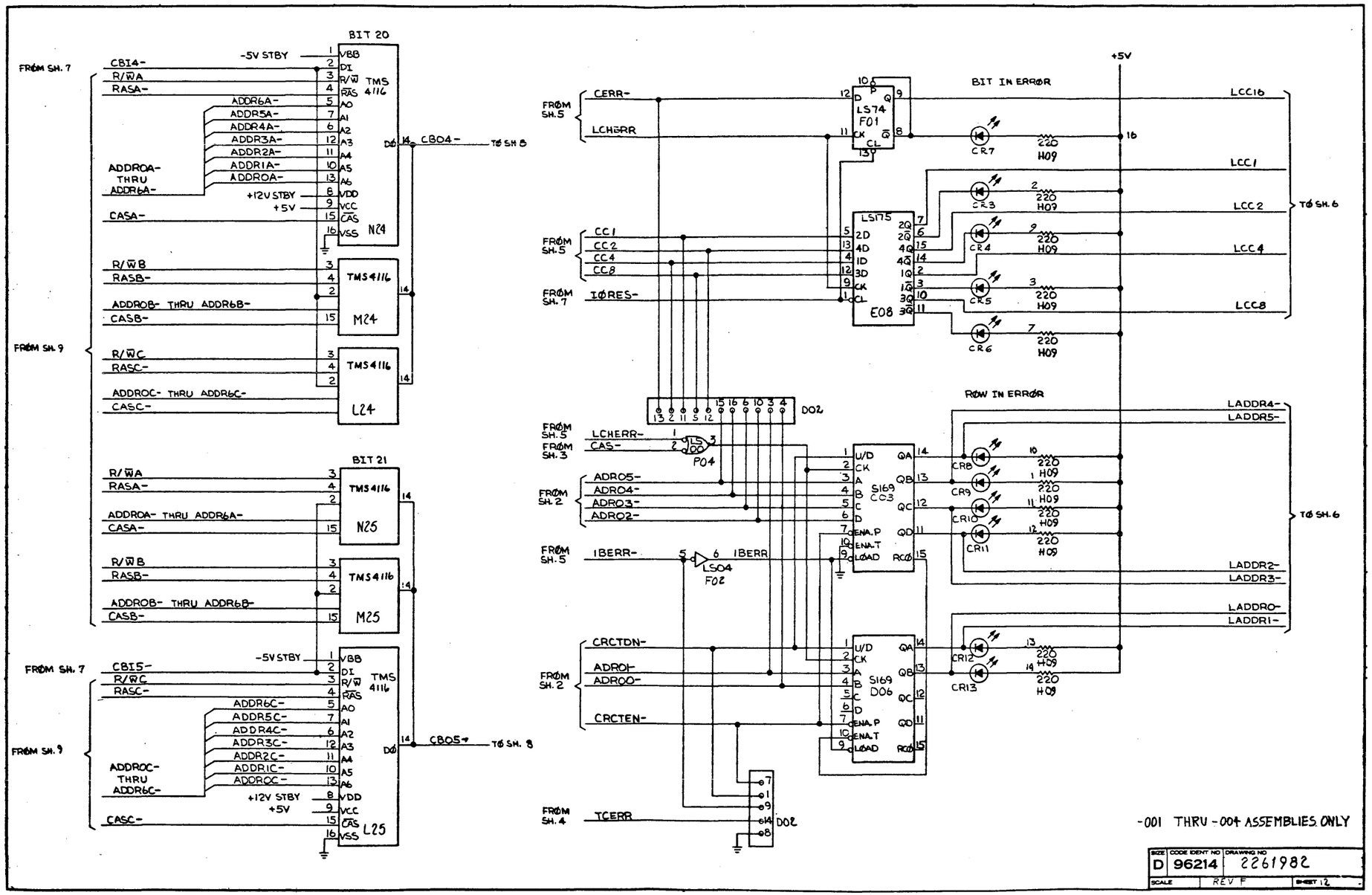

FROM SH. 5
CBI0 THRU CBI5
TO/FROM SH. 5
DB00 THRU DB05
DB01
CBI1
DB04
CBI4
DB05
CBI5
DB00
CBI0
DB03
CBI3
DB02
CBI2
LS258
H08
J09
CBI1-
CBI4-
CBI5-
CBI0-
CBI3-
CBI2-
CBI0-
THRU
CBI5-
TO SH. 8, 11
FROM SH. 8
CB0 THRU CB5
CB0
CB1
CB2
CB3
CB4
CB5
LS368
H06
DB00
DB01
DB02
DB03
DB04
DB05
FROM SH. 2
LREAD-
LS32
H04
RCBEN-
CBEN-
FROM SH. 6
SWCBEN-
FROM SH. 6
BNK2TST
FROM SH. 2
BANK2
FROM SH. 2
BANK3
FROM SH. 6
BNK3TST
FROM SH. 6
EXPTST
FROM SH. 2
SEL-
FROM SH. 6
BNK1TST
FROM SH. 2
BANK1
FROM SH. 2
LREAD
LS54
D01
CERREN
LS00
P04
MSBEN-
FROM SH. 6
ERCLR
F02
C01
IORES-
TO SH. 8
P3-37
TO SH. 2
5,12
P1-14
TLIORES-
TO SH. 6
TEXAS INSTRUMENTS
D96214
2261982
B

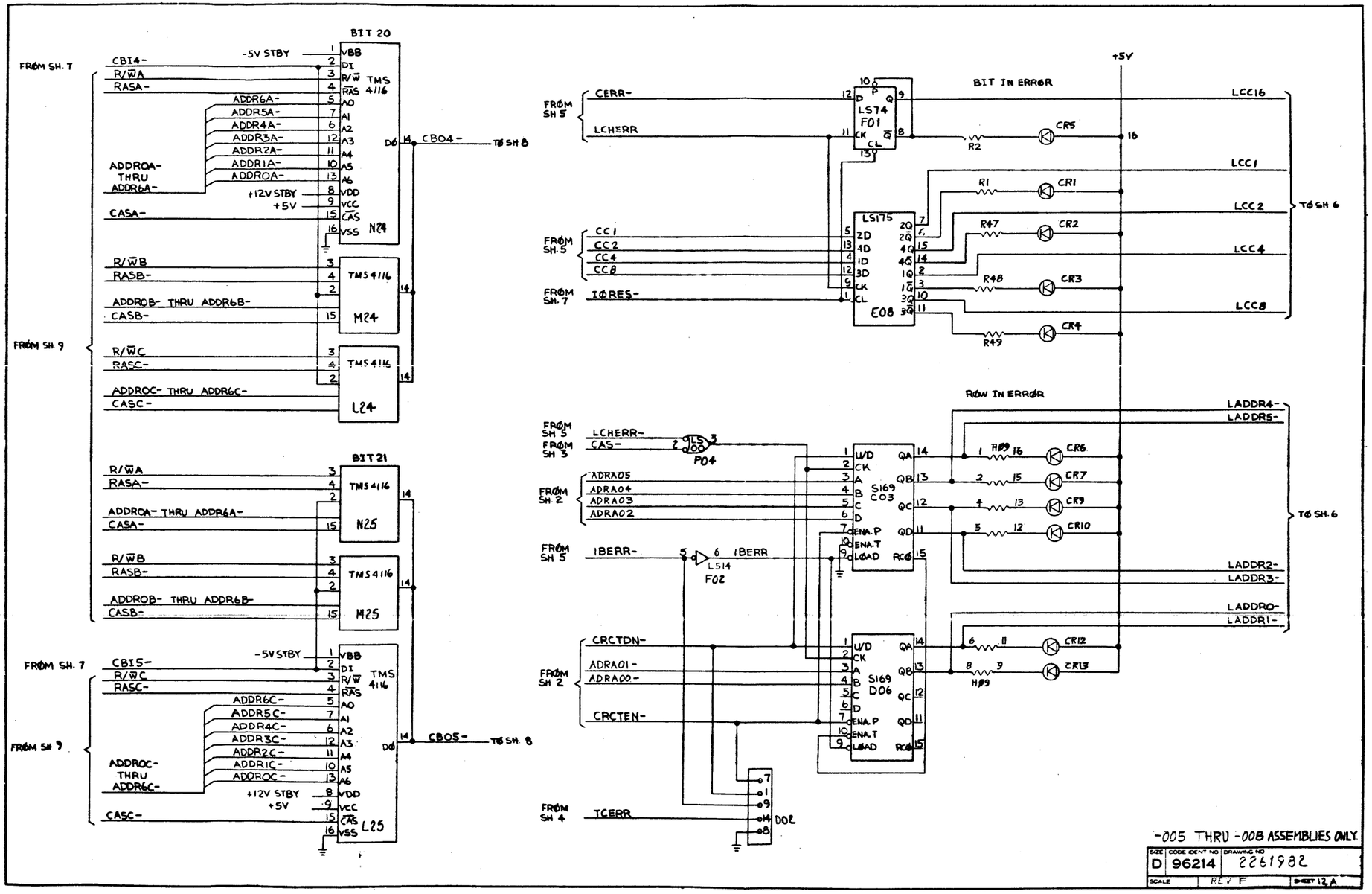

ACAS
MB(0-15)-
LREAD
RSEL-
D000 THRU D015
DB00 THRU DB15
TO/FROM SH. 5
LS368
S373
P03
P04
P05
P06
P07
P08
R04
R05
R06
R07
R08
R09
MSBEN-
LREAD-
CBIO- THRU CBI5-
CB00- THRU CB03-
CB04- AND CB05-
CBO THRU CB5
D B 96214 2261982

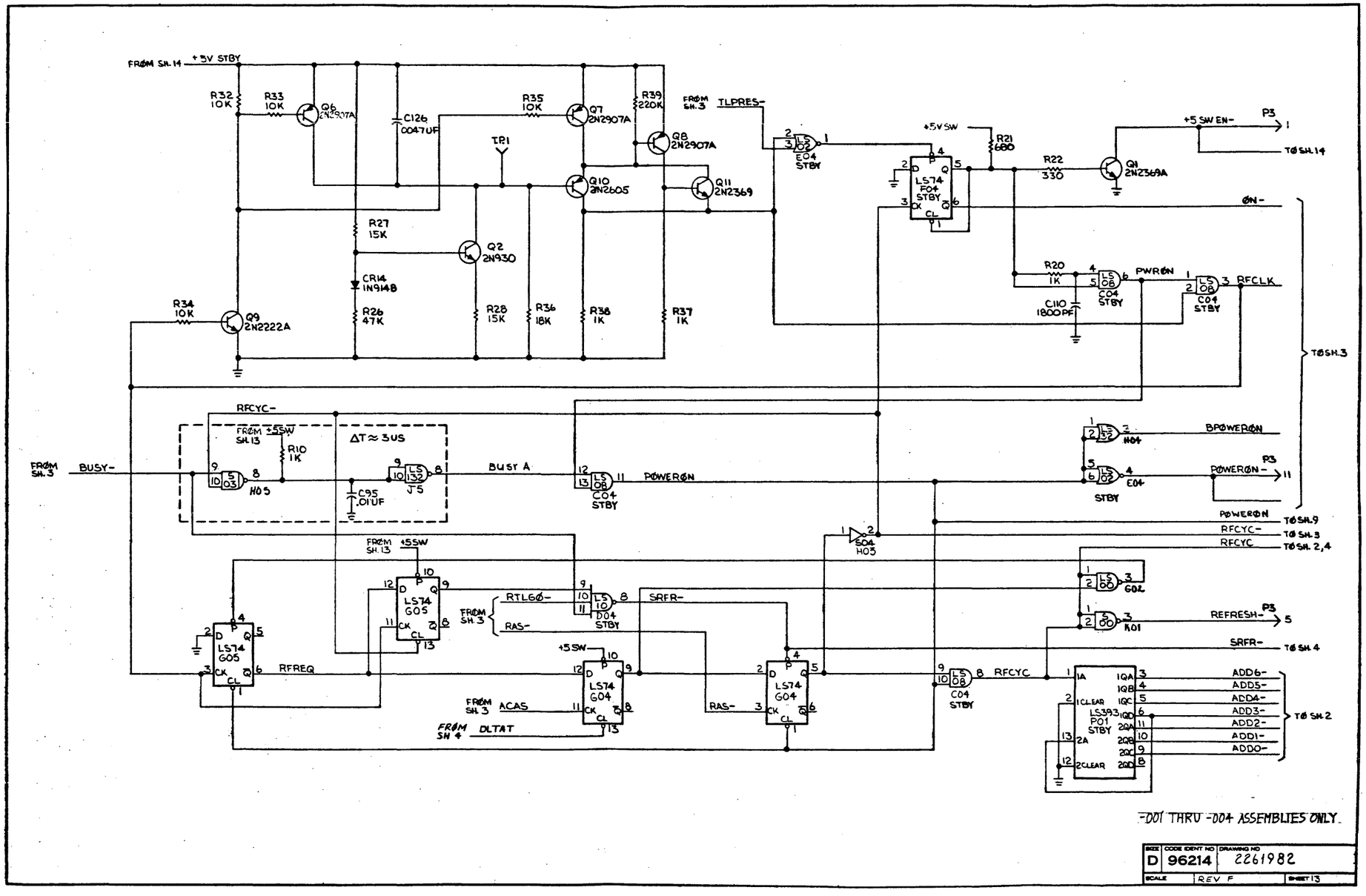

FROM SH.14 +5VSW
FROM SH.2 ADDC THRU ADD6, UISW
FROM SH.14 +5VSTBY
FROM SH.2 BANK1
FROM SH.13 POWERON
FROM SH.3 RAS
FROM SH.2 BANK2
FROM SH.2 BANK3
+5VSW
+5V SW
5VSW -001 THRU -004 12 VSTBY -005 THRU -008
5VSW -001 THRU -004 12VSTBY -005 THRU -008
5 VSW -001 THRU -004 12 VSTBY -005 THRU -008
5VSW -001 THRU -004 12VSTBY -005 THRU -008
M01
M02
N01
N02
L01
L02
L03
R3
R4
R5
R6
R7
R8
22
RASA-
RASB-
RASC-
CASA-
CASB-
CASC-
ADDR3A-
ADDR3B-
ADDR1A-
ADDR1B-
ADDR5A-
ADDR5B-
ADDR6A-
ADDR6B-
ADDR0A-
ADDR0B-
ADDR4A-
ADDR4B-
ADDR2A-
ADDR2B-
R/W A RNWA
R/W B RNWB
ADDR6C-
ADDR4C-
ADDR2C-
ADDR3C-
ADDR0C-
ADDR1C-
ADDR5C-
R/W C
TO SH. 10,11,12
FROM SH.3
CAS
BTLPRES-
READ-
ADD0
ADD1
ADD2
ADD3
ADD4
ADD5
ADD6
UISW
SIZE D
CODE IDENT NO 96214
DRAWING NO 2261982
SCALE
REV F
SHEET 9

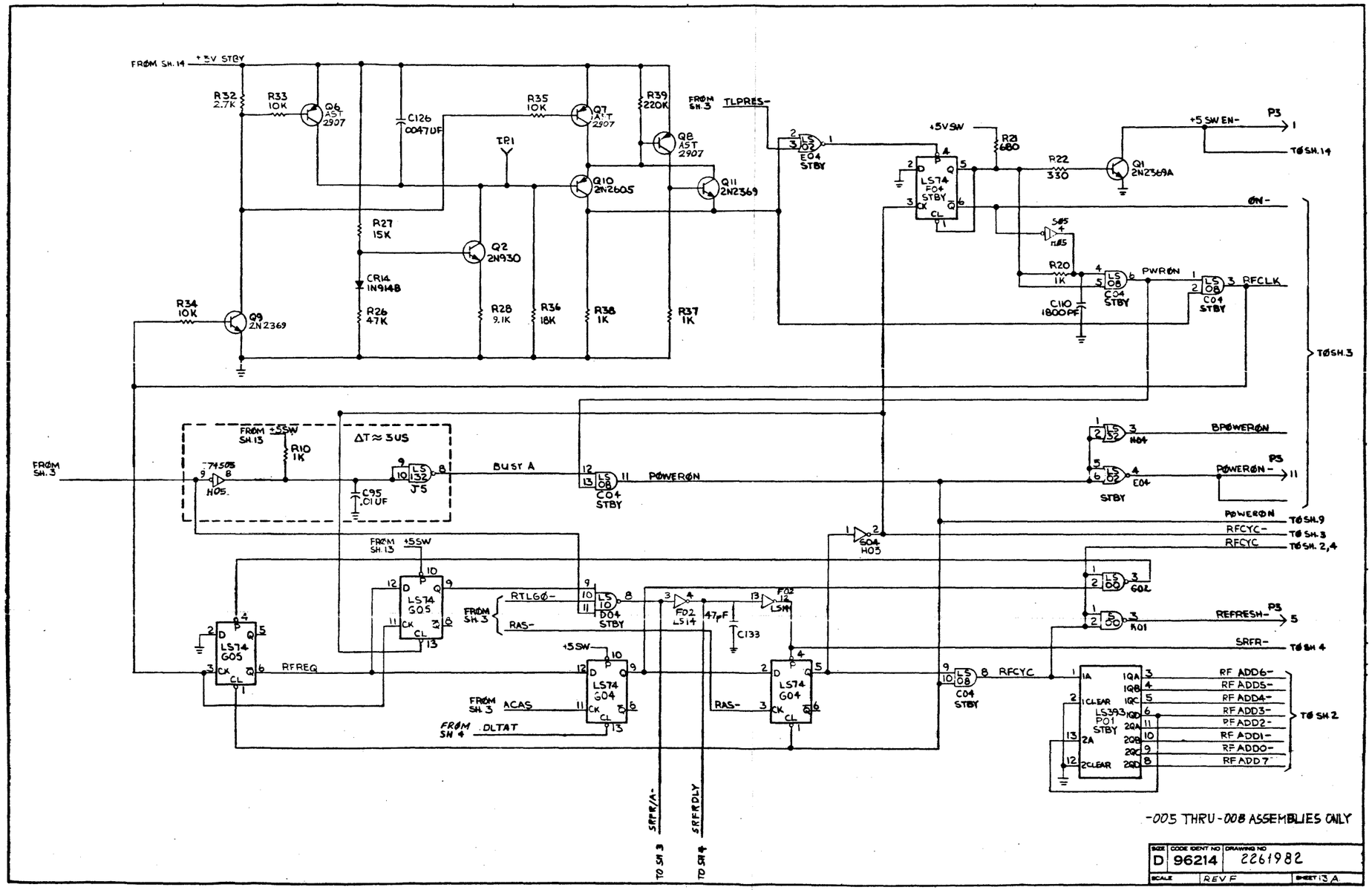

BIT 0
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
BIT 8
BIT 9
TMS 4116
N04
N05
N06
N07
N08
M04
M05
M06
M07
M08
L04
L05
L06
L07
L08
N09
N10
N11
N12
N13
M09
M10
M11
M12
M13
L09
L10
L11
L12
L13
FROM SH. 5
FROM SH. 9
DB00
DB01
DB02
DB03
DB04
DB05
DB06
DB07
DB08
DB09
DØ00
DØ01
DØ02
DØ03
DØ04
DØ05
DØ06
DØ07
DØ08
DØ09
TØ SH. 8
RNWA
RASA-
RNWB
RASB-
RNWC
RASC-
R/W A
R/W B
R/W C
CASA-
CASB-
CASC-
ADDR0A- THRU ADDR6A-
ADDR0B- THRU ADDR6B-
ADDR0C- THRU ADDR6C-
ADDR6A-
ADDR5A-
ADDR4A-
ADDR3A-
ADDR2A-
ADDR1A-
ADDR0A-
ADDR6C-
ADDR5C-
ADDR4C-
ADDR3C-
ADDR2C-
ADDR1C-
ADDR0C-
-5V STBY
+12V STBY
+5V
VBB
DI
R/W
RAS
A0
A1
A2
A3
A4
A5
A6
VDD
VCC
CAS
VSS
NØTE: EACH RØW AND EACH CØLUMN IS WIRED THE SAME UNLESS ØTHERWISE SHØWN
SIZE
CODE IDENT NO
DRAWING NO
D
96214
2261982
SCALE
SHEET 10

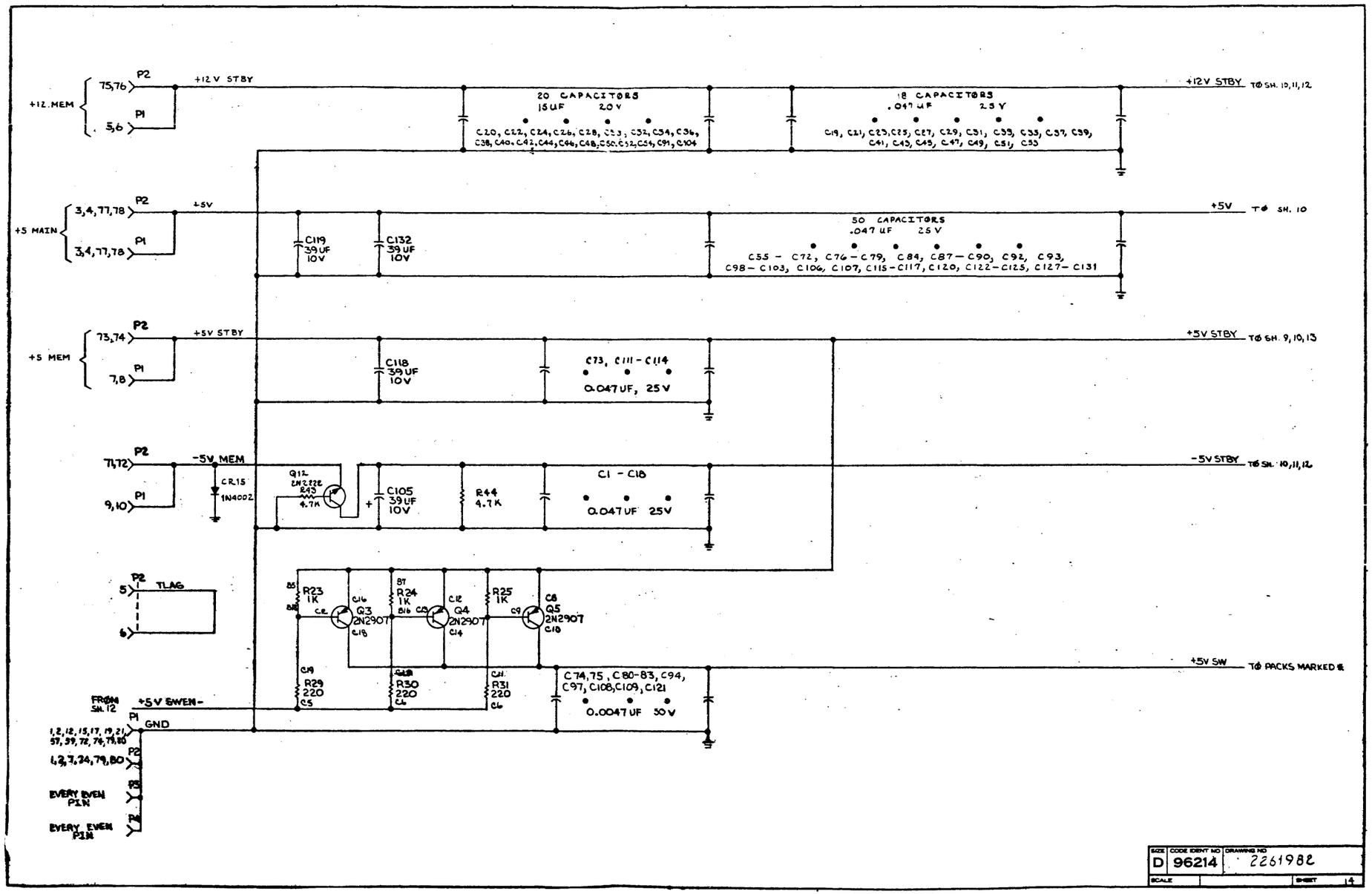

BIT 10
BIT 11
BIT 12
BIT 13
BIT 14
BIT 15
BIT 16
BIT 17
BIT 18
BIT 19
TMS 4116
N14
N15
N16
N17
N18
M14
M15
M16
M17
M18
L14
L15
L16
L17
L18
N19
N20
N21
N22
N23
M19
M20
M21
M22
M23
L19
L20
L21
L22
L23
FROM SH. 5
FROM SH. 9
FROM SH. 7
DB10
DB11
DB12
DB13
DB14
DB15
-5V STBY
+12V STBY
+5V
R/WA
RNWA
RASA-
RASB-
RASC-
CASA-
CASB-
CASC-
ADDR0A- THRU ADDR6A-
ADDR0B- THRU ADDR6B-
ADDR0C- THRU ADDR6C-
DØ10
DØ11
DØ12
DØ13
DØ14
DØ15
CB00-
CB01-
CB02-
CB03-
CBI0-
CBI1-
CBI2-
CBI3-
TØ SH. 8
TØ SH. 7
NOTE: EACH ROW AND COLUMN IS WIRED THE SAME UNLESS OTHERWISE SHOWN
SIZE D
CODE IDENT NO 96214
DRAWING NO 2261982
SCALE
SHEET 11

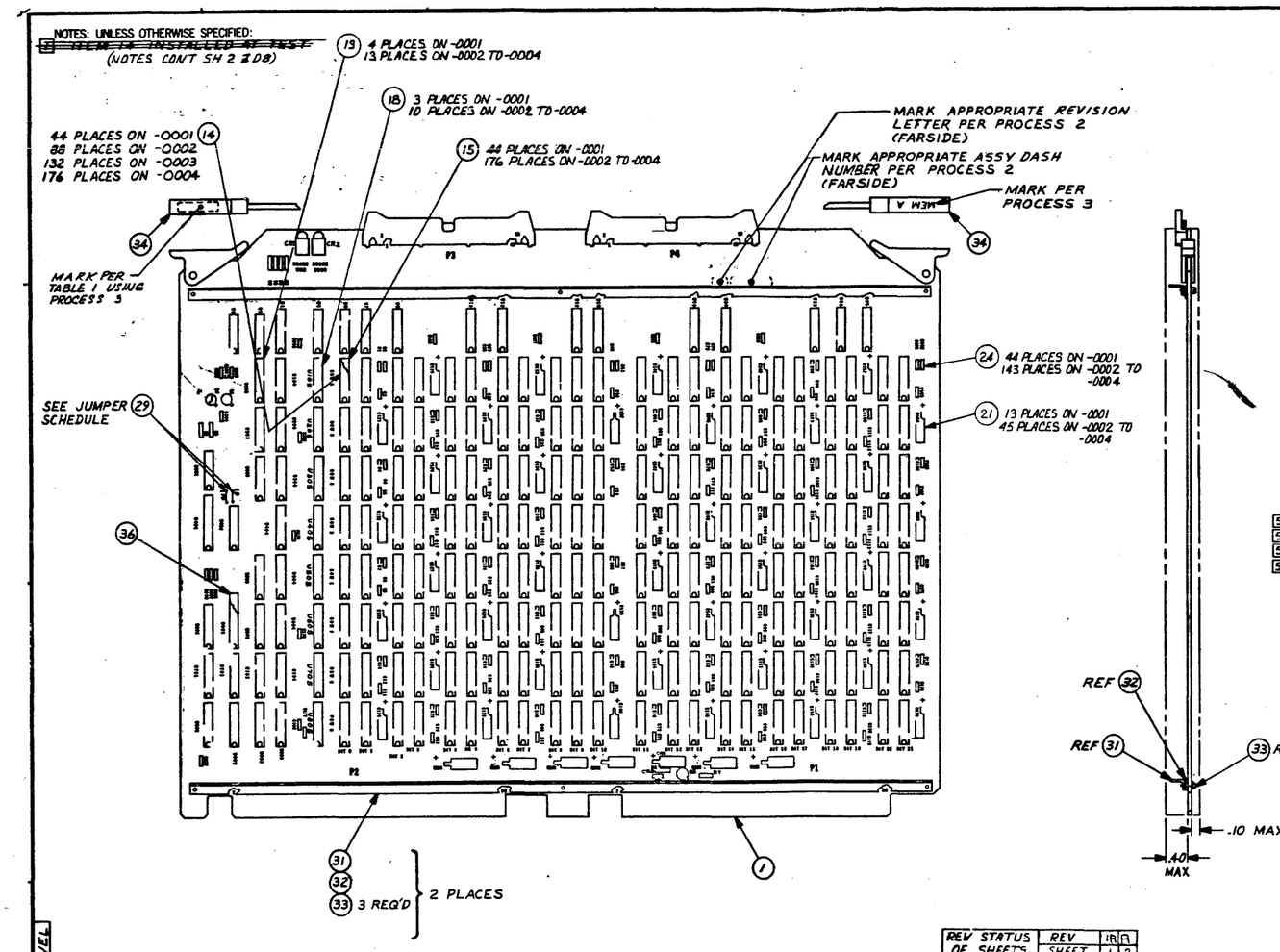

BIT 20
FROM SH. 7
CBI4-
R/W A
RASA-
-5V STBY
ADDR6A-
ADDR5A-
ADDR4A-
ADDR3A-
ADDR2A-
ADDR1A-
ADDR0A-
ADDR0A- THRU ADDR6A-
+12V STBY
+5V
CASA-
TMS 4116
N24
CBO4-
TO SH 8
FROM SH. 9
R/W B
RASB-
ADDR0B- THRU ADDR6B-
CASB-
M24
R/W C
RASC-
ADDR0C- THRU ADDR6C-
CASC-
L24
BIT 21
N25
M25
FROM SH. 7
CBI5-
R/W C
RASC-
-5V STBY
ADDR6C-
ADDR5C-
ADDR4C-
ADDR3C-
ADDR2C-
ADDR1C-
ADDR0C-
ADDR0C- THRU ADDR6C-
+12V STBY
+5V
CASC-
L25
CBO5-
TO SH. 8
+5V
BIT IN ERROR
FROM SH.5
CERR-
LCHERR
LS74
F01
CR7
220
H09
LCC16
TO SH. 6
LCC1
CR3
LCC2
CR4
LCC4
CR5
LCC8
CR6
LS175
E08
CC1
CC2
CC4
CC8
FROM SH. 7
IØRES-
D02
ROW IN ERROR
LADDR4-
LADDR5-
LADDR2-
LADDR3-
LADDR0-
LADDR1-
CR8
CR9
CR10
CR11
CR12
CR13
S169
C03
D06
FROM SH. 3
LCHERR-
CAS-
P04
FROM SH. 2
ADR05-
ADR04-
ADR03-
ADR02-
FROM SH. 5
IBERR-
IBERR
LS04
F02
CRCTDN-
ADR01-
ADR00-
CRCTEN-
FROM SH. 4
TCERR
D02
-001 THRU -004 ASSEMBLIES ONLY
SIZE D
CODE IDENT NO 96214
DRAWING NO 2261982
SCALE
REV F
SHEET 12


BIT 20
FROM SH. 7
CBI4-
R/W̄A
RASA-
ADDR6A-
ADDR5A-
ADDR4A-
ADDR3A-
ADDR2A-
ADDR1A-
ADDR0A-
ADDR0A- THRU ADDR6A-
CASA-
-5V STBY
+12V STBY
+5V
TMS 4116
N24
D6
CB04-
TO SH 8
FROM SH 9
R/W̄B
RASB-
ADDR0B- THRU ADDR6B-
CASB-
M24
R/W̄C
RASC-
ADDR0C- THRU ADDR6C-
CASC-
L24
BIT 21
N25
M25
FROM SH. 7
CBI5-
R/W̄C
RASC-
ADDR6C-
ADDR5C-
ADDR4C-
ADDR3C-
ADDR2C-
ADDR1C-
ADDR0C-
ADDR0C- THRU ADDR6C-
CASC-
L25
CB05-
TO SH. 8
+5V
FROM SH 5
CERR-
LCHERR
LS74
F01
BIT IN ERROR
R2
CR5
LCC16
R1
CR1
LCC1
R47
CR2
LCC2
R48
CR3
LCC4
R49
CR4
LCC8
TO SH 6
FROM SH. 5
CC1
CC2
CC4
CC8
FROM SH. 7
IØRES-
LS175
E08
ROW IN ERRØR
LADDR4-
LADDR5-
LADDR2-
LADDR3-
LADDR0-
LADDR1-
FROM SH 5
LCHERR-
FROM SH 3
CAS-
P04
FROM SH 2
ADRA05
ADRA04
ADRA03
ADRA02
S169
C03
FROM SH 5
IBERR-
L514
F02
IBERR
CRCTDN-
ADRA01-
ADRA00-
CRCTEN-
S169
D06
FROM SH 4
TCERR
D02
-005 THRU -008 ASSEMBLIES ONLY
SIZE D
CODE IDENT NO 96214
DRAWING NO 2261982
SCALE
REV F
SHEET 12A


FROM SH.14 +5V STBY
R32 10K
R33 10K
Q6 2N2907A
C126 .0047UF
R35 10K
Q7 2N2907A
R39 220K
Q8 2N2907A
TP1
Q10 2N2605
Q11 2N2369
FROM SH.3 TLPRES-
E04 STBY
+5V SW
R21 680
R22 330
Q1 2N2369A
+5 SW EN-
P3
TO SH.14
ØN-
R27 15K
Q2 2N930
CR14 1N914B
R34 10K
Q9 2N2222A
R26 47K
R28 15K
R36 18K
R38 1K
R37 1K
R20 1K
C110 1800PF
PWRØN
RFCLK
TO SH.3
RFCYC-
FROM +5SW SH.13
R10 1K
ΔT≈3US
C95 .01UF
H05
J15
FROM SH.3 BUSY-
BUSY A
POWERØN
C04 STBY
BPOWERØN
H04
POWERØN-
P3
11
STBY
POWERØN TO SH.9
RFCYC- TO SH.3
RFCYC TO SH. 2,4
E04 H03
FROM +5SW SH.13
LS74 G05
RTLGØ-
RAS-
FROM SH.3
D04 STBY
SRFR-
G02
REFRESH-
P3
5
H01
SRFR- TO SH.4
RFREQ
+5SW
LS74 G04
FROM ACAS SH.3
FROM DLTAT SH 4
RAS-
C04 STBY
RFCYC
LS393 P01 STBY
ADD6-
ADD5-
ADD4-
ADD3-
ADD2-
ADD1-
ADD0-
TO SH.2
-D01 THRU -D04 ASSEMBLIES ONLY.
SIZE D
CODE IDENT NO 96214
DRAWING NO 2261982
SCALE
REV F
SHEET 13


FROM SH. 14
+5V STBY
R32 2.7K
R33 10K
Q6 AST 2907
C126 .0047UF
R35 10K
Q7 AST 2907
R39 220K
FROM SH.3
TLPRES-
TP1
Q8 AST 2907
Q10 2N2605
Q11 2N2369
R27 15K
Q2 2N930
CR14 1N9148
R34 10K
Q9 2N2369
R26 47K
R28 9.1K
R36 18K
R38 1K
R37 1K
LS10 E04 STBY
+5VSW
R21 680
LS74 F04 STBY
R22 330
Q1 2N2369A
+5 SW EN-
P3
1
TØSH.14
ØN-
5Ø5
R20 1K
C110 1800PF
LS08 C04 STBY
PWRØN
LS08 C04 STBY
RFCLK
TØSH.3
FROM SH.13 +5SW
R10 1K
74S05 H05
ΔT ≈ 3US
C95 .01UF
LS132 J5
BUSY A
LS08 C04 STBY
PØWERØN
BPØWERØN
LS32 H04
PØWERØN-
P3
11
LS02 E04 STBY
PØWERØN
TØ SH.9
RFCYC-
TØ SH.3
RFCYC
TØ SH. 2,4
LS04 H05
FROM SH.13 +5SW
LS74 G05
RTLGØ-
FROM SH.3
RAS-
LS10 D04 STBY
FD2 LS14
47pF
C133
LS00 G02
REFRESH-
P3
5
LS00 A01
SRFR-
TØ SH 4
+5SW
LS74 G04
RFREQ
FROM SH.3 ACAS
FROM SH 4 DLTAT
RAS-
LS08 C04 STBY
RFCYC
LS393 P01 STBY
RF ADD6-
RF ADD5-
RF ADD4-
RF ADD3-
RF ADD2-
RF ADD1-
RF ADDØ-
RF ADD 7
TØ SH 2
SRFR/A-
SRFRDLY
TO SH 3
TO SH 4
-005 THRU -008 ASSEMBLIES ONLY
SIZE D
CODE IDENT NO 96214
DRAWING NO 2261982
SCALE
REV F
SHEET 13A


+12.MEM
P2
75,76
+12 V STBY
P1
5,6
20 CAPACITORS
15UF 20V
C20, C22, C24, C26, C28, C30, C32, C34, C36, C38, C40, C42, C44, C46, C48, C50, C52, C54, C91, C104
18 CAPACITORS
.047 UF 25 V
C19, C21, C23, C25, C27, C29, C31, C33, C35, C37, C39, C41, C43, C45, C47, C49, C51, C53
+12V STBY TO SH. 10, 11, 12
+5 MAIN
P2
3,4,77,78
+5V
P1
3,4,77,78
C119 39 UF 10V
C132 39 UF 10V
50 CAPACITORS
.047 UF 25 V
C55 - C72, C76 - C79, C84, C87 - C90, C92, C93, C98 - C103, C106, C107, C115 - C117, C120, C122 - C125, C127 - C131
+5V TO SH. 10
+5 MEM
P2
73,74
+5V STBY
P1
7,8
C118 39 UF 10V
C73, C111 - C114
0.047 UF, 25V
+5V STBY TO SH. 9, 10, 13
P2
71,72
-5V MEM
P1
9,10
CR.15
1N4002
Q12
2N2222
R43
4.7K
C105 39 UF 10V
R44 4.7K
C1 - C18
0.047 UF 25V
-5V STBY TO SH. 10, 11, 12
P2
5
TLAG
6
R23 1K
Q3 2N2907
R24 1K
Q4 2N2907
R25 1K
Q5 2N2907
C74, 75, C80-83, C94, C97, C108, C109, C121
0.0047 UF 50 V
+5V SW TO PACKS MARKED *
FROM SH. 12
+5V SWEN-
P1
GND
1, 2, 12, 15, 17, 19, 21, 57, 59, 72, 74, 79, 80
P2
1, 2, 7, 24, 79, 80
P3
EVERY EVEN PIN
P4
EVERY EVEN PIN
SIZE D
CODE IDENT NO 96214
DRAWING NO 2261982
SCALE
SHEET 14



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	CN 428573 (D) ... (1) ADD -0001 THRU -0004 LM'S ADDED ITEMS 37,38 & 39 (2) UPDATED REV LEVEL BLOCK	5-16-78	
B	CN 446280 (C) ... (1) REVISED LM PER EXTENSIVE CHANGE (2) ADDED SH2 - NOTE 2, (3) ON SH 1 ADDED ITEMS 13, 18, 21, 24 (2) SH 1, ITEM 15 WAS 176 PL (4) IN BLOCK DESC FOR -0001 THRU -0004 WAS ... 32K, 990/10; ... 64K, 990/10; ... 96K, 990/10; AND ... 128K, 990/10; RESP (5) UPDATED REV LEVEL BLOCK	8-23-78	
C	CN 441026 (B) ... (1) ADDED NOTE 3 ON SH 2 (2) UPDATED REV LEVEL BLOCK	8-23-78	
D	CN 447072 (B) ... (1) ADD LM PN ITEM 37 WAS 972948-0002 (2) UPDATED REV LEVEL BLOCK	10-9-78	
E	CN 451178 (D) ... (1) LM ITEMS 26 & 35 DELETED ON ALL DASH NOS (2) LM ITEM 12 VENDOR PN WAS SN74LS373 ALL DASH NOS (3) ADDED -0004 NONE TO JUMPER SCHEDULE (4) ZONE B-3 DIM .10 MAX WAS .12 MAX (5) DELETED NOTE 1 (6) UPDATE REV LEV BLOCK (7) ZONE B-6 CHGD CR1 MARKING TO CR3 (8) ZONE B-6 MOVED Q13 & R7 MARKING UP FROM UNDER STIFFENER	12-7-78	
F	CN 448554 (B) ... (1) ADDED NOTE 4 ON SH 2 (2) UPDATE REVISION LEVEL BLOCK	1-16-79	
G	CN 441888 (C) ... (1) CREATED -5001, -5002, -5003 AND -5004 LM'S (2) DELETED NOTE 1 (3) ADDED NOTE 5 (4) ADDED TABLE 1 IN B-1 (5) UPDATED REV LEVEL BLOCK	4-5-79	
H	CN 451915 (D) ... (1) UPDATED REV LEVEL BLOCK (2) ON -1, -2, -3 & -4 LM ITEM 15 WAS 539544-2 ITEM 36 WAS 539544-10	4-5-79	

CONTINUED SH 2

5	948955-5004	AUTO-INSERTED PARTS LIST FOR 948955-0004
5	948955-5003	AUTO-INSERTED PARTS LIST FOR 948955-0003
5	948955-5002	AUTO-INSERTED PARTS LIST FOR 948955-0002
5	948955-5001	AUTO-INSERTED PARTS LIST FOR 948955-0001
	948955-0004	MEMORY ADD-ON MODULE, 256KB, 990/16KR
	948955-0003	MEMORY ADD-ON MODULE, 192KB, 990/16KR
	948955-0002	MEMORY ADD-ON MODULE, 128KB, 990/16KR
	948955-0001	MEMORY ADD-ON MODULE, 64KB, 990/16KR
PART NUMBER	DESCRIPTION	

TABLE 1	
DASH NO	SYMBOLIZATION
-0001	64KB
-0002	128 KB
-0003	192 KB
-0004	256KB

JUMPER SCHEDULE	
DASH NO.	INSTALL AT
-0001	E10
-0002	E9
-0003	E9 & E10
-0004	NONE

REV STATUS OF SHEETS	REV	A	A
	SHEET	1	2

REVISION LEVEL																
TEST PROCEDURE 948958-9901	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
LOGIC 948957-9901	*	A	A	A	A	A	B	B	B	B	B	B	B	C	C	C
PWB 948956-0001	B	C	C	C	C	D	D	D	E	E	E	E	E	G	G	G
ASSEMBLY 948955	*	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R

PROCESSES:
1. SOLDER PER F-127, METHOD I AND/OR F-124, METHOD 2
2. MARK PER F-100, METHOD II, CLASS I, HEIGHT .12, COLOR BLACK
3. MARK PER F-100, METHOD VII, CLASS 8, COLOR BLACK, TYPE 6

SEQ NO	IDENT	F-SPEC	NO	ADDITIONAL	NOTES
	PROCESS			CLASSIFICATION	

PROCESSES — FOR CORRELATION TO GOVT/IND SPECIFICATIONS, SEE TI DRAWING 729467

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION	NOTES
		PARTS LIST			

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES ANGLES ±1°; 3 PLACE DECIMALS ± .010; 2 PLACE DECIMALS ± .02
- INTERPRET DRAWING PER MIL-D-1000
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIM
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

.013 THRU .125 +.004 -.001	.126 THRU .250 +.005 -.001	.251 THRU .500 +.006 -.001
.501 THRU .750 +.008 -.001	.751 THRU 1.000 +.010 -.001	1.001 THRU 2.000 +.012 -.001

NEXT ASSY	USED ON
	7506
APPLICATION	

DWN	3	8/29/77
ENGR		5-2-77
MGR		5-11-77
MFG		11-29-77
QA		12/6/77
DESIGN		12/12/77
MFG		12/29/77

TEXAS INSTRUMENTS INCORPORATED Dallas, Texas

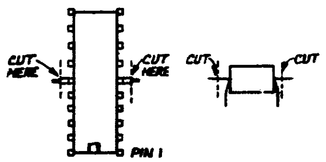
MEMORY ADD-ON MODULE, 990/16 KR

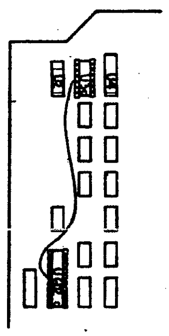
SIZE	FSCM NO	DRAWING NO
D	96214	948955

SCALE 1/1 SHEET 1 OF 2

NOTES CONT.

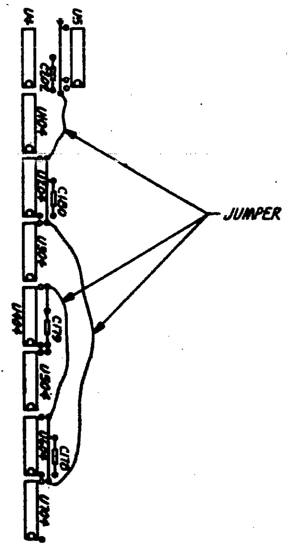
2. REWORK FOR PWB 948956 REV B AND GREATER
~~IF ITEM 10 IS UNAVAILABLE SUBSTITUTE PART 2261987-0001 IN LOCATION U602. REWORK PWB AS FOLLOWS:~~
A. BEND AND CLIP LEADS ON ITEM 10 AS SHOWN BELOW





B. INSTALL ITEM 10 IN LOCATION U602 AND ADD JUMPER WIRE (30 AWG INSULATED) BETWEEN U602 PIN 15 AND U3 PIN 11 AS SHOWN.
C. SECURE JUMPER WIRE WITH THERMOPLASTIC ADHESIVE.

3. REWORK PROCEDURE FOR PWB 948956 UP TO REV C
A. SOLDER 24AWG SOLID CONDUCTOR JUMPER WIRE ON COMPONENT SIDE AS SHOWN:



4. REWORK PROCEDURE FOR ALL REVISION LEVEL PWB'S;
A. CUT PIN 9 AT THE FOLLOWING LOCATIONS:
U104, U204
U304, U404 (-2,-3,-4 ONLY)
U504, U604 (-2,-3,-4 ONLY)
U704, U804 (-2,-3,-4 ONLY)

B. ADD JUMPER WIRES AS FOLLOWS:

FROM	TO	
U104-9 (DEVICE)	U204-9 (DEVICE)	
U204-9 (DEVICE)	C121+	
U304-9 (DEVICE)	U404-9 (DEVICE)	(-2,-3,-4 ONLY)
U404-9 (DEVICE)	C122+	(-2,-3,-4 ONLY)
U504-9 (DEVICE)	U604-9 (DEVICE)	(-2,-3,-4 ONLY)
U604-9 (DEVICE)	C123+	(-2,-3,-4 ONLY)
U704-9 (DEVICE)	U804-9 (DEVICE)	(-2,-3,-4 ONLY)
U804-9 (DEVICE)	C124+	(-2,-3,-4 ONLY)

C. VERIFY ICADSEL TO COLUMN ADDRESS AT MEMORY DEVICE PROPAGATION TIME TO BE LESS THAN 55ns FOR EACH ROW. THIS MAY BE ACCOMPLISHED BY RUNNING PRODUCTION ADAR TEST.

5. ITEM 40 IN -0001, -0002, -0003 AND -0004 LM'S CONSISTS OF COMPONENTS WHICH ARE AUTO-INSERTED AND CONTAINED IN THE -5001, -5002, -5003 AND -5004 LM'S

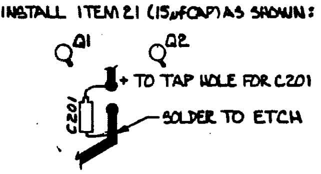
6. REWORK PROCEDURE FOR ALL REVISION LEVEL PWB'S:
A. ADD ITEM 23 (.0047µF AXIAL CAP) IN THE FOLLOWING LOCATIONS:

FROM	TO	
U104-1	C180 (END NEAR U104)	(-1,-2,-3,-4 ONLY)
U304-1	C179 (END NEAR U304)	(-2,-3,-4 ONLY)
U504-1	C178 (END NEAR U504)	(-2,-3,-4 ONLY)
U704-1	C198 (END NEAR U704)	(-2,-3,-4 ONLY)

B. USING 24 AWG SOLID CONDUCTOR JUMPER WIRE, ADD JUMPERS AS FOLLOWS:

FROM	TO	
C121−	C180 (END NEAR U104)	(-1,-2,-3,-4)
C122−	C179 (END NEAR U304)	(-2,-3,-4)
C124−	C198 (END NEAR U704)	(-2,-3,-4)
U802-8	U702-7	(-1,-2,-3,-4)
U702-8	C123−	(-1,-2,-3,-4)

C. INSTALL ITEM 21 (15µF CAP) AS SHOWN:



REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
J	CN441740 (C) (1) ON -5001, 5002, 5003 & 5004 LM DELETED ITEM 21, C191 & C193 ONLY & ITEM 24, C197 ONLY AND ADDED TO -1,2,3, & 4 LM (2) UPDATED REV LEVEL BLOCK	4-5-79	
K	CN 436830 (B) (1) REWORK NOTE 4A U504, U604 WAS (-3,-4 ONLY), U704, U804 WAS (-4 ONLY) (2) REWORK NOTE 4 B, U504-9 AND U604-9 WERE (-3,-4 ONLY), U704-9 AND U804-9 WERE (-4 ONLY) (3) ADDED REWORK NOTE 6 (4) UPDATED REV LEVEL BLOCK (5) -1 LM ITEM 24 QTY WAS 1 (6) -2, -3, -4 LM ITEM 24 QTY WAS 1	5-23-79	
L	CN 448725 (B) B. Bell (1) ON SH 2 NOTE 6A WAS "ADD ITEM 24..." (2) ON LM -1,-2,-3 &-4 ITEM 23 QTY WAS 7, DESC WAS C177-C180, C185, C199 & C202 (3) ON LM -2,-3 &-4 QTY ITEM 24 WAS 5, C203-C206 DELETED FROM DESC, ON -1 QTY WAS 2, C203 DELETED FROM DESC (4) ON LM -5001 THRU -5004 ITEM 24 QTY WAS 43, 142, 142, 142, RESP, C201 DELETED FROM DESC (5) ON LM-1 THRU -4 QTY ITEM 21 WAS 2, ADDED C201 TO DESC (6) ADDED NOTE 6C TO SH 2 (6) UPDATED REV LVL BLK	8-8-79	
M	CN 435043 (E) D. (1) L/M -1,2,3 & 4 ITEM 10 P/N WAS 2261986-0001 (2) UPDATED REV LEVEL BLOCK	8-8-79	
N	CN 435564 (C) JB (1) UPDATED REV LEVEL BLOCK (2) ON SH 2, NOTE 2. DELETED 2ND & 3RD LINES & IN NOTES 2A & 2B ITEM 10 WAS 2261987-0001	11-14-79	
P	CN 451307 (D) JB (1) DELETED FROM -5001, -5002, -5003, & -5004 LM'S ITEM 11, U23 & ADDED TO -0001, -0002, -0003, -0004 LM'S (2) UPDATED REV LEVEL BLOCK	11-14-79	
R	CN 450535 (D) C. (1) ON SHT 1, DELETED BALLOON ITEMS 26 (ZN C-8) & 35 (ZN'S A-7 & B-3) (2) UPDATED REV LEVEL BLOCK.	3 DEC. 79	

TEXAS INSTRUMENTS | DATE 6/22/78 | SIZE D | FSCM NO 96214 | DRAWING NO 948955 | REV R | SHEET 2

TEXAS INSTRUMENTS INCORPORATED — DATE 10/18/79 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM0948955-0001 REV R

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	REF	EA		0948957-9901	LOGIC,MEMORY ADD-ON MODULE,990/10	
0003	REF	EA		0948958-9901	TEST PROCEDURE,MEM ADD-ON MODULE,990/10	
0004	REF	EA		0948959-9901	SPECIFICATION, MEM ADD-ON MODULE,990/10	
0010	00001.000	EA		2261987-0001	ROM,ADDRESS DECODE,16KR MEMORY EXPANSION	
0010A					U602	
0011	00001.000	EA		0972787-0004	NETWORK SN74LS368N	
0011A					U23	
0012	00001.000	EA		0996420-0001	IC, SN74LS373N	001295-SN74LS373N
0012A					U401	
0014	00044.000	EA		0996680-0001	IC, 16K RAM, (SEL)	001295-TMS4116/ZA0727
0014A					UA0 THRU UA21	
0014B					UB0 THRU UB21	
0015	00044.000	EA		2210188-0003	SOCKET,LOW PROFILE,DIP,16 CONT	003612-DIL816P-108
0015A					XUA0 THRU XUA21	
0015B					XUB0 THRU XUB21	
0021	00003.000	EA		0972924-0014	CAP FIX TANT SOLID 15 MFD 10 % 20 VOLT	QPL -M39003/1-2289
0021A					C191 C193 C201	
0022	00005.000	EA		0972924-0006	CAP FIX TANT SOLID 39 MFD 10 % 10 VOLT	QPL -M39003/1-2259
0022A					C190 C192 C194 C195 C196	
0023	00011.000	EA		0972763-0009	CAP,FIXED .0047MF 50 VOLTS	004222-MC105E472Z

DRAFTSMAN — DATE — CKD. DRAFTSMAN J. Roth 10-22-79 — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY ADD-ON MODULE,64KB,990/16KR

APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. 7506 — PART NUMBER LM0948955-0001 REV R

TEXAS INSTRUMENTS INCORPORATED — DATE 10/18/79 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM0948955-0001 REV R

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0023A					C177 C178 C179 C180 C185	
0023B					C199 C202 C203 C204 C205	
0023C					C206	
0024	00001.000	EA		C972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0024A					C197	
0025	00002.000	EA		0972958-0002	TRANSISTOR,2N2907A PNP GEN PURP SW TO-18	TI - 2N2907A
0025A					Q1 Q2	
0027	00001.000	EA		0972547-0008	SWITCH, SLIDE-SPST,DIP 8 SWITCHES	
0027A					U601	
0028	00002.000	EA		0972537-0001	DIODE,LED 550-0103 50 MA 3 V	DIA --550-0103
0028A					CR1 CR2	
0029	00000.100	FT		0411400-0022	WIRE 22AWG ELETRO-TIN-PLATED,COPPER	
0030	00002.000	EA		0972137-0005	CONNECTOR,PC 50 PIN	BEI - 65483-005
0030A					P3 P4	
0031	00002.000	EA		0945239-0001	BRACKET-STIFFENER, PWB, 14IN	
0032	00002.000	EA		0944954-0001	INSULATOR, PWB, 14IN	
0033	00006.000	EA		0972684-0002	SCREW,THD FRMG,HEX WSHR HD,2-56X1/4 LG	
0034	00002.000	EA		0533844-0001	EJECTOR, NYLON, NON-LOCKING, PWB	
0036	00001.000	EA		2210188-0005	SOCKET, LOW PROFILE, DIP, 20 PINS	003612-DIL820P-108
0036A					XU602	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: MEMORY ADD-ON MODULE,64KB,990/16KR

APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM0948955-0001 REV R

T.I. 13649

TEXAS INSTRUMENTS
INCORPORATED

DATE 10/18/79 — LIST OF MATERIAL — PAGE 3 of — PART NUMBER LM0948955-0001 REV R

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0037	00001.000	EA		0972057-0001	TRANSISTOR-A5T2222 NPN SILICON	TI- -A5T2222
0037A					Q3	
0038	00002.000	EA		0972946-0081	RES FIX 4.7K OHM 5 % .25 W CARBON FILM	ROH - R-25
0038A					R7 R8	
0039	00001.000	EA		0539468-0002	DIODE,1N4002 1AMP 100PIV RECTIFIER	TI - IN4002
0039A					CR3	
0040	00001.000	EA		0948955-5801	AUTO-INSERTED PARTS LIST FOR 948955-0001	

DRAFTSMAN	DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						MEMORY ADD-ON MODULE,64KB,990/16KR
APPD.-MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						LM0948955-0001 R

T.I. 13849

TEXAS INSTRUMENTS INCORPORATED — DATE 10/18/79 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM0948955-5001 REV R

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0948956-0001	PWB,MEMORY ADD-ON MODULE,990/10	
0005	00001.000	EA		0219402-7404	NETWORK SN74S04N	
0005A					U3	
0006	00001.000	EA		0222222-7430	NETWORK SN7430N	-SN7430N
0006A					U301	
0007	00001.000	EA		0972900-7474	NETWORK SN74LS74N	
0007A					U2	
0008	00002.000	EA		0996136-0002	IC,SN74LS258N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS258N
0008A					U802 U803	
0009	00002.000	EA		0972652-0001	NETWORK SN74LS283N	
0009A					U701 U702	
0011	00012.000	EA		0972787-0004	NETWORK SN74LS368N	
0011A					U4 U5 U7 U8 U11 U12 U15 U16	
0011B					U19 U20 U24 U25	
0013	00004.000	EA		0972583-0001	NETWORK,SN75365	TI- -SN75365
0013A					U6 U103 U104 U204	
0016	00001.000	EA		0972037-3470	RES. NETWORK,4.7K OHM 2%	
0016A					U402	
0017	00001.000	EA		0972037-2680	NETWORK RESISTOR 680 OHMS 2%	073138-898-3-R680
0017A					U801	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 948955-0001

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0948955-5001 REV R

T.I. 13849

TEXAS INSTRUMENTS INCORPORATED — DATE 10/18/79 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM0948955-5001 REV R

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0018	00003.000	EA		0972037-1220	NETWORK,RES 16 PIN,8 ELEMENT 22 OHMS +2%	073138-898-3-R22
0018A					U105 U205 U203	
0019	00004.000	EA		0972946-0049	RES FIX 220 OHM 5 % .25 W CARBON FILM	ROH - R-25
0019A					R1 R2 R3 R6	
0020	00002.000	EA		0972946-0065	RES FIX 1.0K OHM 5% .25 W CARBON FILM	ROH - R-25
0020A					R4 R5	
0021	00011.000	EA		0972924-0014	CAP FIX TANT SOLID 15 MFD 10 % 20 VOLT	QPL -M39003/1-2289
0021A					C121 C125 C129 C133 C137	
0021B					C141 C145 C149 C153 C157	
0021C					C164	
0024	00042.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0024A					C1 C2 C3 C13 C14 C15 C25	
0024B					C26 C27 C37 C38 C39 C49 C50	
0024C					C51 C61 C62 C63 C73 C74 C75	
0024D					C85 C86 C87 C97 C98 C99	
0024E					C109 C110 C111 C161 C162	
0024F					C163 C181 THRU C184	
0024G					C186 THRU C189 C198	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 948955-0001

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0948955-5001 REV R

T.I. 13849

TEXAS INSTRUMENTS INCORPORATED

DATE 10/18/79 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM0948955-0002 REV R

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	REF	EA		0948957-9901	LOGIC,MEMORY ADD-ON MODULE,990/10	
0003	REF	EA		0948958-9901	TEST PROCEDURE,MEM ADD-ON MODULE,990/10	
0004	REF	EA		0948959-9901	SPECIFICATION, MEM ADD-ON MODULE,990/10	
0010	00001.000	EA		2261987-0001	RON,ADDRESS DECODE,16KR MEMORY EXPANSION	
0010A					U402	
0011	00001.000	EA		0972787-0004	NETWORK SN74LS368N	
0011A					U23	
0012	00001.000	EA		0996420-0001	IC, SN74LS373N	001295-SN74LS373N
0012A					U401	
0014	00088.000	EA		0996680-0001	IC, 16K RAM, (SEL)	001295-TMS4116/ZA0727
0014A					UA0 THRU UA21	
0014B					UB0 THRU UB21	
0014C					UC0 THRU UC21	
0014D					UD0 THRU UC21	
0015	00176.000	EA		2210188-0003	SOCKET,LOW PROFILE,DIP,16 CONT	003612-DIL816P-108
0015A					XUA0 THRU XUA21	
0015B					XUB0 THRU XUB21	
0015C					XUC0 THRU XUC21	
0015D					XUD0 THRU XUD21	
0015E					XUE0 THRU XUE21	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: MEMORY ADD-ON MODULE,128KB,990/16KR

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0948955-0002 REV R

T.I. 13849

TEXAS INSTRUMENTS INCORPORATED

DATE 10/18/79 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM0948955-0002 REV R

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0015F					XUF0 THRU XUF21	
0015G					XUG0 THRU XUG21	
0015H					XUH0 THRU XUH21	
0021	00003.000	EA		0972924-0014	CAP FIX TANT SOLID 15 MFD 10 % 20 VOLT	QPL -M39003/1-2289
0021A					C191 C193 C201	
0022	00005.000	EA		0972924-0006	CAP FIX TANT SOLID 39 MFD 10 % 10 VOLT	QPL -M39003/1-2259
0022A					C190 C192 C194 C195 C196	
0023	00011.000	EA		0972763-0009	CAP,FIXED .0047MF 50 VOLTS	004222-MC105E472Z
0023A					C177 C178 C179 C180 C185	
0023B					C199 C202 C203 C204 C205	
0023C					C206	
0024	00001.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0024A					C197	
0025	00002.000	EA		0972958-0002	TRANSISTOR,2N2907A PNP GEN PURP SW TO-18	TI - 2N2907A
0025A					Q1 Q2	
0027	00001.000	EA		0972547-0008	SWITCH, SLIDE-SPST,DIP 8 SWITCHES	
0027A					U601	
0028	00002.000	EA		0972537-0001	DIODE,LED 550-0103 50 MA 3 V	DIA --550-0103
0028A					CR1 CR2	
0029	00400.100	FT		0411400-0022	WIRE 22AWG ELETRO-TIN-PLATED,COPPER	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: MEMORY ADD-ON MODULE,128KB,990/16KR

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0948955-0002 REV R

T.I. 13849

TEXAS INSTRUMENTS INCORPORATED

DATE 10/18/79 — LIST OF MATERIAL — PAGE 3 of — PART NUMBER LM0948955-0002 REV R

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0030	00002.000	EA		0972137-0005	CONNECTOR,PC 50 PIN	BEI - 65483-005
0030A					P3 P4	
0031	00002.000	EA		0945239-0001	BRACKET-STIFFENER, PWB, 14IN	
0032	00002.000	EA		0944954-0001	INSULATOR, PWB, 14IN	
0033	00006.000	EA		0972684-0002	SCREW,THD FRMG,HEX WSHR HD,2-56X1/4 LG	
0034	00002.000	EA		0533844-0001	EJECTOR, NYLON, NON-LOCKING, PWB	
0036	00001.000	EA		2210188-0005	SOCKET, LOW PROFILE, DIP, 20 PINS	003612-DIL820P-108
0036A					XU602	
0037	00001.000	EA		0972057-0001	TRANSISTOR-A5T2222 NPN SILICON	TI- -A5T2222
0037A					Q3	
0038	00002.000	EA		0972946-0081	RES FIX 4.7K OHM 5 % .25 W CARBON FILM	ROH - R-25
0038A					R7 R8	
0039	00001.000	EA		0539468-0002	DIODE,1N4002 1AMP 100PIV RECTIFIER	TI - IN4002
0039A					CR3	
0040	00001.000	EA		0948955-0002	AUTO-INSERTED PARTS LIST FOR 948955-0002	

DRAFTSMAN / DATE	CKD. DRAFTSMAN / DATE	DESIGN ENGINEER / DATE	TITLE
			MEMORY ADD-ON MODULE,128KB,990/16KR
APPD.-MFG. / DATE	APPD. PROJECT ENGINEER / DATE	RELEASED / DATE	PROJECT NO.
			PART NUMBER LM0948955-0002 REV R

T.I. 13849

TEXAS INSTRUMENTS INCORPORATED — DATE 10/18/79 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM0948955-5002 REV R

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0948956-0001	PWB,MEMORY ADD-ON MODULE,990/10	
0005	00001.000	EA		0219402-7404	NETWORK SN74S04N	
0005A					U3	
0006	00001.000	EA		0222222-7430	NETWORK SN7430N	-SN7430N
0006A					U301	
0007	00001.000	EA		0972900-7474	NETWORK SN74LS74N	
0007A					U2	
0008	00002.000	EA		0996136-0002	IC,SN74LS258N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS258N
0008A					U802 U803	
0009	00002.000	EA		0972652-0001	NETWORK SN74LS283N	
0009A					U701 U702	
0011	00012.000	EA		0972787-0004	NETWORK SN74LS368N	
0011A					U4 U5 U7 U8 U11 U12 U15 U16	
0011B					U19 U20 U24 U25	
0013	00013.000	EA		0972583-0001	NETWORK,SN75365	TI- -SN75365
0013A					U104 U204 U304 U404 U504	
0013B					U604 U704 U804 U6 U103 U303	
0013C					U503 U703	
0016	00001.000	EA		0972037-3470	RES. NETWORK,4.7K OHM 2%	
0016A					U402	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 948955-0002

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0948955-5002 REV R

T.I. 13849

TEXAS INSTRUMENTS INCORPORATED — DATE 10/18/79 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM0948955-5002 REV R

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0017	00001.000	EA		0972037-2680	NETWORK RESISTOR 680 OHMS 2%	073138-898-3-R680
0017A					U801	
0018	03010.000	EA		0972037-1220	NETWORK,RES 16 PIN,8 ELEMENT 22 OHMS +2%	073138-898-3-R22
0018A					U105 U205 U305 U405 U505	
0018B					U605 U705 U805 U203 U603	
0019	00004.000	EA		0972946-0049	RES FIX 220 OHM 5 % .25 W CARBON FILM	ROH - R-25
0019A					R1 R2 R3 R6	
0020	00002.000	EA		0972946-0065	RES FIX 1.0K OHM 5% .25 W CARBON FILM	ROH - R-25
0020A					R4 R5	
0021	00043.000	EA		0972924-0014	CAP FIX TANT SOLID 15 MFD 10 % 20 VOLT	QPL -M39003/1-2289
0021A					C121 THRU C137	
0021B					C139 THRU C160	
0021C					C164 C168 C172 C176	
0024	00141.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0024A					C1 THRU C120 C161 THRU C163	
0024B					C165 THRU C167	
0024C					C169 THRU C171	
0024D					C173 THRU C175	
0024E					C181 THRU C184	
0024F					C186 THRU C189 C198	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 948955-0002

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0948955-5002 REV R

T.I. 13849

TEXAS INSTRUMENTS
INCORPORATED

DATE 10/18/79 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM0948955-0003 REV R

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	REF	EA		0948957-9901	LOGIC,MEMORY ADD-ON MODULE,990/10	
0003	REF	EA		0948958-9901	TEST PROCEDURE,MEM ADD-ON MODULE,990/10	
0004	REF	EA		0948959-9901	SPECIFICATION, MEM ADD-ON MODULE,990/10	
0010	00001.000	EA		2261987-0001	ROM,ADDRESS DECODE,16KR MEMORY EXPANSION	
0010A					U402	
0011	00001.000	EA		0972787-0004	NETWORK SN74LS348N	
0011A					U23	
0012	00001.000	EA		0996420-0001	IC, SN74LS373N	001295-SN74LS373N
0012A					U401	
0014	00132.000	EA		0996680-0001	IC, 16K RAM, (SEL)	001295-TMS4116/ZA072Z
0014A					UA0 THRU UA21	
0014B					UB0 THRU UB21	
0014C					UC0 THRU UC21	
0014D					UD0 THRU UD21	
0014E					UE0 THRU UE21	
0014F					UF0 THRU UF21	
0015	00176.000	EA		2210188-0003	SOCKET,LOW PROFILE,DIP,16 CONT	003612-DIL816P-108
0015A					XUA0 THRU XUA21	
0015B					XUB0 THRU XUB21	
0015C					XUC0 THRU XUC21	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: MEMORY ADD-ON MODULE,192K8,990/16KR

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0948955-0003 REV R

T.I. 13849

TEXAS INSTRUMENTS
INCORPORATED

DATE 10/18/79 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM0948955-0003 REV R

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0015D					XUD0 THRU XUD21	
0015E					XUE0 THRU XUE21	
0015F					XUF0 THRU XUF21	
0015G					XUG0 THRU XUG21	
0015H					XUH0 THRU XUH21	
0021	00003.000	EA		0972924-0014	CAP FIX TANT SOLID 15 MFD 10 % 20 VOLT	QPL -M39003/1-2289
0021A					C191 C193 C201	
0022	00005.000	EA		0972924-0006	CAP FIX TANT SOLID 39 MFD 10 % 10 VOLT	QPL -M39003/1-2259
0022A					C190 C192 C194 C195 C196	
0023	00011.000	EA		0972763-0009	CAP,FIXED .0047MF 50 VOLTS	004222-MC105E472Z
0023A					C177 C178 C179 C180 C185	
0023B					C199 C202 C203 C204 C205	
0023C					C206	
0024	00001.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0024A					C197	
0025	00002.000	EA		0972958-0002	TRANSISTOR,2N2907A PNP GEN PURP SW TO-18	TI - 2N2907A
0025A					Q1 Q2	
0027	00001.000	EA		0972547-0008	SWITCH, SLIDE-SPST,DIP 8 SWITCHES	
0027A					U601	
0028	00002.000	EA		0972537-0001	DIODE,LED 550-0103 50 MA 3 V	DIA --550-0103

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: MEMORY ADD-ON MODULE,192K8,990/16KR

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0948955-0003 REV R

T.I. 13849

TEXAS INSTRUMENTS INCORPORATED — DATE 10/18/79 — LIST OF MATERIAL — PAGE 3 of — PART NUMBER LM0948955-0003 REV R

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0028A					CR1 CR2	
0029	00000.100	FT		0411400-0022	WIRE 22AWG ELETRO-TIN-PLATED,COPPER	
0030	00002.000	EA		0972137-0005	CONNECTOR,PC 50 PIN	BEI - 65483-005
0030A					P3 P4	
0031	00002.000	EA		0945239-0001	BRACKET-STIFFENER, PWB, 14IN	
0032	00002.000	EA		0944954-0001	INSULATOR, PWB, 14IN	
0033	00006.000	EA		0972684-0002	SCREW,THD FRMG,HEX WSHR HD,2-56X1/4 LG	
0034	00002.000	EA		0533844-0001	EJECTOR, NYLON, NON-LOCKING, PWB	
0036	00001.000	EA		2210188-0005	SOCKET, LOW PROFILE, DIP, 20 PINS	003612-DIL820P-108
0036A					XU602	
0037	00001.000	EA		0972057-0001	TRANSISTOR-A5T2222 NPN SILICON	TI- -A5T2222
0037A					Q3	
0038	00002.000	EA		0972946-0081	RES FIX 4.7K OHM 5 % .25 W CARBON FILM	ROH - R-25
0038A					R7 R8	
0039	00001.000	EA		0539468-0002	DIODE,1N4002 1AMP 100PIV RECTIFIER	TI - IN4002
0039A					CR3	
0040	00001.000	EA		0948955-0003	AUTO-INSERTED PARTS LIST FOR 948955-0003	

DRAFTSMAN	DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						MEMORY ADD-ON MODULE,192KB,990/16KR
APPD.-MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						PART NUMBER LM0948955-0003 REV R

T.I. 13849

TEXAS INSTRUMENTS INCORPORATED

DATE 10/18/79 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM0948955-5003 REV R

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0948956-0001	PWB,MEMORY ADD-ON MODULE,990/10	
0005	00001.000	EA		0219402-7404	NETWORK SN74S04N	
0005A					U3	
0006	00001.000	EA		0222222-7430	NETWORK SN7430N	-SN7430N
0006A					U301	
0007	00001.000	EA		0972900-7474	NETWORK SN74LS74N	
0007A					U2	
0008	00002.000	EA		0996136-0002	IC,SN74LS258N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS258N
0008A					U802 U803	
0009	00002.000	EA		0972652-0001	NETWORK SN74LS283N	
0009A					U701 U702	
0011	00012.000	EA		0972787-0004	NETWORK SN74LS368N	
0011A					U4 U5 U7 U8 U11 U12 U15 U16	
0011B					U19 U20 U24 U25	
0013	00013.000	EA		0972583-0001	NETWORK,SN75365	TI- -SN75365
0013A					U104 U204 U304 U404 U504	
0013B					U604 U704 U804 U6 U103 U303	
0013C					U503 U703	
0016	00001.000	EA		0972037-3470	RES. NETWORK,4.7K OHM 2%	
0016A					U402	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 948955-0003

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0948955-5003 REV R

T.I. 13849

TEXAS INSTRUMENTS INCORPORATED

DATE 10/18/79 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM0948955-5003 REV R

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0017	00001.000	EA		0972037-2680	NETWORK RESISTOR 680 OHMS 2%	073138-898-3-R680
0017A					U801	
0018	00010.000	EA		0972037-1220	NETWORK,RES 16 PIN,8 ELEMENT 22 OHMS +2%	073138-898-3-R22
0018A					U105 U205 U305 U405 U505	
0018B					U605 U705 U805 U203 U603	
0019	00004.000	EA		0972946-0049	RES FIX 220 OHM 5 % .25 W CARBON FILM	ROH - R-25
0019A					R1 R2 R3 R6	
0020	00002.000	EA		0972946-0065	RES FIX 1.0K OHM 5% .25 W CARBON FILM	ROH - R-25
0020A					R4 R5	
0021	00043.000	EA		0972924-0014	CAP FIX TANT SOLID 15 MFD 10 % 20 VOLT	QPL -M39003/1-2289
0021A					C121 THRU C137	
0021B					C139 THRU C160	
0021C					C164 C168 C172 C176	
0024	00141.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0024A					C1 THRU C120 C161 THRU C163	
0024B					C165 THRU C167	
0024C					C169 THRU C171	
0024D					C173 THRU C175	
0024E					C181 THRU C184	
0024F					C186 THRU C189 C198	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 948955-0003

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0948955-5003 REV R

T.I. 13849

TEXAS INSTRUMENTS INCORPORATED — DATE 10/18/79 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM0948955-0004 REV R

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	REF	EA		0948957-9901	LOGIC,MEMORY ADD-ON MODULE,990/10	
0003	REF	EA		0948958-9901	TEST PROCEDURE,MEM ADD-ON MODULE,990/10	
0004	REF	EA		0948959-9901	SPECIFICATION, MEM ADD-ON MODULE,990/10	
0010	00001.000	EA		2261987-0001	ROM,ADDRESS DECODE,16KR MEMORY EXPANSION	
0010A					U602	
0011	00001.000	EA		0972787-0004	NETWORK SN74LS368N	
0011A					U23	
0012	00001.000	EA		0996420-0001	IC, SN74LS373N	001295-SN74LS373N
0012A					U401	
0014	00176.000	EA		0996680-0801	IC, 16K RAM, (SEL)	001295-TMS4116/ZA0727
0014A					UA0 THRU UA21	
0014B					UB0 THRU UB21	
0014C					UC0 THRU UC21	
0014D					UD0 THRU UD21	
0014E					UE0 THRU UE21	
0014F					UF0 THRU UF21	
0014G					UG0 THRU UG21	
0014H					UH0 THRU UH21	
0015	00176.000	EA		2210188-0003	SOCKET,LOW PROFILE,DIP,16 CONT	003612-DIL816P-108
0015A					XUA0 THRU XUA21	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: MEMORY ADD-ON MODULE,256KB,990/16KR

PYD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0948955-0004 REV R

T.I. 12649

TEXAS INSTRUMENTS INCORPORATED — DATE 10/18/79 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM0948955-0004 REV R

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0015B					XUB0 THRU XUB21	
0015C					XUC0 THRU XUC21	
0015D					XUD0 THRU XUD21	
0015E					XUE0 THRU XUE21	
0015F					XUF0 THRU XUF21	
0015G					XUG0 THRU XUG21	
0015H					XUH0 THRU XUH21	
0021	00003.000	EA		0972924-0014	CAP FIX TANT SOLID 15 MFD 10 % 20 VOLT	QPL -M39003/1-2289
0021A					C191 C193 C201	
0022	00005.000	EA		0972924-0006	CAP FIX TANT SOLID 39 MFD 10 % 10 VOLT	QPL -M39003/1-2259
0022A					C190 C192 C194 C195 C196	
0023	00011.000	EA		0972763-0009	CAP,FIXED .0047MF 50 VOLTS	004222-MC105E472Z
0023A					C177 C178 C179 C180 C185	
0023B					C199 C202 C203 C204 C205	
0023C					C206	
0024	00001.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0024A					C197	
0025	00002.000	EA		0972958-0002	TRANSISTOR,2N2907A PNP GEN PURP SW TO-18	TI - 2N2907A
0025A					Q1 Q2	
0027	00001.000	EA		0972547-0008	SWITCH, SLIDE-SPST,DIP 8 SWITCHES	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: MEMORY ADD-ON MODULE,256KB,990/16KR

PYD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0948955-0004 REV R

T.I. 12649

TEXAS INSTRUMENTS INCORPORATED — DATE 10/18/79 — LIST OF MATERIAL — PAGE 3 of — PART NUMBER LM0948955-0004 REV R

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0027A					U601	
0028	00002.000	EA		0972537-0001	DIODE,LED 550-0103 50 MA 3 V	DIA --550-0103
0028A					CR1 CR2	
0029	00000.100	FT		0411400-0022	WIRE 22AWG ELETRO-TIN-PLATED,COPPER	
0030	00002.000	EA		0972137-0005	CONNECTOR,PC 50 PIN	BEI - 65483-005
0030A					P3 P4	
0031	00002.000	EA		0945239-0001	BRACKET-STIFFENER, PWB, 14IN	
0032	00002.000	EA		0944954-0001	INSULATOR, PWB, 14IN	
0033	00006.000	EA		0972684-0002	SCREW,THD FRMG,HEX WSHR HD,2-56X1/4 LG	
0034	00002.000	EA		0533844-0001	EJECTOR, NYLON, NON-LOCKING, PWB	
0036	00001.000	EA		2210188-0805	SOCKET, LOW PROFILE, DIP, 20 PINS	003612-DIL820P-108
0036A					XU602	
0037	00001.000	EA		0972057-0001	TRANSISTOR-AST2222 NPN SILICON	TI- -AST2222
0037A					Q3	
0038	00002.000	EA		0972946-0001	RES FIX 4.7K OHM 5 % .25 W CARBON FILM	ROH - R-25
0038A					R7 R8	
0039	00001.000	EA		0539468-0002	DIODE,1N4002 LAMP 100PIV RECTIFIER	TI - IN4002
0039A					CR3	
0040	00001.000	EA		0948955-5004	AUTO-INSERTED PARTS LIST FOR 948955-0004	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: MEMORY ADD-ON MODULE,256KB,990/16KR

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0948955-0004 REV R

TI 13849

TEXAS INSTRUMENTS INCORPORATED

DATE 10/18/79 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM0948955-5004 — REV R

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0948956-0001	PWB,MEMORY ADD-ON MODULE,990/10	
0005	00001.000	EA		0219402-7404	NETWORK SN74S04N	
0005A					U3	
0006	00001.000	EA		0222222-7430	NETWORK SN7430N	-SN7430N
0006A					U301	
0007	00001.000	EA		0972900-7474	NETWORK SN74LS74N	
0007A					U2	
0008	00002.000	EA		0996136-0002	IC,SN74LS258N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS258N
0008A					U802 U803	
0009	00002.000	EA		0972652-0001	NETWORK SN74LS283N	
0009A					U701 U702	
0011	00012.000	EA		0972787-0004	NETWORK SN74LS368N	
0011A					U4 U5 U7 U8 U11 U12 U15 U16	
0011B					U19 U20 U24 U25	
0013	00013.000	EA		0972583-0001	NETWORK,SN75365	TI- -SN75365
0013A					U104 U204 U304 U404 U504	
0013B					U604 U704 U804 U6 U103 U303	
0013C					U503 U703	
0016	00001.000	EA		0972037-3470	RES. NETWORK,4.7K OHM 2%	
0016A					U402	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 948955-0004

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0948955-5004 REV R

T.I. 13849

TEXAS INSTRUMENTS INCORPORATED

DATE 10/18/79 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM0948955-5004 — REV R

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0017	00001.000	EA		0972037-2680	NETWORK RESISTOR 680 OHMS 2%	073138-898-3-R680
0017A					U801	
0018	00010.000	EA		0972037-1220	NETWORK,RES 16 PIN,8 ELEMENT 22 OHMS +2%	073138-898-3-R22
0018A					U105 U205 U305 U405 U505	
0018B					U605 U705 U805 U203 U603	
0019	00004.000	EA		0972946-0049	RES FIX 220 OHM 5 % .25 W CARBON FILM	ROH - R-25
0019A					R1 R2 R3 R6	
0020	00002.000	EA		0972946-0065	RES FIX 1.0K OHM 5% .25 W CARBON FILM	ROH - R-25
0020A					R4 R5	
0021	00043.000	EA		0972924-0014	CAP FIX TANT SOLID 15 MFD 10 % 20 VOLT	QPL -M39003/1-2289
0021A					C121 THRU C137	
0021B					C139 THRU C160	
0021C					C164 C168 C172 C176	
0024	00141.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0024A					C1 THRU C120 C161 THRU C163	
0024B					C165 THRU C167	
0024C					C169 THRU C171	
0024D					C173 THRU C175	
0024E					C181 THRU C184	
0024F					C186 THRU C189 C198	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 948955-0004

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0948955-5004 REV R

T.I. 13849

NØTES: UNLESS ØTHERWISE SPECIFIED;

1. ALL DEVICE TYPES ARE PREFIXED WITH SN74.
2. GRØUND IS APPLIED TØ PIN 7 ØF ALL 14-PIN IC'S AND PIN 8 ØF ALL 16-PIN IC's.
3. VCC IS APPLIED TØ PIN 14 ØF ALL 14-PIN IC'S AND PIN 16 ØF ALL 16-PIN IC's.
4. DEVICE TYPE, PIN NUMBERS, AND REFERENCE DESIGNATØR ØF IC IS SHØWN AS FØLLØWS:

00 AND 04 = DEVICE TYPE
4,5 AND 6 = PIN NUMBERS
U8 AND U14 = REFERENCE DESIGNATØR

5. * INDICATES DEVICES PØWERED BY +5 SW.

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	CN428577 (D)	6-7-78	
	B	CN437777 (C) [illegible] (1) SH. 4 ALL 74365 PKGS PIN 9 WAS TIED TO +5V SW (2) IN ZONE D2 WAS SH. 6,7,8,9,10	2-7-79	
	C	CN433565 (C)	11-1-79	

REV STATUS OF SHEETS											
REV	E	B	C	B							
SHEET	1	2	3	4	5	6	7	8	9	10	11

QTY REQD -2	QTY REQD -1	ITEM NO	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIR
- DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING
- IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY
- INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100

HOLE TOLERANCE

.013 THRU .125 +.004 −.001	.126 THRU .250 +.006 −.001	.250 THRU .500 +.006 −.001
.501 THRU .750 +.008 −.001	.750 THRU 1.000 +.010 −.001	1.001 THRU 2.000 +.012 −.001

NEXT ASSY	USED ON
[illegible]	[illegible]

APPLICATION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES ANGLES ±1° 3 PLACE DECIMALS ±.010 2 PLACE DECIMALS ±.02

MATERIAL:

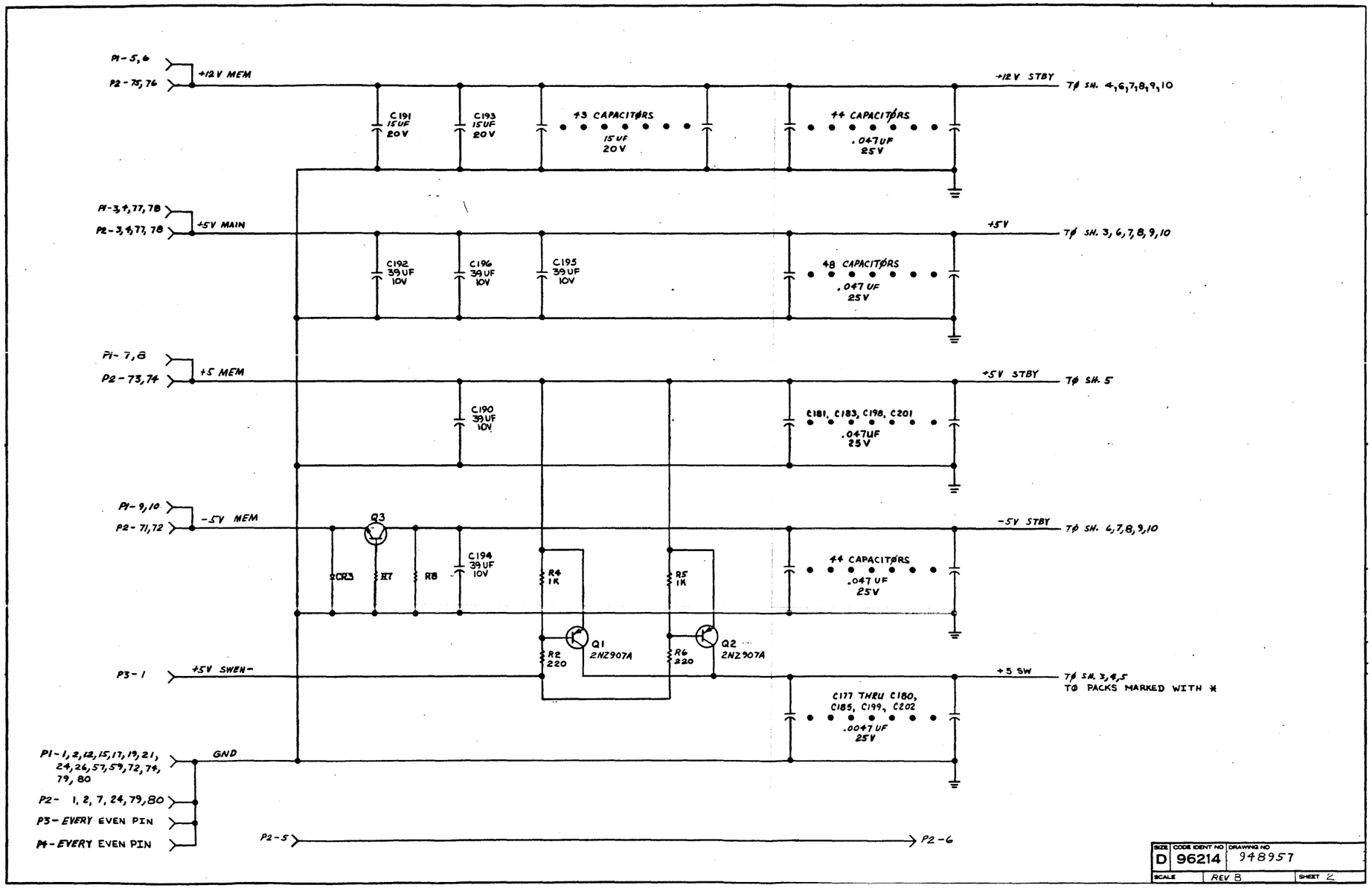
		DATE
DWN		12/8/76
CHK	[illegible]	12-13-76
ENGR		11-29-77
QA		12/1/77
APVD		11-29-77
CONTR NO		
DESIGN ACTIVITY RELEASE		[illegible]

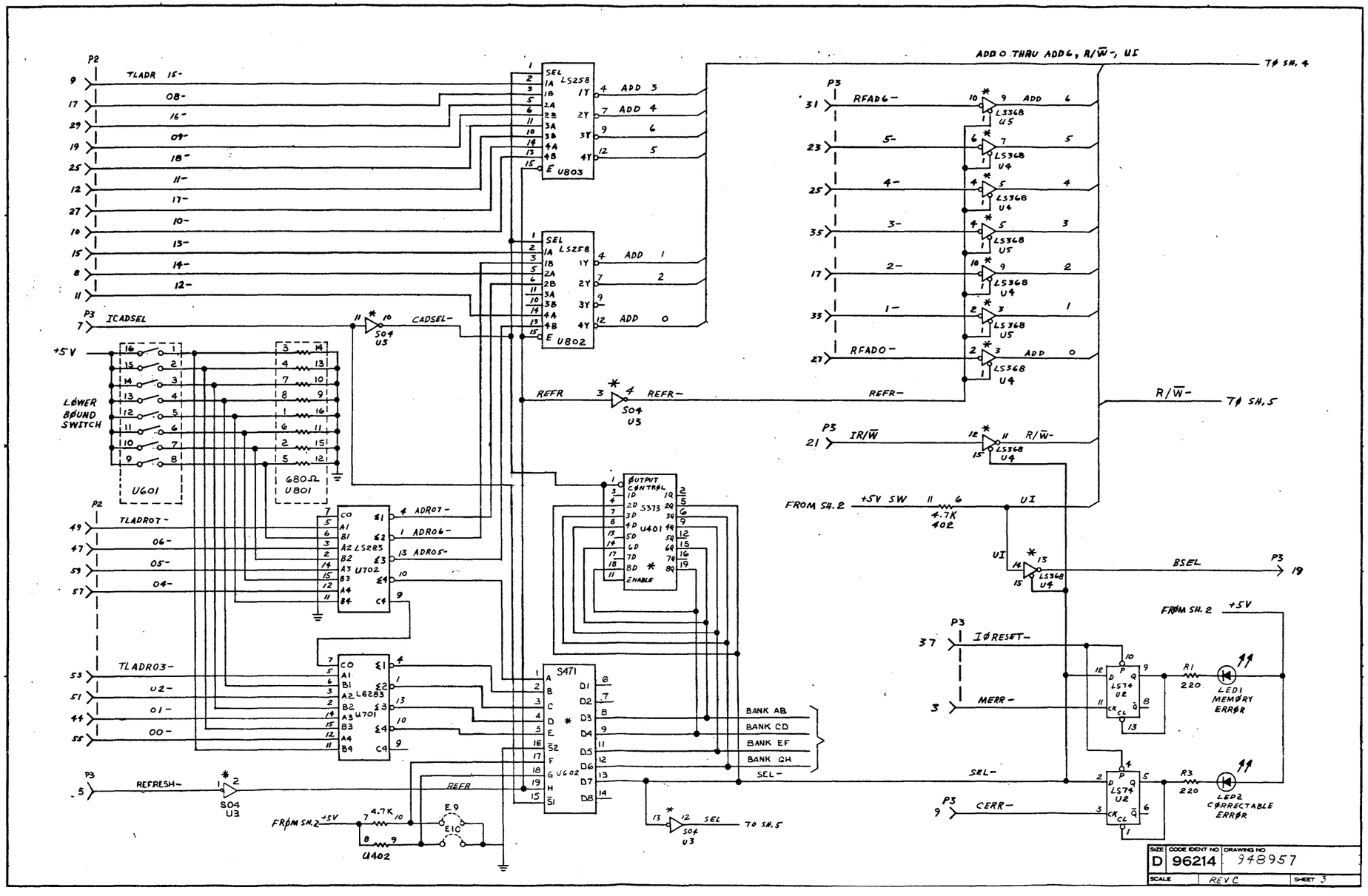
TEXAS INSTRUMENTS INCORPORATED Equipment Group Dallas, Texas

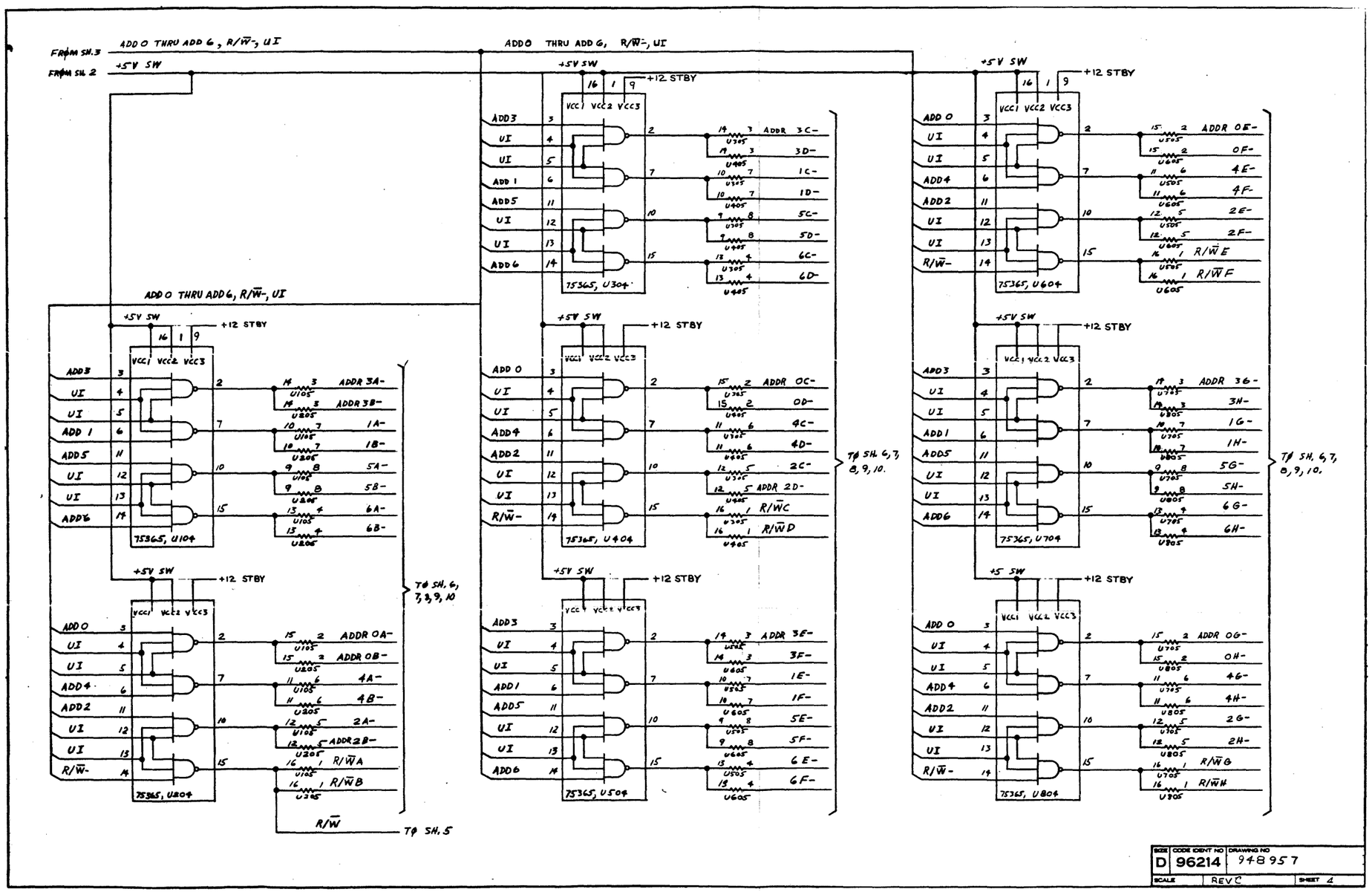
LOGIC DIAGRAM MEMORY ADD-ON MODULE 128K, 990/10

SIZE	CODE IDENT NO	DRAWING NO
D	96214	948957

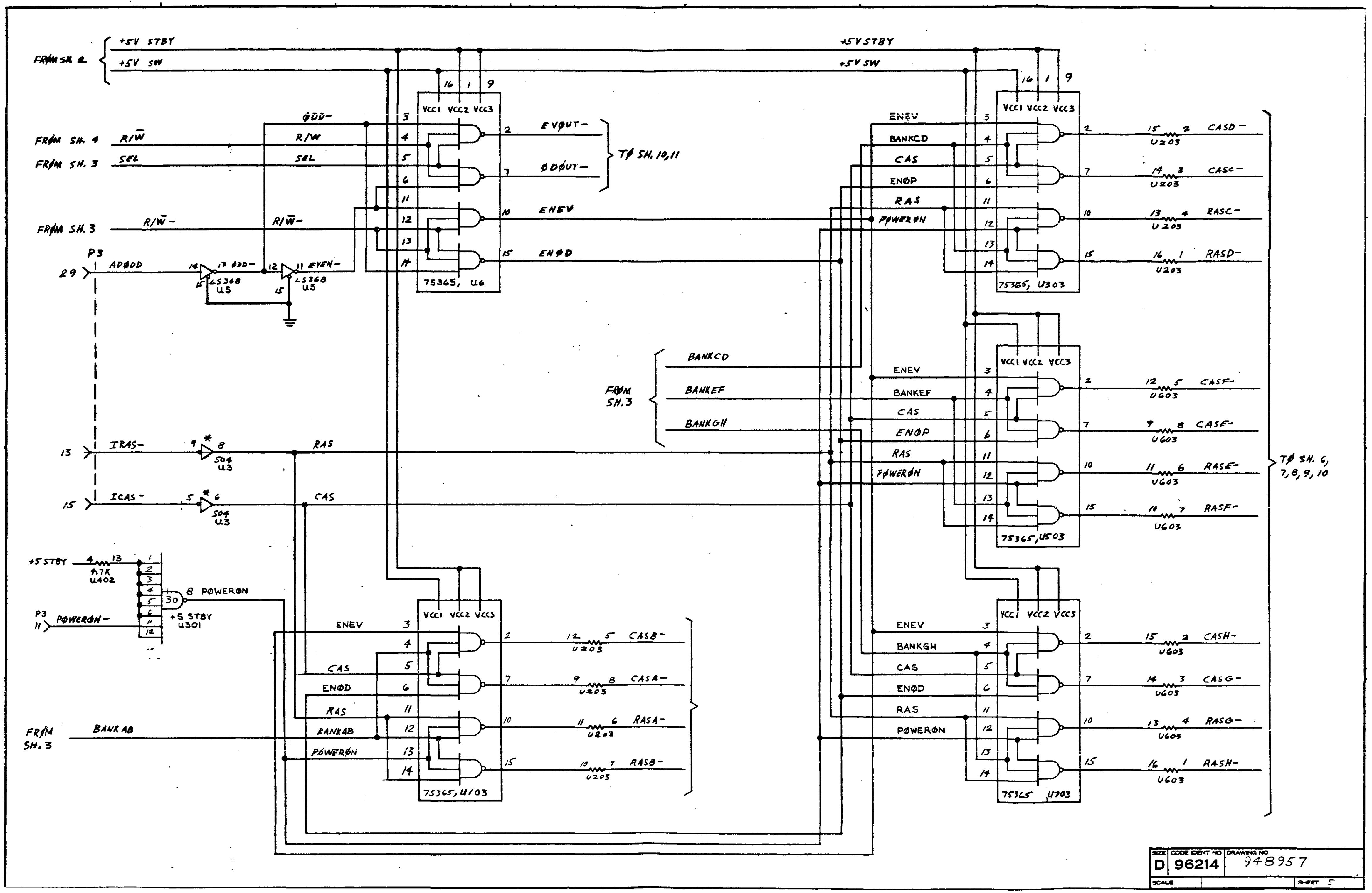
SCALE NONE REV C SHEET 1 OF 11

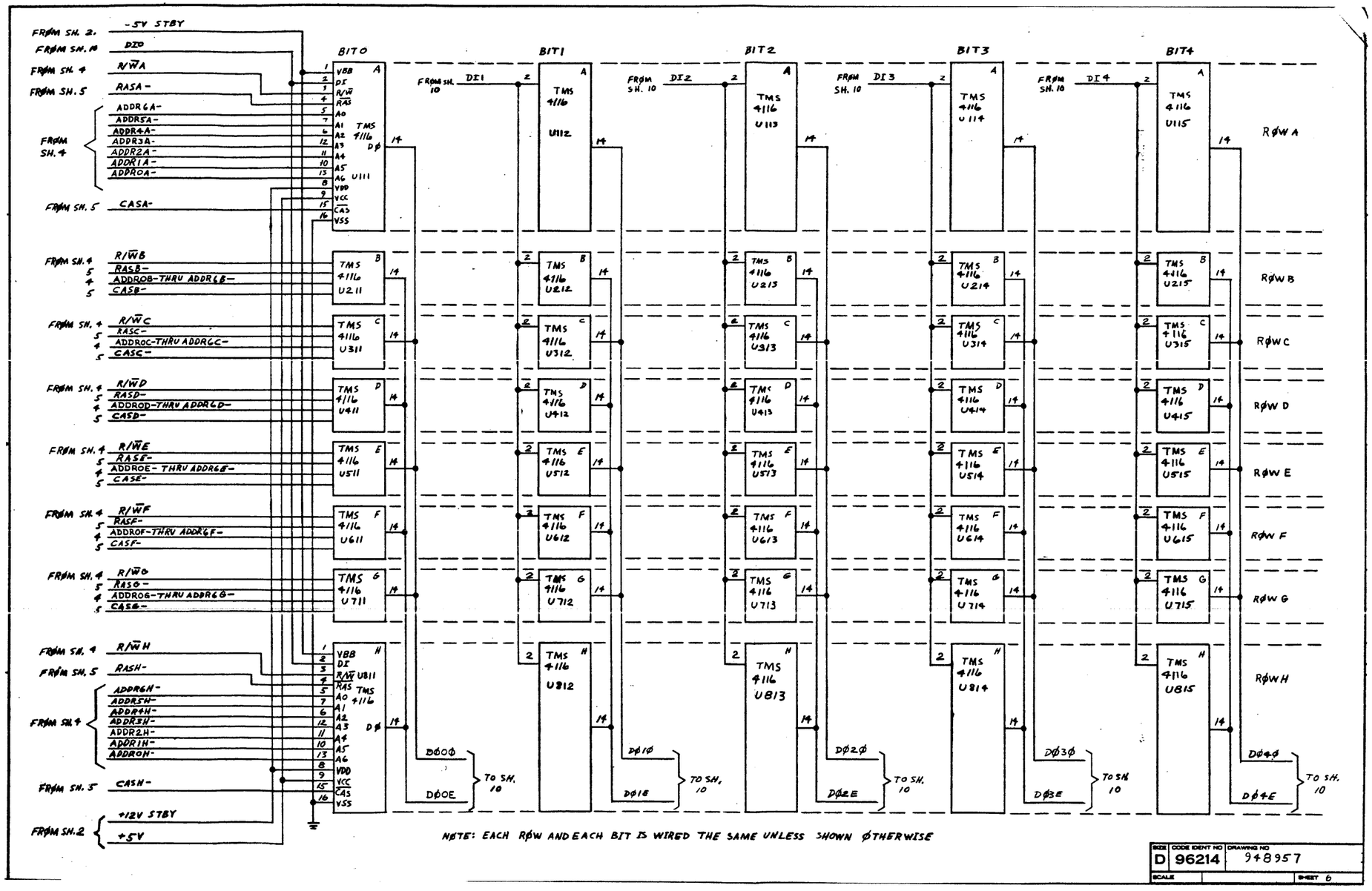

P1-5,6
P2-75,76
+12V MEM
C191 15UF 20V
C193 15UF 20V
13 CAPACITORS 15UF 20V
14 CAPACITORS .047UF 25V
+12V STBY
TØ SH. 4,6,7,8,9,10
P1-3,4,77,78
P2-3,4,77,78
+5V MAIN
C192 39UF 10V
C196 39UF 10V
C195 39UF 10V
48 CAPACITORS .047 UF 25V
+5V
TØ SH. 3,6,7,8,9,10
P1-7,8
P2-73,74
+5 MEM
C190 39UF 10V
C181, C183, C198, C201 .047UF 25V
+5V STBY
TØ SH. 5
P1-9,10
P2-71,72
-5V MEM
Q3
CR3
R7
R8
C194 39UF 10V
R4 1K
R5 1K
11 CAPACITORS .047 UF 25V
-5V STBY
TØ SH. 6,7,8,9,10
Q1 2N2907A
Q2 2N2907A
R2 220
R6 220
P3-1
+5V SWEN-
+5 SW
TØ SH. 3,4,5
TØ PACKS MARKED WITH *
C177 THRU C180, C185, C199, C202 .0047 UF 25V
P1-1,2,12,15,17,19,21,24,26,57,59,72,74,79,80
GND
P2- 1,2,7,24,79,80
P3-EVERY EVEN PIN
P4-EVERY EVEN PIN
P2-5
P2-6
SIZE D
CODE IDENT NO 96214
DRAWING NO 948957
SCALE
REV B
SHEET 2

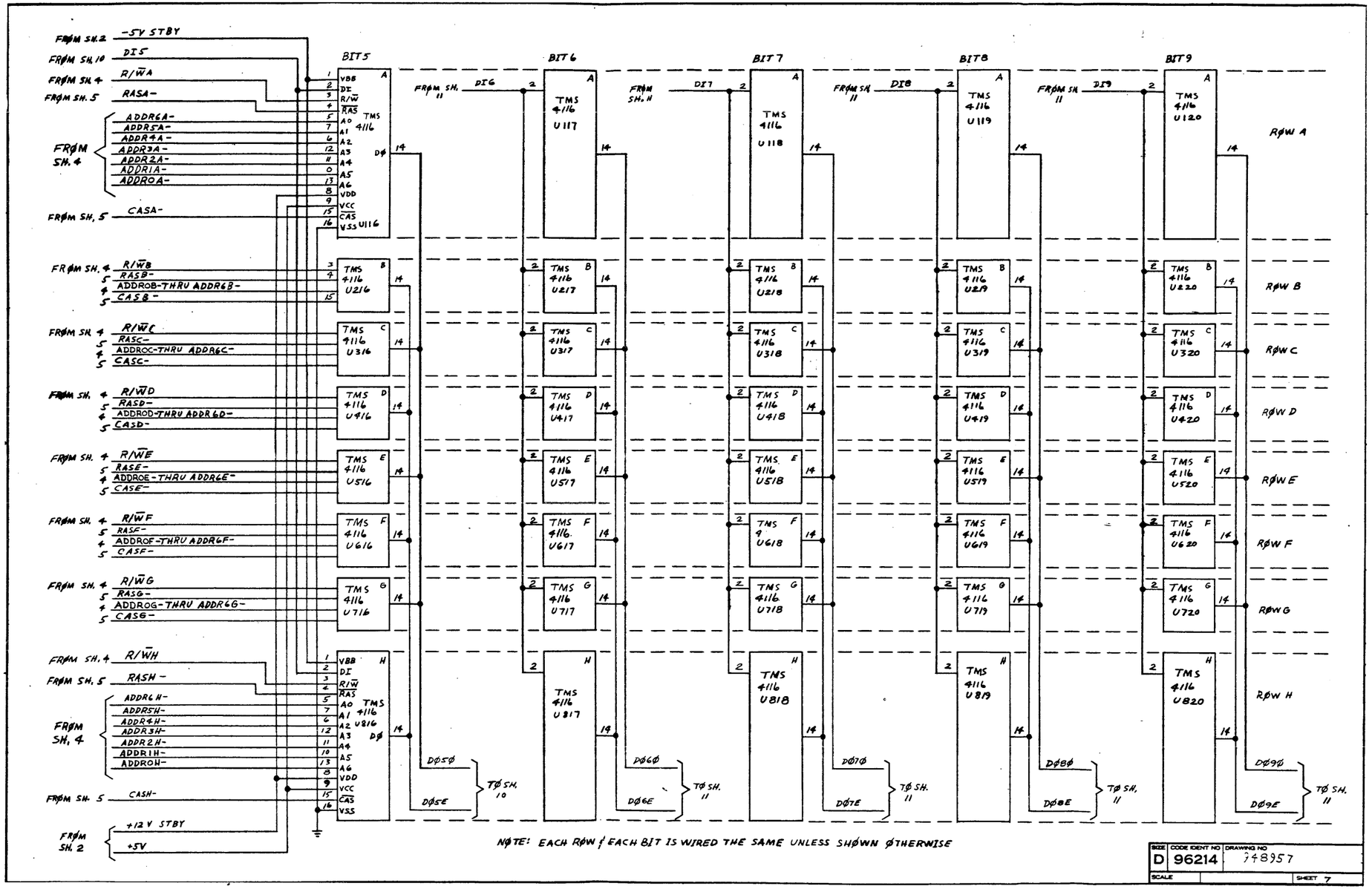

P2
TLADR 15-
08-
16-
09-
18-
11-
17-
10-
13-
14-
12-
P3
ICADSEL
CADSEL-
S04 U3
+5 V
LOWER BOUND SWITCH
U601
680Ω U801
TLADR07-
06-
05-
04-
TLADR03-
02-
01-
00-
U702
U701
LS283
REFRESH-
REFR
REFR-
FROM SH.2 +5V
4.7K
E.9
E.10
U402
SEL
LS258
U803
U802
ADD 3
ADD 4
6
5
ADD 1
2
ADD 0
S471
U602
BANK AB
BANK CD
BANK EF
BANK GH
SEL-
TO SH.5
OUTPUT CONTROL
LS373
U401
ENABLE
ADD0 THRU ADD6, R/W-, UI
TO SH. 4
RFAD6-
5-
4-
3-
2-
1-
RFAD0-
ADD
LS368
U5
U4
R/W-
TO SH,5
IR/W
FROM SH.2 +5V SW
4.7K
402
UI
BSEL
FROM SH. 2 +5V
IØRESET-
MERR-
CERR-
SEL-
LS74
U2
R1
R3
220
LED1 MEMORY ERROR
LED2 CORRECTABLE ERROR
SIZE D
CODE IDENT NO 96214
DRAWING NO 948957
SCALE
REV C
SHEET 3

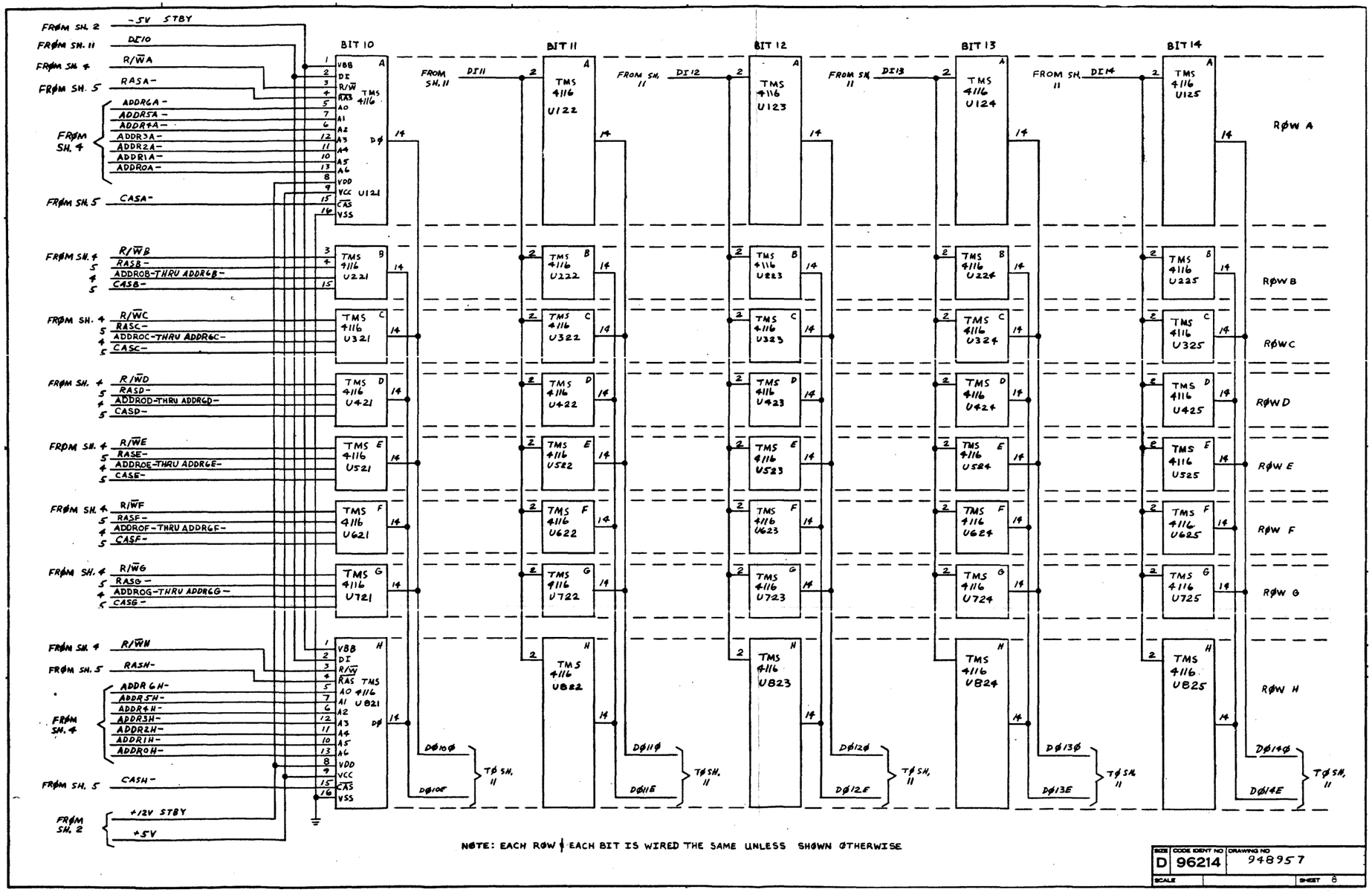


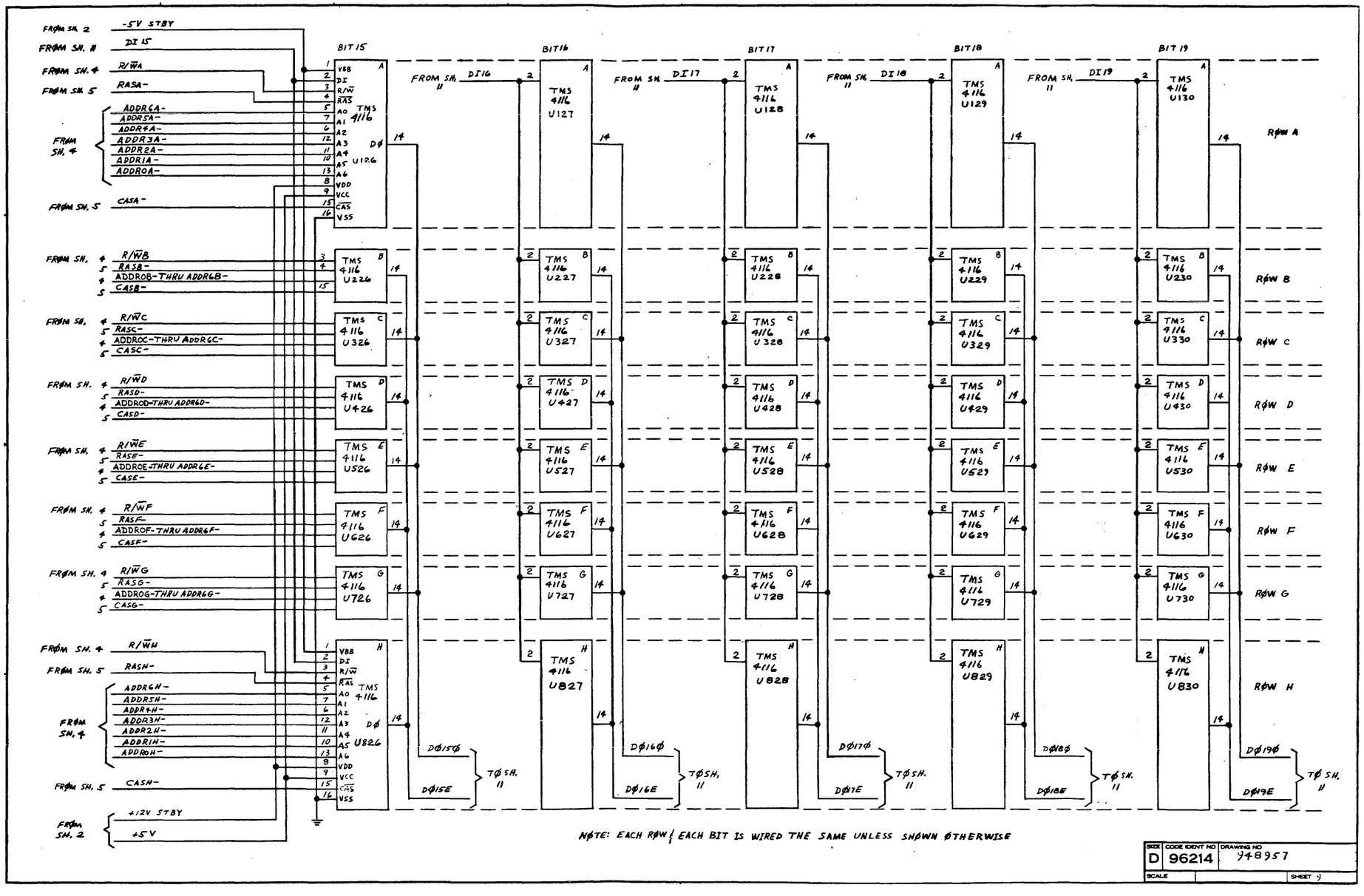
SIZE	CODE IDENT NO	DRAWING NO
D	96214	948957
SCALE	REV C	SHEET 4


FROM SH. 2
+5V STBY
+5V SW
FROM SH. 4 R/W
FROM SH. 3 SEL
FROM SH. 3 R/W-
P3
29 ADØDD
13 IRAS-
15 ICAS-
ØDD-
R/W
SEL
R/W-
EVEN-
LS368 U5
S04 U3
RAS
CAS
75365, U6
EVØUT-
ØDØUT-
TØ SH. 10,11
ENEV
ENØD
+5 STBY
4.7K U402
8 POWERON
+5 STBY U301
P3 11 PØWERØN-
FROM SH. 3 BANKAB
ENEV
CAS
ENØD
RAS
BANKAB
PØWERØN
75365, U103
CASB-
CASA-
RASA-
RASB-
U203
FROM SH. 3
BANKCD
BANKEF
BANKGH
ENEV
BANKCD
CAS
ENØP
RAS
PØWERØN
75365, U303
CASD-
CASC-
RASC-
RASD-
ENEV
BANKEF
CAS
ENØP
RAS
PØWERØN
75365, U503
CASF-
CASE-
RASE-
RASF-
U603
ENEV
BANKGH
CAS
ENØD
RAS
PØWERØN
75365 U703
CASH-
CASG-
RASG-
RASH-
TØ SH. 6, 7, 8, 9, 10
VCC1 VCC2 VCC3
D 96214 948957
SCALE
SHEET 5


BIT0
BIT1
BIT2
BIT3
BIT4
FROM SH. 2. -5V STBY
FROM SH. 10 DI0
FROM SH. 4 R/W A
FROM SH. 5 RASA-
FROM SH. 4 ADDR6A-
ADDR5A-
ADDR4A-
ADDR3A-
ADDR2A-
ADDR1A-
ADDR0A-
FROM SH. 5 CASA-
FROM SH. 4 R/W B
RASB-
ADDR08-THRU ADDR6B-
CASB-
FROM SH. 4 R/W C
RASC-
ADDR0C-THRU ADDR6C-
CASC-
FROM SH. 4 R/W D
RASD-
ADDR0D-THRU ADDR6D-
CASD-
FROM SH. 4 R/W E
RASE-
ADDR0E- THRU ADDR6E-
CASE-
FROM SH. 4 R/W F
RASF-
ADDR0F-THRU ADDR6F-
CASF-
FROM SH. 4 R/W G
RASG-
ADDR0G-THRU ADDR6G-
CASG-
FROM SH. 4 R/W H
FROM SH. 5 RASH-
FROM SH. 4 ADDR6H-
ADDR5H-
ADDR4H-
ADDR3H-
ADDR2H-
ADDR1H-
ADDR0H-
FROM SH. 5 CASH-
FROM SH. 2 +12V STBY
+5V
FROM SH. 10 DI1
FROM SH. 10 DI2
FROM SH. 10 DI3
FROM SH. 10 DI4
R/W A
R/W B
R/W C
R/W D
R/W E
R/W F
R/W G
R/W H
D00Ø
D00E
D01Ø
D01E
D02Ø
D02E
D03Ø
D03E
D04Ø
D04E
TO SH. 10
NOTE: EACH ROW AND EACH BIT IS WIRED THE SAME UNLESS SHOWN ØTHERWISE
SIZE D
CODE IDENT NO 96214
DRAWING NO 948957
SCALE
SHEET 6

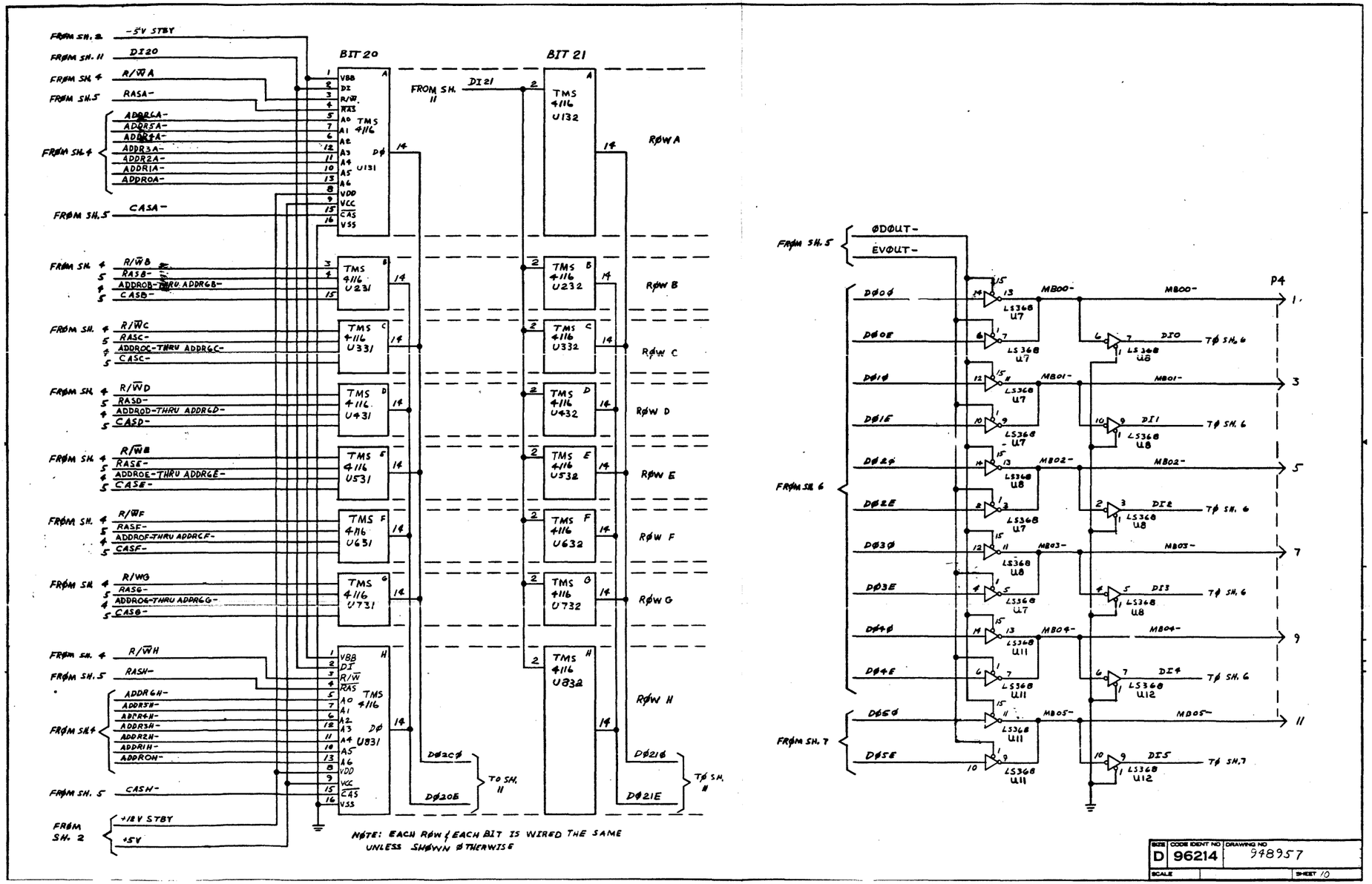

FROM SH.2 -5V STBY
FROM SH.10 DIS
FROM SH.4 R/W A
FROM SH.5 RASA-
FROM SH.4 ADDR6A-
ADDR5A-
ADDR4A-
ADDR3A-
ADDR2A-
ADDR1A-
ADDR0A-
FROM SH. 4
FROM SH, 5 CASA-
BIT5
BIT6
BIT7
BIT8
BIT9
TMS 4116 U116
TMS 4116 U117
TMS 4116 U118
TMS 4116 U119
TMS 4116 U120
FROM SH. 11 DI6
FROM SH. 11 DI7
FROM SH. 11 DI8
FROM SH. 11 DI9
FROM SH. 4 R/W B
5 RASB-
4 ADDR0B-THRU ADDR6B-
5 CASB-
TMS 4116 U216
TMS 4116 U217
TMS 4116 U218
TMS 4116 U219
TMS 4116 U220
RØW B
FROM SH. 4 R/W C
5 RASC-
4 ADDR0C-THRU ADDR6C-
5 CASC-
TMS 4116 U316
TMS 4116 U317
TMS 4116 U318
TMS 4116 U319
TMS 4116 U320
RØW C
FROM SH. 4 R/W D
5 RASD-
4 ADDR0D-THRU ADDR6D-
5 CASD-
TMS 4116 U416
TMS 4116 U417
TMS 4116 U418
TMS 4116 U419
TMS 4116 U420
RØW D
FROM SH. 4 R/W E
5 RASE-
4 ADDR0E-THRU ADDR6E-
5 CASE-
TMS 4116 U516
TMS 4116 U517
TMS 4116 U518
TMS 4116 U519
TMS 4116 U520
RØW E
FROM SH. 4 R/W F
5 RASF-
4 ADDR0F-THRU ADDR6F-
5 CASF-
TMS 4116 U616
TMS 4116 U617
TMS 4116 U618
TMS 4116 U619
TMS 4116 U620
RØW F
FROM SH. 4 R/W G
5 RASG-
4 ADDR0G-THRU ADDR6G-
5 CASG-
TMS 4116 U716
TMS 4116 U717
TMS 4116 U718
TMS 4116 U719
TMS 4116 U720
RØW G
FROM SH. 4 R/W H
FROM SH. 5 RASH-
FROM SH. 4
ADDR6H-
ADDR5H-
ADDR4H-
ADDR3H-
ADDR2H-
ADDR1H-
ADDR0H-
TMS 4116 U816
TMS 4116 U817
TMS 4116 U818
TMS 4116 U819
TMS 4116 U820
RØW H
FROM SH. 5 CASH-
FROM SH. 2 +12 V STBY
+5V
DØ5Ø
DØ5E
TØ SH. 10
DØ6Ø
DØ6E
DØ7Ø
DØ7E
DØ8Ø
DØ8E
DØ9Ø
DØ9E
TØ SH. 11
NØTE: EACH RØW / EACH BIT IS WIRED THE SAME UNLESS SHØWN ØTHERWISE
SIZE D
CODE IDENT NO 96214
DRAWING NO 748957
SCALE
SHEET 7

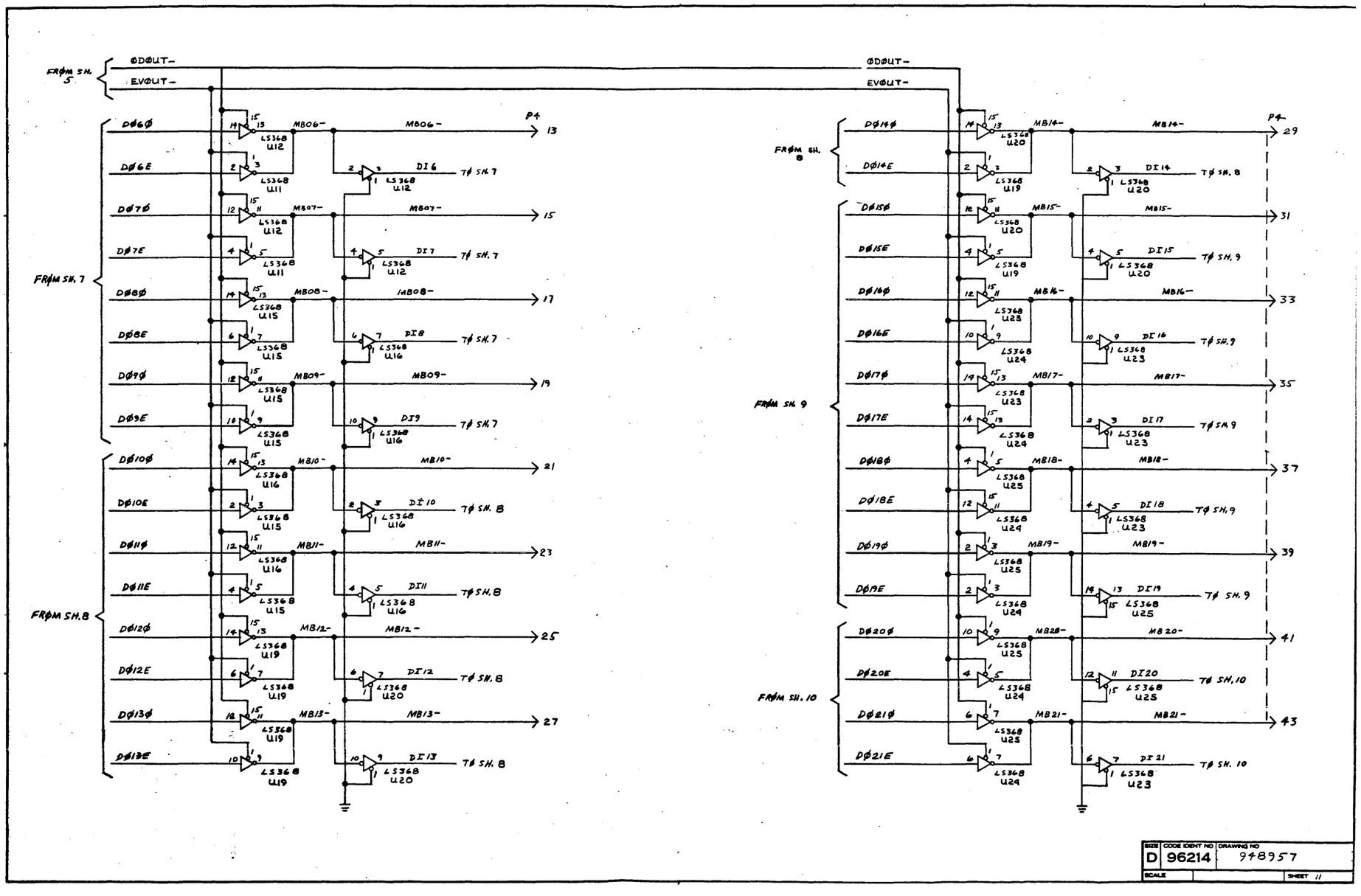

BIT 10
BIT 11
BIT 12
BIT 13
BIT 14
FROM SH. 2 -5V STBY
FROM SH. 11 DI10
FROM SH. 4 R/W A
FROM SH. 5 RASA-
FROM SH. 4 ADDR6A-
ADDR5A-
ADDR4A-
ADDR3A-
ADDR2A-
ADDR1A-
ADDR0A-
FROM SH. 5 CASA-
FROM SH. 4 R/W B
RASB-
ADDR0B-THRU ADDR6B-
CASB-
FROM SH. 4 R/W C
RASC-
ADDR0C-THRU ADDR6C-
CASC-
FROM SH. 4 R/W D
RASD-
ADDR0D-THRU ADDR6D-
CASD-
FROM SH. 4 R/W E
RASE-
ADDR0E-THRU ADDR6E-
CASE-
FROM SH. 4 R/W F
RASF-
ADDR0F-THRU ADDR6F-
CASF-
FROM SH. 4 R/W G
RASG-
ADDR0G-THRU ADDR6G-
CASG-
FROM SH. 4 R/W H
FROM SH. 5 RASH-
ADDR6H-
ADDR5H-
ADDR4H-
ADDR3H-
ADDR2H-
ADDR1H-
ADDR0H-
FROM SH. 5 CASH-
FROM SH. 2 +12V STBY
+5V
FROM SH. 11 DI11
FROM SH. 11 DI12
FROM SH. 11 DI13
FROM SH. 11 DI14
TMS 4116 U121
TMS 4116 U122
TMS 4116 U123
TMS 4116 U124
TMS 4116 U125
TMS 4116 U221
TMS 4116 U222
TMS 4116 U223
TMS 4116 U224
TMS 4116 U225
TMS 4116 U321
TMS 4116 U322
TMS 4116 U323
TMS 4116 U324
TMS 4116 U325
TMS 4116 U421
TMS 4116 U422
TMS 4116 U423
TMS 4116 U424
TMS 4116 U425
TMS 4116 U521
TMS 4116 U522
TMS 4116 U523
TMS 4116 U524
TMS 4116 U525
TMS 4116 U621
TMS 4116 U622
TMS 4116 U623
TMS 4116 U624
TMS 4116 U625
TMS 4116 U721
TMS 4116 U722
TMS 4116 U723
TMS 4116 U724
TMS 4116 U725
TMS 4116 U821
TMS 4116 U822
TMS 4116 U823
TMS 4116 U824
TMS 4116 U825
ROW A
ROW B
ROW C
ROW D
ROW E
ROW F
ROW G
ROW H
DØ10Ø
DØ10E
DØ11Ø
DØ11E
DØ12Ø
DØ12E
DØ13Ø
DØ13E
DØ14Ø
DØ14E
TØ SH. 11
NOTE: EACH ROW & EACH BIT IS WIRED THE SAME UNLESS SHOWN OTHERWISE
SIZE D
CODE IDENT NO 96214
DRAWING NO 948957
SCALE
SHEET 6



NØTE: EACH RØW / EACH BIT IS WIRED THE SAME UNLESS SHØWN ØTHERWISE

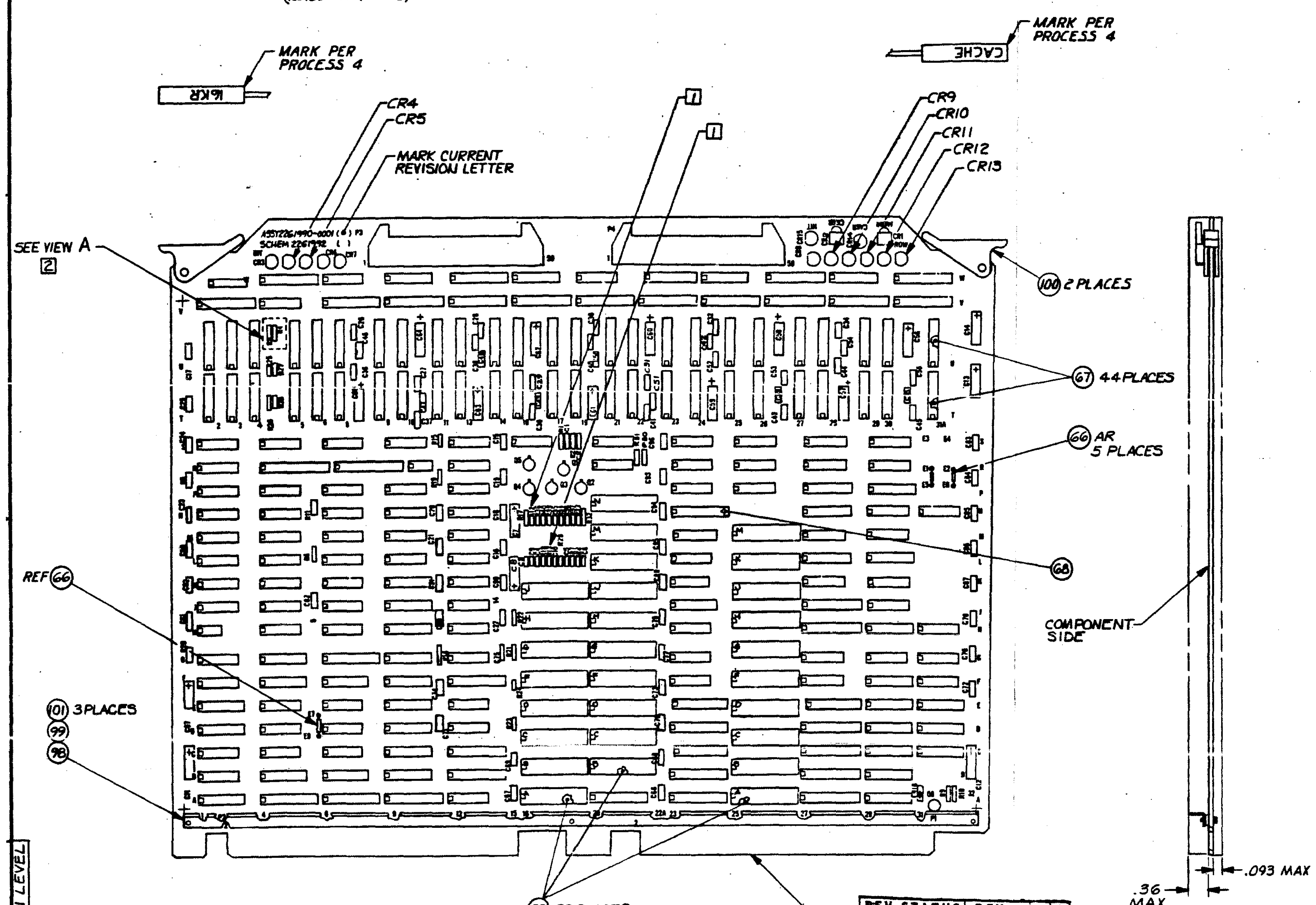
SIZE	CODE IDENT NO	DRAWING NO
D	96214	948957
SCALE		SHEET 9

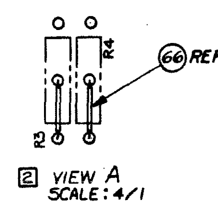

BIT 20
BIT 21
FROM SH. 2 -5V STBY
FROM SH. 11 DI20
FROM SH. 4 R/W A
FROM SH. 5 RASA-
FROM SH. 4 ADDR8A- ADDR7A- ADDR6A- ADDR5A- ADDR4A- ADDR3A- ADDR2A- ADDR1A- ADDR0A-
FROM SH. 5 CASA-
FROM SH. 11 DI21
TMS 4116 U131
TMS 4116 U132
RØW A
FROM SH. 4 R/W B RASB- ADDR0B-THRU ADDR6B- CASB-
TMS 4116 U231
TMS 4116 U232
RØW B
FROM SH. 4 R/W C RASC- ADDR0C-THRU ADDR6C- CASC-
TMS 4116 U331
TMS 4116 U332
RØW C
FROM SH. 4 R/W D RASD- ADDR0D-THRU ADDR6D- CASD-
TMS 4116 U431
TMS 4116 U432
RØW D
FROM SH. 4 R/W E RASE- ADDR0E-THRU ADDR6E- CASE-
TMS 4116 U531
TMS 4116 U532
RØW E
FROM SH. 4 R/W F RASF- ADDR0F-THRU ADDR6F- CASF-
TMS 4116 U631
TMS 4116 U632
RØW F
FROM SH. 4 R/W G RASG- ADDR0G-THRU ADDR6G- CASG-
TMS 4116 U731
TMS 4116 U732
RØW G
FROM SH. 4 R/W H RASH- ADDR6H- ADDR5H- ADDR4H- ADDR3H- ADDR2H- ADDR1H- ADDR0H-
FROM SH. 5 CASH-
TMS 4116 U831
TMS 4116 U832
RØW H
FROM SH. 2 +12V STBY +5V
DØ2CØ DØ2DE TO SH. 11
DØ216 DØ21E TØ SH. 11
NØTE: EACH RØW / EACH BIT IS WIRED THE SAME UNLESS SHØWN ØTHERWISE
FROM SH. 5 ØDØUT- EVØUT-
FROM SH. 6
FROM SH. 7
LS368 U7
LS368 U8
LS368 U11
LS368 U12
MB00- MB01- MB02- MB03- MB04- MB05-
P4
TØ SH. 6
TØ SH. 7
SIZE D CODE IDENT NO 96214 DRAWING NO 948957
SCALE SHEET 10


FROM SH. 5
ØDØUT-
EVØUT-
FRØM SH. 7
DØ6Ø
DØ6E
DØ7Ø
DØ7E
DØ8Ø
DØ8E
DØ9Ø
DØ9E
DØ1Ø Ø
DØ1ØE
DØ11Ø
DØ11E
FRØM SH. 8
DØ12Ø
DØ12E
DØ13Ø
DØ13E
LS368 U12
LS368 U11
LS368 U15
LS368 U16
LS368 U19
LS368 U20
MB06-
MB07-
MB08-
MB09-
MB10-
MB11-
MB12-
MB13-
P4
13
15
17
19
21
23
25
27
DI6
DI7
DI8
DI9
DI10
DI11
DI12
DI13
T/ SH. 7
T/ SH. 8
FRØM SH. 8
DØ14Ø
DØ14E
DØ15Ø
DØ15E
DØ16Ø
DØ16E
DØ17Ø
DØ17E
FRØM SH. 9
DØ18Ø
DØ18E
DØ19Ø
DØ19E
DØ20Ø
DØ20E
FRØM SH. 10
DØ21Ø
DØ21E
LS368 U20
LS368 U19
LS368 U23
LS368 U24
LS368 U25
MB14-
MB15-
MB16-
MB17-
MB18-
MB19-
MB20-
MB21-
29
31
33
35
37
39
41
43
DI14
DI15
DI16
DI17
DI18
DI19
DI20
DI21
T/ SH. 8
T/ SH. 9
T/ SH. 10
SIZE D
CODE IDENT NO 96214
DRAWING NO 948957
SCALE
SHEET 11

NOTES: UNLESS OTHERWISE SPECIFIED:

1. R12 AND R13 ARE NOT INSTALLED
2. R3 AND R4 ARE NOT INSTALLED. SEE VIEW A FOR JUMPER INSTALLATION. (NOTES CONT. SH.2)





2 VIEW A
SCALE: 4/1

REV	DESCRIPTION	DATE	APPROVED
A	CN452023 (C) (1) ITEM 32 ON -1 LM QTY WAS 2 AND ITEM 80 WAS -0545 (2) ITEM 71 QTY WAS 4 AND ADDED ITEM 106 (3) ADDED NOTE 5 (4) UPDATED REV LEVEL BLOCK (5) ADD SH 2	10-25-79	E. Diaz
B	CN 436502 (C) (1) ITEM 32 ON -1 LM QTY WAS 2 (2) UPDATED REV. LEVEL BLOCK	10-25-79	E. Diaz
C	CN 447609 (D) (1) UPDATED REV. LEVEL (2) ADDED PART NO. BLOCK FOR -0001 & -5001 L M (3) ADDED NOTE 4 TO SH2	10-25-79	E. Diaz
D	CN 448700 (C) (1) ADDED NOTE 5 TO SH.2 (2) CHANGED REV LEVEL BLOCK (3) CHANGED ITEM 68 ON LM TO TO XUZN23	10-25-79	E. Diaz
E	CN 453404 (C) C. Letinick (1) ON -5001 LM ITEM 15 QTY WAS 7, ITEM 43 QTY WAS 9 (2) UPDATED REV. LEVEL BLOCK	30 Nov. 79	[illegible]
F	CN 459021 (C) G Sedeholm (1) DELETED ITEMS 55 AND 56 FROM -5001 LM (2) ADDED ITEMS 55 AND 56 TO -0001 LM (3) UPDATED REV LEVEL BLOCK	1-8-80	J. R.
G	CN 450074 (B) (1) ADDED NOTE 6 (2) UPDATED REV LEVEL BLOCK	2-1-80	J. R.
H	CN 453369 (D) G Sedeholm (1) ITEM 64A ON LM WAS UWWI (2) ITEM 66 PN WAS 411400-0024 (3) ITEM 104 PN WAS 972929-0379 (4) DELETED LEADER LINES FOR R3 & R4 MARKINGS AT VIEW A (5) UPDATED REV LEVEL BLOCK	3-14-80	J. R.

REVISION LEVEL									
TEST PROCEDURE (2261993-9901)	*	*	*	*	*	*	*	*	A
LOGIC DIAG. (2261992-9901)	*	*	–	*	*	A	A	C	C
PWB (2261991-0001)	B	C	C	C	C	E	E	G	G
ASSEMBLY (2261990-0001)	*	A	B	C	D	E	F	G	H

REV STATUS OF SHEETS	REV	H	G
	SHEET	1	2

4	2261990-5001	AUTO INSERTED PARTS LIST FOR 2261990-1
	2261990-0001	CACHE MEMORY CONTROLLER
	PARTS NO.	DESCRIPTION

SEQ NO	IDENT	F-SPEC	NO	ADDITIONAL	NOTES
4	MARK	100-07	712	CLR BLACK, TYPE 6	
3	MARK	100-02	21	HGT .06, COLOR BLACK	
2	SLDR	127-01	00		
1	SLDR	124-02	00		
	PROCESS		CLASSIFICATION		

PROCESSES — FOR CORRELATION TO GOVT/IND SPECIFICATIONS. SEE TI DRAWING 729467

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION	NOTES

PARTS LIST

NEXT ASSY	USED ON
2262002	7047

APPLICATION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES: ANGLES ±1°; 3 PLACE DECIMALS ± .010; 2 PLACE DECIMALS ± .02
- INTERPRET DRAWING PER MIL-D-1000
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIM
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

.013 THRU .125: +.004 −.001	.126 THRU .250: +.005 −.001	.251 THRU .500: +.006 −.001
.501 THRU .750: +.008 −.001	.751 THRU 1.000: +.010 −.001	1.001 THRU 2.000: +.012 −.001

		DATE
DWN	[illegible]	03/28/79
CHK	[illegible]	[illegible]
ENGR		
APVD		
QA	[illegible]	6-27-79
COMPR	[illegible]	[illegible]
RLSE	Tony Barker	6-27-79

TEXAS INSTRUMENTS INCORPORATED Dallas, Texas

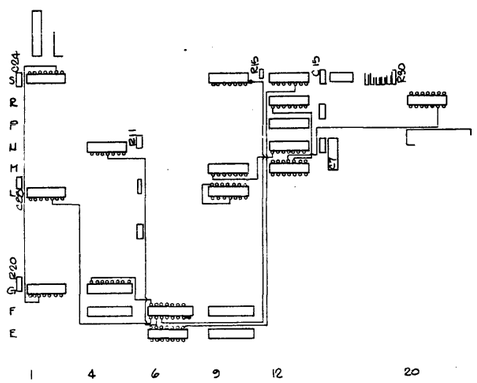
CACHE MEMORY CONTROLLER

SIZE	FSCM NO	DRAWING NO
D	96214	2261990

SCALE 1/1 SHEET 1 OF 2

NOTES (CONT.)

3. REWORK PROCEDURE FOR REV. B PWBs (22-61991):
   A. CUT UE6 PIN 9
      CUT US09 PIN 2
      CUT UG1 PIN 3
      CUT UL9 PIN 4
      CUT UM09 PIN 1
   B. ADD 74S00 AT LOCATION F-6 WITH PIN 14 CUT (INSERT PIN 1 OF I.C. INTO PIN 1 OF LOCATION).
   C. ADD WIRES BETWEEN THE FOLLOWING POINTS AS SHOWN:
      US12 PIN 5 TO UE6 PIN 9 (ON I.C.)
      UG04 PIN 16 TO UF06 PIN 14 (ON I.C.)
      UL01 PIN 5 TO UF06 PIN 1
      UJ04 PIN 4 TO UF06 PIN 2
      UF06 PIN 7 TO PIN 8 OF LOCATION F0-6 (EMPTY PAD)
      UF06 PIN 3 TO FEEDTHROUGH NEAR S9 PIN 7
      UM12 PIN 11 TO UE20 PIN 6
      UM12 PIN 10 TO UR12 PIN 1
      US01 PIN 9 TO UG01 PIN 3 (ON I.C.)
      UL09 PIN 14 TO UL09 PIN 4 (ON I.C.)
      UM09 PIN 1 TO UJ12 PIN 1



4. ITEM 107 IN -0001 LM CONSISTS OF COMPONENTS WHICH ARE AUTO INSERTED & CONTAINED IN THE -5001 LM

5. REWORK PROCEDURE FOR REV B & C PWB (2261991)
   A. CUT UP23 PIN 1
   B. ADD WIRE UP12 PIN 11 TO UP23-1 (ON IC)

6. REWORK PROCEDURE FOR REV B, C, D, E, AND F PWBS
   A. CUT PIN UE06 PIN 8
   B. REMOVE WIRE FROM US12 PIN 5 TO UE6 PIN 9
   C. ADD WIRES BETWEEN THE FOLLOWING POINTS
      FROM US12 PIN 5 TO UF6 PIN 5
      FROM UE6 PIN 10 TO UF6 PIN 4
      FROM UF6 PIN 6 TO UF6 PIN 9
      FROM UF6 PIN 9 TO UF6 PIN 10
      FROM UF6 PIN 8 TO UF6 PIN 12
      FROM UK4 PIN 12 TO UF6 PIN 13
      FROM UF6 PIN 11 TO UF12 PIN 13
      FROM UF12 PIN 7 TO I.C. PAD UE6 PIN 8

TEXAS INSTRUMENTS	DWN	DATE 5-26-79	SIZE D	FSCM NO 96214	DRAWING NO 22-[illegible]	REV G
	ISSUE DATE		SCALE 1/1		SHEET 2 OF 2	

TEXAS INSTRUMENTS INCORPORATED — LIST OF MATERIAL — PAGE 1 of

DATE 02/21/80 — PART NUMBER LM2261990-0001 — REV H

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	REF	EA		2261992-9901	LOGIC DIAGRAM,CACHE MEMORY CONTROLLER	
0003	REF	EA		2261993-9901	TEST PROCEDURE,CACHE MEMORY CONTROLLER	
0004	REF	EA		2261994-9901	SPECIFICATION,CACHE MEMORY CONTROLLER	
0019	00001.000	EA		0219402-7201	NETWORK SN74S201N	
0019A					UA1	
0020	00017.000	EA		0896089-0001	IC,SN74LS240N,LINE DRIVERS	001295-SN74LS240N
0020A					UA23,UA27,UB23,UC23,UH27,	
0020B					UJ27,UV12,UV15,UV18,UV22,	
0020C					UV24,UV26,UV28,UV30,UV9,	
0020D					UW4,UW6	
0021	00001.000	EA		0996089-0002	IC,SN74LS241N,LINE DRIVERS	01295S-N74LS241N
0021A					UP6	
0022	00004.000	EA		0996089-0004	IC,SN74LS244N LINE DRIVER	-SN74LS244N
0022A					UB12,UC12,UE12,UV1	
0024	00001.000	EA		0996138-0001	IC,SN74LS266N 2-INPUT EXCLUSIVE-NOR GATE	TI -SN74LS266N
0024A					UB1	
0025	00002.000	EA		0996029-0001	IC,SN74LS273N OCTAL D-TYPE FLIP/FLOP	TI -SN74LS273N
0025A					UW6,UW30	
0029	00007.000	EA		0996420-0001	IC, SN74LS373N	001295-SN74LS373N
0029A					UB27,UC27,UD23,UD27,UE23,	

DRAFTSMAN — DATE — CKD DRAFTSMAN J.R.Doty 2-22-80 — DATE — DESIGN ENGINEER — DATE — TITLE: CACHE MEMORY CONTROLLER

APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. 7047 — PART NUMBER LM2261990-0001 — REV H

TEXAS INSTRUMENTS INCORPORATED — LIST OF MATERIAL — PAGE 2 of

DATE 02/21/80 — PART NUMBER LM2261990-0001 — REV H

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0029B					UE27,UG6	
0032	00001.000	EA		0219402-7400	NETWORK SN74S00N	
0032A					UF06	
0048	00003.000	EA		0996063-0001	IC,SN74S241N,LINE DRIVERS	001295-SN74S241N
0048A					UA4,UA6,UA9	
0051	00006.000	EA		0996307-0001	IC,SN74S373,OCTAL D, FLIPFLOP	TI -SN74S373
0051A					UA20,UN12,UN22,UN26	
0052	00044.000	EA		0996680-0001	IC, 16K RAM, (SEL)	001295-TMS4116/ZA0727
0052A					UT10,UT11,UT13,UT14,UT16,	
0052B					UT17,UT19,UT21,UT22,UT23,	
0052C					UT24,UT25,UT26,UT27,UT28,	
0052D					UT29,UT30,UT31A,UT5,UT6,	
0052E					UT8,UT9,UU10,UU11,UU13,	
0052F					UU14,UU16,UU17,UU19,UU21,	
0052G					UU22,UU23,UU24,UU25,UU26,	
0052H					UU27,UU28,UU29,UU30,UU31A,	
0052J					UU5,UU6,UU8,UU9	
0053	00001.000	EA		0946693-0067	ROM #1,16K ECC DECODE,990/10	
0053A					UN23	
0054	00002.000	EA		0896462-0001	DELAY LINE,TAPPED	097722-EP-7111

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: CACHE MEMORY CONTROLLER

APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2261990-0001 — REV H

TEXAS INSTRUMENTS INCORPORATED — LIST OF MATERIAL — PAGE 3 of

DATE 02/21/80 — PART NUMBER LM2261990-0001 — REV H

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0054A					UR4,UR7	
0055	00001.000	EA		0996850-0004	DELAY LINE, TAPPED, .09 UHMS, 20 NSEC	016714-TZA4-10
0055A					UH1	
0056	00001.000	EA		0996850-0006	DELAY LINE, TAPPED, 1.1 UHMS, 30 NSEC	016714-TZA6-10
0056A					UR10	
0057	00004.000	EA		0972583-0001	NETWORK,SNZ5365	TI- -SN75365
0057A					UI2,UI3,UW2,UW3	
0062	00002.000	EA		0972037-1220	NETWORK,RES 22 OHM 2% 16PIN #ELEMENT	073138-898-3-R22
0062A					UI4,UU4	
0064	00001.000	EA		2210025-0001	NETWORK,RES 220 OHM 2% 8-PIN FILM FIX	080294-4308M-101-221
0064A					UW1	
0065	00002.000	EA		0972547-0008	SWITCH, SLIDE-SPST,DIP 8 SWITCHES	
0065A					UC31,UD1	
0066	00000.500	FT		0457313-0006	WIRE 24 AWG SOLID,TEFLON,WHITE	QPL - MIL-W-16878/4
0067	00044.000	EA		2210188-0003	SOCKET,LOW PROFILE,DIP,16 CONT	003612-01L816P-108
0067A					XUZT5,XUZW31A,XUZU30,XUZU29	
0067B					XUZT6,XUZT8,XUZT9,XUZT10,	
0067C					XUZT11,XUZT13,XUZT14	
0067D					XUZT16,XUZT17,XUZT19,XUZT21	
0067E					XUZT22,XUZT23,XUZT24,XUZT25	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: CACHE MEMORY CONTROLLER

APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2261990-0001 — REV H

TEXAS INSTRUMENTS INCORPORATED — LIST OF MATERIAL — PAGE 4 of

DATE 02/21/80 — PART NUMBER LM2261990-0001 — REV H

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0067F					XUZT26,XUZT27,XUZT28,XUZT29	
0067G					XUZT30,XUZT31A,XUZU5,XUZU6	
0067H					XUZU8,XUZU9,XUZU10,XUZU11	
0067J					XUZU13,XUZU14,XUZU16,XUZU17	
0067K					XUZU19,XUZU21,XUZU22,XUZU23	
0067L					XUZU24,XUZU25,XUZU26,XUZU27	
0067M					XUZU28	
0068	00001.000	EA		2210188-0005	SOCKET, LOW PROFILE, DIP, 20 PINS	003612-01L820P-108
0068A					XUZN23	
0069	00028.000	EA		2210188-0006	SOCKET,LOW PROFILE,DIP, 22 PINS, LO CONT	003612-01L822P-108
0069A					XUZA16,XUB16,XUZC16,XUZD16	
0069B					XUZF16,XUZG16,XUZH16,XUZJ16	
0069C					XUZB20,XUZC20,XUZD20,XUZF20	
0069D					XUZG20,XUZM20,XUZK20,XUZM20	
0069E					XUZN20,XUZA25,XUZB25,XUZC25	
0069F					XUZD25,XUZF25,XUZG25,XUZH25	
0069G					XUZJ25,XUZK25,XUZM25,XUZJ20	
0077	00002.000	EA		0972946-0081	RES FIX 4.7K OHM 5 % .25 W CARBON FILM	ROH - R-25
0077A					R9,R10	
0081	00002.000	EA		0972753-0012	CAP,FIXED 220PF 25 WVDC 2.0%	UC -C5D0221G

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: CACHE MEMORY CONTROLLER

APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2261990-0001 — REV H

TEXAS INSTRUMENTS INCORPORATED — DATE 02/21/80 — LIST OF MATERIAL — PAGE 5 of — PART NUMBER LM2261990-0001 — REV H

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0081A					C3,C4	
0083	00001.000	EA		0972753-0008	CAPACITOR,100PF 25V 2% FX CERAMIC DIELEC	
0083A					C1	
0085	00001.000	EA		0972757-0016	CAP,FIXED CER 1800PF 50WRDC +10%	007115-CAC02X7R391K10
0085A					C6	
0088	00010.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0088A					C33,C35,C38,C40,C42,C46,	
0088B					C47,C49,C51,C54	
0090	00002.000	EA		0972924-0006	CAP FIX TANT SOLID 39 MFD 10 % 10 WVDC	CPL -M39003/1-2259
0090A					C11,C12	
0091	00001.000	EA		0972057-0001	TRANSISTOR-A5T2222 NPN SILICON	TI- -A5T2222
0091A					Q6	
0092	00004.000	EA		0972958-0002	TRANSISTOR,2N2907A PNP GEN PURP SW TO-18	TI - 2N2907A
0092A					Q2,Q3,Q4,Q5	
0093	00001.000	EA		0972955-0001	XSTR 2N2369A,NPN,HIGH SPEED SW,TO-18	MOT - 2N2369A
0093A					Q1	
0094	00001.000	EA		0539468-0002	DIODE,1N4002 1AMP 100PIV RECTIFIER	TI - 1N4002
0094A					CR16	
0095	00002.000	EA		0972537-0001	DIODE,LED 550-0103 50 MA 3 V	DIA --550-0103
0095A					CR1,CR2	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: CACHE MEMORY CONTROLLER

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM2261990-0001 | REV H

TEXAS INSTRUMENTS INCORPORATED — DATE 02/21/80 — LIST OF MATERIAL — PAGE 6 of — PART NUMBER LM2261990-0001 — REV H

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0096	00013.000	EA		0226609-0001	DIODE,VISIBLE LIGHT EMITTING	
0096A					CR3,CR4,CR5,CR6,CR7,CR8,CR9	
0096B					CR10,CR11,CR12,CR13,CR14	
0096C					CR15	
0097	00002.000	EA		0972137-0005	CONNECTOR,PC 50 PIN	BEI - 65483-005
0097A					P3,P4	
0098	00001.000	EA		0945239-0001	BRACKET-STIFFENER, PWB, 14IN	
0099	00001.000	EA		0944954-0001	INSULATOR, PWB, 14IN	
0100	00002.000	EA		0533844-0001	EJECTOR, NYLON, NON-LOCKING, PWB	
0101	00003.000	EA		0972684-0002	SCREW,TMD FRMG,HEX WSHR HD,2-56X1/4 LG	
0102	00028.000	EA		2210338-0001	IC,RANDOM ACCESS MEM,TTL	007263-93422PC
0102A					UA16 UA25 UB16 UB20 UB25	
0102B					UC16 UC20 UC25 UD16 UD20	
0102C					UD25 UF16 UF20 UF25 UG16	
0102D					UG20 UG25 UH16 UH20 UH25	
0102E					UJ16 UJ20 UJ25 UK20 UK25	
0102F					UM20 UM25 UN20	
0103	00001.000	EA		0539371-0557	RES FIX FILM 61.9K OHM 1% .13 WATT	COR - MC4
0103A					R2	
0104	00001.000	EA		0972757-0001	CAP,FIXED CERAMIC 100 PF 10% 50V	UC -C51C101K

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: CACHE MEMORY CONTROLLER

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM2261990-0001 | REV H

TEXAS INSTRUMENTS
INCORPORATED

DATE 02/21/80 **LIST OF MATERIAL** PAGE 7 of

PART NUMBER LM2261990-0001 REV H

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0104A					C22	
0106	00001.000	EA		0972946-0045	RES FIX 150 OHM 5 % .25 W CARBON FILM	ROH - R-25
0106A					R19	
0107	00001.000	EA		2261990-5001	AUTO INSERTED PARTS LIST FOR 2261990-1	

DRAFTSMAN / DATE	CKD DRAFTSMAN / DATE	DESIGN ENGINEER / DATE	TITLE
			CACHE MEMORY CONTROLLER
APPD MFG / DATE	APPD. PROJECT ENGINEER / DATE	RELEASED / DATE	PROJECT NO. / PART NUMBER / REV
			LM2261990-0001 H

TEXAS INSTRUMENTS INCORPORATED — DATE 02/21/80 — LIST OF MATERIAL — PAGE 1 of — PART NUMBER LM2261990-5001 — REV H

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2261991-0001	PWB,CACHE MEMORY CONTROLLER	
0005	00003.000	EA		0972900-7400	NETWORK SN74LS00N	TI -SN74LS00N
0005A					UN4,UK6,UG29	
0006	00002.000	EA		0972900-7402	NETWORK,SN74LS02N	
0006A					US20,UJ29	
0007	00004.000	EA		0972900-7404	NETWORK SN74LS04N	
0007A					UM6,UE4,UM31,US4	
0008	00004.000	EA		0972749-0001	NETWORK, SN74LS08N	
0008A					UN1,UR1,UR12,UM29	
0009	00002.000	EA		0972900-7410	NETWORK SN74LS10N	
0009A					US12,UL6	
0010	00002.000	EA		0972788-0001	NETWORK,SN74LS11,POSITIVE AND GATE	
0010A					UC6,UJ4	
0011	00004.000	EA		0972900-7432	NETWORK SN74LS32N	TI -SN74LS32N
0011A					UN1,UM27,UM18,UK29	
0012	00001.000	EA		0996780-0001	IC,SN74LS33N QUAD POSITIVE-NOR BUFFER	001295-SN74LS33N
0012A					UA12	
0013	00004.000	EA		0972900-7451	NETWORK SN74LS51N	TI -SN74LS51N
0013A					UP12,UF1,US6,UK27	
0014	00001.000	EA		0972900-7454	NETWORK SN74LS54N	TI -SN74LS54N

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO INSERTED PARTS LIST FOR 2261990-1

APPD -MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM2261990-5001 | REV H

TEXAS INSTRUMENTS INCORPORATED — DATE 02/21/80 — LIST OF MATERIAL — PAGE 2 of — PART NUMBER LM2261990-5001 — REV H

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0014A					UP9	
0015	00006.000	EA		0972900-7474	NETWORK SN74LS74N	
0015A					UG1,UG31,UN31,UL9,UM9,UR20	
0016	00001.000	EA		0996116-0001	IC,SN74LS75N, 4-BIT BISTABLE LATCH	001295-SN74LS75N
0016A					UL29	
0017	00001.000	EA		0972782-0001	NETWORK SN74LS132N	TI -SN74LS132N
0017A					UL12	
0018	00002.000	EA		0972900-7175	NETWORK SN74LS175N	
0018A					UM23,UP29	
0023	00006.000	EA		0996136-0002	IC,SN74LS258N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS258N
0023A					UB4,UC4,UM15,UM9,UK23,UN27	
0024	00001.000	EA		0996138-0001	IC,SN74LS266N 2-INPUT EXCLUSIVE-NOR GATE	TI -SN74LS266N
0024A					UC1	
0026	00002.000	EA		0972652-0001	NETWORK SN74LS283N	
0026A					UB6,UB9	
0027	00001.000	EA		0972653-0001	NETWORK,SN74LS293N	
0027A					UF31	
0028	00002.000	EA		0972787-0004	NETWORK SN74LS368N	
0028A					UM29,UM24	
0030	00001.000	EA		0996424-0001	IC,SN74LS375N 4 BIT BISTABLE LATCHES	001295-SN74LS375N

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO INSERTED PARTS LIST FOR 2261990-1

APPD -MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM2261990-5001 | REV H

T.I. 13849

TEXAS INSTRUMENTS INCORPORATED — DATE 02/21/80 — LIST OF MATERIAL — PAGE 3 of — PART NUMBER LM 2261990-5001 — REV H

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0030A					UG4	
0031	00001.000	EA		0996508-0001	IC,74LS393N DUAL BINARY COUNTER	001295-74LS393N
0031A					UH4	
0032	00002.000	EA		0219402-7400	NETWORK SN74S00N	
0032A					UH23,UJ12	
0033	00002.000	EA		0219402-7404	NETWORK SN74S04N	
0033A					UN12,US9	
0034	00001.000	EA		0219402-7405	NETWORK SN74S05N	
0034A					UM12	
0035	00002.000	EA		0219402-7408	NETWORK SN74S08N	TI- -SN74S08N
0035A					UD4,UL4	
0036	00003.000	EA		0219402-7410	NETWORK SN74S10N	
0036A					UJ6,UK12,UL23	
0037	00002.000	EA		0219402-7411	NETWORK SN74S11N	
0037A					UF4,UP1	
0038	00001.000	EA		0219402-7420	NETWORK SN74S20N	
0038A					UN29	
0039	00001.000	EA		0219402-7430	NETWORK SN74S30N	
0039A					UP25	
0040	00002.000	EA		0219402-7432	NETWORK SN74S32N	TI- -SN74S32N

DRAFTSMAN DATE — CKD. DRAFTSMAN DATE — DESIGN ENGINEER DATE — TITLE: AUTO INSERTED PARTS LIST FOR 2261990-1

APPD.-MFG. DATE — APPD. PROJECT ENGINEER DATE — RELEASED DATE — PROJECT NO. — PART NUMBER LM 2261990-5001 — REV H

TEXAS INSTRUMENTS INCORPORATED — DATE 02/21/80 — LIST OF MATERIAL — PAGE 4 of — PART NUMBER LM 2261990-5001 — REV H

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0040A					UD6,UN9	
0041	00001.000	EA		0996851-0001	IC,QUAD POSITIVE-NAND, SN74S38N	-SN74S38N
0041A					UE6	
0042	00001.000	EA		0219402-7464	NETWORK SN74S64N	
0042A					UH4	
0043	00010.000	EA		0219402-7474	NETWORK SN74S74N	
0043A					UJ1,UK1,UM4,UL1,UR23,UN6,	
0043B					UP4,US1,UM4,UP23	
0044	00001.000	EA		0219402-7486	NETWORK SN74S86N	
0044A					US23	
0045	00002.000	EA		0219402-7133	NETWORK SN74S133N	
0045A					UF9,UK9	
0046	00010.000	EA		2210136-0001	IC-EXCLUSIVE-OR/NOR GATE	001295-SN74S135N
0046A					UB29,UC29,UC9,UD29,UD9,	
0046B					UE29,UE9,UG9,UH9,UJ9	
0047	00002.000	EA		0219402-7138	NETWORK SN74S138N	
0047A					UE31,UF29	
0049	00001.000	EA		0219402-7260	NETWORK SN74S260N	
0049A					UH6	
0050	00014.000	EA		0219402-7280	NETWORK SN74S280N	TI -SN74S280N

DRAFTSMAN DATE — CKD. DRAFTSMAN DATE — DESIGN ENGINEER DATE — TITLE: AUTO INSERTED PARTS LIST FOR 2261990-1

APPD.-MFG. DATE — APPD. PROJECT ENGINEER DATE — RELEASED DATE — PROJECT NO. — PART NUMBER LM 2261990-5001 — REV H

TEXAS INSTRUMENTS INCORPORATED — DATE 02/21/80 — **LIST OF MATERIAL** — PAGE 5 of — PART NUMBER LM 2261990-5001 — REV H

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0050A					UD12,UE12,UF23,UF27,UG12,	
0050B					UG23,UG27,UH12,UR25,UR27,	
0050C					UR29,US25,US27,US29	
0058	00001.000	EA		0802023-0001	NETWORK SN75138N	
0058A					UA29	
0059	00001.000	EA		0972810-0001	NETWORK-SN74LS221N	
0059A					US15	
0060	00001.000	EA		0972037-2680	NETWORK,RES 680 OHM 2% 16PIN 8ELEMENT	073138-898-3-R680
0060A					UD31	
0061	00001.000	EA		0800118-0004	RESISTOR 220 OHMS DIL PULL UP 16 PINS	BEC -8981R220
0061A					UW28	
0063	00002.000	EA		0800118-0013	RESISTOR, FIXED-ARRAY, 4.7K	
0063A					UP27,UE1	
0070	00004.000	EA		0972946-0025	RES FIX 22.0 OHM 5 % .25 W.CARBON FILM	KOH - R-25
0070A					R25,R26,R27,R28	
0071	00003.000	EA		0972946-0041	RES FIX 100 OHM 5 % .25 W CARBON FILM	KOH - R-25
0071A					R11,R15,R20	
0072	00004.000	EA		0972946-0049	RES FIX 220 OHM 5 % .25 W CARBON FILM	KOH - R-25
0072A					R37,R38,R39,R40	
0073	00001.000	EA		0972946-0053	RES FIX 330 OHM 5 % .25 W CARBON FILM	KOH - R-25

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO INSERTED PARTS LIST FOR 2261990-1

APPD MFG. DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM 2261990-5001 | REV H

TEXAS INSTRUMENTS INCORPORATED — DATE 02/21/80 — **LIST OF MATERIAL** — PAGE 6 of — PART NUMBER LM 2261990-5001 — REV H

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0073A					R31	
0074	00001.000	EA		0972946-0038	RES FIX 75.0 OHM 5 % .25 W.CARBON FILM	KOH - R-25
0074A					R14	
0075	00001.000	EA		0972946-0061	RES FIX 680 OHM 5 % .25 W CARBON FILM	KOH - R-25
0075A					R30	
0076	00007.000	EA		0972946-0065	RES FIX 1.0K OHM 5% .25 W CARBON FILM	KOH - R-25
0076A					R6,R29,R32,R33,R34,R35,R36	
0077	00007.000	EA		0972946-0081	RES FIX 4.7K OHM 5 % .25 W CARBON FILM	KOH - R-25
0077A					R5,R7,R8,R21,R22,R23,R24	
0078	00001.000	EA		0539370-0377	RES FIX FILM 825 OHM 1% .25 WATT	CUR - NA55
0078A					R17	
0079	00001.000	EA		0539371-0478	RES FIX FILM 9.31K OHM 1% .13 WATT	CUR - NC4
0079A					R18	
0080	00001.000	EA		0539371-0453	RES FIX FILM 5.11K OHMS 1% .13WATT	CUR - NC4
0080A					R1	
0082	00001.000	EA		0972757-0025	CAP FIX CER .01MF 10% 50V	
0082A					C5	
0084	00001.000	EA		0972753-0016	CAP., 430 PF,2%,25VDC	
0084A					C2	
0086	00001.000	EA		0972757-0021	CAP, FIX, CERAMIC, 4700PF, 50V 10%	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO INSERTED PARTS LIST FOR 2261990-1

APPD MFG. DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM 2261990-5001 | REV H

TEXAS INSTRUMENTS INCORPORATED

DATE 02/21/80 — **LIST OF MATERIAL** — PAGE 7 of — PART NUMBER LM2261990-5001 — REV H

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0086A					C9	
0087	00007.000	EA		0972763-0009	CAP,FIXED .0047MF 50 VOLTS	004222-MC105E4722
0087A					C18,C19,C20,C21,C23,C24,C25	
0088	00055.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0088A					C10,C15,C16,C17,C26,C27,C28	
0088B					C29,C30,C31,C32,C34,C36,	
0088C					C37,C39,C41,C43,C44,C45,	
0088D					C48,C50,C52,C53,C55,C66,	
0088E					C67,C68,C69,C70,C71,C72,	
0088F					C73,C74,C75,C76,C77,C78,	
0088G					C79,C80,C81,C82,C83,C84,	
0088H					C85,C86,C87,C88,C89,C90,	
0088J					C91,C92,C93,C94,C95,C96	
0089	00011.000	EA		0972924-0014	CAP FIX TANT SOLID 15 MFD 10 % 20 VOLT QPL -M39003/1-2289	
0089A					C14,C56,C57,C58,C59,C60,C61	
0089B					C62,C63,C64,C65	
0090	00004.000	EA		0972924-0006	CAP FIX TANT SOLID 39 MFD 10 % 10 VOLT QPL -M39003/1-2259	
0090A					C7,C8,C13,C97	
0105	00002.000	EA		0996136-0001	IC,SN74LS251N,DATA SELECTORS/MULTIPLEXER TI -SN74LS251N	
0105A					UJ23,UL27	

DRAFTSMAN / DATE	CKD. DRAFTSMAN / DATE	DESIGN ENGINEER / DATE	TITLE
			AUTO INSERTED PARTS LIST FOR 2261990-1

APPD. MFG. / DATE	APPD. PROJECT ENGINEER / DATE	RELEASED / DATE	PROJECT NO.	PART NUMBER	REV
				LM2261990-5001	H

TI 13849

NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL DEVICE TYPES ARE PREFIXED WITH SN74.
2. VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC's, PIN 14 OF ALL 14-PIN IC's, PIN 16 OF ALL 16-PIN IC's, PIN 20 OF ALL 20-PIN IC's, ETC.
3. GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC's, PIN 7 OF ALL 14-PIN IC's, PIN 8 OF ALL 16-PIN IC's, PIN 10 OF ALL 20-PIN IC's, ETC.
4. DEVICE TYPE, PIN NUMBERS, AND REFERENCE DESIGNATOR OF IC IS SHOWN AS FOLLOWS:

LS00 AND LS04 = DEVICE TYPE
1, 2 AND 3 = PIN NUMBERS
U2 AND U14 = REFERENCE DESIGNATOR

5. RESISTANCE VALUES ARE IN OHMS.
6. RESISTORS ARE ¼ WATT, 5%.
7. CAPACITANCE VALUES ARE IN MICROFARADS.
8. * = DEVICE POWERED BY +5V SW.
9. ** = DEVICE POWERED BY +5V STNBY.
10. FOR JUMPER SCHEDULE SEE ASS'Y. PRINT 2261990.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	CN453402(C) J Jarvis	4 DEC. 79	J Jarvis
B	CN450056(D) M Blake	1-30-80	J Barry
C	CN453420(E) M Hyatt	2-5-80	J Barry

DATA FLØW
BLØCK DIAGRAM

REV STATUS ØF SHEETS	REV	C	B	B	B	B	B	B	B		B				B	B	B	B	B	B	C	B	B	B	B	
	SH.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25

SEQ NO	IDENT	F-SPEC	NO	ADDITIONAL	NOTES
	PROCESS			CLASSIFICATION	

PROCESSES — FOR CORRELATION TO GOVT/IND SPECIFICATIONS, SEE TI DRAWING 729467

PARTS LIST

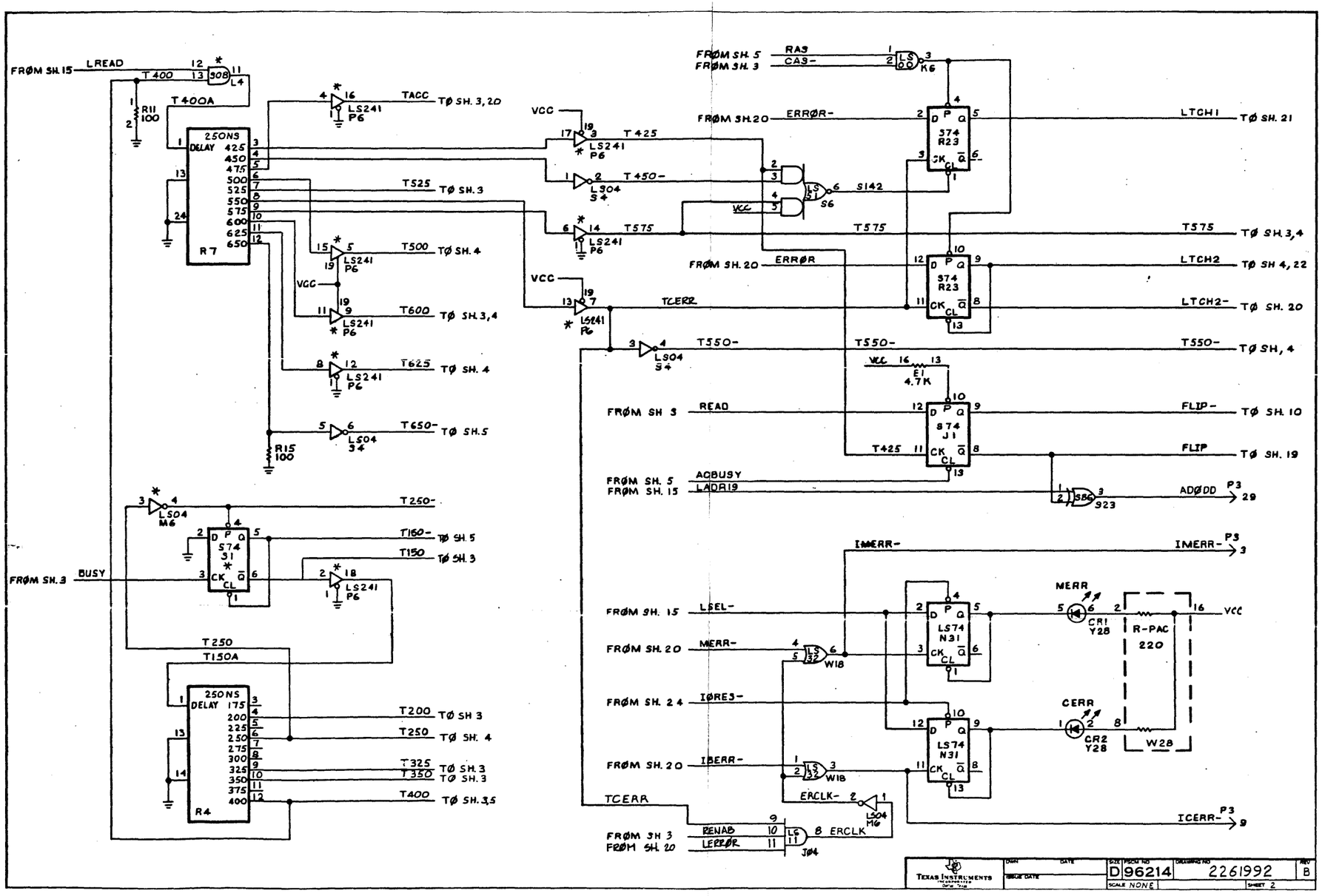
QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION	NOTES
		2261990	7047		
		NEXT ASSY	USED ON		
		APPLICATION			

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES: ANGLES ±1°
  3 PLACE DECIMALS ± .010
  2 PLACE DECIMALS ± .02
- INTERPRET DRAWING PER MIL-D-1000
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIM
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

.013 THRU .204 .125 - .001	.126 THRU .308 .250 - .001	.251 THRU .508 .500 - .001
.501 THRU .508 .750 - .001	.751 THRU .010 1.000 - .001	1.001 THRU 1.012 2.000 - .001

DRAWN	Augustine Vela 6/13/79	TEXAS INSTRUMENTS INCORPORATED DALLAS, TEXAS
CHK	C. Keller 7-4-79	LOGIC DIAGRAM, CACHE MEMORY CONTROLLER
ENGR		
APVD	7-19-79	
QA		
CONTR		
RLSE	Tony Bailey 7-18-79	SIZE D 96214 DRAWING NO 2261992
		SCALE NONE SHEET 1 OF 25


FROM SH.15
LREAD
T400
308
L4
T400A
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25ONS
DELAY
425
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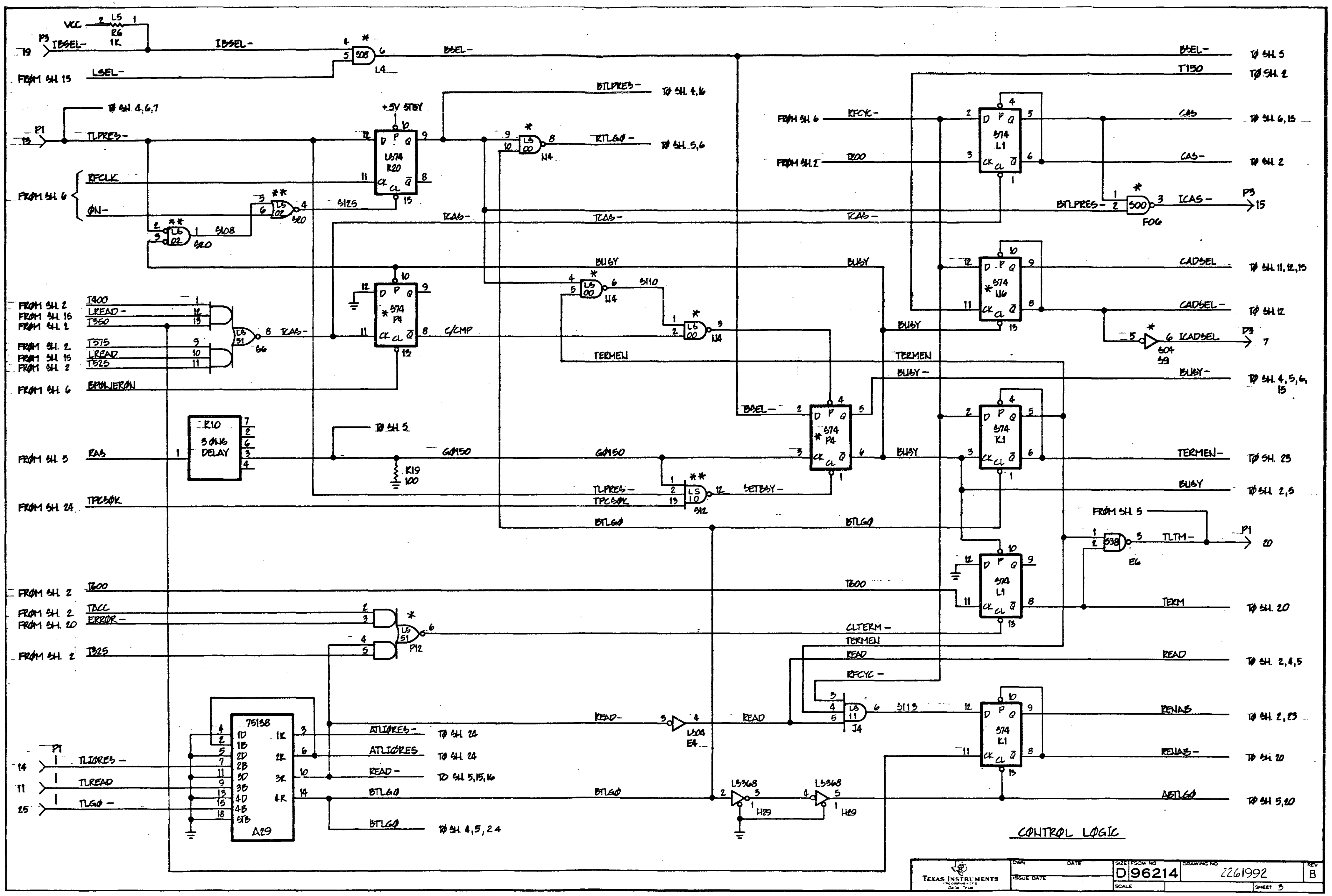
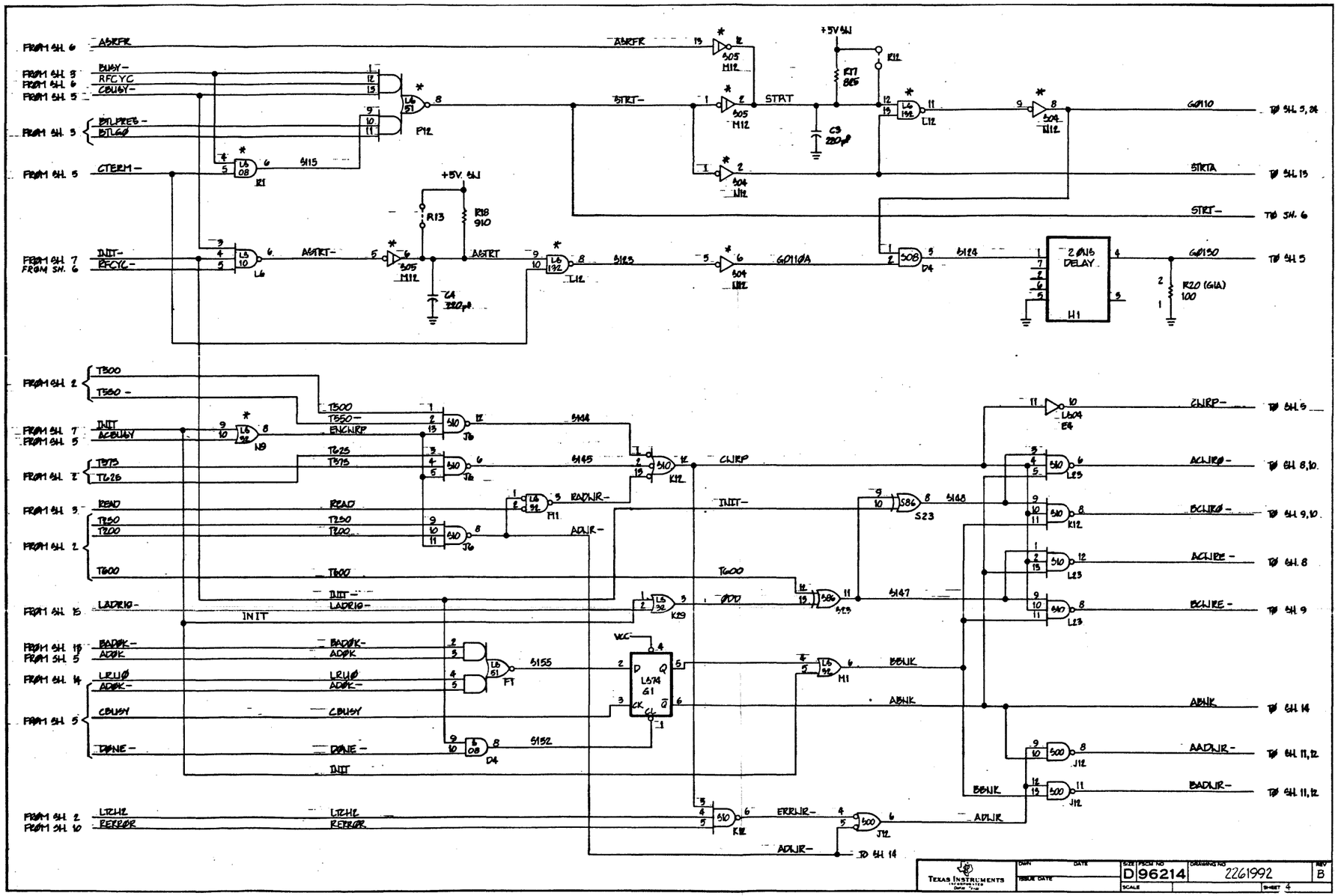
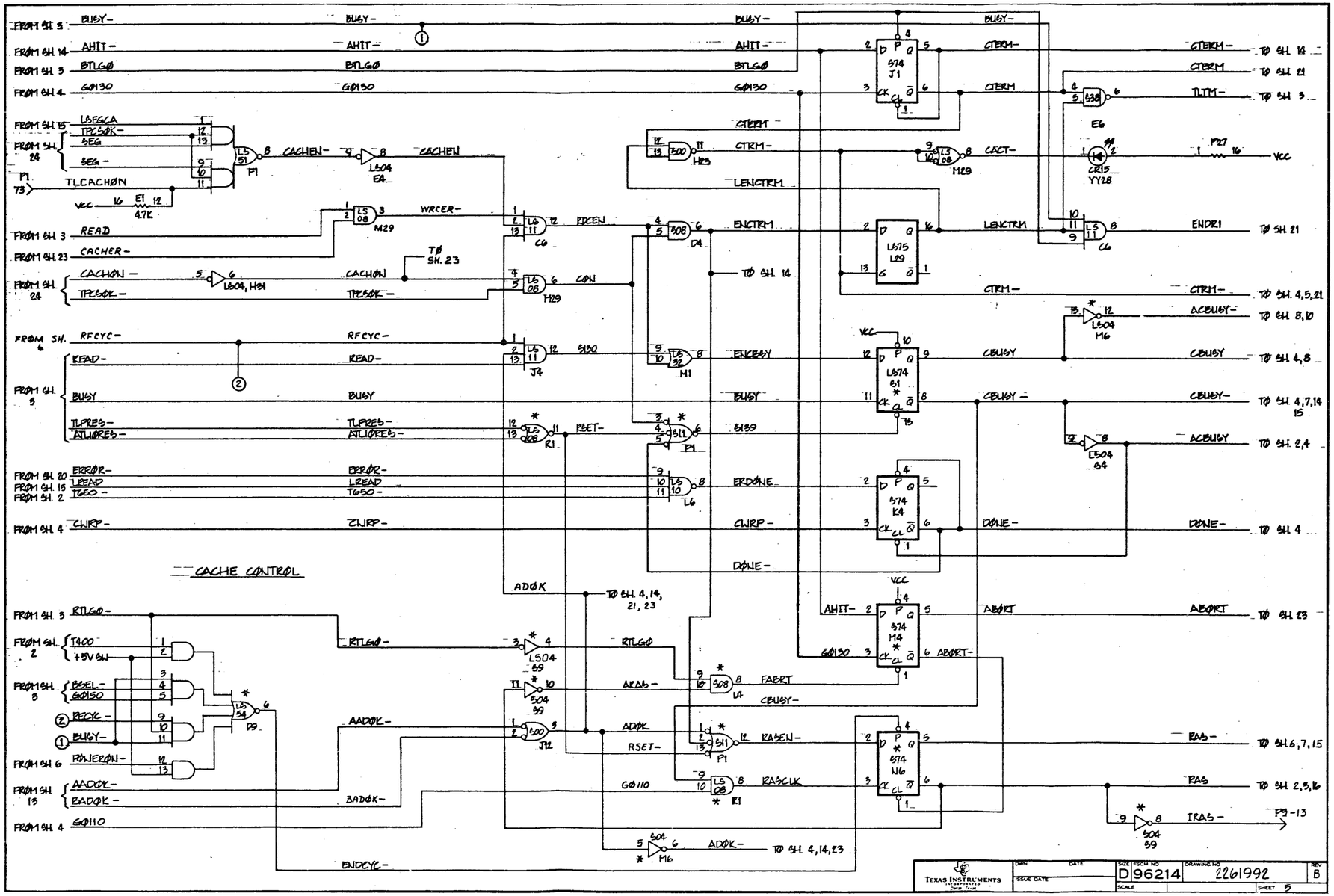
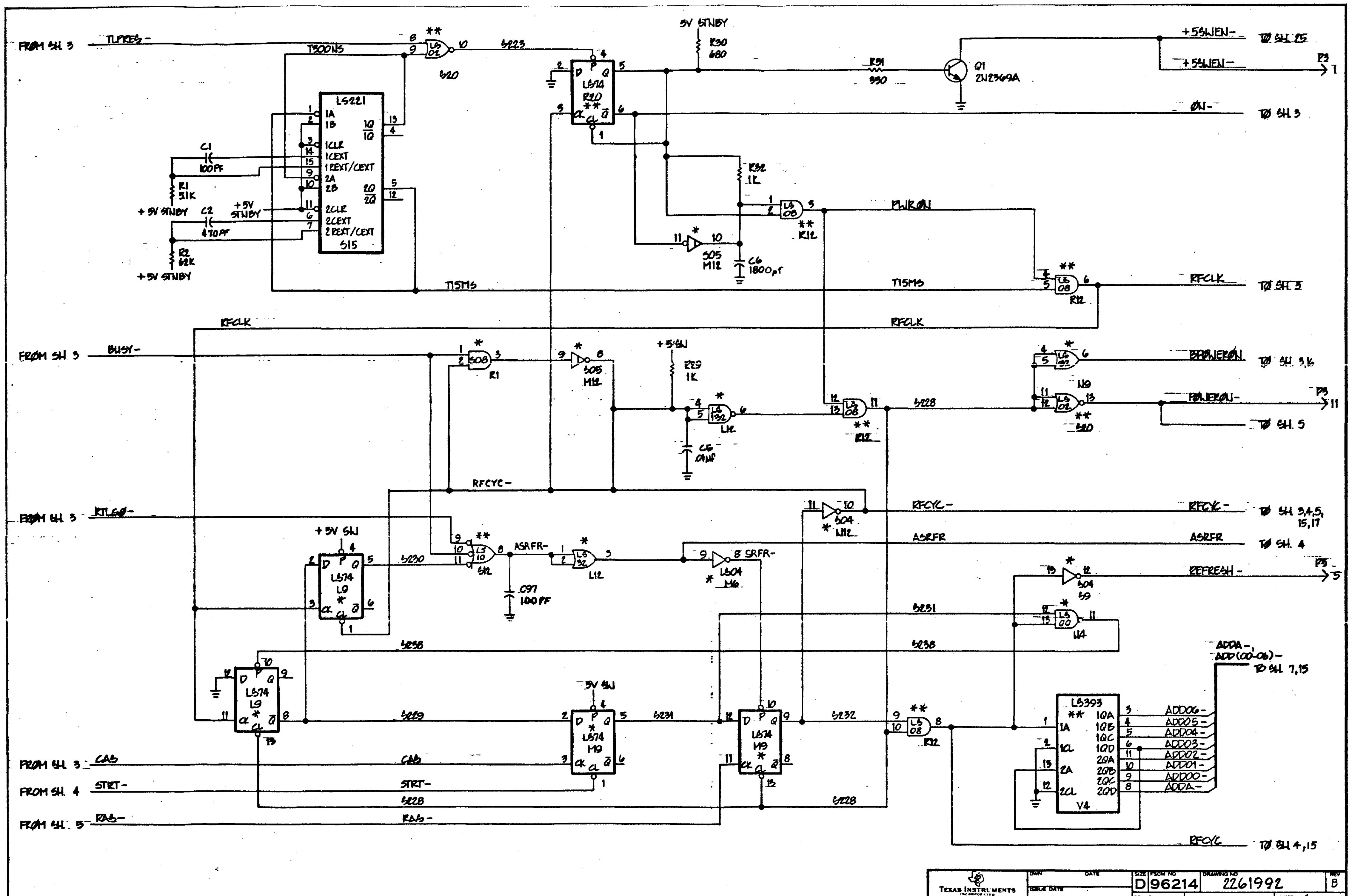
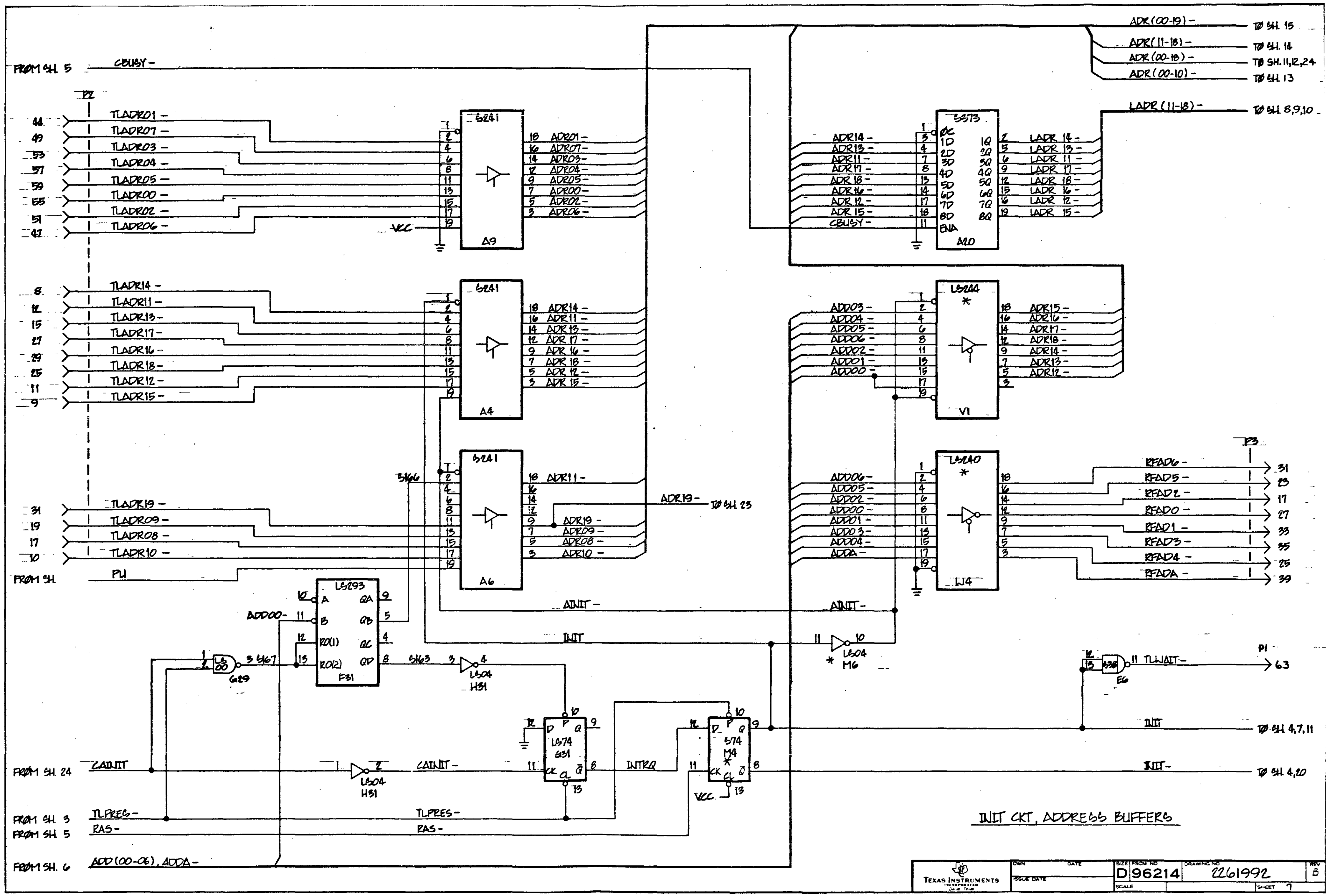
575
600
625
650
R7
TACC
TØ SH. 3, 20
LS241
P6
T525
TØ SH. 3
T500
TØ SH. 4
T600
TØ SH. 3,4
T625
TØ SH. 4
T650-
TØ SH. 5
R15
100
LS04
34
VCC
T425
T450-
LS04
S4
T575
TCERR
T550-
FROM SH 5
RA9
CA9-
FROM SH. 3
K6
FROM SH. 20
ERRØR-
374
R23
LTCH1
TØ SH. 21
S142
S6
ERRØR
LTCH2
TØ SH 4, 22
LTCH2-
TØ SH. 20
T550-
TØ SH, 4
E1
4.7K
READ
FLIP-
TØ SH. 10
J1
T425
FLIP
TØ SH. 19
ACBUSY
LADR19
ADØDD
P3
29
S23
IMERR-
P3
3
FROM SH. 15
LSEL-
FROM SH. 20
MERR-
W18
MERR
CR1
Y28
R-PAC
220
VCC
CERR
CR2
Y28
W28
FROM SH. 24
IØRE3-
IBERR-
ERCLK-
LS04
M16
8 ERCLK
TCERR
ICERR-
P3
9
FROM SH 3
RENAB
FROM SH. 20
LERRØR
J04
FROM SH. 3
BUSY
LS04
M6
T250-
T160-
TØ SH. 5
T150
TØ SH. 3
LS241
P6
T250
T150A
25ONS
DELAY
175
200
225
250
275
300
325
350
375
400
R4
T200
TØ SH 3
T250
TØ SH. 4
T325
T350
TØ SH. 3
T400
TØ SH. 3,5
TEXAS INSTRUMENTS
D96214
2261992
B
SCALE NONE
SHEET 2

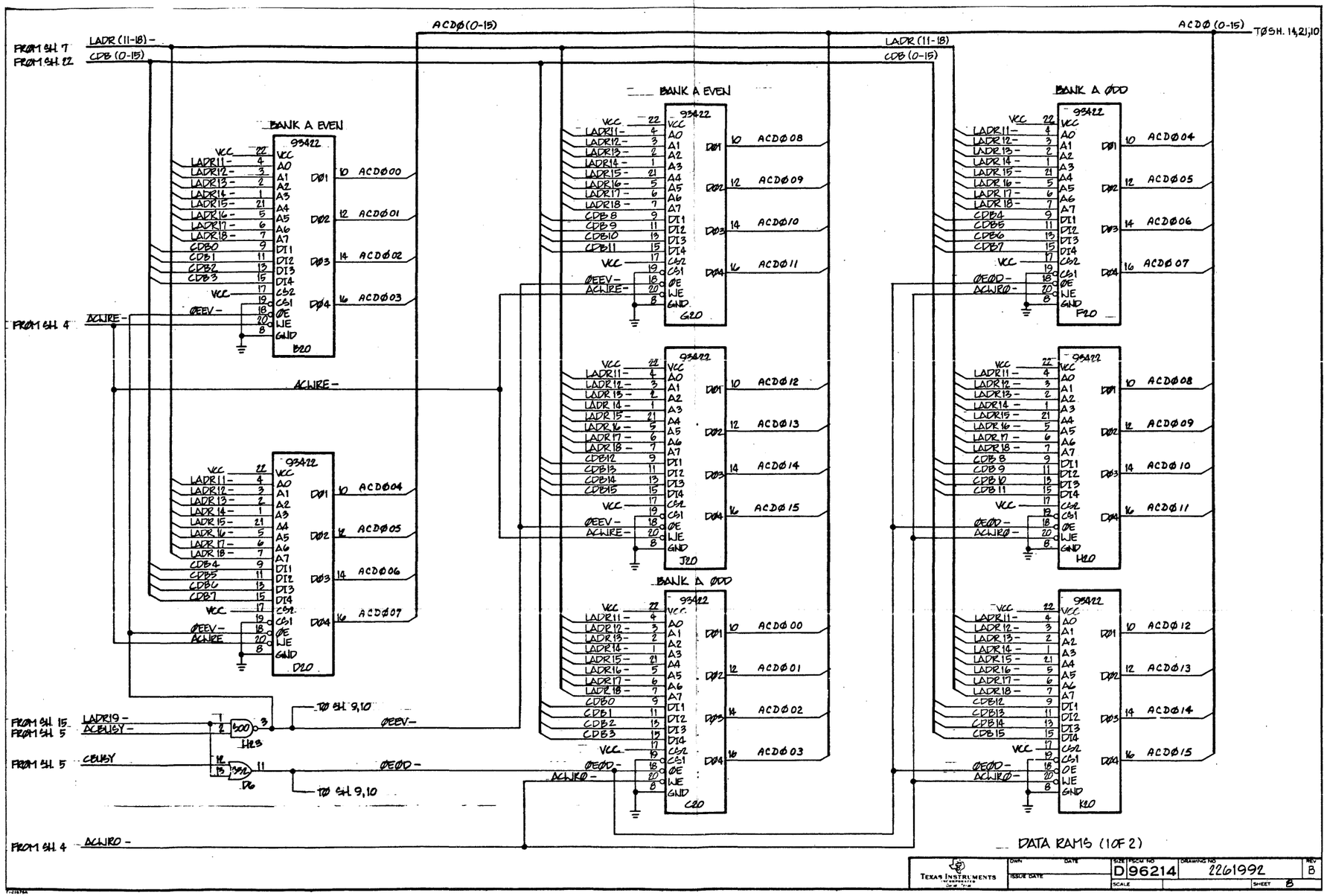

CONTROL LOGIC
TEXAS INSTRUMENTS
D 96214
2261992
B
SHEET 3

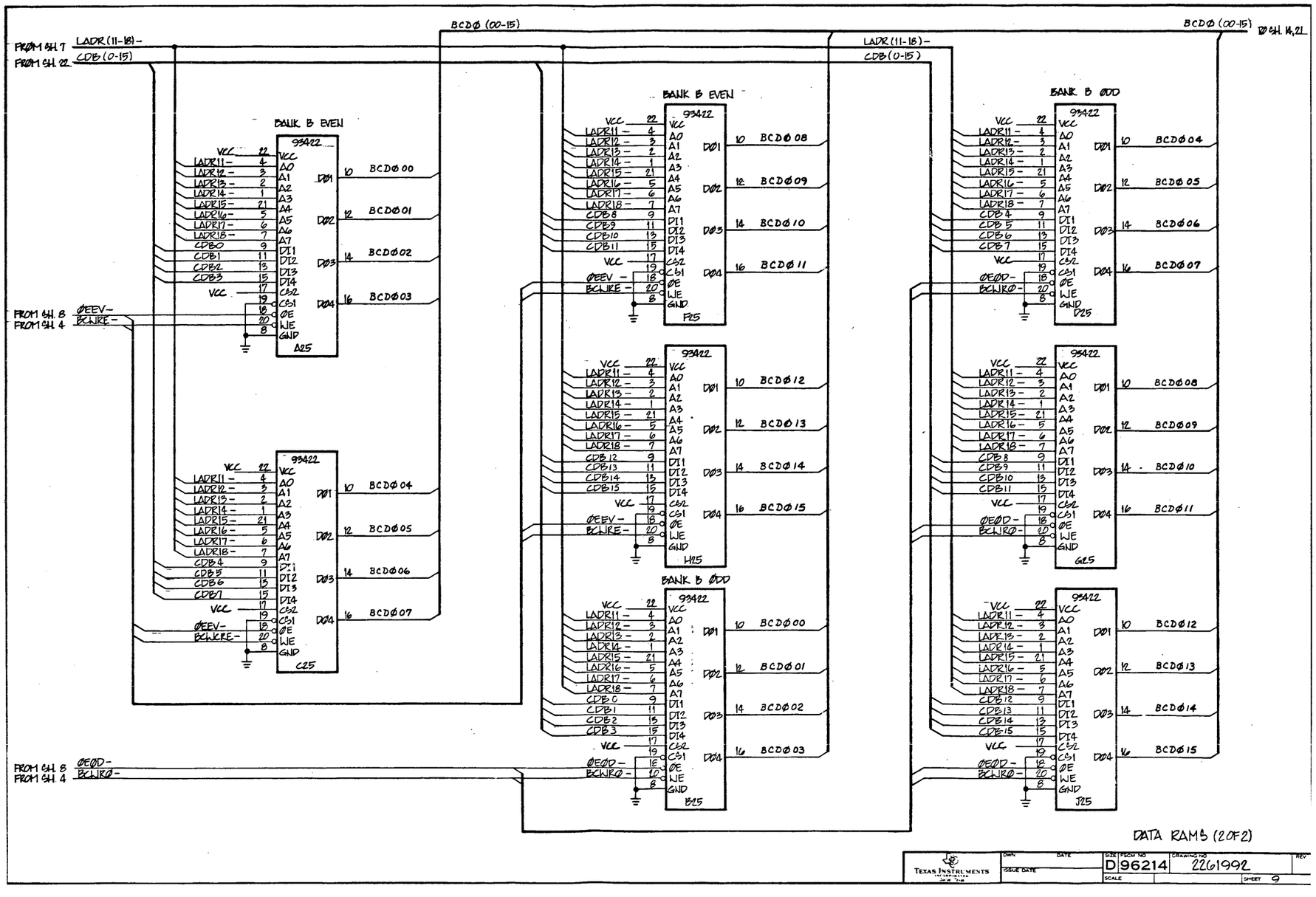

ABRFR
BUSY-
RFCYC
CBUSY-
BTLPRES-
BTLGD
CTERM-
INIT-
RFCYC-
ABSTRT-
ABSTRT
START-
START
+5V SH
R13
R18 910
C4 220pF
R17 665
C3 220pF
GØ110
GØ110A
GØ150
STRTA
2 ØUS DELAY
R20 (GIA) 100
T300
T300-
T625
T675
T675
T626
READ
T250
T200
T600
LADRIO-
BADRK-
ADRK
LRUØ
ADRK-
CBUSY
DONE-
INIT
LITHE
RERROR
ENCWRP
RADWR-
ADWR-
CWRP
INIT-
ERRWR-
BBWK
ABWK
ADWR
CWRP-
ACWRØ-
BCWRØ-
ACWRE-
BCWRE-
AADWR-
BADWR-
TO SH. 5, 2Ø
TO SH. 13
TO SH. 6
TO SH. 5
TO SH. 8,10.
TO SH. 9,10.
TO SH. 8
TO SH. 9
TO SH. 14
TO SH. 11, 12
TO SH. 11, 12
TO SH. 14
TEXAS INSTRUMENTS
D 96214
2261992
B

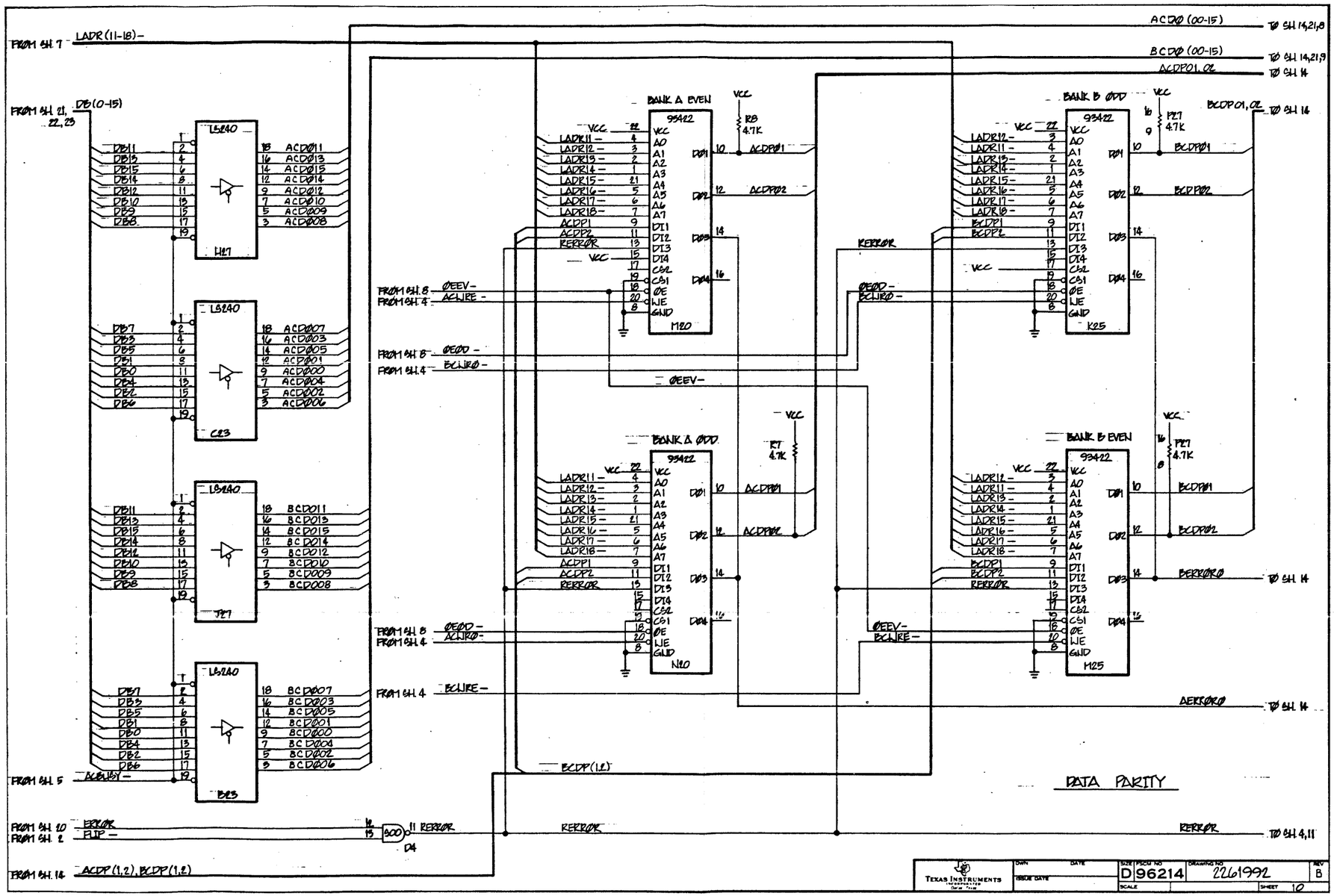

BUSY-
AHIT-
BTLG0
G0130
LSEGCA
TPCSOK-
SEG
SEG-
TLCACHON
CACHEN-
CACHEN
READ
CACHER-
CACHON-
TPCSOK-
CACHON
TO SH. 23
RFCYC-
READ-
BUSY
TLPRES-
ATLIORES-
RSET-
ERROR-
LREAD
TG50-
CWRP-
CACHE CONTROL
RTLG0-
T400
+5V SW
BSEL-
G0150
RCYC-
BUSY-
RWJERON-
AADOK-
BADOK-
G0110
ENDCYC-
WRCER-
RDCEN
CDN
ADOK
RTLG0
ARAS-
RSET-
FABRT
CBUSY-
RASEN-
RASCLK
ENCTRM
ENCBSY
ERDONE
CWRP-
DONE-
CTERM
CTRM-
LENCTRM
CACT-
CTERM-
TLTM-
ENDR1
ACBUSY-
CBUSY
ABORT
RAS-
IRAS-
TO SH. 14
TO SH. 21
TO SH. 9
TO SH. 4,5,21
TO SH. 8,10
TO SH. 4,8
TO SH. 4,7,14,15
TO SH. 2,4
TO SH. 4
TO SH. 23
TO SH. 6,7,15
TO SH. 2,3,16
TO SH. 4,14,23
TO SH. 4,14, 21, 23
P27
VCC
CR15
YY28
E6
E1
4.7K
M29
H29
M16
M1
J4
J1
P1
R1
K4
M4
N6
K1
L4
P9
J12
P9-13
TEXAS INSTRUMENTS
D
96214
2261992
B
SHEET 5

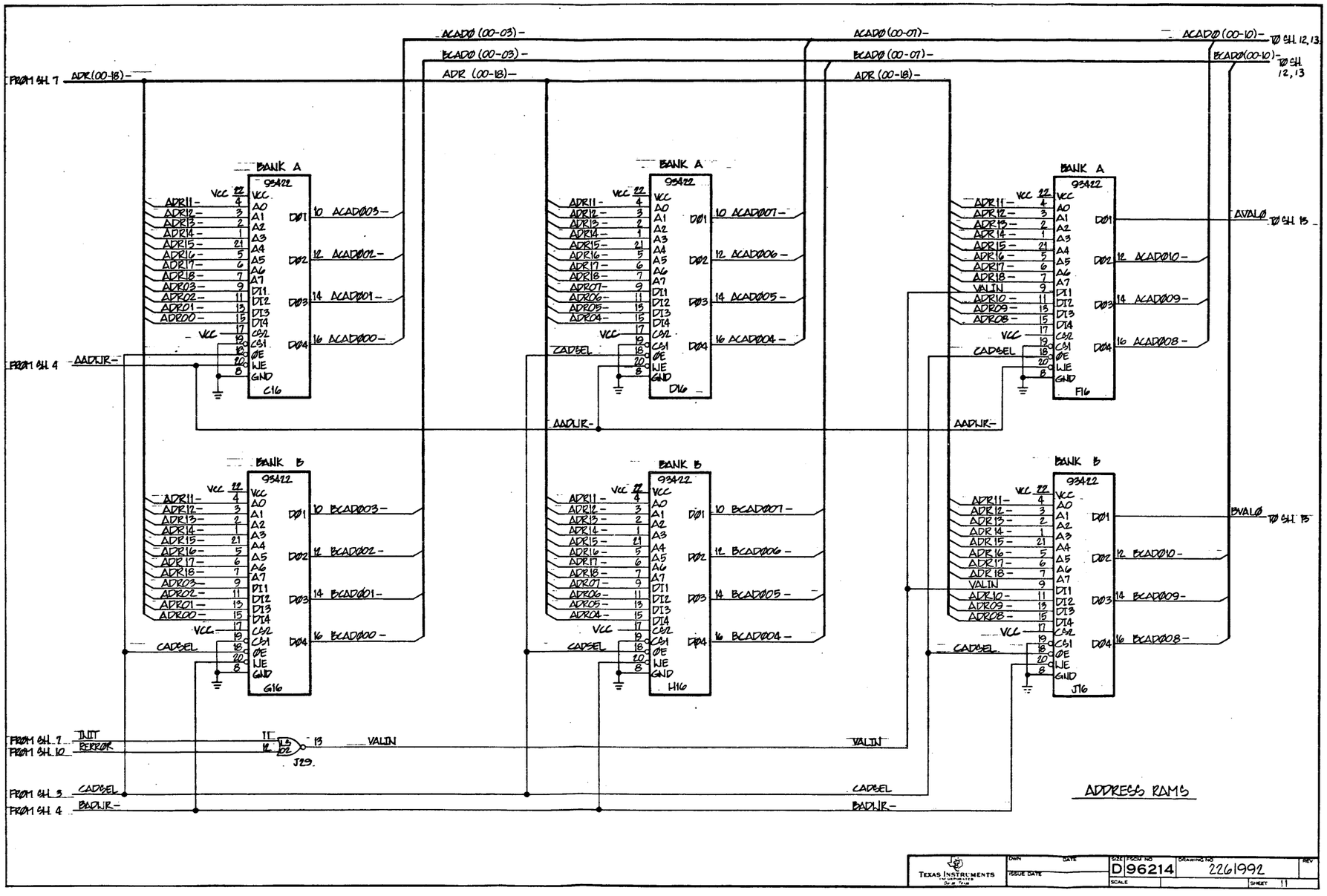

FROM SH. 3
TLPRES-
T300NS
LS221
T15MS
RFCLK
BUSY-
RFCYC-
ASRFR-
SRFR-
FROM SH. 3
CAS
FROM SH. 4
STRT-
FROM SH. 5
RAS-
5V STNBY
Q1
2N2369A
+5SWEN-
TO SH. 25
ON-
TO SH. 3
PWRON
RFCLK
TO SH. 3
BRWRON
TO SH. 3,16
PWRON-
TO SH. 5
RFCYC-
TO SH. 3,4,5,15,17
ASRFR
TO SH. 4
REFRESH-
ADDA-
ADD(00-06)-
TO SH. 7,15
LS393
V4
ADD06-
ADD05-
ADD04-
ADD03-
ADD02-
ADD01-
ADD00-
ADDA-
RFCYC
TO SH. 4,15
TEXAS INSTRUMENTS
D 96214
2261992
B

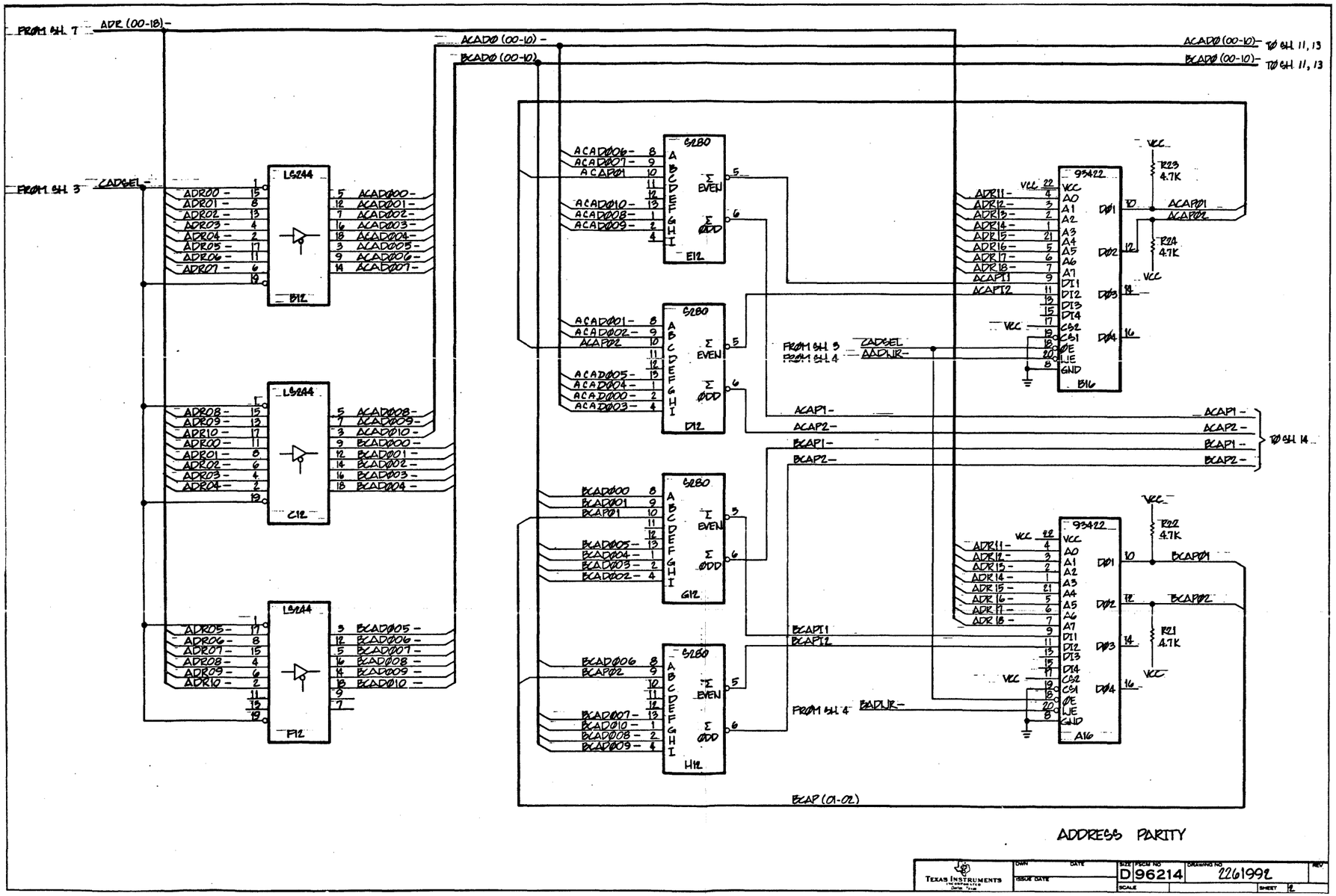

INIT CKT, ADDRESS BUFFERS
TEXAS INSTRUMENTS
D 96214
2261992
B

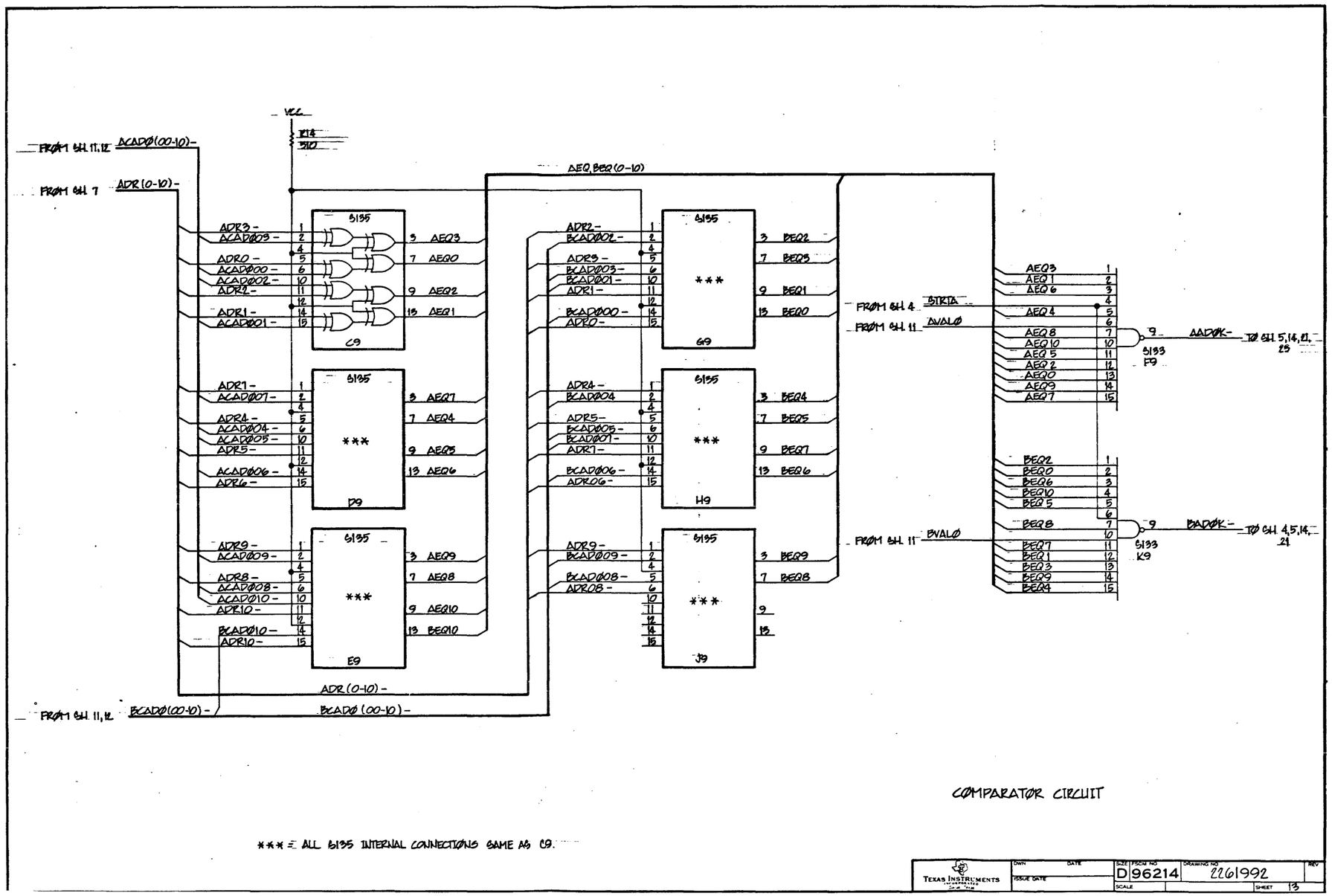

FROM SH 7 LADR (11-18) -
FROM SH 12 CDB (0-15)
ACD∅ (0-15)
LADR (11-18)
CDB (0-15)
ACD∅ (0-15) TO SH. 14,21,10
BANK A EVEN
93422
BANK A ODD
FROM SH 4 ACWRE -
ACWRE -
FROM SH 15 LADR19 -
FROM SH 5 ACBUSY -
FROM SH 5 CBUSY
TO SH 9,10
∅EEV -
∅E∅D -
ACWR∅ -
FROM SH 4 ACWR∅ -
DATA RAMS (1 OF 2)
TEXAS INSTRUMENTS
D 96214
2261992
B


FROM SH 7 LADR(11-18)-
FROM SH 22 CDB(0-15)
BCDØ(00-15)
LADR(11-18)-
CDB(0-15)
BCDØ(00-15) TO SH 14,21
FROM SH 8 ØEEV-
FROM SH 4 BCLKRE-
FROM SH 8 ØEØD-
FROM SH 4 BCLKRQ-
BANK B EVEN
BANK B ØDD
93422
A25
B25
C25
D25
E25
F25
G25
H25
J25
BCDØ00
BCDØ01
BCDØ02
BCDØ03
BCDØ04
BCDØ05
BCDØ06
BCDØ07
BCDØ08
BCDØ09
BCDØ10
BCDØ11
BCDØ12
BCDØ13
BCDØ14
BCDØ15
DATA RAMS (2OF2)
TEXAS INSTRUMENTS
DWN
DATE
ISSUE DATE
SIZE D
FSCM NO 96214
DRAWING NO 2261992
REV
SCALE
SHEET 9


FROM SH. 7 LADR(11-18)-
FROM SH. 21, 22, 23 DB(0-15)
ACD∅(00-15) TO SH. 14,21,9
BCD∅(00-15) TO SH. 14,21,9
ACDP01,02 TO SH. 14
BCDP01,02 TO SH. 16
LS240
H27
J27
C23
D23
BANK A EVEN
BANK A ODD
BANK B ∅∅D
BANK B EVEN
93422
M20
N20
K25
M25
RB 4.7K
RT 4.7K
PZ7 4.7K
∅EEV-
ACWE-
∅∅D-
BCWE-
ERROR
ACDP(1,2), BCDP(1,2)
DATA PARITY
TEXAS INSTRUMENTS
D 96214
2261992
B
SHEET 10


ADDRESS RAMS
BANK A
BANK B
95422
C16
G16
DG
H16
F16
J16
ADR(00-18)-
AADLIR-
CADSEL
VALIN
AVALØ
ACAD0(00-03)-
ACAD0(00-07)-
ACAD0(00-10)-
BCAD0(00-03)-
BCAD0(00-07)-
BCAD0(00-10)-
ACAD0003-
ACAD0002-
ACAD0001-
ACAD0000-
ACAD0007-
ACAD0006-
ACAD0005-
ACAD0004-
ACAD0010-
ACAD0009-
ACAD0008-
BCAD0003-
BCAD0002-
BCAD0001-
BCAD0000-
BCAD0007-
BCAD0006-
BCAD0005-
BCAD0004-
BCAD0010-
BCAD0009-
BCAD0008-
INIT
ERROR
J29
TO SH 12,13
TO SH 15
TO SH 16
FROM SH 7
FROM SH 10
FROM SH 3
FROM SH 4
Texas Instruments
D96214
2261992

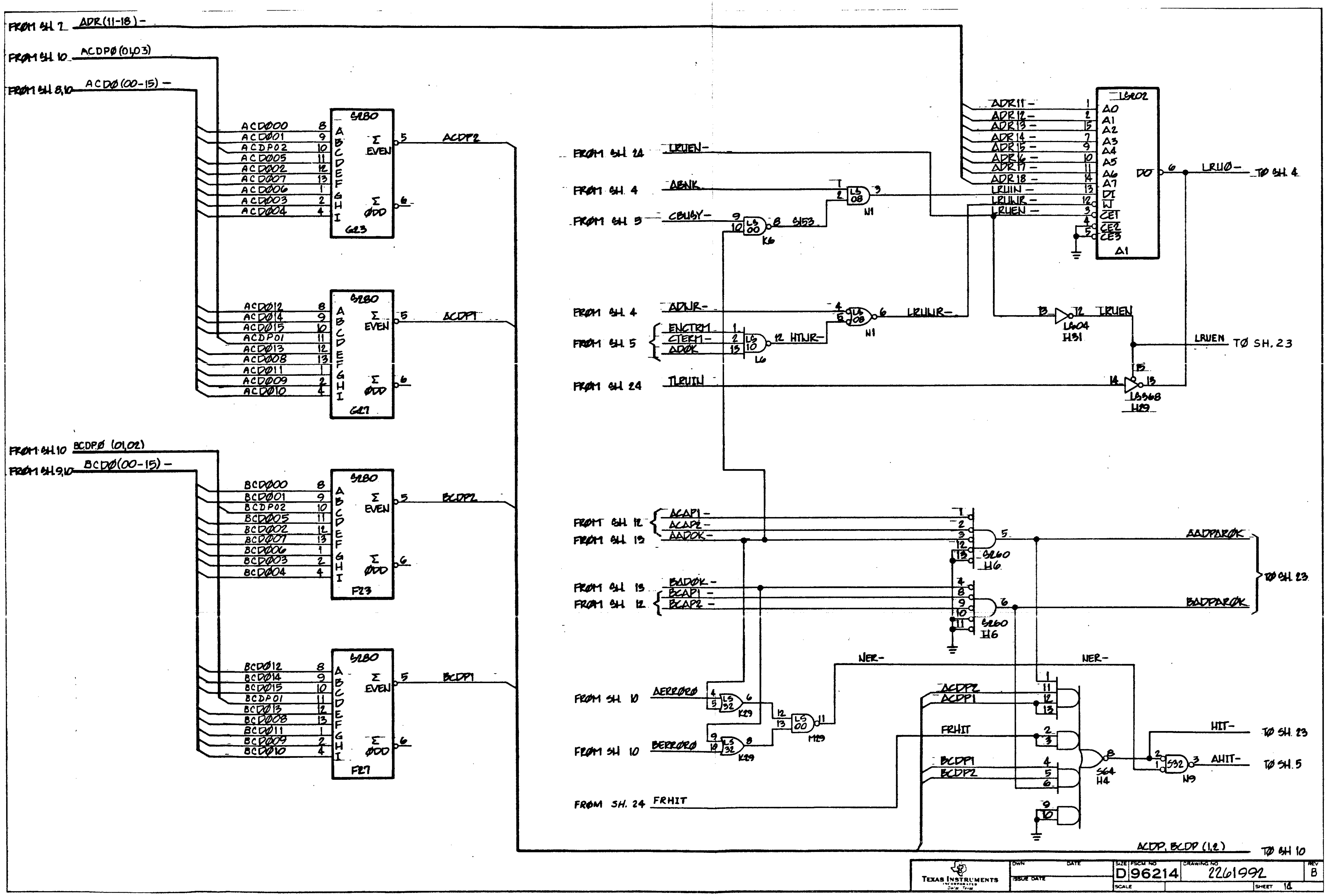

FROM SH. 7
ADR (00-18)-
ACAD0 (00-10) -
BCAD0 (00-10)-
ACAD0 (00-10)- TO SH. 11, 13
BCAD0 (00-10)- TO SH. 11, 13
FROM SH. 3
CADSEL-
LS244
B12
C12
F12
ADR00 -
ADR01 -
ADR02 -
ADR03 -
ADR04 -
ADR05 -
ADR06 -
ADR07 -
ADR08 -
ADR09 -
ADR10 -
ACAD000-
ACAD001-
ACAD002-
ACAD003-
ACAD004-
ACAD005-
ACAD006-
ACAD007-
ACAD008-
ACAD009-
ACAD010-
BCAD000-
BCAD001-
BCAD002-
BCAD003-
BCAD004-
BCAD005-
BCAD006-
BCAD007-
BCAD008-
BCAD009-
BCAD010-
S280
E12
D12
G12
H12
EVEN
ODD
ACAD006-
ACAD007-
ACAP01
ACAD010-
ACAD008-
ACAD009-
ACAD001-
ACAD002-
ACAP02
ACAD005-
ACAD004-
ACAD000-
ACAD003-
BCAD000
BCAD001
BCAP01
BCAD005-
BCAD004-
BCAD003-
BCAD002-
BCAD006
BCAP02
BCAD007-
BCAD010-
BCAD008-
BCAD009-
FROM SH. 5
FROM SH. 4
ZADSEL
ADDPAR-
BADPAR-
ACAP1-
ACAP2-
BCAP1-
BCAP2-
TO SH. 14
BCAP (01-02)
93422
A16
VCC
R23
4.7K
R24
4.7K
R22
4.7K
R21
4.7K
ADR11-
ADR12-
ADR13-
ADR14-
ADR15-
ADR16-
ADR17-
ADR18-
ACAP11
ACAP12
ADDRESS PARITY
TEXAS INSTRUMENTS
D96214
2261992

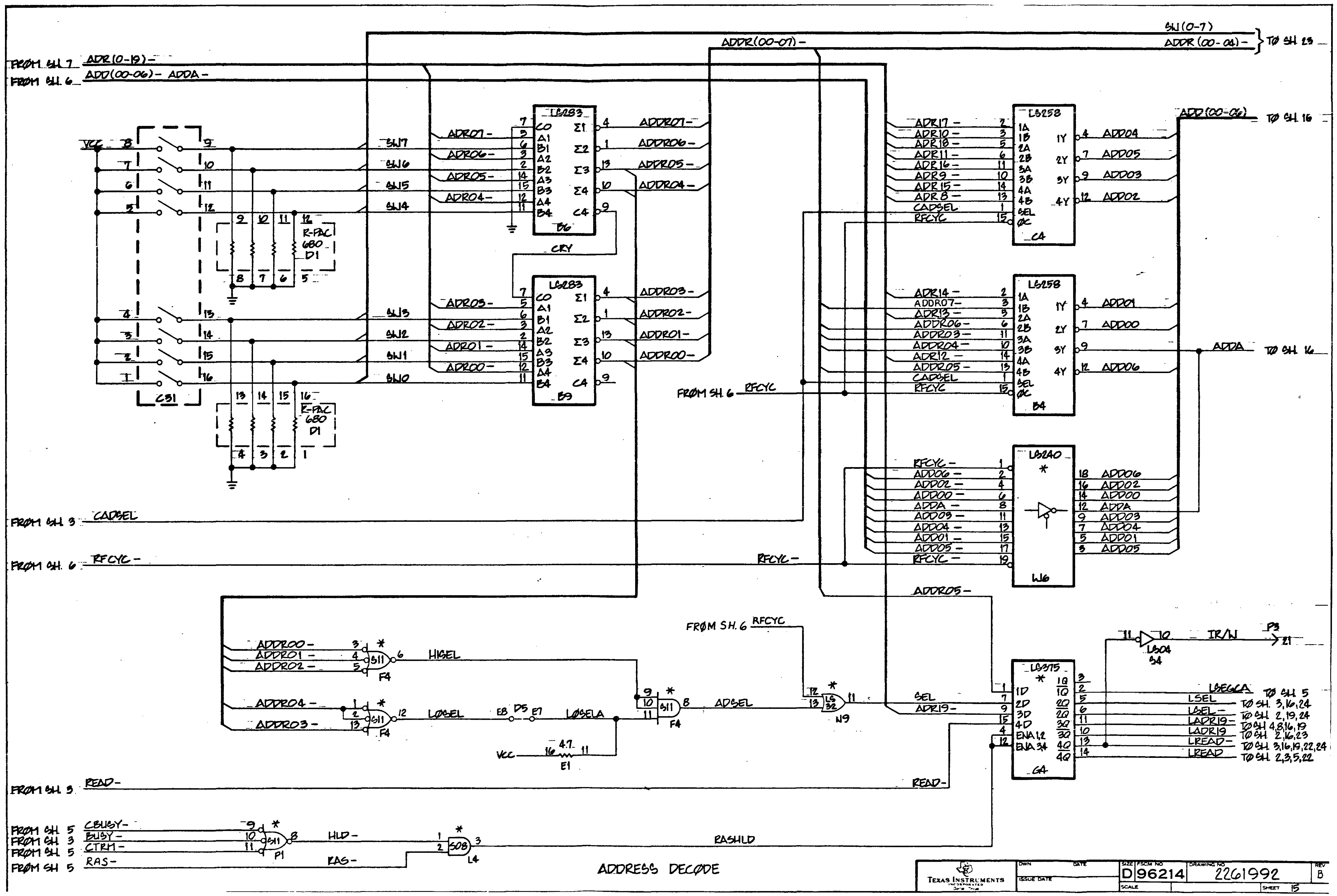


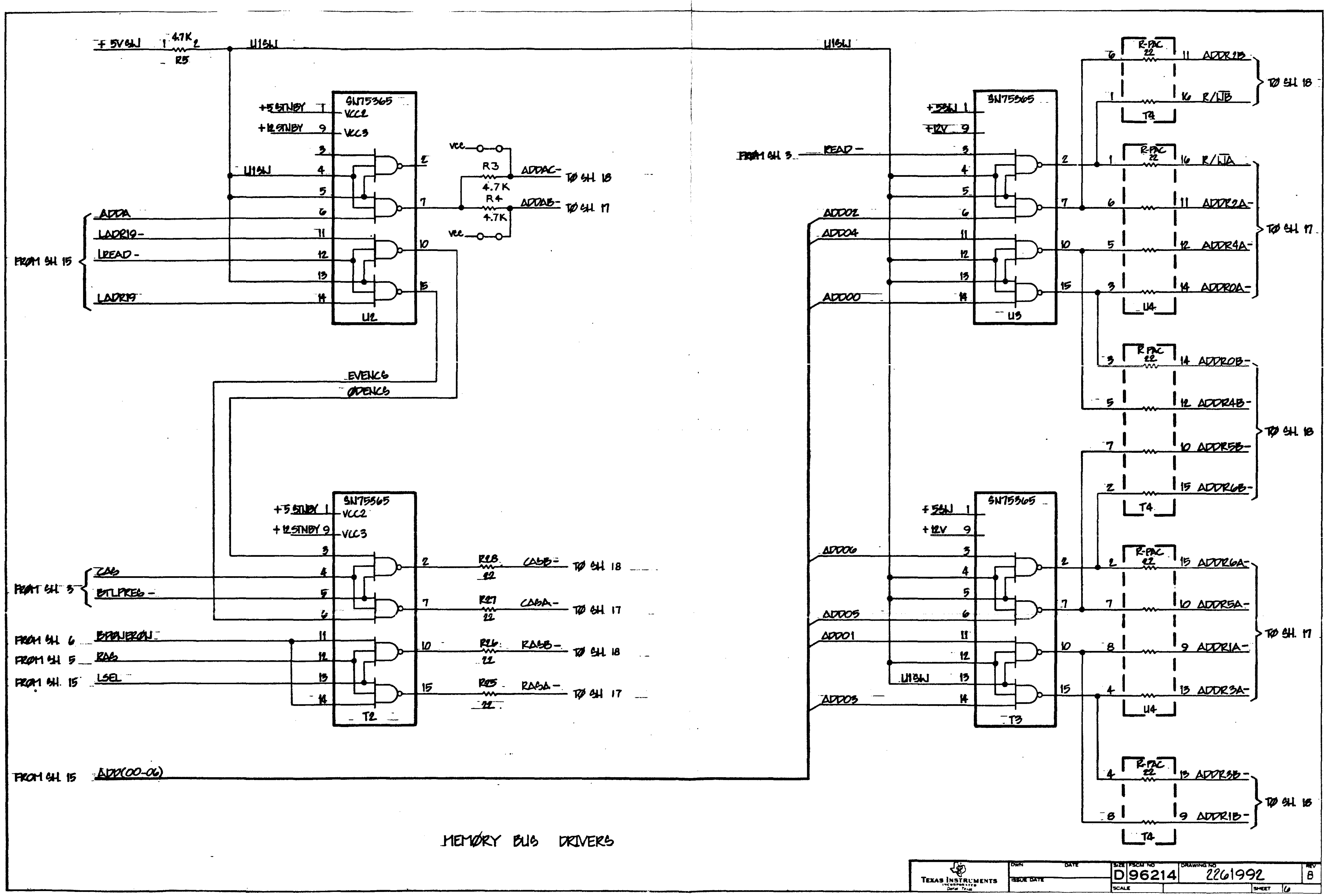
COMPARATOR CIRCUIT

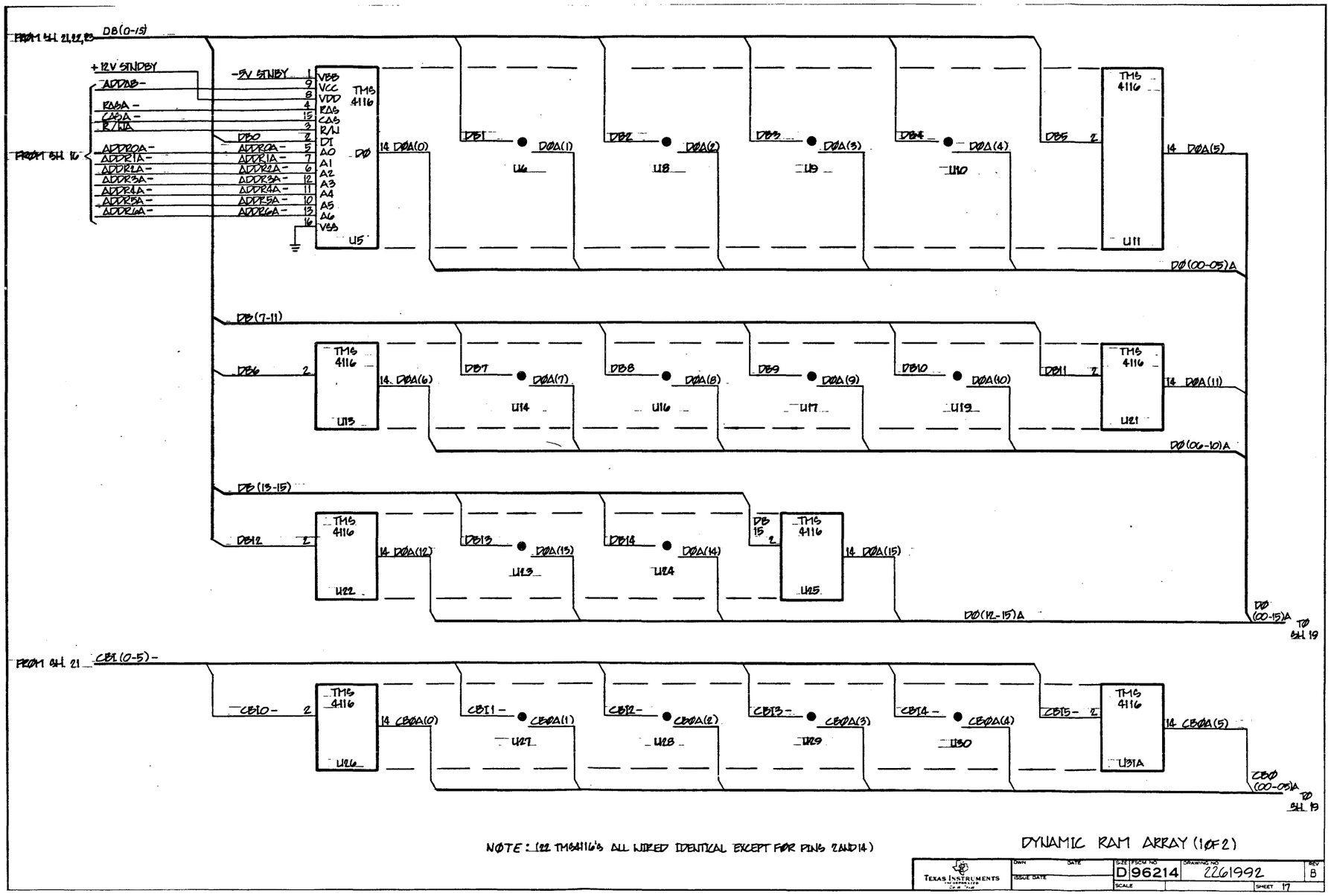
*** = ALL 6135 INTERNAL CONNECTIONS SAME AS C9.

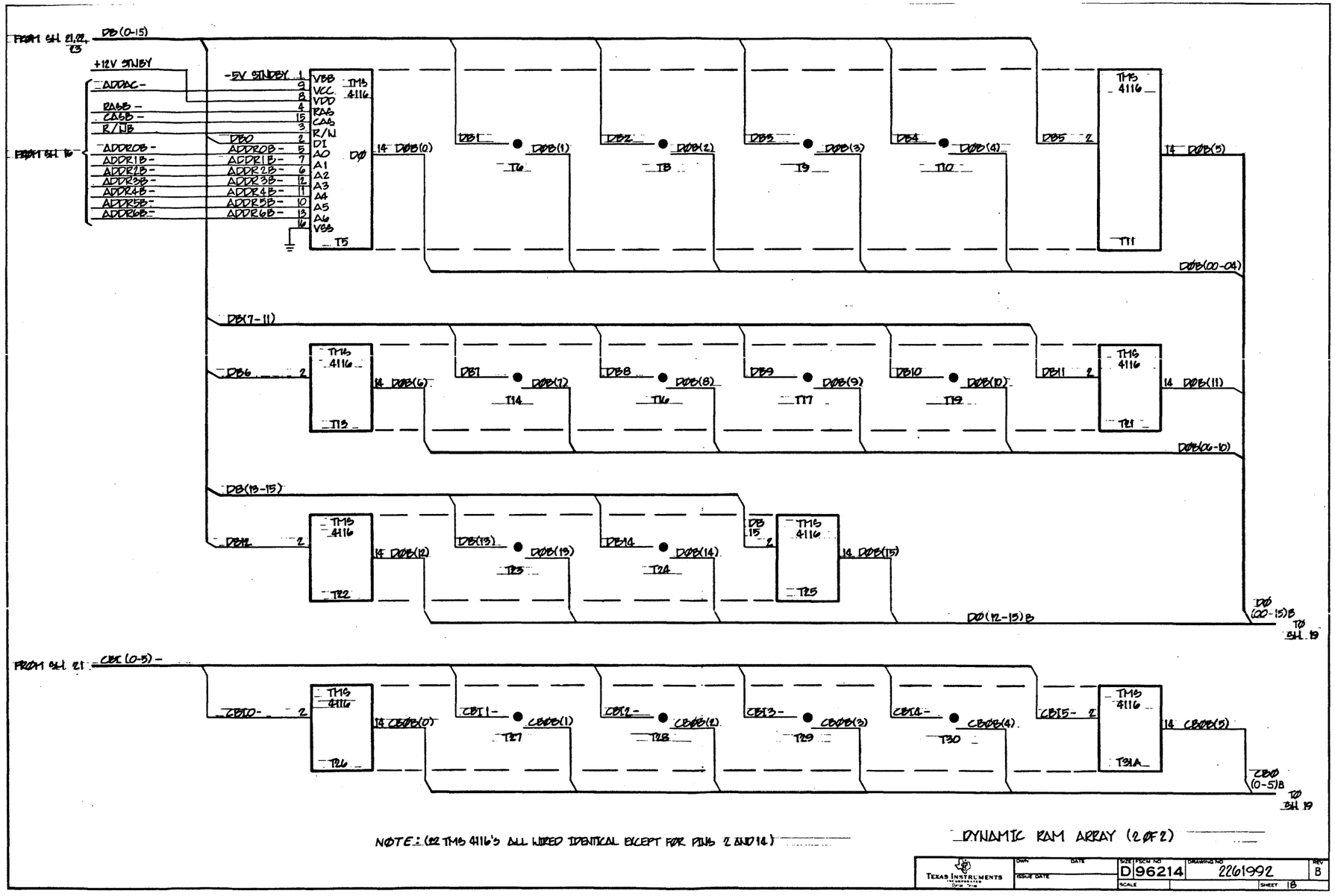
TEXAS INSTRUMENTS	DWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
	ISSUE DATE		D	96214	2261992	
			SCALE		SHEET 13	

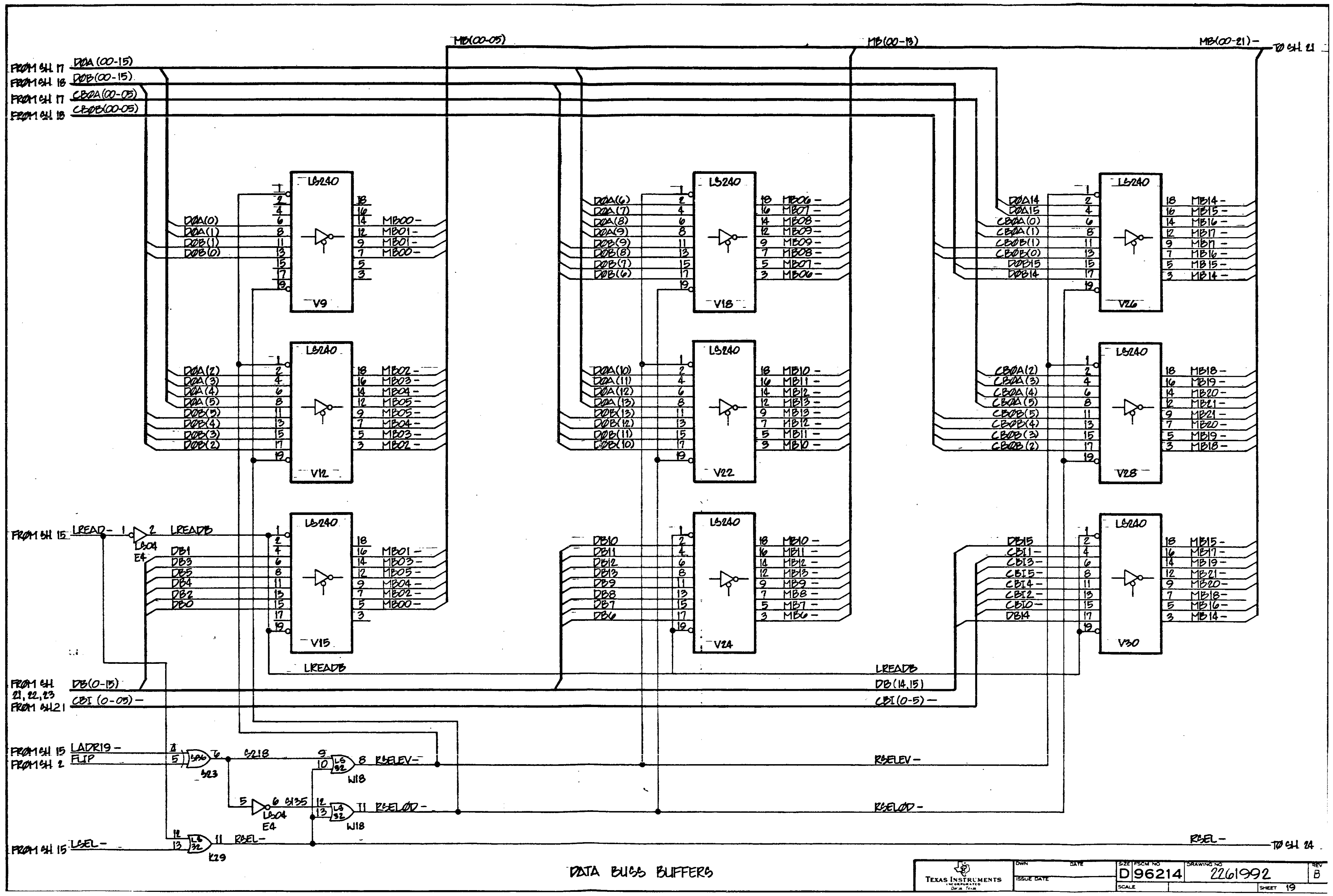

FROM SH 7 ADR(11-18)-
FROM SH 10 ACDPØ(01,03)
FROM SH 8,10 ACDØ(00-15)-
FROM SH 10 BCDPØ (01,02)
FROM SH 9,10 BCDØ(00-15)-
FROM SH 24 LRUEN-
FROM SH 4 ABNK
FROM SH 5 CBUSY-
FROM SH 4 ADWR-
FROM SH 5
ENCTRM-
CTERM-
ADØK
FROM SH 24 TLRUIN
FROM SH 12
FROM SH 13
ACAP1-
ACAP2-
AADØK-
BADØK-
BCAP1-
BCAP2-
FROM SH 10 AERRORØ
FROM SH 10 BERRORØ
FROM SH. 24 FRHIT
LRUØ- TØ SH 4
LRUEN TØ SH.23
AADPARØK
BADPARØK
TØ SH 23
HIT- TØ SH 23
AHIT- TØ SH 5
ACDP, BCDP (1,2) TØ SH 10
ACDP2
ACDP1
BCDP2
BCDP1
NER-
TEXAS INSTRUMENTS
D 96214
2261992
B
SHEET 18


FROM SH 7 ADR(0-19)-
FROM SH 6 ADD(00-06)- ADDA-
SW(0-7)
ADDR(00-07)-
ADDR(00-06)-
TO SH 23
ADD(00-06)
TO SH 16
ADDA
TO SH 16
LS283
B6
B9
CRY
LS258
C4
B4
LS240
W6
C31
R-PAC
680
D1
FROM SH 6 RFCYC
FROM SH 3 CADSEL
FROM SH 6 RFCYC-
ADDR05-
FROM SH. 6 RFCYC
ADDR00-
ADDR01-
ADDR02-
ADDR04-
ADDR03-
HISEL
LOSEL
LOSELA
ADSEL
F4
N9
SEL
ADR19-
VCC
E1
LS175
G4
LS04
S4
TR/W
P3
LSEGA
LSEL
LSEL-
LADR19-
LADR19
LREAD-
LREAD
TO SH 5
TO SH 3,16,24
TO SH 2,19,24
TO SH 4,8,16,19
TO SH 2,16,23
TO SH 3,16,19,22,24
TO SH 2,3,5,22
FROM SH 3 READ-
READ-
FROM SH 5 CBUSY-
FROM SH 3 BUSY-
FROM SH 5 CTRM-
FROM SH 5 RAS-
HLD-
RAS-
P1
L4
RASHLD
ADDRESS DECODE
TEXAS INSTRUMENTS
D 96214
2261992
B
SHEET 15


MEMORY BUS DRIVERS
SN75365
U2
U3
T2
T3
U4
T4
R-PAC
ADDAC-
ADDAB-
EVENCS
ODDENCS
ADD(00-06)
TEXAS INSTRUMENTS
D 96214
2261992
B


FROM SH 21,22,23 DB(0-15)
+12V STNDBY
-5V STNDBY
ADDØB-
RASA-
CASA-
R/WA
FROM SH 16
ADDØA-
ADDR1A-
ADDR2A-
ADDR3A-
ADDR4A-
ADDR5A-
ADDR6A-
DBO
ADDR7A-
ADDR1A-
ADDR2A-
ADDR3A-
ADDR4A-
ADDR5A-
ADDR6A-
VBB
VCC
VDD
RAS
CAS
R/W
DI
DO
A1
A2
A3
A4
A5
A6
VSS
TMS 4116
U5
14 DØA(0)
DB1
DØA(1)
U6
DB2
DØA(2)
U18
DB3
DØA(3)
U9
DB4
DØA(4)
U10
DB5
U11
14 DØA(5)
DØ(00-05)A
DB(7-11)
DB6
U13
14 DØA(6)
DB7
DØA(7)
U14
DB8
DØA(8)
U16
DB9
DØA(9)
U17
DB10
DØA(10)
U19
DB11
U21
14 DØA(11)
DØ(06-10)A
DB(13-15)
DB12
U22
14 DØA(12)
DB13
DØA(15)
U23
DB14
DØA(14)
U24
DB 15
U25
14 DØA(15)
DØ(12-15)A
DØ (00-15)A
TO SH 19
FROM SH 21 CB1(0-5)-
CB10-
U26
14 CBØA(0)
CB11-
CBØA(1)
U27
CB12-
CBØA(2)
U28
CB13-
CBØA(3)
U29
CB14-
CBØA(4)
U30
CB15-
U31A
14 CBØA(5)
CBØ (00-05)A
TO SH 19
NOTE: (12 TMS4116'S ALL WIRED IDENTICAL EXCEPT FOR PINS 2 AND 14)
DYNAMIC RAM ARRAY (1 OF 2)
TEXAS INSTRUMENTS
DWN
DATE
ISSUE DATE
SIZE D
FSCM NO 96214
DRAWING NO 2261992
REV B
SCALE
SHEET 17


FROM SH 21,22, C3
DB(0-15)
+12V STNBY
-5V STNBY
ADDAC-
RASB-
CASB-
R/WB
ADDR0B-
ADDR1B-
ADDR2B-
ADDR3B-
ADDR4B-
ADDR5B-
ADDR6B-
DB0
ADDR0B-
ADDR1B-
ADDR2B-
ADDR3B-
ADDR4B-
ADDR5B-
ADDR6B-
VBB
VCC
VDD
RAS
CAS
R/W
DI
A0
A1
A2
A3
A4
A5
A6
VBB
DO
T5
TMS 4116
DB1
DB2
DB3
DB4
DB5
T6
T8
T9
T10
T11
14 DOB(0)
DOB(1)
DOB(2)
DOB(3)
DOB(4)
14 DOB(5)
DOB(00-04)
DB(7-11)
DB6
DB7
DB8
DB9
DB10
DB11
T13
T14
T16
T17
T19
T21
14 DOB(6)
DOB(7)
DOB(8)
DOB(9)
DOB(10)
14 DOB(11)
DOB(06-10)
DB(13-15)
DB12
DB13
DB14
DB15
T22
T23
T24
T25
14 DOB(12)
DOB(13)
DOB(14)
14 DOB(15)
DO(12-15)B
DO (20-15)B
TO SH 19
FROM SH 21
CBC(0-5)
CBD0-
CBD1-
CBD2-
CBD3-
CBD4-
CBD5-
T26
T27
T28
T29
T30
T31A
14 CBOB(0)
CBOB(1)
CBOB(2)
CBOB(3)
CBOB(4)
14 CBOB(5)
CBO (0-5)B
TO SH 19
NOTE: (12 TMS 4116's ALL WIRED IDENTICAL EXCEPT FOR PINS 2 AND 14)
DYNAMIC RAM ARRAY (2 OF 2)
TEXAS INSTRUMENTS
DWN
DATE
ISSUE DATE
SIZE
FSCM NO
D
96214
DRAWING NO
2261992
REV
B
SCALE
SHEET
18


FROM SH 17 DØA (00-15)
FROM SH 18 DØB (00-15)
FROM SH 17 CBØA(00-05)
FROM SH 18 CBØB(00-05)
MB(00-05)
MB(00-13)
MB(00-21) - TO SH 21
LS240
V9
V12
V15
V18
V22
V24
V26
V28
V30
FROM SH 15 LREAD-
LREADB
FROM SH 21, 22, 23 DB(0-15)
FROM SH 21 CBI (0-05) -
DB(14,15)
CBI(0-5) -
FROM SH 15 LADR19 -
FROM SH 2 FLIP
RSELEV -
RSELØD -
FROM SH 15 LSEL -
RSEL - TO SH 24
DATA BUSS BUFFERS
TEXAS INSTRUMENTS
D 96214 2261992 B
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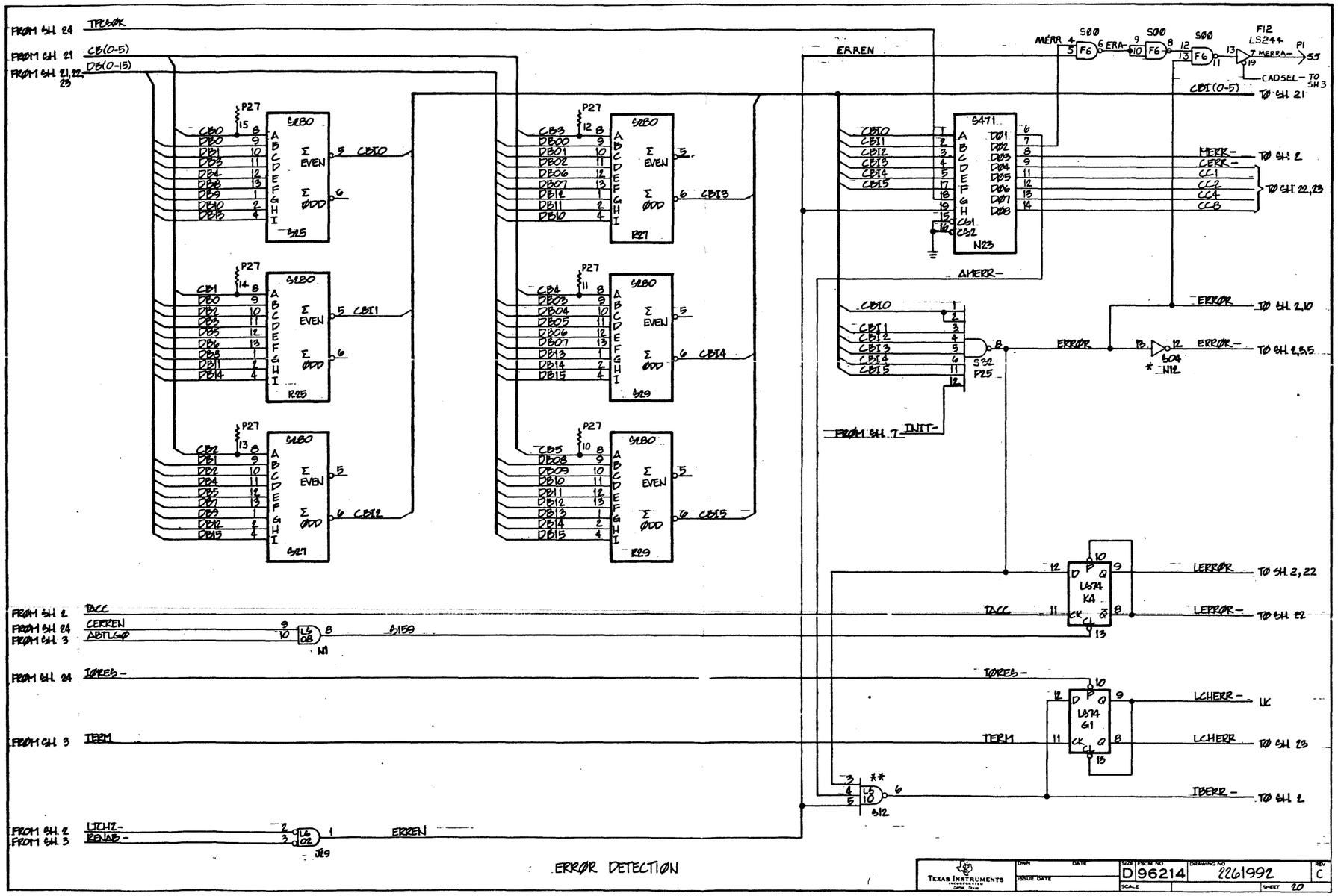
FROM SH 24 TPEROK
FROM SH 21 CB(0-5)
FROM SH 21,22, 23 DB(0-15)
ERREN
MERR
S00
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LS244
P1
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ERA-
MERRA-
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CERR- TO SH 2
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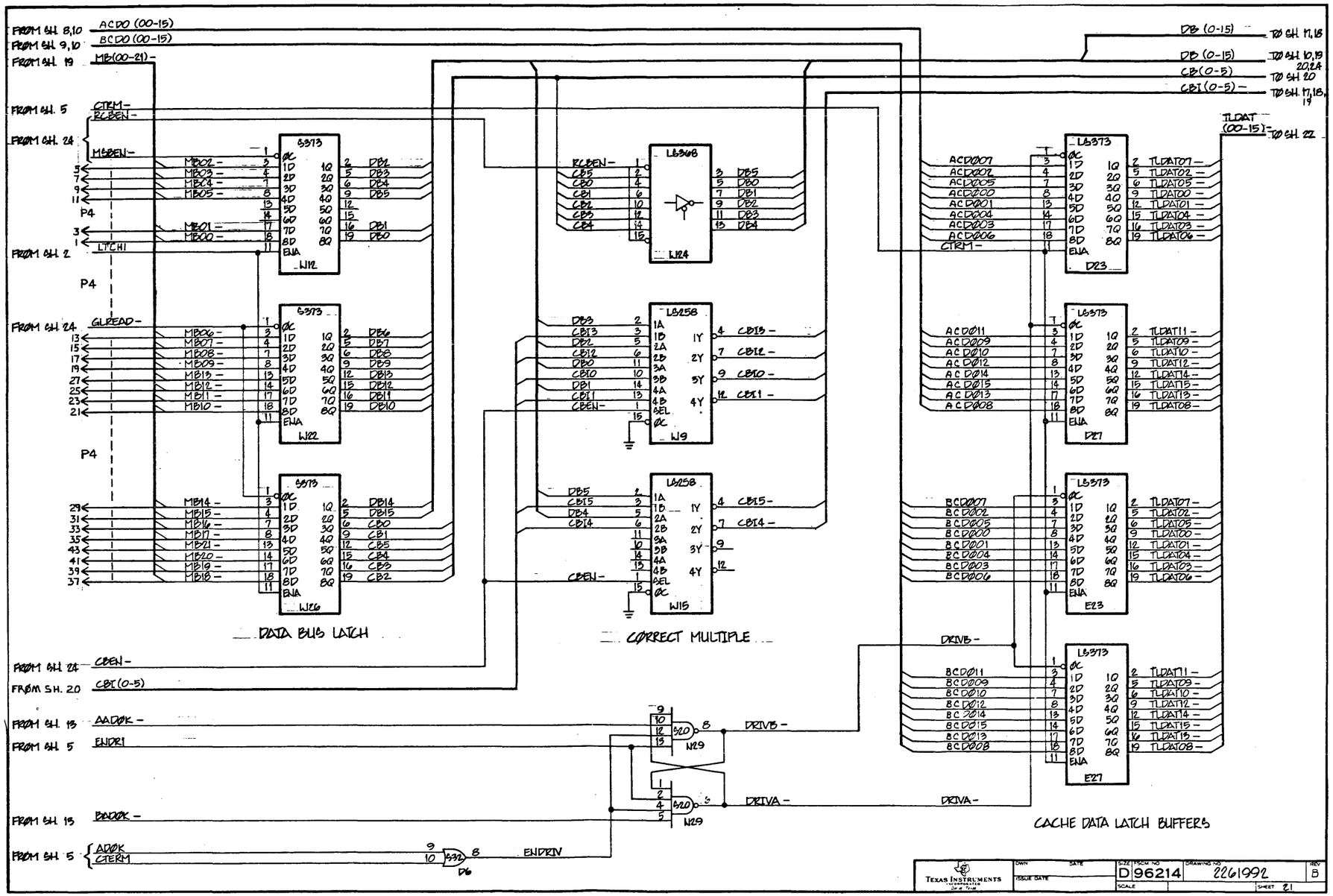
FROM SH 8,10 ACDO (00-15)
FROM SH 9,10 BCDO (00-15)
FROM SH 19 MB(00-21)-
FROM SH. 5 CTRM-
RCBEN-
FROM SH. 24 MSBEN-
FROM SH. 2 LTCHI
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TLDAT (00-15)- TO SH 22
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FROM SH. 20 CBI(0-5)
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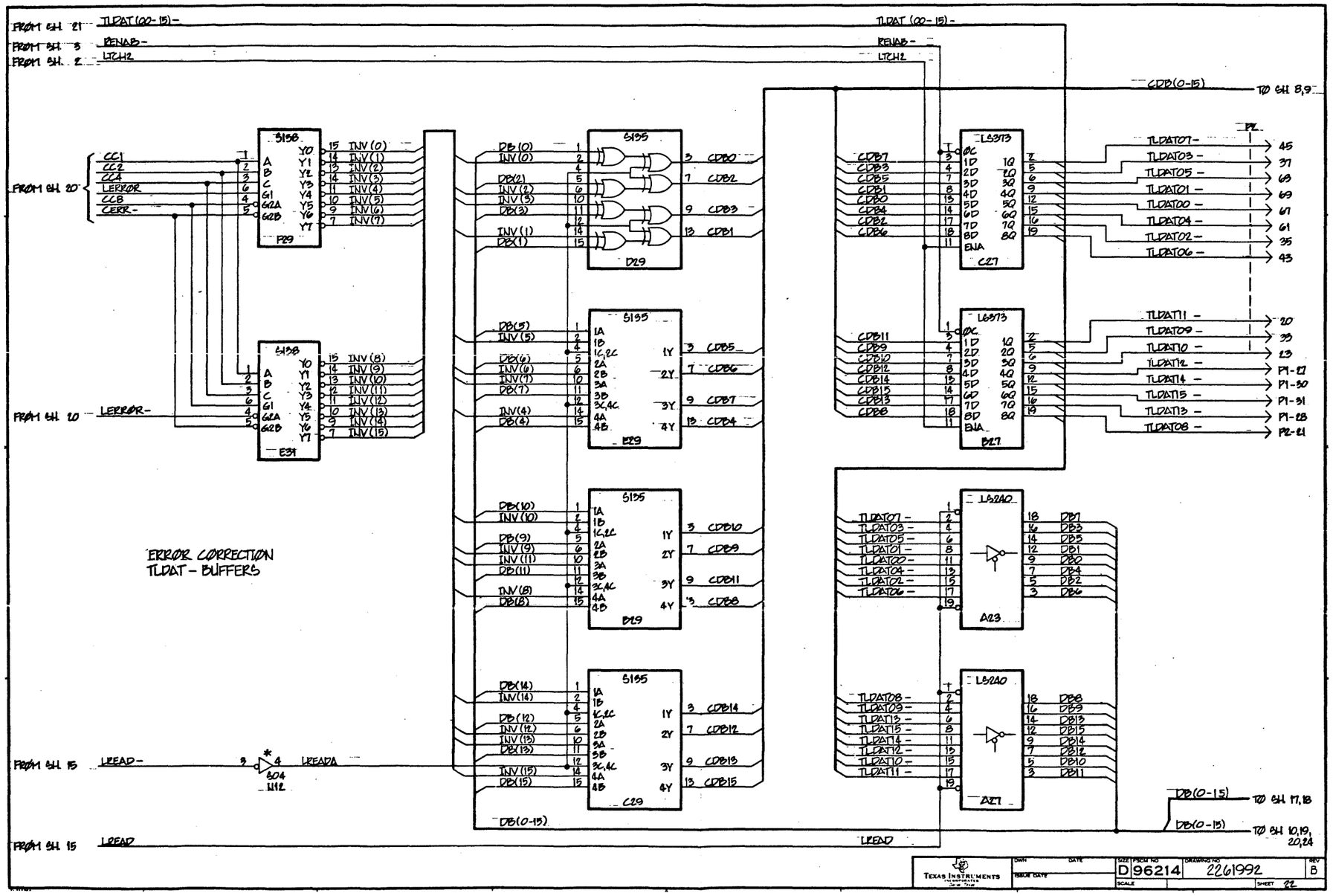
FROM SH 21 TLDAT(00-15)-
FROM SH 3 RENAB-
FROM SH 2 LTCH2
TLDAT(00-15)-
RENAB-
LTCH2
CDB(0-15)
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INV(9)
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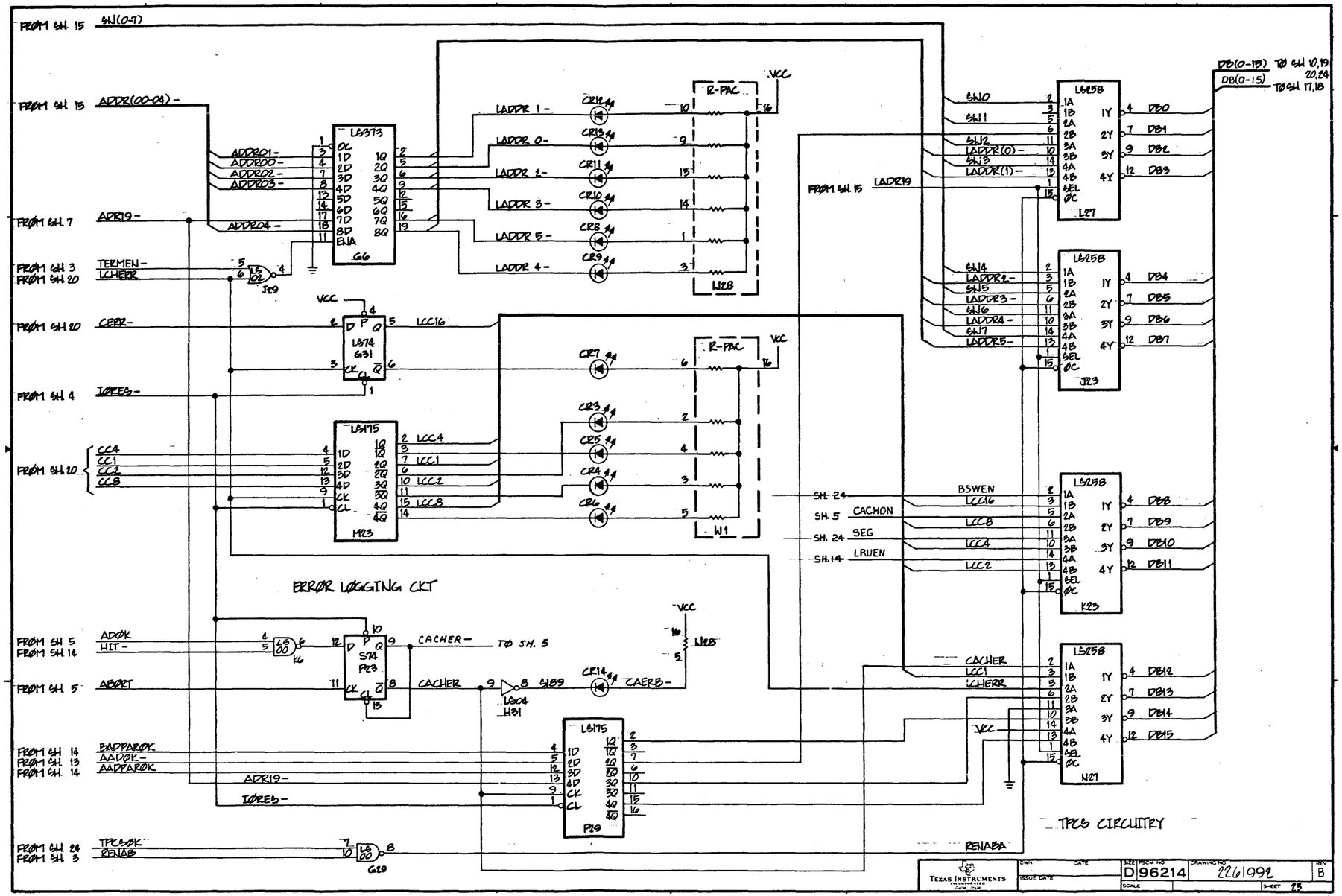
FROM SH. 15 SW(0-7)
FROM SH. 15 ADDR(00-04)-
FROM SH. 7 ADR19-
FROM SH. 3 TERMEN-
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FROM SH. 20 CERR-
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LS175 M23
LCC4 LCC1 LCC2 LCC8
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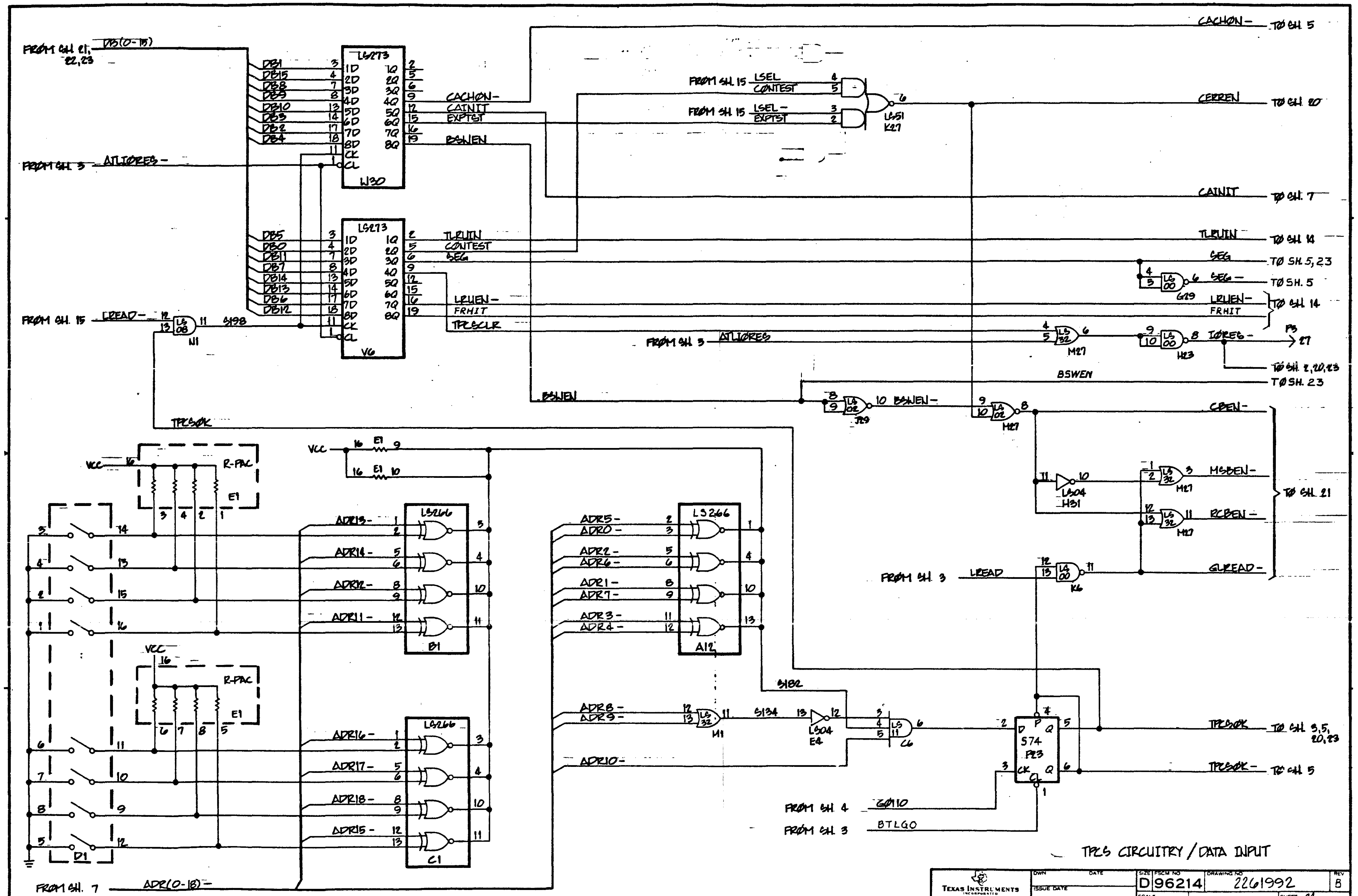

TPCS CIRCUITRY / DATA INPUT
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TPCSOK-
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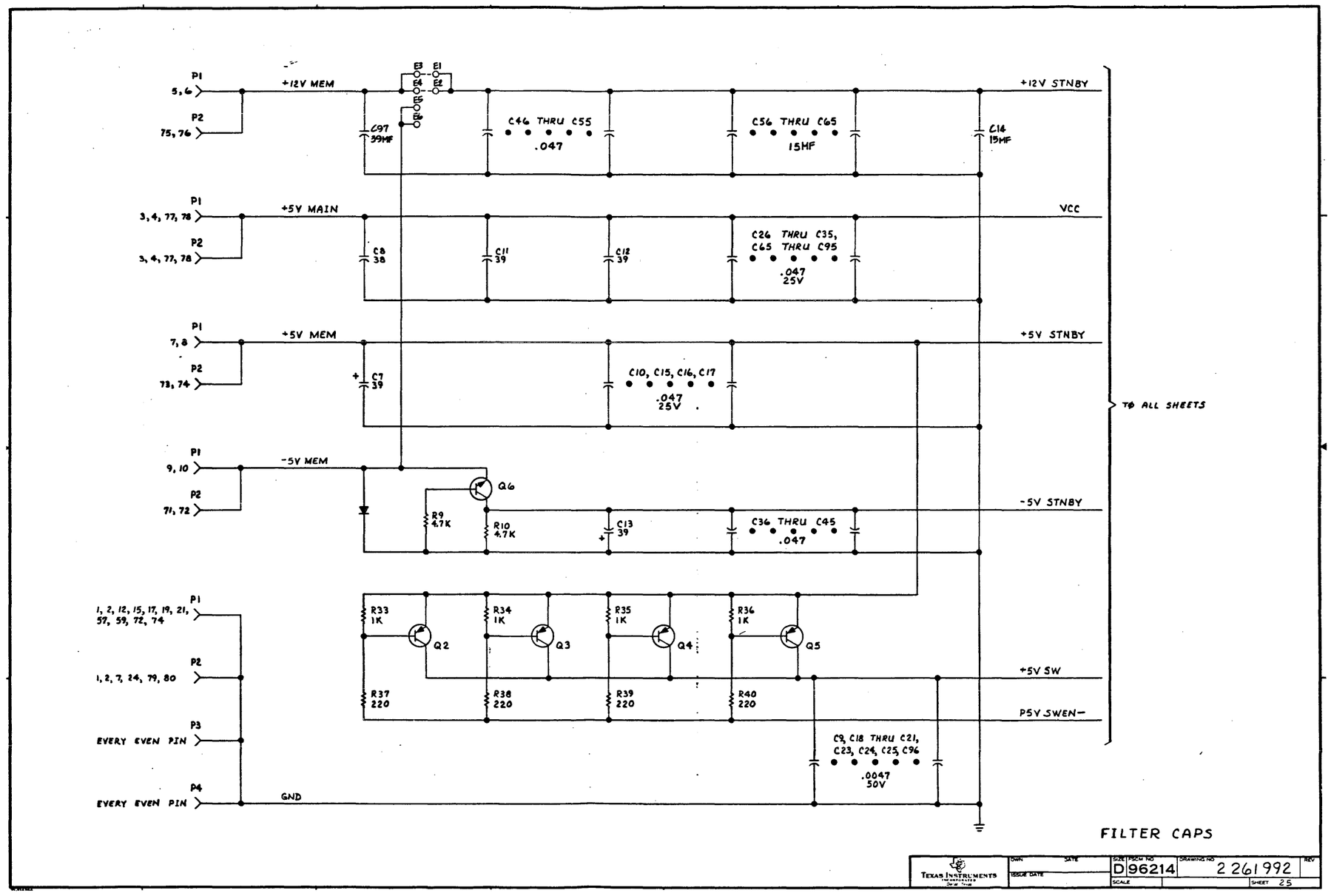
P1
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R35
1K
R36
1K
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Alphabetical Index

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HOW TO USE INDEX

The index, table of contents, list of illustrations, and list of tables are used in conjunction to obtain the location of the desired subject. Once the subject or topic has been located in the index, use the appropriate paragraph number, figure number, or table number to obtain the corresponding page number from the table of contents, list of illustrations, or list of tables.

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The following index lists key words and concepts from the subject material of the manual together with the area(s) in the manual that supply major coverage of the listed concept. The numbers along the right side of the listing reference the following manual areas:

- Sections — Reference to Sections of the manual appear as "Sections x" with the symbol x representing any numeric quantity.

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- Paragraphs — Reference to paragraphs of the manual appear as a series of alphanumeric or numeric characters punctuated with decimal points. Only the first character of the string may be a letter; all subsequent characters are numbers. The first character refers to the section or appendix of the manual in which the paragraph may be found.

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  Tx-yy

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  Fx-yy

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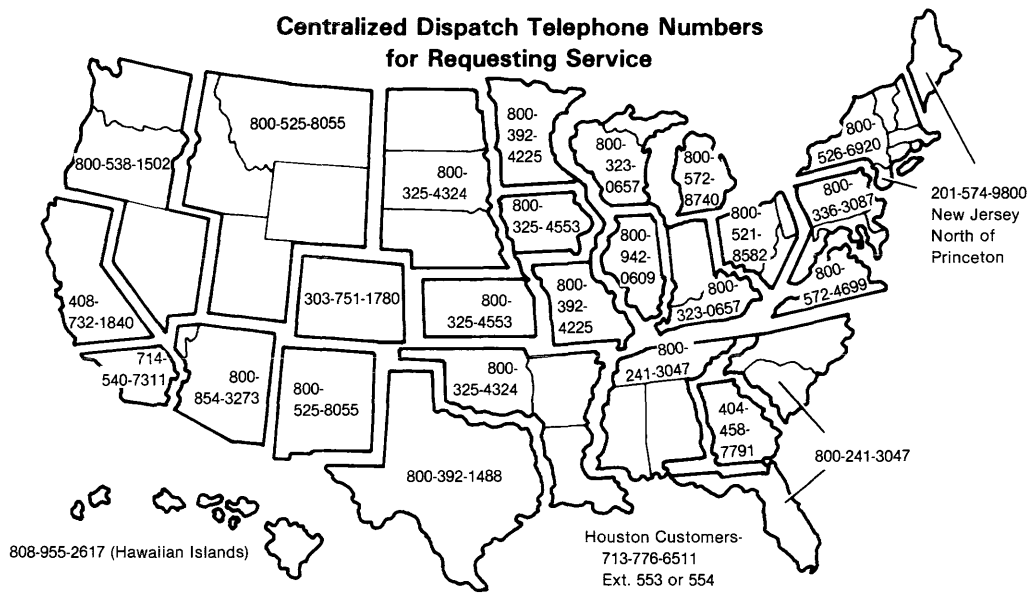

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