

TEXAS INSTRUMENTS

Improving Man's Effectiveness Through Electronics

Model 960/980 Computers Direct Memory Access Channel Controller Manual

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Digital Systems Division



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SECTION I

INTRODUCTION

1-1 SCOPE OF MANUAL.

This manual contains a general introduction to the device controllers for the Direct Memory Access (DMA) subsystem of the Texas Instruments (TI) Model 960 and Model 980 series computers. A brief description of the installation, maintenance, and operation of the DMA controllers is provided as a convenience to the customer. A typical functional configuration is illustrated in Figure 1-1.

1-2 STANDARD DEVICE CONTROLLERS.

The two computer systems (Model 980 and Model 960 series) currently utilize the following DMA device controllers:

- a. Line Printer
- b. Magnetic Tape Transport
- c. Moving Head Disc
- d. Fixed Head Disc

These device controllers and the devices which are controlled by these controllers are described in subsequent sections of this manual. Figure 1-2 is an illustration of the Input/Output (I/O) expansion chassis.

These device controllers constitute the present standard line fully supported by hardware and software.

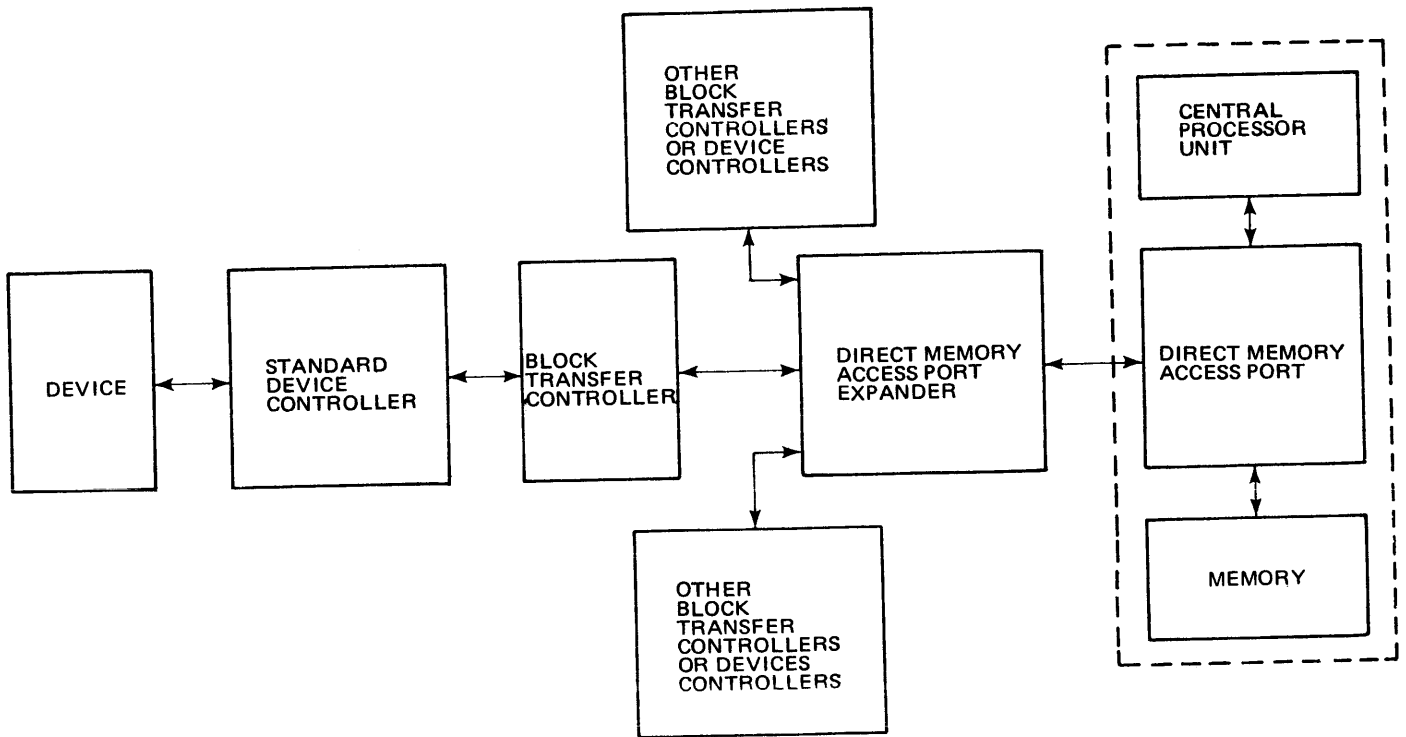
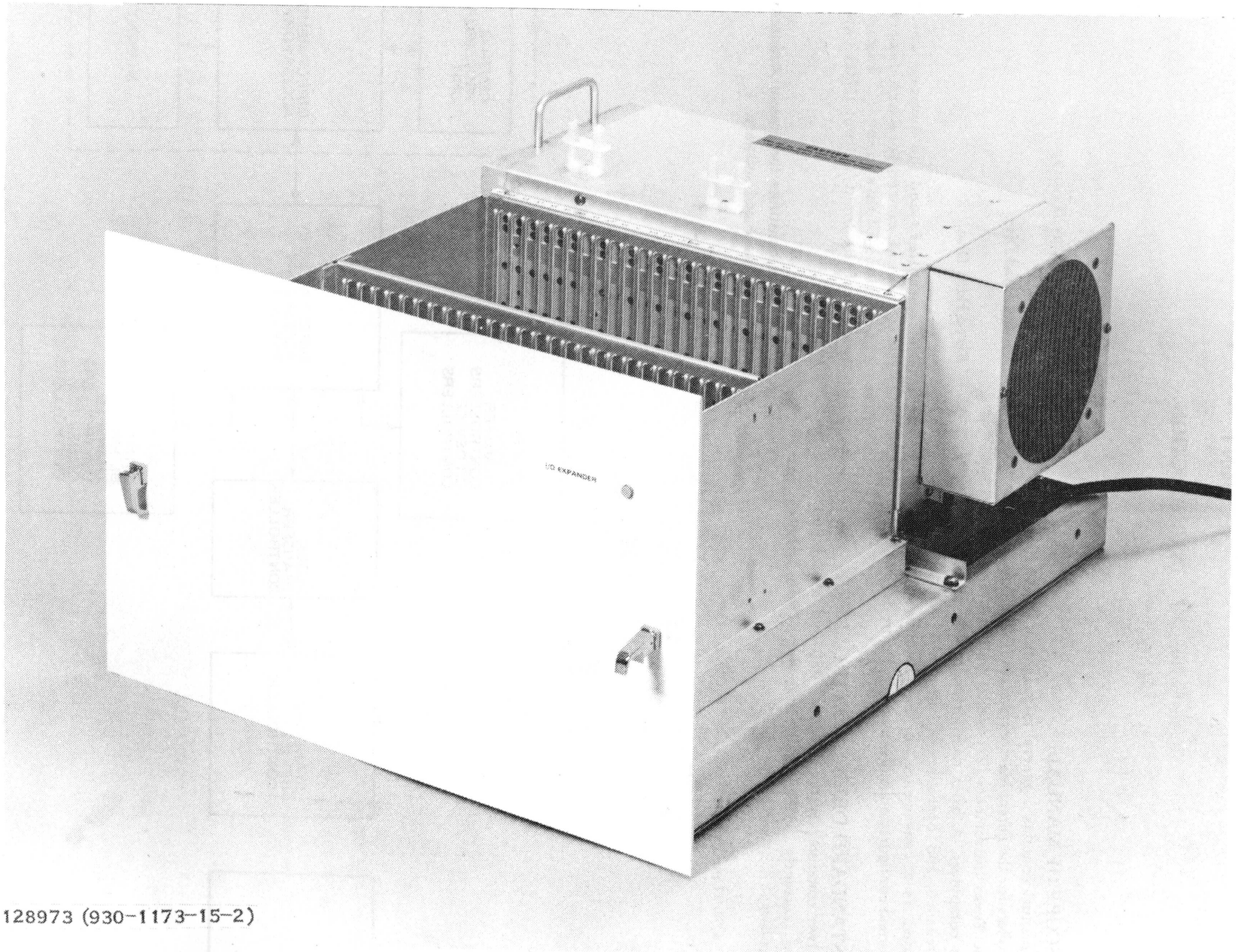


FIGURE 1-1. PERIPHERAL DEVICE, CONTROLLER, AND CENTRAL PROCESSOR
RELATIONSHIP FUNCTIONAL DIAGRAM



128973 (930-1173-15-2)

FIGURE 1-2. I/O EXPANDER CHASSIS

1-3 BLOCK TRANSFER CONTROLLER.

All device controllers must complete the interface to the memory system through the DMA bus, accept activate commands, and store status and data. Therefore, the bidirectional device controllers, which include the tape and disc controllers, use a section of logic called the Block Transfer Controller (BTC) for implementing these functions. A BTC consists of either three multilayer printed circuit boards or three wire-wrapped circuit boards as shown in Figure 1-3. The BTC is described in detail in Section II of this manual.

The line printer controller is only used as an output device; therefore, this controller is not implemented with the BTC.

1-4 INSTALLATION.

A typical DMA peripheral cabinet installation is illustrated in Figure 1-4. The Input/Output (I/O) expansion chassis is also rack mounted. This chassis houses all the DMA controllers. The design concept is to mount the Central Processor Unit (CPU) and I/O expansion chassis in the same cabinet. This minimizes the interface cable length between these units. Cables from the I/O expansion chassis to the DMA peripherals are generally longer (4.57 to 9.14 metres; 15 to 30 feet); therefore, the peripherals generally are mounted in a separate cabinet.

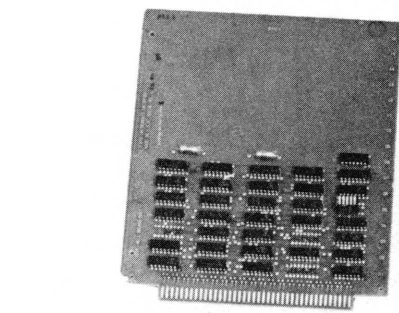
When the buyer purchases cabinets for use in a system configuration the seller (Texas Instruments) will configure and mount the buyers peripherals in the cabinet. The installation would be designed to meet all necessary electrical, mechanical and temperature (cooling) requirements.

1-5 PROGRAMMING.

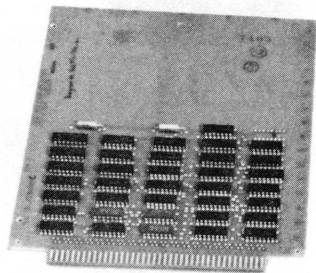
All DMA devices are fully supported by Texas Instruments documented software systems for both the Model 960 and 980 series computers. For the user of the Model 980 series computers, the "Assembly Language Input/Output" Software Instruction Manual (TI Part No. 961961-9734) is designed to introduce the user to programming techniques for DMA devices. A complete list of documents that have been prepared by Texas Instruments to support the DMAC function are listed below in Table 1-1.

1-6 MAINTENANCE.

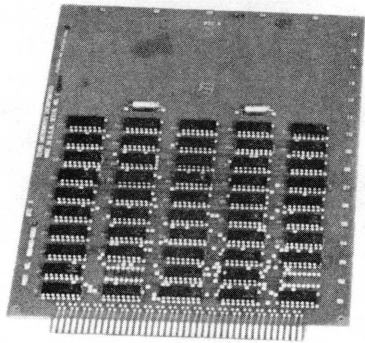
Every DMA peripheral kit is supported by an extensive Performance Demonstration Test (PDT). A PDT kit is shipped with each DMA peripheral. The kit includes a manual and a copy of the object data in card or paper tape form. The PDT manual contains operator instructions, a source listing, and flow charts. These tests are designed for performance assurance testing; however, the tests normally provide a number of diagnostic computer printouts which are designed for use as an aid during maintenance and trouble analysis.



BTC 1

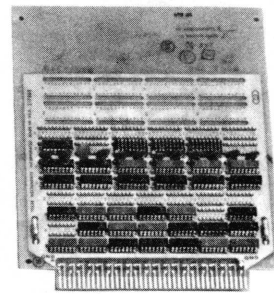


BTC 2

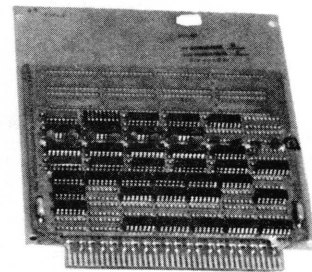


BTC 3

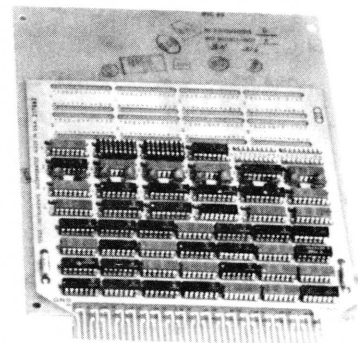
MULTILAYER PRINTED
CIRCUIT BOARDS



BTC 1



BTC 2



BTC 3

WIRE WRAP
CIRCUIT BOARDS

131410 (DSD-575-14-1)

FIGURE 1-3. BLOCK TRANSFER CONTROLLER

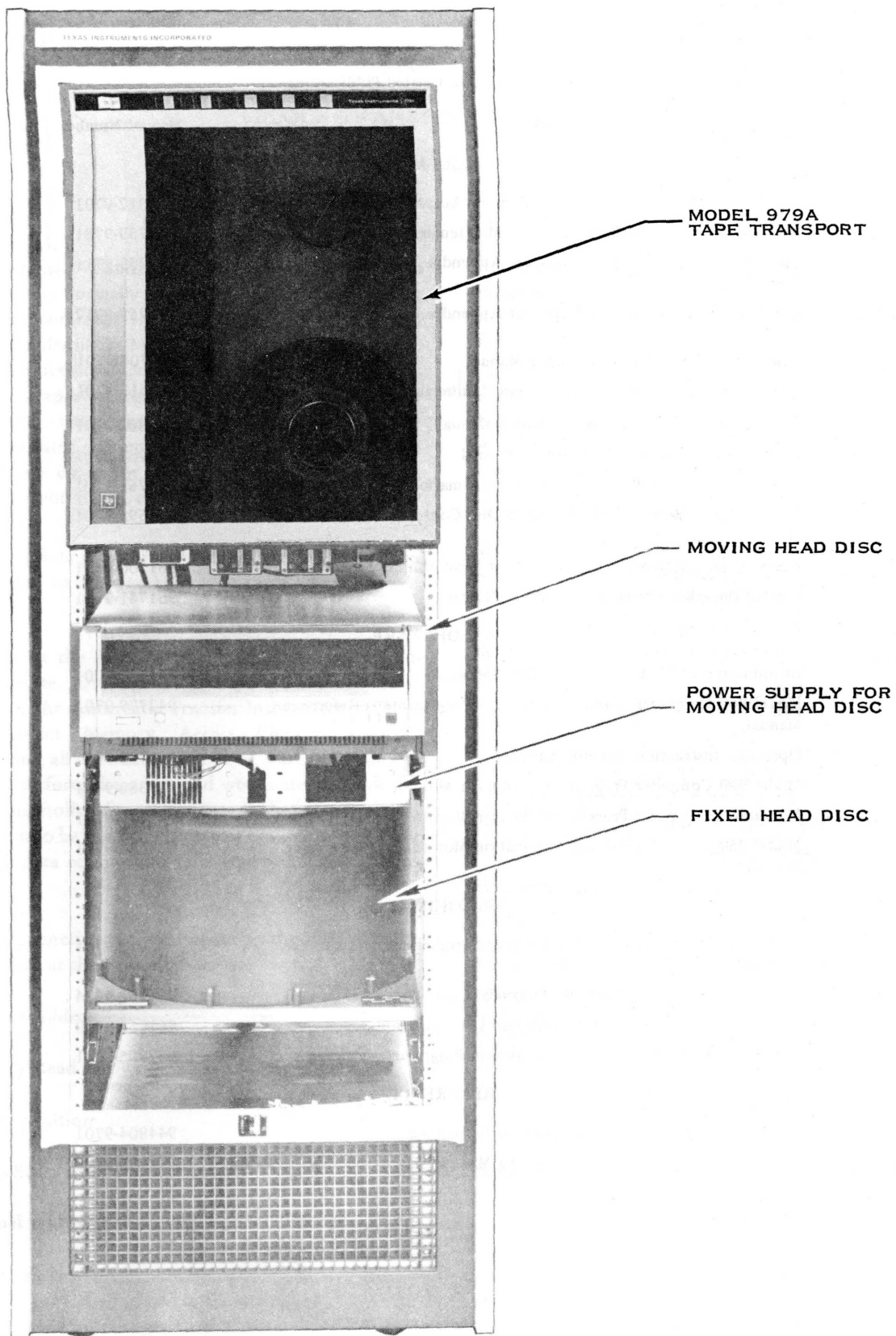


FIGURE 1-4. TYPICAL CABINET INSTALLATION OF DMA PERIPHERALS

Table 1-1. DMAC Related Publications

Title	Manual Number
HARDWARE MANUALS	
Model 960/980 Computers Direct Memory Access Channel Manual	966312-9701
Direct Memory Access Port Expander Maintenance Manual	216759-9701
Direct Memory Access Port Expander Appendix J Connector Plate 966437-0001	216759-9711
Direct Memory Access Port Expander Appendix K Connector Plate 966437-0002	216759-9712
Line Printer Controller Maintenance Manual	217704-9701
Model 979A Tape Transport Subsystem Maintenance Manual	949613-9701
Block Transfer Controller Maintenance Manual	240802-9701
DS330 Disc Controller Maintenance Manual	942764-9701
DS330 Disc System Peripheral Device Information	942765-9701
Model 31 and Model 33 Moving Head Disc Controller Maintenance Manual	961693-9701
Magnetic Disc Memory Controller Fixed Head Maintenance Manual	961700-9701
Single Controller DMAC Maintenance Manual	961741-9701
960 SOFTWARE	
Introduction to Model 960 Computer Software	942768-9701
Model 960 Computer Assembly Language Programmer's Reference Manual	942779-9701
Operating Instructions for 960 Utilities	942770-9701
Model 960 Computer Programming Support Monitor	955380-9701
Model 960 Computer Process Automation Monitor Manual	942777-9701
Model 960 Computer Process Automation Monitor/Disc Operating System	958383-9701
980 SOFTWARE	
Model 980 Computer Assembly Language Programmer's Reference Manual	943013-9701
Model 980 Computer Assembly Language Input/Output	961961-9734
Model 980 Computer Basic System Use and Operation	961961-9710
DX980 General Purpose Operating System Programmer's Guide	943005-9701
REFERENCE	
Model 980 Computer Subject Index to Manual Set	944804-9701
Model 960 Computer Subject Index to Manual Set	944825-9701

SECTION II

BLOCK TRANSFER CONTROLLER

2-1 GENERAL.

The Block Transfer Controller (BTC) provides the general controls which are normally required to complete the interface from a device controller to a Direct Memory Access Port (DMAP) Expander of the Model 960 or 980 series computers. A BTC consists of either three multilayer printed circuit boards or three wire-wrapped circuit boards as shown in Figure 1-3. The functional relationship of the BTC to these computer systems is illustrated in Figure 1-1. The BTC can operate with only one device controller at any given time; however, a maximum of eight BTC's can be connected to the DMAP expander.

The maximum data rate through the BTC is 500 kHz. The BTC is designed to use a maximum of every other available memory cycle.

The interface at the DMAP expander remains fixed from device to device. Only the logical functions of bits 8 through 12 of the Automatic Transfer Instruction (ATI) or Activate Direct Memory Access Channel (ADAC) instruction, and all 16 bits of List Word 3 are undefined to the BTC. Therefore, these bits and words are available for the device controller functions. Bits 0 through 7 of List Word 2 may also be used by the device controller providing 8 bits of the data counter are sufficient to address all data segments.

The following functions are performed by the BTC with the proper interface at the device controller.

- Memory Addressing
- Memory Read and Write Data storage and gating
- List Acquisition
- Status Store and Interrupt control
- Channel Address decoding and signal selection
- Data Counting
- DMAC signal buffering
- ATI or ADAC command monitoring

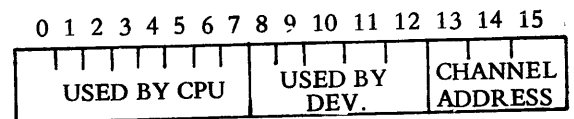
2-2 COMMAND FORMATS.

Formats for the instruction words and list words are included in this section. These are general applications for the standard device controllers, and may be used differently for other applications.

2-2.1 INSTRUCTION FORMAT. The Automatic Transfer Instruction (ATI) in the Model 980 computer and the Activate Direct Access Channel (ADAC) command in the 960 computer are the means by which a device on the Direct Memory Access Channel (DMAC) is activated.

The BTC monitors the ATI instruction from the Model 980 series or the ADAC instruction from the Model 960 series. When the device is not busy, the BTC accepts both words of the instruction and passes them to the device. When the device is busy, the BTC accepts only word 1 and passes it to the device.

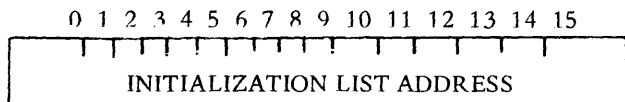
2-2.1.1 Word 1.



The device bit field consists of bits 8 through 12. From every ATI or ADAC instruction which addresses the BTC with the selected channel address in bits 13 through 15, the BTC generates a one clock time strobe (ATII) indicating the presence of a new device bit field in the memory data Buffer Register (MRD), bits 8 through 12. This strobe and bit field from the register are made available to the device controller for command decode at all times. If the instruction is received while the device controller is busy, words 1 and 2 of the instruction are not stored in the BTC register file. If the instruction is received when the device controller is not busy, word 1 is stored in the BTC Register Field 1 (RF1) and word is stored in RF3.

The channel address is located in bits 13 through 15. The BTC compares bits 13 through 15 of the ATI or ADAC instruction with a 3-bit selectable address. The BTC accepts all DMAC device signals that compare. (See Paragraph 2-3.)

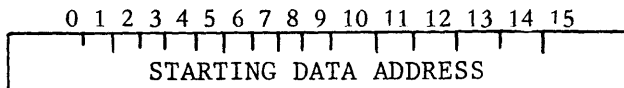
2-2.1.2 Word 2.



The second word is intended for use by the BTC list sub-controller. It is available to the device controller only during the ATI2 strobe. When receiving an ATI or ADAC command and the device controller is not busy, the BTC initialization sub-controller stores this word in RF3 of the BTC register file. The BTC list sub-controller has access to this word when activated by the device controller. The BTC list sub-controller uses this word as the starting memory address for the list words.

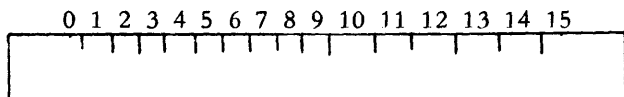
2-2.2 INITIALIZATION LIST. The list words are fetched from memory by the BTC when enabled by the device controller. A total of four words are fetched from memory starting at the memory address which is stored in register file 3 or register file 4. The list acquisition terminates after four list words.

2-2.2.1 List Word 1.



List word 1 is fetched from memory and transferred to the Register File 2 (RF2). This list word is on the device data bus during the one clock time list 1 strobe.

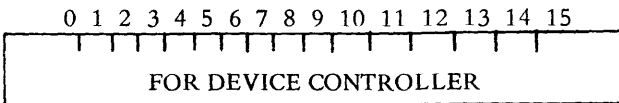
2-2.2.2 List Word 2.



List word 2 is fetched from memory and transferred to the data counter through the Register File 1 (RF1). This list word is on the device data bus during the one clock time list 2 strobe. All 16 bits from the data bus are loaded into the data counter.

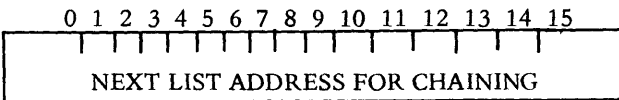
Bits 0 through 7 may be used by the device for other than a counting function because data counter zero is reported to the device for 8 and 16 bits.

2-2.2.3 List Word 3.



This list word is presented to the device controller during the list 3 strobe. The BTC selects this word for output of the register file after all list words have been fetched.

2-2.2.4 List Word 4.



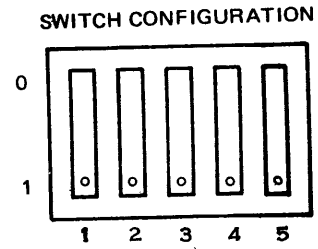
List word 4 is transferred to the BTC Register File 3 or 4 (RF3 or RF4). The BTC list sub-controller can access this word for the next list acquisition if chaining is performed. The device controller has control of the selection of RF3 or RF4. If the list sub-controller uses RF3 for the starting list address, it stores list word 4 in RF4. If RF4 is selected for the starting list address, the next list address is stored in RF3.

2-3 CHANNEL ADDRESS.

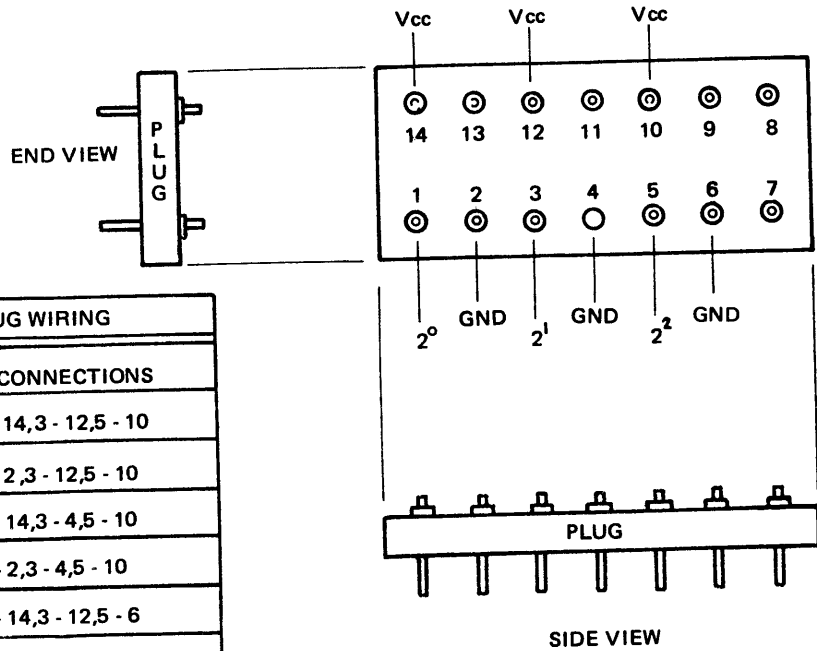
The BTC may be assigned any channel address from channel 0 through channel 7. Circuitry within the controller uses the assigned channel address to determine when to respond to an ATI or ADAC command. This circuitry also determines which request lines to drive and which acknowledge lines to monitor as explained in the following sections.

2-3.1 ADDRESS SELECTION. The channel addressing scheme permits assignment of any channel address and enables the address to be changed if desired. The assigned channel address is; wired on an address select plug as illustrated in Figure 2-1, or selected by a pencil switch as shown in the same figure. The BTC logic performs the proper decoding of the memory read data bits to test for the assigned address in activate word one.

ADDRESS SWITCH CODING					
CHANNEL SELECTED	SWITCH				
	1	2	3	4	5
0	0	0	0		
1	0	0	1	D	D
2	0	1	0	E	E
3	0	1	1	S	S
4	1	0	0	J	J
5	1	0	1	Z	Z
6	1	1	0	J	J
7	1	1	1		



MULTILAYER BOARD



ADDRESS PLUG WIRING	
CHANNEL	CONNECTIONS
0	1 - 14, 3 - 12, 5 - 10
1	1 - 2, 3 - 12, 5 - 10
2	1 - 14, 3 - 4, 5 - 10
3	1 - 2, 3 - 4, 5 - 10
4	1 - 14, 3 - 12, 5 - 6
5	1 - 2, 3 - 12, 5 - 6
6	1 - 14, 3 - 4, 5 - 6
7	1 - 2, 3 - 4, 5 - 6

WIREWRAP BOARD

NOTE: THE CHANNEL ADDRESS SWITCH IS LOCATED ON THE BTC 1 MULTILAYER BOARD IN LOCATION 505, AND ON THE BT 1 WIREWRAP BOARD IN LOCATION B00.

ONLY ONE SWITCH FOR EACH CONTROLLER.

FIGURE 2-1. CHANNEL ADDRESS SELECTION

2-3.2 ADDRESS MODIFICATION. In order to change the channel address without altering the controller logic or connector plate wiring, the controller logic picks up all channel control lines (channel 0 through channel 7) that concern memory access and interrupts. However, only one line of each group is used. That selected line is determined by the assigned channel address and select logic in the BTC.

2-4 MEMORY ACCESS CYCLE.

The BTC must issue a request for memory access and must wait until a memory access granted is received. The time elapsing between a request and receiving granted is dependent on CPU activity, the expander, other device controllers, and the channel address assigned to this controller.

2-5 INTERRUPTS AND STATUS.

The BTC interrupts the program being executed by the CPU and causes the controller status to be processed when enabled by the device controller.

When the status enable pulse (STATEN-) is sent by the device controller with the interrupt enabled True (INTEN-), the BTC status controller issues an interrupt request to the DMAP expander and the CPU. The BTC then waits until an interrupt acknowledge is received before taking further action. The interrupt recognition signal is sent when the DMAC interrupt bit in the CPU status register is armed and a Store Status Block (SSB) command has been executed.

Receiving an interrupt acknowledge enables the controller to proceed with status storage through the memory access request sequence. If interrupts have been disabled, the controller proceeds with status storage as soon as (STATEN-) is received.

2-5.1 RESERVED STATUS LOCATIONS. Locations in both the Model 960 and Model 980 series computers are reserved for status information storage as noted below.

Hexadecimal Location	DMAC Channel
96	Expander
98,99	Channel 0
9A,9B	Channel 1
9C,9D	Channel 2
9E,9F	Channel 3
A0,A1	Channel 4
A2,A3	Channel 5
A4,A5	Channel 6
A6,A7	Channel 7

The preceding channel address scheme also enables the controller to store controller status in the proper location depending on the assigned channel address.

2-5.2 STATUS WORDS. The BTC stores one or two status words. The first status word is taken from the device data bus (RFOUT). The memory address is a function of the selected device address in the BTC. The address for status word 1 is always even. The second status word is either RF3 or RF4 (whichever contains the starting list address for the operation which generated the status), or it will be the data counter which contains the remaining data count at the time the status occurred. The selection of the number of words and the second word is controlled by the device controller. The status store cycle has a memory access priority within the BTC. Refer to the Block Transfer Controller Maintenance Manual (TI Part No. 240802-9701) for additional details.

2-6 BLOCK TRANSFER CONTROLLER CHARACTERISTICS.

All major block transfer controller characteristics are listed in Table 2-1.

TABLE 2-1. BLOCK TRANSFER CONTROLLER CHARACTERISTICS

CHARACTERISTIC	SPECIFICATION
PHYSICAL	Consists of series 74N TTL integrated circuits that are installed on three cards. Cards are installed in a wire wrap card connector plate.
ENVIRONMENTAL: Temperature	Operating range of 0° to 70°C (32° to 158°F). Storage range of -40° to +100°C (-40° to 212°F).
Humidity	Fully operational at 5 to 85% relative humidity (no condensation). Storage environment shall be 5 to 95% relative humidity (no condensation).
Pressure	Operational and storage, barometric pressure, shall be from 508 to 813 mm (20 to 32 in.) of mercury.
RELIABILITY: Mean time between failure Mean time between repair	Approximately 16,000 hours Mean time to isolate failure and repair same is two hours.
POWER	5.0V ±0.1Vdc at 2 A.

SECTION III

LINE PRINTER CONTROLLER

3-1 GENERAL.

The line printer controller is designed for use with the Data Products Corporation Line Printer, Model 2310. The controller is compatible with the 2400 series printers; however, this controller does not support the optional forms control that is available with the 2400 series printers.

The 2310 line printer features 80-column printing in segments of 20 characters (i.e., the line printer unit contains a 20-character buffer which drives the print hammers).

The character set consists of 64 alphanumeric and symbolic characters and 3 control characters. The line printer accepts ASCII coded characters which are supplied from the Central Processor Unit (CPU) and by the software. The line printer controller performs no coding of data to the printer unit.

The printing speed of the line printer for the 64-character drum (rotating speed 1760 rpm) is determined by the number of segments to be printed for each line. The minimum printing speed is specified by the manufacturer for the line print widths as specified in Table 3-1.

TABLE 3-1. LINE PRINTER PRINTING SPEEDS

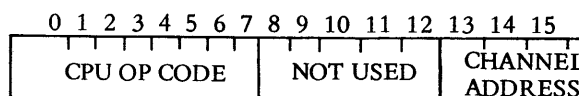
Lines/Minute	Segments	Columns
356	4	1 through 80
460	3	1 through 60
650	2	1 through 40
1110	1	1 through 20

The line printer controller dissipates approximately 5 Watts of power and draws a maximum of 1.0-Ampere.

3-2 COMMAND FORMATS.

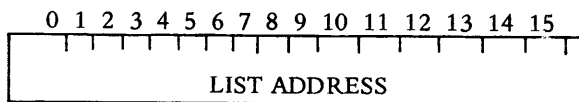
Command formats for the instruction words, status word, and data word are included in this section.

3-2.1 ACTIVATE WORD 1.

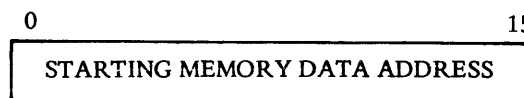


The general channel address for the line printer controller is $5(101_2)$.

3-2.2 ACTIVATE WORD 2.

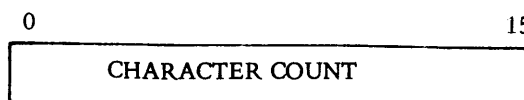


3-2.3 LIST WORD 1.



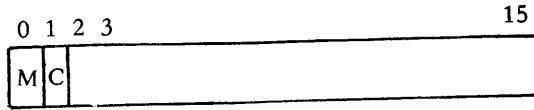
List Word 1 specifies the starting memory address from which is to be transferred. Successive data transfers involve consecutively higher memory locations.

3-2.4 LIST WORD 2.



List word 2 specifies the number of characters to be printed. A count of zero (0) is illegal. The character count is given in binary format. Bit 15 is the LSB.

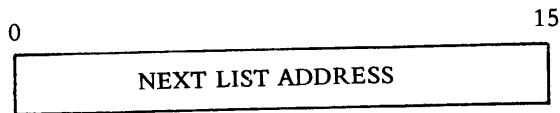
3-2.5 LIST WORD 3.



List Word 3 contains only two bits used by the Line Printer Controller. They are defined as follows:

- Bit 0 Mask Bit. Logic ONE enables the controller to issue an interrupt before storing status. Logic ZERO results in storing status without issuing an interrupt.
- Bit 2 Chain Bit. Logic ONE indicates the controller is to acquire another initialization list after completing the operation specified by the current list.
- Bits 1, 3 Unused.
through 15

3-2.6 LIST WORD 4.



List Word 4 specifies the memory address of the next initialization list to be acquired if chaining is indicated by Bit 2 of List Word 3. If chaining is not indicated by List Word 3, the controller acquires the fourth list word, but it is not used. Chaining enables the controller to acquire data from several different memory areas with the CPU issuing only one ATI or ADAC command.

3-2.7 CONTROLLER STATUS WORD. The status word that is stored in the appropriate location has the following format:

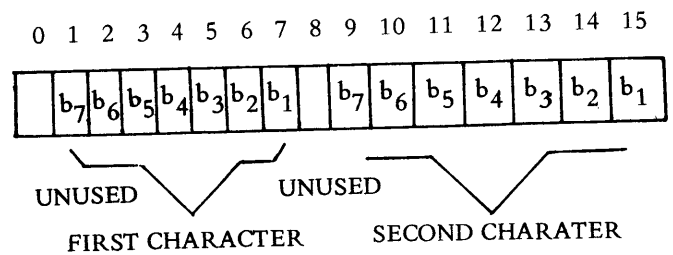
Bits 0 through 11, 13	Unassigned
Bit 12	Controller Busy
Bit 14	Line Printer Not Ready
Bit 15	Operation Complete

3-2.7.1 Controller Busy. Bit 12 is set to a logic ONE when an ATI or ADAC command is issued while the controller is executing a previous list operation (i.e., operation complete has not occurred).

3-2.7.2 Line Printer Not Ready. Bit 14 is set to logic ONE when printer power is Off, the drum gate is not closed, paper is not loaded, or an overtemperature condition exists in the paper drive motor.

3-2.7.3 Operation Complete. Bit 15 is set to logic ONE at the completion of a list operation or if an operation is aborted. If chaining is used, operation complete occurs only after the final list operation is executed.

3-2.7.4 Data Word. The line printer accepts a seven-bit character code which is a modified version of ASCII as listed in Table 3-2. The controller acquires a two-character word from memory and then supplies the characters to the printer unit on demand. The character packing format is illustrated below:



When an odd number of characters are transferred, the controller ignores bits 9 through 15 of the last computer word. Character bit b₇ is the MSB, and bit b₁ is the LSB.

3-3 DATA TRANSFER RATE.

At a printing speed of 356 lines-per-minute with 80 characters-per-line, the data transfer rate from memory to the line printer controller is 238 words-per-second.

3-4 PROGRAMMING.

For programming information; refer to Paragraph 1-5 of this manual.

3-5 INSTALLATION.

The line printer kit consists of a three-card controller, a 6.1-metre (20-foot) cable, and the line printer. The three controller cards are inserted into preassigned card connectors of the DMAC expansion system. The assigned card connectors are identified in Appendices A through I of the "Direct Memory Access Port Expander" Maintenance Manual (TI Part No. 216759) or Section VI of the DMAC Controller Manual (TI Part No. 966312-9701). The cable

TABLE 3-2. CODED CHARACTER SET

b7				0 0 0	0 1 0	0 1 1	1 0 0	1 0 1
b4	b3	b2	b1					
0	0	0	0		Space	0	@	P
0	0	0	1		!	1	A	Q
0	0	1	0		!!	2	B	R
0	0	1	1			3	C	S
0	1	0	0		\$	4	D	T
0	1	0	1		%	5	E	U
0	1	1	0		&	6	F	V
0	1	1	1		!	7	G	W
1	0	0	0		(8	H	X
1	0	0	1)	9	I	Y
1	0	1	0	PF	*	:	J	Z
1	0	1	1		+	;	K	[
1	1	0	0	FF	,	<	L	
1	1	0	1	CR	-	=	M]
1	1	1	0		.	>	N	^
1	1	1	1		/	?	O	

(TI Part No. 217062) is connected to the top edge connector at the number 3 line printer controller card (TI Part No. 217073) and the opposite end of the cable is connected to the rear of the line printer. This cable and the related connections are illustrated in Figure 3-1.

3-6 LINE PRINTER CHARACTERISTICS.

All major line printer performance characteristics are listed in Table 3-3 which is noted below:

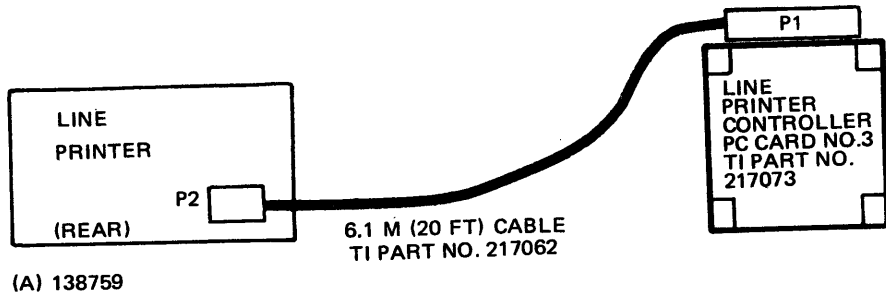


FIGURE 3-1. LINE PRINTER SUBSYSTEM INTERCONNECTIONS

TABLE 3-3. LINE PRINTER PERFORMANCE CHARACTERISTICS

CHARACTERISTIC	SPECIFICATION
Dimensions:	101.60 to 250.83 mm (4.00 to 9.88 in.) wide with 279.40 mm (11.00 in.) between folds
Printer Paper Weight:	
Single Copy	6.8 kg (15.0 lb) bond (minimum)
Multi-copy	5.4 kg (12.0 lb) bond with single-shot carbon for up to six parts
Printer Ribbon:	
Type	Inked roll (nylon)
Width	227.58 to 230.89 mm (8.96 to 9.09 in.)
Length	32 m (105 ft)
Thickness	0.08 to 0.09 mm (0.0030 to 0.0035 in.)

TABLE 3-3. LINE PRINTER PERFORMANCE CHARACTERISTICS (Continued)

CHARACTERISTIC	SPECIFICATION
Signals:	
Input	7 data lines 1 strobe line
Output	1 ready line 1 demand line
Logic Levels:	
Logic ZERO	0 Volt (unless otherwise specified)
Logic ONE	+5 Volts (unless otherwise specified)
Printer Input Voltage (selected at time purchase order placed)	117, 220, 240 Vac ± 10 percent, 47 to 63 Hz, single phase
Printer Power Consumption	350 W
Printer Operating Temperature	10°C (50°F) minimum 43°C (110°F) maximum
Printer nonoperating Temperature	-18°C (0°F) minimum 52°C (125°F) maximum
Printer Humidity:	
Operating	5 to 80% without static eliminator (non-condensating)
Nonoperating	5 to 95% (non-condensating)
Printer Dimensions:	
Height	577.85 mm (22.75 in.)
Width	596.90 mm (23.50 in.)
Depth	558.80 mm (22.00 in.)
Printer Weight	83.81 kg (185 lb)
Printer Paper:	
Type	Standard fanfold, edge-punched with hole spacing 12.70 mm (0.50 in.) apart from center to center.

TABLE 3-3. LINE PRINTER PERFORMANCE CHARACTERISTICS

CHARACTERISTIC	SPECIFICATION
Printable Characters:	
Number	64 (63 characters and space)
Type	ASCII open Gothic print
Size	Typically 2.413 mm (0.095 in.) high and 1.651 mm (0.065 in.) wide
Characters per line	80
Character Drum:	
Characters	64
Speed	1760 rpm
Print Rate (64 character drum)	356 LPM - 80 columns, 4 zones
	460 LPM - 60 columns, 3 zones
	650 LPM - 40 columns, 2 zones
	1110 LPM - 20 columns, 1 zone
Format	Top-of-form control, single line advance with perforation stepover, and carriage return
Paper Slew Speed	330 mm (13 in.) per second (minimum)
Print Area	203 mm (8 in.) wide, left-justified
Character Spacing	2.54±0.0127 mm (0.1000±0.0005 in.) between centers
Line Spacing	4.242±0.254 mm (0.167±0.010 in.: 6 lines-per-inch), each character within ±0.254 mm (±0.010 in.) from mean line through the character
Line Advance Time	20 ms
Hidden Lines	Line visible after 10 lines of print
Character Synchronization	Variable reluctance pick-off designed to sense drum position

SECTION IV

MOVING HEAD DISC CONTROLLERS

4-1 GENERAL.

Texas Instruments offers four different moving head disc units for use with the DMAC interface of either a Model 960 or a Model 980 Computer. These units are:

- **DS31 Disc Drive** — A single drive unit with a removable disc cartridge that provides a total of 1 million words of storage.
- **DS32 Disc Drive** — A single drive unit with a nonremovable disc cartridge that provides a total of 1 million words of storage.
- **DS44 Disc Drive** — A dual drive unit with one removable and one nonremovable disc cartridge that provides a total of 4.5 million words of storage.
- **DS44H Disc Drive** — A dual drive unit with an internal power supply and with one removable and one nonremovable disc cartridge that provides a total of 4.5 million words of storage.

Table 4-1 summarizes the specifications of each of the disc drive units. Two different disc controllers coordinate the data transfer operations between the disc drive(s) and the DMAC, depending upon which disc drive is used:

- **DS31/32 Disc Controller** — A 9-circuit board controller (including three circuit boards comprising the Block Transfer Controller: BTC) that coordinates the operations of DS31 and DS32 disc drives. Up to four of either type of drive (or combinations of the two types of drives) may be connected to one controller.
- **DS44/44H Disc Controller** — A 9-circuit board controller (including three circuit boards comprising the Block Transfer Controller: BTC) that coordinates the operations of DS44 and DS44H disc drives. Up to four of either type of drive (or combinations of the two types of drives) may be connected to one controller.

Table 4-1. Moving Head Disc Characteristics

Characteristic	DS31	DS32	DS44	DS44H
Storage Capacity (data words)	1,143,296	1,143,296	4,595,712	4,595,712
Storage Medium:				
Type	Type 2315 Cartridge	Fixed Disc	Type 5440 Cartridge and Fixed Disc	Type 5440 Cartridge and Fixed Disc
Diameter	15 inches	15 inches	15 inches	15 inches
Lateral Track Density	100 tracks per inch	100 tracks per inch	200 tracks per inch	200 tracks per inch
Recording Format:				
Number of Heads	2	2	4	4
Number of Cylinders	203	203	408	408
Number of Tracks	406	406	1632	1632
Sectors per Track	88	88	88	88
Data Words per Sector	32	32	32	32
Control Words per Sector	3	3	3	3
Recording Density	2200 bpi	2200 bpi	2200 bpi	2200 bpi
Transfer Rate				
Words	97. KHz	97.6 KHz	156.25 KHz	156.25 KHz
Bits	1562 KHz	1562 KHz	2500 KHz	2500 KHz
Transfer Code	Double Frequency Recording	Double Frequency Recording	Double Frequency Recording	Double Frequency Recording
Access Time				
Adjacent Tracks	15 ms	15 ms	8 ms	7 ms
Nonadjacent Tracks (Avg.)	70 ms	70 ms	38 ms	35 ms
Outside to Inside Track	135 ms	135 ms	70 ms	60 ms
Rotational Velocity	1500 rpm $\pm 1\%$	1500 rpm $\pm 1\%$	2400 rpm $\pm 2\%$	2400 rpm $\pm 2\%$
Latency of Rotation	40 ms	40 ms	25 ms	25 ms

Figures 4-1 and 4-2 illustrate the system relationships for the two types of moving head disc configurations.

4-2 DISC DATA ORGANIZATION.

Data is stored on the disc in blocks of data called sectors. Each sector contains a 16-bit preamble, a 16-bit identification word, 32 words of data, plus a 16-bit check character. The disc controller packs 88 sectors to each track on the disc. Each disc contains either 406 tracks (DS31 or DS32) or 816 tracks (DS44 or DS44H). Figure 4-3 illustrates the data organization for all of the moving head discs.

4-2.1 PREAMBLE. The preamble is a 16-bit word generated by the disc controller at the start of each sector. The preamble consists of 15 consecutive zero bits followed by a single one bit (sync bit). When the controller reads this bit sequence from the disc, the sync bit indicates that a new data sector is beginning and synchronizes the read logic of the controller to the recorded bit pattern. The leading pad of zeros differentiates the sync bit from other bit patterns and allows for differences in format and disc unit tolerances. The controller searches for this bit pattern only during sector seek operations, so that a similar

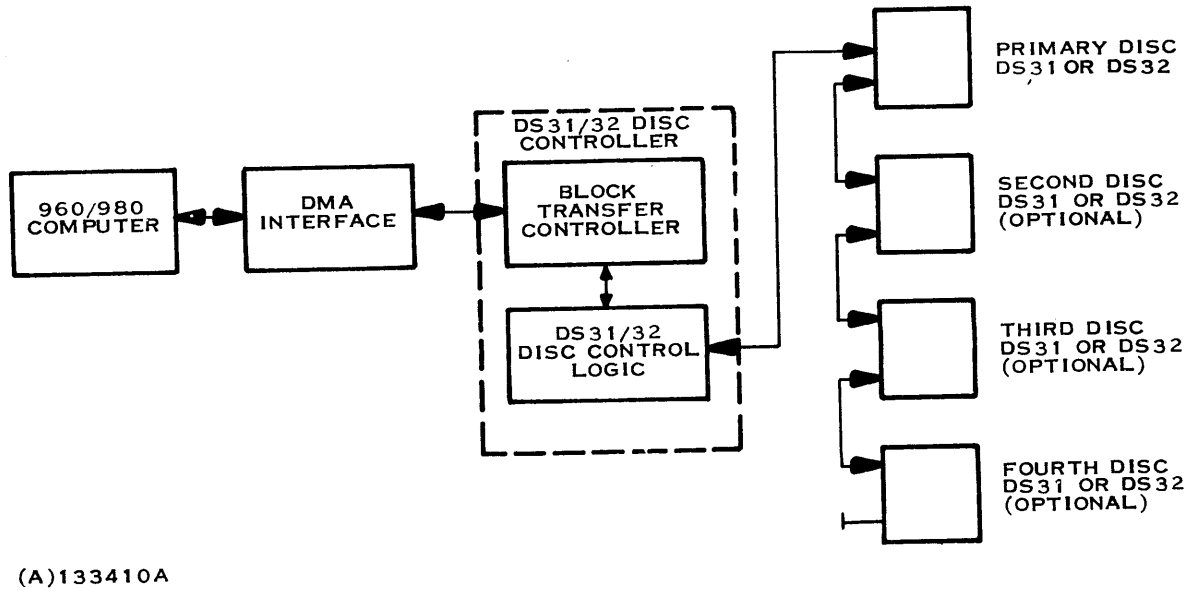


Figure 4-1. DS31/DS32 Disc System Block Diagram

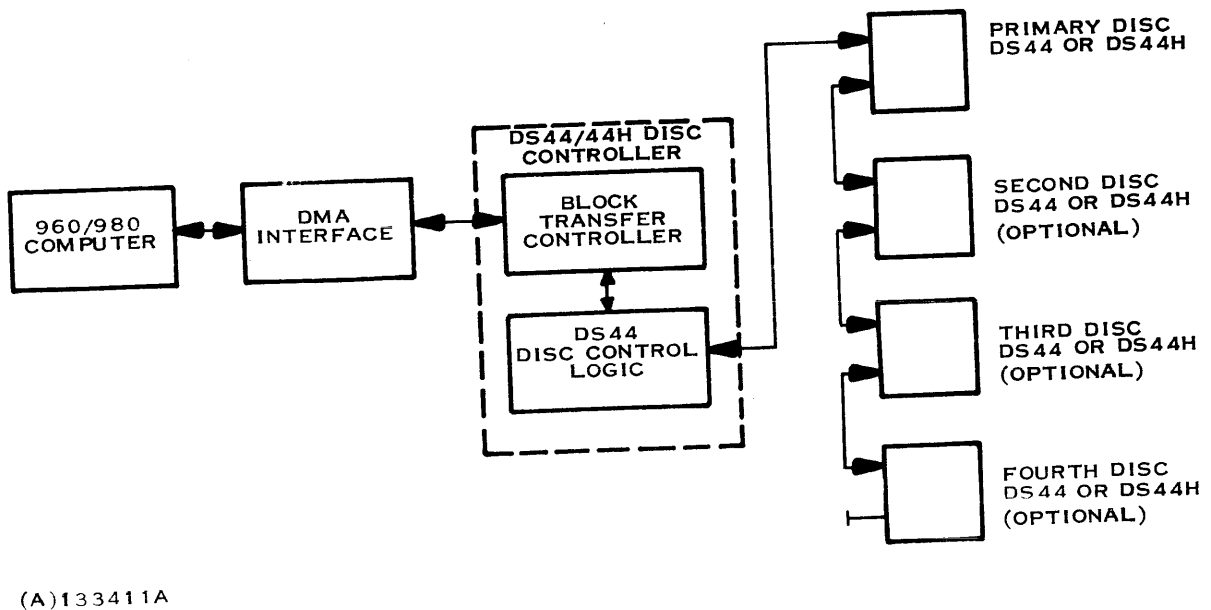


Figure 4-2. DS44/DS44H Disc System Block Diagram

bit pattern that occurs during the data stream does not falsely indicate a new sector

4-2.2 IDENTIFICATION WORD. The identification word is a 16-bit word that immediately follows the preamble for each sector. The identification word contains a write lockout bit, a cylinder address, and a sector address as illustrated in Figure 4-4. The disc controller reads the identification word during a read data, write data or a compare data operation under one of the following conditions:

1. After the controller acquires an initialization list, it checks the identification word of the starting track address before executing the list.
2. When the disc reaches a new cylinder following an automatic cylinder increment, the controller checks the identification word of the new cylinder before continuing with the list.

The controller does not check the identification word if it only switches heads to reach the next sector. Therefore, to avoid destruction of write protected data, a Write ID command should be performed on a cylinder basis.

4-2.2.1 Write Lockout Bit (Bit 0). When set, the Write Lockout Bit indicates that the data in the associated track is protected and should not be overwritten. The data in the track can be written over only with a Write ID command or with a Write Data command with lockout override. If the Write Lockout bit is clear, the data in the track is not protected and the track can be used for storage. The Write Lockout bit is specified in the Write ID command. To protect data on the bottom surface (head address = 1), the whole cylinder (top and bottom tracks) should be protected since the identification word is not verified following a head switch.

4-2.2.2 Cylinder Address (Bits 1 through 8, or Bits 9 and 1 through 8). These bits contain the cylinder address of the track that contains the associated identification word. The cylinder address must be within the range of 0 to 202 (0-CA₁₆) for the DS31 and DS32 disc units, or 0 to 407 (0-197₁₆) for the DS44 and DS44H disc units. To attain the higher address for DS44 and DS44H disc units, bit 9 of the identification word is used as the most significant bit of the cylinder address for the DS44/44H disc controller only.

4-2.2.3 Sector Address (Bits 9 through 15, or Bits 10 through 15). These bits indicate the address of the next sector that will come under the read/write head. Since the most significant bit of this field (bit 9) is used in the

cylinder address field for DS44 and DS44H disc units, all 88 sectors do not have a unique label. Identical sector address labels exist in the same cylinder when the address overflows the allotted 6-bit field for the DS44/DS44H disc controller. However, the sector counter internal to the controller keeps track of the rotational position of the disc so that it can easily differentiate between the similarly labeled sectors. The number in the sector address field is 0 through 87 (0 through 57₁₆) for DS31 and DS32 discs, and is 0 through 63, plus 0 through 24 (0 through 3F₁₆, plus 0 through 18₁₆) for the DS44 and DS44H discs.

4-2.3 CHECK CHARACTER. The check character is a 16-bit parity word for all of the data words stored in the data field of the sector. The character is formed by a series of exclusive OR operations. The first data word is exclusively ORed with the second data word; the resulting word is exclusively ORed with the next data word; and so forth with each succeeding data word. After all 32 data words have been combined in this manner, the resulting check character is stored on the disc. When the data is read from the disc, it is again processed to produce a check character. That check character is exclusively ORed with the check character recorded on the disc. The result of that final operation is a word of all zeros if the data has been read correctly.

4-3 DISC CONTROLLER FUNCTIONS.

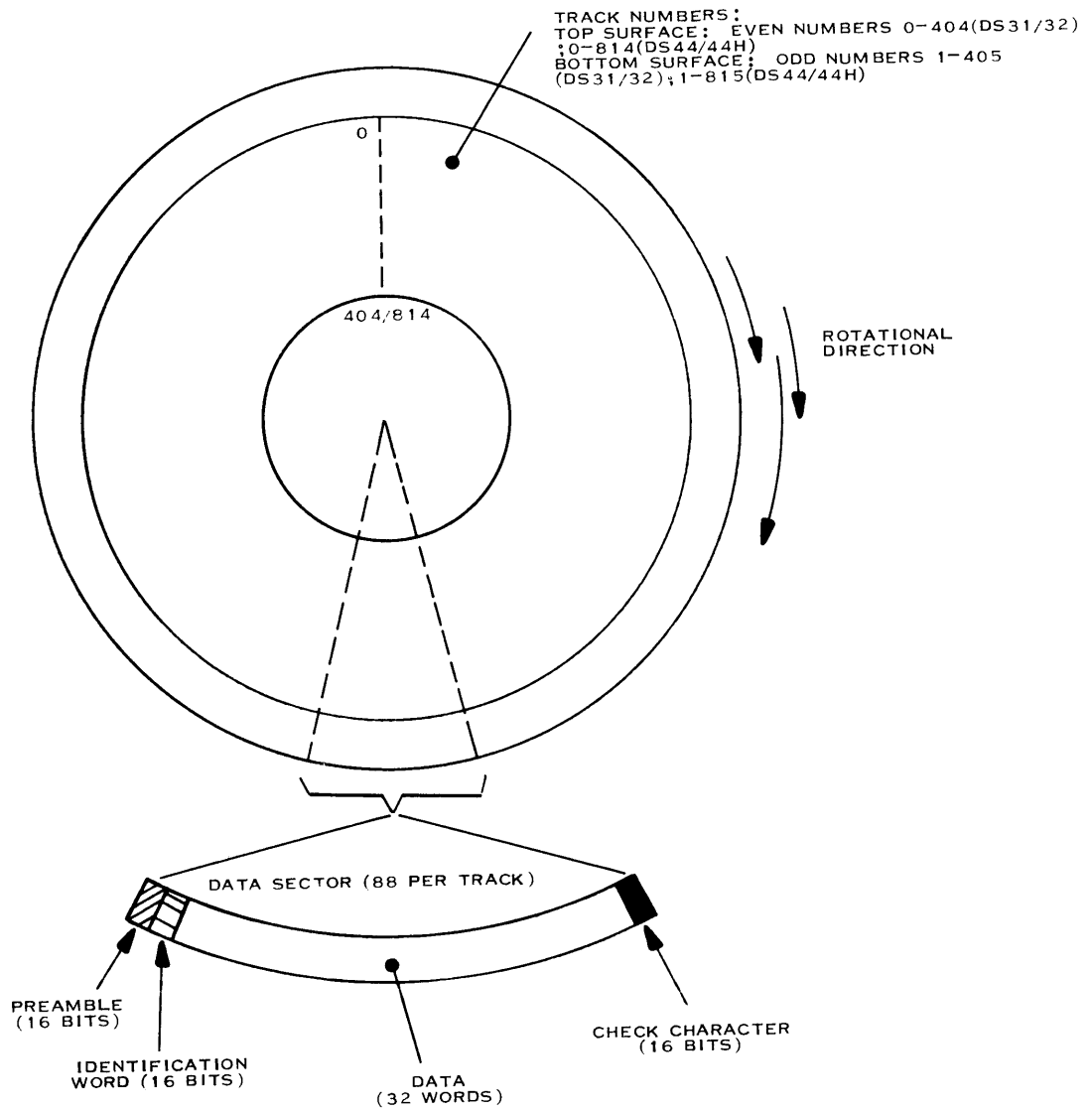
The controller performs several types of read, write, and seek operations. In addition to executing read and write commands, the controller performs automatic functions, such as data checking, head switching and data address verification.

4-3.1 AUTOMATIC SEEKING. When the controller receives a read, write or compare command, it causes the disc to seek to the cylinder address given in list word 3. Therefore, a data transfer command need not be preceded by an independent seek command.

4-3.2 TRACK ADDRESSING. Track addresses on the disc range from 0 to 405 for DS31 or DS32 discs, and from 0 to 815 for the DS44 and DS44H discs. The even numbered tracks are on the top surface of the disc (head address 0) and the odd numbered tracks are on the bottom surface of the disc (head address 1) as illustrated in Figure 4-5. The controller uses a combination of cylinder address and head address to define the track address. The relationship is defined by the following equation:

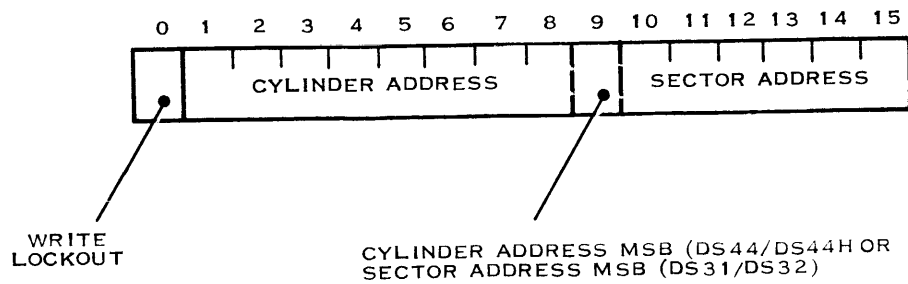
$$2(\text{cylinder address}) + \text{head address} = \text{track address}$$

This equation illustrates that to move from an even numbered track to the next odd numbered track, only the



(A)133412A

Figure 4-3. Moving Head Disc Data Organization



(A)133413A

Figure 4-4. Identification Word Field Assignments

		OUTER EDGE OF DISC	DS31/DS32 END OF DISC (INNER MOST CYLINDER)	DS44/DS44H END OF DISC (INNER MOST CYLINDER)
	CYLINDER ADDRESS	0 1 2 3 4 5 6 . . . 200 201 202	203 . . . 405 406 407	
TOP SURFACE HEAD ADDRESS = 0	TRACK NUMBER	0 2 4 6 8 10 12 . . . 400 402 404	406 . . . 810 812 814	
BOTTOM SURFACE HEAD ADDRESS = 1	TRACK NUMBER	1 3 5 7 9 11 13 . . . 401 403 405	407 . . . 811 813 815	

(A)133414A

Figure 4-5. Disc Track Numbering System

head address need be changed (from 0 to 1); however, to move from an odd numbered track to the next even numbered track requires that the head address be changed (from 1 to 0) and the cylinder address be incremented.

4-3.3 AUTOMATIC TRACK INCREMENT. If the controller encounters an end-of-track during a data transfer and all of the data has not been transferred, the controller automatically switches to the next consecutive track on the disc to continue the data transfer. If the controller is recording on the top surface of the disc, it increments the head address to reach the next track (same cylinder on the bottom surface of the disc), and continues the data transfer with sector zero of that track. For this type of track increment, data transfer is interrupted for only one sector time to make the switch from the top to the bottom surface of the disc. If the controller is recording on the bottom surface of the disc when it encounters an end-of-track, it changes the head address (to select the top surface of the disc) and increments the cylinder address. When the disc locates the new cylinder, the controller verifies the identification word for that track, and continues with the data transfer with sector zero of that track. Because this type of track increment requires an automatic seek for a new cylinder, data transfer is interrupted for one-half revolution of the disc. The delay is only one-half revolution because sector numbering begins on the bottom surface 180° out of phase with the start (and end) of sector numbering on the top surface.

4-4 CONTROL WORDS.

To initiate a data transfer with the disc controller, the computer transfers two Activate Words to the controller as illustrated in Figure 4-6. These two words supply the controller with the information it requires to fetch the initialization list words, as well as control parameters used by the computer. The following paragraphs explain the fields of the two Activate Words.

4-4.1 ACTIVATE WORD 1. Activate Word 1 contains the controller addressing parameters and control bits. This word is divided into the following fields:

- Bits 0 through 7: These bits contain the most significant bits of the CPU Op code for the DMAC activation instruction. For 960 computers this field contains the value 24₁₆ (ADAC instruction); for 980 computers this field contains the value D9₁₆ (ATI instruction).
- Bit 8: When this bit is a 1, it clears the controller and BTC logic; when a 0, this bit indicates that the controller is to fetch an initialization list.
- Bits 9 and 10: These bits select the disc unit that will receive the data transfer operation. The selection is decoded as follows:

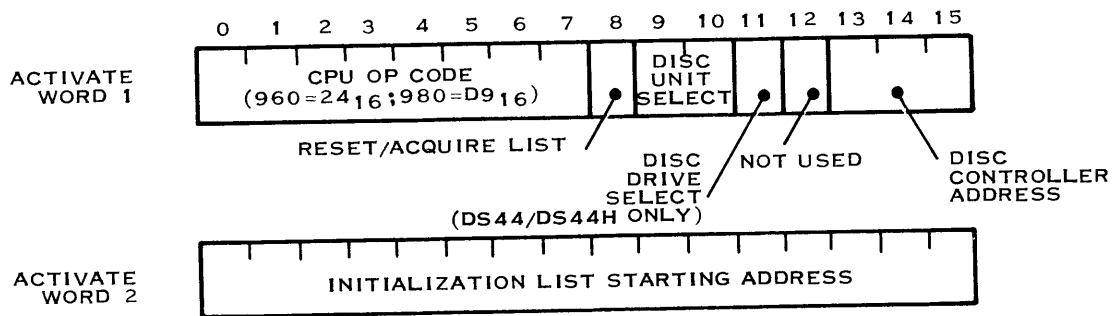
9	10	Selected Disc Unit
0	0	Unit Number 0
0	1	Unit Number 1
1	0	Unit Number 2
1	1	Unit Number 3

- Bit 11: This bit is used by the DS44/DS44H disc controller only to select either the fixed or the removable disc within the selected DS44/DS44H disc unit. The bit is decoded as follows:

- 0 – Fixed Disc
- 1 – Removable Disc

The bit is not used by the DS31/DS32 disc controller.

- Bit 12: This bit is not used.



(A)133415A

Figure 4-6. Disc Controller Activate Words

- Bits 13 through 15: This field contains the DMAC channel address that is assigned to the disc controller. For standard applications this value is zero. The BTC portion of the disc controller decodes this field to determine if the transfer operation is intended for the controller.

4-4.2 ACTIVATE WORD 2. Activate Word 2 contains the starting memory address of the initialization list. The controller uses this address to fetch the list from memory to obtain the parameters that the controller requires to perform the requested transfer. The first list word is located at the starting address; the remaining list words are stored in contiguous locations in memory.

4-5 INITIALIZATION LIST.

When the controller has determined that the operation is intended for it and has received the Activate Words from the computer, it uses the address in Activate Word 2 to fetch the initialization list from memory. The initialization list for the disc controller is a group of three (without chaining) or four (with chaining) words that describe the parameters for the data transfer. Many initialization lists can be chained together to transfer blocks of data to or from different areas of memory or the disc. The controller handles only one list at a time. The following paragraphs explain the function of each of the fields within the initialization list words. Figure 4-7 illustrates the list words for the disc controller.

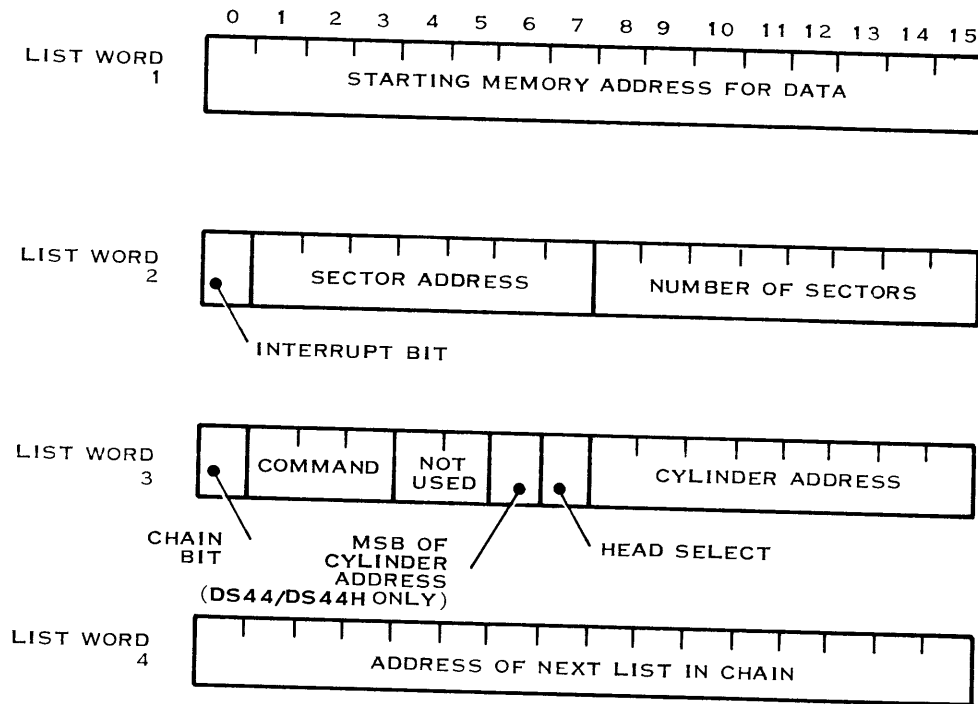
4-5.1 INITIALIZATION LIST WORD 1. List Word 1 specifies the starting memory address where the first data word will be fetched or stored. Successive data words are fetched or stored at consecutively higher memory locations.

4-5.2 INITIALIZATION LIST WORD 2. List Word 2 contains data transfer information that applies to the disc unit. The fields of this word specify the following parameters:

- Bit 0: When this bit is set, the controller must issue an interrupt to the CPU and wait for recognition of the interrupt before storing status in memory. When this bit is clear, the controller can store status in memory at any time without issuing an interrupt.
- Bits 1 through 7: These bits specify the sector address at which the controller begins the data transfer. The value in this field must be within the range 00 to 57₁₆ (0 to 87₁₀). Specifying a value greater than 57₁₆ in this field results in a program error status.
- Bits 8 through 15: These bits specify the number of sectors to be transferred. This field can be any nonzero value from 01 to FF₁₆. Specifying a sector count of 00 in this field produces a program error status.

4-5.3 INITIALIZATION LIST WORD 3. List Word 3 contains control information and a track location specification. The fields of this word specify the following parameters:

- Bit 0: When set, this bit specifies that another initialization list is to be processed following completion of the current list (chaining of the two lists). When the controller finishes with the current list, it fetches the new list from the memory address specified in word 4 of the current list. If this bit is



(A)133416A

Figure 4-7. Disc Controller List Words

clear, the controller terminates operations when it completes the transfer specified in the current list.

- Bits 1 through 3: These bits contain a value that specifies the operation to be performed by the controller. Table 4-2 defines the operation specified by each valid command code.
- Bits 4 and 5: These bits are not used.
- Bits 6, and 8 through 15: These bits specify the cylinder address at which the data transfer will begin. Bit 6 is the most significant bit of the field for DS44 and DS44H discs; this bit is not used for DS31 and DS32 discs. The value in this field must be between 0 and CA₁₆ for DS31 and DS32 discs (bits 8 through 15 only); the value in this field must be between 0 and 197₁₆ for DS44 and DS44H discs (bits 6 and 8 through 15).
- Bit 7: This bit selects one of the two heads for the selected disc to be used in the transfer operation. Together with the cylinder address field this bit

defines a unique track on the disc. The head selection is as follows:

- 0 – Upper head (top surface)
- 1 – Lower head (bottom surface)

4-5.4 INITIALIZATION LIST WORD 4. List Word 4 contains the memory address of the first word of the next initialization list to be processed if another list is chained to the current list. Bit 0 of List Word 3 must be set in order to use this word. If bit 0 of List Word 3 is not set, this word is still acquired from memory but is not used.

4-6 DISC CONTROLLER STATUS.

Each DMAC channel has two reserved memory locations to store words containing device and controller status information. For normal applications with the disc controller assigned to channel 0, the status words are stored in locations 98₁₆ and 99₁₆ in memory. However, the disc controller does not use the second status word locations, so that computer software that monitors disc system status need only check the first status word location in memory.

Table 4-2. List Word 3 Command Field Decode

Command Field Value				Command Definition
Bit	1	2	3	
	0	0	0	Read Data – The controller reads data from the disc and stores it in CPU memory until the number of sectors specified in List Word 2 have been transferred. Automatic track incrementing applies.
	0	0	1	Read Identification Word – The next identification word that comes under the read head is transferred to the memory location specified in List Word 1.
	0	1	0	Compare Data – The controller compares data in memory (starting at address specified in List Word 1) to data on the disc (starting at sector and cylinder specified in List Words 2 and 3, respectively).
	0	1	1	Independent Seek – The controller moves the head to the cylinder address specified in List Word 3. After the disc accepts the seek command, the controller stores operation complete status. The status store occurs 20 to 50 microseconds after receipt of List Word 4. The controller is then ready to accept a command to perform an operation on another unit. When the disc completes the seek, the controller stores seek complete status for that unit whether or not the controller is busy processing a list on another unit.
	1	0	0	Write Data – The controller writes data on the disc until the number of sectors specified in List Word 2 has been written. If the lockout bit (bit 0 of the identification word) is set, no data is written and the controller stores Write Lockout status and terminates.
	1	0	1	Write Identification Word, Lockout Disabled – The identification word is written on the number of sectors specified in List Word 2. The data portion of each sector consists of the data word in the specified memory address of List Word 1.
	1	1	0	Write Identification Word, Lockout Enabled – This operation is the same as write identification word lockout disabled, except that the write lockout bit (bit 0 of identification word) is written as a logic one. Therefore, a write data override lockout command is required to write data on these sectors.
	1	1	1	Write Data, Override Lockout – The number of sectors specified in List Word 2 is written on the disc regardless of the state of the write lockout bit (bit 0 of the identification word). The write lockout bit of the identification word is not altered by this operation.

The controller stores status whenever any of the conditions affecting the status word bits occurs. If the condition is a serious error, the controller also halts the data transfer operation and idles to wait for instructions from the processor. If interrupts are enabled by the last initialization list processed by the controller (bit 0 of List Word 2 is set), the controller generates an interrupt to the processor and waits for a response to the interrupt before storing status. If interrupts are not enabled, the controller performs a normal memory cycle to store the status word each time a new status condition occurs. Table 4-3 lists the status word bit assignments for the disc controller. The following paragraphs explain their operation.

4-6.1 OPERATION COMPLETE (BIT 0). The disc controller stores the status word with bit 0 set when it successfully completes one of the following operations for a nonchained list:

- Read Data
- Write Data

- Read Identification Word
- Write Identification Word
- Compare Data

In addition, the controller sets this bit to indicate that the disc unit has accepted, and is performing, an independent seek operation (when the seek is complete one of the Seek Complete bits, status word bits 12-15, is set).

4-6.2 WRITE PROTECT ENABLED (BIT 1). The disc controller stores the status word with bit 1 set if the controller has attempted to write on a disc when the Write Protect switch on the disc is on. After storing status, the controller idles.

4-6.3 OFFLINE (BIT 2). The disc controller stores the status word with bit 2 set if the controller has attempted to perform a data transfer operation with a disc unit that

Table 4-3. Status Word Bit Assignments

Bit Number	Function	Terminates Operation
0	Operation Complete	Yes
1	Write Protect Enabled	Yes
2	Offline	Yes
3	Data Transfer Error	Yes
4	End of Disc	Yes
5	Program Error	Yes
6	Compare Error	Yes
7	Parity Error	No
8	Identification Compare Error	Write – Yes Others – No
9	Device Busy	No
10	Chain List Taken	No
11	Write Lockout On	Write – Yes Others – No
12	Seek Complete Unit 3	No
13	Seek Complete Unit 2	No
14	Seek Complete Unit 1	No
15	Seek Complete Unit 0	No

is not ready. The not-ready status of the disc may be caused by any of the following conditions:

- Power off
- Disc not at proper speed
- Disc cartridge out of position
- Disc unit not connected
- Disc unit malfunction

After storing status, the controller idles.

4-6.4 DATA TRANSFER ERROR (BIT 3). The disc controller stores the status word with bit 3 set if a data transfer operation failed due to one of the following causes:

- The BTC did not supply a data word at the required time during a disc write operation.
- The controller did not store a data word in memory within the required amount of time during a disc read operation.
- The controller could not locate the required sector during one full revolution of the disc, this may result from:

a) The controller attempted a data transfer operation from a disc that had not been initialized

with a Write Identification Word operation (new disc).

b) The controller attempted a data transfer operation from a disc with a bad surface.

When the error occurs, the data transfer operation halts, the controller stores the status word and then idles.

4-6.5 END OF DISC (BIT 4). The disc controller stores the status word with bit 4 set if it attempts to perform a data transfer operation beyond the last cylinder on the disc (cylinder 202 for DS31 and DS32; cylinder 407 for DS44 and DS44H). When the error occurs, the controller restores the disc to cylinder 00, stores the status word, and idles.

4-6.6 PROGRAM ERROR (BIT 5). The disc controller stores the status word with bit 5 set if it encounters a program error. A program error is caused by:

- Invalid starting sector address in List Word 2
- List Word 2 contains a sector count of zero

After storing the status word, the controller idles.

4-6.7 COMPARE ERROR (BIT 6). The controller stores the status word with bit 6 set if the data read from disc does not match the specified data in memory during a Compare Data operation. When the controller encounters the error, it completes the current sector, stores the status word and then idles. The controller does not chain to the next list if this error occurs.

4-6.8 PARITY ERROR (BIT 7). The controller stores the status word with bit 7 set if the parity read from the disc does not match the parity generated by the controller during a Read Data or a Compare Data operation. When the error occurs, the controller completes reading all sectors in the current list, stores the status word, and then continues by chaining to the next list in the chain. If there is no additional list, the controller idles.

4-6.9 IDENTIFICATION COMPARE ERROR (BIT 8). The controller stores the status word with bit 8 set if the identification word read from the disc does not match the cylinder, head and sector addresses specified by the current list words. If the error occurs during a write operation, the controller stores the status word, terminates the operation before writing on the disc, and then idles. If the error occurs during a read or compare operation, the controller stores the status word and continues with the operation.

4-6.10 DEVICE BUSY (BIT 9). The controller stores the status word with bit 9 set if it receives a new Activate Word from the computer while it is still processing a previous transfer. When the error occurs, the controller stores the status word, and then clears its status register to continue processing the current transfer.

4-6.11 CHAIN LIST TAKEN (BIT 10). When the controller successfully completes a list that has its chain bit (List Word 3, bit 0) set, it uses the address in List Word 4 to acquire the new list. When it has acquired the new list, the controller stores the status word with bit 10 set to indicate successful acquisition of the new list. The controller then proceeds with processing the new list.

4-6.12 WRITE LOCKOUT ON (BIT 11). The controller stores the status word with bit 11 set if it attempts to write on a track and the controller has determined that the write lockout bit (identification word, bit 0) of that track is set. Since the controller does not verify the identification word following a switch from the top surface to the bottom surface in the same cylinder, it will not detect the write lockout bit of the bottom surface being different from the top surface and, therefore, may not detect a write lockout error in that case. When the error is detected, the controller stores the status word and idles without writing on the disc.

4-6.13 SEEK COMPLETE UNIT 0-3 (BITS 12-15). The controller stores the status word with one of these bits set when the corresponding disc unit indicates that it has reached the requested cylinder address. The status storage occurs immediately after the disc notifies the controller,

regardless of what the controller may be doing with any other disc unit. Following the status storage, the controller resumes its previous transfer.

4-7 SITE REQUIREMENTS.

Before installing the disc system, the site must be prepared to meet the environmental, physical and electrical requirements for the system. Table 4-4 summarizes the environmental and electrical requirements of the system. Figures 4-8, 4-9, and 4-10 illustrate the physical characteristics of the disc systems' components.

4-8 INSTALLATION.

The moving head disc kit consists of a nine card controller, a 4.57-metre (15-foot) cable, daisy chain cables, and up to four DS31 or DS32 disc units, or up to four DS44 or DS44H disc units. Either disc controller consists of three cards for the Block Transfer Controller (BTC 1 through 3), and six cards for the disc controller logic. The controller may be installed in a DMA expansion kit or a DMA mounting kit internal to the computer chassis. Plate markings on the right edge of the computer chassis card guide identify the proper slot for each controller card. To install the controller internal to the computer chassis, refer to the DMAC Controller Manual (TI Part No. 966312-9701). That manual also contains information for expansion chassis mounting. Additional information for expansion chassis installation is contained in the "Direct Memory Access Port Expander" Maintenance Manual (TI Part No. 216759-9701). Table 4-5 lists the circuit cards for each disc controller.

Although the DS44 and DS44H disc units are functionally equivalent, since a different vendor supplies the DS44H disc units, there are a few configuration requirements for the DS44H disc unit that differ from those for the DS44 disc unit. Paragraphs 4-8.1 through 4-8.5 describe these differences.

4-8.1 DATA RECOVERY BOARD. The DS44H configuration operates with a tighter timing tolerance, so a new Data Recovery board with a faster Phase Lock Loop (PLL) must be installed. This board is located in the card cage as shown in Figure 4-11.

NOTE

Check the configuration label (see Figure 4-12) on the rear of the DS44H disc unit to ascertain that it is configured for a Model 960/980 Computer. If necessary, follow the Conversion Procedure (TI Part No. 943981) to convert the disc unit to the 960/980 configuration.

4-8.2 DISC SECTOR COUNTER. The DS44H configuration requires 24 hard sector slots (marks). The selection is performed on a sector ring in the bottom side of the disk by the hub.

4-8.3 PWB SWITCH SETTINGS. See Figure 4-12 for a chart depicting the correct option switch settings on all DS44H PWBs. See Figure 4-11 for DS44H PWB locations.

4-8.4 TERMINATOR. Terminating resistors are located on the DS44H I/O PWB. The last DS44H disc unit in a daisy-chain must have the resistors installed. Other DS44H disc units must have their resistors removed as shown in Figure 4-13. The resistor packs labeled XRM(n) are the ones that must be removed.

4-8.5 CONTROLS AND INDICATORS. Six buttons are located on the front panel of the DS44H disc unit (see Figure 4-14); one button is located on top of the disc unit. These seven controls and indicators are described in the following paragraphs.

- **START/STOP** – This control permits starting and stopping of the DS44H disc unit motor to initiate or stop disc operation. The push button lights whenever the DS44H disc unit motor is running.
- **READY** – This indicator lights to show that the DS44H disc unit motor has reached operating speed, the heads are loaded, and the unit is ready for data transfer.
- **ACTIVE** – This indicator lights whenever the DS44H disc unit is engaged in any operation.

- **FAULT/RESET** – This indicator lights whenever a nondamaging fault (such as simultaneously selecting more than one read/write head or simultaneously commanding Read and Write instructions) has occurred. Pressing the lighted **FAULT/RESET** indicator clears the faulty logic and extinguishes the indicator.

- **WRITE PROTECT CART AND WRITE PROTECT FIXED** – These controls allow the operator to protect either the removable (**CART**) or the non-removable (**FIXED**) disc cartridge against data writing. Each indicator lights when its respective condition is active.

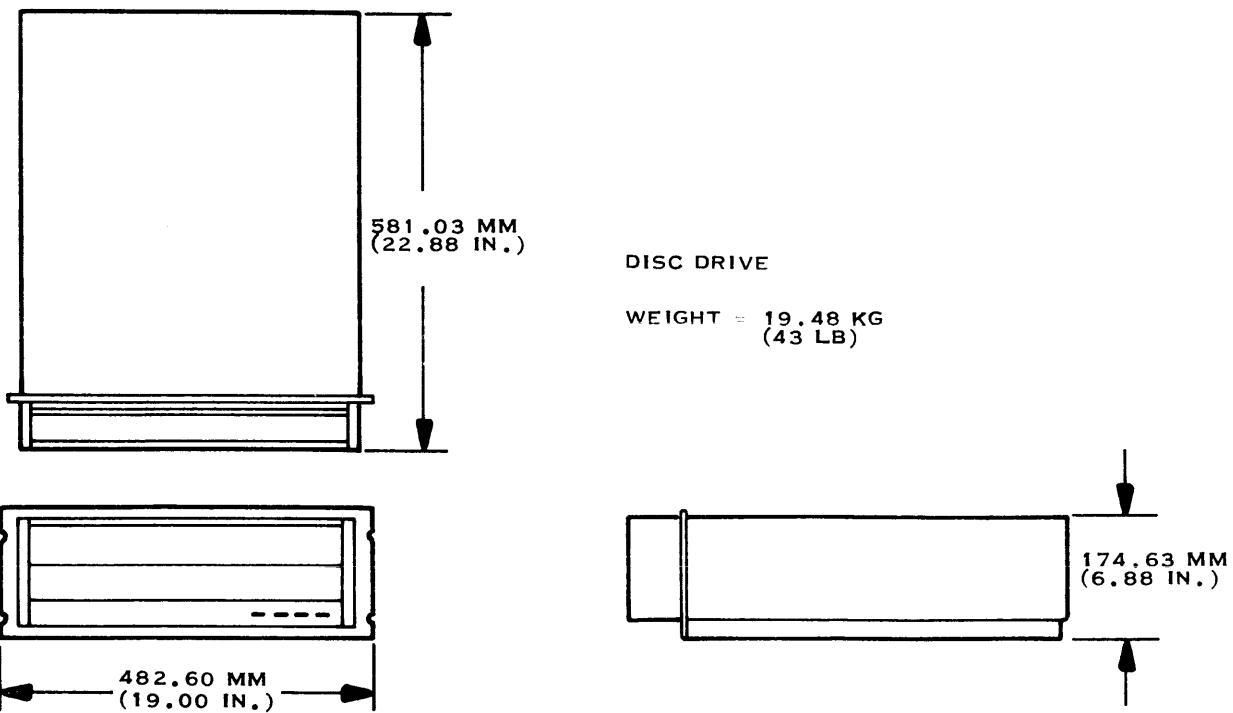
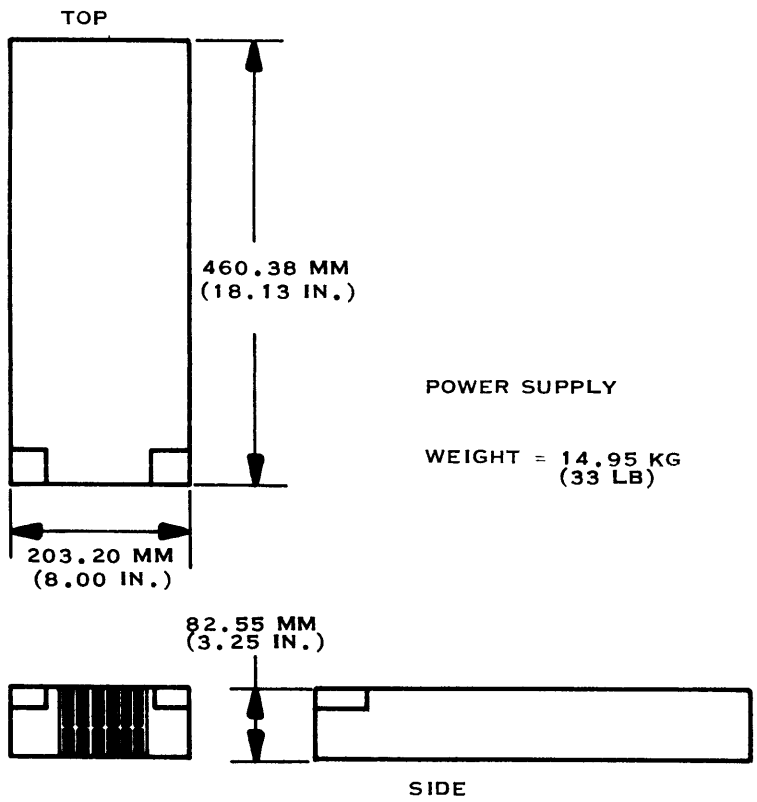
- **Brush** – This indicator is on top of the DS44H disc unit to the upper right of the opening for the DS44H disc cartridge. The indicator resembles a flat-head screw with a black mark on the DS44H disc unit cover on either side of the hole around the indicator. Alignment of the slot with the black marks indicate that the disc cleaning brushes have been retracted and a DS44H disc cartridge may be installed or removed. The slot allows a screwdriver or a coin to be used to retract the brushes, should they fail to retract.

4-9 CABLING.

The interface cable connects the disc unit to the disc controller through the second disc controller circuit board (MHD2). Figure 4-15 illustrates the cabling connections for a DS31/DS32 system. Figure 4-16 illustrates the cabling connections for a DS44 system and Figure 4-17 illustrates the cabling connections for a DS44H system.

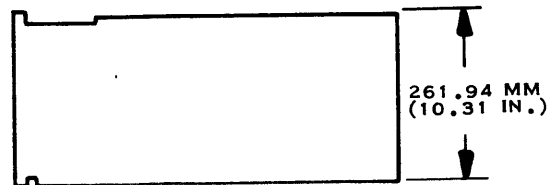
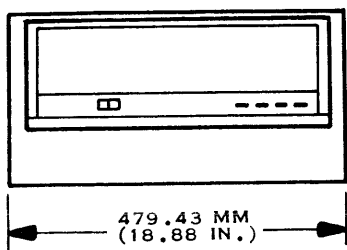
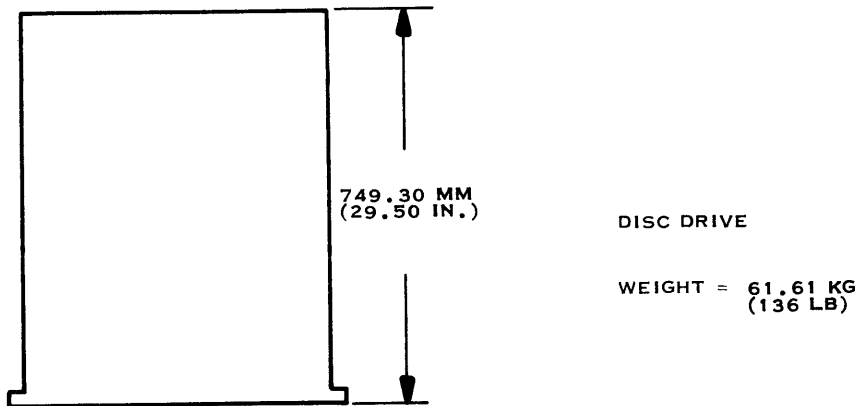
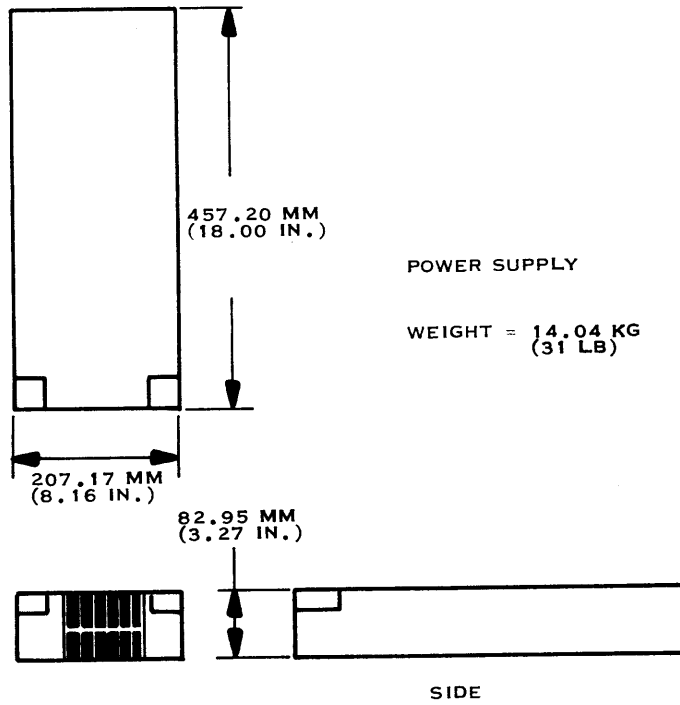
Table 4-4. Installation Site Requirements

Characteristic	Specification
Ac Power Requirement	115 vac $\pm 10\%$ or 220 vac $\pm 10\%$ 50 Hz or 60 Hz ± 1 Hz (Options available through tapped transformer windings in power supply)
Dc Power Requirements (Provided by Power Supply)	DS31/DS32: +15 vdc $\pm 2\%$ @ 8 A average (14.4 A peak) -15 vdc $\pm 2\%$ @ 5.4 A average (11.8 A peak) DS44: +24 vdc $\pm 5\%$ @ 6 A -24 vdc $\pm 5\%$ @ 5 A + 5 vdc $\pm 5\%$ @ 4 A DS44H: Has an internal dc power supply
Operating Environment	
Temperature	15° to 32° C (60° to 90° F)
Relative Humidity	20% to 80% without condensation
Altitude	1829 m (6000 ft) maximum
Storage Environment	
Temperature	-40° to 65° C (-40° to 150° F)
Relative Humidity	5% to 95% without condensation



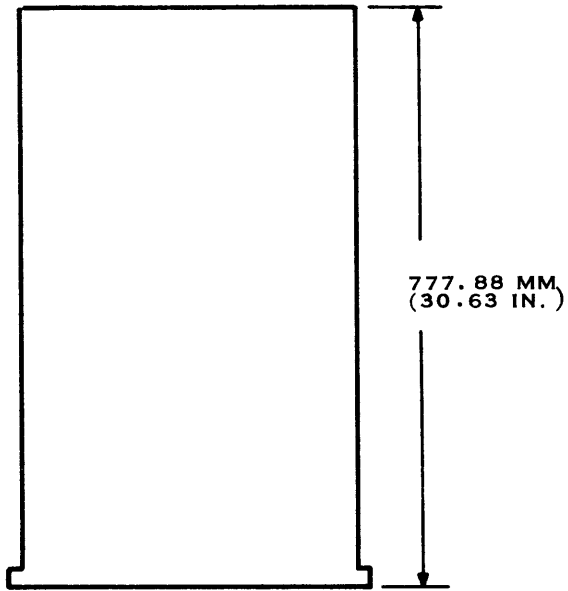
(A)133417A

Figure 4-8. DS31/DS32 Disc System Physical Characteristics



(A)133418A

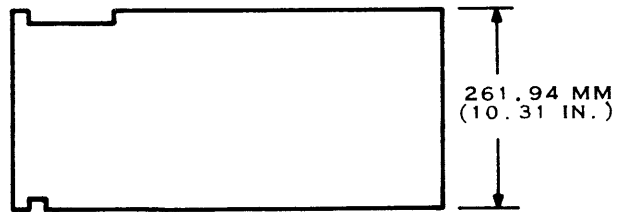
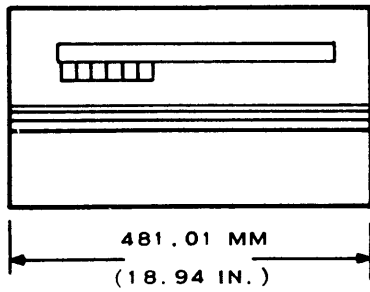
Figure 4-9. DS44 Disc System Physical Characteristics



DISC DRIVE

THE DS44H DISC DRIVE HAS AN INTERNAL DC POWER SUPPLY.

WEIGHT = 67.16 KG (148 LB)



(A) 138752

Figure 4-10. DS44 Disc System Physical Characteristics

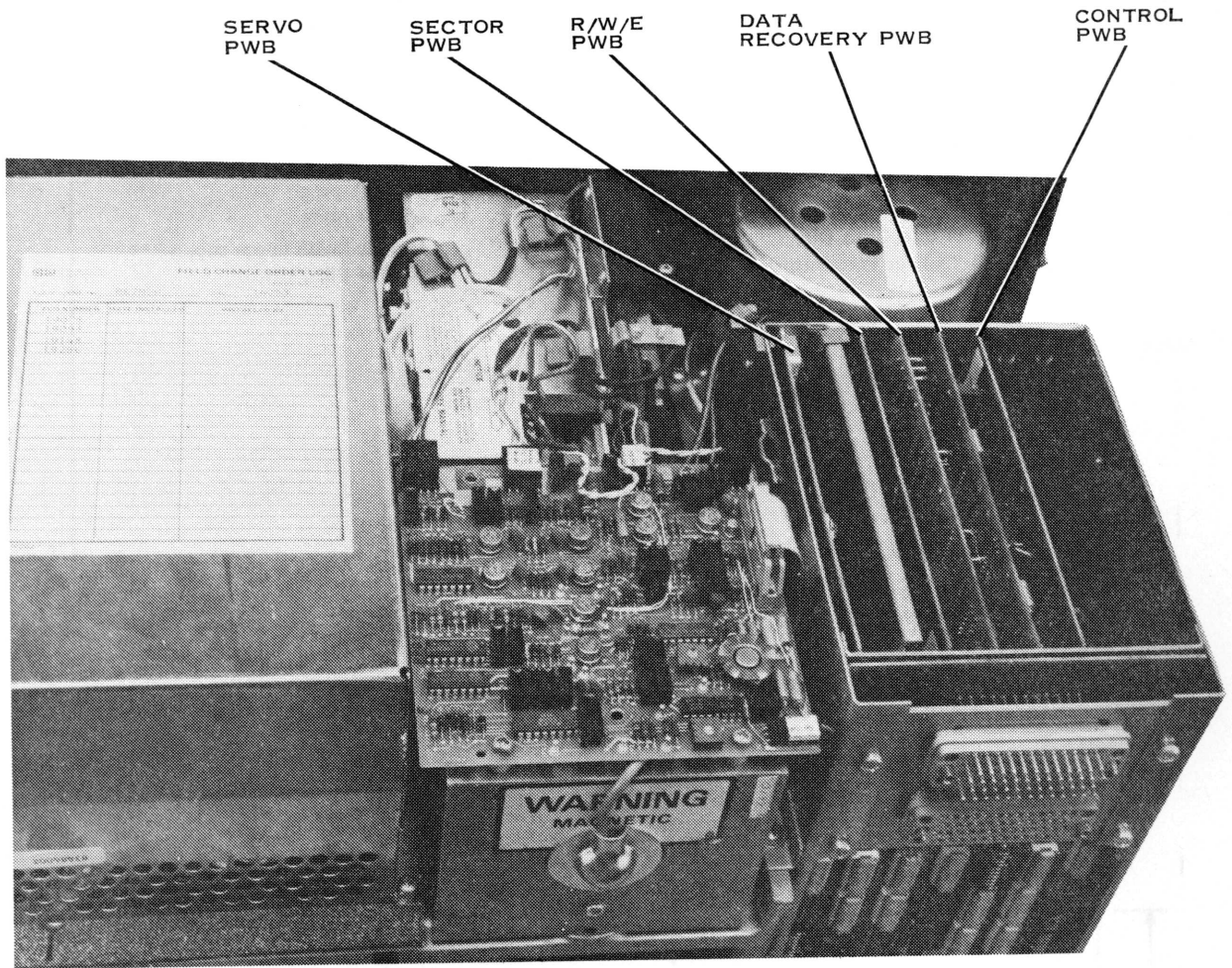
Table 4-5. Moving Head Disc Kit Components

Component	DS31/DS32 System	DS44/DS44H System
Circuit Cards:		
BTC 1	966466-0001	966466-0001
BTC 2	966464-0001	966464-0001
BTC 3	966462-0001	966462-0001
MHD 1	961626-0001	973721-0001*
MHD 2	961628-0001	973678-0001**
MHD 3	961630-0001	961630-0001
MHD 4	961632-0001	973683-0001
MHD 5	973788-0001	973788-0001
MHD 6	973784-0001	973784-0002
Cables:		
Controller to Primary Disc	960279-0001	973690-0015
Daisy Chain	960326-0001	973675-0004
Power Supply to Disc	966622-0005	Included with power supply***
Daisy Chain Terminator	974930-0001 or 966623-0001	973794-0001***

*for the DS44H system: revision level K or higher

**for the DS44H system: revision level P or higher

***not required for the DS44H system



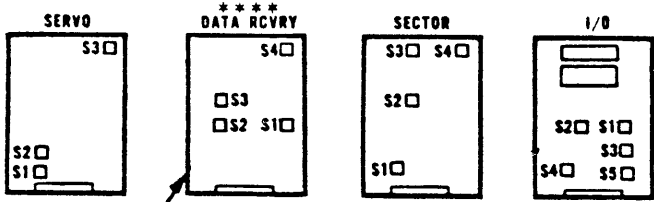
(A)137239 (990-977-35-11)

Figure 4-11. DS44H Disc Unit PWB Locations

NEARSIDE IS COPY SIDE
 FAR SIDE IS ADHESIVE SIDE

SWITCH DESIGNATOR	CONTROL BOARD			SERVO BOARD				DATA RCVRY BOARD				SECTOR BOARD				I/O BOARD				
SWITCH POSITION	S1	S1	S2	S3	S1	S2	S3	S4	S1	S2	S3	S4	S1	S2	S3	S4	S5	S6	S7	S8
1	0	1	0	0	0	0	1	0	1	1	0	0	UN1	INT1	0	0	0			
2	1	1	0	1	1	0	0	0	1	0	0	0	UN2	INT2	1	1	0			
3	1	1	0	1	0	1	0	1	0	0	0	0	UN3	INT3	0	1	0			
4	0	1	0	1	0	1	1	1	1	0	1	0	UN4	INT4	0	1	0			
5	0	1	0	0	0	1	1	0		0	1	0	0	1		0	0			
6	0	1	0	0	0	0	0	0		0	0	1		0		0	0			
7	1	1	0	1	1	1	1		1	0	1		1		0	0	0			
8	0	1	0							0	1	0		0		1	0			
9		1	0											0						
10		0	1											1						

* S1 AND S2 - UM AND INT SWITCHES MUST HAVE SAME UNIT SELECTED
 ** SWITCHES ARE REVERSED FOR 960/980 APPLICATIONS
 *** 1-ON, 0-OFF
 **** CDC PN 75886537 OR 75297105 FOR 990, CDC PN 75881050 FOR 960/980



SPECIAL FOR 960/980

DS10 SWITCH SETTINGS
 THIS UNIT SET FOR 990 960/980

147.83 MM
 (5.82 IN.)

139.70 MM
 (5.50 IN.)

(A) 138753

Figure 4-12. DS44H Disc Unit Configuration Label

(A)137254

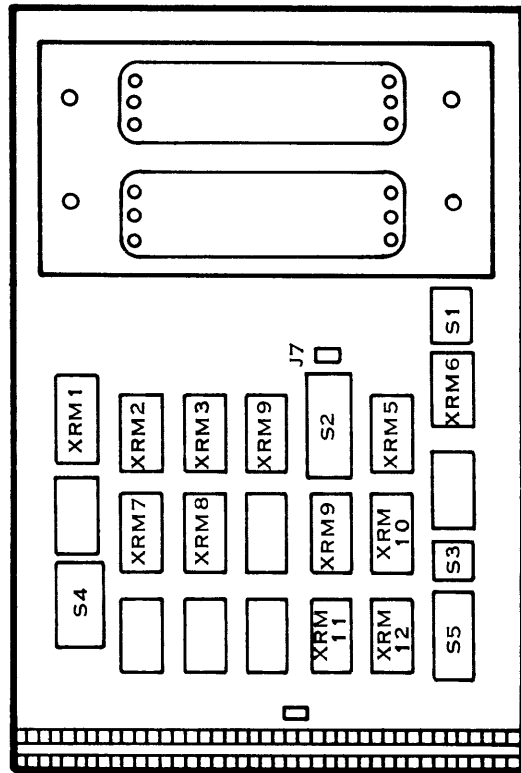
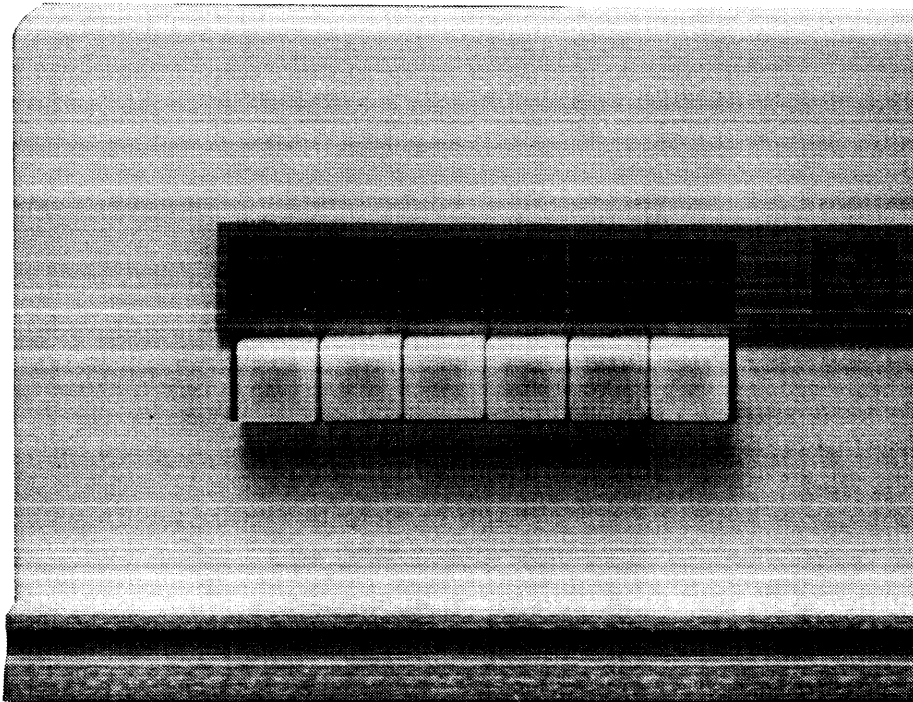
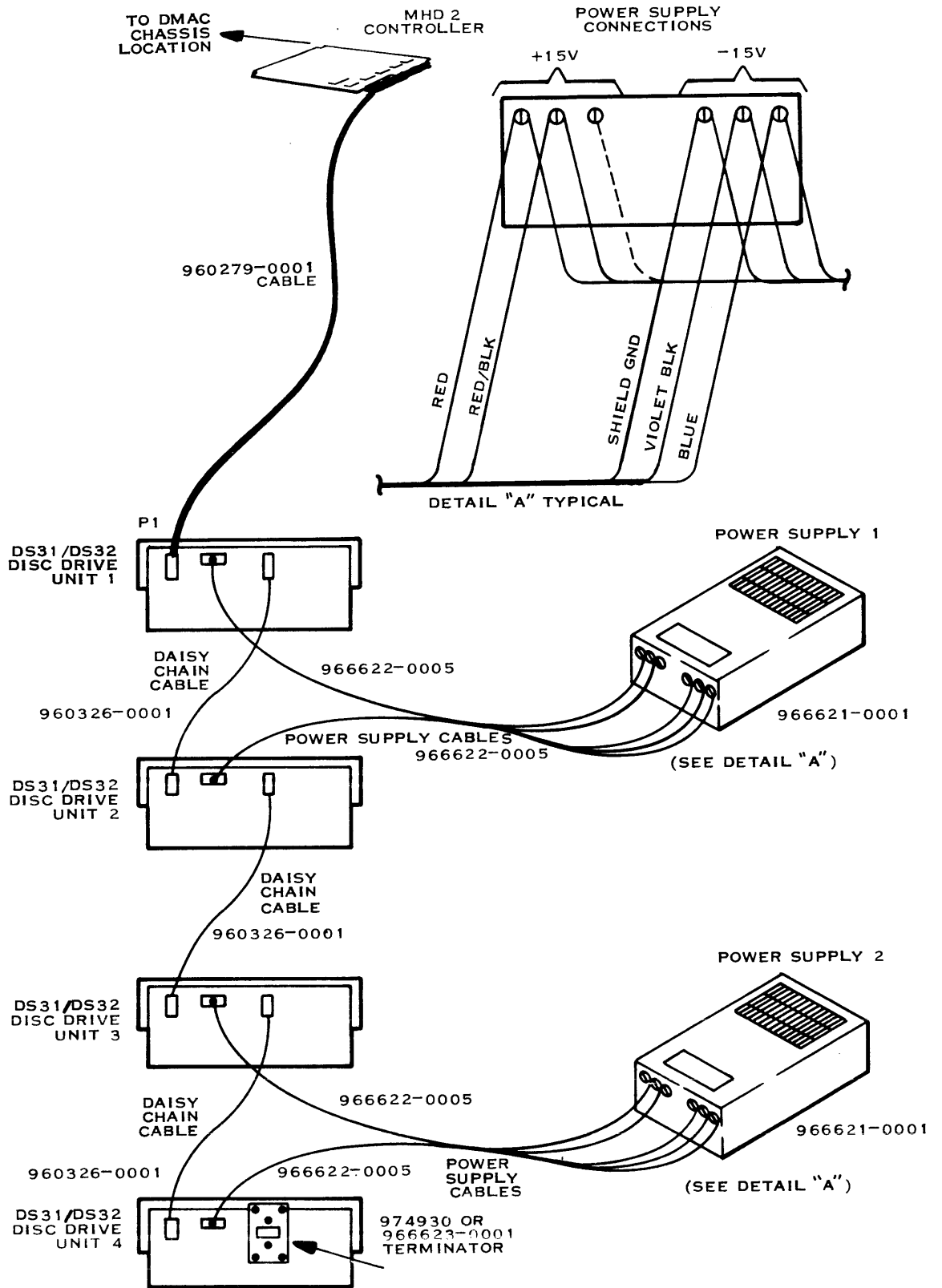


Figure 4-13. Remove XRM(n) Resistor Packs from DS44H Disc Unit I/O Board



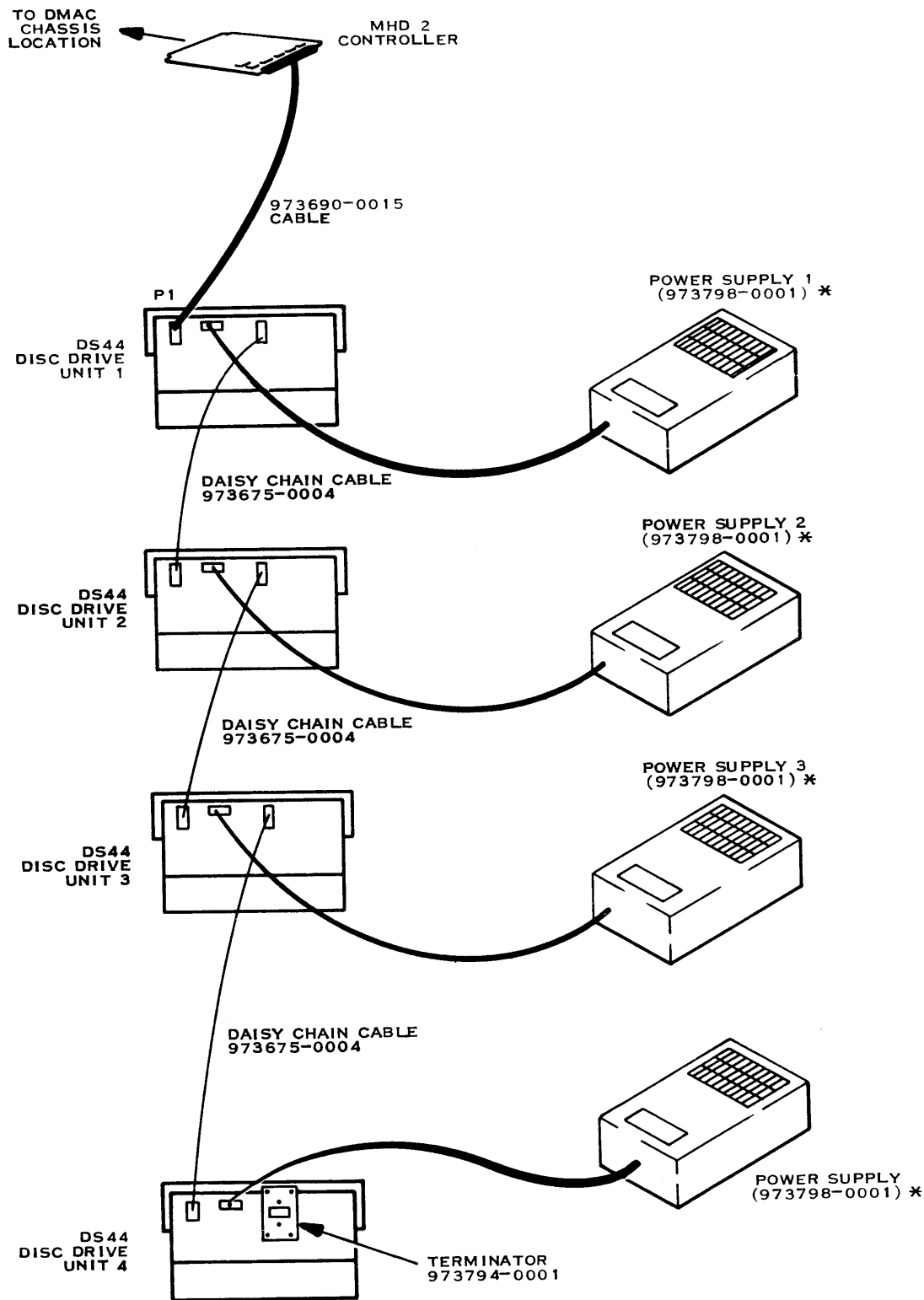
(A) 138754 (990-1177-11-3)

Figure 4-14. DS44H Disc Unit Front Panel Controls and Indicators



(A)133419

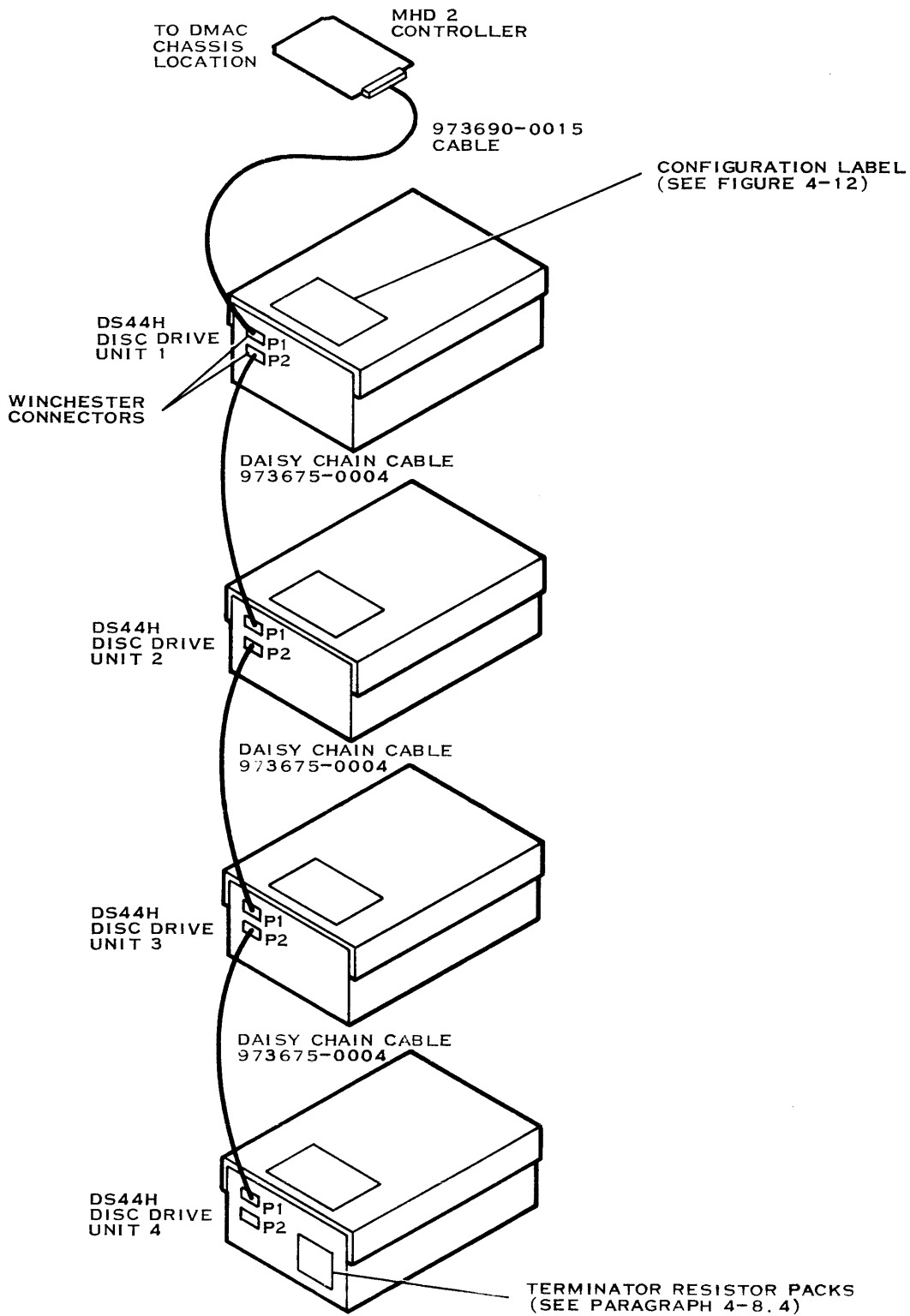
Figure 4-15. DS31/DS32 Disc System Cabling



* ONE POWER SUPPLY IS INCLUDED WITH EACH DISC UNIT.

(A)133420A

Figure 4-16. DS44 Disc System Cabling



(A) 138755

Figure 4-17. DS44H Disc System Cabling

SECTION V

FIXED HEAD DISC CONTROLLER

5-1 GENERAL.

The disc controller completes the interface between the CPU and a Digital Development Corporation Series 6000 or 7310 Disc Memory System. The 6000 series system has a storage capacity of from 57,344 words (16 data bits-per-word) to 458,752 words. The 7310 series has a storage capacity from 688,128 words to 1,835,008 words.

5-1.1 DISC FORMAT. The discs rotate at 3,450 rpm (nominal) resulting in an average access time of 8.7-milliseconds. Data transfer between the CPU and the Disc Memory Controller is in 16-bit words. The controller handles the conversion of serial data that is transferred between the controller and the disc memory unit. The disc format is as follows:

- 16 bits-per-word
- 32 words-per-sector
- 112 sectors-per-track
- 64 tracks-per-surface
- 3584 words-per-track

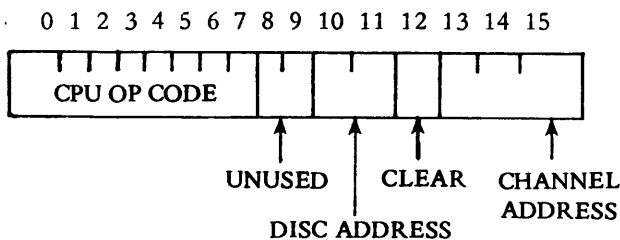
5-1.2 DATA TRANSFER. Data transfer to or from the disc memory unit is accomplished in units of 1 sector (32 words). A maximum of 255 sectors of data may be transferred at a time with the track address automatically incremented (when required).

5-1.3 CONTROLLER POWER. The disc controller requires approximately 5.6 Amperes at 5 Volts dc ($\pm 5\%$). This includes the Block Transfer Controller (BTC). Power requirements for the fixed head disc are listed in a table that is included in Paragraph 5-5.

5-2 COMMAND FORMATS.

Formats for the active, list, and status words are described and illustrated in separate paragraphs which follow.

5-2.1 ACTIVE WORD 1.



Bits 8 and 9

Unassigned

Bits 10 and 11

Disc Address, used to address additional disc memories. This allows up to four disc memories on one Direct Memory Access Channel address as noted below.

Bits 10 11

0	0	First Disc Memory
0	1	Second Disc Memory
1	0	Third Disc Memory
1	1	Fourth Disc Memory

The disc unit selection logic can only be utilized for special systems which require multi fixed head discs. The logic is designed for one block transfer controller to control four sets of disc interface cards (3 cards per set). Each set of disc interface cards is connected to one disc unit. The mounting of this configuration requires a special DMA expansion kit that is tailored for the special system.

Bits 12 CLEAR

If bit 12 is a ONE, a clear command is indicated. This causes the entire disc control logic, including the BTC, to be reset. A clear command is unconditionally accepted by the controller, whether the controller is busy or idle.

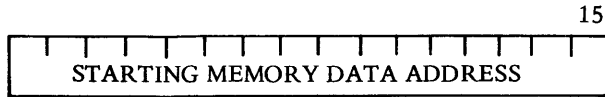
The disc controller is generally assigned address zero.

5-2.2 ACTIVATE WORD 2.



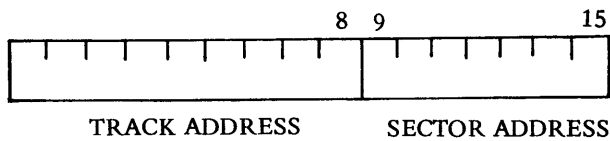
The second active word is the address of the initialization list.

5-2.3 LIST WORD 1.



List word 1 specifies the starting memory address from or to which data is to be transferred. Successive data transfers involve consecutively higher locations.

5-2.4 LIST WORD 2.



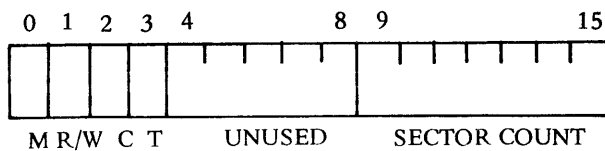
List word 2 specifies the starting disc track and sector address.

- Bits 0-8 Contain disc track address (000-511) which is determined by disc capacity
- Bit 9 High order (0-1) of starting sector address
- Bits 10-15 Low order (00-55) of starting sector address

The 112 sectors are addressed as follows:

ADDRESSED SECTOR	BIT 9	BITS 10-15
0	0	0
55	0	55
56	1	0
112	1	55

5-2.5 LIST WORD 3.



Bit 0 Interrupt bit. A logic ONE enables the controller to issue an interrupt when storing status. A logic ZERO results in storing status without issuing an interrupt.

Bit 1* Read/Write bit. A logic ONE indicates disc write operation; i.e., memory data is transferred to disc. Logic ZERO indicates disc read operation; i.e., disc data is transferred to memory.

Bit 2 Chain bit. A logic ONE indicates controller is to acquire another initialization list after completing operation specified by current list.

Bit 3* Test bit. A logic ONE initiates a comparison test of data read from memory to data read from the disc. This test may be a read-after-write test. Data is first written on the disc and on the next revolution it is read from the disc and compared to data in memory.

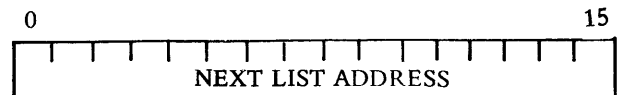
Bits 4 through 7 Not used.

Bits 8 through 15 Sector Count. Specifies number of data sectors to be transferred to or from disc (000-255)₁₀. A count of zero results in a program error status.

*Bits 1 and 3 are used as follows:

Bit 1	Bit 3	
0	0	Read data and store in memory
1	0	Write data from memory
0	1	Read data and compare with data in memory (data not stored in memory)
1	1	Write data from memory then read and compare (this requires an extra disc revolution, 18.7 milliseconds)

5-2.6 LIST WORD 4.



List word 4 specifies memory address of the next Initialization list to be acquired if chaining is indicated by bit 2 of list word 3. If chaining is not indicated by list word 3, the controller acquires the fourth list word; however, it is not used. Chaining enables the controller to acquire data from several areas with the CPU issuing only one ATI or ADAC command.

5-2.7 INTERRUPTS AND STATUS WORD. The disc controller reports status at appropriate times in two status words. The second status word is the starting list address. All status conditions except data parity errors are stored as soon as they occur. Data parity status is stored when the next status store condition occurs. This may be operation complete, busy, or list taken.

The significance of disc controller status word bits is as follows:

Bit 0 (List Taken) Set to a logic one when: the operation specified by a list is complete, the list indicated chaining, and the succeeding list has been acquired.

Bit 8 (Timing Error) Set to a logic ONE when data is not available when needed during write or not taken fast enough during read.

Bit 9 (Program Error) Set to logic ONE any time an initialization list containing ZEROS in bits 9 through 15 of List Word 3 (sector count) is encountered. May also be set to a logic ONE when the sector address (list word 2, bits 10-15) is greater than 55.

Bit 10 (Compare Error) Set to logic ONE as the result of an unequal comparison between the data read from the disc and data read from the memory. This comparison is performed when bit 3 of list word 3 is a logic ONE.

Bit 11 (Parity Error) Set to logic ONE when a read parity error is detected or when a parity error is detected on data transmitted to from memory.

Bit 12 (Controller Busy) Set to logic ONE when an Activate command is issued to the disc controller and the controller is executing a previous list operation; i.e., operation complete has not occurred.

Bit 13 (Disc Unit Not Ready) Set to logic ONE when the disc operating speed or temperature is incorrect or when the head actuation pressure is low.

Bit 14 (Write Lockout) Set to logic ONE when a track (with related track locked out) is addressed with a write command. The write lockout panel is located on the disc unit. Switches on the panel are marked "OFF" and "ON". "OFF" refers to tracks which are write protected. "ON" refers to tracks which are enabled for read and write. The switches are identified as switch No. 1 through No. 16. On the 6000 series disc units, each switch represents 16 tracks. On the 7310 series disc units, each switch may represent any number of specified tracks.

Bit 15 (Operation Complete) Set to logic ONE at the completion of a list operation. If chaining has been employed, operation complete does not occur until the final list operation is completed.

Status Bit	Significance	Condition
0	List Taken	Nonabortive
1-7	Unassigned, always zero	
8	Timing Error	Abortive
9	Program Error	Abortive
10	Compare Error	Abortive
11	Parity Error	Abortive on ATI or List Words
12	Controller Busy	Nonabortive
13	Disc Unit not Ready	Abortive
14	Write Lockout	Abortive
15	Operation Complete	Abortive

5-3 DATA TRANSFER RATE.

The controller transfers data between the buffer register and memory in 16 bit parallel words. Data transferred between the controller and the disc memory unit is processed in serial form at 3.57×10^6 bits-per-second once the starting track and sector address are located. This bit transfer rate requires a word transfer every 4.48 microseconds. This is a 223K word-per-second rate.

5-4 INSTALLATION.

The fixed head disc kit consists of six controller cards, a 6-metre (20-foot) cable, and a disc unit. The controller consists of three boards for the block transfer controller and three wire-wrap boards for the disc interface. If the controller is installed in the mainframe of the CPU, and internal DMA mounting kit is required. The card locations are

identified by an escutcheon plate on the card cage. For installation in the external DMA expansion chassis, refer to the "Direct Memory Access Port Expander" maintenance manual as outlined in the installation of port expander manual or refer to the DMAC manual (TI Part No. 966312-9701) for either installation. The disc unit is supplied with slides which require front and rear mounting. Refer to Figure 5-1 for a typical cabinet installation. A 6-metre (20-foot) cable (TI Part No. 961580) completes the interface between the disc unit and the disc controller as shown in Figure 5-2.

5-5 FIXED HEAD DISC CHARACTERISTICS.

All major fixed head disc characteristics are listed in Table 5-1.

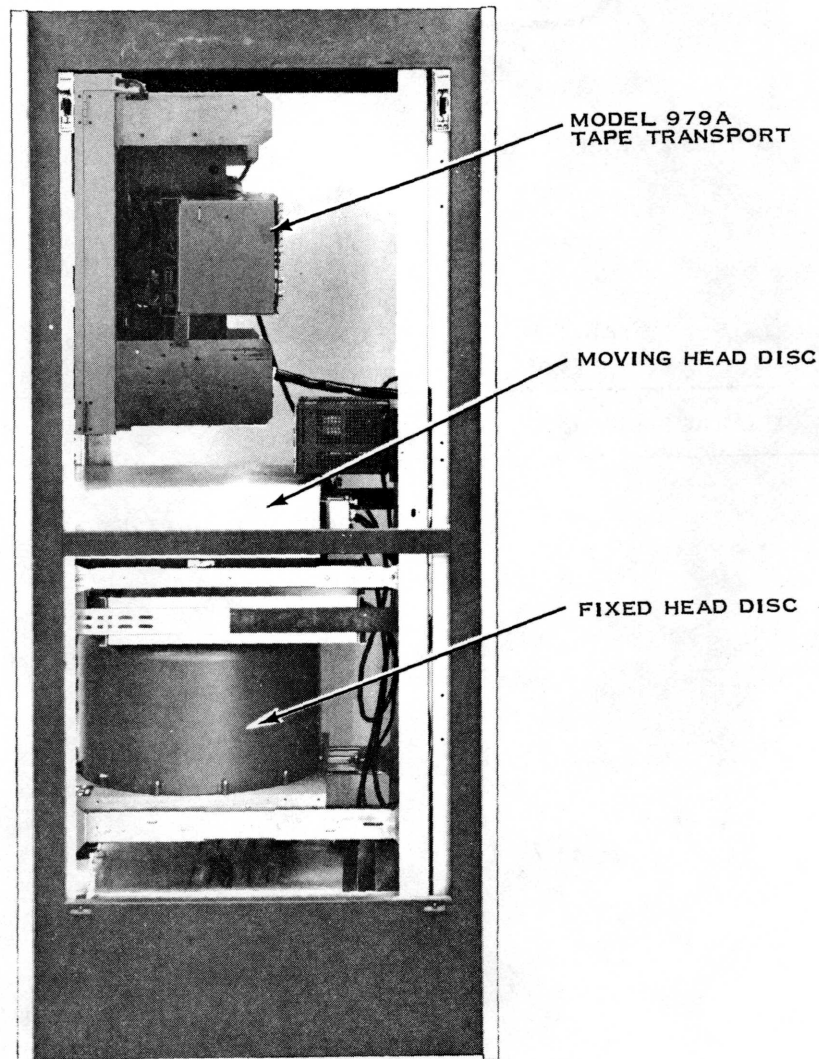


FIGURE 5-1. TYPICAL DISC CONTROLLER CABINET INSTALLATION

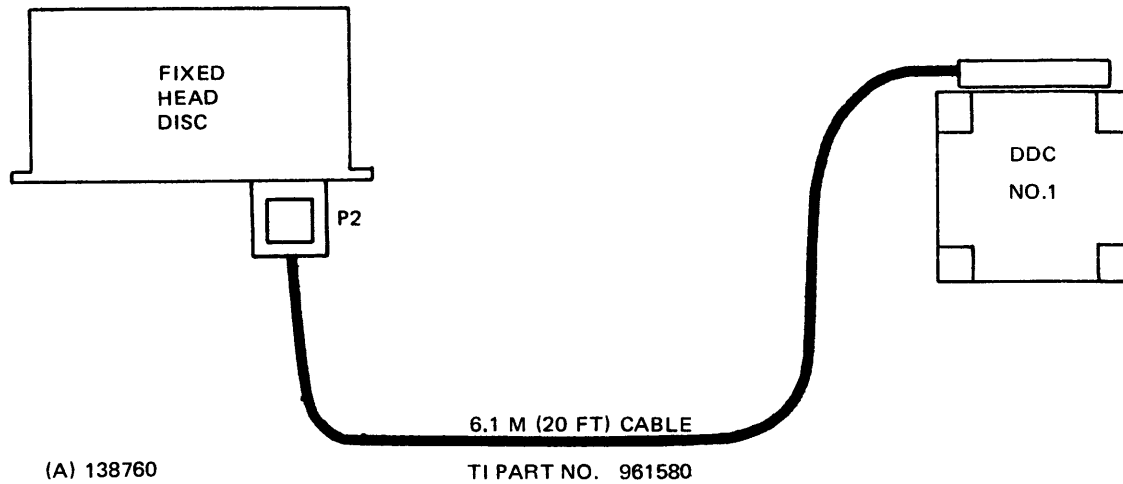


FIGURE 5-2. FIXED HEAD DISC INTERFACE CABLE CONNECTIONS

TABLE 5-1. FIXED HEAD DISC SPECIFICATIONS

CHARACTERISTIC	SPECIFICATION
Speed:	
60 Hz Units	3600 RPM, less 4% slip
50 Hz Units	3000 RPM, less 4% slip
Data Characteristics:	
Average Access Time	8.7 ms (60 Hz), 10.4ms (50 Hz)
Bit Transfer Rate	3.7 mHz maximum
Error Rate	Does not exceed 1 in 10^{13} bits for non-recoverable errors (one which cannot be recovered after 3 read/write tries).
Timing Signals	One data clock, one word mark clock, one sector mark clock and one origin mark clock.
Dimensions:	
General	Enclosure can be slide-mounted for installation in a standard 19-inch (482.6-millimetre) rack. Mounting length can be expandable from 525.8 to 693.4 millimetres (20.7 to 27.3 inches).

TABLE 5-1. FIXED HEAD DISC SPECIFICATIONS (Continued)

CHARACTERISTIC	SPECIFICATION	
Height Width Depth	6000 Series 381.00 mm (15.00 in.) 446.02 mm (17.56 in.) 460.25 mm (18.12 in.)	7310 Series 450.85 mm (17.75 in.) 446.02 mm (17.56 in.) 543.56 mm (21.40 in.)
Weight: Net Shipping	45.3 kg (100 lb) 63.4 kg (140 lb)	63.4 kg (140 lb) 81.5 kg (180 lb)
Power Requirements: AC (Motor Only) DC +25 ±1.0V, ±1% regulation + 5 ±0.25V, ±1% regulation -12 ±1.0V, ±1% regulation	115V, ±10% at 50 or 60 Hz, ±3% (50 Hz and/or 230V specified at time of order) 2.5 A, Starting Current 0.6 A, Run Current 1.0 A Max 2.2 A Max 2.8 A Max 5.5 A Max 1.0 A Max 2.0 A Max	
Environmental Characteristics:		
Temperature	0° to 50°C (32° to 122°F), Operating -40° to 71°C (-40° to 160°F), Nonoperating (Data recorded at any temperature within this range is recoverable at any other temperature within the operating range.)	
Relative Humidity	5% to 95%, Operating and Nonoperating	
Altitude	3048 m (10,000 ft), Operating and Nonoperating	
Shock and Vibration: (operating and nonoperating)		
Shock*	2G's	
Vibration:** 0-10 cps 10-25 cps 25-50 cps Over 50 cps	0.127 mm (0.005 in.) total excursion 0.051 mm (0.002 in.) total excursion 0.025 mm (0.001 in.) total excursion 0.127 mm (0.005 in.) total excursion	
NOTES: * In any direction ** Vibration acceleration not to exceed 2G's		

SECTION VI

MODEL 979A TAPE TRANSPORT CONTROLLER

6-1 GENERAL.

The Model 979A Tape Transport Controller is capable of handling a maximum of three Texas Instruments Model 979 9-Track Computer Tape Transports. These units operate at 952.5 millimetres (37.5 inches) per second and a density of 800 bpi. The 9 tracks include 8 tracks of data and 1 parity track.

The transport units that are handled by a single controller are daisy-chained so that only one data transfer operation may be in progress while the others may be in any rewind combination. (See Figure 6-1.) All three transports may be rewinding simultaneously.

Two primary functions are performed by the Model 979A Tape Transport. The transport is capable of independently retrieving blocks of data from memory and transferring these data blocks to the tape transport for writing on tape. The Model 979A is also capable of independently accepting blocks of data read from tape by the tape transport and storing this data in memory.

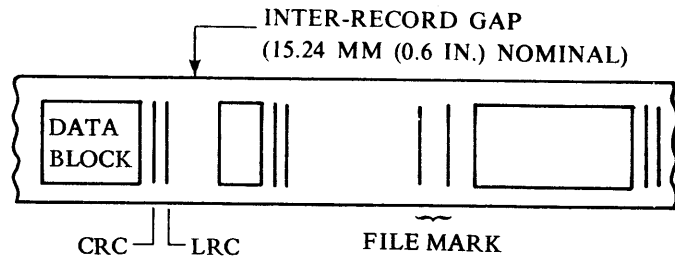
At any given time, only one non-rewind operation may be in progress at any given transport. Any combination of the remaining transports may be rewinding simultaneously.

Rewind commands to the controller require only the execution of an ATI or ADAC command by the CPU for activation of the controller and the appropriate transport. Non-rewind commands require execution of an ATI or ADAC command by the CPU and acquisition of a list by the Block Transfer Controller (BTC) portion of the tape transport controller.

The controller and transport status is reported at appropriate times as either one or two words. Two words are stored only when a data transfer operation has been executed.

The CRC and LRC characters are written to provide an IBM compatible gap and a means of detecting even numbers of parity errors in the data record that would not be detected by the vertical parity check accompanying each data character.

6-1.1 TAPE FORMAT. The 9-Track 979A Tape Controller reads and writes data in an IBM compatible format. The format is illustrated as follows.



Data is recorded in 9-bit characters including 8 data bits and 1 parity bit (odd) grouped together into blocks or records. Each record is followed by two check characters, a Cyclic Redundancy Check (CRC) character and a Longitudinal Redundancy Check (LRC) character.

The inter-record gap (spacing between data blocks) is nominally 15.24 millimetres (0.6 inch).

File marks are used to separate groups of data blocks. The file mark consists of two 9-bit characters separated by a distance equivalent to eight data characters. Each of the two characters is an octal 23 $[(23)_8 = (000100011)_2]$. The file mark is preceded by an erased gap of 88.9 millimetres (3.5 inches).

The following commands are executable in the 9-track tape system.

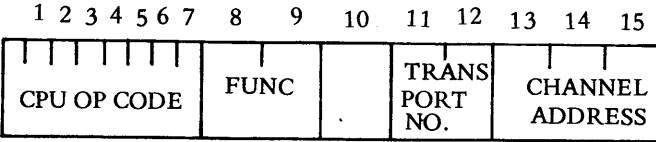
- REWIND
- REWIND AND UNLOAD
- READ BINARY (FORWARD)
- RECORD SKIP (FORWARD or REVERSE)
- WRITE BINARY (FORWARD)
- WRITE END OF FILE (FORWARD)
- ERASE (FORWARD)

6-1.2 DATA TRANSFER. The character transfer rate is 3×10^4 characters per second with a tape density of 800 bpi or 6×10^4 characters per second with a tape density of 1600 bpi. The tape speed is 952.5 millimetres (37.5 inches) per second.

6-2 COMMAND FORMATS.

Formats for the active, list, and status words are described and illustrated in separate paragraphs which follow.

6-2.1 ACTIVE WORD 1.



Bits 8 and 9 Define function to be executed and are coded as follows:

Bits 8	9	
0	0	Rewind selected transport (with interrupt enabled).
0	1	Rewind and unload selected transport (with interrupt enabled).
1	0	Rewind selected transport (with interrupt disabled).
1	1	Acquire list; initiate specified operation.

Bit 10 Must be a logic ZERO.

Bits 11 and 12 These bits define a clear command or a transport to be selected and are coded as follows.

Bits 11	12	
0	0	Clear command
0	1	Select transport number 1
1	0	Select transport number 2
2	1	Select transport number 3

The tape transport controller is generally assigned to channel address one.

6-2.1.1 Rewind Selected Transport (interrupt enabled). This mode of operation causes the addressed tape unit to rewind to the Beginning-of-Tape (BOT) marker on tape. Once the rewind is initiated, an operation complete status is stored preceded by an interrupt. The controller is busy until the status store cycle is completed. When the rewind is completed, a rewind complete status bit is stored preceded by an interrupt.

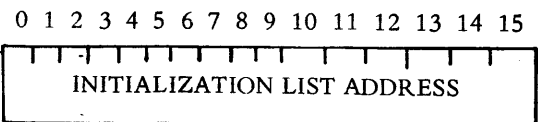
6-2.1.2 Rewind and Unload Selected Transport (interrupt enabled). This mode of operation causes the addressed tape unit to rewind to the BOT marker. Once the BOT marker is detected, the transport servo and vacuum motors are turned off, taking the transport offline. Once the rewind has been initiated, an operation complete status is stored with an interrupt preceding the status storage. No further status is reported. The controller is busy until the status storage is complete.

6-2.1.3 Rewind Selected Transport (interrupt disabled). This mode of operation causes the addressed tape unit to rewind to the BOT marker. Once the rewind is initiated, an operation complete status is stored (without an interrupt). The controller is busy until the status storage is complete. When the rewind is completed, a rewind complete status is stored (without an interrupt).

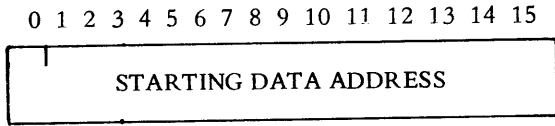
6-2.1.4 Acquire List and Initiate Specified Operation. This mode of operation causes the tape controller to acquire a list via the BTC, and to initiate the specified operation on the selected transport. Once the specified operation is completed (or aborted), the appropriate status is stored. An interrupt precedes the status storage only if enabled during list acquisition. The controller is busy until the status storage is completed.

6-2.1.5 Clear Command. If bits 11 and 12 of the first activate word are both logic ZERO, a clear command is indicated. This causes the entire tape control logic to be reset. A clear command is unconditionally accepted by the controller, whether the controller is busy or idle. All other commands are accepted by the controller only if it is not busy (idle).

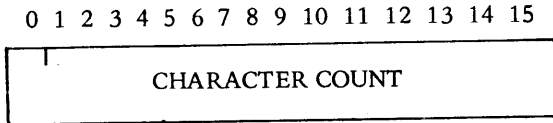
6-2.2 ACTIVATE WORD 2.



6-2.3 LIST WORD 1.

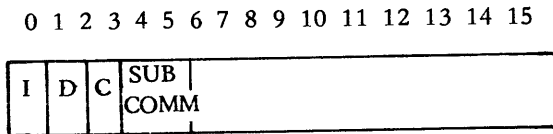


6-2.4 LIST WORD 2.



List word 2 contains the number (in binary format) of 8-bit data characters to be transferred during a data transfer operation. A zero character count for a read or write binary command is allowed, but will only cause an operation complete status to be stored (nothing written on tape).

6-2.5 LIST WORD 3.



List word 3 contains the parameters required by the tape control logic to properly execute a non-rewind operation. The BTC acquires this word from memory and supplies it to the TCL. These bits are defined as follows.

- Bit 0 Interrupt bit. A logic ONE enables the controller to issue an interrupt prior to status storage for a list operation. A logic ZERO causes status to be stored without an interrupt.

- Bit 1 Direction bit. A logic ZERO indicates the forward direction and a logic ONE indicates the reverse direction. It is used only when the operation specified is a record skip.

- Bit 2 Chain bit. A logic ONE indicates that the controller is to acquire another list after completing the current operation. A logic ZERO indicates no chaining. Chaining must specify the same operation and direction.

Bits 3, 4, 5

Subcommand bits. These bits are coded as follows to indicate the desired operation.

BIT	3	4	5	
	0	0	0	Read Binary Forward
	0	0	1	Record Skip
	1	0	0	Write Binary Forward
	1	0	1	Erase Forward
	1	1	0	Write End of File Code
	0	1	0	} No Operation
	0	1	1	
	1	1	1	

6-2.5.1 Read Binary. In a read binary forward operation data is transferred by characters from tape into a buffer register within the controller from which it is assembled into words for transfer to memory. In the transfer of an odd number of characters, the last half of the last word is loaded with all ONE's. Characters are read sequentially from tape and loaded into successive memory words with the first character being loaded into the left (most significant) half of the first word and the next character being loaded into the right (least significant) half of the first word. The direction bit is ignored for a read binary.

6-2.5.2 Record Skip. In a record skip operation, either forward or reverse, the read head is allowed to pass over the next successive record until an inter-record gap is detected. Detection of a file mark code also constitutes a record skipped with the appropriate status reported. The direction bit determines the direction of tape motion.

6-2.5.3 Write Binary. In a write binary forward data words are transferred from memory to the controller where they are disassembled into characters for writing on tape. The left (most significant) half of the data word is written on tape first followed by the character from the right (least

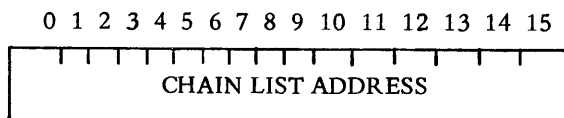
significant) half of the data word. If an odd number of characters is specified, the least significant half of the last data word is ignored. The direction bit is ignored for this operation.

6-2.5.4 Erase. In an erase forward operation the tape is brought up to speed and 88.9 millimetres (3.5 inches) of tape are erased. The direction bit is ignored for this operation.

6-2.5.5 Write End of File. In a write end of file operation the tape is brought up to speed, 88.9 millimetres (3.5 inches) of tape are erased, and the end-of-file code (23)₈ is written. The direction bit is ignored for this operation.

6-2.5.6 No-Op. When a no-op is specified, the controller sets the operation complete status bit and proceeds with a status cycle. Chaining is not allowed when a no-op is specified.

6-2.6 LIST WORD 4.



List word 4 contains the address of the next list to be acquired if chaining is indicated by bit 2 of list word 3. If chaining is not indicated, this word is ignored. List word 4 is registered by the BTC.

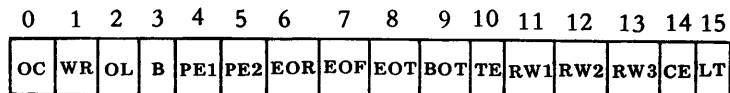
Chaining enables the controller to acquire data from more than one memory buffer with the CPU issuing only one ATI or ADAC command. In chaining from a read binary to a read binary or from a write binary to a write binary, the chaining is always intrarecord, never between records.

6-2.7 STATUS WORDS. The controller is capable of reporting status at appropriate times. Status is stored as a result of the following conditions:

- a. When a non-chained list operation or a rewind operation is successfully completed
- b. When a chained list operation is successfully completed and succeeding list acquisition is accomplished
- c. When a condition occurs that forces an operation to be aborted
- d. When a condition occurs that prevents an operation from being initiated

Status is reported as either one or two words of 16 bits. Two words are stored when a data transfer operation is executed (read binary or write binary). All non-data-transfer operations result in a single word status storage.

6-2.7.1 Status Word 1.



Status Word 1 is supplied by the TCL to the BTC for storage in memory. Significance and definition of the tape controller status word bits are listed below:

Bit 0 Operation Complete (OC). The operation complete bit is set to a logic ONE under the following circumstances.

A REWIND is successfully initiated.

A NO-OP is indicated by List Word 3.

A zero character count accompanies a READ BINARY or a WRITE BINARY.

A list operation that is not chained to a succeeding list is successfully completed.

This status bit causes status storage.

Bit 1 Write Ring (WR). The write ring bit is set to a logic ONE when a WRITE operation is specified and there is no write ring inserted in the transport file reel. This is an abortive status condition and causes status storage.

Bit 2 Offline (OL). The offline status bit is set to a logic ONE when the transport addressed is not ready (offline) and is not in the REWIND mode. This is an abortive status condition.

Bit 3 Busy (B). The busy status bit is set to a logic ONE when the controller receives an activate word (1) while still executing a previous operation, (2) after completing an operation but

waiting to store status, or (3) while the addressed transport is rewinding. The controller is busy until a terminating status storage occurs. Busy status is stored as soon as a status memory cycle can be initiated (with or without an interrupt as previously defined). The status cycle for busy status only is non-terminating except when the addressed transport is rewinding.

Bit 4 CPU/Controller Parity Error (PE1). The CPU/controller parity error status bit is set to a logic ONE when a parity error is detected while transferring data between the CPU and the controller. This status is non-abortive and is stored only when a status storage condition occurs.

Bit 5 Controller/Transport Parity Error (PE1). The controller/transport parity error status bit is set to a logic ONE when one of the following conditions occur.

A read-after-write (character parity) error is detected during a WRITE BINARY operation.

A character parity error is detected during a READ BINARY operation.

A track parity error is detected (LRC check) during either a WRITE BINARY or READ BINARY operation.

This status is non-abortive, represents one or more of the errors described above, and is stored only when a status storage condition occurs.

Bit 6 End-of-Record (EOR). The end-of-record status bit is set to a logic ONE when a READ BINARY operation specified more characters to be read than actually exists in the tape record. This is an abortive status condition and causes status storage.

Bit 7 End-of-File (EOF). The end-of-file status bit is set to a logic ONE when a

Bit 8

READ BINARY FORWARD or a RECORD SKIP is initiated and the next record on tape is the file mark code. This is an abortive status condition and causes status storage.

End-of-Tape (EOT). The end-of-tape status bit is set to a logic ONE when the EOT marker is detected while the tape is moving in the forward direction. This is a non-abortive status and is reported when the next status storage condition occurs. EOT status may be reported more than once if more than one status storage condition occurs while the EOT sensor is positioned over the EOT marker.

EOT status is reported (alone) if a READ BINARY is initiated and no data is found prior to detecting the EOT marker.

Bit 9

Beginning-of-Tape (BOT). The beginning-of-tape status bit is set to a logic ONE if the BOT marker is detected while executing a RECORD SKIP (REVERSE). This is an abortive status condition and causes status storage.

Bit 10

Timing Error (TE). The timing error status bit is set to a logic ONE when the controller fails to transfer a data word between core memory and the controller data register in sufficient time to maintain the proper data transfer rate between the controller and the tape drive. This is an abortive status condition and causes status storage. In the case of a WRITE BINARY operation, the CRC and LRC characters are not written on tape.

Bits 11, 12, 13

Rewind Complete (RW). The rewind complete bit (RW1, RW2, RW3) is set to a logic ONE when the corresponding transport completes a previously initiated rewind. This is a non-abortive status condition and status is stored as soon as a status memory cycle can be initiated. Whether or not an interrupt occurs

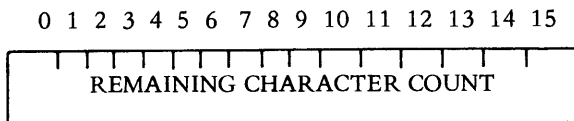
prior to storing status depends on the most recent REWIND command. (See Paragraph 2-2.1.)

Bit 14 Command Error (CE). The command error status bit is set to a logic ONE when the chain list acquired does not specify the same operation as the previous list (which specified the chaining). In the case of a RECORD SKIP operation, the direction must also be the same. This is an abortive status and causes status storage. An interrupt is determined by the list which causes the chain list acquisition.

Bit 15 List Taken (LT). The list taken status bit is set to a logic ONE when the operation specified by a list is completed, the list indicated chaining, the succeeding list has been acquired, and the operation is the same as specified by the previous list. This is a non-abortive status, and status is stored as soon as a status store cycle can be initiated. An interrupt is issued only if the new (chained) list indicates that interrupting is enabled.

Status word 1 is supplied by the TCL to the BTC for storage in memory.

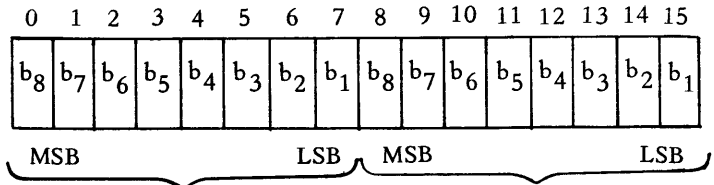
6-2.7.2 Status Word 2.



The second status word is stored when a data transfer operation is executed. This word will contain the remaining character count if an EOR status occurs during a read binary operation or if a write binary operation is aborted. If a data transfer operation is successfully completed, the second status word will be all ZERO's.

The second status word is actually the value remaining in the character count register of the BTC and is stored when the TCL indicates to the BTC that two status words are to be stored.

6-2.8 DATA WORD. The tape transport handles an 8-bit character plus 1 parity bit. The tape transport controller transfers 16-bit (two-character) words to or from memory. Character packing is shown below.



FIRST CHARACTER

SECOND CHARACTER

When an odd number of characters is being transferred, the controller ignores bits 8 through 15 if the operation is a write binary, and if the operation is a read binary, bits 8 through 15 are loaded with ONE's [(FF)₁₆].

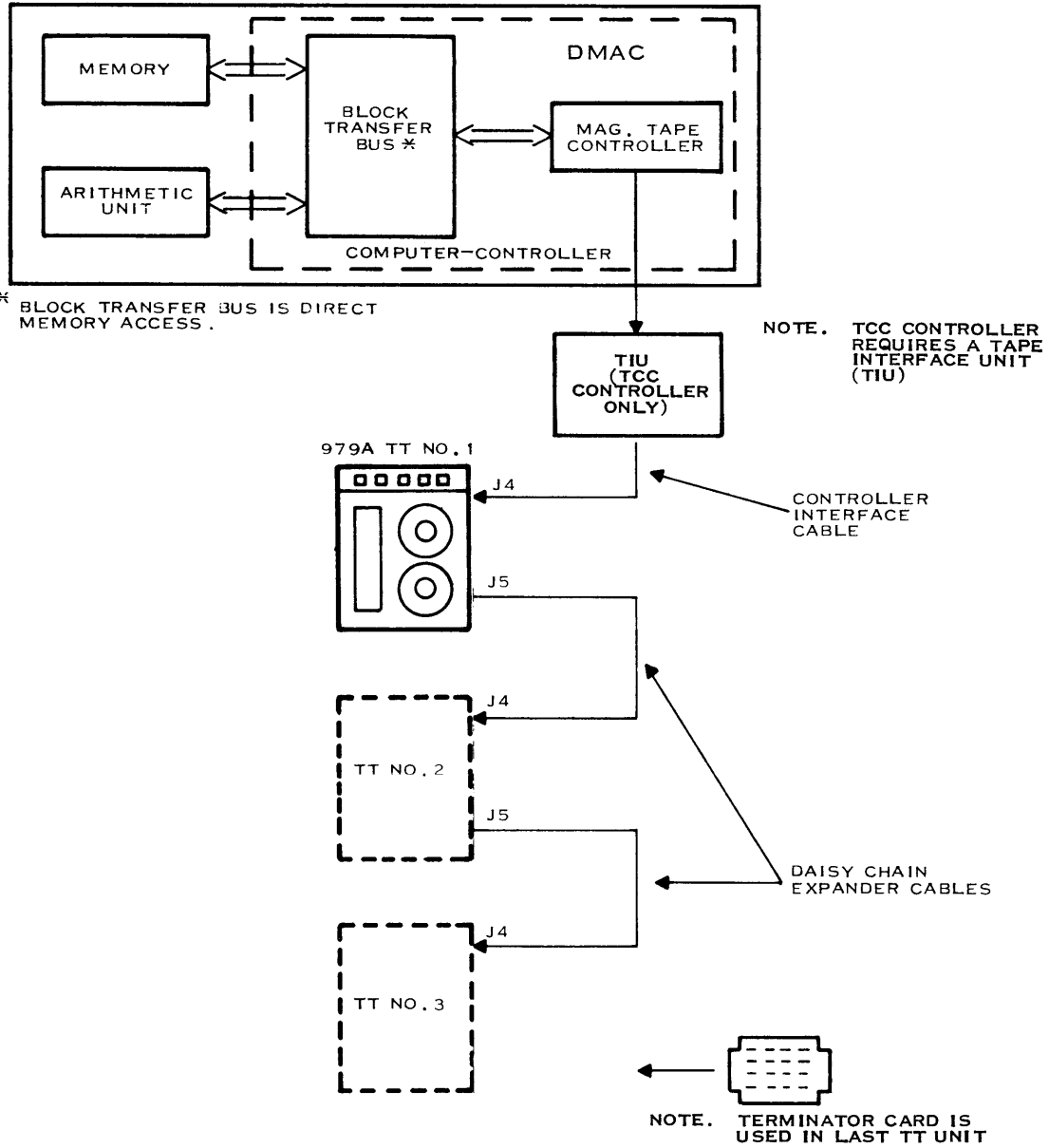
6-4 INSTALLATION.

A functional diagram of the tape transport interface is shown in Figure 6-1. There are two configurations for the Model 979A Tape Transport systems used in a 960/980 environment. One configuration consists of nine controller cards; the other consists of seven controller cards plus a Tape Interface Unit (TIU). Nine controller cards are used in an NRZI (800-bpi) configuration and seven controller cards in PE (1600-bpi) configuration. Both configurations use a Block Transfer Controller (BTC). For NRZI systems, six Tape Control Logic (TCL) cards are used in addition to the BTC. In PE systems four Tape Command Controller (TCC) cards are used. See Figures 6-2 and 6-3 for DMAC slot assignments in the two configurations. Interconnection diagrams are shown in Figures 6-4 and 6-5.

More detailed information may be found in the "Model 979A Tape Transport Subsystem Maintenance Manual" (TI Part No. 949613-9701).

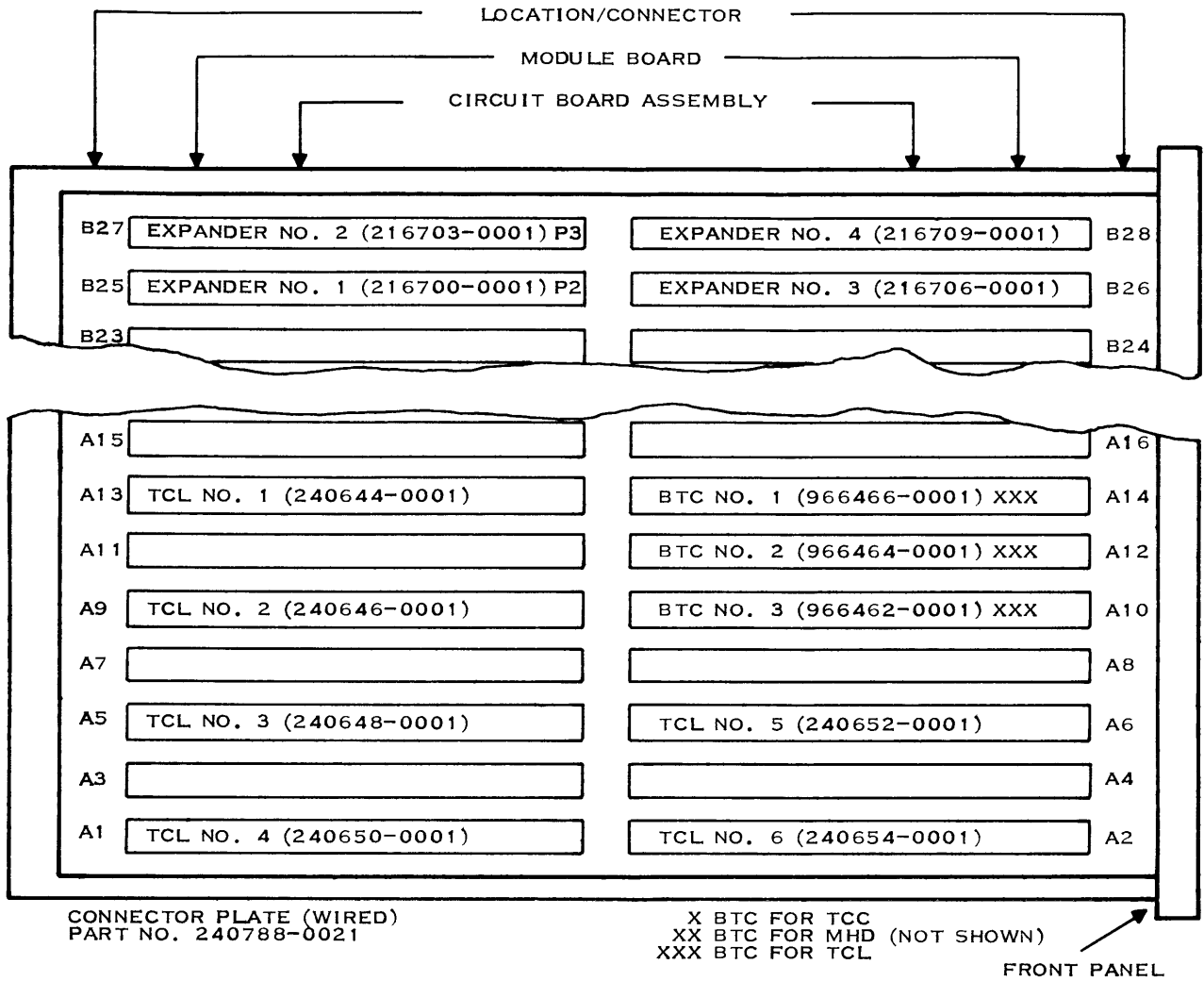
6-5 CHARACTERISTICS.

Characteristics of the Model 979A Tape Transport are listed in Table 6-1. Outline drawings for the tape transport are shown in Figure 6-6, and Figure 6-7 shows the dimensions of a TIU used in the PE system.



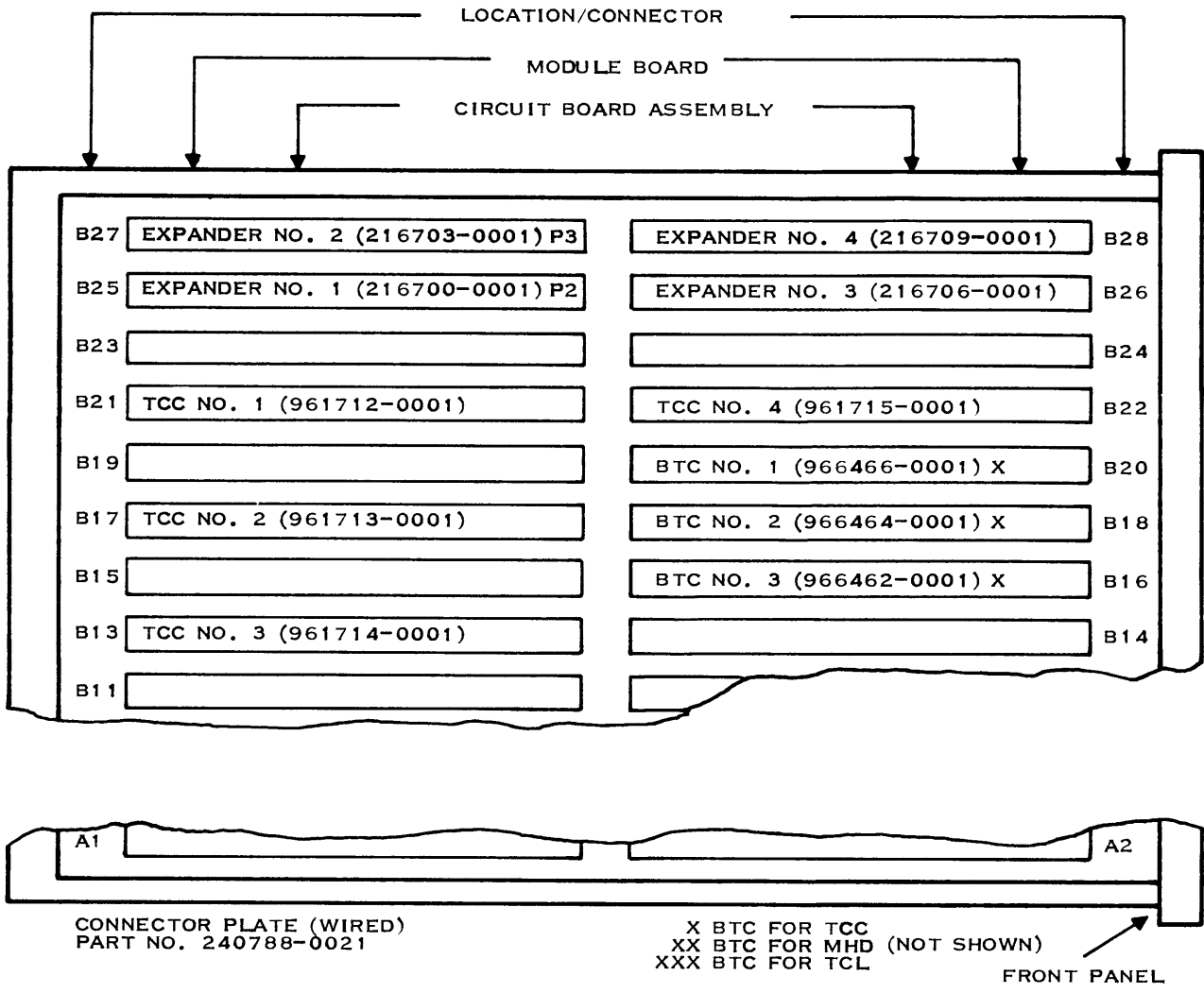
(A) 133969C

FIGURE 6-1. COMPUTER-TAPE TRANSPORT SYSTEM CONFIGURATION



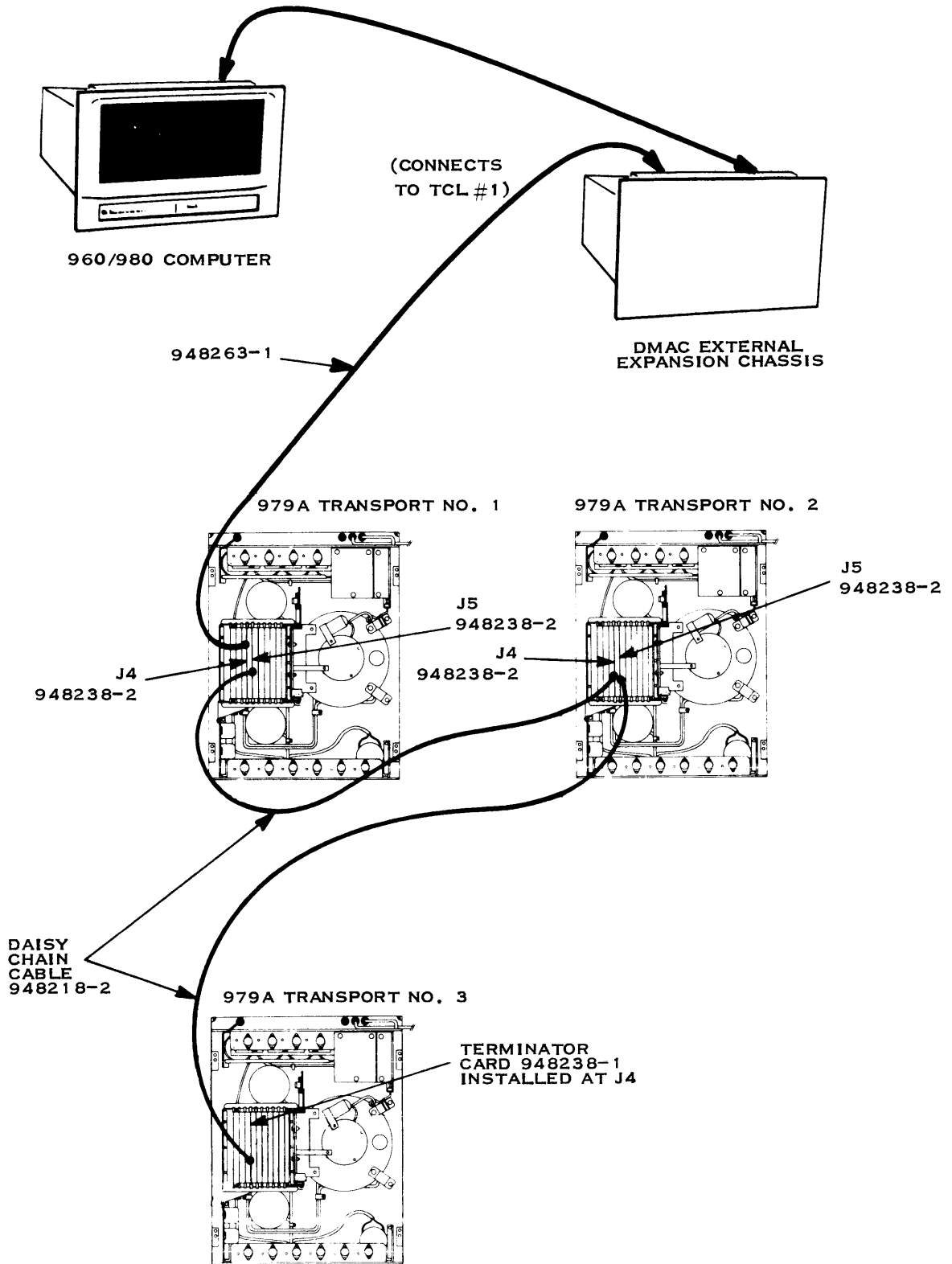
(A) 138388

**FIGURE 6-2. DMAC EXTERNAL EXPANSION CHASSIS 979A TAPE SYSTEM
INTERFACE/CONTROLLER, 960/980 SYSTEM, NRZI FORMAT ONLY**



(A) 138392

**FIGURE 6-3. DMAC EXTERNAL EXPANSION CHASSIS 979A TAPE SYSTEM
INTERFACE/CONTROLLER, 960/980 PE/NRZI FORMAT**



(A) 138389A

FIGURE 6-4. 979A INTERCONNECTION 960/980 SYSTEM, NRZI ONLY

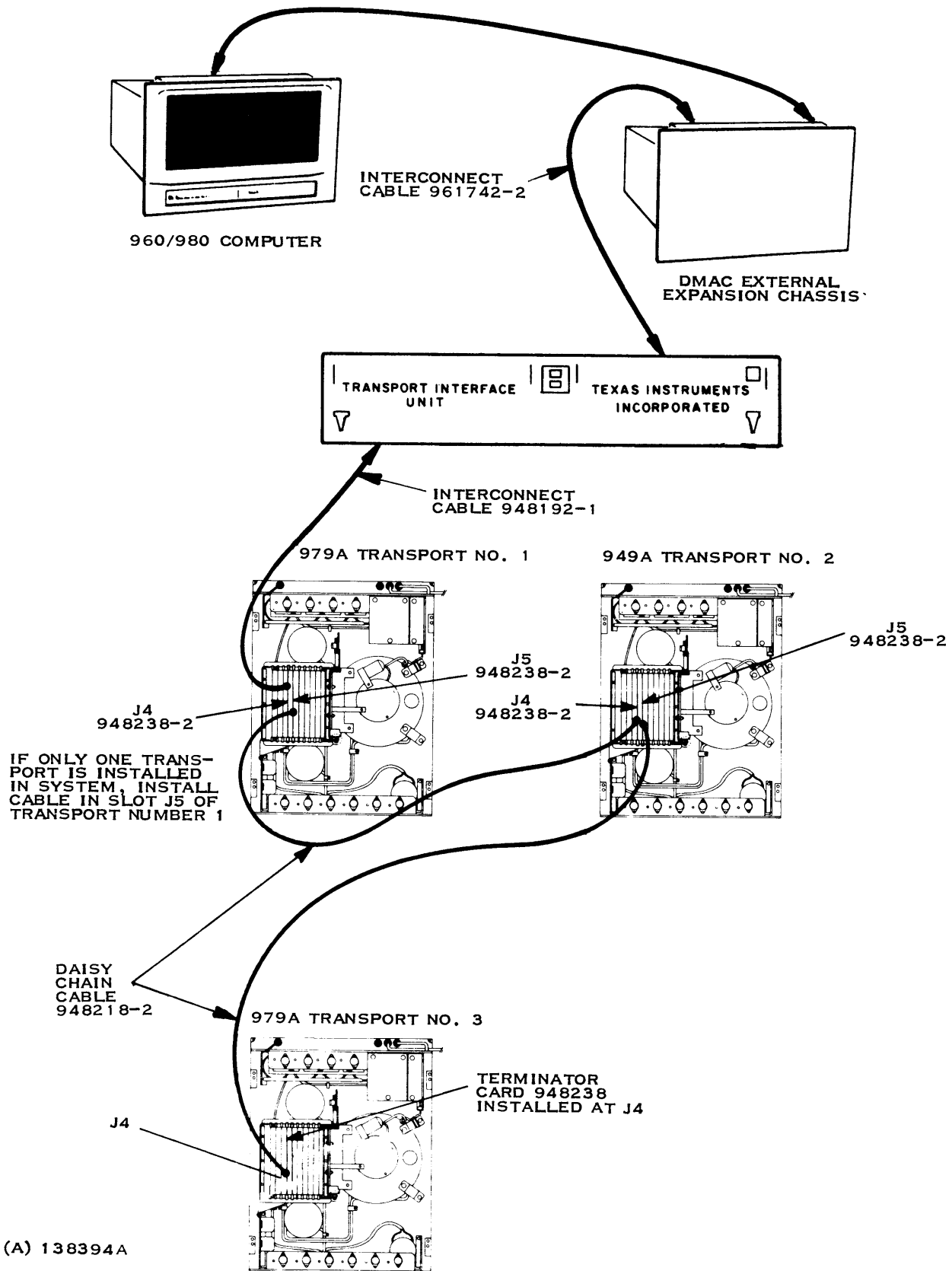
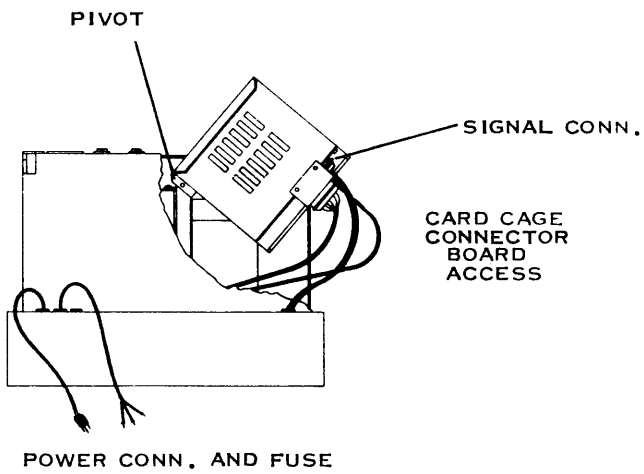


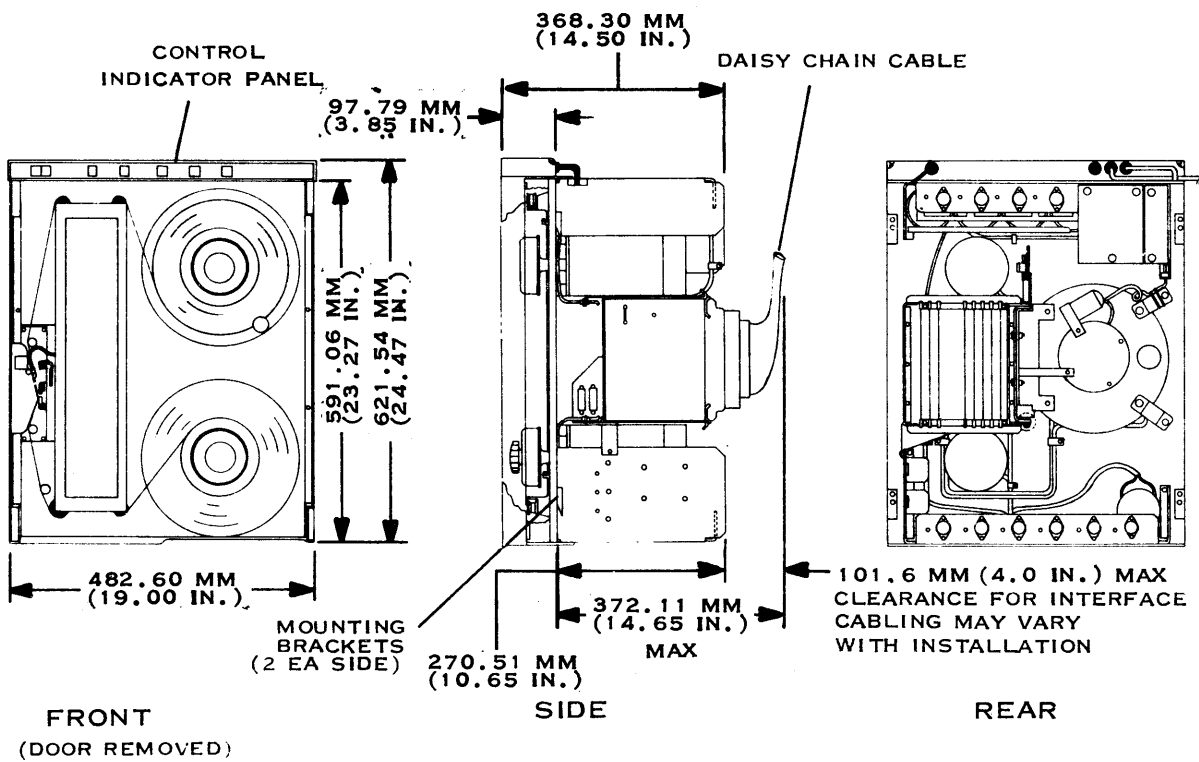
FIGURE 6-5. 979A INTERCONNECTION 960/980 SYSTEM, PE/NRZI FORMAT

Table 6-1. Model 979A Tape Transport Specifications

Features	Multiple-unit operation, file protect ring sensor, BOT and EOT detection, automatic unloading, no programming restrictions, electronic read/write deskew
Characteristics	
Format	9-track NRZI, 800 bpi or 9-track PE, 1600 bpi
Head	Read after write dual gap, 9-track with edge relief slots
Reel	152 to 267 mm (6 to 10.5 in.) IBM or NAB
Tape, width	12.7 mm nominal (12.649 ±0.051 mm) (0.5 in. nominal: 0.498 ±0.002 in.)
thickness	0.038 mm nominal (1.5 mils nominal)
tension	(8 ± 1 oz)
Tape Speed	37.5 ips ±2% long term, ±3% short term
Rewind Time	200 sec max (for 732-m (2400-ft) reel)
Start and Stop Time	10.1 milliseconds ± 10%
Start Distance	4.83 mm (0.19 in.) ± 10%
Stop Distance	5.59 mm (0.22 in.) ± 10%
Skew, static	Electronically adjusted within ±0.5 microns (±20 microinches), read and write
dynamic	Less than 5 microns (200 microinches), peak-to-peak
Head Gap Scatter	Less than 2 microns (75 microinches)
Tape Creepage	Tape motion is zero in absence of drive command.
Reel Jogging	Reel motion is zero for up to 50 hours absence of tape drive for any combination of tape footage.
Reliability	2000 hours MTBF, less than 2 hours MTTR
Site Preparation	
Electrical*	105-125 Vac, 57-63 Hz, 10 amperes maximum, 4 amperes nominal
Dimensions (see Figure 6-6)	
Height	622.30 mm (24.50 in.)
Width	482.60 mm (19.00 in.)
Depth Behind Panel	330.20 mm (13.00 in.), excluding connectors
Depth Overall	419.10 mm (16.50 in.), including connectors
Weight	61 kg (135 lb)
Mounting	Standard EIA 19-inch (483-mm) rack, using quick-set mounting hangers, hardware-supplied
Environment	
Temperature	10° to 32°C (50° to 90°F)
Relative Humidity	20 to 80%
Altitude	1829 m (6000 ft) at 60 Hz input
Shock Acceleration	10 g's any axis when in shipping container
Heat Output	Approximately 1.9 MJ/hr (1800 BTU/hr)
Cooling Requirements	Sufficient cooling must be provided to maintain less than 50°C (122°F) air temperature behind transport plate.
*115 Vac, 50 Hz power optional (An accessory 230/115 Vac transformer is available for operation on 230 Vac mains.)	



TOP



(B) 133953B

FIGURE 6-6. MODEL 979A TAPE TRANSPORT PHYSICAL DETAILS

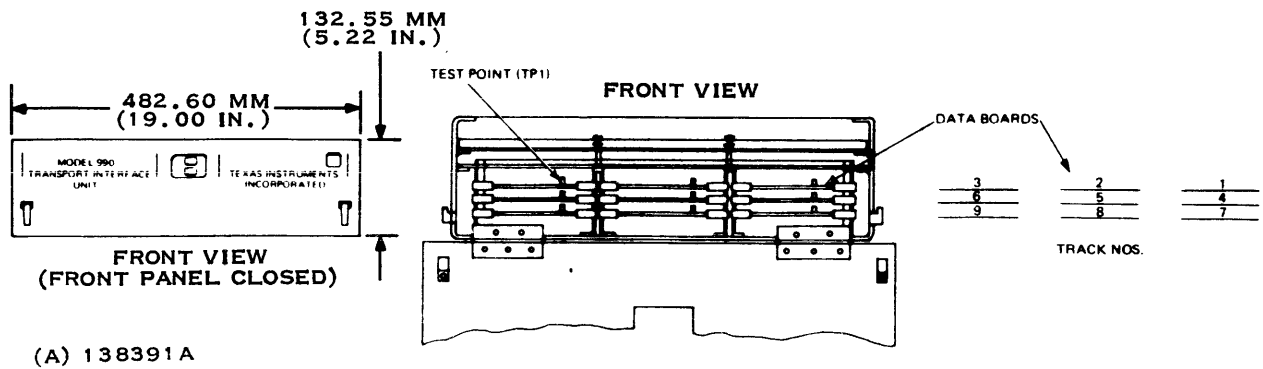
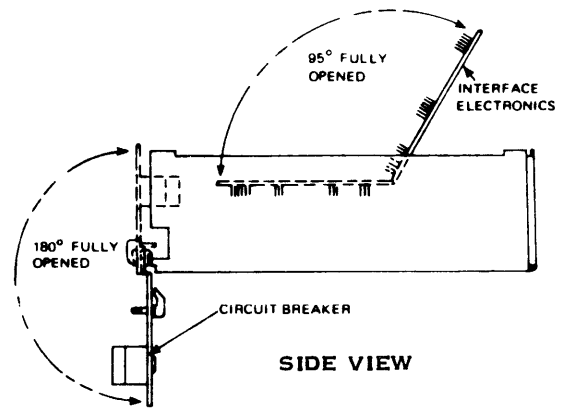
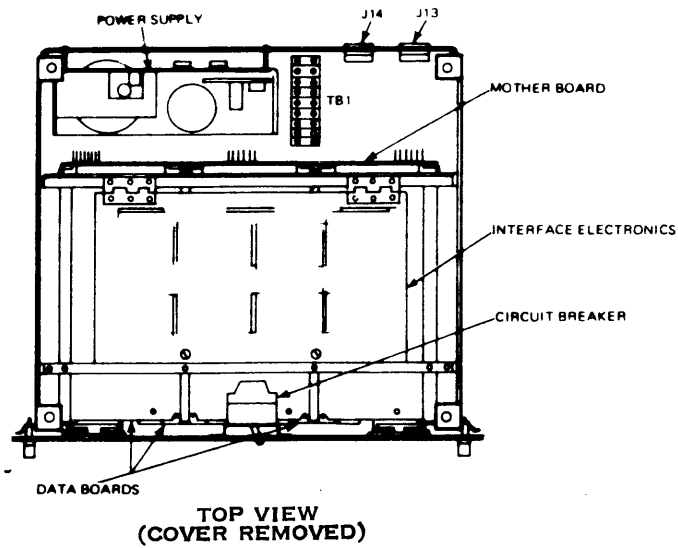


FIGURE 6-7. MODEL 990 TRANSPORT INTERFACE UNIT

FOLD

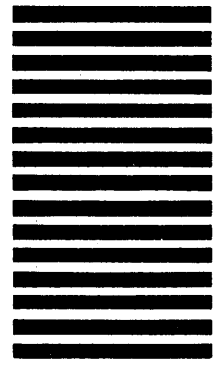


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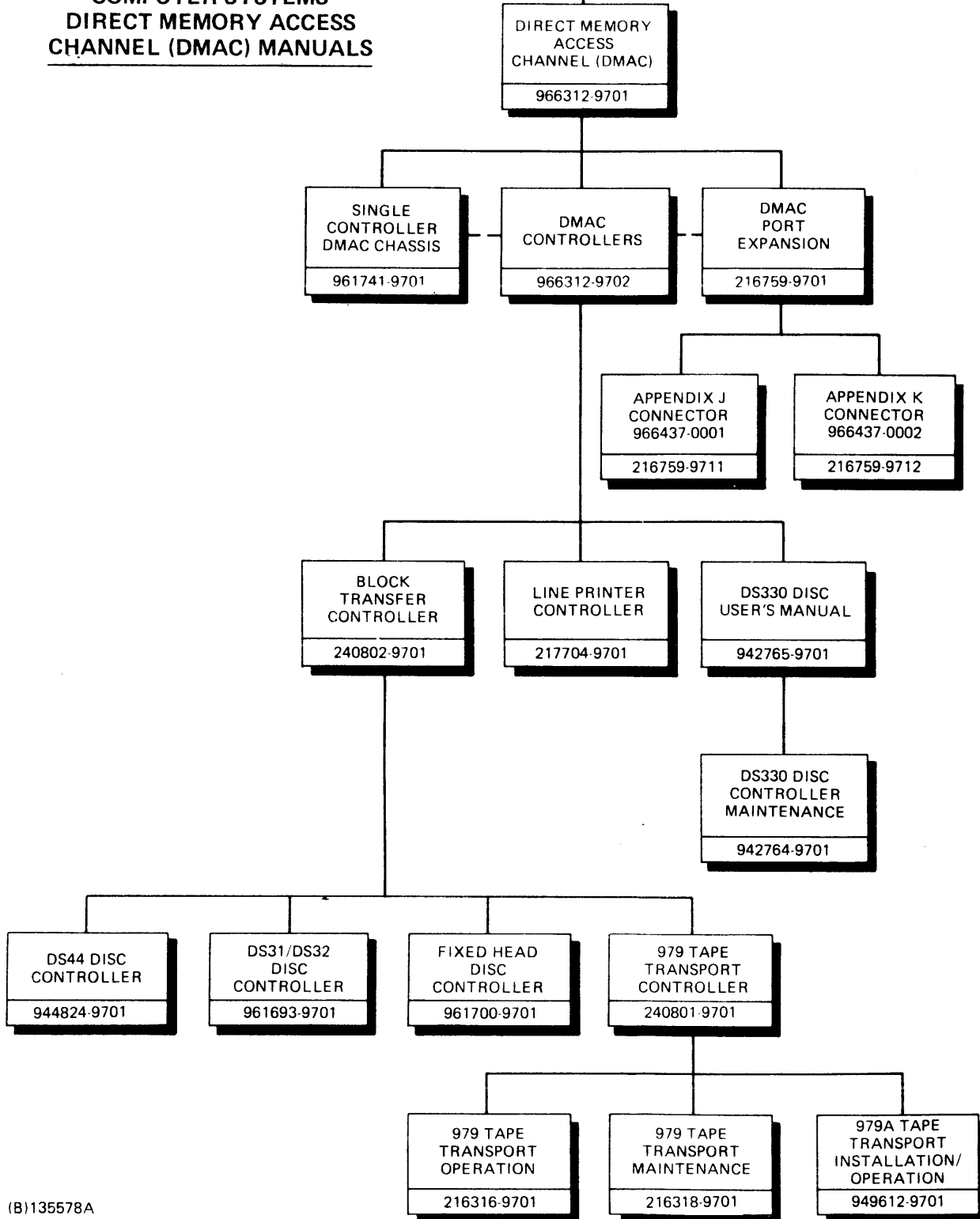
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