TEXAS INSTRUMENTS

Improving Man's Effectiveness Through Electronics

Model 960 Computer

Communications Register Unit
Interval Timer Module
User's Manual

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PREFACE

This manual describes the installation, use, operation, and maintenance of the Interval Timer Module with Texas Instruments' Models 960A and 960B computers. Assembly language programmers, system designers and maintenance personnel will find the information in this manual useful.

The Interval Timer Module interfaces with the 960 series of computers through the Communications Register Unit (CRU). A basic knowledge of this interface is assumed and can be reviewed in the *Model 960 Computer Communications Register Unit Manual* (Manual Number 966313-9701) furnished with each system. Detailed descriptions of CRU input and output instructions are found in the *Model 960 Computer Assembly Language Programmer's Reference Manual* (Manual Number 942779-9701). That manual also describes assembly language programming and input/output techniques. Central Processing Unit (CPU) memory and bootstrap loader initialization are described in the *Model 960 Computer Installation Procedure* (Manual Number 942767-9701).

Information about the Model 960A and Model 960B computers can be found in the following manuals:

Manual Number	Title
226750-9707	*Model 960A Computer Maintenance Manual: Parts List and Assembly Drawings, Volume VII*
226750-9708	*Model 960A Computer Maintenance Manual: Electrical Drawings, Volume VIII*
942773-9704	*Model 960B Computer Maintenance Manual: Parts List and Assembly Drawings*
942773-9705	*Model 960B Computer Maintenance Manual: Electrical Drawings*
958953-9701	*Central Processing Unit Performance Assurance Tests for the Model 960 Computer*
942779-9701	*Model 960 Computer Assembly Language Programmer's Reference Manual*

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SECTION I

GENERAL DESCRIPTION AND INSTALLATION

1.1 GENERAL DESCRIPTION

The Interval Timer Module (figure 1-1) supplies real-time information to the operating system software. A 1, 2, 4, or 8 millisecond (ms) time base can be selected by the user. The module contains a 14-bit program-loadable counter (16,384 maximum counts) that decrements at a rate specified by the time base. An interrupt is issued when the counter reaches zero; however, the counter continues to decrement past zero to prevent the loss of counts.

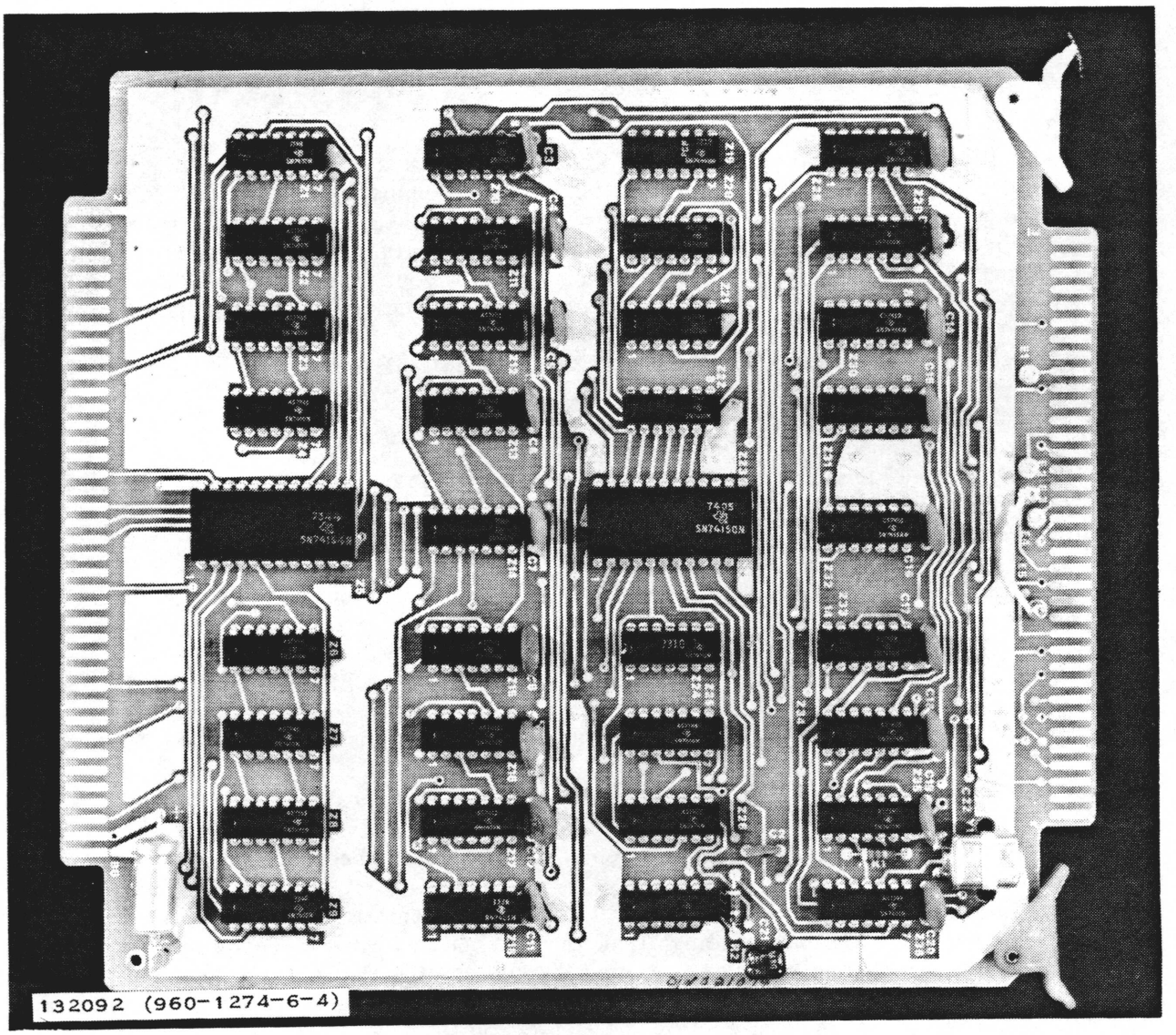

Figure 1-1. Interval Timer Module

There are four configurations of the module available and their differences (the time base) are shown in table 1-1.

Normally, one interval timer per system is adequate. However, additional Interval Timer Modules can be added if additional time bases are required. The modules can be inserted in any CRU port.

The count-down logic of the base module clock supplies free-running clock signals to the top-edge connector of the module. The basic interval timer has a 4.096 MHz clock that is divided down to provide the user selected time base. The top-edge connector clock signals represent the binary multiples of 8 ms divided by 8192 (0.997 microseconds). For example, the limits and several signals from the range of outputs are:

8/8192, 8/4096, 8/2048, . . . , 1, 2, 4, and 8 ms (upper limit)

These clock outputs are available for module test; however, they can also be used by other elements of the system.

The module characteristics are summarized in table 1-2.

1.2 INSTALLATION

Installation of the Interval Timer Module involves time base selection, slot selection, and, possibly, attaching a cable between the top-edge connector of the module and a system component. The following paragraphs provide the detailed information for time base and slot selection. Table 4-1 describes the pin assignments for the top-edge connector and should be referenced when specifying the cable connections for routing the interval timer clock output to an external system device. These considerations are summarized in the installation procedure.

1.2.1 TIME BASE SELECTION. Time base increments of 1, 2, 4, and 8 ms are available. These time increments are selectable by jumpers as listed in table 1-3.

Jumpers are connected between staked terminals using a 20- to 30-watt soldering iron and 22 to 26 gauge, single conductor, insulated wire. Figure 1-2 shows an Interval Timer Module jumpered for a 1 ms time base. The PAM and PAM/D monitors usually use a timer jumpered for a 1 millisecond time base.

1.2.2 SLOT LOCATION. The Interval Timer Module can be installed in any CRU location. These locations are:

- Standard Internal Ports (computer chassis locations EF0, EF1, EF2 and EF3)
- Internal Expansion Ports (computer chassis locations EF4 through EFF)
- External Expansion Ports (expansion chassis locations)

Figure 1-3 illustrates the connections required to generate the module in any of these locations.

The location of the module within the computer chassis or within an expansion chassis determines the CRU base address that the module recognizes. Therefore, before selecting a chassis location for the module, determine the address that the software handling routine expects the module to recognize. PAM and PAM/D systems generally expect the Interval Timer Module to be located in slot marked EF3 on the escutcheon (usually referred to as slot '0F30').

Table 1-1. Interval Timer Module Configurations

Part Number	Description	
214114-0001	Interval timer	1 ms time base
214114-0002	Interval timer	2 ms time base
214114-0003	Interval timer	4 ms time base
214114-0004	Interval timer	8 ms time base

Table 1-2. Interval Timer Module Specifications

Characteristic	Specification
Resolution:	1, 2, 4, or 8 milliseconds (selected by wire jumper)
Maximum Count:	16,384 time increments
Interrupt:	At count = 0 timer causes interrupt, but continues to count negative to prevent any loss of real-time due to interrupt servicing by the computer.
Maximum Time Interval Measured:	Unlimited. Software can load the timer at periodic intervals to keep time indefinitely.
Power Requirements:	+5.0 Vdc @ 0.5A

Table 1-3. Time Interval Jumper Configurations

Time	Jumper*
1 ms	E3-E5
2 ms	E4-E5
4 ms	E2-E5
8 ms	E1-E5

*E1, E2, E3, E4, and E5 are terminals staked to the module.

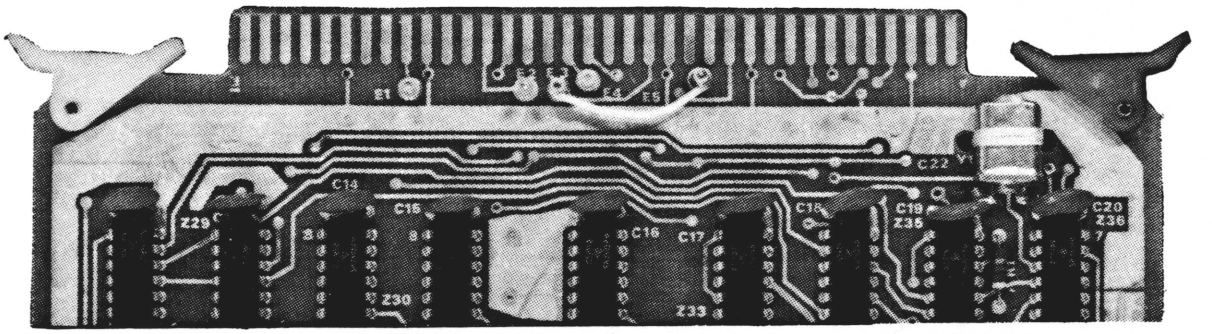

Figure 1-2. Time Base Interval Adjustments

1.2.3 **INSTALLATION PROCEDURE.** After determining the modules location and installing the proper jumper for the selected time base, perform the following steps for installation:

1. Set the ON/OF (CPU power) switch, on the power supply, to the OFF position.

2. Plug the module into the selected chassis location with the component side of the board facing the front of the computer chassis or facing the buffer board in an expansion chassis.

NOTE

Custom cables can be assembled for special application by ordering cable connector and cover (TI part no. 217081-0001) for cables 9.5 mm (3/8-inch) or less; for cables 12.7 mm (1/2-inch) or less, TI part no. 217081-0002 is available. These connectors mate with the 72-pin edge connector on the top edge of the module.

3. If required, connect the custom cable between the interval timer and the system component to receive free-running clocks.

4. Set the ON/OFF (CPU power) switch, on the power supply, to the ON position.

5. Perform the Performance Demonstration Test (PDT) for the Interval Timer Module (described in Section VIII).

6. Installation is complete after successful completion of the PDT. Refer to the maintenance section if the test fails to execute properly.

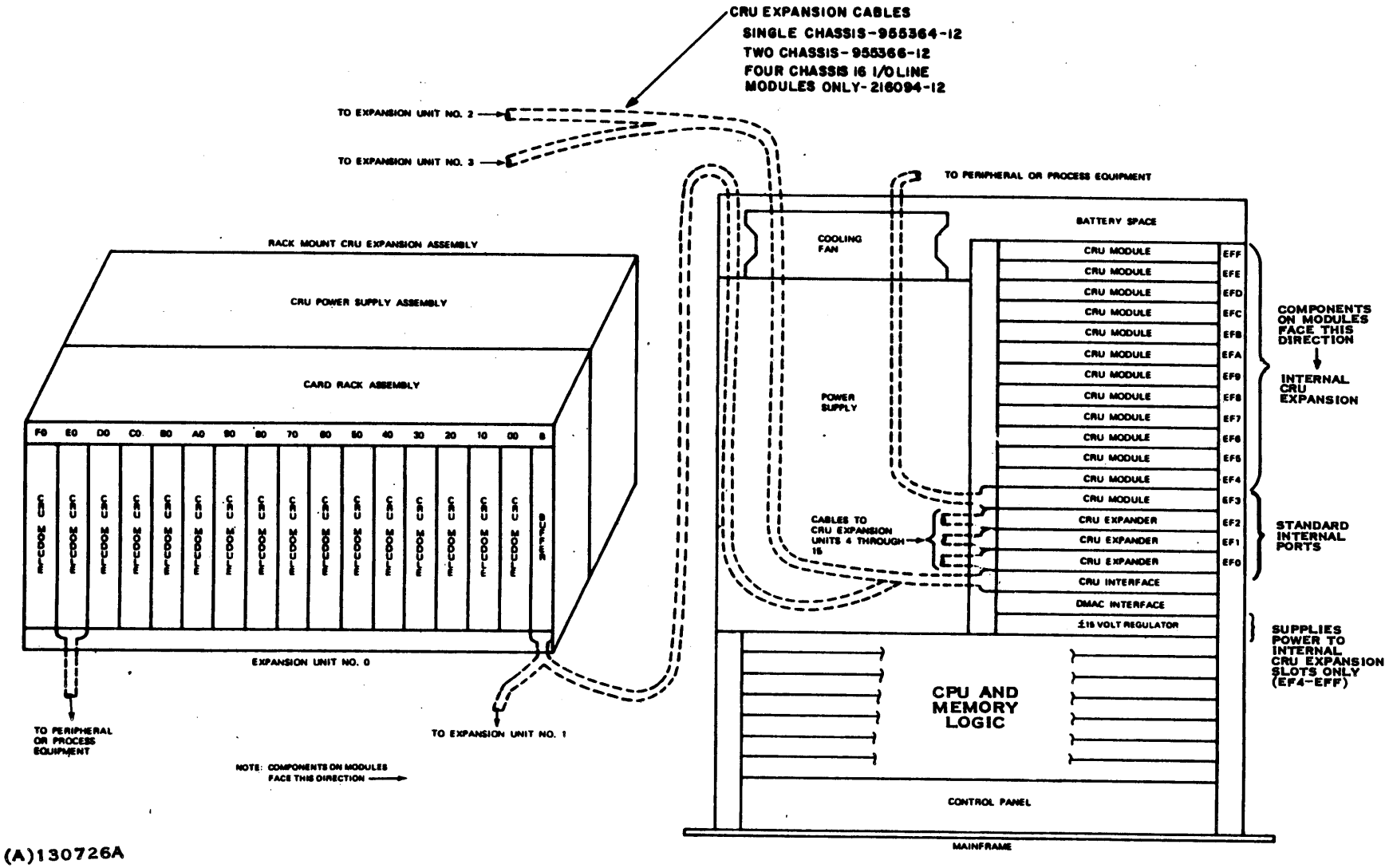

Figure 1-3. CRU Mechanical Configurations

SECTION II

OPERATING INSTRUCTIONS

2.1 GENERAL

Operation of the Interval Timer Module consists entirely of the programming required to initialize, control, and read the timer counter. The CRU instructions such as SETB, BBNE, XBNE, TSBX, LDCR, and STCR are used to implement software routines to handle the Interval Timer Module. CRU instruction formats are included in Section IV.

The interface between the computer and the Interval Timer Module consists of 16 input lines and 16 output lines. Individual bits (lines) or fields of 2 to 16 bits are addressed using CRU instructions. The significance of each input and output line is summarized in table 2-1.

2.2 PROGRAMMING CONSIDERATIONS

The Interval Timer Module is loaded with a count through program control. This count is decremented at a rate determined by the time base (selected by jumpers on the module). When the count reaches zero, an interrupt request is issued. For example, if an interrupt is needed every 100 milliseconds (ms) and the time base decrements the counter every 1 ms, the counter is initially loaded with a count of 100. This interrupt, that occurs every 100 ms, could be used to increment a memory location specifying time in milliseconds. Then other instructions could test this location for updating second, hour; day, month, and year information.

Table 2-1. CRU Bit Functions for the Interval Timer

CRU Output Bit Address*	Function	CRU Input Bit Address*	Function
0	0=Clear Interrupt 1=Set Interrupt	0	Timer Interrupt Status: 1=Interrupt
1 • • • 14	14-Bit Counter Initialization Value from CPU – Bit 1 is LSB	1 (LSB) • • • 14 (MSB)	14-Bit Dynamic Count – Bit 1 is LSB
15	1/0 Start/Stop Control	15	Not Used – Always=0

*Add the CRU port address for actual program address.

If the interrupt request is not processed and the timer is not either reloaded or stopped, the counter continues to decrement at the specified rate past zero. After passing zero the value would appear to be negative if read using the STCR instruction to read bits 1-74. The most significant bit read (bit 14) determines the sign assigned to the counter value.

The programming considerations for loading and reading the Interval Timer counter are described and illustrated in the following paragraphs. The programming examples require the assembler directive statements shown in figure 2-1.

2.2.1 **POWER-UP CONSIDERATIONS.** For the undefined condition of the Interval Timer counter following a power-up sequence, the timer should be stopped and reset to a non-zero value N. The number N multiplied by the selected timer interval is the interval to be measured. Clear the Interval Timer interrupt request because an interrupt may be pending due to power transients during power up. The counter must be non-zero before resetting the timer interrupt request, or otherwise, the interrupt request will not be reset. Start the Interval Timer to measure the specified interval. The sequence of instructions to accomplish this initialization function is shown in figure 2-2.

2.2.2 **INTERRUPT SERVICING.** Timer servicing is required when the counter has been decremented to (or past) zero and has issued an interrupt request. In this case the timer generally is not stopped. The dynamic value in the counter is read until two consecutive values are identical. This is necessary because the timer counter and the CPU have asynchronous clocks. The value N, that defines the specified interval, is added to the present counter value; the sum S is then tested to confirm a positive value (not zero or negative). If the value is not positive, then an interval longer than the interval being measured has elapsed since the interval timer interrupt request occurred. A long interval can result, for example, because of CRU interrupt requests being masked for an extended period of time. N is added to the sum S, consecutively, until the value is finally positive. If a memory location is being used to record the number of N duration intervals, then the program would increment this location each time the value N was added to the sum. The final positive sum S ($0 < \text{sum} \leq N$) is now loaded into the Interval Timer counter. The Interval Timer interrupt request is then cleared and CRU interrupt requests are enabled. The coding of a typical Interrupt Timer read and update routine is shown in figure 2-3.

An error is possible using this technique. One basic timing interval (jumper selected) is lost if the counter changes between the read of the counter and the program load of a new timer count. Thus, if the timer is jumpered for a basic interval of 1 ms and the program selects an interval of 100 ms, the worst case error is 1 percent. This is a low probability event, since the timer handler routine usually requires less than 100 microseconds to execute.

Table 2-2 indicates the relationship between elapsed time and counter values. Note in particular the problem caused by a long-term duration between the interrupt and the read of the counter (last column in the table). In this latter case the counter has decremented more than 2063_{16} counts. When the basic program count of 64_{16} is added, the result is positive and consequently only 100 (decimal) is added to the millisecond counter. The actual elapsed time was 8.393 seconds.

TI 960/980 ASSEMBLY CODING FORM

LABEL (1–6)	OPER (8–11)	OPERAND (13–25)	COMMENTS (26–60)
MASKED	EQU	X'01C0'	
CRUDAT	EQU	4	CRU DATA BASE REGISTER
CRUADR	EQU	7	CRU ADDRESS BASE REGISTER
SLOT	EQU	X'0F30'	CRU TIMER LOCATION-SLOT EF3
PRBASE	EQU	5	PROCEDURE BASE REGISTER
TEMP	EQU	1	TEMPORARY STORAGE REG LOC 81
TEMP1	EQU	X'81'	TEMPORARY STORAGE REG LOC 81
TEMP2	EQU	X'82'	TEMPORARY STORAGE REG LOC 82
EQUAL	EQU	11	
SYSCLK	EQU	100	VALUE USED TO SPECIFY INTERVAL
	BSEQ		BIT SEGMENT DEFINITIONS
SSCON	CON	15	CRU BIT 15, START/STOP CONTROL
COUNT	CON	1,14	COUNTER CRU LOCATION IN/OUT
INTRPT	CON	0	CRU BIT 0, INTERRUPT SET/CLEAR

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Figure 2-1. Assembler Directives

TI 960/980 ASSEMBLY CODING FORM

LABEL (1–6)	OPER (8–11)	OPERAND (13–25)	COMMENTS (26–60)
TIMER	LDS	PCVST	MASK INTERRUPTS
*			
START	LA	CRUDAT,SYSCLK	SET UP BASE REGISTERS -DATA
	LA	CRUADR,SLOT	-ADDRESS
	LA	PRBASE,TIMER	-PROGRAM
*			
	SETB	SSCON,0	STOP COUNTER
	LDCR	COUNT,SYSCLK	INITIALIZE INTERVAL COUNTER
	SETB	INTRPT,0	RESET A PENDING INTERRUPT
			/
	LA	TEMP,0	GET ZERO VALUE TO STORE IN THE
	ST	TEMP,MILSEC	MILLISECOND,SECOND,MINUTE,
	ST	TEMP,SEC	HOUR,DAY AND YEAR COUNTER
	ST	TEMP,MINUTE	LOCATIONS
	SETB	SSCON,1	START COUNTER
PCVST	DATA	START,MASKED	START VECTOR
MILSEC	DATA	0	LOCATIONS > MILLISECONDS
SEC	DATA	0	CONTAINING > SECONDS
MINUTE	DATA	0	ELAPSED > MINUTES

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Figure 2-2. Timer Initialization Example

TI 960/980 ASSEMBLY CODING FORM

LABEL (1–6)	OPER (8–11)	OPERAND (13–25)	COMMENTS (26–60)
	LA	CRUDAT,0	SET DATE BASE TO ZERO FOR
*			REFERENCING REGISTER FILE
READ	STCR	COUNT,TEMP1	READ INTERVAL TIMER COUNTER
	STCR	COUNT,TEMP2	TWICE
	CRL	TEMP,TEMP2	COMPARE READS
	BC	EQUAL,$+4	IF EQUAL,THEN COUNT VALID
	B	READ	READ AGAIN, COUNTER CHANGED
*			DURING READ OPERATION
INCR	AA	TEMP,SYSCLK	ADD BASIC TIME OUT PERIOD TO
*			VALUE READ
	CMI	(TEMP1,CRUDAT),0	IS THE REGISTER VALUE POSITIVE
	B	$+4	NO, GO INCR MILLISEC COUNT
	B	LOAD	YES, GO TO END SEGUENCE
	AMI	MILSEC,SYSCLK	NO, INCREMENT MILLEC COUNT
	B	INCR	NOW REPEAT- INCR & TEST
LOAD	LDCR	COUNT, TEMP1	LOAD INTERVAL TMR COUNTER
	SETB	INTRPT,0	RESET INTERRUPT
	AMI	MILSEC,SYSCLK	INCREMENT MILLISECOND TIMER
	CMI	MILSEC,1000	IS VALUE GREATER OR EQUAL 1000
	B	FINIS	NO
	NOP		YES
	B	UPDATE	GO UPDATE SEC,MIN,HOUR,ETC
UPDATE	....		ROUTINE FOR TIME OF DAY
FINIS	....		RETURN TO MAINLINE

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Figure 2-3. Timer Update Example

Table 2-2. Relationships Between Real Time and the Counter Values

	IMMEDIATE READ FOLLOWING INTERRUPT	READ AFTER ONE ADDITIONAL COUNT	DELAYED READ–DELAY INTERVAL GREATER THAN MEASURED INTERVAL	DELAYED READ–ERROR CONDITION
INTERVAL TIME COUNTER VALUE (HEX) WHEN READ	0000	3FFF	3F3C	1F37
VALUE STORED IN MEMORY BY CPU (HEX)	0000	FFFF	FF3C	1F37
CPU VALUE (SUM S) AFTER ADDING 100_{10} (64_{16}) UNTIL POSITIVE	0064	0063	0004	1FAB
AMOUNT PROGRAM ADDS TO ELAPSED MILLISECOND COUNT (DECIMAL)	100	100	200	100
AMOUNT RETURNED TO INTERVAL TIMER COUNTER (HEX)	0064	0063	0004	1FAB

SECTION III

UNIT SPECIFICATION

This section is not applicable to this manual.

SECTION IV

INTERFACE AND MODULE SPECIFICATION

4.1 GENERAL

This section discusses the computer and Interval Timer Module interfaces, the signatures, and pin assignments for these signals, and the functioning of the signal generation circuitry. It also describes control of data transfer and presents the formats of software instructions used for CRU bit and field manipulation. The electrical and physical characteristics of the data module are specified. The jumper schedules for the various options are shown in table 1-1. Figure 4-1 is a block diagram of the Interval Timer.

4.2 CPU INTERFACE

The following paragraphs discuss the interface between the Interval Timer Module and the CPU. They include discussions of connector pin assignments, addressing of individual modules, control signals and data transfer, and CRU input and output instruction formats.

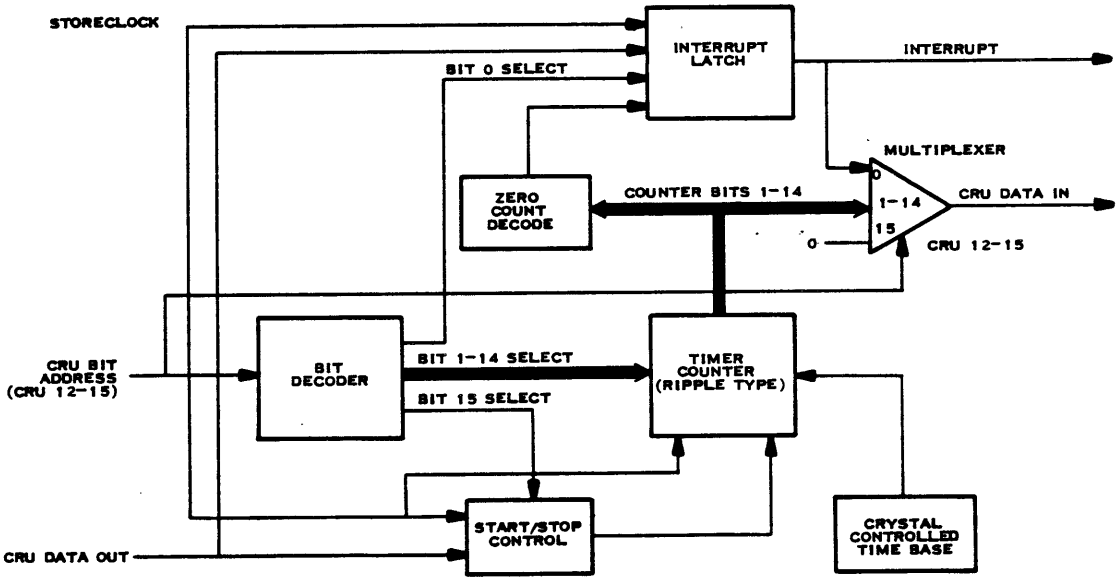


Figure 4-1. Interval Timer Block Diagram

4.2.1 **CONNECTOR PIN ASSIGNMENTS.** The Interval Timer Module interfaces with the CPU through the Communications Register Unit (CRU). This interface is completed through the bottom-edge, 80-pin connector of the module. Table 4-1 lists the interface signal signatures, pin numbers, and descriptions of signals. The logic voltage levels of these signals are TTL-compatible. Signals that are true when the voltage level is low (zero) have signatures that end with a hyphen (-). An example of such a signal signature is CRUSEL0-. This table includes all inputs, outputs, and grounds. All grounds are common and are connected to the CPU digital ground bus. Connection to the module is normally made with 72-pin connector (TI part no. 217081-0001).

The Interval Timer module supplies free-running clock signals to the top-edge connector. Pin assignments for the top-edge connector are specified in table 4-2. The correlation between pin labels and physical position is illustrated in figure 4-2. The free-running clocks are supplied primarily for test purposes; however, external system components can use the clock outputs. Ground pins are adjacent to clock signal pins to facilitate use of twisted-pair wire for signal lines.

4.2.2 **MODULE AND LINE ADDRESSING.** Module selection is accomplished in the CRU interface or Expansion Module by decoding the CRU address rack and module fields (bits 4 through 11) of the CRU base address register. The CRU base address register contains the effective CRU base address. The effective CRU address is calculated by adding the register file

Table 4-1. CPU Interface Signals

Signature	Pin Number	Description
GROUND	1, 2, 79, 80	System ground
CPUDATAOUT	16	Serial data from CPU to module
STORECLOCK-	22	CPU output data strobe
CRUBIT15	34	CRU bit address select line
CRUBIT14	38	CRU bit address select line
CRUBIT13	40	CRU bit address select line
CRUBIT12	42	CRU bit address select line
CRUSEL0-	48	Module select line from CRU rack and slot decode
CRUDATAIN	60	Serial data from module to CPU
CRUMR-	76	Power up/reset
VCC	77, 78	Power, +5 Vdc
CRUINT-	66	Interrupt to CRU

Note: pins 66 and 76 are inputs to CRU all others are output.

Table 4-2. Interval Timer Module Connector Pin Assignments

Pin	Signature/Description	Pin	Signature/Description
1		A	
2		B	
3	GND	C	GND
4	ZERO–	D	T/64
5	INCR	E	
6		F	
7	GND	H	GND
8	T/8192	J	T/32
9	INCR	K	
10		L	
11	GND	M	GND
12	T/4096	N	T/16
13	INCR	P	
14		R	
15	GND	S	GND
16	T/2048	T	1 ms
17	INCR	U	
18		V	
19	GND	W	GND
20	T/1024	X	2 ms
21		Y	
22		Z	
23	GND	a	GND
24	T/512	b	4 ms
25		c	
26		d	
27	GND	e	GND
28	T/256	f	8 ms
29		h	
30		j	
31	GND	k	
32	T/128	l	
33		m	
34		n	
35		p	
36		r	

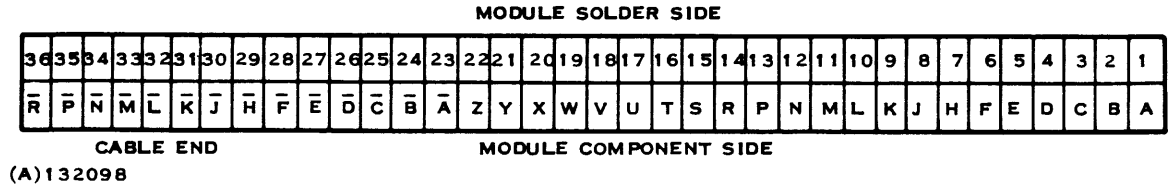
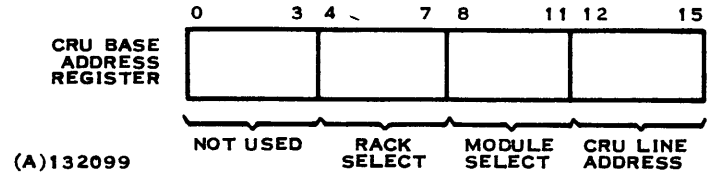


Figure 4-2. Module Connector Pin Arrangement

CRU base address (supervisor mode location 87_{16} or worker mode location $8F_{16}$) and the CRU address field of the instruction being executed. The fields of this address are:



Within the specified chassis (rack) the module select field is decoded to one of sixteen slots. The slot receiving the active select signal, CRUSEL0-, is enabled. The Interval Timer Module is selected by CRUSEL0-. The CRU line address field (bits 12 through 15) determines the specific line or bit to be input or output.

4.2.3 CONTROL AND TRANSFER OF DATA. Data is transferred serially between the Interval Timer Module and the CPU by direct program control. CRU instruction execution selects the module in the port addressed by the effective CRU base address register (contents of memory location 87_{16} or $8F_{16}$ plus the CRU base register modifier). The port of the Interval Timer Module is selected when the CRUSEL0- signal goes true causing the input to be enabled.

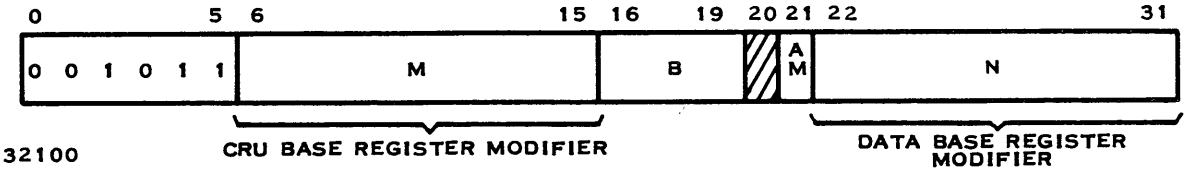
4.2.4 CRU INPUT/OUTPUT INSTRUCTION FORMAT. Each instruction is identified by a unique operation code. In these instructions, the operation code is specified in bit positions 0 through 5 in the instruction word. Other fields included in the formats of the instructions are:

- M and N address fields
- V1 field - immediate value bit, used to specify one of two possible actions or to perform a bit comparison
- AM field - bit that specifies whether alternate mode registers are used; base registers for the inactive mode can be used when the other mode is the execution mode.

Base register relative addressing and alternate mode registers are explained in the *Model 960 Computer Assembly Language Programmer's Reference Manual.*

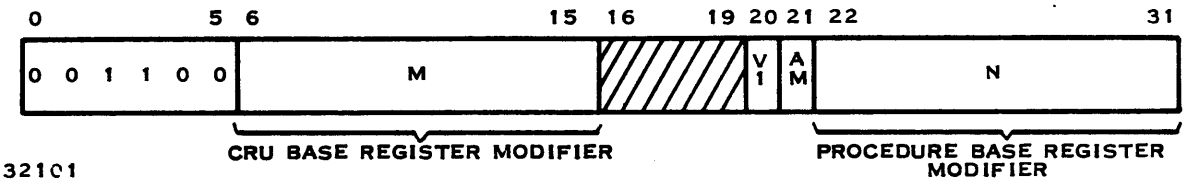
4.2.5 CRU INPUT TRANSFER OF DATA AND INSTRUCTIONS. When the input is enabled, the module decodes the CRU line address and outputs the data (as the serial signal DATAIN) to the CPU. The data is not latched except for the instantaneous value written into memory during an STCR instruction. The four CRU input instructions are described and illustrated in the following paragraphs. Only one of these instructions, the STCR, transfers bits or fields from the Interval Timer module. The other three instructions branch conditionally on the value of a sensed bit.

4.2.5.1 **STCR Instruction.** The format for the Store Communications Register (STCR) instruction is:



The address fields, M and N, contain the CRU base address modifier and the data base register address modifier. Sequential CRU input lines are read and stored as a right-justified bit field in the memory location specified by N plus the contents of the data base register. The CRU input line specified by the contents of the CRU base register plus M is stored as the least significant bit of the field. The B field contains the number of bits to be read and stored in memory. In this field, 0 indicates 16 bits. The bit in the AM field is 0, if execution mode base registers are used and a 1, if alternate mode base registers are used.

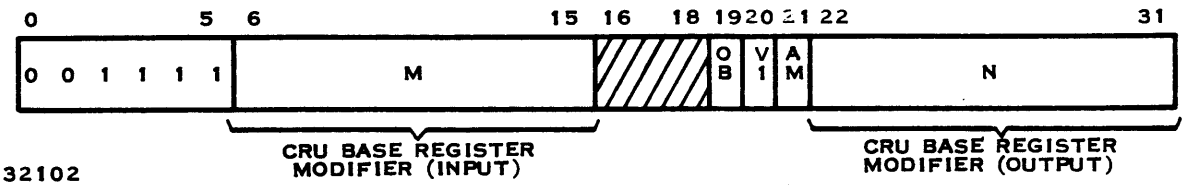
4.2.5.2 **BBNE Instruction.** The format for the Branch on Bit Not Equal (BBNE) instruction is:



The M field is the CRU base register address modifier, and the N field is the procedure base register address modifier. The addressed CRU input line, specified by the modifier in the M field plus the CRU base register, is compared to the bit in the V1 field. If the comparison fails, the Program Counter (PC) or Event Counter (EC) is loaded with the memory address specified by the modifier in the N field plus the contents of the procedure base register.

If the AM bit is 0, the execution mode base registers are used. If the AM bit is 1, the alternate mode CRU base register is used to calculate the CRU address. The branch address is calculated using the active mode procedure base register and the modifier in the N field.

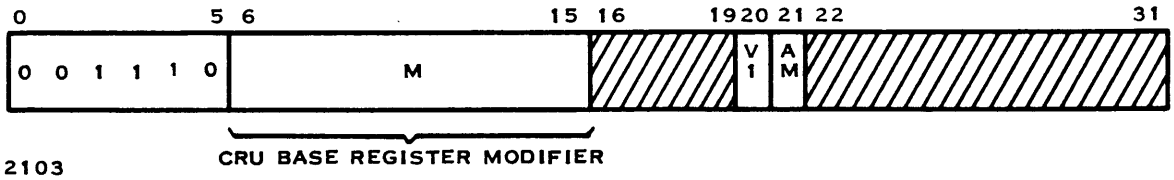
4.2.5.3 **TSBX Instruction.** The format for the Test Input Bit and Switch Mode or Set Output Bit (TSBX) instruction is:



The addressed CRU input line, specified by the address modifier in the M field plus the contents of the CRU base register, is compared to the bit in the V1 field. If the test fails, the mode is changed. If the test is successful, the value of the OB bit is output to the CRU output line specified by the address modifier in the N field plus the contents of the CRU base register.

If the AM bit is 0, the execution mode CRU base register is used. If the AM bit is a 1, the alternate mode CRU base register is used and mode switching is inhibited.

4.2.5.4 **XBNE Instruction.** The format for the Switch Mode On Bit Not Equal (XBNE) instruction is:



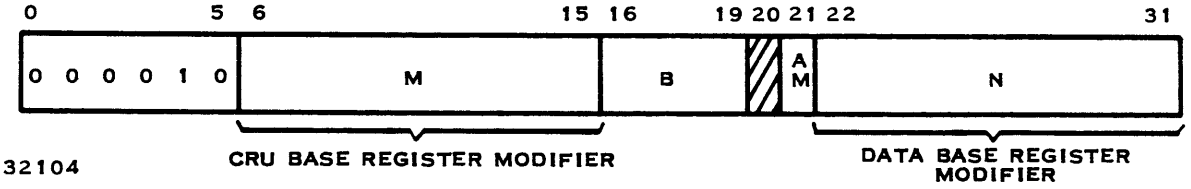
(A)132103

The addresse CRU input line, specified by the address modifier in the M field plus the contents of the CRu base register, is compared to the bit in the V1 field. If the test fails, the mode is changed.

If the AM bit is a 0, the exeuction mode CRU base register is used. If the AM bit is a 1, the alternate mode CRU base register is used.

4.2.6 **CRU OUTPUT TRANSFER OF DATA AND INSTRUCTIONS.** Data is transferred serially between the CPU and the Interval Timer Module on the CPUDATAOUT signal line. The STORECLOCK- control signal indicates that the CPU output data, CPUDATAOUT, is active and stable. The data is latched by the module at the CRU bit location specified by the line address, CRUBIT12-15, on the trailing edge (low-to-high transition) of STORECLOCK-. The formats for the CRU output instructions are described and illustrated in the following paragraphs. These instructions transfer bits or fields to the Interval Timer module.

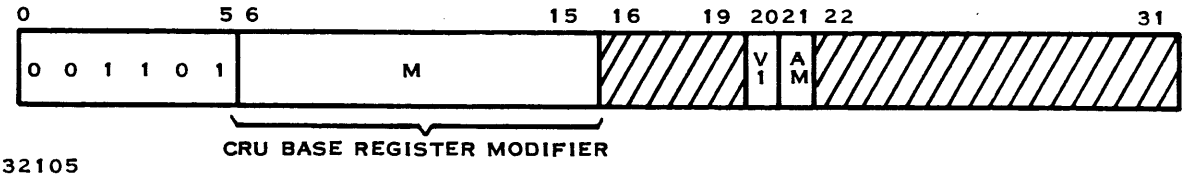
4.2.6.1 **LDCR Instruction.** The format for the Load Communications Register (LDCR) instruction is:



(A)132104

The address fields, M and N, contain the CRU base register address modifier and the data base register address modifier. The B field contains the number of bits to be read from memory and output to the interface. In this field, a 0 indicates 16 bits. The bit in the AM field is a 0 if execution mode base registers are being used, and a 1 if alternate mode base registers are being used. The values in the modifier fields are added to the contents of the corresponding base registers to determine the effective address.

4.2.6.2 **SETB Instruction.** The format for the Set CRU Output Bit (SETB) instruction is:



(A)132105

The M field is the CRU base register modifier or displacement. The bit in the V1 field is used to set the addressed CRU output bit. The V1 bit is a 0 if the addressed bit is false, and a 1 if the addressed bit is true. The bit in the AM field is a 0 if the execution mode base register is used, and a 1 if the alternate mode base register is used. The value in the modifier field is added to the contents of the corresponding base register to determine the effective address.

4.2.6.3 **TSBX Instruction.** The description of this instruction appears in paragraph 4.2.5.3.

4.3 THEORY OF OPERATION

The following discussion references the Interval Timer Module schematic (TI drawing no. 214115) and assumes that the reader has a basic knoweldge of the Communications Register Unit (CRU) presented in the CRU manual provided with each system (TI part no. 966313-9701).

4.3.1 **ADDRESSING.** The CRU line address (CA12-15) is labelled CRUBIT12-15 on the schematic and is a True address. The select signal, CRUSEL0-, is at a low level (True) when the slot in which the module is located is specified by the rack and module fields of the CRU Base Address register (CA04-11). The CRU line address bits CRUBIT12-15 are routed to the input multiplexer Z23 and address decoder Z5 along with the signal CRUSEL0-, which acts as an enable line. As long as CRUSEL0- remains False (high), the module ignores the line address, and the decoder and multiplexer outputs remain high. When CRUSEL0- is True, Z23 selects one of the 16 signals to be CRUDATAIN. Input 0 is the interrupt line and is high when the interrupt flip-flop is set. Inputs 1 through 14 are the contents of the counter. Input 15 is always False (0 when read into memory).

The CRU line address decoder outputs are ADR0- through ADR15-. Only one of these signals is True (low) at any given time. Output ADR0-, used to address the interrupt storage flip-flop, is illustrated in figure 4-3. It is inverted and ANDed with STORECLOCK to provide a single clock edge for the interrupt storage flip-flop. On that edge, D0 (buffered CPUDATAOUT) is gated to the output. Therefore, an instruction can either set or clear (ONE or ZERO) an interrupt. However, if the contents of the counter are zero, then the signal ZEROPRE forces the interrupt storage flip-flop to the high level and prevents a reset of the latch. To reset the interrupt, the counter must be nonzero. ADR1- through ADR14- are used to load the counter flip-flop as illustrated in figure 4-4. CLOCK- is gated with the address lines to sequentially load each flip-flop through the preset and clear inputs from CPUDATAOUT. The D-inputs and clocks are used to form a 14-bit ripple down-counter. The ADR15- signal is inverted and used to clock the COUNT flip-flop (Z34). If D0 is high, COUNT becomes True to enable signals ZEROPRE, TIMECLOCK-, and COUNTPULSE-. (See figure 4-4.)

4.3.2 **INTERRUPTS.** The state of the ZERO flip-flop determines whether or not a CRUINT is True (low). As illustrated in figure 4-2, this is a D-type flip-flop that is preset by ZEROPRE, which is True (low) when the counter contains all zeroes, the COUNT is true, and the 4096 kHz clock is high. Therefore, an interrupt can be cleared only if COUNT is False or the counter is non-zero.

The ZERO- signal is available at the top edge of the module.

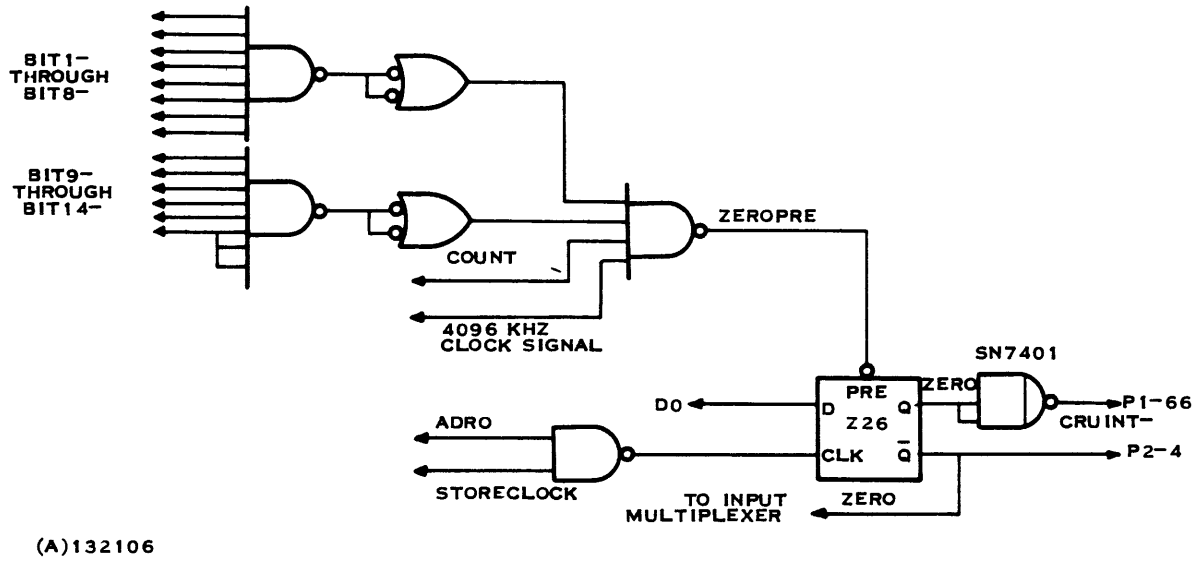


Figure 4-3. Interrupt Storage Flip-Flop Logic

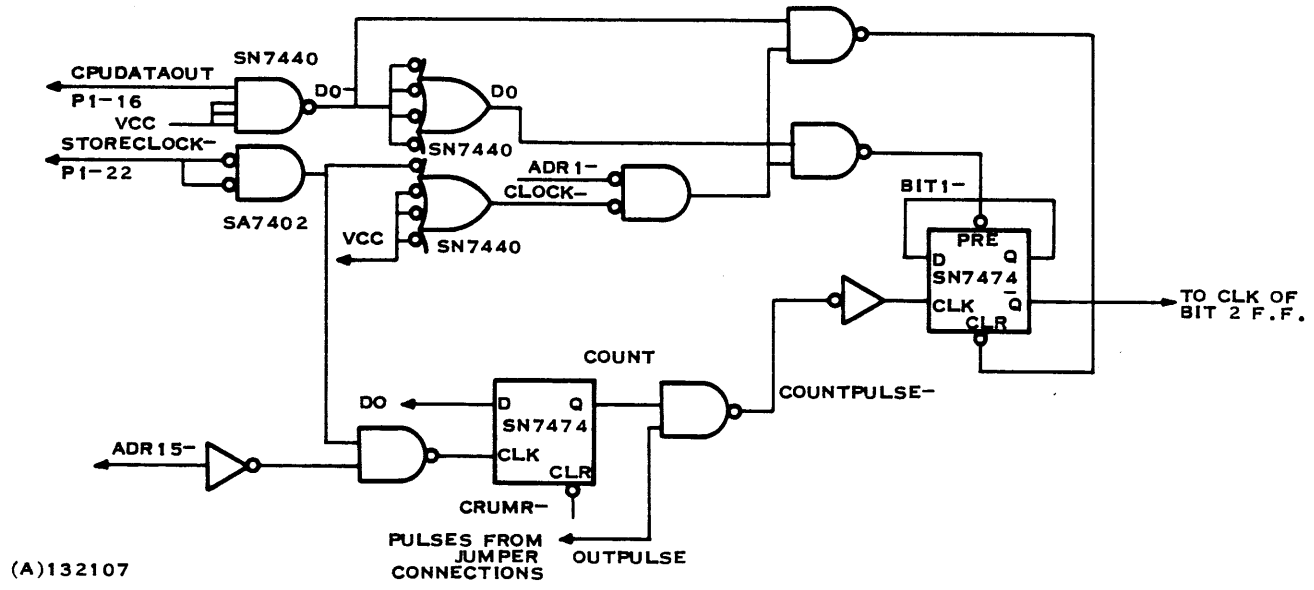


Figure 4-4. Interval Timer Register Loading Logic

4.3.3 **TIME INTERVAL GENERATION.** The basic clock is a 4096 kHz square wave that is produced by sections of Z35 and Z27 in a crystal-stablized multi-vibrator. The clock signal is enabled by COUNT in a section of Z35, inverted to become TIMCLOCK, and divided by 4 in Z33. This signal is further divided by Z30, Z32, and Z34 so that the last four signals that are generated have periods of 1, 2, 4, and 8 ms. One of these clocks is normally routed by a jumper to E5, the input to inverter Z25 which in turn is the clock of flip-flop Z26. The output of Z26 is OUTPULSE. This signal is forced to be a short pulse (16 microseconds) by using an output of Z31 to clear the OUTPULSE every 16 microseconds.

SECTION V

MAINTENANCE

5.1 GENERAL

This section references software tests that check the operation of the Interval Timer Module interface. The tests provide an outline for fault isolation during troubleshooting. Preventive maintenance is not required other than ensuring that cooling air is not impeded by excessive dust and dirt.

5.2 PERFORMANCE DEMONSTRATION TESTS

The Performance Demonstration Test (PDT) certifies proper installation and equipment integrity; as well as providing a systematic approach to fault isolation. The PDT for the Interval Timer Module is described in Section VIII of this manual including the listing, and an operating procedure.

5.3 FAULT ISOLATION

The following paragraphs give the module level and component level fault isolation procedures.

5.3.1 FAULT ISOLATION, MODULE LEVEL. It is generally necessary to locate computer system faults to the module level. A defective module can be located using methodical troubleshooting techniques and replacing a known good module for a suspected bad one. The repaired system is then tested to verify satisfactory operation and the defective module is returned to the manufacturer for repair.

The Central Processor Unit (CPU) and the Communications Register Unit (CRU) must function properly before the Interval Timer Module can be tested. Perform the Arithmetic Unit (AU) Performance Assurance Tests (PAT's). Correct performance of the PAT's confirms the integrity of the CPU and capability to input and output information through the Communications Register Unit (CRU) interface.

Perform the Interval Timer Module PDT to confirm satisfactory operation in the selected CRU port. If the PDT fails to complete properly, the probable causes are defective Interval Timer Module or Communications Register Unit modules. When substituting known good modules, mark the various modules so that the ones used as standards and the suspected defective modules do not get mixed. When testing the Interval Timer Module all other interrupt generating CRU devices must be disabled to prevent unexpected interrupts.

5.3.2 FAULT ISOLATION, COMPONENT LEVEL. Isolation of a failure to the defective component requires the electrical drawings (supplied in Section VI), the test equipment listed in table 5-1, and the PDT listing (supplied in Section VIII). The approach described for the module level fault isolation is used to determine a defective module. The procedure that follows permits the defective component on a module to be identified.

The following procedure can be used to isolate defective components using the Interval Timer Module PDT as a troubleshooting tool.

Table 5-1. Required Test Equipment

Test Equipment	Manufacturer and Type
Multimeter	VOM
Oscilloscope	Tektronix Model 453 or equivalent
Module extender board	TI part no. 226851-0001

Place the defective module in an extender board and the combination in slot EF3. Remove all other modules that might generate interrupts from the CRU.

NOTE

Follow the considerations mentioned in the installation instructions concerning module installation and removal.

Execute the PDT. The PDT is structured as five independent tests to fabricate program looping on an error. When an error occurs, the program will halt (the program counter will not be changing). If an error has occurred, the program will be executing a branch to the present program counter address. Inspection of the instruction register B (IB) will indicate the relative program address of the Halt instruction. This Halt instruction should be located in the listing. This instruction may be altered to cause a branch to the first instruction of the failing section. Program execution can be restarted and the program will continue to loop the failing routine to permit the use of an oscilloscope. This presumes the failure is not intermittent. The description of the failed test in the listing will indicate the area in the logic needing investigation.

Use the logic diagram to locate suspected defective signals. The labels on a logic gate symbol designate the position of a network or connector pin. The components and networks can then be located using the assembly drawing, The labelling of the top-edge connector is described in the theory of operation section.

SECTION VI

DRAWINGS

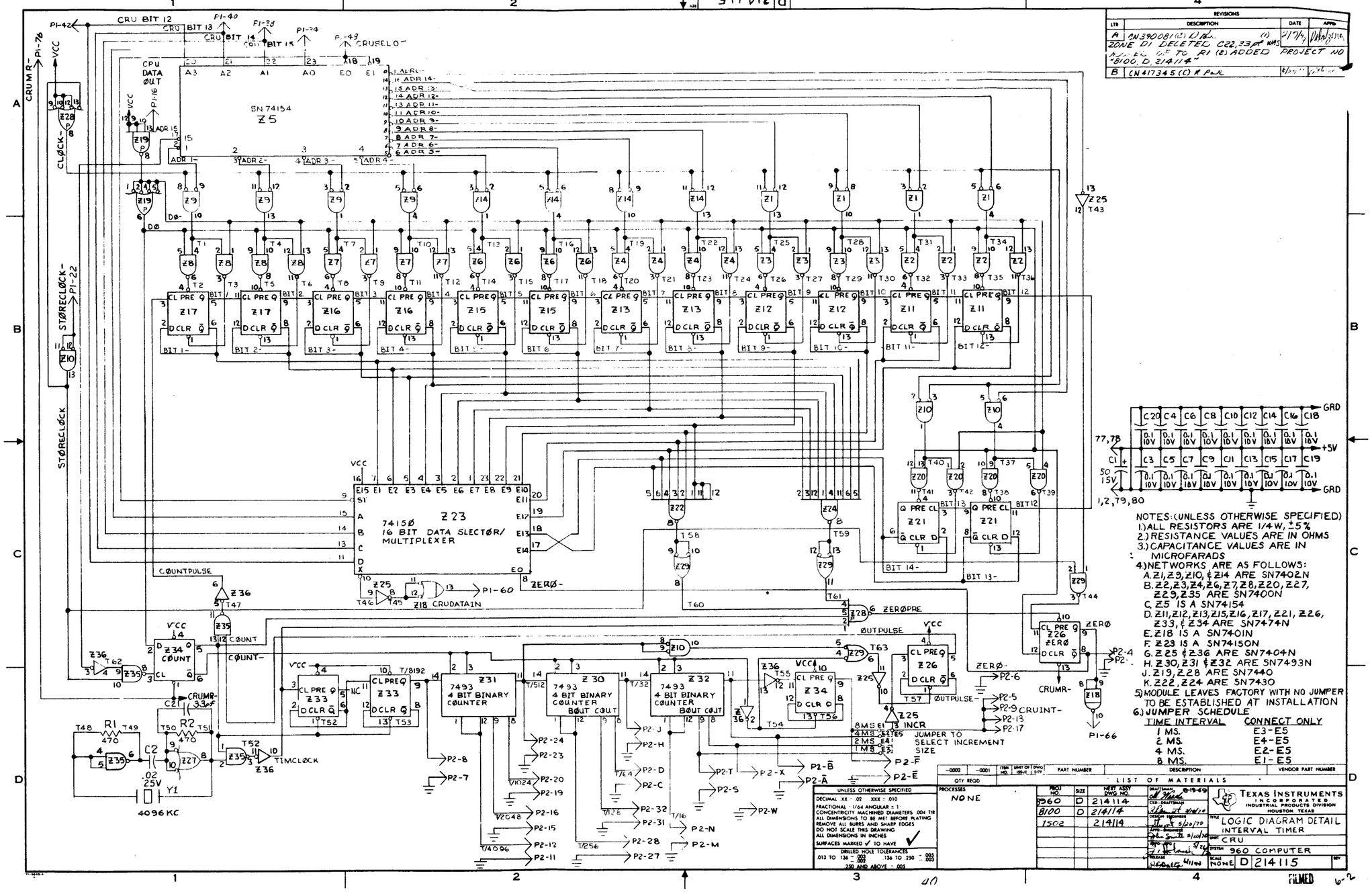
6.1 GENERAL

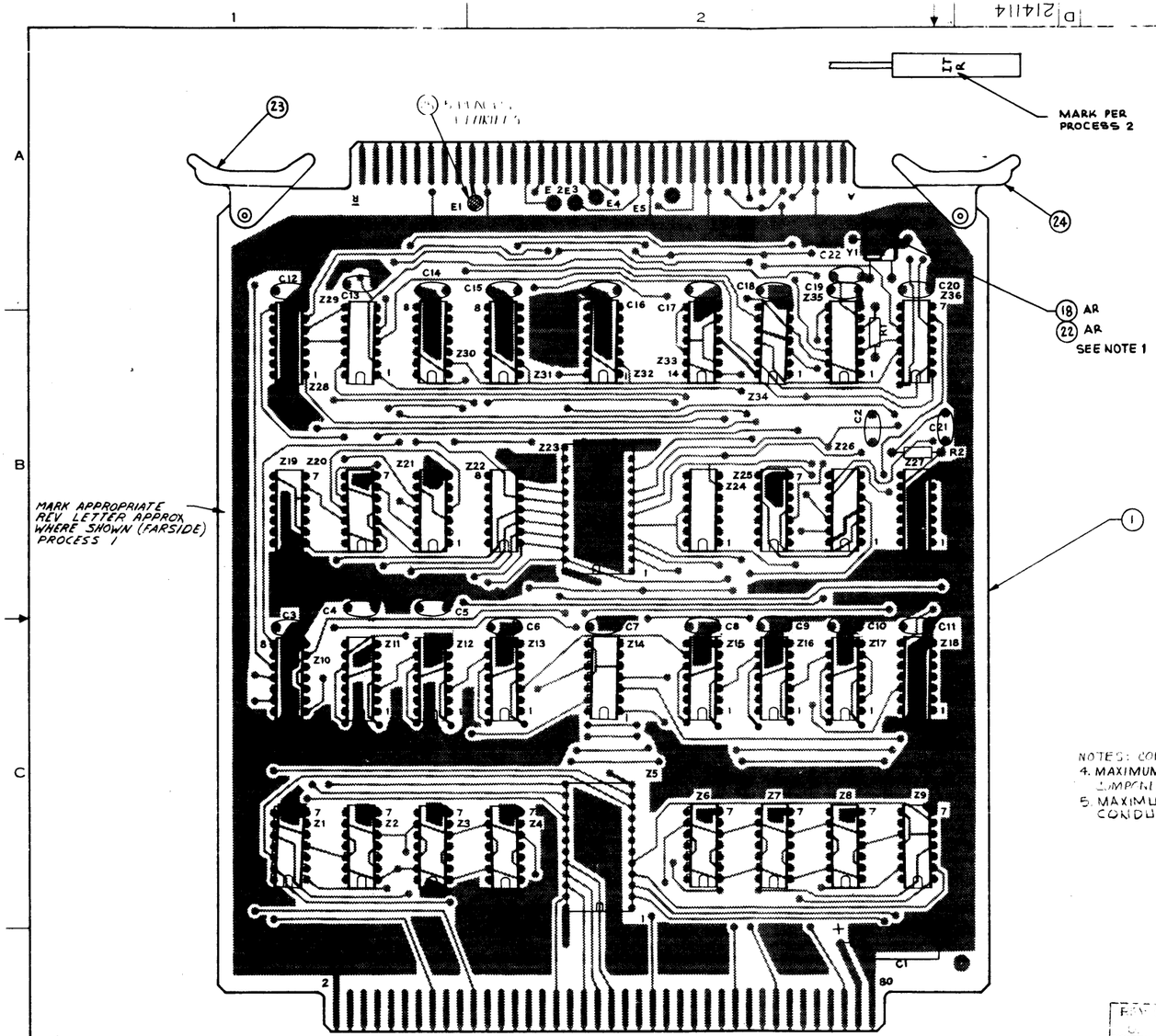
The electrical drawings, assembly drawings, and parts lists that are required to properly service and maintain the Interval Timer Module are included in this section.

Parts lists, assembly drawings, and electrical drawings for the computers are contained in the following manuals:

Title	TI Manual Number
Model 960A Maintenance Manual Parts List and Assembly Drawings	226750-9707
Model 960A Maintenance Manual Electrical Drawings	226750-9708
Model 960B Maintenance Manual Parts List and Assembly Drawings	942773-9704
Model 960B Maintenance Manual Electrical Drawings	942773-9705

An index of drawings and parts lists appears below. This index lists the electrical drawing, assembly drawing, and parts list (LM).


D214115
REVISIONS
LTR | DESCRIPTION | DATE | APPD
A | CN39008(2) (1) ZONE D1 DELETED, C22,33pF WAS (1) R1 & R2 CHG TO R1 (2) ADDED PROJECT NO "8100, D 214114"
B | CN41734 5(1) R PWR
SN74154 Z5
74150 Z23 16 BIT DATA SLECTOR/ MULTIPLEXER
7493 4 BIT BINARY COUNTER
CRUBIT 12
CRU BIT 13
CRU BIT 14
CRU BIT 15
CRUSELO-
CRUMR-
CLOCK-
STORECLOCK-
REGCLOCK
VCC
GRD
+5V
ADR 1- ADR 2- ADR 3- ADR 4- ADR 5-
ADR 10- ADR 11- ADR 12- ADR 13- ADR 14- ADR 15-
ZERO-
ZEROPRE
CRUDATAIN
COUNTPULSE
COUNT
COUNT-
OUTPULSE
OUTPULSE-
TIMCLOCK
4096 KC
R1 470
R2 470
C2 .02 25V
CRUINT-
JUMPER TO SELECT INCREMENT SIZE
8MS E1
4MS E2
2MS E4
1MS E3
INCR
NOTES: (UNLESS OTHERWISE SPECIFIED)
1.) ALL RESISTORS ARE 1/4W, ±5%
2.) RESISTANCE VALUES ARE IN OHMS
3.) CAPACITANCE VALUES ARE IN MICROFARADS
4.) NETWORKS ARE AS FOLLOWS:
A. Z1, Z9, Z10 & Z14 ARE SN7402N
B. Z2, Z3, Z4, Z6, Z7, Z8, Z20, Z27, Z29, Z35 ARE SN7400N
C. Z5 IS A SN74154
D. Z11, Z12, Z13, Z15, Z16, Z17, Z21, Z26, Z33, & Z34 ARE SN7474N
E. Z18 IS A SN7401N
F. Z23 IS A SN74150N
G. Z25 & Z36 ARE SN7404N
H. Z30, Z31 & Z32 ARE SN7493N
J. Z19, Z28 ARE SN7440
K. Z22, Z24 ARE SN7430
5.) MODULE LEAVES FACTORY WITH NO JUMPER TO BE ESTABLISHED AT INSTALLATION
6.) JUMPER SCHEDULE
TIME INTERVAL | CONNECT ONLY
1 MS. | E3-E5
2 MS. | E4-E5
4 MS. | E2-E5
8 MS. | E1-E5
LIST OF MATERIALS
PROCESSES: NONE
TEXAS INSTRUMENTS INCORPORATED INDUSTRIAL PRODUCTS DIVISION HOUSTON, TEXAS
LOGIC DIAGRAM DETAIL INTERVAL TIMER
CRU
960 COMPUTER
SIZE D 214115 REV



NOTES: CONTINUED
4. MAXIMUM COMPONENT HEIGHT FROM COMPONENT SIDE OF CARD IS .31
5. MAXIMUM LEAD LENGTH FROM CONDUCTOR SIDE OF CARD IS .075

NOTES:
1. PUT PLASTIC SLEEVING (ITEM 22) OVER CRYSTAL AND ATTACH TO PWB USING HOT MELT OR EQUIVALENT PROCESS.
~~2. MODIFY LEAVES FACTORY WIRED AS 214114-0001~~
3. JUMPER SCHEDULE (JUMPERS TO BE INSTALLED PRIOR TO UNIT TEST LEAVING ONE END LOOSE. LOOSE END WILL BE SOLDERED AFTER UNIT TEST)

214114-0001	CONNECT ONLY E3 TO E5	1MS
214114-0002	CONNECT ONLY E4 TO E5	2MS
214114-0004	CONNECT ONLY E2 TO E5	4MS
214114-0008	CONNECT ONLY E1 TO E5	8MS

DESCRIPTION	PART NO.
CARD ASSY INTERVAL TIMER MODULE - DOCUMENTATION	214114 -0960
-8MS	214114 -0008
-4MS	214114 -0004
-2MS	214114 -0002
CARD ASSY, INTERVAL TIMER MODULE - E3 TO E5	214114 -0001

REVISIONS

LTR	DESCRIPTION	DATE	APPD
A	367126 (C) 8-11-70	9/15/72	
	CHG, L/M, ITEM 20 WAS 217166-9901, TEST PROCEEDURE		
B	372107(E) 3-2-72		
	ADD: IT 22; DELETED IT 21 FROM BD ; DELETED NOTE 2 FROM DWG. NOTE 1 WAS TIE CRYSTAL TO BD WITH LACING CORD IT. 18 ADDED REV LEVEL BLOCK		
C	366850 (C) J. Pinney 3-21-72	3-28-72	
	CHG: ITEM 21 WAS P/N 236525-0005. ADDED: 1) -0002, -0004, -0008) 2) TO JUMPER SCHED(NOTE 3) -0001, -0002, -0004 & -0008. CHG: REV LEVEL BLOCK- SCHEM NO. WAS 217118		
D	373599 (E) 9/26/72	10-11 72	
	1) ADDED ITEMS 23 & 24 2) ADDED PROCESS 2 3) ADDED TO NEXT ASSY B100 |A| 226700		
E	380982 (D)	3-3-73	
	1) ADDED 1M-0960 & PART NO SCHEDULE 2) ADDED TO NOTE 3 "JUMPER TO BE ---"		
F	380923 (C) 6/8/73	6/8/73	
	1) P/N IN P/N SCHEDULE WAS 214960		
G	390075 (C) D Peter	9/11/74	
	(1) IN L/M-1,-2,-4,-8 ITEM 5 QTY WAS 2, ITEM 5A DELETED C22 (2) 2 C4 ADDED NOTES 4 & 5 (3) 2 A 2 DELETED C22 OUTLINE REF DES ABOVE C19 (4) REVISED REV LEVEL BLOCK		
H	388339(E) (1) Rev-11 in -960; ITEM 2 WAS 96-1798-0001 (P/O 17MOKA, CRU ... (2) ADDED ITEM 5A & (3) UPDATE REV LEV BLK	1-11-75	
J	CN 403045 (B) R Da Lan (1) ITEM 5 QTY WAS 1; (2) ADDED C22 TO ITEM 5A, (3) ITEM 3 QTY WAS 18; (4) ITEM 3A WAS C3-C20 (5) ITEM 6 QTY WAS 1; (6) ADDED C19 TO ITEM 6A, (7) ADDED C22 TO F/O A2	3-19-75	
K	CN 392202 (C) SD Dickson (1) NOTE 3 WAS JUMPER, ... (JUMPERS ... INSTALLED AFTER ... (2) UPDATED REV LVL BLK	5-6-75	
L	CN 393089 (C) R Da Lan (1) NOTE 3 WAS (... PRIOR TO SYSTEM TEST & (2) ADDED PROCESS 3; (3) UPDATED REV LEVEL BLOCK	7-10-75	
M	CN 387789 (D) R Da Lan (1) UPDATED REV LEVEL BLOCK	11-5-75	
N	CN 415245 (C) K Da Lan (1) A/M-960 DELETED ITEM 24 (2) UPDATED REV LEVEL BLOCK	1-30-76	
P	CN 412264 (C) R Da Lan (1) ADDED MFY TO P/N FOR ITEM 3 QTY -0008 & -0008 & QTY 10 FOR ITEM 3 QTY -0008 (2) UPDATED REV LEVEL BLOCK	2-19-76	
R	CN 417150 (E) (1) UPDATED REV LEV BLK & ADDED TEST PROC	11-4-76	

(REVISIONS CONT'D SH. 2)

| REV LEVEL | | |

DWG NO 2M114 SH 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	T	(1) ADD 417-44 (2) CHANGE TO HI (1) ADDED SH 2 (2) UPDATED REV LEVEL BLOCK (3) NOTE 1 WAS --- AND TIE CRYSTAL TO BOARD WITH LACING CORD ITEM 18.		
	U	CHANGE ITEM 18 (1) TO MFR (1) M, -0001, 0002, 0004, 0008 ADDED ITEM 25 & ITEM CALLOUT ON SHT 1 (2) UPDATED REV LEVEL BLOCK	12-5-	

TEXAS INSTRUMENTS	DWN L.TeHa DATE 6 9 11	SIZE D	FSCM NO 96214	DRAWING NO 2M114	REV U
	ISSUE DATE 6 10 11	SCALE NONE		SHEET 2	

TEXAS INSTRUMENTS
INCORPORATED

DATE 09/23/77

LIST OF MATERIAL

PAGE 1 of

PART NUMBER LM0214114-0001 REV U

ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0214113-0001	PRINTED WIRING BD, INTERVAL TIMER	
0002	00002.000	EA		0972946-0057	RES FIX 470 OHM 5 % .25 W CARBON FILM	RCH - 3-25
0002A					R1,R2	
0003	00017.000	EA		0534368-0001	CAP FIX CERAMIC .10 MF 20/80 % 10V	CRL - JCED-104
0003A					C3 THRU C18,C20	
0004	00001.000	EA		0230841-0001	CAP 50.00 MF 16V	SPR -TE-1160
0004A					C1	
0005	00002.000	EA		0972926-0015	CAP FIX MICA 500V 33.0 PF 5 %	DPL -CM06E330J0D
0005A					C21,C22	
0006	00002.000	EA		0532736-0002	CAP FIX CERAMIC .02 MF 20/80% 25 VOLT	CRL - 2DDJ80F203Z4C
0006A					C2,C19	
0007	00004.000	EA		0222222-7402	NETWORK SN7402N	TI- -SN7402N
0007A					Z1,Z9,Z10,Z14	
0008	00010.000	EA		0222222-7400	NETWORK SN7400N	-SN7400N
0008A					Z2 Z3 Z4 Z6 Z7 Z8 Z20 Z27	
0008B					Z29 Z35	
0009	00001.000	EA		0222222-7154	NETWORK SN74154N	-SN74154N
0009A					Z5	
0010	00010.000	EA		0222222-7474	NETWORK SN7474N	-SN7474N
0010A					Z11,Z12,Z13,Z15,Z16,Z17,Z21	

DRAFTSMAN / DATE	CKD. DRAFTSMAN / DATE	DESIGN ENGINEER / DATE	TITLE
	L. Lobig 9-29-77		CARD ASSY-INTERVAL TIMER MODULE, E3 TO E5
APPD. MFG / DATE	APPD. PROJECT ENGINEER / DATE	RELEASED / DATE	PROJECT NO. 8960

PART NUMBER LM0214114-0001 REV U

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PART NUMBER LM0214114-3001 REV U

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0010B					Z26,Z33,Z34	
0011	00001.000	EA		0222222-7401	NETWORK SN7401N	
0011A					Z18	
0012	00001.000	EA		0222222-7150	NETWORK SN74150N	
0012A					Z23	
0013	00002.000	EA		0222222-7404	NETWORK SN7404N	
0013A					Z25,Z36	
0014	00003.000	EA		0222222-7493	NETWORK-SN7493N	
0014A					Z30,Z31,Z32	
0015	00002.000	EA		0222222-7440	NETWORK SN7440N	-SN7440N
0015A					Z19,Z28	
0016	00002.000	EA		0222222-7430	NETWORK SN7430N	-SN7430N
0016A					Z22,Z24	
0017	00001.000	EA		0231642-3025	CRYSTAL 4096.KC + OR - 0.005% W/WIRE LDS MIL	-CR56/J-HC18/U
0017A					Y1	
0018	AR	RL		0231579-0000	CORD LACE .090X.0125-500Y	-#18 BLK.
0019	REF	EA		0214115-9901	LOGIC DIAGRAM DETAILED,INTERVAL TIMER	
0020	REF	EA		0217118-9901	TEST PROCEDURE-INTERVAL TIMER	
0021	AR	FT		0538347-3999	WIRE HOOKUP 8-22 AWG 19 STR WHITE	JUD - 440115
0022	AR	FT		0236277-0000	TUBING 3/8 CLEAR PLASTIC	

DRAFTSMAN / DATE	CKD DRAFTSMAN / DATE	DESIGN ENGINEER / DATE	TITLE
			CARD ASSY-INTERVAL TIMER MODULE,E3 TO E5
APPD MFG. / DATE	APPD PROJECT ENGINEER / DATE	RELEASED / DATE	PROJECT NO / PART NUMBER / REV
			LM0214114-3001 U

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PART NUMBER	REV
LM0214114-0001	U

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0023	00001.000	EA		0533887-0001	EJECTOR,PCB,NON-LOCKING,WHITE	SCA -S-232 WHITE
0024	00001.000	EA		0533887-0009	EJECTOR,PCB,NON-LOCKING,GREEN	SCA -S-232 GREEN
0025	00005.000	EA		0083694-0003	TERMINAL TURRET TYPE	USE - 20108
0025A					E1 E2 E3 E4 E5	

DRAFTSMAN	DATE	CKD DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						CARD ASSY-INTERVAL TIMER MODULE,E3 TO E5
APPD.-MFG	DATE	APPD PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						PART NUMBER: LM0214114-0001 REV: U

T.I. 13849

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INCORPORATED

DATE 09/23/77

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PART NUMBER LM0214114-0002 REV U

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0214113-0001	PRINTED WIRING BD,INTERVAL TIMER	
0002	00002.000	EA		0972946-0057	RES FIX 470 OHM 5 % .25 W CARBON FILM	ROH - R-25
0002A					R1 R2	
0003	00017.000	EA		0534348-0001	CAP FIX CERAMIC .10 MF 20/80 % 10V	CRL - JCED-104
0003A					C3 THRU C18,C20	
0004	00001.000	EA		0230841-0001	CAP 50.00 MF 16V	SPR -TE-1160
0004A					C1	
0005	00002.000	EA		0972926-0015	CAP FIX MICA 500V 33.0 PF 5 %	QPL -CM06F330J00
0005A					C21,C22	
0006	00002.000	EA		0532736-0002	CAP FIX CERAMIC .02 MF 20/80% 25 VOLT	CRL - 2DDJ50E203ZAC
0006A					C2,C19	
0007	00004.000	EA		0222222-7402	NETWORK SN7402N	TI- -SN7402N
0007A					Z1 Z9 Z10 Z14	
0008	00010.000	EA		0222222-7400	NETWORK SN7400N	-SN7400N
0008A					Z2 Z3 Z4 Z6 Z7 Z8 Z20 Z27	
0008B					Z29 Z35	
0009	00001.000	EA		0222222-7154	NETWORK SN74154N	-SN74154N
0009A					Z5	
0010	00010.000	EA		0222222-7474	NETWORK SN7474N	-SN7474N
0010A					Z11 Z12 Z13 Z15 Z16 Z17 Z21	

DRAFTSMAN	DATE	CKD DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						CARD ASSY,INTERVAL TIMER MODULE-24S
APPD MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.

PART NUMBER LM0214114-0002 REV U

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PART NUMBER LM0214114-0002 REV U

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0010B					Z26 Z33 Z34	
0011	00001.000	EA		0222222-7401	NETWORK SN7401N	
0011A					Z18	
0012	00001.000	EA		0222222-7L50	NETWORK SN74150N	
0012A					Z23	
0013	00002.000	EA		0222222-7404	NETWORK SN7404N	
0013A					Z25,Z36	
0014	00003.000	EA		0222222-7493	NETWORK-SN7493N	
0014A					Z30 Z31 Z32	
0015	00002.000	EA		0222222-7440	NETWORK SN7440N	-SN7440N
0015A					Z19 Z28	
0016	00002.000	EA		0222222-7430	NETWORK SN7430N	-SN7430N
0016A					Z22 Z24	
0017	00001.000	EA		0231642-3025	CRYSTAL 4096.KC + OR - 0.005% W/WIRE LDS MIL	-CR56/J-HC18/U
0017A					Y1	
0018	AR	RL		0231579-0000	CORD LACE .090X.0125-500Y	-#19 BLK.
0019	REF	EA		0214115-9901	LOGIC DIAGRAM DETAILED, INTERVAL TIMER	
0020	REF	EA		0217118-9901	TEST PROCEDURE-INTERVAL TIMER	
0021	AR	FT		0538347-3999	WIRE HOOKUP 8-22 AWG 19 STR WHITE	JUD - 441115
0022	AR	FT		0236277-0000	TUBING 3/8 CLEAR PLASTIC	

DRAFTSMAN / DATE	CKD. DRAFTSMAN / DATE	DESIGN ENGINEER / DATE	TITLE
			CARD ASSY, INTERVAL TIMER MODULE-2MS

APPD. MFG. / DATE	APPD. PROJECT ENGINEER / DATE	RELEASED / DATE	PROJECT NO.		PART NUMBER	REV
					LM0214114-0002	U

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PART NUMBER LM0214114-0002 REV U

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0023	00001.000	EA		0533887-0001	EJECTOR,PCB,NON-LOCKING,WHITE	SCA -S-232 WHITE
0024	00001.000	EA		0533887-0009	EJECTOR,PCB,NON-LOCKING,GREEN	SCA -S-232 GREEN
0025	00005.000	EA		0093694-0003	TERMINAL TURRET TYPE	USE - 20109
0025A					E1 E2 E3 E4 E5	

DRAFTSMAN	DATE	CRD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						CARD ASSY,INTERVAL TIMER MODULE-24S
APPD. MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.

PART NUMBER LM0214114-0002 REV U

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PART NUMBER LM0214114-0004 REV U

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0214113-0001	PRINTED WIRING BD, INTERVAL TIMER	
0002	00002.000	EA		0972946-0057	RES FIX 470 OHM 5 % .25 W CARBON FILM	ROH - R-25
0002A					R1 R2	
0003	00017.000	EA		0534348-0001	CAP FIX CERAMIC .10 MF 20/80 % 10V	CRL - JCED-104
0003A					C3 THRU C18,C20	
0004	00001.000	EA		0230841-0001	CAP 50.00 MF 16V	SPR -TE-1150
0004A					C1	
0005	00002.000	EA		0972926-0015	CAP FIX MICA 500V 33.0 PF 5 %	DPL -CM06E330J00
0005A					C21 C22	
0006	00002.000	EA		0532736-0002	CAP FIX CERAMIC .02 MF 20/80% 25 VOLT	CRL - ?JJJ50F203ZAC
0006A					C2 C19	
0007	00004.000	EA		0222222-7402	NETWORK SN7402N	TI- -SN7402N
0007A					Z1 Z9 Z10 Z14	
0008	00010.000	EA		0222222-7400	NETWORK SN7400N	-SN7400N
0008A					Z2 Z3 Z4 Z6 Z7 Z8 Z20 Z27	
0008B					Z29 Z35	
0009	00001.000	EA		0222222-7154	NETWORK SN74154N	-SN74154N
0009A					Z5	
0010	00010.000	EA		0222222-7474	NETWORK SN7474N	-SN7474N
0010A					Z11 Z12 Z13 Z15 Z16 Z17 Z21	

DRAFTSMAN / DATE	CKD. DRAFTSMAN / DATE	DESIGN ENGINEER / DATE	TITLE
			CARD ASSY, INTERVAL TIMER MODULE-44S
APPD. MFG / DATE	APPD. PROJECT ENGINEER / DATE	RELEASED / DATE	PROJECT NO. / PART NUMBER / REV
			LM0214114-0004 U

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PART NUMBER LM0214116-0004 REV U

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0010R					Z26 Z33 Z34	
0011	00001.000	EA		0222222-7401	NETWORK SN7401N	
0011A					Z18	
0012	00001.000	EA		0222222-7150	NETWORK SN74150N	
0012A					Z23	
0013	00002.000	EA		0222222-7404	NETWORK SN7404N	
0013A					Z25 Z36	
0014	00003.000	EA		0222222-7493	NETWORK-SN7493N	
0014A					Z30 Z31 Z32	
0015	00002.000	EA		0222222-7440	NETWORK SN7440N	-SN7440N
0015A					Z19 Z28	
0016	00002.000	EA		0222222-7430	NETWORK SN7430N	-SN7430N
0016A					Z27 Z24	
0017	00001.000	EA		0231642-3025	CRYSTAL 4096.KC + OR - 0.005% W/WIRE LDS	MIL -CR55/U-HC18/U
0017A					Y1	
0018	AR	RL		0231579-0000	CORD LACE .090X.0125-500Y	-#18 BLK.
0019	REF	EA		0214115-9901	LOGIC DIAGRAM DETAILED, INTERVAL TIMER	
0020	REF	EA		0217118-9901	TEST PROCEDURE-INTERVAL TIMER	
0021	AR	FT		0538347-3999	WIRE HOOKUP 8-22 AWG 19 STR WHITE	JUD -.443115
0022	AR	FT		0236277-0000	TUBING 3/8 CLEAR PLASTIC	

DRAFTSMAN / DATE	CKD DRAFTSMAN / DATE	DESIGN ENGINEER / DATE	TITLE
			CARD ASSY, INTERVAL TIMER MODULE-445
APPD MFG / DATE	APPD PROJECT ENGINEER / DATE	RELEASED / DATE	PROJECT NO. / PART NUMBER / REV
			LM0214116-0004 U

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PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0023	00001.000	EA		0533887-0001	EJECTOR,PCB,NON-LOCKING,WHITE	SCA -S-232 WHITE
0024	00001.000	EA		0533887-0009	EJECTOR,PCB,NON-LOCKING,GREEN	SCA -S-232 GREEN
0025	00005.000	EA		0083694-0003	TERMINAL TURRET TYPE	USE - 20109
0025A					E1 E2 E3 E4 E5	

DRAFTSMAN	DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						CARD ASSY,INTERVAL TIMER MODULE-64S
APPD MFG	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.

PART NUMBER	REV
LM0214114-0004	U

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PART NUMBER LM0214114-0008 REV U

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0214113-0001	PRINTED WIRING BD, INTERVAL TIMER	
0002	00002.000	EA		0972946-0057	RES FIX 470 OHM 5 % .25 W CARBON FILM	ROH - R-25
0002A					R1 R2	
0003	00017.000	EA		0534348-0001	CAP FIX CERAMIC .10 MF 20/80 % 10V	CRL - JKIO-104
0003A					C3 THRU C18,C20	
0004	00001.000	EA		0230841-0001	CAP 50.00 MF 16V	SPR -TF-1160
0004A					C1	
0005	00002.000	EA		0972926-0015	CAP FIX MICA 500V 33.0 PF 5 %	DPL -CM06E330J00
0005A					C21,C22	
0006	00002.000	EA		0532736-0002	CAP FIX CERAMIC .02 MF 20/80% 25 VOLT	CRL - 2JJ160E203ZAC
0006A					C2,C19	
0007	00004.000	EA		0222222-7402	NETWORK SN7402N	TI- -SN7402N
0007A					Z1 Z9 Z10 Z14	
0008	00010.000	EA		0222222-7400	NETWORK SN7400N	-SN7400N
0008A					Z2 Z3 Z4 Z6 Z7 Z8 Z20 Z27	
0008B					Z29 Z35	
0009	00001.000	EA		0222222-7154	NETWORK SN74154N	-SN74154N
0009A					Z5	
0010	00010.000	EA		0222222-7474	NETWORK SN7474N	-SN7474N
0010A					Z11 Z12 Z13 Z15 Z16 Z17 Z21	

DRAFTSMAN DATE	CKD DRAFTSMAN DATE	DESIGN ENGINEER DATE	TITLE
			CARD ASSY, INTERVAL TIMER MODULE-8MS

APPD MFG DATE	APPD PROJECT ENGINEER DATE	RELEASED DATE	PROJECT NO.		PART NUMBER LM0214114-0008	REV U

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PART NUMBER LM0214114-0008 REV U

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0010B					Z26 Z33 Z34	
0011	00001.000	EA		0222222-7401	NETWORK SN7401N	
0011A					Z18	
0012	00001.000	EA		0222222-7150	NETWORK SN74150N	
0012A					Z23	
0013	00002.000	EA		0222222-7404	NETWORK SN7404N	
0013A					Z25 Z36	
0014	00003.000	EA		0222222-7493	NETWORK-SN7493N	
0014A					Z30 Z31 Z32	
0015	00002.000	EA		0222222-7440	NETWORK SN7440N	-SN7440N
0015A					Z19 Z28	
0016	00002.000	EA		0222222-7430	NETWORK SN7430N	-SN7430N
0016A					Z22 Z24	
0017	00001.000	EA		0231642-3025	CRYSTAL 4096.KC + OR - 0.005% W/WIRE LDS MIL	-CR64/J-HC18/U
0017A					Y1	
0018	AR	RL		0231579-0000	CORD LACE .090X.0125-500Y	-#18 BLK.
0019	REF	EA		0214115-9901	LOGIC DIAGRAM DETAILED, INTERVAL TIMER	
0020	REF	EA		0217118-9901	TEST PROCEDURE-INTERVAL TIMER	
0021	AR	FT		0538347-3999	WIRE HOOKUP B-22 AWG 19 STR WHITE	JUD - HH2115
0022	AR	FT		0236277-0000	TUBING 3/8 CLEAR PLASTIC	

DRAFTSMAN / DATE	CKD DRAFTSMAN / DATE	DESIGN ENGINEER / DATE	TITLE
			CARD ASSY, INTERVAL TIMER MODULE-BUS
APPD MFG / DATE	APPD PROJECT ENGINEER / DATE	RELEASED / DATE	PROJECT NO / PART NUMBER / REV
			LM0214114-0008 U

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PART NUMBER LM0214114-0008 REV U

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0023	00001.000	EA		0533887-0001	EJECTOR,PCB,NON-LOCKING,WHITE	SCA -S-202 WHITE
0024	00001.000	EA		0533887-0009	EJECTOR,PCB,NON-LOCKING,GREEN	SCA -S-202 GREEN
0025	00005.000	EA		0083694-0003	TERMINAL TURRET TYPE	USF - 20108
0025A					E1 E2 E3 E4 E5	

DRAFTSMAN	DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						CARD ASSY, INTERVAL TIMER MODULE-845
APPD. MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.

PART NUMBER LM0214114-0008 REV U

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PART NUMBER LM0214114-0960 REV U

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0966374-9701	MANUAL,CRU INTERVAL TIMER MODULE 960A	
0003	00001.000	EA		0942715-9901	PD,ITM960,INTERVAL TIMER-PDT960	
0004	00001.000	EA		0942715-9902	AL,,ITM960,INTERVAL TIMER-PDT960	

DRAFTSMAN	DATE	CKD DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						CARD ASSY,INTERVAL TIMER MODULE-DOC
APPD.-MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.

PART NUMBER LM0214114-0960 REV U

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SECTION VII

LOGIC IMPLEMENTATION LIST

This section is not applicable to this manual.

SECTION VIII

PERFORMANCE DEMONSTRATION TEST

8.1 GENERAL

The Performance Demonstration Test (PDT) tests the Interval Timer Module to determine if all functions are working properly. Table 8-1 lists the equipment required to run the PDT for the Interval Timer Module. There are two forms for the object program of the PDT. One, the PTO (TI part no. 942715-1101) is for the paper-tape reader and the other, CDO (TI part no. 942715-1201) is for the card reader.

8.2 PDT DESCRIPTION

The following paragraphs contain a description of the PDT for the Interval Timer Module.

8.2.1 INTRODUCTION. The Interval Timer Module PDT is called ITM960 and is contained at the end of this section. This test is used to verify the accuracy of the decrementing clock counter and valid occurrence of an interrupt using the appropriate counter from the module when properly installed in the CRU.

8.2.2 EQUIPMENT CONFIGURATION. The CRU Interval Timer Module is installed in the CRU at location $EF3_{16}$. No other interrupt producing CRU modules should be installed while this test is in progress. 4K of memory and a loading device such as a paper tape reader, card reader or an ASR733 terminal are required.

8.2.3 DATA STRUCTURE. Data blocks are an integral part of the loaded program and do not require reinitialization during execution. Repeated executions from initial loading can also be accomplished without further action on data blocks.

8.2.4 PROGRAM STRUCTURE. The ITM960 program logic is shown in the flowchart and the assembly language listing. ITM960 consists of a single procedure segment. Normal execution accomplishes the following functions:

1. INITIALIZATION. Loading followed by execution results in initial status register load for pre-indexing, supervisor mode execution, masking of all interrupts (X'01C0'), and transfer to label START. Base registers 4-5-6-7 are loaded. The CRU interrupt location (memory addresses X'0094' and X'0095') is loaded with a store status and branch instruction (SSB) to trap at the label TRAP. TRAP consists of a nine-word data block to process and save information from the CRU interrupts. Any illegal interrupt causes a program stop at label HALT (X'72D2',HALT) and the program relative halt address is displayable in INSTRUCTION REGISTER B. The module CRU lines are zeroed and a check is made to ensure that the module is plugged into the proper CRU slot. The interrupt line is cleared and the status register is reset to enable CRU interrupts.

2. ZERO INPUT INTERRUPT. The interrupt trap base address is altered to permit control by this function. The counter is loaded with a value of zero and a check is made for an interrupt. The interrupt is reset and the interrupt trap is set to the label TWO12 address. The counter is stopped and a check is made for no interrupt. A third alter interrupt trap base is used with a loop to continue the count until the value becomes - 1. A check for no interrupt is also made to end test two.

3. DECREMENT CHECK. The interrupt trap base address is altered to permit control by this function. The counter is loaded with a value of two and a loop is used to permit the counter to decrement one count. A check is made for no interrupt and then another loop for one count decrement. A check is made for an interrupt on this zero count. One more delay loop is used to check for no interrupt and negative count value.

4. CLOCK CALIBRATION. The interrupt trap base address is altered to permit control by this function. A one-count calibration uses the counter loaded with a value of one and the counter is started. A software execution loop using the 4 MHz instruction clock is used for the appropriate time delay. Then a check is made for an interrupt and the counter is stopped. The interrupt is cleared and the interrupt trap base address is reset for full counter calibration. For the counter to go from full value (X'3FFF') to zero using the 8 ms increment requires 131 seconds for an accuracy of 2.5 percent. The method used for one-count calibration is used here. Successful completion of the test is indicated by a delay visible on the console as an incrementing INSTRUCTION REGISTER B value.

5. RETURN TO LOADER. Normal test completion.

8.2.5 **SUPPORT PROGRAMS.** The Bootstrap Loader is required to load the object program. Refer to the CPU PAT's manual for loader program description and loading procedure.

8.2.6 **INPUT.** The ITM960 object program is entered by the loader if the program does not reside in memory. Further input is not necessary to begin execution if the module is plugged into the CRU at address EF3 (X'0F30'). Otherwise the program location specifying the CRU base address must be changed.

8.2.7 **OUTPUT.** Test output is in the form of visual displays from the console only. An error halt is indicated by execution of a branch relative instruction with $72D2_{16}$ displayable in INSTRUCTION REGISTER A and the program relative halt address displayable in INSTRUCTION REGISTER B. Normal test execution results in continued repeat of step 4 in paragraph 8.2.4, Clock Calibration.

8.2.8 **RESTRICTIONS.** The following restrictions must be observed.

- CRU location of the Interval Timer Module is assumed to be $EF3_{16}$ in the CRU. A different CRU base address requires the value at label CRULOC to be altered after loading and before execution.

- All time delay loops assume that one memory cycle of 750 nanoseconds is used every 30 microseconds to refresh semiconductor memory.

8.2.9 **LOADING PROCEDURES.** The following procedures should be followed in order to load ITM960 into the CPU.

1. Set the PC to the ITM960 first word address (assembly listing).

2. Select the appropriate option switch for the interval timer being tested. The options are as follows:

Switch 12	8 ms board
Switch 13	4 ms board
Switch 14	2 ms board
Switch 15	1 ms board

   If no switch is set, the program assumes a 1 ms board.

3. Select RUN and START. Execution begins immediately. Successful checkout results in a return to the loader.

4. SIE MODE permits observation of individual instruction executions and easy access to status and register contents as well as PC alterning. Note that part of the counter check function tests are based on clock times and execution under control of this mode may generate invalid results.

5. Any function test may be repeated or the program may be halted by altering the branch unconditional instruction (B $+2) at the end of each function. The complete program may be repeated or put into a continuous execution loop by altering the branch unconditional instruction (END4 B $+2) to return to the program first instruction.

6. A test failure is indicated by a program halt from execution of a branch relative halt (B @$,5) with the program relative half address displayable in INSTRUCTION REGISTER B. The failure location can be determined by comparison of this address with the location counter (LC) in the assembly listing.

8.2.10 **CONTROL FEATURES.** The following are control features of the ITM960 PDT.

1. NORMAL STOP. Upon completion of the test, control is returned to the loader. If an error occurs, a "B @$,5" is executed.

2. ERROR STOP. Any error halt results in a branch relative instruction (B @$,5) displayable in INSTRUCTION REGISTER A and the program relative halt address displayable in INSTRUCTION REGISTER B. Location of the error can be found by locating the halt address in the assembly listing.

3. RECOVERY PROCEDURE. The program may be stopped and restarted from any function execution or error by a CPU HALT and resetting the PC to the value of any one of the five function label addresses (labelled ONE through FIVE). Each function is independent.

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SAL990  V4L2  ITM960, INTERVAL TIMER MODULE TEST - PDT960A          PAGE  0004
  0814136  SEPT04, 1975

0001                        TITL ITM960, INTERVAL TIMER MODULE TEST - PDT960A
0002                *  TITLE=ITM960 - INTERVAL TIMER MODULE TEST - PDT960A
0003                *  REVISION=ECN#3P7951  MAY, 1974
0004                *   * REVISE ALL 'RTT*16' CRU BIT INSTRUCTIONS
0005                *   *    CHANGE TIME DELAY LOOPS TO ACCOUNT FOR A REFRESH
0006                *   *    CYCLE OF 750 NANOSECONDS EVERY 30 MICROSECONDS.
0007                *   *    INCLUDE SWITCH OPTIONS TO DETERMINE THE COUNTING
0008                *   *    INCREMENT SIZE.
0009                *  COMPUTER=960A,SAL
0010                *  ABSTRACT=THIS PROGRAM IS AN INDEPENDENT, STAND-ALONE
0011                *   * RELOCATABLE 960A PROGRAM DESIGNED TO VERIFY THE
0012                *   * ACCURACY OF THE DECREMENTING CLOCK COUNTER AND THE
0013                *   * VALID OCCURRENCE OF AN INTERRUPT FROM THE 960A CRU
0014                *   * INTERVAL TIMER MODULE INSTALLED IN THE CRU EXPANDER
0015                *   * RACK.  THE FORMAT OF THIS SOFTWARE ROUTINE IS
0016                *   * SIMILAR TO OTHER PAT960 PROGRAMS NOW IN USE.
0017                *   * THE CRU LOCATION OF THE INTERVAL TIMER MODULE IS
0018                *   * ASSUMED TO BE X'0F30'. A DIFFERENT CRU BASE ADDRESS
0019                *   * REQUIRES THE VALUE AT LABEL 'CRULOC' TO BE ALTERED
0020                *   * AFTER LOADING AND BEFORE EXECUTION.
0021                *   *THE COUNTING INCREMENT SIZE IS DETERMINED BY THE OPTION
0022                *   *SWITCHES.  ('UP' POSITION CAUSES THE DESCRIBED TIME)
0023                *   *8 MILLISECONDS      SWITCH 12
0024                *   *4 MILLISECONDS      SWITCH 13
0025                *   *2 MILLISECONDS      SWITCH 14
0026                *   *1 MILLISECOND       SWITCH 15
0027                *   *IF NO SWITCH IS SET, THE PROGRAM WILL DEFAULT TO ONE
0028                *   *MILLISECOND.
0029                *   *NOTE:  ALL DELAY LOOPS ASSUME THAT ONE MEMORY CYCLE OF
0030                *   *750 NANOSECONDS IS USED EVERY 30 MICROSECONDS TO
0031                *   *REFRESH SEMICONDUCTOR MEMORY.
0032                *   *NO EXTERNAL CONNECTIONS ARE USED.
0033                *   * REFERENCE SPECIFICATION INTERVAL TIMER MODULE -
0034                *   * 217331.
0035                *   * FUNCTIONS:
0036                *   * 1. INITIALIZATION - LOADING FOLLOWED BY EXECUTION
0037                *   *    RESULTS IN INITIAL STATUS REGISTER LOAD FOR PRE-
0038                *   *    INDEXING, SUPERVISOR MODE EXECUTION, MASKING OF
0039                *   *    ALL INTERRUPTS (X'01C0') AND TRANSFER TO LABEL
0040                *   *    'START'. BASE REGISTERS 4-5-6-7 ARE LOADED. X'94'
0041                *   *    AND X'95' ARE LOADED WITH A STORE STATUS AND BRANCH
0042                *   *    INSTRUCTION (SSB) TO TRAP AT LABEL 'TRAP'. TRAP
0043                *   *    CONSISTS OF A 9-WORD DATA BLOCK TO PROCESS AND SAVE
0044                *   *    INFORMATION FROM THE CRU INTERRUPTS. ANY ILLEGAL
0045                *   *    INTERRUPT CAUSES A PROGRAM STOP AT LABEL 'HALT'
0046                *   *    (X'7202',@HALT) AND THE PROGRAM RELATIVE HALT
0047                *   *    ADDRESS DISPLAYED IN INSTRUCTION REGISTER 8. THE
0048                *   *    MODULE CRU LINES ARE ZEROED AND A CHECK IS MADE TO
0049                *   *    INSURE THE MODULE IS PLUGGED INTO THE PROPER CRU
0050                *   *    SLOT. THE INTERRUPT LINE IS CLEARED AND THE STATUS
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SAL960  V4L2  ITM960, INTERVAL TIMER MODULE TEST - PDT960A              PAGE  0005
  08:41:36  SEPT04, 1975

0051                *   *     REGISTER IS RESET TO ENABLE CRU INTERRUPTS.
0052                *   *  2. ZERO INPUT INTERRUPT - THE INTERRUPT TRAP BASE
0053                *   *     ADDRESS IS ALTERED TO PERMIT CONTROL BY THIS
0054                *   *     FUNCTION. THE COUNTER IS LOADED WITH A VALUE OF
0055                *   *     ZERO AND A CHECK IS MADE FOR AN INTERRUPT. THE
0056                *   *     INTERRUPT IS RESET AND INTERRUPT TRAP SET TO LABEL
0057                *   *     'TWO12' ADDRESS. THE COUNTER IS STOPPED AND A
0058                *   *     CHECK IS MADE FOR NO INTERRUPT. A THIRD ALTER
0059                *   *     INTERRUPT TRAP BASE IS USED WITH A LOOP TO
0060                *   *     CONTINUE THE COUNT UNTIL THE VALUE BECOMES =1. A
0061                *   *     CHECK FOR NO INTERRUPT IS ALSO MADE TO END TEST 2.
0062                *   *  3. DECREMENT CHECK - THE INTERRUPT TRAP BASE ADDRESS
0063                *   *     IS ALTERED TO PERMIT CONTROL BY THIS FUNCTION. THE
0064                *   *     COUNTER IS LOADED WITH A VALUE OF TWO AND A LOOP IS
0065                *   *     USED TO PERMIT THE COUNTER TO DECREMENT ONE COUNT
0066                *   *     A CHECK IS MADE FOR NO INTERRUPT AND THEN ANOTHER
0067                *   *     LOOP FOR ONE COUNT DECREMENT.  A CHECK IS MADE FOR
0068                *   *     AN INTERRUPT ON THIS ZERO COUNT.  ONE MORE DELAY
0069                *   *     LOOP IS USED TO CHECK FOR NO INTERRUPT AND A
0070                *   *     NEGATIVE COUNT VALUE.
0071                *   *  4. CLOCK CALIBRATION - THE INTERRUPT TRAP BASE ADDRESS
0072                *   *     IS ALTERED TO PERMIT CONTROL BY THIS FUNCTION. A
0073                *   *     ONE COUNT CALIBRATION USES THE COUNTER LOADED WITH
0074                *   *     A VALUE OF ONE AND START COUNTER. A SOFTWARE
0075                *   *     EXECUTION LOOP USING THE 4 MEGAHZ INSTRUCTION CLOCK
0076                *   *     IS USED FOR THE APPROPRIATE MILLISECOND DELAY.
0077                *   *     THEN A CHECK IS MADE FOR AN INTERRUPT AND THE
0078                *   *     COUNTER IS STOPPED.  THE INTERRUPT IS CLEARED AND
0079                *   *     THE INTERRUPT TRAP BASE ADDRESS RESET FOR FULL
0080                *   *     COUNTER CALIBRATION.  FOR THE COUNTER TO GO FROM
0081                *   *     FULL VALUE (X'3FFF') TO ZERO USING THE 8 MSEC
0082                *   *     INCREMENT REQUIRES 131 SECONDS FOR ACCURACY OF
0083                *   *     2.5 PERCENT.  METHOD USED FOR ONE COUNT CALIBRATION
0084                *   *     IS USED HERE.  SUCCESFUL COMPLETION OF TEST IS
0085                *   *     INDICATED BY A DELAY VISIBLE ON THE CONSOLE AS AN
0086                *   *     INCREMENTING INSTRUCTION REGISTER R VALUE.
0087                *   *  5. RETURN TO LOADER - NORMAL TEST COMPLETION AND A
0088                *   *     RETURN TO LOADER CONTROL
0089                      PAGE
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SAL960  V4L2  ITM960, INTERVAL TIMER MODULE TEST - PDT960A          PAGE  0006
  0041838  SEPTM2, 1979

0090  0000            ITM960 PSEG                    INTERVAL TIMER MODULE TEST
0091  0000            ITMCHK EQU  ITM960
0092  0000                   DEF  RTTMCH             ITMCHK RETURN POINT
0093                  *
0094  0000            LOADER EQU  0                  BOOTSTRAP LOADER ENTRY POINT
0095                  *
0096                  *    1. INITIALIZATION
0097                  *
0098  0000 7C0A0002   ONE    LDS  STATUS             LOAD STATUS REGISTER BITS 7-8-9
0099  0002 0035       STATUS DATA CONTIN,X'01C0',0   SET STATUS BITS 7-8-9
      0003 01C0
      0004 0000
0100                  *
0101                  *      DATA STORAGE
0102                  *
0103  0005 0F30       CRULOC DATA X'0F30'            MODULE CRU BASE ADDRESS LOCN
0104                  *
0105  0006 0179       WAIT   DATA FOUR14+4,X'01C0'
      0007 01C0
0106  0008 0030       ENABLE DATA 0,X'0180'          STATUS ENABLE CRU INTERRUPTS
      0009 0180
0107                  *
0108  000A 7882       SSB    DATA X'7882',TRAP       CRU INTERRUPT LOCN INSTRUCTION
      000B 000C
0109                  *
0110  000C 0000       TRAP   DATA 0,0,TRAPSS         CRU INTERRUPT TRAP =  (SSB TRAP
      000D 0000
      000E 000F
0111  000F 7886       TRAPSS DATA X'7886',SSTAT      TRAP STORE STATUS =  (SS SSTAT)
      0010 0013
0112  0011 7202       HALT   DATA X'7202',$HALT      TRAP BRANCH = ($0$,5)
      0012 0011
0113  0013 0000       SSTAT  DATA 0,0                TRAP SS STORAGE
      0014 0000
0114                  *
0115  0015 01AB       RETURN DATA RTTMCH,X'01C0'     SET STATUS FOR RETURN
      0016 01C0
0116                  *
0117  0017 0000       ZERO   DATA 0                  ZERO
0118                  *
0119  0018 0001       COUNT1 DATA 1                  COUNT VALUE = ONE
0120                  *
0121  0019 0002       COUNT2 DATA 2                  COUNT VALUE = TWO
0122                  *
0123  001A 3FFF       FULL   DATA X'3FFF'            FULL COUNT VALUE = 14 BITS
0124                  *
0125  001B FFFF       ONES   DATA X'FFFF'            ALL ONES
0126                  *
0127  001C 08AE       TIMTAB DATA 2222               A MILLISECOND TABLE
0128  001D 0070              DATA 112
```

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SAL96P  V4L2  ITM96P, INTERVAL TIMER MODULE TEST - PDT960A              PAGE  0007
  0R141134  SEPT04, 1975

0129  0020 0459            DATA 1113
0130  0021 0718            DATA 1816
0131  0022 0408            DATA 1240
0132  0023 05F2            DATA 1506
0133  0024 0455            DATA 1109              4 MILLISECOND TABLE
0134  0025 0037            DATA 55
0135  0026 022C            DATA 556
0136  0027 4389            DATA 17289
0137  0028 026C            DATA 620
0138  0029 05F2            DATA 1506
0139  002A 022A            DATA 552               2 MILLISECOND TABLE
0140  002C 001B            DATA 27
0141  002D 0116            DATA 278
0142  002E 21C2            DATA 8642
0143  002F 0136            DATA 310
0144  0030 05F2            DATA 1506
0145  0031 0112            DATA 274               1 MILLISECOND TABLE
0146  0032 000D            DATA 13
0147  0033 0008            DATA 139
0148  0034 1168            DATA 4459
0149  0035 009B            DATA 155
0150  0036 05F2            DATA 1506
0151                 *
0152  0038           OPTION RES  1
0153                       PAGE
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SAL900  V4L2  ITM060, INTERVAL TIMER MODULE TEST - P0T9A0A                PAGE  0008
  00:41:38  SEPT04, 1979

0154  0035 4484A000 CONTIN LA   4,0                 SET DATA BASE REGISTER
0155  0037 44A50000        LA   5,ITMCHK            SET PROCEDURE BASE REGISTER
0156  0039 44A60034        LA   6,OPTION            POINT TO OPTION SWITCHES
0157  003B E4A00034        STPS OPTION              SAVE OPTION SWITCHES
0158  003D 24A0C843        BENE (0,12),1,FOURMS     IS 4MSEC FLAG SET?
0159  003F 44A0001C        LA   0,TIMTAB            YES, POINT TO APPROPRIATE TABLE
0160  0041 70A20051        B    STRTST              BRANCH TO CHANGE CODE
0161  0043 24A0D849 FOURMS BENE (0,13),1,TWOMS     IS 4MSEC FLAG SET?
0162  0045 44A00022        LA   0,TIMTAB+8          YES, POINT TO APPROPRIATE TABLE
0163  0047 70A20051        B    STRTST              BRANCH TO CHANGE CODE
0164  0049 24A0E84F TWOMS  BENE (0,14),1,ONEMS     IS 2MSEC FLAG SET?
0165  004B 44A00028        LA   0,TIMTAB+12         YES, POINT TO APPROPRIATE TABLE
0166  004D 70A20051        B    STRTST
0167  004F 44A0002E ONEMS  LA   0,TIMTAB+18         1MSEC FALG SET
0168  0051 4603A000 STRTST L    3,0,0               PICK UP FIRST VALUE IN TABLE
0169  0053 48A3A12C        ST   3,SNGLP+1           PUT IT IN THE CODE
0170  0055 4603A001        L    3,1,0               PICK UP SEC VALUE IN TABLE
0171  0057 48A3A138        ST   3,FOUR1+1           PUT IT IN THE CODE
0172  0059 4603A002        L    3,2,0               PICK UP THIRD VALUE IN TABLE
0173  005B 48A3A158        ST   3,LOOP41-1          PUT IT IN THE CODE
0174  005D 4603A003        L    3,3,0               PICK UP FOURTH VALUE IN TABLE
0175  005F 48A3A160        ST   3,RMLP+1            PUT IT IN THE CODE
0176  0061 4603A004        L    3,4,0               PICK UP FIFTH VALUE IN TABLE
0177  0063 48A3A16F        ST   3,FOUR3+1           PUT IT IN THE CODE
0178  0065 4603A005        L    3,5,0               PICK UP SIXTH VALUE IN TABLE
0179  0067 48A3A170        ST   3,FOUR3+3           PUT IT IN THE CODE
0180  0069 44A60014        LA   6,SSTAT+1           SET FLAG REGISTER TO STATUS LOC
0181  006B 4407A005        L    7,CRUBOC            SET CRU BASE REGISTER
0182  006D 340FA000        SETB 15,1                INITIAL STOP COUNTER
0183  006F 34A0A000        SETB 0,0                 INITIAL CLEAR INTERRUPT
0184                  *
0185  0071 44A0A011        LA   0,@HALT             LOAD TRAP BRANCH HALT ADDRESS
0186  0073 48A0A012        ST   0,HALT+1            RESTORE HALT TRAP BRANCH ADDR
0187                  *
0188  0075 14AAA034        MOV  SSB,@>34,4          LOAD CRU INTERRUPT LOCATION
0189  0077 14ABA035        MOV  SSB+1,@>35,4        LOAD SSB TRAP ADDRESS
0190                  *
0191  0079 44A0A017        L    0,ZERO              LOAD REGISTER WITH COUNT
0192  007B 28000080        LDCR (0,8),>80           CLEAR ALL MODULE LINES
0193                  *
0194  007D 2C000080        STCR (0,8),>80           INTERROGATE MODULE LINES
0195                  *
0196  007F 10A09410        CM   (>80,4),ONES        CONTINUITY CHECK
0197  0081 7202A081        B    @$,5                ERROR = INTERRUPT LINE NOT SET
0198  0083 7082A087        B    CLEAR               OK = MODULE INTERRUPT
0199  0085 7202A085        B    @$,5                MODULE NOT PLUGGED IN
0200                  *
0201  0087 34A0A000 CLEAR  SETB 0,0                 CLEAR INTERRUPT
0202  0089 44A1A08F        LA   1,END1              LOAD LDS TRANSFER ADDRESS
0203  008B 48A1A008        ST   1,ENABLE            ALTER LDS TRANSFER ADDRESS
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SAL990  V4L2  ITM990, INTERVAL TIMER MODULE TEST - PDT9900A          PAGE  0009
  00141136  SEPT84, 1979

0204  00BD 7C000008         LDS  ENABLE          ENABLE CRU INTERRUPTS
0205                       *
0206  00BF 70020001 END1   B    $+2             TEST 1, COMPLETE
0207                       *
0208                       *   2. ZERO INPUT INTERRUPT
0209                       *
0210  0091 340F0000 TWO    SETB 15,0            STOP COUNTER
0211  0093 34000000        SETB 0,0             CLEAR INTERRUPT
0212  0095 44810041        LA   1,@TWOI1        LOAD TRAP BRANCH ADDRESS
0213  0097 48810012        ST   1,HALT+1        ALTER TRAP BRANCH ADDRESS
0214  0099 44000017        L    0,ZERO          LOAD REGISTER WITH COUNT
0215  009B C801F080        LDCR (1,14),X'80'    ZERO 14 BITS COUNTER
0216  009D 340F0800        SETB 15,1            START COUNTER
0217                       *
0218  009F 7202009F        B    0$,$            ERROR - SHOULD CONTINUE AT $+2
0219                       *
0220  00A1 30000045 TWOI1  BBNE 0,0,$+4         CHECK FOR INTERRUPT
0221  00A3 7202FFA3        B    0$,$            ERROR - NO INTERRUPT
0222                       *
0223  00A5 34000000        SETB 0,0             CLEAR INTERRUPT
0224  00A7 44810040        LA   1,TWO1          LOAD LDS TRANSFER ADDRESS
0225  00A9 48810008        ST   1,ENABLE        ALTER LDS TRANSFER ADDRESS
0226  00AB 7C000008        LDS  ENABLE          CLEAR STATUS REGISTER
0227  00AD 4481FFCF TWO1   LA   1,@TWOI2        LOAD TRAP BRANCH ADDRESS
0228  00AF 48810012        ST   1,HALT+1        ALTER TRAP BRANCH ADDRESS
0229  00B1 340F0000        SETB 15,0            STOP COUNTER
0230  00B3 2C01F080        STCR (1,14),X'80'    RETRIEVE COUNT VALUE
0231  00B5 10009418        CM   (X'80',4),ONES  CHECK FOR NEGATIVE VALUE
0232  00B7 7202FFB7         B    0$,$           ERROR - ILLEGAL VALUE
0233  00B9 70070000         NOP                 VALUE MAY BE ZERO
0234  00BB 70070000         NOP                 CONTINUE
0235                       *
0236  00BD 30000001        BBNE 0,1,$+4         CHECK FOR INTERRUPT
0237  00BF 7202FFBF TWOI2  B    0$,$            ERROR - INTERRUPT
0238                       *
0239  00C1 34000000        SETB 0,0             CLEAR INTERRUPT
0240  00C3 44810005        LA   1,@TWOI3        LOAD TRAP BRANCH ADDRESS
0241  00C5 48810012        ST   1,HALT+1        ALTER TRAP BRANCH ADDRESS
0242  00C7 340F0800        SETB 15,1            START COUNTER
0243  00C9 2C01F080 LOOP2  STCR (1,14),X'80'    RETRIEVE COUNT VALUE
0244  00CB 10009418        CM   (X'80',4),ONES  CHECK FOR -1 VALUE
0245  00CD 7202FFCD         B    0$,$           ERROR - ILLEGAL VALUE
0246  00CF 10020001         B    LOOP2          LOOP UNTIL COUNTER CHANGES
0247  00D1 70070000         NOP                 CONTINUE
0248                       *
0249  00D3 30000001        BBNE 0,1,END2        CHECK FOR INTERRUPT
0250  00D5 7202FFD5 TWOI3  B    0$,$            ERROR - INTERRUPT
0251                       *
0252  00D7 70020001 END2   B    $+2             TEST 2, COMPLETE
0253                       *
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SAL960  V4L2  ITM960, INTERVAL TIMER MODULE TEST - PDT0000A              PAGE  0010
  0B141136  SEPTM4, 1979

0254                    *    3. DECREMENT CHECK
0255                    *
0256  0000 340F0000 THREE   SETB 15,0              STOP COUNTER
0257  0004 34000000         SETB 0,0              CLEAR INTERRUPT
0258  0008 44810000         LA   1,@THREEI        LOAD TRAP BRANCH ADDRESS
0259  000C 48810012         ST   1,HALT+1         ALTER TRAP BRANCH ADDRESS
0260  0010 44000019         LA   0,COUNT2         LOAD REGISTER WITH COUNT
0261  0014 98010000         LDCR (1,14),X'80'     LOAD COUNT VALUE - TWO
0262                    *
0263  0018 340F0000         SETB 15,1             START COUNTER
0264  001C 9C01E080 LOOP31  STCR (1,14),X'80'     RETRIEVE COUNT VALUE
0265  0020 1C8A0001         CMI  (X'80',4),1      CHECK FOR VALUE OF 1
0266  0024 72020000         B    0$,5             ERROR - ILLEGAL VALUE
0267  0028 70020000         B    LOOP31           LOOP UNTIL COUNTER CHANGES
0268  002C 70070000         NOP                   CONTINUE
0269                    *
0270  0030 30000000         RBNE 0,1,LOOP32       CHECK FOR INTERRUPT
0271  0034 72020000         B    0$,5             ERROR - INTERRUPT
0272                    *
0273  0038 9C01E080 LOOP32  STCR (1,14),X'80'     RETRIEVE COUNT VALUE
0274  003C 10000417         CM   (X'80',4),ZERO   CHECK FOR ZERO COUNT
0275  0040 72020000         B    0$,5             ERROR - ILLEGAL VALUE
0276  0044 70020000         B    LOOP32           LOOP UNTIL COUNTER CHANGES
0277  0048 72020000         B    0$,5             ERROR - SHOULD INTERRUPT
0278                    *
0279  004C 30000000 THREEI  RBNE 0,1,THREET       CHECK FOR INTERRUPT
0280  0050 34000000         SETB 0,0              CLEAR INTERRUPT
0281  0054 44830000         LA   3,LOOP33         LOAD LDS TRANSFER ADDRESS
0282  0058 48830000         ST   3,ENABLE         ALTER LDS TRANSFER ADDRESS
0283  005C 7C000000         LDS  ENABLE           CLEAR STATUS REGISTER
0284                    *
0285  0060 9C01E080 LOOP33  STCR (1,14),X'80'     RETRIEVE COUNT VALUE
0286  0064 10000418         CM   (X'80',4),ONES   CHECK FOR -1 COUNT
0287  0068 72020000         B    0$,5             ERROR - ILLEGAL VALUE
0288  006C 70020000         B    LOOP33           LOOP UNTIL COUNTER CHANGES
0289  0070 70070000         NOP                   CONTINUE
0290                    *
0291  0074 30000000         RBNE 0,1,$+4          CHECK FOR INTERRUPT
0292  0078 72020000         B    0$,5             ERROR - INTERRUPT
0293                    *
0294  007C 340F0000         SETB 15,0             STOP COUNTER
0295  0080 34000000         SETB 0,0              CLEAR INTERRUPT
0296                    *
0297  0084 70020000 END3    B    $+2              TEST 3. COMPLETE
0298                    *
0299                    *    4. CLOCK CALIBRATION
0300                    *       INSTRUCTION EXECUTION TIMES FOR TIME DELAY FOLLOW.
0301                    *       COUNT BEGINS AFTER EXECUTION OF THE START COUNTER
0302                    *       (SETB) INSTRUCTION AND ENDS ON ZERO COUNT.
0303                    *            LA      2.583 MICROSECONDS
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SAL968  V4L2  ITM968, INTERVAL TIMER MODULE TEST - PDT968A              PAGE  0011
  0814136  SEPT84, 1979

0304                    *               ST      3.583 MICROSECONDS
0305                    *               B       3.117 MICROSECONDS
0306                    *               ARB     3.416 MICROSECONDS (NO SIGN CHANGES)
0307                    *               ARR     3.167 MICROSECONDS (IF SIGN CHANGES)
0308                    *               BBNE    3.083 MICROSECONDS
0309                    *
0310                    *8MSEC ONE CLOCK CALIBRATION REQUIRES DELAY OF 8000
0311                    *       +/- 200 MICROSECONDS.  INTERRUPT WINDOW IS 7800 TO
0312                    *       8200 MICROSECONDS.
0313                    *4MSEC ONE CLOCK CALIBRATION REQUIRES DELAY OF 4000
0314                    *       +/- 100 MICROSECONDS.  INTERRUPT WINDOW IS 3900 TO
0315                    *       4100 MICROSECONDS.
0316                    *2MSEC ONE CLOCK CALIBRATION REQUIRES DELAY OF 2000
0317                    *       +/- 50 MICROSECONDS. INTERRUPT WINDOW IS 1950 TO
0318                    *       2050 MICROSECONDS.
0319                    *1MSEC ONE CLOCK CALIBRATION REQUIRES DELAY OF 1000
0320                    *       +/- 25 MICROSECONDS. INTERRUPT WINDOW IS 975 TO
0321                    *       1025 MICROSECONDS.
0322                    *
0323  0110 340F0000     FOUR    SETB 15,0               STOP COUNTER
0324  0112 34000000             SETB 0,0                CLEAR INTERRUPT
0325  0114 44810134             LA   1,@FOURT1          LOAD TRAP BRANCH ADDRESS
0326  0118 48810012             ST   1,HALT+1           ALTER TRAP BRANCH ADDRESS
0327  011C 44000018             L    0,COUNT1           LOAD REGISTER WITH COUNT
0328  0120 D801F080             LDCR (1,14),X'80'       LOAD COUNT VALUE - ONE
0329                    *
0330  0124 340F0000             SETB 15,1               START COUNTER
0331  0128 44810000     SNGLP   LA   1,$-$              SINGLE LOOP
0332  012C 0C1F0120             ARR  -1,$,1             DELAY
0333  0130 44820138             LA   2,@FOURT2          LOAD TRAP BRANCH ADDRESS 2.583
0334  0134 48820012             ST   2,HALT+1           ALTER TRAP BRANCH ADDRESS3.583
0335  0138 70020134             B    FOUR1              INTERRUPT MUST NOT OCCUR 3.117
0336                    *
0337  013C 7202013C     FOURI1  B    @$,5               ERROR - INTERRUPT
0338                    *
0339  0140 44020000     FOUR1   LA   2,$-$              WINDOW
0340  0144 0C2F0144             ARR  -1,$,2             DELAY
0341                    *
0342  0148 3000013F     FOURI2  BBNE 0,0,$+4            CHECK FOR INTERRUPT
0343  014C 7202014C             B    @$,5               ERROR - NO INTERRUPT
0344                    *
0345  0150 34000000             SETB 0,0                CLEAR INTERRUPT
0346  0154 44030154             LA   3,FOUR1E           LOAD LDS TRANSFER ADDRESS
0347  0158 48030008             ST   3,ENABLE           ALTER LDS TRANSFER ADDRESS
0348  015C 7C000008             LDS  ENABLE             CLEAR STATUS INTERRUPT
0349                    *
0350  0160 70020164     FOUR1E  B    $+2                ONE COUNT CALIBRATION OK
0351                    *
0352                    *       FULL COUNT CALIBRATION (16383 COUNTS)
0353                    *8MSEC REQUIRES DELAY LOOP OF 131064 +/- 3276 MILLISECONDS
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SAL960  V4L2  ITM060, INTERVAL TIMER MODULE TEST - POTGRA          PAGE  0012
  0A141136  SEPTM4, 1975

0354                    *       INTERRUPT WINDOW IS 127788 TO 134340 MILLISECONDS
0355                    *4MSEC REQUIRES DELAY LOOP OF 65532 +/- 1638 MILLISECONDS
0356                    *       INTERRUPT WINDOW IS 63894 TO 67170 MILLISECONDS
0357                    *2MSEC REQUIRES DELAY LOOP OF 32766 +/- 819 MILLISECONDS
0358                    *       INTERRUPT WINDOW IS 31947 TO 33585 MILLISECONDS
0359                    *1MSEC REQUIRES DELAY LOOP OF 16383 +/- 409 MILLISECONDS
0360                    *       INTERRUPT WINDOW IS 15974 TO 16792 MILLISECONDS.
0361                    *NOTE: ALL DELAY LOOPS ASSUME THAT ONE MEMORY CYCLE OF 750
0362                    *       NANOSECONDS IS USED EVERY 30 MICROSECONDS TO REFRESH
0363                    *       SEMICONDUCTOR MEMORY.
0364                    *THE INTERVAL TIMER IS CHECKED TO AN ACCURACY OF 2.5 PERCENT
0365                    *
0366  0149 340F0000 FOUR2   SETB  15,0              STOP COUNTER
0367  014B 34000000         SETB  0,0              CLEAR INTERRUPT
0368  014D 44810168         LA    1,@FOURT3        LOAD TRAP BRANCH ADDRESS
0369  014F 48810012         ST    1,HALT+1         ALTER TRAP BRANCH ADDRESS
0370  0151 4400001A         L     0,FULL           LOAD REGISTER WITH COUNT
0371  0153 E801E000         LDCR  (1,14),X'80'     LOAD FULL COUNT VALUE = 16383
0372                    *
0373  0155 340F0800         SETB  15,1             START COUNTER
0374  0157 44810000         LA    1,$-$            OUTER LOOP
0375  0159 44827FFF LOOP41  LA    2,X'7FFF'         INNER LOOP = 32,767 TIMES
0376  015B DC2F0150         ARR   -1,*,2            INNER LOOP
0377  015D DC1F0159         ARR   -1,LOOP41,1       OUTER LOOP
0378  015F 44830000 RMLP    LA    3,$-$            REMAINDER LOOP              2,583
0379  0161 DC3F0161         ARR   -1,*,3
0380  0163 30000163         BBNE  0,0,$            ERROR IF BOARD IS REMOVED
0381  0165 44820175         LA    2,@FOURI4         LOAD TRAP BRANCH ADDRESS
0382  0167 48820012         ST    2,HALT+1          ALTER TRAP BRANCH ADDRESS
0383  0169 7002016D         B     FOUR3
0384                    *
0385  016B 7202016B FOURI3  B     0*,*
0386                    *
0387  016D 44830000 FOUR3   LA    3,$-$            LOAD TOLERANCE LOOP
0388  016F 44820000         LA    2,$-$            INNER TOLERANCE LOOP
0389  0171 DC2F0171         ARR   -1,*,2            INNER LOOP
0390  0173 DC3F016F         ARR   -1,*-4,3          OUTER LOOP
0391                    *
0392  0175 30000178 FOURI4  BBNE  0,0,FOUR4         CHECK INTERRUPT
0393  0177 7C000006         LDS   WAIT
0394  0179 7202017B         B     0*,*             ERROR NO INTERRUPT
0395                    *
0396  017B 70820170 FOUR4   B     *+2              FULL COUNT CALIBRATION OK
0397                    *
0398  017D 340F0000         SETB  15,0             STOP COUNTER
0399  017F 34000000         SETB  0,0              CLEAR INTERRUPT
0400  0181 44830187         LA    3,DELAY1         LOAD LDS TRANSFER ADDRESS
0401  0183 48830008         ST    3,ENABLE         ALTER LDS TRANSFER ADDRESS
0402  0185 7C000008         LDS   ENABLE           CLEAR STATUS INTERRUPT
0403                    *
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SAL990  V4L2  ITM990, INTERVAL TIMER MODULE TEST - PDT9A0A              PAGE  0013
  0A141136  SEPTM4, 1975

0404                    *         DELAY FOR POSSIBLE HALT
0405                    *
0406  0187 4883018A DELAY1 ST    3,$+3             STORE SR3 IN LOWER NOP
0407  0189 7007A000         NOP                    TEMPORARY REGISTER STORAGE
0408  018B BC310187         ARR   +1,DELAY1,3      DELAY FOR POSSIBLE HALT
0409  018D 4883A190 DELAY2 ST    3,$+3             STORE SR3 IN LOWER NOP
0410  018F 7007A000         NOP                    TEMPORARY REGISTER STORAGE
0411  0191 BC31018D         ARR   +1,DELAY2,3      DELAY FOR POSSIBLE HALT
0412  0193 4883A196 DELAY3 ST    3,$+3             STORE SR3 IN LOWER NOP
0413  0195 7007A000         NOP                    TEMPORARY REGISTER STORAGE
0414  0197 BC310193         ARR   +1,DELAY3,3      DELAY FOR POSSIBLE HALT
0415  0199 4883A19C DELAY4 ST    3,$+3             STORE SR3 IN LOWER NOP
0416  019B 7007A000         NOP                    TEMPORARY REGISTER STORAGE
0417  019D BC310199         ARR   +1,DELAY4,3      DELAY FOR POSSIBLE HALT
0418  019F 4883A1A2 DELAY5 ST    3,$+3             STORE SR3 IN LOWER NOP
0419  01A1 7007A000         NOP                    TEMPORARY REGISTER STORAGE
0420  01A3 BC31019F         ARR   +1,DELAY5,3      DELAY FOR POSSIBLE HALT
0421                    *
0422  01A5 70A20147 END4   B     $+2               TEST 4, COMPLETE
0423                    *
0424                    *    5, RETURN TO LOADER
0425                    *
0426  01A7 34000000 FIVE   SETB  0,0               CLEAR INTERRUPT
0427  01A9 7C000015         LDS   RETURN           LOAD STATUS TO MASK INTERRUPTS
0428                    *
0429  01AB 70020000 RTTMCH B     LOADER            RETURN TO LOADER CONTROL
0430  01AD                  END   STATUS
```

ALPHABETICAL INDEX

INTRODUCTION

The following index lists key words and concepts from the subject material of the manual together with the area(s) in the manual that supply major coverage of the listed concept. The numbers along the right side of the listing reference the following manual areas:

- Sections - References to Sections of the manual appear as "Section x" with the symbol x representing any numeric quantity.
- Appendixes - References to Appendixes of the manual appear as "Appendix y" with the symbol y representing any capital letter.
- Paragraphs - References to paragraphs of the manual appear as a series of alphanumeric or numeric characters punctuated with decimal points. Only the first character of the string may be a letter; all subsequent characters are numbers. The first character refers to the section or appendix of the manual in which the paragraph is found.
- Tables - References to tables in the manual are represented by the capital letter T followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the table). The second character is followed by a dash (-) and a number:

  Tx-yy

- Figures - References to figures in the manual are represented by the capital letter F followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the figure). The second character is followed by a dash (-) and a number:

  Fx-yy

- Other entries in the Index - References to other entries in the index are preceded by the word "See" followed by the referenced entry.

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Interval Timer Module User's Manual (966374-9701)

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Please list any discrepancy found in this manual by page, paragraph, figure, or table number in the following space. If there are any other suggestions that you wish to make, feel free to include them. Thank you.

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