AN ABSTRACT OF THE THESIS OF

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Title: An Integrated Analog Multiplier Circuit.

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James C. Looney

The exponential characteristic of the base-emitter junction in bipolar transistors was used to make an accurate and fairly temperature independent multiplier.

Using hybrid-pi transistor models and ECAP, a bandwidth of 350 MHz was predicted. Linearity is limited by emitter degeneration in the input differential stage rather than by the small errors in the actual multiplying stage.

The multiplier was fabricated as a monolithic integrated circuit in the Tektronix integrated circuits laboratory. The prototype showed a bandwidth of 200 MHz, and a linearity of 2% over 50% of the dynamic range, when used as a variable gain amplifier.

An Integrated Analog Multiplier Circuit

by

Einar Traa

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AN INTEGRATED ANALOG MULTIPLIER CIRCUIT

INTRODUCTION

With the development of monolithic integrated circuits many new circuit configurations became possible. One reason is that pairs of devices in these circuits can be made with characteristics that match far better than those of discrete devices.

The circuit that is described here is one that requires extremely good matching in order to operate with any accuracy. It was suggested by Barrie Gilbert of Tektronix Inc., and is an off-spring of his work on gain-cell current amplifiers.

The existing samples were designed and built by the integrated circuits group at Tektronix.

A theoretical treatment is first presented, where the principle is established, followed by theoretical prediction of the performance. The design and testing of the circuit is then described. After that the experimental results are reported. Finally some conclusions and suggestions for further work on the project are presented.

THEORETICAL DISCUSSION

Basic Principle.

When deriving the multiplication principle it will be assumed that the transistors do not have any bulk resistances, and that the collector output impedances are infinite. The parameter α is assumed equal to one.

For a p-n junction:

$$I = I_o(\exp\frac{qV}{kT} - 1) \approx I_o \exp\frac{qV}{kT}$$

or

$$V \approx \frac{kT}{q}\log\frac{I}{I_o}$$

Since α=1, for a transistor,

$$I_e = I_c = I_o \exp\frac{qV_{be}}{kT}$$

or

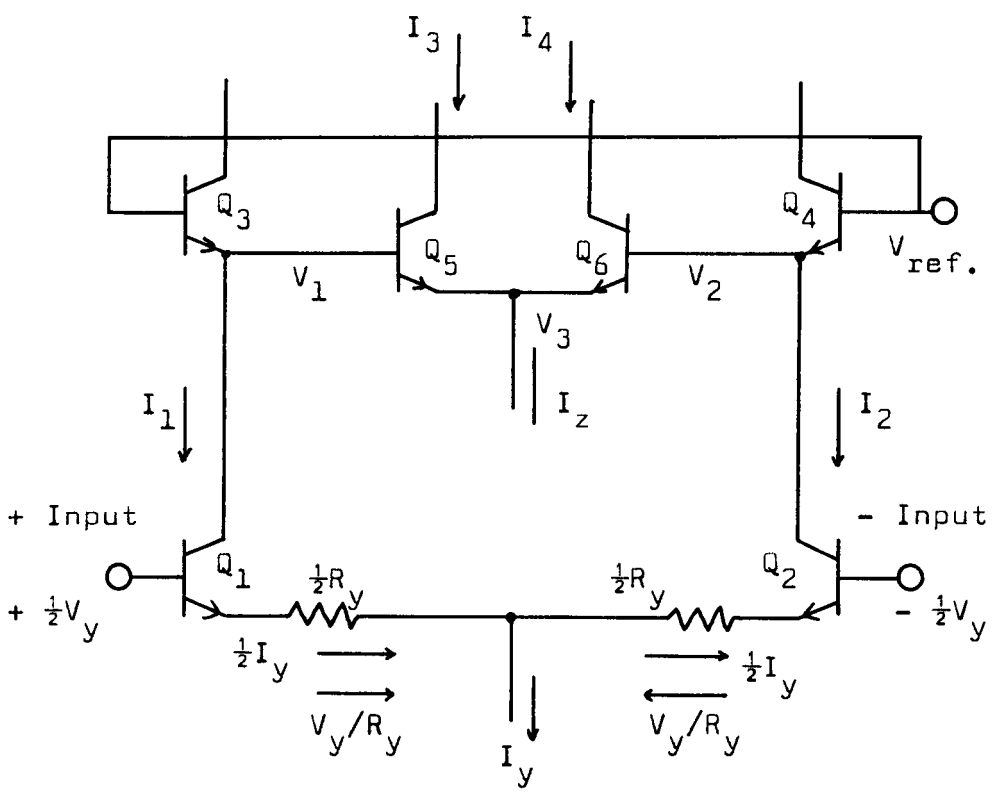
$$V_{be} = \frac{kT}{q}\log\frac{I_e}{I_o}$$

Looking at Fig. 1a, the input can be considered a differential amplifier with a current long-tail. At this point the base-emitter voltage will be neglected, and since R_y is a linear resistor the superposition principle applies. Now I_1 and I_2 can each be considered the sum of

two components. One is $\frac{1}{2}I_y$, which would be the current with no differential voltage on the inputs, and the other, V_y/R_y which is due to the voltage difference between the two inputs. Adding these algebraically gives,

$$I_1 = \tfrac{1}{2}I_y + \frac{V_y}{R_y} \quad \text{and} \quad I_2 = \tfrac{1}{2}I_y - \frac{V_y}{R_y}$$

Fig. 1a. Basic variable gain current amplifier (gain-cell).



Using the bases of Q_3 and Q_4 as voltage reference,

$$V_1 = -\frac{kT}{q}\log\frac{I_1}{I_o} \quad \text{and} \quad V_2 = -\frac{kT}{q}\log\frac{I_2}{I_o}$$

Further,

$$I_3 = I_o\exp\left(\frac{q(V_1-V_3)}{kT}\right)$$

$$I_4 = I_o\exp\left(\frac{q(V_2-V_3)}{kT}\right)$$

Thus, one can write

$$\frac{I_3}{I_4} = \exp\left(\frac{q(V_1-V_3-V_2+V_3)}{kT}\right) = \exp\left(\frac{q(V_1-V_2)}{kT}\right)$$

$$= \exp\left(\frac{q}{kT}\left(-\frac{kT}{q}\right)\left(\log\frac{I_1}{I_o} - \log\frac{I_2}{I_o}\right)\right) = \frac{I_2}{I_1}$$

This result will now be used to show that Fig. 1a can be considered a current amplifier.

From above:

$$\frac{I_3}{I_4} = \frac{I_2}{I_1}$$

Reversing the proportion:

$$\frac{I_3}{I_2} = \frac{I_4}{I_1} = \frac{I_3+I_4}{I_2+I_1} = \frac{I_z}{I_y} = \frac{I_3}{\frac{1}{2}I_y - \frac{V_y}{R_y}} = \frac{I_4}{\frac{1}{2}I_y + \frac{V_y}{R_y}}$$

From these proportions,

$$I_3 = \tfrac{1}{2}I_z - \frac{V_y I_z}{R_y I_y}$$

$$I_4 = \tfrac{1}{2}I_z + \frac{V_y I_z}{R_y I_y}$$

and

$$I_4 - I_3 = 2\frac{V_y I_z}{R_y I_y}$$

Compare this to

$$I_1 - I_2 = 2\frac{V_y}{R_y},$$

and it is proved that the top four transistors (the "gain cell") in Fig. 1a have a current gain of I_z/I_y.

One can add another pair of output transistors, Q_7 and Q_8 in Fig. 1b, without changing the operation of the already existing circuit.

From the previous analysis, by similarity:

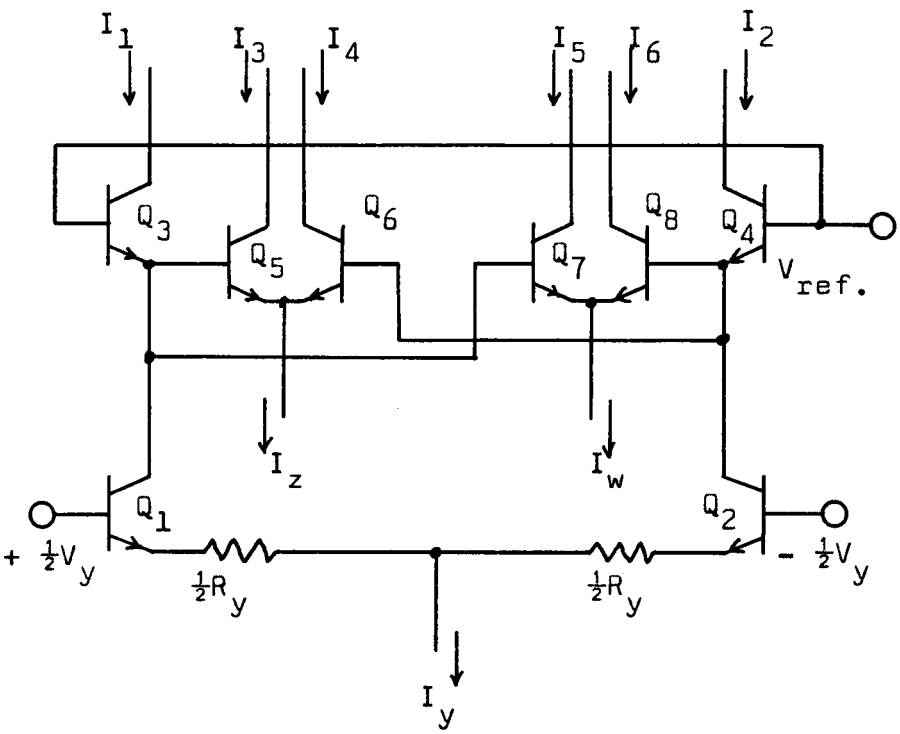
$$I_6 = I_1(\frac{I_w}{I_y}) \quad \text{and} \quad I_5 = I_2(\frac{I_w}{I_y}).$$

Substituting for I_1 and I_2,

$$I_6 = \tfrac{1}{2}I_w + \frac{V_y I_w}{R_y I_y} \quad \text{and} \quad I_5 = \tfrac{1}{2}I_w - \frac{V_y I_w}{R_y I_y}$$

The circuit in Fig. 1b can now be considered an amplifier with one input and two outputs. One output

Fig. 1b. Dual output current amplifier.



has gain regulated by I_z and the other by I_w.

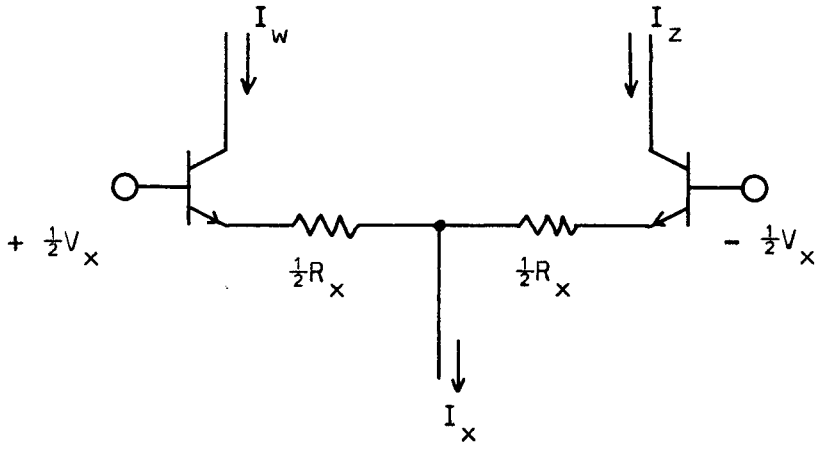
$$I_4 - I_3 = 2\frac{V_y I_z}{R_y I_y} \quad \text{and} \quad I_6 - I_5 = 2\frac{V_y I_w}{R_y I_y}$$

Now, suppose that the two outputs are added together with opposite polarity, then,

$$I_{diff,\ out} = (I_6 - I_5) - (I_4 - I_3) = \frac{2V_y}{R_y I_y}(I_w - I_z).$$

In order to make a multiplier it is necessary to make $I_w - I_z$ proportional to an input voltage V_x. This can be done with a differential input, like the one shown in Fig. 1c.

Fig. 1c. Differential input, used for gain control in Fig. 1b.



From Fig. 1c.

$$I_w - I_z = \tfrac{1}{2}I_x + \frac{V_x}{R_x} - \tfrac{1}{2}I_x + \frac{V_x}{R_x} = 2\frac{V_x}{R_x}$$

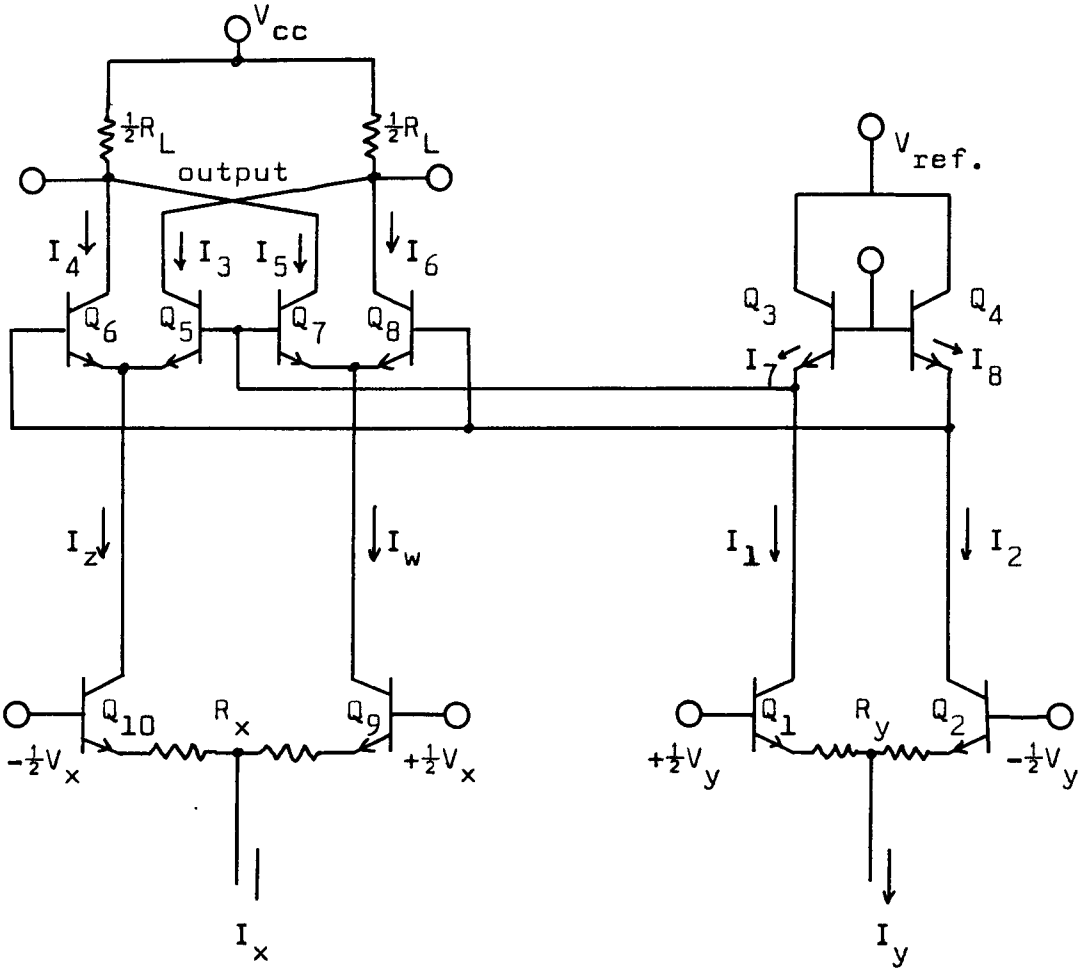
So,

$$I_{diff,\ out} = \frac{2V_y}{R_y I_y}(I_w - I_z) = \frac{4V_x V_y}{R_x R_y I_y}$$

Fig. 2 shows the combination of Fig. 1b and Fig. 1c, with the combined outputs fed into load resistors. The voltage output will be:

$$V_{diff,\ out} = \frac{2V_x V_y R_L}{R_x R_y I_y}.$$

Fig. 2. The complete four quadrant multiplier.



Effects of Base Currents.

In the preceeding analysis it has been assumed that $\alpha=1$. This is not true for a practical transistor, and the effect of this has to be investigated.

In Fig. 2, when $\alpha \neq 1$,

$$I_7 = I_1 + \frac{I_5+I_3}{\beta}$$

and

$$I_8 = I_2 + \frac{I_4+I_6}{\beta}$$

Furthermore,

$$I_1 = (\tfrac{1}{2}I_y + \frac{V_y}{R_y})\alpha$$

$$I_2 = (\tfrac{1}{2}I_y - \frac{V_y}{R_y})\alpha$$

$$I_3 = (\tfrac{1}{2}I_z - \frac{V_y I_z}{R_y I_y \alpha})\alpha$$

$$I_4 = (\tfrac{1}{2}I_z + \frac{V_y I_z}{R_y I_y \alpha})\alpha$$

$$I_5 = (\tfrac{1}{2}I_w - \frac{V_y I_w}{R_y I_y \alpha})\alpha$$

$$I_6 = (\tfrac{1}{2}I_w + \frac{V_y I_w}{R_y I_y \alpha})\alpha$$

Substituting this into the expressions for I_7 and I_8 gives:

$$I_7 = \alpha(\tfrac{1}{2}I_y + \frac{V_y}{R_y}) + \frac{\alpha}{\beta}(\tfrac{1}{2}I_z + \tfrac{1}{2}I_w - \frac{V_y}{R_y}(\frac{I_z+I_w}{\alpha I_y}))$$

$$= \alpha(\tfrac{1}{2}I_y + \frac{V_y}{R_y}) + \frac{\alpha}{\beta}(\tfrac{1}{2}I_x - \frac{V_y}{R_y}(\frac{I_x}{I_y}))$$

Similarly,

$$I_8 = \alpha(\tfrac{1}{2}I_y - \frac{V_y}{R_y}) + \frac{\alpha}{\beta}(\tfrac{1}{2}I_x + \frac{V_y}{R_y}(\frac{I_x}{I_y}))$$

Consider,

$$I_7 + I_8 = \alpha I_y + \frac{\alpha}{\beta}I_x$$

It makes the multiplier work as if the tail current I_y had actually been $I_y\alpha+\frac{\alpha}{\beta}I_x$.

The differential signal current is

$$I_7 - I_8 = 2\frac{V_y}{R_y}\alpha - 2\frac{\alpha V_y I_x}{\beta R_y I_y} = 2\frac{V_y}{R_y}(\alpha - \frac{\alpha}{\beta}\frac{I_x}{I_y}).$$

This gives a correction factor,

$$(\alpha - \frac{\alpha}{\beta}\frac{I_x}{I_y})$$

On the x-input it is noted that since the ratio between I_z and I_w is not altered by α not being unity, and I_z and I_w are multiplied by α, their difference, and

thereby also the gain is multiplied by α. The same reasoning applies to the four output transistors, and this multiplies the gain of the circuit with α again, a total of α^2.

The corrected gain is

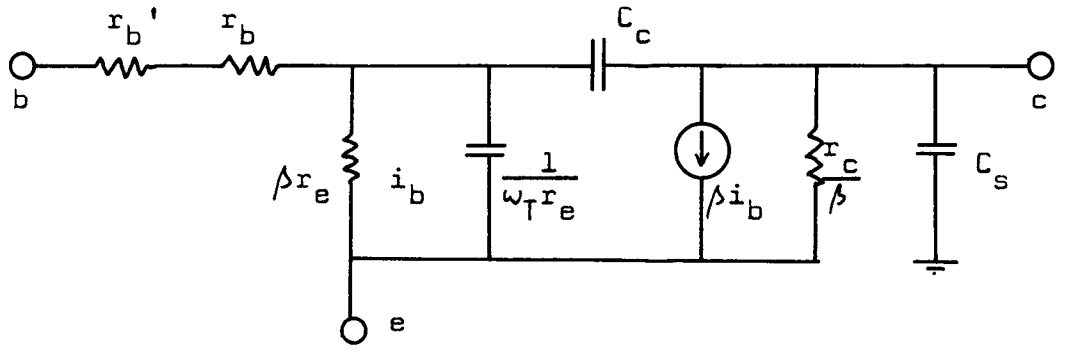
$$V_{out,\ diff.} = \frac{2V_x V_y R_L}{R_x R_y I_y}\left(\frac{\alpha - \frac{\alpha I_x}{\beta I_y}}{\alpha + \frac{\alpha I_x}{\beta I_y}}\right)$$

Modeling to find Bandwidth.

When designing integrated circuits, one has the opportunity to also design the actual transistors that are used. This suggests the use of models with parameters that can be calculated directly from the geometry, and also conveniently measured. A convenient model is the "hybrid pi" model (6 p. 22) that is shown in Fig. 3.

The junction capacitances can generally be estimated using a method given in (5, Sec. 7-4) which uses data from (4). Section 7-5 in (5) treats transistor beta. In practice, when designing circuits, device samples will usually be available to measure these parameters on.

Fig. 3. Hybrid pi model of an integrated circuit transistor.



$\omega_T = 2\pi f_T$

r_e = Impedance of the emitter junction.

r_b' = Bulk resistance of the inactive base region.

r_b = Bulk resistance of the active base region.

C_c = Capacitance of the collector-base junction.

C_s = Capacitance of the collector-substrate junction.

β = Forward current transfer ratio.

r_c = Collector impedance for a common base configuration, with the base grounded.

The collector impedance, r_c, cannot be calculated from the geometry alone, but this is usually no problem. In monolithic integrated circuits most resistors are so small that the collector can be considered an ideal current source.

A simple way to calculate r_b' is to use the geometry of the device, and sheet resistivity of the inactive base region. Again, if samples are available it can be measured. It is approximately equal to the Zener impedance of the emitter-base junction.

It is a little more complicated to calculate r_b accurately, but a good estimate can be made. Using Irvin's curves (3, p. 408) and data from the Tektronix diffusion process, it was found that a 1x0.4 mil emitter with double base stripe has a 380 ohms bulk resistance in the active base region for an infinitesimal current. However, due to the transverse voltage, caused by the base current, the voltage will not be the same across the junction. Consequently the current density is highest along the edges of the junction, lowering the actual bulk resistance of the active base region. Using the results of the analysis that Hauser has done, (1) the graph in Fig. 4 was made. It shows bulk resistance of the active base vs. emitter current for the transistors that were used in the multiplier.

The impedance of the emitter junction is given by the relation

$$r_e = \frac{kT}{qI_e}$$

where

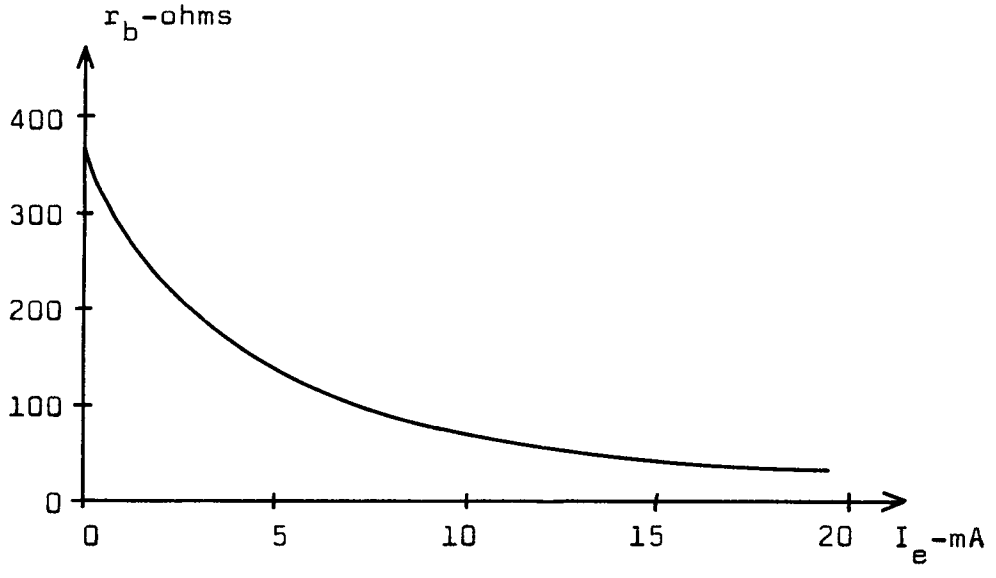
k = Boltzman's constant

T = Absolute temperature

q = charge of an electron

I_e = Emitter current

Fig. 4. Bulk resistance of the active base (r_b) versus emitter current.



Actually, the emitter-base junction is a distributed RC network at high frequencies. Alumped parameter model can still be used to find the approximate cut-off frequency of the circuit. Above that distributed models are needed if any accuracy is wanted. Fig. 5 shows the distributed version of the model in Fig. 3.

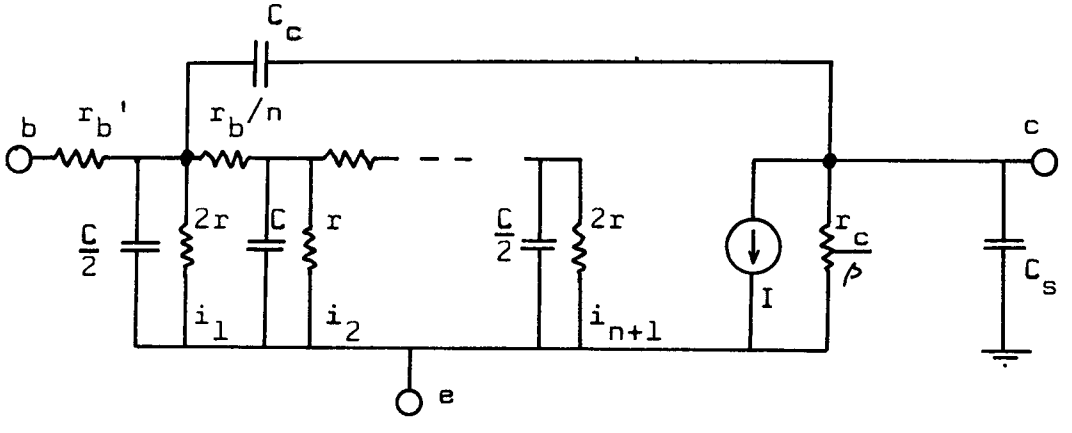
Fig. 5. Distributed hybrid pi transistor model.

$$C = \frac{1}{\omega_T r_e n}$$

$$r = n r_e \beta$$

$$I = \beta \sum_{j=1}^{n+1} i_j$$

n = number of sections (infinite for true distributed models)



The collector-base capacitance can still be fed back to the bulk resistance of the inactive base region with reasonable accuracy, since very little of it is actually under the active base.

Because of symmetry it was only necessary to use one half of the circuit. In Fig. 2, I_3 and I_5 are complimentary to each other, making their signal components equal and opposite. Thus the collector of Q_5 can be grounded through a load resistor, and the grounded current be used to drive a current source of opposite polarity to simulate I_5 coming from Q_7. See Fig. 6c.

The equivalent circuit was used only to predict the bandwidth of the circuit (and not the response past the cut-off frequency) so a distributed model was probably not required. However, since the bandwidth of the circuit depends heavily on device parameters, it was decided to use a quasi-distributed model. The model used is the one in Fig. 5 with n=2. It is redrawn in Fig. 6b for the two sections that were used.

Ecap AC analysis was used to analyze the equivalent circuit of the multiplier, (2).

Fig. 6a. The bias that was used in the analysis.

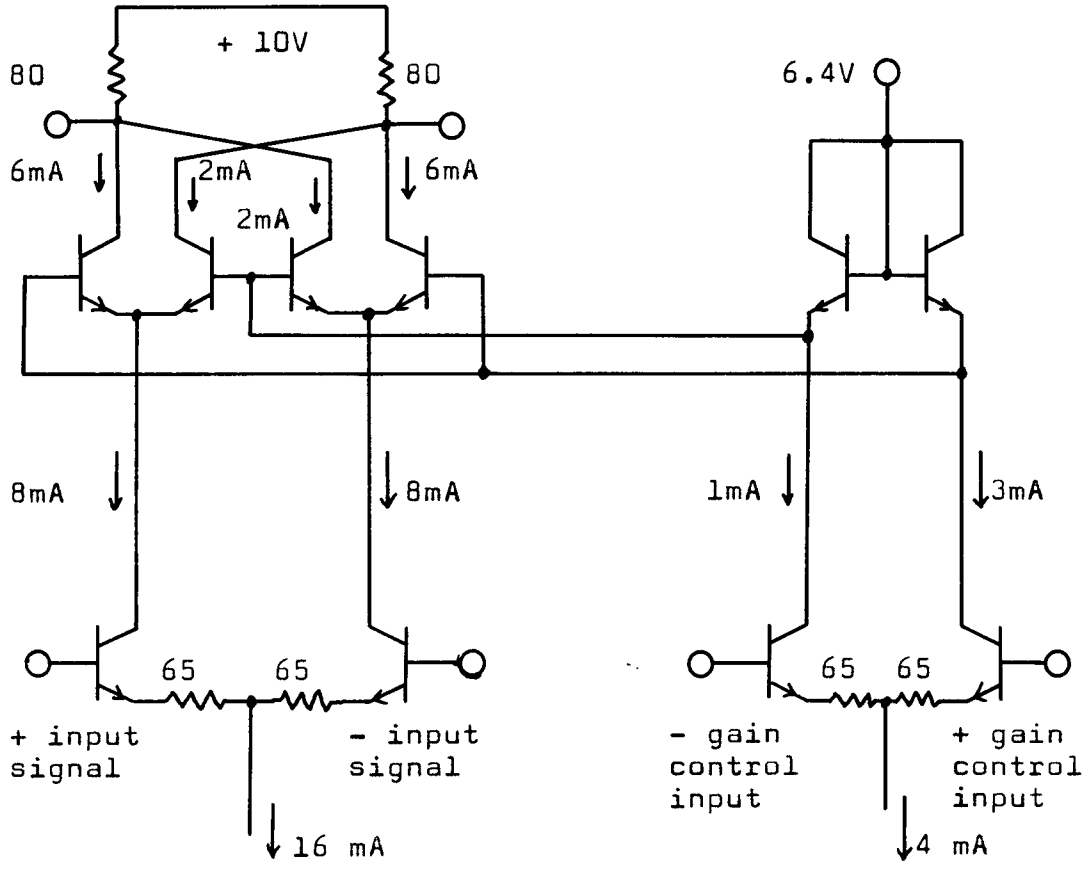
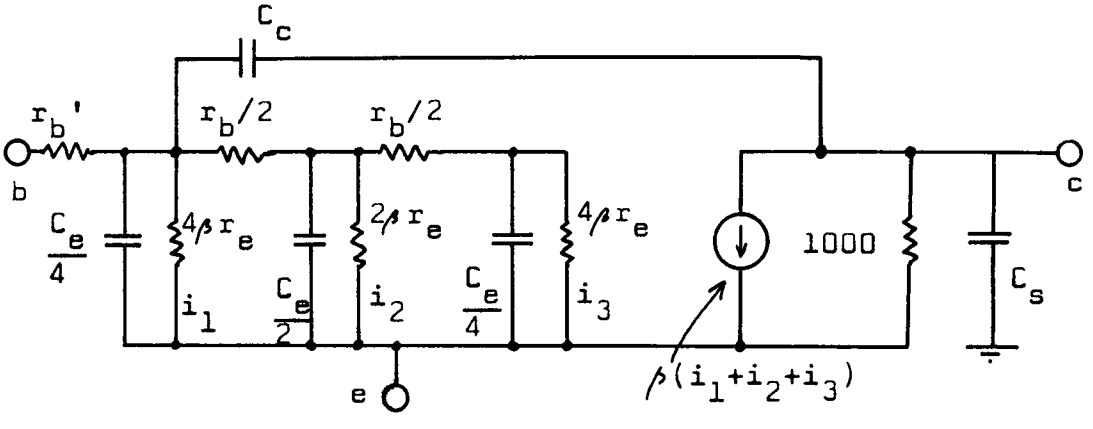


Fig. 6b. The transistor equivalent circuit that was used in the Ecap analysis.



The 1000 ohm resistor was picked arbitrarily, because Ecap requires a resistor on the current source, and all resistors that connect to any one node should be within a range of 1:1000 of each other. This should not make much difference on the bandwidth, since each collector drives a load that is significantly less than 1000 ohms.

r_b' = 33 ohms by measurements of existing samples.

$r_e = \frac{26\ mV}{I_e}$ $\quad r_e$ = 13.8 ohms for 2 mA
4.3 ohms for 6 mA
3.2 ohms for 8 mA

$C_e = \frac{1}{\omega_T r_e}$ $\quad C_e$ = 14.25 pF for 2 mA
42.8 pF for 6 mA
57.0 pF for 8 mA

ω_T = 5.4 Gigaradians per second by measurement of existing devices.

From Fig. 4: $\quad r_b$ = 220 ohms for 2 mA
110 ohms for 6 mA
80 ohms for 8 mA

C_s = 2.3 pF at -10 V; $C_s = 2.3(\frac{10}{V_{cs}})^{0.45}$

The exponent 0.45 has been found to be typical for this junction.

For V_{cs} = 19 V, C_s = 1.72 pF

For V_{cs} = 15 V, C_s = 1.92 pF

C_c = 0.15 pF at -10 V

$$C_c = 0.15\left(\frac{10}{V_{cb}}\right)^{0.36}$$

The exponent 0.36 has been found to be typical of this junction.

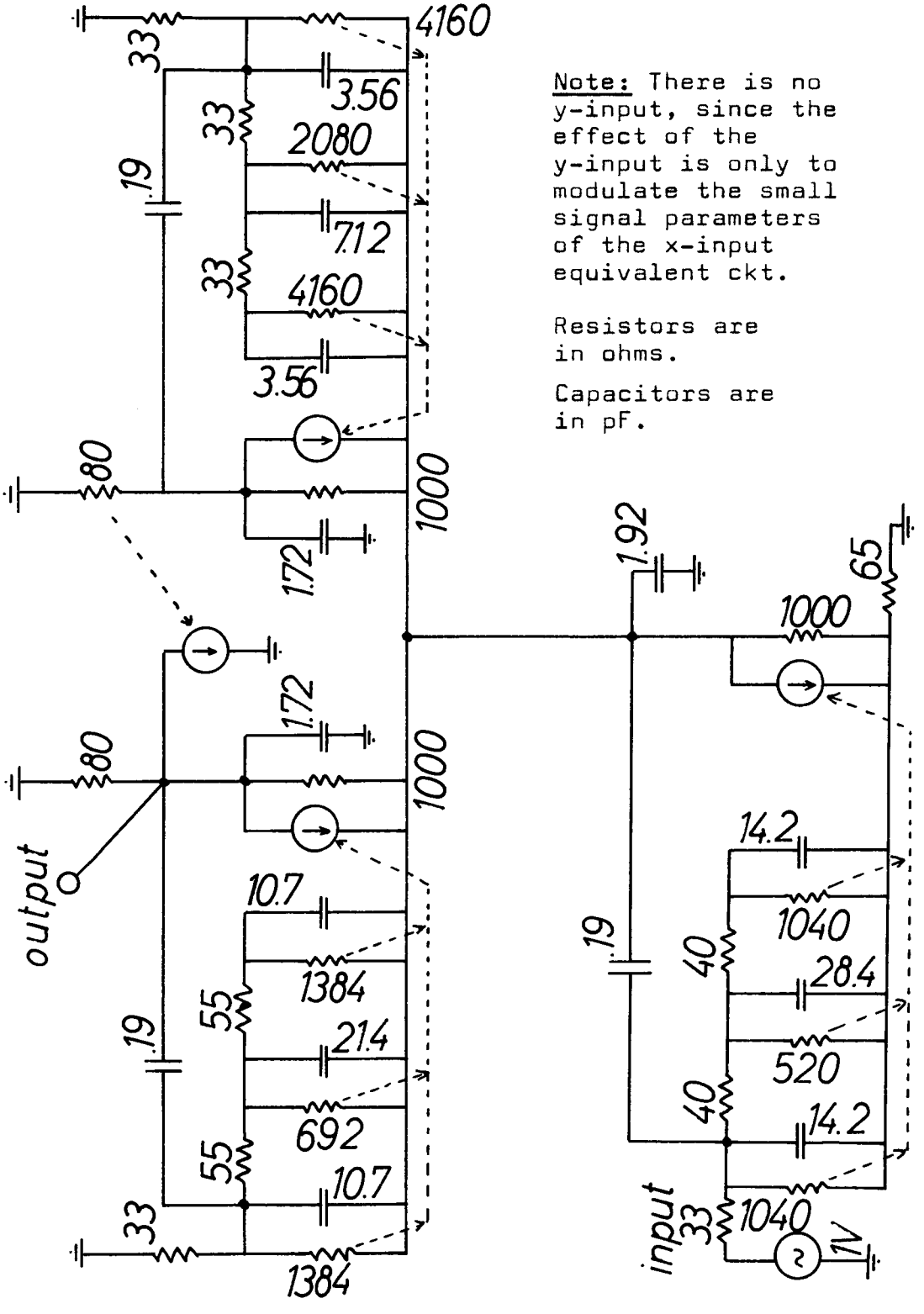
C_c = 0.19 pF since all V_{cb} in the circuit are 5 V.

β = 80, typical for the process and geometry.

Contact resistance between the metal film and the silicon is not considered here. This resistance may sometimes be significant, but it is so hard to predict, and varies so much from time to time, that a model trying to take it into account is not necessarily a better model than one without it.

The equivalent circuit in Fig. 6c gives a frequency response as shown in Fig. 7. The bandwidth is approximately 0.35 GHz, which corresponds to a risetime of about one nanosecond.

Fig. 6c. Ecap equivalent ckt. of the multiplier, used as a variable gain amplifier.

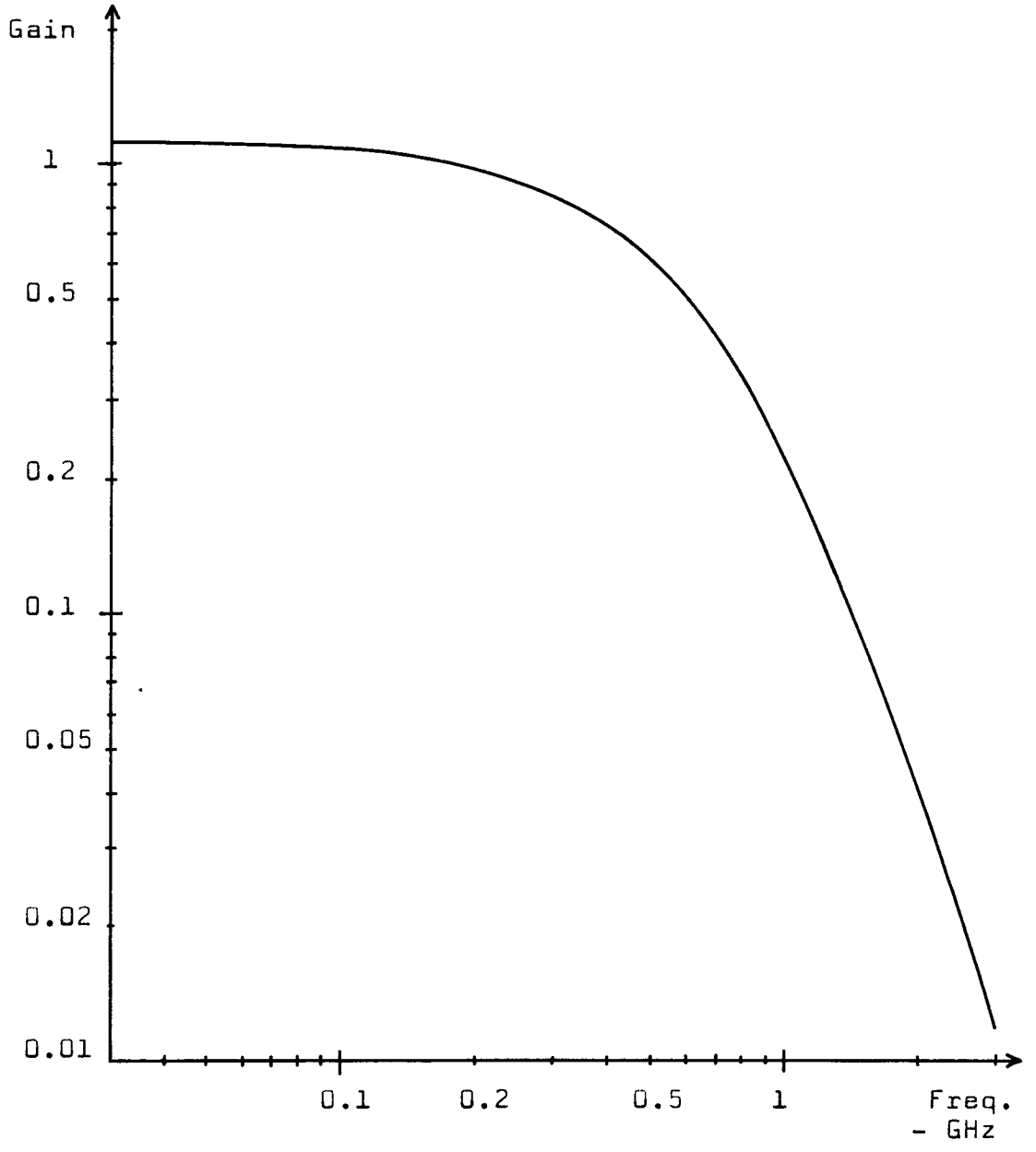


Note: There is no y-input, since the effect of the y-input is only to modulate the small signal parameters of the x-input equivalent ckt.

Resistors are in ohms.

Capacitors are in pF.

Fig. 7. Frequency response of the multiplier, calculated by means of Ecap.



Linearity.

The mathematical analysis was made under the assumption that the transistors were ideal. Several parameters deviate enough from this ideal transistor that they can cause significant non-linearities.

1. The collector admittance is not zero.
2. Non-linearities are existent in the voltage-current relationship of the inputs, caused by varying r_e in the input transistors.
3. There are bulk resistances in the multiplying transistors.
4. Transistors Q_3 and Q_4 may be approaching saturation if collectors and bases are tied together (which they are in the first samples).

The collector admittances are less than one percent of the admittance of any collector load, thus any non-linearities due to small variations in collector admittances should be negligible.

The non-linearities due to variations in r_e in the inputs are similar to those encountered in regular differential amplifiers. They are significant, but can easily be predicted. Figure 8 shows how to find r_e

versus input voltage. The differential loop-current is $V/(R+r_{e1}+r_{e2})$. Since r_e is 26 mV/I_e the linearity depends on the product of R and the tailcurrent of the differential pair.

Fig. 8a. A general differential input pair.

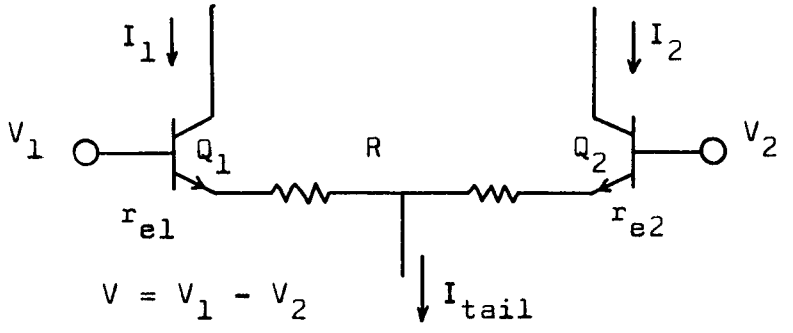
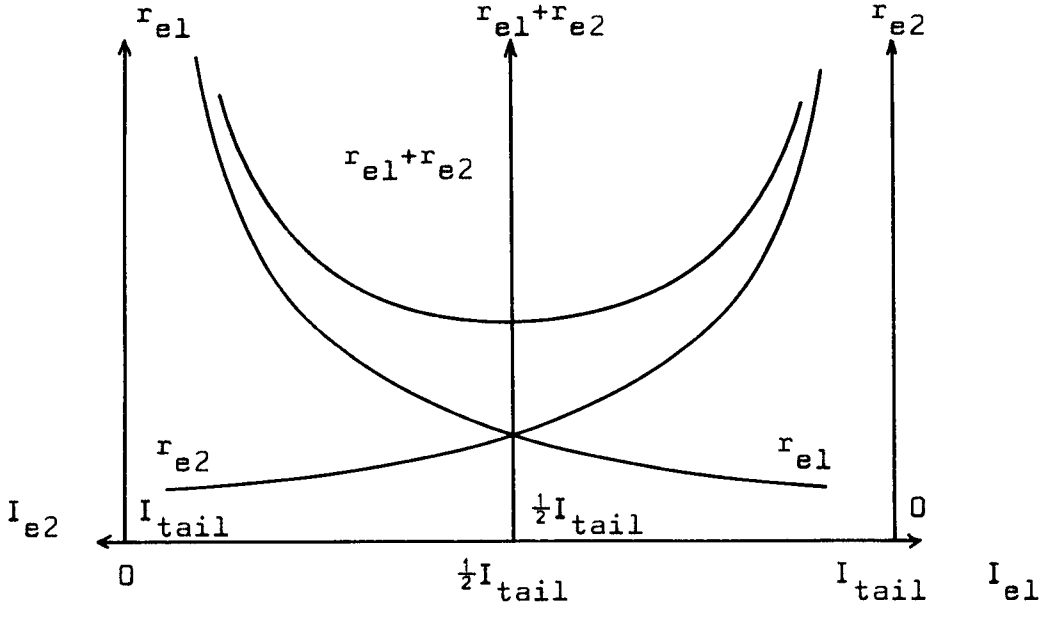


Fig. 8b. Emitter impedance in a differental pair vs. signal.



The method of Fig. 8 is used in Fig. 14 page 39 to compare measured linearity of the whole multiplier to the theoretical linearity of the differential pair alone. Figure 14 is normalized to a gain of one, and shows incremental gain over the dynamic range in % of mid-range gain. It shows that the incremental gain stays theoretically within 2 % of mid-range gain over about half the dynamic range when it is used as a variable gain amplifier with tail currents 10 mA and R = 130 ohms.

The bulk resistances in the multiplier are not very easy to deal with. The non-linearities due to bulk resistances could be calculated, but to be of any value the calculations would have to be carried out to three or four places. This would be quite elaborate, mainly due to the variable r_b parameter, and it was decided to go ahead and build the circuit without these calculations, since these calculations would not help to optimize the design. The bulk resistances are all kept as low as possible anyway.

DESIGN AND TEST OF THE INTEGRATED CIRCUIT

Choice of Transistors and Layout.

The first step in laying out an integrated circuit is usually to decide upon the geometry of the transistors. In this circuit there is no need for high currents, and consequently no need for large emitter areas. The most important property is f_T, which must be reasonably high. Besides, the capacitances must be low. This will give a high bandwidth of the circuit.

The transistor shown in Fig. 9 is frequently used in high-frequency circuits. There exist others, with higher f_T, but they are more elaborate, and unnecessary in this case. The one used has an f_T of about 0.86 GHz, which gives the multiplier a theoretical bandwidth of about 0.35 GHz.

The power swings will be reasonably small in the circuit, giving local temperature differences of only a few degrees. It should therefore be unnecessary to make the layout symmetrical, circuitwise. The most important consideration is to make all pairs of transistors as close to identical as possible, including bulk resistances in the metallization.

From the gain expression it is obvious that an accurately controlled current source is needed for I_y. It should therefore be generated externally.

The tolerances of integrated resistors are poor, but ratios of resistors usually come out quite accurate. Thus integrated resistors can be used for R_L, and either R_x or R_y. Since the tail of the y-input is external anyway, R_y is chosen to be external. The circuit is still in the experimental stage, so it will be desirable to have a variable tail current on the x-input also. Therefore part of that circuit is also left external.

The RC corner frequency of the diffused resistors is around 1 GHz, but even around that frequency and above, these resistors are useful, since the resistivity of the surrounding material is ten times higher than the average resistivity of the diffused resistors.

Fig. 9. The transistor geometry that was used in the multiplier (M 011).

Scale: $\frac{1}{2}$ inch equals 1 mil in the actual circuit.

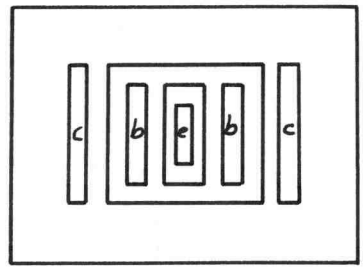
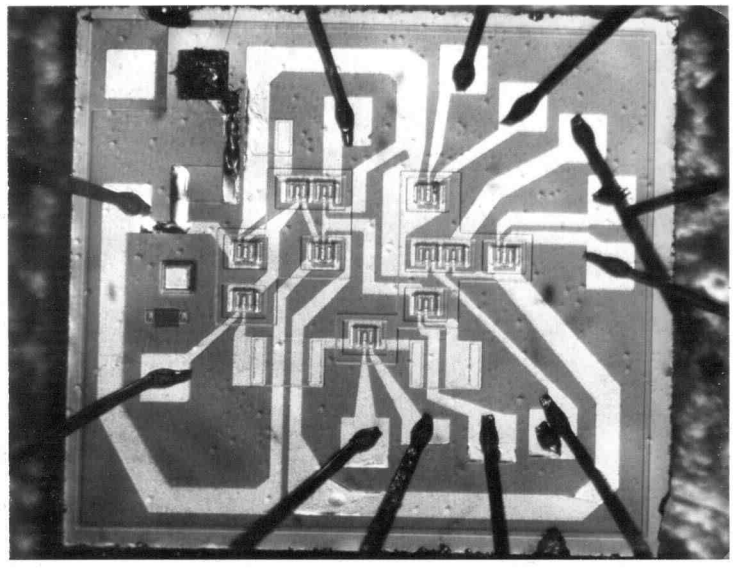


Fig. 10. The integrated layout of the multiplier.

Size: The circuit is 45 x 50 mils.



Circuit Fabrication.

The fabrication process was the double-diffused, epitaxial npn, which now is virtually standard throughout the semiconductor industry.

The substrate wafers were commercial p-type silicon, with a resistivity of 10 ohm-cm.

Buried layers are used under the collectors to reduce saturation resistance, and were put in as an n-type diffusion in the substrate. The resistivity is as low as possible so that it has insignificant resistance compared to the collector body. Next an epitaxial layer was put on, with a resistivity of 0.5 ohm-cm and a thickness 10 micrometers. It is the collector body.

At this time the various circuit components were separated by the isolation diffusion. This is a p-type diffusion, and goes through the epitaxial layer to the substrate.

The base diffusion was actually two diffusions. One is of high sheet resistivity and the other of low sheet resistivity. High resistivity is wanted in the active base area to give high beta and to give low junction capacitances, while low resistance is wanted everywhere else to minimize bulk resistance.

The emitter diffusion is very low resistivity. This is mainly to give high beta (high emitter efficiency).

Each diffusion was masked by the usual photoresist etching process, on SiO_2.

The process described above is the regular high-frequency process at Tektronix.

As a high bandwidth was expected, it was decided to mount the circuit in a 12 pin TO-5 package. This could be accomplished by tying the bases and collectors of Q_4 and Q_5 together, since only the emitter-base junction is needed. Besides, a substrate connection had to be made outside, to the can, instead of to a pin.

The TO-5 package was wanted because it has significantly less pin capacitance than any other package that was available at the time.

Measurements.

The circuit was an original development, so the main interest in measuring performance is to find out how good the circuit can be. Thus it was natural to take the measurements on the best unit in the batch, rather than to find data that is typical of all the units in the batch. Waveforms like the ones in Figs. 15-17 p. 42 were used to select the best one. The one that was finally used was

one of three or four units that were about equally good.

Bandwidth measurements are hard to make at frequencies in the hundreds of Megahertz. Several schemes were tried, and the final socket was made of copper clad fiber board. The circuit was mounted in a 12 pin TO-5 package, and the copper layer on the fiber board cut into 12 sectors with the pins soldered directly onto the sectors. Each signal pin had only a big enough sector to solder it onto. The signal inputs were then fed directly to the pins through 50 ohms coaxial cable, terminated on the pins in small 0.1 W resistors. The outputs had nothing connected to them. They were provided with copper sectors barely big enough to place the probes on. The measurements were made with a "Vector" voltmeter. It has an input im impedance in the megohms, and the probe tips have a very low capacitance. Thus the measurements were made under practically no load conditions.

When evaluating the DC linearity of the multiplier, a DVM was used for the output measurements. The two inputs were accurate reference power supplies, where each voltage could be set with dial switches rather than adjusted and measured. The tail currents were 16 mA for the x-tail and 4 mA for the y-tail in the AC measurements, and 10 mA in each tail for the DC measurements. The tails were transistor collectors to

give good common mode rejection. The values 16 mA and 4 mA were chosen for the bandwidth measurements because f_T falls off rapidly at currents below 3-4 mA in any one transistor. This insured that each signal transistor had at least 4 mA standing current in it. In the linearity measurements it was decided to make the tail currents 10 mA each, in order to keep the non-linearities due to variations in r_e equal in the two inputs, x and y. See Fig. 8 page 24. The total current should not exceed 20 mA due to power limitations.

EXPERIMENTAL RESULTS

Bandwidth.

The bandwidth measurements are shown in Fig. 11 as gain vs. frequency, and show a lower bandwidth than the predicted 0.35 GHz. The measured bandwidth is approximately 0.2 GHz.

Large single-ended signals, uncontrolled by the y-input, came out at the highest frequencies. The output with large signals at high frequencies is the one that is close to one of the inputs. See Fig. 10 p. 28. Since the circuit has a low gain, it is very sensitive to feed-through. The remedy would be to bond the circuit in a different way, in order not to have any two signal paths next to each other.

Linearity.

The linearity measurements are given in Table 1, as output vs. inputs. The results in Table 1 are plotted in Figs. 12 and 13 as output vs. one input with the other input as a parameter, Fig. 12 using y as a parameter and Fig. 13 using x as parameter.

Fig. 11. Measured frequency response of the multiplier, used as a variable gain amplifier.

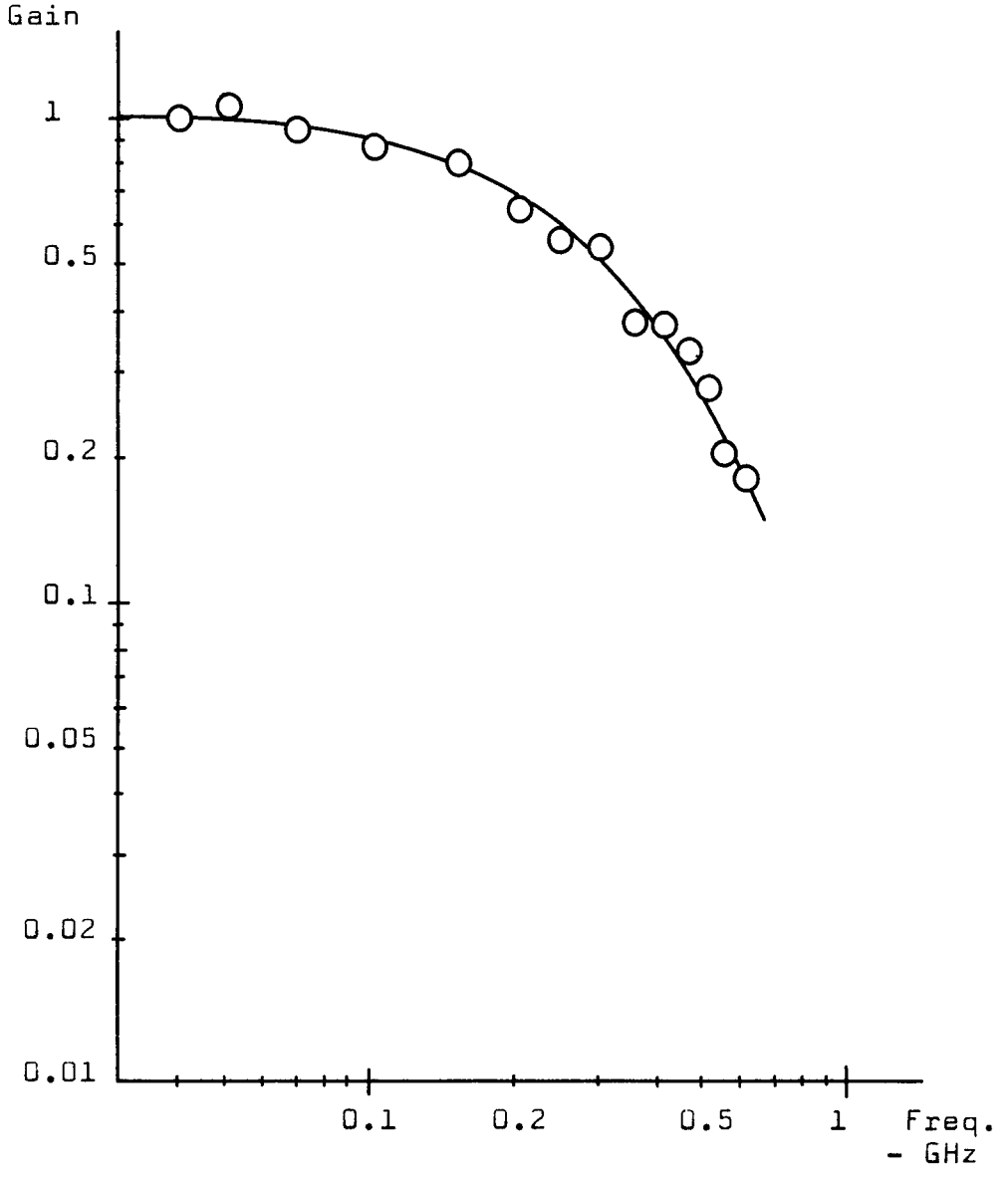


Fig. 14 shows normalized incremental gain of the two inputs compared to that of the differential pair alone. The ideal here would be to have a horizontal line of constant incremental gain over the range.

It appears that the linearity of the x-input is close to that of the differential pair alone, and therefore mainly limited by this. The y-input, however, has additional non-linearities. The most likely cause of these non-linearities is saturation of transistors Q_3 and Q_4 in Fig. 2. The saturation resistance is around 50 ohms. At an input signal of 450 mV the loop current in the input is about 450 mV/140 ohms = 3.2 mA. This plus the bias current of 5 mA adds up to 8.2 mA on the + side, which gives a voltage of 410 mV across the saturation resistance. This is right around the area where the transistor may start going into saturation, and it would thus explain why the y-input is non-linear. The remedy here would be to have the chip bonded in a package that had enough pins to give bases and collectors of Q_3 and Q_4 different pins, so they could be separated in voltage, thus staying well out of saturation.

Table 1. Measured output for various input voltages.

All numbers are in millivolts.

Inputs x	Inputs y	Output	Inputs x	Inputs y	Output
0	0	-13	0	400	- 1.21
100		-17	100		+57.74
200		-22.1	200		116.68
300		-26.38	300		175.58
400		-30.46	400		233.93
500		-34.16	500		291.35
600		-37.04	600		346.24
700		-37.14	700		395.98
0	100	- 8.68	0	500	- 0.66
100		+ 2.66	100		+73.15
200			200		146.90
300		25.69	300		220.25
400		37.44	400		292.82
500		49.36	500		363.74
600		61.42	600		431.36
700		74.43	700		491.66
0	200	- 5.18	0	600	- 0.65
100		+22.16	100		+86.40
200			200		173.32
300		77.18	300		259.57
400		104.81	400		344.76
500		132.32	500		427.76
600		159.27	600		506.62
700		185.14	700		576.48
0	300	- 2.75	0	700	- 0.89
100		+40.58	100		+96.77
200		84.0	200		194.27
300		127.38	300		291.01
400		170.62	400		386.45
500		213.37	500		479.40
600		254.69	600		567.66
700		292.90	700		645.56

Note: The 0.2 V setting on the x-input was intermittent.

Fig. 12. Measured output in Table 1, shown as output voltage vs. x-input voltage, with y-input voltage as parameter.

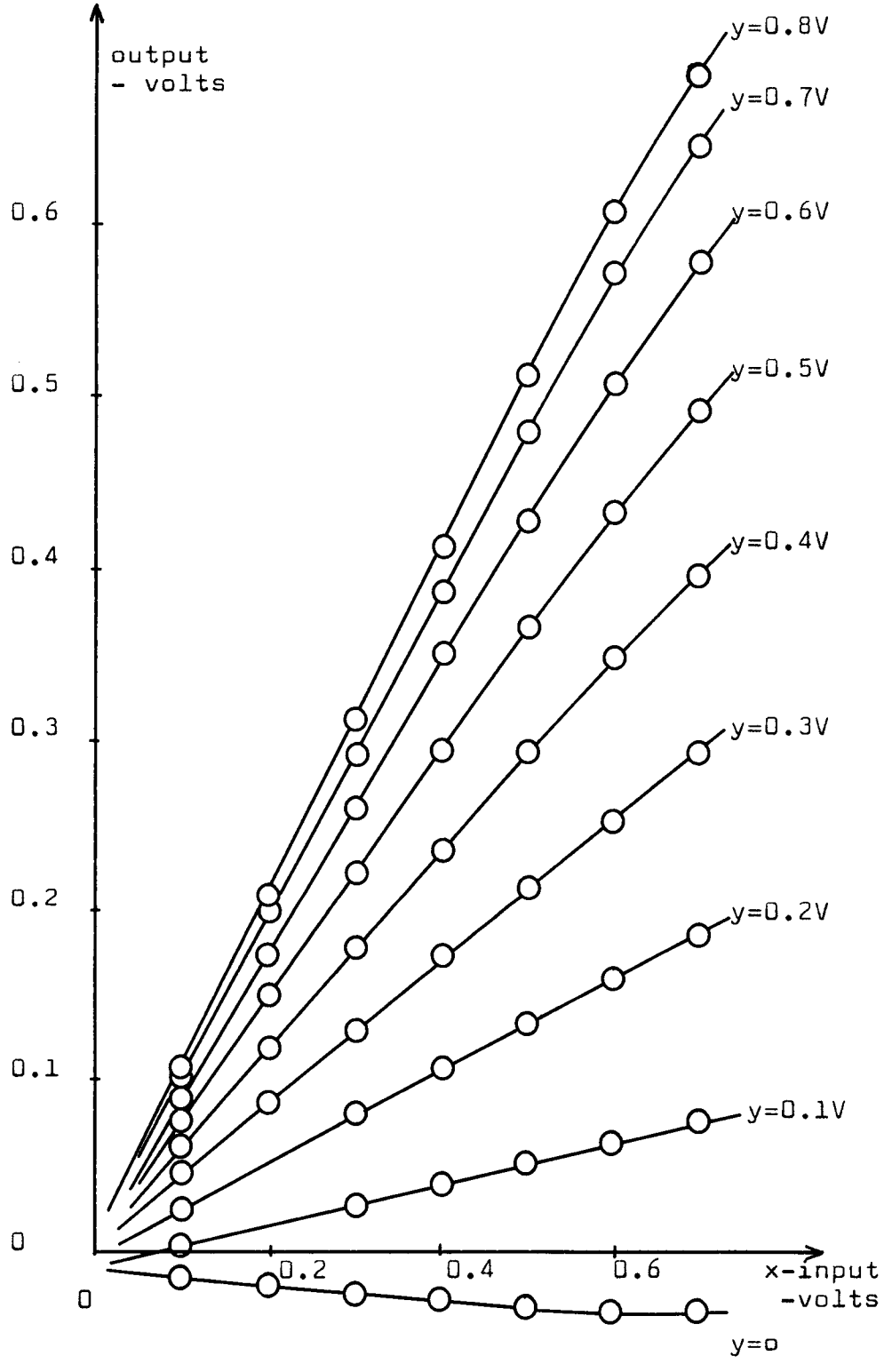


Fig. 13. Measured output in Table 1, shown as output voltage vs. y-input voltage, with x-input voltage as parameter.

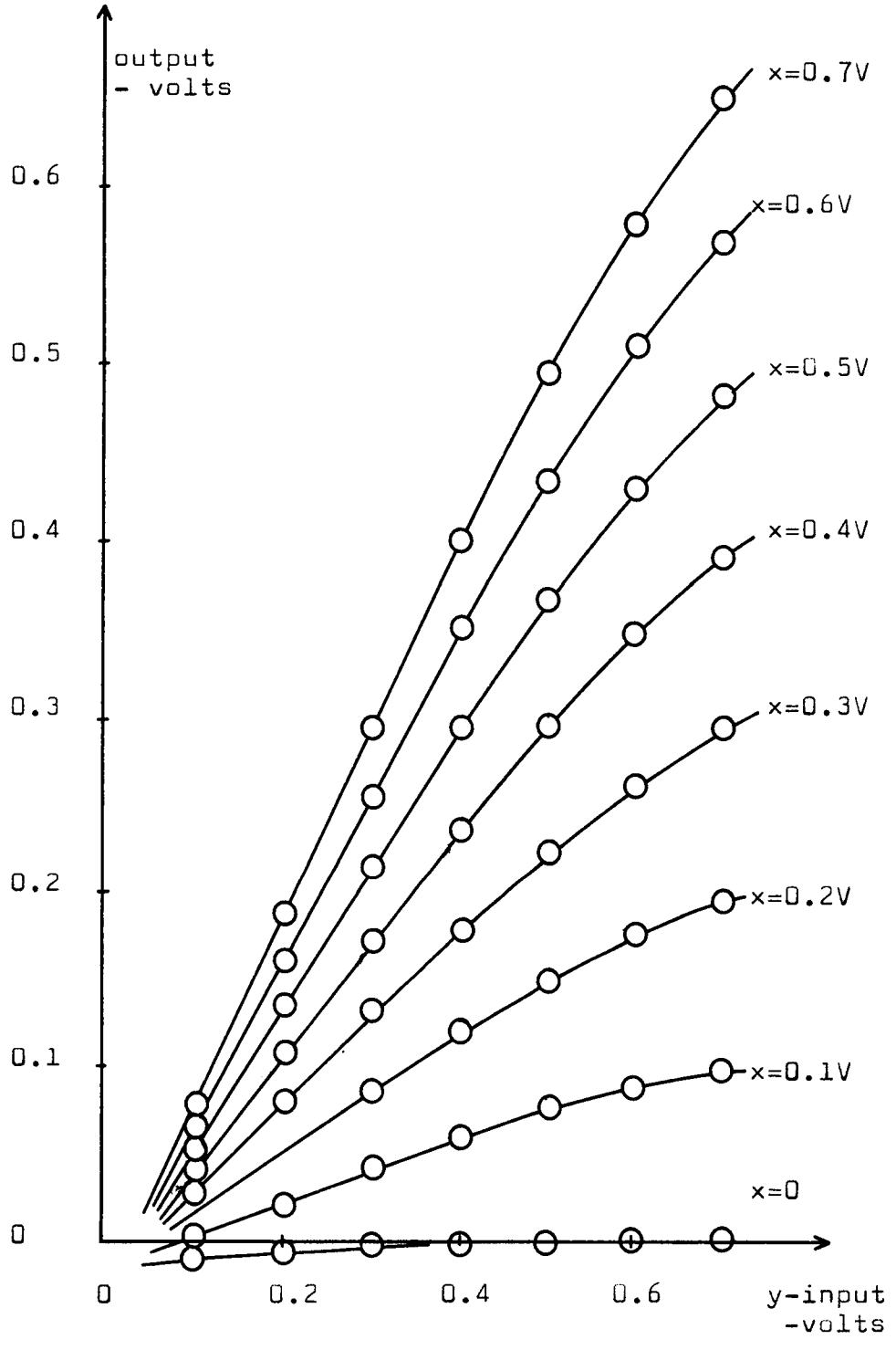
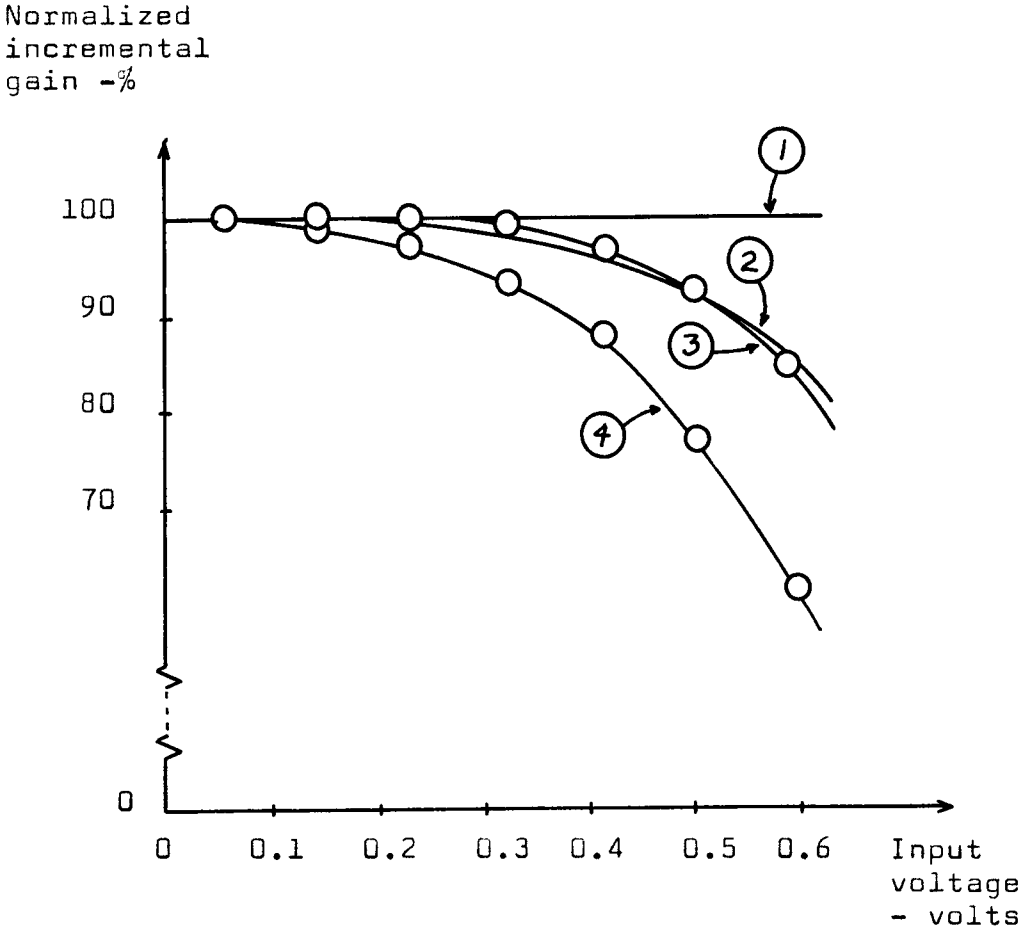


Fig. 14. Incremental gain vs. input voltage, shown in % of incremental gain at zero input voltage.

1. Ideal. Incremental gain is constant.
2. Theoretical gain of a differential pair alone, like the one in Fig. 8,p.24, with tailcurrent 10 mA and R = 130 ohms.
3. Measured for y= 0.4 V. Variable input is x.
4. Measured for x = 0.4 V. Variable input is y.



Gain.

As a check on the expression that was derived for gain on page 12, the data in Table 1 page 36 was used. Inputs x = y = 0.4 V were chosen arbitrarily as midrange values. Measured output was 233.93 mV.

With these inputs the 10 mA tail currents divide approximately as 8 mA and 2 mA in the input transistors. The emitter impedances 26/8 and 26/2 ohms are to be added in series with the two 130 ohms resistors R_x and R_y.

$$\frac{26}{8} + \frac{26}{2} + 130 = 146 \text{ ohms.}$$

$$V = \frac{2 \times 160 \times 0.4 \times 0.4 \times 0.975 \times 0.975}{146 \times 146 \times 10 \times (10^{-3})} = \underline{228.5 \text{ mV}}$$

There are still some factors that were not considered above. The ratio R_L/R_x may be off a couple of percent, but more important are the zero offsets on the inputs. These are apparent in Figs. 12 and 13, and looking at the curves for x=0 and y=0, it appears that these off-sets give output errors of the form (a+f(x))(b+f(y)), where a and b are constants. Keeping this in mind, it can still be said that the calculated output voltage is close to the measured value.

Useful Range.

With maximum DC voltage on the y-input, and a 1 KHz sinewave with variable magnitude on the x-input, the maximum output was 1.3 V p-p. The minimum useful output was limited by the noise, in this mode of operation. The noise was about 0.1 mV p-p on the output, independent of input signal. This was measured with a 1A7 plug-in in a 547 Tektronix Oscilloscope, giving a bandwidth of DC to 500 KHz, in setting the 1A7 at maximum bandwidth. Since this was only a very little part of the useful bandwidth of the multiplier, another measurement was made with a HP 3400A voltmeter, which read a noise level of 1.5 mV rms, up to about 10 MHz.

Next, the 1 KHz sinewave on the x-input was left constant with a magnitude that almost saturated the input. The maximum DC input on y was 0.45 V. The minimum input on y to regulate the gain down was determined by how much distortion could be tolerated. When the y-input was 0.002 volts, the second harmonic of the output was of approximately the same magnitude as the first harmonic. From this, the useful range can be estimated, depending on how much distortion can be tolerated. The second harmonic seems to be a feed-through, independent of gain. It is 45-50 db below maximum signal level.

Examples of Product Waveforms.

Shown below are examples of the multiplier outputs for various input waveforms. All pictures are taken with a horizontal scale of 1 msec/div. Where a sinewave is used, the input frequency is 1 KHz.

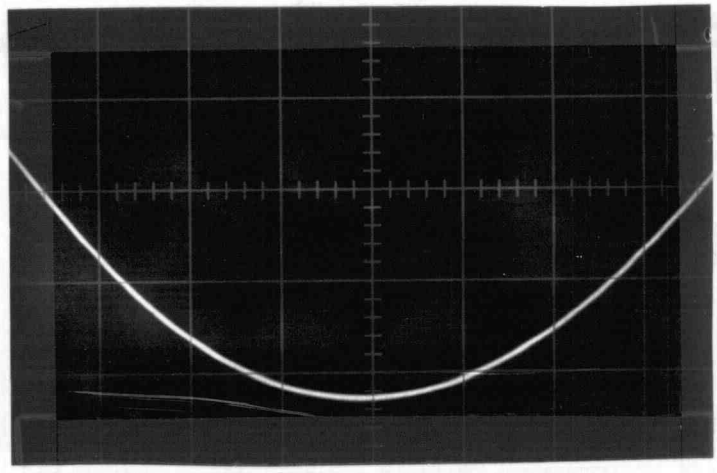


Fig. 15.
ramp x ramp
= parabola.

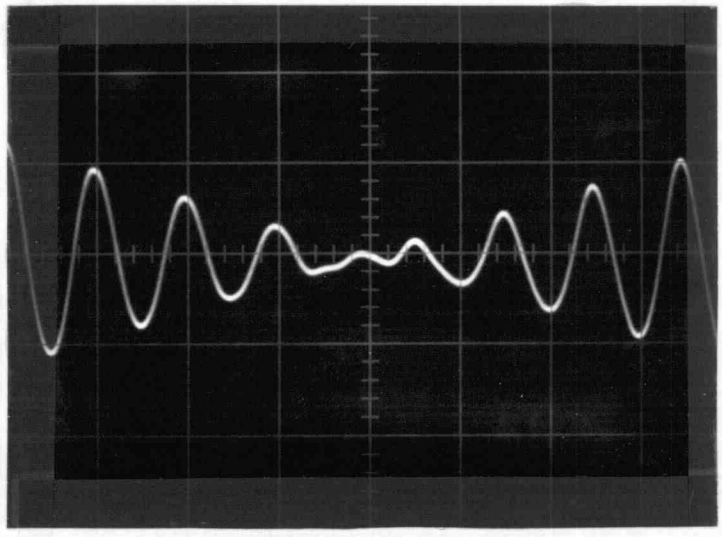


Fig. 16.
ramp x sinewave
= sinewave with
ramp envelope.
note phase
invertion.

Fig. 17.

(sinewave)^2

= sinewave of

double frequency.

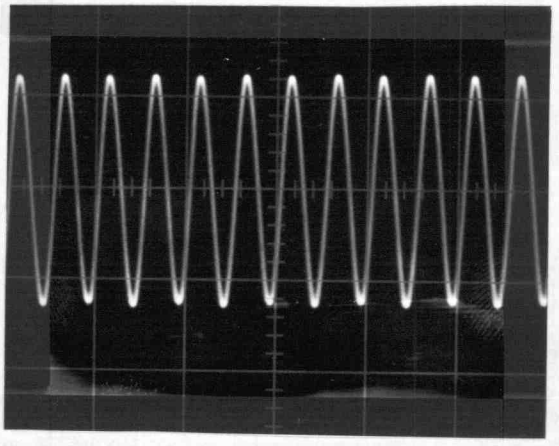


Fig. 18.

squarewave x ramp

= squarewave with

ramp envelope.

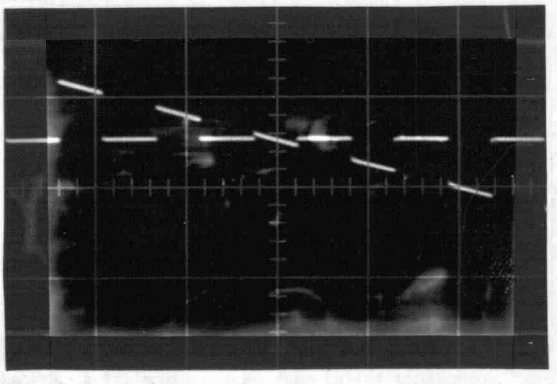
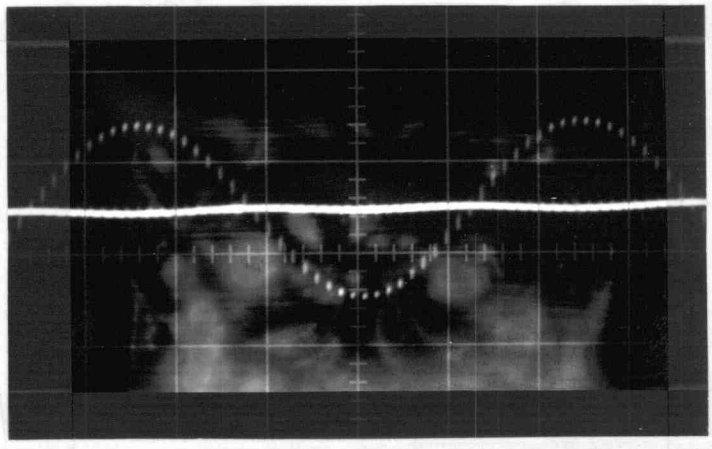


Fig. 19.

sinewave x pulses

= pulses with

sinewave envelope.



CONCLUSIONS

Performance.

Bandwidth:

Theoretical 0.35 GHz

Measured 0.2 GHz

Linearity:

Theoretically 2% half range each input.

Measured 2% half range x-input

7% half range y-input

Scalefactor:

Theoretical output for 0.4 volt inputs 228.5 mV

Measured output for the same inputs 233.93 mV

Range:

Noise is up to 80 db below maximum output, depending on bandwidth of following stages.

Second harmonic (constant feedthrough ?) is 45-50 db below maximum output.

Usefulness.

It can be concluded that the multiplier is functioning. The bandwidth is higher than that of most types of multipliers. It can be made even higher by using faster transistors, if necessary.

The accuracy is less than that required in a general purpose analog computer, but for many special purpose analog computations in different kinds of systems it is undoubtedly useful. One might here mention the possibility of using the circuit as an AM modulator. It will produce a double sideband modulation, with carrier and/or baseband optional, depending on whether a DC component is added to the signal or carrier.

It can also be used as a variable gain amplifier, although for minor gain variations the simpler circuit in Fig. 1a p. 3 can be used, with I_3 and I_4 driving the output, and I_z and I_y being variable current longtails.

Suggestions for further work.

For future production of the multiplier it will be necessary to find a package that has more than 12 pins, and still has low pin capacitance. The available flatpacks have enough pins, but have higher capacitance

on the pins, decreasing the bandwidth. Of course, for low frequency applications this would not matter much. With at least 13 pins, the collectors of Q_3 and Q_4 can be biased at higher voltages than the bases, and thereby stay well out of saturation.

Another problem that will have to be corrected is the pin configuration that has an input and an output right next to each other, causing feed-through at very high frequencies. If one had a 14 pin package, one could simply leave a grounded pin between the two that now are too close.

The only other obvious improvement is that one should continue to decrease the bulk resistances in Q_1 through Q_4, to make the linearity better.

The bandwidth can be increased some if necessary, by using faster transistors, but not very much without mounting the whole chip in waveguides. One GHz seems to be an empirical limit for regular wired circuits.

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