Full In-Circuit Emulation for F8, 3870, 3872, 8080A, TMS9900, 6800, Z80A, 1802, 8085A, 6802 Real-Time Prototype Analyzer, Line Printer **Microprocessor Development Labs** Text Editor, Modular Development Language Debugging Software, Line Display Terminal Macro Relocatable Assemblers Full In-Circuit

MDL Now Supports

8085A	6800
8080A	6802
8048	F8
8049	3870
8035	3872
8039	Z-80A
8039-6	TMS9900
8021	1802

. . . with more to come.

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8002A | Microprocessor Development Lab

A Complete Microprocessor/Microcomputer Development System

Multiple Microprocessor Support

In-Circuit Emulation

Real-Time Prototype Analysis

The 8002A Microprocessor Lab is a complete software development system for the design of microprocessor-based products. A key feature is its ability to support many microprocessor chips, including the Intel 8085A, 8080A, 8048, 8049, 8039, 8039-6, 8035 and 8021, Motorola 6800 and 6802, Texas Instruments TMS9900, Zilog Z-80A, Fairchild F8, RCA 1802, and the Mostek 3870 and 3872.

In addition to multiple microprocessor support, the 8002A offers a superior operating system and powerful text editor, assembler, and debugging programs; three optional levels of emulation for software debugging, partial and full emulation; and a real-time prototype analyzer option offering all the capabilities of a microprocessor analyzer with eight channels of external input.

The 8002A Microprocessor Lab consists of the 8002A Mainframe with 32K of Program Memory, and the dual flexible disc unit. Recommended optional peripherals are the CT 8101 TTY Terminal, the 4024/4025 Computer Display Terminals, or the LP 8200 Line Printer.

Software Development and Debugging

In a typical design sequence, software is developed using all the resources of TEKDOS, the disc-operating system software for the 8002A Microprocessor Lab. TEKDOS performs flexible disc and file utility functions, data transfer functions, and system/peripheral device control functions. In addition to relieving the user of these housekeeping chores, TEKDOS also supervises the text editor, assembler, and linker programs and the optional emulation support, debugging system, and PROM programming routines.

Program entry and editing may be accomplished module by module. The line-oriented text editor provides 150 60-character lines of buffer workspace, and offers several convenience features for preparing, correcting, and modifying the program quickly and easily. The macro command allows a multiple-step routine to be defined by one new command. At the end of each work session, file space is allocated by TEKDOS; duplicate files of important material may be readily created. When program entry has been completed, all program files may be merged with a single TEKDOS command.

The assembler processor, with the appropriate disc inserted in the flexible disc drive, performs program assembly functions for each microprocessor supported by the 8002A.

The powerful macro capability allows the designer to access frequently used sets of code by referencing the macro by name. The linker, working with the relocating features of the Assembler, links and locates multiple code segments into a complete executable program. Additionally, the conditional assembler capability of the 8002A allows the designer to customize the final program by testing conditions to determine which of certain code segments are to be assembled into the final program. Code management is further enhanced by the Assembler's versatile string handling capability. Extension English language diagnostics of the 8002A provide easy to understand error messages and locate the line in which the error has occured. When assembly is completed, the assembled object code is stored on disc in a newly created binary format file.

After an error-free assembly listing has been obtained, the resulting object code may be executed in system emulation mode 0 on the optional emulator processor. The emulator processor is identical to the microprocessor that will finally be installed in the user's prototype. Execution is performed under control of the debug system; during execution, program steps can be traced, software breakpoints can be set, and memory can be examined and changed as required. Should an error be discovered, that portion of the program can be corrected at the source level using the text editor. It can then be reassembled and executed again. This procedure continues until the program is correct.

Partial and Full Emulation

After the software has been debugged, it may be exercised on the prototype circuitry in the partial emulation mode (mode 1). During partial emulation, control may be released from the 8002A to the prototype in stages. The developmental software runs using 8002A memory space and prototype I/O and clock. The 8002A memory mapping feature allows memory to be gradually mapped over to the prototype in 128-byte address blocks. Throughout partial emulation, the user has access to prototype circuitry through the debugging system, which enables him, as before, to trace, set breakpoints, examine and change memory and register contents.

In full emulation (mode 2) the program is run on the prototype, but program execution is still under the complete control of the debug system. All I/O and timing functions are directed by the prototype; all memory has been mapped over to the prototype; and only the prototype control probe is still in place, emulating the target microprocessor. Although the prototype is effectively free-standing, then, the user may still direct program activity from the 8002A.

8002A CHARACTERISTICS

The 8002A Microprocessor Lab is a modular system whose mainframe houses up to 20 plug-in circuit boards. A terminal is necessary for system operation, and may be ordered as an optional peripheral.

The Real-Time Prototype Analyzer module, additional 16K byte Program Memory modules (Standard Program Memory consists of 32k bytes of RAM), and PROM Programmer modules for the 1702 or 2704/2708 are available as system options.

In addition to the standard system console I/O port, the 8002A provides a system communication module with three RS-232-C compatible ports for use with such peripherals as paper tape reader/punchers, line printers (LP8200), printing terminals (CT 8101) modems and other peripherals. One port is designated a general purpose RS-232-C compatible-input/output port with independent input and output baud rate selection. Another port is an RS-232-C compatable-output-only port for use with line printers. The third port is a modem-compatible port for use with half duplex modems. All ports have strap selectable baud rates of 110, 300, 600, 1200, or 2400.

8002A PHYSICAL CHARACTERISTICS

Dimensions	in	cm
Height	9.6	24.7
Width	18.8	48.3
Length	22.3	57.3
Weight	**lb**	**kg**
Net	66	30

8002A ENVIRONMENTAL CHARACTERISTICS

Temperature	
Operating	0°C to +35°C (+32°F to 95°F).
Storage	Not available.
Humidity	To 90° relative noncondensing.
Altitude	
Operating	To 15,000 ft max.
Storage	To 50,000 ft max.

8002A ELECTRICAL CHARACTERISTICS

Ac Input Voltages	115 V ac ±10% or 230 V ac ±10%.
Frequency Range	60 Hz (50 Hz special order).

8002A DUAL FLEXIBLE DISC CHARACTERISTICS

Flexible Disc Unit — The Flexible Disc Unit consists of two disc drives, a controller, and power supplies. The two disc drives are designated as drive 0 and drive 1. Drive 0 is the default system drive. System programs are placed in this drive, including disc-operating system programs, the text editor, and the debugging routines peculiar to a specific emulator processor. Drive 1 may be used for storing user files, for modifying user files, or as a scratch data area. Drive 0 or drive 1 may be designated as the system drive.

Disc Organization — Each disc contains 77 concentric tracks. Each quarter track, or block, is split into eight sectors, and each sector can contain 128 bytes. Due to directory limitations, a maximum of 72 files can be contained on one disc. The disc-operating system reserves track 0 for the disc directory; tracks one through four are normally automatically reserved for system programs.

Write Protection — Each disc has a write-protect slot. If the slot is covered, the disc is write-enabled; if the slot is not covered, the disc is write-protected. If an attempt is made to write to a write-protected disc, an error message will be displayed on the appropriate peripheral.

ENVIRONMENTAL CHARACTERISTICS

Temperature	
Operating	+10°C to 35°C (+50°F to 95°F).
Humidity	
Operating	To 90% relative noncondensing.
Altitude	
Operating	To 15,000 feet max.
Storage	To 50,000 feet max.

PHYSICAL CHARACTERISTICS

Size	**in**	**cm**
Height	10.5	27
Width	17.5	44
Length	23.6	60
Weight	**lb**	**kg**
Net	85	38.6

ELECTRICAL CHARACTERISTICS

Line Voltages	Voltage	Current
	115 V ac±10 at 60 Hz	3.5 A
	230 V ac ±10 at 50 Hz	2.0 A
Line Frequency	at 60 Hz (50 Hz special order)	

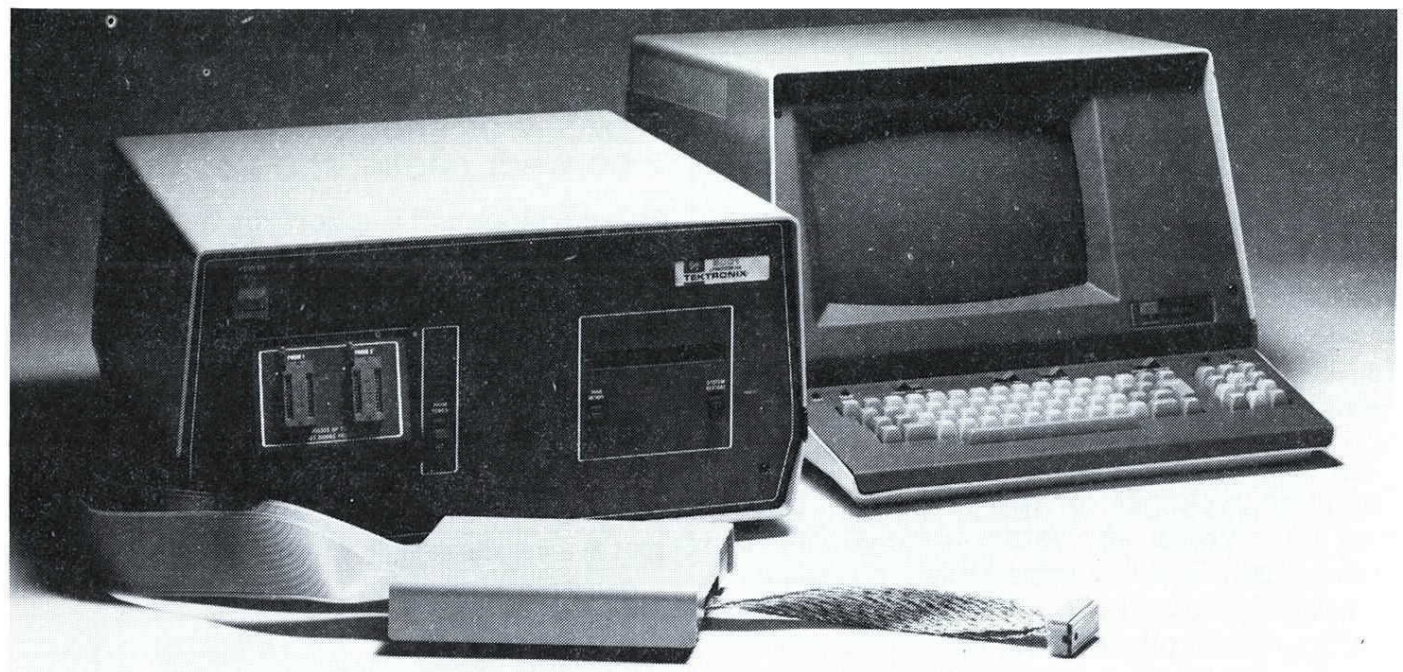
DISC UNIT CHARACTERISTICS

Capacity		**Bits**	**Bytes**
Per Disc	77 x 32 x 128 x 8 bits =	2,523,136	315,392
Per Track	32 x 128 x 8 bits =	32,768	4,096
Per Sector	128 x 8 bits =	1,204	128
Access Time	10 ms/track		

ORDERING INFORMATION

8002A Microprocessor Lab $10,950
****Option 45 32K Program Memory Module . . . +$3100**
****Option 49 16K Program Memory Module . . . +$1550**

*8002A Standard Program Memory consists of 32K bytes of RAM.



The 8001 Microprocessor Lab consists of the 8001 Mainframe with 16K of Program Memory. Microprocessor Support Packages for microprocessors are optional. A Microprocessor Support Package includes an emulator ROM, an emulator processor, and a prototype control probe. The CT 8101 TTY Terminal, 4024/4025 Computer Display Terminals, or the LP8200 Line Printer are recommended optional peripherals.

Multiple Microprocessor Support
In-Circuit Emulation
Real-Time Prototype Analysis

The 8001 Microprocessor Lab is a total hardware debugging system for the design of microprocessor-based products. A key feature is its ability to support many microprocessor chips, including the Intel 8085A, 8080A, 8048, 8049, 8039, 8039-6, 8035 and 8021, Motorola 6800 and 6802, Texas Instruments TMS9900, Zilog Z-80A, Fairchild F8, RCA 1802 and the Mostek 3870 and 3872.

In addition to multiple microprocessor support, the 8001 offers three emulation modes for software debugging, partial and full emulation, as well as a real-time prototype analyzer option offering all the capabilities of a microprocessor analyzer with eight channels of external input.

Three Emulation Modes

In a typical design sequence, software is first developed independently using time-sharing, a minicomputer, another development system, or some other means. It is then downloaded to the 8001 using the Tektronix Hexidecimal File Format to insure accurate transfer of the program. At this point the in-prototype emulation and software/hardware integration capabilities of the 8001 come into play.

After the developed software is downloaded to the 8001, the resulting object code may be executed in system emulation mode 0 on the optional emulator processor. The emulator processor is identical to the microprocessor that will finally be installed in the user's prototype. Execution is performed under control of the debug system; during execution, program steps can be traced, software breakpoints can be set, and memory can be examined and changed as required. Should an error be discovered, that portion of the program can be corrected at the source level using the editing, assembling and linking feature of the host computer. This continues until the program is correct.

Partial emulation mode 1 lets the user release control in methodical steps from the 8001 to the prototype. The developmental software runs using 8001 memory space, prototype I/O and clock. The 8001 memory mapping feature allows memory to be gradually mapped over to the prototype in address blocks as small as 128 bytes. Throughout partial emulation, the user has access to prototype circuitry via the powerful 8001 debugging system, which enables him to trace, set breakpoints, examine and change memory and register contents.

Full emulation mode 2 lets the user exercise the program on the prototype while still maintaining complete control through the Microprocessor Lab. All I/O and timing functions are directed by the prototype; all memory has been mapped over to the prototype; and only the prototype control probe is still in place, emulating the target microprocessor. Although the prototype is effectively free-standing the user may still direct program activity through the prototype control probe.

8001 CHARACTERISTICS

The 8001 Microprocessor Lab is a modular system whose mainframe houses up to 20 plug-in circuit boards. Emulator processor modules for the microprocessor of choice, its associated prototype control probe, and a ROM-based software module are optional. A terminal is necessary for system operation, and may be ordered as an optional peripheral.

The Real-Time Prototype Analyzer module, additional 16K byte Program Memory modules, and PROM Programmer modules for the 1702 or 2704/2708 are available as system options.

In addition to the standard system console I/O port, the 8002A provides a system communication module with three RS-232-C compatible ports for use with such peripherals as paper tape reader/punchers, line printers (LP8200), printing terminals (CT 8101) modems and other peripherals. One port is designated a general purpose RS-232-C compatible input/output port with independent input and output baud rate selection. Another port is an RS-232-C compatible output only port for use with line printers. The third port is a modem compatible port for use with half duplex modems. All ports have strap selectable baud rates of 110, 300, 600, 1200, or 2400.

8001 PHYSICAL CHARACTERISTICS

Dimensions	**in**	**cm**
Height	9.6	24.7
Width	18.8	48.3
Length	22.3	57.3
Weight	**lb**	**kg**
Net	66	30

8001 ENVIRONMENTAL CHARACTERISTICS

Temperature	
Operating	0°C to +35°C (+32°F to 95°F).
Humidity	To 90° relative noncondensing.
Altitude	
Operating	To 15,000 feet max.

8001 ELECTRICAL CHARACTERISTICS

Ac Input Voltages	115 V ac ±10% or 230 V ac ±10%.
Frequency Range	60 Hz (50 Hz special order)

ORDERING INFORMATION

8001 Microprocessor Lab $4950
****Option 45 32K Program Memory Module . . . +$3100**
****Option 49 16K Program Memory Module . . . +$1550**
(**8001 Standard Program Memory consists of 16K bytes of RAM.)

Emulator Processor and Prototype Control Probe Support Packages

The 8002A and 8001 Microprocessor Development Labs support a wide variety of different microprocessors and microcomputers.

Emulators are currently available for the Intel 8080A, 8085A, 8048, 8049, 8039, 8039-6, 8035 and 8021, Motorola 6800 and 6802, Texas Instruments TMS9900, Zilog Z-80A, Fairchild F8, RCA 1802 and the Mostek 3870 and 3872.

Emulator packages for the 8002A and 8001 may be ordered as system options. These options provide the capabilities necessary to fully emulate the target microprocessor in a user's prototype system.

The emulator processor, which resides on a plug-in circuit module along with controlling logic circuitry, enables the user to execute and debug the program on a microprocessor identical to the one which will be used in the prototype, while giving him access to the full 64K bytes of Microprocessor Lab program memory.

The prototype control probe, which links the emulator processor to the prototype system, allows partial and full in-circuit emulation.

All emulation operations are controlled by the powerful Microprocessor Lab system software. The user is able to monitor program execution, set software breakpoints, examine and change memory and register contents. Debug trace information is displayed in a format unique to the microprocessor, with instruction fetches disassembled into mnemonics for easy interpretation.

F8, 3870, 3872 EMULATOR SUPPORT PACKAGE CHARACTERISTICS

F8 refers to microprocessors manufactured by Fairchild's Corporation; the 3870 and 3872 refer to microcomputers manufactured by Mostek Corporation. Tektronix, Inc., does not guarantee that other vendor's versions of the F8, 3870, or 3872 will be compatible with the TEKTRONIX Microprocessor Labs.

PHYSICAL CHARACTERISTICS

Length 6 ft (1.8 m) of cable from emulator processor to the interface assembly. 1 ft (30 cm) of cable from the interface to 40 pin plug.

Cable Configuration

6 ft (1.8 m) — Two 40-conductor ribbon cables with chassis ground plane and signal paths.

1 ft (30 cm) — Two 40-conductor twisted pair cables.

Termination

6 ft (1.8 m) — The interface assembly contains receivers for data, address, and control from the F8/3870/3872 Emulator Processor module.

1 ft (30 cm)—Not terminated.

TIMING CHARACTERISTICS

3870/3872—The 3870/3872 Prototype Control Probe was designed to meet all the ac characteristics of the 3870 and 3872 Microcomputers.

F8 (3850)—The F8 Prototype Control Probe meets all of the F8 ac characteristics with the following exceptions: (1) the worst-case delay from the falling edges of WRITE to the ROMC lines being valid is 650 ns (compared to 550 ns for the F8 CPU); (2) the worst-case skew between an external clock input is 0 to 90 ns longer than that specified for the F8.

NEW

8048, 8049, 8039, 8039-6, 8035 AND 8021 EMULATOR PROCESSOR, PROTOTYPE CONTROL PROBE, AND 8021 ADAPTER

Full development support for the MCS 8048 family is now available for the 8002A/8001 Microprocessor Development Labs. Contact your local MDL specialist for detailed specifications.

ORDERING INFORMATION

Option Description	Factory Price	Field Number	Field Price
8001 Microprocessor Lab	$4950		
Opt. 09 8048 Emulator ROM and Emulator Processor Support (Prototype Control Probe required Opt. 10)	+$3110	8001F09	$3160
Opt. 10 8048 Prototype Control Probe	+$1190	8001F10	$1290
Opt. 11 8021 Prototype Control Probe Adapter (requires Opts. 09 and 10)	+$ 295	8001F11	$ 345

ORDERING INFORMATION

Option Description	Factory Price	Field Number	Field Price
8002A Microprocessor Lab	$10,950		
Opt. 08 8048/8021 Assembler Software Support	+$ 850	8002F08	$ 900
Opt. 23 8048/8021 Emulator Support (Prototype Control Probe Required)	+$2350	8002F23	$2450
Opt. 40 8048 Prototype Control Probe	+$1190	8002F40	$1290
Opt. 41 8021 Prototype Control Probe Adapter (requires Opt. 40)	+$ 295	8002F41	$ 345

ORDERING INFORMATION

Option Description	Factory Price	Field Number	Field Price
8001 Microprocessor Lab	$4950		
Option 06 3870/3872 Microcomputer Support Package	+$4600	8001F06	$4650
Option 07 F8 Microprocessor Support Package	+$4600	8001F07	$4650
8002A Microprocessor Lab	$10,950		
Option 06 F8/3870/3872 Assembler Software Support	+$ 850	8002F06	$ 900
Option 21 F8/3870/3872 Emulator Support	+$2850	8002F21	$2950
Option 36 3870/3872 Prototype Control Probe	+$ 990	8002F36	$1090
Option 37 F8 Prototype Control Probe	+$ 990	8002F37	$1090

8080A EMULATOR SUPPORT PACKAGE CHARACTERISTICS

8080 and 8080A refer to microprocessors manufactured by Intel Corporation. Tektronix, Inc., does not guarantee that other vendors' versions of the 8080 will be compatible with the TEKTRONIX Microprocessor Labs.

PHYSICAL CHARACTERISTICS

Length 6 ft (1.8 m) of cable from the emulator processor to the interface assembly.

1.5 ft. (45.8 cm) of cable from the interface assembly to the 40 pin plug.

Cable Configuration

6 ft (1.8 m) — 2 40-conductor ribbon cables with alternating ground and signal paths.

1.5 ft (45.8 cm) — 2 twisted pair 40 conductor cables.

Termination

6 ft (1.8 m) — The interface assembly contains resistive termination and receivers for data, address, and control from the emulator processor module.

1.5 ft (45.8 cm) — Not terminated.

40 pin plug—40 pin spring plate protected plug. When used with a zero insertion force socket, an included 40 pin low profile DIP socket must be used between the zero insertion force socket and the 40 pin probe plug.

TIMING CHARACTERISTICS

Emulation Interface Delays*

To 8080A from Interface Assembly	Typ	Max (in ns)
ø1	44	60
ø2	44	60
HOLD	44	67
RESET	44	67
RDY**	35	40
INT	63	104
DATA	44	53

From 8080A to Interface Assembly	Typ	Max (in ns)
HOLDA***	39	55
SYNC	37	45
WAIT	37	45
WR	37	45
DBIN	37	45
INTE	39	55
ADDRESS	27	35
DATA	50	63

**Assumes 6 ft of cable at 1.5 ns/ft.*

***RDY is ignored unless user memory or I/O is accessed in control mode 2 or special mode.*

****The equation for HOLDA to tristate timing is as follows: HOLDA • DBIN = FLOAT. Tristate of data and address follows the trailing edges of DBIN or WR by approximately 20 ns.*

ORDERING INFORMATION

Option Description	Factory Price	Field Number	Field Price
8001 Microprocessor Lab	$4950		
Option 01 8080A Microprocessor Support Package	+$4100	8001F01	$4150
8002A Microprocessor Lab	$10,950		
Option 01 8080A Assembler Software Support	+$ 850	8002F01	$ 900
Option 16 8080A Emulator Support	+$2350	8002F16	$2450
Option 31 8080A Prototype Control Probe	+$ 990	8002F31	$1090

6800/6802 EMULATOR SUPPORT PACKAGE CHARACTERISTICS

6800 and 6802 refer to microprocessors manufactured by Motorola Corporation. Tektronix, Inc., does not guarantee that other vendors' versions of the 6800 or 6802 will be compatible with the TEKTRONIX Microprocessor Labs.

PHYSICAL CHARACTERISTICS

Length 6 ft (1.8 m) of cable from the emulator processor to the interface assembly.

1 ft (30 cm) of cable from the interface assembly to the 40 pin plug.

Cable Configuration

6 ft (1.8 m) — 2 40-conductor ribbon cables with alternating ground and signal paths.

1 ft (30 cm) — 2 twisted pair 40 conductor cables made up of signal/ground pairs.

6800 PROTOTYPE CONTROL PROBE

Read/Write Timing (in ns)

Characteristic	Symbol	Min	Typ	Max
Peripheral Read Access Time	^{D}TACC			506
Address Setup Time	^{D}TAD			350
R/W Setup Time	^{D}R/WSU			375
VMA Setup Time	^{D}EVMA			365
Data Setup Time (Read)	^{D}TDDR	119		
Data Delay Time (Write) (relative to 01↑)	^{T}DDW			513
Delay for DBE Rising Edge (relative to 01↑)	^{D}DBER			444
Input Data Hold Time	^{D}HRD	29		
Output Data Hold Time (after 01↑)	^{D}TDWH	40**	10	
Output Data Hold Time (after DBE↓)	^{D}TDWH	20		
Address Hold Time	^{D}ADH	65		
VMA Hold Time	^{D}VMAH	68		
R/W Hold Time	^{D}R/WH	61		

6802 PROTOTYPE CONTROL PROBE

Read/Write Timing (in ns)

Characteristic	Symbol	Min	Typ	Max
Peripheral Read Access Time	^{D}TACC			480
Address Setup Time	^{D}TAD			367
VMA Setup Time	^{D}EVMA			373
R/W Setup Time	^{D}R/WSU			392
Data Setup Time (Read)	^{D}TDDR	127		
Data Delay Time (Write)	^{T}DDW			527
Input Data Hold Time	^{D}HRD	40**	10	
Output Data Hold Time	^{D}TDWH	39		
Address Hold Time	^{D}ADH	63		
VMA Hold Time	^{D}VMAH	66		
R/W Hold Time	^{D}R/WH	70		

**Although data should remain valid at least 40 ns after Enable, typically 10 ns will be sufficient.

ORDERING INFORMATION

Option Description	Factory Price	Field Number	Field Price
8001 Microprocessor Lab	**$4950**		
Option 02 6800 Microprocessor Support Package	**+$4100**	**8001F02**	**$4150**
Option 2A 6802 Prototype Control Probe	**+$ 990**	**8001F2A**	**$1090**
Option 2B 6802 Microprocessor Support Package	**+$4100**	**8001F2B**	**$4150**
8002A Microprocessor Lab	**$10,950**		
Option 02 6800 Assembler Software Support	**+$ 850**	**8002F02**	**$ 900**
Option 17 6800 Emulator Support	**+$2350**	**8002F17**	**$2450**
Option 32 6800 Prototype Control Probe	**+$ 990**	**8002F32**	**$1090**
Option 39 6802 Prototype Control Probe	**+$ 990**	**8002F39**	**$1090**

Z80A EMULATOR SUPPORT PACKAGE CHARACTERISTICS

Z80 and Z80A refer to microprocessors manufactured by Zilog Corporation. Tektronix, Inc., does not guarantee that other vendor's versions of the Z80 will be compatible with the TEKTRONIX Microprocessor Labs.

PHYSICAL CHARACTERISTICS

Length 6 ft (1.8 m) of cable from the emulator processort to the interface assembly.

1 ft (30 cm) of cable from the interface assembly to the 40 pin plug.

Cable Configuration

6 ft. (1.8) — 2 40-conductor ribbon cables with chassis ground plane and signal paths.

1 ft (30 cm) — 2 40-conductor twisted pair cables.

Termination

6 ft (1.8 m) — The interface assembly contains receivers for data, address, and control from the Z80 Emulator Processor module.

1 ft (30 cm) — Not terminated.

TIMING CHARACTERISTICS

The Z80A Emulator Processor was designed to match the ac characteristics of the Z80A and Z80 Microprocessors with two exceptions. Those exceptions are:

Prototype Clock

The prototype clock may not be stretched over a total of 10 μs during any one memory or I/O request when a Microprocessor Lab memory access may occur in the next cycle. This exception is valid only if the prototype clock runs in excess of 1 MHz.

NMI

NMI (Non Maskable Interrupt) must occur one-half cycle earlier than in a standard Z80A configuration. This means the NMI must occur before the next-to-last trailing edge of the M cycle just prior to M1.

ORDERING INFORMATION

Option Description	Factory Price	Field Number	Field Price
8001 Microprocessor Lab	**$4950**		
Option 03 Z80A Microprocessor Support Package	**+$4100**	**8001F03**	**$4150**
8002A Microprocessor Lab	**$10,950**		
Option 03 Z80A Assembler Software Support	**+$ 850**	**8002F03**	**$ 900**
Option 18 Z80A Emulator Support	**+$2350**	**8002F18**	**$2450**
Option 33 Z80A Emulator Prototype Control Probe	**+$ 990**	**8002F33**	**$1090**

TMS9900 EMULATOR SUPPORT PACKAGE CHARACTERISTICS

TMS9900 refers to microprocessors manufactured by Texas Instruments Corporation. Tektronix, Inc., does not guarantee that other vendor's versions of the TMS9900 will be compatible with the TEKTRONIX Microprocessor Labs.

PHYSICAL CHARACTERISTICS

Length 6 ft (1.8 m) of cable from the emulator processor to the interface assembly.

9.5 in (24.2 cm) of cable from the interface assembly to the 64 pin plug.

Cable Configuration

6 ft (1.8 m) — 2 40-conductor ribbon cables with chassis ground plane and signal paths.

9.5 in (24.2 cm) — 2 32-conductor twisted pair cables.

Termination

6 ft (1.8 m) — The interface assembly contains receivers for data, address, and control from the TMS9900 emulator processor module.

9.5 in (24.2 m) — Not terminated.

TIMING CHARACTERISTICS

To TMS9900 from Interface Assembly	Emulation Typical	Interface Delays* Maximum (in ns)
ø1	41	59
ø2	41	59
ø3	41	59
ø4	41	59
CRUIN	12	23
INTREQ	12	18
IC0	12	23
IC1	12	23
IC2	12	23
$\overline{IC3}$	12	23
$\overline{HOLD}$	12	18
$\overline{READY}$	12	18
$\overline{LOAD}$	12	18
RESET	68	98
DATA	14	21

From TMS9900 to Interface Assembly	Typical	Maximum (in ns)
$\overline{DBIN}$	24	41
$\overline{MEMEN}$	12	18
$\overline{WE}$	12	18
CRUCK	12	23
CRUOUT	12	23
HOLDA	12	23
WAIT	12	23
IAQ	12	23
ADDRESS	14	21
DATA	14	21

Assumes 1.5 ft of cable at 1.5 ns/ft.

Note: All inputs and outputs of the 64 pin plug at the end of the prototype control probe are buffered by 74LSXXX type devices. In all cases, data and control should not change during clock ø1.

8002A and 8001 Microprocessor Lab System Options

ORDERING INFORMATION

Option Description	Factory Price	Field Number	Field Price
8001 Microprocessor Lab	**$4950**		
Option 04 TMS9900 Microprocessor Support Package	$4510	8001F04	$4570
8002A Microprocessor Lab	**$10,950**		
Option 04 TMS9900 Assembler Software Support	$ 850	8002F04	$ 900
Option 19 TMS9900 Emulator Support	$2600	8002F19	$2700
Option 34 TMS9900 Prototype Control Probe	+$1160	8002F34	$1260

1802 EMULATOR SUPPORT PACKAGE CHARACTERISTICS

PHYSICAL CHARACTERISTICS

Length — 6 ft (1.8 m) of cable from the emulator processor to the interface assembly. 1.5 ft (45 cm) of cable from the interface assembly to the 40 pin plug.

Cable Configuration

6 ft (1.8 m) — 2 40-conductor ribbon cables with alternating ground and signal paths.

1.5 ft (45 cm) — 2 laminated 40-conductor cables made up of signal-ground pairs.

TIMING CHARACTERISTICS

The 1802 Prototype Control Probe is designed to meet all the ac characteristics of the 1802 Microprocessor —Vcc $\geq$4.0 V.

AC CHARACTERISTICS

Emulation Clock

Mode 1 or Mode 2 (user clock) with 1802 Prototype Control Probe.	6.4 MHz max at 10 Vcc. 25°C, this can be crystal, or external input to clock (pin 1).
Tracking power supply to monitor user voltage (Vcc) and run the probe at the same voltage (4 V to 12 V).	2.5 MHz

EXECUTION SPEED

All modes of operation have zero (0) WAIT states with the following exceptions:

Mode	System Operation	*Number of WAIT States at 12 V and 6.4 MHz
1	8001/8002A Program Memory Used (Map mode)	1
1 or 2	no RTPA installed	1
1 or 2	trace mode selected	1
1 or 2	BKPT set (not EVT)	1

*For wait state requirement at other speeds, check with your service personnel.

ORDERING INFORMATION

	Factory Price	Field Number	Field Price
8001 Microprocessor Lab	**$4950**		
Option 08 1802 Microprocessor Support Package	+$4600	8001F08	$4650
8002A Microprocessor Lab	**$10,950**		
Option 07 1802 Assembler Software Support	+$ 850	8002F07	$ 900
Option 22 1802 Emulator Support	+$2850	8002F22	$2950
Option 38 1802 Prototype Control Probe	+$1090	8002F38	$1090

Standard Accessories

- System Users Package
  - Assembler and Emulator Users Manual
  - Assembler and Emulator Reference Card

8085A EMULATOR SUPPORT PACKAGE CHARACTERISTICS

8085 and 8085A refer to microprocessors manufactured by Intel Corporation. Tektronix, Inc., does not guarantee that other vendor's versions of the 8085 will be compatible with the TEKTRONIX Microprocessor Labs.

PHYSICAL CHARACTERISTICS

Length 6 ft (1.8 m) of cable from the emulator processor to the interface assembly.

1 ft (30 cm) of cable from the interface assembly to the 40 pin plug.

Cable Configuration

6 ft (1.8 m) — 2 40-conductor ribbon cables with chassis ground plane and signal paths.

1 ft (30 cm) — 2 40-conductor twisted pair cables.

Termination

6 ft (1.8 m) — The interface assembly contains receivers for data, address, and control from the 8085 emulator processor module.

1 ft (30 cm) — Not terminated.

AC CHARACTERISTICS

Emulation Clock

Mode 1 or Mode 2 (user's clock), with 8085A Prototype Control Probe.	6.25 MHz max*; crystal, RC timing network or TTL input to X1.
Mode 0 (system clock)	6.25 MHz ±0.01%

Operational Speed

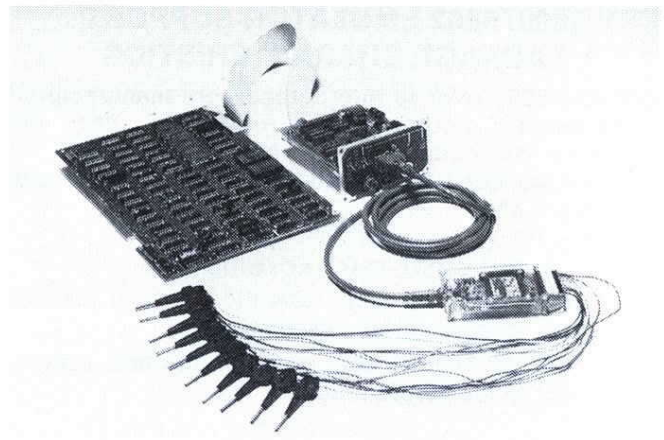
Full speed or 1 wait state per machine cycle during 8001/8002A program memory access selectable with jumper.

One wait state per machine cycle is inserted when using DEBUG breakpoints (BKPT) regardless of jumper position. When the Real-Time Prototype Analyzer option is installed, real-time operation with breakpoints automatically ensured during DEBUG by using the event triggers (EVT).

**A clock error detection circuit ensures that the user's clock is operational and basically within Intel max (1 μs) and min (160 ns) specifications.*

ORDERING INFORMATION

Option Description	Factory Price	Field Number	Field Price
8001 Microprocessor Lab	**$4950**		
Option 05 8085A Microprocessor Support Package	+$4100	8001F05	$4150
8002A Microprocessor Lab	**$10,950**		
Option 05 8085A Assembler Software Support	+$ 850	8002F05	$ 900
Option 20 8085A Emulator Support	+$2350	8002F20	$2450
Option 35 8085A Prototype Control Probe	+$ 990	8002F35	$1090



Real-Time Prototype Analyzer

The Real-Time Prototype Analyzer, Option 46 for the 8002A and 8001 Microprocessor Labs, is comprised of a real-time trace module, a data acquisition interface, and an 8 channel general logic probe. This option provides a real-time trace of the user program executing on the emulator processor, with 43 channels of data acquired simultaneously. The prototype address bus, data bus, control bus, and any eight external locations on the prototype circuit may be monitored without slowing up the operational speed of the processor. The Real-Time Prototype Analyzer is indispensable when isolating critical timing errors and hardware/software sequence discrepancies during the final integration phases of prototype development.

The analyzer module is a separate plug-in circuit card that may be inserted into either the 8002A or 8001 system mainframe. The P6451 Probe connects to the prototype circuitry and permits data transference from the prototype to the analyzer. Data from the prototype is buffered and driven by the probe to the data acquisition interface, and then loaded into the analyzer module's real-time trace buffer.

As the user program executes on the emulator processor, 48 bit data words are sequentially acquired from the prototype and loaded into the real-time trace buffer. Each data word contains 16 bit data from the address bus; 8 bit or 16 bit data from the data bus; 8 bit data from the test probe; 3 bit data identifying cycle type (read, write, I/O, memory, or instruction fetch); and 5 bit data used internally to identify last start/stop of the emulator processor. The analyzer will continue to acquire these sequential cycles of logic input until the processor is stopped or the real-time trace buffer is frozen by a specified trigger occurrence. The real-time trace buffer can retain up to 128 data words in pre-, variable center, or post-trigger modes; thus enabling the storage of pertinent program bus transactions.

The Real-Time Prototype Analyzer offers expanded breakpoints to aid in efficient location of prototype problems. Two event comparators located within the analyzer module can be utilized to halt program execution and stop real-time trace. A trigger may be generated on any specific data occurrence in the address bus, data bus, test probe input, and instruction cycle type. Triggering

may be immediate; delayed by counting the number of passes; or delayed by counting the number of clock select outputs (clock select may be by microseconds, milliseconds, emulator clocks, etc.). In addition, an output pulse may be generated, via the data acquisition interface, to trigger a logic analyzer or an oscilloscope.

The two event comparators (triggers) may be set to designate a break or halt in the program execution. These comparators may be used as independent breakpoints; or they may be used together to enable a breakpoint on a specific event combination. The program execution can be halted when two trigger events occur simultaneously; when one trigger event precedes another; or when either trigger event occurs. When a break in the program execution takes place, program transactions stored in the real-time trace buffer may be displayed or printed.

Data stored in the real-time trace buffer is displayed sequentially in the order it was acquired from the prototype. Buffer content may be displayed in whole or in part. Optional command parameters are available to limit the storing of data to any specific transaction type, such as memory reads only. If the total buffer contents are displayed, a blank line will separate the data sequence associated with each program starting point.

The Real-Time Prototype Analyzer features a convenient and easy-to-understand display format. With this format, the address location, data, probe input, and control bus data of each acquired transaction are displayed. If the transaction was an instruction fetch, the instruction is also disassembled into the appropriate mnemonic readout unique to the emulator type being used.

The Real-Time Prototype Analyzer functions in all emulation modes and operates with all commercial microprocessors supported by the 8002A and 8001 Microprocessor Labs.

REAL-TIME PROTOTYPE ANALYZER CHARACTERISTICS

OPERATIONAL SPEED CHARACTERISTICS

Processor	Maximum Processor Clock Rate*
8085A	3.125 MHz (internal clock)
8080A	2.08 MHz
6800	1.00 MHz
Z80	4.00 MHz
TMS9900	3.33 MHz
3870/3872	4.00 MHz
F8	2.00 MHz
6802	1.00 MHz
1802	6.4 MHz

**Maximum processor clock rate for Real-Time Prototype Analyzer operation.*

INPUT/OUTPUT CHARACTERISTICS

Variable Threshold

Range	$>+10$ V dc to <-10 V dc
Preset TTL Voltage	$+1.4$ V dc ± 200 mV
Event Trigger Out	High level voltage out (when Vcc=Min, Vi=0.5, Ro=50 Ω to GND) is >2 V dc.

Adjustments—Variable Threshold may be adjusted from $>+10$ V dc to <-10 V dc with a screwdriver adjustment accessible at the rear panel of the Microprocessor Lab. This voltage must be monitored with a voltmeter having an input impedance of at least 10 MΩ.

Jumpers—With the internal jumper in position '0-3' the clock threshold is designated to be the same as channels 0-3. In position '4-7' the jumper designates the clock threshold to be the same as channels 4-7.

Cable Length — 50 cm (19.5 in).

ORDERING INFORMATION

Option Description	Factory Price	Field Number	Field Price
8001 Microprocessor Lab	$4950		
Option 46 Real-Time Prototype Analyzer	+$2700	8001F46	$2900
8002A Microprocessor Lab	$10,950		
Option 46 Real-Time Prototype Analyzer	+$2700	8002F46	$2900

Modular Development Language MDL/μ

MDL/μ is a high level language designed specifically for use in microprocessor-based design. Its parent language is ANSI Minimal BASIC, a widely used and well understood programming format. MDL/μ offers an extensive number of enhancements from BASIC that make this new language an extremely effective design tool while retaining the advantages of simplicity and easy learning found in BASIC.

One essential advantage of MDL/μ is that it uses a compiler instead of an interpreter. Each program statement is translated to machine code only once, instead of every time the statement is executed. The result is faster, and often more compact code for final program execution.

MDL/μ allows a module-oriented approach to software development. Two statements, USES and PROVIDES, allow variables, functions and procedures to be shared by programmers working on different modules of an overall program. The USES statement also allows direct access to absolute memory locations, I/O ports and interrupts—all essential for proper control of hardware/software integration.

Variable names and strings have been considerably expanded with MDL/μ. Variable names can contain up to six characters, the first alphabetic and the others alphanumeric, for easy identification during program development. Strings can vary in length from 1 to 255 characters instead of the unalterable 18 used in minimal BASIC. Substring replacement is also enhanced to assist in character manipulation.

I/O features include access to ports and absolute addressing of memory, which allows variables to be assigned a specific address. Both ASCII and general purpose binary file manipulations are possible through a series of I/O statements including OPEN, CLOSE, RESTORE, READ, WRITE, PRINT and INPUT.

Among many other MDL/μ enhancements to BASIC are logical operators (AND, OR, XOR, NOT) plus shift and rotate operations for bit manipulation, DISABLE and ENABLE to turn the interrupt off and on and a built in code optimization.

The conversion of MDL/μ source code to actual machine code is a three-step process. The first step converts MDL/μ source code into assembly language source code which is stored on a file or device. The assembly source code contains the original MDL/μ statements as comments preceding each block of assembly source code. At this stage, the assembly language can be further optimized by using the 8002A's powerful editor. In the second step the assembler converts the assembly language source into object code. The third step is to link the object code with the run time support library and any other assembled object code modules.

ORDERING INFORMATION

MDL/μ

8002A Microprocessor Lab $10,950

Option Description	Factory Price	Field Number	Field Price
Option 01 8080A Assembler Software Support	+$850	8002F01	$900
Option 1A MDL/8080A Software Support* (Requires 64K Program Memory and Option 01)	+$1000	8002F1A	$1050
Option 02 6800 Assembler Software Support	+$850	8002F02	$900
Option 2A MDL/6800 Software Support (Requires 64K Program Memory and Option 02)	+$1000	8002F2A	$1050
Option 03 Z80 Assembler Software Support	+$850	8002F03	$900
Option 3A MDL/Z80A Software Support** (Requires 64K Program Memory and Option 03)	+$1000	8002F3A	$1050
Option 05 8085A Assembler Software Support	+$850	8002F05	$900
Option 1B MDL/8085A Software Support* (Requires 64K Program Memory and Option 05)	+$1000	8002F5A	$1050

*Option 1A and 1B are identical

**The compiler generates 8080A assembly language. This output must be assembled with the 8080A assembler included in Option 3A and run on the Z80.

1702 and 2704/2708 PROM Programmer

The 1702 and 2704/2708 PROM Programmer, Options 47 and 48 for the 8002A and 8001 Microprocessor Labs, provide the ability to program either 1702 or 2704/2708 erasable PROM chips. When the module is installed in an 8002A or 8001 Mainframe, the PROM Programmer software enables communication between 8002A or 8001 program memory and the PROM installed in the front-panel PROM programming porch.

1702 or 2704/2708 PROM Programmer software transfers one data byte at a time, and actual addresses are assigned. Data may be written from 8002A or 8001 program memory (WPROM); read from PROM into program memory (RPROM); or compared on the system terminal (CPROM).

The RPROM command allows the programmed PROM to be read into program memory and dumped to the system console. The CPROM compare function performs an address-by-address comparison between the PROM and the program under development. When an inequality between PROM bytes and memory bytes occurs, the memory address, memory byte content, and PROM byte content are displayed on the system console. A successful comparison between designated PROM and memory bytes is indicated by an End of Job message on the console.

ORDERING INFORMATION

Option Description	Factory Price	Field Number	Field Price
8001 Microprocessor Lab	$4950		
Option 47 1702 PROM Programmer	+$650	8001F47	$700
Option 48 2704/2708 PROM Programmer	+$650	8001F48	$700
8002A Microprocessor Lab	$10,950		
Option 47 1702 PROM Programmer	+$650	8002F47	$700
Option 48 2704/2708 PROM Programmer	+$650	8002F48	$700

CT 8101 Console Terminal

The CT 8101 Console Terminal is an optional peripheral recommended for use with the 8002A and 8001 Microprocessor Labs.

The CT 8101 in interfaced to the 8002A or 8001 through an EIA standard RS-232-C port on the system communications module. Data formats and baud rate are switch-selectable for TTY or EIA operation.

The keyboard provides selection of the full ASCII set of 96 characters. It also features character repeat when any key is pressed at the same time as the REPEAT key.

ELECTRICAL CHARACTERISTICS

Voltage	115 V RMS; +10%, −15%.
Frequency	47 through 63 Hz.
Power	75 W max.

PHYSICAL CHARACTERISTICS

Dimensions	in	cm
Height	4.25	10.79
Width	14.60	37.08
Length	15.25	38.73
Weight	**lb**	
Net	11.20 (including paper)	

ORDERING INFORMATION

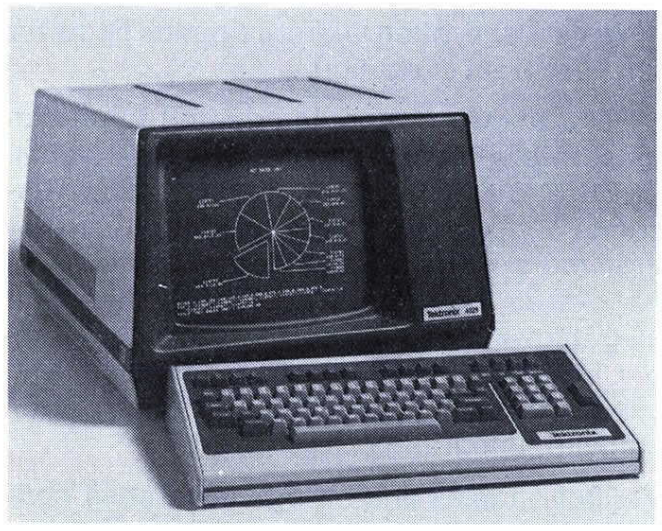
CT8101 Console Terminal $1395

4024 Computer Display Terminal

The 4024 Computer Display Terminal is an optional peripheral recommended for use with the 8001 or 8002A Microprocessor Labs.

The 4024 Computer Display Terminal is serially interfaced to either Microprocessor Development Labs through an EIA standard RS-232-C port on the systems communications module. The 12 inch (30 cm) diagonal crt displays up to 34 line of 80 characters each, and the keyboard contains a full ASCII set of characters in upper and lower case. Option 20 (8K bytes Program Memory) is required for proper 8001 and 8002A operation.

4024 Computer Display Terminal with Option 20* $3245



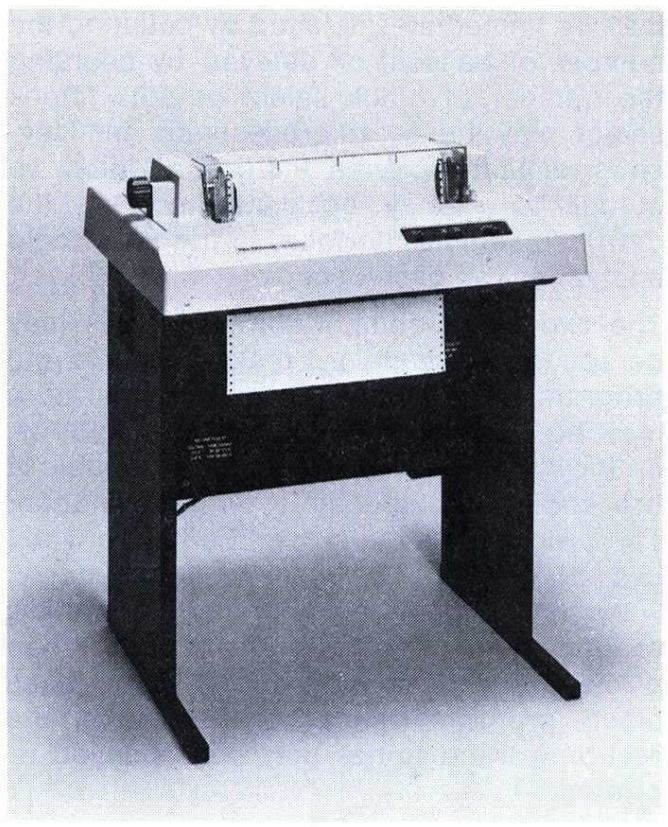
4025 Computer Display Terminal

The 4025 Computer Display Terminal is an optional peripheral for use with the 8001 or 8002A Microprocessor Development Labs.

The 4025 Computer Display Terminal is serially interfaced to either Microprocessor Development Labs through and EIA standard RS-232-C port on the systems communications module. The 4025 Terminal provides all the capabilities of the 4024 plus the ability to expand from basic alphanumerics, to forms ruling and then into graphics. Option 20 (8K bytes Program Memory) is required for proper 8001 and 8002A operation.

4025 Computer Display Terminal with Option 20* $3845

*Option 20 (8K bytes Display Memory) is required for proper 8001 and 8002A operation.



LP 8200 Line Printer

The LP 8200 Line Printer is an optional system peripheral for the 8002A and 8001 Microprocessor Labs.

The LP 8200 is serially interfaced to either Microprocessor Lab through an EIA standard RS-232-C port on the system communications module. Baud rates of 300 to 9600 are selectable.

The printout provides space for 132 characters/line, 6 lines/vertical inch. The full ASCII set of 96 upper/lower case characters is provided.

ELECTRICAL CHARACTERISTICS

Voltage	90 to 132 V ac standard*
Frequency	60 Hz ±1 Hz.
Power	400 W max (printing); 200 W max (idle).

PHYSICAL CHARACTERISTICS

Dimensions	in	cm
Height	33.5	85.09
Width	27.5	69.85
Length	21.7	55.12
Weight	**lb**	
Net	102	

ORDERING INFORMATION

LP8200 Line Printer $3765

*Alternate line voltages are available for the LP 8200. Please contact a Tektronix Field Office in your area for more information.