; <MEIS.SFMEA>SFMEA.DOC.4, 11-Mar-84 01:04:12, Edit by LOUGHEED

Creating SFMEA.A10 files.

The file SFMEA.CMD contains all the compiling information for SFMEA.
Create a non-sharable EXE file, like so:

```
$COMPILE @SFMEA.CMD
$LOAD SFMEA.REL
$CSAVE SFMEA.EXE
```

Now run the CONVRT program to create an A10 file that the -11 can handle.

```
$RUN CONVRT.RUN
*SFMEA.EXE
$                        <-- a .A10 has been created
```

Installing SFMEA on the KLAD.

Put the A10 file in some low numbered directory, such as PS:<OPERATOR>. You must find out the directory's PPN; use the TRANSLATE command to obtain it.

```
$translate ps:<operator>
 PS:<OPERATOR> (IS) PS:[4,5]
```

Now run the FE program to lock up the front-end directory. Use PARSER to mount the FE: device. At this point you must be logged onto the CTY.

```
$RUN SYS:FE
^\
PAR>M MOU
MOU>FE:
MOU>^Z
^\
```

Now run PIP. First delete the old version of SFMEA (if any); KLDCP runs only version 1 of a diagnostic. Then copy the new version from the user directory into the diagnostic directory. Finish by dismounting the FE: device.

```
PAR>M PIP
PIP>DB0:[6,11]SFMEA.A10;*/DE
PIP>[6,11]SFMEA.A10/NV=FE:[340,5]SFMEA.A10
PIP>^Z
^\
PAR>M DMO
DMO>FE:
DMO>^Z
^C              <-- CTRL-C out of the FE program
$
```

The MEIS diagnostic is now available for use.

Running SFMEA.

Shutdown the sytem and mount the KLAD pack on disk unit 0. Bring up the -11 with 203 in the switch register. Get into parser and run the BOO program. To the BOO> prompt type DBOOT and press return. At this point make sure the -11 switches are all off. To the KLDCP prompt, type BT. This loads KLDDT and the KL subroutine package. When you get back to the KLDCP prompt ">. ", you should set the appropriate switches in the -11 (note that bit postion 0 on the -11 switches is bit position 15 of a PDP-10 word). Load SFMEA into -10 memory with the command "P SFMEA". After it is loaded in, typing STD to the KLDCP prompt starts the diagnostic. CTRL-C returns you to KLDCP.

Summary of Tests.

Tests 0 through 177 exercise the Register Control Board. They are:

1	Check for more than one massbus device responding
2	See if device responds to handshake
3	Check for stuck control bits
4	Read drive type register
5	Reset/Write/Read 1's to maintenance register
6	Reset/Write/Read 0's to maintenance register
7	Reset/write 0's/write 1's/read/verify to maintenance register
10	Write 1's/write 0's/read/verify to maintenance register
11	See if Massbus clear works (0's in maint reg)
12	Float 1's in maint reg
13	Float 0's in maint reg
14	Test that parity net can generate a one
15	Test that parity net can generate a zero
16	Test parity net with various patterns
17	Reset/read/verify C01 REG-02
20	Write/read/verify a 1 to C01 REG-02
21	Write a 1/reset/verify C01 REG-02
22	Write a 1/write a 0/read/verify C01 REG-02
23	See that reading reg's 24-37 cause ILR errors
24	See that reading regs 00-23 does not cause ILR
25	Verify operation of REG-02 C03 (parity error)
26	Reset/write 0/verify C03 of REG-02
27	Reset/write 1 to C01 REG-02/read/verify C02 REG-02
30	Reset/write a 1/read/verify C03 REG-02
31	Reset/write a 1/write a 0/read/verify C03 REG-02
32	Reset/write a 1/reset/read/verify C03 REG-02
33	Cause a parity error and see if it's detected
34	Guarantee that GO bit, C00 REG-00, not stuck
35	Verify operation of C00 REG-03 (maintenance mode)
36	Reset/write 1's/read/verify C01-C15, REG-03
37	Verify complete operation of C01-C15 REG-03
40	Verify that no error bits are stuck at 1
41	Test access to all MEIS Controller writeable registers
42	Test selection of MEIS Controller writeable registers
43	Verify that Device Clear works
44	Verify some GO bit control logic

45 Insure erroneous commands aren't executed
46 Test for multi-device response
47 Test that a persistant composite error doesn't exist
50 Verify that Composite Error can be decoded
51 Verify that each REG-02 bit causes Composite Error
52 Verify that ATA can be cleared and set
53 Check Attention Active register

Tests 200 through 277 exercise the data buffer RAM and the address RAM for both the 3MB and 10MB MEIS network interfaces. They are:

200 Find and announce all flavors of network interfaces.
201 Find stuck bits in data buffer
202 Test data buffer addressing
203 Float 0's and 1's in data buffer
204 Test for data buffer locations interacting

205 Find stuck bits in 3MB Address RAM
206 Test for locations interacting in 3MB Address RAM

207 Find stuck bits in 10MB Address RAM
210 Float 0's and 1's in 10MB Address RAM
211 Test for locations interacting in 10MB Address RAM

Tests 300 through 377 exercise data transfer and formatting operations.

300 Test all data modes with a variety of byte sizes

MEIS REGISTER DEFINITIONS

25 July 1984

1. General Description of the MEIS

The MEIS (Massbus Ethernet Interface Subsystem) is a Massbus based Ethernet interface. A MEIS controller can have up to two network interfaces for either

the experimental 3 megabit Ethernet or the industry standard 10 megabit Ethernet.

Basic to every MEIS is a Controller or Register board that serves as the command and data interface to the Massbus. This document describes the register assignments of the Controller Board in detail. Every MEIS also has a Barrel Shifter board for performing data format conversions to and from the standard 8-bit format of the Ethernet. These data modes are also described in detail in this document.

In addition to the Register and Barrel boards, a MEIS may have one to two network interfaces. The interfaces may be of the same or different type. A 3MB interface consists of a single board, while the 10MB interface consists of two boards, a small front-end board and a larger frame buffer board.

As of this writing the microcode revision levels for the different MEIS boards are as follows:

Register Control
REX05

Barrel Shifter
BEX08

3MB Data Board
DEX04

10MB VIA Board
VEX01

10MB NI Board
NTX6 and NRX5

2. Register 0: Control Register

The low six bits of the control register contain a function code that describes a command to the MEIS controller. The high ten bits are unused. Functions 61 and 71 (Transmit and Receive Packet) should be set only by the RH20, and should be initiated in the KL10 by setting the Secondary Transfer Control Register in the RH20. All other functions should be set directly by the KL10, and should not be set as transfers by the RH20.

The LSB of the control register (the GO bit) is set under program control to initiate a function. It is reset by completion of function or assertion of an error condition which prevents the function's completion.

Reading the control register will return the last command function.

Each of the following functions affects only the interface selected by writing the Data Conversion Mode register (Register 13).

Function	Description
1	No operation.

3 Enable Packet Reception. Allows packets received from the Ethernet to be stored in the interface data buffer and enables Receiver Packet Available to cause ATA (generate a hardware interrupt).

5 Disable Packet Reception Prevents packets on the Ethernet from being stored in the interface data buffer and disables the interface from asserting ATA because of packet reception.

7 Flush Received Packet. Removes the current packet from the top of the receive queue in the interface data buffer. The next packet, if one exists, then becomes available for examination, reception, or a similar flushing fate. If no more packets exist, the Received Packet Available status bit for the selected interface is reset.

11 Interface Reset. Clears all bits in the Error Register. Resets ATA. Clears all event bits in the Status Register, i.e. Receiver Buffer Overflow Error and Composite Error. Sends the Drive Clear function to the selected interface, which then does a microcode restart, resetting all registers, pointers, and flags.

13 Flush Transmit Buffer/Microcode Snapshot. For a 3MB interface, this function removes the packet in the transmit buffer and sets the Transmit Available flag in the Status Regiser.

For a 10MB interface, this function writes the contents of the micro machine register file to locations 0 through 17 of data buffer. The register contents may be then read with an absolute buffer read function. The original contents of the lower portion of the transmit buffer at destroyed, hence the interface should be reset before attempting to transmit further packets. This function is useful for debugging the 10MB interface microcode.

21 MEIS Preset. Same as Interface Reset, function 11.

61 Transmit Packet. Causes the MEIS to receive a packet from the Massbus, and to subsequently transmit it over the Ethernet.

71 Receive Packet. Causes the MEIS to transfer the packet at the top of the receive queue in the selected interface over the Massbus to the RH20.

3. Register 1: Status Register

Bit Description

0 Packet Available on Interface 0. A packet is available in the receive buffer of interface 0. Reset otherwise

1 Packet Available on Interface 1. A packet is available in the

receive buffer of interface 1. Reset otherwise

2 Receive Buffer Overflow. Set when the receive queue of the selected interface becomes full. The rest of the packet being received will be ignored. When the end of the packet is detected the packet will be flushed. Cleared by the Interface Reset function.

3 Receiver Enabled. Set if the Enable Packet Reception command has been given for the selected interface. Reset by the Disable Packet Reception command.

4 - 6 Not used.

7 MEIS Ready. Set if MEIS is ready to accept a new command, reset otherwise. Causes ATA on 0 to 1 transition. At present no command lasts long enough to reset this bit.

8 Transmit Buffer Available on Interface 0. Set when the transmit buffer for interface 0 can hold another packet, reset otherwise.

9 Transmit Buffer Available on Interface 1. Set when the transmit buffer for interface 1 can hold another packet, reset otherwise.

10 Transmitter Acquired Ethernet. Set when the selected interface has acquired the Ethernet and is transmitting a packet. Reset otherwise.

11 Interface Installed. Set if the selected interface is installed in the MEIS backplane. Reset if the interface is absent.

12 Ethernet Busy. Set whenever a carrier is detected on the Ether for the selected interface. Reset whenever no carrier is detected.

13 Not used.

14 Composite Error. Set when any bit in the Error Register becomes set. Reset by Interface Reset command.

15 Attention Active. Set when any bit in the Error Register is active or when there is a change in status. Reset otherwise.

The 0 to 1 transition of the following status bits causes Attention Active (ATA): Receiver Packet Available on Interface 0, Receiver Packet Available on Interface 1, Interface Ready, Transmit Buffer Available on Interface 0, Transmit Buffer Available on Interface 1 and Composite Error.

Note: bits 2, 3, 10, 11, and 12 apply only to the Ethernet interface selected by the Data Conversion Mode register (Register 13).

4. Register 2: Error Register

If any bits are set in the Error Register, the Composite Error bit will also be set in the Status Register. The Error Register may be cleared by writing a zero to it or by giving an Interface Clear command.

Bit	Description
0	Illegal Function. Set when an invalid function code is loaded into the Command Register.
1	Illegal Register. Set when an illegal register is read or written.
2	Register Modification Refused. Set when a register, other than the Attention Summary or Maintenance Registers, is written to during a Massbus transfer.
3	Control Bus Parity Error. Set when a parity error is detected on the asynchronous bus during a register write.
4	Data Bus Parity Error. Set when a parity error is detected on the synchronous bus during a data write.
5 - 10	Not used.
11	Massbus Transfer Aborted. Set if a Massbus read or write was timed out by the MEIS controller board.
12	Acquisition Error 0. Set by the failure of Interface 0 to acquire the Ethernet after sixteen attempts.
13	Acquisition Error 1. Set by the failure of Interface 1 to acquire the Ethernet after sixteen attempts.
14	Invalid Write Error. Set by a Transmit Packet command being given when the Transmit Buffer is full. The Massbus transfer is not done.
15	Invalid Read Error. Set by a Receive Packet command being given when the packet buffer is empty. The Massbus transfer is not done.

5. Register 3: Maintenance Register

Bit	Description
0	Maintenance Mode. Setting this bit puts the selected interface into maintenance mode. In this mode, one of several diagnostic functions can be selected to examine and test the MEIS hardware and microcode. Resetting this bit puts the MEIS in normal mode and resets all other bits in the Maintenance Register.
1	Control Bus Parity. Setting this bit causes the MEIS to

generate even parity when putting data on the control bus, which should generate parity errors in the Massbus controller (MBC). Resetting this bit causes the parity to be odd, which is normal.

2 Data Bus Parity. Setting this bit causes the MEIS to generate even parity when putting data on the data bus, which should generate parity errors in the MBC. Resetting this bit causes the parity to be odd, which is normal.

3 Maintenance ATA. Setting this bit causes the MEIS to set the Attention Active register (a one-bit register). Resetting this bit allows the Attention Active register to be cleared by the MBC.

4 Maintenance Receiver Enable. This bit must be set for packets to be received (via loopback or from the net) on the selected interface while maintenance mode is enabled.

5 Address Mask Disable. Setting this bit causes the receiver on the selected interface to respond to all Ethernet addresses. Clearing this bit returns the interface to the previous address mask.

6 Not used.

7 Local Loop Back. Setting this bit causes all transmissions on the selected interface to be looped back to the receiver, and all Ethernet transmission and reception to be disabled. Resetting this bit enables normal transmission and reception.

14 Maintenance Initialize. Setting this bit causes a hardware reset on the MEIS controller and interfaces. This provides a means of resetting the MEIS hardware without resetting all devices on the Massbus. Note that since this is a complete hardware reset, all registers are cleared and the device leaves maintenance mode. Reception is disabled on both interfaces, however the Address RAM's retain their previous state.

15 Maintenance Interface Select. This bit selects which Interface is in maintenance mode. Only one interface may be in maintenance mode at any time. The other will function normally. This bit reset selects the Interface in slot 0, while set selects slot 1.

Note: Bits 4, 5, and 7 apply only to the Interface selected by bit 15, Interface Select.

6. Register 4: Attention Summary Register

This bit is set by the MEIS asserting its Attention line (also called ''raising ATA''). It is reset under program control by writing a one to the appropriate bit. From the MEIS controller standpoint, the Attention summary register is a single bit. From the RH20 standpoint, the register is eight bits, each showing the status of the Attention line on a particular drive. Up to

eight devices can be on an RH20's Massbus and each is assigned a corresponding bit position in the Attention Summary register. When a read is done from register 4, all of the devices respond by driving the appropriate control bus data line.

7. Register 5: Secondary Address Register

This register contains the byte count for a Massus transfer. It must be loaded by the RH20 with the byte count before a Receive Packet or Transmit Packet command is given. Set this register by setting the RH's Secondary Block Address Register (SBAR) before performing a data transfer. The KL does not need to set the register itself.

7.1. Byte counts for packet transmission

In most data modes the byte count is merely the total number of bytes in the packet to be transmitted, including header bytes but not including trailer bytes. In 36-bit mode, however, the following table should be used for calculating the byte count (modulo 18) based on the number of words in the packet (modulo 4):

Num Words	Bytes Xmitted	Byte Count
0	00	00
1	05	05
2	09	09
3	14	12

A byte count of 12 should be set for 3 words of 36-bit data, because if the byte count is set to tell it 14, then when the MEIS has finished processing the third word it still can't tell whether it needs to ask for another word. Whether or not it needs another word, it will have 2 bytes more to output, and it can only detect having one byte left. If the byte count is set to 12, the MEIS notices that it has no more data and dutifully goes off to finish sending the third word. The byte count should be set to 12 instead of 13 so that the ''low byte valid'' signal stays high, i.e. if it were set to 13 the MEIS would send 13 bytes instead of 14.

7.2. Byte counts for packet reception

When the KL is receiving data from the MEIS, the byte count refers to the number of 9-bit bytes that the RH will transfer. Thus it should be exactly four times the number of 36-bit words transferred, no matter what combination of data modes and header lengths is used. Note that for packet reception this count is not the number of octets in the packet being transferred.

8. Register 6: Drive Type Register

Bit	Description
0 - 8	Drive Type Number. Used to denote device type (disk drive, tape drive, MEIS, etc.) For a MEIS the drive type number is 700.
9 - 10	Not used.

11	Drive Request Required. Set denotes device is to be operated in dual port environment. For a MEIS this bit is 0.
12	Not used.
13	Moving Head. Set indicates device is a moving head device. For a MEIS this bit is 0.
14	Tape Drive. Set indicates device is a tape drive. For a MEIS this bit is 0.
15	Not Block Addressed. Reset indicates device is block addressed. For a MEIS this bit is set.

9. Register 7

This register is not used by the MEIS.

10. Register 10: Data Buffer Address Register

This register is used to specify an absolute or relative offset into the selected interface's data buffer and is used in conjunction with the Buffer Data Register (Register 11). Each location addressed is 16 bits wide.

The address field is 12 bits wide for the 3MB interfaces. The transmit buffer runs from location 0_8 to 1777_8 while the receive buffer runs from 2000_8 to 7777_8.

For the 10MB interfaces the address field is 13 bits wide and is evenly split between the transmit buffer (0_8 to 7777_8) and the receive buffer (10000_8 to 17777_8).

If the sign bit (bit 15) is set when writing this register, then the address is absolute. If the sign bit is reset, then the address is relative to the top of the first packet in the receive buffer queue. No bounds checking is done; a bad address returns indeterminate results.

Bit	Description
0 - 12	Receiver Buffer Address. Specifies the address of a word in the receiver buffer.
13 - 14	Not used.
15	Absolute Address Select. Setting this bit causes the data buffer address to be used as an absolute address into the selected interface's data buffer. Clearing this bit causes the data buffer address to be a pointer into the packet at the top of the receive queue.

11. Register 11: Buffer Data Register

Reading the Buffer Data Register returns the contents of the 16 bit location addressed by the Receiver Buffer Address register. In maintenance mode, writing

to this register causes the data to be written in the indicated location. After each read or write of this register, the address selected by the Buffer Address Register is incremented.

Note that after selecting an interface, the Buffer Address Register must be written before reading the Buffer Data Register.

12. Register 12: Packet Status Register

This register contains the status and length of the packet at the top of the receive queue. Note that after selecting an interface, the Status Register must be read before reading the Packet Status Register.

For 10MB interfaces only the packet length is returned. No information is returned for packets that overflowed the receive buffer or had CRC errors.

Bit	Description
0 - 10	Packet Length. Contains the length, in bytes, of the packet at the top of the receive queue.
11	Overflow Error. 3MB interfaces only. If set this bit indicates that part of this packet is missing due to insufficient room in the buffer.
12 - 14	Not used.
15	Data Check Error. 3MB interfaces only. If set this bit indicates that a CRC error occurred in the packet at the top of the receive queue.

13. Register 13: Data Conversion Mode Register

Writing this register will select an interface and will determine which data mode(s) are to be used for the next Massbus transfer.

Bit	Description
0 - 2	Conversion Mode Select. Selects the conversion mode to be used in translating the 8-bit Ethernet format information to or from the 36-bit Massbus format. See the section on MEIS data modes for further details.
3	Interface Select. Determines which network interface is selected for Massbus interrogation and control. All interface related control functions and status information apply only to the selected interface. Resetting this bit selects the interface in slot zero; setting it selects slot one. When a new interface is selected the following applies: 1. The Buffer Address Register must be written before reading theBuffer Data Register. 2. The Ethernet Address Register must be written before it is read.

3. The Status Register must be read before reading the Packet Status Register.

4	Inverse Network Interface Select.
5	Header Mode Select. Selects the header data mode. If this bit is set, header bytes will be read in the 32-bit data mode. If it is reset, they will be read in the 16-bit data mode. See also the Transmit Packet Header Count Register (Register 21).
6	Not used.
7	Trailer Mode. Setting this bit causes the two bytes in the Trailer Register to be appended to the packet in the Transmit Buffer. If this bit is reset, this appending is not done.
8 - 15	Not used.

14. Register 14: MEIS Controller Serial Number Register

This register identifies each MEIS controller with a unique serial number. This serial number is set with jumpers located on the Register Control Board.

15. Register 15: Transmit Trailer Register

Contains two data bytes to be appended to the next transmitted packet. This register should be loaded and the Trailer Mode bit set in the Mode register before giving the Transmit Packet function. The data transferred over the Massbus will be formatted according to the selected data conversion mode and loaded into the transmit buffer. Then, if Trailer Mode is set, the two data bytes are put on the end of the packet to be transmitted. The Data Conversion Mode has no effect on these two bytes. They are transmitted exactly as they are loaded into the register. This is intended for uses such as checksums on PUP protocol packets.

If the byte count for the packet is odd, a garbage byte will be added before the trailer.

16. Register 16: Diagnostic Memory Data Register

All the bits in this register can be read and written by the RH20. Reading and writing this register only affects this register; it has no effect on other MEIS functions or operations. This register can therefore by used to check the data paths and basic functionality of the MEIS. This register is located in the 2901 arithmetic logic unit on the Register Control Board.

17. Register 17: Absolute Data Buffer Address Register

Contains the actual Receiver Buffer memory address indicated by the Buffer Address register. While the buffer address may be relative, with respect to the beginning of the received packet, or absolute, the value in this register is always absolute. See the discussion of Register 10 for the memory layout of the different types of interfaces.

18. Register 20: Ethernet Address Register

The definition of this register depends on which type of interface has been selected by the Data Conversion Mode Register. For the 3MB data board:

Bit	Description
0 - 7	Address Field. This field specifies a particular 8-bit 3MB Ethernet address. If Write Enable is set, a write to this register causes the Address Field to be written into the selected address mask field. If Write Enable is reset, the address mask field is not written. Reading the Address Field yields the contents of the address mask field selected by the last write to the Ethernet Address Register.
8	Receive Enable. When Register 20 is read, this bit indicates whether reception is enabled for packets with the destination address shown in the Address Field. If bit 8 is set, the packets destined for that address will be received. Reception is enabled by writing to Register 20 with Write Enable and Receive Enable set. Reception is disabled by writing with Write Enable set and Receive Enable reset.
9 - 14	unused
15	Write Enable. This bit has an effect only if Status register bit 3, Receiver Enabled, is reset. Writing to Register 20 with this bit set writes the Address Field and Receive Enable, enabling or disabling reception at that address. Writing to Register 20 with this bit reset causes only the Address Field to be written. Reading Register 20 then shows the state of Receive Enable for the Address Field last written.

Address Mask selection for the 10MB Interface is much more complex. A cell in the Address Mask RAM is 8 bits wide and has an 11 bit address. Each bit in a cell comprises a finite state machine. Up to 8 FSM's can be set up for a 10MB interface. A single FSM can listen to one or more addresses, depending on how many wildcarded bits have been set.

An 10MB Ethernet address is comprised of six octets. To set an an address, first form an 11 bit quantiry whose first three bits are the address octet number (0 to 5) and whose last eight bits are the address octet itself. Write this 11 bit quantity to Register 20 to set up a pointer into the Address RAM.

Reading Register 20 at this point will return an 8 bit quantity. Each bit corresponds to one of 8 finite state machines that the address match hardware uses for selecting a packet. The software must make an arbitrary decision as to which FSM (0 through 7) is being set up. Setting the appropriate FSM bit will cause packets whose address octet corresponds to the 11 bit address to be conditionally accepted (all six of the packet's address octets must pass the address filter). Clearing the FSM bit will cause a packet to be rejected.

To set up a FSM bit, the sign bit (bit 15) must be set and the 8 FSM bits must be written to the location that was selected by an earlier write to Register 20.

Bit	Description

0 - 11	Address Mask. High three bits correspond to 10MB Ethernet address octet number (0-5), low 8 bits correspond to the actual contents of that address octet. If Write Enable is off, writing Register 20 will select a location in the Address RAM.
0 - 7	Data Mask. On a read this field contains the status of the 8 finite state machines. A bit set indicates that a packet with an address octet that corresponds to this location in the Address RAM should be conditionally accepted. All six address octets in the packet must be conditionally accepted. If the bit for the particular FSM is cleared, the packet will be rejected.
12 - 14	Not used.
15	Write Enable. If this is bit is set on a write, the FSM bits in the Data Mask field will be set for the Address Mask location that was previously selected.

After selecting an interface the Ethernet Address Register must be written before it is read.

19. Register 21: Packet Header Count Register

Before giving the Transmit Packet or Receive Packet command to the Control Register, the length of the packet header must be written into this register. The packet header is defined as the number of 16-bit words that will be transferred using the conversion mode indicated in bit 5 of the Data Conversion Mode Register. After the header transfers, the remainder of the packet will be transferred using the conversion mode in bits 0 - 2 of the Mode Register.

The header count can be thought of either as the number of 16-bit words in the header or as the number of 18-bit Massbus bytes transferred by the RH20. It is not the number of octets in the header, nor is it the number of 36-bit words transferred. The header count should be even so that the header comes out to be an even number of 36-bit words; unpredictable results will occur from an odd header count. The maximum length of the transmit packet header is 4096 words.

As an example, for the PUP protocols on a 3MB Ethernet, each packet starts out with four octets of network encapsulation containing the source and destination addresses and the protocol type. These are followed by 20 octets of PUP protocol header for a total of 24 octets. An appropriate header count for such a packet would be 12.

20. Register 22: Controller Microcode Version Register

Register 22 contains the version number of the MEIS controller microcode.

Bit	Description
0 - 7	Minor Version Number.
8 - 15	Major Version Number.

21. Register 23: Interface Serial Number Register

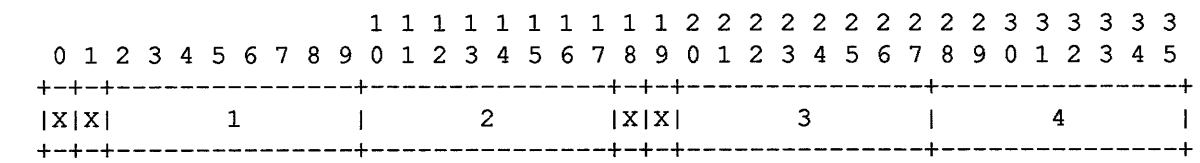
This register identifies each Ethernet interface with a unique serial number. This serial number is set with jumpers located on each interface board. Before reading this register the desired interface must be selected by the Data Conversion Mode Register.

Serial numbers for 3MB interfaces are of the form 3xxx. 10MB interfaces serial numbers are of the form 10xxx. Reading this register is the only way the software can determine the nature of the interface.

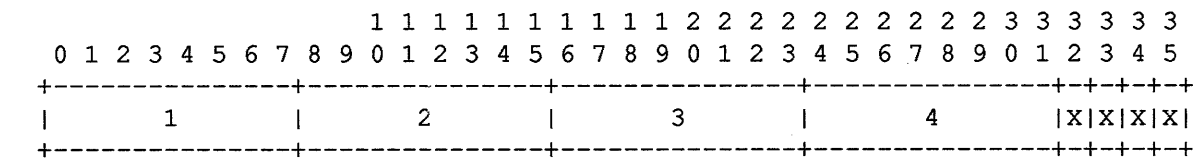
22. MEIS Data Modes

The following data conversion modes can be selected by writing Register 13.

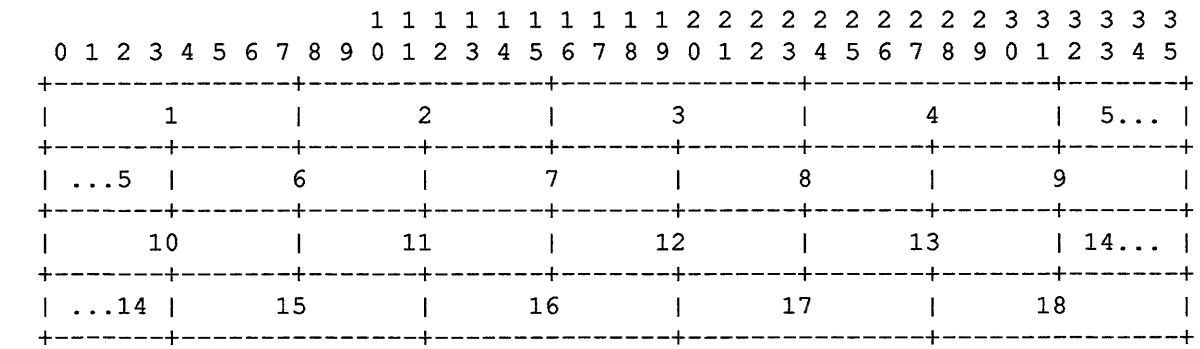
Mode 0 - 16-bit mode



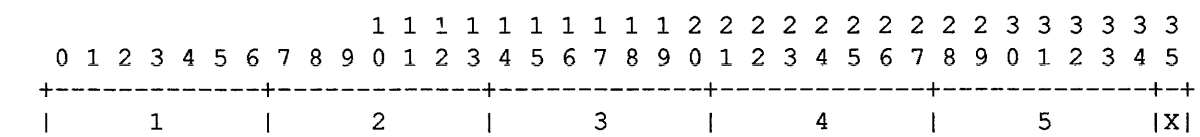
Mode 1 - 32-bit mode

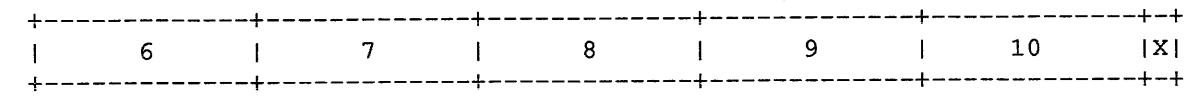


Mode 2 - 36-bit mode

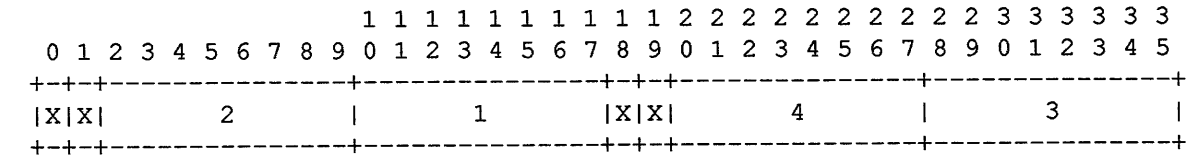


Mode 3 - ASCII mode

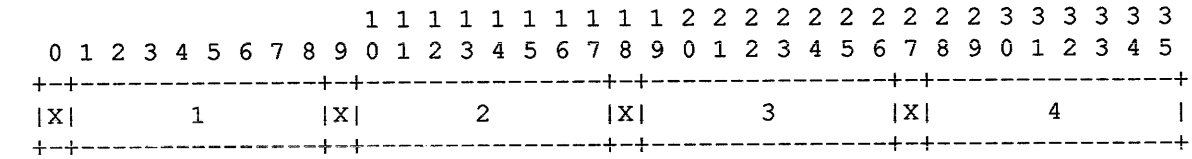




Mode 4 - 16-bit byte swapped



Mode 5 - 9-bit mode



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TITLE: DATA I/O BRD: , SLAVE ID REGISTER

FILE: SLIDE[MEIGFS]

DATE: 23-Oct-81 10:15

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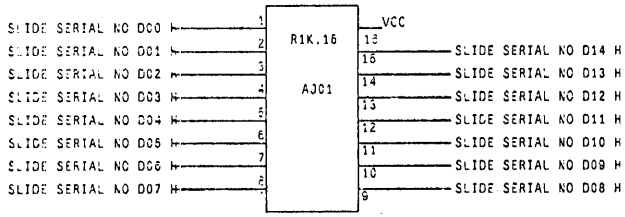

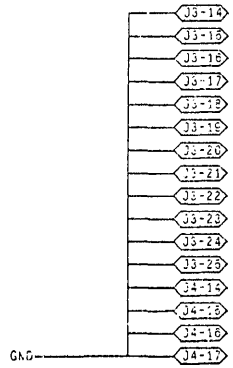

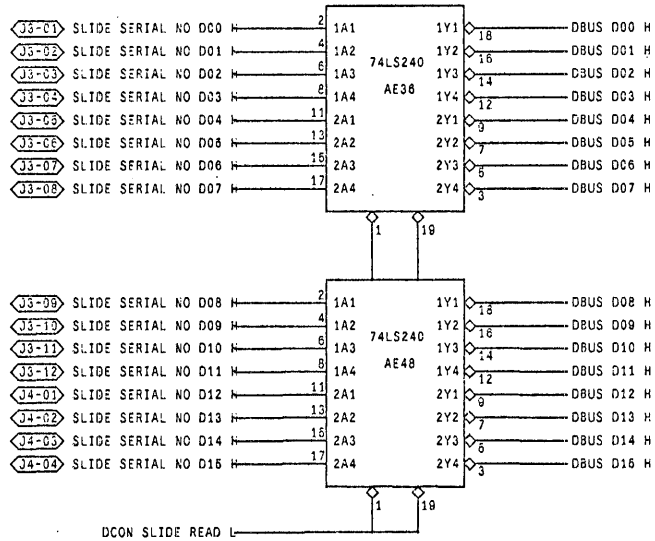

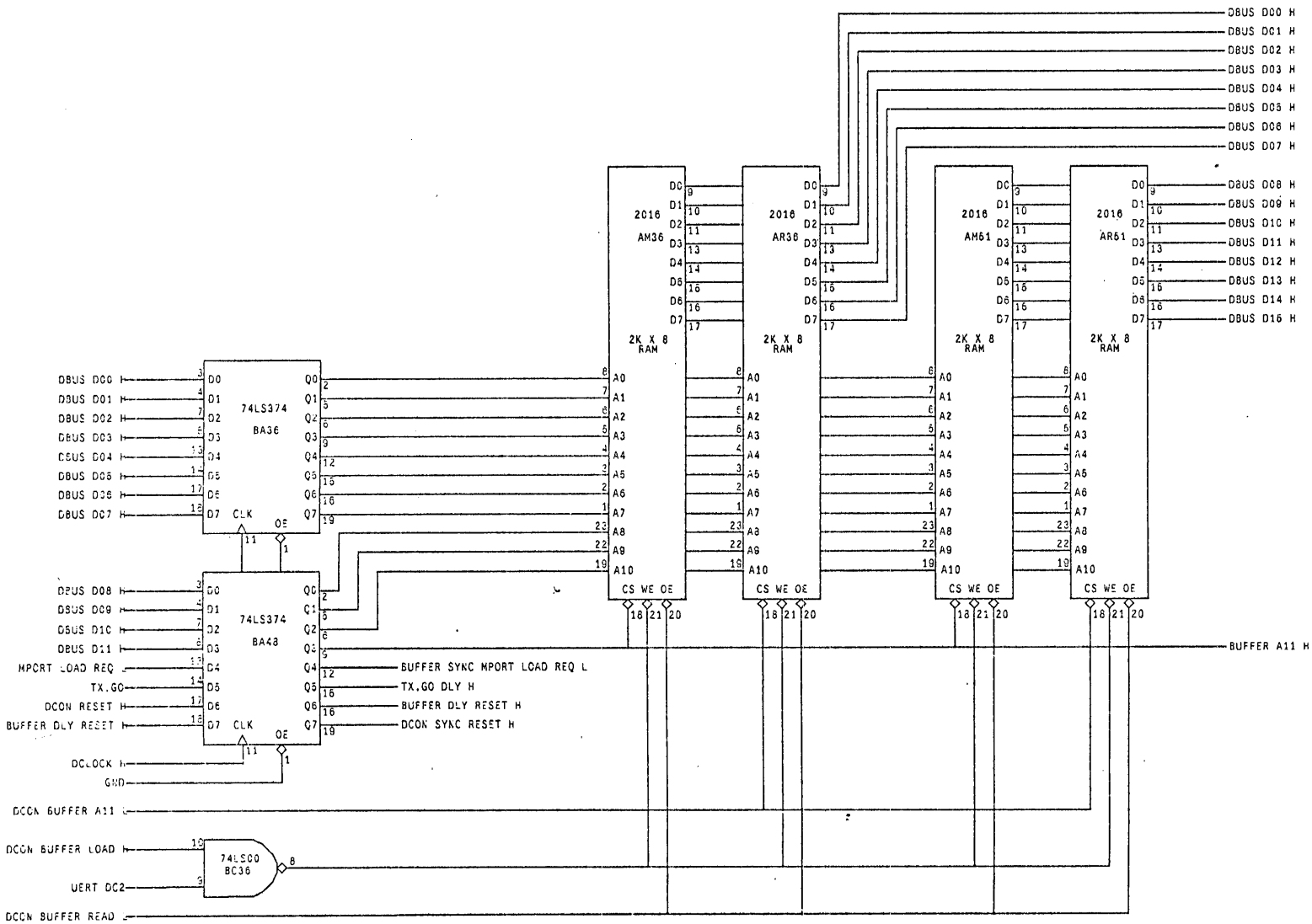

TITLE: DATA I/O BRD:, ADRS REG AND 4K PACKET BUFFER

FILE: BUFFER[MEIGFS]

DATE: 19-May-82 21:16

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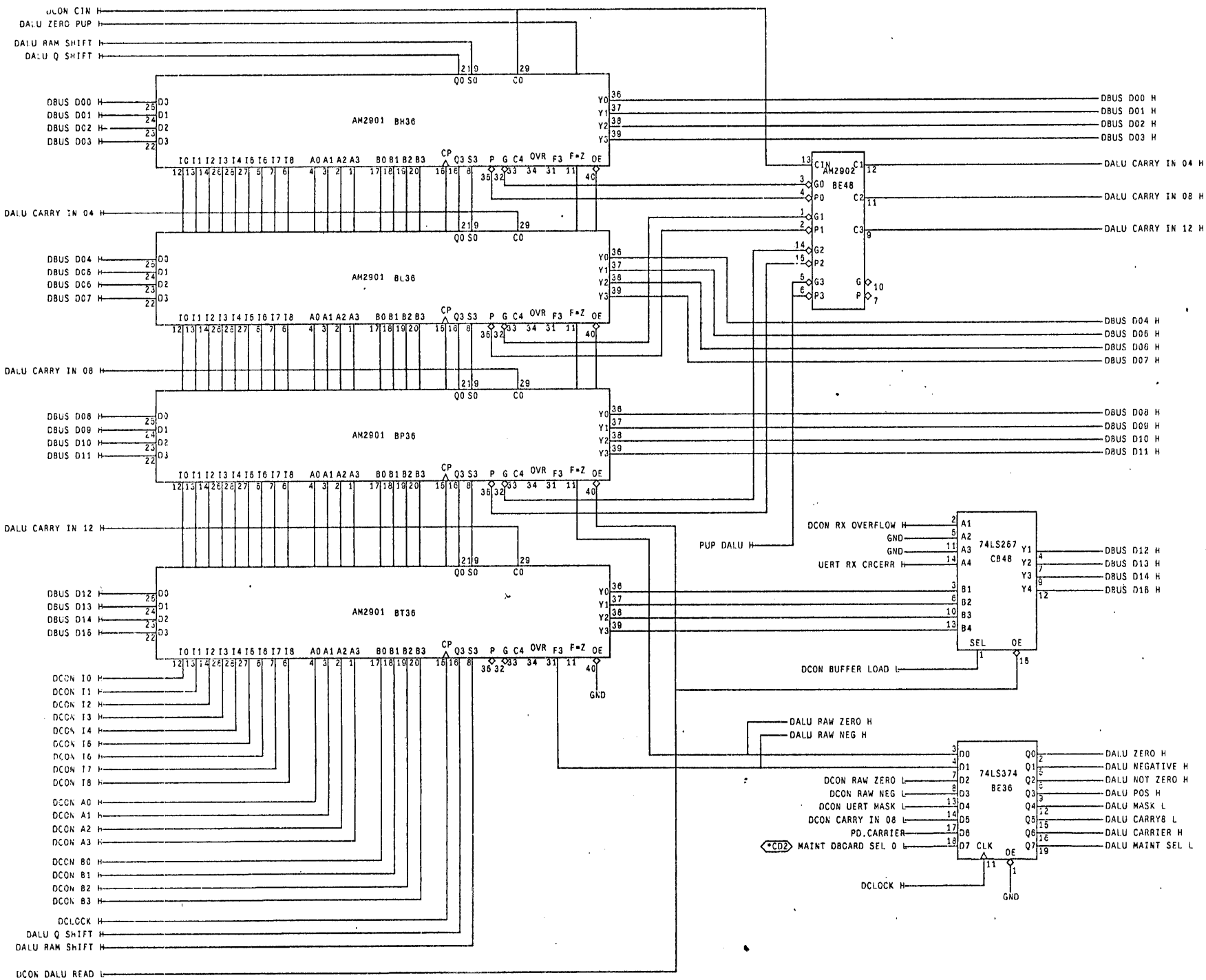
COMPUTER SCIENCE DEPARTMENT, STANFORD UNIVERSITY, STANFORD, CALIFORNIA 94305

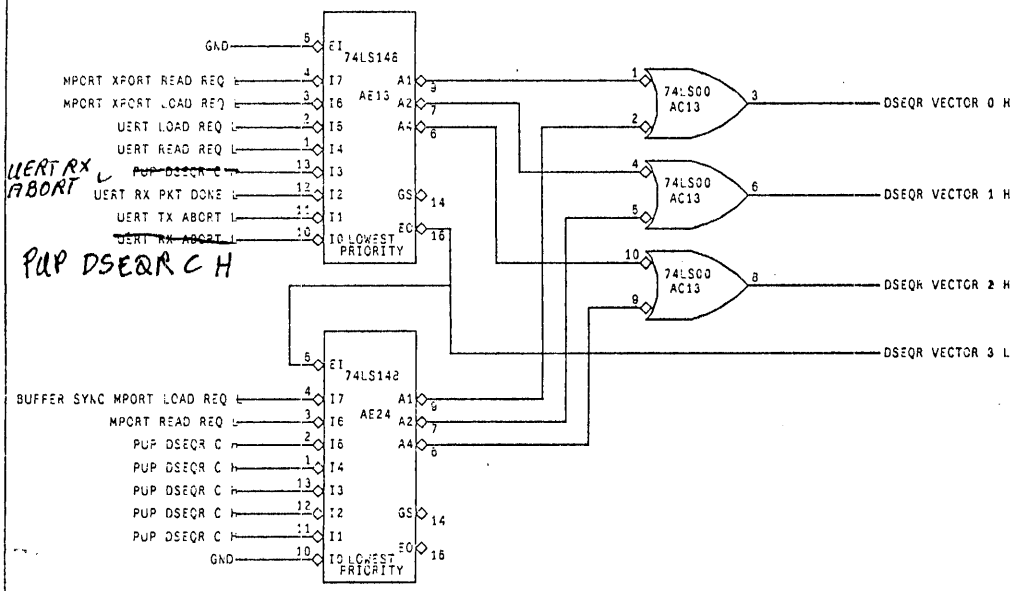
TITLE: DATA I/O BRD:, 16-BIT ALU

FILE: DALU[MEIGFS]

DATE: 26-Jan-82 15:13

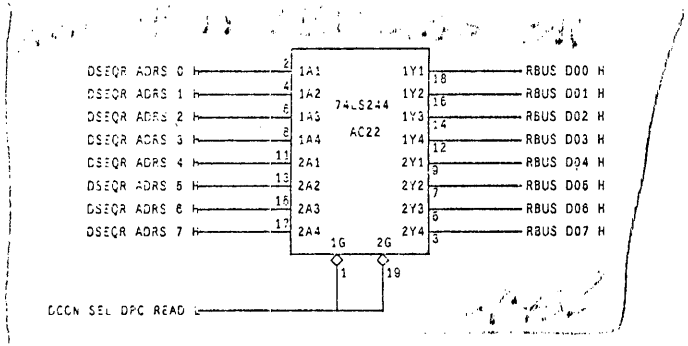
PAGE: OF

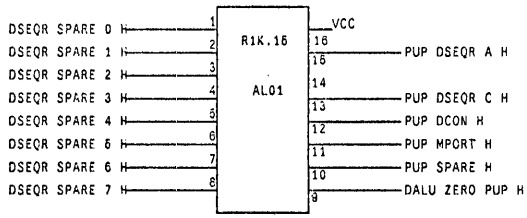


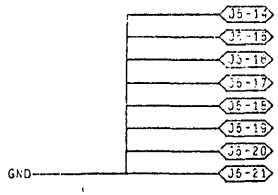


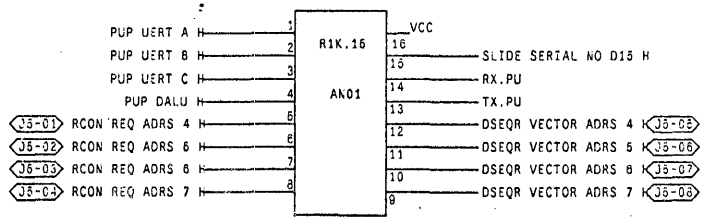
UERT RX ABORT L

PUP DSEQR C H









TITLE: DATA I/O BRD, REQUEST VECTOR GENERATION

FILE: DSEQR2[MEIGFS]

DATE: 19-May-82 21:15

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TITLE: DATA I/O BRD, REQUEST VECTOR GENERATION

FILE: DSEQR2[DW1GFS]

DATE: 10-Nov-82 09:06

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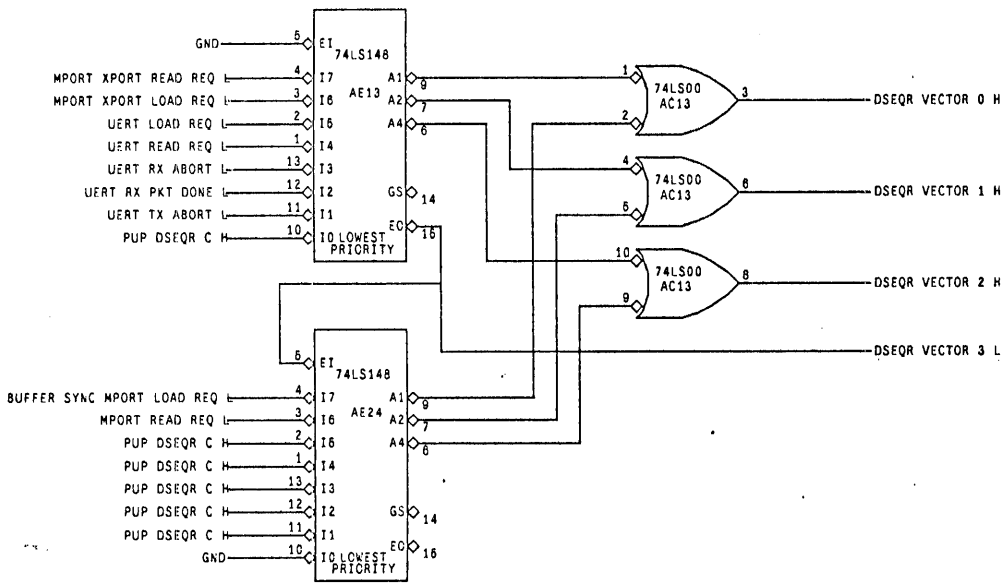

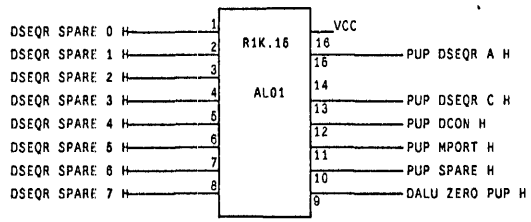

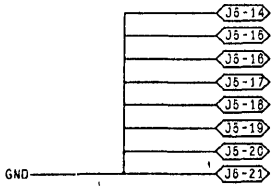

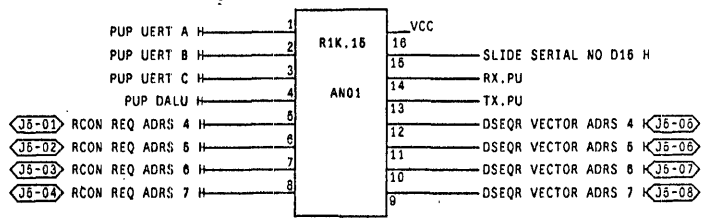

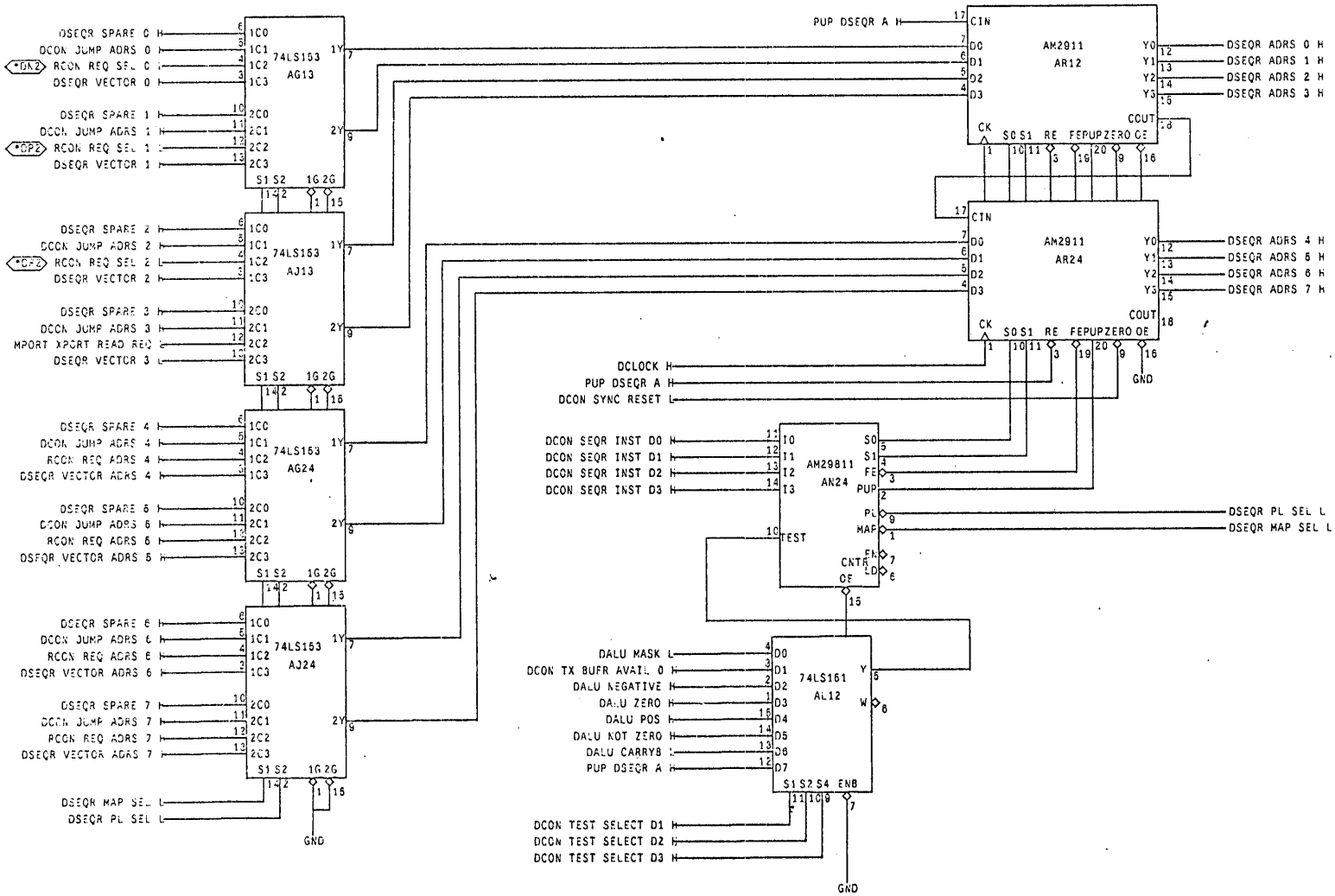

TITLE
DATA I/O BRD:, CONTROL MICROSEQUENCER

FILE
DSEQR1 [ME1GFS]

DATE
17-May-82 20:36

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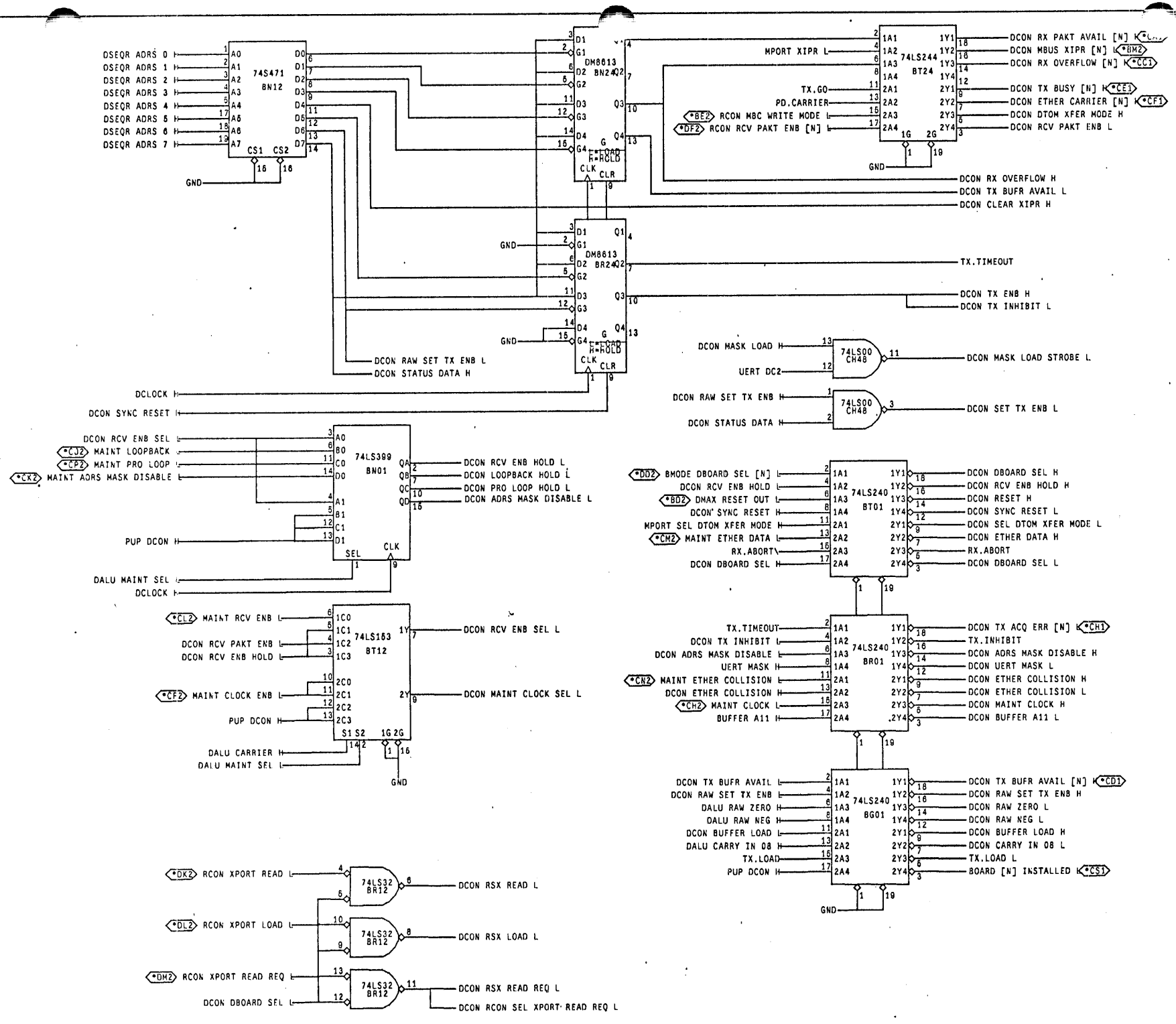
OF

COMPUTER SCIENCE DEPARTMENT, STANFORD UNIVERSITY, STANFORD, CALIFORNIA 94305

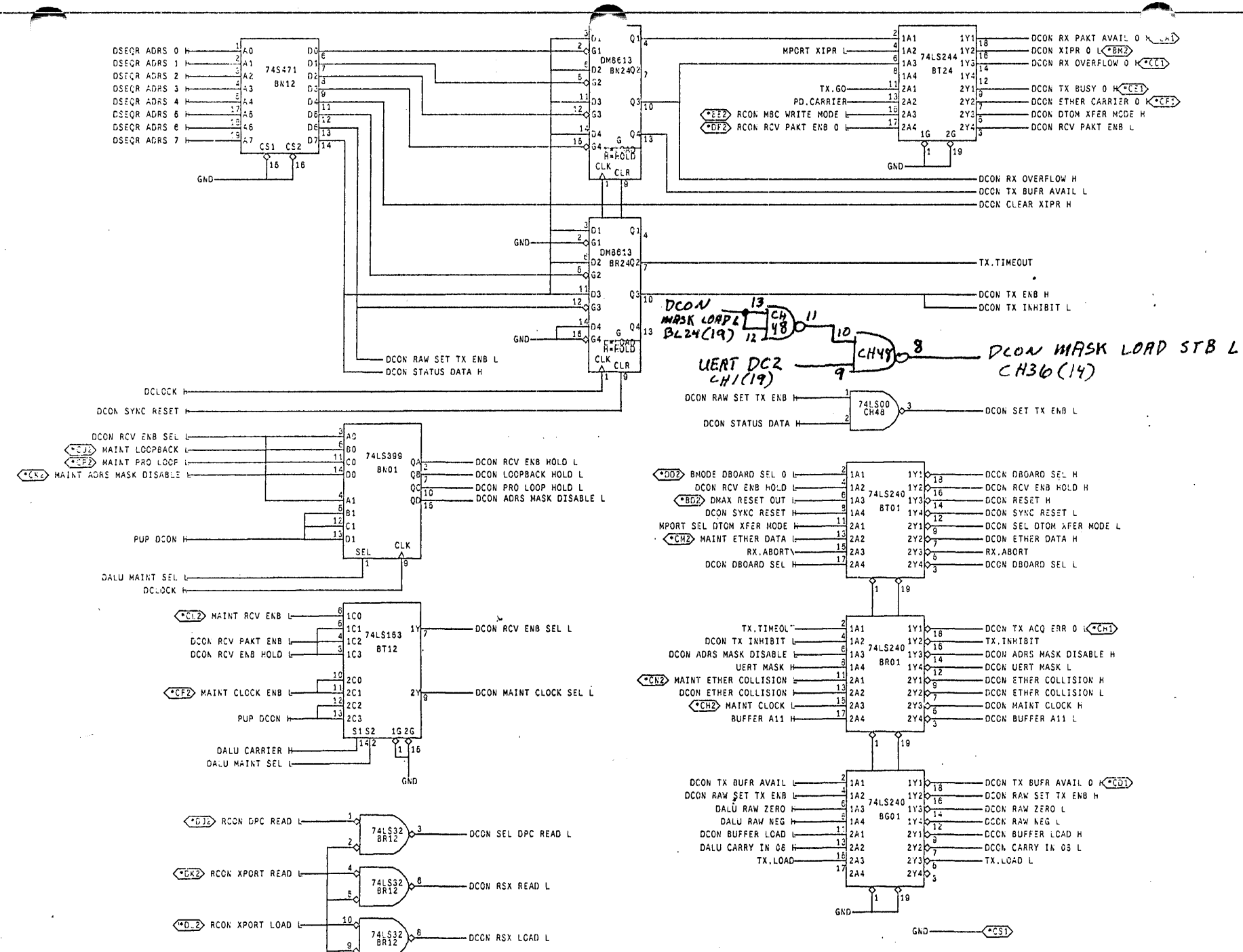


TITLE: DATA I/O BRD, STATUS REGISTER & CNTL I/O

FILE: DCON2[DW1GFS]

DATE: 10-Nov-82 09:06

PAGE: OF



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FILE: DCON2[ME1GFS]

DATE: 19-May-82 20:58

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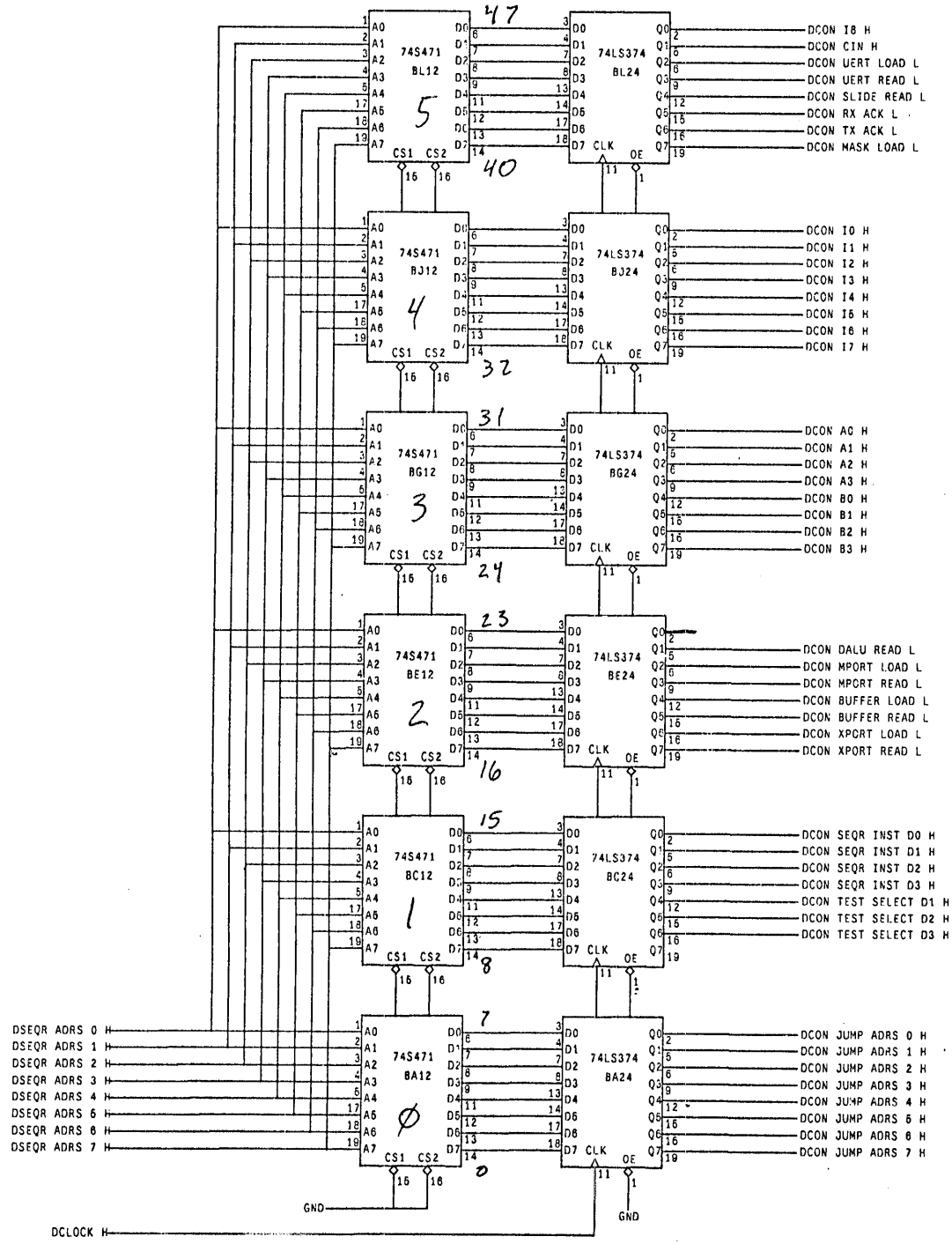

TITLE: DATA I/O BRD, CNTL MEMORY AND PIPELINE REG'S

FILE: DCON1 [MEIGFS]

DATE: 26-Jan-82 15:12

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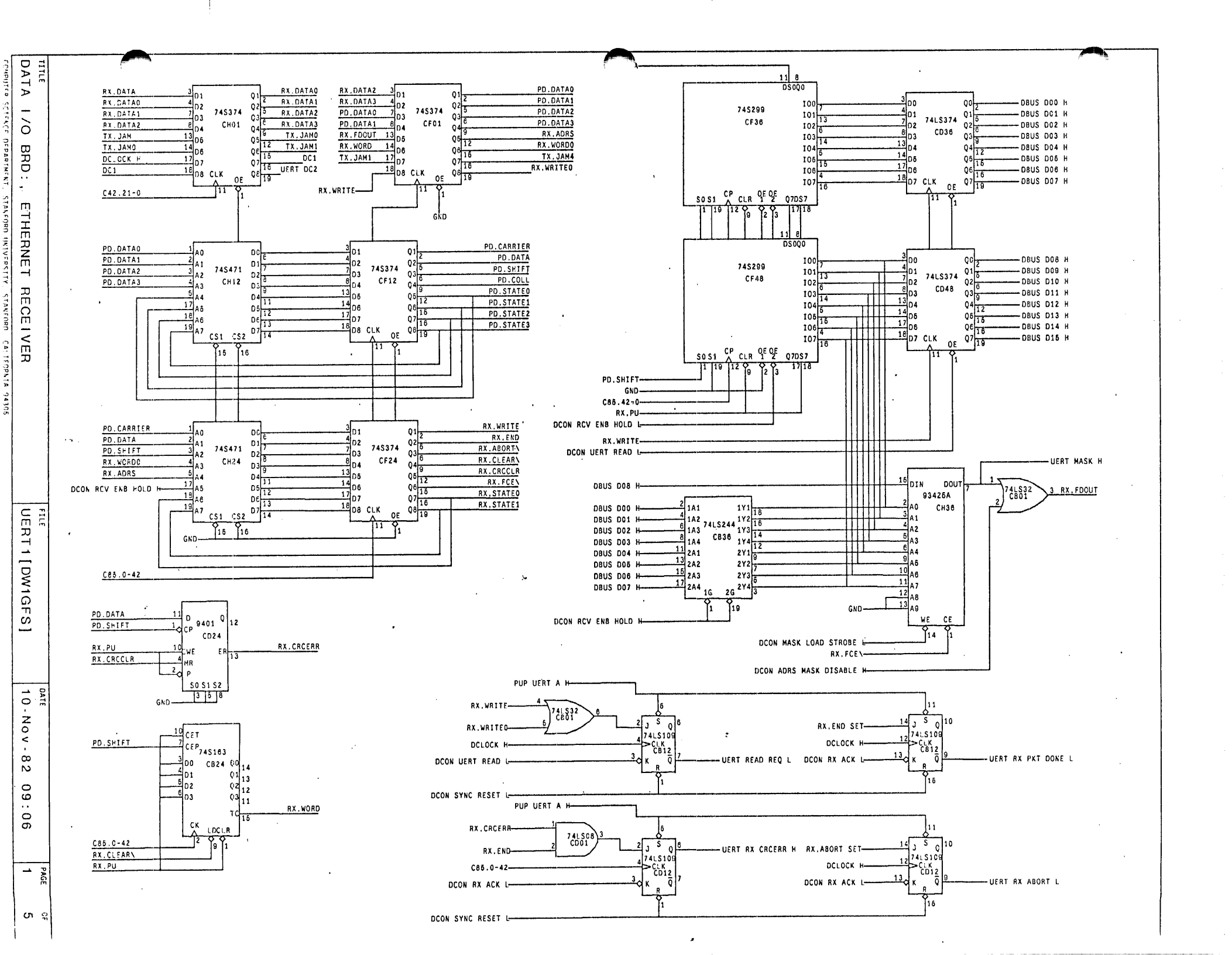
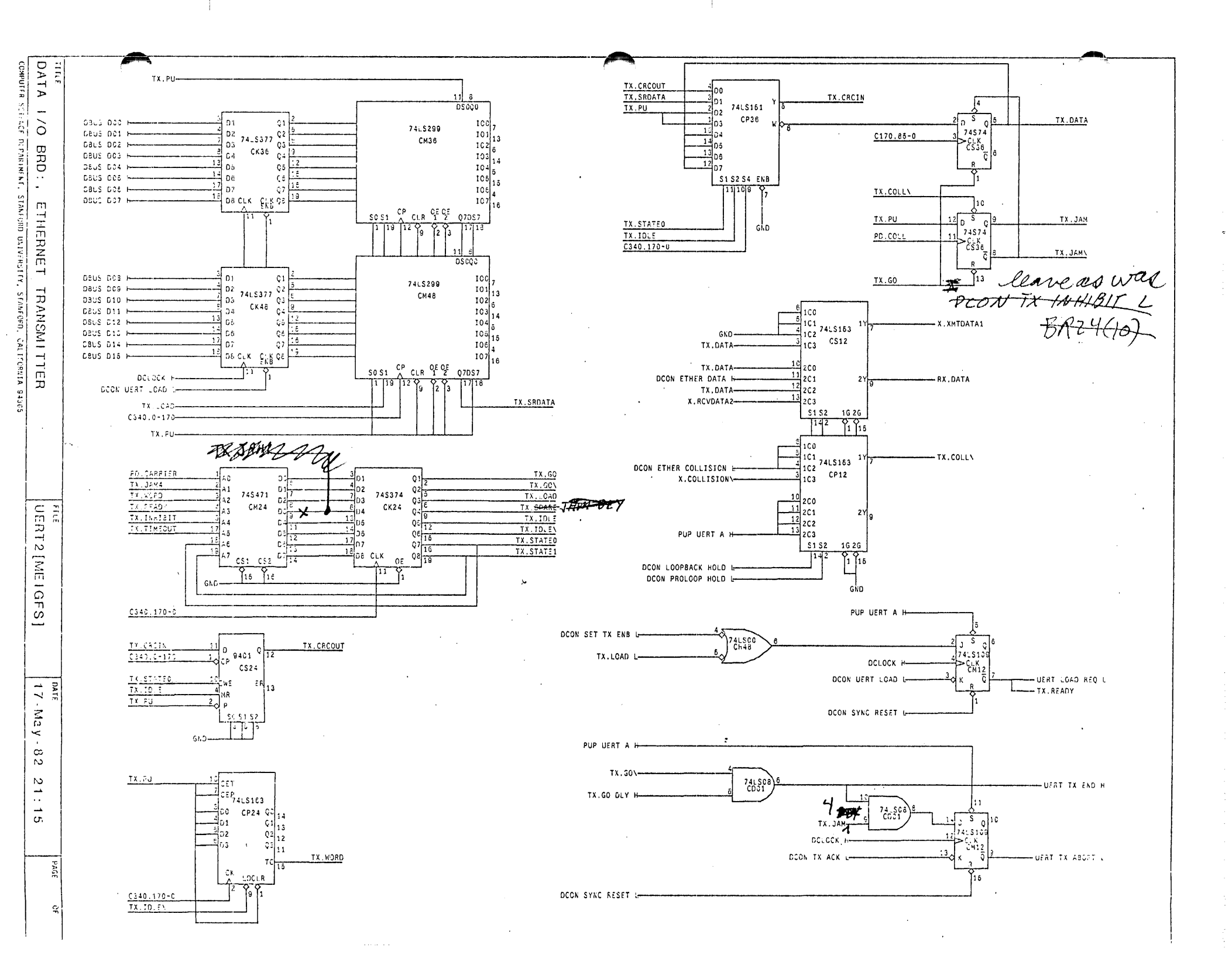
COMPUTER SCIENCE DEPARTMENT, STANFORD UNIVERSITY, STANFORD, CALIFORNIA 94305


COMPUTER SCIENCE DEPARTMENT, STANFORD UNIVERSITY, STANFORD, CALIFORNIA 94305
TITLE
DATA I/O BRD:, ETHERNET RECEIVER
FILE
UERT1[DW1GFS]
DATE
10-Nov-82 09:06
PAGE
1 5 OF
RX.DATA
RX.DATA0
RX.DATA1
RX.DATA2
TX.JAM
TX.JAM0
DC.CCK H
DC1
C42.21-0
74S374 CH01
RX.DATA0
RX.DATA1
RX.DATA2
RX.DATA3
TX.JAM0
TX.JAM1
DC1
UERT DC2
RX.DATA2
RX.DATA3
PD.DATA0
PD.DATA1
RX.FDOUT
RX.WORD
TX.JAM1
RX.WRITE
74S374 CF01
PD.DATA0
PD.DATA1
PD.DATA2
PD.DATA3
RX.ADRS
RX.WORD0
TX.JAM4
RX.WRITE0
GND
PD.DATA0
PD.DATA1
PD.DATA2
PD.DATA3
74S471 CH12
74S374 CF12
PD.CARRIER
PD.DATA
PD.SHIFT
PD.COLL
PD.STATE0
PD.STATE1
PD.STATE2
PD.STATE3
PD.CARRIER
PD.DATA
PD.SHIFT
RX.WORD0
RX.ADRS
DCON RCV ENB HOLD H
74S471 CH24
74S374 CF24
RX.WRITE
RX.END
RX.ABORT\
RX.CLEAR\
RX.CRCCLR
RX.FCE\
RX.STATE0
RX.STATE1
GND
C86.0-42
74S299 CF36
74S299 CF48
DS0Q0
SO S1 CP CLR OE OE Q7DS7
74LS374 CD36
74LS374 CD48
DBUS D00 H
DBUS D01 H
DBUS D02 H
DBUS D03 H
DBUS D04 H
DBUS D05 H
DBUS D06 H
DBUS D07 H
DBUS D08 H
DBUS D09 H
DBUS D10 H
DBUS D11 H
DBUS D12 H
DBUS D13 H
DBUS D14 H
DBUS D15 H
PD.SHIFT
GND
C86.42-0
RX.PU
DCON RCV ENB HOLD L
RX.WRITE
DCON UERT READ L
DBUS D08 H
DBUS D00 H
DBUS D01 H
DBUS D02 H
DBUS D03 H
DBUS D04 H
DBUS D05 H
DBUS D06 H
DBUS D07 H
74LS244 CB36
1G 2G
DCON RCV ENB HOLD H
93426A CH36
DIN DOUT
WE CE
UERT MASK H
74LS32 CB01
3 RX.FDOUT
GND
DCON MASK LOAD STROBE L
RX.FCE\
DCON ADRS MASK DISABLE H
PD.DATA
PD.SHIFT
RX.PU
RX.CRCCLR
9401 CD24
CP WE MR P
S0 S1 S2
ER
RX.CRCERR
GND
PD.SHIFT
74S163 CB24
CET CEP
D0 D1 D2 D3
Q0 Q1 Q2 Q3
TC
CK LDCLR
RX.WORD
C86.0-42
RX.CLEAR\
RX.PU
PUP UERT A H
RX.WRITE
RX.WRITE0
74LS32 CB01
74LS109 CB12
DCLOCK H
DCON UERT READ L
UERT READ REQ L
DCON SYNC RESET L
RX.END SET
DCON RX ACK L
UERT RX PKT DONE L
PUP UERT A H
RX.CRCERR
RX.END
C86.0-42
DCON RX ACK L
74LSC8 CD01
74LS109 CD12
UERT RX CRCERR H
DCON SYNC RESET L
RX.ABORT SET
DCON RX ACK L
UERT RX ABORT L


TITLE
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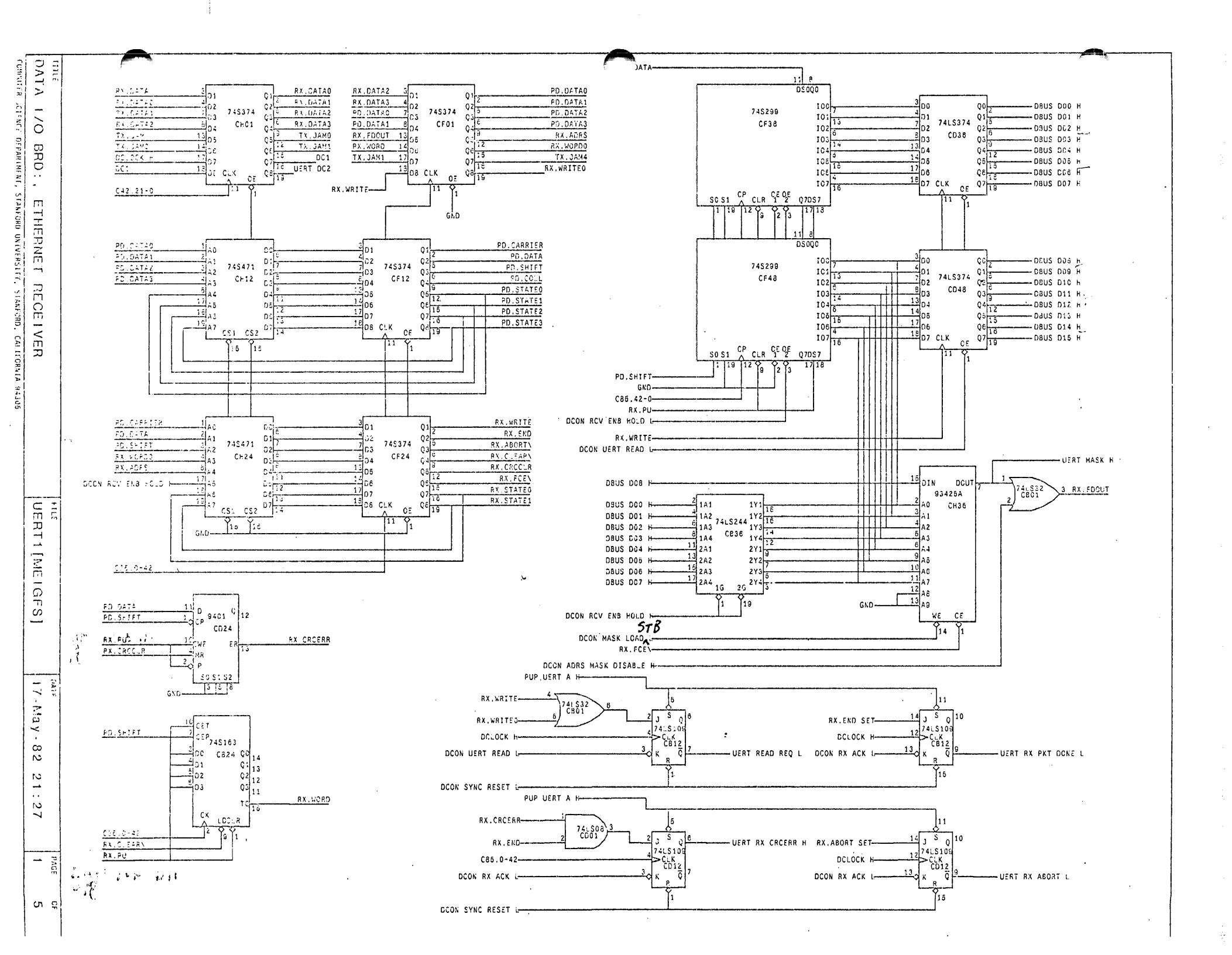
FILE
UERT2[MEIGFS]
DATE
17-May-82 21:15
PAGE
OF
COMPUTER SCIENCE DEPARTMENT, STANFORD UNIVERSITY, STANFORD, CALIFORNIA 94305
TX.PU
DBUS D00
DBUS D01
DBUS D02
DBUS D03
DBUS D04
DBUS D05
DBUS D06
DBUS D07
74LS377 CK36
74LS299 CM36
DBUS D08
DBUS D09
DBUS D10
DBUS D11
DBUS D12
DBUS D13
DBUS D14
DBUS D15
74LS377 CK48
74LS299 CM48
DCLOCK H
DCON UERT LOAD L
TX.LOAD
C340.0-170
TX.SRDATA
TX.PU
PD.CARRIER
TX.JAM4
TX.WORD
TX.READY
TX.INHIBIT
TX.TIMEOUT
74S471 CM24
74S374 CK24
TX.GO
TX.GO\
TX.LOAD
TX.SPARE
TX.IDLE
TX.IDLE\
TX.STATE0
TX.STATE1
GND
C340.170-0
TX.CRCIN
C340.0-170
TX.STATE0
TX.IDLE
TX.PU
9401 CS24
TX.CRCOUT
GND
TX.PU
74LS163 CP24
TX.WORD
C340.170-0
TX.IDLE
TX.CRCOUT
TX.SRDATA
TX.PU
74LS161 CP36
TX.CRCIN
TX.STATE0
TX.IDLE
C340.170-0
GND
C170.85-0
74S74 CS36
TX.DATA
TX.COLL\
TX.JAM
TX.JAM\
PD.COLL
TX.GO
leave as was
DCON TX INHIBIT L
BR24(10)
74LS163 CS12
X.XMTDATA1
GND
TX.DATA
TX.DATA
DCON ETHER DATA H
TX.DATA
X.RCVDATA2
RX.DATA
74LS163 CP12
TX.COLL\
DCON ETHER COLLISION L
X.COLLISION\
PUP UERT A H
DCON LOOPBACK HOLD L
DCON PROLOOP HOLD L
GND
PUP UERT A H
DCON SET TX ENB L
TX.LOAD L
74LS00 CH48
DCLOCK H
DCON UERT LOAD L
74LS109 CM12
UERT LOAD REQ L
TX.READY
DCON SYNC RESET L
PUP UERT A H
TX.GO\
TX.GO DLY H
74LS08 CD31
UERT TX END H
TX.JAM
74S08 CD31
DCLOCK H
DCON TX ACK L
74LS109 CM12
UERT TX ABORT L
DCON SYNC RESET L


TITLE
DATA I/O BRD: ETHERNET RECEIVER
TITLE
UERT1 [MEIGFS]
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17-May-82 21:27
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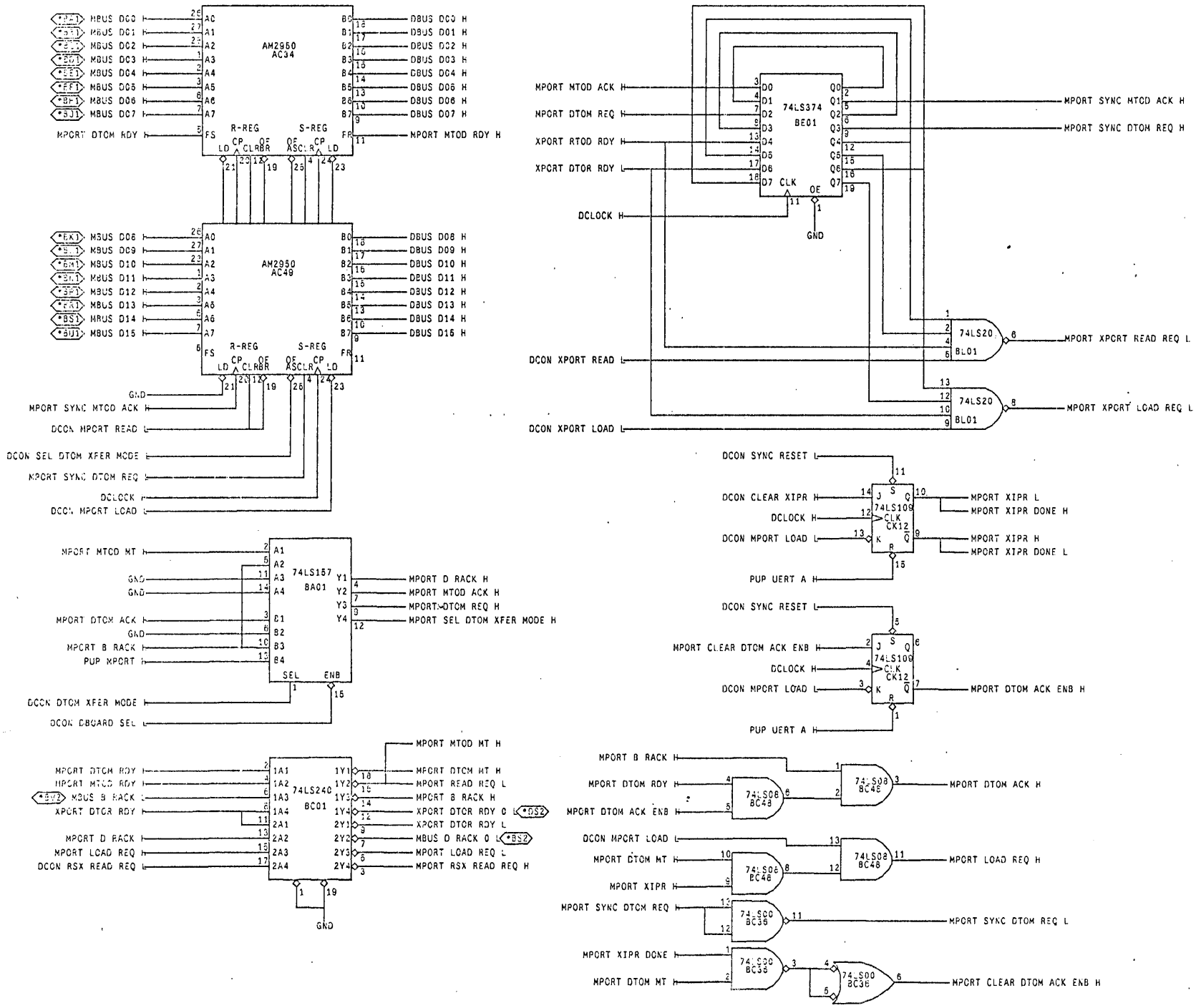
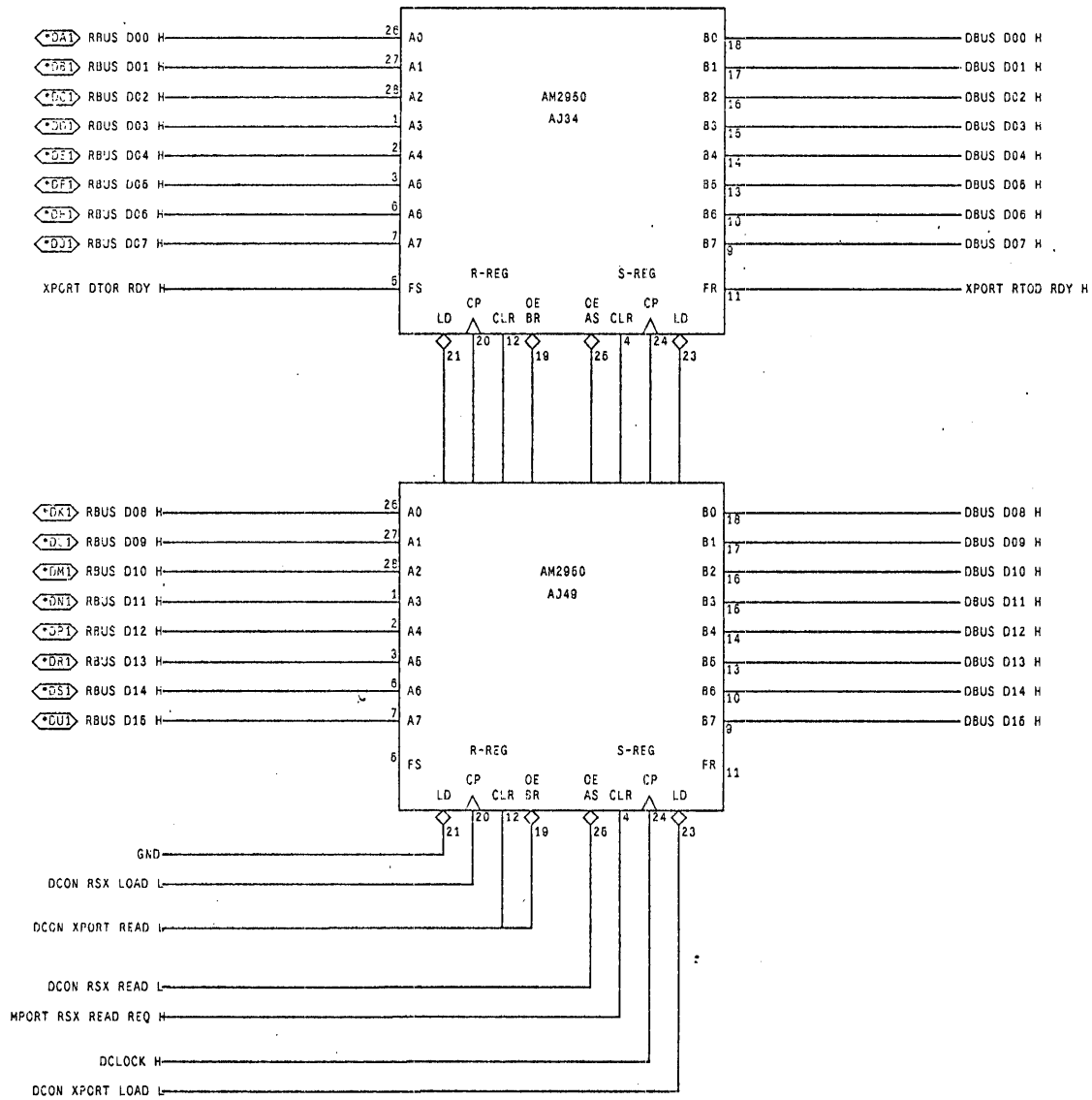
COMPUTER SCIENCE DEPARTMENT, STANFORD UNIVERSITY, STANFORD, CALIFORNIA 94305
74S374 CH01
74S374 CF01
74S471 CH12
74S374 CF12
74S471 CH24
74S374 CF24
74S299 CF38
74S299 CF48
74LS374 CD38
74LS374 CD48
74LS244 CB36
93425A CH36
9401 CD24
74S163 CB24
74LS32 CB01
74LS08 CC01
74LS109 CB12
RX.DATA0
RX.DATA1
RX.DATA2
RX.DATA3
TX.JAM0
TX.JAM1
DC1
UERT DC2
RX.WRITE
GND
PD.DATA0
PD.DATA1
PD.DATA2
PD.DATA3
RX.ADRS
RX.WORD0
TX.JAM4
RX.WRITE0
C42.21-0
PD.CARRIER
PD.DATA
PD.SHIFT
PD.COLL
PD.STATE0
PD.STATE1
PD.STATE2
PD.STATE3
RX.END
RX.ABORT\
RX.C_FAP\
RX.CRCCLR
RX.FCE\
RX.STATE0
RX.STATE1
DCON RCV ENB HOLD L
C42.0-42
DATA
DS0Q0
DBUS D00 H
DBUS D01 H
DBUS D02 H
DBUS D03 H
DBUS D04 H
DBUS D05 H
DBUS D06 H
DBUS D07 H
DBUS D08 H
DBUS D09 H
DBUS D10 H
DBUS D11 H
DBUS D12 H
DBUS D13 H
DBUS D14 H
DBUS D15 H
C86.42-0
RX.PU
RX.WRITE
DCON UERT READ L
UERT MASK H
RX.FDOUT
DCON ADRS MASK DISABLE H
DCON MASK LOAD
STB
PUP.UERT A H
DCLOCK H
DCON SYNC RESET L
UERT READ REQ L
RX.END SET
DCON RX ACK L
UERT RX PKT DONE L
RX.CRCERR
UERT RX CRCERR H
RX.ABORT SET
UERT RX ABORT L

COMPUTER SCIENCE DEPARTMENT, STANFORD UNIVERSITY, STANFORD, CALIFORNIA 94305





TITLE: DATA I/O BRD: , RBUS TRANSCEIVER PORT

FILE: XPORT[MEIGFS]

DATE: 23-Oct-81 10:30

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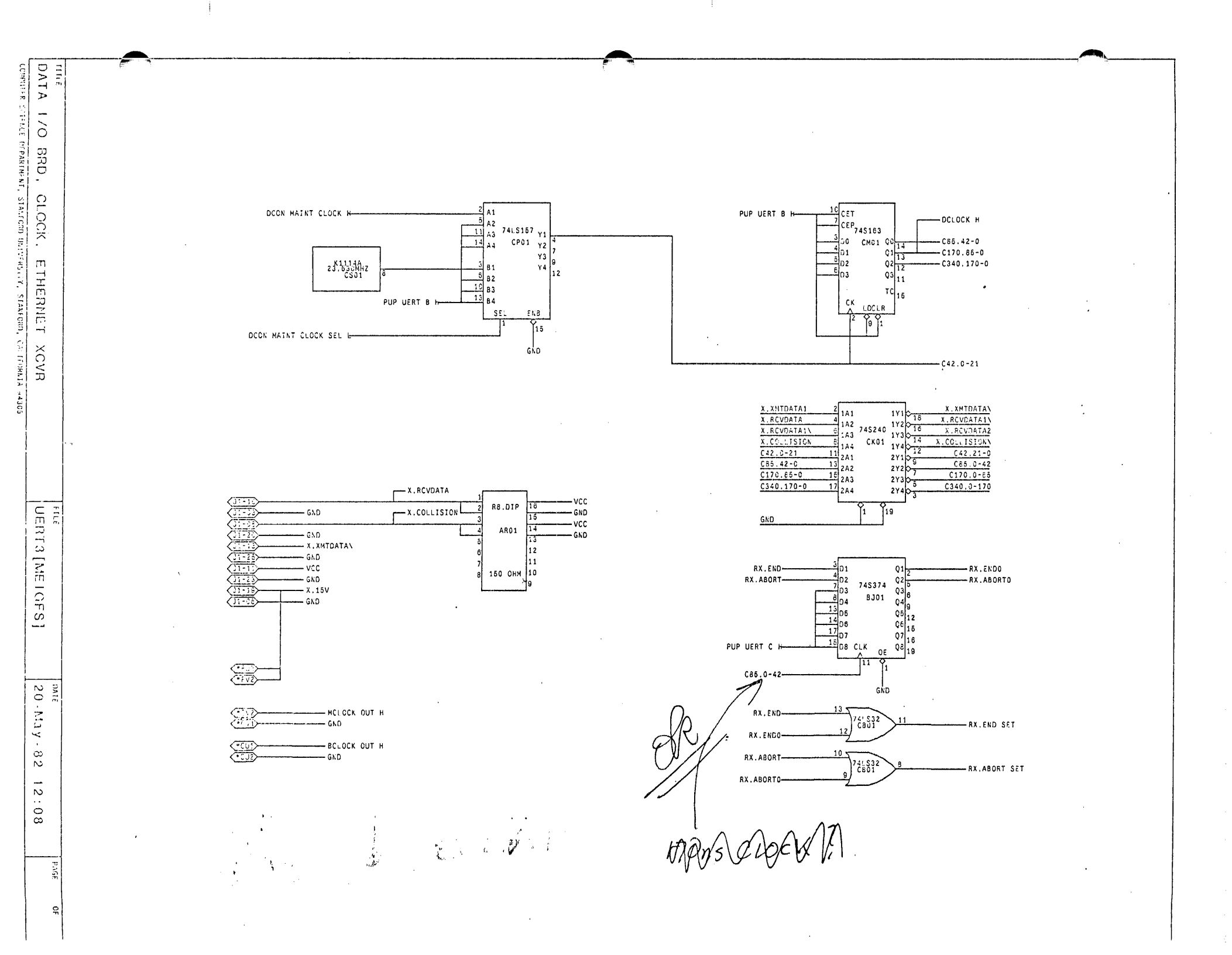
COMPUTER SCIENCE DEPARTMENT, STANFORD UNIVERSITY, STANFORD, CALIFORNIA 94305



TITLE	DATA I/O BRD, CLOCK, ETHERNET XCVR
FILE	UERT3[MEICFS]
DATE	20-May-82 12:08
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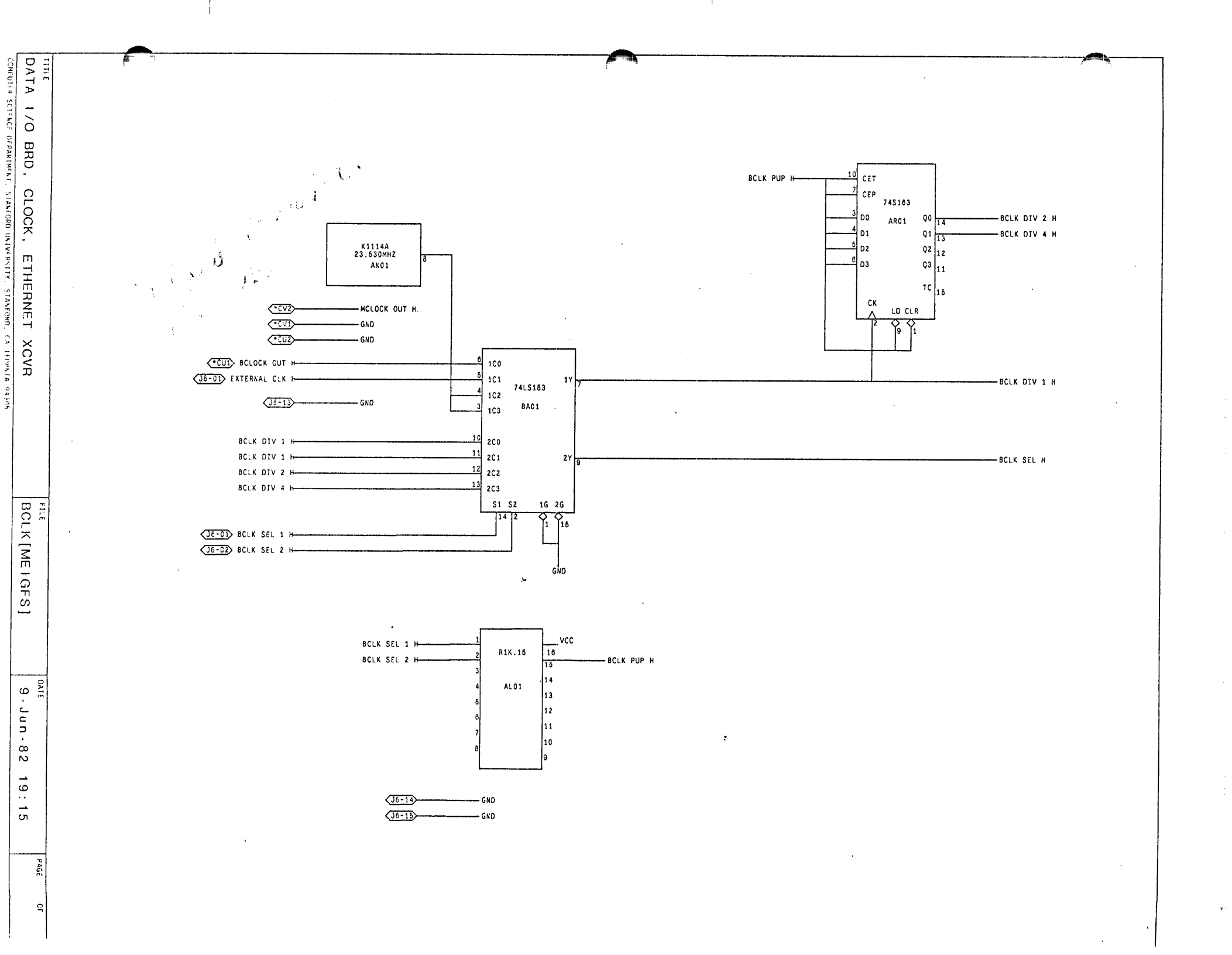

TITLE
DATA I/O BRD, CLOCK, ETHERNET XCVR

FILE
BCLK[MEIGFS]

DATE
9-Jun-82 19:15

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OF

DUAL-WIDTH DEC BOARD PINOUTS

BOARD NAME: DATA BOARD

COLUMN (A,C,E): A

Signal Name					Signal Name
	1	A	2		+5
	1	B	2		-15
	1	C	2		GND
	1	D	2		
	1	E	2		
	1	F	2		
	1	H	2		
	1	J	2		
	1	K	2		
	1	L	2		
	1	M	2		
	1	N	2		
	1	P	2		
	1	R	2		
	1	S	2		
GND	1	T	2		
	1	U	2		
	1	V	2		

COLUMN (B,D,F): B

Signal Name					Signal Name
MBUS DØØ H	1	A	2		+5
DØ1	1	B	2		-15
DØ2	1	C	2		GND
DØ3	1	D	2		DMAX RESET OUT L
DØ4	1	E	2		RCON MBC WRITE MODE L
DØ5	1	F	2		RCON GO L
DØ6	1	H	2		
DØ7	1	J	2		
DØ8	1	K	2		
DØ9	1	L	2		
DIØ	1	M	2		DCON END READ L
DI1	1	N	2		DMAX EOP ACK L
DI2	1	P	2		
DI3	1	R	2		
DI4	1	S	2		MBUS TRANSFER REQ L
GND	1	T	2		
DI5	1	U	2		
	1	V	2		INBUS TRANSFER ACK L

name change

OUTPUT

OUTPUT

DUAL-WIDTH DEC BOARD PINOUTS

BOARD NAME: DATA

ROW (A,C,F) C

Signal Name					Signal Name
DCON NX PACKET AVAIL H	1	A	2		+5 V
BOARD INSTALLED L	1	B	2		-15 V
DCON NX OVERFLOW H	1	C	2		GND
DCON TX BUFFER AVAIL H	1	D	2		MAINT DBOARD SEL L
DCON TX BUSY H	1	E	2		
DCON ETHER CARRIER H	1	F	2		MAINT CLOCK ENB L
DCON TX RCV ERR L	1	H	2		MAINT CLOCK L
	1	J	2		MAINT LOOPBACK L
	1	K	2		MAINT ADRS MASK DISABLE L
	1	L	2		MAINT RCV DISABLE L
	1	M	2		MAINT ETHER DATA L
	1	N	2		MAINT ETHER COLLISION L
	1	P	2		MAINT PRO LOOP L
	1	R	2		MAINT DIAG PROG SEL 0 H
DCON BOARD INSTALLED L (GND)	1	S	2		MAINT DIAG PROG SEL 1 H
GND	1	T	2		
BCLOCK OUT H	1	U	2		GND
GND	1	V	2		MCLOCK OUT H

ROW (B,D,F) D

Signal Name					Signal Name
RBUS D00 H	1	A	2		+5 V
D01	1	B	2		-15 V
D02	1	C	2		GND
D03	1	D	2		BMODE DBOARD SEL L
D04	1	E	2		
D05	1	F	2		RCON RCV PAKT ENB L
D06	1	H	2		
D07	1	J	2		RCON DPC READ L
D08	1	K	2		RCON XPORT READ L
D09	1	L	2		RCON XPORT LOAD L
D10	1	M	2		RCON XPORT READ REQ L
D11	1	N	2		RCON REQ SEL 0 L
D12	1	P	2		1
D13	1	R	2		2
D14	1	S	2		XPORT DTON RDY L
GND	1	T	2		
D15	1	U	2		
	1	V	2		

DUAL-WIDTH DEC BOARD PINOUTS

BOARD NAME: DATA

ROW (A,C,E) C

Signal Name				Signal Name
	1	A	2	+5 V
	1	B	2	-15 V
	1	C	2	GND
	1	D	2	
	1	E	2	
	1	F	2	
	1	H	2	
	1	J	2	
	1	K	2	
	1	L	2	
	1	M	2	
	1	N	2	
	1	P	2	
	1	R	2	
	1	S	2	
GND	1	T	2	
	1	U	2	
	1	V	2	

ROW (B,D,F) F

Signal Name				Signal Name
	1	A	2	+5 V
	1	B	2	-15 V
	1	C	2	GND
	1	D	2	
	1	E	2	
	1	F	2	
	1	H	2	
	1	J	2	
	1	K	2	
	1	L	2	
	1	M	2	
	1	N	2	
	1	P	2	-5V (FOR ECL)
	1	R	2	-5V (FOR ECL)
	1	S	2	
GND	1	T	2	
	1	U	2	+15V (FOR XCVR)
	1	V	2	+15V (FOR XCVR)

21 rows x 5 ICs = 105
3 rows x 4 ICs = 12
117

43 rows of 62 pins
6 rows of 50 pins

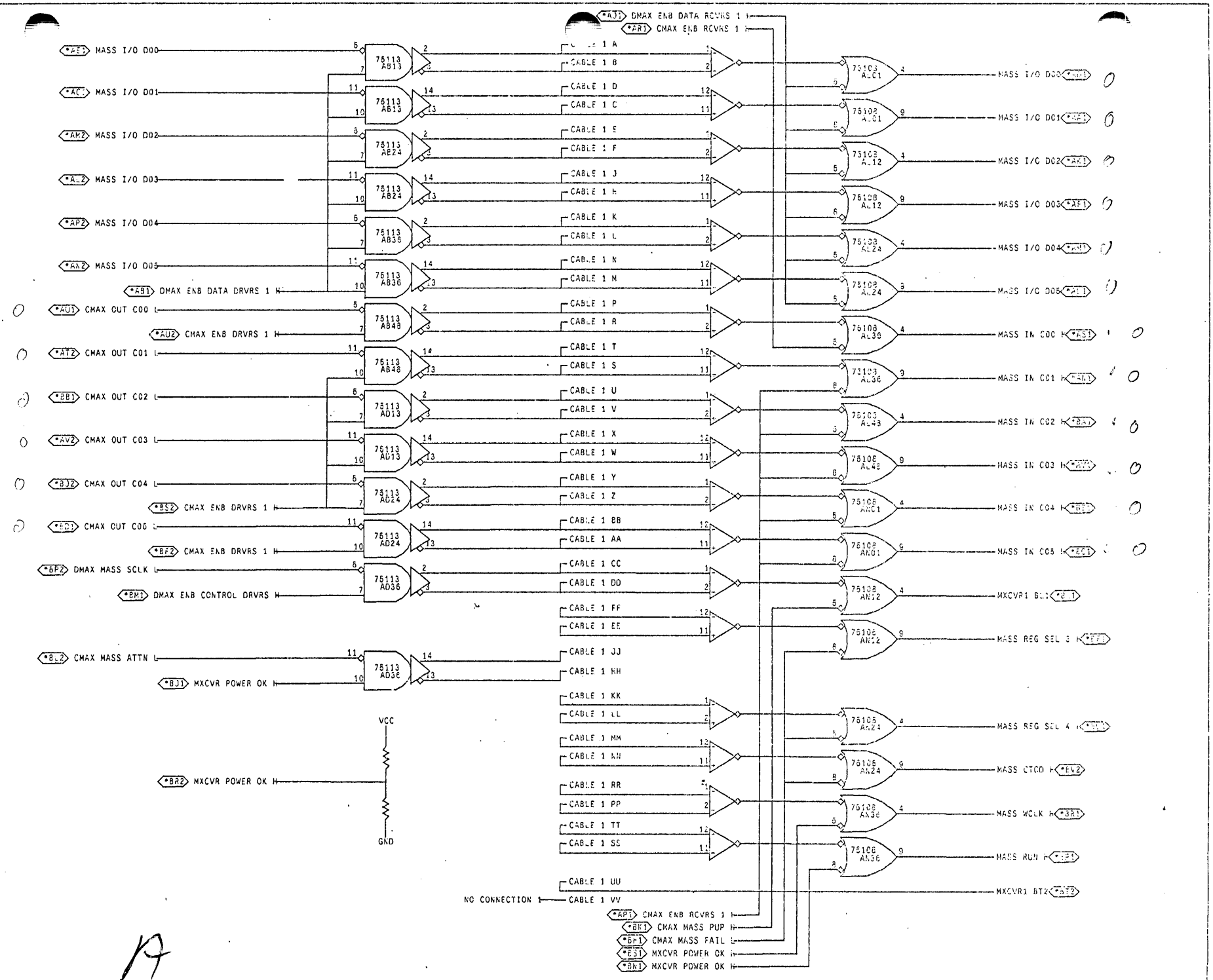
A

LS00 DSEQN2	LS157 MX	2950 MX	2950 MX	
LS148 DSEQN2	LS148 DSEQN2	LS374 MX	LS240 MX	
LS153 0-1	LS153 4-5	~~LS00~~		
↕ DSEQN1 ↕		XPORT	XPORT	
MIK.15 DSEQN2	LS153 2-3	LS153 6-7	~~LS148~~	~~LS148~~
~~74S00~~ LS153 DSEQN1	LS151 DSEQN1	LS151 DSEQN1	2016	2016
MIK.15 DSEQN1	RPAK	29811 DSEQN1		
LS244 DSEQN2	2911 DSEQN1	2911 DSEQN1	2016	2016
	S471 DCON1	LS374 DCON1	LS377 BUFFER	LS377 BUFFER
	S471 DCON1	LS374 DCON1	LS374 DALU	LS374 DALU
	S471 DCON1	LS374 DCON1	LS374 DALU	2902 DALU
	S471 DCON1	LS374 DCON1		
	S471 DCON1	LS374 DCON1	2901	
	S471 DCON1	LS374 DCON1	2901	
	S471 DCON2	8613 DCON2		
	LS151 DCON2	8613 DCON2	2901	
	LS153 DCON2	LS377 DCON2	2901	
LS244 DCON2				

0-7 8-15

LS32 UERT1	LS74 UERT1	LS163 UERT1	LS244 UERT1	LS240 DCON2
APP2 UERT3	LS74 UERT1	9401 UERT1	LS374 UERT1	LS374 UERT1
S374 UERT1	S374 UERT1	S374 UERT1	LS299 UERT1	LS299 UERT1
S374 UERT1	S471 UERT1	S471 UERT1	93425 UERT1	LS240 DCON2
LS240 UERT3	LS74 UERT2	S374 UERT2	LS374 UERT2	LS374 UERT2
[illegible] UERT3	LS74 UERT2	S471 UERT2	LS299 UERT2	LS299 UERT2
LS157 UERT2	LS153 UERT2	LS163 UERT2	LS151 UERT	
[illegible] UERT3	LS153 UERT2	9401 UERT2	LS08 UERT1&2	VPFC UERT3

1 10 (12) (24) (36) (48) 60 62



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FILE: MXCVR1[MEIGFS]

DATE: 28-Apr-81 17:03

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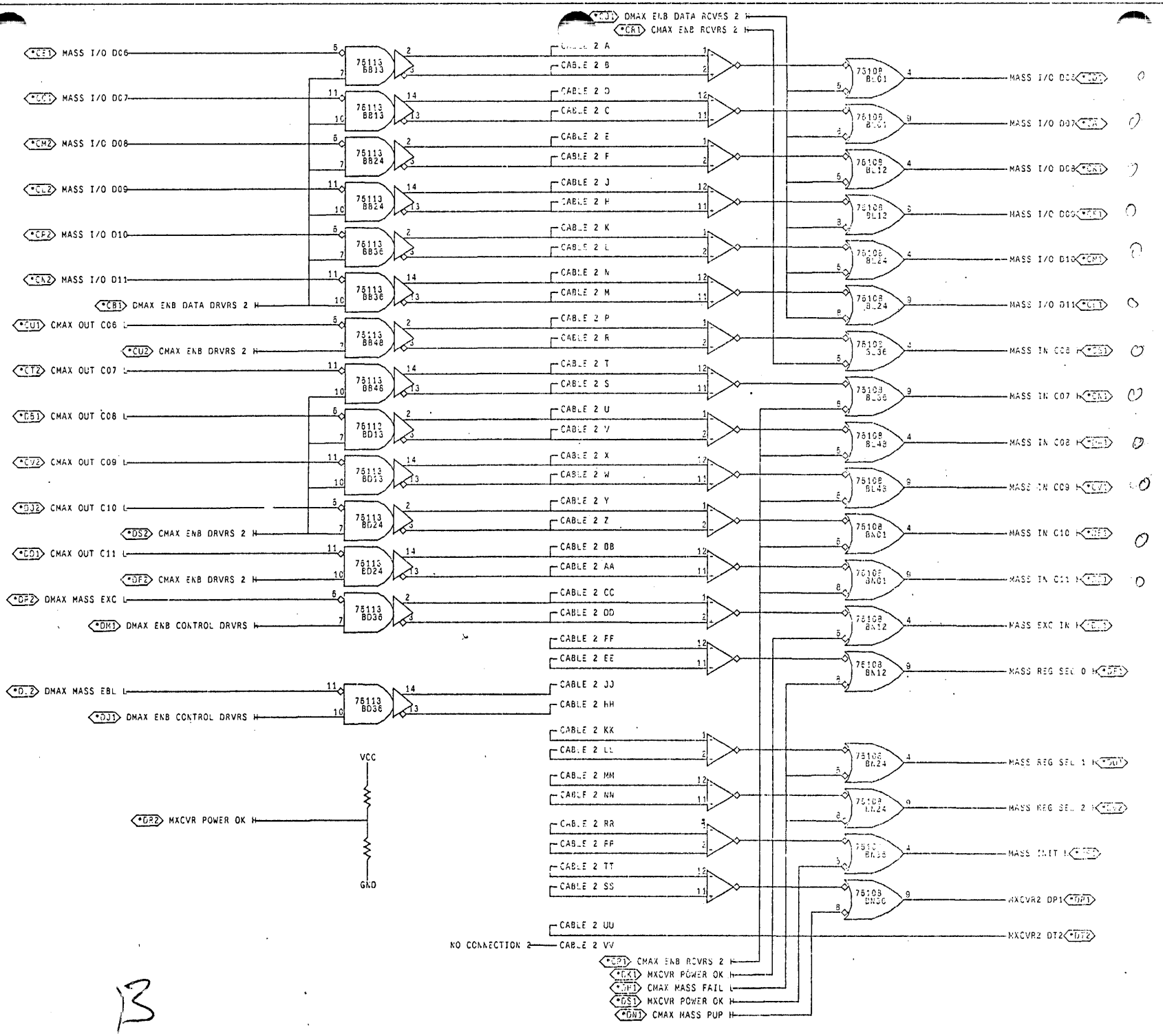

13

TITLE: M5903 MASSBUS TRANSCEIVER,

FILE: MXCVR2 [MEIGFS]

DATE: 28-Apr-81 18:33

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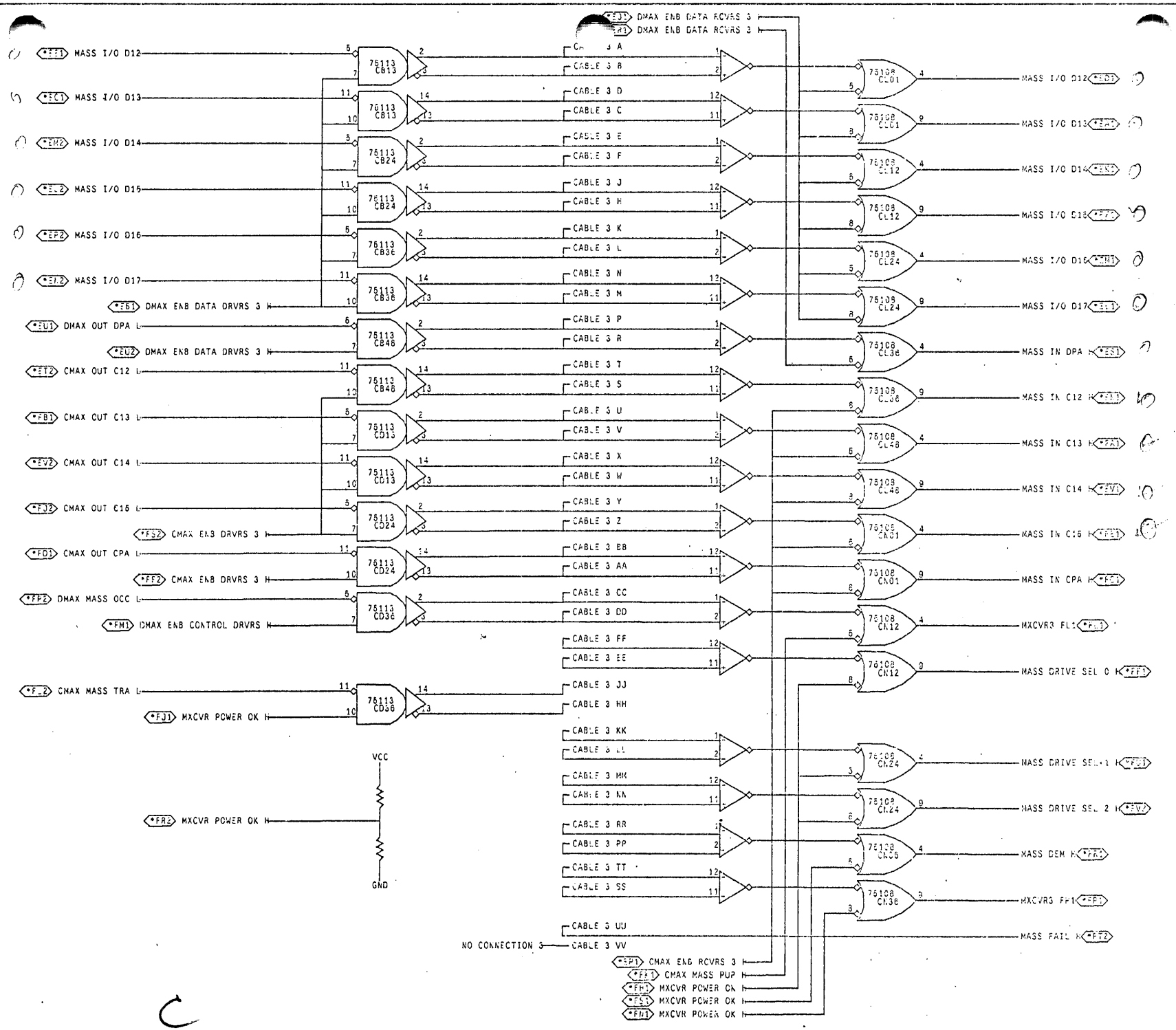


BACKPLANE INTERCONNECTS

BOARD NAME: _____

SLOT: E

ROW: Ø1

(E3)

	PIN	SIDE	Signal Name	SLOT	ROW	PIN	SIDE	Signal Name
D	A	1	TCØ DI 13 A H (MASS D13)	4	E	A	1	MASS IN D13 H
D	B	1	DP1 SYNC TRAN EN A H	2	E	B	1	DABS MASS TRANSMIT H
D	C	1	SN2 BUF 13 L (MASS D13)	4	E	C	1	BRL OUT D13 L
D	D	1	TCØ DI 12 A H (MASS D12)	4	E	D	1	MASS IN D12 H
D	E	1	SN2 BUF 12 L (MASS D12)	4	E	E	1	BRL OUT D12 L
D	F	1	TCØ DI 15 A H (MASS D15)	4	E	F	1	MASS IN D15 H
—	H	1	X	X	X	X	X	X
D	J	1	DP1 SYNC REC EN A H	2	E	J	1	DABS MASS RECEIVE H
D	K	1	TCØ DI 14 A H (MASS D14)	4	E	K	1	MASS IN D14 H
D	L	1	TCØ DI 17 A H (MASS D17)	4	E	L	1	MASS IN D17 H
D	M	1	TCØ DI 16 A H (MASS D16)	4	E	M	1	MASS IN D16 H
C	N	1	TCØ C12 A H (MASS C12)	2	E	N	1	MASS IN C12 H
C	P	1	DP3 REC CONT EN A H	2	E	P	1	CMAX MASS RECEIVE H
D	R	1	DP1 SYNC REC EN A H	2	E	R	1	DABS MASS RECEIVE H
—	S	1	TCØ PARITY SYNC A H (MASS DPA)	4	E	S	1	MASS IN DPA H
—	T	1	GND	←			→	GND
D	U	1	SN4 ODD BUF PAR L (MASS DPA)	4	E	U	1	BRL OUT DPA L
C	V	1	TCØ C14 A H (MASS C14)	2	E	V	1	MASS IN C14 H

	PIN	SIDE	Signal Name	SLOT	ROW	PIN	SIDE	Signal Name
—	A	2	+5	←			→	+5
—	B	2	-15	←			→	-15
—	C	2	GND	←			→	GND
—	D	2	X	X	X	X		X
—	E	2	X	X	X	X		X
—	F	2	X	X	X	X		X
—	H	2	X	X	X	X		X
—	J	2	X	X	X	X		X
—	K	2	X	X	X	X		X
D	L	2	SN2 BUF 15 L (MASS D15)	4	E	L	2	BRL OUT D15 L
D	M	2	SN2 BUF 14 L (MASS D14)	4	E	M	2	BRL OUT D14 L
D	N	2	SN2 BUF 17 L (MASS D17)	4	E	N	2	BRL OUT D17 L
D	P	2	SN2 BUF 16 L (MASS D16)	4	E	P	2	BRL OUT D16 L
—	R	2	X	X	X	X		X
—	S	2	X	X	X	X		X
C	T	2	DPØ TC 12 AB (MASS C12)	2	E	T	2	CMAX OUT C12 L
D	U	2	DP1 SYNC TRAN EN A H	2	E	U	2	DABS MASS TRANSMIT H
C	V	2	DPØ TC 14 AB (MASS C14)	2	E	V	2	CMAX OUT C14 L

BACKPLANE INTERCONNECTS

BOARD NAME: _____

SLOT: F

ROW: ØI

(F3)

PIN	SIDE	Signal Name	SLOT	ROW	PIN	SIDE	Signal Name
A	1	TCØ C13 A H (MASS C13)	2	F	A	1	MASS IN C13 H
B	1	DPØ TC 13 AB (MASS C13)	2	F	B	1	CMAX OUT C13 L
C	1	TCØ PARITY BUS A H (MASS CPA)	2	F	C	1	MASS IN CPA H
D	1	DPI PARITY BUS A L (MASS CPA)	2	F	D	1	CMAX OUT CPA L
E	1	TCØ C15 A H (MASS C15)	2	F	E	1	MASS IN C15 H
F	1	TCØ DRV SEL AØØ H (MASS DSØ)	2	F	F	1	MASS DRV SEL Ø H
H	1	PMØ POWER OK H	2	F	H	1	DABS POWER OK H
J	1	PMØ POWER OK H	2	F	J	1	DABS POWER OK H
K	1	—	—	—	—	—	—
L	1	—	—	—	—	—	—
M	1	DPI TRACEV EN A H	2	F	M	1	DMAX MASS CONTROL ENB H
N	1	PMØ POWER OK H	2	F	N	1	DABS POWER OK H
P	1	—	—	—	—	—	—
R	1	TCØ DEMAND BUS A H (MASS DEM)	2	F	R	1	MASS DEM H
S	1	PMØ POWER OK H	2	F	S	1	DABS POWER OK H
T	1	GND	←		→		GND
U	1	TCØ DRV SEL AØI H (MASS DSI)	2	F	U	1	MASS DRV SEL I H
V	1	X	X	X	X	X	X

PIN	SIDE	Signal Name	SLOT	ROW	PIN	SIDE	Signal Name
A	2	+5	←		→		+5
B	2	-15	←		→		-15
C	2	GND	←		→		GND
D	2	X	X	X	X	X	X
E	2	X	X	X	X	X	X
F	2	DP3 PARITY EN A H	2	F	F	2	CMAX MASS TRANSMIT H
H	2	X	X	X	X	X	X
J	2	DPØ TC 15 AB (MASS C15)	2	F	J	2	CMAX OUT C15 L
K	2	X	X	X	X	X	X
L	2	DP3 TRANSFER AØØ H (MASS TRA)	2	F	L	2	CMAX MASS TRA L
M	2	X	X	X	X	X	X
N	2	X	X	X	X	X	X
P	2	RG3 PMT DATA COM L (MASS PCC)	2	F	P	2	DABS MASS OCC L
R	2	PMØ POWER OK H	2	F	R	2	DABS POWER OK H
S	2	DP3 TRAS A EN H	2	F	S	2	CMAX MASS TRANSMIT H
T	2	TCØ MASS FAIL A H (MASS FAIL A)	2	F	T	2	MASS FAIL H
U	2	X	X	X	X	X	X
V	2	TCØ DRV SEL AØ2 H (MASS DS2)	2	F	V	2	MASS DRV SEL 2 H

DUAL-WIDTH DEC BOARD PINOUTS

BOARD NAME: M5903

IN = DATA INTO M5903, TO MASSBUS
OUT = DATA FROM MASSBUS, FROM M5903

COLUMN (A,C,E): A

Signal Name	1		2	Signal Name
DATA OUT 2	1	A	2	+5
TRANS ENAB COM 1 (1-6)	1	B	2	-15
DATA IN 2	1	C	2	GND
DATA OUT 1	1	D	2	—
DATA IN 1	1	E	2	—
DATA OUT 4	1	F	2	—
—	1	H	2	—
REC ENAB COM 1 (1-6)	1	J	2	—
DATA OUT 3	1	K	2	—
DATA OUT 6	1	L	2	DATA IN 4
DATA OUT 5	1	M	2	DATA IN 3
DATA OUT 8	1	N	2	DATA IN 6
REC ENAB COM 3 (8-12)	1	P	2	DATA IN 5
REC ENAB COM 2 (7)	1	R	2	—
DATA OUT 7	1	S	2	—
GND	1	T	2	DATA IN 8
DATA IN 7	1	U	2	TRANS ENAB COM 2 (7)
DATA OUT 10	1	V	2	DATA IN 10

COLUMN (B,D,F): B

Signal Name	1		2	Signal Name
DATA OUT 9	1	A	2	+5
DATA IN 9	1	B	2	-15
DATA OUT 12	1	C	2	GND
DATA IN 12	1	D	2	—
DATA OUT 11	1	E	2	—
DATA OUT 14	1	F	2	TCPA (12)
REC ENAB COM 5 (14-16)	1	H	2	—
TRANS ENAB COM 6 (14)	1	J	2	DATA IN 11
REC ENAB COM 4 (13)	1	K	2	—
DATA OUT 13	1	L	2	DATA IN 14
TRANS ENAB COM 5 (13)	1	M	2	—
REC ENAB COM 8 (18)	1	N	2	—
DATA OUT 18	1	P	2	DATA IN 13
DATA OUT 17	1	R	2	BOARD ENAB SWITCH (+3V)
REC ENAB COM 7 (17)	1	S	2	TRANS ENAB COM 3,4 (8-11)
GND	1	T	2	MASS FAIL PULL-UP
DATA OUT 15	1	U	2	—
—	1	V	2	DATA OUT 16

MASSBUS 40-PIN FLATCABLE CONNECTOR

Massbus Connector Number: dA

	Signal Name (1)				Signal Name (2)
A	DATA OUT 2	A 01	02 B		+5V
B	TRANS ENAB COM 1 (1-6)	C 03	04 D		-15V
C	DATA IN 2	E 05	06 F		GND
D	DATA OUT 1	H 07	08 J		
E	DATA IN 1	K 09	10 L		
F	DATA OUT 4	M 11	12 N		
H		P 13	14 R		
J	REC ENAB COM 1 (1-6)	S 15	16 T		
K	DATA OUT 3	U 17	18 V		
L	DATA OUT 6	W 19	20 X		DATA IN 4
M	DATA OUT 5	Y 21	22 Z		DATA IN 3
N	DATA OUT 8	AA 23	24 BB		DATA IN 6
P	REC ENAB COM 3 (8-12)	CC 25	26 DD		DATA IN 5
R	REC ENAB COM 2 (7)	EE 27	28 FF		
S	DATA OUT 7	HH 29	30 JJ		
T	GND	KK 31	32 LL		DATA IN 8
U	DATA IN 7	MM 33	34 NN		TRANS ENAB COM 2 (7)
V	DATA OUT 10	PP 35	36 RR		DATA IN 10
		SS 37	38 TT		
		UU 39	40 VV		

<SIL> Template 64. SIL

MASSBUS 40-PIN FLATCABLE CONNECTOR

Massbus Connector Number: B (F)

	Signal Name 1				Signal Name 2
A	DATA OUT 9	A	01	02 B	+5V
B	DATA IN 9	C	03	04 D	-15V
C	DATA OUT 12	E	05	06 F	GND
D	DATA IN 12	H	07	08 J	
E	DATA OUT 11	K	09	10 L	
F	~~TCPA~~ DATA OUT 14	M	11	12 N	TCPA (12)
H	REC ENAB COM 5 (14) (10)	P	13	14 R	
J	TRANS ENAB COM 6 (14)	S	15	16 T	DATA IN 11
K	~~TRA~~ REC ENAB COM 4 (13)	U	17	18 V	
L	DATA OUT 13	W	19	20 X	DATA IN 14
M	TRANS ENAB COM 5 (13)	Y	21	22 Z	
	REC ENAB COM 8 (18)	AA	23	24 BB	
P	DATA OUT 18	CC	25	26 DD	DATA IN 13
R	DATA OUT 17	EE	27	28 FF	+3V Lowitched
S	REC ENAB COM 7 (17)	HH	29	30 JJ	TRANS ENAB COM 3 (4) (8-11)
T	GND	KK	31	32 LL	MASS FAIL PULL-UP
U	DATA OUT 15	MM	33	34 NN	
V		PP	35	36 RR	DATA OUT 16
		SS	37	38 TT	
		UU	39	40 VV	

BACKPLANE INTERCONNECTS

BOARD NAME: _____

SLOT: D

ROW: Ø1

F2)

	PIN	SIDE	Signal Name	SLOT	ROW	PIN	SIDE	Signal Name
C	A	1	TBØ CØ8 A H (MASS CØ8)	2	D	A	1	MASS IN CØ8 H
C	B	1	DPØ TC Ø8 AB (MASS CØ8)	2	D	B	1	CMAX OUT CØ8 L
C	C	1	TBØ C11 A H (MASS C11)	2	D	C	1	MASS IN C11 H
C	D	1	DPØ TC 11 AB (MAS C11)	2	D	D	1	CMAX OUT C11 L
C	E	1	TBØ C1Ø A H (MASS C1Ø)	2	D	E	1	MASS IN C1Ø H
C	F	1	TBØ REG SEL A ØØ H (MASS RSØ)	2	D	F	1	MASS REG SEL Ø H
C	H	1	DP3 MASS FAIL A L	2	D	H	1	CMAX MASS FAIL L
D	J	1	DPI TRACEV EN A H	2	D	J	1	DABS MASS CONTROL ENB H
C	K	1	PMØ POWER OK H	2	D	K	1	DABS POWER OK H
C	L	1	TBØ EXC A H (MASS EXC)	4	D	L	1	MASS EXC H
D	M	1	DPI TRACEV EN A H	2	D	M	1	CMAX MASS CONTROL ENB H
—	N	1	—	—	—	—	—	—
—	P	1	—	—	—	—	—	—
C	R	1	TBØ INIT BUS A H (MASS INIT)	2	D	R	1	MASS INIT H
C	S	1	PMØ POWER OK H	2	D	S	1	DABS POWER OK H
	T	1	GND	←	—	—	→	GND
C	U	1	TBØ REG SEL A Ø1 H (MASS RS1)	2	D	U	1	MASS REG SEL 1H
—	V	1	X	x	x	x	x	X

	PIN	SIDE	Signal Name	SLOT	ROW	PIN	SIDE	Signal Name
—	A	2	+5	←	—	—	→	+5
—	B	2	-15	←	—	—	→	-15
—	C	2	GND	←	—	—	→	GND
—	D	2	X	x	x	x	x	X
—	E	2	X	x	x	x	x	X
C	F	2	DP3 TRAS A EN H	2	D	F	2	CMAX MASS TRANSMIT H
—	H	2	X	x	x	x	x	X
C	J	2	DPØ TC 1Ø AB (MASS C1Ø)	2	D	J	2	CMAX OUT C1Ø L
—	K	2	X	x	x	x	x	X
D	L	2	SN5 EBL (1) L (MASS EBL)	2	D	L	2	DAB MASS EBL L
—	M	2	X	x	x	x	x	X
—	N	2	X	x	x	x	x	X
D	P	2	SN5 EXC L (MASS EXC)	2	D	P	2	DABS MASS EXC L
	R	2	PMØ POWER OK H	2	D	R	2	DABS POWER OK H
	S	2	DP3 TRAS A EN H	2	D	S	2	CMAX MASS TRANSMIT H
—	T	2	—					—
—	U	2	X					X
C	V	2	TBØ REG SEL A Ø2 H (MASS RS2)	2	D	V	2	MASS REG SEL 2 H

4 D 76, Ø

BACKPLANE INTERCONNECTS

BOARD NAME: _____

SLOT: C

ROW: Ø1

(E2)

PIN	SIDE	Signal Name	SLOT	ROW	PIN	SIDE	Signal Name
A	1	TBØ DI Ø7 A H (MASS DØ7)	4	C	A	1	MASS IN DØ7 H
B	1	DPI SYNC TRAN ENA H	2	C	B	1	DABS MASS TRANSMIT H
C	1	SN2 BUF Ø7 L (MASS DØ7)	4	C	C	1	BRL OUT DØ7 L
D	1	TBØ DI Ø6 A H (MASS DØ6)	4	C	D	1	MASS IN DØ6 H
E	1	SN2 BUF Ø6 L (MASS DØ6)	4	C	E	1	BRL OUT DØ6 L
F	1	TBØ DI Ø9 A H (MASS DØ9)	4	C	F	1	MASS IN DØ9 H
H	1	X	X	X	X	X	X
J	1	DPI SYNC REC ENA H	2	C	J	1	DABS MASS RECEIVE H
K	1	TBØ DI Ø8 A H (MASS DØ8)	4	C	K	1	MASS IN DØ8 H
L	1	TBØ DI 11 A H (MASS D11)	4	C	L	1	MASS IN D11 H
M	1	TBØ DI 1Ø A H (MASS D1Ø)	4	C	M	1	MASS IN D1Ø H
N	1	TBØ CØ7 A H (MASS CØ7)	2	C	N	1	MASS IN CØ7 H
P	1	DP3 REC CONT ENA H	2	C	P	1	CMAX MASS RECEIVE H
R	1	DP3 REC CONT ENA H	2	C	R	1	CMAX MASS RECEIVE H
S	1	TBØ CØ6 A H (MASS CØ6)	2	C	S	1	MASS IN CØ6 H
T	1	GND	←		→		GND
U	1	DPØ TCØ6 A L (MASS CØ6)	2	C	U	1	CMAX OUT CØ6 L
V	1	TBØ CØ9 A H (MASS CØ9)	2	C	V	1	MASS IN CØ9 H

PIN	SIDE	Signal Name	SLOT	ROW	PIN	SIDE	Signal Name
A	2	+5	←		→		+5
B	2	-15	←		→		-15
C	2	GND	←		→		GND
D	2	X	X	X	X	X	X
E	2	X	X	X	X	X	X
F	2	X	X	X	X	X	X
H	2	X	X	X	X	X	X
J	2	X	X	X	X	X	X
K	2	X	X	X	X	X	X
L	2	SN2 BUF Ø9 L (MASS DØ9)	4	C	L	2	BRL OUT DØ9 L
M	2	SN2 BUF Ø8 L (MASS DØ8)	4	C	M	2	BRL OUT DØ8 L
N	2	SN2 BUF 11 L (MASS D11)	4	C	N	2	BRL OUT D11 L
P	2	SN2 BUF 1Ø L (MASS D1Ø)	4	C	P	2	BRL OUT D1Ø L
R	2	X	X	X		X	X
S	2	X	X	X	X	X	X
T	2	DPØ TC Ø7 A L (MASS CØ7)	2	C	T	2	CMAX OUT CØ7 L
U	2	DP3 TRAS A ENH	2	C	U	2	CMAX MASS TRANSMIT H
V	2	DPØ TC Ø9 A L (MASS CØ9)	2	C	V	2	CMAX OUT CØ9 L

(4D 9C M

BACKPLANE INTERCONNECTS

SLOTS
1 = M5903's
2 = R BOARD
4 = D BOARD

BOARD NAME: M5903
SLOT: A
ROW: Ø1
(E1, A1)

X denotes no fanout signal on M5903
— denotes M5903 signal not used
↔ denotes bussed by BB11

PIN	SIDE	Signal Name	SLOT	ROW	PIN	SIDE	Signal Name
A	1	TAØ DI Ø1 A H (MASS DØ1)	4	A	A	1	MASS IN DØ1 H
B	1	DP1 SYNC TRAN EN A H	2	A	B	1	DABS MASS TRANSMIT H
C	1	SN2 BUF Ø1 L (MASS DØ1)	4	A	C	1	BRL OUT DØ1 L
D	1	TAØ DI ØØ A H (MASS DØØ)	4	A	D	1	MASS IN DØØ H
E	1	SN2 BUF ØØ L (MASS DØØ)	4	A	E	1	BRL OUT DØØ L
F	1	TAØ DI Ø3 A H (MASS DØ3)	4	A	F	1	MASS IN DØ3 H
H	1	X	X	X	X	X	X
J	1	DP1 SYNC REC EN A H	2	A	J	1	DABS MASS RECEIVE H
K	1	TAØ DI Ø2 A H (MASS DØ2)	4	A	K	1	MASS IN DØ2 H
L	1	TAØ DI Ø5 A H (MASS DØ5)	4	A	L	1	MASS IN DØ5 H
M	1	TAØ DI Ø4 A H (MASS DØ4)	4	A	M	1	MASS IN DØ4 H
N	1	TAØ CØ1 A H (MASS CØ1)	2	A	N	1	MASS IN CØ1 H
P	1	DP3 REC CONT EN A H	2	A	P	1	CMAX MASS RECEIVE H
R	1	DP3 REC CONT EN A H	2	A	R	1	CMAX MASS RECEIVE H
S	1	TAØ CØØ A H (MASS CØØ)	2	A	S	1	MASS IN CØØ H
T	1	GND	←			→	GND
U	1	DPØ TC ØØ A L (MASS CØØ)	2	A	U	1	CMAX OUT CØØ L
V	1	TAØ CØ3 A H (MASS CØ3)	2	A	V	1	MASS IN CØ3 H

PIN	SIDE	Signal Name	SLOT	ROW	PIN	SIDE	Signal Name
A	2	+5	←			→	+5
B	2	-15	←			→	-15
C	2	GND	←			→	GND
D	2	X	X	X	X	X	X
E	2	X	X	X	X	X	X
F	2	X	X				X
H	2	X	X				X
J	2	X					X
K	2	X					X
L	2	SN2 BUF Ø3 L (MASS DØ3)	4	A	L	2	BRL OUT DØ3 L
M	2	SN2 BUF Ø2 L (MASS DØ2)	4	A	M	2	BRL OUT DØ2 L
N	2	SN2 BUF Ø5 L (MASS DØ5)	4	A	N	2	BRL OUT DØ5 L
P	2	SN2 BUF Ø4 L (MASS DØ4)	4	A	P	2	BRL OUT DØ4 L
R	2	X	X				X
S	2	X					X
T	2	DPØ TC Ø1 A L (MASS CØ1)	2	A	T	2	CMAX OUT CØ1 L
U	2	DP3 TRAS A EN H	2	A	U	2	CMAX MASS TRANSMIT H
V	2	DPØ TC Ø3 A L (MASS CØ3)	2	A	V	2	CMAX OUT CØ3 L

BACKPLANE INTERCONNECTS

BOARD NAME: _____

SLOT: B

ROW: Ø4

(F1, B1)

	PIN	SIDE	Signal Name	SLOT	ROW	PIN	SIDE	Signal Name
C	A	1	TAØ CØ2 A H (MASS CØ2)	2	B	A	1	MASS IN CØ2 H
C	B	1	DPØ TC Ø2 A L (MASS CØ2)	2	B	B	1	CMAX OUT CØ2 L
C	C	1	TAØ CØ5 A H (MASS CØ5)	2	B	C	1	MASS IN CØ5 H
C	D	1	DPØ TC Ø5 A L (MASS CØ5)	2	B	D	1	CMAX OUT CØ5 L
C	E	1	TAØ CØ4 A H (MASS CØ4)	2	B	E	1	MASS IN CØ4 H
C	F	1	TAØ REG SEL A Ø3 H (MASS REG SEL 3)	2	B	F	1	MASS REG SEL 3 H
C	H	1	DP3 MASS FAIL A L	2	B	H	1	CMAX MASS FAIL L
C	J	1	PMØ POWER OK H	2	B	J	1	DABS POWER OK H
–	K	1	—	–	–	–	–	—
–	L	1	—	–	–	–	–	—
D	M	1	DPI TRACEV EN A H	2	B	M	1	DABS MASS CONTROL ENB H
C	N	1	PMØ POWER OK H	2	B	N	1	DABS POWER OK H
C	P	1	TAØ RUN A H (MASS RUN)	2	B	P	1	MASS RUN H
D	R	1	TAØ WRT CLK A H (MASS WCLK)	2	B	R	1	MASS WCLK H
C	S	1	PMØ POWER OK H	2	B	S	1	DABS POWER OK H
	T	1	GND	←			→	GND
C	U	1	TAØ REG SEL A Ø4 H (MASS REG SEL 4)	2	B	U	1	MASS REG SEL 4 H
–	V	1	X					X

	PIN	SIDE	Signal Name	SLOT	ROW	PIN	SIDE	Signal Name
–	A	2	+5	←			→	+5
–	B	2	-15	←			→	-15
–	C	2	GND	←			→	GND
–	D	2	X	X	X	Y	Y	X
–	E	2	X	X	X	X	X	X
C	F	2	DP3 TRAS A EN H	2	B	F	2	CMAX MASS TRANSMIT H
–	H	2	X	X	X	X	Y	X
C	J	2	DPØ TC Ø4 A L (MASS CØ4)	2	B	J	2	CMAX OUT CØ4 L
–	K	2	X	Y	Y	Y	Y	X
C	L	2	DP2 ATA A(Ø) H (MASS ATTN)	2	B	L	2	ASR ATA L
–	M	2	X	Y		Y		X
–	N	2	X					X
D	P	2	ECØ BUS SYNC CLK L (MASS SCLK)	2	B	D	2	DABS SCLK L
	R	2	PMØ POWER OK H	2	B	R	2	DABS POWER OK H
	S	2	DP3 TRAS A EN H	2	B	S	2	CMAX MASS TRANSMIT H
–	T	2	—					—
–	U	2	X					X
C	V	2	TAØ CTOD A H (MASS CTOD)	2	B	V	2	MASS CTOD H

HD 17C, 3

LS109

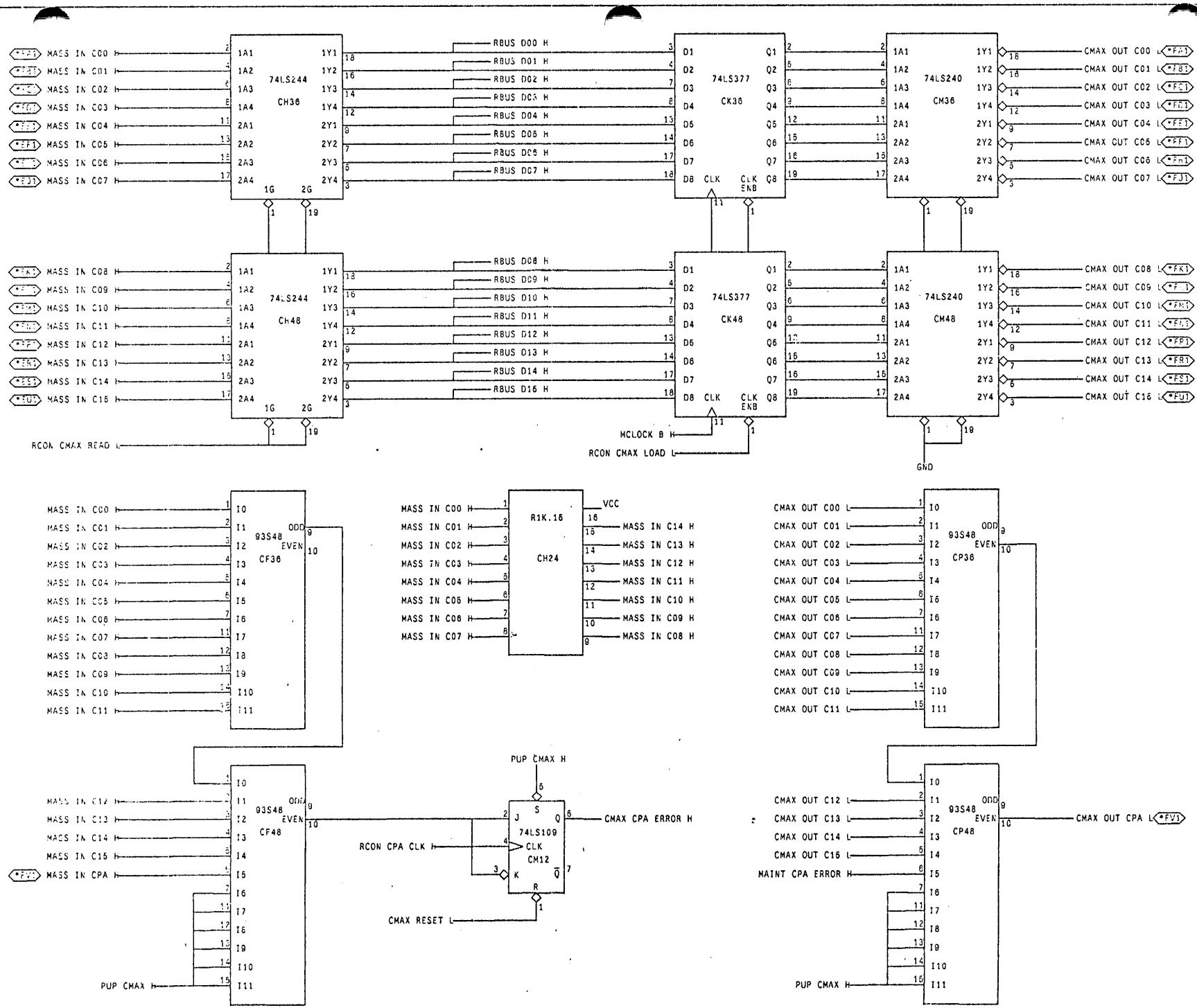
00

02

08

run hold
Rcon 610

maint DP17 error
C700 Hold



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TITLE: CMAX1 [RW3GFS]

DATE: 3-Aug-82 16:02

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TITLE: REGISTER CONTROL BRD, MICRO-PROGRAM SEQUENCER

FILE: RSEQR[RW4GFS]

DATE: 8-Sep-82 16:03

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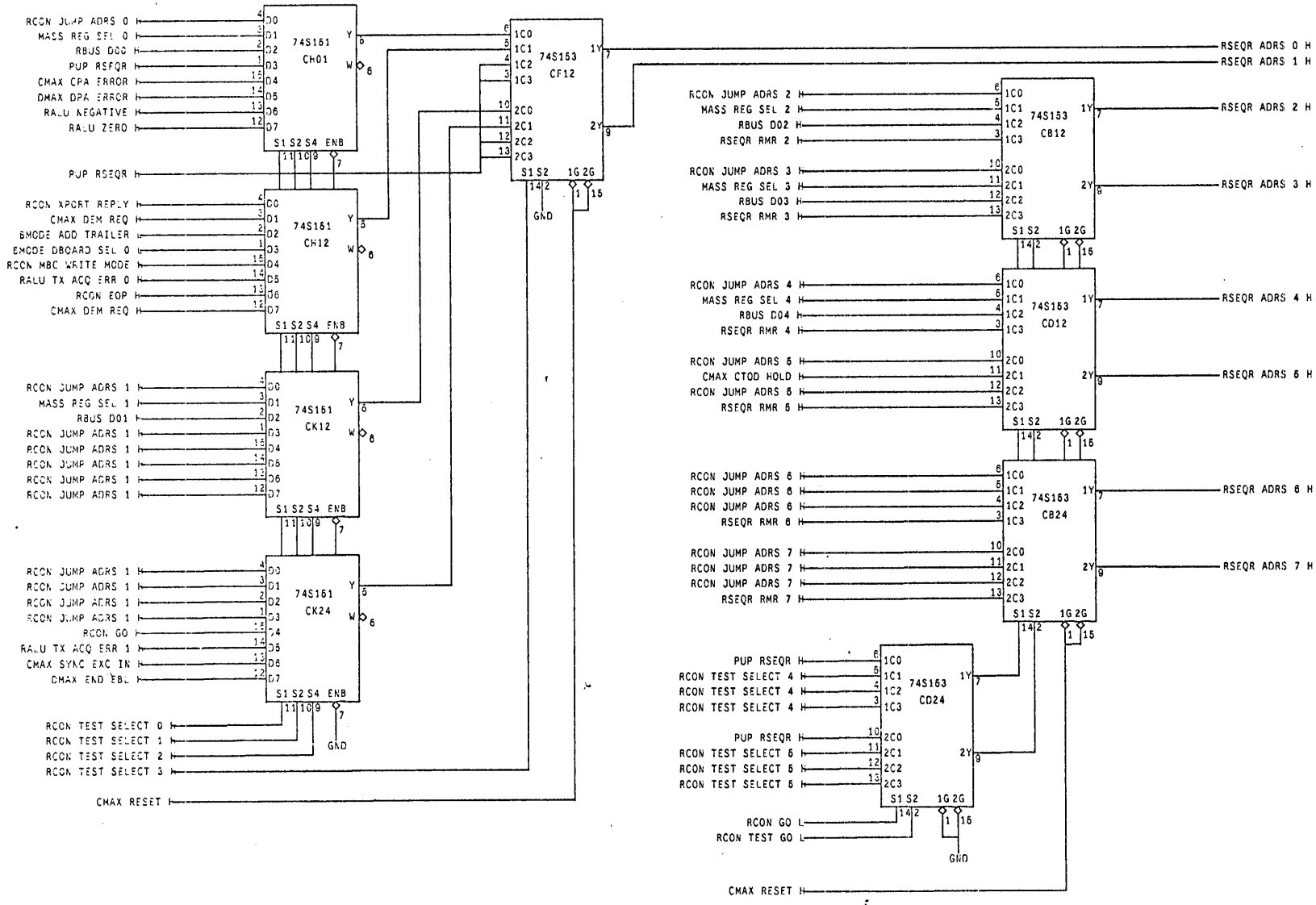

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FILE: RCON1[RW4GFS]

DATE: 8-Sep-82 16:03

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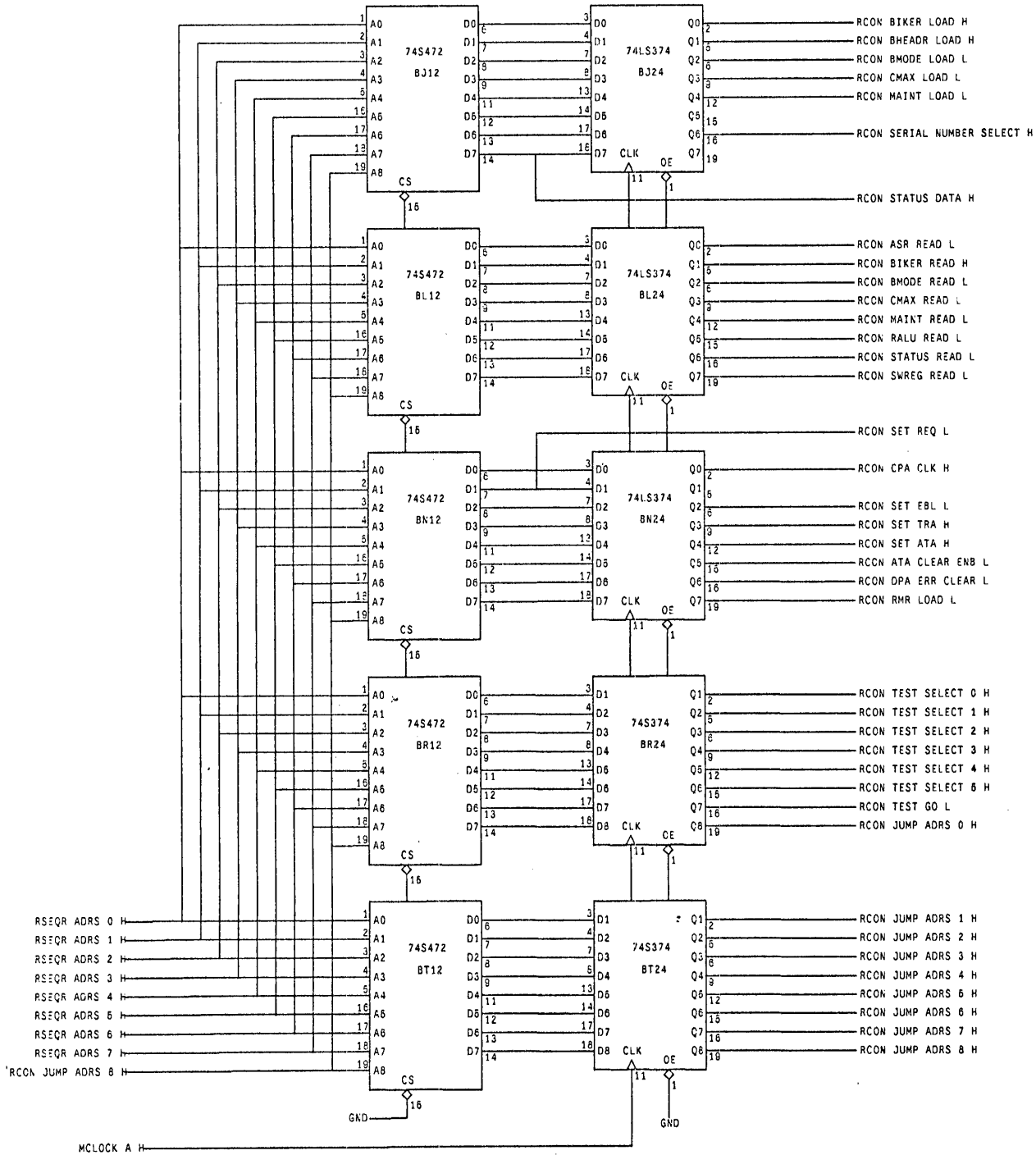

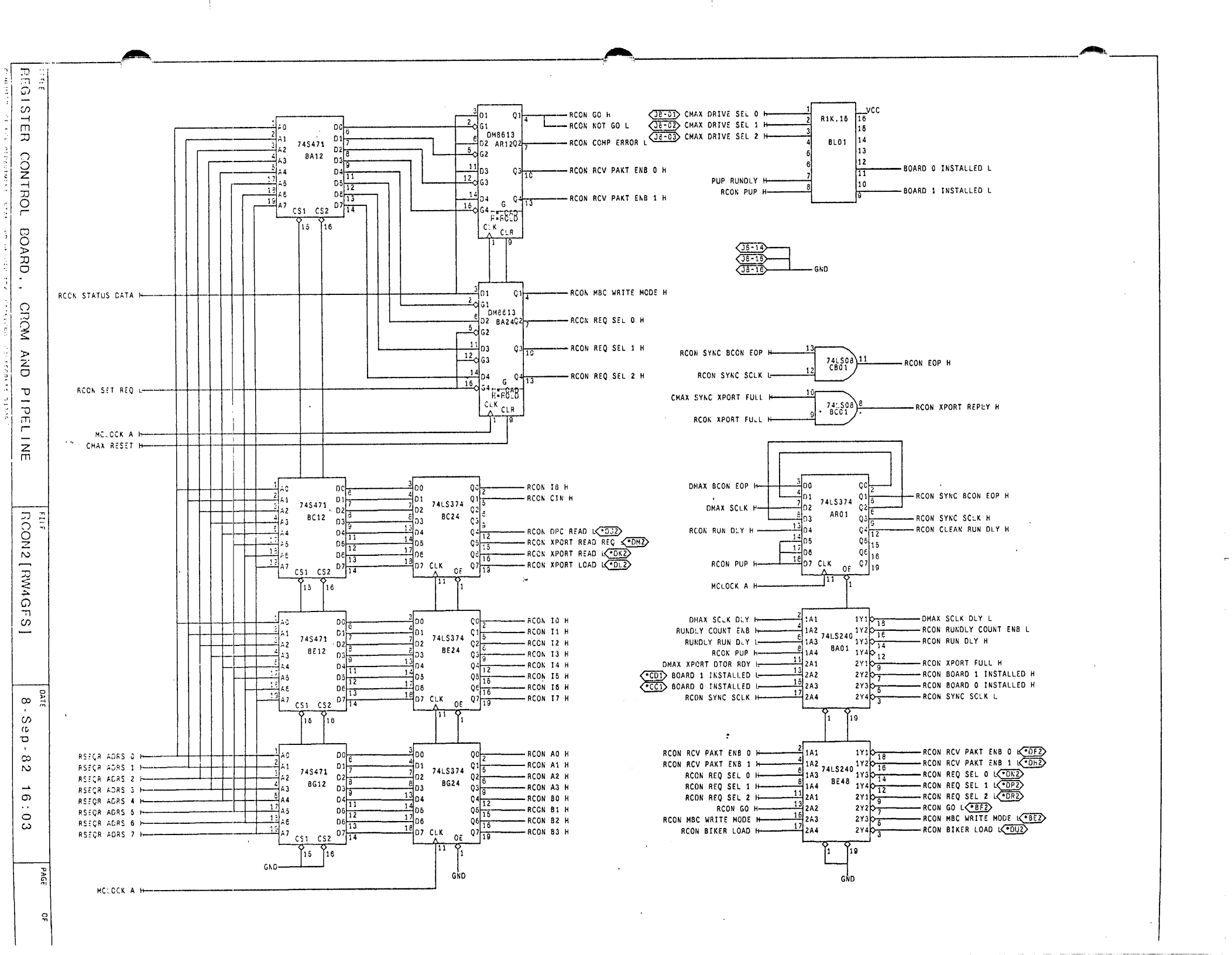
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DATE
8-Sep-82 16:03
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74S471 BC12
74LS374 BC24
74S471 BE12
74LS374 BE24
74S471 BG12
74LS374 BG24
R1K.16 BL01
74LS08 CB01
74LS08 BC01
74LS374 AR01
74LS240 BA01
74LS240 BE48
RCON STATUS DATA H
RCON SET REQ L
MCLOCK A H
CMAX RESET H
RSEQR ADRS 0
RSEQR ADRS 1
RSEQR ADRS 2
RSEQR ADRS 3
RSEQR ADRS 4
RSEQR ADRS 5
RSEQR ADRS 6
RSEQR ADRS 7
RCON GO H
RCON NOT GO L
RCON COMP ERROR L
RCON RCV PAKT ENB 0 H
RCON RCV PAKT ENB 1 H
RCON MBC WRITE MODE H
RCON REQ SEL 0 H
RCON REQ SEL 1 H
RCON REQ SEL 2 H
CMAX DRIVE SEL 0
CMAX DRIVE SEL 1
CMAX DRIVE SEL 2
PUP RUNDLY H
RCON PUP H
BOARD 0 INSTALLED L
BOARD 1 INSTALLED L
VCC
GND
RCON SYNC BCON EOP H
RCON SYNC SCLK L
RCON EOP H
CMAX SYNC XPORT FULL
RCON XPORT FULL H
RCON XPORT REPLY H
DMAX BCON EOP H
DMAX SCLK H
RCON RUN DLY H
RCON SYNC BCON EOP H
RCON SYNC SCLK H
RCON CLEAN RUN DLY H
RCON I8 H
RCON CIN H
RCON DPC READ L
RCON XPORT READ REQ L
RCON XPORT READ L
RCON XPORT LOAD L
RCON I0 H
RCON I1 H
RCON I2 H
RCON I3 H
RCON I4 H
RCON I5 H
RCON I6 H
RCON I7 H
RCON A0 H
RCON A1 H
RCON A2 H
RCON A3 H
RCON B0 H
RCON B1 H
RCON B2 H
RCON B3 H
DMAX SCLK DLY H
RUNDLY COUNT ENB
RUNDLY RUN DLY L
DMAX XPORT DTOR RDY L
BOARD 1 INSTALLED L
BOARD 0 INSTALLED L
DMAX SCLK DLY L
RCON RUNDLY COUNT ENB L
RCON RUN DLY H
RCON XPORT FULL H
RCON BOARD 1 INSTALLED H
RCON BOARD 0 INSTALLED H
RCON SYNC SCLK L
RCON RCV PAKT ENB 0 L
RCON RCV PAKT ENB 1 L
RCON REQ SEL 0 L
RCON REQ SEL 1 L
RCON REQ SEL 2 L
RCON GO L
RCON MBC WRITE MODE L
RCON BIKER LOAD L

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FILE
DMAX1[RW3GFS]

DATE
3-Aug-82 16:02

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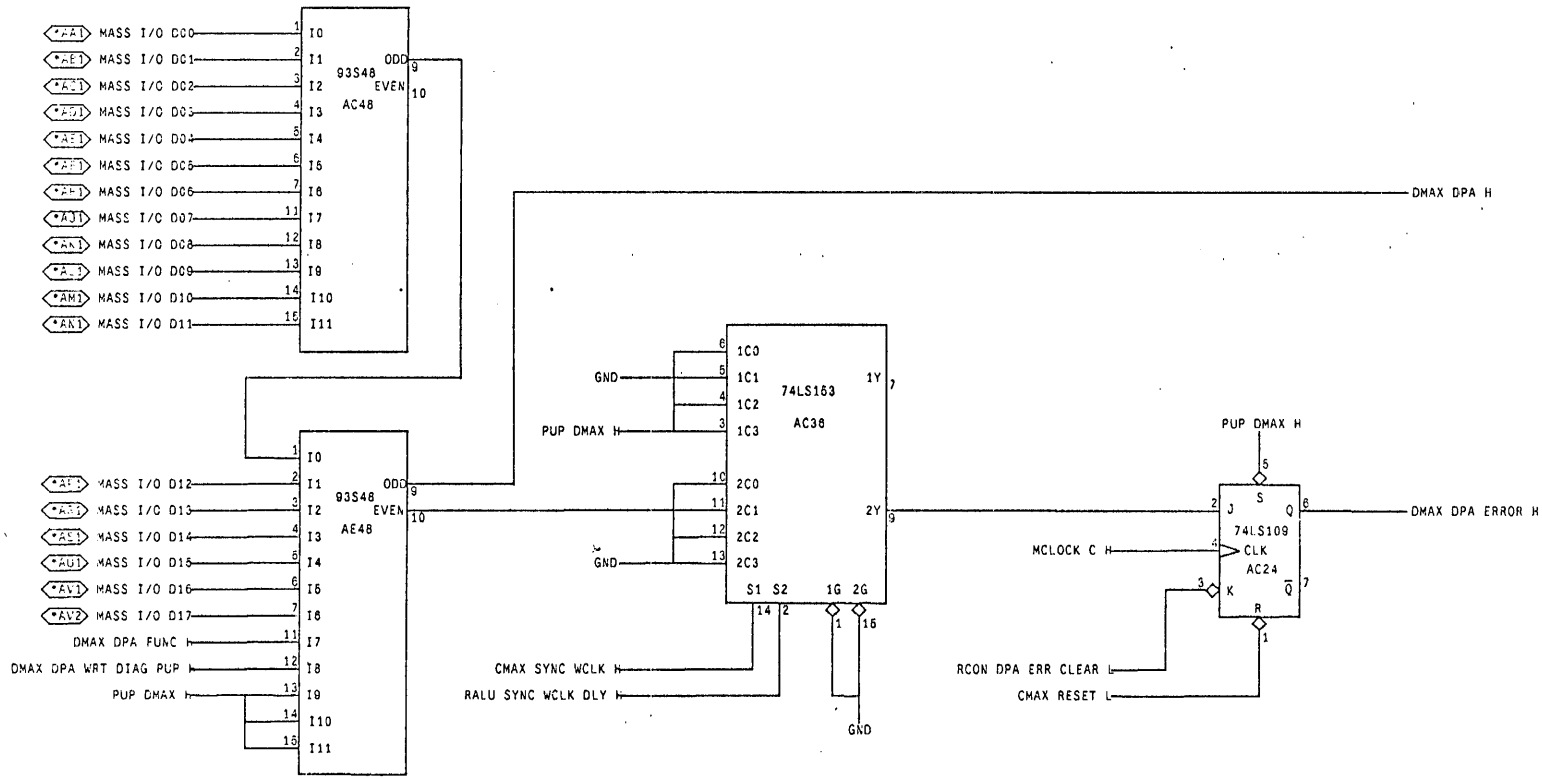

COMPUTER SCIENCE DEPARTMENT, STANFORD UNIVERSITY, STANFORD, CALIFORNIA 94305

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FILE: BMODE[RW3GFS]

DATE: 3-Aug-82 16:02

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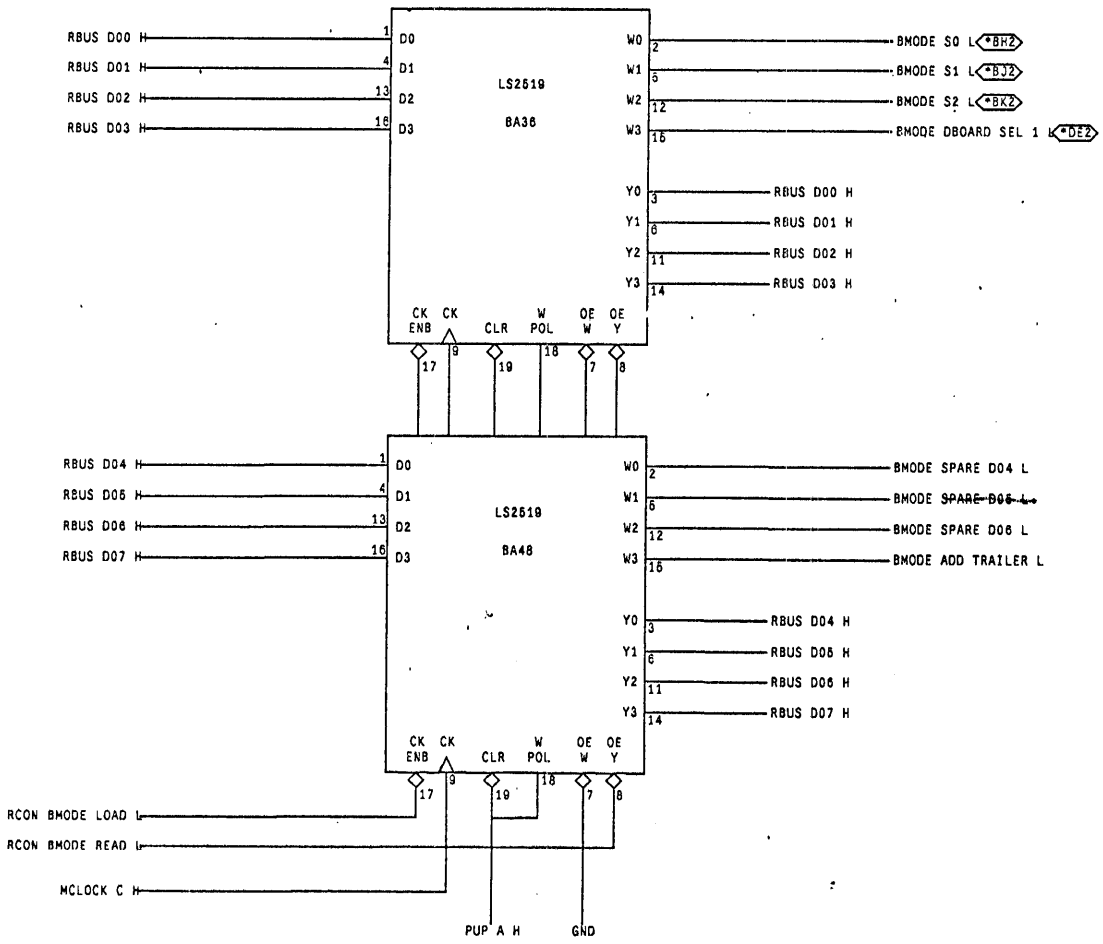
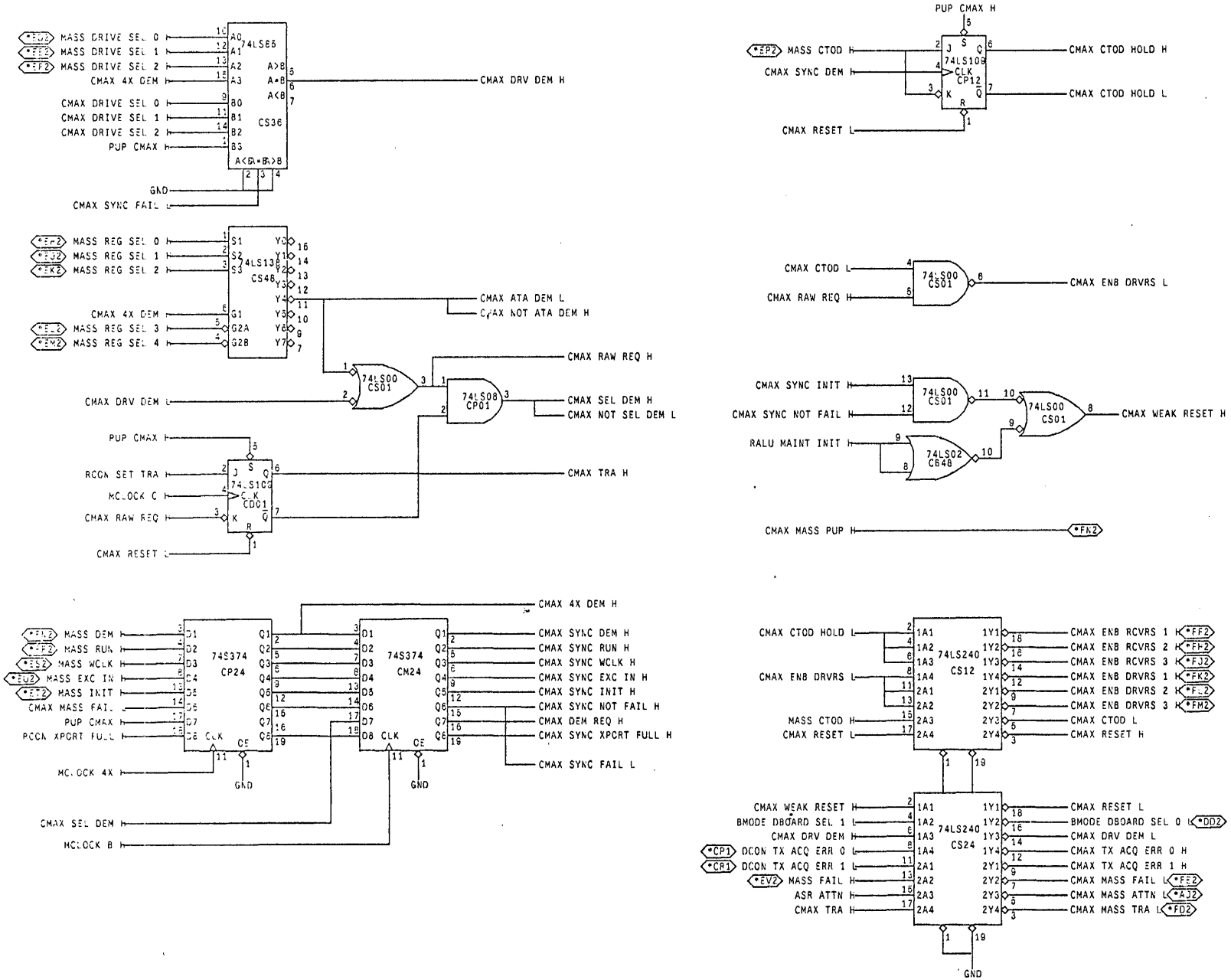
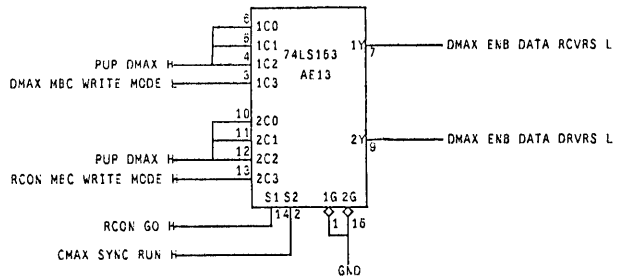



MASS DRIVE SEL 0
MASS DRIVE SEL 1
MASS DRIVE SEL 2
CMAX 4X DEM
CMAX DRIVE SEL 0
CMAX DRIVE SEL 1
CMAX DRIVE SEL 2
PUP CMAX
GND
CMAX SYNC FAIL L
74LS85
CS36
A<B A=B A>B
CMAX DRV DEM H
MASS REG SEL 0
MASS REG SEL 1
MASS REG SEL 2
MASS REG SEL 3
MASS REG SEL 4
74LS138
CS48
CMAX ATA DEM L
CMAX NOT ATA DEM H
74LS00
CS01
CMAX RAW REQ H
CMAX DRV DEM L
74LS08
CP01
CMAX SEL DEM H
CMAX NOT SEL DEM L
PUP CMAX
RCON SET TRA
MCLOCK C
CMAX RAW REQ
74LS109
CD01
CMAX TRA H
CMAX RESET L
CMAX 4X DEM H
MASS DEM
MASS RUN
MASS WCLK
MASS EXC IN
MASS INIT
CMAX MASS FAIL L
PUP CMAX
RCON XPORT FULL L
74S374
CP24
74S374
CM24
CMAX SYNC DEM H
CMAX SYNC RUN H
CMAX SYNC WCLK H
CMAX SYNC EXC IN H
CMAX SYNC INIT H
CMAX SYNC NOT FAIL H
CMAX DEM REQ H
CMAX SYNC XPORT FULL H
CMAX SYNC FAIL L
MCLOCK 4X
CMAX SEL DEM
MCLOCK B
PUP CMAX H
MASS CTOD H
CMAX SYNC DEM
CMAX RESET L
74LS109
CP12
CMAX CTOD HOLD H
CMAX CTOD HOLD L
CMAX CTOD L
CMAX RAW REQ H
74LS00
CS01
CMAX ENB DRVRS L
CMAX SYNC INIT H
CMAX SYNC NOT FAIL H
RALU MAINT INIT H
74LS00
CS01
74LS00
CS01
74LS02
CB48
CMAX WEAK RESET H
CMAX MASS PUP H
CMAX CTOD HOLD L
CMAX ENB DRVRS L
MASS CTOD H
CMAX RESET L
74LS240
CS12
CMAX ENB RCVRS 1 H
CMAX ENB RCVRS 2 H
CMAX ENB RCVRS 3 H
CMAX ENB DRVRS 1 H
CMAX ENB DRVRS 2 H
CMAX ENB DRVRS 3 H
CMAX CTOD L
CMAX RESET H
CMAX WEAK RESET H
BMODE DBOARD SEL 1 L
CMAX DRV DEM H
DCON TX ACQ ERR 0 L
DCON TX ACQ ERR 1 L
MASS FAIL H
ASR ATTN H
CMAX TRA H
74LS240
CS24
CMAX RESET L
BMODE DBOARD SEL 0 L
CMAX DRV DEM L
CMAX TX ACQ ERR 0 H
CMAX TX ACQ ERR 1 H
CMAX MASS FAIL L
CMAX MASS ATTN L
CMAX MASS TRA L
GND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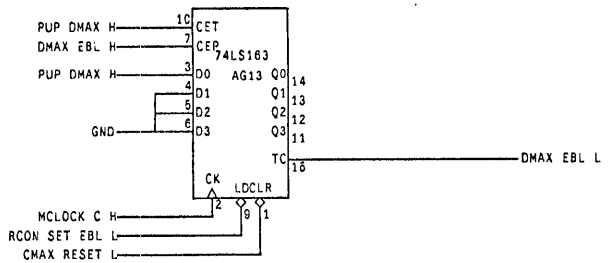
AE13
PUP DMAX H
DMAX MBC WRITE MODE L
PUP DMAX H
RCON MBC WRITE MODE H
RCON GO H
CMAX SYNC RUN H
DMAX ENB DATA RCVRS L
DMAX ENB DATA DRVRS L
GND


74LS163
AG13
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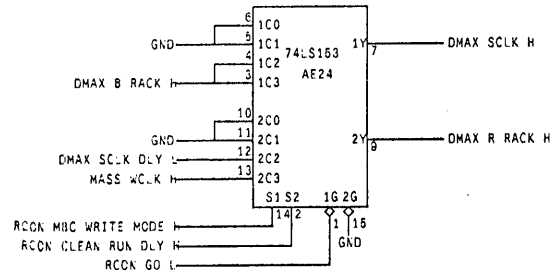
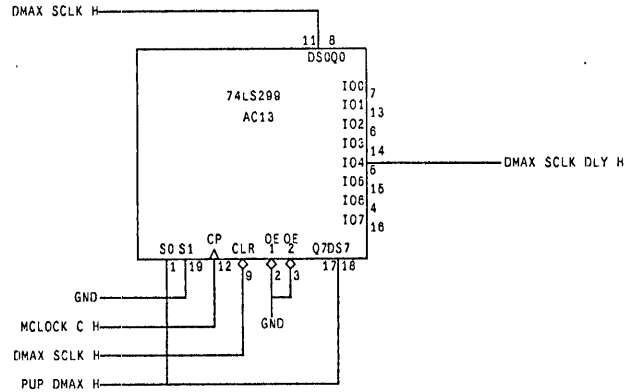
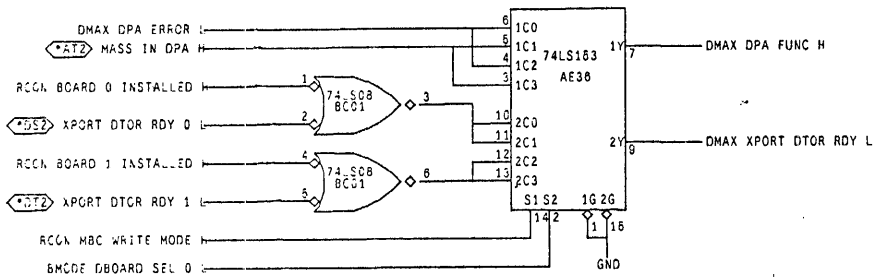
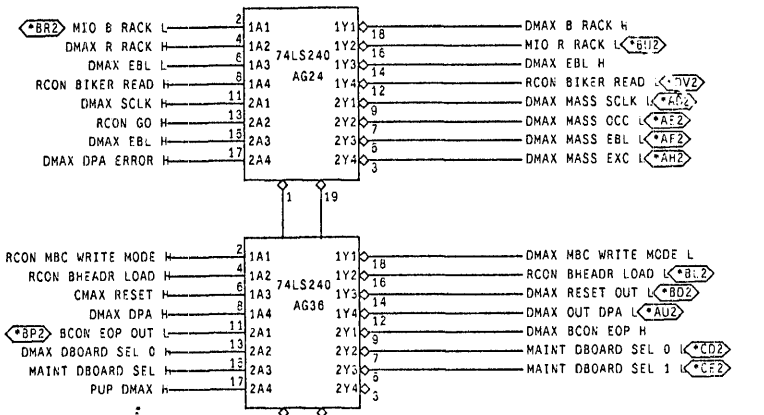
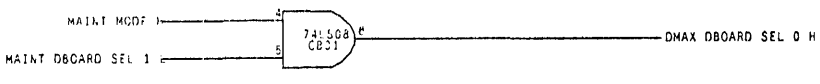
DMAX EBL H
PUP DMAX H
GND
MCLOCK C H
RCON SET EBL L
CMAX RESET L
DMAX EBL L


74LS163
AE24
GND
DMAX B RACK H
GND
DMAX SCLK DLY L
MASS WCLK H
RCON MBC WRITE MODE H
RCON CLEAN RUN DLY H
RCON GO L
DMAX SCLK H
DMAX R RACK H
GND


74LS299
AC13
DMAX SCLK H
DMAX SCLK DLY H
GND
MCLOCK C H
DMAX SCLK H
PUP DMAX H
GND


74LS163
AE36
DMAX DPA ERROR L
MASS IN DPA H
RCON BOARD 0 INSTALLED
XPORT DTOR RDY 0 L
RCON BOARD 1 INSTALLED
XPORT DTOR RDY 1 L
RCON MBC WRITE MODE
BMCDE DBOARD SEL 0
74LS08
BC01
DMAX DPA FUNC H
DMAX XPORT DTOR RDY L
GND


74LS240
AG24
MIO B RACK L
DMAX R RACK H
DMAX EBL L
RCON BIKER READ H
DMAX SCLK H
RCON GO H
DMAX EBL H
DMAX DPA ERROR H
DMAX B RACK H
MIO R RACK L
DMAX EBL H
RCON BIKER READ L
DMAX MASS SCLK L
DMAX MASS OCC L
DMAX MASS EBL L
DMAX MASS EXC L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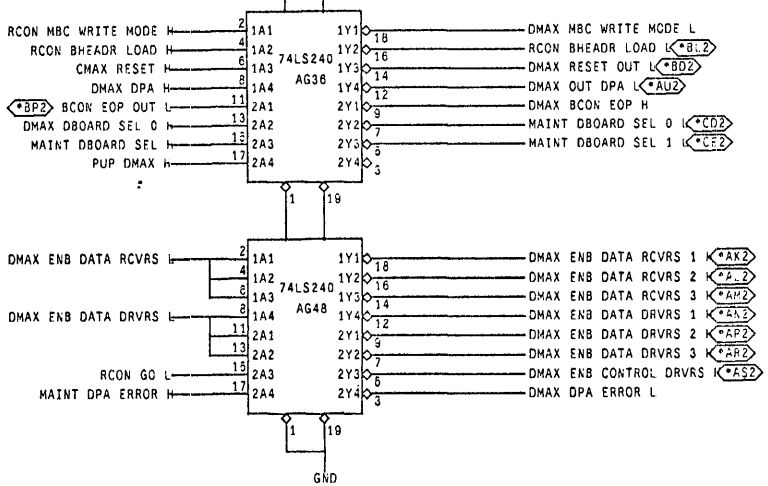
MAINT DBOARD SEL 1 L
74LS08
CB01
DMAX DBOARD SEL 0 H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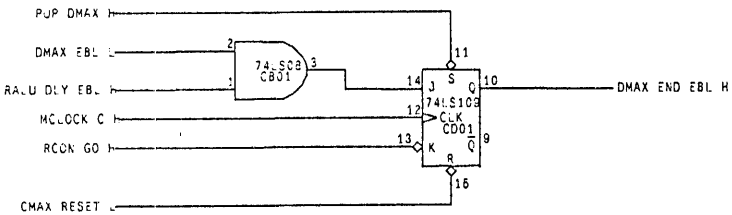
AG36
RCON MBC WRITE MODE H
RCON BHEADR LOAD H
CMAX RESET H
DMAX DPA H
BCON EOP OUT L
DMAX DBOARD SEL 0 H
MAINT DBOARD SEL H
PUP DMAX H
DMAX MBC WRITE MODE L
RCON BHEADR LOAD L
DMAX RESET OUT L
DMAX OUT DPA L
DMAX BCON EOP H
MAINT DBOARD SEL 0 L
MAINT DBOARD SEL 1 L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DMAX EBL L
74LS08
CB01
RALU DLY EBL H
MCLOCK C H
RCON GO H
74LS109
CD01
CLK
CMAX RESET L
DMAX END EBL H

74LS240
AG48
DMAX ENB DATA RCVRS L
DMAX ENB DATA DRVRS L
RCON GO L
MAINT DPA ERROR H
DMAX ENB DATA RCVRS 1 L
DMAX ENB DATA RCVRS 2 L
DMAX ENB DATA RCVRS 3 L
DMAX ENB DATA DRVRS 1 L
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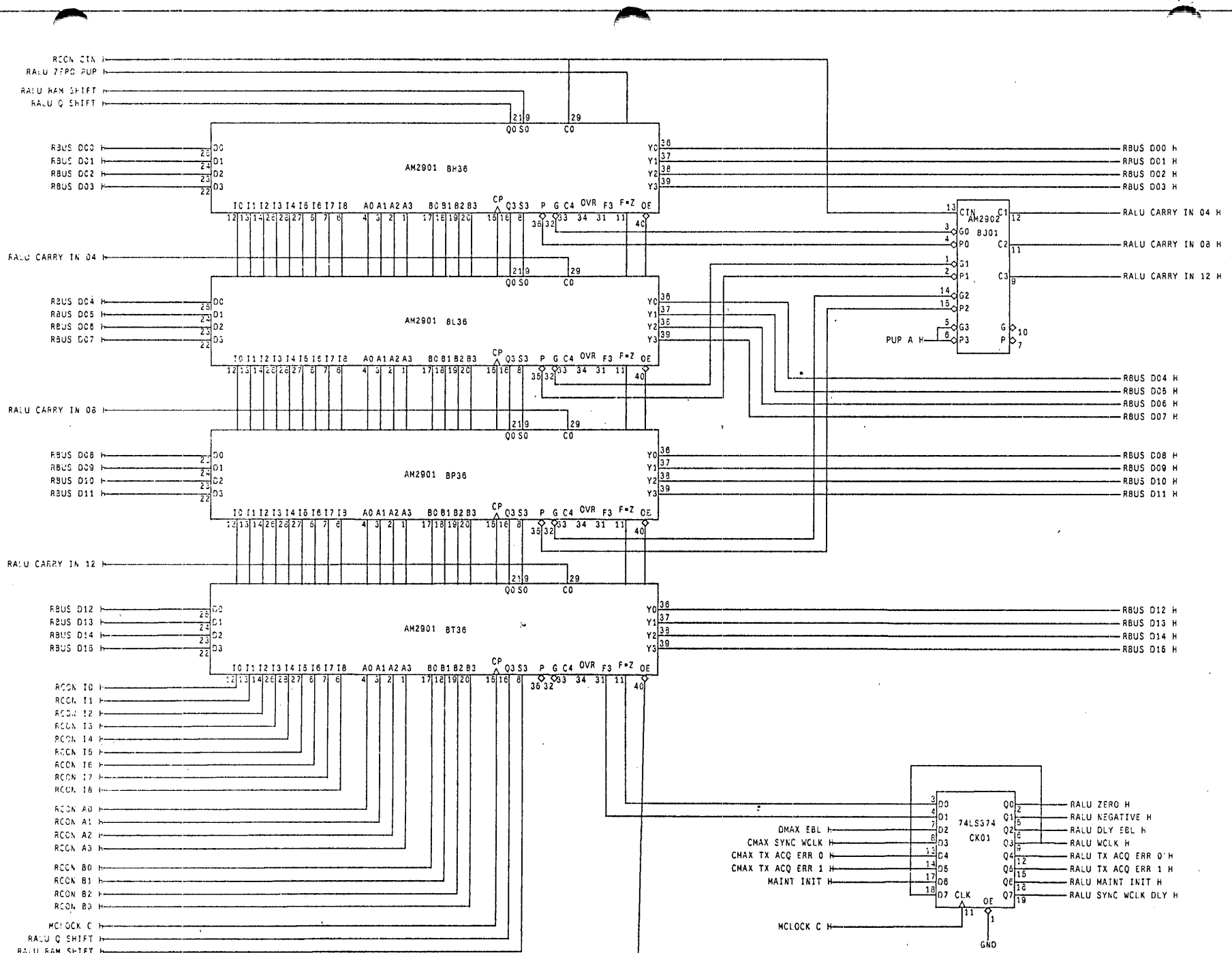
DMAX DPA ERROR L
GND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3-Aug-82 16:02
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RALU Q SHIFT H
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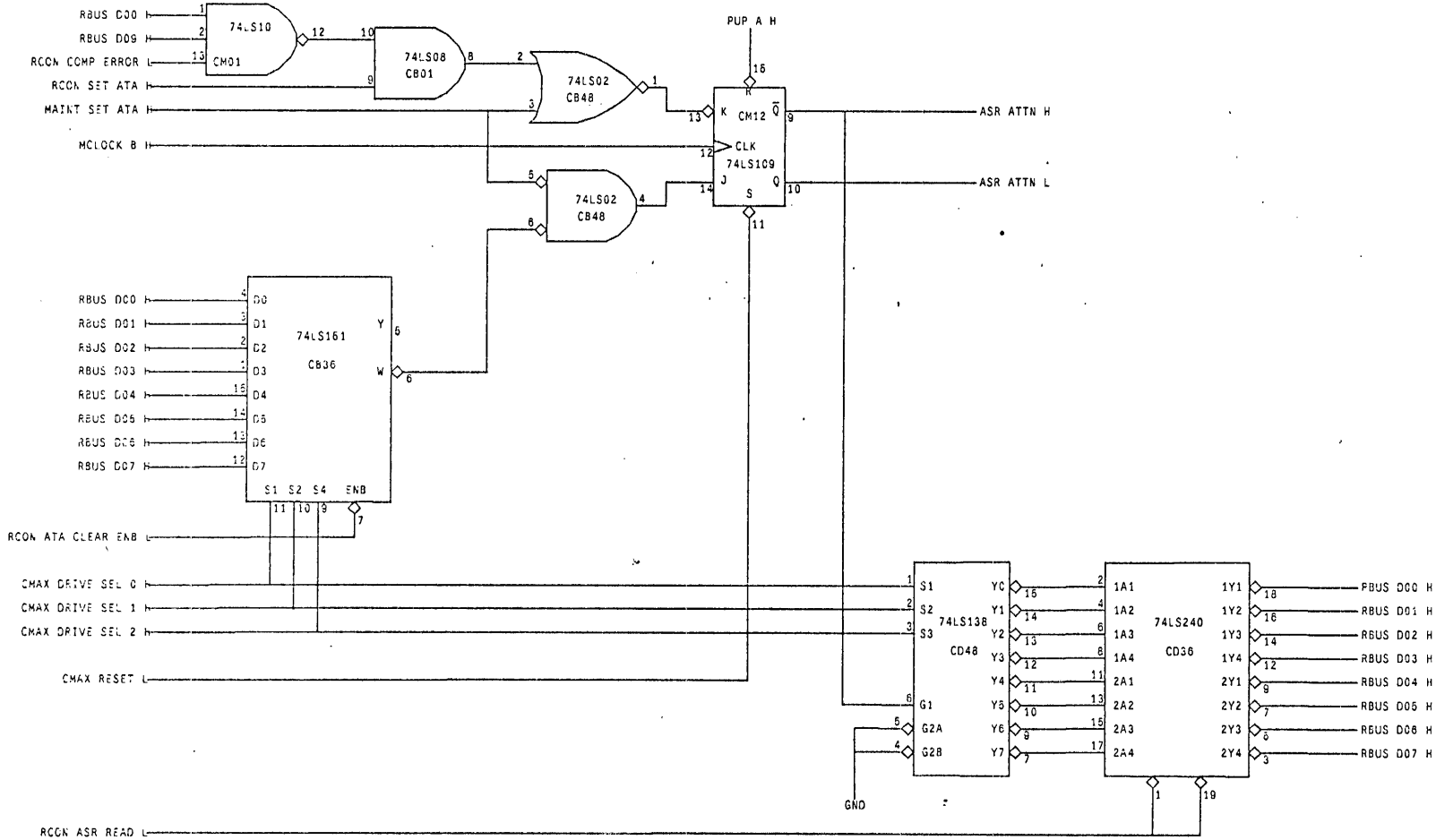
AM2901 BL36
AM2901 BP36
AM2901 BT36
RBUS D00 H
RBUS D01 H
RBUS D02 H
RBUS D03 H
RBUS D04 H
RBUS D05 H
RBUS D06 H
RBUS D07 H
RBUS D08 H
RBUS D09 H
RBUS D10 H
RBUS D11 H
RBUS D12 H
RBUS D13 H
RBUS D14 H
RBUS D15 H
RALU CARRY IN 04 H
RALU CARRY IN 08 H
RALU CARRY IN 12 H
AM2902
PUP A H
RCON I0 H
RCON I1 H
RCON I2 H
RCON I3 H
RCON I4 H
RCON I5 H
RCON I6 H
RCON I7 H
RCON I8 H
RCON A0 H
RCON A1 H
RCON A2 H
RCON A3 H
RCON B0 H
RCON B1 H
RCON B2 H
RCON B3 H
MCLOCK C H
RALU Q SHIFT H
RALU RAM SHIFT H
RCON RALU READ L
DMAX EBL H
CMAX SYNC WCLK H
CMAX TX ACQ ERR 0 H
CMAX TX ACQ ERR 1 H
MAINT INIT H
74LS374
CK01
RALU ZERO H
RALU NEGATIVE H
RALU DLY EBL H
RALU WCLK H
RALU TX ACQ ERR 0 H
RALU TX ACQ ERR 1 H
RALU MAINT INIT H
RALU SYNC WCLK DLY H
GND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RBUS D09 H
RCON COMP ERROR L
RCON SET ATA H
MAINT SET ATA H
74LS10
CM01
74LS08
CB01
74LS02
CB48
PUP A H
CM12
ASR ATTN H
MCLOCK B H
74LS109
ASR ATTN L
74LS02
CB48
RBUS D00 H
RBUS D01 H
RBUS D02 H
RBUS D03 H
RBUS D04 H
RBUS D05 H
RBUS D06 H
RBUS D07 H
74LS161
CB36
S1 S2 S4 ENB
RCON ATA CLEAR ENB L
CMAX DRIVE SEL 0 H
CMAX DRIVE SEL 1 H
CMAX DRIVE SEL 2 H
CMAX RESET L
74LS138
CD48
74LS240
CD36
GND
RCON ASR READ L
RBUS D00 H
RBUS D01 H
RBUS D02 H
RBUS D03 H
RBUS D04 H
RBUS D05 H
RBUS D06 H
RBUS D07 H

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FILE: STATUS[RW3GFS]

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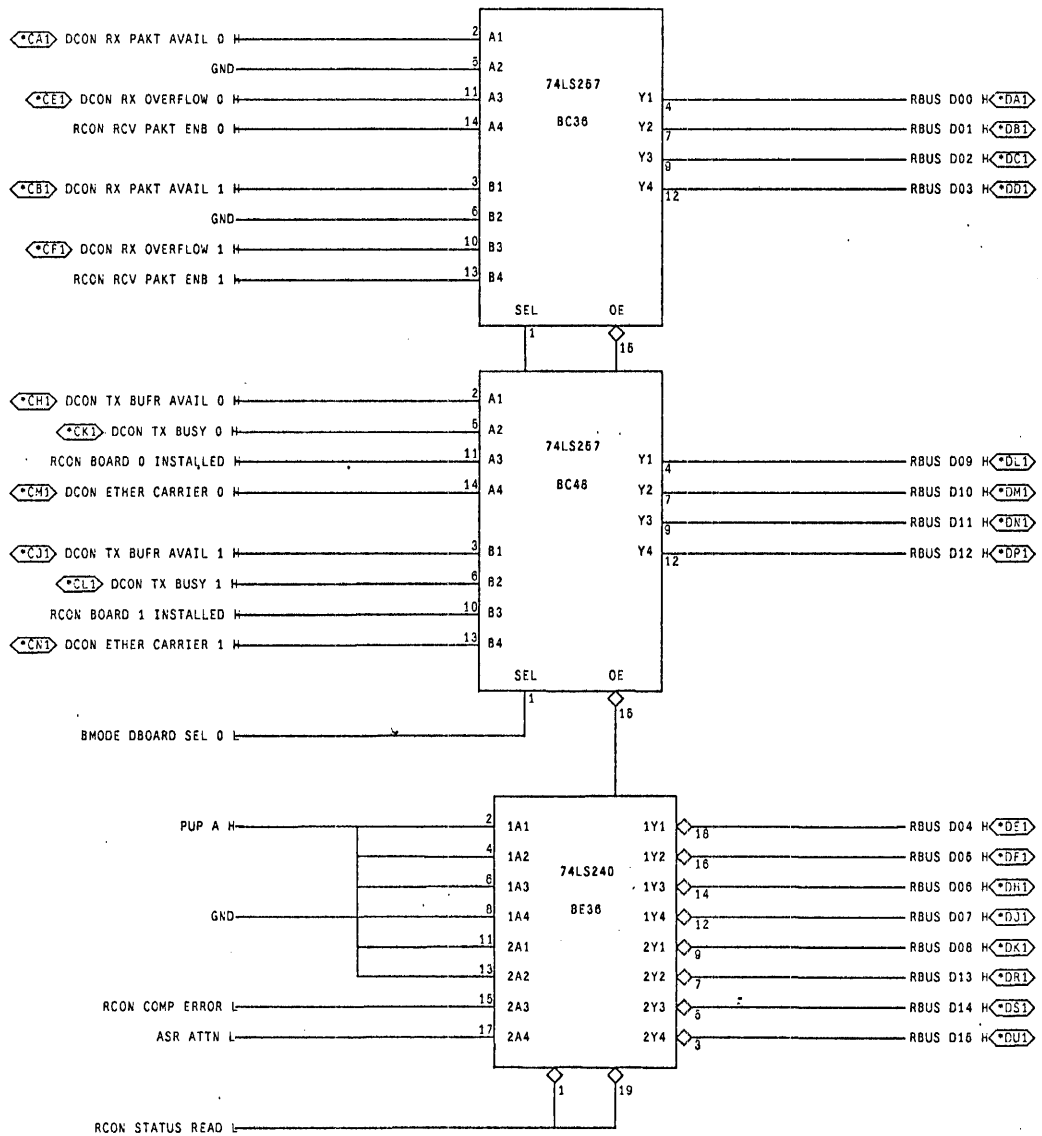

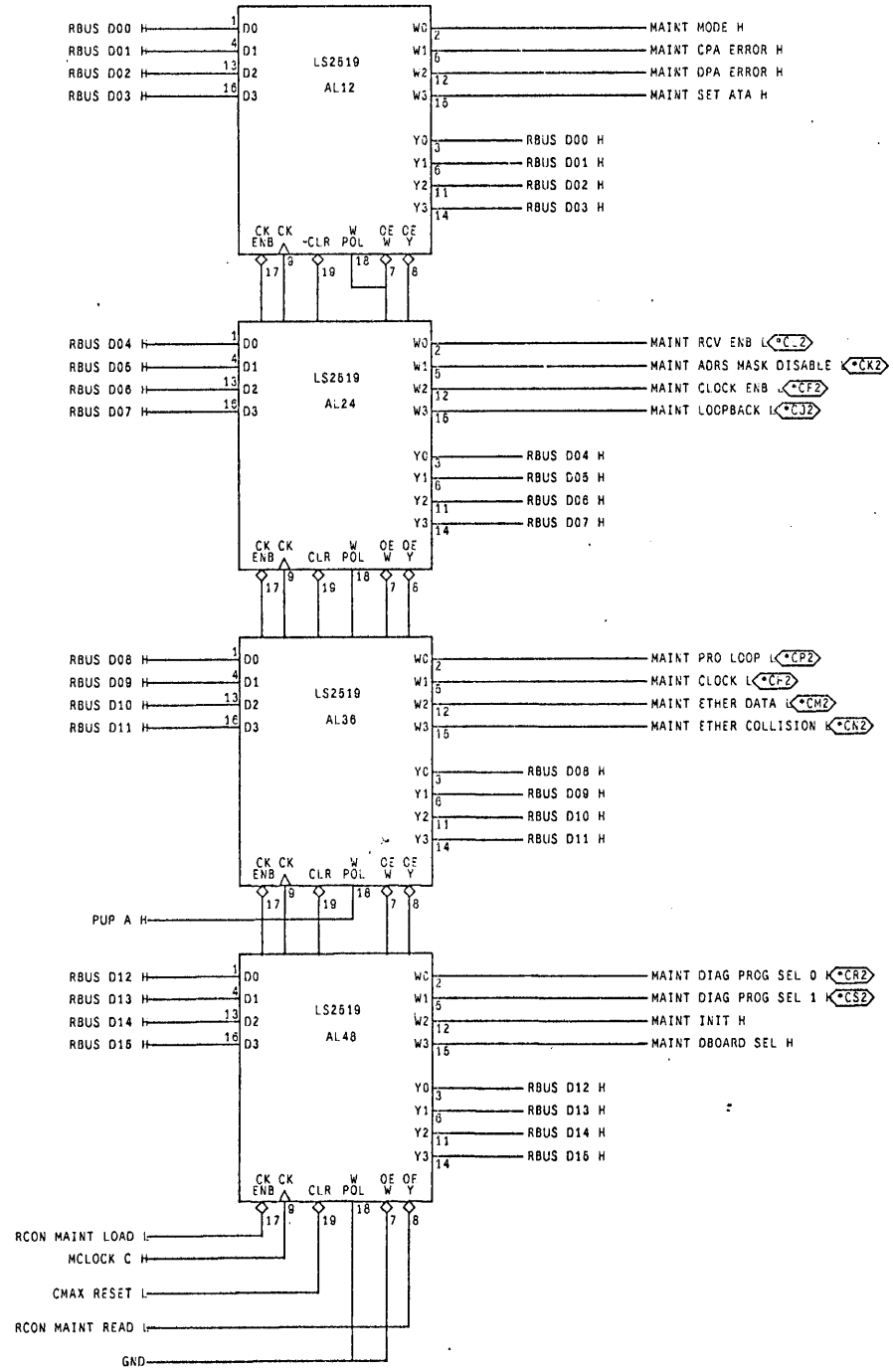

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FILE: MAINT[RW3GFS]

DATE: 3-Aug-82 16:02

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TITLE: REGISTER CNTL BRD, , SWITCH REGISTER

FILE: SWREG[RW4GFS]

DATE: 8-Sep-82 16:03

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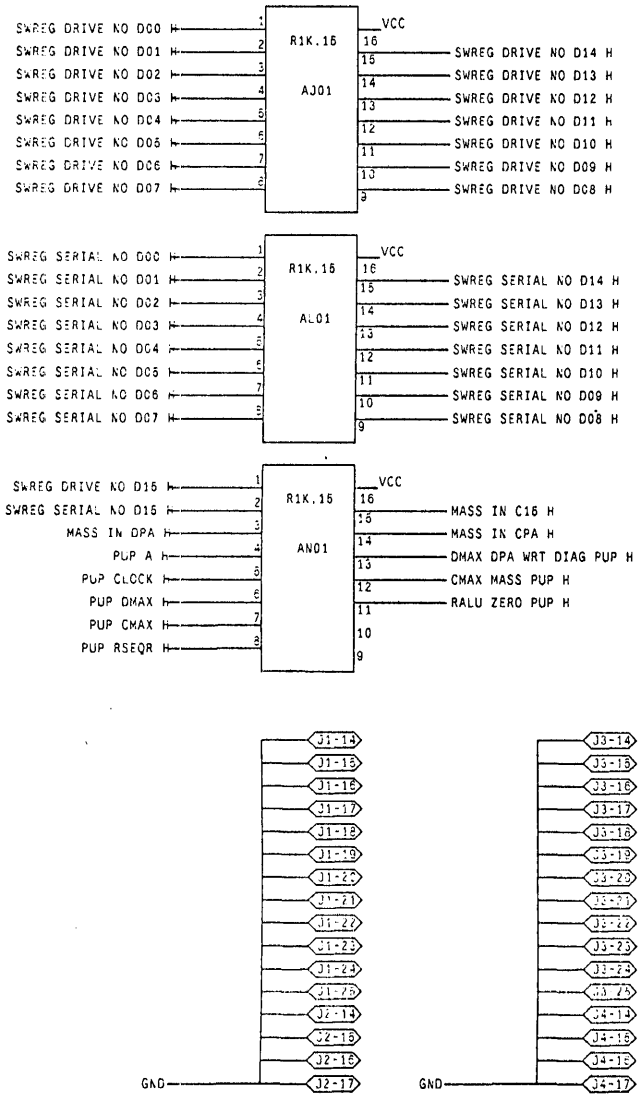
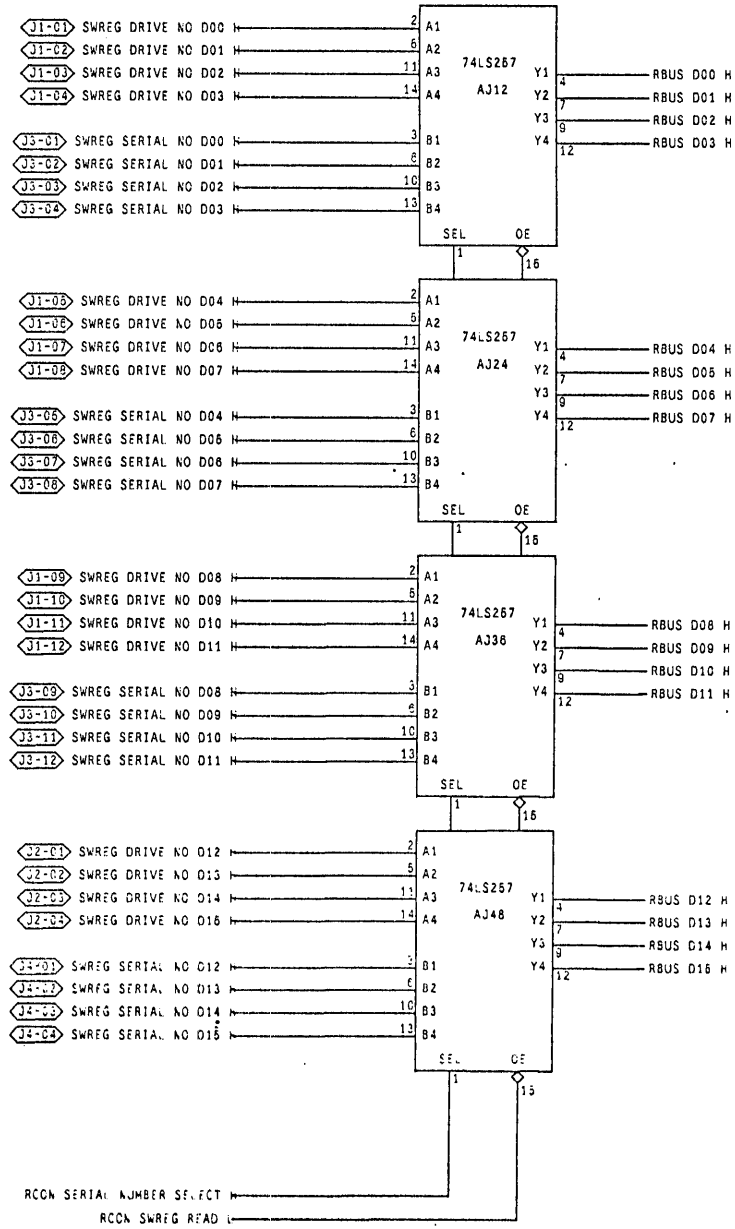


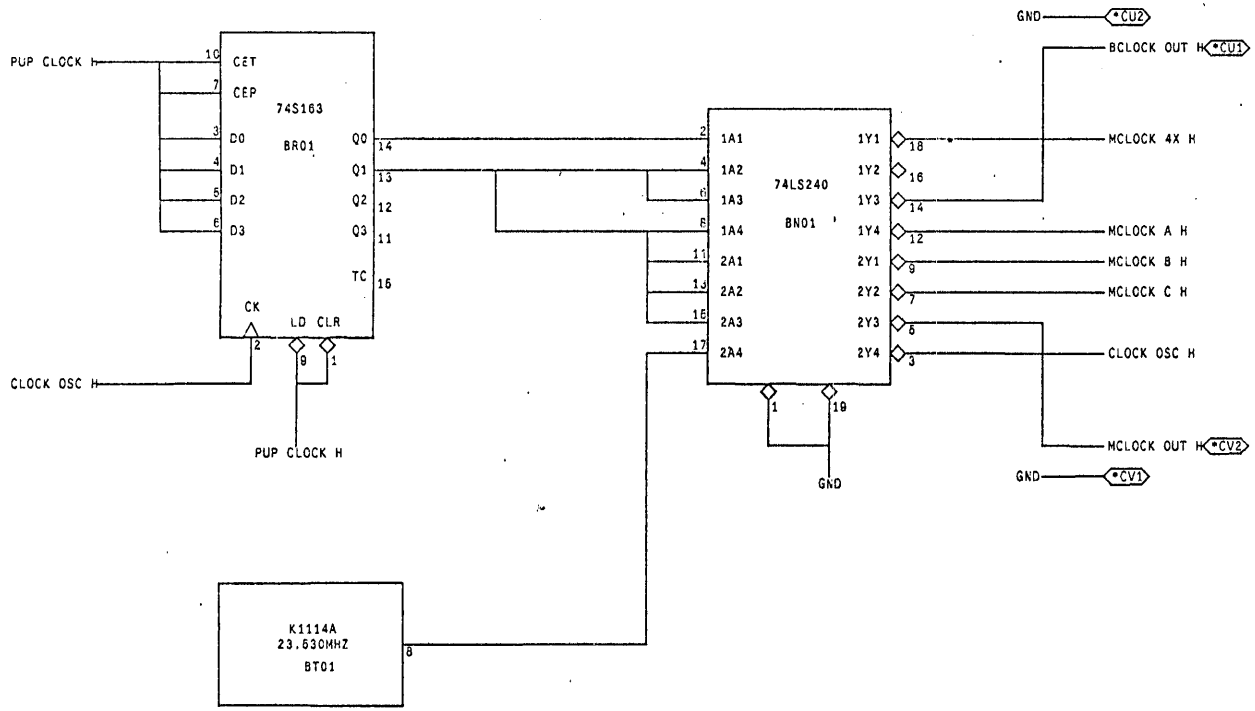


TITLE: REGISTER CNTL BRD., CLOCK GENERATION

FILE: CLOCK [RW3GFS]

DATE: 3-Aug-82 16:02

PAGE: OF



DUAL-WIDTH DEC BOARD PINOUTS

BOARD NAME: REGISTER CONTROL

COLUMN (A,C,E): A

Signal Name					Signal Name	
MASS I/O DØØ	1	A	2		+5	
DØ1	1	B	2		-15	
DØ2	1	C	2		GND	
DØ3	1	D	2		DMAX MASS SCLK L	0
DØ4	1	E	2		DMAX MASS OCC L	1
DØ5	1	F	2		DMAX MASS EBL L	2
DØ6	1	H	2		DMAX MASS EXC L	3
DØ7	1	J	2		DMAX MASS ATTN L	4
DØ8	1	K	2		DMAX ENB DATA RCVRS 1 H	5
DØ9	1	L	2		2	
D1Ø	1	M	2		3	
D11	1	N	2		DMAX ENB DATA DRVRS 1 H	6
D12	1	P	2		2	
D13	1	R	2		3	
D14	1	S	2		DMAX ENB CONTROL DRVRS H	
GND	1	T	2		MASS IN DPA H	
D15	1	U	2		DMAX OUT DPA L	
D16	1	V	2		MASS I/O D17	

COLUMN (B,D,F): B

Signal Name					Signal Name	
	1	A	2		+5	
	1	B	2		-15	
	1	C	2		GND	
	1	D	2		DMAX RESET OUT L	
	1	E	2		RCON MEC WRITE MODE L	7
	1	F	2		RCON GO L	8
	1	H	2		BMODE SØ L	
	1	J	2		BMODE S1 L	
	1	K	2		BMODE S2 L	
	1	L	2		DMAX BHEADR LOAD L	9
	1	M	2			
	1	N	2			10
	1	P	2		BCON EOP L	11
	1	R	2		MIO TRANSFER REQ L	12
	1	S	2			
GND	1	T	2			
	1	U	2		MIO TRANSFER ACK L	13
	1	V	2			

DUAL-WIDTH DEC BOARD PINOUTS

BOARD NAME: CONTROL

COLUMN (A,C,E): C

Signal Name					Signal Name
DCON RX PACKET AVAIL ØH	1	A	2		+5
DCON RX PACKET AVAIL 1H	1	B	2		-15
DCON RX ALERT ØH	1	C	2		GND
DCON RX ALERT 1H	1	D	2		MAINT DBOARD SEL ØL
DCON RX OVERFLOW ØH	1	E	2		MAINT DBOARD SEL 1L
DCON RX OVERFLOW 1H	1	F	2		MAINT CLOCK ENB L
DCON TX BUFFER AVAIL ØH	1	H	2		MAINT CLOCK L
DCON TX BUFFER AVAIL 1H	1	J	2		MAINT LOOPBACK L
DCON TX BUSY ØH	1	K	2		MAINT ADRS MASK DISABLE L
DCON TX BUSY 1H	1	L	2		MAINT RCV DISABLE L
DCON ETHER CARRIER ØH	1	M	2		MAINT ETHER DATA L
DCON ETHER CARRIER 1H	1	N	2		MAINT ETHER COLLISION L
DCON TX ACQ.CRM ØL	1	P	2		MAINT PRO LOOP L
DCON TX ACQ ENB 1L	1	R	2		MAINT DIAG PROG SEL ØH
DCON BOARD INSTALLED 1L	1	S	2		MAINT DIAG PROM SEL 1H
GND	1	T	2		
BCLOCK OUT H	1	U	2		GND
GND	1	V	2		MCLOCK OUT H

COLUMN (B,D,F): D

Signal Name				Signal Name
RBUS DØØ H	A	2		+5
DØ1	B	2		-15
DØ2	C	2		GND
DØ3	D	2		BMODE DBOARD SEL ØL
DØ4	E	2		1
DØ5	F	2		RCON RCV PAKT ENB ØL
DØ6	H	2		1
DØ7	J	2		RCON DPC READ L
DØ8	K	2		RCON XPORT READ L
DØ9	L	2		RCON XPORT LOAD L
D10	M	2		RCON XPORT READ REQ L
D11	N	2		RCON REQ SEL ØL
D12	P	2		1
D13	R	2		2
D14	S	2		XPORT DTOR RDY ØL
GND	T	2		XPORT DTOR RDY 1L
D15	U	2		RCON BIXER LOAD L
RCON	V	2		RCON BIXER READ L

DUAL-WIDTH DEC BOARD PINOUTS

BOARD NAME: CONTROL

COLUMN (A,C,E): E

Signal Name					Signal Name
MASS IN CØØ H	1	A	2		+5
CØ1	1	B	2		-15
CØ2	1	C	2		GND
CØ3	1	D	2		MASS DRIVE SEL Ø H
CØ4	1	E	2		MASS DRIVE SEL 1 H
CØ5	1	F	2		MASS DRIVE SEL 2 H
CØ6	1	H	2		MASS REG SEL Ø H
CØ7	1	J	2		MASS REG SEL 1 H
CØ8	1	K	2		MASS REG SEL 2 H
CØ9	1	L	2		MASS REG SEL 3 H
C1Ø	1	M	2		MASS REG SEL 4 H
C11	1	N	2		MASS DEM H
C12	1	P	2		MASS CTOD H
C13	1	R	2		MASS RUN H
C14	1	S	2		MASS WCLK H
GND	1	T	2		MASS INIT H
C15	1	U	2		MASS EXC IN H
MASS IN CPA H	1	V	2		MASS FAIL H

COLUMN (B,D,F): F

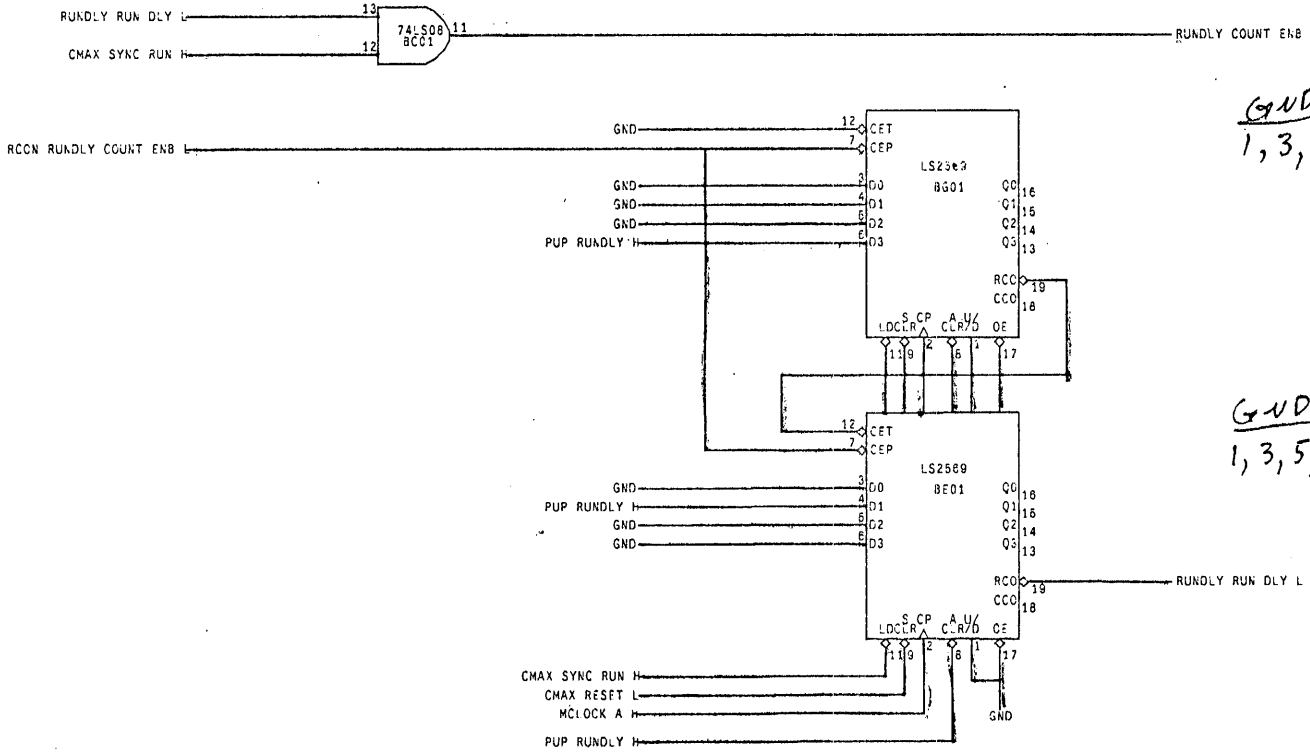
Signal Name					Signal Name
CMAX OUT CØØ L	1	A	2		+5
CØ1	1	B	2		-15
CØ2	1	C	2		GND
CØ3	1	D	2		CMAX MASS TRAL
CØ4	1	E	2		CMAX MASS FAIL L
CØ5	1	F	2		CMAX ENB RCVRS 1 H
CØ6	1	H	2		CMAX ENB RCVRS 2 H
CØ7	1	J	2		3 H
CØ8	1	K	2		CMAX ENB DRVRS 1 H
CØ9	1	L	2		2 H
C1Ø	1	M	2		3 H
C11	1	N	2		CMAX PUP H
C12	1	P	2		
C13	1	R	2		
C14	1	S	2		
GND	1	T	2		
C15	1	U	2		
CMAX OUT CPA L	1	V	2		

TITLE: BARREL SHIFTER BRD, BYTE COUNT REGISTER

FILE: RUNDLY[RW3GFS]

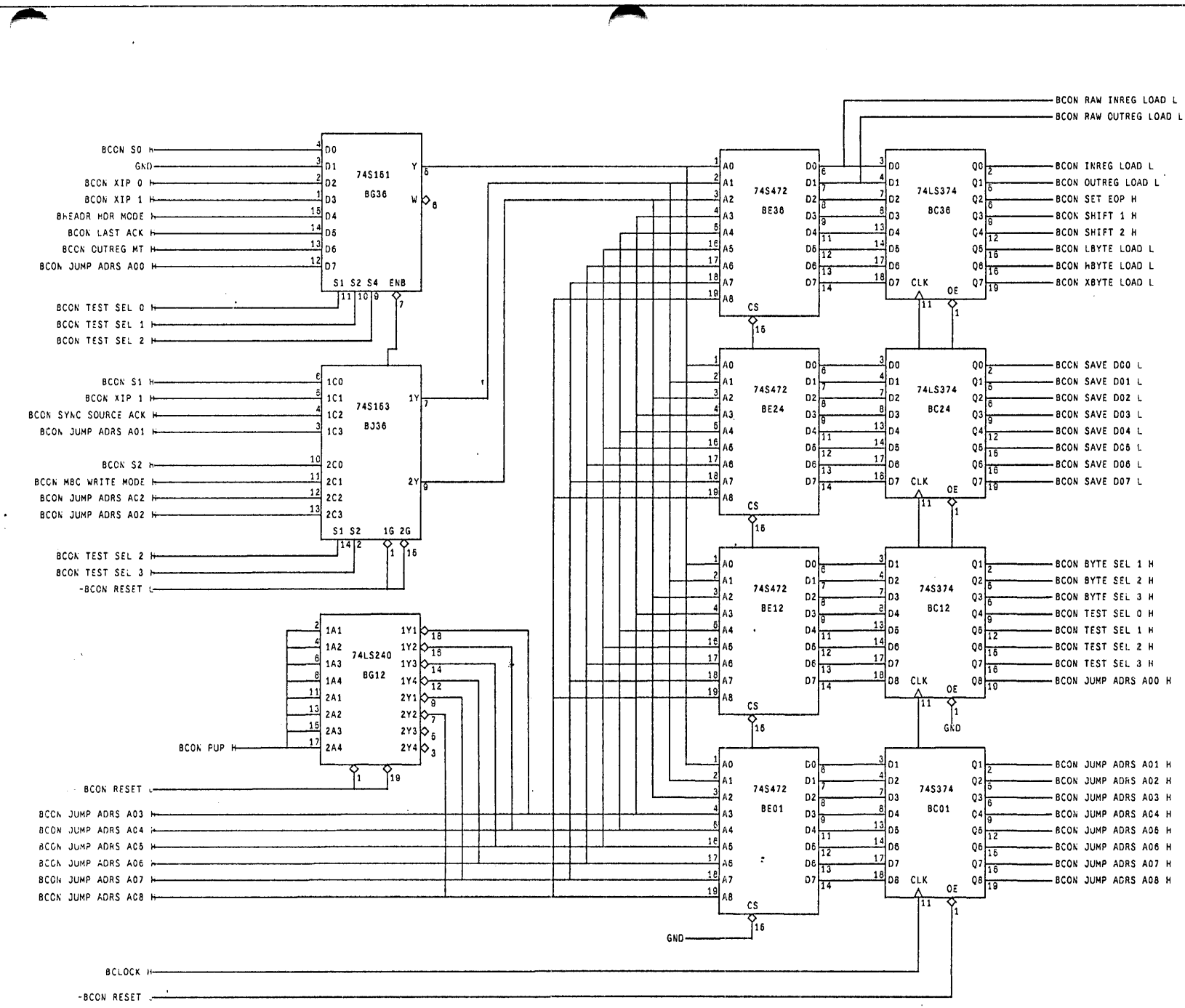
DATE: 3-Aug-82 16:02

PAGE: OF



GND
1, 3, 4, 5, 12, 17 ✓

GND
1, 3, 5, 6, 17 ✓



TITLE: BARREL SHIFTER BRD. - MICROCODE CONTROL

FILE: BCON1[MEIGFS]

DATE: 13-Oct-82 14:22

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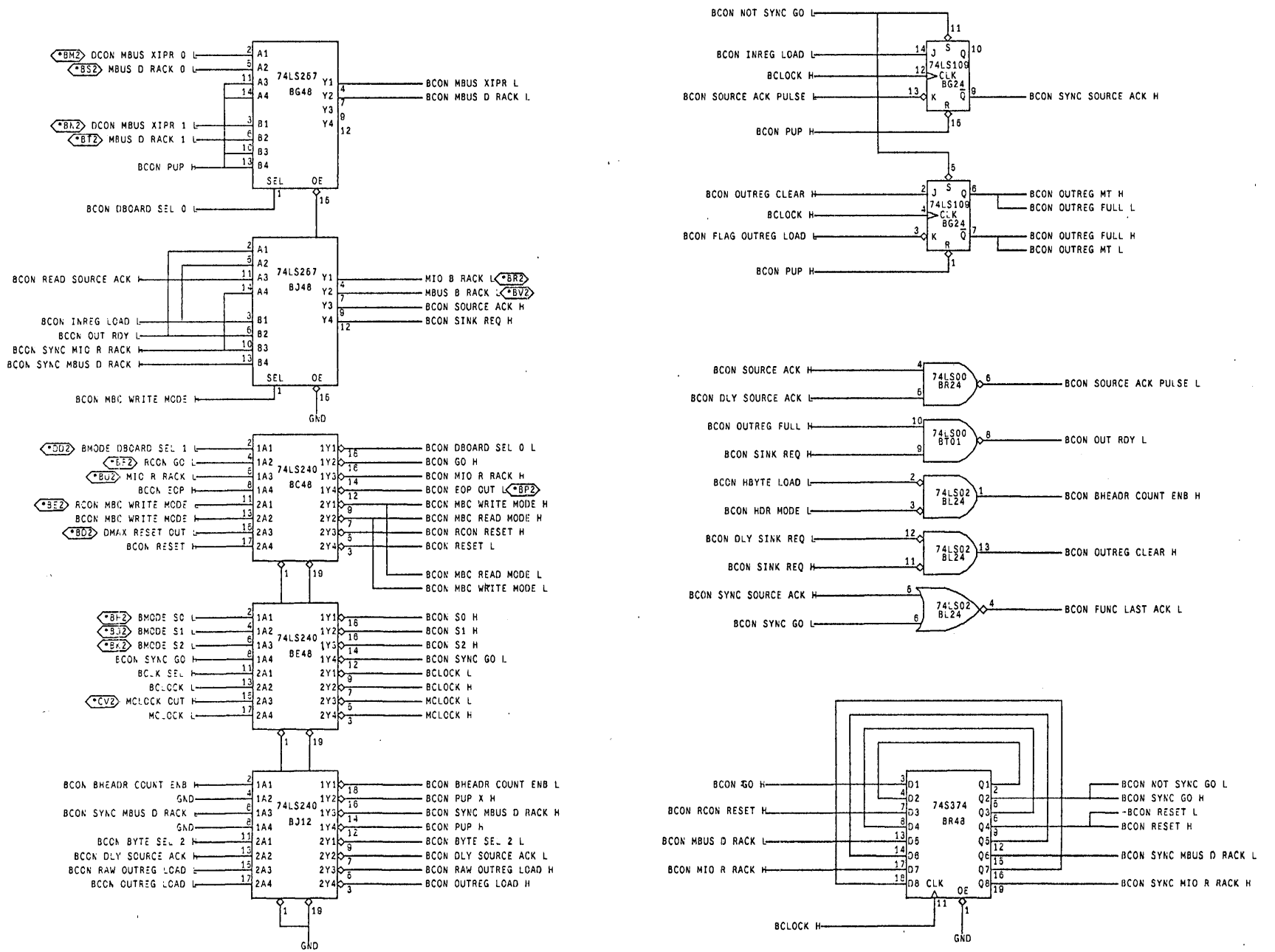
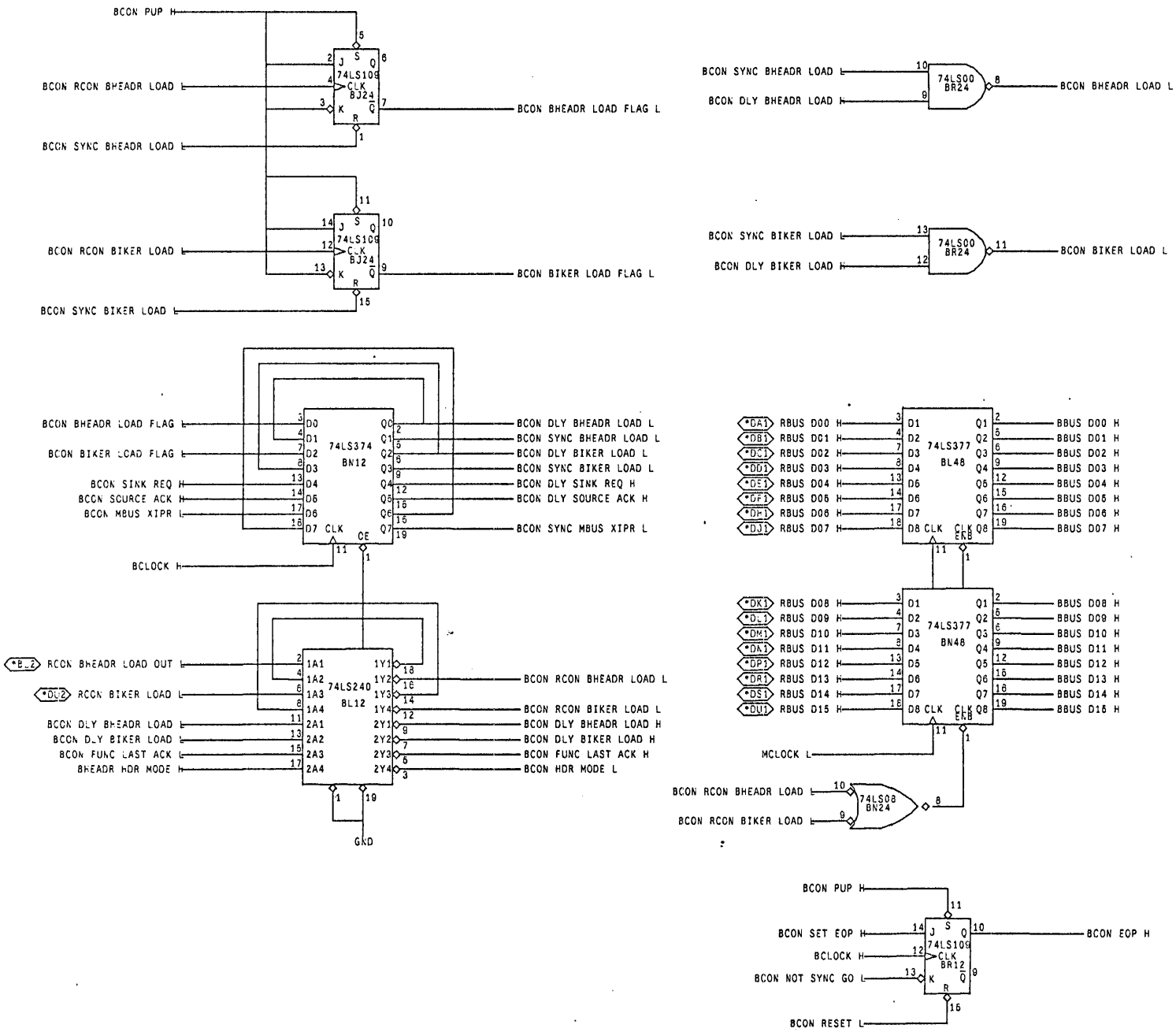




TITLE
BARREL SHIFTER BRD, HEADER BYTE COUNTER

FILE
BCON3 [MEIGFS]

DATE
13-Oct-82 14:24

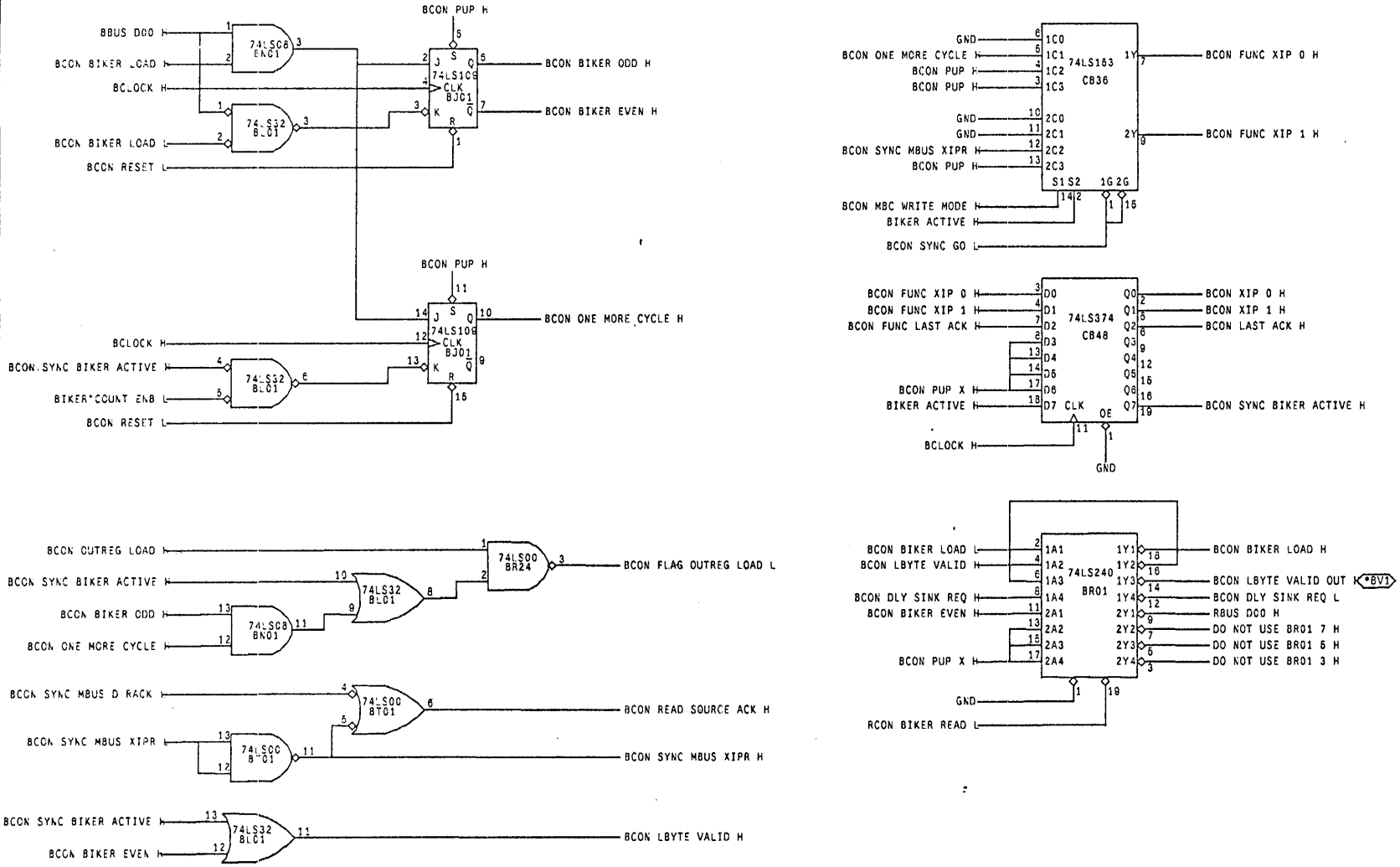
PAGE
OF

TITLE: BARREL SHIFTER BRD, HEADER BYTE COUNTER

FILE: BCON4[MEIGFS]

DATE: 19-May-82 21:32

PAGE: OF



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TITLE: BARREL SHIFTER BRD, HEADER BYTE COUNTER

FILE: BHEADR[MEIGFS]

DATE: 19-May-82 21:34

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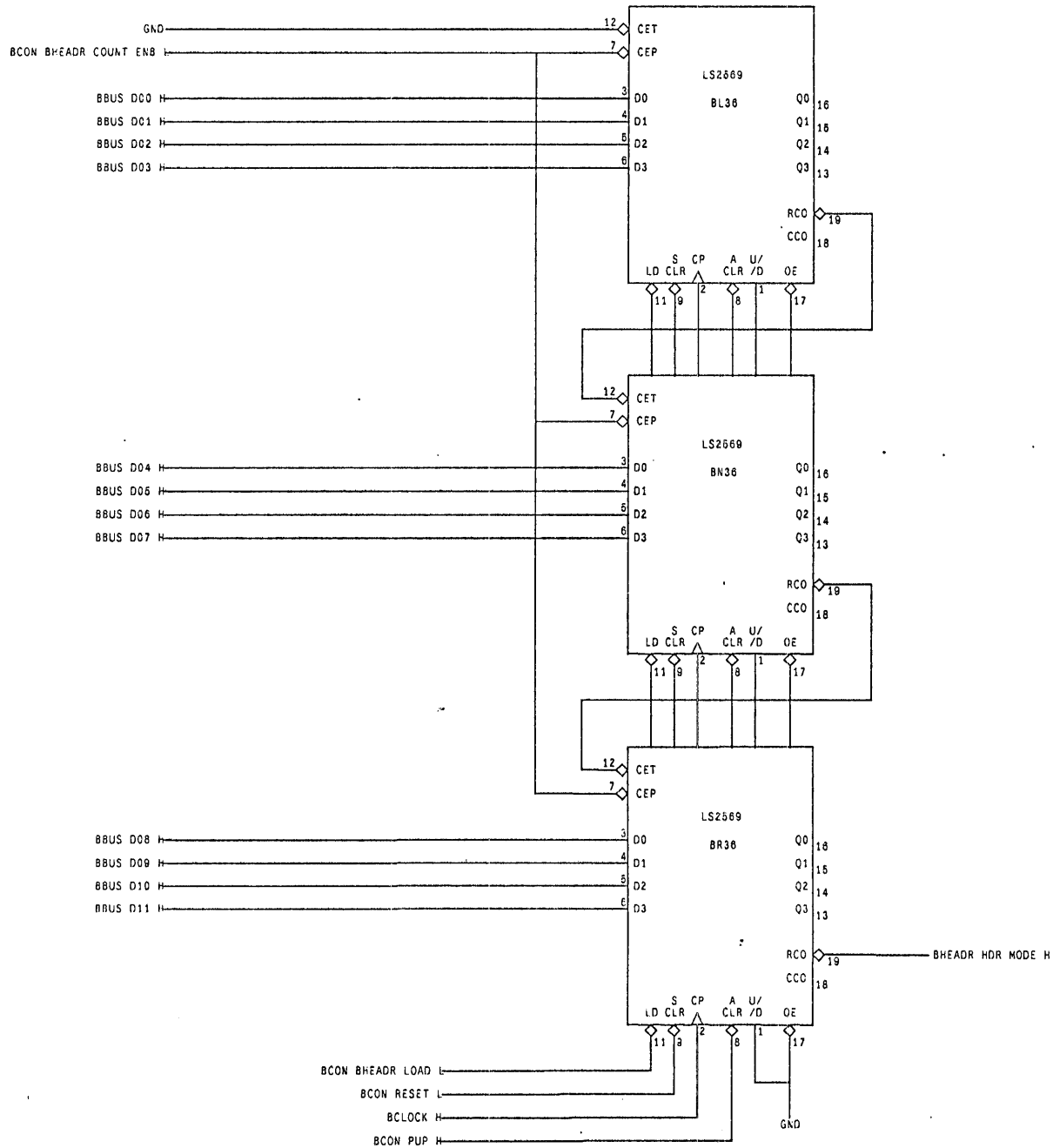

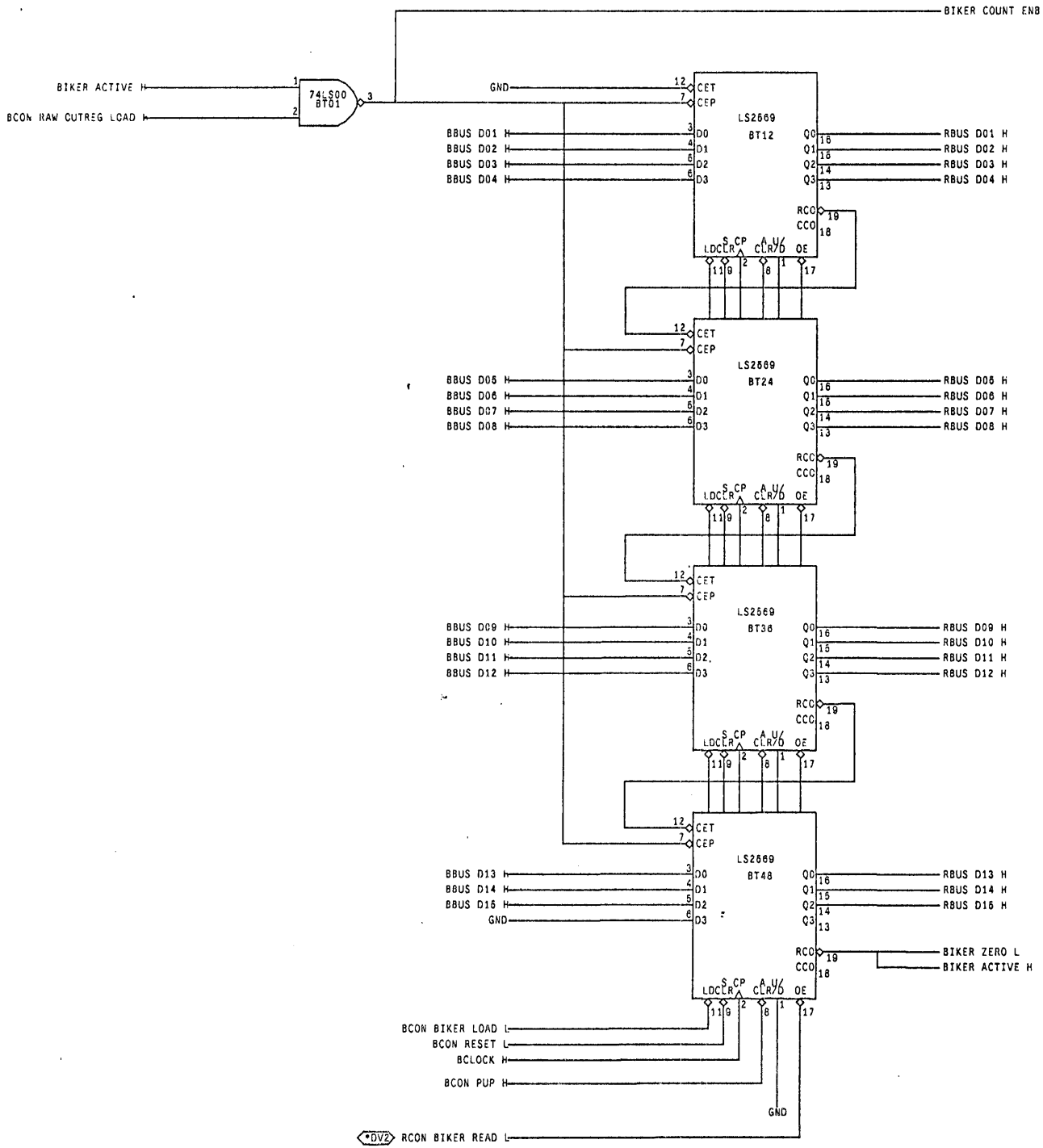

TITLE
BARREL SHIFTER BRD, BYTE COUNT REGISTER

FILE
BIKER[MEIGFS]

DATE
27-Jul-82 15:53

PAGE
OF

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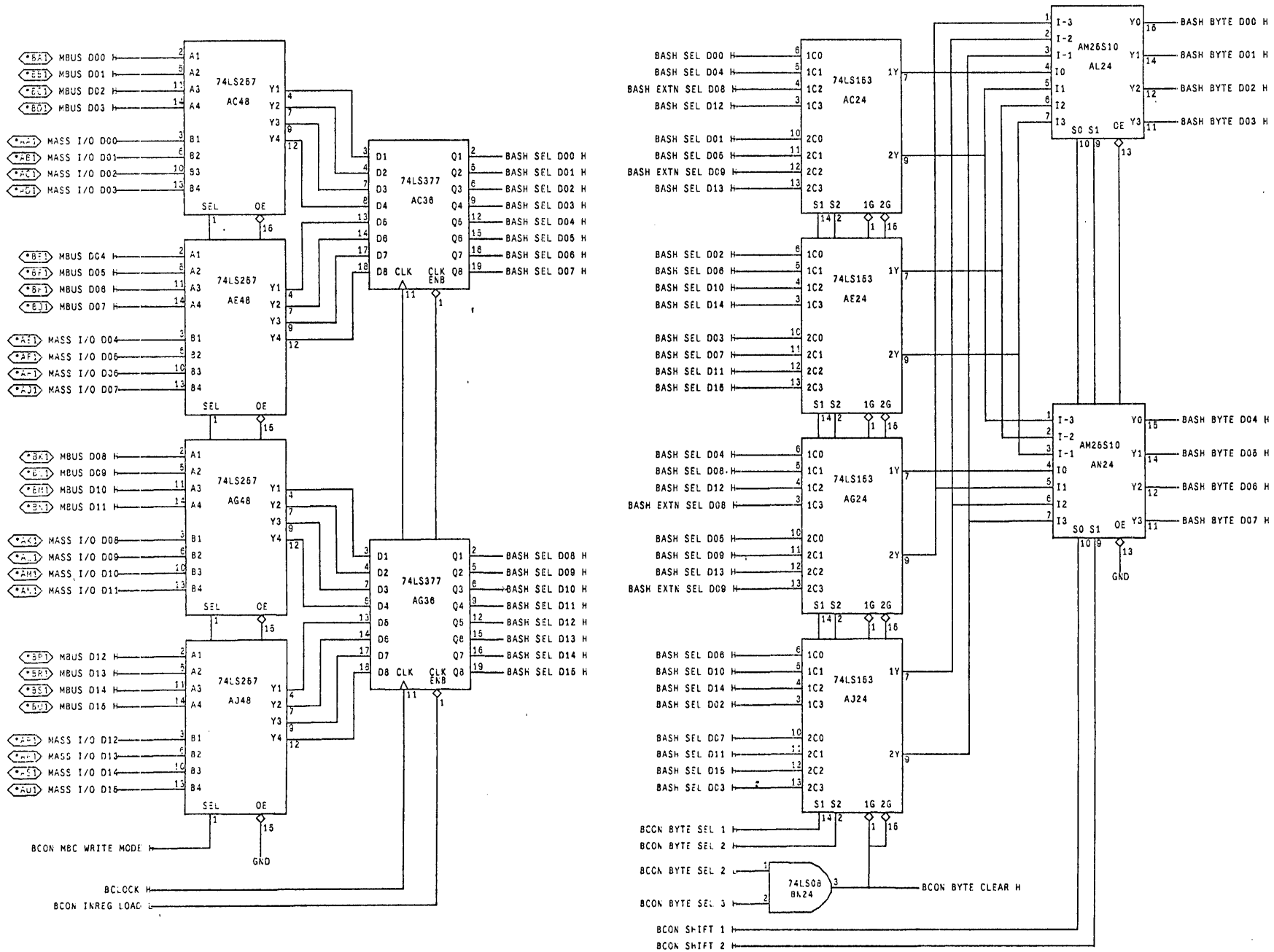

TITLE: BARREL SHIFTER BRD., INPUT DATA PATH

FILE: BASH1[MEIGFS]

DATE: 13-Oct-82 14:25

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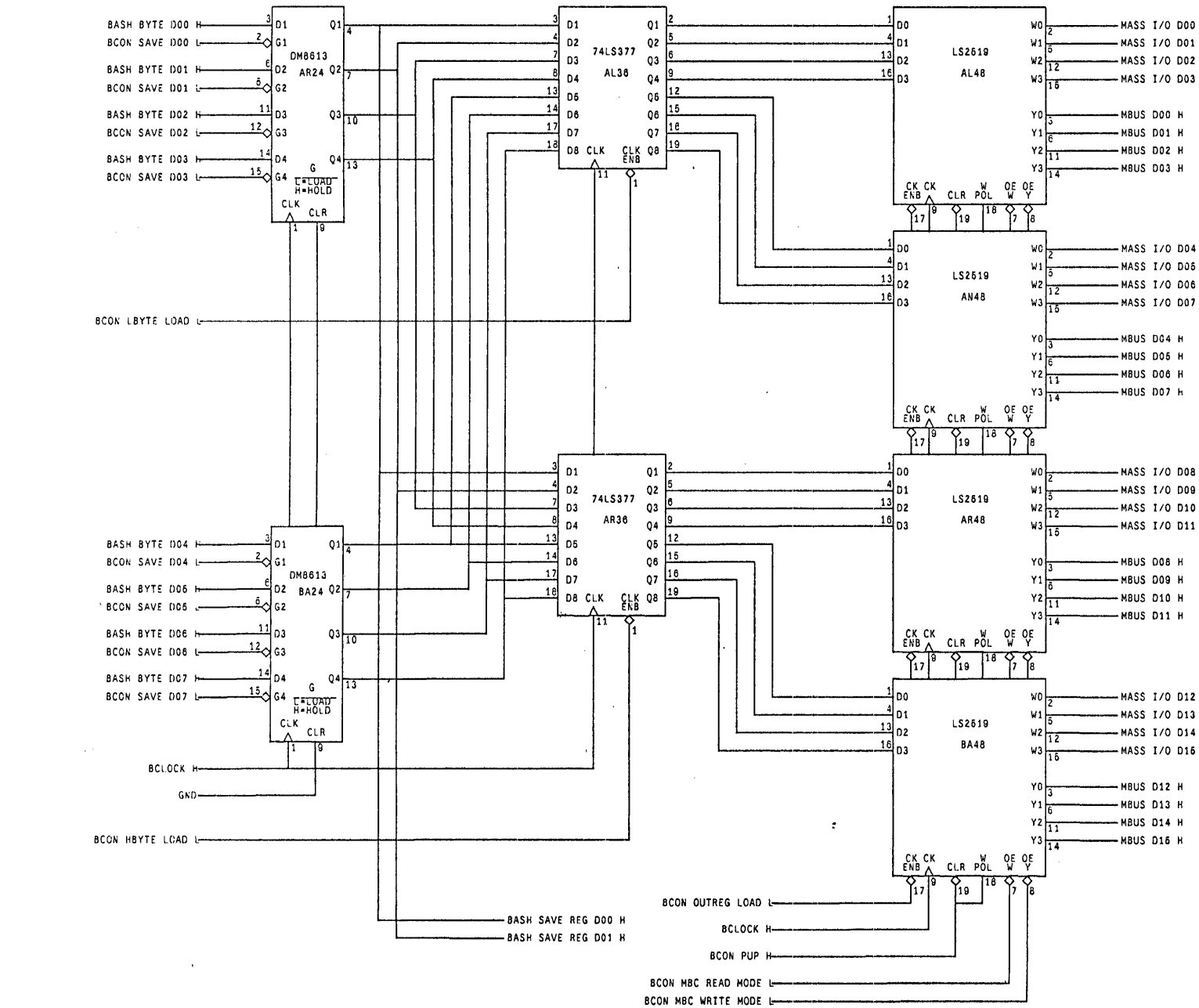

TITLE: BARREL SHIFTER BRD, , OUTPUT DATA PATH

FILE: BASH2[MEIGFS]

DATE: 12-May-82 14:27

PAGE: 6

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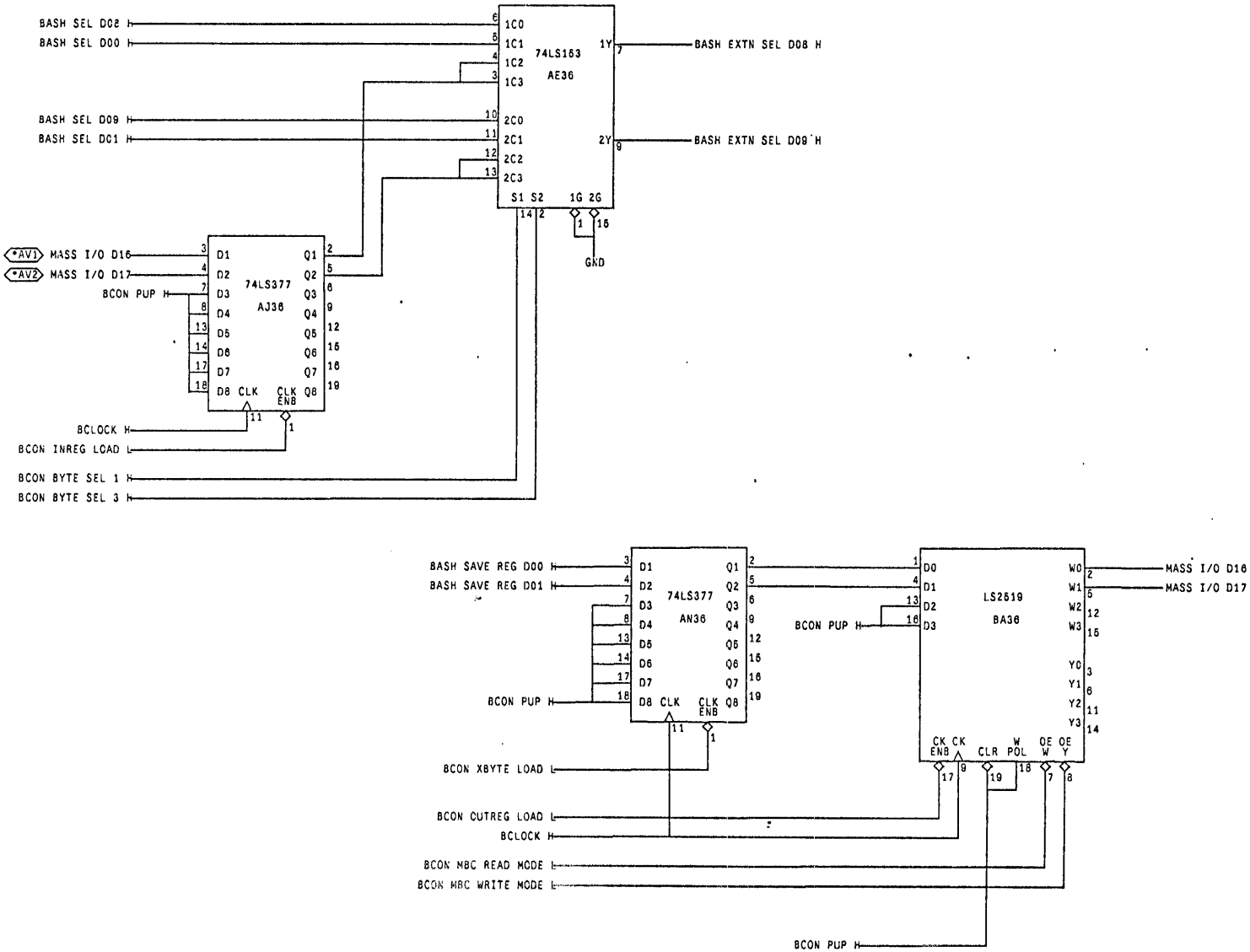
TITLE: BARREL SHIFTER BRD, EXTEND BITS (D16::17)

FILE: BASH3[MEIGFS]

DATE: 12-May-82 14:28

PAGE: C6



DUAL-WIDTH DEC BOARD PINOUTS

BOARD NAME: BARREL SHIFTER

COLUMN (A,C,E): A

Signal Name					Signal Name
MASS I/O DØØ	1	A	2		+5
DØ1	1	B	2		-15
DØ2	1	C	2		GND
DØ3	1	D	2		
DØ4	1	E	2		
DØ5	1	F	2		
DØ6	1	H	2		
DØ7	1	J	2		
DØ8	1	K	2		
DØ9	1	L	2		
D1Ø	1	M	2		
D11	1	N	2		
D12	1	P	2		
D13	1	R	2		
D14	1	S	2		
GND	1	T	2		
D15	1	U	2		
D16	1	V	2		MASS I/O D17

COLUMN (B,D,F): B

Signal Name					Signal Name
MBUS DØØ H	1	A	2		+5
DØ1	1	B	2		-15
DØ2	1	C	2		GND
DØ3	1	D	2		DMAX RESET OUT L
DØ4	1	E	2		RCON MBC WRITE MODE L
DØ5	1	F	2		RCON GO L
DØ6	1	H	2		BMODE SØ L
DØ7	1	J	2		BMODE S1 L
DØ8	1	K	2		BMODE S2 L
DØ9	1	L	2		DMAX BHEADR LOAD L
D1Ø	1	M	2		DCON END READ Ø L
D11	1	N	2		DCON END READ 1 L
D12	1	P	2		BCON EOP L
D13	1	R	2		MIØ TRANSFER REQ L
D14	1	S	2		MBUS TRANSFER REQ ØL
GND	1	T	2		MBUS TRANSFER REQ 1 L
D15	1	U	2		MIO TRANSFER ACK L
BCON L BYTE VALID H	1	V	2		MBUS TRANSFER ACK L

DUAL-WIDTH DEC BOARD PINOUTS

BOARD NAME: BARREL SHIFTER

COLUMN (A,C,E): C

Signal Name					Signal Name
	1	A	2		+5
	1	B	2		-15
	1	C	2		GND
	1	D	2		
	1	E	2		
	1	F	2		
	1	H	2		
	1	J	2		
	1	K	2		
	1	L	2		
	1	M	2		
	1	N	2		
	1	P	2		
	1	R	2		
	1	S	2		
GND	1	T	2		
BCLOCK OUT H	1	U	2		GND
GND	1	V	2		MCLOCK OUT H

COLUMN (B,D,F): D

Signal Name					Signal Name
RBUS DØØ H	1	A	2		+5
DØ1	1	B	2		-15
DØ2	1	C	2		GND
DØ3	1	D	2		BMODE DBOARD SEL Ø L
DØ4	1	E	2		
DØ5	1	F	2		
DØ6	1	H	2		
DØ7	1	J	2		
DØ8	1	K	2		
DØ9	1	L	2		
DIØ	1	M	2		
DI1	1	N	2		
DI2	1	P	2		
DI3	1	R	2		
DI4	1	S	2		
GND	1	T	2		
DI5	1	U	2		RCON BIKER LOAD L
	1	V	2		RCON BIKER MERD L

SFMCB

WPKT/ WRITE PACKET
RDR601/
RDR6B/
RDR6C/
RDR6CC/
RHERR/
P/
T300LP/
T301LP/
SNDDAT/
SKTRET/
EPTICP/
RECBUF

RH20 60-63

CCW ADDR = 0 FOR FILL XFER (EPT LOC FOR RD)

ICW IN EPT 00-37 (CHAN # * 4)

DEVICE

SYNC CLOCK DRIVEN BY DEVICE

LE CHG DATA ON RD

TE RH ACCEPTS DATA

WRT CLK DRIVEN BY RH - ECHO OF SYN CLK

LE ACCEPTS DATA ON WR STBS

TE RH CHG DATA

EBL DCL ASSERTS AFTER LAST SYNC CLK

EXC DCL ASSERTS AT OR PRIOR TO DCL

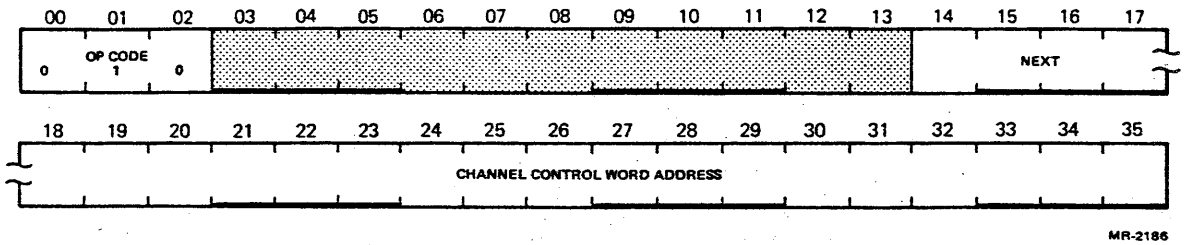
DCL ASSERTS AT END OF EBL

RUN DCL SAMPLED AT TE. OF EBL FOR CONTINUE

CHANNEL COMMAND CODES

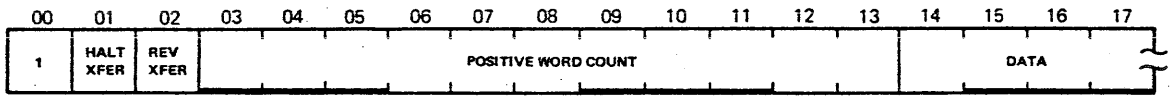
Code	Operation	Code	Operation
000	HALT	100	FORWARD DATA TRANSFER (DO NOT HALT)
001	NOT USED	101	REVERSE DATA TRANSFER (DO NOT HALT)
010	JUMP	110	FORWARD DATA TRANSFER (HALT)
011	NOT USED	111	REVERSE DATA TRANSFER (HALT)

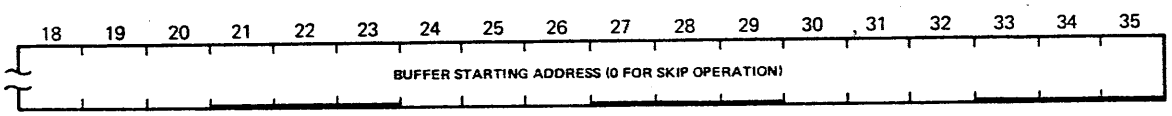
CCW JUMP



MR-2186

CCW DATA TRANSFER





NOTE: WORD COUNT FIELD = POSITIVE WORD COUNT STORED IN CHAN AND DECREMENTED, IF BIT 1 = 1 HALT WHEN WC = 0
ADDRESS = 22 BIT PHYSICAL ADDRESS:

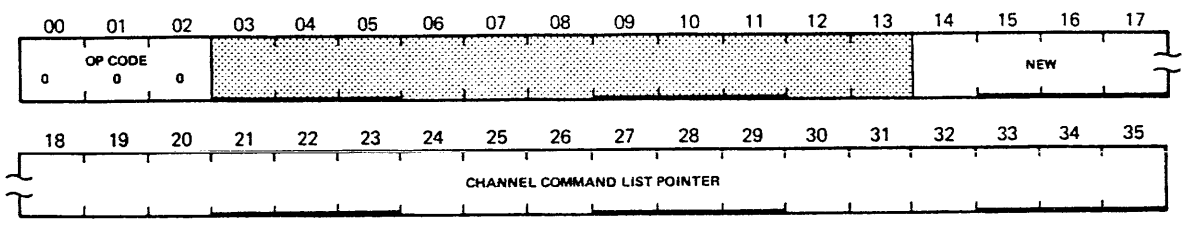
IF = 0; SKIP
IF DEVICE READ; DON'T MOVE DATA TO MEMORY
IF DEVICE WRITE; CHANNEL SUPPLIES FILL DATA FROM EXEC PROCESS TABLE LOCATIONS 60--63 TO WRITE REMAINDER OF DRIVES DATA BLOCK

01 HALT AFTER LAST TRANSFER

02 REVERSE DATA TRANSFER

MR-2187

CCW HALT



MR-2185

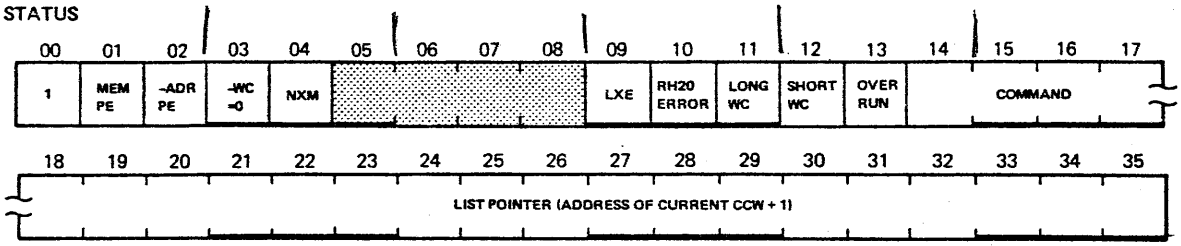
COMPANY CONFIDENTIAL

WORD 0 JUMP

NOTE: EXECUTED AS A RESULT OF RH20 ASSERTING CBUS RESET.

MR-2188

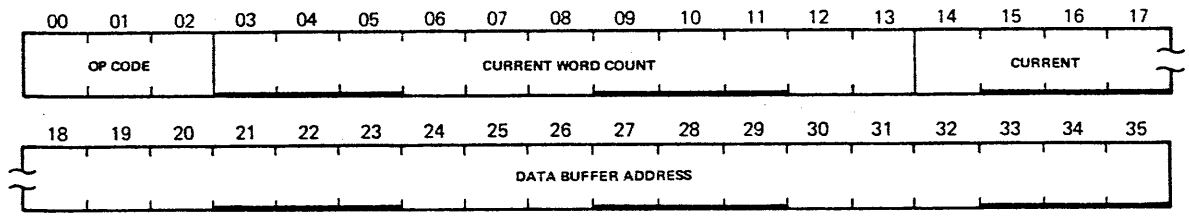
WORD 1 STATUS



01 MEMORY PARITY ERROR
02 NOT ADDRESS PARITY ERROR
03 CHAN WORD COUNT DID NOT = 0 WHEN CHAN DID STORE TO EPT
04 CHAN REF NON EXIST MEM
09 ERROR DETECTED AFTER RH20 TERM XFER, CHAN ABORTS NEXT XFER
10 RH20 TRIED TO START CHAN WHEN CHAN WAS NOT READY
11 RH20 COMP XFER, BUT WORD COUNT IN CCW NOT REACHED
12 CHAN XFERRED DATA SPEC BY CCW, BUT RH20 STILL HAS DATA
13 IF DEV READ, RH20 SENT DATA BUT CHAN BUFF WERE FULL
IF DEV WRITE, RH20 REQ DATA BUT CHAN BUFF WERE EMPTY

MR-2189

WORD 2 STATUS



<00:01> CURRENT FUNCTION CODE IN CCW
00 = HALT
01 = NOT IMPLEMENTED
02 = JUMP
03 = NOT IMPLEMENTED
04 = FWD DATA XFER
05 = REV DATA XFER
06 = FWD DATA XFER (HALT LAST XFER)
07 = REV DATA XFER (HALT LAST XFER)

<03:13> NORMALLY 0 AT END OF TRANSFER
<14:35> ADDRESS OF LAST DATA TRANSFERRED TO/FROM MEMORY

MR-2190

WORD 3 STATUS

NOTE: WORD 3 OF THE CHANNEL LOGOUT AREA IS NOT CURRENTLY USED BUT THE PROGRAM MAY USE IT AS THE VECTOR INTERRUPT ADDRESS FOR THE ASSOCIATED CHANNEL.

MR-2191

COMPANY CONFIDENTIAL

CHAN

RH/DISK Function Codes

Nondata Transfer Codes			Data Transfer Codes		
Code	Fixed Head	Moving Head	Code	Fixed Head	Moving Head
01	NO-OP	NO-OP	51*	WR CK DATA	WR CK DATA
03		UNLOAD	53*		WR CK HDR/DATA
05		SEEK	61	WR DATA	WR DATA
07		RECAL	63		WR HRD/DATA
11	DRIVE CLEAR	DRIVE CLEAR	71	RD DATA	RD DATA
13		RELEASE	73		RD HDR/DATA
15		OFFSET			
17		RET TO C.L.			
21	RD-IN PRESET	RD-IN PRESET			
23		PACK ACK			
31	SEARCH	SEARCH			

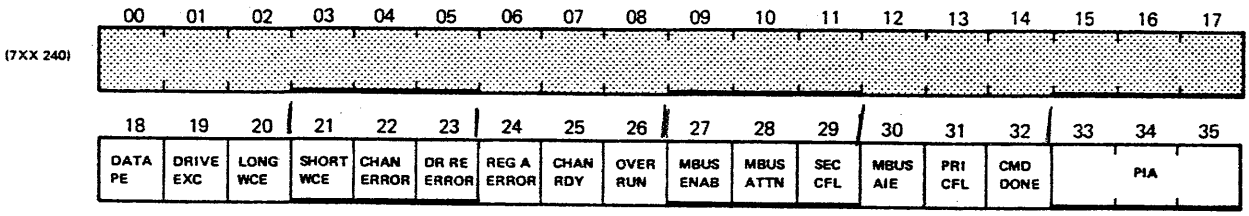
*Implemented in RH11 controllers only.

RH/TAPE Function Codes

Nondata Transfer Codes			Data Transfer Codes	
Code	Magnetic Tape	Code	Magnetic Tape	
01	NO-OP	51*	WR CHECK FORWARD	
03	REWIND - OFF LINE	57*	WR CHECK REVERSE	
07	REWIND	61	WR FORWARD	
11	DRIVE CLEAR	71	RD FORWARD	
21	RD-IN PRESET	77	RD REVERSE	
25	ERASE			
27	WR FILE MARK			
31	SPACE FORWARD			
33	BACKSPACE			

*Implemented in RH11 controllers only.

CONI RHn



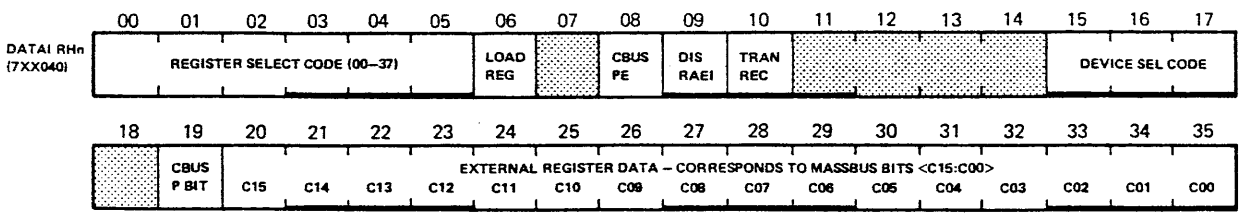
NOTE: BITS 24, 28 AND 32 WILL CAUSE AN INTERRUPT.

18	DATA BUS PARITY ERROR
19	DRIVE EXCEPTION ERROR
20	LONG WORD COUNT ERROR
21	SHORT WORD COUNT ERROR
22	CHANNEL ERROR
23	DRIVE RESPONSE ERROR
24	REGISTER ACCESS ERROR (CBTO OR CBPE)
25	CHANNEL READY TO BEGIN TRANSFER
26	DATA OVERRUN ERROR
27	MASSBUS ENABLE
28	MASSBUS ATTENTION
29	SECONDARY COMMAND FILE LOADED
30	MASSBUS ATTENTION INTERRUPT ENABLED
31	PRIMARY COMMAND FILE LOADED
32	COMMAND DONE
<33:35>	PRIORITY INTERRUPT CHANNEL

MR-2048

Reg	Adr	R/W	Name
--		R W	PREP - Preparation Register (not addressed directly)
7	0	R W	SBAR - Secondary Block Address Register
7	1	R W	STCR - Secondary Transfer Control Register
7	2	R -	PBAR - Primary Block Address Register
7	3	R -	PTCR - Primary Transfer Control Register
7	4	R W	IVIR - Interrupt Vector Index Register
7	5	R -	RR - Read Register (Diagnostic Use)
7	6	- W	WR - Write Register (Diagnostic Use)
7	7	- W	DCR - Diagnostic Control Register (Diagnostic Use)

EXT – External Registers (00–37)



NOTE: REFER TO PREP REG FOR DEFINITION OF BITS <00:05>, 6, AND <15:17>.

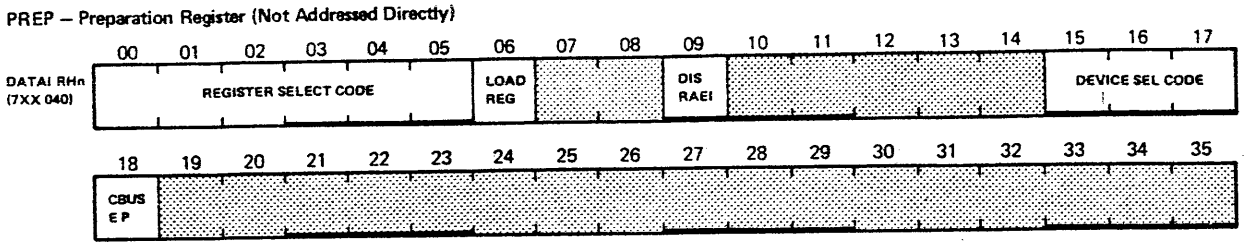
08	CONTROL BUS PARITY ERROR
09	DISABLE REG ACCESS ERROR, INTERRUPTS AND SUBSEQUENT REG WRITES
10	TRANSFER RECEIVED (DEVICE RESPONDED)
19	CONTROL BUS PARITY BIT

MR-2050

COMPANY CONFIDENTIAL

RH20 I/O

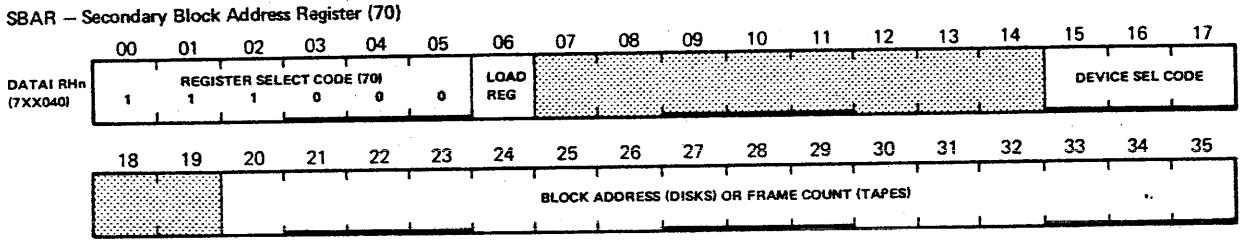
PREP – Preparation Register (Not Addressed Directly)



NOTE: REFER TO DATAO PREP REG FOR DEFINITIONS OF BITS.

MR-2048

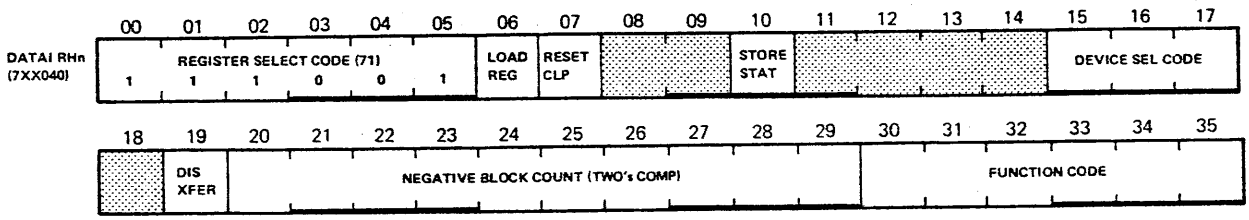
SBAR – Secondary Block Address Register (70)



NOTE: REFER TO PREP REG FOR DEFINITIONS OF <00:05>, 06 AND <15:17>.

MR-2052

STCR – Secondary Transfer Control Register (71)



NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05>, 06, AND <15:17>.

Refer to the function code tables which precede the RH10 I/O bit maps.

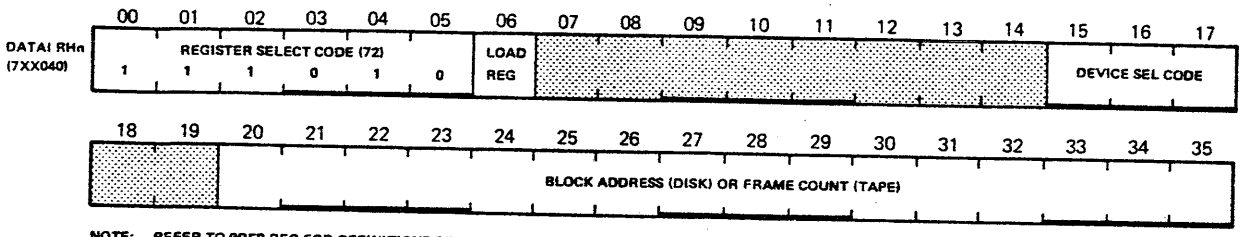
07 RESET COMMAND LIST POINTER
10 STORE CHANNEL STATUS CONTROL BIT
19 DISABLE TRANSFER ERROR STOP BIT

MR-2054

COMPANY CONFIDENTIAL

RH20 I/O

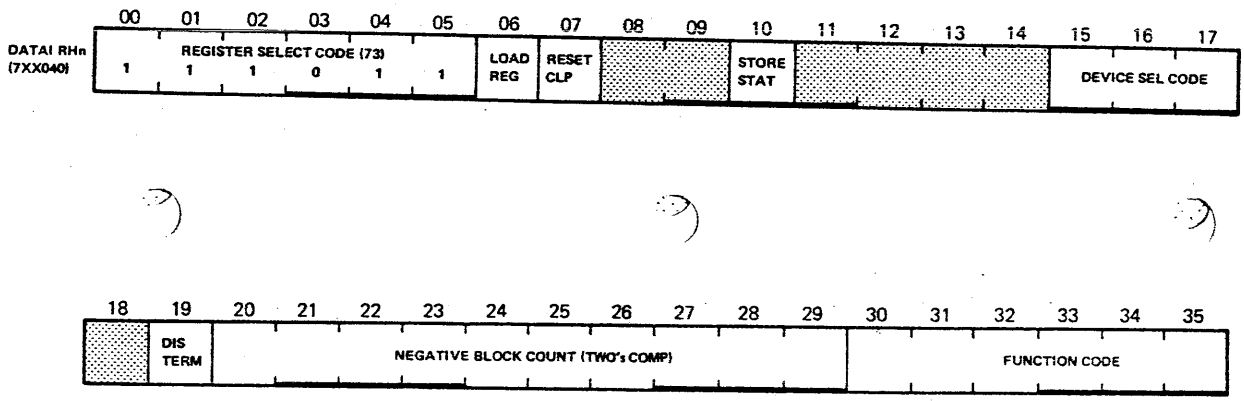
PBAR – Primary Block Address Register (72)



NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05>, 06, AND <15:17>.
REFER TO SBAR REG FOR DEFINITIONS OF BITS <20:35>.

MR-2055

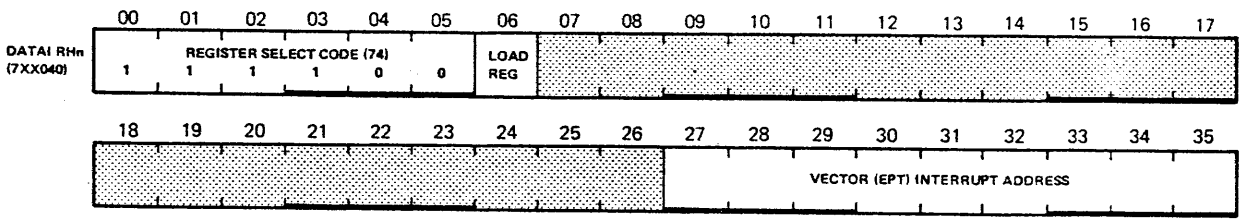
PTCR – Primary Transfer Control Register (73)



NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05>, 06, AND <15:17>.
Refer to the function code tables which precede the RH10 I/O bit maps.
REFER TO STCR REG FOR DEFINITION OF BITS 07, 10, AND 19.

MR-2056

IVIR – Interrupt Vector InJex Register (74)



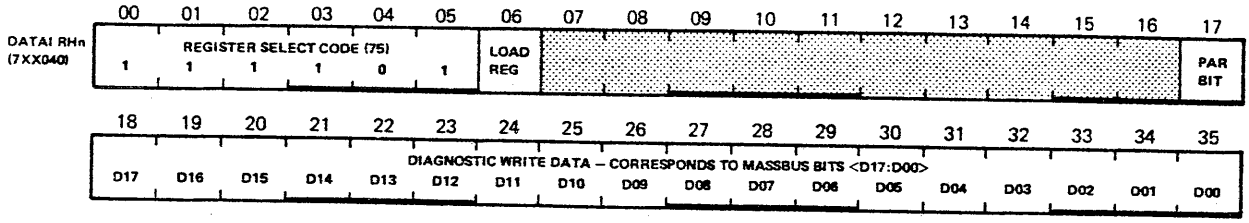
NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05> AND 06.

MR-2058

COMPANY CONFIDENTIAL

RH20 I/O

RR – Read Register (75) Diagnostic Use

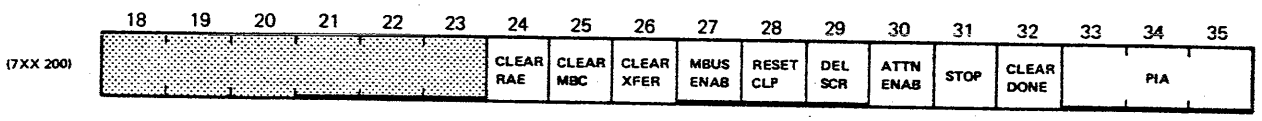


NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05> AND 06.

17 PARITY BIT
<18:35> WRITE DATA AND PARITY (17) LOOPED BACK VIA MASSBUS XCVRS DURING DIAG WRITE

MR-2059

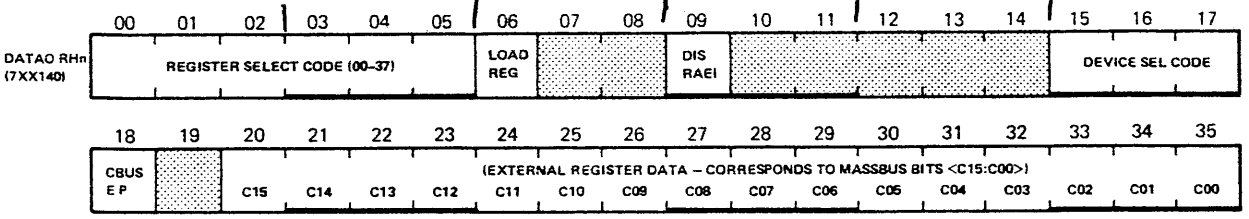
CONO RHn



24 CLEAR REGISTER ACCESS ERROR
25 CLEAR MASSBUS CONTROLLER
26 CLEAR TRANSFER ERRORS
27 MASSBUS ENABLE
28 RESET COMMAND LIST POINTER
29 DELETE SECONDARY CONTROL REGISTER
30 ATTENTION INTERRUPT ENABLE
31 STOP TRANSFER (STATUS BITS NOT CLEARED)
<33:35> PRIORITY INTERRUPT CHANNEL

MR-2045

EXT – External Registers (00–37)



NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05>, 06, AND <15:18>.

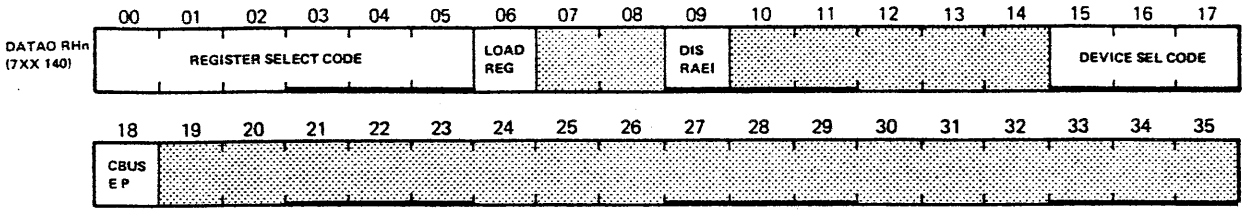
09 DISABLE REG ACCESS ERROR, INTERRUPTS AND SUBSEQUENT REG WRITES.

MR-2049

RH20 I/O

COMPANY CONFIDENTIAL

PREP – Preparation Register (Not Addressed Directly)

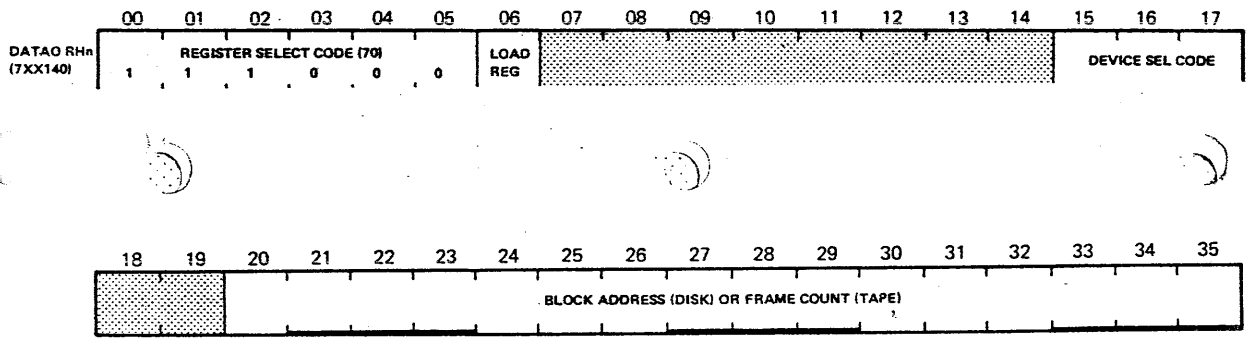


NOTE: BITS <00:05>, 06 AND <15:17> HAVE A COMMON DEFINITION FOR MANY RH REGISTERS, TO ELIMINATE REDUNDENCY THEY ARE DESCRIBED ONCE HERE.

<00:05> REGISTER SELECT CODE. SPECIFIES WHICH REGISTER IS TO BE LOADED IF BIT 06 IS SET.
06 LOAD REGISTER. IF 0 LOAD PREP REG. IF 1 LOAD REG SPECIFIED BY BITS <00:05>
09 DISABLE REG ACCESS ERROR INTERRUPTS AND SUBSEQUENT REG WRITES
<15:17> DEVICE SELECT CODE. SPECIFIES WHICH DEVICE (0–7) IS TO BE USED IN THE OPERATION.
18 CONTROL BUS EVEN PARITY

MR-2047

SBAR – Secondary Block Address Register (70)

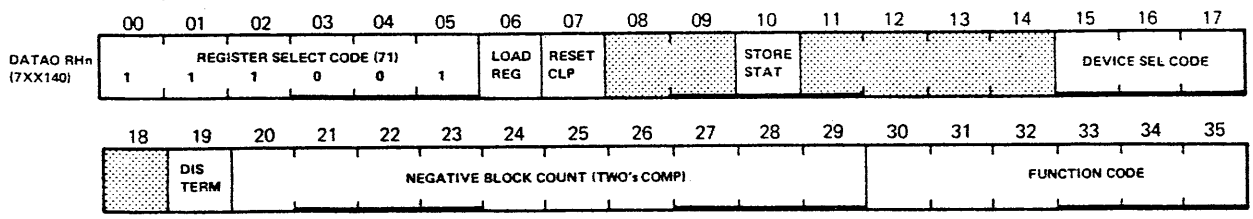


NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05>, 06, <15:17>.

<20:35> TAPE – FRAME COUNT 20 = MSD 35 = LSD
<23:27> DISK – TRACK ADDRESS
<31:35> DISK – SECTOR ADDRESS

MR-2051

STCR – Secondary Transfer Control Register (71)



NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05>, 06, AND <15:17>.

Refer to the function code tables which precede the RH10 I/O bit maps.

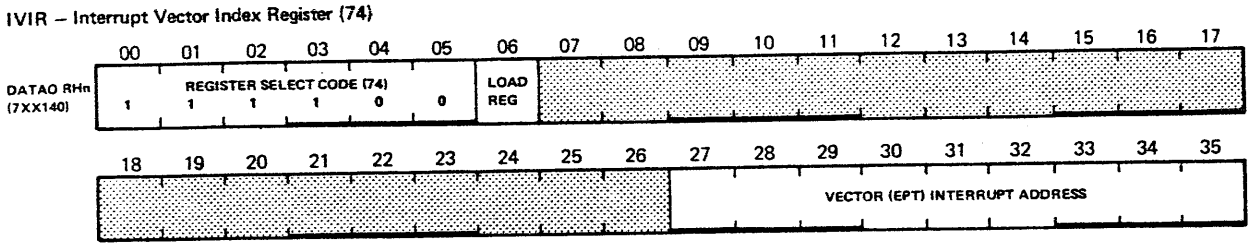
07 RESET COMMAND LIST POINTER
10 STORE CHANNEL STATUS CONTROL BIT
19 DISABLE TERMINATION OF TRANSFERS DUE TO DATA BUS PARITY ERRORS OR DRIVE EXCEPTION ERRORS.

MR-2053

COMPANY CONFIDENTIAL

RH20 I/O

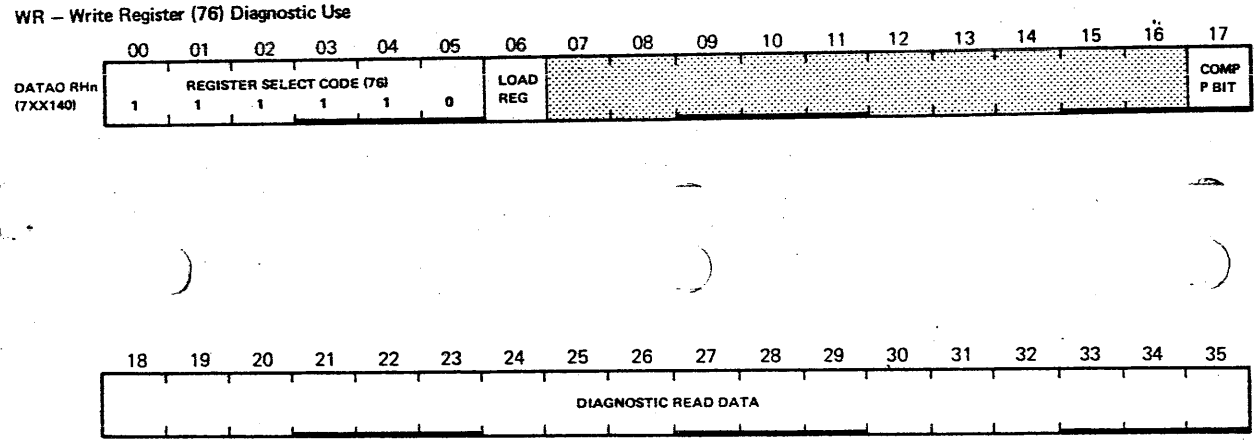
IVIR – Interrupt Vector Index Register (74)



NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05> AND 06.

MR-2057

WR – Write Register (76) Diagnostic Use

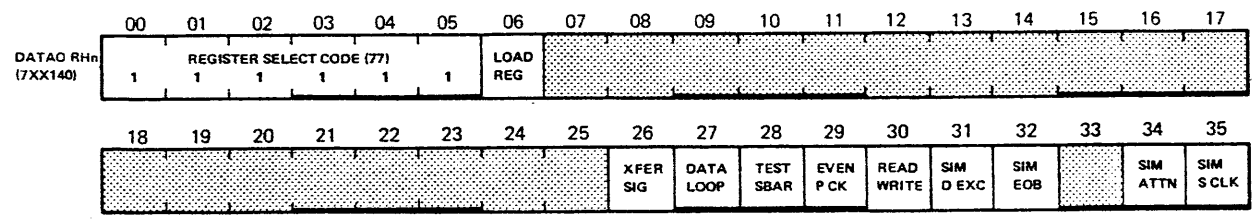


NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05> AND 06.

17 COMPUTED PARITY BIT (BY PROG) FOR DIAG READ DATA

MR-2060

DCR – Diagnostic Control Register (77) Diagnostic Use



NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05> AND 06.

26 TRANSFER SIGNAL (SIMULATED)
27 DATA LOOPBACK (VIA MASSBUS XCVRS)
28 TEST SBAR
29 EVEN PARITY CHECK
30 READ/WRITE-SET ON DIAG READ (LOOPS RD DATA VIA MASSBUS XCVRS)
31 SIMULATES DRIVE EXCEPTION
32 SIMULATES END OF BLOCK
34 SIMULATES ATTENTION
35 SIMULATES SYNC CLOCK SIGNAL

MR-2061

MES

SCSS

1	M5903's	
2	RP2	
3	———	
4	BARREL SHIFT	
5	——	
6	VP1	} UNIT Ø
7	NP2	
8	VP1	} UNIT 1
9	NP2	