

M37450S1SP/FP, M37450S2SP/FP, M37450S4SP/FP

MITSUBISHI (MICMPTR/MIPRC) 61E D

8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37450S1SP/FP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or an 80-pin plastic molded QFP. In addition to its simple instruction sets, the ROM, RAM and I/O addresses are placed on the same memory map to enable easy programming. It is suited for office automation equipment and control devices. The low power consumption made possible by the use of a CMOS process makes it especially suitable for battery powered devices requiring low power consumption. It also has a unique feature that enables it to be used as a slave microcomputer.

M37450S1SP/FP, M37450S2SP/FP and M37450S4SP/FP have basically the same functions as M37450M2-XXXSP/FP except the RAM size and the fact that these three need external ROM area. The differences among M37450S1SP/FP, M37450S2SP/FP and M37450S4SP/FP are as shown below.

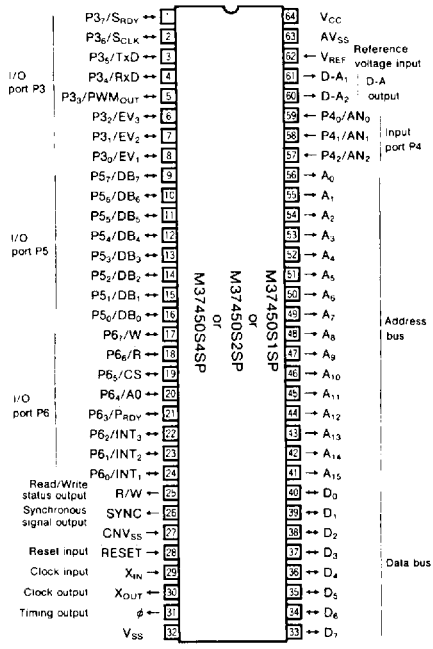
| Type | RAM size |
|---------------|-----------|
| M37450S1SP/FP | 128 bytes |
| M37450S2SP/FP | 256 bytes |
| M37450S4SP/FP | 448 bytes |

Also M37450S1SP has the same function as M37450M2-XXXSP/FP in microprocessor mode and M37450S2SP/FP has the same function as M37450M4-XXXSP/FP in microprocessor mode.

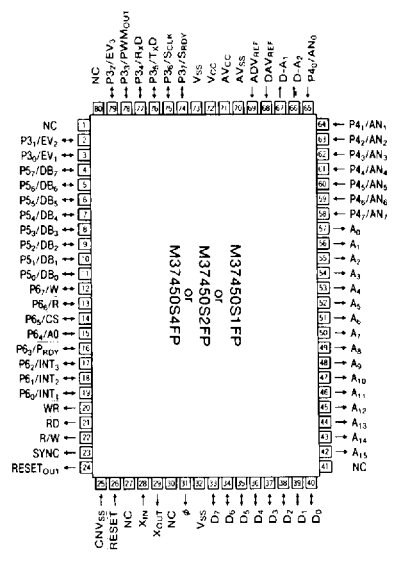
FEATURES

- Number of basic instructions..... 71
69 MELPS 740 basic instructions + 2 multiply/divide instructions
- Memory size ROM..... None
RAM..... 128 bytes (M37450S1SP/FP)
256 bytes (M37450S2SP/FP)
448 bytes (M37450S4SP/FP)
- Instruction execution time
(minimum instructions at 10 MHz frequency)..... 0.8μs
- Single power supply..... 5V ± 10%
- Power dissipation normal operation mode
(at 10MHz frequency)..... 30mW
- Subroutine nesting..... 64 levels max. (M37450S1SP/FP)
- Interrupt..... 15 events
- Master CPU bus interface..... 1 byte
- 16-bit timer..... 3
- 8-bit timer (Serial I/O use)..... 1
- Serial I/O (UART or clock synchronous)..... 1
- A-D converter (8bit resolution)..... 3 channels (DIP)
8 channels (QFP)
- D-A converter (8-bit resolution)..... 2 channels
- PWM output (8-bit or 16-bit)..... 1
- Programmable I/O
(Ports P0, P1, P2, P3, P5, P6)..... 48
- Input (Port P4)..... 3 (DIP), 8 (QFP)
- Output (Port D-A₁, D-A₂)..... 2

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B



Outline 80P6

NC : No connection

APPLICATION

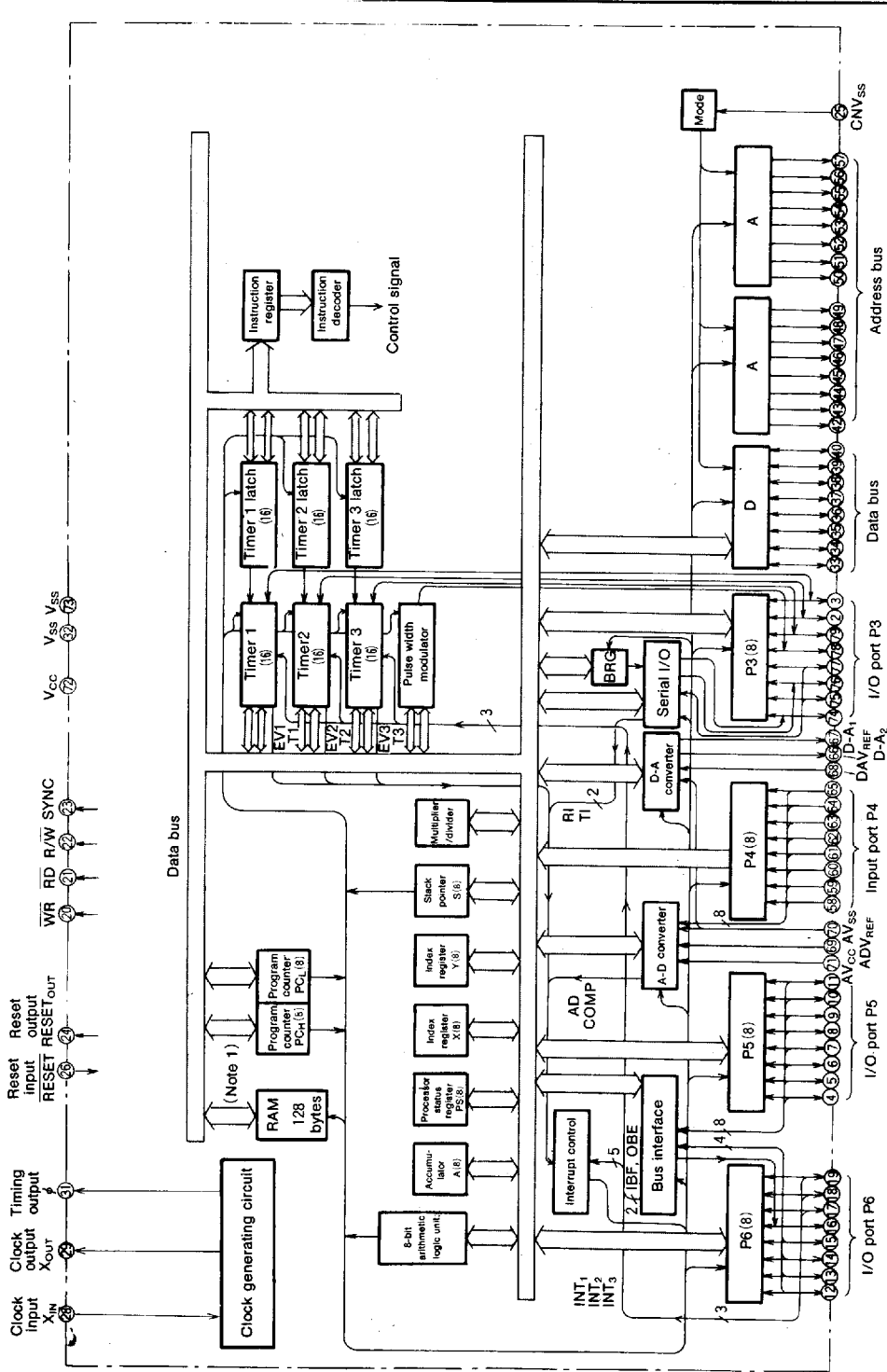
- Slave controller for PPCs, facsimiles and page printers
- HDD, optical disk, inverter and industrial motor controllers
- Industrial robots and machines

**M37450S1SP/FP, M37450S2SP/FP
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8-BIT CMOS MICROCOMPUTER

MITSUBISHI (MICMPTR/MIPRC) 61E D

M37450S1FP BLOCK DIAGRAM



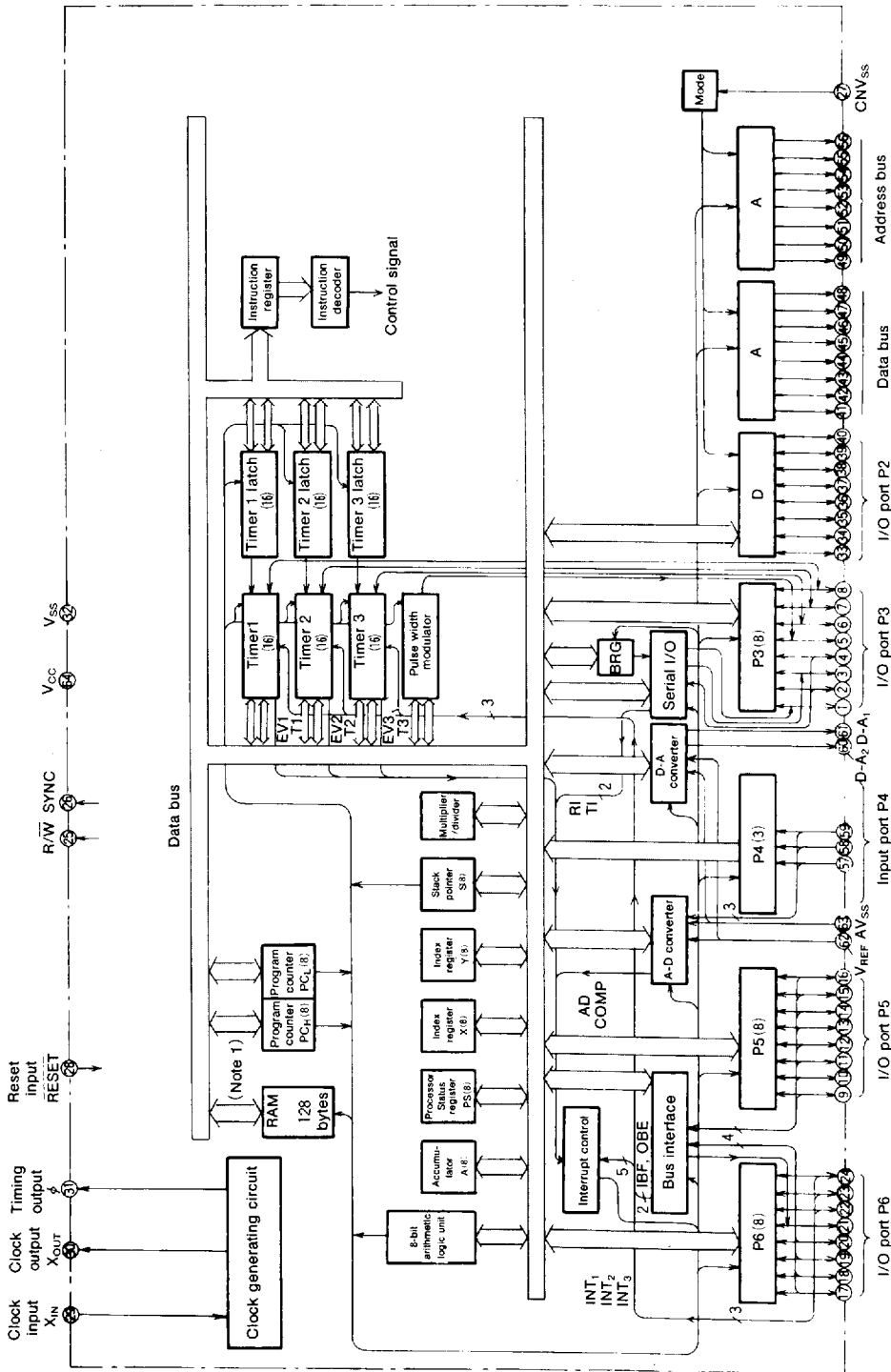
Note 1 : 256 bytes for M37450S2FP and 448 bytes for M37450S4FP.

M37450S1SP/FP, M37450S2SP/FP M37450S4SP/FP

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M37450S1SP BLOCK DIAGRAM



Note 1 : 256 bytes for M37450S2SP and 448 bytes for M37450S4SP.

**M37450S1SP/FP, M37450S2SP/FP
M37450S4SP/FP**

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8-BIT CMOS MICROCOMPUTER

FUNCTIONS OF M37450S1SP/FP, M37450S2SP/FP, M37450S4SP/FP

| Parameter | | Function |
|------------------------------|------------------------------------|--|
| Number of basic instructions | | 71(69 MELPS 740 basic instructions+2) |
| Instruction execution time | | 0.8μs(minimum instructions, at 10MHz of frequency) |
| Clock frequency | | 10MHz(max.) |
| RAM size | M37450S1SP/FP | 128 bytes |
| | M37450S2SP/FP | 256 bytes |
| | M37450S4SP/FP | 448 bytes |
| Input/Output port | P3, P5, P6 | I/O 8-bitX3 |
| | P4 | Input 3-bitX1(8-bitX1 for 80-pin model) |
| | D-A | Output 2-bitX1 |
| Serial I/O | | UART or clock synchronous |
| Timers | | 16-bit timerX3, 8-bit timer(serial I/O baud rate generator)X1 |
| A-D converter | | 8-bitX3 channels(8 channels for 80-pin model) |
| D-A converter | | 8-bitX2 channels |
| Pulse width modulator | | 8-bit or 16-bitX1 |
| Data bus buffer | | 1-byte input and output each |
| Subroutine nesting | | 64-levels(max. for M37450S1SP/FP) |
| Interrupt | | 96-levels(max. for M37450S2SP/FP, M37450S4SP/FP) |
| Clock generating circuit | | Built-in(ceramic or quartz crystal oscillator) |
| Supply voltage | | 5V±10% |
| Power dissipation | | 30mW(at 10MHz frequency) |
| Input/Output characters | Input/Output voltage | 5V |
| | Output current | ±5mA(max.) |
| Operating temperature range | | -10~70°C |
| Device structure | | CMOS silicon gate |
| Package | M37450S1SP, M37450S2SP, M37450S4SP | 64-pin shrink plastic molded DIP |
| | M37450S1FP, M37450S2FP, M37450S4FP | 80-pin plastic molded QFP |

**M37450S1SP/FP, M37450S2SP/FP
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PIN DESCRIPTION

| Pin | Name | Input/ Output | Functions |
|---|-----------------------------|------------------|---|
| V _{CC} , V _{SS} | Supply voltage | | Power supply inputs 5V±10% to V _{CC} , and 0V to V _{SS} . |
| CNV _{SS} | CNV _{SS} | Input | This is connected to V _{CC} . |
| RESET | Reset input | Input | To enter the reset state, the reset input pin must be kept at a "L" for more than 8 clock cycles(under normal V _{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time. |
| X _{IN} | Clock input | Input | This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins. If an external clock is used, the clock source should be connected to the X _{IN} pin and the X _{OUT} pin should be left open. |
| X _{OUT} | Clock output | Output | |
| φ | Timing output | Output | Outputs signal consisting of oscillating frequency divided by four. |
| SYNC | Synchronous signal output | Output | This signal is output "H" during operation code fetch and is used to control single stepping of programs. |
| R/W | Read/Write status output | Output | This signal determines the direction of the data bus. It is "H" during read and "L" during write |
| A ₀ ~A ₁₅ | Address bus | Output | This is 16-bit address bus. |
| D ₀ ~D ₇ | Data bus | I/O | This is 8-bit data bus. |
| P ₃₀ ~P ₃₇ | Input/Output port P3 | I/O | Port P3 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. The output structure is CMOS output. Serial I/O, PWM output, or even I/O function can be selected with a program. |
| P ₄₀ ~P ₄₂ (P ₄₀ ~P ₄₇) | Input port P4 | Input | Analog input pin for the A-D converter. The 64-pin model has three pins and the 80-pin model has eight pins. They may also be used as digital input pins. |
| P ₅₀ ~P ₅₇ | Input/Output port P5 | I/O | An 8-bit input/output port with the same function as P3. This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program. |
| P ₆₀ ~P ₆₇ | Input/Output port P6 | I/O | An 8-bit input/output port with the same function as P0. Pins P ₆₃ ~P ₆₇ change to a control bus for the master CPU when slave mode is selected with a program. Pins P ₆₀ ~P ₆₂ may be programmed as external interrupt input pins. |
| D-A ₁ , D-A ₂ | D-A output | Output | Analog signal from D-A converter is output. |
| V _{REF} | Reference voltage input | Input | Reference voltage input pin for A-D and D-A converter. This pin is for 64-pin model only. |
| ADV _{REF} | A-D reference voltage input | Input | Reference voltage input pin for A-D converter. This pin is for 80-pin model only. |
| DAV _{REF} | D-A reference voltage input | Input | Reference voltage input pin for D-A converter. This pin is for 80-pin model only. |
| AV _{SS} | Analog power supply | | Ground level input pin for A-D and D-A converter. Same voltage as V _{SS} is applied. |
| AV _{CC} | Analog power supply | | Power supply input pin for A-D converter. This pin is for 80-pin model only. Same voltage as V _{CC} is applied. In the case of the 64-pin model AV _{CC} is connected to V _{CC} internally. |
| RD | Read signal output | Output | Control signal output as active "L" when valid data is read from data bus. This pin is for 80-pin model only. |
| WR | Write signal output | Output | Control signal output as active "L" when writing data from data bus to external component. This pin is for 80-pin model only. |
| RESET _{OUT} | Reset output | Output | Control signal output as active "H" during reset. It is used as a reset output signal for peripheral components. This pin is for 80-pin model only. |

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BASIC FUNCTION BLOCKS

The differences between M37450M2-XXXSP/FP and M37450S1SP/FP are noted below. Other functions are the same as M37450M2-XXXSP/FP in microprocessor mode.

MEMORY

A memory map for the M37450S1SP/FP is shown in Figure 1. Addresses FF0₁₆ to FFFF₁₆ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addresses FFE0₁₆ to FFFF₁₆ are vector addresses used for the reset and interrupts (This area must be located in ROM area). Addresses 0000₁₆~00FF₁₆ are the zero page address area.

By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area. Addresses 0000₁₆ to 007F₁₆ are the RAM address area assigned to the M37450S1SP/FP and consist of 128 bytes. Addresses 0000₁₆ to 00BF₁₆ and 0100₁₆ to 013F₁₆ are the RAM address area assigned to the M37450S2SP/FP and consist of 192 bytes and 64 bytes respectively. Addresses 0000₁₆ to 00BF₁₆ and 0100₁₆ to 01FF₁₆ are the RAM address area assigned to the M37450S4SP/FP and consist of 192 bytes and 256 bytes respectively. In addition to data storage, this RAM is used for the stack during subroutine calls and interrupts.

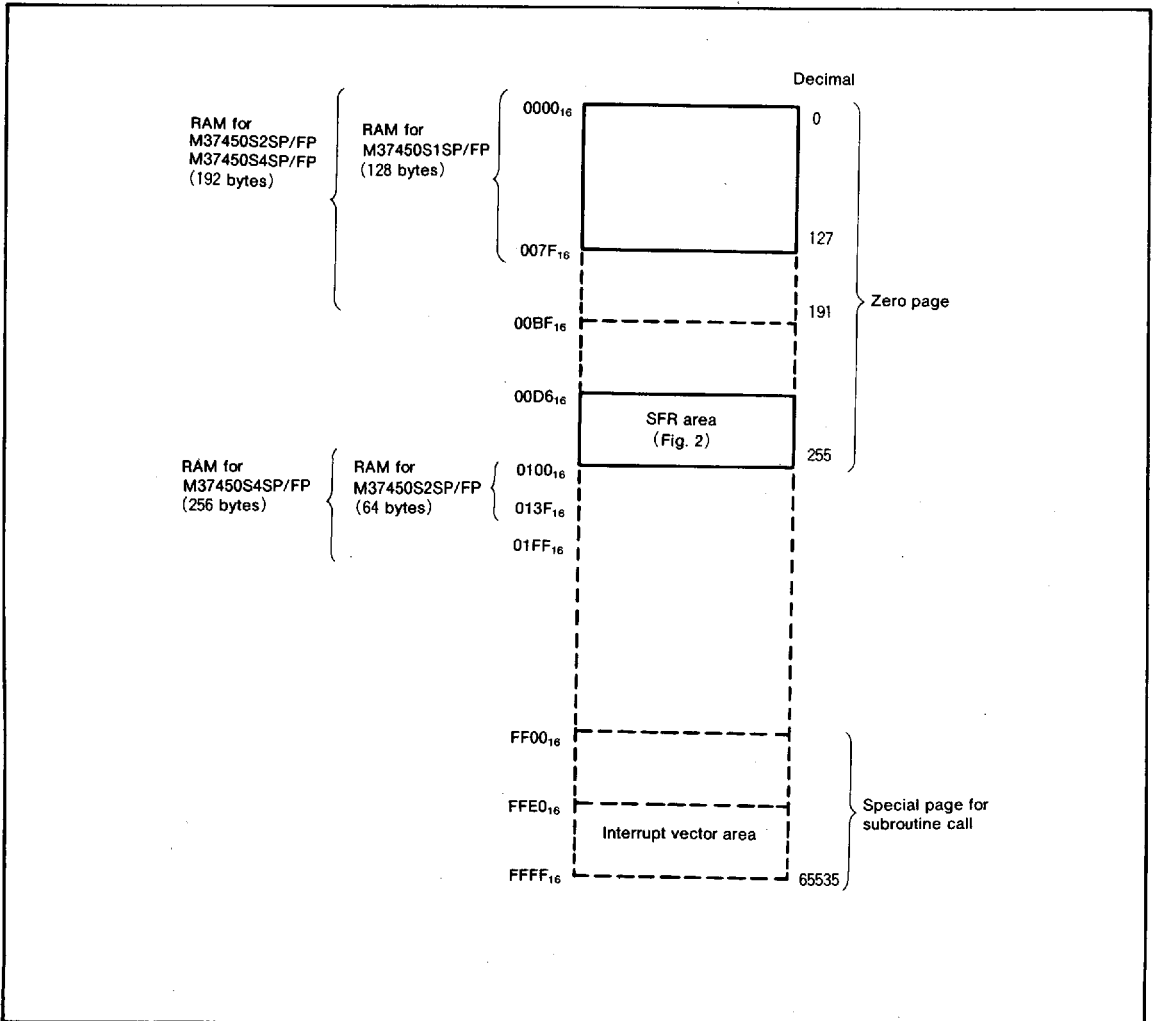


Fig. 1 Memory map

**M37450S1SP/FP, M37450S2SP/FP
M37450S4SP/FP**

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| | |
|--------------------|----------------------------------|
| 00D6 ₁₆ | P3 register |
| 00D7 ₁₆ | P3 directional register |
| 00D8 ₁₆ | P4 register |
| 00D9 ₁₆ | Reserved |
| 00DA ₁₆ | P5 register |
| 00DB ₁₆ | P5 directional register |
| 00DC ₁₆ | P6 register |
| 00DD ₁₆ | P6 directional register |
| 00DE ₁₆ | MISRG1 |
| 00DF ₁₆ | MISRG2 |
| 00E0 ₁₆ | D-A1 register |
| 00E1 ₁₆ | D-A2 register |
| 00E2 ₁₆ | A-D register |
| 00E3 ₁₆ | A-D control register |
| 00E4 ₁₆ | Data bus buffer register |
| 00E5 ₁₆ | Data bus buffer status register |
| 00E6 ₁₆ | Receive/transmit buffer register |
| 00E7 ₁₆ | Serial I/O status register |
| 00E8 ₁₆ | Serial I/O control register |
| 00E9 ₁₆ | UART control register |
| 00EA ₁₆ | Baud rate generator |
| 00EB ₁₆ | PWM register (low-order) |
| 00EC ₁₆ | PWM register (high-order) |
| 00ED ₁₆ | Timer 1 control register |
| 00EE ₁₆ | Timer 2 control register |
| 00EF ₁₆ | Timer 3 control register |
| 00F0 ₁₆ | Timer 1 register (low-order) |
| 00F1 ₁₆ | Timer 1 register (high-order) |
| 00F2 ₁₆ | Timer 1 latch (low-order) |
| 00F3 ₁₆ | Timer 1 latch (high-order) |
| 00F4 ₁₆ | Timer 2 register (low-order) |
| 00F5 ₁₆ | Timer 2 register (high-order) |
| 00F6 ₁₆ | Timer 2 latch (low-order) |
| 00F7 ₁₆ | Timer 2 latch (high-order) |
| 00F8 ₁₆ | Timer 3 register (low-order) |
| 00F9 ₁₆ | Timer 3 register (high-order) |
| 00FA ₁₆ | Timer 3 latch (low-order) |
| 00FB ₁₆ | Timer 3 latch (high-order) |
| 00FC ₁₆ | Interrupt request register 1 |
| 00FD ₁₆ | Interrupt request register 2 |
| 00FE ₁₆ | Interrupt control register 1 |
| 00FF ₁₆ | Interrupt control register 2 |

Fig. 2 SFR (Special Function Register) memory map

**M37450S1SP/FP, M37450S2SP/FP
M37450S4SP/FP**

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ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|------------------|--|--|---------------------------|------|
| V _{CC} | Supply voltage | With respect to V _{SS} Output transistors are at "OFF" state. | -0.3~7 | V |
| V _I | Input voltage RESET, X _{IN} | | -0.3~7 | V |
| V _I | Input voltage D ₀ ~D ₇ , P ₃₀ ~P ₃₇ , P ₄₀ ~P ₄₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇ , ADV _{REF} , DAV _{REF} , V _{REF} , AV _{CC} | | -0.3~V _{CC} +0.3 | V |
| V _I | Input voltage CNV _{SS} | | -0.3~13 | V |
| V _O | Output voltage A ₀ ~A ₁₅ , D ₀ ~D ₇ , P ₃₀ ~P ₃₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇ , X _{OUT} , φ, RD, WR, R/W, RESET _{OUT} , SYNC | | -0.3~V _{CC} +0.3 | V |
| P _d | Power dissipation | T _a = 25°C | 1000 (Note 1) | mW |
| T _{opr} | Operating temperature | | -10~70 | °C |
| T _{stg} | Storage temperature | | -40~125 | °C |

Note 1 : 500mW for QFP type.

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±10%, T_a=-10~70°C unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|-----------------------|---|--------------------|-------|---------------------|------|
| | | Min. | Norm. | Max. | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V _{SS} | Supply voltage | | 0 | | V |
| V _{IH} | "H" Input voltage RESET, X _{IN} , CNV _{SS} (Note 2) | 0.8V _{CC} | | V _{CC} | V |
| V _{IH} | "H" Input voltage D ₀ ~D ₇ , P ₃₀ ~P ₃₇ , P ₄₀ ~P ₄₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇ (except Note 2) | 2.0 | | V _{CC} | V |
| V _{IL} | "L" Input voltage CNV _{SS} (Note 2) | 0 | | 0.2V _{CC} | V |
| V _{IL} | "L" Input voltage D ₀ ~D ₇ , P ₃₀ ~P ₃₇ , P ₄₀ ~P ₄₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇ (except Note 2) | 0 | | 0.8 | V |
| V _{IL} | "L" Input voltage RESET | 0 | | 0.12V _{CC} | V |
| V _{IL} | "L" Input voltage X _{IN} | 0 | | 0.16V _{CC} | V |
| I _{OL(peak)} | "L" peak output current A ₀ ~A ₁₅ , D ₀ ~D ₇ , P ₃₀ ~P ₃₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇ | | | 10 | mA |
| I _{OL(avg)} | "L" average output current A ₀ ~A ₁₅ , D ₀ ~D ₇ , P ₃₀ ~P ₃₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇ (Note 3) | | | 5 | mA |
| I _{OH(peak)} | "H" peak output current A ₀ ~A ₁₅ , D ₀ ~D ₇ , P ₃₀ ~P ₃₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇ | | | -10 | mA |
| I _{OH(avg)} | "H" average output current A ₀ ~A ₁₅ , D ₀ ~D ₇ , P ₃₀ ~P ₃₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇ (Note 3) | | | -5 | mA |
| f(X _{IN}) | Clock oscillating frequency | 1 | | 10 | MHZ |

Note 2 : Ports operate as INT₁~INT₃(P₆₀~P₆₇), EV₁~EV₃(P₃₀~P₃₇), RxD(P₃₄) and S_{CLK}(P₃₆)

3 : The average output current I_{OH(avg)} and I_{OL(avg)} are the average value during a 100ms.

4 : The total of "L" output current I_{OL(peak)} of port P₃, P₅, P₆, R/W SYNC, RESET_{OUT}, RD, WR and φ is less than 40mA.

The total of "H" output current I_{OH(peak)} of port P₃, P₅, P₆, R/W SYNC, RESET_{OUT}, RD, WR and φ is less than 40mA.

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ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = -10 \sim 70^\circ C$, $f(X_{IN}) = 10MHz$, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|-------------------|--|--|--------------|------|------|---------|
| | | | Min. | Typ. | Max. | |
| V_{OH} | "H" output voltage RD, WR, R/W, SYNC, RESET _{OUT} , ϕ | $I_{OH} = -2mA$ | $V_{CC} - 1$ | | | V |
| V_{OH} | "H" output voltage $A_0 \sim A_{15}$, $D_0 \sim D_7$, $P_{30} \sim P_{37}$, $P_{50} \sim P_{57}$, $P_{60} \sim P_{67}$ | $I_{OH} = -5mA$ | $V_{CC} - 1$ | | | V |
| V_{OL} | "L" output voltage $A_0 \sim A_{15}$, $D_0 \sim D_7$, $P_{30} \sim P_{37}$, $P_{50} \sim P_{57}$, $P_{60} \sim P_{67}$, RD, WR, R/W, SYNC, RESET _{OUT} , ϕ | $I_{OL} = 2mA$ | | | 0.45 | V |
| V_{OL} | "L" output voltage $A_0 \sim A_{15}$, $D_0 \sim D_7$, $P_{30} \sim P_{37}$, $P_{50} \sim P_{57}$, $P_{60} \sim P_{67}$ | $I_{OL} = 5mA$ | | | 1 | V |
| $V_{T+} - V_{T-}$ | Hysteresis INT ₁ ~INT ₃ (P ₆₀ ~P ₆₂), EV ₁ ~EV ₃ (P ₃₀ ~P ₃₂), RxD(P ₃₄), SCLK(P ₃₆) | Function input level | 0.3 | | 1 | V |
| $V_{T+} - V_{T-}$ | Hysteresis RESET | | | | 0.7 | V |
| $V_{T+} - V_{T-}$ | Hysteresis X _{IN} | | 0.1 | | 0.5 | V |
| I_{IL} | "L" input current $D_0 \sim D_7$, $P_{30} \sim P_{37}$, $P_{40} \sim P_{47}$, $P_{50} \sim P_{57}$, $P_{60} \sim P_{67}$, RESET, X _{IN} | $V_i = V_{SS}$ | -5 | | 5 | μA |
| I_{IH} | "H" input current $D_0 \sim D_7$, $P_{30} \sim P_{37}$, $P_{40} \sim P_{47}$, $P_{50} \sim P_{57}$, $P_{60} \sim P_{67}$, RESET, X _{IN} | $V_i = V_{CC}$ | -5 | | 5 | μA |
| V_{RAM} | RAM retention voltage | At stop mode | 2 | | | V |
| I_{CC} | Supply current | At system operation $f(X_{IN}) = 10MHz$ | | 6 | 10 | mA |
| | | At stop mode (Note 5) | | 1 | 10 | μA |

Note 5 : The terminals RD, WR, R/W, SYNC, RESET_{OUT}, ϕ , D-A₁, and D-A₂ are all open. The other ports, which are in the input mode, are connected to V_{SS}. A-D converter is in the A-D completion state. The current through ADV_{REF} and DAV_{REF} is not included(Fig.6).

A-D CONVERTER CHARACTERISTICS

($V_{CC} = AV_{CC} = 5V$, $V_{SS} = AV_{SS} = 0V$, $T_a = 25^\circ C$, $f(X_{IN}) = 10MHz$, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---------------|-----------------------------------|--|-----------|-----------|-----------|-------------|
| | | | Min. | Typ. | Max. | |
| — | Resolution | | | | 8 | Bits |
| — | Absolute accuracy | $V_{CC} = AV_{CC} = ADV_{REF} = 5.12V$ | | ± 1.5 | ± 3 | LSB |
| t_{CONV} | Conversion time | | | | 49 | $t_c(\phi)$ |
| V_{IA} | Analog input voltage | | AV_{SS} | | AV_{CC} | V |
| V_{ADVREF} | Reference input voltage | | 2 | | V_{CC} | V |
| R_{LADDER} | Ladder resistance value | $ADV_{REF} = 5V$ | 2 | 7.5 | 10 | k Ω |
| $I_{IADVREF}$ | Reference input current | $ADV_{REF} = 5V$ | 0.5 | 0.7 | 2.5 | mA |
| V_{AVCC} | Analog power supply input voltage | | | V_{CC} | | V |
| V_{AVSS} | Analog power supply input voltage | | | 0 | | V |

D-A CONVERTER CHARACTERISTICS ($V_{CC} = 5V$, $V_{SS} = AV_{SS} = 0V$, $T_a = 25^\circ C$, unless otherwise noted)

| Symbol | Parameter | Test condition | Limits | | | Unit |
|--------------|-----------------------------------|------------------------------|--------|------|----------|------------|
| | | | Min. | Typ. | Max. | |
| — | Resolution | | | | 8 | Bits |
| — | Absolute accuracy | $V_{CC} = DAV_{REF} = 5.12V$ | | | 1.0 | % |
| t_{SU} | Setup time | | | | 3 | μs |
| R_O | Output resistance | | 1 | 2 | 4 | k Ω |
| V_{AVSS} | Analog power supply input voltage | | | 0 | | V |
| V_{DAVREF} | Reference input voltage | | 4 | | V_{CC} | V |
| I_{DAVREF} | Reference power input current | | 0 | 2.5 | 5 | mA |

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TIMING REQUIREMENTS

Port/Single-chip mode ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_A=-10\sim 70^\circ C$, unless otherwise noted)

| Symbol | Parameter | Test condition | Limits | | | Unit |
|--------------------|--------------------------------------|----------------|--------|------|------|------|
| | | | Min. | Typ. | Max. | |
| $t_{SU}(P3D-\phi)$ | Port P3 input setup time | Fig. 3 | 200 | | | ns |
| $t_{SU}(P4D-\phi)$ | Port P4 input setup time | | 200 | | | ns |
| $t_{SU}(P5D-\phi)$ | Port P5 input setup time | | 200 | | | ns |
| $t_{SU}(P6D-\phi)$ | Port P6 input setup time | | 200 | | | ns |
| $t_h(\phi-P3D)$ | Port P3 input hold time | | 40 | | | ns |
| $t_h(\phi-P4D)$ | Port P4 input hold time | | 40 | | | ns |
| $t_h(\phi-P5D)$ | Port P5 input hold time | | 40 | | | ns |
| $t_h(\phi-P6D)$ | Port P6 input hold time | | 40 | | | ns |
| $t_c(X_{IN})$ | External clock input cycle time | | 100 | | 1000 | ns |
| $t_w(X_{INL})$ | External clock input "L" pulse width | | 30 | | | ns |
| $t_w(X_{INH})$ | External clock input "H" pulse width | | 30 | | | ns |
| $t_r(X_{IN})$ | External clock rising edge time | | | | 20 | ns |
| $t_f(X_{IN})$ | External clock falling edge time | | | | 20 | ns |

Master CPU bus interface timing (\bar{R} and \bar{W} separation type mode)

($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_A=-10\sim 70^\circ C$, unless otherwise noted)

| Symbol | Parameter | Test condition | Limits | | | Unit |
|----------------|------------------------------------|----------------|--------|------|------|------|
| | | | Min. | Typ. | Max. | |
| $t_{SU}(CS-R)$ | CS setup time | Fig. 3 | 0 | | | ns |
| $t_{SU}(CS-W)$ | CS setup time | | 0 | | | ns |
| $t_h(R-CS)$ | CS hold time | | 0 | | | ns |
| $t_h(W-CS)$ | CS hold time | | 0 | | | ns |
| $t_{SU}(A-R)$ | A_0 setup time | | 40 | | | ns |
| $t_{SU}(A-W)$ | A_0 setup time | | 40 | | | ns |
| $t_h(R-A)$ | A_0 hold time | | 10 | | | ns |
| $t_h(W-A)$ | A_0 hold time | | 10 | | | ns |
| $t_w(R)$ | Read pulse width | | 160 | | | ns |
| $t_w(W)$ | Write pulse width | | 160 | | | ns |
| $t_{SU}(D-W)$ | Data input setup time before write | | 100 | | | ns |
| $t_h(W-D)$ | Data input hold time after write | | 10 | | | ns |

Master CPU bus interface timing (R/W type mode)

($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_A=-10\sim 70^\circ C$, unless otherwise noted)

| Symbol | Parameter | Test condition | Limits | | | Unit |
|----------------|------------------------------------|----------------|--------|------|------|------|
| | | | Min. | Typ. | Max. | |
| $t_{SU}(CS-E)$ | CS setup time | Fig. 4 | 0 | | | ns |
| $t_h(E-CS)$ | CS hold time | | 0 | | | ns |
| $t_{SU}(A-E)$ | A_0 setup time | | 40 | | | ns |
| $t_h(E-A)$ | A_0 hold time | | 10 | | | ns |
| $t_{SU}(RW-E)$ | R/W setup time | | 40 | | | ns |
| $t_h(E-RW)$ | R/W hold time | | 10 | | | ns |
| $t_w(EL)$ | Enable clock "L" pulse width | | 160 | | | ns |
| $t_w(EH)$ | Enable clock "H" pulse width | | 160 | | | ns |
| $t_r(E)$ | Enable clock rising edge time | | | | 25 | ns |
| $t_f(E)$ | Enable clock falling edge time | | | | 25 | ns |
| $t_{SU}(D-E)$ | Data input setup time before write | | 100 | | | ns |
| $t_h(E-D)$ | Data input hold time after write | | 10 | | | ns |

**M37450S1SP/FP, M37450S2SP/FP
M37450S4SP/FP**

MITSUBISHI(MICMPTR/MIPRC) 61E D

8-BIT CMOS MICROCOMPUTER

Local bus/Memory expansion mode, Microprocessor mode

($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=-10 \sim 70^\circ C$, unless otherwise noted)

| Symbol | Parameter | Test condition | Limits | | | Unit |
|------------------|-----------------------|----------------|--------|------|------|------|
| | | | Min. | Typ. | Max. | |
| $t_{SU}(D-\phi)$ | Data input setup time | Fig. 5 | 100 | | | ns |
| $t_{H}(\phi-D)$ | Data input hold time | | 0 | | | ns |
| $t_{SU}(D-RD)$ | Data input setup time | | 100 | | | ns |
| $t_{H}(RD-D)$ | Data input hold time | | 0 | | | ns |

**M37450S1SP/FP, M37450S2SP/FP
M37450S4SP/FP**

MITSUBISHI(MICMPTR/MIPRC) BLE D

8-BIT CMOS MICROCOMPUTER

SWITCHING CHARACTERISTICS

Port/Single-chip mode ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10\sim 70^\circ C$, unless otherwise noted)

| Symbol | Parameter | Test condition | Limits | | | Unit |
|-----------------|--------------------------------------|----------------|--------|------|------|------|
| | | | Min. | Typ. | Max. | |
| $t_d(\phi-P3O)$ | Port P3 data output delay time | Fig. 3 | | | 200 | ns |
| $t_d(\phi-P5O)$ | Port P5 data output delay time | | | | 200 | ns |
| $t_d(\phi-P6O)$ | Port P6 data output delay time | | | | 200 | ns |
| $t_c(\phi)$ | Cycle time | | 400 | | 4000 | ns |
| $t_w(\phi H)$ | ϕ clock pulse width ("H" level) | | 190 | | | ns |
| $t_w(\phi L)$ | ϕ clock pulse width ("L" level) | | 170 | | | ns |
| $t_r(\phi)$ | ϕ clock rising edge time | | | | 20 | ns |
| $t_f(\phi)$ | ϕ clock falling edge time | | | | 20 | ns |

Master CPU bus interface (R and W separation type mode)

($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10\sim 70^\circ C$, unless otherwise noted)

| Symbol | Parameter | Test condition | Limits | | | Unit |
|-----------------|--|----------------|--------|------|------|------|
| | | | Min. | Typ. | Max. | |
| $t_a(R-D)$ | Data output enable time after read | Fig. 4 | | | 120 | ns |
| $t_v(R-D)$ | Data output disable time after read | | 10 | | 85 | ns |
| $t_{PLH}(R-PR)$ | P_{RDY} output transmission time after read | | | | 150 | ns |
| $t_{PLH}(W-PR)$ | P_{RDY} output transmission time after write | | | | 150 | ns |

Master CPU bus interface (R/W type mode) ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10\sim 70^\circ C$, unless otherwise noted)

| Symbol | Parameter | Test condition | Limits | | | Unit |
|-----------------|--|----------------|--------|------|------|------|
| | | | Min. | Typ. | Max. | |
| $t_a(E-D)$ | Data output enable time after read | Fig. 4 | | | 120 | ns |
| $t_v(E-D)$ | Data output disable time after read | | 10 | | 85 | ns |
| $t_{PLH}(E-PR)$ | P_{RDY} output transmission time after E clock | | | | 150 | ns |

Local bus/Memory expansion mode, microprocessor mode

($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10\sim 70^\circ C$, unless otherwise noted)

| Symbol | Parameter | Test condition | Limits | | | Unit |
|------------------|---|----------------|--------|------|------|------|
| | | | Min. | Typ. | Max. | |
| $t_d(\phi-A)$ | address delay time after ϕ | Fig. 5 | | | 120 | ns |
| $t_v(\phi-A)$ | address effective time after ϕ | | 10 | | | ns |
| $t_v(RD-A)$ | address effective time after RD | | 10 | | | ns |
| $t_v(WR-A)$ | address effective time after WR | | 10 | | | ns |
| $t_d(\phi-D)$ | data output delay time after ϕ | | | | 140 | ns |
| $t_d(WR-D)$ | data output delay time after WR | | | | 140 | ns |
| $t_v(\phi-D)$ | data output effective time after ϕ | | 20 | | | ns |
| $t_v(WR-D)$ | data output effective time after WR | | 20 | | | ns |
| $t_d(\phi-RW)$ | R/W delay time after ϕ | | | | 120 | ns |
| $t_d(\phi-SYNC)$ | SYNC delay time after ϕ | | | | 120 | ns |
| $t_w(RD)$ | RD pulse width | | 170 | | | ns |
| $t_w(WR)$ | WR pulse width | | 170 | | | ns |

**M37450S1SP/FP, M37450S2SP/FP
M37450S4SP/FP**

MITSUBISHI (MICMPTR/MIPRC) 61E D

8-BIT CMOS MICROCOMPUTER

TEST CONDITION

Input voltage level : V_{IH} 2.4V

V_{IL} 0.45V

Output test level : V_{OH} 2.0V

V_{OL} 0.8V

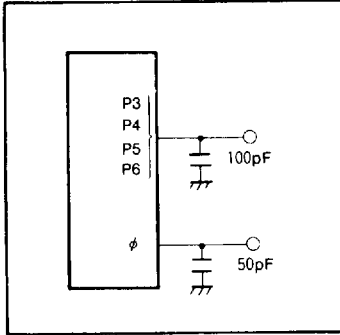


Fig. 3 Test circuit in single-chip mode

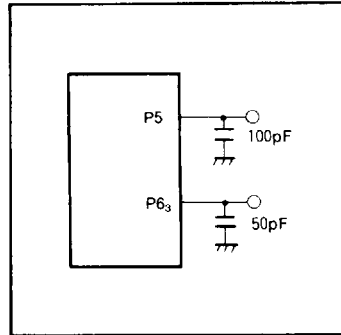


Fig. 4 Master CPU bus interface test circuit

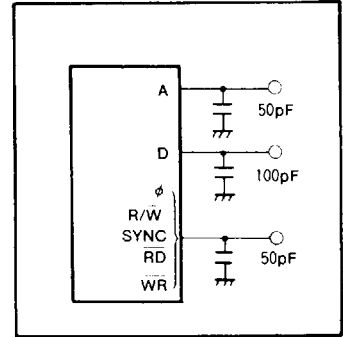


Fig. 5 Local bus test circuit

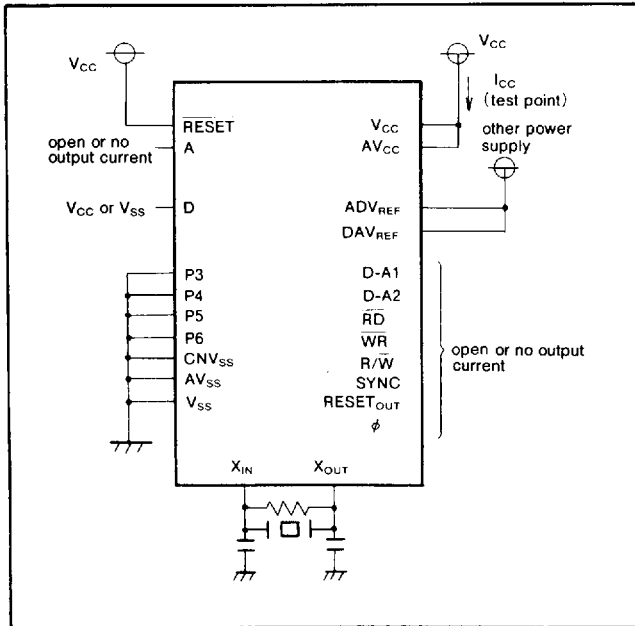
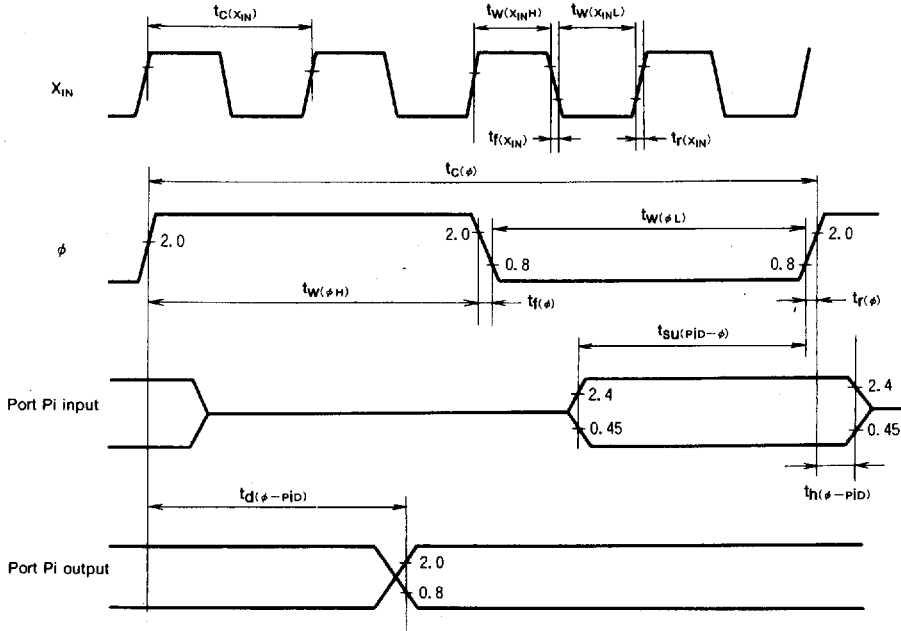


Fig. 6 I_{CC} (at stop mode) test condition

TIMING DIAGRAM

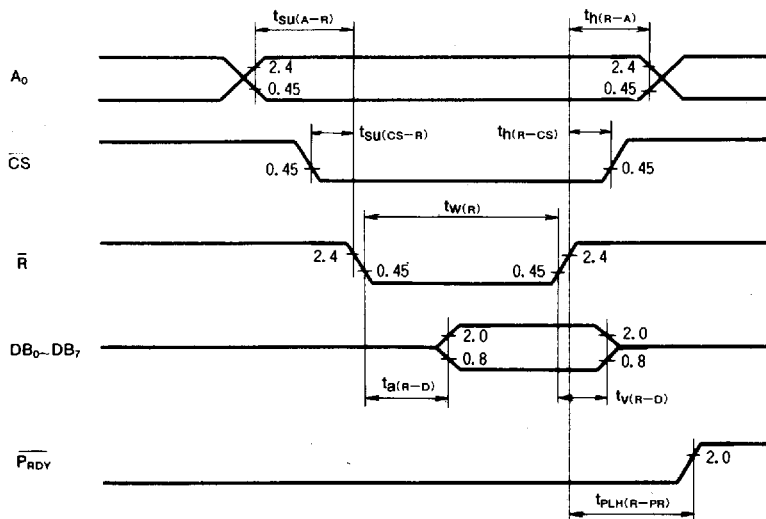
Port/single-chip mode timing diagram



Note : $V_{IH}=0.8V_{CC}$, $V_{IL}=0.16V_{CC}$ of X_{IN}

Master CPU bus interface/ R and W separation type timing diagram

Read

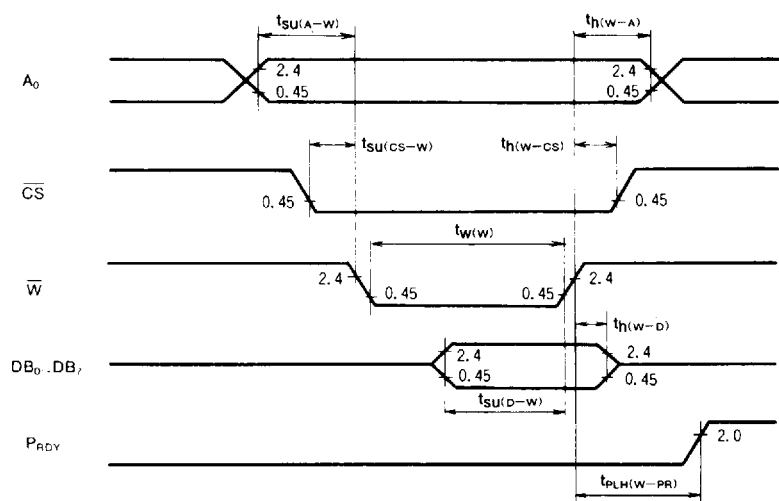


**M37450S1SP/FP, M37450S2SP/FP
M37450S4SP/FP**

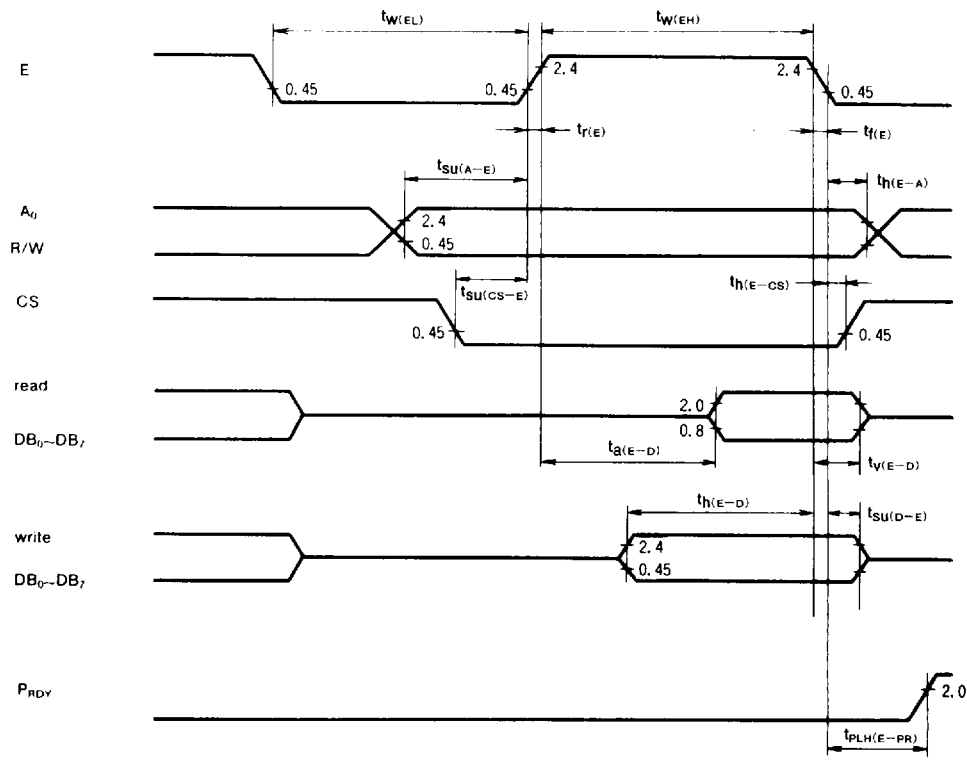
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Write



Master CPU interface/ R/W type timing diagram



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Local bus timing diagram

