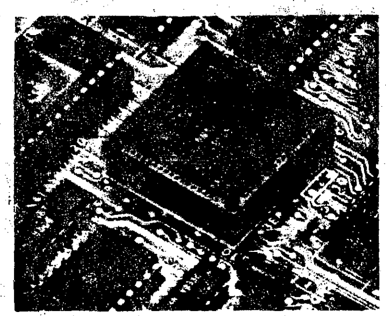
5000 PFM
Data Controller Chip Set

5050 PFM
Data Sequencer

5060 PFM
Four-Channel Memory Controller

5070 PFM MFM
VCO/Encode/Decode Chip



OMTI's advanced VLSI controller chip set is a third generation CMOS design that provides the design engineer with all of the necessary components for a high-performance and cost-effective controller design.

This advanced chip set makes possible such disk controller features as consecutive sector transfers, ECC error detection and correction, 2.0 megabyte host data transfer rates, and intelligent buffer management capable of being implemented in a minimum part count controller design.

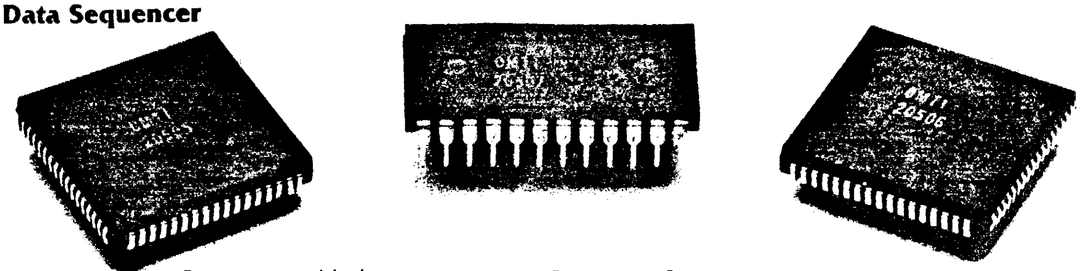
The PFM 5050 Data Sequencer is designed to be used with a commercially available, low-cost microprocessor or microcomputer to manage the flow of block-level information between serial device interfaces and a memory controller.

The OMTI PFM 5060 Four-Channel Memory Controller is intended to be used to manage the flow of block-level information between buffer memory and host and/or byte-oriented peripheral interfaces.

The PFM 5070 VCO/Encode/Decode chip is designed to be used with disk drives requiring MFM encoded data. This device is a fifth generation data separator design that requires only passive components to implement.

OMTI

5050 PFM Data Sequencer



The OMTI PFM 5050 Data Sequencer chip is a fully programmable 15 megabit CMOS/VLSI device designed to be used with the PFM 5060 Four-Channel Memory Controller, a byte-oriented Microprocessor, RAM buffer and appropriate drivers and receivers in high-performance, low-cost data controller designs.

The PFM 5050 data sequencer is designed to provide the high-speed, bit-serial data management, format control, error detection and serialization/deserialization functions normally associated with data controllers. The PFM 5050 data sequencer is designed to be used directly with NRZ interfaces such as SMD, LMD, ESDI, etc. or with the PFM 5070 VCO/Encode/Decode chip when used with MFM interfaces such as SA1000, Q2000, ST506, ST412, etc.

Controller design flexibility is provided by making the normally non-programmable format parameters such as gap lengths, gap characters, Header fields, ECC error detection/correction polynomials and data field lengths to be length and value programmable. These parameters may be loaded once, and are used as constants during the execution of the high level command set.

The command set consists of a simple and versatile set of high level commands such as read data, write data, etc. These commands use 32 individually addressable 8-bit registers for storage of the data transfer parameters necessary for command execution. During multiple block operations, registers that control incrementing parameters, such as block number, are automatically incremented.

The microprocessor is relieved of the responsibility of processing real time events such as "timeouts" by providing a register that is decremented from a programmed value by time related events, such as index pulses. This register defaults to the original value upon error-free block processing.

Features:

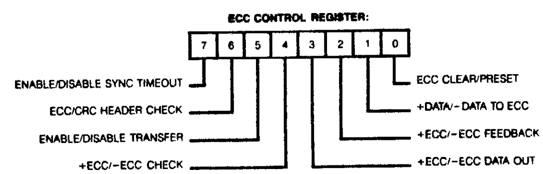
68 PIN LEADLESS PLASTIC PACKAGE
15 MEGAHERTZ BIT RATE
NRZ SERIAL DISK INTERFACE
EIGHT BIT PARALLEL OUTPUT
REAL TIME PROCESSOR INTERVENTION NOT REQUIRED
HIGH LEVEL INSTRUCTION SET
64 BIT PROGRAMMABLE (ECC) POLYNOMIAL
CRC OR ECC HEADER ERROR DETECTION POLYNOMIALS
PROGRAMMABLE HEADER SIZES TO 256 BYTES/HEADER
USER DEFINABLE HEADER FLAG BYTES
PROGRAMMABLE CAP SIZES AND FILL CHARACTERS
PROGRAMMABLE SECTOR SIZES TO 65536 BYTES/SECTOR
PROGRAMMABLE TRACK SIZES TO 256 SECTORS/TRACK
MULTIPLE SECTOR READ/WRITE CAPABILITY
ESDI SECTOR AND ADDRESS MARK OPERATION

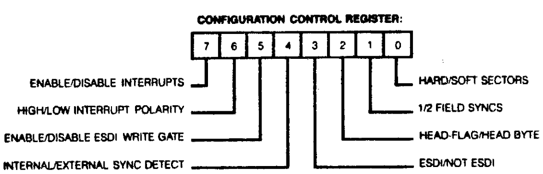
Commands:

READ DATA—Read data block(s) to buffer.
READ VERIFY—Read data block(s) and compare with buffer.
READ WITHOUT DATA TRANSFER—Read data block(s) and check for errors.
READ ECC SYNDROME—Read data block plus ECC syndrome to buffer.
READ ID—Read header(s) to buffer.
READ LONG—Read data block plus ECC to buffer.
WRITE DATA—Write data block(s) from buffer.
WRITE FORMAT—Write header and data block(s) from buffer.
WRITE LONG—Write data block(s) plus ECC from buffer.

Data Transfer Parameter Register:

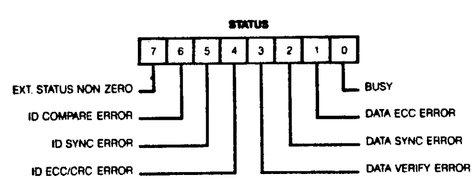
CYLINDER HIGH	CYLINDER LOW
HEAD ADDRESS	BLOCK NUMBER
NUMBER OF BLOCKS TO TRANSFER	TIMEOUT COUNT
ECC CONTROL	CONFIGURATION CONTROL

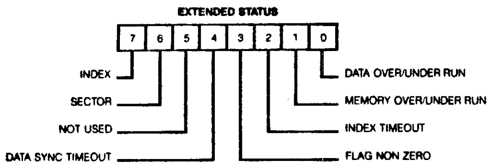


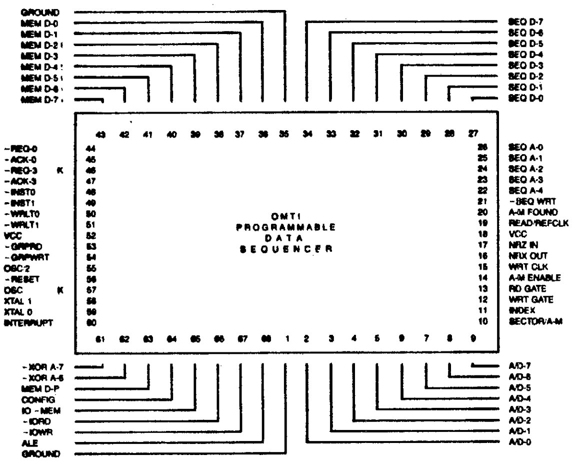


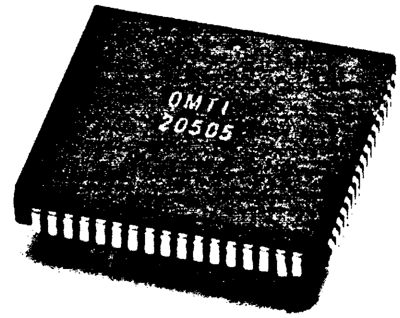
Format Parameter Registers:

PRE INDEX GAP	POST INDEX GAP
HEADER PREAMBLE	HEADER SYNC FIELD
HEADER ID MARK	HEADER FIELD LENGTH
HEADER ECC/CRC POLYNOMIAL	HEADER POSTAMBLE
DATA PREAMBLE	DATA SYNC FIELD
DATA ID MARK	DATA FIELD LENGTH
DATA ECC POLYNOMIAL	DATA POSTAMBLE
INTERBLOCK GAP	DATA POSTAMBLE









These registers can be used to augment the internal microprocessor registers without increasing valuable real estate or parts cost.

5060 PFM Four-Channel Memory Controller

The OMTI PFM 5060 Four-Channel Memory Controller chip is a programmable 5 megabyte CMOS/VLSI device intended for use with the PFM 5050 Data Sequencer in high throughput, multi-function, multi-tasking, block-oriented data controller designs.

The PFM 5060 memory controller is designed to provide buffer management and data transfer control functions required in high-performance data controllers. The PFM 5060 memory controller contains four independent DMA channels with contention resolution based on preassigned channel priority. Design freedom in the amount and speed of the buffer memory is provided with sixteen bit direct memory addressing (65K) and programmable memory cycle times.

All of the DMA channels are general purpose channels designed for a direct connection to the PFM 5050 data sequencer or the microprocessor bus. All channels can be independently enabled or disabled and memory addresses can be independently set and automatically incremented. 16-bit byte counts can be independently set and are automatically decremented as well as being optionally reinitialized at channel end. Channel end interrupts can be independently enabled or disabled.

The data transfer protocol used is a standard DMA memory Request/Acknowledge protocol with independent polarity control over the Request/Acknowledge signals. Two of the DMA channels are, however, programmable as specific purpose channels. One channel can be programmed to use the SCSI Request/Acknowledge data transfer handshake protocol. The second programmable channel can be programmed as a byte oriented peripheral channel using QIC-02 Transfer/Acknowledge data transfer protocol. The ability to program the polarity of the SCSI and QIC 02 handshake signals also allows the ability to adapt these channels to any byte oriented host or peripheral interface.

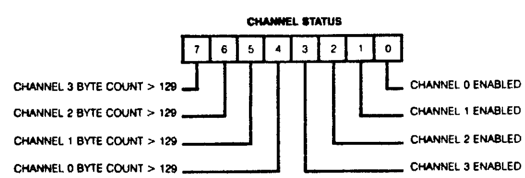
The PFM 5060 memory controller also provides the ability to address up to eight external registers.

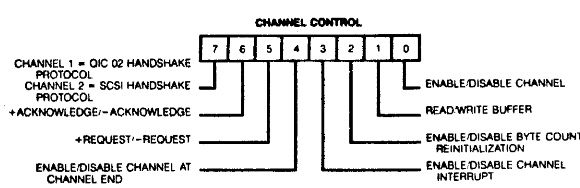
Features:

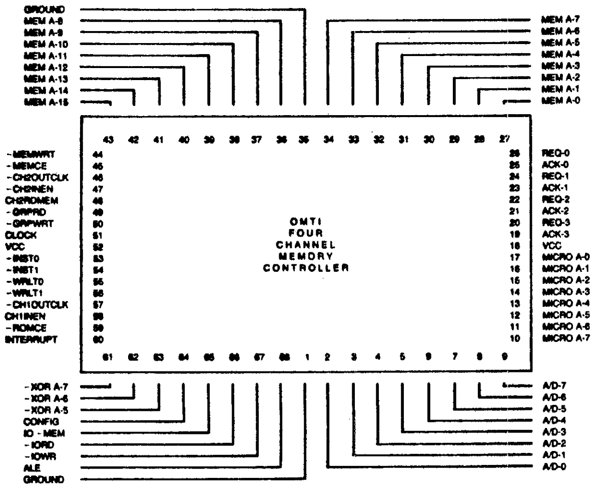
68 PIN LEADLESS PLASTIC PACKAGE
FOUR ASYNCHRONOUS DMA CHANNELS
INDEPENDENT CONTROL OF EACH CHANNEL
5 MEGABYTE DEVICE BANDWIDTH
CONTENTION RESOLUTION ON CHANNEL PRIORITY BASIS
16 BIT MEMORY ADDRESSING
AUTOMATIC ADDRESS INCREMENT
AUTOMATIC BYTE COUNT DECREMENT
AUTOMATIC REINITIALIZATION OF BYTE COUNT
REQUEST/ACKNOWLEDGE DMA HANDSHAKE PROTOCOL
INDEPENDENT POLARITY CONTROL OF REQUEST/ACKNOWLEDGE SIGNALS
PROGRAMMABLE MEMORY CYCLE TIME
INDEPENDENT CONTROL OF CHANNEL END INTERRUPT
CONFIGURABLE 'SASI' REQUEST/ACKNOWLEDGE HANDSHAKE PROTOCOL
CONFIGURABLE 'QIC 02' TRANSFER/ACKNOWLEDGE HANDSHAKE PROTOCOL
CONTROL OF UP TO 8 EXTERNAL REGISTERS

Device Commands:

COMMAND	REGISTER SIZE
READ CHANNEL STATUS REGISTER	8 bits
LOAD MEMORY CYCLE TIME/ INTERRUPT POLARITY REGISTER	8 bits
LOAD EXTERNAL REGISTER CONTROL	8 bits







The PFM 5070 VCO/Encode/Decode chip is capable of operation at data rates to 10 megabits per second by proper selection of the external frequency and loop gain components. Costly delay lines are eliminated by selecting write pre-compensation values with an internally temperature compensated external RC network.

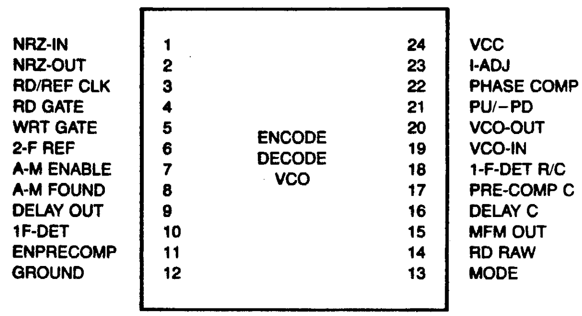
Features:

- 24 PIN PLASTIC PACKAGE
- INTERNAL VCO AND PHASE LOCKED LOOP
- DATA RATE CONTROL TO 10 MEGABITS PER SECOND
- NO EXTERNAL LOGIC REQUIRED
- MFM TO NRZ AND NRZ TO MFM CONVERSION
- ADDRESS MARK DETECTION AND GENERATION
- WRITE PRECOMPENSATION
- INTERNAL EARLY, ON TIME AND LATE TIMING

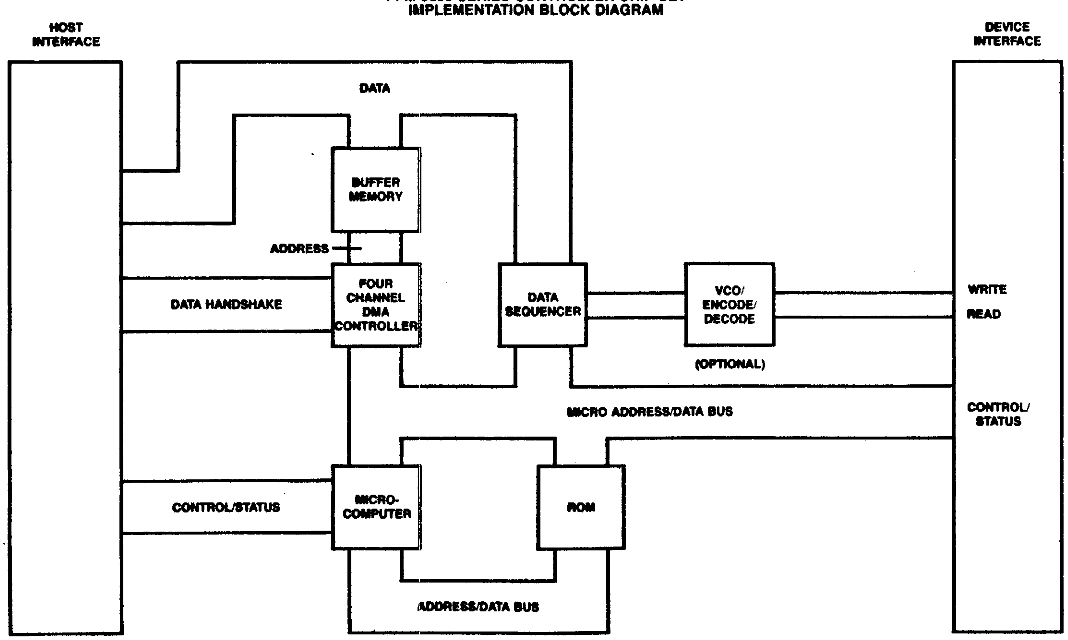
5070 PFM MFM VCO/Encode/Decode Chip

The PFM 5070 VCO/Encode/Decode chip provides all of the necessary functions needed to convert disk drives with MFM serial data interfaces (i.e., ST506/412, SA1000) to NRZ data and clock.

The PFM 5070 VCO/Encode/Decode chip is a completely self contained MFM/NRZ and NRZ/MFM data translator with an internal voltage controlled oscillator, phase locked loop, encode/decode logic, dropped clock address mark generation/detection and write precompensation circuitry.



PFM 5000 SERIES CONTROLLER CHIP SET
IMPLEMENTATION BLOCK DIAGRAM



OMTI

A Data Controller Company

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HIGH PERFORMANCE PROGRAMABLE DISK SEQUENCER

* UP TO 20 MBIT / SEC TRANSFER RATE
* MAX 2^8 * 2^8 BYTES PER SECTOR LENGTHS
* HIGH LEVEL COMMANDS (NO REAL TIME INTERVENTION)
* PROGRAMABLE ECC TO 64 BIT POLYNOMIAL & ID CRC OR ECC
* TOTAL FIELD COUNT AND VALUE PROGRAMABILITY
* NRZ INPUT / OUTPUT
* AUTOMATIC SECTOR INCREMENT FOR MULTI-SECTOR OPERATIONS
* ESDI SECTOR / ADDRESS MARK MODE
* 68 PIN PLASTIC LEADLESS CHIP CARRIER

```
GROUND      ---------------------------+
MEM D-0     ------------------------+  !  +------------------------- SEQ D-7
MEM D-1     ---------------------+  !  !  !  +---------------------- SEQ D-6
MEM D-2     ------------------+  !  !  !  !  !  +------------------- SEQ D-5
MEM D-3     ---------------+  !  !  !  !  !  !  !  +---------------- SEQ D-4
MEM D-4     ------------+  !  !  !  !  !  !  !  !  !  +------------- SEQ D-3
MEM D-5     ---------+  !  !  !  !  !  !  !  !  !  !  !  +---------- SEQ D-2
MEM D-6     ------+  !  !  !  !  !  !  !  !  !  !  !  !  !  +------- SEQ D-1
MEM D-7     ---+  !  !  !  !  !  !  !  !  !  !  !  !  !  !  !  +---- SEQ D-0
            +------------------------------------------------------+
            !  43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27  !
            !                                                      !
-REQ-0      ! 44                                                26 ! SEQ A-0
            !                                                      !
-ACK-0      ! 45                                                25 ! SEQ A-1
            !                                                      !
-REQ-3      ! 46                                                24 ! SEQ A-2
            !                                                      !
-ACK-3      ! 47                                                23 ! SEQ A-3
            !                                                      !
-INST0      ! 48                                                22 ! SEQ A-4
            !                                                      !
-INST1      ! 49                                                21 ! -SEQ WRT
            !                                                      !
-WRLT0      ! 50                                                20 ! A-M FOUND
            !                      O M T I                         !
-WRLT1      ! 51                                                19 ! READ/REFCL
            !               P R O G R A M M A B L E                !
VCC         ! 52                                                18 ! VCC
            !                      D I S K                         !
-GRPRD      ! 53                                                17 ! NRZ IN
            !                 S E Q U E N C E R                    !
-GRPWRT     ! 54                                                16 ! NRZ OUT
            !                                                      !
OSC/2       ! 55                                                15 ! WRT CLK
            !                                                      !
-RESET      ! 56                                                14 ! A-M ENABLE
            !                                                      !
OSC         ! 57                                                13 ! RD GATE
            !                                                      !
XTAL 1      ! 58                                                12 ! WRT GATE
            !                                                      !
XTAL 0      ! 59                                                11 ! INDEX
            !                                                      !
INTERRUPT   ! 60                                                10 ! SECTOR/A-M
            !                                                      !
            !  61 62 63 64 65 66 67 68 1  2  3  4  5  6  7  8  9   !
            +------------------------------------------------------+
-XOR A-7    ---+  !  !  !  !  !  !  !  !  !  !  !  !  !  !  !  +---- A/D-7
-XOR A-6    ------+  !  !  !  !  !  !  !  !  !  !  !  !  !  +------- A/D-6
MEM D-P     ---------+  !  !  !  !  !  !  !  !  !  !  !  +---------- A/D-5
CONFIG      ------------+  !  !  !  !  !  !  !  !  !  +------------- A/D-4
IO/-MEM     ---------------+  !  !  !  !  !  !  !  +---------------- A/D-3
-IORD       ------------------+  !  !  !  !  !  +------------------- A/D-2
-IOWR       ---------------------+  !  !  !  +---------------------- A/D-1
ALE         ------------------------+  !  +------------------------- A/D-0
GROUND      ---------------------------+
```

SYMBOL	TYPE	NAME AND FUNCTION
A/D 0-7	I/O	MULTIPLEXED ADDRESS / DATA BUS: 3-STATE ADDRESS / DATA LINES THAT INTERFACE WITH THE CPU LOWER 8 BIT ADDRESS / DATA BUS. THE ADDRESSES ARE LATCHED INTO THE ADDRESS REGISTER ON THE FALLING EDGE OF ALE. THE 8 BIT DATA IS EITHER WRITTEN INTO OR READ FROM THE DISK SEQUENCER REGISTERS DEPENDING ON -IOWR OR -IORD INPUT CONTROL LINES, IF THE ADDRESS IN WITHIN THE RANGE OF THE INTERNAL CHIP SELECT.
ALE	I	ADDRESS LATCH ENABLE: THIS INPUT STROBE IS FOR STORING ADDRESS 0-7 INTO THE ADDRESS REGISTER ON THE FALLING EDGE OF ALE FOR INTERNAL CHIP AND REGISTER SELECT.
-IOWR	I	I/O WRITE: THIS ACTIVE LOW INPUT STROBE IS USED BY THE CPU TO LOAD INFORMATION IN THE DISK SEQU-ENCER WITH THE PROPER ADDRESS FOR CHIP AND REGISTER SELECTION.
-IORD	I	I/O READ: THIS ACTIVE LOW INPUT STROBE IS USED BY THE CPU TO READ STATUS INFORMATION FROM THE DISK SEQUENCER WITH THE PROPER ADDRESS FOR CHIP AND REGISTER SELECTION.
IO/-MEM	I	IO/-MEMORY: THIS INTERNALLY PULLED-UP INPUT IS USED FOR AN ACTIVE HIGH CHIP ENABLE. IN AN 8085 SYSTEM THIS LINE IS CONNECTED TO THE SAME MICRO LINE OR IN ANY OTHER MICRO MAY BE LEFT OPEN.
XOR 7-6	I	EXCLUSIVE OR ADDRESS 7 - 6: THESE INTERNALLY PULLED-UP INPUTS ARE USED FOR THE INTERNAL CHIP SELECT. THEY CONTROL THE POLARITY OF THE CORROSPONDING ADDRESS LINE. IF ANOTHER GROUP CHIP SELECT IF REQU-IRED , GROUND THE APPROPRIATE LINE.

SYMBOL	TYPE	NAME AND FUNCTION
CONFIG	I	CONFIG: THIS INTERNALY PULLED-UP LINE IS USED TO SELECT THE MICRO STROBE INPUTS. WHEN THIS INPUT IS GROUNDED THE CHIP IS CONFIGURED FOR AN 8085 TYPE MICRO. WHEN LEFT OPEN THE CHIP IS CONFIGURED AS A Z-8 TYPE MICRO.
XTAL 0/1	I/O	CRYSTAL 0 / 1: THE XTAL LINES ARE TO BE CONNECTED TO AN EXTERNAL CRYSTAL WITH A FREQUENCY OF 4 * THE DISK 1-F DATA RATE. A CLOCK INPUT MAY BE CONNECTED TO THE XTAL 0 INPUT WITH THE XTAL 1 LINE LEFT OPEN IF AN EXTERNAL CLOCK SOURCE IS AVAILABLE.
OSC	O	OSCILLATOR: THIS OUTPUT IS A TTL OUTPUT OF THE XTAL FREQUENCY
OSC/2	O	OSCILLATOR / 2: THIS OUTPUT IS A FREE RUNNING CLOCK AT 1/2 THE OSCILLATOR OUTPUT.
-RESET	I	-RESET: THIS INPUT WHEN ACTIVE RESETS READ GATE OR WRITE GATE AND PUTS THE CHIP IN A NOT BUSY MODE.
INTERRUPT	O	INTERRUPT: THIS OUTPUT, IF ENABLED IS ACTIVE WHEN THE SEQUENCER IS COMPLETED WITH A COMMAND. THIS OUTPUT IS RESET THEN THE MICRO READS STATUS.
-INST0-1	O	IN STATUS 0 / 1: THESE OUTPUT STROBES ARE INTERALLY DECODE I/O READ STROBES INTENDED TO BE USED BY THE MICRO TO READ DEVICE STATUS THROUGH AN EXTERNAL BUFFER TO THE MICRO DATA BUS.

SYMBOL	TYPE	NAME AND FUNCTION
-WRLTO-1	O	WRITE LATCH 0 / 1: THESE OUTPUT STROBES ARE INTERALLY DECODE I/O WRITE STROBES INTENDED TO BE USED BY THE MICRO TO WRITE DEVICE CONTROL THROUGH AN EXT-RNAL LATCH FROM THE MICRO DATA BUS.
-GRPRD/WR/O		GROUP READ / WRITE STROBE: THESE INTERNALLY DECODED GROUP-SELECT ARE INTENDED TO BE INTERFACED WITH AN EXTERNAL PERIPHERAL CHIP WITH THE REQUIREMENT OF BLOCK MEMORY I/O FROM THE MEMORY CONTROLLER.
-REQ 0	O	DMA SEQUENCER REQUEST: THE DMA REQUEST 0 LINE IS ACTIVATED WHEN THE SEQUENCER NEEDS TO TRANSFER DATA TO / FROM THE MEMORY CONTROLLER.
-ACK 0	I	DMA MEMORY ACKNOWLEDGE 0: THIS DMA ACKNOWLEDGE LINE IS TO ENABLE DATA FROM THE SEQUENCER IN A WRITE MEMORY FUNCTION OR SAVE DATA IN THE SEQUENCER IN A READ MEMORY FUNCTION.
-REQ-3	O	REQUEST 3: THIS OUTPUT IS USED FOR THE MICRO TO REQUEST DATA TO OR FROM THE MEMORY CONTROLLER SYSTEM.
-ACK-3	I	ACKNOWLEDGE 3: THIS INPUT IS A RESPONSE FROM REQ-3 FROM THE MEMORY CONTROLLER SYSTEM.
MEMD 0-7	I/O	MEMORY DATA 0-7: THIS 8 BIT BIDIRECTIONAL DATA BUS IS THE PATH THE DATA GETS TO AND FROM THE MEMORY.
MEMD P	O	MEMORY DATA PARITY: THIS OUTPUT IS A FALL THROUGH ODD PARITY OF THE MEMORY DATA BUS.

SYMBOL	TYPE	NAME AND FUNCTION
NRZ OUT	O	NRZ DATA OUT: THIS SERIAL DATA OUTPUT LINE, WHEN WRITE GATE IS TRUE, OUTPUTS ALL SERIAL DATA AND THE ECC FIELD AS PROGRAMED IN THE SEQUENCER.
NRZ IN	I	NRZ DATA IN: THIS SERIAL DATA INPUT LINE, IS THE OUTPUT FROM THE DATA SEPARATOR OR ESDI TYPE DISK DRIVE.
WRT CLK	O	WRITE CLOCK: THIS OUTPUT IS THE 1-F NRZ WRITE AT THE RD/REFERANCE CLOCK RATE.
RD/REFCLK	I	READ / REFERENCE CLOCK: THIS INPUT, THE NRZ WRITE CLOCK OR THE READ NRZ CLOCK IF READ GATE IS TRUE. A CLOCK MUST ALWAYS BE A CLOCK PRESENT AT THIS INPUT.
A-M EN	O	ADDRESS MARK ENABLE: THIS OUTPUT, IF ESDI MODE IS SELECTED IS TRUE AT STATE 1 STROBE TIME. THIS FUNCTION IS FOR WRITING THE ADDRESS MARK TO THE DISK DRIVE. IF ESDI MODE IS NOT SELECTED, THIS OUTPUT IS TRUE FOR STATE STROBE 2 & 8 AND CAN BE USED FOR EXTERNAL ENCODING OF THE DROP CLOCK BYTE.
RD GATE	O	READ GATE: THIS OUTPUT IS TRUE WHEN THE DISK SEQUENCER IS IN READ MODE. IT IS THE RESPONSIBILITY OF DATA SEPARATOR CHIP TO PROVIDE AM FOUND IF THE SEQUENCER IS IN EXTERNAL SYNC MODE.

SYMBOL	TYPE	NAME AND FUNCTION
WRT GATE	O	WRITE GATE: THIS OUTPUT IS TRUE WHEN THE DISK SEQUENCER IS WRITE DATA TO THE DISK.
INDEX	I	INDEX: THIS INPUT IS FROM THE DISK AND IS PULSED EVERY REVOLUTION. THE SEQUENCER USES THE LEADING EDGE OF THIS SIGNAL ONLY FOR A FORMAT COMMAND, AND FOR A PROGRAMABLE "WATCH DOG TIMMER".
SEC/A-M	I	SEC / A-M FOUND / SYNC: THIS INPUT CAN BE CONFIGURED AS EITHER THE SECTOR LINE IN A HARD-SECTORED DRIVE OR THE ADDRESS-MARK-FOUND INPUT FROM A ESDI TYPE DRIVE.
A-M FND	I	ADDRESS MARK FOUND: THIS INPUT IS TO BE USED WITH THE ENCODE / DECODE VCO CHIP FOR MFM BYTE SYNC.
SEQ D0-7	I/O	SEQUENCER DATA 0-7: THIS 8 BIT BI-DIRECTIONAL DATA BUS IS USED BY THE SEQUENCER AS A REGISTER FILE OR RAM FOR STORING THE SEQUENCE FIELD COUNT AND VALUE.
SEQ A0-4	O	SEQUENCER ADDRESS 0-4: THESE FIVE ADDRESS LINES ARE USED TO SELECT THE SPECIFIC REGISTER CORRESPONDING TO THE STATE THE SEQUENCER IS IN.
-SEQWRT	O	SEQUENCER WRITE: THIS OUTPUT IS TRUE WHEN THE MICRO IS DOWN LOADING THE SEQUENCER REGISTER FILE.

COMMAND / CONTROL REGISTER ASSIGNMENT

ADDRESS REGISTER AND CONTROL

7	6	5	4	3	2	1	0	-IOWR	-IORD	REGISTER FUNCTION
S	S	1	0	0	0	0	0	0	1	COMMAND
S	S	1	0	0	0	0	1	0	1	SEQUENCER LOOP COUNT
S	S	1	0	0	0	1	0	0	1	TIME-OUT
S	S	1	0	0	0	1	1	0	1	SECTOR SUB-BLOCK COUNT
S	S	1	0	0	1	0	0	0	1	CYLINDER HIGH (HDR BYTE 0)
S	S	1	0	0	1	0	1	0	1	CYLINDER LOW (HDR BYTE 1)
S	S	1	0	0	1	1	0	0	1	HEAD / FLAG (HDR BYTE 2)
S	S	1	0	0	1	1	1	0	1	SECTOR (HDR BYTE 3)
S	S	1	0	1	0	0	0	0	1	MICRO TO MEMORY
S	S	1	0	1	0	0	1	0	1	SEQ START / RE-START STATE
S	S	1	0	1	0	1	0	0	1	SEQUENCER LOOP END STATE
S	S	1	0	1	0	1	1	0	1	BIT RING START
S	S	1	0	1	1	0	0	0	1	ECC CONTROL
S	S	1	0	1	1	0	1	0	1	ENCODE / DECODE CONTROL
S	S	1	0	1	1	1	0	0	1	SEQ COUNT REG @ RESTART
S	S	1	0	1	1	1	1	0	1	SEQ VALUE REG @ RESTART

S S = INTERNAL CHIP SELECT

STATUS / HEADER REGISTER ASSIGNMENT

ADDRESS REGISTER AND CONTROL

7	6	5	4	3	2	1	0	-IOWR	-IORD	REGISTER FUNCTION
S	S	1	0	0	0	0	0	1	0	STATUS
S	S	1	0	0	0	0	1	1	0	EXTENDED STATUS
S	S	1	0	0	0	1	0	1	0	RETRY COUNT / STATE ADDRESS
S	S	1	0	0	0	1	1	1	0	FLAG BYTE (HDR BYTE 4)
S	S	1	0	0	1	0	0	1	0	CYLINDER HIGH (HDR BYTE 0)
S	S	1	0	0	1	0	1	1	0	CYLINDER LOW (HDR BYTE 1)
S	S	1	0	0	1	1	0	1	0	HEAD / FLAG (HDR BYTE 2)
S	S	1	0	0	1	1	1	1	0	SECTOR (HDR BYTE 3)
S	S	1	0	1	0	0	0	1	0	MEMORY TO MICRO
S	S	1	0	1	0	0	1	1	0	SEQUENCER LOOP COUNT
S	S	1	0	1	0	1	0	1	0	NOT USED
S	S	1	0	1	0	1	1	1	0	NOT USED
S	S	1	0	1	1	0	0	1	0	NOT USED
S	S	1	0	1	1	0	1	1	0	NOT USED
S	S	1	0	1	1	1	0	1	0	SEQ COUNT REG @ RESTART
S	S	1	0	1	1	1	1	1	0	SEQ VALUE REG @ RESTART

S S = INTERNAL CHIP SELECT

LOAD ECC POLYMONIAL CONFIGURATION REGISTER ASSIGNMENT

WRITE EXTERNAL I/O STROBES

ADDRESS REGISTER AND CONTROL

7	6	5	4	3	2	1	0	-IOWR	-IORD	REGISTER FUNCTION
S	S	1	1	0	0	0	0	0	1	POLYNOMIAL 0 - 7
S	S	1	1	0	0	0	1	0	1	POLYNOMIAL 8 - 15
S	S	1	1	0	0	1	0	0	1	POLYNOMIAL 16 - 23
S	S	1	1	0	0	1	1	0	1	POLYNOMIAL 24 - 31
S	S	1	1	0	1	0	0	0	1	POLYNOMIAL 32 - 39
S	S	1	1	0	1	0	1	0	1	POLYNOMIAL 40 - 47
S	S	1	1	0	1	1	0	0	1	POLYNOMIAL 48 - 55
S	S	1	1	0	1	1	1	0	1	POLYNOMIAL 56 - 63
S	S	1	1	1	0	0	0	0	1	EXTERNAL OUT STROBE 0
S	S	1	1	1	0	0	1	0	1	EXTERNAL OUT STROBE 1
S	S	1	1	1	0	1	0	0	1	NOT USED
S	S	1	1	1	0	1	1	0	1	NOT USED
S	S	1	1	1	1	0	0	0	1	EXTERNAL GROUP STROBE
S	S	1	1	1	1	0	1	0	1	EXTERNAL GROUP STROBE
S	S	1	1	1	1	1	0	0	1	EXTERNAL GROUP STROBE
S	S	1	1	1	1	1	1	0	1	EXTERNAL GROUP STROBE

S S= INTERNAL CHIP SELECT

READ ECC SYNDROME REGISTER ASSIGNMENT

READ EXTERNAL I/O STROBES

ADDRESS REGISTER AND CONTROL

7	6	5	4	3	2	1	0	-IOWR	-IORD	REGISTER FUNCTION
S	S	1	1	0	0	0	0	1	0	NOT USED
S	S	1	1	0	0	0	1	1	0	NOT USED
S	S	1	1	0	0	1	0	1	0	NOT USED
S	S	1	1	0	0	1	1	1	0	NOT USED
S	S	1	1	0	1	0	0	1	0	NOT USED
S	S	1	1	0	1	0	1	1	0	NOT USED
S	S	1	1	0	1	1	0	1	0	NOT USED
S	S	1	1	0	1	1	1	1	0	NOT USED
S	S	1	1	1	0	0	0	1	0	EXTERNAL IN STROBE 0
S	S	1	1	1	0	0	1	1	0	EXTERNAL IN STROBE 1
S	S	1	1	1	0	1	0	1	0	NOT USED
S	S	1	1	1	0	1	1	1	0	MICRO-DMA MEM TO GROUP
S	S	1	1	1	1	0	0	1	0	EXTERNAL GROUP STROBE
S	S	1	1	1	1	0	1	1	0	EXTERNAL GROUP STROBE
S	S	1	1	1	1	1	0	1	0	EXTERNAL GROUP STROBE
S	S	1	1	1	1	1	1	1	0	EXTERNAL GROUP STROBE

S S= INTERNAL CHIP SELECT

LOAD SEQUENCER FIELD COUNT REGISTER ASSIGNMENT

RESTART REGISTER AND CONTROL

7	6	5	4	3	2	1	0	-IOWR	-IORD	REGISTER FUNCTION
X	X	X	X	0	0	0	0	0	1	ESDI SECTOR GAP COUNT
X	X	X	X	0	0	0	1	0	1	POST-INDEX-GAP COUNT
X	X	X	X	0	0	1	0	0	1	ID PREAMBLE COUNT
X	X	X	X	0	0	1	1	0	1	ID SYNC BYTE COUNT
X	X	X	X	0	1	0	0	0	1	ID MARKER BYTE COUNT
X	X	X	X	0	1	0	1	0	1	ID DATA FIELD COUNT
X	X	X	X	0	1	1	0	0	1	ID ECC BYTE COUNT
X	X	X	X	0	1	1	1	0	1	ID POSTAMBLE COUNT
X	X	X	X	1	0	0	0	0	1	DATA PREAMBLE COUNT
X	X	X	X	1	0	0	1	0	1	DATA SYNC BYTE COUNT
X	X	X	X	1	0	1	0	0	1	DATA MARKER BYTE COUNT
X	X	X	X	1	0	1	1	0	1	DATA FIELD COUNT
X	X	X	X	1	1	0	0	0	1	DATA ECC BYTE COUNT
X	X	X	X	1	1	0	1	0	1	DATA POSTAMBLE COUNT
X	X	X	X	1	1	1	0	0	1	INTER-SECTOR-GAP COUNT
X	X	X	X	1	1	1	1	0	1	PRE-INDEX-GAP COUNT

READ SEQUENCER FIELD COUNT REGISTER ASSIGNMENT

RESTART REGISTER AND CONTROL

7	6	5	4	3	2	1	0	-IOWR	-IORD	REGISTER FUNCTION
X	X	X	X	0	0	0	0	1	0	ESDI SECTOR GAP COUNT
X	X	X	X	0	0	0	1	1	0	POST-INDEX-GAP COUNT
X	X	X	X	0	0	1	0	1	0	ID PREAMBLE COUNT
X	X	X	X	0	0	1	1	1	0	ID SYNC BYTE COUNT
X	X	X	X	0	1	0	0	1	0	ID MARKER BYTE COUNT
X	X	X	X	0	1	0	1	1	0	ID DATA FIELD COUNT
X	X	X	X	0	1	1	0	1	0	ID ECC BYTE COUNT
X	X	X	X	0	1	1	1	1	0	ID POSTAMBLE COUNT
X	X	X	X	1	0	0	0	1	0	DATA PREAMBLE COUNT
X	X	X	X	1	0	0	1	1	0	DATA SYNC BYTE COUNT
X	X	X	X	1	0	1	0	1	0	DATA MARKER BYTE COUNT
X	X	X	X	1	0	1	1	1	0	DATA FIELD COUNT
X	X	X	X	1	1	0	0	1	0	DATA ECC BYTE COUNT
X	X	X	X	1	1	0	1	1	0	DATA POSTAMBLE COUNT
X	X	X	X	1	1	1	0	1	0	INTER-SECTOR-GAP COUNT
X	X	X	X	1	1	1	1	1	0	PRE-INDEX-GAP COUNT

LOAD SEQUENCER FIELD VALUE REGISTER ASSIGNMENT

RESTART REGISTER AND CONTROL

7	6	5	4	3	2	1	0	-IOWR	-IORD	REGISTER FUNCTION
X	X	X	X	0	0	0	0	0	1	ESDI SECTOR GAP VALUE
X	X	X	X	0	0	0	1	0	1	POST-INDEX-GAP VALUE
X	X	X	X	0	0	1	0	0	1	ID PREAMBLE VALUE
X	X	X	X	0	0	1	1	0	1	ID SYNC BYTE VALUE
X	X	X	X	0	1	0	0	0	1	ID MARKER BYTE VALUE
X	X	X	X	0	1	0	1	0	1	NOT USED
X	X	X	X	0	1	1	0	0	1	NOT USED
X	X	X	X	0	1	1	1	0	1	ID POSTAMBLE VALUE
X	X	X	X	1	0	0	0	0	1	DATA PREAMBLE VALUE
X	X	X	X	1	0	0	1	0	1	DATA SYNC BYTE VALUE
X	X	X	X	1	0	1	0	0	1	DATA MARKER BYTE VALUE
X	X	X	X	1	0	1	1	0	1	FORMAT DATA FIELD VALUE
X	X	X	X	1	1	0	0	0	1	NOT USED
X	X	X	X	1	1	0	1	0	1	DATA POSTAMBLE VALUE
X	X	X	X	1	1	1	0	0	1	INTER-SECTOR-GAP VALUE
X	X	X	X	1	1	1	1	0	1	PRE-INDEX-GAP VALUE

READ SEQUENCER FIELD VALUE REGISTER ASSIGNMENT

RESTART REGISTER AND CONTROL

7 6 5 4 3 2 1 0	-IOWR	-IORD	REGISTER FUNCTION
X X X X 0 0 0 0	1	0	ESDI SECTOR GAP VALUE
X X X X 0 0 0 1	1	0	POST-INDEX-GAP VALUE
X X X X 0 0 1 0	1	0	ID PREAMBLE VALUE
X X X X 0 0 1 1	1	0	ID SYNC BYTE VALUE
X X X X 0 1 0 0	1	0	ID MARKER BYTE VALUE
X X X X 0 1 0 1	1	0	NOT USED
X X X X 0 1 1 0	1	0	NOT USED
X X X X 0 1 1 1	1	0	ID POSTAMBLE VALUE
X X X X 1 0 0 0	1	0	DATA PREAMBLE VALUE
X X X X 1 0 0 1	1	0	DATA SYNC BYTE VALUE
X X X X 1 0 1 0	1	0	DATA MARKER BYTE VALUE
X X X X 1 0 1 1	1	0	FORMAT DATA FIELD VALUE
X X X X 1 1 0 0	1	0	NOT USED
X X X X 1 1 0 1	1	0	DATA POSTAMBLE VALUE
X X X X 1 1 1 0	1	0	INTER-SECTOR-GAP VALUE
X X X X 1 1 1 1	1	0	PRE-INDEX-GAP VALUE

COMMAND REGISTER

WRITE DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
! ! ! ! ! ! ! +--------   1 = READ
! ! ! ! ! ! !
! ! ! ! ! ! +----------   1 = WRITE
! ! ! ! ! !
! ! ! ! ! +------------   0 = NORMAL
! ! ! ! ! +------------   1 = FORMAT / ID DATA
! ! ! ! !
! ! ! ! +--------------   0 = NORMAL
! ! ! ! +--------------   1 = LONG ( ECC TO / FROM BUFFER )
! ! ! !
! ! ! +----------------   1 = SYNDROME TO BUFFER
! ! !
! ! +------------------   0 = ABORT ON FLAG NON-ZERO
! ! +------------------   1 = IGNORE FLAG CONDITION
! !
! +--------------------   1 = VERIFY ( BUFFER TO DISK DATA )
!
+----------------------   1 = NO DATA TRANSFER
```

SEQUENCER COUNT

WRITE DATA BUS

```
7 6 5 4 3 2 1 0

! ! ! ! ! ! ! !
+-+-+-+-+-+-+-+-------   NUMBER OF SECTORS ( N = N )
```

INDEX TIME-OUT

WRITE DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
! ! ! ! +-+-+-+-------   # OF REVS BEFORE TIMEOUT ( 2 - F )
```

SUB-BLOCK COUNT

WRITE DATA BUS

```
                         TOTAL BYTES PER SECTOR =
7 6 5 4 3 2 1 0          DATA FIELD COUNT * SUB-BLOCK COUNT
! ! ! ! ! ! ! !
+-+-+-+-+-+-+-+-------   # OF SUB-BLOCKES PER SECTOR
```

CYLINDER HIGH

WRITE DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
+-+-+-+-+-+-+-+-------     00 - FF
```

CYLINDER LOW

WRITE DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
+-+-+-+-+-+-+-+-------     00 - FF
```

HEAD

WRITE DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
+-+-+-+-+-+-+-+-------     00 - FF
```

SECTOR

WRITE DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
+-+-+-+-+-+-+-+-------     00 - FF
```

MICRO TO MEMORY

WRITE DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
+-+-+-+-+-+-+-+-------     00 - FF
```

SEQUENCER START / RE-START

WRITE DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
! ! ! ! +-+-+-+-------    START STATE X0 - XF
! ! ! !
+-+-+-+---------------    RE-START STATE 0X - FX
```

SEQUENCER LOOP STATE

WRITE DATA BUS

```
7 6 5 4 3 2 1 0
X X X X ! ! ! !
X X X X +-+-+-+-------    LOOP STATE X0 - XF
```

BIT RING START COUNT

WRITE DATA BUS

```
7 6 5 4 3 2 1 0
X X X X ! ! ! !
X X X X +-+-+-+-------    START BIT 0 - F
```

ECC CONTROL

WRITE DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
! ! ! ! ! ! ! +-------    0 = ECC CLEAR ON INIT
! ! ! ! ! ! ! +-------    1 = ECC PRESET ON INIT
! ! ! ! ! ! !
! ! ! ! ! ! +---------    0 = DATA TO ECC
! ! ! ! ! ! +---------    1 = -DATA TO ECC
! ! ! ! ! !
! ! ! ! ! +-----------    0 = ECC FEEDBACK
! ! ! ! ! +-----------    1 = -ECC FEEDBACK
! ! ! ! !
! ! ! ! +-----------    0 = ECC DATA OUT
! ! ! ! +-----------    1 = -ECC DATA OUT
! ! ! !
! ! ! +---------------    0 = ECC CHECK
! ! ! +---------------    1 = -ECC CHECK
! ! !
! ! +-----------------    0 = XFER DISABLE
! ! +-----------------    1 = XFER ENABLE
! !
! +-------------------    0 = I-D = CRC
+---------------------    1 = ENABLE DATA FIELD SYNC TIMEOUT
```

CONFIG CONTROL

WRITE DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
! ! ! ! ! ! ! !
! ! ! ! ! ! ! +-------     0 = SOFT SECTORED
! ! ! ! ! ! ! +-------     1 = HARD SECTORED
! ! ! ! ! ! !
! ! ! ! ! ! +---------     0 = 1 FIELD SYNC
! ! ! ! ! ! +---------     1 = 2 FIELD SYNC
! ! ! ! ! !
! ! ! ! ! +-----------     0 = HEAD / FLAG BYTE
! ! ! ! ! +-----------     1 = FLAG BYTE
! ! ! ! !
! ! ! ! +-------------     0 = NOT ESDI CONFIG
! ! ! ! +-------------     1 = ESDI CONFIG
! ! ! !
! ! ! +---------------     0 = INTERNAL SYNC DETECT
! ! ! +---------------     1 = EXTERNAL SYNC DETECT
! ! !
! ! +-----------------     0 = DISABLE WRITE GATE EDGE
! ! +-----------------     1 = ENABLE WRITE GATE EDGE
! !
! +-------------------     0 = INTERRUPT ACTIVE LOW
! +-------------------     1 = INTERRUPT ACTIVE HIGH
!
+---------------------     0 = INTERRUPT DISABLED
+---------------------     1 = INTERRUPT ENABLED
```

MICRO TO MEMORY

WRITE DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
+-+-+-+-+-+-+-+-------     00 - FF
```

EXTERNAL REGISTER 0 STROBE

WRITE DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
+-+-+-+-+-+-+-+-------     00 - FF
```

EXTERNAL REGISTER 1 STROBE

WRITE DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
+-+-+-+-+-+-+-+-------     00 - FF
```

STATUS

READ DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
! ! ! ! ! ! ! +-------     1 = BUSY
! ! ! ! ! ! !
! ! ! ! ! ! +---------     1 = DATA ECC ERROR
! ! ! ! ! !
! ! ! ! ! +-----------     1 = DATA SYNC + MARKER NOT FOUND
! ! ! ! !
! ! ! ! +-------------     1 = DATA VERIFY ERROR
! ! ! !
! ! ! +---------------     1 = ID ECC ERROR
! ! !
! ! +-----------------     1 = ID SYNC + MARKER NOT FOUND
! !
! +-------------------     1 = ID DATA NO COMPARE
!
+---------------------     1 = EXTENDED STATUS NON ZERO
```

EXTENDED STATUS

READ DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
! ! ! ! ! ! ! +-------     1 = DISK DATA OVER / UNDER RUN
! ! ! ! ! ! !
! ! ! ! ! ! +---------     1 = MICRO MEM OVER / UNDER RUN
! ! ! ! ! !
! ! ! ! ! +-----------     1 = INDEX TIMEOUT
! ! ! ! !
! ! ! ! +-------------     1 = FLAG BYTE / BIT NON-ZERO
! ! ! !
! ! ! +---------------     1 = DATA FIELD SYNC TIMEOUT
! ! !
! ! +-----------------     NOT USED
! !
! +-------------------     SECTOR
!
+---------------------     INDEX
```

RETRY COUNT

READ DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
! ! ! ! +-+-+-+-------     X0 - XF = RETRY COUNT
! ! ! !
+-+-+-+---------------     0X - FX = SEQUENCER STATE ADDRESS
```

FLAG BYTE

READ DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
+-+-+-+-+-+-+-+-------     00 - FF = FLAG BYTE (HDR BYTE 4)
```

CYLINDER HIGH

READ DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
+-+-+-+-+-+-+-+-------     00 - FF = CYL HIGH   (HDR BYTE 0)
```

CYLINDER LOW

READ DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
+-+-+-+-+-+-+-+-------     00 - FF = CYL LOW     (HDR BYTE 1)
```

HEAD / FLAG

READ DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
+-+-+-+-+-+-+-+-------     00 - FF = HEAD FLAG   (HDR BYTE 2)
```

SECTOR

READ DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
+-+-+-+-+-+-+-+-------     00 - FF = SECTOR      (HDR BYTE 3)
```

MEMORY TO MICRO

READ DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
+-+-+-+-+-+-+-+-------     00 - FF = MEMORY TO MICRO
```

EXTERNAL STATUS 0

READ DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
+-+-+-+-+-+-+-+-------     00 - FF = EXTERNAL STATUS 0
```

EXTERNAL STATUS 1

READ DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
+-+-+-+-+-+-+-+-------     00 - FF = EXTERNAL STATUS 1
```

FORMAT COMMAND -- STATE SEQUENCE

MODE	STATE	FUNCTION	COUNT	VALUE
	0	NOT USED		
START	1	POST-INDEX-GAP	SEQ-CNT	SEQ-VAL
RESTART	2	ID PREAMBLE	SEQ-CNT	SEQ-VAL
	3	ID SYNC	SEQ-CNT	SEQ-VAL
	4	ID MARK	SEQ-CNT	SEQ-VAL
	5	ID DATA FIELD	SEQ-CNT	MEMORY
	6	ID ECC	SEQ-CNT	ECC GENERATER
	7	ID POSTAMBLE	SEQ-CNT	SEQ-VAL
	8	DATA PREAMBLE	SEQ-CNT	SEQ-VAL
	9	DATA SYNC	SEQ-CNT	SEQ-VAL
	A	DATA MARK	SEQ-CNT	SEQ-VAL
	B	DATA FIELD	CNT*BLK	SEQ-VAL
	C	DATA ECC	SEQ-CNT	ECC GENERATER
	D	DATA POSTAMBLE	SEQ-CNT	SEQ-VAL
LOOP	E	INTER-SECTOR-GAP	SEQ-CNT	SEQ-VAL
HOLD	F	PRE-INDEX-GAP	INDEX	SEQ-VAL
	10	DONE		

READ COMMAND -- STATE SEQUENCE

MODE	STATE	FUNCTION	COUNT	VALUE
	0	NOT USED		
	1	NOT USED		
	2	NOT USED		
SRT/RESRT	3	ID SYNC	SEQ-CNT	SEQ-VAL
	4	ID MARK	SEQ-CNT	SEQ-VAL
	5	ID DATA FIELD	SEQ-CNT	HEADER REGISTER
	6	ID ECC	SEQ-CNT	ECC CHECK
	7	SKIP STATE	1	
	8	SKIP STATE	1	
	9	DATA SYNC	SEQ-CNT	SEQ-VAL
	A	DATA MARK	SEQ-CNT	SEQ-VAL
	B	DATA FIELD	CNT*BLK	DATA TO MEMORY
	C	DATA ECC	SEQ-CNT	ECC CHECK
	D	SKIP STATE	1	
LOOP	E	SKIP STATE	1	
	F	NOT USED		

READ LONG COMMAND -- STATE SEQUENCE

MODE	STATE	FUNCTION	COUNT	VALUE
	0	NOT USED		
	1	NOT USED		
	2	NOT USED		
SRT/RESRT	3	ID SYNC	SEQ-CNT	SEQ-VAL
	4	ID MARK	SEQ-CNT	SEQ-VAL
	5	ID DATA FIELD	SEQ-CNT	HEADER REGISTER
	6	ID ECC	SEQ-CNT	ECC CHECK
	7	SKIP STATE	1	
	8	SKIP STATE	1	
	9	DATA SYNC	SEQ-CNT	SEQ-VAL
	A	DATA MARK	SEQ-CNT	SEQ-VAL
	B	DATA FIELD	CNT*BLK	DATA TO MEMORY
	C	DATA ECC	SEQ-CNT	ECC TO MEMORY
	D	SKIP STATE	1	
LOOP	E	SKIP STATE	1	
	F	NOT USED		

READ SYNDROME COMMAND -- STATE SEQUENCE

MODE	STATE	FUNCTION	COUNT	VALUE
	0	NOT USED		
	1	NOT USED		
	2	NOT USED		
SRT/RESRT	3	ID SYNC	SEQ-CNT	SEQ-VAL
	4	ID MARK	SEQ-CNT	SEQ-VAL
	5	ID DATA FIELD	SEQ-CNT	HEADER REGISTER
	6	ID ECC	SEQ-CNT	ECC CHECK
	7	SKIP STATE	1	
	8	SKIP STATE	1	
	9	DATA SYNC	SEQ-CNT	SEQ-VAL
	A	DATA MARK	SEQ-CNT	SEQ-VAL
	B	DATA FIELD	CNT*BLK	DATA TO MEMORY
	C	DATA ECC	SEQ-CNT	SYND TO MEMORY
	D	SKIP STATE	1	
LOOP	E	SKIP STATE	1	
	F	NOT USED		

WRITE COMMAND -- STATE SEQUENCE

MODE	STATE	FUNCTION	COUNT	VALUE
	0	NOT USED		
	1	NOT USED		
	2	NOT USED		
SRT/RESRT	3	ID SYNC	SEQ-CNT	SEQ-VAL
	4	ID MARK	SEQ-CNT	SEQ-VAL
	5	ID DATA FIELD	SEQ-CNT	HEADER REGISTER
	6	ID ECC	SEQ-CNT	ECC CHECK
	7	ID POSTAMBLE	SEQ-CNT	
	8	DATA PREAMBLE	SEQ-CNT	SEQ-VAL
	9	DATA SYNC	SEQ-CNT	SEQ-VAL
	A	DATA MARK	SEQ-CNT	SEQ-VAL
	B	DATA FIELD	CNT*BLK	DATA FROM MEM
	C	DATA ECC	SEQ-CNT	ECC CHECK
	D	DATA POSTAMBLE	SEQ-CNT	SEQ-VAL
LOOP	E	SKIP STATE	1	
	F	NOT USED		

WRITE LONG COMMAND -- STATE SEQUENCE

MODE	STATE	FUNCTION	COUNT	VALUE
	0	NOT USED		
	1	NOT USED		
	2	NOT USED		
SRT/RESRT	3	ID SYNC	SEQ-CNT	SEQ-VAL
	4	ID MARK	SEQ-CNT	SEQ-VAL
	5	ID DATA FIELD	SEQ-CNT	HEADER REGISTER
	6	ID ECC	SEQ-CNT	ECC CHECK
	7	ID POSTAMBLE	SEQ-CNT	
	8	DATA PREAMBLE	SEQ-CNT	SEQ-VAL
	9	DATA SYNC	SEQ-CNT	SEQ-VAL
	A	DATA MARK	SEQ-CNT	SEQ-VAL
	B	DATA FIELD	CNT*BLK	DATA FORM MEM
	C	DATA ECC	SEQ-CNT	DATA FROM MEM
	D	DATA POSTAMBLE	SEQ-CNT	SEQ-VAL
LOOP	E	SKIP STATE	1	
	F	NOT USED		

READ VERIFY COMMAND -- STATE SEQUENCE

MODE	STATE	FUNCTION	COUNT	VALUE
	0	NOT USED		
	1	NOT USED		
	2	NOT USED		
SRT/RESRT	3	ID SYNC	SEQ-CNT	SEQ-VAL
	4	ID MARK	SEQ-CNT	SEQ-VAL
	5	ID DATA FIELD	SEQ-CNT	HEADER REGISTER
	6	ID ECC	SEQ-CNT	ECC CHECK
	7	SKIP STATE	1	
	8	SKIP STATE	1	
	9	DATA SYNC	SEQ-CNT	SEQ-VAL
	A	DATA MARK	SEQ-CNT	SEQ-VAL
	B	DATA FIELD	CNT*BLK	DATA FROM MEM
	C	DATA ECC	SEQ-CNT	ECC CHECK
	D	SKIP STATE	1	
LOOP	E	SKIP STATE	1	
	F	NOT USED		

READ VERIFY LONG COMMAND -- STATE SEQUENCE

MODE	STATE	FUNCTION	COUNT	VALUE
	0	NOT USED		
	1	NOT USED		
	2	NOT USED		
SRT/RESRT	3	ID SYNC	SEQ-CNT	SEQ-VAL
	4	ID MARK	SEQ-CNT	SEQ-VAL
	5	ID DATA FIELD	SEQ-CNT	HEADER REGISTER
	6	ID ECC	SEQ-CNT	ECC CHECK
	7	SKIP STATE	1	
	8	SKIP STATE	1	
	9	DATA SYNC	SEQ-CNT	SEQ-VAL
	A	DATA MARK	SEQ-CNT	SEQ-VAL
	B	DATA FIELD	CNT*BLK	DATA FORM MEM
	C	DATA ECC	SEQ-CNT	DATA FROM MEM
	D	SKIP STATE	1	
LOOP	E	SKIP STATE	1	
	F	NOT USED		

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PRODUCT SPECIFICATION

for

OMTI PFM 5050 PROGRAMMABLE DATA SEQUENCER

MAY 1984

OMTI PFM 5050 PROGRAMMABLE DATA SEQUENCER
PRODUCT SPECIFICATION
(PART #20505)

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

Page Number

LIST OF TABLES

CHAPTER 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

The OMTI PFM 5050 Data Sequencer is a special-purpose CMOS/VLSI component that manages the flow of block-level information between serial disk device interfaces and a DMA memory controller in advanced Winchester disk controller designs.

The 5050 is designed to be used with the PFM 5060 Four-Channel Memory Controller, a RAM buffer, a byte-oriented microprocessor, and appropriate drivers and receivers. The Data Sequencer can also be used with the PFM 5070 VCO/Encode/Decode chip to provide all the functions needed to interface to disk drives using MFM-encoded data.

The Data Sequencer provides the bit-serial data management, format control, error detection, and serialization/de-serialization functions normally associated with data controllers. The chip is designed to be used directly with NRZ interfaces such as SMD, LMD, ESDI; when used with the PFM 5070 chip, it provides all the control lines required for MFM interfaces such as Shugart Associates 1000, the Quantum Q2000, and the Seagate Technology ST506 and ST412 drives.

1.2 5050 DATA SEQUENCER CAPABILITIES

* High level instruction set
* Total field count and value programmability:

  Programmable sector sizes to 65536 bytes/sector

  Programmable header sizes to 256-bytes/header

  Programmable gap sizes and fill characters

  User-definable header flag bytes

  64-bit programmable (ECC) polynomial and ID CRC or ECC

* ESDI sector/address mark mode
* 15 MHz bit rate--up to 15M bit/sec transfer rate
* NRZ serial disk interface
* Multiple sector transfers capability with automatic sector increment for multi-sector operations
* Programmable number of automatic ID field retries
* 68-pin leadless plastic package

1.3 ARCHITECTURAL OVERVIEW

Figure 1 illustrates a conceptual block diagram of the PFM 5050 Data Sequencer, including the major logic blocks. There are three logic blocks entirely within the 5050; four additional blocks define the four external interfaces. The internal blocks are discussed below; the interfaces are discussed in Section 1.4. (For more information concerning details of the implementation, Figure 2 is provided, which includes pin inputs and outputs as well as logic blocks and internal data flow.)

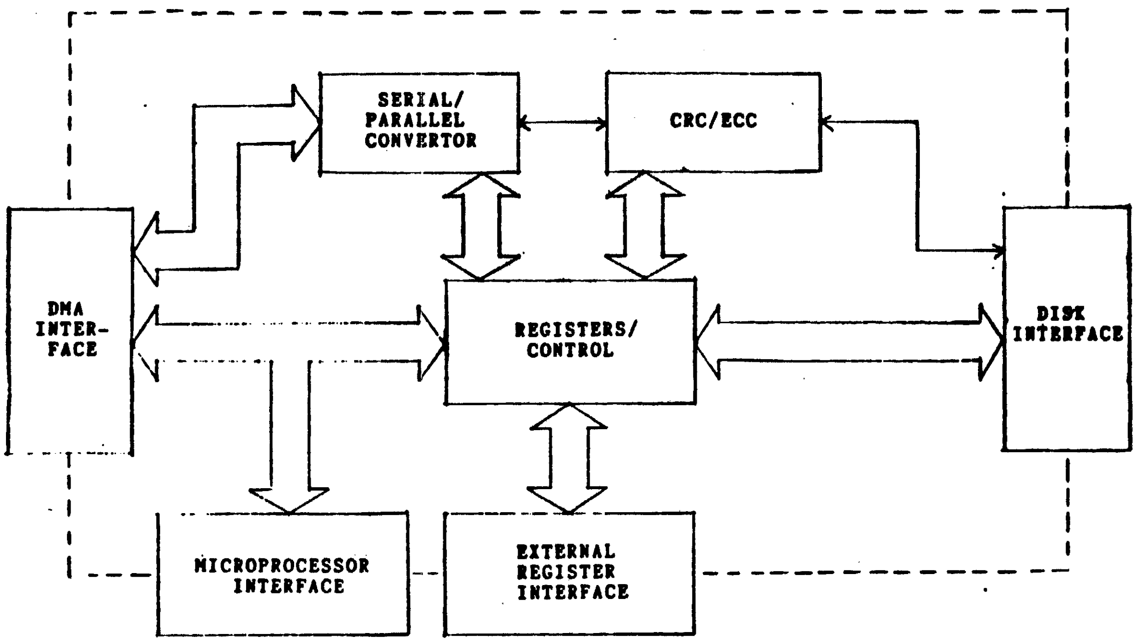


Figure 1. Conceptual Block Diagram

1.3.1 Registers/Control Logic

The Registers/Control block contains 32 8-bit internal control registers and associated control logic. The registers may be individually written to initialize the parameters that control data transfer, and individually read to obtain status information about command execution. Commands are issued to the 5050 by writing to these registers.

1.3.2 ECC/CRC Logic

The ECC/CRC logic generates and checks the ECC or CRC bytes appended to the ID and data fields. Bit 6 of WR12 governs whether the fixed CCITT standard CRC-16 polynomial ($x^{16} + x^{12} + x^5 + 1$) or the programmable ECC polynomial is appended to the ID field. The ECC polynomial is up to 64 bits in length (modulo 8 bits) and is determined at initialization time by values written into WR16-23.

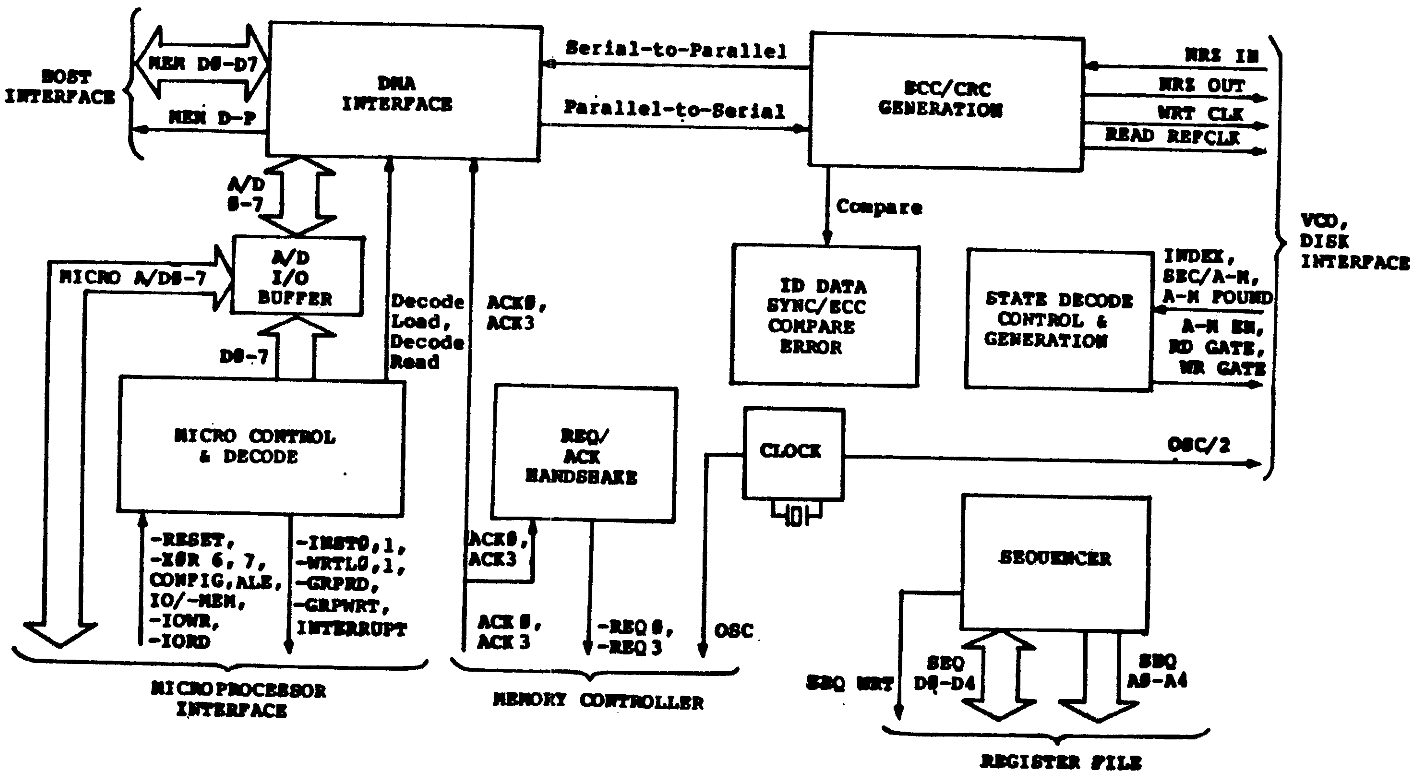


Figure 2. Functional Block Diagram

1.3.3 Serial/Parallel Conversion Logic

Data to and from the disk device must be serial in form, while the host memory bus transfers data in byte-parallel form. The serial/parallel conversion logic is composed of high-speed shift registers which effect the necessary translation between serial and parallel data formats.

1.4 SYSTEM CONFIGURATION

Illustrated below is a typical system configuration, incorporating the Data Sequencer, the 5Ø6Ø Memory Controller, and the 5Ø7Ø VCO/Encode/Decode chip.

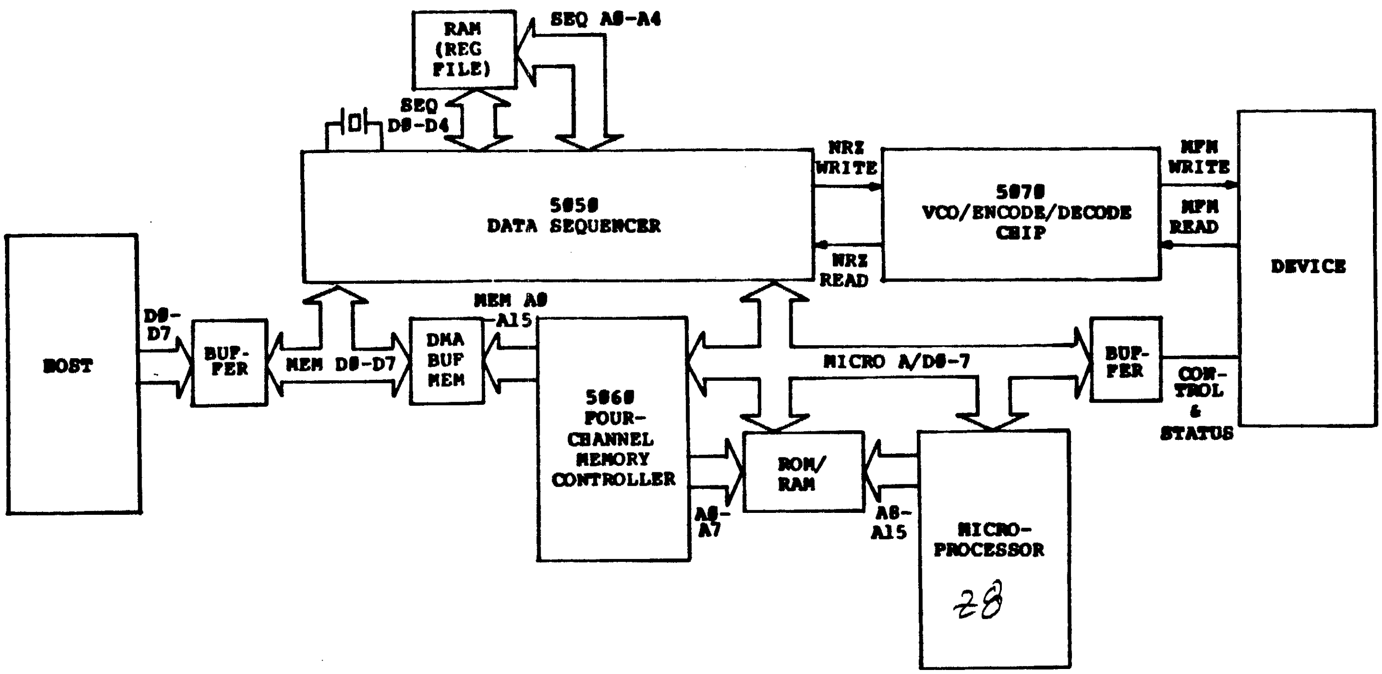


Figure 3. Typical System Configuration

1.4.1 Host Interface

Communication with the host is via an 8-bit bidirectional bus. The host interface block contains the logic to transfer data between the 5Ø5Ø and the DMA buffer memory over this bus. The 5Ø6Ø DMA Memory Controller provides the addresses in the buffer to which this data is to be transferred.

1.4.2 Disk Interface

The disk interface block contains the logic necessary to drive the control and status lines of the disk itself. In addition, the serial data stream to and from the disk runs through this block.

1.4.3 Local Microprocessor Interface

This block contains the logic necessary to allow the local microprocessor to read or write the internal registers. An 8-bit bus connects this block to the register file.

1.4.4 External Register Interface

To provide greater flexibility in disk drive selection, 32 of the 64 read/write registers are not on the 5050 chip itself. These registers are located in an external RAM register file accessed via the external register interface block. (Drive select is thus simply a matter of indexing into the Register file containing the format parameters for the particular disk.)

CHAPTER 2

FUNCTIONAL DESCRIPTION

2.1 INTRODUCTION

The 5050's basic function is to translate serial data from a high-speed Winchester disk storage device into parallel bytes of data that are in turn sent to the 5060 Memory Controller for DMA to host memory. The 5050 can be initialized in many different ways to customize it to the unique hardware requirements of different disk drives. This initialization is performed by a program in the local microprocessor (as described in Appendix A) using the programmable Data Transfer Parameter registers of the 5050.

The 5050 is designed to be initialized by a microprocessor having the proper control lines (for example, a Z8- or 8085/8051-type microprocessor). Depending on the microprocessor used, the timing and pin functions of the 5050 vary slightly. (See Chapter 3, Interfacing, for specific details.)

2.2 REGISTERS

Registers on the PFM 5050 Data Sequencer are of two types: Data Transfer Parameter Registers, which are used to issue commands and return status information, and Format Parameter Registers, which are used to hold parameter-type information necessary for command execution. Both types of registers are individually addressable.

2.2.1 Data Transfer Parameter Registers

The Data Transfer Parameter registers are summarized in Table 1. Their addresses are contained in Table 2. Following the tables is a description of the individual bits in each of the registers.

Table 1. Data Transfer Parameter Registers

Read Register	Functions	Write Register	Functions
RRØ	Status	WRØ	Command Register
RR1	Extended Status	WR1	Sequencer Loop Count
RR2	Retry Count/State Address	WR2	Index Time-Out
RR3	Flag Byte	WR3	Sub-Block Count
RR4	Cylinder High	WR4	Cylinder High
RR5	Cylinder Low	WR5	Cylinder Low
RR6	Head/Flag	WR6	Head Address
RR7	Sector	WR7	Sector
RR8	Memory to Micro	WR8	Micro to Memory
RR9	Sequencer Loop Count	WR9	Sequencer Start/Re-Start
RR1Ø	Not Used	WR1Ø	Sequencer Loop State
RR11	Not Used	WR11	Bit Ring Start Count
RR12	Not Used	WR12	ECC Control
RR13	Not Used	WR13	Configuration Control
RR14	Seq Count Reg @ Seq Start	WR14	Seq Count Reg @ Seq Start
RR15	Seq Value Reg @ Seq Start	WR15	Seq Value Reg @ Seq Start
RR16	Not Used	WR16	Polynomial Ø-7
RR17	Not Used	WR17	Polynomial 8-15
RR18	Not Used	WR18	Polynomial 16-23
RR19	Not Used	WR19	Polynomial 24-31
RR2Ø	Not Used	WR2Ø	Polynomial 32-39
RR21	Not Used	WR21	Polynomial 4Ø-47
RR22	Not Used	WR22	Polynomial 48-55
RR23	Not Used	WR23	Polynomial 56-63
RR24	External Status Ø	WR24	External Register Ø Strobe
RR25	External Status 1	WR25	External Register 1 Strobe
RR26	Not Used	WR26	Not Used
RR27	Micro-DMA Memory to Group	WR27	Not Used
RR28	External Group Strobe	WR28	External Group Strobe
RR29	External Group Strobe	WR29	External Group Strobe
RR3Ø	External Group Strobe	WR3Ø	External Group Strobe
RR31	External Group Strobe	WR31	External Group Strobe

Table 2. Data Transfer Parameter Register Map

AD5	AD4	AD3	AD2	AD1	AD0	Write	Read
1	0	0	0	0	0	WR0	RR0
1	0	0	0	0	1	WR1	RR1
1	0	0	0	1	0	WR2	RR2
1	0	0	0	1	1	WR3	RR3
1	0	0	1	0	0	WR4	RR4
1	0	0	1	0	1	WR5	RR5
1	0	0	1	1	0	WR6	RR6
1	0	0	1	1	1	WR7	RR7
1	0	1	0	0	0	WR8	RR8
1	0	1	0	0	1	WR9	RR9
1	0	1	0	1	0	WR10	NOT USED
1	0	1	0	1	1	WR11	NOT USED
1	0	1	1	0	0	WR12	NOT USED
1	0	1	1	0	1	WR13	NOT USED
1	0	1	1	1	0	WR14	RR14
1	0	1	1	1	1	WR15	RR15
1	1	0	0	0	0	WR16	NOT USED
1	1	0	0	0	1	WR17	NOT USED
1	1	0	0	1	0	WR18	NOT USED
1	1	0	0	1	1	WR19	NOT USED
1	1	0	1	0	0	WR20	NOT USED
1	1	0	1	0	1	WR21	NOT USED
1	1	0	1	1	0	WR22	NOT USED
1	1	0	1	1	1	WR23	NOT USED
1	1	1	0	0	0	WR24	RR24
1	1	1	0	0	1	WR25	RR25
1	1	1	0	1	0	NOT USED	NOT USED
1	1	1	0	1	1	NOT USED	RR27
1	1	1	1	X	X	WR28	RR28
1	1	1	1	X	X	WR29	RR29
1	1	1	1	X	X	WR30	RR30
1	1	1	1	X	X	WR31	RR31

X = don't care

WRITE REGISTER 0: COMMAND

```
  7   6   5   4   3   2   1   0
+-------------------------------+
|   |   |   |   |   |   |   |   |
+-------------------------------+
  |   |   |   |   |   |   |   |_______  1 = Read
  |   |   |   |   |   |   |
  |   |   |   |   |   |   |___________  1 = Write
  |   |   |   |   |   |
  |   |   |   |   |   |_______________  0 = Normal
  |   |   |   |   |   |_______________  1 = Format I/D Data
  |   |   |   |   |
  |   |   |   |   |___________________  0 = Normal
  |   |   |   |   |___________________  1 = Long (ECC to/from
  |   |   |   |                             Buffer)
  |   |   |   |
  |   |   |   |_______________________  1 = Syndrome to Buffer
  |   |   |
  |   |   |___________________________  0 = Abort on Flag Non-Zero
  |   |   |___________________________  1 = Ignore Flag Condition
  |   |
  |   |_______________________________  1 = Verify (Buffer to
  |                                         Disk Data)
  |___________________________________  1 = No Data Transfer
```

The Command register contains 5050 commands and command options.

Bits 0 and 1 determine whether the operation is a read or a write. When bit 0 is set, data is read from the disk to the buffer; when bit 1 is set, data is written from the buffer to the disk.

When bit 2 is set, and the operation is a read, only ID fields will be read to the buffer. In the case of write operations, the entire track will be formatted, i.e., both the ID and data fields will be written to the disk. In this case, the ID information is read from the buffer, and data information is read from the sequencer's Register File at State 11, with the number of requests for each ID determined by the Count register.

When bit 3 is set, both the data and the ECC check bits will be written to or read from the buffer.

When bit 4 is set, the syndrome (the result of the ECC check) will be written to the buffer.

Bit 5 allows processor intervention on all flag conditions. Normally, this bit is clear, i.e., reads and writes to sectors with a flag condition will cause the command to be aborted and the FLAG BYTE/BIT NON-ZERO bit of the Extended Status register to be set. However, having determined the cause of the error, the microprocessor may decide to read or write the sector anyway, in which case it sets this bit.

When bit 6 is set, data is read from the buffer, and the sequencer performs a byte-by-byte comparison with data on the disk.

Bit 7 permits data fields to be read and checked for errors without transfer of the data to the buffer.

WRITE REGISTER 1: SEQUENCER LOOP COUNT

```
   7   6   5   4   3   2   1   Ø
 +-------------------------------+
 |   |   |   |   |   |   |   |   |
 +-------------------------------+
   |___|___|___|___|___|___|___|_______ Number of Sectors
                                        (N = N)
```

This register specifies the number of sectors to be read or written, or in the case of a format command, the number of sectors on the disk. (Actually, the value in this register specifies the number of times the loop in the predefined state sequence for the particular command is executed, as explained in Section 3.2.) This value is decremented for each sector handled by the command. An internal count register contains the initial value of this register, so that for repeated commands involving the same number of sectors, the register will be automatically reloaded with the proper value.

WRITE REGISTER 2: INDEX TIME-OUT

```
   7   6   5   4   3   2   1   Ø
 +-------------------------------+
 |   |   |   |   |   |   |   |   |
 +-------------------------------+
                   |___|___|___|_______ Number of Revolutions
                                        Before Time-Out
```

This register specifies the number of disk revolutions (as measured by the number of index pulses) before time-out. Thus, the number of automatic retries per command attempted by the sequencer may be from 2 to 15.

WRITE REGISTER 3: SUB-BLOCK COUNT

```
    7   6   5   4   3   2   1   0
  +---------------------------------+
  |   |   |   |   |   |   |   |   |
  +---------------------------------+
    |___|___|___|___|___|___|___|_______ Number of Sub-Blocks
                                          per Sector
```

This register specifies the number of sub-blocks per sector. The total bytes per sector is equal to this value times the data field count; thus, the sector size may be as large as 65K bytes.

WRITE REGISTER 4: CYLINDER HIGH

```
    7   6   5   4   3   2   1   0
  +---------------------------------+
  |   |   |   |   |   |   |   |   |
  +---------------------------------+
    |___|___|___|___|___|___|___|_______   00-FF
```

This register contains the most significant eight bits of the desired cylinder number. This value is used in conjunction with the Cylinder Low register, specifying a range of 0 to 65535.

WRITE REGISTER 5: CYLINDER LOW

```
    7   6   5   4   3   2   1   0
  +---------------------------------+
  |   |   |   |   |   |   |   |   |
  +---------------------------------+
    |___|___|___|___|___|___|___|_______   00-FF
```

This register contains the least significant eight bits of the desired cylinder number.

WRITE REGISTER 6: HEAD ADDRESS

```
    7   6   5   4   3   2   1   0
  +---------------------------------+
  |   |   |   |   |   |   |   |   |
  +---------------------------------+
    |___|___|___|___|___|___|___|_______   00-FF
```

This register contains the address of the read/write head accessed by the command.

WRITE REGISTER 7: SECTOR NUMBER

```
   7   6   5   4   3   2   1   0
 +-------------------------------+
 |   |   |   |   |   |   |   |   |
 +-------------------------------+
   |___|___|___|___|___|___|___|_______   00-FF
```

This register specifies the sector number to be read or written. It is a counter register that is auto-incremented at the end of a data field operation.

WRITE REGISTER 8: MICRO TO MEMORY

```
   7   6   5   4   3   2   1   0
 +-------------------------------+
 |   |   |   |   |   |   |   |   |
 +-------------------------------+
   |___|___|___|___|___|___|___|_______   00-FF
```

This register contains data to be transferred from the microprocessor to DMA buffer memory.

WRITE REGISTER 9: SEQUENCER START/RE-START

```
   7   6   5   4   3   2   1   0
 +-------------------------------+
 |   |   |   |   |   |   |   |   |
 +-------------------------------+
   |   |   |   |   |___|___|___|_______   Start State X0-XF
   |   |   |   |
   |___|___|___|_______________________   Re-Start State 0X-FX
```

During the execution of a command, bits 0-3 specify the state number at which the sequencer will begin execution; bits 4-7 specify the state number from which the sequence will be re-started after the state number specified in WR10 has been reached (and RR1 does not equal 0).

For purposes of initializing the Register File, bits 0-3 are used as an index into the Register File; data contained in WR14 or WR15 will be written to a Count or Value register, respectively.

WRITE REGISTER 10: SEQUENCER LOOP STATE

```
     7   6   5   4   3   2   1   0
  +---------------------------------+
  |   |   |   |   |   |   |   |   |
  +---------------------------------+
                     |___|___|___|_______  Loop State X0-XF
```

This register determines the state number of the LOOP mode, at which a jump to the RE-START mode is performed. This value will, of course, depend on the command and the particular disk configuration.

WRITE REGISTER 11: BIT RING START COUNT

```
     7   6   5   4   3   2   1   0
  +---------------------------------+
  |   |   |   |   |   |   |   |   |
  +---------------------------------+
                     |___|___|___|_______  Start Bit 0X-XF
```

This register allows the user to specify the bit-level timing relationship between sync detect and byte clock (see Figure 4). The value in this register is the ring counter start state for a four-bit ring counter.

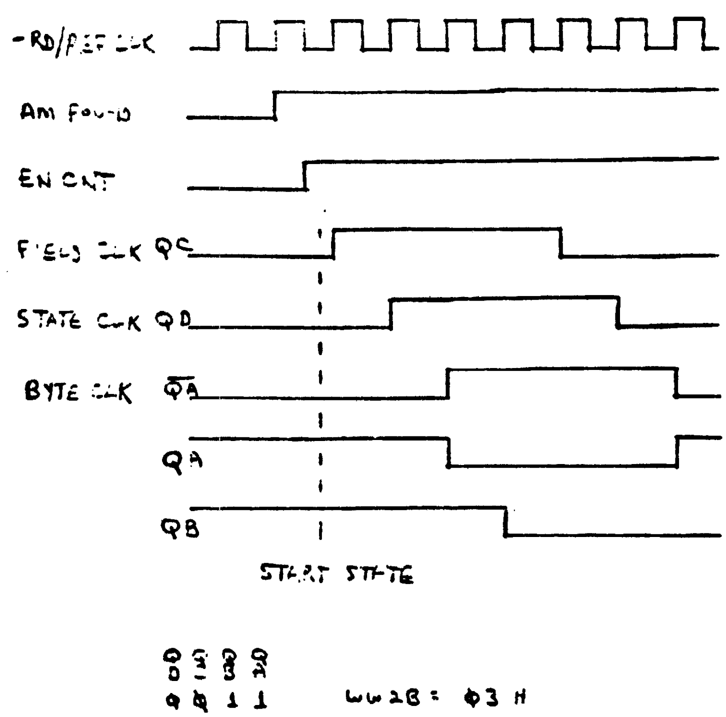


Figure 4. Sync Detect and Byte Clock Timing

WRITE REGISTER 12: ECC CONTROL

```
 7   6   5   4   3   2   1   0
+-------------------------------+
|   |   |   |   |   |   |   |   |
+-------------------------------+
 |   |   |   |   |   |   |   |
 |   |   |   |   |   |   |   |____  0 = ECC Clear on Init
 |   |   |   |   |   |   |   |____  1 = ECC Preset on Init
 |   |   |   |   |   |   |
 |   |   |   |   |   |   |________  0 = Data to ECC
 |   |   |   |   |   |   |________  1 = -Data to ECC
 |   |   |   |   |   |
 |   |   |   |   |   |____________  0 = ECC Feedback
 |   |   |   |   |   |____________  1 = -ECC Feedback
 |   |   |   |   |
 |   |   |   |   |________________  0 = ECC Data Out
 |   |   |   |   |________________  1 = -ECC Data Out
 |   |   |   |
 |   |   |   |____________________  0 = ECC Check
 |   |   |   |____________________  1 = -ECC Check
 |   |   |
 |   |   |________________________  0 = Xfer Disable
 |   |   |________________________  1 = Xfer Enable
 |   |
 |   |____________________________  0 = I-D = CRC
 |
 |________________________________  1 = Enable Data Field
                                        Sync Time-Out
```

This register allows format and media compatability with a variety of peripheral chips and various error correction formats.

Bit 0 determines whether or not initialization of the shift register string is cleared (to all zeros) or preset (to all ones).

Bits 1-4 control XOR gates, which determine the polarity of the data at various stages in the ECC check logic. Figure 5 illustrates these gates in relation to the relevant ECC circuits.

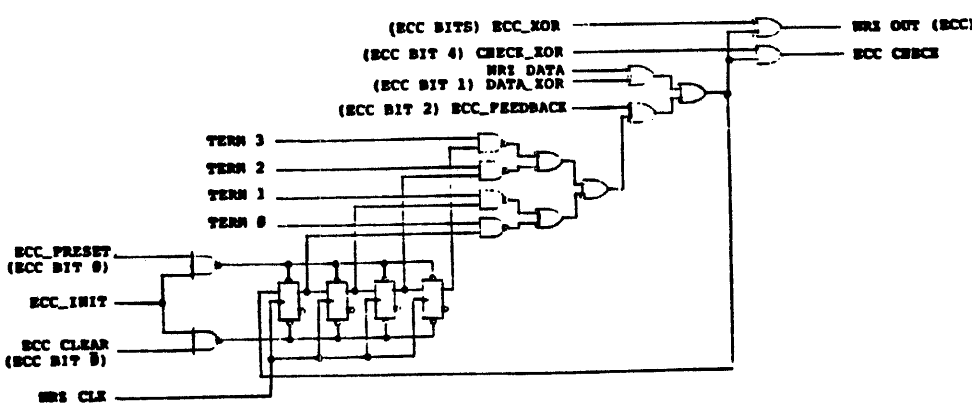


Figure 5. XOR Gate Circuit Diagram

Bit 5, when set, enables the auto-read DMA write function, in which data is transferred from an external peripheral chip to DMA buffer memory via RR31.

When bit 6 is cleared, ID information is the fixed CCITT CRC-16 polynomial, rather than the preprogrammed data field polynomial (as specified in WR16-27).

When bit 7 is set, and an ID field has been properly read, failure to find the data field sync after 512 bit times will result in a data field sync time-out.

WRITE REGISTER 13: CONFIGURATION CONTROL

```
   7   6   5   4   3   2   1   Ø
 +-------------------------------+
 |   |   |   |   |   |   |   |   |
 +-------------------------------+
   |   |   |   |   |   |   |   |______  Ø = Soft Sectored
   |   |   |   |   |   |   |   |______  1 = Hard Sectored
   |   |   |   |   |   |   |
   |   |   |   |   |   |   |__________  Ø = 1 Field Sync
   |   |   |   |   |   |   |__________  1 = 2 Field Sync
   |   |   |   |   |   |
   |   |   |   |   |   |______________  Ø = Head/Flag Byte
   |   |   |   |   |   |______________  1 = Flag Byte
   |   |   |   |   |
   |   |   |   |   |__________________  Ø = Not ESDI Config
   |   |   |   |   |__________________  1 = ESDI Config
   |   |   |   |
   |   |   |   |______________________  Ø = Internal Sync Detect
   |   |   |   |______________________  1 = External Sync Detect
   |   |   |
   |   |   |__________________________  Ø = Disable Write Gate Edge
   |   |   |__________________________  1 = Enable Write Gate Edge
   |   |
   |   |______________________________  Ø = Interrupt Active Low
   |   |______________________________  1 = Interrupt Active High
   |
   |__________________________________  Ø = Interrupt Disabled
   |__________________________________  1 = Interrupt Enabled
```

Bit Ø selects between the hard sector and soft sector disk drive environments.

Bit 1 selects between the 1 field sync (hard sector) and 2 field sync (soft sector) formats.

Bit 2 selects between the Head/Flag Byte (RR6) and the Flag Byte (RR3).

Bit 3 selects between an ESDI and a non-ESDI interface.

Bit 4 selects between internal sync detect (used for hard sector and ESDI-type interfaces) and external sync detect (used when the sequencer is configured with the VCO/Encode/Decode chip).

Setting bit 5 disables the write gate for two bit times preceding each data field preamble, thereby providing an edge of write gate for every PLO sync field as required by ESDI-type drives.

Bit 6 selects between interrupt active Low or High.

Bit 7 enables or disables interrupts.

WRITE REGISTER 14: SEQ COUNT REG @ SEQ START

```
   7   6   5   4   3   2   1   0
+-------------------------------+
|   |   |   |   |   |   |   |   |
+-------------------------------+
  |___|___|___|___|___|___|___|_______   00-FF
```

This register is used, in conjunction with WR9, to select a Count register in the Register File.

WRITE REGISTER 15: SEQ VALUE REG @ SEQ START

```
   7   6   5   4   3   2   1   0
+-------------------------------+
|   |   |   |   |   |   |   |   |
+-------------------------------+
  |___|___|___|___|___|___|___|_______   00-FF
```

This register is used, in conjunction with WR9, to select the Value register in the Register File.

WRITE REGISTERS 16-23: POLYNOMIAL GENERATOR

```
   7   6   5   4   3   2   1   0
+-------------------------------+
|   |   |   |   |   |   |   |   |
+-------------------------------+
  |___|___|___|___|___|___|___|_______   00-FF
```

These registers contain the polynomial to be used in ECC error detection and correction.

WRITE REGISTER 24: EXTERNAL REGISTER Ø STROBE

```
  7   6   5   4   3   2   1   Ø
+-------------------------------+
|   |   |   |   |   |   |   |   |
+-------------------------------+
  |___|___|___|___|___|___|___|_______   ØØ-FF
```

When this register is written, -WRTLØ (pin 5Ø) is asserted and may be used to strobe information from the microprocessor's data bus into an external peripheral chip. The information in this register may be used as additional device control lines.

WRITE REGISTER 25: EXTERNAL REGISTER 1 STROBE

```
  7   6   5   4   3   2   1   Ø
+-------------------------------+
|   |   |   |   |   |   |   |   |
+-------------------------------+
  |___|___|___|___|___|___|___|_______   ØØ-FF
```

When this register is written, -WRTL1 (pin 51) is asserted and may be used to strobe information from the microprocessor's data bus into an external peripheral chip. The information in this register may be used as additional device control lines.

WRITE REGISTER 28-31: EXTERNAL GROUP STROBE

```
  7   6   5   4   3   2   1   Ø
+-------------------------------+
|   |   |   |   |   |   |   |   |
+-------------------------------+
  |___|___|___|___|___|___|_______________   ØØ-FF
```

When these registers are written, -GRPWRT (pin 52) is asserted and may be used to strobe information from the microprocessor's data bus into an external peripheral chip. The information in these registers may be used as additional device control lines.

READ REGISTER Ø: STATUS

```
   7   6   5   4   3   2   1   Ø
+-------------------------------+
|   |   |   |   |   |   |   |   |
+-------------------------------+
  |   |   |   |   |   |   |   |_______ 1 = Busy
  |   |   |   |   |   |   |
  |   |   |   |   |   |   |__________ 1 = Data ECC Error
  |   |   |   |   |   |
  |   |   |   |   |   |______________ 1 = Data Sync +
  |   |   |   |   |                       Marker Not Found
  |   |   |   |   |
  |   |   |   |   |__________________ 1 = Data Verify Error
  |   |   |   |
  |   |   |   |______________________ 1 = ID ECC Error
  |   |   |
  |   |   |__________________________ 1 = ID Sync + Marker
  |   |                                   Not Found
  |   |
  |   |______________________________ 1 = ID Data No Compare
  |
  |__________________________________ 1 = Extended Status
                                          Non-Zero
```

The Status register holds device status information, and is read at the completion of every command to determine whether execution was successful. During command execution, this register may be polled by the microprocessor in order to determine the bit-significant status of sector field reads on a sector-by-sector basis. For example, when a time-out has occurred, the microprocessor can determine whether or not an ID was read successfully (though the ID did not compare), or whether no IDs were successfully read, in which case the disk is improperly formatted or incompatible with the controller.

Bit Ø is set when a command is in progress.

Bit 1 is set during read operations when the sequencer detects an ECC error in the data field.

Bit 2 is set when, in external sync mode, the Address Mark is detected (A-M FOUND is true) but the byte value does not compare with the sync or marker byte in the Register Register File (see Section 2.2.2).

Bit 3 is set when an error is detected during the Read Verify command.

Bit 4 is set if an ECC error is detected in the ID field.

Bit 5 is set during execution of read/write operations if the sector's ID sync and ID address mark (or deleted address mark) cannot be found. The number of disk revolutions which may occur before this bit is set is determined by the value in WR2.

Bit 6 is set when the sequencer detects that the four-byte ID data field does not correspond to the contents of WR4-7.

Bit 7 is set when any bit in the Extended Status register is set.

READ REGISTER 1: EXTENDED STATUS

```
   7   6   5   4   3   2   1   0
+--------------------------------+
|   |   |   |   |   |   |   |   |
+--------------------------------+
  |   |   |   |   |   |   |   |______  1 = Disk Data Over/
  |   |   |   |   |   |   |                Under Run
  |   |   |   |   |   |   |
  |   |   |   |   |   |   |__________  1 = Micro Mem Over/
  |   |   |   |   |   |                    Under Run
  |   |   |   |   |   |
  |   |   |   |   |   |______________  1 = Index Time-Out
  |   |   |   |   |
  |   |   |   |   |__________________  1 = Flag Byte/Bit Non-Zero
  |   |   |   |
  |   |   |   |______________________  1 = Data Field Sync
  |   |   |                                Time-Out
  |   |   |
  |   |   |__________________________  Not Used
  |   |
  |   |______________________________  Sector
  |
  |__________________________________  Index
```

The Extended Status register contains additional device status information about command execution.

Bit 0 is set either when the buffer is not emptied fast enough to keep up with new data being transferred to it from the disk (overrun), or when the transfer of data from the buffer to the sequencer doesn't keep up with the sequencer's requests for data (underrun).

Bit 1 is set either when the buffer is not emptied fast enough to keep up with new data being transferred to it from the microprocessor (overrun), or when the transfer of data from the buffer to the microprocessor doesn't keep up with the microprocessor's requests for data (underrun).

Bit 2 is set when the maximum number of revolutions per command retry have occurred.

Bit 3 is set when any bit in the Flag register or the flag field of the Head/Flag register is set.

Bit 4 is set when the ID field has been properly read, but the data field sync has not been detected after 512 bit times.

Bits 6 and 7 are status bits reflecting the state of the Sector and Index lines, respectively.

READ REGISTER 2: RETRY COUNT/STATE ADDRESS

```
     7   6   5   4   3   2   1   Ø
 +--------------------------------+
 |   |   |   |   |   |   |   |   |
 +--------------------------------+
     |   |   |   |   |___|___|___|_______  XØ-XF = Retry Count
     |   |   |   |
     |___|___|___|_______________________  ØX-FX = Sequencer
                                                   State Address
```

Bits Ø-3 contain the actual number of retries on error attempted by the sequencer.

Bits 4-7 are a fall-through of the SEQ AØ-3 lines, thus reflecting the real-time state of the sequencer.

READ REGISTER 3: FLAG BYTE

```
     7   6   5   4   3   2   1   Ø
 +--------------------------------+
 |   |   |   |   |   |   |   |   |
 +--------------------------------+
     |___|___|___|___|___|___|___|_______  ØØ-FF = Flag Byte
                                                   (Header Byte 4)
```

This register contains the fifth byte of header flag information for disks so configured.

READ REGISTER 4: CYLINDER HIGH

```
  7   6   5   4   3   2   1   0
+-------------------------------+
|   |   |   |   |   |   |   |   |
+-------------------------------+
  |___|___|___|___|___|___|___|_______  00-FF = Cylinder High
                                                (Header Byte 4)
```

The Cylinder High register contains the most significant byte of the cylinder number in the current ID field, with which the sequencer has established proper ID sync.

READ REGISTER 5: CYLINDER LOW

```
  7   6   5   4   3   2   1   0
+-------------------------------+
|   |   |   |   |   |   |   |   |
+-------------------------------+
  |___|___|___|___|___|___|___|_______  00-FF = Cylinder Low
                                                (Header Byte 1)
```

The Cylinder Low register contains the least significant byte of the cylinder number in the current ID field, with which the sequencer has established the proper ID sync.

READ REGISTER 6: HEAD/FLAG

```
  7   6   5   4   3   2   1   0
+-------------------------------+
|   |   |   |   |   |   |   |   |
+-------------------------------+
  |   |   |   |   |___|___|___|_______  00-FF = Head Address
  |   |   |   |                                 (Header Byte 2)
  |   |   |   |
  |   |   |   |
  |___|___|___|_______________________  Flag
```

Bits 0-3 contain the head address for the currently executing command.

Bits 4-7 contain bit-specific error information. When these bits are non-zero, the command is aborted, the Busy and Extended Status Non-Zero bits in the Status register are reset, and Flag Byte/Bit Non-Zero bit in the Extended Status register is set.

READ REGISTER 7: SECTOR

```
   7   6   5   4   3   2   1   0
+-------------------------------+
|   |   |   |   |   |   |   |   |
+-------------------------------+
  |___|___|___|___|___|___|___|________   00-FF = Sector
                                                  (Header Byte 3)
```

The Sector register contains the sector number in the current ID field, with which the sequencer has established proper ID sync.

READ REGISTER 8: MEMORY TO MICRO

```
   7   6   5   4   3   2   1   0
+-------------------------------+
|   |   |   |   |   |   |   |   |
+-------------------------------+
  |___|___|___|___|___|___|___|________   00-FF = Memory to Micro
```

This register contains information transferred from DMA buffer memory to the microprocessor.

READ REGISTER 9: SEQUENCER LOOP COUNT

```
   7   6   5   4   3   2   1   0
+-------------------------------+
|   |   |   |   |   |   |   |   |
+-------------------------------+
  |___|___|___|___|___|___|___|________   Number of Sectors
                                          (N = N)
```

This register returns the current value of WR1, which is the remaining number of sectors to be handled by the currently executing command.

READ REGISTER 14: SEQ COUNT REG @ SEQ START

```
   7   6   5   4   3   2   1   0
+-------------------------------+
|   |   |   |   |   |   |   |   |
+-------------------------------+
  |___|___|___|___|___|___|___|________   00-FF
```

This register returns the value in the Register File indexed by WR9.

READ REGISTER 15: SEQ VALUE REG @ SEQ START

```
   7   6   5   4   3   2   1   0
 +-------------------------------+
 |   |   |   |   |   |   |   |   |
 +-------------------------------+
   |___|___|___|___|___|___|___|_______     00-FF
```

This register returns the value in the Register File indexed by WR9.

READ REGISTER 24: EXTERNAL STATUS 0

```
   7   6   5   4   3   2   1   0
 +-------------------------------+
 |   |   |   |   |   |   |   |   |
 +-------------------------------+
   |___|___|___|___|___|___|___|_______     00-FF = External Status 0
```

When this register is read, INST0 is asserted (pin 48), and additional device status information contained in an external peripheral chip may be read by the microprocessor from its data bus.

READ REGISTER 25: EXTERNAL STATUS 1

```
   7   6   5   4   3   2   1   0
 +-------------------------------+
 |   |   |   |   |   |   |   |   |
 +-------------------------------+
   |___|___|___|___|___|___|___|_______     00-FF = External Status 1
```

When this register is read, INST1 is asserted (pin 49), and additional device status information contained in an external peripheral chip may be read by the microprocessor from its data bus.

READ REGISTER 27: MICRO-DMA MEMORY TO EXTERNAL GROUP

```
   7   6   5   4   3   2   1   0
 +-------------------------------+
 |   |   |   |   |   |   |   |   |
 +-------------------------------+
   |___|___|___|___|___|___|___|_______     00-FF
```

When this register is read, a write strobe is generated to a peripheral chip, enabling data to be written to it from the Memory to

Micro register (RR8). On the trailing edge of the strobe, a DMA request is issued to read the next location of the buffer memory to RR8, in order that the entire operation can be repeated.

READ REGISTERS 28-31: EXTERNAL IN GROUP STROBE

```
  7   6   5   4   3   2   1   0
+-------------------------------+
|   |   |   |   |   |   |   |   |
+-------------------------------+
  |___|___|___|___|___|___|_______________   00-FF
```

When these registers are read, -GRPRD (pin 53) is asserted, and additional device status information contained in external registers may be read by the microprocessor from its data bus. When the XFER Enable bit in the ECC Control register is set, a read from RR31 generates a read strobe to an external peripheral device, enabling information to be latched into the Micro to Memory register (WR8). The rising edge of this strobe causes a DMA request to be written into the buffer memory, thereby initiating preparation for a repeat of the operation.

2.2.2 Format Parameter Register File

The Format Parameter Register File is a bank of 32 individually addressable 8-bit registers, which specify the size and content of the various fields on the disk. These registers may be located in any type of external memory (e.g., RAM, bipolar ROM, ROM, EPROM). The registers are grouped in pairs, each pair corresponding to a field on the disk. For each such field, the Count register specifies the number of bytes in the particular field, and the Value register specifies the actual value contained in that field.

Accesses to the Register File are made via three registers: WR9, WR14, and WR15. The address contained in WR9 indexes into the Register File and, together with the data contained in WR14 or WR15, selects a Count or Value register to be read or written. (This is explained in detail in Appendix A.) These registers and the corresponding contents of WR9 are listed in Table 3.

Table 3. Format Parameter Register File

Register Pair Name	WR9 Bits 0-3	Count Register	Value Register
ESDI Sector Gap	0	Y	Y
Post-Index Gap	1	Y	Y
ID Preamble	2	Y	Y
ID Sync	3	Y	Y
ID Marker	4	Y	Y
ID Data Field	5	Y	N
ID ECC	6	Y	N
ID Postamble	7	Y	Y
Data Preamble	8	Y	Y
Data Sync	9	Y	Y
Data Marker	10	Y	Y
Data Field	11	Y	Y
Data ECC	12	Y	N
Data Postamble	13	Y	Y
Inter-Sector-Gap	14	Y	Y
Pre-Index Gap	15	Y	Y

2.3 COMMANDS

All commands executed by the 5050 Data Sequencer are accomplished by a predefined sequence of steps, or states, each performing a specific operation. Each state in the sequence has both a count and a value parameter associated with it. These values are stored either in the Count and Value registers in the Register File, in one of the internal registers, or in memory. At each state in the sequence, the value parameter is read from or written to the disk the number of times specified by the count. The state sequence for the Format Command is shown in Figure 6.

FORMAT COMMAND

State	Mode	Function	Count	Value
0		----		
1	START	POST INDEX GAP	SEQ-CNT	SEQ-VAL
2	RESTART	ID PREAMBLE	SEQ-CNT	SEQ-VAL
3		ID SYNC BYTE	SEQ-CNT	SEQ-VAL
4		ID MARKER BYTE	SEQ-CNT	SEQ-VAL
5		ID DATA FIELD	SEQ-CNT	MEMORY
6		ID ECC	SEQ-CNT	ECC GENERATOR
7		ID POSTAMBLE	SEQ-CNT	SEQ-VAL
8		DATA PREAMBLE	SEQ-CNT	SEQ-VAL
9		DATA SYNC BYTE	SEQ-CNT	SEQ-VAL
10		DATA MARKER BYTE	SEQ-CNT	SEQ-VAL
11		DATA FIELD	CNT*BLK	SEQ-VAL
12		DATA ECC	SEQ-CNT	ECC GENERATOR
13		DATA POSTAMBLE	SEQ-CNT	SEQ-VAL
14	LOOP	INTER SECTOR GAP	SEQ-CNT	SEQ-VAL
15	HOLD	PRE-INDEX GAP (HOLD)	INDEX	SEQ-VAL
16		DONE		

Figure 6. State Sequence for Format Command

Execution begins at the start state and continues sequentially to the loop state. It then jumps back to the restart state and repeats the sequence for each sector to be formatted.

Three internal registers are used to control the execution of the state sequence. Bits 0-3 of WR9 (Sequencer Start/Restart State) determine the state number at which the sequencer will begin execution. Bits 0-3 of WR10 (Sequencer Loop State) specify the state at which the jump (i.e., the state number of the LOOP mode as shown in Figure 5) will be performed, the jump being taken if WR1 (Sequencer Loop Count register) is not equal to 0. If the jump is taken, the next state to be executed will be the state number specified in bits 4-7 of WR9. Each time a jump is taken, WR1 is decremented.

The HOLD mode is reached after the loop has been executed the specified number of times. The 5050 stays in this mode until an index pulse is received, thereby re-establishing synchronization with the disk.

Appendix B contains the state sequences for all commands used with the standard soft-sectored format. Appendix C contains the state sequences of selected commands for hard-sectored, ESDI-sectored, and ESDI Address Mark disk environments.

2.4 OPERATING MODES

The 5050 has two basic operating modes: a Z8-type mode and an 8085/8051-type mode. The only differences between these two modes result from the specific microprocessor control lines used in the microprocessor-5050 interface (e.g., Read/Write in the Z8 vs. Read Strobe and Write Strobe in the 8085/8051). Thus the timing characteristics and pin functions vary somewhat. Chapter 3 provides the specific information.

CHAPTER 3

INTERFACING

3.1 SIGNAL DESCRIPTIONS

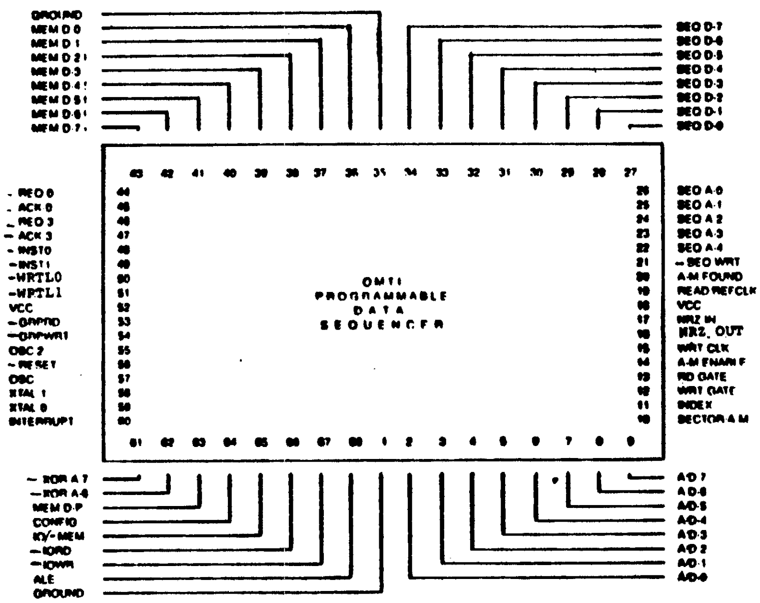


Figure 7. Pin Assignments

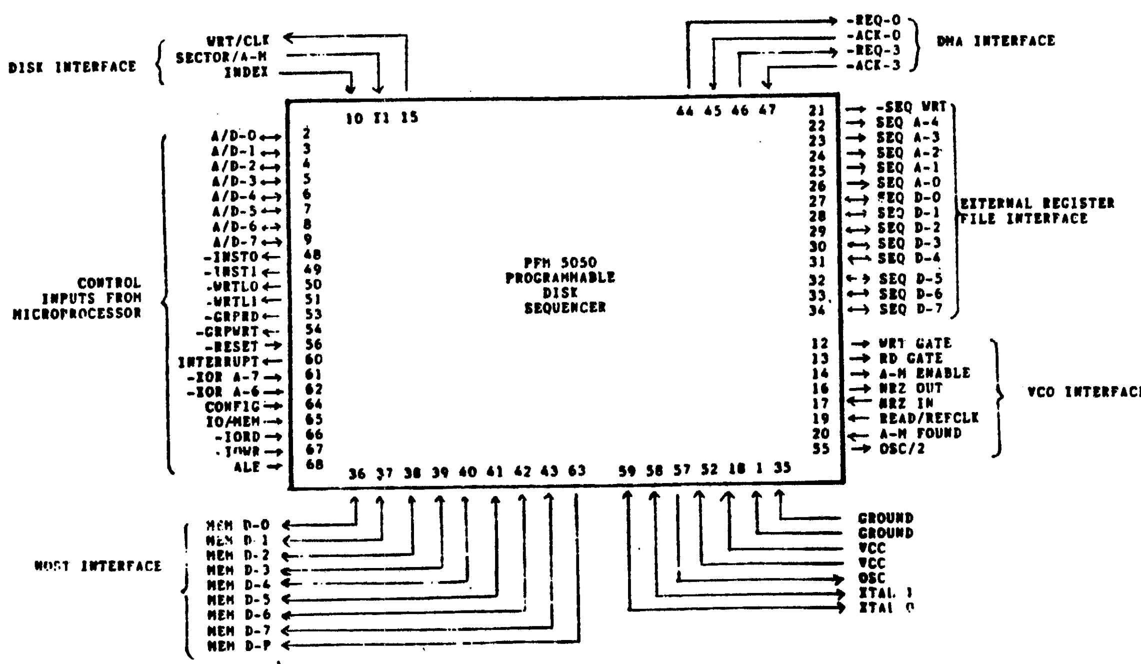


Figure 8. Pin Functions

Table 4. Pin Descriptions

Symbol	Type	Pin #	Name and Function
-ACK0 -ACK3	I	45 47	DMA Memory Acknowledge. (Active Low.) This input strobe is used to enable data from the data sequencer in a write memory operation, or to save data in the sequencer in a read memory operation.
A/D0- A/D7	I/O	2-9	Address/Data Bus. (Active High, 3-state.) These multiplexed lines interface with the low-order eight bits of the microprocessor's Address/Data bus. Addresses are latched into the address register on the falling edge of ALE. If the address is within the range of the internal chip select, data is either written into or read from the Data Sequencer registers, depending on whether -IOWR or -IORD is active.
ALE	I	68	Address Latch Enable. (Active High.) The falling edge of ALE is used to latch A/D0-A/D7 into the selected address register.
A-M ENABLE	O	14	Address Mark Enable. (Active High.) If ESDI mode is selected, this output is active at state 1 strobe time. This function is for writing the Address Mark to the disk. If ESDI mode is not selected, A-M ENABLE is active for state strobe 3 and 9, and can be used for external encoding of the drop clock byte.
A-M FOUND	I	20	Address Mark Found. (Active High.) This signal an output from the VCO/Encode/Decode chip, and is used by the Data Sequencer for MFM byte synchronization.
CONFIG	I	64	Configuration. (Active High.) This input signal is internally pulled-up and is used to select the microprocessor strobe inputs. When this line is grounded, the chip is configured for an 8085/8051 type processor; when it is left open, the chip is configured for a Z8-type processor.

Table 4. Pin Descriptions, continued

Symbol	Type	Pin #	Name and Function
-GRPRD	O	53	Group Read Strobe. (Active Low.) This output strobe provides an interface to an external peripheral chip in order to perform block transfers via the 5060 Memory Controller.
-GRPWRT	O	52	Group Write Strobe. (Active Low.) This output strobe provides an interface to an external peripheral chip in order to perform block transfers via the 5060 Memory Controller.
INDEX	I	11	Index. (Active High.) This signal from the disk is pulsed each revolution. The Data Sequencer uses the rising edge of this signal only during formatting, and for resynchronizing the timing circuitry on each revolution.
-INST0 -INST1	O O	48 49	In Status 0-1. (Active Low.) These output strobes are internally decoded I/O read strobes (enabled by reading from RR24 or RR25, respectively), used by the microprocessor to read device status from an external peripheral chip to the A/D bus.
INTERRUPT	O	60	Interrupt. (Active High.) If enabled, this signal is asserted when the Data Sequencer has completed executing a command. This output is deasserted when the microprocessor reads the Status Register.
IO/-MEM	I	65	I/O/-Memory. (I/O active High, Memory active Low.) This signal is used for active High chip enable. In 8085/8051 mode, this line is connected to the 8085/8051's IO/-MEM line; in Z8 mode, this line is an active Low chip enable.
-IORD	I	66	I/O Read. (Active Low.) When this input is Low, it is used by the microprcessor to read status information from the Data Sequencer. Data is read from the appropriate register, as selected by the current value of the address register.
-IOWR	I	67	I/O Write. (Active Low.) When this input is Low, it is used by the microprocessor to write information to the Data Sequencer. Data is written to the appropriate register, as selected by the current value of the address register.

Table 4. Pin Descriptions, continued

Symbol	Type	Pin #	Name and Function
MEM DØ- MEM D7	I/O	36- 43	I/O Memory Data. (Active High.) This 8-bit bidirectional bus is used to transfer data to and from DMA buffer memory.
MEM D-P	O	63	Memory Data Parity. (Active High.) This output line is a fall-through odd parity of the memory data bus. It allows parity checking to be performed on transfers to or from DMA buffer memory.
NRZ IN	I	17	NRZ Data In. (Active High.) This serial data input line is the output of the 5Ø7Ø VCO/Encode/Decode chip or an ESDI-type disk drive.
NRZ OUT	O	16	NRZ Data Out. (Active High.) When WRT GATE is active, this serial data output line transmits all serial data and the ECC field as programmed in the sequencer.
OSC	O	57	Oscillator. (Active High.) This is a TTL output of the XTAL frequency.
OSC/2	O	55	Oscillator 2. (Active High.) This signal is a free running clock at one half the oscillator output.
RD GATE	O	13	Read Gate. (Active High.) This output line is active during read commands. The 5Ø7Ø VCO/Encode/Decode chip must provide AM FOUND when the sequencer is in external sync mode.
RD/REFCLK	I	19	Read/Reference Clock. (Active High.) This input signal has two alternative functions. When RD GATE is true, this signal provides the read clock after the VCO is locked to the data. When WRT GATE is true, it outputs the reference clock. A clock must always be present at this input.
-REQØ -REQ3	O O	44 46	DMA Sequencer Request. (Active Low.) These output lines are used by the sequencer to request data transfers to or from the 5Ø6Ø Memory Controller.

Table 4. Pin Descriptions, continued

Symbol	Type	Pin #	Name and Function
-RESET	I	56	Reset. (Active Low.) When active, this input signal resets RD GATE or WRITE GATE and puts the chip in a not-busy mode.
SECTOR/ A-M FOUND	I	10	SEC/A-M Found/Sync. (Active High.) This line can be configured as either the sector line in a hard-sectored drive, or as the address-mark-found input from an ESDI-type drive.
SEQ A0- SEQ A4	O	26- 22	Sequencer Address. (Active High.) The address lines SEQ A0-A3 select the sequencer's state (0 - 15); SEQ A4 selects the state's Count or Value field (Count = 1, Value = 0).
SEQ D0- SEQ D7	I/O	27- 34	Sequencer Data. (Active High.) The sequencer uses this 8-bit bidirectional data bus to access the external Format Parameter Register File.
-SEQ WRT	O	21	Sequencer Write. (Active Low.) This signal is active when the microprocessor is downloading the sequencer's external Register File.
-WRTL0- -WRTL1	O	50 51	Write Latch 0-1. (Active Low.) These output strobes enable the writing of device status from external peripheral devices via an external latch to the microprocessor's data bus.
WRT CLK	O	15	Write Clock. (Active High.) This signal is the 1-f NRZ Write Clock at the RD/REFCLK rate.
WRT GATE	O	12	Write Gate. (Active High.) This signal is asserted during disk write operations.
XOR6- XOR7	I	62- 61	Exclusive OR Address. (Active Low.) These internally pulled up signals are used for the internal chip select. They control the polarity of the corresponding address line. If another Group Chip Select is required, the appropriate line must be grounded.

Table 4. Pin Descriptions, continued

Symbol	Type	Pin #	Name and Function
XTAL0-XTAL1	I/O	59-58	Crystal 0-1. (Active High.) The XTAL lines must be connected to an external crystal oscillator to provide the OSC and OSC/2 outputs. If an external clock source is available, a clock input can be connected to the XTAL0 input, with the XTAL1 line left open.
VCC	I	52, 18	VCC. +5 V.
GND	I	35, 1	Ground.

3.2 A.C. CHARACTERISTICS

The two relevant timing diagrams and associated A.C. characteristics for interfacing the OMTI 5050 PFM Data Sequencer to a Z8 or an 8085/8051 processor are given below. (For more information about these chips, the reader is referred to Zilog's Z8681/82 ROMless Z8 Microcomputer Product Specification or Intel's 8051 Single Chip 8-Bit N-Channel Microprocessors Data Sheet.)

3.2.1 Z8 Mode Timing Characteristics (Configuration = 0)

Number	Parameter	Min (ns) (10 MHz)	Max (ns) (10 MHz)
1	-AS Low Pulse Width	50	
2	Address Setup to -AS High	25	
3	Address Hold after -AS High	25	
4	-AS High to -DS Low	50	
5	-DS Low Pulse Width	100	
6	-DS High to -AS Low	40	
7	Data Setup to -DS (Write)	25	
8	Data Hold after -DS (Write)	25	
9	-DS Low to Data Valid (Read)		50
10	-DS High to Data Invalid (Read)	0	
11	-DS High to Data Float (Read)		35

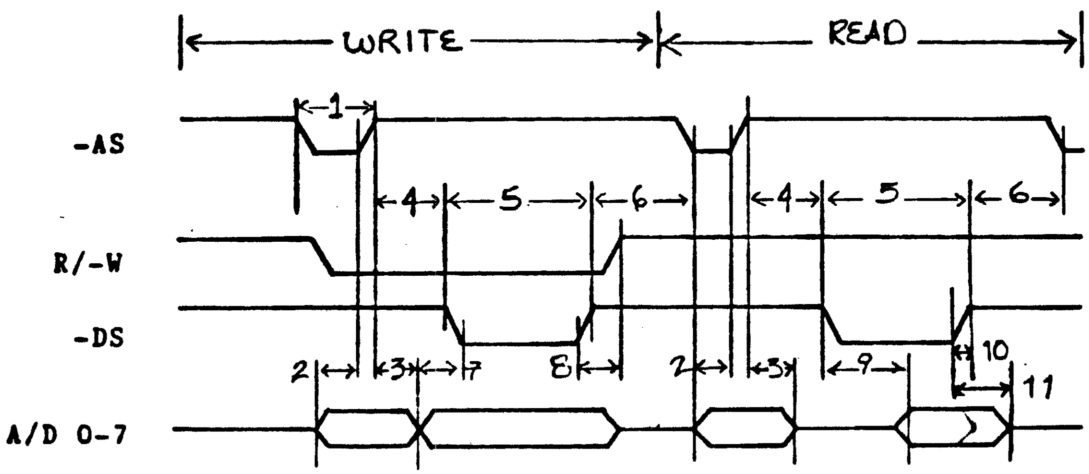


Figure 9. Z8 Mode Timing

3.2.2. 8085/8051 Mode Timing Characteristics (Configuration = 1)

Number	Parameter	Min (ns) (10 MHz)	Max (ns) (10 MHz)
1	ALE High Pulse Width	50	
2	Address Setup to ALE Low	25	
3	Address Hold after ALE Low	25	
4	ALE Low to -IORD/-IOWR Low	50	
5	-IORS/-IOWR Low Pulse Width	100	
6	Data Setup to -IOWR High	40	
7	Data Hold after -IOWR High	25	
8	Data Hold after -IOWR High	25	
9	-IORD Low to Valid Dataa		50
10	-IORD High to Data Invalid	0	
11	-IORD High to Data Float		35

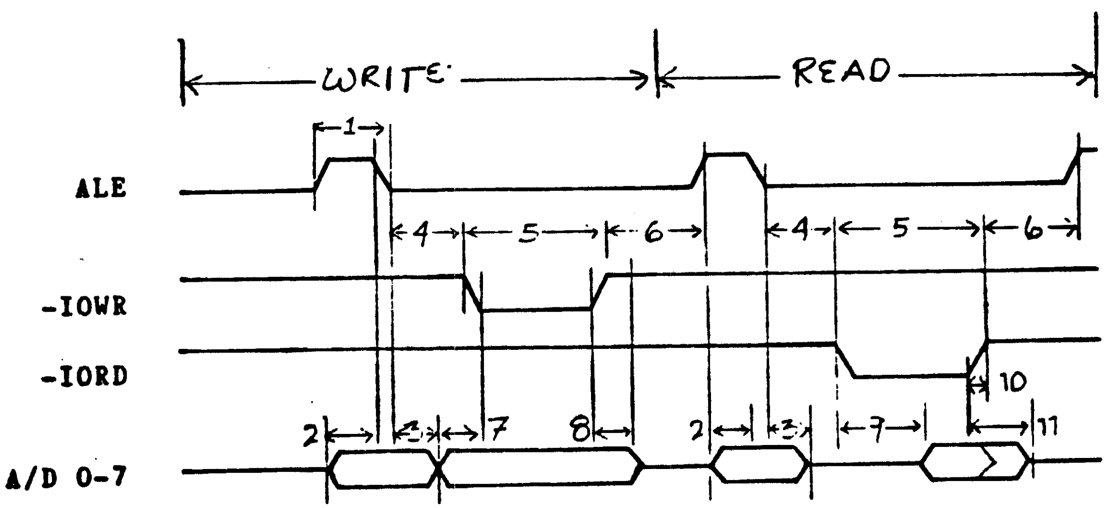


Figure 10. 8085/8051 Mode Timing

3.3 D.C. INFORMATION

3.3.1 Absolute Maximum Ratings

- Voltages on all pins with respect to GND range from -0.3 V to +7.0 V.
- Ambient operating temperature is 0°C to +70°C .
- Storage temperature ranges from -65°C to +150°C.

Note that stresses greater than those indicated may cause permanent damage. Operation of the chip at conditions above those shown is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the chip's reliability.

3.3.2 Standard Test Conditions

The characteristics shown below apply for the following test conditions, unless otherwise noted. Voltages are referenced to GND. Positive current flows into the reference pin. Standard conditions are as follows:

- +4.75 V < VCC < +5.25 V
- GND = 0 V
- 0°C < TA < +70°C

3.3.3 D.C. Characteristics

Parameter	Min	Max	Unit	Condition	Notes
Input High Voltage	2	VCC	V		
Input Low Voltage	-0.3	-8	V		
Output High Voltage	2	VCC	V		
Output Low Voltage		0.4	V		
Input Leakage	-30	10	uA		
Output Leakage		10	uA		
VCC Supply Current		50	mA		

3.4 PACKAGE DIMENSIONS

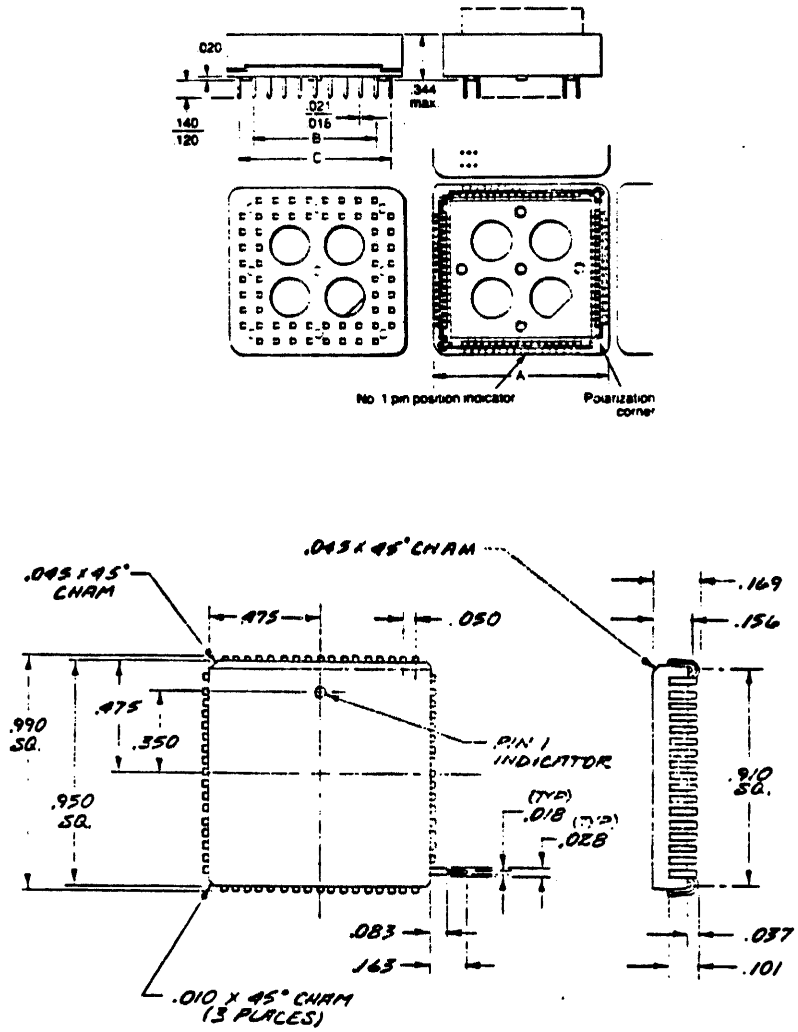


Figure 11. Socket and Package Dimensions

APPENDIX A

INITIALIZATION OF THE REGISTER FILE

In order to initialize the Format Parameter Register File, a table is first set up, typically in ROM, containing the values to be written into the file. Each Define Byte directive specifies the contents of a Count or Value register. An example table for a soft-sectored format is as follows:

```
SEQTBL:
        DB    001H          ;; State 0 Count
        DB    000H          ;; State 0 Value
        DB    00BH          ;; Post Index Byte Count
        DB    04EH          ;; Post Index Data Value
        DB    00CH          ;; ID Preamble Byte Count
        DB    000H          ;; ID Preamble Data Value
        DB    001H          ;; ID Sync Byte Count
        DB    0A1H          ;; ID Sync Byte Value
        DB    001H          ;; ID Marker Byte Count
        DB    0FEH          ;; ID Marker Byte Value
        DB    004H          ;; ID Data Field Byte Count
        DB    000H          ;; ID Data Field Value (No Care)
        DB    004H          ;; ID ECC Field Count
        DB    000H          ;; ID ECC Field Value (No Care)
        DB    002H          ;; ID Postamble Byte Count
        DB    000H          ;; ID Postamble Data Value
        DB    00CH          ;; Data Field Preamble Byte Count
        DB    000H          ;; Data Field Preamble Value
        DB    001H          ;; Data Sync Byte Count
        DB    0A1H          ;; Data Sync Byte Value
        DB    001H          ;; Data Marker Byte Count
        DB    0F8H          ;; Data Marker Byte Value
        DB    004H          ;; Data Field Byte Count
        DB    0E5H          ;; Data Field Format Value
        DB    004H          ;; Data Field ECC Byte Count
        DB    000H          ;; Data Field ECC Value (No Care)
        DB    002H          ;; Data Field Postamble Byte Count
        DB    000H          ;; Data Field Postamble Data Value
        DB    00EH          ;; Inter-Sector Gap Byte Count
        DB    04EH          ;; Inter-Sector Gap Data Value
        DB    001H          ;; Pre-Index Gap Count (Wait for Index)
        DB    04EH          ;; Pre-Index Gap Value
TBLEND: EQU   $             ;; End of Table
```

Data in the table is then used by a download program to initialize the Register File. The following is an example of such a program in Z8 assembly language.

```
LOADSRF:  LD    R2,#SEQTBL > 8        ;; POINT TO TABLE HIGH
          LD    R3,#SEQTBL&0FFH       ;; POINT TO TABLE LOW
          LD    R1,.LRSTST            ;; INDEX POINTER
          LD    R4,#80H               ;; INIT HIGH BYTE OF RR4
          LD    R5,.LSEQCNT           ;; COUNT REGISTER
          LD    R9,#16                ;; LOOP COUNT
          LD    R10,#0                ;; POINTER VALUE
LOADSRF1: LDE   @RR0,R10              ;; OUTPUT INDEX VALUE
          LDC   R14,@RR2              ;; GET COUNT FROM TABLE
          LDE   @RR4,R14              ;; OUTPUT COUNT TO REGISTER FILE
          INCW  RR2                   ;; BUMP TABLE POINTER
          INC   R5                    ;; VALUE REGISTER
          LDC   R14,@RR2              ;; GET VALUE FROM TABLE
          LDE   @RR4,R14              ;; OUTPUT VALUE TO REGISTER FILE
          INCW  RR2                   ;; BUMP TABLE POINTER
          DEC   R5                    ;; COUNT REGISTER
          INC   R10                   ;; NEXT INDEX VALUE
          DJNZ  R9,LOADSRF1           ;; DO 16 TIMES
          LD    R14,#033H             ;; RESTART/START STATE
          LDE   @RR0,R14              ;; REPLACE VALUE TO SEQUENCER
          CLR   R14                   ;; CLEAR A
          LD    R1,.LSEQCMD           ;; POINT TO COMMAND
          LDE   @RR0,R14              ;; NOP COMMAND TO SEQUENCER
          INC   R1                    ;; POINT TO EXTENDED STATUS
          LDE   R14,@RR0              ;; READ EXTENDED STATUS (CLEAR STATUS)
          RET
```

A flowchart for this program is given below. Symbols enclosed in parenthesis represent the contents pointed to by the symbol.

```
     initialize cmd_ptr to point to command register
RR2  initialize table_ptr
RR4  initialize reg_ptr to point to count register; value reg
                assumed to be reset address.
RRØ  initialize index_ptr
R9   initialize loop_count = 16
R1Ø  initialize ptr_val = Ø
          |
          |
|---------V
|    move ptr_val to (index_ptr)
|    inc  ptr_val
|    move (table_ptr) to (reg_ptr)
|    inc  table_ptr
|    move (table_ptr) to (reg_ptr + 1)
|    inc  table_ptr
|    dec  loop-count
|         |
|         |
|         V
|  no
|----< loop-count > = Ø
          |  yes
          |
          V

     move Ø33H to (index_ptr)
     move ØØH to (cmd_ptr)
     move ØØH to (cmd_ptr + 1)
          |
          V

       return
```

The initialization process is summarized in Figure A-1. A register pair is selected by writing a register index number (ptr_val) into WR9. The first value in the table, which in this case is the ESDI Sector Gap Count Register, is written into WR14, thereby selecting the Count register. Using the same index value (WR9 = Ø), the value parameter (the second entry in the table) is written into WR15, thereby selecting the Value register. WR9 is then incremented, and the operation is repeated for the remaining values to be transferred.

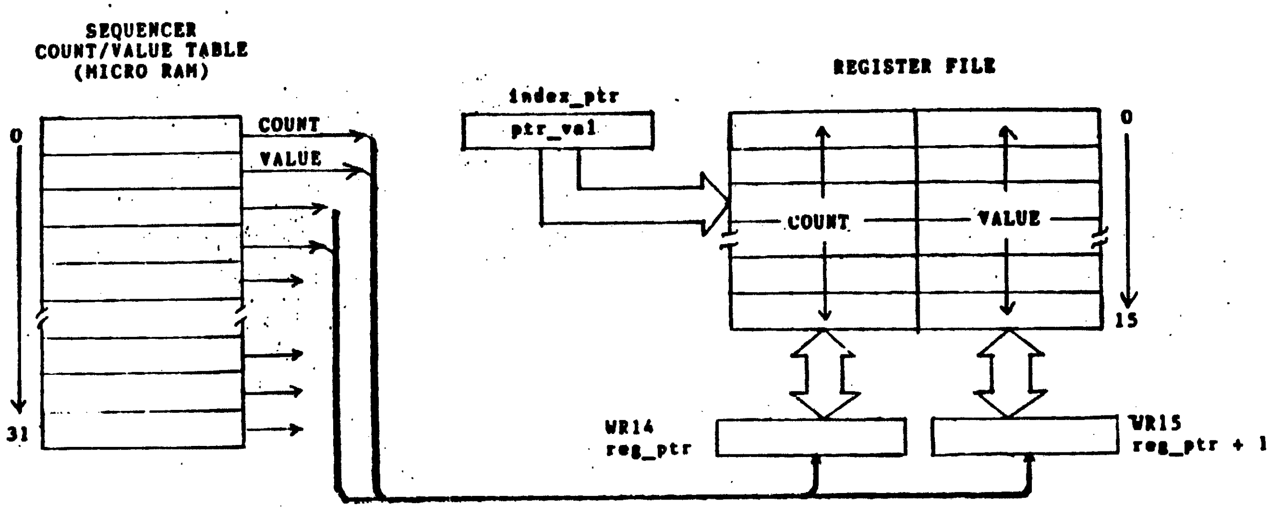


Figure A-1. Initializing the Register File

APPENDIX B

SEQUENCER STATE FLOW CHART (SOFT-SECTORED)

FORMAT COMMAND

State	Mode	Function	Count	Value
0		----		
1	START	POST INDEX GAP	SEQ-CNT	SEQ-VAL
2	RESTART	ID PREAMBLE	SEQ-CNT	SEQ-VAL
3		ID SYNC BYTE	SEQ-CNT	SEQ-VAL
4		ID MARKER BYTE	SEQ-CNT	SEQ-VAL
5		ID DATA FIELD	SEQ-CNT	MEMORY
6		ID ECC	SEQ-CNT	ECC GENERATOR
7		ID POSTAMBLE	SEQ-CNT	SEQ-VAL
8		DATA PREAMBLE	SEQ-CNT	SEQ-VAL
9		DATA SYNC BYTE	SEQ-CNT	SEQ-VAL
10		DATA MARKER BYTE	SEQ-CNT	SEQ-VAL
11		DATA FIELD	CNT*BLK	SEQ-VAL
12		DATA ECC	SEQ-CNT	ECC GENERATOR
13		DATA POSTAMBLE	SEQ-CNT	SEQ-VAL
14	LOOP	INTER SECTOR GAP	SEQ-CNT	SEQ-VAL
15	HOLD	PRE-INDEX GAP (HOLD)	INDEX	SEQ-VAL
16		DONE		

READ COMMAND

State	Mode	Function	Count	Value
0		----		
1		----		
2		----		
3	ST/RESTRT	ID SYNC BYTE	SEQ-CNT	SEQ-VAL
4		ID MARKER BYTE	SEQ-CNT	SEQ-VAL
5		ID DATA FIELD	SEQ-CNT	SEQ-VAL
6		ID ECC	SEQ-CNT	SEQ-VAL
7		ID POSTAMBLE	1	
8		SKIP STATE	1	
9		DATA SYNC BYTE	SEQ-CNT	SEQ-VAL
10		DATA MARKER BYTE	SEQ-CNT	SEQ-VAL
11		DATA FIELD	CNT*BLK	DATA TO MEMORY
12		DATA ECC	SEQ-CNT	SEQ-VAL
13		SKIP STATE	1	
14	LOOP	SKIP STATE	1	
15		----		
16		----		

READ LONG COMMAND

State	Mode	Function	Count	Value
Ø		----		
1		----		
2		----		
3	ST/RESTRT	ID SYNC BYTE	SEQ-CNT	SEQ-VAL
4		ID MARKER BYTE	SEQ-CNT	SEQ-VAL
5		ID DATA FIELD	SEQ-CNT	HEADER REGISTER
6		ID ECC	SEQ-CNT	ECC CHECK
7		SKIP STATE	1	
8		SKIP STATE	1	
9		DATA SYNC BYTE	SEQ-CNT	SEQ-VAL
1Ø		DATA MARKER BYTE	SEQ-CNT	SEQ-VAL
11		DATA FIELD	CNT*BLK	DATA TO MEMORY
12		DATA ECC	SEQ-CNT	ECC TO MEMORY
13		SKIP STATE	1	
14	LOOP	SKIP STATE	1	
15		----		
16		----		

READ SYNDROME COMMAND

State	Mode	Function	Count	Value
Ø		----		
1		----		
2		----		
3	ST/RESTRT	ID SYNC BYTE	SEQ-CNT	SEQ-VAL
4		ID MARKER BYTE	SEQ-CNT	SEQ-VAL
5		ID DATA FIELD	SEQ-CNT	HEADER REGISTER
6		ID ECC	SEQ-CNT	ECC CHECK
7		SKIP STATE	1	
8		SKIP STATE	1	
9		DATA SYNC BYTE	SEQ-CNT	SEQ-VAL
1Ø		DATA MARKER BYTE	SEQ-CNT	SEQ-VAL
11		DATA FIELD	CNT*BLK	DATA TO MEMORY
12		DATA ECC	SEQ-CNT	SYND TO MEMORY
13		SKIP STATE	1	
14	LOOP	SKIP STATE	1	
15		----		
16		----		

READ VERIFY COMMAND

State	Mode	Function	Count	Value
0		----		
1		----		
2		----		
3	ST/RESTRT	ID SYNC BYTE	SEQ-CNT	SEQ-VAL
4		ID MARKER BYTE	SEQ-CNT	SEQ-VAL
5		ID DATA FIELD	SEQ-CNT	HEADER REGISTER
6		ID ECC	SEQ-CNT	ECC CHECK
7		SKIP STATE	1	
8		SKIP STATE	1	
9		DATA SYNC BYTE	SEQ-CNT	SEQ-VAL
10		DATA MARKER BYTE	SEQ-CNT	SEQ-VAL
11		DATA FIELD	CNT*BLK	DATA FROM MEMORY
12		DATA ECC	SEQ-CNT	ECC CHECK
13		SKIP STATE	1	
14	LOOP	SKIP STATE	1	
15		----		
16		----		

READ VERIFY LONG COMMAND

State	Mode	Function	Count	Value
0		----		
1		----		
2		----		
3	ST/RESTRT	ID SYNC BYTE	SEQ-CNT	SEQ-VAL
4		ID MARKER BYTE	SEQ-CNT	SEQ-VAL
5		ID DATA FIELD	SEQ-CNT	HEADER REGISTER
6		ID ECC	SEQ-CNT	ECC CHECK
7		SKIP STATE	1	
8		SKIP STATE	1	
9		DATA SYNC BYTE	SEQ-CNT	SEQ-VAL
10		DATA MARKER BYTE	SEQ-CNT	SEQ-VAL
11		DATA FIELD	CNT*BLK	DATA FROM MEMORY
12		DATA ECC	SEQ-CNT	DATA FROM MEMORY
13		SKIP STATE	1	
14	LOOP	SKIP STATE	1	
15		----		
16		----		

WRITE COMMAND

State	Mode	Function	Count	Value
0		----		
1		----		
2		----		
3	ST/RESTRT	ID SYNC BYTE	SEQ-CNT	SEQ-VAL
4		ID MARKER BYTE	SEQ-CNT	SEQ-VAL
5		ID DATA FIELD	SEQ-CNT	HEADER REGISTER
6		ID ECC	SEQ-CNT	ECC CHECK
7		ID POSTAMBLE	SEQ-CNT	
8		DATA PREAMBLE	SEQ-CNT	SEQ-VAL
9		DATA SYNC BYTE	SEQ-CNT	SEQ-VAL
10		DATA MARKER BYTE	SEQ-CNT	SEQ-VAL
11		DATA FIELD	CNT*BLK	DATA FROM MEMORY
12		DATA ECC	SEQ-CNT	ECC CHECK
13		DATA POSTAMBLE	SEQ-CNT	SEQ-VAL
14	LOOP	SKIP STATE	1	
15		----		
16		----		

WRITE LONG COMMAND

State	Mode	Function	Count	Value
Ø		----		
1		----		
2		----		
3	ST/RESTRT	ID SYNC BYTE	SEQ-CNT	SEQ-VAL
4		ID MARKER BYTE	SEQ-CNT	SEQ-VAL
5		ID DATA FIELD	SEQ-CNT	HEADER REGISTER
6		ID ECC	SEQ-CNT	ECC CHECK
7		ID POSTAMBLE	SEQ-CNT	
8		DATA PREAMBLE	SEQ-CNT	SEQ-VAL
9		DATA SYNC BYTE	SEQ-CNT	SEQ-VAL
1Ø		DATA MARKER BYTE	SEQ-CNT	SEQ-VAL
11		DATA FIELD	CNT*BLK	DATA FROM MEMORY
12		DATA ECC	SEQ-CNT	DATA FROM MEMORY
13		DATA POSTAMBLE	SEQ-CNT	SEQ-VAL
14	LOOP	SKIP STATE	1	
15		----		
16		----		

APPENDIX C

SEQUENCER STATE FLOW CHARTS FOR HARD-SECTORED, ESDI-SECTORED, AND ESDI ADDRESS MARK FORMATS

	DMA HARD SECTORED		ESDI SECTOR		ESDI ADDRESS MARK
	------		------	START	POST INDEX GAP
ST/LP	POST INDEX/SECTOR GAP	ST-LP	POST INDEX/SECTOR GAP	LOOP-IN	A-M ENABLE
	ID PREAMBLE		ID PREAMBLE		ID PREAMBLE
	ID SYNC BYTE		DECODE SYNC		DECODE SYNC
	ID MARKER BYTE		SYNC BYTE		SYNC BYTE
	ID DATA FIELD		ID DATA FIELD		ID DATA FIELD
	ID ECC		ID ECC		ID ECC
	ID POSTAMBLE		ID POSTAMBLE		ID POSTAMBLE
	DATA PREAMBLE		DATA PREAMBLE		DATA PREAMBLE
	DATA SYNC BYTE		DECODE SYNC		DECODE SYNC
	DATA MARKER BYTE		SYNC BYTE		SYNC BYTE
	DATA FIELD		DATA FIELD		DATA FIELD
	DATA ECC		DATA ECC		DATA ECC
	DATA POSTAMBLE		DATA POSTAMBLE		DATA POSTAMBLE
	INTER SECTOR GAP		MORE POSTAMBLE	JUMP	INTER SECTOR GAP
JUMP	PRE-IND/SEC GAP (HOLD)	JUMP	PRE-IND/SEC GAP (HOLD)		PRE-INDEX GAP (HOLD)
	DONE		DONE		DONE

	DMA HARD SECTORED		ESDI SECTOR		ESDI ADDRESS MARK
	------		------		------
	------		------		------
	------		------		------
ST/LP	ID SYNC BYTE	ST/LP	SECTOR TO RG DELAY	ST/LP	A-M TO RG DELAY
	ID MARKER BYTE		SYNC BYTE		SYNC BYTE
	ID DATA FIELD		ID DATA FIELD		ID DATA FIELD
	ID ECC		ID ECC		ID ECC
	ID POSTAMBLE		ID POSTAMBLE		ID POSTAMBLE
	SKIP STATE		SKIP STATE		SKIP STATE
	DATA SYNC BYTE		SKIP STATE		SKIP STATE
	DATA MARKER BYTE		SYNC BYTE		SYNC BYTE
	DATA FIELD		DATA FIELD		DATA FIELD
	DATA ECC		DATA ECC		DATA ECC
	SKIP STATE		SKIP STATE		SKIP STATE
JUMP	SKIP STATE	JUMP	SKIP STATE	JUMP	SKIP STATE
	------		------		------
	------		------		------

	DMA HARD SECTORED		ESDI SECTOR		ESDI ADDRESS MARK
	------		------		------
	------		------		------
	------		------		------
ST/LP	ID SYNC BYTE	ST/LP	SECTOR TO RG DELAY	ST/LP	A-M TO RG DELAY
	ID MARKER BYTE		SYNC BYTE		SYNC BYTE
	ID DATA FIELD		ID DATA FIELD		ID DATA FIELD
	ID ECC		ID ECC		ID ECC
	ID POSTAMBLE		ID POSTAMBLE		ID POSTAMBLE
	DATA PREAMBLE		DATA PREAMBLE		DATA PREAMBLE
	DATA SYNC BYTE		DECODE SYNC		DECODE SYNC
	DATA MARKER BYTE		SYNC BYTE		SYNC BYTE
	DATA FIELD		DATA FIELD		DATA FIELD
	DATA ECC		DATA ECC		DATA ECC
	DATA POSTAMBLE		DATA POSTAMBLE		DATA POSTAMBLE
JUMP	SKIP STATE	JUMP	SKIP STATE	JUMP	SKIP STATE
	------		------		------
	------		------		------

APPENDIX D

DATA TRANSFER PARAMETER REGISTER SUMMARY

WRITE REGISTER 0: COMMAND

Bits: 7 6 5 4 3 2 1 0

- Bit 0: 1 = Read
- Bit 1: 1 = Write
- Bit 2: 0 = Normal; 1 = Format I/D Data
- Bit 3: 0 = Normal; 1 = Long (ECC to/from Buffer)
- Bit 4: 1 = Syndrome to Buffer
- Bit 5: 0 = Abort on Flag Non-Zero; 1 = Ignore Flag Condition
- Bit 6: 1 = Verify (Buffer to Disk Data)
- Bit 7: 1 = No Data Transfer

WRITE REGISTER 1: SEQUENCER LOOP COUNT

Bits: 7 6 5 4 3 2 1 0

- Bits 7-0: Number of Sectors (N = 0)

WRITE REGISTER 2: INDEX TIME-OUT

Bits: 7 6 5 4 3 2 1 0 (bits 7-4: X X X X)

- Bits 3-0: Number of Revolutions Before Time-Out

WRITE REGISTER 3: SUB-BLOCK COUNT

Bits: 7 6 5 4 3 2 1 0

- Bits 7-0: Number of Sub-Blocks per Sector

WRITE REGISTER 4: CYLINDER HIGH

Bits: 7 6 5 4 3 2 1 0

- Bits 7-0: 00-FF

WRITE REGISTER 5: CYLINDER LOW

Bits: 7 6 5 4 3 2 1 0

- Bits 7-0: 00-FF

WRITE REGISTER 6: HEAD ADDRESS

Bits: 7 6 5 4 3 2 1 0

- Bits 7-0: 00-FF

WRITE REGISTER 7: SECTOR NUMBER

Bits: 7 6 5 4 3 2 1 0

- Bits 7-0: 00-FF

WRITE REGISTER 8: MICRO TO MEMORY

Bits: 7 6 5 4 3 2 1 0

- Bits 7-0: 00-FF

WRITE REGISTER 9: SEQUENCER START/RE-START

Bits: 7 6 5 4 3 2 1 0

- Bits 3-0: Start State X0-XF
- Bits 7-4: Re-Start State 0X-FX

WRITE REGISTER 10: SEQUENCER LOOP STATE

Bits: 7 6 5 4 3 2 1 0 (bits 7-4: X X X X)

- Bits 3-0: Loop State X0-XF

WRITE REGISTER 11: BIT RING START COUNT

Bits: 7 6 5 4 3 2 1 0 (bits 7-4: X X X X)

- Bits 3-0: Start Bit 0X-XF

WRITE REGISTER 12: ECC CONTROL

Bits: 7 6 5 4 3 2 1 0

- Bit 0: 0 = ECC Clear on Init; 1 = ECC Preset on Init
- Bit 1: 0 = Data to ECC; 1 = ~Data to ECC
- Bit 2: 0 = ECC Feedback; 1 = ~ECC Feedback
- Bit 3: 0 = ECC Data Out; 1 = ~ECC Data Out
- Bit 4: 0 = ECC Check; 1 = ~ECC Check
- Bit 5: 0 = Xfer Disable; 1 = Xfer Enable
- Bit 6: 0 = I-D = CRC
- Bit 7: 1 = Enable Data Field Sync Time-Out

WRITE REGISTER 13: CONFIGURATION CONTROL

Bits: 7 6 5 4 3 2 1 0

- Bit 0: 0 = Soft Sectored; 1 = Hard Sectored
- Bit 1: 0 = 1 Field Sync; 1 = 2 Field Sync
- Bit 2: 0 = Head/Flag Byte; 1 = Flag Byte
- Bit 3: 0 = Not ESDI Config; 1 = ESDI Config
- Bit 4: 0 = Internal Sync Detect; 1 = External Sync Detect
- Bit 5: 0 = Disable Write Gate Edge; 1 = Enable Write Gate Edge
- Bit 6: 0 = Interrupt Active Low; 1 = Interrupt Active High
- Bit 7: 0 = Interrupt Disabled; 1 = Interrupt Enabled

WRITE REGISTER 14: SEQ COUNT REG @ SEQ START

Bits: 7 6 5 4 3 2 1 0

- Bits 7-0: 00-FF

WRITE REGISTER 15: SEQ VALUE REG @ SEQ START

Bits: 7 6 5 4 3 2 1 0

- Bits 7-0: 00-FF

WRITE REGISTERS 16-23: POLYNOMIAL GENERATOR

Bits: 7 6 5 4 3 2 1 0

- Bits 7-0: 00-FF

WRITE REGISTER 24: EXTERNAL REGISTER 0 STROBE

Bits: 7 6 5 4 3 2 1 0

- Bits 7-0: 00-FF

WRITE REGISTER 25: EXTERNAL REGISTER 1 STROBE

Bits: 7 6 5 4 3 2 1 0

- Bits 7-0: 00-FF

WRITE REGISTER 28-31: EXTERNAL GROUP STROBE

Bits: 7 6 5 4 3 2 1 0

- Bits 7-0: 00-FF

READ REGISTER 0: STATUS

7 6 5 4 3 2 1 0

- 1 = Busy
- 1 = Data ECC Error
- 1 = Data Sync + Marker Not Found
- 1 = Data Verify Error
- 1 = ID ECC Error
- 1 = ID Sync + Marker Not Found
- 1 = ID Data No Compare
- 1 = Extended Status Non-Zero

READ REGISTER 1: EXTENDED STATUS

7 6 5 4 3 2 1 0

- 1 = Disk Data Over/ Under Run
- 1 = Micro Mem Over/ Under Run
- 1 = Index Time-Out
- 1 = Flag Byte/Bit Non-Zero
- 1 = Data Field Sync Time-Out
- Not Used
- Sector
- Index

READ REGISTER 2: RETRY COUNT/STATE ADDRESS

7 6 5 4 3 2 1 0

- X0-XF = Retry Count
- 0X-FX = Sequencer State Address

READ REGISTER 3: FLAG BYTE

7 6 5 4 3 2 1 0

- 00-FF = Flag Byte (Header Byte 4)

READ REGISTER 4: CYLINDER HIGH

7 6 5 4 3 2 1 0

- 00-FF = Cylinder High (Header Byte 4)

READ REGISTER 5: CYLINDER LOW

7 6 5 4 3 2 1 0

- 00-FF = Cylinder Low (Header Byte 1)

READ REGISTER 6: HEAD/FLAG

7 6 5 4 3 2 1 0

- 00-FF = Head Address (Header Byte 2)
- Flag

READ REGISTER 7: SECTOR

7 6 5 4 3 2 1 0

- 00-FF = Sector (Header Byte 3)

READ REGISTER 8: MEMORY TO MICRO

7 6 5 4 3 2 1 0

- 00-FF = Memory to Micro

READ REGISTER 9: SEQUENCER LOOP COUNT

7 6 5 4 3 2 1 0

- Number of Sectors (N = N)

READ REGISTER 14: SEQ COUNT REG @ SEQ START

7 6 5 4 3 2 1 0

- 00-FF

READ REGISTER 15: SEQ VALUE REG @ SEQ START

7 6 5 4 3 2 1 0

- 00-FF

READ REGISTER 24: EXTERNAL STATUS 0

7 6 5 4 3 2 1 0

- 00-FF = External Status 0

READ REGISTER 25: EXTERNAL STATUS 1

7 6 5 4 3 2 1 0

- 00-FF = External Status 1

READ REGISTER 27: MICRO-DMA MEMORY TO EXTERNAL GROUP

7 6 5 4 3 2 1 0

- 00-FF

READ REGISTERS 28-31: EXTERNAL GROUP STROBE

7 6 5 4 3 2 1 0

- 00-FF

9-28-84

To: All Engineers, L Ebisu, D Gunderson, and B Murray

From: R Kellert

Re: **OMTI 5050 R/W Sequencer**

The following is a brief list of answers to questions that have arisen concerning the 5050 as well as a few errors in documentation that have been found. For more complete information please ask Somebody. He will be glad to help.

1) The 8 bit parity generator circuit on the memory data bus is in fact an even parity generator and not an odd parity generator as the spec claims. An external invereter is required to obtain odd parity.

2) Bit 6 of the ECC Control register, (WR12), must be set to a 1 to obtain CRC-CCITT on the ID, not a 0 as in the spec.

3) WRGATE is tied explicitly to index for format purposes. For an imbedded servo drive that does not inhibit WRGATE internally there is a F/W fix possible. Disable index from the drive during format and poll index in F/W. Now count bytes(words) past the servo information. A write to WR26 synthesizes an index hence your resolution is now tied to the Z8. Any such drive is likely to lose servo anyway so hang it up.

4) Values of 0 in the sequencer ram do not force a skip state, they are equivalent to a value of 256 decimal. For example in format, data postamble may not be skipped, but a number (n) should be entered, and the next state is programmed as 1 or n less whichever applies.

5) The ECC hardware is not intended to assist in any way with any part of a correction algorithim. By inspection, the ECC register is clocked only by RD/REF_CLK. You may not do preshift or syndrome location unless an external clock mux is used which is not recommended.

6) One may have only a four byte ID with an additional fifth flag byte where the sync character is not considered part of this length and any trailing ID information is ignored. The fifth flag byte is always compared for zero unless disabled. The fourth byte or ID register is the only location capable of auto-increment hence, if the Sector address is not located there, then multi sector transfers will be somewhat difficult.

5050

PROGRAMMABLE

DATA SEQUENCER

Timing Diagram
Labels

5050

Programmable Data Sequencer

AØ, A1 — SEQ AØ (pin 26), SEQ A1 (pin 25)

WRT* — -SEQ WRT (pin 21)

DØ, D1 — SEQ DØ (pin 27), SEQ D1 (pin 28)

INT* — INTERRUPT (pin 60)

NRZ IN — (pin 17)

WR GT — WRT GATE (pin 12)

WR CK — WRT CLK (pin 15)

MFM OUT — pin 15 of VCO chip

AS* — ALE (pin 68) [address strobe]

DS* — -IORD (pin 66) [data strobe]

WR* — -IOWR (pin 67)

ENPRECOMP — pin 11 of VCO chip

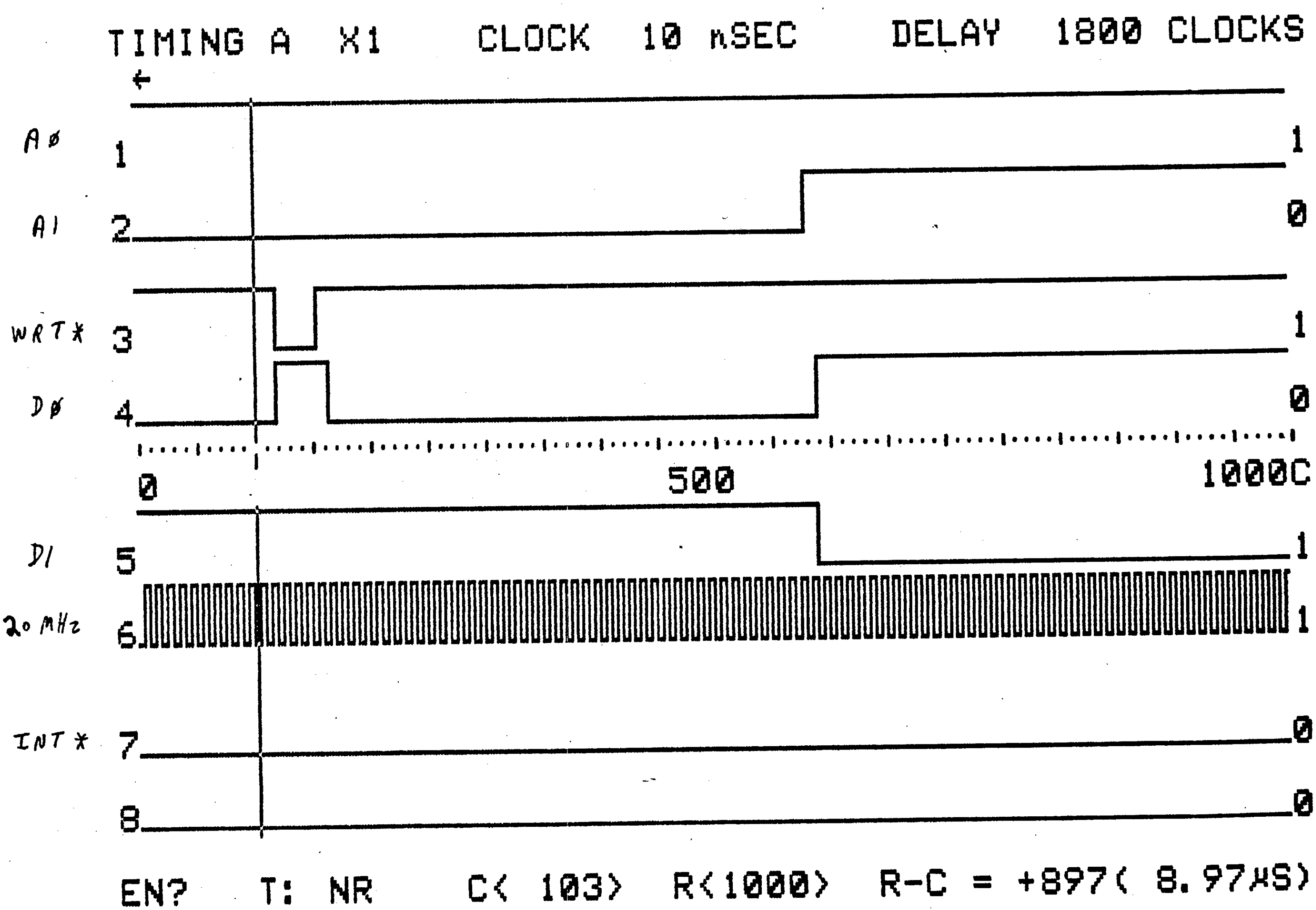
DM* — IO/MEM (pin 65)

INSTØ — pin 48

WRLTØ — pin 50

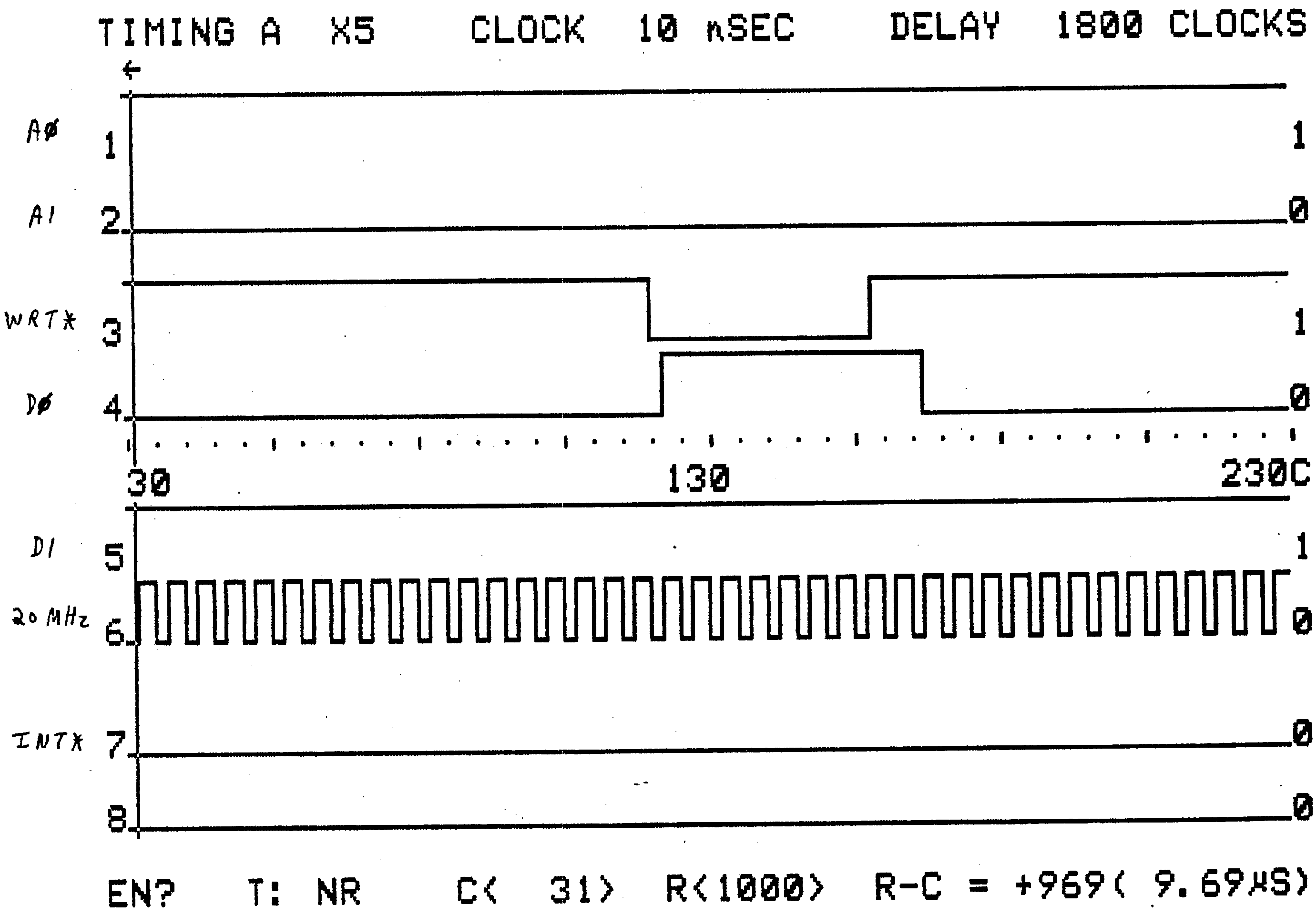
5050 Sequencer Chip Timing

Sequencer RAM Write / Read



5050 Sequencer Chip Timing

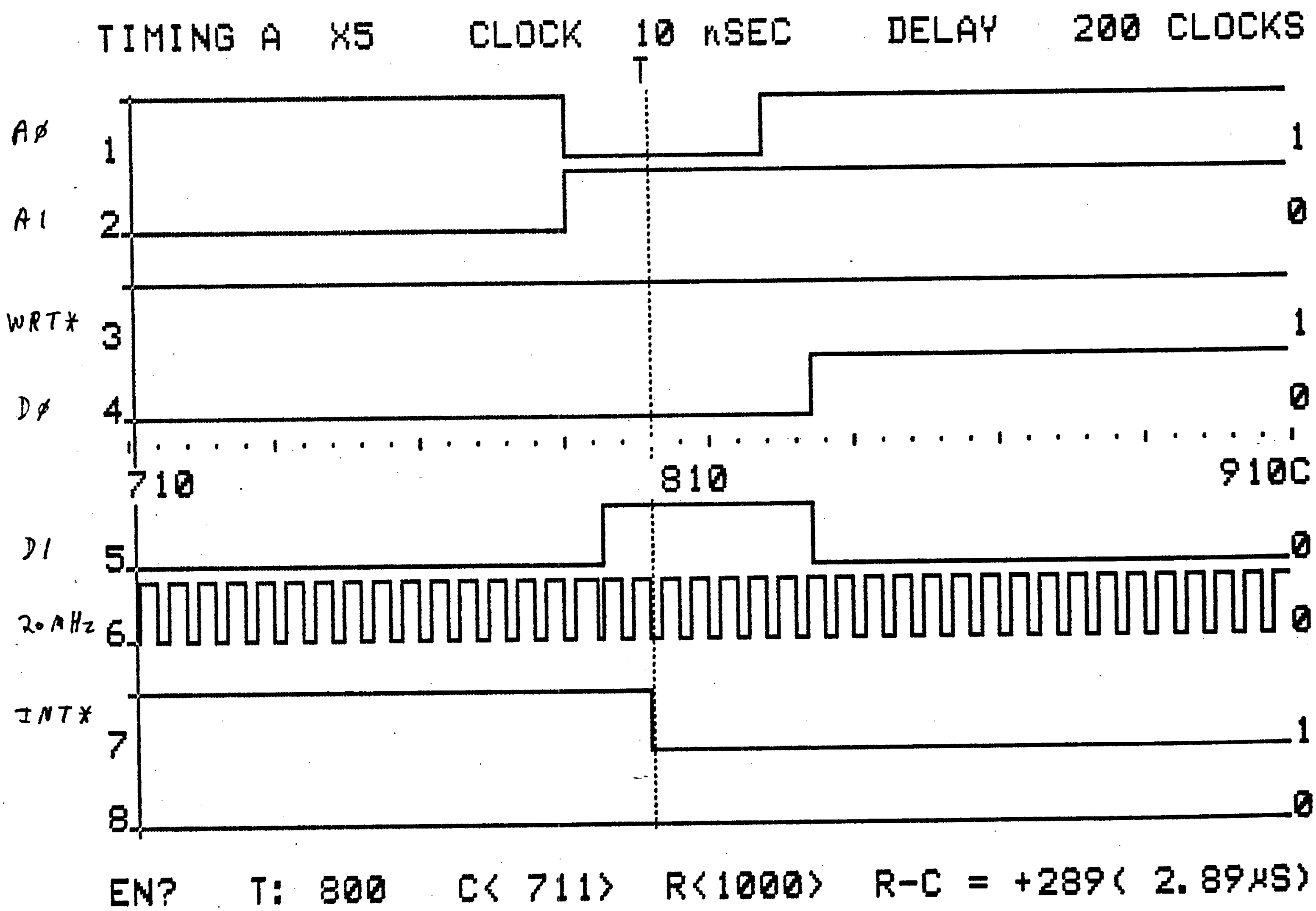
Sequencer RAM Write
Data Set-up and Hold Times



5050 Sequencer Chip Timing

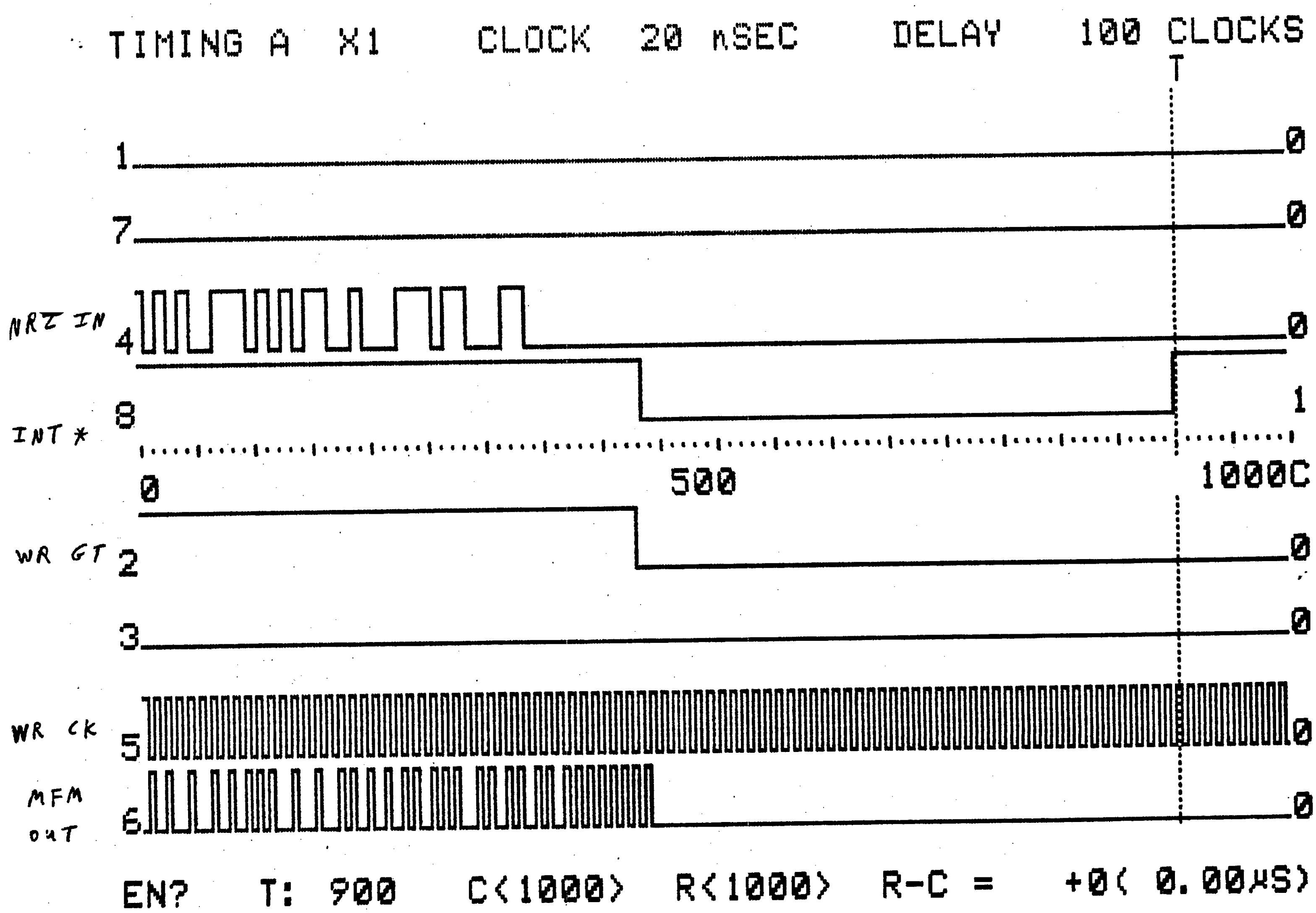
Sequencer RAM Read

Read Access Timing



5050 Sequencer Chip Timing

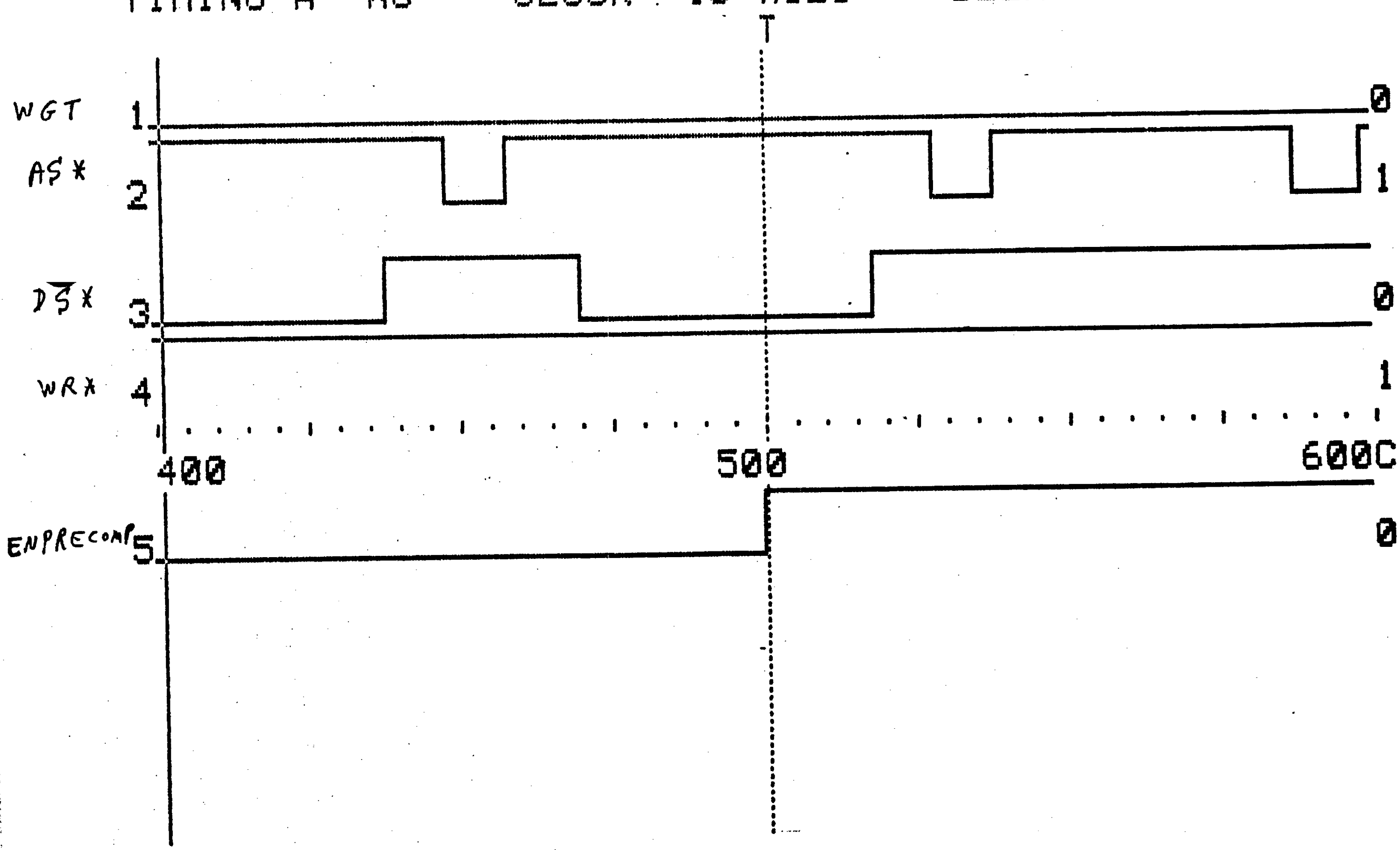
Write Data
Sequencer Completion
Timing



5050 Sequencer Chip Timing

Enable Precompensation Timing

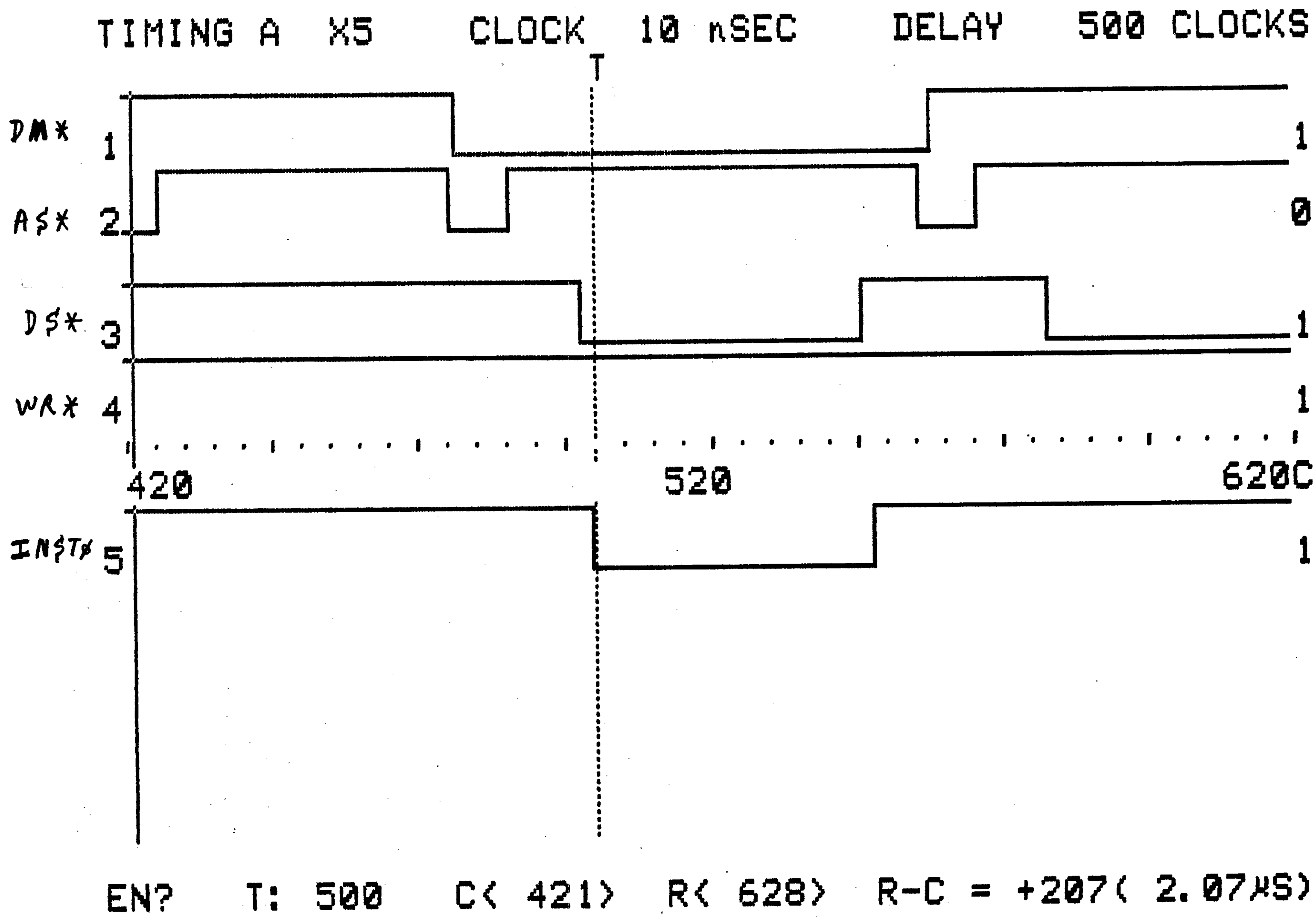
TIMING A X5 CLOCK 10 nSEC DELAY 500 CLOCKS



EN? T: 500 C(401) R(628) R-C = +227(2.27µS)

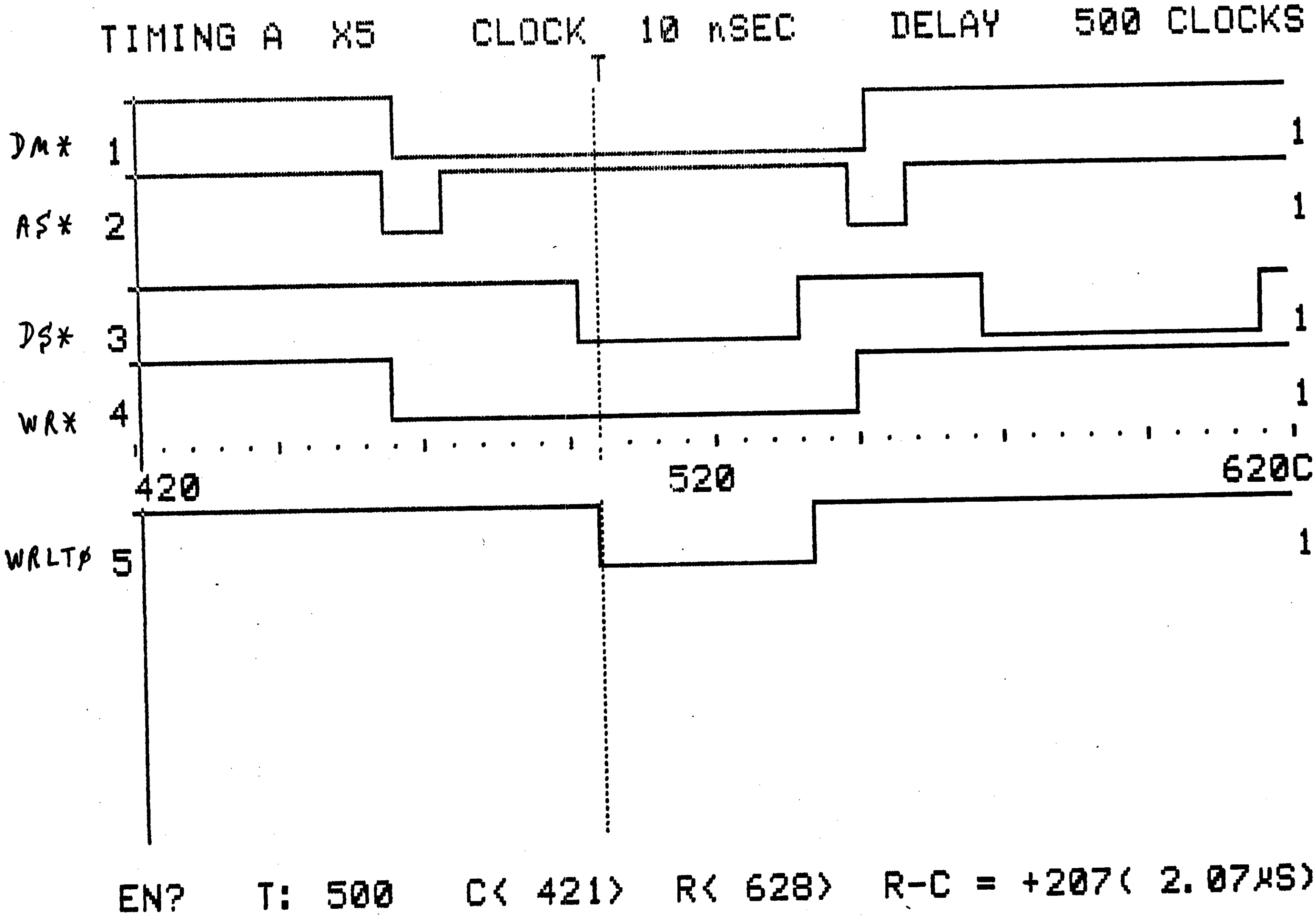
5050 Sequencer Chip Timing

Input Status Strobe



5050 Sequencer Chip Timing

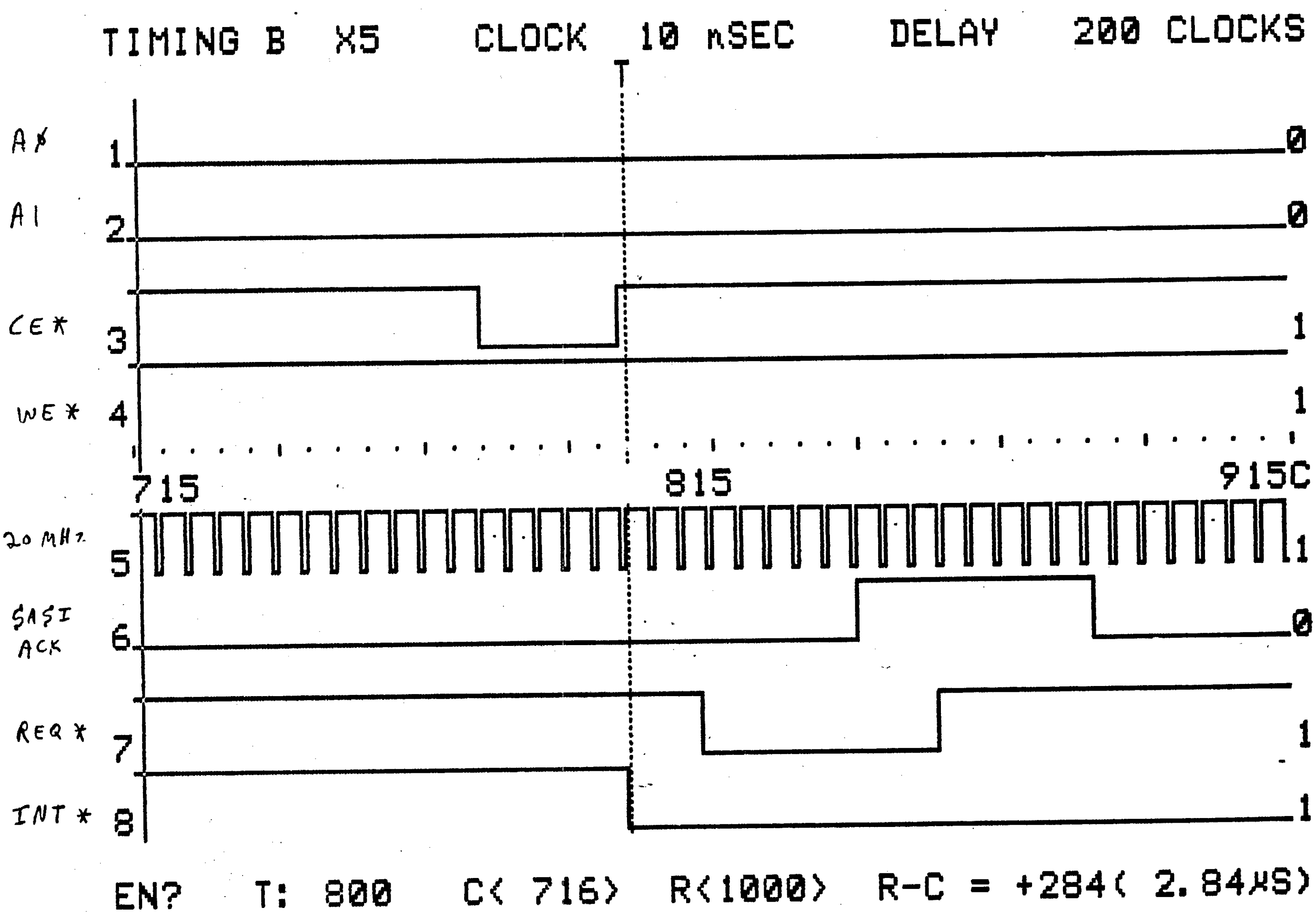
Write Latch Strobe



5060 DMA Chip Timing

Buffer Memory Read / Completion

SASI Bus / Sector Buffer Timing



NOVEMBER 03 1983

* HIGH PERFORMANCE FOUR CHANNEL MEMORY CONTROLLER

* FOUR INDEPENDENT DMA CHANNELS
* TRANSFER RATE UP TO 5 M-BYTES/SECOND
* ENABLE / DISABLE CONTROL OF REQUESTS
* INDEPENDENT POLARITY CONTROL OF REQ / ACK
* INDEPENDENT CONTROL OF CHANNEL END INTERRUPT
* PROGRAMABLE MEMORY CYCLE (2 TO 5 CLOCK CYCLES)
* AUTO ADDRESS INCREMENT
* AUTO WORD COUNT DECREMENT
* PROGRAMABLE CHANNEL 1 QIC II XFER / ACK PROTOCOL
* PROGRAMABLE CHANNEL 2 SASI REQ / ACK PROTOCOL
* 68 PIN PLASTIC LEADLESS CHIP CARRIER
* INDEPENDENT AUTO-REINITALIZATION OF WORD COUNT FOR ALL CHANNELS
* NO REAL TIME INTERVENTION

```
GROUND         ----------------------------+
MEM A-8        -------------------------+  !  +------------------------ MEM A-7
MEM A-9        ----------------------+  !  !  !  +--------------------- MEM A-6
MEM A-10       -------------------+  !  !  !  !  !  +------------------ MEM A-5
MEM A-11       ----------------+  !  !  !  !  !  !  !  +--------------- MEM A-4
MEM A-12       -------------+  !  !  !  !  !  !  !  !  !  +------------ MEM A-3
MEM A-13       ----------+  !  !  !  !  !  !  !  !  !  !  !  +--------- MEM A-2
MEM A-14       -------+  !  !  !  !  !  !  !  !  !  !  !  !  !  +------ MEM A-1
MEM A-15       ----+  !  !  !  !  !  !  !  !  !  !  !  !  !  !  !  +--- MEM A-0
               +------------------------------------------------------+
               !  43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27  !
               !                                                      !
-MEMWRT        !  44                                              26  ! REQ-0
               !                                                      !
-MEMCE         !  45                                              25  ! ACK-0
               !                                                      !
-CH2OUTCLK     !  46                                              24  ! REQ-1
               !                                                      !
-CH2INEN       !  47                                              23  ! ACK-1
               !                                                      !
CH2RDMEM       !  48                                              22  ! REQ-2
               !                                                      !
-GRPRD         !  49                                              21  ! ACK-2
               !                                                      !
-GRPWRT        !  50                   O M T I                    20  ! REQ-3
               !                                                      !
CLOCK          !  51                   F O U R                    19  ! ACK-3
               !                                                      !
VCC            !  52                C H A N N E L                 18  ! VCC
               !                                                      !
-INST0         !  53                 M E M O R Y                  17  ! MICRO A-0
               !                                                      !
-INST1         !  54             C O N T R O L L E R              16  ! MICRO A-1
               !                                                      !
-WRLT0         !  55                                              15  ! MICRO A-2
               !                                                      !
-WRLT1         !  56                                              14  ! MICRO A-3
               !                                                      !
-CH1OUTCLK     !  57                                              13  ! MICRO A-4
               !                                                      !
CH1INEN        !  58                                              12  ! MICRO A-5
               !                                                      !
-ROMCE         !  59                                              11  ! MICRO A-6
               !                                                      !
INTERRUPT      !  60                                              10  ! MICRO A-7
               !                                                      !
               !  61 62 63 64 65 66 67 68  1  2  3  4  5  6  7  8  9  !
               +------------------------------------------------------+
-XOR A-7       ----+  !  !  !  !  !  !  !  !  !  !  !  !  !  !  !  +--- A/D-7
-XOR A-6       -------+  !  !  !  !  !  !  !  !  !  !  !  !  !  +------ A/D-6
-XOR A-5       ----------+  !  !  !  !  !  !  !  !  !  !  !  +--------- A/D-5
CONFIG         -------------+  !  !  !  !  !  !  !  !  !  +------------ A/D-4
IO/-MEM        ----------------+  !  !  !  !  !  !  !  +--------------- A/D-3
-IORD          -------------------+  !  !  !  !  !  +------------------ A/D-2
-IOWR          ----------------------+  !  !  !  +--------------------- A/D-1
ALE            -------------------------+  !  +------------------------ A/D-0
GROUND         ----------------------------+
```

SYMBOL	TYPE	NAME AND FUNCTION
A/D 0-7	I/O	MULTIPLEXED ADDRESS / DATA BUS: 3-STATE ADDRESS / DATA LINES THAT INTERFACE WITH THE CPU LOWER 8 BIT ADDRESS / DATA BUS. THE ADDRESSES ARE LATCHED INTO THE ADDRESS REGISTER ON THE FALLING EDGE OF ALE. THE 8 BIT DATA IS EITHER WRITTEN INTO OR READ FROM THE MEMORY CONTROLLER REGISTERS DEPENDING ON -IOWR OR -IORD INPUT CONTROL LINES, IF THE ADDRESS IN WITHIN THE RANGE OF THE INTERNAL CHIP SELECT.
ALE	I	ADDRESS LATCH ENABLE: THIS INPUT STROBE IS FOR STORING ADDRESS 0-7 INTO THE ADDRESS REGISTER ON THE FALLING EDGE OF ALE FOR INTERNAL CHIP AND REGISTER SELECT.
-IOWR	I	I/O WRITE: THIS ACTIVE LOW INPUT STROBE IS USED BY THE CPU TO LOAD INFORMATION IN THE MEMORY CONT-ROLLER WITH THE PROPER ADDRESS FOR CHIP AND REGISTER SELECTION.
-IORD	I	I/O READ: THIS ACTIVE LOW INPUT STROBE IS USED BY THE CPU TO READ STATUS INFORMATION FROM THE MEMORY CONTROLLER WITH THE PROPER ADDRESS FOR CHIP AND REGISTER SELECTION.
REQ 0-3	I	DMA MEMORY REQUEST 0-3: THE DMA REQUEST LINES ARE INDIVIDUALLY ASYNC-HRONOUS CHANNEL REQUEST INPUTS BY THE PERIPH-ERAL TO OBTAIN DMA SERVICE. THE PRIORITY IS FIXED WITH REQ-0 HAVING THE HIGHEST AND REQ-3 HAVING THE LOWEST PRIORITY. POLARITY OF ALL REQUEST INPUTS HAVE INDEPENDENT CONTROL. IF CHANNEL 1 IS CONFIGURED FOR THE QIC II PROTOCALL, REQ 1 IS THEN THE QIC II ACK SIGNAL. IF CHANNEL 2 IS CONFIGURED FOR THE SASI PROTOCALL, REQ 2 IS CONFIGURED FOR THE SASI ACK SIGNAL.

SYMBOL	TYPE	NAME AND FUNCTION
ACK 0-3	O	DMA MEMORY ACKNOWLEDGE 0-3: THE DMA ACKNOWLEDGE LINES ARE TO NOTIFY THE INDIVIDUAL REQUESTING PERIPHERAL WHEN IT HAS BEEN GRANTED A MEMORY CYCLE. POLARITY OF ALL ACK OUTPUT LINES HAVE INDEPENDENT CONTROL. IF CHANNEL 1 IS CONFIGURED FOR THE QIC II PROTOCALL, ACK 1 IS THEN THE QIC II XFER SIGNAL. IF CHANNEL 2 IS CONFIGURED FOR THE SASI PROTOCALL, ACK 2 IS THEN THE SASI REQ SIGNAL.
A 0-15	O	ADDRESS 0-15: THE 16 BIT ADDRESS LINES ARE FOR INTERFACING THE ACKNOWLEDGED ADDRESS COUNTERS VALUE TO THE MEMORY ARRAY.
-MEMCE	O	MEMORY CHIP ENABLE: THIS ACTIVE LOW STROBE IS ACTIVE WHEN ANY OF THE ACK 0-3 LINES ARE ACTIVE, USED TO ENABLE THE MEMORY ADDRESSED BY A 0-15.
-MEMWRT	O	MEMORY WRITE: THIS ACTIVE LOW OUTPUT THEN -MEMCE IS ACTIVE IS FOR WRITING THE RAM ARRAY. MEMCE TRUE WITH MEMWRT FALSE IS A MEMORY READ CYCLE.
CLOCK	I	CLOCK: THIS INPUT IS USED FOR CONTROLLING THE INTERNAL ARBITERATION OF ALL REQ TO ACK. CLOCK IS ALSO USED IN THE PROGRAMABLE MEMORY TIMING AND THE SASI AND QIC II PROTOCALL SEQUENCERS.
-CHOUTCK	O	CHANNEL 1-2 OUT CLOCK: THIS OUTPUT IS USED TO SAVE DATA FROM THE MEMORY READ CYCLE TO THE REGISTER OF EITHER THE QIC II OR SASI HOST INTERFACE.

SYMBOL	TYPE	NAME AND FUNCTION
-CHINEN	O	CHANNEL 1-2 INPUT ENABLE: THIS OUTPUT IS USED TO ENABLE DATA FOR THE MEMORY WRITE CYCLE FROM EITHER THE QIC II OR THE SASI HOST BUS BUFFER.
CH2RDMEM	O	CHANNEL 2 READ MEMORY: THIS OUTPUT IS USED FOR THE SASI I/O INTERFACE SIGNAL. THIS IS A DIRECT OUTPUT OF THE CHANNEL CONTROL REGISTER.
MICA 0-7	O	MICRO ADDRESS 0 - 7: THIS 8 BIT ADDRESS BUS IS THE MICROS ADDRESS LATCHED FROM THE MICRO A/D BUS AT ALE TIME. THIS IS INTENDED TO BE USED WITH THE MICRO'S EXTERNAL MEMORY AND PARIPHERIALS.
IO/-MEM	I	IO/-MEMORY: THIS INTERNALLY PULLED-UP INPUT IS USED FOR AN ACTIVE HIGH CHIP ENABLE. IN AN 8085 SYSTEM THIS LINE IS CONNECTED TO THE SAME MICRO LINE OR IN ANY OTHER MICRO MAY BE LEFT OPEN.
-XOR 7-5	I	EXCLUSIVE OR ADDRESS 7 - 5: THESE INTERNALLY PULLED-UP INPUTS ARE USED FOR THE INTERNAL CHIP SELECT. THEY CONTROL THE POLARITY OF THE CORROSPONDING ADDRESS LINE. IF ANOTHER GROUP CHIP SELECT IF REQUIRED, GROUND THE APPROPRIATE LINE.
CONFIG	I	CONFIG: THIS INTERNALY PULLED-UP LINE IS USED TO SELECT THE MICRO STROBE INPUTS. WHEN THIS INPUT IS GROUNDED THE CHIP IS CONFIGURED FOR AN 8085 / 8051 TYPE MICRO. WHEN LEFT OPEN THE CHIP IS CONFIGURED AS A Z-8 TYPE MICRO WITH THE FOLLOWING INTERFACE SIGNAL CHANGES, -IORD = -DATA STROBE, -IOWR = R/-W, ALE = -AS, IO/MEM = -DM.

SYMBOL	TYPE	NAME AND FUNCTION
-INST0-1	O	IN STATUS 0 / 1: THESE OUTPUT STROBES ARE INTERALLY DECODED I/O READ STROBES INTENDED TO BE USED BY THE MICRO TO READ DEVICE STATUS THROUGH AN EXTERNAL BUFFER TO THE MICRO DATA BUS.
-WRLT0-1	O	WRITE LATCH 0 / 1: THESE OUTPUT STROBES ARE INTERALLY DECODED I/O WRITE STROBES INTENDED TO BE USED BY THE MICRO TO WRITE DEVICE CONTROL THROUGH AN EXT-RNAL LATCH FROM THE MICRO DATA BUS.
INTERRUPT	O	INTERRUPT: THIS OUTPUT, IS SET TO THE POLARITY CONFIG-URED IN THE MEMORY CONTROL REGISTER WHEN A CHANNEL WITH THE INTERUPT ENABLED HAS A WORD COUNT OF ZERO WITH THE AUTO DISABLE, ENABLED. THE INTERUPT IS RESET WHEN THE STATUS IS READ.
-ROMCE	O	ROM CHIP ENABLE: THIS OUTPUT IS TRUE WHEN RD IS TRUE AND WRITE WITH SELECT IS FALSE.

ADDRESS REGISTER AND CONTROL

7	6	5	4	3	2	1	0	-IOWR	-IORD	REGISTER FUNCTION
S	S	S	0	0	0	0	0	0	1	LOAD CHANNEL 0 ADDRESS 0-7
S	S	S	0	0	0	0	1	0	1	LOAD CHANNEL 0 ADDRESS 8-15
S	S	S	0	0	0	1	0	0	1	LOAD CHANNEL 0 WORD CT 0-7
S	S	S	0	0	0	1	1	0	1	LOAD CHANNEL 0 WORD CT 8-15
S	S	S	0	0	1	0	0	0	1	LOAD CHANNEL 1 ADDRESS 0-7
S	S	S	0	0	1	0	1	0	1	LOAD CHANNEL 1 ADDRESS 8-15
S	S	S	0	0	1	1	0	0	1	LOAD CHANNEL 1 WORD CT 0-7
S	S	S	0	0	1	1	1	0	1	LOAD CHANNEL 1 WORD CT 8-15
S	S	S	0	1	0	0	0	0	1	LOAD CHANNEL 2 ADDRESS 0-7
S	S	S	0	1	0	0	1	0	1	LOAD CHANNEL 2 ADDRESS 8-15
S	S	S	0	1	0	1	0	0	1	LOAD CHANNEL 2 WORD CT 0-7
S	S	S	0	1	0	1	1	0	1	LOAD CHANNEL 2 WORD CT 8-15
S	S	S	0	1	1	0	0	0	1	LOAD CHANNEL 3 ADDRESS 0-7
S	S	S	0	1	1	0	1	0	1	LOAD CHANNEL 3 ADDRESS 8-15
S	S	S	0	1	1	1	0	0	1	LOAD CHANNEL 3 WORD CT 0-7
S	S	S	0	1	1	1	1	0	1	LOAD CHANNEL 3 WORD CT 8-15

S S S = INTERNAL CHIP SELECT

ADDRESS REGISTER AND CONTROL

7	6	5	4	3	2	1	0	-IOWR	-IORD	REGISTER FUNCTION
S	S	S	1	0	0	0	0	0	1	LOAD CHANNEL 0 CONTROL
S	S	S	1	0	0	0	1	0	1	LOAD CHANNEL 1 CONTROL
S	S	S	1	0	0	1	0	0	1	LOAD CHANNEL 2 CONTROL
S	S	S	1	0	0	1	1	0	1	LOAD CHANNEL 3 CONTROL
S	S	S	1	0	1	0	0	0	1	LOAD MEMORY CYCLE TIMING
S	S	S	1	1	0	0	0	0	1	EXTERNAL OUT STROBE 0
S	S	S	1	1	0	0	1	0	1	EXTERNAL OUT STROBE 1
S	S	S	1	1	1	X	X	0	1	EXTERNAL OUT GROUP STROBE
S	S	S	0	0	0	0	0	1	0	CHANNEL STATUS
S	S	S	1	1	0	0	0	1	0	EXTERNAL IN STROBE 0
S	S	S	1	1	0	0	1	1	0	EXTERNAL IN STROBE 1
S	S	S	1	1	1	X	X	1	0	EXTERNAL IN GROUP STROBE

S S S = INTERNAL CHIP SELECT

CHANNEL CONTROL

WRITE DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
! ! ! ! ! ! ! +--------    0 = CHANNEL DISABLE
! ! ! ! ! ! ! +--------    1 = CHANNEL ENABLE
! ! ! ! ! ! !
! ! ! ! ! ! +----------    0 = READ RAM ( WRITE PERIPHERAL )
! ! ! ! ! ! +----------    1 = WRITE RAM ( READ PERIPHERAL )
! ! ! ! ! !
! ! ! ! ! +------------    0 = AUTO WORD CT RE-LOAD DISABLED
! ! ! ! ! +------------    1 = AUTO WORD CT RE-LOAD ENABLED
! ! ! ! !
! ! ! ! +--------------    0 = CHANNEL INTERRUPT DISABLE
! ! ! ! +--------------    1 = CHANNEL INTERRUPT ENABLE
! ! ! !
! ! ! +----------------    0 = WORD CT TC = CHANNEL DISABLE
! ! ! +----------------    1 = CHANNEL ALWAYS ENABLED
! ! !
! ! +------------------    0 = REQUEST LOW TO HIGH EDGE
! ! +------------------    1 = REQUEST HIGH TO LOW EDGE
! !
! +--------------------    0 = ACKNOWLEDGE LOW STROBE
! +--------------------    1 = ACKNOWLEDGE HIGH STROBE
!
!                               CHANNEL 0
!
+----------------------        NOT USED
!
!
!                               CHANNEL 1
!
+----------------------    0 = CHANNEL REQ / ACK PROTOCOL
+----------------------    1 = QIC II XFER / ACK PROTOCOL
!
!
!                               CHANNEL 2
!
+----------------------    0 = CHANNEL REQ / ACK PROTOCOL
+----------------------    1 = SASI REQ / ACK PROTOCOL
!
!
!                               CHANNEL 3
!
+----------------------    0 = MEMORY SELECT
+----------------------    1 = MEMORY DESELECT
```

MEMORY CYCLE TIMING

WRITE DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
! ! ! ! ! ! +-+-------     0 0 = 2 CLOCK CYCLES ( 100 NS )
! ! ! ! ! ! +-+-------     0 1 = 3 CLOCK CYCLES ( 150 NS )
! ! ! ! ! ! +-+-------     1 0 = 4 CLOCK CYCLES ( 200 NS )
! ! ! ! ! ! +-+-------     1 1 = 5 CLOCK CYCLES ( 250 NS )
! ! ! ! ! !
! ! ! ! ! +-----------     0 = INTERRUPT LOW
! ! ! ! ! +-----------     1 = INTERRUPT HIGH
! ! ! ! !
+-+-+-+-+-------------     NOT USED
```

CHANNEL STATUS

READ DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
! ! ! ! ! ! ! +--------    1 = CHANNEL 0 ENABLED
! ! ! ! ! ! +----------    1 = CHANNEL 1 ENABLED
! ! ! ! ! +------------    1 = CHANNEL 2 ENABLED
! ! ! ! +--------------    1 = CHANNEL 3 ENABLED
! ! ! +----------------    1 = CHANNEL 0 WORD COUNT > 129
! ! +------------------    1 = CHANNEL 1 WORD COUNT > 129
! +--------------------    1 = CHANNEL 2 WORD COUNT > 129
+----------------------    1 = CHANNEL 3 WORD COUNT > 129
```

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PRODUCT SPECIFICATION

for

OMTI PFM 5060 FOUR-CHANNEL MEMORY CONTROLLER

MAY 1984

OMTI PFM 5060 FOUR-CHANNEL MEMORY CONTROLLER
PRODUCT SPECIFICATION
(PART #20506)

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TABLE OF CONTENTS

Page Number

LIST OF ILLUSTRATIONS

LIST OF TABLES

CHAPTER 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

The OMTI PFM 5060 Four-Channel Memory Controller is a special-purpose CMOS/VLSI component that manages the flow of block-level information between buffer memory and byte-oriented peripheral interfaces in advanced Winchester disk controller designs.

The Memory Controller provides 5 megabyte/second data transfers using four independently programmable DMA channels with contention resolution based on preassigned channel priority, 16-bit addresses, and programmable memory cycle times. The device can be configured to interface with either SCSI protocol busses or QIC-02 protocol busses.

The 5060 is designed to be used with the OMTI PFM 5050 Data Sequencer, a RAM buffer, a byte-oriented microprocessor, and appropriate drivers and receivers.

1.2 5060 MEMORY CONTROLLER CAPABILITIES

* Four asynchronous DMA channels
* Contention resolution on channel priority basis
* Request/Acknowledge DMA handshake protocol
* Configurable SCSI and QIC-02 Request/Acknowledge handshake protocol
* Independent polarity control of Request/Acknowledge signals
* Automatic address increment and word count decrement for all channels
* Independent auto-reinitialization of word count for all channels
* Independent control of channel-end interrupt
* Enable/disable control of channel requests
* Programmable memory cycle time (2 to 5 clock cycles)
* Control of up to 8 external registers
* Transfer rate of up to 5 megabyte/sec

* 16-bit memory addressing

* No real-time intervention required

* 68-pin leadless plastic package

1.3 ARCHITECTURAL OVERVIEW

Figure 1 illustrates a conceptual block diagram of the PFM 5060 Memory Controller, including the major logic blocks. There are two logic blocks entirely within the 5060; additional blocks define the four external interfaces. The internal blocks are discussed below; the interfaces are discussed in Section 1.4. A more detailed description of the implementation is provided by Figure 2, which includes pin inputs and outputs as well as logic blocks and internal data flow.

1.3.1 Registers/Control Logic

The Registers/Control block contains 22 8-bit internal registers and associated control logic. In addition, 12 external registers are provided. The write registers may be individually written to initialize the parameters that control data transfer; the read registers may be individually read to obtain status information about command execution.

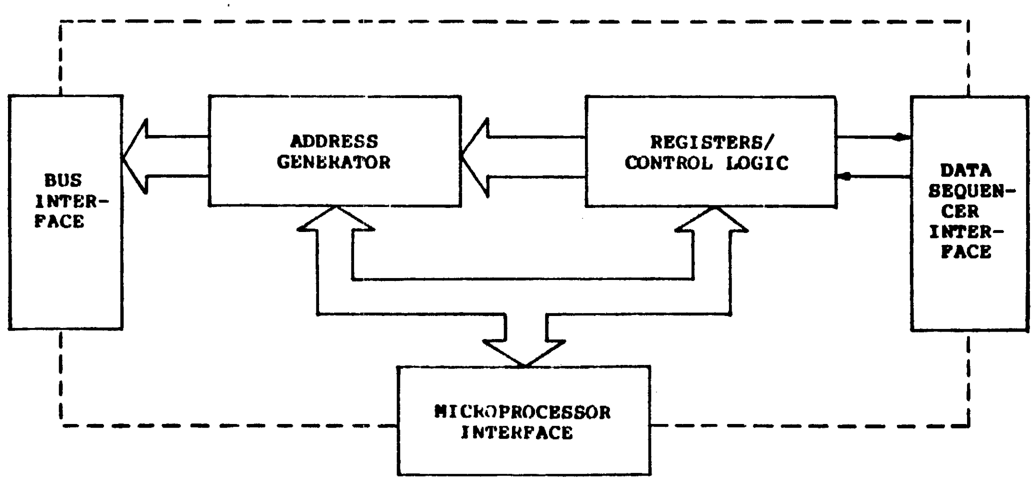


Figure 1. Conceptual Block Diagram

1.3.2 Address Generator

The Address Generator outputs addresses to the DMA buffer memory that serve to locate the stream of data to be transferred to the disk via the Data Sequencer. The Address Generator automatically increments the address value to point to the next location in the buffer.

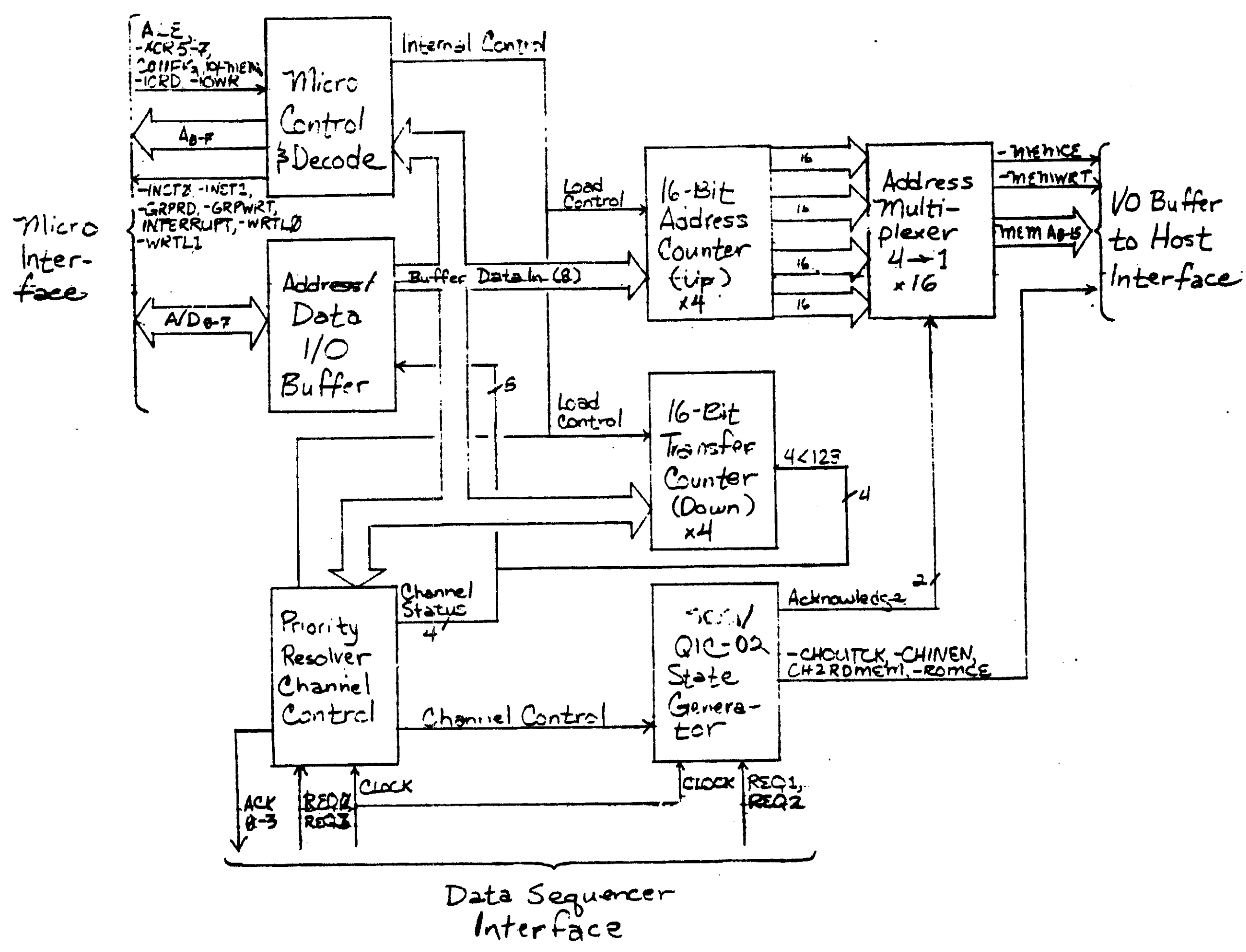


Figure 2. Functional Block Diagram

1.4 SYSTEM CONFIGURATION

Illustrated below is a typical system configuration, incorporating the 5060, the 5050 Data Sequencer, and the 5070 VCO/Encode/Decode chip.

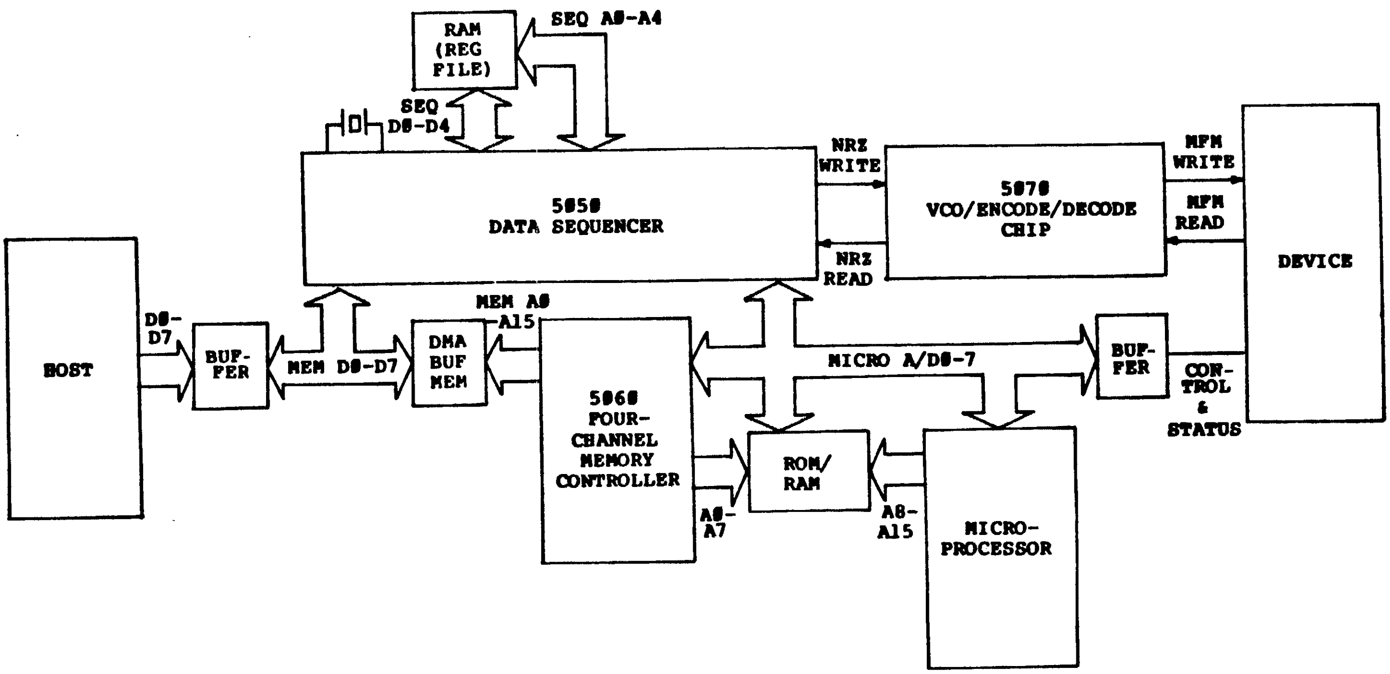


Figure 3. Typical System Configuration

1.4.1 Buffer Interface

Addresses from the Address Generator are transferred across the buffer interface and used to locate blocks of memory in the buffer. The Memory Controller then causes the Data Sequencer to transfer data to or from these memory blocks.

1.4.2 Data Sequencer Interface

Two groups of lines connect the 5060 Memory Controller with the 5050 Data Sequencer. These lines serve to transmit request/acknowledge signals between the two chips, so their operation can be coordinated. The 5060 uses these lines to initiate a block transfer from the 5050 to the DMA buffer memory after the address has been generated.

1.4.3 Local Microprocessor Interface

This block contains the logic necessary to allow the local microprocessor to read or write the internal registers. An 8-bit bus connects this block to the Register File.

CHAPTER 2

FUNCTIONAL DESCRIPTION

2.1 INTRODUCTION

The 5060's basic function is to control the transfer of blocks of data between the 5050 Data Sequencer and the DMA buffer memory. The 5060 performs this control function by generating sequences of addresses into the buffer that serve to locate the words of data that comprise a block, and activating the 5050 to actually perform the data transfer.

The 5060 has four DMA channels that can be independently controlled. One of these may be programmed to interface to an SCSI bus connecting the disk controller with its host. A second channel may be programmed to interface to a QIC-02 bus connecting the disk controller with the host. All four channels are used to generate addresses into the buffer and to enable the transfers of data to and from the buffer.

The 5060 can be initialized in many different ways to customize it to the requirements of a particular disk controller design. This initialization is performed by a program in the local microprocessor using the programmable Control registers of the 5060. The 5060 is designed to be initialized either by a Z8- or 8085/8051-type microprocessor; the timing and pin functions of the 5060 are slightly different depending on which microprocessor is used. (See Chapter 3, Interfacing, for specific details).

2.2 REGISTERS

There are two types of registers on the 5060 Memory Controller: Control registers (WR0-WR20, WR24, WR25, and WR28-WR31) and Status registers (RR0, RR24, RR25, and RR28-RR31). These registers are summarized in Table 1; their addresses are contained in Table 2. Following the tables is a description of the individual bits in each of the registers.

Table 1. 5060 Control and Status Registers

Control (Write) Register Functions		Status (Read) Register Functions	
WR0	Channel 0 Address 0-7	RR0	Channel Status
WR1	Channel 0 Address 8-15	RR1	Not Used
WR2	Channel 0 Word Count 0-7	RR2	Not Used
WR3	Channel 0 Word Count 8-15	RR3	Not Used
WR4	Channel 1 Address 0-7	RR4	Not Used
WR5	Channel 1 Address 8-15	RR5	Not Used
WR6	Channel 1 Word Count 0-7	RR6	Not Used
WR7	Channel 1 Word Count 8-15	RR7	Not Used
WR8	Channel 2 Address 0-7	RR8	Not Used
WR9	Channel 2 Address 8-15	RR9	Not Used
WR10	Channel 2 Word Count 0-7	RR10	Not Used
WR11	Channel 2 Word Count 8-15	RR11	Not Used
WR12	Channel 3 Address 0-7	RR12	Not Used
WR13	Channel 3 Address 8-15	RR13	Not Used
WR14	Channel 3 Word Count 0-7	RR14	Not Used
WR15	Channel 3 Word Count 8-15	RR15	Not Used
WR16	Channel 0 Control	RR16	Not Used
WR17	Channel 1 Control	RR17	Not Used
WR18	Channel 2 Control	RR18	Not Used
WR19	Channel 3 Control	RR19	Not Used
WR20	Memory Cycle Timing	RR20	Not Used
WR21	Not Used	RR21	Not Used
WR22	Not Used	RR22	Not Used
WR23	Not Used	RR23	Not Used
WR23	Not Used	RR23	Not Used
WR24	External Out Strobe 0	RR24	External In Strobe 0
WR25	External Out Strobe 1	RR25	External In Strobe 1
WR26	Not Used	RR26	Not Used
WR27	Not Used	RR27	Not Used
WR28	External Out Group Strobe	RR28	External In Group Strobe
WR29	External Out Group Strobe	RR29	External In Group Strobe
WR30	External Out Group Strobe	RR30	External In Group Strobe
WR31	External Out Group Strobe	RR31	External In Group Strobe

Table 2. 5060 Register Map

AD4	AD3	AD2	AD1	AD0	Write	Read
0	0	0	0	0	WR0	RR0
0	0	0	0	1	WR1	NOT USED
0	0	0	1	0	WR2	NOT USED
0	0	0	1	1	WR3	NOT USED
0	0	1	0	0	WR4	NOT USED
0	0	1	0	1	WR5	NOT USED
0	0	1	1	0	WR6	NOT USED
0	0	1	1	1	WR7	NOT USED
0	1	0	0	0	WR8	NOT USED
0	1	0	0	1	WR9	NOT USED
0	1	0	1	0	WR10	NOT USED
0	1	0	1	1	WR11	NOT USED
0	1	1	0	0	WR12	NOT USED
0	1	1	0	1	WR13	NOT USED
0	1	1	1	0	WR14	NOT USED
0	1	1	1	1	WR15	NOT USED
1	0	0	0	0	WR16	NOT USED
1	0	0	0	1	WR17	NOT USED
1	0	0	1	0	WR18	NOT USED
1	0	0	1	1	WR19	NOT USED
1	0	1	0	0	WR20	NOT USED
1	0	1	0	1	NOT USED	NOT USED
1	0	1	1	0	NOT USED	NOT USED
1	0	1	1	1	NOT USED	NOT USED
1	1	0	0	0	WR24	RR24
1	1	0	0	1	WR25	RR25
1	1	0	1	0	NOT USED	NOT USED
1	1	0	1	1	NOT USED	NOT USED
1	1	1	X	X	WR28	RR28
1	1	1	X	X	WR29	RR29
1	1	1	X	X	WR30	RR30
1	1	1	X	X	WR31	RR31

X = don't care

2.2.1 Control Registers

There are 27 Control registers, including those which direct various chip-level functions as well as those which direct the activities of the individual channels.

The chip-level registers include: Memory Cycle Timing, External Out Strobe 0, External Out Strobe 1, and External Out Group Strobe.

Each of the Memory Controller's four channels has a group of registers which govern that channel's activities. Each group consists of a Memory Address 0-7, Memory Address 8-15, Word Count 0-7, Word Count 8-15, and Channel Control register. Because these registers, with the exception of the Channel Control registers, function identically for all four channels, they are grouped together by type in the following discussion. The four Channel Control registers are discussed separately.

WRITE REGISTER 0, 4, 8, 12: MEMORY ADDRESS 0-7

```
   7   6   5   4   3   2   1   0
+---------------------------------+
|   |   |   |   |   |   |   |   |
+---------------------------------+
  |___|___|___|___|___|___|___|_______ 00-FF
```

The Memory Address 0-7 register specifies the least-significant byte of the starting address of the memory block where data is available (for output), or where data is to be stored (for input). The address is incremented after each data transfer.

WRITE REGISTER 1, 5, 9, 13: MEMORY ADDRESS 8-15

```
   7   6   5   4   3   2   1   0
+---------------------------------+
|   |   |   |   |   |   |   |   |
+---------------------------------+
  |___|___|___|___|___|___|___|_______ 00-FF
```

The Memory Address 8-15 register specifies the most-significant byte of the starting address of the memory block where data is available (for outptut), or where data is to be stored (for input). This register is incremented by overflow in Memory Address 0-7.

WRITE REGISTER 2, 6, 10, 14: WORD COUNT 0-7

```
      7   6   5   4   3   2   1   0
    +---------------------------------+
    |   |   |   |   |   |   |   |   |
    +---------------------------------+
      |___|___|___|___|___|___|___|_______   00-FF
```

The Word Count 0-7 register contains the least-significant byte of the value specifying the number of word transfers to be performed. The word count is decremented after each transfer.

WRITE REGISTER 3, 7, 11, 15: WORD COUNT 8-15

```
      7   6   5   4   3   2   1   0
    +---------------------------------+
    |   |   |   |   |   |   |   |   |
    +---------------------------------+
      |___|___|___|___|___|___|___|_______   00-FF
```

The Word Count 8-15 register contains the most-significant byte of the value specifying the number of word transfers to be performed. This register is decremented by underflow in Word Count 0-7.

WRITE REGISTER 16: CHANNEL Ø CONTROL

```
  7   6   5   4   3   2   1   Ø
+-------------------------------+
|   |   |   |   |   |   |   |   |
+-------------------------------+
  |   |   |   |   |   |   |   |_____ Ø = Channel Disable
  |   |   |   |   |   |   |   |_____ 1 = Channel Enable
  |   |   |   |   |   |   |
  |   |   |   |   |   |   |_________ Ø = Read RAM (Write
  |   |   |   |   |   |   |              Peripheral)
  |   |   |   |   |   |   |_________ 1 = Write RAM (Read
  |   |   |   |   |   |                  Peripheral)
  |   |   |   |   |   |
  |   |   |   |   |   |  ___________ Ø = Auto Word CT
  |   |   |   |   |   |                  Re-Load Disabled
  |   |   |   |   |   |  ___________ 1 = Auto Word CT
  |   |   |   |   |                      Re-Load Enabled
  |   |   |   |   |
  |   |   |   |   |_________________ Ø = Channel Interrupt
  |   |   |   |   |                      Disable
  |   |   |   |   |_________________ 1 = Channel Interrupt
  |   |   |   |                          Enable
  |   |   |   |
  |   |   |   |_____________________ Ø = Word Count TC =
  |   |   |   |                          Channel Disable
  |   |   |   |_____________________ 1 = Channel Always Enabled
  |   |   |
  |   |   |_________________________ Ø = Request Low to High Edge
  |   |   |_________________________ 1 = Request High to Low Edge
  |   |
  |   |_____________________________ Ø = Acknowledge Low Strobe
  |   |_____________________________ 1 = Acknowledge High Strobe
  |
  |_________________________________ Reserved
```

Bit Ø enables or disables the channel.

Bit 1 specifies the direction of data transfer: when set, data is transferred from the DMA buffer memory to the peripheral; when cleared, data is transferred from the peripheral device to the DMA buffer memory.

When bit 2 is set, completion of DMA service is followed by the automatic reloading of the channel's Word Count register with its value prior to the transfer. This option allows a sequence of records to be transferred via DMA, without requiring re-initialization of the channel's Address and Word Count registers prior to each record's transfer. (For continuous DMA operation, bits Ø and 4 in this register must also be set.)

When bit 3 is set, completion of a data transfer (WC = Ø) is followed by an interrupt request sent to the microprocessor. The microprocessor responds to the interrupt by reading the channel's Status register or, if bit 4 = 1, by issuing another command. When bit 3 is cleared, interrupts from the channel are disabled. This option avoids the neccesity of polling when only a single channel is being used.

When bit 4 is cleared, DMA operations will be automatically prevented when the word count equals zero. To begin another operation on that channel, the enable bit (bit Ø) must be reprogrammed by reading the Status register. When bit 4 is set, the channel remains enabled after the word count equals zero. In this case, interrupts are reenabled (bit 3 = 1) by a command from the microprocessor.

Bits 5 and 6 control the polarity of the request and acknowledge signals, respectively.

Bit 7 is reserved.

WRITE REGISTER 17: CHANNEL 1 CONTROL

```
      7   6   5   4   3   2   1   Ø
    +---------------------------------+
    |   |   |   |   |   |   |   |   |
    +---------------------------------+
      |   |   |   |   |   |   |   |_____ Ø = Channel Disable
      |   |   |   |   |   |   |   |_____ 1 = Channel Enable
      |   |   |   |   |   |   |
      |   |   |   |   |   |   |_________ Ø = Read RAM (Write
      |   |   |   |   |   |   |              Peripheral)
      |   |   |   |   |   |   |_________ 1 = Write RAM (Read
      |   |   |   |   |   |                  Peripheral)
      |   |   |   |   |   |
      |   |   |   |   |   |  ___________ Ø = Auto Word CT
      |   |   |   |   |   |                  Re-Load Disabled
      |   |   |   |   |   |  ___________ 1 = Auto Word CT
      |   |   |   |   |                      Re-Load Enabled
      |   |   |   |   |
      |   |   |   |   |_________________ Ø = Channel Interrupt
      |   |   |   |   |                      Disable
      |   |   |   |   |_________________ 1 = Channel Interrupt
      |   |   |   |                          Enable
      |   |   |   |
      |   |   |   |_____________________ Ø = Word Count TC =
      |   |   |   |                          Channel Disable
      |   |   |   |_____________________ 1 = Channel Always Enabled
      |   |   |
      |   |   |_________________________ Ø = Request Low to High Edge
      |   |   |_________________________ 1 = Request High to Low Edge
      |   |
      |   |_____________________________ Ø = Acknowledge Low Strobe
      |   |_____________________________ 1 = Acknowledge High Strobe
      |
      |_________________________________ Ø = Channel Req/Ack Protocol
      |_________________________________ 1 = QIC-Ø2 XFER/Ack Protocol
```

Bit Ø enables or disables the channel.

Bit 1 specifies the direction of data transfer: when set, data is transferred from the DMA buffer memory to the peripheral; when cleared, data is transferred from the peripheral device to the DMA buffer memory.

When bit 2 is set, completion of DMA service is followed by the automatic reloading of the channel's Word Count register with its value prior to the transfer. This option allows a sequence of records to be transferred via DMA, without requiring re-initialization of the channel's Address and Word Count registers prior to each record's transfer. (For continuous DMA operation, bits Ø and 4 in this register must also be set.)

When bit 3 is set, completion of a data transfer (WC = Ø) is followed by an interrupt request sent to the microprocessor. The microprocessor responds to the interrupt by reading the channel's Status register or, if bit 4 = 1, by issuing another command. When bit 3 is cleared, interrupts from the channel are disabled. This option avoids the neccesity of polling when only a single channel is being used.

When bit 4 is cleared, DMA operations will be automatically prevented when the word count equals zero. To begin another operation on that channel, the enable bit (bit Ø) must be reprogrammed by reading the Status register. When bit 4 is set, the channel remains enabled after the word count equals zero. In this case, interrupts are reenabled (bit 3 = 1) by a command from the microprocessor.

Bits 5 and 6 control the polarity of the request and acknowledge signals, respectively.

When bit 7 is set, the channel will use the QIC-Ø2 transfer/acknowledge data transfer handshake protocol. When this bit is cleared, the channel will use the standard DMA memory request/acknowledge protocol.

WRITE REGISTER 18: CHANNEL 2 CONTROL

```
  7   6   5   4   3   2   1   Ø
+-------------------------------+
|   |   |   |   |   |   |   |   |
+-------------------------------+
  |   |   |   |   |   |   |   |______ Ø = Channel Disable
  |   |   |   |   |   |   |   |______ 1 = Channel Enable
  |   |   |   |   |   |   |
  |   |   |   |   |   |   |__________ Ø = Read RAM (Write
  |   |   |   |   |   |   |               Peripheral)
  |   |   |   |   |   |   |__________ 1 = Write RAM (Read
  |   |   |   |   |   |                   Peripheral)
  |   |   |   |   |   |
  |   |   |   |   |   |  ____________ Ø = Auto Word CT
  |   |   |   |   |   |                   Re-Load Disabled
  |   |   |   |   |   |  ____________ 1 = Auto Word CT
  |   |   |   |   |                       Re-Load Enabled
  |   |   |   |   |
  |   |   |   |   |__________________ Ø = Channel Interrupt
  |   |   |   |   |                       Disable
  |   |   |   |   |__________________ 1 = Channel Interrupt
  |   |   |   |                           Enable
  |   |   |   |
  |   |   |   |______________________ Ø = Word Count TC =
  |   |   |   |                           Channel Disable
  |   |   |   |______________________ 1 = Channel Always Enabled
  |   |   |
  |   |   |__________________________ Ø = Request Low to High Edge
  |   |   |__________________________ 1 = Request High to Low Edge
  |   |
  |   |______________________________ Ø = Acknowledge Low Strobe
  |   |______________________________ 1 = Acknowledge High Strobe
  |
  |__________________________________ Ø = Channel Req/Ack Protocol
  |__________________________________ 1 = SCSI Req/Ack Protocol
```

Bit Ø enables or disables the channel.

Bit 1 specifies the direction of data transfer: when set, data is transferred from the DMA buffer memory to the peripheral; when cleared, data is transferred from the peripheral device to the DMA buffer memory.

When bit 2 is set, completion of DMA service is followed by the automatic reloading of the channel's Word Count register with its value prior to the transfer. This option allows a sequence of records to be transferred via DMA, without requiring re-initialization of the channel's Address and Word Count registers prior to each record's transfer. (For continuous DMA operation, bits Ø and 4 in this register must also be set.)

When bit 3 is set, completion of a data transfer (WC = Ø) is followed by an interrupt request sent to the microprocessor. The microprocessor responds to the interrupt by reading the channel's Status register or, if bit 4 = 1, by issuing another command. When bit 3 is cleared, interrupts from the channel are disabled. This option avoids the neccesity of polling when only a single channel is being used.

When bit 4 is cleared, DMA operations will be automatically prevented when the word count equals zero. To begin another operation on that channel, the enable bit (bit Ø) must be reprogrammed by reading the Status register. When bit 4 is set, the channel remains enabled after the word count equals zero. In this case, interrupts are reenabled (bit 3 = 1) by a command from the microprocessor.

Bits 5 and 6 control the polarity of the request and acknowledge signals, respectively.

When bit 7 is set, the channel will use the SCSI request/acknowledge data transfer handshake protocol. When this bit is cleared, the channel will use the standard DMA memory request/acknowledge protocol.

WRITE REGISTER 19: CHANNEL 3 CONTROL

```
   7   6   5   4   3   2   1   0
 +-------------------------------+
 |   |   |   |   |   |   |   |   |
 +-------------------------------+
   |   |   |   |   |   |   |   |_____ Ø = Channel Disable
   |   |   |   |   |   |   |   |_____ 1 = Channel Enable
   |   |   |   |   |   |   |
   |   |   |   |   |   |   |_________ Ø = Read RAM (Write
   |   |   |   |   |   |   |              Peripheral)
   |   |   |   |   |   |   |_________ 1 = Write RAM (Read
   |   |   |   |   |   |                  Peripheral)
   |   |   |   |   |   |
   |   |   |   |   |   |  ___________ Ø = Auto Word CT
   |   |   |   |   |   |                  Re-Load Disabled
   |   |   |   |   |   |  ___________ 1 = Auto Word CT
   |   |   |   |   |                      Re-Load Enabled
   |   |   |   |   |
   |   |   |   |   |_________________ Ø = Channel Interrupt
   |   |   |   |   |                      Disable
   |   |   |   |   |_________________ 1 = Channel Interrupt
   |   |   |   |                          Enable
   |   |   |   |
   |   |   |   |_____________________ Ø = Word Count TC =
   |   |   |   |                          Channel Disable
   |   |   |   |_____________________ 1 = Channel Always Enabled
   |   |   |
   |   |   |_________________________ Ø = Request Low to High Edge
   |   |   |_________________________ 1 = Request High to Low Edge
   |   |
   |   |_____________________________ Ø = Acknowledge Low Strobe
   |   |_____________________________ 1 = Acknowledge High Strobe
   |
   |_________________________________ Ø = Reserved
```

Bit 0 enables or disables the channel.

Bit 1 specifies the direction of data transfer: when set, data is transferred from the DMA buffer memory to the peripheral; when cleared, data is transferred from the peripheral device to the DMA buffer memory.

When bit 2 is set, completion of DMA service is followed by the automatic reloading of the channel's Word Count register with its value prior to the transfer. This option allows a sequence of records to be transferred via DMA, without requiring re-initialization of the channel's Address and Word Count registers prior to each record's transfer. (For continuous DMA operation, bits 0 and 4 in this register must also be set.)

When bit 3 is set, completion of a data transfer (WC = 0) is followed by an interrupt request sent to the microprocessor. The microprocessor responds to the interrupt by reading the channel's Status register or, if bit 4 = 1, by issuing another command. When bit 3 is cleared, interrupts from the channel are disabled. This option avoids the neccesity of polling when only a single channel is being used.

When bit 4 is cleared, DMA operations will be automatically prevented when the word count equals zero. To begin another operation on that channel, the enable bit (bit 0) must be reprogrammed by reading the Status register. When bit 4 is set, the channel remains enabled after the word count equals zero. In this case, interrupts are reenabled (bit 3 = 1) by a command from the microprocessor.

Bits 5 and 6 control the polarity of the request and acknowledge signals, respectively.

Bit 7 is reserved.

WRITE REGISTER 2Ø: MEMORY CYCLE TIMING

```
   7   6   5   4   3   2   1   Ø
 +---------------------------------+
 |   |   |   |   |   |   |   |   |   |
 +---------------------------------+
   |   |   |   |   |   |   |   |
   |   |   |   |   |   |   Ø   Ø    =  2 Clock Cycles (1ØØ ns)
   |   |   |   |   |   |   Ø   1    =  3 Clock Cycles (15Ø ns)
   |   |   |   |   |   |   1   Ø    =  4 Clock Cycles (2ØØ ns)
   |   |   |   |   |   |   1   1    =  5 Clock Cycles (25Ø ns)
   |   |   |   |   |   |
   |   |   |   |   |   |  ________  Ø = Interrupt Active Low
   |   |   |   |   |   |__________  1 = Interrupt Active High
   |   |   |   |   |
   |___|___|___|___|______________  Reserved
```

Bits Ø and 1 specify the number of clock cycles used in the memory cycle for each word transferred. This option is provided to allow the Memory Controller to accomodate both low-speed and high-speed memories.

Bit 2 specifies the polarity of the Memory Controller's Interrupt Request line (pin 6Ø).

Bits 3-7 are reserved.

WRITE REGISTER 24: EXTERNAL OUT STROBE Ø

```
   7   6   5   4   3   2   1   Ø
 +---------------------------------+
 |   |   |   |   |   |   |   |   |   |
 +---------------------------------+
   |___|___|___|___|___|___|___|_______  ØØ-FF
```

When this register is written, -WRTLØ (pin 55) is asserted and may be used to strobe information from the microprocessor's A/D bus into an external register. The information in this register may be used as additional device control lines.

WRITE REGISTER 25: EXTERNAL OUT STROBE 1

```
   7   6   5   4   3   2   1   0
+--------------------------------+
|   |   |   |   |   |   |   |   |
+--------------------------------+
  |___|___|___|___|___|___|___|__________  00-FF
```

When this register is written, -WRTL1 (pin 56) is asserted and may be used to strobe information from the microprocessor's A/D bus into an external register. The information in this register may be used as additional device control lines.

WRITE REGISTER 28-31: EXTERNAL OUT GROUP STROBE

```
   7   6   5   4   3   2   1   0
+--------------------------------+
|   |   |   |   |   |   |   |   |
+--------------------------------+
  |___|___|___|___|___|__________________  00-FF
```

When these registers are written, -GRPWWRT (pin 50) is asserted and may be used to strobe information from the microprocessor's A/D bus into external registers. Information in these registers may be used as additional device control lines.

2.2.2 Status Registers

The 5060 contains seven Status registers, which provide device status information about the progress of data transfers.

READ REGISTER 0: CHANNEL STATUS REGISTER

```
   7   6   5   4   3   2   1   0
+--------------------------------+
|   |   |   |   |   |   |   |   |
+--------------------------------+
  |   |   |   |   |   |   |   |___ 1 = Channel 0 Enabled
  |   |   |   |   |   |   |_______ 1 = Channel 1 Enabled
  |   |   |   |   |   |___________ 1 = Channel 2 Enabled
  |   |   |   |   |_______________ 1 = Channel 3 Enabled
  |   |   |   |___________________ 1 = Channel 0 Word Count > 129
  |   |   |_______________________ 1 = Channel 1 Word Count > 129
  |   |___________________________ 1 = Channel 2 Word Count > 129
  |_______________________________ 1 = Channel 3 Word Count > 129
```

Bits Ø-3 enable or disable channels Ø-3, respectively.

Bits 4-7 are cleared when the last 128 words of data are being transferred. This allows the microprocessor to monitor the progress of data transfers, and manage the loading and unloading of the buffer accordingly.

READ REGISTER 24: EXTERNAL IN STROBE Ø

```
   7   6   5   4   3   2   1   Ø
 +---------------------------------+
 |   |   |   |   |   |   |   |   |
 +---------------------------------+
   |___|___|___|___|___|___|___|________  ØØ-FF
```

When this register is read, -INSTØ is asserted (pin 53), and additional device status information contained in an external peripheral chip may be read by the microprocessor from the A/D bus.

READ REGISTER 25: EXTERNAL IN STROBE 1

```
   7   6   5   4   3   2   1   Ø
 +---------------------------------+
 |   |   |   |   |   |   |   |   |
 +---------------------------------+
   |___|___|___|___|___|___|___|________  ØØ-FF
```

When this register is read, -INST1 is asserted (pin 54), and additional device status information contained in an external peripheral chip may be read by the microprocessor from the A/D bus.

READ REGISTER 28-31: EXTERNAL IN GROUP STROBE

```
   7   6   5   4   3   2   1   Ø
 +---------------------------------+
 |   |   |   |   |   |   |   |   |
 +---------------------------------+
   |___|___|___|___|___|________________  ØØ-FF
```

When these registers are read, -GRPRD (pin 49) is asserted, and additional device status contained in an external peripheral chip may be read by the microprocessor from the A/D bus.

2.3 OPERATING MODES

The 5060 has two operating modes: 8085/8051 mode and Z8 mode. The 5060's operation in these two modes differs only in the pin functions and the timing characteristics, which are matched to the appropriate microprocessor. Chapter 3 provides the specific information.

CHAPTER 3

INTERFACING

3.1 SIGNAL DESCRIPTIONS

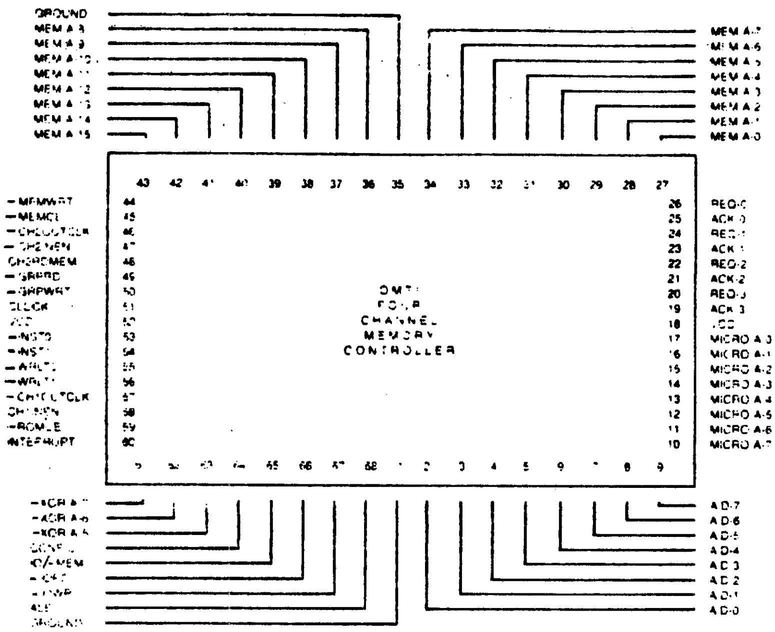


Figure 4. Pin Assignments

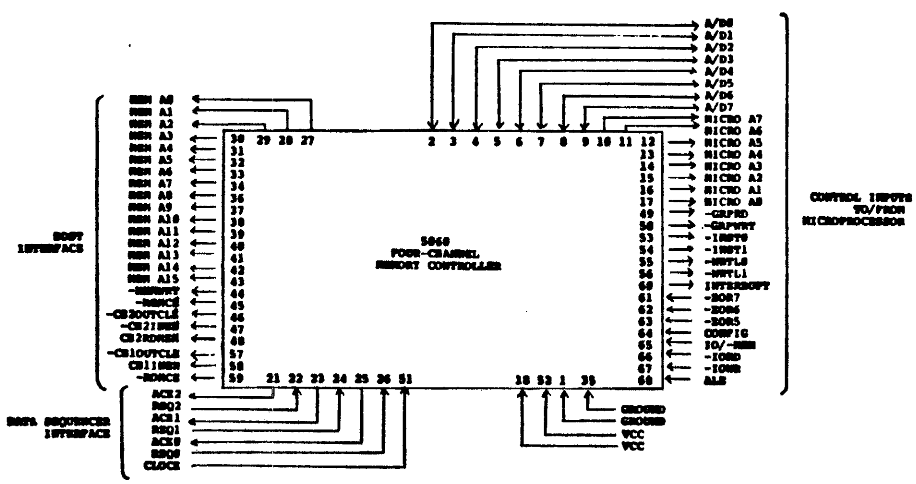


Figure 5. Pin Functions

Table 3. Pin Descriptions

Symbol	Type	Pin #	Name and Function
ACKØ ACK1 ACK2 ACK3	O O O O	25 23 21 19	DMA Acknowledge. (Active High.) These signals notify the individual peripherals when one has been granted a memory cycle. Polarity of all ACK outputs is programmable. When channel 1 is configured for the QIC-Ø2 protocol, ACK 1 is configured for the QIC-Ø2 XFER signal; when channel 2 is configured for the SCSI protocol, ACK 2 is configured for the SCSI REQ signal.
A/DØ- A/D7	I/O	2-9	Address/Data Bus. (Active High, 3-state.) These multiplexed lines interface with the low-order 8 bits of the microprocessor's Address/Data bus. Addresses are latched into the Memory Controller's address register on the falling edge of ALE. If the address is within the range of the internal chip select, data is either written into or read from the Memory Controller's registers, depending on whether -IOWR or -IORD is active.
ALE	I	68	Address Latch Enable. (Active High.) The falling edge of ALE is used to latch ADØ-AD7 into the selected register.
-CH1OUTCLK	O	57	Channel 1 Out Clock. (Active Low.) This output is used to strobe data from a memory read cycle into an external register of the QIC-Ø2 host interface.
-CH2OUTCLK	O	46	Channel 2 Out Clock. (Active Low.) This output is used to strobe data from a memory read cycle into an external register of the SCSI host interface.
CH1INEN	O	58	Channel 1 Input Enable. (Active High.) This output signal is used to enable data for the memory write cycle from the QIC-Ø2 host bus buffer.
-CH2INEN	O	47	Channel 2 Input Enable. (Active Low.) This output signal is used to enable data for the memory write cycle from the SCSI host bus buffer.

Table 3. Pin Descriptions, continued

Symbol	Type	Pin #	Name and Function
-CH2RDMEM	O	48	Channel 2 Read Memory. (Active Low.) This output is used for the SCSI I/O interface signal and is a direct output of bit 7 of the Channel 2 Control register. The maximum clock rate is 12 MHz.
CLOCK	I	51	Clock. (Active High.) This input controls the internal arbitration of all REQ and ACK signals. It also controls the programmable memory-cycle timing (WR20), as well as the SCSI and QIC-02 protocol sequences (see Figure 6., State Sequences Diagram).
CONFIG	I	64	Configuration. (Active High.) This input in pulled up internally to select the microprocessor strobe inputs. When this line is grounded, the chip is configured for an 8085/8051-type processor. When the line is left open, the chip is configured for a Z8-type processor, with the following interface changes: -IORD = -DATA STROBE, -IOWR = R/-W, ALE = -AS, IO/-MEM = -DM.
-GRPRD	O	49	Group Read Strobe. (Active Low.) This output strobe provides an interface to an external peripheral chip.
-GRPWRT	O	50	Group Write Strobe. (Active Low.) This output strobe provides an interface to an external peripheral chip.
-INST0 -INST1	O O	53 54	In Status 0-1. (Active Low.) These outputs are internally decoded I/O read strobes (enabled by reading from RR24 or RR25, respectively), used by the microprocessor to read device status via an external buffer to the A/D0-7 bus.
INTERRUPT	O	60	Interrupt. (Active High.) The polarity of the interrupt line is specified by bit 2 in the Memory Cycle Timing register (WR20). This output is asserted according to conditions specified by bits in each channel's Control register.

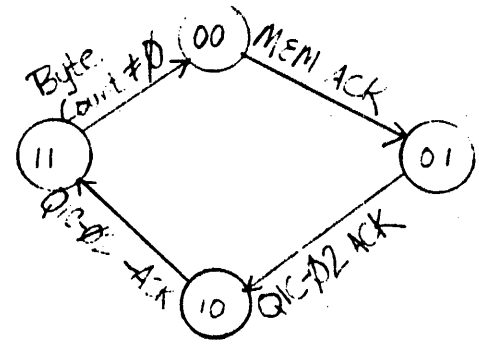
Table 3. Pin Descriptions, continued

Symbol	Type	Pin #	Name and Function
IO/-MEM	I	65	I/O/-Memory. (I/O active High, Memory active Low.) This signal is used for active High chip enable. In 8Ø85/8Ø51 mode, this line is connected to the 8Ø51's IO/-MEM line; in Z8 mode, this line is an active Low chip enable.
-IORD	I	66	I/O Read. (Active Low.) When this input is Low, it is used by the microprocessor to read status information from the Memory Controller. Data is read from the appropriate register as selected by the current value of the address register.
-IOWR	I	67	I/O Write. (Active Low.) When this input Low, it is used by the microprocessor to load information to the Memory Controller. Data is written to the appropriate register as selected by the current value of the address register.
MEMAØ-7 MEMA8-15	O O	27-34, 36-43	Memory Address. (Active High.) The Memory Address bus is used to output the contents of the Memory Address register of the currently selected channel to the DMA buffer memory.
-MEMCE	O	45	Memory Chip Enable. (Active Low.) -MEMCE is an active Low strobe used to enable the DMA buffer memory addressed by MEMAØ-15.
-MEMWRT	O	44	Memory Write. (Active Low.) When both this output and -MEMCE are asserted, data written to the selected memory location in the DMA buffer memory is enabled. When this output is active and -MEMCE is deasserted, data read from the selected memory location in the DMA buffer memory is enabled.
MICROAØ-MICROA7	O	17-1Ø	Micro Address. (Active High.) This 8-bit address bus is the address demultiplexed from the microprocessor's A/D bus, which is latched on the falling edge of ALE. This bus may be used to access the microprocessor's external memory and peripherals.

Table 3. Pin Descriptions, continued

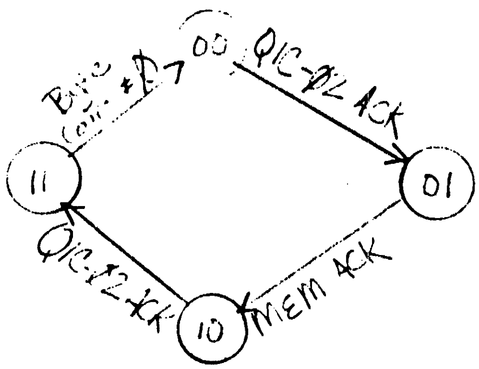
Symbol	Type	Pin #	Name and Function
REQ0 REQ1 REQ2 REQ3	I I I I	26 24 22 20	DMA Request. (Active High.) These lines are asynchronous request inputs used by peripheral devices to obtain DMA service. The priority is fixed, with REQ0 having the highest priority, and REQ3 the lowest priority. Polarity of all REQ inputs is programmable. When channel 1 is configured for the QIC-02 protocol, REQ1 is configured for the QIC-02 ACK signal; when channel 2 is configured for the SCSI protocol, REQ2 is configured for the SCSI ACK signal.
-ROMCE	O	59	ROM Chip Enable. (Active Low.) This output is true when -IORD is true and both -IOWR and IO/-MEM are false.
-WRTL0 -WRTL1	O O	55 56	Write Latch 0-1. (Active Low.) These outputs are internally decoded write strobes (enabled by writing to WR24 or WR25, respectively), used by the microprocessor to write device control via an external latch to the A/D0-7 bus.
-XOR 5 -XOR 6 -XOR 7	I I I	63 62 61	Exclusive OR Address. (Active Low.) These internally pulled up signals are used for internal chip select. They control the polarity of the corresponding address lines. If another group chip select is required, the appropriate line must be grounded.
VCC	I	18, 52	+5 V.
GND	I	35, 1	Ground.

Transfer from Memory to Device via QIC-02:



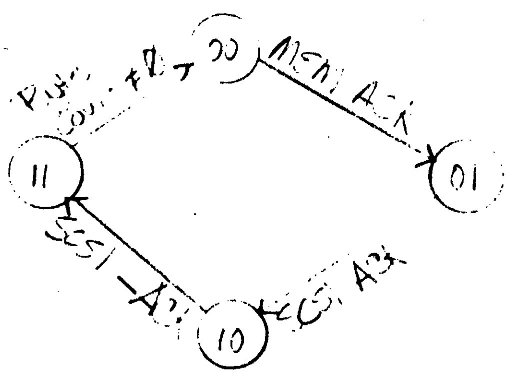
ØØ = Request Memory
Ø1 = QIC-Ø2 Transfer
1Ø = NOP
11 = NOP (hold if false; otherwise loop to ØØ)

Transfer from Device to Memory via QIC-02:



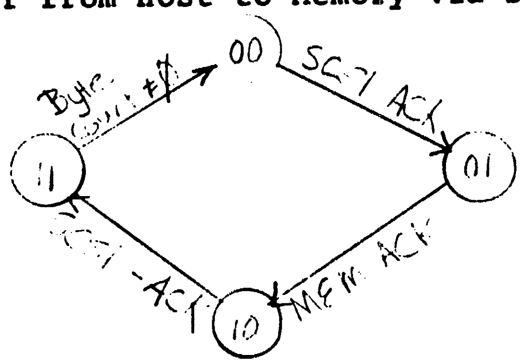
ØØ = NOP (wait for QIC-Ø2 ACK)
Ø1 = Request Memory
1Ø = QIC-Ø2 Xfer
11 = NOP (hold if false; otherwise loop to ØØ)

Transfer from Memory to Host via SCSI:



ØØ = Request Memory
Ø1 = SCSI Request
1Ø = NOP
11 = NOP (hold if false; otherwise loop to ØØ)

Transfer from Host to Memory via SCSI:



ØØ = SCSI Request
Ø1 = Request Memory
1Ø = NOP
11 = NOP (hold if false; otherwise loop to ØØ)

Figure 6. State Sequences for QIC-Ø2 and SCSI Data Transfers

3.2 TIMING

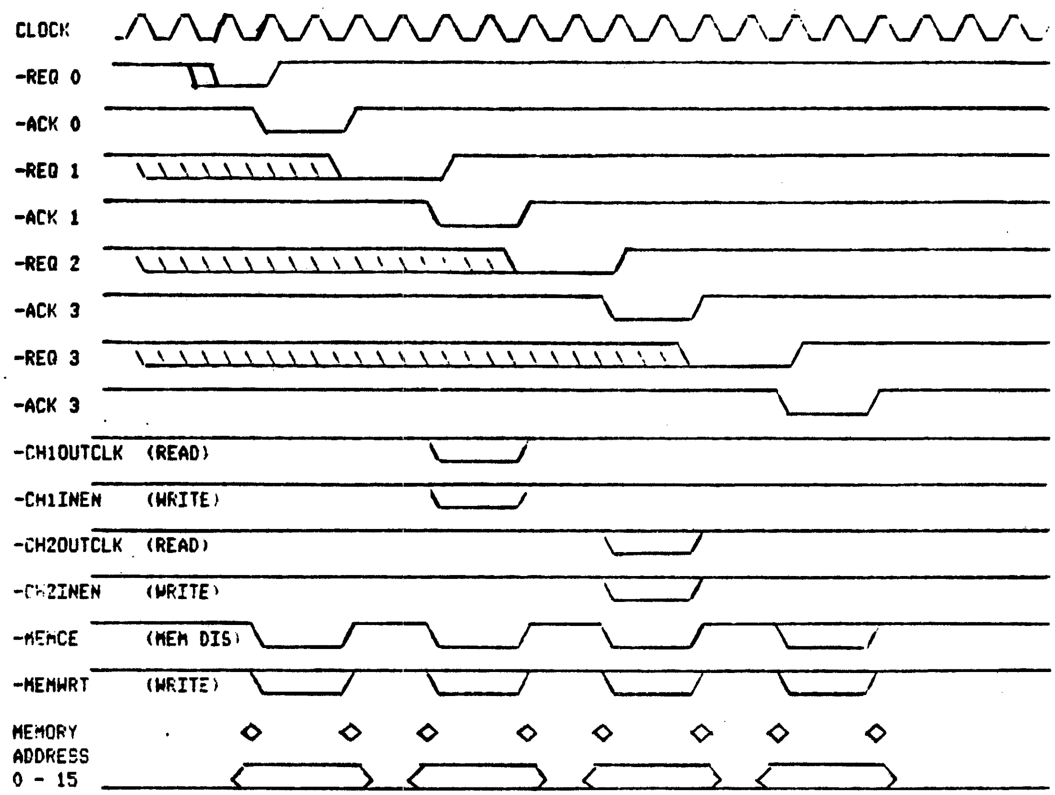


Figure 7. DMA Four Channel REQ/ACK Timing

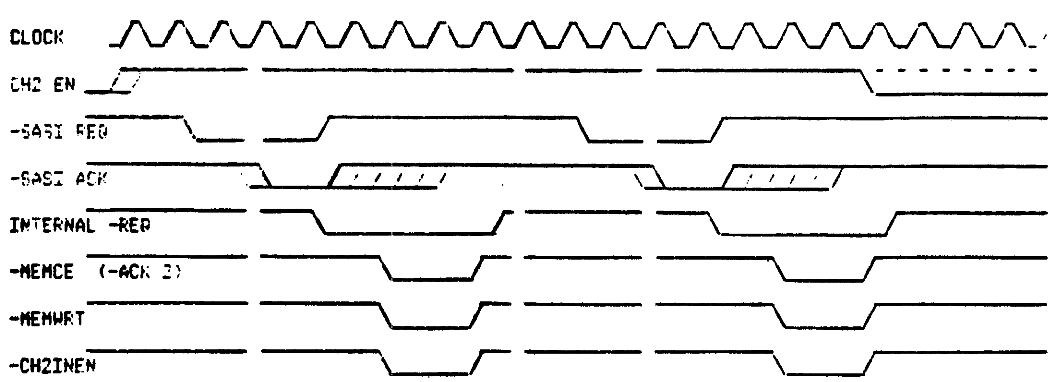


Figure 8. SCSI Host to Buffer Timing

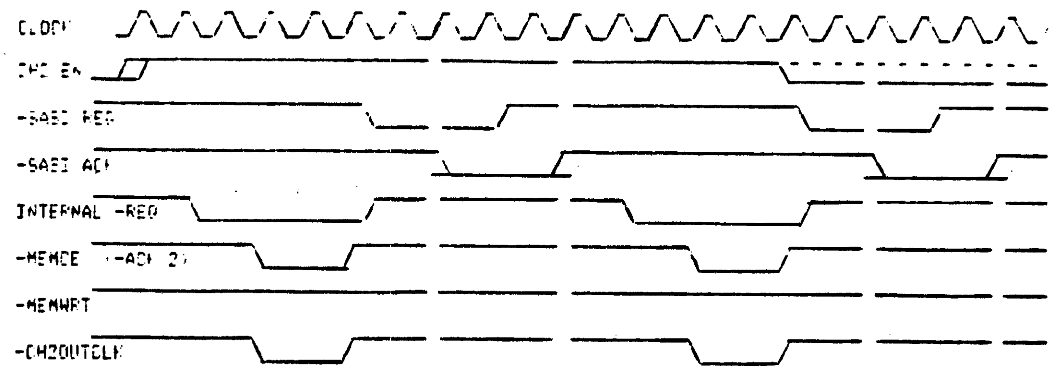


Figure 9. Buffer to SCSI Host Timing

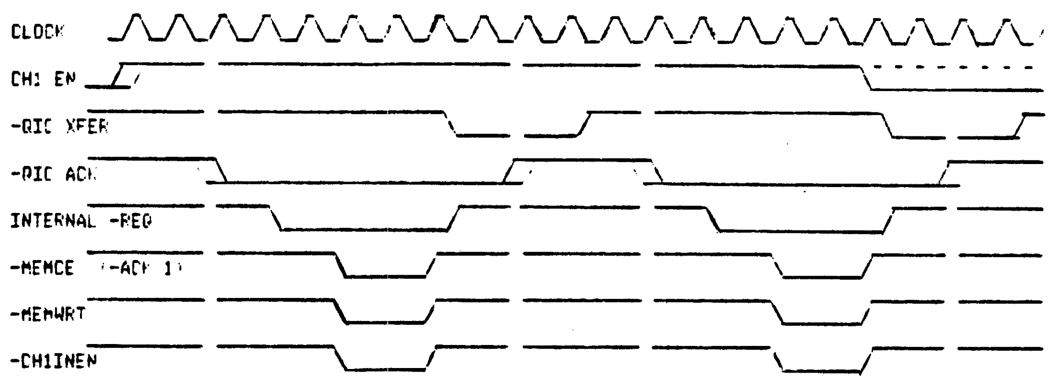


Figure 10. QIC-02 Tape to Buffer Timing

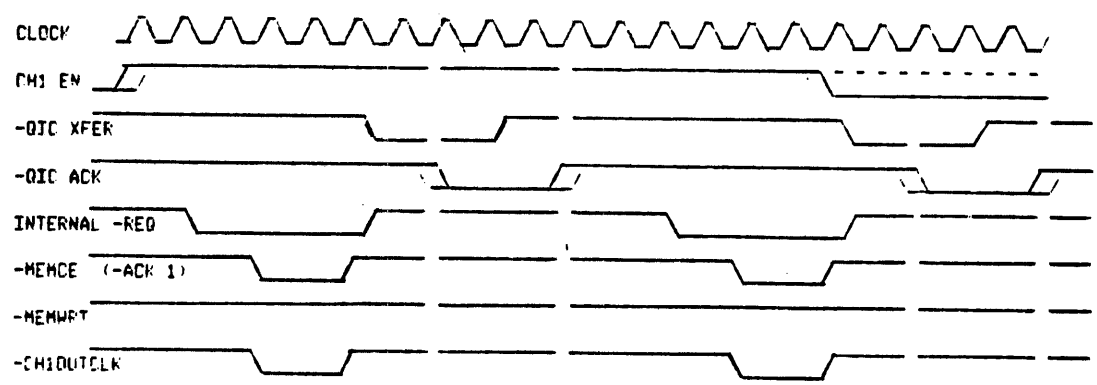


Figure 11. Buffer to QIC-02 Tape Timing

3.3 A.C. CHARACTERISTICS

The two relevant timing diagrams and A.C. characteristics for interfacing the 5060 Memory Controller are given below. (For more information about these chips, the reader is referred to Zilog's Z8681/82 ROMless Z8 Microcomputer Product Specification or Intel's 8051 Single Chip 8-Bit N-Channel Microprocessor Data Sheet.)

3.3.1 Z8 Mode Timing Characteristics (Configuration = 0)

Number	Parameter	Min (ns) (10 MHz)	Max (ns) (10 MHz)
1	-AS Low Pulse Width	50	
2	Address Setup to -AS High	25	
3	Address Hold after -AS High	25	
4	-AS High to -DS Low	50	
5	-DS Low Pulse Width	100	
6	-DS High to -AS Low	40	
7	Data Setup to -DS (Write)	25	
8	Data Hold after -DS (Write)	25	
9	-DS Low to Data Valid (Read)		50
10	-DS High to Data Invalid (Read)	0	
11	-DS High to Data Float (Read)		35

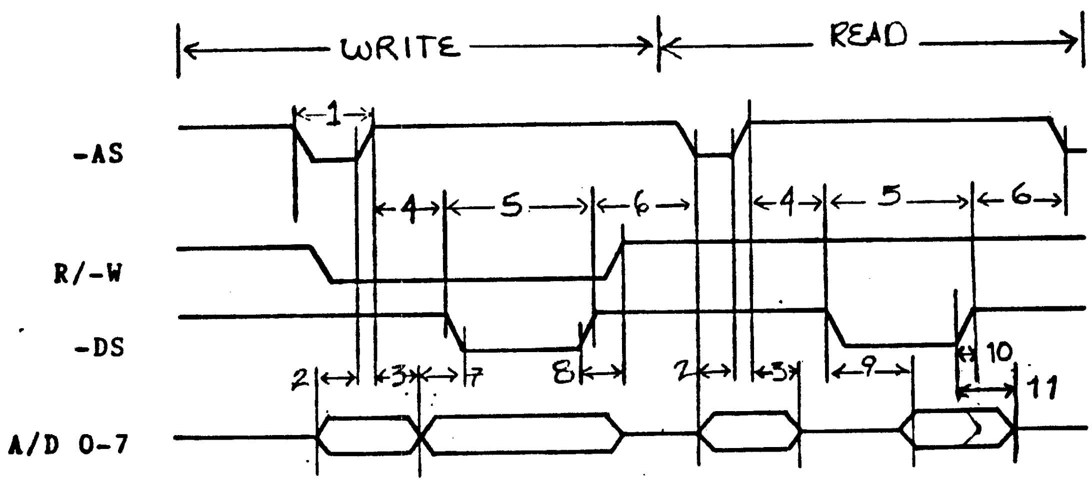


Figure 12. Z8 Mode Timing

3.3.2. 8Ø85/8Ø51 Mode Timing Characteristics (Configuration = 1)

Number	Parameter	Min (ns) (1Ø MHz)	Max (ns) (1Ø MHz)
1	ALE High Pulse Width	5Ø	
2	Address Setup to ALE Low	25	
3	Address Hold after ALE Low	25	
4	ALE Low to -IORD/-IOWR Low	5Ø	
5	-IORS/-IOWR Low Pulse Width	1ØØ	
6	Data Setup to -IOWR High	4Ø	
7	Data Hold after -IOWR High	25	
8	Data Hold after -IOWR High	25	
9	-IORD Low to Valid Data		5Ø
1Ø	-IORD High to Data Invalid	Ø	
11	-IORD High to Data Float		35

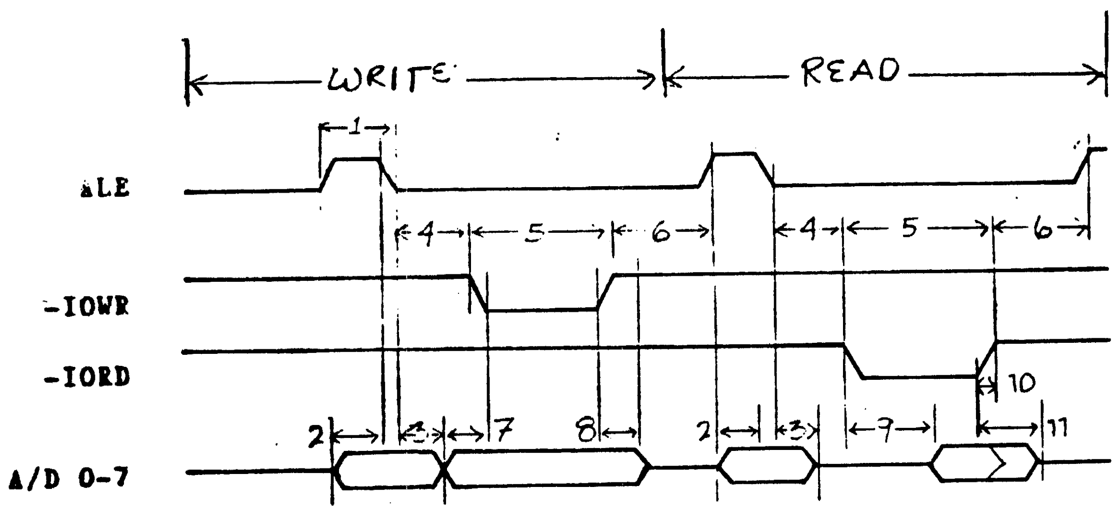


Figure 13. 8Ø85/8Ø51 Mode Timing

3.4 D.C. INFORMATION

3.4.1 Absolute Maximum Ratings

- o Voltages on all pins with respect to GND range from -0.3 V to +7.0 V.
- o Ambient operating temperature is 0°C to +70 C.
- o Storage temperature ranges from -65°C to +150 C.

Note that stresses greater than those indicated may cause permanent damage. Operation of the chip at conditions above those shown is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the chip's reliability.

3.4.2 Standard Test Conditions

The characteristics shown below apply for the following test conditions, unless otherwise noted. Voltages are referenced to GND. Positive current flows into the reference pin. Standard conditions are as follows:

- o +4.75 V < VCC < +5.25 V
- o GND = 0 V
- o 0°C < TA < +70°C

3.4.3 D.C. Characteristics

Parameter	Min	Max	Unit	Condition	Notes
Input High Voltage	2	VCC	V		
Input Low Voltage	-0.3	0.8	V		
Output High Voltage	2	VCC	V		
Output Low Voltage		0.4	V		
Input Leakage	-30	10	uA		
Output Leakage		10	uA		
VCC Supply Current		50	mA		

3.5 PACKAGE DIMENSIONS

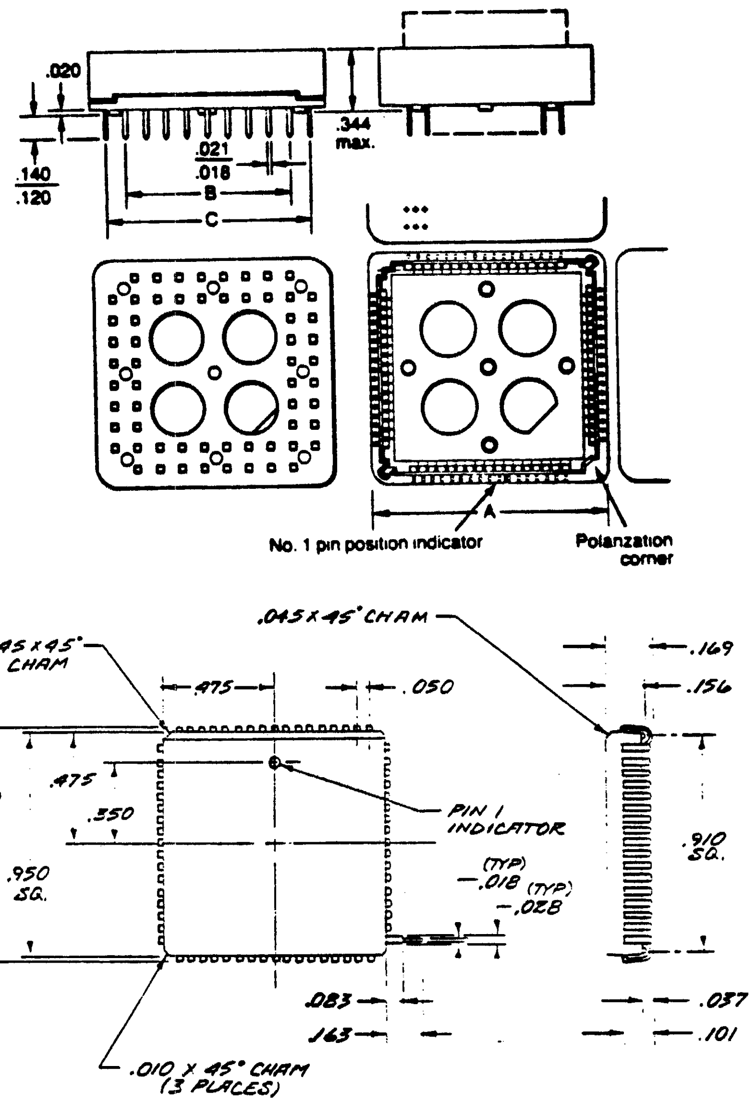


Figure 14. Socket and Package Dimensions

APPENDIX A

REGISTER SUMMARY

WRITE REGISTER 0, 4, 8, 12: MEMORY ADDRESS 0-7

Bits 7 6 5 4 3 2 1 0 — 00-FF

WRITE REGISTER 1, 5, 9, 13: MEMORY ADDRESS 8-15

Bits 7 6 5 4 3 2 1 0 — 00-FF

WRITE REGISTER 2, 6, 10, 14: WORD COUNT 0-7

Bits 7 6 5 4 3 2 1 0 — 00-FF

WRITE REGISTER 3, 7, 11, 15: WORD COUNT 8-15

Bits 7 6 5 4 3 2 1 0 — 00-FF

WRITE REGISTER 18: CHANNEL 2 CONTROL

- Bit 0: 0 = Channel Disable; 1 = Channel Enable
- Bit 1: 0 = Read RAM (Write Peripheral); 1 = Write RAM (Read Peripheral)
- Bit 2: 0 = Auto Word CT Re-Load Disabled; 1 = Auto Word CT Re-Load Enabled
- Bit 3: 0 = Channel Interrupt Disable; 1 = Channel Interrupt Enable
- Bit 4: 0 = Word Count TC = Channel Disable; 1 = Channel Always Enabled
- Bit 5: 0 = Request Low to High Edge; 1 = Request High to Low Edge
- Bit 6: 0 = Acknowledge Low Strobe; 1 = Acknowledge High Strobe
- Bit 7: 0 = Channel Req/Ack Protocol; 1 = SCSI Req/Ack Protocol

WRITE REGISTER 16: CHANNEL 0 CONTROL

- Bit 0: 0 = Channel Disable; 1 = Channel Enable
- Bit 1: 0 = Read RAM (Write Peripheral); 1 = Write RAM (Read Peripheral)
- Bit 2: 0 = Auto Word CT Re-Load Disabled; 1 = Auto Word CT Re-Load Enabled
- Bit 3: 0 = Channel Interrupt Disable; 1 = Channel Interrupt Enable
- Bit 4: 0 = Word Count TC = Channel Disable; 1 = Channel Always Enabled
- Bit 5: 0 = Request Low to High Edge; 1 = Request High to Low Edge
- Bit 6: 0 = Acknowledge Low Strobe; 1 = Acknowledge High Strobe
- Bit 7: Not Used

WRITE REGISTER 19: CHANNEL 3 CONTROL

- Bit 0: 0 = Channel Disable; 1 = Channel Enable
- Bit 1: 0 = Read RAM (Write Peripheral); 1 = Write RAM (Read Peripheral)
- Bit 2: 0 = Auto Word CT Re-Load Disabled; 1 = Auto Word CT Re-Load Enabled
- Bit 3: 0 = Channel Interrupt Disable; 1 = Channel Interrupt Enable
- Bit 4: 0 = Word Count TC = Channel Disable; 1 = Channel Always Enabled
- Bit 5: 0 = Request Low to High Edge; 1 = Request High to Low Edge
- Bit 6: 0 = Acknowledge Low Strobe; 1 = Acknowledge High Strobe
- Bit 7: Not Used

WRITE REGISTER 17: CHANNEL 1 CONTROL

- Bit 0: 0 = Channel Disable; 1 = Channel Enable
- Bit 1: 0 = Read RAM (Write Peripheral); 1 = Write RAM (Read Peripheral)
- Bit 2: 0 = Auto Word CT Re-Load Disabled; 1 = Auto Word CT Re-Load Enabled
- Bit 3: 0 = Channel Interrupt Disable; 1 = Channel Interrupt Enable
- Bit 4: 0 = Word Count TC = Channel Disable; 1 = Channel Always Enabled
- Bit 5: 0 = Request Low to High Edge; 1 = Request High to Low Edge
- Bit 6: 0 = Acknowledge Low Strobe; 1 = Acknowledge High Strobe
- Bit 7: 0 = Channel [illegible]/Ack Protocol; 1 = QIC-02 [illegible]/Ack Protocol

```
WRITE REGISTER 20:  MEMORY CYCLE TIMING

     7   6   5   4   3   2   1   0
   +-------------------------------+
   |   |   |   |   |   |   |   |   |
   +-------------------------------+
     |   |   |   |   |   |   |   |
     |   |   |   |   |   |   0   0   =  2 Clock Cycles (100 ns)
     |   |   |   |   |   |   0   1   =  3 Clock Cycles (150 ns)
     |   |   |   |   |   |   1   0   =  4 Clock Cycles (200 ns)
     |   |   |   |   |   |   1   1   =  5 Clock Cycles (250 ns)
     |   |   |   |   |   |
     |   |   |   |   |   |  _______  0 = Interrupt Low
     |   |   |   |   |   |_________  1 = Interrupt High
     |   |   |   |   |
     |___|___|___|___|_____________  Not Used


WRITE REGISTER 21:  EXTERNAL OUT STROBE 0

     7   6   5   4   3   2   1   0
   +-------------------------------+
   |   |   |   |   |   |   |   |   |
   +-------------------------------+
     |___|___|___|___|___|___|___|______   00-FF


WRITE REGISTER 22:  EXTERNAL OUT STROBE 1

     7   6   5   4   3   2   1   0
   +-------------------------------+
   |   |   |   |   |   |   |   |   |
   +-------------------------------+
     |___|___|___|___|___|___|___|______   00-FF


WRITE REGISTER 28-31:  EXTERNAL OUT GROUP STROBE

     7   6   5   4   3   2   1   0
   +-------------------------------+
   |   |   |   |   |   |   |   |   |
   +-------------------------------+
     |___|___|___|___|___|___|___|______   00-FF


READ REGISTER 0:  CHANNEL STATUS REGISTER

     7   6   5   4   3   2   1   0
   +-------------------------------+
   |   |   |   |   |   |   |   |   |
   +-------------------------------+
     |   |   |   |   |   |   |   |___ 1 = Channel 0 Enabled
     |   |   |   |   |   |   |_______ 1 = Channel 1 Enabled
     |   |   |   |   |   |___________ 1 = Channel 2 Enabled
     |   |   |   |   |_______________ 1 = Channel 3 Enabled
     |   |   |   |___________________ 1 = Channel 0 Word Count > 129
     |   |   |_______________________ 1 = Channel 1 Word Count > 129
     |   |___________________________ 1 = Channel 2 Word Count > 129
     |_______________________________ 1 = Channel 3 Word Count > 129


READ REGISTER 21:  EXTERNAL IN STROBE 0

     7   6   5   4   3   2   1   0
   +-------------------------------+
   |   |   |   |   |   |   |   |   |
   +-------------------------------+
     |___|___|___|___|___|___|___|______   00-FF


READ REGISTER 22:  EXTERNAL IN STROBE 1

     7   6   5   4   3   2   1   0
   +-------------------------------+
   |   |   |   |   |   |   |   |   |
   +-------------------------------+
     |___|___|___|___|___|___|___|______   00-FF


READ REGISTER 28-31:  EXTERNAL IN GROUP STROBE

     7   6   5   4   3   2   1   0
   +-------------------------------+
   |   |   |   |   |   |   |   |   |
   +-------------------------------+
     |___|___|___|___|___|___|___|______   00-FF
```

5060

FOUR CHANNEL MEMORY CONTROLLER

Timing Diagram

Labels

5060

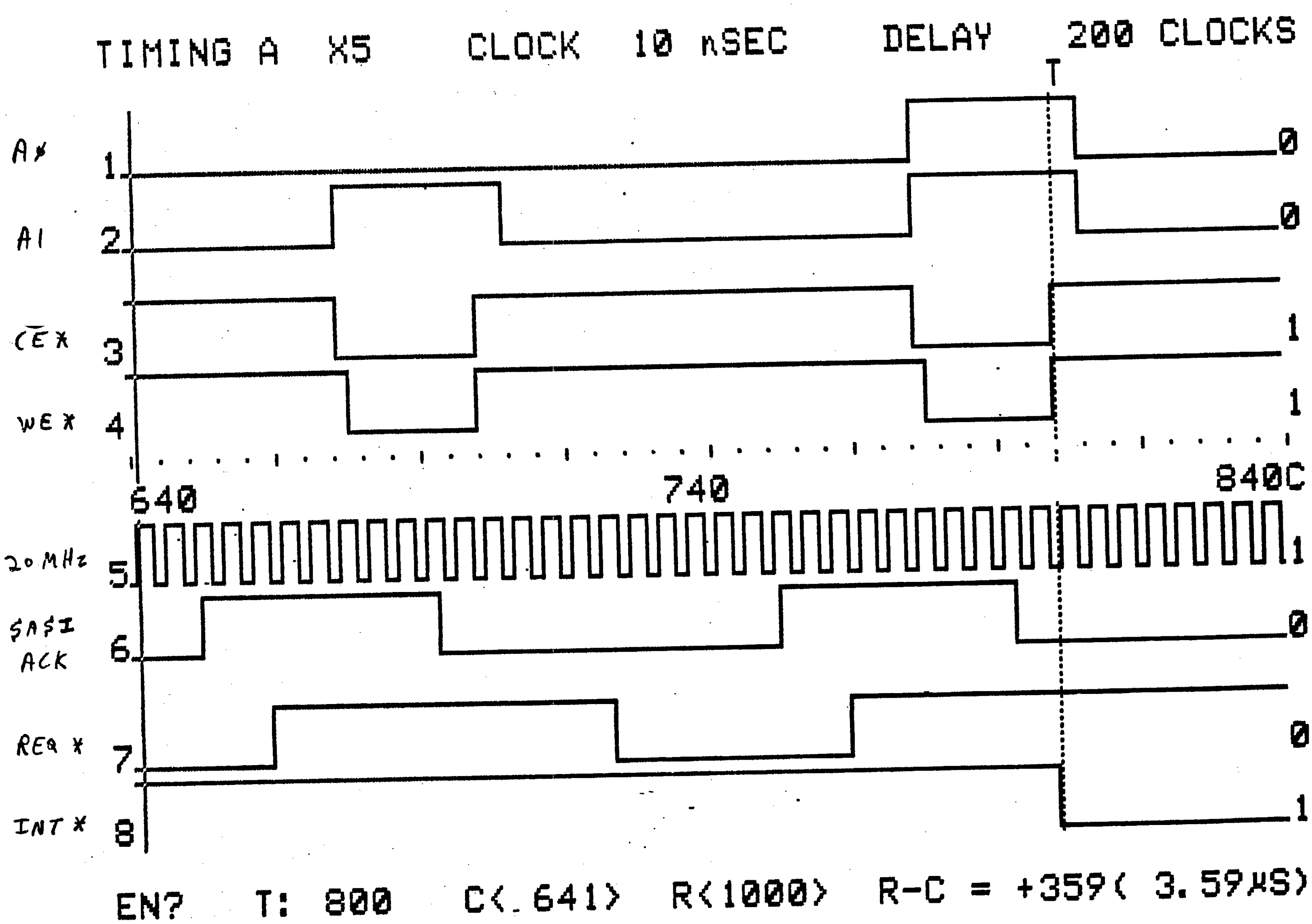
Four Channel Memory Controller

CE* — -MEMCE (pin 45)
WE* — -MEMWRT (pin 44)
AØ, A1 — MEMAØ (pin 27), MEMA1 (pin 28)
SASI ACK — REQ 2 (pin 22)
REQ* — ACK 2 (pin 21)
INT* — INTERRUPT (pin 60)
CH2 OUT CLK — pin 46

5060 DMA Chip Timing

Buffer Memory Write / Completion

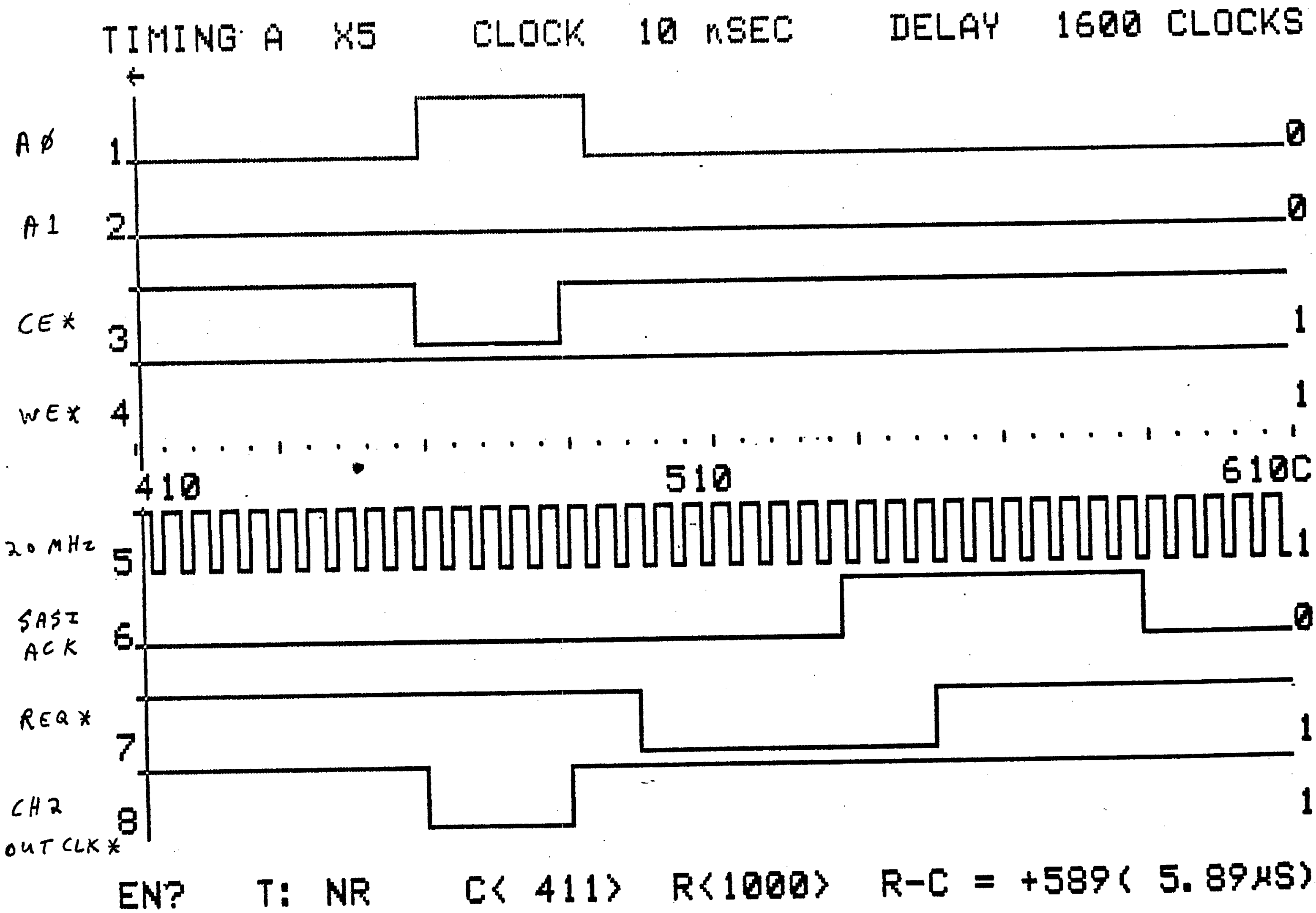
SASI Bus / Sector Buffer Timing



5060 DMA Chip Timing

Buffer Memory Read

SASI Bus / Sector Buffer Timing



NOVEMBER 03, 1983

ENCODE/DECODE/VCO

* MFM/NRZ AND NRZ/MFM CONVERSION
* ADDRESS MARK DETECTION AND GENERATION
* EXTERNALLY CONTROLLED WRITE PRECOMPENSATION
* CONTROL FOR EXTERNAL FILTER/VARACTOR
* 24 PIN .6 CENTER

```
             +--------------------+
NRZ-IN       ! 1               24 ! VCC
NRZ-OUT      ! 2               23 ! I-ADJ
RD/REF CLK   ! 3               22 ! PHASE COMP
RD GATE      ! 4               21 ! PU/-PD
WRT GATE     ! 5               20 ! VCO-OUT
2-F REF      ! 6    ENCODE     19 ! VCO-IN
A-M ENABLE   ! 7    DECODE     18 ! 1-F-DET R/C
A-M FOUND    ! 8     VCO       17 ! PRE-COMP C
DELAY OUT    ! 9               16 ! DELAY C
1F-DET       ! 10              15 ! MFM OUT
ENPRECOMP    ! 11              14 ! RD RAW
GROUND       ! 12              13 ! MODE
             +--------------------+
```

SYMBOL	TYPE	NAME AND FUNCTION
NRZ IN	I	NRZ SERIAL INPUT: THIS INPUT IS THE SERIAL NRZ OUTPUT FROM THE DISK SEQUENCER. THE INPUT MUST BE AT THE DATA RATE OF THE READ / REFERANCE CLOCK.
NRZ OUT	I	NRZ SERIAL OUTPUT: THIS OUTPUT IS THE SERIAL OUTPUT TO THE DISK SEQUENCER. THIS OUTPUT IS AT THE DATA RATE OF THE READ / REFERANCE CLOCK.
RDREF CLK	O	READ / REFERANCE CLOCK: THIS MULTIPLEXED OUTPUT IS USED BY THE DISK SEQUENCER FOR BOTH READ AND WRITE CLOCK. THE 2-F REFERANCE CLOCK / 2 WILL BE PRESENT AT THIS LINE, EXCEPT WHEN READ GATE IS TRUE. THEN THE VCO CLOCK / 2 WILL BE PRESENT AT THIS LINE.
RD GATE	I	READ GATE: THIS INPUT LINE WHEN TRUE, SELECTS THE VCO CLOCK / 2 TO BE PRESENT AT THE RD/REF CLK LINE. THE TRANSITION FROM FALSE TO TRUE, CONFIGURES THE CHIP IN "SEARCH SYNC MODE".
WRT GATE	I	WRITE GATE: THIS INPUT WHEN TRUE, ENABLES ENCODING OF NRZ SERIAL DATA TO MFM ENCODED DATA.
2-F REF	I	2-F REFERENCE CLOCK: THIS INPUT IS A FREE RUNNING CLOCK AT 2 TIMES THE DATA RATE. THIS INPUT IS USED TO GENERATE THE REFERANCE CLOCK AND TO LOCK THE VCO TO WHEN READ GATE IS FALSE.

SYMBOL	TYPE	NAME AND FUNCTION
A-M EN	I	ADDRESS MARK ENABLE: THIS INPUT WHEN TRUE WITH WRITE GATE TRUE ENCODES A SPECIAL BYTE WITH A CLOCK TRANSITION MISSING. THIS IS USED FOR BYTE SYNCRONIZATION WHEN IN READ MODE. WHEN TRUE WITH READ GATE LOCKES THE SEQUENCER FROM RESYNCING. THIS IS USED FOR EXTERNAL SYNC DETECT.
A-M FND	O	ADDRESS MARK FOUND: THIS OUTPUT IS TRUE AFTER READ GATE IS TRUE AND THE MISSING CLOCK PATTERN IS DETECTED. THIS IS USED BY THE DISK SEQUENCER FOR BYTE SYNCRONIZATION.
DELAY	O	DELAY OUTPUT: THIS TEST OUTPUT IS USED TO CALIBRATE THE 1-SHOT R/C USED FOR THE 1/4 BIT CELL DELAY CIRCUIT.
1-F DET	O	1-F DETECT: THIS TEST OUTPUT IS USED TO CALIBRATE THE RETRIGIABLE 1-SHOT R/C USED FOR THE PREAMBLE DETECT CIRCUIT.
EPC	I	ENABLE PRECOMPENSATION: WHEN HIGH THIS SIGNAL ENABLES WRITE DATA RECOMPENSATION. WHEN THIS SIGNAL IS LOW, WRITE DATA IS NOT PRECOMPENSATED.
MODE	I	MODE ENABLE: THIS INPUT WHEN LOW ENABLES THE VCO LOCK SEQUENCER TO LOCK TO DATA AFTER 1 CLOCK OF 2-F, AND ALSO SETS SAM AFTER 8 CLOCK CYCLES NOT 32.
RD RAW	I	READ RAW DATA: THIS INPUT IS THE ENCODED DATA OUTPUT FROM THE DISK DRIVE.

SYMBOL	TYPE	NAME AND FUNCTION
MFM OUT	O	MFM WRT DATA: THIS LINE IS THE MFM ENCODED DATA OUTPUT WHEN WRITE GATE IS TRUE.
DEL C	I/O	DELAY C: THIS I/O LINE IS FOR CONNECTING A VARIABLE CAPACITOR USED FOR THE 1/4 BIT CELL DELAY.
1-F DET	I/O	1-F DETECT C R/C: THIS I/O LINE IS FOR CONNECTING AN R/C FOR THE RETRIGERABLE ONE SHOT USED IN DETECTING THE 1-F USED FOR VCO SYNC IN THE PREAMBLE.
VCO IN	I	VCO INPUT: THIS INPUT IS THE OUTPUT OF THE VCO CONTROLLED BY THE CHARGE-PUMP DELAY OF THE VCO OUTPUT.
VCO OUT	O	VCO OUTPUT: THIS OUTPUT IS USED FOR THE VCO SOURCE WITH THE DELAY CONTROLLED BY THE CHARGE-PUMP,AND FEED-BACK IN THE VCO INPUT.
PU/-PD	O	FILTER SOURCE/-SINK: THIS TRI-STATE OUTPUT WILL BE ENABLED HIGH WHEN PHASE COMPARATOR REQUIRES A VCO INCREASE IN FREQUENCY, AND WILL BE ENABLED LOW WHEN THE PHASE COMPARATOR REQUIRES A VCO DECREASE IN FREQUENCY.
P-C C	I/O	PRECOMP C: THIS I/O LINE IS FOR CONNECTING AN EXTERNAL CAPACITOR USED FOR THE WRITE PRECOMP DELAY TIME IF PRECOMP IS ENABLED.

OMTI
557 SALMAR AVE.
CAMPBELL, CALIFORNIA 95008
(408) 370-3555

PRODUCT SPECIFICATION

for

OMTI PFM 5070 VCO/ENCODE/DECODE CHIP

MAY 1984

OMTI PFM 5070 VCO/ENCODE/DECODE CHIP
PRODUCT SPECIFICATION
(PART #20507)

REV.	REVISION HISTORY	PRINT DATE
	Original Issue	May 18 1984

TABLE OF CONTENTS

Page Number

LIST OF ILLUSTRATIONS

LIST OF TABLES

CHAPTER 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

The OMTI PFM 5070 VCO/Encode/Decode chip provides all of the necessary functions needed to convert disk drives with MFM serial data interfaces (i.e., ST506/412, SA1000) to NRZ data and clock. It contains an internal voltage controlled oscillator, phase-locked loop, encode/decode logic, Address Mark generation and detection, and all the circuitry required for write precompensation.

The PFM 5070 is capable of operation at data rates up to 10 megabits per second by proper selection of the external frequency and loop gain components. The need for delay lines is eliminated by selecting write precompensation values with a constant current controlled RC network.

1.2 5070 VCO/ENCODE/DECODE CHIP CAPABILITIES

* Data rate control to 10 megabits per second
* No external logic required
* Internal VCO and phase-locked loop
* MFM to NRZ and NRZ to MFM conversion
* Internal address mark detection and generation circuitry
* Externally controlled write precompensation
* Internal early, on time, and late timing
* Control for external filter/varactor
* 24-pin plastic package

1.3 FUNCTIONAL OVERVIEW

Figure 1 illustrates the internal block diagram of the PFM 5070 VCO/Encode Decode chip. Each logic block is discussed in the following sections.

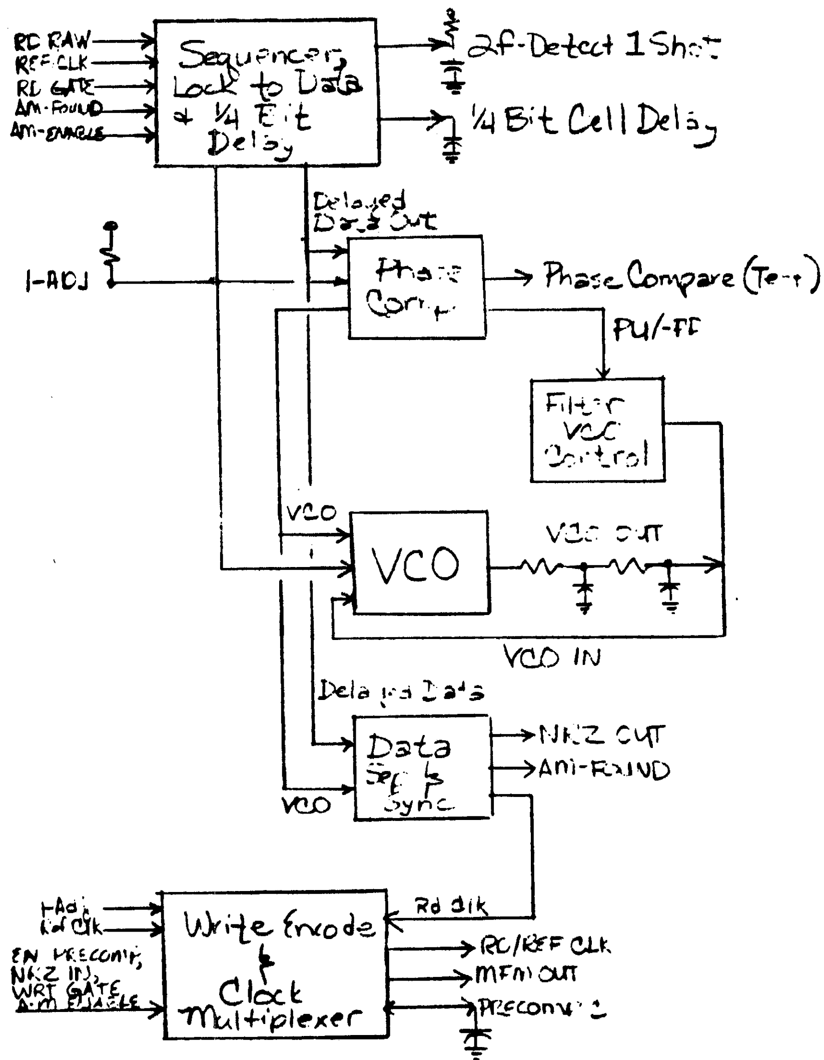


Figure 1. Internal Block Diagram

1.3.1 Sequencer, Lock to Data and 1/4-Bit Delay

This block delays the raw data from the disk by 1/4-bit cell time in preparation for use by the Phase Comparator. It also provides the A-M FOUND signal to the Data Sequencer, which allows it to lock on the data. Figure 2 contains a flow chart describing the Search Sync mode and AM Detect operations performed by this block.

1.3.2 Phase Comparator

The Phase Comparator compares the phase and frequency of the incoming signal with the VCO frequency, and generates an error voltage that is related to the phase and frequency difference between the two signals. The PU/-PD (Pump-Up/Pump-Down) signal communicates the result of the comparison to the VCO via the Filter VCO Control.

1.3.3 Filter VCO Control

The Filter VCO Control attenuates the high-frequency error components of the PU/-PD and inputs the corrected signal to the VCO (via the VCO IN line).

1.3.4 VCO

The Voltage Controlled Oscillator is a voltage to frequency converter used to provide a clock which is at the same frequency and phase as the raw data. The clock's frequency is determined by the PU/-PD signal.

1.3.5 Data Separator and Synchronization

The Data Separator and Synchronization block generates the NRZ output from the delayed data and the clock generated by the VCO.

1.3.6 Write Encode and Clock Multiplexer

This block converts NRZ data (from the Data Sequencer) into an MFM (Modified Frequency Modulated) data stream. The derived MFM signal can then be used to record information on the disk. When AM-ENABLE is active, a clock pulse will be deleted in the outgoing MFM stream in order to record Address Marks on the disk. In addition, precompensation signals are generated, when needed, for use in recording inner tracks.

SEQUENCE AFTER RD GATE TRUE EDGE:

1. Wait for 8 read raw pulses at high frequency; if not, retriggerable 1-shot will time-out and restart sequence.
2. Set lock to data: disable VCO for 2 read raw pulses and start VCO in phase with read raw.
3. Wait for 24 more read raw pulses at high frequency; if not, retriggerable 1-shot will time-out and restart sequence.
4. Set Search Address Mark and output VCO/2 to RD/REF clock. Wait for a "1" or 96 more read raw pulses. If no "1", restart sequence.
5. If "1" is detected, Adress Mark Found and lock up or 12 raw read pulses and restart sequence.

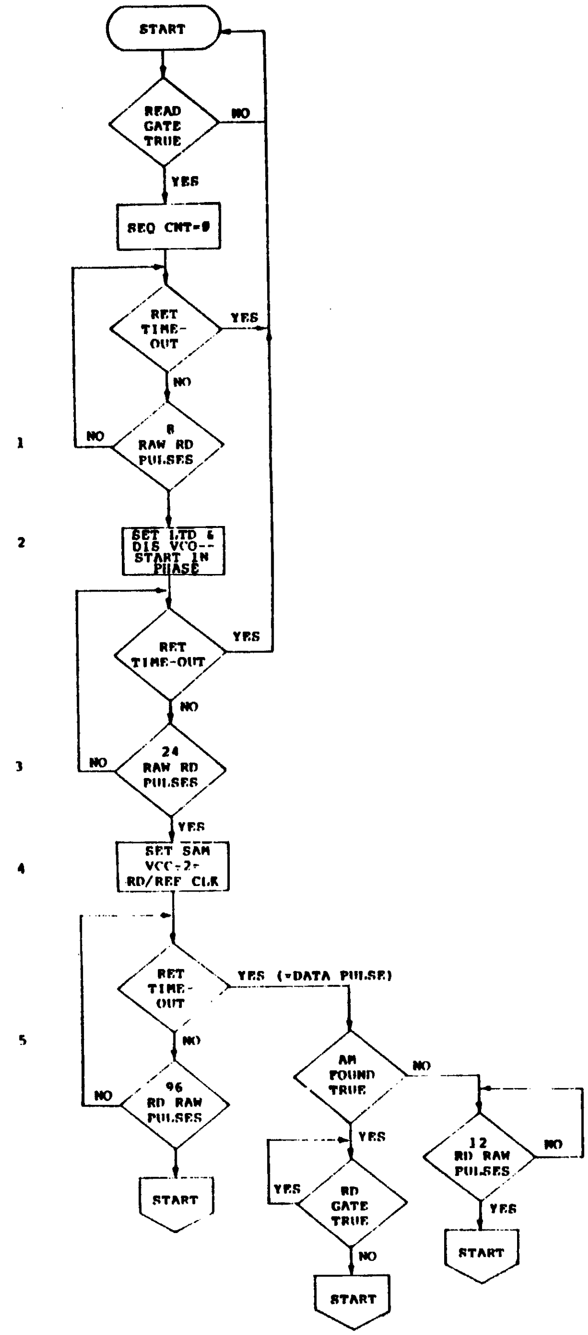


Figure 2. Flow Chart of Search Sync Mode

1.4 SYSTEM CONFIGURATION

Illustrated below is a typical system configuration, incorporating the VCO/Encode/Decode chip, the 5050 Data Sequencer, and the 5060 Memory Controller. Figure 4 shows all the external RC circuitry for a standard 5 MHz interface.

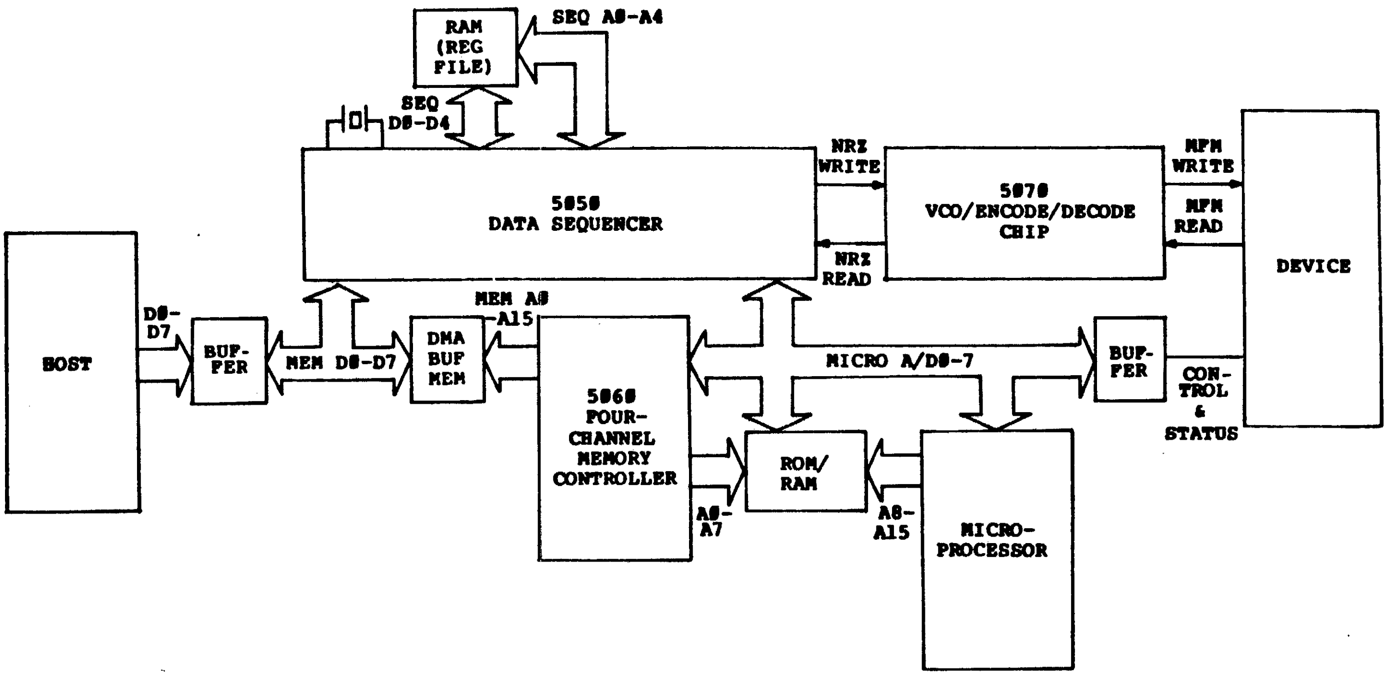


Figure 3. Typical System Configuration

1.4.1 Disk Interface

The disk interface consists of the MFM OUT line containing MFM-encoded data written to the disk, and the RD RAW line containing the MFM-encoded data to be translated to NRZ and input to the Data Sequencer.

1.4.2 Data Sequencer Interface

Three pairs of lines connect the 5070 with the 5050 Data Sequencer. These lines serve to transmit NRZ serial data between the two chips, enable the encoding and decoding of Address Marks, and provide various clock pulses to coordinate the data transfer.

1.4.3 Microprocessor Interface

The ENPRECOMP signal from the microprocessor enables precompensation for write operations on inner disk tracks.

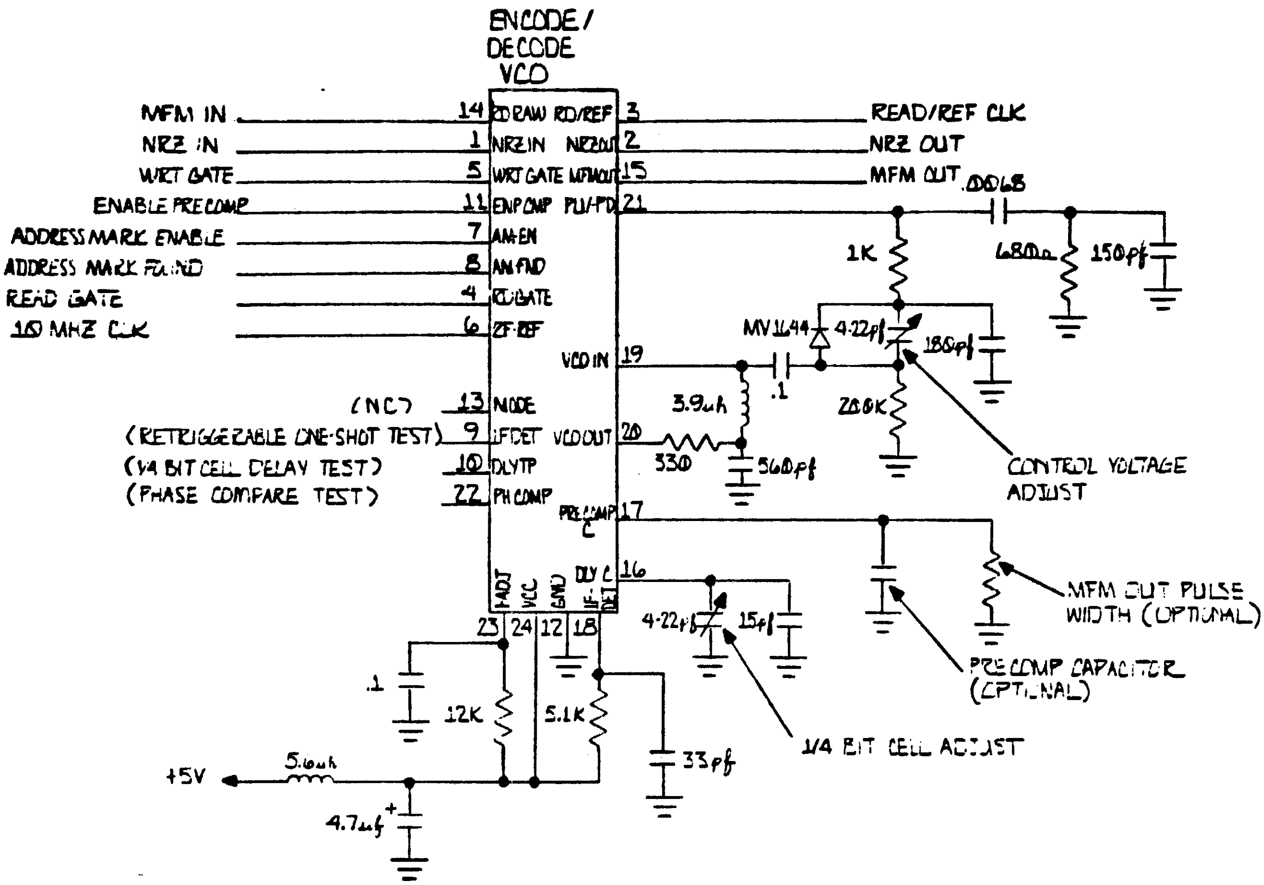


Figure 4. VCO Encode/Decode External RC Circuitry

CHAPTER 2

INTERFACING

2.1 SIGNAL DESCRIPTIONS

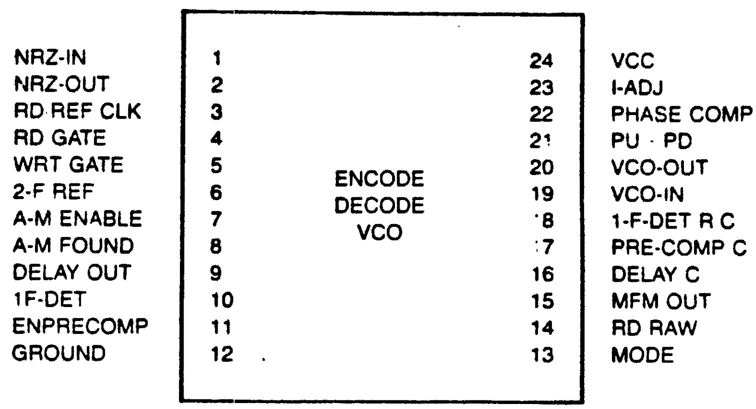


Figure 5. Pin Assignments

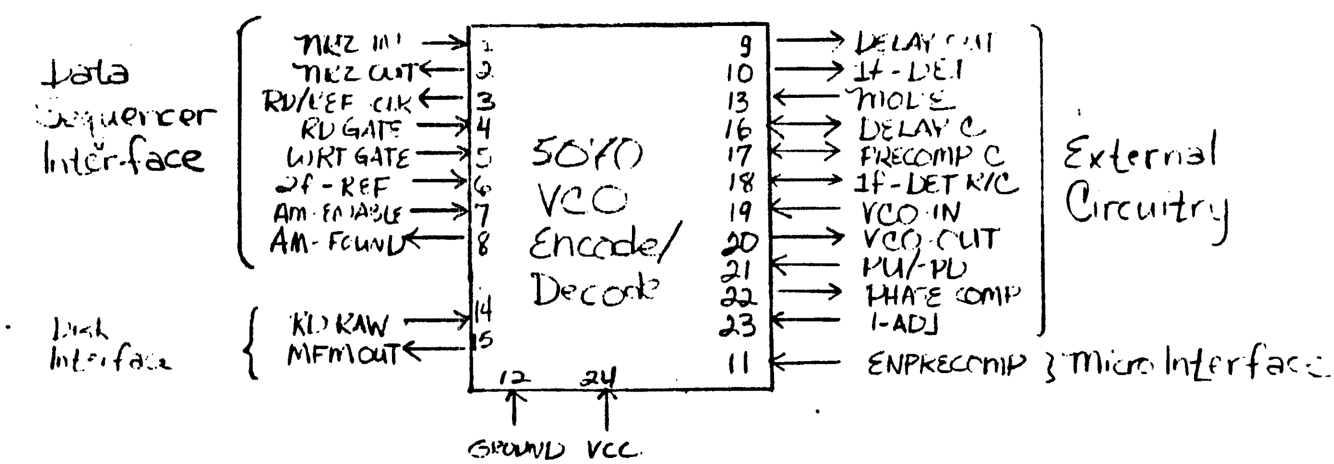


Figure 6. Pin Functions

Table 1. Pin Descriptions

Symbol	Type	Pin #	Name and Function
1-F DET	O	10	1-f Detect. (Active High.) This test output is used to calibrate the retriggerable One-Shot RC used for the Preamble detect circuit.
1-F DET RC	I/O	18	1-f Detect Connect RC. (Active High.) This I/O line is connected to the junction point between a resistor to VCC and a capacitor to GND. This circuit is used for the retriggerable One-Shot that detects the 1-f used for VCO sync in the Preamble.
2-F REF	I	6	2-f Reference Clock. (Active High.) When RD GATE is false, this signal is divided by 2 and output on the RD/REF clock line.
A-M ENABLE	I	7	Address Mark Enable. (Active High.) When both this signal and WRT GATE are active, A-M ENABLE encodes an Address Mark (a special byte with a missing clock pulse). When A-M ENABLE is true and RD GATE is active, the Data Sequencer is locked from resyncing, thus placing the sequencer in external sync detect mode.
A-M FOUND	O	8	Address Mark Found. (Active High.) This output line goes High after RD GATE goes High and the missing clock pattern of the Address Mark is detected. The Data Sequencer uses this signal for byte synchronization during Read operations.
DELAY C	I/O	16	Delay Cell. (Active High.) This I/O pin is connected to a variable capacitor used to generate the 1/4-bit cell delay.
DELAY OUT	O	9	Delay Output. (Active High.) This test output is used to calibrate the One-Shot RC used for the 1/4-bit cell delay circuit.
ENPRECOMP	I	11	Enable Precompensation. (Active High.) When active, this signal enables precompensation for disk write operations on inner tracks. When this signal is inactive, write precompensation is disabled.

Table 1. Pin Descriptions, continued

Symbol	Type	Pin #	Name and Function
I-ADJ	I	23	Input Adjust. (Active High.) This input provides the current reference for all constant current controlled elements of the chip, i.e. phase comparator, PU/-PD signal, 1/4 bit cell delay, and write precompensation circuitry. An external fixed resistor from 5 V connected to this pin determines the constant current value.
MFM OUT	O	15	MFM Write Data. (Active High.) This signal is the MFM-encoded data output when WR GATE is active.
MODE	I	13	Mode Enable. (Active High.) When Low, this signal enables the VCO lock sequencer to lock to data after 1 clock of 2-f, and also sets Search Address Mode after 8, rather than 32, clock cycles.
NRZ IN	I	1	NRZ Serial Input. (Active High.) This serial data input line is the output from the Data Sequencer. This input must be at the data rate of the read/reference clock.
NRZ OUT	O	2	NRZ Serial Output. (Active High.) This signal is the serial output to the Data Sequencer. This signal must be at the data rate of the read/reference clock.
PHASE COMP	O	22	Phase Compare. (Active High.) This output is used for calibration of the 1/4-bit cell delay.
PRECOMP C	I/O	17	Precomp Capacitor. (Active High.) This I/O line is connected to an external capacitor used to generate the write precompensation delay time when precompensation is enabled.
PU/-PD	I	21	Filter Source/-Sink. (Filter Source active High; -Sink active Low; 3-state.) This 3-state output will be enabled High when the phase comparator requires a VCO increase in frequency, and will be enabled Low when the phase comparator requires a VCO decrease in frequency. The active High or Low current source/sink is proportional to the I-ADJ signal.

Table 1. Pin Descriptions, continued

Symbol	Type	Pin #	Name and Function
RD GATE	I	4	Read Gate. (Active High.) The transition of this signal from Low to High configures the chip in Search Sync mode (see Figure 4). During the Search for Address Mark phase of the Search Sync mode (VCO is locked), this signal selects the VCO clock/2 to be present at the RD/REFCLK line.
RD RAW	I	14	Read Raw Data. (Active High.) This input is the raw data containing both clock and data pulses output from the disk drive.
RD/REFCLK	O	3	Read/Reference Clock. (Active High.) This multiplexed output is used by the Data Sequencer for both read and write clock. The 2-f reference clock/2 will be present at this line when RD GATE is false. When RD GATE is true during the Search for Address Mark phase (VCO is locked), the VCO clock/2 will be present at this line.
VCO IN	I	19	VCO Input. (Active High.) This signal is the output of the VCO controlled by the charge-pump delay of the VCO output.
VCO OUT	O	20	VCO Output. (Active High.) This signal is used for the VCO source with the delay controlled by the charge-pump, and feed-back in the VCO input.
WRT GATE	I	5	Write Gate. (Active High.) When active, this signal enables encoding of NRZ serial data to MFM encoded data.
VCC	I	24	VCC. +5 V.
GND	I	12	Ground.

2.2 TIMING

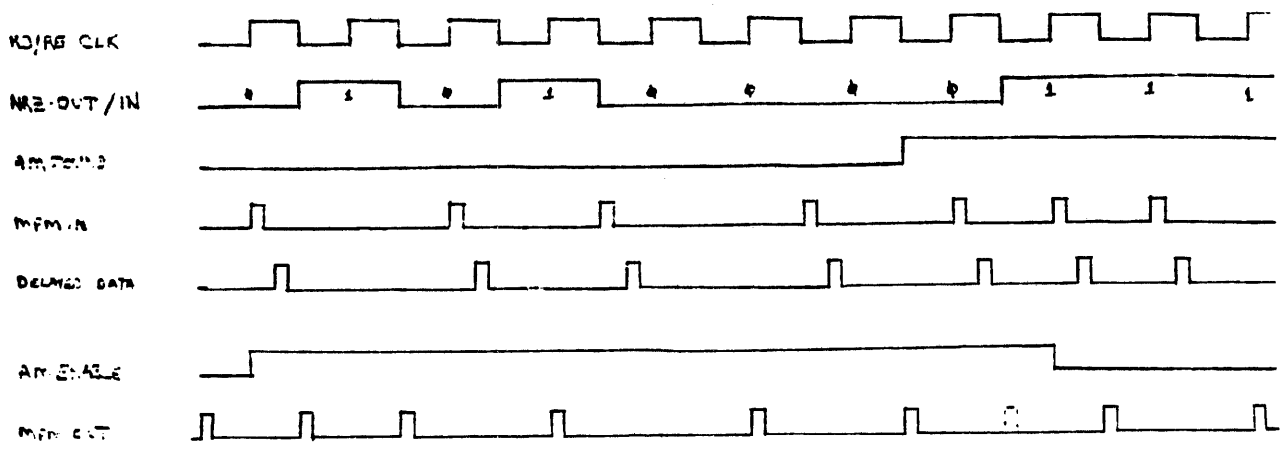


Figure 7. VCO/Encode/Decode Timing

2.3 D.C. INFORMATION

2.3.1 Absolute Maximum Ratings

- o Voltages on all pins with respect to GND range from -Ø.3 V to +7.Ø V.
- o Ambient operating temperature is Ø°C to +7Ø°C.
- o Storage temperature ranges from -65°C to +15Ø°C.

Note that stresses greater than those indicated may cause permanent damage. Operation of the chip at conditions above those shown is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the chip's reliability.

2.3.2 Standard Test Conditions

The characteristics shown below apply for the following test conditions, unless otherwise noted. Voltages are referenced to GND. Positive current flows into the reference pin. Standard conditions are as follows:

- o +4.75 V < VCC < +5.25 V
- o GND = Ø V
- o Ø°C < TA < +7Ø°C

2.3.3 D.C. Characteristics

Parameter	Min	Max	Unit	Condition	Notes
Input High Voltage	2	VCC	V		
Input Low Voltage	-0.3	0.8	V		
Output High Voltage	2	VCC	V		
Output Low Voltage		0.4	V		
Input Leakage	-30	10	uA		
Output Leakage		10	uA		
VCC Supply Current		50	mA		

2.4 PACKAGE DIMENSIONS

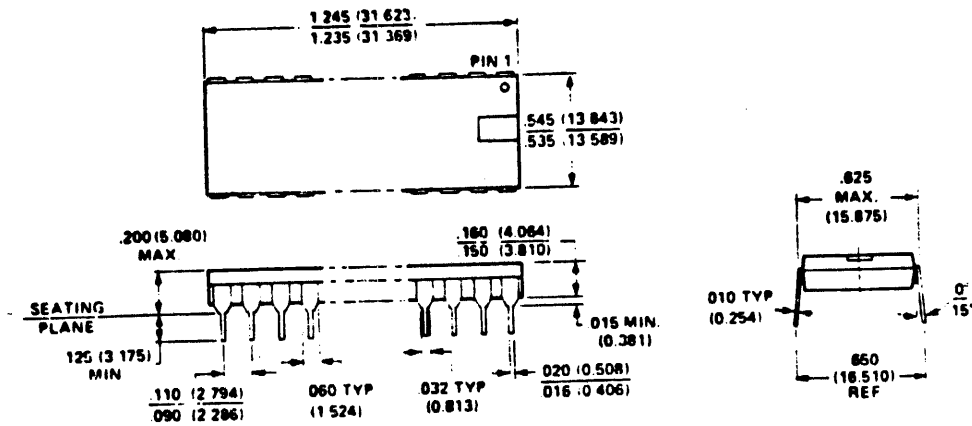


Figure 8. Package Dimensions

5070

VCO

ENCODE/DECODE

Timing Diagram
Labels

5070
VCO Encode / Decode

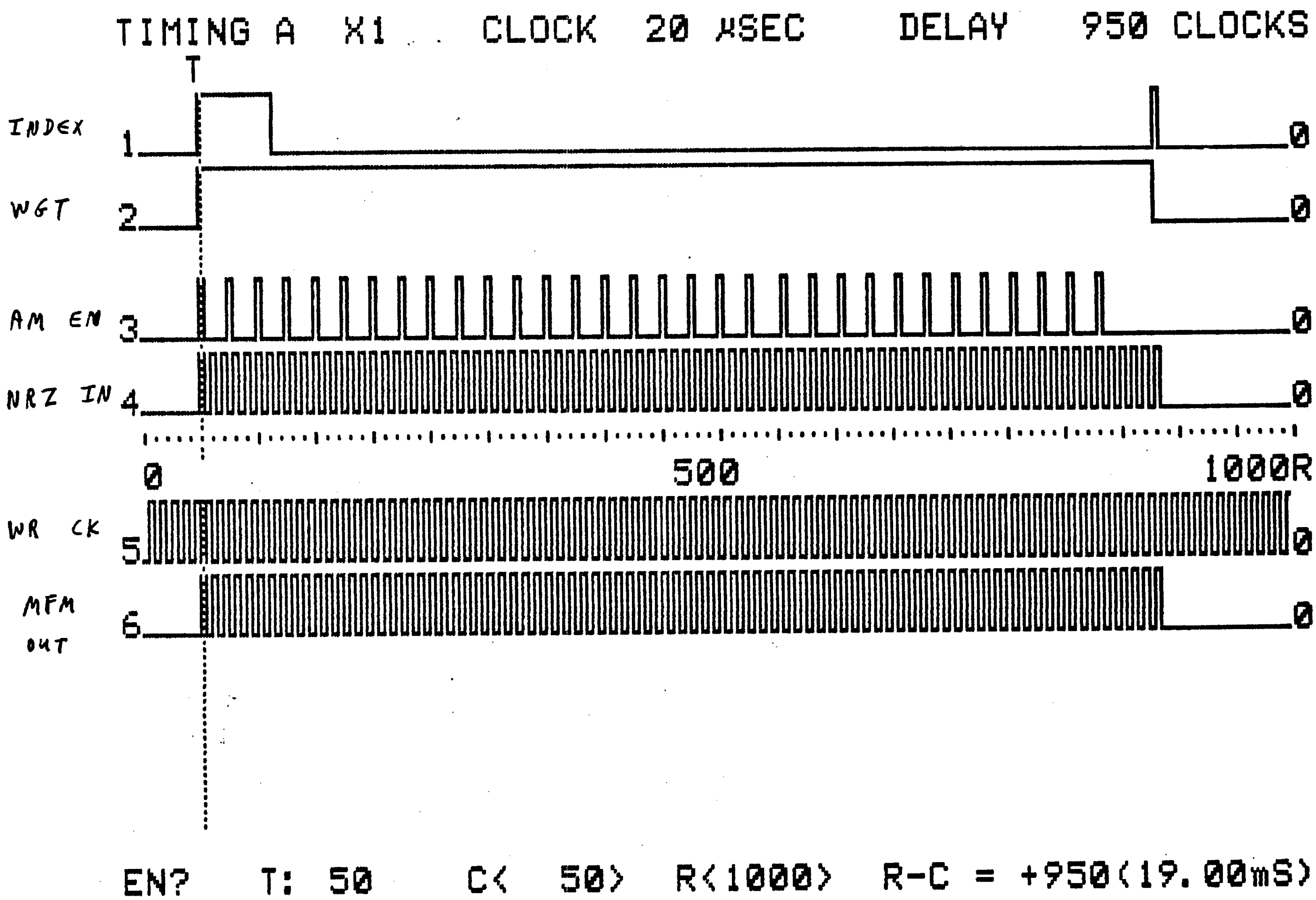
AM EN — AM ENABLE (pin 7)
RD CK — RD REF CLK (pin 3)
WGT — WRT GATE (pin 5)
WR CK — 2F REF (pin 6)
HF DETECT — IF DET (pin 10)
AM FND — AM FOUND (pin 8)
RAW RD — RD RAW (pin 14)
VCO IN — pin 19
VCO OUT — pin 20
NRZ IN — pin 1
NRZ OUT — pin 2
MFM OUT — pin 15
PHASE COMP — pin 22
PU/PD — pin 21
RD GATE — pin 4

5070 VCO Chip Timing

Format Track

Whole Track
Displayed

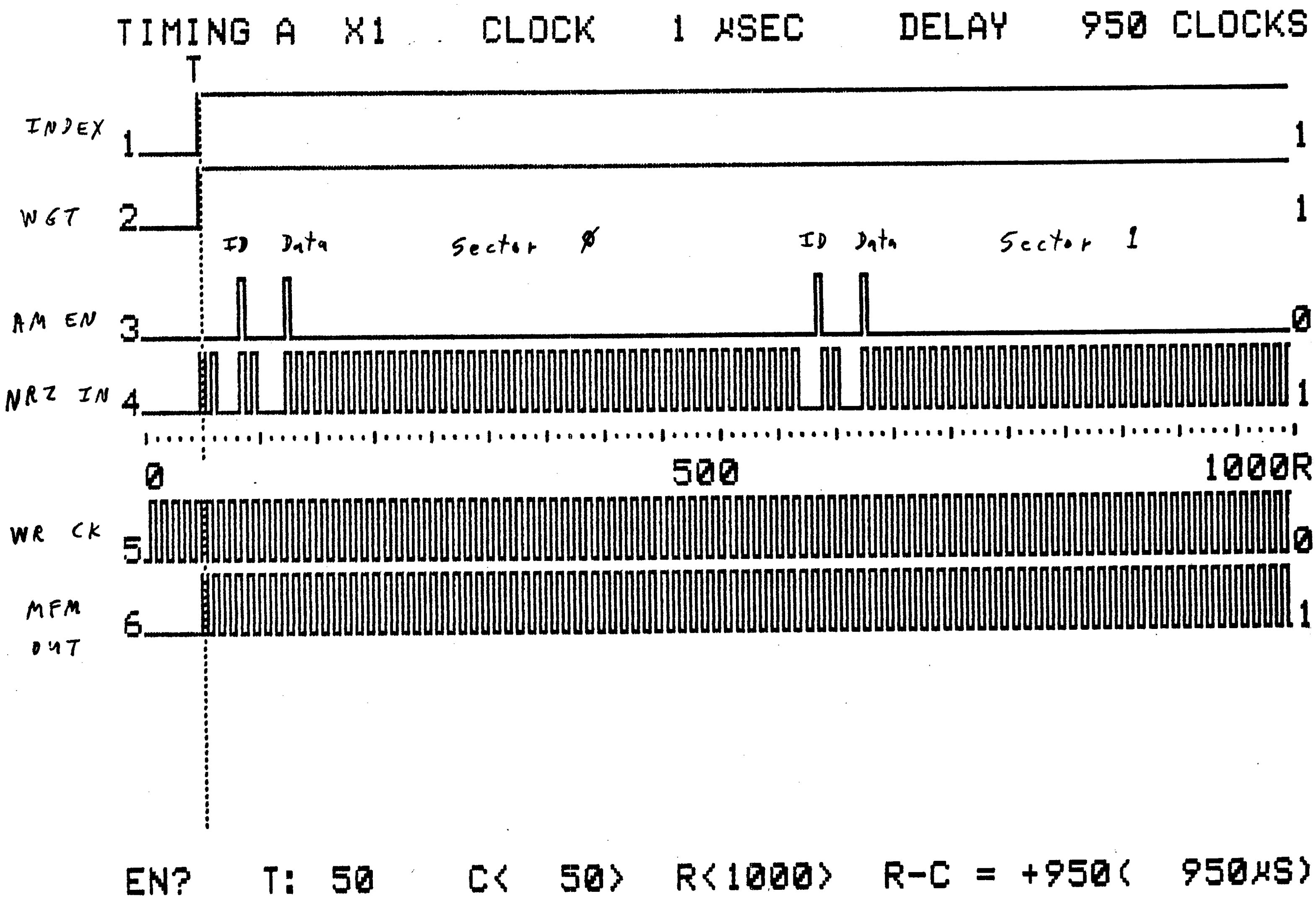
32 Sectors /256 bytes



5070 VCO Chip Timing

Format Track

First
Two Sectors
Displayed

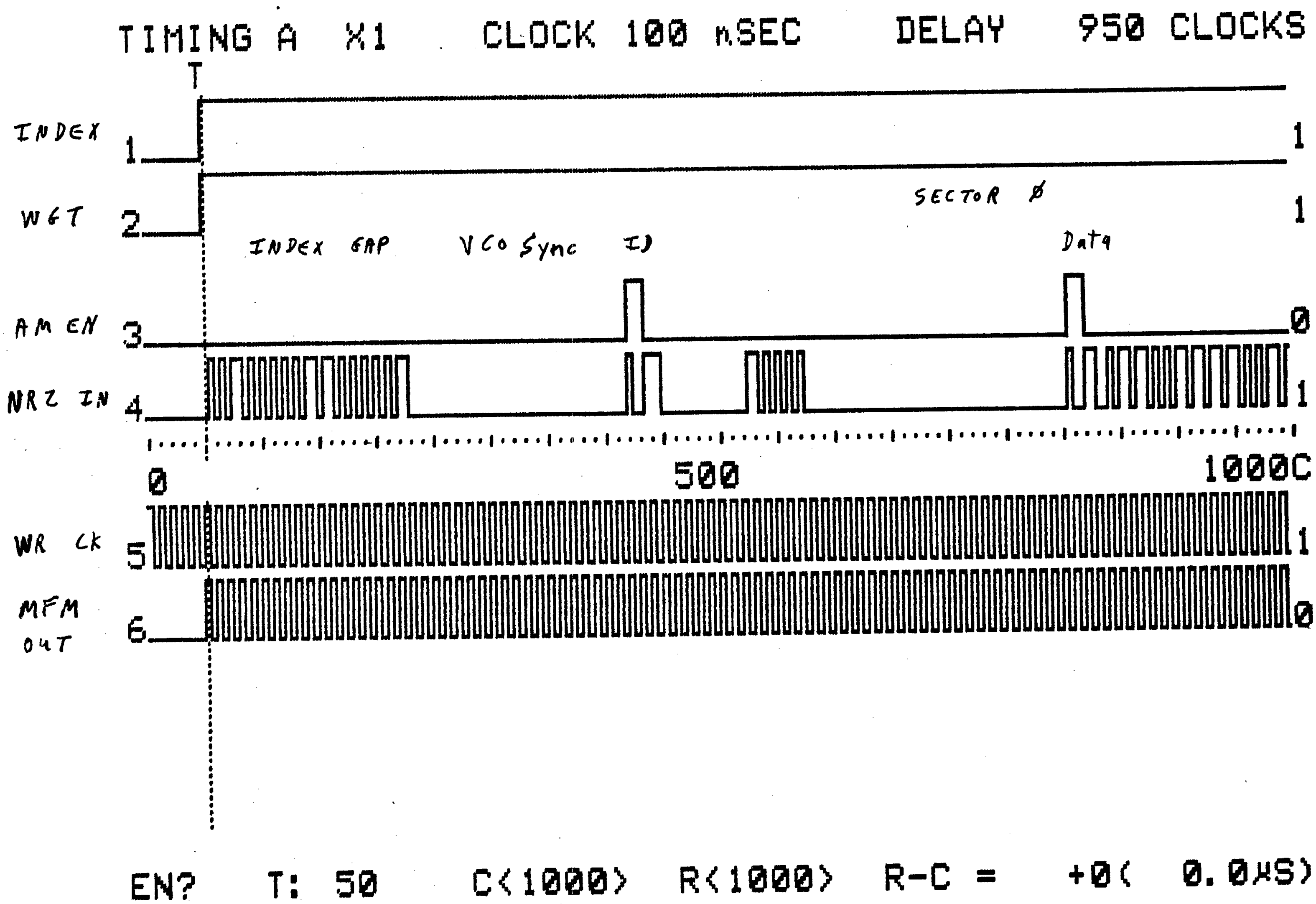


5070 VCO Chip Timing

Format Track

First Sector

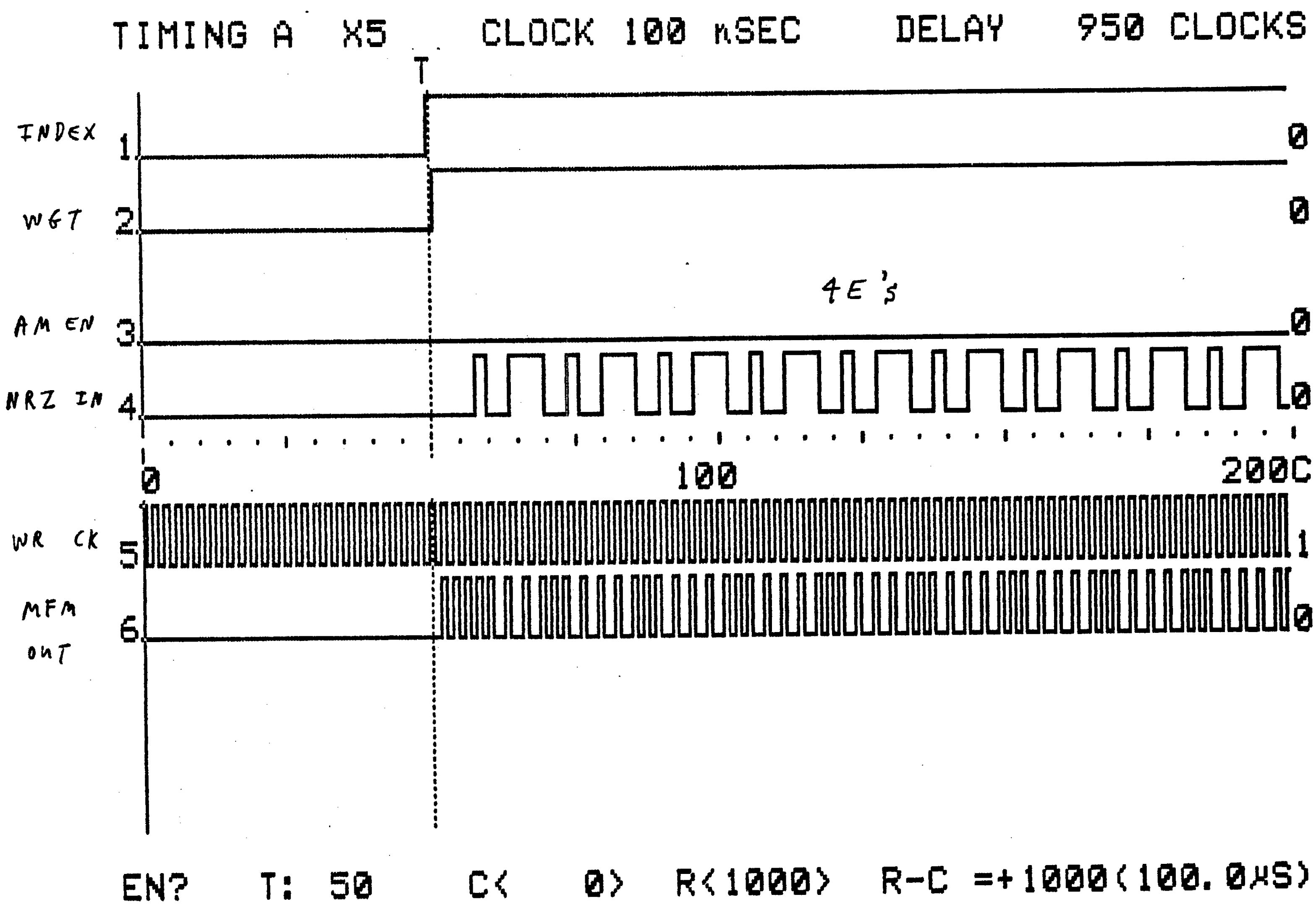
Index Gap, Sector Ø ID
and Beginning Data Fields



5070 VCO Chip Timing

Format Track

Index Gap

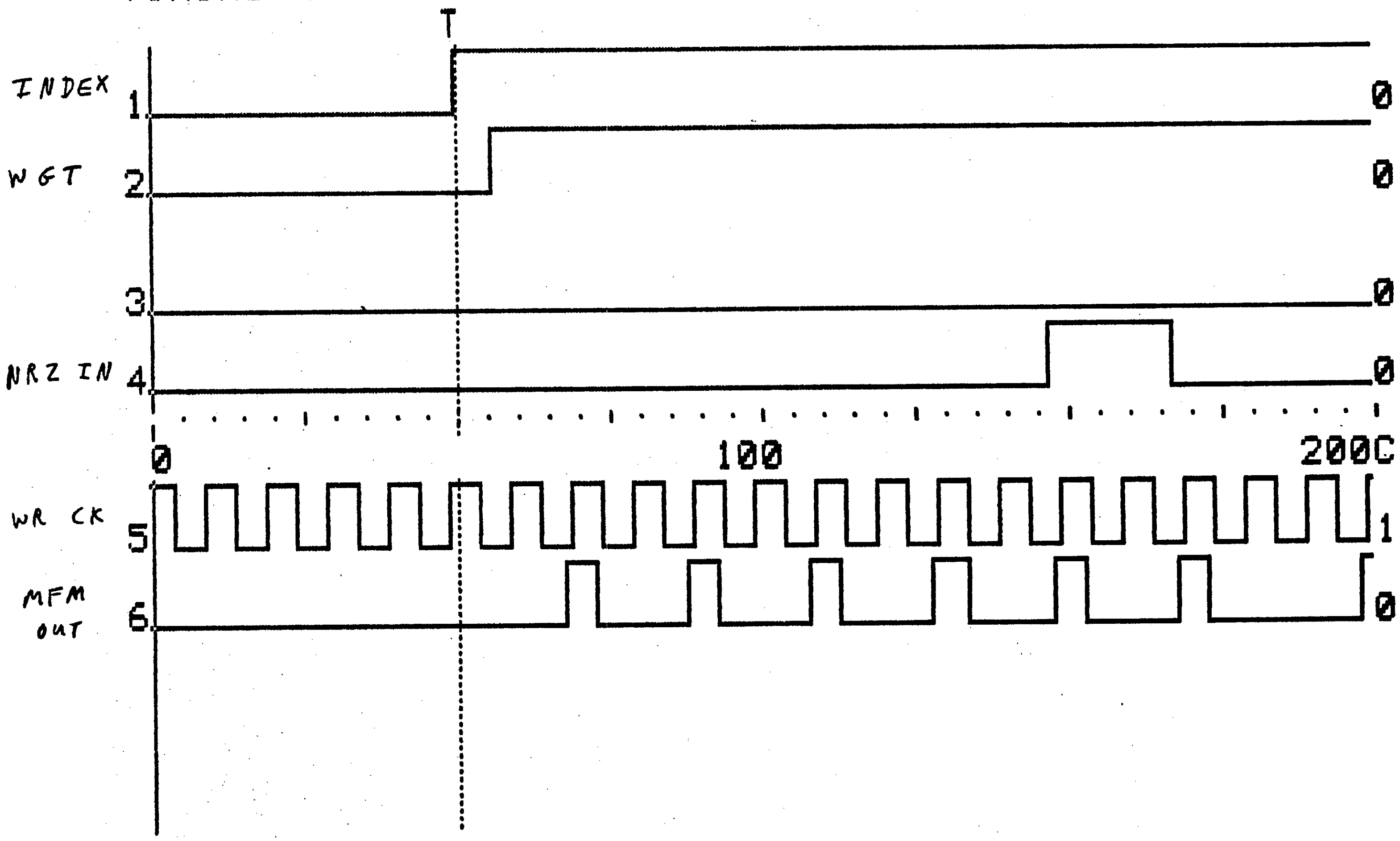


5070 VCO Chip Timing

Format Track

Index Gap Write

TIMING A X5 CLOCK 10 nSEC DELAY 950 CLOCKS



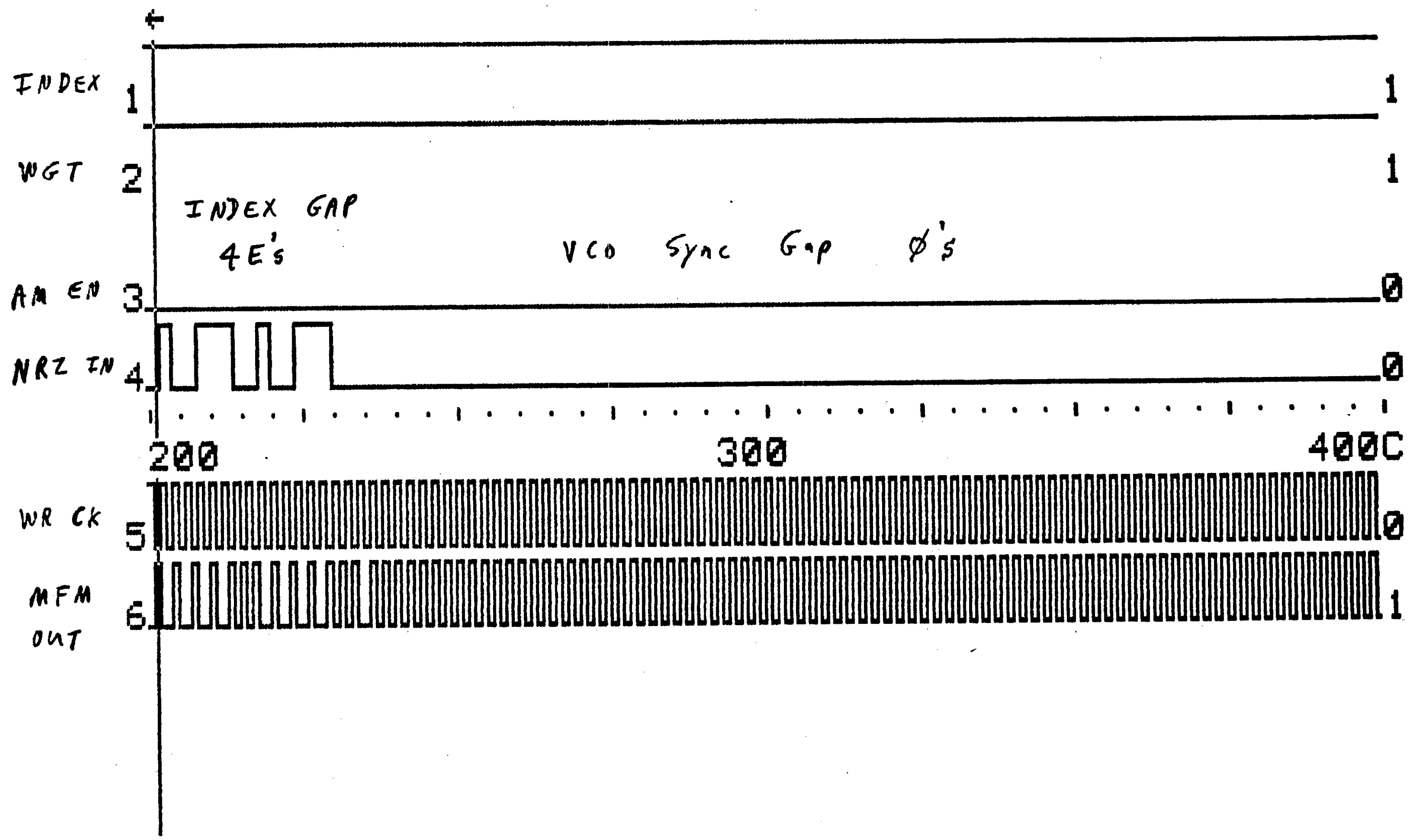
EN? T: 50 C< 0> R<1000> R-C =+1000(10.00µS)

5070 VCO Chip Timing

Format Track

VCO Sync Gap

TIMING A X5 CLOCK 100 nSEC DELAY 950 CLOCKS

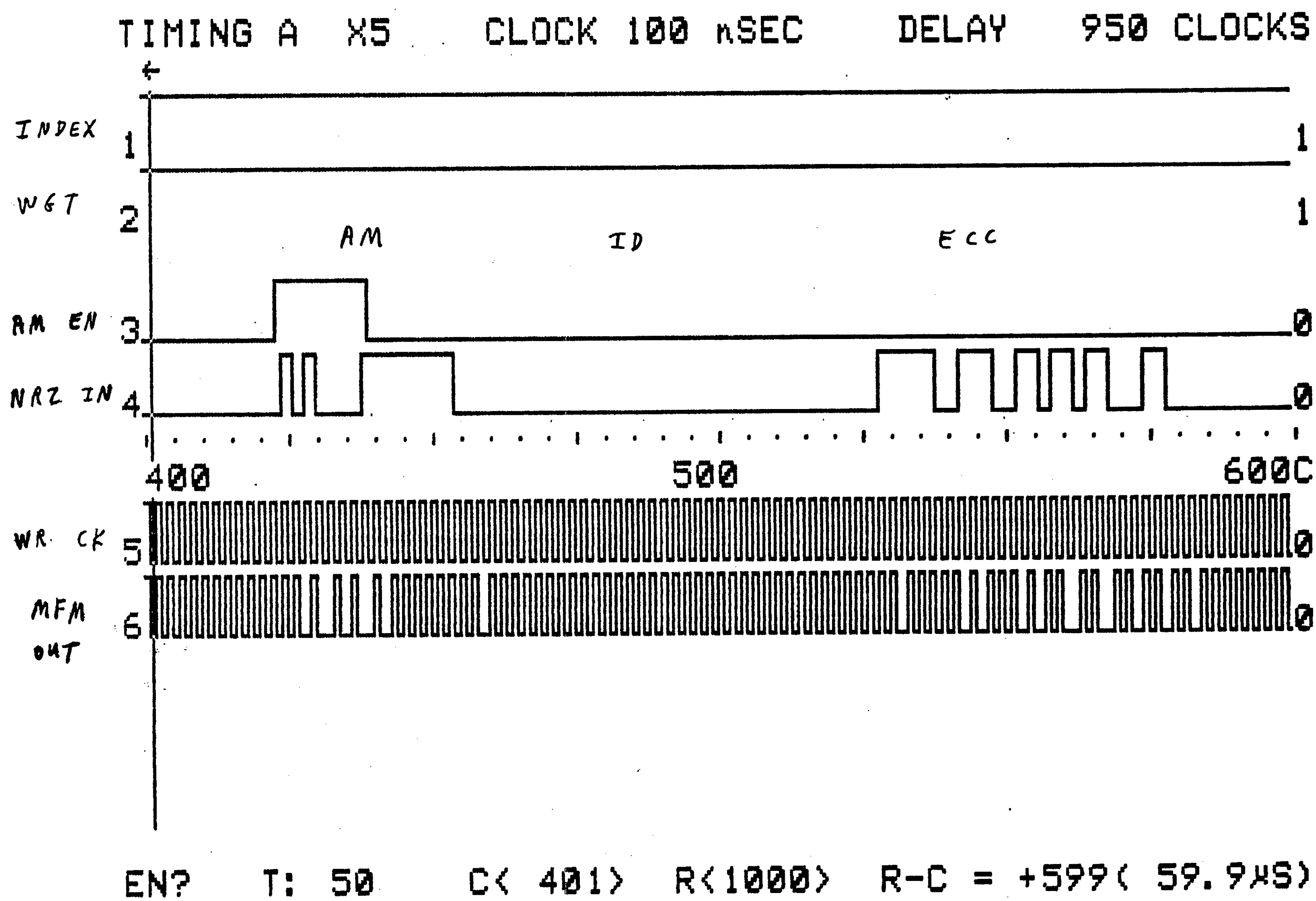


EN? T: 50 C< 201> R<1000> R-C = +799(79.9µS)

5070 VCO Chip Timing

Format Track

ID Field

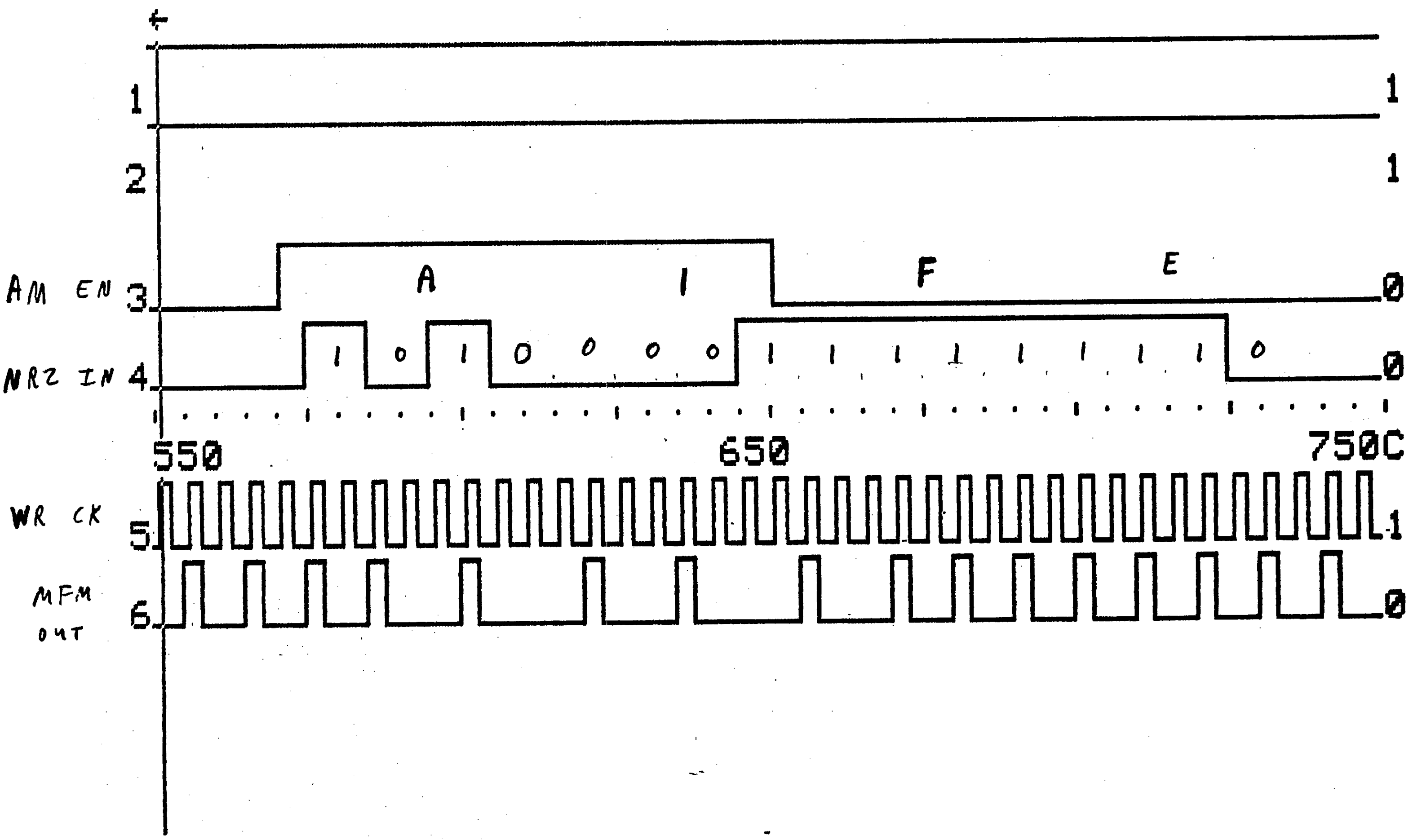


5020 VCO Chip Timing

Format Track

Write ID AM

TIMING A X5 CLOCK 20 nSEC DELAY 2300 CLOCKS

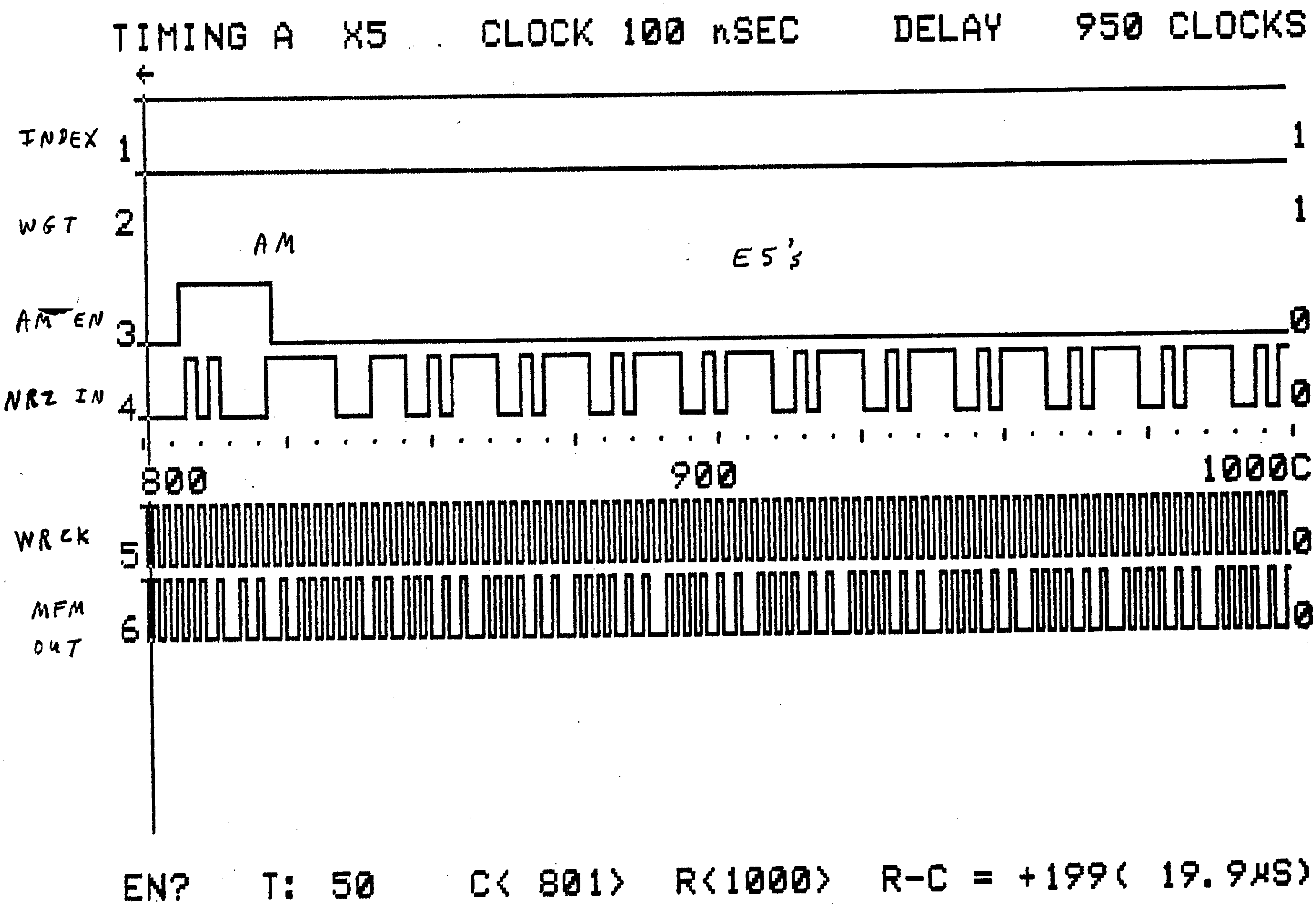


EN? T: NR C< 551> R<1000> R-C = +449(8.98µS)

5070 VCO Chip Timing

Format Track

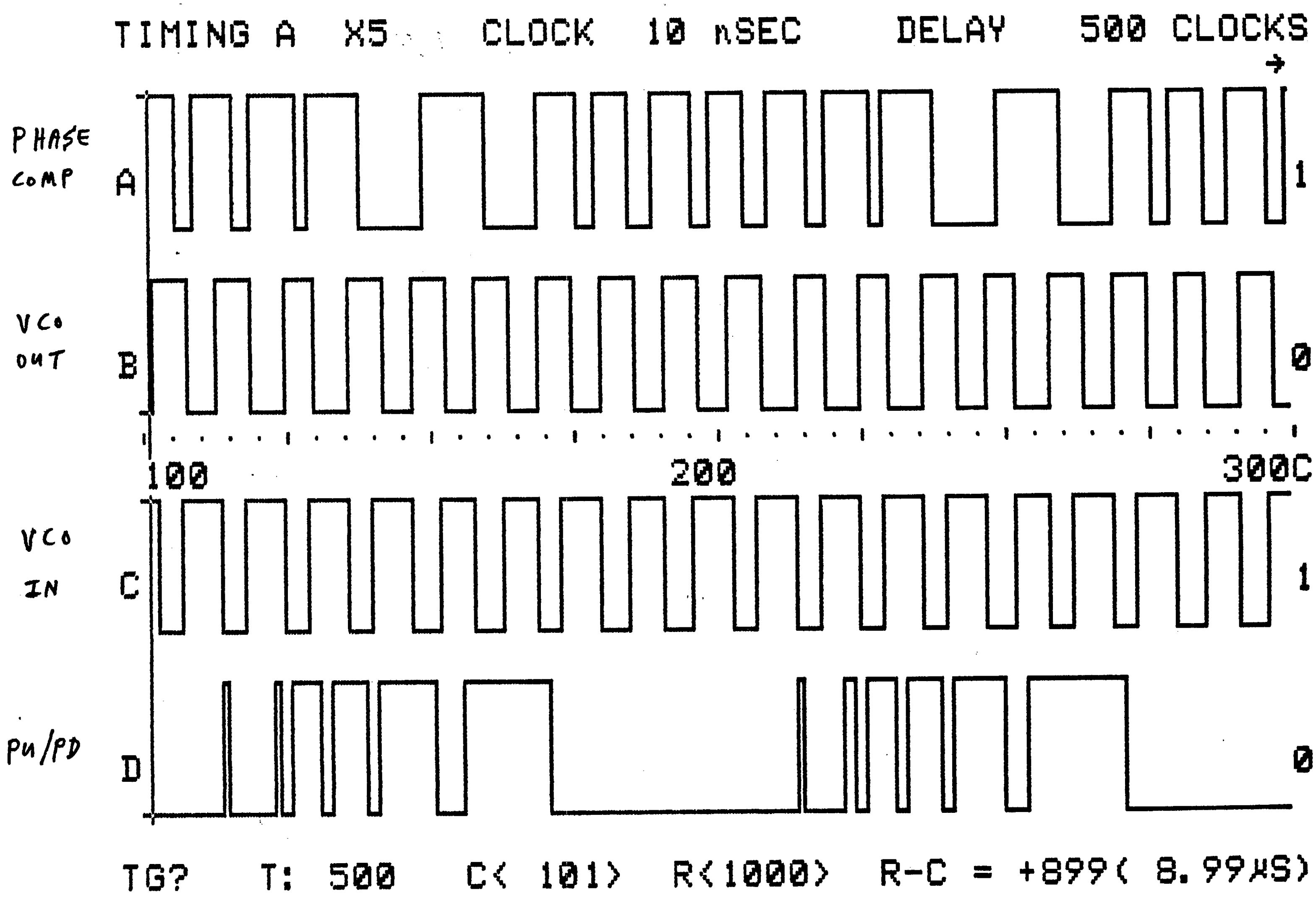
Data Field



5070 VCO Chip Timing

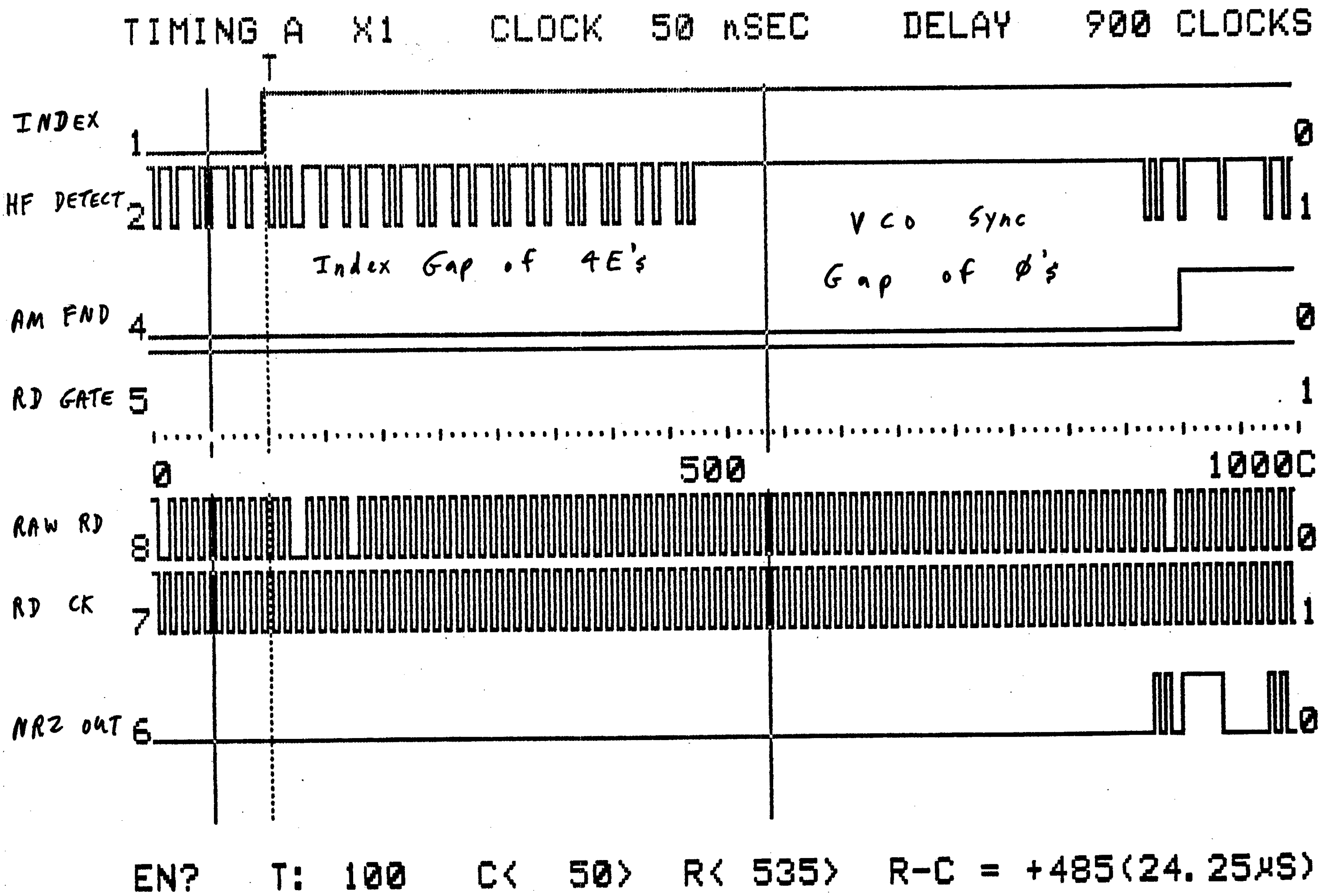
VCO Signals

During Data Read



5070 VCO Chip Timing

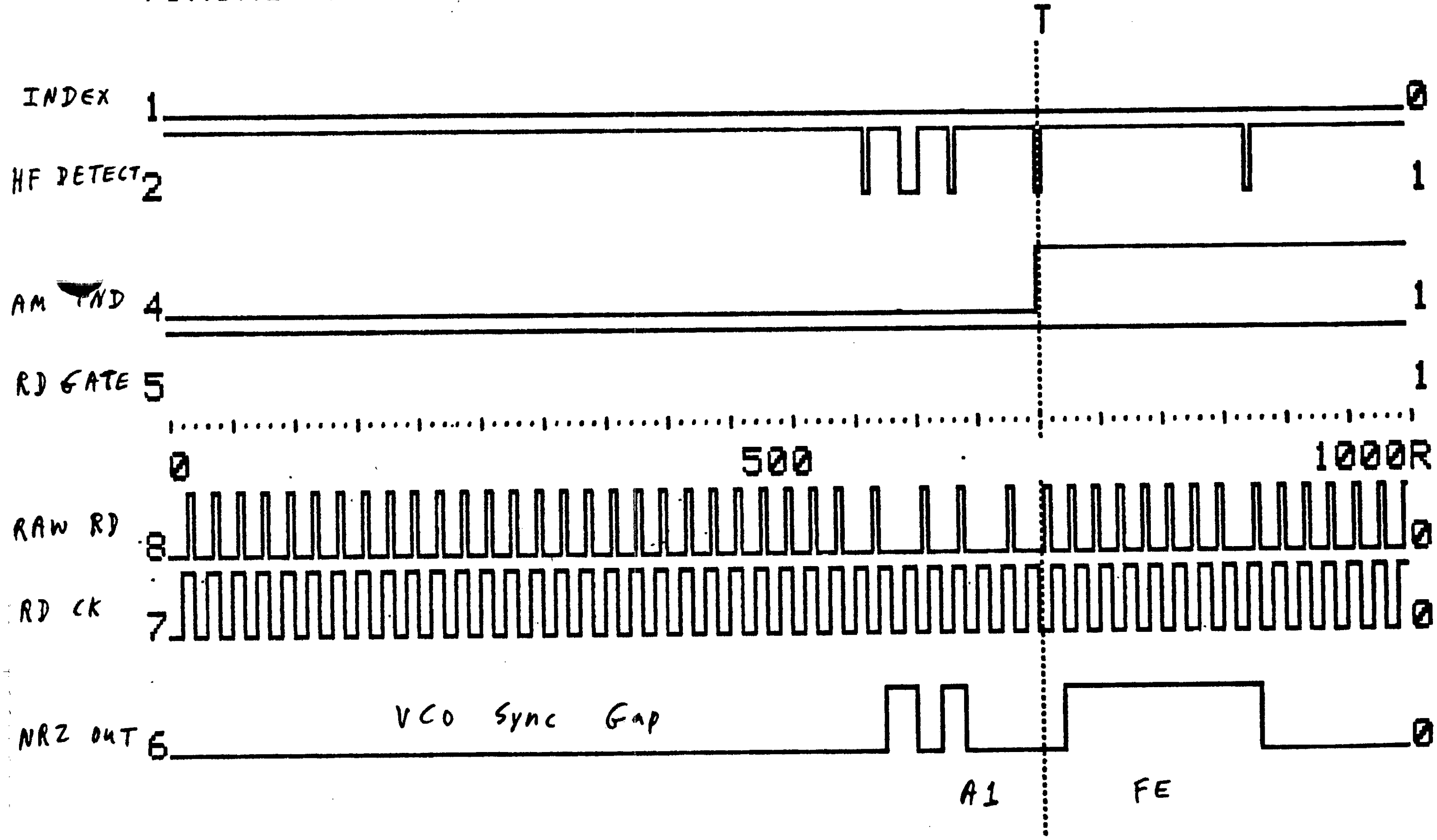
Search Sequence
from Index



5070 VCO Chip Timing

AM Search

TIMING A X1 CLOCK 10 nSEC DELAY 300 CLOCKS

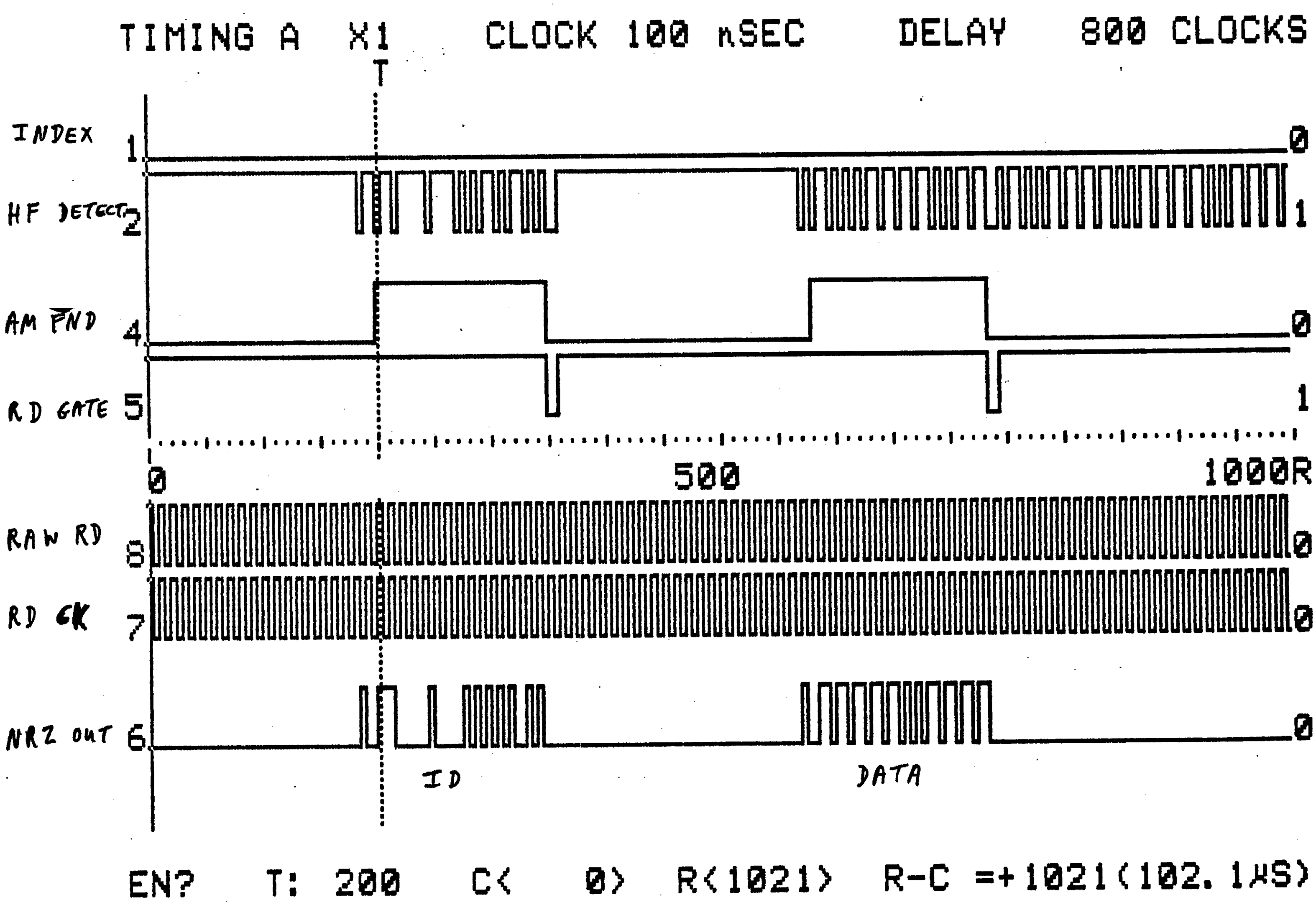


EN? T: 700 C<1000> R<1000> R-C = +0(0.00µS)

5070 VCO Chip Timing

ID Search

ID NOT FOUND

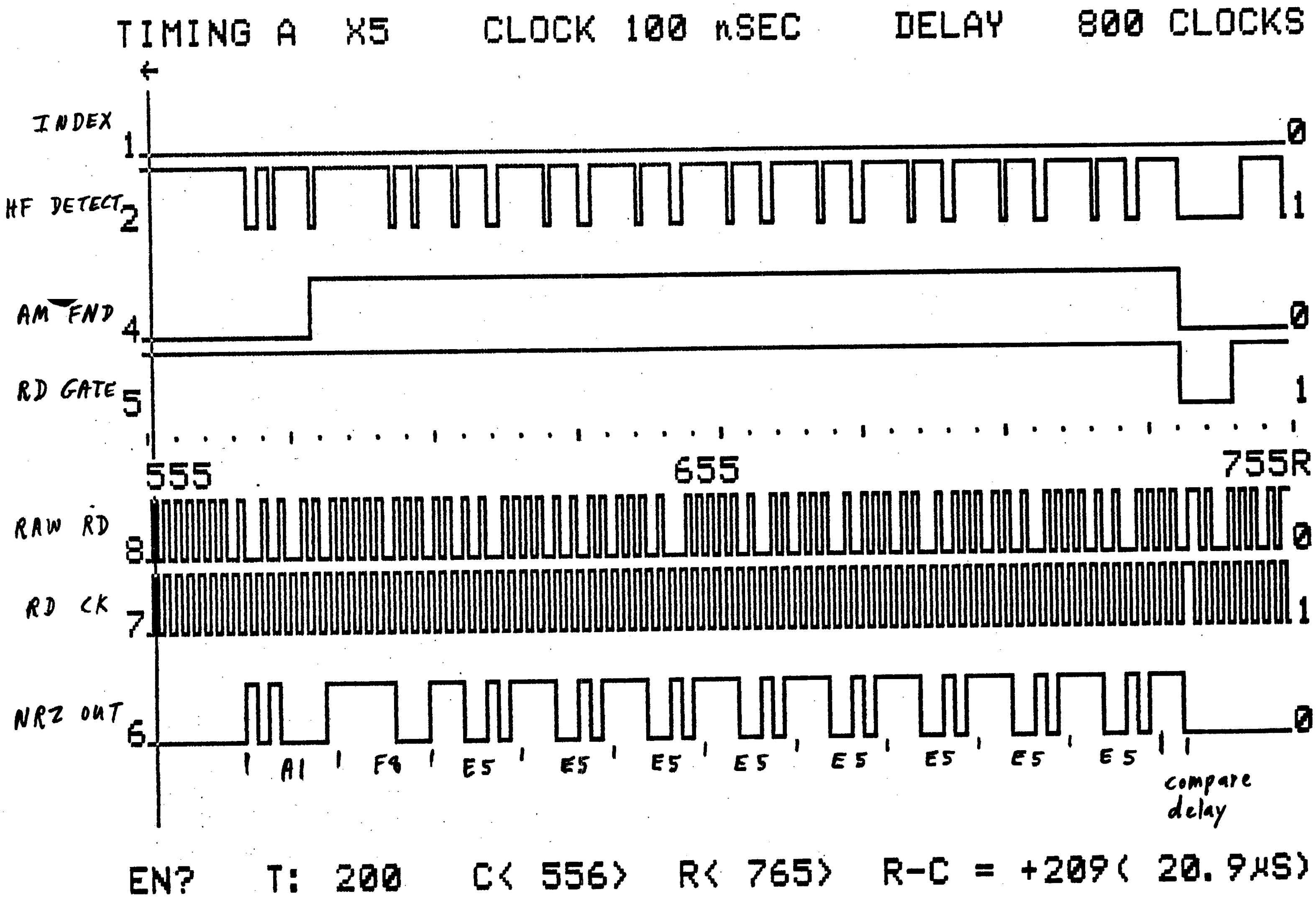


5070 VCO Chip Timing

ID Search

Data field found but not matched

It is apparent from this diagram that the 5070 doesn't compare on a byte by byte basis, or at least does not terminate it's search sequence until all ID bytes are assembled.

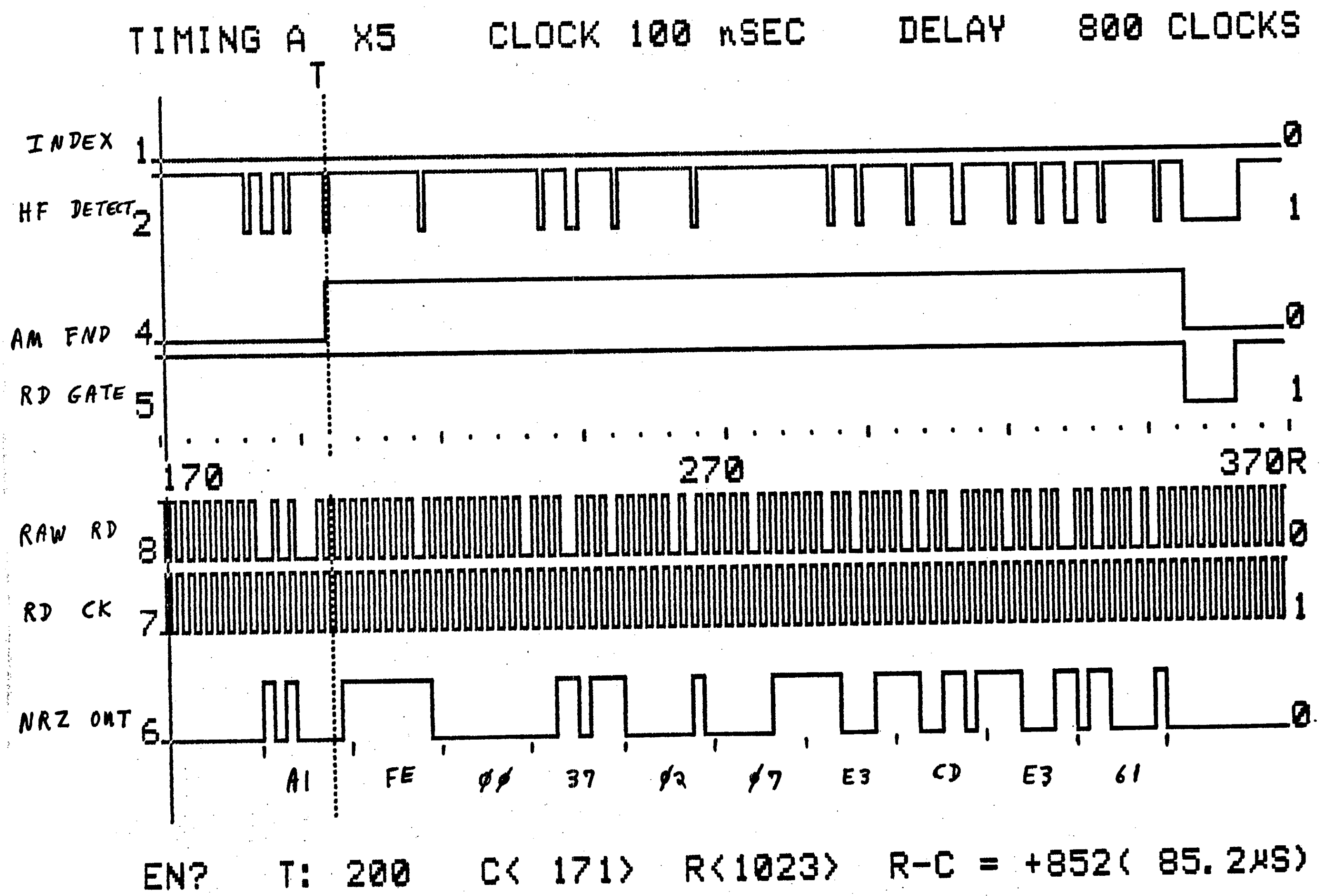


When an ID comparison fails after an AM is found, READ GATE is turned off then turned back on to begin another search sequence.

5070 VCO Chip Timing

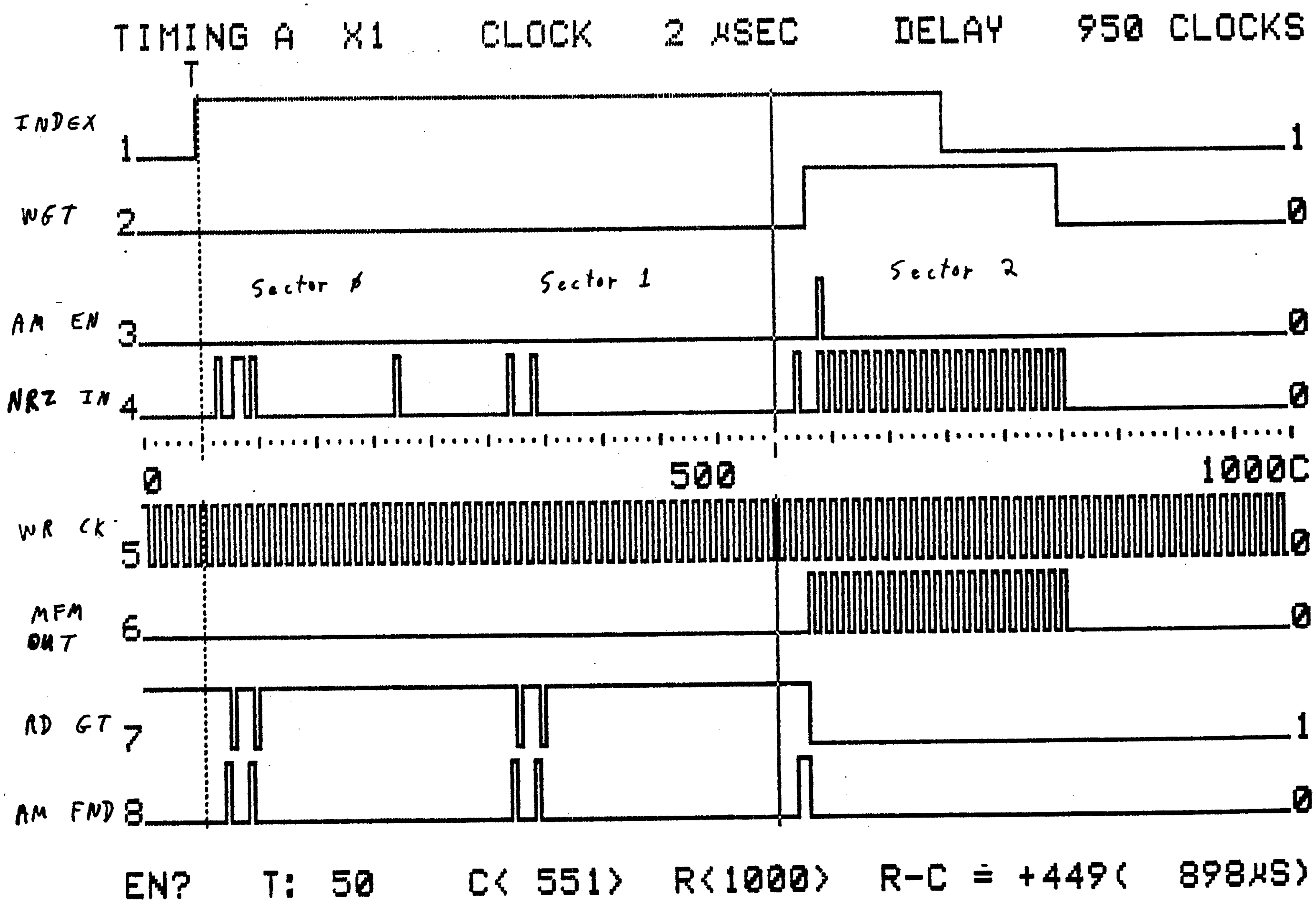
ID Search

ID field found but
not matched



5070 VCO Chip Timing

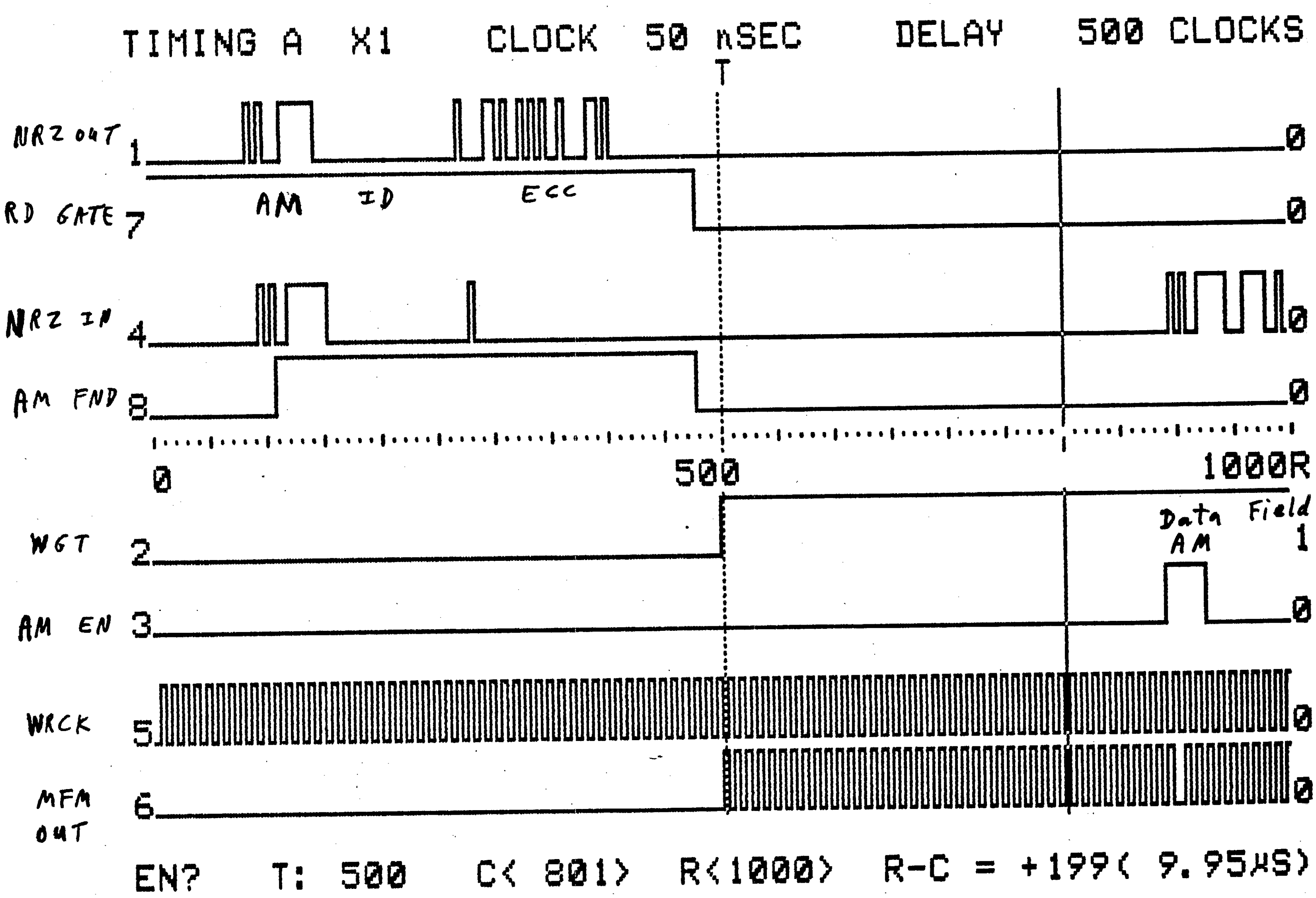
Write Sector 2



5070 VCO Chip Timing

Write Sector

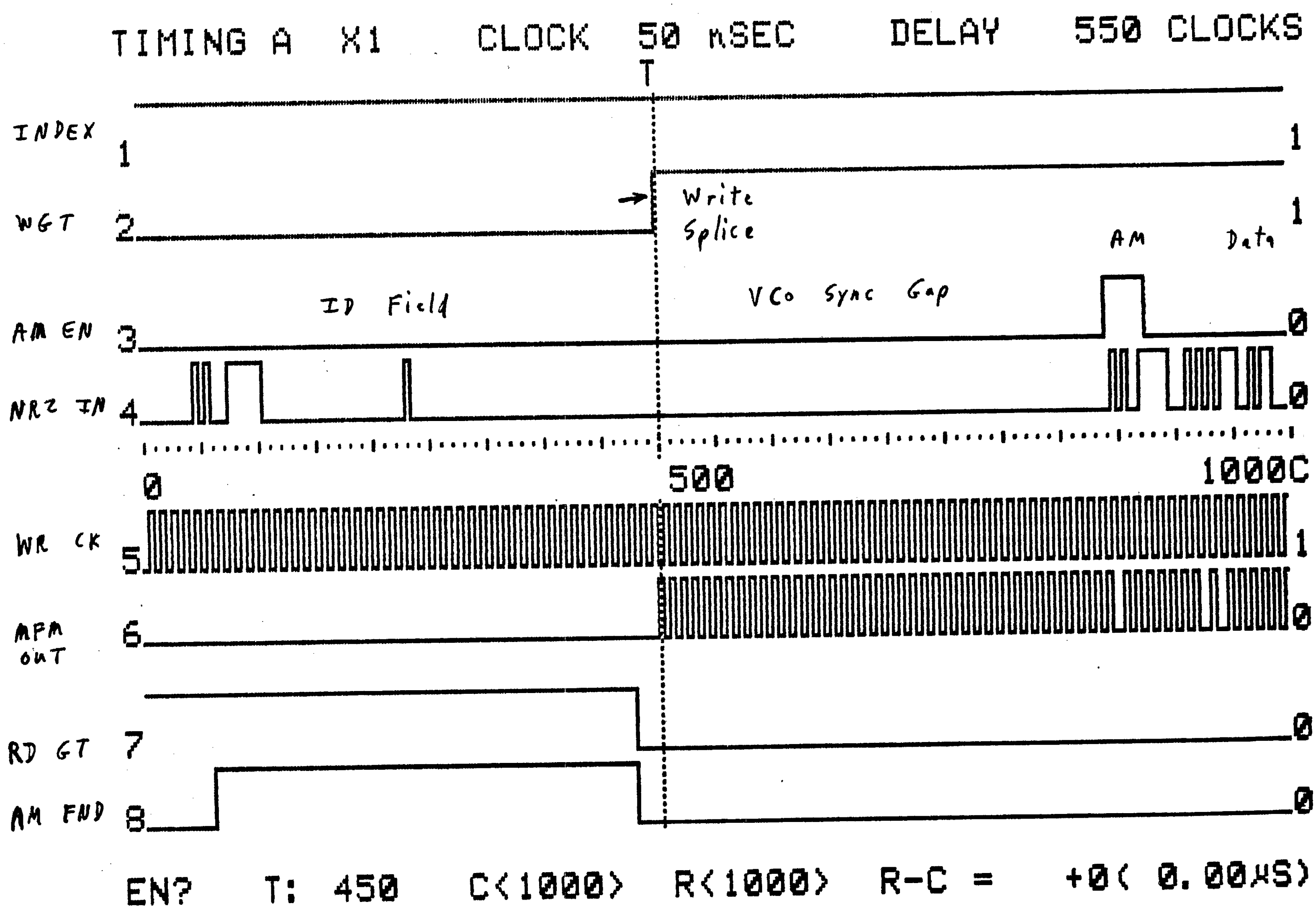
ID Match
Write Splice
Data Field AM



5070 VCO Chip Timing

Write Sector

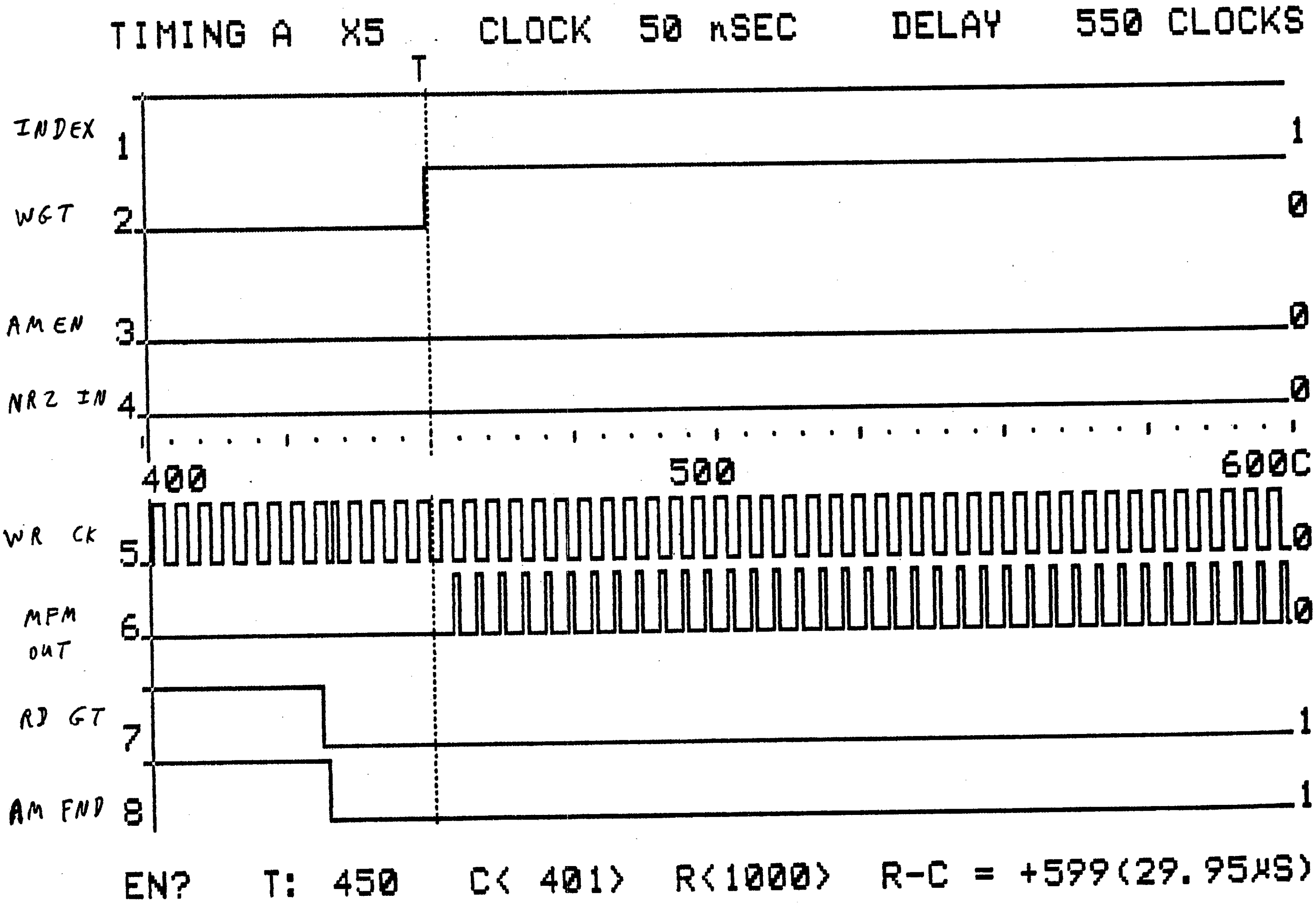
Write Splice



5070 VCO Chip Timing

Write Sector

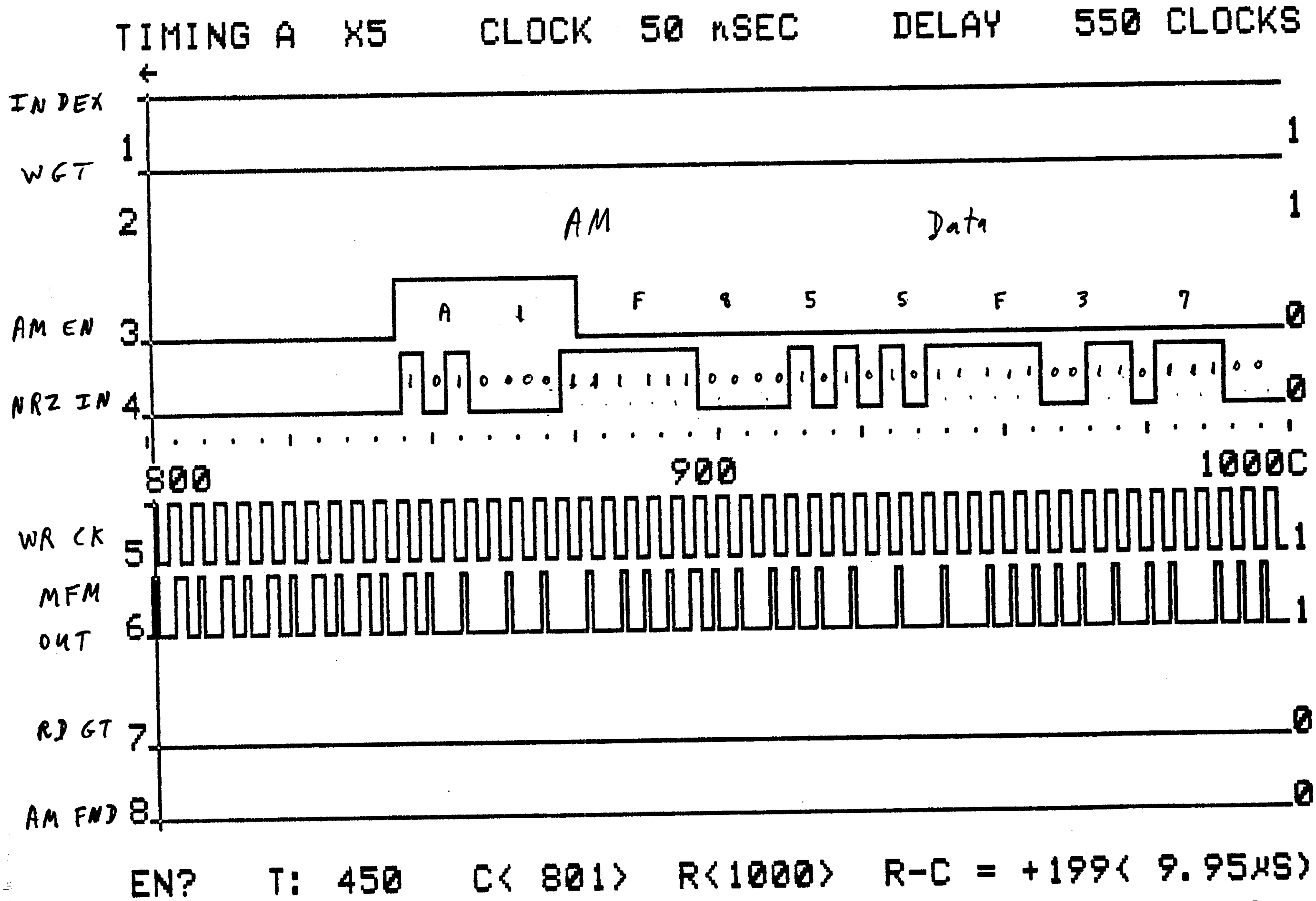
Write Splice



5070 VCO Chip Timing

Write Sector

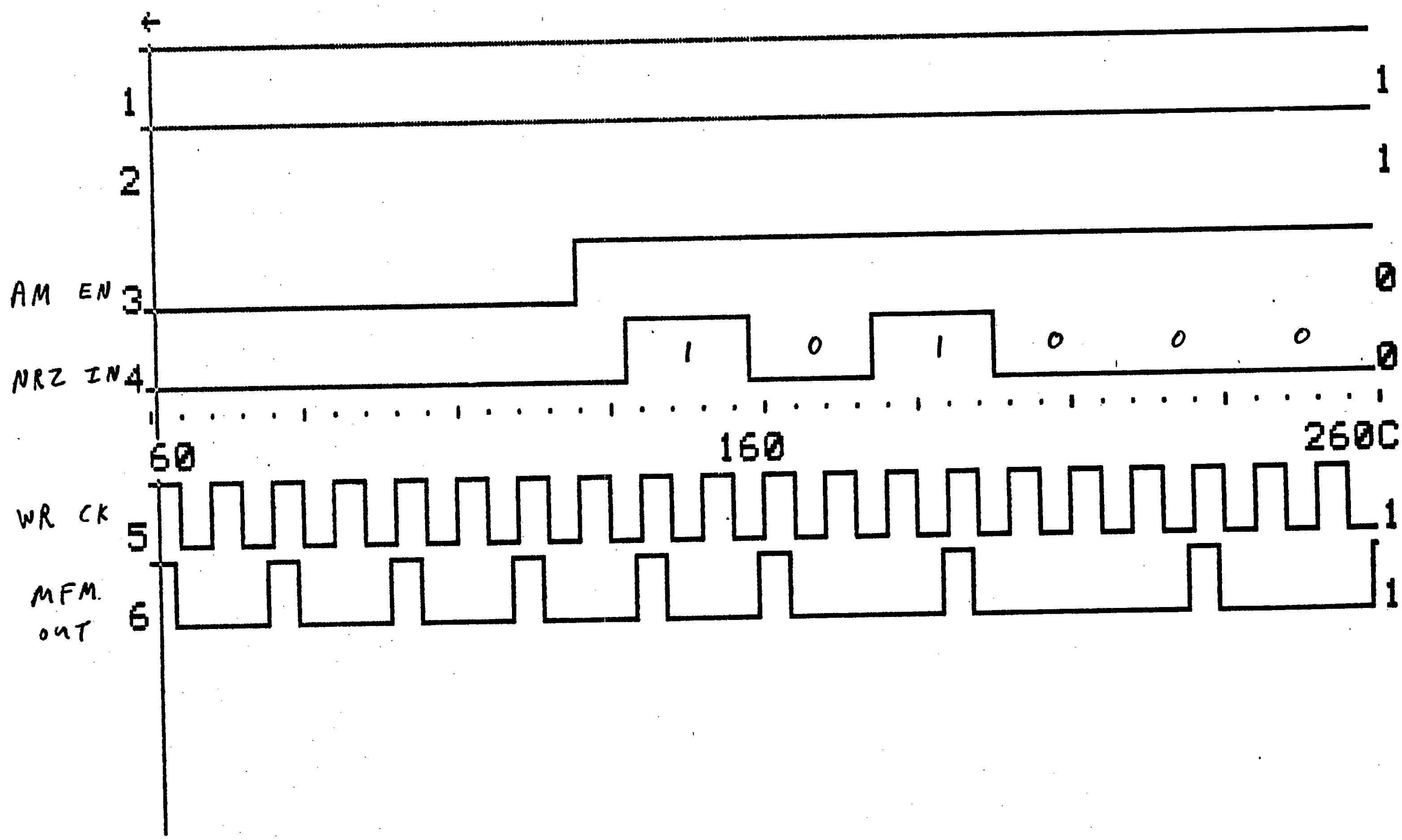
Data AM + Data



5020 VCO Chip Timing

Write Data AM

TIMING A X5 CLOCK 10 nSEC DELAY 4600 CLOCKS



EN? T: NR C< 61> R<1000> R-C = +939(9.39µS)

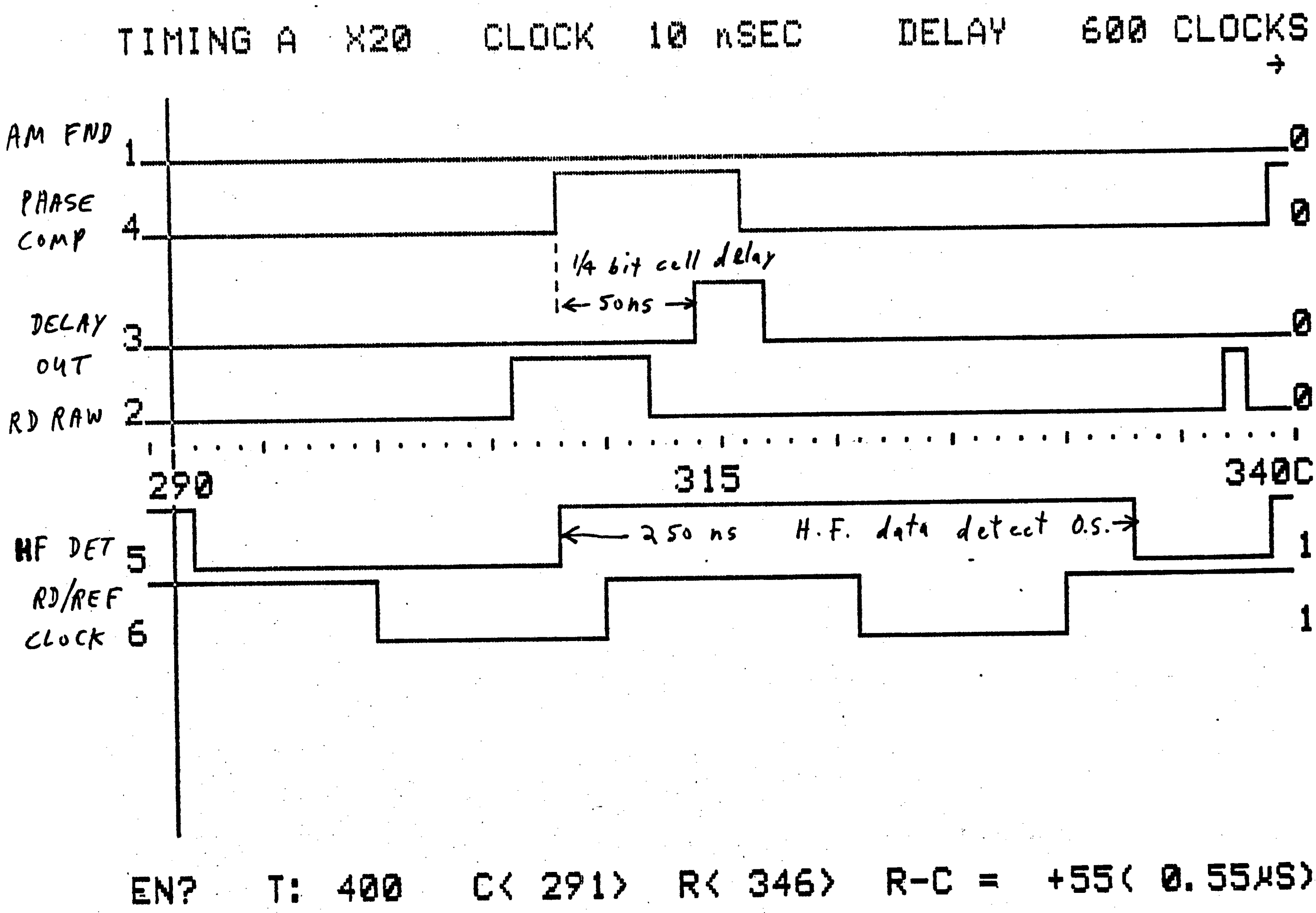
5070 VCO Chip Timing

Test Outputs

ID Search Sequence on Low Freq. Data

1/4 bit cell delay

HF detect O.S.



FEBRUARY 22, 1984

SCSI BUS CONTROLLER

* PROGRAMABLE INITIATOR / TARGET CONFIGURATION
* PROGRAMABLE I/O OR DMA DATA TRANSFER MODE
* PROGRAMABLE MICRO INTERRUPT MODE
* PROGRAMABLE CONTROLLER ID
* PROGRAMABLE PARITY CHECK / NO CHECK
* PROGRAMABLE TARGET ASYNC / SYNC DATA TRANSFER
* PROGRAMABLE SYNCHRONOUS REQ / ACK OFFSET OF 1 TO 255
* UP TO 2 MEGABYTES / SECOND IN ASYNCHRONOUS MODE
* UP TO 4 MEGABYTES / SECOND IN SYNCHRONOUS MODE
* INTERNAL SINGLE-ENDED DRIVERS & RECIEVERS
* 68 PIN PLASTIC LEADLESS CHIP CARRIER

```
GROUND      ---------------------------+
-H DATA 0   ------------------------+  !  +------------------------ MEM D-0
  DATA 1    ---------------------+  !  !  !  +--------------------- MEM D-1
DRV GROUND  ------------------+  !  !  !  !  !  +------------------ MEM D-2
-H DATA 2   ---------------+  !  !  !  !  !  !  !  +--------------- MEM D-3
-H DATA 3   ------------+  !  !  !  !  !  !  !  !  !  +------------ MEM D-4
-H DATA 4   ---------+  !  !  !  !  !  !  !  !  !  !  !  +--------- MEM D-5
-H DATA 5   ------+  !  !  !  !  !  !  !  !  !  !  !  !  !  +------ MEM D-6
DRV GROUND  ---+  !  !  !  !  !  !  !  !  !  !  !  !  !  !  !  +--- MEM D-7
            +-----------------------------------------------------+
            !  43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27 !
            !                                                     !
-H DATA 6   ! 44                                               26 !  -DMA REQ
            !                                                     !
-H DATA 7   ! 45                                               25 !  -DMA ACK
            !                                                     !
-H DATA P   ! 46                                               24 !  -DMA I/O
            !                                                     !
-ATN        ! 47                                               23 !  -OUTCLK
            !                                                     !
DRV GROUND  ! 48                                               22 !  -INEN
            !                                                     !
-BSY        ! 49                                               21 !  CLOCK
            !                                                     !
-ACK        ! 50                                               20 !  -RESET OUT
            !                      O M T I                        !
-RST        ! 51                                               19 !  -RESET R/C
            !                      S C S I                        !
   C        ! 52                                               18 !  VCC
            !                       B U S                         !
-MSG        ! 53                                               17 !  OUT DRV EN
            !                C O N T R O L L E R                  !
DRV GROUND  ! 54                                               16 !  INIT / TARG
            !                                                     !
-SEL        ! 55                                               15 !
            !                                                     !
-C/D        ! 56                                               14 !
            !                                                     !
-REQ        ! 57                                               13 !  PAR EN
            !                                                     !
-I/O        ! 58                                               12 !  ID 0
            !                                                     !
DRV GROUND  ! 59                                               11 !  ID 1
            !                                                     !
INTERRUPT   ! 60                                               10 !  ID 2
            !                                                     !
            !  61 62 63 64 65 66 67 68 1  2  3  4  5  6  7  8  9  !
            +-----------------------------------------------------+
-XOR A-7    ---+  !  !  !  !  !  !  !  !  !  !  !  !  !  !  !  +--- A/D-7
-XOR A-6    ------+  !  !  !  !  !  !  !  !  !  !  !  !  !  +------ A/D-6
-XOR A-5    ---------+  !  !  !  !  !  !  !  !  !  !  !  +--------- A/D-5
CONFIG      ------------+  !  !  !  !  !  !  !  !  !  +------------ A/D-4
IO/-MEM     ---------------+  !  !  !  !  !  !  !  +--------------- A/D-3
   RD       ------------------+  !  !  !  !  !  +------------------ A/D-2
 IOWR       ---------------------+  !  !  !  +--------------------- A/D-1
ALE         ------------------------+  !  +------------------------ A/D-0
GROUND      ---------------------------+
```

OMTI PROPRIETARY

SYMBOL	TYPE	NAME AND FUNCTION
A/D 0-7	I/O	MULTIPLEXED ADDRESS / DATA BUS: 3-STATE ADDRESS / DATA LINES THAT INTERFACE WITH THE CPU LOWER 8 BIT ADDRESS / DATA BUS. THE ADDRESSES ARE LATCHED INTO THE ADDRESS REGISTER ON THE FALLING EDGE OF ALE. THE 8 BIT DATA IS EITHER WRITTEN INTO OR READ FROM THE SCSI CONTROLLER REGISTER, DEPENDING ON -IOWR OR -IORD INPUT CONTROL LINES, IF THE ADDRESS IN WITHIN THE RANGE OF THE INTERNAL CHIP SELECT.
ALE	I	ADDRESS LATCH ENABLE: THIS INPUT STROBE IS FOR STORING ADDRESS 0-7 INTO THE ADDRESS REGISTER ON THE FALLING EDGE OF ALE FOR INTERNAL CHIP AND REGISTER SELECT. IF THE CONFIG INPUT IS HIGH, THE ALE INPUT IS INVERTED CONVERTING IT TO -AS.
-IOWR	I	I/O WRITE: THIS ACTIVE LOW INPUT STROBE IS USED BY THE CPU TO LOAD INFORMATION IN THE SCSI CONTROLLER WITH THE PROPER ADDRESS FOR CHIP AND REGISTER SELECTION. IF THE CONFIG INPUT IS HIGH, THE -IOWR INPUT IS CONVERTED TO READ -WRITE (R/-W). IN THIS CONFIGERATION R/-W IS USED WITH -DS TO EITHER READ OR WRITE A REGISTER.
-IORD	I	I/O READ: THIS ACTIVE LOW INPUT STROBE IS USED BY THE CPU TO READ STATUS INFORMATION FROM THE SCSI CONTROLLER WITH THE PROPER ADDRESS FOR CHIP AND REGISTER SELECTION. IF THE CONFIG INPUT IS HIGH, THE -IORD INPUT IS CONVERTED TO -DATA STROBE (-DS). IN THIS CONFIGURATION -DS IS USED WITH R/-W TO EITHER READ OR WRITE A REGISTER.
IO/-MEM	I	IO/-MEMORY: THIS INPUT IS USED FOR AN ACTIVE HIGH CHIP ENABLE. IN AN 8085 SYSTEM THIS LINE IS CONNECTED TO THE SAME MICRO LINE. IF CONFIG IS HIGH THIS INPUT IS INVERTED AND IS CONVERTED TO -DATA MEMORY (-DM).

SYMBOL	TYPE	NAME AND FUNCTION
XOR 7-5	I	EXCLUSIVE OR ADDRESS 7 - 5: THESE INTERNALLY PULLED-UP INPUTS ARE USED FOR THE INTERNAL CHIP SELECT. THEY CONTROL THE POLARITY OF THE CORROSPONDING ADDRESS LINE. IF ANOTHER GROUP CHIP SELECT IF REQUIRED , GROUND THE APPROPRIATE LINE.
CONFIG	I	CONFIG: THIS INTERNALY PULLED-UP LINE IS USED TO SELECT THE MICRO STROBE INPUTS. WHEN THIS INPUT IS GROUNDED THE CHIP IS CONFIGURED FOR AN 8085 / 8051 TYPE MICRO. WHEN LEFT OPEN THE CHIP IS CONFIGURED FOR A Z-8 TYPE MICRO.
-RESET	~~I~~ O	-RESET: THIS OUTPUT IS ACTIVE LOW TRUE ON POWER UP OR WHEN THE SCSI RESET INPUT IS TRUE.
RESET R/C	IO	RESET R/C: THIS I/O LINE IS TO BE CONNECTED TO AN EXTERNAL CAPACITOR USED FOR THE ON CHIP POWER ON RESET TO PROVIDE A RESET PULSE OF EXTERNAL CONTROLLABLE WIDTH.
INTERRUPT	O	INTERRUPT: THIS OUTPUT, IF ENABLED IS ACTIVE WHEN A ANY ENABLED INTERRUPTING SEQUENCE IS DETECTED AND IS CLEARED WHEN THE MICRO READS STATUS.
CLOCK	I	CLOCK: THIS INPUT IS FOR A FREE RUNNING CLOCK USED FOR THE INTERNAL ARBITRATION LOGIC. ALL TIMING IS CALCULATED WITH A 20 MHZ CLOCK.
ID 0-2	I	ID 0-3: THESE INPUTCS ARE USED FOR THE DEFAULT SCSI CONTROLLER ID INFORMATION. THESE BITS ARE ACCESSABLE TO THE MICRO IN A READ PORT OPPERATION.

SYMBOL	TYPE	NAME AND FUNCTION
PAR EN	I	PARITY ENABLE: THIS INPUT IS USED FOR THE DEFAULT SCSI PARITY CONFIGERATION. THIS BIT IS ACCESSABLE TO THE MICRO IN A READ PORT OPPERATION.
HDATA 0-7	IO	HOST DATA 0 - 7: ** THIS 8 BIT BIDIRECTIONAL DATA BUS DRIVER / RECEIVER IS USED TO TRANSFER PARALLEL DATA TO / FROM THE HOST COMPUTER.
H DATA P	I/O	HOST DATA PARITY: ** THIS DRIVER / RECEIVER I/O LINE, IN OUTPUT MODE IS ODD PARITY OF THE HOST DATA BUS. IN INPUT MODE THE HOST MUST GENERATE ODD PARITY OF THE BUS AND THE SCSI CONTROLLER WILL CHECK FOR VALID PARITY IF INTERNALLY ENABLED.
BUSY	I/O	BUSY: ** THIS DRIVER / RECEIVER I/O LINE, IN TARGET MODE IS DRIVEN BY THIS SCSI CONTROLLER CHIP. IN INITIATOR MODE THIS SCSI CONTROLLER CHIPS RECEIVES THE BUSY LINE DRIVEN BY THE TARGET WHEN IT IS SELECTED.
ACK	I/O	ACKNOWLEDGE: ** THIS DRIVER / RECEIVER I/O LINE, IN TARGET MODE IS RECEIVED BY THIS SCSI CONTROLLER CHIP IN RESPONSE TO REQUEST BY THIS CONTROLLER FOR DATA TRANSFER. IN INITIATOR MODE THIS LINE IS DRIVED BY THE CONTROLLER CHIP IN RESPONSE TO THE REQUEST BY THE TARGET FOR DATA TRANSFER.
MSG	I/O	MESSAGE: ** THIS DRIVER / RECEIVER I/O LINE, IN TARGET MODE IS DRIVEN BY THIS CONTROLLER CHIP TO INDICATE A STATUS BYTE IS IN PROGRESS. IN INITIATOR MODE THIS LINE IS RECEIVED BY THIS SCSI CONTROLLER CHIP TO INDICATE A STATUS BYTE IS IN PROGRESS.

SYMBOL	TYPE	NAME AND FUNCTION
REQ	I/O	REQUEST: **
		THIS DRIVER / RECEIVER I/O LINE, IN TARGET MODE IS DRIVEN BY THIS SCSI CONTROLLER CHIP TO REQUEST DATA TRANSFER TO / FROM THE INIT-IATOR. IN INITIATOR MODE THIS LINE IS RECEIVED BY THIS CONTROLLER CHIP WHEN THE TARGET IS REQUESTING DATA TRANSFER.
SELECT	I/O	SELECT: **
		THIS DRIVER / RECEIVER I/O LINE, IN TARGET MODE IS RECEIVED BY THIS CONTROLLER CHIP WITH THE DESIRED TARGETS ID ON THE HDATA BUS. IN THE INITIATOR MODE THIS SCSI CONTROLLER CHIP DRIVES THIS LINE WITH THE TARGETS ID ON THE HDATA BUS TO SELECT THE DESIRED TARGET.
C/D	I/O	CONTROL / DATA: **
		THIS DRIVER / RECEIVER I/O LINE, IN TARGET MODE IS DRIVEN BY THIS CONTROLLER FOR ALL COMMAND / STATUS TRANSFER. IN INITIATOR MODE THIS LINE IS RECEIVED TO INDICATE THE TARGET HAS COMMAND / STATUS TRANSFER.
RESET	I	RESET:
		THIS RECEIVER LINE IS ASSERTED BY THE HOST TO ABORT ANY OPPERATION IN PROCESS AND RETURN THE BUS TO AN IDLE STATE.
I/O	I/O	INPUT / OUTPUT: **
		THIS DRIVER / RECEIVER I/O LINE, IN TARGET MODE IS DRIVEN BY THIS CONTROLLER TO INDICATE DATA / COMMAND / STATUS TO BE TRANSFERED TO THE INITIATING CONTROLLER. IN INITIATOR MODE THIS LINE IS RECEIVED TO INDICATE DATA TRANSFER DIRECTION .

** DRIVER / RECEIVER

DRIVERS SYNC 48 MA @ .4 VDC ASSERTED
RECEIVERS ASSERTED AT INPUT 0.0 TO 0.8 VDC
NON-ASSERTED AT INPUT 2.0 TO 5.25 VDC
MINIMUN INPUT HYSTERESIS = 0.2 VDC

ADDRESS REGISTER AND CONTROL

7 6 5 4 3 2 1 0	-IOWR	-IORD	REGISTER FUNCTION
S S S 0 0 0 0 0	0	1	INTERRUPT MASK REGISTER
S S S 0 0 0 0 1	0	1	BUS CONTROL REGISTER
S S S 0 0 0 1 0	0	1	COMMAND REGISTER
S S S 0 0 0 1 1	0	1	SYNCHRONOUS MODE OFFSET
S S S 0 0 1 0 0	0	1	SYNCHRONOUS MODE RATE
S S S 0 0 1 0 1	0	1	CONTROLLER ID REGISTER
S S S 0 0 1 1 0	0	1	HOST DATA OUT REGISTER
S S S 0 0 1 1 1	0	1	HOST DATA OUT REGISTER (R/A)
S S S 0 0 0 0 0	1	0	INTERRUPT STATUS PORT
S S S 0 0 0 0 1	1	0	BUS CONTROL STATUS PORT
S S S 0 0 0 1 0	1	0	STATUS PORT
S S S 0 0 0 1 1	1	0	SYNCHRONOUS OFFSET COUNT PORT
S S S 0 0 1 0 0	1	0	(NOT USED)
S S S 0 0 1 0 1	1	0	CONFIG PORT
S S S 0 0 1 1 0	1	0	HOST DATA INPUT PORT
S S S 0 0 1 1 1	1	0	HOST DATA INPUT PORT (R/A)

S S S = INTERNAL CHIP SELECT

(R/A) = REQUEST / ACK I/O HANDSHAKE

(BASE + 0) INTERRUPT MASK REGISTER

DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
! ! ! ! ! ! ! +---------     1 = SELECT
! ! ! ! ! ! !
! ! ! ! ! ! +----------      1 = RE-SELECT
! ! ! ! ! !
! ! ! ! ! +------------      1 = ARBITRATION WON
! ! ! ! !
! ! ! ! +--------------      1 = TARGET SELECTED
! ! ! !
! ! ! +----------------      1 = I/O TARGET DATA EMPTY
! ! !
! ! +------------------      1 = I/O INITIATOR DATA REQUEST
! !
! +--------------------      1 = INITIATOR I/O C/D STATE CHANGE
!
+----------------------      1 = PARITY ERROR
```

(BASE + 0) INTERRUPT STATUS PORT

DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
! ! ! ! ! ! ! +--------      1 = SELECT
! ! ! ! ! ! !
! ! ! ! ! ! +----------      1 = RE-SELECT
! ! ! ! ! !
! ! ! ! ! +------------      1 = ARBITRATION WON
! ! ! ! !
! ! ! ! +--------------      1 = TARGET SELECTED
! ! ! !
! ! ! +----------------      1 = I/O TARGET DATA EMPTY
! ! !
! ! +------------------      1 = I/O INITIATOR DATA REQUEST
! !
! +--------------------      1 = INITIATOR I/O C/D STATE CHANGE
!
+----------------------      1 = PARITY ERROR
```

(BASE + 1) BUS CONTROL REGISTER

DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
0 0 0 0 0 0 0 0 -------    = CLEAR REQUEST
0 0 0 0 0 0 0 1 -------    = CLEAR ACKNOWLEGE
0 0 0 0 0 0 1 0 -------    = CLEAR SELECT
0 0 0 0 0 0 1 1 -------    = CLEAR BUSY
0 0 0 0 0 1 0 0 -------    = CLEAR INPUT / OUTPUT
0 0 0 0 0 1 0 1 -------    = CLEAR COMMAND / DATA
0 0 0 0 0 1 1 0 -------    = CLEAR MESSAGE
0 0 0 0 0 1 1 1 -------    = CLEAR ATTENTION

0 0 0 0 1 0 0 0 -------    = SET REQUEST
0 0 0 0 1 0 0 1 -------    = SET ACKNOWLEGE
0 0 0 0 1 0 1 0 -------    = SET SELECT
0 0 0 0 1 0 1 1 -------    = SET BUSY
0 0 0 0 1 1 0 0 -------    = SET INPUT / OUTPUT
0 0 0 0 1 1 0 1 -------    = SET COMMAND / DATA
0 0 0 0 1 1 1 0 -------    = SET MESSAGE
0 0 0 0 1 1 1 1 -------    = SET ATTENTION
```

(BASE + 1) BUS STATUS PORT

DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
! ! ! ! ! ! ! +--------    1 = REQUEST
! ! ! ! ! ! !
! ! ! ! ! ! +----------    1 = ACKNOWLEDGE
! ! ! ! ! !
! ! ! ! ! +------------    1 = SELECT
! ! ! ! !
! ! ! ! +--------------    1 = BUSY
! ! ! !
! ! ! +----------------    1 = INPUT / OUTPUT
! ! !
! ! +------------------    1 = COMMAND / DATA
! !
! +--------------------    1 = MESSAGE
!
+----------------------    1 = ATTENTION
```

(BASE + 2) COMMAND REGISTER

DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
0 0 0 0 0 0 0 0 -------    = CLEAR ARBITRATION (SELECT)
0 0 0 0 0 0 0 1 -------    = SET TARGET MODE
0 0 0 0 0 0 1 0 -------    = SET I/O MODE
0 0 0 0 0 0 1 1 -------    = SET SELECT ARBITRATION
0 0 0 0 0 1 0 0 -------    = SET ASYNCHRONOUS MODE
0 0 0 0 0 1 0 1 -------    = (RESERVED) CLEAR IO ENABLE
0 0 0 0 0 1 1 0 -------    = SET INTERRUPT LOW
0 0 0 0 0 1 1 1 -------    = CLEAR PARITY CHECK

0 0 0 0 1 0 0 0 -------    = SET ARBITRATION
0 0 0 0 1 0 0 1 -------    = SET INITIATOR MODE
0 0 0 0 1 0 1 0 -------    = SET DMA MODE
0 0 0 0 1 0 1 1 -------    = SET RE-SELECT ARBITRATION
0 0 0 0 1 1 0 0 -------    = SET SYNCHRONOUS MODE
0 0 0 0 1 1 0 1 -------    = (RESERVED) SET IO ENABLE
0 0 0 0 1 1 1 0 -------    = SET INTERRUPT HIGH
0 0 0 0 1 1 1 1 -------    = SET PARITY CHECK
```

(BASE + 2) STATUS PORT

DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
! ! ! ! ! ! ! +--------    1 = SCSI BUS FREE STATE
! ! ! ! ! ! !
! ! ! ! ! ! +----------    1 = INITIATOR MODE
! ! ! ! ! !
! ! ! ! ! +------------    1 = DMA MODE
! ! ! ! !
! ! ! ! +--------------    1 = SYNCHRONOUS MODE
! ! ! !
! ! ! +----------------    0 = ( NOT USED )
! ! !
! ! +------------------    0 = ( NOT USED )
! !
! +--------------------    1 = SYNCHRONOUS DELTA = MAX
!
+----------------------    1 = SYNCHRONOUS DELTA = 0
```

(BASE + 3) SYNCHRONOUS OFFSET REGISTER

DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
+-+-+-+-+-+-+-+--------   0 TO FF = DELTA REQ / ACK OFFSET
```

(BASE + 3) SYNCHRONOUS RATE REGISTER

DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
+-+-+-+-+-+-+-+--------   0 TO FF = DELTA REQ / ACK OFFSET
```

SYNCHRONOUS RATE REGISTER

DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
0 0 0 0 0 0 0 0 -------   DELAY 1 CLOCK
0 0 0 0 0 0 0 1 -------   DELAY 2 CLOCK
0 0 0 0 0 0 1 0 -------   DELAY 3 CLOCK
0 0 0 0 0 0 1 1 -------   DELAY 4 CLOCK
0 0 0 0 0 1 0 0 -------   DELAY 5 CLOCK
0 0 0 0 0 1 0 1 -------   DELAY 6 CLOCK
0 0 0 0 0 1 1 0 -------   DELAY 7 CLOCK
0 0 0 0 0 1 1 1 -------   DELAY 8 CLOCK
0 0 0 0 1 0 0 0 -------   ( NOT USED )
! ! ! ! ! ! ! ! -------   ( NOT USED )
1 1 1 1 1 1 1 1 -------   ( NOT USED )
```

(BASE + 5) CONTROLLER ID REGISTER

DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
0 0 0 0 0 0 0 1 -------   = CONTROLLER ID 0
0 0 0 0 0 0 1 0 -------   = CONTROLLER ID 1
0 0 0 0 0 1 0 0 -------   = CONTROLLER ID 2
0 0 0 0 1 0 0 0 -------   = CONTROLLER ID 3
0 0 0 1 0 0 0 0 -------   = CONTROLLER ID 4
0 0 1 0 0 0 0 0 -------   = CONTROLLER ID 5
0 1 0 0 0 0 0 0 -------   = CONTROLLER ID 6
1 0 0 0 0 0 0 0 -------   = CONTROLLER ID 7
```

(BASE + 5) CONFIG PORT

DATA BUS

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
! ! ! ! ! +-+-+--------   DEFAULT CONTROLLER ID
! ! ! ! !
! ! ! ! +-------------    1 = DEFAULT PARITY ENABLE
! ! ! !
+-+-+-+---------------    0 = ( NOT USED )
```

(BASE + 6 OR 7) HOST DATA REGISTER

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
+-+-+-+-+-+-+-+--------   HOST DATA OUTPUT
```

(BASE + 6 OR 7) HOST DATA PORT

```
7 6 5 4 3 2 1 0
! ! ! ! ! ! ! !
+-+-+-+-+-+-+-+--------   HOST DATA INPUT
```