FWD5000 Floppy/Fixed Disk Drive Controller OEM Manual

Scientific Micro Systems, Inc.

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Document No: 3000616
Revision: F
Date: March 1, 1983

Applicable Product Numbers:

Assy.: 0004086 Rev. A and up
Prog. Assy.: 1001985 Rev. A and up

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I. CONTROLLER OVERVIEW

A. INTRODUCTION AND FEATURES

The FWD5000 controller is a complete preprogrammed controller for both Winchester and floppy disk drives. IBM compatible single and double density floppy formats are supported for 128, 256, 512, and 1K byte sectors and for single and dual sided diskettes. Optional single bit error correction is provided on the floppy by reduction of the standard IBM CRC residue. MFM encoding is used on the Winchester to support 256 and 512 byte sectors. A 24 bit ECC is used to provide correction of all 6-bit or less errors and detection of all 10-bit or less errors. The user may optionally use the ECC for error detection only. Physical sector interleave, head offset, and cylinder offset may be used to format both the Winchester and the floppy for maximum system performance. A full sector buffer (for up to 512 bytes) is provided on the FWD5000. Automatic buffer transfer, as well as direct transfer, is supported for multiple sector transfers across both head and cylinder boundaries. Error correction is performed on buffered transfers with no host interaction required.

The FWD5000 will support up to two 8" floppy disk drives and up to two 8" Winchester drives. The drive type which is to be used is programmed into straps on the pc board so that field changes may be accomplished without rewriting existing handlers. Other strap options include floppy write precompensation disable and various diagnostic and self test options. The FWD5000 is available completely packaged with drives and power in both rack mounting and table top versions as the FWT5000 series.

The host interface is a simple byte parallel port with optional parity. Commands to the controller and status from the controller are passed across this port a byte at a time following a handshake type protocol. This protocol has been designed to minimize the amount of hardware required to interface the FWD5000 to microprocessors and other byte oriented systems by utilizing the latest generation of support circuitry such as DMA controllers and intelligent I/O ports. See SMS application note number 3000672 for details and example circuits.

The host interface is hardware compatible with the Shugart SA1403D controller and supports a subset of the SA1403D command set. The following is an overview of the advantages provided by the FWD5000.

- Comprehensive self test and drive test diagnostics included on board.
- Cylinder and head offset at format as well as selectable sector interleave.
- IBM deleted data address mark support on the floppy for true compatibility.
- Direct transfers and sector buffered transfers.
- 128, 256, 512 and 1K byte sectors on floppy in single and double density.
- Programmable Winchester sector size of 256 or 512 bytes.
- 6 bit ECC on the Winchester and single bit ECC on the floppy.

Additional FWD5000 features include:

- Direct connection to Shugart 1000/1100, Quantum 2000 Winchester drives and Shugart 800/850/860 or Tandon TM848 floppy drives.
- Single 8.25" x 13.7" PC controller supports Winchester and floppy disk drives.
- Controls up to 2 floppy drives and 2 Winchester drives.
- Supports single or dual head floppy drives.
- IBM compatible 3740 and 2/2D floppy disk formats.
- Patented data recovery phase lock loop design.
- Easy to use byte oriented TTL interface.
- Logical or physical addressing of the disk surface.
- Up to 256 contiguous sector data transfer with single command.
- Programmable error retry operation.
- Single +5 volt power supply.

B. FWD5000 COMMANDS AND STATUS

All disk operations performed by the FWD5000 are initiated by the transfer of a command from the host to the controller. Each command consists of six bytes. The content of these command bytes is detailed in section III for all commands. The method of transferring these bytes is detailed in section IV (Host Interface Protocol).

The command set minimizes host overhead by maximizing the function performed per command. A single FORMAT command will format the entire disk with specified head offset, cylinder offset and sector interleave factor. A single READ command will read up to 256 sectors, retry all access errors and perform data error correction before transferring the data to the host. Commands are provided for determining disk format, head location, and extensive operation status. The high level of function provided by the FWD5000 commands means that there will be less host software due to fewer commands per task, no host implemented retry etc., and higher system performance due to fewer interrupts and simple error diagnosis.

At the termination of each command, two bytes of status are provided to the host. The content of these bytes is detailed in section III. The method of transferring these bytes is detailed in section IV. These status bytes allow the host to determine whether the operation completed without error, and to determine complete drive status.

C. FWD5000 DATA TRANSFER

Both direct and buffered data transfers are supported by the FWD5000. In a direct transfer operation, the host must be able to follow the data transfer rate of the disk. If this can be done, the direct transfer is the fastest transfer method. From 1 to 256 sectors may be transferred in one operation. No error correction is done on direct transfer since the controller cannot access the data. If an ECC error occurs on a direct transfer, the host may recover that sector by performing a buffered transfer.

In a buffered transfer operation there are no constraints on the host data rate. Once the host has completed its fill/empty buffer operation, the controller will perform the next disk access. Note that the fill/empty buffer operation is overlapped with any seek access to improve performance. A sector interleave may be specified at format time such that the next sequential sector is available once the buffer is ready without an entire disk revolution being required. From 1 to 256 sectors may be transferred in a single operation and error correction is automatically performed by the controller before the data is sent to the host on a read.

In both direct and buffered transfers, head switching and seeks are automatically handled by the controller. Head offset and cylinder offset may be chosen at format time such that the next sequential sector is available after the head select delay or the head step delay. The controller assumes that head 0 to N will be read in order before the next sequential cylinder is accessed to maximize performance.

The performance implications of direct transfer and formats with offsets should not be underestimated. For example, a complete backup of 1.2 Mbytes from a Winchester to a floppy diskette can be performed in less than 40 seconds (with a 16 Kbyte buffer). A controller without these features would require over a minute to backup to a 2 to 1 interleaved diskette.

D. FWD5000 ECC/CRC

The standard 16 bit IBM CRC is used for error detection on all sector ID fields and floppy disk data fields. The detection capability of this code is excellent when it is used for detection only. SMS recommends that the code be used for detection under normal operation. Occasionally however, a single bit error will develop in a valuable file, such as on a backup floppy diskette. Under these circumstances the FWD5000 may be used to recover the data by enabling ECC on the read.

Winchester disk data integrity is provided by a 24 bit Fire code. This code will detect all bursts of 10 bits or less and will correct all bursts of 6 bits or less. All error correction codes, including the SMS code, have some probability of miscorrection. This occurs when a group of independent errors result in the same error residue as would have occurred with a certain correctable error. To prevent this situation, the FWD5000 saves all error residues from the first read, reads the sector again, and compares the residue before making a correction. This process virtually guarantees user data integrity. The price for this reliability is that two disk revolutions, rather than one, elapse whenever an error is encountered. This results in negligible performance loss and is well worth the price. The error correction function may be disabled by the user if for some reason he desires detection only.

E. FWD5000 DIAGNOSTICS

Whenever power is applied, or a reset operation performed, W4 and W5 are checked to determine what diagnostic program is to be performed. See Table 1.

TABLE 1. DIAGNOSTIC OPTIONS

	W4	W5	
	OUT	OUT	Run drive test continuously and halt on error.
	OUT	IN	No test to be performed. Start functional program immediately.
	IN	OUT	Format ready drives, run drive test continuously and halt on error.
*	IN	IN	Run self test once and start functional program if no error.

*Factory configuration at shipment.

A single LED is supplied to report the result of the diagnostics as described in the following paragraphs.

Self Test

Self test is an exercise program designed to test the controller hardware as thoroughly as is possible. Pattern testing is done on the RAM, checksum is done on the ROM, and the disk interface hardware is checked. If the self test completes successfully, the on-board LED will be turned off.

Drive Test

Drive test is an exercise program designed to test the entire drive controller sub-system. The first step of drive test is to run the self test. If the self test fails, the on-board LED will remain on. The next step of the drive test is a random seek and read operation on all ready drives in the system (no data is written). (The controller will wait for up to 30 sec. for W0 to go ready before starting the seek/read test or Winchester format.) If a failure occurs at this step, or if there are no ready drives, the on-board LED will blink on and off at a 100 ms rate and self test will continue to loop. If both parts of the test pass, the LED will be turned off and the test execution begun again. If self test fails at any point after the initial pass, the LED will be turned on. Note that if the format is performed before drive test, both the floppy and the Winchester will be formatted using the SA1403D compatible formats (FM0-FM2=000).

II. DISK SURFACE MANAGEMENT AND FORMATS

A. DISK SURFACE LAYOUT

The surface of a disk (both floppy and fixed) is divided into a series of concentric circles. Each one of these circles is called a track. As the disk rotates, a track passes under a read/write head which is used to transfer information from/to the disk. Many disk drives support multiple read/write heads, all of which are mounted on a single carriage. The carriage moves or positions the heads over the disk surface. On drives which support multiple heads, all tracks which can be accessed from one position of the carriage are called a cylinder. Thus a cylinder consists of 1 to N tracks where N is the number of read/write heads mounted on the carriage.

Each track is divided into several records called sectors. The sectors are numbered from 1 to X where X is the number of sectors per track. The number of sectors per cylinder is thus X times the number of heads. All sectors on one cylinder are of the same size.

B. SECTOR INTERLEAVING

When sector interleaving is used, consecutive sectors on a disk are never read or written. Interleaving typically does not affect disk storage capacity, but does affect system throughput and performance.

Interleaving normally is used to reduce the effective data transfer rate. For example, on a buffered transfer, an interleave may be used so that the next sector to be transferred is available immediately after the buffer has been filled or emptied. Interleaving can be accomplished logically by host software, or physically when the disk is formatted.

When interleaving is used, any physical offset (see next section) and interleave are not additive. The number of sectors skipped is the greater of the offset and interleave factor.

C. CYLINDER OFFSET

Cylinder offsetting is a technique used to improve system performance on transfers crossing cylinder boundaries. To understand why cylinder offsetting is useful, it is necessary to look at the timing constraints of a disk drive. A disk drive can take from 10 to 20 msec to move a read/write head from one cylinder to the next (see specification section). If a transfer is taking place such that the last sector on track X has just been read and the next sector to be read is the first sector on track X+1, it is desirable to be able to read this sector as soon as the head has been positioned over track X+1. Typically this is not possible because step time is greater than the delay provided by the disk rotation. Thus the controller must wait an entire rotation before the desired sector can be read. This controller allows offsets on both the fixed and floppy disks to improve system performance. See Table 2 for SMS recommended cylinder offsets on the Winchester.

D. HEAD OFFSET

The head offset is similar in concept to the cylinder offset. A certain amount of time is required for the controller to deselect one head and select another due to controller overhead and drive requirements (see specification section). Head offset is provided such that the next sector to be transferred will be available after this delay has elapsed. See Table 2 for SMS recommended head offsets on the Winchester.

E. FLOPPY DISK FORMAT

This controller supports the IBM single/double density formats. These formats are 'soft-sectored' formats. This means that the position of each sector on a track is marked by the controller writing a special pattern, called an address mark (AM), on the diskette. The address mark, along with other identification data (track, head, sector and format), is written only when the diskette is formatted. In normal reads/writes only the data, data address mark and data CRC bytes are written.

It is important to distinguish between what 'formatting' a diskette means versus how the data is arranged on the diskette. Format implies what the encoding type is, what address marks are used and the number of bytes per sector. On the other hand, data can be arranged by the host on the diskette using various interleave and offset factors.

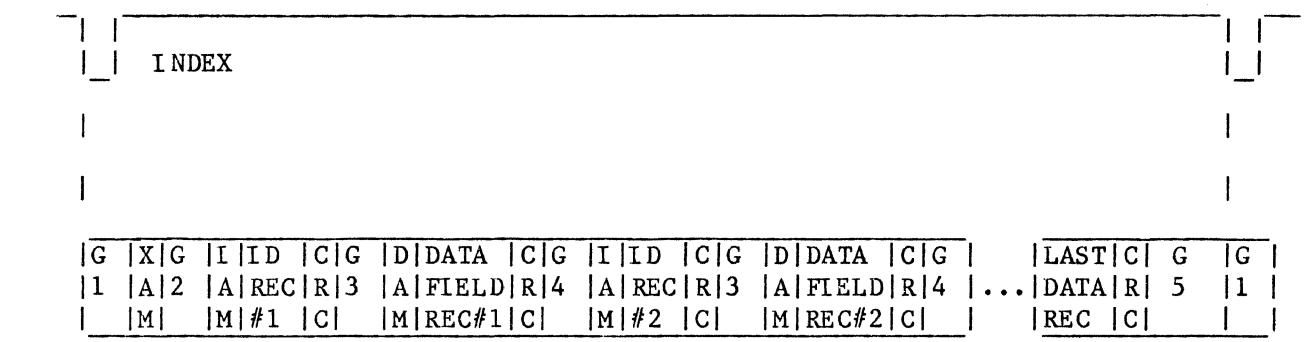
The IBM single density format implies frequency modulation (FM) encoding and single byte address marks. The IBM double density format implies Modified Frequency Modulation (MFM) and four byte address marks.

The IBM formats have one other important feature -- the format of the first track is constant regardless of the format of the remainder of the diskette. The format for cylinder 0, head 0 is IBM single density, 128 bytes/sector. If the diskette is double sided cylinder 0, head 1 can be one of two formats only. These are single density, 128 bytes/sector if the remainder of the diskette is single density or double density, 256 bytes/sector if the remainder of the diskette is double density.

The following table summarizes the aspects of the various formats:

Density	Encoding	Bytes/ Sect.	Sect./ Track	Gap 4	Gap 5
IBM SD	FM	128	26	33	274
		256	15	48	212
		512	8	72	313
		1024	4	86	667
IBM DD	MFM	256	26	66	653
		512	16	61	352
		1024	8	128	771

The arrangement of sectors, ID, etc. on each floppy track is shown below:

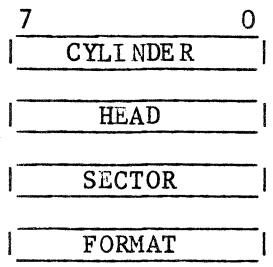


where G1 to G5 is GAP1 to GAP5
XAM is Index Address Mark (1 byte in single density, 4 in double density)
IAM is ID Address Mark (1 byte in single density, 4 in double density)
ID REC is ID Record (4 bytes)
DAM is Data address mark (1 byte in single density, 4 in double density)
CRC is Cyclic Redundancy Check (2 bytes)
Gaps 1,2 and 3 are fixed and have the following values:

	Gap 1	Gap 2	Gap 3
IBM Single Density	46	32	17
IBM Double Density	92	62	34

Gaps 4 and 5 vary depending on the diskette format and drive tolerance. The nominal values for these gaps are shown on the previous page.

Each ID record consists of 4 bytes in the following format:

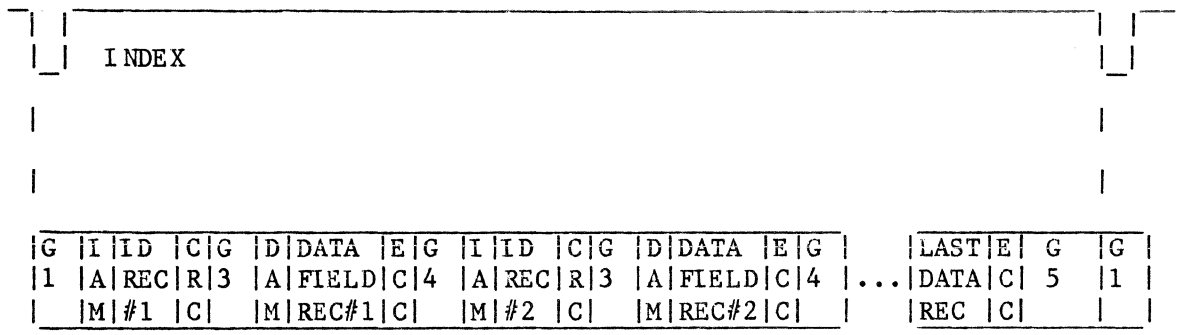


where format 00 (hex) = 128 bytes/sector
01 (hex) = 256 bytes/sector
02 (hex) = 512 bytes/sector
03 (hex) =1024 bytes/sector

Note that all floppy diskettes contain 77 cylinders addressed from 0 to 76. The single sided drive has one head addressed 0. The double sided drive has two heads per cylinder addressed 0 and 1. If a single sided diskette is used in a double sided drive, head 1 should not be accessed. On all floppy formats the sectors are addressed from 1 to N where N is the number of sectors per track (per side).

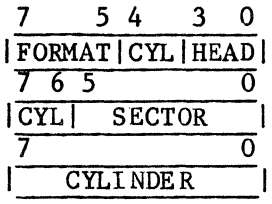
F. FIXED DISK FORMAT

The SA1000 and Q2000 series are soft sectored Winchesters and the track format is similar to the floppy disk except that there is no index address mark (XAM) or gap 2 (G2). This means that gap 1 immediately precedes the ID address mark for sector 1. It should also be noted that the 2 byte data CRC which is used on the floppy disk is replaced with a 3 byte data ECC capable of detecting all bursts of up to 10 bits and correcting up to a 6 bit burst error. The arrangement of sectors, ID, etc., on each track is shown below:



where G1 to G5 is GAP1 to GAP5
IAM is ID Address Mark (3 bytes)
ID REC is ID Record (3 bytes)
DAM is Data address mark (1 byte)
CRC is Cyclic Redundancy Check (2 bytes)
ECC is Error Correction Code (3 bytes)
Gap 1 is fixed at 18 bytes (includes sync bytes which precede AM)
Gap 3 is fixed at 14 bytes (includes sync bytes which precede AM)
Gap 4 and Gap 5 depend on format (see Table 2).

Each ID record consists of 3 bytes in the following format:



where format 01 (hex) = 32 256 byte sectors/track
05 (hex) = 31 256 byte sectors/track
02 (hex) = 17 512 byte sectors/track
06 (hex) = 16 512 byte sectors/track

In the following table the capacities of the four different formats are shown. Due to the fact that there is no clock track on the Winchester, rotational velocity variation will result in changes in the gap size after the data has been overwritten. The users choice of format must then reflect the particular line frequency variation in his area of use. SMS feels that any of these formats may be used without sector interleave with U.S. domestic power.

TABLE 2. WINCHESTER FORMATS

FORMAT	SPEED TOL.* W	W/O	GAP 4 '00'	GAP 5 '4E'	CYL OFF 1000	2000	HD OFF	COMMAND BYTE 6 FM2	FM1	FM0
256 byte - 32 sectors/track	1.59%	2.83%	34	320	2 hex	1C hex	2	0	0	0
256 byte - 31 sectors/track	3.30%	3.50%	44	336	2 hex	1C hex	2	1	0	0
512 byte - 17 sectors/track	2.90%	3.50%	57	340	2 hex	F hex	2	0	1	0
512 byte - 16 sectors/track	3.50%	3.50%	93	395	2 hex	F hex	2	1	1	0

* W implies rotation to rotation with write to read recovery (i.e. used for consecutive sectors)
W/O implies rotation to rotation without write to read recovery (i.e. used for interleaved sectors).

Table 2 shows that if command byte 6 has FM2-FM0 of 000, a format with 32 256 byte sectors per track is indicated. This format may be used reliably for consecutive sector transfer as long as the time from index to index does not vary by more than $\pm$ 1.59%.

The user should select interleave based upon his system performance requirements and limitations.

The Shugart SA1000 series of drives all contain 256 cylinders addressed from 0 to 255. The SA1002 has two heads per cylinder addressed 0 and 1. The SA1004 has four heads per cylinder addressed 0 to 3. The SA1100 series of drives all contain 660 cylinders addressed from 0 to 659. The SA1104 has three heads per cylinder addressed 0 to 2. The SA1106 has five heads addressed 0 to 4. In all cases, the sectors are addressed from 1 to N where N is the maximum number of sectors per track (per head). The total formatted capacities are shown in Table 3.

The Quantum 2000 series of drives contain 512 cylinders addressed from 0 to 511 except Q2080 which contains 1172 cylinders, addressed from 0 to 1171. The Q2010 has two heads per cylinder addressed 0 and 1. The Q2020 has four heads per cylinder address 0 to 3. The Q2080 has seven heads addressed 0 to 6. The Q2040 has eight heads per cylinder addressed 0 to 7. Formatted capacities are shown in Table 3.

TABLE 3. WINCHESTER CAPACITIES.

FORMAT	SA1002	SA1004	SA1104	SA1106	Q2010	Q2020	Q2080	Q2040
256 byte - 32 sectors/track	4.194M	8.388M	16.22M	27.03M	8.388M	16.77M	67.21M	33.55M
256 byte - 31 sectors/track	4.063M	8.126M	15.71M	26.18M	8.126M	16.25M	65.11M	32.50M
512 byte - 17 sectors/track	4.456M	8.912M	17.23M	28.72M	8.912M	17.82M	71.41M	35.65M
512 byte - 16 sectors/track	4.194M	8.388M	16.22M	27.03M	8.388M	16.77M	67.21M	33.55M

G. LOGICAL ADDRESSING

The FWD5000 allows sectors to be addressed logically as well as physically. Logical records are addressed sequentially with logical record 0 beginning at cylinder 0, head 0, and sector 1. All heads are accessed sequentially up to the maximum number, then the next sequential cylinder is accessed beginning with head zero. The number of logical records available is one less than the number of sectors on the disk (since logical records start at 0). Table 4 lists the maximum logical record number (MLRN) as a function of device type and format. Note: The maximum logical record numbers for the SA860 and the TM848 are the same as listed for the SA850.

Logical addressing is used by the FWD5000 controller whenever the PA bit is set to zero in the sixth command byte. Twenty-one bits are used to form the logical address with byte 2 bit 4 as most significant bit and byte 4 bit 0 as least significant bit. When logical addressing is enabled, the command format is identical to the SA1403D. See command descriptions for details.

TABLE 4. MAXIMUM LOGICAL RECORD NUMBER

DEVICE	FORMAT	MLRN	DEVICE	FORMAT	MLRN
SA800	SD 128	2001*	SA800	DD 256	2001
SA800	SD 256	1165	SA800	DD 512	1241
SA800	SD 512	633	SA800	DD 1024	633
SA800	SD 1024	329			
SA850	SD 128	4003	SA850	DD 256	4003*
SA850	SD 256	2331	SA850	DD 512	2483
SA850	SD 512	1267	SA850	DD 1024	1267
SA850	SD 1024	659			
SA1002	32 x 256	16383*	SA1002	17 x 512	8703
SA1002	31 x 256	15871	SA1002	16 x 512	8191
SA1004	32 x 256	32767*	SA1004	17 x 512	17407
SA1004	31 x 256	31743	SA1004	16 x 512	16383
Q2010	32 x 256	32767	Q2010	17 x 512	17407
Q2010	31 x 256	31743	Q2010	16 x 512	16383
Q2020	32 x 256	65535	Q2020	17 x 512	34815
Q2020	31 x 256	63487	Q2020	16 x 512	32767
Q2080	32 x 256	262527	Q2080	17 x 512	139467
Q2080	31 x 256	254323	Q2080	16 x 512	131263
Q2040	32 x 256	131071	Q2040	17 x 512	69631
Q2040	31 x 256	126975	Q2040	16 x 512	65535
SA1104	32 x 256	63359	SA1104	17 x 512	33659
SA1104	31 x 256	61379	SA1104	16 x 512	31679
SA1106	32 x 256	105599	SA1106	17 x 512	56099
SA1106	31 x 256	102299	SA1106	16 x 512	52799

* SA1403D compatible format

III. COMMANDS AND STATUS

Each FWD5000 command consists of six bytes which are sent to the controller according to the protocol described in section IV. Two bytes of status are returned at the completion of each command according to the protocol defined in section IV. The following section describes the content of the command and status bytes and details command operation.

In all cases the floppy and Winchester drive types are determined from W6, W8, W9, W10, and W11 (see Table 13) which must be properly set when power is applied to the board. For all commands, drive addresses 0 and 1 are reserved for Winchester drives, and drive addresses 2 and 3 are reserved for floppy drives.

For all the following command descriptions, bit 0 is shown on the right and is assumed to be the least significant bit. The least significant bit of any field is the rightmost bit or the bit with the smallest bit position number. These bit position numbers are carried through as the data bus numbers on the interface connector. In other words, command bit 0 corresponds to data bus bit 0 on J06 pin 2 and should be wired to the least significant bit of the host port.

A. FORMAT COMMAND

7	6	5	4	3	2	1	0	
0	0	0	0	0	1	0	0	1st byte
0	DA1	DA0	HO4	HO3	HO2	HO1	HO0	2nd byte
0	0	0	0	0	0	0	0	3rd byte
0	0	0	CO4	CO3	CO2	CO1	CO0	4th byte
0	0	0	SI4	SI3	SI2	SI1	SI0	5th byte
0	0	0	0	OE	FM2	FM1	FM0	6th byte

DA0 - DA1: Drive address field (0 and 1 Winchester; 2 and 3 floppy)

OE: Offset enable bit. If OE=0 the H0 and C0 fields are ignored (SA1403D compatible).

C00 - C04: Cylinder offset field specifies the number of sectors following the last sector on the last head of the previous cylinder, and preceeding sector 1 on the current cylinder. An offset of zero or one results in no intermediate sectors, an offset of two results in a single intermediate sector, etc. See Table 2 for recommended offsets.

H00 - H04: Head offset field determines the number of sectors following the last sector on the last head of the previous track, and preceeding sector 1 on the current track. An offset of zero or one results in no intermediate sectors, an offset of two results in a single intermediate sector, etc. The head offset is not used at cylinder boundaries. See Table 2 for recommended offsets.

SI0 - SI4: Sector interleave field determines the number of intermediate sectors between sectors with sequential addresses (i.e. sequential data). An interleave of zero or one is defined to be no interleave. An interleave of two has a single sector between sectors which are read consecutively. At a cylinder boundary, the greater of cylinder offset and the interleave will be chosen as the actual offset. At a track boundary the greater of head offset and interleave will be used as the actual offset.

FM0 - FM2: Format field determines density, sector size and number of sectors per track as shown (see II-E and F for details):

For Winchester (DA=0 or 1):

FM2	FM1	FM0		FM2	FM1	FM0	
1	1	1	illegal	0	1	1	illegal
1	1	0	16 x 512	0	1	0	17 x 512
1	0	1	illegal	0	0	1	illegal
1	0	0	31 x 256	0	0	0	32 x 256

For floppy (DA=2 or 3):

FM2	FM1	FM0		FM2	FM1	FM0		
1	1	1	SD 1024	0	1	1	DD 1024	
1	1	0	SD 512	0	1	0	DD 512	
1	0	1	SD 256	0	0	1	DD 256	
1	0	0	SD 128	0	0	0	DD 256	if 2 sided diskette, else SD 128.

The FORMAT command causes the controller to initialize an entire disk (or diskette) with address marks, sector ID fields, record gaps, and E5 (hex) bytes in every sector as specified by the selected drive and format.

If a single density diskette is being formatted, track 0 sides 0 and 1 (cylinder 0) will be formatted using 128 byte sectors irrespective of the specified sector size. If a double density diskette is being formatted, track 0 side 0 will be formatted using 128 byte single density sectors and track 0 side 1 will be formatted using 256 byte double density sectors irrespective of the specified sector size. All other sectors will be formatted according to the sector size and density specified in command byte 6. This procedure is required for IBM compatibility.

Status is returned upon completion of the FORMAT command or upon error termination. See section IV for state and timing details on status transfer.

B. FORMAT TRACK COMMAND

7	6	5	4	3	2	1	0	
0	0	0	0	0	1	1	0	1st byte
0	DA1	DA0	CA10	HA3	HA2	HA1	HA0	2nd byte
CA9	CA8	X	A04	A03	A02	A01	A00	3rd byte
CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	4th byte
X	X	X	SI4	SI3	SI2	SI1	SI0	5th byte
0	0	0	0	PA (OE)	FMZ	FM1	FM0	6th byte

DA0 - DA1: Drive address field (0 and 1 Winchester; 2 and 3 floppy)

CA0 - CA10: Cylinder address field (if PA = 1)

HA0 - HA3: Head address field (if PA = 1)

A00 - A04: Absolute offsetfield (if PA = 1). Determines the offset from index to the first sector on the selected track. A0=1, first sector will start at index.

PA (OE): The physical addressing (offset enable) bit, If PA=1, allows physical addressing with the absolute offset (A00-A04) enabled. If PA=0, logical addressing with no offsetting is used (SA1403D compatible). The 21 bit logical address is determined with byte 2 bit 4 the MS bit and byte 4 bit 0 the LS bit. The FWD5000 converts the logical address to physical and uses only the head and cylinder address, the sector is unused in format track.

SI0 - SI4: Sector interleave field determines the number of intermediate sectors between sectors with sequential addresses (i.e. sequential data). An interleave of zero or one is defined to be no interleave. An interleave of two has a single sector between sectors which are read consecutively.

FM0 - FM2: Format field determines density, sector size and number of sectors per track as shown (see II-E and F for details):

For Winchester (DA=0 or 1):

FM2	FM1	FM0		FM2	FM1	FM0	
1	1	1	illegal	0	1	1	illegal
1	1	0	16 x 512	0	1	0	17 x 512
1	0	1	illegal	0	0	1	illegal
1	0	0	31 x 256	0	0	0	32 x 256

For floppy (DA=2 or 3):

FM2	FM1	FM0		FM2	FM1	FM0		
1	1	1	SD 1024	0	1	1	DD 1024	
1	1	0	SD 512	0	1	0	DD 512	
1	0	1	SD 256	0	0	1	DD 256	
1	0	0	SD 128	0	0	0	DD 256	if 2 sided diskette, else SD 128.

The format track command causes the controller to initialize a single track on a Winchester disk (or floppy diskette) with address marks, sector ID fields, Record gaps, and E5 (NEX) bytes in every sector.

If a single density diskette is being formatted, track 0 sides 0 and 1 (cylinder 0) will be formatted using 128 byte sectors irrespective of the specified sector size. If a double density diskette is being formatted, track 0 side 0 will be formatted using 128 byte single density sectors and track 0 side 1 will be formatted using 256 byte double density sectors irrespective of the specified sector size. All other sectors will be formatted according to the sector size and density specified in command byte 6. This procedure is required for IBM compatibility.

Status is returned upon completion of the FORMAT TRACK command or upon error termination. See section IV for state and timing details on status transfer.

C. WRITE COMMAND

7	6	5	4	3	2	1	0	
0	0	0	FH	1	0	1	0	1st byte
0	DA1	DA0	CA10	HA3	HA2	HA1	HA0	2nd byte
CA9	CA8	SA5	SA4	SA3	SA2	SA1	SA0	3rd byte
CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	4th byte
NS7	NS6	NS5	NS4	NS3	NS2	NS1	NS0	5th byte
DR	CC	DD	DT	PA	FM2	FM1	FM0	6th byte

DA0 - DA1: Drive address field (0 and 1 Winchester; 2 and 3 floppy)

FH: Fast handshake bit. When FH=1, the fast handshake is used on buffered transfers to allow the user more time to perform the memory access (thereby reducing interleave). See section IV-B DATA TRANSFER for timing details.

DT: Direct transfer bit. When DT=1 the transfer is direct from host to disk. When DT=0 the transfer is through the buffer.

DD: Deleted data bit. When DD=1 each sector is written with IBM compatible deleted data address marks. DD is not used on the Winchester.

CC: Correction control for buffered transfers; does not affect write operation.

DR: Disable retry bit. When DR=1 no retries are performed.

FM0 - FM2: Format field. For Winchester (DA=0 or 1):

FM2	FM1	FM0		FM2	FM1	FM0	
1	1	1	illegal	0	1	1	illegal
1	1	0	16 x 512	0	1	0	17 x 512
1	0	1	illegal	0	0	1	illegal
1	0	0	31 x 256	0	0	0	32 x 256

For floppy (DA=2 or 3):

FM2	FM1	FM0		FM2	FM1	FM0	
1	1	1	SD 1024	0	1	1	DD 1024
1	1	0	SD 512	0	1	0	DD 512
1	0	1	SD 256	0	0	1	DD 256
1	0	0	SD 128	0	0	0	DD 256 if 2 sided diskette, else SD 128.

PA: Physical address bit. If PA=1 then physical addressing is used (as shown in command bytes and described below). If PA=0, a 21-bit logical sector address is determined with byte 2 bit 4 the MS bit and byte 4 bit 0 the LS bit.

CA0 -CA10: Cylinder address of starting sector (if PA=1).

HA0 - HA3: Head address of starting sector (if PA=1).

SA0 - SA5: Sector address field of starting sector (if PA=1).

NS0 - NS7: Number of sectors to be written on this operation. When this field is zero, 256 sectors will be transferred.

The WRITE command initiates a write of one or more sectors on the disk. The controller will seek the heads to the specified cylinder and verify position automatically.

If the transfer is direct, the controller will wait for the target sector and then handshake the data from the host at disk rate until all sectors have been transferred. Note that interruptions in the data stream timing will occur during gaps and access operations. See section IV for handshake and timing details. The data address mark and ECC/CRC bytes are automatically written by the controller. Note that if a data overrun error occurs during a direct transfer (see section IV), the handshake will stop and the controller will complete the sector with random data and correct CRC/ECC.

If the transfer is buffered, the controller will handshake the data from the host at host rate until the first sector is in the buffer. Any required seek will be done while the buffer is being filled. The buffer will then be written to the target sector and the buffer fill operation begun again until all sectors have been transferred. See section IV for handshake and timing details. The data address mark and ECC/CRC bytes are automatically written by the controller.

If for any reason a sector cannot be located, the WRITE command will be terminated and status returned with the error bit set. The SENSE command is used to determine the cause of failure. If retries are enabled, any error which could be caused by incorrect head positioning (i.e. positioning error, no AM's error, sector ID error) is retried up to two times with a head recalibrate on each retry before status is returned. The retry bit in the second status byte will be set if retries were performed even if the operation was successful. See section IV for details on command termination and see status description at end of this section for status details. Status is returned at the end of the command operation if no errors occur during transfer.

D. READ COMMAND

7	6	5	4	3	2	1	0	
0	0	0	FH	1	0	0	0	1st byte
0	DA1	DA0	CA10	HA3	HA2	HA1	HA0	2nd byte
CA9	CA8	SA5	SA4	SA3	SA2	SA1	SA0	3rd byte
CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	4th byte
NS7	NS6	NS5	NS4	NS3	NS2	NS1	NS0	5th byte
DR	CC	DD	DT	PA	FM2	FM1	FM0	6th byte

DA0 - DA1: Drive address field (0 and 1 Winchester; 2 and 3 floppy)

FH: Fast handshake bit. When FH=1, the fast handshake is used on buffered transfers to allow the user more time to perform the memory access (thereby reducing interleave). See section IV-B for timing details.

DT: Direct transfer bit. When DT=1 the transfer is direct from host to disk. When DT=0 the transfer is through the buffer.

DD: Deleted data bit. Unused for read operations.

CC: Correction control bit. Error correction disable for buffered Winchester transfers. Error correction enable for buffered floppy transfers. For example if CC=0, error correction is performed on Winchester reads but not on floppy reads.

DR: Disable retry bit. When DR=1 no retries are performed.

FM0 - FM2: Format field. For Winchester (DA=0 or 1):

FM2	FM1	FM0		FM2	FM1	FM0	
1	1	1	illegal	0	1	1	illegal
1	1	0	16 x 512	0	1	0	17 x 512
1	0	1	illegal	0	0	1	illegal
1	0	0	31 x 256	0	0	0	32 x 256

For floppy (DA=2 or 3):

FM2	FM1	FM0		FM2	FM1	FM0	
1	1	1	SD 1024	0	1	1	DD 1024
1	1	0	SD 512	0	1	0	DD 512
1	0	1	SD 256	0	0	1	DD 256
1	0	0	SD 128	0	0	0	DD 256 if 2 sided diskette, else SD 128.

PA: Physical address bit. If PA=0, a 21-bit logical sector address is determined with byte 2 bit 4 the MS bit and byte 4 bit 0 the LS bit. If PA=1, the address is physical as described below.

CA0 -CA10: Cylinder address of starting sector (if PA=1).

HA0 - HA3: Head address of starting sector (if PA=1).

SA0 - SA5: Sector address field of starting sector (if PA=1).

NS0 - NS7: Number of sectors to be read on this operation. When this field is zero, 256 sectors will be transferred.

The READ command initiates a read of one or more sectors on the disk. Controller will seek the heads to the specified cylinder and verify position automatically.

If the transfer is direct, the controller will wait for the target sector and then handshake the data to the host at disk rate until all sectors have been transferred. Note that interruptions in the data stream will occur during gaps and access operations. See section IV for handshake and timing details.

If the transfer is buffered, the controller will wait for the target sector and transfer the sector into the buffer. The host must then empty the buffer at host rate. See section IV for handshake and timing details. Any required seek will be performed while the buffer is being emptied. Once the host has emptied the buffer the controller will read the next sector into the buffer. This process continues until all sectors have been transferred. If a correctable ECC error occurs, and error correction has been enabled, the controller will correct the data in the buffer before transfer to the host.

If retries are enabled, any error which could be caused by incorrect head positioning (i.e. positioning error, no AM's error, sector ID error) is retried up to two times with a head recalibrate on each retry before status is returned. A no data AM error or a data ECC/CRC error is fatal on direct transfer and will not be automatically retried even if retries are enabled. A non-correctable ECC error, data CRC error, or no data AM error will be retried up to eight times (with no recalibrate) on buffered transfers.

If the read command operation completes successfully, status will be returned at completion with no errors. The second status byte will contain information on successful retries and error correction. If a fatal error occurs, status will be returned with the error bit set. The SENSE command is used to determine error type. If a deleted data address mark is encountered at any time during a floppy read, the command will be terminated and status returned with the error bit set. The deleted data sector is transferred to the host before termination. The deleted data error code is set in the sense bytes (see SENSE command section III-H).

E. READID COMMAND

7	6	5	4	3	2	1	0	
1	1	1	0	0	0	1	0	1st byte
0	DA1	DA0	0	HA3	HA2	HA1	HA0	2nd byte
0	0	0	0	0	0	0	0	3rd byte
0	0	0	0	0	0	0	0	4th byte
0	0	0	0	0	0	0	0	5th byte
0	0	0	0	0	FM2	0	0	6th byte

DA0 - DA1: Drive address field (0 and 1 Winchester; 2 and 3 floppy)

HA0 - HA3: Head address for read operation

FM2: Single density bit; if set to 0 the read will first be attempted in double density; if set to 1 the read will first be attempted in single density; used for floppy only

The READID command initiates a sector ID search on the current cylinder. The specified head is selected but no seek is performed. If the floppy is addressed, both densities will be attempted before the operation is terminated. The first attempt will be with the density specified in the command.

Six bytes will be transferred to the host according to the normal data transfer protocol. These bytes are described in Table 5. The first four of these bytes are determined from the sector ID field which is read by the READID command. These bytes are valid only if the operation completed without an error as determined by the status bytes. The last two bytes are controller configuration bytes and are valid even though an error occurred on the read access. This allows the host to determine configuration information, such as drive type, even though the drive is not ready.

Normal status is returned at the completion of the READID command. See the status section for details.

TABLE 5. FWD5000 READID BYTES

7	6	5	4	3	2	1	0	
CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	1st byte
CA9	CA8	*	CA10	HA3	HA2	HA1	HA0	2nd byte
*	*	SA5	SA4	SA3	SA2	SA1	SA0	3rd byte
*	*	*	*	*	FM2	FM1	FM0	4th byte
W4	W5	W6	W7	*	*	*	*	5th byte
W8	W9	W10	W11	*	*	*	*	6th byte

CA0 -CA10: Cylinder address of the sector ID field which was read by the Read ID operation.

HA0 - HA3: Head address of the sector ID field.

SA0 - SA5: Sector address of the sector ID field.

FM0 - FM2: Format of the disk or diskette. For Winchester (DA=0 or 1):

FM2	FM1	FM0		FM2	FM1	FM0	
1	1	1	illegal	0	1	1	illegal
1	1	0	16 x 512	0	1	0	17 x 512
1	0	1	illegal	0	0	1	illegal
1	0	0	31 x 256	0	0	0	32 x 256

For floppy (DA=2 or 3):

FM2	FM1	FM0		FM2	FM1	FM0	
1	1	1	SD 1024	0	1	1	DD 1024
1	1	0	SD 512	0	1	0	DD 512
1	0	1	SD 256	0	0	1	DD 256
1	0	0	SD 128	0	0	0	illegal

W4 - W11: Configuration straps read from the FWD5000 controller board. See Table 13 for detailed description of strap meaning.

F. SEEK COMMAND

7	6	5	4	3	2	1	0	
0	0	0	0	1	0	1	1	1st byte
0	DA1	DA0	CA10	0	0	0	0	2nd byte
CA9	CA8	0	0	0	0	0	0	3rd byte
CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	4th byte
0	0	0	0	0	0	0	0	5th byte
0	0	0	0	PA	FM2	FM1	FM0	6th byte

DA0 - DA1: Drive address field (0 and 1 Winchester; 2 and 3 floppy)

PA: Physical address bit. If PA=0, a 21-bit logical sector address is determined with byte 2 bit 4 the MS bit and byte 4 bit 0 the LS bit. If PA=1, the physical cylinder address (CA0-CA9) is the target.

FM0 - FM2: Format field determines the format. For Winchester (DA=0 or 1):

FM2	FM1	FM0		FM2	FM1	FM0	
1	1	1	illegal	0	1	1	illegal
1	1	0	16 x 512	0	1	0	17 x 512
1	0	1	illegal	0	0	1	illegal
1	0	0	31 x 256	0	0	0	32 x 256

For floppy (DA=2 or 3):

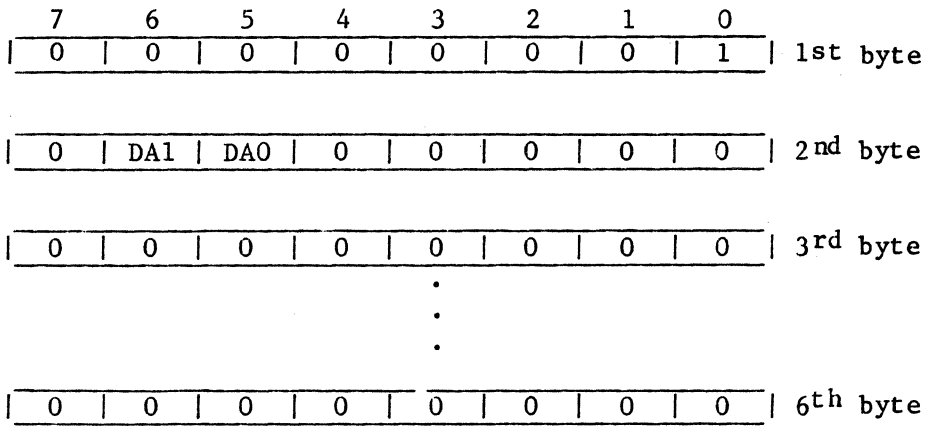
FM2	FM1	FM0		FM2	FM1	FM0	
1	1	1	SD 1024	0	1	1	DD 1024
1	1	0	SD 512	0	1	0	DD 512
1	0	1	SD 256	0	0	1	DD 256
1	0	0	SD 128	0	0	0	DD 256 if 2 sided diskette, else SD 128.

CA0 -CA10: Cylinder address field determines the target cylinder (if PA=1).

The SEEK command performs a seek operation on the addressed drive. The destination cylinder is specified in the command bytes. (If PA=0, the heads will be positioned to the cylinder which contains the specified logical sector.) No verification of target cylinder is performed until a subsequent read or write operation.

If the seek operation is successful, status will be returned with no errors. If an error occurs, the error bit will be set in the status bytes.

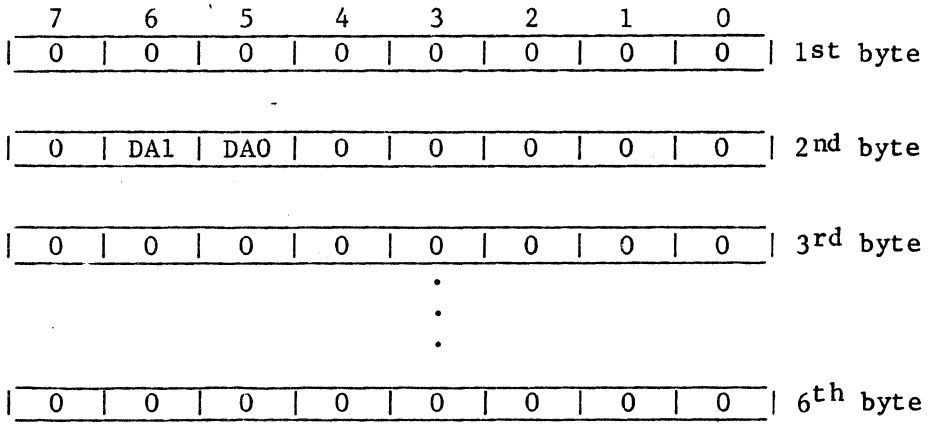
G. RECALIBRATE COMMAND



The RECAL command positions the heads of the addressed drive at cylinder zero. The normal two bytes of status are returned at command completion.

Note that this command is supported for compatibility with the SA1403D. It is never necessary to perform a RECAL on the FWD5000 since the controller will automatically perform a RECAL before a new operation if a new disk has been installed, a seek error has occurred, or power has been applied.

H. TEST READY COMMAND



The TEST READY command selects the drive which is addressed by the DA0-1 bits and tests for ready. The returned status bytes will indicate an error if the drive is not ready.

The TEST READY command is supported for compatibility. It should never be required since the FWD5000 returns both new disk and drive ready bits in the completion status byte.

I. SENSE COMMAND

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	1	1	1st byte
0	DA1	DA0	0	0	0	0	0	2nd byte
0	0	0	0	0	0	0	0	3rd byte
0	0	0	0	0	0	0	0	4th byte
0	0	0	0	0	0	0	0	5th byte
0	0	0	0	PA	0	0	0	6th byte

DA0 - DA1: Drive address field (0 and 1 Winchester; 2 and 3 floppy). This field determines the drive for which status will be returned, however, the sense bytes which are returned DO NOT necessarily apply to this drive address.

PA: Physical address bit. If PA=0, a 21-bit logical sector address is returned in the sense bytes with byte 2 bit 4 as MS bit and byte 4 bit 0 as LS bit. If PA=1, the returned address will be a physical address as described in Table 6.

The SENSE command initiates the transfer of four bytes to the host according to the normal data transfer protocol. These bytes contain the status of the last operation (except for error code byte not necessarily for the drive addressed in the 2nd byte). The structure of these bytes is shown in Table 6. The SENSE command is used to determine the cause of an error and the problem sector when an error is detected in the returned status. The address which is returned in the bytes (see Table 6) is valid only after an error condition on a read or write command.

Note that normal status is returned at the completion of the SENSE command as it is for all commands. These two status bytes will always contain information on the addressed drive rather than on the last operation. See the status section.

TABLE 6. FWD5000 SENSE BYTES

0	0	EC5	EC4	EC3	EC2	EC1	EC0	1st sense byte
0	DA1	DA0	CA10	HA3	HA2	HA1	HA0	2nd sense byte
CA9	CA8	SA5	SA4	SA3	SA2	SA1	SA0	3rd sense byte
CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	4th sense byte

EC0 - EC5: Error code as described in Table 7.

DA0 - DA1: Drive address field (0 and 1 Winchester; 2 and 3 floppy)

HA0 - HA3: Head address of last operation (if PA=1 in command).*

SA0 - SA5: Sector address of last operation (if PA=1 in command).*

CA0 -CA10: Cylinder address of last operation (if PA=1 in command).*

*If PA=0 in command, a 21-bit logical sector address is returned with byte 2 bit 4 as MS bit and byte 4 bit 0 as LS bit (SA1403D compatible).

Note: The address returned in the sense bytes is valid only after an error condition on a read or a write command. The error code is the last error on the addressed drive. The error code and the address refer to the same error situation only when the drive addressed in the command bytes is the drive which had the most recent read/write error.

TABLE 7. FWD5000 ERROR CODES

ERROR CODE	
00 (00 hex)	No error occurred.
01 (01)	No index error -- no index signal detected from drive.
02 (02)	No seek complete error -- seek did not complete on Winchester.
03 (03)	Write fault error -- Winchester write fault detected.
04 (04)	Not ready error -- unit accessed was not ready.
06 (06)	Track zero error -- no track zero detected on a recalibrate operation.
17 (11)	Data ECC/CRC error -- a CRC error or a non-correctable ECC error was encountered on data field. (May be correctable ECC error if transfer was direct.)
18 (12)	No AM's error -- no sector ID address marks of the specified format were found on track.
19 (13)	No data AM error -- no data AM found on target sector.
20 (14)	Sector ID error -- target sector was not found due to address mismatch or sector ID CRC error.
21 (15)	Positioning error -- cylinder address in sector ID did not compare with target cylinder.
22 (16)	Data overrun error -- host acknowledge occurred late during direct transfer -- transfer stops at error and error reported end of sector.
23 (17)	Write protected error -- command attempted a write or format operation on a write protected diskette.
27 (1B)	Deleted data error -- last sector transferred had a deleted data address mark. (The sector transfer is always completed before this error is reported.)
28 (1C)	Sector length error -- a valid sector ID was found but incorrect sector length was specified in the command bytes.
29 (1D)	Head select error -- a valid sector ID was found but head address field did not match command bytes.
30 (1E)	Density error -- a valid sector ID was found on the floppy but incorrect density was specified in the command bytes.
31 (1F)	Data parity error -- one or more bytes were received with incorrect parity on a write data operation.

TABLE 7. FWD5000 ERROR CODES (continued)

ERROR CODE	
32 (20)	Command error -- illegal command format received. May be illegal op code or ECC enabled on direct transfer.
33 (21)	Logical address error -- illegal logical sector address received on a command using logical addressing.
34 (22)	Sector address error -- illegal sector address received on a command using physical addressing.
35 (23)	Head address error -- illegal head address received on a command using physical addressing.
36 (24)	Cylinder address error -- illegal cylinder address error received on a command using physical addressing.
37 (25)	Buffer error -- received command requested a buffer operation on a 1K byte sector.
39 (27)	Disk overrun error -- transfer attempted beyond end of disk.
40 (28)	Command parity error -- one or more command bytes were received with incorrect parity.
49 (31)	Drive type error -- W8-W11 are strapped illegally such that the controller cannot determine drive type.
50 (32)	Illegal state error -- high speed processor in illegal state. Hardware failure.
51 (33)	Timeout error 1 -- high speed processor did not advance to state 111. Hardware failure.
52 (34)	Timeout error 2 -- high speed processor did not advance to state 0XX. Hardware failure.
53 (35)	Timeout error 3 -- high speed processor did not advance to state XX0. Hardware failure.

J. STATUS

7	6	5	4	3	2	1	0	
0	DA1	DA0	0	0	0	ER	PE	1st byte
*	TO	WP	TS	DR	RT	EC	ND	2nd (completion) byte

PE: Parity error occurred on a previous transfer. Data parity errors will terminate data transfer to/from the host and will be reported at the completion of the current sector on direct transfers. Transfer will continue to end of sector on buffered transfers.

ER: Fatal error occurred on last operation (or deleted data AM found).

DA0 - DA1: Drive address for which the status is valid.

ND: This command was the first after insertion of a new diskette into the floppy. A recalibration was performed automatically on receipt of the previous command. Note: The ND bit is undefined if Tandon TM848 floppy drives are used.

EC: Error correction was performed on transfer -- not a fatal error.

RT: Retries were performed on transfer -- not a fatal error.

DR: Drive is ready if DR is set.

TS: Two sided diskette is installed if TS is set.

WP: Write protected diskette is installed if WP is set.

TO: Drive is positioned at track zero if TO is set.

*: Undefined state

Two bytes of status are returned by the controller at the completion of each command. If the command were terminated by an error condition an error bit in the first byte would be set. If the command completed successfully, the error bits would be zero. The second byte contains drive status information for the drive addressed by the terminating command.

If the error bit is set in the first byte, operation information may be obtained by issuing the SENSE command as previously described. Note however that the SENSE command must be issued before an operation is begun on another drive. The information returned by the SENSE command is valid only for the last operation even though the two status bytes are always valid for the addressed drive. For example, if an error occurred on drive 1, then a write was performed on drive 2, and then a SENSE command was issued to drive 1, the three bytes of address returned by the SENSE command would apply to the write operation on drive 2 (error code status byte applies to addressed drive) and the two status bytes returned at the completion of the SENSE command would apply to drive 1.

The controller notifies the host that status is available by asserting CON and OUT as described in the protocol section. The status bytes are transferred as described in the protocol section.

IV. HOST INTERFACE PROTOCOL

The following section describes the protocol used to transfer commands, data and status between the host and the controller. All commands, data and status are transferred on an 8-bit bidirectional data bus. The controller will generate and check odd parity on this bus if parity is enabled (i.e. W2 is installed).

The host sources three control signals to the controller. The first line is RST. Assertion of this line will force the controller to terminate any current operation and to become ready to accept a command. The second line is SEL. Assertion of this line indicates that the host is prepared to transfer a command to the controller. The third line is ACK. Assertion of this line indicates that the host has accepted the data from the data bus or that the host has placed data on the data bus for transfer to the controller.

The controller sources five state signals to the host. The first line is BSY. Assertion by the controller indicates that an operation is in progress and the controller is not ready to accept a new command. The second line is CON. Assertion by the controller indicates that a command byte or status byte is being transferred on the bus. The third line is OUT. Assertion by the controller indicates that the current transfer is from controller to host. The fourth line is REQ. Assertion by the controller indicates that the controller has accepted the data from the data bus or that the controller has placed data on the data bus for transfer to the host. The last state signal is MSG. Assertion by the controller indicates that the final status byte is to be transferred on the data bus.

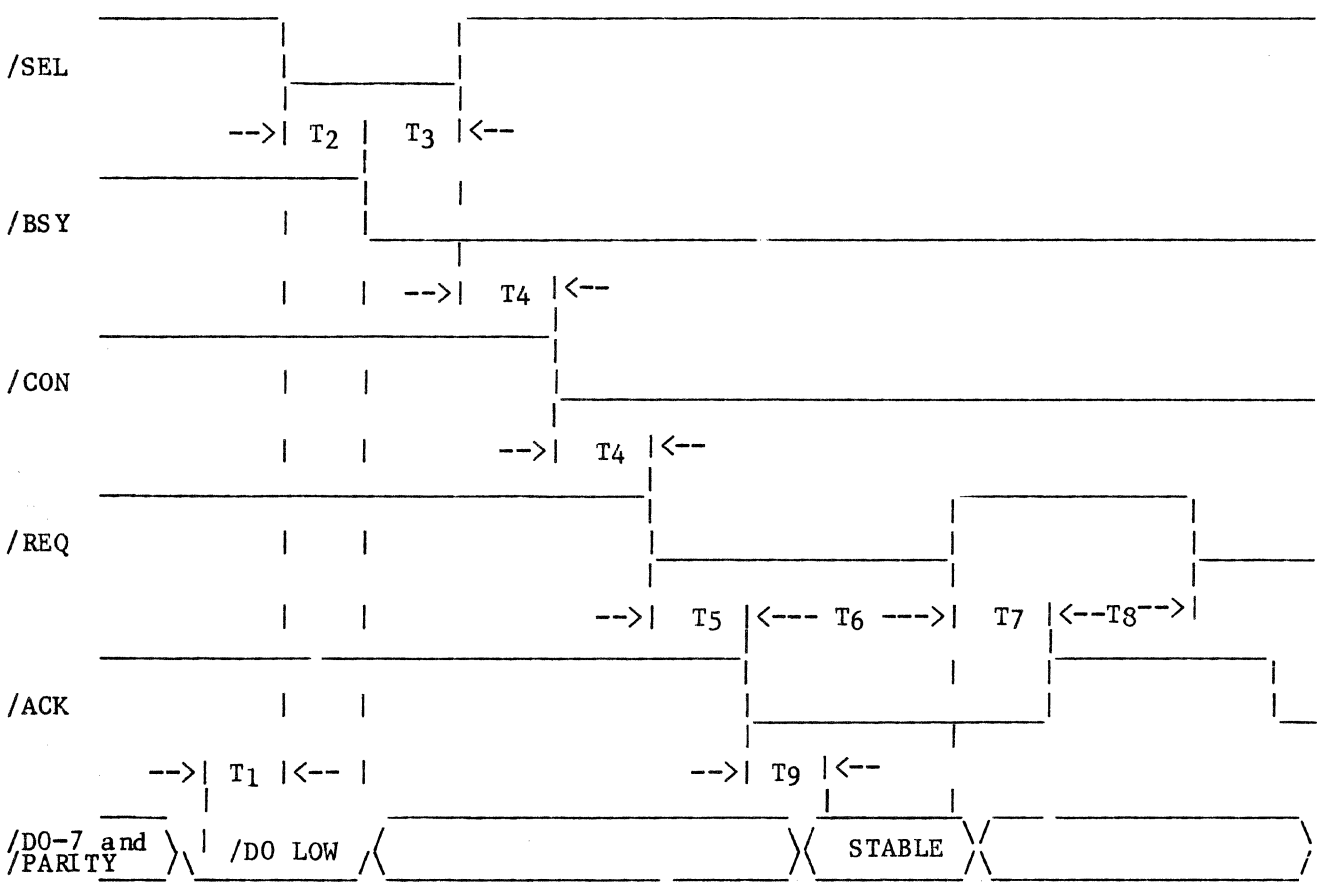
A. COMMAND TRANSFER

All disk controller activity is initiated by the host system via commands. Each of the commands requires a transfer of six bytes from the host to the controller. The content of these bytes and the controller response was discussed in the preceding section.

The host system may request a disk operation by initiating a command transfer. The protocol is shown in Figure 1. The host may initiate command sequences whenever the controller has not asserted the BSY signal. (Note that whenever the controller is not busy, OUT will be deasserted.) The sequence is begun by asserting DO and then asserting the SEL signal. The controller will then assert BSY and the host must then deassert SEL. The FWD5000 will indicate that it is ready to transfer the first byte by asserting the CON and the REQ signals. The host should then place the first command byte on the data port and assert ACK. The command byte should remain stable until the controller deasserts REQ. When the FWD5000 is ready to receive the next byte, it asserts REQ again. The host should place the next command byte on the data port and assert ACK. This procedure should be repeated until six bytes have been transferred. The CON line will remain asserted and OUT will remain deasserted until all command bytes have been passed.

Note that in all cases the command byte must be stable by 400ns after the host asserts ACK and remain stable until REQ is deasserted by the controller. This means that the host may assert ACK prior to placing the byte on the port as long as the byte becomes stable within 400ns. This feature greatly simplifies the hardware required to interface to the controller.

After the last command byte has been transferred, the controller will prepare for either a status or a data transfer. In the case of a WRITE command, OUT will remain deasserted. OUT will be asserted for all other commands. In all cases, OUT will be stable before CON is deasserted to insure that no hazards exist in the host logic. Even if an error was detected during the command transfer or if no data transfer is required, CON will be deasserted for lus (min) and then reasserted to indicate that status is available.



T_1 = 90ns (min)
T_2 = 460ns (min)
T_3 = 0ns (min)
T_4 = 690ns (min)
T_5 = 0ns (min)
T_6 = 460ns (min)
T_7 = 0ns (min)
T_8 = 460ns (min)
T_9 = 400ns (max)

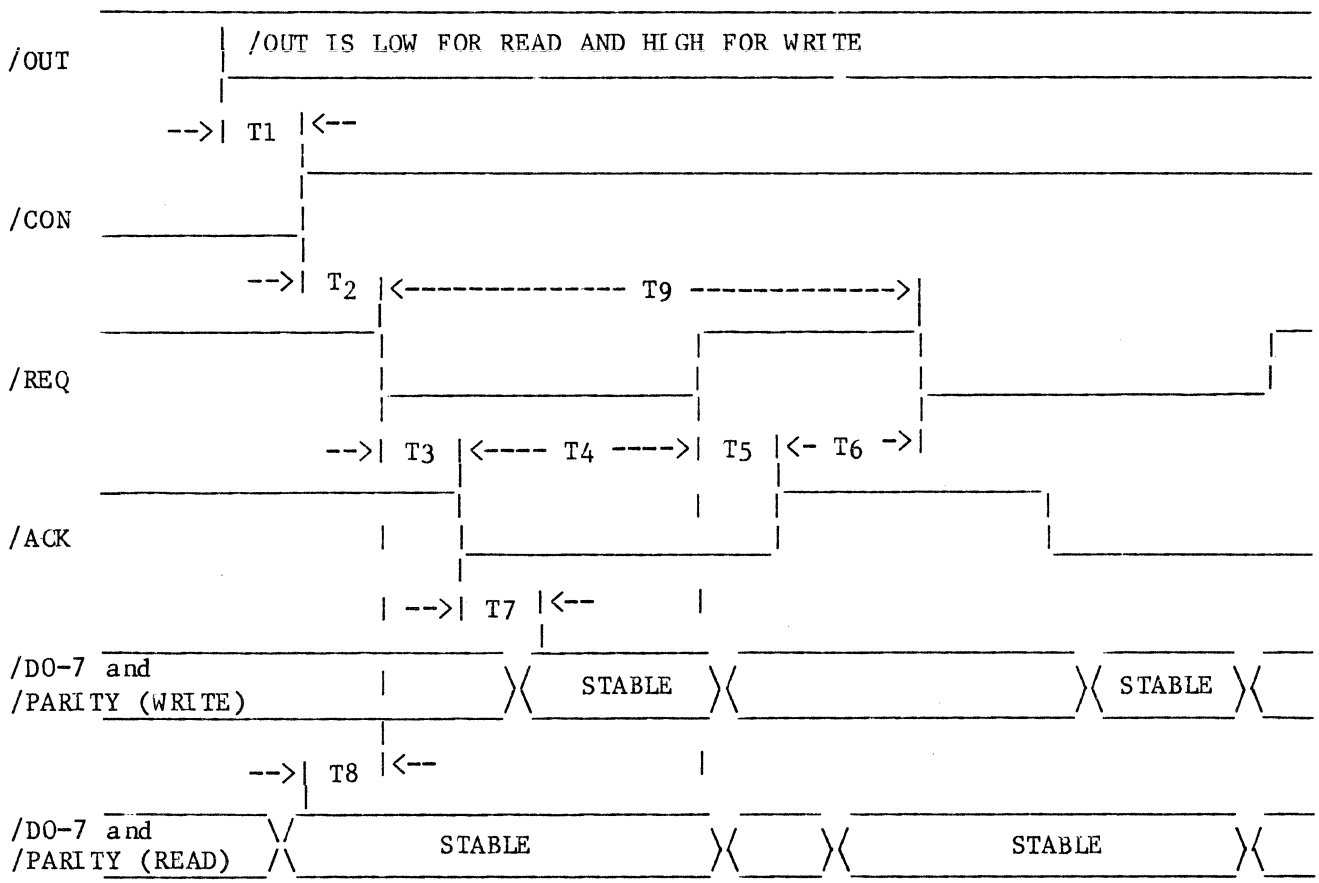
Figure 1. Command Transfer Timing

B. DATA TRANSFER

A data byte transfer request (read or write) is indicated when the controller asserts REQ. The host system, in turn, acknowledges the data byte transfer request by reading/writing the data byte and asserting ACK. When writing to the controller, the byte and parity must be stable 400ns after asserting ACK. When reading, the byte and parity will be stable 350ns before the controller asserts REQ. This is true for buffered and unbuffered transfers.

Buffered Data Transfers

Figure 2 shows the timing for both buffered reading and buffered writing by the host system. In this mode, the controller asserts the REQ signal after placing a data byte on the DATA port (buffered read) or when it is waiting for a new byte from the host (buffered write). When the host acknowledges the data transfer by accepting/sourcing the data and asserting ACK, the controller continues. There are no timing constraints placed on the user's response.



T_1 = 1us (min)
T_2 = 690ns (min), max is function of access delay
T_3 = 0ns (min)
T_4 = 460ns (min)
T_5 = 0ns (min)
T_6 = 460ns (min)
T_7 = 400ns (max)
T_8 = 350ns (min)
T_9 = 1.38us (min) for T_3, T_5 < 230ns

Figure 2. FWD5000 Buffered Data Transfer.

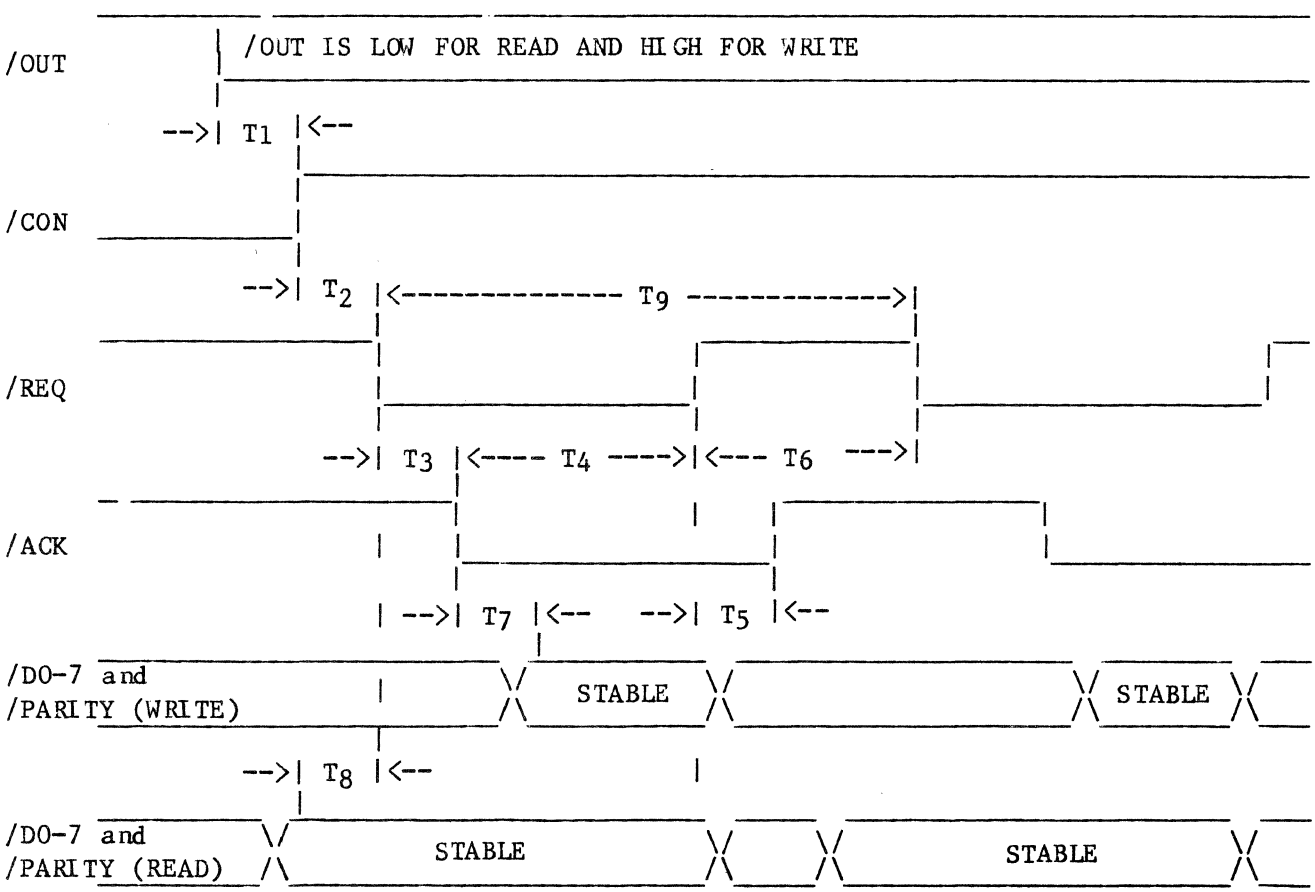
Figure 3 shows the timing for buffered reading and buffered writing when the fast handshake is enabled (FH bit set in command byte). Note that the host memory access is performed during T3 between the assertion of REQ by the controller and the assertion of ACK by the host. With the SA1403D compatible handshake shown in Figure 2, the amount of time allowed for the user memory access is:

$$T_{access\ (max)} = (N \times 230ns) - 1.38us + 230ns$$

where N x 230 is the desired cycle time to read or write one byte. For a single sector interleave on the Winchester, a cycle time of 1.84us (N=8) is required (must empty the buffer in a sector time). Therefore the memory access must be performed in about 690ns maximum. With the SMS fast handshake shown in Figure 3, the amount of time allowed for the user memory access is:

$$T_{access\ (max)} = (N \times 230ns) - 1.15us + 460ns$$

which means that a single sector interleave on the Winchester may be achieved with a host memory access time of 1.15us.

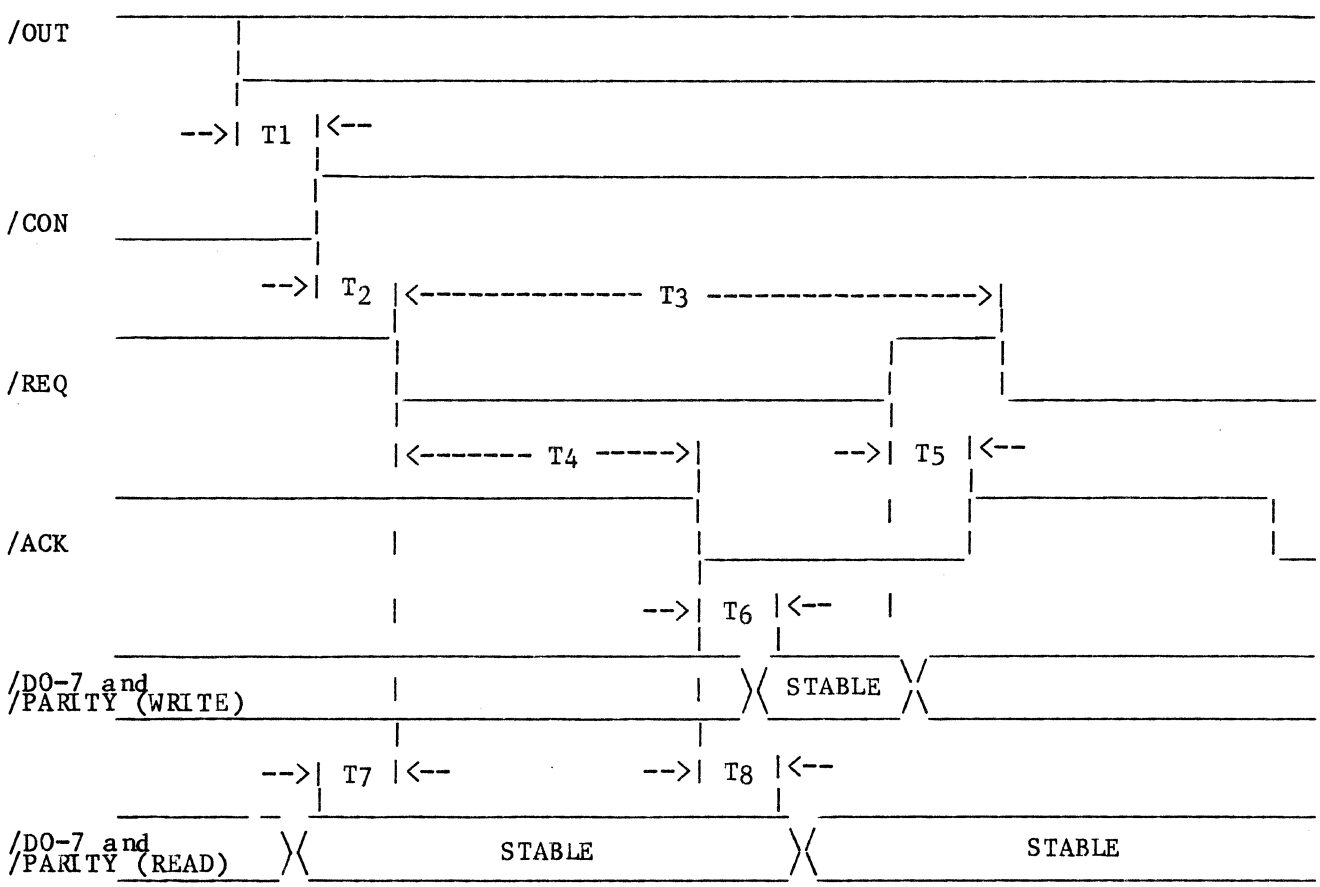


T_1 = 1us (min)
T_2 = 690ns (min), max is function of access delay
T_3 = 0ns (min)
T_4 = 460ns (min)
T_5 = 690ns (max)
T_6 = 230ns
T_7 = 400ns (max)
T_8 = 350ns (min)
T_9 = 1.15us (min) for $T_3 < 460ns$

Figure 3. FWD5000 Buffered Data Transfer (FH=1)

Direct Data Transfers

Figure 4 illustrates direct read/write data transfer. During a floppy read/write operation, REQ is asserted every 32 ± 1.4usec in single density and every 16 ± .75 usec in double density to indicate data is available on the DATA port (read) or data is requested from the host (write). The host acknowledges the data transfer request by asserting ACK. If the host fails to acknowledge a data transfer within 20 usec (nominal) for single density or within 10 usec (nominal) for double density, the read/write operation is aborted and a data overrun error generated. REQ is asserted every 1.84usec ± 64ns during a read/write Winchester operation and the host must acknowledge the transfer within 1.15us (nominal).



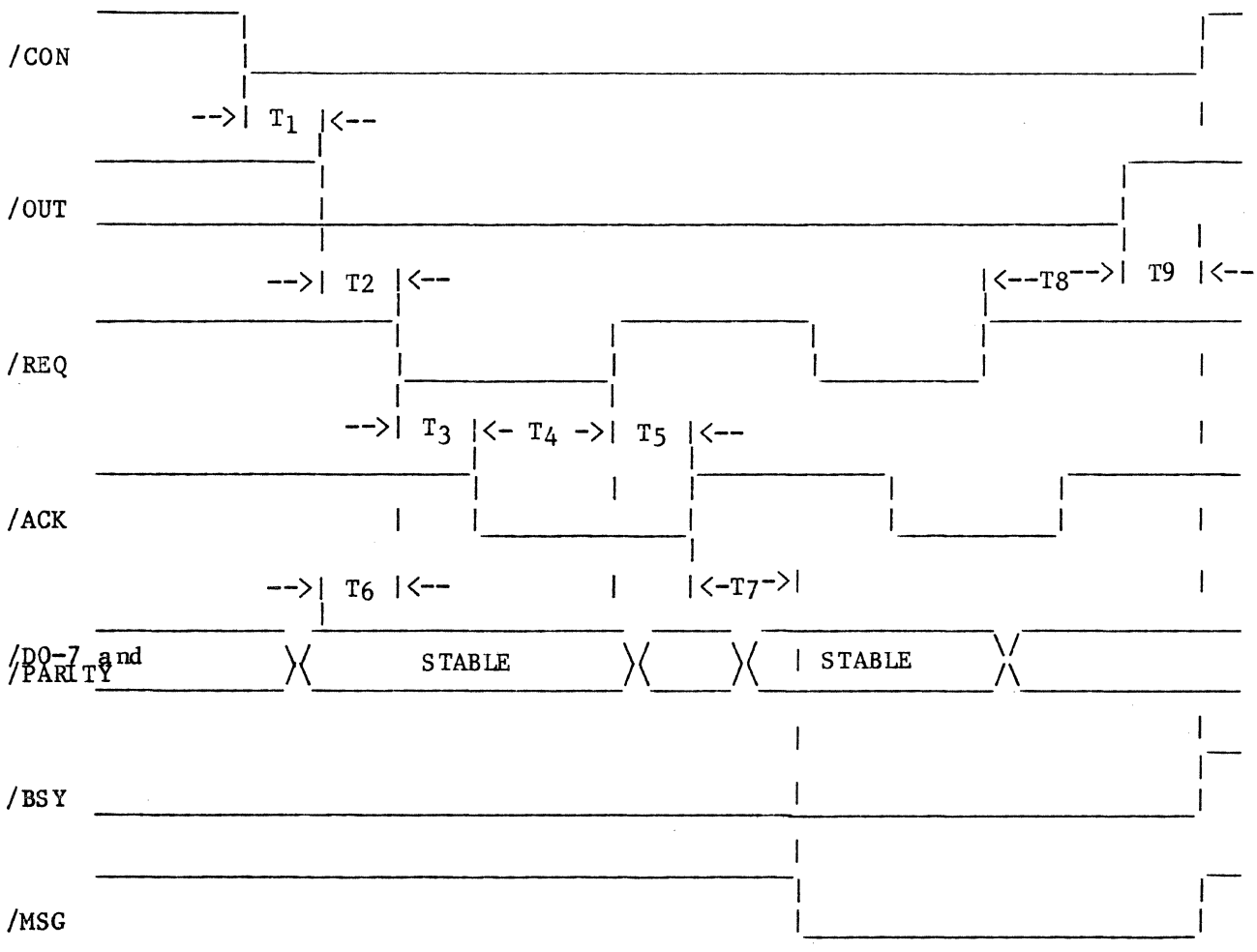
T_1 = 1us (min)
T_2 = 690ns (min), max is function of access delay
T_3 = 32us ± 1.4us (single density floppy)
= 16us ∓ .75us (double density floppy)
=1.84us ∓ 64ns (Winchester)

T_4 = 5/8 T3 (max)
T_5 = 0ns (min), 6/8 T3 (max)
T_6 = 400ns (max)
T_7 = 350ns (min)
T_8 = 230ns (min)

Figure 4. FWD5000 Direct Data Transfer

C. STATUS TRANSFER

Status is presented as two bytes which are made available at completion of all commands. Status is available when the controller asserts CON and OUT. The first byte indicates if an error occurred on the last command. The second byte contains drive status information. The first status byte is placed on the data port by the FWD5000 and REQ is asserted. When the host has read the byte from the data port, it asserts ACK. The FWD5000 then asserts REQ again to indicate the second byte is ready. It then waits for the host to assert ACK after it has read the byte. The controller then deasserts REQ, deasserts CON, deasserts OUT, deasserts BSY, and becomes ready to accept a new command. In all cases the status byte and parity will be stable 350ns before REQ is asserted.



T_1, T_9 = 1us (min)
T_2 = 690ns (min)
T_3 = 0ns (min)
T_4 = 460ns (min)
T_5 = 0ns (min)
T_6 = 350ns (min)
T_7 = 460ns (min)
T_8 = 460ns (min)

Figure 5. Status Transfer

D. INTERFACE INITIALIZATION

The controller may be reset from any state when power is applied or the FWD5000 RST is asserted. The RST is asserted by pulling the /RST line to a low level for 1 usec (min) and then returning the line to a high level. The controller performs a self test sequence (if W4 and W5 are installed) and becomes ready to accept a new command. During the self test the /BSY line will be deasserted. However, if /SEL is asserted by the host during self test, the controller will assert /BSY, /CON, and /REQ only after self test completes. The self test requires less than 500ms to complete.

E. PROTOCOL FEATURES

The FWD5000 host interface protocol has been designed to minimize the cost and complexity of the hardware and software required to interface the controller to the host system. The following considerations may be helpful in the design of your interface.

Handler Simplifications

All commands are six bytes which simplifies the handler design. Note that all six bytes are always transferred, even if a parity error is detected. The handler must be able to assert SEL and monitor BSY under program control. Typically the hardware is designed to perform the request/acknowledge handshake. Once the SEL signal is asserted the command bytes may be written to the port.

Two bytes of status are always available at command completion. These bytes contain enough information so that a SENSE command may be avoided on a successful operation.

Interrupt Design

Once the command has been issued to the controller, the host should be able to continue processing and receive an interrupt at command completion or error termination.

A simple method of interrupt generation requires no gating logic at the host interface. The falling edge of the /CON signal is used directly to generate the interrupt. If this method is used, the host must disable interrupts at the start of the command transfer (before CON is asserted) and re-enable interrupts after CON is asserted. This means that the handler must have access to the CON signal at a processor port. Note that unlike competitive controllers, the FWD5000 always deasserts CON before a status transfer is required, even if an error occurred on command transfer or if no data transfer was required by the command (as in a format operation).

Data Transfer

On all transfers on the data bus the byte is guaranteed to be stable for 350ns before REQ is asserted. This allows REQ to be used directly as the input strobe since adequate setup time is provided for the input data latches. Similarly the data byte is not sampled by the controller for a minimum of 400ns after ACK is asserted by the host. This allows ACK to be used as the output strobe since adequate propagation delay is provided for the output data drivers. Note that when using an output port, such as the 8255, the bulk of the 400ns is needed just for the propagation delay of the MOS device.

The direct data transfer capability of the FWD5000 is extremely valuable from a performance standpoint. Without direct data transfer, systems which can easily accommodate the 16/32us per byte transfer rate of the floppy disk are forced to interleave. Performance is severely degraded on file loads/unloads and backup operations even if the floppy is not used as a primary system device. There are also many systems where direct transfer may be used on the Winchester. The FWD5000 provides 1.15us for the host memory access on a direct transfer -- the SA1403D controller provides only 690ns for the host memory access even when a sector interleave is used. If static RAM, dynamic RAM with hidden refresh, or a FIFO interface is used, even a slow (2 MHz) system can support direct transfer. (See SMS Application Note number 3000672 for detailed information.)

If the user requires buffered operation due to system limitations, the fast handshake provided by the FWD5000 may be used to maximize the performance of buffered operation. With the fast handshake, a full 1.15us is provided for host memory access with a single sector interleave. This makes single sector interleave a possibility for many systems where two sector interleave would be required by the SA1403D controller.

/MSG Signal

The MSG signal is provided to maintain strict hardware and protocol compatibility with the Shugart SA1403D controller. A minimum cost host adapter need not receive this signal. Notice that the second status byte (the completion byte), which is transferred while MSG is asserted, is used by the FWD5000 to pass drive status to the host. This prevents the host from having to issue a SENSE command after a successful operation. The SA1403D controller does not return this information.

V. SPECIFICATIONS

A. PERFORMANCE SPECIFICATIONS

Performance specifications for the FWD5000 controller family are in Table 8.

TABLE 8. FWD5000 PERFORMANCE SPECIFICATIONS

Floppy drives supported:	Shugart 800, 850, 860, Tandon TM848 or compatible
Diskette formats:	IBM Diskette 1, 2/2D with program selected bytes/sector of 128, 256, 512 or 1024 on single density and 256, 512 or 1024 on double density.
Fixed drives supported:	Shugart SA1002, SA1004, SA1104, SA1106, Quantum Q2010, Q2020, Q2080 and Q2040.
Fixed drive format:	MFM encoding with selectable formats of 256 or 512 bytes/sector
Data transfer rates:	IBM diskette 1: 31.25 Kbytes/sec peak IBM 2D: 62.50 Kbytes/sec peak Winchester: 543.5 Kbytes/sec peak
Data capacities:	IBM diskette 1: up to 256 Kbyte capacity IBM 2D: up to 1.24 Mbyte capacity SA1000 Win.: up to 8.90 Mbyte capacity SA1100 Win.: up to 28.72 Mbyte capacity Q2000 Win.: up to 71.40 Mbyte capacity

TABLE 8. FWD5000 PERFORMANCE SPECIFICATIONS (continued)

Data access times:	SA800:	head load time*	35ms
		head step time	8ms
		head settle time	8ms
		rotational latency	167ms
	SA850:	head load time*	50ms
		head step time	3ms
		head settle time	15ms
		head switch time	150us
		rotational latency	167ms
	SA860:	motor on time	165ms
		head step time	3ms
		head settle time	13ms
		rotational latency	167ms
	TM848:	motor on time	750ms
		head step time	3ms
		head settle time	15ms
		rotational latency	167ms
	SA1000:	head step time*	19ms
		head switch time	150us
		rotational latency	19.2ms
		avg. seek latency	70ms
	SA1100:	head step time*	10ms
		rotational latency	19.2ms
		avg. seek latency	35ms
	Q2000:	head step time*	15ms
		head switch time	150us
		rotational latency	20ms
		avg. seek latency	50ms
* includes settle time	Q2080:	head step time	10ms
		head switch	150us
		rotational latency	20ms
		avg. seek latency	40ms

B. FWD5000 ENVIRONMENT RATING

The environmental ratings of the FWD5000 controller are presented in Table 9.

TABLE 9. FWD5000 ENVIRONMENTAL SPECIFICATIONS

Relative humidity:	10 - 90%
Operating temperature*:	0 to 50 degrees C

Wetbulb and dew point temperatures (i.e. humidity temperature combinations) which cause condensation are not allowed.

*Extreme temperatures may require forced air cooling if free convection is restricted, i.e. 50 degrees C ambient requires 150 linear feet/minute over component side of pc board in a typical card cage application.

Storage temperature:	-65 to 70 degrees C

NOTE: Environmental requirements for media may vary.

C. FWD5000 POWER REQUIREMENTS

The FWD5000 PC board receives power via its J203 connector as illustrated in Figure 6. The voltage is 5V ± 5% at a maximum current of 5.00 Amps. Typical operating current is approximately 4.6 Amps. Ripple and noise must be less than 100mV peak to peak. The mating connector is AMP P/N 1-480270-0 with AMP pins P/N 60619-1 or equivalent.

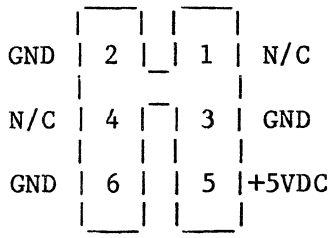


Figure 6. FWD5000 PC Board Power Connector

D. HOST INTERFACE SPECIFICATIONS

All host interface signals are low true and, when asserted, should maintain a level of no greater than .4V. The deasserted signal should maintain a level of greater than 2.5V. Open collector logic should be used for all drivers and 220/330 termination networks must be used at the receiver. The receiver should guarantee a low threshold of .8V minimum and a high threshold of 2V maximum. Since the data bus is bidirectional, 220/330 networks must terminate both ends and 48mA drivers must be used. Other signals are terminated only at the receiver and therefore 24mA drivers may be used. See Figure 7 for schematic details.

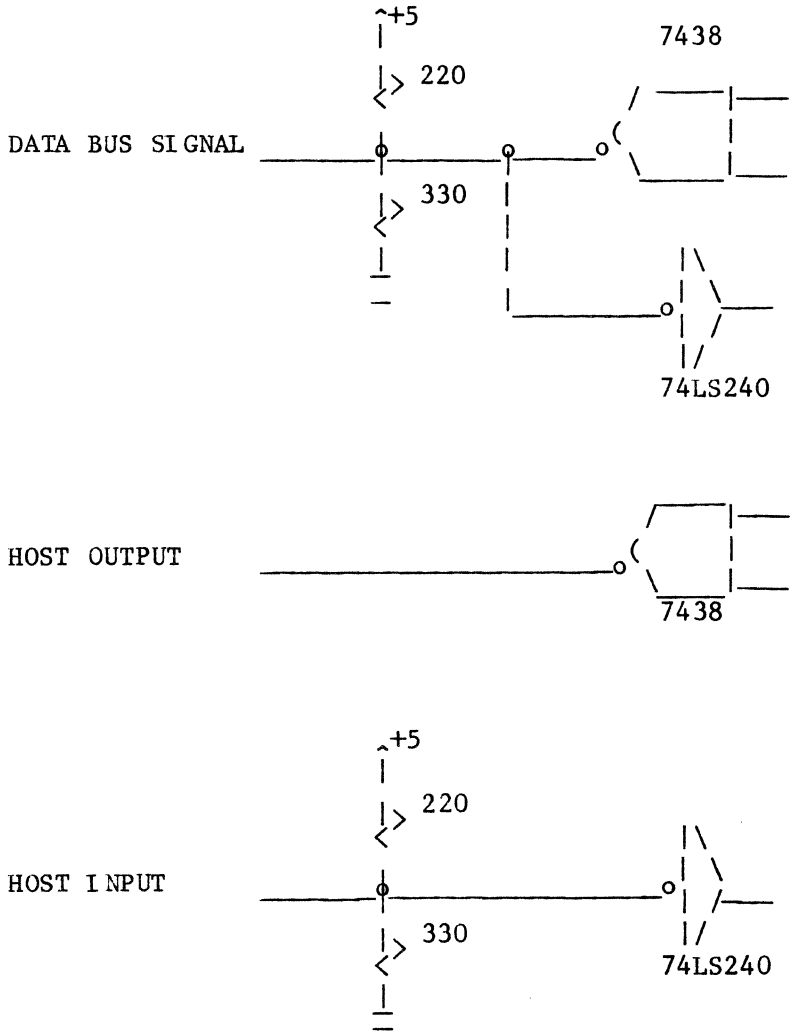


Figure 7. Host Interface Examples

The host to controller cable is to be 50-conductor flat cable. The mating connector is 3M P/N 3425-6020, Berg P/N 65484-023, or equivalent. The maximum cable length is to be 20 feet. The host interface connector is J06. Specifications and pinout are shown in Table 10.

TABLE 10. HOST INTERFACE CONNECTOR, J06

Parameter	Symbol	Conditions	Limits		Units
			Min.	Max.	
High Level Input Voltage	V_{IH}		2.0		V
Low-Level Input Voltage	VIL			0.8	V
Input Clamp Voltage	V_{CL}	I_I=-18mA		-1.5	V
High-Level Input Current	IIH	VCC=4.75V V_{IH}=3.5V		5.75	mA
Low-Level Input Current	IIL	VCC=5.25V V_{IH}=0.4V		-22.2	mA
Low-Level Output Voltage (Open Collector Outputs)	VOL	VCC=4.75V I_{OL}=48mA		0.4	V

Pin No.		Pin No.		Pin No.	
1	Key	18	/Parity	35	Ground Ret
2	/D0	19	Ground Ret	36	/BSY
3	Ground Ret	20	Spare	37	Ground Ret
4	/D1	21	Gnd	38	/ACK
5	Ground Ret	22	Spare	39	Ground Ret
6	/D2	23	Gnd	40	/RST
7	Ground Ret	24	Spare	41	Ground Ret
8	/D3	25	Gnd	42	/MSG
9	Ground Ret	26	Spare	43	Ground Ret
10	/D4	27	Gnd	44	/SEL
11	Ground Ret	28	Spare	45	Ground Ret
12	/D5	29	Gnd	46	/CON
13	Ground Ret	30	Spare	47	Ground Ret
14	/D6	31	Gnd	48	/REQ
15	Ground Ret	32	Spare	49	Ground Ret
16	/D7	33	Gnd	50	/OUT
17	Ground Ret	34	Spare		

E. DRIVE INTERFACE SPECIFICATIONS

Controller to drive interfacing is accommodated by three connectors: J107, J108 and J109. J109 carries all floppy disk drive signals and Winchester access control signals. J107 and J108 carry Winchester data for one or two drives. Pin functions for these connectors are presented in Tables 11 and 12.

TABLE 11. DISK INTERFACE CONNECTOR (J109) ELECTRICAL PARAMETERS

(Limits apply for V_{CC}=5V + 5%, 0 degrees C < T(A) < 50 degrees C unless specified otherwise. Note: Outputs all open collector.)

Parameter	Symbol	Conditions	Limits			Units
			Min.	Typ.	Max.	
Low-Level Output Voltage	VOL	VCC=4.75V I_{OL}=48mA			0.4	V
Low-Level Input Voltage	VIL				0.8	V
Low-Level Input Current	I_{IL}				24	mA

NOTE: Mating connector is 3M P/N 3425-6020, Berg P/N 65484-023, or equivalent.

Pin No.		Pin No.		Pin No.	
1	Ground Ret	17	Ground Ret	34	Direction
2	Low Current/ Read Postcomp	18	*Head Select 1	35	Ground Ret
		19	Ground Ret	36	Step
3	Ground Ret	20	Index	37	Ground Ret
4		21	Ground Ret	38	Write Data
5	Ground Ret	22	Ready	39	Ground Ret
6	Load Head 2	23	Ground Ret	40	Write Gate
7	Ground Ret	24		41	Ground Ret
8	Seek Complete	25	Ground Ret	42	Track 00
9	Ground Ret	26	Drive Select 0	43	Ground Ret
10	Two Sided	27	Ground Ret	44	Write Protect/Unsafe
11	Ground Ret	28	Drive Select 1	45	Ground Ret
12		29	Ground Ret	46	Read Data
13	Ground Ret	30	Drive Select 2	47	Ground Ret
14	Head Select 0	31	Ground Ret	48	
15	Ground Ret	32	Drive Select 3	49	Ground Ret
16	Load Head 3	33	Ground Ret	50	Key

* DC Floppy Drives (SA860, TM848) use Pin 18 as Motor-On.

TABLE 12. DISK DATA CONNECTOR (J107 AND J108) ELECTRICAL PARAMETERS

(Limits apply for V_{CC}=5V + 5%, 0 degrees C $\leq$ T(A) $\leq$ 50 degrees C unless specified otherwise.

Parameter	Symbol	Conditions	Limits			Units
			Min.	Typ.	Max.	
Low-Level Output Voltage	V_{OL}	VCC=4.75V (see note 1)			0.1	V
High-Level Input Voltage	V_{OH}	VCC=4.75V (see note 1)	1.25			V
Differential Input Threshold Voltage	VTH(D)	(see note 2)			0.2	V

NOTES:

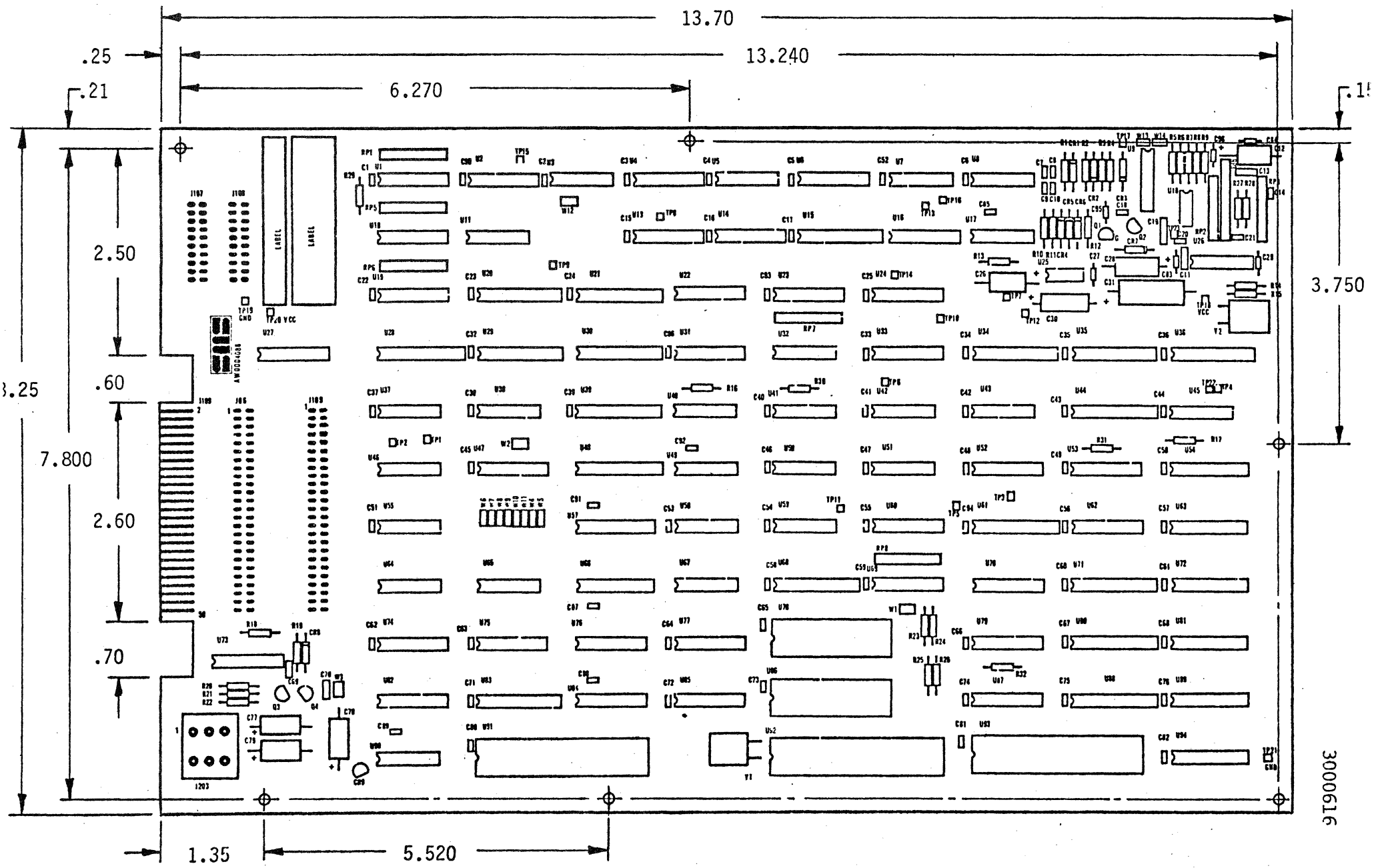
1. Specifications apply when driving a 75107B receiver terminated to ground with 51 ohm as is done on the SA1000 series.

2. Differential receiver is MC3486 or equivalent with dual 51 ohm termination to ground.

3. Mating connector is 3M 3421-6020, Berg 65484-007, or equivalent.

4. J107 is the data connector for drive 0 and J108 is the data connector for drive 1.

Pin No.		Pin No.	
1	Key	11	Gnd
2	Gnd	12	Gnd
3		13	Wdata
4	Gnd	14	/Wdata
5		15	Gnd
6	Gnd	16	Gnd
7		17	Rdata
8	Gnd	18	/Rdata
9	CLK	19	Gnd
10	/CLK	20	Gnd


13.70
.25
13.240
.21
6.270
.15
2.50
3.750
.60
3.25
7.800
2.60
.70
1.35
5.520
3000616

VI. SYSTEM INSTALLATION

The first step in system installation is to apply power to J203 of the FWD5000. No host connection or drive connection should be made. The W4 and W5 straps should be installed. When power is applied the on board LED should flash on and then remain off. If this occurs, the controller hardware is most likely operational.

The second step in installation is to power down the controller and attach the drives. Drives must be optioned according to Table 14. Be sure that the 20-pin data cable from Winchester 0 goes to J107 on the controller (J108 is for Winchester 1). Also, be certain to terminate on the Winchester at the end of the signal cable from J109 on the controller. The controller should be properly optioned for the floppy type and Winchester type according to Table 13. W4 should be in and W5 should be out to select the format and test diagnostic, and diskettes should be installed in the floppy drives. When power is applied to the controller, the LED should flash on and then remain off as the controller begins to format all the drives.

When the format operation is complete, the drive test will begin to run. If after a few minutes of operation, that is random seeks and reads on all drives, the on board LED remains off, the drive and controller subsystem is operational. Note that if the drives have been previously formatted, the normal drive test (W4 out and W5 out) may be run to verify that the drive and controller subsystem is operational. See section I-E for option details and LED interpretation on system test.

Once the drive and controller subsystem is operational, the controller should be powered down and optioned properly for normal operation per Table 1 and Table 13. The cable to the host logic may now be installed at J06. When power is applied the controller should become ready to accept a command from the host.

If any problem occurs in the above procedure, Table 15 should be followed in an attempt to isolate the problem. If, after following the trouble isolation procedure, the problem persists, contact SMS customer service for application support.

TABLE 13. FWD5000 PCB OPTIONS

STRAP NUMBER	MEANING
W2	PARITY ENABLE
	REMOVED - PARITY DISABLED
	* INSTALLED - PARITY ENABLED
W4, W5	POWER ON/RESET DIAGNOSTICS
	W4 W5
	OUT OUT CONTINUOUS DRIVE TEST
	OUT IN NO SELF-TEST AT RESET
	IN OUT FORMAT DRIVE TEST
	* IN IN RUN SELF-TEST AT RESET
W6,W11	FLOPPY TYPE
	W6 W11
	* IN IN SA850
	IN OUT SA800
	OUT IN TM848
	OUT OUT SA860
W7	WRITE PRECOMPENSATION ENABLE FOR DOUBLE SIDED, DOUBLE DENSITY FLOPPY DISKETTES.
	REMOVED - NO PRECOMP
	* INSTALLED - PRECOMP DONE ON TK40 - TK76.
W8, W9, W10	WINCHESTER TYPE
	W8 W9 W10
	* IN IN IN SA1002
	IN IN OUT SA1004
	IN OUT IN Q2010
	IN OUT OUT Q2020
	OUT IN IN Q2080
	OUT IN OUT Q2040
	OUT OUT IN SA1104
	OUT OUT OUT SA1106
W1, W3, W12-W14	ALWAYS REMOVED -- USED FOR TESTING.

* FACTORY CONFIGURATION AT SHIPMENT

TABLE 14. DISK DRIVE OPTIONS

SHUGART 800-2

The Shugart 800-2 must be optioned as follows for the FWD5000:

DRIVE	JUMPER
DRIVE 2	DS3,X,Y,A,T1,T2,800*,HL,J1 Pin 6 to C post
DRIVE 3	DS4,X,Y,A,T1,T2,800*,HL,J1 Pin 16 to C post

*The 800 strap is only applicable to level 4 boards.

In floppy only systems, whichever of the above drives is to be physically (and electrically) the last drive on the cable requires the addition of the following jumpers: T3, T4, T5, T6. The L jumper should be configured properly for the negative voltage power supply used. No other jumpers are to be implemented.

SHUGART 850

The Shugart 850 must be optioned as follows for the FWD5000:

DRIVE	JUMPER
DRIVE 2	A,X,Y,R,I,C POST TO J1/6 AND TO H POST*,S2,2S,DS3,850,HL,IT,RM,IW,M
DRIVE 3	A,X,Y,R,I,C POST TO J1/16 AND TO H POST*,S2,2S,DS4,850,HL,IT,RM,IW,M

*The H post is connected to the IT jumper on the pc board and the C post is connected to the X strap on the pc board. Both the C post and the H post must be connected to J1 pin 6 on drive 2 by the user. Since J1/16 is connected to the D post, C post, D post and H post should be connected on drive 3.

In floppy only systems, a terminator pack should be installed in the last drive on the cable at pcb location 5E. DD, RR, and RI are etched on pc board and are assumed to be connected. Z and B are connected via straps at location 4F on the drive and should be cut. No other jumpers are to be implemented.

SHUGART SA860

DRIVE	JUMPER
DRIVE 2	DS3,TR,S2,SR,Y,2S,MD,SE,MMO
DRIVE 3	DS4,TR,S2,SR,Y,2S,MD,SE,MMO

In floppy only systems, a terminator pack should be installed in the last drive on the cable in location U9. RTR, R, RR, and WP are etched on the pc board and are assumed to be connected. No other jumpers are to be implemented.

TABLE 14. DISK DRIVE OPTIONS (continued)

TANDON TM848

DRIVE	JUMPER
DRIVE 2	DS2,MC2
DRIVE 3	DS4,D

Cut pc board traces M1, M3 and MC1. Connect common M3-M4 pad to trace common to MC1, MC2, MC3, and connect to drive side of 'D' jumper (same as U13-1). Z (U3-1), HL (U3-2), and B (U3-4) are connected via straps at location U3 and should be cut. S2, 2S, RI, WP, and RR are etched on the pc board and are assumed to be connected. No other jumpers are to be implemented.

In floppy only systems, a terminator pack (RP1) should be installed in the last drive on the cable.

SHUGART SA1000 / SA1100

DRIVE	JUMPER
DRIVE 0	DS1
DRIVE 1	DS2

A terminator pack should be installed in the last drive of the chain (C8). Voltage selection strap (-5/-15) is a user option; see SA1000 OEM Manual.

QUANTUM Q2000

DRIVE	JUMPER
DRIVE 0	DS1
DRIVE 1	DS2

A terminator pack should be installed in the last drive (6J). Voltage optioning should be as required by user.

TABLE 15. TROUBLE ISOLATION CHECKLIST

|1.| With no host connection and no drive connection, the LED does not turn off when power is applied:

1. LED blinking? --> Check that W4 and W5 are IN.

2. LED on? --> Check that power is 4.75 to 5.25V.

If W4 and W5 are installed and power is OK, then there is a controller hardware failure.

|2.| With no host connection and with drives installed, the LED does not turn off when power is applied:

1. LED blinking? --> Check drive strapping per Table 14. Check that controller strapping matches drive type per Table 13. Remove and add drives to isolate possible bad unit. Try drive test with and without format (see Table 1) to determine if bad or unformatted media.

2. LED on? --> Remove drive connections from controller, strap for self test (W4 and W5 in) and go to |1.|.

|3.| With host connection present and drives connected, the LED does not turn off when power is applied:

1. LED blinking? --> Check that W5 is IN. Remove host connection and go to |2.|.

2. LED on? --> Check that RST is not being asserted by the host. Check power supply voltage. Remove host connection from controller, install W4 and W5 and go to |1.|.

|4.| With host connection and drive connection, the LED flashes ON and then OFF when power is applied but does not become ready to accept a command:

1. Remove host connector and check that all host interface signals are greater than 2.5V at connector J06. If any signal is less than 2.5V there is a controller problem.

   If all signals are greater than 2.5V there is most likely a short in the host cable or logic which is grounding /BSY, /CON, /OUT or /REQ.