United States Patent

[11] 3,578,912

[72] Inventors **William E. Beavers, Jr.**
Maryland City;
William H. Sturdevant, Bladensburg, Md.

[21] Appl. No. **707,615**
[22] Filed **Feb. 23, 1968**
[45] Patented **May 18, 1971**
[73] Assignee **Singer-General Precision, Inc.**

[54] **SOUND GENERATOR**
9 Claims, 2 Drawing Figs.

[52] **U.S. Cl.** **179/1**
[51] **Int. Cl.** **G10l 1/00**
[50] **Field of Search** ..... 179/1 (AS); 179/15.55; 340/384 (E); 340/172.5

[56] **References Cited**

UNITED STATES PATENTS

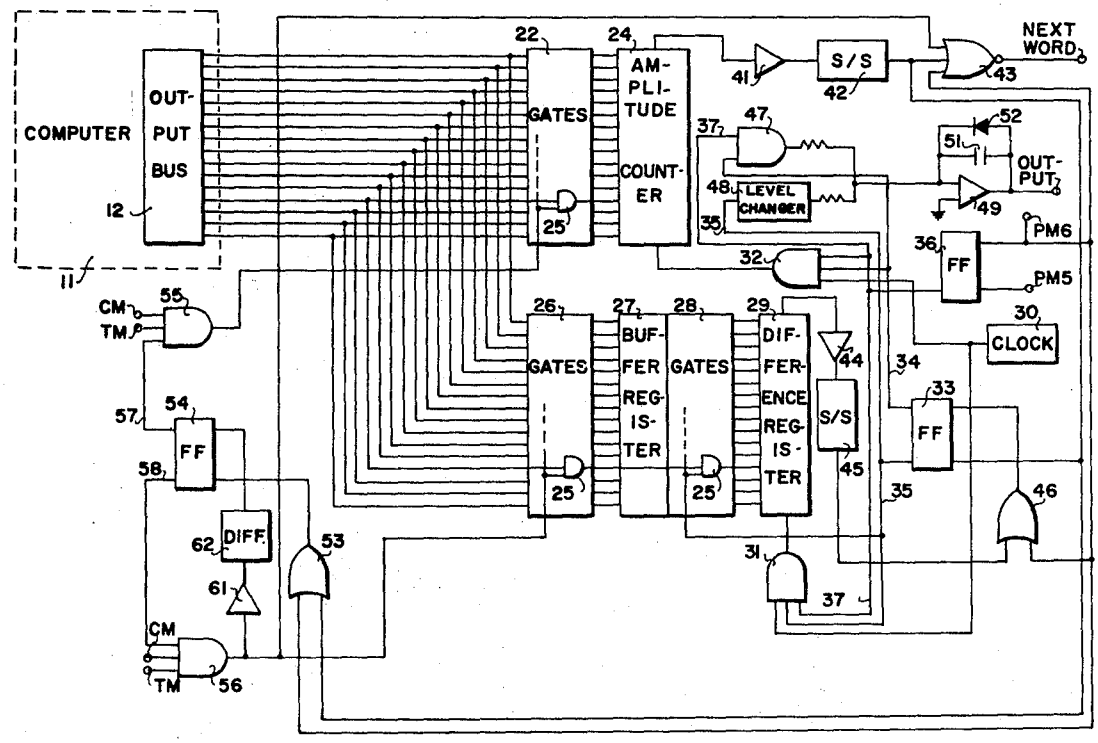
2,974,424	3/1961	Roberts	340/384(E)
3,165,734	1/1965	Grodzinsky et al.	340/384(E)
3,254,336	5/1966	Campbell	340/384(E)
3,388,330	6/1968	Kretzmer	179/15.55

OTHER REFERENCES

IBM Technical Disclosure Bulletin, Senzig, Single Arithmetic Unit Vector Processor, Vol. 8, No. 4, September 1965.

Primary Examiner—Kathleen H. Claffy
Assistant Examiner—Jon Bradford Leaheey
Attorneys—Francis L. Masselle and William Grobman

ABSTRACT: This invention comprises a system for digitally generating desired sounds under the control of a digital computer. The sound generator of this invention can be used to duplicate or synthesize available sounds. To accomplish this, the sound to be duplicated is analyzed to indicate which frequency bands are present in the sound and the relative amplitudes for each band. The actual generation of the sound is by a transducer, such as a loudspeaker, which is fed by the output of a flip-flop. The time duration of a complete cycle of the flip-flop determines the frequency of the signal being generated, and the duty cycle determines the amplitude of that signal. There are many different ways to achieve a duplicate of a known sound. For example, if the sound to be duplicated contains a fundamental frequency and primarily odd harmonics, then the output of the flip-flop, a rectangular wave, can be fed directly to the transducer. Other shaped waves, such as triangular waves, sine waves, etc., can be produced by the use of differentiating circuits, integrating circuits, filters, and the like. In addition, the harmonics can be generated and supplied simultaneously by using duplicate apparatus, or they can be generated in sequence using a single apparatus if they are sufficiently close in time to create the impression of a single, composite sound.



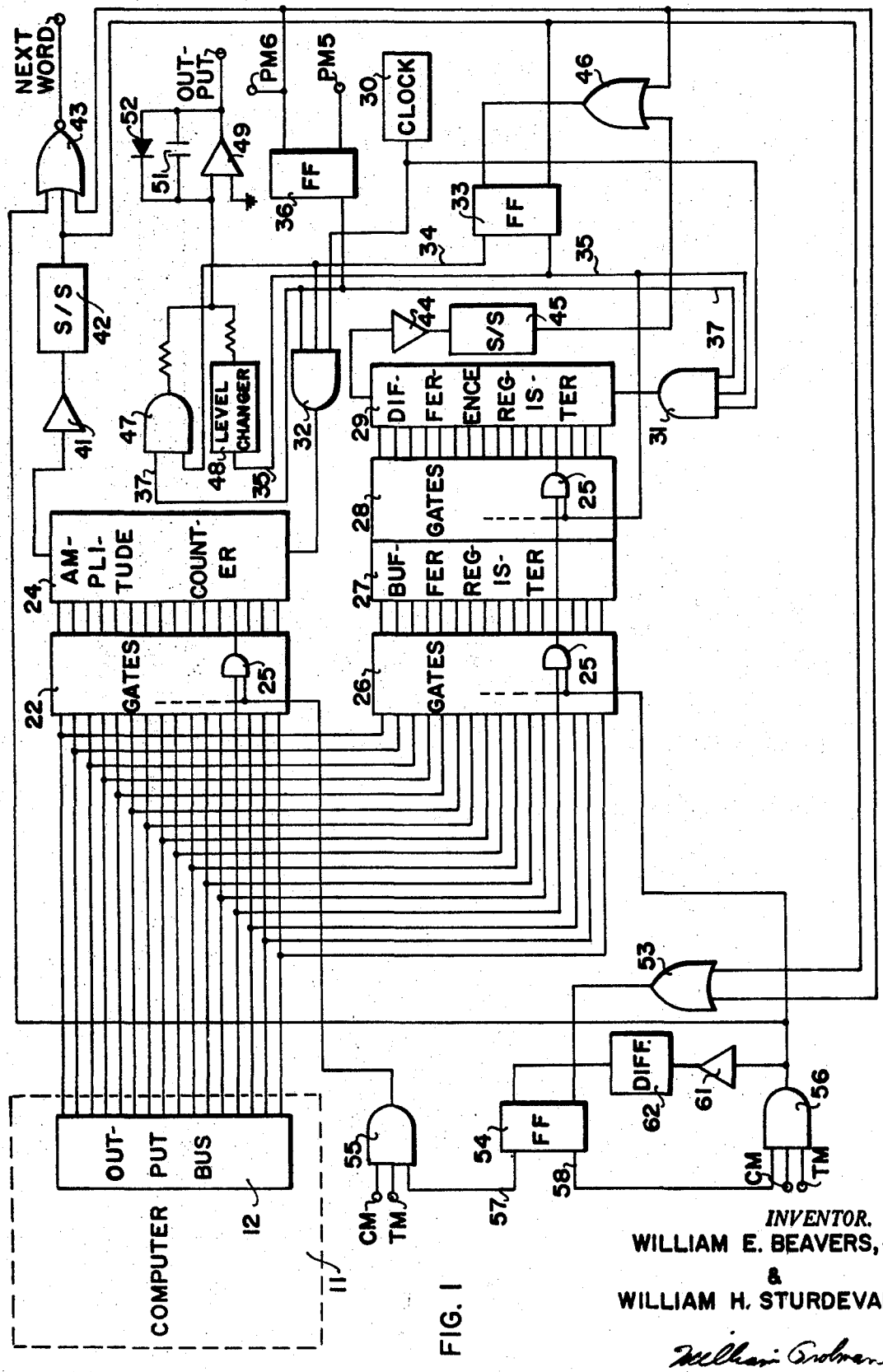


FIG. 1

INVENTOR.
WILLIAM E. BEAVERS, JR.
&
WILLIAM H. STURDEVANT

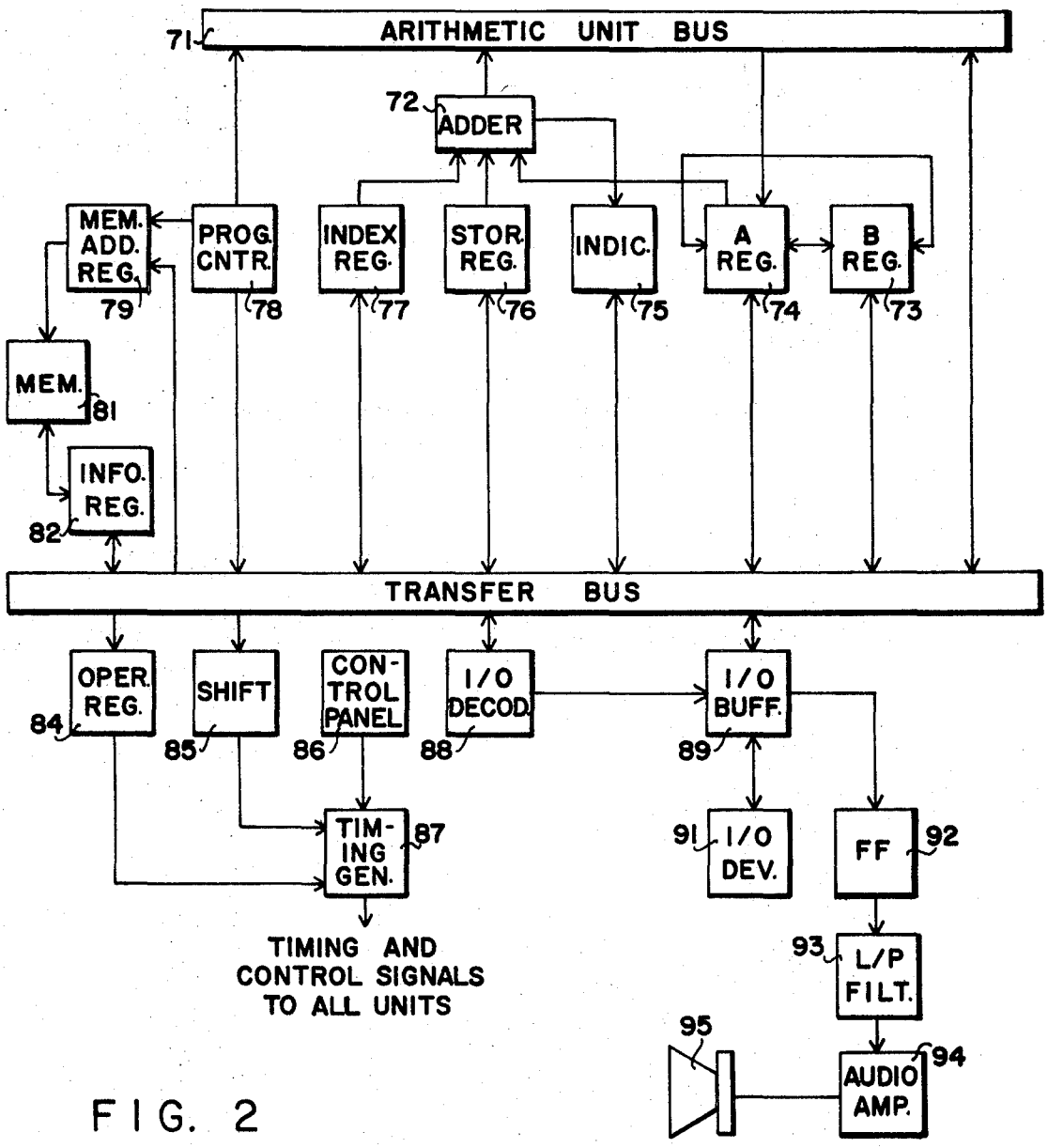


FIG. 2

INVENTOR.
WILLIAM E. BEAVERS, JR.
&
WILLIAM H. STURDEVANT

William Grolman

SOUND GENERATOR

This invention relates to sound generators and, more particularly, to systems for synthesizing selected sounds, for generating noise, and for producing unique sounds.

The sound generation art has application to many broad fields of endeavor. For example, a suitable sound generator can be used for training purposes by simulating sounds found at different times in the performance of a specific job. Sound generators have found use in the medical profession, both physiological and psychological. The problem in the past has been to devise a system which can be used for the generation of a wide range of sounds. In most cases, sound generators each is specialized and are used to generate only a single type of sound.

It is an object of this invention to provide a new and improved sound generation system.

It is another object of this invention to provide a new and improved sound generation system for generating a wide range of sounds.

It is a further object of this invention to provide a new and improved sound generation system for generating a wide range of sounds digitally.

It is still another object of this invention to provide a new and improved sound generating system which produces sounds by using digital words of varying content.

It is still a further object of this invention to provide a new and improved sound generation system in which the characteristics of the sound being generated can be controlled by the digital words which are first generated.

Other objects and advantages of this invention will become more apparent as the following description proceeds, which description should be considered together with the accompanying drawings in which:

FIG. 1 is a logical block diagram of one system according to this invention; and

FIG. 2 is a logical block diagram of a second embodiment of a sound generation system according to this invention.

Referring now to the drawings in detail and more particularly to FIG. 1, the reference character 11 designates a block shown in dashed lines which represents a computer or other suitable control device utilized in this invention. Within the block 11 the output bus is designated as 12. For the particular example of this application it is assumed that the output bus 12 discharges a word which comprises 16 bits, all in parallel. For this reason, the output from the output bus 12 is shown as comprising 16 lines which are applied to a block or a bank of gates 22. The output of the gates 22 are individually applied in parallel to an amplitude counter 24. A single gate 25 is shown in the bank of gates 22 as illustrative. A second bank of gates 26, also containing a sample gate 25, receives the same information in parallel from the output bus 12 and applies it to the input of a buffer register 27. The buffer register 27 includes its own bank of output gates 28 whose outputs are applied in parallel to the inputs of a difference register 29. A clock 30 generates clock pulses which are applied simultaneously to a count gate 31 whose output is applied to the difference register 29 and to a count gate 32 whose output is applied to the amplitude counter 24. A flip-flop 33 diplexes the two counters 24 and 29. The set output from the flip-flop 33 is labeled 34 and is applied simultaneously to one input to the count gate 32 and as one input to a gate 47. The reset output 35 from the flip-flop 33 is simultaneously applied as inputs to the count gate 31 and to the sample gate 25 contained in the bank of gates 28 and to the input of a level changer 48. An inhibit flip-flop 36 has a single reset output 37 which is applied simultaneously as an input to both of the count gates 31 and 32 and also as an input to the gate 47. In this manner, pulses from the clock 30 are applied through the count gates 31 and 32 to the two counters 24 and 29. The zero or full count output from the counter 24 is applied through an inverter 41, which may or may not be necessary depending on the particular circuit components used, to the input of a single-shot or one-shot multivibrator 42. The unstable output from the single-shot 42 is

applied as one input to a NOR gate 43, as the restore input to the flip-flop 33, and as one input to an OR gate 53. Similarly, the zero or full count output from the difference register 29 is applied through an inverter 44 to the input of a single-shot 45 whose unstable output is applied as an input to an OR gate 46. The output from the OR gate 46 is the set input to the flip-flop 33. The output from the gate 47 is combined, through appropriate resistors, with an output from the level changer 48, and the sum is applied as one input to an integrating operational amplifier 49, which has its other input grounded and which includes an integrating circuit comprising a capacitor 51 and a diode 52 in its feedback path. The system output is taken from the output of the operational amplifier 49.

The output of the single-shot 42 is also applied as an input to an OR gate 53, the output of which is the restore input to a flip-flop 54. The restore output of the flip-flop 54 is designated 58, and this is applied as one input to a gate 56, the output from which is applied as another input to the NOR gate 43. The output from the NOR gate 43 is a signal which is applied through appropriate circuitry to the computer 11, or other control device, to indicate when the next word should be transferred from the output bus 12. The output from the gate 56 is also applied through an inverter 61 and a differentiator 62 as the set input to the flip-flop 54. The set output of the flip-flop 54 is designated 57 and is one of the inputs to a gate 55, the output of which is applied to the transfer gates in the block of gates 22. The output from the gate 56 is also applied to the transfer gates in the block of gates 26. Additional inputs to the NOR gate 43, to the inhibit flip-flop 36, to the OR gate 46, to the OR gate 53, to the AND GATE 55, and to the AND gate 56 are derived from the computer 11 in the normal operation of the control device, and will be discussed later in the description of the operation of the system.

In operation, the flip-flop 33 generates the output pulses for the system. One way in which this is accomplished is by utilizing the computer 11 to follow a program which generates binary words representing quantities. The values of the words generated, there are two words for each cycle of operation, determine when the flip-flop 33 is set and when it is restored. The output bus 12 from the computer 11 provides 16 bits on the 16 output lines. These bits are applied simultaneously to the two blocks of gates 22 and 26. During the time that information is available on the output bus 12, the computer 11 generates output pulses. For examples, many computers will generate control marks or pulses under the control of the program and also timing and channel selection marks. The gate 56 has a program control pulse CM and a timing pulse TM applied to it as inputs. When the gate 56 is opened by the simultaneous application of a timing and control mark at a time when the flip-flop 54 is restored, the output of the gate 56 is applied to the gate 25 in the block of gates 26, opening those gates and transferring the word which then exists on the output bus 12 into the buffer register 27. At the same time, this signal, the output from the gate 56, is applied as an input to the NOR gate 43 and passes through to generate the "next word" signal which is applied to the computer 11 requesting that the next word appear at the output bus 12. Meanwhile, the output from the gate 56 is inverted in the inverter 61, and the inverted signal is differentiated by the differentiator 62 to provide a spike. The spike output of the differentiator 62 is applied as a set input signal to the flip-flop 54, placing that flip-flop in the set condition. This occurs one pulse time after the gate 56 opens to emit a pulse, and it removes one of the enabling signals 58 from the input to the gate 56 closing that gate, and applies an enabling signal 57 to the gate 55. Gate 55 then opens and applies a signal to the gates 25 in the block of gates 22, opening those gates and transferring the word then present on the output bus 12 into the amplitude counter 24. A program control pulse CHM6 applied to the set input to the flip-flop 36 places the flip-flop 36 in the set state providing one enabling signal on the two gates 31 and 32. The flip-flop 33 was placed in the set condition by the same program control pulse CHM6. This places a second conditioning signal on

the gate 32, permitting the clock 30 to transmit pulses through the gate 32 into the amplitude counter 24. At the same time, the output 34 from the flip-flop 33 is applied to the gate 47, and the output 35 is applied to the level changer 48. The output 35 from the flip-flop 33 is zero which produces a zero signal at the output of the level changer 48. At the same time, the set output from the flip-flop 36 and the set output 34 from the flip-flop 33 are both plus, opening the gate 47. The output of the gate 47 is high which, when applied to the input to the operational amplifier 49, is integrated downwardly by that amplifier. While the amplifier 49 is downwardly integrating its input, the clock 30 is applying clock pulses to the amplitude counter 24 causing that counter to count down to zero. This may be done in either of two ways. Either the counter 24 may be a downward-counting counter in which case the desired number of counts initially is inserted, or the number stored initially in the counter 24 is the complement of the desired value and the clock pulses cause the counter 24 to count upwardly in a normal fashion. In either case, the effect is for the counter 24 to count to zero. When the counter has counted to zero, an output pulse is generated therein and supplied through the inverter 41 to the single-shot 42 to set the single-shot 42 to its unstable condition. This transmits a signal through the NOR gate 43 calling for the next word, applies a pulse to the restore input to the flip-flop 33 and applies a signal through the OR gate 53 to restore the flip-flop 54. The computer 11 supplies three signals to the system shown in FIG. 1. In those computers which have a plurality of output channels, a single channel must be selected for the transfer of words from the computer. When this selection is the channel which transfers words to the system of FIG. 1, a channel pulse CM is applied as an input to the gates 55 and 56. Of course, if a computer has only a single output channel, this signal is not present. Also, during the time that the computer is in condition to transfer information out to the system of FIG. 1, a timing mark TM is applied as input to the gates 55 and 56. The channel and timing marks CM and TM are provided by the computer 11 itself. The program control pulses PM6 and PM5, applied to the set and restore inputs of the flip-flop 36, are generated by the program and are the start and stop signals for the equipment. When the program calls for the generation of a sound, the signal PM6 is generated to set flip-flop 36. When the sound generation is to stop, the signal PM5 is generated to restore flip-flop 36 and remove the signal from line 37 to close the count gates 31 and 32. Restoring flip-flop 33 applies a plus signal to the level changer 48, whose output becomes negative, and removes the input 34 to the gate 47. This applies a negative voltage to the operational amplifier 49 which starts integrating upwardly. The restore output 35 of the flip-flop 33 is now applied to the gate 31 to open that gate and also to the gates in the block of gates 28 to transfer the word from the buffer register into the difference register 29. At the same time, the output 34 from the flip-flop 33 is removed from the gate 32 closing that gate. When the flip-flop 54 is placed in its set condition, the output 57 is applied to the input of the gate 55 opening that gate to apply a signal to the gates in the block of gates 22. When the next word appears at the output bus 12, it is transferred through the gates 26 into the buffer register 27 as described above. In the mean time, the clock 30 has been supplying clock pulses through the gate 31 into the difference register 29 causing that register to count down to zero. When that register counts to zero, the zero output signal is applied through the inverter 44 to the single-shot 45 to place the single-shot in its unstable condition. This applies a signal through the OR gate 46 to the set input of the flip-flop 33 to generate the set output signal 34.

Another form of sound generator according to this invention is illustrated in FIG. 2 in which an arithmetic bus is designated 71. An adder 72 has an output connected to the bus 71 and another output connected to the indicators 75. The adder 72 receives inputs from the an A register 74, a storage register 76, and an index register 77. The A register can be connected with a B register 73 to form a double sized register for use in receiving a double length word such as the product formed by multiplication process for example. The A register also receives an input from the arithmetic bus 71. The B register 73, A register 74, indicators 75, storage register 76 and index register 77 all have reciprocal communication links with a data transfer bus 83. In addition, a program counter 78 has one output connected to the arithmetic bus 71 and another output connected to the transfer bus 83 as well as a third output connected to a memory address register 79. Another input to the address register 79 comes from the transfer bus 83. The output of the address register 79 is applied to a memory 81, which is in reciprocal communication with a memory information register 82. The memory information register 82 is also connected by a reciprocal data link with the transfer bus 83. Connected to the output of the transfer bus 83 are an operation register 84 and a shift register 85 both of which feed their outputs to a timing and control generator 87. A manual control panel 86 also applies its outputs to the timing and control generator 87. The outputs from the timing and control generator 87 are applied to all of the control circuits and many of the data circuits.

An input/output decoder 88 transfers information through a data link to and from the transfer bus 83. The output from the I/O decoder 88 is applied to an input of an input/output buffer 89 which also has a reciprocal data link connecting it to the transfer bus 83. In addition, standard input/output devices, shown here as block 91, can be connected on a reciprocal basis with the output bus 89. The output from the input/output buffer 89 is applied to a flip-flop 92 which feeds a low pass filter 93. The output from the filter 93 is applied as an input to an audio amplifier 94 which feeds its output to a sound transducer and to display devices 95.

The control circuits are represented, in this case, by the program counter 78, the address register 79, the memory 81, the memory information register 82, the operation and shift registers 84 and 85, the manual control panel 86 and the timing and control generator 87. The adder 72 is the single arithmetic unit of the device and it supplies its output to the arithmetic bus 71 from which it is applied to the A register 74. Although not shown in order to keep the drawings as simple as possible, appropriate control circuits can connect the A register 74 and the B register 73 in tandem to store information in a double sized register. The B register 73, under these conditions, would then receive its information from the A register 74. The indicators 75 are merely indicative of any sort of lights or other display devices which may be incorporated into the computer and which are often used to display the contents of any register. The storage register 76 can be considered as a buffer register to store information from the transfer bus 83 until it is time for that information to take part in a computation performed by the adder 72. The index quantity which is fed through the index register 77 can be inserted from external equipment, can be manually inserted by the operator himself, or can be part of a program itself. Thus, assuming that multiplication is a subroutine which is often utilized and which is separately programmed, the multiplication instruction can contain the index quantity which, when added to the contents of the program counter 78, will produce the address of the first instruction in the multiplication routine. The contents of the program counter 78 are decoded and applied to the memory address register 79 to open the appropriate gates at the appropriate time in the memory 81. The information being taken from the memory 81 or supplied to it passes through the memory information register 82. This register is also in the nature of a buffer register. The transfer bus 83, as is common in most digital computers, is a large, two-way highway along which flows information both into and out of the various components forming the computer itself.

The transfer bus 83 transfers not only data among the various data components in the system, but it also transfers instructions from the memory to the operation register 84. The operation register 84 decodes the particular instruction required and applies the appropriate signals to the timing and

control generator 87. The outputs of the timing and control generator 87 are then applied to the individual circuits in the computer to open those gates which must be opened, to close those gates which must be closed, and to cause the appropriate transfer of information when necessary. In addition to inputs from the operation register 84, the timing and control generator 87 also receives inputs from the shift register 85. The shift register 85 receives shift words which have been recovered from memory and are part of a shift instruction. These instructions are decoded in the operation register 84, and the output signals are applied to the timing and control generator 87. The resulting control signal outputs from the generator 87 are applied to the appropriate portions of the computer; for example, to the A and B registers to provide the mechanism for actually shifting the desired quantities by the desired amount. Also, a manual control panel 86 provides an operator with means for inserting into the timing and control generator 87 specific individual instructions to accomplish a desired result and for testing the system.

Data outputs from the transfer bus 83 are applied to the input/output decoder 88 which decodes the information and applies it to the input/output buffer 89. The buffer 89 feeds two different systems. Standard input/output devices shown as a single block 91 are fed from the buffer 89. These devices would include high-speed printers, typewriters, tape or card punches, and similar devices. The input/output devices are used together with the input/output buffer 89, deriving its information directly from the transfer bus 83 when a program is to be printed out or when the contents of the memory 81 are to be dumped into a punched tape. Although these operations are not necessary to the particular invention described herein, their operation does render the overall system more feasible. The decoded output from the decoder 88 applied through the buffer 89 controls the setting of a flip-flop 92. Thus, one output from the buffer 89 will place the flip-flop 92 in its set condition, and a subsequent output of the buffer 89 will place the flip-flop 92 into its restored state. The time required for a complete cycle, from the setting of the flip-flop 92 through the restoring of the flip-flop 92 and back to the point where the flip-flop 92 is again set, determines the frequency of the sound being generated by the system. The duty cycle of the flip-flop 92, or that portion of the overall cycle during which the flip-flop is set, determines the amplitude of the sound output. A low-pass filter 93 can be used in those cases where the harmonics of the flip-flop output are considered deleterious and are to be eliminated. Normally, the output of a flip-flop is a rectangular wave, and rectangular waves contain odd harmonics. The filter 93 could, in effect, transform the rectangular wave output from the flip-flop 92 into a sine wave having the same fundamental frequency. The output of the filter 94 is applied to a transducer for converting the electrical energy into sound energy or compressional waves through an amplifier 94.

In this embodiment of the invention, the characteristics of the sound are determined by the setting and restoring of the flip-flop 92. In this case, there is no external clock which provides the timing for determining how long the flip-flop 92 will remain in either of its stable states. The computer itself counts a prescribed number of cycles of its own internal operation for controlling the change in state of the flip-flop 92. Thus, taking into consideration the length of time that a computer cycle comprises, the flip-flop 92 can be set by an output from the buffer 89. The computer then counts through a prescribed number of cycles which will equal the time that it is desired the flip-flop 92 stay in its set state. When the proper number of cycles have been counted, another control pulse is applied through the buffer 89 to the flip-flop 92 to place the flip-flop back into its restored state. A second number of cycles is counted to determine the time elapsing before the flip-flop 92 is again set. The system can operate by supplying to the A register 74 a digital word which represents the number of cycles to be counted. Each time the computer goes through a complete cycle, the quantity in the A register is reduced by one. When the quantity in the A register 74 reaches zero, an end-of-operation signal, or a zero signal from the A register 74, is generated and is applied through the transfer bus 83 and the buffer 89 to the flip-flop 92 to change the state of that flip-flop.

It must be borne in mind that the output of the flip-flop 92 generates sound in the same manner as described above in connection with the description of FIG. 1 for the flip-flop 33. Thus, when a familiar sound is to be simulated, it is analyzed to determine the number of narrow pass-bands of frequencies which are present in that sound and the relative amplitude of each of these pass bands. Each pass band is then simulated by reproducing —by means of the flip-flop 92 —the central frequency of that pass band together with an output which has an amplitude comparable to the average amplitude of that pass band. When a single sound comprises a number of separate pass bands together, a plurality of flip-flops 92 can be provided to simultaneously generate each of the signals which are then combined to form the composite sound, or a single flip-flop 92 can be operated on a multiplexing type of operation whereby each pass band is represented by a subsequently generated cycle all of which cycles are then combined by the ear to give the impression of a single composite sound.

It should be borne in mind that in this invention, a single electrical circuit, (in the examples given a flip-flop) is caused to modify its conductive state under the control of an automatic system. In the examples of FIGS. 1 and 2, that automatic system is a computer, but any readily controlled device can be used. A digital computer is useful for the purpose because a plurality of numbers can be automatically supplied at a high rate to generate a series of sounds in rapid succession and in a desired order. The system of FIG. 1 utilizes an integrating operational amplifier 49 on the output of the flip-flop 33 to convert the rectangular output from the flip-flop into a triangular wave. Similarly, the system of FIG. 2 uses a filter 93 connected to the output of the flip-flop 92 to produce a sine wave output. A plurality of similar devices for modifying the harmonic content of the output waves can be provided, each with its own switching means which are all under the control of the control device, to provide a wide variety of output waveforms. This increases the versatility of the system and renders the use of the computer as the control device more feasible. Or, the basic invention can use a simple control means for generating a single sound. In any case, it is realized that the above specification may indicate to others in the art additional forms that this invention may take without departing from its principles. It is, therefore, intended that this invention be limited only by the scope of the appended claims.

We claim:

1. A system for generating a variety of signals whose waveforms substantially duplicate those of selected sounds, said system comprising a device having more than one stable state, control equipment for controlling the state of said device, said control equipment comprising means for cycling said device through its range of operative states and for separately determining the duration of each cycle, said cycling means including means for separately controlling the portion of each cycle that the device remains in each of its operative states, the time duration of the entire cycle determining the frequency of the generated signal and the relative proportion of each cycle assigned to each state determining the amplitude of the generated signal.

2. The system defined in claim 1 wherein said device comprises an electrical switching means, and wherein said cycling means comprises an automatic selectively settable means.

3. The system defined in claim 2 wherein said electrical switching means comprises a bistable trigger apparatus and wherein said settable means includes means for generating output pulses, and means for applying said output pulses to an input of said bistable means.

4. The system defined in claim 3 further comprising a first counter and a second counter, means for loading said first counter with a first number, means for loading said second

counter with a second number, a clock for generating clock pulses, means for supplying clock pulses from said clock to said first counter, said first counter generating a first output pulse when a first prescribed count is reached, and means for applying said first output pulse to said trigger apparatus to place said trigger apparatus in a first operative condition.

5. The system defined in claim 4 further including means responsive to said first output pulse for applying said clock pulses to said second counter, said second counter generating a second output pulse when a second prescribed count is reached, and means for applying said second output pulse to said trigger apparatus to place said trigger apparatus in a second operative condition.

6. The system defined in claim 5 further including switching means having at least two operative conditions, means for applying said first output pulse to said switching means to place it in its first operative condition, means for applying said second output pulse to said switching means in its second operative condition, means for connecting said clock to said switching means, and means for connecting said switching means to said first and second counters whereby the output from one counter causes clock pulses to be supplied to the other counter.

7. The system defined in claim 4 wherein said means for loading said first and second counters comprises a general purpose digital computer.

8. The system defined in claim 5 wherein said means for loading said first and second counters comprises a general purpose digital computer.

9. A system for generating a variety of signals whose waveforms substantially duplicate waveforms of selected sounds, said system comprising a device having at least two conditions of operation, and a programming means for cycling said devices through all of its conditions separately and in sequence and for separately controlling the relative times that said device remains in each of its operative conditions, the length of time of a complete cycle of its operative conditions determine the frequency content and the relative portions of the cycle time that said device remains in each of its operative conditions determining the total energy content of the resulting waveform.