

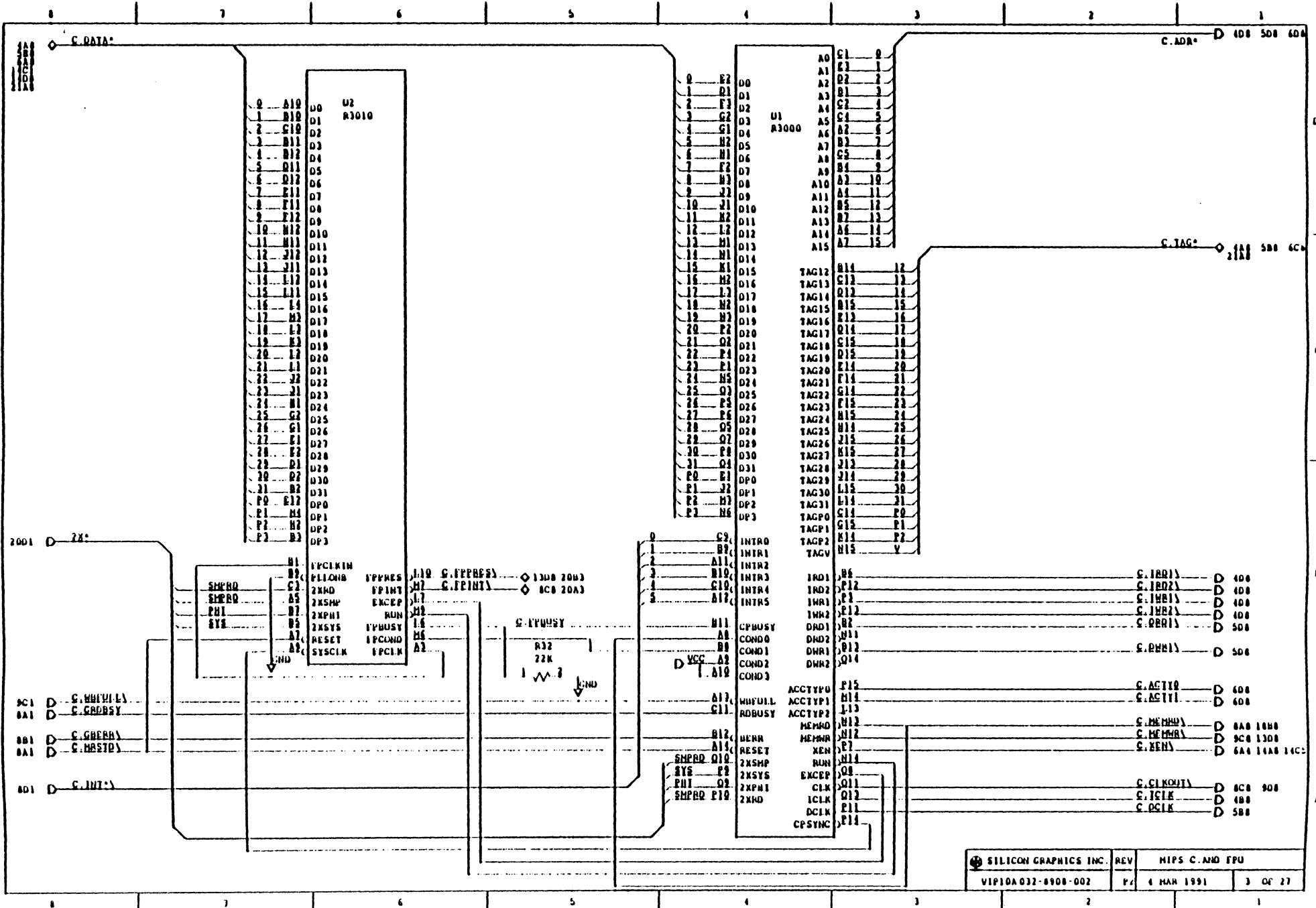
REVISIONS			
ZONE	REV	DESCRIPTION	DATE

APPLICATIONS		SILICON GRAPHICS INC.			
		drw			
		chk			
		iss.			
030-8029	-----				
NEXT ASSEMBLY	USED ON	APPROVALS	DATE	NON.	DRAWING NUMBER
				VIP10	032-8908-002
				REV	DATE
				F2	4 MAR 1991
					SHEET
					1 OF 27

VIP10_CPU

PAGE 1 DESCRIPTION

03 CPU AND FPU
04 INSTRUCTION CACHE
05 DATA CACHE
06 CPU ADDRESS AND PERIPHERAL DATA BUFFERS
07 BOOT PROM, LED REGISTER, ADDRESS DECODE
08 CPU INTERRUPTS
09 CPU BUFFER ENABLES
10 DUART0: KEYBOARD AND MOUSE
11 DUART1: PORTS 1 AND 2
12 TIMER AND RTC
13 CTLL GATE ARRAY
14 MEMORY DATA BUFFERS AND PARITY LATCH
15 INTERRUPT CONTROLLER
16 GRAPHICS I/F AND VME LOCATION MONITOR
17 VME CONTROLS, IACK AND SYSCLOCK
18 VME BUS ARBITER
19 CONSOLE
20 CPU CLOCKS, PUPS & PUDS
21 PUP & PUDS
22 I/O CONNECTORS
23 CPU to I/O BOARD CONNECTOR
24 CPU to MEMORY BOARD CONNECTOR
25 VME P1A, B, C AND P2B CONNECTORS
26 VME P2A, C CONNECTOR
27 BYPASS CAPACITORS



C.DATA

C.TAG D 408 508 608

- U2 R3010
- 0 A19 D0
 - 1 B18 D1
 - 2 C18 D2
 - 3 D11 D3
 - 4 B12 D4
 - 5 D11 D5
 - 6 D12 D6
 - 7 E11 D7
 - 8 F11 D8
 - 9 F12 D9
 - 10 H12 D10
 - 11 H11 D11
 - 12 J12 D12
 - 13 J11 D13
 - 14 L12 D14
 - 15 L11 D15
 - 16 L14 D16
 - 17 H12 D17
 - 18 L13 D18
 - 19 H12 D19
 - 20 L12 D20
 - 21 L11 D21
 - 22 J12 D22
 - 23 J11 D23
 - 24 H11 D24
 - 25 G12 D25
 - 26 G11 D26
 - 27 E11 D27
 - 28 E12 D28
 - 29 D11 D29
 - 30 D12 D30
 - 31 B12 D31
 - DP0 E12 DP0
 - DP1 H11 DP1
 - DP2 H12 DP2
 - DP3 B13 DP3

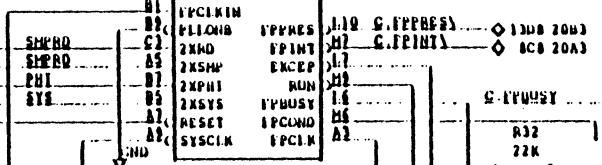
- U1 A3000
- 0 E2 D0
 - 1 D1 D1
 - 2 F3 D2
 - 3 G2 D3
 - 4 G1 D4
 - 5 H2 D5
 - 6 H1 D6
 - 7 F2 D7
 - 8 H3 D8
 - 9 J1 D9
 - 10 H2 D10
 - 11 H2 D11
 - 12 L2 D12
 - 13 H1 D13
 - 14 H1 D14
 - 15 H1 D15
 - 16 H2 D16
 - 17 L2 D17
 - 18 H2 D18
 - 19 H2 D19
 - 20 F2 D20
 - 21 G2 D21
 - 22 F4 D22
 - 23 E1 D23
 - 24 H5 D24
 - 25 G7 D25
 - 26 F2 D26
 - 27 F6 D27
 - 28 G5 D28
 - 29 G7 D29
 - 30 F4 D30
 - 31 G4 D31
 - DP0 E1 DP0
 - DP1 J2 DP1
 - DP2 H7 DP2
 - DP3 H6 DP3

- A0 C1 0
- A1 E1 1
- A2 D2 2
- A3 B1 3
- A4 G2 4
- A5 C4 5
- A6 B2 6
- A7 B2 7
- A8 C2 8
- A9 B4 9
- A10 B2 10
- A11 A1 11
- A12 B5 12
- A13 B2 13
- A14 A6 14
- A15 A7 15
- TAG12 B14 12
- TAG13 C13 13
- TAG14 D12 14
- TAG15 B12 15
- TAG16 E12 16
- TAG17 Q14 17
- TAG18 C15 18
- TAG19 D12 19
- TAG20 E14 20
- TAG21 F11 21
- TAG22 G14 22
- TAG23 F12 23
- TAG24 H15 24
- TAG25 H14 25
- TAG26 J15 26
- TAG27 K15 27
- TAG28 J12 28
- TAG29 J14 29
- TAG30 L12 30
- TAG31 E14 31
- TAGP0 G14 P0
- TAGP1 G15 P1
- TAGP2 K14 P2
- TAGV H15 V

C.TAG D 408 508 608

2001 D 2X

- SC1 D C.MH1(L)
- SA1 D C.GDBSY
- SB1 D C.GHERY
- SA1 D C.MASTD
- SD1 D C.INTV



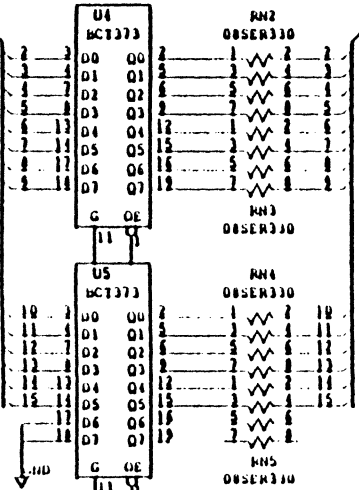
- 0 C2 INTR0
- 1 B2 INTR1
- 2 A11 INTR2
- 3 B10 INTR3
- 4 C10 INTR4
- 5 A12 INTR5
- H11 CPBUSY
- H12 CONDO0
- H13 CONDO1
- H14 CONDO2
- H15 CONDO3
- A17 MHFULL
- G11 RDBUSY
- B12 UERR
- A14 RESET
- SHPRD Q10 2XSHW
- SYS P2 2XSYS
- PNT Q2 2XPNT
- SHPRD P10 2XND

- INTR0 B2
- INTR1 A11
- INTR2 B10
- INTR3 C10
- INTR4 A12
- INTR5
- CPBUSY H11
- CONDO0 H12
- CONDO1 H13
- CONDO2 H14
- CONDO3 H15
- MHFULL A17
- RDBUSY G11
- UERR B12
- RESET A14
- 2XSHW SHPRD Q10
- 2XSYS SYS P2
- 2XPNT PNT Q2
- 2XND SHPRD P10
- ACTYP0 F15
- ACTYP1 H14
- ACTYP2 J13
- MEMRD H12
- MEMWR H12
- XEN E7
- RUN H14
- EXCEP Q8
- CLK Q11
- ICLK Q12
- DCLK E11
- CPSYNC F14
- C.IRR1 D 408
- C.IRR2 D 408
- C.IRR3 D 408
- C.IRR4 D 408
- C.IRR5 D 508
- C.PRR1 D 508
- C.PRR2 D 508
- C.ACT0 D 608
- C.ACT1 D 608
- C.MEMRD D 8A8 1A88
- C.MEMWR D 9C8 1308
- C.XEN D 6A4 1A48 1CC
- C.CLK0 D 8C8 908
- C.ICLK D 488
- C.DCLK D 588

3A1 D C. IADR2
3B1 D C. IADR2

3A1 D C. IADR1
3B1 D C. IADR1

3A1 D C. IADR*

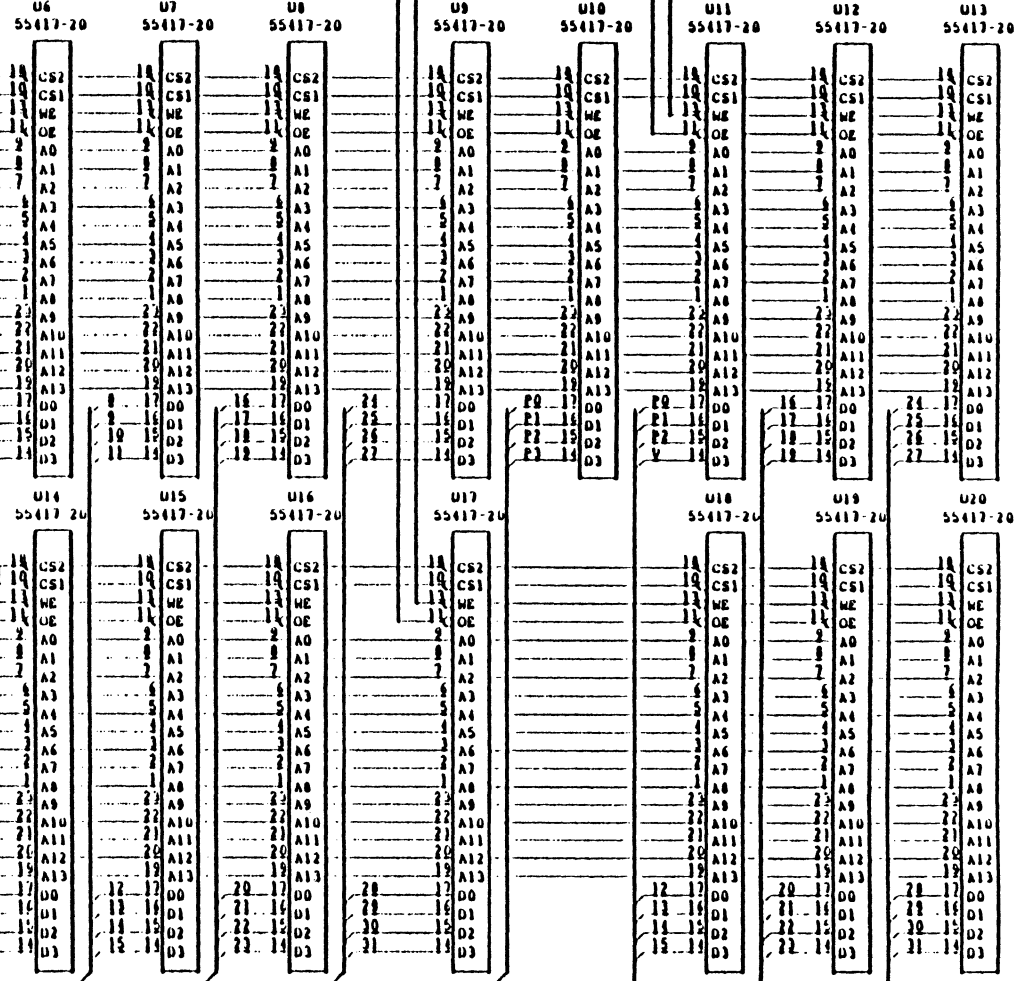


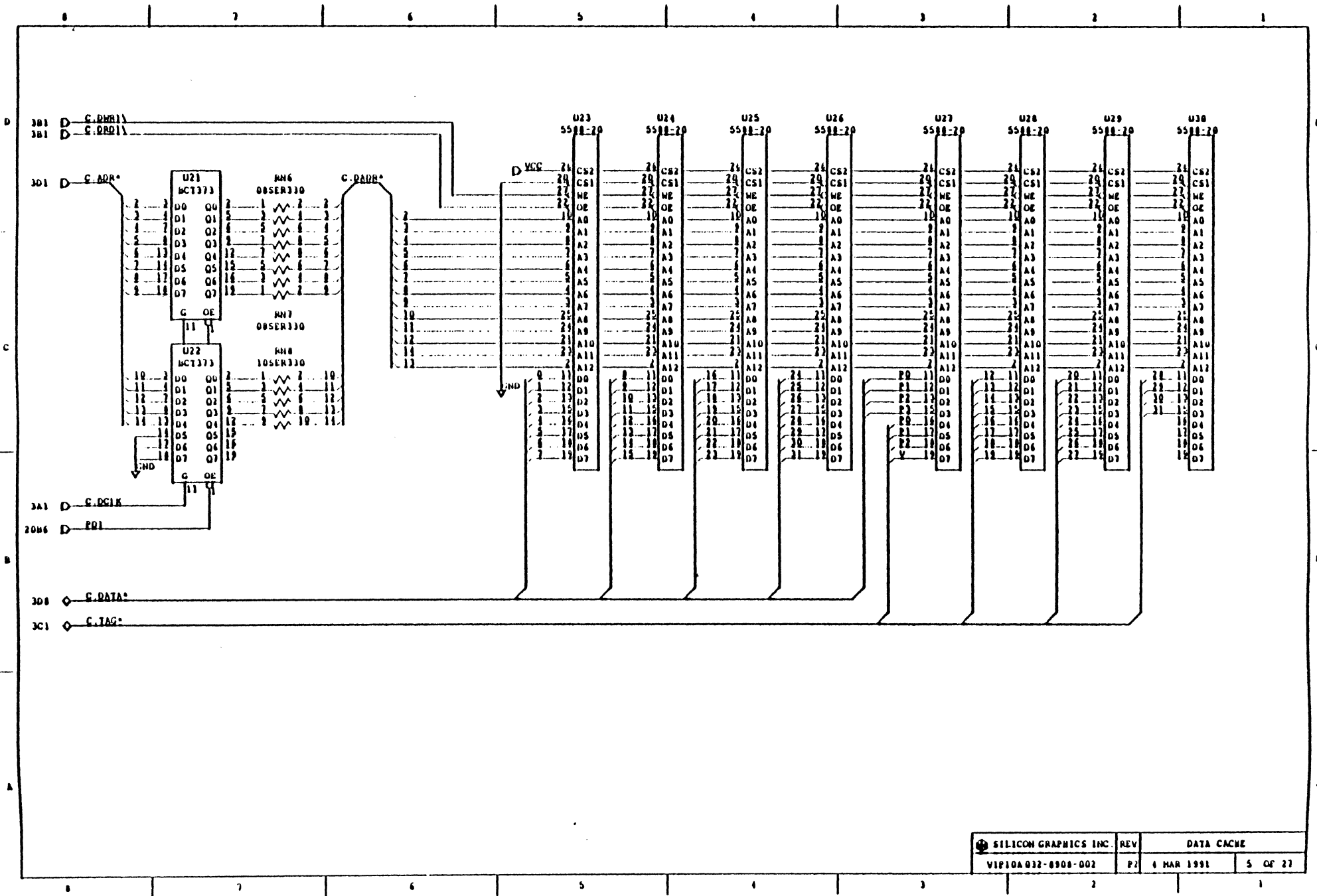
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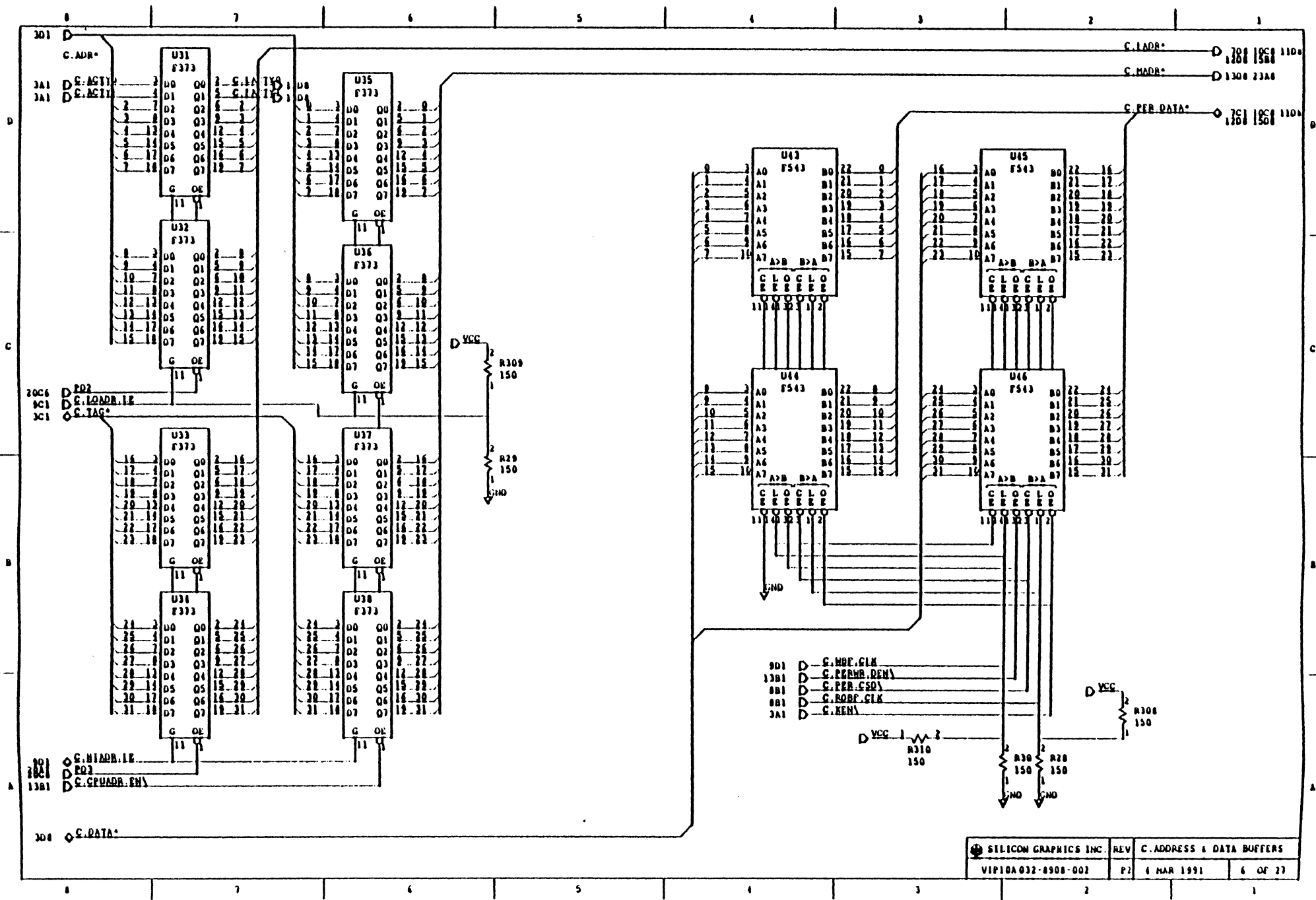
3A1 D C. IADR
20C6 D PDR

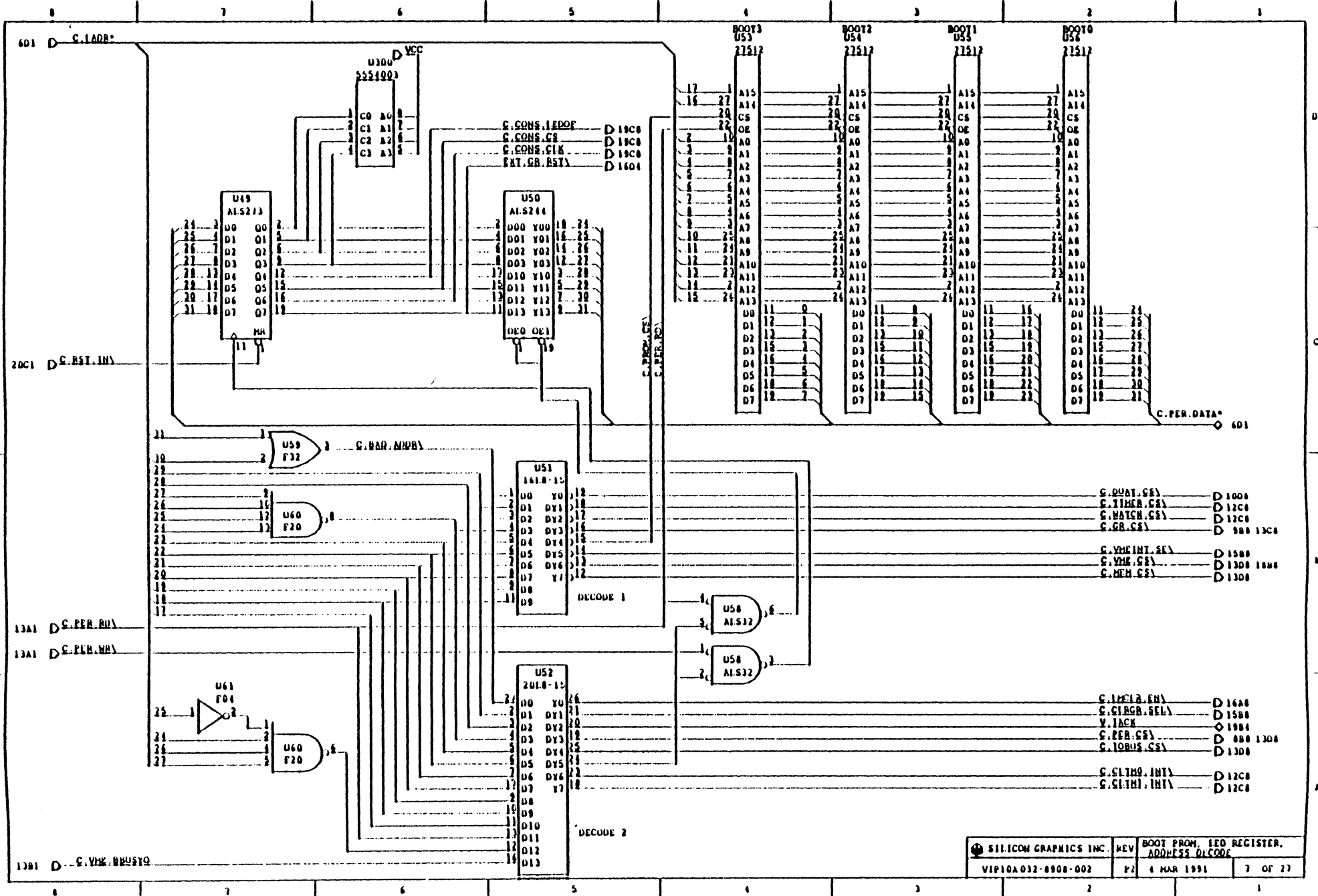
3A0 C. DATA*
3C1 C. TAG*

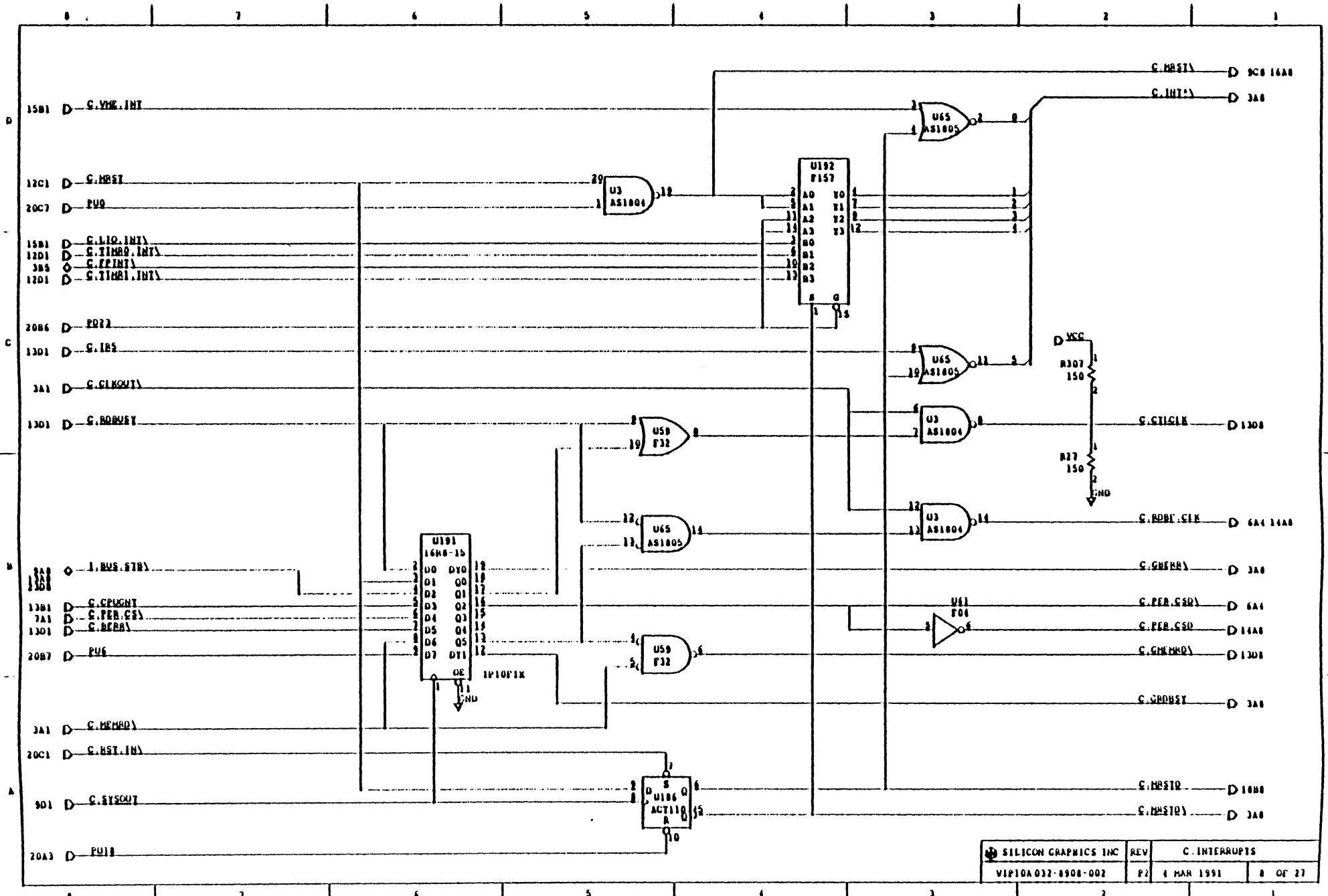
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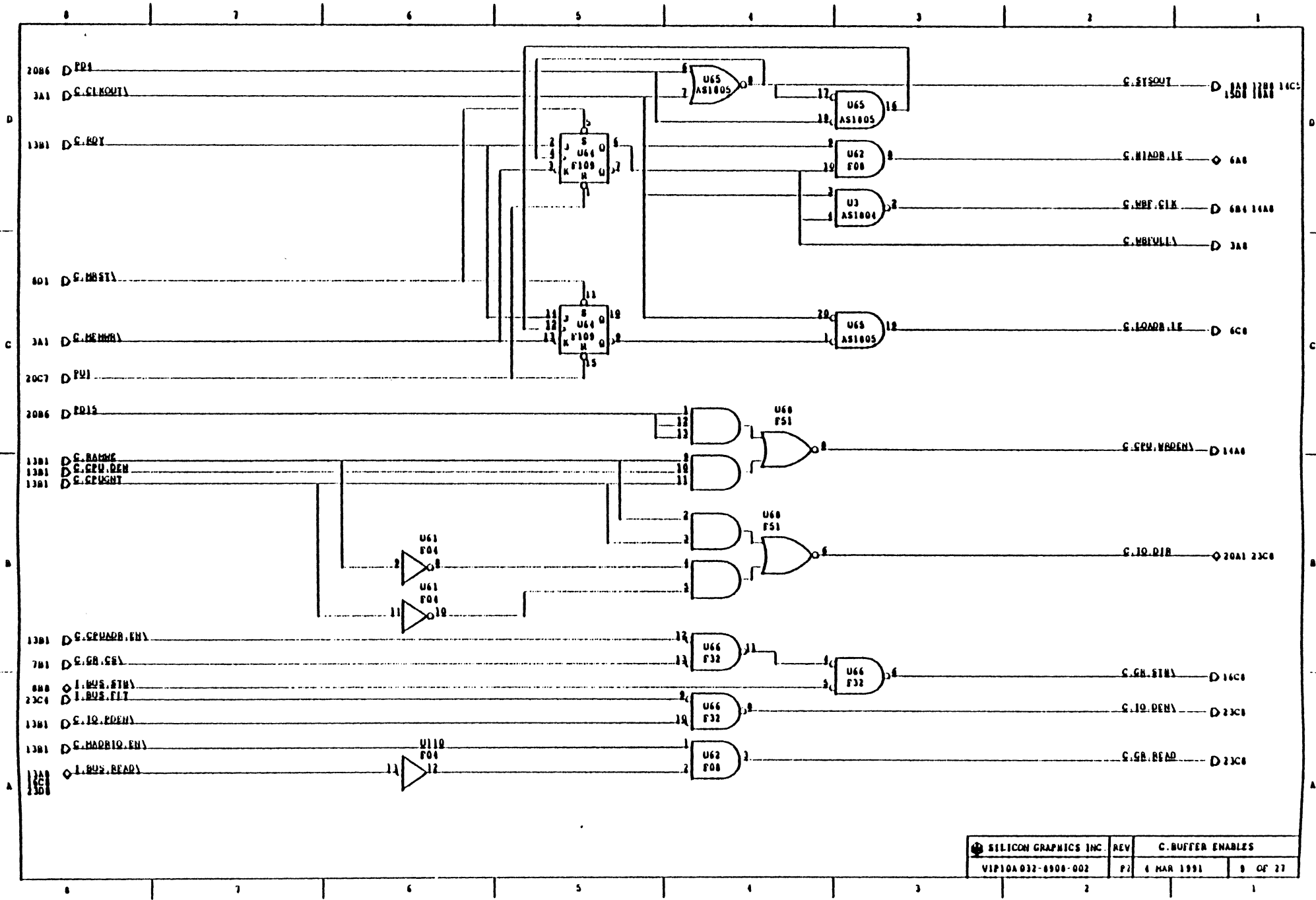


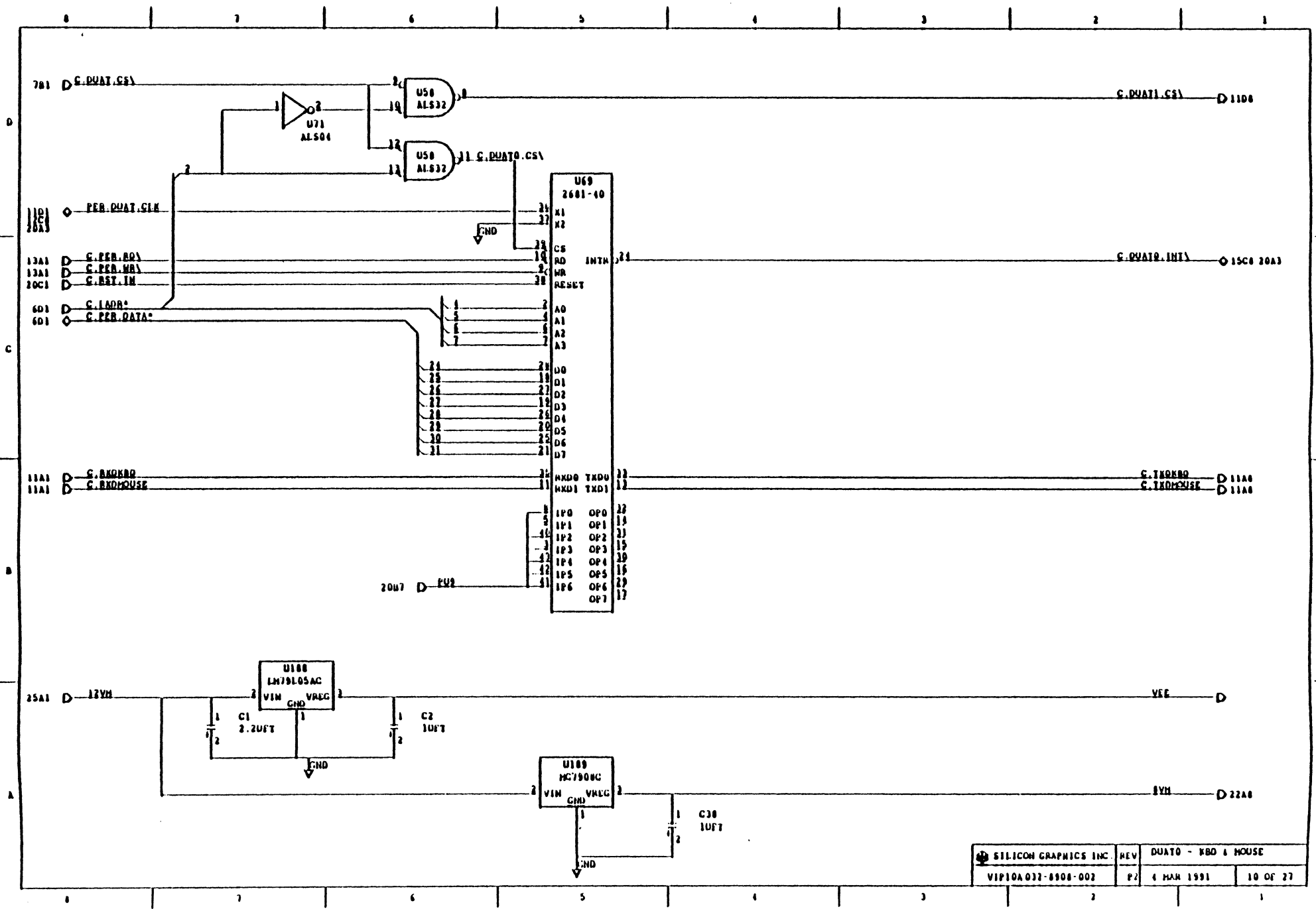


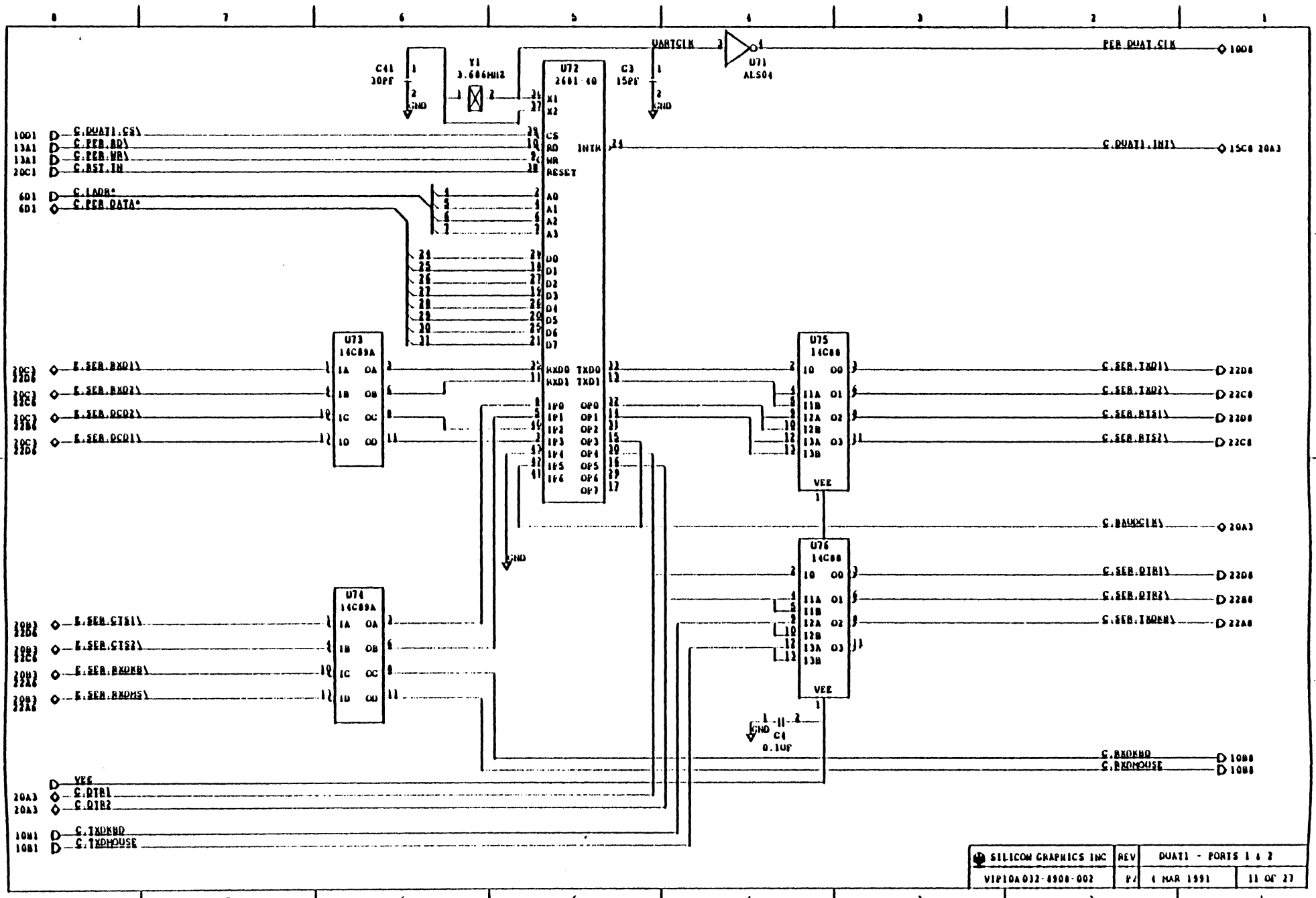


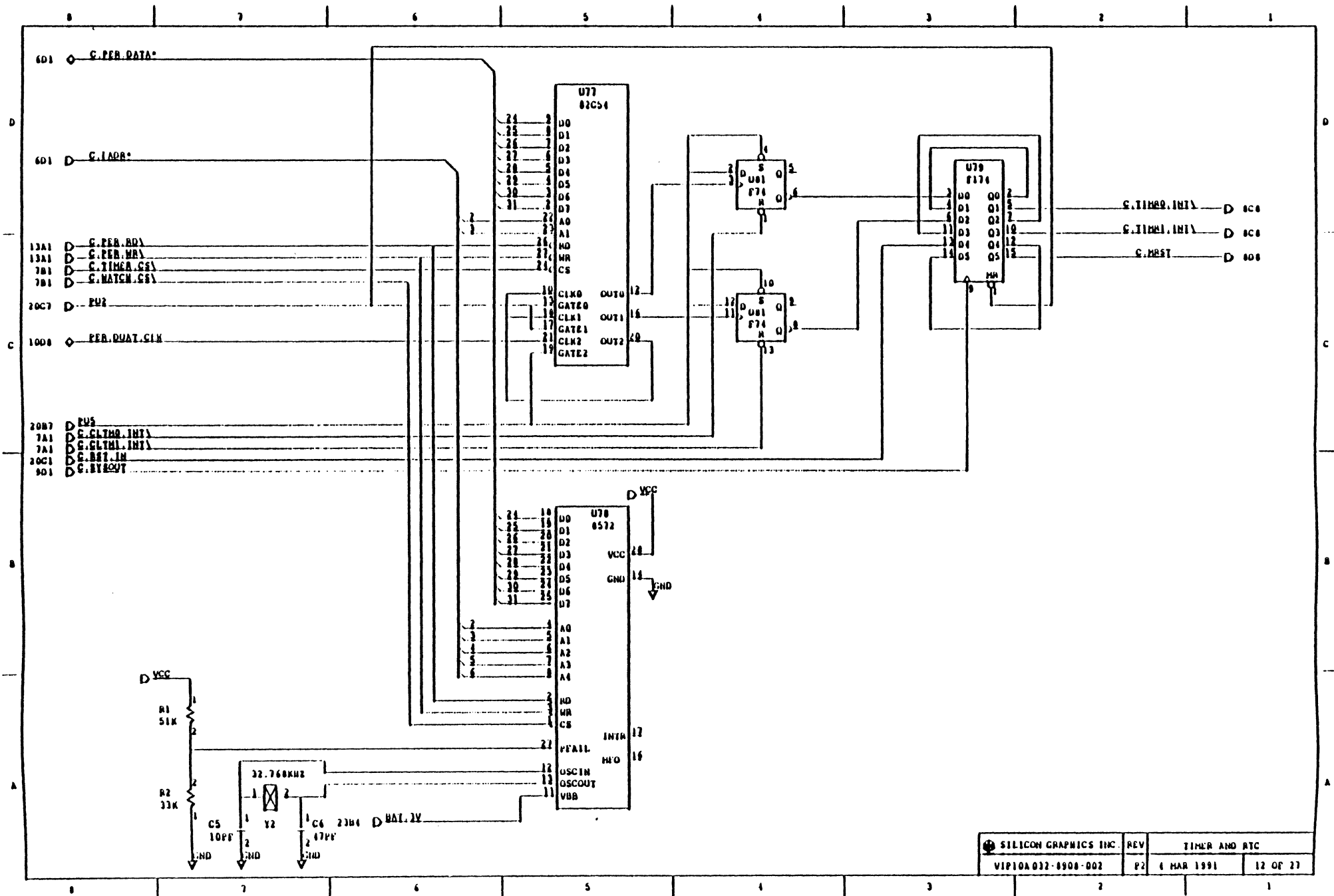


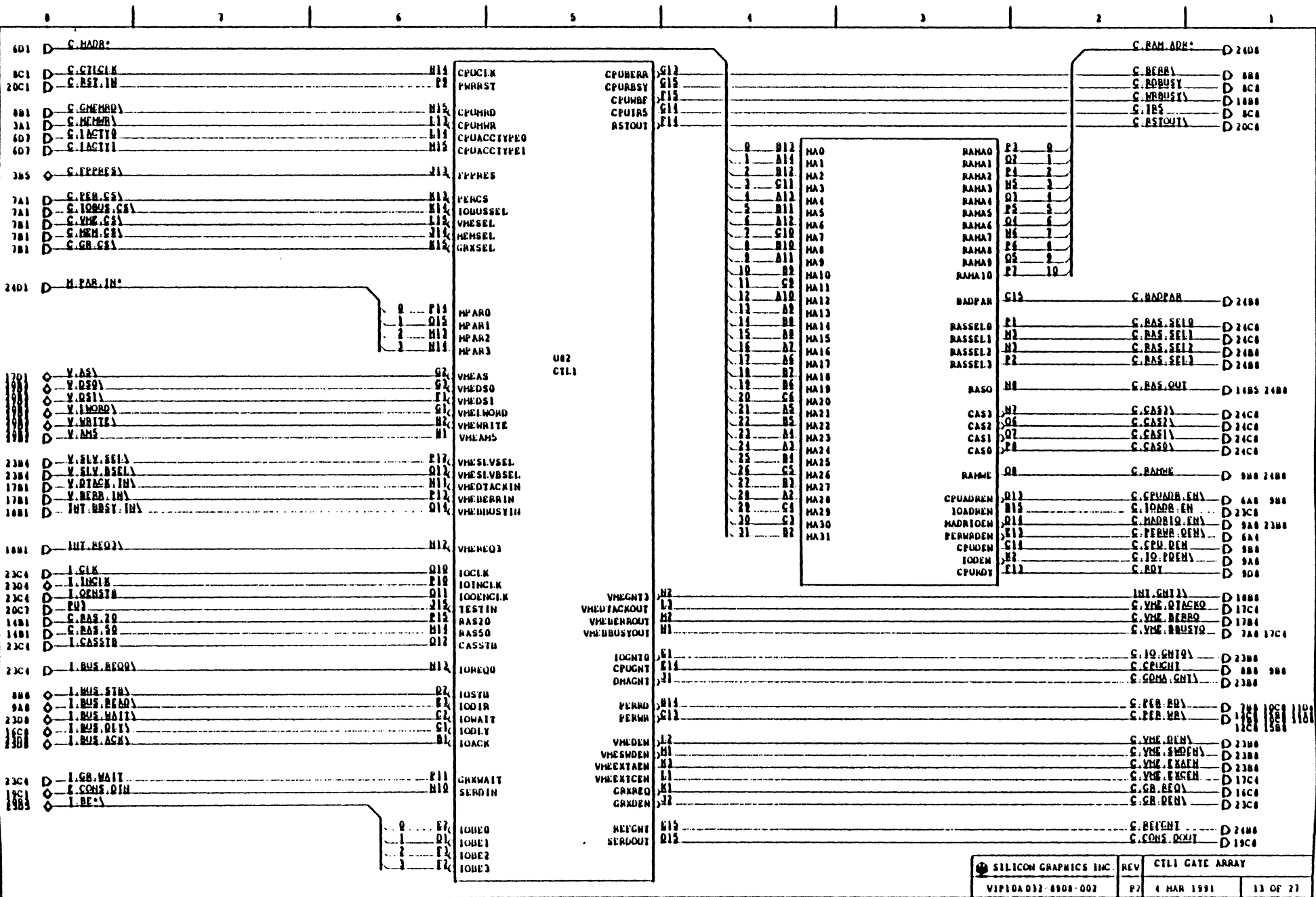










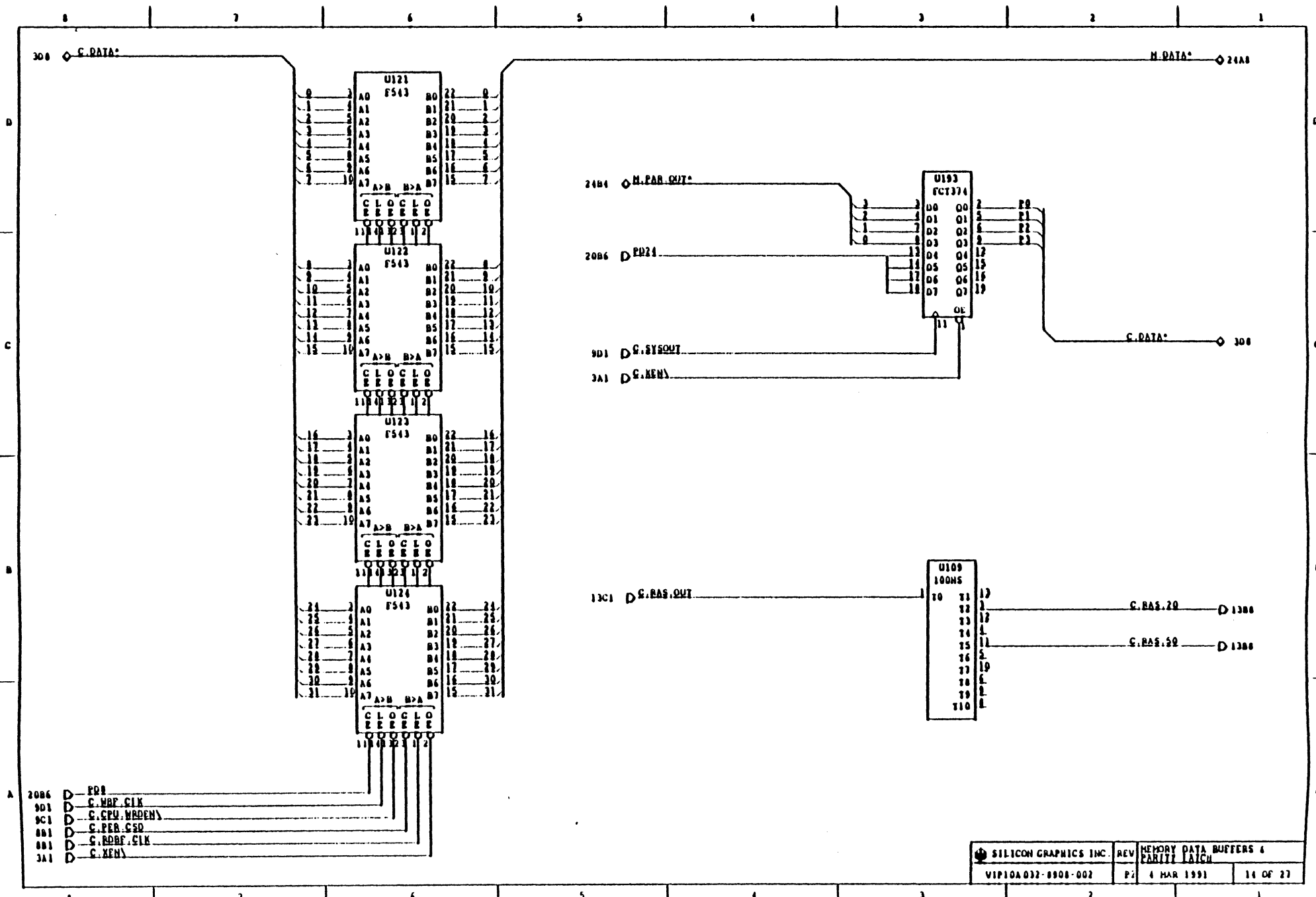


601	D	C.HADR*	
8C1	D	C.STICK	H14
20C1	D	C.RET.IN	P2
801	D	C.GMEMRD	H15
3A1	D	C.MEMRD	L13
6D7	D	C.LACTIO	L14
6D7	D	C.LACTII	H15
305	D	C.FPPRES	J13
7A1	D	C.PEB.CS	H13
7A1	D	C.TORUS.CS	H13
7B1	D	C.VME.CS	L13
7B1	D	C.MEM.CS	J13
7B1	D	C.GR.CS	H13
2401	D	H.PAR.IN*	
		0	P14
		1	O15
		2	H12
		3	H13
17D	D	V.AS	G2
17D	D	V.DS0	G2
17D	D	V.DS1	F1
17D	D	V.WORD	G1
17D	D	V.WRTE	H1
17D	D	V.AMS	H1
2304	D	V.SLV.SEL	F12
2304	D	V.SLV.BSEL	O12
17B1	D	V.DTACK.IN	H11
17B1	D	V.BERR.IN	F12
18B1	D	INT.BBSY.IN	O12
18B1	D	INT.REQ	H12
23C4	D	I.CLK	O10
23C4	D	I.INCLK	F10
23C4	D	I.GENSTA	O11
20C7	D	FU	J15
14B1	D	C.RAS.Z0	F12
14B1	D	C.RAS.Z0	H11
23C4	D	I.CASSTA	O12
23C4	D	I.BUS.REQ	H12
800	D	I.MIS.STA	O2
9A0	D	I.BUS.BERR	F2
23D0	D	I.BUS.WAIT	F1
16C1	D	I.BUS.DIV	G1
23D1	D	I.BUS.ACK	B1
23C4	D	I.GR.WAIT	F11
18C1	D	E.CONS.DIN	H10
19B1	D	I.BE*	
		0	F2
		1	O1
		2	F2
		3	F2

CPUCLK	H14
PMRST	P2
CPUMRD	H15
CPUMHR	L13
CPUACCTYPE0	L14
CPUACCTYPE1	H15
FPPRES	J13
PECS	H13
IONUSSEL	H13
VMESEL	L13
MEMSEL	J13
GRSEL	H13
MPAR0	P14
MPAR1	O15
MPAR2	H12
MPAR3	H13
VMEAS	G2
VMEAS0	G2
VMEAS1	F1
VMEIWORD	G1
VMEWRITE	H1
VMEAMS	H1
VMEVSEL	F12
VMEVBSSEL	O12
VMEDTACKIN	H11
VMEBERRIN	F12
VMEBUSYIN	O12
VMEREQ	H12
IOCLK	O10
IOINCLK	F10
IOENCLK	O11
TESTIN	J15
RASZ0	F12
RASZ0	H11
CASSTA	O12
IOREQ	H12
IOSTB	O2
IODIR	F2
IOWAIT	F1
IODIV	G1
IOACK	B1
GRWAIT	F11
SERDIN	H10
IOREQ0	F2
IOREQ1	O1
IOREQ2	F2
IOREQ3	F2

CPUBERR	G12
CPURBSY	G15
CPUMBF	F13
CPURAS	G14
ASTOUT	F14
MA0	B12
MA1	A14
MA2	B12
MA3	C11
MA4	A12
MA5	B11
MA6	A12
MA7	C10
MA8	B10
MA9	A11
MA10	B2
MA11	C2
MA12	A10
MA13	B2
MA14	B2
MA15	B2
MA16	A7
MA17	A6
MA18	B7
MA19	B6
MA20	C6
MA21	A5
MA22	B5
MA23	A1
MA24	A2
MA25	B1
MA26	C5
MA27	B2
MA28	A2
MA29	C1
MA30	C2
MA31	B2
VMEGNT	H2
VMEUTACKOUT	L2
VMEBERROUT	H2
VMEBUSYOUT	H1
IOGNT0	G1
CPUGNT	F14
DMGNT	J1
PERNR	H11
PERMR	F12
VMEEN	J2
VMEWDEN	H1
VMEXTREN	H2
VMEEXTREN	H2
VMEEXTREN	H1
VMEEXTREN	H1
GRREQ	H1
GRDEN	J2
NEIGNT	H15
SERDOUT	O15

C.RAM.ADR*	D 2408
C.BERR	D 808
C.RBUSY	D 8C8
C.MRBSY	D 1400
C.IRS	D 8C8
C.RSTOUT	D 20C4
RAMA0	F2 0
RAMA1	Q2 1
RAMA2	F4 2
RAMA3	H5 3
RAMA4	Q7 4
RAMA5	F2 5
RAMA6	Q4 6
RAMA7	H6 7
RAMA8	F6 8
RAMA9	Q5 9
RAMA10	F7 10
BADPAR	G15 C.HADPAR D 2408
RASSEL0	F1 C.RAS.SEL0 D 24C8
RASSEL1	H2 C.RAS.SEL1 D 24C8
RASSEL2	H2 C.RAS.SEL2 D 2408
RASSEL3	F2 C.RAS.SEL3 D 2408
RASO	H8 C.RAS.OUT D 14B5 2408
CAS3	H2 C.CAS3 D 24C8
CAS2	Q6 C.CAS2 D 24C8
CAS1	Q7 C.CAS1 D 24C8
CAS0	F8 C.CAS0 D 24C8
RAMME	Q8 C.RAMME D 908 2408
CPUADREN	D12 C.CPUADREN D 6A8 908
LOADREN	H12 C.LOADREN D 23C8
MADRIDEN	D14 C.MADRIDEN D 9A8 2308
PERMADREN	F12 C.PERMADREN D 6A4
CPUDEN	G14 C.CPUDEN D 908
IOOEN	H2 C.IO.OEN D 9A8
CPUKDY	F12 C.RDY D 908
INT.GNT	D 1008
C.VME.DTACKO	D 17C4
C.VME.BERR0	D 17B4
C.VME.BBUSY0	D 7A8 17C4
C.IO.GNT0	D 2308
C.CPUGNT	D 808 908
C.GDMA.GNT	D 2308
C.PEB.BD	D 708 10E1 1101
C.PEB.MR	D 14E1 15E1 1101
C.VME.DIV	D 2308
C.VME.WDEN	D 2308
C.VME.KACK	D 2308
C.VME.FXSEN	D 17C4
C.GR.REQ	D 16C8
C.GR.DEN	D 23C8
C.BEIGNT	D 2408
C.CONS.ROUT	D 19C8



308 C.DATA

M.DATA 24A8

24A4 M.PAR.OUT

20B6 D.PAR2

9D1 D.SYSOUT

3A1 D.XEN

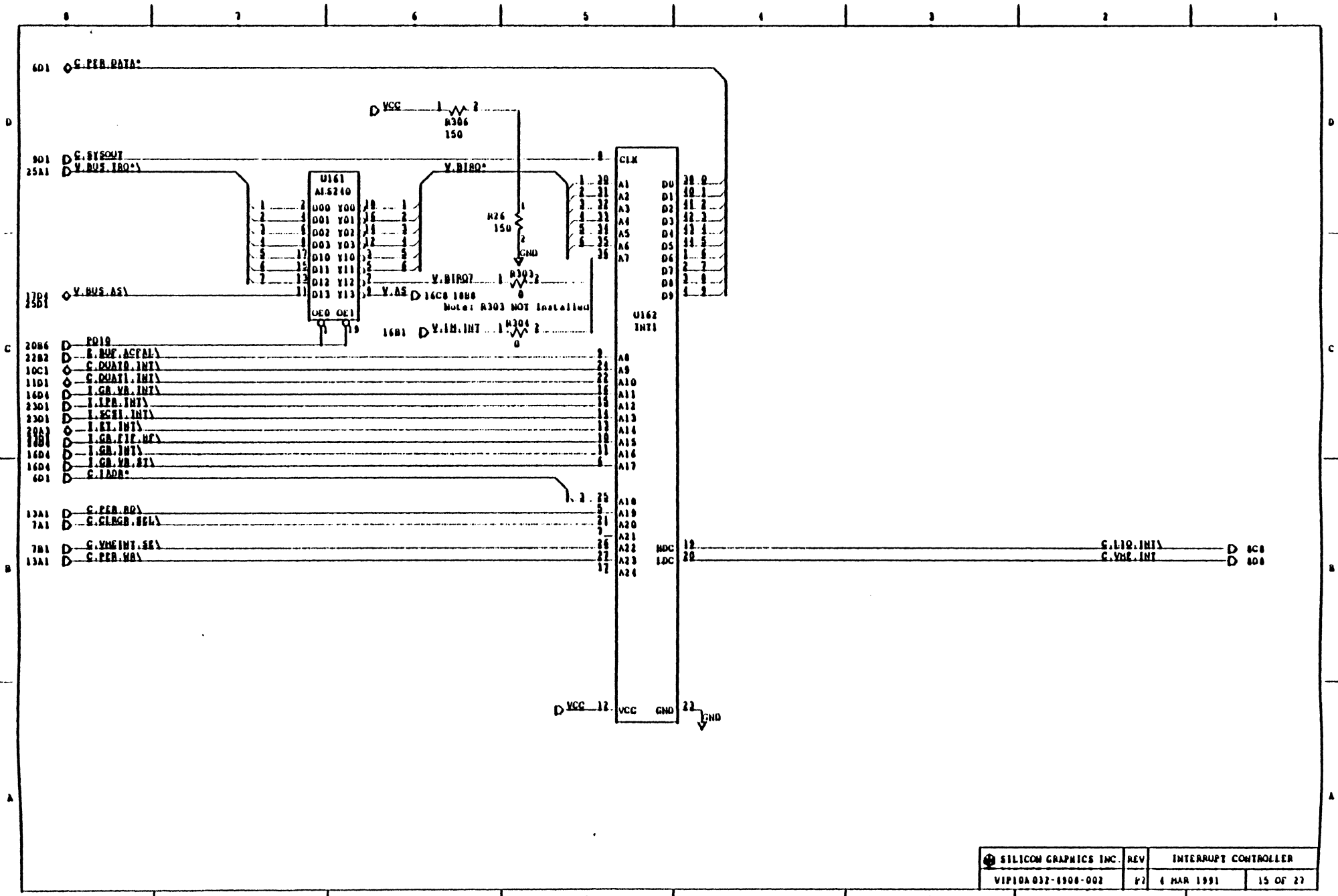
C.DATA 308

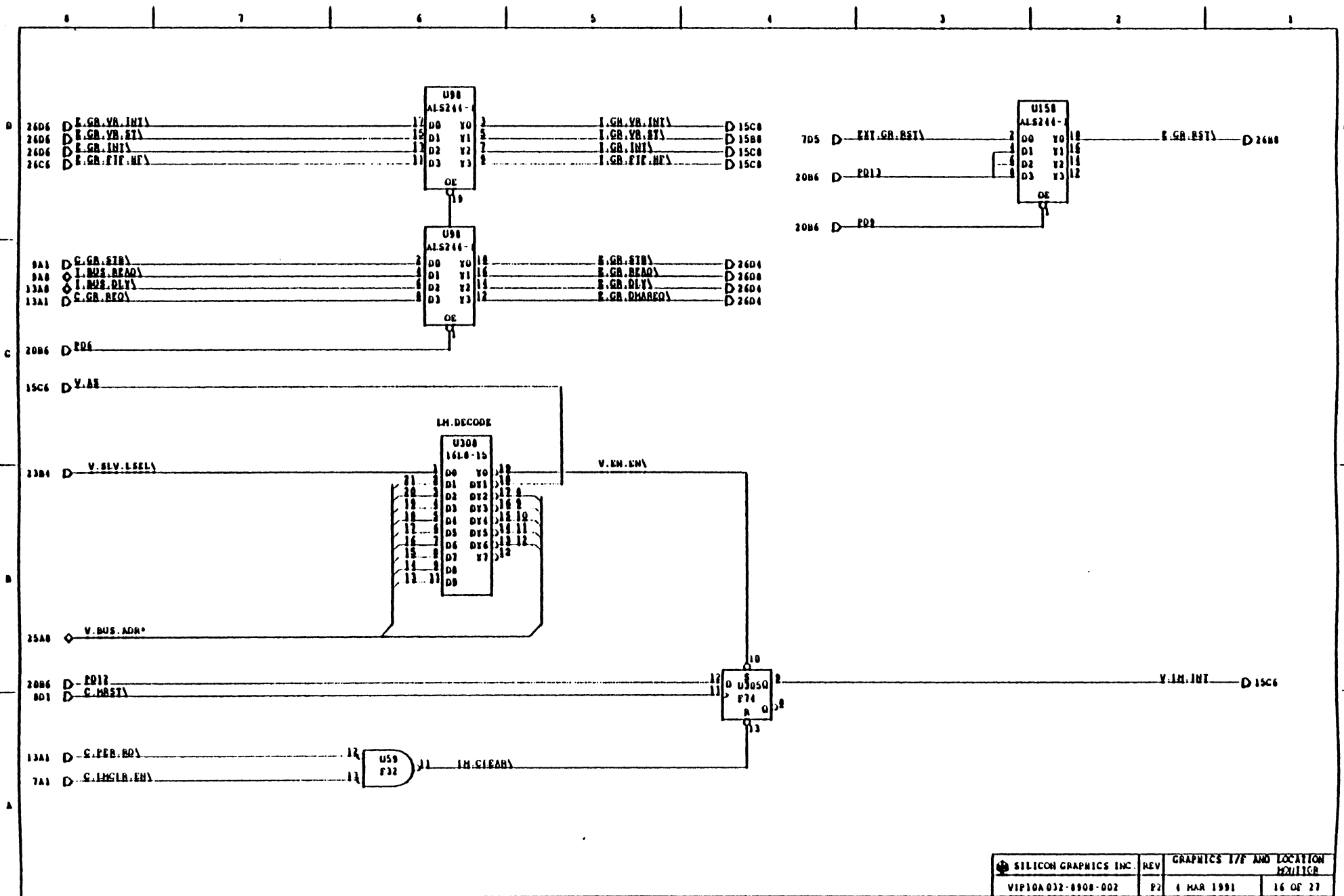
13C1 D.CAS.OUT

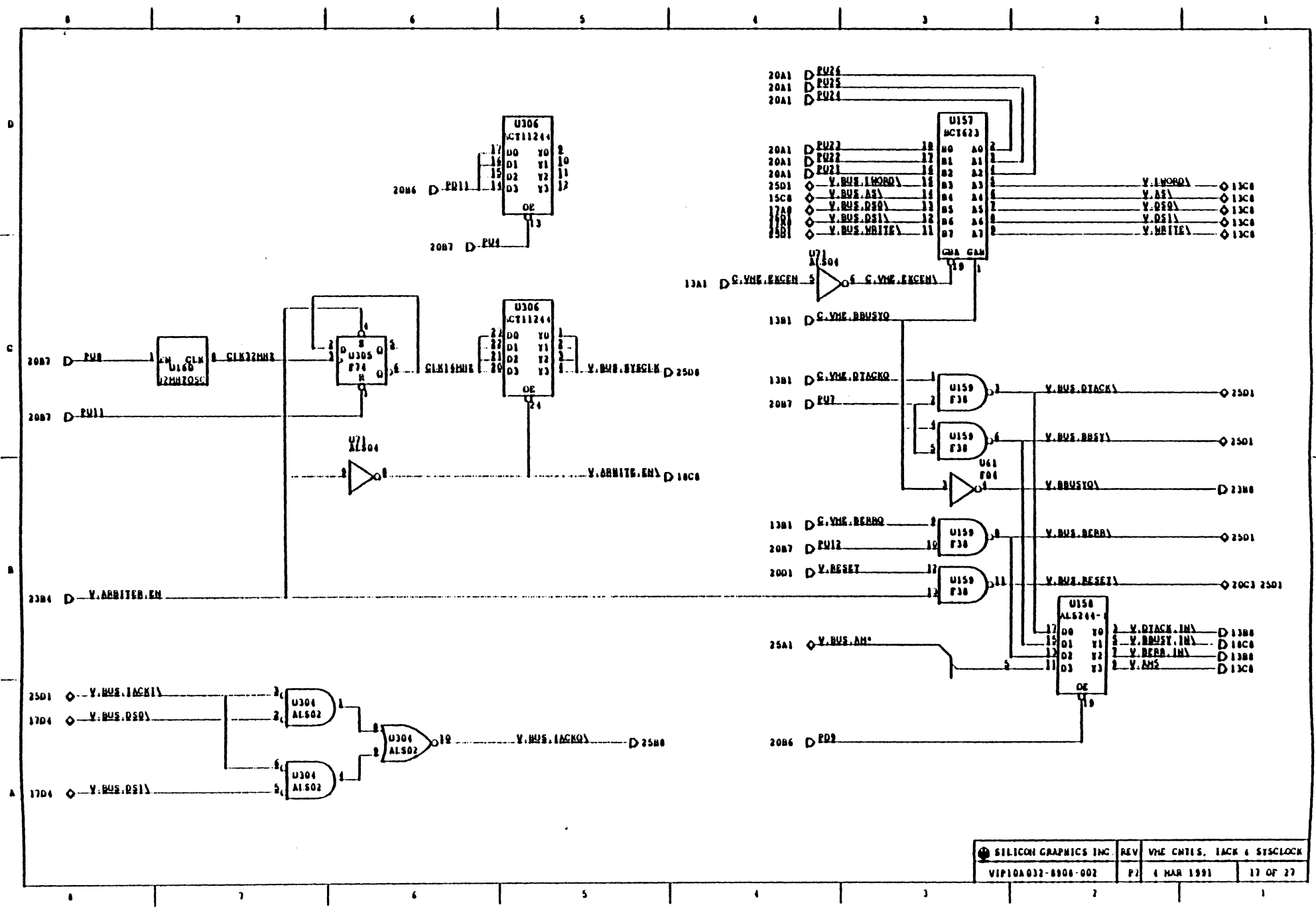
C.BAS.Z0 D.13B6

C.BAS.Z1 D.13B6

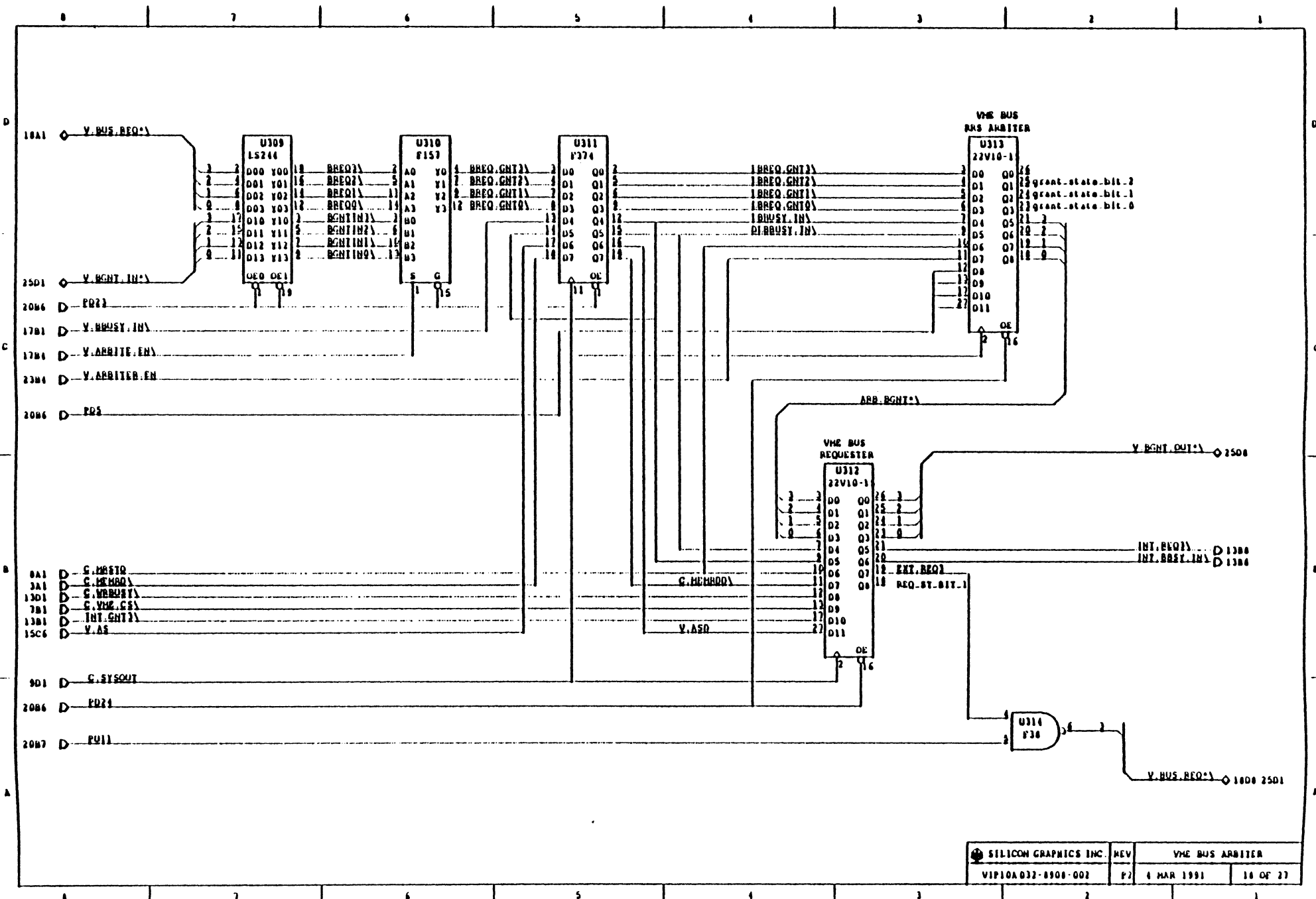
- 20B6 D.FD1
- 9D1 D.C.WBF.CLK
- 9C1 D.C.CPU.WDEN
- 8D1 D.C.PEB.CSD
- 8B1 D.C.RBF.CLK
- 3A1 D.C.XEN

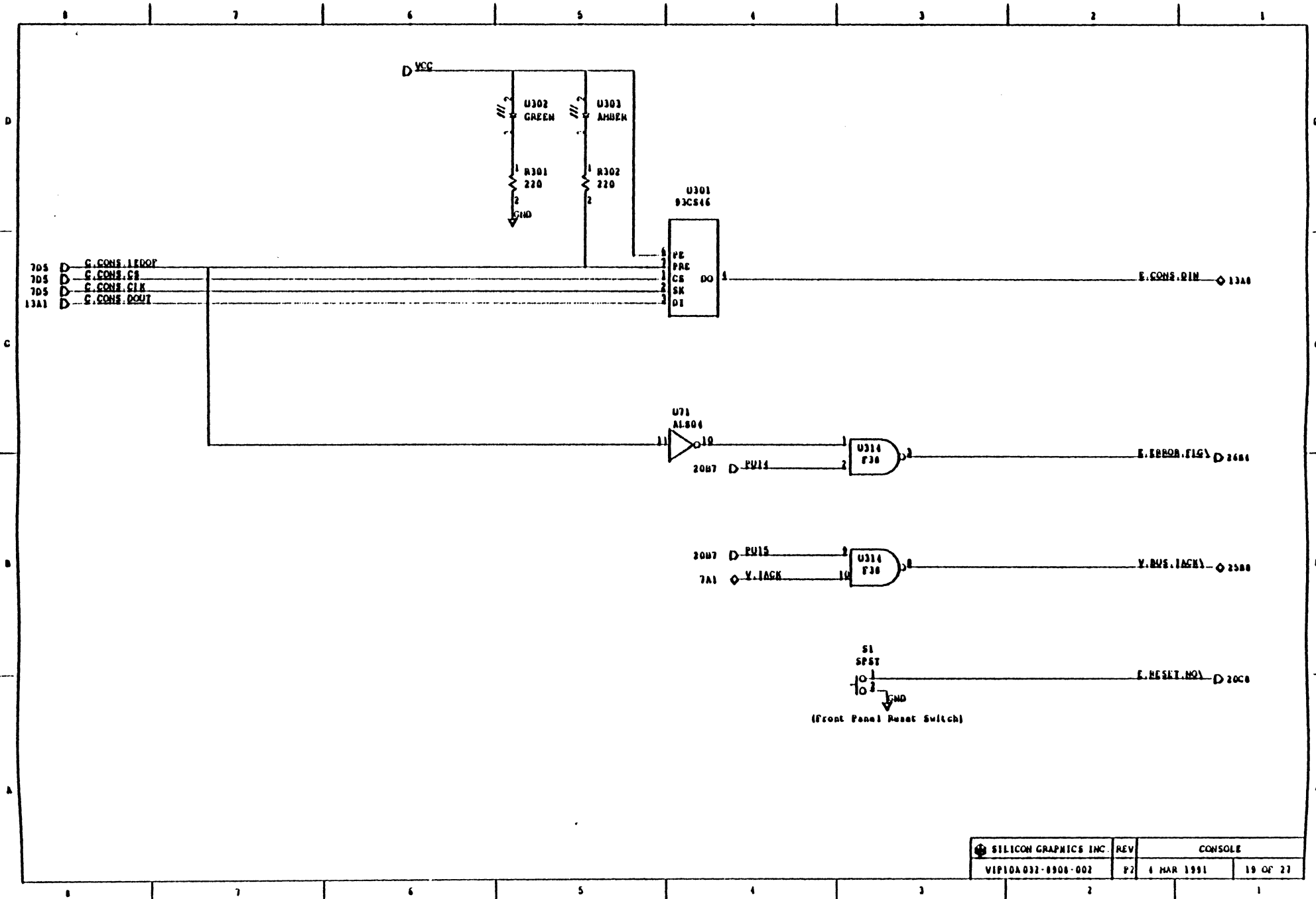


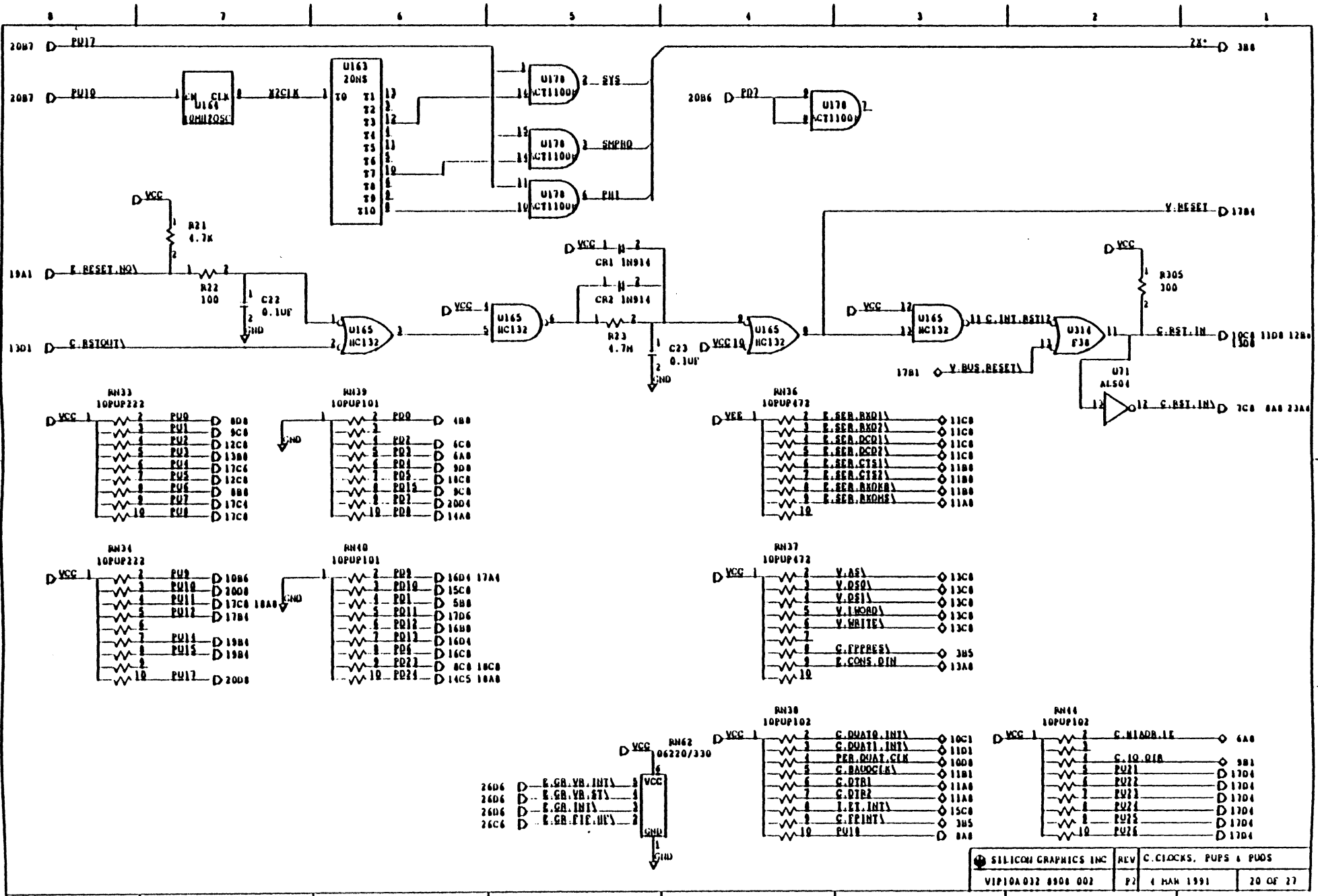


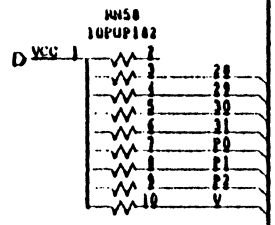
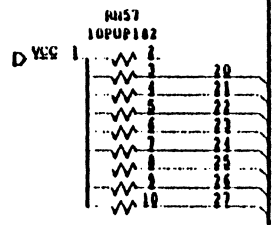
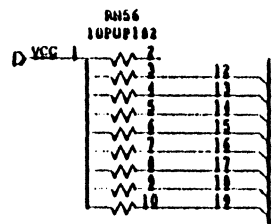
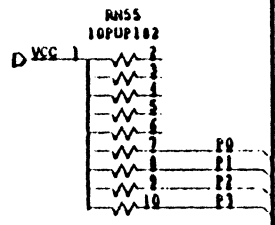
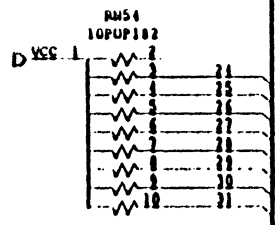
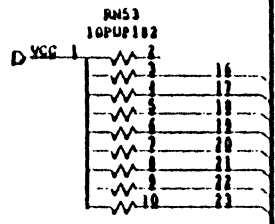
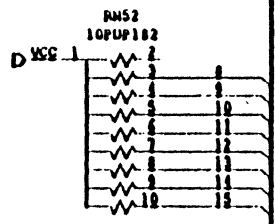
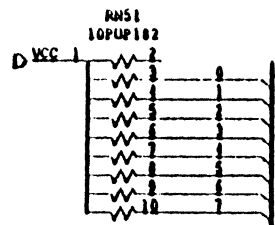


- 20A1 D PU26
- 20A1 D PU25
- 20A1 D PU24
- 20A1 D PU27
- 20A1 D PU22
- 20A1 D PU21
- 25D1 D V.BUS.LMOR0
- 15C8 D V.BUS.AS
- 17A9 D V.BUS.DS0
- 17B0 D V.BUS.DS1
- 25D1 D V.BUS.WRITE
- U71 A7104
- 13A1 D G.VME.EXGEN
- 13B1 D G.VME.BBUSTO
- 13B1 D G.VME.DTACKO
- 20B7 D PU7
- 13B1 D G.VME.BERRQ
- 20B7 D PU12
- 20D1 D V.RESET
- 25A1 D V.BUS.AM
- 20B6 D PD2
- U157 MCT673
- U159 F30
- U159 F30
- U61 F04
- U159 F30
- U159 F30
- U159 F30
- U158 ALS244
- 13C8 V.LMOR0
- 13C8 V.AS
- 13C8 V.DS0
- 13C8 V.DS1
- 13C8 V.WRITE
- 25D1 V.BUS.IACK0
- 25D1 V.BUS.BSY
- 23B8 V.BBUSTO
- 25D1 V.BUS.BERR
- 20C3 25D1 V.BUS.RESET
- 13B8 V.DIACK.IN
- 16C8 V.BBUST.IN
- 13B8 V.BERR.IN
- 13C8 V.AM2



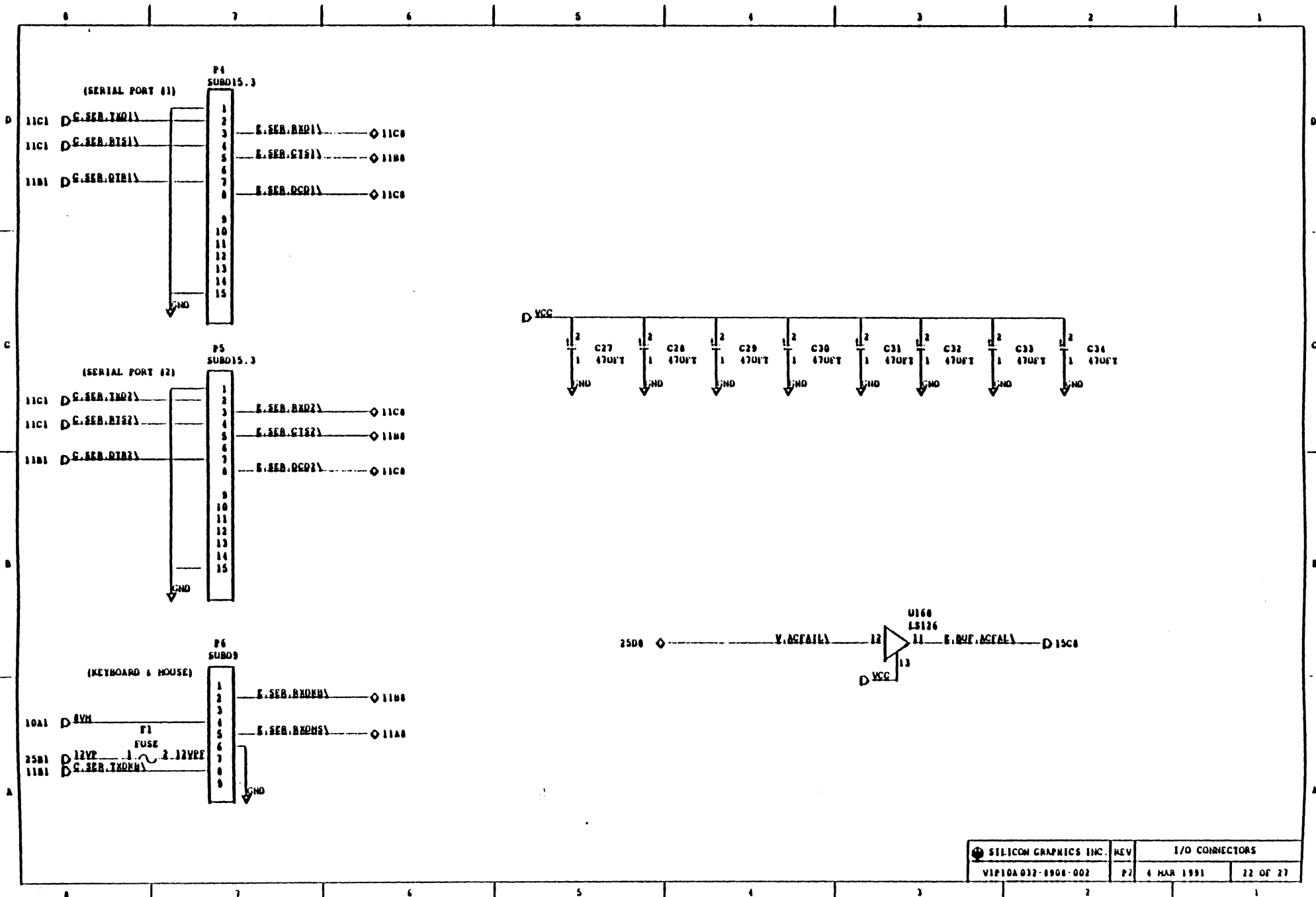


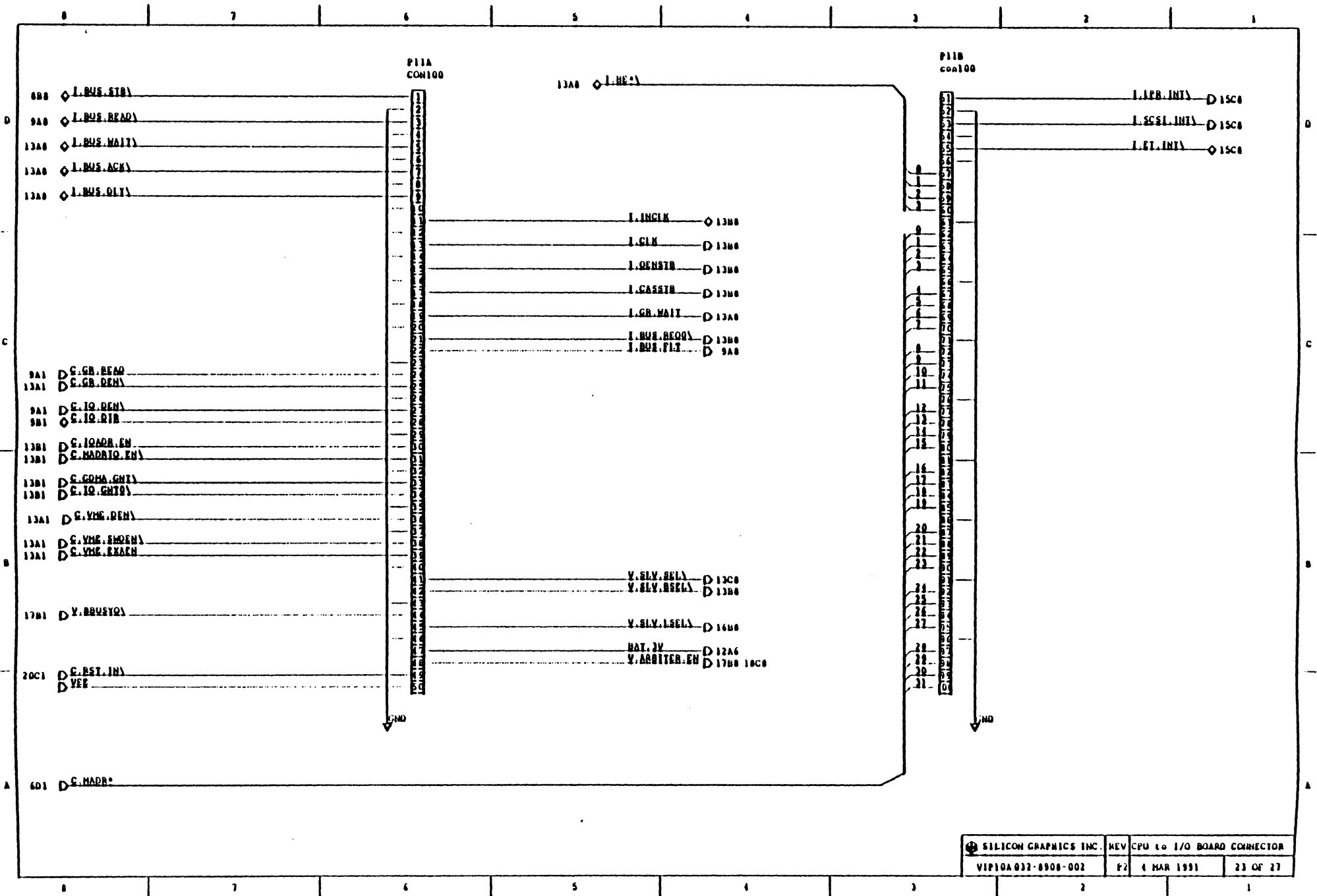


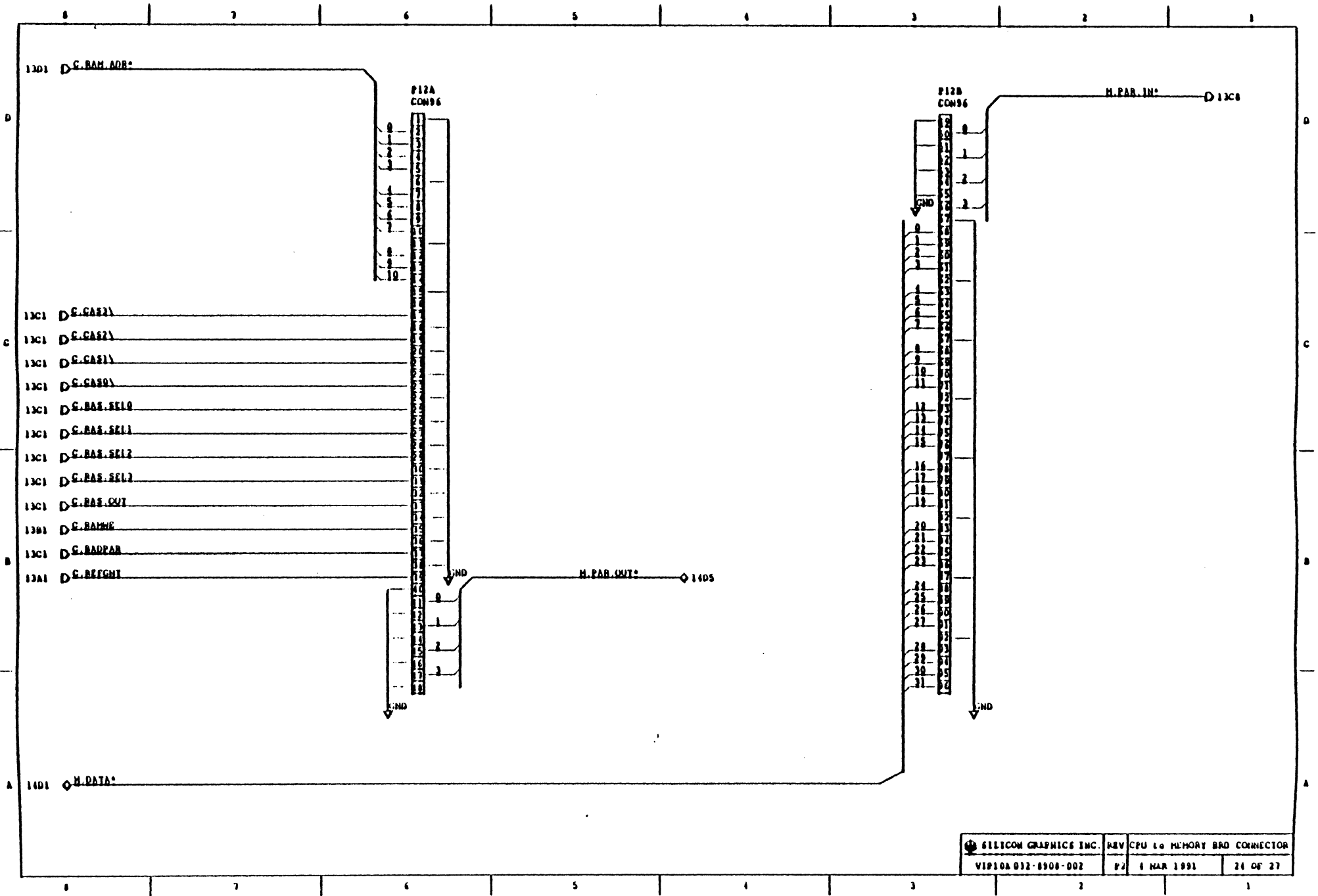


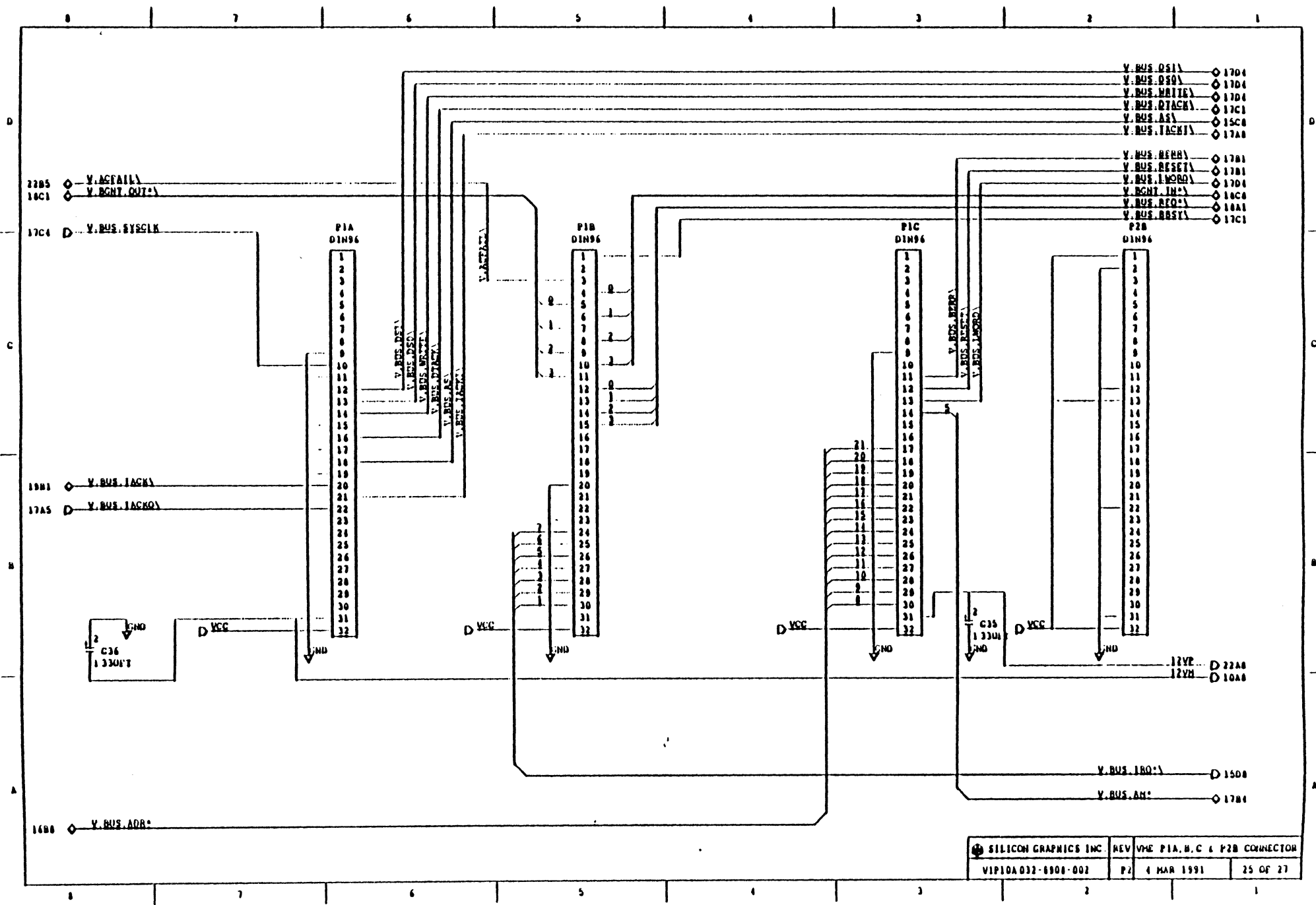
300 ○ C. DATA*

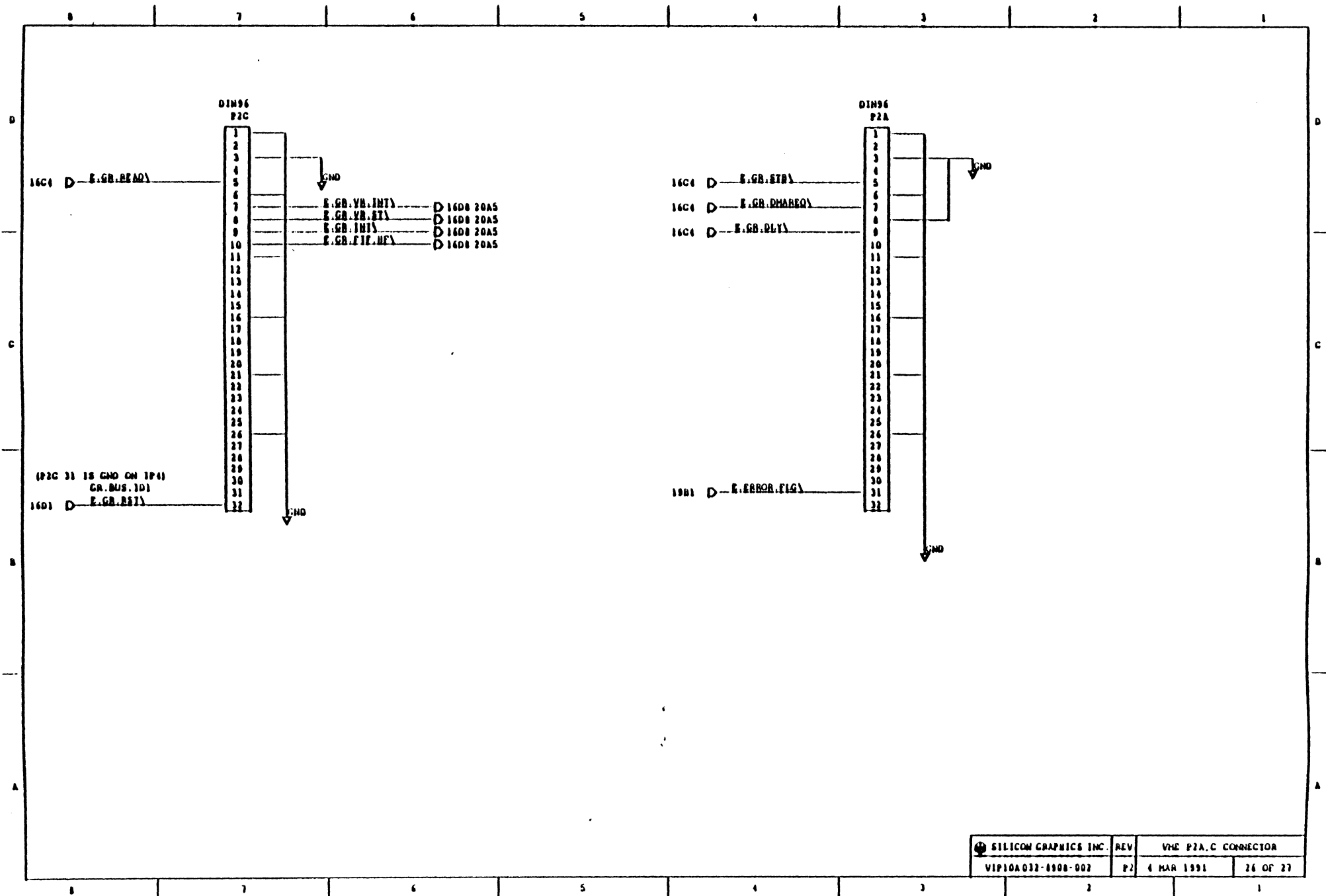
301 ○ C. TAG*

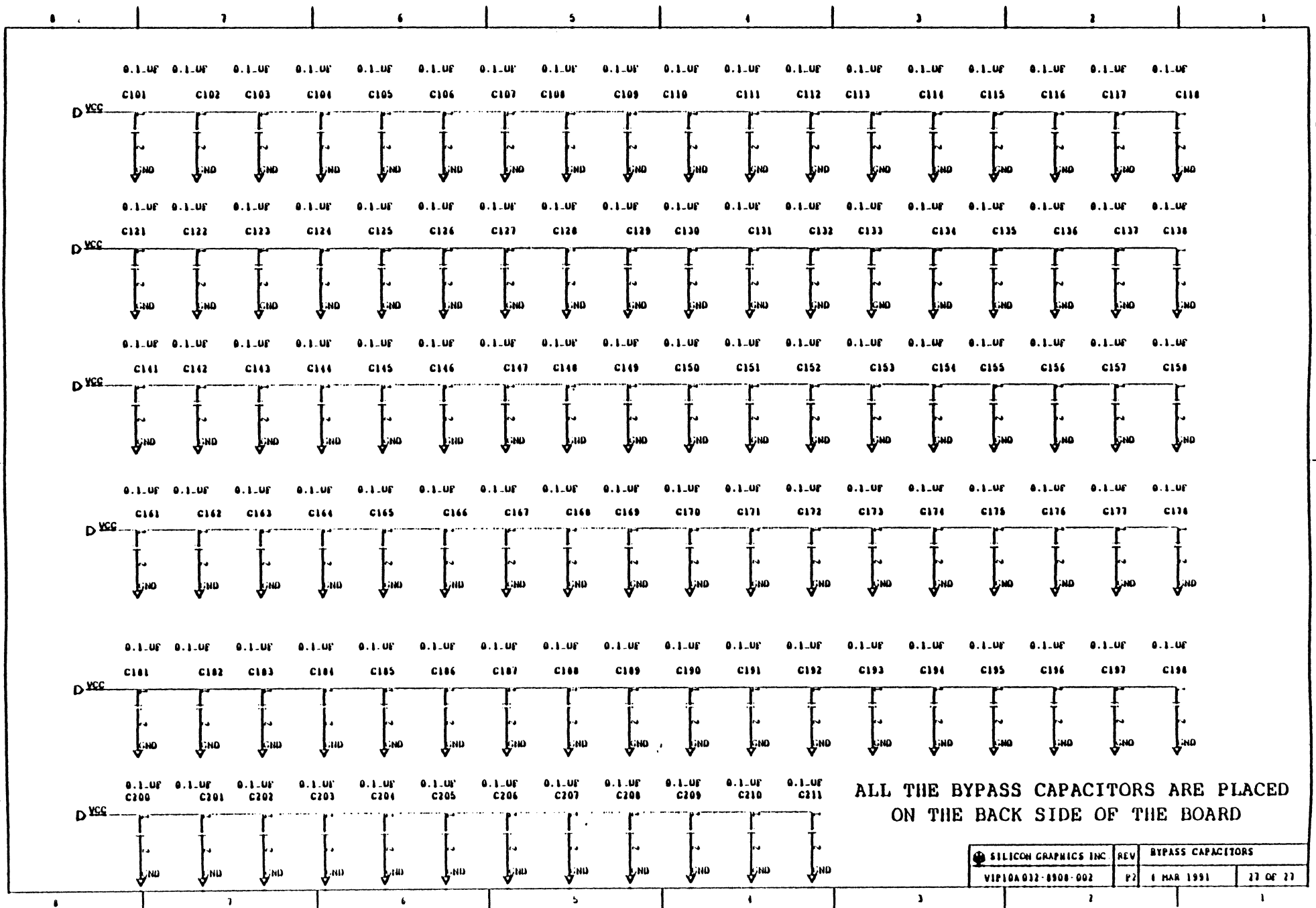






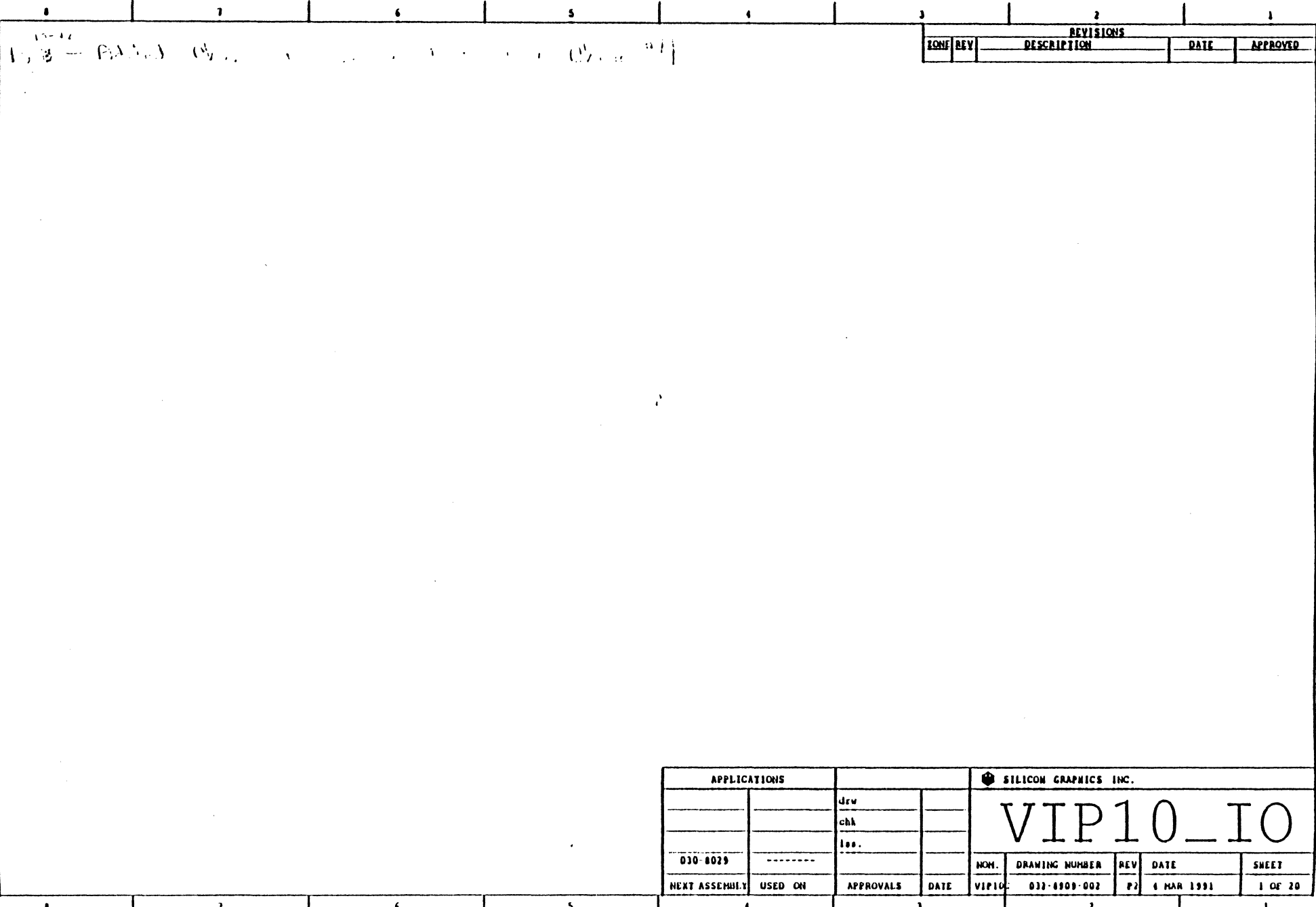






ALL THE BYPASS CAPACITORS ARE PLACED ON THE BACK SIDE OF THE BOARD

SILICON GRAPHICS INC VIP10A032-0500-002	REV	BYPASS CAPACITORS	
	P2	1 MAR 1991	27 OF 27



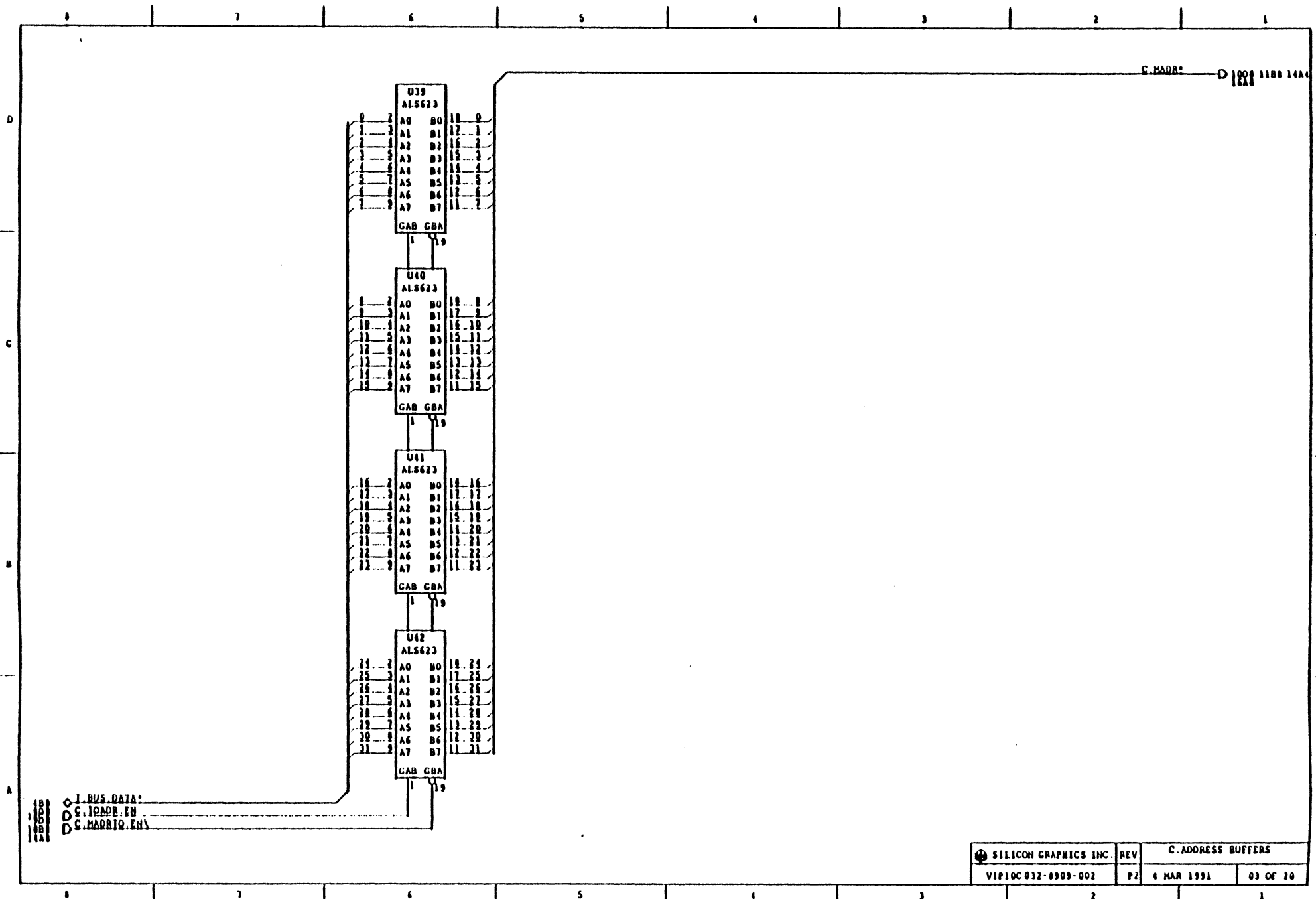
1, 3 - P.A.M. (y... .. (y... ..)

REVISIONS				
CONF	REV	DESCRIPTION	DATE	APPROVED

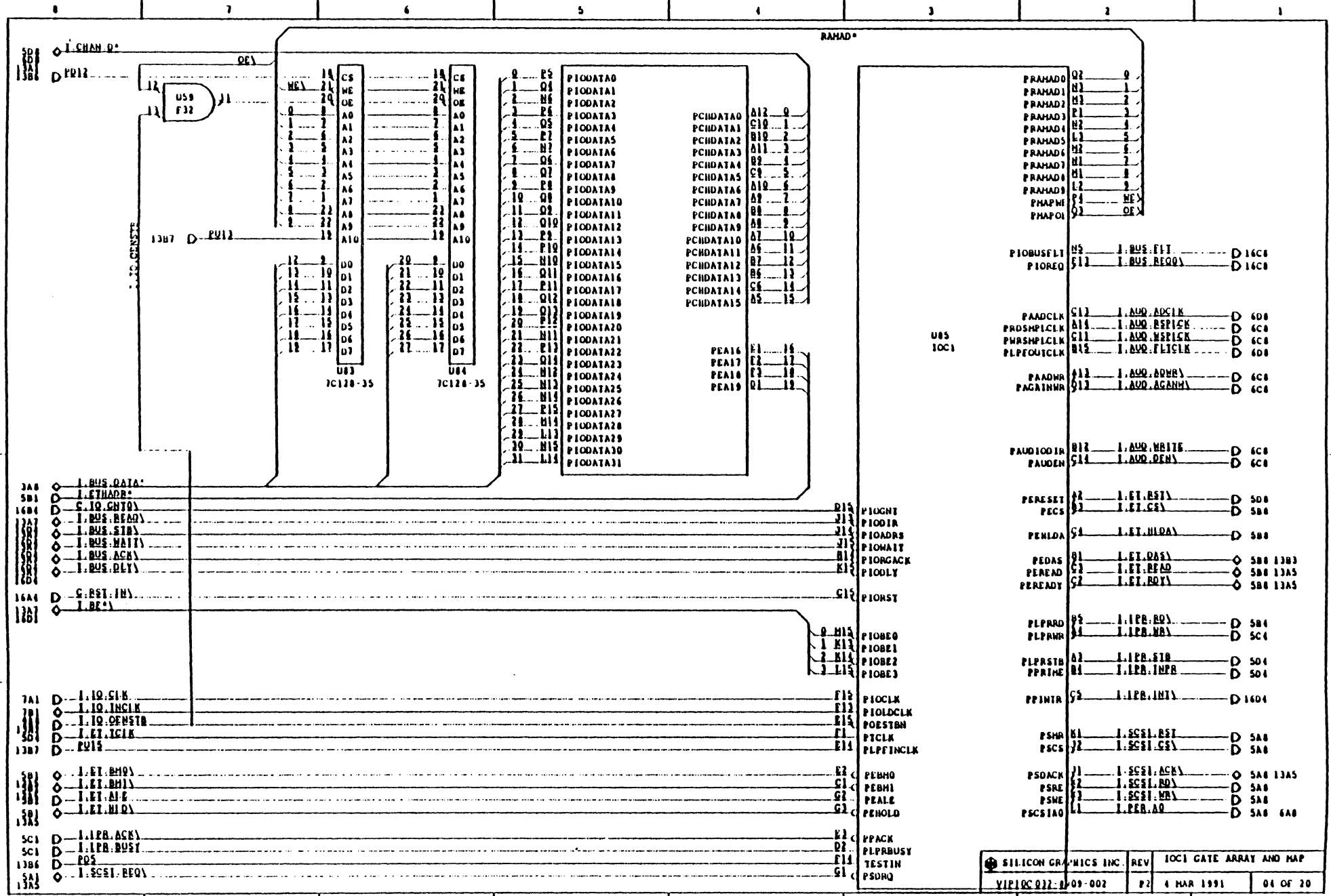
APPLICATIONS		SILICON GRAPHICS INC.						
		dev		VIP10_IO				
		chk						
		iss.						
030-8029	-----			MON.	DRAWING NUMBER	REV	DATE	SHEET
NEXT ASSEMBLY	USED ON	APPROVALS	DATE	VIP10:	030-8900-002	P2	4 MAR 1991	1 OF 20

PAGE 1 DESCRIPTION

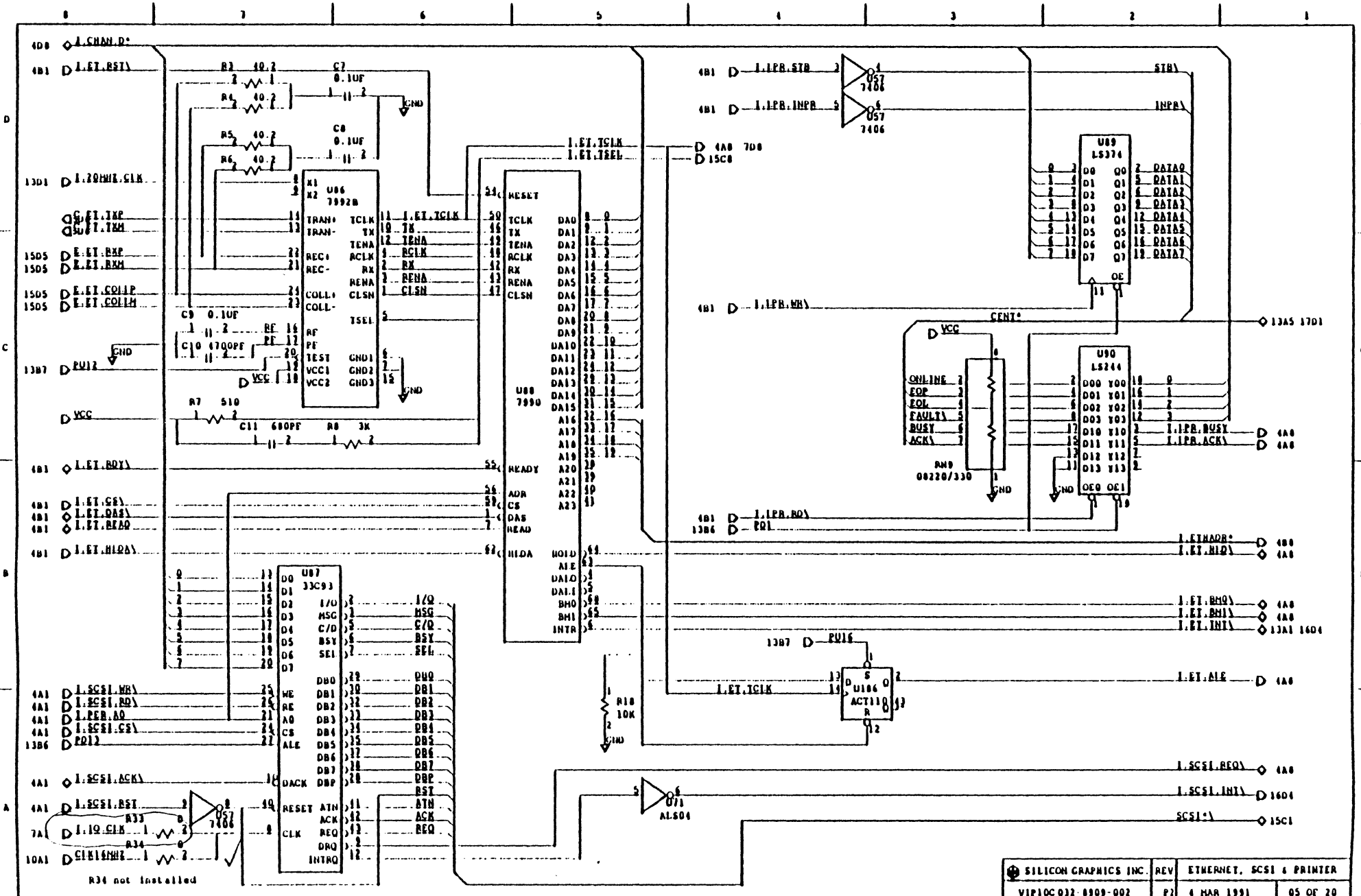
03	CPU ADDRESS BUFFERS
04	IOC GATE ARRAY AND MAP
05	ETHERNET, SCSI AND PRINTER
06	AUDIO I/O
07	GRAPHICS I/F AND I/O CLOCKS
08	GRAPHICS BUFFERS
09	MEMORY DATA BUFFERS
10	VME DATAPATH
11	VME SLAVE ADDRESS DECODING
12	VME BUS TIMER
13	PUPS & PUGS, BATTERY, OSC1
14	BUS PUPS
15	PERIPHERAL CONNECTORS
16	CPU to I/O BOARD CONNECTOR
17	I/O to MEMORY BOARD CONNECTOR
18	VME P1A,B,C AND P2B CONNECTORS
19	VME P2A,C (GRAPHICS) CONNECTORS
20	BYPASS CAPACITORS



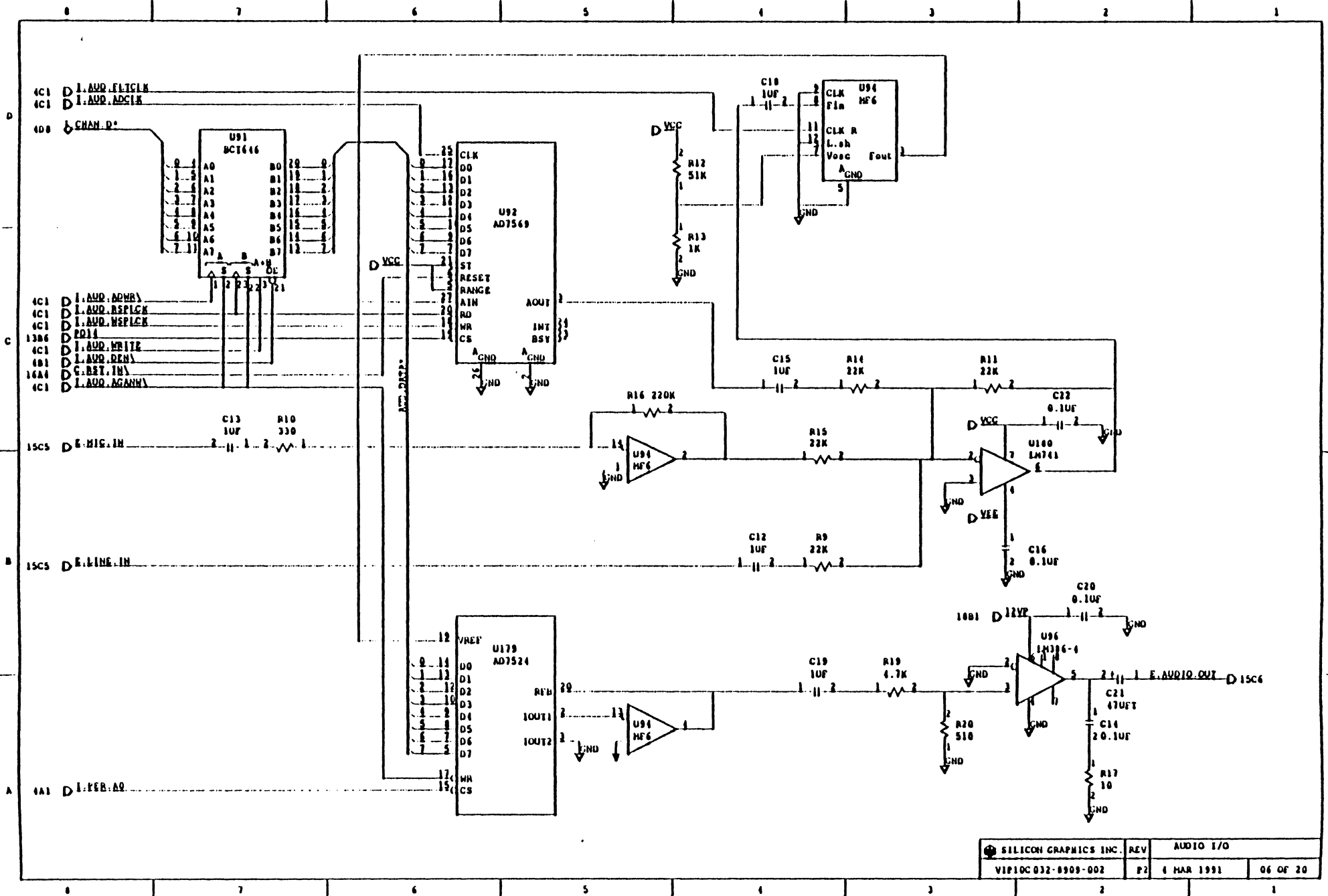
SILICON GRAPHICS INC.	REV	C. ADDRESS BUFFERS	
	P2	4 MAR 1991	03 OF 28

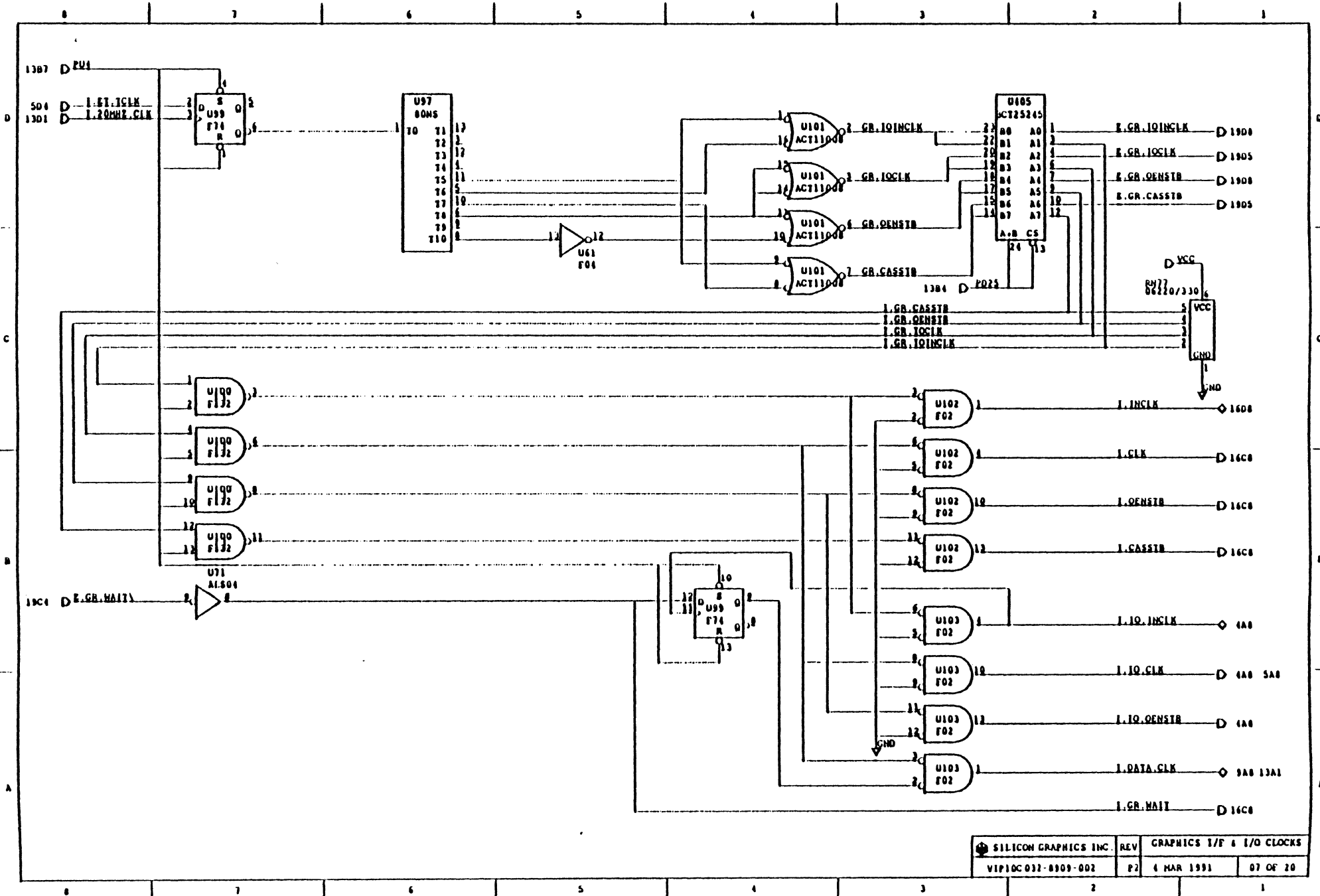


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	09-002	P2	4 MAR 1991
VIPI0C022-8			01 OF 20

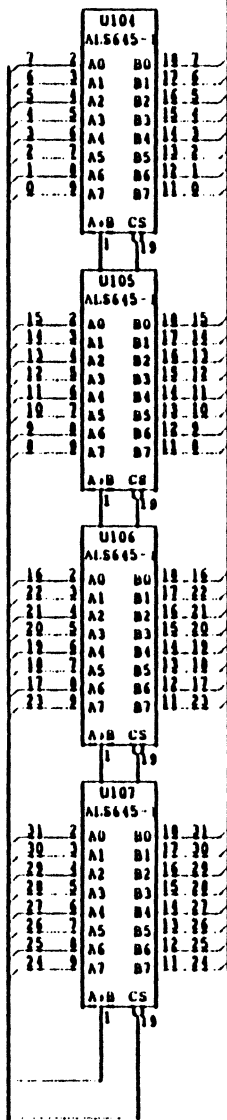


R34 not installed





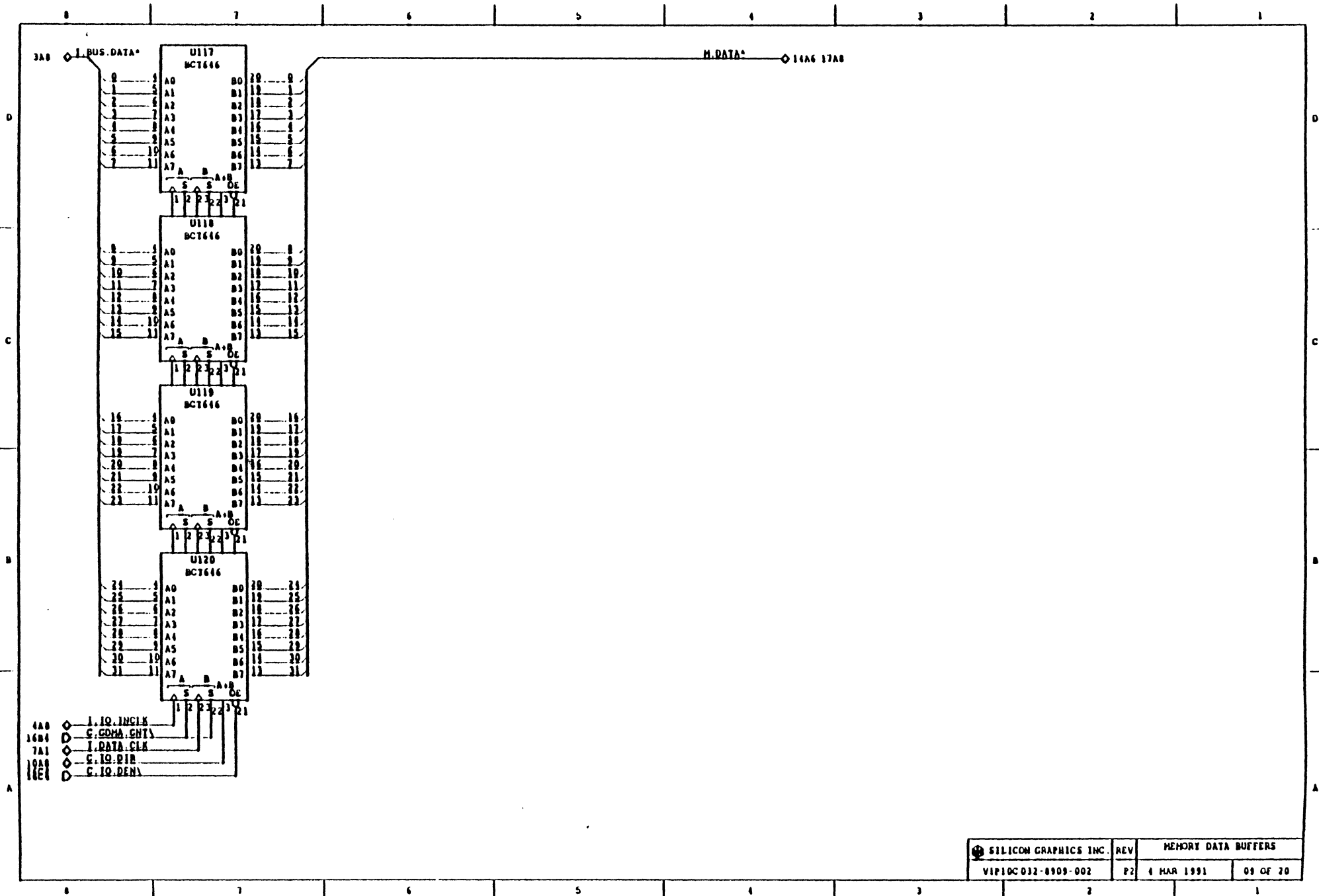
JAB \diamond I.BUS DATA*

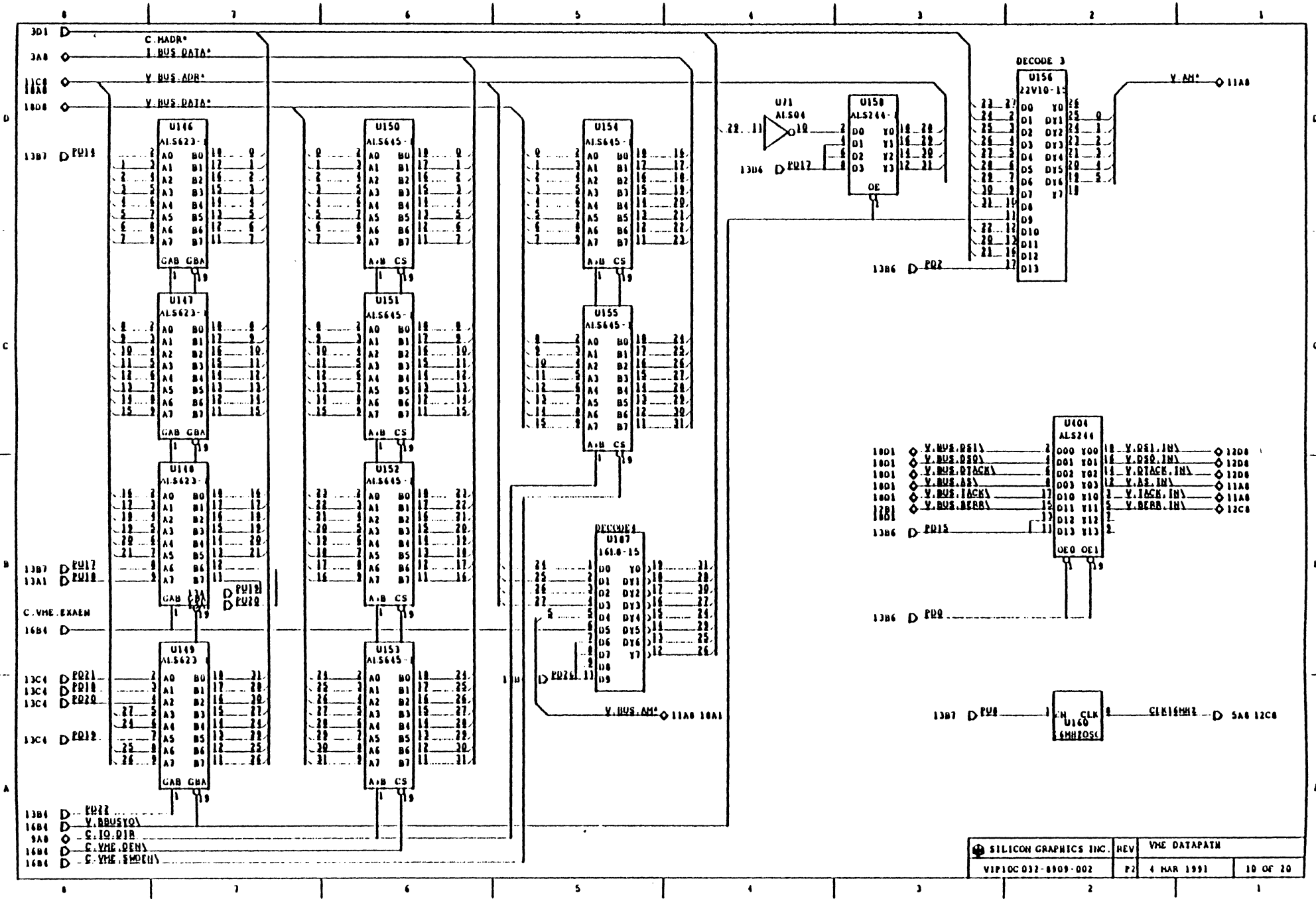


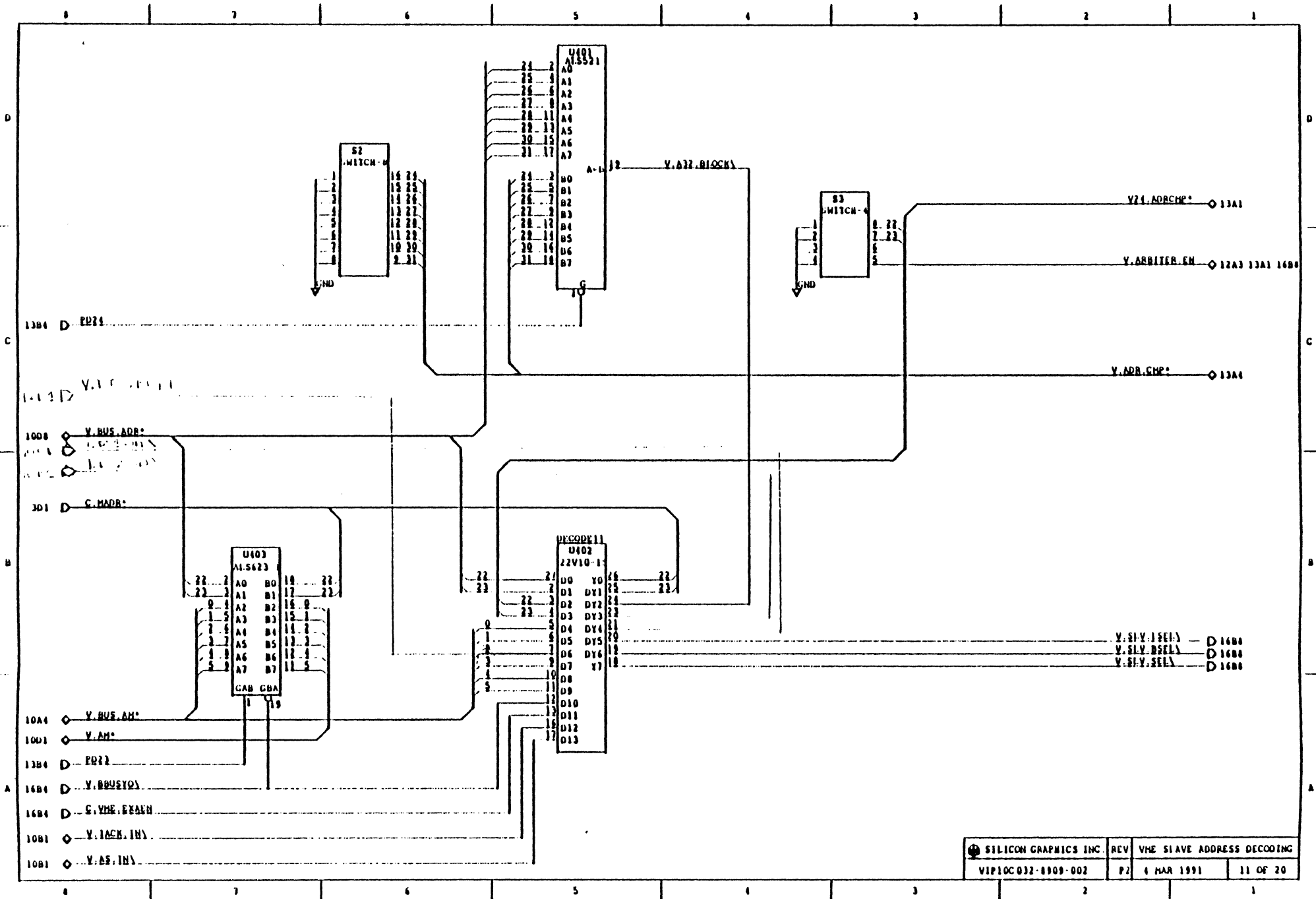
16C4 D - S.GB. READ

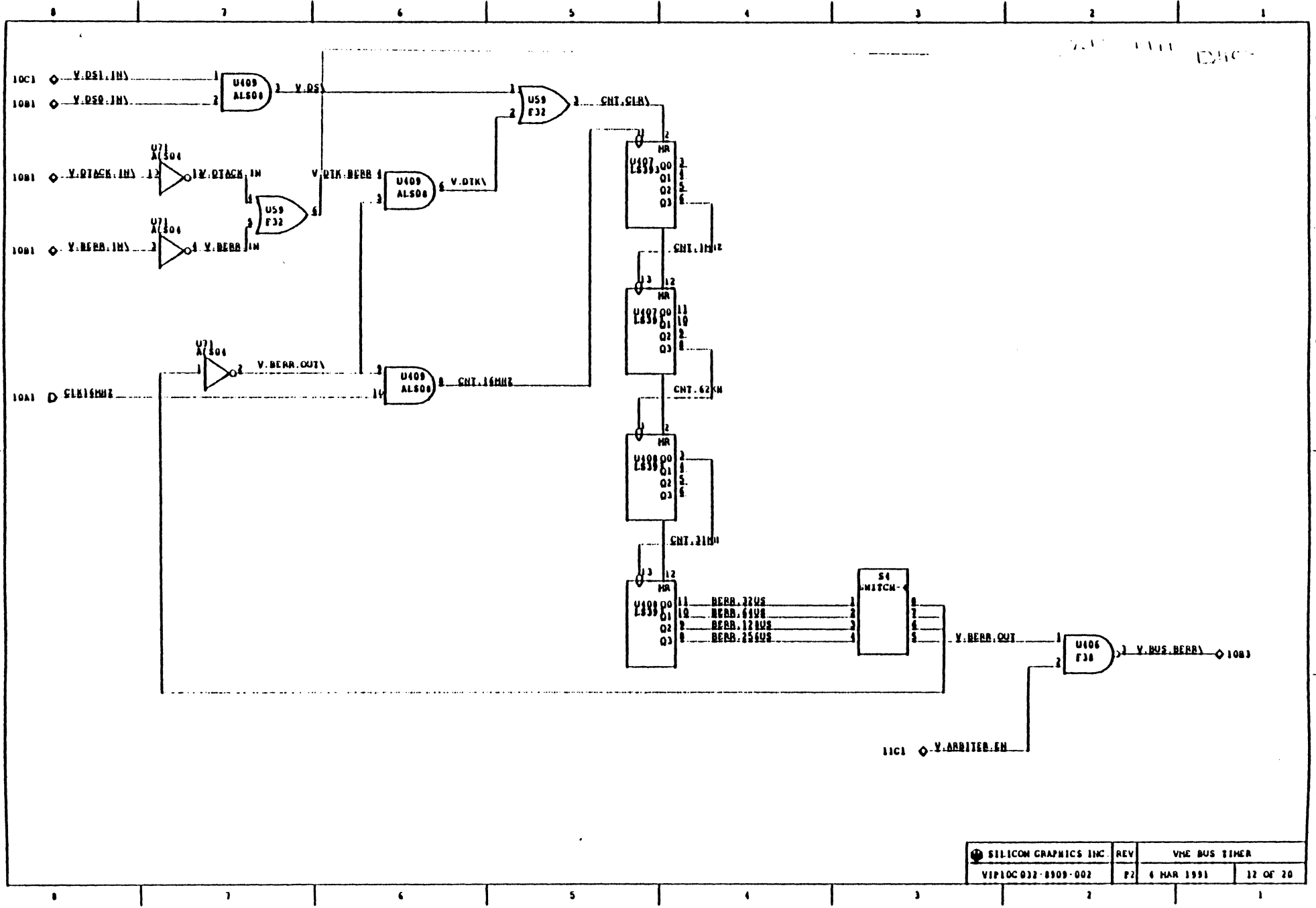
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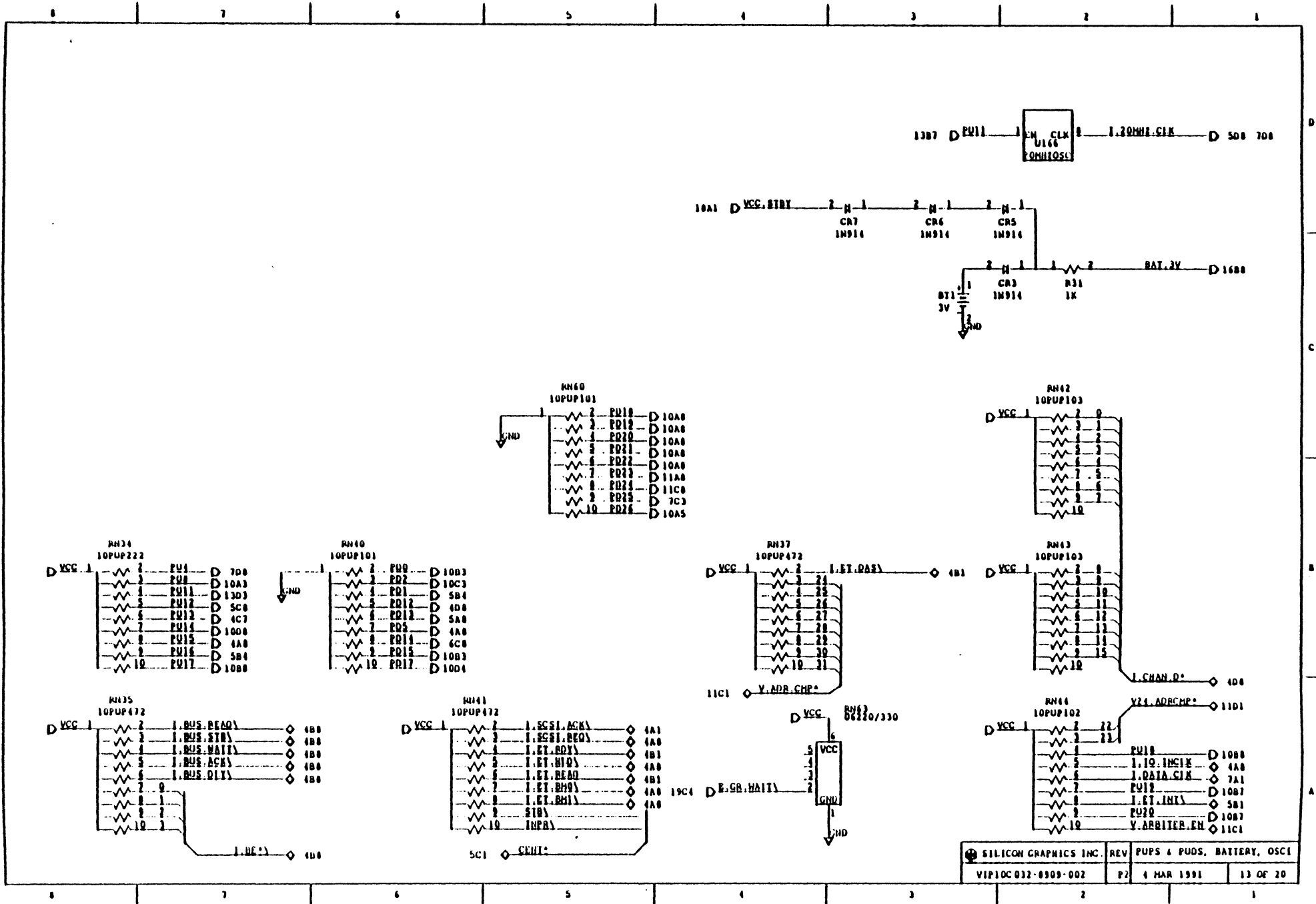
S.GR. DATA* \diamond 19A8











13B7 D PUL1 — 1 — CM CLK U166 1.20MHZ CLK — 8 — 508 708

10A1 D VCC STBY — 2 — H — 1 — 2 — H — 1 — 2 — H — 1 — CR7 1M914 CR6 1M914 CR5 1M914
 — 2 — H — 1 — 1 — R31 1K — 2 — BAT 3V — 1688
 BT1 3V — 1 — 1 — GND — 2 —

RN60 10PUP101
 2 PU18 — 10A8
 3 PD18 — 10A8
 4 PD19 — 10A8
 5 PD20 — 10A8
 6 PD21 — 10A8
 7 PD22 — 10A8
 8 PD23 — 11A8
 9 PD24 — 11C8
 10 PD25 — 7C3
 11 PD26 — 10A5

RN12 10PUP103
 2 0
 3 1
 4 2
 5 3
 6 4
 7 5
 8 6
 9 7
 10 8

RN36 10PUP222
 2 PU1 — 708
 3 PU8 — 10A3
 4 PU11 — 1303
 5 PU12 — 5C8
 6 PU13 — 4C7
 7 PU14 — 1006
 8 PU15 — 1A8
 9 PU16 — 5B4
 10 PU17 — 1088

RN40 10PUP101
 2 PU9 — 10B3
 3 PD2 — 10C3
 4 PD1 — 5B4
 5 PD12 — 4D8
 6 PD13 — 5A8
 7 PD5 — 4A8
 8 PD14 — 6C8
 9 PD15 — 10B3
 10 PR17 — 10D4

RN37 10PUP472
 2 21
 3 22
 4 23
 5 24
 6 27
 7 28
 8 29
 9 30
 10 31

11C1 — V. ADDR. CHP* — 4B1
 11C1 — V. ADDR. CHP* — 4D8

RN13 10PUP103
 2 8
 3 9
 4 10
 5 11
 6 12
 7 13
 8 14
 9 15
 10 16

Y24. ADDR. CHP* — 11D1

RN35 10PUP472
 2 1. BUS. BEAD — 4B8
 3 1. BUS. STBY — 4B8
 4 1. BUS. WAIT — 4B8
 5 1. BUS. ACK — 4B8
 6 1. BUS. DLY — 4B8
 7 8
 8 1
 9 2
 10 3

1. BE. — 4B8

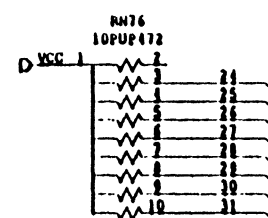
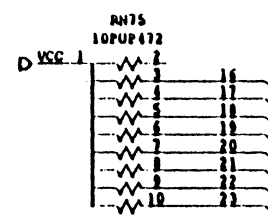
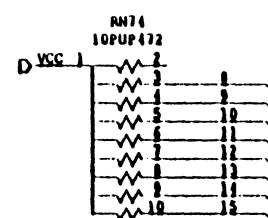
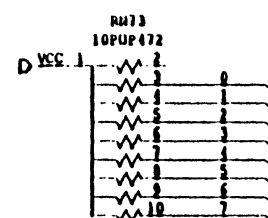
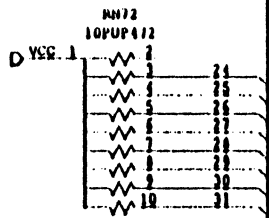
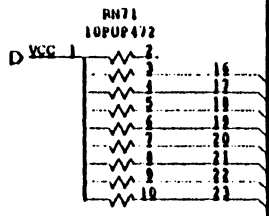
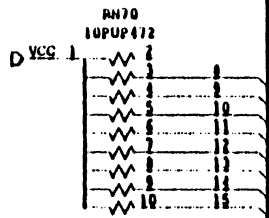
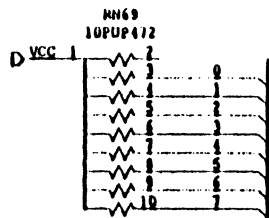
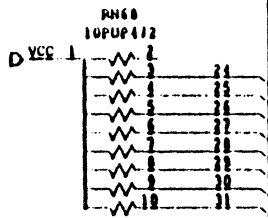
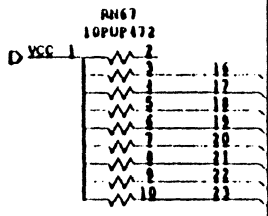
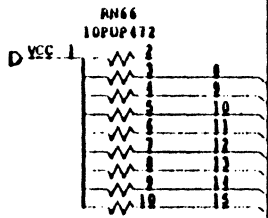
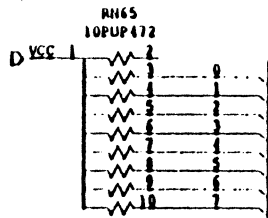
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 2 1. CS1. ACK — 4A1
 3 1. CS1. BEQ — 4A8
 4 1. ET. RDY — 4B1
 5 1. ET. HLD — 4A8
 6 1. ET. BEAD — 4B1
 7 1. ET. BHO — 4A8
 8 1. ET. BHI — 4A8
 9 STBY — 4A8
 10 INPR — 4A8

19C4 — 19C4
 5C1 — CHP* — 4A8

RN32 06220/330
 5 VCC
 6 GND
 1 GND

19C4 — 19C4
 5C1 — CHP* — 4A8

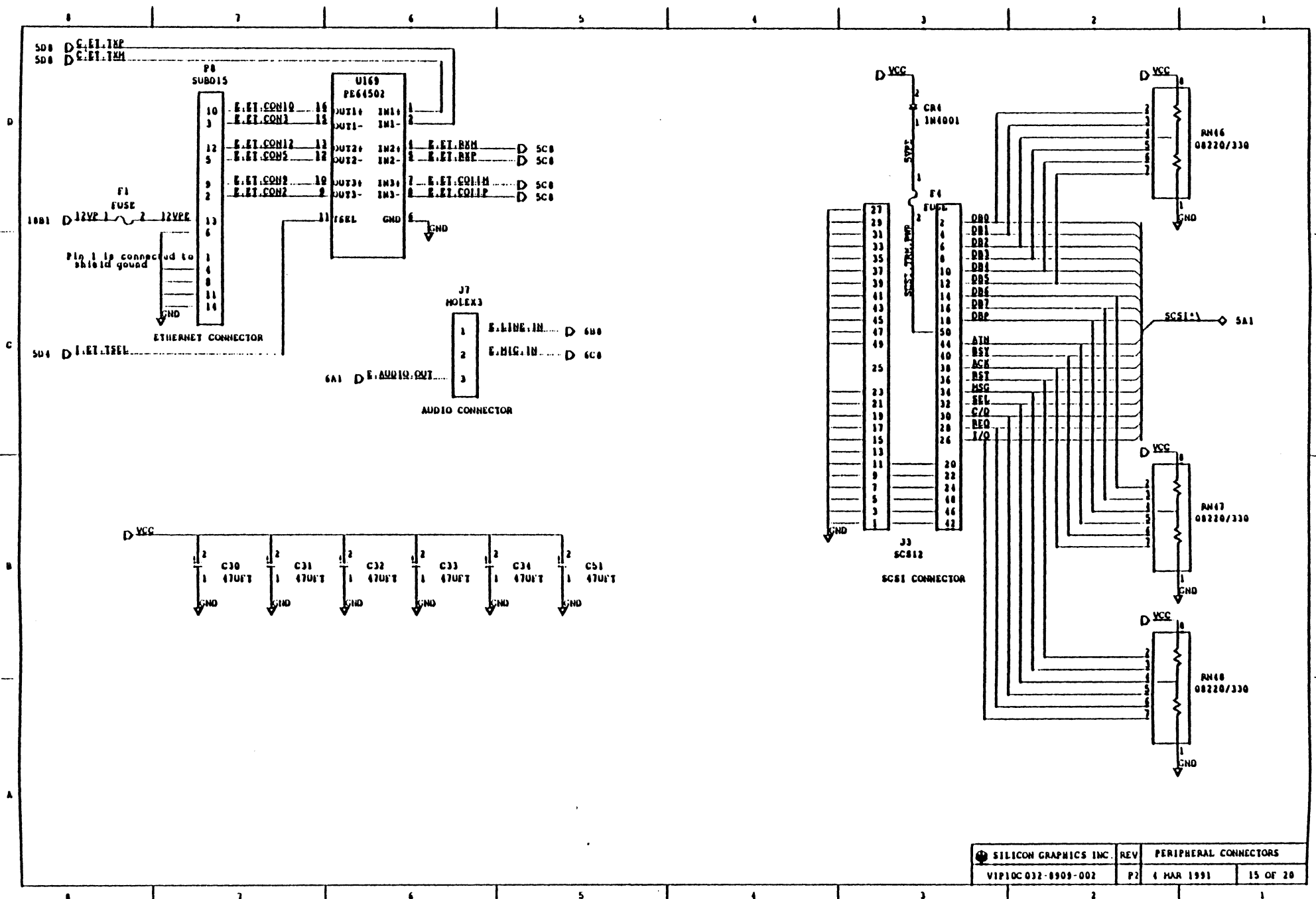
RN44 10PUP102
 2 22
 3 23
 4 24
 5 1. IO. INCK — 4A8
 6 1. DATA. CLK — 7A1
 7 PU18 — 10B8
 8 1. ET. INT — 5B1
 9 PU28 — 10B7
 10 V. ARBITER. EN — 11C1

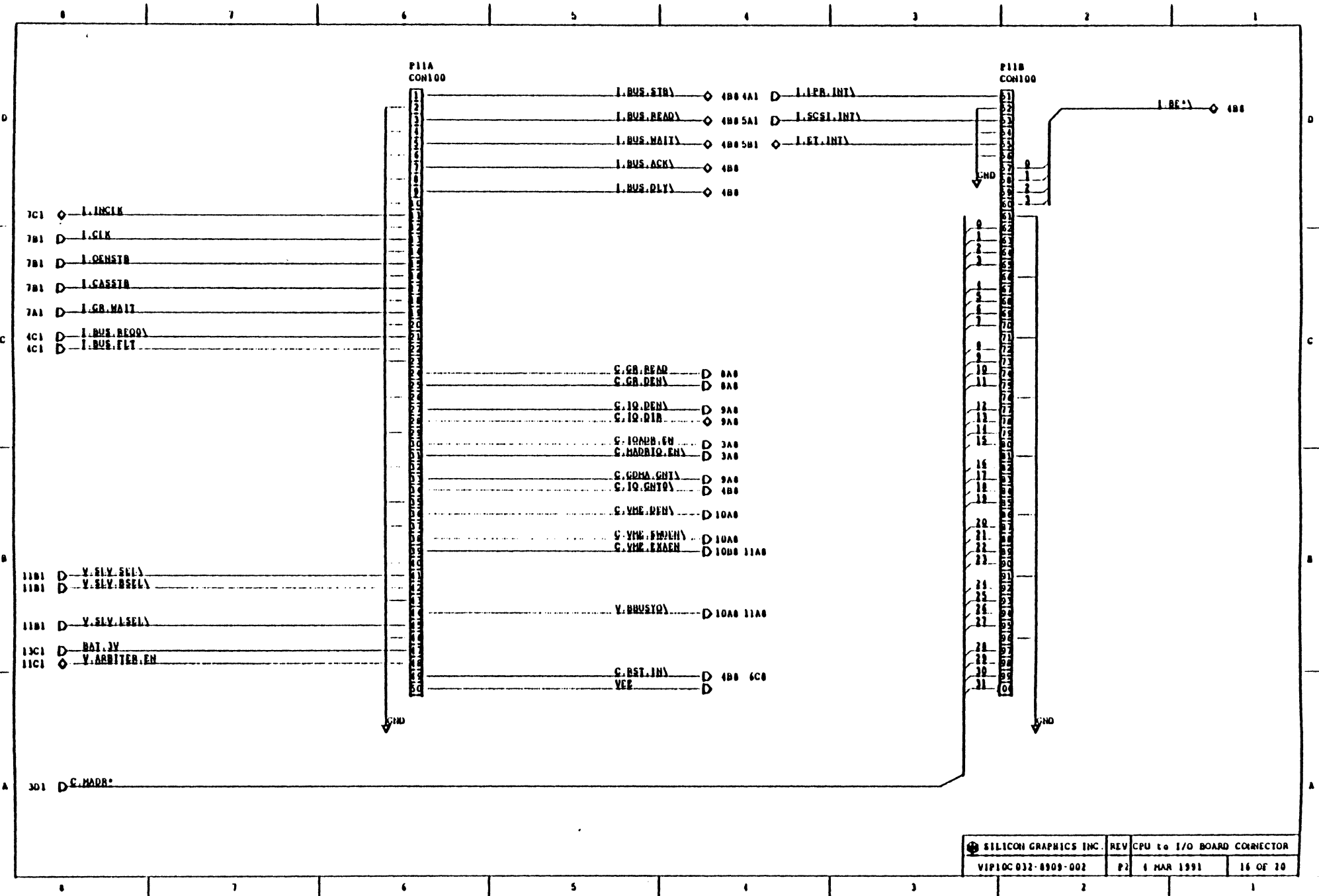


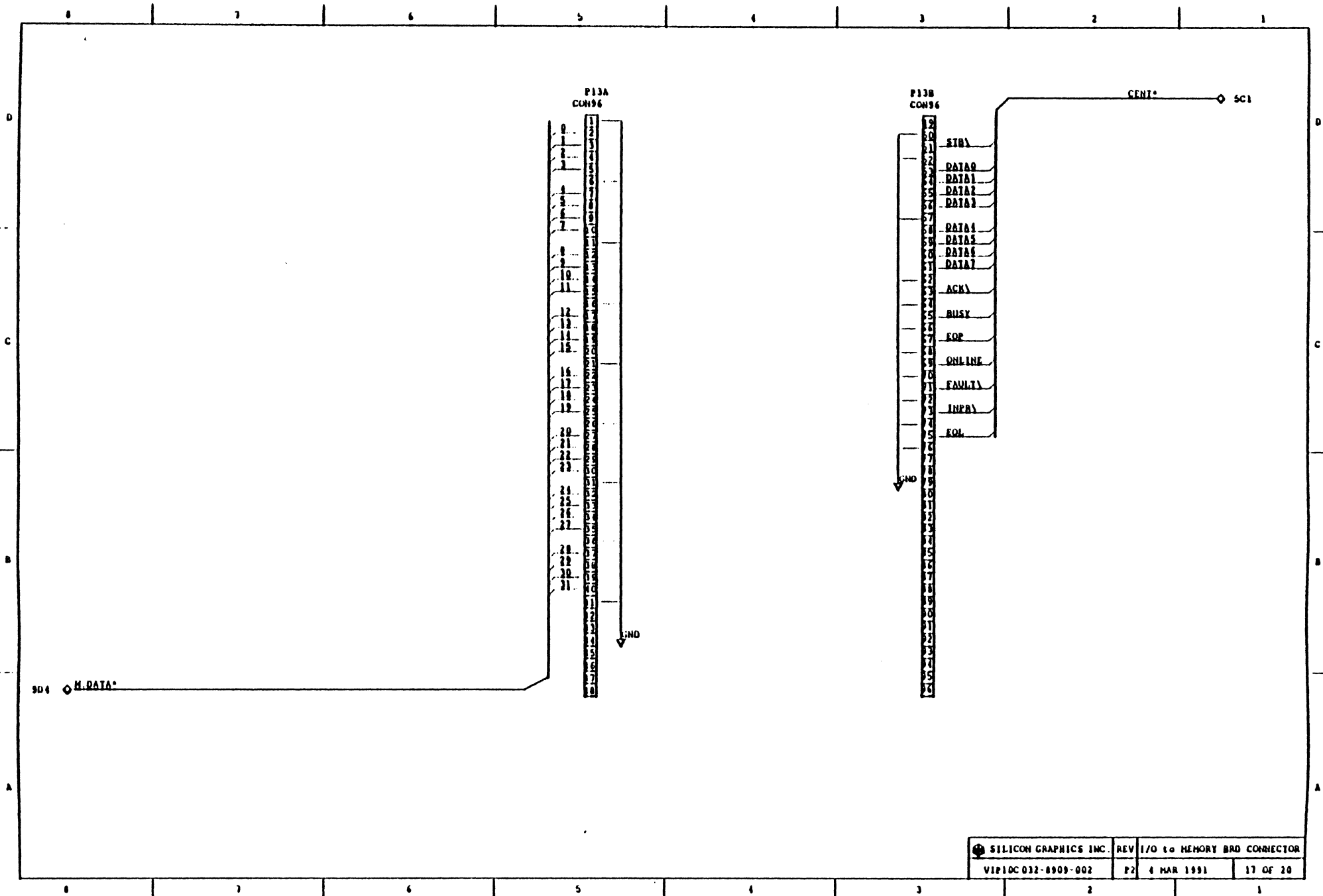
3A8 I. BUS DATA*

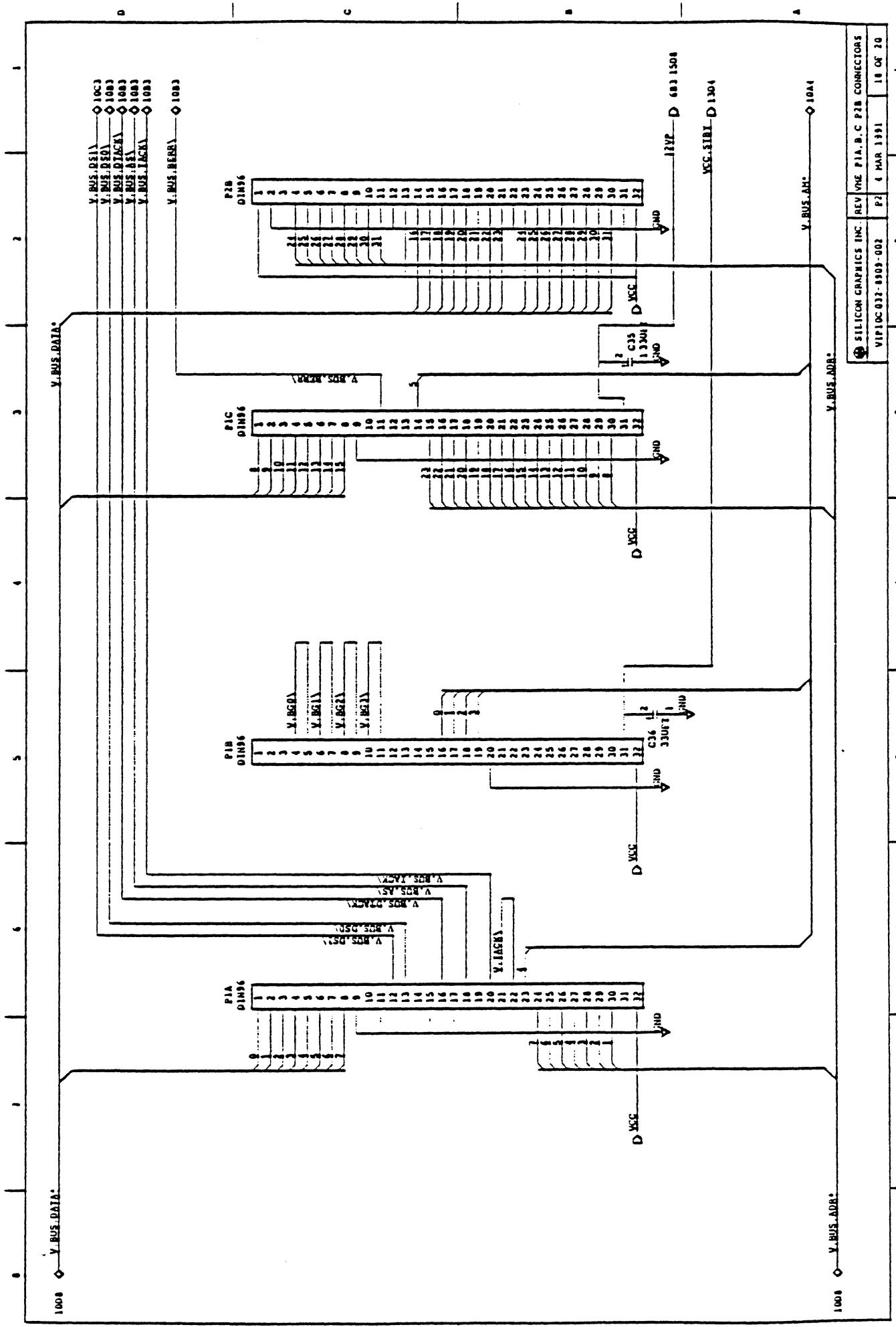
3D4 M. DATA*

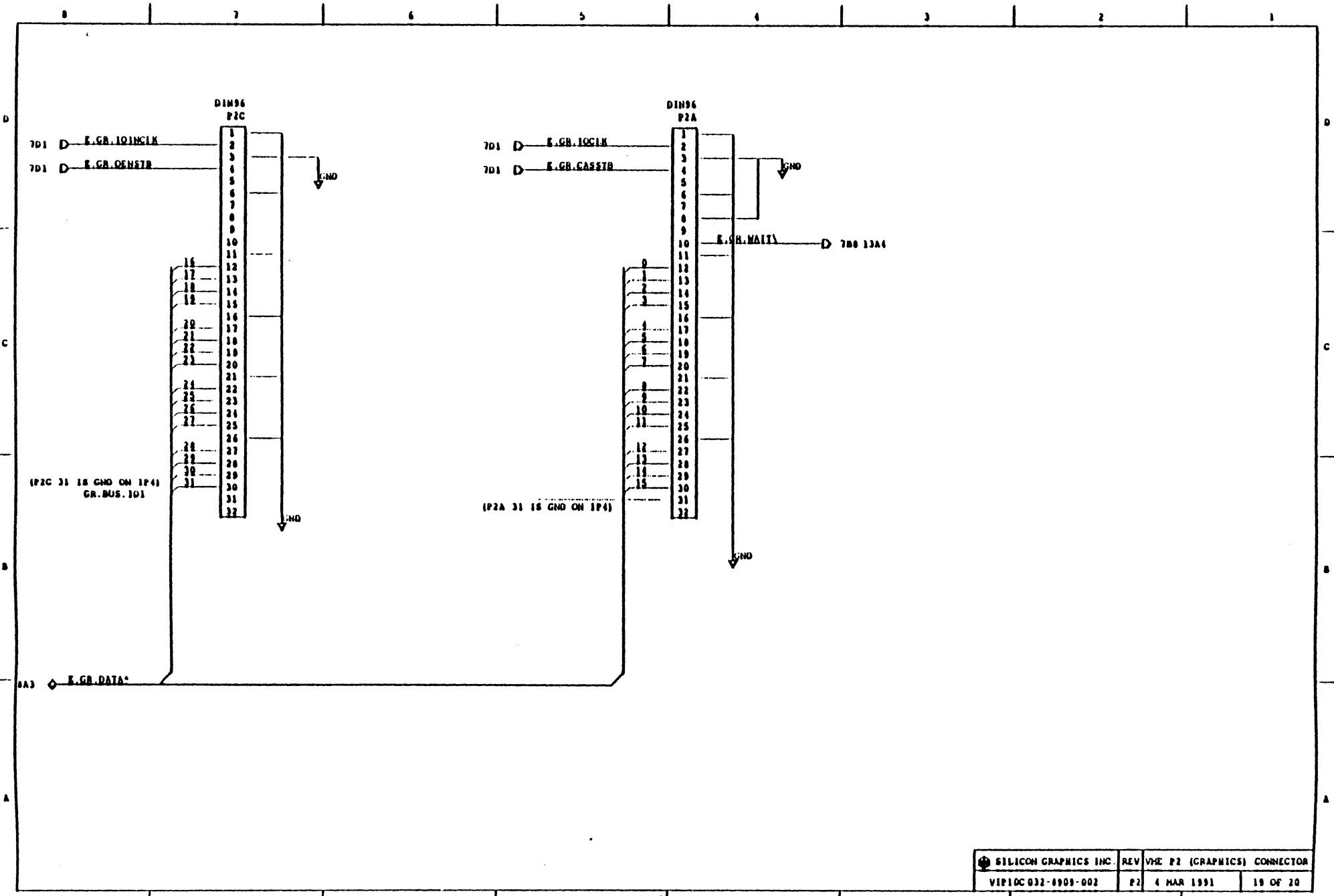
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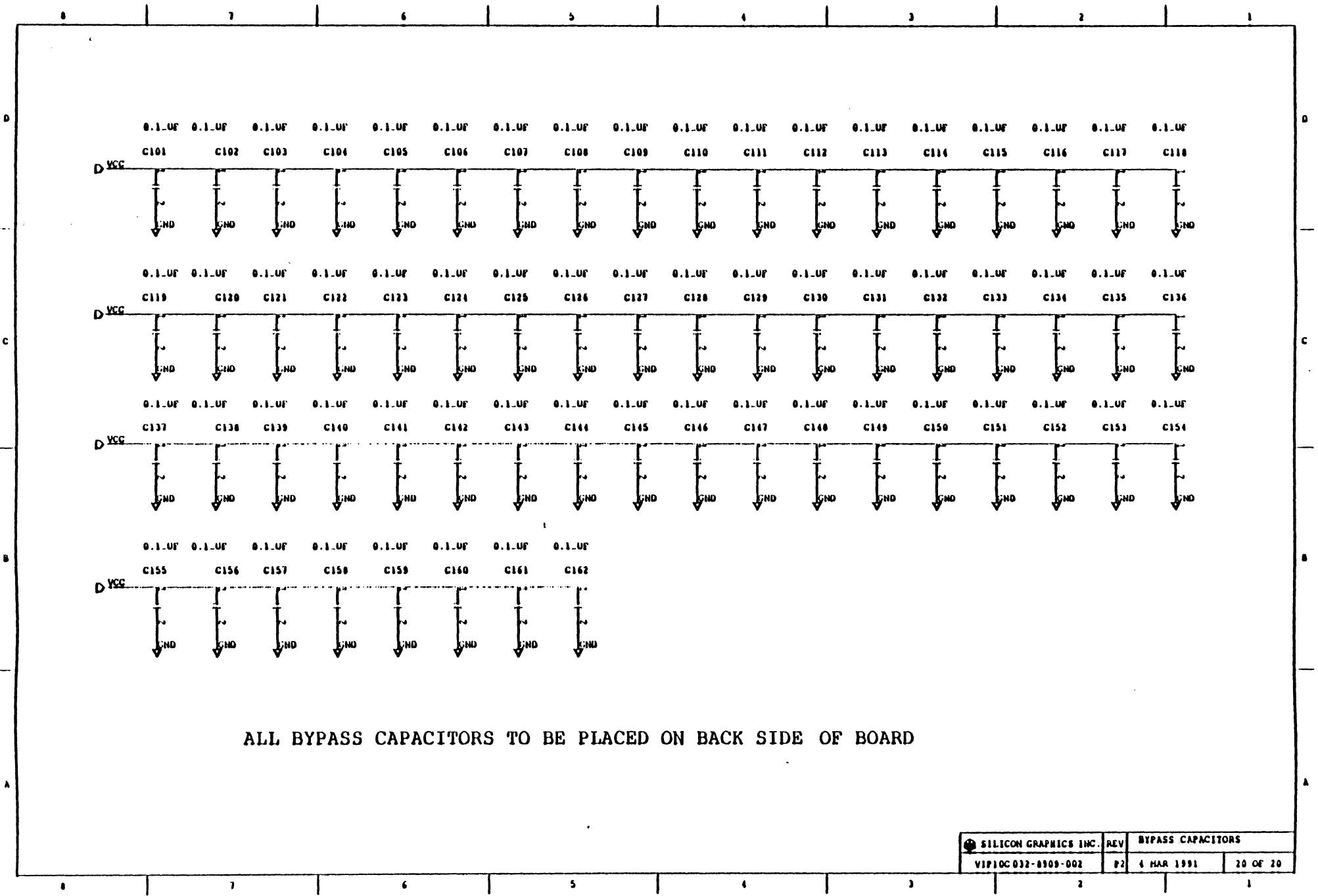












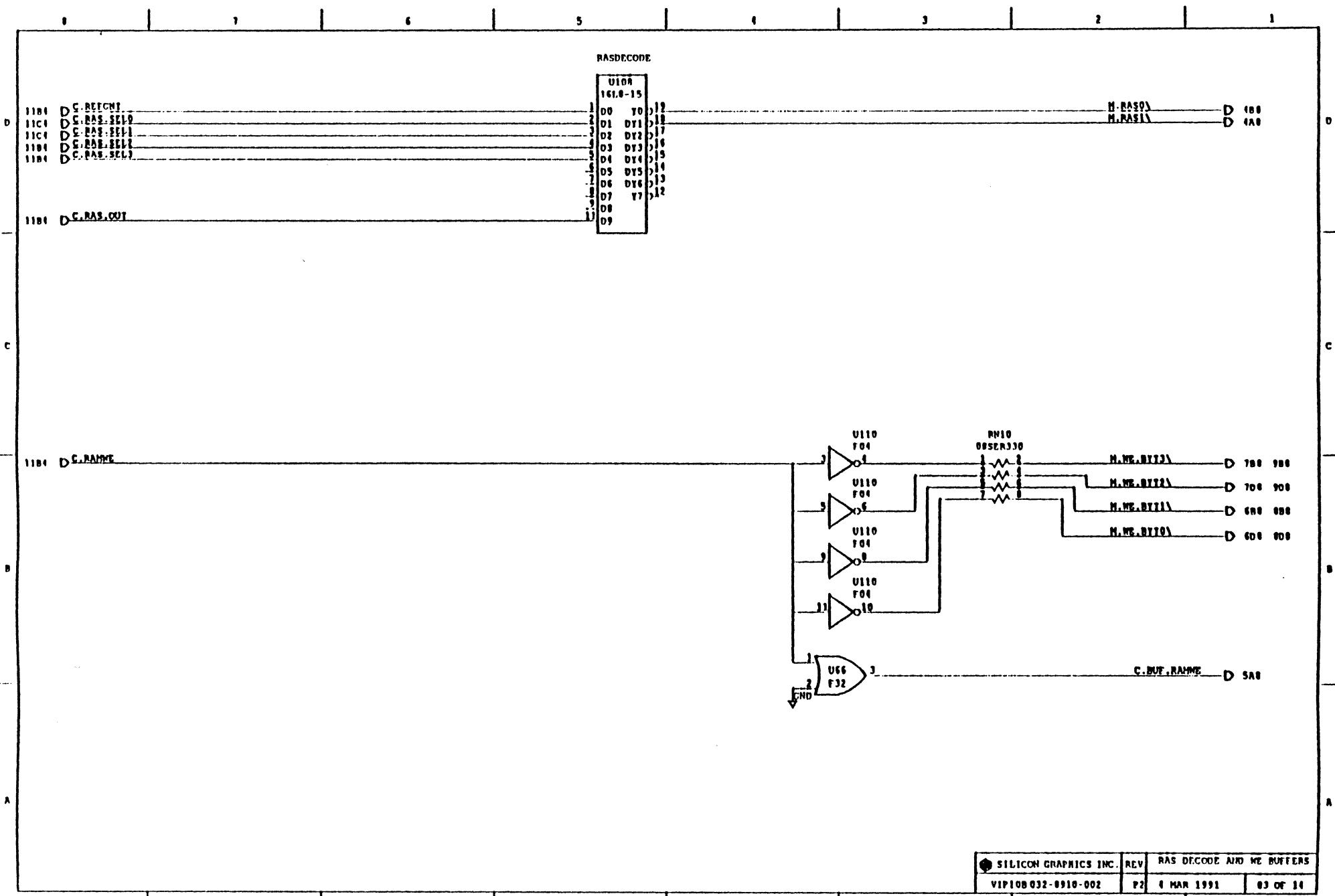
ALL BYPASS CAPACITORS TO BE PLACED ON BACK SIDE OF BOARD

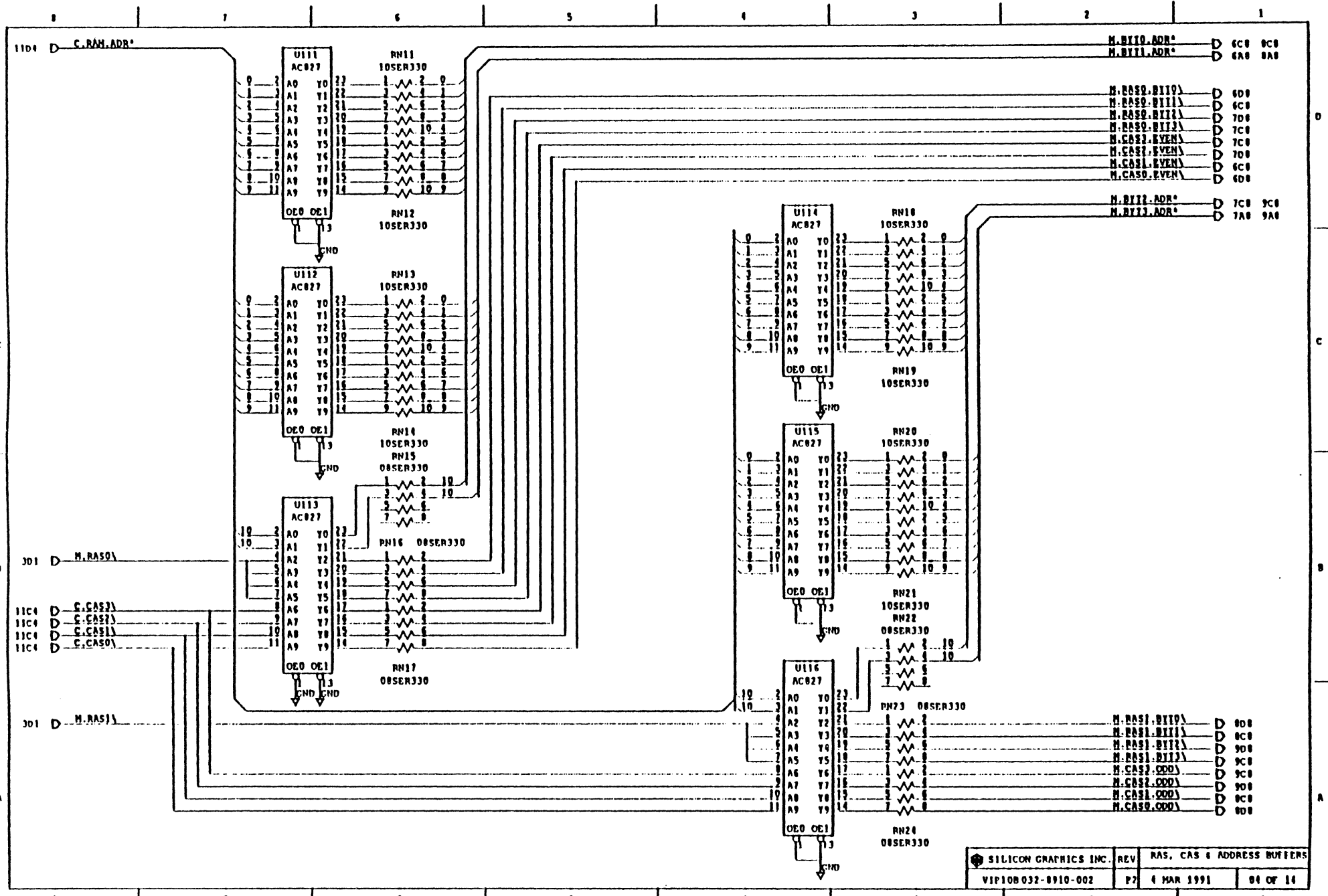
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

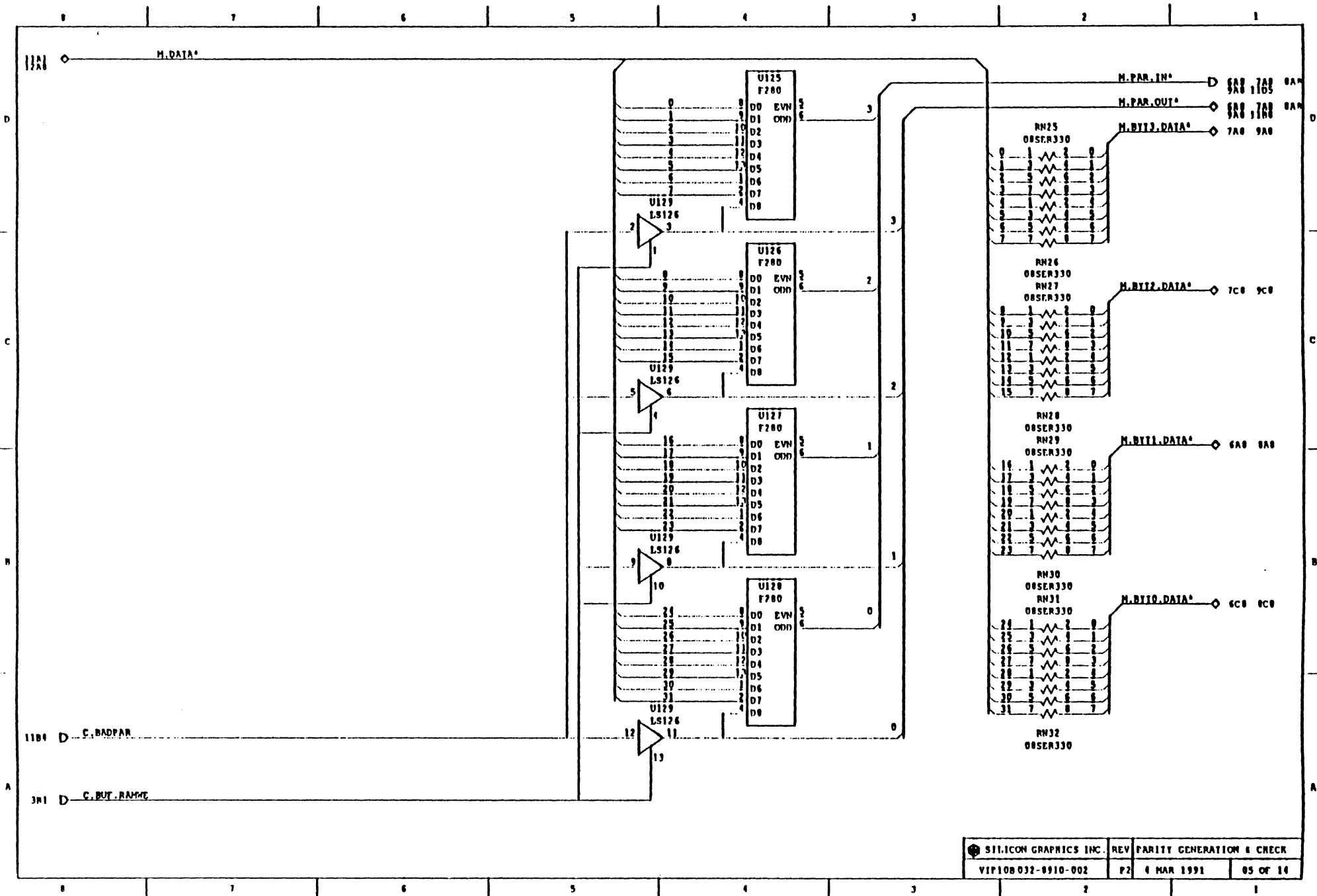
APPLICATIONS		SILICON GRAPHICS INC.	
		drw	
		chk	
		iss.	
030 8029			
NEXT ASSEMBLY	USED ON	APPROVALS	DATE
		VIP10 MEM	
		NUM.	DRAWING NUMBER
		REV	DATE
		VIP10	032-8910-002
		P2	4 MAR 1991
			1 OF 14

PAGE 1 DESCRIPTION

- 03 RAS DECODER AND WE BUFFERS
- 04 RAS, CAS AND ADDRESS BUFFERS
- 05 PARITY GENERATION AND CHECK
- 06 MEMORY BANK 0, BYTE 0,1
- 07 MEMORY BANK 0, BYTE 2,3
- 08 MEMORY BANK 1, BYTE 0,1
- 09 MEMORY BANK 1, BYTE 2,3
- 10 I/O CONNECTORS
- 11 CPU to MEMORY BOARD CONNECTION
- 12 I/O to MEMORY BOARD CONNECTION
- 13 VME P1 AND P2 CONNECTORS
- 14 BYPASS CAPACITORS





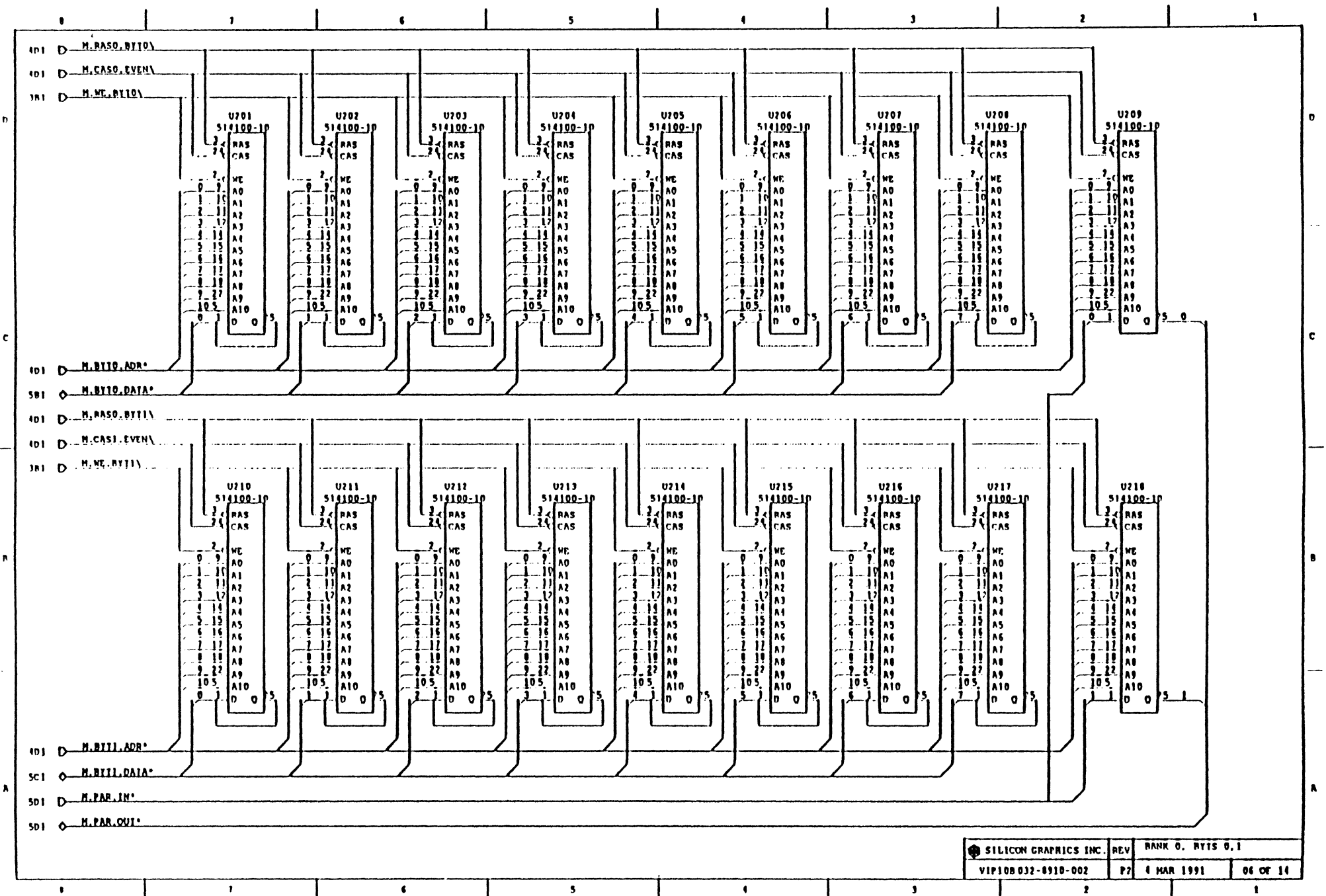


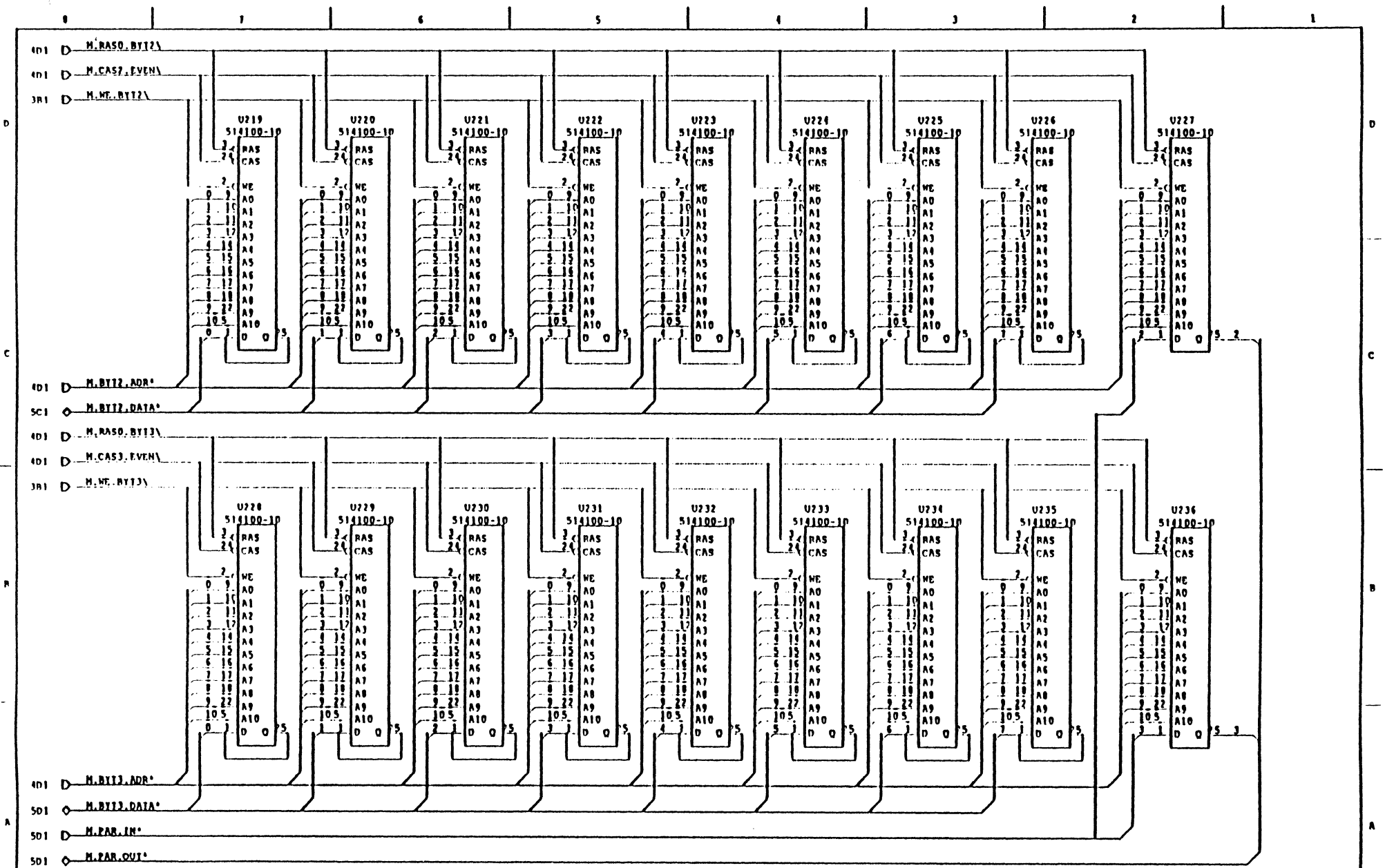
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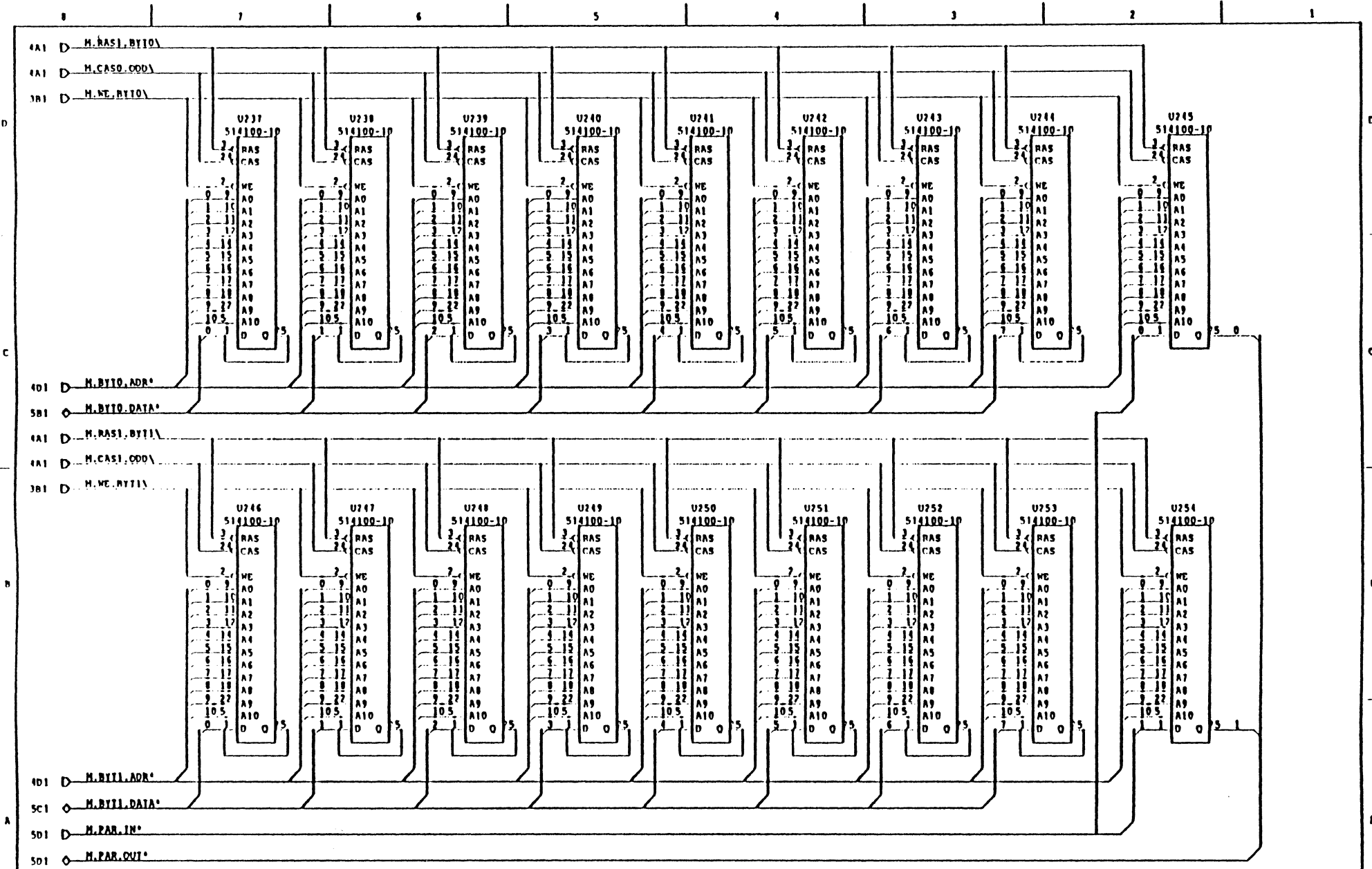
1189 C.BADPAR

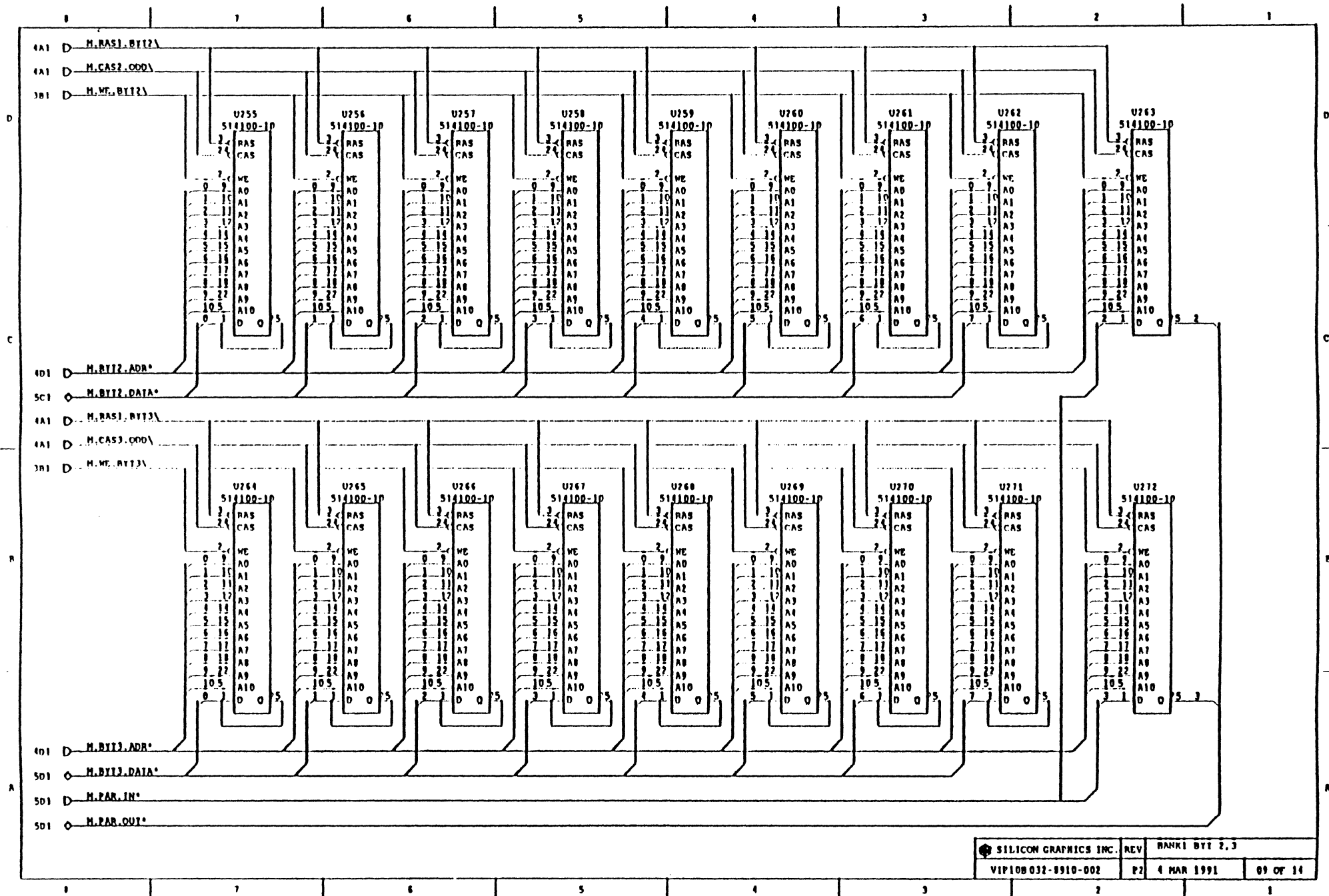
381 C.BUT.RANGE

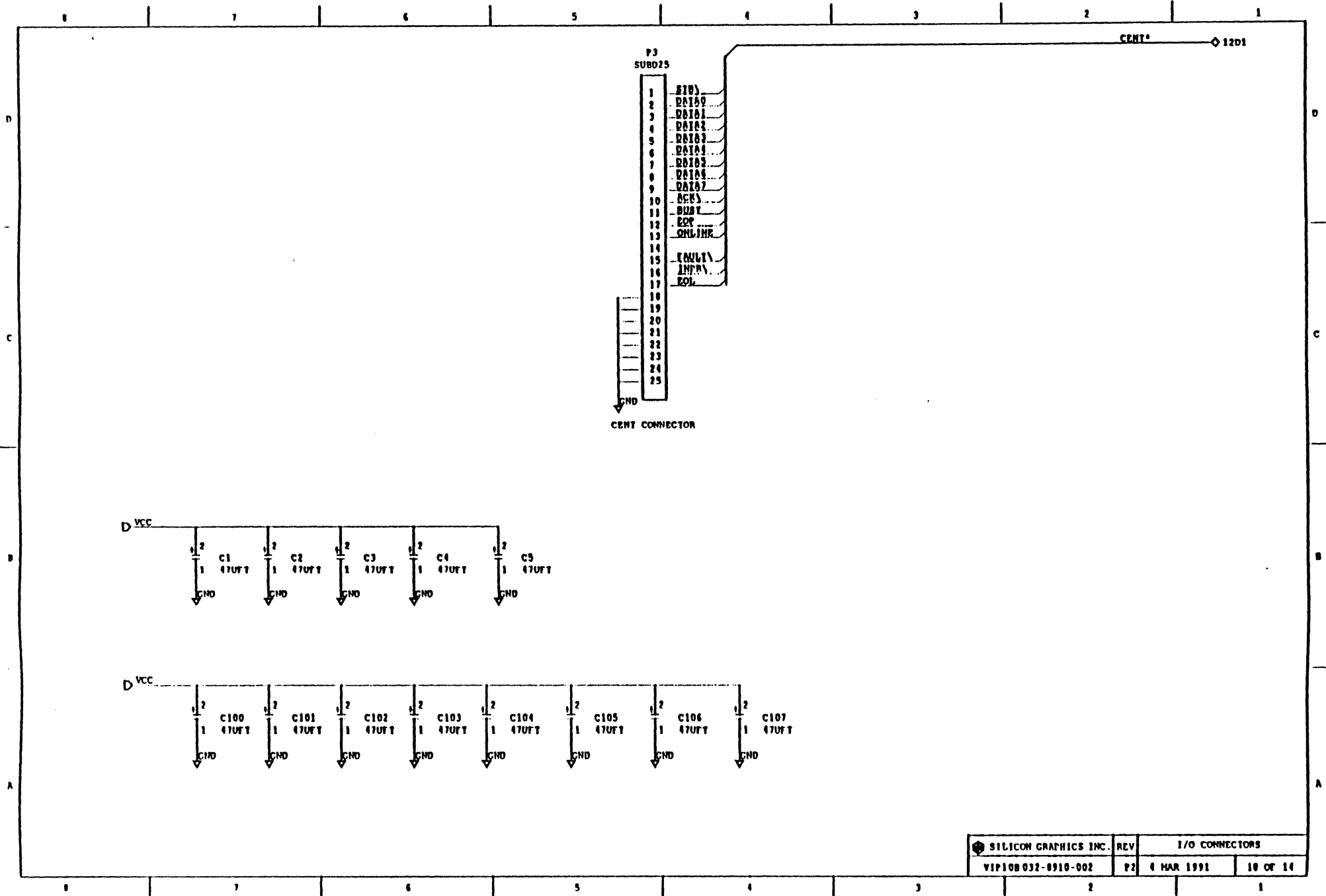
SILICON GRAPHICS INC.	REV	PARITY GENERATION & CHECK	
	P2	4 MAR 1991	05 OF 16







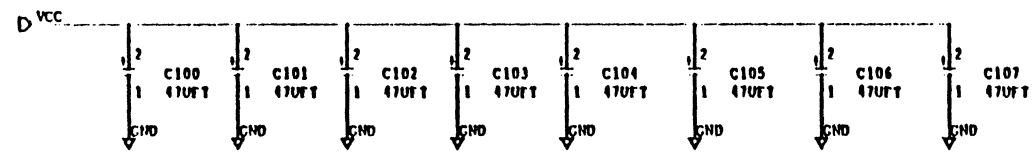
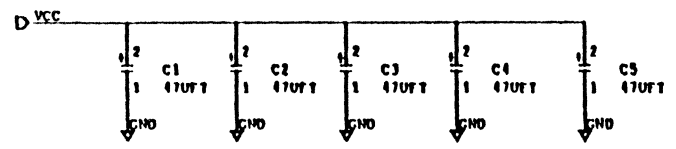


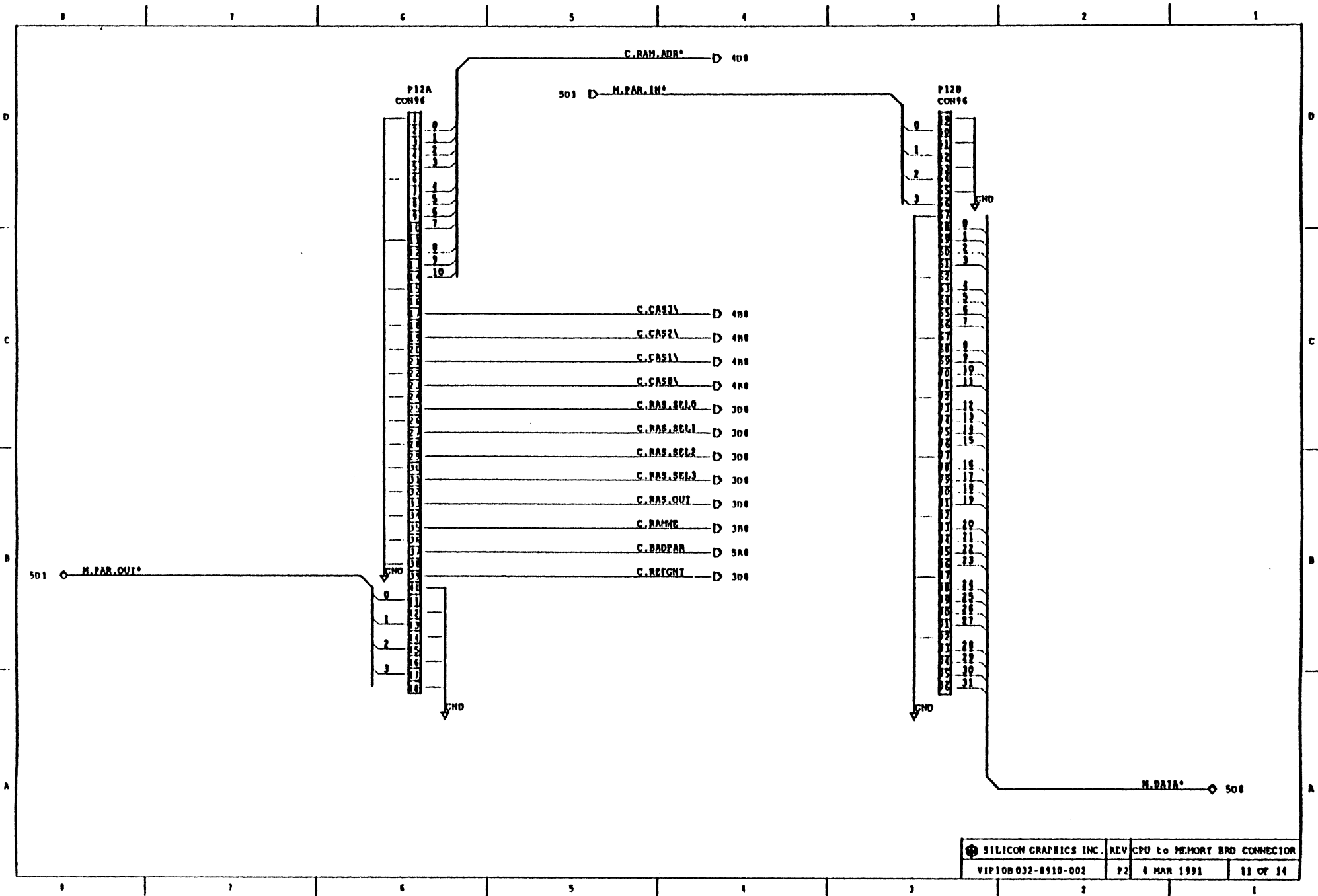


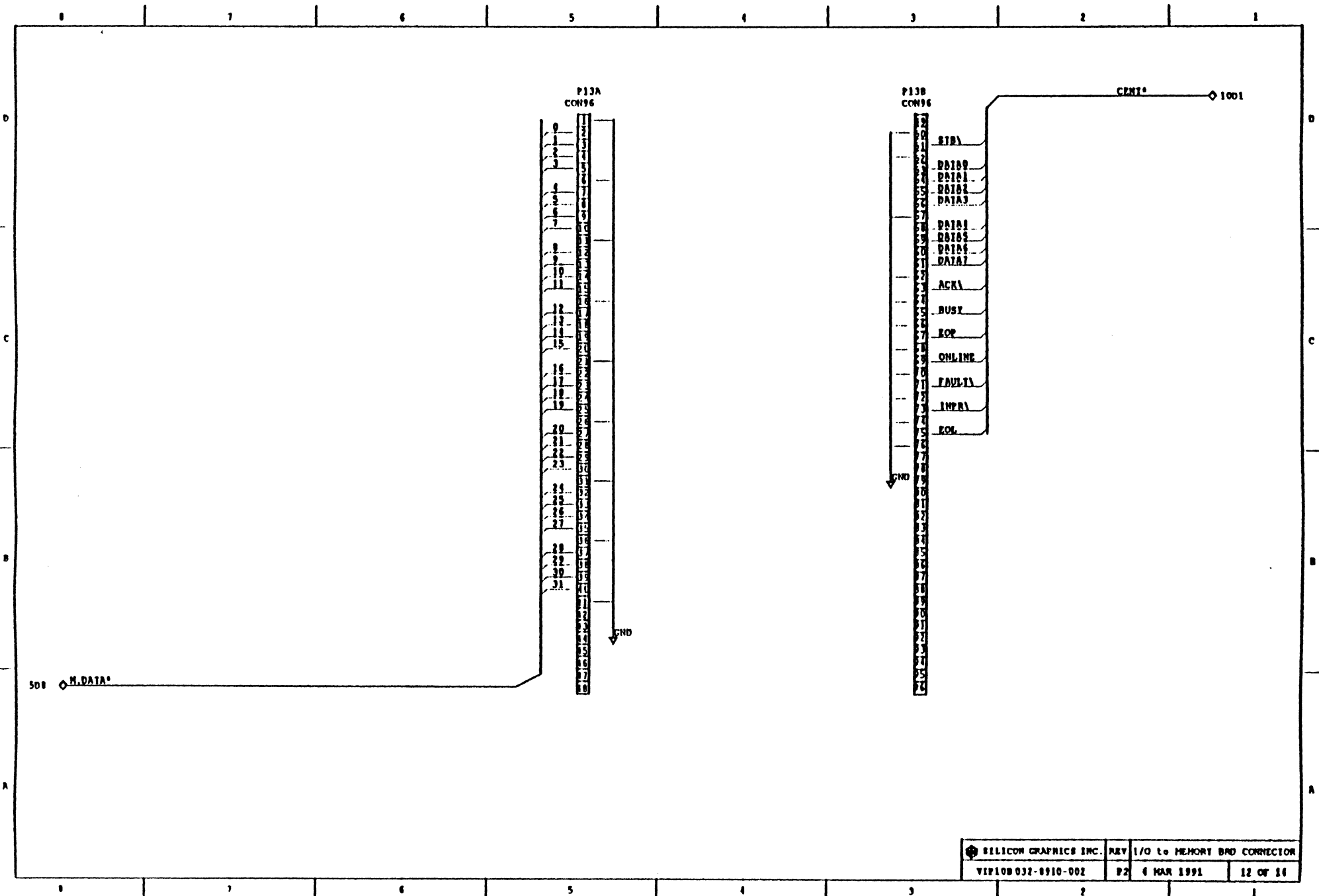
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SUBD25

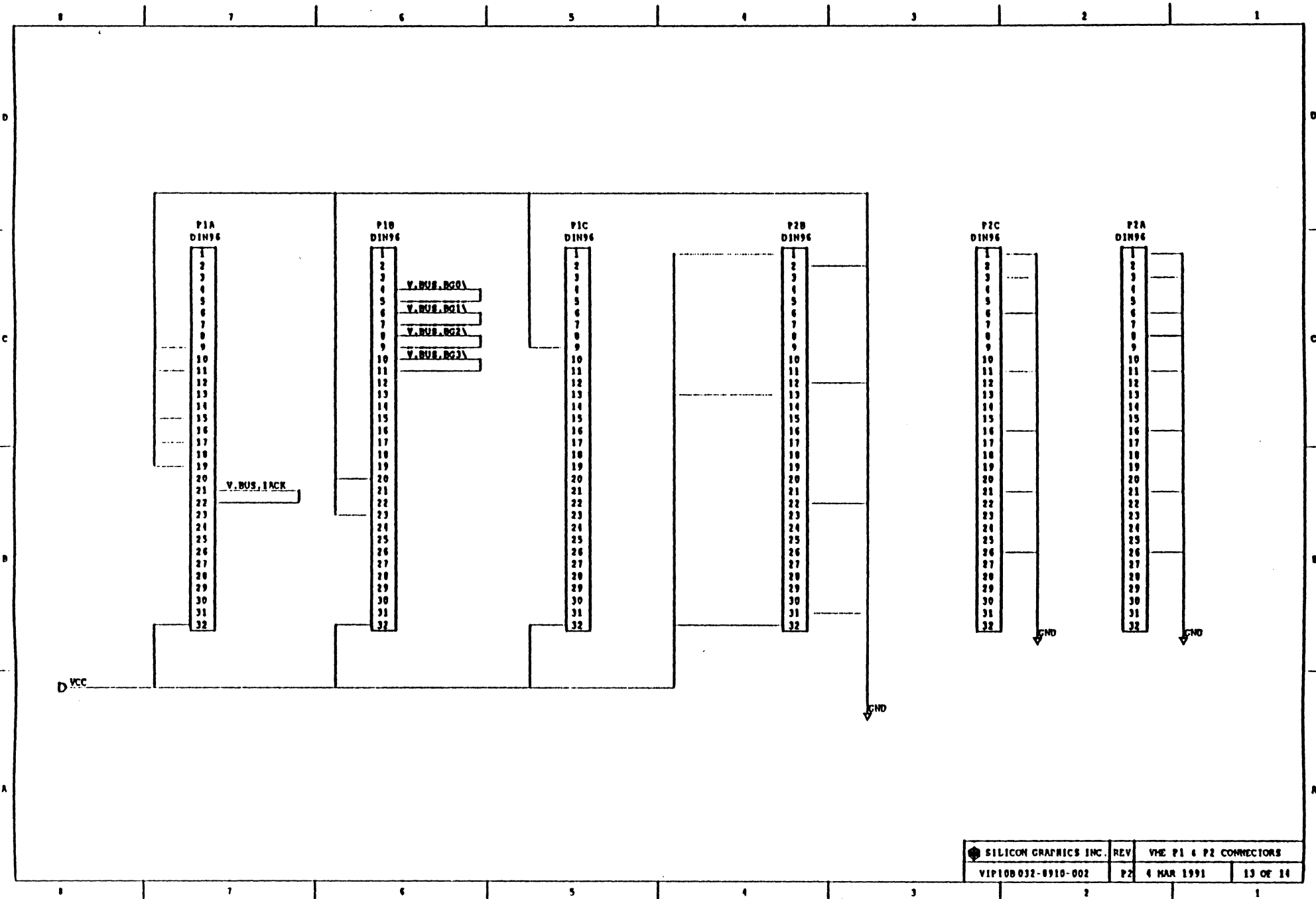
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3	DATA1
4	DATA2
5	DATA3
6	DATA4
7	DATA5
8	DATA6
9	DATA7
10	ACK
11	BUSY
12	EOP
13	ONLINE
14	FAULT
15	INTR
16	EOL
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23	
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25	

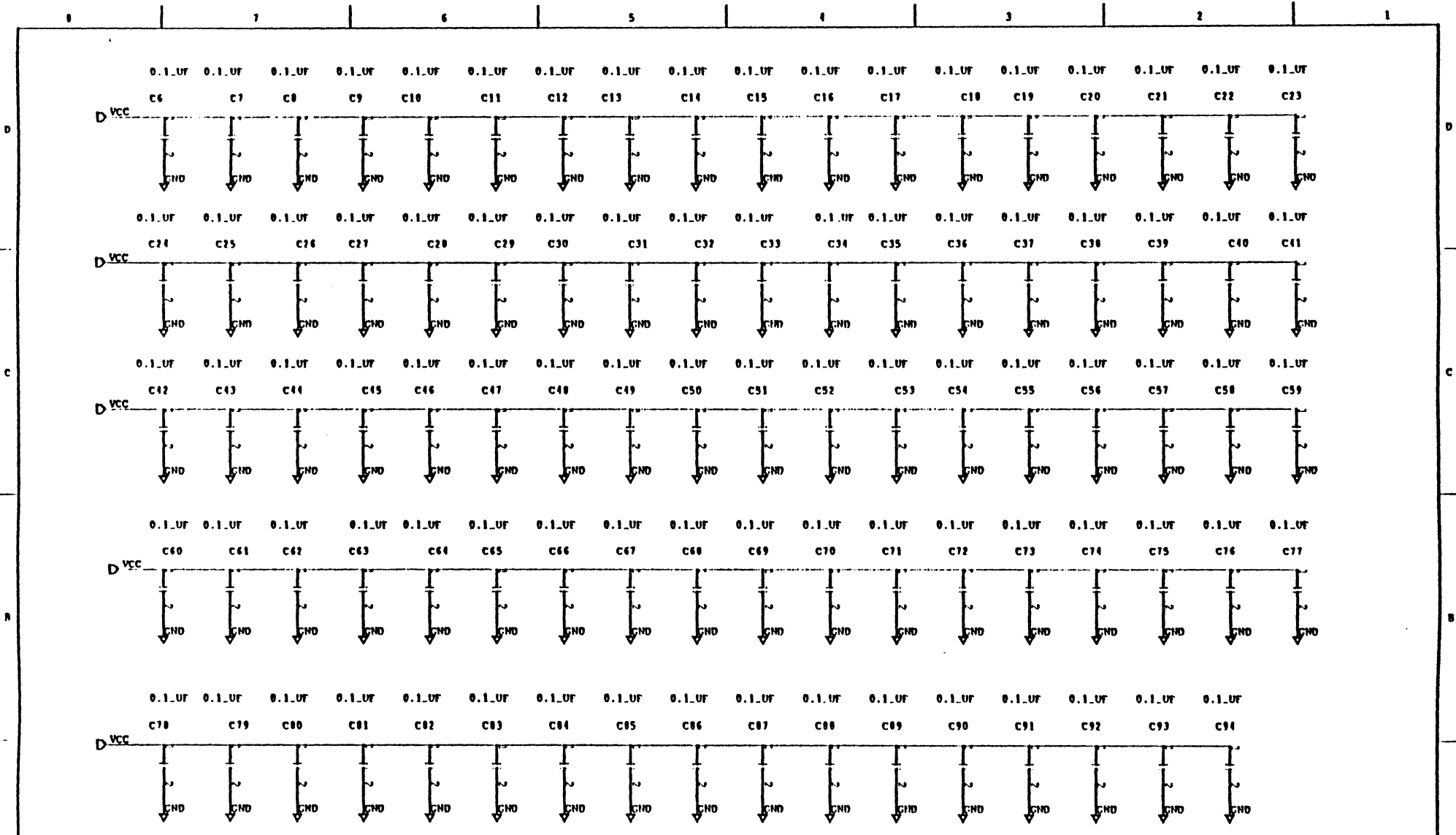
CENT CONNECTOR











ALL BYPASS CAPACITORS TO BE PLACED ON BACK SIDE OF BOARD

SILICON GRAPHICS INC.	REV	BYPASS CAPACITORS	
	P2	4 MAR 1991	11 OF 11