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PROGRAM DESCRIPTION

Page 1 of 10

Catalog No. 303014A

IDENTIFICATION: Inter-Map Verification Check Program

AUTHOR: Systems Engineering Laboratories

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PURPOSE: This program is designed to verify the proper execution of specific memory reference instructions which are located on the memory boundary between Map 2 and Map 3.

COMPUTER CONFIGURATION: SEL 810A Computer

SUBROUTINES REQUIRED: Not applicable.

STORAGE: '02470-'2515, '2773-'3005, '3470-'3505, '4000-'4504, '5000-'5372 locations.

TIMING: Not applicable.

LOADING PROCEDURE:

1. Load the program into memory by using the Standard Relocatable Loader. When loading is complete the computer will halt. The program should not be relocated.
2. Enter the starting address of the program ('05000) into the program counter.
3. Press the START switch on the console twice.
4. The program will remain in a test loop until a program halt is detected or the CPU is manually halted. The program performs all 18 tests listed in the Method section of this document.

USE: The program is designed to check the proper execution of specific memory reference instructions located on the map boundary between Map 2 and Map 3. The program also checks several skip instructions to determine if the CPU has functioned correctly.

METHOD:

1. INSTRUCTIONS

The following list shows the instructions used by the program to verify the proper execution of the CPU on the map boundary and the halt locations associated with each test.

Test No.	Halt (PC location)	Instruction
Test 1	'5022	Store B accumulator
" 2	'5040	Store A accumulator
" 3	'5051	Load A accumulator
" 4	'5063	Load B accumulator
" 5	'5076	Add memory to A
" 6	'5111	Add memory to B
" 7	'5122	Subtract memory from A accumulator
" 8	'3002	Skip A zero (A NQ zero) B accumulator equal 1
" 9	'3002	Skip A negative (A not negative) B accumulator equal 2
" 10	'3002	Skip A positive (A not positive) B accumulator equal 3
" 11	'3006	Skip A negative (A not negative) B accumulator equal 4
" 12	'3006	Skip A positive (A not positive) B accumulator equal 5
" 13	'3006	Skip A zero (A NQ zero) B accumulator equal 6
" 14	'5225	Add memory to A accumulator (Indirect) B accumulator equal 7
" 15	'5241	Subtract memory from A accumulator (Indirect) B accumulator equal 10
" 16	'3003	Increment memory and skip
" 17	'5265	B accumulator equal 11
" 17	'3474	Store place and branch B accumulator equal 12
" 18	'3003	Skip no overflow
	'5311	B accumulator equal 13

2. TEST DESCRIPTION

The program is designed to use locations '2774 thru '3004 as test locations. The program will insert the operands that are to be checked into the test locations from the main program starting at location '5000.

The primary purpose of the program is to ensure that memory reference instructions on a map boundary use the memory location within the same map as the

METHOD (CONT'D):

2. TEST DESCRIPTION (CONT'D)

instruction itself. A malfunction will be detected if the memory address accessed is in the next map instead of the map containing the instruction.

Test 1. Store B Accumulator.

The program will execute a Store B Accumulator instruction with the memory reference address in the same map as the instruction. The program location of the Store B Accumulator command is location '02777 and the memory address is '02504. The test locations are as follows:

Location	OP Code	Address	Comment
'02776	NOP		Augmented instruction.
'02777	STB	T5	T5 location is '02504
'03000	BRU*	Test	Return to main program

Halt Location.

If the CPU has functioned properly the program will proceed to Test 2, otherwise a halt will occur at location '05022. This indicates that the memory address of the Store B instruction was in location '03505 of the next map rather than in location '02504 of the map that contained the instruction.

The A accumulator contains the data from location '02504, the B accumulator contains the data from location '03504.

Test 2. Store A Accumulator.

The program will execute a Store A Accumulator instruction with the memory reference address in the same map as the instruction. The program will Store the contents of the A accumulator from location '02777. The memory address is '02504. The test locations are as follows:

Location	OP Code	Address	Comment
'02776	NOP		Augmented instruction
'02777	STA	T5	T5 location is '2504
'03000	BRU*	Test	Return to main program

Halt Condition.

If the CPU has functioned properly the program will proceed to Test 3, otherwise a halt will occur at location '05040. This indicates that the memory address of

METHOD (CONT'D):

Test 2. Store A Accumulator (Cont'd)

the Store A instruction was in location '3504 of the next map rather than in location '2504 of the map that contained the instruction.

The A accumulator contains the contents of location '2504 which should be '177777. The B accumulator contains the contents of location '3504 which should be '000000. If the data in A is '000000 and the B accumulator contains '177777 the CPU has a malfunction.

Test 3. Load A Accumulator.

The program will execute a Load A Accumulator instruction with the memory reference address in the same map as the instruction. The A accumulator should contain 177777. If the memory address was in the next map the A accumulator will contain zero's which indicate a CPU malfunction. The test locations are as follows:

Location	OP Code	Address	Comment
'02776	NOP		Augmented instruction
'02777	LAA	T1	T1 location is '2500
'03000	BRU*	Test	Return to main program

Halt Location.

If the CPU has functioned properly the program will proceed to Test 4, otherwise the program will halt at location '05051.

This indicates that the memory address of the Load A instruction was in location '3500 of the next map rather than in location '02500 of the map that contained the instruction. The A accumulator has the incorrect data.

Test 4. Load B Accumulator.

The program will execute a Load B Accumulator instruction with the memory reference address in the same map as the instruction. The B accumulator should contain '177777. If the memory address was in the next map the B accumulator will contain zeros which indicate a CPU malfunction. The test locations are as follows:

Location	OP Code	Address	Comment
'02776	NOP		Augmented instruction
'02777	LBA	T1	T1 location is '3500
'03000	BRU*	Test	Return to main program

METHOD (CONT'D):

Test 4. Load B Accumulator (Cont'd)

Halt Location.

If the CPU has functioned properly the program will proceed to Test 5, otherwise the program will halt at location '05063.

This indicates that the memory address of the Load B Accumulator instruction was in location '3500 of the next map rather than in location '2500 of the map that contained the instruction. The A accumulator has the incorrect data.

Test 5. Add Memory to A Accumulator.

The program will execute an Add Memory to A Accumulator instruction with the memory reference address in the same map as the instruction. The A accumulator should contain '177777. If the memory address was from the next map the A accumulator will contain '077777.

Halt Location.

If the CPU has functioned properly the program will proceed to Test 6, otherwise the program will halt at location '05076. This indicates that the memory address of the Add Memory to A accumulator was in location '03502 of the next map rather than in location '02502 of the map that contained the instruction. The test locations are as follows:

Location	OP Code	Address	Comment
'02776	NOP		Augmented instruction T3 EQ T1 000001
'02777	AMA	T3	
'03000	BRU*	Test	

Test 6. Add Memory to B Accumulator.

The program will execute an Add Memory to B Accumulator instruction with the memory address in the same map as the instruction. The B accumulator after execution of the instruction should contain '177777. If the memory address was in the next map, the B accumulator will contain '077777 indicating a malfunction in the CPU. The test locations are as follows:

Location	OP Code	Address	Comment
02776	NOP		Augmented instruction T3 EQ 000001 Return
02777	AMB	T3	
03000	BRU*	Test	

METHOD (CONT'D):

Test 6. Add Memory to B Accumulator (cont'd).

Halt Location.

If the CPU has functioned properly, the program will proceed to Test 7, otherwise a halt will occur at location '05111. The A accumulator will contain the incorrect data.

Test 7. Subtract Memory from A Accumulator.

The program will execute Subtract Memory from A Accumulator instruction with the memory address in the same map as the instruction. The test locations are as follows:

Location	OP Code	Address	Comment
'02776	NOP		A contains 177777
'02777	SMA	T4	T4 EQ to '100000
'03000	BRU*	Test	Return

Halt Location.

If the CPU has functioned properly the program will proceed to Test 8, otherwise a halt will occur at location '05122. The A accumulator will display the incorrect data value of '177777. The correct data value is '077777.

Test 8. Skip A Zero.

The augmented instruction SAZ will be executed from location '02776. The data in the A accumulator is not equal to zero, therefore the program should not cross the map boundary.

Halt Locations.

If the CPU has functioned properly the program will proceed to Test 9, otherwise a halt will occur at location '03002. This indicates that the CPU has crossed the map boundary which is an error. The B accumulator will contain '000001 indicating the error number.

Test 9. Skip A Negative.

The augmented instruction SAN will be executed from location '02776. The data in the A accumulator is not negative, therefore the program should not cross the map boundary.

METHOD (CONT'D):

Test 9. Skip A Negative (cont'd).

Halt Locations.

If the CPU has functioned properly the program will proceed to Test 10, otherwise a halt will occur at location '03002. This indicates that the CPU has crossed the map boundary which is an error. The B accumulator will contain '000002 indicating the error number.

Test 10. Skip A Positive.

The augmented instruction SAP will be executed from location '02776. The data in the A accumulator is not positive, therefore the program should not cross the map boundary.

Halt Location.

If the CPU has functioned properly the program will proceed to Test 11, otherwise a halt will occur at location '03002. This indicates that the CPU has crossed the map boundary which is an error. The B accumulator will contain '000003 indicating the error number.

Test 11. Skip A Negative.

The augmented instruction SAN will be executed from location '02777. The data in the A accumulator will be a positive number, therefore the program will cross the map boundary to the first location of the next map.

Halt Location.

If the CPU has functioned properly the program will proceed to Test 12, otherwise a halt will occur at location '03006. This indicates that the CPU has crossed the map boundary but skipped incorrectly. The B accumulator will contain '000004 indicating the error number.

Test 12. Skip A Positive.

The augmented instruction SAP will be executed from location '02777. The data in the A accumulator will be negative, therefore the program will cross the map boundary and execute the first instruction of the next map.

Halt Location.

If the CPU has functioned properly the program will proceed to Test 13, otherwise a halt will occur at location '03006. This indicates that the CPU has skipped on A positive when the data in A was negative. The B accumulator will contain '000005 indicating the error number.

METHOD (CONT'D):

Test 13. Skip A Zero.

The augmented instruction SAZ will be executed from location '027777. The data in the A accumulator will not be zero, therefore the program will cross the map boundary and execute the first instruction of the next map.

Halt Location.

If the CPU has functioned properly the program will proceed to Test 14, otherwise a halt will occur at location '03006. This indicates that the CPU has skipped on A zero when the data in A was positive. The B accumulator will contain 000006 indicating the error number.

Test 14. Add Memory to A (Indirect)

The program will execute an Add Memory to A Accumulator instruction with the indirect-bit set. The memory address will be indirect thru the map which contains the instruction. When the command has been executed the value in A should be '177777. If the memory address was in the next map the value in A will be '100000. The test locations are as follows:

Location	OP Code	Address	Comment
'02776	NOP		Augmented instruction
'02777	AMA*	T2	A EQ 177777
'03000	BRU*	Test	Return

Halt Location.

If the CPU has functioned properly the program will proceed to Test 15, otherwise a halt will occur at location '05225. The operator may visually observe the contents of A accumulator. The data value should be '177777. Any other value indicates an error. The B accumulator will contain 000007 indicating the error number.

Test 15. Subtract Memory from A (Indirect).

The program will execute a Subtract Memory from A Indirect instruction with the indirect address in the same map as the instruction. When the command has been executed, the data in the A accumulator should be '077777. If the memory address was in the next map the value will be '177777. The test locations are as follows:

Location	OP Code	Address	Comment
'02776	FRA		A EQ 177777
'02777	SMA*	T4	T4 EQ 100000
'03000	BRU*	Test	Return

METHOD (CONT'D):

Test 15. Subtract Memory from A (Indirect) (cont'd)

Halt Location.

If the CPU has functioned properly the program will proceed to Test 16, otherwise a halt will occur at location '05241. The operator may visually observe the contents of the A accumulator. The data should be '077777. Any other data indicates an error. The B accumulator will contain 000010 indicating the error number.

Test 16. Increment Memory and Skip.

The program will execute an Increment Memory and Skip instruction with the memory address in the same map as the instruction. The A accumulator after execution of the instruction should contain 000000. If the memory address was in the next map, the data in A will be 000001. The test locations are as follows:

Location	OP Code	Address	Comment
'02776	NOP		Augmented Code
'03000	IMS	T6	T6 EQ 177777
'03001	HLT		
'03002	BRU*		

Halt Location.

If the CPU has functioned properly the program will proceed to test 17, otherwise a halt will occur at location '03003 or '05265. The B accumulator contains the error number count which is equal to 000011. The halt at '03003 indicates that the IMS instruction didnot skip properly. The halt at '05265 indicates that the incremented memory address was in the next map rather than in the same map as the instruction.

Test 17. Store Place and Branch.

The program will execute a Store Place and Branch instruction with the branch location in the same map as the SPB instruction. The subroutine in the same map will clear the A accumulator indicating that the subroutine was entered. The test locations are as follows:

Location	OP Code	Address	Comment
'02776	NOP		Augmented instruction
'02777	SPB	THMP	location is 2470
'03000	BRU*	Test	Return

METHOD (CONT'D):

Test 17. Store Place and Branch (cont'd).

Halt Location.

If the CPU has functioned properly the program will proceed to Test 18, otherwise a halt will occur at location '03474. The operator may visually observe the contents of the A accumulator. The data value should be 177777, which indicates an error. The B accumulator should have a value of 000012. This verifies that the SPB test is the one which caused the failure.

Test 18. Skip No Overflow Test.

The program will execute a Skip No Overflow instruction. The skip instruction crosses an intermap boundary. The overflow latch is not set. The test locations are as follows:

Location	OP Code	Address	Comment
02776	SOF		Overflow not set
02777	HLT		Incorrect skip
03000	BRU*	Test	Return

Halt Location.

If the CPU has functioned properly, the progra will reset all counters and begin with Test 1, otherwise the program will halt at location '3003 or '05311. The B accumulator should contain a value of 000013. The halt at location '03003 indicates that the SOF didnt skip properly to the next map.

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0001 00000 00000000 *** INTER-MAP VERIFICATION CHECK PROGRAM 810A 303014A
0002 00000 00000000 *** J.B. BOYER AUG 30, 1967
0003 02470 60002470 ORG '2470
0004 02470A00000000 THMP ZZZ THIS MAP
0005 02471 00000033 NBP
0006 02472 00000003 CLA
0007 02473 11202470 BRU* THMP
0008 02500 60002500 ORG '2500
0009 02500 00177777 T1 DATA '177777
0010 02501 00077777 T2 DATA '077777
0011 02502 00000001 T3 DATA '000001
0012 02503 00100000 T4 DATA '100000
0013 02504 00000000 T5 DATA 0
0014 02505 00000000 T6 DATA 0 SAME MAP
0015 02506 14002505 IMS IMS T6
0016 02507 05202510 AMAA AMA* T6D
0017 02510 25402502 T6D DAC T3
0018 02511 06202512 SMAA SMA* T7D
0019 02512 25402503 T7D DAC T4
0020 02513 12002470 SPB SPB THMP
0021 02514 11002515 BRUB BRU T7
0022 02515 11202773 T7 BRU* TEST
0023 02773 60002773 ORG '2773
0024 02773 00000000 TEST ZZZ **
0025 02774 00000033 NBP LOCATION 2774
0026 02775 00000033 NBP LOCATION 2775
0027 02776 00000033 NBP LOCATION 2776
0028 02777 00000033 NBP LOCATION 2777
0029 03000 00000033 NBP LOCATION 3000
0030 03001 00000033 NBP LOCATION 3001
0031 03002 00000033 NBP LOCATION 3002
0032 03003 00000033 NBP LOCATION 3003
0033 03004 00000033 NBP LOCATION 3004
0034 03005 00000000 *
0035 03005 11202773 BRU* TEST
0036 03006 11202773 BRUA BRU* TEST
0037 03007 00002777 TES1 EQU TEST+4
0038 03470 60003470 ORG '3470
0039 03470A00000000 NTMP ZZZ NEXT MAP IF PROGRAM COUNTER ADVANCED

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0040	03471	00000033		NØP	
0041	03472	00000000		HLT	INDICATES INCØRRECT BRANCH
0042	03473	11203470		BRU* NTMP	
0043	03500	60003500		ØRG '3500	
0044	03500	00000000	TA	DATA 0	
0045	03501	00000000	TB	DATA 0	
0046	03502	00000000	TC	DATA 0	
0047	03503	00000000	TD	DATA 0	
0048	03504	00000000	TE	DATA 0	
0049	03505	EQ00000000	TF	DATA	NEXT MAP
0050	04000	60004000		ØRG '4000	
0051	04000	01004500	LAA	LAA T1D	T1D EQ 177777
0052	04001	02004500	LBA	LBA T1D	
0053	04002	05004502	AMA	AMA T3D	T3D EQ 000001
0054	04003	16004502	AMB	AMB T3D	T3D EQ 000001
0055	04004	06004503	SMA	SMA T4D	T4D EQ 100000
0056	04005	04004504	STB	STB T5D	
0057	04006	03004504	STA	STA T5D	T5D EQ 0
0058	04007	00000022	SAZA	SAZ	
0059	04010	00000024	SAP	SAP	
0060	04011	00000023	SAN	SAN	
0061	04012	00001712	FRA	FRA 15	
0062	04013	00001716	LSL	LSL 15	
0063	04014	00000025	SØF	SØF	
0064	04015	25405372	LC04	DAC L304+1	
0065	04016	25405365	LC00	DAC L300	
0066	04500	60004500		ØRG '4500	
0067	04500	00177777	T1D	DATA '177777	
0068	04501	00077777	T2D	DATA '077777	
0069	04502	00000001	T3D	DATA '000001	
0070	04503	00100000	T4D	DATA '100000	
0071	04504	00000000	T5D	DATA '0	
0072	05000	60005000		ØRG '5000	
0073	05000	12005335	TAR	SPB SIBS	
0074	05001	00000000	****S		STØRE B INSTRUCTION
0075	05001	00000003	CLA		
0076	05002	03005332	STA	CNT	CØUNTER
0077	05003	01004005	LAA	STB	STB INSTRUCTION
0078	05004	03002777	STA	TES1	STØRED INTØ TEST LØCATION
0079	05005	00000003	CLA		

0080	05006	03002504	STA	T5	LOCATION IN SAME MAP AS STR
0081	05007	03003504	STA	TE	LOCATION IN NEXT MAP
0082	05010	14005332	IMS	CNT	COUNTER
0083	05011	02002500	LBA	T1	T1 EQ TO 177777
0084	05012	12002773	SPB	TEST	TEST SUBROUTINE
0085	05013	01002504	LAA	T5	T5 IS IN SAME MAP AS STB
0086	05014	15002500	CMA	T1	T1 EQ 177777
0087	05015	11005017	BRU	**2	NO
0088	05016	11005021	BRU	0T	YES GO TO NEXT TEST
0089	05017	02003504	LBA	TE	GET VALUE INTO B
0090	05020	00000000	HLT		A CONTAINS DATA OF SAME MAP LOCATION
0091	05021	00000000	*		B CONTAINS DATA OF NEXT MAP LOCATION
0092	05021	00000000	*		CORRECT DATA VALUE SHOULD BE 177777
0093	05021	01004006	0T	LAA	STORE A INSTRUCTION
0094	05022	03002777		STA	TES1
0095	05023	00000000	*****		CHECK STORE A INSTRUCTION
0096	05023	00000003		CLA	
0097	05024	03002504	STA	T5	SAME MAP AS STA
0098	05025	03003504	STA	TE	NEXT MAP
0099	05026	14005332	IMS	CNT	COUNTER INCREMENTED
0100	05027	01002500	LAA	T1	T1 EQ TO 177777
0101	05030	12002773	SPB	TEST	
0102	05031	01002504	LAA	T5	CHECK SAME MAP FOR DATA
0103	05032	15002500	CMA	T1	T1 EQ 177777
0104	05033	11005035	BRU	**2	
0105	05034	11005037	BRU	0A	
0106	05035	02003504	LBA	TE	
0107	05036	00000000	HLT		A CONTAINS VALUE FROM SAME MAP AS STA
0108	05037	00000000	****		B CONTAINS DATA FROM NEXT MAP
0109	05037	00000033	0A	NOP	
0110	05040	01004000	LAA	LAA	
0111	05041	03002777	STA	TES1	LAA SET TO LOAD FROM SAME MAP
0112	05042	14005332	IMS	CNT	COUNTER
0113	05043	00000003	CLA		
0114	05044	03003504	STA	TE	
0115	05045	12002773	SPB	TEST	TEST SUBROUTINE
0116	05046	00000023	SAN		
0117	05047	00000000	HLT		
0118	05050	14005332	IMS	CNT	COUNTER INCREMENTED
0119	05051	01004001	LAA	LBA	LBA CHECK

0120	05052	03002777	STA	TES1	SET TEST LOCATION TO LRA INSTRUCTION
0121	05053	00000003	CLA		SET A+B TO ZERO
0122	05054	03003504	STA	TE	
0123	05055	00000005	TAB		
0124	05056	12002773	SPB	TEST	TEST SUBROUTINE
0125	05057	00000004	TBA		
0126	05060	00000023	SAN		CHECK A FOR NEGATIVE VALUE
0127	05061	00000000	HLT		
0128	05062	00000000	*****		CHECK ADD MEMORY TO A
0129	05062	01004002	LAA	AMA	
0130	05063	03002777	STA	TES1	STORE AMA INSTRUCTION INTO TEST LOCATION
0131	05064	14005332	IMS	CNT	COUNTER FOR INSTRUCTION
0132	05065	01002501	LAA	T2	T2 EQUAL TO 077777
0133	05066	12002773	SPB	TEST	TEST
0134	05067	00000025	SOF		
0135	05070	11005071	BRU	**1	TURN OFF OVERFLOW
0136	05071	15002503	CMA	T4	T4 EQ 100000
0137	05072	11005074	BRU	**2	
0138	05073	11005075	BRU	**2	
0139	05074	00000000	HLT		VALUE OF INCORRECT DATA IS IN A ACCUMULATOR
0140	05075	00000000	*****		CHECK ADD MEMORY TO B
0141	05075	14005332	IMS	CNT	COUNTER
0142	05076	01004003	LAA	AMB	AMB INSTRUCTION USES T3 EQ TO
0143	05077	03002777	STA	TES1	STORE AMB INSTRUCTION INTO TEST LOCATION
0144	05100	00000003	CLA		
0145	05101	02002501	LBA	T2	T2 VALUE IS 077777
0146	05102	12002773	SPB	TEST	TEST ROUTINE
0147	05103	00000004	TBA		
0148	05104	15002503	CMA	T4	T4 EQ TO 100000
0149	05105	11005107	BRU	**2	
0150	05106	11005110	BRU	**2	
0151	05107	00000000	HLT		
0152	05110	00000000	*****		CHECK SMA INSTRUCTION
0153	05110	01004004	LAA	SMA	SMA USES T4 EQ TO 100000
0154	05111	03002777	STA	TES1	STORE SMA INTO TEST LOCATION
0155	05112	14005332	IMS	CNT	
0156	05113	01002500	LAA	T1	T1 VALUE IS 177777
0157	05114	12002773	SPB	TEST	TEST SUBROUTINE
0158	05115	15002501	CMA	T2	T2 VALUE IS 077777
0159	05116	11005120	BRU	**2	

0160	05117	11005121	BRU	**2	
0161	05120	00000000	HLT		A CONTAINS INCORRECT VALUE SHOULD BE 077777
0162	05121	00000000	****		SAZ TEST A ACCUMULATOR NOT EQ ZERO
0163	05121	00000000	*		SHOULD NOT CROSS MAP BOUNDARY LAST LOCATION OF
0164	05121	00000000	*		TEST MAP HAS A BRU* TEST WHICH SHOULD RETURN TO
0165	05121	00000000	*		MAIN PROGRAM
0166	05121	00000000	*		B ACC CONTAINS ERROR NUMBER
0167	05121	01005334	LAA	HLT	
0168	05122	03205365	STA*	L300	TEST LOCATION
0169	05123	14005332	IMS	CNT	INCREMENT COUNTER
0170	05124	00000003	CLA		
0171	05125	00000005	TAB		
0172	05126	03005333	STA	STBT	STBT WILL BE TEMPORARY STORAGE FOR COUNTER
0173	05127	03005372	STA	L304+1	TEST LOCATION
0174	05130	01004007	LAA	SAZA	
0175	05131	03205363	STA*	L276	TEST LOCATION
0176	05132	01003006	LAA	BRUA	
0177	05133	03205364	STA*	L277	TEST LOCATION
0178	05134	00000026	IBS		INCREMENT COUNTER
0179	05135	00000033	NOP		
0180	05136	04005333	STB	STBT	SAVE ERROR COUNTER
0181	05137	12002773	SPB	TEST	
0182	05140	14005332	IMS	CNT	
0183	05141	00000000	****		SAN TEST A ACCUMULATOR EQ POSITIVE NUMBER
0184	05141	00000000	*		WHICH IS THE AUGMENTED INSTRUCTION
0185	05141	12005353	SPB	BUPD	INCREMENT B SUBROUTINE
0186	05142	01004011	LAA	SAN	
0187	05143	03205363	STA*	L276	TEST LOCATION
0188	05144	12002773	SPB	TEST	TEST SUBROUTINE
0189	05145	00000000	****		SAP TEST A ACCUMULATOR EQ NEGATIVE NUMBER
0190	05145	14005332	IMS	CNT	INCREMENT COUNTER
0191	05146	12005353	SPB	BUPD	INCREMENT B SUBROUTINE
0192	05147	01004010	LAA	SAP	SAP SET TO TEST LOCATION
0193	05150	03205363	STA*	L276	TEST LOCATION
0194	05151	01004503	LAA	T4D	T4D EQ 100000
0195	05152	12002773	SPB	TEST	TEST SUBROUTINE
0196	05153	01005331	LAA	SAZ	
0197	05154	03205365	STA*	L300	
0198	05155	01003006	LAA	BRUA	TEST LOCATION
0199	05156	03205372	STA*	L304+1	

0200	05157	12005335	SPB	STBS	RESET COUNTERS
0201	05160	01004011	LAA	SAN	
0202	05161	03205364	STA*	L277	TEST LOCATION
0203	05162	01003006	LAA	BRUA	
0204	05163	03205365	STA*	L300	NEXT MAP
0205	05164	01005334	LAA	HLT	HALT
0206	05165	03205371	STA*	L304	HALT SHOULD OCCUR
0207	05166	12005353	SPB	BUPD	INCREMENT COUNTER SUBROUTINE
0208	05167	01004011	LAA	SAN	POSITIVE NUMBER IN A
0209	05170	12002773	SPB	TEST	
0210	05171	00000000	*		SAP TEST OVER MAP
0211	05171	14005332	IMS	CNT	COUNTER
0212	05172	12005353	SPB	BUPD	INCREMENT B COUNTER
0213	05173	01004010	LAA	SAP	
0214	05174	03205364	STA*	L277	TEST LOCATION
0215	05175	01004503	LAA	T4D	T4D EQ 100000
0216	05176	12002773	SPB	TEST	TEST SUBROUTINE
0217	05177	00000000	*		
0218	05177	14005332	IMS	CNT	COUNTER
0219	05200	12005353	SPB	BUPD	INCREMENT B COUNTER
0220	05201	01004007	LAA	SAZA	
0221	05202	03205364	STA*	L277	TEST LOCATION
0222	05203	01004503	LAA	T4D	T4D EQ 100000
0223	05204	12002773	SPB	TEST	TEST SUBROUTINE
0224	05205	00000000	*		
0225	05205	12005335	SPB	STBS	RESET ALL TEST LOCATIONS TO NOP
0226	05206	00000000	****		
0227	05206	00000000	*		MAP
0228	05206	00000000	*****		AMA* TEST INSTRUCTION IS LOCATED IN LAST
0229	05206	00000000	*		MEMORY CELL OF THE MAP
0230	05206	14005332	IMS	CNT	INCREMENT COUNTER
0231	05207	12005353	SPB	BUPD	
0232	05210	01005331	LAA	SAZ	
0233	05211	03205363	STA*	L276	RESET TEST LOCATION TO NOP
0234	05212	01002507	LAA	AMAA	
0235	05213	03002777	STA	TES1	TES1 IS THE TEST LOCATION
0236	05214	01002501	LAA	T2	T2 EQ 077777
0237	05215	12002773	SPB	TEST	G0 TO TEST
0238	05216	00000025	S0F		
0239	05217	00000033	N0P		

0240	05220	15002503	CMA	T4	T4 EQ 100000
0241	05221	11005223	BRU	**2	
0242	05222	11005224	BRU	**2	
0243	05223	00000000	HLT		A HAS INCORRECT DATA SHOULD BE 100000
0244	05224	00000000	*****		SMA* TEST
0245	05224	00000000	*		INSTRUCTION LOCATED IN LAST CELL OF THE MAP
0246	05224	12005353	SPB	BUPD	
0247	05225	01004012	LAA	FRA	
0248	05226	03002776	STA	TES1-1	SHIFT THRU ALL BITS
0249	05227	01002511	LAA	SMAA	
0250	05230	03002777	STA	TES1	TEST LOCATION
0251	05231	14005332	IMS	CNT	COUNTER INCREMENT
0252	05232	01004503	LAA	T4D	T4D EQ 100000
0253	05233	00000000	*		FRA WILL SET ALL BITS TO N
0254	05233	00000000	*		FRA WILL SET ALL BITS TO ONES PRIOR TO
0255	05233	00000000	*		SUBTRACT INDIRECT
0256	05233	12002773	SPB	TEST	TEST SUBROUTINE
0257	05234	02005333	LBA	STBT	
0258	05235	15002501	CMA	T2	
0259	05236	11005240	BRU	**2	
0260	05237	11005241	BRU	**2	DATA EQ
0261	05240	00000000	HLT		A EQ TO INCORRECT DATA
0262	05241	01005331	LAA	SAZ	
0263	05242	03002776	STA	TES1-1	
0264	05243	00000000	****		IMS TEST
0265	05243	12005353	SPB	BUPD	
0266	05244	01004500	LAA	T1D	
0267	05245	03002505	STA	T6	T6 EQ 177777
0268	05246	00000003	CLA		
0269	05247	03003505	STA	TF	ZERO IN TF
0270	05250	00000000	*		INCREMENT B COUNTER
0271	05250	03205365	STA*	L300	HLT WILL OCCUR IF MEMORY NOT ZERO
0272	05251	01002506	LAA	IMS	
0273	05252	03205364	STA*	L277	
0274	05253	14005332	IMS	CNT	COUNTER
0275	05254	01003006	LAA	BRUA	BRU* SET TO 2ND LOCATION OF MAP
0276	05255	03205366	STA*	L301	
0277	05256	12002773	SPB	TEST	TEST SUBROUTINE
0278	05257	01002505	LAA	T6	
0279	05260	00000023	SAN		

0280	05261	11005270	BRU	ØPR	
0281	05262	01002505	LAA	T6	
0282	05263	00000000	HLT		
0283	05264	01002505	LAA	T6	
0284	05265	02003505	LBA	TF	
0285	05266	00000033	NØP		
0286	05267	02005333	LBA	STBT	
0287	05270	00000003	ØPR	CLA	
0288	05271	03002505	STA	T6	RESET TEST LOCATION TO ZERO
0289	05272	03003505	STA	TF	RESET
0290	05273	00000000	*		A CONTAINS SAME MAP LOCATION WHICH SHOULD BE
0291	05273	00000000	*		ZERO ORIGINAL DATA WAS 177777
0292	05273	00000000	*		CHECK FOR VALUE
0293	05273	00000000	*		
0294	05273	00000000	*****		SPB TEST ROUTINE
0295	05273	01004013	LAA	LSL	LSL 15 TO LOCATION X776
0296	05274	03205363	STA*	L276	NEXT TO LAST LOCATION OF THE MAP
0297	05275	01002513	LAA	SPB	
0298	05276	03205364	STA*	L277	SET SPB INSTRUCTION TO TEST LOCATION
0299	05277	01005334	LAA	HLT	
0300	05300	03205366	STA*	L301	SET HALT TO
0301	05301	12005353	SPB	BUPD	INCREMENT COUNTER FOR ERROR DISPLAY
0302	05302	01003006	LAA	BRUA	
0303	05303	03205365	STA*	L300	RETURN BRU* OUT OF TEST PROGRAM
0304	05304	01002500	LAA	T1	T1 EQ TO 000001
0305	05305	12002773	SPB	TEST	
0306	05306	00000022	SAZ		
0307	05307	00000000	HLT		CHECK B ACCUMULATOR FOR ERROR NUMBER
0308	05310	00000000	*		IF SPB FUNCTIONED PROPERLY A SHOULD BE CLEAR
0309	05310	00000000	*		
0310	05310	00000003	CLA		
0311	05311	03002470	STA	THMP	CLEAR SUBROUTINE ENTRANCE LOCATION
0312	05312	03003470	STA	NTMP	CLEAR SUBROUTINE ENTRANCE LOCATION
0313	05313	12005335	ØK1A	SPB	STBS
0314	05314	00000000	*****		SØF TEST
0315	05314	12005353	SPB	BUPD	INCREMENT B COUNT
0316	05315	12005335	SPB	STBS	
0317	05316	01004014	LAA	SØF	OVERFLOW CHECK OVERFLOW WILL BE SET
0318	05317	03205363	STA*	L276	2776 CONTAINS SØF INSTRUCTION
0319	05320	00000003	CLA		

0320	05321	03205364	STA*	L277	SET TEST LOCATION 2777 TO HALT
0321	05322	01003006	LAA	BRUA	
0322	05323	03205365	STA*	L300	
0323	05324	14005332	IMS	CNT	INCREMENT COUNTER
0324	05325	01002502	LAA	T3	T3 EQ 000001
0325	05326	05002502	AMA	T3	NO OVERFLOW
0326	05327	12002773	SPB	TEST	
0327	05330	11005000	BRU	TAR	
0328	05331	00000033	SAZ	NOP	
0329	05332	00000000	CNT	DATA 0	
0330	05333	00000000	STBT	DATA 0	TEMP STORAGE FOR ERROR COUNTER
0331	05334	00000000	HLT	HLT	
0332	05335	00000000	STBS	ZZZ **	
0333	05336	04005333	STB	STBT	
0334	05337	02077773	STRT	LBA =-5	
0335	05340	01005331	LAA	SAZ	
0336	05341	03605372	STA*	L304+1,1	SET TEST LOCATIONS TO NOP
0337	05342	00000026	IBS		
0338	05343	11005340	BRU	*-3	
0339	05344	02077774	LBA	=-4	
0340	05345	01005331	LAA	SAZ	
0341	05346	03605365	STA*	L300,1	SET TEST LOCATIONS TO MOP
0342	05347	00000026	IBS		
0343	05350	11005345	BRU	*-3	
0344	05351	02005333	LBA	STBT	
0345	05352	11205335	BRU*	STBS	
0346	05353	00000000	RUPD	ZZZ **	COUNTER UPDATE SUBROUTINE
0347	05354	00000000	*		
0348	05354	02005333	LBA	STBT	
0349	05355	00000026	IBS		INCREMENT ERROR COUNTER
0350	05356	00000033	NOP		
0351	05357	04005333	STB	STBT	SAVE NEW ERROR NUMBER
0352	05360	11205353	BRU*	BUPD	
0353	05361	00000000	*		
0354	05361	25402774	L274	DAC '2774	LOCATIONS TO BE USED
0355	05362	25402775	L275	DAC '2775	TO CHECK INTER MAP
0356	05363	25402776	L276	DAC '2776	
0357	05364	25402777	L277	DAC '2777	
0358	05365	25403000	L300	DAC '3000	
0359	05366	25403001	L301	DAC '3001	

Page 10

Catalog No. 303014A

0360	05367	25403002	L302	DAC	'3002
0361	05370	25403003	L303	DAC	'3003
0362	05371	25403004	L304	DAC	'3004
0363	05372	25403005	L305	DAC	'3005
0364	05373	60400000		END	