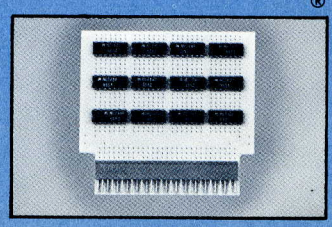
systems engineering laboratories, incorporated

BULLETIN 9032B

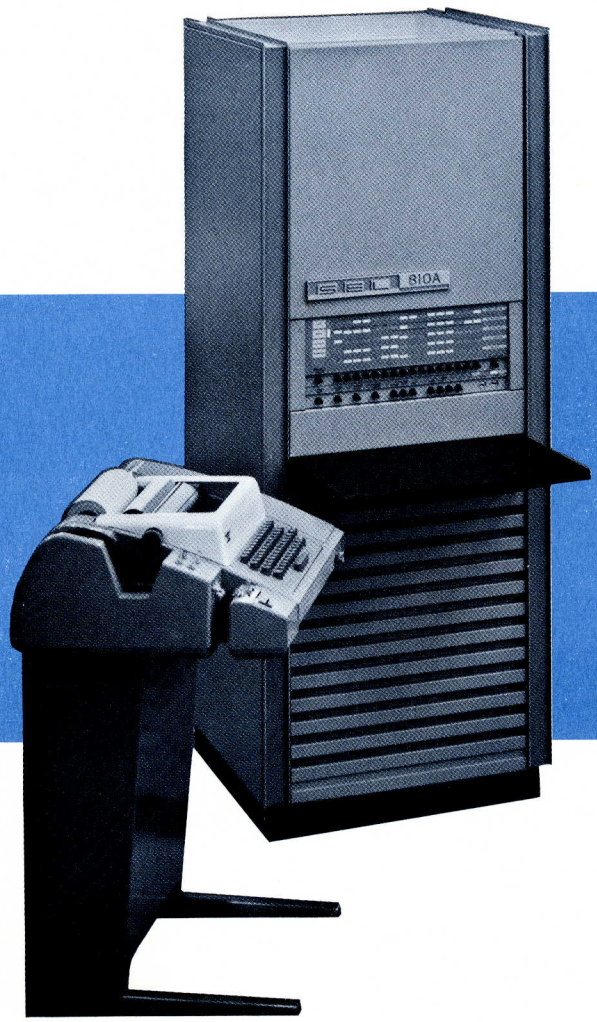
SEL 810A GENERAL PURPOSE DIGITAL COMPUTER

SEL®



FEATURES

- **ALL SILICON MONOLITHIC INTEGRATED DIGITAL CIRCUITS**
- 1.75 MICROSECONDS FULL CYCLE TIME
- 16-BIT WORD LENGTH PLUS PARITY AND PROGRAM PROTECT BITS (MAXIMUM OF 18 BITS)
- MEMORY EXPANDABLE TO 32K WORDS IN 4K OR 8K INCREMENTS
- FULLY PARALLEL OPERATION
- HARDWARE MULTIPLY (7 MICROSECONDS)
- HARDWARE DIVIDE (10.5 MICROSECONDS)
- BINARY TWO'S COMPLEMENT NUMBER REPRESENTATION
- DOUBLE LENGTH ACCUMULATOR
- HARDWARE INDEX REGISTER
- MULTILEVEL INDIRECT ADDRESSING
- UP TO 96 LEVELS OF PRIORITY INTERRUPTS, INDIVIDUALLY ARMABLE
- UNIT I/O CONTROL COMMUNICATING WITH UP TO 64 DATA CHANNELS
- UP TO EIGHT AUTOMATIC, DIRECT MEMORY DATA CHANNELS
- ONE PASS FORTRAN IV
- EXTENSIVE SET OF PERIPHERAL UNITS
- COMPATIBLE WITH SEL STANDARD ACQUISITION AND PROCESS CONTROL SYSTEM COMPONENTS
- CONSTANT THROUGHPUT RATE OF 572,000 16-BIT WORDS PER SECOND



THE SEL 810A GENERAL PURPOSE 16-BIT PARALLEL COMPUTER HAS THE HIGHEST THROUGHPUT RATE OF ANY MACHINE IN ITS SIZE AND PRICE CLASS. IN ADDITION TO FULFILLING REQUIREMENTS FOR VERSATILE HIGH SPEED COMPUTATION, THE SEL 810A PROVIDES SYSTEM CAPABILITIES DEVELOPED THROUGH EXTENSIVE SEL EXPERIENCE IN THE DATA ACQUISITION AND CONTROL FIELDS. A COMPREHENSIVE INPUT/OUTPUT CONFIGURATION PRODUCES THE FLEXIBILITY NECESSARY FOR SEL 810A USE IN THESE APPLICATIONS:

- HIGH SPEED OFF-LINE DATA PROCESSING
- ON-LINE, REAL TIME DATA COMPUTATION & DISPLAY
- ON-LINE DATA COMPRESSION AND RECORDING
- REAL TIME CLOSED LOOP DIRECT DIGITAL CONTROL
- HIGH SPEED AUTOMATIC CHECKOUT & TESTING
- AUTOMATION OF INDUSTRIAL PROCESSES
- SCIENTIFIC COMPUTATION
- SUPERVISORY CONTROL SYSTEMS

SEL 810A BASIC SPECIFICATIONS

WORD SIZE

16 Bits

INTERNAL OPERATION

Full Parallel

INTERNAL MEMORY FULL CYCLE TIME

1.75 Microseconds

CORE STORAGE

4096 Words

I/O UNIT

ASR-33 Typewriter with Paper Tape Reader and Punch
(20 Characters/Second Read . . . 10 Characters/Second Punch)

TEMPERATURE ENVIRONMENT

10°C to 35°C (50°F to 95°F)

SIZE

62" High x 26" Deep x 23¼" Wide

COMPUTATION TIMES INCLUDING ACCESS AND INDEXING:

ADD .....3.5 Microseconds
SUBTRACT .....3.5 Microseconds
MULTIPLY .....7 Microseconds
DIVIDE .....10.5 Microseconds

THE FOLLOWING FEATURES ARE INCLUDED IN THE BASIC CONFIGURATION

Hardware Multiply and Divide
Hardware Program Counter
Double Length Accumulator
2 Priority Interrupt Levels
Multi-Level Indirect Addressing
Complete Software Package
Manual Program Stop and Four Sense Switches
Hardware Index Register
Unit I/O Control
Power Fail Safe

SEL 810A STANDARD OPTIONS

ADDITIONAL CORE STORAGE

Up to 32,768 words in modules of 4096 or 8192 words each

MEMORY PARITY GENERATOR/CHECKER

I/O PARITY GENERATOR/CHECKER

PRIORITY INTERRUPT LEVELS

Up to 96, each individually armable

AUTO START

ASR-35 TYPEWRITER

TABLE TOP OPERATOR'S CONSOLE

TIME SHARING OPTIONS

Program Protect
Instruction Trap
Stall Alarm
Variable Base Register

BLOCK TRANSFER CONTROL CHANNELS

Enables block transfer logic to transfer data between memory and peripheral units in a fully buffered, cycle stealing mode. Any number of BTC channels up to a total of eight may be added to the computer. Up to 16 units or multi-unit controllers may be connected to each BTC. A single, micro-programmed instruction may be executed to initialize a block transfer and command a unit to produce or accept data. A cyclic, automatic block transfer reinitialization capability is also provided.

SEL 810A COMPUTER ORGANIZATION

MEMORY

Up to 32,768 words consisting of 4,096 or 8,192 word magnetic core modules. Memory is divided into 512-word memory address partition (MAP) areas. Any location in the first MAP or the MAP currently addressed by program counter can be directly addressed.

"A" ACCUMULATOR (A)

Main Arithmetic Register

"B" ACCUMULATOR (B)

The 16-Bit extension of the "A" accumulator

REGISTER (T)

The transfer register into which all words from memory are stored pending operation.

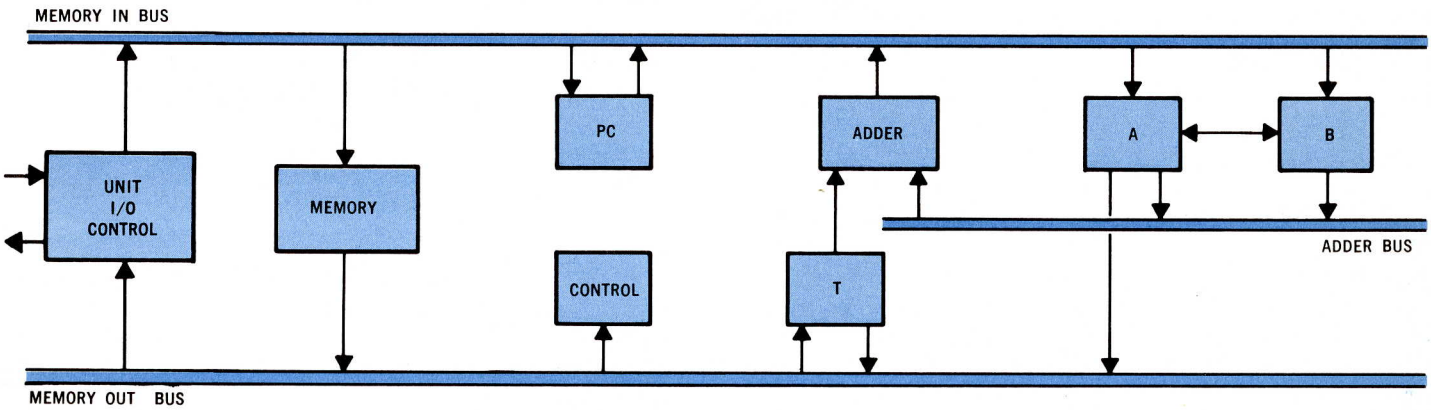
ADDER

Full 16-Bit parallel adder used in all arithmetic and logical operations

PROGRAM COUNTER (PC)

A 15-Bit incremental counter that provides the current instruction address

SEL 810A BLOCK DIAGRAM



INPUT/OUTPUT CONFIGURATION

The basic SEL 810A is equipped with a Unit I/O Control which can connect 64 I/O data channels to the processor. For maximum versatility the 16-bit data words are transferred through the I/O control to/from memory or to/from the A accumulator.

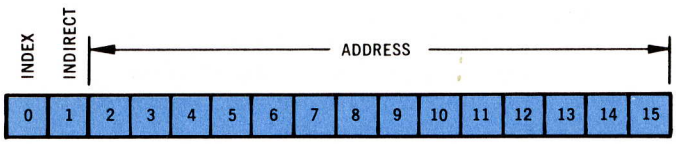
Up to eight block transfer control (BTC) channels can be added as options to allow direct communication between I/O devices and computer memory.

Data transfer is fully buffered and may occur at word rates up to 572 KC. Only one memory cycle is stolen for each word transferred. The block transfer logic is capable of automatic reinitialization from the contents of two fixed memory locations each time a block transfer is completed.

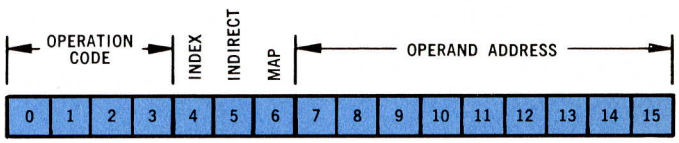
I/O parity generation and checking is available as an option.

SEL 810A WORD FORMAT

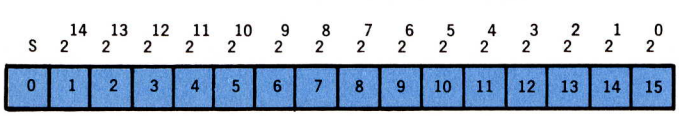
INDIRECT ADDRESS FORMAT



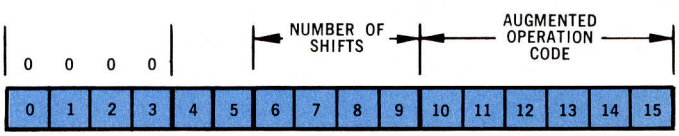
INSTRUCTION FORMAT



DATA FORMAT



AUGMENTED INSTRUCTION FORMAT



SEL 810A SOFTWARE PACKAGE

The SEL 810A is delivered with an unusually powerful software package for a machine of its size. These programs are extremely valuable aids to the efficient use of the SEL 810A hardware. The software package includes a mnemonic assembler, compiler, a complete subroutine library, utility, maintenance, and program debugging routines.

FORTRAN IV

The SEL 810A FORTRAN IV allows — in addition to all the capabilities of FORTRAN II — double precision real, complex, logical, and Hollerith data type representation. Mixed mode expressions of data types are allowable and present an unusually simple method of rapidly obtaining an operating scientific program without undue attention to data representation. Mixed Fortran IV and assembly language statement capability is a vital feature of interest to the programmer faced with a requirement to program for real time operation. The SEL 810A Fortran IV meets the standards of the ASA. It requires 8K words of memory.

MNEMBLER

The SEL 810A MNEmonic asseMBLER is a translation program that allows machine language coding in easily written mnemonic operation codes. It also allows symbolic representation of core locations and provides many programmer conveniences, such as number base translation. Two modes are provided — a fast one-pass mnembler for speed limited I/O hardware configurations, and a two-pass mnembler that produces more compact object tapes. Both assemblers operate with only 4K of memory required. Automatic address mapping is performed by the mnembler to permit the programmer to ignore the MAP addressing system used by the hardware.

LIBRARY

The SEL 810A library includes a comprehensive set of subroutines for use by the programmer. The Fortran IV set is included and is callable by both the Fortran IV compiler and mnembler. Routines include sine, cosine, arctan, square root, exponential, log, number base conversion, and many others.

UTILITY ROUTINES

The utility routines include an efficient tape editor, an on-line dynamic de-bug, dumps, listing, conversion programs, I/O handlers and others.

MAINTENANCE ROUTINES

The standard SEL 810A maintenance routines allow checkout of all 810A hardware.

SEL 810A INSTRUCTION LIST

The SEL 810A is equipped with a powerful repertoire of direct address and augmented instructions. These instructions, including two 3-way branch/skip instructions and multiply and divide instructions, are coupled with hardware indexing and indirect address chaining to provide maximum program flexibility and speed. The 15-bit program counter of the basic computer is capable of addressing the full 32,768 memory locations, while the 9-bit operand address has access to the 512-word memory address partition (MAP) currently within the range of the program counter. The MAP bit, when set to zero, allows direct access to any of the first 512 words of memory (reference MAP area). Addresses outside the current MAP or reference boundaries can be addressed through the use of the hardware index register to directly address the full 32,768 memory locations. An index operation does not increase instruction time, and an indirect operation requires only 1.75 additional microseconds.

CLASS	CODE MNEMONIC	TIME (Microseconds)	FUNCTION
ARITHMETIC	AMA	3.5	Add Memory to A.
	AMB	3.5	Add Memory to B
	SMA	3.5	Subtract Memory from A.
	MPY	7.0	Multiply B times Memory.
	DIV	10.5	Divide A and B by Memory.
	RNA'	1.75	Round A by MSB in B.
LOAD/STORE	LAA	3.5	Load A from Memory
	LBA	3.5	Load B from Memory
	STA	3.5	Store Memory from A.
	STB	3.5	Store Memory from B.
	LCS'	1.75	Load Control Switches in A.
BRANCH/SKIP	BRU	1.75	Unconditional Branch
	SPB	3.5	Store Place and Branch
	SNS'	1.75	Skip if Sense Switch Not Set.
	IMS	5.25	Increment Memory and Skip.
	CMA	5.25	Compare Memory and A (3 way) n+1(—), n+2(0), n+3(+)
	IBS'	1.75	Increment B (Index) and Skip.
	SAZ'	1.75	Skip if A is Zero
	SAP'	1.75	Skip if A is Positive
	SAN'	1.75	Skip if A is Negative
	SOF'	1.75	Skip no Overflow
	SAS'	1.75	Skip on A. Sign (3 way) n+1(—), n+2(0), n+3(+)
	SNO'	1.75	Skip if A is Not Normalized
	LOB'	3.5	Long Branch
LOGICAL	ABA'	1.75	AND A and B
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	NEG'	1.75	Negate A
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	CSB'	1.75	Transfer B Sign to Carry and Clear B Sign to Positive.
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	FRA'		Right Shift A and B
	FLA'		Left Shift A and B
	RSL'		Right Logical Shift A
	FRL'		Logical Rotate A and B
	LSL'		Left
	FLL'		Left Logical Shift A
			Left Logical Shift A and B
CONTROL	HLT'	1.75	Halt
	NOP'	1.75	No Operation
	TOI'	1.75	Turn off Interrupt
	PIE'	3.5	Priority Interrupt Enable
	PID'	3.5	Priority Interrupt Disable
INPUT/ OUTPUT	AIP	5.25	Accumulator Input
	AOP	5.25	Accumulator Output
	MIP	5.25	Memory Input
	MOP	5.25	Memory Output
	CEU	5.25	Command External Unit
	TEU	5.25	Test External Unit
	PON*	3.5	Protect Bit ON
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	TBV*	1.75	Transfer B to VBR
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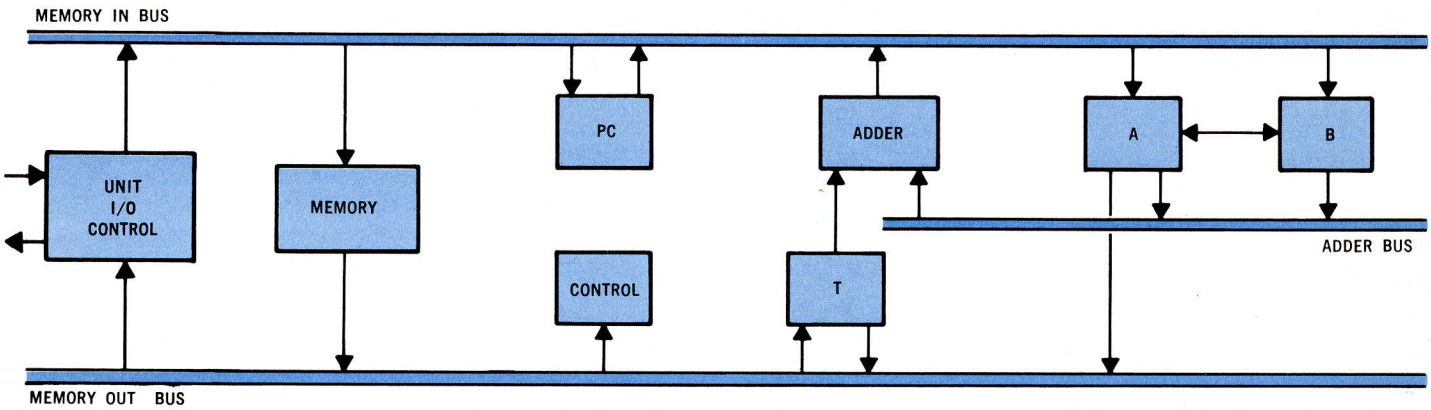

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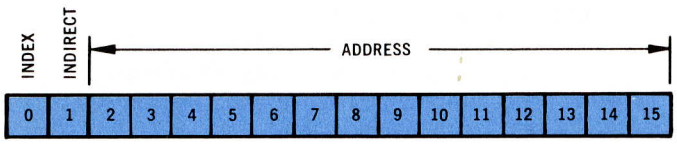

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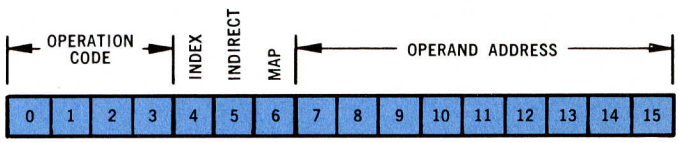
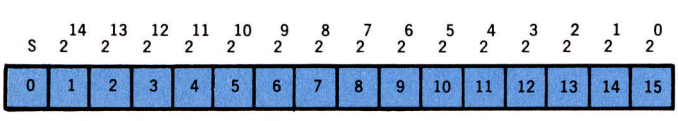


DATA FORMAT



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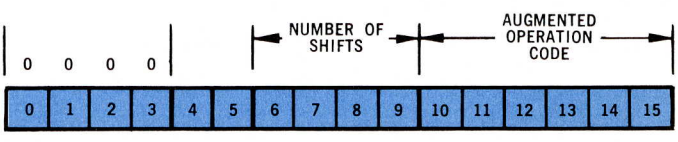

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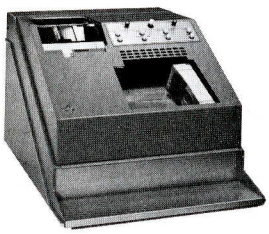
* Optional Augmented

SEL 800 SERIES PERIPHERAL EQUIPMENT

The SEL 810A computer has a wide range of available input/output equipment. Each peripheral device has its own control unit which contains a word or character buffer as required. Up to 64 input units plus 64 output units may be connected to the Unit I/O control.

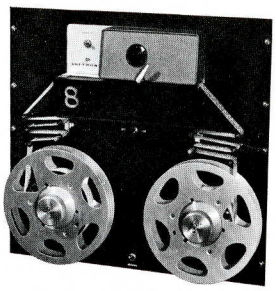
SEL 810A PERIPHERAL EQUIPMENT

Catalog No.	Description



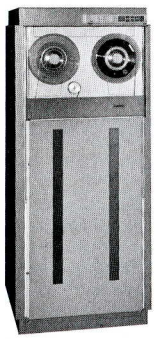
CARD READERS AND PUNCHES

81-410A — Medium Speed Reader ..... 200 Cards/Minute
81-450A — High Speed Reader ..... 400 Cards/Minute
81-440A — Punch ..... 100 Cards/Minute



PAPER TAPE READERS AND PUNCHES

81-510A — High Speed Photoelectric Reader ..... 300 Characters/Second
81-520A — High Speed Punch ..... 110 Characters/Second
81-525A — High Speed Punch/Reader ..... 110 and 300 Characters/Second
80-530A — Paper Tape Spooler

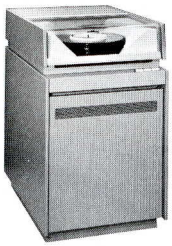


MAGNETIC TAPE AND DISC SYSTEMS

81-610A — Tape Control Unit—Handles up to 8 ea. 80-615A Magnetic Tape Units, 7 or 9 Tracks
80-615A — Magnetic Tape Unit, 200, 556 and 800 bits at 45, 75, 120, 150 IPS, 7 or 9 Tracks
81-653A — Disc File ..... 1,500,000 Word Capacity

TYPEWRITERS AND LINE PRINTERS

80-712A — ASR33, KSR33, RO33, ASR35, KSR35, RO35 ..... 10 Characters Second
81-730A — Line Printer ..... 300 Lines Minute
81-731A — Line Printer ..... 600 Lines Minute } 120 Columns
81-732A — Line Printer ..... 1000 Lines Minute



PLOTTERS AND DISPLAYS

81-810A — Incremental Plotter ..... 12-in. chart width
81-812A — Incremental Plotter ..... 31-in. chart width } 300 steps/sec.
81-816A — 16" CRT Display
81-820A — Vector Generator
81-822A — Character Generator
81-824A — Refresh Memory
81-830A — Light Pen
} Used with 81-816A

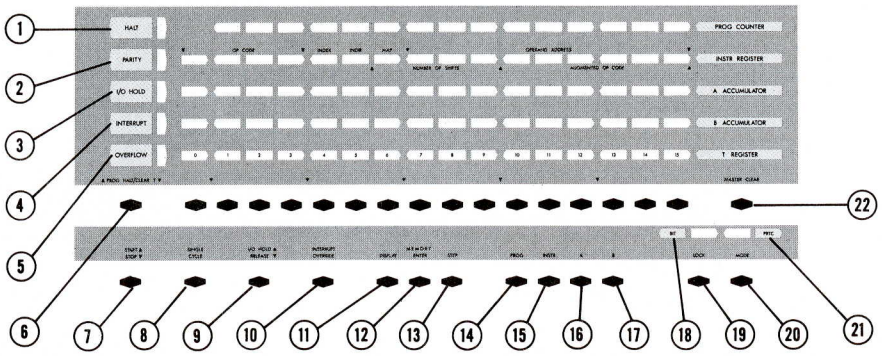
OTHER PERIPHERALS

81-850A — Data Terminal, 16-Bit
81-030A — Interval Timer
80-903A — Low Level Reed Multiplexer/ADC Combination (128 Channels)

OPERATOR'S CONTROL PANEL

The operator's control panel is unusually complete with parallel display of all registers. Provision to enter manual data into any register or core location is standard. The SEL 810A is the only machine in its size or price class with a hardware program stop available at the console. The entire panel is designed for maximum operator/machine communication.

SEL 810A CONTROL PANEL



1 Lights to indicate a program halt.

2 Lights to indicate the detection of a memory parity error. The parity error indicator will be reset when the start/stop switch is depressed.

3 Lights to indicate a wait for I/O function.

4 Lights to indicate a priority interrupt.

5 Lights to indicate an arithmetic condition.

6 Raised to connect switches 0-15 as program HALT switches. Depressed to clear the contents of the "T" register.

7 Depressed once to start program. The next time depressed will stop the program.

8 Depressed to execute single instructions in normal sequence.

9 Depressed to release I/O wait and allow computer to resume.

10 Depressed to inhibit operation of priority interrupts (lock).

11 Depressed to display the contents of the current memory location.

12 Depressed to load the contents of T into the current memory location.

13 Used with the display or enter switch (in up position) to display or enter sequential memory locations by depressing the step switch.

14 Depressed to transfer the contents of the T register to the program counter.

15 Depressed to transfer the contents of the T register to the instruction register.

16 Depressed to transfer the contents of the T register to the A accumulator.

17 Depressed to transfer the contents of the T register to the B accumulator.

18 *Indicates the presence of a program protect bit in the latest word accessed from memory.

19 *This key lock switch inhibits the operation of all control switches.

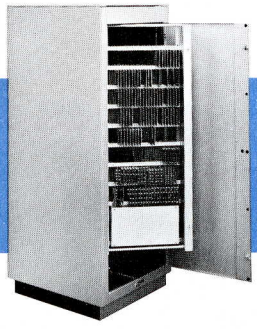
20 *This key lock switch puts the computer in the program protect mode.

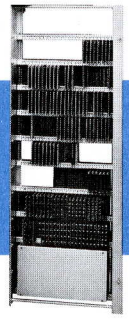
21 *Indicates the status of the program protect latch.

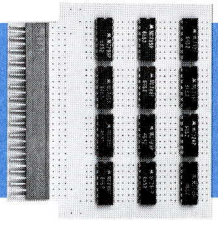
22 Depressed to clear all major registers and control latches.

*These indicators and switches are supplied with the program protect option.

MAINTENANCE EFFICIENCY UNSURPASSED







SEL 810A MAINFRAME

SEL 810A Mainframe opens in rear, and "pages" containing micrologic modules swing out exposing all computer circuitry for maintenance.

PAGE

Pages contain circuit modules. Connectors are Elco Varicon. Wire wrap used exclusively for highest reliability and easiest field service.

SEL MICROLOGIC MODULE

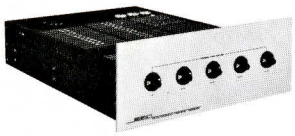
Silicon monolithic integrated digital circuits exclusively. Dual In-Line packaging allows same serviceability as discrete component circuits, but gives latest state of the art speed and reliability. Components mounted on one side only.

SEL SERVICE FOR 810A USERS

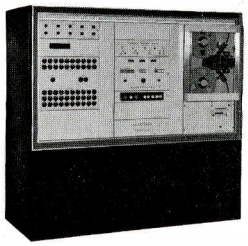
- Two Week Programming and Four Week Maintenance Courses Beginning Once Each Quarter in Fort Lauderdale.
- On Call Service Contracts.
- Field Resident Service/Operation contracts.
- Programming Services.

OTHER SEL PRODUCTS

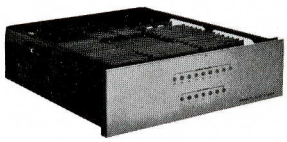
SEL LOW LEVEL MULTIPLEXERS have several patented features which provide the advantages of an amplifier-per-channel system at a fraction of the cost. Up to hundreds of input channels with random access programming, random addressable individual channels gains, channel displays, individual channel offset, and highest sampling rates are available.



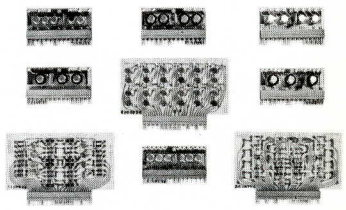
SEL 600 DATA ACQUISITION SYSTEMS can handle from a few to hundreds of inputs from your transducers, digitize this information and produce digital tapes ready for processing in your computer. Special features include linearizing and scaling of data and complete conversion to engineering units.

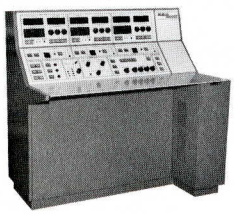


SEL MAGNETIC CORE MEMORY SYSTEMS provide capacity ranges from 128 to 8192 words per basic unit, and word size according to customer requirement. Standard addressing types available are random access, sequential, sequential / interlace. Combinations of types are also available.

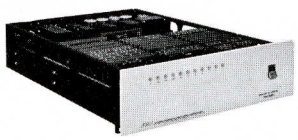


SEL DIGITAL LOGIC MODULES employ conventional solid-state circuitry in the 8000 series and the latest micrologic techniques in the 8500 series. SEL modules are designed to implement any logical requirement and at the same time, provide dependable and efficient operation.

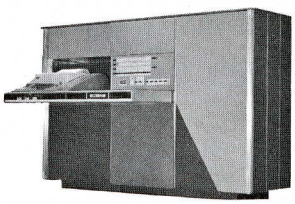




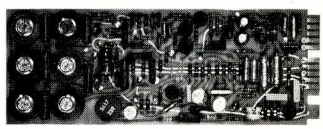
SEL 900 SERIES INDUSTRIAL CONTROL SYSTEMS for Real Time On-Line Process Control, Supervisory/Optimizing Control and Pre-Set Control. SEL computers provide all computation, comparison and stored program functions for these direct digital and hybrid control systems.



SEL ANALOG-TO-DIGITAL CONVERTERS provide low, medium or high speed conversions. Binary or BCD outputs, sample and hold, internal or external command, and display can be provided at customer option.



SEL 840A 24-BIT SERIES DIGITAL COMPUTING SYSTEMS provide capability for on-line or off-line processing of data and find wide usage in processing control applications. Features include single address instruction with indexing and indirect addressing. All types of peripheral equipment are available.



SEL OPERATIONAL AMPLIFIERS are completely solid state and provide the resolution previously available only in vacuum tube models. Features include outputs to ± 100 volts, overload protection, and low input current without temperature compensation. Several card and connector configurations are available for customer packaging requirements.

SEL®

SYSTEMS ENGINEERING LABORATORIES, INCORPORATED

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