ST11R RLL CONTROLLER

PRODUCT MANUAL

Seagate

ST11R RLL Controller Product Manual

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CONTENTS

1.0 GENERAL PRODUCT DEFINITION AND INTERFACE SUMMARY

The ST11R supports up to two Seagate ST412 interface drives with RLL encoding. Programs written to run on standard IBM hard disc controllers will operate correctly. The ST11R's onboard software allows configuration for specific drive characteristics.

1.1 DMA OR PROGRAM I/O

Commands are transferred under program I/O (PIO) mode.

Data can be transferred under either program I/O or DMA mode. The controller may be configured to DMA channel 1, 2, or 3 on the IBM PC or PC XT computer. The DMA mode can be disabled through the control register, therefore, another I/O device can share the DMA channel. The default DMA channel is 3. See Note.

1.1.1 INTERRUPT GENERATION

The ST11R may be configured to generate interrupts on IRQ5 or IRQ2. The default is IRQ5. Interrupt generation can be disabled through the control register.

Note: Changing the DMA channel or Interrupt level requires a hardware change and either a new BIOS or a new system-level software driver. Neither the BIOS or software driver are presently available from Seagate.

1.2 AUTOMATIC SEEK AND VERIFY

A seek command is implied in every data transfer command. If the heads are not positioned over the correct cylinder, a seek is initiated, and a cylinder verification is performed after the seek completes.

1.2.1 FAULT DETECTION

Four classes of faults are flagged to improve error handling:

- Drive faults
- Controller faults
- Command related faults
- Miscellaneous errors

1.2.2 AUTOMATIC HEAD AND CYLINDER SWITCHING

If the end of a track is reached during a multi-block transfer, the controller automatically switches to the next track. If the end of a cylinder is reached, the controller issues a seek and resumes the transfer.

1.2.3 DATA ERROR RECOVERY

If a data error is detected during a read operation, the controller will instigate the following error recovery procedure:

1. Reread 8 times
2. Seek to the maximum cylinder followed by a seek to Track Ø
3. Apply error correction
4. Microstep and reread 8 times
5. Microstep and apply error recovery 8 times

If an error is encountered during a seek operation, the following error recovery procedure is applied:

1. Calculate actual location versus expected and reseek
2. Seek to the maximum cylinder followed by a seek to Track Ø
3. Reseek

1.2.4 SECTOR INTERLEAVE

Sector interleaving is programmable from 1 to (sectors/tracks)-1.

1.2.5 ALTERNATE TRACK ASSIGNMENT

The host can assign an alternate track for a defective track. Subsequent accesses to the defective track will cause the controller to transfer data from the new track automatically.

1.3 INTERFACE CONNECTIONS

The ST11R controller is designed to operate in the IBM PC/XT. It contains 8-bit data paths. The DMA arbitration operates according to the scheme described in the IBM PC or PC/XT Technical Reference Manual. The IBM standard I/O channel pin description is outlined in Appendix A. System configuration is illustrated in *Figure 1 on page 3-2.*

2.0 ELECTRICAL/MECHANICAL SPECIFICATIONS

2.1 DC POWER REQUIREMENTS

Voltage:	5 VDC ± 5%

2.2 BOARD DIMENSIONS

Width:	4.20 in. max.
Length:	5.12 in. max.
Height:	0.80 in. max.

2.3 ENVIRONMENTAL SPECIFICATIONS

2.3.1 AMBIENT TEMPERATURE

Operating:	0^{o} C to 55^{o} C (32^{o} F to 131^{o} F)
Nonoperating:	-40^{o} C to 75^{o} C (-40^{o} F to 177^{o} F)

2.3.2 RELATIVE HUMIDITY

Maximum Wet Bulb:	30^{o} C (86^{o} F)
Operating:	10% to 95% noncondensing
Nonoperating:	10% to 95% noncondensing

3.0 SYSTEM CONFIGURATION

3.1 INSTALLATION

The ST11R assists the end-user during the install session with *help screens.* Refer to the ST11R installation guide for install instructions.

3.2 PORT/PROM ADDRESSES

The port and PROM addresses for the ST11R are jumper selectable.

Pins A-B	Pins C-D	BIOS PROM	IO Port
open	open	C8000-CBFFF	320-323
shorted	open	D0000-D3FFF	324-327
open	shorted	D8000-DBFFF	328-32B
shorted	shorted	E0000-E3FFF	32C-32F

3.3 DRIVE POWER CONNECTOR

The J5 header on the ST11R may be used to provide disk drive power on systems lacking power connectors. J5 is a 5-pin right angle double row header on 0.1 inch centers.

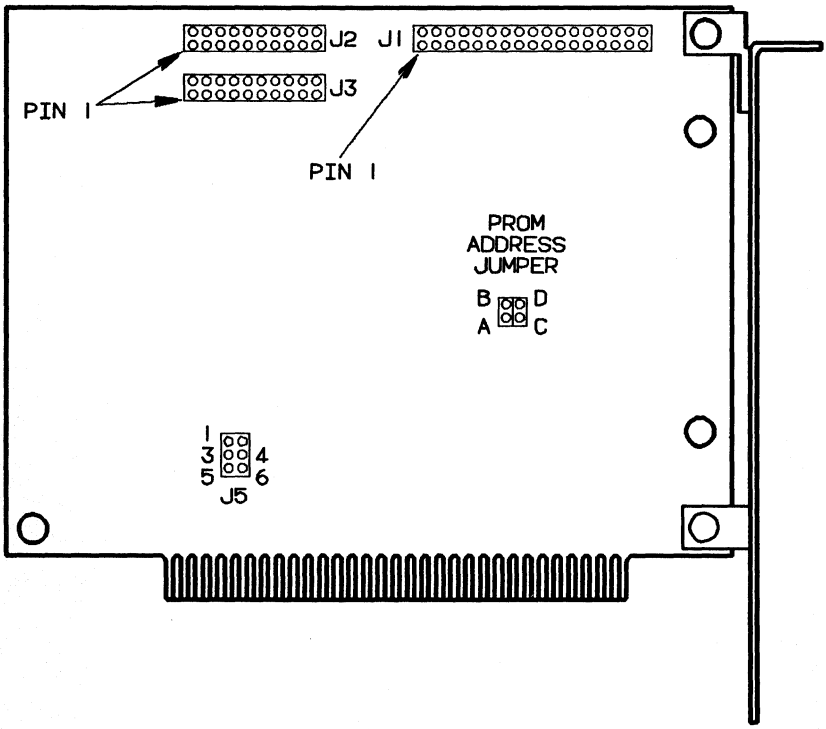
Note: Some configurations of the ST11R may not include the J5 header.

J5 Pin-Out

Pin	Signal	Description
1	+ 12 V	+ 12 Volt Supply
2	+ 12 V	+ 12 Volt Supply
3	+ 5 V	+ 5 Volt Supply
4	GND	Ground (Pin removed)
4	GND	Ground
4	GND	Ground

Pin 4 is removed to allow connector keying.

FIGURE 1: ST11R



4.0 SOFTWARE INTERFACE

4.1 INTERFACE REGISTER DEFINITIONS

The base I/O address is determined by jumpers (see *"3.2 Port/PROM Addresses" on page 3-1*).

I/O Address 320, 324, 328 or 32C

DATA REGISTER

Read	from Data Buffer
Write	to Data Buffer

I/O Address 321, 325, 329 or 32D

STATUS REGISTER/RESET

Read	bit 0 + Request
	bit 1 + Input/-Output
	bit 2 + Command/-Data
	bit 3 + Busy
	bit 4 + DRQ
	bit 5 + IRQ
	bit 6 not used, will be 0
	bit 7 not used, will be 0
Write	Reset Controller

I/O Address 322, 326, 32A or 32E

CONFIGURATION REGISTER

Read	Configuration, will return 01_H
Write	Select Controller

I/O Address 323, 327, 32B or 32F

DMA/INTERRUPT CONTROL

Read	Reserved

Write Control
bit 0 +Enable DMA
bit 1 +Enable Interrupt
bit 2 - bit 7 not used

4.1.1 DATA INPUT/OUTPUT REGISTER (DIOR)

Disc read/write data, command bytes, completion status, and controller sense bytes are passed through this register. The data is held for each handshake cycle.

4.1.2 RESET CONTROLLER

When any data is written to this port, the internal state of the controller is initialized as if a system reset had occurred.

4.1.3 STATUS REGISTER

The status register is a read-only register. It contains controller status bits that enable the host computer to monitor the status of the controller during command execution.

FIGURE 2: Status Register

BIT	7	6	5	4	3	2	1	0
NAME	x	x	INTR	DREQ	SEL	COM/ DATA	IN/OUT	READY

INTR: * The controller is requesting an interrupt.
DREQ: * The controller is requesting a data transfer to or from the host. (See IN/OUT.)
SEL: The controller has been successfully selected by the host.
COM/DTA: A zero indicates that the bytes transferred through the DIO register are data bytes. A one indicates that the bytes are command or status bytes.

IN/OUT: A zero indicates data flow from host to controller. A one indicates data flow from controller to host.

READY: Indicates that the controller is ready to receive data/command or transmit data from/to the host. When ready is one, bits 1 & 2 are interpreted as follows:

* Active only if enabled in control register.

Meaning of Bytes Passed

In/Out	Cmd/ Data	
0	0	Data out of host.
0	1	Command byte out of host.
1	0	Data to host.
1	1	Completion status byte to host.

4.1.4 SELECT CONTROLLER

When any data is written to this port, the controller is selected to begin a command sequence. It will initialize to command input status.

4.1.5 CONTROL REGISTER

This write-only register contains the interrupt enable and DMA enable bits.

FIGURE 3: Control Register

BIT	7	6	5	4	3	2	1	0
NAME	x	x	x	x	x	x	INTE	DMAE

INTE: Interrupt Enable. Enables the interrupt upon the completion of each command.

DMAE: DMA Enable. Enables the DMA transfer of data.

4.2 HOST INTERACTION PROTOCOL

There are three possible phases to a host/controller interaction. They are the command, data, and result phases. Handshaking is done through the status register.

The phase is indicated by the bits in the status register. When the ready bit is 1, the C/D and I/O bits are valid and may be examined to find the current phase.

4.2.1 SELECTION

When the controller is idle (no command is in progress, select = 0) and is selected by the host (by writing to the select port), a command phase will be initiated. The select bit in the status register will be set to one.

4.2.2 COMMAND PHASE

In this phase, ready will be 1, C/D will be 1, and I/O will be 0.

The host should send bytes of the command descriptor block (CDB) to the controller, waiting for the ready line to be 1 before sending each byte.

4.2.3 DATA PHASE

In this phase, ready will be 1, C/D will be 0, and I/O will be 0 or 1 depending on the direction of the transfer of data.

Some commands which do not transfer data (e.g.,Test Drive Ready) do not generate a data phase and skip to the result phase.

The controller will transfer the data as commanded. If PIO is used, the host should handshake each byte on the ready bit in the status register. If DMA is used, the controller and the host DMA will handshake automatically using the DREQ line.

4.2.4 RESULT PHASE

In this phase, ready will be 1, C/D will be 1, and I/O will be 1.

The controller will set the INTR bit in the status register if INTE is set in the control register and request an interrupt in the host at this time.

A completion status byte will be loaded into the data I/O register. The host should read this byte and check the error bit. When the byte is read, the select bit in the status register will become 0, and the controller becomes idle again.

FIGURE 4: Completion Status Byte

BIT	7	6	5	4	3	2	1	0
NAME	x	x	LUN	x	x	x	Error	x

LUN: Device logical unit number, drive 0 or 1.

Error: An error occurred during the command. The host may issue a Request Sense command for a detailed description of the error.

4.3 HOST INTERACTION PROCEDURE

4.3.1 SELECTION

The host outputs a byte to the controller select port. Then it waits for the selected and ready signals to be asserted in the status register, which means the controller is ready for command transfer.

4.3.2 WAIT FOR CONTROLLER READY

The host waits for the ready bit to be asserted. When ready is set, I/O and C/D are valid. The decode of the two bits should indicate command byte transfer (I/O = 0 C/D = 1).

4.3.3 SET UP CONTROL REGISTER

The host writes to the control register to indicate whether DMA and interrupt facilities will be used with this command.

4.3.4 TRANSFER CDB TO CONTROLLER

When the decode indicates a command transfer, the device driver then writes six command bytes into the data I/O register one at a time using programmed I/O. The ready bit may be used by the host to determine when the controller is prepared to accept each byte.

Note: After the driver has verified that the controller is ready for command transfer, the first 6 command bytes can actually be written to the controller without handshaking each byte from the host. However, it is recommended that handshaking be performed.

4.3.5 CHECK FOR CONTROLLER READY

After the command bytes have been transferred, the driver should check on the ready bit to see if an error has occurred. If ready is cleared, then the command bytes have been transferred correctly.

4.3.6 DATA PHASE WITH NO DMA

If the data is transferred under program I/O, the host can use a procedure similar to the command byte transfer. The host should handshake with the ready bit in the status register to write bytes to the data I/O register.

4.3.7 DATA PHASE WITH DMA

The host should set up the DMA channel and initiate the transfer. The controller will assert DREQ whenever the controller is ready to send or receive data to/from the host. The host DMA should be programmed in single transfer mode and the word count should be programmed to

the number of blocks to be transferred multiplied by the number of bytes per sector, minus one.

4.3.8 RESULT PHASE

Upon the completion of the command (either due to normal or abnormal conditions), the controller will load the completion status byte (CSB) into the DIOR. If an interrupt was requested, the controller will issue an interrupt to the host. Otherwise, the host must check the C/D and I/O bits in the status register to detect the result phase.

The host acknowledges this signal by turning off the INTE and DMAE bits in the control register, and then reads the completion status byte from the DIOR. This will return the INTR and DREQ bits to a high-impedance condition on the host bus.

When the CSB is read, the controller de-asserts the SEL bit in the status register and is ready to be reselected again for the next command. (This is the idle state of the controller.)

If the error bit is set in the completion status byte, the driver should issue a Request Sense command to receive detailed error information.

5.0 HARDWARE INTERFACE

5.1 I/O BUS OPERATION

The controller occupies 4 sequential locations in the I/O address space. The base I/O address is jumper selectable. The default address is 320_H. For jumper configurations see *"3.2 Port/PROM Addresses" on page 3-1*.

5.2 INTERRUPT OPERATION

The ST11/11R can generate a hardware interrupt on command completion if the interrupt enable bit is set in the control register. The state of the INTR bit in the status register corresponds to the state of the IRQ line on the host bus. Once the interrupt is generated, the interrupt request line is asserted until the interrupt enable is cleared. The interrupt is jumper selectable between IRQ5 and IRQ2. The default interrupt is IRQ5.

5.3 DMA OPERATION

The DMA channel in the ST11/11R is enabled when the DMAE bit is asserted in the control register. The state of the DREQ flag in the status register corresponds to the state of the DREQ line in the host bus. The DMA channel is jumper selectable between DMA channel 1, 2, or 3. The default is DMA channel 3.

5.4 BIOS DECODE OPERATION

The ST11/11R provide BIOS decode for either an 8K or 16K ROM. The BIOS size is jumper selectable, the default size is 16K. The base memory address decide is jumper selectable, the default address is $C8000_H$. The last 64 bytes of each 8K block of the BIOS ROM is decoded to a scratchpad RAM. If a 16K BIOS size is selected, the same 64 byte RAM is decoded at the end of each 8K block.

8K BIOS Decode:

Pins A-B	Pins C-D	BIOS	RAM
Open	Open	C8000-C9FBF	C9FC0-C9FFF
Shorted	Open	D0000-D1FBF	D1FC0-D1FFF
Open	Shorted	D8000-D9FBF	D9FC0-D9FFF
Shorted	Shorted	E0000-E1FBF	E1FC0-E1FFF

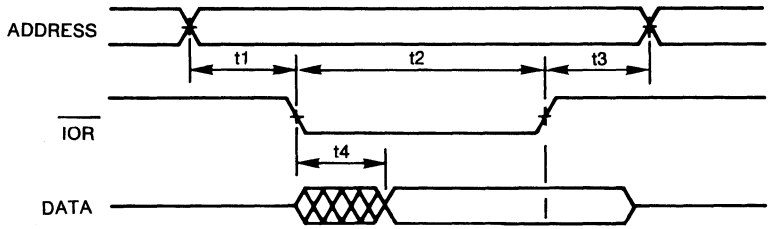
16K BIOS Decode:

Pins A-B	Pins C-D	BIOS	RAM
Open	Open	C8000-C9FBF, CA000-CBFBF	C9FC0-C9FFF, CBFC0-CBFFF
Shorted	Open	D0000-D1FBF, D2000-D3FBF	D1FC0-D1FFF, D3FC0-D3FFF
Open	Shorted	D8000-D9FBF, DA000-DBFBF	D9FC0-D9FFF, DBFC0-DBFFF
Shorted	Shorted	E0000-E1FBF, E2000-E3FBF	E1FC0-E1FFF, E3FC0-E3FFF

5.5 BUS TIMING

5.5.1 I/O READ TIMING

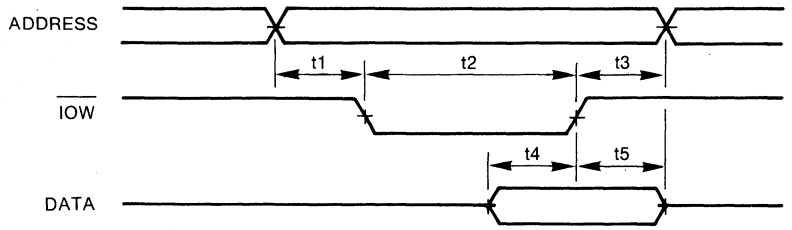
FIGURE 5: I/O Read Timing



t1	address setup	50 ns.	Min.
t2	pulse width	100 ns.	Min.
t3	address hold	0	Min.
t4	data valid	85 ns.	Max.

5.5.2 I/O WRITE TIMING

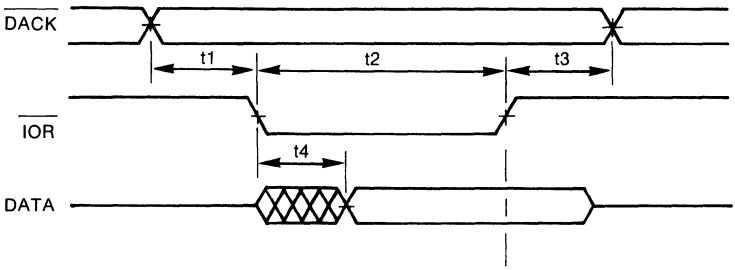
FIGURE 6: I/O Write Timing



t1	address setup	50 ns.	Min.
t2	pulse width	100 ns.	Min.
t3	address hold	20 ns.	Min.
t4	data setup	62 ns.	Min.
t5	data hold	20 ns.	Min.

5.5.3 DMA READ TIMING

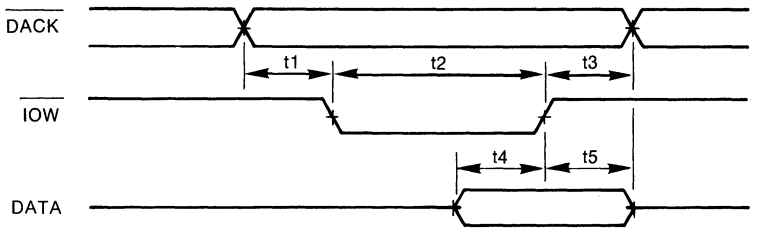
FIGURE 7: DMA Read Timing



t1	DACK setup	0	Min.
t2	pulse width	100 ns.	Min.
t3	DACK hold	0	Min.
t4	data valid	85 ns.	Max.

5.5.4 DMA WRITE TIMING

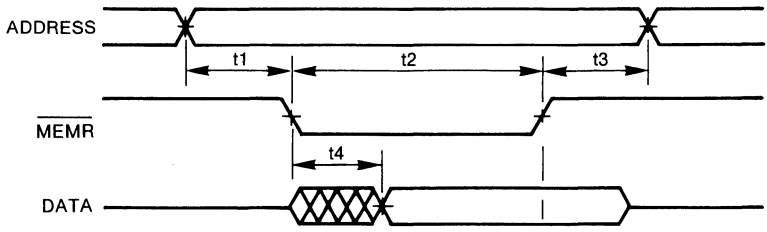
FIGURE 8: DMA Write Timing



t1	DACK setup	0	Min.
t2	pulse width	100 ns.	Min.
t3	DACK hold	0	Min.
t4	data setup	62 ns.	Min.
t5	data hold	20 ns.	Min.

5.5.5 MEMORY READ TIMING

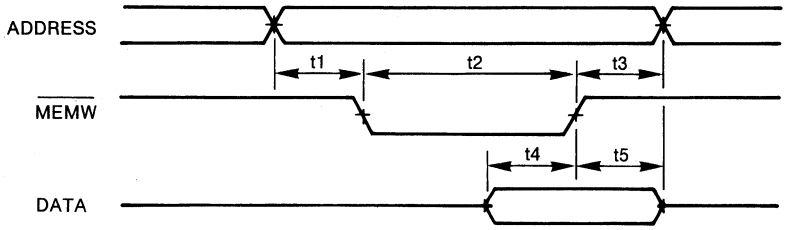
FIGURE 9: Memory Read Timing



t1	address setup	50 ns.	Min.
t2	pulse width	100 ns.	Min.
t3	address hold	0	Min.
t4	data valid	112 ns.	Max.

5.5.6 MEMORY WRITE TIMING

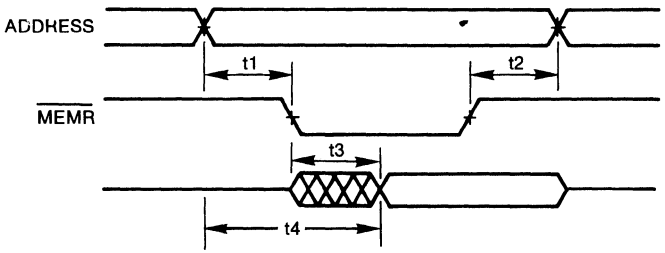
FIGURE 10: Memory Write Timing



t1	address setup	50 ns.	Min.
t2	pulse width	100 ns.	Min.
t3	address hold	20 ns.	Min.
t4	data setup	62 ns.	Min.
t5	data hold	10 ns.	Min.

5.5.7 BIOS DECODE TIMING

FIGURE 11: BIOS Decode Timing



t1	address setup	50 ns.	Min.
t2	address hold	0 ns.	Min.
t3	data valid	152 ns.	Max.
t4	address access	262 ns.	Max.

6.0 HARD DISC COMMANDS

Commands issued by the ST11/11R are categorized into three classes:

Class 0	Control, Data Transfer, and Status commands
Class 1-6	Reserved
Class 7	Diagnostic commands

6.1 COMMAND BLOCKS

FIGURE 12: General Command Block

BIT BYTE	7	6	5	4	3	2	1	0
0	Class			Opcode				
1	LUN			Head Number				
2	Cyl. High			Sector Number				
3	Cylinder Low							
4	Number of Blocks / Interleave							
5	Control							

6.1.1 COMMAND CODE (BYTE 0)

The command code consists of the class, bits 7 to 5, and the opcode, bits 4 to 0.

6.1.2 LUN (BYTE 1)

This field specifies the logical unit number of the drive to be selected. It corresponds to the drive select jumpers (with normal addressing) on the drives as follows:

Winchester Drive Select 2 = LUN 1

Note: Bits 7 and 6 of the LUN field will be ignored.

6.1.3 HEAD NUMBER (BYTE 1)

This field specifies the disc head number to be selected. Legal range is 0 to 15 decimal.

6.1.4 SECTOR NUMBER (BYTE 2)

This field specifies the sector number. See Section 7.0 for track format.

6.1.5 CYLINDER HIGH (BYTE 2)

This field specifies the two most significant bits of the cylinder number.

6.1.6 CYLINDER LOW (BYTE 3)

This field specifies the eight least significant bits of the cylinder number.

6.1.7 NUMBER OF BLOCKS (BYTE 4)

This field specifies the number of sectors to be transferred. One sector transfer is a value of 1. A value of 0 will result in a transfer of 256 sectors.

6.1.8 INTERLEAVE (BYTE 4)

This field specifies the interleave during the Format operation.

Interleave is a factor used while formatting a drive so the user can optimize the throughput of the data transfer of the system. The throughput of the system is affected by the controller's turnaround time for the next sector, and the data transfer rate on the host bus. The entire disc should be formatted with the same interleave factor. (See Section 7.0)

6.1.9 CONTROL (BYTE 5)

This field contains the control bits that tells the controller how to react if an error condition is encountered.

FIGURE 13: Control (Byte 5)

BIT	7	6	5	4	3	2	1	0
NAME	DRT	DRR	x	x	x	x	x	x

bit 6	bit 7	
0	0	**Do retry.** Corrected ECC not reported. Pass back good data. Stop on any reported error.
0	1	**No retry.** Pass back good data. Stop on any reported error.
1	0	**Do retry report correction.** Pass back good data.
1	1	**Same as No retry above.**

6.2 ST11R COMMANDS

The general form of an ST11R command is as follows:

FIGURE 14: Commands Format

BIT BYTE	7	6	5	4	3	2	1	0
0	Class			Opcode				
1	LUN			Head Number				
2	Cyl. High			Sector Number				
3	Cylinder Low							
4	Number of Blocks / Interleave							
5	Control							

FIGURE 15: Command Table

Opcode	*Command*
00	Test Drive Ready
01	Recalibrate
02	Reserved
03	Request Sense
04	Format Drive
05	Read Verify
06	Format Track
07	Format Bad Track
08	Read
09	Reassign Sector
0A	Write
0B	Seek
0C	Initialize Drive Characteristics
0D	Read ECC Burst Error Length
0E	Read Sector Buffer
0F	Write Sector Buffer
11	Assign Alternate Track
12	Inquiry Command
E0	RAM Diagnostic
E1	Reserved
E3	Drive Diagnostic
E4	Controller Internal Diagnostics
E5	Read Long
E6	Write Long
E7-FF	Reserved

6.2.1 OPCODE 00: TEST DRIVE READY

This command selects the specified drive and verifies that the drive is ready for access. (Ready true, Seek Complete true, no drive fault)

FIGURE 16: Opcode 00: Test Drive Ready

BIT BYTE	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0
1	LUN			0				
2	0							
3	0							
4	0							
5	0							

The required fields for this command are: Opcode and LUN.

6.2.2 OPCODE 01: RECALIBRATE

This command positions the read/write heads to Track Ø.

FIGURE 17: Opcode 01: Recalibrate

BIT BYTE	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	1
1	LUN			0				
2	0							
3	0							
4	0							
5	0							

The required fields for this command are: Opcode, and LUN.

6.2.3 OPCODE 03: REQUEST SENSE

This command returns four sense bytes to the host as data (C/D deasserted).

FIGURE 18: Opcode 03: Reqest Sense

BIT BYTE	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1	1
1	LUN			0				
2	0							
3	0							
4	0							
5	0							

The required fields for this command are: Opcode and LUN.

The sense bytes are returned in the following format:

FIGURE 19: Sense Data

BIT BYTE	7	6	5	4	3	2	1	0
0	Error Code							
1	LUN			Head Number				
2	Cyl. High		Sector Number					
3	Cylinder Low							

Byte 0: This byte details the nature of the error. The bits are defined as follows:

FIGURE 20: Sense Data: Byte 0

BIT BYTE	7	6	5	4	3	2	1	0
0	BV	x	Error Type		Error Code			

BV (Block Address Valid): This bit indicates that bytes 1 through 3 of the sense information will contain the valid address of the block at which the error occurred.

Error Type (Bits 5 and 4): These bits describe the general type of error. The bits can contain one of the following:

00	Drive-related errors
01	Controller-related errors
10	Command-related errors
11	Miscellaneous errors

Error Code (Bits 3 to 0): This describes the actual error interpretation under each general type of error. Refer to Appendix B for interpretations of this code.

Bytes 1-3: When BV (in byte 0) equals 1, these bytes indicate the ogical unit number of the drive, and the address where the error oc- ;urred.

;.2.4 OPCODE 04: FORMAT DRIVE

'his command formats all the tracks starting from the address in the ;ommand block to the end of the specified drive with the selected track ɔrmat. The sectors will be placed on the tracks according to the in- ɛrleave code specified in the command block and the data fields will e filled with an AA data pattern. Defects will be slipped 1 sector if ıere is 1 defective sector on a track. If there are two or more defects ıen the track will be formatted as a bad track.

FIGURE 21: Opcode 04: Format Drive

BIT BYTE	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	0
1	LUN			Head Number				
2	Cyl. High		0					
3	Cylinder Low							
4	Interleave							
5	0							

The required fields for this command are: Opcode, LUN, Head Number, Cylinder Number, and Interleave.

6.2.5 OPCODE 05: READ VERIFY

This command reads the specified number of blocks starting from the initial block address given in the command block but does not transfer the data to host. This command performs the same retry (including correction) as the Read command.

FIGURE 22: Opcode 05: Read Verify

BIT BYTE	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	1
1	LUN			Head Number				
2	Cyl. High		Sector Number					
3	Cylinder Low							
4	Number of Blocks							
5	Control							

The required fields for this command are: Opcode, LUN, Sector Number, Head Number, Cylinder Number, Number of Blocks and Control.

6.2.6 OPCODE 06: FORMAT TRACK

This command formats the specified track with no flags set in the ID fields of all sectors on the track. It also fills the data field with a AA data pattern. The interleave must be the same for the entire drive.

FIGURE 23: Opcode 06: Format Track

BIT BYTE	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0
1	LUN			Head Number				
2	Cyl. High			0				
3	Cylinder Low							
4	Interleave							
5	0							

The required fields for this command are: Opcode, LUN, Head Number, Cylinder Number, and Interleave.

.2.7 OPCODE 07: FORMAT BAD TRACK

he Format Bad Track command formats the specified track with the ad block flag set in all ID fields on the track. The data pattern from ıe sector buffer is filled in the data field.

FIGURE 24: Opcode 07: Format Bad Track

BIT BYTE	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	1
1	LUN			Head Number				
2	Cyl. High		0					
3	Cylinder Low							
4	Interleave							
5	0							

The required fields for this command are: Opcode, LUN, Head Number, Cylinder Number, and Interleave.

6.2.8 OPCODE 08: READ

This command reads the specified number of blocks starting from the initial block address given in the command block and transfers them to the host.

FIGURE 25: Opcode 08: Read

BIT BYTE	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	0
1	LUN			Head Number				
2	Cyl. High		Sector Number					
3	Cylinder Low							
4	Number of Blocks							
5	Control							

The required fields for this command are: Opcode, LUN, Sector Number, Head Number, Cylinder Number, Number of Blocks and Control

6.2.9 OPCODE 09: REASSIGN SECTOR

FIGURE 26: Opcode 09: Reassign Sector

BIT BYTE	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	1
1	LUN			Head Number				
2	Cyl. High		Sector Number					
3	Cylinder Low							
4	0							
5	0							

The required fields for this command are: Opcode, LUN, Head Number, Cylinder Number, and Sector Number.

After the controller receives the command, it will convert the sector number to a physical sector number based on the interleave factor. This sector is then added to the known defect list. The sector will be flagged as defective on any subsequent format. If the track already has one defective sector, the entire track will be flagged bad on a subsequent format.

6.2.10 OPCODE 0A: WRITE

The Write command gets the data from the host and writes the specified number of blocks starting from the initial address given in the command block.

FIGURE 27: Opcode 0A: Write

BIT BYTE	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1	0
1	LUN			Head Number				
2	Cyl. High		Sector Number					
3	Cylinder Low							
4	Number of Blocks							
5	Control							

The required fields for this command are: Opcode, LUN, Sector Number, Head Number, Cylinder Number, Number of Blocks and Control.

6.2.11 OPCODE 0B: SEEK

This command initiates a seek to the cylinder where the block specified in the command block is located.

FIGURE 28: Opcode 0B: Seek

BIT BYTE	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1	1
1	LUN			Head Number				
2	Cyl. High		0					
3	Cylinder Low							
4	0							
5	Control							

The required fields for this command are: Opcode, LUN, Sector Number, Head Number, Cylinder Number, and Control.

6.2.12 OPCODE 0C: INITIALIZE DRIVE CHARACTERISTICS

This command allows the host to set up drives with different capacities and characteristics.

FIGURE 29: Opcode 0C: Initialize Drive Characteristics

BIT BYTE	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	0	0
1	LUN			0				
2	0							
3	0							
4	0							
5	0							

The required fields for this command are: Opcode and LUN.

6.2.12.1 DRIVE CHARACTERISTICS FORMAT

Eight bytes of parameters will be collected from the host as data (C/D deasserted) using the following format:

FIGURE 30: Drive Characteristics Format

BIT BYTE	7	6	5	4	3	2	1	0
0	Max. Number of Cylinders high							
1	Max. Number of Cylinders low							
2	Max. Number of Heads							
3	Reserved							
4	Reserved							
5	Reserved							
6	Reserved							
7	Reserved							

Upon reset, the controller will default to the characteristics specified in the drive. If no valid geometry is written on the drive then the following defaults will apply:

Maximum number of cylinders:	613
Maximum number of heads:	4
Sectors per track:	25

6.2.13 OPCODE 0D: READ ECC ERROR LENGTH

This command transfers one byte of data to the host. This byte contains the length of the error that the controller detected for a correctable ECC data error during the last Read command.

FIGURE 31: Opcode 0D: Read ECC Error Length

BIT BYTE	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	0	1
1	0							
2	0							
3	0							
4	0							
5	0							

The required field for this command is: Opcode.

6.2.14 OPCODE 0E: READ SECTOR BUFFER

This command reads 512 bytes of data from the sector buffer to the host. No data transfer occurs between controller and drives.

FIGURE 32: Opcode 0E: Read Sector Buffer

BIT BYTE	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	1	0
1	0							
2	0							
3	0							
4	0							
5	0							

The required field for this command is: Opcode.

6.2.15 OPCODE 0F: WRITE SECTOR BUFFER

This command gets 512 bytes of data from the host and writes it to the sector buffer. No data transfer occurs between the controller and drives.

FIGURE 33: Opcode 0F: Write Sector Buffer

BIT BYTE	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	1	1
1	0							
2	0							
3	0							
4	0							
5	0							

The required field for this command is: Opcode.

6.2.16 OPCODE 11: ASSIGN ALTERNATE TRACK

This command formats the alternate track specified in the command with the alternate track bit set in the flag byte of the ID field. The ID bytes are written with the ID of the actual alternate track. The track is interleaved according to the interleave factor in the command byte.

The bad track is formatted with the bad track with alternate bit set in the flag byte of the ID fields. The ID fields are written with the address of the alternate track. The data fields of the bad track and alternate are filled with an AA data pattern.

After a track has been alternated, future read or write access to the primary track will cause the controller to automatically seek to the secondary (alternate) track and do the read/write operations there. This process is transparent to the host. This feature allows the host to perceive the drive as a continuous, error-free media without special software.

FIGURE 34: Opcode 11: Assign Alternate Track

BIT BYTE	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0	1
1	LUN			Head Number				
2	Cyl. High			0				
3	Cylinder Low							
4	Interleave							
5	Control							

The required fields for this command are: Opcode, LUN, Head Number, Interleave and Control.

After the controller recieves the command it will collect the alternate track address as data from the host in the following format.

FIGURE 35: Assign Alternate Track Data

BIT BYTE	7	6	5	4	3	2	1	0
0	0			Secondary Head Number				
1	Cyl. High			0				
2	Secondary Cylinder Low							
3	0							

6.2.17 OPCODE 12: INQUIRY COMMAND

The Inquiry command returns 2 bytes of data. The first byte is the controller type:

80 ST11R

The second byte byte contains the revision level (i.e. 01).

FIGURE 36: Opcode 12: Inquiry Command

BIT BYTE	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	1	0
1	0							
2	0							
3	0							
4	0							
5	0							

6.2.18 OPCODE E0: RAM DIAGNOSTIC

This command performs a data pattern test on the controller memory.

FIGURE 37: Opcode E0: RAM Diagnostic

BIT BYTE	7	6	5	4	3	2	1	0
0	1	1	1	0	0	0	0	0
1	0							
2	0							
3	0							
4	0							
5	0							

The required field for this command is Opcode.

6.2.19 OPCODE E3: DRIVE DIAGNOSTIC

This command performs a diagnostic on the specified LUN. It does a read verify sector 0 on all tracks sequentially. The controller does not perform any write operation during this command. If an error occurs other than flagged bad track or illegal access to alternate track, it is reported and the test is terminated.

FIGURE 38: Opcode E3: Drive Diagnostic

BIT BYTE	7	6	5	4	3	2	1	0
0	1	1	1	0	0	0	1	1
1	LUN			0				
2	0							
3	0							
4	0							
5	Control							

The required fields for this command are: Opcode, LUN, and Control.

6.2.20 OPCODE E4: CONTROLLER INTERNAL DIAGNOSTICS

This command performs the controller internal diagnostics.

FIGURE 39: Opcode E4: Controller Internal Diagnostics

BIT BYTE	7	6	5	4	3	2	1	0
0	1	1	1	0	0	1	0	0
1	0							
2	0							
3	0							
4	0							
5	0							

The required field for this command is: Opcode.

6.2.21 READ LONG / WRITE LONG DATA FORMAT

These commands read blocks of data and ECC information (4 bytes) from the host and transfers them to the disc. For example, a Write Long of a 512-byte sector will read 516 bytes of data from the host, using the last 4 bytes to fill the ECC positions on the disc sector.

512 Bytes of Data	ECC3	ECC2	ECC1	ECC0

6.2.22 OPCODE E5: READ LONG

This command reads 1 block of data and ECC information (4 bytes) from the disc and transfers them to the host. For example, a Read Long of a 512-byte sector will return 516 bytes of data to the host. If an ECC error occurs during the Read Long command, the controller does not attempt to correct the data. No ECC error will be reported.

FIGURE 40: Opcode E5: Read Long

BIT BYTE	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	1	1	1	0	0	1	0	1
1	LUN			Head Number				
2	Cyl. High		Sector Number					
3	Cylinder Low							
4	Number of Blocks = 1							
5	Control							

The required fields for the Read Long command are: Opcode, LUN, Sector Number, Head Number, Cylinder Number, Number of Blocks (1) and Control.

6.2.23 OPCODE E6: WRITE LONG

This command gets 1 block of data and ECC bytes (4 bytes) from the host and writes them to the disc without generating ECC for the data. The format of the data is the same as for the Read Long command above.

FIGURE 41: Opcode E6: Write Long

BIT BYTE	7	6	5	4	3	2	1	0
0	1	1	1	0	0	1	1	0
1	LUN			Head Number				
2	Cyl. High		Sector Number					
3	Cylinder Low							
4	Number of Blocks = 1							
5	Control							

The required fields for the Read/Write Long commands are: Opcode, LUN, Sector Number, Head Number, Cylinder Number, Number of Blocks (1) and Control.

7.0 512 BYTE / SECTOR FORMAT

		Repeated 27 Times						
	GAP 1	SYNC	**ID Field**	GAP 2	**Data Field**	GAP 3		GAP 4
Hex Data	4E	00	-	00	-	0	4E	4E
Num. of Bytes	14	12	10	15	518	2	5	166

SYNC — A field of all zeros to synch the VFO for the ID

ID Field

	PRE ID AM	ID AM	CYL	HD	SECT	FLAG	ID ECC
Hex Data	A1	FE	X	X	X	X	X
Num. of Bytes	1	1	1	1	1	1	4

PRE ID AM — $A1_H$ with a dropped clock to notify the controller that data follows

ID AM — FE_H defining that ID field data follows

CYL — A numerical value in Hex defining the detent position of the actuator

HD — A numerical value in Hex defining the head selected

SECT — A numerical value in Hex defining the sector for this section of the rotation

FLAG

bit 0	Defective Sector
bit 1	Bad Track Without Alternate
bit 2	Track ID = Alternate
bit 3	This is an Alternate Track
bit 4-7	Reserved

ID ECC — Error Correction Code used to verify the validity of the ID field

Data Field

	PRE DATA AM	DATA AM	DATA FIELD	DATA ECC
Hex Data	A1	F8	X	X
Num. of Bytes	1	1	512	4

PRE DATA AM $A1_H$ with a dropped clock to notify the controller that data follows

DATA AM $F8_H$ indicates that user data follows

DATA FIELD User Data

DATA ECC Error Correction Code used to verify the validity of the user data field

APPENDIX A. IBM-PC/XT I/O BUS DEFINITION

FIGURE 42: Component Side Pins

Pin	Signal	Description
A1	-I/O CH CK	Failure in I/O channel or Memory parity
A2	+D7	Data Bit 7 (Most significant bit)
A3	+D6	Data Bit 6
A4	+D5	Data Bit 5
A5	+D4	Data Bit 4
A6	+D3	Data Bit 3
A7	+D2	Data Bit 2
A8	+D1	Data Bit 1
A9	+D0	Data Bit 0 (Least significant bit)
A10	+I/O CH RDY	I/O Channel Ready (no wait state)
A11	+AEN	DMA Channel on
A12	+A19	Address Bit 19
A13	+A18	Address Bit 18
A14	+A17	Address Bit 17
A15	+A16	Address Bit 16
A16	+A15	Address Bit 15
A17	+A14	Address Bit 14
A18	+A13	Address Bit 13
A19	+A12	Address Bit 12
A20	+A11	Address Bit 11
A21	+A10	Address Bit 10
A22	+A9	Address Bit 9
A23	+A8	Address Bit 8
A24	+A7	Address Bit 7
A25	+A6	Address Bit 6

A26	+A5	Address Bit 5
A27	+A4	Address Bit 4
A28	+A3	Address Bit 3
A29	+A2	Address Bit 2
A30	+A1	Address Bit 1
A31	+A0	Address Bit 0

FIGURE 43: Solder Side Pins

Pin	Signal	Description
B1	GND	Ground
B2	+RESET DRV	Positive I/O Reset
B3	+5V	+5 Volt Supply
B4	+IRQ2	Interrupt Request 2
B5	-5V	-5 Volt Supply
B6	+DRQ2	DMA Request 2
B7	-12V	-12 Volt Supply
B8	CRD SLCTD	Card Selected
B9	+12V	+12 Volt Supply
B10	GND	Ground
B11	-MEMW	Memory Write Strobe
B12	-MEMR	Memory Read Strobe
B13	-IOW	I/O Write Strobe
B14	-IOR	I/O Read Strobe 3
B15	-DACK3	DMA Acknowledge 3
B16	+DRQ3	DMA Request 3
B17	-DACK1	DMA Acknowledge 1
B18	+DRQ1	DMA Request 1
B19	-DACK0	DMA Acknowledge 0 (Refresh)
B20	CLOCK	4.77 Mhz System Clock
B21	+IRQ7	Interrupt Request 7
B22	+IRQ6	Interrupt Request 6
B23	+IRQ5	Interrupt Request 5
B24	+IRQ4	Interrupt Request 4
B25	+IRQ3	Interrupt Request 3
B26	-DACK2	DMA Acknowledge 2
B27	+T/C	DMA Terminal Count
B28	+ALE	Address Latch Enable
B29	+5V	+5 Volt Supply
B30	+OSC	14.31818 Mhz Clock
B31	GND	Ground

APPENDIX B. ERROR CODES

SENSE BLOCK ERROR CODES

These error code descriptions are related to Byte 0 of the sense block after the Request Sense command (Class 0, Opcode 03).

FIGURE 44: Type 0 (Drive) Error Codes

0 No error status.

2 No Seek Complete signal from drive.

Possible error causes are:
- Bad Drive
- Bad Control Cable
- Bad Controller

3 Write fault signal received from the drive. This error occurs if the controller detects an active Write Fault signal from the drive while the drive is selected.

Possible error causes are:
- Drive Power supply voltage out of range
- Bad Drive
- Bad Control Cable
- Bad Unit Cable
- Bad Controller

4 Drive not ready. This error occurs if the controller fails to receive drive ready after selection.

Possible error causes are:
- Drive Power supply voltage out of range
- Drive not yet up to operating speed following power on. - Bad Drive
- Bad Control Cable
- Bad Controller

9 Drive not Available.

- Drive not attached
- Drive not powered on

FIGURE 45: Type 1 (Controller) Error Codes

10 ID field read error. During a data transfer ot format command, address marks were detected, but the target sector was not found and an ECC error occured on one or more ID fields.

Possible error causes are:
- Media defect on drive
- Bad Drive
- Bad Controller

Media defects may be overcome by deleting the defective sectors from system use.

11 Uncorrectable data error in the data field. The controller detects a data error that could not be corrected using ECC.

Possible error causes are:
- Media defect on drive
- Bad Drive
- Bad Controller

Media defects may be overcome by deleting the defective sectors from system use.

12 Sector address mark not found. The controller did not detect an address mark (AM) from the drive within its timing window. An address mark is a special recording pattern preceeding the ID field of a sector. The AM is only written at format time. The AM tells the controller where new sectors start. The error may occur during any data transfer or format command. The error may mean that no address marks were detected on the track, or the target sector address mark was not detected.

Possible error causes are:
- Media defect on drive
- Drive has not been formatted
- Bad Drive
- Bad Unit Cable (J2, J3)
- Bad Controller

Media defects may be overcome by deleting the defective sectors from system use.

13 Data address marker not found.

14 Target sector not found. The target sector was not located within two revolutions of the disk. This error usually occurs when there is a media defect in the address mark field of the target sector.

Possible error causes are:
- Media defect on drive
- Bad Drive
- Bad Controller

Media defects may be overcome by deleting the defective sectors from system use.

15 Seek error. After a seek, the target disk address did not match the ID address read from the disk. Either the cylinder or head bytes did not match.

Possible error causes are:
- Incorrect seek option specified in the command
- Bad Drive
- Bad Control Cable (J1)
- Bad Controller

Media defects may be overcome by deleting the defective sectors from system use.

18 Correctable data field error. The controller detected a media error while reading that was corrected by ECC. This error code informs the host software that error correction has taken place. This is the only error where the data is passed to the host before returning the error status.

19 Track is flagged bad. The last data transfer command encountered a track that had been flagged as defective using the format bad track command. Host software is responsible for insuring that deleted tracks are never accessed.

1C Alternate track not flagged as an alternate.

1E Illegal access to an alternate track.

1F Recovery mode not available.

FIGURE 46: Type 2 (Command) Error Codes.

20 Invalid command. The controller has received an invalid commnad from the host.

21 Illegal disc address. The controller detected an address that is beyond the maximum address.

22 Illegal parameter. The controller detected an invalid passed parameter.

FIGURE 47: Type 3 (Misc.) Error codes.

30 RAM error. The controller detected a data error during the RAM sector-buffer diagnostic.

APPENDIX C. PHYSICAL CYLINDER 0

On all drives, cylinder zero is reserved for the controller and will be designated as logical cylinder minus 1. Logical cylinder 0 starts at physical cylinder 1.

APPENDIX D. BIOS SUPPORT

INTERRUPT 13_H

This routine is executed after the IBM hard disc routine and takes charge of the Int 13_H vector. If the request is for diskette (DL $< 80_H$), the diskette routine is executed. If DL $> = 80_H$, then the request is for a hard disc. The IBM discs will be assigned the lower numbers while the higher numbers will be handled by this SCSI driver.

INPUT

(AH = Hex Value)

(AH) = 00	Reset Disc (hard and floppy)
(AH) = 01	Read the Status of the Last Disc Operation into (AL)
(AH) = 02	Read Sectors
(AH) = 03	Write Sectors
(AH) = 04	Verify Sectors
(AH) = 05	Format Track
(AH) = 06	Format Bad Track
(AH) = 07	Format Drive Starting at Specified Track
(AH) = 08	Return Current Drive Parameters
(AH) = 09	Initialize Drive Characteristics
(AH) = 0A	Read Long
(AH) = 0B	Write Long
(AH) = 0C	Seek
(AH) = 0D	Reset (hard disc only)
(AH) = 0E	Read Sector Buffer
(AH) = 0F	Write Sector Buffer
(AH) = 10	Test Drive Ready
(AH) = 11	Recalibrate
(AH) = 12	Controller RAM Diagnostic
(AH) = 13	Drive Diagnostic
(AH) = 14	Controller Internal Diagnostic
(AH) = 15	Read DASD Type
(AH) = 55	Seagate Extended Interupt 13_H Functions

SEAGATE EXTENDED INTERUPT 13_H FUNCTIONS

AL = 00
AL = 10 Reserved

AL = 11 Inquiry data to ES:BX (Psuedo-Inquiry SCSI)

Returns device type quailfier, drive model no. and drive serial no.

AL = 12 Special ST11x/12x Mode Select

(not currently implemented, returns good status)

AL = 13 Set BIOS Flag 0 bits

For a true condition, the bits have the following meaning:

7 user-entered defects
6 Reserved
5 drive was initialized using BIOS routine (INIT-DRV)
4 recovery mode enabled for this drive
3 manufacturer's defects present on minus 1 track
2 drive geometry present on minus 1 track
1 drive is "initialized"
0 Reserved

Note: Bit 1 is set at the completion of a format drive command.

AL = 14 Returns controller identification (model #, BIOS rev.)

DH = 0 returns BIOS rev. in CL, CH
DH = 1 returns microcode rev. in CL, CH

Exit:

AX = $0FEDB_H$ (ST11R)
BL = total number of hard discs in system
BH = number of drives connected to this controller
CL = major revision number of BIOS/microcode (see DH above)

CH = minor revision number of BIOS/microcode (see DH above)
DH = LUN (same as DL upon entry of INT 13)

AL = 15 Start/Stop drive (Recal/Park)

CH = 02_H 200 series drive
CH = 40_H 4000 series
DH = 00_H for Stop (park)
DH = 01_H for Start (recal)

AL = 16 Reserved

AL = 17 Format minus 1 cylinder

BX = 5354_H (Safety signature)
CH = interleave factor DH = head

AL = 18 Read sectors from minus 1 cylinder

ES:BX = data buffer
CL = starting sector
CH = block count DH = head

AL = 19 Reserved

AL = 1A Write sectors to minus 1 cylinder

ES:BX = data buffer
CL = starting sector
CH = block count DH = head

AL = 1B
AL = FF Reserved

REGISTERS USED FOR FIXED DISC SUPPORT

(DL) Drive Number 80 + Disc Number (0-N)

(DH) Head Number

(CH) Cylinder Number

(CH) Sector Number

Note: High 2 bits of cylinder number are placed in the high 2 bits of the CL register (10 bits total).

(AL) Number of sectors ($01\text{-}80_H$, for read/write long $1\text{-}79_H$) (interleave value for format $1\text{-}16_H$)

(ES:BX) Address of buffer for reads, writes and inquiries (not required for verify)

Output

AH Status of current operation
status bits ore defined in the equates below.

CY = 1 successful operation (AH = 0 on return)
= 0 failed operation (AH has error code)

Note Error 11_H indicates that the data read had a recoverable error which was corrected by the ECC algorithm. The data is probably good, however the BIOS routine indicates an error to allow the controlling program a chance to decide for itself. The error may not reoccur if the data is rewritten.

If drive parameters were requested:

DL Number of acknowledging drives attached

DH Maximum value for head number

CH Maximum value for cylinder number

CL Maximum value for sector number and cylinder number high bits

Registers will be preserved except when they are used to return information.

Note: If an error is reported by the disc code, the appropriate action is to reset the disc, then retry the operation.

INTERUPT 13_H ERROR CODE

$0FF_H$	Sense operation failed
$0CC_H$	Write Fault on drive
$0BB_H$	Undefined error occurred
$0AA_H$	Drive not ready
80_H	Attachment failed to respond
40_H	Seek operation failed
20_H	Controller has failed
11_H	ECC corrected data error
10_H	Bad ECC on disc read
$0E_H$	Drive not present
$0D_H$	Attempt to directly access an alternate track
$0B_H$	Bad track flag detected
$0A_H$	Bad sector flag detected
09_H	Attempt to DMA across 64K boundary
07_H	Drive parameter activity failed
05_H	Reset failed
04_H	Requested sector not found
03_H	Write protect error
02_H	Address mark not found
01_H	Bad command passed to disc I/O
0_H	Bad sector flag detected

NOTES

NOTES

Seagate Publication: 36030-001, Revision A
920 Disc Drive, Scotts Valley, California 95066-4554, USA