SIGMA 5–9 DIAGNOSTIC PROGRAM, MAGNETIC TAPE LIBRARY CONTROL PROGRAM 1

SIGMA 5–9 RELOCATABLE DIAGNOSTIC PROGRAM LOADER 2

SIGMA 5–9 DIAGNOSTIC PROGRAM MONITOR (DPM) 3

SIGMA 5–9 KEYBOARD PRINTER (ASR/KSR) 4

SIGMA 5–9 COMPREHENSIVE CARD EQUIPMENT (TEST) 5

SIGMA 5–9 COMPREHENSIVE RAD/CARTRIDGE DISK TEST (COMPR RAD) 6

SIGMA 5–9 REMOVABLE DISK STORAGE TEST (724X) 7

SIGMA 5–9 REMOVABLE DISK STORAGE TEST (7270/71) 8

SIGMA 5–9 ROTATING MEMORY TEST (726X/7275) 9

SIGMA 5–9 9-CHANNEL MAGNETIC TAPE TEST 10

SIGMA 5–9 7-CHANNEL MAGNETIC TAPE TEST 11

SIGMA 5–9 COMPREHENSIVE LINE PRINTER TEST (744X-745X) 12

SIGMA 5–9 LINE PRINTER DIAGNOSTIC (746X) 13

SIGMA 5–9 INTERFACE AND SWITCH REFERENCE DATA 14

# Section 1

# SIGMA 5 - 9
DIAGNOSTIC PROGRAM
MAGNETIC TAPE LIBRARY
CONTROL PROGRAM

## PROGRAM NO. 705691

## Section 1

## CONTENTS

| Chapter | | Page |
|---|---|---|
| I | INTRODUCTION | 1-1 |
| | General | 1-1 |
| | Operating Procedure | 1-1 |
| | To Load Programs from Magnetic Tape | 1-1 |
| | Input Procedure | 1-1 |
| | Program Name Listing Procedure | 1-1 |
| | Procedure to Follow When Operator Does Not Know or Cannot Remember Program Name | 1-2 |
| | Procedure to Follow When Operator Remembers Partial Program Name | 1-2 |
| | Other Operating Features | 1-2 |
| II | OPERATING PROCEDURE | 1-3 |
| | General | 1-3 |
| | Updating Programs to the Magnetic Tape Library | 1-3 |
| | Adding Programs to the Magnetic Tape Library | 1-3 |
| | Replacing Programs on the Magnetic Tape Library | 1-3 |
| | Deleting Programs from the Magnetic Tape Library | 1-3 |
| | Copying the Magnetic Tape Library | 1-3 |
| | Verifying the Updated Magnetic Tape Library | 1-4 |
| III | CONTROL CARD FORMATS | 1-5 |
| | Card Formats | 1-5 |
| | Adding and/or Replacing Program Control Card | 1-5 |
| | Delete Program Control Card | 1-5 |
| | End Card | 1-5 |
| | Deck Set-Up Adding and/or Replacing Programs | 1-5 |
| | Deck Set-Up Deleting Program | 1-5 |
| | Deck Set-Up Copying Programs | 1-6 |
| | Messages | 1-6 |

## Chapter I
## INTRODUCTION

### 1-1 GENERAL

This document covers the operating procedure, updating procedures, copy procedure and the various messages associated with the magnetic tape library. All procedures, with the exception of the operation procedure, are tutorial.

### 1-2 OPERATING PROCEDURE

### 1-3 TO LOAD PROGRAMS FROM MAGNETIC TAPE

a. Remove write ring from tape reel and mount to tape unit 0.

b. If the systems configuration prohibits the contents of the upper core from being destroyed (for example, shared memory system), set sense switch 1 and reset sense switches 2, 3, and 4. Otherwise, reset all sense switches.

c. Execute a LOAD from the processor control panel CP). If sense switch 1 is set, the program will come to WAIT. Enter the maximum memory address to general register 1, reset sense switch 1 and clear the WAIT condition. If sense switch 1 is reset, the program will not come to a WAIT.

d. A message giving the magnetic tape library title will be typed to the operator keyboard, KSR, and control will be given to the KSR for input.

e. Type in the program name, followed by a NL (New Line-EBCDIC 15) character. The program will be loaded, the tape rewound and control transferred to the program.

f. Refer to individual program write-ups for each program.

Further explanations assume that the program has been loaded and is ready to receive data from the operator.

### 1-4 INPUT PROCEDURE

a. Valid inputs to the KSR can be a program name, a simple NL (New Line - EBCDIC 15) character, or a utility request for UPDATE.

b. All valid KSR input will be terminated with termination character, NL (New Line - EBCDIC 15).

c. Input errors to the KSR can be cleared by the EOM (End of Message - EBCDIC 08) character if the EOM character is input before the termination character (NL).

### 1-5 PROGRAM NAME LISTING PROCEDURE

a. A message giving the magnetic tape library title will be typed to the operator keyboard, KSR, and control will be given to the KSR for input.

b. Type in a NL (New Line - EBCDIC 15) character.

c. Program name, revision level, loader type, if the program is interfaced to the diagnostic program monitor, and the starting address of the program will be printed.

The program name will be listed in the following format:

XXXX. . . XXX A B C YYYYY

| | |
|---|---|
| XXXX. . X | Program name. This is the name used in calling the program from the magnetic tape library. |
| A | Program revision level. This should always correspond to the latest revision level. The revision level is not required as a part of the name to call a program. |
| B | Loader Type. If this field is blank, it means that the program uses the Relocatable Diagnostic (Sigma 5 and 7 Program No. 704356, Sigma 2 and 3 Program No. 705299) Loader Program. If this field prints letter L, it means that the program uses the CPU Loader. |
| C | Diagnostic Program Monitor. If this field is blank, it means that the program is a stand-alone program and does not interface to the diagnostic program monitor. (Refer to Sigma 5 and 7 Program No. 705682, Sigma 2 and 3 Program No. 705681). If this field prints letter M, it means that the program uses the diagnostic program monitor. |
| YYYYY | The starting address of the program in hexadecimal. |

## 1-6 PROCEDURE TO FOLLOW WHEN OPERATOR DOES NOT KNOW OR CANNOT REMEMBER PROGRAM NAME

a. List program names as described in paragraph 1-5.

b. Find the appropriate name. Input the name to the KSR, followed by a NL (New Line) character. The program will be loaded, the tape rewound, and control transferred to the program.

## 1-7 PROCEDURE TO FOLLOW WHEN OPERATOR REMEMBERS PARTIAL PROGRAM NAME

a. Type in the partial program name followed by a NL (New Line) character.

b. All program names with a matching partial program name will be listed on the operator keyboard, KSR. Then the partial name will be typed on the KSR. The user will complete the program name and terminate input with the NL (New Line) character. The program will be loaded, the tape rewound, and control transferred to the program.

## 1-8 OTHER OPERATING FEATURES

All message outputs can be terminated by the user by depressing the BREAK key.

## Chapter II

## OPERATING PROCEDURE

### 2-1 GENERAL

The magnetic tape library updating function requires a minimum of two tape drives. The availability of a third drive can reduce all operator interventions. The updating function covers the program adding feature, the program deleting feature, and the program replacing feature, all of which are very similar operations.

### 2-2 UPDATING PROGRAMS TO THE MAGNETIC TAPE LIBRARY

a. The master tape is assumed to be mounted to tape unit 0 with the write enable ring removed. Insert write ring to scratch tape and mount to unit 1. If a third drive is available, insert a write ring to the tape that the new magnetic tape library is to go on and mount to unit 2.

b. Place an update control card in front of each object deck and place an update termination card at the bottom of the deck. See paragraph 3-1 for control card format and description. The deck must be sequenced in the same order that the program names exist on the library tape.

c. Stack the card deck in the card reader and set card reader ready.

d. Type in UPDATE followed by a NL (New Line) character.

e. The cards will be read, and the updating will start. Users with only two tape drives will be alerted to leave the scratch tape on unit 1 and mount a scratch tape (the tape that is to be designated as the new master) on unit 2. To do this, the master must be removed from unit 0. Users with three tape drives will ignore this message.

f. The completion of the updating of programs is indicated by a message informing the operator that the copy portion of update is completed on unit 2.

g. The operator now has the option of verifying the new master tape or of taking the new master without verification. Users wishing to verify the new tape should refer to paragraph 2-7.

### 2-3 ADDING PROGRAMS TO THE MAGNETIC TAPE LIBRARY

a. To add programs to the magnetic tape library, the operator must make certain that the first 38 characters of the program name being assigned to the program, in the program name field on the control card, are unique. The operator should then follow the instructions in paragraph 2-2 to perform the update. See Sigma 2 for deck set-up.

b. If the operator has any doubts about the name, check all program names by listing them as described in paragraph 1-5.

### 2-4 REPLACING PROGRAMS ON THE MAGNETIC TAPE LIBRARY

a. To replace programs on the magnetic tape library, the operator must make certain that the first 38 characters of the program name, in the program name field of the control card, correspond to the existing name of the program to be replaced. The new revision level letters should reflect a difference of one level. Refer to paragraph 3-5 for a graphic depiction of deck set-up.

b. When the program names have been checked, follow the instructions in paragraph 2-2 to perform the update.

c. If the operator has any doubts about the name, list the program name as described in paragraph 1-5.

### 2-5 DELETING PROGRAMS FROM THE MAGNETIC TAPE LIBRARY

a. Deleting programs from the magnetic tape library does not require object decks behind the control cards as described in step (b) of paragraph 2-2.

b. To delete programs from the magnetic tape library, the operator must make certain that the first 38 characters of the program name, in the program name field of the control card, correspond to the name of the program to be deleted. Refer to paragraph 3-5 for an illustration of deck set-up.

c. Stack the delete control cards, place a termination card at the bottom of the deck and follow the instructions of paragraph 2-2 to perform the update.

d. If the operator has any doubts about the name, list the program name as described in paragraph 1-5.

### 2-6 COPYING THE MAGNETIC TAPE LIBRARY

a. Copying the magnetic tape library is accomplished through the update mechanism and only quires a termination card to be put in the card reader. Refer to paragraph 3-7 for an illustration of deck set-up.

b. Follow instructions in paragraph 2-2 to perform the copy.

## 2-7 VERIFYING THE UPDATED MAGNETIC TAPE LIBRARY

a. After the magnetic tape library addition, deletion and/or copying function is completed, the operator may verify his new master tape.

b. To verify the updated magnetic tape, leave the new master tape on unit 2. If the user is only using two tape drives, mount the old master tape on unit 0. If three tape drives are available, leave the tapes in the original updating configuration and restack the cards in the hopper.

c. When the verification is completed, the operator will be notified by a message informing him that update is complete and that he should remove the write ring from the tape on unit 2.

Copy Tape to Tape !COPY

## Chapter III

## CONTROL CARD FORMATS

### 3-1 CARD FORMATS

There are two types of card formats, the updating card format and the termination card format. Column 1 is the updating control character field. Columns 2 through 39 are the program name field. Columns 40 through 59 are the revision letter and date field. Columns 60 is the loader type field. Column 65 is the diagnostic program monitor field. Columns 70 through 74 are the starting address field.

### 3-2 ADDING AND/OR REPLACING PROGRAM CONTROL CARD

a. Column 1 must contain a + (plus).

b. Columns 2 through 39 must contain the program name. When adding programs to the magnetic tape library, the name in this field must be unique from any name currently on the magnetic tape library. When replacing or deleting programs on the magnetic tape library, the name in this field must be identical to an existing name on the magnetic tape library.

Columns 40 through 59 should contain the letters representing the program revision level and a date, if desired.

c. Column 60 must be left blank if the program uses the meta-symbol loader (Program No. 704356). Column 60 must contain an L if the program uses the CPU format loader. (Program No. 704029).

d. Column 65 must be left blank if the program is not interfaced to the Diagnostic Program Monitor (Program No. 705682). Column 65 must contain an M if the program is interfaced to Diagnostic Program Monitor.

e. Columns 70 through 74 must contain the starting address of the program in hexadecimal.

### 3-3 DELETE PROGRAM CONTROL CARD

a. Column 1 must contain a - (minus).

b. Other fields are identical to the description in paragraph 3-2.

### 3-4 END CARD

a. All END cards have the same format.

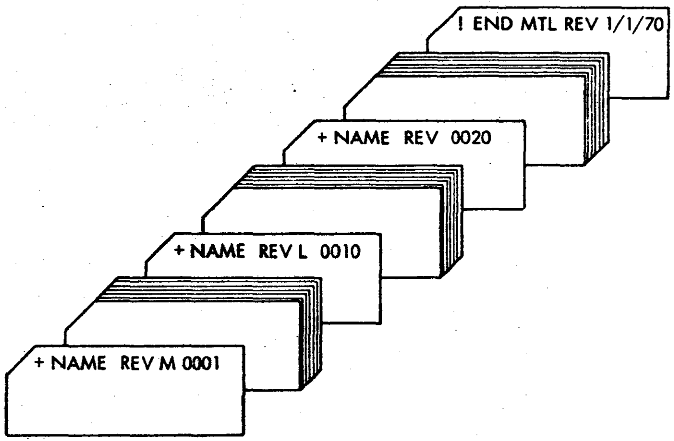
b. Column 1 must contain an ! (exclamation).

c. Columns 2 through 39 must contain the magnetic tape library title.

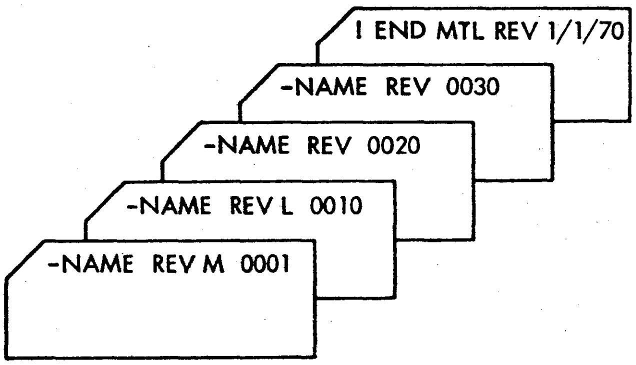
d. Columns 40 through 59 must contain the magnetic tape library revision level and creation date.

This information will become the new title which is printed on the operator keyboard, KSR, when the magnetic tape library is loaded.

### 3-5 DECK SET-UP ADDING AND/OR REPLACING PROGRAMS



### 3-6 DECK SET-UP DELETING PROGRAMS



## 3-7 DECK SET-UP COPYING PROGRAMS

```
! END MTL REV 1/1/70
```

## 3-8 MESSAGES

Most messages are self-explanatory. Those messages which require operator intervention will continue to print in 30-second intervals until the operator intervenes. In the cases of card reader errors, the updating can proceed by taking the card which causes the error and restacking it in the card reader.

# Section 2

# SIGMA 5 - 9
# RELOCATABLE
# DIAGNOSTIC PROGRAM LOADER

## PROGRAM NO. 704356

## Section 2

## CONTENTS

Page

Program Objectives . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 2-1
Operating Requirements and Specifications . . . . . . . . . . . . . . . . . . . . . . . 2-1
  Required Equipment . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 2-1
  Loading Procedures . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 2-1
  Program Options . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 2-1
Program Waits and Loops . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 2-1
Usage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 2-2

# 2. SIGMA 5–9 RELOCATABLE DIAGNOSTIC PROGRAM LOADER

## Chapter I

## PROGRAM OBJECTIVES

### OGRAM OBJECTIVES

The Sigma 5 through 9 Relocatable Diagnostic Program Loader is designed to use a minimum instruction repertoire and to provide adequate flexibility to the user. The program provides the capability to detect sequence errors, checksum errors, and many input device errors. In addition, the loader protects itself from self destruction. The loader may be used as a subroutine to load additional programs. This is described in the usage section.

### OPERATING REQUIREMENTS AND SPECIFICATIONS

#### Required Equipment

Sigma 5 through 9 with minimum 4K memory. ASR/KSR for message input/output if relocation is desired. Paper tape reader, card reader, or magnetic tape for program input.

#### Loading Procedure

1. Set compute switch to idle.
2. Clear memory by simultaneously pressing CPU/CLEAR and CPU/RESET switches for Sigma 5/6/7 or by pressing the memory clear switch for Sigma 8/9.

. Set the unit address switches to the address of the desired input peripheral device.

4. Set the watchdog timer switch to halt.
5. Set the interleave switch to the desired position, interleave or diagnostic mode.
6. Set the parity error mode switch to continue.
7. Set clock mode switch to continue.
8. Set the address stop switch to the off position.
9. For Sigma 9 press not normal switch and check for normal indication.
10. Set sense switches for desired options (see program options).
11. Press I/O reset and then load switch.
12. Move compute switch from idle to run.

    At this point the program will be loaded according to the sense switch settings.

#### rogram Options

Sense Switch 1:

OFF Loading will complete without waits.

ON Loading will halt after the loader has been stored in lower core. At this time a prompt message will be output to the ASR/KSR. The prompt messages are:

Message:

Relocation bias for resident loader in hex

Response:

1. (Hex value) N/L - This value will be the starting location of the loader.
2. A N/L with no preceding characters tells the loader to place itself at the top of memory.
3. An EOM specifies that the preceding input should be disregarded.

Message:

Relocation bias for diagnostic program in hex

Response:

1. (Hex value) N/L - This value will be the starting location of the program to be loaded.
2. A N/L with no preceding characters tells the loader to use the bias where the program has assembled.
3. Same as 3. above.

Message:

Alternate input device address

Response:

1. (Hex value) N/L - This is the address that the diagnostic program will be loaded from.
2. A N/L with no preceding characters tells the loader to use the address indicated by the unit address switches.
3. Same as 3. above.

Sense Switch 2:

OFF Loading will complete without waits.

ON After loading is complete and just before the loader transfers control to the loaded program, SS2 is checked and the loader comes to a wait with the contents of register 12 pointing to the starting address. Indicated on the end card. Clearing the wait executes a branch indirect on register 12.

PROGRAM WAITS AND LOOPS

When a wait occurs at location 000F0 or 00149, the ASR/KSR did not respond to device address 1. Store correct address into register 2 and clear wait.

USAGE

Use as a subroutine to load additional object modules. Register 1 contains the starting location of the loader. This must be saved to communicate with the loader. The contents of the location pointed to by register 1 is the address of table. The contents of table are as follows:

| | | |
|---|---|---|
| Table<br>Table+1 | 0<br>0 | These locations are for future expansion. |
| Table+2<br>Table+3 | Loader Address<br>BA of Loader | These are the values that are used to protect the loader from self destruction.<br>These values may be altered to protect additional memory locations. |
| Table+4 | Teletype Address | The device address used to notify the operator of errors that occur during the load operation. |
| Table+5 | LIA Address | This address is where processing starts. |
| Table+6 | LIC Address | This address contains a NOP and could be used to insert a branch instruction for user interpretation of buffer data, input by the loader. |
| Table+7 | Expr Address | Address of an useful subroutine. |
| Table+8 | FOB Address | Address of an useful subroutine. |
| Table+9 | ENDPROGRAM | First location above loader (Table +2)+(Table +9)=First unused location. (Table+2) +478=Last unused location. |

Other useful locations are:

| | | |
|---|---|---|
| SCNT | Table Address | SCNT is the label that is attached to location indicated by register 1. |
| SCNT+1 | I/O Return Address | When input is done by the user, this is where sequence and checksum checking starts. |
| SCNT+2 | IOCD | IOCD used by the loader SIO. |
| SCNT+3 | * | |
| SCNT+4 | Address of the loader SIO | |
| SCNT+5 | Input Device Address | |
| SCNT+6 | Last Memory Address | |
| SCNT+7 | Buffer Address used by the loader for input. | |

When using the loader as a subroutine, register 11 should contain the address that the loader returns to. If register 11 contains a zero, the loader goes to the address indicated on the end card of the object deck. Register 0 must contain the amount of relocation bias to be added to the object module to be loaded. This value can not be negative. An example would be:

```
LI,0      RELOCATIONBIAS
LI,1      LOADERADDRESS
BAL,11    8,1
GO                  The loader will return here.
```

# Section 3

# SIGMA 5 - 9
# DIAGNOSTIC PROGRAM MONITOR (DPM)

## PROGRAM NO. 705682

## Section 3

## CONTENTS

Page

Subject Model . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 3-1
Program Loading Instructions . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 3-1
Required Equipment . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 3-1
Directives . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 3-2
Loader Error Messages . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 3-4
Monitor Error Messages . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 3-4
Start Procedure . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 3-5
Termination Indication . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 3-5
Restart Procedure . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 3-5
Remote Facility . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 3-6
PCP Facility . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 3-7
Command Doubleword Format . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 3-9
Input/Output Instructions . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 3-10
General Condition Codes . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 3-10
Status Bits for I/O Instructions . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 3-11
Monitor Link Table (MLT) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 3-12
Program Interface Table (PIT) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 3-14

# 3. SIGMA 5–9 DIAGNOSTIC PROGRAM MONITOR (DPM)

**SUBJECT MODEL** -- This program is used as the operating monitor program for DPM peripheral test programs. Refer to the individual test programs for further information.

**REQUIRED EQUIPMENT** -- Minimum Memory Size: 16K; Input Device: Card Reader, Paper Tape Reader or Magnetic Tape Input; Output Device: Keyboard Printer or Line Printer. The remote facility is available in systems with more than 16K of memory.

## PROGRAM LOADING INSTRUCTIONS

From Magnetic Tape Library

- Mount tape on unit 0 (without write-ring) and set its address on the control panel
- Reset all sense switches
  Exception: Set sense switch 1 if the upper core protection is desired
- Execute a LOAD from the control panel:
  1. If sense switch 1 is reset, the loader is loaded to the upper end of memory.
  2. If sense switch 1 is set, the following occurs:
     a. If the keyboard printer is not on IOP 0, device address 1, the program will come to a wait. Enter the correct address into register 2 and clear the wait.
     b. If the keyboard printer is at the standard address or the correct address has been entered, the following three messages will be printed: (Reset sense switch 1 once printing has begun)
        - RELOCATION BIAS FOR RESIDENT LOADER IN HEX; Type in the hexadecimal memory address of the first location the resident loader is to occupy in memory followed by a carriage return. Minimum address is 400 and the maximum address is IFE00 or maximum memory size less 200.
        - RELOCATION BIAS FOR DIAGNOSTIC PROGRAM IN HEX; DPM programs may not be relocated, therefore type in only a carriage return.
        - ALTERNATE INPUT DEVICE ADDRESS; To continue loading, type in only a carriage return.
        - Loading will continue following the third entry

  A message giving the tape library title and revision letter should be typed out from the keyboard

- Type in the program name desired and a N/L
  1. If a listing of all programs on tape is desired, type: !LIST, ADR, N/L N/L where ADR = output device address in hex. Default is to the keyboard printer.
  2. If the full name cannot be remembered, type in the partial name and a N/L. Complete the partial name by selecting the desired name from the suggested names typed out by program.
- To make a copy of the MTL, mount MTL on unit 0 and execute a LOAD. Mount scratch tape on unit 1 and make ready. Type: !COPY. The MTL tape will be copied to the scratch tape and verified.

From Card Deck (same for Paper Tape)

- Place card deck in Card Reader and set its address on the control panel
- Reset all sense switches
  Exceptions: Set sense switch 1 if the upper core protection is desired or sense switch 2 if register control is desired by the keyboard printer (ASR DPM) test, program no. 705651
- Execute a LOAD from the control panel:
  1. If sense switch 1 is reset, no wait will occur unless sense switch 2 is set (see 3.)
  2. If sense switch 1 is set, the following occurs:
     a. If the keyboard printer is not on IOP 0, device address 1, the program will come to a wait. Enter the correct address into register 2 and clear the wait.
     b. If the keyboard printer is at the standard address or the correct address has been entered, the following three messages will be printed: (Reset sense switch 1 once printing has begun)
        - RELOCATION BIAS FOR RESIDENT LOADER IN HEX; Type in the hexadecimal memory address of the first location the resident loader is to occupy in memory, followed by a carriage return. Minimum address is 400 and the maximum address is IFE00 or maximum memory size less 200.
        - RELOCATION BIAS FOR DIAGNOSTIC PROGRAM IN HEX; DPM programs may not be relocated, therefore type in only a carriage return.
        - ALTERNATE INPUT DEVICE ADDRESS; To continue loading, type in only a carriage return.
        - Loading will continue following the third entry
  3. If sense switch 2 is set, the program comes to a wait:
     - Clear the wait, the program will come to a second wait
     - Enter X'FFFFFFFF' into register 0
     - Reset sense switch 2
     - Clear the wait
     - The test program is automatically loaded (without requiring a "LOAD" directive) and comes to a wait.

  - The KSR/ASR program will operate in register control mode.

  Exceptions: Sense switch 2 option was used or the keyboard is not on IOP 0, device address 001.

  1. If sense switch 2 option was used, "LOAD" directive will automatically be performed
  2. If keyboard is not address 001, the program will come to a wait:
     - Enter IOP and device address of the keyboard into register 2, i.e. X'105'
     - Clear the wait
     - "!" should be typed on keyboard

- Type in "LOAD" and a "Space Character" if sense switch 2 option was not used. A message giving the program name and revision letter should be typed out

**DIRECTIVES** –directives are entered after a "!" is typed out

| Name | Format | Parameter | | | |
|---|---|---|---|---|---|
| | | ID | Definition | Value Range | Standard Value (default) |
| Monitor Directives | | | | | |
| Message Output Device | MOD, A, IXX | A | Device type | TY (KSR/ASR)<br>LP (Line Printer) | TY |
| | | I | IOP number | 0 ~ 1F | 0 |
| | | XX | Device controller address | 00 ~ 7F | 01 |
| Message Input Device | MID, A, IXX | A | Device type | TY (KSR/ASR)<br>CR (Card Reader)<br>PR (Paper Tape Reader) | TY |
| | | I | IOP number | 0 ~ 1F | 0 |
| | | XX | Device controller address | 00 ~ 7F | 01 |
| Dump Memory | DMP, H1, H2 [ ,C ] | H1 | Starting address | 0 ~ FFFFF | |
| | | H2 | Ending address | 0 ~ FFFFF | |
| | | C | Relative address flag (displacement from the starting address) | C ≠ 0 | 0 |
| Dump Memory on ASR/KSR | TDMP, H1, H2 [ ,C ] | H1 | Starting address | 0 ~ FFFFF | |
| | | H2 | Ending address | 0 ~ FFFFF | |
| | | C | Relative address flag (displacement from the starting address) | C ≠ 0 | 0 |
| Alter Memory | ALT, H1, X1 [ ,...,XN] | H1 | Memory address | 0 ~ FFFFF | |
| | | X1<br>.<br>.<br>.<br>XN | Values to be inserted into memory starting from H1 | N ≤ 254 | |
| Load Program (from object deck) | LOAD, [H1] | H1 | Load device address | 0 ~ 1FFF | Initial loading device |
| Program Directives – Environmental Directives | | | | | |
| System Environment | SYST, D1, D2, H3, H4,...,HN | D1<br>D2<br>H3<br>H4<br>.<br>.<br>.<br>HN | Device or controller model number | The 'SYST directive interpretation and value ranges are supplied by the program loaded by the 'LOAD' directive. Refer to the applicable diagnostic program reference manual. Also, the diagnostic program will generally print its 'SYST' format following the 'LOAD' operation. | |
| Program Directives – Testing Directives | | | | | |
| Test Directives (used to test a device or to modify test data) | Determined by Diagnostic Program | | Supplied by the Diagnostic Program. Refer to the applicable Diagnostic Program Reference Manual. | | |
| Note: Parameter of any directive beginning with a D means decimal, with an H means hexadecimal. | | | | | |

(Continued)

**DIRECTIVES** (Continued)

| Name | Format | Parameter | | | |
|---|---|---|---|---|---|
| | | ID | Definition | Value Range | Standard Value (default) |
| Monitor Directives (Available Only If Memory Size > 16K). | | | | | |
| These directives simulate PCP control and provide remote troubleshooting facilities. | | | | | |
| Turn On Pseudo Sense Switches | SON [,D1, D2, D3, D4] | D1 | Sense switch number | 1 ~ 4 | D1 thru D4 =0, display pseudo sense switches |
| | | D2 | Sense switch number | 1 ~ 4 | |
| | | D3 | Sense switch number | 1 ~ 4 | |
| | | D4 | Sense switch number | 1 ~ 4 | |
| Turn Off Pseudo Sense Switches | SOFF [,D1, D2, D3, D4] | D1 | Sense switch number | 1 ~ 4 | D1 thru D4 =0, display pseudo sense switches |
| | | D2 | Sense switch number | 1 ~ 4 | |
| | | D3 | Sense switch number | 1 ~ 4 | |
| | | D4 | Sense switch number | 1 ~ 4 | |
| Use Real Sense Switches | SSWC | | | | |
| Simulate PCP Reset | RES | | | | |
| Set Address Stop | STOP [,H1] | H1 | Stop address | 0 ~ FFFFF | D1 = 0; Remove address stop |
| Continue with next instruction after program wait or address stop (from stop directive) | GO (continue with next location after wait)<br>GO1 (continue with next location +1 after wait) | | | | |
| Start Program at Location n. | BR, H1 | H1 | Branch address | 0 ~ FFFFF | Note: Registers or flags may not be set up correctly. |
| Allow Remote User to Log On | LOG, A, H2, H3 | A | 4-character password | Alpha/num characters | |
| | | H2 | COC address | 0 ~ 1F7F | |
| | | H3 | DIO address of COC | 0 ~ F | 0 |
| Swap Control Between Controller and Observer | SWAP | | | | |
| Disconnect Remote Users | ROFF | | | | |
| Load Another Program from MTL | BOOT [,H1] | H1 | Load device address | 0 ~ 1FFF | Initial loading device |

## LOADER ERROR MESSAGES

| Error Message | Description of Error |
|---|---|
| Sequence Error Job Aborted | The last record read was out of sequence (if reading cards, the deck may be missing a card) and loading has been aborted |
| Checksum Error Job Aborted | The last record read had a checksum error (the input media may be damaged) and loading has been aborted |
| Dev Not Redy | The input device failed to come 'READY' following the last read operation and loading has been aborted |
| Illegal Load ITM | The last record read contained an illegal load item type and loading has been aborted |

1. If any loader error message is printed, loading has been aborted
2. Retry entire loading procedure:
   a. If identical error occurs, obtain a new copy of the program
   b. If loading still fails, check input device for correct operation

## MONITOR ERROR MESSAGES

All monitor error messages are output to the keyboard, KSR, and have the following format:

MONITOR ERROR XXXX where XXXX is a four-digit number.

The four-digit error numbers have the following interpretation:

| ERROR NO. | DESCRIPTION OF ERROR |
|---|---|
| 0700 | Illegal address (ALT directive, DMP directive, message print routine) |
| 1000 | Illegal device mnemonic, parameter A1, MOD directive |
| 1100 | Illegal device mnemonic, parameter A1, MID directive |
| 1200 | Illegal character in a hexadecimal parameter |
| 1201 | Illegal character in a decimal parameter |
| 1202 | No termination or continuation character in first 72 characters of a record containing a directive input from a device other than the keyboard/printer |
| 1203 | First character of a continuation line is not an exclamation |
| 1301 | First character of a record is not an exclamation |
| 1302 | Illegal directive |
| 1303 | More parameters indicated for a directive than authorized |
| 1800 | No parameters with SYST directive |
| 1801 | Diagnostic program does not show the model number specified in a SYST directive that is executed while diagnostic program is loaded |
| 1802 | Context data block in diagnostic program is not long enough |
| 1804 | Context data table in diagnostic program shows zero model numbers to which a context data block applies |
| 2201 | SIO yielded IOP halt |
| 2202 | SIO yielded incorrect length indication |
| 2203 | SIO yielded IOP memory error indication |
| 2204 | SIO yielded memory address error indication |
| 2205 | SIO yielded transmission memory error indication |
| 2206 | SIO yielded transmission data error |
| 2301 | SIO not accepted after maximum delay |
| 2302 | I/O address not recognized |
| 2303 | I/O interrupt fails to reset |
| 2304 | Device not operational |
| 2305 | Controller not operational |
| 2306 | SIO rejected after operational status byte obtained |
| 2307 | Manual mode |

## START PROCEDURE

1. Sense Switch Options

| Sense Switch | Position | Function |
|---|---|---|
| 1 | Reset | Continuous operation, no looping |
| 1 | Set | Loop on failing test or selected test if SSW3 is set |
| 2 | - | Not used * |
| 3 | Reset | Wait on error or successful completion of tests. (Clearing the wait causes looping on the error or selected test. PCP instruction address increment before clearing the wait continues the program without looping.) |
| 3 | Set | No wait after error or successful completion of test. See SSW1 for looping |
| 4 | Reset | Print all message(s) |
| 4 | Set | No message printout except from the monitor |

*Note: Sense switch 2 may be used during the loading of the Diagnostic Program Monitor, see Program Loading Instructions.

2. Monitor Directive Options - Desired Monitor Directive(s) entered
3. Environmental Directives - SYST directive is entered for test environment (Diagnostic Program Dependent)
4. Test Strategy Selection (Diagnostic Program Dependent)
5. Repeat 1, 2 and 4 when the program terminates. Repeat 3 only if system environment is to be changed

## TERMINATION INDICATION

1. Completion of a directive - Control returns to the message input device or loops on an instruction sequence
2. Error indication - Error message printout or looping on an instruction sequence
3. PCP interrupt - Control returns to the message input device and the current operation is aborted
4. Watchdog timer trap - WAIT without message (if no jumper for I/O reset)
   - Looping with message (if no jumper is connected, Sigma 5: 4C17 to 6C15, Sigma 7: 27G21 to Ground)
5. Other traps or interrupts - The following type-out will occur:

   TRAP/INTER = XX    TCC = YYYY    REGSAVE = AAAAAAAA
   PSW1 = TTTTTTTT    PSW2 = RRRRRRRR

   where:

   | | |
   |---|---|
   | XX | Denotes the trap or interrupt location |
   | YYYY | Denotes the trap condition codes |
   | AAAAAAAA | Denotes the location in memory where the register contents at the time of the trap or interrupt are stored |

   TTTTTTTT and RRRRRRRR are the contents of the Program Status Doubleword saved by the LPSD instruction executed as a result of the Trap or Interrupt

   a. Memory Fault Trap or Interrupt only - The program will Type-Out: (Sigma 8 and 9 only)
      MSWO = WWWWWW    MSW1 = EEEEEE    MSW2 = RRRRRR
      Giving the status of the faulted memory
   b. Processor Fault Interrupt only - The program will type-out: (Sigma 8 and 9 only)
      PROC. NO.    SS    F/STAT = C
      Giving the faulted processor address and the fault status

## RESTART PROCEDURE

1. Perform applicable steps under Start Procedure
2. Depress System or CPU reset switches and return the system to a RUN condition. Control returns to the message input device and the current operation (if any) is aborted
3. PCP Interrupt - Control returns to the message input device and the current operation (if any) is aborted
4. If program fails to restart correctly, reload the program

## REMOTE FACILITY

### Control

To allow a remote user to log on, the controller must use the directive !LOG. The parameters contain the password, the COC address, and the DIO Address (0 - F) e.g., !LOG, DIAG, 5, 1

Upon receipt of this directive, the COC will be activated and all lines scanned for input. If (and when) a connect signal is received, a log in message is sent to that line. The valid reply to the log in message is password. If the password is received, that teletype becomes the observer and all other lines are ignored. The controller is informed when the user has logged on.

To transfer control from the controller to the observer, the controller must use the directive !SWAP. There are no parameters for the directive.

To disconnect the COC and the remote user, the local user when he is the controller can issue the directive !ROFF. No parameters are required.

If the program detects that the remote user is "lost" due to some malfunction, the program continues with the local user as the controller even if the remote user was controller; and the COC is set up ready to reconnect the remote user equivalent to its state following a !LOG directive.

If the local ASR/KSR is "lost" due to a malfunction, the program will "WAIT".

### Directive Mode

In directive mode the controller is issuing a directive to the system. The observer obtains a copy of the directive but cannot communicate with the system or the controller.

The system is in directive mode when:

a. The DPM has typed out a ! and is awaiting input.
b. The system was running and the controller types in a !.
c. The local user, if controller, stops output with break key.
d. The remote user, if controller, stops output with the ! or escape key.

The system is not running when in directive mode.

If the local user is the controller, the local ASR/KSR is in input mode and characters input are passed to the system for use as the directive and any associated parameters. The input is copied to the remote user. Input from the remote user is ignored except as outlined under Message Mode.

If the remote user is the controller, characters from this device are used as the directive and its associated parameters. All characters input are echoed to the device and copied to the local ASR/KSR. Input from the remote user is ignored except as outlined under Message Mode.

Directives are terminated by any character other than:

A - Z 0 - 9, ; - ( )!

### Message Mode

In message mode, the two users can communicate with each other via their respective teletype devices. The characters are passed from one to the other and do not effect the system operation.

The system is in message mode when:

a. The program is running.
b. The system entered directive mode and the controller has not input any characters.
c. The system was in directive mode and the controller types in a (. This condition continues until the controller types in a ) or a !.

Characters from the remote user are echoed to the device and copied to the local ASR/KSR.

Input from the local ASR/KSR is copied to the remote user. The local ASR/KSR is input mode at all times unless chracters need to be output to it.

If the local user is the controller and the device is not in input mode because of output the user can obtain control by the procedure described under System Output.

### System Output

System output is sent to both the local ASR/KSR and the remote user.

Input other than a !, escape, or NUL character from the remote user is ignored.

Output can be stopped by the controller in two different ways.

a. Output of a single message line can be terminated by the controller hitting the NUL key if he is the remote user or depressing the break key from .1 to .9 seconds if he is the local user.
b. Output can be terminated and the DPM forced into directive mode by the controller hitting the ! or escape key if he is the remote user or depressing the break key for more than 1 second if he is the local user.

## PCP FACILITY

### Sense Switches

Real sense switches - these are the hardware sense switches on the PCP which are switched manually and their position can be found by a read direct instruction.

Pseudo sense switches - these are four positions in a defined memory location. If the bit is a one, the switch is on. Directives are available to change the settings.

After loading, if no information is received from the magnetic tape library control program about pseudo sense switches, and until (if ever) a directive is used to adjust the pseudo sense switches, the real sense switches control the program.

Following a directive to set/reset one or more of the pseudo sense switches, the pseudo sense switches control the program. A directive allows the system to switch back to using the real sense switches.

If the magnetic tape library control program informs the DPM that the pseudo sense switches are in use, then the settings will be used as received and pseudo switches will control the program until the !SSWC (see below) directive is used.

The pseudo sense switch directives are:

For turning switches on:
!SON, $n_1,n_2,n_3,n_4$

For turning switches off:
!SOFF, $n_1,n_2,n_3,n_4$

Any number of parameters up to a maximum of four can be used and the values must be in the range 1 to 4.

| | | |
|---|---|---|
| e.g., | !SON,3 | Turns on pseudo sense switch 3 |
| | !SOFF,4,1 | Turns off pseudo sense switch 4 and 1. |

If the first pseudo sense switch directive used following the use of the real sense switches does not change all four switches, the state of the others are copied from the corresponding real switches.

Following a pseudo sense switch directive the state of all the switches are shown, e.g., assume that real switches are 0101, and this is the first pseudo sense switch directive.

```
!SON,1
!!SW1234
!!  1101
```

If no parameters are given, no switches are set or reset but a printout of the current positions occurs.

A type-in of either:

```
!SON or !SOFF
```

results in a type-out of:

```
!!SW1234
!!  0101
```

To revert to the use of real sense switches the directive !SSWC is used, no parameters are required.

### WAIT Instructions

Because WAIT instructions cannot be observed or cleared from a remote location they will be eliminated as far as possible from the system.

A WAIT instruction in the last program is replaced by a call to a subroutine in the DPM. The routine will type a message and then give the user control, e.g.,

```
BAL,15          :WAIT           (address via MLT+43)
DATA            MESS1           ADDRESS OF MESSAGE
```

The controller can use the !ALT directive to adjust any locations required and use the !GO or !GO1 directives described below to continue the program.

The only situations which still require PCP control are:

1. If after loading, an ASR/KSR cannot be found - a WAIT is performed and the user puts a valid ASR/KSR address in register 2.
2. If I/O to the ASR/KSR cannot be performed the program will WAIT.
3. If a manual reset is required after a trap - the program hangs.
4. If the local user depressed control panel interrupt switch to gain control of the program.

## PCP FACILITY (Continued)

Address Stop Function

A directive is implemented to simulate the address stop feature of the PCP.

To set an address stop the controller uses the !STOP directive. The parameter is the address at which the program should stop, e.g.,

!STOP,2FE.

This directive will cause an XPSD to be placed into the address specified. If the XPSD is executed, a type out of the saved PSW1, PSW2 and the address of a stack containing the saved PSW1, PSW2 and all the registers (0-15) will occur and the user obtains control. The PCP will not reflect the saved machine state.

The user may change the saved PSW1, PSW2 and registers by use of the !ALT directive. The layout of the stack will be:

```
ADDRESS PRINTED        REGISTER 0
                       REGISTER 1
                           .
                           .
                           .
                           .
                       REGISTER 15
                       PSW1
                       PSW2
```

and the address of register zero will be on a 16 word boundary.

The controller can continue the program with the replaced instruction, or with the new environment if he has changed any of the saved values, by using the !GO directive.

A second !STOP directive with a new address causes the initial instruction to be replaced at its correct address and the XPSD to replace the instruction at the address specified.

A !STOP directive without an address causes the XPSD to be removed and the location replaced with its valid instruction; i.e., the address stop is removed.

Reset Function

A directive is implemented to simulate a reset from the PCP. A reset from PCP is performed by:

a. Hitting the interrupt button.
b. Putting the CPU into IDLE, hitting reset, and putting CPU to RUN.

This function can be simulated by the controller using the !RES directive. No parameters are required.

A reset does not disconnect the remote user. In all cases the DPM will remember if there was a remote user. Control after a reset will revert to the controller.

Continue Function

Two directives are implemented to work in conjunction with the !STOP directive, the programmed WAIT instruction and to simulate the RUN/IDLE switch on the PCP. When the program has stopped running because:

a. It arrived at the simulated stop address.
b. It arrived at the :WAIT subroutine.
c. The controller typed in an ! character or stopped output via break key.

The program can be continued correctly at the next "logical" instruction by using the !GO directive. No parameters are required. The next "logical" instruction is defined in the three cases above as:

a. The instruction which was replaced by the XPSD, or the new environment if the user altered PSW1, PSW2 and/or any of the saved registers.

b. The instruction which presently follows the WAIT instruction.

c. The next instruction in the main line code which would have been executed if the system had not switched to directive mode. There will be a loss of output if break key stopped output. A continuation of the test (with GO directive) may lead to error printouts.

At present following a WAIT associated with the sense switch routine the user either clears the WAIT and continues at the next instruction, or he increases the Instruction Register by 1 and then continues. The !GO directive simulates the former action and another new directive !GO1 will simulate the latter action.

## PCP FACILITY (Continued)

Between the time the program stops running and the issuance of the !GO or !GO1 directives the user may issue any of the following directives:

!LOG, !SON, !SOFF, !SSWC, !STOP, !MID, !MOD, !DMP, !ALT, !TDMP

If any other directives are issued the DPM will "forget" the "place to go", e.g.,

SYSTEM RUNNING
!DMP (DPM remembers next logical instruction)
!ALT
!SON
!GO
System restart at next logical instruction
SYSTEM RUNNING
!SON (DPM remembers next logical instruction)
!TST1
System restarts with Test 1 and forgets the logical instruction address.

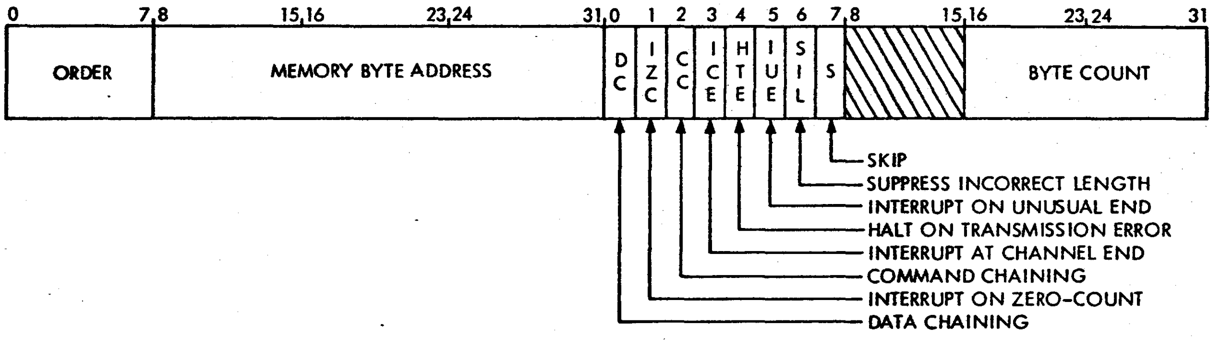
### Branch Function

A new directive is implemented to allow the controller to branch to any location he requires. The directive requires one parameter:

!BR,2FE.

The directive is intended to allow the user to depart from the normal diagnostic program procedure. Having taken the branch there is no guarantee that the program will perform according to the specification. The directive must be used with caution.

## COMMAND DOUBLEWORD FORMAT


0
7
8
15
16
23
24
31
ORDER
MEMORY BYTE ADDRESS
0 1 2 3 4 5 6 7
DC
IZC
CC
ICE
HTE
IUE
SIL
S
8 15 16 23 24 31
BYTE COUNT
SKIP
SUPPRESS INCORRECT LENGTH
INTERRUPT ON UNUSUAL END
HALT ON TRANSMISSION ERROR
INTERRUPT AT CHANNEL END
COMMAND CHAINING
INTERRUPT ON ZERO-COUNT
DATA CHAINING

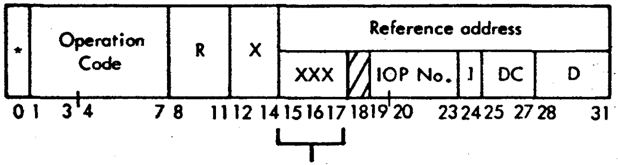
## INPUT/OUTPUT INSTRUCTIONS

### I/O ADDRESS

### I/O STATUS RESPONSE

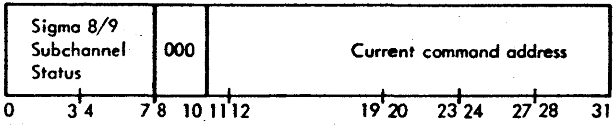
SIO, HIO, TIO, AND TDV

Multiunit device controllers (bit 24 is 1)

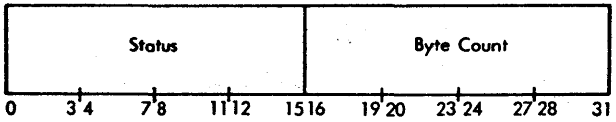

*
Operation Code
R
X
Reference address
XXX
IOP No.
1
DC
D
0 1 3 4 7 8 11 12 14 15 16 17 18 19 20 23 24 25 27 28 31

Sigma 8/9 systems only
000 = HIO
001 = RIO
010 = POLP
011 = POLR

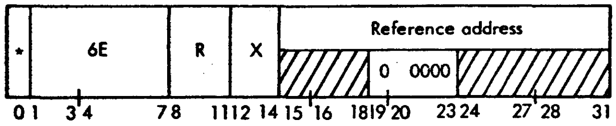
Word into register R

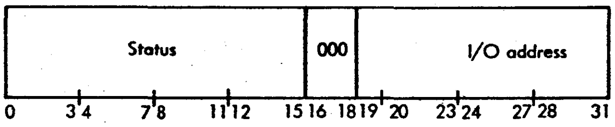

Sigma 8/9 Subchannel Status
000
Current command address
0 3 4 7 8 10 11 12 19 20 23 24 27 28 31

Word into register Ru1


Status
Byte Count
0 3 4 7 8 11 12 15 16 19 20 23 24 27 28 31

AIO


*
6E
R
X
Reference address
0 0000
0 1 3 4 7 8 11 12 14 15 16 18 19 20 23 24 27 28 31


Status
000
I/O address
0 3 4 7 8 11 12 15 16 18 19 20 23 24 27 28 31

## GENERAL CONDITION CODES

Note: These condition codes apply to most devices but they may differ. Refer to the individual device reference manual for correct condition code.

The condition code settings are:

| 1 | 2 | 3* | 4 | Result of SIO |
|---|---|---|---|---|
| 0 | 0 | - | - | I/O address recognized and SIO accepted |
| 0 | 1 | - | - | I/O address recognized but SIO not accepted |
| 1 | 0 | - | - | device controller is attached to a "busy" selector IOP or Sigma 8/9 MIOP operating in Burst Mode |
| 1 | 1 | - | - | I/O address not recognized |

| 1 | 2 | 3* | 4 | Result of TIO |
|---|---|---|---|---|
| 0 | 0 | - | - | I/O address recognized and acceptable SIO is currently possible |
| 0 | 1 | - | - | I/O address recognized but acceptable SIO is not currently possible |
| 1 | 0 | - | - | device controller is attached to "busy" selector IOP or Sigma 8/9 MIOP operating in Burst Mode |
| 1 | 1 | - | - | I/O address not recognized |

| 1 | 2 | 3* | 4 | Result of HIO |
|---|---|---|---|---|
| 0 | 0 | - | - | I/O address recognized and device controller is not "busy" |
| 0 | 1 | - | - | I/O address recognized but device controller was "busy" at the time of the halt |
| 1 | 1 | - | - | I/O address not recognized |

| 1 | 2 | 3 | 4 | Result of RIO (Sigma 8/9 only) |
|---|---|---|---|---|
| 0 | 0 | - | - | I/O address recognized |
| 1 | 1 | - | - | I/O address not recognized |

| 1 | 2 | 3 | 4 | Result of POLP or POLR (Sigma 8/9 only) |
|---|---|---|---|---|
| 0 | 0 | - | - | processor fault interrupt not pending |
| 0 | 1 | - | - | processor fault interrupt pending |
| 1 | 1 | - | - | processor address not recognized |

| 1 | 2 | 3* | 4 | Result of TDV |
|---|---|---|---|---|
| 0 | 0 | - | - | I/O address recognized |
| 0 | 1 | - | - | I/O address recognized and device-dependent condition is present |
| 1 | 0 | - | - | device controller is attached to "busy" selector IOP or Sigma 8/9 MIOP operating in Burst Mode |
| 1 | 1 | - | - | I/O address not recognized |

| 1 | 2 | 3* | 4 | Result of AIO |
|---|---|---|---|---|
| 0 | 0 | - | - | normal interrupt recognition |
| 0 | 1 | - | - | previous operations ended with unusual end or transmission error |
| 1 | 0 | - | - | AIO is accepted |
| 1 | 1 | - | - | no interrupt recognition |

*On Sigma 8/9 systems only
CC 3 = 0 Status information in general registers is correct
CC 3 = 1 Status information in general registers is incorrect

## STATUS BITS FOR I/O INSTRUCTIONS

Position and State in Register Ru1

| Device Status Byte | | Operational Status Byte * | | Significance for SIO, HIO, and TIO | Significance for TDV |
|---|---|---|---|---|---|
| 0 1 2 3 | 4 5 6 7 | 8 9 10 11 | 12 13 14 15 | | |
| 1 - - - | - - - - | - - - - | - - - - | Dev Interrupt Pending | * |
| - 0 0 - | - - - - | - - - - | - - - - | Dev Ready | * |
| - 0 1 - | - - - - | - - - - | - - - - | Dev Not Oper | * |
| - 1 0 - | - - - - | - - - - | - - - - | Dev Unavailable | * |
| - 1 1 - | - - - - | - - - - | - - - - | Dev Busy | * |
| - - - 0 | - - - - | - - - - | - - - - | Dev Manual | Unique |
| - - - 1 | - - - - | - - - - | - - - - | Dev Automatic | to the |
| | | | | | device |
| - - - - | 1 - - - | - - - - | - - - - | Dev Unusual End | and the |
| - - - - | - 0 0 - | - - - - | - - - - | Dev Cntr Ready | device |
| - - - - | - 0 1 - | - - - - | - - - - | Dev Cntr Not Oper | cntr |
| - - - - | - 1 0 - | - - - - | - - - - | Dev Cntr Unavail | * |
| - - - - | - 1 1 - | - - - - | - - - - | Dev Cntr Busy | * |
| - - - - | - - - 0 | - - - - | - - - - | Unassigned | * |
| - - - - | - - - - | 1 - - - | - - - - | Incorrect Length | * |
| - - - - | - - - - | - 1 - - | - - - - | Trans Data Error | * |
| - - - - | - - - - | - - 1 - | - - - - | Trans Mem Error | Same |
| - - - - | - - - - | - - - 1 | - - - - | Mem Addr Error | as for |
| | | | | | SIO, |
| - - - - | - - - - | - - - - | 1 - - - | IOP Mem Error | HIO, |
| - - - - | - - - - | - - - - | - 1 - - | IOP Contl Error | TIO |
| - - - - | - - - - | - - - - | - - 1 - | IOP Halt | * |
| - - - - | - - - - | - - - - | - - - 1 | Selector IOP Busy | * |

Position and State in Register R

| Device Status Byte | | Operational Status Byte * | | Significance for AIO |
|---|---|---|---|---|
| 0 1 2 3 | 4 5 6 7 | 8 9 10 11 | 12 13 14 15 | |
| 1 - - - | - - - - | - - - - | - - - - | * |
| - 1 - - | - - - - | - - - - | - - - - | * |
| - - 1 - | - - - - | - - - - | - - - - | * |
| - - - 1 | - - - - | - - - - | - - - - | * |
| | | | | Unique to the |
| | | | | device and |
| - - - - | 1 - - - | - - - - | - - - - | device controller |
| - - - - | - 1 - - | - - - - | - - - - | * |
| - - - - | - - 1 - | - - - - | - - - - | * |
| - - - - | - - - 1 | - - - - | - - - - | * |
| - - - - | - - - - | 1 - - - | - - - - | Incorrect Length |
| - - - - | - - - - | - 1 - - | - - - - | Trans Data Error |
| - - - - | - - - - | - - 1 - | - - - - | Zero BC Interrupt |
| - - - - | - - - - | - - - 1 | - - - - | Channel End Intrpt |
| - - - - | - - - - | - - - - | 1 - - - | Unusual End Intrpt |
| - - - - | - - - - | - - - - | - 0 - - | Unassigned |
| - - - - | - - - - | - - - - | - - 0 - | Unassigned |
| - - - - | - - - - | - - - - | - - - 0 | Unassigned |

## MONITOR LINK TABLE (MLT)

The MLT table allows the interfaced diagnostic program access to subroutines with the DPM and allows for data/information exchange between the DPM and the interfaced program.

| Name | Definition | Memory Location | |
|---|---|---|---|
| | | Program Location | Core Location |
| MLT | Absolute program recovery address | MLT+0 | X'200' |
| MLT01 | Parameter 1 | MLT+1 | X'201' |
| MLT02 | Parameter 2 | MLT+2 | X'202' |
| MLT03 | Parameter 3 | MLT+3 | X'203' |
| MLT04 | Parameter 4 | MLT+4 | X'204' |
| MLT05<br>•<br>MLT12 | Unassigned | MLT+5<br>•<br>MLT+12 | X'205'<br>•<br>X'20C' |
| MLT13 | Temporary ASR mode flag | MLT+13 | X'20D' |
| MLT14 | Unassigned | MLT+14 | X'20E' |
| MLT15 | 'DMP' directive routine call location for interfaced programs | MLT+15 | X'20F' |
| MLT16 | DPM Reentry | MLT+16 | X'210' |
| MLT17 | Parameter status word | MLT+17 | X'211' |
| MLT18 | Unassigned | MLT+18 | X'212' |
| MLT19 | Binary coded decimal (BCD) to binary, conversion subroutine interface location | MLT+19 | X'213' |
| MLT20 | Directive return address - returns control to the DPM | MLT+20 | X'214' |
| MLT21 | Unassigned | MLT+21 | X'215' |
| MLT22 | Binary to EBCDIC conversion subroutine interface location | MLT+22 | X'216' |
| MLT23 | Decimal to EBCDIC conversion subroutine interface location | MLT+23 | X'217' |
| MLT24 | Hexadecimal to EBCDIC conversion subroutine interface location | MLT+24 | X'218' |
| MLT25 | One-byte input subroutine interface location | MLT+25 | X'219' |
| MLT26 | Current character counter for one-byte input routine | MLT+26 | X'21A' |
| MLT27 | Error report subroutine interface location | MLT+27 | X'21B' |
| MLT28 | Message print subroutine interface location | MLT+28 | X'21C' |
| MLT29 | Sense switch check subroutine interface location | MLT+29 | X'21D' |
| MLT30 | 'WAIT' instruction, after I/O failure of 'MOD/MID' device | MLT+30 | X'21E' |
| MLT31 | Branch instruction - retry after I/O failure | MLT+31 | X'21F' |
| MLT32 | I/O address of current 'MOD' device (branch instruction) | MLT+32 | X'220' |
| MLT33 | I/O address of current 'MID' device | MLT+33 | X'221' |
| MLT34 | I/O address of initial loading device | MLT+34 | X'222' |
| MLT35 | Teletype print routine location | MLT+35 | X'223' |
| MLT36 | I/O address of default 'MOD/MID' device | MLT+36 | X'224' |
| MLT37 | Computer type code storage, 0 = Sigma 5/7, 9 = Sigma 8/9 | MLT+37 | X'225' |
| MLT38 | Relocation bias of DPM program | MLT+38 | X'226' |
| MLT39 | Resident loader base address | MLT+39 | X'227' |

(Continued)

**MONITOR LINK TABLE (MLT)** (Continued)

| Name | Definition | Memory Location | |
|---|---|---|---|
| | | Program Location | Core Location |
| MLT40 | Unassigned | MLT+40 | X'228' |
| MLT41 | Parameter error report subroutine interface location | MLT+41 | X'229' |
| MLT42 | Quick sense routine address | MLT+42 | X'22A' |
| MLT43 | Wait routine address | MLT+43 | X'22B' |
| MLT44 | DPM directive dictionary base address | MLT+44 | X'22C' |
| MLT45 | Length of DPM directive dictionary | MLT+45 | X'22D' |
| MLT46 | Address of last memory location | MLT+46 | X'22E' |
| MLT47 | Address of last memory location interfaced program may use | MLT+47 | X'22F' |
| MLT48 | Base address of 120 byte input buffer | MLT+48 | X'230' |
| MLT49 | Base address of 40 word parameter input buffer | MLT+49 | X'231' |
| MLT50 | 'LOAD' directive memory location | MLT+50 | X'232' |
| MLT51 | Input routine address | MLT+51 | X'233' |
| MLT52 | Output routine address | MLT+52 | X'234' |
| MLT53 | Error routine address for DPM IO errors | MLT+53 | X'235' |
| MLT54 | Directive preprocessor | MLT+54 | X'236' |
| MLT55 | Unassigned | MLT+55 | X'237' |
| • | | • | • |
| • | | • | • |
| • | | • | • |
| MLT63 | | MLT+63 | X'23F' |

## PROGRAM INTERFACE TABLE (PIT)

The PIT table is established by the user program at 'LOAD' time and provides the DPM with information describing the user diagnostic program.

| Name | Definition | Memory Location | |
|---|---|---|---|
| | | Program Location | Core Location |
| PIT | Unassigned | PIT+0 | X'300' |
| PIT01 | Address of the user program's title message | PIT+1 | X'301' |
| PIT02 | Address of the user program's directive dictionary | PIT+2 | X'302' |
| PIT03 | The count of the number of words in the user program's directive dictionary | PIT+3 | X'303' |
| PIT04 | Address of the user program's absolute recovery routine | PIT+4 | X'304' |
| PIT05 | Address of the user program's context description table | PIT+5 | X'305' |
| PIT06 | The count of the number of words in the user program's context description table | PIT+6 | X'306' |
| PIT07 | Unassigned | PIT+7 | X'307' |
| PIT08 | Address of the user program's initializer routine | PIT+8 | X'308' |
| PIT09 | Contains the last device model number input via 'SYST' directive transferred to a context data block | PIT+9 | X'309' |
| PIT10 | Specifies the number of the faulty parameter in a parameter error message | PIT+10 | X'30A' |
| PIT11 | The DPM stores a zero in PIT11 prior to branching to the user program's initialization routine. If this location is non zero upon returning to the DPM, the contents are assumed to be a message address and the message is printed | PIT+11 | X'30B' |
| PIT12 | The user program's RUN switch. This location must be non zero to execute a user directive. If zero when a user directive is called, the error mesage: 'ENTER SYST DIRECTIVE' is printed | PIT+12 | X'30C' |
| PIT13<br>PIT14 | Unassigned | PIT+13<br>PIT+14 | X'30D'<br>X'30E' |
| PIT15 | Address of the user program's trap and fault interrupt handling routine | PIT+15 | X'30F' |
| PIT16<br>.<br>.<br>.<br>PIT31 | Unassigned | PIT+16<br>.<br>.<br>.<br>PIT+31 | X'310'<br>.<br>.<br>.<br>X'31F' |

# Section 4

# SIGMA 5 - 9
# KEYBOARD PRINTER (ASR/KSR)

## PROGRAM NO. 705651

## Section 4

## CONTENTS

Page

Subject Model . . . . . 4-1
Required Equipment . . . . . 4-1
Program Prerequisites . . . . . 4-1
General Operating Procedures . . . . . 4-1
Directives . . . . . 4-2
Start Procedure . . . . . 4-4
Program Test Description . . . . . 4-5
Order Codes . . . . . 4-5
TDV Status . . . . . 4-6
AIO Status . . . . . 4-6
Functional Subtests and Related Error Messages . . . . . 4-7

**SUBJECT MODEL** -- KSR, Model number 7012, ASR, Model number 7020

**REQUIRED EQUIPMENT** -- Minimum Memory Size: 8K: Input Device: Card Reader, Paper Tape Reader or Magnetic Tape Unit: Output Device: Keyboard Printer or Line Printer

## PROGRAM PREREQUISITES

If the keyboard printer is inoperative, register mode of operation must be selected at program load time.

The ASR punch tests require blank paper tape and the reader tests require prepunched paper tape from the corresponding punch test.

## GENERAL OPERATING PROCEDURES

General operating procedures of the Xerox Sigma 5 through 9 Diagnostic Program Monitor (DPM) apply to this program.

The following additional operating procedures are unique to this program. See also START PROCEDURE.

### Program Loading Instructions

If the message input/message output device is the device to be tested, the method of loading is determined by the operational state of the KSR/ASR.

### KSR/ASR Operational

The test program can be loaded either from cards or MTL using normal loading procedures. (Sense switch 2 must be OFF if loaded from cards.) Program/User communication is via the message input/message output device (operation mode 1).

### KSR/ASR Not Operational

The test program can be loaded only from cards. Since the KSR/ASR is not available for program/user communication, a procedure is established to automatically load the test program and to control the program via registers.

- Set sense switch 2 to ON position.
- Boot in loader. The deck consists of:

  Loader
  Relocation Card
  DPM
  ASR/KSR test program
- Clear first wait.
- On second wait enter a -1 in register 0 and clear wait.
- The DPM and the ASR/KSR test program are loaded.
- Test program defaults to register communication mode (operation mode 0).

### Operation Modes

Mode 0

In mode 0 operation, all program-operator communication is accomplished using the PCP general registers for directive input and message output. This mode is normally used when the ASR (or KSR) under diagnosis is the only message device available in the system and the device cannot be relied upon for error-free communication with the program. Test directives 'TST0', 'TST1' and 'TST2' can be invoked in the operating mode. Messages and error number messages appear in a general register.

Mode 1

In mode 1 operation, program-operator communication is accomplished using the input/output device(s) specified by the operator (refer to DPM directives 'MID' and 'MOD'). Also, pertinent status and data information is available in the general registers (this is due to the duality of the program).

Changing of Operation Modes:

If the program operation mode is to be changed from mode 0 to mode 1, press PCP reset switch and go to RUN. The program will type a 1.

To change from mode 1 to mode 0, enter SYST directive with parameter 4 = 0.

**DIRECTIVES** - directives are entered after a " ! " is typed out when operating in mode 1.

See START PROCEDURE for entering directives via general registers when operating in mode 0.

| Name | Format | Parameter | | | |
|---|---|---|---|---|---|
| | | ID | Definition | Value Range | Standard Value (default) |
| Program Directives - Environmental Directives | | | | | |
| System Environment | SYST, D1, H2, H3, H4 | D1 | Device model number | 7012 KSR<br>7020 ASR | |
| | | H2 | Revision number | | |
| | | H3 | IOP and device address | 0 - 1FFF | |
| | | H4 | Operation mode | 0 = Mode 0 register communication<br>1 = Mode 1 MID/MOD communication | |
| Program Directives - Testing Directives | | | | | |
| Comprehensive Test (all functional tests 1 - 13, and random tests 1 - 2) | TST0 | | | | |
| Functional Test | TST1 | D1 | First subtest to be executed | 1 - 13 | 0 |
| | | D2 | Last subtest to be executed | 1 - 13 | 0 |
| | | | D1, D2 = 0 | all subtests | |
| | | | $0 < D1 \le D2 \le 13$ | | |
| Random Exerciser Test | TST2 | D1 | First test to be executed | 1 - 2 | 0 |
| | | D2 | Last test to be executed | 1 - 2 | 0 |
| | | | $0 < D1 \le D2 \le 2$ | | |
| Utility Test | TST3, D1, D2 | D1 | Utility test selection | | |
| | | D2 | Function selection | | |
| | | D1=1 | Printer character spacing<br>D2 - not used | | |
| | | D1=2 | Paper tape punch/read/verify<br>D2 = 1 Punch a preselected pattern with 20 byte leader<br>D2 = 2 Punch a preselected pattern without leader<br>D2 = 3 Read paper tape ignoring leader<br>D2 = 4 Read paper tape immediate<br>D2 = 5 Read paper tape (ignoring leader) and verify with preselected pattern.<br>D2 = 6 Read paper tape (immediate) and verify with preselected pattern | | |
| | | D1=3 | Mechanical print check test<br>D2 - not used | | |

**DIRECTIVES** (Continued)

| Name | Format | Parameter | | | |
|---|---|---|---|---|---|
| | | ID | Definition | Value Range | Standard Value (default) |
| Program Directives - Optional Directives | | | | | |
| Pattern Selection (for Utility Test TST3,2) | DATA, D1, H2, H3 | D1<br>H2<br>H3 | = 0, Fixed pattern<br>= 1, Incremental pattern<br>= 2, Random pattern<br>= 4, Paper tape pattern<br>Pattern seed (for D1 = 0, 1, 2)<br>Incrementing constant (for D = 1) | 0 - 4<br>00000000<br>FFFFFFFF | |
| Length of Record Selection (for Utility Test TST3,2) | LEN, D1 | D1 | Length of record in bytes (Must be a multiple of 4) | Min. = 4<br>Max. = 1600 | |
| Pass Control and Pass Count Printout for TST0,2,3 | LIMT, D1, D2, D3 | D1<br>D2<br>D3 | = 2 Effect pass control only<br>Number of passes after which pass count is to be printed out.<br>Total number of passes to be completed. | 2<br>$D2 \geq 0$<br>$D3 \geq 0$ | |

## START PROCEDURE

1. Sense Switch Options, Monitor Directive Options, and Environmental Directives - Refer to DPM section of this manual.
2. Test Strategy Selection

| | Comprehensive Test | Functional Test | Random Exerciser Test | Utility Test |
|---|---|---|---|---|
| Recommended Application | Normal Usage | Solid Failure Detection and Specific Problem Analysis | Intermittent Failure Detection | Test Printer, Paper Tape Reader/Punch |
| Test Directive | TST0 | TST1 | TST2 | TST3 |
| Prerequisite | None | None | TST1 | TST1 |
| Optional Directives | LIMT | LIMT | LIMT | LIMT, DATA, LEN |
| Subtests | All functional subtests (1-13) and random exerciser tests | 13 subtests (see error messages for the test types) | Print; punch and read paper tape | Print; punch and read paper tape |
| Error Message Format (from MOD or general register) | 1. ERROR NO. DDDD LOC XXXX<br>2. Self-explanatory | ERROR NO. DDDD LOC XXXX | Self-explanatory | Self-explanatory |

3. Start/Restart Procedures (unique to this program)

START:

Mode 0 - After the program is successfully loaded, the program comes to a wait condition with message #1 in general register 1 (X'80000001'). The user may then input into register 0 the desired test directive in the following format:

Byte 0 - Test number
0 = TST0
1 = TST1
2 = TST2
Byte 1 - Must be 0
Byte 2 - Starting subtest number (in hex)
Byte 3 - Ending subtest number (in hex)

Clearing the wait causes the test to begin.

Mode 1 - After the program is successfully loaded and the program identification is printed, the operator may specify any test directive(s) (using the message input device).

Unless a 'SYST' directive is entered, the program assumes (by default) model 7012 (KSR), device address X'01' and mode 0 operation.

RESTART:

Mode 0 - The PCP interrupt switch, when depressed, causes the program to request a directive be entered into register 0. The PCP system reset switch, when depressed, causes the program to re-initialize and request a directive input from the last declared message input device. In this manner, the conversion from mode 0 to mode 1 may be accomplished, as the operator may then enter a 'SYST' directive specifying mode 1 operation.

Mode 1 - Both the PCP interrupt and system reset switch, when depressed, causes the program to re-initialize and request a directive input from the last declared message input device.

TERMINATION PROCEDURE:

The completion of a test or subtest is indicated by the directive input request message #1 (mode 0) or by the message input device's request for a directive.

SUCCESS-FAILURE INDICATIONS:

WAITS:

The program comes to a wait condition:

1. During an error message report (SSW3=0).
2. After a test completion (SSW3=0).
3. During a message requesting future operator intervention.
4. If the device address was not recognized, the wrong address will be found in register 2. To continue, enter the new device address in register 2 and clear the wait.

LOOPS:

The program loops on an instruction sequence producing an error or loops on a test or subtest (SSW1=1 or SSW3=0).

## PROGRAM TEST DESCRIPTION

The following is a description of the tests contained in the ASR/KSR test program.

### TST0

The directive selects the comprehensive test consisting of the functional tests (subtests 1-13) and the random exerciser (subtests 1-2).

### TST1

The test descriptions of each functional test are included at the beginning of each subtest error number in the Functional Subtest and Related Error Message section.

### TST2

The random exerciser operates the device in a random manner in order to detect intermittent logic failures. The random exerciser consists of 2 subtests, each subtest independently selectable. Punching and reading portions of the random exerciser test are automatically bipassed if the KSR is under test.

Subtest 1 - Print ripple pattern,punch random paper tape.
Subtest 2 - Read and verify the random paper tape.

### TST3

This directive selects one of the following utility tests.

TST3,1 Character spacing adjustment and ribbon shift option test
A set of 12 pre-determined characters is printed to aid in keyboard printer character spacing adjustments. The ribbon shift option is checked by sending shift-out and printing the first 6 character lines in red then sending shift-in and printing the second 6 character lines in black.

TST3,2 Paper tape punch/reader tests
The DATA and LEN directives are available to specify the pattern and record length respectively.

TST3,2,1 Paper tape punch with leader
A paper tape is punched with a 20-byte leader. The punched pattern is selected by the 'DATA' directive. The punched pattern length is selected by the 'LEN' directive.

TST3,2,2 Paper tape punch
A paper tape is punched (without leader). The pattern and length are selected by the 'DATA' and 'LEN' directives, respectively.

TST3,2,3 Paper tape read ignoring leader
A paper tape is read (ignoring leader). The length is selected by the 'LEN' directive.

TST3,2,4 Paper tape read immediate
A paper tape is read (immediate). The length is selected by the 'LEN' directive.

TST3,2,5 Paper tape read and verify
A paper tape is read (ignoring leader) and verified. The length is selected by the 'LEN' directive and the pattern used for verification is selected by the 'DATA' directive.

TST3,2,6 Paper tape read immediate and verify
A paper tape is read (immediate) and verified. The length is selected by the 'LEN' directive and the pattern used for verification is selected by the 'DATA' directive.

TST3,3 Mechanical print check test
A 40 line pattern is printed to verify the mechanical alignment of the printer.

## ORDER CODES

| | | Applicable Devices | |
|---|---|---|---|
| | | KSR | ASR |
| X'00' | Stop | - | 1 |
| X'01' | Punch | - | 1 |
| X'02' | Read | - | 1 |
| X'05' | Type | 1 | 1 |
| X'06' | Read keyboard continuously until EOM character is typed or "count done" signal | 1 | 1 |
| X'82' | Read immediate | - | 1 |
| X'86' | Read keyboard until control character [codes 05 (HT), 08 (EOM), or 15 (NL)] is typed or "count done" signal | 1 | 1 |

## TDV STATUS

<table>
<tr><th rowspan="2">MODEL</th><th colspan="8">BITS</th></tr>
<tr><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th></tr>
<tr><td>7012</td><td colspan="8">NOT USED</td></tr>
<tr><td>7020</td><td colspan="3">NOT USED</td><td>Read Manual</td><td>Unit Off-Line</td><td colspan="3">NOT USED</td></tr>
</table>

## AIO STATUS

<table>
<tr><th rowspan="2">MODEL</th><th colspan="8">BITS</th></tr>
<tr><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th></tr>
<tr><td>7012</td><td colspan="8">NOT USED</td></tr>
<tr><td>7020</td><td colspan="8">NOT USED</td></tr>
</table>

## FUNCTIONAL SUBTESTS AND RELATED ERROR MESSAGES

### MESSAGE PRINTOUT

Mode 0 During mode 0 operation, program messages have the following format in register 0:
(REG 0) = X'800000DD' where DD = message number defined under register operation messages.

The error messages have the following format in register 0:
(REG 0) = X'C000DDDD' where DDDD = error number defined in the fault index.

Mode 1 During mode 1 operation, the standard error messages have the following format:
ERR NO.DDDD LOC.XXXX where DDDD=error message number defined in the fault dictionary and XXXX is the listing location where the error was detected.

### REGISTER OPERATION (MODE 0) MESSAGES

Register Operation Messages:

| | |
|---|---|
| 0001 | Enter a test directive into register 0. Clear wait. |
| 0003 | Enter one or two failing characters (in EBCDIC) into Reg 0 (bytes 2 and 3) and clear wait. If no failing character(s), depress the PCP instr addr increment switch and clear wait. |
| 0004 | Echo test 1 is to begin. Clear wait. |
| 0005 | Echo test 2 is to begin. Clear wait. |
| 0006 | Echo test 3 is to begin. Clear wait. |
| 0007 | Insert punched paper tape into reader. |

### FAULT INDEX DESCRIPTION - FUNCTIONAL SUBTESTS

The fault index contains a brief description of each functional subtest and a list of associated error numbers with a brief description of each error. The subtests and error numbers are arranged in ascending sequence. The description of subtest NN is numbered NN00. The first two digits of the error number correspond to the associated subtest; the last two numbers correspond to the individual errors within the subtest.

NN = 0 indicates a general error message.

Functional Test Error Messages:

| | |
|---|---|
| 0001 | Test directive parameter P1 invalid. Input correct directive. |
| 0002 | Test directive parameter P2 invalid. Input correct directive. |
| 0003 | Test directive parameter P3 invalid. Input correct directive. |
| 0004 | Test directive invalid. Input correct directive. |
| 0005 | Watchdog timer trap has occurred indicating an IO instruction hang-up. (Reg 1) = address of trapped IO instruction. |
| 0006 | Trap has occurred.(Reg 1) = address of trapped instruction. |
| 0007 | Spurious interrupt received from a disarmed interrupt location. |
| 0008 | AIO instruction condition codes 1,2 indicate device address not recognized. Previous SIO received address recognition. |
| 0009 | AIO instruction results in invalid condition codes 1,2 = 10. |
| 0010 | AIO instruction results in unusual interrupt recognition condition codes 1,2 = 01.(Reg 2) = status, device address. |
| 0011 | AIO instruction status bit(s) set indicating failure in status line(s). (Reg 2) = status, device address. |
| 0012 | AIO instruction returned device address unequal to specified device address. (Reg 2) = status, device address. |
| 0013 | SYST directive parameter invalid. Program will return to monitor for error message printout attempt. |

Subtest Description:

TST1,1 Tests the HIO, TDV and TIO instructions.

| | |
|---|---|
| 0101 | HIO instruction results in invalid condition codes 1,2 = 10. (DOR(TTSH)) |
| 0102 | HIO instruction condition codes 1,2 indicate address not recognized. (DOR(TTSH)) |
| 0103 | HIO instruction status indicates both device, controller not operative. (REG2, REG3) = STATUS DW. (UNEN/DCB) (STATUS(TSH)1,2) |
| 0104 | HIO instruction device status bits 1,2 unequal to controller status bits 5,6. (REG2, REG3) = STATUS DW. (STATUS(TSH)6) |
| 0105 | HIO instruction device status bit 3 reset to indicate device is manual. (REG2,REG3) = STATUS DW. (RAUT:R) (STATUS(TSH)3) |
| 0106 | HIO instruction device status indicates device not available. (REG2,REG3) = STATUS DW. (STATUS(TSH)1) (RAUT:R) |
| 0107 | HIO instruction device and controller status bits 1,5 unequal. (REG2,REG3) = STATUS DW. (STATUS(TSH)1,5) |
| 0108 | HIO instruction condition codes 1,2 = 01 indicating previous HIO failed to clear busy condition. (REG2,REG3) = STATUS DW. (SUBCONTROLLER PBLM) (IOR(HIO)) (DCBUSY) |
| 0109 | HIO instruction condition codes 1,2 = 00 while device status indicates device busy. (REG2,REG3)=STATUS DW. (DCBUSY) |
| 0110 | HIO instruction condition codes 1,2 = 00, device not busy while controller status indicates controller busy. (REG2,REG3)=STATUS. (STATUS(TSH)5,6) |
| 0111 | HIO instruction interrupt pending status bit set. (REG2,3) STATUS DW. (CIL) (STATUS(TST)0) |
| 0112 | HIO instruction unusual end status bit set. (REG2,3)=STATUS DW. (UNE) (STATUS(TST)4) |
| 0113 | HIO instruction status bit 7 set. (REG2,3)=STATUS DW. (STATUS(TSH)7) |
| 0121 | TDV instruction condition codes 1,2 indicate device address not recognized after previous HIO received address recognition. (SUBCONTROLLER PROBLEM) |
| 0122 | TDV instruction condition codes 1,2=01 indicating subcontroller in test mode. (REG2,3)=STATUS DW. (IOR(TDV)) (TEST) |
| 0123 | TDV instruction condition codes 1,2=10 indicating busy selector IOP. (REG2,3)=STATUS DW. (SUBCONTROLLER PBLM) |
| 0124 | TDV instruction status bit(s) 0 thru 2 or 5 thru 7 set. (REG2,3)=STATUS DW. (STATUS(TSH)0,1,2,5,6,7) |
| 0125 | TDV instruction status bit 4 set indicating device off-line. (REG2,3)=STATUS DW. (NONLINE) (STATUS(TDV)4) |
| 0126 | TDV instruction status bit 3 set indicating device reader manual. (REG2,3)=STATUS DW. (NRAUT:R) (STATUS(TDV)3) |
| 0131 | TIO instruction condition codes 1,2 indicate no address recognition. Previous HIO and TDV received address recognition. (SUBCONTROLLER PBLM) |
| 0132 | TIO instruction condition codes 1,2=10 indicating busy selector IOP. Previous HIO, TDV condition codes 1,2=00. (REG2,3)=STATUS. (SUBCONTROLLER PBLM) |
| 0133 | TIO instruction condition codes 1,2=01 indicating SIO not possible. Previous HIO condition codes 1,2 and status correct. (REG2,3)=STATUS DW. (NDCBUSY) (CIL) (OPER/SI) (SUBCONTROLLER PBLM) |
| 0134 | TIO instruction status error after successful HIO. (REG2,3)= STATUS DW. (SUBCONTROLLER PBLM) |

TST1,2 Tests the SIO instructions associated with the printing operation. Tests TIO busy indications. Tests the SIO instructions associated with the input operation function.

| | |
|---|---|
| 0201 | SIO instruction condition codes 1,2 indicate device address not recognized. (SUBCONTROLLER PBLM) |
| 0202 | SIO instruction condition codes 1,2=10 indicating busy selector IOP. (REG2,3)= STATUS DW. (SUBCONTROLLER PROBLEM) |
| 0203 | SIO instruction condition codes 1,2=01 indicating SIO not accepted. (SUBCONTROLLER PBLM) |
| 0204 | SIO instruction device and/or controller status error. (REG 2,3)=STATUS DW. |
| 0205 | TIO instruction condition codes 1,2=11 during SIO execution. (REG2,3)=STATUS DW. |
| 0206 | TIO instruction condition codes 1,2=10 during SIO execution. (REG2,3)=STATUS DW. |
| 0207 | TIO instruction condition codes 1,2=01 while status indicates not busy during SIO execution. (REG 2,3)=STATUS DW. (STATUS(TSH)1,2) (DCBUSY) (UNEN/DCB) |
| 0208 | TIO instruction status indicates device not operational after SIO accepted. (REG2,3)= STATUS DW. |
| 0209 | TIO instruction status indicates device not available after SIO accepted. (REG 2,3)= STATUS DW. |

TST1, 2 (Continued)

| | |
|---|---|
| 0210 | TIO instruction condition codes 1,2 and status indicate device not busy 50 msec after SIO (print) accepted. (REG 2,3)=STATUS DW. (NCDN/S1EN) |
| 0211 | TIO instruction condition codes 1,2=00 while status indicates device busy 50 msec after SIO (print) accepted. (DCBUSY) |
| 0212 | TIO instruction device status indicates busy while controller status does not. Condition exists 50 msec after SIO (print) accepted. (REG 2,3)=STATUS DW. (STATUS(TSH)5,6) |
| 0213 | TIO instruction status indicates operational error during SIO (print). (REG 2,3)=STATUS DW. |
| 0214 | TIO instruction status interrupt pending bit set during SIO (print) but no interrupt requested. (REG 2,3)=STATUS DW. (CIL) (CIL/S1) |
| 0215 | TIO instruction condition codes 1,2 and status indicate device busy after SIO (print) accepted but status unusual end bit set. (REG 2,3)=STATUS DW. (DOP:R) (ORDENABLE) |
| 0216 | TIO instruction condition codes 1,2=00 indicates SIO (print 2 characters) terminated prematurely after 175 msec. (REG 2,3)=STATUS DW. |
| 0217 | TIO instruction condition codes 1,2=01 indicating SIO (print 2 characters) not terminated after 275 msec. (REG 2,3)=STATUS DW. (PROUT) (CTR/C) |
| 0218 | TIO instruction status error after SIO (print) execution. (REG 2,3)=STATUS DW. |
| 0219 | SIO instruction (read) not accepted. Previous SIO (print) accepted and completed. (SUBCONTROLLER PBLM) |
| 0220 | SIO instruction status error after previous SIO status correct. (REG 2,3)=STATUS DW. |
| 0221 | TIO instruction condition codes 1,2=00 after SIO (read) accepted. (REG 2,3)=STATUS DW. (KBINP) (INSR) |
| 0222 | TIO instruction byte count reduced from 2 during SIO (read) with no input expected. (REG 2,3)=STATUS DW. (INSR) |
| 0223 | TIO instruction status indicates device not busy during SIO (read). (REG 2,3)=STATUS DW. |
| 0224 | TIO instruction status indicates controller not busy during SIO (read) execution. (REG 2,3)=STATUS DW. |
| 0225 | HIO instruction condition codes 1,2=00 during SIO (read) execution. (REG 2,3)=STATUS DW. |
| 0226 | TIO instruction condition codes 1,2 indicate HIO instruction did not terminate SIO (read) execution. (REG 2,3)=STATUS DW. (HIOU) (PHSL.T100) |
| 0227 | TIO instruction byte count not equal to 1 at 50 msec after SIO (print 2 characters) accepted. (REG 2,3)=STATUS DW. (KA/C) (CNTR/C) (CSL/S1) |
| 0228 | TIO instruction byte count not reduced to 0 at 175 msec after SIO (print 2 characters) accepted. (REG 2,3)=STATUS DW. |

TST1,3 Tests the AIO instruction, the channel end and the zero byte count interrupts, and the HIO instruction interrupt - clearing.

| | |
|---|---|
| 0301 | SIO instruction condition codes indicate no address recognition. |
| 0302 | No channel end interrupt received after SIO (print 2 characters) terminated. TIO instruction indicates device not busy, and no interrupt pending status. (REG 2,3)=STATUS DW. (SUBCONTROLLER PBLM) |
| 0303 | No channel end interrupt received after SIO (print 2 characters) terminated. TIO instruction indicates device not busy but status interrupt pending bit set. (REG 2,3)=STATUS DW. (IO INTERRUPT PBLM) |
| 0304 | TIO instruction condition codes 1,2 indicate SIO (print 2 characters with interrupt) not terminated after 225 msec. (REG 2,3)=STATUS DW. |
| 0305 | TIO instruction condition codes 1,2 indicate SIO (print 2 characters with interrupt) not terminated after 225 msec but status interrupt pending bit set and no interrupt received. (REG 2,3)=STATUS DW. |
| 0306 | AIO instruction status bit(s) 1 thru 7 set. (REG 2)=STATUS. |
| 0307 | AIO instruction status bit 0 set after SIO (print 2 characters with interrupt) indicating data overrun. (REG 2)=STATUS. |
| 0308 | AIO instruction operational status after SIO (print 2 characters with interrupt) indicates operational error. (REG 2)=STATUS. |
| 0309 | AIO instruction operational status channel end interrupt bit not set after SIO (print with channel end interrupt). Interrupt was received. (REG 2)=STATUS. |
| 0310 | TIO instruction indicates AIO did not clear interrupt pending. (REG 2,3)=STATUS DW. (SUBCONTROLLER PBLM) |
| 0311 | TIO instruction indicates device not ready after SIO (print 2 characters with interrupt) terminated. Interrupt was received and cleared. (REG 2,3)=STATUS DW |
| 0312 | TIO instruction indicates channel end interrupt pending status not cleared. (REG 2,3)=STATUS DW. |
| 0313 | No zero byte count interrupt received after SIO (print 2 characters with ZBC) accepted. |
| 0314 | AIO instruction status indicates error. (REG 2)=STATUS. |
| 0315 | AIO instruction operational status zero byte count interrupt bit not set after SIO (print 2 characters with ZBC) terminated and interrupt received. (REG 2)=STATUS. |
| 0316 | Disabled interrupt received after SIO (print 2 characters) terminated. (REG 2)=AIO STATUS. (IO INTERRUPT PBLM) |
| 0317 | TIO instruction condition codes 1,2 indicate SIO possible after SIO (print 2 characters with interrupt) terminated and no AIO issued to clear interrupt. (REG 2,3)=STATUS DW. |
| 0318 | TIO instruction condition codes 1,2=01 after SIO (print 2 characters with interrupt) but status interrupt pending bit not set. No AIO issued to clear IP. (REG 2,3)=STATUS DW. |
| 0319 | HIO instruction condition codes 1,2 not 00 when instruction issued to clear interrupt pending. (REG 2,3)=STATUS DW. |
| 0320 | TIO instruction indicates device not ready after HIO. (REG 2,3)=STATUS DW. |
| 0321 | TIO instruction indicates HIO did not clear interrupt pending. Device not ready. (REG 2,3)=STATUS DW. |
| 0322 | TIO instruction indicates HIO did not reset interrupt pending status bit. (REG 2,3)=STATUS DW. |

TST1,4 Tests the printing of all alpha and numeric characters. Subtest prints failing character input by the operator.

Operation Intervention:

Operator visually verifies the alpha and numeric characters. Operator may enter one or two characters into Reg 0 (bytes 2,3) for continuous printing (SSW1=1).

| | |
|---|---|
| 0401 | HIO instruction condition codes 1,2 or status error after previous HIO. (REG 2,3)=STATUS DW. |
| 0402 | SIO instruction not accepted after previous HIO successful. (REG 2,3)=STATUS DW. |
| 0403 | TIO instruction indicates previously accepted SIO (new line carriage movement) was not terminated after 500 msec. (REG 2,3)=STATUS DW. |
| 0404 | TIO instruction indicates a status error after SIO (new line carriage movement) terminated. (REG 2,3)=STATUS DW. |
| 0405 | SIO instruction not accepted after previously successful TIO. (REG 2,3)=STATUS DW. |
| 0406 | TIO instruction indicates a status error or failure to complete SIO (print 1 character) after 110 msec. (REG 2,3)=STATUS DW. |

TST1,5 Tests the printing using variable length records.

| | |
|---|---|
| 0501 | SIO instruction status error after HIO. (REG 2,3)=STATUS DW. |
| 0502 | TIO instruction indicates an SIO (print new line carriage movement) status error. (REG 2,3)=STATUS DW. |
| 0503 | TIO instruction indicates status or operational status error after SIO terminated. (REG 2,3)=STATUS DW. |

TST1,6 Tests the data chaining function.

| | |
|---|---|
| 0601 | SIO instruction (print with data chaining) not accepted or status error. (REG 2,3)=STATUS DW. |
| 0602 | TIO instruction indicates accepted SIO (print with data chaining) terminated prematurely at 400 msec. (REG 2,3)=STATUS DW. |
| 0603 | TIO instruction indicates the SIO command address not changed from first IOCD address to second IOCD address. (REG 2,3)=STATUS DW. |
| 0604 | TIO instruction indicates SIO not terminated. (REG 2,3)=STATUS DW. |

**TST1,7** Tests the command chaining function.

| | |
|---|---|
| 0701 | SIO instruction not accepted/status error after HIO. (REG 2,3)=STATUS DW. |
| 0702 | TIO instruction indicates SIO terminated prematurely. (REG 2,3)=STATUS DW. |
| 0703 | TIO instruction indicates an unexpected command address during SIO. (REG 2,3)=STATUS DW. |
| 0704 | TIO instruction indicates device terminated after first operation of the SIO (command chaining). (REG 2,3)=STATUS DW. |
| 0705 | TIO instruction indicates the second command address not present during second operation of SIO (command chaining). (REG 2,3)=STATUS DW. |
| 0706 | TIO instruction indicates a status error at SIO (command chaining) termination. (REG 2,3)=STATUS DW. |

**TST1,8** Echo test 1. Test the input SIO instruction and function by printing each received character input by the operator.

Operator intervention:

Operator inputs characters 'HT'=(horizontal tab), then "NL'=(new line) then any characters. Each character is echoed back. Termination character is 'EOM'.

After the EOM char is detected, up to 80 chars/line are printed 10 times.

| | |
|---|---|
| 0801 | SIO instruction not accepted or status error after HIO. (REG 2,3)=STATUS DW. |
| 0802 | No channel interrupt received within 15 seconds indicating either operator had not entered character or logic failure has occurred. (KBINP) (KSRDI) (KAO/SEN) |
| 0803 | TIO instruction indicates a status error after SIO (input 1 character) channel end received. (REG 2,3)=STATUS DW. |
| 0804 | Character received during SIO (input) not 'HT' (X'5') character. (REG 2)=CHARACTERS RECEIVED. (DL0 thru DL7) |
| 0805 | First character received during SIO (input) not 'HT' (X'5'). Second character is 'HT' indicating operator error (first character required to be 'HT'). (REG 2)=CHARACTERS RECEIVED. |
| 0806 | TIO instruction indicates 'HT' character did not terminate SIO (input 2 characters, order code X'86') operation. Byte count not 1 as expected. (REG 2,3)=STATUS DW. (KBEDM/DET) (KBLA:D) |
| 0807 | Character received during SIO (input) not 'NL' (X'15') character. (REG 2)=CHARACTERS RECEIVED. (DL0 thru DL7) |
| 0808 | First character received during SIO (input) not 'NL' (X'15'). Second character received is 'NL' indicating operator error (first character required to be 'NL'). (REG 2)=CHARACTERS RECEIVED. |
| 0809 | TIO instruction indicates 'NL' character did not terminate SIO (input 2 characters, order code X'86') operation. Byte count not 1 as expected. (REG 2,3)=STATUS DW. |
| 0810 | TIO instruction indicates a status error after SIO (input 1 character, order X'06') terminates. (REG 2,3)=STATUS DW. |
| 0811 | TIO instruction byte count not reduced to zero after SIO (input 1 character, order X'06') terminates. (REG 2,3)=STATUS DW. |
| 0812 | TIO instruction indicates status error after SIO (input 2 characters, order X'86') terminated by 'NL' character. (REG 2,3)=STATUS DW. |

**TST1,9** Echo test 2. Test IO lines by printing of 16 characters and requiring the operator to input each character as it is printed.

Operator intervention:

Operator inputs each character as it is received.

| | |
|---|---|
| 0901 | SIO instruction not accepted or status error after HIO. (REG 2,3)=STATUS DW. |
| 0902 | TIO instruction status error after SIO (print new line character) terminated. (REG 2,3)=STATUS DW. |
| 0903 | SIO instruction not accepted or status error. (REG 2,3)=STATUS DW. |
| 0904 | Character received not equal to previously printed character. (REG 1)=PRINTED BYTE. (REG 2)=OBSERVED BYTE. (DL0 thru DL7) (KA0/S1 thru KA7/S1) |

**TST1,10** Echo test 3. Test IO lines and multiple character input by printing 8 characters and requiring the operator to input the characters after the printout is complete.

Operator intervention:

Operator inputs character string identical to that received.

| | |
|---|---|
| 1001 | SIO instruction not accepted or status error after HIO. (REG 2,3)=STATUS DW. |
| 1003 | Character string received not equal to previously printed character string. (REG 1)=PRINTED 4 BYTES. (REG 2)=OBSERVED 4 BYTES. |

**TST1,11** Tests the SIO instruction and paper tape punching function. Automatic bipassing of test if KSR unit under test.

Operator intervention:

Operator insures blank paper tape is in punch station.

| | |
|---|---|
| 1101 | SIO instruction not accepted or status error after HIO. (REG 2,3)=STATUS DW. |
| 1102 | TIO instruction indicates device busy after maximum allowable time (2.4 sec) of SIO (punch leader) operation. (REG 2,3)=STATUS DW. |
| 1103 | TIO instruction indicates device not busy but SIO (punch leader) byte count not reduced to 0. (REG 2,3)=STATUS DW. |
| 1104 | TIO instruction indicates status error after SIO (punch leader) terminated. (REG 2,7)=STATUS DW. |
| 1105 | TIO instruction indicates status error after SIO (punch pattern) terminated. (REG 2,3)=STATUS DW. (OUT:D) |
| 1106 | Error detected during punching of 80 byte trailer (blanks). |

**TST1,12** Tests the SIO instruction, paper tape read function. Automatic bipassing of test if KSR unit under test.

Operator intervention:

Operator visually verifies first portion of paper tape and inserts tape into read station:

| BYTES | PUNCH |
|---|---|
| 0–15 | Blank |
| 16–19 | X'FF' |
| 20–23 | Blanks |
| 24–31 | X'01' |
| 32–39 | X'02' |
| 40–47 | X'04' |
| (etc) | |
| 80–87 | X'80' |
| 88–95 | Alt. X'00'–X'FF' |
| 96–103 | Alt. X'55'–X'AA' |
| 104–307 | Random numbers |
| 308–388 | Blank |

| | |
|---|---|
| 1201 | SIO instruction not accepted or status error. (REG 2,3)=STATUS DW. |
| 1202 | TIO instruction indicates SIO (read ignoring leader) not terminated within 15 sec. (REG 2,3)=STATUS DW. |
| 1203 | TIO instruction indicates status error after SIO (read ignoring leader) terminated. (REG 2,3)=STATUS DW. |

TST1, 12 (Continued)

1204 TIO instruction indicates SIO (read ignoring leader) byte count not equal to 0. (REG 2,3)=STATUS DW.

1205 First four bytes read not equal to X'FF'. (REG 1)=EXPECTED 4 CHARACTERS. (REG 2)=RECEIVED 4 CHARACTERS. (DL0:R thru DL7:R) (ASR(X)KA/S)

1206 SIO instruction not accepted or status error. (REG 2,3)= STATUS DW.

1207 TIO instruction indicates SIO (read immediate) accepted but device not busy. (REG 2,3)=STATUS DW.

1208 TIO instruction indicates SIO (read immediate) accepted, device busy, but byte count not being reduced. (REG 2,3)= STATUS DW.

1209 TIO instruction indicates SIO (read immediate) terminated but byte count not reduced to 0. (REG 2,3)=STATUS DW.

1210 Character received not equal to character expected. (REG 1) =EXPECTED CHARACTER. (REG 2)=CHARACTER RECEIVED. (ASR(X)KA/S) (DL0:R thru DL7:R) (DA0 thru DA7)

TST1,13 Checks for channel end and unusual end interrupt when break key is depressed.

Operator intervention:

Before entering subtest 13 insure that mode 1 is in effect with a SYST directive. This test will not run in mode 0. Operator presses break key when message from KSR says 'PRESS BREAK KEY'. Break key should not be held down for more than 1 sec any one time.

1300 SIO not accepted or device not recognized. Status, byte count in register 5.

1301 Expected channel end, unusual end interrupts did not come.

1302 AIO instruction issued, expected CEI, UEI, bits not set. Status may be found in reg. 2.

1303 TIO instruction issued, expected conditions: device ready, controller ready and/or device unusual end bit not set. Status may be found in register 2.

1304 AIO issued, condition code did not signal an expected unusual interrupt recognition. CC1,2. EXPECTED CC1,2=01

# Section 5

# SIGMA 5 - 9
# COMPREHENSIVE CARD EQUIPMENT (TEST)

## PROGRAM NO. 706169

## Section 5

## CONTENTS

Page

Subject Model . . . . . . . . . . 5-1
Required Equipment . . . . . . . . . . 5-1
Program Prerequisites . . . . . . . . . . 5-1
General Operating Procedures . . . . . . . . . . 5-1
Directives . . . . . . . . . . 5-2
Start Procedure . . . . . . . . . . 5-4
Program Test Description . . . . . . . . . . 5-5
Order Codes . . . . . . . . . . 5-7
Normal TDV Status . . . . . . . . . . 5-8
Test Mode TDV Status . . . . . . . . . . 5-8
AIO Status . . . . . . . . . . 5-8
Functional Subtests and Related Error Messages . . . . . . . . . . 5-9
Card Samples (TST1) . . . . . . . . . . 5-15
50 Card Test Deck (TST1, 48 and 49) . . . . . . . . . . 5-16

# 5. SIGMA 5–9 COMPREHENSIVE CARD EQUIPMENT (TEST)

**SUBJECT MODEL** -- Card Readers Model Numbers 7120, 7121, 7122, 7140 and/or Card Punches Model Numbers 7160-1, 7160-2, 7165.

**REQUIRED EQUIPMENT** -- Minimum Memory Size: 16K; Input Device: Card Reader, Paper Tape Reader or Magnetic Tape Unit; Output Device: Keyboard Printer or Line Printer.

## PROGRAM PREREQUISITES

Test Deck: For card reader only systems, a test deck may be obtained from the Xerox software library. The test deck (706169-74A) consists of the following cards:

a. Checkerboard deck - used for TST1, 41

b. 50 card test deck - used for TST1, 49

c. Invalid EBCDIC - coded card - used for TST1, 50

d. Mode switching card - used for TST1, 51

e. 500 random data cards - used for TST2

f. Blank cards required for TST1 are not included

## GENERAL OPERATING PROCEDURES

General operating procedures of the Xerox Sigma 5 through 9 Diagnostic Program Monitor (DPM) apply to this program.

# 5. SIGMA 5–9 COMPREHENSIVE CARD EQUIPMENT (TEST)

SYST, 7120, 0, 003

**DIRECTIVES** – directives are entered after a "!" is typed out

| Name | Format | Parameter | | | |
|---|---|---|---|---|---|
| | | ID | Definition | Value Range | Standard Value (default) |
| Program Directives – Environmental Directives | | | | | |
| System Environment (Normally two SYST directives would be entered for a system, one specifying a card reader and one a card punch. Only the device selected by the last SYST directive will be used during the functional testing). | SYST, D1, H2, H3 | D1 | Device model number | 7120, 7121, 7122 7140 card readers<br>7160, 7165 card punches | 003<br>004 |
| | | H2 | Revision number of controller | 0 for card readers<br>0 for 7160-1 or 7165 card punches<br>2 for 7160-2 card punch | |
| | | H3 | IOP and device address<br>Note: A SYST directive with a device address of 'FFFFFFFF' will insure that no test will be attempted for that device. (To be used for systems without either a card reader or card punch). | 0 – 1FFF | |
| Program Directives – Testing Directives | | | | | |
| Comprehensive Test (all functional tests, 1 – 52, and random exerciser test)<br>The functional tests will be run on the device specified in the most recent 'SYST' directive only.<br>The random exerciser will process 750 cards. This test expects to punch and read verify cards.<br>Note: See Program Test Description for detailed procedures. | TST0 | | | | |
| Functional Test (Punch device specified in most recent 'SYST' directive only) | TST1 [,D1 [,D2]] | D1 | The first subtest to be executed | 0 (all subtests) 1 – 52<br>0 First subtest | 0 |
| | | D2 | Last subtest to be executed | | |
| Random Exerciser Test (This test expects to punch and read verify cards).<br>Note: See Program Test Description for detailed procedures. | TST2, D1, D2 | D1 | Number of cards to be punched | D1 > 0 | |
| | | D2 | Number of punch retries | D2 ≥ 0 | |

**DIRECTIVES** (Continued)

| Name | Format | Parameter | | | |
|---|---|---|---|---|---|
| | | ID | Definition | Value Range | Standard Value (default) |
| Program Directives - Testing Directives (continued) | | | | | |
| Utility Test | TST3, D1, H2, H3, H4 | D1 | Utility test selected<br>0 Punch/Read EBCDIC cards<br>H2 1 Punch<br>2 Reader | | |
| | | | 1 Punch/Read binary cards<br>H2 = 1 Punch<br>= 2 Reader | | |
| | | | = 2 Punch/Read cards<br>H2 = 1 Punch<br>= 2 Reader<br>H3 Valid Punch/Read order | | |
| | | | = 3 Punch card matrix<br>H2 X coordinate (row) | 1 ~ 12 is row<br>10 is invalid<br>13 is all rows | |
| | | | H3 Y coordinate (column) | 0 Punch all columns<br>1 ~ 80 is single column | |
| | | | = 4 Punch/Reader speed test<br>H2 = 1 Punch<br>= 2 Reader | | |
| | | | = 5 Punch/Read then delay<br>H2 = 1 Punch<br>= 2 Reader<br>H3 Number of cards<br>H4 Delay in milliseconds | | |
| | | | = 6 Punch/Read functional test deck<br>H2 = 1 Punch<br>= 2 Reader<br>H3 = 0 All Decks<br>= 40 Checkerboard deck<br>= 48 50-Card test deck<br>= 50 Invalid EBCDIC coded card<br>= 51 Mode switching card | | |
| | | | = 7 Punch/Read shifting pattern<br>H2 = 1 Punch<br>= 2 Reader<br>H3 12 Bit pattern to be shifted throughout the card (Punch Only) | | |
| Program Directives - Optional Directives | | | | | |
| Pattern Selection (for Utility Tests TST3, 0 and TST3, 1 Only) | DATA, D1, H2, H3 | D1 | = 0, Fixed pattern (2 columns)<br>= 1, Incremental pattern (1 column)<br>= 2, Random Pattern | 0 ~ 2 | |
| | | H2 | Pattern seed | 00000000 ~ FFFFFFFF | |
| | | H3 | Incrementing constant (for D1=1) | | |
| Set Testing Limits | LIMT, D1, D2, D3 | D1 | = 1 Limit compare error printouts<br>D2 = Maximum number of printouts | | |
| | | | = 2 TST2 Random delay limits<br>D2 = Lower delay limit in milliseconds<br>D3 = High limit of delay in milliseconds | | |

Note: Parameter of any directive beginning with a D means decimal; with an H means hexadecimal

## START PROCEDURE

1. Sense Switch Options, Monitor Directive Options, and Environmental Directives - Refer to DPM section of this manual.
2. Test Strategy Selection

| | Comprehensive Test | Functional Test | Random Exerciser Test | Utility Test |
|---|---|---|---|---|
| Recommended Application | Normal Usage | Solid Failure Detection and Specific Problem Analysis | Intermittent Failure Detection | Punch/Read Tests |
| Test Directive | TST0 | TST1 | TST2 | TST3 |
| Prerequisite | None | None | TST1 | TST1 |
| Optional Directives | LIMT, D1 = 1,2 | LIMT, D1 = 1 | LIMT, D1 = 1, 2 | LIMT, D1 = 1 |
| Subtests | All functional subtests (1 ~ 52) and random exerciser test | 52 subtests (see error messages for the test types) | Punch and Read binary and EBCDIC cards with random patterns | Punch or Read an operator selected pattern |
| Error Message Format | 1. ERROR NO. DDDD LOC XXXX<br>2. Self-explanatory | ERROR NO. DDDD LOC XXXX | Self-explanatory | Self-explanatory |

3. System reset should normally be used in order to insure the resetting of controller test mode logic.

## PROGRAM TEST DESCRIPTION

The following is a description of the tests contained in the Comprehensive Card Equipment test program.

TST0
The directive selects the comprehensive test consisting of the functional tests (subtests 1-52) and the random exerciser test.

Parameters: None

Test Variations:

1. The functional test will be run on the device specified in the most recent 'SYST' directive (in sequence, subtest 1 thru 52).
2. The random exercisor will attempt to simultaneously punch and read cards. The card count and retry on error parameters are initialized to 750 and 2 respectively. If a failure is encountered an error message is printed and the exercising continues.
3. To avoid exercising a card punch or reader, enter a SYST directive for a punch or reader with an address of 'FFFFFFFF'.

Example:
```
SYST, 7121, 0, FFFFFFFF
SYST, 7165, 0, 4
TST0
```

1. The functional test will be run on the Model 7165 card punch at address 4 (in sequence, subtest 1 thru 52).
2. The random exercisor will be run only on the Model 7165 card punch. 750 cards will be punched with an error retry count of 2.

Note: If only a card reader is being tested (card punch inhibited), the reader must be preloaded with a functional test deck and a 750 card random exerciser test deck prior to running.

TST1
The directive selects the entire functional test (no parameters entered) or selects one or more contiguous functional subtests. This test will be run only on the device specified in the most recent SYST directive.

Parameters:
D1 - First Functional Subtest
D2 - Last Functional Subtest

Where $0 < D1 \leq D2 \leq 52$

TST1, D1, D2

Example:
```
SYST, 7122, 0, 3
TST1
```

Run all functional subtests that apply to a Model 7122 card reader on the device at address '3'.

Example:
```
SYST, 7122, 0, 3
SYST, 7165, 0, 5
TST1, 40, 40
```

Execute functional subtest 40 on the Model 7165 card punch at device address '5'.

Example:
```
TST1, 46, 46
```

Execute functional subtest 46 on the device specified in the most recent SYST directive. Since subtest 46 applies only to a Model 7165 card punch, the most recent SYST directive should have been for that model card punch.

Note: The functional test card requirements are listed immediately following the error message listing.

TST2
This directive selects the random exerciser test, which exercises either or both the punch and reader devices specified in the most recent SYST directives. Binary and EBCDIC cards with random patterns are randomly intermixed when punching. These same cards can be read in any order. Exercising for any device can be terminated by placing that device in 'Manual' mode.

Parameters:
D1-Number of cards to be punched
$(0 \leq D1 < 32,768)$
D2-Number of punch retries
$(0 \leq D2 \leq 99)$

TST2, D1, D2

Test Variations:
LIMT: The limit directive limits the range of the random delays introduced between successive card operations.
SYST: A SYST directive for a card punch or reader with a device address of 'FFFFFFFF' will exclude that device from this test.

Example:
```
TST2, 2000, 1
```

The random exerciser will punch 2000 cards and/or read and verify all cards in the card reader.

This test punches valid binary (punches in rows 1 and 2 of column 1) and EBCDIC cards in random sequence using a regenerative pattern. All reading takes place in the automatic mode, therefore binary cards are read in binary mode and EBCDIC cards are read in EBCDIC mode. These cards have no special sequence.

Cards in the punch error stacker should be read varified seperately to determine punch errors/check read errors.

TST3
This directive selects one of the following utility tests:

| | |
|---|---|
| TST3, 0 | Punch or Read EBCDIC Cards (Pattern punched and verified is that specified by the most recent data directive). |
| TST3, 1 | Punch or Read Binary Cards (Pattern punched and verified is that specified by the most recent data directive). |
| TST3, 2 | Using a valid device order specified by the operator, punch or read cards. |
| TST3, 3 | Punch Card Matrix. Cards are punched with the punched positions selected by specifying the row number and column. A row number of 13 will cause the punching of all rows; a column entry of 0 will cause punching of all columns. |
| TST3, 4 | Punch/Reader Speed Test. The speed of the punch or reader is determined by punching or reading 31 cards and averaging the speed over 1 minute. |
| TST3, 5 | Punch/Read then Delay. Binary cards with random patterns are punched; no verification is performed on a read operation. The number of cards punched/read, and the following delay are specified by the operator. |
| TST3, 6 | Punch/Read Functional Subtest Decks . All or individual functional subtest decks can be punched and verified. |

## PROGRAM TEST DESCRIPTION (Continued)

TST3, 7 Punch/Read Shifting Pattern.
When punching, a 12-bit operator specified pattern for column 1 is circularly shifted throughout the binary card. Read verification of these cards is provided.

Test Variations:
SYST: The utility tests assume that SYST directives for the devices to be exercised have previously been entered by the operator.
Sense Switches: The following sense switch options apply to all TST3 tests.
SSW3 Reset - Wait at end of test
SSW1 Set - Loop on test
SSW1 Reset - End Testing

Parameters: D1-Utility Test Selection
H2=1, Punch; H2=2, Read
H3-Defined by the utility test selected
H4-Defined by the utility test selected

Examples: TST3, 0, 1
Punch EBCDIC cards using the pattern specified by the most recent 'DATA' directive.

TST3, 2, 1, 4D
If the card punch last specified in a SYST directive was a model 7165, punch an EBCDIC card with the pattern specified by the most recent data directive.

TST3, 3, 1, 52
Punch cards with a single punch in row 1 of column 52.

TST3, 3, 13, 5
Punch Cards with punches in all rows of column 5.

TST3, 4, 2
Perform a speed test on the last card reader specified in a SYST directive

TST3, 5, 1, 10, 10000
Punch 10 cards then delay 10 seconds. Repeat if SSW1 set

TST3, 6, 1, 0
Punch all functional subtest decks

TST3, 6, 2, 48
Read and verify the 50-card test deck

TST3, 7, 1, 001
Punch a binary card where the bit pattern of column 1 (X'001') is shifted by 1 throughout successive columns of the card (Col. 2 = X'002', Col. 3 = X'004',..)

## ORDER CODES

Card Punch Orders:

Model 7160 (EBCDIC)

| | |
|---|---|
| X'05' | Stack card in normal stacker. |
| X'0D' | If no error, stack card in normal stacker – on error, stack card in alternate stacker. |
| X'15' | Stack card in alternate stacker. |
| X'1D' | Stack card in alternate stacker. |

Model 7160 (Binary)

| | |
|---|---|
| X'01' | Stack card in normal stacker. |
| X'09' | If no error, stack card in normal stacker – on error, stack card in alternate stacker. |
| X'11' | Stack card in alternate stacker. |
| X'19' | Stack card in alternate stacker. |

Model 7165 (EBCDIC)

| | |
|---|---|
| X'05' | Stack card normally. |
| X'45' | Stack card normally and interrupt at data transmission complete. |
| X'0D' | Offset stack on error. |
| X'4D' | Offset stack on error and interrupt at data transmission complete. |
| X'15' | Offset stack. |
| X'1D' | Offset stack. |
| X'55' | Offset stack and interrupt at data transmission complete. |
| X'5D' | Offset stack and interrupt at data transmission complete. |

Model 7165 (Binary)

| | |
|---|---|
| X'01' | Stack card normally. |
| X'41' | Stack card normally and interrupt at data transmission complete. |
| X'09' | Offset stack on error. |
| X'49' | Offset stack on error and interrupt at data transmission complete. |
| X'11' | Offset stack. |
| X'19' | Offset stack. |
| X'51' | Offset stack and interrupt at data transmission complete. |
| X'59' | Offset stack and interrupt at data transmission complete. |

Card Reader Orders:

/ phys' Jnd'

Model 7120 (EBCDIC)

| | |
|---|---|
| X'06' | Stack card in normal stacker. |
| X'16' | Stack card in alternate stacker 1. |
| X'36' | Stack card in alternate stacker 2. |
| X'0E' | If no validity error or data overrun occurs, stack card in normal stacker; if validity error or data overrun occurs, stack card in alternate stacker 2. |
| X'1E' | If no validity error or data overrun occurs, stack card in alternate stacker 1; if validity error or data overrun occurs, stack card in alternate stacker 2. |
| X'3E' | Stack card in alternate stacker 2. |

Model 7120 (Binary)

| | |
|---|---|
| X'02' | Stack card in normal stacker. |
| X'12' | Stack card in alternate stacker 1. |
| X'32' | Stack card in alternate stacker 2. |
| X'0A' | If no data overrun occurs, stack card in normal stacker; if data overrun occurs, stack card in alternate stacker 2. |
| X'1A' | If no data overrun occurs, stack card in alternate stacker 1; if data overrun occurs, stack card in alternate stacker 2. |
| X'3A' | Stack card in alternate stacker 2. |

Model 7140 (EBCDIC)

| | |
|---|---|
| X'06' | Stack card in normal stacker. |
| X'16' | Stack card in alternate stacker. |
| X'36' | Stack card in normal stacker. |
| X'0E' | If no validity error or data overrun occurs, stack card in normal stacker; if validity error or data overrun occurs, stack card in alternate stacker. |
| X'1E' | If no validity error or data overrun occurs, stack card in normal stacker; if validity error or data overrun occurs, stack card in alternate stacker. |
| X'3E' | Stack card in normal stacker. |

Model 7140 (Binary)

| | |
|---|---|
| X'02' | Stack card in normal stacker. |
| X'12' | Stack card in alternate stacker. |
| X'32' | Stack card in alternate stacker. |
| X'0A' | If no data overrun occurs, stack card in normal stacker; if data overrun occurs, stack card in alternate stacker. |
| X'1A' | If no data overrun occurs, stack card in normal stacker; if data overrun occurs, stack card in alternate stacker. |
| X'3A' | Stack card in normal stacker. |

Note: Model's 7121 and 7122 accept all the above card reader orders, but offer no alternate stacking.

## NORMAL TDV STATUS

TDV SET 1

| | BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| MODEL | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 7160-1/2 | Data Overrun | Not Used | Read Check | Parity Error | Row 15 time | Test Switch | ← Not Used → | |
| 7165 | Data Overrun | Not Used | Punch Error | ← Not Used → | | | | |
| CARD READERS | Data Overrun | ← Not Used → | | | | | | |

## TEST MODE TDV STATUS

| | BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| MODEL/SET | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 7160-2 PUNCH/READ/VERIFY SET 2 | Punch Register PRO1 | Read Register PRO1 | Read Verify Bug RVCB4 | RVCB3 | RVCB2 | RVCB1 | Motor Speed | Chaining Mode |
| 7160-2 ROW, SKIP, DECODE SET 3 | Row Counter RCTD(MSB) | RCTC | TCTB | TCTA (LSB) | Skip Counter SCTA | SCTB | Binary Decode DATAB | EBCDIC Decode DATAE |
| 7160-2 DATA BUFFER SET 4 | Data Buffer DBO(MSB) | DB1 | DB2 | DB3 | DB4 | DB5 | DB6 | DB7(LSB) |

## AIO STATUS

| | BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| MODEL | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 7160 | Data Overrun | Not Used | Read Check (7160-2 Only) | ← Not Used → | | | | Stop Order Interrupt |
| 7165 | Data Overrun | Not Used | Punch Error | ← Not Used → | | | | |
| CARD READERS | Data Overrun | ← Not Used → | | | | | | |

# FUNCTIONAL SUBTESTS AND RELATED ERROR MESSAGES

## FAULT INDEX DESCRIPTION - FUNCTIONAL SUBTESTS

The fault index contains a brief description of each functional subtest and a list of associated error numbers with a brief description of each error. The subtests and error numbers are arranged in ascending sequence. The description of subtest NN is numbered NN00. The first two digits of the error number correspond to the associated subtest; the last two numbers correspond to the individual errors within the subtest.

TST1, 1 HIO, TIO, TDV and AIO Instr. Recog. HIO, TIO, TDV and AIO instructions are issued and condition codes, status tested.

0101 HIO instr. cond. codes or status error.
0102 TIO instr. cond. codes or status error.
0103 TDV instr. cond. codes or status error.
0104 AIO instr. cond. code error. Expected no interrupt recognition.

TST1, 2 SIO invalid order test. An SIO is issued with an invalid order and the controller is tested for UE status.

0201 SIO condition codes indicate SIO not accepted. Card punch (Order = X'02').
0202 SIO status error for invalid order. Card punch (Order = X'02').
0203 TIO status indicates contr. remains busy after invalid order. Card punch (Order = X'02').
0204 TIO status error after invalid order. Expected UE status and contr. ready. Card punch (Order = X'02').
0205 Terminal byte count not the same as starting byte count for invalid order. Expected term. BC = 120. Card punch (Order = X'02').
0211 SIO condition codes indicate SIO not accepted. Card reader (Order = X'01').
0212 SIO status error for invalid order. Card reader (Order = X'01').
0213 TIO status indicates contr. remains busy after invalid order. Card reader (Order = X'01').
0214 TIO status error after invalid order. Expected UE status and contr. ready. Card reader (Order = X'01').
0215 Terminal byte count not the same as starting byte count for invalid order. Expected term. BC = 120. Card reader (Order = X'01').
0221 SIO condition codes indicate SIO not accepted. Card reader (Order = X'03').
0222 SIO status error for invlaid order. Card reader (Order = X'03').
0223 TIO status indicates contr. remains busy after invalid order. Card reader (Order = X'03').
0224 TIO status error after invalid order. Expected UE status and contr. ready. Card reader (Order = X'03').
0225 Terminal byte count not the same as starting byte count for invalid order. Expected term. BC = 120. Card reader (Order = X'03').
0231 SIO condition codes indicate SIO not accepted. Card reader (Order = X'42').
0232 SIO status error for invalid order. Card reader (Order = X'42').
0233 TIO status indicates contr. remains busy after invalid order. Card reader (Order = X'42').
0234 TIO status error after invalid order. Expected UE status and contr. ready. Card reader (Order = X'42').
0235 Terminal byte count not the same as starting byte count for invalid order. Expected term. BC = 120. Card reader (Order = X'42').
0241 SIO condition codes indicate SIO not accepted. Card reader (Order = X'86').
0242 SIO status error for invalid order. Card reader (Order = X'86').
0243 TIO status indicates contr. remains busy after invalid order. Card reader (Order = X'86').
0244 TIO status error after invalid order. Expected UE status and contr. ready. Card reader (Order = X'86').
0245 Terminal byte count not the same as starting byte count for invalid order. Expected term. BC = 120. Card reader (Order = X'86').
0250 Read check verification. The read check flag should be set by the invalid order (Models 7160-1 and 7160-2).

TST1,3 Test mode selection. SIO issued to select and reset controller test mode. TDV is used to verify test mode. (CC2 = 1 - Test mode).

0301 SIO instr. cond. code or status error.
0302 TIO instr. indicates contr. busy beyond normal termination time for select test mode order (X'13').
0303 TIO indicates UE for select test mode order.
0304 TIO indicates status error for select test mode order.
0305 Test mode byte not taken by contr.
0306 Contr. performed data in instead of data out for test mode order.
0307 TDV cond. codes 1, 2 not equal 01 following test mode order.
0308 SIO cond. code or status error while contr. in test mode.
0309 TIO indicates cond. code or status error following test mode order to reset test mode.
0310 TDV cond. code or status error following test mode order to reset test mode.

TST1, 4 interrupt generation test. The following orders are issued for a 7160-2 controller: X'13' (Data byte = 00), and X'02' in order to test the ICE, IZC, and IUE interrupt generation. AIO and HIO instr's are used to test the interrupt clearing.

0401 TIO indicates IP status not present after X'13' order with ICE flag set in the IOCD.
0402 TIO indicates cond. code or status error after X'13' order with ICE flag set.
0403 AIO instr. cond. code, status or device address error following X'13' order raising IP.
0404 HIO instr. did not reset IP in controller.
0405 TIO indicates IP not set by X'13' order with IZC flag set in the IOCD.
0406 TIO indicates cond. code or status error after X'13' order with IZC flag set in the IOCD.
0407 AIO instr. cond. code, status or device address error after X'13' order with IZC flag set in the IOCD.
0408 AIO or HIO instr. did not reset IP in controller.
0409 TIO indicates invalid order with IUE flag did not set IP in the controller.
0410 TIO indicates cond. code or status error after invalid order with IUE flag set in IOCD. Expected UE and IP.
0411 AIO instr. cond. code, status or device error after invalid order with IUE flag set in the IOCD.
0412 TIO indicates status error after AIO or HIO instruction to clear IP.
0413 TIO indicates HIO or AIO instr. did not reset IP in contr.
0414 AIO instr. did not reset IP in the controller.
0420 'Interrupt pending' not reported by the Model 7160-1 punch.
0421 AIO status error detected (7160-1). Expecting 'interrupt pending' and 'unusual end' indications. Refer to printout for observed status.
0422 TIO status error detected (7160-1). AIO did not reset 'interrupt pending' in the controller.
0430 'Interrupt pending' not reported by the Model 7165 punch.
0431 AIO status error detected (7165). Expecting 'interrupt pending' and 'unusual end' indications. Refer to printout for observed status.
0432 TIO status error detected (reader). AIO did not reset 'interrupt pending' in the controller.
0440 'Interrupt pending' not reported by card reader.
0441 AIO status error detected (reader). Expecting 'interrupt pending' and 'unusual end' indications. Refer to printout for observed status.

TST1, 4 (Continued)

0442 TIO status error detected (7165). AIO did not reset 'interrupt pending' in the controller.

TST1, 5 IO interrupt generation. Using an invalid order, verify that the punch/reader can generate 'channel end' and 'unusual end' interrupts.

0501 Interrupt not received by the CPU
0502 TIO status error after CPU received an interrupt from contr.
0503 AIO cond. code, status or device address error after ICE interrupt received by the CPU.
0504 TIO indicates HIO did not reset IP in the controller.
0505 AIO cond. code, status or device address error after IZC interrupt received by the CPU.
0506 TIO indicates HIO did not reset IP in the contr.
0507 AIO cond. code, status or device address error after IUE interrupt received by the CPU.
0508 TIO indicates HIO did not reset IP in the contr.
0510 Timeout occurred – No interrupt received.
0511 Status error detected after interrupt received. Refer to printout for expected and observed status.

TST1, 6 command chaining. Two test mode orders are command chained and chaining verified. Invalid order command chained to test mode order is tested for command chain termination after invalid order.

0601 TIO indicates contr. busy beyond normal termination time for command chain operation.
0602 TIO indicates status error during command chaining.
0603 TIO indicates operational status error during command chaining.
0604 Byte count not 0 following command chaining.
0605 TIO indicates command chaining did not terminate with the second IOCD.
0606 Contr. busy with invalid order.
0607 TIO indicates UE not generated by contr. for invalid order.
0608 TIO indicates status error for invalid order command chained to test mode order.
0609 Terminal byte count not 1 for invalid order command chained to test mode order.
0610 Command chaining not terminated by UE of invalid order.

TST1, 9 motor speed (test mode). A binary order is issued in test mode and TDV status tested to insure punch motor speed indicator is set.

0901 Test mode selection error. Expected TDV CC1, 2 = 01.
0902 SIO status error for binary order.
0903 TIO indicates contr. busy with binary order beyond normal termination time. Motor speed indicator is set.
0904 TIO indicates status error for binary order.
0905 TDV set 3 indicates motor speed indicator not set following a binary order.
0906 TDV set 3 indicates motor speed indicator not set during a binary order.

TST1, 10 stop and interr. A stop and interr. (X'80') order is issued and interrupt generation is verified.

1001 Interrupt not generated by contr. for stop and interrupt order.
1003 TIO cond. code or status error after interrupt received.
1004 AIO cond. code, status or device address error for interrupt of the stop and interrupt order.
1005 TIO indicates status error after AIO cleared the interrupt.

TST1, 11 valid orders (test mode). The following valid orders are issued in test mode with a byte count of one: X'00', X'01', X'15', X'0D', X'11', X'15', X'19', X'1D'. Correct termination of each order is verified.

1101 Test mode selection error. Expected TDV CC1, 2 = 01.
1102 SIO status error for valid order.
1103 TIO indicates status error after valid order.
1104 TIO indicates contr. busy with valid order beyond normal termination time.

TST1, 12 one-byte data buffer (test mode). A binary order is issued in test mode to transfer one byte (X'00' thru X'FF') to the contr. one-byte buffer. TDV set 4 is used to verify the buffer contents.

1201 Test mode selection error. Expected TDV CC1, 2 = 01.
1202 TIO indicates contr. busy with binary order beyond normal termination time.
1203 TIO indicates UE for binary order.
1204 TIO indicates status error for binary order.
1205 TIO indicates operational status error for binary order.
1207 Terminal byte count incorrect. Expected 0, received 1.
1208 Data buffer contents not correct for binary order. See printout.

TST1, 13 punch order completion/chaining mode. (test mode). A binary order is issued in test mode with byte count = 120. Test is made that all bytes are transferred and the chaining modifier set.

1301 Test mode selection error. Expected TDV CC1, 2 = 01.
1305 TIO indicates contr. busy beyond normal termination time for a binary order with byte count of 120.
1306 TIO indicates UE for binary order with byte count of 120.
1307 TIO indicates status error for binary order.
1308 Terminal byte count not 0 for binary order with starting byte count of 120.
1309 Operational status error for a binary order.
1311 Chaining modifier not set.

TST1, 14 row counter (test mode). A binary order is issued in test mode and TDV set 2 is used to verify the row counter increments from card row 1 (X'0') to card row 15 (X'E').

1401 Test mode selection error. Expected TDV CC1, 2 = 01.
1402 TDV set 2 indicates row counter did not reset to row 1 (X'0') after the binary order. See printout.
1403 TDV set 2 indicates row counter did not increment correctly. See printout.
1404 TIO indicates status error for binary order.

TST1, 15 skip counter (test mode). Binary orders are issued to test the binary skip counter. TDV set 2 is used to verify that the 2-bit skip counter assumes the following states in sequence: binary 10, 11 and 00.

1501 Test mode selection error. Expected TDV CC1, 2 = 01.
1502 TDV set 2 indicates the skip counter did not increment correctly (10 to 11 to 00 to etc.) after the binary order.
1503 TIO indicates status error for binary order with byte count = 1.

TST1, 18 binary decode (test mode). A series of binary orders are issued with data bytes of X'00', X'01', X'02', D'04'... and TDV set 2 is used to verify the binary decode output (DATAB) for each row time.

1801 Test mode selection error. Expected TDV CC1, 2 = 01.
1802 SIO status error for binary order.
1803 TIO indicates contr. busy beyond normal time for one row.
1804 TDV set 2 indicates row counter did not increment correctly.
1805 TDV set 2 indicates row counter did not increment correctly.
1806 TDV set 2 indicates binary decode output (DATAB) incorrect.

TST1, 19 EBCDIC decode (test mode). A series of EBCDIC orders are issued with all EBCDIC bytes. TDV set 2 is used to determine the EBCDIC decode output for each character and row. EBCDIC decode is accumulated and verified at the conclusion.

1901 Test mode selection error. Expected TDV CC1, 2 = 01.
1902 SIO status error for EBCDIC order with byte count = 80.

TST1, 19 (Continued)

1903 TIO indicates contr. busy beyond normal termination time for EBCDIC order with byte count = 80.
1905 TDV set 2 indicates row counter incremented incorrectly.
1906 EBCDIC decode error. See printout.

TST1, 22 punch register/read register – shifting (test mode). An EBCDIC order is issued with X'40' bytes and TDV set 3 is used to verify that the EBCDIC decode output (0 for X'40') is shifted through the punch register and through the read register. The test is repeated with X'00' bytes (row punches T0981) to verify that a 1 bit is shifted to the read register.

2201 Test mode selection error. Expected TDV CC1, 2 = 01.
2202 Channel end interrupt not received for the EBCDIC order with byte count = 80.
2203 Status error for EBCDIC order. See printout.
2204 TDV set 3 indicates the 1 bit was not shifted thru to the read register column 1 position.
2205 TDV set 3 indicates the 0 bit was not shifted thru to the read register column 1 position.

TST1, 23 incorrect length (test mode). Binary orders with byte counts of 119 and 121 and EBCDIC orders with byte counts of 79 and 81 are issued to verify the incorrect length reporting.

2301 Test mode selection error. Expected TDV CC1, 2 = 01.
2302 Channel end interrupt not received.
2303 Status error after EBCDIC or binary order.
2304 IL status not reported.

TST1, 24 sense order (test mode). Sense orders are issued with byte counts of 1 to 80 in order to verify the contr. ability to transfer the 80-bit read register data to the CPU.

2401 Test mode selection error. Expected TDV CC1, 2 = 01.
2402 SIO status error for sense (X'04') order.
2403 TIO indicates contr. busy after normal termination time for sense order.
2404 Status error for sense order.

TST1, 27 punch register/read register – 0's and 1's (test mode). A series of EBCDIC orders are issued with X'40' bytes and sense orders used to verify that all 0's are transferred to the read register for all row times. The test is repeated to verify all 1's are transferred for all row times.

2701 Test mode selection error. Expected TDV CC1, 2 = 01.
2702 TIO status error for EBCDIC order.
2703 TIO status error for sense order.
2704 Read register not all 0's for EBCDIC order with X'40' bytes. See printout.
2705 Read register not all 1's for EBCDIC order. See printout.

TST1, 28 punch register/read register–random bits (test mode). A series of binary orders are issued to transfer alternating 1's and 0's and random bits to the punch and read registers. Sense orders are used to verify the read register contents.

2801 Test mode selection error. Expected TDV CC1, 2 = 01.
2802 SIO status error for binary order.
2803 TIO status error for binary order.
2804 TIO status error for sense order.
2805 Read register contents incorrect. See printout.

TST1, 29 punch register/read register – random bits (test mode). A series of EBCDIC orders are issued to transfer random bits to the punch and read registers. Sense orders are used to verify the read register contents.

2901 Test mode selection error. Expect TDV CC1, 2 = 01.
2902 SIO status error for EBCDIC order.
2903 TIO indicates status error for EBCDIC order.
2904 TIO indicates status error for sense order.
2905 Read register contents incorrect. See printout.

TST1, 33 read verification registers A, B–incrementing test mode. An EBCDIC order is issued to transfer X'40' bytes. TDV set 3 is used to verify that 'read verify reg. B' contains all 1's. (The 1's complement of 'read verif. reg. A' after it has received no EBCDIC decode 1 bits.) The test is repeated using data bytes producing 'read verif. reg. B' outputs of X'E' thru X'0'.

3301 Test mode selection error. Expected TDV CC1, 2 = 01.
3302 TIO indicates status error for EBCDIC order.
3303 TDV set 3 indicates read verification register B contents incorrect. See printout.

TST1, 34 read verification (test mode). EBCDIC orders are issued with varying patterns producing EBCDIC decode outputs of 0 thru 15. TDV set 3 and 1 are used to verify the read verif. reg B contents and the read verification indicator.

3401 Test mode selection error. Expected TDV CC1, 2 = 01.
3402 TIO indicates status error for EBCDIC order.
3403 TIO indicates status error for 2nd EBCDIC order.
3404 TDV set 3 indicates read verif. reg. B not X'F' after being decremented during 2nd EBCDIC order.
3405 TDV set 1 indicates read verification error indicator set.

X TST1, 36 card feed test #1. Verify that the device can correctly feed a blank card.

3601 Unsuccessful attempt to read an EBCDIC blank card. See printout for expected and observed status.
3602 Nonzero information was received from the card. Information should have been all blanks (X'40').
3603 Unsuccessful attempt to punch an EBCDIC blank card. See printout for expected and observed status.
3605 Unsuccessful attempt to read a blank binary card. See printout for expected and observed status.
3606 Nonzero information was received from the card. Information should have been all blanks (X'40').
3607 Unsuccessful attempt to punch a binary blank card. See printout for expected and observed status.

X TST1, 37 incorrect length. Verifies that the device can correctly respond to punch/read orders with the following byte counts: 79, 81, 119, 121.

3701 Timeout on punch/read operation. TIO indicated that SIO still not currently possible. Byte count = 79.
3702 Status error detected on punch/read operation. Refer to printout for expected and observed status. Byte count = 79.
3703 Timeout on punch/read operation. TIO indicated that SIO still not currently possible. Byte count = 81.
3704 Status error detected on punch/read operation. Refer to printout for expected and observed status. Byte count = 81.
3705 Timeout on punch/read operation. TIO indicated that SIO still not currently possible. Byte count = 119.
3706 Status error detected on punch/read operation. Refer to printout for expected and observed status. Byte count = 119.
3707 Timeout on punch/read operation. TIO indicated that SIO still not currently possible. Byte count = 121.
3708 Status error detected on punch/read operation. Refer to printout for expected and observed status. Byte count = 121.

X TST1, 38 punch blank cards. A series of 10 binary orders are issued to punch 10 blank cards, or a series of 12 binary orders are issued to read 12 cards.

3801 Status error detected on punch/read operation. Refer to printout for expected and observed status.

TST1, 38 (Continued)

3802 AIO status error on punch/read operation. Refer to printout for expected and observed status.

3803 TIO status error. Controller remained busy after operation.

TST1, 40 checkerboard pattern. A series of 10 cards are punched with a double checkerboard pattern. Visual verification is optional.

4001 IO interrupt not received for binary order.

4002 Punch status error for binary order punching checkerboard pattern.

TST1, 41 verify double checkerboard pattern. Read/verify double checkerboard pattern (deck of 10 cards).

4101 Timeout on read operation. Refer to printout for expected and observed status.

4102 Incorrect data entered by card reader. Refer to printout for failing columns.

TST1, 43 read brushes - column punching. A series of 80 cards are punched with each column read brush tested by moving the column being punched from col 1 to col 80. All rows are punched. Visual verification is optional.

4301 SIO status error for binary order.

4302 TIO indicates status or terminal byte count error.

4303 TDV indicates read check error for indicated column. See printout.

TST1, 44 read brushes - row punching. A series of 12 cards are punched with each column read brush tested by moving the rows being punched from row 9 thru row 12. Visual verification is optional.

4401 SIO status error for binary order.

4402 TIO status or terminal byte count error for binary order.

4403 TDV indicates read check error.

TST1, 45 read check - EBCDIC punching. A series of 10 EBCDIC cards are punched with random patterns. Read check is verified.

4501 Status error detected after binary punch operation. Refer to printout for expected and observed status.

TST1, 46 interrupt at data transmission complete. Verify that for a model 7165 card punch, the following orders generate an interrupt at data transmission complete: (X'45', X'4D', X'55', X'5D', X'41', X'49', X'51', X'59').

4601 Timeout occurred - No interrupt received (Order = X'45').

4602 AIO/TIO status error detected (Order = X'45'). Refer to printout for expected and observed status.

4603 Timeout occurred - No interrupt received (Order = X'4D').

4604 AIO/TIO status error detected (Order = X'4D'). Refer to printout for expected and observed status.

4605 Timeout occurred - No interrupt received (Order = X'55').

4606 AIO/TIO status error detected (Order = X'55'). Refer to printout for expected and observed status.

4607 Timeout occurred - No interrupt received (Order = X'5D').

4608 AIO/TIO status error detected (Order = X'5D'). Refer to printout for expected and observed status.

4609 Timeout occurred - No interrupt received (Order = X'41').

4610 AIO/TIO status error detected (Order = X'41'). Refer to printout for expected and observed status.

4611 Timeout occurred - No interrupt received (Order = X'49').

4612 AIO/TIO status error detected (Order = X'49'). Refer to printout for expected and observed status.

4613 Timeout occurred - No interrupt received (Order = X'51').

4614 AIO/TIO status error detected (Order = X'51'). Refer to printout for expected and observed status.

4615 Timeout occurred - No interrupt received (Order = X'59').

4616 AIO/TIO status error detected (Order = X'59'). Refer to printout for expected and observed status.

TST1, 48 punch 50-card deck. 25 binary cards followed by 25 EBCDIC cards are punched with pattern which allow for visual verification.

4801 Punch status error.

TST1, 49 read 50-card deck. The 50-card deck punched by TST1, 48 is verified.

4901 Read status error and/or pattern error detected on punched card. See printout.

TST1, 50 trans. error test (reader). A prepunched invalid-coded EBCDIC card is used to test the invalid EBCDIC code logic of the card reader.

5001 Unsuccessful attempt to read the card. Interrupt not received from the device.

5002 Read status error detected. Refer to printout for expected and observed status.

5003 Nonzero data was entered into the input buffer. All data read from the card should have been zero.

TST1, 51 automatic mode switch test (reader). A prepunched mode-switching card is used to test the ability of the card reader to automatically switch from automatic to binary mode when rows 1 and 2 of column 1 contain holes.

5101 Timeout. TIO cond. codes indicate that the device did not return to the 'ready' state after feeding a card.

5102 TIO status error detected. Refer to printout for expected and observed status.

5103 Error detected in observed data. Refer to printout for failing columns.

TST1, 52 transmission error test (punch). Any prepunched card is used to test the ability of the punch to detect extraneous punches.

5201 Unsuccessful attempt to punch the card. Interrupt not received from the device.

5202 Punch status error detected. Refer to the printout for expected and observed status.

FUNCTIONAL TEST (TST1) (SS1 = 0, SS3 = 1)
INITIALIZING CONDITIONS AND EXPECTED RESULTS

1. Initializing Conditions:
Card Reader Test: (All Models)
The following subtests will expect the following number of cards with their respective patterns to be in the card reader before each subtest

| Subtest | Number of cards | Pattern of Each Card |
|---|---|---|
| 36 | 2 | Blank |
| 37 | 4 | Blank |
| 38 | 12 | Blank (Command Chained) |
| 41 | 10 | Double Checkerboard |
| 49 | 50 | 50-Card Test Deck |
| 50 | 1 | Invalid-Coded EBCDIC Card |
| 51 | 1 | Mode Switching Card |

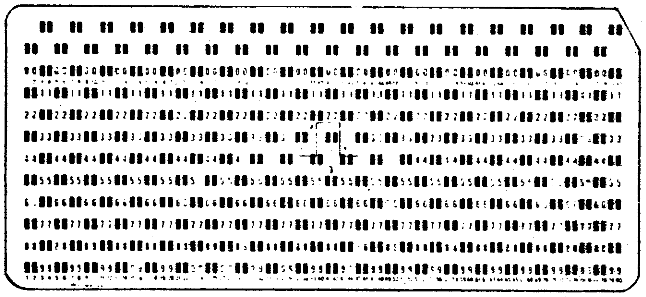
2. Expected Results:
Card Punch Test:
Expected Results of each Subtest.

| | Subtest | Number of Cards | Pattern of Each Card |
|---|---|---|---|
| Model 7160 | 36 | 2 | Blank |
| | 38 | 10 | Random (Command Chained) |
| | 40 | 10 | Double Checkerboard |
| | 43 | 80 | All Rows of a Column |
| | 44 | 12 | All Columns of a Row |
| | 45 | 10 | Random |
| | 48 | 50 | Standard Test Deck |
| | 52 | 2 | Operator Loads a Prepunched Deck into the Punch |
| Model 7165 | 36 | 2 | Blank |
| | 37 | 4 | Blank |
| | 38 | 10 | Blank (Command Chained) |
| | 40 | 10 | Double Checkerboard |
| | 43 | 80 | All Rows of a Column |
| | 44 | 12 | All Columns of a Row |
| | 45 | 10 | Random |
| | 46 | 8 | Random (4 Offset Stacked) |
| | 48 | 50 | Standard Test Deck |

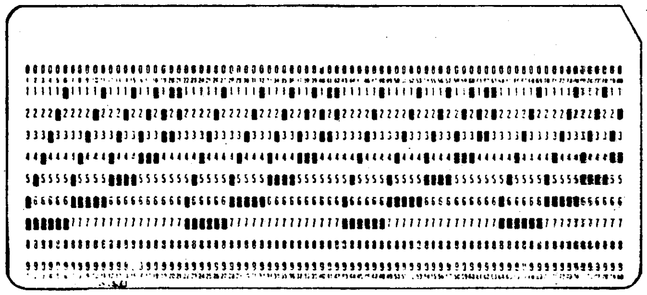
TEST/DEVICE REFERENCE TABLE

| Test | Device Model Numbers | | | | | | | Not Used |
|---|---|---|---|---|---|---|---|---|
| | 7160-1 | 7160-2 | 7165 | 7120 | 7121 | 7122 | 7140 | |
| TST0 | X | X | X | X | X | X | X | |
| TST1 | | | | | | | | |
| 1 | X | X | X | X | X | X | X | |
| 2 | X | X | X | X | X | X | X | |
| 3 | | X | | | | | | |
| 4 | X | X | X | X | X | X | X | |
| 5 | X | X | X | X | X | X | X | |
| 6 | | X | | | | | | |
| 7 | | | | | | | | X |
| 8 | | | | | | | | X |
| 9 | | X | | | | | | |
| 10 | X | X | | | | | | |
| 11 | | X | | | | | | |
| 12 | | X | | | | | | |
| 13 | | X | | | | | | |
| 14 | | X | | | | | | |
| 15 | | X | | | | | | |
| 16 | | | | | | | | X |
| 17 | | | | | | | | X |
| 18 | | X | | | | | | |
| 19 | | X | | | | | | |
| 20 | | | | | | | | X |
| 21 | | | | | | | | X |
| 22 | | X | | | | | | |
| 23 | | X | | | | | | |
| 24 | | X | | | | | | |
| 25 | | | | | | | | X |
| 26 | | | | | | | | X |
| 27 | | X | | | | | | |
| 28 | | X | | | | | | |
| 29 | | X | | | | | | |
| 30 | | | | | | | | X |
| 31 | | | | | | | | X |
| 32 | | | | | | | | X |
| 33 | | X | | | | | | |
| 34 | | X | | | | | | |
| 35 | | | | | | | | X |
| 36 | X | X | X | X | X | X | X | |
| 37 | | | X | X | X | X | X | |
| 38 | X | X | X | X | X | X | X | |
| 39 | | | | | | | | X |
| 40 | X | X | X | | | | | |
| 41 | | | | X | X | X | X | |
| 42 | | | | | | | | X |
| 43 | X | X | X | | | | | |
| 44 | X | X | X | | | | | |
| 45 | X | X | X | | | | | |
| 46 | | | X | | | | | |
| 47 | | | | | | | | X |
| 48 | X | X | X | | | | | |
| 49 | | | | X | X | X | X | |
| 50 | | | | X | X | X | X | |
| 51 | | | | X | X | X | X | |
| 52 | X | X | | | | | | |
| TST2 | X | X | X | X | X | X | X | |
| TST3 | | | | | | | | |
| 0 | X | X | X | X | X | X | X | |
| 1 | X | X | X | X | X | X | X | |
| 2 | X | X | X | X | X | X | X | |
| 3 | X | X | X | | | | | |
| 4 | X | X | X | X | X | X | X | |
| 5 | X | X | X | X | X | X | X | |
| 6 | X | X | X | X | X | X | X | |
| 7 | X | X | X | X | X | X | X | |

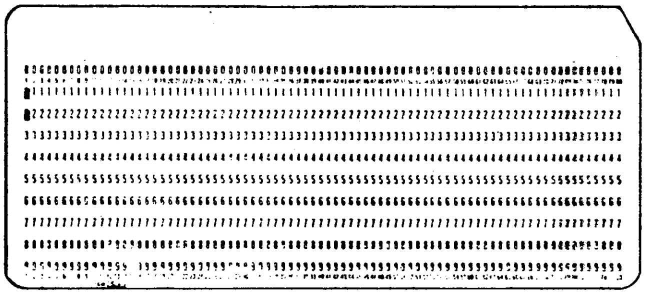
## CARD SAMPLES (TST1)



Double Checkerboard Pattern, 10 Identical Cards (TST1, 40 and 41)

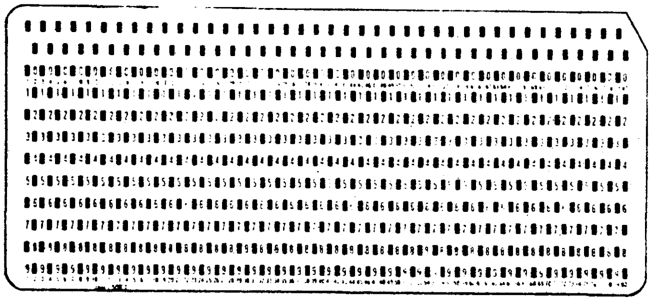


Transmission Error Test Card (TST1, 50)



Automatic Mode Switching Card (TST1, 51)

## 50 CARD TEST DECK (TST1, 48 AND 49)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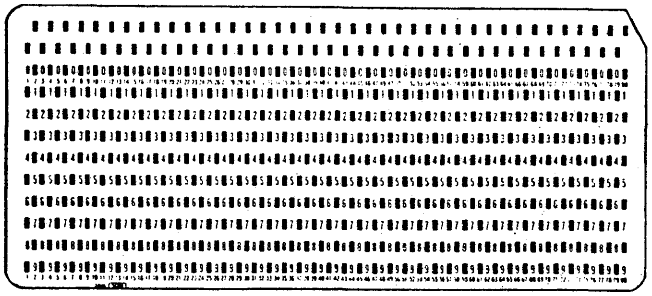
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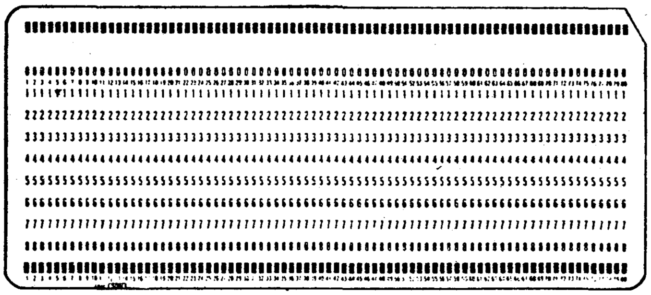
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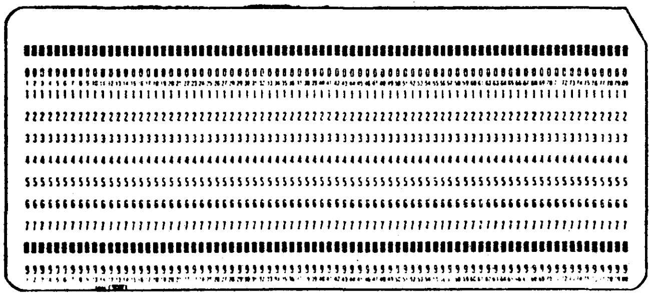
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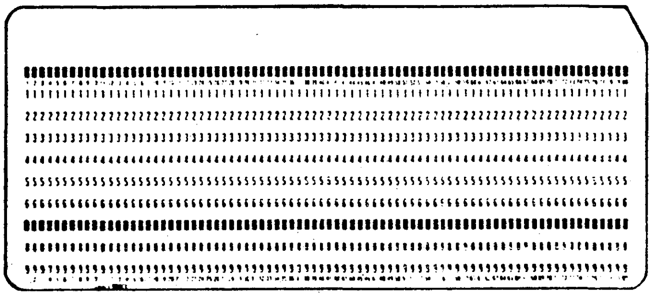
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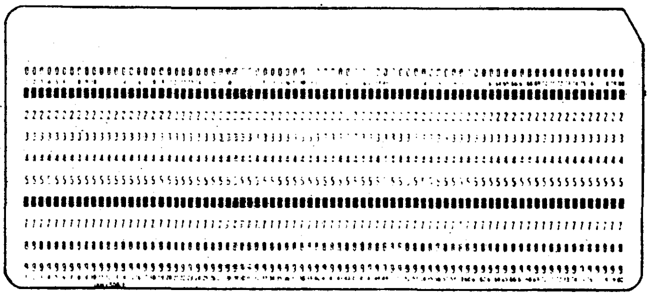
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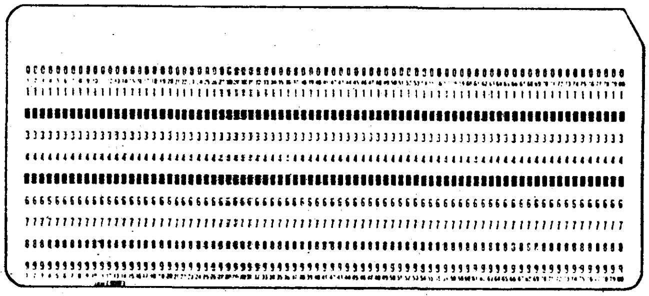
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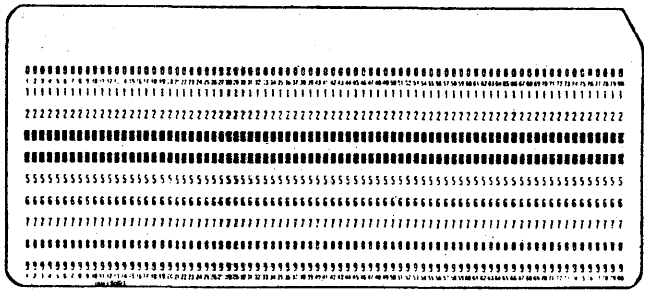
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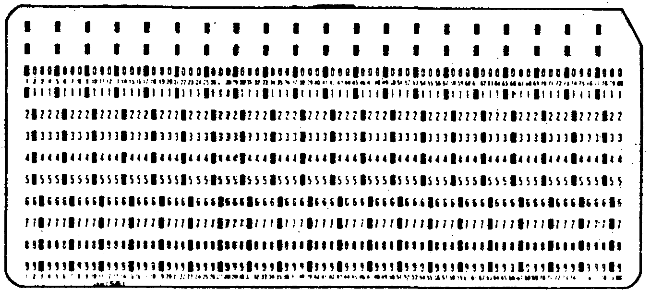
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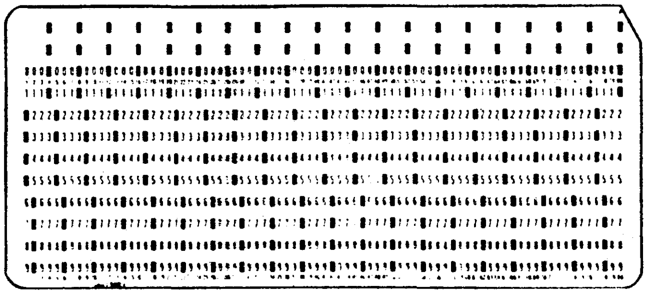
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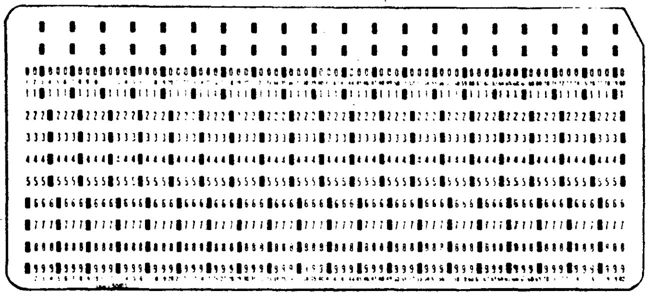
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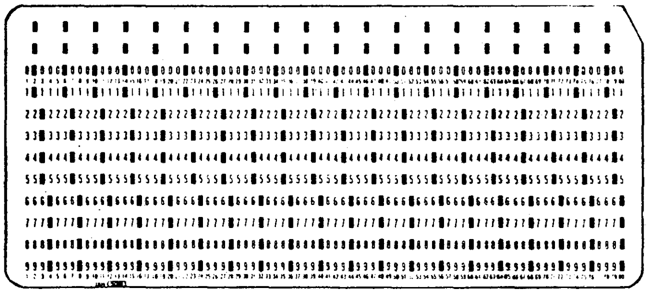
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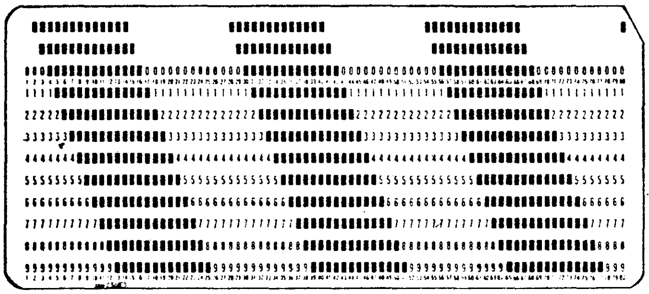
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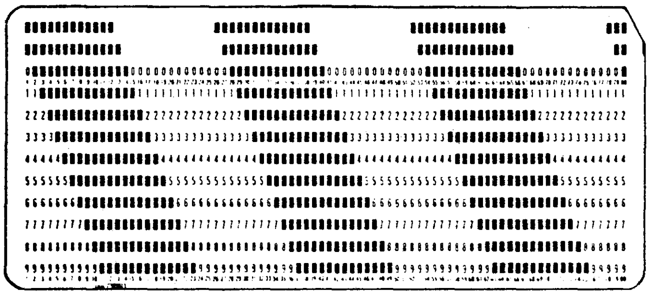
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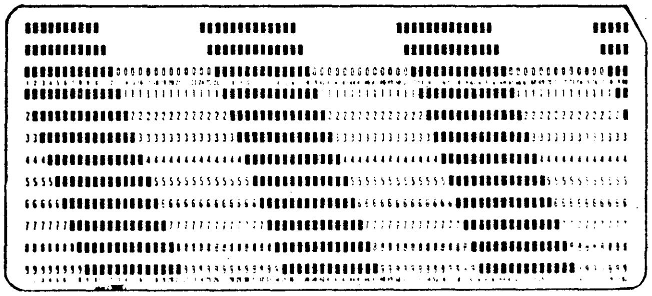
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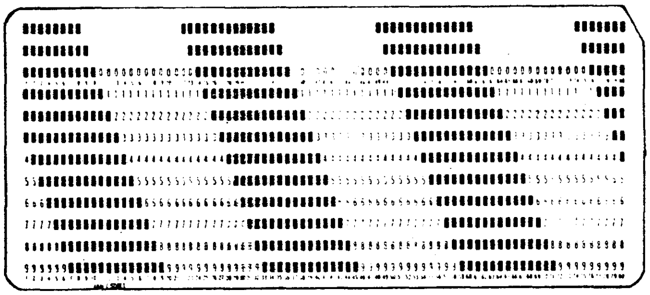
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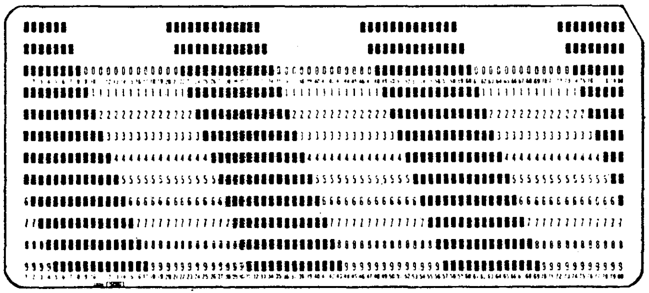
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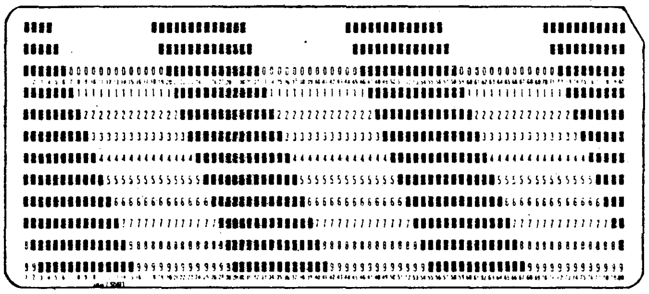
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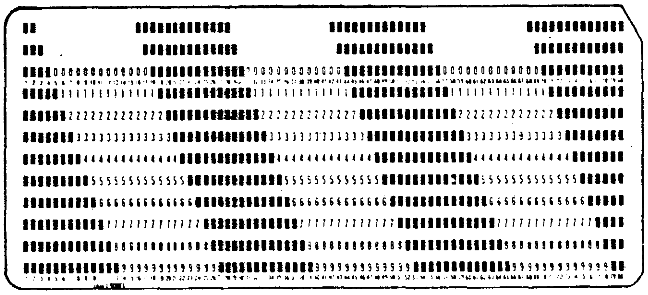
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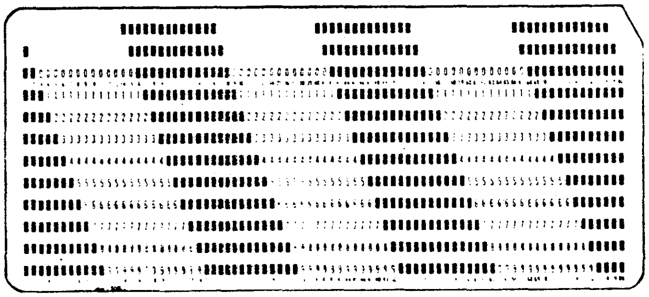
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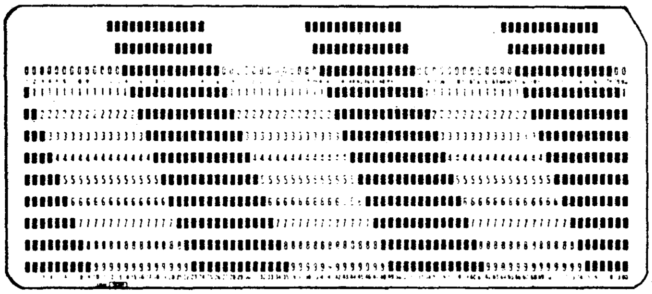
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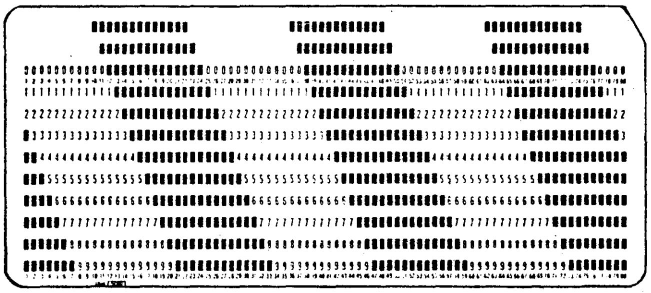
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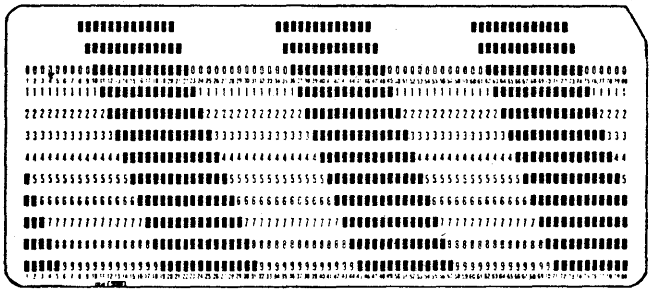
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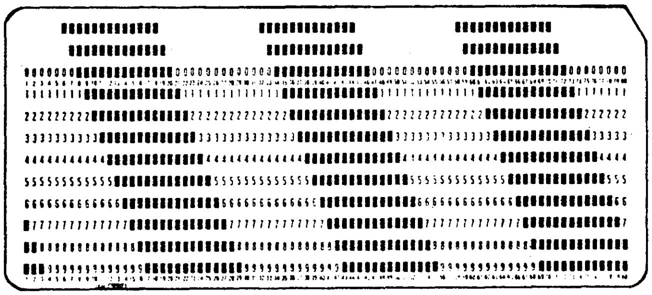
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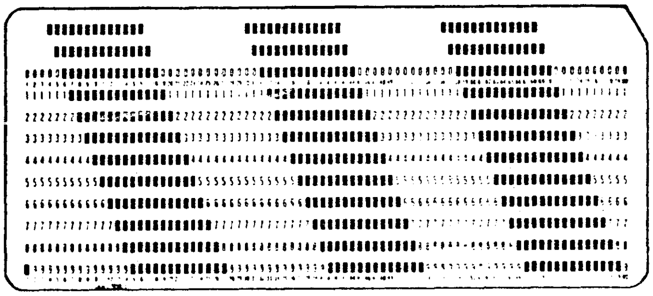
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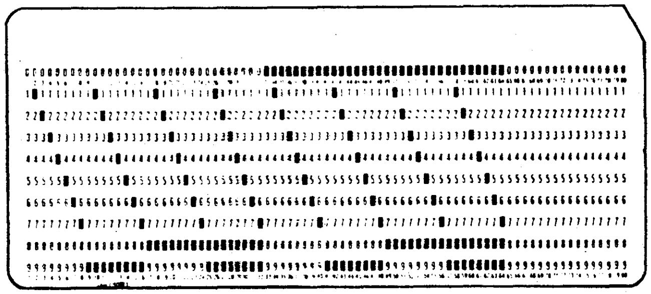
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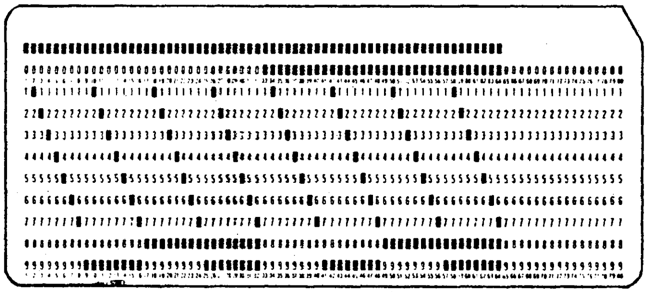
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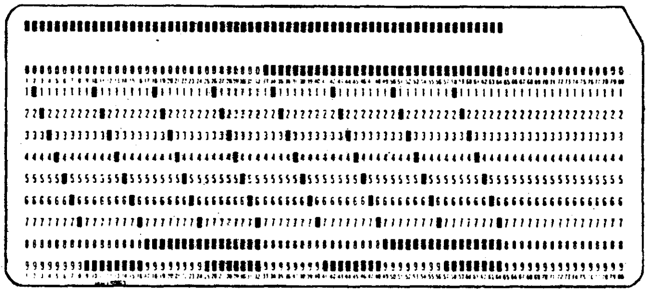
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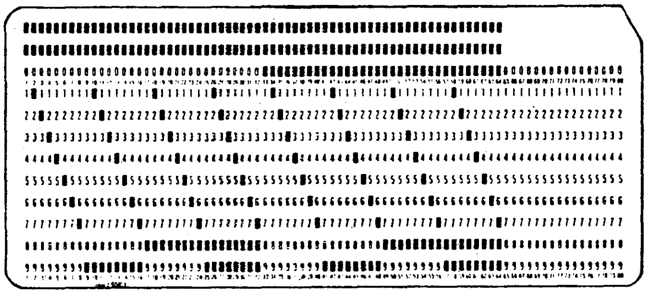
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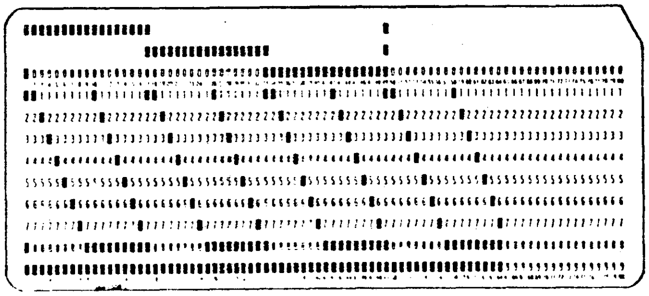
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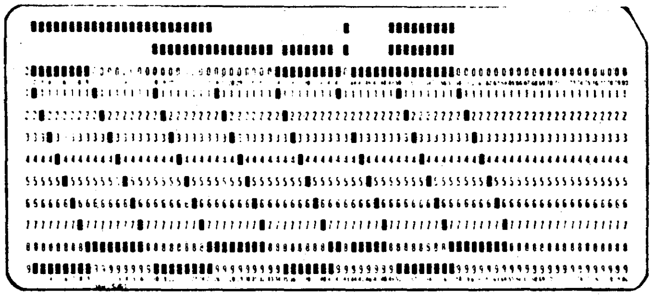
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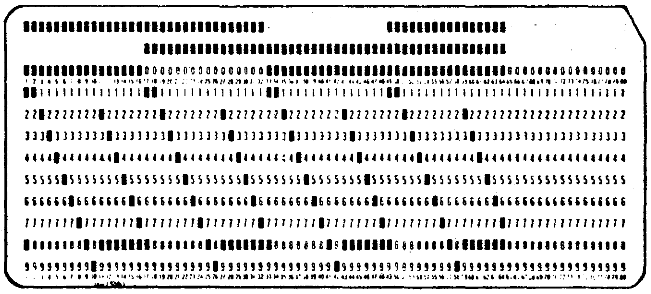
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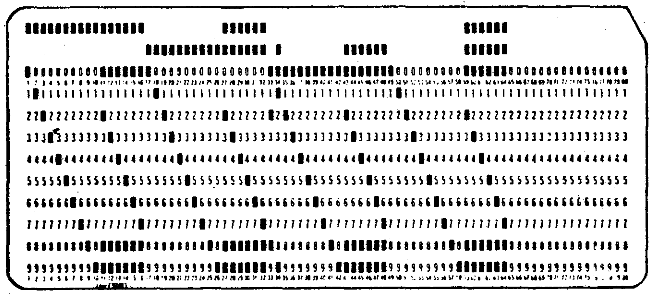
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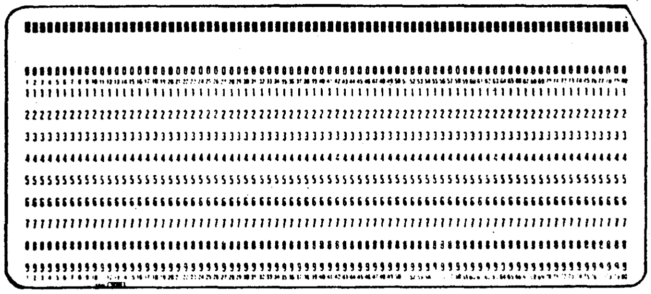
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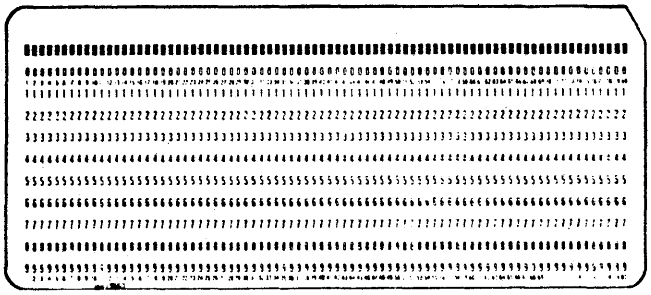
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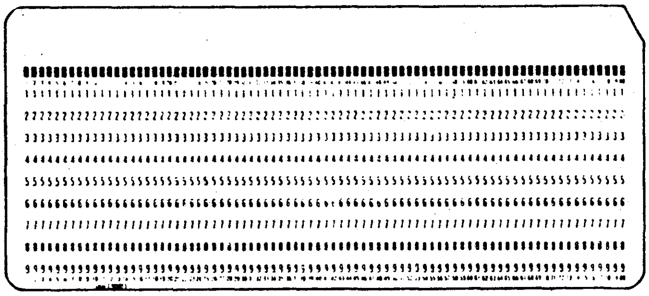
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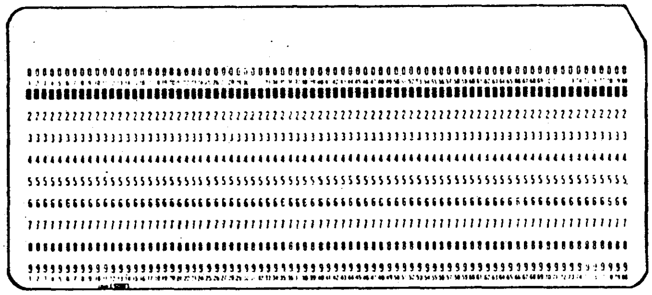
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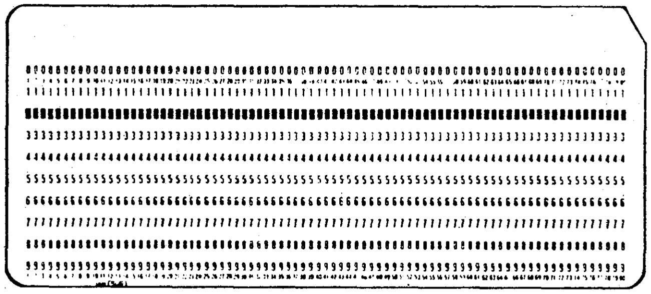
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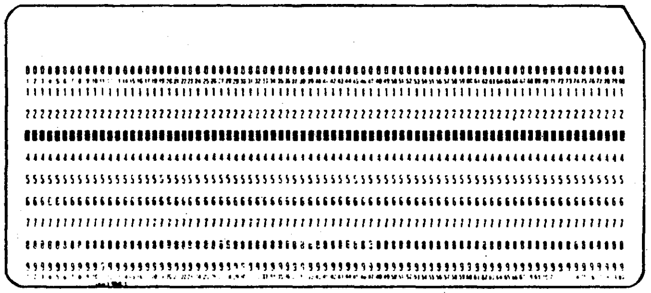
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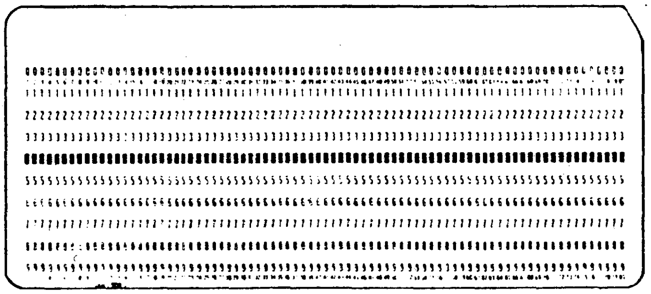
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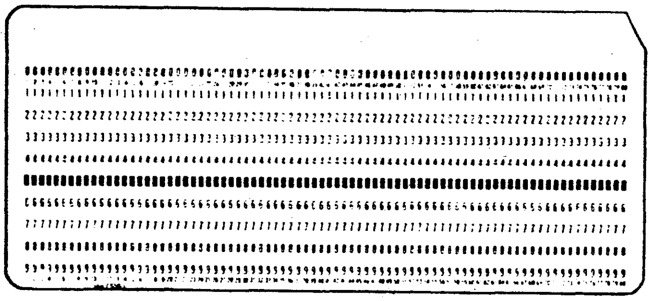

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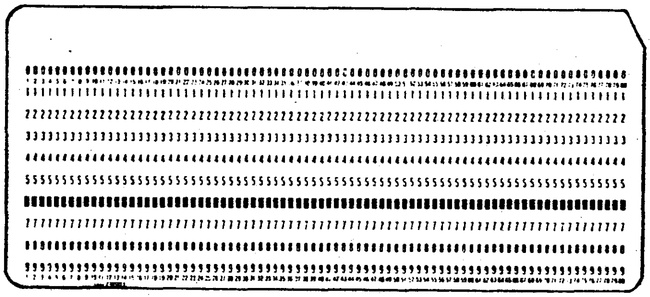

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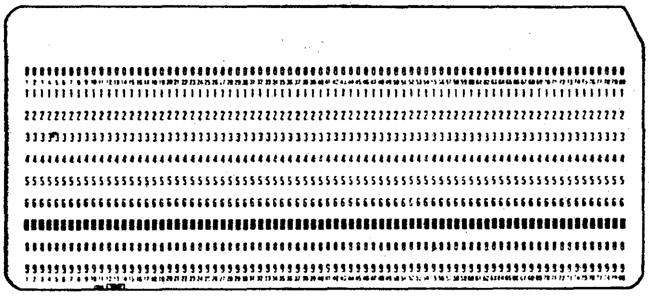

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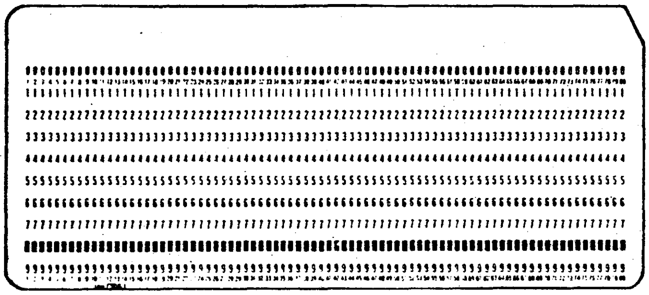

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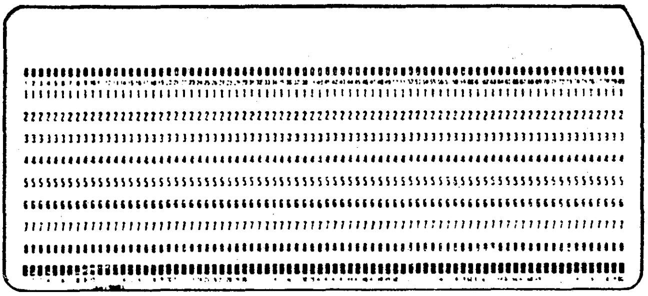

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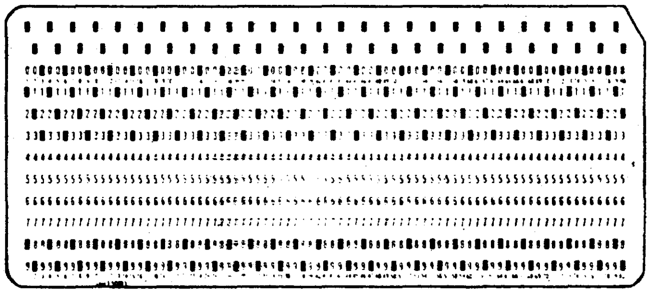

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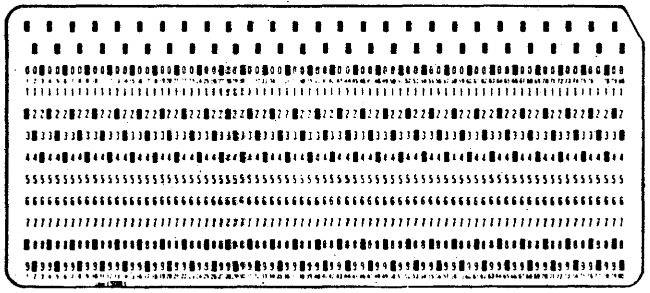

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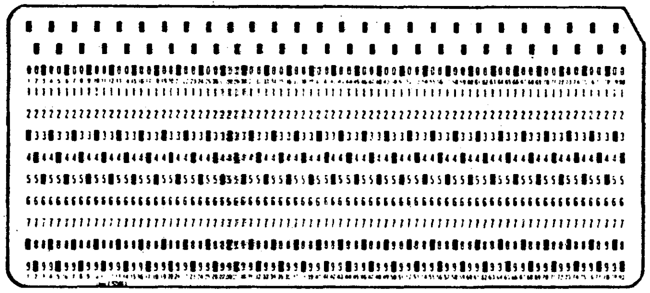

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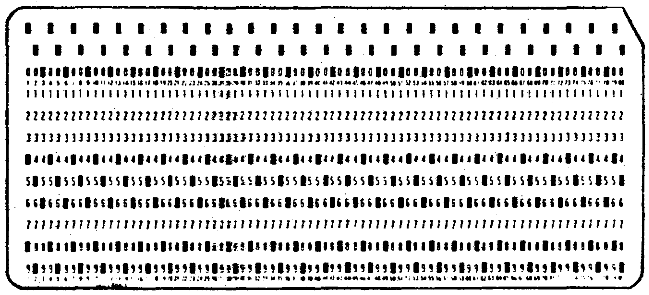

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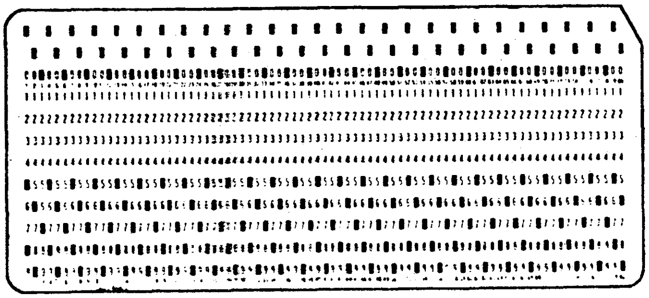


Card 50

# Section 6

# SIGMA 5 - 9
# COMPREHENSIVE RAD/CARTRIDGE DISK TEST (COMPR RAD)

## PROGRAM NO. 705730

## Section 6

## CONTENTS

Page

Subject Model . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 6-1
Required Equipment . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 6-1
Program Prerequisites . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 6-1
General Operating Procedures . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 6-1
Directives . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 6-2
Start Procedure . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 6-3
Program Test Description . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 6-4
Order Codes . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 6-4
TDV and AIO Status . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 6-4
Test Mode Data Byte . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 6-5
Addressing Format . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 6-5
Functional Subtests and Related Error Messages . . . . . . . . . . . . . . . . . 6-6

# 6. SIGMA 5–9 COMPREHENSIVE RAD/CARTRIDGE DISK TEST (COMPR RAD)

**SUBJECT MODEL**-- RAD Controllers, Model numbers 7201, 7211, 7231, New Extended Interface Controllers, Model numbers 7201-3, 7231-3, Cartridge Disk (CD) Controller 7250, RAD Storage Units, Model numbers 7202, 7203, 7204, 7212, 7232, Cartridge Disk (CD) Drives 7251, 7252

**REQUIRED EQUIPMENT** -- Minimum Memory Size: 16K; Input Device: Card Reader, Paper Tape Reader or Magnetic Tape Unit; Output Device: Keyboard Printer or Line Printer

## PROGRAM PREREQUISITES

None

## GENERAL OPERATING PROCEDURES

General operating procedures of the Sigma 5 through 9 Diagnostic Program Monitor (DPM), apply to this program.

**DIRECTIVES** - directives are entered after a "!" is typed out

| Name | Format | Parameter | | | |
|---|---|---|---|---|---|
| | | ID | Definition | Value Range | Standard Value (default) |
| Program Directives - Environmental Directives | | | | | |
| System Environment | SYST, D1, D2, H3, H4, D5, H6, [, H7, D8, H9 . . . , H25, D26, H27] | D1 | Controller model number | 7201, 7211, 7231, 7250 | |
| | | H2 | IOP Type and Revision number | H2 = 000000XX; MIOP<br>H2 = 000001XX; SIOP<br>H2 = 00000X03; (7201-3, 7231-3)<br>H2 = 00000X00; (all other RADs) | |
| | | H3 | Valid IOP and Controller but invalid Storage Unit address | 80 ~ 1FFF (If blank, or 0, or 8 units are specified, TST1, 2 is skipped) | |
| | | H4 | Device address of the first RAD/CD | 80 ~ 1FFF 1FD | |
| | | D5 | Model number of the first Storage Unit | 7202, 7203, 7204, 7212, 7232, 7251, 7252 | |
| | | H6 | Write protection of the first Storage Unit | 00XY00ZW (See table for X, Y, Z, W at next page) | |
| | | H7<br>D8<br>H9 | Same as H4, D5, H6 except for the second RAD/CD | | |
| | | ⋮ | | | |
| | | H25<br>D26<br>H27 | Same as H4, D5, H6 except for the eighth RAD/CD | | |
| Program Directives - Testing Directives | | | | | |
| Comprehensive Test (all functional tests, 1 ~ 50, and random exerciser test) | TST0, D1, D2 | D1 | Number of ordered sequences executed by random exerciser | 0 ~ 99999999 | 5000 (D1 = 0) |
| | | D2 | Number of retries | 0 ~ 99999999 | 0 |
| Functional Test | TST1[, D1[, D2]] | D1 | The first subtest to be executed | 0 (all subtests) ~ 50 | 0 |
| | | D2 | Last subtest to be executed | 1 | D1 |
| Random Exerciser Test | TST2, D1, D2 | D1 | Number of cycles to be performed | D1 > 0 | |
| | | D2 | Number of retries before next cycle | D2 ≥ 0 | |
| Utility Test | TST3, D1, D2, D3, D4 | D1 | Surface test | 1 | |
| | | D2 | = 0, Write and read (verify data)<br>= 1, Write only<br>= 2, Read only (verify data)<br>= 3, Read only (no data verification)<br>= 4, Checkwrite | 0 ~ 4 | |
| | | D3 | Number of retries | D3 ≥ 0 | |
| | | D4 | Number of reads after write (when D2 = 0) | D4 > 0 | |
| Program Directives - Optional Directives | | | | | |
| Pattern selection (for Utility Test) | DATA, D1, H2, H3 | D1 | = 0, Fixed Pattern<br>= 1, Incremental Pattern<br>= 2, Random Pattern<br>= 3, Current Seek Address | 0 ~ 3 | |
| | | H2 | Pattern seed (for D1 = 0, 1, 2) | 00000000 ~ FFFFFFFF | |
| | | H3 | Incrementing constant (for D = 1) | | |
| Usable surface area limitation | SEEK, D1, D2, D3, D4 | D1 | Starting track (band) address | 0 ~ 511 (0 ~ 63) | |
| | | D2 | Starting sector address | 0 ~ 15 (0 ~ 81) | |
| | | D3 | Ending track (band) address | 0 ~ 511 (0 ~ 63) | |
| | | D4 | Ending sector address | 0 ~ 15 (0 ~ 81) | |
| Limitation of Error printouts | LIMT, D1, D2 | D1 | = 1 Limit Compare error printouts/sector to D2 | 1 | |
| | | D2 | Maximum number of printouts (No limit if D2 = 0) | D2 ≥ 0 | |
| Pass Control and Pass Count Printout for TST0, 2, 3 | LIMT, D1, D2, D3 | D1 | = 2 effect pass control only | 2 | |
| | | D2 | Number of passes after which pass count is to be printed out. | D2 ≥ 0 | |
| | | D3 | Total number of passes to be completed. | D3 ≥ 0 | |
| I/O buffer area definition | MEM [, H1, H2] | H1 | First location of I/O buffer area | Obtainable by typing in MEM/ | Area between Diag. Prog. and DPM |
| | | H2 | Last location of I/O buffer area | | |

Note: Parameter of any directive beginning with a D means decimal, with an H means hexadecimal

## DIRECTIVES (Continued)

Write Protection Parameter in SYST directive

| Models 7202, 7203, 7204 (16 sectors/track)<br>7232 (12 sectors/track) | | | | | | | |
|---|---|---|---|---|---|---|---|
| XY | Protected Tracks | Track Available | | | | ZW | Protected Tracks |
| | | 7202 | 7203 | 7204 | 7232 | | |
| 00 | None | - | - | - | - | 00 | None |
| 01 | 0 - 31 | - | - | - | - | 01 | All |
| 02 | 0 - 63 | - | - | - | - | 02 | 32 - 511 |
| 03 | 0 - 95 | - | - | - | - | 03 | 64 - 511 |
| 04 | 0 - 127 | - | - | - | - | 04 | 96 - 511 |
| 05 | 0 - 159 | | - | - | - | 05 | 128 - 511 |
| 06 | 0 - 191 | | - | - | - | 06 | 160 - 511 |
| 07 | 0 - 223 | | - | - | - | 07 | 192 - 511 |
| 08 | 0 - 255 | | - | - | - | 08 | 224 - 511 |
| 09 | 0 - 287 | | | - | - | 09 | 256 - 511 |
| 10 | 0 - 319 | | | - | - | 10 | 288 - 511 |
| 11 | 0 - 315 | | | - | - | 11 | 320 - 511 |
| 12 | 0 - 383 | | | - | - | 12 | 352 - 511 |
| 13 | 0 - 415 | | | - | - | 13 | 384 - 511 |
| 14 | 0 - 447 | | | - | - | 14 | 416 - 511 |
| 15 | 0 - 479 | | | - | - | 15 | 448 - 511 |
| 16 | All | | | - | - | 16 | 480 - 511 |

| Model 7212 (64 bands available)<br>(82 sectors/bank) | | | |
|---|---|---|---|
| XY | Protected Bands | ZW | Protected Bands |
| 00 | None | 00 | None |
| 01 | 0 - 3 | 01 | All |
| 02 | 0 - 7 | 02 | 4 - 63 |
| 03 | 0 - 11 | 03 | 8 - 63 |
| 04 | 0 - 15 | 04 | 12 - 63 |
| 05 | 0 - 19 | 05 | 16 - 63 |
| 06 | 0 - 23 | 06 | 20 - 63 |
| 07 | 0 - 27 | 07 | 24 - 63 |
| 08 | 0 - 31 | 08 | 28 - 63 |
| 09 | 0 - 35 | 09 | 32 - 63 |
| 10 | 0 - 39 | 10 | 36 - 63 |
| 11 | 0 - 43 | 11 | 40 - 63 |
| 12 | 0 - 47 | 12 | 44 - 63 |
| 13 | 0 - 51 | 13 | 48 - 63 |
| 14 | 0 - 55 | 14 | 52 - 63 |
| 15 | 0 - 59 | 15 | 56 - 63 |
| 16 | All | 16 | 60 - 63 |

NOTE: For 725X Cartridge Disks, the parameter must be set to zero.

## START PROCEDURE

1. Sense Switch Options, Monitor Directive Options, and Environmental Directives – Refer to DPM section of this manual.
2. Test Strategy Selection

| | Comprehensive Test | Functional Test | Random Exerciser Test | Utility Test |
|---|---|---|---|---|
| Recommended Application | Normal Usage | Solid Failure Detection and Specific Problem Analysis | Intermittent Failure Detection | Surface Test |
| | TST0 | TST1 | TST2 | TST3 |
| | None | None | TST1 | TST1 |
| Optional Directives | SEEK, LIMT, MEM | SEEK, LIMT, MEM | SEEK, LIMT, MEM | SEEK, LIMT, MEM, DATA |
| Subtests | All functional subtests (1 50) and random exerciser test | 49 subtests (see error messages for the test types) | 1. Exerciser Initiation: Random data written on entire surface<br>2. Random Selection of:<br>a. Device<br>b. Order Sequences<br>c. Buffer Areas<br>d. Buffer Length<br>e. Data | WRITE only<br>READ only (Verify data)<br>READ only (No data verification)<br>CHECKWRITE<br>WRITE/READ TEST |
| Error Message Format | 1. ERROR NO. DDDD LOC XXXX<br>2. Self-explanatory | ERROR NO. DDDD LOC XXXX | Self-explanatory | Self-explanatory |

## PROGRAM TEST DESCRIPTION

Test descriptions of each functional test are included at the beginning of each subtest error number in the Functional Subtest and Related Error Message Section.

## ORDER CODES

| | |
|---|---|
| X'01' | WRITE |
| X'02' | READ RECORD (Report any transmission error of "count done') |
| X'03' | SEEK |
| X'04' | SENSE |
| X'05' | CHECKWRITE |
| X'12' | READ SECTOR (Terminate data transfer and report any transmission error at end of current sector if error is encountered) |
| X'13' | TEST |

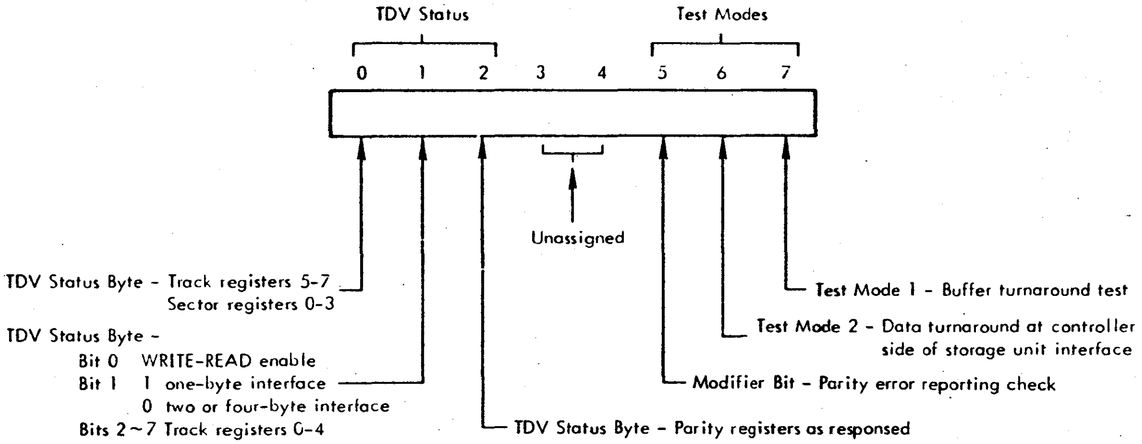
## TDV AND AIO STATUS

| BITS | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Data Overrun | Not Used | Sector Unavailable | Write-Protect Violated - | No Syncronization * | ◄── | NOT USED | ──► |

* For TDV on extended RAD controller and 725X only.

## TEST MODE DATA BYTE

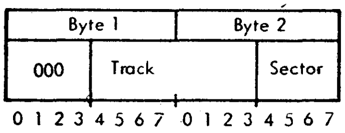
**For Models 7201-3, 7231-3 and 7250 only**


TDV Status
Test Modes
0 1 2 3 4 5 6 7
Unassigned
TDV Status Byte - Track registers 5-7
Sector registers 0-3
TDV Status Byte -
Bit 0 WRITE-READ enable
Bit 1 1 one-byte interface
0 two or four-byte interface
Bits 2 ~ 7 Track registers 0-4
TDV Status Byte - Parity registers as responsed
Test Mode 1 - Buffer turnaround test
Test Mode 2 - Data turnaround at controller side of storage unit interface
Modifier Bit - Parity error reporting check

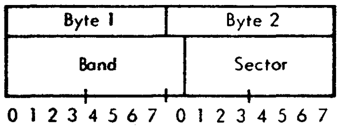
## ADDRESSING FORMAT

1. The format of the two byte sent to the RAD by a SEEK order is:

Model 720X, 723X, 725X

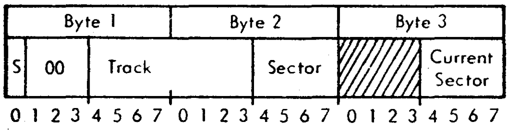

Byte 1
Byte 2
000
Track
Sector
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7

Model 7211

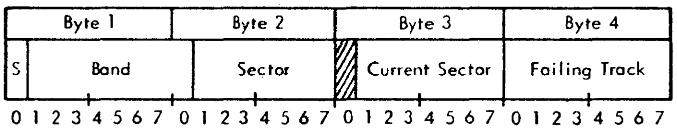

Byte 1
Byte 2
Band
Sector
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7

2. The format of the bytes received on a SENSE order is:

Model 720X, 723X, 725X


Byte 1
Byte 2
Byte 3
S
00
Track
Sector
Current Sector
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7

Model 7211


Byte 1
Byte 2
Byte 3
Byte 4
S
Band
Sector
Current Sector
Failing Track
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7

| Where: | |
|---|---|
| S | is the setting of the write-protect switch for the indicated track (band) (0 not write-protected; 1 write-protected) |
| Track (Band) | is the track (band) number selected by the RAD controller address register |
| Sector | is the sector number selected by the RAD controller address register |
| Current Sector | is the current sector position of the RAD |
| Failing Track | bits 0-7 indicate that track 0-7, respectively, have failed (8 tracks/band) |

NOTE: Bits 0, 1, and 2 of the track address are not used.

## FUNCTIONAL SUBTESTS AND RELATED ERROR MESSAGES

### FAULT INDEX DESCRIPTION – FUNCTIONAL SUBTESTS

The fault index contains a brief description of each functional subtest and a list of associated error numbers with a brief description of each error. The subtests and error numbers are arranged in ascending sequence. The description of subtest NN is numbered NN00. The first two digits of the error number correspond to the associated subtest; the last two numbers correspond to the individual errors within the subtest.

XX in the following messages indicates test number.

| | |
|---|---|
| XX00 | Watchdog timer trap |
| XX90 | A control fault was detected by the Test Mode Reset subroutine. |
| XX91 | A control fault was detected by the Set Test Mode 1 subroutine. |
| XX92 | A control fault was detected by the Set Test Mode 2 subroutine. |
| XX95 | A control fault was detected during the execution of the 'SEEK' subroutine. |
| XX96 | A control fault was detected during the execution of the 'WRITE' subroutine. |
| XX97 | A control fault was detected during the execution of the 'SENSE' subroutine. |

#### TST1, 01 Interrupt Pending Test

| | |
|---|---|
| 0115 | HIO did not reset pending interrupt, no reset generated. |

#### TST1, 02 Valid Controller Address but Invalid Storage Unit Address Test (Bypassed if H3 0 of SYST Directive)

| | |
|---|---|
| 0210 | Testing HIO, CC1 was 0 should be 1<br>a. Condition Code error<br>b. Device address recognition where one shouldn't exist. |
| 0211 | Testing HIO, CC2 was 1 should be 0<br>a. Condition Code error<br>b. Controller should indicate controller address recognition but not device address. |

#### TST1, 03 HIO Instruction Recognition Test

| | |
|---|---|
| 0310 | Testing HIO, CC1 was 1 should be 0<br>a. Condition Code error<br>b. I/O address not recognized |
| 0311 | Testing HIO, CC2 was 1 should be 0<br>a. Condition Code error<br>b. I/O address not recognized<br>c. I/O address recognized and device controller was busy |
| 0312 | Device status byte error during execution of HIO, only "device automatic" bit should be set. |

#### TST1, 04 TIO Instruction Recognition Test

| | |
|---|---|
| 0410 | Testing TIO, CC1 was 1 should be 0<br>a. Condition Code error<br>b. I/O address not recognized |
| 0411 | Testing TIO, CC2 was 1 should be 0<br>a. Condition Code error<br>b. I/O address recognized but SIO can't be accepted<br>c. I/O address not recognized |
| 0412 | Device status byte error during execution of SIO, only "device automatic" bit should be set. |

#### TST1, 05 TDV Instruction Recognition Test

| | |
|---|---|
| 0510 | Testing TDV, CC1 was 1 should be 0<br>a. Condition Code error<br>b. I/O address not recognized |
| 0511 | Testing TDV, CC2 was 1 should be 0<br>a. Condition Code error<br>b. I/O address not recognized<br>c. I/O address recognized but previous operation was terminated due to a fault condition. |
| 0512 | Testing TDV, status bits should be all zeros but were not. |

#### TST1, 06 SIO Instruction Recognition Test

| | |
|---|---|
| 0610 | Testing SIO, CC1 was 1 should be 0<br>a. Condition Code error<br>b. I O address not recognized |
| 0611 | Testing SIO, CC2 was 1 should be 0<br>a. Condition Code error<br>b. I O address not recognized<br>c. I O address recognized but SIO not accepted. (RAD was busy or device interrupt pending) |
| 0612 | Device status byte error from SIO, only "device automatic" bit should be set. |
| 0613 | Testing SIO, byte count was reduced by "STOP" order, should not be. |
| 0615 | Testing SIO, status bytes of TDV were not returned as all zeros. They should be. |
| 0616 | RAD was in "BUSY" state when it was halted. |
| 0617 | Device status byte erroneously returned from HIO, only "unusual end" and "device automatic" should be set. |
| 0619 | "Unusual end" bits were not reset by HIO, but should be. |

#### TST1, 07 Back to Back SIO Test – RAD should accept back to back "STOP" SIO's without watchdog timer trapping or returning incorrect status (Order STOP; Flags SKIP; Byte Count Variable).

| | |
|---|---|
| 0710 | SIO, CC2 was 1 should be 0<br>a. Condition Code error<br>b. I/O address not recognized |
| 0711 | Byte count should not be reduced between SIO's, but was. |
| 0712 | Device status byte error from SIO, only "device automatic" and "unusual end" bits should be set but were not. |

#### TST1, 08 Interrupt Generation Test – RAD should generate an interrupt and return status and condition code (Order STOP; Flags UE, SKIP; Byte Count Variable).

| | |
|---|---|
| 0810 | Device status byte error from TIO, only "device automatic" and "unusual end" bits should be set but were not. |
| 0811 | "Interrupt pending" bit was not set by TIO, but should be. |
| 0812 | TIO, CC2 was 0 should be 1<br>a. Condition Code error<br>b. RAD in "ready" condition with no interrupt pending<br>c. I/O address not recognized |
| 0813 | Operational status byte error of TIO, all bits should be 0 but were not. |
| 0814 | No interrupt occurred despite an actual interrupt pending. |
| 0815 | TDV, CC2 was 1 should be 0<br>a. Condition Code error<br>b. Previous operation terminated due to a fault condition |
| 0816 | TDV status bits were not returned as all 0's but should be |
| 0817 | "Interrupt pending" bit in TIO status should be reset by HIO but was not. |
| 0818 | Pending interrupt should be reset by HIO but was not (may be caused by not having HIO reset mode in IOP) |

#### TST1, 09 AIO Instruction Test – RAD should generate an interrupt with a "STOP" order then clear it with an "AIO". (Order STOP; Flags UE, SKIP; Byte Count Variable)

| | |
|---|---|
| 0910 | Device status byte error from TIO, only "device automatic", "interrupt pending", and "unusual end" bits should be set. |
| 0911 | "Interrupt pending" bit was not set during TIO, but should be. |
| 0912 | TIO, CC2 was 0 should be 1<br>a. Condition Code error<br>b. RAD is in "ready" condition with no device interrupt pending. |
| 0913 | Interrupt did not occur, even though one was pending. |
| 0914 | AIO did not clear the pending interrupt. |

TST1, 09 (Continued)

0915 AIO, CC1 was 1 should be 0
- a. Condition Code error
- b. Interrupt not recognized

0916 AIO returned address did not compare with the expected.

0917 AIO, CC1 was 0 should be 1
- a. Condition Code error
- b. Abnormal interrupt was not recognized

0918 "Unusual end" bit was not set during AIO, but should be.

0919 "Interrupt pending" bit of TIO was not reset by AIO, but should be.

TST1, 10 SEEK Test 1 - Verify order recognition, count done recognition, order-in generation, terminal order generation and length testing logic.

1010 Verifying execution of SEEK order, HTE flag, byte count equals 2. Check error message.

1015 Data in the output buffer was altered by the SEEK.

1020 Verifying execution of SEEK order, IUE flag, byte count equals 2. Check error message.

1030 Verifying execution of SEEK order, IZC flag, byte count equals 2. Check error message.

1040 Verifying execution of SEEK order, ICE flag, byte count equals 2. Check error message.

TST1, 11 SEEK Test 2 - Verify order recognition, count done recognition, order-in generation and length testing logic by SEEK operation with byte count less than 2.

*Do not apply to high speed RAD*

1110 Verifying "incorrect length" response to SEEK order, IUE flag, byte count equals 1. Check error message.

1115 Data in the output buffer was altered by the SEEK.

1120 Verifying "incorrect length" and "unusual end" response to SEEK order, HTE flag, byte count equals 1. Check error message.

1130 Verifying "channel end" response to SEEK order, ICE flag, byte count equals 1. Check error message.

TST1, 12 SEEK Test 3 - Verify order recognition, count done recognition, order-in generation, terminal order generation and length testing logic by SEEK operation with byte count greater than 2.

*Do not apply to high speed RAD or RAD on SIOP.
*Specify SIOP with SYST directive parameter 2.

1210 Verifying "incorrect length" and "channel end" response to SEEK order, ICE flag, byte count equals 3. See error message.

1215 Data in the output buffer was altered by the SEEK.

1220 Verifying "incorrect length" and "unusual end" response to SEEK order, HTE flag, byte count equals 3. See error message.

1230 Verifying RAD not reporting "unusual end" in response to SEEK order, IUE flag, byte count equals 3. See error message.

1240 Verifying RAD not reporting "zero byte count" in response to SEEK order, IZC flag, byte count equals 3. See error message.

TST1, 13 SENSE Test 1 - Verify order recognition, count done recognition, order-in generation and length testing logic by SENSE operation with byte count of 4 (for Model 7212) or 3 (for others).

1310 Verifying proper execution of SENSE order, IUE flag, byte count equals 4 (or 3). See error message.

1315 Data in the input buffer was not altered by the SENSE operation.

1316 More data was altered in input buffer than was expected by the SENSE operation.

1320 Verifying proper execution of SENSE order, HTE flag, byte count equals 3 (or 4). See error message.

1330 Verify "zero byte count" response to SENSE order, IZC flag, byte count equals 3 (or 4). See error message.

1340 Verifying 'channel end' response to SENSE order, ICE flag, byte count equals 3 (or 4). See error message.

TST1, 14 Sense Test 2 - Verify order recognition, count done recognition, order-in generation and length testing logic by SENSE operation with byte count less than required.

'Do not apply to high speed RAD'

1410 Verifying 'incorrect length' response to SENSE order, IUE flag, byte count equals 2. See error message.

1415 Data in the input buffer was not altered by the SENSE operation.

1416 More data was altered in input buffer than was expected by the SENSE operation.

1420 Verifying 'incorrect length' and 'unusual end' response to the SENSE order, HTE flag, byte count equals 2. See error message.

1430 Verifying 'channel end' response to the SENSE order, ICE flag, byte count equals 2. See error message.

TST1, 15 SENSE Test 3 - Verify order recognition, count done recognition, order-in generation and length testing logic by SENSE operation with byte count more than required.

1510 Verifying "incorrect length" and "channel end" response to SENSE order, ICE flag, byte count equals 5 (or 4). See error message.

1515 Data in the input buffer was not altered by the SENSE operation.

1516 More data was altered in input buffer than was expected by the SENSE operation.

1520 Verifying 'incorrect length' and 'unusual end' response to the SENSE order, HTE flag, byte count equals 4 (or 5). See error message.

1530 Verifying 'unusual end' response to the SENSE order, IUE flag, byte count equals 4 (or 5). See error message.

1540 Verifying no 'zero byte count' response to the SENSE order, IZC flag, byte count equals 4 (or 5). See error message.

TST1, 16 BUSY/NOT BUSY Test - Device is made busy and then ready.

*Do not apply to high speed RAD*
*Error message may be reported if an XP or MS RAD is connected to a SIOP*

1610 TIO, CC2 was 0 (ready) should be 1 (not ready).

1620 At the time of TIO, RAD storage unit and controller were NOT BUSY should be BUSY.

1630 TIO, CC2 was 1 (not ready) should be 0 (ready) after SEEK was accepted.

1640 RAD storage unit or controller remained BUSY after SEEK was accepted but should be NOT BUSY.

*Apply to Model 7201-3, 7231-3, 725X only*

TST1, 17 TEST Mode Test - Verify that controller can be set into and out of TEST Mode.

1710 Reset TEST Mode test, flags HTE, IUE and ICE, byte count = 1. A control fault occurred during accepting and decoding a TEST mode reset operation.

1715 Reset TEST mode test, TDV was issued, CC2 = 1 should be 0. Controller has falsely entered a TEST mode state. (To clear TEST mode, press RESET on the PCP).

1720-1727 Set TEST mode order test, flags HTE, IUE and ICE, byte count = 1. A control fault occurred during accepting the TEST mode order and entering the TEST mode state. The last digit of the error number (0-7) identifies the one-bit in the TEST Mode Data Byte.

1730-1737 Set TEST mode order test, TDV was issued, CC2 = 0 should be 1. Controller has not entered a TEST mode state. The last digit of the error number (0-7) identifies the one-bit in the TEST Mode Data Byte.

1740-1747 Reset TEST mode order test, flags HTE, IUE and ICE, byte count = 1. A control fault occurred during order execution. The last digit of the error number (0-7) identifies the one-bit in the TEST Mode Data Byte which was used to set the controller into TEST mode. TEST Mode Data Byte = X'00' when reset.

1750-1757 Reset TEST mode order test, TDV was issued. CC2 = 1 should be 0. Controller remains in TEST mode after a TEST mode reset. The last digit of the error number (0-7) indicates the one-bit of the TEST Mode Data Byte which was used to set the controller into TEST mode.

TST1, 17 (Continued)

1760 Set TEST mode order test, TEST Mode Status Byte = X'40'. Bit 1 of TDV Status Byte was 0 should be 1 (one-byte interface).

TST1, 18 Byte 'A' Data Path Test - The sequence of input data flow is as follows: IOP to 'CA' register to 'J' register to track and sector registers. When data is retrieved via the TDV TEST mode path, data flow is from the track and sector registers to the function response lines of the I/O bus. When data is retrieved via the SENSE operation, the output data flow is as follows: track and sector registers to 'K' register to 'DA' register to IOP.

*Apply to Model 7201-3, 7231-3, 725X only*

1825 Data or transfer fault in data path for byte 'A'. The following assumptions can be made about a single fault, as a likely cause of the fault:

| TDV | | SENSE | | |
|---|---|---|---|---|
| Byte 1 | Byte 2 | Byte 1 | Byte 2 | Conclusion |
| Good | Good | Good | Good | Test Passed |
| Bad | Bad | Good | Good | If single bit fault, check corresponding function response line.<br>If multiple bit fault, check transfer term to function response lines. |
| Bad | Good | Good | Good | Check transfer logic from track register to function response lines. |
| Good | Bad | Good | Good | Check transfer logic from track/sector register to function response lines. |
| Good | Good | Bad | Bad | If single bit fault, check corresponding bit in 'K' register, 'DA' register, data line driver.<br>If multiple bit fault, check transfer logic for 'K' to 'DA' register and 'DA' to data line drivers. |
| Good | Good | Bad | Good | Check transfer logic from track register to 'K' register. |
| Good | Good | Good | Bad | Check transfer logic from track/sector register to 'K' register. |
| Bad | Bad | Bad | Bad | If single bit fault, check corresponding bit of data line receiver, 'CA' register and 'J' register.<br>If multiple bit fault, check transfer logic from data line receivers to 'CA' register and 'CA' register to 'J' register. |
| Bad | Good | Bad | Good | If single bit fault, check corresponding track register FF.<br>If multiple bit fault, check transfer logic from 'J' register to track reg. |
| Good | Bad | Good | Bad | If single bit fault, check corresponding track/sector register FF.<br>If multiple bit fault, check transfer logic from 'J' register to track/sector register. |

TST1, 19 Current Sector Test - All sectors of the RAD can be sensed. Each sector is sensed once. When error occurs, a table will be output showing the number of times each sector was sensed.

TST1, 20 SEEK/SENSE Test - All sectors and tracks (bands) can be SEEKed then SENSEd. When error occurs, a table will be output showing the number of times each sector or track (band) was sensed.

2010 A sector was not found or was found more than once during SEEK and SENSE operations. (A table would be output).

2020 A track (band) was not found or was found more than once during SEEK and SENSE operations. (A table would be output).

TST1, 21 Track (Band) Availability and Not Write-Protect Test - All tracks (bands) allocated to the functional test are both available and not write-protected.

2110 The track (band) number listed on the printout should be available but was not.

2120 The track (band) number listed on the printout was reported write-protected in the TDV status but should not be.

2130 The track (band) number listed on the printout was reported write-protected in the returned sense word but should not be.

TST1, 22 Unavailability Test - Sector unavailable will be reported whenever an unavailable sector or track (band) is SEEKed.

2210 This test seeks unavailable sector. Check error message for the type of failures. (Does not apply to Model 7201, MS RAD).

2220 This test seeks unavailable track (band). Check error message for the type of failures.

TST1, 23 Command Chaining Test - The ability to detect and respond to command chaining.

2310 Command chaining did not occur properly.

2311 Command chaining did not take place after execution of HIO.

2312 Device did not stop on STOP order.

2320 Command chaining occurred on a STOP order. Check error message for the type of failure.

2321 Command chaining took place on a STOP order.

TST1, 24 FAM Write/READ Byte Count Test - This test is designed to operate the controller in TEST mode 1. It transfers from 1 to 16 bytes of data from the I/O buffer which starts on a word boundary to the FAM in the controller and subsequently transfers 1 to 16 bytes from the FAM to the I/O buffer.

*Apply to Model 7201-3, 7231-3, 725X only*

2421-2436 WRITE byte transfer test (test mode 1): Flags IUE, ICE; byte count 1 to 16. Error numbers 2421 to 2436 define the corresponding byte count of 1 to 16 which was used for the WRITE operation during which a control fault occurred.

2441-2456 READ byte transfer test (test mode 1): Flags IUE, ICE; byte count 1 to 16. Error numbers 2441 to 2456 define the corresponding byte count of 1 to 16 which was used for the READ operation during which a control fault occurred.

TST1, 25 FAM WRITE/READ Data Test-This test is designed to operate the controller in Test mode 1. This test checks the data path to and from the FAM and the 4-byte data path to and from the IOP.

*Apply to Model 7201-3, 7231-3, 725X only*

2510 WRITE test; Flags IUE, ICE and DC; byte count = 1. This test checks that 16 IOCD's can be executed to fill the FAM over the byte 'A' data path without control faults.

2511 WRITE test; Flags IUE and ICE, byte count = 16. This test checks that 16 bytes can be transferred to fill the FAM over the 4 byte interface (if it is installed) without control errors.

2512 WRITE test; Flags IUE, ICE and DC; byte count = 1. This test checks that 16 IOCD's can be executed to fill the FAM over the byte 'A' data path without control faults.

2520 READ test; Flags IUE, ICE and DC; byte count = 1. This test checks that 16 IOCD's can be executed to read the FAM via the byte 'A' data path without control faults.

2521 READ test; Flags IUE, ICE and DC; byte count = 1. This test checks that 16 IOCD's can be executed to read the FAM via the byte 'A' data path without control faults.

2522 READ test; Flags HTE, IUE and ICE; byte count = 16. This test checks that data can be transferred from the FAM via the 4 byte interface (if it is installed) without control faults.

2530 Data or transfer failure in data path 'A'. The failure is most likely in the output of the J register, the FAM, the input to the K register or in the associated control logic.

TST1, 25 (Continued)

2531 Data or transfer failure in data path 'B,C,D'. The failure is most likely in the input path from the data lines to the 'CB', 'CC' 'CD' registers or in the transfer logic to the J register.

2532 Data or transfer failure in data path 'B, C, D'. The failure is most likely in the output path to the IOP, the 'CB','CC','CD' registers, the 'DB','DC','DD' registers or associated control logic.

TST1, 26 FAM WRITE/READ Byte Alignment Test - This test is designed to operate the controller in TEST mode 1. It tests the ability of the controller to handle data patterns that do not start on word boundaries in memory.

*Apply to Model 7201-3, 7231-3, 725X only*

2620 WRITE alignment test; Flags IUE and ICE; byte count = 16. This test checks that a WRITE operation starting at byte 1 can be executed without control faults.

2621 WRITE alignment test; Flags IUE and ICE; byte count = 16. This test checks that a WRITE operation starting at byte 2 can be executed without control faults.

2622 WRITE alignment test; Flags IUE and ICE; byte count = 16. This test checks that a WRITE operation starting at byte 3 can be executed without control faults.

2623-2625 WRITE alignment test; Flags IUE and ICE; byte count = 16. These tests fill the FAM for the READ alignment test. Error indicates a control fault during the execution of a WRITE.

2630-2632 READ alignment test; Flags IUE, ICE; byte count = 16. These tests empty the FAM for this WRITE alignment test. Error indicates a control fault during the execution of a READ.

2633 READ alignment test; Flags IUE, ICE; byte count = 15. This test checks that a READ operation starting at byte 1 can be executed without control faults.

2634 READ alignment test; Flags IUE and ICE; byte count = 14. This test checks that a READ operation starting at byte 2 can be executed without control faults.

2635 READ alignment test; Flags HTE, IUE and ICE; byte count = 13. This test checks that a READ operation starting at byte 3 can be executed without control faults.

2640 Compare alignment data failure; WRITE starts with byte 1 and consists of 16 bytes; READ starts on word boundary and consists of 16 bytes. See compare printout for failing bytes.

2641 Compare alignment data failure; WRITE starts with byte 2 and consists of 16 bytes, READ starts on word boundary and consists of 16 bytes. See compare printout for failing bytes.

2642 Compare alignment data failure; WRITE starts with byte 3 and consists of 16 bytes, READ starts on word boundary and consists of 16 bytes. See compare printout for failing bytes.

2643 Compare alignment data failure; WRITE starts on word boundary and consists of 16 bytes, READ starts with byte 1 and consists of 15 bytes. See compare printout for failing bytes.

2644 Compare alignment data failure; WRITE starts on word boundary and consists of 16 bytes, READ starts with byte 2 and consists of 14 bytes. See compare printout for failing bytes.

2645 Compare alignment data failure; WRITE starts on word boundary and consists of 16 bytes, READ starts with byte 2 and consists of 13 bytes. See compare printout for failing bytes.

TST1, 27 READ Byte Counter Register Test - This test verifies the byte counter, the parity register, the data register, the data path from the parity register and the associated control logic. This test starts with a READ order of 1 byte. After each READ operation the byte count is incremented by 1 and another READ operation is performed. When the byte count equals 1 sector, the data is also verified.

*Apply to Model 7201-3, 7231-3, 725X only*

2710 READ byte counter test; Flags HTE, IUE and ICE; 1 ≤ byte count ≤ (BYTCURR). This test checks that all byte counts from 1 to (BYTCURR) can be performed. Error indicates that a control fault occurred during the execution of a READ.

2720 READ byte counter test; Flags HTE, IUE and ICE, byte count = (BYTCURR). This test checks that data for 1 sector can be READ. Error indicates that a control fault occurred during the execution of a READ.

2725 Data compare error after reading 1 sector in test mode 2. The READ data is generated by the byte counter. The data flow is from the byte counter to the parity register, data register, and J register and finally into the FAM. See compare printout for expected and observed data.

TST1, 28 Parity Error Test - This test verifies that the controller can detect and respond correctly to forced parity errors. Both READ X'02' and X'12' orders are executed for single and multiple sectors to verify correct data transfer termination.

*Apply to Model 7201-3, 7231-3, 725X only*

2810 Parity error test; order = X'02'; Flags HTE, IUE and ICE; byte count = 1 sector. This test checks that the modifier bit was set and detected by controller, and that the controller can detect and respond correctly to a parity error. Error indicates a control or detection fault occurred during the execution of the READ.

2820 Parity error test; order = X'02'; Flags HTE, IUE and ICE; byte count = 2 sectors. This test checks that the controller can detect and respond correctly to parity errors in multi length sectors.

2830 Parity error test; order = X'12', Flags HTE, IUE, ICE; byte count = 1 sector. This test checks that the controller can detect and respond correctly to parity errors in a single sector.

2840 Parity error test; order = X'12', Flags HTE, IUE, ICE; byte count = 1 sector + 3. This test checks that the controller can detect and respond correctly to parity errors in multi length sectors.

TST1, 29 WRITE Parity Generate Test - This test verifies the data path from the 'K' register to the data register, the parity generating logic, the preamble generating logic and its transfer to the data register and the generation of the WRITE enable signal. This test first writes data in a normal fashion to the controller, it then retrieves the resulting parity byte generated via the TDV test mode path.

*Apply to Model 7201-3, 7231-3, 725X only*

2910 WRITE parity generate test; Flags HTE, IUE and ICE; byte count = 1 sector. This test checks that a WRITE operation can be performed without control faults. No data will be written on the RAD.

2915 Parity generation or data transfer fault; the sequence of events tested by this test is as follows: The 'K' register is transferred to the data register, the data register is shifted one byte at a time to the parity generator logic, the parity register is shifted to store new generated parity bit. The error comparison printout displays 4 differently generated parity bytes compared to 4 expected parity bytes. If an error exists in the same 1 bit position for each parity byte the fault is most likely in the 'K' register. Otherwise the fault can be either in the shifting of the data register or parity register or in the parity generating logic.

2935 WRITE enable test; TDV status indicates that WRITE enable is true while the controller is in a READY state.

2940 WRITE enable test; error indicates, byte count was never decremented for WRITE operation.

2945 WRITE enable test; TDV status indicates that WRITE enable is false while the controller is writing.

TST1, 30 CHECKWRITE Byte Count Register Test - This test verifies that the checkwriting logic works properly. It first CHECKWRITEs patterns that are in error by 1 bit to verify that the error detection logic does indeed detect and report errors. It also CHECKWRITEs a good pattern to verify that the CHECKWRITE logic does not report errors on a matching pattern.

*Apply to Model 7201-3, 7231-3, 725X only*

3010 CHECKWRITE error test; Flags HTE, IUE and ICE; byte count = 1 sector. This test checks the ability of the controller to generate and report the detection of a data error when a bit from the IOP = 1 and the bit from the byte count register = 0.

3020 CHECKWRITE error test; Flags HTE, IUE and ICE, byte count = 1 sector. This test checks the ability of the controller to generate and report the detection of a data error when a bit from the IOP = 0 and the bit from the byte count register = 1.

TST1, 30 (Continued)

3030 CHECKWRITE test; Flags HTE, IUE and ICE; byte count = 1 sector. This test checks the ability of the controller to compare the pattern generated by the byte counter with an identical pattern sent from the IOP. Error indicates a data error.

TST1, 31 WRITE Test 1 - The ability to correctly receive and respond to WRITE a sector.

3110 Order WRITE, Flags HTE and IUE, byte count = 1 sector of data. Check error message.

3115 Data was altered in the output buffer by the WRITE operation.

3120 Order WRITE, flag IZC, byte count = 1 sector of data. Check error message.

3130 Order WRITE, Flag HTE and IUE, byte count = 2 sectors of data. Check error message.

3140 Order WRITE, Flag IZC, byte count = 2 sectors of data. Check error message.

TST1, 32 WRITE Test 2 - The ability to correctly receive and respond to WRITE less than a sector.

3210 Order WRITE, Flags HTE, IUE and ICE, byte count = less than 1 sector of data. Check error message.

3215 Data was altered in the output buffer by the WRITE operation.

TST1, 33 WRITE Test 3 - The ability to correctly receive and respond to WRITE greater than a sector.

3310 Order WRITE, Flags HTE, IUE and ICE, byte count = more than 1 sector of data. Check error message.

3315 Data was altered in the output buffer by the WRITE operation.

TST1, 34 Sector Increment Test - Verify that the SEEK address register can be incremented. Each sector or track (band) is SEEKed once. Any error detected a table will be output showing the number of times a particular sector or track (band) was observed.

3410 A sector was not found or was found more than once per track (band) during the execution of WRITE a sector and SENSE the increment of address register until the entire track (band) is attempted. A table should be output.

3420 A track (band) was not found or was found more than once during the execution of WRITE a sector and SENSE the increment of address register to the next higher track (band) until all tracks (bands) specified by 'SYST' and 'SEEK' directives are attempted. A table should be output.

3430 RAD did not report sector unavailable when the address register is incremented past the end of logical surface. This test is performed only if the end of the logical surface is available and not limited by 'SYST' and 'SEEK' directives.

TST1, 35 READ Test 1 - Ability to correctly receive and respond to READ (order X'02') a sector.

3510 No track (band) anywhere on the RAD has a sync pattern after being written.

3516 Searches the tracks (bands) on the RAD until one good track (band) is located. Error reports a good track (band) could not be found. Check error message.

3520 Order READ (X'02'), Flag IZC, byte count = 1 sector of data. Check error message.

TST1, 36 READ Test 2 - Ability to correctly receive and respond to READ (order X'02') less than a sector.

3610 A good track (band) could not be found.

3616 A good track (band) could not be located by the test. Check error message.

3620 Order READ (X'02'), Flag IZC, byte count = less than 1 sector of data. Check error message.

TST1, 37 READ Test 3 - Ability to correctly receive and respond to READ (order X'02') greater than a sector.

3710 A good track (band) could not be found.

3716 A good track (band) could not be located by the test. Check error message.

3720 Order READ (X'02'), Flag IZC, byte count = more than 1 sector of data. Check error message.

TST1, 38 WRITE-READ Test - Ability to WRITE and READ a pattern. Only preamble and the data transferred is tested. First, find a good track (band). If none exists, the test assumes the surface area is good but the logic is failing.

3810 A good track (band) could not be found.

3816 A good track (band) could not be located by the test. Check error message. (Either the logic generates or the logic checks the preamble is defective).

3820 The byte count was not reduced to zero by the test.

3825 Order READ (X'02'), Flag IZC, byte count = 1 sector of data. This test compares the data pattern received from a track of no preamble error against the increment pattern written there. If an error is detected, another track of no preamble error will be tried. After 10 tries, if the data received still in error, hardware failure is assumed. Check error message.

TST1, 39 Parity Test. Test the parity checking logic of the RAD.

3910 A good track could not be found.

3916 A good track could not be located by the test. Check error message.

3920 Verify that the pattern (X'55AA55AA', X'AA55AA55', X'55AA55AA', etc.) may be written/read without parity errors. Check error message. (Order READ (X'02'), Flag ICE, byte count = 1 sector of data).

3930 Verify that the pattern (X'AA55AAAA', X'AA55AA55', X'55AA55AA', etc.) may be written/read without parity errors. Check error message. (Order READ (X'02'), Flag ICE, byte count = 1 sector of data).

3940 Verify that the pattern (X'55AA5555', X'AA55AA55', X'55AA55AA', etc.) may be written/read without parity errors. Check error message. (Order READ (X'02'), Flag ICE, byte count = 1 sector of data).

3950 Verify that the pattern X'00000000', X'00000000', X'00000000', etc.) may be written/read without parity errors. Check error message. (Order READ (X'02'), Flag ICE, byte count = 1 sector of data).

3960 Verify that the pattern (X'FFFFFFFF', X'FFFFFFFF', X'FFFFFFFF', etc.) may be written/read without parity errors. Check error message. (Order READ (X'02'), Flag ICE, byte count = 1 sector of data).

TST1, 40 WRITE/READ (X'02') Test. READ an entire sector to verify that in writing less than a sector, the remaining sector is written with zeros.

4010 The RAD could not find a good track.

4016 A good track could not be located by the test. Check error message.

4020 Verify that the RAD has reduced byte count to zero. Check error message. (Order READ (X'02'), Flags ICE, byte count = 1 sector of data).

4025 Data written in shortened sector was not correct. Check error message.

4035 The zeros were not written in remaining sector area.

4040 Parity error was reported due to this operation.

TST1, 41 TRACK (BAND) SEARCH Test 1. Tests the ability of the RAD to WRITE and READ all tracks (bands) per sectors from the lowest to the highest available track (band).

4107 Error appeared during the execution of writing on all zero pattern on the RAD starting at the lowest available track (band). Check error message for type and location of failure.

TST1, 41 (Continued)

4108 Error appeared during the execution of reading an all zero pattern from the RAD starting at the lowest available track (band). Check error message for type and location of failure.

4109 Surface or addressing error, detected during the testing of the zero pattern read from the disc surface. See table printouts to determine types and locations of failures.

4110 Error appeared during the writing of a random pattern on the RAD starting at the lowest available track (band) to highest available track (band). Check error message.

4111 Error appeared during the reading of a random pattern from the RAD starting at the lowest available track (band) to highest available track (band). Check error message.

4112 Surface or address error was detected during the testing of the disc surface. Check error message.

TST1, 42 TRACK (BAND) SEARCH Test 2. Tests the ability of the RAD to WRITE and READ all tracks (bands) per sector from the highest to lowest available track (band).

4210 Error appeared during writing of a random pattern on the RAD starting at the highest available track (band) to lowest available track (band). Check error message.

4211 Error appeared during the reading of a random pattern on the RAD starting at the lowest available track (band) to the highest available track (band). Check error message.

4212 Surface or address error was detected during the testing of the disc surface. Check error message.

TST1, 43 READ (X'12') Test. Tests the ability of the RAD to receive and respond correctly to READs (Order X'12') of a sector.

4310 The RAD did not respond and receive correctly to READ of a sector.

4320 Verifies that RAD will report "incorrect length" to byte transfer of greater than a sector but less than 2 sectors. Check error message. (Order READ (X'12'), Flags IZC, byte count = greater than 1 sector of data).

TST1, 44 CHECKWRITE 1 Test. Find a good track, build a pattern, write this pattern on one sector of the RAD and then check this pattern with a CHECKWRITE. A comparison is expected.

4410 The RAD could not find a good track.
4416 A good track could not be located by the operations. Check error message.
4420 Verify that no errors are detected when a pattern of all zeros is compared to an identical pattern by means of a CHECKWRITE.
4430 Bit 0 of sense byte 4 (failing track) was a "1" should be "0". Test applies to H.S. RAD (7212) only.
4431 Bit 1 of sense byte 4 (failing track) was a "1" should be "0". Test applies to H.S. RAD (7212) only.
4432 Bit 2 of sense byte 4 (failing track) was a "1" should be "0". Test applies to H.S. RAD (7212) only.
4433 Bit 3 of sense byte 4 (failing track) was a "1" should be "0". Test applies to H.S. RAD (7212) only.
4434 Bit 4 of sense byte 4 (failing track) was a "1" should be "0". Test applies to H.S. RAD (7212) only.
4435 Bit 5 of sense byte 4 (failing track) was a "1" should be "0". Test applies to H.S. RAD (7212) only.
4436 Bit 6 of sense byte 4 (failing track) was a "1" should be "0". Test applies to H.S. RAD (7212) only.
4437 Bit 7 of sense byte 4 (failing track) was a "1" should be "0". Test applies to H.S. RAD (7212) only.
4440 Verify that no errors are detected when a pattern of all ones is compared to an identical pattern by means of a CHECKWRITE.
4450 Bit 0 of sense byte 4 (failing track) was a "1" should be "0". Test applies to H.S. RAD (7212) only.
4451 Bit 1 of sense byte 4 (failing track) was a "1" should be "0". Test applies to H.S. RAD (7212) only.
4452 Bit 2 of sense byte 4 (failing track) was a "1" should be "0". Test applies to H.S. RAD (7212) only.
4453 Bit 3 of sense byte 4 (failing track) was a "1" should be "0". Test applies to H.S. RAD (7212) only.
4454 Bit 4 of sense byte 4 (failing track) was a "1" should be "0". Test applies to H.S. RAD (7212) only.
4455 Bit 5 of sense byte 4 (failing track) was a "1" should be "0". Test applies to H.S. RAD (7212) only.
4456 Bit 6 of sense byte 4 (failing track) was a "1" should be "0". Test applies to H.S. RAD (7212) only.
4457 Bit 7 of sense byte 4 (failing track) was a "1" should be "0". Test applies to H.S. RAD (7212) only.

TST1,45 CHECKWRITE 2 Test. Find a good track, build a pattern, WRITE this pattern on one sector of the RAD and then alter this pattern so that 1 bit a pass will cause an error.

4510 The RAD could not find a good track.
4516 A good track could not be located by the operation. Check error message.
4520 Bit 0 from IOP was a "1" and from the RAD was a "0", but no transmission error was detected.
4521 Bit 1 from IOP was a "1" and from the RAD was a "0", but no transmission error was detected.
4522 Bit 2 from IOP was a "1" and from the RAD was a "0", but no transmission error was detected.
4523 Bit 3 from IOP was a "1" and from the RAD was a "0", but no transmission error was detected.
4524 Bit 4 from IOP was a "1" and from the RAD was a "0", but no transmission error was detected.
4525 Bit 5 from IOP was a "1" and from the RAD was a "0", but no transmission error was detected.
4526 Bit 6 from IOP was a "1" and from the RAD was a "0", but no transmission error was detected.
4527 Bit 7 from IOP was a "1" and from the RAD was a "0", but no transmission error was detected.
4530 Bit 0 of sense byte 4 (failing track) was a "0" should be a "1". Test applies to H.S. RAD (7212) only.
4531 Bit 1 of sense byte 4 (failing track) was a "0" should be a "1". Test applies to H.S. RAD (7212) only.
4532 Bit 2 of sense byte 4 (failing track) was a "0" should be a "1". Test applies to H.S. RAD (7212) only.
4533 Bit 3 of sense byte 4 (failing track) was a "0" should be a "1". Test applies to H.S. RAD (7212) only.
4534 Bit 4 of sense byte 4 (failing track) was a "0" should be a "1". Test applies to H.S. RAD (7212) only.
4535 Bit 5 of sense byte 4 (failing track) was a "0" should be a "1". Test applies to H.S. RAD (7212) only.
4536 Bit 6 of sense byte 4 (failing track) was a "0" should be a "1". Test applies to H.S. RAD (7212) only.
4537 Bit 7 of sense byte 4 (failing track) was a "0" should be a "1". Test applies to H.S. RAD (7212) only.
4540 Bit 0 from the IOP was a "0" and from the RAD was a "1", but no transmission error was detected.
4541 Bit 1 from the IOP was a "0" and from the RAD was a "1", but no transmission error was detected.
4542 Bit 2 from the IOP was a "0" and from the RAD was a "1", but no transmission error was detected.
4543 Bit 3 from the IOP was a "0" and from the RAD was a "1", but no transmission error was detected.
4544 Bit 4 from the IOP was a "0" and from the RAD was a "1", but no transmission error was detected.
4545 Bit 5 from the IOP was a "0" and from the RAD was a "1", but no transmission error was detected.
4546 Bit 6 from the IOP was a "0" and from the RAD was a "1", but no transmission error was detected.
4547 Bit 7 from the IOP was a "0" and from the RAD was a "1", but no transmission error was detected.
4550 Bit 0 of sense byte 4 (failing track) was a "0" but should be a "1". Test applies to H.S. RAD (7212) only.
4551 Bit 1 of sense byte 4 (failing track) was a "0" but should be a "1". Test applies to H.S. RAD (7212) only.
4552 Bit 2 of sense byte 4 (failing track) was a "0" but should be a "1". Test applies to H.S. RAD (7212) only.
4553 Bit 3 of sense byte 4 (failing track) was a "0" but should be a "1". Test applies to H.S. RAD (7212) only.
4554 Bit 4 of sense byte 4 (failing track) was a "0" but should be a "1". Test applies to H.S. RAD (7212) only.
4555 Bit 5 of sense byte 4 (failing track) was a "0" but should be a "1". Test applies to H.S. RAD (7212) only.
4556 Bit 6 of sense byte 4 (failing track) was a "0" but should be a "1". Test applies to H.S. RAD (7212) only.
4557 Bit 7 of sense byte 4 (failing track) was a "0" but should be a "1". Test applies to H.S. RAD (7212) only.

TST1,46 HALT WRITE Test. Verify that a HIO can stop a WRITE operation and cause the device to report the condition of the RAD just prior and after the HALT occurs.

HIO, CC2 = 0
- a. Condition Code error
- b. I/O address was recognized and RAD was not busy when HALT occurred but should have been.

4620 Incorrect status was returned from HALT operation. Check error message.

TST1, 47 HALT READ Test. Verify that a HIO can stop a READ operation and cause the device to report the condition of the RAD just prior and after the HALT occurs.

4710 HIO, CC2 = 0
- a. Condition Code error
- b. I/O address was recognized and RAD was not busy when HALT occurred but should have been.

4720 Incorrect status was returned from HALT operation. Check error message.

TST1, 48 Data Overrun. This test forces a Data Overrun to occur by executing many 1 or 4 byte data chained IOCD's. This test is not run on 725X (CD).

*False errors may be reported if an Extended Performance RAD with 4 byte option is connected to an SIOP*

4810 Data Overrun did not occur for a series of WRITE short data chained IOCD's.

4820 Data Overrun did not occur for a series of READ short data chained IOCD's.

TST1, 49 WRITE PROTECT Test. Verify that all tracks (bands) can report Write Protection, both from sense information and status return from a WRITE operation. Set the desired Write-protect switches to be tested. Test is limited by both the 'SYST' and 'SEEK' directives. This test is not run on 725X (CD).

4910 Reports that Write Protection switches were set and detected as part of the status returned after a WRITE operation. This is not an error if the Write-protect switches are set.

4920 Reports that Write-protect switches were set and detected as part of the sense word returned by a device SENSE operation. This is not an error if the Write-protect switches are set.

TST1, 50 CHECKWRITE Test. This subtest verifies that checkwrite of less than or greater than a sector functions correctly.

5010 The RAD could not find a good track.

5016 A good track could not be located by the operation, check error message for type of failure.

5020 Checkwrite error for the checking of byte counts not equal to a sector. Checkwrite expects the last part of a sector to contain zeros. If transmission error is reported this was not the case.

# Section 7

## SIGMA 5 - 9
## REMOVABLE DISK STORAGE TEST (724X)

PROGRAM NO. 705534

7

## Section 7

## CONTENTS

Page

Subject Model . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 7-1
Required Equipment . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 7-1
Program Prerequisites . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 7-1
General Operating Procedures . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 7-1
Directives . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 7-2
Start Procedure . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 7-3
Program Test Description . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 7-4
Order Codes . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 7-4
TDV Status . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 7-4
AIO Status . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 7-4
Test Mode Data Byte . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 7-5
Addressing Format . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 7-5
Functional Subtests and Related Error Messages . . . . . . . . . . . . . . . . . . 7-6

# 7. SIGMA 5–9 REMOVABLE DISK STORAGE TEST (724X)

**SUBJECT MODEL** -- Removable Disk Controller, Model number 7240, Removable Disk Storage Units, Model numbers 7242, 7246

**REQUIRED EQUIPMENT** -- Minimum Memory Size: 16K; Input Device: Card Reader, Paper Tape Reader or Magnetic Tape Unit; Output Device: Keyboard Printer or Line Printer

## PROGRAM PREREQUISITES

None

## GENERAL OPERATING PROCEDURES

General operating procedures of the Xerox Sigma 5 through 9 Diagnostic Program Monitor (DPM) apply to this program.

# 7. SIGMA 5–9 REMOVABLE DISK STORAGE TEST (724X)

**DIRECTIVES** - directives are entered after a "!" is typed out

| Name | Format | Parameter | | | |
|---|---|---|---|---|---|
| | | ID | Definition | Value Range | Standard Value (default) |
| Program Directives - Environmental Directives | | | | | |
| System Environment | SYST, D1, D2,<br>H3, H4, H5, H6<br>,H7 . . .,H17,H18 | D1<br>D2<br>H3<br>H4<br>H5<br>H6<br>:<br>H17<br>H18 | Controller model number<br>Revision number<br>Storage Unit Device Address (1st)<br>Available cylinders (1st)<br>Storage Unit Device Address (2nd)<br>Available cylinders (2nd)<br>Same as H3, H4 except for<br>8th Storage Unit | 7240<br>0<br>80 ~ 1FFF<br>00XY00ZW<br>80 ~ 1FFF<br>00XY00ZW<br>XY · 1st cylinder<br>ZW · last cylinder | |
| Program Directives - Testing Directives | | | | | |
| Comprehensive Test (all functional tests, 1 70, and random exerciser Test) | TST0, D1, D2 | D1<br>D2 | Number of ordered sequences executed by random exerciser<br>Number of retries | 0 ~ 99999999<br>0 ~ 99999999 | 5000 (D1 = 0)<br>0 |
| Functional Test | TST1 [, D1 [, D2]] | D1<br>D2 | The first subtest to be executed<br>Last subtest to be executed | 0 (all subtests) ~ 70<br>1 | 0<br>D1 |
| Random Exerciser Test | TST2, D1, D2 | D1<br>D2 | Number of cycles to be performed<br>Number of retries before next cycle | D1 ≥ 0<br>D2 ≥ 0 | |
| Utility Test | TST3, D1, D2, D3, H4 | | D1 - Utility Test selection<br>D2 - Function selection or serial number<br>D3 - Retry count; not used if D1 = 3<br>D1 = 1 Surface Test<br>D2 = 0 Write and then read all sectors<br>D2 = 1 Write all sectors<br>D2 = 2 Read all sectors<br>D2 = 3 Read all sectors (no data check)<br>D2 = 4 Checkwrite all sectors<br>D2 = 5 Write and then checkwrite all sectors<br>D1 = 2 Header Test<br>D2 = 0 Write and then read all headers<br>D2 = 1 Write all headers<br>D2 = 2 Read all headers<br>D2 = 3 Read all headers (no data check)<br>D1 = 3 Disk Initialization<br>D2 = Pack serial Number<br>D3 = 0 - Not used<br>H4 = Date = 00MMDDYY<br>D1 = 4 Flaw A Track<br>D2 = Alternate Cylinder Address<br>D3 = Alternate Head ADR | 200 ~ 202<br>0 - 19 | |
| Program Directives - Optional Directives | | | | | |
| Pattern selection (for Utility Test) | DATA, D1, H2, H3 | D1<br>H2<br>H3 | = 0, Fixed Pattern<br>= 1, Incremental Pattern<br>= 2, Random Pattern<br>= 3, Current Seek Address<br>Pattern seed (for D1 = 0, 1, 2)<br>Incrementing constant (for D = 1) | 0 ~ 3<br>00000000 ~<br>FFFFFFFF | |
| Usable surface area limitation | SEEK, D1, D2, D3, D4 | D1<br>D2<br>D3<br>D4 | Starting cylinder address<br>Starting head address<br>Starting sector address<br>Additional sectors to be used after starting address D1, D2, D3 | 0 ~ 202<br>0 ~ 19<br>0 ~ 5<br>(0 ~ 81) | |
| Limitation of Error printouts | LIMT, D1, D2 | D1<br>D2 | = 1 Limit Compare error printouts/sector to D2<br>Maximum number of printouts (No limit if D2 = 0) | 1<br>D2 ≥ 0 | |
| I/O buffer area definition | MEM [, H1, H2] | H1<br>H2 | First location of I/O buffer area<br>Last location of I/O buffer area | Obtainable by typing in MEM/ | Area between Diag. Prog. & DPM |
| I/O Reset | RSET | 0 | | | Not available |

Note: Parameter of any directive beginning with a D means decimal, with an H means hexadecimal

# 7. SIGMA 5–9 REMOVABLE DISK STORAGE TEST (724X)

## START PROCEDURE

1. Sense Switch Options, Monitor Directive Options, and Environmental Directives - Refer to DPM section of this manual.
2. Test Strategy Selection

| | Comprehensive Test | Functional Test | Random Exerciser Test | Utility Test |
|---|---|---|---|---|
| Recommended Application | Normal Usage | Solid Failure Detection and Specific Problem Analysis | Intermittent Failure Detection | Surface Test |
| Test Directive | TST0 | TST1 | TST2 | TST3 |
| Prerequisite | None | None | TST1 | TST1 |
| Optional Directives | SEEK, LIMT, MEM | SEEK, LIMT, MEM | SEEK, LIMT, MEM | SEEK, LIMT, MEM, DATA |
| Subtests | All functional subtests (1 ~ 70) and random exerciser test | 70 subtests (see error messages for the test types) | 1. Exerciser Initiation: Random data written on entire surface<br>2. Random Selection of:<br>a. Device<br>b. Order Sequences<br>c. Buffer Areas<br>d. Buffer Length<br>e. Data | WRITE only<br>READ only (Verify data)<br>READ only (No data verification)<br>READ header<br>CHECKWRITE<br>WRITE/READ TEST<br>WRITE header |
| Error Message Format | 1. ERROR NO. DDDD LOC XXXX<br>2. Self-explanatory | ERROR NO. DDDD LOC XXXX | Self-explanatory | Self-explanatory |

Procedure 2 of Restart Procedure of DPM should normally be used to clear a wait from a watchdog timer trap.

## PROGRAM TEST DESCRIPTION

Test descriptions of each functional test are included at the beginning of each subtest error number in the Functional Subtest and Related Error Message Section.

## ORDER CODES

| | |
|---|---|
| X'00' | STOP |
| X'01' | WRITE |
| X'02' | READ 2 (Report any transmission error at "count done") |
| X'03' | SEEK |
| X'04' | SENSE |
| X'05' | CHECKWRITE |
| X'12' | READ 1 (Terminate data transfer and report any transmission error at end of current sector if error is encountered) |
| X'13' | SELECT TEST MODE |
| X'80' | STOP AND INTERRUPT (at location X'5C') |
| X'09' | HEADER WRITE |
| X'0A' | HEADER READ |
| X'33' | RESTORE CARRIAGE |
| X'23' | RELEASE |

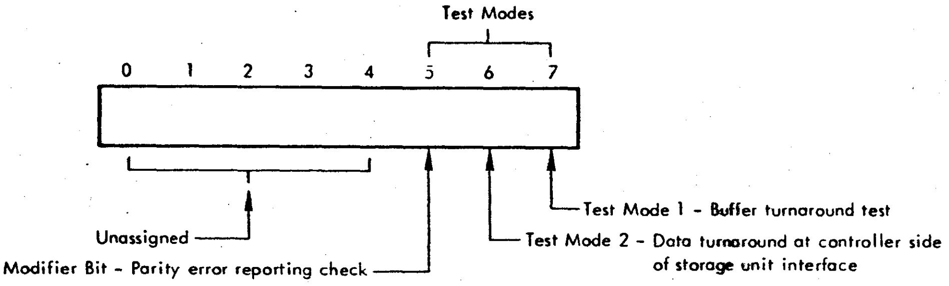
## TDV STATUS

| | BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| MODEL | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| REM DISK | Data Overrun | Flaw Mark | Sector Unavailable | Unassigned | Header Verification Error | Head On Cylinder | Seek Timeout Error | Header Parity Error |

## AIO STATUS

| | BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| MODEL | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| REM DISK | Data Overrun | ← | UNASSIGNED | → | Device Interrupt | Head On Cylinder | Seek Timeout Error | Unassigned |

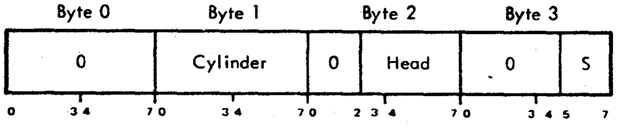
## TEST MODE DATA BYTE


Test Modes
0 1 2 3 4 5 6 7
Unassigned
Modifier Bit - Parity error reporting check
Test Mode 1 - Buffer turnaround test
Test Mode 2 - Data turnaround at controller side of storage unit interface

## ADDRESSING FORMAT

1. The format of the four byte sent to the Disk Pack by a SEEK order is:

Model 7240

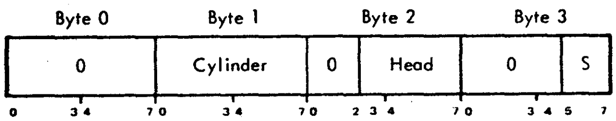

Byte 0
Byte 1
Byte 2
Byte 3
0
Cylinder
0
Head
0
S
0 3 4 7 0 3 4 7 0 2 3 4 7 0 3 4 5 7

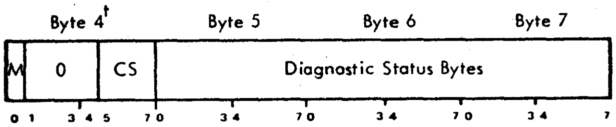
where S signifies sector number.

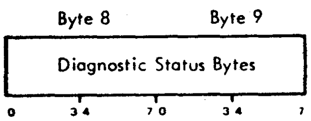
2. The format of the bytes received on a SENSE order is:

SENSE (X'04')

The Sense order causes the controller to transmit up to 10 bytes of information to the IOP, as follows:


Byte 0
Byte 1
Byte 2
Byte 3
0
Cylinder
0
Head
0
S
0 3 4 7 0 3 4 7 0 2 3 4 7 0 3 4 5 7


Byte 4†
Byte 5
Byte 6
Byte 7
M
0
CS
Diagnostic Status Bytes
0 1 3 4 5 7 0 3 4 7 0 3 4 7 0 3 4 7


Byte 8
Byte 9
Diagnostic Status Bytes
0 3 4 7 0 3 4 7

where

S signifies sector number

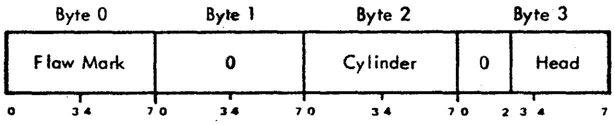
M signifies modifier bit

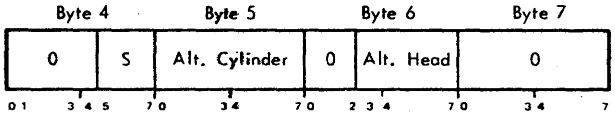
CS signifies current sector number

3. The format of the 8 bytes sent to the Disk Pack by a WRITE header order is:

HEADER WRITE (X'09')

The Header Write order causes the controller to consider all subsequent data bytes as header information. Each header requires the following bytes:


Byte 0
Byte 1
Byte 2
Byte 3
Flaw Mark
0
Cylinder
0
Head
0 3 4 7 0 3 4 7 0 3 4 7 0 2 3 4 7


Byte 4
Byte 5
Byte 6
Byte 7
0
S
Alt. Cylinder
0
Alt. Head
0
0 1 3 4 5 7 0 3 4 7 0 2 3 4 7 0 3 4 7

Sense Status Bytes 8 and 9

| Byte No. | Bit No. | Function |
|---|---|---|
| 8 | 0 | Data parity error |
| | 1 | Check-Write error |
| | 2 | Sector verification error |
| | 3 | Head verification error |
| | 4 | Cylinder verification error |
| | 5 | Sector address not zero at start of header write operation |
| | 6 | Difference select sent to device |
| | 7 | Sector select sent to device |
| 9 | 0 | Control select sent to device |
| | 1 | Head select sent to device |
| | 2 | Cylinder select sent to device |
| | 3 | Seek forward set |
| | 4 | Read gate sent to device |
| | 5 | Write and erase gate sent to device |
| | 6 | Read cylinder select sent to device |
| | 7 | Not used |
| Note: Bytes 8 and 9 are used by diagnostic programs. | | |

---

† Three bits of byte 4 indicate current sector number, but if the most significant bit (M) is a 1, the arm was in motion at time of sense and current sector number is meaningless. If the head number is nonexistent, (M) will also be a 1.

## FUNCTIONAL SUBTESTS AND RELATED ERROR MESSAGES

### FAULT INDEX DESCRIPTION – FUNCTIONAL SUBTESTS

The fault index contains a brief description of each functional subtest and a list of associated error numbers with a brief description of each error. The subtests and error numbers are arranged in ascending sequence. The description of subtest NN is numbered NN00. The first two digits of the error number correspond to the associated subtest; the last two numbers correspond to the individual errors within the subtest.

System error numbers
8500 Controller did not return to Ready condition after Test Mode order.
8501 Controller not in Test Mode after Test Mode order. TDV CC = 0.
8502 Controller in Test Mode after resetting Test Mode. TDV CC = 4.
8510 Controller did not return to Ready condition after Restore order.
8511 Device not on cylinder after a Restore order.

TST1, 01 AIO, HIO, TIO, TDV instruction recognition.

0110 AIO Condition Code error. No interrupt recognition expected.
0111 HIO Condition Code or Status error. See print-out.
0112 TIO Condition Code or Status error. See print-out. Preceding HIO did not reset Status.
0113 TDV Condition Code error. See print-out.

TST1, 02 SIO Invalid Order Test

0210 SIO for Invalid order not accepted. See print-out.
0211 Controller not ready after Invalid order (00 or F8). Order output and order input phases must be executed.
0212 Status error after Invalid order. UE expected.
0213 Byte count was changed during execution of Invalid order. Data phase not required.

TST1, 03 Test Mode Selection Test. A TDV instruction is used to verify setting and resetting of Test Mode.

0301 Test Mode byte = X'FF'.
0302 Test Mode byte = X'01'.
0303 Test Mode byte = X'02'.
0310 TDV CC2 reset. Device controller not in Test Mode.
0311 Output buffer changed during Test Mode order (Select). Data in phase not expected.
0312 TDV CC2 set. Device controller remains in Test Mode. CC2 = 0 expected.
0313 Output buffer contains ones after Test Mode order (Reset).
0315 TIO CC1 or CC2 set. Controller not ready after Test Mode order.
0316 TDV, TIO Status error or byte count error. See preceding print-out. Operation: Order out (X'13'), data out (1 byte), order in.
0321, 0322, 0323 TST1, 3 Data byte of FF, 01, and 02 was used during data output phase. See preceding print-out.

TST1, 04 Interrupt generation and HIO, AIO Instruction Test. The following orders will be issued: X'00', X'13' (data byte = 01), X'1' (data byte = 00) in order to set Interrupt Pending due to IUE, ICE and IZC respectively. Each order will be repeated once to allow resetting of IP with an HIO and an AIO instruction.

0410 TIO Status error during TST1, 4 after SIO. IP must be set and controller and device must be ready. IUE, ICE, and IZC flags are used.
0411 HIO did not reset IP. No reset generated.
0412 AIO Status error during TST1, 4. Preceeding SIO resulted in IP.
0413 AIO did not reset IP. No reset generated.
0421, 0422, 0423 TST1, 4 IOP flags for IUE, ICE, and IZC used respectively. See print-out.

TST1, 05 IO Interrupt Test. A Test Mode order with ICE flag will be issued and tests will be performed to verify that the program is only interrupted if the IO Interrupt is armed and enabled.

0510 TIO Status error during TST1, 5 after SIO. IP must be set. IO Interrupt is disarmed/disabled. Program should not be interrupted.
0511 Program was interrupted while IO Interrupt was disarmed/disabled.
0512 Program was interrupted while IO Interrupt was armed/disabled.
0513 Program was not interrupted while IO Interrupt was armed/enabled.

TST1, 06 Command Chaining Test. Two Test Mode orders will be Command Chained. Command Chaining will be tested. Invalid order Command Chained to a Test Mode order should not result in Command Chaining.

0610 TIO Status error during TST1, 6 after Command Chaining or Command Chaining not performed. See preceding printout.
0611 TIO Status error during TST1, 6. Status error or Command Chaining not inhibited by UE from Invalid order.

TST1, 07 FAM Write/Read Byte Count Test. Write and Read orders with byte counts varying sequentially from 1 to 16 are issued in Test Mode 1. Zero byte count expected.

0710 Controller not ready after Write order in TM1.
0711 Controller not ready after Read order in TM1.
0712 Byte count not equal to zero after Write order in TM1.
0713 Byte count not equal to zero after Read order in TM1.

TST1, 08 FAM Write/Read Data Test. Write Command-Chain Read orders will be issued with varying data pattern. The Read data will be compared to the Write data. During the 2nd part of the test 4 Write/CC/Read orders with counts of 13 will be issued to test the byte alignment logic.

0810 Controller not ready after Write/CC/Read order in TM1.
0811 Compare errors during TST1, 8. Output buffer: IOBF1, Input buffer: IOBUF.
0812 Controller not ready after Write/CC/Read (BC = 13) Test Mode 1.
0813–0816 Read Data compare error following Write/CC/Read (BC = 13)
If last digit is 3, data started on word boundary
If last digit is 4, data started at byte 1
If last digit is 5, data started at byte 2
If last digit is 6, data started at byte 3

TST1, 09 Test Mode 2 – Seek Order Byte Count Test. Seek orders with byte counts of 3, 4, 5 are issued to the controller and the status response is tested.

0910 Controller not ready after Seek order in Test Mode 2.
0911 Status error after Seek order in Test Mode 2. Expected: IL, UE, zero byte count, on-cylinder. See printout.
0912 Status error after Seek order in Test Mode 2. Expected: Not IL, zero byte count, on cylinder. See printout.
0913 Status error after Seek order in Test Mode 2. Expected: IL, byte count = 1, on-cylinder. See printout.
0914 Output buffer (:IOBF1) altered during Seek in TM2.

TST1, 10 Test Mode 2 – Seek Order Interrupt Address Test. Seek orders will be to device 0 through 7 in sequence and the address returned with the AIO Status will be verified. Change above mask from X'04000000' to X'0C000000' if Device Interrupt Engineering Order is available.

1010 Status error after Seek order with Interrupt Modifier bit. Expected: IP, zero byte count, on cylinder. See printout.
1011 AIO Status error after Seek order with Interrupt Modifier bit. IP set prior to AIO. Expected: Address verification. See printout.
1012 Preceding AIO did not clear Seek complete interrupt (TIO/IP = 0).

TST1, 13 Test Mode 2 – Sense Order Byte Count Test. Sense orders with byte counts of 1 through 11 are issued to the controller and the Status Response is tested.

1310 Controller not ready after Sense order in Test Mode 2.

TST1, 13 (Continued)

1311 Status error after Sense order in Test Mode 2. No unusual status expected. See print-out.
1312 Byte count not equal to zero after a Sense order with a byte count ≤ 10. See print-out.
1314 First 8 bytes of input buffer (IOBF1) not changed during Sense order. Data input expected.

TST1, 15 Test Mode 2 - Seek Tag Line Test. See/Command Chain/ Sense orders are executed and the Tag Line information in byte 8 of the Sense data is verified.

1510 Controller not ready after Seek/CC/Sense order in Test Mode 2.
1511 Status error after Sense order or Command Chaining not performed. See print-out
1512 Seek Tag Line error or Sense order not functioning properly. Sense buffer: IOBF1. See print-out.

TST1, 16 Test Mode 2 - Head and Sector Address Test. Seek/CC/ Sense orders are issued sequentially varying the Device Address from 0 - 7. Sense data is verified. Sense orders are issued sequentially to all devices to insure that the addresses are not changed. The same sequence is repeated with the Device Address varied from 7 - 0. The complement of the data pattern in pass 1 is used in Pass 2. A unique pattern is used for each device.

1610 Controller not ready after Seek/CC/Sense order in Test Mode 2.
1611 Controller not ready after Sense order in Test Mode 2.
1620-1627 Head and Sector Address obtained during Sense not equal to original data. Last digit of error number indicates Device Address used. Address sequence 0 - 7. Order sequence: Seek/ CC/Sense.
1630-1637 Head and Sector Address obtained during Sense not equal to original data. Check addressing of Head and Sector FAM. Last digit of error number indicates Device Address used.
1640-1647 Same as 1620-1627. Address sequence 7 - 0.
1650-1657 Same as 1630-1637.

TST1, 17 Test Mode 2 - Head and Sector Address Validy Test. Seek and Sense are issued 203 times varying the Sector Address from 0–7 and the Head Address from 0–25. Sector unavailable will be tested for Sector Address > 5 and Head Address > 19. The combined Sector and Head Address which is returned as Cylinder Address during Seek will be verified.

1710 Controller not ready after Seek order in Test Mode 2.
1711 Status error after Seek order in Test Mode 2 with illegal sector Address (7). UE, sector unavailable, on cylinder expected.
1712 See 1711. Illegal Head Address was issued during Seek.
1713 Status error after Seek order in Test Mode 2. Legal Head and Sector Address were used. See print-out.
1714 Controller not ready after Sense order in Test Mode 2.
1715 Seek/Sense compare error. The Head/Sector Address was not returned correctly as the Cylinder Address. See print-out.

TST1, 19 Test Mode 2 - Cylinder Difference Logic Test. Seek and Sense orders are issued systematically varying the Cylinder and Head/Sector Address. 5 passes will be performed:

1. Cyl and Hd/Sect = 0 - 202.
2. Cyl = 0 - 202, Hd/Sect = 0
3. Cyl = 0, Hd/Sect = 0 - 202
4. Cyl = 202 - 0, Hd/Sect = 0
5. Cyl = 0, Hd/Sect = 202 - 0

1910 Controller not ready after Seek order in Test Mode 2.
1911 Controller not ready after Sense order (Byte count = 10) in Test Mode 2.
1912 The difference between Head/Sector and the Cylinder Address returned in byte 7 of the Sense order is not correct. See print-out.
1913 Controller not ready after the 2nd Seek order in Test Mode 2. Two Seek orders are required to obtain the correct difference in byte 7 of the Sense data.

TST1, 20 Test Mode 2 - Illegal Cylinder Address Test. Seek orders are issued with illegal Cylinder Address (203 - 255) and the Status Response is verified.

2010 Controller not ready after Sense order in Test Mode 2.
2011 Status error after Seek order in Test Mode 2 with Illegal Cylinder Address (203 - 255). UE, sector unavailable, on cylinder expected.

TST1, 23 Test Mode 2 - Restore Order Test. A Seek/CC/Restore and Sense order sequence is sequentially issued to all devices (0 - 7). The test verifies the status after the Restore orders and verifies with a Sense order (Byte count = 10) that the Head and Sector Address in the FAM are cleared to zero and that the Restore order generated the correct Tag Lines.

2310 Controller not ready after Seek/CC/Restore orders in Test Mode 2.
2311 Status error after Restore order in Test Mode 2. Not UE, byte count = 1 (no changes). See print-out.
2312 Controller not ready after Sense order in Test Mode 2.
2313 Bytes 2 (Head) and 3 (Sector) of Sense data not 0. Preceding Restore order did not clear controller registers (FAM).
2314 Restore Tag Line error. Sense buffer: IOBF1. See print-out.

TST1, 24 Test Mode 2 - Release Order Test. A Release order and a Sense order is issued. The test verifies the status after the Release and verifies with a Sense order (Byte count = 10) that the Release order generated the correct Tag Lines.

2410 Controller not ready after Release order in Test Mode 2.
2411 Status error after Release order in Test Mode 2. Not UE, byte count = 1 (No change) expected. See print-out.
2412 Controller not ready after Sense order in Test Mode 2.
2413 Release Tag Line error. Sense buffer: IOBF1. See print-out.

TST1, 25 Test Mode 2 - Read Order Tag Line and Data Test. Read orders X'02' and X'12' are issued in sequence. The status and byte count are verified. The Read data is compared to the expected information. A Sense order verifies that the Tag Lines are correctly generated for a Read order.

2510 Controller not ready after Read order (02) in Test Mode 2.
2511 See 2510. Read order (12).
2512 Status error after Read order in Test Mode 2. Not UE, not IL, not TE, byte count = 0 expected. See print-out.
2513 See 2512. Read order (12).
2514 Data compare error in Test Mode 2; Read order (02). See print-out.
2515 See 2514. Read order (12).
2516 Controller not ready after Sense order in Test Mode 2.
2517 Read (02) Tag Line error. Sense buffer: IOBF1. See print-out.
2518 See 2517. Read order (12).
2519 Status error in diagnostic Sense byte (byte 8 of Sense data) defines Read error.
2520 See 2519. Read order (12).

TST1, 26 Test Mode 2 - Read Order Incorrect Length Test. Read orders are issued with byte count sequentially varied from 1008 to 1025 (not 1024). The status will be verified. For byte counts < 1024 the test verifies that the controller terminates data-in at the correct byte count.

2610 Controller not ready after Read order (02) in Test Mode 2.
2611 Remaining byte count after Read order with incorrect length not zero. See print-out.
2612 Status error after Read order in Test Mode 2. IL expected. See print-out.
2613 Data compare error in Test Mode 2; Read order (02). For byte count < 1024 the remaining bytes in input buffer must be zero.

TST1, 27 Test Mode 2 - Read Order/Head and Sector Incrementation Test. Seek/CC/Read and Sense order sequences are issued with a Read byte count of 1024. Sector and Head Address incrementation is verified.

TST1, 27 (Continued)

2710 Controller not ready after Seek/CC/Read (02) orders in Test Mode 2.
2711 Status error after Seek/CC/Read in Test Mode. No abnormal status expected. See print-out.
2712 Controller not ready after Sense order in Test Mode 2.
2713 Address received during Sense not expected. Head or Sector Address may not increment properly. See print-out.

TST1, 28 Test Mode 2 - Read Order Cylinder Boundary Test. A Read order with a byte count of 1025 is issued starting at Head 19, Sector 5. Read operation will terminate after 1 sector and sector unavailable will be reported.

2810 Controller not ready after Seek/CC/Read (02) orders in Test Mode 2.
2811 Status error after Read order (Seek Address = Head 19. Sector 5, byte count = 1025). UE, sector unavailable, byte count = 1 expected: See print-out.

TST1, 29 Test Mode 2 - Header Read Order Test. Seek/CC/Header Read orders sequences are issued with Header Read byte count of 8. The status and byte count are verified. The Header Read data is compared to the expected information. A Sense order verifies that the Tag Lines are correctly generated and that the Head and Sector Address are incremented correctly.

2910 Controller not ready after Seek/CC/Header-Read orders in Test Mode 2.
2911 Status error after Header Read order. No abnormal status expected. See print-out.
2912 Header data compare error in Test Mode 2. See print-out.
2913 Controller not ready after Sense order in Test Mode 2. See print-out.
2914 Header Read Tag Line error. Sense buffer: IOBUF. See print-out.
2915 Status error in diagnostic Sense byte (Byte 8 of Sense data) defines Header Read error.
2916 Address received during Sense not expected. Head or Sector Address may not increment properly. See print-out.

TST1, 30 Test Mode 2 - 120 Sector Header Read Test. A Seek/CC/Header Read order with a Header Read byte count of 960 is issued. The Header data is verified. No data error indicates that the Head and Sector Incrementation Logic performs correctly.

3010 Controller not ready after Header Read order in Test Mode 2.
3011 Byte count not zero after Header Read order (960 bytes).
3012 Status error after Header Read order. No abnormal status expected.
3013 Header data compare error in Test Mode 2. See print-out.

TST1, 31 Test Mode 2 - Header Read Byte Count Test. Header Read orders with byte counts of 7 and 9 are issued to the controller and the Status Response is tested.

3110 Controller not ready after Header Read order in Test Mode 2.
3111 Status error after Header Read order (byte count 7). Expected: IL, no UE, byte count = 0. See print-out.
3112 See 3111. Header Read order byte count = 9.

TST1, 32 Test Mode 2 - Header Read Order Cylinder Boundary Test. A Header Read order with a byte count of 9 is issued starting at Head 19 Sector 5. Read operation will terminate after one sector and sector unavailable will be reported.

3210 Controller not ready after Header Read order in Test Mode 2.
3211 Status error after Header Read order (Seek address = Head 19, Sector 5, byte count = 9). UE, sector unavailable, byte count = 1 expected.

TST1, 35 Test Mode 2 - Header Write Order Test. Seek/CC/Header Write order sequences are issued with Header Write byte counts of 48. The Header data consists of a X'A5A5A5A5' pattern. The status and byte count are verified. A Sense order verifies that the Tag Lines are correctly generated and that the Head and Sector Address increment correctly.

3510 Controller not ready after Seek/CC/Header-Write orders in Test Mode 2.
3511 Status error after Header Write order. No abnormal status expected. See print-out.
3512 Controller not ready after Sense order in Test Mode 2.
3513 Header Write Tag Line error. Sense buffer: IOBF1. See print-out.
3514 Status error in diagnostic Sense byte (byte 8 of Sense data) defines Header Write error.
3515 Address received during Sense not expected. Head or Sector Address may not increment properly. See print-out.

TST1, 36 Test Mode 2 - 120 Sector Header Write Test. A Seek/CC/Header Write order sequence with a Header Write byte count of 960 is issued. A Sense order is issued to verify that the Head and Sector Address are incremented to Head 20 Sector 0.

3610 Controller not ready after Seek/CC/Header-Write orders in Test Mode 2.
3611 Byte count not zero after Header Write order (960 bytes).
3612 Status error after Header Write order. No abnormal status expected.
3613 Controller not ready after Sense order in Test Mode 2.
3614 Address received during Sense not expected. Header or Sector Address have not been incremented past Head 19 Sector 5.

TST1, 37 Test Mode 2 - Header Write Byte Count Test. Header Write orders with byte counts of 7 and 9 are issued to the controller and the Status Response is tested.

3710 Controller not ready after Seek/CC/Header-Write order in Test Mode 2.
3711 Status error after Header Write order (byte count 4). Expected: IL, no UE, byte count = 0. See print-out.
3712 See 3711. Header Write order byte count = 9.

TST1, 38 Test Mode 2 - Header Write Order Cylinder Boundary Test. A Header Write order with a byte count of 49 is issued starting at Head 19 Sector 0. Write operation will terminate after 6 sectors and sector unavailable will be reported.

3810 Controller not ready after Header Write order in Test Mode 2.
3811 Status error after Header Write order (Seek Address = Head 19, Sector 0, byte count = 49). UE, sector unavailable, byte count = 0 expected.

TST1, 39 Test Mode 2 - Header Write Starting Address Test. Header Write orders with Starting Sector Address of 0 through 5 are sequentially issued. For all Starting Addresses except 0, byte 8 of the Sense data will indicate Header Address error.

3910 Controller not ready after Header Write order in Test Mode 2.
3911 Status error after Header Write order. No abnormal status expected.
3912 Controller not ready after Sense order in Test Mode 2.
3920-3925 Status error in diagnostic Sense byte (byte 8 of Sense data). The least significant digit of error number reflects the Starting Sector Address of the Header-Write operation. Header-Address error is expected for all Starting Address except Sector 0.

TST1, 40 Test Mode 2 - Write Order Test. Seek/CC/Write order sequences are issued with Write byte count 3 or 1024. The Write data consists of byte values starting at 224, with each successive byte = byte (N) + 1. These values reflect the byte counter in the controller at the time of writing each byte. Status and byte count are verified. A Sense order verifies that the Tag Lines are correctly generated and that the Head and Sector Address increment correctly.

4010 Controller not ready after Seek/CC/Write orders in Test Mode 2.
4011 Status error after Write order. No abnormal status expected.
4012 Controller not ready after Sense order in Test Mode 2.
4013 Write Tag Line error. Sense buffer: IOBF1. See print-out.
4014 Status error in diagnostic Sense byte (byte 8 of Sense data) defines Write error.
4015 Address received during Sense not expected. Head and Sector Address may not increment properly. See print-out.

TST1, 41 Test Mode 2 - Write Order Incorrect Length Test. Seek/CC/Write order sequences are issued with byte counts sequentially varied from 1008 to 1025 (not 1024). The status will be verified.

4110 Controller not ready after Write order in Test Mode 2.
4111 Remaining byte count after Write order with Incorrect Length not zero. See print-out.
4112 Status error after Write order in Test Mode 2. IL expected. See print-out.

TST1, 42 Test Mode 2 - Write Order Cylinder Boundary Test. A Write order with a byte count of 1025 is issued starting at Head 19 Sector 5. The Write operation will terminate after 1 sector and sector unavailable will be reported.

4210 Controller not ready after Write order in Test Mode 2.
4211 Status error after Write order (Seek Address = Head 19, Sector 5 byte count 1025). UE, sector unavailable, byte count = 0 expected.

TST1, 45 Test Mode 2 - Check-Write Order Test. Seek/CC/Check-Write order sequences are issued with byte counts of 1024. The Check Write data consists of byte values starting at 224, with each successive byte = byte (N) +1. A Sense order verifies that the Tag Lines are correctly generated and that the Head and Sector Address increments correctly.

4510 Controller not ready after Seek/CC/Check-Write orders in Test Mode 2.
4511 Status error after Check-Write order. No abnormal status expected. See print-outs.
4512 Controller not ready after Sense order in Test Mode 2.
4513 Check-Write Tag Line error. Sense buffer: IOBF1. See print-out.
4514 Status error in diagnostic Sense byte (byte 8 of Sense data) defines Check-Write error.
4515 Address received during Sense not correct. Head or Sector Address may not increment properly. See print-out.

TST1, 46 Test Mode 2 - Check-Write Order Incorrect Length Test. Seek/CC/Check-Write order sequences are issued with byte counts sequentially varied from 1008 to 1025 (not 1024). The status will be verified.

4610 Controller not ready after Seek/CC/Check-Write order in Test Mode 2.
4611 Remaining byte count after Check-Write order with Incorrect Length not zero. See print-out.
4612 Status error after Check-Write order in Test Mode 2. IL expected. See print-out.

TST1, 47 Test Mode 2 - Check-Write Order Cylinder Boundary Test. A Check-Write order with a byte count of 1025 is issued starting at Head 19 Sector 5. The Check-Write operation will terminate after one sector and sector unavailable will be reported.

4710 Controller not ready after Check-Write order in Test Mode 2.
4711 Status error after Check-Write order (Seek address = Head 19, Sector 5, byte count 1025). UE, sector unavailable, byte count = 0 expected.

TST1, 48 Test Mode 2 - Check-Write Transmission Error Test. Seek/CC/Check-Write order sequences with byte counts of 2048 are issued. The Check-Write data consists of byte values starting at 224 (X'E0'), with each successive byte = byte (N) + 1. During the first 8 passes one bit in byte 32 (X'FF') is sequentially dropped starting with bit 0 ending with bit 7. During the 2nd 8 passes one bit in byte 33 (X'00') is sequentially picked-up starting with bit 0, ending with bit 7. The test verifies that a single bit failure in a sector is detected and reported as TE and that the operation terminates after the first sector. The remaining byte count must be ≥ 1000.

4810 Controller not ready after Seek/CC/Check-Write order in Test Mode 2.
4811 Remaining byte count after Check-Write order (2048 bytes) less than 1008. Check-Write operation did not terminate after one sector.
4812 Controller not ready after Sense order in Test Mode 2.
4813 Address received during Sense not correct. Head or Sector Address may have been incremented by two sectors.
4814 Status error in diagnostic Sense byte (byte 8 of Sense data) should indicate Check-Write error.
4820-4827 Status error after Check-Write order. TE and not IL or UE expected. The least significant digit of the error number indicates which bit of byte 32 of the Check-Write data was dropped to induce a Check-Write error.
4830-4837 See 4820-4827. The least significant digit of the error number indicates which bit of byte 33 of the Check-Write data was added to induce a Check-Write error.

TST1, 49 Test Mode 2 - Halt On Transmission Error Test. Seek/CC/Write order sequences with byte counts of 1020 are issued to test setting of UE, IL and IOP/Halt. Seek/CC/Check-Write order is issued to check setting of TE.

4910 Controller not ready after Seek/CC/Write (or Check-Write) in Test Mode 2.
4911 Status error after Write order in Test Mode 2. UE, IL and IOP/Halt setting expected.
4912 Status error after Write order in Test Mode 2. IL and not UE and not IOP/Halt setting expected.
4913 Status error after Check-Write order in Test Mode 2. UE, TE and IOP/Halt setting expected.

TST1, 50 Test Mode 3 (Parity) - Read Order 12 Parity Test. A Sense/CC/Read 12 order sequence is issued with a Read byte count of 2048. The controller will generate a parity error. The test verifies the status (TE and not UE) and verifies with a Sense order that the Read order terminated after a sector. The remaining byte count must be = 1024.

5010 Controller not ready after Seek/CC/Read 12 order in Parity Test Mode.
5011 Remaining byte count after Read 12 order (2048 bytes) not equal to 1024. Read 12 operation did not terminate after one sector.
5012 Status error after Read 12 order. TE and not IL or UE expected. See Print-out.
5013 Controller not ready after Sense order in Parity Test Mode.
5014 Status error in diagnostic Sense byte (byte 8 of Sense data) should indicate data parity error.
5015 Address received during Sense not correct. Head or Sector Address may have been incremented by 2 sectors.

TST1, 51 Test Mode 3 (Parity) - Read Order 02 Parity Test. A Sense/CC/Read 02 order sequence is issued with a Read byte count of 3072 (3 data-chain operation). The test verifies that Reading continues until the byte count = zero. The expected status is TE, not UE.

| | |
|---|---|
| 5110 | Controller not ready after Seek/CC/Read02/DC/Read02/DC/Read02 in Parity Test Mode. |
| 5111 | Status error after Read02 order. TE and not IL or UE and byte zero and Current Command Address = Starting Address + 3 expected. |
| 5112 | Controller not ready after Sense order in Parity Test Mode. |
| 5113 | Address received during Sense not correct. Head or Sector Address did not increment correctly. |

TST1, 52 Normal Mode - Restore Order Test. A Restore order is issued to the storage unit. The test verifies that the controller and device are ready and that positioning is complete and that no time out error has occurred.

| | |
|---|---|
| 5210 | Controlled not ready after Restore order. |
| 5211 | On cylinder bit TDV(5) not received after Restore order. |
| 5212 | Status error after Device order. See print-out. |

TST1, 53 Normal Mode - Seek Order Test. A Restore order is issued to the storage unit. The test proceeds to issue Seek orders for all sectors on cylinder 0. No head motion is involved except possibly during the Restore order. The test verifies that Seek orders can be completed without errors.

| | |
|---|---|
| 5310 | Controller not ready after Seek order. |
| 5311 | On-cylinder bit TDV(5) not received after Seek order. No head motion required. |
| 5312 | Status error after Seek order. See print-out. |

TST1, 54 Normal Mode - Release Order Test. A Release order is issued. The test verifies the status after the release.

| | |
|---|---|
| 5410 | Controller not ready after Restore order in normal mode. |
| 5411 | Status error after Restore order in normal mode. Not UE, byte count = 1 (no change) expected. See print-out. |

TST1, 55 Header Read - Failure Isolation Test. A Restore order is issued to position the heads at cylinder 0. Seek/CC/Header-Read sequences will be issued for all 120 sectors of cylinder 0. No errors will be reported until all operations are completed. A summary of all errors will be printed. The test will proceed to loop on the first failure with immediate error print-outs. Information other than zeros in the flaw byte or alternate Address byte will not be considered an error.

| | |
|---|---|
| 5510 | Controller not ready after Seek/CC/Header Read order. |
| 5511 | Status error after Header-Read order. See print-out. |
| 5512 | Compare error of Header data. Bytes 0, 5 and 6 of each Header are not tested. |

TST1, 56 Normal Mode - Sense Order/Angular Position. A Restore order is issued to the storage unit. The test issues a Sense order and verifies the status. The test proceeds to issue up to 6 Sense orders in order to verify angular position 0. Following position 0, 5 Sense orders are issued to verify angular position 1-5.

| | |
|---|---|
| 5610 | Controller not ready after Sense order. |
| 5611 | Status error after Sense order. See print-out. |
| 5612 | Controller not ready after Sense order. |
| 5613 | 6 attempts failed to find angular position of 0 in byte 4 of Sense data. |
| 5621-5625 | Controller not ready after Sense order. The least significant digit of the error number indicates the current angular position expected in the Sense data. |
| 5631-5635 | The expected angular position as indicated by the least significant digit of the error number not in byte 4 of Sense data. |

TST1, 57 Normal Mode - Sense Order Test. A Restore order is issued to position the heads at cylinder 0. Seek/CC/Sense sequences will be issued for all 120 sectors of cylinder 0. The test verifies that the Address returned during the Sense operation is correct and that normal status is returned.

| | |
|---|---|
| 5710 | Controller not ready after Sense order. |
| 5711 | Status error after Sense order. See print-out. |
| 5712 | Compare error of Seek and Sense data. See print-out. |
| 5713 | Status error in diagnostic Sense byte (byte 8 of Sense data) should indicate no errors. |

TST1, 58 Sequential Head Positioning Test. Sequential Seek orders are issued to the disk storage unit. After verifying successful completion of each Seek order, a Sense order is issued to verify the Seek operation. If a Header parity error is detected during the Sense order, the Sense operation will be automatically retried six additional times before an error is reported. If the cylinder Address obtained is correct, the next Seek/Sense sequence will be initiated. On retries after a cylinder compare error, the Seek Address will be decremented by 1 (not < 0) and a Restore order will be issued prior to retry.

| | |
|---|---|
| 5810 | Controller not ready after a Seek order. |
| 5811 | Controller not ready after Sense order. Arm was in motion execution of Sense order. |
| 5812 | Arm in motion bit in byte 4 of Sense data not received. |
| 5813 | On cylinder bit TDV(5) not received after Seek order. The Seek order intiated head motion. |
| 5814 | Controller not ready after Sense order. Arm motion was previously completed. TDV(5) = 1. |
| 5815 | All six Sense orders issued to the drive unit indicate that a Header parity error was detected. |
| 5816 | Compare error of Seek and Sense data. See print-out. |

TST1, 60 Complex Head Positioning, Seek Access Timing and Seek Complete Interrupt Test. This test consists of four passes. The passes differ by the type of head motion.

1. Seek (M) Sense Seek (N) Sense 203 times. M varies from 0 to 202, N is always = 0.
2. Seek (M) Sense Seek (N) Sense 203 times. M is always 202. N varies from 202 to 0.
3. Seek (M) Sense Seek (N) Sense 203 times. M varies from 0 to 202, N varies from 202 to 0.
4. Seek (R) Sense Seek (R) Sense 203 times. R is a random number.

During retries the last successful Seek/Sense sequence is repeated. Average Seek access time is computed and if it exceeds the limit, it is printed out. The test is initialized if retry is requested.

| | |
|---|---|
| 6010 | Controller not ready after Seek order. |
| 6011 | Expected Seek complete interrupt was not received. |
| 6012 | Status error after Seek complete interrupt has been received. See print-out. |
| 6013 | Controller not ready after Sense order. |
| 6014 | Header parity error indicated by bit 7 of TDV following Sense orders. The Sense order has been issued 7 times to automatically recover from the problem. Possible bad Headers on the disk. |
| 6015 | Head positioning error. See preceding print-out. The expected Sense data defines the Seek Address. The observed Sense data defines the Current Address in the controller. Prior to the Seek operation. |
| 6016 | Average Head positioning time greater than 95 msec. All Seek operations in this test are used in the computation of the average time. |

TST1, 63 Comprehensive Write/Read/Checkwrite Test. During the first phase of this test, attempts are made to locate a cylinder with error-free Headers. The cylinders used are determined by the SYST-directive entry for each device. Once a good cylinder has been located, a Write/Read/Checkwrite pass will be performed 3 times, each time with a different pattern.

Pass 1: Fixed pattern of X'AA55AA55'

Pass 2: Incremented pattern of X'00010203', X'04050607', X'08090A0B'

TST1, 63 (Continued)

Pass 3: Current Seek Address X'00000000' for cyl = 0, HD=0, Sect 0, X'00NN0803' for cyl NN,HD=08,Sect=3.

Any recoverable error (6 retries are automatically attempted) or solid failure will cause the selection of another cylinder. The objective of this procedure is to avoid looping on an error which may be caused by surface flaws.

| | |
|---|---|
| 6310 | Attempts to find a cylinder (120 sectors) with good Headers and no assigned Alternate Addresses not successful. Program used only those cylinders which were made available to the program with the SYST directive. |
| 6311 | Controller not ready after Header Read order of 120 sectors. |
| 6312 | Byte count after Header Read order not reduced to zero. |
| 6313 | Status error after Header Read order. No unusual status expected. |
| 6314 | Header data compare error. See print-out. If a flaw byte or an Alternate Address is found in the Header, the current cylinder will not be used for the Write/Read/Checkwrite portion of this test. |
| 6315 | Header Read operation not successful for current cylinder. Errors 6311 through 6314 describe the nature of the failure. Next cylinder will be automatically selected. |
| 6320 | Controller not ready after Seek order. |
| 6321 | Controller not ready after Sense order. |
| 6322 | Seek/Sense compare error. See expected and observed data. The Sense order was issued after a Write, Read, or Checkwrite order. The Sense data should reflect the current Address. |
| 6330 | Controller not ready after Write order. Preceding Seek order successful. |
| 6331 | Status error after Write order. No unusual status expected. The Write order will be automatically retried 6 times. |
| 6332 | Status error after Write order. The diagnostic Sense byte (byte 8 of Sense data) should indicate no errors. |
| 6333-6335 | See 6330 through 6332, respectively. Current order was a Read. The sector in error may have been incorrectly written. |
| 6336 | Read compare error. See print-out. The error may result from incorrect writing of the data. |
| 6337-6339 | See 6330 through 6332, respectively. Current order was a Checkwrite. The sector in error may have been incorrectly written if Read errors are detected. |
| 6340 | Write errors on current cylinder. If Sense Switch 1 is reset and 3 set, the Read and Check-Write portion of this test will be skipped and a new cylinder will be selected. Fixed pattern of X'AA55AA55AA5...'. |
| 6341 | Read erros on current cylinder. If Sense Switch 1 is off and 3 on, the Checkwrite portion of this test will be skipped and a new cylinder will be selected. Fixed pattern of X'AA55AA55AA5...'. |
| 6342 | Checkwrite errors on current cylinder. If Sense Switch 1 is off and 3 on, a new cylinder will be selected. Fixed pattern of X'AA55AA55AA5...'. |
| 6343 | See 6340. Write errors. Incremented pattern X'00010203040506..' |
| 6344 | See 6341. Read errors. Incremented pattern X'00010203040506..' |
| 6345 | See 6342. Check-Write errors. Incremented pattern X'00010203040506...'. |
| 6346 | See 6340. Write errors. Current Seek Address used as pattern. |
| 6347 | See 6341. Read errors. Current Seek Address used as pattern. |
| 6348 | See 6342. Check-Write errors. Current Seek Address used as pattern. |

TST1, 64 Short Record Write Test. During the first phase of this test, attempts are made to locate a sector which can be recorded and verified. Once a good sector has been located, a 4 byte record is written and verified with a Read order. Bytes 4 through 1023 are expected to be zero.

| | |
|---|---|
| 6410 | Controller not ready after Seek/CC/Write order. |
| 6411 | Status error after Write order. Normal termination expected. |
| 6412 | Controller not ready after Seek/CC/Read order. |
| 6413 | Status error after Read order. Normal termination expected. |
| 6414 | Data compare error on current sector. |
| 6415 | Controller not ready after Seek/CC/Write order (4 bytes). The remaining bytes of the current sector should contain zeros. |
| 6416 | Status error after Write order (4 bytes). Only IL is expected. |
| 6417 | Controller not ready after Seek/CC/Read order (1024 bytes). The preceding Write order recorded only 4 bytes of data. |
| 6418 | Status error after Read order. Normal termination expected. |
| 6419 | Data compare error on current sector. If word count of compare error MSG > 0, the controller failed to write zeros for bytes 4 through 1023. |
| 6420 | Write or Read errors on current sector. Another sector, if available, will be selected. |
| 6430 | Device not ready after Seek/CC/Read (BC=253)/CC/Sense. |
| 6431 | Status error after Seek/CC/Read (BC=253)/CC/Sense. Normal termination expected. |
| 6432 | Device failed to report correct sector on sense at least once in 256 cycles of: Seek/CC/Read (BC=253)/CC/Sense. |

TST1, 65 Header Write Test. This test will only be executed if cylinder 202 is made available to the test program with the SYST directive. The test will write all Headers on cylinder 202 for Heads 16 through 19. The original Headers will be saved at the start of the test and restored at the end of the test.

| | |
|---|---|
| 6510 | Controller not ready after Seek/CC/Header Write order (6 sectors). |
| 6511 | Status error after Header Write order. Normal termination expected. |
| 6512 | Controller not ready after Seek/CC/Header Read order (6 sectors). |
| 6513 | Status error after Header Read order. Normal termination expected. Headers may have been incorrectly written. |
| 6514 | Header compare errors. Each Header consists of 8 bytes. Headers may have been incorrectly written. |
| 6515 | Controller not ready after Sense order. |
| 6516 | Status in diagnostic Sense byte (byte 8 Sense data) should indicate no errors. |
| 6517 | Attempts to save 24 Headers starting at cylinder 202, Head 16, Sector 0 not successful. Remainder of this test will be skipped. |

TST1, 66 Header Error Detection Test. This test will only be executed if cylinder 202 is made available to the test program with the SYST directive. The test consists of the following 3 sections:

1. Headers with flaw bytes are written for cylinder 202, Head 17 Sense, Header Read, and Read orders are issued to verify the detection of the flaw byte and setting of UE (UE will not be set during Header Read).
2. Headers with a cylinder address of 225 are written for cylinder 202, Head 18. A Sense order is issued to verify the setting of verification error, UE, and cylinder compare error (byte 8 of Sense data).
3. Headers for cylinder 202, Head 19 contain the following information: Sector 0 OK, Sector 1 OK, Sector 2 OK, Sector 3 cylinder wrong, Sector 4 Head wrong, Sector 5 sector wrong.

4. Header Read and Read orders are issued to verify that cylinder, head, and sector compare errors are set (byte 8 of Sense data) and that the orders terminate correctly after detection of an erroneous Header.

The original Headers will be saved at the start of the test and restored at the end of the test.

| | |
|---|---|
| 6610 | See 6517 |
| 6611 | Controller not ready after Seek/CC/Header Write order (24 sectors). |
| 6612 | Status error after Header Write order. Normal termination expected. |
| 6620 | Controller not ready after Seek/CC/Sense order. All six headers starting at cylinder 202, Head 17 have flaw bytes recorded from preceding Write Pass. |
| 6621 | Status error after Sense order. UE, flaw byte (TDV bit 1) and not TE expected. All six headers starting at cylinder 202, Head 17 have flaw bytes recorded from preceding Write Pass. |
| 6622 | Controller not ready after Seek/CC/Header Read order. See also 6620. |
| 6623 | Status error after Header Read order. Flaw byte, not UE or TE expected. See also 6621. |
| 6624 | Controller not ready after Seek/CC/Read order. See also 6620. |

TST1, 66 (Continued)

6625 Status error after Read order. UE, flaw byte (TDV bit) and not TE expected. See also 6621.

6626 Controller not ready after Seek/CC/Sense order. All six headers starting at cylinder 202, Head 18 have a wrong cylinder Address (cylinder   255) recorded from preceding Write order.

6627 Status error after Sense order. UE, verification error (TDV bit 4) not UE, and byte count = 0 expected. See 6626 for header data.

6628 Controller not ready after Seek order.

6629 Controller not ready after Sense order. Status after Sense order will not be tested.

6630 Controller not ready after Header Read order at cylinder 202, Head 19, Sector 3. Header of Sector 3 was previously written with wrong cylinder Address.

6631 Status error after Header Read order. UE, verification error, and byte count = 0 expected. See also 6630 for Seek Address and data.

6632 Status in diagnostic Sense byte (byte 8 of Sense data) should indicate cylinder compare error. See also 6630 for Seek Address and data.

6633 Controller not ready after Header Read order at cylinder 202, Head 19, Sector 4. Header of Sector 4 was previously written with wrong Head Address.

6634 Status error after Header Read order. UE, verification error, and byte count = 0 expected. See also 6653 for Seek Address and data.

6635 Status in diagnostic Sense byte (byte 8 of Sense data) should indicate Head compare error. See also 6633 for Seek Address and data.

6636 Controller not ready after Header Read order at cylinder 202, Head 19, Sector 5. Header of Sector 5 was previously written with wrong Sector Address.

6637 Status error after Header Read order. UE, verification error, and byte count = 0 expected. See also 6636 for Seek Address and data.

6638 Status in diagnostic Sense byte (byte 8 of Sense data) should indicate Sector compare error. See also 6636 for Seek Address and data.

6639 Controller not ready after Header Read order (17 bytes) at cylinder 202, Head 19, Sector 2. Header of Sector 2 OK, Header of Sector 3 was previously written with the wrong Cylinder Address.

6640 Status error after Header Read order (17 bytes). UE, verification error, and byte count = 1 expected. Headers for Sectors 2 and 3 should be read. See also 6639 for Seek Address and data.

6641 Status in diagnostic Sense byte (byte 8 of Sense data) should indicate cylinder compare error. See also 6639 for Seek Address and data.

6642 Controller not ready after Read order (1 byte) at cylinder 202, Head 19, Sector 3. Header of Sector 3 was previously written with wrong Cylinder Address.

6643 Status error after Read order. UE, verification error, byte count   1 expected. See also 6642 for Seek Address and data.

6644 Status in diagnostic Sense byte (byte 8 of Sense data) should indicate Sector compare error. See also 6642 for Seek Address and data.

6645 Controller not ready after Read order (1025 bytes) at cylinder 202, Head 19, Sector 2. Header of Sector 2 OK, Header of Sector 3 was previously written with wrong Cylinder Address.

6646 Status error after Read order. UE, verification error, byte count = 1 expected. See also 6645 for Seek Address and data.

6647 Status in diagnostic Sense byte (byte 8 of Sense data) should indicate cylinder compare error. See also 6645 for Seek Address and data.

6648 Controller not ready after Read order (1 byte) at cylinder 202, Head 19, Sector 5. Header of Sector 5 was previously written with wrong Cylinder Address.

6649 Status error after Read order. UE, verification error, byte count = 1 expected. See also 6648 for Seek Address and data.

6650 Status in diagnostic Sense byte (byte 8 of Sense data) should indicate Sector compare error. See also 6648 for Seek Address or data.

6660 Controller not ready after Seek order (cylinder 202, Head 17, Sector 0)//CC// HD Read//CC//Seek (cylinder 202, Head 18, Sector 0)//Read.

6661 Status error. No UE, no flawmark, Command Address +3 expected.

TST1, 70 Dual Controller Test. An SIO order is sent to the first controller which will reserve the device until a Release order is issued. The second controller will now try to influence that device while the first controller is in both Busy and Ready state. After the test sequence is completed, the second controller is tested in the same way. Device Address must be entered with the SYST directive:

SYST, D1, X2, X3, X4, X5, X6, X7, X8, X9, X10
where each pair (X3, X5), (X7, X9), etc., must have the same device on different controllers. A minimum of 1 pair must be entered (maximum 4 pairs).

Example: SYST, 7240, 0, F0, 202, 1F0, 202
Or: SYST, 7240, 0, F0, 202, E0, 202

7010 Expected 2 or more Device Addresses entered by 'SYST' directive.

7011 Release order for device 2 not accepted. See print-out.

7012 Release order for device 1 not accepted. See print-out.

7013 SIO to device 1 not accepted. See print-out.

7014 IO order to device 2 was accepted, should have been rejected. See print-out.

7015 IO interrupt did not occur within time limit.

# Section 8

# SIGMA 5 - 9
# REMOVABLE DISK STORAGE TEST (7270/71)

## PROGRAM NO. 706424

## Section 8

## CONTENTS

Page

Subject Model . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 8-1
Required Equipment . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 8-1
Program Prerequisites . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 8-1
General Operating Procedures . . . . . . . . . . . . . . . . . . . . . . . . . . . . 8-1
Directives . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 8-2
Start Procedure . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 8-3
Program Test Description . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 8-4
Order Codes . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 8-4
TDV Status . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 8-4
AIO Status . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 8-4
Test Mode Data Byte . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 8-5
Addressing Format . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 8-5

# 8. SIGMA 5–9 REMOVABLE DISK STORAGE TEST (7270/71)

**SUBJECT MODEL** -- Removable Disk Controller Model number 7270, Removable Disk Storage Units, Model number 7271, Removable Disk Controller Modified, Model number 7240, Removable Disk Storage Unit, ISS Model number 715X, 715DX

**REQUIRED EQUIPMENT**--Minimum Memory Size: 16K; Input Device: Card Reader, Paper Tape Reader or Magnetic Tape Unit; Output Device: Keyboard Printer or Line Printer

## PROGRAM PREREQUISITES

None

## GENERAL OPERATING PROCEDURES

General operating procedures of the Xerox Sigma 5 through 9 Diagnostic Program Monitor (DPM) apply to this program.

# 8. SIGMA 5–9 REMOVABLE DISK STORAGE TEST (7270/71)

**DIRECTIVES** - directives are entered after a "!" is typed out

| Name | Format | Parameter | | | |
|---|---|---|---|---|---|
| | | ID | Definition | Value Range | Standard Value (default) |
| Program Directives - Environmental Directives | | | | | |
| System Environment | SYST, D1, D2,<br>H3, H4, H5, H6<br>,H7 . . . ,H17,H18 | D1 | Controller model number | 7270, 7240 | |
| | | D2 | Revision number | 0 | |
| | | H3 | Storage Unit Device Address (1st) | 80 ~ 1FFF | |
| | | H4 | Available cylinders (1st) 405 → | 00XY00ZW | |
| | | H5 | Storage Unit Device Address (2nd) | 80 ~ 1FFF | |
| | | H6 | Available cylinders (2nd) 405 → | 00XY00ZW | |
| | | ⋮ | | | |
| | | H17<br>H18 | Same as H3, H4 except for 8th Storage Unit | XY = 1st cylinder<br>ZW = last cylinder | |
| Program Directives - Testing Directives | | | | | |
| Comprehensive Test (all functional tests, 1 thru 70, and random exerciser Test) | TST0, D1, D2 | D1 | Number of ordered sequences executed by random exerciser | 0 ~ 99999999 | 5000 (D1 = 0) |
| | | D2 | Number of retries | 0 ~ 99999999 | 0 |
| Functional Test | TST1 [, D1 [, D2]] | D1 | The first subtest to be executed | 0 (all subtests) ~ 70 | 0 |
| | | D2 | Last subtest to be executed | 1 | D1 |
| Random Exerciser Test | TST2, D1, D2 | D1 | Number of cycles to be performed | D1 ≥ 0 | |
| | | D2 | Number of retries before next cycle | D2 ≥ 0 | |
| Utility Test | TST3, D1, D2, D3, H4<br>TST3,2,0 → | | D1 - Utility Test selection<br>D2 - Function selection or serial number<br>D3 - Retry count; not used if D1 = 3<br>D1 = 1 Surface Test<br>D2 = 0 Write and then read all sectors<br>D2 = 1 Write all sectors<br>D2 = 2 Read all sectors<br>D2 = 3 Read all sectors (no data check)<br>D2 = 4 Checkwrite all sectors<br>D2 = 5 Write and then checkwrite all sectors<br>D1 = 2 Header Test<br>D2 = 0 Write and then read all headers<br>D2 = 1 Write all headers<br>D2 = 2 Read all headers<br>D2 = 3 Read all headers (no data check)<br>D1 = 3 Disk Initialization<br>D2 = Pack serial Number<br>D3 = 0 - Not used<br>H4 = Date = 00MMDDYY<br>D1 = 4 Flaw A Track<br>D2 = Alternate Cylinder Address<br>D3 = Alternate Head ADR | 400 ~ 405<br>0 - 19 | |
| Program Directives - Optional Directives | | | | | |
| Pattern selection (for Utility Test) | DATA, D1, H2, H3 | D1 | = 0, Fixed Pattern<br>= 1, Incremental Pattern<br>= 2, Random Pattern<br>= 3, Current Seek Address | 0 ~ 3 | |
| | | H2 | Pattern seed (for D1 = 0, 1, 2) | 00000000 ~ FFFFFFFF | |
| | | H3 | Incrementing constant (for D = 1) | | |
| Usable surface area limitation | SEEK, D1, D2, D3, D4 | D1 | Starting cylinder address | 0 ~ 405 | |
| | | D2 | Starting head address | 0 ~ 19 | |
| | | D3 | Starting sector address | 0 ~ 5 | |
| | | D4 | Additional sectors to be used after starting address D1, D2, D3 | (0 ~ 81) | |
| Limitation of Error printouts | LIMT, D1, D2 | D1 | = 1 Limit Compare error printouts/sector to D2 | 1 | |
| | | D2 | Maximum number of printouts (No limit if D2 = 0) | D2 ≥ 0 | |
| I/O buffer area definition | MEM [, H1, H2] | H1 | First location of I/O buffer area | Obtainable by typing in MEM | Area between Diag. Prog. & DPM |
| | | H2 | Last location of I/O buffer area | | |
| I/O Reset | RSET | 0 | | | Not available |

Note: Parameter of any directive beginning with a D means decimal, with an H means hexadecimal

# 8. SIGMA 5-9 REMOVABLE DISK STORAGE TEST (7270/71)

## START PROCEDURE

1. Sense Switch Options, Monitor Directive Options, and Environmental Directives - Refer to DPM section of this manual.
2. Test Strategy Selection

| | Comprehensive Test | Functional Test | Random Exerciser Test | Utility Test |
|---|---|---|---|---|
| Recommended Application | Normal Usage | Solid Failure Detection and Specific Problem Analysis | Intermittent Failure Detection | Surface Test |
| Test Directive | TST0 | TST1 | TST2 | TST3 |
| Prerequisite | None | None | TST1 | TST1 |
| Optional Directives | SEEK, LIMT, MEM | SEEK, LIMT, MEM | SEEK, LIMT, MEM | SEEK, LIMT, MEM, DATA |
| Subtests | All functional subtests (1 ~ 70) and random exerciser test | 70 subtests (see error messages for the test types) | 1. Exerciser Initiation: Random data written on entire surface<br>2. Random Selection of:<br>a. Device<br>b. Order Sequences<br>c. Buffer Areas<br>d. Buffer Length<br>e. Data | WRITE only<br>READ only (Verify data)<br>READ only (No data verification)<br>READ header<br>CHECKWRITE<br>WRITE/READ TEST<br>WRITE header |
| Error Message Format | 1. ERROR NO. DDDD LOC XXXX<br>2. Self-explanatory | ERROR NO. DDDD LOC XXXX | Self-explanatory | Self-explanatory |

3. Procedure 2 of Restart Procedure of DPM should normally be used to clear a wait from a watchdog timer trap.

## PROGRAM TEST DESCRIPTION

Test descriptions of each functional test are included at the beginning of each subtest error number in the Functional Subtest and Related Error Message Section.

## ORDER CODES

| | |
|---|---|
| X'00' | STOP |
| X'01' | WRITE |
| X'02' | READ 2 (Report any transmission error at count done) |
| X'03' | SEEK |
| X'04' | SENSE |
| X'05' | CHECKWRITE |
| X'12' | READ 1 (Terminate data transfer and report any transmission error at end of current sector if error is encountered) |
| X'13' | SELECT TEST MODE |
| X'80' | STOP AND INTERRUPT (at location X'5C') |
| X'09' | HEADER WRITE |
| X'0A' | HEADER READ |
| X'33' | RESTORE CARRIAGE |
| X'23' | RELEASE |
| X'83' | SEEK (and cause a device interrupt on position complete or time out) |

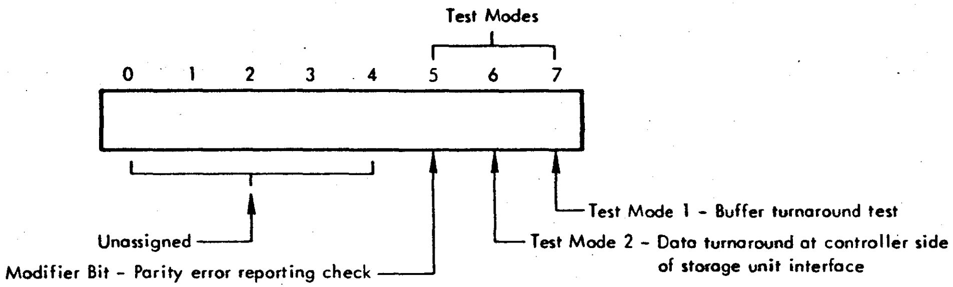
## TDV STATUS

| | BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| MODEL | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| REM DISK | Data Overrun | Flaw Mark | Sector Unavailable | Unassigned | Header Verification Error | Head On Cylinder | Seek Timeout Error | Header Parity Error |

## AIO STATUS

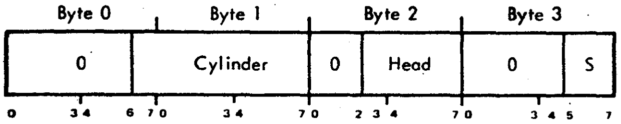
| | BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| MODEL | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| REM DISK | Data Overrun | ←—— UNASSIGNED ——→ | | | Device Interrupt | Head On Cylinder | Seek Timeout Error | Unassigned |

## TEST MODE DATA BYTE


Test Modes
0
1
2
3
4
5
6
7
Unassigned
Modifier Bit - Parity error reporting check
Test Mode 1 - Buffer turnaround test
Test Mode 2 - Data turnaround at controller side of storage unit interface

## ADDRESSING FORMAT

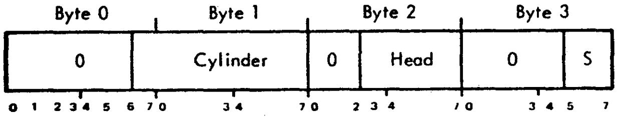
1. The format of the four byte sent to the Disk Pack by a SEEK order is:

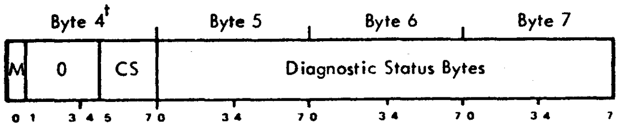

Byte 0
Byte 1
Byte 2
Byte 3
0
Cylinder
0
Head
0
S
0 3 4 6 7 0 3 4 7 0 2 3 4 7 0 3 4 5 7

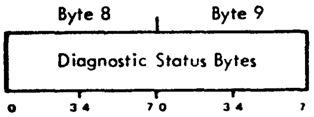
where S signifies sector number.

2. The format of the bytes received on a SENSE order is:
SENSE (X'04')

The Sense order causes the controller to transmit up to 10 bytes of information to the IOP, as follows:


Byte 0
Byte 1
Byte 2
Byte 3
0
Cylinder
0
Head
0
S
0 1 2 3 4 5 6 7 0 3 4 7 0 2 3 4 7 0 3 4 5 7

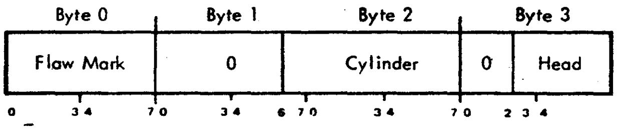

Byte 4†
Byte 5
Byte 6
Byte 7
M
0
CS
Diagnostic Status Bytes
0 1 3 4 5 7 0 3 4 7 0 3 4 7 0 3 4 7

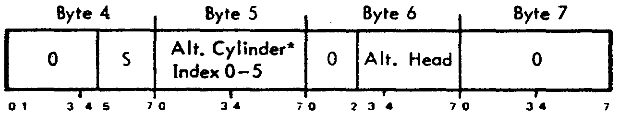

Byte 8
Byte 9
Diagnostic Status Bytes
0 3 4 7 0 3 4 7

where
S signifies sector number
M signifies modifier bit
CS signifies current sector number

3. The format of the 8 bytes sent to the Disk Pack by a WRITE header order is:
HEADER WRITE (X'09')

The Header Write order causes the controller to consider all subsequent data bytes as header information. Each header requires the following bytes:


Byte 0
Byte 1
Byte 2
Byte 3
Flaw Mark
0
Cylinder
0
Head
0 3 4 7 0 3 4 6 7 0 3 4 7 0 2 3 4


Byte 4
Byte 5
Byte 6
Byte 7
0
S
Alt. Cylinder* Index 0–5
0
Alt. Head
0
0 1 3 4 5 7 0 3 4 7 0 2 3 4 7 0 3 4 7

*The alternate cylinder index (8 bits) represents a cylinder index into cylinder 400–405.

Sense Status Bytes 8 and 9

| Byte No. | Bit No. | Function |
|---|---|---|
| 8 | 0 | Data parity error |
| | 1 | Check-Write error |
| | 2 | Sector verification error |
| | 3 | Head verification error |
| | 4 | Cylinder verification error |
| | 5 | Sector address not zero at start of header write operation |
| | 6 | Difference select sent to device |
| | 7 | Sector select sent to device |
| 9 | 0 | Control select sent to device |
| | 1 | Head select sent to device |
| | 2 | Cylinder select sent to device |
| | 3 | Seek forward set |
| | 4 | Read gate sent to device |
| | 5 | Write and erase gate sent to device |
| | 6 | Read cylinder select sent to device |
| | 7 | Not used |
| Note: Bytes 8 and 9 are used by diagnostic programs. | | |

---

† Three bits of byte 4 indicate current sector number, but if the most significant bit (M) is a 1, the arm was in motion at time of sense and current sector number is meaningless. If the head number is nonexistent, (M) will also be a 1.

## FAULT INDEX DESCRIPTION - FUNCTIONAL SUBTESTS

The fault index contains a brief description of each functional subtest and a list of associated error numbers with a brief description of each error. The subtests and error numbers are arranged in ascending sequence. The description of subtest NN is numbered NN00. The first two digits of the error number correspond to the associated subtest; the last two numbers correspond to the individual errors within the subtest.

System error numbers
8500 Controller did not return to Ready condition after Test Mode order.
8501 Controller not in Test Mode after Test Mode order. TDV CC = 0.
8502 Controller in Test Mode after resetting Test Mode. TDV CC = 4.
8510 Controller did not return to Ready condition after Restore order.
8511 Device not on cylinder after a Restore order.

TST1, 01 AIO, HIO, TIO, TDV instruction recognition.

0110 AIO Condition Code error. No interrupt recognition expected.
0111 HIO Condition Code or Status error. See printout.
0112 TIO Condition Code or Status error. See printout. Preceding HIO did not reset Status.
0113 TDV Condition Code error. See printout.

TST1, 02 SIO Invalid Order Test

0210 SIO for Invalid order not accepted. See printout.
0211 Controller not ready after Invalid order (00 or F8). Order output and order input phases must be executed.
0212 Status error after Invalid order. UE expected.
0213 Byte count was changed during execution of Invalid order. Data phase not required.

TST1, 03 Test Mode Selection Test. A TDV instruction is used to verify setting and resetting of Test Mode.

0301 Test Mode byte = X'FF'.
0302 Test Mode byte = X'01'.
0303 Test Mode byte = X'02'.
0310 TDV CC2 reset. Device controller not in Test Mode.
0311 Output buffer changed during Test Mode order (Select). Data in phase not expected.
0312 TDV CC2 set. Device controller remains in Test Mode. CC2 = 0 expected.
0313 Output buffer contains ones after Test Mode order (Reset).
0315 TIO CC1 or CC2 set. Controller not ready after Test Mode order.
0316 TDV, TIO Status error or byte count error. See preceding printout. Operation: Order out (X'13'), data out (1 byte), order in.
0321, 0322, 0323 TST1, Three data byte of FF, 01, and 02 was used during data output phase. See preceding printout.

TST1, 04 Interrupt generation and HIO, AIO Instruction Test. The following orders will be issued: X'00', X'13' (data byte = 01), X'1' (data byte = 00) in order to set Interrupt Pending due to IUE, ICE and IZC, respectively. Each order will be repeated once to allow resetting of IP with an HIO and an AIO instruction.

0410 TIO Status error during TST1, 4 after SIO. IP must be set and controller and device must be ready. IUE, ICE, and IZC flags are used.
0411 HIO did not reset IP. No reset generated.
0412 AIO Status error during TST1, 4. Preceding SIO resulted in IP.
0413 AIO did not reset IP. No reset generated.
0421, 0422, 0423 TST1, 4 IOP flags for IUE, ICE, and IZC used, respectively. See printout.

TST1, 05 IO Interrupt Test. A Test Mode order with ICE flag will be issued and tests will be performed to verify that the program is only interrupted if the IO Interrupt is armed and enabled.

0510 TIO Status error during TST1, 5 after SIO. IP must be set. IO Interrupt is disarmed/disabled. Program should not be interrupted.
0511 Program was interrupted while IO Interrupt was disarmed/disabled.
0512 Program was interrupted while IC Interrupt was armed/disabled.
0513 Program was not interrupted while IC Interrupt was armed/disabled.

TST1, 06 Command Chaining Test. Two Test Mode orders will be Command Chained. Command Chaining will be tested. Invalid order Command Chained to a Test Mode order should not result in Command Chaining.

0610 TIO Status error during TST1, 6 after Command Chaining or Command Chaining not performed. See preceding printout.
0611 TIO Status error during TST1, 6. Status error or Command Chaining not inhibited by UE from Invalid order.

TST1, 07 FAM Write/Read Byte Count Test. Write and Read orders with byte counts varying sequentially from 1 to 16 are issued in Test Mode 1. Zero byte count expected.

0710 Controller not ready after Write order in TM1.
0711 Controller not ready after Read order in TM1.
0712 Byte count not equal to zero after Write order in TM1.
0713 Byte count not equal to zero after Read order in TM1.

TST1, 08 FAM Write/Read Data Test. Write Command-Chain Read orders will be issued with varying data pattern. The Read data will be compared to the Write data. During the second part of the test 4 Write/CC/Read orders with counts of 13 will be issued to test the byte alignment logic.

0810 Controller not ready after Write/CC/Read order in TM1.
0811 Compare errors during TST1, 8. Output buffer: IOBF1, Input buffer: IOBUF.
0812 Controller not ready after Write/CC/Read (BC = 13) Test Mode 1.
0813-0816 Read Data compare error following Write/CC/Read (BC = 13).
If last digit is 3, data started on word boundary
If last digit is 4, data started at byte 1
If last digit is 5, data started at byte 2
If last digit is 6, data started at byte 3

TST1, 09 Test Mode 2 - Seek Order Byte Count Test. Seek orders with byte counts of 3, 4, 5 are issued to the controller and the status response is tested.

0910 Controller not ready after Seek order in Test Mode 2.
0911 Status error after Seek order in Test Mode 2. Expected: IL, UE, zero byte count, on-cylinder. See printout.
0912 Status error after Seek order in Test Mode 2. Expected: Not IL, zero byte count, on cylinder. See printout.
0913 Status error after Seek order in Test Mode 2. Expected: IL, byte count = 1, on-cylinder. See printout.
0914 Output buffer (:IOBF1) altered during Seek in TM2.

TST1, 10 Test Mode 2 - Seek Order Interrupt Address Test. Seek orders will be to device 0 through 7 in sequence and the address returned with the AIO Status will be verified. Change above mask from X'04000000' to X'0C000000' if Device Interrupt Engineering Order is available.

1010 Status error after Seek order with Interrupt Modifier bit. Expected: IP, zero byte count, on cylinder. See printout.
1011 AIO Status error after Seek order with Interrupt Modifier bit. IP set prior to AIO. Expected: Address verification. See printout.
1012 Preceding AIO did not clear Seek complete interrupt (TIO/IP=0).

TST1, 13 Test Mode 2 - Sense Order Byte Count Test. Sense orders with byte counts of 1 through 11 are issued to the controller and the Status Response is tested.

1310 Controller not ready after Sense order in Test Mode 2.
1311 Status error after Sense order in Test Mode 2. No unusual status expected. See printout.
1312 Byte count not equal to zero after a Sense order with a byte count ≤10. See printout.
1314 First 8 bytes of input buffer (IOBF1) not changed during Sense order. Data input expected.

TST1, 15 Test Mode 2 - Seek Tag Line Test. See/Command Chain/ Sense orders are executed and the Tag Line information in byte 8 of the Sense data is verified.

1510 Controller not ready after Seek/CC/Sense order in Test Mode 2.
1511 Status error after Sense order or Command Chaining not performed. See printout.
1512 Seek Tag Line error or Sense order not functioning properly. Sense buffer: IOBF1. See printout.

TST1, 16 Test Mode 2 - Head and Sector Address Test. Seek/CC/ Sense orders are issued sequentially varying the Device Address from 0 - 7. Sense data is verified. Sense orders are issued sequentially to all devices to insure that the addresses are not changed. The same sequence is repeated with the Device Address varied from 7 - 0. The complement of the data pattern in pass 1 is used in pass 2. A unique pattern is used for each device.

1610 Controller not ready after Seek/CC/Sense order in Test Mode 2.
1611 Controller not ready after Sense order in Test Mode 2.
1620-1627 Head and Sector Address obtained during Sense not equal to original data. Last digit of error number indicates Device Address used. Address sequence 0 - 7. Order sequence: Seek/ CC/Sense.
1630-1637 Head and Sector Address obtained during Sense not equal to original data. Check addressing of Head and Sector FAM. Last digit of error number indicates Device Address used.
1640-1647 Same as 1620-1627. Address sequence 7 - 0.
1650-1657 Same as 1630-1637.

TST1, 17 Test Mode 2 - Head and Sector Address Validity Test. Seek and Sense are issued 406 times varying the Sector Address from 0-7 and the Head Address from 0-25. Sector unavailable will be tested for Sector Address > 5 and Head Address > 19. The combined Sector and Head Address which is returned as Cylinder Address during Seek will be verified.

1710 Controller not ready after Seek order in Test Mode 2.
1711 Status error after Seek order in Test Mode 2 with illegal sector Address (7). UE, sector unavailable, on cylinder expected.
1712 See 1711. Illegal Head Address was issued during Seek.
1713 Status error after Seek order in Test Mode 2. Legal Head and Sector Address were used. See printout.
1714 Controller not ready after Sense order in Test Mode 2.
1715 Seek/Sense compare error. The Head/Sector Address was not returned correctly as the Cylinder Address. See printout.

TST1, 19 Test Mode 2 - Cylinder Difference Logic Test. Seek and Sense orders are issued systematically varying the Cylinder and Head/Sector Address. Five passes will be performed:

1. Cyl and Hd/Sect 0 - 405.
2. Cyl = 0 - 405, Hd/Sect 0
3. Cyl = 0, Hd/Sect = 0 - 405
4. Cyl = 405 - 0, Hd/Sect 0
5. Cyl 0, Hd/Sect = 405 - 0

1910 Controller not ready after Seek order in Test Mode 2.
1911 Controller not ready after Sense order (Byte count = 10) in Test Mode 2.
1912 The difference between Head/Sector and the Cylinder Address returned in byte 7 of the Sense order is not correct. See printout.
1913 Controller not ready after the second Seek order in Test Mode 2. Two Seek orders are required to obtain the correct difference in byte 7 of the Sense data.

TST1, 20 Test Mode 2 - Illegal Cylinder Address Test. Seek orders are issued with illegal Cylinder Address (406 - 511) and the Status Response is verified.

2010 Controller not ready after Sense order in Test Mode 2.
2011 Status error after Seek order in Test Mode 2 with Illegal Cylinder Address (406 - 511). UE, sector unavailable, on cylinder expected.

TST1, 23 Test Mode 2 - Restore Order Test. A Seek/CC/Restore and Sense order sequence is sequentially issued to all devices (0 - 7). The test verifies the status after the Restore orders and verifies with a Sense order (Byte count = 10) that the Head and Sector Address in the FAM are cleared to zero and that the Restore order generated the correct Tag Lines.

2310 Controller not ready after Seek/CC/Restore orders in Test Mode 2.
2311 Status error after Restore order in Test Mode 2. Not UE, byte count = 1 (no changes). See printout.
2312 Controller not ready after Sense order in Test Mode 2.
2313 Bytes 2 (Head) and 3 (Sector) of Sense data not 0. Preceding Restore order did not clear controller registers (FAM).
2314 Restore Tag Line error. Sense buffer: IOBF1. See printout.

TST1, 24 Test Mode 2 - Release Order Test. A Release order and a Sense order is issued. The test verifies the status after the Release and verifies with a Sense order (Byte count = 10) that the Release order generated the correct Tag Lines.

2410 Controller not ready after Release order in Test Mode 2.
2411 Status error after Release order in Test Mode 2. Not UE, byte count = 1 (No change) expected. See printout.
2412 Controller not ready after Sense order in Test Mode 2.
2413 Release Tag Line error. Sense buffer: IOBF1. See printout.

TST1, 25 Test Mode 2 - Read Order Tag Line and Data Test. Read orders X'02' and X'12' are issued in sequence. The status and byte count are verified. The Read data is compared to the expected information. A Sense order verifies that the Tag Lines are correctly generated for a Read order.

2510 Controller not ready after Read order (02) in Test Mode 2.
2511 See 2510. Read order (12).
2512 Status error after Read order in Test Mode 2. Not UE, not IL, not TE, byte count = 0 expected. See printout.
2513 See 2512. Read order (12).
2514 Data compare error in Test Mode 2; Read order (02). See printout.
2515 See 2514. Read order (12).
2516 Controller not ready after Sense order in Test Mode 2.
2517 Read (02) Tag Line error. Sense buffer: IOBF1, See printout.
2518 See 2517. Read order (12).
2519 Status error in diagnostic Sense byte (byte 8 of Sense data) defines Read error.
2520 See 2519. Read order (12).

TST1, 26 Test Mode 2 - Read Order Incorrect Length Test. Read orders are issued with byte count sequentially varied from 1008 to 1025 (not 1024). The status will be verified. For byte counts < 1024 the test verifies that the controller terminates data-in at the correct byte count.

2610 Controller not ready after Read order (02) in Test Mode 2.
2611 Remaining byte count after Read order with incorrect length not zero. See printout.
2612 Status error after Read order in Test Mode 2. IL expected. See printout.
2613 Data compare error in Test Mode 2; Read order (02). For byte count < 1024 the ramaining bytes in input buffer must be zero.

TST1, 27 Test Mode 2 - Read Order/Head and Sector Incrementation Test. Seek/CC/Read and Sense order sequences are issued with a Read byte count of 1024. Sector and Head Address incrementation is verified.

2710 Controller not ready after Seek/CC/Read (02) orders in Test Mode 2.
2711 Status error after Seek/CC/Read in Test Mode. No abnormal status expected. See printout.
2712 Controller not ready after Sense order in Test Mode 2.
2713 Address received during Sense not expected. Head or Sector Address may not increment properly. See printout.

TST1, 28 Test Mode 2 - Read Order Cylinder Boundary Test. A Read order with a byte count of 1025 is issued starting at Head 19, Sector 5. Read operation will terminate after 1 sector and sector unavailable will be reported.

2810 Controller not ready after Seek/CC/Read (02) orders in Test Mode 2.
2811 Status error after Read order (Seek Address = Head 19. Sector 5, byte count = 1025). UE, sector unavailable, byte count = 1 expected. See printout.

TST1, 29 Test Mode 2 - Header Read Order Test. Seek/CC/Header Read orders sequences are issued with Header Read byte count of 8. The status and byte count are verified. The Header Read data is compared to the expected information. A Sense order verifies that the Tag Lines are correctly generated and that the Head and Sector Address are incremented correctly.

2910 Controller not ready after Seek/CC/Header-Read orders in Test Mode 2.
2911 Status error after Header Read order. No abnormal status expected. See printout.
2912 Header data compare error in Test Mode 2. See printout.
2913 Controller not ready after Sense order in Test Mode 2. See printout.
2914 Header Read Tag Line error. Sense buffer: IOBUF. See printout.
2915 Status error in diagnostic Sense byte (Byte 8 of Sense data) defines Header Read error.
2916 Address received during Sense not expected. Head or Sector Address may not increment properly. See printout.

TST1, 30 Test Mode 2 - 120 Sector Header Read Test. A Seek/CC/Header Read order with a Header Read byte count of 960 is issued. The Header data is verified. No data error indicates that the Head and Sector Incrementation Logic performs correctly.

3010 Controller not ready after Header Read order in Test Mode 2.
3011 Byte count not zero after Header Read order (960 bytes).
3012 Status error after Header Read order. No abnormal status expected.
3013 Header data compare error in Test Mode 2. See printout.

TST1, 31 Test Mode 2 - Header Read Byte Count Test. Header Read orders with byte counts of 7 and 9 are issued to the controller and the Status Response is tested.

3110 Controller not ready after Header Read order in Test Mode 2.
3111 Status error after Header Read order (byte count 7). Expected: IL, no UE, byte count = 0. See printout.
3112 See 3111. Header Read order byte count = 9.

TST1, 32 Test Mode 2 - Header Read Order Cylinder Boundary Test. A Header Read order with a byte count of 9 is issued starting at Head 19, Sector 5. Read operation will terminate after one sector and sector unavailable will be reported.

3210 Controller not ready after Header Read order in Test Mode 2.
3211 Status error after Header Read order (Seek address = Head 19, Sector 5, byte count = 9). UE, sector unavailable, byte count = 1, expected.

TST1, 35 Test Mode 2 - Header Write Order Test. Seek/CC/Header Write order sequences are issued with Header Write byte counts of 48. The Header data consists of a X'A5A5A5A5' pattern. The status and byte count are verified. A Sense order verifies that the Tag Lines are correctly generated and that the Head and Sector Address increment correctly.

3510 Controller not ready after Seek/CC/Header-Write orders in Test Mode 2.
3511 Status error after Header Write order. No abnormal status expected. See printout.
3512 Controller not ready after Sense order in Test Mode 2.
3513 Header Write Tag Line error. Sense buffer: IOBF1. See printout.
3514 Status error in diagnostic Sense byte (byte 8 of Sense data) defines Header Write error.
3515 Address received during Sense not expected. Head or Sector Address may not increment properly. See printout.

TST1, 36 Test Mode 2 - 120 Sector Header Write Test. A Seek/CC/Header Write order sequence with a Header Write byte count of 960 is issued. A Sense order is issued to verify that the Head and Sector Address are incremented to Head 20, Sector Sector 0.

3610 Controller not ready after Seek/CC/Header-Write orders in Test Mode 2.
3611 Byte count not zero after Header Write order (960 bytes).
3612 Status error after Header Write order. No abnormal status expected.
3613 Controller not ready after Sense order in Test Mode 2.
3614 Address received during Sense not expected. Header or Sector Address have not been incremented past Head 19, Sector 5.

TST1, 37 Test Mode 2 - Header Write Byte Count Test. Header Write orders with byte counts of 7 and 9 are issued to the controller and the Status Response is tested.

3710 Controller not ready after Seek/CC/Header-Write order in Test Mode 2.
3711 Status error after Header Write order (byte count 4). Expected: IL, no UE, byte count = 0. See printout.
3712 See 3711. Header Write order byte count = 9.

TST1, 38 Test Mode 2 - Header Write Order Cylinder Boundary Test. A Header Write order with a byte count of 49 is issued starting at Head 19, Sector 0. Write operation will terminate after six sectors and sector unavailable will be reported.

3810 Controller not ready after Header Write order in Test Mode 2.
3811 Status error after Header Write order (Seek Address = Head 19, Sector 0, byte count = 49). UE, sector unavailable, byte count = 0 expected.

TST1, 39 Test Mode 2 - Header Write Starting Address Test. Header Write orders with Starting Sector Address of 0 through 5 are sequentially issued. For all Starting Addresses except 0, byte 8 of the Sense data will indicate Header Address error.

3910 Controller not ready after Header Write order in Test Mode 2.
3911 Status error after Header Write order. No abnormal status expected.
3912 Controller not ready after Sense order in Test Mode 2.
3920-3925 Status error in diagnostic Sense byte (byte 8 of Sense data). The least significant digit of error number reflects the Starting Sector Address of the Header-Write operation. Header-Address error is expected for all Starting Address except Sector 0.

TST1, 40 Test Mode 2 - Write Order Test. Seek/CC/Write order sequences are issued with Write byte count 3 or 1024. The Write data consists of byte values starting at 224, with each successive byte   byte (N) + 1. These values reflect the byte counter in the controller at the time of writing each byte. Status and byte count are verified. A Sense order verifies that the Tag Lines are correctly generated and that the Head and Sector Address increment correctly.

4010 Controller not ready after Seek/CC/Write orders in Test Mode 2.

4011 Status error after Write order. No abnormal status expected.

4012 Controller not ready after Sense order in Test Mode 2.

4013 Write Tag Line error. Sense buffer: IOBF1. See printout.

4014 Status error in diagnostic Sense byte (byte 8 of Sense data) defines Write error.

4015 Address received during Sense not expected. Head and Sector Address may not increment properly. See printout.

TST1, 41 Test Mode 2 - Write Order Incorrect Length Test. Seek/CC/Write order sequences are issued with byte counts sequentially varied from 1008 to 1025 (not 1024). The status will be verified.

4110 Controller not ready after Write order in Test Mode 2.

4111 Remaining byte count after Write order with Incorrect Length not zero. See printout.

4112 Status error after Write order in Test Mode 2. IL expected. See printout.

TST1, 42 Test Mode 2 - Write Order Cylinder Boundary Test. A Write order with a byte count of 1025 is issued starting at Head 19, Sector 5. The Write operation will terminate after 1 sector and sector unavailable will be reported.

4210 Controller not ready after Write order in Test Mode 2.

4211 Status error after Write order (Seek Address = Head 19, Sector 5 byte count 1025). UE, sector unavailable, byte count = 0 expected.

TST1, 45 Test Mode 2 - Check-Write Order Test. Seek/CC/Check-Write order sequences are issued with byte counts of 1024. The Check Write data consists of byte values starting at 224, with each successive byte = byte (N) + 1. A Sense order verifies that the Tag Lines are correctly generated and that the Head and Sector Address increments correctly.

4510 Controller not ready after Seek/CC/Check-Write orders in Test Mode 2.

4511 Status error after Check-Write order. No abnormal status expected. See printouts.

4512 Controller not ready after Sense order in Test Mode 2.

4513 Check-Write Tag Line error. Sense buffer: IOBF1. See printout.

4514 Status error in diagnostic Sense byte (byte 8 of Sense data) defines Check-Write error.

4515 Address received during Sense not correct. Head or Sector Address may not increment properly. See printout.

TST1, 46 Test Mode 2 - Check-Write Order Incorrect Length Test. Seek/CC/Check-Write order sequences are issued with byte count sequentially varied from 1008 to 1025 (not 1024). The status will be verified.

4610 Controller not ready after Seek/CC/Check-Write order in Test Mode 2.

4611 Remaining byte count after Check-Write order with Incorrect Length not zero. See printout.

4612 Status error after Check-Write order in Test Mode 2. IL L L expected. See printout.

TST1, 47 Test Mode 2 - Check-Write Order Cylinder Boundary Test. A Check-Write order with a byte count of 1025 is issued starting at Head 19, Sector 5. The Check-Write operation will terminate and after one sector and sector unavailable will be reported.

4710 Controller not ready after Check-Write order in Test Mode 2.

4711 Status error after Check-Write order (Seek address = Head 19, Sector 5, byte count 1025). UE, sector unavailable, byte count 0 expected.

TST1, 48 Test Mode 2 - Check-Write Transmission Error Test. Seek/CC/Check-Write order sequences with byte counts of 2048 are issued. The Check-Write data consists of byte values starting at 224 (X'E0'), with each successive byte = byte (N) + 1. During the first 8 passes one bit in byte 32 (X'FF') is sequentially dropped starting with bit 0 and ending with bit 7. During the second 8 passes one bit in byte 33 (X'00') is sequentially picked-up starting with bit 0 and ending with bit 7. The test verifies that a single bit failure in a sector is detected and reported as TE and that the operation terminates after the first sector. The remaining byte count must be ≥1000.

4810 Controller not ready after Seek/CC/Check-Write order in Test Mode 2.

4811 Remaining byte count after Check-Write order (2048 bytes) less than 1008. Check-Write operation did not terminate after one sector.

4812 Controller not ready after Sense order in Test Mode 2.

4813 Address received during Sense not correct. Head or Sector Address may have been incremented by two sectors.

4814 Status error in diagnostic Sense byte (byte 8 of Sense data) should indicate Check-Write error.

4820-4827 Status error after Check-Write order. TE and not IL or UE expected. The least significant digit of the error number indicates which bit of byte 32 of the Check-Write data was dropped to induce a Check-Write error.

4830-4837 See 4820-4827. The least significant digit of the error number indicates which bit of byte 33 of the Check-Write data was added to induce a Check-Write error.

TST1, 49 Test Mode 2 - Halt On Transmission Error Test. Seek/CC/Write order sequences with byte counts of 1020 are issued to test setting of UE, IL and IOP/Halt. Seek/CC/Check-Write order is issued to check setting of TE.

4910 Controller not ready after Seek/CC/Write (or Check-Write) in Test Mode 2.

4911 Status error after Write order in Test Mode 2. UE, IL and IOP/Halt setting expected.

4912 Status error after Write order in Test Mode 2. IL and not UE and not IOP/Halt setting expected.

4913 Status error after Check-Write order in Test Mode 2. UE, TE and IOP/Halt setting expected.

TST1, 50 Test Mode 3 (Parity) - Read Order 12 Parity Test. A Sense/CC/Read 12 order sequence is issued with a Read byte count of 2048. The controller will generate a parity error. The test verifies the status (TE and not UE) and verifies with a Sense order that the Read order terminated after a sector. The remaining byte count must be = 1024.

5010 Controller not ready after Seek/CC/Read 12 order in Parity Test Mode.

5011 Remaining byte count after Read 12 order (2048 bytes) not equal to 1024. Read 12 operation did not terminate after one sector.

5012 Status error after Read 12 order. TE and not IL or UE expected. See Printout.

5013 Controller not ready after Sense order in Parity Test Mode.

5014 Status error in diagnostic Sense byte (byte 8 of Sense data) should indicate data parity error.

5015 Address received during Sense not correct. Head or Sector Address may have been incremented by two sectors.

TST1, 51 Test Mode 3 (Parity) - Read Order 02 Parity Test. A Sense/CC/Read 02 order sequence is issued with a Read byte count of 3072 (3 data-chain operation). The test verifies that Reading continues until the byte count = zero. The expected status is TE, not UE.

5110 Controller not ready after Seek/CC/Read02/DC/Read02/DC/Read02 in Parity Test Mode.

TST1, 51 (Continued)

5111 Status error after Read02 order. TE and not IL or UE and byte zero and Current Command Address Starting Address + 3 expected.
5112 Controller not ready after Sense order in Parity Test Mode.
5113 Address received during Sense not correct. Head or Sector Address did not increment correctly.

TST1, 52 Normal Mode - Restore Order Test. A Restore order is issued to the storage unit. The test verifies that the controller and device are ready and that positioning is complete and that no time out error has occurred.

5210 Controlled not ready after Restore order.
5211 On cylinder bit TDV (5) not received after Restore order.
5212 Status error after Device order. See printout.

TST1, 53 Normal Mode - Seek Order Test. A Restore order is issued to the storage unit. The test proceeds to issue Seek orders for all sectors on cylinder 0. No head motion is involved except possibly during the Restore order. The test verifies that Seek orders can be completed without errors.

5310 Controller not ready after Seek order.
5311 On-cylinder bit TDV (5) not received after Seek order. No head motion required.
5312 Status error after Seek order. See printout.

TST1, 54 Normal Mode - Release Order Test. A Release order is issued. The test verifies the status after the release.

5410 Controller not ready after Restore order in normal mode.
5411 Status error after Restore order in normal mode. Not UE, byte count 1 (no change) expected. See printout.

TST1, 55 Header Read - Failure Isolation Test. A Restore order is issued to position the heads at cylinder 0. Seek/CC/Header-Read sequences will be issued for all 120 sectors of cylinder 0. No errors will be reported until all operations are completed. A summary of all errors will be printed. The test will proceed to loop on the first failure with immediate error printouts. Information other than zeros in the flaw byte or alternate Address byte will not be considered an error.

5510 Controller not ready after Seek/CC/Header-Read order.
5511 Status error after Header-Read order. See printout.
5512 Compare error of Header data. Bytes 0, 5 and 6 of each Header are not tested.

TST1, 56 Normal Mode - Sense Order/Angular Position. A Restore order is issued to the storage unit. The test issues a Sense order and verifies the status. The test proceeds to issue up to 6 Sense orders in order to verify angular position 0. Following position 0, 5 Sense orders are issued to verify angular position 1-5.

5610 Controller not ready after Sense order.
5611 Status error after Sense order. See printout.
5612 Controller not ready after Sense order.
5613 Six attempts failed to find angular position of 0 in byte 4 of Sense data.
5621-5625 Controller not ready after Sense order. The least significant digit of the error number indicates the current angular position expected in the Sense data.
5631-5635 The expected angular position as indicated by the least significant digit of the error number not in byte 4 of Sense data.

TST1, 57 Normal Mode - Sense Order Test. A Restore order is issued to position the heads at cylinder 0. Seek/CC/Sense sequence will be issued for all 120 sectors of cylinder 0. The test verifies that the Address returned during the Sense operation is correct and that normal status is returned.

5710 Controller not ready after Sense order.
5711 Status error after Sense order. See printout.
5712 Compare error of Seek and Sense data. See printout.
5713 Status error in diagnostic Sense byte (byte 8 of Sense data) should indicate no errors.

TST1, 58 Sequential Head Positioning Test. Sequential Seek orders are issued to the disk storage unit. After verifying successful completion of each Seek order, a Sense order is issued to verify the Seek operation. If a Header parity error is detected during the Sense order, the Sense operation will be automatically retried six additional times before an error is reported. If the cylinder Address obtained is correct, the next Seek/Sense sequence will be initiated. On retries after a cylinder compare error, the Seek Address will be decremented by 1 (not 0) and a Restore order will be issued prior to retry.

5810 Controller not ready after a Seek order.
5811 Controller not ready after Sense order. Arm was in motion execution of Sense order.
5813 On cylinder bit TDV (5) not received after See order. The Seek order initiated head motion.
5814 Controller not ready after Sense order. Arm motion was previously completed. TDV(5) 1.
5815 All six Sense orders issued to the drive unit indicate that a Header parity error was detected.
5816 Compare error of Seek and Sense data. See printout.

TST1, 60 Complex Head Positioning, Seek Access Timing and Seek Complete Interrupt Test. This test consists of four passes. The passes differ by the type of head motion.

1. Seek (M) Sense Seek (N) Sense 406 times. M varies from 0 to 405, N is always 0.
2. Seek (M) Sense Seek (N) Sense 406 times. M is always 405. N varies from 405 to 0.
3. Seek (M) Sense Seek (N) Sense 406 times. M varies from 0 to 405, N varies from 405 to 0.
4. Seek (R) Sense Seek (R) Sense 406 times. R is a random number.

During retries the last successful Seek/Sense sequence is repeated. Average Seek access time is computed and if it exceeds the limit, it is printed out. The test is initialized if retry is requested.

6010 Controller not ready after Seek order.
6011 Expected Seek complete interrupt was not received.
6012 Status error after Seek complete interrupt has been received. See printout.
6013 Controller not ready after Sense order.
6014 Header parity error indicated by bit 7 of TDV following Sense orders. The Sense order has been issued seven times to automatically recover from the problem. Possible bad Headers on the disk.
6015 Head positioning error. See preceding printout. The expected Sense data defines the Seek Address. The observed Sense data defines the Current Address in the controller. Prior to the Seek operation.
6016 Average Head positioning time greater than 48 ms. All Seek operations in this test are used in the computation of the average time.

TST1, 63 Comprehensive Write/Read/Checkwrite Test. During the first phase of this test, attempts are made to locate a cylinder with error-free Headers. The cylinders used are determined by the SYST-directive entry for each device. Once a good cylinder has been located, A Write/Read/Checkwrite pass will be performed three times, each time with a different pattern.

Pass 1: Fixed pattern of X'AA55AA55'
Pass 2: Incremented pattern of X'00010203', X'04050607', X'08090A0B'
Pass 3: Current Seek Address X'00000000' for cyl 0, HD 0, Sect 0, X'00NN0803' for cyl NN, HD 08, Sect 3.

Any recoverable error six retries are automatically attempted) or solid failure will cause the selection of another cylinder. The objective of this procedure is to avoid looping on an error which may be caused by surface flaws.

**TST1, 63 (Continued)**

| | |
|---|---|
| 6310 | Attempts to find a cylinder (120 sectors) with good Headers and no assigned Alternate Addresses not successful. Program used only those cylinders which were made available to the program with the SYST directive. |
| 6311 | Controller not ready after Header Read order of 120 sectors. |
| 6312 | Byte count after Header Read order not reduced to zero. |
| 6313 | Status error after Header Read order. No unusual status expected. |
| 6314 | Header data compare error. See printout. If a flaw byte or an Alternate Address if dound in the Header, the current cylinder will not be used for the Write/Read/Checkwrite portion of this test. |
| 6315 | Header Read operation not successful for current cylinder. Errors 6311 through 6314 describe the nature of the failure. Next cylinder will be automatically selected. |
| 6320 | Controller not ready after Seek order. |
| 6321 | Controller not ready after Sense order. |
| 6322 | Seek/Sense compare error. See expected and observed data. The Sense order was issued after a Write, Read, or Checkwrite order. The Sense data should reflect the current Address. |
| 6330 | Controller not ready after Write order. Preceding Seek order successful. |
| 6331 | Status error after Write order. No unusual status expected. The Write order will be automatically retried six times. |
| 6332 | Status error after Write order. The diagnostic Sense byte (byte 8 of Sense data) should indicate no errors. |
| 6333-6335 | See 6330 through 6332, respectively. Current order was a Read. The sector in error may have been incorrectly written. |
| 6336 | Read compare error. See printout. The error may result from incorrect writing of the data. |
| 6337-6339 | See 6330 through 6332, respectively. Current order was a Checkwrite. The sector in error may have been incorrectly written if Read errors are detected. |
| 6340 | Write errors on current cylinder. If Sense Switch 1 is reset and 3 set, the Read and Check-Write portion of this test will be skipped and a new cylinder will be selected. Fixed pattern of X'AA55AA55AA5 . . . '. |
| 6341 | Read errors on current cylinder. If Sense Switch 1 is off and 3 on, the Checkwrite portion of this test will be skipped and a new cylinder will be selected. Fixed pattern of X'AA55AA55AA55. . .'. |
| 6342 | Checkwrite errors on current cylinder. If Sense Switch 1 is off and 3 on, a new cylinder will be selected. Fixed pattern of X'AA55AA55AA55. . . '. |
| 6343 | See 6340. Write errors. Incremented pattern X'00010203040506..' |
| 6344 | See 6341. Read errors. Incremented pattern X'00010203040506..' |
| 6345 | See 6342. Check-Write errors. Incremented pattern X'00010203040506 . . . '. |
| 6346 | See 6340. Write errors. Current Seek Address used as pattern. |
| 6347 | See 6341. Read errors. Current Seek Address used as pattern. |
| 6348 | See 6342. Check-Write errors. Current Seek Address used as pattern. |

**TST1, 64** Short Record Write Test. During the first phase of this test, attempts are made to locate a sector which can be recorded and verified. Once a good sector has been located, a 4 byte record is written and verified with a Read order. Bytes 4 through 1023 are expected to be zero.

| | |
|---|---|
| 6410 | Controller not ready after Seek/CC/Write order. |
| 6411 | Status error after Write order. Normal termination expected. |
| 6412 | Controller not ready after Seek/CC/Read order. |
| 6413 | Status error after Read order. Normal termination expected. |
| 6414 | Data compare error on current sector. |
| 6415 | Controller not ready after Seek/CC/Write order (4 bytes). The remaining bytes of the current sector should contain zeros. |
| 6416 | Status error after Write order (4 bytes). Only IL is expected. |
| 6417 | Controller not ready after Seek/CC/Read order (1024 bytes). The preceding Write order recorded only 4 bytes of data. |
| 6418 | Status error after Read order. Normal termination expected. |
| 6419 | Data compare error on current sector. If word count of compare error MSG> 0, the controller failed to write zeros for bytes 4 through 1023. |
| 6420 | Write or Read errors on current sector. Another sector, if available, will be selected. |
| 6430 | Device not ready after Seek/CC/Read (BC 253)/CC/Sense. |
| 6431 | Status error after Seek/CC/Read (BC 253)/CC/Sense. Normal termination expected. |
| 6432 | Device failed to report correct sector on sense at least once in 256 cycles of: Seek/CC/Read (BC 253)/CC/Sense. |

TST1, 65 Header Write Test. This test will only be executed if cylinder 405 is made available to the test program with the SYST directive. The test will write all Headers on cylinder 405 for Heads 16 through 19. The original Headers will be saved at the start of the test and restored at the end of the test.

| | |
|---|---|
| 6510 | Controller not ready after Seek/CC/Header Write order (6 sectors). |
| 6511 | Status error after Header Write order. Normal termination expected. |
| 6512 | Controller not ready after Seek/CC/Header Read order (6 sectors). |
| 6513 | Status error after Header Read order. Normal termination expected. Headers may have been incorrectly written. |
| 6514 | Header compare errors. Each Header consists of 8 bytes. Headers may have been incorrectly written. |
| 6515 | Controller not ready after Sense order. |
| 6516 | Status in diagnostic Sense byte (byte 8 Sense data) should indicate no errors. |
| 6517 | Attempts to save 24 Headers starting at cylinder 405, Head 16, Sector 0 not successful. Remainder of this test will be skipped. |

TST1, 66 Header Error Detection Test. This test will only be executed if cylinder 405 is made available to the test program with the SYST directive. The test consists of the following 3 sections:

1. Headers with flaw bytes are written for cylinder 405, Head 17 Sense, Header Read, and Read orders are issued to verify the detection of the flaw byte and setting of UE (UE will not be set during Header Read).
2. Headers with a cylinder address of 445 are written for cylinder 405, Head 18. A Sense order is issued to verify the setting of verification error, UE, and cylinder compare error (byte 8 of Sense data).
3. Headers for cylinder 405, Head 19 contain the following information: Sector 0 OK, Sector 1 OK, Sector 2 OK, Sector 3 cylinder wrong, Sector 4 Head wrong, Sector 5 sector wrong.
4. Header Read and Read orders are issued to verify that cylinder, head, and sector compare errors are set (byte 8 of Sense data) and that the orders terminate correctly after detection of an erroneous Header.

The original Headers will be saved at the start of the test and restored at the end of the test.

| | |
|---|---|
| 6610 | See 6517 |
| 6611 | Controller not ready after Seek/CC/Header Write order (24 sectors). |
| 6612 | Status error after Header Write order. Normal termination expected. |
| 6620 | Controller not ready after Seek/CC/Sense order. All six headers starting at cylinder 405, Head 17 have flaw bytes recorded from preceding Write Pass. |
| 6621 | Status error after Sense order. UE, flaw byte (TDV bit 1) and not TE expected. All six headers starting at cylinder 405, Head 17 have flaw bytes recorded from preceding Write Pass. |
| 6622 | Controller not ready after Seek/CC/Header Read order. See also 6620. |
| 6623 | Status error after Header Read order. Flaw byte, not UE or TE expected. See also 6621. |
| 6624 | Controller not ready after Seek/CC/Read order. See also 6620. |
| 6625 | Status error after Read order. UE, flaw byte (TDV·bit) and not TE expected. See also 6621. |
| 6626 | Controller not ready after Seek/CC/Sense order. All six headers starting at cylinder 405, Head 18 have a wrong cylinder Address (cylinder 455) recorded from preceding Write order. |
| 6627 | Status error after Sense order. UE, verification error (TDV bit 4) not UE, and byte count 0 expected. See 6626 for header data. |
| 6628 | Controller not ready after Seek order. |

TST1, 66 (Continued)

6629 Controller not ready after Sense order. Status after Sense order will not be tested.

6630 Controller not ready after Header Read order at cylinder 405, Head 19, Sector 3. Header of Sector 3 was previously written with wrong cylinder Address.

6631 Status error after Header Read order. UE, verification error, and byte count = 0 expected. See also 6630 for Seek Address and data.

6632 Status in diagnostic Sense byte (byte 8 of Sense data) should indicate cylinder compare error. See also 6630 for Seek Address and data.

6633 Controller not ready after Header Read order at cylinder 405, Head 19, Sector 4. Header of Sector 4 was previously written with wrong Head Address.

6634 Status error after Header Read order. UE, verification error, and byte count = 0 expected. See also 6653 for Seek Address and data.

6635 Status in diagnostic Sense byte (byte 8 of Sense data) should indicate Head compare error. See also 6633 for Seek Address and data.

6636 Controller not ready after Header Read order at cylinder 405, Head 19, Sector 5. Header of Sector 5 was previously written with wrong Sector Address.

6637 Status error after Header Read order. UE, verification error, and byte count = 0 expected. See also 6636 for Seek Address and data.

6638 Status in diagnostic Sense byte (byte 8 of Sense data) should indicate Sector compare error. See also 6636 for Seek Address and data.

6639 Controller not ready after Header Read order (17 bytes) at cylinder 405, Head 19, Sector 2. Header of Sector 2 OK, Header of Sector 3 was previously written with the wrong Cylinder Address.

6640 Status error after Header Read order (17 bytes). UE, verification error, and byte count = 1 expected. Headers for Sectors 2 and 3 should be read. See also 6639 for Seek Address and data.

6641 Status in diagnostic Sense byte (byte 8 of Sense data) should indicate cylinder compare error. See also 6639 for Seek Address and data.

6642 Controller not ready after Read order (1 byte) at cylinder 405, Head 19, Sector 3. Header of Sector 3 was previously written with wrong Cylinder Address.

6643 Status error after Read order. UE, verification error, byte count = 1 expected. See also 6642 for Seek Address and data.

6644 Status in diagnostic Sense byte (byte 8 of Sense data) should indicate Sector compare error. See also 6642 for Seek Address and data.

6645 Controller not ready after Read order (1025 bytes) at cylinder 405, Head 19, Sector 2. Header of Sector 2 OK, Header of Sector 3 was previously written with wrong Cylinder Address.

6646 Status error after Read order. UE, verification error, byte count = 1 expected. See also 6645 for Seek Address and data.

6647 Status in diagnostic Sense byte (byte 8 of Sense data) should indicate cylinder compare error. See also 6645 for Seek Address and data.

6648 Controller not ready after Read order (1 byte) at cylinder 405, Head 19, Sector 5. Header of Sector 5 was previously written with wrong Cylinder Address.

6649 Status error after Read order. UE, verification error, byte count = 1 expected. See also 6648 for Seek Address and data.

6650 Status in diagnostic Sense byte (byte 8 of Sense data) should indicate Sector compare error. See also 6648 for Seek Address or data.

6660 Controller not ready after Seek order (cylinder 405, Head 17, Sector 0)//CC//HD Read//CC//Seek (cylinder 405, Head 18, Sector 0)//Read.

6661 Status error. No UE, no flowmark, Command Address +3 expected.

TST1, 70 Dual Controller Test. An SIO order is sent to the first controller which will reserve the device until a Release order is issued. The second controller will now try to influence that device while the first controller is in both Busy and Ready state. After the test sequence is completed, the second controller is tested in the same way. Device Address must be entered with the SYST directive:

SYST, D1, X2, X3, X4, X5, X6, X7, X8, X9, X10
where each pair (X3, X5), (X7, X9), etc., must have the same device on different controllers. A minimum of 1 pair must be entered (maximum 4 pairs).

Example: SYST, 7270, 0, F0, 202, 1F0, 202
Or: SYST, 7270, 0, F0, 202, E0, 202

7010 Expected 2 or more Device Addresses entered by 'SYST' directive.

7011 Release order for device 2 not accepted. See printout.

7012 Release order for device 1 not accepted. See printout.

7013 SIO to device 1 not accepted. See printout.

7014 IO order to device 2 was accepted, should have been rejected. See printout.

7015 IO interrupt did not occur within time limit.

# Section 9

# SIGMA 5 - 9
# ROTATING MEMORY
# TEST (726X/7275)

## PROGRAM NO. 706249

## Section 9

## CONTENTS

Page

Subject Model . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 9-1
Required Equipment . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 9-1
Program Prerequisites . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 9-1
General Operating Procedures . . . . . . . . . . . . . . . . . . . . . . . . . 9-1
Directives . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 9-2
Start Procedure . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 9-5
Program Test Description . . . . . . . . . . . . . . . . . . . . . . . . . . . . 9-6
Order Codes . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 9-8
TDV Status . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 9-8
AIO Status . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 9-8
Test Mode Data Byte . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 9-9
Addressing Format . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 9-9
Functional Subtests . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 9-11

9

# 9. SIGMA 5–9 ROTATING MEMORY TEST (726X/7275)

**SUBJECT MODEL** -- Rotating Memory Devices with Removable Disk Storage System Model 726X and 7275 through 7277

**REQUIRED EQUIPMENT** -- Minimum Memory Size: 16K; Input Device: Card Reader, Paper Tape Reader, or Magnetic Tape Units; Output Device: Keyboard Printer or Line Printer.

## PROGRAM PREREQUISITES

Disk Packs with Prerecorded Headers Without Flowmarks and with alternate cylinder and head fields containing ones if the alternate address field is not used.

a. If a Disk Pack has flowmarks written in some of its headers, some subtests of the functional test will report errors. e.g.: Flowmark in sector zero of head zero and cylinder zero will make the subtests 70, 71, 73, 82, 83, 84, 86, 87, 88, 90, 93, 95 and 100 fail.

b. Using a Selector IOP might cause error printout in some subtests of the functional test for the 726X.

TST1, 98 and 99 are dual access tests and require explicit release mode.
TST1, 79, 87 89 and 90 cannot be interrupted. If interrupted, the original header at cylinder 202, head 0, sector 0 is lost.
TST1, 106 requires a CE Pack and the tester.

## GENERAL OPERATING PROCEDURES

General operating procedures of the Xerox Sigma 5 through 9 Diagnostic Program Monitor apply to this program.

**DIRECTIVES** – directives are entered after a "!" is typed out

| Name | Format | Parameter | | | |
|---|---|---|---|---|---|
| | | ID | Definition | Value Range | Standard Value (default) |
| Program Directives – Environmental Directives | | | | | |
| System Environment | SYST,D1,X2,D3,X4,<br>X5,,,X24 | D1 | Controller model number | 7260 or 7275 | |
| | | X2 | 0 | 0 | |
| | | D3 | Device type<br>5: Disk A: 203 Cyl, 20 Heads, 11 Sect/Track<br>7: Disk 33: 411 Cyl, 19 Heads, 11 Sect/Track | 5, 7 | |
| | | X4 | Description Device Number 1<br>Bit 0: IOP Type<br>0 Multiplexor<br>1 Selector<br>Bits 1-15: Device Address } Dual Access B<br>Bit 16: IOP Type<br>(same above)<br>Bits 17-31: Device Address } Dual Access A | | |
| | | X5<br>.<br>.<br>. | Description Device Number 2 | | |
| | | D(N) | Device type | 5, 7 | |
| | | X(NH) | Description Device Number 1 | | |
| Program Directives – Testing Directives | | | | | |
| Comprehensive Test (all functional tests, 1 ~ 99, and random exerciser test) | TST0 | | | | |
| Functional Test | TST1 [,D1[,D2[,D3,D4] | D1 | 1st Subtest | 1 ~ 106 | D1 1 |
| | | D2 | Last Subtest | D2 > D1 | D2 99 |
| | | D3 | Loop count | 1 ~ 999 | 1 |
| | | D4 | Message suppress mask | 0 - FFFF | 0 |
| Random Exerciser Test | TST2,D1,D2 | D1 | Number of I/O operations to perform | 1 ~ 65535 | |
| | | D2 | Retry count | 0 ~ 99 | |
| Utility Test | TST3,D1,D2,D3,D4 | D1 | 1 Surface Test | D2 0,1,2,3,4,5 | |
| | | | 2 Header Test | D2 0,1,2,3 | |
| | | | 3 Disk Pack Initialization and Flawing | D2 0 or alternate address in Hex to be assigned.<br>Bits 8-15 cylinder, bits 16-23 head, bits 24-31 0 | |
| | | D2 | 0 Write, Read and Verify<br>1 Write<br>2 Read and Verify<br>3 Read<br>4 Checkwrite<br>5 Write and Read | | |
| | | D3 | Retry count | 0 ~ 99 | |
| | | D4 | Read after Write count | 0 ~ 65535 | (TST3,1,0<br>TST3,1,5<br>TST3,2,0 only) |

**DIRECTIVES** - (Continued)

| Name | Format | Parameter | | | |
|---|---|---|---|---|---|
| | | ID | Definition | Value Range | Standard Value (default) |
| Program Directives - Optional Directives | | | | | |
| Pattern Selection | DATA,D1[,H2,D3] | D1 | Pattern type | 0,1,2,3 | D1 = 0 |
| | | D1 | 0, Fixed Pattern | | H2 = 0 |
| | | | H2 Pattern | 0~FFFFFFFF | D3 = 0 |
| | | | D3 0 | | |
| | | D1 | 1, Incrementing Pattern | | |
| | | | H2 Starting Pattern | 0~FFFFFFFF | |
| | | | D3 Increment | 0~FFFFFFFF | |
| | | D1 | 2, Random Pattern | | |
| | | | H2 Starting Seed | 0~FFFFFFFF | |
| | | | D3 0 | | |
| | | D1 | 3, Seek Address Fixed Pattern | | |
| | | | H2 0 | | |
| | | | D3 0 | | |
| Limitation Parameter | LIMT,D1,D2[,D3,H4] | D1 | 1, Limit the compare error printout to D2 lines. | | D2 = 5 |
| | | D1 | 2, Summary message, pass control | | |
| | | | D2 0 Inhibit cycle summary message(s). | | |
| | | | N Print pass summary message every N passes. | | D2 1, D3 1 |
| | | | D3 N Total number of passes to perform. | | |
| | | D1 | 3 | | |
| | | | D2 0 Reset | | |
| | | | 1 Display unconditional (Test 1 only) | | |
| | | | 2 Suppress constant part of messages. | | |
| | | | 4 Suppress stepping tests. | | D2 = 0 |
| | | D1 | 4 TST2,TST3 error message print/inhibit. | | H4 = X'FFFFFFFF' |
| | | | D2 0 | | |
| | | | D3 0 | | |
| | | | H4 32-bit message mask (Bit 0–Suppress; Bit 1–Print) | | |
| | | | Bit Message | | |
| | | | 0 TSTX IO Address XXXX | | |
| | | | 1 -------------------- | | |
| | | | 2 Time | | |
| | | | 3 (Test Description),NL,*** | | |
| | | | 4 Interrupt Not Expected | | |
| | | | 5 SIO Not Expected | | |
| | | | 6 Timeout | | |
| | | | 7 Status Error | | |
| | | | 8 Data Error | | |
| | | | 9 *** | | |
| | | | 10 ***Start of Operation*** | | |
| | | | 11 SIO Status | | |
| | | | 12 TDV Status | | |
| | | | 13 Start Time | | |
| | | | 14 Seek Address | | |
| | | | 15 Command Word Address | | |
| | | | 16 IOCD | | |
| | | | 17 *** | | |
| | | | 18 ***Status at End of Oper.*** | | |
| | | | 19 Interrupt Not Received | | |
| | | | 20 AIO Status | | |
| | | | 21 TIO Status | | |
| | | | 22 TDV Status | | |
| | | | 23 Current Command Doubleword | | |
| | | | 24 Remaining Byte Count | | |
| | | | 25 Status Correct | | |
| | | | 26 (Sense Data Avail. Flag) | | |
| | | | 27 Sense Data (W Issue) | | |
| | | | 28 *** | | |
| | | | 29 ***Data at End of Oper.*** | | |
| | | | 30 (Compare Data) | | |
| | | | 31 (System Status) | | |

**DIRECTIVES** - (Continued)

| Name | Format | Parameter | | | |
|---|---|---|---|---|---|
| | | ID | Definition | Value Range | Standard Value (default) |
| Memory Limitation for I/O Buffer | MEM,H1,H2 | H1<br>H2 | Starting Buffer Word Address<br>Ending Buffer Word Address | 0 ~ Mex Mem<br>H1 < H2 | Maximum available memory reset to default value. Set by SYST directive. |
| Surface Limitation | SEEK,D1,D2,D3,D4 | D1 | Starting Cylinder or Track | 0 ~ 202 (Disk A)<br>0 ~ 410 (Disk 33) | The Entire Surface |
| | | D2 | Starting Head or 0 | 0 ~ 19 (Disk A)<br>0 ~ 18 (Disk 33) | |
| | | D3 | Starting Sector | 0 ~ 10 | |
| | | D4 | Number of Sectors to be tested | 0 ~ 44660 (Disk A)<br>0 ~ 85899 (Disk 33) | |

## START PROCEDURE

1. Sense Switch Options, Monitor Directives Options, and Environmental Directives - Refer to DPM Manual No. 901649
2. Test Strategy Selections

| | Comprehensive Test | Functional Test | Random Exerciser | Utility Test |
|---|---|---|---|---|
| Recommended Application | Normal Usage | Solid Failure Detection and Specific Problem | Intermittent Failure Detection | Surface Test |
| Test Directive | TST0 | TST1 | TST2 | TST3 |
| Prerequisite | None | None | TST1 | TST1 |
| Optional Directives | SEEK, LIMT, MEM | LIMT, DATA (Test 104 Only) | SEEK, LIMT, MEM | SEEK, LIMT, MEM, DATA |
| Subtests | Functional test 1 ~ 99 and Random Exerciser | 106 subtests Four of them require operator intervention. See description. | 1. Surface Initialization<br>2. Random Exercising<br>3. Surface Verification | 1. Surface Test<br>2. Header Test (Disk Pack)<br>3. Disk Pack Initialization and Flawing |
| Error Message Format | Self-explanatory | Self-explanatory | Self-explanatory | Self-explanatory |

## PROGRAM TEST DESCRIPTION

The following is a description of the tests contained in the Rotating Memory Controller Test Program.

TST0 Comprehensive Test
This directive selects the functional test 1 ~ 99 and the random exerciser and executes them with reporting of Start and End of the tests.

Parameters: None

TST1 Functional Test
The functional test performs testing on one or more devices one device at a time.

Parameters:
- P1 Number of first subtest
- P2 Number of last subtest
- P3 Loop count
- P4 Message suppress flag

Default Values: For TST1: P1 1, P2 99, P3 1 and P4 0

The functional test consists of over 100 subtests. These subtests are arranged in a sequence in order to perform the basic functions first and then the more complex ones:

| Number | Subject of Test | Mode |
|---|---|---|
| 1– 5 | Basic IOP and cont. functions | Normal/test mode |
| 6– 9 | FAM buffer tests | Buffer test mode |
| 10– 64 | Controller functions | Contr./Incr. contr. TM |
| 65– 99 | Device and contr. functions | Normal/device test mode |
| 100–106 | Special tests with manual intervention | |

There are three ways of selecting these subtests with the directive 'TST1':

1. No Parameter, e.g., TST1 (Equal to TST1, 0, 0)
   All subtests from 1 to 99 are performed sequentially.
2. One Parameter, e.g., TST1, 15
   Only one subtest is performed.
3. Two Parameters, e.g., TST1, 10, 15
   The subtests from subtest parameter 1 to subtest parameter 2 are performed sequentially.

When the selected subtest(s) is (are) finished, the next device (according to SYST directive) will be tested. The subtests 1 to 64 are testing only controller functions. They are issued with the controller address 'XXXF'. No actual device is needed to perform these subtests. Yet a model number and a device address are to be inserted with the SYST directive. This determines the device type. According to this device type are the controller functions tested.

Print out will not occur, if the subtests run successfully and display mode was not selected. (Exception: subtests 101, 102, and 103, which need manual intervention)

The error printout is controlled by the sense switches and the limit-directive.

The interrupt and reset buttons on the CPU Control Panel should not be used to stop the execution of a subtest. The use of these buttons might cause errors in the next selected subtest because controller and device are not reset to the initial state.

Definition of the Sense Switches

| SSW 1 | 2 | 3 | 4 | Definition |
|---|---|---|---|---|
| X | X | X | 1 | Print inhibit |
| X | 0 | 0 | X | Wait after test sequence(if error)/sequence of subtests |
| 0 | 0 | 1 | X | Continue with next test sequence(if error)/return to DPM |
| 1 | 0 | 1 | X | Loop on test sequence(if error)/sequence of subtests |
| X | 1 | X | X | Loop on intermittent error |

A test sequence consists of one or more I/O instructions and tests on data. It is the smallest unit in the functional test on which looping and reporting is performed. A sequence of subtests consists of the subtests selected thru the parameters 1 and 2 of the TST1-directive.

Priorities of Looping and Printing Control

| Priority | Means of Control |
|---|---|
| | Printing |
| 1 | Sense switch 4: Print inhibit |
| 2 | Display directive: Print unconditionally |
| 3 | Print inhibit set by program |
| 4 | Print of errors |
| | Looping |
| 1 | Loop inhibit set by program |
| 2 | Sense switch 1, 2 and 3 in functional test driver |
| 3 | Loop count after subtest |
| 4 | Sense switch 1, 3 after subtest |

The third parameter (P3) of the TST1-directive specifies a loop count. It specifies how often a subtest shall be repeated, before the next subtest can be performed.

Default Value: 1 (0 is set equal 1)

The fourth parameter (P4) of the TST1-directive specifies a suppress flag. The suppress flag is a 16 bit mask written as a hexadecimal number. Each bit in this mask stands for one of 16 functional test subroutines:

| Bit | Mask | | |
|---|---|---|---|
| 0 | 8000 | T1APT | Pattern spread routine |
| 1 | 4000 | T1ATM | Test mode selection routine |
| 2 | 2000 | T1ASK | Seek routine |
| 3 | 1000 | T1AIS | Instruction sequence routine |
| 4 | 0800 | T1AEX | Execution routine |
| 5 | 0400 | T1AES1 | Escape routine 1 (special testing) |
| 6 | 0200 | T1ASIO | Start I/O routine |
| 7 | 0100 | T1AWT | Wait for IO completion routine |
| 8 | 0080 | T1AES2 | Escape routine 2 (special testing) |
| 9 | 0040 | T1AST | Stepping routine |
| 10 | 0020 | T1AIO1 | IO instruction routine 1 (TIO,TDV,HIO,AIO) |
| 11 | 0010 | T1AIO2 | IO instruction routine 2 (TIO,TDV,HIO,AIO) |
| 12 | 0008 | T1AIO3 | IO instruction routine 3 (TIO,TDV,HIO,AIO) |
| 13 | 0004 | T1ASN | Sense routine |
| 14 | 0002 | T1ACP | Compare routine |
| 15 | 0001 | T1AES3 | Escape routine 3 (special testing) |

If the corresponding bit is set, no report is made for this subroutine. If any bit is set, the heading with subtest number and IO address is suppressed also, e.g., 'FFFC' suppresses all but the printout of the compare routine and the escape routine. See error printout example for the use or parameters.

Default Value: 0

Some subtests are performed under certain conditions: Subtest 98 and 99 are only performed for a dual access configuration.

Different Modes to be used in TST1

Display Mode
In display mode a report is printed out after each execution of a test sequence, this mode is selected by the Limit directive.
e.g., LIMT,3,1 Sets display, LIMT,3,0 Resets display

Suppress Mode

In suppress mode all constant text is suppressed in the printout. Only the decimal, hexadecimal or binary numbers are printed. This mode is selected by the Limit directive.
e.g., LIMT,3,2 Sets suppress mode, LIMT,3,0 Resets

Suppress Stepping Tests

In this mode all tests using stepping mode are suppressed. This mode is selected by the LIMT directive.
E.G.: LIMT,3,4 sets suppress stepping tests
The selection of TST2 or TST3 also causes a suppression of these tests. The suppression by TST2 or TST3 selection cannot be reset, because the memory area containing the expected stepping data is used as buffer area for TST2 and TST3.

TST2 Random Exerciser
The random exerciser performs testing on one or more devices in a pseudo random manner. All devices are kept as busy as possible.

Parameters: P1 Number of I/O operations to perform
P2 Retry count

Example: TST2, 5000, 1
Perform the exerciser for 5000 operations.
Retry of errors: one

The exercising consists of three parts:
1. Surface Initialization – Random data is placed on all surface (or surface limited by seek directive).
2. Random Exercising – Individual and combinations (DC and CC) of operations are performed on randomly selected surfaces.
3. Surface Verification – Surface is read and data re-verified.

Flaw marks are acceptable (correct termination status is checked). Status or data errors cause operation to be repeated P2 times. Status errors inhibit checking of corresponding data. Exercising is controlled (in order of precedence) by:
1. Number of IO operations specified in TST2 directive.
2. Number of passes to perform specified in LIMT directive.
3. Looping controlled by sense switch 1.

All available memory is used unless limited by the MEM directive. However, a minimum of 1025 words are required for buffer area. The LIMT directive may be used to suppress all error message constants and/or suppress any portion of the error message.

TST3 Utility Tests
The utility tests consist of a set of tests to perform sequential surface and header testing and disk pack initialization/flawing.

Parameters: P1 = 1 Surface Test
  P2 = 0 Write, Read and Verify
  P2 1 Write
  P2 2 Read and Verify
  P2 3 Read (No Verify)
  P2 4 Checkwrite
  P2 = 5 Write and Read (No Verify)
P1 2 Header Test (Disk Pack Only)
  P2 0 Write, Read and Verify
  P2 1 Write
  P2 2 Read and Verify
  P2 = 3 Read
P1 3 Disk Pack Initialization and Flawing
  P2 0 or Alternate (in HEX) to be assigned (Bits 8–15 CYL; Bits 16–23 Head)
P3 = Retry Count (0 ≤ P3 ≤ 99)
  Default 0
P4 = Read after Write Count (TST3,1,0 and TST3,1,5 and TST3,2,0 Only)
  (0 ≤P4 65535)

Surface Testing – All surface is used unless limited by Seek directive. Status errors are retried a maximum of P3 times. Data errors with no accompanying status errors cannot be retried. Data used is specified by the data directive. Flaw marks are acceptable (correct termination status is checked).

Header Testing – All surface is used unless limited by Seek directive. Status errors are retried a maximum of P3 times. Header data errors (including flaw marks in header) with no accompanying status errors cannot be retried. Therefore flaw marks are reported as errors.

Disk Pack Init and Alternate Assignment Flawing – Initialization consists of one pass each: Write Header, Read Header, Write Data, Read Data. All surface is used unless limited by Seek directive. Data used is specified by Data directive. Header status errors cause premature termination of test. Surface errors are retried a maximum of P3 times. Failure after P3 retries causes all sectors of the failing track (CYL,HEAD) to be flawed (Flaw mark placed in headers of sectors 0 thru N). Flawing of more than 6 tracks (CYL,HEAD) causes premature test termination. No alternates are assigned.

Alternate assignment/flawing consists of writing of headers in sectors 0 thru N of the cylinder and head specified in the Seek directive. The headers written contain flaw marks and alternate CYL, head assignments specified by TST3 directive P2. Note that P2 non-zero selects the assignment/flawing operation. Therefore CYL 0, HEAD 0 cannot be used as alternates.

Speed of testing is a function of the type of data used. All available memory is used unless limited by the MEM directive. However, a minimum of 770 words are required for buffer area.

Testing is controlled (in order of precidence) by:
1. Number of sectors specified
2. Read after Write count specified by TST3 directive P4 (TST3,1,0 and TST3,1,5 and TST3,2,0 only)
3. Number of passes to perform specified in LIMT directive.
4. Looping controlled by sense switch 1.

Example: Sense Switch 1 = 0
LIMT,2,1,2 Entered
SEEK,0,0,0,220 Entered
DATA,2, 12345678
TST3,1,0,4,50 Entered

Result: All sectors of cylinder 0 are written with random data, then all sectors of cylinder 0 are read and data is verified, then all sectors of cylinder 0 are read and verified 50 additional times, then all above is repeated once again (since LIMT directive pass count set to 2). All status errors result in operation retries not to exceed 4.

The LIMT directive may be used to suppress all error message constants and/or suppress any portion of the error messages.

A particular random pattern found failing on particular sector(s) during the random exercising may be used during the surface test by limiting the surface with the Seek directive and specifying Data,2,P2 directive with P2 equal to the value of the "Base Seed" printed in the error message of TST2.

# 9. SIGMA 5–9 ROTATING MEMORY TEST (726X/7275)

## ORDER CODES

| | |
|---|---|
| X'01' | WRITE |
| X'02' | READ 2 |
| X'03' | SEEK |
| X'04' | SENSE |
| X'05' | CHECKWRITE |
| X'07' | RESERVE |
| X'09' | HEADER WRITE |
| X'0A' | HEADER READ |
| X'0F' | CONDITION RELEASE INTERRUPT |
| X'12' | READ 1 |
| X'13' | SELECT TEST MODE (See Test Mode Data Bytes) |
| X'1F' | CONDITION RELEASE INTERRUPT (and Set a CIL on Device Release) |
| X'17' | RELEASE |
| X'33' | RESTORE CARRIAGE |
| X'83' | SEEK (and Cause a Device Interrupt on Positioning Complete or SEEK Timeout Error) |
| X'B3' | RESTORE CARRIAGE (and cause a Device Interrupt on Positioning Complete) |

## TDV STATUS

| MODEL | BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| RMC | Not Assigned | Flaw Detection | Programming Error | Write Protect Violation | Parity Error (IOP) | Operational Error | Verification Error | Header Parity Error |

## AIO STATUS

| MODEL | BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| RMC | Rate Error (Data overrun) | Attention Interrupt | Release Interrupt | Not Assigned | On-Sector Interrupt | Not Assigned | Seek Timeout Error Interrupt | Not Assigned |

DETAILED DESCRIPTION OF TDV STATUS

| Bit Position | Function | Value | |
|---|---|---|---|
| | | | TDV Bit 1 -- Flaw Detection |
| 1 | | 1 | Flaw byte detected during Header Read, Write, Read, or Checkwrite |
| | | | TDV Bit 2 -- Programming Error |
| 2 | | 1 | Invalid order detected; or illegal address (address X'F' used for orders other than Select Test Mode or Conditional Release Interrupt); or invalid Seek address; or address incremented out of limits while attempting a Read or Write order; or invalid test mode; or Seek order received while arm was in motion; or first seven bits of Seek order were not zero; or incorrect length detected for Seek, Sense, Header Read, or Header Write order. |
| | | | TDV Bit 3 -- Write Protect Violation |
| | | | Write-protect violation |
| | | | TDV Bit 4 -- Parity Error (IOP) |
| | | | Order parity error detected; or Seek address parity error detected; or even parity received on a terminal order; or IOP detected an address parity error (channel address parity error). |
| | | | TDV Bit 5 -- Operational Error |
| | | | Device interface error detected; or missing an on-sector signal from device during a multi-sector Read or Write; or missing Read or Write clock, command strobe, or status request acknowledgement from the device; or detection of Seek address transfer verification comparison error during Seek, Read, or Write; or device unavailable error, or "not operational" signal detected from device by the controller, or a seek error during a Read or Write. |
| | | | TDV Bit 6 -- Verification Error |
| 6 | Verification | 1 | Head address verification error detected; or sector address verification error detected; or cylinder address verification error detected. |
| | | | TDV Bit 7 -- Header Parity Error |
| 7 | Header check byte | 1 | Header check byte error |

## TEST MODE DATA BYTE

Test mode order puts the controller in test mode and requests two data bytes from the IOP.

| | |
|---|---|
| 1st Data Byte | Test Mode |
| 2nd Data Byte | Device type or diagnostic conditions |

1st DATA BYTE

| Bits | Meaning |
|---|---|
| When Set | |
| 7 | Buffer Test Mode |
| 6 | Controller Test Mode |
| 5 | Device Test Mode |
| 4 | Incremental Clock Test Mode |
| 3 | Force Device I/O Parity Error |
| 2 | Force Read Data Error |
| 1 | Force IOP Input Parity Error |
| 0 | Force IOP Output Parity Error |

(Bits 0–7 0 Invalid Test Order)

2nd DATA BYTE

| Bits | Meaning |
|---|---|
| 0–7 | Diagnostic Test Conditions for the Device<br>(In Device Test Mode only) |
| 5–7 | Device Type Code<br>(In Controller Test Mode only)<br>X'5' = Disk Drive A<br>X'7' = Disk 33 |

## ADDRESSING FORMAT

1. The format of the four bytes seek address is:

| Byte 0 | Byte 1 | Byte 2 | Byte 3 |
|---|---|---|---|
| ◄—— Cylinder | ——► | Head | Sector |

Description of Parameters:
Cylinder 0 ~ 202 (Disk Drive A)
0 ~ 411 (Disk Drive 33)
Head 0 ~ 19 (Disk Drive A)
0 ~ 18 (Disk Drive 33)
Sector = 0 ~ 10

2. The format of the sixteen bytes of information to be received by the IOP when a sense order is issued is:

Byte 0 Byte 1 Byte 2 Byte 3

| | | | | | | |
|---|---|---|---|---|---|---|
| W | 0 0 0 0 0 0 | ◄— Cylinder —► | 0 0 0 | Head | 0 0 0 | Sector |
| 0 | 1 2 3 4 5 6 | 7 0 7 | 0 1 2 | 3 7 | 0 1 2 | 3 7 |

Byte 4 Byte 5 Byte 6 Byte 7

| | | | | | |
|---|---|---|---|---|---|
| M | R | Angular Position | Configuration | Device Status | 0 ——— 0 |
| 0 | 1 | 2 7 | 0 7 | 0 7 | 0 7 |

| Byte 8 | Byte 9 | Byte 10 | Byte 11 |
|---|---|---|---|
| Faults | Faults | Seek Modifier Bits | |
| 0 7 | 0 7 | 0 7 | 8 15 |

| Byte 12 | Byte 13 | Byte 14 | Byte 15 |
|---|---|---|---|
| Check Bytes | | Difference | |
| 0 | 15 | 0 | 15 |

These four words describe the controllers current state.

Description of Parameters:
W Write Protect Bit.
If set, current address is Write Protected.
Cylinder 9-Bit Cylinder Address
Head Head Address
Sector Sector Address
M Modifier Bit.
If set, arm is in motion and file inaccesible.

R Reserve/Release Mode.
If set: Implicit reserve, explicit release in effect
If reset: Implicit reserve and release in effect
Angular Position: A Sector Number.
When this equal to sector address, file is accessible.
Configuration Bit 0 (Set) = Addressed device has the dual access feature.
Bits 1–3 Device Type
X'5' Disk Drive A
X'7' = Disk Drive 33
Bits 4–7 Device Physical Address
Device Status Status Received
Faults Diagnostic Fault Data. Resulted from 'Transmission Errors' and 'Unusual End' terminations. They are as follows:

Byte 8

| Bit 0 | Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7 |
|---|---|---|---|---|---|---|---|
| Check Write Error | Data Check Byte Error | IOP Parity Error | Rate Error (Data Over-run) | Head Address Incre-mented Out of Limits | Arm in Motion Error | Order Parity Error | Test Mode Order Error |

Byte 9

| Bit 0 | Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7 |
|---|---|---|---|---|---|---|---|
| Seek Address Trans-fer Error | Device Error | Head Address Verifi-cation Error | Sector Address Verifi-cation Error | Cyl. Address Verifi-cation Error | Unas-signed | Channel Address Error | Read/ Write Error |

Seek Modifier Bits Seek/Restore Carriage Modifier Bits.
Bit 0 Device Address 0
Bit 14 Device Address X'E'
A "One" set in any bit position means an interrupt is pending or seek timeout.
Checkbytes Last check bytes received by controller.
Difference Difference last computed by controller during a seek order execution.
Least Sig. Bit Bit 15
Most Sig. Bit Bit 7

## ADDRESSING FORMAT (Continued)

3. The format of the eight bytes header size is:

| Byte 0 | Byte 1 | Byte 2 | Byte 3 |
|---|---|---|---|
| Flow | ◄——— Cylinder ———► | | Head |
| 0 7 | | | |

| Byte 4 | Byte 5 | Byte 6 | Byte 7 |
|---|---|---|---|
| Sector | Alternate Cylinder | Alternate Head | 0 ——— 0 |

Description of Parameters:

| | |
|---|---|
| Flow | Flow Byte. This is written X'FF' in every sector header of a track in which a flaw is detected. If no flaws, the flaw byte is all zeros. |
| Cylinder | Current Cylinder Address. |
| Head | Current Head Address. |
| Sector | Current Sector Address. |
| Alternate Cylinder | Address of an alternate cylinder should this sector be flawed, otherwise it is all ones. |
| Alternate Head | Address of alternate head should this sector be flawed. Otherwise it is all ones. |

## FUNCTIONAL SUBTESTS

### FUNCTIONAL SUBTESTS - DESCRIPTION

#### TST1,01 HIO, TIO, TDV Recognition Test

Mode: Normal Mode

HIO, TIO and TDV instructions are issued. I/O address recognition and normal status expected. This subtest and the subtest 02 to subtest 64 are using a modified device address to select only the controller. The least significant 4 bits are set to X'F'.

#### TST1,02 Invalid Order Test

Mode: Normal Mode

SIO instructions are issued with all valid orders except test mode selection order and condition release interrupt order. With device address 'F' these orders are terminated as invalid orders with TIO bit 4 and TDV bit 2 set. The byte count is 1. It is expected that the byte count is not changed.

An Hio is used to reset the TIO/TDV status. The reset is verified with another TIO/TDV.
Test Variations:
1. Check of TIO status
2. Check of TDV status

#### TST1,03 Test Mode Selection Test

Mode: Buffer/Controller/Device Test Mode

Test mode selection orders are issued with the bytes X'01', X'02', and X'04' in order to switch the controller in buffer-, controller-, and device-test mode. Set and reset of the test mode indication is verified by a sequence of TDV, HIO and TDV instructions.
Test Variations:
1. First Testmode Byte = 01
2. First Testmode Byte = 02
3. First Testmode Byte = 04

#### TST1,04 Interrupt Generation Test

Mode: Normal Mode

Test mode selection orders are issued with 1 Byte equal zero. Therefore unusual end is always expected. The interrupt flags are set to test interrupts on unusual end, channel end and zero byte count. In three passes, the following conditions are tested:
Test Variations:
1. Interrupt disarmed, reset in int. pend. by HIO
2. Interrupt disarmed, reset of int. pend. by AIO
3. Interrupt armed, reset of int. pend. by AIO, another AIO is issued to check for no int. recogn.

#### TST1,05 Command Chaining Test

Mode: Normal Mode

Two test mode selection orders are issued command chained.
Test Variations:
1. Testmode Byte = 0, no CC expected
2. Testmode Byte = 1, CC expected

TIO and TDV instructions are used to verify the correct execution.

#### TST1,06 FAM Write/Read: Byte Count Test

Mode: Buffer Test Mode

Write and Read orders are issued. The byte counts 1 thru 32 are used. Final byte count of zero is expected. A TIO instruction is used to verify the correct execution.

#### TST1,07 FAM Write/Read: Interface Test

Mode: Buffer Test Mode

Write and Read orders are issued to test the byte alignment logic of the controller.
Test Variations:
1. 4 IOCDS (2 Write,BC=2 and 2 Read,BC=2)
2. 3 IOCDS (2 Write,BC=2 and 1 Read,BC=4)
3. 3 IOCDS (1 Write,BC=4 and 2 Read,BC=2)
4. 2 IOCDS (1 Write,BC=4 and 1 Read,BC=4)

A TIO instruction is used to verify the correct execution. The observed data are compared with the expected data.

Four passes are executed with the data: X'010203041', X'F1F2F3F4', X'1F2F3F4F'. X'A55AC33C'

#### TST1,08 FAM Write/Read: Byte Alignment Test

Mode: Buffer Test Mode

Write and Read orders are issued with byte counts equal 13 to test the byte alignment logic of the controller and the IOP.

The 4 byte alignment cases are exercised in 4 passes. Before each pass the 1st and the 4th words of the Read Data Buffer are filled with the pattern X'FFFFFFFF'. A TIO instruction is used to verify the correct execution. The observed data are compared with the expected data.

#### TST1,09 FAM Write/Read: Random Data Test

Mode: Buffer Test Mode

A Write order command chained to a read order is issued. The byte count is 32.

A TIO instruction is used to verify the correct execution. The observed data are compared with the expected data.

The test sequence is repeated 100 times with random data.

#### TST1,14 Sense Test

Mode: Incremental Controller Test Mode

A Sense order is issued. TDV instructions are used to increment the controller clock and to collect data from the following modules of the controller: Phase Register, Byte Count Register, Device Command Register and Data Bus.

Phase Data, Byte count data and device command data are verified by comparison with expected data. Bus data are not checked.

#### TST1,15 Sense Test

Mode: Controller Test Mode
Test Variations:
1. Sense orders are issued with byte counts 1 thru 16. TIO and TDV instructions are used to verify the correct execution.
2. A Sense order is issued. Controller fault bits and interrupt modifier bits are checked for zeros.

#### TST1,16 Condition Release Interrupt Test

Mode: Controller Test Mode

A condition release interrupt order is issued. TIO and TDV instructions and a sense order are used to verify the correct execution of the order.

### TST1,17 Release Test

Mode: Controller Test Mode

A Release order is issued. TIO and TDV instructions and a Sense order are used to verify the correct execution of the order.

### TST1,18 Restore Test

Mode: Incremental Controller Test Mode

A Restore order is issued. TDV instructions are used to increment the controller clock and to collect data from the following modules of the controller: Phase Register, Byte Count Register, Device Command Register and Data Bus. Phase data, byte count data, device command data and data bus data are verified by comparison with expected data.

### TST1,19 Restore Test

Mode: Controller Test Mode

A Restore order is issued. TIO and TDV instructions and a Sense order are used to verify the correct execution of the order.

### TST1,20 Seek Test

Mode: Incremental Controller Test Mode

A Seek order is issued. The Seek address consists of the pattern X'FFFFAA00'. TDV instructions are used to increment the controller clock and to collect data from the following modules of the controller: Phase Register, Byte Count Register, Device Command Register and Data Bus. Phase data, byte count data, device command data and data bus data are verified by comparison with expected data.

### TST1,21 Seek Test

Mode: Controller Test Mode

A Seek order is issued. The Seek address is Cylinder - 0, Head - 0, Sector - 0. TIO and TDV instructions and a Sense order are used to verify the correct execution of the order.

### TST1,24 Seek: Incorrect Length Test

Mode: Controller Test Mode

Seek orders are issued. The Seek address is 0/0/0. Incorrect length is checked with the byte counts of 1,2,3 and 5. TIO and TDV instructions and a Sense order are used to verify the correct execution of the order.

### TST1,25 Seek: Incorrect Address Test

Mode: Controller Test Mode
Seek orders are issued. The Seek address is always incorrect.
Test Variations:

1. Incorrect Sector Address
2. Incorrect Head Address
3. Incorrect Cylinder Address

TIO and TDV instructions and a Sense order are used to verify the correct execution of the order.

### TST1,26 Seek: Difference Test

Mode: Controller Test Mode
Two Seek orders are issued. The Seek address of the first Seek order is constant: Cylinder 0, Head 0, Sector 0. The Seek address of the second Seek order is changing the Cylinder address from 0 to N, Head 0 and Sector 0. TIO and TDV instructions and a Sense order are used to verify the correct execution of the order.
N 202 for Disk A
N 410 for Disk 33

### TST1,27 Seek: Device Interface Error Test

Mode: Controller Test Mode

Seek orders are issued in controller testmode with Seek addresses different from zero. Sense orders are issued to verify that address transfer error is set (Sense byte 9, bit 0).
Test Variations:

1. Cylinder Address 1
2. Head Address 1
3. Sector Address 1

### TST1,28 Seek: Address Buffer Test

Mode: Controller Test Mode

Seek orders are issued with all device addresses and the Seek address consisting of the following patterns:
Disk: X'00000F07' and X'00001008'
RAD: X'01FF000B' and X'01AA0007'
Sense orders are issued to read these addresses back for verification.

### TST1,29 IOP Device Address Parity Error Test

Mode: Controller Test Mode
Sigma 9 Only
Test Variations:

1. The test mode selection order is set to force a device parity error during ASC. The parity of forced to '1'. Therefore, all addresses with odd parity will result in a parity error.
2. The test mode selection order is set to force a device parity error for I/O instructions. If the device is in the busy state, the parity line is forced to a '0'. Therefore, all addresses with even parity will result in parity errors.

### TST1,32 Header Write Test

Mode: Incremental Controller Test Mode

A Header Write order is issued. TDV instructions are used to increment the controller clock and to collect data from the following modules of the controller: Phase Register, Byte Count Register, Device Command Register and Data Bus. Phase data, byte count data, device command data and data bus data are verified by comparison with expected data.

### TST1,33 Header Write Test

Mode: Controller Test Mode

A Header Write order is issued. The byte count is 8. TIO and TDV instructions and a sense order are used to verify the correct execution of the order.

### TST1,34 Header Read Test

Mode: Incremental Controller Test Mode

A Header Read order is issued. TDV instructions are used to increment the controller clock and to collect data from the following modules of the controller: Phase Register, Byte Count Register, Device Command Register and Data Bus. Phase data, byte count data, device command data and data bus data are verified by comparison with expected data.

### TST1,35 Header Read Test

Mode: Controller Test Mode

A Header Read order is issued. The byte count is 8. TIO and TDV instructions and a Sense order are used to verify the correct execution of the order. The Header data are verified. All data in controller test mode consist of the repetitive pattern X'803FD56A'.

### TST1,36 Read Test

Mode: Incremental Controller Test Mode

A Read order is issued. TDV instructions are used to increment the controller clock and to collect data from the following modules of the controller: Phase Register, Byte Count Register, Device Command Register and Data Bus. Phase data, byte count data, device command data and data bus data are verified by comparison with expected data.

### TST1,37 Read Test

Mode: Controller Test Mode

A Read order is issued. The byte count is 1024. TIO and TDV instructions and a Sense order are used to verify the correct execution of the order. The Read data are compared with the expected data.

### TST1,38 Write Test

Mode: Incremental Controller Test Mode

A Write order is issued. TDV instructions are used to increment the controller clock and to collect data from the following modules of the controller: Phase Register, Byte Count Register, Device Command Register and Data Bus. Phase data, byte count data, device command data and data bus data are verified by comparison with expected data.

### TST1,39 Write Test

Mode: Controller Test Mode

A Write order is issued. The byte count is 1024. TIO and TDV instructions and a Sense order are used to verify the correct execution of the order.

### TST1,40 Check Write Test

Mode: Incremental Controller Test Mode

A Check Write order is issued. TDV instructions are used to increment the controller clock and to collect data from the following modules of the controller: Phase Register, Byte Count Register, Device Command Register and Data Bus. Phase data, byte count data, device command data and data bus data are verified by comparison with expected data.

### TST1,41 Check Write Test

Mode: Controller Test Mode

A Check Write order is issued. The byte count is 1024. TIO and TDV instructions and a Sense order are used to verify the correct execution of the order.

### TST1,42 Short Record Test

Mode: Controller Test Mode

Read, Write and Check Write orders are issued. The byte counts are 2. TIO and TDV instructions and a Sense order are used to verify the correct execution of the order. The Read data are compared with the expected data.

### TST1,43 Checkwrite Error Test

Mode: Controller Test Mode

A Check Write order is issued. The byte count is 1024.
Test Variations:
1. Checkwrite error in 1st byte
2. Checkwrite error in 1024th byte
TIO and TDV instructions and a Sense order are used to verify the correct execution of the order.

### TST1,45 Header Write,...: Incorrect Length Test

Mode: Controller Test Mode

Header Write and Header Read orders are issued. Incorrect length is checked with the byte counts of 6,7,9 and 10. TIO and TDV instructions and a Sense order are used to verify the correct execution of the order.

### TST1,46 Write,...: Incorrect Length Test

Mode: Controller Test Mode

Write, Check Write and Read orders are issued. The byte counts are number of bytes per sector plus -2, -1, +1, +2. TIO and TDV instructions and a Sense order are used to verify the correct execution of the order.

### TST1,47 IOP Halt Test

Mode: Controller Test Mode

Write, Check Write and Read orders are issued command chained to a double transfer in channel. An IOP halt is forced during the execution of the orders by the double transfer in channel. TIO and TDV instructions and a Sense order are used to verify the correct execution of the order. The test is repeated with the byte counts of 512, 256, 128, 64, 32, 16, 8 and 4.

### TST1,48 HIO Halt Test

Mode: Controller Test Mode

Write, Check Write and Read orders are issued. An HIO is issued during the execution of the orders. TIO and TDV instructions are used to verify the correct termination.

### TST1,49 IOP Output Parity Error Test

Mode: Controller Test Mode

The test mode selection order is set to force IOP output parity errors: in five passes the following subjects are tested:
Test Variations:
1. Failure in Order Out, Seek Order X'03' (Sigma 9 Only)
2. Failure in Data Out, Seek Order X'83'
3. Failure in Data Out, Write Order
4. Failure in Data Out, Write Order (Sigma 9 Only)
5. Failure in Terminal Order, Read Order (Sigma 9 Only)

### TST1,50 IOP Input Parity Error Test

Mode: Controller Test Mode

The test mode selection order is set to force IOP input parity errors.
1. Read order is issued with a byte count of 1024.
2. Write order is issued with a byte count of 1023. (Sigma 9 Only)
TIO and TDV instructions and a Sense order are used to verify the correct execution of the order.

### TST1,51 Rate Error Test

Mode: Controller Test Mode

Write, Check Write and Read orders are issued with a byte count of 1 and data chaining. The continuous data chaining and transfer in channel slow the IOP down in its byte transfer rate to cause rate error. TIO and TDV instructions and a Sense order are used to verify the correct execution of the order.

TST1,53 Interrupt Modifier Bit Test

Mode: Controller Test Mode

The interrupt modifier bit test verifies the correct setting of the Seek modifier bits on Seek orders X'83' or Restore orders X'B3' (Disk Only) and the correct resetting by AIO's for all device addresses. This test also verifies for all device addresses:

1. The generation of interrupt pending
2. The rejection of SIO's to addresses with interrupt pending
3. The execution of SIO's while interrupts are pending for other addresses.

TST1,54 Write, ...: Address Incrementing

Mode: Controller Test Mode

Write, Check Write, Read, Header Write and Header Read orders are issued to check the address incrementing. TIO and TDV instructions and a Sense order are issued to verify the correct execution. The Seek address is varied in two passes:
Test Variations:

1. Cyl/Head/Sect - 0/0/0
2. Cyl/Head/Sect - 0/0/9

TST1,56 Write,...: Address Boundary Test

Mode: Controller Test Mode

Write, Check Write, Read, Header Write and Header Read orders are issued to check the boundary. TIO and TDV instructions and a Sense order are issued to verify the correct execution. The byte count is 1024.
Test Variations:

1. The Seek address is set to Write,... at the last sector of Cyl. 0
2. Another Write,... order is issued without a previous Seek order.

TST1,57 Controller Busy Test

Mode: Controller Test Mode

A Read order is issued with the device address 'F'. During the execution of this order SIO, TIO, TDV and HIO instructions are issued with device addresses 0 to E.

TST1,65 Invalid Order Test

Mode: Normal Mode

SIO instructions with invalid orders are issued. All invalid orders are used.
Test Variations:
1st Test of TIO status
2nd Test of TDV status

TST1,66 Sense Test

Mode: Incremental Device Test Mode

TDV instructions are used to increment the controller clock and to collect data from the following modules of the controller: Phase Register, Byte Count Register, Device Command Register and Data Bus. Phase data, byte count data and device command data are verified by comparison with expected data. Bus data are not checked.

TST1,67 Sense Order and Angular Position Test

Mode: Normal Mode

Sense orders are issued. TIO and TDV instructions are issued to verify the correct execution. All Sense data are verified, except byte 5, bit 0 (Dual Access Configuration Flag), byte 5, bit 4-7 (Hardware Device Address) and byte 12 and 15.
Test Variations:

1. A maximum of 11 Sense orders are issued to find sector zero.
2. With 10 Sense orders, angular position 1 thru 10 is checked.

TST1,68 Seek Test

Mode: Incremental Device Test Mode

A Seek order is issued. The Seek address consists of the pattern X'00CA1309'. TDV instructions are used to increment the controller clock and to collect data from the following modules of the controller: Phase Register, Byte Count Register, Device Command Register and Data Bus. Phase data, byte count data and device command data are verified by comparison with expected data. Bus data are not checked.

TST1,69 Seek Test

Mode: Normal Mode

Seek orders are issued. TIO and TDV instructions and a Sense order are issued to verify the correct execution.
Test Variations:

1. Seek address: Sector 0 thru 10
2. Seek address: Head 0 thru 19 (Disk A)
   0 thru 18 (Disk 33)

TST1,70 Header Read Test

Mode: Normal Mode

The sequence of orders Seek - Header Read is issued. TIO and TDV instructions and a Sense order are issued to verify the correct execution. The byte count is 8. The Header data are expected to be zero. The data buffer for observed data (Buffer B) is filled with the pattern X'FFFFFFFF', X'FF0000FF'.

TST1,71 Write, Check Write and Read Test

Mode: Normal Mode

The sequences of orders Seek - Write, Seek - Check Write, and Seek - Read are issued. TIO and TDV instructions and a Sense order are issued to verify the correct execution.
Test Variations:

1. Write order
2. Check Write order
3. Read order

The byte count is 1024. The Read data are compared with the expected data.

TST1,72 Reserve and Release Test

Mode: Normal Mode

1. A SIO instruction is issued with a reserve order. TIO and TDV instructions are used to verify the correct execution.
2. A SIO instruction is issued with a release order. TIO and TDV instructions are used to verify the correct execution.

No operation is expected by these orders.

TST1,73 Matrix Test

Mode: Normal Mode

The matrix test is supposed to check all heads and to print errors in the form of a matrix.

Header Read orders are issued to all heads. The errors unusual end, verification error, flaw mark and the observed header data are printed out for each faulty head.
e.g.:

```
         UE V  F  HEADER DATA
Head 001  1 1  1  FF00  0001  0000  0000
```

TST1,74 Restore and Seek Test

Mode: Normal Mode

Restore and Seek orders are issued. TIO and TDV instructions and a Sense order are issued to verify the correct execution. The Seek address is Cyl N, Head 0, Sector 0. Test Variations:

1. Restore order
2. Seek order
3. Restore order
4. Seek order /CC/ Restore order

Address and difference of Sense are tested.
N 202 for Disk A
N 410 for Disk B

TST1,75 Seek Order: Interrupt Test

Mode: Normal Mode

Seek orders are issued. (Seek with interrupt on Sector Flag.) TIO and TDV instructions and a Sense order are issued to verify the correct execution. Test Variations:

1. Check for interrupt
2. Check for withdrawal of interrupt during one revolution

TST1,76 Restore Order: Interrupt Test

Mode: Normal Mode

Restore orders are issued. (Restore with interrupt on Sector.) TIO and TDV instructions and a Sense order are issued to verify the correct execution. Test Variations:

1. Check for interrupt
2. Check for withdrawal of interrupt during one revolution

TST1,77 Seek Order: Head Moving Test

Mode: Normal Mode

Seek orders with command chained Sense orders are issued. TIO and TDV instructions are issued to verify the correct execution. The Cylinder address is incremented from 0 to N and then decremented from N to 0. Head and Sector address are zero. Byte 4 Bit 0 of the Sense data is checked (Head in motion bit).
N 202 for Disk A
N - 410 for Disk B

TST1,78 Seek Order: Head Positioning Test

Mode: Normal Mode

Seek orders are issued. (Seek Interrupt Flag.) TIO and TDV instructions are issued to verify the correct execution. Header Read orders are issued to verify the Seek position. Two Seek addresses are used in sequence. These two addresses Addr. 1 and Addr. 2 are va varying the Cylinder address part in four passes. The Head and Sector parts of the addresses are zero. Test Variations:

1. Addr. 1 is increm. from 0 to N, Addr. 2 0
2. Addr. 1 is decrem. from N to 0, Addr. 2 N
3. Addr. 1 is increm. and Addr. 2 is decremented
4. Random addresses for Addr. 1 and Addr. 2 (N+1 times).

After each pass the average access time is computed. An average access time greater than M mSec is an error which causes a printout.

| | |
|---|---|
| N = 202 for Disk A | M = 57 msec (Disk A) |
| N = 410 for Disk 33 | M = 48 msec (Disk 33) |

TST1,79 Header Write and Header Read Test

Mode: Normal Mode

The sequences of orders Seek – Header Read and Seek – Header Write are issued. TIO and TDV instructions and a Sense order are issued to verify the correct execution. The Seek address is Cyl 202, Head 0, Sector = 0. The byte count is 8. Test Variations:

1. Header Write: Data = 0, 0, 202, 0, 0, X'FFFF00'
2. Header Read with compare
3. Header Write: Data 0,0,202,0,0,0,0,0
4. Header Read with compare

TST1,82 Write Order: Multiple Sector Write Test

Mode: Normal Mode

Write orders are issued to Write all sectors of Cyl. 0. TIO and TDV instructions and a Sense order are issued to verify the correct execution. The byte count is 1024. The Write order is repeated by using data chaining and transfer in channel until an interrupt on unusual end occurs because of boundary error. The minimal time for this operation is:

25 Msec/Sect x 30 Tracks/Cyl 500 Msec/Cyl

TST1,83 Header Read Order: Multiple Sector Read Test

Mode: Normal Mode

Header Read orders are issued to Read the Headers of all sectors of the first cylinder. TIO and TDV instructions and a Sense order are issued to verify the correct execution. The byte count is 8. The Header Read order is repeated by using data chaining and transfer in channel until an interrupt on unusual end occurs because of boundary error. The minimal time for this operation is:

25 Msec/Sect x 20 Tracks/Cyl 500 Msec/Cyl

TST1,84 Short Record Test

Mode: Normal Mode

The sequences of orders Seek - Write, Seek - Checkwrite and Seek - Read are issued. TIO and TDV instructions and a Sense order are issued to verify the correct execution. Test Variations:

1. Short Record Write: Byte count 4
2. Short Record Checkwrite: Byte count 4
3. Short Record Read: Byte count 4
4. Checkwrite: Byte count 1024
5. Read: Byte count 1024, compare of data

TST1,86 Surface Test

Mode: Normal Mode

The sequences of orders Seek - Write and Seek - Read are issued. TIO and TDV instructions and a Sense order are issued to verify the correct execution. Random data pattern are used. The seed for the random pattern is a random number combined with the Seek address by an exclusive or operation. The Read data are compared with the expected data. Test Variations:

Disk: 1. Write on all sectors of Cyl. 1,78,201,0,2,77,79,200,202
2. Read from all sectors of Cyl. 1,78,201,0,2,77,79,200,202

TST1,87 Header Read: Check Byte Error Test

Mode: Device Test Mode

A Header Write order is issued to Write a flaw mark on Header Cyl 202, Head 0, Sect 0. The test mode selection order is set to force check byte errors on the following Header Read order. (The first two bits are forced to zero.) TIO and TDV instructions and a Sense order are used to verify the correct execution of the order.

TST1, 88 Read: Check Byte Error Test

Mode: Controller Test Mode

A Write order is issued to Write a data pattern. The test mode selection order is set to force check byte errors on the following Read orders (X'02' and X'12'). (The first two bits are forced to zero.)
Test Variations:

1. Byte count is 2048
2. Buffer address not multiple 4

TIO and TDV instructions and a Sense order are used to verify the correct execution of the order.

### TST1,89 Flaw Mark Test

Mode: Normal Mode

The sequences of orders Seek - Header Write and Seek - Header Read are issued. TIO and TDV instructions and a Sense order are issued to verify the correct execution. The Seek address is Cyl 202, Head 0, Sector , 0.
Test Variations:
1. A Header with a flaw mark is written
2. Header Read order
3. Write, Check write and Read orders
4. The Header of Cyl. 202, Head 0, Sector 0 is rewritten;

Byte 0 - 3 of the Sense data (Address) is verified.

### TST1,90 Wrong Address Simulation Test

Mode: Normal Mode

The sequences of orders Seek - Header Write, Seek - Header Read, Seek - Write, Seek - Check write and Seek - Read are issued. TIO and TDV instructions and a Sense order are issued to verify the correct execution. The Seek address is Cyl = 202, Head = 0, Sector = 0.
Test Variations:
1. Header with Cyl. = 0
2. Header with Head = 1
3. Header with Sector = 1
4. Rewrite Header only

In the first three passes, Write, Check write, Read and Header Read orders are issued and the error indication verified.

### TST1,94 Double Seek Test

Mode: Normal Mode

A Seek order (X'03') command chained to another Seek order is issued. TIO and TDV instructions and a Sense order are issued to verify the correct execution. The Seek address is Cyl/Head/Sect = 202/0/0.

### TST1,95 Write: HIO and Device Reset Test

Mode: Device Test Mode

This subtest verifies that the HIO instruction and the device reset command are not destroying any data.
Test Variations:
1. Write, Disk Cyl. 0,1,2,3
2. Write, Address = X'020000', HIO during phase 'Write Data'
3. Read and Verify
4. Write, Disk Cyl. 0,1,2,3
5. Write, Address = X'020000', Dev. reset phase 'Write Data'
6. Read and Verify

### TST1,96 Device Address Parity Test

Mode: Device Test Mode

A Seek order is issued. A previous test mode selection order has set the condition for a device address parity error simulation. The device will go 'not operational'. A device reset order is issued to clear the device again.

### TST1,97 Seek Order: Time Out Test

Mode: Device Test Mode

1. A Seek order is issued with the address Cyl 12 (190)
2. The device is set in incremental device test mode and a second Seek order is issued with a Cylinder addr. 0 (202). The Seek operation is performed only to the point where the address is stored in the device.
3. Seek time out interrupt is expected
4. A restore order is issued

### TST1,98 Reserve and Release Test

Mode: Normal Mode

(This test is valid only in dual access configurations with explicit release feature installed)
An SIO instruction with a Reserve order reserves device A. TIO and TDV instructions are used to verify the correct execution. A TIO instruction is issued to device B to verify the reservation. A Release, order is issued to device A. TIO and TDV instructions are used to verify the correct execution. A TIO instruction is issued to device B to verify the release. Sense data are checked for dual access flag (byte 5, bit 0) and explicit release flag (byte 4, bit 1).
Explanation:
Device A Access to disk with controller A
Device B Access to disk with controller B

### TST1,99 Reserve and Release: Interrupt Test

Mode: Normal Mode

(This test is valid only in dual access configurations with explicit release feature installed)
An SIO instruction with a Seek order is issued to reserve device A.
A condition release interrupt order is issued to controller B. A Release order is then issued to device A.
Test Variations:
1. Condition rel. with interrupt modif. bit interrupt expected. Verification of device address.
2. Condition rel. without interrupt modif. bit no interrupt expected.

Sense data are checked for dual access flag (byte 5, bit 0) and explicit release flag (byte 4, bit 1).
Explanation:
Device A Access to disk with controller A
Device B Access to disk with controller B

### TST1,100 Device Power Down Test

Mode: Device Test Mode

The sequences of orders Seek - Write and Seek - Read are issued. This subtest verifies that data is not destroyed during a power down sequence. The power down sequence is forced by the TDV address 'B' (set diagnostic condition) and the 2nd Test mode byte X'80'.
Test Variations:
1. Write, Disk Cyl. 0,1,2,3
2. Write, Address X'020000', TDV during phase 'Write Data'
3. Read and Verify

### TST1,101 Write Protect Test

Mode: Normal Mode, Device Test Mode

The sequence of orders Seek - Write is issued twice. TIO and TDV instructions and a Sense order are issued to verify the correct execution.
Test Variations:
1. Write Protection by Controller
2. Write Protection by Device

This subtest prints the message: 'Set All Write Protect Switches For This Test'. After setting these switches, the operator has to inset any character at the KSR to continue the test.

### TST1,102 Attention Interrupt Test

Mode: Normal Mode

Wait for attention interrupt. This subtest prints the message: 'Set Attention Interrupt'. After setting attention interrupt, the operator has to insert any character at the KSR to continue the test.

### TST1,103 Not Operational Test

Mode: Device Test Mode

This subtest prints the message: 'Set Any Error: Interlock Error, Envir. Error'. After setting any of these errors, the operator has to insert any character at the KSR to continue the test. A printout of this test sequence occurs for this subtest independent from errors. The operator has to verify the correct setting of the corresponding bits.

### TST1,104 Write, Read, Check Write: Surface Test

Mode: Normal Mode

This subtest is designed to perform a complete and fast test of the disk surface. In order to achieve the desired operational speed, data chaining plus transfer-in-channel back to the first IOCD is used. The data chaining operation is performed until an interrupt on unusual end terminates the sequences. There are three reactions on this termination:
Error Recoveries:

1. Cylinder End: Continue with next Cylinder. No error, no report
2. Flaw Mark: Continue with next Track (Addr. derived from Sense data.) No error, no report
3. Any other error: Issue a Restore and continue with next sector (Addr. derived from Sense error: reporting, summary)

After writing the entire surface with the same data pattern which was specified by the Data directive, the entire surface is Read (Check Written) in the same way with data chaining. At the termination of the chaining sequence, a data comparison of the last data is made. The error recovery is the same as in the Write operation.
The following operations are performed:

1. Write the surface once } Default
2. Read the surface once }
3. Check write the surface once
4. Read the surface 8 more times

At program load time, the default value is set to 2 for one Write and one Read pass. The default value may be changed to a value from 1 to 11. A value of 10 performs item 1. 2. and 3. above and 7 Read passes of item 4.

### TST1, 105 Read Strobe Test

Mode: Device Test Mode/Normal Mode
Device Type: Disk

This subtest executes write, read and checkwrite operations in a similar fashion as subtest 104. The operations write, read, checkwrite. . . . are executed twice in two passes.
Pass1: Read Strobe Advanced
Pass2: Read Strobe retarded
The read strobe advanced/retarded mode is set for each I/O operation separately. The write, read, or checkwrite operations are executed in normal controller mode.
The default value for the loop count is 2. The loop count can be changed with the alt-directive. By changing location X'242'. For example: Alt, 242, N. N A value 3-11 indicating the number of reads.

### TST1, 106 Head Alignment Test

Mode: Device Test Mode
Device Type: Disk 33

This subtest requires a CE Pack and the tester.

The test performs the following steps:

1. 1500 seek operations are performed to cylinders 240 and 245.
2. The offset values for each head are determined in the following sequence:
   Reverse direction and positive polarity
   Forward direction and positive polarity
   Reverse direction and negative polarity
   Forward direction and negative polarity

   The initial and final sign values as well as the offset values are saved for all head for evaluation in Step 3.

3. The offset value is computed using the following formula:
   ((+OR-POSITIVE OFFSET) - (+OR-NEGATIVE OFFSET))/2
   The polarity of the offset is determined by the sign at 0 offset position.

   A summary of all heads is reported. Offset values greater than +OR- 150 micro inches are indicated by ***. The out of range messages means that there was no sign change within +OR- 1200 micro inches.

TST1 - EXAMPLE OF ERROR REPORTING

**Printout** / **Printed by the Functional Subroutine**

Header (Supplied by Test Driver)

```
TST1,037    IO ADDRESS 04AF
---------------------------
*** ERROR ***
READ TEST
***
```

Pattern Spread Routine (X'8000')

```
***
SPREAD DATA
PATTERN TYPE : 0
BUFFER : 003192
CLEAR BUFFER B : 003294
***
```

Test Mode Selection Routine (X'4000')

```
TEST MODE SELECTION EXECUTED , BYTES 0205
***
```

Seek Routine (X'2000')

```
SEEK EXECUTED , ADDRESS 0000 00 00
***
```

Execution Routine (X'0800')

```
*** START OF IO OPERATION ***
SIO STATUS
    01234567 89ABCDEF CC(1-4)
EXP 0XX1X000 XXXXXXXX 00XX
OBS 00010000 00000000 0000
COMMAND WORD ADDRESS 001E32
IOCD 0200CA50 08000400
*** STATUS AT END OF IO OPERATION ***
TIO STATUS
    01234567 89ABCDEF CC(1-4)
EXP X001X000 XXXXXXXX 0XXX
OBS 00010000 00000000 0010
CURRENT COMMAND DOUBLE WORD ADDRESS EXP 000F19 OBS 000F19
REMAINING BYTE COUNT EXP 0000 OBS 0000
***
```

IO Routine 1 (X'0020')

```
TIO STATUS
    01234567 89ABCDEF CC(1-4)
EXP 00010000 00000000 00XX
OBS 00010000 00000000 0010
***
```

IO Routine 2 (X'0010')

```
TDV STATUS
    01234567 89ABCDEF CC(1-4)
EXP 01000011 XXXXXXXX 01XX
OBS 01000011 00000000 0110
***
```

Sense Routine (X'0004')

```
*** ERROR ***
SENSE DATA
BYTE  0   1   2   3    4   5   14   15
EXP   XX  XX  XX  XX   XX  XX  XX   XX
OBS   00  00  00  01   00  00  00   00
DEVICE FAULTS (BYTE 6)
EXP     XXXX XXXX
OBS     0000 0000
CONTROLLER FAULTS (BYTE 8,9)
EXP     0100 0000 0011 1000
OBS     0000 0000 0011 1000
INTERRUPT BITS (BYTE 10,11)
EXP     0000 0000 0000 0000
OBS     0000 0000 0000 0000
CHECK BYTES (BYTE 12,13)
EXP     1000 0000 0011 1111
OBS     0000 0000 0000 0000
***
```

Compare Routine (X'0002')

```
*** ERROR ***
COMPARE OF DATA
BUFFER A : 003192
BUFFER B : 003294
COMPARE ERROR
    *BYTE 0 * *BYTE 1 * *BYTE 2 * *BYTE 3 * WD CNT
EXP 1000 0000 0011 1111 1101 0101 0110 1010   0000
OBS 0000 0000 0000 0000 0000 0000 0000 0000
EXP 1000 0000 0011 1111 1101 0101 0110 1010   0001
OBS 0000 0000 0000 0000 0000 0000 0000 0000
EXP 1000 0000 0011 1111 1101 0101 0110 1010   0002
OBS 0000 0000 0000 0000 0000 0000 0000 0000
EXP 1000 0000 0011 1111 1101 0101 0110 1010   0003
OBS 0000 0000 0000 0000 0000 0000 0110 1010
EXP 1000 0000 0011 1111 1101 0101 0110 1010   0015
OBS 1000 0000 0000 0000 0000 0000 0000 0000
PRINT LIMIT : ERROR COUNT 0239
```

END (Supplied by Test Driver)

```
*** END ***
```

GENERAL EXPLANATION

1. The underlined test heading defines the failing test and unit.
2. The line following the heading indicates that the test failed if the '*** ERROR ***' line is printed. If display is selected and the current test did not fail, '*** DISPLAY ***' is indicated.
3. Groups of lines are separated by a '****' line. Each group of lines is printed by a functional test subroutine. The name of each functional test subroutine responsible for the output of the above example is indicated. The hexadecimal number following the subroutine name indicates the mask value which must be entered with parameter 4 of TST1 in order to suppress the corresponding lines.
4. Those functional test subroutines which detected an error during testing will display an '*** ERROR ***' line following the '****' line which is a group separator.
   In the preceding example (page 1-18), errors were detected in the Sense Routine and the Compare Routine.
5. Expected data bits which represent a 'don't care' condition, are indicated by an 'X'.

ANALYSIS

1. From the test subroutine description for TST1,37, it can be seen that a read order in test mode was attempted.
2. From the test mode selection routine printout, it can be seen that the test mode data bytes are X'0205'. From the test mode data byte description, this test mode is a controller test mode for device, type 5 (see also SYST directive).
3. The IOCD line of the execution routine printout indicates that a read order of X'400' bytes (1024) was used during this test and that the operation terminated with a byte count of zero.
4. The first error is indicated by the Sense Routine. The controller fault bytes indicate that the second bit of byte 8 is in error and from the sense data byte description, the error is a "data check byte error". Bytes 12 and 13 of the sense order show the expected and observed check bytes and confirm that the check bytes do not match.
5. The subsequent compare error printout shows that the data received from the controller is all zeros.
6. Conclusion:
   Since the read operation itself operated correctly and terminated with a byte count of zero, the only problem appears to be that the simulated read data from the controller turnaround operation was not generated properly.

# Section 10

# SIGMA 5 - 9
# 9 - CHANNEL
# MAGNETIC TAPE TEST

## PROGRAM NO. 705542

## Section 10

## CONTENTS

Page

Subject Model . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 10-1
Required Equipment . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 10-1
Program Prerequisites . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 10-1
General Operating Procedures . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 10-1
Directives . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 10-2
Start Procedure . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 10-4
Order Codes . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 10-4
TDV Status . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 10-5
AIO Status . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 10-5
Functional Subtests and Related Error Messages . . . . . . . . . . . . . . . . . . 10-6

10

# 10. SIGMA 5–9 9-CHANNEL MAGNETIC TAPE TEST

**SUBJECT MODEL** -- Magnetic Tape Controller Model numbers 7320, 7321. Magnetic Tape Storage Units Model numbers 7322, 7323. Potter Magnetic Tape Units Speeds 75, 120, 150.

**REQUIRED EQUIPMENT** -- Minimum Memory Size: 16K; Input Device: Card Reader, Paper Tape Reader or Magnetic Tape Unit; Output Device: Keyboard Printer or Line Printer

## PROGRAM PREREQUISITES

None

## GENERAL OPERATING PROCEDURES

General operating procedures of the Xerox Sigma 5 through 9 Diagnostic Program Monitor (DPM) apply to this program.

# 10. SIGMA 5–9 9-CHANNEL MAGNETIC TAPE TEST

**DIRECTIVES** – directives are entered after a "!" is typed out

| Name | Format | Parameter | | | |
|---|---|---|---|---|---|
| | | ID | Definition | Value Range | Standard Value (default) |
| Program Directives – Environmental Directives | | | | | |
| System Environment | SYST,D1,D2,D3 [,D4,D5,D6,D7 ,D8,D9,D10] | D1 | Device station model number | 7322, 7323, 75*, 120*, 150* | NOTE:<br>Intermixing of tape stations of 75 IPS and 150 IPS during TST0 or TST1 is not allowed |
| | | D2 | = 0 | 0 | |
| | | D3 | Valid IOP, Controller and device address of first unit | 80 ~ 1FFFF | |
| | | D4 | Device address of the second unit | 80 ~ 1FFFF | |
| | | : | | | |
| | | D10 | Device address of the eighth unit | 80 ~ 1FFFF | |
| Program Directives – Testing Directives | | | | | |
| Comprehensive Test (Functional tests, 1 ~ 37, and random exerciser test. Functional tests 38–41 are not executed) | TST0,D1,D2 | D1 | Number of ordered sequences executed by random exerciser | 0 ~ 99999999 | 000 (D1 = 0) |
| | | D2 | Number of retries in the random exerciser | | |
| Functional Test | TST1 [,D1 [,D2]] | D1 | The first subtest to be executed | 0 (all subtests)~41 | 0 |
| | | D2 | Last subtest to be executed | 1 ~ 41 | 41 |
| Random Exerciser Test | TST2,D1,D2 | D1 | Number of cycles to be performed | D1 > 0 | |
| | | D2 | Number of retries on error | D2 ≥ 0 | |
| Utility Test | TST3,D1,D2,D3,D4 | D1 | = 1 Tape Test<br>D2 = 0 Write, Rewind, Read Forward, Read Backward D3 Records<br>= 1 Write D3 records<br>= 2 Read forward D3 records<br>= 4 Read forward and backward D3 records in sequence<br>D3 = 0 Continue operation until EOT or BOT is reached<br>D4 Delay in milliseconds between operation sets | | NOTE:<br>To alter retry count in TST3, 1; change Loc. X'240' for writing and Loc. X'241' for reading. Preset value for both = 5. |
| | | D1 | = 2 Deskew Test<br>D2 = 0, 1 Write to EOT and rewind<br>= 2 Read forward to EOT and rewind<br>= 3 Read backward to BOT<br>= 4 Read forward to EOT and backward to BOT<br>= 5 Capstan slippage exerciser | | |
| | | D1 | = 3 Sync on a Character Test<br>D2 = 1 Read forward and space record backward<br>= 2 Read backward and space record forward<br>D3 Byte to sync on<br>D4 Delay in milliseconds between syncs | | |
| | | D1 | = 4 Compatibility and Noise Pattern Test<br>D2 = 0, 1 Write, Read backward, read forward all records<br>= 2 Space forward, read forward, read backward all records<br>= 3 Read forward, read backward, space forward all records<br>= 4 Read forward all records<br>= 5 Write all records<br>D3 = No of Records | (1-1500) | |

## DIRECTIVES

| Name | Format | Parameter | | | |
|---|---|---|---|---|---|
| | | ID | Definition | Value Range | Standard Value (default) |
| Program Directives – Testing Directives (Continued) | | | | | |
| | | D1 | = 5 Read/Space Test<br>D2 = 0 Rewind and read forward N records<br>= 1 Rewind and space forward N records<br>= 2 Read forward N records<br>= 3 Space forward N records<br>= 4 Space backward N records<br>D3 Number of records (N)<br>D4 = 0 Do not print record<br>= 1 Print record in error<br>= 2 Print record N | | |
| Program Directives – Optional Directives | | | | | |
| Pattern selection (for Utility Test TST3,1) | DATA,D1,H2,H3,H4 | D1 | = 0, Fixed Pattern<br>= 2, Random Pattern<br>= 5, Bit Crowding Pattern | 0 ~ 5 | |
| | | H2 | Pattern seed (for D1 = 0, 2)<br>Two Track Numbers (for D1 = 5) | 0 ~ FFFFFFFF<br>01 ~ 78 | |
| | | H3 | Byte string for first track D1 = 5 | 0 ~ FFFFFFFF | |
| | | H4 | Byte string for second track | | |
| Length of record selection (for Utility Test TST3, 1) | LEN,D1 | D1 | Length of Record in Bytes | Min. = 0<br>Max. = Function of Memory Size | |
| Limitation of Error printouts | LIMT,D1,D2 | D1 | = Limit Compare error printouts/record to D2 | 1 | |
| | | D2 | Maximum number of printouts (No limit if D2 = 0) | D2 ≥ 0 | |

Note: Parameter of any directive beginning with a D means decimal, with an H means hexadecimal

## START PROCEDURE

1. Sense Switch Options, Monitor Directive Options, and Environmental Directives - Refer to DPM section of this manual.
2. Test Strategy Selection

| | Comprehensive Test | Functional Test | Random Exerciser Test | Utility Test |
|---|---|---|---|---|
| Recommended Application | Normal Usage | Solid Failure Detection and Specific Problem Analysis | Intermittent Failure Detection | Deskew Adjustment, Threshold check, Capstan Ramp Adjustment, Compatibility Check |
| Test Directive | TST0 | TST1 | TST2 | TST3 |
| Prerequisite | None | None | TST1 | TST1 |
| Optional Directives | LIMT | LIMT | LIMT | LIMT, LEN, DATA |
| Subtests | Functional subtests (1 ~ 37) and random exerciser test | 41 subtests (see error messages for the test types) | Random selection of:<br>Order sequence<br>Buffer length<br>Data<br>The identical operation is performed on each selected device in turn, then the next operation is begun. | See program directive TST3 |
| Error Message Format | 1. ERROR NO. DDDD<br>2. Self-explanatory | ERROR NO. DDDD | Self-explanatory | Self-explanatory |

## ORDER CODES

| | |
|---|---|
| X'01' | Write |
| X'02' | Read Record (Forward) |
| X'03' | Set Correction } Not used with Potter units |
| X'04' | Sense } Not used with Potter units |
| X'0C' | Read Record Backward |
| X'13' | Rewind and Interrupt |
| X'23' | Rewind Off Line |
| X'33' | Rewind |
| X'43' | Space Record Forward |
| X'4B' | Space Record Backward |
| X'53' | Space File Forward |
| X'5B' | Space File Backward |
| X'63' | Set Erase |
| X'73' | Write Tape Mark |

### TDV STATUS

| MODEL | BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4* | 5 | 6 | 7 |
| 7322/3 | Rate Error | Write Permitted | Write Protect Error | End of File | Uncorrectable Read Error | Load Point | End of Tape | Rewind On-Line |

*TDV bit 4 always set for Potter units.

### AIO STATUS

| MODEL | BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 7322/3 | Rate Error | Device End | Write Protect Error | End of File | Uncorrectable Read Error | ◄— | NOT USED | —► |

## FUNCTIONAL SUBTESTS AND RELATED ERROR MESSAGES

### FAULT INDEX DESCRIPTION - FUNCTIONAL SUBTESTS

The fault index contains a brief description of each functional subtest and a list of associated error numbers with a brief description of each error. The subtests and error numbers are arranged in ascending sequence. The description of subtest NN is numbered NN00. The first two digits of the error number correspond to the associated subtest; the last two numbers correspond to the individual errors within the subtest.

### DESCRIPTIVE ERROR MESSAGES

Error numbers can be preceded by descriptive messages which will aid in the isolation of failures.

### FUNCTIONAL TEST

TST1, 1 AIO, HIO, TIO, TDV Test

Check the ability of the 9-track mag tape system to correctly respond to the AIO, HIO and the TDV instructions. AIO will only check the no interrupt pending condition. Verify address recognition and status response to these instructions. Any error in this test may indicate a possible problem in the sub-controller area.

| | |
|---|---|
| 0101 | AIO condition code error. No interrupt recognition expected. |
| 0102 | HIO condition code or status error. See printout. |
| 0103 | TIO condition code or status error. See printout. |
| 0104 | TDV condition code or status error. See printout. |

TST1, 2 Invalid Order Test

Check the invalid order detection by issuing two SIO's with invalid order codes (X'09', X'7B'). This test is designed to check order decoding, order-output and order-input phases in the controller and unusual end detection. The remaining byte count will be tested to verify that no data phases were executed. Check the ability of the HIO to reset UE condition.

| | |
|---|---|
| 0201 | SIO for invalid order not accepted. Condition code error. |
| 0202 | SIO for invalid order status error. UE and no interrupt pending expected. (WRITE backward) |
| 0203 | HIO did not reset interrupt pending bit in status. |
| 0204 | SIO for invalid order not accepted, condition code error. |
| 0205 | SIO for invalid order status error. UE and no interrupt pending expected. (WRITE TM backward) |

TST1, 3 Erase Order Test

Check the execution of the first valid order. This test is designed to further check order decoding, order-output and order-input phase in the controller, and order termination without unusual end. The remaining byte count will be tested to verify that no data phases were executed. The status response will be tested.

| | |
|---|---|
| 0301 | SIO condition code error on set erase. |
| 0302 | TIO status error on set erase. No UE or byte count reduction expected. No data phases executed. |

TST1, 4 Set Correction Order Test (Bypassed for Potter Units)

This test is designed to verify the data-output phase in the controller and order termination.

Three set corrections will be used:

1. Byte count = 1, Data byte = X'FF'
2. Byte count = 1, Data byte = X'00'
3. Byte count = 2

The remaining byte count will be tested to verify that data transfer can be terminated by the controller and that a data-output operation was actually performed. The status response will be tested.

| | |
|---|---|
| 0401 | SIO for set correction condition code error. (BC = 1, INFO = 00) |
| 0402 | TIO for set correction status error. No UE or INT pend expected. |
| 0403 | SIO for set correction caused information to change from 00. |
| 0404 | SIO for set correction condition code error. (BC = 1, INFO = FF) |
| 0405 | TIO for set correction status error. No UE or INT pend expected. |
| 0406 | SIO for set correction caused information to change from FF. |
| 0407 | SIO for set correction condition code error. (BC = 2, INFO = 00) |
| 0408 | TIO for set correction status error. BC = 1, No UE and no INT pend expected. |
| 0409 | SIO for set correction caused information to change from 00. |

TST1, 5 Sense Order Test (Bypassed for Potter Units)

This test is designed to verify the data-input phase in the controller and order termination.

Three sense orders will be used:

1. Byte count = 1, Data byte in buffer = X'FF'
2. Byte count = 1, Data byte in buffer = X'00'
3. Byte count = 2

The remaining byte count will be tested to verify that data transfer can be terminated by the controller and that a data input operation was actually performed. The status response will be tested.

| | |
|---|---|
| 0501 | SIO for sense condition code error. (BC = 1, INFO = 00) |
| 0502 | TIO for sense status error. BC = 0, No UE expected. |
| 0503 | SIO for sense caused information to change from 00. |
| 0504 | SIO for sense condition code error. (BC = 1, INFO = 00) |
| 0505 | TIO for sense status error. BC = 0, No UE expected. |
| 0506 | SIO for sense should cause information to change from FF to 00. |
| 0507 | SIO for sense condition code error. |
| 0508 | TIO for sense status incorrect. BC = 1, no UE expected. |
| 0509 | SIO for sense caused information to change from 00. |

TST1, 7 Interrupt on UE, CE, ZBC, and AIO (Bypassed for Potter Units)

Check the ability of the controller to generate an interrupt on unusual end, channel end, and zero byte count using a WRITE backward, erase, and sense order respectively. Check the execution of the AIO instruction. Verify that AIO and HIO can reset the interrupt pending condition. All status responses will be tested.

| | |
|---|---|
| 0701 | SIO for invalid order condition code error. (WRITE BKW, UE set) |
| 0702 | No UE interrupt on invalid WRITE backward with UE set. |
| 0703 | No UE set on AIO after invalid order or INT pending not reset after AIO. |
| 0704 | SIO for set erase condition code error. (Erase, CE set) |
| 0705 | No CE interrupt on erase with CE set. |
| 0706 | No interrupt pending set after HIO following the erase order. |
| 0707 | SIO for sense condition code error. (Sense, BC = 1, IZC set) |
| 0708 | No IZC interrupt on sense with IZC set. |
| 0709 | No interrupt pending reset after AIO following sense order or IZC not set in AIO status. |
| 0710 | HIO status response error following AIO. UE or IP should not be set. |
| 0711 | TIO status response error following HIO. IP should not be set. |

TST1, 8 I/O Interrupt Test

Check the ability of the IOP and CPU to interrupt the program whenever an interrupt call is generated by the controller. Verify proper operation of interrupt arm/disarm and enable/disable modes.

| | |
|---|---|
| 0801 | TIO status response error after an invalid order. IP and UE should be set. (WRITE BKW, UE set with INT disarmed) |
| 0802 | TIO status response error after interrupt armed and disabled. |
| 0803 | No interrupt received on invalid order with UE set after interrupt armed and enabled. |

### TST1, 9 Command Chaining (Bypassed for Potter Units)

Test the command chaining ability of the controller by issuing an erase/set correction/sense order sequence. Test the termination of the command chaining sequence by issuing a WRITE-backward/sense order sequence. All status responses will be tested.

0901 SIO condition code error on command chaining order (erase set correction, and sense).
0902 No interrupt on command chaining erase, set correct, and sense.
0903 The last double word address is incorrect on command chaining. The address should be sense.
0904 SIO condition code on command chaining order. (WRITE BKW, sense).
0905 No interrupt received on command chaining WRITE BKW, erase.
0906 The last double word address is incorrect on command chaining. The address should be WRITE backward.

### TST1, 11 Rewind Test

Check the execution of a rewind on-line order. The test will verify that the tape is positioned at load point after completion of the rewind order. Check the execution of a rewind and interrupt order. This test will verify that the tape remains at load point and that the device initiates on interrupt request. Verify that an AIO and HIO instruction can reset the interrupt pending condition in the tape controller and the tape station. Verify that device end status is returned during the AIO. All status responses will be tested.

1101 TDV status error after rewind on line. No load point bit set.
1102 TIO status error after rewind and interrupt. No interrupt pending set.
1103 TIO status error after HIO on rewind with interrupt.
1104 TIO status error after rewind with interrupt. Interrupt pending not set.
1105 AIO status error after rewind with interrupt. Device end not set.
1106 TIO status error after AIO. Interrupt pending not reset.
1107 TDV status error after rewind with interrupt. No load point set.

### TST1, 12 READ, Space Record and File Backward from BOT Test

Check the execution of a READ, space record, and space file order in the backward direction with tape positioned at load point. Verify that the controller responds with unusual end, end of file (TDV and AIO) and load point status. The test will check that the tape remains at load point. The byte count for all orders specified must remain unchanged.

1201 No interrupt received after READ backward at load point. (BC = 2)
1202 TIO or TDV status error on READ BKW at load point. UE, load point, and BC = 2 expected.
1203 No interrupt on space backward at load point. (BC = 2)
1204 TIO or TDV status error on space BKW at load point. UE, load point, and BC = 2 expected.
1205 No interrupt received on space file backward at load point.
1206 TIO or TDV status error on space file BKW at load point. UE, load point, and no EOF expected.

### TST1, 13 WRITE Tape Mark Test at BOT

Check the execution of a WRITE tape mark order. The test will verify that tape can be moved off load point and that the order can be terminated with both controller and station returning to ready. If tape run-away, issue HIO. Rewind tape and test load point. End of file status will not be tested. The byte count for the order must remain unchanged.

1301 No interrupt on WRITE tape mark at load point. (CE and BC = 2 set)
1302 TIO or TDV status error on WRITE tape mark at load point. EOF and BC = 2 expected.

### TST1, 14 Space Record Forward Test

Check the execution of a space forward order. The test will verify that tape can be moved off the load point and that the order can be terminated with both controller and station returning to ready. If tape run-away, issue HIO. Rewind tape and test for load point. End of file and unusual end status will not be tested. The byte count for the order must remain unchanged.

1401 No interrupt received on WRITE tape mark after rewind.
1402 No interrupt received on space forward over a tape mark at load point. (CE and BC 2 set.)
1403 Byte count on space FWD at load point error. Should be 2.
1404 TIO status error on space FWD at load point. No error expected.

### TST1, 15 WRITE Test (Byte 1 to 64)

Check the execution of WRITE orders using X'FF' as data pattern and a starting at a byte count of one up to a maximum byte count of 64. The test will verify that tape can be moved off the load point, that the order can be terminated with both controller and tape station returning to ready, that a data-output operation is actually performed, and that the byte count is always reduced to zero. Verify that incorrect length is not detected. Rewind tape and test for load point. TE (Transmission errors) not checked in this test.

1501 TIO or TDV status error on WRITE records 1-64 byte length. No incorrect length or UE expected, BC = 00.

### TST1, 16 READ Test

Test the execution of READ orders using a starting byte count of one up to a maximum count of 64. WRITE 64 records with a fixed byte count of 100 bytes (Pattern = X'FF') and rewind tape. This test will check the response to a READ forward operation (off load point, zero). Rewind tape and test load point. TE (Transmission errors) not checked in this test.

1601 TIO or TDV status error on writing 100 bytes all bits on. No incorrect length or UE expected, BC = 00.
1602 TIO or TDV status error on READ forward 100 bytes all bits on with Byte count 1–64. Incorrect length and no IZC expected.

### TST1, 17 EOF Test (Potter Units Only)

1701 Record write error (no UE, write permitted, no data error, zero byte count).
1702 Incorrect load point indication.
1703 Load point expected.
1704 Read backward error (device and controller not ready, no UE, no incorrect length, zero byte count, write permitted.
1705 Space file backward error (no UE, EOF, no data error).
1706 Space file forward error (no UE, EOF, no data error).
1707 Read forward error (same as 1704 read backward error).
1708 Incorrect record number.
1709 Double EOF detected.

### TST1, 18 WRITE READ Data Test

WRITE N records with a fixed byte count and data pattern of X'FF'. Rewind tape and READ N records in the forward direction. Verify that data can be recorded and READ from each track. TE (transmission errors) not checked in this test.

1801 TIO or TDV status error on writing 100 bytes all bits on. No incorrect length or UE expected, BC 00.

### TST1, 19 WRITE, READ Data Test (Data X'00' to X'80')

WRITE N records with a fixed byte count and the current data pattern data will be varied from X'00' through X'80'. Rewind tape and READ N records in the forward direction. Verify for each pass that only one track contains information and that all other tracks are zero. After each pass, loop on the data pattern which has caused an error and continue testing until a successful pass has been made.

1901 WRITE, READ forward, on information errors when saturating one track. 100 records of 100 bytes pattern 00, 01, 02, 04, 08, 10, 20, 40, 80.

### TST1, 20 Set Erase-WRITE Test

Check the capability of the tape station to skip over an area on the tape by checking the delay between the start of the WRITE order and the start of the data transfer.

2001 Erase time set too long. See message printout.

2002 Erase time set too short. See message printout.

2003 No interrupt on zero byte count occurred within 9 ms.

### TST1, 21 WRITE, Space FWD and BKW Test

WRITE N records with a fixed byte count. Rewind tape to load point. Space one record in the forward and backward direction. Space another record in the backward direction and check load point indicator. Space N records in the forward direction and then the reverse direction. Check all status response. Rewind to load point.

2101 TIO or TDV status error on writing 100 bytes all bits on.

2102 TIO or TDV status error on spacing forward over 100 bytes at load point.

2103 TIO or TDV status error on spacing backward over 100 bytes one record beyond load point. No UE or load point expected.

2104 TIO or TDV status error on spacing backward one record at load point. UE and load point expected.

2105 TIO or TDV status error on spacing forward over 100 bytes all bits on. No UE or error expected, BC = 00.

2106 TIO or TDV status error on spacing backward over 100 bytes all bits on. No UE or error expected, BC = 00.

### TST1, 22 WRITE Tape Mark Test

WRITE N tape marks and verify that end of file status is reported after each order. All tape marks are read forward and backward.

2201 TIO or TDV status error on writing a tape mark. Tape mark and no UE expected.

2202 TIO or TDV status error on reading backward over 100 tape marks. Tape mark and UE expected.

2203 TIO or TDV status error on reading forward over 100 tape marks. Tape mark and UE expected.

### TST1, 23 WRITE Tape Mark - Space File and Space Record Test

WRITE N tape marks and rewind to load point. Space file in the forward direction and verify end of file and no unusual end status. Space file backward and check end of file and no unusual end. Space file backward again and check end of file, beginning of tape and no unusual end. Verify all other status. Verify that unusual end and end of file status is reported when spacing or reading over a tape mark. WRITE N records followed by a tape mark. Verify space record in both directions.

2301 TIO or TDV status error on writing a tape mark. Tape mark and no UE expected.

2302 TIO or TDV status error on space file forward. Tape mark and no UE expected.

2303 TIO or TDV status error on space file backward. Tape mark and no UE expected.

2304 TIO or TDV status error on space file backward at load point. Load point, tape mark, and no UE expected.

2305 TIO or TDV status error on writing a record 100 bytes. No error expected, BC = 00.

2306 TIO or TDV status error on writing a tape mark. No error expected, tape mark.

2307 TIO or TDV status error on spacing backward over a tape mark. UE and tape mark expected.

2308 TIO or TDV status error on spacing forward over a tape mark. UE and tape mark expected.

### TST1, 24 Tape Loop Test

Rewind with command chain. Write with data chain 27,000 words loop back to rewind. This sequence is repeated 10 times in an effort to cause the tape to loop out in the vacuum columns.

2401 TIO or TDV status error after rewinding and writing a record of 27,000 words, looping 10 times. No error expected.

### TST1, 25 WRITE, READ Backward Data

WRITE N records with a fixed byte count. READ N records backward and verify data and status. READ another record backward and test beginning of tape status.

2501 TIO or TDV status error on writing a record of 100 bytes. No UE expected, BC = 00.

2502 TIO or TDV status error on reading 100 bytes backward. No UE expected, BC = 00.

2503 Incorrect information on reading 100 bytes backward all bits on.

2504 TIO or TDV status error on reading a record backward at load point. UE, load point and EOF expected.

### TST1, 26 Incorrect Length Test

WRITE a record and READ in both directions by using byte count –1 byte count +1 for the READ orders. Verify incorrect length and all other status indications. Suppress incorrect length feature in the IOP will also be tested.

2601 TIO or TDV status error on writing 100 bytes all bits on. No errors expected, BC = 00, no incorrect length.

2602 TIO or TDV status error on reading a record backward. No error expected, BC = 00. No incorrect length.

2603 TIO or TDV status error on reading a record forward. No error expected, BC = 00, no incorrect length.

2604 TIO or TDV status error on reading a 100 byte record backward with a BC = 99. Incorrect length, UE and BC = 00 expected.

2605 TIO or TDV status error on reading a 100 byte record forward with a BC = 99. Incorrect length, UE and BC = 00 expected.

2606 TIO or TDV status error on reading a 100 byte record backward with suppress inc length, BC = 101. Inc length, BC = 1, no UE expected.

2607 TIO or TDV status error on reading a 100 byte record forward with suppress inc length, BC = 101. Inc length, BC = 1, no UE expected.

2608 TIO or TDV status error on reading forward a 100 byte record with suppress inc length, BC = 99. Inc length, BC = 0, no UE expected.

### TST1, 27 Data Chaining Test

Test the data chaining capability of the IOP using WRITE and READ orders.

2701 TIO or TDV status error on writing 2 bytes data chain 98. No errors expected, BC = 00.

2702 TIO or TDV status error on reading backward 6 bytes data chain chain 94. No error expected, BC = 00.

2703 Information error on reading a record BKW 6 bytes data chain 94.

2704 TIO or TDV status errors on reading forward 48 bytes data chain 52. No error expected, BC = 00.

2705 Information error on reading a record FWD 48 bytes data chain 52.

### TST1, 28 Byte Boundary Test

This test performs READ and WRITE operations from all possible memory boundaries. For Potter tape units, the minimum byte count = 11 instead of 4.

2801 TIO or TDV status error when writing from WA, WA+1 byte, WA+2 bytes, WA+3 bytes.

2802 TIO or TDV status error when reading BKW into WA, WA+1 byte, WA+2 bytes, WA+3 bytes.

2803 Information error when reading BKW into WA, WA+1 byte, WA+2 bytes, WA+3 bytes.

2804 TIO or TDV status error when reading FWD into WA, WA+1 byte, WA+2 bytes, WA+3 bytes.

2805 Information error when reading FWD into WA, WA+1 byte, WA+2 bytes, WA+3 bytes.

2806 TIO or TDV status error on writing a record 4, 16, 32, 64, ... bytes in length.

2807 TIO or TDV status error on reading a record BKW 4, 16, 32, 64, ... bytes in length.

2808 Information error on reading backward 4, 16, 32, 64, ... bytes.

2809 TIO or TDV status error on reading a record FWD 4, 16, 32, 64, ... bytes in length.

2810 Information error on reading forward 4, 16, 32, 64, ... bytes.

### TST1, 29 Data Test Noise Patterns and Bit Crowding

This test will WRITE and READ variable data patterns. The sequence will always be WRITE, READ reverse and READ forward. The record size will be varied after each record. Noise sensitive and bit crowding data pattern will be used. WRITE and READ retries will be allowed if sense switch 1 is set.

2901 TIO or TDV status error on writing an incremented record with saturated tracks and noise pattern.
2902 TIO or TDV status error on reading backward on incremented record with saturated tracks and noise patterns.
2903 Information error on reading BKW incremented record with special saturated tracks and noise patterns.
2904 TIO or TDV status error on reading forward on incremented record with saturated tracks and noise patterns.
2905 Information error on reading forward an incremented record with saturated tracks and noise pattern.

### TST1, 31 CRC Test (Bypassed for Potter Units)

Check the ability to set all bits in the CRC character. A blank CRC character will also be written, READ FWD, and READ BKW 100 times. CRC register bits 123456789
Where 1 = Parity Bit
Where 2 = MSB
Where 9 = LSB

3101 TIO or TDV status error on writing a record with one bit set in the CRC character.
3102 TIO or TDV status error on reading a record backward with one bit set in the CRC character.
3103 Information error on reading a record FWD with one bit set in the CRC character.
3104 TIO or TDV status error on reading a record forward with one bit set in the CRC character.
3105 Information error on reading a record BKW with one bit set in the CRC character.
3106 TIO or TDV status error on writing a record with a blank CRC character.
3107 TIO or TDV status error on reading a record backward with a blank CRC character.
3108 Information error on reading a record BKW with a blank CRC char.
3109 TIO or TDV status error on reading a record forward with a blank CRC character.
3110 Information error on reading a record FWD with a blank CRC char.

### TST1, 32 READ - Set Correction Test (Bypassed for Potter Units)

The test will WRITE one error free record and sequentially set one bit at a time in the error pattern register for both forward and reverse READ modes. The data will be verified after each READ order to insure that the data remains unchanged.

3201 TIO or TDV status error on writing a record 100 bytes. No error expected.
3202 TIO or TDV status error on reading a record backward with 100 bytes. No error expected.
3203 Information error on reading a record BKW with 100 bytes.
3204 TIO and TDV status error on reading a record forward with 100 bytes. No error expected.
3205 Information error on reading a record FWD with 100 bytes.
3206 TIO or TDV status error on set correction bytes 01-80.
3207 TIO or TDV status error on READ backward with set correction.
3208 Information error on reading BKW with set correction bytes 01-80.
3209 TIO or TDV status error on set correction bytes 01-80.
3210 TIO or TDV status error on READ forward with set correction.
3211 Information error on reading FWD with set correction bytes 01-80.

### TST1, 33 READ - Sense Test (Bypassed for Potter Units)

WRITE one error free record in both directions. The sense order after each READ order should return a byte of all zeros to the IOP.

3301 TIO or TDV status error on writing a 100 byte record.
3302 TIO or TDV status error on reading a record BKW with 100 bytes.
3303 Information error on reading a record backward with 100 bytes.
3304 TIO or TDV status error on sense with information byte 00.
3305 Information error on sense. Should not change from 00.
3306 TIO or TDV status error on reading a record FWD with 100 bytes.
3307 Information error on reading a record forward with 100 bytes.
3308 TIO or TDV status error on sense with information byte 00.
3309 Information error on sense. Should not change from 00.

### TST1, 34 Ready - Busy Test

Check the busy condition after issuance of an order. The test will also attempt to issue an SIO to a busy controller and to a ready controller and a busy station.

3401 TIO error. Device should be busy while writing 1000 bytes.
3402 No interrupt received after writing 1000 bytes.
3403 TIO or TDV status error on writing a 1000 byte record.
3404 TIO error. Controller should be busy whil reading 1000 bytes..
3405 No interrupt received after reading a record BKW with 1000 bytes.
3406 SIO error. Controller should be busy on initiating rewind.
3407 TIO error. Device should be busy on rewinding.

### TST1, 35 Tape Creep Test

This test will WRITE one record followed by a set erase order and another WRITE order. A space record backward and rewrite sequence will now be repeated N times. After reading and verifying the data of the first record, READ the second record and compute the delay between the start of the READ order and the start of the data transfer. The direction of the creep will be determined by comparing the delay to the original value.

3501 TIO or TDV error on writing a 100 byte record.
3502 TIO or TDV error on spacing backward over a 16 byte record.
3503 TIO or TDV error on writing a 16 byte record.
3504 TIO or TDV error on spacing backward over a 16 byte record.
3505 TIO or TDV status error on spacing backward over 100 bytes.
3506 TIO or TDV status error on reading a 100 byte record forward.
3507 Information error on reading a 100 byte record forward.
3508 Tape creep tolerance exceeded in the tape creep test.
3509 Tape creep negative in the tape creep test.

### TST1, 36 Erase Verification Test

This test will test the erase order by rewinding tape and then writing N one byte records. The records are followed by a tape mark. After a rewind, WRITE one record, set erase, and WRITE one record. The tape is rewound. The records are counted to verify the erase order execution.

3601 The erase order did not remove the correct number of records when verifying the erase order.

### TST1, 37 Gap Length Timing Test

This routine verifies gap timing and is intended as a scoping aid for adjusting the forward and reverse ramp. The test can only be run on a system with a real time clock.
Operator intervention required if SS1 is set.

3701 TIO or TDV status error on writing 16 bytes in the I.R.G.* test.
3702 TIO or TDV status error on spacing backward over 16 bytes.
3703 TIO or TDV status error on writing 16 bytes in the I.R.G. test.
3704 TIO or TDV status error on spacing backward over 16 bytes.
3705 I.R.G. time is incorrect. See printout.

*I.R.G. Inter Record Gap

### TST1, 38 End of Tape Test (Bypassed for Potter Units)

This test will continue to WRITE records until the end of tape indicator is detected. One additional record will be recorded and the EOT condition will be verified again. Two records will be READ in the backward direction. After the second READ order, the EOT indicator should be reset. The tape will be rewound.

3801 TIO or TDV error writing 1000 bytes in the end of tape test.
3802 TIO or TDV error writing 1000 bytes beyond EOT indication. End of tape flag should be set.

TST1, 38 (Continued)

3803 TIO or TDV error reading backward 1000 bytes at EOT. The EOT flag should be set.

3804 TIO or TDV error reading backward 1000 bytes near EOT. The EOT flag should be reset.

TST1, 39 Set Correction Test (Bypassed for Potter Units)

This routine requires the user to force a READ error as specified by the program. This test will verify that READ errors can be corrected and that a noncorrectable status will be returned if the error is caused by at least two tracks. For the READ with correction test to prevent setting READ register F/F when the AR signal is missing in all dual threshold:

Put jumper from GND to 7W43
GND to 15W41
GND to 15W07

To install jumpers for recoverable READ errors:
Track 1 (CH 0 - Data Bit 0) 3V23 (LRCT) to 19W43
Track 2 (CH 1 - Data Bit 1) 3V23 (LRCT) to 19W28
Track 3 (CH 2 - Data Bit 2) 3V23 (LRCT) to 19W12
Track 4 (CH 3 - Data Bit 3) 3V23 (LRCT) to 19W33
Track 5 (CH 4 - Data Bit 4) 3V23 (LRCT) to 19W17
Track 6 (CH 5 - Data Bit 5) 3V23 (LRCT) to 19W02
Track 7 (CH 6 - Data Bit 6) 3V23 (LRCT) to 18W13
Track 8 (CH 7 - Data Bit 7) 3V23 (LRCT) to 18W33
Track 9 (CH P - Data Parity) 3V23 (LRCT) to 18W18
Operator intervention required

3901 TIO or TDV status error on writing 100 bytes.

3902 TIO or TDV status error on reading backward 100 bytes.

3903 TIO or TDV status error on reading forward 100 bytes.

3904 Error when reading backward with a track error forced. An uncorrectable TE is expected.

3906 Status error on sense in the track correction test.

3907 Information from sense is incorrect. (80, 40, 20, 10, 08, 04, 02, 01, 00).

3908 Status error on set correction in the track correction test.

3909 Status error on READ BKW and correct in the track correction test.

3910 Error when reading forward with a track error forced. A correctable TE is expected.

3911 Error when reading forward with 2 track errors forced. An uncorrectable TE is expected.

3912 Status error on sense in the track correction test.

3913 Information from sense is incorrect. (80, 40, 20, 10, 08, 04, 02, 01, 00).

3914 Status error on set correction in the track correction test.

3915 Status error on READ FWD and correct in the track correction test.

3916 Information error verifying 100 bytes in the BKW direction.

3917 Information error verifying 100 bytes in the FWD direction.

3918 Information error reading BKW and correcting 100 bytes.

3919 Information error reading FWD and correcting 100 bytes.

TST1, 40 Operator Control Panel Test

This test will check every switch on the operator control panel in the sequence specified by the program and verify the WRITE protect feature. Messages are printed describing the action required by the operator.
Operator intervention required.

4001 Status error on writing a record designation unit 0, 1, 2, 3, 4, 5, 6, 7.

4002 Status error on reading BKW with designation unit 0, 1, 2, 3, 4, 5, 6, 7.

4003 Information error reading BKW record from unit 0, 1, 2, 3, 4, 5, 6, 7.

4004 Status error on reading FWD with designation unit 0, 1, 2, 3, 4, 5, 6, 7.

4005 Information error reading FWD record from unit 0, 1, 2, 3, 4, 5, 6, 7.

4006 Status error when trying to WRITE on a unit with the WRITE ring removed. A WRITE protect is expected.

4007 Status error when trying to WRITE a tape mark with the WRITE ring removed. A WRITE protect is expected.

4008 No interrupt was received when the attention button was set by the operator.

4009 Status error on rewind and put off line. The device should be manual and the controller ready.

4010 TDV status incorrect. Load point and ready expected.

## RANDOM EXERCISER TEST AND RELATED ERROR MESSAGES

TST2 RANDOM EXERCISER TEST

This test provides a means of operating a magnetic tape system with pseudo-random operation, order sequence, data pattern, I/O area, time delay, and record size for the purpose of detecting intermittent failures and exercising all tape units. All Potter units are rewound and put off-line at the end of test.

The random exerciser test will report errors as they occur, but only as to the function that failed. No error looping is provided except for limited retries.

D1 = Number of cycles, set to 1000 IF 0.
D2 = Number of error retries.

From the random seed the following masks are used to get type of operation, word size of record, and time delay in milliseconds.
X'00003FF0' To get random record word size
X'001F0000' To get random time delay in milliseconds
X'0000000F' To get random operation set

Random Operation Sets
0 WRITE, WRITE, WRITE, WRITE, WRITE
1 WRITE, WRITE, WRITE, WRITE, READ BKW
2 WRITE, WRITE, WRITE, WRITE, Space BKW
3 WRITE, WRITE, WRITE, READ BKW, READ BKW
4 WRITE, WRITE, WRITE, READ BKW, Space BKW
5 WRITE, WRITE, WRITE, Space BKW, READ BKW
6 WRITE, WRITE, WRITE, Space BKW, Space BKW
7 WRITE, WRITE, WRITE, Space BKW, READ FWD
8 WRITE, WRITE, WRITE, READ BKW, Space FWD
9 WRITE, WRITE, READ BKW, READ BKW, READ FWD
A WRITE, WRITE, READ BKW, READ BKW, Space FWD
B WRITE, WRITE, Space BKW, Space BKW, READ FWD
C WRITE, WRITE, Space BKW, READ BKW, Space FWD
D WRITE, READ BKW, READ FWD, READ BKW, READ FWD
E WRITE, READ BKW, READ FWD, Space BKW, READ FWD
F WRITE, Space BKW, Space FWD, READ BKW, READ FWD

Descriptive Error Messages

Note: Most of those error messages listed under TST1 may occur during TST2
Terminating Message
(Normally printed at the end of TST0 and printed at the end of TST2 if errors have been detected)

Device XXXX Perm WRT TALY AAAA Temp WRT TALY BBBB
Perm R B TALY CCCC Temp R B TALY DDDD Perm RF
TALY EEEE Temp R F TALY FFFF

Device XXXX Reported the following errors:
AAAA Permanent WRITE errors (retries unsuccessful)
BBBB Temporary WRITE errors (retries successful)
CCCC Permanent READ backward errors (retries unsuccessful)
DDDD Temporary READ backward errors (retries successful)
EEEE Permanent READ forward errors (retries unsuccessful)
FFFF Temporary READ forward errors (retries successful)

Random Exerciser Standard Error Messages

Rand Word AAAAAAAA Dev. XXXX PASS HEX PPPPPPPP
Failing Seq: S,S,S,S,S

Device XXXX Failed pass PPPPPPPP using random Data Seed AAAAAAAA while executing sequence of operations S,S,S,S,S

## UTILITY TESTS

### TST3 UTILITY TESTS

The utility test routine allows the user to select a specific function and to control the data pattern (see data directive) and the record length (see 'LEN' directive).

Parameters D1 = Utility test selection
D1 = 1 tape test
D1 = 2 deskew test
D1 = 3 sync on a character test
D1 = 4 compatibility and noise pattern test
D1 = 5 read/space test
D2 = operations requested according to test
D3 = parameter requested according to test
D4 = parameter requested according to test

### TST3, 1 TAPE TEST

This test allows the user to WRITE, READ forward, READ backward, READ forward and then backward, or WRITE followed by rewind and READ forward and READ backward N records or until EOT is reached.

Parameters D1 = 1 tape test
D2 = 0 WRITE, rewind, READ forward, READ backward D3 records
 1 WRITE D3 records
 2 READ forward D3 records
 3 READ backward D3 records
 4 READ forward and backward D3 records in sequence
D3 = number of records to be written or read.
 If D3 = 0 continue until EOT or BOT is reached
D4 = delay in milliseconds between operation sets

Example TST3, 1, 1, 1000, 5
WRITE 1000 records with a 5 millisecond delay after each WRITE operation

### TST3, 2 DESKEW UTILITY TEST

This test is provided as a scoping aid during checking and adjusting the READ/WRITE skew. A pattern of all ones will be recorded as a continuous record. At EOT the tape will be rewound.

Parameters D1 = 2 Deskew test
D2 = 0, 1 WRITE until EOT is reached and rewind
 2 READ forward until EOT and rewind
 3 READ backward until BOT is reached
 4 READ FWD till EOT, READ BKW till BOT, no rewinds
 5 capstan slippage exerciser
D3 = not used
D4 = not used

Example TST3, 2, 2
READ forward until EOT and rewind

### TST3, 3 SYNC ON A CHARACTER UTILITY

This test is provided as a scoping aid by executing a unique I/O instruction (TDV) after the byte count specified in the test has been reached.

Parameters D1 = 3 SYNC on a character test
D2 = 1 READ forward and space record backward
 2 READ backward and space record forward
D3 = Byte to SYNC on
D4 = Delay in milliseconds between SYNCS

Example TST3, 3, 1, 375, 10
READ forward 375 bytes, signal (TDV) and wait 10 milliseconds. Space backward

### TST3, 4 COMPATIBILITY AND NOISE PATTERN TEST

This test allows the user to WRITE, READ forward, READ backward, or READ forward and backward a predetermined incremented noise pattern.

Parameters D1 = 4 compatibility and noise pattern test
D2 = 0, 1 WRITE, READ backward, and READ forward all records
 2 space forward, READ backward, READ forward all records
 3 READ forward, READ backward, space forward all records
 4 READ forward all records
 5 WRITE all records
D3 = number of records (1-1500)
D4 = not used

Example TST3, 4, 5
WRITE all records

### TST3, 5 READ/SPACE TEST

This test allows the user to READ or space N records with or without rewind. Only non-recoverable transmission errors will cause error printout, backspace and a halt.

Parameters D1 = 5 READ/space test
D2 = 0 rewind and READ FWD N records
 1 rewind and space FWD N records
 2 don't rewind, READ FWD N records
 3 don't rewind, space FWD N records
 4 don't rewind, space BKW N records
D3 = number of records to READ or space
D4 = 0 don't printout record
 1 printout record in error
 2 printout nth record

Example TST3, 5, 0, 100, 1
Rewind, READ 100 records, print error records

## OPTIONAL DIRECTIVES

DATA The directive selects a pattern type to be used during the tape test (TST3, 1 only).

Parameters D1 = pattern type
 0 fixed pattern
 2 random pattern
 5 bit crowding pattern
D2 = if D1 = 0 fixed pattern
 if D1 = 2 random pattern seed
 if D1 = 5 two track numbers
D3 = if D1 = 5 byte string for 1st track
D4 = if D1 = 5 byte string for 2nd track

Examples DATA, 2, 12876541
Generate random pattern starting with seed 12876541
DATA, 5, 37, FF00FF00, 00FF00FF
Generate a bit string FF00FF00 on track 3,
Generate a bit string 00FF00FF on track 7

LIMT The directive limits specific operation during execution of the test.

Parameters D1 = limit type
 D2 = limit count
D1 = 1 limit compare error printout
 D2 = number of compare errors to be reported in each record

Example LIMT, 1, 5
Report up to 5 compare errors for each record

LEN This directive selects the byte length of the record to be used in the tape test (TST3, 1 only).

Parameters D1 = byte length of record
D2 = not used
D3 = not used
D4 = not used

Example LEN, 980
Generate a record of 980 bytes

# Section 11

# SIGMA 5 - 9
# 7 - CHANNEL
# MAGNETIC TAPE TEST

## PROGRAM NO. 705735

## Section 11

## CONTENTS

Page

Subject Model . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 11-1
Required Equipment . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 11-1
Program Prerequisites . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 11-1
General Operating Procedures . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 11-1
Directives . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 11-2
Start Procedure . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 11-4
Program Test Description . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 11-4
Order Codes . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 11-5
TDV Status . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 11-5
AIO Status . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 11-5
Functional Subtests and Related Error Messages . . . . . . . . . . . . . . . . . . . 11-6

# 11. SIGMA 5–9 7-CHANNEL MAGNETIC TAPE TEST

**SUBJECT MODEL** -- Magnetic Tape Stations, Model numbers 7362, 7372, Magnetic Tape Controllers, Model numbers 7361/7365, 7371/7374.

**REQUIRED EQUIPMENT** -- Minimum Memory Size: 16K; Input Device: Card Reader, Paper Tape Reader or Magnetic Tape Unit; Output Device: Keyboard Printer or Line Printer.

## PROGRAM PREREQUISITES

None

## GENERAL OPERATING PROCEDURES

General operating procedures of the Xerox Sigma 5 through 9 Diagnostic Program Monitor (DPM) apply to this program.

# 11. SIGMA 5–9 7-CHANNEL MAGNETIC TAPE TEST

**DIRECTIVES** - directives are entered after a "!" is typed out

| Name | Format | Parameter | | | |
|---|---|---|---|---|---|
| | | ID | Definition | Value Range | Standard Value (default) |
| Program Directives - Environmental Directives | | | | RWTH - 7322 | |
| System Environment<br>Example:<br>SYST,7372,0,81,83,87<br>Tape devices 81,83,87 on 7372 (75 IPS)<br>SYST,7362,0,80<br>Tape devices 80 on 7362 (37.5 IPS) | SYST,D1,D2,D3 [,D4,D5,D6,D7 ,D8,D9,D10] | D1 | Device station number | 7362, 7365 (37.5 IPS)<br>7372, 7374 (75 IPS) | NOTE:<br>Intermixing of tape stations of 37.5 IPS and 75 IPS during the functional test is not allowed |
| | | D2 | = 0 | 0 | |
| | | D3 | Valid IOP, controller and device address of first unit | 80 ~ 1FFFF | |
| | | D4 | Device address of 2nd unit | | |
| | | : | | | |
| | | D10 | Device address of 10th unit | | |
| Program Directives - Testing Directives | | | | | |
| Comprehensive Test (all functional tests, 1 ~ 37 and random exerciser test) | TST0,D1,D2 | D1 | Number of loops on the random exerciser | 0 ~ 99999999 | If D1 = 0<br>1000 loops and 5 retries |
| | | D2 | Number of retries on the random exerciser | | |
| Functional Test | TST1[,D1,D2] | D1 | The first subtest to be executed | 1 ~ 40 | |
| | | D2 | Last subtest to be executed | | |
| Random Exerciser Test | TST2,D1,D2 | D1 | Number of passes to be executed | 0 ~ 99999999 | |
| | | D2 | Number of retries if any errors | | |
| Utility Test | TST3,D1,D2[,D3,D4] | D1 | = 1 Tape test<br>D2 = 0 Write, rewind, read forward, space backward D3 records<br>1 Write D3 records<br>2 Read forward D3 records<br>3 Space backward D3 records<br>4 Read forward and space backward D3 records in sequence<br>8 Write, rewind, read fwd, space backward D3 records (BCD)<br>9 Write D3 records (BCD)<br>10 Read fwd D3 records (BCD)<br>12 Read fwd, space bkw D3 records (BCD)<br>D3 = Number of records to be written or read. If D3 = 0 continue until EOT or BOT is reached<br>D4 = Delay in milliseconds between operation sets | | |
| | | D1 | = 2 Deskew test<br>D2 = 0, 1 Write until EOT is reached and rewind<br>2 Read forward until EOT and rewind<br>3 Space backward until BOT is reached<br>4 Read fwd until EOT, space bkw until BOT, no rewinds<br>5 Capstan slippage exerciser<br>D3 = Not used<br>D4 = Not used | | |
| | | D1 | = 3 Sync on a character test<br>D2 = 1 Read forward and space record backward<br>2 Space backward and space record forward<br>D3 = Byte to sync on<br>D4 = Delay in milliseconds between syncs | | |

**DIRECTIVES** (continued)

| Name | Format | Parameter | | | |
|---|---|---|---|---|---|
| | | ID | Definition | Value Range | Standard Value (default) |
| Program Directives - Testing Directives (Continued) | | | | | |
| | | D1 | = 4 Compatibility and noise pattern test<br>D2 = 0, 1 Write, space backward, and read forward all records<br>2 Space forward, space backward, read forward all records<br>3 Read forward, space backward, space forward all records<br>4 Read forward all records<br>5 Write all records<br>D3 = The number of records to be written (1 - 1500)<br>D4 = Not used | | |
| | | D1 | = 5 Read/space test<br>D2 = 0 Rewind and read fwd N records<br>1 Rewind and space fwd N records<br>2 Don't rewind, read fwd N records<br>3 Don't rewind, space fwd N records<br>4 Don't rewind, space bkw N records<br>8 Rewind, read fwd N records with even parity, decimal (BCD)<br>10 Don't rewind, read fwd with even parity, decimal (BCD)<br>D3 = Number of records to read or space<br>D4 = 0 Don't printout record<br>1 Printout record in error<br>2 Printout Nth record | | |
| Program Directives - Optional Directives | | | | | |
| Pattern selection<br>(for Utility Test)<br>(TST3, 1 only)<br>Example: DATA,2,12876541<br>Generate random pattern starting with seed 12876541.<br>DATA,5,36, FF00FF00, 00FF00FF.<br>Generate a bit string FF00FF00 on track 3.<br>Generate a bit string 00FF00FF on track 6. | DATA,D1,H2[,H3,H4] | D1 | Pattern type<br>0 = Fixed pattern<br>2 = Random pattern<br>5 = Bit crowding pattern | 0,2,5 | |
| | | H2 | Pattern seed (for D1 = 0, 2)<br>two track number (for D1 = 5) | 0 ~ FFFFFFFF<br>01 ~ 78 | |
| | | H3 | Byte string for 1st track (for D1=5) | 0 ~ FFFFFFFF | |
| | | H4 | Byte string for 2nd track (for D1=5) | | |
| Byte length of record for TST3, 1 only<br>Example: LEN,980<br>Generate a record of 980 bytes | LEN,D1 | D1 | Byte length of record | 0 ~ (Function of memory size) | |
| Limitation<br>Example: LIMT,1,5<br>Report up to 5 compare errors for each record | LIMT,D1,D2 | D1 | Limit type<br>1 = Limit compare error printout | 1 | |
| | | D2 | Number of compare errors to be reported on each record (for D1=1) | D2 ≥ 0 (No limit if D2 = 0) | |

Note: Parameter of any directive beginning with a D means decimal, with an H means hexadecimal

## START PROCEDURE

1. Sense Switch Options, Monitor Directive Options, and Environmental Directives - Refer to DPM section of this manual.
2. Test Strategy Selection

| | Comprehensive Test | Functional Test | Random Exerciser Test | Utility Test |
|---|---|---|---|---|
| Recommended Application | Normal Usage | Solid Failure Detection and Specific Problem Analysis | Intermittent Failure Detection | Deskew adjustment<br>Threshold check<br>Capstan ramp adjustment<br>Compatibility check |
| Test Directive | TST0 | TST1 | TST2 | TST3 |
| Prerequisite | None | None | TST1 | TST1 |
| Optional Directives | LIMT | LIMT | LIMT | LIMT, LEN, DATA |
| Subtests | All function subtests (1 ~37) and random exerciser test | 40 subtests (see error messages for the test types) | Random selection of order sequence buffer length data. The identical operation is performed on each selected device in turn, then the next operation begins. | See program directive TST3 |
| Error Message Format | 1. Error No. DDDD LOC XXXX<br>2. Self-explanatory | Error No. DDDD LOC XXXX | Self-explanatory | Self-explanatory |

## PROGRAM TEST DESCRIPTION

The following is a description of the tests contained in the Magnetic Tape Test program.

TST1 Functional Test

The functional test performs a systematic test of all logic functions of the tape controller and all tape devices specified by the SYST directives. The functional test consists of a number of subtests which may be selected individually or in groups. The functional tests can be run at any density if 75 IPS. The tape creep test (TST1, 35) and the gap length timing test (TST1, 37) tolerance is set for 800 BPI.

When a fault has been detected, automatic error looping thru sense switch control is implemented whenever possible. Write and read retries will only be done in the data test (TST1, 33).

For a description of individual subtests refer to the Functional Subtest and Related Error Messages Section. Each subtest is preceded by a test description.

TST2 Random Exerciser Test

This test provides a means of operating a Magnetic Tape System with pseudo-random operation, order sequence, data pattern, I/O area, time delay, and record size for the purpose of detecting intermittent failures and exercising all tape units. The random exerciser test will report errors as they occur, but only as to the function that failed. No error looping is provided except for limited retries.

TST3 Utility Test Routines

The utility test routine allows the user to select a specific function and to control the data pattern (see DATA directive ) and the record length (see 'LEN' directive). The utility tests can be run at any density if 75 IPS.

1. Tape Test
This test allows the user to write, read forward, read backward, read forward and then backward, or write followed by rewind and read forward and read backward N records or until EOT is reached.

2. Deskew Test
This test is provided as a scoping aid during checking and adjusting the read/write skew. A pattern of all ones will be recorded as a continuous record. At EOT the tape will be rewound.

3. Sync On Character Test
This test is provided as a scoping aid by executing a unique I/O instruction (TDV) after the byte count specified in the test has been reached.

4. Compatibility and Noise Pattern Test
This test allows the user to write, read forward, read backward, or read forward and backward a predetermined incremented noise pattern.

5. Read/Space Test
This test allows the user to write, read, or space N records, with or without rewind. Only nonrecoverable transmission errors will cause error printout, backspace, and a halt.

## ORDER CODES

| | |
|---|---|
| X'01' | Write packed (binary) |
| X'02' | Read packed (binary) |
| X'05' | Write (binary) |
| X'06' | Read (binary) |
| X'0D' | Write decimal (BCD) |
| X'0E' | Read decimal (BCD) |
| X'13' | Rewind and interrupt |
| X'23' | Rewind off line |
| X'33' | Rewind |
| X'43' | Space record forward |
| X'4B' | Space record backward |
| X'53' | Space file forward |
| X'5B' | Space file backward |
| X'63' | Set erase |
| X'73' | Write tape mark |

## TDV STATUS

| | BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| MODEL | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 7362/72 | Rate Error | Write Permitted | Write Protect Error | End of File | Not Used | Load Point | End of Tape | Rewind On-Line |

## AIO STATUS

| | BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| MODEL | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 7362/72 | Rate Error | Device End | Write Protect Error | End of File | ← NOT USED → | | | |

## FUNCTIONAL SUBTESTS AND RELATED ERROR MESSAGES

### FAULT INDEX DESCRIPTION - FUNCTIONAL SUBTESTS

The fault index contains a brief description of each functional subtest and a list of associated error numbers with a brief description of each error. The subtests and error numbers are arranged in ascending sequence. The description of subtest NN is numbered NN00. The first two digits of the error number correspond to the associated subtest; the last two numbers correspond to the individual errors within the subtest.

TST1, 1 AIO, HIO, TIO, TDV Test - Check the ability of the 7-track mag tape system to correctly respond to the AIO, HIO and the TDV instructions. AIO will only check the no interrupt pending condition. Verify address recognition and status response to these instructions. Any error in this test may indicate a possible problem in the sub-controller area.

0101 AIO condition code error. No interrupt recognition expected.
0102 HIO condition code or status error. See printout.
0103 TIO condition code or status error. See printout.
0104 TDV condition code or status error. See printout.

TST1, 2 Invalid Order Test - Check the invalid order detection by issuing two SIO's with invalid order codes (X'0C', X'03). This test is designed to check order decoding, order-output and order-input phases in the controller and unusual end detection. The remaining byte count will be tested to verify that no data phases were executed. Check the ability of the HIO to reset UE condition.

0201 SIO for invalid order not accepted. Condition code error.
0202 SIO for invalid order status error. UE and no interrupt pending expected (read backward).
0203 HIO did not reset interrupt pending bit in status.
0204 SIO for invalid order not accepted. Condition code error.
0205 SIO for invalid order status error. UE and no interrupt pending expected (set correction).

TST1, 3 Erase Order Test - Check the execution of the first valid order. This test is designed to further check order decoding, order-output and order-input phases in the controller, and order termination without unusual end. The remaining byte count will be tested to verify that no data phases were executed. The status response will be tested.

0301 SIO condition code error on set erase.
0302 TIO status error on set erase. No UE or byte count reduction are expected. No data phases executed.

TST1, 7 Interrupt on UE, CE and AIO - Check the ability of the controller to generate an interrupt on unusual end and channel end using a read backward and the set erase order in that sequence. Check the execution of the AIO instruction. Verify that AIO and HIO can reset the interrupt pending condition. All status responses will be tested.

0701 SIO for invalid order condition code error (read bkw. UE set).
0702 No UE interrupt on invalid read backward with UE set.
0703 No UE set on AIO after invalid order or interrupt pending not reset after AIO.
0704 SIO for set erase condition code error (erase, CE set).
0705 No CE interrupt on erase with CE set.
0706 No interrupt pending set after HIO following the erase order.
0710 HIO status response error following AIO. UE or IP should not be set.
0711 TIO status response error following HIO. IP should not be set.

TST1, 8 I/O Interrupt Test - Check the ability of the IOP and CPU to interrupt the program whenever an interrupt call is generated by the controller. Verify proper operation of interrupt arm/disarm and enable/disable modes.

0801 TIO status response error after an invalid order. IP and UE should be set (read bkw, UE set with INT disarmed).
0802 TIO status response error after interrupt armed and disabled.
0803 No interrupt received on invalid order with UE set after interrupt armed and enabled.

TST1, 9 Command Chaining - Test the command chaining ability of the controller by issuing a set erase/read backward order sequence. Test the termination of the command chaining sequence by issuing a read-bkw/set erase order sequence. All status responses will be tested.

0901 SIO condition code error on command chaining order (erase read backward).
0902 No interrupt on command chaining erase, read backward.
0903 The last double word address is incorrect on command chaining. The address should be read backward.
0904 SIO condition code on command chaining order (read bkw, sense).
0905 No interrupt received on command chaining read bkw, erase.
0906 The last double word address is incorrect on command chaining. The address should be read backward.

TST1, 11 Rewind Test - Check the execution of a rewind on-line order. The test will verify that the tape is positioned at load point after completion of the rewind order. Check the execution of a rewind and interrupt order. This test will verify that the tape remains at load point and that the device initiates an interrupt request. Verify that an AIO and HIO instruction can reset the interrupt pending condition in the tape controller and the tape station. Verify that device end status is returned during the AIO. All status responses will be tested.

1101 TDV status error after rewind on line. No load point bit set.
1102 TIO status error after rewind and interrupt. No interrupt pend set.
1103 TIO status error after HIO on rewind with interrupt.
1104 TIO status error after rewind with interrupt. Inter/pend not set.
1105 AIO status error after rewind with interrupt. Device end not set.
1106 TIO status error after AIO. Interrupt pending not reset.
1107 TDV status error after rewind with interrupt. No load point set.

TST1, 12 Space Record and File Backward from BOT Test - Check the execution of space record and space file orders in the backward direction with tape positioned at load point. Verify that the controller responds with unusual end, end of file (TDV and AIO) and load point status. The test will check that the tape remains at load point. The byte count for all orders specified must remain unchanged.

1203 No interrupt on space backward at load point. (BC = 2)
1204 TIO or TDV status error on space bkw at load point. UE, load point, and BC = 2 expected.
1205 No interrupt received on space file backward at load point.
1206 TIO or TDV status error on space file bkw at load point. UE, load point, and no EOF expected.

TST1, 13 Write Tape Mark Test at BOT - Check the execution of a write tape mark order. The test will verify that tape can be moved off load point and that the order can be terminated with both controller and station returning to ready. If tape run-away, issue HIO. Rewind tape and test load point. End of file status will not be tested. The byte count for the order must remain unchanged.

1301 No interrupt on write tape mark at load point. (CE and BC = 2 set)
1302 TIO or TDV status error on write tape mark at load point. EOF and BC = 2 expected.

TST1, 14 Space Record Forward Test - Check the execution of a space forward order. The test will verify that tape can be moved off the load point and that the order can be terminated with both controller and station returning to ready. If tape run-away, issue HIO. Rewind tape and test for load point. End of file and unusual end status will not be tested. The byte count for the order must remain unchanged.

TST1, 14 (Continued)

1401 No interrupt received on write tape mark after rewind.
1402 No interrupt received on space forward over a tape mark at load point. (CE and BC = 2 set)
1403 Byte count on space fwd at load point error. Should be 2
1404 TIO status error on space fwd at load point. No error expected.

TST1, 15 Write Test (Byte 1 to 64) – Check the execution of write orders using X'FF' as data pattern and a starting at a byte of one up to a maximum byte count of 64. The test will verify that tape can be moved off the load point, that the order can be terminated with both controller and tape station returning to ready, that a data-output operation is actually performed, and that the byte count is always reduced to zero. Verify that incorrect length is not detected. Rewind tape and test for load point.
TE (transmission errors) not checked in this test.
Interrupt on ZBC checked in this subtest.

1501 TIO or TDV status error on write records 1-64 byte length. No incorrect length or UE expected, BC = 00.
1502 No interrupt received on writing 64 bytes with interrupt on ZBC.
1503 AIO or TIO status error on writing 64 bytes with interrupt on ZBC set.

TST1, 16 Read Test – Test the execution of read orders using a starting byte count of one up to a maximum count of 64. Write 64 records with a fixed byte count of 100 bytes (pattern = X'FF') and rewind tape. This test will check the response to a read forward operation (off load point, order transmission, data input operation, byte count reduced to zero). Rewind tape and test load point.
TE (Transmission errors) not checked in this test.

1601 TIO or TDV status error on writing 100 bytes all bits on. No incorrect length or UE expected, BC = 00.
1602 TIO or TDV status error on read forward 100 bytes all bits on with byte count 1-64. Incorrect length and no IZC expected.

TST1, 18 Write Read Data Test – Write N records with a fixed byte count and data pattern of X'FF'. Rewind tape and read N records in the forward direction. Verify that data can be recorded and read from each track.
TE (transmission errors) not checked in this test.

1801 TIO or TDV status error on writing 100 bytes all bits on, No incorrect length or UE expected, BC = 00.

TST1, 19 Write, Read Data Test (Data X'00' to X'20') – Write N records with a fixed byte count and the current data pattern data will be varied from X'00' thru X'20'. Rewind tape and read N records in the forward direction. Verify for each pass that only one track contains information and that all other tracks are zero. After each pass, loop on the data pattern which has caused an error and continue testing until a successful pass has been made.

1901 Write, Read forward, or information errors when saturating one track. 100 records of 100 bytes pattern 00, 01, 02, 04, 08, 10, 20.

TST1, 20 Set Erase-Write Test – Check the capability of the tape station to skip over an area on the tape by checking the delay between the start of the write order and the start of the data transfer.

2001 Erase time set too long. See message printout.
2002 Erase time set too short. See message printout.
2003 No interrupt on zero byte count occurred within 9ms.

TST1, 21 Write, Space FWD and BKW Test – Write N records with a fixed byte count. Rewind tape to load point. Space one record in the forward and backward direction. Space another record in the backward direction and check load point indicator. Space N records in the forward direction and then the reverse direction. Check all status response. Rewind to load point.

2101 TIO or TDV status error on writing 100 bytes all bits on.
2102 TIO or TDV status error on spacing forward over 100 bytes at load point.
2103 TIO or TDV status error on spacing backward over 100 bytes one record beyond load point. No UE or load point expected.
2104 TIO or TDV status error on spacing backward one record at load point. UE and load point expected.
2105 TIO or TDV status error on spacing forward over 100 bytes all bits on. No UE or error expected, BC = 00.
2106 TIO or TDV status error on spacing backward over 100 bytes all bits on. No UE or error expected, BC = 00.

TST1, 22 Write Tape Mark Test – Write N tape marks and verify that end of file status is reported after each order. All tape marks are read forward and space bkw.

2201 TIO or TDV status error on writing a tape mark. Tape mark and no UE expected.
2202 TIO or TDV status error on spacing backward over 100 tape marks. Tape mark and UE expected.
2203 TIO or TDV status error on reading forward over 100 tape marks. Tape mark and UE expected.
2204 Timeout error while command chaining set erase and space backward. No interrupt received from set erase or TM flag missing when spacing over a TM.
2205 TIO or TDV error when command chaining set erase and space backward over a tape mark. UE and TM expected.

TST1, 23 Write Tape Mark – Space File and Space Record Test – Write N tape marks and rewind to load point. Space file in the forward direction and verify end of file and no unusual end status. Space file backward and check end of file and no unusual end. Space file backward again and check end of file, beginning of tape and no unusual end. Verify all other status. Verify that unusual end and end of file status is reported when spacing or reading over a tape mark. Write N records followed by a tape mark. Verify space record in both directions.

2301 TIO or TDV status error on writing a tape mark. Tape mark and no UE expected.
2302 TIO or TDV status error on space file forward. Tape mark and no UE expected.
2303 TIO or TDV status error on space file backward. Tape mark and no UE expected.
2304 TIO or TDV status error on space file backward at load point. Load point, tape mark, and no UE expected.
2305 TIO or TDV status error on writing a record 100 bytes. No error expected, BC = 00.
2306 TIO or TDV status error on writing a tape mark. No error expected, tape mark.
2307 TIO or TDV status error on spacing backward over a tape mark. UE and tape mark expected.
2308 TIO or TDV status error on spacing forward over a tape mark. UE and tape mark expected.

TST1, 24 Tape Loop Test – Rewind with command chain. Write with data chain 27,000 words, loop back to rewind. This sequence is repeated 10 times in an effort to cause the tape to loop out in the vacuum columns.

2401 TIO or TDV status error after rewinding and writing a record of 27,000 words, looping 10 times. No error expected.

TST1, 26 Incorrect Length Test – Write a record and read in the forward direction using a byte count – 1, byte count + 1 for the read orders. Verify incorrect length and all other status indications. Suppress incorrect length feature in the IOP will also be tested.

2601 TIO or TDV status error on writing 96 bytes all bits on. No errors expected, BC = 00. No incorrect length.
2602 TIO or TDV status error on spacing a record backward. No error expected.

TST1, 26 (Continued)

2603 TIO or TDV status error on reading a record forward. No error expected. BC = 00. No incorrect length.
2604 TIO or TDV status error on spacing a 96 byte record backward. No error expected.
2605 TIO or TDV status error on reading a 96 byte record forward with a BC = 95 incorrect length, UE and BC = 00 expected.
2606 TIO or TDV status error on spacing a 96 byte record backward. No error expected.
2607 TIO or TDV status error on reading a 96 byte record forward with suppress inc length, BC = 97. Inc. length BC = 1, no UE expected.
2608 TIO or TDV status error on spacing bkw over record. No UE expected.
2609 TIO or TDV status error on reading forward a 96 byte record with suppress inc. length, BC = 95. Inc. length, BC = 0, no UE expected.

TST1, 27 Data Chaining Test - Test the data chaining capability of the IOP using write and read orders.

2701 TIO or TDV status error on writing 2 bytes data chain 94. No errors expected, BC = 00.
2702 TIO or TDV status error on spacing backward over record (2 bytes data chain 94). No error expected.
2704 TIO or TDV status errors on reading forward 48 bytes data chain 48 bytes. No error expected, BC = 00.
2705 Information error on reading a record fwd 48 bytes data chain 48.

TST1, 28 Byte Boundary Test - This test performs read and write operations from all possible memory boundaries.

2801 TIO or TDV status error when writing from WA, WA+1 byte, WA+2 bytes, WA+3 bytes.
2802 TIO or TDV status error on spacing backward. No error expected.
2804 TIO or TDV status error when reading fwd into WA, WA+1 byte, WA+2 bytes, WA+3 bytes.
2805 Information error when reading fwd into WA, WA+1 byte, WA+2 bytes, WA+3 bytes.
2806 TIO or TDV status error on writing a record 4,16,32,64....bytes in length.
2807 TIO or TDV status error on spacing bkw over 4,16,32,64,128.... bytes in length.
2809 TIO or TDV status error on reading a record fwd 4,16,32,64.... bytes in length.
2810 Information error on reading forward 4,16,32,64....bytes.

TST1, 29 Decimal (BCD) Mode Data Test - This test will write data using translation. The data will be read and the information verified with and without translation. Transmission errors will be expected on reading without translation.

2901 TIO or TDV status error when writing the BCD character set. No error expected.
2902 TIO or TDV status error when spacing backward over BCD record. No error expected.
2903 TIO or TDV status error when reading the BCD character set. No error expected.
2904 Information error on the BCD character set record.
2905 TIO or TDV status error when spacing over the BCD character set.
2906 TIO or TDV status error when reading the BCD character set without translation. Transmission errors expected.
2907 Information error on BCD record read without translation.
2908 TIO or TDV error when writing a 4 byte record checking zero translation. No error expected.
2909 TIO or TDV error when spacing bkw over zero translation record.
2911 TIO or TDV error when reading 4 byte zero translation record. No error expected.
2912 Information error on zero translation record. Information expected X'F0F0F0F0'.

TST1, 30 Binary Mode Data Test - This test will write data using the binary mode. The data will be read and the information verified with and without translation. Transmission errors will be expected on reading with translation.

3001 TIO or TDV status error when writing a binary record X'00'-X'3F'.
3002 TIO or TDV status error when spacing bkw over binary record.
3003 TIO or TDV status error when reading a binary record X'00'-X'3F'.
3004 Information error on reading binary record X'00'-X'3F'.
3005 TIO or TDV status error spacing bkw over binary record.
3006 TIO or TDV status error when reading binary record with BCD. Transmission error expected.
3007 Information error when reading binary record with BCD.

TST1, 31 Packed Binary Data Test - This test will write data X'00' - X'FF' using the packed binary mode. The data will be read and verified. This subtest will be bypassed if not applicable to the system.

3101 TIO or TDV status error when writing a packed binary record X'00' - X'FF'. No error expected.
3102 TIO or TDV status error when spacing bkw over a packed binary record X'00' - X'FF'.
3103 TIO or TDV status error when reading a packed binary record X'00' - X'FF'.
3104 Information error when reading a packed binary record.
3105 TIO or TDV status error writing packed binary record of 6,7,8 bytes to test the packed binary end condition.
3106 TIO or TDV status error when spacing bkw over packed binary record.
3107 TIO or TDV status error reading a packed binary record of 6,8,9 bytes to test the end condition.
3108 Information error on packed binary record checking end condition.

TST1, 32 LRC Test - Check the ability to set all bits in the LRC character. The LRC will be tested in the packed binary, binary, and decimal (BCD) mode. Any section not applicable to the unit being tested will be bypassed.

3201 TIO or TDV status error writing a packed binary record to set one bit at a time in the LRC character.
3202 TIO or TDV status error spacing bkw over packed binary record.
3203 TIO or TDV status error reading a packed binary record to set one bit at a time in the LRC character.
3204 Information error on packed binary record that sets a bit at a time in the LRC character.
3205 TIO or TDV status error writing a binary record to set one bit at a time in the LRC character.
3206 TIO or TDV status error spacing backward over a binary record.
3207 TIO or TDV status error reading a binary record to set one bit at a time in the LRC character.
3208 Information error on binary record that sets a bit in the LRC.
3209 TIO or TDV status error writing a BCD record with a blank LRC, then sets a particular bit and the parity bit in the LRC char.
3210 TIO or TDV status error spacing bkw over BCD record.
3211 TIO or TDV status error reading the BCD record with a blank LRC, then sets a particular bit and the parity bit in the LRC char.
3212 Information error reading a BCD record with a blank LRC, and particular bits in the LRC character.

TST1, 33 Data Test Noise Patterns and Bit Crowding - This test will write and read variable data patterns. The sequence will always be write, space reverse and read forward. The record size will be varied after each record. Noise sensitive and bit crowding data pattern will be used. Write and read retries will be allowed.

3301 TIO or TDV status error on writing an incremented record with saturated tracks and noise pattern.
3302 TIO or TDV status error on space backward over an incremented record with saturated tracks and noise patterns.
3303 TIO or TDV status error on reading forward an incremented record with saturated tracks and noise patterns.
3304 Information error on reading forward an incremented record with saturated tracks and noise patterns.

TST1, 34 Ready - Busy Test - Check the busy condition after issuance of an order. The test will also attempt to issue an SIO to a busy controller and to a ready controller and a busy station.

TST1, 34 (Continued)

3401 TIO error. Device should be busy while writing 1000 bytes.
3402 No interrupt received after writing 1000 bytes.
3403 TIO or TDV status error on writing a 1000 byte record.
3404 TIO error. Controller should be busy while reading 1000 bytes.
3405 No interrupt received after reading a record bkw. with 1000 bytes.
3406 SIO error. Controller should be busy on initiating rewind.
3407 TIO error. Device should be busy on rewinding.

TST1, 35 Tape Creep Test - This test will write one record followed by a set erase order and another write order. A space record backward and rewrite sequence will now be repeated N times. After reading and verifying the data of the first record, read the second record and compute the delay between the start of the read order and the start of the data transfer. The direction of the creep will be determined by comparing the delay to the original value. The tolerance is set for 800 BPI if 75 IPS.

3501 TIO or TDV status error on writing a 96 byte record.
3502 TIO or TDV status error when writing a 12 byte record.
3503 TIO or TDV status error when writing a 12 byte record.
3504 TIO or TDV status error when spacing backward over a 12 byte record.
3505 TIO or TDV status error spacing backward over 96 bytes.
3506 TIO or TDV status error reading a 96 byte record.
3507 Information error reading a 96 byte record.
3508 Tape creep tolerance exceeded in the tape creep test.
3509 Tape creep negative in the tape creep test.

TST1, 36 Erase Verification Test - This test will test the erase order by rewinding tape and then writing N one byte records. The records are followed by a tape mark. After a rewind, write one record, set erase, and write one record. The tape is rewound. The records are counted to verify the erase order execution.

3601 The erase order did not remove the correct number of records when verifying the erase order.

TST1, 37 Gap Length Timing Test - This routine verifies gap timing and is intended as a scoping aid for adjusting the forward and reverse ramp. The test can only be run on a system with a real time clock. The tolerance is set for 800 BPI if 75 IPS.

3701 TIO or TDV status error writing 12 bytes in the I.R.G. Test.
3702 TIO or TDV status error on spacing backward over 12 bytes.
3703 TIO or TDV status error writing 12 bytes in the I.R.G. test.
3704 TIO or TDV status error on spacing backward over 12 bytes.
3705 I.R.G. time is incorrect. See printout.

TST1, 38 End of Tape Test - This test will continue to write N records until the end of tape indicator is detected. One additional record will be recorded and the EOT condition will be verified again. Two records will be spaced in the backward direction. After the second space, the EOT indicator should be reset. The tape will be rewound.

3801 TIO or TDV error writing 1000 bytes in the end of tape test.
3802 TIO or TDV error writing 1000 bytes beyond EOT indication. End of tape flag should be set.
3803 TIO or TDV status error spacing backward over 1000 bytes at EOT. EOT flag should be set.
3804 TIO or TDV status error spacing bkw. over 1000 bytes near EOT. EOT flag should be reset.

TST1, 40 Operator Control Panel Test - This test will check every switch on the operator control panel in the sequence specified by the program and verify the write protect feature.

4001 Status error on writing a record designating unit 0,1,2,3,4,5,6,7.
4002 Status error spacing bkw. with unit designation 1,2,3,4,5,6,7.
4004 Status error on reading fwd. with designation unit 0,1,2,3,4,5,6,7.
4005 Information error reading fwd. record from unit 0,1,2,3,4,5,6,7.
4006 Status error when trying to write on a unit with the write ring removed. A write protect is expected.
4007 Status error when trying to write a tape mark with the write ring removed. A write protect is expected.
4008 No interrupt was received when the attention button was set by the operator.
4009 Status error on rewind and put off line. The device should be manual and the controller ready.
4010 TDV status incorrect. Load point and ready expected.
4013 The density dial is set incorrectly or the actual density of the 1000 byte record was incorrect.
4014 TIO or TDV status error on writing a 96 byte record with the density dial set to a particular density.
4015 TIO or TDV status error on spacing backward over a record with the density dial set at a particular density.
4016 TIO or TDV status error reading 96 bytes with the density dial set at a particular density.
4017 Information error on the 96 byte record read with the density dial set at a particular density.

## TST2 RANDOM EXERCISER TEST

This test provides a means of operating a magnetic tape system with pseudo-random operation, order sequence, data pattern, I/O area, time delay, and record size for the purpose of detecting intermittent failures and exercising all tape units.

The random exerciser test will report errors as they occur, but only as to the function that failed. No error looping is provided except for limited retries.

Parameters D1 = Number of cycles, set to 1000 if 0
D2 = Number of error retries

From the random seed, the following masks are used to get type of operation, word size of record, and time delay in milliseconds.

X'00003FF0' To get random record word size
X'001F0000' To get random time delay in milliseconds
X'0000000F' To get random operation set

Random Operation Sets

| | |
|---|---|
| 0 | Write, write, write, write, write |
| 1 | Write, write, write, write, space bkw |
| 2 | Write, write, write, space bkw, space bkw |
| 3 | Write, write, write, space bkw, read fwd |
| 4 | Write, write, space bkw, read fwd, space bkw |
| 5 | Write, write, space bkw, space bkw, read fwd |
| 6 | Write, write, space bkw, space bkw, space fwd |
| 7 | Write, space bkw, read fwd, write, write |
| 8 | Write, space bkw, read fwd, write, space bkw |
| 9 | Write, space bkw, write, space bkw, read fwd |
| A | Write, space bkw, read fwd, space bkw, write |
| B | Write, space bkw, read fwd, space bkw, read fwd |
| C | Write, space bkw, space fwd, write, write |
| D | Write, space bkw, write, space bkw, space fwd |
| E | Write, space bkw, read fwd, space bkw, read fwd |
| F | Write, space bkw, space fwd, space bkw, read fwd |

## TST3 UTILITY TESTS

The utility test routine allows the user to select a specific function and to control the data pattern (see data directive) and the record length (see 'LEN' directive).

Parameters D1 = Utility test selection
D1 = 1 Tape test
D1 = 2 Deskew test
D1 = 3 Sync on a character test
D1 = 4 Compatibility and noise pattern test
D1 = 5 Read/space test
D2 = Operations requested according to test
D3 = Parameter requested according to test
D4 = Parameter requested according to test

### TST3, 1 Tape Test

This test allows the user to write, read forward, space backward, read forward and space backward, or write followed by rewind, read forward and space backward N records or until EOT is reached.

Parameters D1 = 1 Tape Test
D2 = 0 Write, rewind, read forward, space backward D3 records
  1 Write D3 records
  2 Read forward D3 records
  3 Space backward D3 records
  4 Read forward and space backward D3 records in sequence
  8 Write, rewind, read fwd, space bkw D3 records (BCD)
  9 Write D3 records (BCD)
  10 Read fwd D3 records (BCD)
  12 Read fwd, space bkw D3 records (BCD)
D3 = Number of records to be written or read. If D3=0 continue until EOT or BOT is reached.
D4 = Delay in milliseconds between operation sets

Example TST3, 1, 1, 1000, 5
Write 1000 records with a 5 millisecond delay after each write operation.

### TST3, 2 Deskew Utility Test

This test is provided as a scoping aid during checking and adjusting the read/write skew. A pattern of all ones will be recorded as a continuous record. At EOT the tape will be rewound.

Parameter D1 = 2 Deskew test
D2 = 0, 1 Write until EOT is reached and rewind
  2 Read forward until EOT and rewind
  3 Space backward until BOT is reached
  4 Read fwd until EOT, space bkw until BOT, no rewinds
  5 Capstan slippage exerciser
D3 = Not used
D4 = Not used

Example TST3, 2, 2
Read forward until EOT and rewind.

### TST3, 3 Sync on a Character Utility Test

This test is provided as a scoping aid by executing a unique I/O instruction (TDV) after the byte count specified in the test has been reached.

Parameters D1 = 3 Sync on a character test
D2 = 1 Read forward and space record backward
D3 = Byte to sync on
D4 = Delay in milliseconds between syncs

Example TST3, 3, 1, 375, 10
Read forward 375 bytes, signal (TDV) and delay 10 milliseconds. Space backward.

### TST3, 4 Compatibility and Noise Pattern Test

This test allows the user to write, read forward, read backward, or read forward and backward a predetermined incremented noise pattern.

Parameters D1 = 4 Compatibility and noise pattern test
D2 = 0, 1 Write, space backward, and read forward all records
  2 Space forward, space backward, read forward all records
  3 Read forward, space backward, space forward all records
  4 Read forward all records
  5 Write all records
D3 = Not used
D4 = Not used

Example TST3, 4, 5
Write all records.

### TST3, 5 Read/Space Test

This test allows the user to read or space N records, with or without rewind. Only non-recoverable transmission errors will cause error printout, backspace, and a halt.

Parameters D1 = 5 Read/space test
D2 = 0 Rewind and read fwd N records
  1 Rewind and space fwd N records
  2 Don't rewind, read fwd N records
  3 Don't rewind, space fwd N records
  4 Don't rewind, space bkw N records
  8 Rewind, read fwd N records with even parity, decimal (BCD)
  10 Don't rewind, read fwd with even parity, decimal (BCD)
D3 = Number of records to read or space
D4 = 0 Don't printout record
  1 Printout record in error
  2 Printout Nth record

Example TST3, 5, 0, 100, 1
Rewind, read 100 records. Printout error record.

# Section 12

# SIGMA 5 - 9
# COMPREHENSIVE LINE PRINTER
# TEST (744X - 745X)

## PROGRAM NO. 706167

12

## Section 12

## CONTENTS

Page

Subject Model . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 12-1
Required Equipment . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 12-1
Program Prerequisites . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 12-1
General Operating Procedures . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 12-1
Directives . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 12-2
Start Procedure . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 12-4
Program Test Description . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 12-5
Order Codes . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 12-5
Normal TDV Status . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 12-6
Test Mode TDV Status . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 12-6
AIO Status . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 12-6
Format Codes for Format Operations . . . . . . . . . . . . . . . . . . . . . . . . 12-7
Diagnostic Control Byte (7441 Only) . . . . . . . . . . . . . . . . . . . . . . . . 12-8
Diagnostic Control Byte (7446 Only) . . . . . . . . . . . . . . . . . . . . . . . . 12-8
Functional Subtests and Related Error Messages . . . . . . . . . . . . . . . . . 12-9

# 12. SIGMA 5–9 COMPREHENSIVE LINE PRINTER TEST (744X/745X)

**SUBJECT MODEL** -- Line Printer Model Numbers 3451, 7440/7445, 7441, 7446, 7450, 7442

**REQUIRED EQUIPMENT** -- Minimum Memory Size: 16K; Input Device: Card Reader, Paper Tape Reader or Magnetic Tape Unit; Output Device: Keyboard Printer or Line Printer

## PROGRAM PREREQUISITES

The vertical format tape must be removed when running the function test (TST1) on model 7441, 7446, and 7442

## GENERAL OPERATING PROCEDURES

General operating procedures of the Xerox Sigma 5 through 9 Diagnostic Program Monitor (DPM) apply to this program.

# 12. SIGMA 5–9 COMPREHENSIVE LINE PRINTER TEST (744X/745X)

**DIRECTIVES** - directives are entered after a "!" is typed out

| Name | Format | Parameter | | | |
|---|---|---|---|---|---|
| | | ID | Definition | Value Range | Standard Value (default) |
| Program Directives - Environmental Directives | | | | | |
| System Environment | SYST, D1, X2, X3 | D1<br>X2<br>X3 | Device model number<br>Revision number of controller<br>IOP and Device address | 7440, 7441, 7442, 7445 7446, 7450, 3451<br>0 for all printers<br>01 ~ 1F7F | 7441 |
| Program Directives - Testing Directives | | | | | |
| Comprehensive Test (all functional tests, 1 ~ 73, and random exerciser test) | TST0 | | | | |
| Functional Test | TST1 [,D1 [,D2]] | D1<br>D2 | The first subtest to be executed<br>Last subtest to be executed | 0 (all subtests) ~ 73 | 0 |
| Random Exerciser Test | TST2, D1 | D1 | Number of cycles to be performed | D1 > 0 | 1 |
| Utility Test | TST3, D1, D2, D3, D4 | D1 | = 0 Hammer registration<br>D2=Line count | D2 Not entered = Print continuously<br>D2=0 Print 1 line<br>D2≠0 Print D2 lines | |
| | | | = 1 Checkerboard pattern<br>D2=Line count | D2 Not entered=Print continuously<br>= 0 Print 1 line<br>≠ 0 Print D2 lines | |
| | | | = 2 Ripple pattern<br>D2=Line count | D2 Not entered=Print continuously<br>= 0 Print 1 line<br>≠ 0 Print D2 lines | |
| | | | = 3 Printer speed test<br>D2=Character set count<br>7450 ONLY | 7450 Only<br>1 ≤ D2 ≤ 63 | Size of character sets:<br>7440/45=40<br>7441 =42<br>7446 =42<br>7450 =44<br>7442 =42<br>3451 =40 |
| | | | = 4 Printer load test<br>D2=Line count | D2 Not entered=Print continuously<br>= 0 Print 1 line<br>≠ 0 Print D2 lines | |
| | | | = 5 Broadside pattern<br>D2=Line count | D2 Not entered=Print continuously<br>= 0 Print 1 line<br>≠ 0 Print D2 lines | |
| | | | = 6 Selectable pattern/position (Data determined by DATA directive)<br>D2=Number of lines to be printed<br>D3=Number of lines to be printed as a group<br>D4=Number of blank lines between groups | D2 Not entered=Print continuously<br>D2=0 Print 1 line<br>D2≠0 Print D2 lines<br>D3=0 Print continuous lines<br>≠ 0 No. lines/group<br>0 ≤ D4 | |
| | | | = 7 Space lines (space orders are issued to each of the 15 possible positions in sequence) | | |
| | | | = 8 Channel search<br>D2=Channel number | D2 Not entered=Skip to all channels in sequence<br>0 ≤ D2 ≤ 7 | |
| | | | = 9 All Utility tests in sequence<br>D2=Line count | D2=0 Print 1 line<br>D2≠0 Print D2 lines | |
| | | | = 10 Line printer cleaner<br>D2=Line count | D2=0 Print 1 line<br>D2≠0 Print D2 lines | |

**DIRECTIVES** (Continued)

| Name | Format | Parameter | | | |
|---|---|---|---|---|---|
| | | ID | Definition | Value Range | Standard Value (default) |
| Program Directives – Optional Directives | | | | | |
| Pattern selection (for Utility Test)(TST3, 6) | DATA, D1, D2, D3, D4 | D1 | = 4 Variable pattern | -4 | |
| | | D2 | Starting column | 1 ~ 132 | |
| | | D3 | Ending column | 1 ~ 132 | |
| | | D4 | EBCDIC character string<br>(up to 4 EBCDIC characters) | Any printable codes<br>00 ~ FF<br>(F0F1F2F3) | |
| Limitation of program parameters | LIMT, D1, D2, D3 | D1 | = 1 Limit compare error printouts<br>D2=Maximum number of compare error printouts | 1, 2<br>0 ≤ D2 | |
| | | | = 2 Limit delay time<br>D2=Minimum delay time<br>D3=Maximum delay time | -6<br>0 ≤ D2 ≤ D3 | |

Note: Parameter of any directive beginning with a D means decimal; with an H means hexadecimal.

### START PROCEDURE

1. Sense Switch Options, Monitor Directive Options, and Environmental Directives - Refer to DPM section of this manual.
2. Test Strategy Selection

| | Comprehensive Test | Functional Test | Random Exerciser Test | Utility Test |
|---|---|---|---|---|
| Recommended Application | Normal Usage | Solid Failure Detection and Specific Problem Analysis | Intermittent Failure Detection | Print Quality Verification |
| Test Directive | TST0 | TST1 | TST2 | TST3 |
| Prerequisite | None | None | TST1 | TST1 |
| Optional Directives | LIMT | LIMT | LIMT | LIMT, DATA |
| Subtests | All functional subtests (1 ~ 73) and random exerciser test | 73 subtests (see error messages for the test types) | Prints a predetermined set of test patterns | Prints one or all of predetermined patterns |
| Error Message Format | 1. ERROR NO. DDDD LOC XXXX<br>2. Self-explanatory | ERROR NO. DDDD LOC XXXX | Self-explanatory | Self-explanatory |

3. System reset should normally be used in order to insure the resetting of controller test mode logic.

## PROGRAM TEST DESCRIPTION

The following is a description of the tests contained in the Comprehensive Line Printer test program.

### TST0

The directive selects the comprehensive test consisting of the functional test (subtests 1-73) and the random exerciser test.

Parameters: None

Example: TST0

1. The functional test will be run on the printer in sequence (subtest 1 through 73).
2. The random exerciser will run until six cycles have been completed. If a failure is encountered, an error message is printed and the exercising continues.

### TST1

The directive selects the entire functional test (no parameters entered) or selects one or more contiguous functional subtests.

Parameters: D1 - First functional subtest
D2 - Last functional subtest

where $0 < D1 \leq D2 \leq 73$

Examples: Run all functional subtests.

TST1, 35, 49

Run functional subtests 35 through 49.

### TST2

The directive selects the random exerciser test.

Parameters: D1 - Number of cycles to be executed by random exerciser

Example: TST2, 3

The random exerciser will run until three cycles have been completed.

### TST3

The utility test routine allows the user to select a specific utility function and/or print patterns which aid the operator in printer adjustments.

Parameters: D1 - Utility test selection
D2 - Defined by the utility test selected
D3 - Defined by the utility test selected
D4 - Defined by the utility test selected

D1 = 0 Hammer registration
D2 = Line count

Generates pattern of broadside character 'E' (same character in all positions) continuously as a reference in checking printer hammer alignment

D1 = 1 Checkerboard pattern
D2 = Line count

Generates a worst-case pattern to expose ghost character printing. The pattern consists of alternating character 'E' and blanks.

TST3(Continued)

D1 = 2 Ripple pattern
D2 = Line count

Generates a pattern consisting of all characters per line, each succeeding line having the characters shifted one position to the left

D1 = 3 Printer speed test
D2 = Character count (7450 only)

A 36-line pattern of characters is printed to produce maximum print rate. The average time to print and upspace is calculated and the printer speed is determined and reported.

D1 = 4 Printer load test
D2 = Line count

Generates a pattern of an increasing number of character 'E' each line until 132 positions are printed, then a decreasing number of character 'E' each line

D1 = 5 Broadside pattern
D2 = Line count

Generates a 64-line pattern of all printable characters broadside

D1 = 6 Selectable pattern/position
D2 = Line count
D3 = Group/line count
D4 = Group/space count

Generates a selectable character and position(s) pattern

D1 = 7 Space lines
D2 = Unused

Space orders are issued to each of the 15 possible positions in sequence.

D1 = 8 Channel search
D2 = Channel number

Channel searches are issued to the operator-specified channel.

D1 = 9 Utility test
D2 = Line count

Run all utility tests in sequence

D1 = 10 Line Printer Cleaner
D2 = Line count

Print ripple pattern with inhibit upspace

Examples: TST3, 7

Space orders are issued to each of the 15 possible positions in sequence.

TST3, 8, 4

Exercise the printer VFU control. Channel 4 is to be searched.

## ORDER CODES

| | |
|---|---|
| X'01' | Print a line |
| X'41' | Print a line - interrupt at data transmission complete |
| X'03' | Format order (see format codes) |
| X'43' | Format order - interrupt at data transmission complete (see format codes) |
| X'05' | Print with format |
| X'45' | Print with format - interrupt at data transmission complete |
| X'04' | Diagnostic sense (7441, 7442 and 7446) |
| X'44' | Diagnostic sense (7441, 7442 and 7446) - interrupt at data transmission complete |
| X'07' | Diagnostic control (7441, 7442 and 7446) (see diagnostic control bytes) |
| X'47' | Diagnostic control (7441, 7442 and 7446) - interrupt at data transmission complete (see diagnostic control bytes) |

## NORMAL TDV STATUS

TDV SET 1

| MODEL | BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 7440/7445<br>3451 | Not Used | Print Fault | Paper Low | Top of Page | Paper Moving | Paper Runaway | Not Used | Not Used |
| 7450 | Not Used | Typeline in Odd Sector = 1 | Paper Low | Top of Page | Paper Moving | Paper Runaway | Print Order Expected | Maintenance Panel Used |
| 7441<br>7442 | Not Used | Buffer Parity Error | Paper Low | Top of Page | Interlock | Paper Runaway | IO Parity Error | Hammer Drive Supply Low |
| 7446 | Not Used | Recovery Mode 1 | Recovery Mode 2 | Top of Page | Buffer Parity Error | Code Disc Parity Error | IO Parity Error | Print Error |

## TEST MODE TDV STATUS

| MODEL/SET | BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 7441/7446/7442<br>Printer States/Control<br>Set 2 | State A | State B | State C | State D | State E | Print Complete | Buffer Scan Complete | Control Byte Received |
| 7441/7446/7442<br>Format Register<br>Set 3 | Search | Space | Inhibit Upspace | Line Marker Clock | Format Register Bit 4 | Format Register Bit 5 | Format Register Bit 6 | Format Register Bit 7 |
| 7441/7442<br>Paper Motion Control<br>Set 4 | PAPDR | PSCD | PAPSE | LMCLK | ECLB1 | ECLB2 | EBRB1 | EBRB2 |
| 7446<br>Paper Motion Control<br>Set 4 | Paper Move | Paper Stop | End Hi Speed Boost | End Low Speed Boost | End Brake Boost | Shift | End Format Scan | Paper Clamp |
| 7441/7446/7442<br>Address Counters<br>Set 5 | X'AD0' | X'AD1' | X'AD2' | X'AD3' | X'AD4' | X'AD5' | X'AD6' | X'AD7' |
| 7446<br>Vertical Format Channel<br>Set 6 | VFUCH0 | VFUCH1 | VFUCH2 | VFUCH3 | VFUCH4 | VFUCH5 | VFUCH6 | VFUCH7 |
| 7441/7446/7442<br>Set 7 | ◄—— NOT USED ——► | | | | | | | |
| 7446<br>Buffer Output Register<br>Set 8 | SR0 | SR1 | SR2 | SR3 | SR4 | SR5 | SR6 | SR7 |

## AIO STATUS

For Model 7441/7446/7440/7445/7450

| BITS | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| NOT USED | DATA TRANSMISSION COMPLETE INTERRUPT | ◄—— NOT USED ——► | | | | | |

## FORMAT CODES FOR FORMAT OPERATIONS

### MODEL 7441/7446 and 7442

| | |
|---|---|
| X'60' | Inhibit automatic space after print |
| X'C0' | Space 0 lines |
| X'C1' | Space 1 line |
| X'C2' | Space 2 lines |
| X'C3' | Space 3 lines |
| X'C4' | Space 4 lines |
| X'C5' | Space 5 lines |
| X'C6' | Space 6 lines |
| X'C7' | Space 7 lines |
| X'C8' | Space 8 lines |
| X'C9' | Space 9 lines |
| X'CA' | Space 10 lines |
| X'CB' | Space 11 lines |
| X'CC' | Space 12 lines |
| X'CD' | Space 13 lines |
| X'CE' | Space 14 lines |
| X'CF' | Space 15 lines |
| X'E0' | Space 0 lines and inhibit automatic upspace |
| X'E1' | Space 1 line and inhibit automatic upspace |
| X'E2' | Space 2 lines and inhibit automatic upspace |
| X'E3' | Space 3 lines and inhibit automatic upspace |
| X'E4' | Space 4 lines and inhibit automatic upspace |
| X'E5' | Space 5 lines and inhibit automatic upspace |
| X'E6' | Space 6 lines and inhibit automatic upspace |
| X'E7' | Space 7 lines and inhibit automatic upspace |
| X'E8' | Space 8 lines and inhibit automatic upspace |
| X'E9' | Space 9 lines and inhibit automatic upspace |
| X'EA' | Space 10 lines and inhibit automatic upspace |
| X'EB' | Space 11 lines and inhibit automatic upspace |
| X'EC' | Space 12 lines and inhibit automatic upspace |
| X'ED' | Space 13 lines and inhibit automatic upspace |
| X'EE' | Space 14 lines and inhibit automatic upspace |
| X'EF' | Space 15 lines and inhibit automatic upspace |
| X'F0' | Skip to channel 0 (bottom of page) |
| X'F1' | Skip to channel 1 (top of page) |
| X'F2' | Skip to channel 2 |
| X'F3' | Skip to channel 3 |
| X'F4' | Skip to channel 4 |
| X'F5' | Skip to channel 5 |
| X'F6' | Skip to channel 6 |
| X'F7' | Skip to channel 7 |

### MODEL 7446

| | |
|---|---|
| X'D0' | Skip to channel 0 (BOP) and inhibit automatic upspace |
| X'D1' | Skip to channel 1 (TOP) and inhibit automatic upspace |
| X'D2' | Skip to channel 2 and inhibit automatic upspace |
| X'D3' | Skip to channel 3 and inhibit automatic upspace |
| X'D4' | Skip to channel 4 and inhibit automatic upspace |
| X'D5' | Skip to channel 5 and inhibit automatic upspace |
| X'D6' | Skip to channel 6 and inhibit automatic upspace |
| X'D7' | Skip to channel 7 and inhibit automatic upspace |

### MODEL 7440/7445 and 3451

| | |
|---|---|
| X'60' | Inhibit automatic space after print |
| X'C0' | Space 0 lines |
| X'C1' | Space 1 line |
| X'C2' | Space 2 lines |
| X'C3' | Space 3 lines |
| X'C4' | Space 4 lines |
| X'C5' | Space 5 lines |
| X'C6' | Space 6 lines |
| X'C7' | Space 7 lines |
| X'C8' | Space 8 lines |
| X'C9' | Space 9 lines |
| X'CA' | Space 10 lines |
| X'CB' | Space 11 lines |
| X'CC' | Space 12 lines |
| X'CD' | Space 13 lines |
| X'CE' | Space 14 lines |
| X'CF' | Space 15 lines |
| X'E0' | Space 0 lines and inhibit automatic upspace |
| X'F0' | Skip to channel 0 (bottom of page) |
| X'F1' | Skip to channel 1 (top of page) |
| X'F2' | Skip to channel 2 |
| X'F3' | Skip to channel 3 |
| X'F4' | Skip to channel 4 |
| X'F5' | Skip to channel 5 |
| X'F6' | Skip to channel 6 |
| X'F7' | Skip to channel 7 |

### MODEL 7450

| | |
|---|---|
| X'60' | Inhibit automatic space after print |
| X'C0' | Space 0 lines |
| X'C1' | Space 1 line |
| X'C2' | Space 2 lines |
| X'C3' | Space 3 lines |
| X'C4' | Space 4 lines |
| X'C5' | Space 5 lines |
| X'C6' | Space 6 lines |
| X'C7' | Space 7 lines |
| X'E0' | Space 0 lines and inhibit automatic upspace |
| X'E1' | Space 1 line and inhibit automatic upspace |
| X'E2' | Space 2 lines and inhibit automatic upspace |
| X'E3' | Space 3 lines and inhibit automatic upspace |
| X'E4' | Space 4 lines and inhibit automatic upspace |
| X'E5' | Space 5 lines and inhibit automatic upspace |
| X'E6' | Space 6 lines and inhibit automatic upspace |
| X'E7' | Space 7 lines and inhibit automatic upspace |
| X'F0' | Skip to channel 0 (bottom of page) |
| X'F1' | Skip to channel 1 (top of page) |

### DIAGNOSTIC CONTROL BYTE (7441 ONLY)

| BIT | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | MEANING |
|---|---|---|---|---|---|---|---|---|---|
| | 1 | - | - | - | - | - | - | - | 0 = Normal<br>1 = Step mode (state register advances on TDV) |
| | - | 1 | - | - | - | - | - | - | 0 = Normal<br>1 = Inhibit print (disable hammers and paper motion) |
| | - | - | 1 | - | - | - | - | - | Unassigned |
| | - | - | - | - | 1 | - | - | - | 0 = Normal<br>1 = Inhibit buffer clear |
| | - | - | - | 1 | - | - | - | - | 0 = Input buffer<br>1 = Input code disk |
| | - | - | - | - | - | X | X | X | Select TDV states 1 through 8 |

### DIAGNOSTIC CONTROL BYTE (7446 ONLY)

| BIT | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | MEANING |
|---|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | - | - | - | - | - | Normal |
| | 1 | X | 0 | - | - | - | - | - | Step mode (state register advances on TDV) |
| | X | 1 | 0 | - | - | - | - | - | Inhibit print (disable hammers and paper motion) |
| | 0 | 0 | 1 | - | - | - | - | - | Force print error during printing in state C |
| | 0 | 1 | 1 | - | - | - | - | - | Force code disk parity error during printing in state C |
| | 1 | 0 | 1 | - | - | - | - | - | Force buffer parity error during printing in state C |
| | 1 | 1 | 1 | - | - | - | - | - | Force IO parity error on data out in state B or state D |
| | - | - | - | 1 | - | - | - | - | 0 = Input buffer<br>1 = Input code disk |
| | - | - | - | - | 1 | - | - | - | 0 = Normal<br>1 = Inhibit buffer clear |
| | - | - | - | - | - | X | X | X | Select TDV status set 1 through 8 |

## FUNCTIONAL SUBTESTS AND RELATED ERROR MESSAGES

### FAULT INDEX DESCRIPTION - FUNCTIONAL SUBTESTS

The fault index contains a brief description of each functional subtest and a list of associated error numbers with a brief description of each error. The subtests and error numbers are arranged in ascending sequence. The description of subtest NN is numbered NN00. The first two digits of the error number correspond to the associated subtest; the last two numbers correspond to the individual errors within the subtest.

NOTE

All functional tests for 7441 also applies for 7442 and all functional tests for 7440/7445 also applies for 3451.

TST1, 1 HIO, TIO, TDV and AIO instruction recognition (7440/7445, 7441, 7446, 7450). HIO, TIO, TDV and AIO instructions are issued and condition codes status tested.

0101 HIO instruction condition codes or status error.
0102 TIO instruction condition codes or status error.
0103 TDV instruction condition codes or status error.
0104 AIO instruction condition code error. Expect no interrupt recognition.

TST1, 2 SIO invalid order (7440/7445, 7441, 7446, 7450). SIO is issued with all invalid orders and controller tested for unusual end.

0201 SIO instruction condition codes not 00 as expected.
0202 SIO instruction status error.
0203 TIO instruction indicates controller busy 50 μs after SIO. Expect UE.
0204 TIO instruction indicates status error after SIO (invalid order). Expected UE, controller not busy.
0205 TIO instruction terminal byte count not = 1 indicating controller accepted one byte for invalid order.

TST1, 3 Test Mode Selection. (7441, 7446). SIO issued to select and reset controller test mode. TDV is used to verify test mode (CC2 = 1—test mode).

0301 SIO instruction condition code or status error.
0302 TIO instruction indicates controller busy beyond normal termination time for select test mode order.
0303 TIO instruction indicates controller terminated with UE for select test mode order.
0304 TIO instruction indicates status error after select test mode order.
0305 Test mode byte not accepted by controller.
0306 Test mode byte disturbed by controller data in operation. Expected data out (one byte) operation.
0307 TDV condition codes not 01. Expected CC1, 2 = 01 (test mode selected).
0308 SIO instruction condition code or status error while controller in test mode.
0309 TIO indicates condition code or status error for reset test mode order.
0310 TDV condition codes not 00 indicating reset test mode order not performed correctly. Expected CC1, 2 = 00.

TST1, 4 interrupt generation and HIO, AIO instruction resetting (7441, 7446). The following orders are issued: X'07', X'07', and X'00' in order to test the generation of ICE, IZC and IUE. AIO and HIO instructions are issued to test the interrupt clearing.

0401 TIO instruction indicates IP status not present after X'07' order issued with ICE flag set.
0402 TIO instruction condition code or status error after X'07' order issued with ICE flag set.
0403 AIO instruction condition code, status or device address error following A X'07' order raising IP.
0404 HIO instruction did not clear IP in controller.
0405 TIO instruction indicates IP not set by X'07' order with IZC flag set.
0406 TIO instruction condition code or status error after X'07' order with IZC flag set.
0407 AIO instruction condition code, status or device address error after X'07' order with IZC flag set.
0408 AIO or HIO instruction did not reset IP status in controller.
0409 TIO indicates X'00' order with IUE flag set did not set IP in controller.
0410 TIO indicates condition code or status error after X'00' order with IUE flag set.
0411 AIO condition code, status or device address error after X'00' order with IUE flag set.
0412 TIO indicates no UE status for X'00' order.
0413 TIO condition code or status error after AIO or HIO issued with IP status present.
0414 AIO did not reset IP status in controller.

TST1, 5 data transmission complete interrupt (7441, 7446). A test mode order with DTC flag (X'47') is used to verify data transmission complete interrupt generation.

0501 Data transmission complete interrupt not generated.
0502 TIO indicates condition code or status error for X'47' order. Expected IP status.
0503 AIO condition code, status or device address error after DTC interrupt generated in controller. Expected AIO status bit 1 set.

TST1, 6 IO Interrupt (7441, 7446). Test mode orders are issued with ICE, IZC and IUE flags to verify the interrupts are received by the IOP and CPU.

0601 Interrupt not received by CPU.
0602 TIO status error after CPU received interrupt from controller.
0603 AIO condition code, status or device address error after interrupt received by CPU.
0604 TIO indicates HIO did not reset IP in controller.
0605 AIO condition code, status or device address error after interrupt received by CPU.
0606 TIO indicates HIO did not reset IP status in controller.
0607 AIO condition code, status or device address error after interrupt received by CPU.
0608 TIO indicates HIO did not reset IP in controller.

TST1, 7 Command Chaining. (7441, 7446) Two test mode orders are command chained and chaining verified. Invalid order command chained to test mode order is tested for command chain termination after the invalid order.

0701 TIO indicates controller busy beyond normal termination time for command chain operation.
0702 TIO indicates status error during command chaining operation.
0703 TIO indicates operational status error following command chain operation.
0704 Byte count not 0 following command chaining operation.
0705 TIO indicates command chaining terminated with first IOCD instead of second IOCD.
0706 Controller busy with invalid order.
0707 TIO indicates UE not generated for invalid order.
0708 TIO status error following invalid order command chained to test mode order.
0709 Terminal byte count not 0 following an invalid order command chained to test mode order.
0710 Command chaining not terminated by UE of invalid order.

TST1, 11 State Progression - Print order (test mode) (7441, 7446). A print order (X'01') is issued in test mode and TDV instruction used to step the controller through states A, B, A. TDV set 2 verifies the state progression. Print, buffer clearing and paper motion is inhibited.

1101 Test mode selection error. Expected TDV CC1, 2 = 01.
1102 TDV set 2 indicates controller not in quiescent state A.
1103 SIO condition code or status error for print order.

TST1, 11 (Continued)

1104 SIO for print order accepted but TIO status does not indicate device, controller busy.
1105 TIO device and controller status inconsistent. Expected device, controller busy for print order (state progression).
1106 TIO status error during a print order (state progression). Expected controller, device busy.
1107 TDV set 2 inconsistent. Expected controller in state B following a data out (one byte) phase.
1108 TDV set 2 indicates controller did not progress from state A to state B for a print order (one byte transfer).
1109 TDV set 2 inconsistent. Expected state A following a data out phase (one byte) in state B.
1110 TDV set 2 indicates controller did not return to state A following a data out phase (one byte) in state B.
1111 TIO status error following a print order (state progression).
1112 Terminal byte count not 0 indicating data byte not taken while controller in data out state B.
1113 TDV set 2 inconsistent. Expected controller in state A following an order out phase.
1114 TDV set 2 indicates controller not in state A following an order out phase.

TST1, 12 State Progression - Format order (test mode) (7441, 7446). A format order (X'03') is issued in test mode and TDV instructions used to step the controller through states A, D, E, A. TDV set 2 verifies the state progression. Printing, buffer clearing and paper motion is inhibited.

1201 Test mode selection error. Expected TDV CC1, 2 = 01.
1202 TDV set 2 indicates controller not in quiescent state A.
1203 SIO status error for format order.
1204 TDV set 2 indicates controller not in state A following an order out phase.
1205 TDV set 2 indicates control byte (format byte) not received while controller in state D. Expected TDV bit 3, 7 set.
1206 TDV set 2 indicates controller did not progress from state D (data out phase, one byte) to state E (paper motion inhibited).
1207 TDV set 2 inconsistent. Expected state A (order in phase) following state E (paper motion inhibited).
1208 TDV set 2 indicates controller did not progress from state E (paper motion inhibited) to state A (order in phase).
1209 TIO status error following a format order.
1210 TIO indicates controller busy after a format order. Expected controller ready and no paper motion.
1211 Terminal byte count not 0 for a format order indicating controller did not accept format byte while in state D.
1212 TDV set 2 indicates controller did not progress from state A (order out phase) to state D (data out phase, one byte).

TST1, 13 State Progression - Print W format order (test mode) (7441, 7446). A print with format order (X'05') is issued in test mode and TDV instructions used to step the controller through states A, D, E, B, A. TDV set 2 verifies the state progression. Printing, buffer clearing and paper motion is inhibited.

1301 Test mode selection error. Expected TDV CC1, 2 = 01.
1302 TDV set 2 indicates controller not in quiescent state A.
1303 SIO status error for print with format order.
1304 TDV set 2 indicates controller not in state A (order out phase).
1305 TDV set 2 indicates controller did not receive control byte (format byte) while in state D.
1306 TDV set 2 indicates controller did not progress from state D (data out, format byte) to state E (paper motion inhibited).
1307 TDV set 2 indicates controller did not progress from state E to state B (data out, one character).
1308 TDV set 2 indicates controller did not progress from state B (data out, one character) to state A (order in).
1309 TIO status error after print with format order.
1310 Controller busy in state A (order in phase).
1311 Terminal byte count not 0 indicating format byte not accepted in state D.
1312 TDV set 2 indicates controller did not progress from state A (order out) to state D (data out, format byte).

TST1, 15 Print Order (test mode) (7441, 7446). Print orders are issued in test mode (buffer clearing, printing and paper motion inhibited) with from 1 through 133 bytes transferred. Terminal status is verified.

1501 Test mode selection error. Expected TDV CC1, 2 = 01.
1502 SIO status error for print order.
1503 Controller busy after normal termination time for print order with indicated byte count.
1504 TIO status error after print order with indicated byte count.
1505 Controller terminated print order with UE.
1506 IOP error for print order with byte count = 132.
1507 IL status set for print order with byte count = 132.
1508 Operational status error for print order with byte count = 132.
1509 TDV set 1 indicates an IO parity error detected by controller during a print order with X'A5' characters transferred.
1512 Terminal byte count for print order not 0.
1513 IL not set by controller for print order with byte count unequal to 132 bytes.
1514 IOP status error indicated for print order.
1515 Operational status error for print order with byte count unequal to 132.

TST1, 16 Print With Format Order (test mode) (7441, 7446). Print with format orders are issued in test mode (buffer clearing, printing and paper motion inhibited) with from 1 through 133 bytes transferred. Terminal status is verified.

1601 Test mode selection error. Expected TDV CC1, 2 = 01.
1602 SIO status error for print with format order.
1603 Controller busy beyond normal termination time for print with format order.
1604 TIO status error after print with format order with indicated byte count.
1605 Controller terminated print with format order with UE.
1606 IOP error after print with format order with byte count = 132.
1607 Operational status error after print with format order with byte count = 133.
1609 TDV set 1 indicates controller detected a buffer parity error for a print with format order with X'A5' bytes transferred.
1610 TDV set 1 indicates controller detected an IO parity error for a print with format order with X'A5' bytes transferred.
1611 IL not set by controller for a print with format order with byte count unequal to 133.
1612 IOP status error for print with format order.
1613 Operational status error for print with format order.
1614 Terminal byte count not 0 for a print with format order.

TST1, 17 Format Order (test mode) (7441, 7446). Format orders are issued in test mode (paper motion inhibit) with byte counts of 1 through 10. Terminal status is verified.

1701 Test mode selection error. Expected TDV CC1, 2 = 01.
1702 SIO status error for format order.
1703 Controller busy beyond normal termination time for format order.
1704 TIO indicates status error for format order with byte count > 1.
1705 TIO indicates UE not received for format order with byte count > 1.
1706 IOP error for format order.
1707 Operational status error for format order with byte count = 1.
1708 IL status set by controller for format order with byte count = 1.
1709 TDV set 1 indicates IO parity error detected for format order with X'C1' byte.
1710 TDV set 1 indicates buffer parity error for format order.
1711 IL status not set by controller for format order with byte count greater than one.
1712 IOP status error for format order with byte count greater than one.
1713 Operational status error for format order with byte count greater than one.
1714 Controller accepted more than one byte for a format order with byte count greater than one.
1715 TIO status error after format order with byte count = 1. Controller ready and no UE expected.

TST1, 20 Address Counter - Print order (test mode) (7441, 7446). Print orders are issued in test mode (buffer clearing, printing and paper motion inhibited) with byte counts of 1 through 132. TDV set 5 verifies the incrementing of the character buffer address counter.

2001 Test mode selection error. Expected TDV CC1, 2 = 01.
2002 Status error after print order with byte count = 132.
2003 TDV set 5 indicates address counter is not incrementing. See printout.
2004 TDV set 5 indicates address counter is not incrementing correctly for a print order. See printout.

TST1, 21 Address Counter - Print with format order (test mode) (7441, 7446). Print with format orders are issued in test mode (buffer clearing, printing and paper motion inhibited) with byte counts of 1 through 133. TDV set 5 verifies the incrementing of the character buffer address counter.

2101 Test mode selection error. Expected TDV CC1, 2 = 01.
2102 Status error for print with format order.
2103 TDV set 5 indicates address counter not incrementing for a print with format order.
2104 TDV set 5 indicates address counter not incrementing correctly for a print with format order. See printout.

TST1, 22 Address Counter - Format order (test mode) (7441, 7446). Format orders are issued in test mode (paper motion inhibited) with byte counts of 1 through 10. TDV set 5 verifies that the character buffer address counter does not increment during the format order.

2201 Test mode selection error. Expected TDV CC1, 2 = 01.
2203 Status error for format order.
2204 TDV set 5 indicates address counter not at X'00' configuration after a format order.
2205 Status error for format order with byte count >1.

TST1, 23 Sense Character Buffer Order (test mode) (7441, 7446). Sense character buffer orders are issued in test mode with byte counts of 1 through 132. Terminal status is tested and all sense bytes (character buffer contents) are verified to be X'00'.

2301 Test mode selection error. Expected TDV CC1, 2 = 01.
2302 SIO status error for sense order.
2303 Controller busy beyond normal termination time for a sense character buffer order.
2304 TIO status indicates controller terminated sense character buffer order with UE.
2305 TIO status error for sense character buffer order.
2306 IOP error for sense character buffer order.
2307 IL status set for sense character buffer order.
2308 Operational status error for sense character buffer order.
2309 Terminal byte count for sense character buffer not = 0.
2310 Sensed character buffer bytes not all X'00'. See printout.

TST1, 24 Character Buffer - Data (test mode) (7441, 7446). Print orders are issued in test mode (buffer clearing, printing and paper motion inhibited) with byte counts of 132 and data bytes of X'00' through X'FF'. Sense character buffer orders are used to verify the contents of the character buffer (character bits 2-7 only).

2401 Test mode selection error. Expected TDV CC1, 2 = 01.
2402 Status error for print order with byte count = 132.
2403 Status error for sense character buffer order with byte count of 132.
2404 Character buffer contents incorrect. See printout.

TST1, 25 Character Buffer - Parity (test mode) (7441, 7446). Print orders are issued in test mode (buffer clearing, printing and paper motion inhibited) with byte counts of 132 and data bytes of X'00' thru X'FF'. Sense character buffer orders are used to verify the contents of the character buffer including odd parity.

2501 Test mode selection error. Expected TDV CC1, 2 = 01.
2502 Status error for print order with byte count = 132.
2503 Status error for sense character buffer order with byte count of 132.
2504 Character buffer parity failure. See printout.

TST1, 26 Character Buffer - Byte Positioning (test mode) (7441, 7446). Print orders are issued in test mode (buffer clearing, printing and paper movement inhibited) with byte counts of 132. Each data pattern of X'40' (blank) characters contains one X'FF' character sequentially, then randomly placed in the pattern. Sense character buffer orders are used to verify character buffer contents.

2601 Test mode selection error. Expected TDV CC1, 2 = 01.
2602 Status error for print order with byte count = 132.
2603 Status error for sense character buffer order with byte count of 132.
2604 Character buffer failure in character positioning. See printout.

TST1, 27 Character Buffer - Blanks (test mode) (7441, 7446). A print order is issued in test mode (buffer clearing, printing and paper motion inhibited) with byte count of 132 and data pattern of X'40' characters. A sense character buffer order is used to verify the character buffer contains X'00' bytes.

2701 Test mode selection error. Expected TDV CC1, 2 = 01.
2702 Status error for print order with byte count of 132.
2703 Status error for sense character buffer order with byte count of 132.
2704 Character buffer contents not X'00'. See printout.

TST1, 31 Format Register - Format Order (test mode) (7441, 7446). Format orders are issued in test mode (paper motion inhibited) with format bytes of X'00' thru X'FF'. TDV set 3 is used to verify the format register and paper motion control values.

3101 Test mode selection error. Expected TDV CC1, 2 = 01.
3102 SIO status error for format order.
3103 Status error for format order with byte count = 1.
3104 TDV set 3 indicates format register contents and/or paper motion control signals incorrect. See printout.
3105 TIO status error after format order with byte count = 2.
3106 TDV set 3 indicates format register contents disturbed by the format byte.
3107 Terminal byte count for a format order (byte count = 2) not = 1.

TST1, 32 Format Register - Print with format order (test mode) (7441, 7446). Print with format orders are issued in test mode (buffer clearing, printing and paper motion inhibited) with byte counts of 1 through 133. Random format bytes are used and TDV set 3 is used to verify the format register contents.

3201 Test mode selection error. Expected TDV CC1, 2 = 01.
3202 SIO status error for print with format order.
3203 Status error for print with format order with byte count = 133.
3204 Status error for print with format order with byte count unequal to 133.
3205 TDV set 3 indicates format register and/or paper control signals incorrect. See printout.

TST1, 35 Code Disk - Sense Order (test mode) (7441, 7446). Code disk sense orders are issued in test mode to transfer from 1 to 129 bytes of code disk information. Terminal status is tested.

TST1, 35 (Continued)

3501 Test mode selection error. Expected TDV CC1, 2 = 01.
3502 SIO status error for sense code disk order X'04'.
3504 TIO indicates controller busy beyond normal termination time for sense code disk order.
3505 Status error for code disk sense order.
3506 TDV set 1 indicates parity error during code disk sense order.

TST1, 36 Code Disk – Data and Parity (test mode) (7441, 7446). A sense code order is issued in test mode to transfer 128 bytes (two code images). Code disk images (including parity) are verified.

3601 Test mode selection error. Expected TDV CC1, 2 = 01.
3602 Status error for code disk sense order.
3603 Code disk images not correct. See printout.

TST1, 37 Code Disk Timing (test mode) (7441, 7446). A sense order is issued in test mode and the transfer time between bytes (initiated by code disk clocks) is verified.

3701 Test mode selection error. Expected TDV CC1, 2 = 01.
3702 Time between code disk clocks has exceeded the nominal 850 μs.

TST1, 40 State Progression – Comparator (test mode) (7441, 7446). A print order is issued (printing and paper motion inhibited) and TDV instruction used to step the controller through states A, B, C, A. TDV set 2 verifies the states and comparator scanning completion.

4001 Test mode selection error. Expected TDV CC1, 2 = 01.
4002 TDV set 2 indicates controller not in state A after order out.
4003 TDV set 2 indicates controller not in state B (data out, 132 bytes) after state A.
4004 TDV set 2 indicates print complete (pseudo indication for test mode) not set for state C (character buffer scanning state).
4005 TDV set 2 indicates controller did not progress from state C (character buffer scan) to state E (paper motion inhibited).
4006 Status error after print order with character buffer scan.
4007 TDV set 2 indicates character buffer scanning was not completed in state C 'blank' characters transferred to character buffer.
4008 TDV set 2 indicates controller did not progress from state B (data out, 132 bytes) to state C (character buffer scan).
4009 TDV set 2 indicates controller did not progress from state E to state A (order in phase).
4010 TDV set 1 indicates status error after print order with character buffer scan.

TST1, 41 Comparator – Character Buffer Clearing (test mode) (7441, 7446). A series of 64 print orders are issued and all 64 printable characters are transferred. Sense character buffer orders are used to verify the comparator for all characters.

4101 Test mode selection error. Expected TDV CC1, 2 = 01.
4102 TIO indicates controller busy for print order with byte count of 132.
4103 TDV set 1 indicates a buffer parity error during character buffer scanning.
4104 Status error for print order with byte count = 132.
4105 Status error for sense character buffer order.
4106 Character buffer not cleared by comparator scanning. See printout.

TST1, 42 State Progression – Format Order/Paper Motion (test mode) (7441, 7446). A format order is issued in test mode and TDV set 4 is used to verify the paper movement control signals for a format byte (X'C1' to X'CF' for 7441 and X'C1' to X'C5' for 7446).

4201 Test mode selection error. Expected TDV CC1, 2 = 01.
4202 TDV set 1 indicates status error after format order with paper motion completion.
4203–4211 TDV set 4 indicates paper motion control error. See printout.

TST1, 43 State Progression – Print Order/Paper Motion (test mode) (7441, 7446). A print order is issued in test mode and TDV instruction used to step the controller through states A, B, C, E, A. TDV set 2 verifies the progression and terminal status and character buffer contents are verified.

4301 TDV set 1 indicates paper low, interlock or hammer driver supply low for 7441. TDV set 1 indicates TDV status error for 7446.
4302 Test mode selection error. Expected TDV CC1, 2 = 01.
4303 TDV set 2 indicates controller not in state A after order out.
4304 TDV set 2 indicates controller did not progress from state A (order out) to state B (data out, 132 bytes).
4305 TDV set 2 indicates controller did not progress from state B to state C (character buffer scan).
4306 TDV set 2 indicates character buffer scan not completed in state C.
4307 TDV set 2 indicates sentinel monitor signal not set in state C.
4308 TDV set 2 indicates control byte received signal in error in state C.
4309 TDV set 2 indicates controller did not progress from state C to state E (paper motion).
4310 Test mode selection error. Expected TDV CC1, 2 = 01.
4311 TDV set 1 indicates interlock error for print order for 7441.
4312 Status error for print order with byte count = 132.
4313 Character buffer not cleared while controller in state E. See printout.
4314 TDV set 1 indicates paper motion/printing error after print order.
4315 TDV set 1 indicates error after sense character buffer order.

TST1, 44 State Progression – Print with format order (test mode) (7441, 7446). A print with format order is issued in test mode and TDV instruction used to step the controller through states A, D, E, B, C, E, A. TDV set 2 verifies the progression.

4401 Test mode selection error. Expected TDV CC1, 2 = 01.
4402 TDV set 2 indicates controller not in state A after order out.
4403 TDV set 2 indicates controller did not progress from state A to state D (data out, format byte).
4404 TDV set 2 indicates controller did not progress from state D to state E (paper motion).
4405 TDV set 2 indicates controller did not progress from state E to state B (data out, 132 bytes).
4406 TDV set 2 indicates controller did not progress from state B to state C (character buffer scan, print).
4407 TDV set 2 indicates controller did not progress from state C to state E (paper motion) or print error occurred.
4408 Status error for print with format order.
4409 Test mode selection error. Expected TDV CC1, 2 = 01.
4410 TDV set 4 indicates paper motion control signal error after paper motion.
4411 TDV set 1 indicates status error after print with format order.
4412 Status error for print with format (no data chain).
4413 TDV set 2 indicates controller did not progress from state E to state A (data chain).
4414 TDV set 2 indicates controller did not progress from state E to state A (no data chain).

TST1, 45 State Progression – Format Order/Paper Motion (high speed slew) (7446). A format order is issued in test mode and TDV set 4 is used to verify the paper movement control signals for a X'C6' to X'CF' format byte.

4501 Test mode selection error. Expected TDV CC1, 2 = 01.
4502 TDV set 1 indicates status error after format order with paper motion completion.
4503–4510 TDV set 4 indicates paper motion control error. See printout.

TST1, 46 Paper Clamp – Print Order/Paper Motion (test mode) (7446). A print order is issued in test mode and TDV instruction used to step the controller through states A, B, C, E, A. TDV set 4 verifies the paper clamp timing.

4601 Test mode selection error. Expected TDV CC1, 2 = 01.
4602-4605 TDV set 4 indicates paper clamp control error (see printout).

TST1, 47 Print Order – Automatic Upspacing (7441, 7446). A print order is issued to print a pattern of 'E' characters. Terminal status is verified.

4701 Status error for print order.
4702 Test mode selection error. Expected TDV CC1, 2 = 01.
4703 TDV set 2 indicates print control error for print order.
4704 TDV set 1 indicates print error for print order (7446).
4705 TDV set 4 indicates print control error for print order.

TST1, 48 Print with Format Order – Inhibit Upspace (7441, 7446). A print with format order is issued to perform a print operation with inhibit upspace format. Terminal status and character buffer verified.

4801 Controller busy beyond normal termination time for print with format order (upspace inhibited).
4802 Status error for print with format order (upspace inhibited).
4803 Test mode selection error. Expected TDV CC1, 2 = 01.
4804 Character buffer not cleared for print with inhibit upspace order.
4805 TDV set 1 indicates status error for print with inhibit upspace.

TST1, 49 Format Order – Space Lines (7441, 7446). A format order (X'C1' to X'CF' byte) is issued and terminal status verified.

4901 Status error for format order.
4902 Test mode selection error. Expected TDV CC1, 2 = 01.
4903 TDV set 4 indicates paper motion control signal error for format order.
4904 TDV set 3 indicates format register error after format order.
4905 TDV set 1 indicates status error for format order.

TST1, 50 Print N Format (7441, 7446). A print with format order is issued to space 2 lines and print line of 'E' characters. Terminal status is verified.

5001 Status error for print with format order.
5002 Test mode selection error. Expected TDV CC1, 2 = 01.
5003 TDV set 4 indicates paper motion control error for print with format order.

TST1, 52 Print Blanks (7441, 7446). A print order is issued to print one line of blanks. Terminal status is tested.

5201 Status error for print blanks.
5202 Test mode selection error. Expected TDV CC1, 2 = 01.
5203 TDV set 2 indicates print control error for print blank line.
5204 TDV set 3 indicates format control error for print blank line.
5205 TDV set 4 indicates paper motion control error for print blank line.
5206 TDV set 5 indicates address counter not at correct terminal state.

TST1, 53 Print Continuous (7441, 7446). A series of 10 lines of 'E' characters are printed. Terminal status is tested.

5301 Status error for print 'E' character lines.
5304 Test mode selection error. Expected TDV CC1, 2 = 01.
5305 TDV set 2 indicates print control error.
5306 TDV set 4 indicates paper motion control error.
5307 TDV set 3 indicates format control error.

TST1, 54 Print Broadside Pattern (7441, 7446). A broadside pattern of all characters are printed. Terminal status is tested.

5401 Status error for broadside line.

TST1, 55 Error Induction/Reporting (7446). Using a print order and test mode to: (1) force print echo error, (2) force buffer parity error, (3) force IO parity error, (4) force code disk parity error. Each time verify that induced error is reported correctly.

5501 Test mode selection error. Expected TDV CC1, 2 = 01.
5502 TDV set 1 indicates no print error reported.
5503 TDV set 1 indicates no buffer parity error reported.
5504 TDV set 1 indicates no IO parity error reported.
5505 TDV set 1 indicates no code disk parity error reported.
5506 TIO status indicates no unusual end reported.

TST1, 56 IO Parity Induction/Reporting (7446). The following orders are issued: 128 X'01', X'03', X'05', and X'01' in order to test for the correct error reporting of data parity and order out for 5/7 and 8/9 computer.

5601 Test mode selection error, expected TDV CC1, 2 = 01.
5602 TDV set 1 indicates incorrect report of data parity error.
5603 TDV set 1 indicates incorrect report of parity error. (Sigma 8/9 order out) (Sigma 5/7 data parity).
5605 TIO indicates incorrect byte count.

TST1, 58 Invalid Character Test (7442 only). Print two lines of invalid characters then two lines of mixed valid and invalid characters. After a long delay for each print, printer should still be busy. No printing occurs for invalid characters.

5801 Line printer not busy after printing invalid character.

TST1, 60 Format Order – Inhibit Upspace (7440/7445, 7450). A format order of a byte count of one, then a byte count of two is issued. Terminal status is verified and that no paper motion has occurred.

6001 SIO status error for format order.
6002 Device, controller busy beyond normal termination time for format order.
6003 Paper motion occurred for a format with inhibit upspace.
6004 Status error for format order.
6005 Byte count did not decrement after format order.

TST1, 61 Interrupt Generation and HIO, AIO Instruction Resetting (7450, 7440/7445). The following orders are issued: X'07', X'07', and X'00' in order to test the generation of ICE, IZC, and IUE. AIO and HIO instructions are issued to test the interrupt clearing.

6101 TIO instruction indicates IP status not present after X'07' order with ICE flag set.
6102 TIO instruction condition code or status error after X'07' order issued with ICE flag set.
6103 AIO instruction condition code, status or device address error following a X'07' order raising IP.
6104 HIO instruction did not clear IP in controller.
6105 TIO instruction indicates IP not set by X'07' order with IZC flag set.
6106 TIO instruction condition code or status error after X'07' order with IZC flag set.
6107 AIO instruction condition code, status or device address error after X'07' order with IZC flag set.
6108 AIO or HIO instruction did not reset IP status in controller.
6109 TIO indicates X'00' order with IUE flag set did not set IP in controller.
6110 TIO indicates condition code or status error after X'00' order with IUE flag set.
6111 AIO condition code, status or device address error after X'00' order with IUE flag set.
6112 TIO indicates no UE status for X'00' order.
6113 TIO condition code or status error after AIO or HIO issued with IP status present.
6114 AIO did not reset IP status in controller.

TST1, 62 IO Interrupt Generation (7440/7445, 7450). A format with ICE flag is issued. Verify that the program is interrupted when the IO interrupt is armed and enabled.

| | |
|---|---|
| 6201 | TIO instruction indicates IP not set by SIO, IO interrupt is disarmed. |
| 6202 | Program was interrupted while IO interrupt was disarmed. |
| 6203 | Program was not interrupted while IO interrupt was armed/ enabled. |
| 6204 | TIO indicates IP not cleared by an AIO instruction. |

TST1, 63 Print with Format - Inhibit Upspace (blank characters) (7440/7445). A print with format order is issued to perform a print operation with inhibit upspace format. Terminal status and no paper motion is verified. Bytes of 2 through 134 are transferred.

| | |
|---|---|
| 6301 | Paper motion has occurred for a print with format order. |
| 6302 | Byte count not equal to zero after a print with format order. |
| 6303 | IL not set for byte count unequal to 132. |
| 6304 | IL set for byte count equal to 132. |
| 6305 | Status error for print with format. |
| 6306 | SIO status error for print with format. |

TST1, 64 Print with Format - Inhibit Upspace (blank characters) (7450). First then second print with format order are issued. Printer expects first then second print order is verified. Byte 2 through 129 are transferred. Terminal status and no paper motion is verified.

| | |
|---|---|
| 6401 | Paper motion has occurred for a first print with format order. |
| 6402 | Paper motion has occurred for a second print with format order. |
| 6403 | Byte count not equal to zero after a first print with format order. |
| 6404 | Byte count not equal to zero after a second print with format order. |
| 6405 | Status error for first print with format order. |
| 6406 | Status error for second print with format order. |
| 6407 | SIO status error for first print with format order. |
| 6408 | SIO status error for second print with format order. |
| 6409 | Expect first print order TDV bit not set for first print order. |
| 6410 | Expect first print order TDV bit set for second print order. |
| 6411 | Typeline sector error (should always be one). |

TST1, 65 Data Transmission Complete (DTC) Interrupt (7440/7445, 7450). Using print with format and interrupt on data transmission complete, verify data transmission complete interrupt is generated.

| | |
|---|---|
| 6501 | Data transmission complete interrupt not generated. |
| 6502 | TIO indicates condition code or status error for X'45' order. Expected IP status. |
| 6503 | AIO condition code, status or device address error after DTC interrupt generated in controller expected AIO status bit 1 set. |
| 6504 | Print fault - see printout. |

TST1, 66 Command Chaining (7440/7445, 7450) (Sigma 5/7). Using the invalid order, verify the command chaining operation; verify that the UE status terminates the command chaining.

| | |
|---|---|
| 6601 | TIO indicates controller busy beyond normal termination time for command chain operation. |
| 6602 | TIO indicates status error during command chaining operation. |
| 6603 | TIO indicates operational status error following command chain operation. |
| 6604 | Byte count not 0 following command chaining operation. |
| 6605 | TIO indicates command chaining terminated with first IOCD instead of second IOCD. |
| 6606 | Controller busy with invalid order. |
| 6607 | TIO indicates UE not generated for invalid order. |
| 6608 | TIO status error following invalid order command chained. |
| 6609 | Terminal byte count zero following an invalid order command chained. |
| 6610 | Command chaining not terminated by UE of invalid order. |
| 6611 | SIO status error for invalid order command chained. |
| 6612 | SIO status error for command chained. |

TST1, 68 Format - Space One Line (7440/7445, 7450). A format order is issued to space one line. Verify that paper motion and no print operation occurs.

| | |
|---|---|
| 6801 | Status error for format order. |
| 6802 | No paper motion for space one line format order. |

TST1, 69 Print with Auto Upspace (7440/7445, 7450). Six print orders are issued to verify each code disk character. Verify that paper motion and no print error occurs.

| | |
|---|---|
| 6901-6906 | Status error for a print order. |
| 6907 | Paper motion for print with auto upspace. |

TST1, 70 Print Broadside Pattern (7440/7445, 7450). A broadside pattern of all characters are printed. Terminal status is tested.

| | |
|---|---|
| 7001 | Status error for broadside line. |

TST1, 71 Print - Sliding One Column Pattern (7440/7445,7450). Print with auto upspace is issued with incrementing byte counts of a sliding 1 column pattern. Verify that no print errors occur.

| | |
|---|---|
| 7101 | Status error for a print order. |

TST1, 73 Pattern and Format Test (7440/7445, 7450). Run a selected set of utility tests in sequence. Verify that no print error or paper fault occur.

| | |
|---|---|
| 7301 | Status error for hammer registration. |
| 7302 | Status error for checkerboard pattern. |
| 7303 | Status error for ripple test pattern. |
| 7304 | Status error for printer speed test. |
| 7305 | Status error for skip line test. |
| 7306 | Status error for channel search test. |

# 12. SIGMA 5–9 COMPREHENSIVE LINE PRINTER TEST (744X/745X)

TEST/DEVICE REFERENCE TABLE

| | Subtest | Model Number | | | | Not Used |
|---|---|---|---|---|---|---|
| | | 7440/7445 3451 | 7441 7442 | 7446 | 7450 | |
| TST1 | 1 | X | X | X | X | |
| | 2 | X | X | X | X | |
| | 3 | | X | X | | |
| | 4 | | X | X | | |
| | 5 | | X | X | | |
| | 6 | | X | X | | |
| | 7 | | X | X | | |
| | 8 | | | | | X |
| | 9 | | | | | X |
| | 10 | | | | | X |
| | 11 | | X | X | | |
| | 12 | | X | X | | |
| | 13 | | X | X | | |
| | 14 | | | | | X |
| | 15 | | X | X | | |
| | 16 | | X | X | | |
| | 17 | | X | X | | |
| | 18 | | | | | X |
| | 19 | | | | | X |
| | 20 | | X | X | | |
| | 21 | | X | X | | |
| | 22 | | X | X | | |
| | 23 | | X | X | | |
| | 24 | | X | X | | |
| | 25 | | X | X | | |
| | 26 | | X | X | | |
| | 27 | | X | X | | |
| | 28 | | | | | X |
| | 29 | | | | | X |
| | 30 | | | | | X |
| | 31 | | X | X | | |
| | 32 | | X | X | | |
| | 33 | | | | | X |
| | 34 | | | | | X |
| | 35 | | X | X | | |
| | 36 | | X | X | | |
| | 37 | | X | X | | |
| | 38 | | | | | X |
| | 39 | | | | | X |
| | 40 | | X | X | | |
| | 41 | | X | X | | |
| | 42 | | X | X | | |
| | 43 | | X | X | | |
| | 44 | | X | X | | |
| | 45 | | | X | | |
| | 46 | | | X | | |
| | 47 | | X | X | | |
| | 48 | | X | X | | |
| | 49 | | X | X | | |
| | 50 | | X | X | | |
| | 51 | | | | | X |
| | 52 | | X | X | | |
| | 53 | | X | X | | |
| | 54 | | X | X | | |
| | 55 | | | X | | |
| | 56 | | | X | | |
| | 57 | | | | | X |
| | 58 | | | | | X |
| | 59 | | | | | X |
| | 60 | X | | | X | |
| | 61 | X | | | X | |
| | 62 | X | | | X | |
| | 63 | X | | | | |
| | 64 | | | | X | |
| | 65 | X | | | X | |
| | 66 | X | | | X | |
| | 67 | | | | | X |
| | 68 | X | | | X | |
| | 69 | X | | | X | |
| | 70 | X | | | X | |
| | 71 | X | | | X | |
| | 72 | | | | | X |
| | 73 | X | | | X | |

| | Subtest | Model Number | | | | Not Used |
|---|---|---|---|---|---|---|
| | | 7440/7445 3451 | 7441 7442 | 7446 | 7450 | |
| TST2 | | X | X | X | X | |
| TST3 | D1=X | 7440/7445 3451 | 7441 7442 | 7446 | 7450 | |
| | 1 | X | X | X | X | |
| | 2 | X | X | X | X | |
| | 3 | X | X | X | X | |
| | 4 | X | X | X | X | |
| | 5 | X | X | X | X | |
| | 6 | X | X | X | X | |
| | 7 | X | X | X | X | |
| | 8 | X | X | X | X | |
| | 9 | X | X | X | X | |

FUNCTIONAL TEST (TST1) (SS1 = 0, SS3 = 1)
INITIALIZING CONDITIONS AND EXPECTED RESULTS

1. Initializing Conditions: None
2. Expected Results:

| | Subtest | Results |
|---|---|---|
| Models 7441, 7442 and 7446 | 42 | Space 1 to 15 lines in sequence (7441 only) |
| | | Space 1 to 5 lines in sequence (7446 only) |
| | 43 | Print 1 line broadside character 'E' |
| | 44 | Space 1 line and print 1 line broadside character 'E' |
| | 45 | Space 6 to 15 lines in sequence |
| | 47 | Print 15 lines of blank characters |
| | | Print 132 lines of sliding one column pattern of character 'E' |
| | | Print 30 lines of one character 'E' random positioning |
| | | Print 10 lines broadside character 'E' |
| | | Print 30 lines random column, random number of columns |
| | 48 | Print with inhibit upspace |
| | 49 | Space 1 to 15 lines in sequence |
| | 50 | Space 2 lines and print 1 line broadside character 'E' |
| | 52 | Print 1 line of blank characters |
| | 53 | Print 10 lines broadside character 'E' |
| | 54 | Print 64 lines broadside pattern of all printable characters |
| Model 7440/7445 7450 and 3451 | 68 | Space 1 line |
| | 69 | Print 1 character per line: characters A, B, D, H &, - |
| | 70 | Print 64 lines broadside pattern of all printable characters |
| | 71 | Print 132 sliding one column pattern |
| | 73 | Print 32 lines broadside character 'E' |
| | | Print 32 lines of alternating blank and character 'E' |
| | | Print 132 lines of ripple test pattern |
| | | Print 36 lines of printer speed test |
| | | Print 263 lines of printer load test pattern |
| | | Space 1 to 7 lines in sequence (7450 only) |
| | | Space 1 to 15 lines in sequence (7440/7445 only) |
| | | Skip to top and bottom of page (7450 only) |
| | | Skip to all 7 channels in sequence (7440/7445 only) |

## HAMMER DRIVER MODULE LOCATION CHART

| COLUMN NUMBER | MODULE LOCATION | | | |
|---|---|---|---|---|
| | 7440/7445 3451 | 7441/7442 See note 1 | 7446 See note 2 | 7450 |
| 1 | 25G | 13HJ | 12HJ | 13HJ |
| 2 | 25G | 13HJ | 12HJ | 13HJ |
| 3 | 25G | 13HJ | 12HJ | 13HJ |
| 4 | 24G | 13HJ | 12HJ | 13HJ |
| 5 | 24G | 13HJ | 12HJ | 13HJ |
| 6 | 24G | 13HJ | 12HJ | 13HJ |
| 7 | 23G | 13HJ | 12HJ | 13HJ |
| 8 | 23G | 13HJ | 12HJ | 13HJ |
| 9 | 23G | 12HJ | 11HJ | 13HJ |
| 10 | 22G | 12HJ | 11HJ | 12HJ |
| 11 | 22G | 12HJ | 11HJ | 12HJ |
| 12 | 22G | 12HJ | 11HJ | 12HJ |
| 13 | 21G | 12HJ | 11HJ | 12HJ |
| 14 | 21G | 12HJ | 11HJ | 12HJ |
| 15 | 21G | 12HJ | 11HJ | 12HJ |
| 16 | 20G | 12HJ | 11HJ | 12HJ |
| 17 | 20G | 13HJ | 10HJ | 12HJ |
| 18 | 20G | 12HJ | 10HJ | 12HJ |
| 19 | 19G | 13HJ | 10HJ | 12HJ |
| 20 | 19G | 12HJ | 10HJ | 12HJ |
| 21 | 19G | 12HJ | 10HJ | 13HJ |
| 22 | 18G | 13HJ | 10HJ | 13HJ |
| 23 | 18G | 12HJ | 10HJ | 13HJ |
| 24 | 18G | 13HJ | 10HJ | 13HJ |
| 25 | 17G | 11HJ | 9HJ | 11HJ |
| 26 | 17G | 11HJ | 9HJ | 11HJ |
| 27 | 17G | 11HJ | 9HJ | 11HJ |
| 28 | 16G | 11HJ | 9HJ | 11HJ |
| 29 | 16G | 11HJ | 9HJ | 11HJ |
| 30 | 16G | 11HJ | 9HJ | 11HJ |
| 31 | 15G | 11HJ | 9HJ | 11HJ |
| 32 | 15G | 11HJ | 9HJ | 11HJ |
| 33 | 15G | 10HJ | 8HJ | 10HJ |
| 34 | 14G | 10HJ | 8HJ | 10HJ |
| 35 | 14G | 10HJ | 8HJ | 10HJ |
| 36 | 14G | 10HJ | 8HJ | 10HJ |
| 37 | 13G | 10HJ | 8HJ | 10HJ |
| 38 | 13G | 10HJ | 8HJ | 10HJ |
| 39 | 13G | 10HJ | 8HJ | 10HJ |
| 40 | 12G | 10HJ | 8HJ | 10HJ |
| 41 | 12G | 11HJ | 6HJ | 10HJ |
| 42 | 12G | 10HJ | 6HJ | 10HJ |
| 43 | 11G | 11HJ | 6HJ | 10HJ |
| 44 | 11G | 10HJ | 6HJ | 10HJ |
| 45 | 11G | 10HJ | 6HJ | 11HJ |
| 46 | 10G | 11HJ | 6HJ | 11HJ |
| 47 | 10G | 10HJ | 6HJ | 11HJ |
| 48 | 10G | 11HJ | 6HJ | 11HJ |
| 49 | 9G | 9HJ | 5HJ | 9HJ |
| 50 | 9G | 9HJ | 5HJ | 9HJ |
| 51 | 9G | 9HJ | 5HJ | 9HJ |
| 52 | 8G | 9HJ | 5HJ | 9HJ |
| 53 | 8G | 9HJ | 5HJ | 9HJ |
| 54 | 8G | 9HJ | 5HJ | 9HJ |
| 55 | 7G | 9HJ | 5HJ | 9HJ |
| 56 | 7G | 9HJ | 5HJ | 9HJ |
| 57 | 7G | 8HJ | 4HJ | 8HJ |
| 58 | 6G | 8HJ | 4HJ | 8HJ |
| 59 | 6G | 8HJ | 4HJ | 8HJ |
| 60 | 6G | 8HJ | 4HJ | 8HJ |
| 61 | 5G | 8HJ | 4HJ | 8HJ |
| 62 | 5G | 8HJ | 4HJ | 8HJ |
| 63 | 5G | 8HJ | 4HJ | 8HJ |
| 64 | 4G | 8HJ | 4HJ | 8HJ |
| 65 | 4G | 9HJ | 3HJ | 8HJ |
| 66 | 4G | 8HJ | 3HJ | 8HJ |
| 67 | 3G | 9HJ | 3HJ | 8HJ |
| 68 | 3G | 8HJ | 3HJ | 8HJ |
| 69 | 3G | 8HJ | 3HJ | 9HJ |
| 70 | 2G | 9HJ | 3HJ | 9HJ |
| 71 | 2G | 8HJ | 3HJ | 9HJ |
| 72 | 2G | 9HJ | 3HJ | 9HJ |
| 73 | 1G | 7HJ | 12HJ | 7HJ |
| 74 | 1G | 7HJ | 13HJ | 7HJ |
| 75 | 1G | 7HJ | 13HJ | 7HJ |
| 76 | 1F | 7HJ | 13HJ | 7HJ |
| 77 | 1F | 7HJ | 13HJ | 7HJ |
| 78 | 1F | 7HJ | 13HJ | 7HJ |
| 79 | 2F | 7HJ | 13HJ | 7HJ |
| 80 | 2F | 7HJ | 13HJ | 7HJ |
| 81 | 2F | 6HJ | 12HJ | 6HJ |
| 82 | 3F | 6HJ | 12HJ | 6HJ |
| 83 | 3F | 6HJ | 12HJ | 6HJ |
| 84 | 3F | 6HJ | 12HJ | 6HJ |
| 85 | 4F | 6HJ | 13HJ | 6HJ |
| 86 | 4F | 6HJ | 13HJ | 6HJ |
| 87 | 4F | 6HJ | 13HJ | 6HJ |
| 88 | 5F | 6HJ | 13HJ | 6HJ |
| 89 | 5F | 7HJ | 10HJ | 6HJ |
| 90 | 5F | 6HJ | 10HJ | 6HJ |
| 91 | 6F | 7HJ | 10HJ | 6HJ |
| 92 | 6F | 6HJ | 10HJ | 6HJ |
| 93 | 6F | 6HJ | 11HJ | 7HJ |
| 94 | 7F | 7HJ | 11HJ | 7HJ |
| 95 | 7F | 6HJ | 11HJ | 7HJ |
| 96 | 7F | 7HJ | 11HJ | 7HJ |
| 97 | 8F | 5HJ | 8HJ | 5HJ |
| 98 | 8F | 5HJ | 8HJ | 5HJ |
| 99 | 8F | 5HJ | 8HJ | 5HJ |
| 100 | 9F | 5HJ | 8HJ | 5HJ |
| 101 | 9F | 5HJ | 9HJ | 5HJ |
| 102 | 9F | 5HJ | 9HJ | 5HJ |
| 103 | 10F | 5HJ | 9HJ | 5HJ |
| 104 | 10F | 5HJ | 9HJ | 5HJ |
| 105 | 10F | 4HJ | 7HJ | 4HJ |
| 106 | 11F | 4HJ | 7HJ | 4HJ |
| 107 | 11F | 4HJ | 7HJ | 4HJ |
| 108 | 11F | 4HJ | 7HJ | 4HJ |
| 109 | 12F | 4HJ | 7HJ | 4HJ |
| 110 | 12F | 4HJ | 7HJ | 4HJ |
| 111 | 12F | 4HJ | 7HJ | 4HJ |
| 112 | 13F | 4HJ | 7HJ | 4HJ |
| 113 | 13F | 5HJ | 6HJ | 4HJ |
| 114 | 13F | 4HJ | 6HJ | 4HJ |
| 115 | 14F | 5HJ | 6HJ | 4HJ |
| 116 | 14F | 4HJ | 6HJ | 4HJ |
| 117 | 14F | 4HJ | 7HJ | 5HJ |
| 118 | 15F | 5HJ | 7HJ | 5HJ |
| 119 | 15F | 4HJ | 7HJ | 5HJ |
| 120 | 15F | 5HJ | 7HJ | 5HJ |
| 121 | 16F | 3HJ | 4HJ | 3HJ |
| 122 | 16F | 3HJ | 4HJ | 3HJ |
| 123 | 16F | 3HJ | 4HJ | 3HJ |
| 124 | 17F | 3HJ | 4HJ | 3HJ |
| 125 | 17F | 3HJ | 5HJ | 3HJ |
| 126 | 17F | 3HJ | 5HJ | 3HJ |
| 127 | 18F | 3HJ | 5HJ | 3HJ |
| 128 | 18F | 3HJ | 5HJ | 3HJ |
| 129 | 18F | 3HJ | 3HJ | |
| 130 | 19F | 3HJ | 3HJ | |
| 131 | 19F | 3HJ | 3HJ | |
| 132 | 19F | 3HJ | 3HJ | |

Notes:

1. In 7441/7442 printers, the front hammer driver chassis is for the odd-numbered columns; the rear for the even.
2. In 7446 printers, the front hammer driver chassis is for the even-numbered columns; the rear for the odd.

# Section 13

# SIGMA 5 - 9

# LINE PRINTER DIAGNOSTIC (746X)

## PROGRAM NO. 706473

# Section 13

## CONTENTS

Page

Subject Model . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 13-1
Required Equipment . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 13-1
Program Prerequisites . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 13-1
General Operating Procedures . . . . . . . . . . . . . . . . . . . . . . . . . . . . 13-1
Directives . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 13-2
Start Procedure . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 13-4
Program Test Description . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 13-5
Normal TDV Status . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 13-6
AIO Status . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 13-6
Format Codes for Format Operations . . . . . . . . . . . . . . . . . . . . . . . 13-6
Functional Subtests and Related Error Messages . . . . . . . . . . . . . . . . 13-7

# 13. SIGMA 5–9 LINE PRINTER DIAGNOSTIC (746X)

**SUBJECT MODEL** -- Line Printer Model Numbers 7461, 7462, 7463, 7464, 7465, 7466

**REQUIRED EQUIPMENT** -- Minimum Memory Size: 16K; Input Device: Card Reader, Paper Tape Reader or Magnetic Tape Unit; Output Device: Keyboard Printer or Line Printer

## PROGRAM PREREQUISITES

Need vertical format tape with all channels punched.

## GENERAL OPERATING PROCEDURES

General operating procedures of the Xerox Sigma 5 through 9 Diagnostic Program Monitor (DPM) apply to this program.

**DIRECTIVES** - directives are entered after a "!" is typed out

| Name | Format | Parameter | | | |
|---|---|---|---|---|---|
| | | ID | Definition | Value Range | Standard Value (default) |
| Program Directives - Environmental Directives | | | | | |
| System Environment | SYST, D1, X2, X3 | D1 | Device model number | 7461, 7462, 7463, 7464, 7465, 7466 | |
| | | X2 | Revision number of controller | 0 for all printers | |
| | | X3 | IOP and Device address | 01 ~ 1F7F | 7461 |
| Program Directives - Testing Directives | | | | | |
| Comprehensive Test (all functional tests, 1 ~ 20, and random exerciser test) | TST0 | | | | |
| Functional Test | TST1 [,D1 [,D2]] | D1<br>D2 | The first subtest to be executed<br>Last subtest to be executed | 0 (all subtests) ~ 22 | 0 |
| Random Exerciser Test | TST2, D1 | D1 | Number of cycles to be performed | D1 > 0 | 1 |
| Utility Test | TST3, D1, D2, D3, D4 | D1 | = 0 Hammer registration<br>D2=Line count | D2 Not entered = Print continuously<br>D2=0 Print 1 line<br>D2≠0 Print D2 lines | |
| | | | = 1 Checkerboard pattern<br>D2=Line count | D2 Not entered=Print continuously<br>= 0 Print 1 line<br>≠ 0 Print D2 lines | |
| | | | = 2 Ripple pattern<br>D2=Line count | D2 Not entered=Print continuously<br>= 0 Print 1 line<br>≠ 0 Print D2 lines | |
| | | | = 3 Printer speed test<br>D2 =Character set count | 1 ≤ D2 ≤ 95 | |
| | | | = 4 Printer load test<br>D2=Line count | D2 Not entered=Print continuously<br>= 0 Print l line<br>≠ 0 Print D2 lines | |
| | | | = 5 Broadside pattern<br>D2=Line count | D2 Not entered=Print continuously<br>= 0 Print l line<br>≠ 0 Print D2 lines | |
| | | | = 6 Selectable pattern/position (Data determined by DATA directive)<br>D2=Number of lines to be printed<br>D3=Number of lines to be printed as a group<br>D4=Number of blank lines between groups | D2 Not entered=Print continuously<br>D2=0 Print l line<br>D2≠0 Print D2 lines<br>D3=0 Print continuous lines<br>≠ 0 No. lines/group<br>0 ≤ D4 | |
| | | | = 7 Space lines (space orders are issued to each of the 30 possible positions in sequence) | Space Order<br>C0 - CF<br>E0 - EF | |
| | | | = 8 Channel search<br>D2=Channel number<br>D3≠0 Skip channel no. with inhibit upspace | D2 Not entered=Skip to all channels in sequence<br>0 ≤ D2 < 7 | |
| | | | =10 All Utility tests in sequence<br>D2 Line count | D2=0 Print 1 line<br>D2≠0 Print D2 lines | |
| | | | = 9 Paper Slew speed<br>D2 not used | | |

**DIRECTIVES** (Continued)

| Name | Format | Parameter | | | |
|---|---|---|---|---|---|
| | | ID | Definition | Value Range | Standard Value (default) |
| Program Directives - Optional Directives | | | | | |
| Pattern selection (for Utility Test)(TST3, 6) | DATA, D1, D2, D3, D4 | D1 | = 4 Variable pattern | -4 | |
| | | D2 | Starting column | 1 ~ 132 | |
| | | D3 | Ending column | 1 ~ 132 | |
| | | D4 | EBCDIC character string (up to 4 EBCDIC characters) | Any printable codes 00 ~ FF (F0F1F2F3) | |
| Limitation of program parameters | LIMT, D1, D2, D3 | D1 | = 1 Limit compare error printouts | 1, 2 | |
| | | | D2=Maximum number of compare error printouts | 0 ≤ D2 | |
| | | | = 2 Limit delay time | -6 | |
| | | | D2=Minimum delay time | 0 ≤ D2 ≤ D3 | |
| | | | D3=Maximum delay time | | |

Note: Parameter of any directive beginning with a D means decimal; with an H means hexadecimal.

## START PROCEDURE

1. Sense Switch Options, Monitor Directive Options, and Environmental Directives – Refer to DPM section of this manual.
2. Test Strategy Selection

| | Comprehensive Test | Functional Test | Random Exerciser Test | Utility Test |
|---|---|---|---|---|
| Recommended Application | Normal Usage | Solid Failure Detection and Specific Problem Analysis | Intermittent Failure Detection | Print Quality Verification |
| Test Directive | TST0 | TST1 | TST2 | TST3 |
| Prerequisite | None | None | TST1 | TST1 |
| Optional Directives | LIMT | LIMT | LIMT | LIMT, DATA |
| Subtests | All functional subtests (1 ~ 20) and random exerciser test | 22 subtests (see error messages for the test types) | Prints a predetermined set of test patterns | Prints one or all of predetermined patterns |
| Error Message Format | 1. ERROR NO. DDDD LOC XXXX<br>2. Self-explanatory | ERROR NO. DDDD LOC XXXX | Self-explanatory | Self-explanatory |

3. System reset should normally be used in order to insure the resetting of controller test mode logic.

## PROGRAM TEST DESCRIPTION

The following is a description of the tests contained in the Comprehensive Line Printer test program.

### TST0

The directive selects the comprehensive test consisting of the functional test (subtests 1-20) and the random exerciser test.

Parameters: None

Example: TST0

1. The functional test will be run on the printer in sequence (subtest 1 through 20).
2. The random exerciser will run until six cycles have been completed. If a failure is encountered, an error message is printed and the exercising continues.

### TST1

The directive selects the entire functional test (no parameters entered) or selects one or more contiguous functional subtests.

Parameters: D1 - First functional subtest
D2 - Last functional subtest

where $0 < D1 \leq D2 \leq 22$

Examples: Run all functional subtests.

TST1, 5, 9

Run functional subtests 5 thru 9.

### TST2

The directive selects the random exerciser test.

Parameters: D1 - Number of cycles to be executed by random exerciser

Example: TST2, 3

The random exerciser will run until three cycles have been completed.

### TST3

The utility test routine allows the user to select a specific utility function and/or print patterns which aid the operator in printer adjustments.

Parameters: D1 - Utility test selection
D2 - Defined by the utility test selected
D3 - Defined by the utility test selected
D4 - Defined by the utility test selected

D1 = 0 Hammer registration
D2 = Line count

Generates pattern of broadside character 'E' (same character in all positions) continuously as a reference in checking printer hammer alignment

D1 = 1 Checkerboard pattern
D2 = Line count

TST3(Continued)

Generates a worst-case pattern to expose ghost character printing. The pattern consists of alternating character 'E' and blanks.

D1 = 2 Ripple pattern
D2 = Line count

Generates a pattern consisting of all characters per line, each succeeding line having the characters shifted one position to the left

D1 = 3 Printer speed test
D2 = Character count (7450 only)

A 36-line pattern of characters is printed to produce maximum print rate. The average time to print and upspace is calculated and the printer speed is determined and reported.

D1 = 4 Printer load test
D2 = Line count

Generates a pattern of an increasing number of character 'E' each line until 132 positions are printed, then a decreasing number of character 'E' each line

D1 = 5 Broadside pattern
D2 = Line count

Generates a 64/95 line pattern of all printable characters broadside

D1 = 6 Selectable pattern/position
D2 = Line count
D3 = Group/line count
D4 = Group/space count

Generates a selectable character and position(s) pattern

D1 = 7 Space lines
D2 = Unused

Space orders are issued to each of the 15 possible positions in sequence.

D1 = 8 Channel search
D2 = Channel number
D3 ≠ 0 Skip to channel number with inhibit upspace.

Channel searches are issued to the operator-specified channel.

D1 = 9 Paper Slew speed
D2 = Not used

Space 15 lines, determine paper slew and report the results.

D1 = 10 Utility test
D2 = Line count

Run all utility tests in sequence

Examples: TST3, 7

Space orders are issued to each of the 15 possible positions in sequence.

TST3, 8, 4

Exercise the printer VFU control. Channel 4 is to be searched.

## ORDER CODES

| | |
|---|---|
| X'01' | Print a line |
| X'41' | Print a line - interrupt at data transmission complete |
| X'03' | Format order (see format codes) |
| X'43' | Format order - interrupt at data transmission complete (see format codes) |
| X'05' | Print with format |
| X'45' | Print with format - interrupt at data transmission complete |

## NORMAL TDV STATUS

| MODEL | BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 7461, 7462,<br>7463, 7464,<br>7465, 7466 | Not Used | Recovery Mode 1 | Recovery Mode 2 | Top of Page | Not Used | Not Used | IO Parity Error | Not Used |

## AIO STATUS

For Model 7461, 7462, 7463, 7464, 7465, 7466

| BITS | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| NOT USED | DATA TRANSMISSION COMPLETE INTERRUPT | ← NOT USED → | | | | | |

## FORMAT CODES FOR FORMAT OPERATIONS

MODEL 7461, 7462, 7463, 7464, 7465, 7466

| | |
|---|---|
| X'60' | Inhibit automatic space after print |
| X'C0' | Space 0 lines |
| X'C1' | Space 1 line |
| X'C2' | Space 2 lines |
| X'C3' | Space 3 lines |
| X'C4' | Space 4 lines |
| X'C5' | Space 5 lines |
| X'C6' | Space 6 lines |
| X'C7' | Space 7 lines |
| X'C8' | Space 8 lines |
| X'C9' | Space 9 lines |
| X'CA' | Space 10 lines |
| X'CB' | Space 11 lines |
| X'CC' | Space 12 lines |
| X'CD' | Space 13 lines |
| X'CE' | Space 14 lines |
| X'CF' | Space 15 lines |
| X'E0' | Space 0 lines and inhibit automatic upspace |
| X'E1' | Space 1 line and inhibit automatic upspace |
| X'E2' | Space 2 lines and inhibit automatic upspace |
| X'E3' | Space 3 lines and inhibit automatic upspace |
| X'E4' | Space 4 lines and inhibit automatic upspace |
| X'E5' | Space 5 lines and inhibit automatic upspace |
| X'E6' | Space 6 lines and inhibit automatic upspace |
| X'E7' | Space 7 lines and inhibit automatic upspace |
| X'E8' | Space 8 lines and inhibit automatic upspace |
| X'E9' | Space 9 lines and inhibit automatic upspace |
| X'EA' | Space 10 lines and inhibit automatic upspace |
| X'EB' | Space 11 lines and inhibit automatic upspace |
| X'EC' | Space 12 lines and inhibit automatic upspace |
| X'ED' | Space 13 lines and inhibit automatic upspace |
| X'EE' | Space 14 lines and inhibit automatic upspace |
| X'EF' | Space 15 lines and inhibit automatic upspace |

| | |
|---|---|
| X'F0' | Skip to channel 0 (bottom of page) |
| X'F1' | Skip to channel 1 (top of page) |
| X'F2' | Skip to channel 2 |
| X'F3' | Skip to channel 3 |
| X'F4' | Skip to channel 4 |
| X'F5' | Skip to channel 5 |
| X'F6' | Skip to channel 6 |
| X'F7' | Skip to channel 7 |
| X'F8' | Skip to channel 8 |
| X'F9' | Skip to channel 9 |
| X'FA' | Skip to channel 10 |
| X'FB' | Skip to channel 11 |
| X'FC' | Skip to channel 8 |
| X'FD' | Skip to channel 9 |
| X'FE' | Skip to channel 10 |
| X'FF' | Skip to channel 11 |
| X'D0' | Skip to channel 0 (BOP) and inhibit automatic upspace |
| X'D1' | Skip to channel 1 (TOP) and inhibit automatic upspace |
| X'D2' | Skip to channel 2 and inhibit automatic upspace |
| X'D3' | Skip to channel 3 and inhibit automatic upspace |
| X'D4' | Skip to channel 4 and inhibit automatic upspace |
| X'D5' | Skip to channel 5 and inhibit automatic upspace |
| X'D6' | Skip to channel 6 and inhibit automatic upspace |
| X'D7' | Skip to channel 7 and inhibit automatic upspace |
| X'D8' | Skip to channel 8 and inhibit automatic upspace |
| X'D9' | Skip to channel 9 and inhibit automatic upspace |
| X'DA' | Skip to channel 10 and inhibit automatic upspace |
| X'DB' | Skip to channel 11 and inhibit automatic upspace |
| X'DC' | Skip to channel 8 and inhibit automatic upspace |
| X'DD' | Skip to channel 9 and inhibit automatic upspace |
| X'DE' | Skip to channel 10 and inhibit automatic upspace |
| X'DF' | Skip to channel 11 and inhibit automatic upspace |

## FUNCTIONAL SUBTESTS AND RELATED ERROR MESSAGES

### FAULT INDEX DESCRIPTION - FUNCTIONAL SUBTESTS

The fault index contains a brief description of each functional subtest and a list of associated error numbers with a brief description of each error. The subtests and error numbers are arranged in ascending sequence. The description of subtest NN is numbered NN00. The first two digits of the error number correspond to the associated subtest; the last two numbers correspond to the individual errors within the subtest.

TST1, 1 HIO, TIO, TDV and AIO instruction recognition. HIO, TIO, TDV and AIO instructions are issued and condition codes status tested.

| | |
|---|---|
| 0101 | HIO instruction condition codes or status error. |
| 0102 | TIO instruction condition codes or status error. |
| 0103 | TDV instruction condition codes or status error. |
| 0104 | AIO instruction condition code error. Expect no interrupt recognition. |

TST1, 2 SIO invalid order. SIO is issued with all invalid orders and controller tested for unusual end.

| | |
|---|---|
| 0201 | SIO instruction condition codes not 00 as expected. |
| 0202 | SIO instruction status error. |
| 0203 | TIO instruction indicates controller busy 50 usec after SIO. Expect UE. |
| 0204 | TIO instruction indicates status error after SIO (invalid order). Expected UE, controller not busy. |
| 0205 | TIO instruction terminal byte count not = 1 indicating controller accepted one byte for invalid order. |

TST1, 03 Format Order - Inhibit Upspace. A format order of a byte count of one, then a byte count of two is issued. Terminal status is verified and that no paper motion has occurred.

| | |
|---|---|
| 0301 | SIO status error for format order. |
| 0302 | Device, controller busy beyond normal termination time for format order. |
| 0303 | Paper motion occurred for a format with inhibit upspace. |
| 0304 | Status error for format order. |
| 0305 | Byte count did not decrease after format order. |

TST1, 05 Interrupt Generation and HIO, AIO Instruction Resetting. The following orders are issued: X'03', X'03', and X'00' in order to test the generation of ICE, IZC and IUE. AIO and HIO instructions are issued to test the interrupt clearing.

| | |
|---|---|
| 0501 | TIO instruction indicates IP status not present after X'03' order with ICE flag set. |
| 0502 | TIO instruction condition code or status error after X'03' order issued with ICE flag set. |
| 0503 | AIO instruction condition code, status or device address error following a X'03' order raising IP. |
| 0504 | HIO instruction did not clear IP in controller. |
| 0505 | TIO instruction indicates IP not set by X'03' order with IZC flag set. |
| 0506 | TIO instruction condition code or status error after X'03' order with IZC flag set. |
| 0507 | AIO instruction condition code, status or device address error after X'03' order with IZC flag set. |
| 0508 | AIO or HIO instruction did not reset IP status in controller. |
| 0509 | TIO indicates X'00' order with IUE flag set did not set IP in controller. |
| 0510 | TIO indicates condition code or status error after X'00' order with IUE flag set. |
| 0511 | AIO condition code, status or device address error after X'00' order with IUE flag set. |
| 0512 | TIO indicates no UE status for X'00' order. |
| 0513 | TIO condition code or status error after AIO or HIO issued with IP status present. |
| 0514 | AIO did not reset IP status in controller. |

TST1, 06 IO Interrupt Generation. A format with ICE flag is issued. Verify that the program is interrupted when the IO interrupt is armed and enabled.

| | |
|---|---|
| 0601 | TIO instruction indicates IP not set by SIO, IO interrupt is disarmed. |
| 0602 | Program was interrupted while IO interrupt was disarmed. |
| 0603 | Program was not interrupted while IO interrupt was armed/enabled. |
| 0604 | TIO indicates IP not cleared by an AIO instruction. |

TST1, 07 Print with Format - Inhibit Upspace (blank characters). A print with format order is issued to perform a print operation with inhibit upspace format. Terminal status and no paper motion is verified. Bytes of 2 through 134 are transferred.

| | |
|---|---|
| 0701 | TDV status error. |
| 0702 | Byte count not equal to zero after a print with format order. |
| 0703 | IL not set for byte count greater than 132. |
| 0704 | IL set for byte count less or equal to 132. |
| 0705 | Status error for print with format. |
| 0706 | SIO status error for print with format. |

TST1, 08 Data Transmission Complete (DTC) Interrupt. Using print with format and interrupt on data transmission complete, verify data transmission complete interrupt is generated.

| | |
|---|---|
| 0801 | Data transmission complete interrupt not generated. |
| 0802 | TIO indicates condition code or status error for X'45' order. Expected IP status. |
| 0803 | AIO condition code, status or device address error after DTC interrupt generated in controller expected AIO status bit 1 set. |

TST1, 09 Command Chaining. Using the invalid order, verify the command chaining operation; verify that the UE status terminates the command chaining.

| | |
|---|---|
| 0901 | TIO indicates controller busy beyond normal termination time for command chain operation. |
| 0902 | TIO indicates status error during command chaining operation. |
| 0903 | TIO indicates operational status error following command chain operation. |
| 0904 | Byte count not 0 following command chaining operation. |
| 0905 | TIO indicates command chaining terminated with first IOCD instead of second IOCD. |
| 0906 | Controller busy with invalid order. |
| 0907 | TIO indicates UE not generated for invalid order. |
| 0908 | TIO status error following invalid order command chained. |
| 0909 | Terminal byte count zero following an invalid order command chained. |
| 0910 | Command chaining not terminated by UE of invalid order. |
| 0911 | SIO status error for invalid order command chained. |
| 0912 | SIO status error for command chained. |

TST1, 11 Format - Space One Line. A format order is issued to space one line. Verify that paper motion and no print operation occurs.

| | |
|---|---|
| 1101 | Status error for format order. |

TST1, 13 Print Broadside Pattern. A broadside pattern of all characters are printed. Terminal status is tested.

1301 Status error for broadside line.

TST1, 14 Print - Sliding One Column Pattern. Print with auto upspace is issued with incrementing byte counts of a sliding 1 column pattern. Verify that no print errors occur.

1401 Status error for a print order.

TST1, 15 Unavailable Character Print Test. This test will print a line composed of all 8-bit codes between 0 and 127 corresponding to unavailable characters followed by a similar line composed of all 8-bit codes between 128 to 255 corresponding to unavailable characters.

1501 Invalid characters print status error for 8-bit codes 0 to 127.
1502 Invalid characters print status error for 8-bit codes 128-255.

TST1, 17 Space Line Test. This test will issue space lines to test the correct mapping of the format code. Operation is to observe if line printer have spaced the correct space.

1701 Space XX lines IO status error.
1702 Skip to top of page IO status error.

TST1, 18 Skip Channel Test. This test will issue skip to channel to test the correct mapping of the format code. Operator to observe the line printer have skipped to the correct channel.

1801 Skipped to channel XX IO status error.
1802 Print message IO status error.

TST1, 19 Detect Top of Page Test. This test will issue skip to bottom of page then space one line until top of page is detected.

1901 Skip to bottom of page IO status error.
1902 Space one line IO status errors.
1903 Top of page not detected.

TST1, 20 Pattern and Format Test. Run a selected set of utility tests in sequence. Verify that no print error or paper fault occur.

2001 Status error for hammer registration.
2002 Status error for checkerboard pattern.
2003 Status error for ripple test pattern.
2004 Status error for printer speed test.
2005 Status error for printer load test.
2006 Status error for skip line test.
2007 Status error for channel search test.
2008 Status error for paper slew speed test.

TST1, 22 IOP Halt Test (Sigma 7-9). This test will generate an IOP halt at the end of a data transmission of 1 through 8 bytes with upspacing inhibited. After the generation of each IOP halt the entire line will be printed. This will verify the inhibit upspace and response to an IOP Halt.

2201 SIO status error with two TIC's.
2202 IO status error with two TIC's.
2203 SIO status error with one TIC.
2204 IO status error with one TIC.

FUNCTIONAL TEST (TST1) (SS 1 = 0, SS3 = 1)
INITIALIZING CONDITIONS AND EXPECTED RESULTS

1. Initializing Conditions: None
2. Expected Results:

| SUBTEST | RESULTS |
|---|---|
| TST1, 11 | Space 1 line |
| TST1, 13 | Print 64 lines broadside pattern of all printable characters |
| TST1, 14 | Print 132 sliding one column pattern |
| TST1, 15 | Print 2 lines of unavailable characters |
| TST1, 17 | Space many lines |
| TST1, 18 | Skip many lines |
| TST1, 19 | Go to top of page |
| TST1, 20 | Print 32 lines broadside character 'E'<br>Print 32 lines of alternating blank and character 'E'<br>Print 132 lines of ripple test pattern<br>Print 36 printer speed test<br>Print 263 printer load test pattern<br>Space 1 to 15 lines in sequence two times<br>Skip to channel 1 to 12 in sequence two times<br>Space 15 lines paper slew speed test |
| TST1, 22 | Print 8 lines of all XXXX characters |

# Section 14

# SIGMA 5 - 9

# INTERFACE AND SWITCH REFERENCE DATA

## Section 14

## CONTENTS

Page

Sigma Memory Processor Interface . . . . . . . . . . . . . . . . . . . . . . . . . . . . 14-1
Sigma IOP – Device Controller Interface . . . . . . . . . . . . . . . . . . . . . . . . . 14-6
Sigma DIO Interface . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 14-12
Sigma CPU – IOP Interface . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 14-14
Sigma 9 High-Speed RAD Interface . . . . . . . . . . . . . . . . . . . . . . . . . . 14-17
Sigma Extended Performance and Medium Speed RAD Interface . . . . . . . . . . 14-20
Sigma 9 Access Code Card Selection . . . . . . . . . . . . . . . . . . . . . . . . . 14-21
Sigma 9 Map Register Card Selection . . . . . . . . . . . . . . . . . . . . . . . . . 14-22
Sigma 8/9 Write Locks Card Selection . . . . . . . . . . . . . . . . . . . . . . . . 14-23
Sigma 8/9 General Register Card Selection . . . . . . . . . . . . . . . . . . . . . . 14-24
Sigma 6/7 Map Register Card Selection . . . . . . . . . . . . . . . . . . . . . . . . 14-25
Sigma 6/7 Lock Code Card Selection . . . . . . . . . . . . . . . . . . . . . . . . . 14-26
Sigma 6/7 Program Control Bits Card Selection . . . . . . . . . . . . . . . . . . . 14-27
Sigma 6/7 General Register Card Selection . . . . . . . . . . . . . . . . . . . . . . 14-28
Sigma 5 General Register Card Selection . . . . . . . . . . . . . . . . . . . . . . . 14-29
Sigma 8/9 CPU, MIOP, RIOP Switches . . . . . . . . . . . . . . . . . . . . . . . . 14-30
Sigma 8/9 Memory Switches . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 14-31
Sigma 5/7 Memory Switches . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 14-32
Sigma 5/7 Memory Configuration . . . . . . . . . . . . . . . . . . . . . . . . . . . 14-33
Sigma 9 Memory Remote Configuration . . . . . . . . . . . . . . . . . . . . . . . . 14-34
Sigma 5/7 Switches . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 14-35
Sigma 30 OHM Cable Card Relationships . . . . . . . . . . . . . . . . . . . . . . . 14-38
Sigma 7 Port Expander . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 14-39
Sigma 7 – 8457 Memory Interface . . . . . . . . . . . . . . . . . . . . . . . . . . 14-40
Sigma 7 CPU External Interrupt . . . . . . . . . . . . . . . . . . . . . . . . . . . 14-41
Sigma 7 REU Interfaces . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 14-42
Sigma 7 CPU – Decimal, Power Monitor, Memory, IOP Interfaces . . . . . . . . . . 14-43
Sigma 8/9 MIOP Single Phase Operation Program . . . . . . . . . . . . . . . . . . 14-44

SIGMA 8/9 MEMORY - PROCESSOR INTERFACE

| CABLE | PIN PANEL | Cable 1 | Cable 2 | Cable 3 | Cable 4 | Cable 5 | Cable 6 |
|---|---|---|---|---|---|---|---|
| 1/A | D 2<br>R 6 | M01 | M15 | M29 | L16 | AH | L10 |
| 2/B | D 1<br>R 4 | M00 | M14 | M28 | L15 | MQ | L11 |
| 3/C | D 9<br>R 10 | M03 | M17 | M31 | L18 | DR | L12 |
| 4/D | D 3<br>R 8 | M02 | M16 | M30 | L17 | AR | L13 |
| 5/E | D 12<br>R 13 | M04 | M18 | L29 | L19 | PE | L14 |
| 6/F | D 15<br>R 18 | M05 | M19 | L30 | L20 | SRA | L32 |
| 7/G | D 19<br>R 20 | M06 | M20 | L31 | L21 | M32 | MFI |
| 8/H | D 23<br>R 22 | M07 | M21 | MW0 | L22 | ABO | DBUSY |
| 9/K | D 25<br>R 27 | M08 | M22 | MW1 | L23 | POK | MUWS |
| 10/L | D 33<br>R 34 | M09 | M23 | MW2 | L24 | MR | MUWC |
| 11/M | D 35<br>R 36 | M10 | M24 | MW3 | L25 | HPQ | SIGMA9 |
| 12/N | D 37<br>R 38 | M11 | M25 | DG | L26 | ORIL | |
| 13/P | D 39<br>R 40 | M12 | M26 | EDR | L27 | HOF | |
| 14/R | D 45<br>R 42 | M13 | M27 | OM | L28 | MFR | |
| SIGMA 8/9<br>CPU | | ADD<br>03L,AG60 | ADD<br>05L,AG60 | ADD<br>10K,AG60 | ADD<br>02K,AG61 | ADD<br>07L,AG60 | ADD<br>06K,AG60 |
| MIOP | P: | 14C,AG60 | 17C,AG60 | 23C,AG60 | 25C,AG60 | 19C,AG60 | 27C,AG60 |
| RIOP | | 26D,AG70 | 30D,AG70 | 15C,AG60 | 11C,AG60 | 18C,AG60 | 13C,AG60 |
| MEMORY | P1: | 06C,AG60 | 08C,AG60 | 07B,AG60 | 08A,AG10 | 05B,AG60 | 06A,AG60 |
| | P2: | 10C,AG60 | 12C,AG60 | 11B,AG60 | 12A,AG10 | 09B,AG60 | 10A,AG60 |
| | P3: | 23C,AG60 | 21C,AG60 | 22B,AG60 | 21A,AG10 | 24B,AG60 | 23A,AG60 |
| | P4: | 27C,AG60 | 25C,AG60 | 26B,AG60 | 25A,AG10 | 28B,AG60 | 27A,AG60 |
| SIGMA 5/6/7<br>5CPU | | 12M,AT11 | 25P,AT11 | 18R,AT11 | 15R,AT12 | 15S,AT11 | |
| 6/7CPU | | 21S,AT11 | 19P,AT11 | 27N,AT11 | 15Y,AT11 | 14V,AT11 | |
| MIOP | | 18A,AT11 | 16A,AT11 | 14A,AT70 | 12A,AT61 | 10A,AT11 | |
| SIOP | | 20D,AT11 | 18D,AT11 | 15D,AT11 | 11D,AT12 | 13D,AT11 | |
| MEMORY | A | 02A,AT11 | 02B,AT11 | 04A,AT11 | 04C,AT10 | 06C,AT11 | |
| (OLD) | B | 06A,AT11 | 06B,AT11 | 04B,AT11 | 02D,AT10 | 04D,AT11 | |
| | C | 08A,AT11 | 08B,AT11 | 08C,AT11 | 06D,AT10 | 08D,AT11 | |
| MEMLRY | 1 | 09B,AT60 | 10A,AT60 | 08A,AT60 | 06C,AT60 | 07B,AT60 | |
| (NEW) | 2 | 14B,AT60 | 15A,AT60 | 13A,AT60 | 11C,AT60 | 12B,AT60 | |
| | 3 | 19B,AT60 | 18A,AT60 | 20A,AT60 | 22C,AT60 | 21B,AT60 | |
| | 4 | 24B,AT60 | 23A,AT60 | 25A,AT60 | 27C,AT60 | 26B,AT60 | |
| CFE-3 | | 32B,AT11 | 30B,AT11 | 28B,AT11 | 24B,AT12 | 26B,AT11 | |

## MEMORY-PROCESSOR INTERFACE

| | |
|---|---|
| ABO | Abort Signal - generated by CPU only.<br>As a result of a write protect violation, overrides a write operation and prevents changing the contents of memory. |
| AH | Address Here - generated by addressed port.<br>Indicates particular address exists. |
| AR | Address Release - generated by addressed port.<br>Indicates that memory cycle has started and Processor can drop MQ, L, MW, OM signals. |
| DBUSY | Data Bus Busy - generated by addressed port.<br>Inhibits data transmission from other banks on that port. Only used by memory units. |
| DG | Data Gate - generated by addressed port.<br>During read operations gates data into Processors (MIOP) input register. |
| DR | Data Release - generated by addressed port.<br>Indicates during write operation that the data lines may be dropped, during read operation indicates that next memory cycle can use data bus. |
| EDR | Early Data Release - generated by addressed port.<br>During read cycle RIOP uses signal to clear receiving register. Sigma 8/9 CPU delays signal and generates Internal DG. |
| HOF | Halt on Fault - generated by CPU PCP. (Unused by Sigma 8/9)<br>Causes address memory to stay busy until PE is cleared. |
| HPQ | High Priority Request - generated by Processor.<br>Indicates requesting Processor wants priority changed to higher queue, used with MQ. (Unused in Sigma 5-7 processors, wired high in Sigma 9 MIOP, low in CPU but dynamic in Sigma 9 RIOP) |
| L10-L31 | Address Lines - sent by Processor.<br>Location processor is requesting, signals must remain stable until AR. |
| L32 | Address Parity Line - generated by Processor.<br>Odd parity bit for L10-L31, MW0-MW3 and OM. |

## Memory-Processor Interface (Continued)

| | |
|---|---|
| M00-31 | Memory Data Lines - bidirectional lines.<br>During read cycle reset at DR time, during write cycle strobed. |
| M32 | Memory Data Parity Line - bidirectional line.<br>Odd parity bit for data lines M00-M31. |
| MFI | Memory Fault Interrupt - generated by port.<br>Indicates to Processor a Data Loop Check Error, Parity Error, Overtemp or Voltage Irregularities in magnetics. Reset by MFR or MR. |
| MFR | Memory Fault Reset - generated by CPU.<br>Resets memory fault latch, status latches and the memory fault light signals in all ports connected to CPU bus. |
| MQ | Memory Request - generated by Processor. (Unused by Sigma 8/9)<br>Initiates a request for a memory cycle in the addressed memory. |
| MR | Memory Reset - generated by CPU.<br>Resets memory. |
| MUWC | Multiple Word Control - generated by Processor.<br>N/A, not currently used. |
| MUWS | Multiple Word Service - generated by Processor.<br>N/A, not currently used. |
| MW0-MW3 | Memory Write Byte Lines - generated by Processor.<br>Used with OM to determine memory operation. If OM is false then MW0-MW3 indicates which bytes are to be written into memory. Reset by AR. |
| OM | Operating Mode - generated by CPU.<br>In conjunction with MW0-MW3 determines the type of memory operation. |

14

Memory-Processor Interface (Continued)

| OM | MW0 | MW1 | MW2 | MW3 | Sigma 9 Memory Response |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | Read |
| 0 | X | X | X | X | Any bit set will cause that byte to be written into memory. |
| 1 | 0 | 0 | 0 | 0 | Load and Set |
| 1 | 0 | 0 | 0 | 1 | Read and Inhibit Parity Trap |
| 1 | 0 | 0 | 1 | 0 | Read and Change Parity – force P.E. |
| 1 | 0 | 1 | 1 | 1 | Set Memory Margins |
| 1 | 1 | 0 | 0 | 0 | Read Status Word 0 |
| 1 | 1 | 0 | 0 | 1 | Read Status Word 1 |
| 1 | 1 | 0 | 1 | 0 | Read Status Word 2 |
| 1 | 1 | 1 | 0 | 0 | Read Status Word 0 and clear all status |
| 1 | 1 | 1 | 1 | 0 | Read Status Word 2 and clear all status |
| 1 | 1 | 1 | 1 | 1 | Clear Memory |

| | |
|---|---|
| ORIL | Override Interleaving – generated by CPU PCP.<br>Disables interleaving for all banks. |
| PE | Parity Error – generated by port.<br>Indicates uncorrectable magnetic data parity error for read or partial write cycles, address or data bus parity at port, or port selection error in driver or matrix. (Different significance for Sigma 7 vs Sigma 9 memory) |
| POK | Parity OK – generated by port.<br>No PE conditions (see above). |

## Memory-Processor Interface (Continued)

| | |
|---|---|
| SIGMA 9 | Generated by Processor.<br>Indicates all memory interfaces are to be parity checked and also selects faster interface timing. |
| SRA | Second Request Allowed - generated by port.<br>Indicates to CPU, during read operation, that a new memory request can be initiated. Not used by Sigma 9 system. |

### IOP - DEVICE CONTROLLER INTERFACE

| | | (AT56) | | (AT57) | | | |
|---|---|---|---|---|---|---|---|
| CABLE | PANEL | Cable 1 | Cable 2 | Cable 3 | Cable 4 | Cable 5 | Cable 6 |
| 1/A | D 2<br>R 6 | FR7 | DA7 | RST (15) | HPI (35)<br>(06) | DB0 | DC4 |
| 2/B | D 1<br>R 4 | FR6 | DA6 | CL1 (07) | HPS (33)<br>(09) | DB1 | DC5 |
| 3/C | D 9<br>R 10 | FR5 | DA5 | ES (17) | FAST (31)<br>(10) | DB2 | DC6 |
| 4<br>D | D 3<br>R 8 | FR4 | DA4 | RSA (18) | AVO (29)<br>AVI (08) | DB3 | DC7 |
| 5/E | D 12<br>R 13 | FR3 | DA3 | SIO ($) | | DB4 | BM |
| 6/F | D 15<br>R 18 | FR2 | DA2 | HIO ($) | | DB5 | DD0 |
| 7/G | D 19<br>R 20 | FR1 | DA1 | TIO (19) | AVIH1 | DB6 | DD1 |
| 8/H | D 23<br>R 22 | FR0 | DA0 | TDV (22) | AVIH2 | DB7 | DD2 |
| 9/K | D 25<br>R 27 | RS (07) | DAP | AIO (30) | DCOFF (30)<br>(02) | EDX2 | DD3 |
| 10/L | D 33<br>R 34 | IOR (47) | ED | ASC (33) | | DC0 | DD4 |
| 11/M | D 35<br>R 36 | FSL (50) | PC | FS (36) | | DC1 | DD5 |
| 12/N | D 37<br>R 38 | DX2 (45) | DOR | SIC (35) | AT83 | DC2 | DD6 |
| 13/P | D 39<br>R 40 | IC (43) | SC | WADR (44) | PANEL | DC3 | DD7 |
| 14/R | D 45<br>R 42 | DX4 (39) | AP | IER (45) | | EDX4 | |
| SIGMA 8/9<br>MIOP | | 13H,AG70 | 10G,AG70 | 04G,AG70 | 04H,AG60 | 09F,AG70 | 12E,AG70 |
| MAINT.SUB | | 10J,AT56 | 13J,AG70 | 17J,AT57 | 04H,AG60 | 15J,AG70 | 27J,AG70 |
| SIGMA 5/6/7<br>IIOP 5 | | 10L,AT10 | 08L,AT11 | 09F,AT12 | 09E,AT11 | | |
| MIOP | | 14B,AT10 | 32A,AT11 | 14C,AT12 | 01D,AT11 | 19C,AT11 | 29A,AT11 |
| SIOP | 14 | 14E,AT10 | 21E,AT11 | 11E,AT12 | 09E,AT11 | 19E,AT11 | 17E,AT11 |
| MAINT.SUB | | 31A,AT56 | 29A,AT60 | 27A,AT57 | 25A,AT83 | 19A,AT60 | 17A,AT60 |
| EP RAD 7231 | | 32C,AT12 | 30C,AT11 | 28C,AT10 | 26C,AT83 | 28B,AT11 | 31B,AT11 |
| HS RAD 7211 | | 32D,AT12 | 30D,AT11 | 28D,AT10 | 26D,AT83 | 27C,AT11 | 30C,AT11 |
| DISK PAK | | 32B,AT56 | 30B,AT60 | 28B,AT57 | 26B,AT83 | 29A,AT60 | 31A,AT60 |
| 1 BYTE CONT | | 32x,AT12 | 30x,AT11 | 28x,AT10 | 26x,AT83 | | |
| PERF SW | X | 32B,AT61 | 30B,AT60 | 28B,AT10 | 26B,AT38 | | |
| | | 24B,AT61 | 22B,AT60 | 20B,AT10 | 18B,AT38 | | |
| | | 32A,AT10 | 30A,AT11 | 28A,AT12 | 26A,AT11 | | |
| PERF SW (7722) | | | | | X | 23A,AT60 | 21A,AT60 |
| | | | | | Y | 15A,AT60 | 13A,AT60 |
| | | | | | Switched | 19A,AT11 | 17A,AT11 |

## IOP-DEVICE CONTROLLER INTERFACE

| | |
|---|---|
| AIO | Acknowledge I/O Interrupt - generated by IOP during AIO instruction.<br>Used with FS and IC to identify type of instruction CPU is requesting interrupting device controller to perform. |
| ASC | Acknowledge Service Call - generated by IOP.<br>Used with FS and SC to signal that IOP is free to begin requested service cycle with highest priority device. |
| AP | Address Parity - generated by Device Controller.<br>Odd parity bit for FR0–7 during service cycles. Currently only recognized by Sigma 9 MIOP. (DX2 used to request address parity check) |
| AVI | Available Input - signal received by Device Controller.<br>Used with FS and function indicators to establish priority for a service cycle. |
| AVIH1<br>AVIH2 | Available Input - generated by IOP.<br>High levels used by special terminator to generate AVI into highest priority device controller. |
| AVO | Available Output - signal generated by Device Controller.<br>Indicates to next device controller that this D.C. has received FS and was not addressed. |
| BM | Burst Mode - generated by Device Controller.<br>Request IOP to continue service connection. Wide interface must be used (EDX4, DX4, NIER). Currently only recognized by Sigma 9 MIOP. |
| CL1 | 1.024MH - clock transmitted by IOP.<br>Crystal controlled signal driven continuously by CPU. |
| DA0–7 | Data Lines - bidirectional.<br>Exchange of data on DA lines controlled by RS and RSA. |

## IOP-Device Controller Interface (Continued)

| | DA LINES | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| IOP Uses | | | | | | | | |
| TTSH | Device/Device Controller Address | | | | | | | |
| ORDER OUT | Order Byte | | | | | | | |
| DATA OUT | Data Byte | | | | | | | |
| TERMINAL ORDER | INT | CDN | CCH | IOPH | AE | Not Used | | |
| Device Controller Uses | | | | | | | | |
| AIO | Status | | | | | | | |
| DATA IN | Data Byte | | | | | | | |
| ORDER IN | TE | IL | CM | CE | UE | Not Used | | |

| | |
|---|---|
| DAP | Data Parity Line - bidirectional.<br>Odd parity for data path in use, always generated by IOP, Device Controller may or may not generate (see PC). |
| DB, DC, DD0-7 | Data Lines - bidirectional.<br>Optional data lines used during 4-byte data transfer sequences only. Controlled by DX4, EDX4 and IER. |
| DCOFF | Device Controller Off - generated by Maintenance Subcontroller.<br>Causes all device controllers to Go Off line. Program controllable FF generates signal. Only recognized by AT83, AT87. |
| DOR | Data/Order Request - generated by Device Controller.<br>Identifies request (RS) during service cycles and condition code 2 during I/O Instruction. |
| DX2 | Two Byte Request - generated by Device Controller. Also see AP. |

## IOP-Device Controller Interface (Continued)

| | |
|---|---|
| DX4 | Four Byte Request - generated by Device Controller.<br>Device Controller is requesting IOP to use wide interface (DA, DB, DC and DD lines) for data path, requires that Device Controller have wide interface option and that the IOP signal has signalled wide interface option (EDX4). |
| ED | End Data - bidirectional line.<br>The IOP or Device Controller may raise ED to indicate no more data is to be transferred in this service sequence. If ED is true and ES is false IOP is signaling device Controller that a terminal order must be requested. |
| EDX2 | Enable Two Byte - generated by IOP.<br>Indicates IOP has wide interface (DA, DB line) installed, used with DX2, IER. (Not used in Sigma 5-9) |
| EDX4 | Enable Four Byte - generated by IOP.<br>Indicates IOP has wide interface (DA, DB, DC and DD lines) installed, used with DX4, IER. |
| ES | End Service - generated by IOP.<br>The IOP drives ES and RSA to indicate the service sequence is to terminate on the byte being transferred. |
| FAST | Fast - generated by Device Controller.<br>No ZBCI during Data chaining. |
| FR0-FR7 | Function Response Lines - generated by addressed Device Controller.<br>When DC is responding to FS accompanied by a TTSH (TIO, TDV, SIO, HIO), indicator FR0-7 carry D.C. status. During ASC or AIO functions FR0-7 are driven with device address. |
| FS | Function Strobe - generated by IOP.<br>Indicates device controllers should look at function indicators when they receive AVI.<br>During TTSH addressed device controller responds by raising FSL, with status on FR0-7. During AIO or ASC highest priority calling (IC or SC) device controller responds by raising FSL, with DC add on FR0-7. FS and FSL work in a closed-loop manner. |

## IOP-Device Controller Interface (Continued)

| | |
|---|---|
| FSL | Function Strobe Acknowledge - generated by device controller.<br>Indicates to IOP that a device controller has received AVI and identified the operation that the IOP signaled on the function lines. FS and FSL work in a closed-loop manner. (See FS) |
| HIO | Halt I/O Device - generated by IOP.<br>Used with FS and DA0-7 to identify type of instruction CPU is requesting addressed device controller to perform. |
| HPI | High Priority Interrupt - generated and used by device controller.<br>Used by device controller to put itself into high priority queue for AIO function. No standard XDS equipment raises this line. |
| HPS | High Priority Service - generated and used by device controller.<br>Used by device controller to put itself into high priority queue for ASC function. No standard XDS equipment raises this line. |
| IC | Interrupt Call - generated by device controller.<br>Signal passed thru IOP to CPU causing interrupt to X'5C'. |
| IER | Inhibit Extended Request - generated by IOP.<br>Denies device controller usage of wide interface because of non word bound byte address or insufficient byte count, used to override DX4, EDX4. |
| IOR | Input/Output Request - generated by device controller.<br>Identifies request (RS) during service sequence, High Output, Low Input; condition code information during TTSH AIO sequence, H = >NCOND1. |
| PC | Parity Check - generated by IOP and some Device Controllers.<br>Request for parity to be checked on DATA (DA0-7). |
| RS | Request Strobe - generated by service connected Device Controller.<br>Signals to the IOP that a data byte is to be exchanged on the DA lines. RS and RSA work in closed-loop manner. |
| RSA | Request Strobe Acknowledge - generated by IOP.<br>Signals to the device controller that exchange of data byte is complete, i.e. during input operation IOP has accepted byte sent by D.C., during output operation IOP is sending requested data byte. |
| RST | Reset - generated by IOP.<br>Reset signal to all device controllers generated by CPU PCP I/O reset, or SYST reset switch, or as a result of a RIO instruction. (Sigma 9 only) |

## IOP–Device Controller Interface (Continued)

| | |
|---|---|
| SC | Service Call - generated by device controller.<br>Device controllers use this line to request an IOP service cycle. The IOP will respond with FS and ASC. |
| SIC | Special Interrupt Call - generated by IOP.<br>Used when FAST is true to indicate ZBCI during Data Chaining, not used. |
| SIO | Start I/O Device - generated by IOP.<br>Used with FS to identify type of instruction CPU is requesting addressed device controller to perform. FS is driven to DC's after SIO indicator and DA0–7 (Device Address). |
| TDV | Test Device - generated by IOP.<br>Used with FS to identify type of instruction CPU is requesting addressed D.C. to perform. |
| TIO | Test I/O - generated by IOP.<br>Used with FS to identify type of instruction CPU is requesting address controller to perform. |
| WADR | Word Aligned Data Required - generated by IOP.<br>Full word being transmitted. Sigma 3 uses.<br>Static line held true by IOP not capable of byte alignment on wide interface. |
| ZBCI | Zero Byte Count Interrupt - generated by SIOP.<br>Used when controller drives FAST, driven by SIOP when IZBC and DC flags are true and zero byte count is reached. |

## DIO INTERFACE

| CABLE | BACK PANEL | Cable 1 | Cable 2 | Cable 3 | Cable 4 |
|---|---|---|---|---|---|
| 1/A | D 2<br>R 6 | DB01 | DB15 | DB29 | A03 |
| 2/B | D 1<br>R 4 | DB00 | DB14 | DB28 | A02 |
| 3/C | D 9<br>R 10 | DB03 | DB17 | DB31 | |
| 4/D | D 3<br>R 8 | DB02 | DB16 | DB30 | A04 |
| 5/E | D 12<br>R 13 | DB04 | DB18 | FS | A00 |
| 6/F | D 15<br>R 18 | DB05 | DB19 | FSA | A01 |
| 7/G | D 19<br>R 20 | DB06 | DB20 | WD | A08 |
| 8/H | D 23<br>R 22 | DB07 | DB21 | A05 | A09 |
| 9/K | D 25<br>R 27 | DB08 | DB22 | A06 | A10 |
| 10/L | D 33<br>R 34 | DB09 | DB23 | A07 | A11 |
| 11/M | D 35<br>R 36 | DB10 | DB24 | A12 | CC3 |
| 12/N | D 37<br>R 38 | DB11 | DB25 | A13 | CC4 |
| 13/P | D 39<br>R 40 | DB12 | DB26 | A14 | RES |
| 14/R | D 45<br>R 42 | DB13 | DB27 | A15 | 1MHZ |

| SIGMA 8/9 | REG | AUX | AUX | AUX |
|---|---|---|---|---|
| CPU | 09K,AG60 | 22E,AG60 | 26E,AG60 | 29E,AG60 |
| MIOP | 32B,AG60 | 30B,AG60 | 28B,AG60 | 15B,AG60 |
| RIOP | 04B,AG60 | 07B,AG60 | 01A,AG60 | 03A,AG60 |
| EXT.INTER | | 22E,AG60 | 26E,AG60 | 29E,AG60 |
| SIGMA 5/6/7 | | | | |
| 5CPU | 09M,AT11 | 22Q,AT11 | 26Q,AT11 | 29Q,AT11 |
| 6/7CPU | 23S,AT11 | 27Q,AT11 | 30P,AT11 | 29N,AT11 |
| MAINT.SUB | | 11A,AT11 | 13A,AT11 | 15A,AT11 |
| COC 7611 | | 13B,AT11 | 15B,AT11 | 17B,AT11 |
| PERF. SW (7720) | | | 04A,AT60 | 02A,AT60 |
| DIO ADAP X | | 18A,AT60 | 14A,AT60 | 10A,AT60 |
| (7710) Y | | 16A,AT60 | 12A,AT60 | 08A,AT60 |
| Switched | | 06A,AT11 | 04A,AT11 | 02A,AT11 |
| CFE-3 | 23S,AT11 | 27E,AT11 | 25E,AT11 | 30D,AT11 |

## DIO INTERFACE

| | |
|---|---|
| A00-A15 | Address Lines - generated by CPU.<br>16 least significant bits of the RD/WD instruction. |
| CC3,CC4 | Condition Code Lines - generated by Addressed Device.<br>Can be used by device during RD/WD to set condition codes in CPU. |
| CL1 | 1.024 MHz Clock - generated by CPU.<br>Crystal controlled signal driven continuously by the CPU. |
| DB00-DB31 | Data Bus - bidirectional data lines.<br>During WD, CPU puts R data on lines before sending FS; during RD addressed device puts data on lines before sending FSA. (Some devices use only DB16-31). |
| FS | Function Strobe - generated by CPU.<br>Signals devices to compare address lines (A00-15) with their assigned address. FS and FSA work in a closed-loop manner. |
| FSA | Function Strobe Acknowledge - generated by addressed device.<br>Response to CPU FS. FSA signals CPU that device has recognized address and during WD has accepted data or during RD is transmitting data. FS and FSA work in a closed loop manner. |
| RES | Reset - generated by CPU.<br>Raised by I/O RESET or SYST RESET switch on PCP or during power on or power off. |
| WD | Write Direct - generated by CPU.<br>Sent with address to indicate operation that device is to perform. High = >Write Direct, Low = >Read Direct.<br><br>Address of<br>1xxx = Mode 1 - Interrupt Control<br>2xxx = Mode 2 - Testers<br>30xx = Mode 3 - Communications Equipment<br>9xxx = Mode 9 - Switching Equipment<br>Axxx = Mode A - System Interface Units<br>Bxxx = Mode B - Miscellaneous<br>Cxxx = Mode C - System Interface Units |

## CPU - IOP INTERFACE

| CABLE | BACK PANEL | Sigma 8/9 Cable 1 | Sigma 8/9 Cable 2 | | Sigma 5/6/7 Cable 1 | |
|---|---|---|---|---|---|---|
| 1/A | D 2<br>R 6 | FNC0 | HMSP0 | | FNC0 | |
| 2/B | D 1<br>R 4 | FNC1 | HMSP1 | | FNC1 | |
| 3/C | D 9<br>R 10 | FNC2 | HMSP2 | | FNC2 | |
| 4/D | D 3<br>R 8 | ADRS2 | HMSP3 | | IOPA0 | |
| 5/E | D 12<br>R 13 | ADRS3 | HMSP4 | | IOPA1 | |
| 6/F | D 15<br>R 18 | ADRS4 | HMSP5 | | IOPA2 | |
| 7<br>G | D 19<br>R 20 | *CNST<br>CNST | ADRS1 | | CNST<br>CNST | Component SIDE<br>Etch SIDE |
| 8<br>H | D 23<br>R 22 | *AVL<br>AVL/IN | ADRS0 | | | |
| 9/K | D 25<br>R 27 | NCOND1 | IR1 | | NCOND1 | |
| 10/L | D 33<br>R 34 | NCOND2 | IR2 | | NCOND2 | |
| 11/M | D 35<br>R 36 | CL1S | IR3 | | CL1S | |
| 12/N | D 37<br>R 38 | RIO | PFI | | RIO | |
| 13/P | D 39<br>R 40 | IR0 | COND3 | | IR | |
| 14/R | D 45<br>R 42 | PR | RQ | | PR | |

| | | | | | |
|---|---|---|---|---|---|
| SIGMA 8/9 | | CONT | CONT | | |
| CPU | PBP | 15J,AG13 | 13J,AG60 | | |
| | PBA | 21J,AG13 | 19J,AG60 | | |
| MIOP | PBP | 09D,AG13 | 03D,AG60 | | |
| | PBA | 06D,AG13 | 01D,AG60 | | |
| RIOP | PBP | 18A,AG13 | 16A,AG60 | | |
| | PBA | 13A,AG13 | 11A,AG60 | | |
| SIGMA 5/6/7 | | | | 5CPU | 05F,AT13 |
| | | | | 6/7CPU | 29L,AT11 |
| | | | | MIOP | 12C,AT13 |
| | | | | SIOP | 10F,AT13 |

*These two signals are routed through the circular bus terminator locations, all other signals on cable one are terminated at these locations.

| Sigma 8/9 | Comp side | Etch side | |
|---|---|---|---|
| PBP | 06E,ZT23 & | 04E,ZT23 | in the AUX Frame |
| PBA | 10E,ZT23 & | 08E,ZT23 | in the AUX Frame |

PBP is Processor Bus Primary

PBA is Processor Bus Alternate (OPTIONAL)

Bus selection is by SW1,03J CON CPU
SW1,01B MIOP
SW1,09A RIOP

## CPU - IOP INTERFACE

| | |
|---|---|
| ADRS0-ADRS4 | Processor Address Lines - generated by CPU only.<br>If the Instruction is a TIO TDV SIO HIO POLP POLR or RIO, then lines contain Address of Processor that is to execute the indicated Instruction (FNC). If the Instruction is an AIO, then ADRS3 and 4 contain the number of the CPU issuing the AIO. |
| AVL, AVL/IN | Bus Available - daisy chained signal used by the CPU's (8/9)<br>In a multiprocessor system, indicated that the Bus is not in use. Response to a RQ signal, requesting CPU will stop AVL/IN and not pass AVL to next CPU. |
| CL1S | 1.024 MHz Clock - generated by CPU.<br>Crystal controlled signal driven continuously by the CPU. |
| CNST | Control Strobe - daisey chained signal, originated by a CPU.<br>Causes Processors to interogate address lines (ADRS0-4), the processor that recognized address will process instruction (FNC0-2) and respond with PR. |
| NCOND1,<br>NCOND2,<br>COND3 | Condition Code Lines - driven by addressed processor.<br>Indicates condition code information to the CPU.<br>COND3 used only by Sigma 8/9. |
| FNC0-FNC2 | Function Code Lines - generated by the CPU.<br>Indicates the instruction that the addressed processor is to perform.<br>000 = SIO<br>001 = TIO<br>010 = TDV<br>011 = HIO<br>100 = RIO (8/9)<br>101 = POLP (8/9)<br>110 = AIO<br>111 = POLR (8/9) |
| HMSP0-<br>HMSP5 | Homespace Bias - bidirectional lines (8/9)<br>During TIO TDV SIO or HIO instructions, the CPU sends Homespace so the IOP can access the correctly biased cell 20 and 21. During POLP or POLR instructions, the addressed processor indicates failure to CPU. |

| | 8/9 CPU | 8/9 MIOP | RIOP |
|---|---|---|---|
| HMSP0 | INST. EXCP. TRAP | N/A | N/A |
| HMSP1 | DATA BUS CHECK | DATA BUS CHECK | DATA BUS CHECK |
| HMSP2 | MEMORY PARITY E | CONTROL CHECK | N/A |
| HMSP3 | WATCHDOG TIMER | N/A | N/A |
| HMSP4 | MAP PARITY ERR | N/A | N/A |

## CPU - IOP Interface (Continued)

| | |
|---|---|
| IR0-IR3 | Interrupt Request Lines - generated by IOP's<br>Triggers CPU interrupt X'5C'. One line assigned to each CPU in a multiprocessor system. |
| PFI | Processor Fault Interrupt - generated by erring processor (8/9)<br>Triggers CPU interrupt X'56'. Enabled by BCF or CCF in IOP's. Enabled by double PDF in CPU. |
| PR | Proceed - generated by addressed processor<br>Indicates addressed processor has completed function (FNC0-2). CNST and PR work in a closed-loop manner. |
| RQ | REQUEST - generated by CPU and used only by CPU (8/9)<br>CPU desiring use of Bus raises this line to request usage of bus then waits for AVL/IN before using Bus. |
| RIO | Reset I/O - generated by CPU<br>Raised by I/O RESET or SYST RESET switches on PCP or during power up or power down. |

## SIGMA 9 HIGH-SPEED RAD INTERFACE

| CABLE | | BACK PANEL | Cable 1 | Cable 2 | Cable 3 | | Cable 1 | Cable 2 | Cable 3 |
|---|---|---|---|---|---|---|---|---|---|
| 1/A | D<br>R | 2<br>6 | CMD1 | CMD3 | STAT1 | | WENR | | Pin #<br>for AT27 |
| 2/B | D<br>R | 1<br>4 | CMD2 | CMD4 | STAT2 | | RENR | | |
| 3/C | D<br>R | 9<br>10 | DATA06 | CLOCK | STAT3 | | RD3D<br>WD6R | | DV0D(07) |
| 4/D | D<br>R | 3<br>8 | DATA07 | ID2 | | | DS3D<br>WD7R | | |
| 5/E | D<br>R | 12<br>13 | DATA05 | CLEAR | ADDST7 | | DS1D<br>WD5R | NMANRST | TRPD(19) |
| 6/F | D<br>R | 15<br>18 | DATA04 | STAT0 | ADDST6 | | RD1D<br>WD4R | DVTD | AN6D(21) |
| 7/G | D<br>R | 19<br>20 | DATA03 | DATA15 | ADDST5 | | DS2D<br>WD3R | DS7D | AN5D(20) |
| 8/H | D<br>R | 23<br>22 | DATA02 | DATA14 | ADDST4 | | RD2D<br>WD2R | RD7D | AD4D(33) |
| 9/K | D<br>R | 25<br>27 | DATA01 | DATA13 | ADDST3 | | DS0D<br>WD1R | DS5D | AN3D(31) |
| 10/L | D<br>R | 33<br>34 | DATA00 | DATA12 | ADDST2 | | RD0D<br>WD0R | RD5D | AN2D(34) |
| 11/M | D<br>R | 35<br>36 | WCL | DATA11 | ADDST1 | | SC2R | DS6D | AN1D(44) |
| 12/N | D<br>R | 37<br>38 | CMD0 | DATA10 | ADDST0 | | SLNR | RD6D | AN0D(45) |
| 13/P | D<br>R | 39<br>40 | ID1 | DATA09 | SP | | ID1R | DS4D | SPD(46) |
| 14/R | D<br>R | 45<br>42 | ID0 | DATA08 | IP | | ID0R | RD4D | IPD(47) |
| SIGMA 9<br>RIOP UB: | | | 21H,AG70 | 07H,AG70 | 27H,AG70 | | | | |
| 7212 H.S. RAD SELECTION UNIT | | | | | | | 30A,AT11 | 32A,AT11 | 32B,AT27 |
| 7211 H.S. RAD CONTROLLER | | | | | | | 11A,AT11 | 22A,AT11 | 30A,AT11 |

Signal names given at H.S. RAD Selection Unit Interface.

## 7212 HIGH SPEED RAD INTERFACE

| | |
|---|---|
| AN0–AN6 | Angular Position - sent by Unit Selected<br>Indicates the sector that is currently under the Heads. |
| DS0–DS7 | Data Strobe - sent by Unit Selected<br>Used to clock associated data channel (RD0–RD7) into the deskew logic in the Controller during a read operation. |
| DVT<br>(STAT0) | Device Test - sent by Addressed Unit<br>True if storage unit is being addressed and is operational (Disc up to speed and AC/DC power stable). |
| DVO<br>(STAT3) | Device Operational - sent by Unit Selected<br>True if storage unit is selected and is operational (Disc up to speed and AC/DC power stable). Monitored by controller during operation. |
| ID0–ID1 | Identification Lines - sent by Controller<br>Specifies one of four storage units during an I/O Instruction. |
| IP | Index Pulse - sent by Unit Selected<br>One pulse per revolution of the disc, identifies sector zero. |
| NMANRST<br>(CLEAR) | Not Reset Signal - sent by Controller<br>Inverted reset signal to all storage units. |
| RD0–RD7 | Read Data - sent by Unit Selected<br>Regenerated data from disk. Clocked to controller during a read operation by clock DS0–DS7. |
| REN<br>(CMD2) | Read Enable - sent by Controller<br>Enables data decoders in Unit Selected. |
| SC2<br>(WCL) | 3 MHz Write Clock - sent by Controller<br>Used by Unit Selected to encode and format data (WD0–WD7) for writing on the disc, enabled by write enable signal (WEN). |
| SLN<br>(CMD0) | Select Now - sent by Controller<br>Selects addressed (ID0 and 1) storage unit and deselects all other units during a SIO instruction. |
| SP | Sector Pulse - sent by Unit Selected<br>80 pulses per revolution of disc, identifies beginning of next sector. |

## 7212 High Speed RAD Interface (Continued)

| | |
|---|---|
| TRP | Track Protected - sent by Unit Selected<br>True when selected band is write protected. |
| WD0-WD7 | Write Data Lines - sent by Controller<br>During Write operation, Data for tracks 0 thru 7. During Sector Gap, Band Address on WD2-WD7. |
| WEN<br>(CMD1) | Write Enable - sent by Controller<br>Enables write amplifiers, data encoders and clock doubler. |

## EP AND MS RAD INTERFACE

| CABLE | PANEL | Cable 1 | Cable 2 |
|---|---|---|---|
| 1/A | D 2<br>R 6 | DAT | IP |
| 2/B | D 1<br>R 4 | NMNRST | PWRMONR |
| 3/C | D 9<br>R 10 | SLN | DS |
| 4/D | D 3<br>R 8 | IDS | SP |
| 5/E | D 12<br>R 13 | DAM | DAI |
| 6/F | D 15<br>R 18 | WEN | TRP |
| 7/G | D 19<br>R 20 | REN | DVT |
| 8/H | D 23<br>R 22 | SC2 | DVO |
| 9/K | D 25<br>R 27 | SC1 | TYP0 |
| 10/L | D 33<br>R 34 | SAI | TYP1 |
| 11/M | D 35<br>R 36 | TRK | AN0 |
| 12/N | D 37<br>R 38 | ID0 | AN1 |
| 13/P | D 39<br>R 40 | ID1 | AN2 |
| 14R | D 45<br>R 42 | ID2 | AN3 |
| E.P.RAD<br>CON. 7231 | | 28A,AT12 | 26A,AT10 |
| DEV. 7232 | | 03A,AT10 | 05A,AT12 |
| M.S.RAD<br>CON. 7201 | | 32A,AT12 | 30A,AT10 |
| DEV. 720X | | 18A,AT10 | 28A,AT12 |

## SIGMA 9

### ACCESS CODE CARD SELECTION (FG25)

| MPB REG ADDRESS | LM Lines 15 16 17 18 19 20 | OUTPUT BITS MPB15–22 |
|---|---|---|
| 00 - 3F | 0 0 COLUMN BYTE | 24A |
| 40 - 7F | 0 1 | 23A |
| 80 - BF | 1 0 | 24B |
| C0 - FF | 1 1 | 23B |
| | | AUX FRAME |

### ACCESS CODE FINAL BIT SELECTION

| LM Lines | 21 22 | | OUTPUT | BIT |
|---|---|---|---|---|
| | 0 0 | Selects | MPB15 | MPD16 |
| | 0 1 | Selects | MPB17 | MPB18 |
| | 1 0 | Selects | MPB19 | MPB20 |
| | 1 1 | Selects | MPB21 | MPB22 |
| | | | MPB0 | MPB1 |

### ACCESS CODE WRITE CLOCKS

| MPB REG ADDRESS | Bits 15–22 |
|---|---|
| 00 - 3F | MPBW.CK-13B21 |
| 40 - 7F | MPBW.CK-13B28 |
| 80 - BF | MPBW.CK-13B24 |
| C0 - FF | MPBW.CK-13B43 |
| | AUXILIARY FRAME |

### ACCESS CODE DATA INPUT BITS

| MPB REG ADDRESS | Bits 15–22 |
|---|---|
| 00 - 7F | S24-5 thru S31-5 |
| 80 - FF | S24-6 thru S31-6 |
| | AUXILIARY FRAME |

## SIGMA 9

### MAP REGISTER CARD SELECTION (FG25)

| MAP REG ADDRESS | LM Lines 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | MAP REGISTER OUTPUTS MAP10–14 & P | MAP15–22 |
|---|---|---|---|---|---|---|---|---|---|---|
| 00 - 0F | 0 | 0 | 0 | 0 | C | | BYTE | | 32A | 22A |
| 10 - 1F | 0 | 0 | 0 | 1 | O | | | | 31A | 21A |
| 20 - 2F | 0 | 0 | 1 | 0 | L | | | | 30A | 20A |
| 30 - 3F | 0 | 0 | 1 | 1 | U | | | | 29A | 19A |
| 40 - 4F | 0 | 1 | 0 | 0 | M | | | | 32B | 22B |
| 50 - 5F | 0 | 1 | 0 | 1 | N | | | | 31B | 21B |
| 60 - 6F | 0 | 1 | 1 | 0 | | | | | 30B | 20B |
| 70 - 7F | 0 | 1 | 1 | 1 | | | | | 29B | 19B |
| 80 - 8F | 1 | 0 | 0 | 0 | | | | | 28A | 18A |
| 90 - 9F | 1 | 0 | 0 | 1 | | | | | 27A | 17A |
| A0 - AF | 1 | 0 | 1 | 0 | | | | | 26A | 16A |
| B0 - BF | 1 | 0 | 1 | 1 | | | | | 25A | 15A |
| C0 - CF | 1 | 1 | 0 | 0 | | | | | 28B | 18B |
| D0 - DF | 1 | 1 | 0 | 1 | | | | | 27B | 17B |
| E0 - EF | 1 | 1 | 1 | 0 | | | | | 26B | 16B |
| F0 - FF | 1 | 1 | 1 | 1 | | | | | 25B | 15B |
| | | | | | | | | | AUXILIARY FRAME | |

MAP REGISTER WRITE CLOCKS

| MAP REG ADDRESS | Bits 10–14 & P | Bits 15–22 |
|---|---|---|
| 00 - 3F<br>80 - BF | MAPW-1.CK-13B21 | MAPW-3.CK-13B28 |
| 40 - 7F<br>C0 - FF | MAPW-2.CK-13B24 | MAPW-4.CK-13B43 |
| | AUXILIARY FRAME | |

MAP REGISTER DATA INPUT BITS

| MAP REG ADDRESS | Bits 10–14 & P | Bits 15–22 |
|---|---|---|
| 00 - 7F | S19-5 thru S23-5<br>SPARITY/BY23-1 | S24-5 thru S31-5 |
| 80 - FF | S19-6 thru S23-6<br>SPARITY/BY23-2 | S24-6 thru S31-6 |
| | AUXILIARY FRAME | |

LB REGISTER TRANSFER TERMS

| MAP REG ADDRESS | Bits 10–15 | Bits 16–22 |
|---|---|---|
| 00 - 7F | LBXMAP/A-1 | LBXMAP/A-2 |
| 80 - FF | LBXMAP/B-1 | LBXMAP/B-2 |
| | ADDRESS FRAME | |

## WRITE LOCKS CARD SELECTION (FG25)

| LK REG ADDRESS | 15 | 16 | 17 | 18 | 19 | 20 | OUTPUT BITS LK15–22 |
|---|---|---|---|---|---|---|---|
| 00 - 07<br>20 - 27<br>40 - 47<br>60 - 67<br>80 - 87<br>A0 - A7<br>C0 - C7<br>E0 - E7 | BYTE | | | 0 | 0 | COLUMN | 21K |
| 08 - 0F<br>28 - 2F<br>48 - 4F<br>68 - 6F<br>88 - 8F<br>A8 - AF<br>C8 - CF<br>E8 - EF | | | | 0 | 1 | | 22K |
| 10 - 17<br>30 - 37<br>50 - 57<br>70 - 77<br>90 - 97<br>B0 - B7<br>D0 - D7<br>F0 - F7 | | | | 1 | 0 | | 23K |
| 18 - 1F<br>38 - 3F<br>58 - 5F<br>78 - 7F<br>98 - 9F<br>B8 - BF<br>D8 - DF<br>F8 - FF | | | | 1 | 1 | | 24K |
| | | | | | | | ADD FRAME |

## WRITE LOCKS DATA INPUT BITS

| LK REG ADDRESS | Bits 15–22 |
|---|---|
| 00 - FF | S24-7 thru S31-7 |
| | ADDRESS FRAME |

## WRITE LOCK WRITE CLOCKS

| LK REG ADDRESS | Bits 15–22 |
|---|---|
| 00 - FF | LKW.CK-31P22 |
| | ADDRESS FRAME |

## WRITE LOCK FINAL BIT SELECTION

| LB Lines | 21 | 22 | | OUTPUT | BIT |
|---|---|---|---|---|---|
| | 0 | 0 | Selects | LK15 | LK16 |
| | 0 | 1 | Selects | LK17 | LK18 |
| | 1 | 0 | Selects | LK19 | LK20 |
| | 1 | 1 | Selects | LK21 | LK22 |
| | | | | LK0 | LK1 |

## SIGMA 8/9

### GENERAL REGISTER CARD SELECTION

| REG BLOCK ADDRESS | RL Lines 26 27 28 29 30 31 | RR00-07 | OUTPUT BITS RR08-15 | RR16-23 | RR24-31 |
|---|---|---|---|---|---|
| 0 | 0 0 C BYTE | 16K | 13K | 14K | 15K |
| 1 | 0 1 L<br>U | 10K | 05K | 06K | 08K |
| 2 | 1 0 M<br>N | 04Q | 01Q | 02Q | 03Q |
| 3 | 1 1 | 26S | 30S | 29S | 27S |
| | | REGISTER FRAME | | | |

### REGISTER CLOCKS

| REG BLOCK ADDRESS | RR00-07 | RR08-15 | RR16-23 | RR24-31 |
|---|---|---|---|---|
| 0 - 3 | RWBY0.<br>CK-03P03 | RWBY1.<br>CK-03P06 | RWBY2.<br>CK-03P43 | RWBY3.<br>CK-03P50 |

### REGISTER INPUT BITS

| REG BLOCK ADDRESS | RR00-31 |
|---|---|
| 0 - 3 | S00 thru S31 |

## SIGMA 6/7

### MAP REGISTER CARD SELECTION (FT25)

| MAP REG ADDRESS | 15 | 16 | 17 | 18 | 19 | 20 21 22 | OUTPUT BITS MAP15-22 |
|---|---|---|---|---|---|---|---|
| 00 - 0F | 0 | 0 | 0 | 0 | C | BYTE | 17Y |
| 10 - 1F | 0 | 0 | 0 | 1 | O | | 18Y |
| 20 - 2F | 0 | 0 | 1 | 0 | L | | 19Y |
| 30 - 3F | 0 | 0 | 1 | 1 | U | | 20Y |
| 40 - 4F | 0 | 1 | 0 | 0 | M | | 21Y |
| 50 - 5F | 0 | 1 | 0 | 1 | N | | 22Y |
| 60 - 6F | 0 | 1 | 1 | 0 | | | 23Y |
| 70 - 7F | 0 | 1 | 1 | 1 | | | 24Y |
| 80 - 8F | 1 | 0 | 0 | 0 | | | 25Y |
| 90 - 9F | 1 | 0 | 0 | 1 | | | 26Y |
| A0 - AF | 1 | 0 | 1 | 0 | | | 27Y |
| B0 - BF | 1 | 0 | 1 | 1 | | | 28Y |
| C0 - CF | 1 | 1 | 0 | 0 | | | 29Y |
| D0 - DF | 1 | 1 | 0 | 1 | | | 30Y |
| E0 - EF | 1 | 1 | 1 | 0 | | | 31Y |
| F0 - FF | 1 | 1 | 1 | 1 | | | 32Y |

### MAP REGISTER WRITE CLOCKS

| MAP REG ADDRESS | Bits 15-22 |
|---|---|
| 00 - 4F | MAPW.CK24U08 |
| 50 - FF | MAPW-1.CK24U08 |

### LB REGISTER TRANSFER TERMS

| MAP REG ADDRESS | Bits 15-22 |
|---|---|
| 00 - FF | MAP-1 & MAP |

### MAP REGISTER DATA INPUT BITS

| MAP REG ADDRESS | Bits 15-22 |
|---|---|
| 00 - 4F | D24 thru D31 |
| 50 - FF | MAPW15 thru MAPW22 |

## SIGMA 6/7

### LOCK CODE CARD SELECTION (FT25)

| LOCK REG ADDRESS | LB Lines | | | | OUTPUT BITS LOCK15-22 |
|---|---|---|---|---|---|
| | 15 | 16 | 17 18 | 19 20 | |
| 00 - 3F | 0 | 0 | COLUMN | BYTE | 05Y |
| 40 - 7F | 0 | 1 | | | 06Y |
| 80 - BF | 1 | 0 | | | 07Y |
| C0 - FF | 1 | 1 | | | 08Y |

### LOCK CODE FINAL BIT SELECTION

| LB Lines | 21 | 22 | | OUTPUT BITS | |
|---|---|---|---|---|---|
| | 0 | 0 | Selects | LOCK15 | LOCK16 |
| | 0 | 1 | Selects | LOCK17 | LOCK18 |
| | 1 | 0 | Selects | LOCK19 | LOCK20 |
| | 1 | 1 | Selects | LOCK21 | LOCK22 |
| | | | | LOCK0 | LOCK1 |

### LOCK REGISTERS

| | LOCK REG ADDRESS | Bit 15-22 |
|---|---|---|
| WRITE CLOCK - | 00 - FF | LOCKW.CK-24U04 |
| INPUT BITS - | 00 - FF | NMAP15 thru NMAP22 |

## SIGMA 6/7

### PROGRAM CONTROL BITS CARD SELECTION (FT25)

| PCB REG ADDRESS | LM Lines 15 | 16 | 17 18 19 20 | OUTPUT BITS PCB15-22 |
|---|---|---|---|---|
| 00 - 3F | 0 | 0 | COLUMN BYTE | 09Y |
| 40 - 7F | 0 | 1 | | 10Y |
| 80 - BF | 1 | 0 | | 11Y |
| C0 - FF | 1 | 1 | | 12Y |

### PROGRAM CONTROL BITS FINAL BIT SELECTION

| LM Lines | 21 22 | | OUTPUT BITS | |
|---|---|---|---|---|
| | 0 0 | Selects | PCB15 | PCB16 |
| | 0 1 | Selects | PCB17 | PCB18 |
| | 1 0 | Selects | PCB19 | PCB20 |
| | 1 1 | Selects | PCB21 | PCB22 |
| | | | NPCB0 | NPCB1 |

### PROGRAM CONTROL BITS

| | PCB REG ADDRESS | Bits 15-22 |
|---|---|---|
| WRITE CLOCK - | 00 - FF | PCBW.CK24U06 |
| INPUT BITS - | 00 - FF | NMAP15 thru NMAP22 |

## SIGMA 6/7

### GENERAL REGISTER CARD SELECTION (FT25)

| REG BLOCK ADDRESS | 23 24 25 26 27 | RR0-7 | RR8-15 | RR16-23 | RR24-31 |
|---|---|---|---|---|---|
| 0 | 0 0 0 0 0 | 01T | 15T | 01L | 01Q |
| 1 | 0 0 0 0 0 | 02T | 16T | 02L | 02Q |
| 2 | 0 0 0 1 0 | 03T | 17T | 03L | 03Q |
| 3 | 0 0 0 1 1 | 04T | 18T | 04L | 04Q |
| REGISTER SELECTION BITS | | LR28-1<br>LR29-1<br>LR30-1<br>LR31-1 | | LR28-2<br>LR29-2<br>LR30-2<br>LR31-2 | LR28-1<br>LR29-1<br>LR30-1<br>LR31-1 |

### REGISTER CLOCKS

| REG BLOCK ADDRESS | RR0-7 | RR8-15 | RR16-23 | RR24-31 |
|---|---|---|---|---|
| 0 - 3 | RWB0.<br>CK-32P47 | RWB1.<br>CK-32P45 | RWB2.<br>CK-32P42 | RWB3.<br>CK-32P43 |

### REGISTER INPUT BITS

| REG BLOCK ADDRESS | RR0-31 |
|---|---|
| 0 - 3 | RW0-31 |

## SIGMA 5

### GENERAL REGISTER CARD SELECTION (FT25)

| REG BLOCK ADDRESS | RP Lines | OUTPUT BITS | | | |
|---|---|---|---|---|---|
| | 24 25 26 27 | RR0-7 | RR8-15 | RR16-23 | RR24-31 |
| 0 | 0 0 0 0 | 09K | 19K | 05S | 09T |
| 1 | 0 0 0 1 | 10K | 18K | 06S | 10T |
| 2 | 0 0 1 0 | 11K | 17K | 07S | 11T |
| 3 | 0 0 1 1 | 12K | 16K | 08S | 12T |
| REGISTER SELECTION BITS | | NIOFM/1<br>LR28-1<br>LR29-1<br>LR30-1<br>LR31-1 | | NIOFM-1<br>LR28-0<br>LR29-0<br>LR30-0<br>LR31-0 | |

### REGISTER CLOCKS

| REG BLOCK ADDRESS | RR0-7 | RR8-15 | RR16-23 | RR24-31 |
|---|---|---|---|---|
| 0 - 3 | RWB0.<br>CK-32P42 | RWB1.<br>CK-32P38 | RWB2.<br>CK-32P45 | RWB3.<br>CK-32P47 |

### REGISTER INPUT BITS

| REG BLOCK ADDRESS | RR0-31 |
|---|---|
| 0 - 3 | RW0 thru RE31 |

## SIGMA 8/9 CPU SWITCHES

| | CONT 03J,SG10 | CONT 02J,SG10 | AUX 03D,SG10 |
|---|---|---|---|
| SW1 | NKPBALT | KCPUN0/D | INTCTRSW1 |
| SW2 | KHMSP12 | KCPUN1/D | INTCTRSW2 |
| SW3 | KHMSP13 | KPBCPUEND | INTCTRSW3 |
| SW4 | KHMSP14 | NKMPCUOP | INTCTRSW4 |
| SW5 | KHMSP15 | - | INTCTRSW5 |
| SW6 | KHMSP16 | - | INTCTRSW6 |
| SW7 | KHMSP17 | - | - |

INTCTRSW 1 & 2 = Counter 1
INTCTRSW 3 & 4 = Counter 2
INTCTRSW 5 & 6 = Counter 3

| | | |
|---|---|---|
| 0 | 0 | 500Mhz |
| 0 | 1 | PWRFREQ |
| 1 | 0 | 2Khz |
| 1 | 1 | EXT FREQ |

## SIGMA 8/9 MIOP SWITCHES

| | 01B,SG10 | 07B,LG26 | 09C,LG26 |
|---|---|---|---|
| SW1 | PB/PRIM | DION0 | - |
| SW2 | DIOABLE/SW | DION1 | CPUN0 |
| SW3 | NCLKMGHI | DION2 | CPUN1 |
| SW4 | - | DION3 | CCUN0 |
| SW5 | - | DION4 | CCUN1 |
| SW6 | - | DION5 | CCUN2 |
| SW7 | - | DION6 | CCUN3 |

## SIGMA 9 RIOP SWITCHES

| | 09A,SG10 | 05A,LG26 | 20A,LG26 |
|---|---|---|---|
| SW1 | PRIALT | MI:ADRSW4 | CPUN0 |
| SW2 | MI:DISABLE | MI:ADRSW5 | CPUN1 |
| SW3 | - | MI:ADRSW6 | RIOPN0 |
| SW4 | - | MI:ADRSW7 | RIOPN1 |
| SW5 | - | MI:ADRSW8 | RIOPN2 |
| SW6 | UBABLE | MI:ADRSW9 | RIOPN3 |
| SW7 | TYPE1/1 | MI:ADRSW10 | RIOPN4 |

## SIGMA 8/9 MEMORY SWITCHES

| | DRIVER A 31B,ST49 | DRIVER A 31C,ST49 | DRIVER A 31A,ST49 |
|---|---|---|---|
| SW1 | SW:UN0 | SW:L12/SA* | CM0 |
| SW2 | SW:UN1 | SW:L13/SA* | CM1 |
| SW3 | SW:UN2 | SW:L14/SA* | CM2 |
| SW4 | SW:UN3 | SW:L15/SA* | CM3 |
| SW5 | - | SW:L16/SA* | CM4 |
| SW6 | SW:L10/SA* | SW:L17/SA* | SW:IL/BBIU* |
| SW7 | SW:L11/SA* | SW:L18/SA* | SW:IL/BTU* |

| DRIVER B 31A,AT49 | |
|---|---|
| CM0 | Early Write |
| CM1 | Late Write |
| CM2 | Early Strobe |
| CM3 | Late Strobe |
| CM4 | Early DR,PE,POK |
| - | |
| - | |

| | MATRIX 0 02C,SG10 | MATRIX 1 02C,SG10 | MATRIX 2 02C,SG10 |
|---|---|---|---|
| SW1 | INHP1* | INHP5* | INHP9 * |
| SW2 | INHP2* | INPH6* | INHP10* |
| SW3 | INHP3* | INHP7* | INHP11* |
| SW4 | INHP4* | INHP8* | INHP12* |
| SW5 | - | - | - |
| SW6 | - | - | - |
| SW7 | - | - | - |

*These Switches must be in the UP position to enable the Remote Cable to the Memory Configuration Panel (MCP).

## SIGMA 5/7 8265/8465 MEMORY SWITCHES

| | | | | |
|---|---|---|---|---|
| | | 31C | 29C | PORT 1/5 |
| | | 20C | 18C | PORT 2/6 |
| | | 15C | 13C | PORT 3/7 |
| | | 04C | 02C | PORT 4/8 |
| | DRIVER A 29B, ST49 | MATRIX , ST49 | MATRIX , ST49 | |
| SW1 | BN0 | L15ASW | L15BSW | |
| SW2 | BN1 | L16ASW | L16BSW | |
| SW3 | BN2 | L17ASW | L17BSW | |
| SW4 | BN3 | L18ASW | L18BSW | |
| SW5 | AUXENB | ENBASW | ENBBSW | |
| SW6 | IL4 | BUSPARSW | - | |
| SW7 | IL2 | CPUBUSSW | | |

## SIGMA 5/7 8265/8465 MEMORY CONFIGURATION INFORMATION

| | | | |
|---|---|---|---|
| SW1 | BN0 | L15ASW | L15BSW |
| SW2 | BN1 | L16ASW | L16BSW |
| SW3 | BN2 | L17ASW | L17BSW |
| SW4 | BN3 | L18ASW | L18BSW |
| SW5 | AUXENB | ENBASW | ENBBSW |
| SW6 | IL4 | BUSPARSW | - |
| SW7 | IL2 | CPUBUSSW | - |

| CABLE | PANEL | 29B, ST49<br>DRIVER A<br>CABLE | ST49<br>MATRIX<br>Port1-31C<br>Port2-20C<br>Port3-15C<br>Port4-04C<br>CABLE | ST49<br>MATRIX<br>Port1-29C<br>Port2-18C<br>Port3-13C<br>Port4-02C<br>CABLE |
|---|---|---|---|---|
| A | 01 | R:BN3 | RPi:L18A | RPi:L18B |
| B | 07 | R:BN2 | RPi:L17A | RPi:L17B |
| C | - | - | - | - |
| D | 24 | R:IL2 | RPi:CPUBUS | - |
| E | - | - | - | - |
| F | - | - | - | - |
| G | 26 | R:IL4 | RPi:BUSPAR | - |
| H | - | - | - | - |
| K | - | - | - | - |
| L | 10 | | | |
| M | 28 | R:AUXENB | RPi:ENBA | RPi:ENBB |
| N | - | - | - | - |
| P | 30 | R:BN1 | RPi:L16A | RPi:L16B |
| R | 44 | R:BN0 | RPi:L15A | RPi:L15B |

## SIGMA 9 MEMORY REMOTE CONFIGURATION CABLE

| PIN | | |
|---|---|---|
| CABLE | PANEL | CABLE |
| A | 1 | - |
| B | 3 | - |
| C | 7 | - |
| D | 10 | - |
| E | 14 | L/R:IL/BBIU |
| F | 18 | L/R:IL/BTU |
| G | 22 | L/R:L10/SA |
| H | 26 | L/R:L11/SA |
| K | 30 | L/R:L12/SA |
| L | 34 | L/R:L13/SA |
| M | 38 | L/R:L14/SA |
| N | 42 | L/R:L15/SA |
| P | 45 | L/R:L16/SA |
| R | 50 | L/R:L17/SA |
| 1 | 4 | L/R:L18/SA |
| 2 | 6 | - |
| 3 | 8 | L/R:INHP1 |
| 4 | 12 | L/R:INHP2 |
| 5 | 17 | L/R:INHP3 |
| 6 | 19 | L/R:IMHP4 |
| 7 | 21 | L/R:INHP5 |
| 8 | 24 | L/R:INHP6 |
| 9 | 28 | L/R:INHP7 |
| 10 | 33 | L/R:INHP8 |
| 11 | 36 | L/R:INHP9 |
| 12 | 40 | L/R:INHP10 |
| 13 | 43 | L/R:INHP11 |
| 14 | 47 | L/R:INHP12 |
| | | 30D, ZT23<br>DRIVER A |

**Port Expansion and Maintenance Switches**

| Memory Location 20C |
|---|
| is PORT B expanded? Yes, set S1-1 |
| is PORT A expanded? Yes, set S1-2 |
| For maintenance MQA set S1-3 |
| For maintenance MQB set S1-4 |
| For maintenance MQC set S1-5 |

**Real Time Clock**

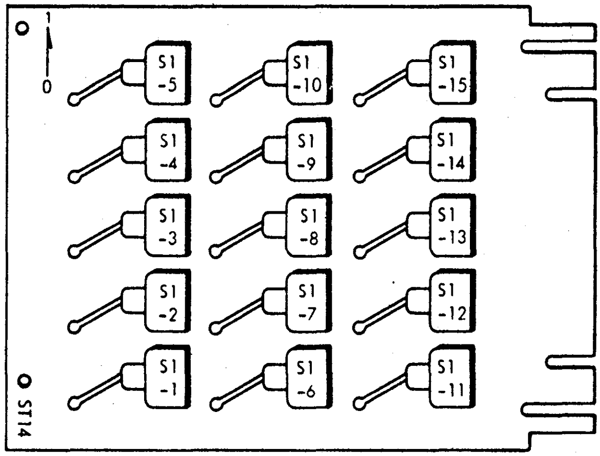
| CPU Location 24W | | | |
|---|---|---|---|
| FREQ | CP3 | CP2 | CP1 |
| 8KHZ | S1-5 | S1-10 | S1-15 |
| 2KHZ | S1-4 | S1-9 | S1-14 |
| 500HZ | S1-3 | S1-8 | S1-13 |
| LINE | S1-2 | S1-7 | S1-12 |
| EXT. | above sw's off | above sw's off | above sw's off |

ea. for 8KHZ
CP3 set (1)
S1-5, reset
(0) S1-4,
S1-3, S1-2

| | |
|---|---|
| 8411 Opt. | LT16 in 15W? No set S1-1, S1-6 |
| Unass. Int. | LT16 in 23W? No set S1-11 |

**Priority Int LT16 Switches**

| Prior. Int Chas ST14 1J | | |
|---|---|---|
| If LT16 is in Loc | Set Switches | Int Level LSD |
| 7J | None | X0, X1 |
| 8J | S1-1, S1-2 | X2, X3 |
| 9J | S1-3, S1-4 | X4, X5 |
| 10J | S1-5, S1-6 | X6, X7 |
| 14J | S1-7, S1-8 | X8, X9 |
| 15J | S1-9, S1-10 | XA, XB |
| 16J | S1-11, S1-12 | XC, XD |
| 17J | S1-13 | XE, XF |



**Memory Fault-Door Number**

| Mem 21C | S1-8 | S1-9 | S1-10 |
|---|---|---|---|
| Door 0 | 0 | 0 | 0 |
| Door 1 | 0 | 0 | 1 |
| Door 2 | 0 | 1 | 0 |
| Door 3 | 0 | 1 | 1 |
| Door 4 | 1 | 0 | 0 |
| Door 5 | 1 | 0 | 1 |
| Door 6 | 1 | 1 | 0 |
| Door 7 | 1 | 1 | 1 |

**Interleave Block Size**

| Mem 21C | S1-3 | S1-4 | S1-5 | S1-6 |
|---|---|---|---|---|
| None | 0 | 0 | 0 | 0 |
| 8K | 1 | 0 | 0 | 0 |
| 16K | 0 | 1 | 0 | 0 |
| 32K | 0 | 0 | 1 | 0 |
| 64K | 0 | 0 | 0 | 1 |

**Memory Size**

| Mem 21C | S1-1 | S1-2 |
|---|---|---|
| 4K | 0 | 0 |
| 8K | 0 | 1 |
| 12K | 1 | 0 |
| 16K | 1 | 1 |

**Memory Starting Address (8451)**

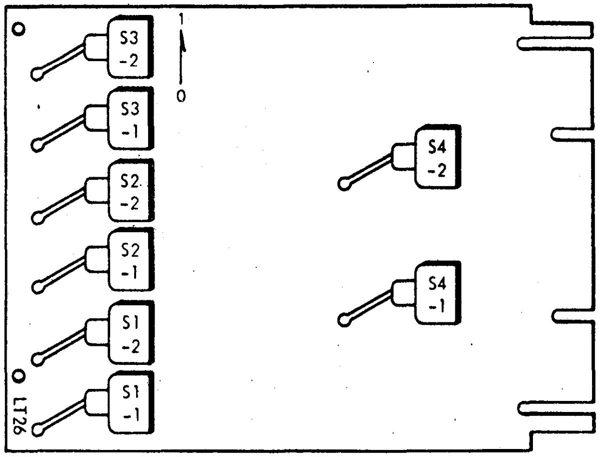
| | Set starting addr sw's for | L15 | L16 | L17 | L18 | L19 |
|---|---|---|---|---|---|---|
| Memory | (20C) Port A | S11 | S12 | S13 | S14 | S15 |
| | (20C) Port B | S6 | S7 | S8 | S9 | S10 |
| | (21C) Port C | S11 | S12 | S13 | S14 | S15 |
| Port expanders F and S | F(24D) S(21E) Port 1 | S1 | S2 | S3 | S4 | S5 |
| | F(24D) S(21E) Port 2 | S6 | S7 | S8 | S9 | S10 |
| | F(25D) S(22E) Port 3 | S1 | S2 | S8 | S4 | S5 |
| | F(25D) S(22E) Port 4 | S6 | S7 | S8 | S9 | S10 |
| | Bit weight | 64K | 32K | 16K | 8K | 4K |

**Priority Int. Group Addresses**

| Prior. Int. Chas. LT26 30J | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| For Group | S1-1 | S2-1 | S3-1 | S4-1 | Group | S1-1 | S2-1 | S3-1 | S4-1 |
| 2 | 0 | 0 | 1 | 0 | 9 | 1 | 0 | 0 | 1 |
| 3 | 0 | 0 | 1 | 1 | A | 1 | 0 | 1 | 0 |
| 4 | 0 | 1 | 0 | 0 | B | 1 | 0 | 1 | 1 |
| 5 | 0 | 1 | 0 | 1 | C | 1 | 1 | 0 | 0 |
| 6 | 0 | 1 | 1 | 0 | D | 1 | 1 | 0 | 1 |
| 7 | 0 | 1 | 1 | 1 | E | 1 | 1 | 1 | 0 |
| 8 | 1 | 0 | 0 | 0 | F | 1 | 1 | 1 | 1 |

**REU Address**

| REU Chas. LT26 32A | | | |
|---|---|---|---|
| For BLKs | S3-2 | S3-1 | S2-2 |
| 4-7 | 0 | 0 | 1 |
| 8-11 | 0 | 1 | 0 |
| 12-15 | 0 | 1 | 1 |
| 16-19 | 1 | 0 | 0 |
| 20-23 | 1 | 0 | 1 |
| 24-27 | 1 | 1 | 0 |
| 28-31 | 1 | 1 | 1 |



**SIOP**

| SIOP Chas. LT26 8F | |
|---|---|
| Switch | Function |
| S1-1 | IOP address bit 0 |
| S1-2 | Set if high priority bus shar. IOP |
| S2-1 | IOP address bit 1 |
| S2-2 | Set if bus shar. opt |
| S3-1 | IOP address bit 2 |
| S4-1 | Set if last IOP |

**MIOP**

| MIOP Chas. LT26 13C | |
|---|---|
| Switch | Function |
| S1-1 | IOP address bit 0 |
| S1-2 | Set if last IOP |
| S2-1 | IOP address bit 1 |
| S2-2 | Set if 4 byte opt(8473) |
| S3-1 | IOP address bit 2 |
| S3-2 | Set if high prior bus sharing IOP (8473) |

**Sub Controller DVC Number**

| DVC Controller Loc 24 LT16 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Addr Bit | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Switch | S4-2 | S3-2 | S2-2 | S1-2 | S4-1 | S3-1 | S2-1 | S1-1 |

**MS DIO Addr**

| MS LT26 21A | |
|---|---|
| S1-1 | A10 |
| S2-1 | A9 |
| S3-1 | A8 |
| S4-1 | A7 |
| S1-2 | A6 |
| S2-2 | A5 |
| S3-2 | A4 |
| S4-2 | A3 |
| Switches on 23A and 22A must be up | To disable MS, put switch on 23A down |

**CFE-3**

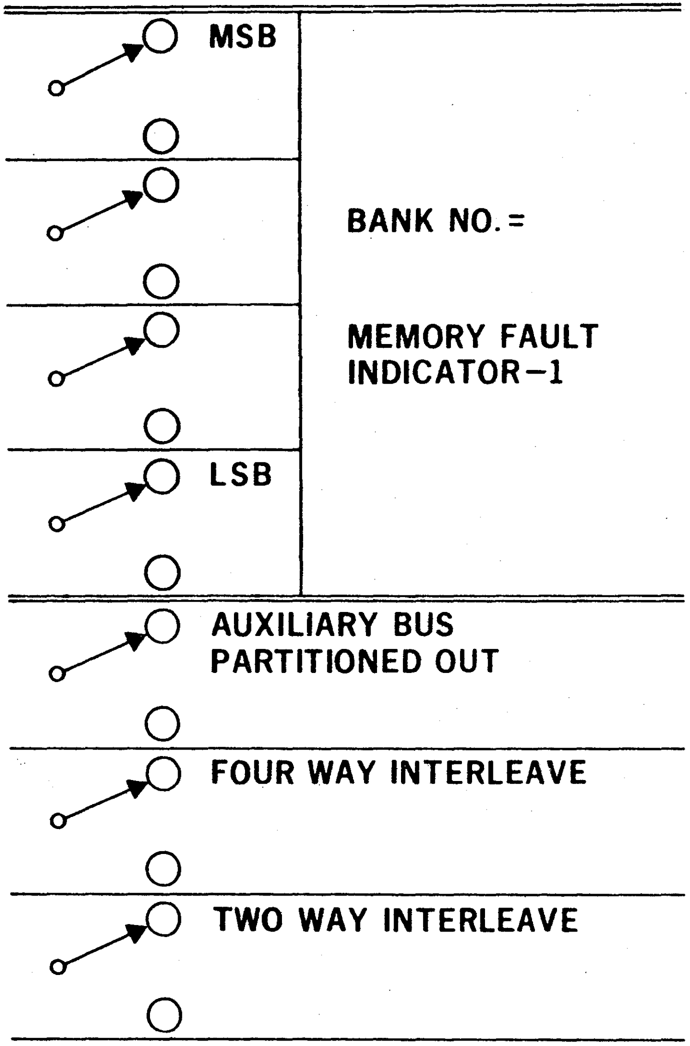
| CFE cont. chasis LT26 3A | |
|---|---|
| Switch | Function |
| S1-1, S1-2 | |
| S2-1, S2-2 | for test mode |
| S3-1 | Test mode (1) |
| S3-2 | Test mode clear |
| S4-1 | CFE controller (0 or 1) |
| S4-2 | Test selector 1→test 2 |

# MATRIX SWITCH SETTINGS

| PORT | | | 1 OR 5 | | 2 OR 6 | | 3 OR 7 | | 4 OR 8 | |
|---|---|---|---|---|---|---|---|---|---|---|
| BANK | | | A | B | A | B | A | B | A | B |
| SLOT | | | 31 | 29 | 20 | 18 | 15 | 13 | 04 | 02 |
| STARTING ADDRESS | 64K | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 32K | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 16K | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 8K | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| PARTITION PORT OUT | YES | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| CHECK INCOMING DATA PARITY | YES | ○ | ○ | X | ○ | X | ○ | X | ○ | X |
| | | ○ | ○ | | ○ | | ○ | | ○ | |
| CPU BUS<br>If this switch is in the "yes" position any port encountering a parity error will cause the PE line for this port to be raised. | YES | ○ | ○ | X | ○ | X | ○ | X | ○ | X |
| | | ○ | ○ | | ○ | | ○ | | ○ | |

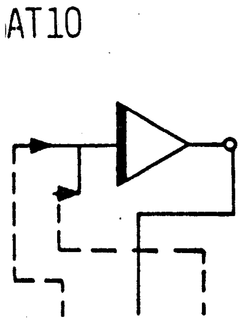
BLACKEN CIRCLES IN PENCIL TO REPRESENT NORMAL SYSTEM SETTINGS

# DRIVER SWITCH SETTINGS
## SLOT 29B

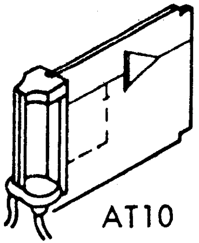

MSB
BANK NO. =
MEMORY FAULT INDICATOR–1
LSB
AUXILIARY BUS PARTITIONED OUT
FOUR WAY INTERLEAVE
TWO WAY INTERLEAVE

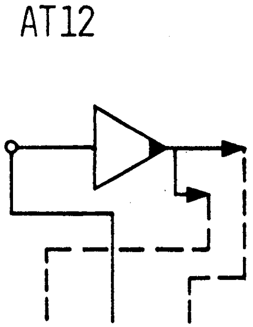
BLACKEN CIRCLES IN PENCIL TO INDICATE NORMAL SYSTEM SETTINGS

# TYPICAL RELATIONSHIPS 30 OHM CABLE CARDS

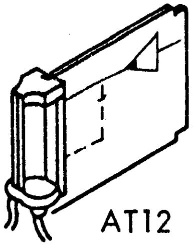


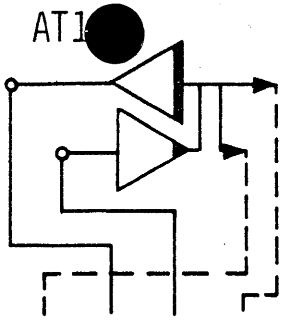
| P3 | P1 | P2 |
|---|---|---|
| A | 6 | 1 |
| B | 4 | 2 |
| C | 10 | 3 |
| D | 8 | 4 |
| E | 13 | 5 |
| F | 18 | 6 |
| G | 20 | 7 |
| H | 22 | 8 |
| K | 27 | 9 |
| L | 34 | 10 |
| M | 36 | 11 |
| N | 38 | 12 |
| P | 40 | 13 |
| R | 42 | 14 |



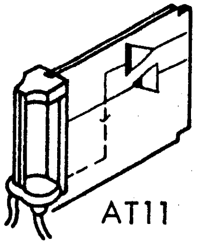


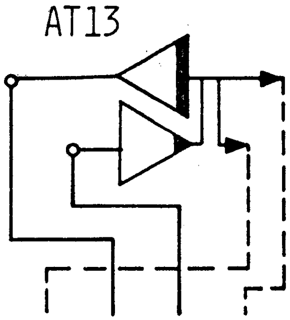
| P3 | P1 | P2 |
|---|---|---|
| A | 2 | 1 |
| B | 1 | 2 |
| C | 9 | 3 |
| D | 3 | 4 |
| E | 12 | 5 |
| F | 15 | 6 |
| G | 19 | 7 |
| H | 23 | 8 |
| K | 25 | 9 |
| L | 33 | 10 |
| M | 35 | 11 |
| N | 37 | 12 |
| P | 39 | 13 |
| R | 45 | 14 |



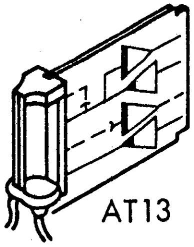


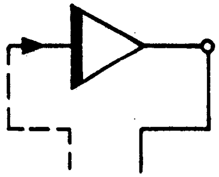
| P3 | P1 | P1 | P2 |
|---|---|---|---|
| A | 6 | 2 | 1 |
| B | 4 | 1 | 2 |
| C | 10 | 9 | 3 |
| D | 8 | 3 | 4 |
| E | 13 | 12 | 5 |
| F | 18 | 15 | 6 |
| G | 20 | 19 | 7 |
| H | 22 | 23 | 8 |
| K | 27 | 25 | 9 |
| L | 34 | 33 | 10 |
| M | 36 | 35 | 11 |
| N | 38 | 37 | 12 |
| P | 40 | 39 | 13 |
| R | 42 | 45 | 14 |





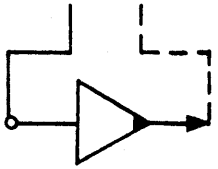
| P3 | P1 | P1 | P2 |
|---|---|---|---|
| A | 6 | 2 | 1 |
| B | 4 | 1 | 2 |
| C | 10 | 9 | 3 |
| D | 8 | 3 | 4 |
| E | 13 | 12 | 5 |
| F | 18 | 15 | 6 |
| K | 27 | 25 | 9 |
| L | 34 | 33 | 10 |
| M | 36 | 35 | 11 |
| N | 38 | 37 | 12 |
| P | 40 | 39 | 13 |
| R | 42 | 45 | 14 |

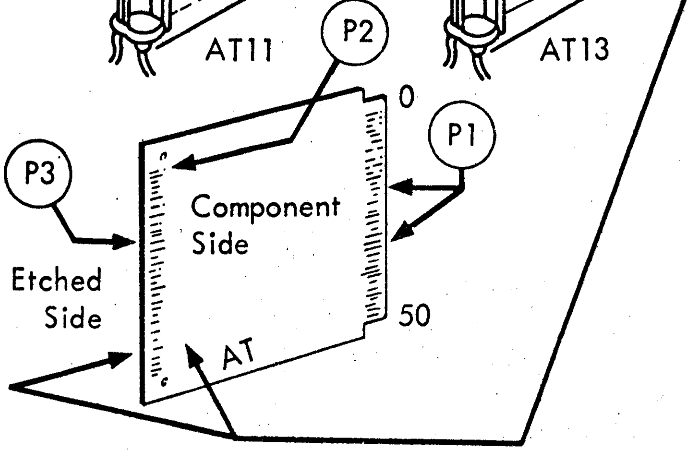




| P3 | P1 |
|---|---|
| G | 20 |
| H | 22 |

| | |
|---|---|
| 19 | 7 |
| 23 | 8 |
| P1 | P2 |




P2
0
P1
P3
Component Side
Etched Side
50
AT

| P3 (Etch) | P2 (Component) |
|---|---|
| Ground | Ground |
| A | 1 |
| Ground | Ground |
| B | 2 |
| Ground | Ground |
| . | . |
| . | . |
| . | . |
| Ground | Ground |
| P | 13 |
| Ground | Ground |
| R | 14 |
| Ground | Ground |

## SIGMA 7 PORT EXPANDER

8457 F 3 to 6 port expander 1 memory assy 130625
8457 S 3 to 6 port expander 2nd memory assy 130626
Module Location Chart - 133621
Installation Drawing Port Exp F 133762
Installation Drawing Port Exp S 133688
Switch Settings - see system switch settings

| | | |
|---|---|---|
| ST14S | 24D, 25E | F expander |
| | 21E, 22E | S expander |

Cables connecting sources to port expander are connected normal from the bottom, but are attached upside down at the port expander. Cable pin numbers will have to be transposed when using the signal map in the interface section.

Port Ex. Memory Cables, twisted pair ZT38

| | FROM | | TO | |
|---|---|---|---|---|
| Twisted Pair | XF | XS | Port A | Port B |
| Mem Cab #1 | 6C | 8C | 2A | 6A |
| #2 | 11C | 13C | 2B | 6B |
| #3 | 17C | 19C | 4A | 4B |
| #4 | 21C | 23C | 4C | 2D |
| #5 | 25C | 27C | 6C | 4D |

Additional signals provided to the port expander, via the ZT38 modules, on memory interface cables 4 and 5.

| | | | |
|---|---|---|---|
| Port XF | | 21C | 25C |
| Port XS | | 23C | 27C |
| Mem Port A | | 4C | 6C |
| Mem Port B | | 2D | 4D |
| CABLE CONDUCTOR | MOD PINS | MEMORY CABLE 4 | MEMORY CABLE 5 |
| 15 | 7(S) | NR08 | START |
| | 11(L) | | |
| 16 | 17(S) | NR16 | TW500 |
| | 14(L) | | |
| 17 | 21(S) | NR32 | TO |
| | 26(L) | | |
| 18 | 29(S) | NR64 | NPFSRD |
| | 28(L) | | |
| 19 | 31(S) | NS1 | |
| | 30(L) | | |
| 20 | 43(S) | NS0 | |
| | 44(L) | | |
| 21 | 47(S) | (12K) | |
| | 46(L) | | |

(S) Source e.g. Memory Source Signal NR08 is provided
(L) Load at pin 7 of the memory and is received at pin 11 in the Port Expander

| | | | | | |
|---|---|---|---|---|---|
| PORT 1 | 2B AT11 | 2D AT11 | 10B AT11 | 18D AT10 | 26B AT11 |
| PORT 2 | 4B AT11 | 4D AT11 | 12B AT11 | 20B AT10 | 28B AT11 |
| PORT 3 | 6B AT11 | 6D AT11 | 14B AT11 | 22B AT10 | 30B AT11 |
| PORT 4 | 8B AT11 | 8D AT11 | 16B AT11 | 24B AT10 | 32B AT11 |

CABLES CONNECTING SOURCES TO PORT EXPANDER BUS ARE CONNECTED NORMAL FROM THE BOTTOM, BUT ARE ATTACHED UPSIDE DOWN AT THE PORT EXPANDER

| CABLE PINS | BACK PANEL PINS | MEMORY CABLE #1 | MEMORY CABLE #2 | MEMORY CABLE #3 | MEMORY CABLE #4 | MEMORY CABLE #5 |
|---|---|---|---|---|---|---|
| 13,P | 39 | M00D | M14D | M28D | L15D | MQD |
| | 40 | M00R | M14R | M28R | | |
| 14,R | 45 | M01D | M15D | M29D | L16D | * |
| | 42 | M01R | M15R | M29R | | AHR |
| 11,M | 35 | M02D | M16D | M30D | L17D | * |
| | 36 | M02R | M16R | M30R | | ARR |
| 12,N | 37 | M03D | M17D | M31D | L18D | * |
| | 38 | M03R | M17R | M31R | | DRR |
| 10,6 | 33 | M04D | M18D | L29D | L19D | * |
| | 34 | M04R | M18R | | | PER |
| 9,K | 25 | M05D | M19D | L30D | L20D | * |
| | 27 | M05R | M19R | | | SRAR |
| 8,H | 23 | M06D | M20D | L31D | L21D | * |
| | 22 | M06R | M20R | | | - |
| 7,G | 19 | M07D | M21D | MW0D | L22D | AB0D |
| | 20 | M07R | M21R | | | |
| 6,F | 15 | M08D | M22D | MW1D | L23D | * |
| | 18 | M08R | M22R | | | POKR |
| 5,E | 12 | M09D | M23D | MW2D | L24D | * |
| | 13 | M09R | M23R | | | |
| 4,D | 3 | M00D | M24D | MW3D | L25D | * |
| | 8 | M10R | M24R | * | | |
| 3,C | 9 | M11D | M25D | DGR | L26D | * |
| | 10 | M11R | M25R | * | | |
| 2,B | 1 | M12D | M26D | EDRR | L27D | * |
| | 4 | M12R | M26R | | | |
| 1,A | 2 | M13D | M27D | * | L28D | * |
| | 6 | M13R | M27R | | | |

Σ7- 8457 MEMORY INTERFACE

ALL SIGNALS DESCRIBED FROM THE POINT OF VIEW OF THE MEMORY PORT EXPANDER.

## CPU EXTERNAL INTERRUPT INTERFACE

| | 8421 | 26J AT11 | 12J AT11 | 19J AT11 | 32J AT11 |
|---|---|---|---|---|---|
| | CPU | 30V AT11 | | | |
| Cable Pins | Module Pins | Ex Int/CPU | Ex Int/EQ | EX Int/EQ | Ex Int/EQ |
| 1,A | 2 | LIN01 | ECPURST2 | ECPURST1 | ECPURST |
| | 6 | DAT17 | | | |
| 2,B | 1 | LIN00 | | | |
| | 4 | DAT16 | | | |
| 3,C | 9 | LIN03 | | IS10 | IS4 |
| | 10 | DAT19 | | | |
| 4,D | 3 | LIN02 | | IS11 | IS5 |
| | 8 | DAT18 | | | |
| 5,E | 12 | LIN04 | IS15 | IS9 | IS3 |
| | 13 | DAT20 | | | |
| 6,F | 15 | LIN05 | IS14 | IS8 | IS2 |
| | 18 | DAT21 | | | |
| 7,G | 19 | LIN06 | IS13 | IS7 | IS1 |
| | 20 | DAT22 | | | |
| 8,H | 23 | LIN07 | IS12 | IS6 | IS0 |
| | 22 | DAT23 | | | |
| 9,K | 25 | LIN08 | | | |
| | 27 | DAT24 | | ERQ11 | ERQ05 |
| 10,L | 33 | LINREQ | | | |
| | 34 | DAT25 | | ERQ10 | ERQ04 |
| 11,M | 35 | | | | |
| | 36 | DAT26 | ERQ15 | ERQ9 | ERQ03 |
| 12,N | 37 | | | | |
| | 38 | DAT27 | ERQ14 | ERQ8 | ERQ02 |
| 13,P | 39 | | | | |
| | 40 | DAT28 | ERQ13 | ERQ7 | ERQ01 |
| 14,R | 45 | | | | |
| | 42 | DAT29 | ERQ12 | ERQ6 | ERQ00 |

Interface Viewed At------External Interrupt Chassis------

## REU-CPU INTERFACE

| | CPU | 5T AT11 | 19T AT11 | 5L AT11 | 5Q AT11 | 28U ZT23 | |
|---|---|---|---|---|---|---|---|
| | REU | 27A AT11 | 15A AT11 | 25A AT11 | 6A AT11 | 30A ZT23 | |
| Cable Pins | Module Pins | Read/Write Byte 0 | Read/Write Byte 1 | Read/Write Byte 2 Address | Read/Write Byte 3 Address | Clock CPU | 1st REU |
| 1,A | 2<br>6 | | | NLR28-2 | RP24 | CREU1 | CRX2 |
| 2,B | 1<br>4 | | | LR28-2 | RP23 | CREU2 | CRX2 |
| 3,C | 9<br>10 | | | LR30-2 | RP26 | CREU3 | CRX3 |
| 4,D | 3<br>8 | | | LR29-2 | RP25 | CREU4 | CRX4 |
| 5,E | 12<br>13 | | | LR31-2 | RP27 | CREU5 | CRX5 |
| 6,F | 15<br>18 | RWB0 | RWB1 | RWB2 | RWB3 | CREU6 | CRX6 |
| 7,G | 19<br>20 | RR0<br>S0RRWXS/0 | RR8<br>S8RRWXS/1 | RR16<br>S16RRWXS/2 | RR24<br>S24RRWXS/3 | CREU7 | CRX7 |
| 8,H | 23<br>22 | RR1<br>S1RRWXS/0 | RR9<br>S9RRWXS/1 | RR17<br>S17RRWXS/2 | RR25<br>S25RRWXS/3 | | |
| 9,K | 25<br>27 | RR2<br>S2RRWXS/0 | RR10<br>S10RRWXS/1 | RR18<br>S18RRWXS/2 | RR26<br>S16RRWXS/3 | | |
| 10,L | 33<br>34 | RR3<br>S3RRWXS/0 | RR11<br>S11RRWXS/1 | RR19<br>S19RRWXS/2 | RR27<br>S2RRWXS/3 | | |
| 11,M | 35<br>36 | RR4<br>S4RRWXS/0 | RR12<br>S12RRWXS/1 | RR20<br>S20RRWXS/2 | RR28<br>S28RRWXS/3 | | |
| 12,N | 37<br>38 | RR5<br>S5RRWXS/0 | RR13<br>S13RRWXS/1 | RR21<br>S21RRWXS/2 | RR29<br>S29RRWXS/3 | | |
| 13,P | 39<br>40 | RR6<br>S6RRWXS/0 | RR14<br>S14RRWXS/1 | RR22<br>S22RRWXS/2 | RR30<br>S30RRWXS/3 | | |
| 14,R | 45<br>42 | RR7<br>S7RRWXS/0 | RR15<br>S15RRWXS/1 | RR23<br>S23RRWXS/2 | RR31<br>S31RRWXS/3 | | |

Signal presence governed by the installation of the wire changes below.

Signals represented from the point of view of the REU.

| ZT23 Cable Pins | = Module Pins |
|---|---|
| 1 | 4 |
| A | 1 |
| 2 | 6 |
| B | 3 |
| 3 | 8 |
| C | 7 |
| 4 | 12 |
| D | 10 |
| 5 | 17 |
| E | 14 |
| 6 | 19 |
| F | 18 |
| 7 | 21 |
| G | 22 |
| 8 | 24 |
| H | 26 |
| 9 | 28 |
| K | 30 |
| 10 | 33 |
| L | 34 |
| 11 | 36 |
| M | 38 |
| 12 | 40 |
| N | 42 |
| 13 | 43 |
| P | 45 |
| 14 | 47 |
| R | 50 |

Clocking-Clock Cable from the CPU Plugs into Position 30A of REU No. 1. Coaxial (Part No. 128147-372) and Additional CPU Wiring for REU's are as follows.

| For REU | Add Wire Sigma 7, CPU | FROM Coax | | FROM Shield | TO Coax | | TO Shield |
|---|---|---|---|---|---|---|---|
| #1 | | 30A04 | REU#1 | 30A02 | 12A13 | REU#1 | 12A16 |
| 2 | 28U03-29U17 | 30A06 | REU#1 | 30A05 | 12A13 | REU#2 | 12A16 |
| 3 | 28U07-29U19 | 30A08 | REU#1 | 30A09 | 12A13 | REU#3 | 12A16 |
| 4 | 28U10-29U21 | 30A12 | REU#1 | 30A13 | 12A13 | REU#4 | 12A16 |
| 5 | 28U14-29U23 | 30A17 | REU#1 | 30A16 | 12A13 | REU#5 | 12A16 |
| 6 | 28U18-29U25 | 30A19 | REU#1 | 30A21 | 12A13 | REU#6 | 12A16 |
| 7 | 28U22-29U27 | 30A21 | REU#1 | 30A23 | 12A13 | REU#7 | 12A16 |

## CPU-DEC, CPU-PWR MON-MEM, CPU-IOP INTERFACES

| | | | | |
|---|---|---|---|---|
| | SIOP | | | 10F AT13 |
| | MIOP | | | 12C AT13 |
| | MEM | | 2C AT11 | |
| | DEC | 32C AT11 | | |
| | CPU | 18D AT11 | 30Q AT11 | 29L AT11 |
| | PWR MON | | J5 AT13 | |
| Cable Pins | Module Pins | DEC | PWR MON | IOP |
| 1,A | 2 | DU0 | (MFL1) | |
| | 6 | DU0 | | FNC0 |
| 2,B | 1 | DU1 | (MFL0) | |
| | 4 | DU1 | | FNC1 |
| 3,C | 9 | DU2 | (MFL3) | |
| | 10 | DU2 | | FNC2 |
| 4,D | 3 | DU3 | | |
| | 8 | DU3 | (ST) | IOPA0 |
| 5,E | 12 | DU4 | (MFL4) | |
| | 13 | DU4 | | IOPA1 |
| 6,F | 15 | DU5 | (MFL5) | |
| | 18 | DU5 | | IOPA2 |
| 7,G | 19 | DU6 | | |
| | 20 | DU6 | (RTC) | CNST |
| 8,H | 23 | DU7 | | |
| | 22 | DU7 | (IOEN) | |
| 9,K | 25 | | | NCC1 |
| | 27 | DUCLOCK | (ION) | |
| 10,L | 33 | | | NCC2 |
| | 34 | DUSTART | (IOFF) | |
| 11,M | 35 | DUEND | (MFL2) | |
| | 36 | | | 1MC |
| 12,N | 37 | | | |
| | 38 | DUCLEAR | | RIO |
| 13,P | 39 | DU12 | (MFL6) | IR |
| | 40 | DUMDM | | |
| 14,R | 45 | DU13 | (MFL7) | PR |
| | 42 | | | |
| Interface Viewed At | | DEC | MEMORY | IOP |

## SIGMA 8/9 MIOP Single Phase Operation Program

This program will single phase the MIOP thru a complete SIO/IOCD sequence. After each phase step the program will come to a WAIT (location 117). At that time R1 will equal the number of step operations completed and R5 thru RF will contain status information for that phase (the attached sheets provide expected data for each operation). Modifications are provided to allow the program to be addressed to the TTY and/or to do single operation (each step will advance the MIOP thru a SIO, or 00, or DI or 0I operation).

```
 26     68000100    B           X'100'
TRAP ROUTINE
 46     0F000080    XPSD,0      X'80'
 80     00000000    DATA        X'00000000'
 81     00000000    DATA        X'00000000'
 82     00000084    DATA        X'00000084'
 83     00000000    DATA        X'00000000'
 84     0E100086    LPSD,1      X'86'           Clear PDF
 85     00000000
 86     0000010C    DATA        X'0000010C'
 87     00000000    DATA        X'00000000'
PROGRAM
 100    22100001    LI,1        X'01'           Initialize counter
 101    4F004000    RIO,0       X'000'          Reset MIOP
*102    22480000    LI,4        X'80000'        Put the M.S.Online and the
 103    6D40200F    WD,4        X'200F'         Controllers Offline.
 104    22403000    LI,4        X'3000'         Wait for the AT83's to go Offline.
 105    64400105    BDR,4       X'105'
 106    224700FF    LI,4        X'700FF'        Set M.S. Address = 07 and
 107    6D40200D    WD,4        X'200D'         Data byte = FF.
#108    22401800    LI,4        X'1800'         Put the MIOP (CH A) in Single
 109    6D402008    WD,4        X'2008'         Phase Mode.
 10A    22000090    LI,0        X'90' (120)
*10B    4C200007    SIO,2       X'007'          Start Operation
 10C    6C502000    RD,5        X'2000'    }
 10D    6C602001    RD,6        X'2001'    }    Read CCU Groups
 10E    6C702002    RD,7        X'2002'    }
 10F    6C802008    RD,8        X'2008'    }
 110    6C902009    RD,9        X'2009'    }    Read CH A Groups
 111    6CA0200A    RD,A        X'200A'    }
 112    6CB0200B    RD,B        X'200B'    }
 113    6CC0200C    RD,C        X'200C'    }
 114    6CD0200D    RD,D        X'200D'    }    Read M.S. Groups
 115    6CE0200E    RD,E        X'200E'    }
 116    6DF0200F    RD,F        X'200F'    }
 117    2E000000    WAIT
 118    20100001    SI,1        X'01'           Update counter
 119    6D402008    WD,4        X'2008'         Step MIOP
 11A    22503000    LI,5        X'3000'         Wait for MIOP to do Step
 11B    6450011B    BDR,5       X'11B'
 11C    6800010C    B           X'10C'          Collect new Status

I/O COMMAND DOUBLEWORD                      122
 120    06000488    DATA        X'06000488'     IOCD to READ one Byte into
 121    00000001    DATA        X'00000001'     location 122
 122    XX                                      Data input location
```

---

```
*Changes to use TTY
  102   68000108    B           X'108'          Bypass M.S. setup
  10B   4C200001    SIO,2       X'001'          Address TTY

#Changes to do single Operation stepping
  108   22403000    LI,4        X'3000'         Put MIOP in Single Operation
```

## SIGMA 8/9 MIOP Single Step Operation

M.S. Address = 07

| Single Phase<br>(R1) | Group 0 | Group 8 | Group 9 | Group C | Group E | Group F | Single Operation<br>(R1) |
|---|---|---|---|---|---|---|---|
| | SIO INSTRUCTION | | | | | | |
| 1 | | 40040000 | 003D2X00 | 00000000 | 00008400 | 00004800 | |
| 2 | 00000020 | 00240180 | 00212000 | 0000C007 | 00008400 | 00000C80 | |
| 3 | 07800020 | 00150180 | 22212600 | 00000007 | 00002400 | 00000C81 | |
| 4 | 07C00021 | 000C8190 | 04212400 | 00000007 | 00008408 | 00002C80 | |
| 5 | 07C00021 | 80000010 | 04352000 | 00000000 | 00008408 | 00002400 | ← 1 |
| | ORDER OUT | | | | | | |
| 6 | 07C00021 | 40000C30 | 263D2200 | 00000000 | 00001408 | 00002405 | |
| 7 | 07C00021 | 20018000 | 8CB12800 | 00000000 | 00001508 | 00008400 | |
| 8 | 07C00021 | 08008000 | 88B1EC00 | 00000000 | 00001508 | 00008400 | |
| 9 | 00000121 | 040083C0 | 88B1E800 | 00000000 | 00001508 | 00008400 | |
| A | 00000121 | 0201C240 | 88B1E800 | 00000006 | 00000D08 | 00008C00 | |
| B | 00000121 | 01004000 | 88B1C800 | 00000006 | 00000D08 | 00008E00 | |
| C | 00000121 | 80004000 | 84F5C800 | 00000000 | 00008438 | 0000EE00 | ← 2 |
| | DATA IN | | | | | | |
| D | 00000121 | 40004020 | A6FDCA00 | 00000000 | 00001438 | 0000EE05 | |
| E | 00000121 | 20018000 | 0C310800 | 0000FFFF | 00001538 | 00000600 | |
| F* | 04400122 | 01004180 | 88B10C80 | 000000FF | 00000D38 | 00008600 | |
| 10 | 04400122 | 80004000 | 84F50480 | 00000040 | 00008498 | 0000EE00 | ← 3 |
| | ORDER IN | | | | | | |
| 11 | 04400122 | 40004020 | A6FD0C80 | 00000040 | 00001498 | 0000EE05 | |
| 12 | 04400122 | 20018000 | 8CB10C00 | 0000FFFF | 00001598 | 00008600 | |
| 13 | 04400122 | 01004000 | 88B1AC00 | 000000FF | 00000D98 | 00008600 | |
| 14 | 04400122 | 80004000 | 80F5AC00 | 00000000 | 00008480 | 0000CC00 | ← 4 |
| (R1) | Group 0 | Group 8 | Group 9 | Group C | Group E | Group F | (R1) |

*Location 122 now has data byte of FF