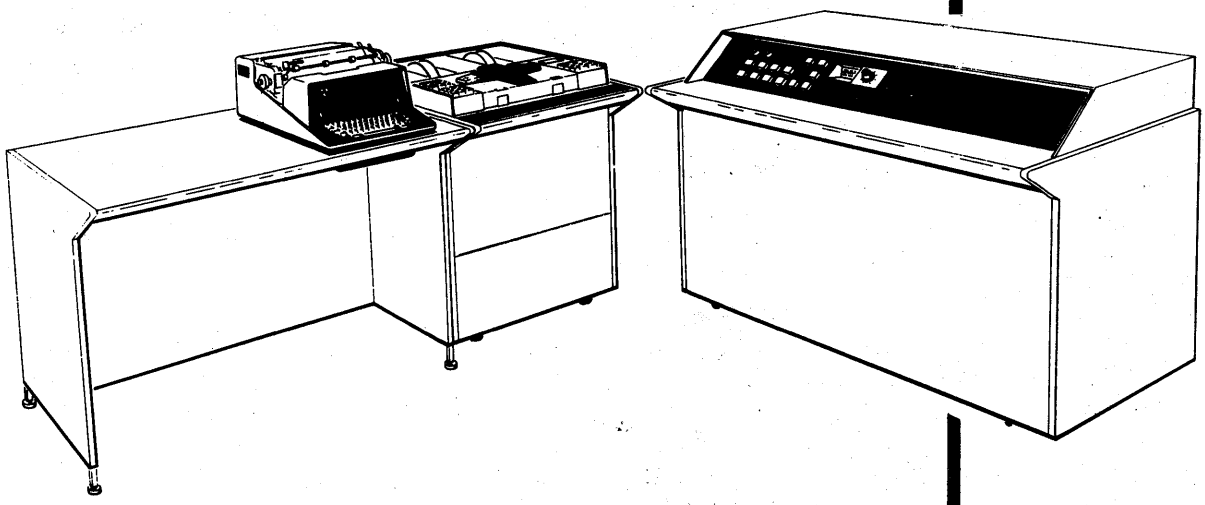
RPC 4000 ELECTRONIC COMPUTER SYSTEM

MAINTENANCE AND TRAINING MANUAL



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PREFACE

This manual contains all the necessary information for the maintenance of the RPC-4000 Computer System. The manual is divided into the following parts, each preceded by its own Table of Contents:

SECTION 1:	INTRODUCTION
SECTION 2:	INSTALLATION
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SECTION 1

INTRODUCTION

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SECTION 1

INTRODUCTION

1.1 Purpose of Manuscript--This manuscript is issued as the basic source of technical information on the RPC-4000 Electronic Computer System. Descriptive data, explanations of the theory of operation, and operating and maintenance instructions are provided herein for the two units of the basic RPC-4000 system (the RPC-4010 Computer and the RPC-4500 Tape-Typewriter System).

1.2 Purpose of Equipment--The RPC-4000 is a general purpose, solid-state, internally programmed, electronic computer system. It provides operating speeds, memory capacity, and operating features normally associated with larger computer systems. The RPC-4000 system is designed to meet the computing needs of scientific, engineering, and business data processing functions.

1.3 Description of System--The RPC-4000 system may be assembled from a variety of available peripheral equipment in addition to the RPC-4010 Computer and RPC-4500 Tape-Typewriter System covered in this manual. A complete manual is furnished for each of the devices available for use with the basic RPC-4000 system (table 1-1).

TABLE 1-1

LIST OF AUXILIARY EQUIPMENT

MODEL NO.	DESCRIPTION	CHARACTERISTICS
RPC-4410	Photo-Electric Tape Reader	Reads 500 characters per second
RPC-4431	Auxiliary Reader/Punch	Reads 60 characters per second Punches 30 characters per second
RPC-4440	High Speed Punch	Punches 300 characters per second
RPC-4430	Auxiliary Typewriter	Types 10 characters per second
RPC-4600	Auxiliary Tape-Typewriter	Identical to the RPC-4500 but does not contain master input/output control

RPC 443: Reads 120 CP Punches 60 CP

1.4 RPC-4010 Computer--The heart of the RPC-4000 system is the RPC-4010 Computer (figure 1-1), which contains arithmetic and control registers and internal memory for the system. Operation of the computer is under control of an internally stored program. The operator is provided with means to select any one of a wide variety of operational modes, ascertain internal states of operation by means of a visual display and he may interrupt, intervene, or alter the system program through an array of indicators and manually operated switches located on the control panels.

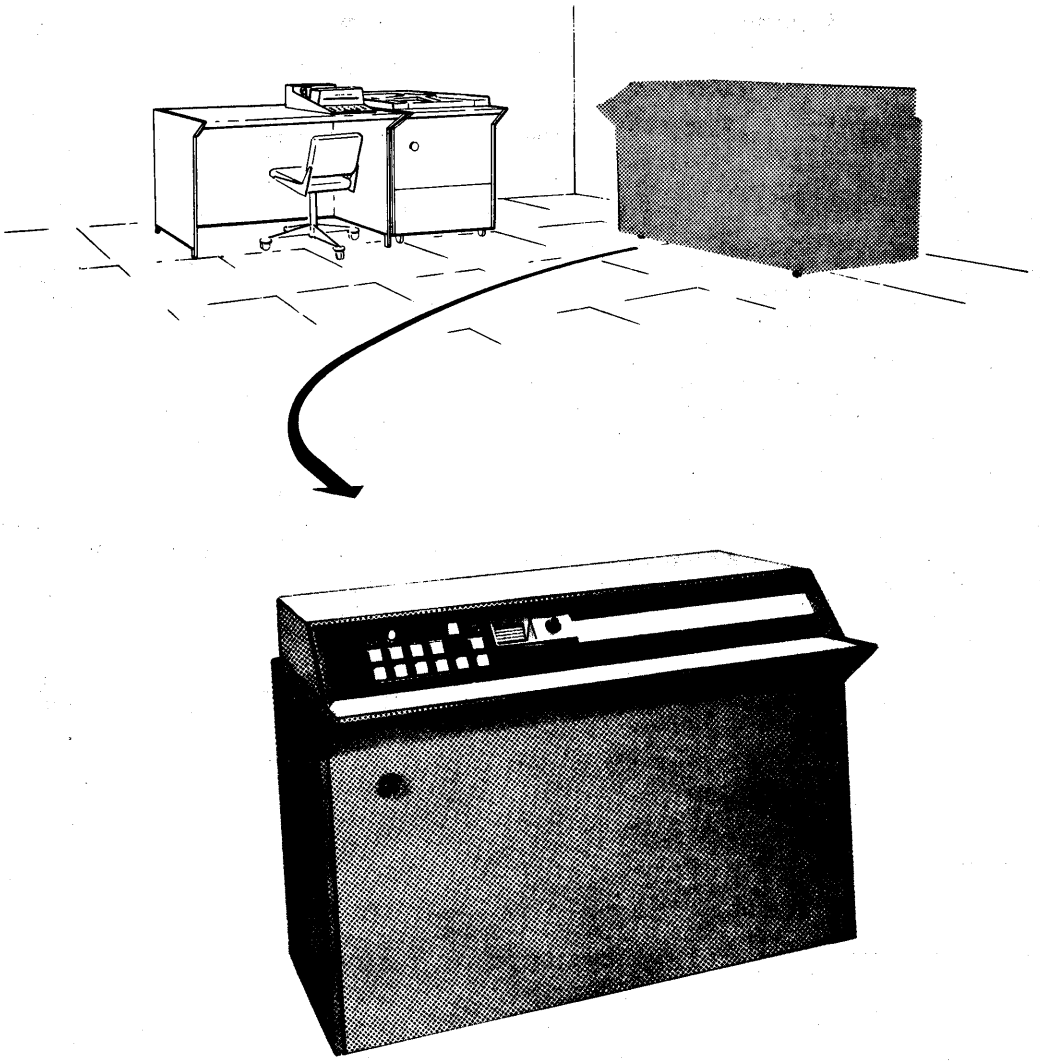

FIGURE 1-1 RPC 4010 COMPUTER

The RPC-4010 Computer is a two address, serial, binary, digital, calculating device with a magnetic drum memory of approximately 8,000 words capacity. Minimum command execution time is four word periods, or about one millisecond.

1.4.1 Word Structure

The basic unit of information is a word containing 32 bits, which may represent either a data word or an instruction word. When used as a data word, the most significant bit position indicates the algebraic sign. The remaining 31 bits represent up to nine significant decimal digits in fractional binary representation.

Instruction words hold the command identification in the 5 most significant bit positions, followed by two 13 bit addresses. The last address is that of the next instruction to be searched for and executed. Each address identifies the track number (first seven bits) and sector number (next six bits) which locate the operand or instruction in main memory.

The least significant bit position of each instruction word controls the addition of the index register content to the operand address of the instruction

as it is used from memory. A zero in the least significant bit position leaves the instruction unchanged. A one in the least significant bit position will augment the operand address by the number in the operand address portion of the index register.

Normal numbers are represented in fractional binary notation as a sign and 31 bits. Negative numbers, with a "1" in the sign bit, are held as two's complements. Multiplication produces a double length product with no sign bit in the lower half. The lower half has only 31 bits, so the LSB is zero. A double length number, such as produced by multiplication, is used as the numerator for double length division. Also, shifting preserves the format of the upper and lower halves of double length numbers (figure 1-2).

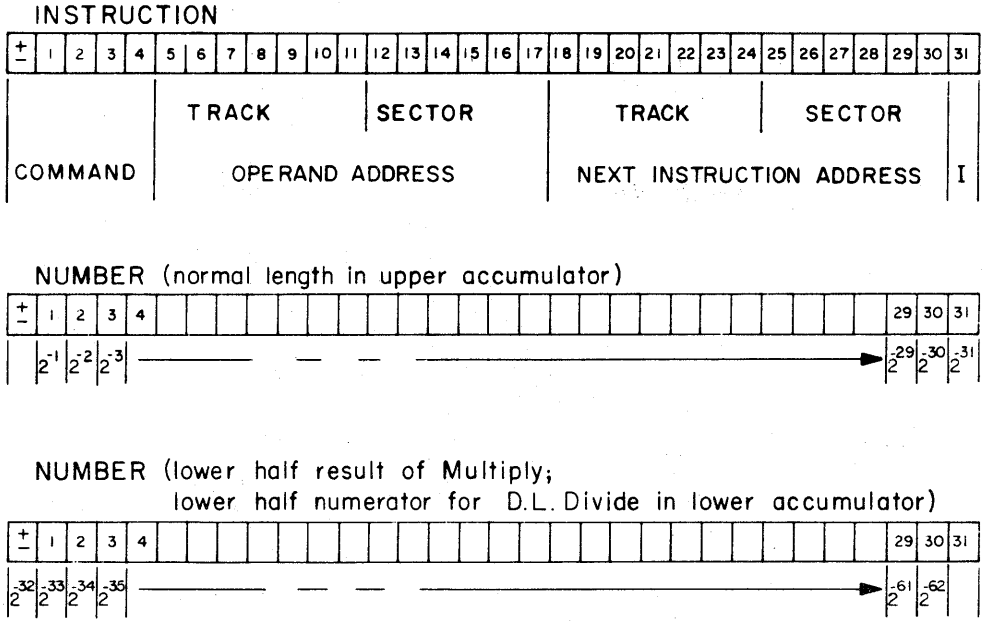

FIGURE 1-2 WORD STRUCTURE

1.4.2 Registers

There are four 1-word registers in the RPC-4010, each with a capacity of one 32 bit word. Two of the registers are used as operating accumulators. They are the upper and lower accumulators, designated U and L, respectively. The third register is the command register, C, which holds instruction words. The fourth register is the index register, X, which is used to modify operand addresses, to hold the repeat count for a repeat command, and to hold the location of the operand when a successful comparison has been made.

By application of appropriate exchange commands, the lower accumulator may be operated in lengthened mode. That is, L is an eight word length register rather than the normal one word length. In lengthened mode, the eight words in L have primitive sector numbers 0 through 7, corresponding to the main memory sector numbers reduced modulo 8. Any addressed instruction operating on L, then operates on the word or words with appropriate primitive sector numbers. When L is put in the one word length mode, that word of lengthened L whose primitive sector number is the same as the primitive sector number of the exchange command operand address will be retained in L.

1.4.3 Memory

The magnetic drum main memory contains 128 tracks, numbered 0 through 127. Each track contains 64 words, which are identified by sector numbers 0 through 63 (figure 1-3). To decrease access time, two of the tracks are designated dual access tracks, and one as a fast access track. In the dual access tracks, two track numbers refer to the same track, but at different times. This permits each word in such a track to be accessible twice during each drum revolution. The fast access track is an 8 word circulating line with a main memory track address, in which each of the 8 words is accessible 8 times per drum revolution. The use of the above features decreases the total memory capacity below the potential 8,192 words, but increases the speed of running optimized programs (figure 1-4).

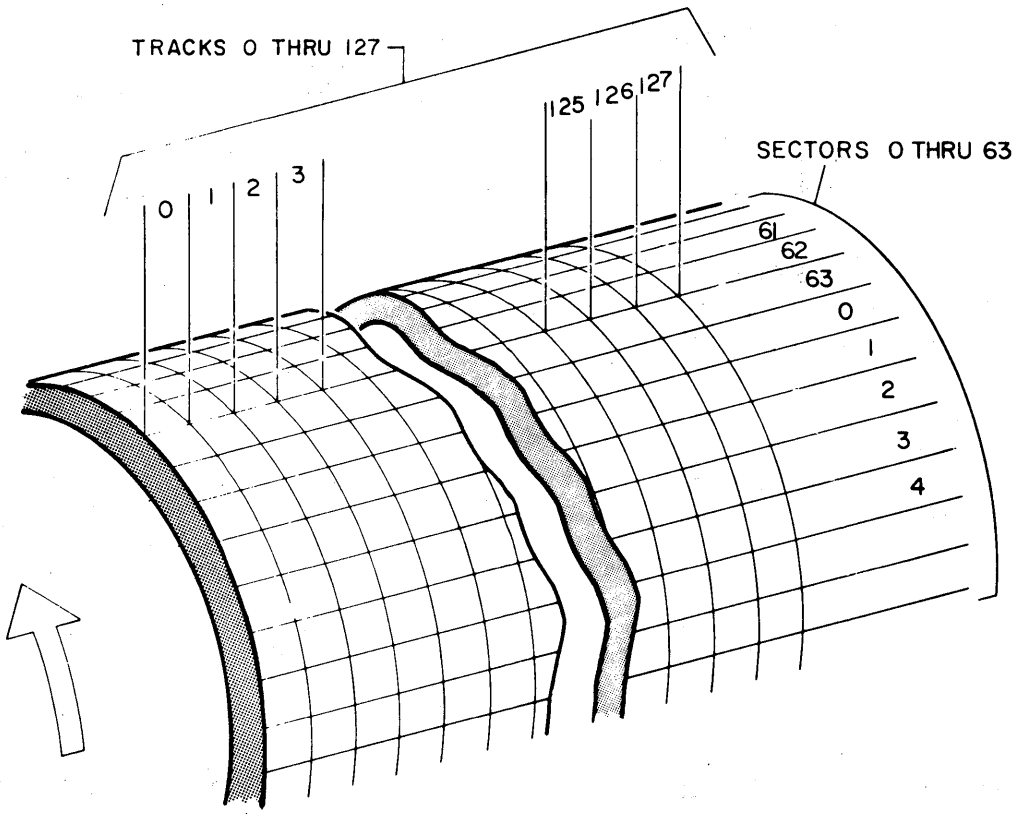

FIGURE 1-3 MEMORY DRUM

1.4.4 Phasing

Operation of the RPC-4010 Computer takes place in four phases. These are:

Phase 1 Search for Next Instruction

Phase 2 Read Instruction into Command Register

Phase 3 Search for Operand

Phase 4 Execute Command

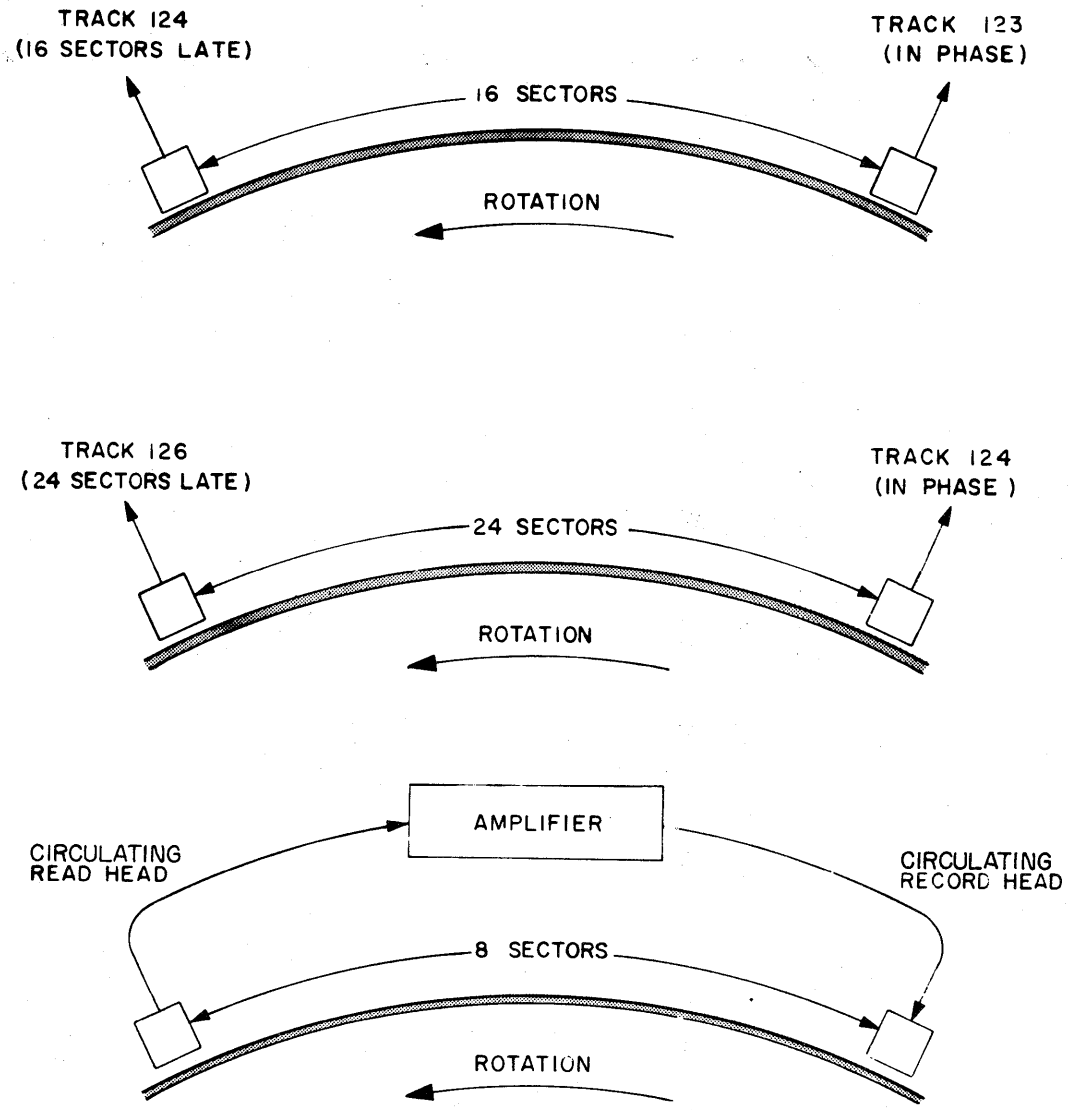

FIGURE 1-4 FAST ACCESS AND DOUBLE ACCESS TRACKS

The search phases (1 and 3) may take from 1 to 64 word times, determined by the relative sector addresses of the instruction and operand word locations. Phase 2 is executed in 1 word time, and for most commands phase 4 is also 1 word time in length. For SHIFT, SHIFT LEFT AND COUNT, MULTIPLY, and DIVIDE commands, phase 4 has a primary execution of 1 word time and a secondary execution, designated phase 4a, of up to 66 word times.

The repeat mode is applicable to all commands except SHIFT, SHIFT LEFT AND COUNT, MULTIPLY, DIVIDE and REPEAT. The effect of repeat mode is to repeat the execution (phase 4) of a command up to 128 times. Repeat mode is applied to a command by preceding the command with a REPEAT command, which loads the repeat count (the number of times the instruction is to be repeated) into the next instruction track of the index register. An instruction to which repeat mode is applied begins execution at its operand address and continues for the designated number of sectors within the addressed track. That is, no change of track number occurs, but sectors are considered in turn, regardless of the starting point.

The duration of the secondary part of phase 4 for the SHIFT LEFT AND COUNT and SHIFT commands depends on the number of places shifted. If the primary part of phase 4 is one word period, the total SHIFT or SHIFT LEFT AND COUNT time is 4 word periods plus 1 word period for each bit shifted. The total phase 4 time for MULTIPLY or DIVIDE is 67 word periods.

There are some exceptions to the normal phase sequence. A successful TRANSFER ON MINUS or TRANSFER ON BRANCH CONTROL command uses what is normally the operand address to locate the next instruction. In this case, phases 4 and 1 are skipped, and phase 3 (during which the address is searched for) advances directly to phase 2. Consequently, these commands may take as little as 2 word periods. Unsuccessful executions of these commands take 1 word period in phases 3 and 4, and a normal phase 1 is entered.

The computer will stop in blocked state, phase 3, in response to a STOP command, or when in one operation mode. A start signal from the START COMPUTE switch will unblock the search for operand in phase 3, and allow the computer to proceed. In one operation mode, blocked state is entered every time a command is read into the command register.

1.5 RPC-4500 Tape-Typewriter--The basic input/output unit of the RPC-4000 system is the RPC-4500 Tape-Typewriter System, which is composed of an RPC-4430 Paper Tape Reader/Punch (figure 1-5) and a separately packaged RPC-4480 Typewriter

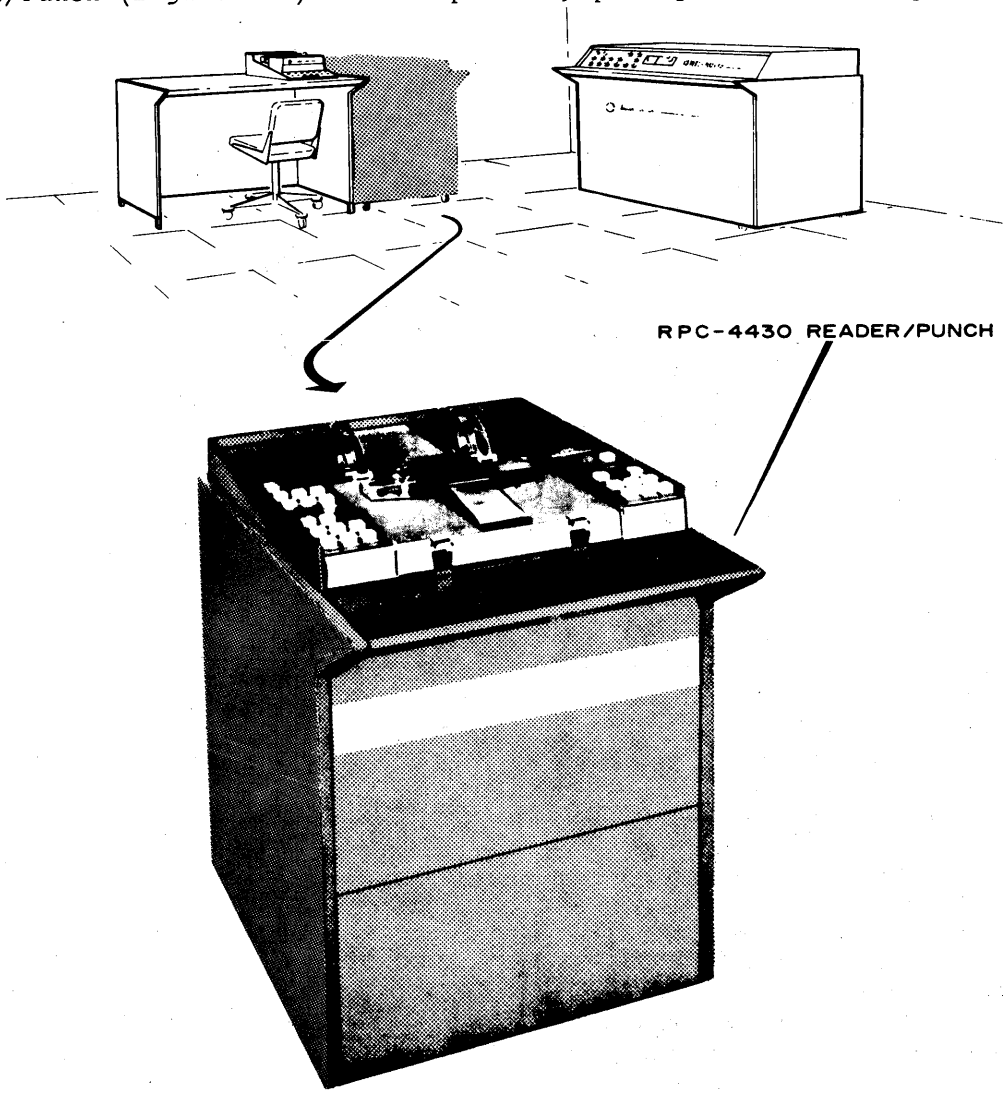

FIGURE 1-5 RPC 4430 READER/PUNCH

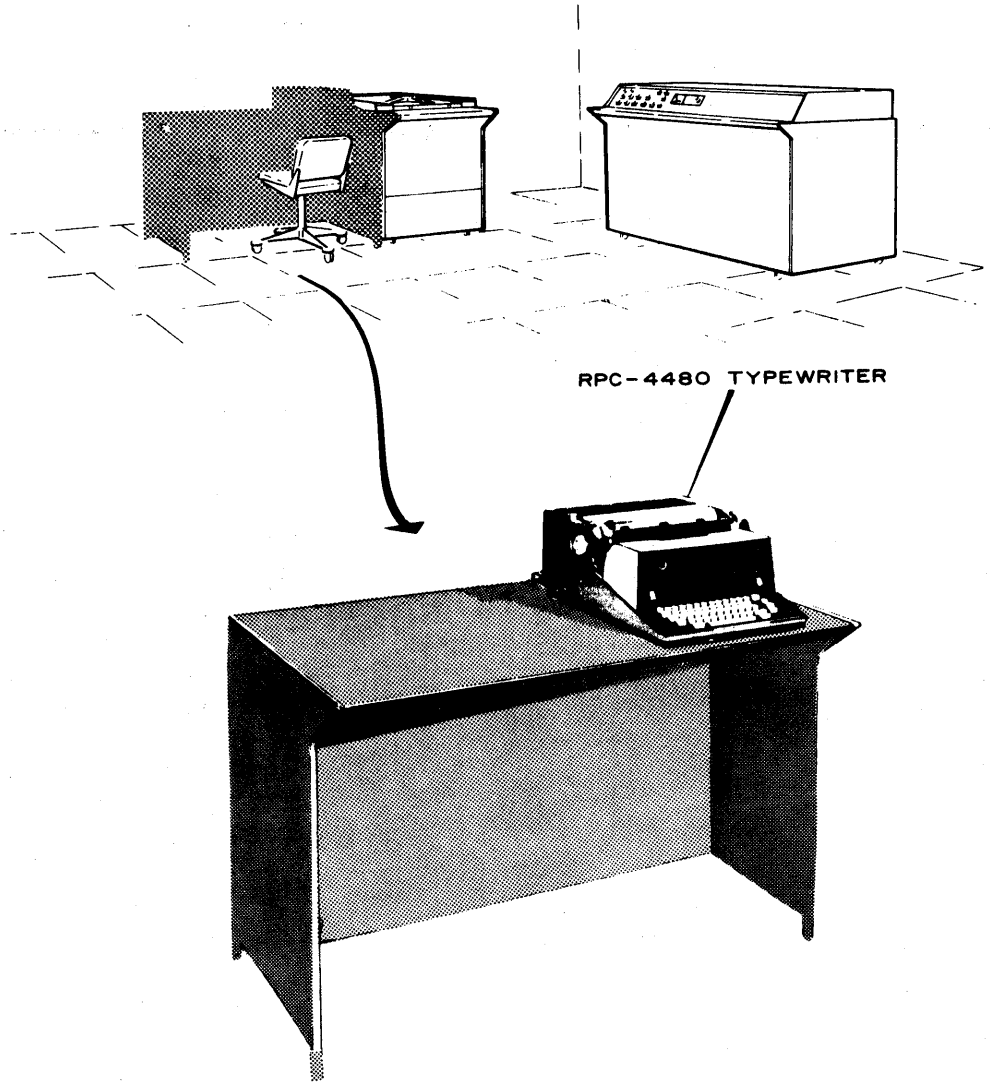

FIGURE 1-6 RPC 4480 TYPEWRITER

(figure 1-6). These two units are interconnected to form a multiple-function system, capable of a wide variety of operations, both on-line and off-line.

1.5.1 RPC-4430 Reader/Punch

The RPC-4430 Reader/Punch provides communication into and out of the computer by means of punched paper tape. The reader portion is capable of operating at a speed of 60 characters per second; the punch section operates at a speed of 30 characters per second. All data moving into or out of the computer from any input or output device passes through the system control section of the RPC-4430 Reader/Punch, where parity checking is accomplished.

1.5.2 RPC-4480 Typewriter

The RPC-4480 Typewriter is designed specifically for the RPC-4000 system. The typing speed is 10 characters per second under automatic control. The RPC-4430 and RPC-4480 are so interlocked, that any combination of devices may be used to produce both paper tapes and hard copy proofs. The effective speed of any combination is that of the slowest unit. Keyboard operation of the typewriter is identical to that of conventional machines except for the addition of a SPECIAL key, which allows the operator to backspace both the paper tape in the punch and the typewriter carriage.

SECTION 2

INSTALLATION

ILLUSTRATIONS

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SECTION 2

INSTALLATION

2.1 Unpacking and Inspection--All RPC-4000 system installations will normally be handled by Control Data service personnel. However, the equipment has been designed so that installation in any office or engineering lab is possible with little, or no, site preparation. Therefore installation may be accomplished by the purchaser (table 2-1).

TABLE 2-1

RPC-4000 SYSTEM

COMPONENT DIMENSIONS

DESIGNATION	DESCRIPTION	W	D	H	WEIGHT
RPC-4010	Computer	46 3/4"	27"	34 3/4"	498 lbs.
RPC-4430	Reader/ Punch	23 3/8"	27 5/8"	32 1/4"	246 lbs.
RPC-4480	Typewriter and Table	46 3/4"	27 3/4"	29 1/2"	244 lbs.

Each unit is carefully packaged and completely assembled, except for the RPC-4480, which is packaged as two separate units--the typewriter and the desk. Interconnecting cables are provided for completing all necessary circuits (figure 2-1).

2.2 Site Preparation--The compact, solid-state design of the system eliminates most site preparation problems. The displacement factor of all units is less than 60 pounds per square foot. Standard 110-120 volt AC outlets provide the necessary power to operate the system. Special air conditioning is not necessary, due to the low heat dissipation of the equipment.

2.3 Equipment Set-Up--Components of the RPC-4000 system may be arranged in any convenient order as long as the interconnecting cables are plugged in as illustrated (figure 2-1). The memory drum must be prepared by removing the shipping screw which bears against the end of the motor shaft. The shipping screw must be replaced with a cap screw (figure 2-2).

CAUTION

Prior to initial starting, check the freeness of the unit by rotating the drum manually (see Section 5.4.1, Head Adjustment and Replacement Procedure, Step 4).

Every typebar of the typewriter must be manually lifted to the platen before the application of power, to prevent damage to the typebars.

2.4 Checkout--Initial checkout shall be performed by Control Data service personnel upon completion of each system installation.

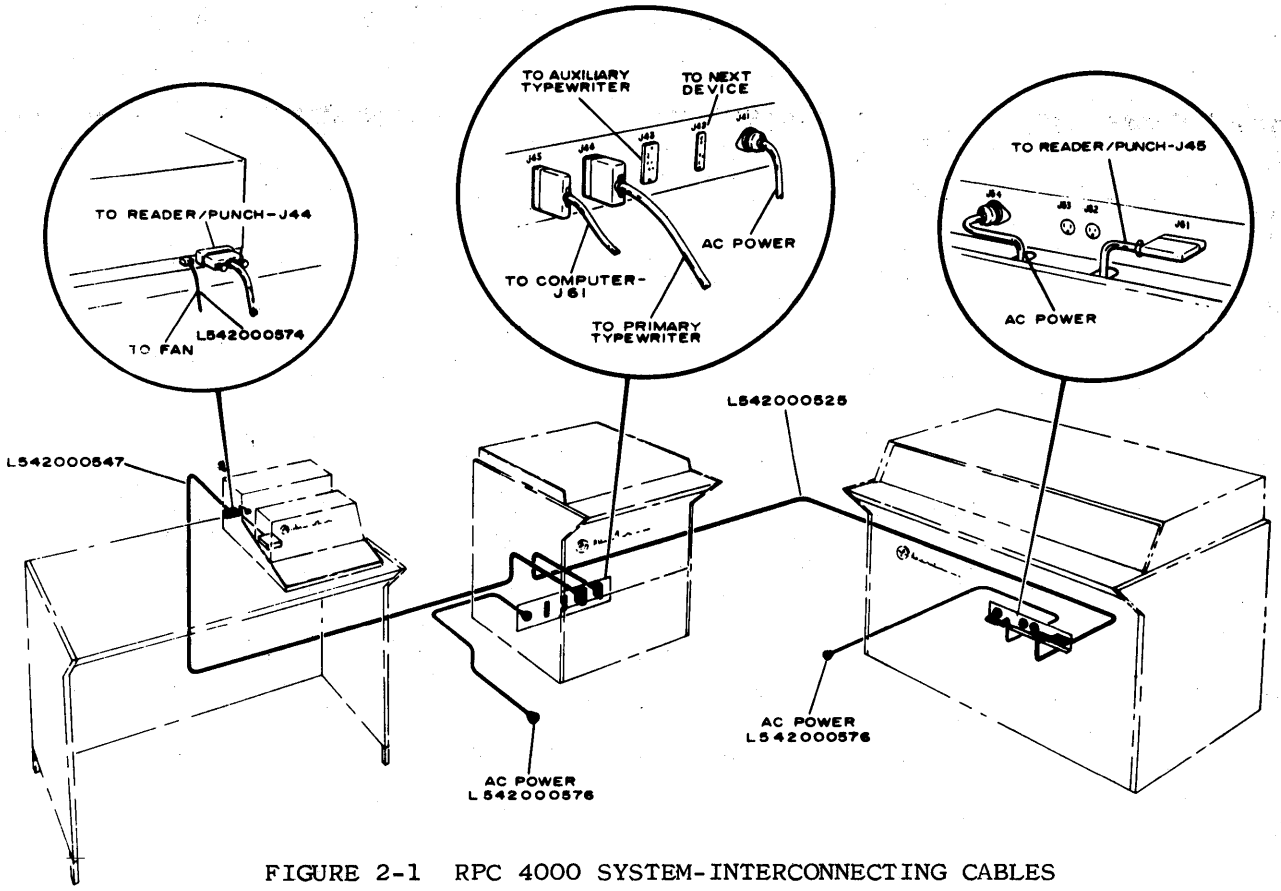

FIGURE 2-1 RPC 4000 SYSTEM-INTERCONNECTING CABLES

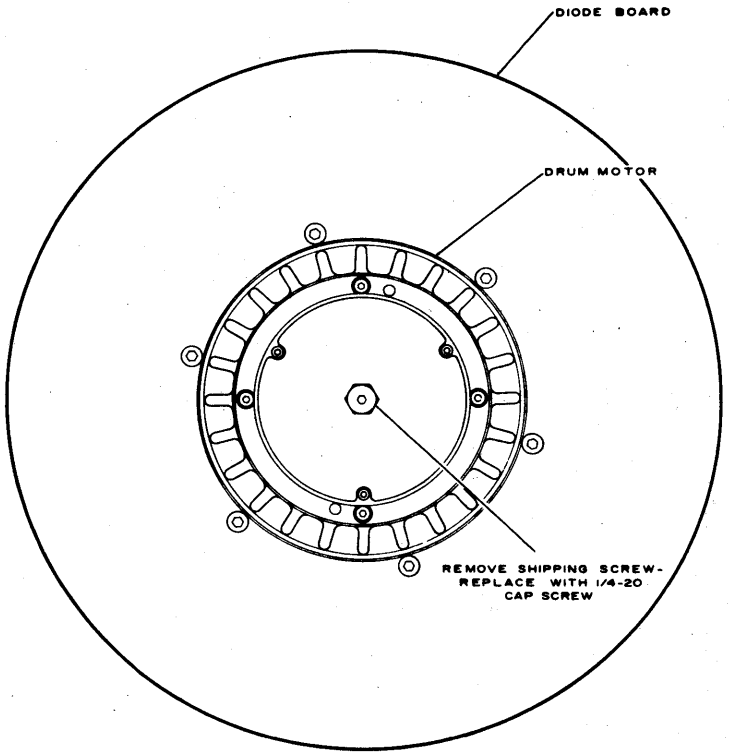

FIGURE 2-2 DRUM SHIPPING SCREW LOCATION

SECTION 3

OPERATION

ILLUSTRATIONS

SECTION 3

OPERATION

3.1 Operating Controls and Indicators--The operating controls for the RPC-4000 system are contained on three control panels, in addition to the typewriter keyboard. The RPC-4010 Computer control panel provides operator control of the computer and the digital display on which the contents of the register are displayed.

The two control panels on the RPC-4430 Reader/Punch provide manual control of the input/output devices, either on-line or off-line. The primary control panel provides operator control over the complete RPC-4000 system and gives a visual representation of the next character to be read. The auxiliary control panel gives the operator manual control of the Reader/Punch and Typewriter whether they are operating on-line or off-line.

3.2 RPC-4010 Control Panel--The computer control panel (figure 3-1) contains the switches necessary to provide operator control of the computer and the digital display on which the contents of the four registers are displayed.

The POWER ON and POWER OFF switches are non-latching. When the power is off, no lights are on. When the POWER ON switch is depressed, a holding relay closes which completes the AC circuit to the drum motor, fan, and DC power supply. When the POWER ON button glows it indicates that the AC power circuit is complete.

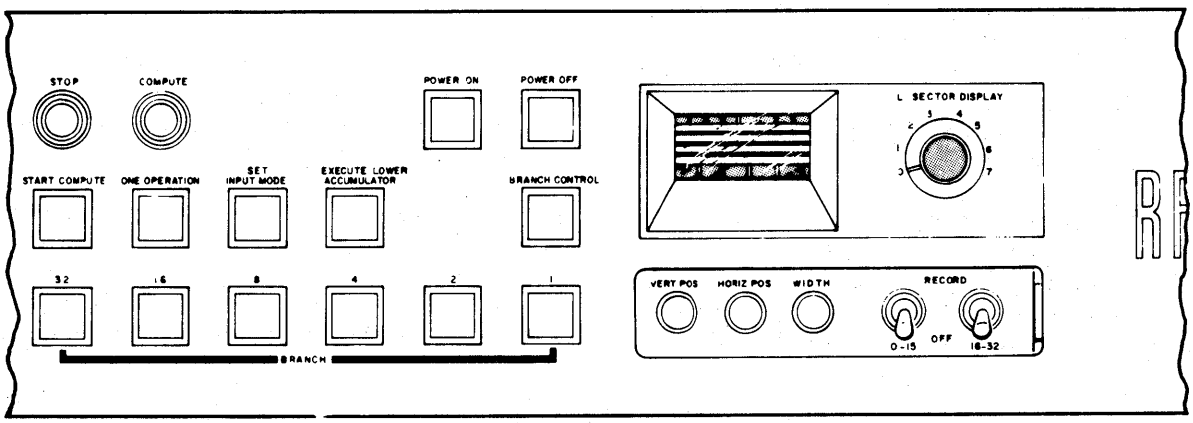

FIGURE 3-1 RPC 4010 CONTROL PANEL

Recording is prevented by a time delay until the drum reaches full speed in order to prevent loss of data from main memory. When the time delay relay closes, power is available for the rest of the control panel lights. The START COMPUTE light is turned on, and other lights may be on, depending on the setting of the switches. This indicates that the computer is ready to operate.

There are two indicator lights, a red one labeled STOP and an amber one labeled COMPUTE. The COMPUTE light is on when there is continual cycling through the phases, and the STOP light is on when the computer is stopped in phase 1 or phase 3. When the computer is stopped, it may be started by pressing the button labeled START COMPUTE.

The switch labeled ONE OPERATION is a latching switch. When it is depressed, the computer will stop in phase 3 after the execution of each instruction.

The effect of the SET INPUT MODE switch is dependent on the ONE OPERATION switch. With the ONE OPERATION switch depressed, the SET INPUT MODE switch conditions the computer to accept information from the input devices by setting an INPUT command (08) in the order flip-flops. With the ONE OPERATION switch not depressed, the SET INPUT MODE switch clears the lower accumulator.

The EXECUTE LOWER ACCUMULATOR switch is effective only when the ONE OPERATION switch is depressed. When it is depressed in the ONE OPERATION mode, the lower accumulator, rather than memory, becomes the source of the next instruction.

To input and execute an instruction manually, the following steps are followed:

1. Depress ONE OPERATION.

2. Depress SET INPUT MODE.

3. Depress EXECUTE LOWER ACCUMULATOR.

4. Read in one or two words from the typewriter or tape. If two words are read, the first word goes into the upper accumulator. The last word entered remains in the lower accumulator and is the instruction to be executed.

5. Depress START COMPUTE (or stop code on tape, or stop code key on typewriter).

The instruction in the lower accumulator will be transferred to the command register and executed. To input additional instructions and execute them, repeat steps 3, 4, and 5.

The BRANCH CONTROL light comes on when the branch control flip-flop is turned on. Depressing the BRANCH CONTROL switch resets the banch control flip-flop. The BRANCH switches, labeled 1, 2, 4, 8, 16, and 32 are used in conjunction with the SENSE (00) command to sense the operand track number of this command. When any bit of the track number corresponds to a depressed BRANCH switch, the branch control flip-flop is turned on.

The DIGITAL DISPLAY is a cathode ray tube covered with a mask to designate the four sweeps which display the contents of U, L, C, and X. Three controls are provided beneath the face of the oscilloscope to allow the operator to align the four sweeps in their respective windows. Two RECORD switches are located under a sliding panel to protect a program that is to be stored permanently. The left hand switch inhibits recording in tracks 0 through 15. The right hand switch inhibits recording in tracks 16 through 31.

3.3 Control Panel Operations--The operator may step through a program without executing any of the commands, by manipulating the SET INPUT and START COMPUTE switches, with the computer in one operation mode. With the ONE OPERATION switch depressed, the SET INPUT switch is depressed. This sets up an input order which is executed instead of the order in the C register, which remains unchanged. When the START COMPUTE switch is depressed, the input order is initiated and the computer stops in phase 1. Pressing the START COMPUTE switch will then end the input cycle and replace the contents of the C register with the contents of the memory location specified by the previous next instruction address in C. Because the ONE OPERATION switch is latched, the computer then stops in phase 3.

If the operator wishes to step through a program, executing one operation at a time, he may do so by depressing the ONE OPERATION switch. When the START COMPUTE switch is depressed, the computer will execute the instruction in C, copy the next instruction into C and stop.

To enter a bootstrap routine into the computer, both the ONE OPERATION and EXECUTE LOWER ACCUMULATOR switches are latched, and the SET INPUT switch is depressed. When the START COMPUTE switch is depressed, the input command set up by the SET INPUT switch is executed and the selected input device is started. After the information is read into the computer, the input device sends the computer a start signal as a result of: reading a stop code on the tape, depressing the stop code key on the typewriter, or depressing the START COMPUTE switch on the primary control panel of the RPC-4430 Reader/Punch, which places the computer in phase 3. With the EXECUTE LOWER ACCUMULATOR switch latched, the instruction which has just been read into L is transferred to C before phase 3 is entered. The START COMPUTE switch is depressed to execute the instruction, and the SET INPUT switch is depressed to set the computer for another input. Both the ONE OPERATION and EXECUTE LOWER ACCUMULATOR switches are unlatched, and the START COMPUTE switch is depressed to execute the input instruction. When these last operations are completed, manual loading is finished and the balance of the bootstrap program enters the computer under program control.

3.4 RPC-4430 Primary Control Panel--Control of input and output of information is exercised through the primary control panel of the RPC-4430 Reader/Punch, located on the top right hand side of the unit (figure 3-2). The functions of the switches on this panel are as follows:

SYSTEM POWER is a two-position switch which is used to turn electrical power on or off for all input and output devices in the system. The POWER switches on the individual input or output devices are connected in series with this SYSTEM POWER switch, so that both switches must be on to apply power to the unit.

SINGLE CHAR. MODE is a two-position switch used to stop input and start the computer after each character is read. The SINGLE CHAR. MODE switch also enables the computer to receive some characters it would otherwise ignore. The computer cannot be used in lengthened lower mode with the RPC-4500 in single character mode.

There are two switches associated with the PARITY MONITOR. INHIBIT is a two-position switch used to inhibit parity checking of input data when latched. RESET is a momentary switch to reset the error when a parity error is detected and the computer stops.

The MASTER RESET switch, when depressed, disconnects all selected input and output units from the computer.

There are two switches associated with INPUT DUPLICATION. The SELECT switch allows selected output devices to duplicate input data as it enters the system. The RESET switch inhibits input duplication.

The START READ and STOP READ switches are used to initiate and inhibit the operation of the selected input device.

The START COMPUTE switch manually initiates computer operation.

In addition to the controls on the primary control panel, there are seven character indicator lights which represent the bit pattern of the next character to be read into the computer.

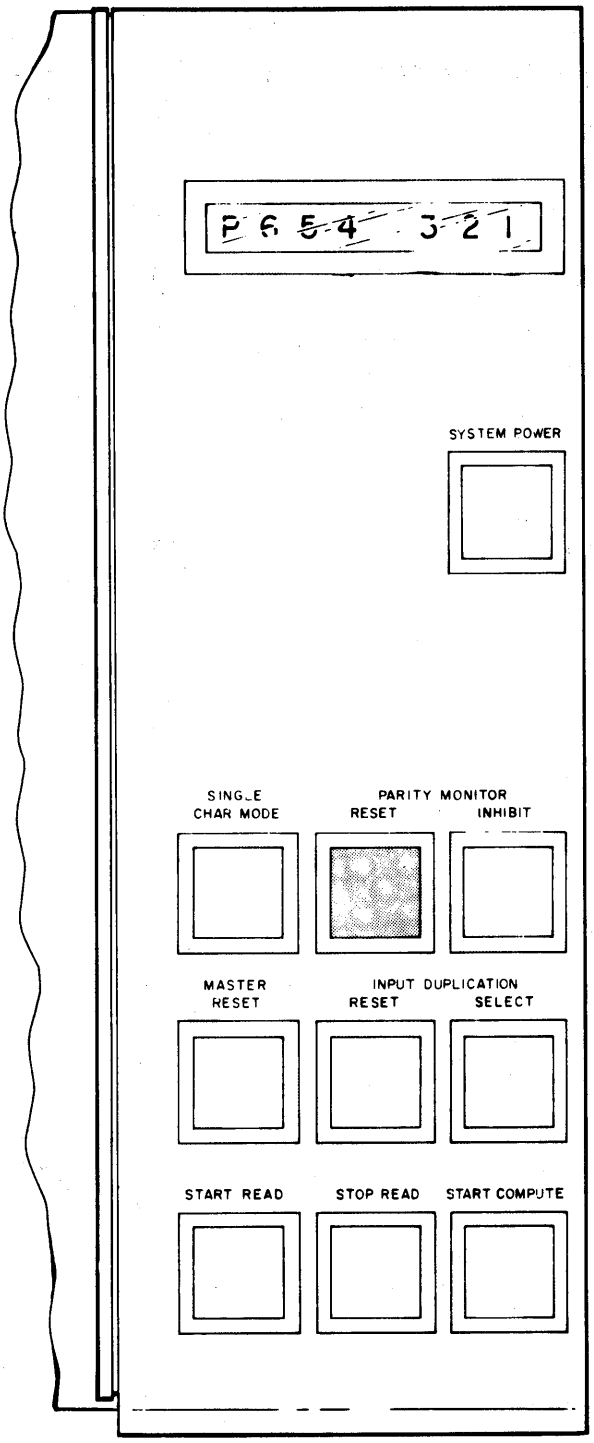

FIGURE 3-2 RPC 4430 READER/PUNCH CONTROL PANEL

3.5 RPC-4430 Auxiliary Control Panel--In addition to its operation as the input/output control unit of the RPC-4000 system, the RPC-4500 Tape-Typewriter System may be used off-line as a tape controlled, tape producing, manual or automatic typewriter. Selection of input or output units to be connected to the computer

is also controlled by the auxiliary control panel located on the top left hand side of the RPC-4430 Reader/Punch (figure 3-3).

The POWER switch turns the RPC-4500 power on or off. The SELECTION MONITOR indicator glows, indicating that a unit of the RPC-4500, selected for operation with the computer, is in the off-line mode of operation.

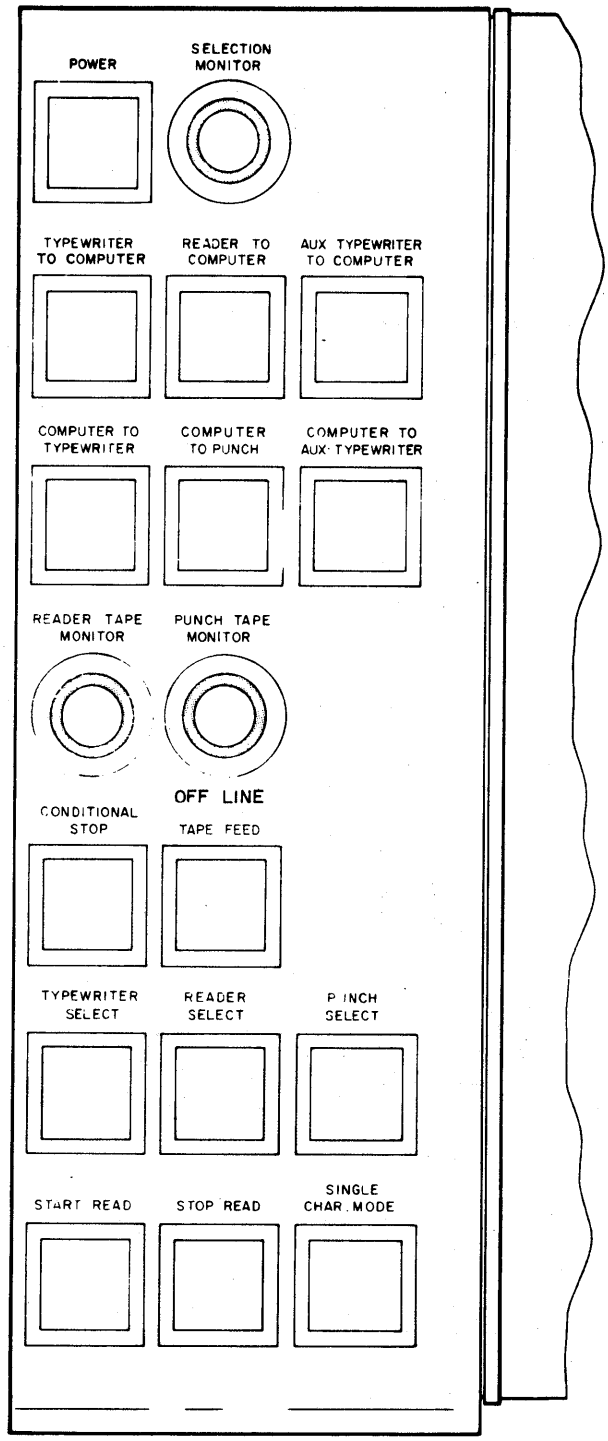

FIGURE 3-3 RPC 4430 READER/PUNCH AUXILIARY CONTROL PANEL

Six switches are provided to manually interconnect the input and output units of the RPC-4500 with the computer. The labels on these switches indicate their functions as follows: TYPEWRITER TO COMPUTER, READER TO COMPUTER, AUX. TYPEWRITER TO COMPUTER, COMPUTER TO TYPEWRITER, COMPUTER TO PUNCH, and COMPUTER TO AUX. TYPEWRITER.

TAPE MONITOR lights are provided for both the tape reader and the tape punch. When either of the units is out of tape, or the tape is jammed, the light will glow to indicate the unit that is inoperative.

The CONDITIONAL STOP switch is depressed to allow continued operation of an input device when a stop code is sensed.

The TAPE FEED switch is depressed to punch sprocket feed holes in the paper tape.

Three switches are provided to select the RPC-4500 units to operate in the off-line mode. The switches are labeled: TYPEWRITER SELECT, PUNCH SELECT, and READER SELECT. START READ and STOP READ switches are provided to initiate or inhibit reader operation in the off-line mode. The SINGLE CHAR. MODE switch allows the reader to read only one character and stop.

SECTION 4

THEORY OF OPERATION

THEORY OF OPERATION (Cont.)

ILLUSTRATIONS

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SECTION 4

THEORY OF OPERATION

4.1 General--The logical design of the RPC-4000 computer system is based on the specification of conditions under which the states of the internal flip-flops are determined, or output signals are generated. These conditions are described symbolically as logical function of the states of these flip-flops and inputs to the logical network.

The algebraic equations used in describing logical operations are expressed as minus five volts corresponding to the on (or true) state of the signal, and zero volts corresponding to the off (or false) state of the signal.

With respect to the flip-flops, an unmodified character denotes the signal derived from the on side of the flip-flop, and an underscored character denotes the signal derived from the off side of the flip-flop. For example, with flip-flop F on, the F output is true (-5V) and the $\underline{F}$ output is false (0V). With F off, the F output is false (0V) and the $\underline{F}$ output is true (-5V).

The conditions required to set a flip-flop on or off are denoted by a prime (') symbol after the character, thus the equation $F' = \underline{F}\ G\ \underline{H} + \ldots$ indicates: set the F flip-flop true if F is false, G is true, and H is false. The plus sign followed by three periods indicates that the F' signal may be generated by additional terms not included in this equation.

For the purpose of understanding the theory of operation, the RPC-4000 computer system may be divided into five major sections: the control panel, the main memory, the four operating registers, the logic sections, and the input/output section (figure 4-1).

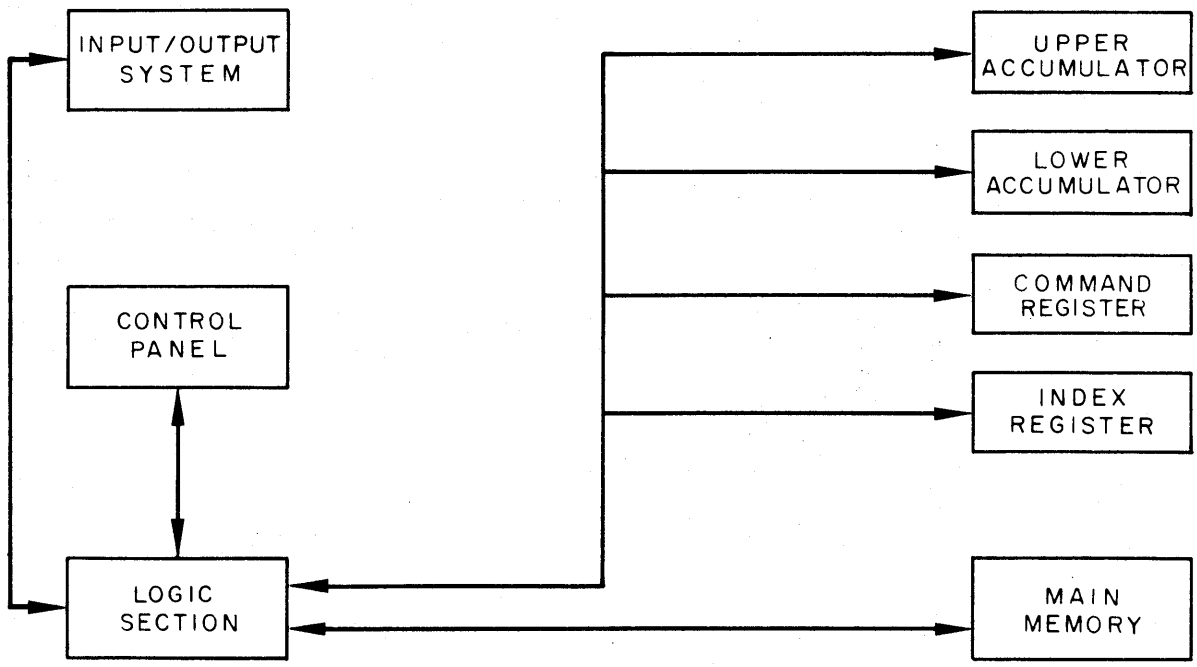


FIGURE 4-1 RPC 4000 COMPUTER SYSTEM BLOCK DIAGRAM

4.2 RPC-4010 Computer--The control panel contains the switches necessary to provide operator control of all computer functions. A display of the contents of the four operating registers is provided on the panel, along with associated controls.

Main memory is composed of 8,008 words of storage on a magnetic drum, and the associated logic necessary to locate a specific track and sector of the drum. One hundred twenty-eight track addresses are provided, each with sixty-four sectors of one word length (32 bits).

The four operating registers are normally one word circulating lines, recording on and reading from the magnetic drum.

The logic section of the RPC-4010 Computer contains the electronic circuits which perform control and arithmetic functions according to program or operator instructions.

The input/output section is composed of a typewriter, a paper tape reader, a paper tape punch, and the logic required for co-ordinating these devices with the computer. These units are described in section 4.10 of this manual.

4.3 RPC-4010 Control Panel--The controls on the RPC-4010 Computer provide the means of determining the mode of operation and a visual display of the state of selected components of the computer.

POWER ON is a momentary pushbutton which applies AC power to the computer elements by energizing Relay K-1 (figure 4-2). In turn, Relay K-1 completes a

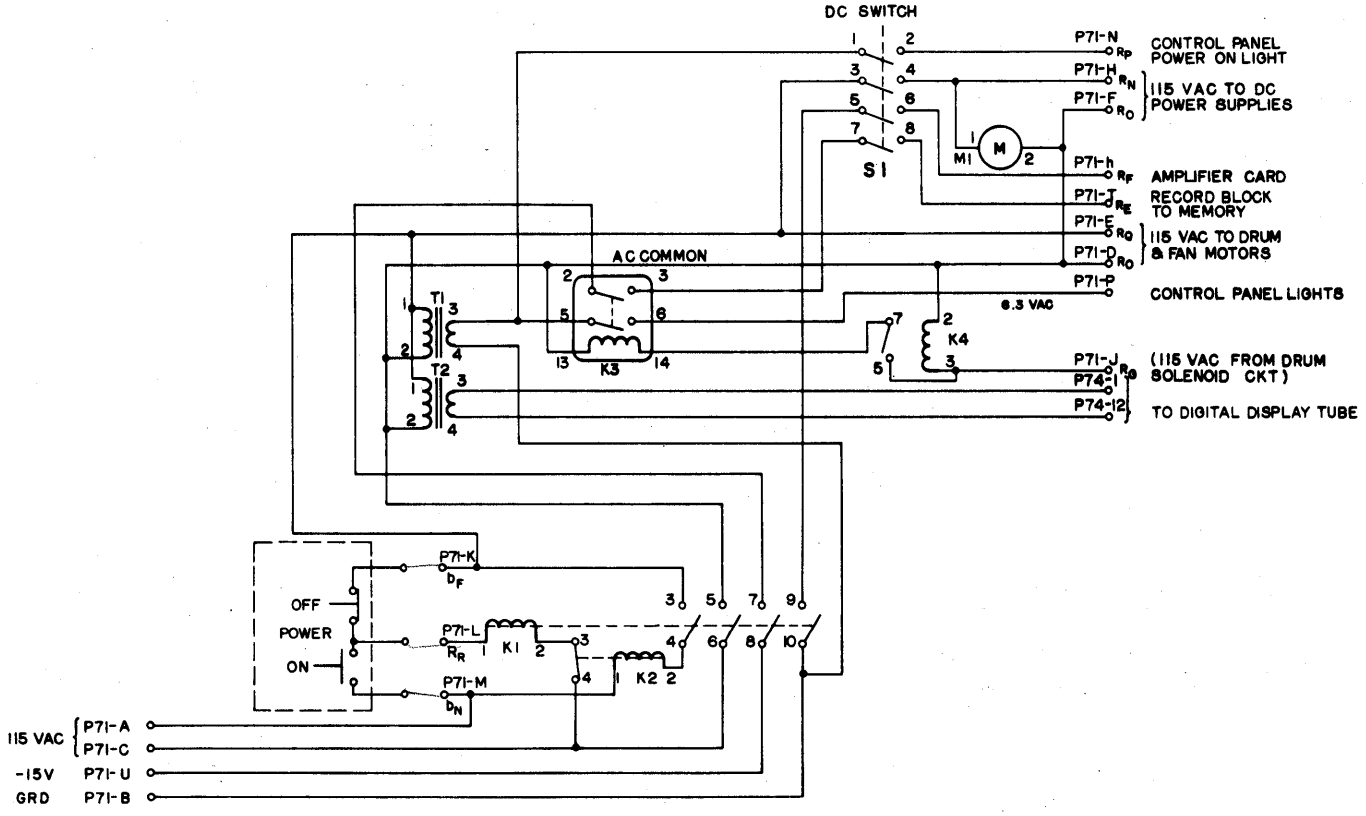


FIGURE 4-2 COMPUTER POWER CIRCUIT

holding circuit through overload Relay K-2 and the POWER OFF pushbutton. Relay K-1 also completes the AC common circuit, applies an AC potential to switch S-1, completes the AC circuit to transformers T-1 and T-2, applies a -15 volt DC potential to Relay K-3, and applies DC ground to switch S-1.

With AC power applied to the drum motor, a 90 second time delay relay on the drum completes the AC circuit to K-4, a 90 second time delay relay in the power control section. These relays allow approximately three minutes for the drum to reach operating speed before energizing Relay K-3. Relay K-3 applies the -15 volt DC R_e signal to memory, allowing information to be written into or read from memory. Relay K-3 also completes the 6.3 volt AC circuit from transformer T-1 to the control panel lights.

The -15 volt DC is applied to Relay K-3 through Relay K-1. When a line transient occurs which is large enough to make Relay K-1 drop out, recording is immediately inhibited so that resulting transients from the DC power supplies can do no damage. Thus, memory is protected against transients which might turn the computer off.

With S-1 (the DC switch) in the on position, the AC circuit is completed to the DC power supplies, and DC ground is applied to the amplifier card and to the POWER ON light.

The POWER OFF pushbutton opens the K-1 relay holding circuit. When K-1 opens, all power to the computer is removed, except to the POWER ON pushbutton.

The START COMPUTE switch is a momentary make-before-break pushbutton which holds the computer start compute signal (b_S) to the same potential as the start compute signal (Z_S) from the RPC-4430 Reader/Punch. When the START COMPUTE switch is depressed, or when Z_S from the Reader/Punch goes true, input enable is pulled false and b_S is pulled true by a resistor on the logic board. The make-before-break prevents contact noise from giving the effect of multiple start signals (figure 4-3).

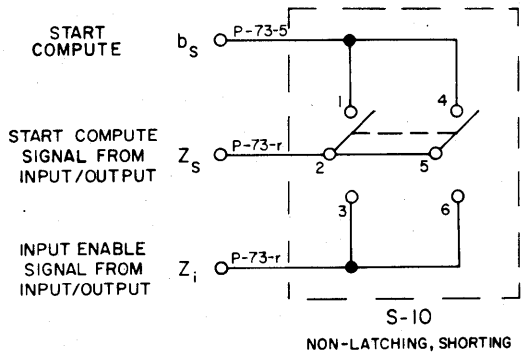


FIGURE 4-3 START COMPUTE CIRCUIT

The ONE OPERATION switch is a two-position pushbutton which, when depressed, allows the computer to operate through one cycle of the four phases and then stop, rather than operate continuously. When ONE OPERATION is not depressed, the execute lower accumulator signal (bc) is held to ground, effectively interlocking the EXECUTE LOWER ACCUMULATOR and SET INPUT pushbutton (figure 4-4).

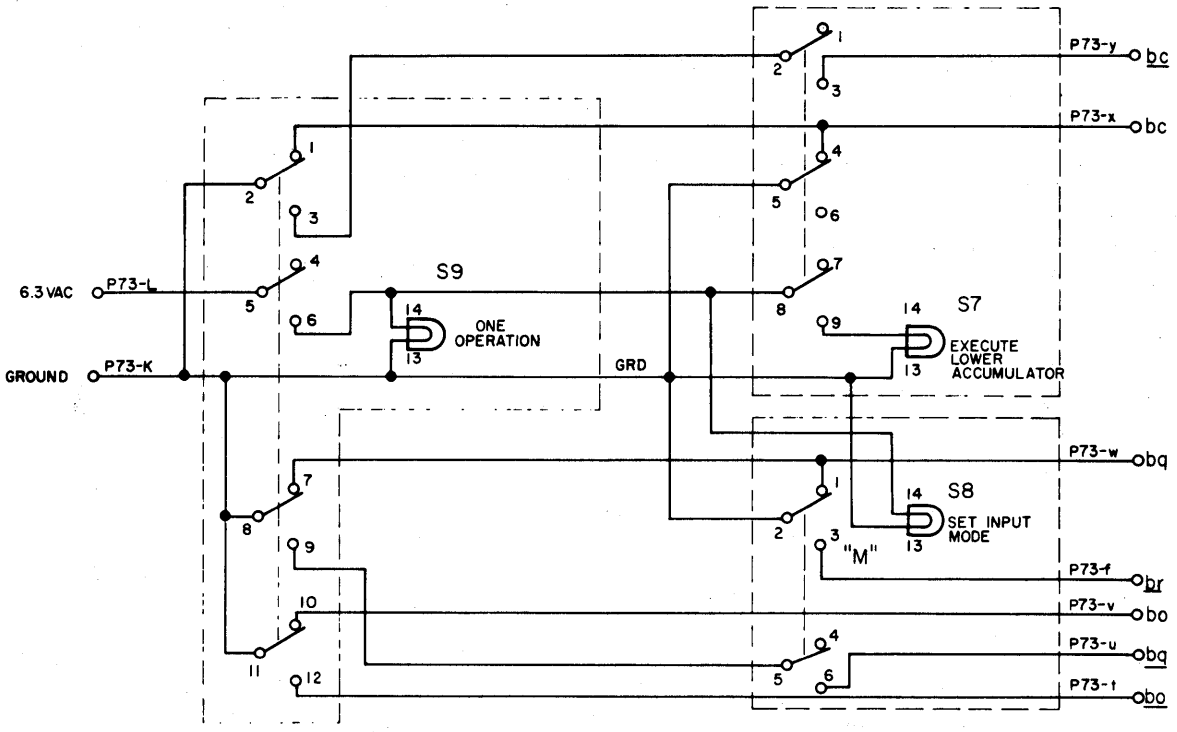


FIGURE 4-4 ONE OPERATION INTERLOCK

Pressing the SET INPUT MODE momentary contact pushbutton is effective only when the ONE OPERATION pushbutton is depressed, as indicated when both the ONE OPERATION and SET INPUT MODE pushbuttons glow. When depressed, contacts 1 and 2 of the SET INPUT MODE pushbutton remove ground from the set input signal (b_q), and contacts 5 and 6 hold $\underline{b_q}$ to ground. This sets the lower accumulator to non-lengthened mode, and forces the order (Q) flip-flops into the input mode, thus conditioning the computer to accept information from input. Also, the operand track in the command register is set to zero, to insure that the character flip-flops reset and that the computer will accept input in four-bit mode. The lower accumulator is set to zero at this time to accept input data. In addition, the phasing flip-flops are set to phase 3.

The EXECUTE LOWER ACCUMULATOR switch is a two-position pushbutton, which is effective in the one operation mode only. When depressed, the b_c signal is held true, and the lower accumulator (either lengthened or non-lengthened), rather than memory, is the source of the next instruction word.

When in the normal, or off position, contacts 2 and 3 are open, allowing $\underline{b_c}$ to go negative, and contacts 4 and 5 are closed, holding b_c to ground. This causes memory (V) to be the source of the next instruction.

The light under the BRANCH CONTROL pushbutton indicates that the branch control flip-flop is on. The BRANCH CONTROL pushbutton lets the reset signal (b_b) go on. This resets the branch control flip-flop, which turns off the light under the pushbutton.

The two-position branch switches, labeled 1, 2, 4, 8, 16, and 32, are used in conjunction with the OO (SENSE) command. The six switched lines are normally held to ground (false). When depressed, the ground connection is broken, allowing the output to go true, and causing the light under the pushbutton to glow. (See Section 4.9.2, description of the OO (SENSE) command for operation.)

Two RECORD switches are provided which control the record voltage (R_e) to columns 0 and 1 of the main memory head matrix. In the on position, the 0-15 switch allows normal record/read functions on tracks 0 through 15. When it is in the off position, record or read functions may not be carried out on tracks 0 through 15. This non-record/read is accomplished by opening the R_e circuit to column 0. Similarly the 16-31 switch controls column 1 of the main memory matrix. These switches are used to protect the information recorded on tracks 0 through 31.

4.4 Digital Display--The digital display is located on the right side of the control panel. Associated with the display are the sweep positioning and size controls, and the L SECTOR DISPLAY switch.

The contents of the U, L, C, and X registers are displayed on the digital display tube. Each register is displayed cyclically for one word period out of every eight.

The digital display circuits are contained on two cards, the horizontal drive card and the vertical drive card. The horizontal drive circuit applies a sawtooth sweep signal to the horizontal deflection plates of the oscilloscope display tube. The vertical drive circuit provides four sweeps, vertically displaced from each other, and applies the digital information to be displayed to the vertical deflection plates (figure 4-8).

On the horizontal drive card (figure 4-5), flip-flop FF, composed of transistors Q8 and Q11, controls the sawtooth generator. When FF is off, the horizontal sweep occurs; when FF is on, the retrace occurs. During the sign bit period of each word, timing signal t_6 is true. FF is turned off by the leading edge of a t_6 pulse and is turned on at the end of the following t_6. Thus, FF is off for 33 bit periods (one word period plus one bit period) for the horizontal sweep. This arrangement allows the horizontal sweep one bit period in which to become linear. A mask on the face of the oscilloscope prevents the display of the extra bit.

The horizontal sweep is produced by a sawtooth generator composed of transistors Q1 and Q2. With FF true, Q2 is conducting and holds the base of Q5 to ground. When FF goes false, Q2 cuts off, allowing Q1 to pull the base of Q5 negative. As Q5 begins conducting, Q6 and Q8 convert the current waveform produced into a voltage waveform of the proper amplitude for one horizontal plate. Transistors Q7 and Q10 function in the same manner to produce a voltage waveform of the proper amplitude for the other horizontal plate. Thus, the horizontal sweep is produced during alternate word periods.

The vertical drive card (figure 4-6) selects the four registers sequentially by the use of a counter. The two flip-flops which are connected to form the counter are referred to only as A and B in this description. A is composed of Q1 and Q3; B is composed of Q2 and Q4. Flip-flops A and B change state only when FF is changing state from false to true. This occurs at intervals of two word per-

iods, and the counter remains at each count for two word periods. Diode logic gates combine the four signals, A, $\underline{A}$, B, and $\underline{B}$, into AB, $A\underline{B}$, $\underline{A}B$, and $\underline{AB}$. These signals are combined, in another diode gate, with the inverted read signals of the four registers: U, C, L, and X. The output of this gate is designated, in this description only, as Ru', the input signal to Q6. The logical equation is:

$$Ru' = (A\ \underline{B}\ \underline{U} + \underline{A}\ \underline{B}\ \underline{L} + \underline{A}\ B\ \underline{C} + A\ B\ \underline{X})\ \underline{FF}$$

The output of Q6 (Ru) is the information to be displayed. It is fed through the vertical gain control to the lower vertical deflection plate.

The combined signals from A and B are sent to the upper vertical plate through the vertical positioning circuit. $A\underline{B}$ is connected directly to the base of Q5 to produce the upper trace. $\underline{AB}$ and $\underline{A}B$ are connected through the L-position and C-position potentiometers, respectively, to the base of Q5 to produce the two intermediate traces. These two traces are independently adjustable. AB bypasses Q5, producing the lowest trace.

The counter remains in each of its four states for two word periods (figure 4-7). During the first word period, the content of U is displayed as the upper trace, followed by one word period of retrace. In the third word period, the content of L is displayed as the upper intermediate trace, followed by one word period of retrace. During the fifth word period, the content of C is displayed as the lower intermediate trace, followed by one word period of retrace. In the seventh word period the content of X is displayed as the lowest trace, followed by one word period of retrace. The length of a complete cycle is 2 milliseconds, $\frac{1}{4}$ of a millisecond for each display. The cyclic rate is such that four simultaneous traces appear on the face of the tube.

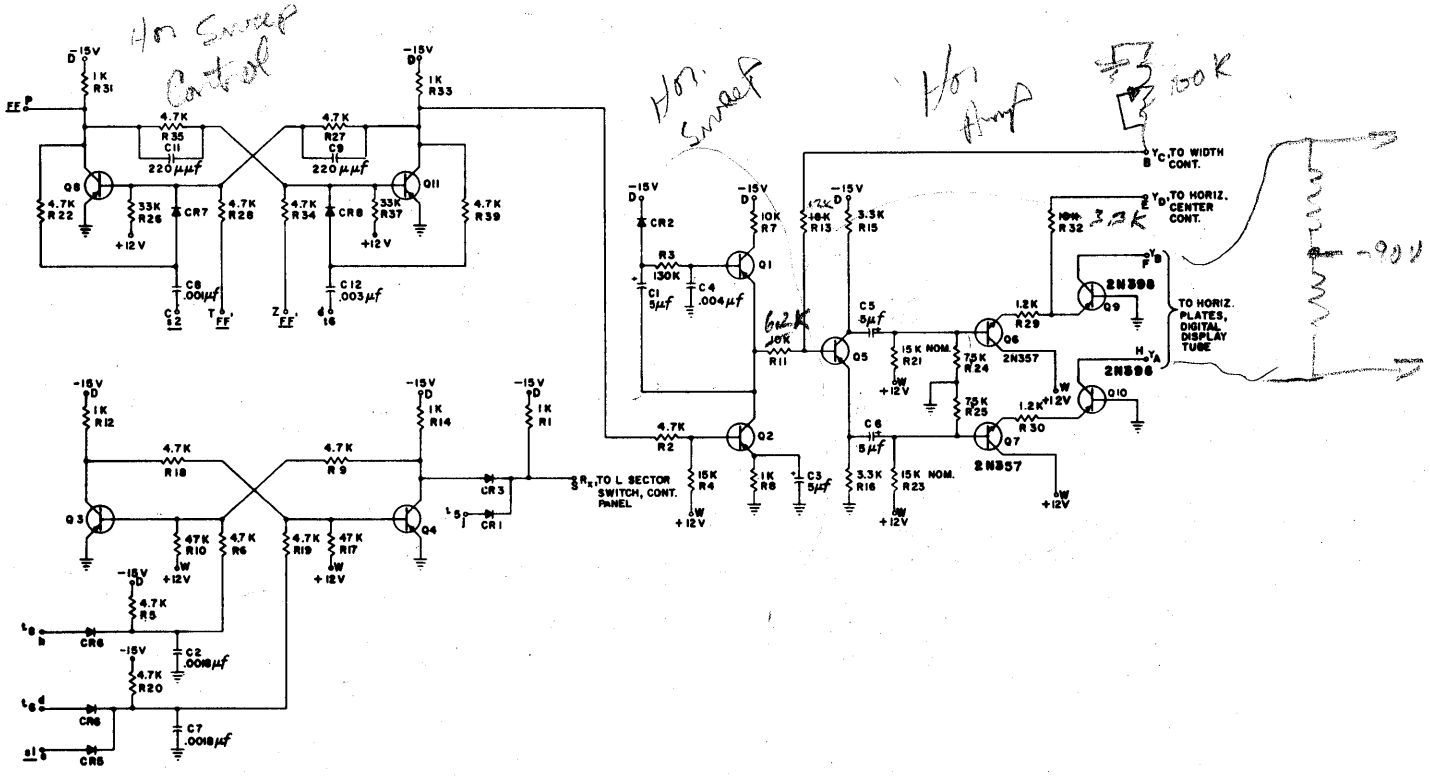


FIGURE 4-5 DIGITAL DISPLAY HORIZONTAL DRIVE CIRCUIT

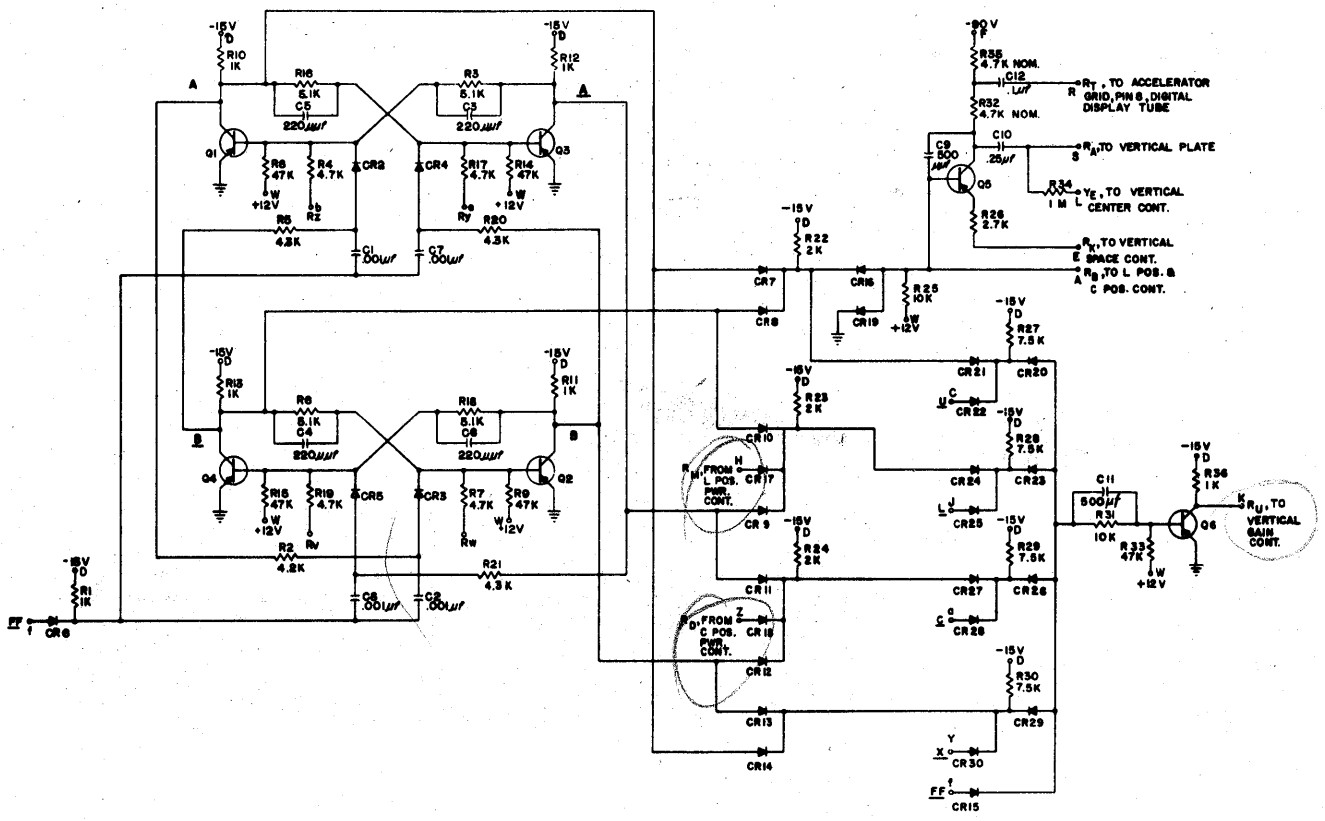


FIGURE 4-6 DIGITAL DISPLAY VERTICAL DRIVE CIRCUIT

When L, the lower accumulator, is in lengthened mode, i.e., eight words long, different information is read from L every word time. When eight word times have elapsed, the words are repeated. Since the Ru logic allows the same word to be displayed every eight words, only one word of lengthened L will be displayed. By selecting the primitive sector numbers, the L SECTOR DISPLAY switch selects which of the eight words in the eight word line is to be displayed.

The last bit time of every eighth word is defined by timing pulse t_8, which occurs simultaneously with t_6 during word period 7. The flip-flop, composed of Q3 and Q4 on the horizontal drive card is set true by t_8 and remains true during word period 0. The equation $\underline{S}_1\ t_6$ is true at sign time of every word period except when t_8 is true. $\underline{S}_1\ t_6$ sets the flip-flop false at the end of word period 0, and it cannot go true until the next t_8 sets it true. Hence it is true only during word period 0. The true output of this $\underline{S}_1\ t_6$ flip-flop is combined with timing pulse t_5 in an AND gate. This term is true at t_5 time, which is near the middle of the word period, and pulls the three wipers of the L SECTOR DISPLAY switch negative. The position of the L SECTOR DISPLAY switch forces flip-flops FF, A, and B to assume any one of eight possible combinations during word 0. Each of the eight different combinations will allow a specific word, of the eight words of lengthened L, to be displayed. During the remaining seven word periods the flip-flops count as indicated. L is displayed only when A, B, and FF are all false. The words in the other registers are unaffected since they are repeated every word time.

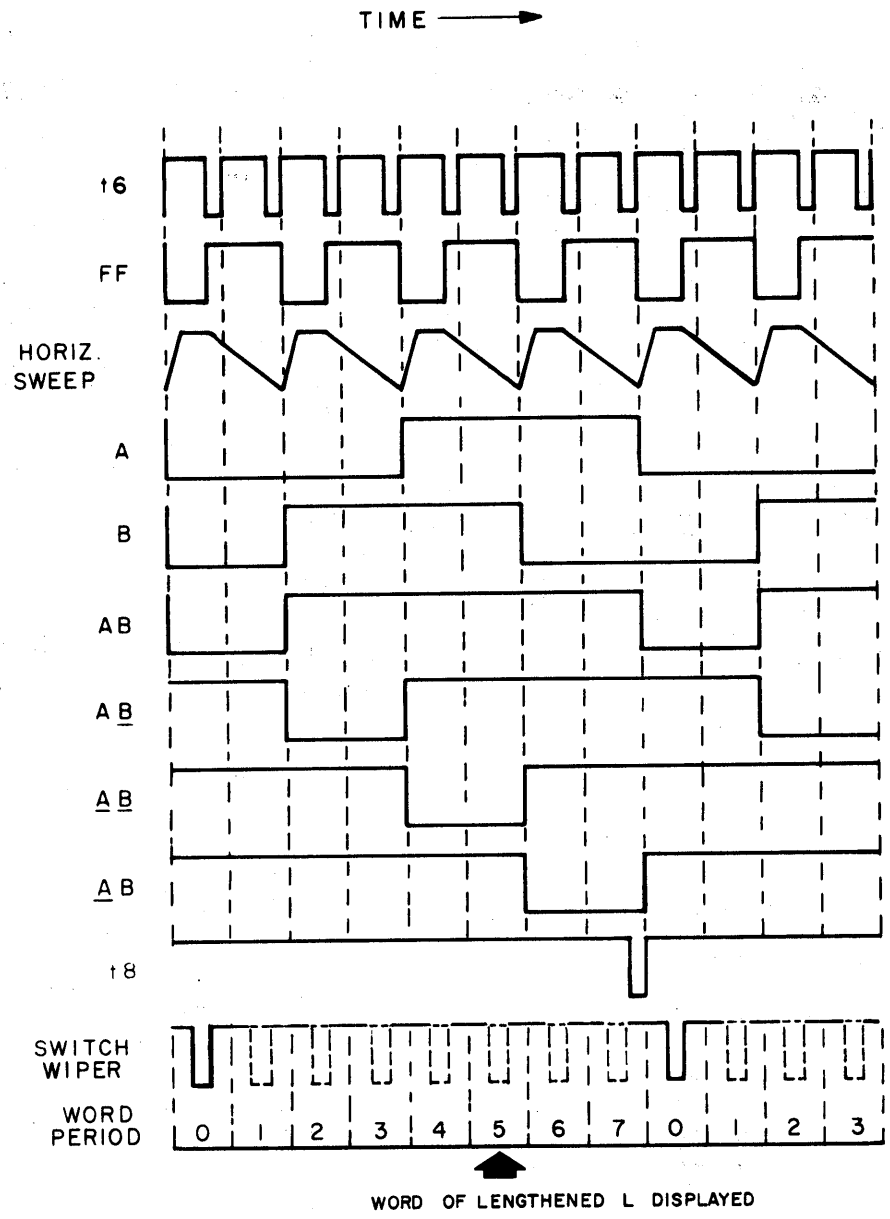


FIGURE 4-7 DIGITAL DISPLAY TIMING

4.5 Memory--The storage of all programs and data in the RPC-4010 Computer is on the magnetic drum. The magnetic coating of the drum is capable of storing approximately 256,000 bits (8,000 words of 32 bits) of main memory, and 640 bits (20 words of 32 bits) of temporary storage. It contains four permanently recorded timing tracks. In addition, spare tracks are provided.

The drum is a tapered aluminum cylinder coated with magnetic material. It is driven by a synchronous motor at 3,600 RPM. Thus, one drum revolution is about 17 milliseconds, one word time is 260 microseconds, and a bit time is 8.2 microseconds.

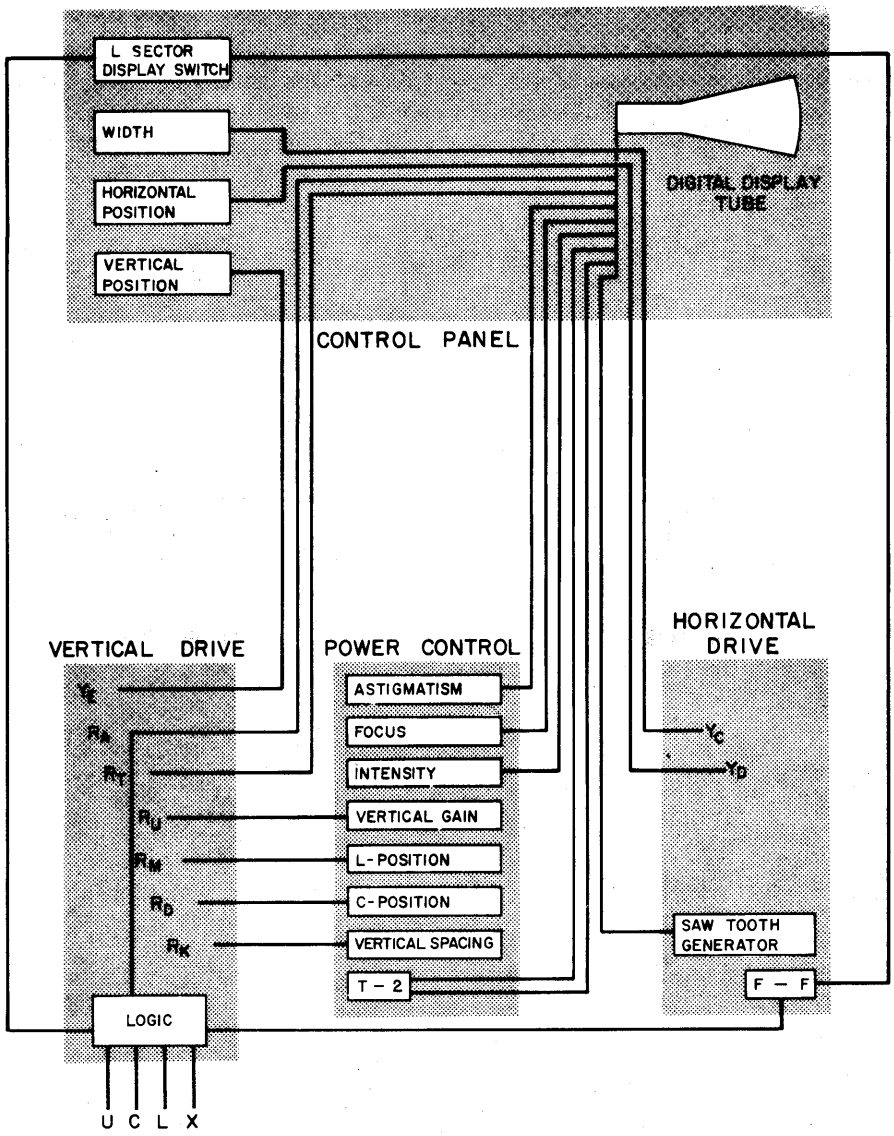


FIGURE 4-8 DIGITAL DISPLAY DIAGRAM

The heads read and record on a track which is 0.025 inches wide. Each track is divided into 64 sectors containing 32 bits, giving 2,048 bits per track. The tracks are numbered 000 through 127 and sectors are numbered 00 through 63. Any word recorded on the drum may be located by specifying its track and sector numbers. For example, the word recorded on sector 62 of track 15 is addressed as 01562. Selection of main memory record/read heads is made by the track selection matrix. The specific head addressed is selected by activating the row and column which intersect the head circuit (figure 4-9). The sector is found by comparing the sector with the permanently recorded sector numbers on the S_1 timing track. When these match, the following sector is selected. Timing and wave forms of the various signals are illustrated in figure 4-10.

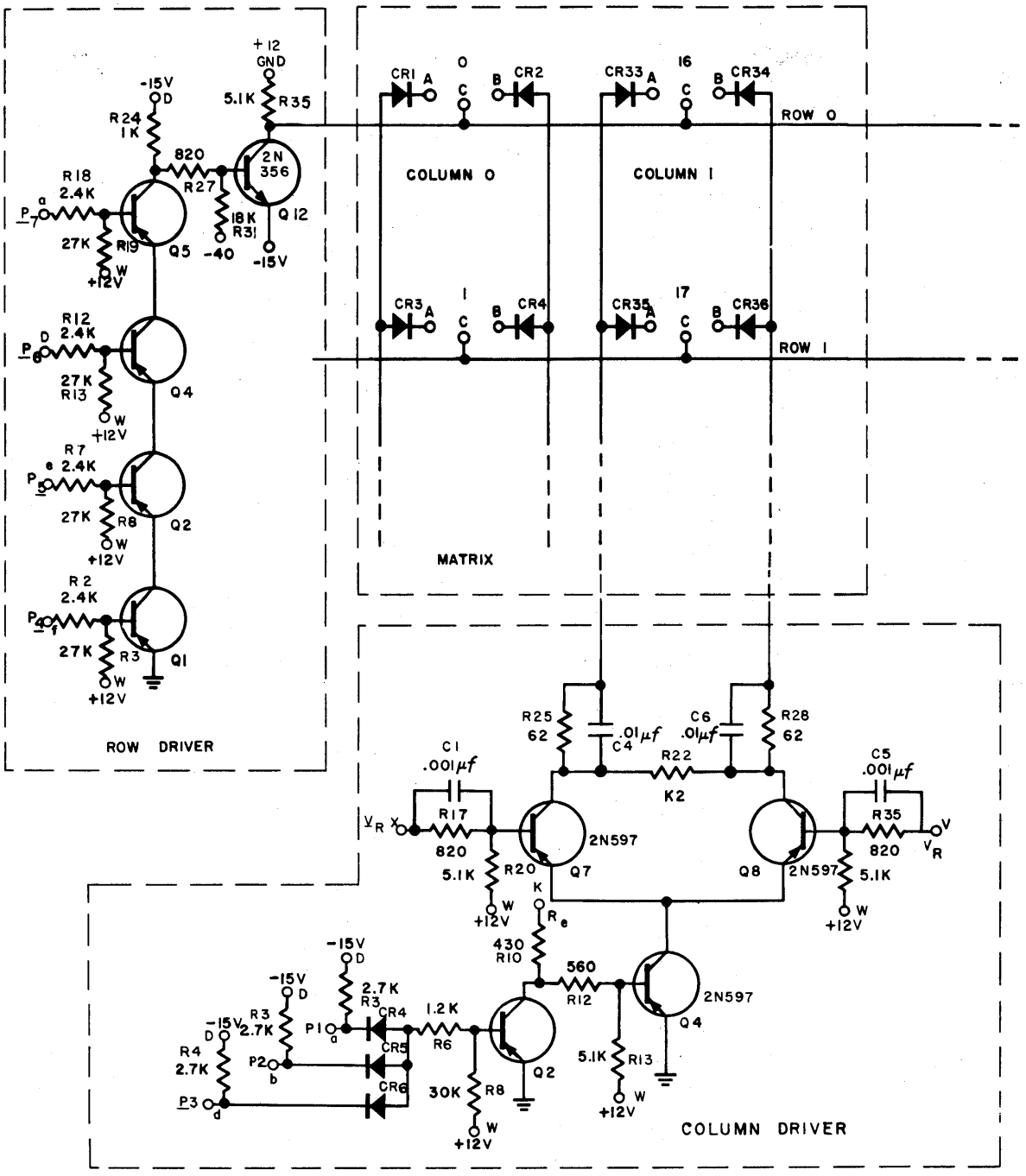


FIGURE 4-9 MAIN MEMORY HEAD SELECTION-RECORD

4.5.1 Read and Record Technique

Information is recorded on the drum by the Ferranti or phase modulation method. This method takes advantage of the fact that a change of direction of magnetic flux in the middle of a bit will generate a positive voltage in one direction. If the change is in the opposite direction, a negative voltage will be generated. With data recorded as phase information rather than amplitude in-

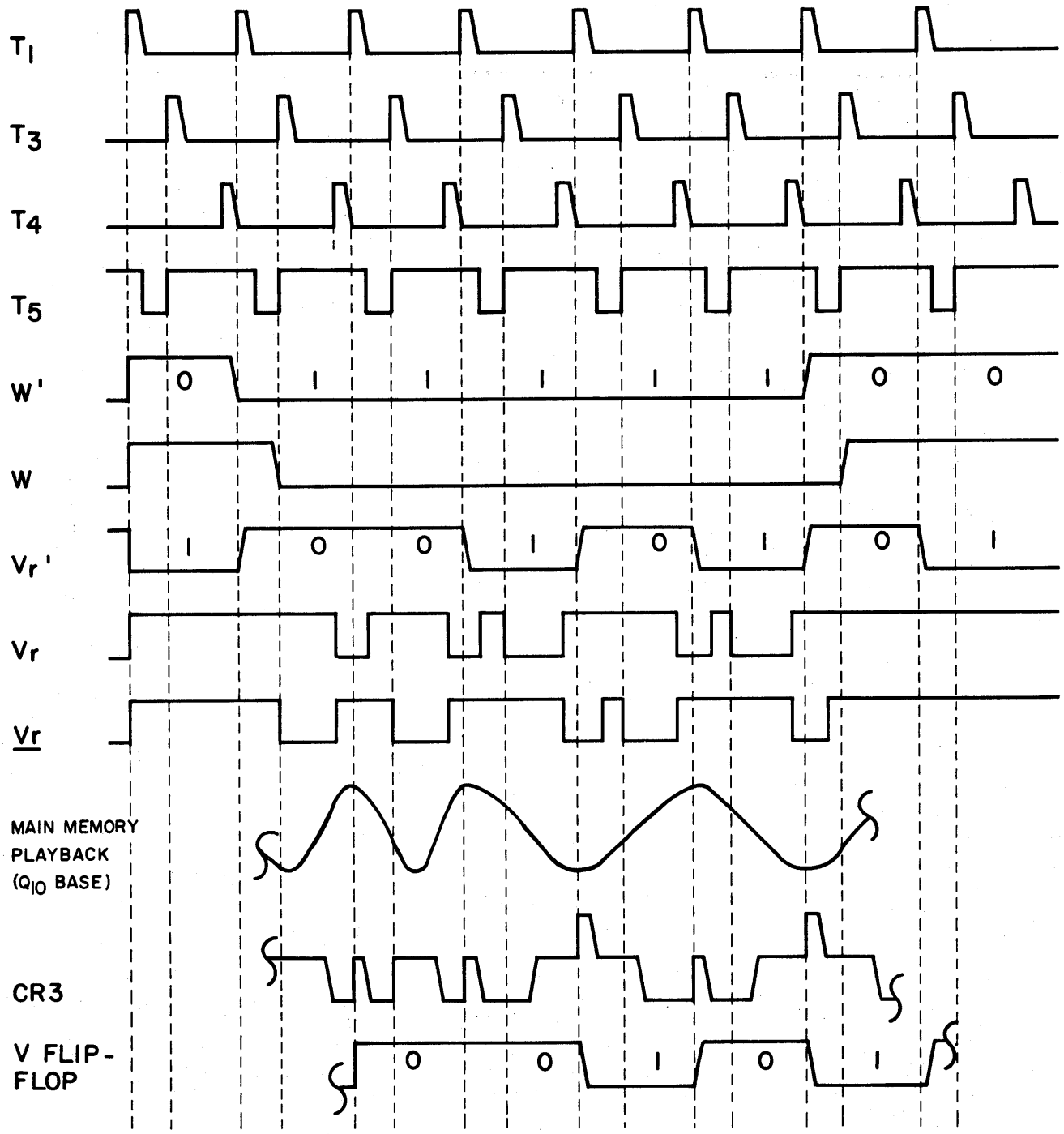


FIGURE 4-10 MAIN MEMORY TIMING WAVEFORMS

formation, each bit has a definite signal. This is opposed to NRZ (non return to zero) recording, wherein a signal occurs only at a change of bit information.

Each read/record head (figure 4-11) has a center-tapped winding on two pole pieces of ferrite. The pole pieces are separated by a silver shim. The silver provides a high reluctance path, causing the magnetic flux to pass around the shim through the air. At this point, the read/record head is 0.0013 of an inch from the magnetic surface of the drum, and the magnetic flux will magnetize the drum surface.

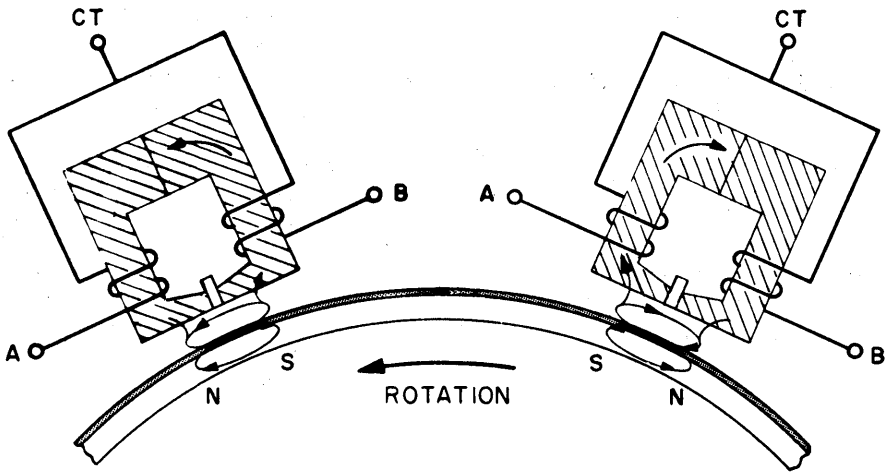


FIGURE 4-11 READ RECORD HEADS

A current of 200 milliamps applied to the A side of the head will generate a magnetic flux in the clockwise direction. As this flux passes the air gap, the surface of the drum will be magnetized. To complete recording of a bit, a 200 milliamp current is applied to the B side of the head one half bit period later. This generates a magnetic flux in a counter-clockwise direction. This flux magnetizes the drum surface in the opposite direction as it passes the air gap. The phase shift required for Ferranti recording may be caused in either direction by starting with the A or B lead. The direction of magnetism of the recorded areas on the drum surface will allow translation as they are read.

Reading of information from the drum surface takes place as the recorded areas pass under the head. The magnetization of each recorded area will cause a flux to be generated in the pole pieces of the head. As the flux changes direction, a voltage is induced in the head windings. At clock time, this voltage is read and amplified. A "one" or a "zero" is set into a read flip-flop on a read amplifier card, depending on the direction of the voltage.

The head voltage signal has two frequencies. All "one" or all "zero" signals have a frequency of 120 KC, and the alternating "1", "0", "1", "0", etc., signal has a 60 KC frequency. This frequency change is characteristic of the Ferranti recording system. There is always a signal peak in the middle of each bit, and the peak is clocked into the flip-flop to identify the bit.

4.5.2 Clock and Timing Tracks

The clock track is recorded on the drum and is read by a read head connected to the clock read amplifier. The head voltage is fed to transformed T1, on the clock read amplifier card. The outputs of T1 are amplified and drive the flip-flop composed of Q2 and Q3. The input to this read amplifier is approximately a sine wave, while the outputs CFF and $\overline{\text{CFF}}$ of the clock flip-flop are square waves with a period of approximately 8 microseconds.

Each clock flip-flop output triggers a blocking oscillator on the clock generator card (figure 4-12). The true side of the clock flip-flop triggers Q1 to drive switch Q2 and generate clock pulse T2. Through a 3 microsecond delay, switch Q3 is driven to generate T4.

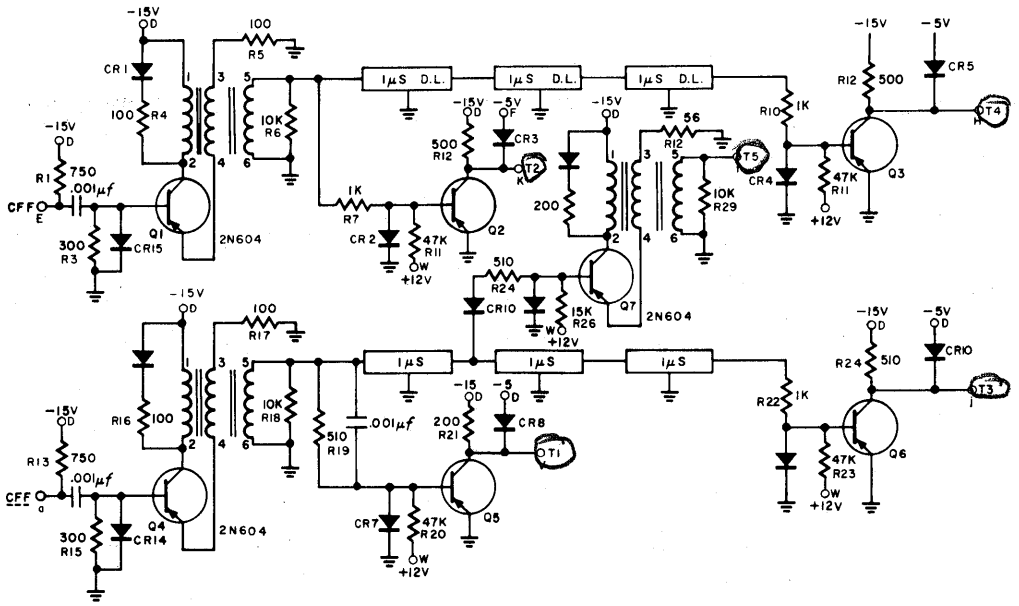


FIGURE 4-12 CLOCK GENERATOR

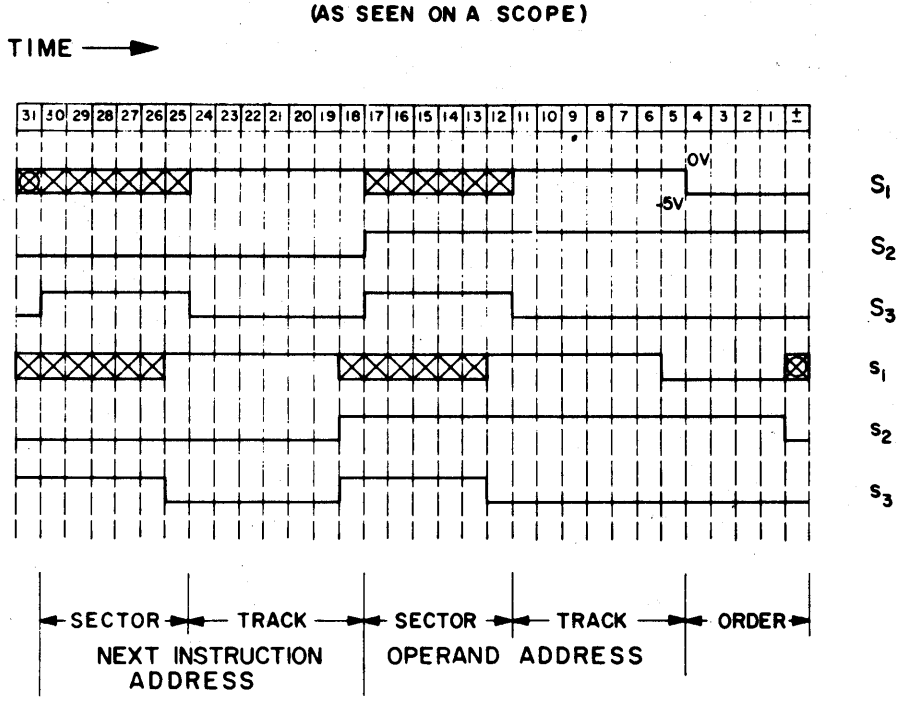
The false side of the clock flip-flop triggers Q4 to drive switch Q5 and generate clock pulse T1. Through a 3 microsecond delay, switch Q6 generates clock pulse T3; clock pulse T5 is generated by another blocking oscillator driven by Q7. Clock pulses T1, T2, T3, and T4 are about one half to one microsecond wide with a rise time, from -5 volts to ground, of one tenth of a microsecond. Clock pulse T5 is 2 microseconds wide and goes from above ground to approximately -5 volts.

Timing tracks S_1, S_2, and S_3 are recorded on the drum and are combined to identify order time, operand address (track and sector), next instruction address (track and sector), and index time (figure 4-13). Track S_1 contains the sector number of every sector as 6 bits of information which occur twice during every word time. Track S_2 is true every word time during next instruction address. Track S_3 is false during both sector times of each word. Bit position 31 in S_1 is true in all sectors whose numbers are divisible by 8 and false in all other sectors. Bit 31 is used to form the t_8 signal.

The read amplifiers used for the timing tracks are the same as those used for the circulating registers described below. The outputs of the read flip-flops in each amplifier are designated s_1, s_2, and s_3. A second flip-flop is driven by the first, one bit time later. The outputs of the second flip-flops are designated S_1, S_2, and S_3. The six flip-flop outputs are logically combined to give the timing signals t_1 through t_8.

4.5.3 Circulating Lines

The circulating lines or registers provide fast temporary storage. Each such line consists of a record head and one or more read heads on the same track of the magnetic drum (figure 4-14). "Circulating" means that the output of a read head is routed to the record head. This causes the contents of the track to be preserved and available for access during each word time.



⊠ SECTOR NUMBER IN BINARY

⊠ TRUE EVERY EIGHTH SECTOR

$t_1 = \underline{S}_2(\underline{S}_1 + \underline{S}_3)$ OPERAND ADDRESS

$t_2 = \underline{S}_1 S_2 S_3 (\underline{s}_2 + s_3)$ NEXT INSTRUCTION TRACK

$t_3 = S_1 S_3 s_3$ ORDER TIME

$t_4 = S_3 s_2 \underline{s}_3$ BIT 31

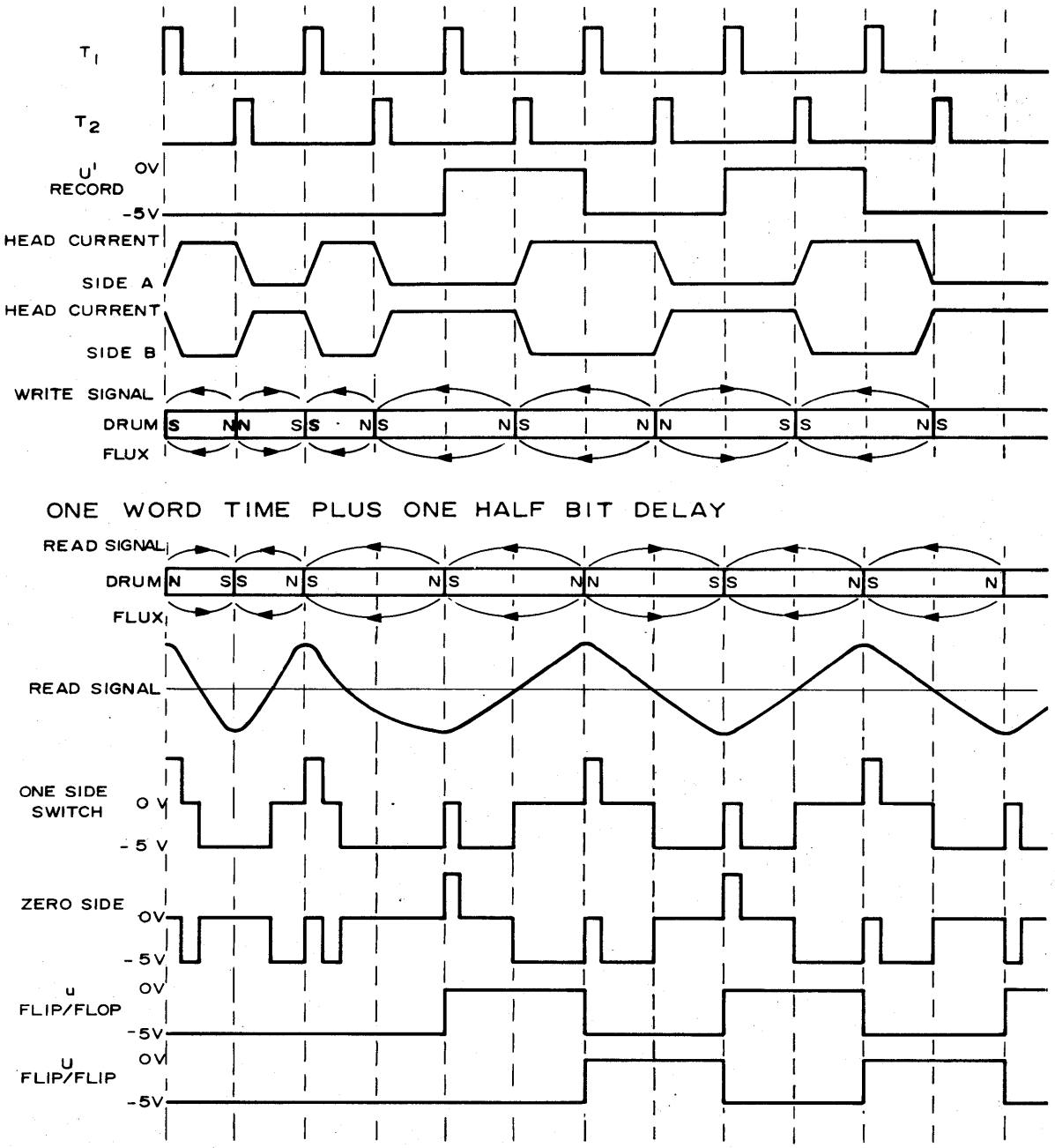
$t_5 = \underline{S}_2 \underline{S}_3$ OPERAND SECTOR

$t_6 = \underline{S}_2 s_2$ SIGN TIME

$t_8 = \underline{S}_2 s_2 s_1 = t_6 s_1$ SIGN TIME WORD 7

FIGURE 4-13 TIMING SIGNALS

The record amplifier drives current through the write head windings to write a one or a zero on the drum. Later the bit is sensed by the read head, the output of which is sent to the read amplifier card. On this card, the read head signal is amplified and clocked into the read flip-flop. The read flip-flop signal, a, is clocked into a second flip-flop, A, which presents the information to the record amplifier through the logic board. The second flip-flop, A, is used in the read circuits of all circulating lines. In order to overcome the delay inherent in this method of recording, information is read into main memory from the output of the read flip-flop of the circulating lines one bit early.



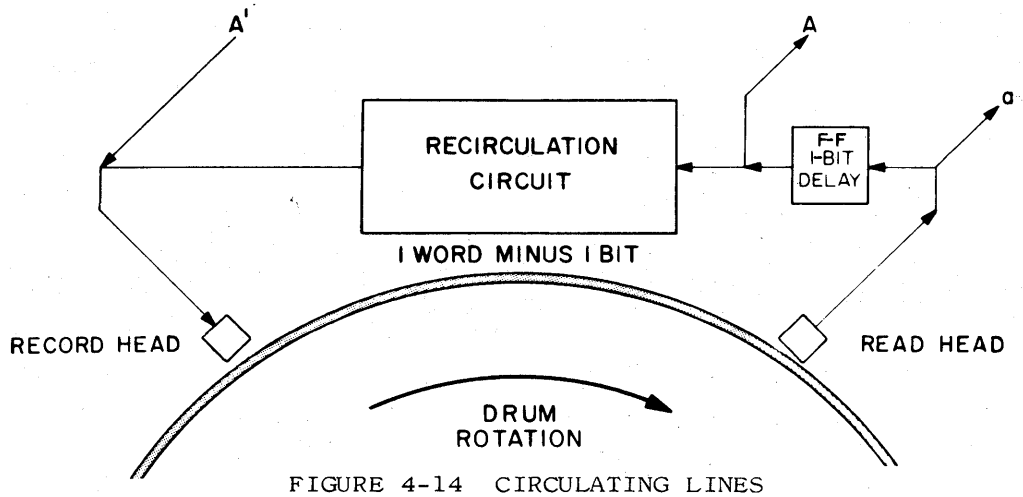


FIGURE 4-14 CIRCULATING LINES

The five registers in the computer are designated as: U, upper accumulator; L, lower accumulator; C, command register; X, index register; and D, Track 127 register.

U is normally one word long. Its function is to hold, receive, or send information to main memory, L or X. During multiply and divide operations, U is extended to two words plus one bit by using the U* read head. This is controlled by the computer logic.

L is normally one word long and its function is to supplement U. During lengthened mode operation, L is extended to eight words by using the L* read head. This is accomplished through program control.

C is a one word register which holds the instruction to be executed. The instruction is composed of the command, operand address, next instruction address, and index bit.

X is a one word register which is used to modify other computer words.

D is an eight word register which is used for fast access in main memory. It is addressed as track 127.

4.5.4 Record Amplifier

Bits to be recorded on the circulating lines enter the record amplifier through Q1 on the record amplifier card (figure 4-15). They are clocked, by clock pulse T_1, into the flip-flop composed of Q4 and Q6. The output of Q1 determines the state of the flip-flop; if negative, Q4 is turned off, or if ground, Q6 is turned off. The flip-flop is complemented by clock pulse T_2. Clock pulse T_2 occurs in the middle of a bit time by gating the inputs of Q4 and Q6 through switches Q2 and Q7. Clock pulse T_2 turns Q4 off if Q7 is negative, and turns Q6 off if Q2 is negative.

The state of the flip-flop determines whether output transistor Q3 or Q5 is conducting. A 200 milliamp current flows through one side of the head to record on the drum. The complementing of the flip-flop causes the recording current to switch to the opposite winding of the record head, producing the phase shift.

4.5.5 Read Amplifier

The output of the read heads is connected to a two stage differential amplifier (figure 4-16). Transistor Q8 drives switch Q5. Transistor Q10 drives switch Q6 to set the flip-flop composed of Q2 and Q3 to "one" or "zero," depending on the phase of the input to the Read Amplifier. The output of this flip-flop is "u" "c" "l" "x" or "d". This output is used to read into main memory. It also sets a second flip-flop one bit time later, producing "U" "C" "L" "X" or "D".

The upper and lower accumulators have a second read head which is located beyond the normal head. These heads are designated as follows: "L*", which allows eight words to be circulated in the lower accumulator, and "U*", which allows two words plus one bit to be circulated in the upper accumulator.

4.5.6 Main Memory

Information to be written in main memory is presented to the V_R' flip-flop (figure 4-17) from "u" or "l" through transistors Q9 and Q3. The infor-

mation is then gated into the flip-flop by T_3. T_4 reverses the state of the flip-flop in the middle of each bit time, providing the necessary Ferranti phase shift.

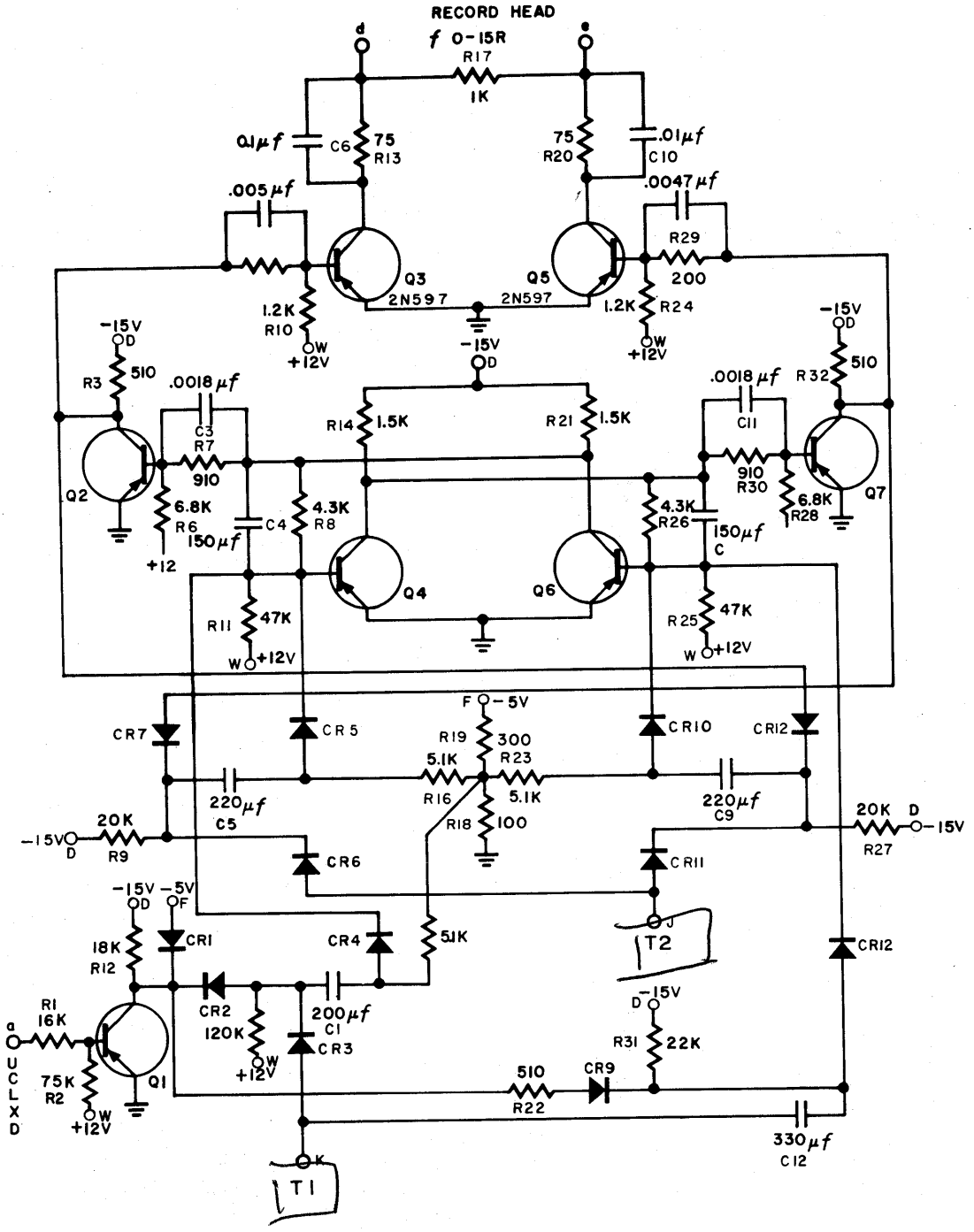


FIGURE 4-15 RECORD AMPLIFIER

The output switches of V_R, viz., Q4 and Q8, are gated by transistors Q2 and Q10, which are controlled by the W flip-flop (figure 4-18). In order to record in main memory, W must be true. The state of W in the logic indicates the

early write period as the selected sector is under the selected main memory head. Transistors Q4 and Q8 are also gated by clock pulse T_5. T_5 stops recording early enough to prevent end record signals at T_1 time.

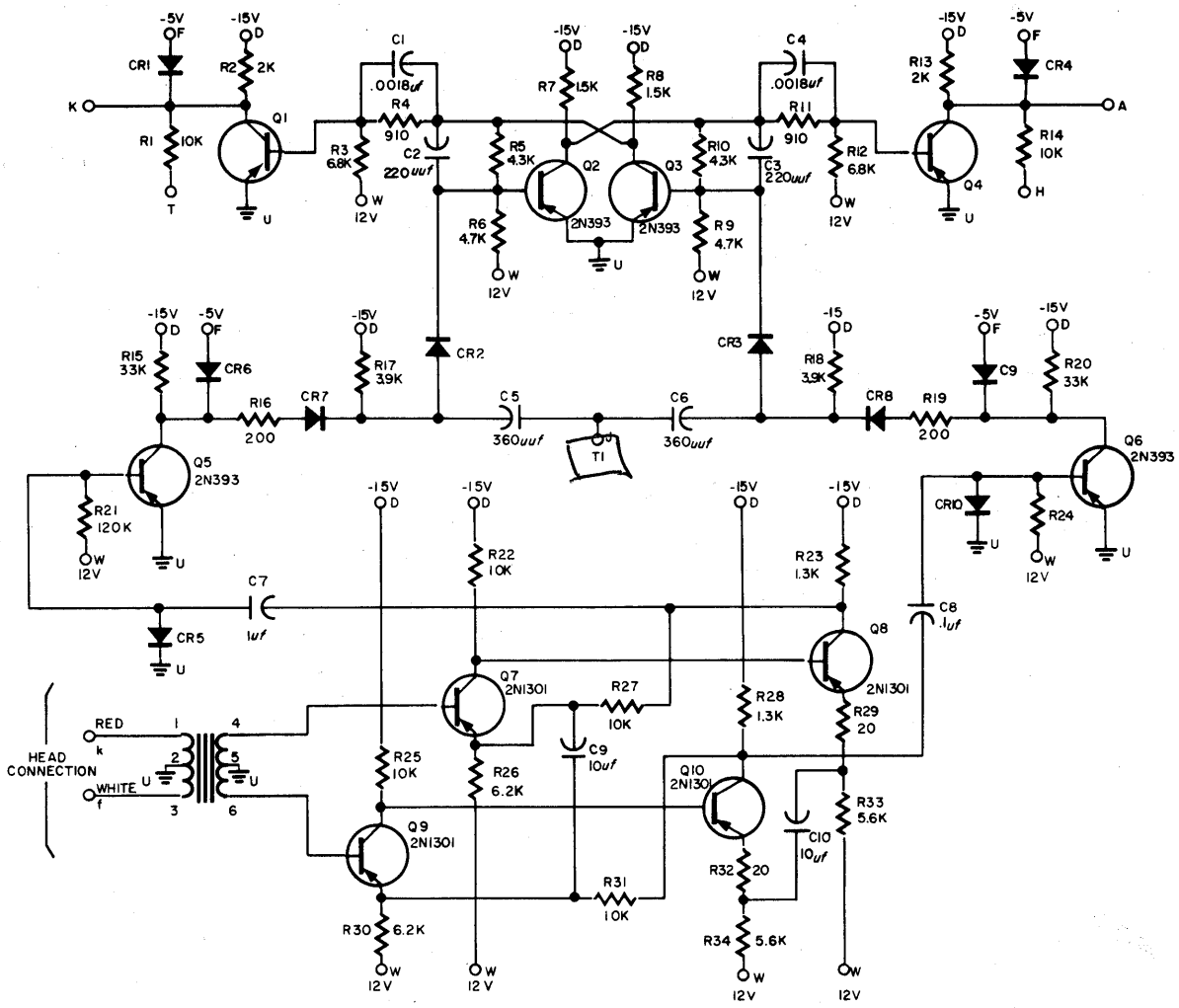


FIGURE 4-16 READ AMPLIFIER

4.5.7 Column Drivers

The output of the V_R flip-flop goes to the column drivers (figure 4-9). Selection of a specific one of the eight columns is determined by eight settings of the P_1, P_2, and P_3 flip-flops, combined through a diode AND gate. Thus, the specific combination of the P flip-flops will select the output, and allow recording in a selected row intersecting the column in the head matrix.

4.5.8 Row Drivers

In order to select the row which designates the heads in a column to be selected for recording, the settings of the P_4, P_5, P_6, and P_7 flip-flops are combined in a transistor AND gate on the row driver card (figure 4-9). For example, each of the P flip-flops controls a transistor. The outputs of the transistors are combined logically to apply a negative voltage to the selected row.

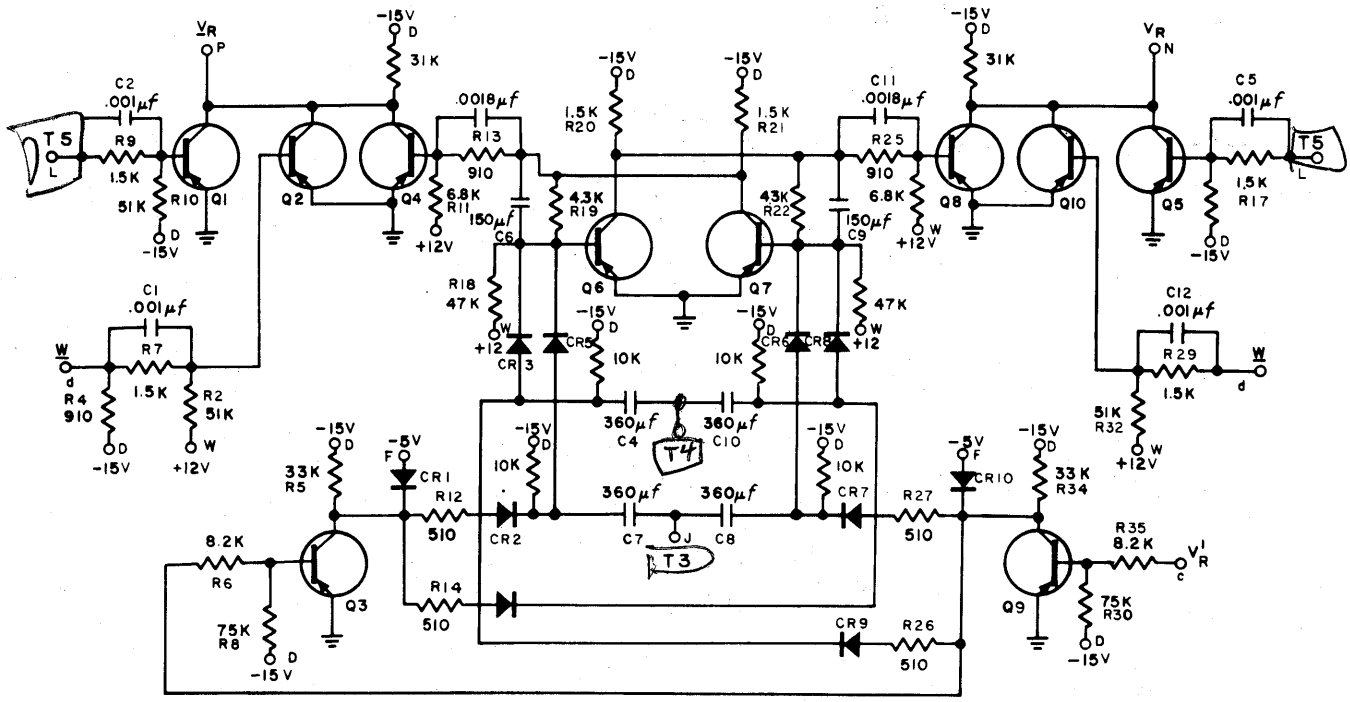


FIGURE 4-17 V_r FLIP-FLOP

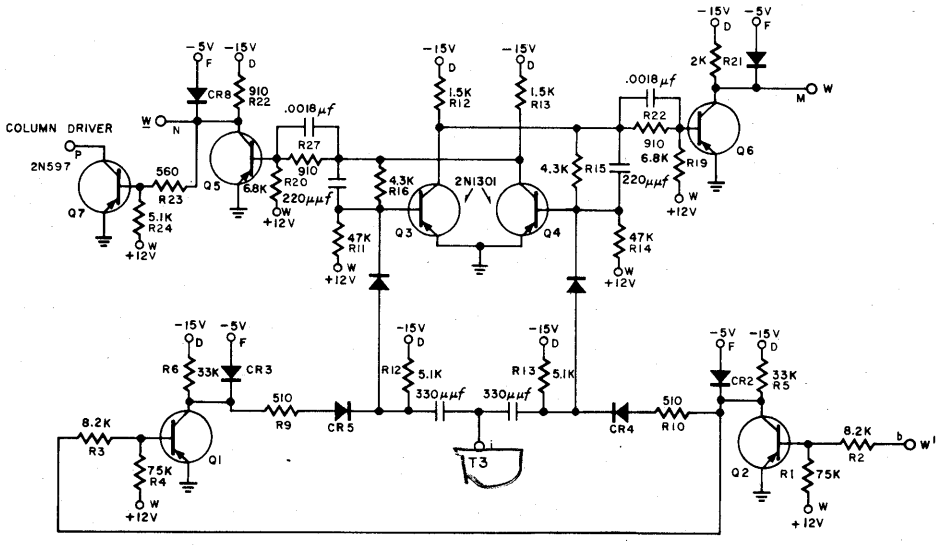


FIGURE 4-18 W FLIP-FLOP

The center taps of eight heads (0, 16, 32, 48, 64, 80, 96, and 112) are driven to -15 volts by the selection of row zero. If column one has been selected by the column driver logic, the outputs of V_R and $\underline{V_R}$ will go to memory heads 16 through 31. At head 16, the V_R or $\underline{V_R}$ signal will allow 200 milliamps to flow through the selected head winding to write on track 16. The W signal will go true and allow V_R or $\underline{V_R}$ to be true only during the selected sector time.

To read from main memory (figure 4-19) the column driver selects a column by combining the P_1, P_2, and P_3 flip-flop outputs. If P_1, P_2, and P_3 are

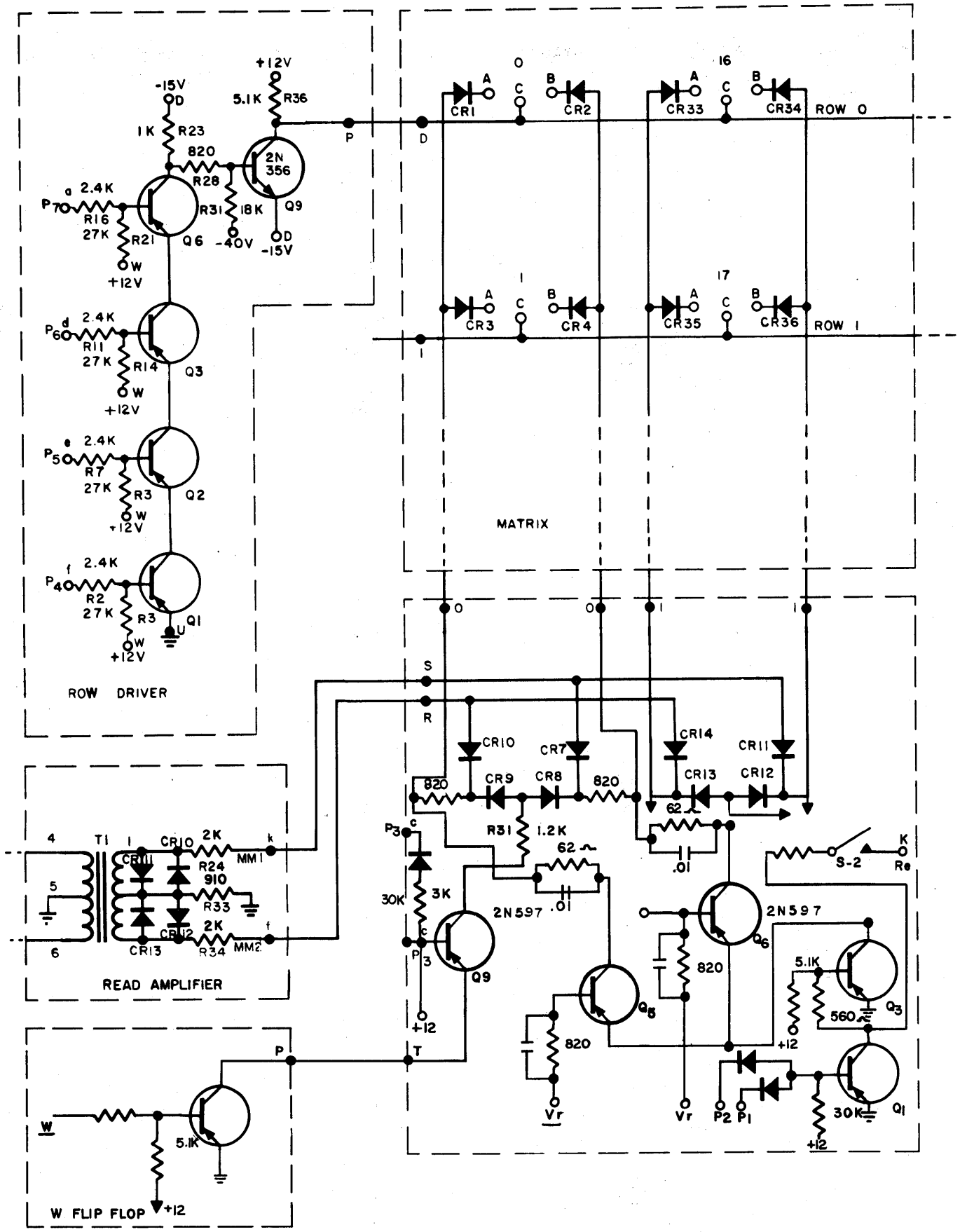


FIGURE 4-19 MAIN MEMORY HEAD SELECTION-READ

false, transistor Q9 is cut off and all the other transistors are conducting. With Q9 cut off, the output of column zero will be read.

The P_4, P_5, P_6, and P_7 flip-flops select a row to be read by applying -15 volts to the center taps of all heads in the row. As in the write process, the matrix selects the one head with a negative voltage on the center tap which intersects the selected column. The output of the selected column driver goes to the main memory read amplifier. Just as with the circulating lines and the clock, the main memory read amplifier is composed of a differential amplifier which drives the read flip-flop, V. Unlike the other two types of read amplifiers, the signal is not repeated through a second flip-flop, but is used directly in the logic.

4.6 Logic Board--The logic equations specifying the conditions necessary to perform various operations in the RPC-4010 Computer are implemented by diode logic gates (figure 4-20) located on the logic board. By combining the logical AND and OR terms, the electronic elements achieve the desired electronic and logical results. The logical product is defined as an AND gate, derived from the fact that for the product of terms to be true, they all must be true. The logical sum is defined as an OR gate, derived from the fact that the sum of the terms is true, if any one is true.

The logical product of signals A and B is developed when both signals are true (-5V). When both signals are true, the top of R-1 is clamped to -5V, and AB is true. If either signal is false (OV), the resistor is grounded, and AB is false (OV).

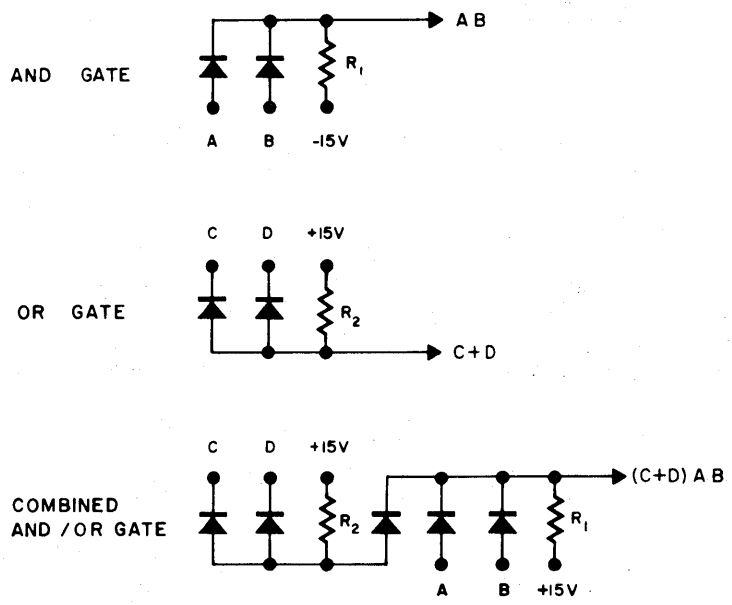


FIGURE 4-20 DIODE LOGIC

The logical sum of signals C and D is developed when either signal is true (-5V). When both signals are false (OV), the resistor is held to ground and the output C+D is false. With either or both signals true, the output is true.

4.7 Flip-Flop--Figure 4-21 is a schematic diagram of the flip-flop used in the RPC-4010. It is actually more than a flip-flop; in addition to the flip-flop itself utilizing two 2N1301 transistors, there are two buffer amplifiers, each using a 2N404 transistor.

The signal called T_1 is the computer clock signal. This is a square pulse which is normally at -5 volts and rises to 0 volts once every 8 microseconds (approximately) and remains at 0 volts for about one microsecond.

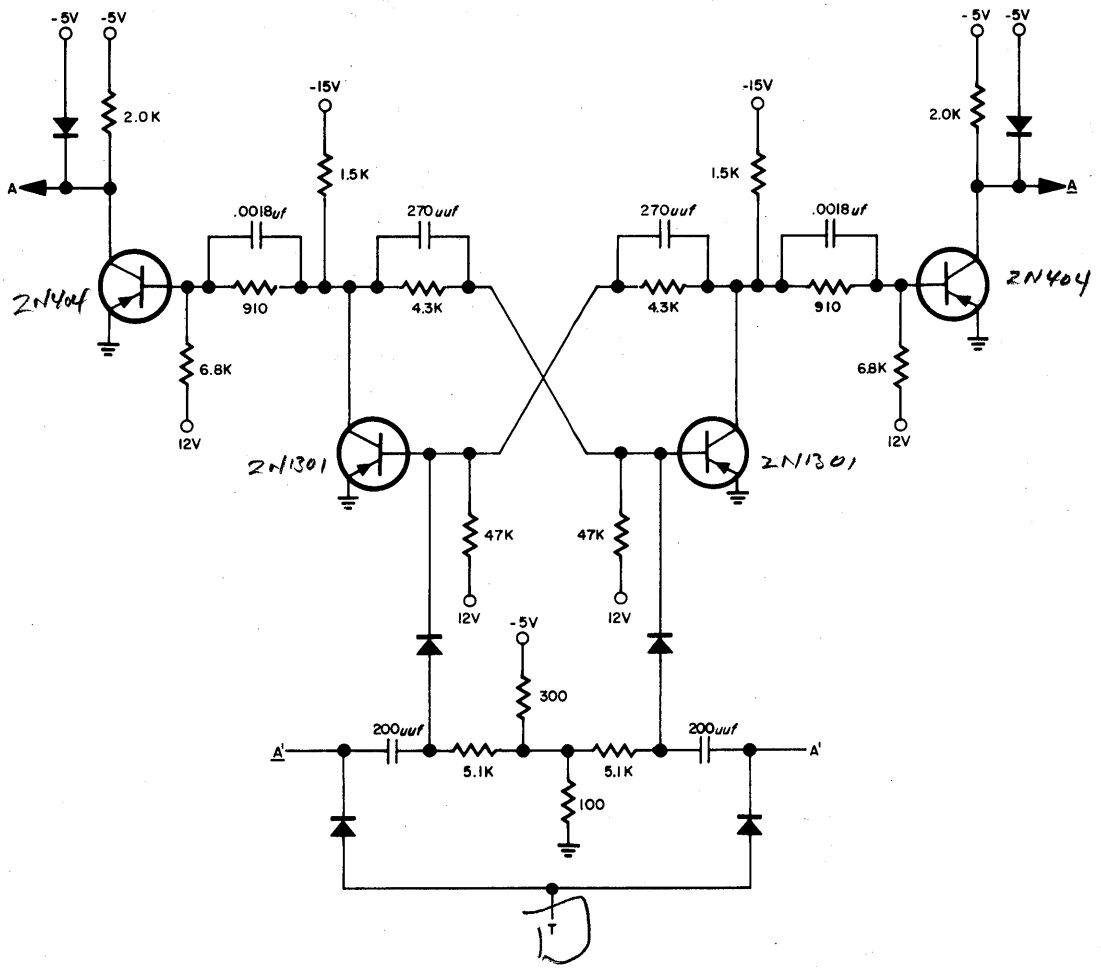


FIGURE 4-21 RPC 4010 FLIP-FLOP

The flip-flop is triggered in this manner: when the 2N1301 on the right is conducting, the 2N1301 on the left is cut off. Likewise, when the 2N404 on the right is conducting, the 2N404 on the left is cut off. Under these conditions, signal A is true and A is false. That is, the flip-flop is off. If A' is at -5 volts, a positive pulse is coupled through the 200 micro-microfarad capacitor and the diode to the base of the 2N1301 transistor on the right. A positive pulse into the base makes this transistor stop conducting. The one on the left begins to conduct, and A becomes true while A becomes false. To state it another way, if A' is true (-5 volts) at clock time, the flip-flop will switch to its true (on) state. If A' is false (0V) at clock time, the flip-flop does not change. Similarly, if A' is true at clock time, the flip-flop will switch to its false state.

The 2,000-ohm load resistor in the collector circuit of the 2N404 buffer amplifier insures a maximum turn-off time of not more than two microseconds. Without biasing, the buffer amplifier can handle sixty milliamperes of AND gate loading, but no OR gate loading. If it is necessary to use the flip-flop signal in OR gates, an additional load resistor must be connected from the flip-flop output to some negative potential. The value of this resistor must be chosen so that it supplies the total OR current required. The amount of AND current which can be supplied is then reduced by the amount of current required by this additional resistor. The minimum value of this additional load resistor is that value which will draw sixty milliamperes. This might be 680 ohms to -40 volts or 270 ohms to -15 volts. If this value is used, the flip-flop can drive no AND gates, only OR gates.

The flip-flop itself changes state in less than 0.5 microsecond, but the 2N404 amplifiers are somewhat slower. Under the worst loading conditions they will change from -5 volts to 0 volts in less than one microsecond, and from 0 volts to -5 volts in less than two microseconds. If the load is non-capacitive, this two-microsecond figure is reduced to about one microsecond.

4.8 Phase Sequencing--Computer operation occurs in phases which are controlled by the phase control flip-flops F, G, and H. The phases are defined as follows:

$\overline{F}\ \overline{G}\ \overline{H}$	Phase 1	Search for next instruction
$\overline{F}\ G\ \overline{H}$	Phase 2	Transfer instruction word from memory to C register
$F\ \overline{G}\ \overline{H}$	Phase 3	Search for data
$F\ G\ \overline{H}$	Phase 4	Execute instruction
$\overline{H}$	Phase 4a	Extended execution

Most instructions do not require an extension of execution, so H is usually off. The logic for proceeding from one phase to a succeeding phase is based on a simple binary counter, the logic for which is:

$$F' = \overline{F}\ G\ \overline{H}$$

$$\overline{F}' = F\ G\ \overline{H}$$

$$G' = \overline{G}\ \overline{H}$$

$$\overline{G}' = G\ \overline{H}$$

It is in this manner that F changes state at the end of phase 2 and 4 and that G changes state at the end of every phase, and H remains false.

The equations above are incomplete because they do not show when to change phase. Al phases change at sign time when timing signal t_6 is true. As described in section 4.5.2 on timing, $t_6 = \overline{S_2}\ s_2$. This signal occurs during only one bit time of each word period and identifies the sign bit, the most significant bit in each word.

The search flip-flop K is on during phase 1 while searching for the next instruction sector, and during phase 3 while searching for the data word. At the end of every word period K is turned on:

$$K' = t_6 + \ldots$$

When the computer enters phase 1, K is on. The logic for turning K off in phase 1 is:

$$\underline{K}' = \underline{F}\ \underline{G}\ \underline{H}\ S_2\ \underline{S_3}\ (S_1\ \underline{C} + \underline{S_1}\ C) + \ldots$$

$\underline{F}\ \underline{G}\ \underline{H}$ indicates phase 1, and $S_2\ \underline{S_3}$ indicates next instruction sector time. This tells us that during phase 1, K can be turned off only during the next instruction sector time. Additionally, $(S_1\ \underline{C} + \underline{S_1}\ C)$ indicates that S_1 must be true while C is false, or S_1 must be false while C is true, to turn K off. That is, K is turned off unless S_1 is identical to C in the next instruction sector.

Now a more complete equation can be written for ending phase 1:

$$G' = \underline{G}\ \underline{H}\ K\ t_6\ (\underline{A}\ Z_i) + \ldots$$

During both the next instruction sector time and operand sector time, S_1 carries the number in binary code of the next sector on the memory drum. If S_1 is identical to C throughout the next instruction sector portion of the command, the desired instruction is located in the following sector of memory. K is turned off during every word time that a mismatch occurs, and remains on only when a match of S_1 and C indicates that the selected next instruction is available during the following word time. Phase 1 is then ended and phase 2 started by turning G on.

During phase 1, while the next instruction sector search is taking place, the instruction track number is copied from C into the P flip-flops. To accomplish this the f_7 signal is generated through diode logic:

$$f_7 = \underline{F}\ \underline{G}\ \underline{H}\ \underline{S_1}\ S_2\ S_3 + \ldots$$

NOTE

Lower case logic signs do not refer to flip-flops or record amplifiers.

The f_7 logic shows that during phase 1 ($\underline{F}\ \underline{G}\ \underline{H}$) and the next instruction track time ($\underline{S_1}\ S_2\ S_3$), f_7 is true. The number is set into the P flip-flops by the following logic:

$$P_1' = f_7\ C + \ldots$$

$$\underline{P_1}' = f_7\ \underline{C} + \ldots$$

$$P_2' = f_7\ P_1 + \ldots$$

$$\underline{P_2}' = f_7\ \underline{P_1} + \ldots$$

and so forth, to

$$P_7' = f_7\ P_6 + \ldots$$

$$\underline{P_7}' = f_7\ \underline{P_6} + \ldots$$

Thus, the next instruction track number is copied bit by bit from the C register into the P flip-flops during phase 1, so that when the sector is found, the head selection matrix has already selected the correct head.

Remainder is transferred via the adder "e₂"

$C' = \underline{F}\,G\,\underline{H}\,(e_2(S_1+S_2+t_4)$ Adder Not Order Time

order portion of the

During phase 2, the instruction is transferred into C.

$$C' = \underline{F}\ G\ \underline{H}\ \left[\underline{b_c}\ V + b_c\ (\underline{NL} + NL^*)\right] S_1 S_2 S_3 \text{ order time}$$

The term $\underline{F}\ G\ \underline{H}$ identifies phase 2. The signal b_c is from the EXECUTE LOWER ACCUMULATOR switch and is false during normal operation, allowing the next instruction to come from memory ($\underline{b_c}\ V$). When in execute lower accumulator mode, the next instruction comes from the lower accumulator $\left[b_c\ (\underline{NL} + NL^*)\right]$.

The five most significant bits of an instruction word contain the command. At the same time that these bits are being transferred into C, during phase 2, the f_8 signal is used to set these bits into the Q flip-flops. The term f_8 is defined as:

Note: Adder inp. to during $\phi 2$ indexing
$I_1' = \underline{H}\,\underline{F}\,MX + 1$, $\phi 2$ Index right OP Adr., $I_2' = \underline{H}\,\underline{F}\,(\underline{b_c}\,V + e_7)$ $\phi 2$ mem EA Lower

$$f_8 = \underline{F}\ G\ \underline{H}\ S_1\ S_3\ s_3$$

$\underline{F}\ G\ \underline{H}$ determines phase 2 and $S_1\ S_3\ s_3$ determines order time. The Q flip-flops are set by:

$$Q_1' = f_8\left[\underline{b_c}\ V + b_c\ (\underline{NL} + NL^*)\right] + \ldots$$

$$\underline{Q_1}' = f_8\left[\underline{b_c}\ \underline{V} + b_c\ (\underline{NL} + \underline{NL^*})\right] + \ldots$$

$$Q_2' = f_8\ Q_1 + \ldots$$

$$\underline{Q_2}' = f_8\ \underline{Q_1} + \ldots$$

and so forth, to

$$Q_5' = f_8\ Q_4 + \ldots$$

$$\underline{Q_5}' = f_8\ \underline{Q_4} + \ldots$$

Phase 2 lasts only one word time. It is ended and phase 3 is entered by:

$$F' = \underline{F}\ G\ \underline{H}\ t_6 + \ldots$$

$$\underline{G}' = \underline{F}\ G\ \underline{H}\ t_6 + \ldots,$$

Phase 2 is identified by $\underline{F}\ G\ \underline{H}$, and the end of word time is identified by t_6.

Phase 3 initiates another sector search, this time for the data word upon which the instruction is to operate. In order to accomplish this, more logic must be added to $\underline{K}'$. K is turned on at the end of every word by:

$$K' = t_6 + \ldots$$

By adding to $\underline{K}'$

$$\underline{K}' = (\underline{F}\ \underline{G}\ \underline{H}\ S_2\ \underline{S_3} + F\ \underline{G}\ \underline{H}\ \underline{S_2}\ \underline{S_3})\ (\underline{S_1}\ C + S_1\ \underline{C}) + \ldots$$

K is turned off in phase 1 ($\underline{F}\ \underline{G}\ \underline{H}$) at next instruction time ($S_2\ \underline{S_3}$) or in phase 3 ($F\ \underline{G}\ \underline{H}$) at data word time ($\underline{S_2}\ \underline{S_3}$) when the search is not successful ($\underline{S_1}\ C + S_1\ \underline{C}$). Reducing the equation to its simplest form results in:

$$\underline{K}' = \underline{G}\ \underline{S_3}\ \underline{H}\ \ (\underline{F}\ S_2 + F\ \underline{S_2})\ (\underline{S_1}\ C + S_1\ \underline{C}) + \ldots$$

Note M flip flop is set on bit 31 $\phi 2$ if X reg set 1 in that position see A1-12.

When C matches the sector being searched for, K will stay on, ending phase 3 by:

$$G' = \underline{G}\ \underline{H}\ K\ t_6 + \ldots$$

The operand track is selected in phase 3 in the same manner as the next instruction track is selected in phase 1— by adding more terms to f_7:

$$f_7 = \underline{G}\ \underline{H}\ \underline{S_1}\ S_3\ (\underline{F}\ S_2 + F\ \underline{S_2}) + \ldots$$

Phase 4 normally (e.g.,ADD) lasts one word time, during which the data word is available as V (the output from memory). The MULTIPLY, DIVIDE, SHIFT, and INPUT instructions make use of phase 4a by setting the H flip-flop true to provide additional execution time. F and G are turned off after one word time of phase 4 by:

$$\underline{F}' = F\ G\ t_6 + \ldots$$

$$\underline{G}' = G\ t_6 + \ldots$$

If H is turned on at this time, phase 4a begins. If H is not turned on, phase 1 begins.

4.9 Execution of Commands--All 32 commands (figure 4-22) used in controlling the operation of the RPC-4010 Computer are described on the following pages.

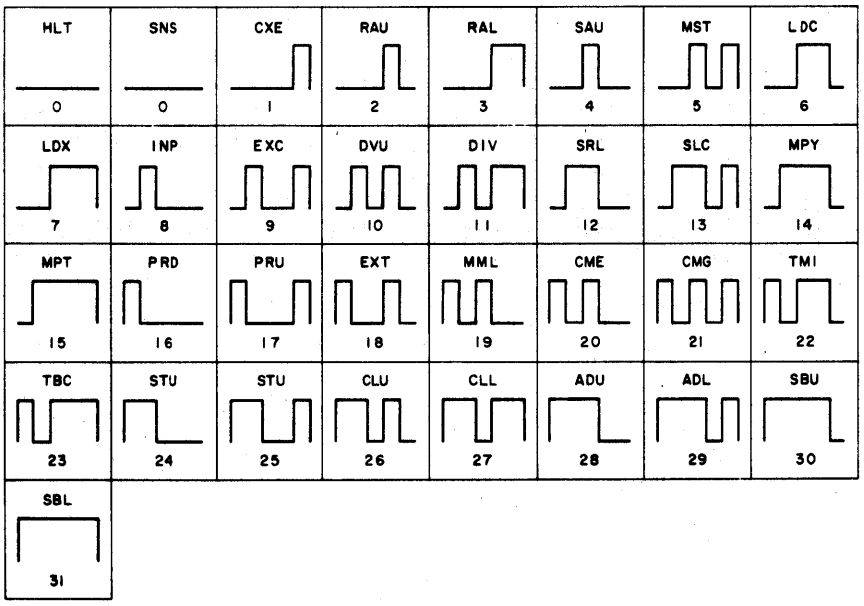


FIGURE 4-22 RPC 4010 COMMAND WAVEFORMS

4.9.1 HALT, 00, HLT (Track 0), $\underline{Q_1}\ \underline{Q_2}\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5}$

Stop in phase 3 and wait for a start signal before proceeding to phase 4.

The 00 command has two functions, and is treated as two separate commands. With data track 0, the 00 command is called HALT (HLT), and its function is to stop the computer. With a non-zero data track, its function is to interrogate the branch switches, and it is called SENSE (SNS). The SENSE command is explained separately in section 4.9.2.

The computer is stopped by not allowing it to proceed from phase 3 to phase 4. The A flip-flop stops the computer by preventing G from going true at the end of phase 1 or phase 3 unless A is false. The G' logic is:

$$G' = Z_i \; K \; \underline{H} \; \underline{A} \; t_6 + \ldots$$

Thus, the computer cannot proceed from phase 3 to phase 4 or from phase 1 to phase 2 unless A is false.

In the one operation mode, the computer stops in phase 3 before executing the instruction in the C register. This is accomplished by turning A on at the sign time of phase 2 when the ONE OPERATION switch is depressed. The A' logic is:

$$A' = \underline{F} \; G \; \underline{H} \; t_6 \; b_o + \ldots$$

The computer remains in phase 3 until a start signal turns A off. The $\underline{A}'$ logic is:

$$\underline{A}' = \underline{G} \; \underline{H} \; b_s + \ldots$$

The b_s signal is obtained when the START COMPUTE switch is depressed or when a start signal is received from input/output. When A is false, G is able to be turned on, and the computer can proceed to phase 4, executing the instruction in C.

In the normal mode, the computer will not stop in phase 3 except on a HALT command because A is turned off at the end of phase 2. The $\underline{A}'$ logic for this is:

$$\underline{A}' = \underline{F} \; G \; \underline{H} \; t_6 \; \underline{b_o} + \ldots$$

In both the normal and one operation modes, the computer will not stop in phase 1 (except during an input command) because A is turned off at the end of phase 4. The $\underline{A}'$ logic in this instance is:

$$\underline{A}' = t_6 \; F \; G \; \underline{H} \; (Q_1 + \underline{Q_2} + Q_3 + Q_4 + Q_5) + \ldots$$

The Q terms turn A off for every command except the input command.

When the computer is turned on initially, it is possible for the computer to be in either phase 1 or phase 3. To make sure that the computer is in phase 3, F is turned on when the ONE OPERATION switch is latched and the SET INPUT switch is depressed.

$$F' = b_q + \ldots$$

The HLT command is executed by turning A on during the command time of phase 3. This prevents the computer from going into phase 4. The A' logic is:

$$A' = \underline{Q_1} \; \underline{Q_2} \; \underline{Q_3} \; \underline{Q_4} \; \underline{Q_5} \; \underline{M} \; F \; \underline{G} \; t_3 + \ldots$$

The $\underline{M}$ term differentiates between the HLT and SNS commands. If M is true, the SENSE command is present and A will not be turned on.

The M flip-flop is turned off at the end of phase 2 by:

$$\underline{M}' = \underline{F}\ \underline{H}\ t_6 + \ldots$$

It can be turned on in phase 3 by:

$$M' = F\ \underline{G}\ \underline{H}\ \underline{S_1}\ \underline{S_2}\ S_3\ \underline{Q_2}\ C + \ldots$$

The factor $\underline{S_1}\ \underline{S_2}\ S_3$ defines data track time. If the command is OO, M is turned on only if C goes true during data track time, that is. if the data track is non-zero. $\underline{Q_2}$ prevents M from turning on during data track time with the INPUT command. Thus, M is turned on in phase 3 and remains on during phase 4 for all cases where Q_2 is false except command OO, track O.

To proceed after a HLT command has been executed, the START COMPUTE switch is depressed, making b_s true. With b_s true, A is turned off and M is turned on so that the computer can proceed to phase 4.

The $\underline{A}'$ logic is: $\underline{A}' = \underline{G}\ \underline{H}\ b_s + \ldots$

The M' logic is: $M' = b_s\ \underline{Q_2}\ \underline{G} + \ldots$

If M were not turned on, the computer would remain in phase 3 because A would be continually turned on by the $\underline{Q_1}\ \underline{Q_2}\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5}$ M F $\underline{G}\ t_3$ term.

If the HLT command is index modified a non-zero track number may result, converting it into a SENSE command (OO, track non-zero).

4.9.2 SENSE, OO, SNS, $\underline{Q_1}\ \underline{Q_2}\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5}$

Turn on B (the branch control flip-flop) if for any branch switch which is depressed, the corresponding data track bit contains a "1". There is no branch switch that corresponds to the 64's data track bit. Turn B on if the 64's data track bit contains a "1" and one of the following conditions exists:

1. No input device is selected.

2. A selected input or output device is not ready.

Turn B off if none of the above conditions is true.

B is unconditionally turned off in the last word period of phase 3 by:

$$\underline{B}' = K\ F\ \underline{G}\ t_6\ Z_i\ \underline{A}\ (\underline{Q_1}\ \underline{Q_2}\ \underline{Q_3}\ \underline{Q_4})\ (P_1 + k_{23} + P_2 + P_3 + P_4 + P_5 + P_6) + \ldots$$

As explained under HALT, A is false at the end of phase 3 except for the HALT and INPUT commands. $\underline{A}$ in this equation prevents turning B off for a HALT command, or when the computer is in the one operation mode. This enables the computer operator to determine whether any previously executed commands turned B on by observing the RESET light on the control panel. The P_{1-6} and k_{23} terms prevent B from being turned off after a HALT if B was on as a result of previously executed commands. In one operation mode, phase 3 of SNS, B is turned off by pressing the START COMPUTE switch because one or more of the P flip-flops will be true.

B is then turned on in phase 4 only if the below stated conditions are met.

$$B' = F\ G\ t_6\ \underline{Q_1}\ \underline{Q_2}\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5}\ (P_1\ \underline{Z_q} + P_2\ b_2 + P_3\ b_3 + P_4\ b_4 + P_5\ b_5 + P_6\ b_6 + P_7\ b_7) + \ldots$$

Z_q is a synchronism signal from input/output. $\underline{Z_q}$ is true only if an input device is selected and, in addition, all selected input and output devices are ready. For example, Z_q will be false if the photo-reader is selected and searching.

The branch switch symbols and their corresponding track bits are shown in the following table:

Track Bit	64	32	16	8	4	2	1
Branch Switch	None	b_2	b_3	b_4	b_5	b_6	b_7
P Flip-Flop	P_1	P_2	P_3	P_4	P_5	P_6	P_7

4.9.3 COMPARE X EQUAL, 01, CXE, $\underline{Q_1}\ \underline{Q_2}\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5}$

Turn B OFF if ON, then compare the data address in the instruction with the data address in the index register. If they are equal, turn B ON.

B is turned off at the end of phase 3 by:

$$\underline{B}' = K\ F\ \underline{G}\ t_6\ Z_i\ \underline{A}\ \ \underline{Q_1}\ \underline{Q_2}\ \underline{Q_3}\ \underline{Q_4}\ (Q_5 + \ldots) + \ldots$$

The carry flip-flop, A, is used to record the results of the comparison. As explained earlier, A is always false upon entering phase 4. In phase 4, A is turned on if any bit of the index register is not the same as the corresponding bit of the command register during data address time. If A is still off at sign time of phase 4, this indicates that X and C were found to have equal data addresses.

$$A' = F\ G\ \underline{H}\ t_1\ \underline{Q_2}\ \underline{Q_3}\ (X\ \underline{C} + \underline{X}\ C)\ \underline{S_2}\ (\underline{S_1} + \underline{S_3}) + \ldots$$

$\underline{S_2}\ (\underline{S_1} + \underline{S_3})$ defines data address time. $\underline{Q_2}\ \underline{Q_3}$ defines eight commands altogether, of which the state of A has meaning only for the CXE command.

If A is off at sign time of phase 4, B is turned on by:

$$B' = F\ G\ t_6\ \underline{Q_1}\ \underline{Q_2}\ \underline{Q_3}\ \underline{Q_4}\ Q_5\ \underline{A}$$

4.9.4 RESET AND ADD TO UPPER, 02, RAU, $\underline{Q_1}\ \underline{Q_2}\ \underline{Q_3}\ Q_4\ \underline{Q_5}$

Replace the contents of U with the contents of the memory location specified by the data address.

The contents of U are circulated during phases 1, 2, and 3 by:

$$U' = U\ \underline{H}\ (\underline{F} + \underline{G})$$

During phase 4, V (memory) is read into U by:

$$U' = F\ G\ \underline{H}\ \underline{Q_1}\ \underline{Q_2}\ \underline{Q_3}\ Q_4\ \underline{Q_5}\ V$$

Thus, during phase 4, the 02 command reads the contents of memory into U.

4.9.5 RESET AND ADD TO LOWER, 03, RAL, $\underline{Q_1}\ \underline{Q_2}\ \underline{Q_3}\ Q_4\ Q_5$

Replace the contents of L with the contents of the memory location specified by the data address.

The contents of L are circulated during phases 1, 2, and 3 by:

$$L' = (\underline{N}\ L + N\ L^*)\ \underline{H}\ (\underline{F} + \underline{G})$$

The term $\underline{N}\ L + N\ L^*$ indicates that the lower accumulator is in either normal or lengthened mode.

During phase 4, V is read into L by:

$$L' = F\ G\ \underline{H}\ \underline{Q_1}\ \underline{Q_2}\ \underline{Q_3}\ Q_4\ Q_5\ V$$

Thus, during phase 4, the 03 command reads the contents of memory into L.

4.9.6 STORE ADDRESS FROM UPPER, 04, SAU, $\underline{Q_1}\ \underline{Q_2}\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5}$

Store the data address portion of U into the memory location specified by the data address portion of the instruction.

In order to record in memory, W must be true. For SAU, W is true during early data address time of phase 4:

$$W' = \underline{Q_1}\ \underline{Q_2}\ Q_3\ \underline{Q_4}\ \underline{Q_5}\ \underline{s_2}\ (\underline{s_1} + \underline{s_3})\ F\ G$$

Early data address time is defined by $\underline{s_2}\ (\underline{s_1} + \underline{s_3})$ which begins and ends one bit before data address time. The early signal is necessary for recording in memory as explained in the section on Ferranti recording. The signal which is recorded while W is true is:

$$V' = \underline{Q_5}\ u + \ldots$$

The u signal is the upper accumulator, occurring one bit early. Thus, the SAU command records the data address portion of U in memory.

4.9.7 MASKED STORE, 05, MST, $\underline{Q_1}\ \underline{Q_2}\ Q_3\ \underline{Q_4}\ Q_5$

Store L into the memory location specified by the data address portion of the instruction where U contains 1's. Where U contains 0's, leave the memory location unaltered.

Recording is allowed all during early phase 4 whenever u contains "1" by:

$$W' = (F\ G\ \underline{t_6} + F\ \underline{G}\ K\ t_6)\ \underline{Q_1}\ \underline{Q_2}\ Q_3\ \underline{Q_4}\ Q_5\ u + \ldots$$

The term $F\ G\ \underline{t_6} + F\ \underline{G}\ K\ t_6$ identifies early phase 4, u specifies the time early U has 1's. The signal which is recorded during this time is:

$$V' = Q_5\ (\underline{N}\ 1 + N\ 1^*)$$

Thus, the 05 command records L into memory where U contains 1's. Where U contains 0's, nothing is recorded, and the original content of memory is undisturbed.

4.9.8 LOAD COUNT AND REPEAT, 06, LDC, $\underline{Q_1}\ \underline{Q_2}\ Q_3\ Q_4\ \underline{Q_5}$

Replace the contents of the instruction track portion of the X register with the repeat count (n), which comes from the next instruction track portion of the addressed word in memory. Place the computer in repeat mode. The instruction following LOAD COUNT AND REPEAT will have its phase 4 executed n + 1 times. The operands of the instruction will be the consecutive memory locations specified by (n), beginning with the operand address in the instruction word. Each time phase 4 is repeated, the instruction track portion of X is diminished by 1. Phase 4 ends when the Repeat Count reaches 0. This leaves all 1's in the instruction track portion of X, and the computer is then taken out of repeat mode.

The repeat count is loaded into the X register from memory in phase 4 of the repeat command by:

$$X' = F\ G\ \underline{Q_1}\ \underline{Q_2}\ Q_3\ Q_4\ \underline{Q_5}\ \underline{S_1}\ S_2\ S_3\ V + \ldots$$

The computer is in repeat mode when R, the repeat flip-flop is on. R is turned on in phase 4 of the REPEAT command by:

$$R' = F\ G\ t_6\ \underline{Q_1}\ \underline{Q_2}\ Q_3\ Q_4\ \underline{Q_5}$$

The logic for ending phase 4 is:

$$\underline{G}' = G\ \underline{H}\ t_6\ (\underline{R} + \underline{Q_1}\ \underline{Q_2}\ Q_3\ Q_4\ \underline{Q_5}) + \ldots$$

$$\underline{F}' = F\ G\ t_6\ (\underline{R} + \underline{Q_1}\ \underline{Q_2}\ Q_3\ Q_4\ \underline{Q_5}) + \ldots$$

For each word time of a repeated phase 4, the repeat count in X is reduced by 1. The logic which accomplishes this is:

$$X' = F\ G\ (Q_1 + Q_2 + \underline{Q_3} + \underline{Q_4} + Q_5)\ \underline{S_1}\ S_2\ S_3$$
$$\left[\underline{R}\ X + R\ (K\ \underline{X} + \underline{K}\ X)\right] + \ldots$$

The term $(Q_1 + Q_2 + \underline{Q_3} + \underline{Q_4} + Q_5)$ allows the subtraction of a binary 1 from X to occur each phase 4 of every repeated command except the REPEAT command itself. K is turned ON at sign time of phase 4 by:

$$K' = t_6\ G + \ldots$$

To subtract 1 from a binary number, successively replace the least significant 0's with 1's, and replace the first 1 encountered with a 0, and leave the remaining bits unchanged.

The function of K is to indicate whether a one has been encountered or not. K is turned on by the logic above, and remains on for all least significant 0's. K is turned off when the least significant 1 is encountered by:

$$\underline{K}' = F\ G\ \underline{H}\ \underline{S_1}\ S_2\ S_3\ X + \ldots$$

K is on at sign time of phase 3 and upon entering phase 4 for all commands except INPUT. K is always off when entering phase 4 of INPUT, thus, the first word of repeated phase 4 in input is not counted.

The term $R\ (\underline{K}\ X + K\ \underline{X})$ in the X' logic replaces the least significant 0's with 1's, and the first 1 encountered with 0, since K is on for these cases. After a 1 is encountered, K is turned off at the following clock time, and X is

circulated without change.

When the repeat count portion of X is zero, the subtraction process leaves K on and all 1's in the repeat count. With K on at data address time, R is turned off by:

$$\underline{R}' = F\ G\ t_1\ K$$

With R turned off at data address time, phase 4 is ended by the F and G logic above.

When phase 4 ends, the computer goes into phase 4a or phase 1.

4.9.9 LOAD X, 07, $\underline{Q_1}\ \underline{Q_2}\ Q_3\ Q_4\ Q_5$

Replace the data address portion of the index register with the data address portion of the instruction word.

The command register obtains the instruction word from memory during phase 2. During phase 4, the operand address is copied into the index register by:

$$X' = F\ G\ \underline{Q_1}\ \underline{Q_2}\ Q_3\ Q_4\ Q_5\ (\underline{S_1} + \underline{S_3})\ \underline{S_2}\ C + \ldots$$

The term $(\underline{S_1} + \underline{S_3})\ \underline{S_2}$ defines data address time. The LOAD X command may be index modified to become add to index.

4.9.10 INPUT, 08, INP, $\underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5}$

Send a signal calling for an input to an input/output unit. Stop in phase 1 until a character is presented from input/output. When a character is presented, go directly from phase 1 to phase 3, then 4, then 4a, entering the character into the least significant character position of L. Go into phase 1 and wait for a new character. Repeat this cycling for each character entered until a START COMPUTE signal is received. The computer then goes on to the next instruction. If the data track address has 0 in the 64's place, accept only the least significant four bits of each character. If the data track address has 1 in the 64's place, accept all six bits of the character presented. If L is one word long, read into the double accumulator, composed of U and L. If L is eight words long, read into L.

This is the only instruction which cycles through the phases repeatedly while executing a single instruction. In the first cycle all four phases occur in the normal manner, beginning with phase 1, wherein the input instruction is located in memory as the next instruction, through phase 4. Phase 4 is followed by one word time of phase 4a. In phases 4 and 4a of this first cycle, the signal Y_i is sent to input/output which calls for input. The input information is entered during the following cycles, one character per cycle.

Flip-flop M is used to distinguish between the first cycle and the other cycles. During the first cycle M remains off, but beginning with the second cycle, M is turned on in phase 3. M is always turned off in phase 1 and 2 by:

$$\underline{M}' = \underline{F}\ \underline{H}\ t_6 + \ldots$$

M is turned on in phase 3 for the INPUT command only if Z_b, a signal for input/output, is true.

$$M' = F\ \underline{G}\ t_6\ Z_b\ Q_2 + \ldots$$

Z_b is true only while a character is being presented to the computer for input. Z_b is never true during the first cycle, since input/output has not yet been informed that an input is desired, hence no character is being presented for input. Therefore, M remains off in the first cycle.

During the first cycle, the logic for ending phase 3 is:

$$G' = F\ \underline{G}\ \underline{H}\ t_6\ Z_i\ \underline{A}\ \left[\underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5}\ (\underline{N} + t_8)\right] + \ldots$$

Z_i is a signal from input/output which is normally true when Z_b is false. A was set false in phase 2 if the computer was not in the one operation mode. In the first phase 3 of an INPUT command, Z_i is true. When L is eight words long, defined by N, phase 3 of the first cycle lasts until the next t_8 pulse occurs. This causes phase 4 to begin with a word time whose sector address modulo 8 is zero.

In all cycles of INPUT, phase 4 is followed by phase 4a:

$$H' = F\ G\ \underline{H}\ t_6\ \underline{Q_1}\ Q_2\ \underline{Q_5}\ \underline{R} + \ldots$$

In phases 4 and 4a of the first cycle, a signal, Y_i, is sent to input/output calling for an input:

$$Y_i = (F\ G + H)\ \underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5}\ \underline{M}$$

Input/output responds to this, either by starting a selected reader or indicating by a light that typewriter input is expected.

Phase 4a is always followed by phase 1 as has been explained elsewhere. Phase 4a lasts one word time if L is one word long. If L is eight words long, phase 4a ends with the next t_8 pulse.

$$\underline{H}' = H\ t_6\ \underline{Q_3}\ \underline{Q_4}\ (\underline{N} + t_8) + \ldots$$

Thus, normally (when phase 4 is not repeated), phases 4 and 4a together have a duration of two word times when L is one word long. They last eight word times, beginning and ending with t_8, when L is 8 words long. During phase 4 and 4a of the first cycle, if L is one word long, U and L are connected as a two word circulating line.

$$U' = k_1\ \underline{N}\ \underline{M}\ L + \ldots$$

$$L' = k_1\ \underline{N}\ U + \ldots$$

$$k_1 = (F\ G + H)\ \underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5}$$

If L is eight words long during phases 4 and 4a of the first cycle, U is circulated on itself and L is circulated as an eight word line:

$$U' = k_1\ N\ U + \ldots$$

$$L' = k_1\ N\ \underline{M}\ L^* + \ldots$$

Phase 1 cannot end in the normal way, i.e., when the search for next instruction is successful, so long as A is true.

$$G' = \underline{G}\ t_6\ Z_i\ K\ \underline{A}\ \underline{H} + \ldots$$

A will be true because it is always turned on in phase 4a of the input order by:

$$A' = k_1 + \ldots$$

Therefore, the computer remains in phase 1 until the action started by sending Y_i in phases 4 and 4a, results in the presentation of a character for input. When a character is presented, Z_b becomes true and the computer proceeds directly from phase 1 to phase 3 by:

$$F' = \underline{F}\ \underline{H}\ t_6\ Z_b\ \underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5} + \ldots$$

skipping phase 2. Then A,which is still on after the computer skips phase 1, must be reset so that the computer can proceed to phase 4. This is accomplished by turning A off with an input order during phase 3:

$$\underline{A}' = F\ \underline{G}\ M\ \underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5} + \ldots$$

The M term allows A to be reset for every phase 3 of an input order except the first. This is to prevent having to step through the input of every character in the one operation mode, or on the other hand, failing to stop in one operation mode before the execution of an input order.

The input instruction word is retained in the command register and the input order is retained in the Q flip-flops until a start signal b_s is received instead of a new character. The start signal turns A off when in phase 1, thus permitting phase 1 to be followed by phase 2.

$$\underline{A}' = b_s\ \underline{G}\ \underline{H} + \ldots$$

In Section 4.8, Phase Sequencing, it is explained how the track number is shifted from the C register into the P flip-flops during phases 1 and 3. This shifting occurs only when f_7 is true.

$$f_7 = (\underline{M} + \underline{Q_2})\ (\underline{F}\ \underline{G}\ \underline{H}\ \underline{S_1}\ S_2\ S_3 + F\ \underline{G}\ \underline{H}\ \underline{S_1}\ \underline{S_2}\ S_3)$$

During the first word time of phase 3, M is false and shifting occurs. At the end of the first word time of phase 3, M is turned on if Z_b is true.

$$M' = F\ \underline{G}\ t_6\ Z_b\ Q_2 + \ldots$$

In every cycle except the first, Z_b must be true to enter phase 3, and since Z_b remains true for more than 1 word time, M always goes true at the end of the first word time of every cycle except the first.

Since both M and Q_2 are true after the first word period of phase 3, f_7 is false and shifting into the P flip-flops cannot occur in phase 3 after the first word period. Instead, the P flip-flops are set by the B flip-flops in input/output.

$$P_2' = k_{39}\ B_6$$

$$P_3' = k_{39}\ B_5$$

$$P_4' = k_{39}\ B_4$$

$$P_5' = k_{39}\ B_3$$

$$P_6' = k_{39}\ B_2$$

$$P_7' = k_{39}\ B_1$$

$$k_{39} = F\ \underline{G}\ M\ \underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5}$$

If the data track number is non-zero, some of the P flip-flops will be true as a result of shifting the data track number into them. No provision is made to set the P flip-flops false, therefore, they can be a true copy of the B flip-flops only if the track number is 0 or 64. The P_2 through P_7 flip-flops will be off at the end of the first word time of phase 3 when M goes true; then after the B flip-flops are copied in by the above logic, a P flip-flop will be true only if its contributing B flip-flop is true. But if any P flip-flop is already true as a result of the operand track number, it remains true even if the contributing B flip-flop is false.

The setting of P_1 is not affected at all by the B flip-flops, and it holds the state which it obtained from the operand track number.

Phase 3 continues so long as Z_b remains true. When Z_b goes false, Z_i becomes true and permits the computer to enter phase 4 by:

$$G' = F\ \underline{G}\ \underline{H}\ t_6\ Z_i\ \underline{A}\ \underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5}\ (\underline{N} + t_8) + \ldots$$

If N is false (L is 1 word long), phase 4 begins at the end of the next sign time. If N is true (L is 8 words long), phase 4 cannot begin until t_8 is true.

In phases 4 and 4a, if L is 1 word long, L and U are coupled as a two word line, and the character that was set into the P flip-flops in phase 3 is shifted into the two word accumulator, in the least significant character position of the L line. If P_1 is true (track number more than 64), the full, 6-bit character enters the accumulator thus:

$$P_2' = k_1\ (\underline{N}\ L + N\ L^*) + \ldots \qquad \underline{P_2}' = k_1\ (\underline{N}\ \underline{L} + N\ \underline{L^*}) + \ldots$$

$$P_3' = k_1\ P_2 + \ldots \qquad \underline{P_3}' = k_1\ \underline{P_2} + \ldots$$

$$P_4' = k_1\ P_1\ P_3 \qquad \underline{P_4}' = k_1\ P_1\ \underline{P_3}$$

$$P_5' = k_1\ P_4 + \ldots \qquad \underline{P_5}' = k_1\ \underline{P_4} + \ldots$$

$$P_6' = k_1\ P_5 + \ldots \qquad \underline{P_6}' = k_1\ \underline{P_5} + \ldots$$

$$P_7' = k_1\ P_6 + \ldots \qquad \underline{P_7}' = k_1\ \underline{P_6} + \ldots$$

$$U' = k_1\ \underline{N}\ (\underline{M}\ L + M\ P_7) + \ldots$$

$$L' = k_1\ \underline{N}\ U + \ldots$$

During phases 4 and 4a of the first cycle of INPUT defined by $k_1\ \underline{M}$, U and L are connected as a two word circulating line, as the above logic shows. During phases 4 and 4a of the remaining cycles, when M is on, the input to U is from the 6-bit shift register composed of the 6 P flip-flops P_2-P_7. The input to this shift register is from L, and the input to L is from U. This makes a delay line that is two words plus 6 bits long. The character that is just about to enter the two word line (i.e., the character in the P flip-flops) at the beginning of phase 4 must be just about to leave the two-word line (i.e., in the least significant character position of L) two word times later, at the end of phase 4a. Any characters which were located in the 2 word line at the beginning of phase 4 have been shifted left one character position at the end of phase 4a, due to the fact that they undergo a delay of 6 bits in the P flip-flops.

During phase 1 and phase 3, each accumulator is independently circulated, so that it retains all characters in their positions until the next phase 4.

$$U' = U\ \underline{H}\ (\underline{F} + \underline{G}) + \ldots$$

$$L' = \underline{N}\ L\ \underline{H}\ (\underline{F} + \underline{G}) + \ldots$$

If P_1 is false, P_4 does not receive its input from P_3 but from L.

$$P_4' = k_1\ \underline{P_1}\ (\underline{N}\ L + N\ L^*) + \ldots$$

$$\underline{P_4}' = k_1\ \underline{P_1}\ (\underline{N}\ \underline{L} + N\ \underline{L^*}) + \ldots$$

Then only the least significant four bits of each character enter the two-word accumulator, and the characters already present in the accumulator at the beginning of phase 4 are shifted left only 4 bits.

When N is true, P_2 and P_4 receive their inputs from L*

$$P_2' = k_1\ (\underline{N}\ L + N\ L^*)$$

$$\underline{P_2}' = k_1\ (\underline{N}\ \underline{L} + N\ \underline{L^*})$$

$$P_4' = k_1\ P_1\ P_3 + k_1\ \underline{P_1}\ (\underline{N}\ L + N\ L^*)$$

$$\underline{P_4}' = k_1\ P_1\ \underline{P_3} + k_1\ \underline{P_1}\ (\underline{N}\ \underline{L} + N\ L^*)$$

L receives its input directly from P_7 when N is true, and U is circulated independently.

$$L' = k_1\ \underline{N}\ U + k_1\ N\ (\underline{M}\ L^* + M\ P_7)$$

$$U' = k_1\ \underline{N}\ (\underline{M}\ L + M\ P_7) + k_1\ N\ U$$

Thus, when L is an eight word line, characters are set into the eight word accumulator, L, in the same way that they are set into the two word accumulator when L is a one word line. When M is false (i.e., during phases 4 and 4a of the first cycle) L* is circulated on itself.

An indefinite number of characters can be entered in this fashion. If the number of characters entered exceeds the capacity of the two-word accumulator in the non-lengthened mode, information is shifted into the P flip-flops in phase 4 and destroyed in phase 1 when the P flip-flops receive the track number.

The process may be ended during any phase 1 by depressing the START COMPUTE switch, or by receiving a stop code from input/output. In either case, Z_b does not go true, but instead b_s goes true, setting A false, as explained above.

4.9.11 EXCHANGE, 09, EXC, $\underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ Q_5$

Perform any non-conflicting combinations of the operations described below. The desired combinations are selected by the data track number.

Data track 1 true--(P_7)

Replace the contents of L with U

Data track 2 true--(P_6)

Replace the contents of U with L

Data track 4 true--(P_5)

Replace the contents of X with U

Data track 8 true--(P_4)

Replace the contents of U with X

Data track 16 true--(P_3)

Set L to 8 word length

Data track 32 true--(P_2)

Set L to 1 word length

Data tracks 16 and 32 true--(P_2, P_3)

Set L to opposite state

The contents of L are replaced with U by:

$$L' = F\ G\ \underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ Q_5\ P_7\ U + (\underline{N}\ L + N\ L^*)\ \underline{H}\ \underline{Q_1}\ Q_2\ \underline{Q_4}\ Q_5\ \underline{P_7} + \ldots$$

Data track 1 is indicated by P_7. The second term permits normal circulation of L if P_7 is false.

The contents of U are replaced with L or X by:

$$U' = F\ G\ \underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ Q_5\ (P_6\ L + P_4\ X) + \underline{H}\ \underline{Q_4}\ Q_5\ \underline{P_4}\ \underline{P_6}\ U$$

Data track 2 is indicated by P_6, and data track 8 is indicated by P_4. If both P_4 and P_6 are true, the resulting word in U is the logical "OR" of the words in L and X. The second term permits normal circulation of U if P_4 and P_6 are both false.

The contents of X are replaced with the contents of U by:

$$X' = F\ G\ \underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ Q_5\ P_5\ \underline{R}\ U + (\underline{P_5} + R)\ X + \ldots$$

Data track 4 is indicated by P_5. The logic is written so that R (Repeat) must be false before the index register may be altered in order to prevent a dynamic halt on a repeated EXCHANGE command. The index register contains the repeat count. If this could be altered, phase 4 might never end. If the EXCHANGE command with data track 4 true is repeated, it becomes a do-nothing command. If R is true or P_5 is false, X is circulated normally.

The length of L is changed by:

$$N' = \underline{N}\ F\ G\ t_6\ \underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ Q_5\ P_3 + \ldots$$

$$\underline{N}' = N\ F\ G\ t_6\ \underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ Q_5\ P_2 + \ldots$$

Data tracks 16 and 32 are indicated by P_3 and P_2 respectively. When N is true,

L is 8 words long; when N is false, L is 1 word long. If P_3 and P_2 are both true, N changes from its present state to the opposite state.

4.9.12 DIVIDE UPPER, 10, DVU, $\underline{Q_1}\ Q_2\ \underline{Q_3}\ Q_4\ \underline{Q_5}$

Divide the contents of U by the contents of the memory location specified by the data address. Leave the quotient in U and the remainder in L.

The procedure for division is a non-restoring system in which each step brings the partial remainder (U) toward zero by subtracting or adding the divisor (L) as their signs agree or disagree.

The divisor is copied into L from the memory location specified by the data address during phase 4 (word period 1) by:

$$L' = F\ G\ \underline{H}\ V\ \underline{Q_1}\ Q_2\ \underline{Q_3}\ Q_4 + \ldots$$

At sign time of word period 1, the sign of the divisor sets P_6 by:

$$P_6' = F\ G\ \underline{H}\ t_6\ Q_4\ \underline{R}\ V + \ldots$$

$$\underline{P_6}' = F\ G\ \underline{H}\ t_6\ Q_4\ \underline{R}\ \underline{V} + \ldots$$

This sign is carried by P_6 throughout the execution of the DIVIDE command. The sign of the dividend sets P_7 during sign time of word period by:

$$P_7' = F\ G\ \underline{H}\ t_6\ Q_4\ \underline{R}\ U + \ldots$$

$$\underline{P_7}' = F\ G\ \underline{H}\ t_6\ Q_4\ \underline{R}\ \underline{U} + \ldots$$

On subsequent odd word periods, P_7 is set by the sign of the new remainder (U) by:

$$P_7' = H\ P_1\ t_6\ \underline{Q_3}\ Q_4\ U + \ldots$$

$$\underline{P_7}' = H\ P_1\ t_6\ \underline{Q_3}\ Q_4\ \underline{U} + \ldots$$

During each pair of word periods the sign of the remainder becomes the least significant bit of the quotient and the remainder is shifted one digit position.

Odd and even word periods are designated by the state of P_1. The initial setting of P_1 occurs during word period 1, by:

$$\underline{P_1}' = F\ G\ \underline{H}\ t_6\ \underline{R}\ Q_4 + \ldots$$

P_1 is set false at sign time of word period 3. P_1 remains false throughout word period 4 to indicate an even word period. Thus P_1 acts as a two position counter:

$$P_1' = H\ \underline{P_1}\ t_6\ Q_4 + \ldots$$

$$\underline{P_1}' = H\ P_1\ t_6\ Q_4 + \ldots$$

Word period 1 is identified by F G $\underline{H}$; word periods 2 and 3 are identified by $\underline{F}$ $\underline{G}$ H; word periods 4 through 64 are identified by F $\underline{G}$ H; word period 65 is identified by F G H; and word periods 66 and 67 are identified by $\underline{F}$ G H.

Addition or subtraction of U and L takes place during even word periods according to the S signal. If the sign of U is the same as the sign of L, S is true and L is subtracted from U.

$$S = H\ \underline{Q_3}\ (F + \underline{G})\ (P_6\ P_7 + \underline{P_6}\ \underline{P_7}) + \ldots$$

To carry out the addition or subtraction U and L are presented as I_1 and I_2 during even word periods by:

$$I_1' = H\ \underline{Q_3}\ (\underline{F}\ \ \underline{P_1}\ u^* + F\ U^*) + \ldots$$

$$I_2' = H\ \underline{Q_3}\ \underline{P_1}\ (\underline{F}\ P_7 + \underline{G})\ e_{11} + \ldots$$

The result is the signal e_2, which is derived from:

$$e_2 = A\ I_1\ I_2 + A\ \underline{I_1}\ \underline{I_2} + \underline{A}\ \underline{I_1}\ I_2 + \underline{A}\ I_1\ \underline{I_2}$$

The result, e_2 is then copied into U by:

$$U' = e_2\ H\ Q_4\ \underline{Q_3} + \ldots$$

This process continues until word period 64, subtracting L from U, shifting U one bit position, and inserting the quotient in the unused portion of U.

By the end of the 64th word period, sector coincidence occurs. However, three more word periods are required to complete the division process. The 64th word period is identified by:

$$K' = t_6\ Q_4 + \ldots$$

$$\underline{K}' = \underline{G}\ \underline{S_3}\ H\ Q_4\ \underline{S_2}\ (S_1\ \underline{C} + \underline{S_1}\ C) + \ldots$$

In turn, K turns G on by:

$$G' = \underline{G}\ t_6\ H\ K\ F$$

During word period 66, the remainder is available, but possibly needs restoration from the previous subtraction (or addition) which occurred in word period 64. This restoration is indicated by the last quotient digit developed, which also controls the state of P_7. Hence P_7 is used to gate the divisor into I_2 during word period 66:

$$I_1 = H\ \underline{F}\ \underline{Q_3}\ \underline{P_1}\ u^*$$

$$I_2 = H\ \underline{P_1}\ (\underline{N}\ L + N\ L^*)\ (\underline{F}\ \underline{Q_3}\ P_7) + \ldots$$

The sign of the divisor, indicated by P_6, determines whether the restoration requires an addition or subtraction.

$$S = H\ \underline{F}\ G\ P_6 + \ldots$$

The output of the adder, e_2, is then the correct remainder and is read into L, which has been holding the divisor up to this time:

$$L = G\ e_2\ \underline{P_1}\ H\ Q_4 + \ldots$$

During word period 67 the full quotient is available in either its true or its complemented form and is copied into U by:

$$U' = G\ e_2\ \underline{F}\ H\ Q_4 + \ldots$$

$$I_1 = H\ \underline{F}\ \underline{Q_3}\ P_1\ P_6\ U^* + H\ \underline{F}\ \underline{Q_3}\ G\ P_1\ \underline{P_6}\ \underline{U^*}$$

Because of the system of division used, the determining factor of whether the quotient is complemented or not is the sign of the divisor. If the sign is positive, the quotient will be complemented in word period 67 by the above I_1 logic.

If the divisor is negative, the quotient must be corrected by adding one in the least significant digit.

$$S = H\ \underline{F}\ G\ P_6 + \ldots$$

$$I_2 = H\ \underline{F}\ G\ P_1\ P_6\ \underline{Q_3} + \ldots$$

The simplified word periods for division are given in table 4-1.

Table 4-1

RPC-4010 COMPUTER-

DIVISION TIMETABLE

WORD PERIOD	F	G	H	P_1	U'	L'	I_1	I_2	S
1 (Ph 4)	1	1	0	-	#	V	-	-	-
2 (Ph 4a)	0	0	1	0	e_2	L	u*	L	$P_6P_7+\underline{P_6}\underline{P_7}$
3 (Ph 4a)	0	0	1	1	e_2	L	U*	0	$P_6P_7+\underline{P_6}\underline{P_7}$
4--62 (even WP)	1	0	1	0	e_2	L	U*	L	$P_6P_7+\underline{P_6}\underline{P_7}$
5--63 (odd WP)	1	0	1	1	e_2	L	U*	0	$P_6P_7+\underline{P_6}\underline{P_7}$
64 (K on)	1	0	1	0	e_2	L	U*	L	$P_6P_7+\underline{P_6}\underline{P_7}$
65	1	1	1	1	e_2	L	U*	0	$P_6P_7+\underline{P_6}\underline{P_7}$
66	0	1	1	0	e_2	e_2	u*	P_7 L	P_6
67	0	1	1	1	e_2	L	P_6 U* $+P_6$ $\underline{U^*}$	P_6	P_6

\# This signal is 0 for single length division (DVU) and L for double length division (DIV).

NOTE: $P_6' = F\ G\ H\ t_6\ V$ (Sign of divisor)

$P_7' = F\ G\ H\ P_1\ t_6\ U$ (Dividend digits)

4.9.13 DIVIDE, 11, DIV, $\underline{Q_1}\ Q_2\ \underline{Q_3}\ Q_4\ Q_5$

Divide the contents of U and L (double length format) by the contents of the memory location specified by the data address.

The procedure for double length division is identical to that of single length, with the exception that during word period 1, the previous contents of L are copied into U at the same time the divisor is copied from the memory location specified by the data address into L by:

$$U' = F\ G\ \underline{H}\ \underline{Q_1}\ Q_2\ \underline{Q_3}\ Q_4\ Q_5\ L$$

The remainder of this operation is identical to DIVIDE SINGLE LENGTH. The exception of copying L into U is noted in table 4-1.

4.9.14 SHIFT RIGHT OR LEFT, 12, SRL, $\underline{Q_1}\ Q_2\ \underline{Q_3}\ Q_4\ \underline{Q_5}$

Shift the contents of the double length accumulator (combined upper and lower) to the right if the least significant data track bit is zero; or shift the contents to the left if the least significant data track bit is one. The number of bit positions shifted is dependent upon the number in the data address sector. Turn on branch control if overflow occurs during shift left.

Since there is no operand to search for in a shift command, phase 3 is ended after one word period by:

$$G' = G\ t_6\ \underline{Q_1}\ Q_2\ Q_3\ \underline{Q_4} + \ldots$$

Phase 4 lasts one word period and is identified as word period 1 of the execution of the shift command. Word period 1 and word period 2 are identical for both the SHIFT RIGHT and the SHIFT LEFT command. Word periods are defined by the states of signals indicated on the "Shift and Normalize Timing Chart" (figure 4-23). During word period 1, U is circulated by:

$$U' = \underline{H}\ \underline{Q_1}\ Q_3\ \underline{Q_4}\ U + \ldots$$

Phase 4 (word period 1) is ended after one word period by:

$$H' = F\ G\ \underline{H}\ t_6\ \underline{R}\ \underline{Q_1}\ Q_2\ Q_3\ \underline{Q_4} + \ldots$$

The state of P_1 is indeterminate until the end of phase 4, at which time it is turned off by:

$$\underline{P_1}' = F\ G\ \underline{H}\ t_6\ \underline{R}\ Q_3 + \ldots$$

Thus, P_1 is off during phase 4a, word period 2. At the end of word period 2, P_1 is turned on by:

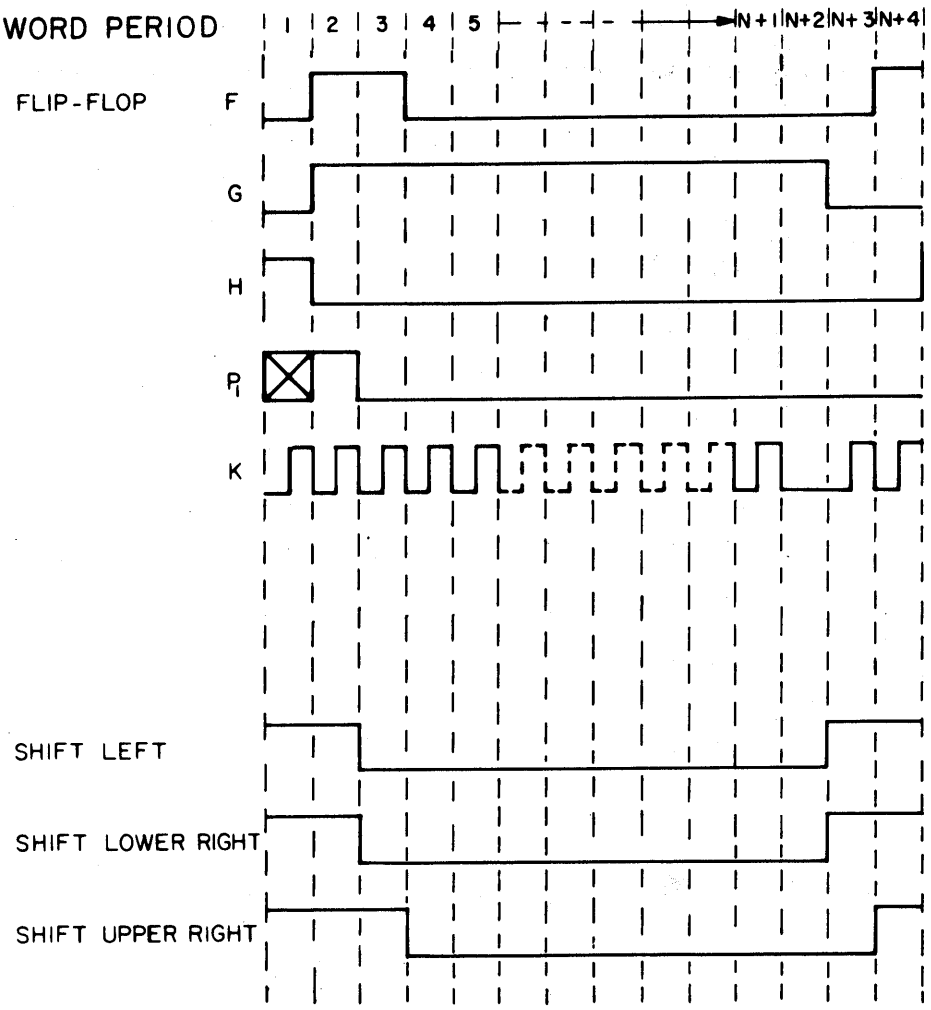
$$P_1' = H\ \underline{P_1}\ t_6\ \underline{Q_3} + \ldots$$

For the remainder of the shift command P_1 is true.

As is done for all instructions, F and G are turned off at the end of phase 4 (word period 1) by:

$$\underline{F}' = F\ G\ \underline{R}\ t_6 + \ldots$$

$$\underline{G}' = G\ \underline{H}\ \underline{R}\ t_6 + \ldots$$



NOTE: N EQUALS NUMBER OF BIT POSITIONS TO BE SHIFTED

FIGURE 4-23 SHIFT AND NORMALIZE TIMING CHART

At the end of word period 3, F is turned on by:

$$F' = \underline{F}\ \underline{G}\ H\ P_1\ Q_3\ t_6 + \ldots$$

For both SHIFT RIGHT and SHIFT LEFT commands, during word period 1 U is circulated by:

$$U' = \underline{H}\ \underline{Q_1}\ Q_3\ \underline{Q_4}\ U + \ldots$$

Also, during word period 1, L is circulated by:

$$L' = \underline{H}\ \underline{Q_1}\ Q_2\ Q_3\ \underline{Q_4}\ L + \ldots$$

During word period 2, except for sign time (H $\underline{R}$ t_6), U and L are circulated and the P flip-flops set by:

$$U' = H\ \underline{P_1}\ Q_3\ \underline{Q_4}\ \underline{Q_5}\ U + \ldots$$

$$L' = H\ \underline{P_1}\ Q_3\ \underline{Q_4}\ \underline{Q_5}\ L + \ldots$$

$$P_3' = H\ \underline{P_1}\ \underline{t_6}\ Q_3\ U + \ldots$$

$$\underline{P_3}' = H\ \underline{P_1}\ \underline{t_6}\ Q_3\ \underline{U} + \ldots$$

$$P_4' = H\ \underline{t_6}\ Q_3\ P_3 + \ldots$$

$$\underline{P_4}' = H\ \underline{t_6}\ Q_3\ \underline{P_3} + \ldots$$

$$P_5' = H\ \underline{t_6}\ Q_3\ P_4 + \ldots$$

$$\underline{P_5}' = \underline{t_6} + \ldots$$

The P_3, P_4, and P_5 flip-flops are tested every sign time for overflow. During a SHIFT LEFT command, the B flip-flop is turned on to indicate an overflow by:

$$B' = \underline{G}\ H\ \underline{K}\ P_7\ Q_3\ \underline{Q_4}\ \underline{Q_5}\ t_6 \left[\underline{P_3}\ P_4 + P_3\ \underline{P_4} + P_3\ P_4\ \underline{P_5}\ (\underline{N}\ \underline{L} + N\ \underline{L^*})\right] + \ldots$$

During word period 2, U and L are circulated by:

$$U' = H\ Q_3\ \underline{Q_4}\ U\ \underline{F}\ \underline{P_1}\ (Q_5 + P_7)$$

$$L' = H\ Q_3\ \underline{Q_4}\ \underline{Q_5}\ \underline{F}\ \underline{P_1}\ (\underline{N}\ L + N\ L^*)$$

Flip-flops P_2 and P_4 are turned off by:

$$\underline{P_2}' = Q_3\ H\ t_6 + \ldots$$

$$\underline{P_4}' = Q_3\ H\ t_6 + \ldots$$

And the P_3 flip-flop is set with the sign bit of L by:

$$P_3' = H\ \underline{P_1}\ t_6\ Q_3\ (\underline{N}\ L + N\ L^*) + \ldots$$

$$\underline{P_3}' = H\ \underline{P_1}\ t_6\ Q_3\ (\underline{N}\ \underline{L} + N\ \underline{L^*}) + \ldots$$

At t_6 time a test is made for overflow or zero shift during word period 3 and the following word periods of the SHIFT LEFT command (figure 4-24). U is delayed one bit each word period through flip-flop P_3:

$$P_3' = H\ P_1\ \underline{t_6}\ Q_3\ U + \ldots$$

$$\underline{P_3}' = H\ P_1\ \underline{t_6}\ Q_3\ \underline{U} + \ldots$$

$$U' = \underline{G}\ H\ P_1\ P_7\ Q_3\ \underline{Q_4}\ P_3 + \ldots$$

The P_4 and P_5 flip-flops are set by:

$$P_4' = H\ \underline{t_6}\ Q_3\ P_3 + \ldots$$

$$\underline{P_4}' = H\ \underline{t_6}\ Q_3\ \underline{P_3} + \ldots$$

$$P_5' = H\ \underline{t_6}\ Q_3\ P_4 + \ldots$$

Note that P_5 can be turned on by P_4, but cannot be turned off. P_5 will be reset each t_6 time by:

$$\underline{P_5}' = H\ Q_3\ t_6$$

The one bit shift for each word period is accomplished in L by shifting through P_2:

$$P_2' = H\ \underline{t_6}\ Q_3\ L + \ldots$$

$$\underline{P_2}' = H\ \underline{t_6}\ Q_3\ \underline{L} + \ldots$$

$$L' = \underline{G}\ H\ P_1\ P_7\ Q_3\ \underline{Q_4}\ P_2 + \ldots$$

At sign time the most significant bit in U is shifted out and lost. The second most significant bit from L sets P_3:

$$P_3' = H\ P_1\ t_6\ Q_3\ P_2 + \ldots$$

$$\underline{P_3}' = H\ P_1\ t_6\ Q_3\ \underline{P_2} + \ldots$$

and becomes the least significant bit of U in the next word period by:

$$U' = \underline{G}\ H\ P_1\ P_7\ Q_3\ \underline{Q_4}\ P_3 + \ldots$$

Flip-flops P_2 and P_4 are set to zero each sign time by:

$$\underline{P_2}' = H\ t_6\ Q_3 + \ldots$$

$$\underline{P_4}' = H\ t_6\ Q_3 + \ldots$$

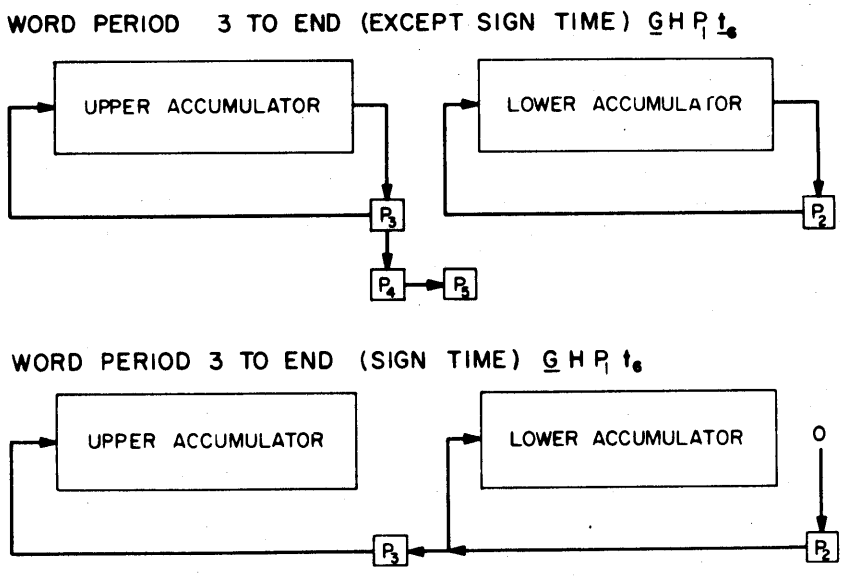


FIGURE 4-24 SHIFT LEFT-W/P 3 TO END

The zero set into P_2 goes into the least significant bit position of L by:

$$L' = \underline{G}\ H\ P_1\ P_7\ Q_3\ \underline{Q}_4\ P_2 + \ldots$$

The above operation is repeated to shift the contents of the combined U and L accumulators one bit to the left each word period.

At each word period of phase 4a, the data sector portion of C is reduced by one through the use of K as a carry on complement control.

$$C' = H\ Q_3\ \underline{Q}_4\ \underline{S}_2\ \underline{S}_3\ (C\ K + \underline{C}\ K) + \ldots$$

Every t_6 time K is turned on by:

$$K' = t_6\ Q_3 + \ldots$$

And is turned off by the first "1" in the data sector of C:

$$\underline{K}' = H\ Q_3\ \underline{Q}_4\ P_1\ \underline{Q}_5\ C + \ldots$$

When the shift count is reduced to zero after the designated number of bits have been shifted, K remains on through sign time and turns G on by:

$$G' = \underline{G}\ t_6\ H\ K\ F + \ldots$$

With G on, shifting stops and F is turned off at the next word period.

$$\underline{F}' = F\ t_6\ G\ H$$

H is turned off during the following word period by:

$$\underline{H}' = H\ t_6\ \underline{F}\ G\ P_1$$

A shift command ends at this word period when G is turned off by:

$$\underline{G}' = G\ t_6\ \underline{F}\ P_1$$

4.9.15 SHIFT RIGHT (word period 3 to end)

During word period 3 of the SHIFT RIGHT command (figure 4-25), U is circulated.

The one-bit shift is accomplished in L by circulating L one bit early:

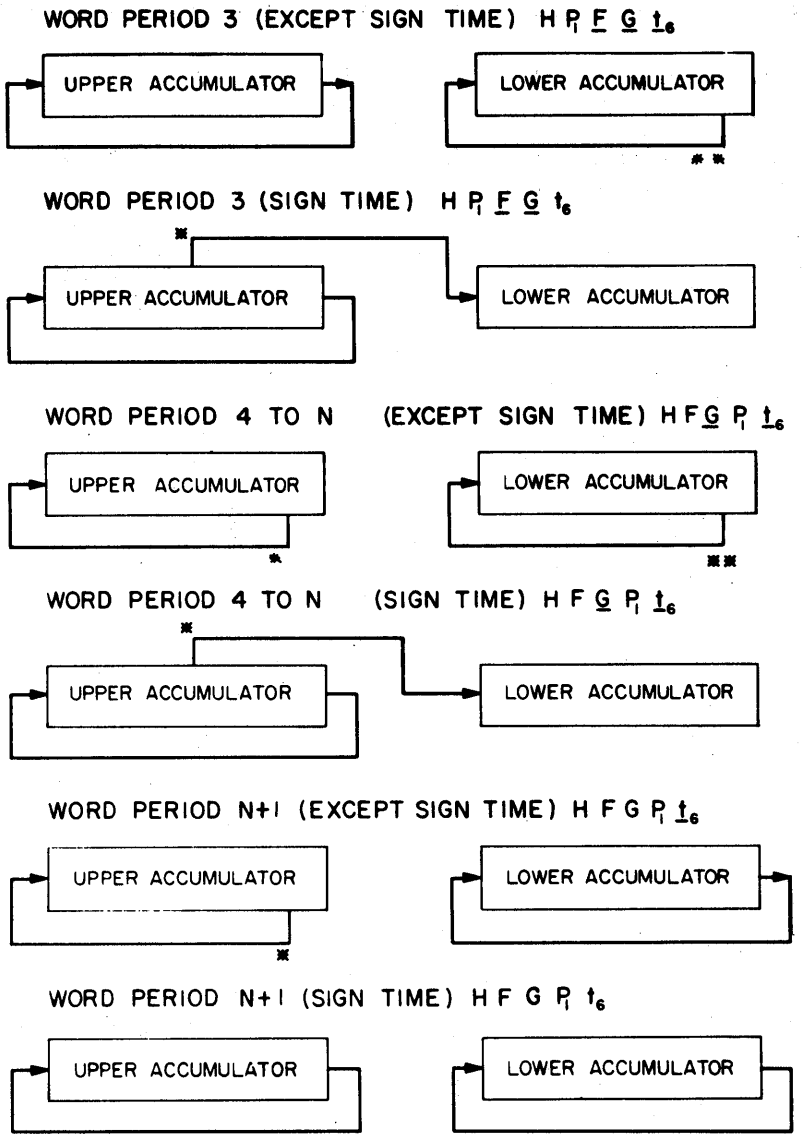
$$L' = H\ Q_3\ \underline{Q}_4\ \underline{Q}_5\ \underline{P}_7\ P_1\ \underline{G}\ 1\ \underline{t}_6 + \ldots$$

During word period 3, U is circulated by:

$$U' = H\ Q_3\ \underline{Q}_4\ \underline{Q}_5\ \underline{P}_7\ \underline{F}\ U + \ldots$$

The least significant bit of L is lost in each shift, and the least significant bit of U is entered into the most significant bit position of L by:

$$L' = H\ Q_3\ \underline{Q}_4\ \underline{Q}_5\ \underline{P}_7\ P_1\ \underline{G}\ \ t_6\ u\ + \ldots$$



NOTE: * U 1 BIT EARLY
** L 1 BIT EARLY

FIGURE 4-25 SHIFT RIGHT-W/P 3 TO END

During word periods 4 through n (where n equals the number of bits to be shifted) U is copied one bit early:

$$U' = H\ Q_3\ \underline{Q}_4\ \underline{Q}_5\ \underline{P}_7\ F\ \ \underline{t}_6\ u + \ldots$$

Again L is circulated one bit early by:

$$L' = H\ Q_3\ \underline{Q}_4\ \underline{Q}_5\ \underline{P}_7\ F\ \ \underline{G}\ \ t_6\ l\ \ + \ldots$$

During sign time of word periods 4 through n, the sign of U is repeated to give an algebraic shift:

$$U' = H\ Q_3\ \underline{Q}_4\ \underline{Q}_5\ \underline{P}_7\ t_6\ U + \ldots$$

The least significant bit of L is lost and the least significant bit of U is copied into the most significant bit position of L during sign time.

$$L' = H\ Q_3\ \underline{Q}_4\ \underline{Q}_5\ \underline{P}_7\ F\ \underline{G}\ t_6\ u + \ldots$$

During word period n + 1, when SHIFT RIGHT is completed, U is circulated one bit early, except sign time:

$$U' = H\ Q_3\ \underline{Q}_4\ \underline{Q}_5\ \underline{P}_7\ F\ \ \underline{t}_6\ u + \ldots$$

And L is circulated by:

$$L' = H\ Q_3\ \underline{Q}_4\ \underline{Q}_5\ G\ (\underline{N}\ L + N\ L^*) + \ldots$$

During sign time of word period n + 1, and all of word period n + 2, both U and L are circulated:

$$U' = H\ Q_3\ \underline{Q}_4\ \underline{Q}_5\ \underline{P}_7\ U\ (t_6 + \underline{F})$$

$$L' = H\ Q_3\ \underline{Q}_4\ \underline{Q}_5\ G\ (\underline{N}\ L + N\ L^*) + \ldots$$

At the end of either SHIFT RIGHT or SHIFT LEFT, the contents of the combined upper and lower accumulators will have been shifted the number of bits indicated in the data track address of the shift command. If a SHIFT RIGHT or SHIFT LEFT command is given with a zero in the data track address, H is turned off before shifting starts in word period 3 and no shift takes place.

$$\underline{H}' = H\ t_6\ (\underline{F}\ \underline{G}\ \underline{P}_1\ K\ Q_3\ \underline{Q}_4\ \underline{Q}_5) + \ldots$$

4.9.16 NORMALIZE, 13, SLC, $\underline{Q}_1\ Q_2\ Q_3\ \underline{Q}_4\ Q_5$

The value contained in the double length accumulator (U and L) is shifted left until it is in normalized form, that is, until bit 1 contains the first significant magnitude bit. Following the shift, L is cleared to zero and the number of places shifted is put in bits 5-17 of L.

During word period 1, phase 4, U and L are circulated as in the shift commands:

$$U' = \underline{H}\ \underline{Q}_1\ Q_3\ \underline{Q}_4\ U + \ldots$$

$$L' = \underline{H}\ \underline{Q}_1\ Q_2\ Q_3\ \underline{Q}_4\ L + \ldots$$

Phase 4a, word period 2, is entered by:

$$H' = F\ G\ \underline{H}\ t_6\ \underline{Q}_1\ Q_2\ Q_3\ \underline{Q}_4$$

$$\underline{G}' = G\ t_6\ \underline{H}\ \underline{R}$$

$$\underline{F}' = F\ G\ t_6\ \underline{R}$$

Again, word period 2 is executed exactly as in the shift commands, with U and L circulated by:

$$U' = H\ Q_3\ \underline{Q_4}\ \underline{F}\ \underline{P_1}\ U\ Q_5 + \ldots$$

$$L' = H\ Q_3\ \underline{Q_4}\ \underline{F}\ \underline{P_1}\ (\underline{N}\ L + N\ L^*) + \ldots$$

The P flip-flops are set by:

$$P_3' = H\ Q_3\ \underline{P_1}\ \underline{t_6}\ u + \ldots$$

$$\underline{P_3}' = H\ Q_3\ \underline{P_1}\ \underline{t_6}\ \underline{u} + \ldots$$

$$P_4' = H\ Q_3\ \underline{t_6}\ P_3 + \ldots$$

$$\underline{P_4}' = H\ Q_3\ \underline{t_6}\ \underline{P_3} + \ldots$$

$$P_5' = H\ Q_3\ \underline{t_6}\ P_4 + \ldots$$

During sign time of word period 2, flip-flops P_2 and P_4 are turned off by:

$$\underline{P_2}' = Q_3\ H\ t_6 + \ldots$$

$$\underline{P_4}' = Q_3\ H\ t_6 + \ldots$$

Flip-flop P_3 is set by:

$$P_3' = H\ Q_3\ \underline{P_1}\ t_6\ (\underline{N}\ L + N\ L^*)$$

$$\underline{P_3}' = H\ Q_3\ \underline{P_1}\ t_6\ (\underline{N}\ \underline{L} + N\ \underline{L}^*)$$

Both U and L continue to be circulated as above. During word period 3 and the following word periods, U is circulated through P_3, causing a one-bit shift to the left:

$$U' = H\ Q_3\ \underline{Q_4}\ \underline{G}\ P_3\ P_1\ Q_5 + \ldots$$

and L is circulated through P_2, causing a one-bit delay.

$$L' = H\ \underline{G}\ Q_3\ \underline{Q_4}\ P_1\ P_2\ Q_5 + \ldots$$

Flip-flops P_4 and P_5 are set by:

$$P_4' = H\ Q_3\ \underline{t_6}\ P_3 + \ldots$$

$$\underline{P_4}' = H\ Q_3\ \underline{t_6}\ \underline{P_3} + \ldots$$

$$P_5' = H\ Q_3\ \underline{t_6}\ \underline{P_4} + \ldots$$

$$\underline{P_5}' = t_6 + \ldots$$

During the first bit of word period 3 and during all bits of the following word periods, the content of P_3 is set into the least significant bit position of U by:

$$U' = H\ \underline{G}\ P_1\ Q_3\ \underline{Q_4}\ P_3 + \ldots$$

Both P_2 and P_4 are set to zero:

$$\underline{P_2}' = H\ Q_3\ t_6 + \ldots$$

$$\underline{P_4}' = H\ Q_3\ t_6 + \ldots$$

and L is circulated through P_2 to set the least significant bit position to zero.

$$L' = H\ \underline{G}\ Q_3\ \underline{Q_4}\ P_1\ P_2 + \ldots$$

At sign time, P_3 has the new sign of U, and P_4 has the new 1/2 bit of U. If these bits are 0 and 1, the number in U is at least + 1/2 ($\underline{P_3}$ and P_4 are true). If the bits are 1 and 0, the number is less than - 1/2 (P_3 and $\underline{P_4}$ true). A stop must be generated when these conditions are met.

As -1 is not wanted as a result of SLC, stop must also be generated when U is exactly - 1/2 (which would become -1 on the next shift). P_5 identifies - 1/2 by indicating any "1's" to the right of the 1/2 bit in U during sign time.

One more bit must be considered, namely the sign bit of L. If this bit is a "1", another shift is possible without developing -1 in U. Thus, the stop term developed is:

$$G' = H\ Q_3\ \underline{Q_4}\ Q_5\ t_6 \left[(P_3\ \underline{P_4} + \underline{P_3}\ P_4 + P_3\ P_4\ \underline{P_5})\ (\underline{N}\ \underline{L} + N\ \underline{L^*})\right]$$

G goes true when the next shift would cause an overflow. The content of U and L is now normalized. Setting G true causes F to go false the following word period:

$$\underline{F}' = F\ t_6\ G\ H + \ldots$$

This will cause G and H to go false the next odd word period by:

$$\underline{H}' = H\ t_6\ G\ F\ P_1 + \ldots$$

$$\underline{G}' = G\ t_6\ P_1\ \underline{F} + \ldots$$

causing the computer to enter phase 1 of the following command.

During each execution of the NORMALIZE command, the shift count is entered into the operand sector of the C register by:

$$\underline{K}' = H\ Q_3\ \underline{Q_4}\ (P_1 + F)\ Q_5\ \underline{C}\ \underline{S_2}\ \underline{S_3}$$

$$C' = H\ Q_3\ \underline{Q_4}\ \underline{S_2}\ \underline{S_3}\ (C\ \underline{K} + \underline{C}\ K) + \ldots$$

During n + 1 operand sector time, L receives the shift count by:

$$L' = H\ Q_3\ \underline{Q_4}\ \underline{S_2}\ \underline{S_3}\ C\ F\ G\ Q_5 + \ldots$$

The final result is that the contents of U and L are shifted to the left to normalize the count and L is zero except for the shift count in the operand sector.

4.9.17 MULTIPLY, 14, MPY, $\underline{Q_1}\ Q_2\ Q_3\ Q_4\ \underline{Q_5}$

The contents of U are multiplied by the contents of the memory location specified by the data address. The resulting double length products are held in U and L. Timing is co-ordinated with the phases as indicated in table 4-2.

Table 4-2

RPC-4010 COMPUTER

MULTIPLICATION TIMETABLE

WORD PERIOD	F	G	H	P_1	U'	L'	I_1	I_2	S
1 (Ph4)	1	1	0	-	U t_6	V	-	-	-
2 (Ph 4a)	0	0	1	0	e_2	L	0	P_7 L	1
3	0	0	1	1	e_2 $\underline{t_6}$	L	U*	P_6	1
4--62 (even WP)	1	0	1	0	e_2	L	U*	P_7 L	0
5--63 (odd WP)	1	0	1	1	e_2 $\underline{t_6}$	L	U*	P_7 P_6	0
64 (K on)	1	0	1	0	e_2	L	U*	P_7 L	0
65	1	f 1	1	1	e_2 $\underline{t_6}$	L	U*	P_7 L	0
66	0	1	1	0	e_2	e_2	U*	0	0
67	0	1	1	1	e_2	L	U*	0	0

NOTE: P_6' = F G $\underline{H}$ t_6 V (sign of multiplicand)

P_7' = F G H P_1 t_6 U* + F G $\underline{H}$ t_6 U (multiplier digits)

The process of multiplication consists of a series of additions of the multiplicand to the partial product and the shifting of the partial product for each digit of the multiplier. As multiplication continues from the first digit of the multiplier to the last, the partial product formed by each addition and shift increases from one word to approximately two. Thus, a multiplication requires 64 word periods (two for each digit of the multiplier) to complete the product.

To retain the digits of the full product, U is extended to two words plus one bit by the use of the second read head, U*. During the first word period, the two words in U contain the multiplier and one bit of the partial product. As multiplication continues, the partial product increases to approximately two words and the multiplier decreases to zero. This is accomplished by dropping each digit of the multiplier from circulation as it is used, and shifting the remainder of the multiplier and the increased partial product to the next most significant digit position.

The bits presented by U* occur exactly 65 bit periods after being recorded. In other words U* shifts the information for one bit left each two word periods of multiplication.

The bits of the multiplier are dropped as they are used by inhibiting the recording of U' at the last sign time of each two word period of multiplication. To accomplish this, the U' record equation is formed of only those terms which

include the sign time of the last of the two word periods. During phase 4, word period 1, U is circulated and the sign bit dropped by:

$$U' = \underline{Q_1}\ Q_3\ \underline{Q_5}\ \underline{t_6}\ U\ \ \underline{H} + \ldots$$

To mark each of the two word periods required for the addition of the multiplicand to the partial product, flip-flop P_1 is turned off at the end of the first word period of phase 4. At the end of the next word period it is set on, and alternates throughout the execution of multiplication. That is to say, during each odd word period, P_1 is on, and during each even word period, is off.

$$P_1' = H\ \underline{P_1}\ t_6\ (Q_3 + Q_4)$$

$$\underline{P_1}' = F\ G\ \underline{H}\ t_6\ \underline{Q_1}\ \underline{Q_2}\ Q_3\ Q_4\ \underline{Q_5} + H\ \ P_1\ Q_4\ t_6 + \ldots$$

The memory location specified by the data address is copied into L as the multiplicand during word period 1 by:

$$L' = F\ G\ \underline{H}\ V\ \underline{Q_1}\ Q_2\ Q_4\ \underline{Q_5} + \ldots$$

The sign of the multiplicand is set into P_6 during phase 4 by:

$$P_6' = F\ G\ \underline{H}\ t_6\ Q_4\ \underline{R}\ V + \ldots$$

$$\underline{P_6}' = F\ G\ \underline{H}\ t_6\ Q_4\ \underline{R}\ \underline{V} + \ldots$$

The sign of U is set into P_7 during phase 4 by:

$$P_7' = F\ G\ \underline{H}\ t_6\ Q_4\ \underline{R}\ U + \ldots$$

$$\underline{P_7}' = F\ G\ \underline{H}\ t_6\ Q_4\ \underline{R}\ \underline{U} + \ldots$$

During sign time of the following odd word periods of phase 4a, P_7 will be set by the successive multiplier digits:

$$P_7' = H\ P_1\ t_6\ Q_3\ Q_4\ U^* + \ldots$$

$$\underline{P_7}' = H\ P_1\ t_6\ Q_3\ Q_4\ \underline{U}^* + \ldots$$

During periods 2 through 67 of the MULTIPLY command, the result of I_1 and I_2 (e_2) is copied into U by:

$$U' = H\ Q_4\ (\underline{P_1} + \underline{t_6}\ \underline{F}\ G)\ e_2$$

$$e_2 = A\ I_1\ I_2 + A\ \underline{I_1}\ \underline{I_2} + \underline{A}\ I_1\ \underline{I_2} + \underline{A}\ \underline{I_1}\ I_2$$

During even word periods of the execution of MULTIPLY, A is the carry:

$$A' = I_2\ (I_1\ \underline{S} + \underline{I_1}\ S)\ Q_4\ H\ Q_3\ \underline{P_1} + \ldots$$

$$\underline{A}' = \underline{I_2}\ (I_1\ S + \underline{I_1}\ \underline{S})\ H\ Q_4 + \ldots$$

Addition of U and L is performed through I_1 and I_2, as indicated by the contents of L:

$$I_1' = H\ (F + G\ Q_3 + P_1\ \underline{G})\ U^* + \ldots$$

$$I_2' = H\ P_1\ P_6\ (\underline{F}\ \underline{G}\ Q_3 + F\ Q_3\ P_7) + H\ \underline{P_1}\ \underline{G}\ P_7\ (\underline{N}\ \underline{L} + N\ \underline{L}^*) + \ldots$$

P_6 is ture and S is true during WP 66 and 67. S is always true during WP 2 and 3.

$$S' = H\ (\underline{F}\ \underline{G}\ Q_3 + \underline{F}\ G\ P_6)$$

During word periods 3 through 67, I_1 is the content of U, which is shifted left each even word period. The contents of L become I_2 during even word periods when P_7 is true. I_2 is true for all odd word periods when U is negative and P_6 is true, indicating the multiplicand is negative. Each even word period that P_7 is true, I_2, which is L, is added to I_1, the result is copied into U, and U is shifted one bit position. Bits in L which are zero cause nothing to be added to I_1, but the one bit shift is accomplished as before. At word period 66, the double length result is in extended U. At this time, e_2 is copied into L:

$$L' = H\ Q_4\ \underline{P_1}\ G\ e_2 + \ldots$$

and into U:

$$U' = H\ Q_4\ \underline{P_1}\ e_2 + \ldots$$

During word period 67, both U and L are circulated as the double length product of U and the contents of memory specified by the data address.

4.9.18 MULTIPLY BY TEN, 15, MPT, $\underline{Q_1}\ Q_2\ Q_3\ Q_4\ Q_5$

Multiply the contents of U by ten if the data track number is 0. Multiply the contents of L by ten if the data track number is 64.

To multiply by ten, only one word period of phase 4 is required for execution. The operation is carried out by delaying data one bit (multiplying by two), then delaying the same data three bits (multiplying by eight) and adding the two results.

During execution, the P_1 flip-flop is used to determine whether U or L will be multiplied. The P_2 flip-flop copies L:

$$P_2' = (\underline{N}\ L + N\ L^*)\ F\ G\ \underline{Q_1}\ Q_2\ Q_3\ Q_4\ Q_5\ \underline{t_6} + \ldots$$

$$\underline{P_2}' = (\underline{N}\ \underline{L} + N\ \underline{L}^* + t_6)\ F\ G\ \underline{Q_1}\ Q_2\ Q_3\ Q_4\ Q_5 + \ldots$$

Note at sign time that P_2 is turned off. The output of P_2 is L-delayed one bit and thus multiplied by 2:

$$P_2 = 2 \times L$$

The output of P_3 is U-delayed one bit and thus multiplied by 2:

$$P_3' = U\ F\ G\ \underline{Q_1}\ Q_2\ Q_3\ Q_4\ Q_5\ \underline{t_6} + \ldots$$

$$\underline{P_3}' = (\underline{U} + t_6)\ F\ G\ \underline{Q_1}\ Q_2\ Q_3\ Q_4\ Q_5 + \ldots$$

$$P_3 = 2 \times U$$

The state of P_1 determines whether P_2 or P_3 is copied by P_4:

$$P_4' = F\ G\ \underline{Q_1}\ Q_2\ Q_3\ Q_4\ Q_5\ (\underline{P_1}\ P_3 + P_1\ P_2)\ \underline{t_6}$$

$$\underline{P_4}' = F\ G\ \underline{Q_1}\ Q_2\ Q_3\ Q_4\ Q_5\ (\underline{P_1}\ \underline{P_3} + P_1\ \underline{P_2} + t_6)$$

As with P_2 and P_3, P_4 is turned off at sign time. The output of P_4 sets P_5, except at sign time:

$$P_5' = F\ G\ \underline{Q_1}\ Q_2\ Q_3\ Q_4\ Q_5\ P_4\ \underline{t_6} + \ldots$$

$$\underline{P_5}' = F\ G\ \underline{Q_1}\ Q_2\ Q_3\ Q_4\ Q_5\ (\underline{P_4} + t_6)$$

The output of P_5 is either U or L-delayed three bit periods, thus multiplied by 2^3 or 8:

$$P_5 = 8 \times U$$

or

$$P_5 = 8 \times L$$

To complete the multiplication, it is necessary to add P_2 and P_5 for L, or P_3 and P_5 for U:

$$8 \times L + 2 \times L = 10 \times L$$

or

$$8 \times U + 2 \times U = 10 \times U$$

To add, the quantities to be added become the inputs to I_1 and I_2:

$$I_1' = \underline{H}\ F\ \underline{Q_1}\ (\underline{P_1}\ P_3 + P_1\ P_2)$$

$$I_2' = \underline{H}\ F\ \underline{Q_1}\ P_5$$

The sum appears as e_2. If $\underline{P_1}$ is true, U is multiplied by ten:

$$U' = F\ G\ \underline{P_1}\ \underline{Q_1}\ Q_2\ Q_3\ Q_4\ Q_5\ e_2 + \ldots$$

If P_1 is true, L is multiplied by ten:

$$L' = F\ G\ P_1\ Q_2\ Q_3\ Q_4\ Q_5\ e_2 + \ldots$$

Modified by E.C.

The original contents of the four P flip-flops P_2, P_3, P_4, and P_5 are important. ~~When data tracks 0 or 64 are given, these flip-flops contain zeros. If other data track numbers are given, the contents of these four flip-flops~~ will add 1, 2, 3, 5, 6, 7, or 8 to the product of U or L in the least significant bit positions (table 4-3).

4.9.19 PRINT DATA ADDRESS, 16, PRD, $\underline{Q_1}\ \underline{Q_2}\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5}$

The PRD command presents the data track number as a binary output to input/output. Track numbers 0 through 63 are characters to be printed or punched (table 4-4) and track numbers 64 through 127 are control functions (table 4-5).

The operand sector number is disregarded except in the case of a completely optimum address, where the operand sector is two greater than the location of the command. In this instance, the interlock from input/output (Z_0) is overridden and the computer will not wait for a ready signal from input/output: it assumes the I/O device is in the process of executing a previous print command.

Table 4-3

RPC-4010 COMPUTER-

QUANTITIES ADDED DURING

MPT COMMAND

Changed by E/C.

FLIP-FLOPS					RESULT	
P_1	P_2	P_3	P_4	P_5		
0	X	0	0	0	10L	L
0	X	0	0	1	10L+1	L
0	X	0	1	0	10L+2	L
0	X	0	1	1	10L+3	L
0	X	1	0	0	10L+5	L
0	X	1	0	1	10L+6	L
0	X	1	1	0	10L+7	L
0	X	1	1	1	10L+8	L
1	0	X	0	0	10U	U
1	0	X	0	1	10U+1	U
1	0	X	1	0	10U+2	U
1	0	X	1	1	10U+3	U
1	1	X	0	0	10U+5	U
1	1	X	0	1	10U+6	U
1	1	X	1	0	10U+7	U
1	1	X	1	1	10U+8	U

X No Effect on Operation

During execution of the PRD command, U and L are circulated by:

$$U' = U \underline{H} Q_1 \underline{Q_3} \underline{Q_4} + \ldots$$

$$L' = (\underline{N} L + N L^*) \underline{H} Q_1 \underline{Q_3} \underline{Q_4} + \ldots$$

During phase 3 of the PRD or PRU command, K is on, so a successful sector search in the first wordtime of phase 3 causes entry into phase 4. If the first sector of phase 3 is not addressed, K depends on Z_o being true. Hence, a sector search cannot end phase 3 while the interlock is false. When Z_o goes true, G

goes on, entering phase 4 immediately. The operand track number is set into the P flip-flops by f_7:

$$f_7 = \underline{G}\ \underline{H}\ \underline{S_1}\ S_3\ F\ \underline{S_2}\ \underline{Q_2} + \ldots$$

During phase 4, a Y_o signal is sent to input/output, indicating data is being presented for output:

$$Y_o = F\ G\ Q_1\ \underline{Q_2}\ \underline{Q_3}\ \underline{Q_4}$$

Table 4-4

RPC-4010 COMPUTER

ALPHANUMERIC AND FUNCTION

CODE

NUMERIC	DEFINITION	BINARY	NUMERIC	DEFINITION	BINARY
00	Tape Feed	000000	32	G	100000
01	Carriage Return	000001	33	H	100001
02	Tab	000010	34	I	100010
03	Backspace	000011	35	J	100011
04	Color Shift	000100	36	K	100100
05	Upper Case	000101	37	L	100101
06	Lower Case	000110	38	M	100110
07	Line Feed	000111	39	N	100111
08	*Stop Code	001000	40	O	101000
09		001001	41	P	101001
10		001010	42	Q	101010
11	Photo Reader	001011	43	R	101011
12		001100	44	S	101100
13	End of Message	001101	45	T	101101
14		001110	46	U	101110
15		001111	47	V	101111
16	0)	010000	48	W	110000
17	1 o	010001	49	X	110001
18	2 "	010010	50	Y	110010
19	3 #	010011	51	Z	110011
20	4 Σ	010100	52	, $	110100
21	5 Δ	010101	53	= :	110101
22	6 @	010110	54	[;	110110
23	7 &	010111	55	] %	110111
24	8 '	011000	56		111000
25	9 (	011001	57		111001
26	A	011010	58	+ ?	111010
27	B	011011	59	- _	111011
28	C	011100	60	. .	111100
29	D	011101	61	Space	111101
30	E	011110	62	/ $\div$	111110
31	F	011111	63	Code delete	111111

Table 4-5

INPUT/OUTPUT SELECTION CODES
RPC-4000 System

Data Track No.	Input/Output Unit & Function:
64	4500 Reader Input
65	4500 Reader Input & Punch Output
66	4500 Reader Input & Typewriter Output
67	4500 Reader Input & Punch & Typewriter Output
68	4500 Typewriter Input
69	4500 Typewriter Input & Punch Output
70	4500 Typewriter Input & Typewriter Output
71	4500 Typewriter Input & Punch & Typewriter Output
72	4410 Photo-Reader, Forward & Search
73	4410 Photo-Reader, Reverse & Search
74	4410 Photo-Reader, Forward
75	4410 Photo-Reader, Reverse
76-79	Available for Additional Units
80	4600 Reader Input
81	4600 Reader Input & Punch Output
82	4600 Reader Input & Typewriter Output
83	4600 Reader Input & Punch & Typewriter Output
84	4600 Typewriter Input
85	4600 Typewriter Input & Punch Output
86	4600 Typewriter Input & Typewriter Output
87	4600 Typewriter Input & Punch & Typewriter Output
88-94	Available for Additional Units
95	Master Reset
96	Available for Additional Units
97	4500 Punch Output
98	4500 Typewriter Output
99	4500 Punch & Typewriter Output
100	Available for Additional Units
101	4500 Punch Output
102	4500 Typewriter Output
103	4500 Punch & Typewriter Output
104	4410 Photo-Reader Search Mode
105	4410 Photo-Reader Search Mode
106	4440 High Speed Punch
107-112	Available for Additional Units
113	4600 Punch Output
114	4600 Typewriter Output
115	4600 Punch & Typewriter Output
116	Available for Additional Units
117	4600 Punch Output
118	4600 Typewriter Output
119	4600 Punch & Typewriter Output
120	4290 Input & Output Translator Select
121	4290 Input Translator Select
122	4290 Output Translator Select
123	4290 Input Translator Reset
124	4290 Output Translator Reset
125	Input Duplication On
126	Input Duplication Off
127	Reset Output Units

With Y_O true, input/output reads the states of the P flip-flops. The combination of their states causes either a character to be printed or punched, or an input/output function to be executed. The logic involved is explained in the section on input/output, section 4.10.

4.9.20 PRINT FROM UPPER, 17, PRU, Q_1 $\underline{Q_2}$ $\underline{Q_3}$ $\underline{Q_4}$ $\underline{Q_5}$

The PRU command presents the most significant four or six bits of U as an output. A "1" in bit position 5 results in a six-bit output. A "0" in bit position 5 results in a four-bit output. The two remaining bits of the output word are bit positions 6 and 7 of the instruction word in the C register.

The operand sector number is disregarded except in the case of a completely optimum address, where the operand sector is two greater than the location of the command. As in PRD, the computer will not wait for a ready signal from input/output.

$$U' = U\ \underline{H}\ Q_1\ \underline{Q_3}\ \underline{Q_4} + \ldots$$

$$L' = (\underline{N}\ L + N\ L^*)\ \underline{H}\ Q_1\ \underline{Q_3}\ \underline{Q_4} + \ldots$$

Bit position 5 sets P_1 by:

$$P_1' = f_7\ C + \ldots$$

$$\underline{P_1}' = f_7\ \underline{C} + \ldots$$

$$f_7 = \underline{G}\ \underline{H}\ \underline{S_1}\ S_3\ F\ \underline{S_2} + \ldots$$

The remaining P flip-flops are set during phase 3 by U. The state of P_1 determines whether 4 or 6 bits from U are used to set the P flip-flops:

$$P_2' = k_2\ P_1\ U + \ldots \qquad \text{(6-bit output)}$$

$$\underline{P_2}' = k_2\ P_1\ \underline{U} + \ldots \qquad \text{" " "}$$

$$P_3' = k_2\ P_1\ U^* + \ldots \qquad \text{" " "}$$

$$\underline{P_3}' = k_2\ P_1\ \underline{U}^* + \ldots \qquad \text{" " "}$$

$$P_4' = k_2\ P_1\ P_3 + k_2\ \underline{P_1}\ U + \ldots \qquad \text{(4-bit output)}$$

$$\underline{P_4}' = k_2\ P_1\ \underline{P_3} + k_2\ \underline{P_1}\ \underline{U} + \ldots \qquad \text{" " "}$$

$$P_5' = k_2\ P_4 + \ldots \qquad \text{" " "}$$

$$\underline{P_5}' = k_2\ \underline{P_4} + \ldots \qquad \text{" " "}$$

$$P_6' = k_2\ P_5 + \ldots \qquad \text{" " "}$$

$$\underline{P_6}' = k_2\ \underline{P_5} + \ldots \qquad \text{" " "}$$

$$P_7' = k_2\ P_6 + \ldots \qquad \text{" " "}$$

$$\underline{P_7}' = k_2\ \underline{P_6} + \ldots \qquad \text{" " "}$$

$$k_2 = F\ \underline{G}\ S_1\ Q_1\ \underline{Q_2}\ \underline{Q_3}\ \underline{Q_4}\ Q_5\ S_3$$

The k_2 signal is on for only 6 bit times, so it is necessary to take the input for P_3 from U*.

Phase 3 is ended by:

$$G' = \underline{G}\ t_6\ Z_i\ F\ Z_o\ Q_1\ \underline{Q_2}\ \underline{Q_3}\ \underline{Q_4} + \ldots$$

During phase 4, a Y_o signal is sent along with the output to input/output to indicate the computer is ready to output data.

$$Y_o = F\ G\ Q_1\ \underline{Q_2}\ \underline{Q_3}\ \underline{Q_4}$$

The setting of the P flip-flops is read into Input/Output during phase 4.

4.9.21 EXTRACT, 18, EXT, $Q_1\ \underline{Q_2}\ \underline{Q_3}\ Q_4\ \underline{Q_5}$

The EXT command logically combines the contents of the memory location specified by the data address bit by bit with the contents of U. The result, in U, contains "1's" in both memory and U. That is, the result in U is the Boolean "AND" of the memory word and the previous contents of U.

During the execution of EXT, L is circulated by:

$$L' = (\underline{N}\ L + N\ L^*)\ \underline{H}\ (Q_1 + \underline{Q_2})\ \underline{Q_5} + \ldots$$

During phase 4, memory and U are combined by:

$$U' = U\ \underline{H}\ F\ G\ V\ \underline{Q_2}\ \underline{Q_3}\ Q_4\ \underline{Q_5} + \ldots$$

The result of this combination is held in U.

4.9.22 MASKED MERGE LOWER, 19, MML, $Q_1\ \underline{Q_2}\ \underline{Q_3}\ Q_4\ \underline{Q_5}$

The MML command combines the word specified by the data address with L bit by bit through a mask in U. Bits in L are kept where U is 0, or are replaced by bits in memory where U is 1.

During phase 4 of MML, L is the result of:

$$L' = G\ (\underline{N}\ L + N\ L^*)\ \underline{H}\ Q_1\ \underline{Q_2}\ \underline{Q_3}\ \underline{U} + F\ G\ \underline{H}\ \underline{Q_2}\ \underline{Q_3}\ Q_4\ \underline{Q_5}\ U\ V$$

By this logic, L is either the contents of L when U is false, or the contents of memory when U is true.

4.9.23 COMPARE MEMORY EQUAL, 20, CME, $Q_1\ \underline{Q_2}\ Q_3\ \underline{Q_4}\ \underline{Q_5}$

The CME command compares U with the addressed word in memory through a mask in L. If the two words are identical in the bit positions where L has "1's", the branch control (B) flip-flop is turned on.

At the end of the last word period of phase 3 of the CME command, the B flip-flop is turned off by:

$$\underline{B}' = Z_i\ F\ \underline{G}\ t_6\ \underline{A}\ \ Q_1\ \underline{Q_2}\ Q_3\ \underline{Q_4}\ K + \ldots$$

Throughout the execution of the command, U and L are circulated by:

$$U' = U\ \underline{H}\ \underline{Q_2}\ Q_3 + \ldots$$

$$L' = (\underline{N}\ L + N\ L^*)\ \underline{H}\ \underline{Q_2}\ Q_3 + \ldots$$

The comparison with U of the word in memory specified by the data address takes place in phase 4. The indication that the words are equal is that B is true.

A is preset off at sign time of phase 2:

$$\underline{A}' = \underline{F}\ t_6\ \underline{H} + \ldots$$

A is turned on by a mismatch during the word, where there are "1's" in L:

$$A' = F\ G\ \underline{H}\ \underline{t_6}\ \underline{Q_2}\ Q_3 \left[(\underline{N}\ L + N\ L^*)\ \underline{U}\ V\ \underline{Q_5} + (\underline{N}\ L + N\ L)\ U\ \underline{V}\right] + \ldots$$

At sign time, if A is off or if the mask has all "0's", a successful comparison is indicated to B by:

$$B' = F\ G\ t_6\ Q_1\ \underline{Q_2}\ Q_3\ \underline{Q_4}\ \underline{A}\ (\underline{N}\ \underline{L} + N\ \underline{L}^* + U\ V + \underline{U}\ \underline{V}) + \ldots$$

During comparison when in repeat mode, until a successful comparison is made, S_1 is copied into X in the next instruction sector position. When B goes on, X starts circulating the sector obtained, which is one greater than the sector in which the successful comparison was made.

$$X' = F\ G\ Q_1\ \underline{Q_2}\ Q_3\ \underline{Q_4}\ S_1\ S_2\ \underline{S_3}\ \underline{B}\ R$$

4.9.24 COMPARE MEMORY GREATER, 21, CMG, $Q_1\ \underline{Q_2}\ Q_3\ \underline{Q_4}\ Q_5$

The CMG command compares the data word in the memory location specified by the data address with U through a mask in L.

If the word in memory is equal to or greater than U in the bit psoitions where L has "1's", B is turned on.

At the end of phase 3 of the CMG command, the B flip-flop is turned off by:

$$B' = F\ \underline{G}\ t_6\ Q_1\ \underline{Q_2}\ Q_3\ (\underline{Q_4} + Q_5) + \ldots$$

Throughout the execution of the command U and L are circulated by:

$$U' = U\ \underline{H}\ \underline{Q_2}\ Q_3 + \ldots$$

$$L' = (\underline{N}\ L + N\ L^*)\ \underline{H}\ \underline{Q_2}\ Q_3 + \ldots$$

The comparison of the word in memory specified by the data address with U takes place in phase 4. This is an algebraic compare on sign digit, if the mask has a "1" in the sign digit position. If the word in memory specified by the data address is equal to or greater than U, B is turned on:

$$B' = F\ G\ t_6\ Q_1\ \underline{Q_2}\ Q_3\ \underline{Q_4}\ \underline{A}\ \left[(\underline{N}\ \underline{L} + N\ \underline{L} + U\ V + \underline{U}\ \underline{V}) + Q_5\ (\underline{N}\ L + N\ L^*\ \underline{U}\ V)\right]$$

The A flip-flop must be false in order to turn the B flip-flop on. A is turned off when memory is greater than U, gated through the mask by:

$$\underline{A}' = F\ G\ Q_1\ \underline{Q_2}\ Q_5\ V\ \underline{U}\ (\underline{N}\ L + N\ L^*) + \ldots$$

When U is greater than V, A is turned on by:

$$A' = F\ G\ \underline{H}\ \underline{Q_2}\ Q_3\ \underline{t_6}\ (\underline{N}\ L + N\ L^*)\ U\ \underline{V} + \ldots$$

Thus, with A true, B will not go true. With A false, the B flip-flop is turned on when there is no mask in L, when U and V are equal, or when V is greater than U.

As in the CMG command, the sector is copied into X and circulated following a successful compare.

4.9.25 TRANSFER ON MINUS, 22, TMI, $Q_1\ \underline{Q_2}\ Q_3\ Q_4\ \underline{Q_5}$

The TMI command tests the sign of U. If U is negative, the operand address of the command word is used to locate the next instruction. If U is positive, the next instruction address of the command word is used to locate the next instruction.

During the execution of the TMI command, U and L are circulated by:

$$U' = U\ \underline{H}\ \underline{Q_2}\ Q_3 + \ldots$$

$$L' = (\underline{N}\ L + N\ L^*)\ \underline{H}\ \underline{Q_2}\ Q_3 + \ldots$$

During phase 3, the sign of U determines the location of the next instruction. If U is negative during sign time the F flip-flop is turned off when the sector search is completed, as indicated by K:

$$\underline{F}' = F\ t_6\ K\ \underline{A}\ Q_1\ \underline{Q_2}\ Q_3\ Q_4\ \underline{Q_5}\ U + \ldots$$

This returns the computer to phase 2, and the operand address of the command word becomes the next instruction address.

If U is positive, the G flip-flop is turned on immediately:

$$G' = F\ \underline{A}\ \underline{H}\ Q_1\ Q_3\ Q_4\ \underline{Q_5}\ \underline{U}\ \underline{G}\ t_6\ Z_i + \ldots$$

This causes the computer to enter phase 4 directly, go to phase 1 and use the next instruction address to locate the next instruction.

4.9.26 TRANSFER ON BRANCH CONTROL, 23, TBC, $Q_1\ \underline{Q_2}\ Q_3\ Q_4\ Q_5$

The TBC command tests the branch control flip-flop B. If B is true, the operand address of the command is used as the next instruction address and B is turned off. If B is false when tested, the command has no effect, and the next instruction is specified in the next instruction address portion of the command word.

During the execution of the TBC command, U and L are circulated by:

$$U' = U\ \underline{H}\ \underline{Q_2}\ Q_3 + \ldots$$

$$L' = (\underline{N}\ L + N\ L^*)\ \underline{H}\ \underline{Q_2}\ Q_3 + \ldots$$

During phase 3, the state of B determines the location of the next instruction. If B is on, the F flip-flop is turned off:

$$\underline{F}' = F\ t_6\ K\ Z_i\ \underline{A}\ Q_1\ \underline{Q_2}\ Q_3\ Q_4\ Q_5\ B + \ldots$$

This returns the computer to phase 2, and the operand address of the command word becomes the next instruction address. At the same time, B is turned off by:

$$\underline{B}' = Z_i\ F\ \underline{G}\ t_6\ K\ \underline{A}\ \ Q_1\ \underline{Q_2}\ Q_3\ Q_5 + \ldots$$

If the B flip-flop is already off, G is turned on by:

$$G' = \underline{G}\ t_6\ \underline{A}\ F\ \underline{H}\ Q_1\ Q_3\ Q_4\ Q_5\ \underline{B} + \ldots$$

This causes the computer to enter phase 4 and use the next instruction address to locate the next instruction.

4.9.27 STORE UPPER, 24, STU, $Q_1\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5}$

The STU command stores the contents of U in the memory location specified by the data address. The contents of U are undisturbed.

During the execution of the STU command, U and L are circulated by:

$$U' = U\ \underline{H}\ Q_1\ \underline{Q_3}\ \underline{Q_4} + \ldots$$

$$L' = (\underline{N}\ L + N\ L^*)\ \underline{H}\ Q_1\ \underline{Q_3}\ \underline{Q_4}$$

In order to record information in memory, W must be true. This is accomplished at index time of the last WP of phase 3 and phase 4 by:

$$W' = (F\ \underline{H}\ \underline{G}\ K\ t_6\ \underline{A} + \underline{H}\ F\ G\ \underline{t_6})\ Q_1\ Q_2\ \underline{Q_3} + \ldots$$

The contents of U are recorded into memory by reading U one bit early as u:

$$V' = \underline{Q_5}\ u$$

W and V will record the contents of U into the memory location specified by the data address.

4.9.28 STORE LOWER, 25, STL, $Q_1\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5}$

The STL command stores the contents of L in the memory location specified by the data address. The contents of L are undisturbed.

During the execution of the STL command, U and L are circulated by:

$$U' = U\ \underline{H}\ Q_1\ \underline{Q_3}\ \underline{Q_4}$$

$$L' = (\underline{N}\ L + N\ L^*)\ \underline{H}\ Q_1\ \underline{Q_3}\ \underline{Q_4}$$

In order to record information in memory, W must be true. This is accomplished at index time of the last WP of phase 3 and in phase 4 by:

$$W' = (F\ \underline{H}\ \underline{G}\ K\ t_6\ \underline{A} + \underline{H}\ F\ G\ \underline{t_6})\ Q_1\ Q_2\ \underline{Q_3} + \cdots$$

The contents of L are recorded into memory by reading L one bit early as 1:

$$V' = Q_5\ (\underline{N}\ 1 + N\ 1^*)$$

W and V will record the contents of L into the memory location specified by the data address.

4.9.29 CLEAR UPPER, 26, CLU, $Q_1\ Q_2\ \underline{Q_3}\ Q_4\ \underline{Q_5}$

The CLU command stores the contents of U in the memory location specified by the data address and sets U to zero. During the execution of the CLU command, U is not circulated but reads "0's". L is circulated by:

$$L' = (\underline{N}\ L + N\ L^*)\ \underline{H}\ Q_1\ \underline{Q_5}$$

In order to record information in memory, W must be true. This is accomplished at index time of the last WP of phase 3 and during phase 4 by:

$$W' = (F\ \underline{H}\ \underline{G}\ K\ t_6\ \underline{A} + \underline{H}\ F\ G\ \underline{t_6})\ Q_1\ Q_2\ \underline{Q_3}$$

The contents of U are recorded into memory by reading U one bit early as u:

$$V' = \underline{Q_5}\ u$$

W and V will record the contents of U into the memory location specified by the data address.

4.9.30 CLEAR LOWER, 27, CLL, $Q_1\ Q_2\ \underline{Q_3}\ Q_4\ \underline{Q_5}$

The CLL command stores the contents of L in the memory location specified by the data address and sets L to zero.

During the execution of the CLL command, L is not circulated but reads "0's". U is circulated by:

$$U' = U\ \underline{H}\ Q_1\ Q_5$$

In order to record information in memory, W must be true. This is accomplished at index time of the last WP of phase 3 and during phase 4 by:

$$W' = (F\ \underline{H}\ \underline{G}\ K\ t_6\ \underline{A} + \underline{H}\ F\ G\ \underline{t_6})\ Q_1\ Q_2\ \underline{Q_3}$$

The contents of L are recorded into memory by reading L one bit early, as 1:

$$V' = Q_5\ (\underline{N}\ 1 + N\ 1^*)$$

W and V will record the contents of L into the memory location specified by the data address.

4.9.31 ADD TO UPPER, 28, ADU, $Q_1\ Q_2\ Q_3\ \underline{Q}_4\ \underline{Q}_5$

The ADU command adds the contents of the memory location specified by the data address to U. The sum is retained in U. If the sum is less than -1 or greater than $1-2^{-31}$, overflow occurs and the branch control flip-flop, B, is turned on.

Throughout the execution of the ADU command, L is circulated by:

$$L' = (\underline{N}\ L + N\ L^*)\ \underline{H}\ Q_1\ \underline{Q}_5$$

During phase 4 the contents of U become the I_1 signal:

$$I_1 = \underline{H}\ F\ Q_1\ \underline{Q}_5\ U$$

At the same time, the contents of the memory location specified by the data address become the I_2 signal:

$$I_2 = \underline{H}\ F\ Q_1\ V$$

The S flip-flop is off, so I_1 and I_2 are added. The combination of I_1 and I_2 determines the state of the A flip-flop. The A flip-flop is turned on by:

$$A' = I_1\ I_2\ \underline{S}\ G\ Q_2\ \underline{t}_6 + \ldots$$

At sign time the A flip-flop is preset off by:

$$\underline{A}' = F\ G\ \underline{H}\ t_6\ Q_1$$

The sum of U and V is recorded into U as the e_2 signal:

$$e_2 = A\ I_1\ I_2 + A\ \underline{I}_1\ \underline{I}_2 + \underline{A}\ I_1\ \underline{I}_2 + \underline{A}\ \underline{I}_1\ I_2$$

and U becomes:

$$U' = e_2\ F\ G\ Q_1\ Q_2\ Q_3\ \underline{Q}_5$$

An overflow is sensed by the B flip-flop at sign time by:

$$B' = F\ G\ t_6\ Q_1\ Q_2\ Q_3\ (\underline{A}\ I_1\ I_2\ \underline{S} + A\ \underline{I}_1\ \underline{I}_2\ \underline{S})$$

Thus, the ADU command adds the contents of the memory location specified by the data address to L. The sum is retained in L. If the sum is less than -1 or greater than $1-2^{-31}$, overflow occurs and the branch control flip-flop, B, is turned on.

4.9.32 ADD TO LOWER, 29, ADL, $Q_1\ Q_2\ Q_3\ \underline{Q}_4\ Q_5$

The ADL command adds the contents of the memory location specified by the data address to L. The sum is retained in L. If the sum is less than -1, or greater than $1-2^{-31}$, overflow occurs and the branch control flip-flop, B, is turned on.

Throughout the execution of the ADL command, U is circulated by:

$$U' = U \underline{H}\, Q_1\, Q_5$$

During phase 4 the contents of L become the I_1 signal:

$$I_1 = \underline{H}\, F\, Q_1\, Q_5\, (\underline{N}\, L + N\, L^*) + \ldots$$

At the same time, the contents of the memory location specified by the data address become the I_2 signal:

$$I_2 = \underline{H}\, F\, Q_1\, V + \ldots$$

The combination of I_1 and I_2 determines the state of the A flip-flop. The A flip-flop is turned off by:

$$\underline{A}' = \underline{I_1}\, \underline{I_2}\, \underline{S}\, Q_2\, \underline{t_6}\, G + \ldots$$

The A flip-flop is turned on by:

$$A' = I_1\, I_2\, \underline{S}\, Q_2\, \underline{t_6}\, G + \ldots$$

Thus, the A flip-flop is on at sign time only when there is a carry.

The sum of L and V is recorded into L as the e_2 signal:

$$e_2 = A\, I_1\, I_2 + A\, \underline{I_1}\, \underline{I_2} + \underline{A}\, \underline{I_1}\, I_2 + \underline{A}\, I_1\, \underline{I_2}$$

and L becomes:

$$L' = F\, G\, e_2\, Q_1\, Q_2\, Q_3\, Q_5 + \ldots$$

An overflow is sensed by the B flip-flop at sign time by:

$$B' = F\, G\, t_6\, Q_1\, Q_2\, Q_3\, (\underline{A}\, I_1\, I_2\, \underline{S} + A\, \underline{I_1}\, \underline{I_2}\, \underline{S}) + \ldots$$

Thus, the ADL command adds the contents of the memory location specified by the data address to L and turns B on if an overflow occurs. Carry is reset each sign time, so the addition of each word in lengthened L is independent.

4.9.33 SUBTRACT FROM UPPER, 30, SBU, $Q_1\, Q_2\, Q_3\, Q_4\, \underline{Q_5}$

The SBU command subtracts the contents of the memory location specified by the data address from U. The remainder is retained in U. If the remainder is less than -1 or greater than $1-2^{-31}$, overflow occurs and the branch control flip-flop, B, is turned on.

Throughout the execution of the SBU command, L is circulated by:

$$L' = \underline{H}\, Q_1\, \underline{Q_5}(\underline{N}\, L + N\, L^*) + \ldots$$

During phase 4, the contents of U become the I_1 signal:

$$I_1 = F\, \underline{H}\, Q_1\, \underline{Q_5}\, U + \ldots$$

At the same time, the contents of the memory location specified by the data address become the I_2 signal:

$$I_2 = F\ \underline{H}\ Q_1\ V + \ldots$$

During execution of a subtract command, the S signal is true:

$$S = F\ \underline{H}\ Q_1\ Q_4 + \ldots$$

The combination of I_1 and I_2 determines the state of the A flip-flop. The A flip-flop is turned on by:

$$A' = \underline{I_1}\ I_2\ S\ Q_2\ \underline{t_6}\ G + \ldots$$

At sign time, the A flip-flop is turned off by:

$$\underline{A}' = I_1\ \underline{I_2}\ S\ Q_2\ G\ \underline{t_6} + t_6\ F\ G\ \underline{H}\ Q_1$$

Thus, the A flip-flop is on at sign time only when there is a carry.

The remainder of the subtraction of V from U is recorded in U as the e_2 signal:

$$e_2 = A\ I_1\ I_2 + A\ \underline{I_1}\ \underline{I_2} + \underline{A}\ I_1\ \underline{I_2} + \underline{A}\ \underline{I_1}\ I_2$$

and U becomes:

$$U' = e_2\ F\ G\ Q_1\ Q_2\ Q_3\ \underline{Q_5}$$

An overflow is sensed by the B flip-flop at sign time by:

$$B' = F\ G\ t_6\ Q_1\ Q_2\ Q_3\ (\underline{A}\ \underline{I_1}\ I_2\ S + A\ I_1\ \underline{I_2}\ S)$$

Thus, the SBU command subtracts the content of the memory location specified by the data address from U and turns B on if an overflow occurs.

4.9.34 SUBTRACT FROM LOWER, 31, SBL, $Q_1\ Q_2\ Q_3\ Q_4\ Q_5$

The SBL command subtracts the contents of the memory location specified by the data address from L. The remainder is retained in L. If the remainder is less than -1 or greater than $1-2^{-31}$, overflow occurs and the Branch Control flip-flop B is turned on.

Throughout the execution of the SBL command U is circulated by:

$$U' = U\ \underline{H}\ Q_1\ Q_5 + \ldots$$

During phase 4, the contents of L become the I_1 signal:

$$I_1 = F\ \underline{H}\ Q_1\ Q_5\ (\underline{N}\ L + N\ L^*) + \ldots$$

At the same time, the contents of the memory location specified by the data address become the I_2 signal:

$$I_2 = F\ \underline{H}\ Q_1\ V + \ldots$$

During the execution of a subtract command, the S signal is true:

$$S = F\ \underline{H}\ Q_1\ Q_4 + \ldots$$

The combination of I_1 and I_2 determines the state of the A flip-flop. The A flip-flop is turned on by:

$$A' = \underline{I_1}\ I_2\ S\ Q_2\ \underline{t_6}\ G + \ldots$$

At sign time the A flip-flop is turned off by:

$$\underline{A}' = I_1\ \underline{I_2}\ S\ Q_2\ \underline{t_6}\ G + t_6\ F\ G\ \underline{H}\ Q_1 + \ldots$$

Thus, the A flip-flop is on at sign time only when there is a carry.

The remainder of the subtraction of V from L is recorded into L as the e_2 signal:

$$e_2 = A\ I_1\ I_2 + A\ \underline{I_1}\ \underline{I_2} + \underline{A}\ I_1\ \underline{I_2} + \underline{A}\ \underline{I_1}\ I_2 + \ldots$$

and L becomes:

$$L' = F\ G\ e_2\ Q_1\ Q_2\ Q_3\ Q_5 + \ldots$$

An overflow is sensed by the B flip-flop at sign time by:

$$B' = F\ G\ t_6\ Q_1\ Q_2\ Q_3\ (\underline{A}\ \underline{I_1}\ I_2\ S + A\ I_1\ \underline{I_2}\ S) + \ldots$$

Thus, the SBL command subtracts the contents of the memory location specified by the data address from L and turns the B flip-flop on if an overflow occurs.

4.10 RPC-4500 TAPE-TYPEWRITER SYSTEM--Communication between the Computer and the operator is carried out through the RPC-4500 Tape-Typewriter System. This system allows the operator to enter information in the form of commands or data into the computer. The information which the unit prints may be used as a permanent record of operations. The RPC-4500 Tape-Typewriter System is composed of the RPC-4430 Reader/Punch and the RPC-4480 Typewriter. Up to 60 input or output units may be connected to the computer through the RPC-4430 Reader/Punch (figure 4-26 and 4-27).

The reader/punch is designed to use one inch wide paper tape. Characters are represented by seven holes across the width of the tape. Six of the holes define the character, while the seventh hole is used for a parity bit to insure that there is an even number of holes representing each character.

The typewriter appears to the system as two devices, just as the reader/punch is two devices. It appears as an input device when an operator types information being received by the computer, and it appears as an output device when it accepts information from the computer to be transformed into printed copy. Characters are represented as the outputs of seven logic gates in the same binary code as the reader/punch tape holes.

The control panels on the RPC-4430 Reader/Punch allow the operator to interrupt or override computer control of input/output equipment. When the input/output system is not being used in conjunction with the computer the operator has autonomous control of the input/output equipment.

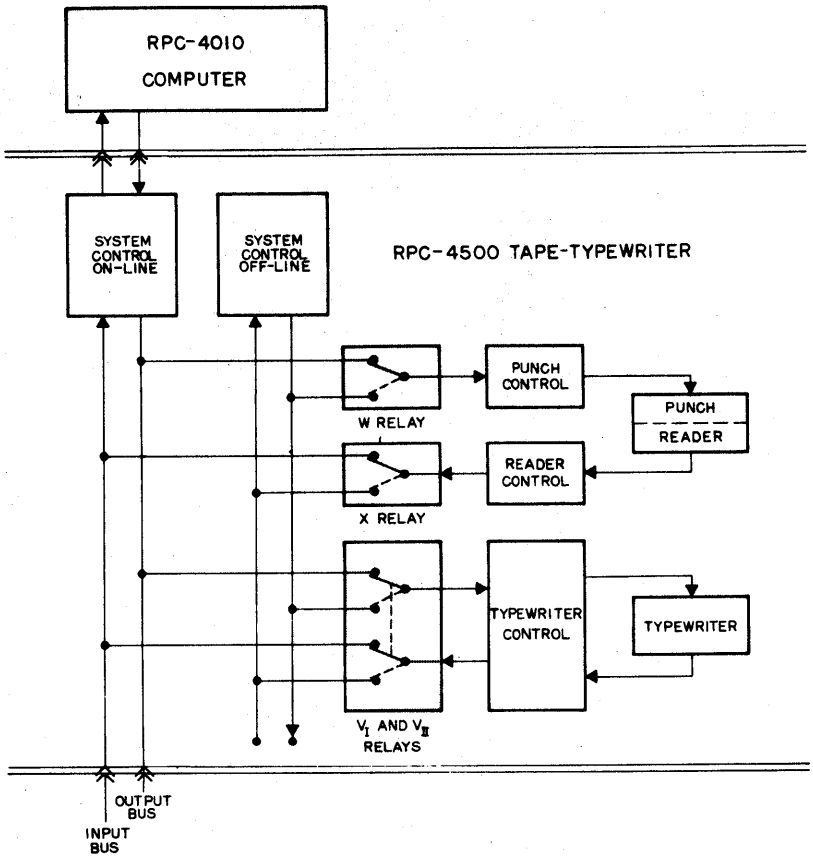


FIGURE 4-26 RPC 4500 TAPE TYPEWRITER SYSTEM

Operating on-line (with the computer) the input/output equipment responds to commands issued by the computer. The computer is capable of selecting specific devices with which to communicate. While only one input device may be selected for operation with the computer at any one time, several output devices can receive information from the computer simultaneously. Selections are made by the computer under program control, but the operator may intercede by means of the control panel.

Duplication of information entering the computer may be accomplished on selected output devices by use of Input Duplication mode. When devices are used simultaneously the speed of the system is that of the slowest operating device. For example, the reader will wait after presenting a character while the slower typewriter or punch duplicates the character.

The usual input to the computer consists of a group of characters followed by a code indicating the end of a word. The operator may select Single Character Input mode; in which only one character enters the computer each time the computer requests input. (Single Character Input mode cannot be used for data entry while the lower accumulator is in lengthened mode.)

On-line operation of the system provides a test for correct (even) parity. This function (Parity Monitor) may be inhibited manually by depressing the PARITY MONITOR INHIBIT switch on the control panel.

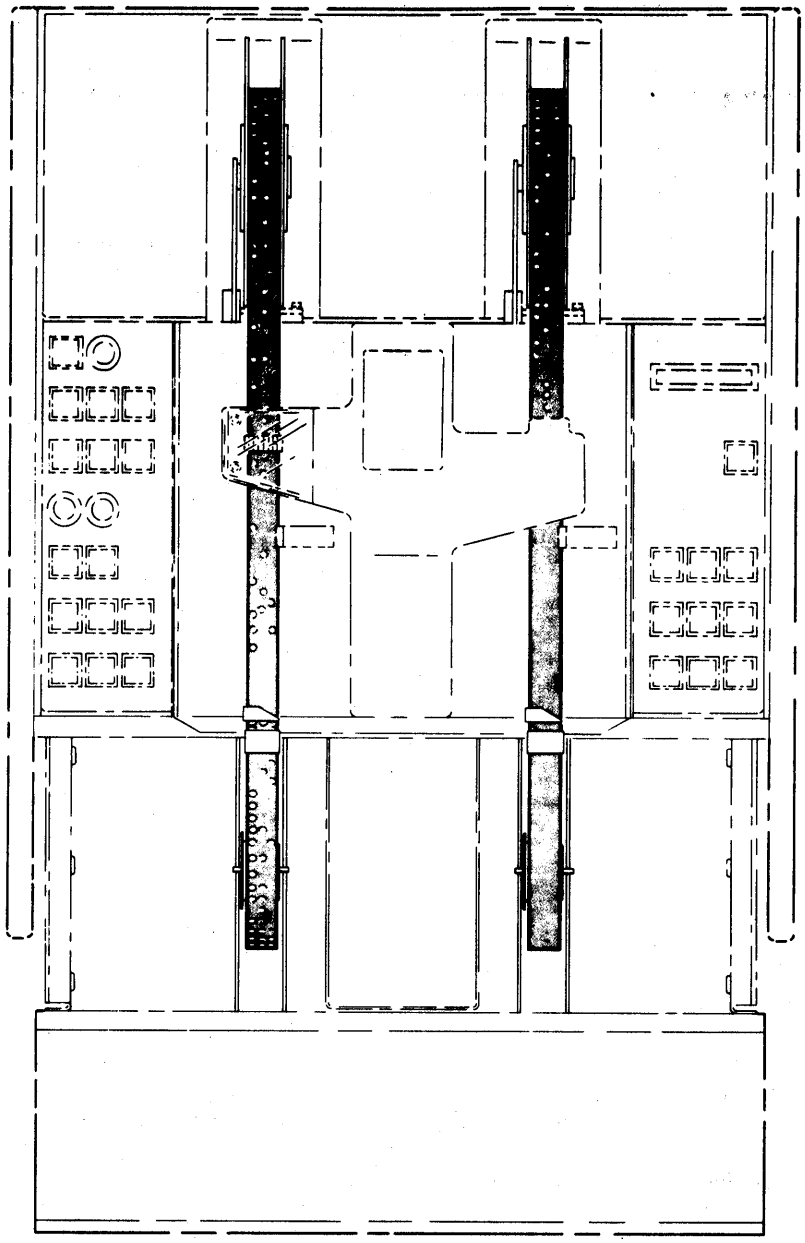


FIGURE 4-27 RPC 4430 READER/PUNCH

Off-line operation of the system incorporates many of the features of on-line operation. The typewriter, reader, and punch can be used off-line in any meaningful combination to prepare, examine, or modify tapes. In addition, when operating off-line the stop code may be ignored to allow tapes to be duplicated without initiating a read cycle each time this code is read.

4.10.1 SYSTEM CONTROL, ON-LINE

The system control (on-line) section functions as interpreter between the computer and input or output devices; no signals pass directly between the

computer and any device. This section synchronizes the activities of several simultaneously operating output devices and/or a single input device by checking the device "READY" signals (R). It then controls the computer accordingly with synchronizing signals (Z). Input and output characters are stored within this section in a set of 7 bit flip-flops (B). System Control also performs the function of controlling automatic (program controlled) selection of input and output devices by producing the SELECTION gate sampling pulse (S) after determining whether a character from the computer is to be used for output or selection. Signals pertinent to controlling devices and the input and output data are routed to devices via information bus lines. A parity check (for even parity) is made on all input information present on the bus lines so that any input device connected with the system uses the parity check feature. Different modes of operation can be set up by program control or through manipulation of the control panel. These various modes are handled by the system control section, and thus any device installed in the system can operate in these alternate modes. They are: Input Duplication (program selectable), Parity Monitor Inhibit, and Single Character Input (manually selectable). (4 bit or 6 bit input is determined within the computer.) The system can accommodate up to 60 devices utilizing the information bus lines, all devices being program selectable and monitored by system control (on-line).

4.10.2 SYSTEM CONTROL, OFF-LINE

This section is completely independent of the on-line system control section although it performs similar functions. This section does not communicate with the computer and the modes of operation must be manually selected. There is no parity check installed off-line. The off-line information busses driven and monitored by the computer accommodate only a typewriter and a reader/punch unit. Characters to be processed are stored in 7, tape hole, flip-flops (H). All necessary tape preparing and editing modes are provided.

4.10.3 DEVICE CONTROL

Practically any input or output device can be connected to the information bus lines from on-line system control, since sufficient control and data information is presented to or accepted by these lines. Input/output devices do differ in the power required to drive them, power level supplied, and in polarity (and sometimes duration) of signals. The function of the device control circuits is to accommodate any device to the information bus lines. There are also functions peculiar to individual devices which require internally generated or "shaped" signals; these are also formed by the device control circuits. Automatic selection of a device is accomplished with a circuit which is similar in each device (1 transistor and up to 8 components decode a selection pattern). This circuit usually sets (a simpler one resets) a selection flip-flop (Q). The B signals form a code which is sampled, using the selection signal (S). Input devices present character information (which sets B or H flip-flops) as B_1*-B_7* or H_1*-H_7* signals. Output devices accept character information from B or H signals. Either device presents "READY" synchronism signals (R). The output device "GO-AHEAD" signal (G) starts an output device cycling. The input device "ADVANCE" signal (A) initiates an input cycling. The signals A, B, B*, B_1*-B_7*, H*, H_1*-H_7*, P_1-P_5, and S, as well as K and U either from or to system control, are derived from on-line or off-line information bus lines. Character information is processed or transmitted only if a device is selected (on-line) when Q is true, or a device is selected off-line and it has been manually switched off-line. Only devices within the RPC-4500 and RPC-4600 can be manually

switched off-line. This operation switches device control to respond to off-line system control information bus lines (emanating from circuit cards 12 and 13), rather than on-line information bus lines.

4.11 RPC-4500 CONTROLS--The RPC-4480 Typewriter is equipped with three keys which perform special input/output functions. The BACKSPACE key normally backs the typewriter platen one character when depressed. When it is depressed while the SPECIAL key is held down, the tape in the punch section of the reader/punch is backed one character position at the same time the platen is backed. This is accomplished by completing the circuit through relay K-1 on the power control chassis (figure 4-28). Normally, X is used on the typewriter in its usual func-

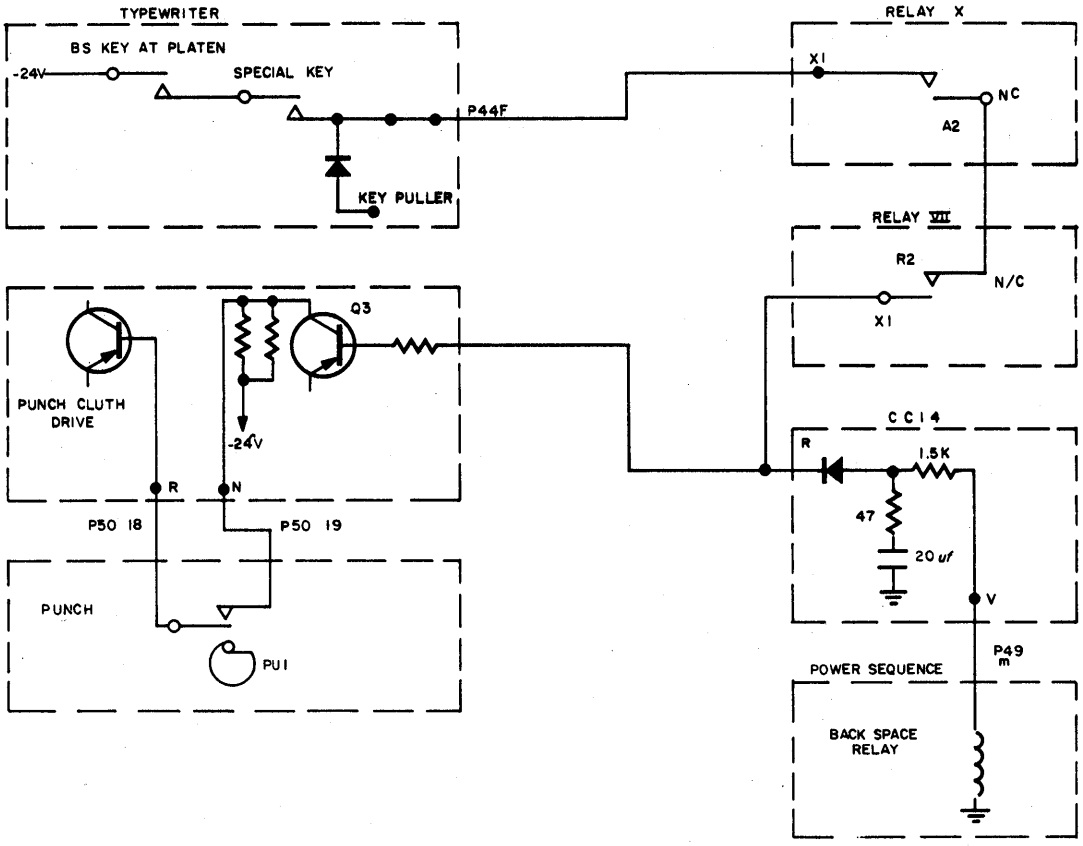
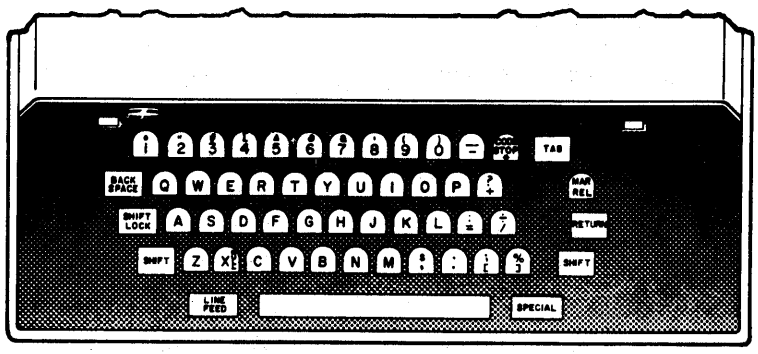


FIGURE 4-28 TAPE TYPEWRITER BACKSPACE CIRCUIT

tion. When pressed at the same time SPECIAL is held down, a NULL code is generated on the paper tape. The CODE STOP prints an asterisk and generates the stop code to stop the operation of an input device. The normal keys of the typewriter print their specific characters and generate the RPC-4010 binary code, available at the output of the typewriter (figure 4-29).

4.11.1 PRIMARY CONTROL PANEL

Control of all input/output equipment used with the RPC-4000 Computer System is accomplished manually by use of the RPC-4430 Reader/Punch control panels



NOTE: CHARACTER CODE TABLE 4-4

FIGURE 4-29 TYPEWRITER KEYBOARD

(figure 4-30). The primary control panel is located on the top right side of the unit. The switches on this panel are described as follows:

The SYSTEM POWER switch (figure 4-31) is a two-position, latching switch, which when depressed completes the AC power circuit to all system input and output equipment. When contacts 2 and 3 of the SYSTEM POWER switch are closed, the circuit through the coil of system power relay K-3 in the power control chassis is completed, energizing relay K-3 and completing the 115V, AC circuit to the power supply.

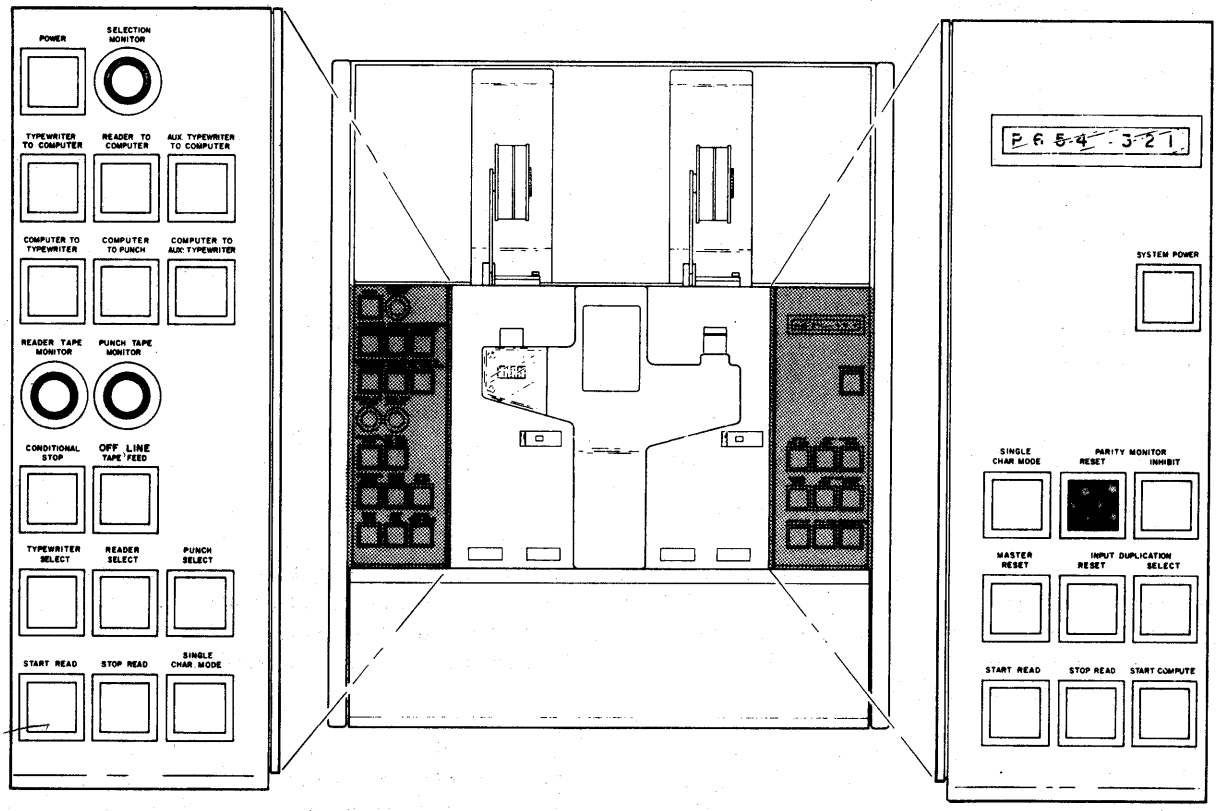


FIGURE 4-30 READER/PUNCH CONTROL PANELS

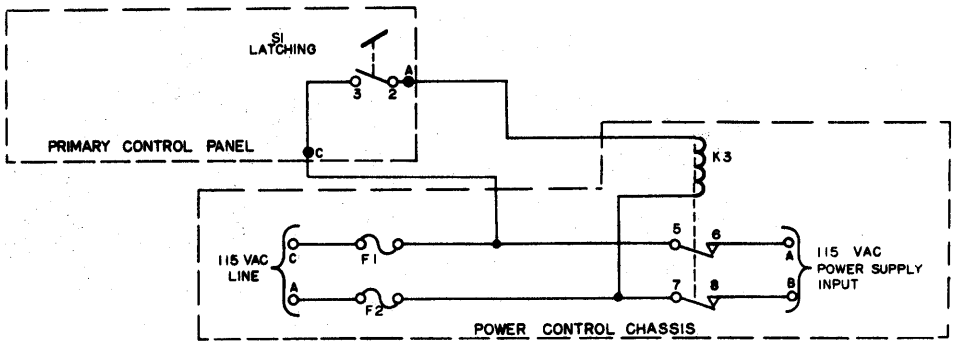


FIGURE 4-31 RPC 4500 SYSTEM POWER CIRCUIT

There are two PARITY MONITOR switches (figure 4-32). RESET, a two-position, non-latching switch, when depressed resets the parity error signal (E). This signal when true inhibits data flow. A parity error is indicated by a light in the RESET button. When contacts 1 and 2 of the RESET switch are opened, the B flip-flops are set and generate a correct parity code. (This code is B_1 B_2 B_3 B_4 B_5 $\underline{B}_6$ B_7.)

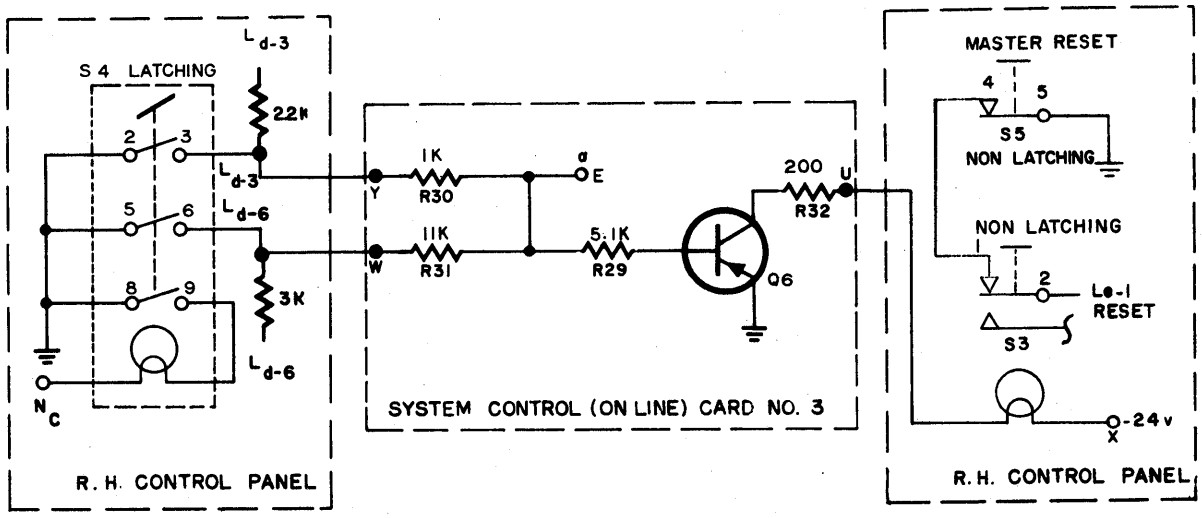


FIGURE 4-32 PARITY MONITOR RESET AND INHIBIT CIRCUITS

Before a parity error can be detected, the system is committed to process the character. The computer will receive the error character, unless it is a stop code. To reset the error signal and resume operation, the STOP READ switch should be depressed and the error corrected prior to the PARITY MONITOR RESET switch being pressed.

INHIBIT, a two-position, latching switch, when depressed overrides the results of parity checking of input data. When contacts 2 and 3 of the INHIBIT switch are closed the start signal (Z_S) is unaffected by E. When contacts 5 and 6 are closed the synchronizing signal (Z_r) is unaffected by E, allowing data to

be read regardless of the state of E. Contacts 8 and 9 of the INHIBIT switch complete the circuit to the light, which is illuminated when the switch is depressed.

The MASTER RESET switch (figure 4-33), a two-position, non-latching switch, when depressed disconnects all input/output units from the computer. When contacts 4 and 5 of the MASTER RESET switch are opened, the B flip-flops are set to the code B_1 B_2 B_3 B_4 B_5 $\underline{B_6}$ B_7 which allows the UNSELECT signal (U) to go true. Also, the ground to Q_7 on system control card #5 is opened and the SELECT signal (S) goes true, enabling the selection gate at each output device to be reset by the logic term SU. Input device selection is reset by the logic term B_6 S.

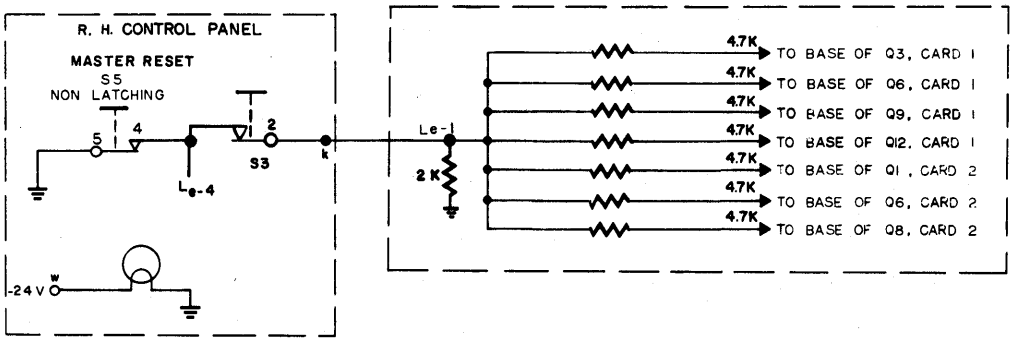


FIGURE 4-33 MASTER RESET CIRCUIT

There are two INPUT DUPLICATION switches (figure 4-34). SELECT, a two-position, non-latching switch, when depressed sets the RPC-4500 Tape-Typewriter to the input duplication mode. When contacts 1 and 2 of the SELECT switch are opened, the input copy mode flip-flop (C) on system control card #4 is set true. RESET, a two-position, non-latching switch, when depressed stops the RPC-4500 Tape-Typewriter input duplication mode. When the RESET switch is depressed contacts 1 and 2 are opened, and the input copy mode flip-flop (C) on system control card #4 is set false.

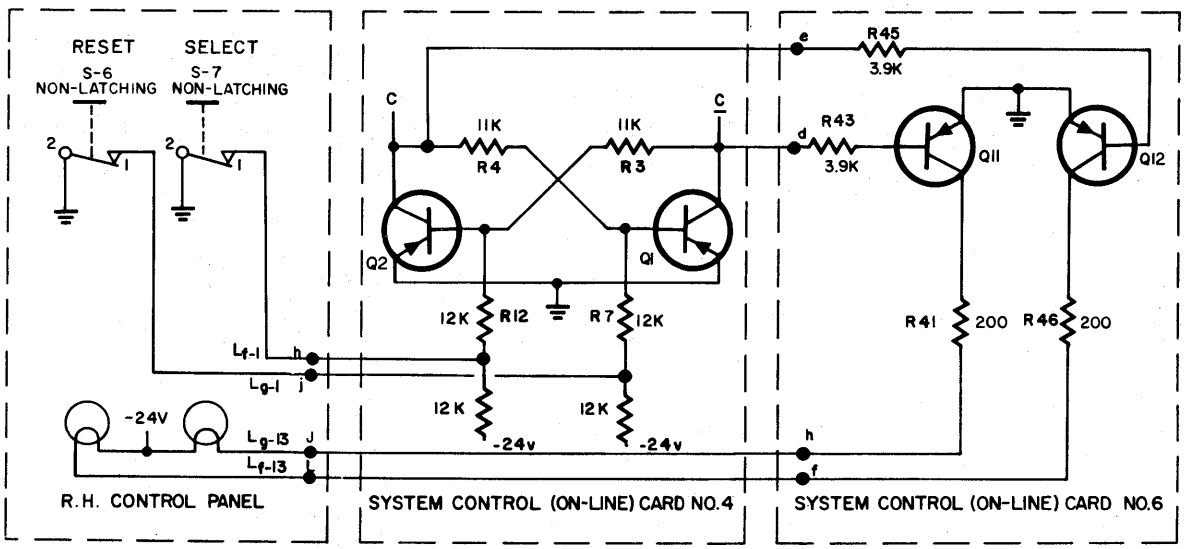


FIGURE 4-34 INPUT DUPLICATION SELECT AND RESET CIRCUITS

The START READ switch (figure 4-35), a two-position, non-latching, shorting (make before break) switch, when depressed and subsequently released initiates operation of the selected input device. When contacts 2 and 3 are closed, the synchronizing READY signal (Z_r) is held false, inhibiting operation. When contacts 1 and 2 open, signal L_{h-1} goes true, turning on the input flip-flop (I_c).

The STOP READ switch, a two-position, non-latching switch, when depressed stops the operation of the selected input device. When contacts 1 and 2 on the STOP READ switch are opened, the input flip-flop (I_c) on system control card #5 is set false by the L_{i-1} signal, which stops the input of data to the computer.

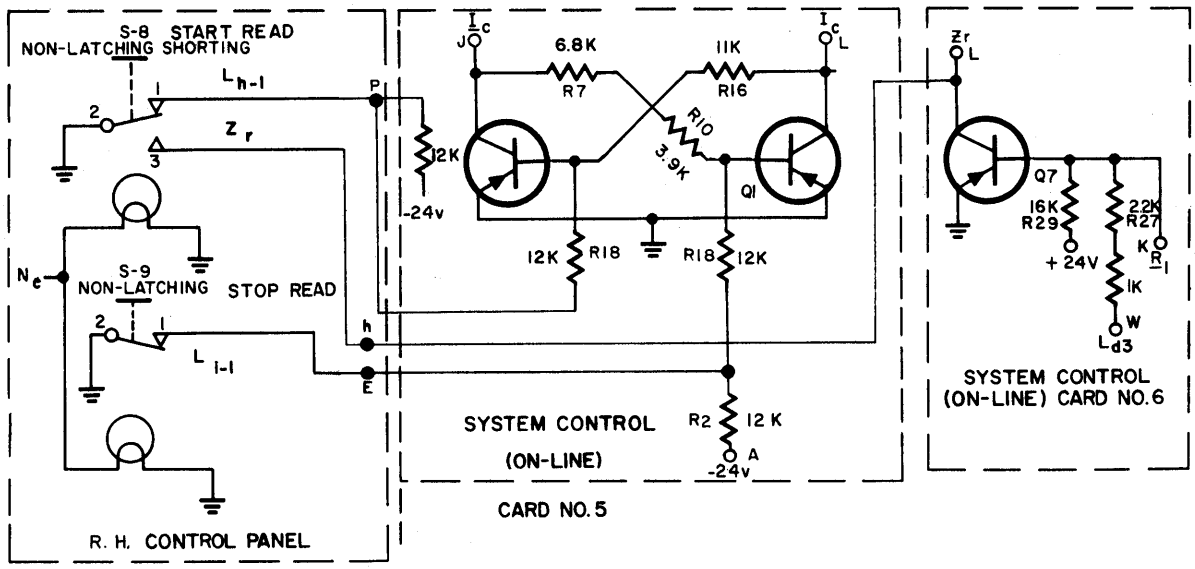


FIGURE 4-35 START READ AND STOP READ CIRCUITS (ON-LINE)

The START COMPUTE switch (figure 4-36), a two-position, non-latching, shorting (make before break) switch, when depressed and subsequently released sets the computer to compute mode. When contacts 2 and 3 of the START COMPUTE switch are closed, the INPUT-ENABLE-COMPUTE signal (Z_i) to the computer is held false. When contacts 1 and 2 open, the START COMPUTE signal (Z_s) is forced true. The computer cannot proceed until contacts 2 and 3 re-open.

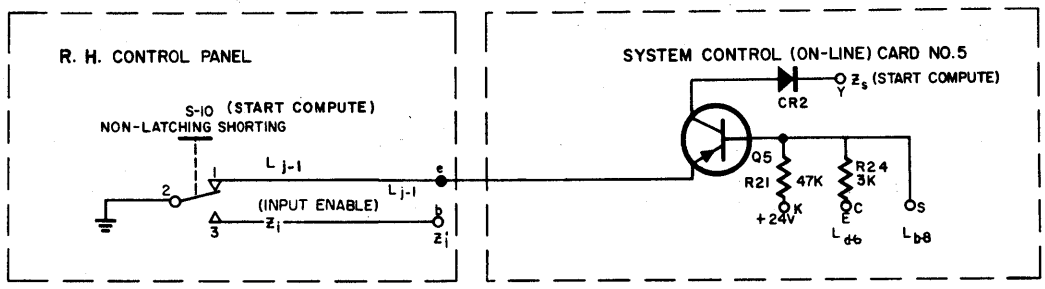


FIGURE 4-36 START COMPUTE CIRCUIT

The SINGLE CHARACTER MODE switch (figure 4-37), a two-position, latching switch, when depressed causes the input device to halt and the computer to go into compute mode after a single character entry. In this mode, the computer can receive any character presented. (Normally, character codes less than 16 in binary value are inhibited from entering the computer.) This mode cannot be used for data entry when the computer is in lengthened mode. When contacts 2 and 3 of the SINGLE CHARACTER MODE switch are closed the INPUT BEGIN signal (Z_b) is routed to turn I_c off. When contacts 4 and 5 are opened, Z_b is allowed to go true for any character. When contacts 8 and 9 are closed the START COMPUTE signal (Z_s) generated by transistor Q_5 on system control card #5, is controlled by signal (M), derived from a one-shot multivibrator on system control card #4, rather than by the stop code. "Meter Pulse input signal"

There are seven character indicator lights on the primary control panel. These lights are designated P, 6, 5, 4, 3, 2, and 1 and are illuminated to indicate the next character code to be read by the paper tape in the RPC-4430. The signals to these lamps are generated by the transistors Q_3 through Q_9 on reader control card #7, and are a reading of the reader brushes.

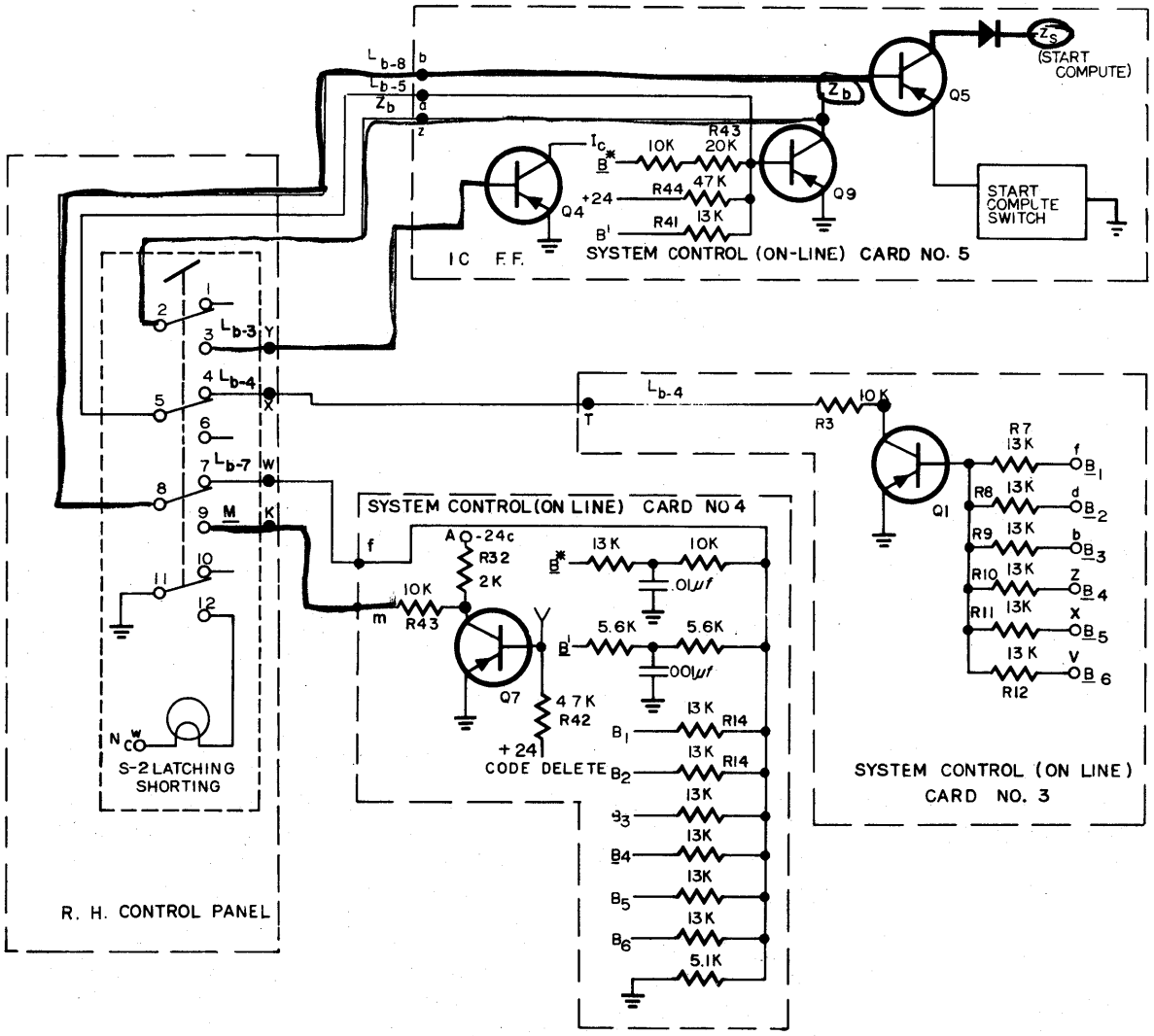


FIGURE 4-37 SINGLE CHARACTER MODE CIRCUIT (ON-LINE)

4.11.2 AUXILIARY CONTROL PANEL

The auxiliary control panel is located on the top left side of the RPC-4430 Reader/Punch unit. The switches on this panel are described as follows:

The POWER switch (figure 4-38), a two-position, latching switch, when depressed applies AC power to the RPC-4500 Tape-Typewriter System devices. When contacts 2 and 3 of the POWER switch are closed, the circuit through device power relay K-2 on the power control chassis is completed. Contacts 3 and 4 of the device power relay complete the AC power circuit to the reader/punch and the typewriter. Contacts 5 and 6, 7 and 8, and 9 and 10 route the DC voltage to the reader/punch and the typewriter and their device control circuit cards.

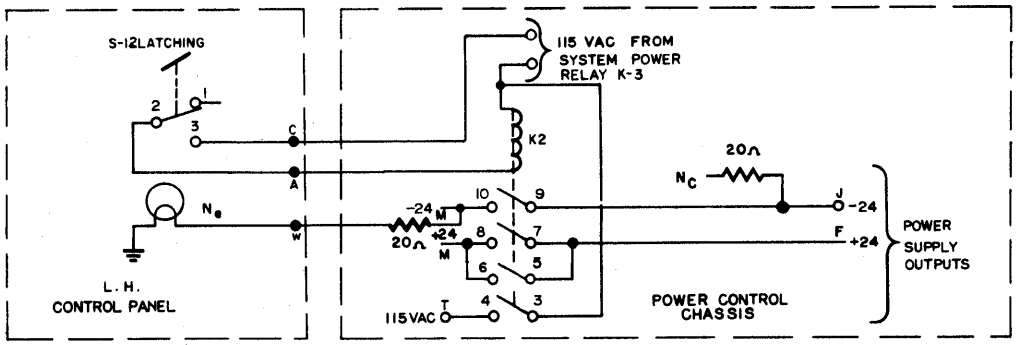


FIGURE 4-38 RPC 4500 UNIT POWER CIRCUIT

A SELECTION MONITOR light (figure 4-39) is provided which when illuminated indicates that an on-line input or output device is operating off-line. The circuit to the SELECTION MONITOR light is completed by any one of the input or output device selection flip-flops being set true.

The TYPEWRITER TO COMPUTER switch (figure 4-40), a two-position, non-latching switch, when depressed establishes the typewriter to computer interconnection. It is illuminated to indicate that the typewriter has been selected on-line as the input device. When contacts 1 and 2 of the TYPEWRITER TO COMPUTER switch are opened, the signal L_{m-1} goes true, turning on the typewriter select flip-flop (Q_i) on card #14, enabling the typewriter to operate as an input device.

The READER TO COMPUTER switch (figure 4-41), a two-position, non-latching switch, when pressed establishes the paper tape reader to computer interconnection. It is illuminated to indicate that the paper tape reader has been selected on-line as the input device. When contacts 1 and 2 of the READER TO COMPUTER switch are opened, the signal L_{n-1} goes true, turning on the reader select flip-flop (Q_r) on card #8, enabling the paper tape reader to operate on-line.

The AUX TYPEWRITER TO COMPUTER switch (figure 4-42), a two-position, non-latching switch, when pressed establishes the auxiliary typewriter to computer interconnection. It is illuminated to indicate that the auxiliary typewriter has been selected on-line as the input device. When contacts 1 and 2 of the AUX TYPEWRITER TO COMPUTER switch are opened, the signal L_{o-1} goes true, turning on the auxiliary typewriter select flip-flop (Q_y) on card #14 (at card position 29), enabling the typewriter to operate as an input device.

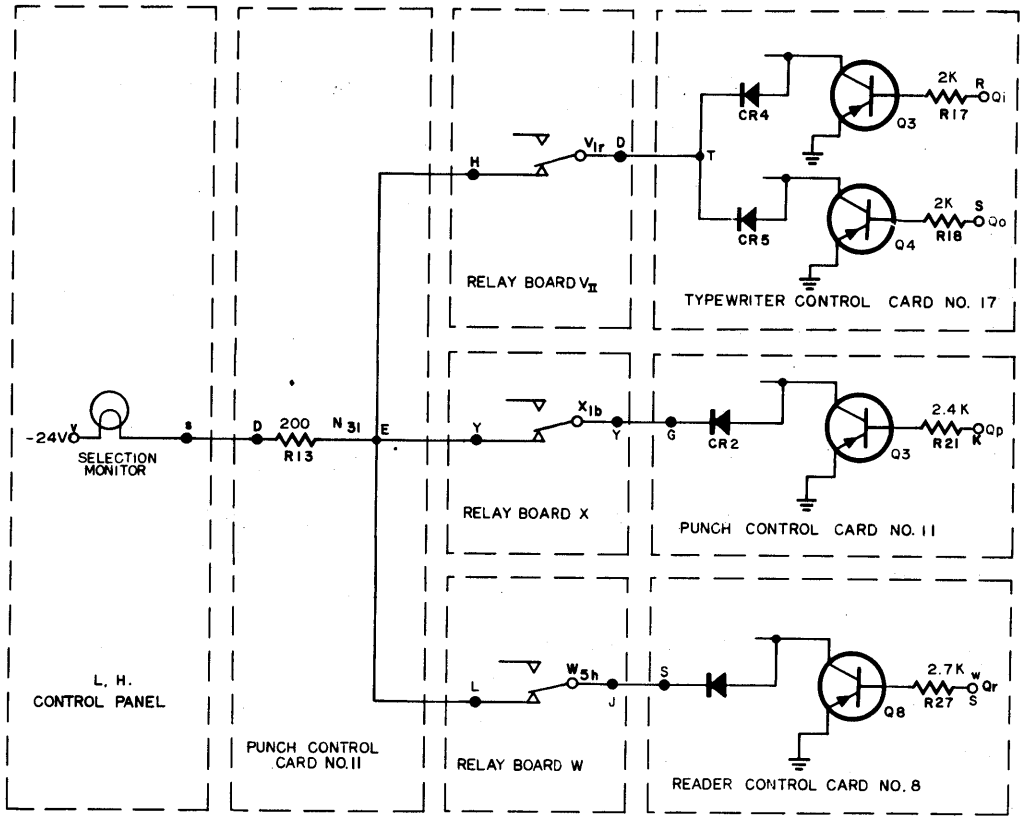


FIGURE 4-39 SELECTION MONITOR CIRCUIT

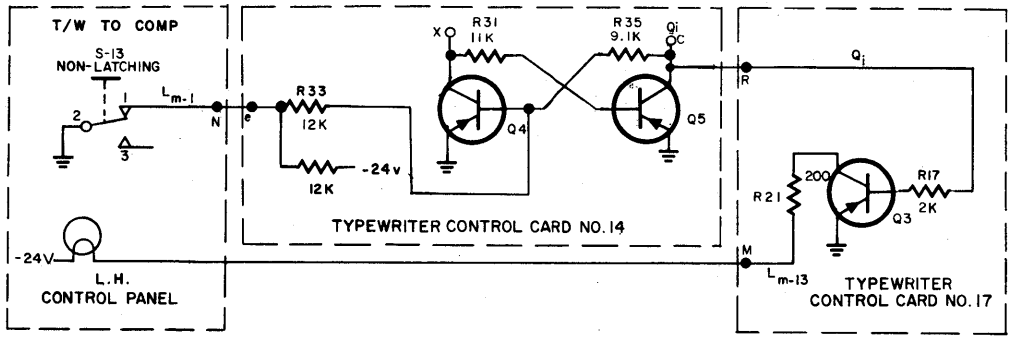


FIGURE 4-40 TYPEWRITER TO COMPUTER CIRCUIT

The COMPUTER TO TYPEWRITER switch (figure 4-43), a two-position, non-latching switch, when depressed establishes the computer to typewriter interconnection. It is illuminated to indicate that the typewriter has been selected on-line as an output device. When contacts 1 and 2 of the COMPUTER TO TYPEWRITER switch are opened, the signal L_{p-1} goes true, turning on the typewriter select flip-flop (Q_o) on card #17, enabling the typewriter to operate as an output device.

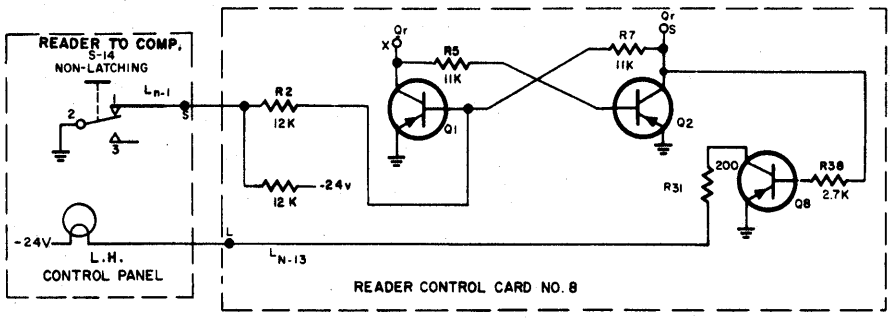


FIGURE 4-41 READER TO COMPUTER CIRCUIT

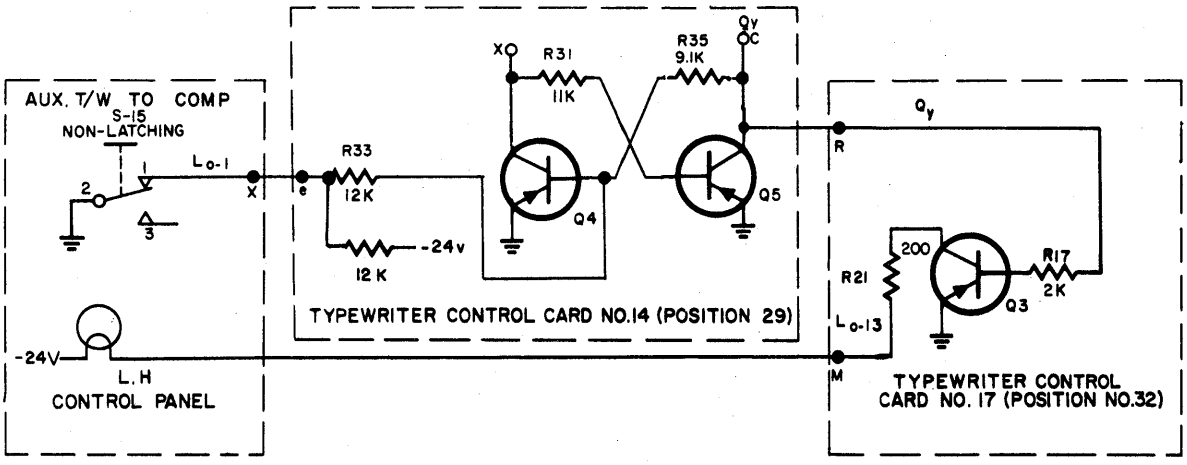


FIGURE 4-42 AUXILIARY TYPEWRITER TO COMPUTER CIRCUIT

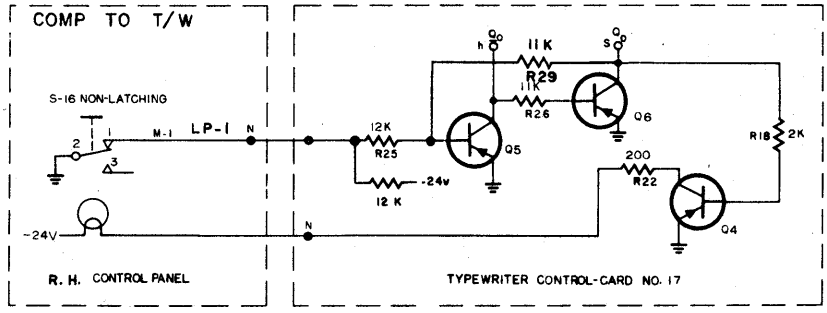


FIGURE 4-43 COMPUTER TO TYPEWRITER CIRCUIT

The COMPUTER TO PUNCH switch (figure 4-44), a two-position, non-latching switch, when depressed establishes the computer to paper tape punch interconnection. It is illuminated to indicate that the paper tape punch has been selected as an output device. When contacts 1 and 2 of the COMPUTER TO PUNCH switch are opened, the signal L_{q-1} goes true, turning on the punch select flip-flop (Q_p) on card #11, enabling the paper tape punch to operate as an output device.

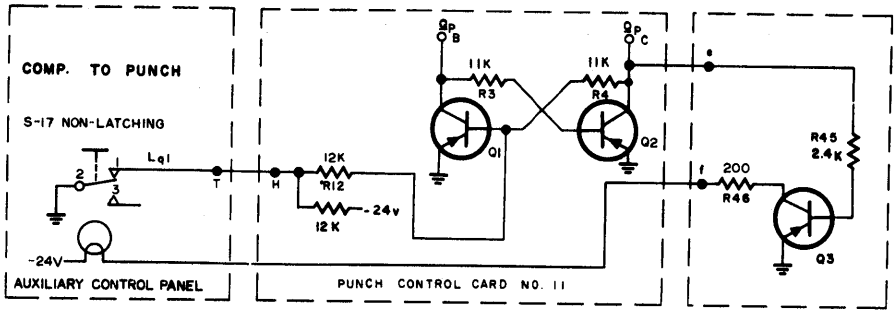


FIGURE 4-44 COMPUTER TO PUNCH CIRCUIT

The COMPUTER TO AUX TYPEWRITER switch (figure 4-45), a two-position, non-latching switch, when depressed establishes the computer to auxiliary typewriter interconnection. It is illuminated to indicate that the auxiliary typewriter has been selected as an output device. When contacts 1 and 2 of the COMPUTER TO AUX TYPEWRITER switch are opened, the auxiliary typewriter select flip-flop (Q_z) on card #17 (at card position 32) is set, enabling the auxiliary typewriter to operate as an output device.

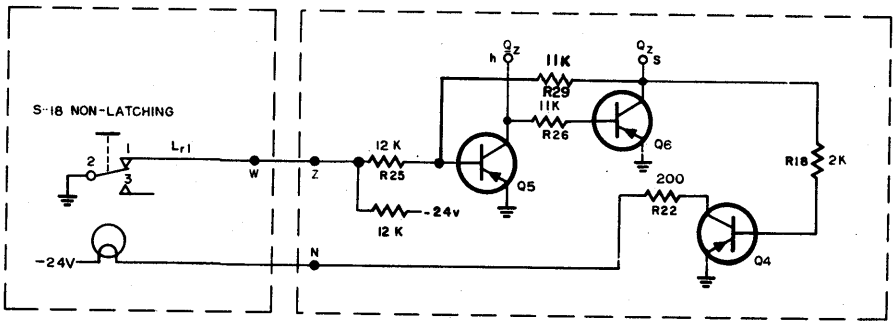


FIGURE 4-45 COMPUTER TO AUXILIARY TYPEWRITER CIRCUIT

The READER TAPE MONITOR light (figure 4-46) is illuminated when the paper tape reader is out of tape, or when the tape is jammed. When tape trouble occurs, the reader if selected will stop and halt system operation until the trouble is corrected.

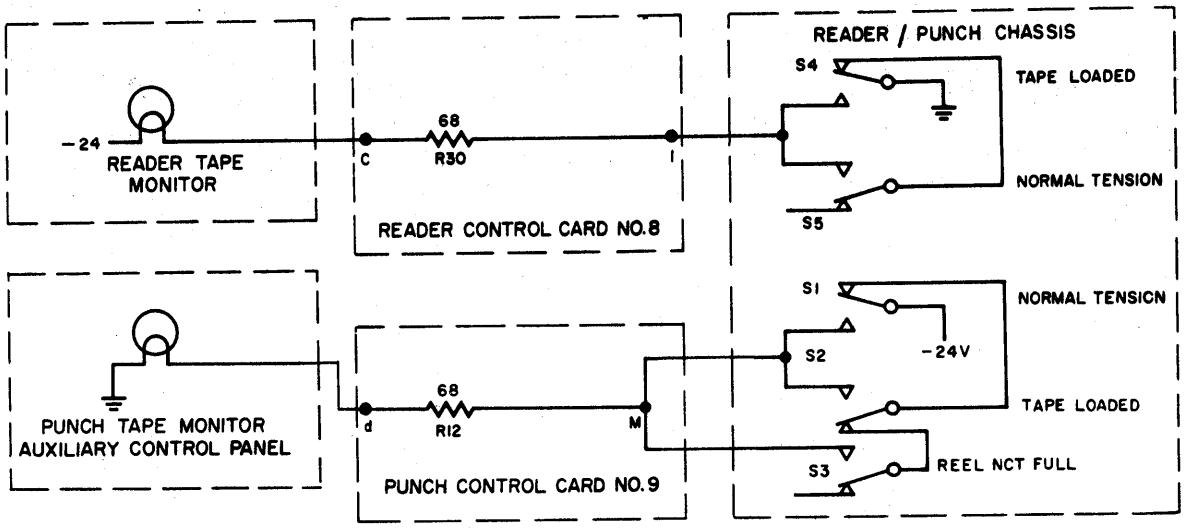


FIGURE 4-46 TAPE MONITOR CIRCUITS

4.11.3 OFF-LINE CONTROL

The following switches are used to control off-line operations:

The CONDITIONAL STOP switch (figure 4-47), a two-position, latching switch (illuminated when depressed), when depressed allows the off-line system to continue although a stop code character has been sensed. When it is not depressed, the system requires that the START READ switch be depressed following a stop code. Similarly, the SINGLE CHARACTER MODE switch is ignored when the CONDITIONAL STOP switch is depressed. At this time, contacts 2 and 3 close, causing transistor Q_6 on card #12 to conduct, which holds $\underline{I_m}'$ false, inhibiting turn off of the I_m flip-flop.

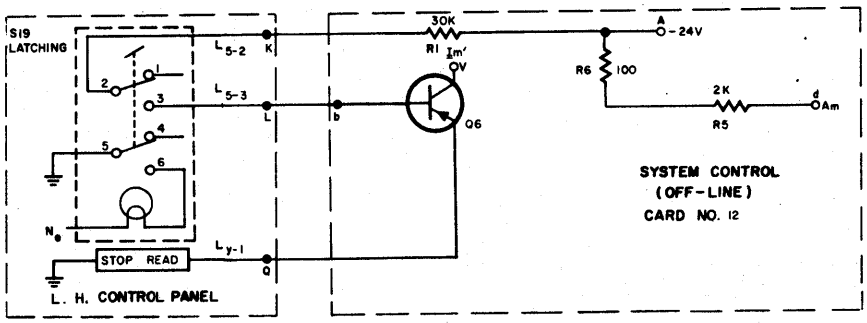


FIGURE 4-47 CONDITIONAL STOP CIRCUIT

The TAPE FEED switch (figure 4-48), a two-position, non-latching switch, when depressed causes the paper tape punch to punch tape feed holes if the PUNCH SELECT switch is depressed. When contacts 2, 3, 5, and 6 of the TAPE FEED switch

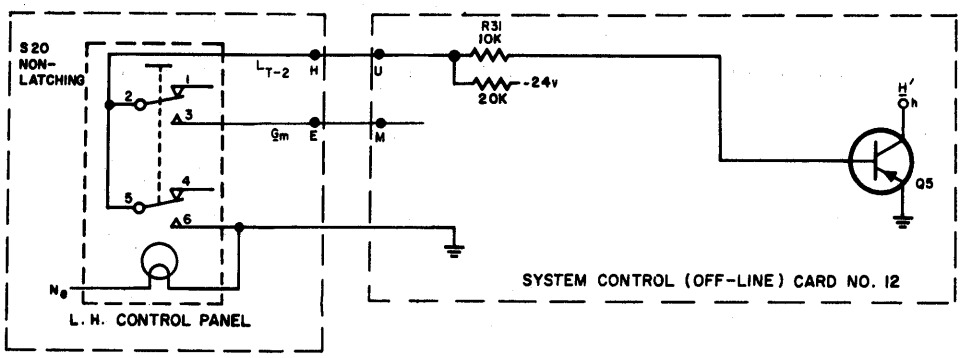


FIGURE 4-48 TAPE FEED CIRCUIT

are closed, the H' and G_m signals are produced, forcing the H flip-flops false and causing the punch to cycle.

The TYPEWRITER SELECT switch (figure 4-49), a two-position, latching switch, when depressed releases the typewriter from the on-line system, allowing off-line operation. When contacts 4 and 5 of the TYPEWRITER SELECT switch open, the relays on relay cards V_I and V_{II} release, and switch the typewriter inputs and outputs to off-line system control. Closure of contacts 2 and 3 causes the on-line signals A_p and Q_i to be ignored. When contacts 1 and 2 open, O_t is held off unless READER SELECT is depressed.

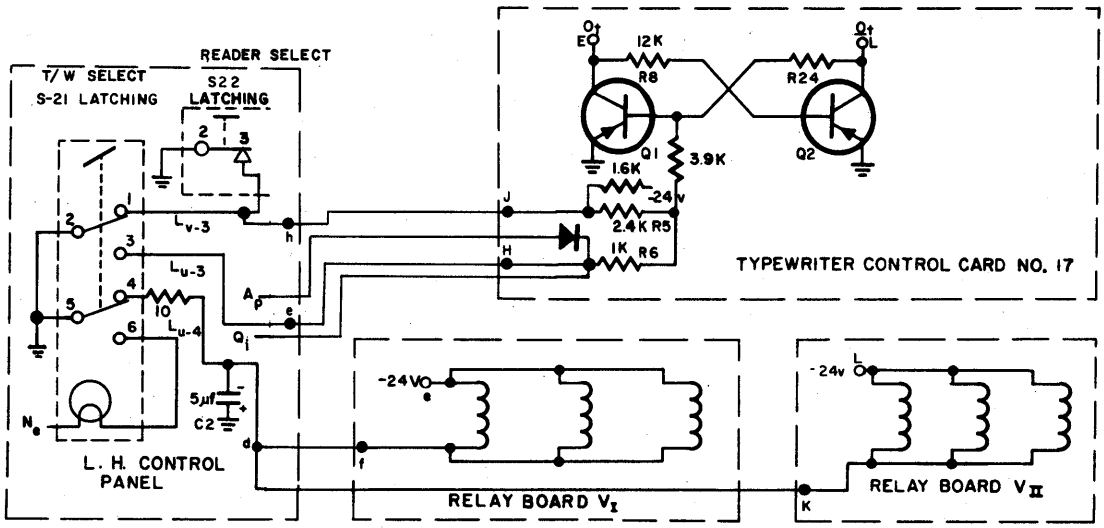


FIGURE 4-49 TYPEWRITER SELECT CIRCUIT

The PUNCH SELECT switch (figure 4-50), a two-position, latching switch, when depressed disconnects the paper tape punch from the on-line system, allowing off-line operation. When contacts 1 and 2 of the PUNCH SELECT switch are opened, the relays on relay card X release and switch the punch from on-line to off-line system control.

The READER SELECT switch (figure 4-51), a two-position, latching switch, when depressed disconnects the paper tape reader from the on-line system, allowing

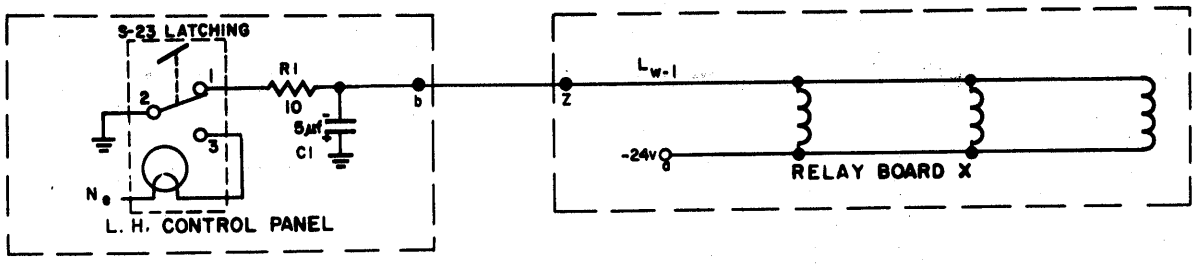


FIGURE 4-50 PUNCH SELECT CIRCUIT

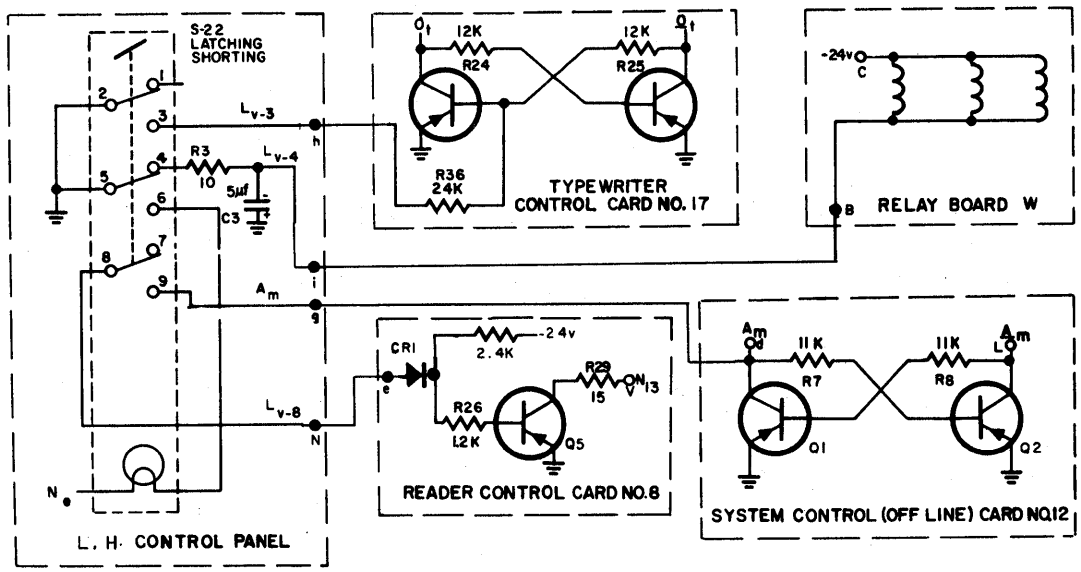


FIGURE 4-51 READER SELECT CIRCUIT

off-line operation. When contacts 2 and 3 close, the typewriter output flip-flop (O_t) on card #17 is no longer held off (while the typewriter is off-line). Contacts 4 and 5 open to remove ground from relay coils on relay board W which release, and switch the reader from on-line to off-line system control. Contacts 7 and 8 are opened and contacts 8 and 9 are closed, switching reader control signals (A_p and A_m) from computer to manual (off-line) control.

The START READ switch (figure 4-52), a non-latching, shorting (make before break), momentary switch, when depressed and subsequently released initiates operation of the typewriter or the tape reader when in the off-line mode. When contacts 1 and 2 of the START READ switch are opened, the input flip-flop (I_m) on card #12 is set true. When contacts 2 and 3 are closed, advance flip-flop (A_m) is held off by making the signal R_5 false, inhibiting a read cycle until the switch is released.

The STOP READ switch, a two-position, non-latching switch, when depressed stops operation in the off-line mode. When contacts 1 and 2 are opened, the input flip-flop (I_m) on card #12 is turned off.

The SINGLE CHARACTER MODE switch (figure 4-53), a two-position, latching switch, when depressed causes the paper tape reader (or typewriter) to stop after

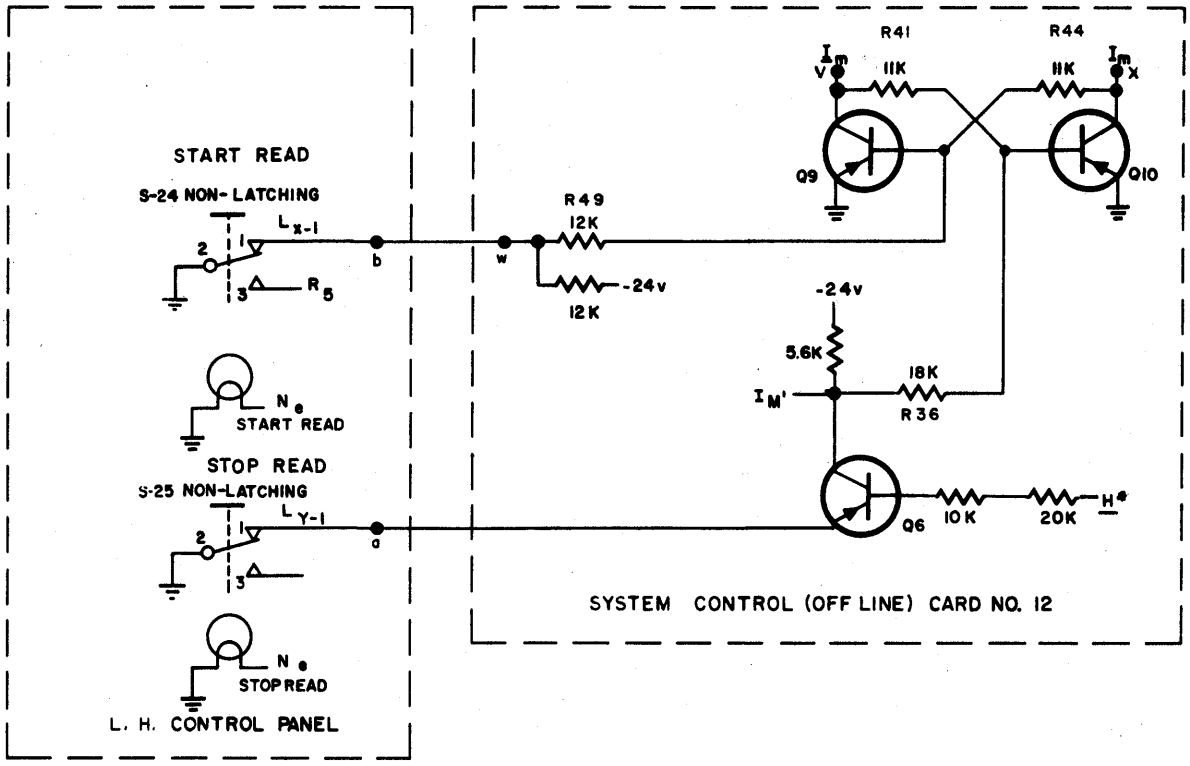


FIGURE 4-52 START READ/STOP READ CIRCUITS (OFF-LINE)

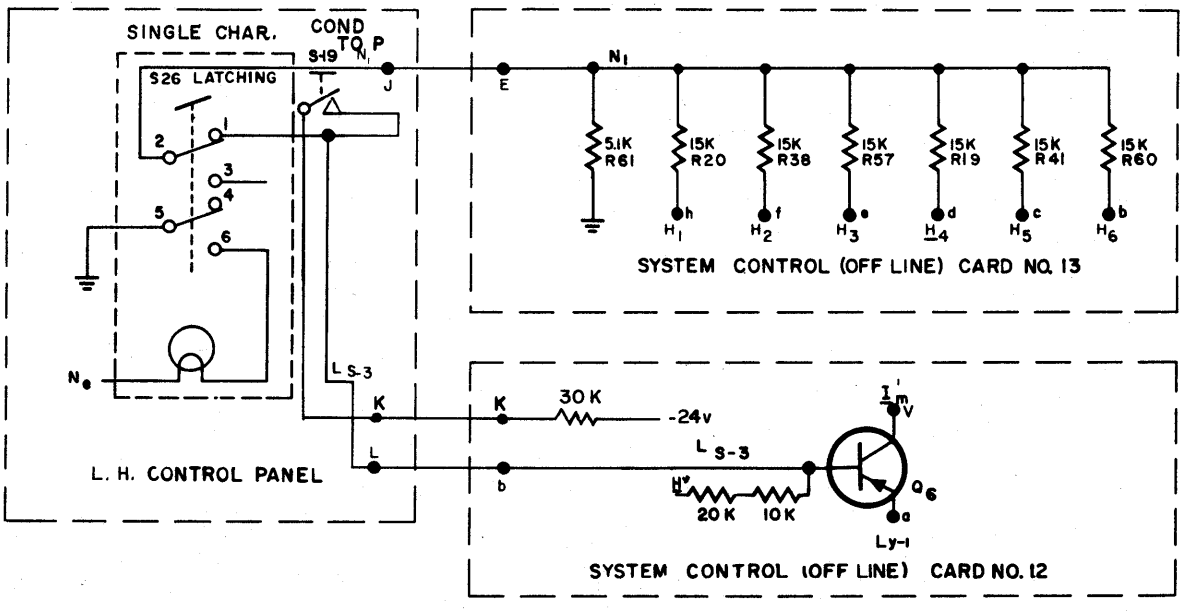


FIGURE 4-53 SINGLE CHARACTER MODE CIRCUIT (OFF-LINE)

each character is read. In this mode, each depression of the START READ switch initiates the reading of one character with the reader in the off-line mode. When contacts 1 and 2 of the SINGLE CHARACTER MODE switch are opened, the input flip-flop (I_m) on card #12 will be set off each time the input signal (H*) is true, causing the reader to read one character each time the START READ switch is pressed. The CONDITIONAL STOP switch overrides the function of the SINGLE CHARACTER MODE switch.

Synchronizing signals to the computer are used to coordinate input and output of information and indicate the state of the various input and output devices. The START COMPUTE signal (Z_s) (figure 4-54) is generated by pressing the START COMPUTE pushbutton, by a stop code with the PARITY MONITOR INHIBIT pushbutton depressed (L_d), or no parity error (E) and not in single character mode:

$$Z_s = (L_d + E) \quad \underline{L}_b \, \underline{B}_1 \, \underline{B}_2 \, \underline{B}_3 \, \underline{B}_4 \, \underline{B}_5 \, \underline{B}_6 \, (\underline{B}') \, B^* + L_b \, M \quad + L_j$$

The READY synchronism signal (Z_r) (figure 4-55) is generated by an output device READY signal (R_1), the start read pushbutton not depressed ($\underline{L}_h$) and no parity error ($\underline{E}$), or the PARITY MONITOR INHIBIT pushbutton depressed (L_d).

$$Z_r = R_1 \, \underline{L}_h \, (\underline{E} + L_d)$$

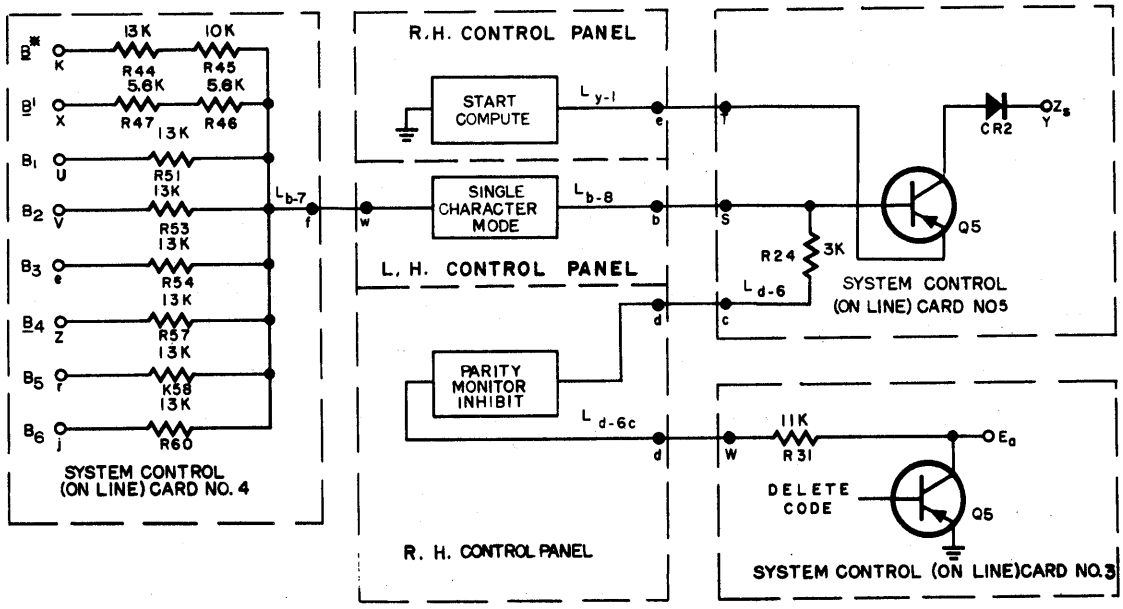


FIGURE 4-54 START COMPUTE SIGNAL

4.12 READER INPUT--The reader control circuit cards in the RPC-4500 Tape-Typewriter control the functions of the paper tape reader both on-line and off-line. The reader select flip-flop (Q_r) is turned on by a select code from the computer or by the READER TO COMPUTER switch (figure 4-56) on the auxiliary control panel. The B_{3p}, B_{4p}, B_{5p}, and B_{6p} signals (power outputs of the B flip-flops) are combined in a resistor-transistor NOR gate; if any one of these signals is true, the gating transistor (Q3) is saturated and its output is false. With all the above mentioned B signals false, the S signal is not blocked by transistor Q3 and it saturates the transistor Q1 grounding the $\underline{Q}_r$ signal, and sets Q_r true. When the READER TO COMPUTER switch is pressed, the ground which holds signal

L_{n-1} false is removed, and Q_1 is saturated grounding the base of Q_2 and turning the Q_r flip-flop on.

$$Q_r' = S\ \underline{B}_3\ \underline{B}_4\ \underline{B}_5\ \underline{B}_6 + L_n$$

The reader select flip-flop is turned off by the select signal and any one of the B_{3p} B_{4p} or B_{5p} signals being true, combined with B_{6p} being false. This grounds the base of transistor Q_4 and causes the S signal to saturate Q_2 holding Q_r false, resetting the Q_r flip-flop. As the READER SELECT switch (L_v) is pressed, the Q_r flip-flop is reset by a signal from the reader off-line relay (W_{14b}), which saturates transistor Q_2.

$$\underline{Q}_r' = S\ \underline{B}_6\ \underline{(Q_r')} = \underline{\frac{d}{dt}}\ L_v \quad \text{(leading)}$$

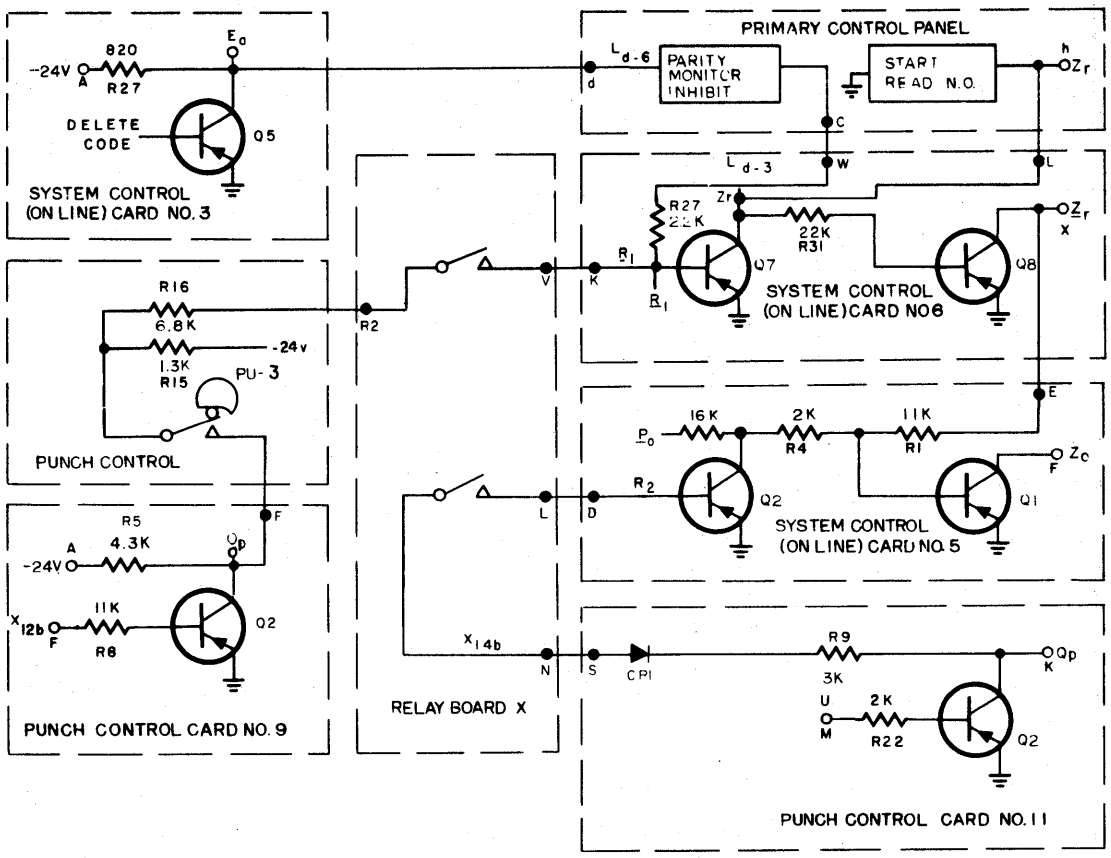


FIGURE 4-55 SYNCHRONIZING SIGNALS (Z_r, R_1, Z_o, R_2)

The on-line system control section also generates the signals which control the input and output functions of all on-line input and output equipment. The input, or read, mode is indicated by the input flip-flop (I_c). During phase 4 of the first cycle of an INPUT command the computer produces the signal Y_i.

$$Y_i = (F\ G + H)\ \underline{Q}_1\ Q_2\ \underline{Q}_3\ \underline{Q}_4\ \underline{Q}_5\ \underline{M}$$

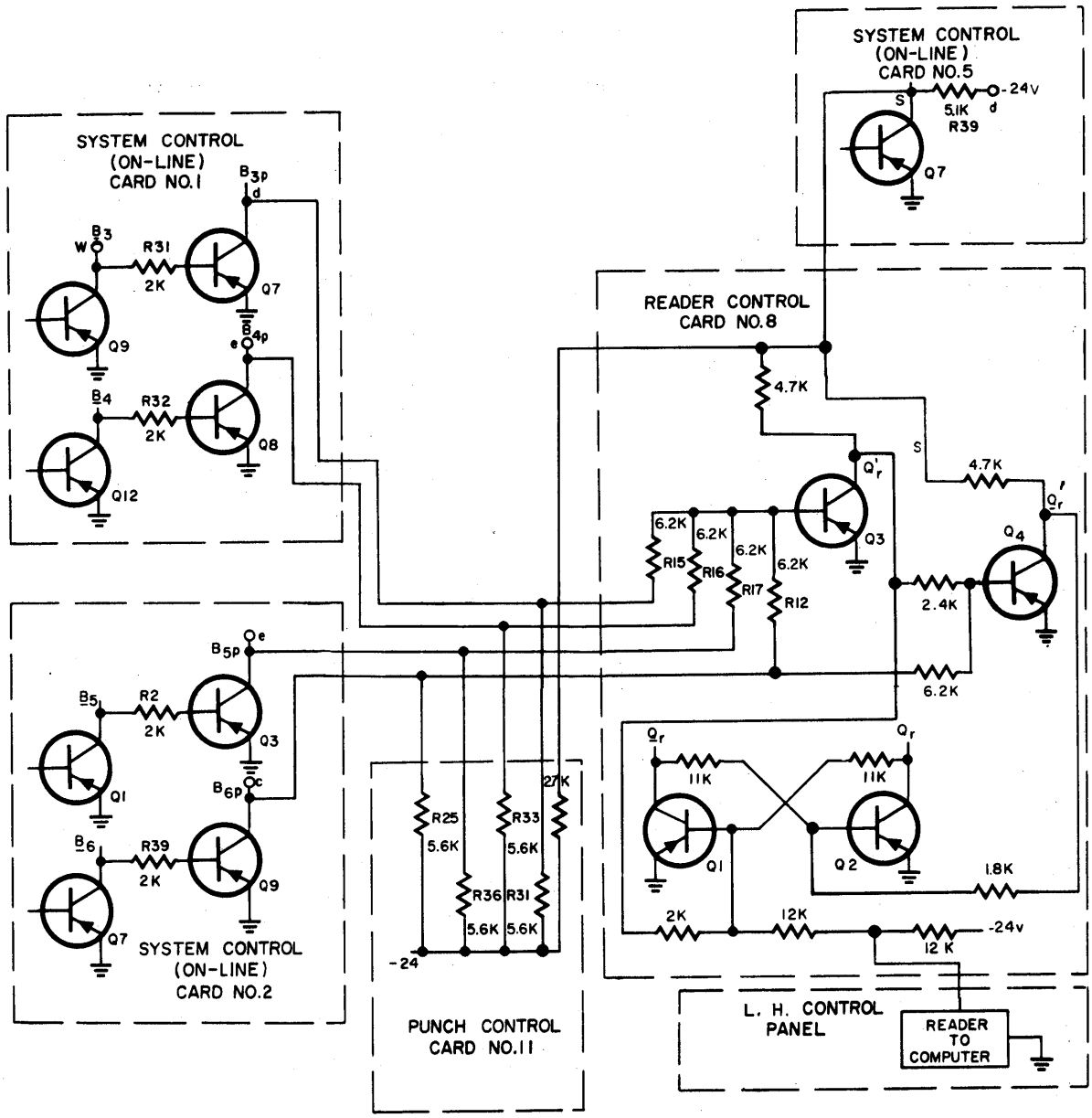


FIGURE 4-56 READER SELECT (Q_r)

The signal $\underline{Y_i}$ is routed to the I_c flip-flop through a diode so that when $\underline{Y_i}$ goes false Q_4 is cut off, allowing I_c to go true, which holds the $\underline{I_c}$ signal to ground. When the START READ switch on the primary control panel is depressed a negative voltage saturates the off side transistor of the I_c flip-flop, grounding the $\underline{I_c}$ signal and causing I_c to go true (figure 4-57). The logic which turns I_c on is:

$$I_c' = Y_i + L_h$$

The input flip-flop is turned off by a START COMPUTE signal (Z_s) to the computer which saturates the on side transistor and holds I_c to ground. It may also be turned off by a SELECT signal (S) which drives the on side transistor into saturation and grounds the I_c signal. When the SINGLE CHARACTER MODE switch

on the primary control panel is depressed and a character is being presented for input (indicated by Z_b) I_c will be turned off. The STOP READ switch on the primary control panel will turn I_c off also, by allowing the $\underline{I_c}$ transistor to saturate and ground the I_c signal. The logic which controls the above operations is:

$$\underline{I_c}' = Z_s + S + Z_b L_b + L_i$$

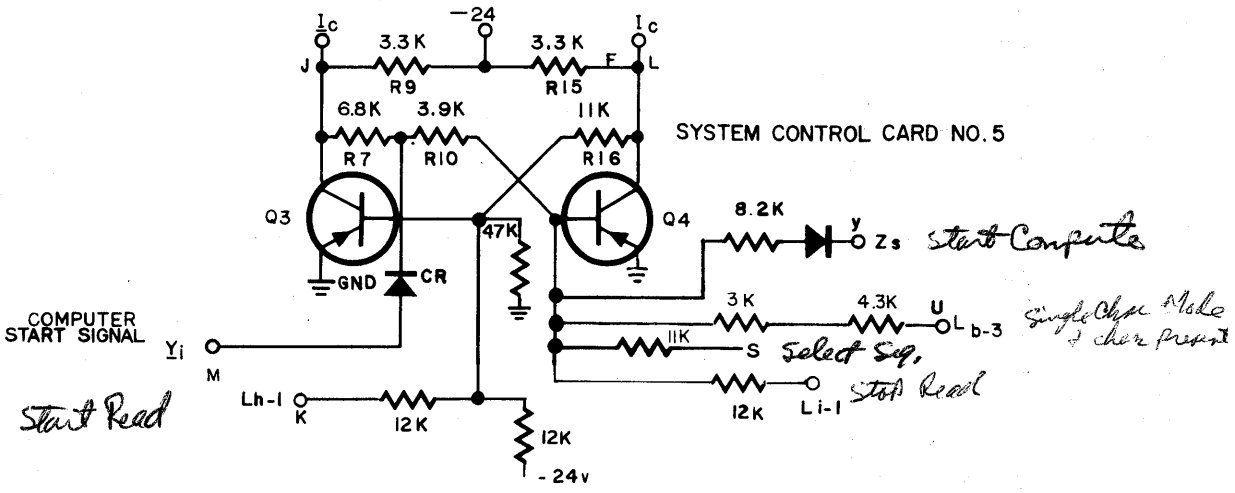


FIGURE 4-57 INPUT FLIP-FLOP (I_c)

The advance flip-flop (A_c) (figure 4-58) initiates a read cycle when turned on. A read cycle is begun only when in the input or read mode (I_c) and when all devices are ready (Z_q):

$$A_c' = I_c Z_q$$

The advance flip-flop is turned off by the trailing edge of the differentiated B* pulse:

$$\underline{A_c}' = \frac{d}{dt} B^* \quad \text{(trailing)}$$

The SELECT signal (S) (figure 4-59) indicates device or mode selection. It goes true when the MASTER RESET switch on the primary control panel is pressed, opening the ground circuit to the emitter of the transistor, generating the S signal.

$$S' = L_e + \ldots$$

In order to set the B flip-flops and read into the computer, B* must be true. When the reader select flip-flop and the advance flip-flop are true and the READER SELECT switch (off-line) is not depressed at the time reader cam 1 is true, the B* signal goes true:

$$B^* = (\text{Reader Cam 1})\ Q_r\ A_c\ \underline{L_v}$$

(B* is actually derived from a one-shot multivibrator set by this term.)

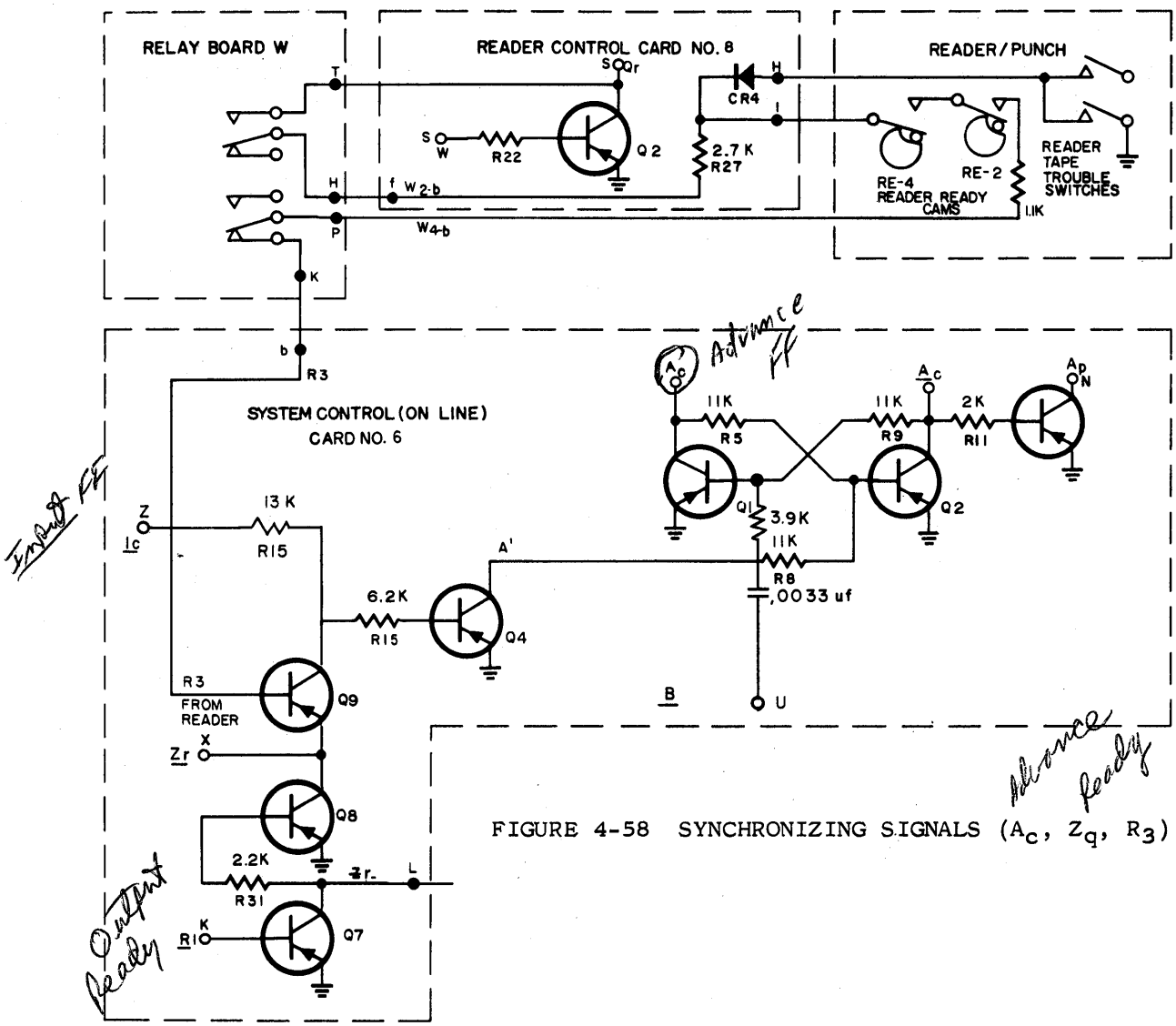


FIGURE 4-58 SYNCHRONIZING SIGNALS (A_c, Z_q, R_3)

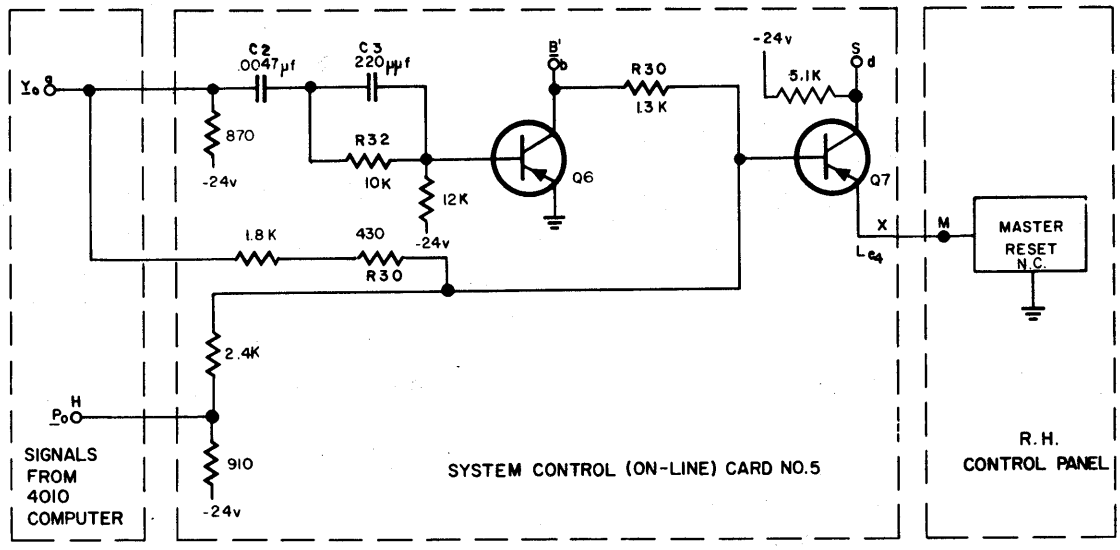


FIGURE 4-59 SELECT SIGNAL (S)

When operating off-line, the reader select flip-flop (Q_r) is ignored, and the READER SELECT switch must be in the off-line mode:

$$H^* = (\text{Reader Cam 1})\ A_m\ L_v$$

The reader tape-sensing brush signals are identified as T_1 through T_7. When operating on-line, the brushes which are in contact with the drum through holes in the paper tape set the B flip-flops by energizing the drum with B*. Off-line operations are identical, except that the H flip-flops of the off-line system control section are set:

$$B_{1-7}^* = (T_{1-7})\ B^*$$

$$H_{1-7}^* = (T_{1-7})\ H^*$$

During input of data to the computer, the B* signal generates $\underline{B}'$ which sets all of the $\underline{B}$ flip-flops false (figure 4-60). Signals from input devices are designated $B_{(n)}*$ and set the respective B flip-flop true in much the same manner as the $P_{(n)o}$ signals. When a $B_{(n)}^*$ signal is true it drives the off side transistor of the $\underline{B}_{(n)}$ flip-flop into saturation, which grounds the $\underline{B}_{(n)}$ output and allows the $B_{(n)}$ output to go true.

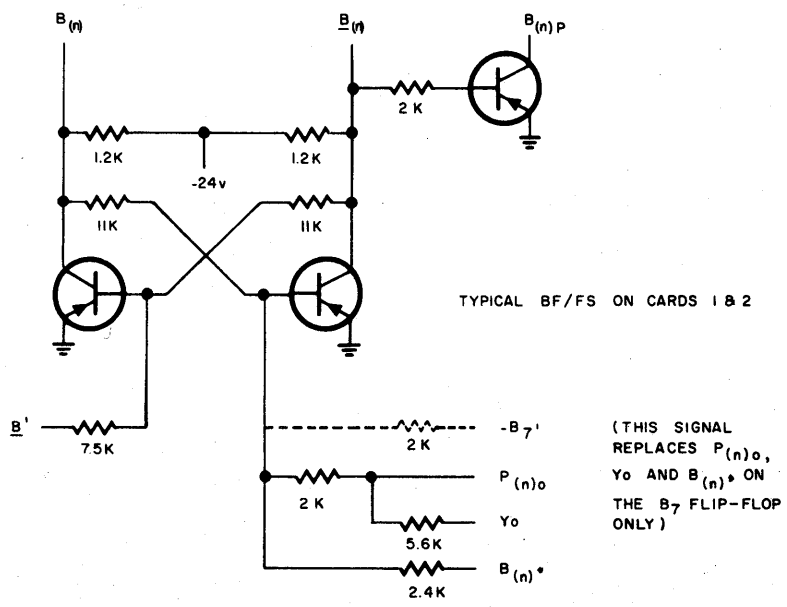


FIGURE 4-60 B FLIP-FLOP CIRCUIT

It should be noted that the B_6 flip-flop may also be set false and B_7 set true by an L_e signal from the MASTER RESET switch or an L_c signal from the PARITY MONITOR RESET switch. The signals which accomplish this are:

$$\underline{B}_6' = \underline{B}' + L_e + L_c$$

$$B_7' = B_7^* + Y_o\ \underline{(B')}\ E + L_e + L_c$$

$$B_1' = B_1^*$$

$$B_2' = B_2^* + \ldots$$

$B_3' = B_3^* + \ldots$

$B_4' = B_4^* + \ldots$

$B_5' = B_5^* + \ldots$

$B_6' = B_6^* + \ldots$

Characters are stored in a set of seven B flip-flops, designated B_1 through B_7, located on system control cards 1 and 2. Operation of each of the B flip-flops is identical. A $\underline{B}'$ signal is sent to the base of the on side transistors, which sets all of the flip-flops false by saturating these transistors, therefore grounding the outputs. The logic for turning the B flip-flops off is:

$\underline{B}_1' = \underline{B}'$

$\underline{B}_2' = \underline{B}'$

$\underline{B}_3' = \underline{B}'$

$\underline{B}_4' = \underline{B}'$

$\underline{B}_5' = \underline{B}'$

$\underline{B}_6' = \underline{B}' + L_e + L_c$

$\underline{B}_7' = \underline{B}'$

The $\underline{B}'$ signal is generated during output of data from the computer or input of data by an input device:

$$\underline{B}' = \frac{d}{dt} Y_o \text{ (leading)} + \frac{d}{dt} B^* \text{ (leading)}$$

Where $\frac{d}{dt}$ is the differentiated leading or trailing edge of the designated signal.

The Y_o signal is generated during phase 4 of a print command from the computer by:

$Y_o = F\ G\ Q_1\ \underline{Q}_2\ \underline{Q}_3\ \underline{Q}_4$

During each word period of an output command from the computer, the Y_o signal is false until phase 4. Signals from the computer P flip-flops designated $P_{(n)o}$, are presented (but not necessarily accepted) at all times to the B flip-flops. The $P_{(n)o}$ signals will, if true, saturate the false transistor of a corresponding B flip-flop, gated by the Y_o signal. Thus, a true signal from the computer will hold the false side of the corresponding B flip-flop to ground setting the B flip-flop true. The logic for performing the above operation for each of the B flip-flops is:

$B_1' = Y_o\ P_{70} + L_e + L_c + \ldots$

$B_2' = Y_o\ P_{60} + L_e + L_c + \ldots$

$B_3' = Y_o\ P_{50} + L_e + L_c + \ldots$

$B_4' = Y_o\ P_{40} + L_e + L_c + \ldots$

$$B_5' = Y_o P_{30} + L_e + L_c + \ldots$$

$$B_6' = Y_o P_{20} + \ldots$$

The B_7 flip-flop represents the parity bit, and its state is generated when the $\underline{B}'$ signal is false and the PARITY ERROR signal (E) is true, so that the output of the computer is augmented to have correct (even) parity. (E will be false after B is set correctly.) This operation is also gated by Y_o:

$$B_7' = Y_o \underline{(B')}\ E + L_e + L_c + \ldots$$

The B_1 through B_5 and B_7 flip-flops are also set true by an L_e signal from the MASTER RESET switch or an L_c signal from the PARITY MONITOR RESET switch.

The tape feed ADVANCE TAPE signal to the reader (figure 4-61) is generated on-line by the READER SELECT signal (Q_r), the advance flip-flop (A_c) and the READER SELECT switch in the on-line position ($\underline{L_v}$).

$$\text{TAPE FEED} = A_c\ Q_r\ \underline{L_v} + A_m\ L_v$$

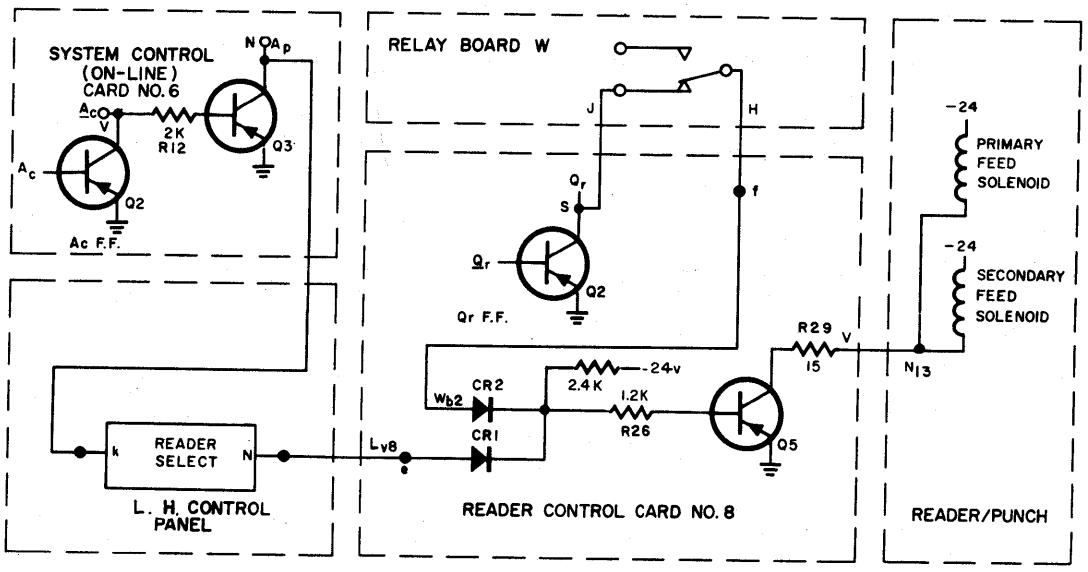


FIGURE 4-61 READER TAPE FEED

The reader clutch (figure 4-62) is engaged when the reader select flip-flop is true (Q_r) or when operating off-line by the input flip-flop (I_m) and the READER SELECT switch in the off-line position.

$$\text{READER CLUTCH} = Q_r\ Re_3\ \underline{L_v} + L_v\ I_m$$

The advance on-line flip-flop (A_c) is controlled by R_3. In order to generate an R_3 signal, the reader must be ready (Reader Cams 2 and 4) (figure 4-63), the reader select flip-flop must be true (Q_r), the READER SELECT switch must be in the on-line position ($\underline{L_v}$), and the tape trouble switches must be false. Control of the off-line advance flip-flop (A_m) is through R_5. In this mode, the reader must be ready (Reader Cams 2 and 4), the READER SELECT switch must be in the off-line psoition, and the tape trouble switches must be false.

R_3 = (Reader Cams 2 and 4) Q_r $\underline{L_v}$ (Reader Tape Trouble Switches)

R_5 = (Reader Cams 2 and 4) L_v (Reader Tape Trouble Switches)

INPUT begin (Z_b) is generated by an input sampling signal, (B*), the absence of the flip-flop reset signal ($\underline{B'}$) and the SINGLE CHARACTER MODE pushbutton depressed or an acceptable character with the typewriter function signal false ($\underline{F}$).

$$Z_b = B^* \ \underline{(B')} \left[L_b + (\underline{B_1} + \underline{B_2} + \underline{B_3} + \underline{B_4} + \underline{B_5} + \underline{B_6}) \ \underline{F} \right]$$

The INPUT ENABLE signal (Z_i) requires the absence of an input sampling signal ($\underline{B^*}$) and the non-depression of the START COMPUTE switch ($\underline{L_j}$).

$$Z_i = \underline{B^*} \ \underline{L_j}$$

A non-readiness query being false tests the readiness of all devices. The Z_q signal is generated by the READY synchronism signal (Z_r) and an input DEVICE READY signal (R_3).

$$Z_q = Z_r \ R_3$$

Parity checking of information in the RPC-4000 system is accomplished in both input and output modes by the system control section of the RPC-4500 Tape-Typewriter System. Each character contains six bits of identification and a seventh parity bit, which is included or excluded to bring the total to an even number of ones, or true bits, in each character.

Input and output information is sent through the B flip-flops character by character. The parity check is made of each character by reading the settings of the B flip-flops and by generating an error signal (E) if an odd number of ones is recognized.

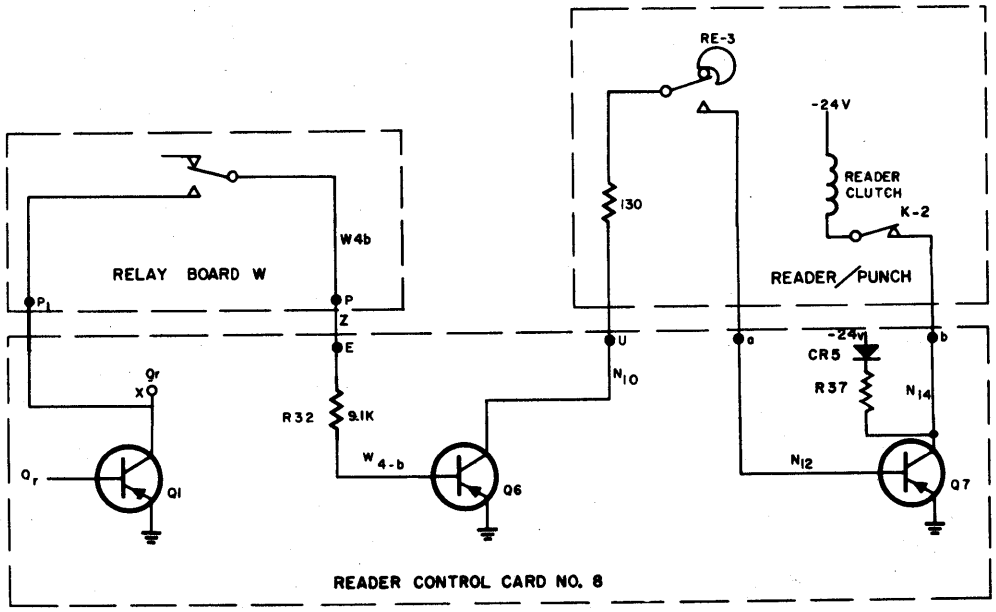


FIGURE 4-62 READER CLUTCH

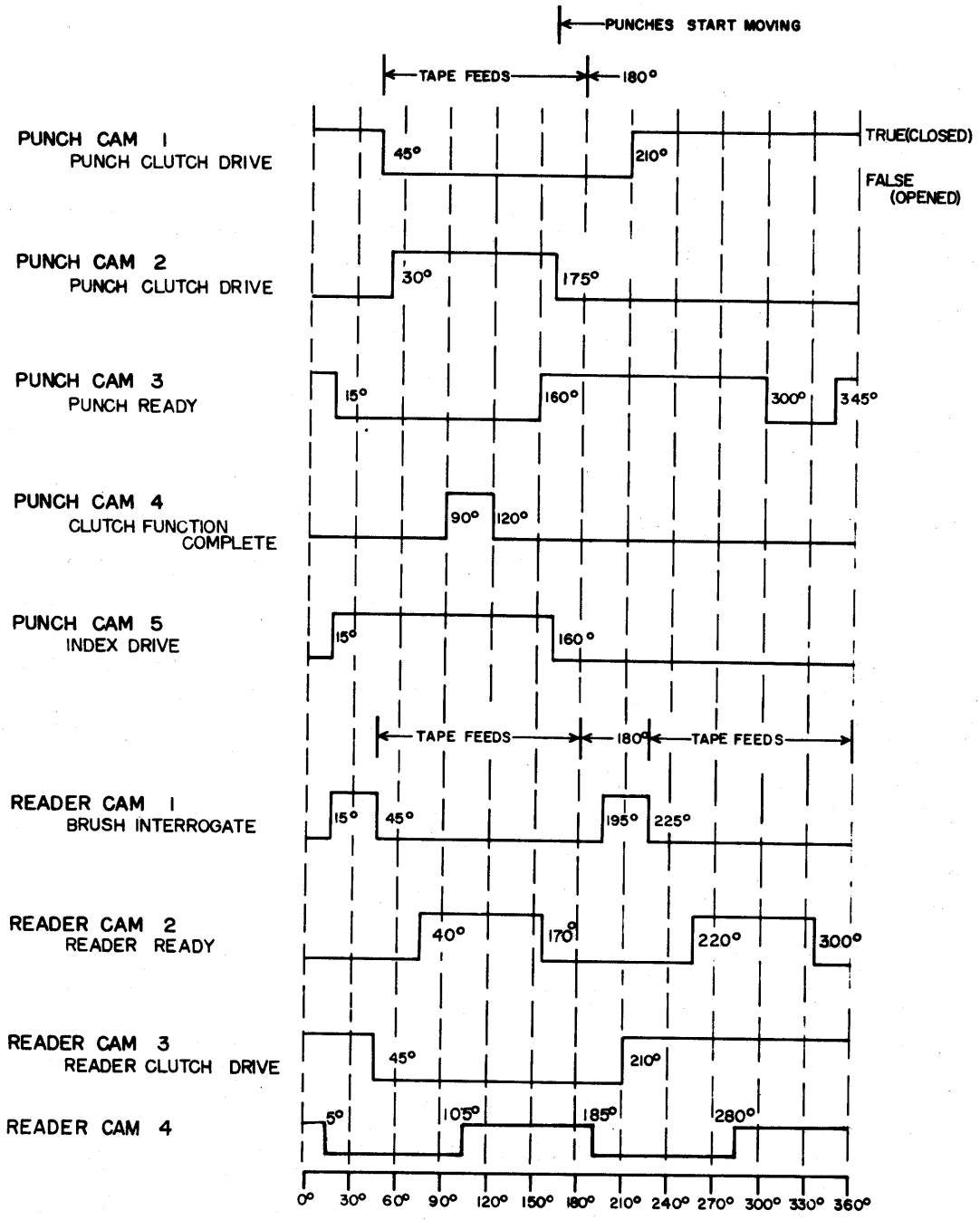


FIGURE 4-63 CAM TIMING

With the computer in input mode, E will stop the operation of both the computer and input device if the PARITY MONITOR INHIBIT pushbutton is not depressed. In the event of an error a correction may be typed or re-read into the computer, provided the PARITY MONITOR RESET pushbutton has been pressed to resume operation. Pressing the PARITY MONITOR RESET pushbutton should be preceded by pressing the STOP READ pushbutton.

With the computer in the output mode, E will go to a negative voltage when an odd number of true bits is detected and set the B_7 flip-flop true to generate the necessary parity bit.

The outputs of the B flip-flops are inputs to system control card #3 (figure 4-64). The B signals are compared through "exclusive NOR" gates which detect an odd or even number of ones in the character to determine the state of E as true or false. The states of B_1 and B_2 are compared to Q2. Both B_1 and B_2 are connected to the emitter of Q2 through a diode gate. Thus, when B_1 and B_2 are both false (at ground potential) the emitter and base of Q2 are held at ground. As a result Q2 is cut off, and the collector is at a negative voltage. When B_1 and B_2 are true (at a negative voltage) the emitter and base of Q2 are held negative. Again, Q2 is cut off, and the collector is negative. When B_1 and B_2 are both false or both true, an even number of bits is determined in B_1 and B_2 and indicated by Q2 output being true.

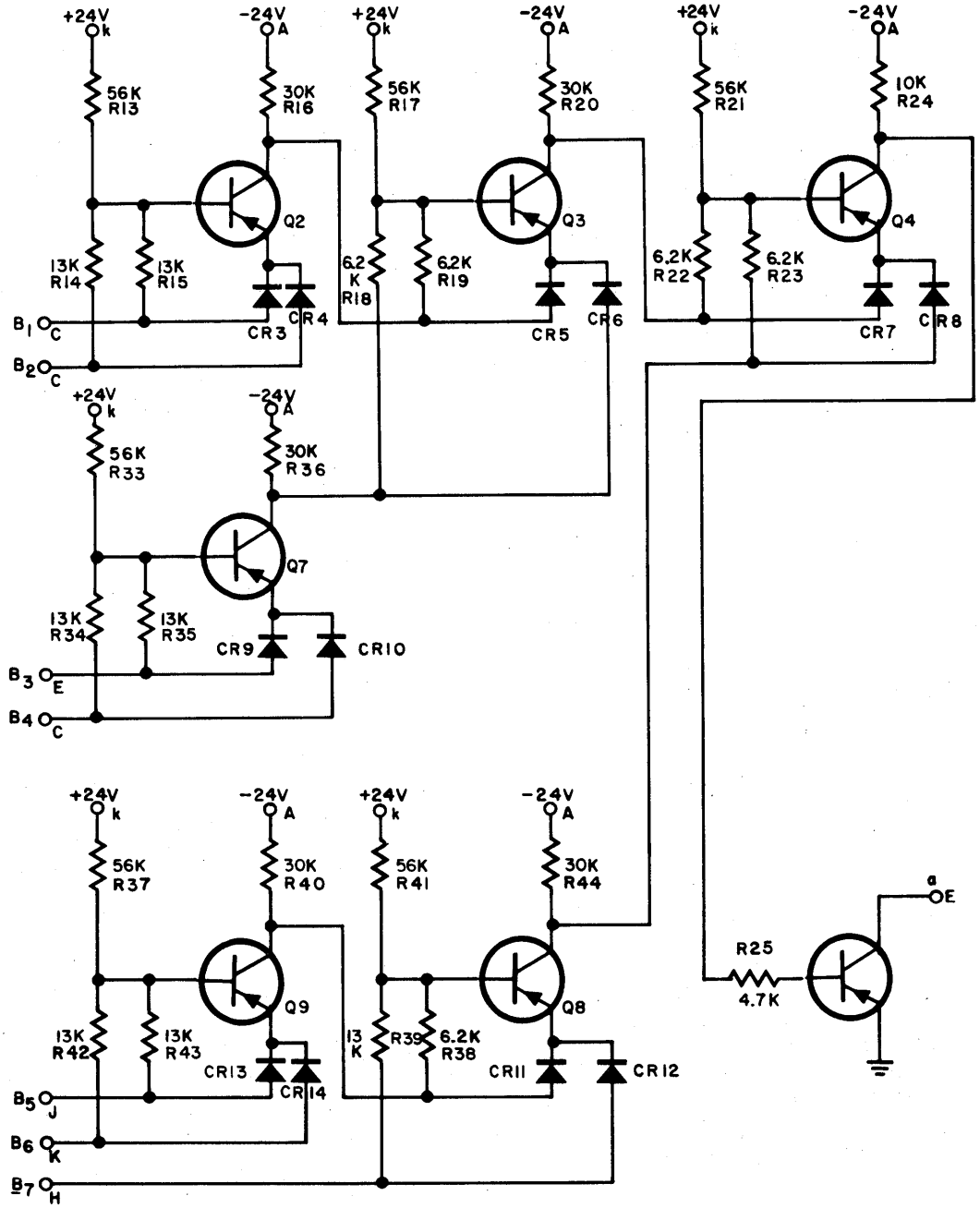


FIGURE 4-64 PARITY ERROR CIRCUIT

In the event B_1 and B_2 do not coincide (B_1 false and B_2 true, or B_1 true and B_2 false), the emitter of Q2 will be held to ground and the base deflected to a negative voltage. Consequently, Q2 will conduct and the collector will be held false, indicating an odd number of true bits for B_1 and B_2.

The Q2 circuit determines the number of true bits in B_1 and B_2. In the same manner, the Q7 circuit determines the number of true bits in B_3 and B_4 and the Q9 circuit determines the state of the B_5 and B_6 combination.

In the next stage the number of true bits in the outputs of Q2 and Q7 are determined by Q3. If the outputs are both false (indicating that B_1 and B_2 are odd and that B_3 and B_4 are odd) or both are true (indicating that both combinations, B_1 B_2 and B_3 B_4 are even) the output of Q3 is true, indicating that the number of true bits in B_1, B_2, B_3, and B_4 is even. An even number of true bits in these four B flip-flops will be indicated by:

$$(B_1\ B_2 + \underline{B}_1\ \underline{B}_2)\ (B_3\ B_4 + \underline{B}_3\ \underline{B}_4) + (B_1\ \underline{B}_2 + \underline{B}_1\ B_2)\ (B_3\ \underline{B}_4 + \underline{B}_3\ B_4)$$

If the outputs of Q2 and Q7 are not the same, that is, Q2 is false (indicating B_1 and B_2 contain an odd number of true bits) and Q7 is true (indicating B_3 and B_4 contain an even number of true bits) or if Q2 is true and Q7 is false, the collector of Q3 will be false indicating an odd number of true bits in B_1, B_2, B_3, and B_4. An odd number of true bits in these four flip-flops will be indicated by:

$$(B_1\ B_2 + \underline{B}_1\ \underline{B}_2)\ (B_3\ \underline{B}_4 + \underline{B}_3\ B_4) + (B_1\ \underline{B}_2 + \underline{B}_1\ B_2)\ (\underline{B}_3\ \underline{B}_4 + B_3\ B_4)$$

The Q8 circuit compares the output of Q9 with $\underline{B}_7$. If the output of Q9 is negative, B_5 and B_6 have an even number of true bits. If Q9 is at ground, B_5 and B_6 have an odd number of true bits. The $\underline{B}_7$ output of the B_7 flip-flop is true when there is no parity bit and false when there is a parity bit. The collector of Q8 will be negative when Q9 and B_7 are alike, and will be held to ground when Q9 and B_7 are not alike. The logic which indicates an even number of true bits in B_5, B_6, and B_7 is:

$$(B_5\ B_6 + \underline{B}_5\ \underline{B}_6)\ \underline{B}_7 + (B_5\ \underline{B}_6 + \underline{B}_5\ B_6)\ B_7$$

An odd number of true bits is determined by:

$$(B_5\ B_6 + \underline{B}_5\ \underline{B}_6)\ B_7 + (B_5\ \underline{B}_6 + \underline{B}_5\ B_6)\ \underline{B}_7$$

A final comparison is made between Q3 and Q8 by the circuit at Q4. A true output from Q4 indicates that B_{1-7} contain an even number of true bits or no parity error. The collector of Q4 drives the base of Q5. Consequently the collector of Q5 (E) is true when an odd number of true bits are detected, or false when an even number of true bits are detected.

The false outputs of the B flip-flops are compared through a NOR gate to determine if a delete code (B_{1-7} true) has been set into the B flip-flops. When this occurs, Q1 will not conduct:

$$E = \underbrace{(\underline{B}_1 + \underline{B}_2 + \underline{B}_3 + \underline{B}_4 + \underline{B}_5 + \underline{B}_6)}_{\text{not delete code}}\ \underbrace{\left[(B_1\ B_2 + \underline{B}_1\ \underline{B}_2)\ (B_3\ B_4 + \underline{B}_3\ \underline{B}_4) + (B_1\ \underline{B}_2 + \underline{B}_1\ B_2)\ (B_3\ \underline{B}_4 + \underline{B}_3\ B_4)\right]}_{B_1 - B_4 \text{ even}}$$

$$\Big[(B_5\ B_6 + \underline{B}_5\ \underline{B}_6)\ B_7 + (B_5\ \underline{B}_6 + \underline{B}_5\ B_6)\ \underline{B}_7\Big] +$$

$B_5 - B_7$ odd

$$\Big[(B_1\ B_2 + \underline{B}_1\ \underline{B}_2)\ (B_3\ \underline{B}_4 + \underline{B}_3\ B_4) + (B_1\ \underline{B}_2 + \underline{B}_1\ B_2)\ (\underline{B}_3\ \underline{B}_4 + B_3\ B_4)\Big]$$

$B_1 - B_4$ odd

$$\Big[(B_5\ B_6 + \underline{B}_5\ \underline{B}_6)\ \underline{B}_7 + (B_5\ \underline{B}_6 + \underline{B}_5\ B_6)\ B_7\Big]$$

$B_5 - B_7$ even

There is no parity check incorporated in off-line system control, and the busses accommodate only the typewriters and the reader/punch. Characters to be processed are stored in 7 tapehole flip-flops designated H_1 through H_7. All tape preparation and editing modes are provided.

The input or read mode for operation off-line is indicated by the input flip-flop (I_m). The input flip-flop is set by depressing the START READ switch on the auxiliary control panel. When the L_{x-1} signal goes true, the off side transistor of the I_m flip-flop is saturated, grounding the $\underline{I}_m$ signal and allowing the I_m signal to go true.

$$I_m' = L_x$$

The input mode flip-flop is reset by a stop code being detected, or during single character mode (L_z) after each character is processed, providing the CONDITIONAL STOP switch (L_s) is not depressed. The I_m flip-flop is also reset by pressing the STOP READ switch (L_y), or by the READER SELECT switch on the auxiliary control panel being depressed.

$$\underline{I}_m' = L_y + H^* \underline{(H')}\ (L_z + \underline{H}_1\ \underline{H}_2\ \underline{H}_3\ \underline{H}_4\ \underline{H}_5\ \underline{H}_6)\ \underline{L}_s + \frac{d}{dt} L_y \quad \text{(leading)}$$

To initiate a read cycle the advance flip-flop (A_m) must be set. The advance flip-flop is set by both the input DEVICE READY signal (R_5) and the output DEVICE READY signal (R_4) being true simultaneously (synchronization of input and output devices) when the off-line system is in the "input" mode (I_m true):

$$A_m' = R_5\ R_4\ I_m = K_m\ R_5$$

The advance flip-flop is reset by the differentiated H* signal.

$$\underline{A}_m' = \frac{d}{dt} H^* \text{ (trailing)}$$

To initiate an output cycle, the GO AHEAD signal (G_m) must be true (actually the $\underline{G}_m$ signal being false is employed). When the TAPE FEED switch on the auxiliary control panel is pressed or when the advance flip-flop is set true, the G_m signal is generated:

$$G_m = L_t + \frac{d}{dt} A_m \quad \text{(leading)}$$

When the input flip-flop is true, and the output device ready signal (R_4) is true, the off-line OK TO TYPE (or PUNCH) signal K_m goes true:

$$K_m = I_m\ R_4$$

The H flip-flops are set by the H_{1-7}* signals from an input device. At the beginning of each cycle the true side transistors of the H flip-flops are saturated by the H' signal, which sets the H flip-flops false:

$$\underline{H}_{1-7}' = \underline{H}'$$

The $\underline{H}'$ signal is generated by the leading edge of the H* signal or by the TAPE FEED switch on the auxiliary control panel being pressed:

$$\underline{H}' = \frac{d}{dt} H^* \text{ (leading)} + L_t$$

4.13 PUNCH OUTPUT--The punch control section of the RPC-4500 Tape-Typewriter System controls the on-line and off-line operations of the paper tape punch. The punch select flip-flop (Q_p) indicates that the paper tape punch is selected as an on-line device. The punch may be selected on-line by depressing the COMPUTER TO PUNCH switch which causes the signal L_{q-1} to saturate the off side transistor and hold it to ground. This in turn grounds the base of the on side transistor and forces the Q_p flip-flop to go true. The punch select code combines the B_{1p}, B_{4p}, and B_{5p} signals through a gate which forces the collector of transistor Q4 to ground when B_4 or B_5 is true or B_1 is false, and isolates the S signal from the Q_p transistor. When the B signals are set to the punch select code (S) holds $\underline{Q}_p$ to ground forcing Q_p true.

$$Q_p' = S\ B_1\ \underline{B_4}\ \underline{B_5} + L_q$$

The punch select flip-flop is reset by a combination of the SELECT signal (S) and the UNSELECT signal (U) which disengages all previously selected output devices. The punch may also be reset by depressing the PUNCH SELECT switch (L_w) on the auxiliary control panel which opens the X relay and causes signal X_{3b} to saturate the $\underline{Q}_p$ transistor.

$$\underline{Q}_p' = S\ U + \frac{d}{dt} L_w \text{ (leading)}$$

In order to activate the punch clutch and indicate that a punching cycle is in process, the output flip-flop (O_p) must be true. Operating on-line, if the PUNCH SELECT switch on the auxiliary control panel is not depressed, the G_c signal is directed to the base of the transistor controlling O_p. O_p will be set true by $\underline{G}_c$ being false, and $\underline{Q}_p$ being false and $\underline{L}_w$ being true. Operating off-line, the PUNCH SELECT switch is depressed, and the $\underline{G}_m$ signal is directed to the base of the on side of the O_p flip-flop. In order to set the output flip-flop, either G_c or G_m must be true, depending on the state of the PUNCH SELECT switch.

$$O_p' = Q_p\ G_c\ \underline{L}_w + G_m\ L_w + L_t$$

The output flip-flop is turned off by punch cam 4 indicating that the punch is committed to cycle or is held off by the punch select flip-flop in the off state ($\underline{Q}_p$) and the punch operating on-line ($\underline{L}_w$).

Either of these conditions will saturate the true side transistor of the output flip-flop and hold the O_p signal to ground.

$$\underline{O}_p' = (\text{Punch Cam 4}) + \underline{Q}_p\ \underline{L}_w$$

The punch clutch (figure 4-65) operates when the output flip-flop is true, punch cam 1 is true, and the punch tape trouble switches are false:

PUNCH CLUTCH CONTROL = O_p (Punch Cam 1) (Punch Tape Trouble Switches)

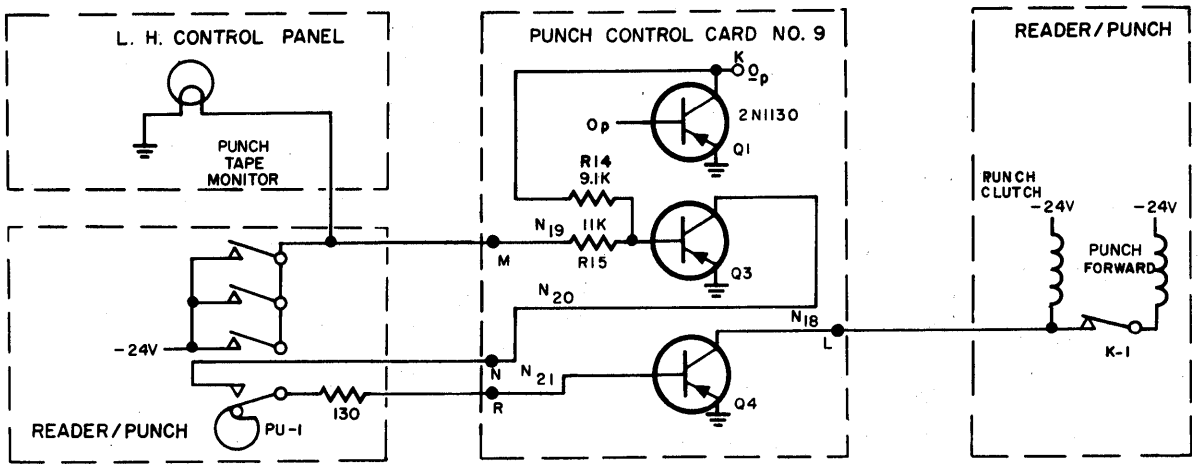


FIGURE 4-65 PUNCH CLUTCH

The punch will operate in the forward direction when the output flip-flop is true, punch cam 1 is true, the punch tape trouble switches are false, and the reverse tape feed mode is false.

FORWARD TAPE FEED = O_p (Punch Cam 1) (P.T.T.S.) (R.T.F.M.)

The reverse tape feed mode is true only when the tape backspace relay (K1) is energized. This mode can be entered only when the punch and typewriter are both off-line.

REVERSE TAPE FEED = Tape Backspace Relay

The feed hole magnet is energized when punch cam 5 is true and the punch is not in reverse tape feed mode.

FEED HOLE MAGNET = (Punch Cam 5) (Reverse Tape Feed Mode)

The paper tape punch magnets 1 through 7 are energized by either the power outputs of the B flip-flops, B_{1-7p} when L_w is true or by the H flip-flops, H_{1-7} when L_w is true and when punch cam 2 is true (figure 4-66).

CHARACTER PUNCH MAGNETS 1 through 7 = $\left[(B_{1-7})\ \underline{L_w} + (H_{1-7})\ L_w\right]$ (Punch Cam 2)

The OUTPUT ENABLE signal (Z_o) requires the READY synchronism signal (Z_r) and an output DEVICE SELECTION (R_2) or a PRINT command with a selection (P_o).

$$Z_o = Z_r\ (R_2 + P_o)$$

If during a print command, the computer generates a select signal (P_o):

$$P_o = P_1\ Q_5$$

it is combined with the negation of ($\underline{B}'$) and the computer produced Y_o signal to generate S (Y_o indicates phase 4 of any print command):

$$S = P_o \, (\underline{B}') \, Y_o + \ldots$$

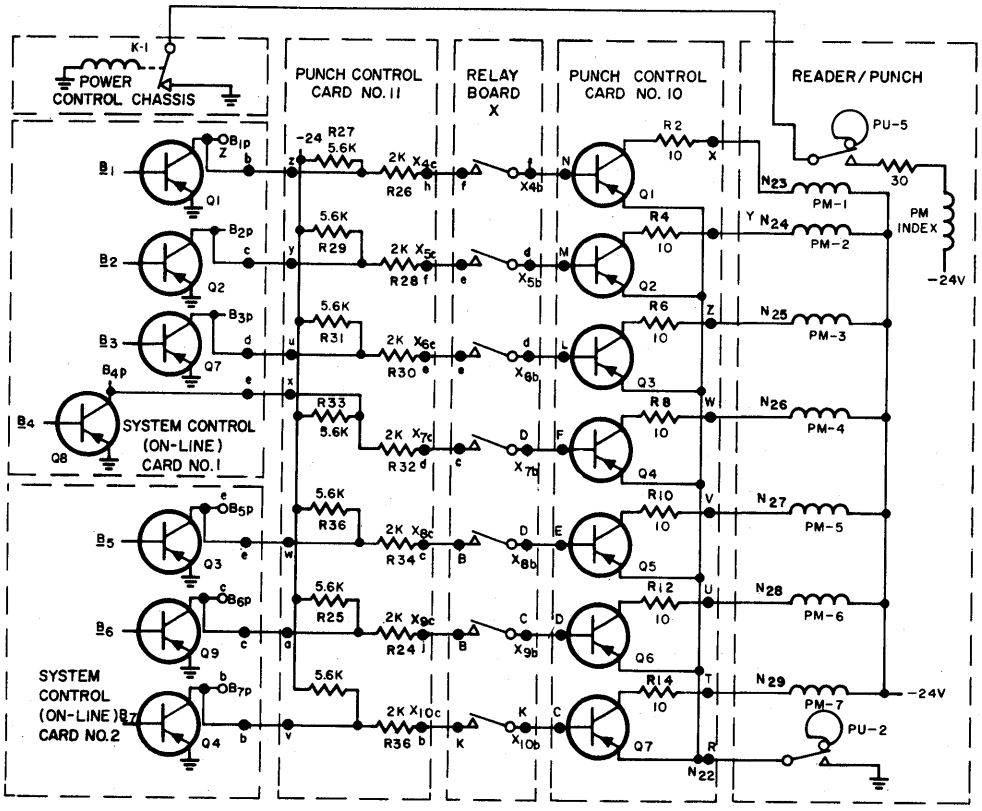


FIGURE 4-66 PUNCH MAGNETS

To initiate an output cycle by any on-line selected output device, a G_c signal is generated. When input information is to be copied during an input cycle (input duplication mode) G_c is formed by combining the leading edge of the differentiated A_c signal with the copy flip-flop.

$$G_c = \frac{d}{dt} A_c \text{ (leading) } C + \ldots$$

An output cycle is initiated by the computer during phase 4 of a non-selection print command by combining the computer print out signal (Y_o) with a false selection signal ($\underline{P}_o$).

$$G_c = Y_o \, \underline{P}_o + \ldots$$

All selected input and output devices may be disengaged on-line, by the UNSELECT signal (U). The U signal is generated by the B_1 through B_5 flip-flops in the true state.

$$U = B_1 \, B_2 \, B_3 \, B_4 \, B_5$$

(U must be combined with S at output device control circuit to function properly.)

The input duplication mode is dependent on the copy flip-flop (C) for operation. The copy flip-flop may be turned on by pressing the INPUT DUPLICATION pushbutton, which releases the L_{g-1} signal from ground and allows transistor Q1 to become saturated grounding the $\underline{C}$ signal. The copy flip-flop may also be set by a select signal under computer control:

$$C' = S\ B_1\ \underline{B_2}\ B_3\ B_4\ B_5\ B_6 + L_g$$

The copy flip-flop is turned off by pressing the INPUT DUPLICATION RESET pushbutton, releasing L_{f-1}, or by computer control:

$$\underline{C}' = S\ \underline{B_1}\ B_2\ B_3\ B_4\ B_5\ B_6 + L_f$$

4.14 TYPEWRITER CONTROL--The typewriter control section of the RPC-4500 Tape-Typewriter System controls all typewriter functions of input or output both on-line and off-line. When an auxiliary typewriter is connected to the RPC-4500, an identical control section (differing only in selection code) is added to control the auxiliary typewriter. The typewriter functions as two devices, an input device and an output device, just as the reader/punch unit is two devices.

Operating on-line the typewriter is selected as an input device by setting the typewriter input select flip-flop (Q_i) (figure 4-67). This may be accomplished by depressing the TYPEWRITER TO COMPUTER switch on the L.H. control panel or may be accomplished with the SELECT signal (S) true, signal B_3 true, and signals B_{4p}, B_{5p}, and B_{6p} false. When the TYPEWRITER TO COMPUTER switch is depressed the off side transistor is saturated, grounding the $\underline{Q_i}$ signal and driving the Q_i signal true. The Q_i flip-flop may also be set by the Q_i' signal which combines the outputs of the B_4, B_5, B_6, and B_3 flip-flops through a resistor-transistor diode gate with the S signal in a manner similar to reader or punch selection. When B_3 is false or any of the B_4, B_5, B_6 flip-flops are true they inhibit transmission of the S signal. Otherwise the S signal becomes Q_i' which saturates the off side transistor and sets the Q_i flip-flop to the true state.

$$Q_i' = S\ B_3\ \underline{B_4}\ \underline{B_5}\ \underline{B_6} + L_m$$

The typewriter select flip-flop is turned off in a manner similar to the reset of the reader select flip-flop Q_i by the select signal and $\underline{B_6}$ and the absence of Q_i' which sets the Q_i flip-flop. The Q_i flip-flop may also be reset by depressing the TYPEWRITER SELECT switch on the L.H. control panel.

$$\underline{Q_i}' = S\ \underline{B_6}\ (\underline{Q_i}') + \frac{d}{dt}\ L_u\ \text{(leading)}$$

The typewriter is selected as an output device while operating on-line by turning on the typewriter output select flip-flop (Q_o). To turn Q_o on, the Q_o' signal is generated by gating the SELECT signal (S) with a combination of B_{2p}, B_{4p}, and B_{5p}. The Q_o flip-flop may also be set by depressing the COMPUTER TO TYPEWRITER switch on the L.H. control panel.

$$Q_o' = S\ B_2\ \underline{B_4}\ \underline{B_5} + L_p$$

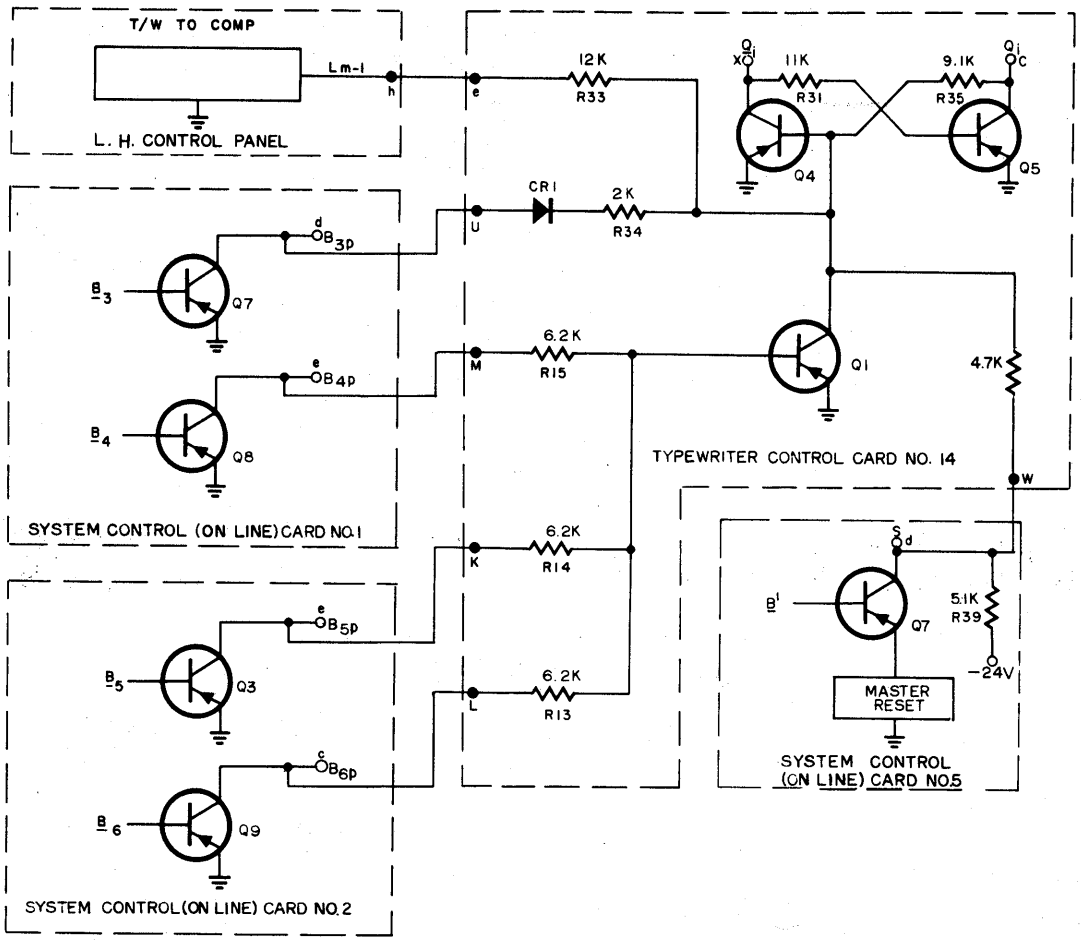


FIGURE 4-67 TYPEWRITER INPUT SELECT CIRCUITS

In order to turn the Q_O flip-flop off, the SELECT signal is combined with the UNSELECT signal or the signal produced as the TYPEWRITER SELECT switch on the L.H. control panel is being depressed.

$$\underline{Q_o}' = S\ U + \frac{d}{dt}\ L_u \text{ (leading)}$$

The typewriter may be operated off-line by depressing the TYPEWRITER SELECT switch on the L.H. control panel which de-energizes both the V_I and V_{II} relays, switching all typewriter control signals from on-line to off-line system control.

To drive the typewriter, as an output device, through a typing cycle, the typewriter output flip-flop (O_t) must be set. This is accomplished by the on-line GO AHEAD signal (G_c) when the TYPEWRITER SELECT switch on the L.H. control panel is not depressed, and by G_m when TYPEWRITER SELECT switch is depressed.

The typewriter OK TO TYPE signal (K_c) (figure 4-68), which indicates when a selected typewriter will be recognized as an input device, is controlled by the READY synchronism signal (Z_r) and the input flip-flop (I_c).

$$K_c = I_c\ Z_r$$

The typewriter FUNCTION signal (F), which represents characters not accepted by the computer unless in single character mode, is true when B_5 and B_6 are false.

$$F = \underline{B_5}\ \underline{B_6}$$

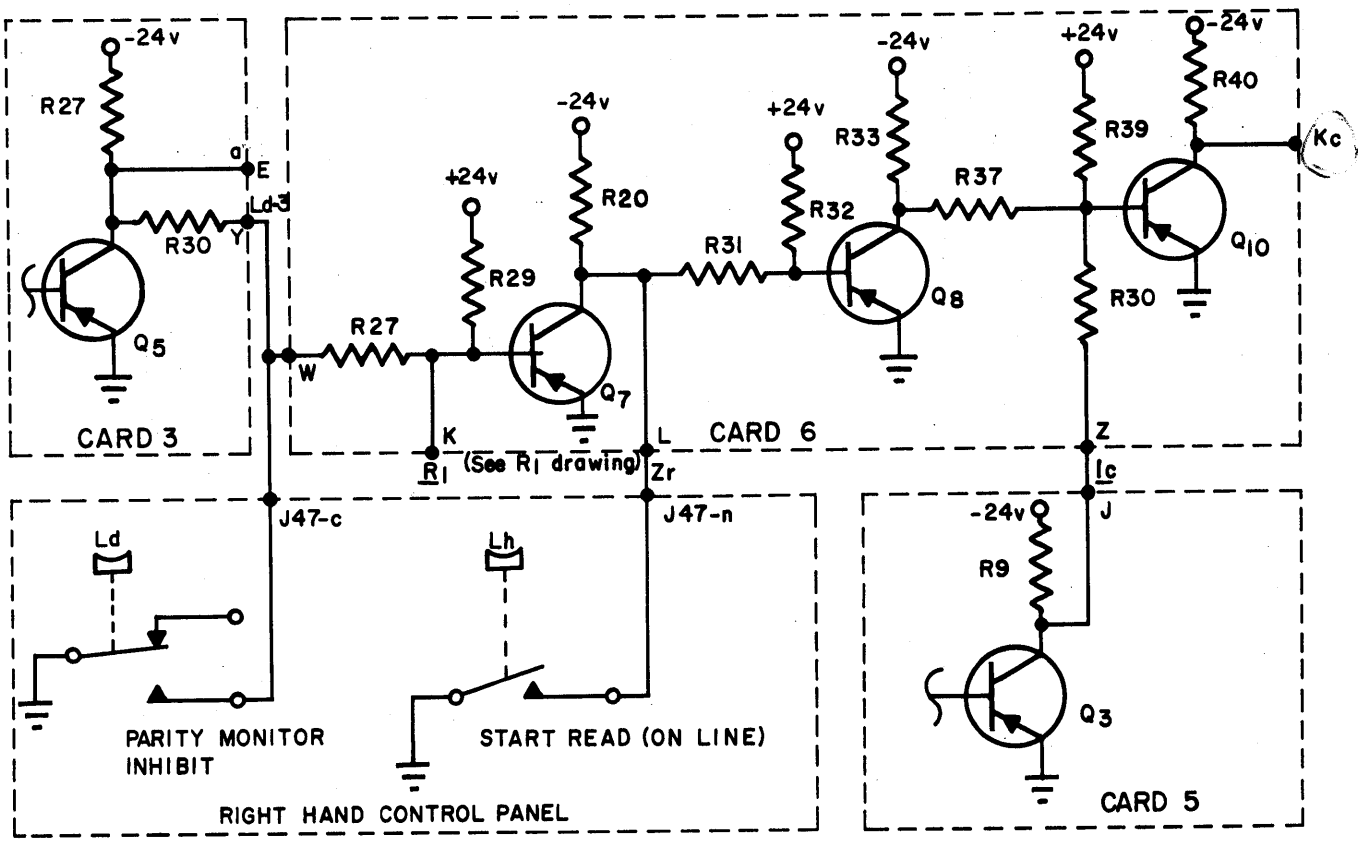


FIGURE 4-68 OK TO TYPE SIGNAL

The F signal is ignored when the SINGLE CHARACTER MODE pushbutton is depressed.

The O_t flip-flop is held off when the typewriter should not accept the G_c or G_m signals. This is true if the typewriter is used as an input device, or is not selected as an output device. The typewriter output flip-flop is reset by the leading edge of the differentiated signal (N_{46}) indicating that a key has typed:

$$\underline{O_t}' = \frac{d}{dt}\ N_{46}\ \text{(leading)} + \underline{Q_o}\ \underline{L_u} + L_u\ \underline{L_v} + Q_i\ A_c\ \underline{L_u}$$

The typewriter circuit is so designed that each key is energized by a discrete electronic code of seven bits. At the time the hammer is at the platen, the sampling signal (N_{46}) is generated whether the key was driven manually or energized electromechanically. This completes diode logic encoding to read or input the state of the seven bits describing a character. On-line input operation requires the B* signal; it is generated by the TYPEWRITER SELECT switch

(L_u) on the L.H. control panel not being depressed, the advance flip-flop (A_c) being true, and the typewriter input select flip-flop (Q_i) being true at sampling time:

$$B^* = \underline{L}_u \, A_c \, Q_i \, N_{46}$$

(B* is derived from a one-shot multivibrator set by this term.)

$$B_{1-7^*} = \text{(Encoder bits 1, 2, 4, 8, F, A, P) } B^*$$

Off-line operation requires that the TYPEWRITER SELECT switch on the L.H. control panel be depressed, the READER SELECT switch not be depressed, and the off-line advance flip-flop be set at sampling time.

$$H^* = (L_u \, \underline{L}_v) \, A_m \, N_{46}$$

$$H_{1-7^*} = \text{(Encoder bits: 1, 2, 4, 8, F, A, P) } H^*$$

SECTION 5

MAINTENANCE

ILLUSTRATIONS

TABLES

SECTION 5

MAINTENANCE

5.1 GENERAL--The maintenance procedures used on the RPC-4010 Computer and RPC-4500 Tape-Typewriter System follow standard electronic practice. Special instructions and equipment are necessary only for maintenance of the magnetic drum. This special equipment is supplied with the computer, and maintenance instructions are contained in section 5.4.

Maintenance of the Reader/Punch Unit (891-PC) is covered in the Control Data release FA 002, and maintenance of the Typewriter (180-XE) in the Control Data release FA 001.

5.2 DISASSEMBLY-- Disassembly of the RPC-4010 Computer (figure 5-1), the RPC-4430 Reader/Punch (figure 5-2), or the RPC-4480 Typewriter (figure 5-3) is required only when a failure has occurred in the unit. In order to carry out normal maintenance routines, removal of the cover panels is the only disassembly necessary. The units can be operated with their covers removed to aid in trouble shooting. As far as possible, all circuits are contained on removable cards to facilitate repair.

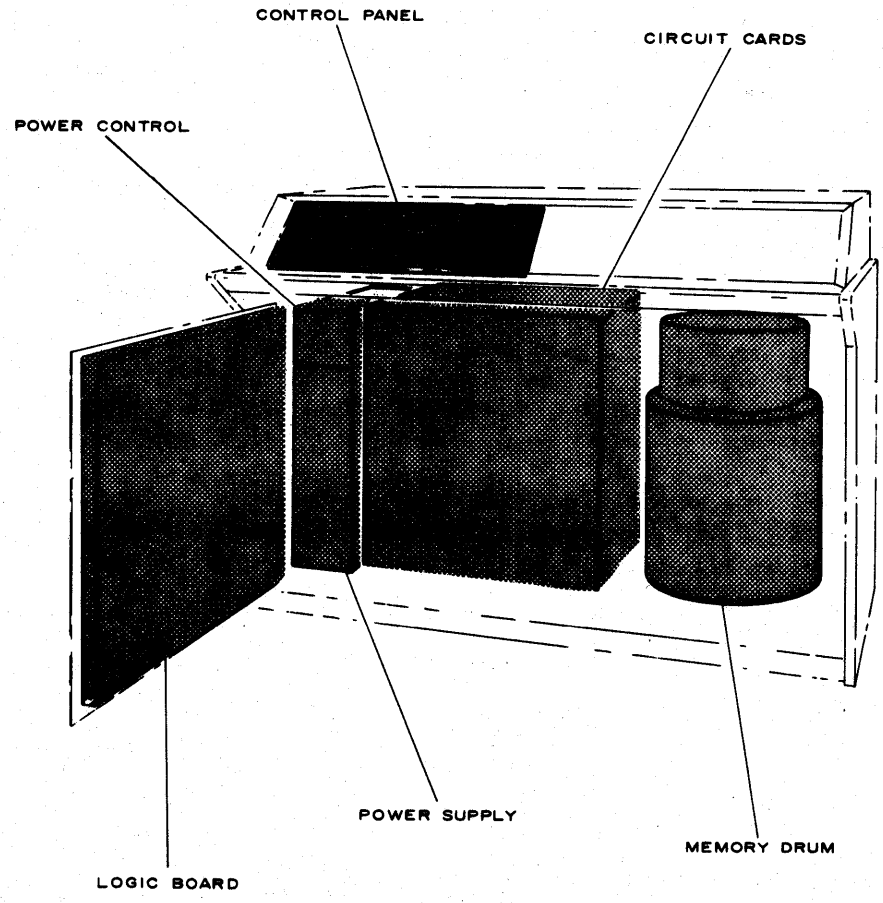


FIGURE 5-1 RPC 4010 COMPUTER ASSEMBLY
(6 ILLUSTRATIONS)

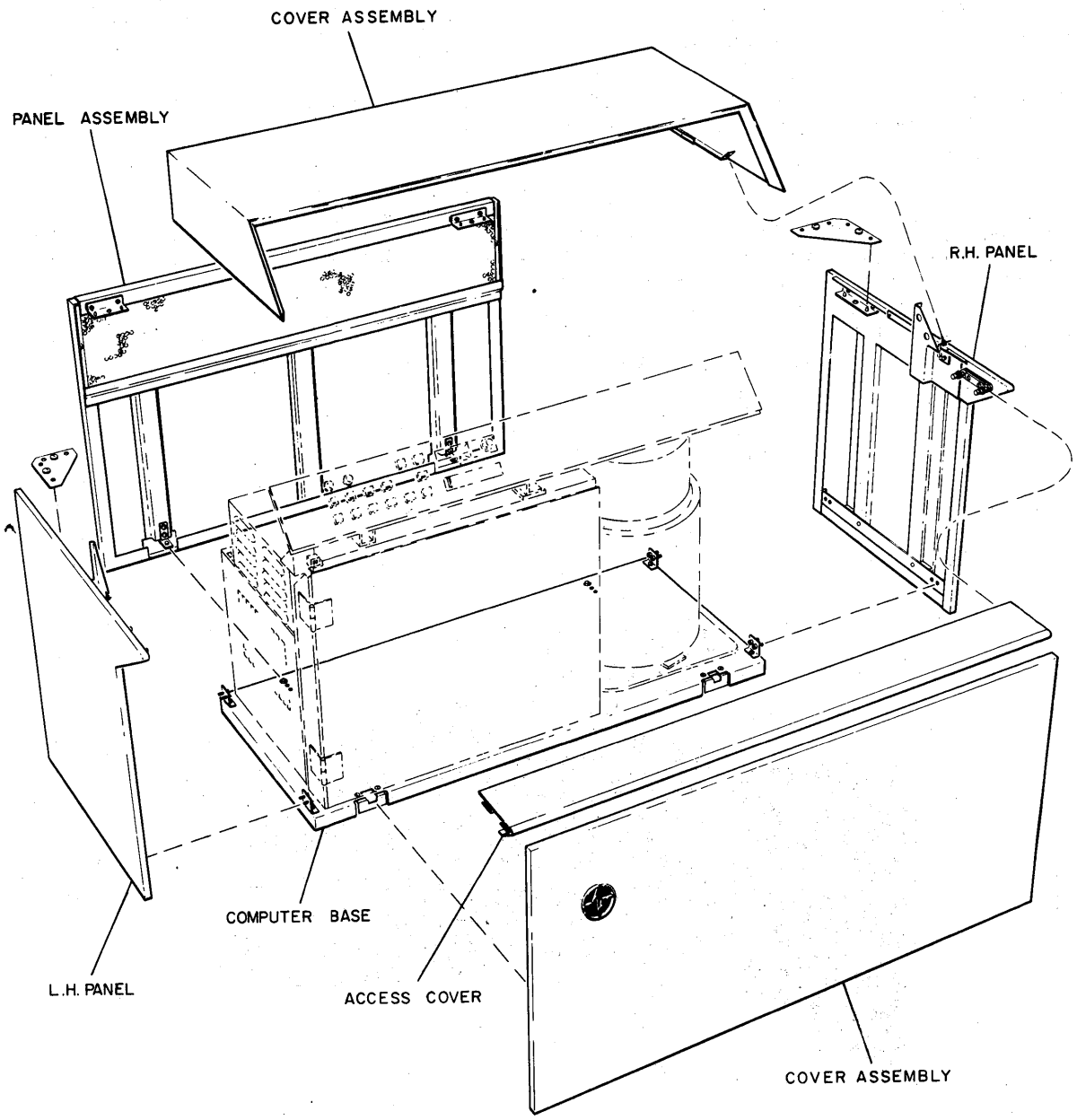


FIGURE 5-1 (2 of 6)

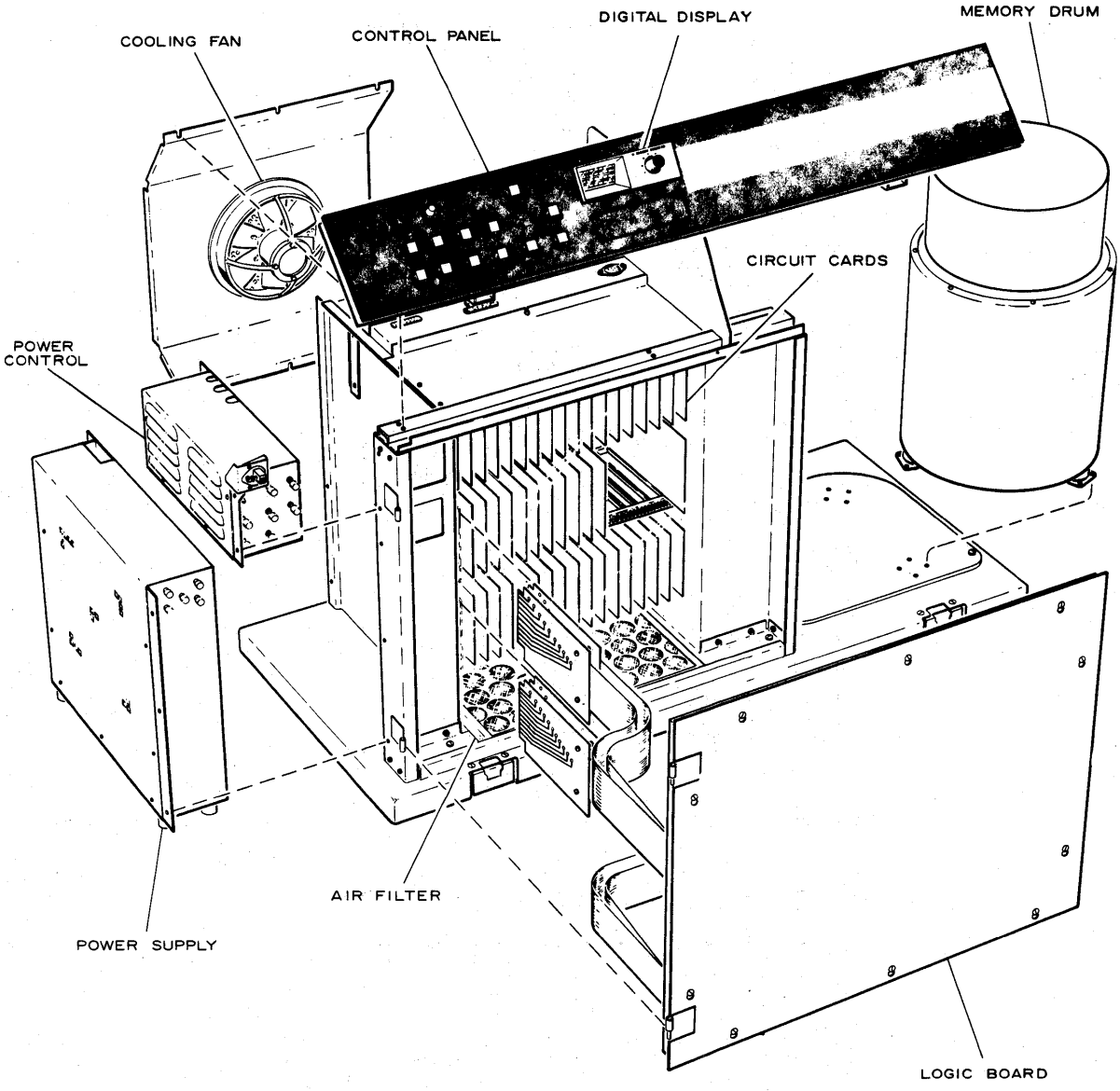


FIGURE 5-1 (3 of 6)

UPPER ROW–RIGHT TO LEFT

POSITION	CARD	DRAWING NO.
1.	X RECORD	L 200 006 162
2.	D RECORD	L 200 006 162
3.	C RECORD	L 200 006 162
4.	L RECORD	L 200 006 162
5.	U RECORD	L 200 006 162
6.	SPARE	— — — —
7.	COL. DR. 0-1	L 200 006 165
8.	COL. DR. 2-3	L 200 006 165
9.	COL. DR. 4-5	L 200 006 165
10.	COL. DR. 6-7	L 200 000 165
11.	ROW DR. 0-1-2-3	L 200 006 161
12.	ROW DR. 4-5-6-7	L 200 006 161
13.	ROW DR. 8-9-10-11	L 200 006 161
14.	ROW DR. 12-13-14-15	L 200 006 161
15.	MAIN MEM. READ	L 200 009 985-L200 007324
16.	W FLIP FLOP	L 200 006 056
17.	V_R FLIP FLOP	L 200 006 163
18.	SPARE	— — — —
19.	HORIZONTAL	L 200 006 241
20.	VERTICAL	L 200 006 242

CENTER ROW–RIGHT TO LEFT

POSITION	CARD	DRAWING NO.
21.	POWER DISTRIBUTION	L 200 007 292
22.	FLIP FLOP INDICATOR	— — — —
23.	SPARE	— — — —
24.	SPARE	— — — —
25.	SPARE	— — — —
26.	SPARE	— — — —
27.	SPARE	— — — —
28.	S1-S2-S3 FLIP FLOP	L 200 006 242
29.	C R X FLIP FLOP	L 200 006 242
30.	U* L L* FLIP FLOP	L 200 006 242
31.	M N U FLIP FLOP	L 200 006 242
32.	B K A FLIP FLOP	L 200 006 242
33.	F G H FLIP FLOP	L 200 006 242
34.	P5-P6-P7 FLIP FLOP	L 200 006 242
35.	P2-P3-P4 FLIP FLOP	L 200 006 242
36.	Q4-Q5-P1 FLIP FLOP	L 200 006 242
37.	Q1-Q2-Q3 FLIP FLOP	L 200 006 242
38.	INVERTER	L 200 006 164
39.	LOGIC	— — — —
40.	LOGIC	— — — —

LOWER ROW–RIGHT TO LEFT

POSITION	CARD	DRAWING NO.
41.	CLOCK READ	L 200 009 983-L200 006160
42.	CLOCK GENERATOR	L 200 006 166
43.	S-3 READ	L 200 007 300
44.	S-2 READ	L 200 007 300
45.	S-1 READ	L 200 007 300
46.	X READ	L 200 007 300
47.	D READ	L 200 007 300 ALSO
48.	C READ	L 200 007 300 L 200 009984
49.	L* READ	L 200 007 300
50.	L READ	L 200 007 300
51.	U* READ	L 200 007 300
52.	U READ	L 200 007 300
53.	SPARE	— — — —
54.	SPARE	— — — —
55.	SPARE	— — — —
56.	SPARE	— — — —
57.	SPARE	— — — —
58.	AMPLIFIER	L 200 006 158
59.	LOGIC	— — — —
60.	LOGIC	— — — —

FIGURE 5-1 (4 of 6)

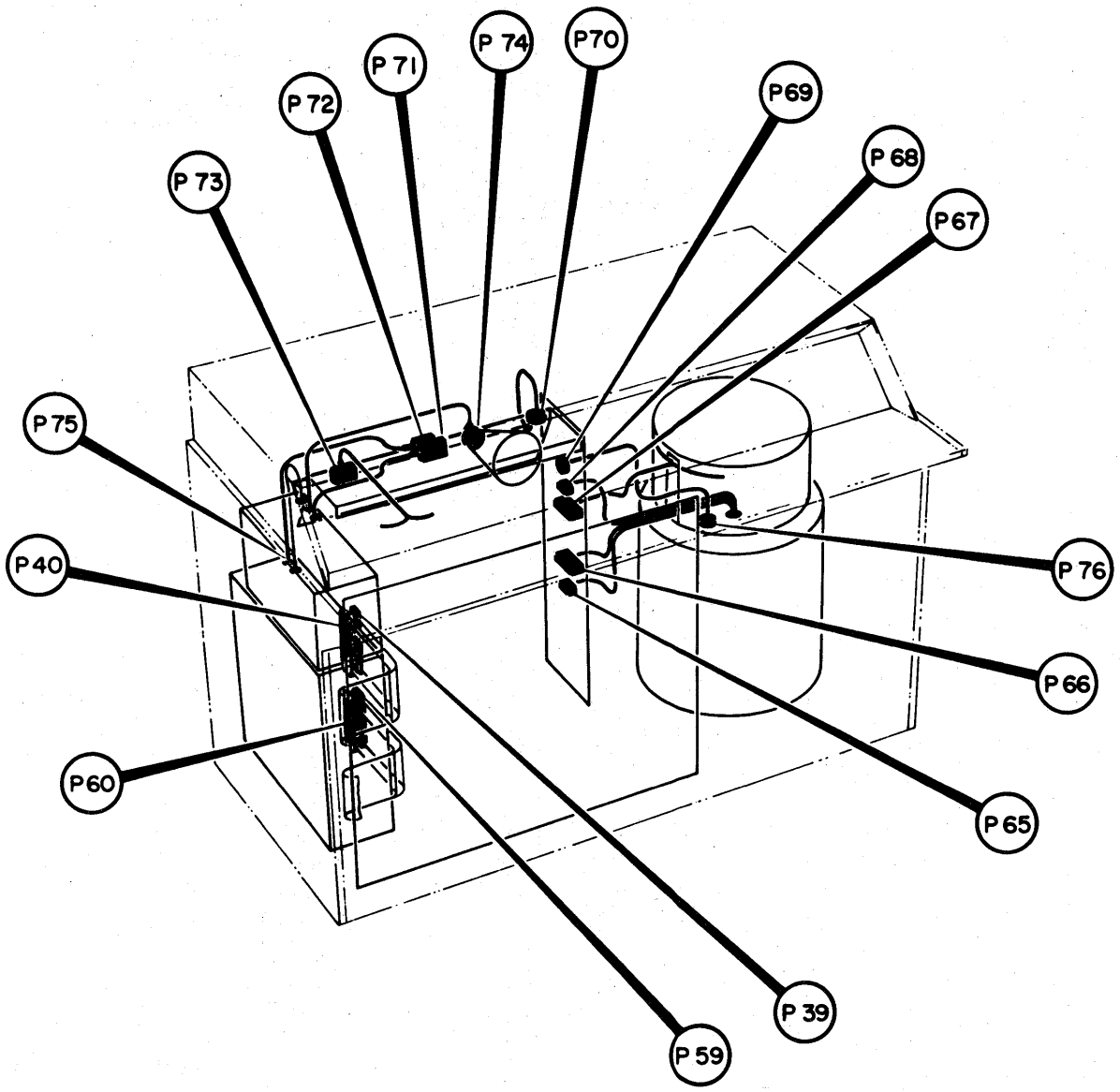


FIGURE 5-1 (5 of 6)

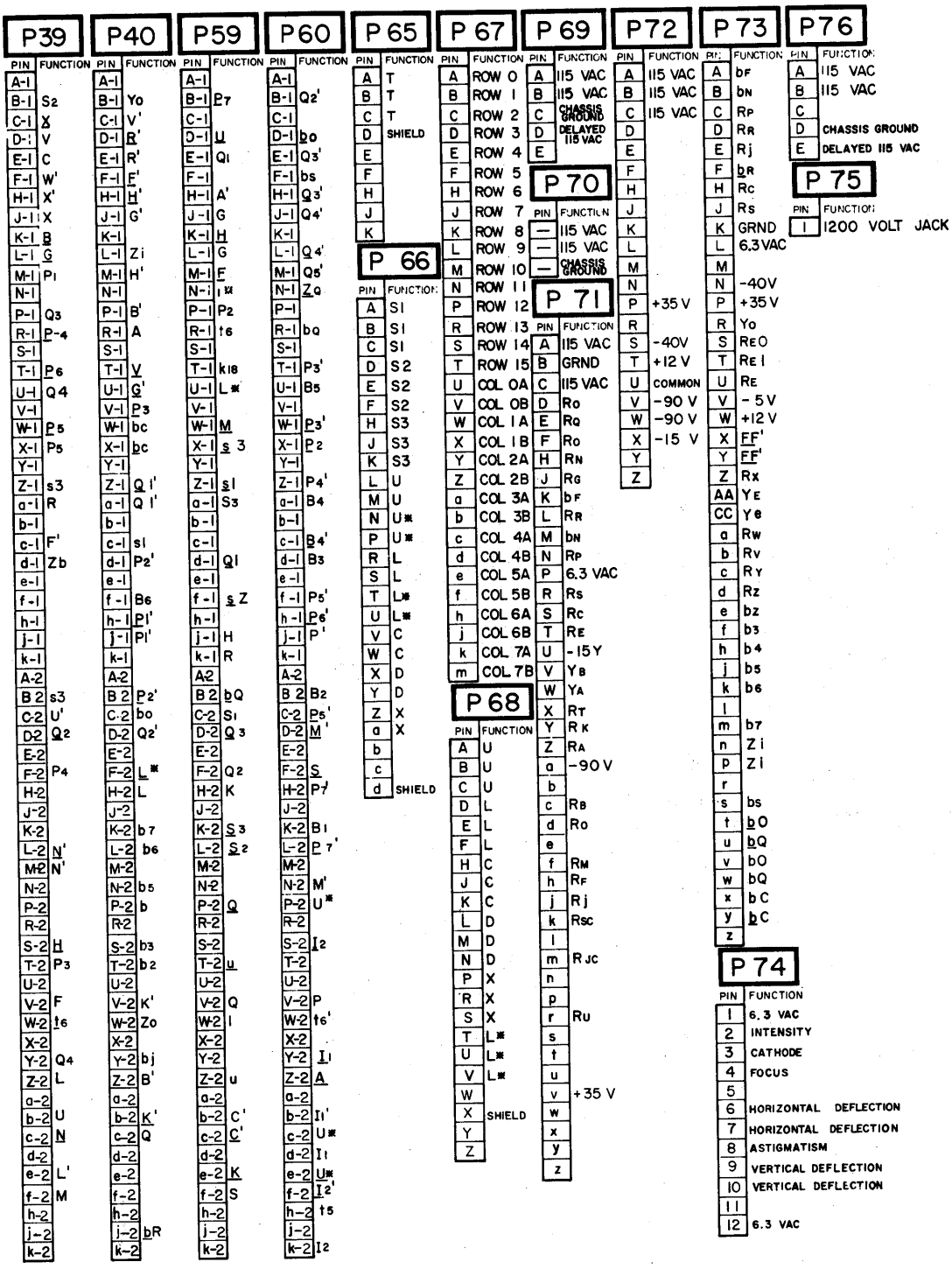


FIGURE 5-1 (6 of 6)

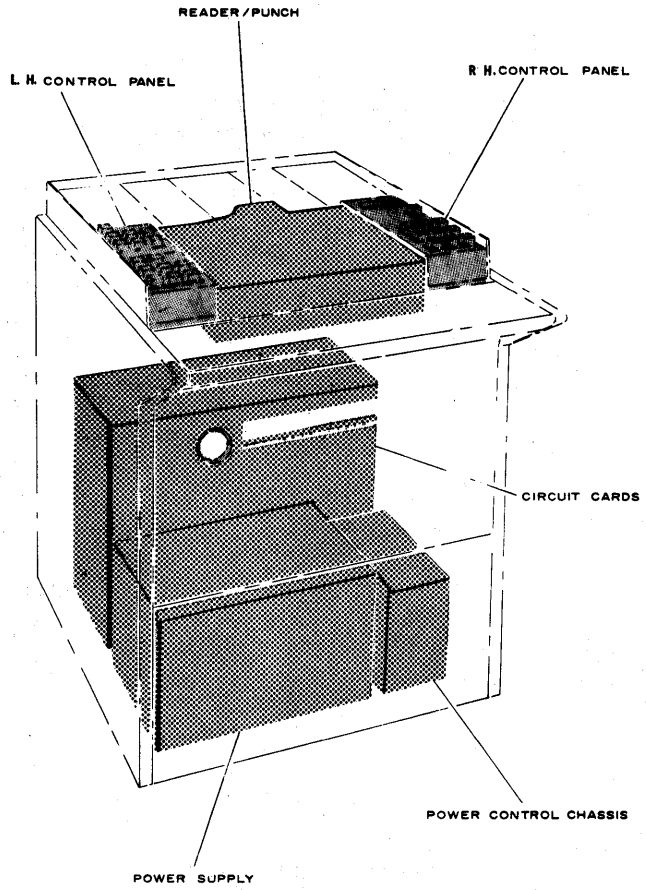


FIGURE 5-2 RPC 4430 READER/PUNCH ASSEMBLY
(4 ILLUSTRATIONS)

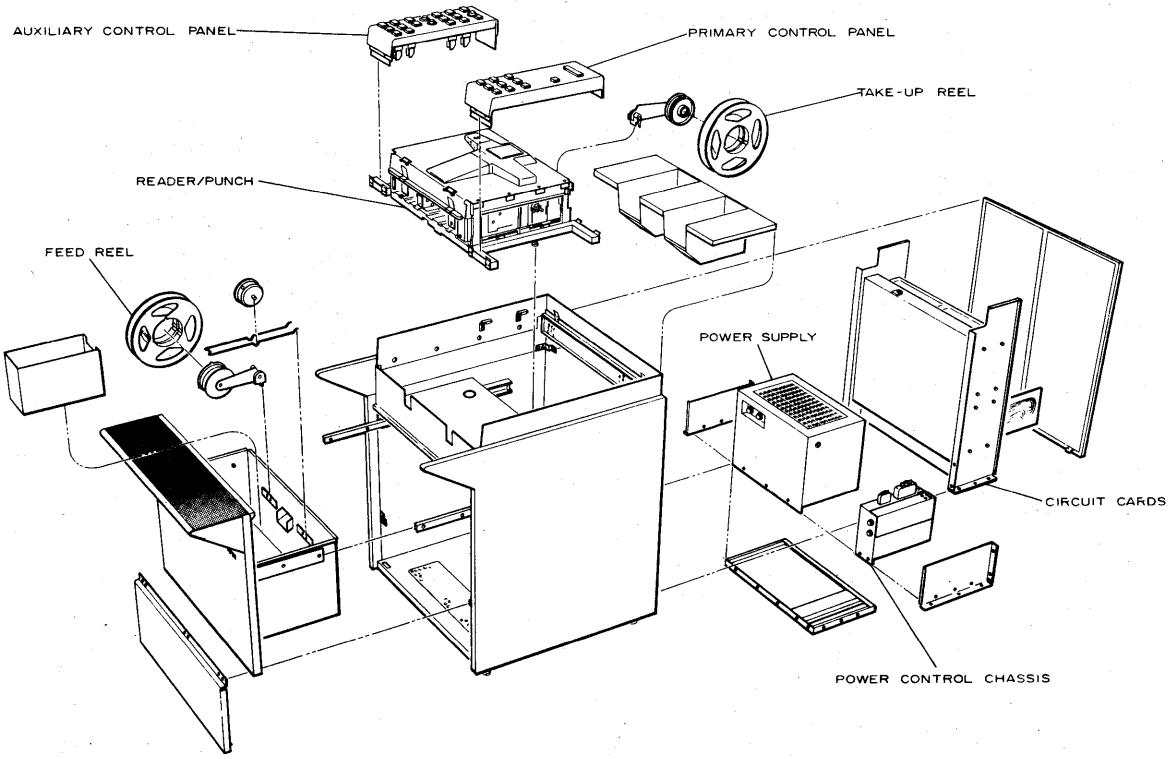


FIGURE 5-2 (2 of 4)

Mod 4343

LOWER ROW RIGHT TO LEFT

POSITION	CARD			DRAWING NO.
1	CARD	1	SYSTEM CONTROL (ON-LINE)	L200006090
2	CARD	2		L200006246
3	CARD	3		L200006247
4	CARD	4		L200006248
5	CARD	5		L200007201
6	CARD	6		L200006236
7	CARD	7	READER CONTROL	L200006249
8	CARD	8		L200006250
9	CARD	9	PUNCH CONTROL	L200006251
10	CARD	10		L200006252
11	CARD	11		L200006253
12	CARD	12	SYSTEM CONTROL (OFF-LINE)	L200006254
13	CARD	13		L200006255
14	CARD	14	PRIMARY TYPEWRITER CONTROL	L200007202
15	CARD	15		L200007203
16	CARD	16		L200007204
17	CARD	17		L200007205
18	SPARE			— — — —
19	SPARE			— — — —
20	SPARE			— — — —

Modified Cards

New cards

UPPER ROW RIGHT TO LEFT

POSITION	CARD			DRAWING NO.
21	RELAY	BOARD W-READER RELAY		L200002353
22	RELAY	BOARD X-PUNCH RELAY		L200002354
23	SPARE			— — — —
24	SPARE			— — — —
25	RELAY	BD VII	TYPEWRITER RELAYS	L200002356
26	RELAY	BD V7		L200002355
27	JUNCTION	STRIP #1		— — — —
28	JUNCTION	STRIP #2		— — — —
29	CARD	14	AUX TYPEWRITER CONTROL	L200007202
30	CARD	15		L200007203
31	CARD	16		L200007204
32	CARD	17		L200007205
33	SPARE			— — — —
34	SPARE			— — — —
35	SPARE			— — — —
36	SPARE			— — — —
37	SPARE			— — — —
38	SPARE			— — — —
39	SPARE			— — — —
40	SPARE			— — — —

FIGURE 5-2 (3 of 4)

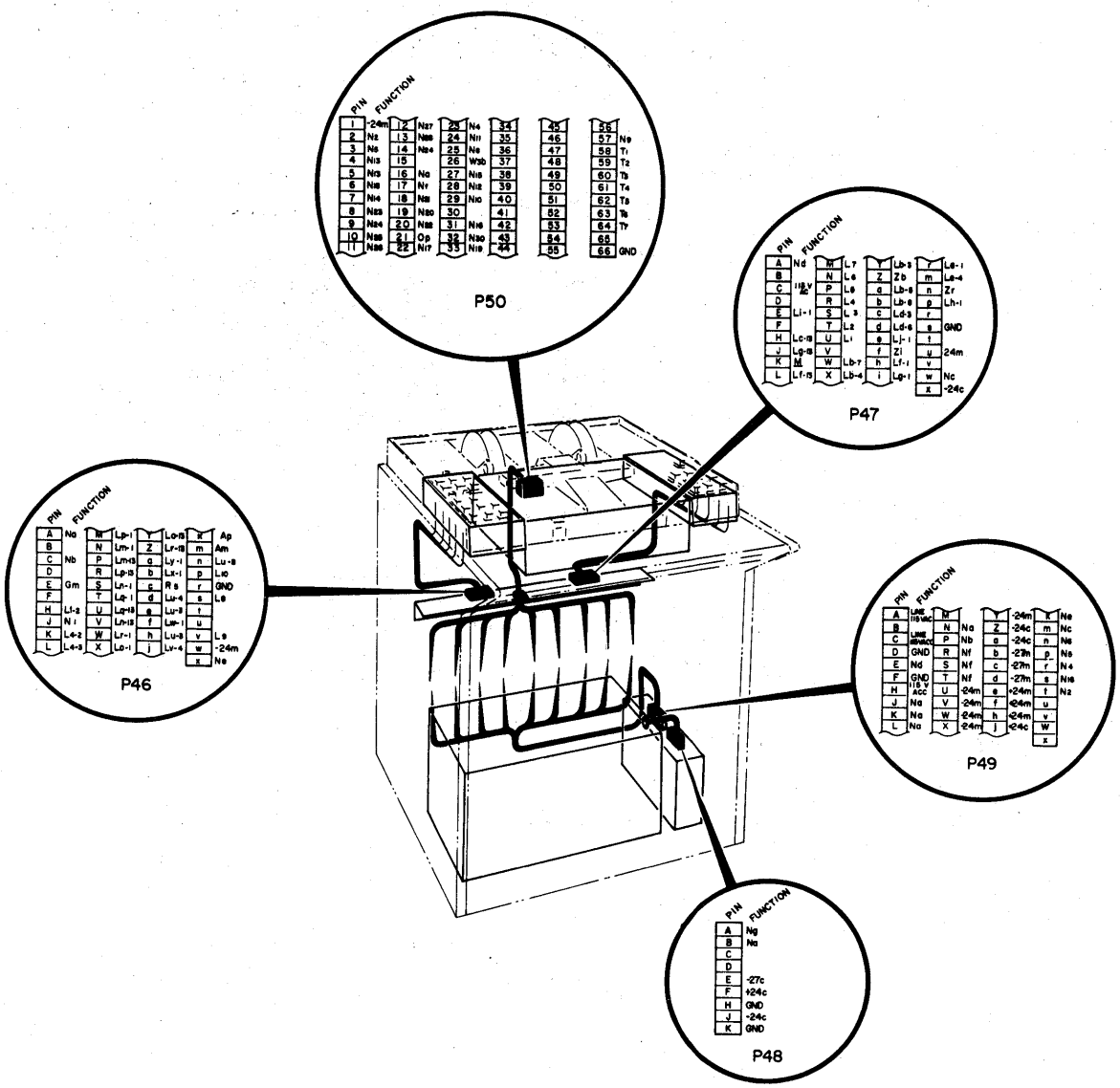


FIGURE 5-2 (4 of 4)

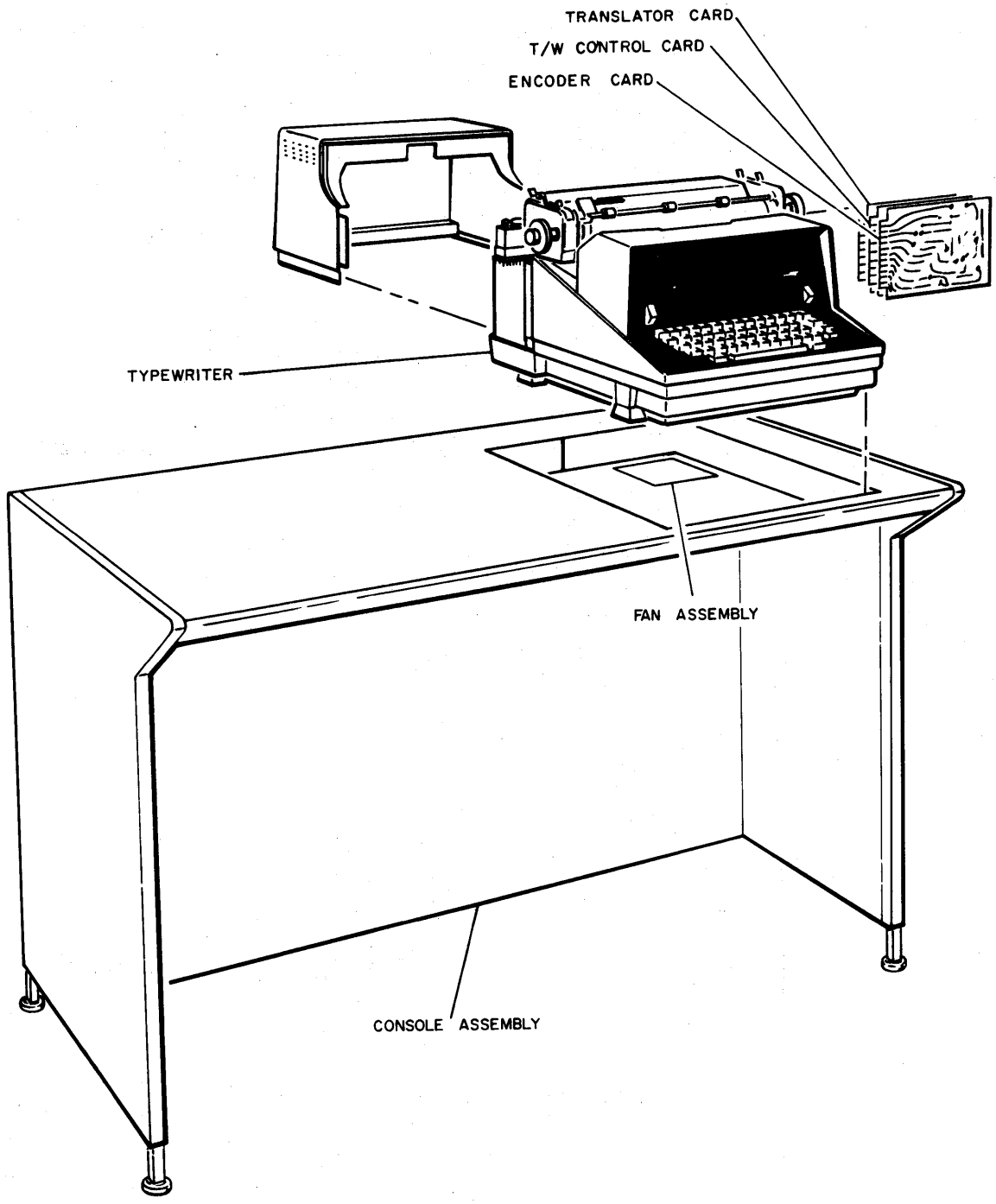


FIGURE 5-3 RPC 4480 TYPEWRITER ASSEMBLY

5.3 SYSTEM SCHEMATICS--In order to understand the interaction of the various units which make up the complete computer system and tape-typewriter system, system schematics are provided in Appendix 3. These schematics and a brief description of operation will assist in locating the source of troubles which occur in the system.

When the source of the trouble has been located, the card schematics which follow the system schematics may be used to repair or replace the components of the card which have failed.

5.4 MAGNETIC DRUM--The memory of the RPC-4010 Computer uses a magnetic drum manufactured by The Bryant Computer Products Company. The drum is a delicate precision instrument which requires that all maintenance and adjustment is carried out by thoroughly trained, experience personnel. It is recommended that maintenance and alignment of the memory section be confined to circuit adjustment and modifications in order to reduce the chance of damaging the drum.

Due to the extremely close tolerance between the drum surface and the heads, temperature variations and dust are apt to cause damage to the drum surface. The dust cover serves the dual purpose of protecting the drum from dust and of maintaining equal temperature of the shroud and drum. The dust cover should be removed only when necessary, and never for long periods of time. After stopping the drum, a minimum of four hours must elapse before the dust cover is removed. This allows the drum and the shroud to reach room ambient temperature.

CAUTION

To operate the drum with the dust cover removed, it must be removed before starting, with the drum at room ambient temperature and must be replaced before stopping the drum.

Removing the dust cover while the drum is operating will allow the shroud to cool suddenly, and by its contraction drive the heads into the drum surface. If the drum is allowed to stop with the dust cover removed, the shroud will cool more rapidly than the drum, again driving the heads into the drum surface.

All main memory heads (figure 5-4) should have a minimum signal at 120 KC of 20 millivolts per half or 40 millivolts across the whole head. All circulating heads and dual access heads should be adjusted axially so that both read and write heads are on the same track, i.e., read heads should be adjusted so that signals are of at least minimum amplitude and undistorted.

In the event that main memory heads or adjusted circulating heads fail to produce the minimum voltage, head replacement is necessary.

5.4.1 HEAD ADJUSTMENT AND REPLACEMENT PROCEDURE

The tolerances involved in the magnetic drum unit require careful fitting of replacement heads. The fitting of heads (figure 5-5) must follow the procedure given below.

CAUTION

The drum must be at room ambient temperature when replacing heads. All equipment and components must be free of grease and chips.

Step 1--Remove inoperative head from its head mount. Make sure head mount is tight. Press replacement head very lightly against drum surface and tighten head set screw.

CAUTION

Do not exert excessive pressure on drum surface.

Step 2--Remove head mount from shroud and install in head setting fixture supplied with computer.

NOTE

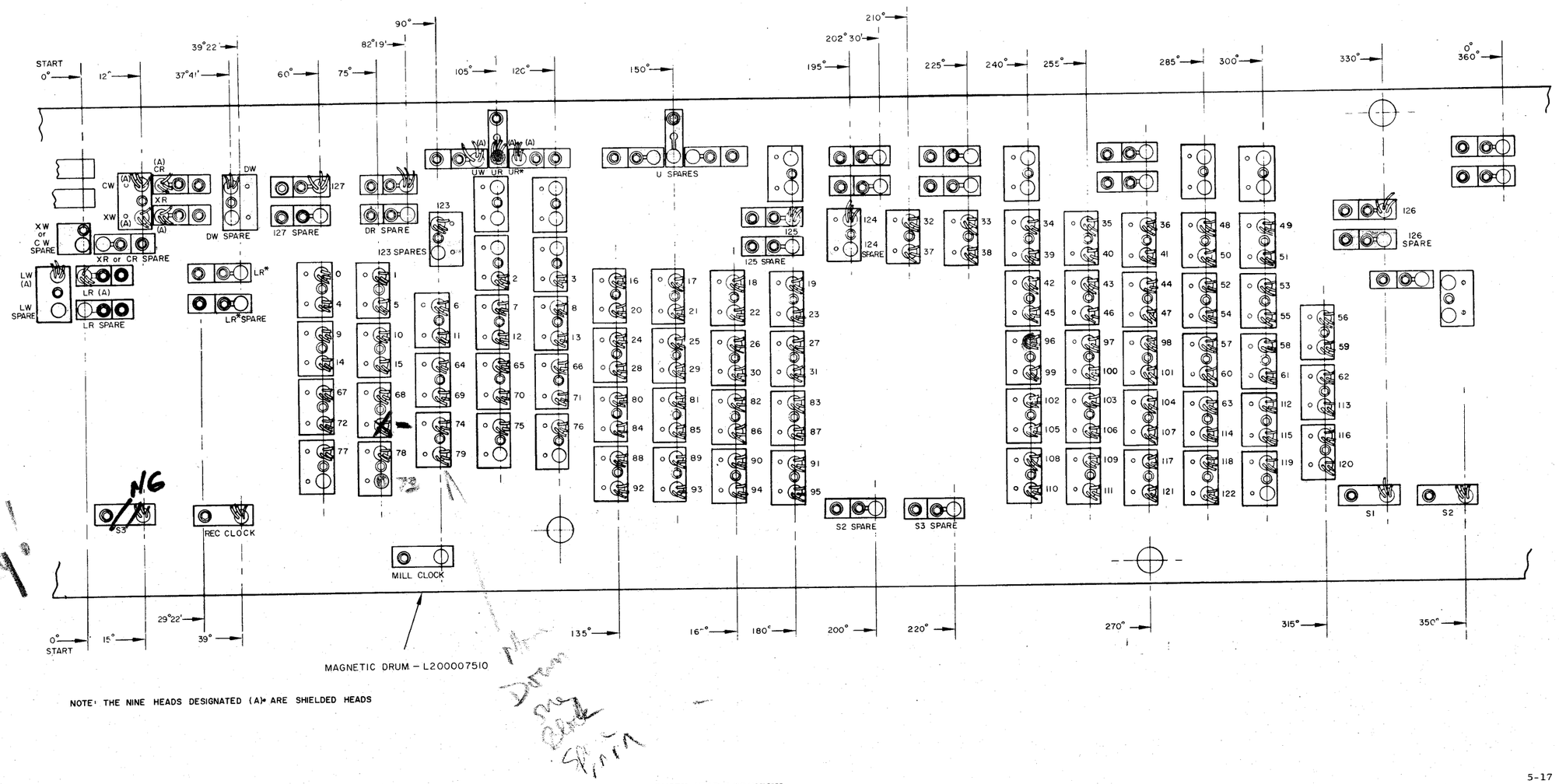
The head setting fixture is adaptable for either main memory or circulating line head mounts.

Lock head mount in head setting fixture. Adjust height so that head is in contact with the polished surface of head setting fixture. Hold fixture up to light and view from two sides, at least 90° apart, to insure that the head is exactly perpendicular to the polished surface.

Step 3--Loosen the head set screw and place a 1.3 mil (0.0013") shim between the head face and the surface of the head setting fixture. Align the heads in the head mounts, using the scribed marks on both components. This insures that the poles of the head will be aligned with the memory track on the drum. Tighten the head in the head mount.

Step 4--Remove head mounts from head setting fixture and install on drum shroud. The resulting head-to-drum surface clearance will be 1.3 mils at room ambient temperature. Rotate drum by hand, using a soft plastic-tipped rod through an inspection port, and make sure heads clear drum surface throughout rotation.

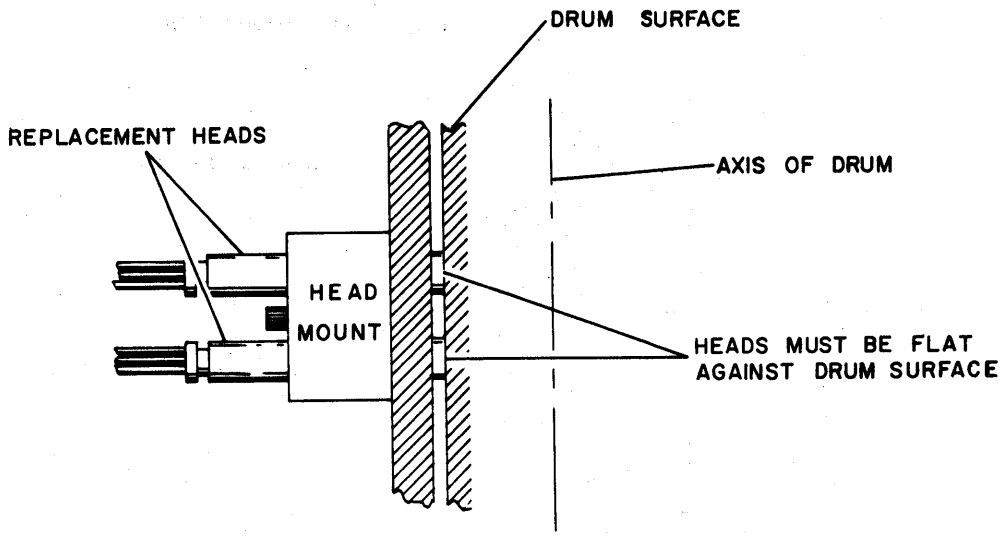
5.5 LOGIC BOARD--The diode logic which combines the signals in the RPC-4010 Computer is located on the logic board. In order to test and repair the gates which perform the logical combinations, the signal which is sought is located in the index pages (Table 5-1). The index gives the page of figure 5-6 which contains a detail drawing and location reference for the gate providing the specific signal.



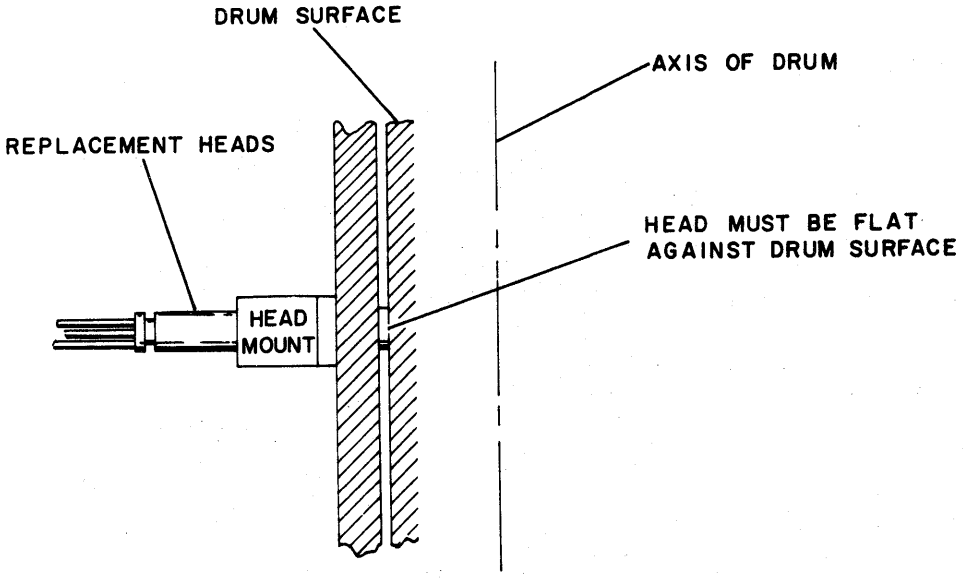
MAGNETIC DRUM – L200007510

NOTE: THE NINE HEADS DESIGNATED (A) ARE SHIELDED HEADS

FIGURE 5-4 MAIN MEMORY HEAD LOCATIONS



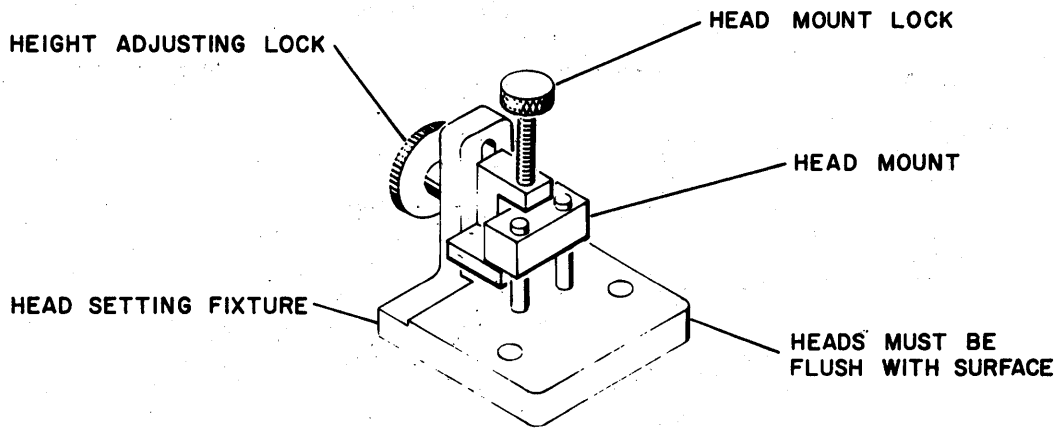
MAIN MEMORY HEADS



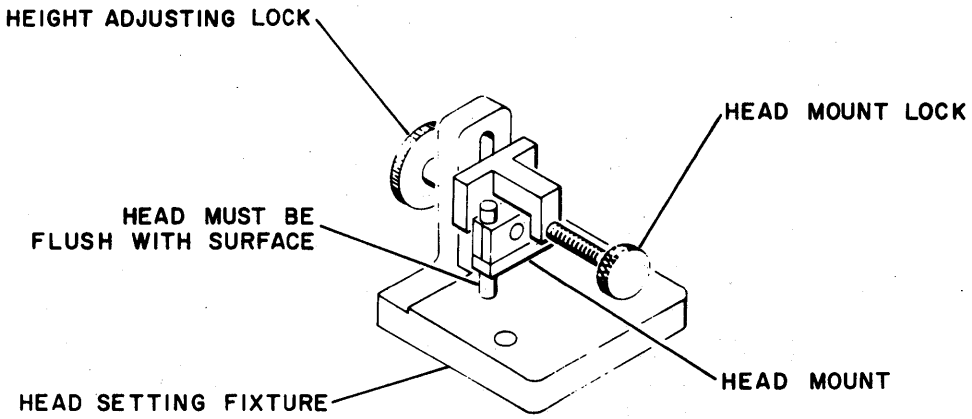
RECIRCULATING LINE HEADS

NOTE: DO NOT USE EXCESSIVE PRESSURE ON HEADS.

FIGURE 5-5 INSTALLATION OF MAGNETIC HEADS
(6 ILLUSTRATIONS)

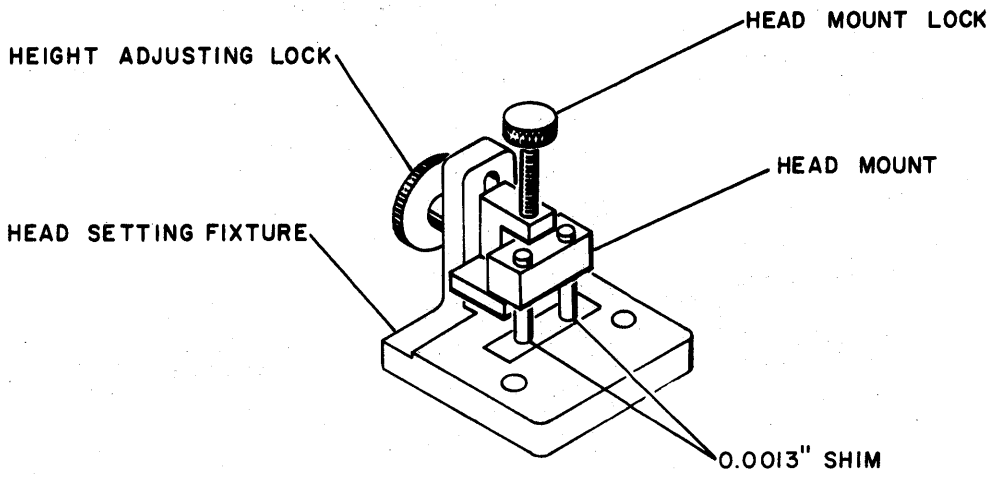


MAIN MEMORY HEADS

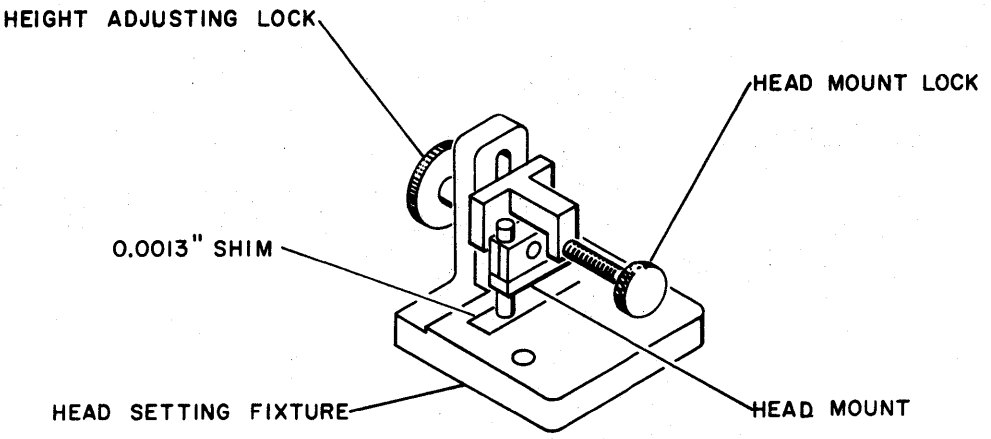


RECIRCULATING LINE HEADS

FIGURE 5-5 (2 of 4)

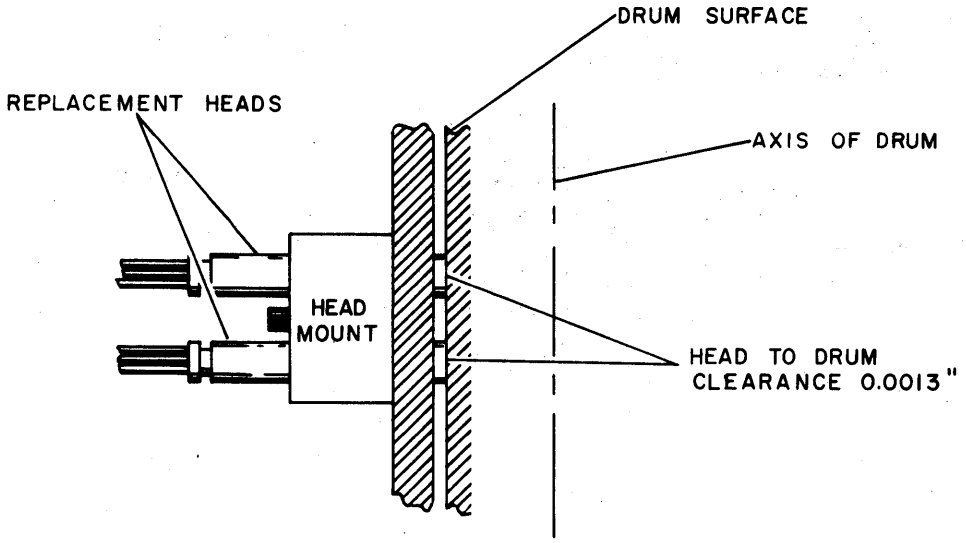


MAIN MEMORY HEADS

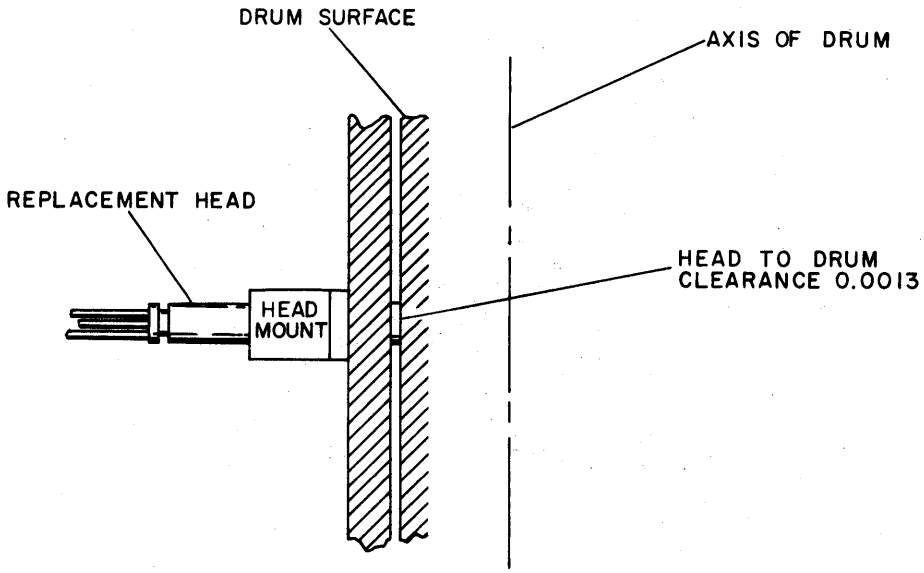


RECIRCULATING LINE HEADS

FIGURE 5-5 (3 of 4)



MAIN MEMORY HEADS



RECIRCULATING LINE HEADS

FIGURE 5-5 (4 of 4)

TABLE 5-1

LOCATION OF GATE OUTPUTS

	SIGNAL	LOCATION	PAGE NO.
Flip-Flop Input Signals	A'	XX-51	5-42
	$\underline{A}$'	XX-65	5-43
	B'	W-60	5-34
	$\underline{B}$'	JJ-46	5-39
	F'	A-79	5-29
	$\underline{F}$'	D-60	5-29
	G'	E-50	5-29
	$\underline{G}$'	J-39	5-30
	H'	J-46	5-30
	$\underline{H}$'	N-55	5-33
	K'	FF-59	5-39
	$\underline{K}$'	NN-60	5-40
	M'	f-41	5-45
	$\underline{M}$'	k-62	5-45
	N'	X-64	5-35
	$\underline{N}$'	W-73	5-35
	P_1'	D-3	5-28
	$\underline{P_1}$'	D-13	5-28
	P_2'	H-13	5-28
	$\underline{P_2}$'	M-10	5-30
	P_3'	W-14	5-32
	$\underline{P_3}$'	EE-12	5-37
	P_4'	JJ-3	5-38
	$\underline{P_4}$'	NN-3	5-38
	P_5'	TT-7	5-41
	$\underline{P_5}$'	XX-5	5-41
	P_6'	XX-17	5-41
	$\underline{P_6}$'	XX-23	5-41
	P_7'	b-10	5-43
	$\underline{P_7}$'	f-7	5-44
	Q_1'	N-21	5-32
	$\underline{Q_1}$'	W-22	5-32
	Q_2'	AA-23	5-37
	$\underline{Q_2}$'	BB-22	5-37
	Q_3'	FF-21	5-39

TABLE 5-1 (Cont.)

	SIGNAL	LOCATION	PAGE NO.
Flip-Flop Input Signals (Cont.)	$\underline{Q}_3'$	JJ-25	5-39
	Q_4'	KK-21	5-40
	$\underline{Q}_4'$	NN-25	5-40
	Q_5'	PP-21	5-41
	$\underline{Q}_5'$	TT-25	5-41
	R'	T-64	5-35
	$\underline{R}'$	W-70	5-35
	C'	y-80	5-48
	L'	TT-91	5-46
	U'	AA-92	5-36
	X'	M-100	5-31
Main Memory Input Signals	W'	p-95	5-49
	V'	y-91	5-49
Input-Output Signals	Y_o	N-64	5-33
	Y_i	BB-68	5-35
	P_O	1-27	5-47
Addition Alpha Signals	I_1'	p-44	5-47
	I_2'	u-44	5-47
	S	y-70	5-48
Miscellaneous Alpha Signals	e_1	YY-61	5-44
	e_2	p-58	5-49
	e_3	H-23	5-28
	e_4	b-60	5-44
	e_5	UU-37	5-42
	e_6	YY-37	5-44
	e_7	S-27	5-32
	e_8	TT-61	5-42
	e_9	W-25	5-32
	e_{10}	k-13	5-46
	e_{11}	p-13	5-47
	e_{12}	AA-33	5-37
	e_{13}	YY-39	5-44

TABLE 5-1 (Cont.)

	SIGNAL	LOCATION	PAGE NO.
Phase Control Alpha Signals	f_1	r-51	5-47
	f_2	c-54	5-45
	f_3	c-51	5-45
	f_4	FF-61	5-39
	f_5	r-53	5-47
	f_6	TT-37	5-41
	f_7	KK-35	5-40
	f_8	N-23	5-32
	f_9	b-68	5-44
	f_{10}	c-62	5-45
	f_{11}	X-61	5-35
	f_{12}	E-51	5-30
	f_{13}	S-91	5-34
	f_{14}	T-61	5-35
Command Alpha Signals	k_1	BB-65	5-35
	k_2	J-18	5-30
	k_3	S-34	5-33
	k_4	FF-14	5-37
	k_5	X-19	5-37
	k_6	J-65	5-31
	k_8	XX-9	5-41
	k_9	M-88	5-32
	k_{10}	N-58	5-33
	k_{11}	N-61	5-33
	k_{12}	KK-61	5-41
	k_{13}	J-54	5-31
	k_{14}	A-22	5-28
	k_{15}	E-25	5-28
	k_{16}	J-25	5-30
	k_{17}	f-22	5-45
	k_{18}	YY-64	5-44
	k_{19}	S-74	5-33
	k_{20}	J-61	5-31
	k_{21}	J-58	5-31

TABLE 5-1 (Cont.)

	SIGNAL	LOCATION	PAGE NO.
Command Alpha Signals (Cont.)	k_{22}	FF-64	5-39
	k_{23}	S-76	5-33
	k_{24}	S-82	5-34
	k_{25}	N-88	5-34
	k_{26}	N-85	5-34
	k_{27}	AA-17	5-37
	k_{28}	k-4	5-46
	k_{29}	c-64	5-45
	k_{30}	X-67	5-35
	k_{31}	c-19	5-45
	k_{32}	H-21	5-28
	k_{33}	c-16	5-45
	k_{34}	D-61	5-30
	k_{36}	KK-64	5-41
	k_{38}	KK-37	5-40
	k_{39}	FF-18	5-37
	k_{40}	KK-67	5-41
	t_1	FF-69	5-40
	t_2	E-81	5-30
	t_3	N-71	5-33
	t_4	E-83	5-30
	t_5	r-81	5-49
	t_6	1-21	5-47
	t_8	N-20	5-32

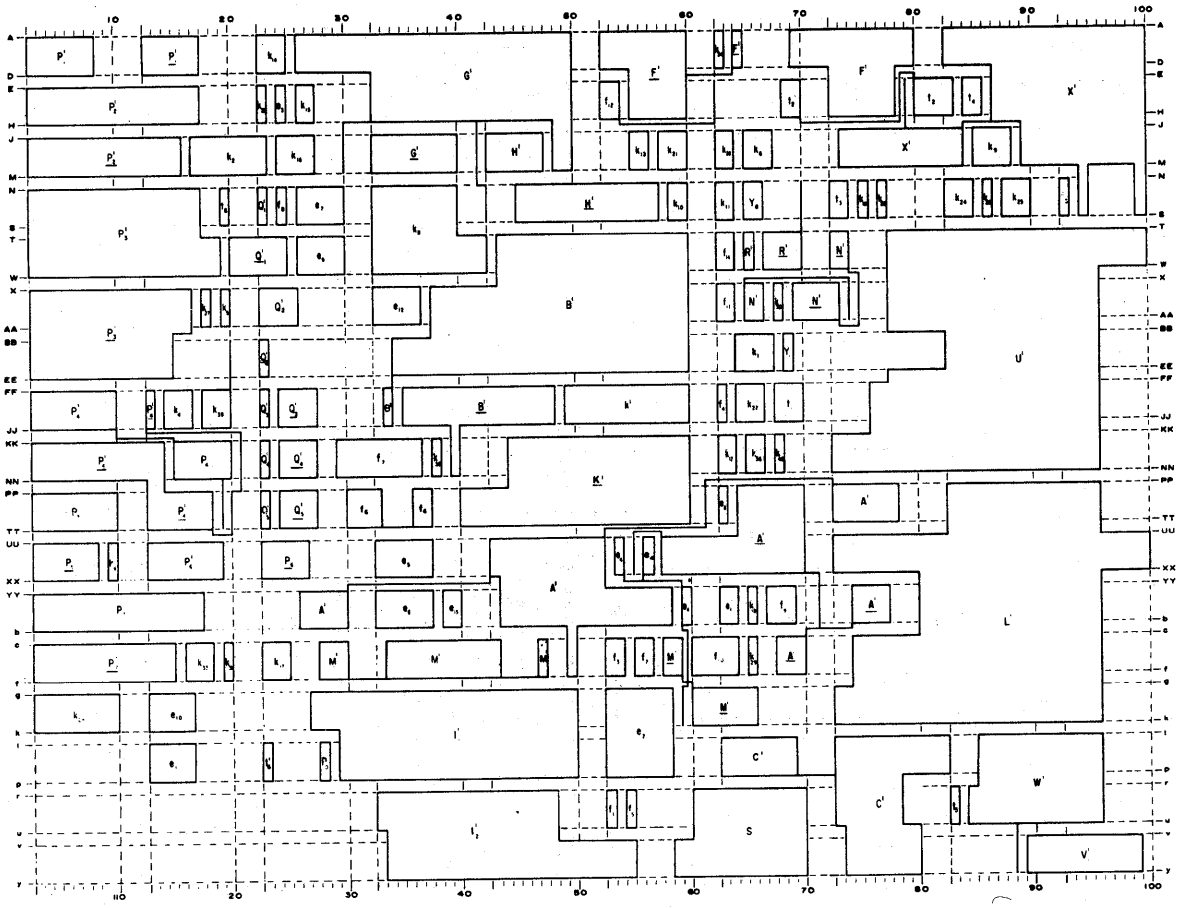


FIGURE 5-6 RPC 4010 COMPUTER LOGIC CIRCUITS
(23 ILLUSTRATIONS)

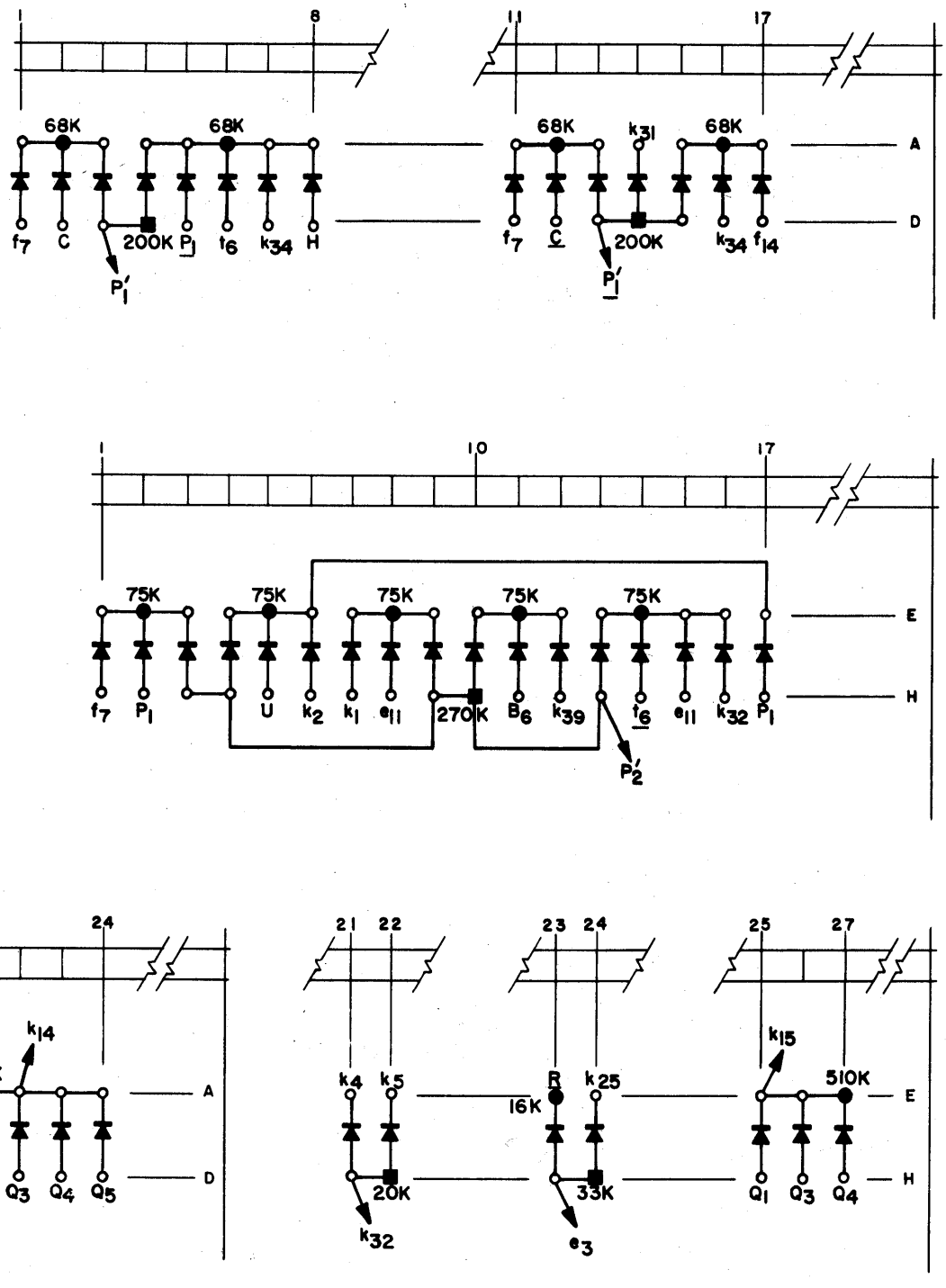


FIGURE 5-6 (2 of 23)

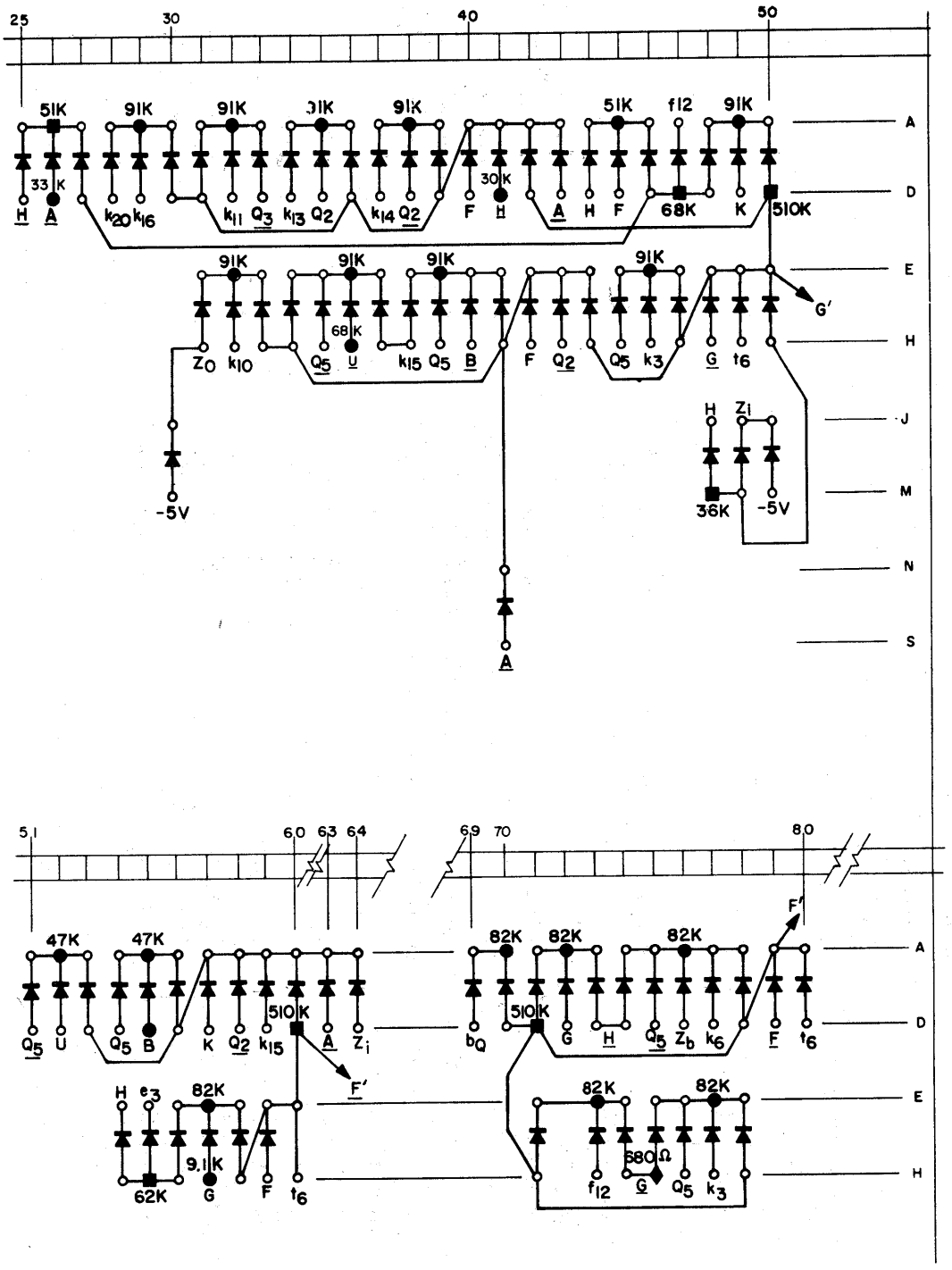


FIGURE 5-6 (3 of 23)

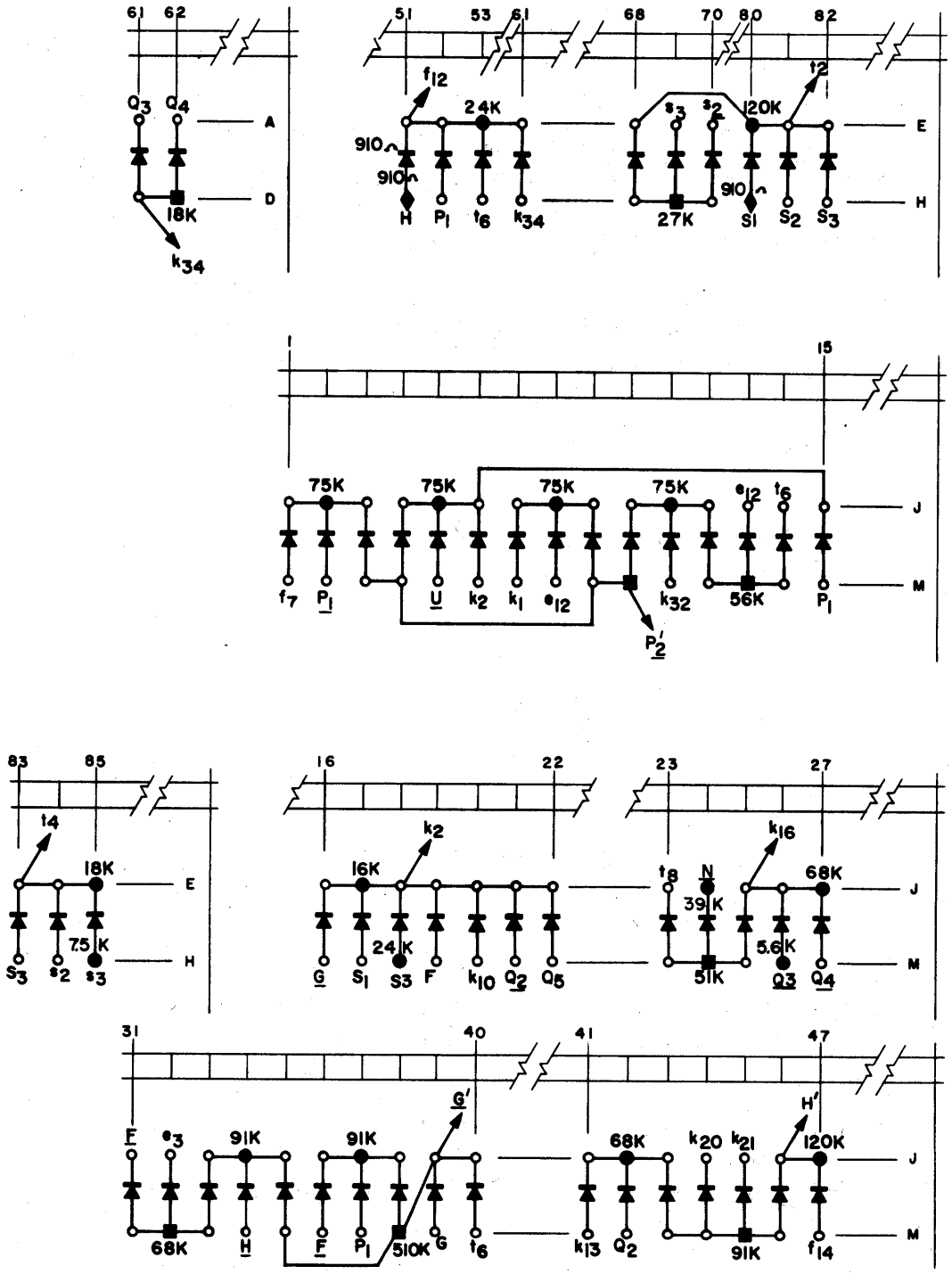


FIGURE 5-6 (4 of 23)

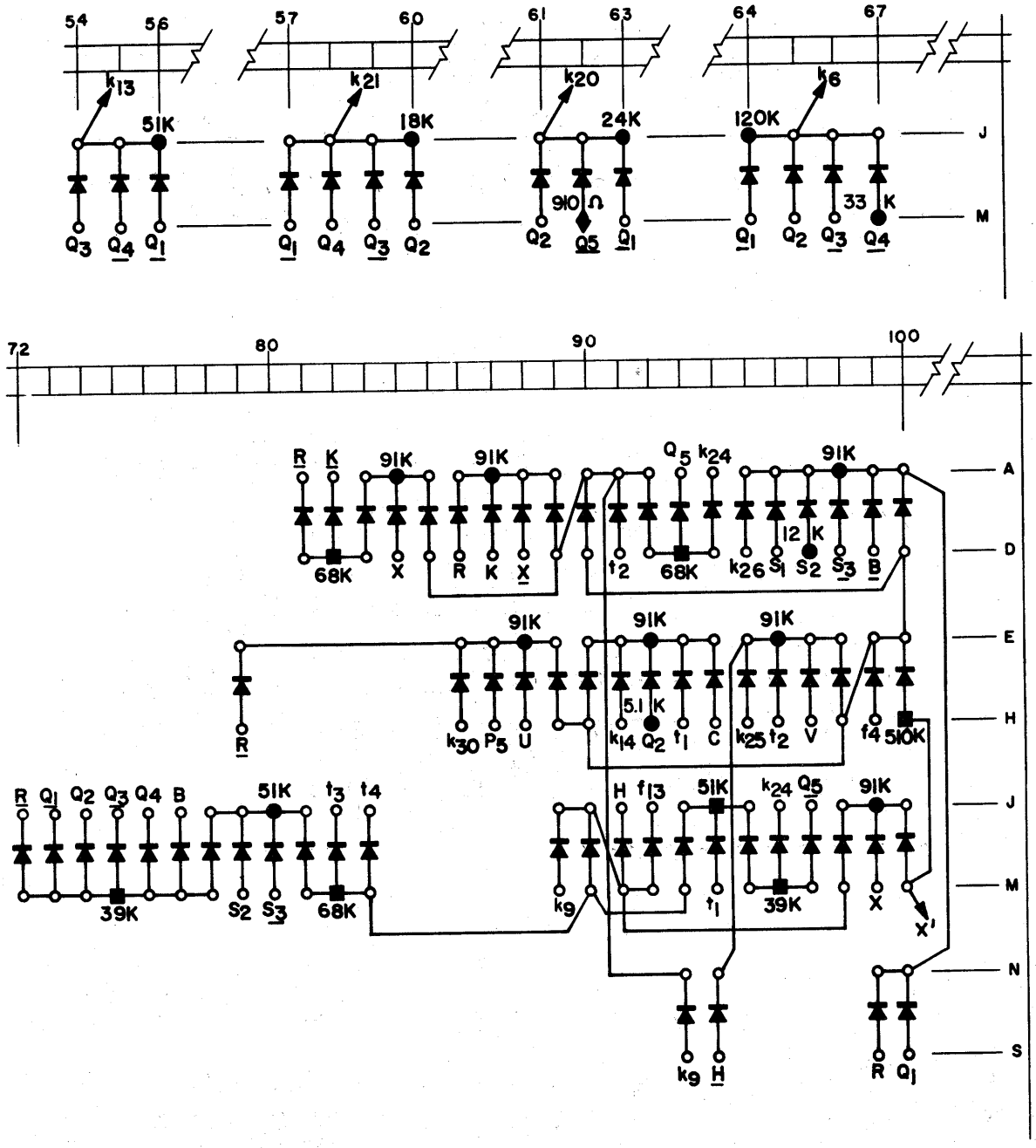


FIGURE 5-6 (5 of 23)

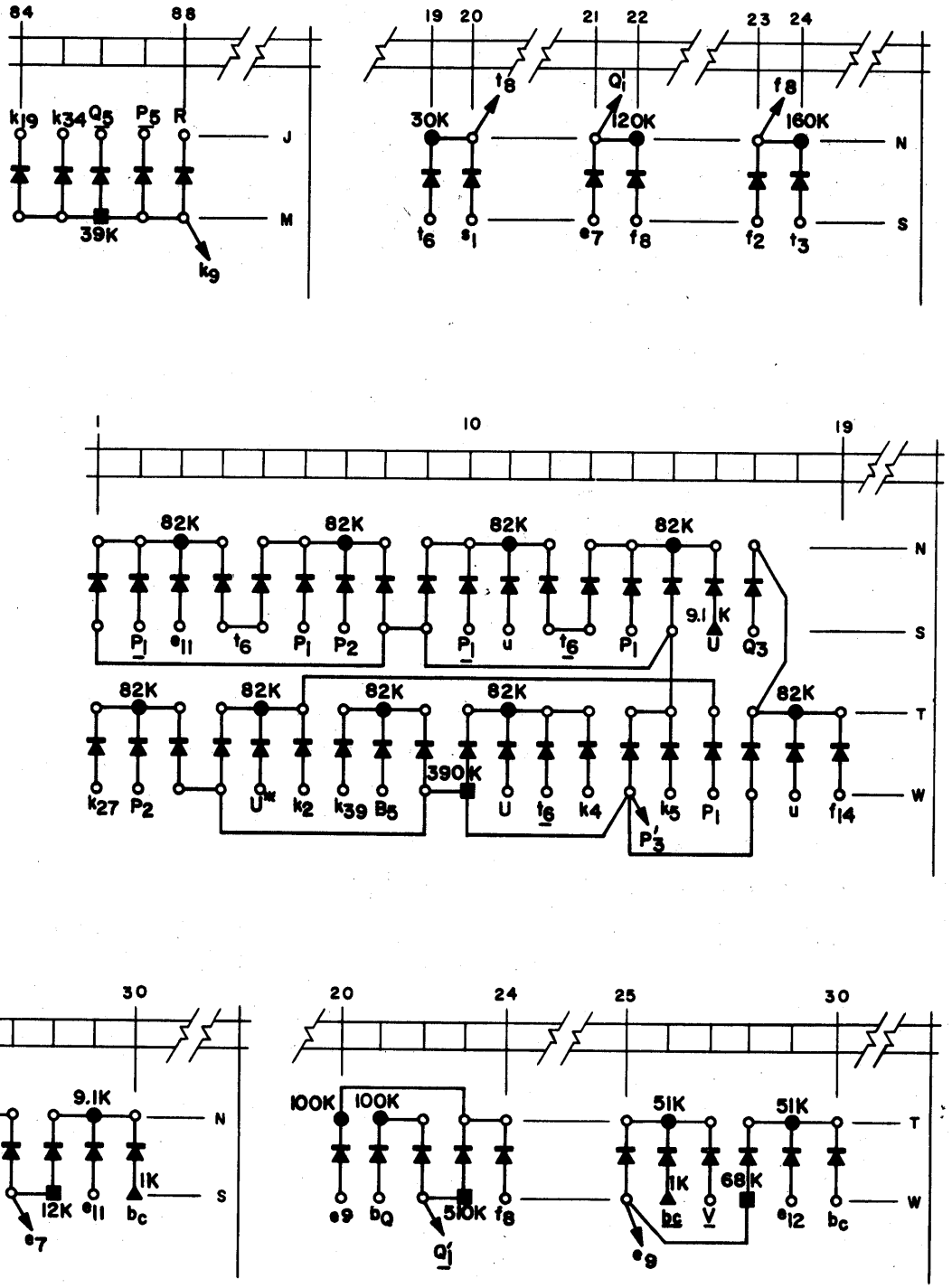


FIGURE 5-6 (6 of 23)

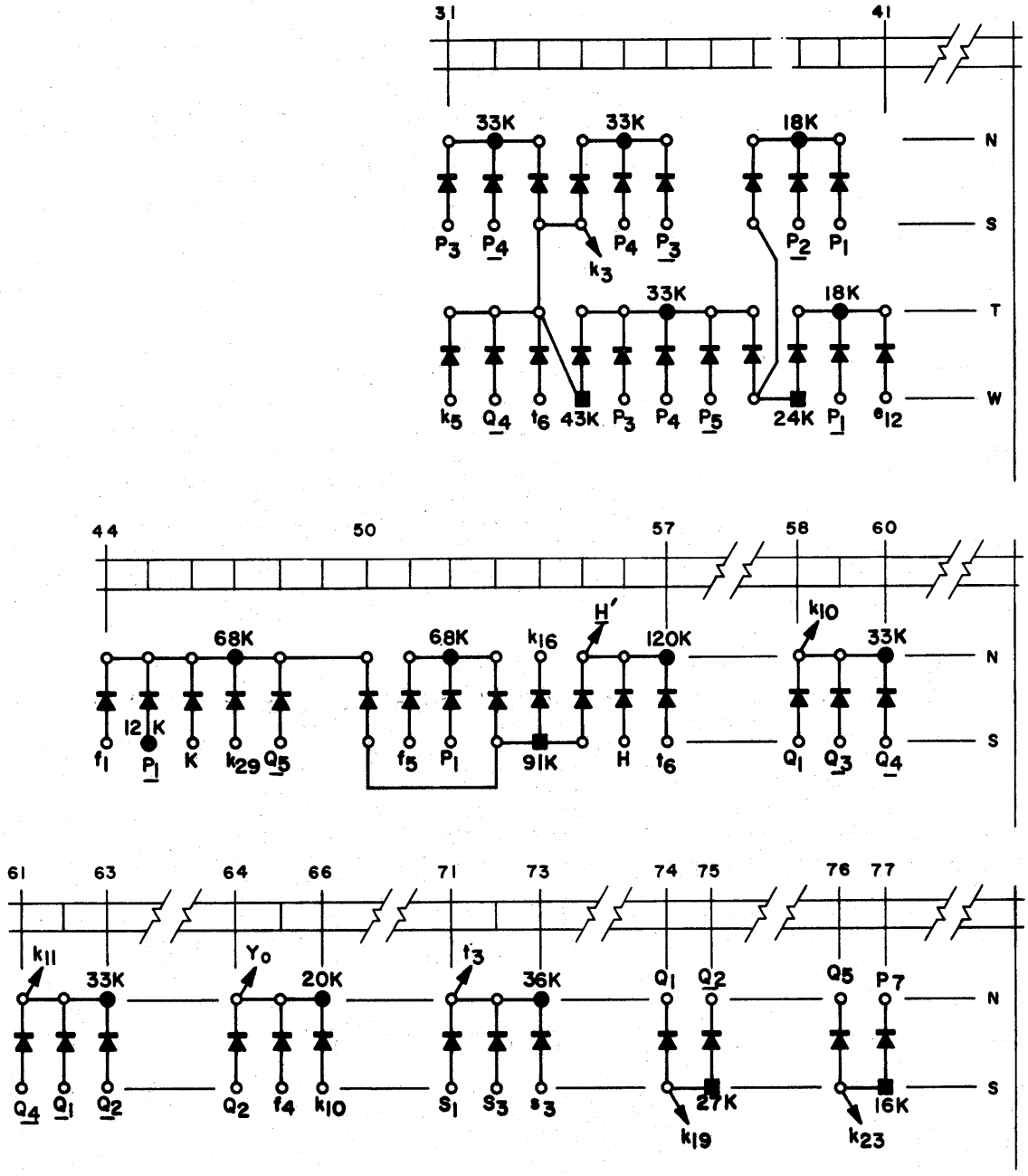


FIGURE 5-6 (7 of 23)

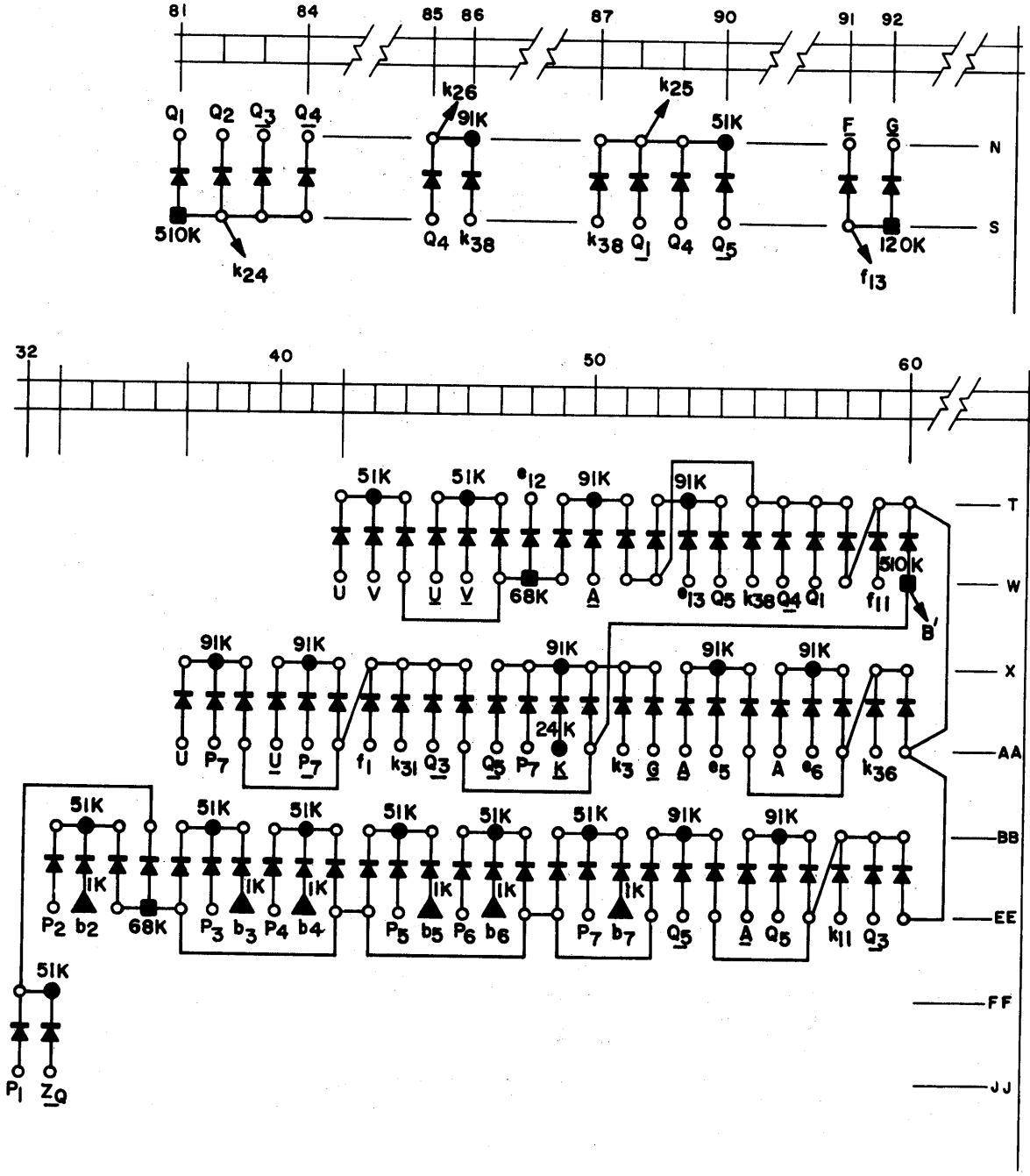


FIGURE 5-6 (8 of 23)

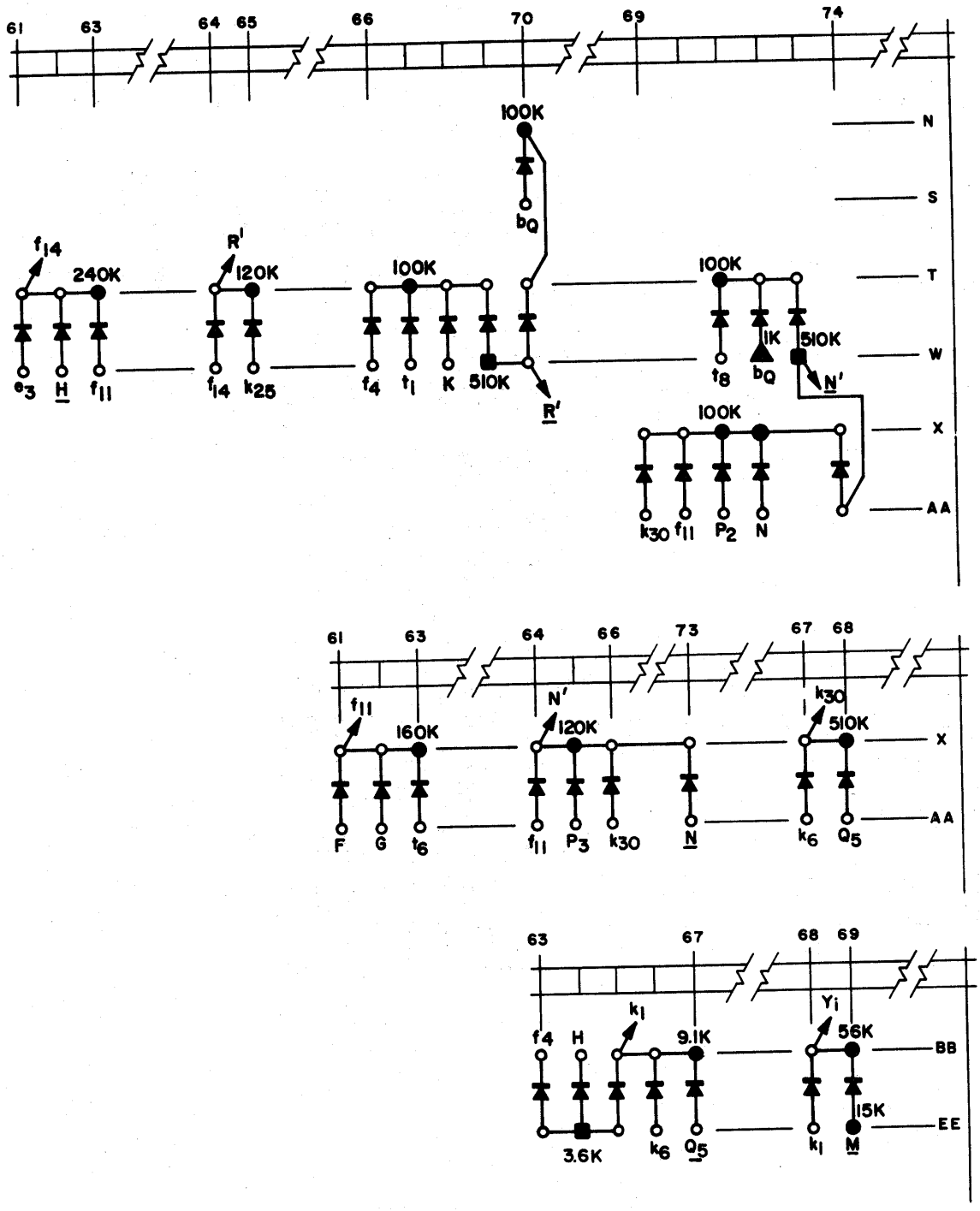


FIGURE 5-6 (9 of 23)

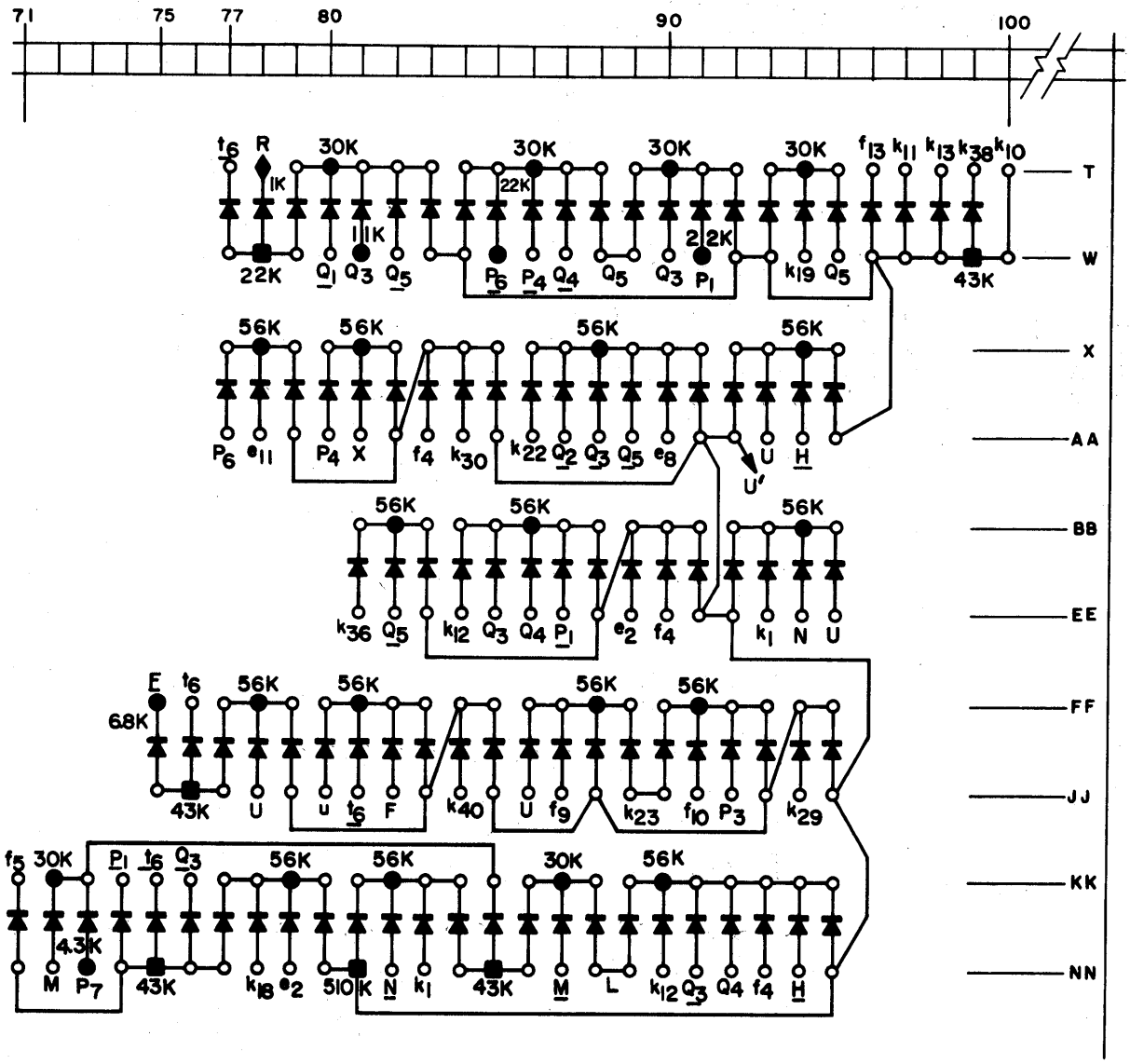


FIGURE 5-6 (10 of 23)

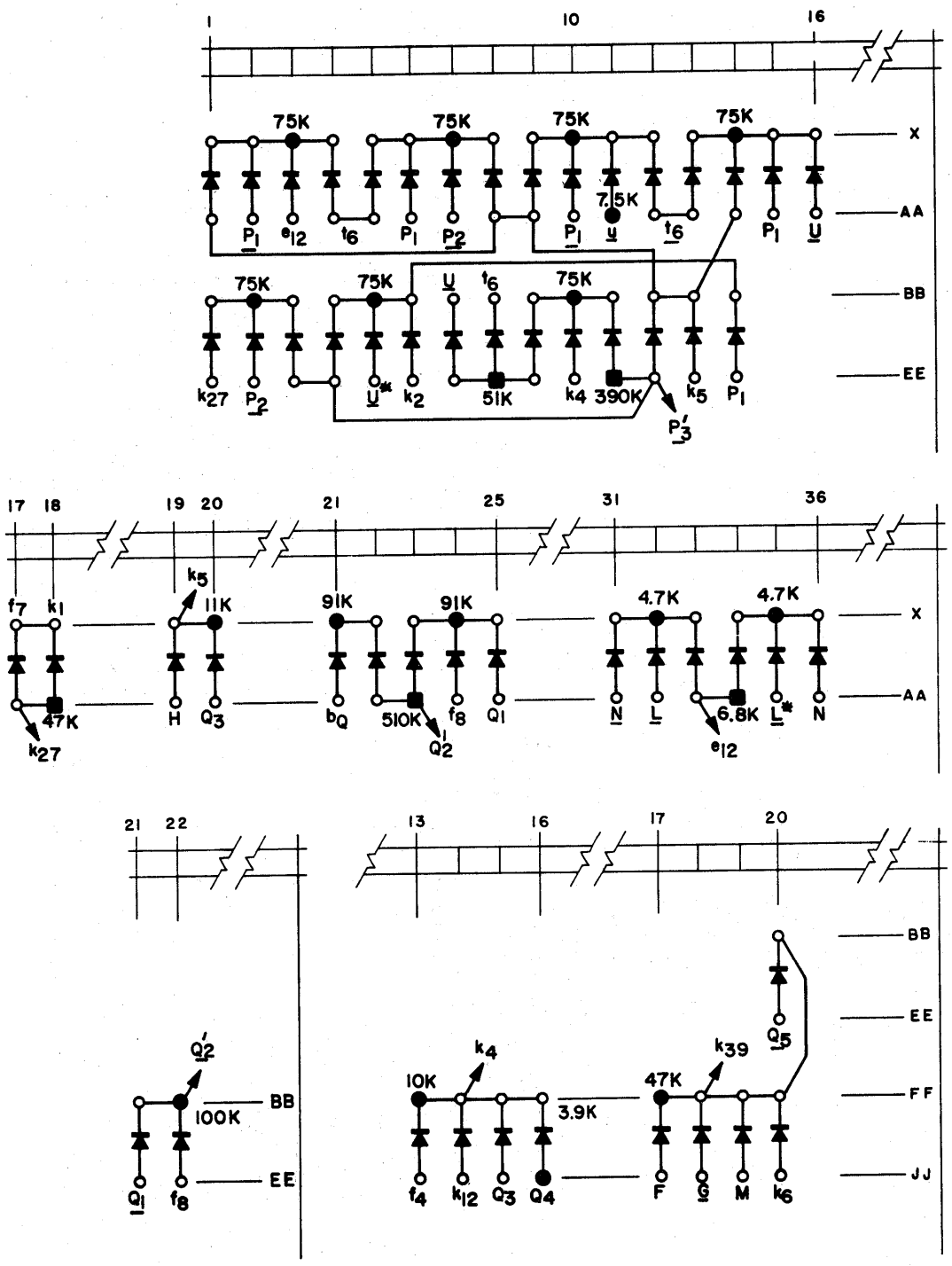


FIGURE 5-6 (11 of 23)

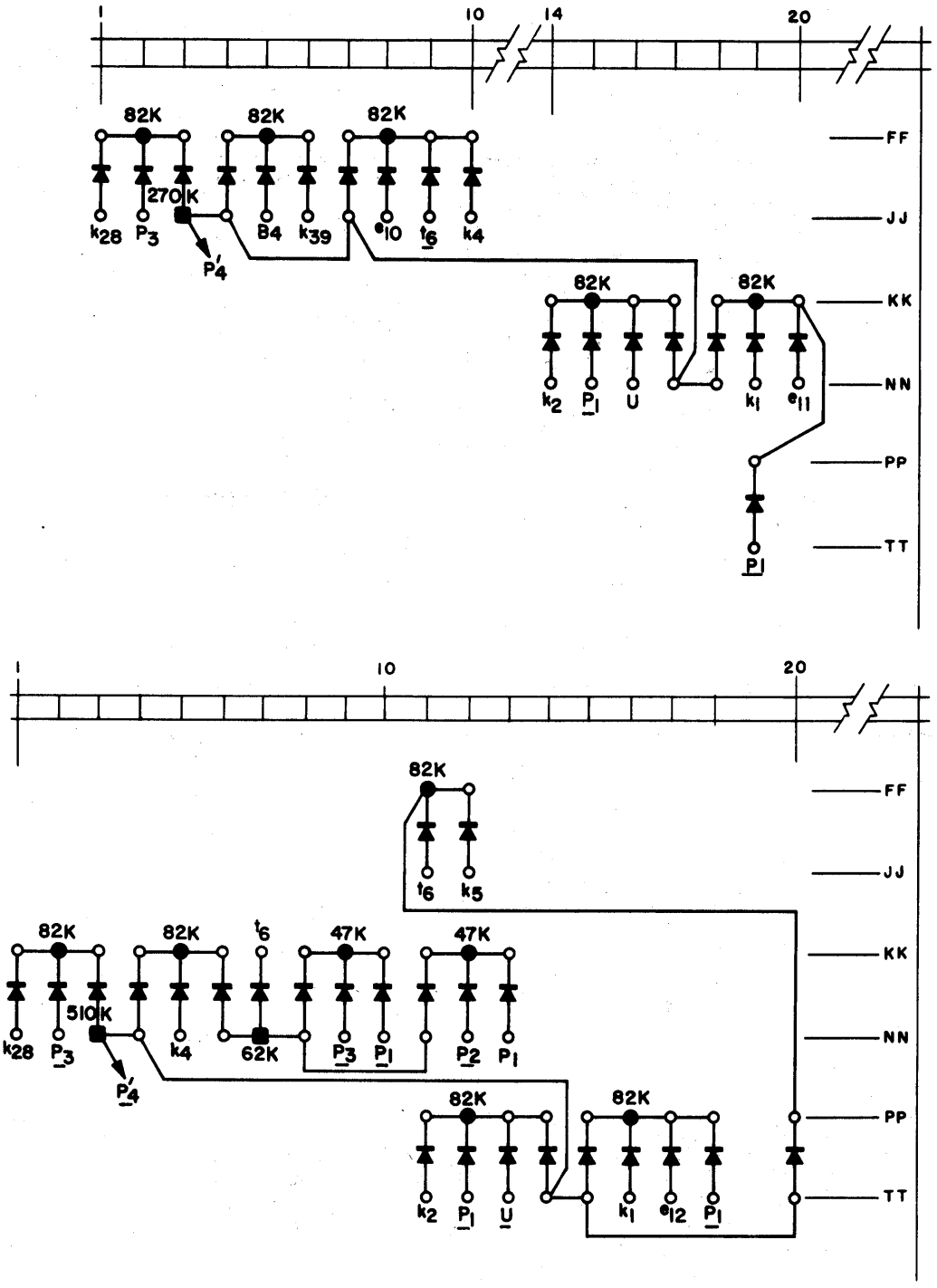


FIGURE 5-6 (12 of 23)

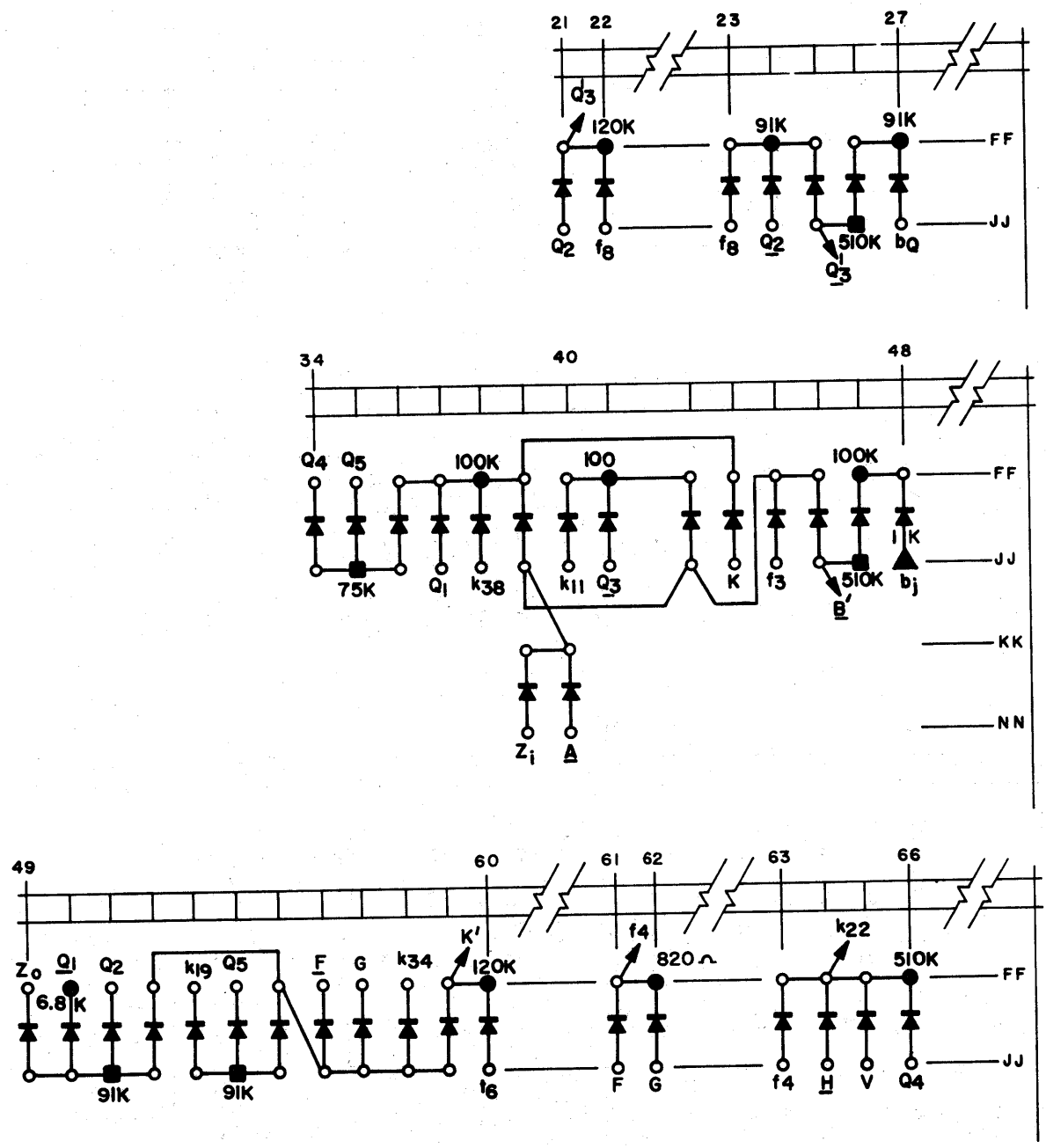


FIGURE 5-6 (13 of 23)

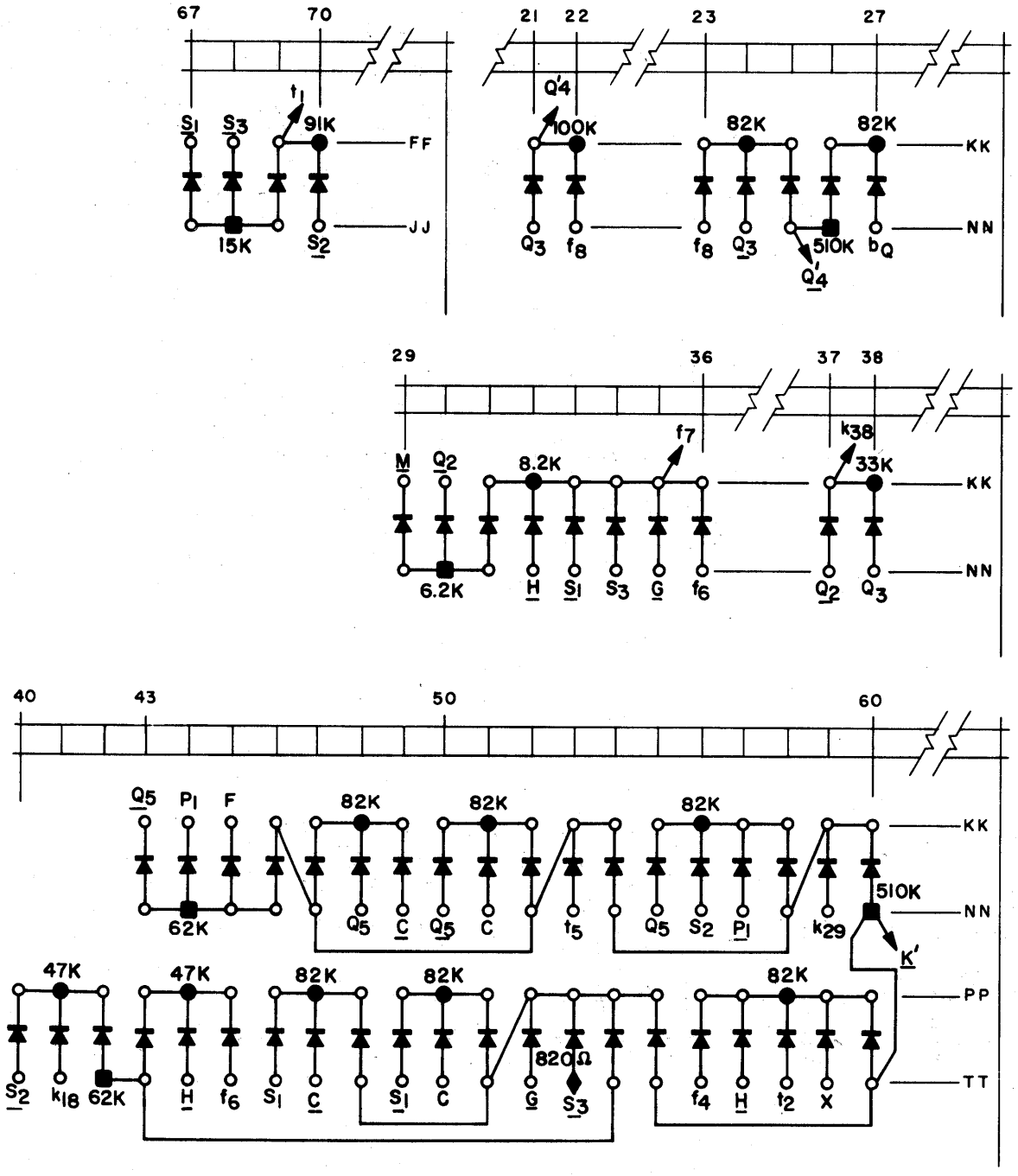


FIGURE 5-6 (14 of 23)

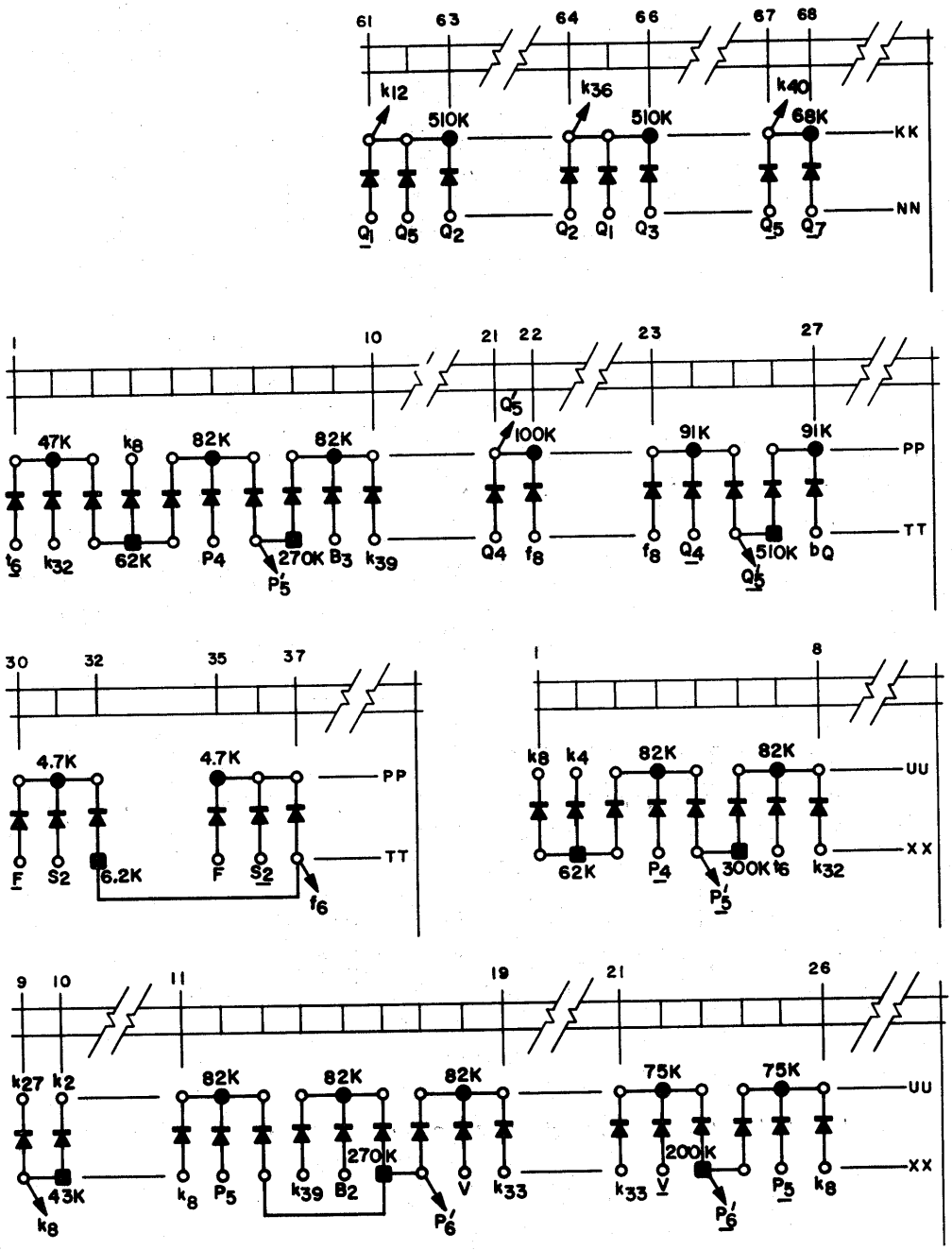


FIGURE 5-6 (15 of 23)

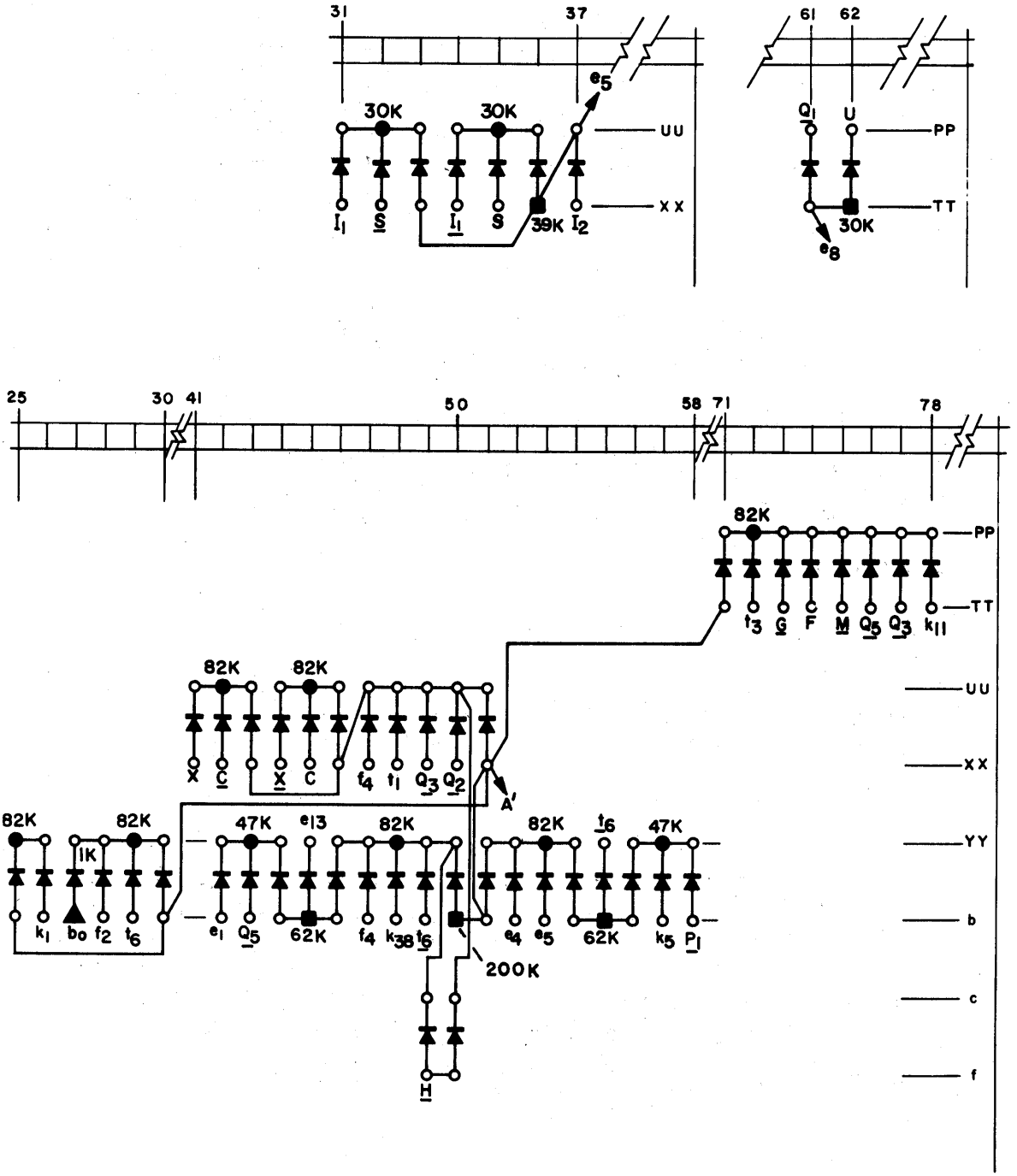


FIGURE 5-6 (16 of 23)

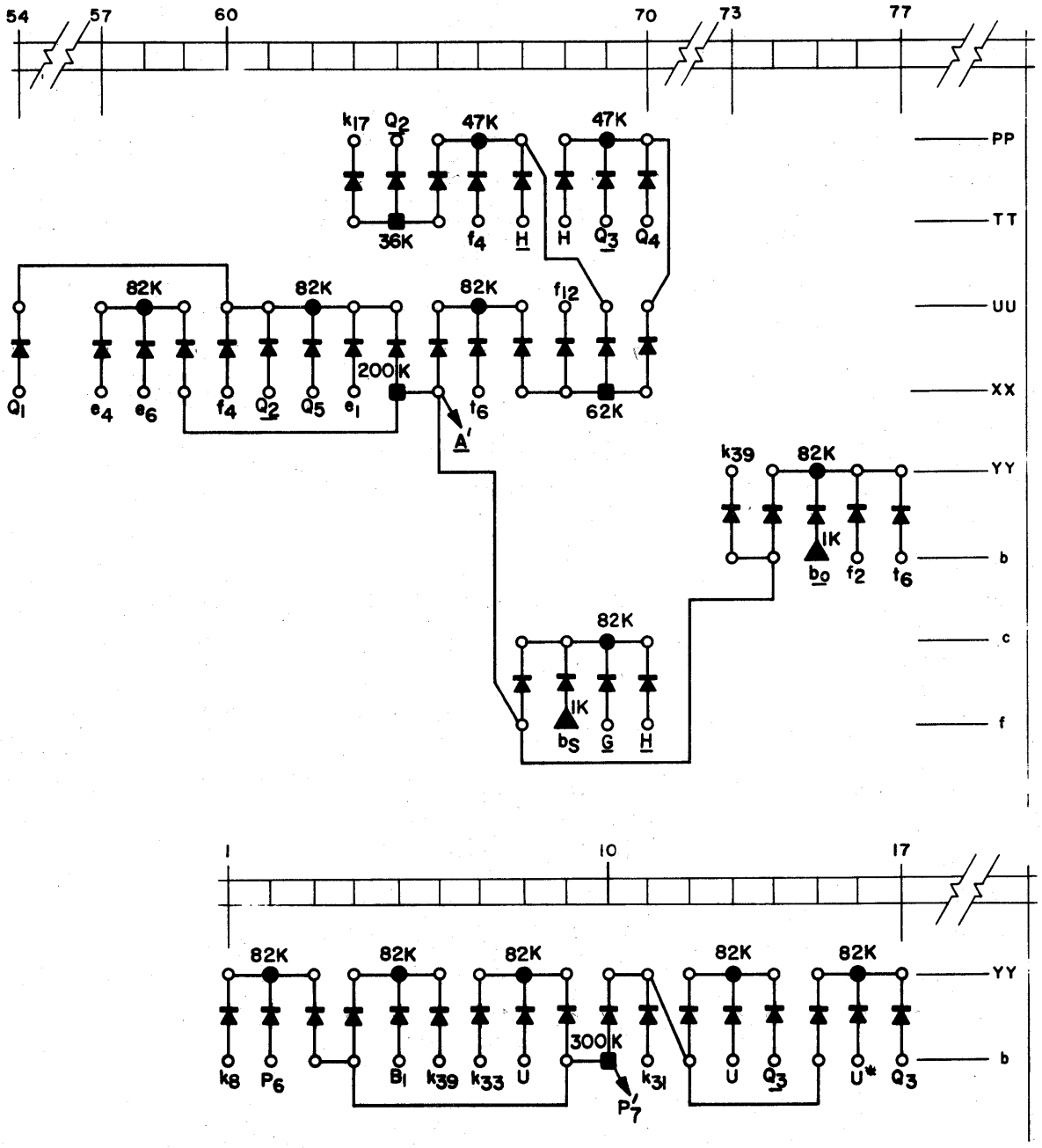


FIGURE 5-6 (17 of 23)

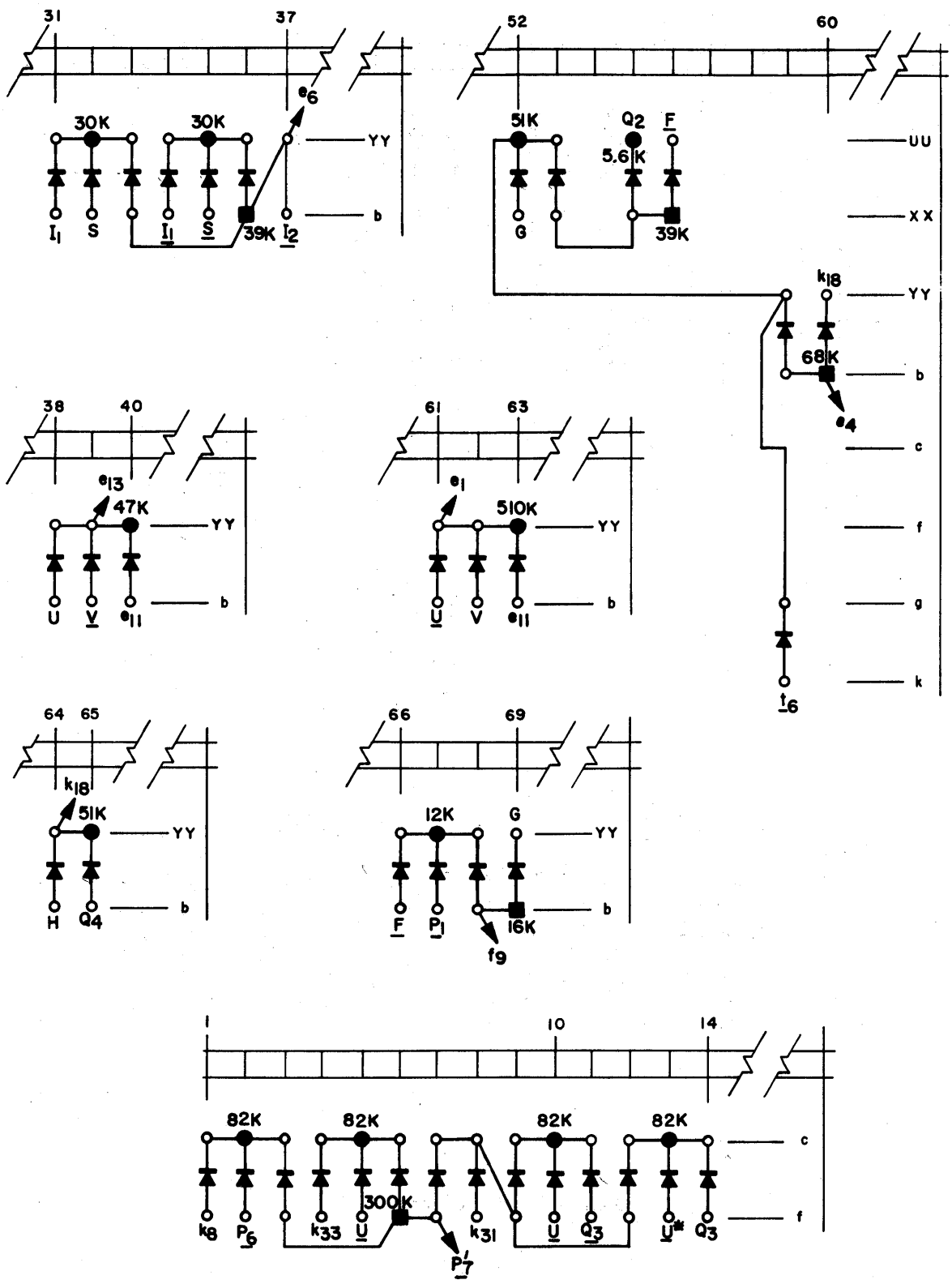


FIGURE 5-6 (18 of 23)

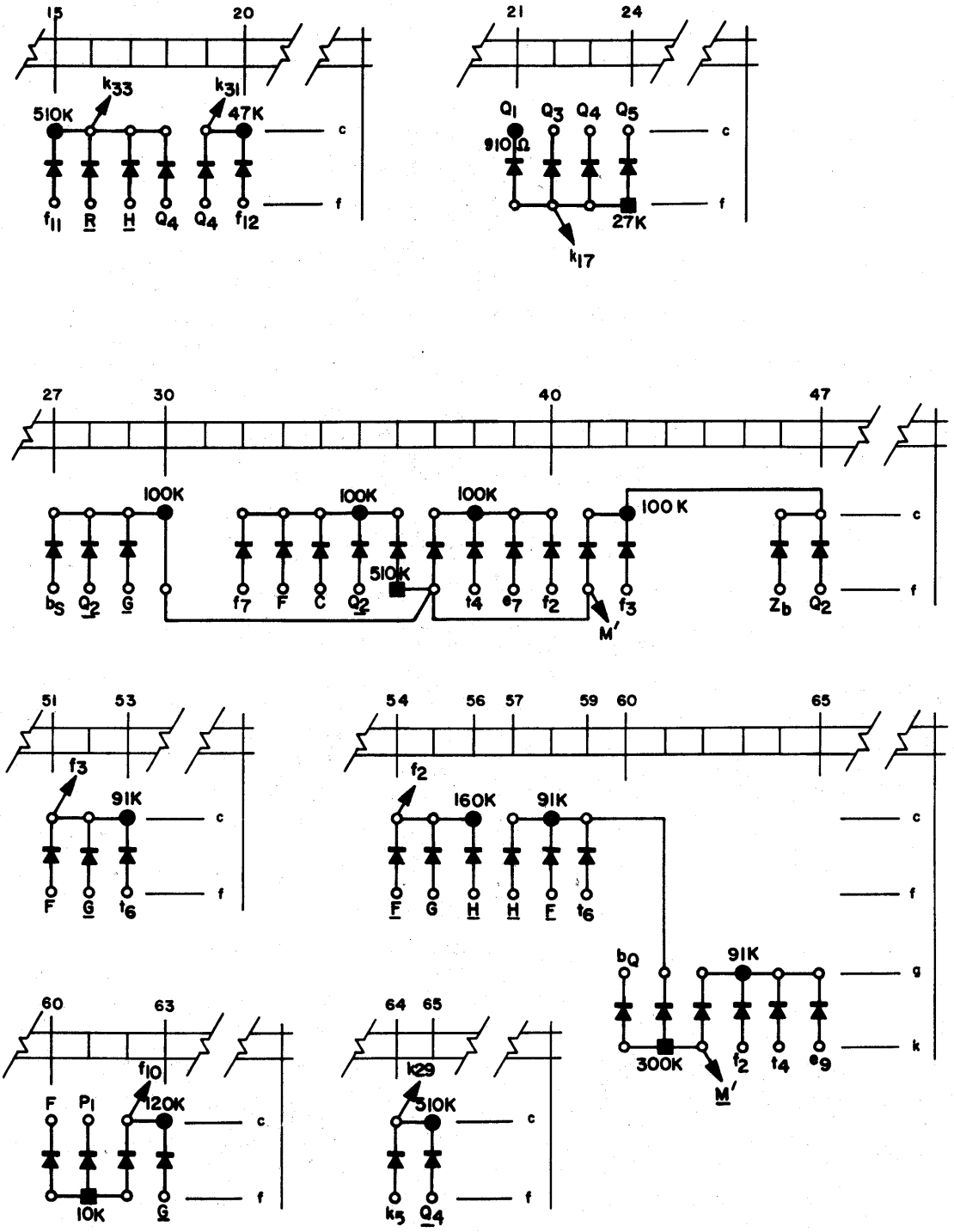


FIGURE 5-6 (19 of 23)

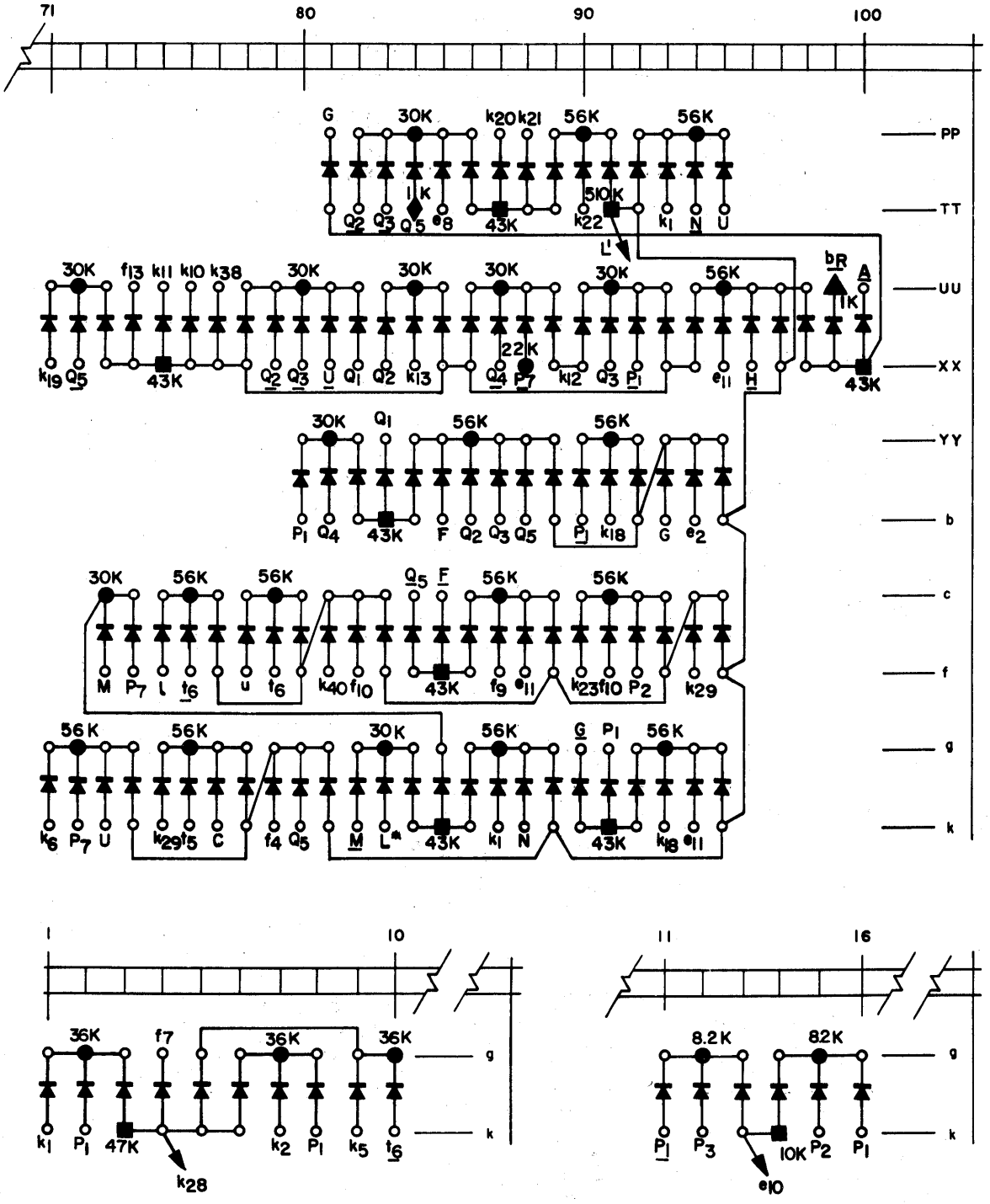


FIGURE 5-6 (20 of 23)

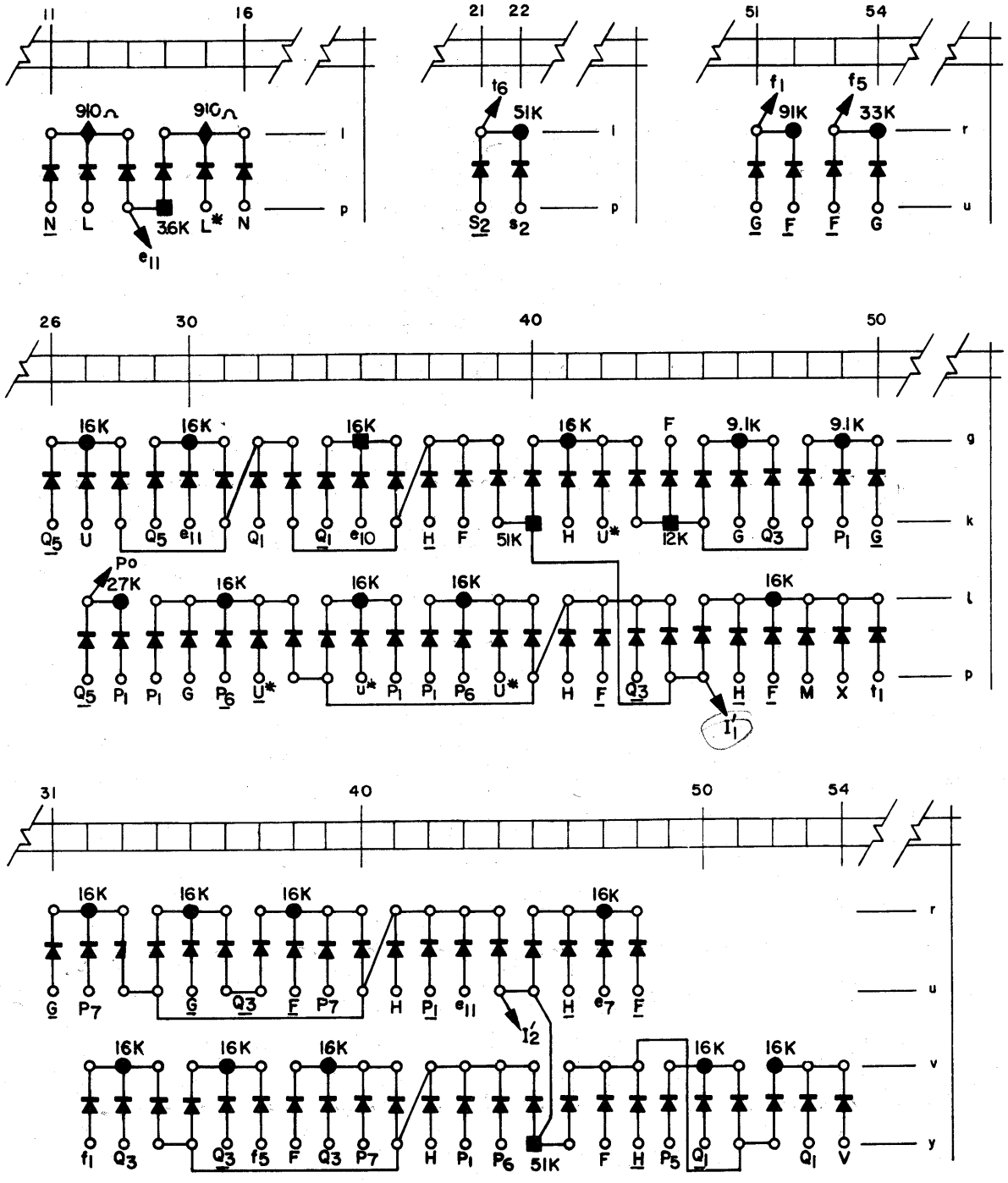
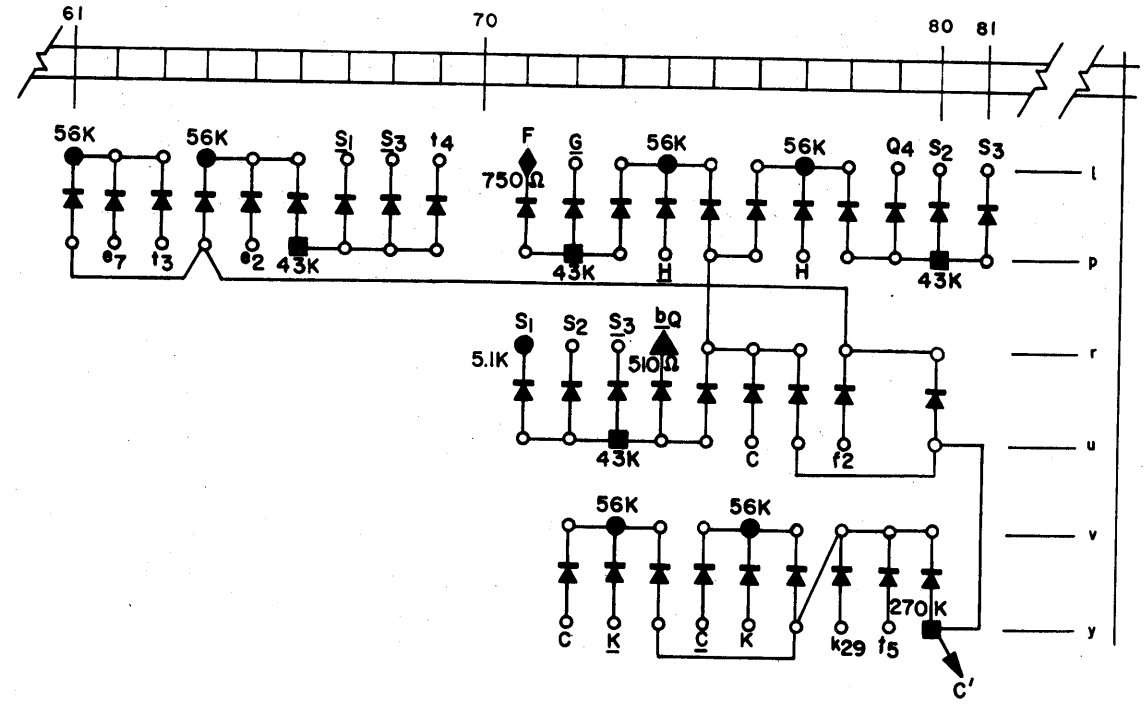


FIGURE 5-6 (21 of 23)



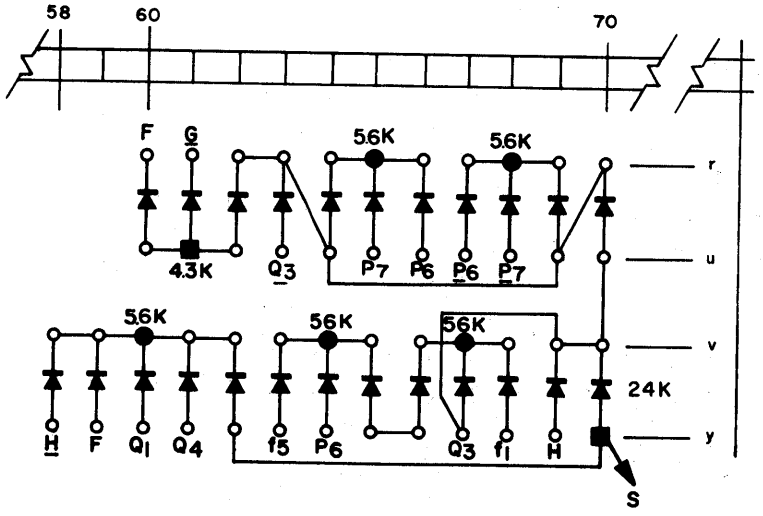


FIGURE 5-6 (22 of 23)

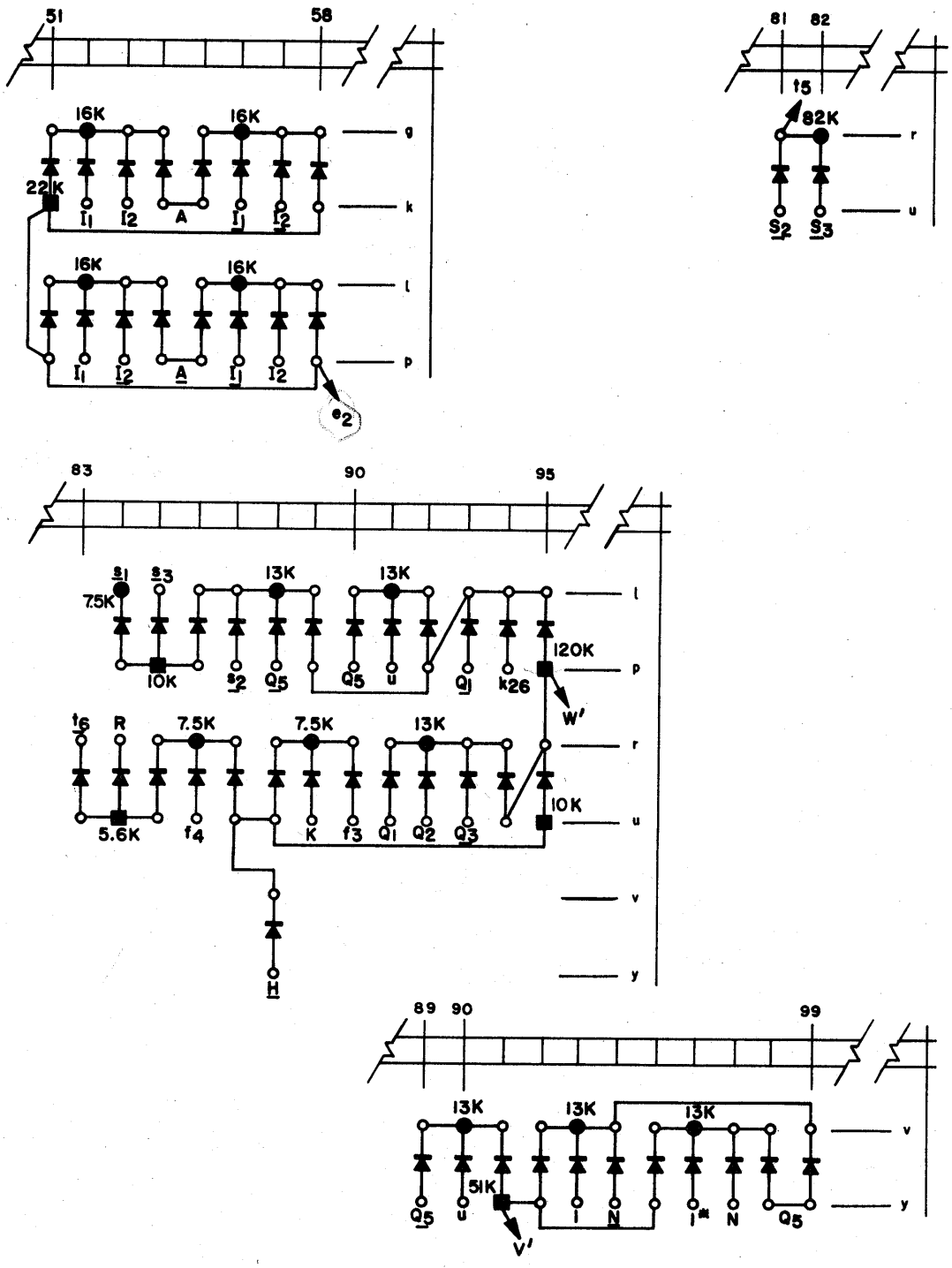


FIGURE 5-6 (23 of 23)

APPENDIX 1

RPC 4010 LOGIC EQUATIONS

APPENDIX I

RPC-4010 LOGIC EQUATIONS

A1.1 DEFINITION OF TERMS

A1.1.1 Some Explanations

The output of a logic gate which is the input to a circulating line, a flip-flop, or an inverter is indicated by a prime ('). For example, the input signal to flip-flop F is called F'.

The Phases are identified as follows:

Phase 1	$\underline{F}\ \underline{G}\ \underline{H}$
Phase 2	$\underline{F}\ G\ \underline{H}$
Phase 3	$F\ \underline{G}\ \underline{H}$
Phase 4	$F\ G\ \underline{H}$
Phase 4	H

The logical equations beginning in Section A1.2 are written in the following format: The top line shows the long form of the equation, with a minimum of alpha signals. The second line shows the form of the equation actually used in the computer with all the alpha signals. The third line contains explanatory notes to aid in the understanding of the equation.

A1.1.2 Timing Tracks

S_1, S_2, S_3

s_1, s_2, s_3

A1.1.3 Input-Output Signals (Synchronism Signals Originating in Input-Output)

Z_B	Character Being Presented for Input
Z_1	Character Not Being Presented for Input
Z_O	Output Device Ready for next character
Z_S	Start Compute
Z_Q	Output Devices and Selected Input Device ready

A1.1.4 Control Panel Signals

$b_2 \longrightarrow b_7$	Branch (SENSE) switches
b_b	Branch Control (BC) switch
b_C	Execute Lower Accumulator switch
b_o	One Operation switch

b_q	Set Input switch or One Operation switch
b_s	Start Compute switch
b_r	Set Input switch

A1.1.5 Flip-flops See Section A1.2, page A1-7

A	Carry
B	Branch Control
F	Phase Control
G	Phase Control
H	Phase Control
K	Sector Search
M	Index Control; Halt Control
N	Lengthened Mode Control
$P_1 \longrightarrow P_7$	Track Selection; Character Holders
$Q_1 \longrightarrow Q_5$	Order Holders
R	Repeat Mode Control

A1.1.6 Recirculating Lines (Registers) See Section A1.3, page A1-19

NOTE: c, 1, 1*, and u are identical to C, L, L*, and U except that they occur 1 bit early.

C	Command Register
c	Early C
L	Lower Accumulator (one word)
1	Early L
L*	Lower Accumulator (eight words)
1*	Early L*
U	Upper Accumulator
u	Early U
X	Index Register

A1.1.7 Main Memory See Section A1.4, page A1-23

W	Time to Record

V'	Information to Record in Memory
V	Information Being Read from Memory

A1.1.8 Input-Output Signals (Synchronism Signals Originating in the Computer)
See Section A1.5, page A1-23

Y_0	One character ready for output
Y_I	Start Input Device
P_0	Interpret Output Character as selection code

A1.1.9 Alpha Signals

An Alpha signal is the output of a logic gate or of an inverter which is used in logic gates.

I_1, I_2	Signals to be added in the Add Logic - Section A1.6, page A1-24
S	Subtraction Control - Section A1.7, page A1-25
$e_1 \longrightarrow e_{13}$	A miscellaneous collection of signals - Section A1.8, page A1-25
$f_1 \longrightarrow f_{14}$	Phase Control Signals - Section A1.9, page A1-26
$k_1 \longrightarrow k_{40}$	Command Signals - Section A1.10, page A1-28
$t_1 \longrightarrow t_8$	Timing Signals - Section A1.11, page A1-33

A1.2 FLIP-FLOPS

$$A' = I_2 (I_1 \underline{S} + \underline{I_1} S) \left[G(Q_2 + \underline{F})\, \underline{t_6} + H\, Q_4\right](\underline{t_6} + H\, Q_3\, \underline{P_1})$$

e_5 — Carry for Adder

e_4 — Ph2 or Ph4 Not (CXE, CME, CMG) or Ph4A

$(\underline{t_6} + K_5\, P_1)$ — Reset MPY No reset Even WP

$$+ \underline{H}\, F\, G\, Q_3\, \underline{Q_2}\, \underline{t_6} \left[(\underline{N}\, L + N\, L^*)\, \underline{U}\, V\, \underline{Q_5} + (\underline{N}\, L + N\, L^*)\, U\, \underline{V}\right]$$

$+ \underline{H}\, f_4\, k_{38}\, \underline{t_6}$ — Ph4

e_1 — CME U V

$\underline{Q_5}$ — CME

e_{13} — CMG U V

$$+ \underline{H}\, F\, G\, \underline{S_2}\, (\underline{S_1} + \underline{S_3})\, \underline{Q_2}\, \underline{Q_3}\, (X\, \underline{C} + \underline{X}\, C)$$

$\underline{H}\, f_4$ — Ph4 OP

t_1 — Adr

$\underline{Q_2}\, \underline{Q_3}\, (X\, \underline{C} + \underline{X}\, C)$ — CXE X C

$$+ \underline{Q_1}\ \underline{Q_2}\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5}\ \underline{M}\ F\ \underline{G}\ t_3 + \underline{F}\ G\ \underline{H}\ t_6\ b_o$$

$$K_{11}\ \ \underline{Q_3}\ \ \underline{Q_5}\ \underline{M}\ F\ \underline{G}\ t_3 + f_2\ \ t_6\ b_o$$

ph3 HLT ONE OP ph2

$$+ (F\ G + H)\ \underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5}$$

k_1

Ph4 and 4a INP

$$\underline{A}' = \underline{I_2}\ (I_1\ S + \underline{I_1}\ \underline{S})\ \left[G\ (Q_2 + \underline{F})\ \underline{t_6} + H\ Q_4\right]$$

e_6 e_4

Carry for Adder Ph2 or Ph4 Not CXE, CME, CMG

$$+ t_6\left[F\ G\ \underline{H}\ (Q_1 + Q_3 + Q_4 + Q_5 + \underline{Q_2}) + H\ \underline{Q_3}\ Q_4\right] + H\ P_1\ (Q_3 + Q_4)\ t_6$$

$$t_6\left[f_4\ \ \underline{H}\ (k_{17} + \underline{Q_2}) + H\ \underline{Q_3}\ Q_4\right] + f_{12}$$

Reset Ph4 or 4 Ph 4a Odd WP Last Bit

$$+ F\ G\ Q_1\ \underline{Q_2}\ Q_5\ V\ \underline{U}\ (\underline{N}\ L + N\ L^*)$$

$$+ f_4\ \ Q_1\ \underline{Q_2}\ Q_5 \qquad e_1$$

Ph4 CMG U V

$$+ \underline{G}\ \underline{H}\ b_s + F\ \underline{G}\ M\ \underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5} + \underline{F}\ G\ \underline{H}\ t_6\ \underline{b_o}$$

$$+ \underline{G}\ \underline{H}\ b_s + k_{39} + F_2\ \ t_6\ \underline{b_o}$$

Ph1 or 3 INP Ph3 Not First Cycle Ph2

$$\underline{B}' = F\ G\ t_6\left\{(\underline{Q_1}\ \ \underline{Q_2}\ \underline{Q_4})\underline{Q_3}\ \left[\underline{Q_5}\ (P_1\ \underline{Z_q} + P_2\ b_2\right.\right.$$

$$f_{11}\ \ \left\{(k_{11})\ \ \underline{Q_3}\ \left[\underline{Q_5}\ (P_1\ \underline{Z_q}\ \ P_2\ b_2\right.\right.$$

Ph4 SNS

$$+ P_3\ b_3 + P_4\ b_4 + P_5\ b_5 + P_6\ b_6 + P_7\ b_7) + Q_5\ \underline{A}\Big]$$

$$+ P_3\ b_3 + P_4\ b_4 + P_5\ b_5 + P_6\ b_6 + P_7\ b_7) + Q_5\ \underline{A}\Big]$$

Switch Sensing CXE

$$+ Q_1\ \underline{Q}_2\ Q_3\ \underline{Q}_4 \left[\underline{A}\ (\underline{N}\ \underline{L} + N\ \underline{L}^* + U\ V + \underline{U}\ \underline{V})\right.$$

$$+ Q_1\ \ k_{38}\ \ \underline{Q}_4 \left[\underline{A}\ (\quad e_{12} \quad + U\ V + \underline{U}\ \underline{V})\right.$$

CME CMG No sign mask Signs Same

$$\left. + Q_5\ U\ \underline{V}\ (\underline{N}\ L + N\ L^*)\right] + Q_1\ Q_2\ Q_3 \left[\underline{A}\ I\ (I_1\ \underline{S} + \underline{I}_1 S)\right.$$

$$\left. + Q_5 \quad e_{13} \quad\right] + \quad k_{36} \quad \left[\underline{A} \quad e_5\right.$$

CMG U Neg., V Pos. ADU, ADL, SBU, SBL, Overflow

$$\left. + A\ \underline{I}_2\ (I_1\ S + \underline{I}_1\ \underline{S})\right]\Big] + \underline{F}\ \underline{G}\ H\ P_1\ t_6\ Q_4\ \underline{Q}_3\ (U\ P_7 + \underline{U}\ \underline{P}_7)$$

$$\left. + A \quad e_6 \quad\right]\Big] + f_1 \quad k_{31}\ \ \underline{Q}_3\ (U\ P_7 + \underline{U}\ \underline{P}\ )$$

WP3 Ph4a DIV DVU Overflow

$$+ \underline{G}\ P_7\ \underline{K}\ \underline{Q}_5 \Big[H\ Q_3\ \underline{Q}_4\ t_6 \left[\underline{P}_3\ P_4 + P_3\ \underline{P}_4 + P_3\ P_4\ \underline{P}_5\ (\underline{N}\ \underline{L} + N\ \underline{L}^*)\right]\Big]$$

$$+ \underline{G}\ P_7\ \underline{K}\ Q_5 \quad\quad k_3$$

SLT Overflow

$$\underline{B}' = Z_i\ F\ \underline{G}\ t_6\ \underline{A}\ \left[Q_1\ \underline{Q}_2\ Q_3\ (\underline{Q}_4 + Q_5)\ K + \underline{Q}_1\ \underline{Q}_2\ \underline{Q}_3\ \underline{Q}_4\right] + b_b$$

$$= Z_i\ f_3\ \underline{A}\ \left[Q_1\ \ k_{38}\ (\underline{Q}_4 + Q_5)\ K + k_{11}\ \ \underline{Q}_3\right] + b_b$$

Last WP Ph3 TBC CME CMG CXE, SNS Reset Sw

$$F' = \underline{F}\ t_6 \left[G\ \ \underline{H} \quad + \underline{G}\ H\ P_1\ t_6 \quad (Q_3 + Q_4)\right.$$

$$\underline{F}\ t_6 \left[G\ \ \underline{H} \quad + \underline{G} \quad f_{12} \quad k_{34}\right.$$

Ph2 to Ph3 WP3 Ph4A Not INP

$$+ \underline{G}\ Q_5 \Big[H\ Q_3\ \underline{Q}_4\ t_6 \left[P_3\ \ \underline{P}_4 + \underline{P}_3\ P_4 + P_3\ P_4\ \underline{P}_5\ (\underline{N}\ \underline{L} + N\ \underline{L}^*)\right]\Big]$$

$$+ \underline{G}\ Q_5 \quad\quad k_3$$

End SLC

$$+ \underline{H}\ Z_b\ \underline{Q}_1\ Q_2\ \underline{Q}_3\ \underline{Q}_4\ \underline{Q}_5\Big) + b_q$$

$$+ \underline{H}\ Z_b\ k_6\ Q_5\Big) + b_q$$

Ph1 to Ph3 Inp SET INP Sw

$$\underline{F}' = F\ t_6 \Big[G\ (H + \underline{R} + \underline{Q}_1\ \underline{Q}_2\ Q_3\ Q_4\ \underline{Q}_5)$$

$$F\ t_6 \Big[G\ (H + e_3\ )$$

End Ph4A End Ph4

$$+ K\ Z_i\ \underline{A}\ Q_1\ \underline{Q}_2\ Q_3\ Q_4\ (\underline{Q}_5\ U + Q_5\ B)\Big]$$

$$+ K\ Z_i\ \underline{A}\ Q_1\ \underline{Q}_2\ k_{15}\ (\underline{Q}_5\ U + Q_5\ B)\Big]$$

Ph3 to Ph2 Suc TMI TBC

$$G' = \underline{G}\ t_6\ (Z_i + H) \begin{cases} K\ (\underline{A}\ \underline{H} + H\ F + H\ P_1\ t_6) \\ K\ (\underline{A}\ \underline{H} + H\ F + f_{12}\ ) \end{cases}$$

Ph1 to Ph2 Ph3 to Ph4 End Ph4A, Not INP

$$+ Q_5\ H\ Q_3\ \underline{Q}_4\ t_6 \Big[P_3\ \underline{P}_4 + \underline{P}_3\ P_4 + P_3\ P_4\ \underline{P}_5\ (\underline{N}\ \underline{L} + N\ \underline{L}^*)\Big]$$

$$+ Q_5\ k_3$$

End Ph4A SLC

$$+ \underline{A}\ F\ \underline{H}\ \Big[\underline{Q}_1\ Q_2\ \underline{Q}_5\ \underline{Q}_3\ \underline{Q}_4\ (\underline{N} + t_8) + \underline{Q}_1\ \underline{Q}_2\ \underline{Q}_4\ \underline{Q}_3$$

$$+ \underline{A}\ F\ \underline{H}\ \Big[k_{20}\ k_{16} + k_{11}\ \underline{Q}_3$$

Ph3 to Ph4 INP SNS CXE

$$+ \underline{Q}_1\ Q_3\ \underline{Q}_4\ Q_2 + \underline{Q}_1\ Q_3\ Q_4\ Q_5\ \underline{Q}_2\Big]$$

$$+ k_{13}\ Q_2 + k_{14}\ \underline{Q}_2\Big]$$

SRT SLT SLC LDX

$$+ F \underline{A}\, \underline{Q_2}\ (Z_o\ Q_1\ \underline{Q_3}\ \underline{Q_4} + Q_1\ Q_3\ Q_4\ \underline{Q_5}\ \underline{U}$$

$$+ F \underline{A}\, \underline{Q_2}\ (Z_o\ k_{10} + k_{15}\ Q_5\ \underline{U}$$

Ph3 to Ph4 PRD PRU Unsuc TMI

$$+ Q_1\ Q_3\ Q_4\ Q_5\ \underline{B}\ \Big|$$

$$+ k_{15}\ Q_5\ \underline{B}\ \Big|$$

Unsuc TBC

$$\underline{G}' = G\ t_6 \Big[\underline{H}\ (\underline{F} + \underline{R} + \underline{Q_1}\ \underline{Q_2}\ Q_3\ Q_4\ \underline{Q_5}) + \underline{F}\ P_1\Big]$$

$$G\ t_6 \Big[\underline{H}\ (\underline{F} + e_3) + \underline{F}\ P_1\Big]$$

Ph2 to Ph3 End Ph4 WP67 MPY DIV DVU

$$H' = F\ G\ \underline{H}\ t_6\ (\underline{R} + \underline{Q_1}\ \underline{Q_2}\ Q_3\ Q_4\ \underline{Q_5})\ (\underline{Q_1}\ \underline{Q_4}\ Q_3\ Q_2$$

$$f_{14} \qquad (\ k_{13}\ Q_2$$

End of Ph4 SLC SRT SLT

$$+ \underline{Q_1}\ Q_2\ \underline{Q_5} + \underline{Q_1}\ Q_2\ \underline{Q_3}\ Q_4)$$

$$+ k_{20} + k_{21}\ )$$

INP MPY DVU DIV

$$\underline{H}' = H\ t_6 \Big[\underline{F}\ G\ P_1 + \underline{Q_3}\ \underline{Q_4}\ (\underline{N} + t_8) + \underline{F}\ \underline{G}\ \underline{P_1}\ K\ Q_3\ \underline{Q_4}\ \underline{Q_5}\Big]$$

$$H\ t_6 \Big[f_5\ P_1 + k_{16} + f_1\ \underline{P_1}\ K\ k_{29}\ \underline{Q_5}\Big]$$

MPY DIV DVU SRT SLT SLC INP WP2 SRT 0 SLT 0

$$K' = t_6 \Big[\underline{F} + G + (Q_3 + Q_4) + (Z_o + \underline{Q_1} + Q_2)\ (Q_1 + \underline{Q_2} + Q_5)\Big]$$

$$t_6 \Big[\underline{F} + G + k_{34} + (Z_o + \underline{Q_1} + Q_2)\ (\ k_{19} + Q_5)\Big]$$

Ph1,2,4 Ph4A DIV DVU SRT MPY SLC SLT Not PRD, PRU unless Z_o Not INP

$$\underline{K}' = \underline{G}\,\underline{S_3}\left[\underline{H}\ (\underline{F}\,S_2 + F\,\underline{S_2}) + H\,Q_4\,\underline{S_2}\right](S_1\,\underline{C} + \underline{S_1}\,C)$$

$$\underline{G}\,\underline{S_3}\left[\underline{H} \qquad f_6 \qquad + \quad k_{18}\,\underline{S_2}\right](S_1\,\underline{C} + \underline{S_1}\,C)$$

Ph1 NI Ph3 OP Ph4A OP $C \neq S_1$

$$+ H\,Q_3\,\underline{Q_4}\left[(\underline{Q_5} + P_1 + F)\,(Q_5\,\underline{C} + \underline{Q_5}\,C)\,\underline{S_2}\,\underline{S_3} + Q_5\,S_2\,\underline{P_1}\right]$$

$$+ \quad k_{29} \quad \left[(\underline{Q_5} + P_1 + F)\,(Q_5\,\underline{C} + \underline{Q_5}\,C) \qquad t_5 + Q_5\,S_2\,\underline{P_1}\right]$$

Ph4A SRT SLT Not WP2 SLC SRT SLT OP Sector SLC, No Search NI WP2

$$+ F\,G\,\underline{H}\,\underline{S_1}\ S_2\,S_3\,X$$

$$+ \quad f_4\underline{H} \qquad t_2 \qquad X$$

Ph4 Repeated NI trk

$$\underline{M}' = F\,\underline{G}\,t_6\,(Z_b\ Q_2)$$

$$f_3 \qquad (Z_b\ Q_2)$$

Ph3 INP if Z_b

$$+ \underline{G}\,\underline{H}\,\underline{S_1}\,S_3\ (\underline{M} + \underline{Q_2})\ (\underline{F}\,S_2 + F\ \underline{S_2})\ F\ C\ \underline{Q_2}$$

$$+ \qquad\qquad f_7 \qquad\qquad F\ C\ \underline{Q_2}$$

Ph3 OP TRK Not 0, SNS

$$+ \underline{F}\,G\,\underline{H}\,S_3\,\underline{s_3}\,s_2\left|\underline{b_c}\ V + \left[b_c\ (\underline{N}\ L + N\ L^*)\right]\right| + b_s\,\underline{Q_2}\,\underline{G}$$

$$+ \quad f_2 \qquad t_4 \qquad\qquad e_7 \qquad\qquad b_s\,\underline{Q_2}\,\underline{G}$$

Ph2 Bit 31 Index Bit Ph1 or 3, Not INP

$$\underline{M}' = \underline{F}\,\underline{H}\,t_6 + \underline{F}\,G\,\underline{H}\ S_3\,\underline{s_3}\,s_2\left[\underline{b_c}\,\underline{V} + b_c\ (\underline{N}\ \underline{L} + N\ \underline{L^*})\right] + b_q$$

$$\underline{F}\,\underline{H}\,t_6 + \quad f_2 \quad t_4\left[\qquad e_9 \qquad\qquad\right] + b_q$$

Ph1 or 2 Ph2 Bit 31 No Index Bit Set INP Sw

$N' = \underline{N}\ F\ G\ t_6\ \underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ Q_5\ P_3$

$\underline{N}\ f_{11}\ k_{30}\ P_3$

Ph4 EXC

$\underline{N}' = N\ F\ G\ t_6\ \underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ Q_5\ P_2 + b_q\ t_8$

$N\ f_{11}\ k_{30}\ P_2 + b_q\ t_8$

Ph4 EXC Set INP Sw

$P_1' = f_7\ C + H\ \underline{P_1}\ t_6\ (Q_3 + Q_4)$

$f_7\ C + H\ \underline{P_1}\ t_6\ k_{34}$

OP or NI Trk Ph4A Even WP Not INP

$\underline{P_1}' = f_7\ \underline{C} + F\ G\ \underline{H}\ t_6\ (\underline{R} + \underline{Q_1}\ \underline{Q_2}\ Q_3\ Q_4\ \underline{Q_5})\ (Q_3 + Q_4)$

$f_7\ \underline{C}\ f_{14}\ k_{34}$

OP or NI Trk PH4 last WP LDC Not INP

$+ H\ P_1\ Q_4\ t_6$

$+\ k_{31}$

Ph4A Odd WP MPY, DVU, DIV

$P_2' = f_7\ P_1 + k_2\ P_1\ U + k_1\ (\underline{N}\ L + N\ L^*)$

$f_7\ P_1 + k_2\ P_1\ U + k_1\ e_{11}$

OP or NI Trk PRU Ph3 Order INP Ph4 or 4A

$+ F\ \underline{G}\ M\ k_6\ \underline{Q_5}\ B_6 + \underline{t_6}\ (H\ Q_3 + k_4)\ (\underline{N}\ L + N\ L^*)$

$+\ k_{39}\ B_6 + \underline{t_6}\ k_{32}\ e_{11}$

Input Set SLT SLC MPT Ph4

$$\underline{P}_2' = f_7\ \underline{P}_1 + k_2\ P_1\ \underline{U} + k_1\ (\underline{N}\ \underline{L} + N\ \underline{L}^*)$$

$$f_7\ \underline{P}_1 + k_2\ P_1\ \underline{U} + k_1 \qquad e_{12}$$

OP or NI Trk PRU Ph3 Order INP Ph4 or 4A

$$+ (H\ Q_3 + k_4)\left[(\underline{N}\ \underline{L} + N\ \underline{L}^*) + t_6\right]$$

$$+ \quad k_{32} \cdot \left[(\quad e_{12} \quad) + t_6\right]$$

SLT SLC MPT Ph4

$$P_3' = (f_7 + k_1)\ P_2 + k_2\ P_1\ U^* + F\ \underline{G}\ M\ k_6\ \underline{Q}_5\ B_5$$

$$k_{27}\ P_2 + k_2\ P_1\ U^* + \qquad k_{39} \qquad B_5$$

OP or NI Trk or INP PRU Ph3 Input Set

$$+ H\ Q_3\left[t_6\ \underline{P}_1\ (\underline{N}\ L + N\ L^*) + \underline{t}_6\ \underline{P}_1\ u + t_6\ P_1\ P_2 + \underline{t}_6\ P_1\ U\right]$$

$$+ \quad k_5\left[t_6\ \underline{P}_1 \qquad e_{11} \qquad + \underline{t}_6\ \underline{P}_1\ u + t_6\ P_1\ P_2 + \underline{t}_6\ P_1\ U\right]$$

SLT SLC WP2 WP3 to End

$$+ k_4\ U\ \underline{t}_6$$

$$+ k_4\ U\ \underline{t}_6$$

Ph4 MPT

$$\underline{P}_3' = (f_7 + k_1)\ \underline{P}_2 + k_2\ P_1\ \underline{U}^* + FG\ (\underline{U} + t_6)$$

$$k_{27} \qquad \underline{P}_2 + k_2\ P_1\ \underline{U}^* + k_4\ (\underline{U} + t_6)$$

OP or NI Trk or INP PRU Ph3 MPT Ph4

$$+ H\ Q_3\left[t_6\ \underline{P}_1\ (\underline{N}\ \underline{L} + N\ \underline{L}^*) + \underline{t}_6\ \underline{P}_1\ \underline{u} + t_6\ P_1\ \underline{P}_2 + \underline{t}_6\ P_1\ \underline{U}\right]$$

$$+ \quad k_5\left[t_6\ \underline{P}_1 \qquad e_{12} \quad + \underline{t}_6\ \underline{P}_1\ \underline{u} + t_6\ P_1\ \underline{P}_2 + \underline{t}_6\ P_1\ \underline{U}\right]$$

SLT SLC WP2 WP3 to End

$$P_4' = (f_7 + k_1 P_1 + k_2 P_1 + \underline{t}_6 H Q_3) P_3 + k_2 \underline{P}_1 U$$

$$k_{28} \qquad P_3 + k_2 \underline{P}_1 U$$

Trk INP PRU Ph3 SLT SLC PRU Ph3, 4-Bit

$$+ F \underline{G} M k_6 \underline{Q}_5 B_4 + k_4 (\underline{P}_1 P_3 + P_1 P_2) \underline{t}_6$$

$$+ k_{39} B_4 + k_4 e_{10} \underline{t}_6$$

Input Set MPT Ph4

$$+ k_1 \underline{P}_1 (\underline{N} L + N L^*)$$

$$+ k_1 \underline{P}_1 e_{11}$$

INP 4-Bit

$$\underline{P}_4' = (f_7 + k_1 P_1 + k_2 P_1 + \underline{t}_6 H Q_3) \underline{P}_3 + H Q_3 t_6$$

$$k_{28} \qquad \underline{P}_3 + k_5 t_6$$

Trk INP PRU Ph3 SLT SLC SLT SLC

$$+ k_4 (\underline{P}_1 \underline{P}_3 + P_1 \underline{P}_2 + t_6) + k_2 \underline{P}_1 \underline{U} + k_1 \underline{P}_1 (\underline{N} \underline{L} + N \underline{L}^*)$$

$$+ k_4 (\underline{P}_1 \underline{P}_3 + P_1 \underline{P}_2 + t_6) + k_2 \underline{P}_1 \underline{U} + k_1 \underline{P}_1 e_{12}$$

MPT Ph4 PRU Ph3 INP

$$P_5' = \left[f_7 + k_1 + k_2 + (H Q_3 + k_4) \underline{t}_6\right] P_4$$

$$\left[k_8 + k_{32} \underline{t}_6\right] P_4$$

Trk INP PRU Ph3 SLT SLC MPT Ph4

$$+ F \underline{G} M k_6 \underline{Q}_5 B_3$$

$$+ k_{39} B_3$$

Input Set

$$\underline{P_5}' = (f_7 + k_1 + k_2 + k_4)\ \underline{P_4} + (H\ Q_3 + k_4)\ t_6$$

$$(\quad k_8 + k_4)\ \underline{P_4} + \quad k_{32}\quad t_6$$

Trk INP PRU Ph3 MPT Ph4 SLT SLC MPT Ph4

$$P_6' = (f_7 + k_1 + k_2)\ P_5 + F\ \underline{G}\ M\ k_6\ \underline{Q_5}\ B_2 + F\ G\ \underline{H}\ t_6\ Q_4\ \underline{R}\ V$$

$$k_8 \quad P_5 + \quad k_{39}\quad B_2 + \quad k_{33}\quad V$$

Trk INP PRU Input Set DIV DVU MPY

$$\underline{P_6}' = (f_7 + k_1 + k_2)\ \underline{P_5} + F\ G\ \underline{H}\ t_6\ Q_4\ \underline{R}\ \underline{V}$$

$$k_8 \quad \underline{P_5} + \quad k_{33}\quad \underline{V}$$

Trk INP PRU Last WP Ph4 DIV DVU MPY

$$P_7' = (f_7 + k_1 + k_2)\ P_6 + F\ \underline{G}\ M\ k_6\ \underline{Q_5}\ B_1$$

$$k_8 \quad P_6 + \quad k_{39}\quad B_1$$

Trk INP PRU Input Set

$$+ F\ G\ \underline{H}\ t_6\ Q_4\ \underline{R}\ U + H\ P_1\ t_6\ Q_4\ (Q_3\ U^* + \underline{Q_3}\ U)$$

$$+ \quad k_{33}\quad U + \quad k_{31}\quad (Q_3\ U^* + \underline{Q_3}\ U)$$

Last WP Ph4 DIV DVU MPY Ph4A Odd WP MPY DIV DVU

$$\underline{P_7}' = (f_7 + k_1 + k_2)\ \underline{P_6} + F\ G\ \underline{H}\ t_6\ Q_4\ \underline{R}\ \underline{U}$$

$$k_8 \quad \underline{P_6} + \quad k_{33}\quad \underline{U}$$

Trk INP PRU Last WP Ph4 DIV DVU MPY

$$+ H\ P_1\ t_6\ Q_4\ (Q_3\ \underline{U}^* + \underline{Q_3}\ \underline{U})$$

$$+ \quad k_{31}\quad (Q_3\ \underline{U}^* + \underline{Q_3}\ \underline{U})$$

Ph4A Odd WP MPY DIV DVU

$$Q_1' = \underline{F}\ G\ \underline{H}\ S_1\ S_3\ s_3 \left[\underline{b_c}\ V + b_c\ (\underline{N}\ L + N\ L^*) \right]$$

f_8 e_7

Ph2 Order Mem or L on Ex L sw

$$Q_1' = \underline{F}\ G\ \underline{H}\ S_1\ S_3\ s_3 \left[\underline{b_c}\ \underline{V} + b_c\ (\underline{N}\ \underline{L} + N\ \underline{L^*}) \right] + b_q$$

f_8 $\left[b_c\ \underline{V} + b_c\ e_{12} \right] + b_q$

Ph2 Order Mem or L on Ex L Sw Set Mode Input

$$Q_2' = \underline{F}\ G\ \underline{H}\ S_1\ S_3\ s_3\ Q_1 + b_q$$

f_8 $Q_1 + b_q$

Ph2 Order Set Input Mode

$$\underline{Q_2}' = \underline{F}\ G\ \underline{H}\ S_1\ s_3\ \underline{Q_1}$$

f_8 $\underline{Q_1}$

Ph2 Order

$$Q_3' = \underline{F}\ G\ \underline{H}\ S_1\ S_3\ s_3\ Q_2$$

f_8 Q_2

Ph2 Order

$$\underline{Q_3}' = \underline{F}\ G\ \underline{H}\ S_1\ S_3\ s_3\ \underline{Q_2} + b_q$$

f_8 $\underline{Q_2} + b_q$

Ph2 Order Set Input Mode

Q_4' = $\underline{F}$ G $\underline{H}$ S_1 S_3 s_3 Q_3

f_8 Q_3

Ph2 Order

$\underline{Q}_4'$ = $\underline{F}$ G $\underline{H}$ S_1 S_3 s_3 $\underline{Q}_3$ + b_q

f_8 $\underline{Q}_3$ + b_q

Ph2 Order Set Input Mode

Q_5' = $\underline{F}$ G $\underline{H}$ S_1 S_3 s_3 Q_4

f_8 Q_4

Ph2 Order

$\underline{Q}_5'$ = $\underline{F}$ G $\underline{H}$ S_1 S_3 s_3 $\underline{Q}_4$ + b_q

f_8 $\underline{Q}_4$ + b_q

Ph2 Order Set Input Mode

R' = F G t_6 $\underline{Q}_1$ $\underline{Q}_2$ Q_3 Q_4 $\underline{Q}_5$

f_{11} k_{25}

Ph4 LDC

$\underline{R}'$ = F G $\underline{S}_2$ ($\underline{S}_1$ + $\underline{S}_3$) K + b_q

f_4 t_1 K + b_q

Ph4 OP Adr Last WP

A1.3 REGISTERS

$$C' = \underline{F}\ G\ \underline{H} \left| e_2 \ (\underline{S}_1 + \underline{S}_3 + t_4) + \left[\underline{b}_c\ V + b_c\ (\underline{N}\ L + N\ L^*)\right] S_1\ S_3\ s_3 \right|$$

$$f_2 \left| e_2 \ (\underline{S}_1 + \underline{S}_3 + t_4) + e_7 \ t_3 \right|$$

Ph2 — Adder Not Order — "Mem" or "L" on Ex L Sw — Order

$$+ H\ Q_3\ \underline{Q}_4\ \underline{S}_2\ \underline{S}_3\ (C\ \underline{K} + \underline{C}\ K)$$

$$+ k_{29}\ t_5\ (C\ \underline{K} + \underline{C}\ K)$$

SLT SLC SRT OP Sector — Shift Count

$$+ C\ (S_1 + S_2 + \underline{S}_3 + \underline{b}_q) \left[\underline{H}\ (F + \underline{G}) + H\ (Q_4 + S_3 + S_2)\right]$$

$$+ C\ (S_1 + S_2 + \underline{S}_3 + \underline{b}_q) \left[\underline{H}\ (F + \underline{G}) + H\ (Q_4 + S_3 + S_2)\right]$$

Not OP Trk if b_q — Ph1, 3, 4 MPY DIV INP SRT SLT SLC DVU Not OP Sector

$$L' = (\underline{N}\ L + N\ L^*)\ (\underline{b}_r + G + \underline{A})\ \underline{H} \left[\underline{F} + \underline{G} + \underline{Q}_1\ \underline{Q}_2\ \underline{Q}_4 + Q_2\ \underline{Q}_1\ Q_3\ \underline{Q}_4\right.$$

$$e_{11}\ (\underline{b}_r + G + \underline{A})\ \underline{H} \left[f_{13} + k_{11} + Q_2\ k_{13}\right.$$

Clears L on Set Input if Blocked State — Ph1, 2, 3 SNS HLT SRT SLT SAU CXE SLC MST

$$+ (Q_1 + \underline{Q}_2)\ \underline{Q}_5 + \underline{Q}_1\ Q_2\ Q_5\ Q_3\ \underline{P}_1 + \underline{Q}_1\ Q_2\ Q_5\ \underline{Q}_4\ \underline{P}_7$$

$$+ k_{19}\ \underline{Q}_5 + k_{12}\ Q_3\ \underline{P}_1 + k_{12}\ \underline{Q}_4\ \underline{P}_7$$

RAU EXT CLU ADU SBU — MPT < 64 — EXC, Not U⟶L

$$+ \underline{Q}_2\ Q_3 + Q_1\ \underline{Q}_3\ \underline{Q}_4 + Q_1\ \underline{Q}_2\ \underline{Q}_3\ \underline{U}\left.\right]$$

$$+ k_{38} + k_{10} + Q_1\ \underline{Q}_2\ \underline{Q}_3\ \underline{U}\left.\right]$$

CMG TMI TBC LDC LDX CME — PRU PRD STU STL — MML

$$+ F\ G\ \underline{H}\ V\ Q_4 \left[\underline{Q_2}\ \underline{Q_3}\ Q_5\ (\underline{Q_1} + U) + \underline{Q_1}\ Q_2\ \underline{Q_5} + \underline{Q_1}\ Q_2\ \underline{Q_3}\right]$$

$$+ \quad k_{22} \quad \left[\underline{Q_2}\ \underline{Q_3}\ Q_5 \quad e_8 \quad + \quad k_{20} \quad + \quad k_{21}\right]$$

Ph4 RAL MML MPY DIV DVU

$$+ k_1\ \underline{N}\ U + k_1\ N\ (\underline{M}\ L^* + M\ P_7) + (\underline{G} + P_1)\ H\ Q_4\ (\underline{N}\ L + N\ L^*)$$

$$+ k_1\ \underline{N}\ U + k_1\ N\ (\underline{M}\ L^* + M\ P_7) + (\underline{G} + P_1) \quad k_{18} \quad e_{11}$$

INP Non Length INP Lengthen Ph4A Not WP66 MPY DIV DVU

$$+ F\ G\ Q_5\ (\underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ P_7\ U + H\ Q_3\ \underline{Q_4}\ \underline{S_2}\ \underline{S_3}\ C)$$

$$+ f_4\ Q_5\ (\quad k_6 \quad P_7\ U + \quad k_{29} \quad t_5 \quad C)$$

EXC Ph4 SLC Term OP Sector

$$+ G\ e_2 \left[\underline{P_1}\ H\ Q_4 + F\ Q_2\ Q_3\ Q_5\ (Q_1 + P_1\ Q_4)\right]$$

$$+ G\ e_2 \left[\underline{P_1} \quad k_{18} + F\ Q_2\ Q_3\ Q_5\ (Q_1 + P_1\ Q_4)\right]$$

Adder MPY DIV DVU Ph4A Ph4 ADL SBL MPT $\geq$ 64

$$+ H\ Q_3\ \underline{Q_4} \left[(Q_5+P_7)\underline{G}\ (F + P_1) \quad P_2\right.$$

$$+ \quad k_{29} \quad \left[k_{23}\ f_{10} \quad P_2\right.$$

SLT SLC

$$+ (\underline{Q_5} + \underline{F})\ (\underline{F}\ \underline{P_1} + G)\ (\underline{N}\ L + N\ L^*) + \underline{Q_5}\ \underline{P_7}(F + P_1)\underline{G}\ (1\ \underline{t_6} + u\ t_6)\Big]$$

$$(\underline{Q_5} + \underline{F}) \quad f_9 \quad e_{11} \quad + \quad k_{40} \quad f_{10}\ (1\ \underline{t_6} + u\ t_6)\Big]$$

WP2 and Term SRT

$$U' = U\ \underline{H} \left[\underline{F} + \underline{G} + \underline{Q_1}\ \underline{Q_2}\ \underline{Q_4} + \underline{Q_1}\ Q_3\ \underline{Q_4}\right.$$

$$U\ \underline{H} \left[\quad f_{13} \quad k_{11} \quad k_{13}\right.$$

Ph 1,2,3 SNS HLT SAU CXE SRT SLT SLC MST

$$+ (Q_1 + \underline{Q_2})\ Q_5 + Q_3\ Q_5\ P_1 + \underline{Q_4}\ Q_5\ \underline{P_4}\ \underline{P_6}$$

$$+ \quad k_{19} \quad Q_5 + Q_3\ Q_5\ P_1 + \underline{Q_4}\ Q_5\ \underline{P_4}\ \underline{P_6}$$

RAL COL CLL ADL SBL — MPT $\geq$ 64 — EXC, Not L $\longrightarrow$ U; Not X $\longrightarrow$ U

$$+ \underline{Q_2}\ Q_3 \quad + \quad Q_1\ \underline{Q_3}\ \underline{Q_4} + \underline{Q_1}\ Q_3\ \underline{Q_5}\ (\underline{t_6} + R)\Big]$$

$$k_{38} \quad + \quad k_{10} + \underline{Q_1}\ Q_3\ \underline{Q_5}\ (\underline{t_6} + R)\Big]$$

CMG TMI TBC LDC LDX CME — PRU PRD STU STL — MPY

$$+ F\ G\ \underline{H}\ V\ Q_4\ \underline{Q_2}\ \underline{Q_3}\ \underline{Q_5}\ (\underline{Q_1} + U) + k_1\ \underline{N}\ (\underline{M}\ L + M\ P_7)$$

$$+ \quad k_{22} \quad \underline{Q_2}\ \underline{Q_3}\ \underline{Q_5} \quad e_8 \quad + k_1\ \underline{N}\ (\underline{M}\ L + M\ P_7)$$

RAU EXT — INP Non-Lengthen Ph4 or 4A

$$+ k_1\ N\ U + F\ G\ \underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ Q_5\ (P_6\ \underline{N}\ L + N\ L^* + P_4\ X)$$

$$+ k_1\ N\ U + f_4 \quad k_{30} \quad (P_6\ e_{11} + P_4\ X)$$

INP Lengthen Ph4 or 4A — Ph4 — EXC — L $\longrightarrow$ U — X $\longrightarrow$ U

$$+ e_2\ F\ G\ (Q_1\ Q_2\ Q_3\ \underline{Q_5} + \underline{Q_1}\ Q_2\ Q_5\ Q_3\ Q_4\ \underline{P_1})$$

$$+ e_2\ f_4 \quad (\quad k_{36} \quad \underline{Q_5} + \quad k_{12} \quad Q_3\ Q_4\ \underline{P_1})$$

Adder Ph4 — ADU SBU — MPT < 64

$$+ e_2\ H\ Q_4\ (\underline{P_1} + \underline{t_6} + \underline{Q_3} + \underline{F}\ G) + F\ G\ \underline{H}\ \underline{Q_1}\ Q_2\ Q_5\ \underline{Q_3}\ Q_4\ L$$

$$+ e_2 \quad k_{18}\ (\underline{P_1} + \underline{t_6} + \underline{Q_3} + f_5\ ) + \quad f_4\ \underline{H} \quad k_{12} \quad \underline{Q_3}\ Q_4\ L$$

Adder Ph4A MPY — DIV, DVU — Ph4 DIV

$$+ H\ Q_3\ \underline{Q_4}\ \Big\{U\ (\underline{F}\ \underline{P_1} + G)\ (Q_5 + P_7) + P_3\ \underline{G}\ (F + P_1)\ (Q_5 + P_7)$$

$$+ \quad k_{29} \quad \Big\{U \quad f_9 \quad k_{23} \quad + P_3 \quad f_{10} \quad k_{23}$$

Ph4A — SLC SLT WP2 and Term. — SLC SLT WP3 on

$$+ \underline{Q}_5 \; \underline{P}_7 \left[U \; (\underline{F} + t_6) + u \; F \; \underline{t}_6 \right] \Big|$$

$$+ k_{40} \left[U \; (\underline{F} + t_6) + u \; F \; \underline{t}_6 \right] \Big|$$

SRT WP2 Not WP2

$$X' = X \Big| (Q_1 + \underline{Q}_2 + Q_3 + Q_4 + \underline{Q}_5 + \underline{P}_5 + R) \left[S_1 \; S_3 \; s_3 + \right.$$

$$X \Big| \qquad\qquad k_9 \qquad\qquad \left[t_3 + \right.$$

Ph4, Not EXC (U ⟶ X) Order

$$+ S_3 \; s_2 \; \underline{s}_3 + S_2 \; \underline{S}_3 \; (\underline{Q}_1 + Q_2 + \underline{Q}_3 + Q_4 + B + \underline{R})$$

$$t_4 \qquad + S_2 \; \underline{S}_3 \; (\underline{Q}_1 + Q_2 + \underline{Q}_3 + Q_4 + B + \underline{R})$$

Bit 31 NI Sector Not CME, CMG Unless B when repeated

$$+ (\underline{Q}_1 + Q_2 + \underline{Q}_3 + \underline{Q}_4 + \underline{Q}_5) \; \underline{S}_2 \; (\underline{S}_1 + \underline{S}_3) \Big] + H + \underline{F} + \underline{G} \Big|$$

$$+ \qquad k_{24} \qquad + \underline{Q}_5) \qquad t_1 \qquad \Big] \quad + H + f_{13} \Big|$$

Not LDX OP Adr Ph1,2,3,4A

$$+ F \; G \Big| (Q_1 + Q_2 + \underline{Q}_3 + \underline{Q}_4 + Q_5) \; \underline{S}_1 \; S_2 \; S_3$$

$$+ f_4 \Big| (\qquad k_{24} \qquad\qquad + Q_5) \qquad t_2$$

Ph4 Not LDC NI Trk

$$\left[(\underline{R} + \underline{K}) \; X + R \; K \; \underline{X} \right] \quad (Q_1 + \underline{Q}_2 + Q_3 + Q_4 + \underline{Q}_5 + \underline{P}_5 + R)$$

$$\left[(\underline{R} + \underline{K}) \; X + R \; K \; \underline{X} \right] \qquad\qquad\qquad\qquad k_9$$

Recirc if $\underline{R}$ Count X down if R Not EXC (U ⟶ X)

$$+ \underline{Q}_1 \; Q_2 \; \underline{Q}_3 \; \underline{Q}_4 \; Q_5 \; P_5 \; U \; \underline{R} + Q_1 \; \underline{Q}_2 \; Q_3 \; \underline{Q}_4 \; S_1 \; S_2 \; \underline{S}_3 \; \underline{B} \; R$$

$$k_{30} \qquad P_5 \; U \; \underline{R} + Q_1 \qquad k_{26} \; S_1 \; S_2 \; \underline{S}_3 \; \underline{B} \; R$$

EXC (U⟶X) CME CMG NI Sector, repeated

$$+ \underline{Q_1}\ Q_3\ Q_4\ Q_5\ \underline{Q_2}\ \underline{S_2}\ (\underline{S_1} + \underline{S_3})\ C + \underline{H}\ \underline{Q_1}\ \underline{Q_2}\ Q_3\ Q_4\ \underline{Q_5}\ \underline{S_1}\ S_2\ S_3\ V \Big|$$

$$+ \quad k_{14} \quad \underline{Q_2} \quad t_1 \quad C + \underline{H} \quad k_{25} \quad t_2 \quad V \Big|$$

LDX OP Adr — LDC NI Trk

A1.4 MAIN MEMORY

$$W' = \underline{H} \left[F\ G\ (\underline{t_6} + R) + F\ \underline{G}\ t_6\ K\ \underline{A} \right] \Big| Q_1\ Q_2\ \underline{Q_3}$$

$$\left[f_4\ (\underline{t_6} + R) + f_3 \quad K \right] \Big| Q_1\ Q_2\ \underline{Q_3}$$

Early Phase 4 — STU STL CLU CLL

$$+ \underline{Q_1}\ \underline{Q_2}\ Q_3\ \underline{Q_4} \left[\underline{Q_5}\ \underline{s_2}\ (\underline{s_1} + \underline{s_3}) + Q_5\ u \right] \Big|$$

$$+ \underline{Q_1} \quad k_{26} \quad \left[\underline{Q_5}\ \underline{s_2}\ (\underline{s_1} + \underline{s_3}) + Q_5\ u \right] \Big|$$

SAU Early OP Adr MST

$$V' = \underline{Q_5}\ u + Q_5\ (\underline{N}\ 1 + N\ 1^*)$$

$$= \underline{Q_5}\ u + Q_5\ (\underline{N}\ 1 + N\ 1^*)$$

STU CLU (SAU) STL CLL MST

A1.5 INPUT-OUTPUT SIGNALS

$$Y_o = F\ G\ Q_1\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_2}$$

$$f_4 \quad k_{10} \quad \underline{Q_2}$$

Ph4 PRU PRD

$$Y = (F\ G + H)\ \underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5}\ \underline{M}$$

$$k_1 \quad \underline{M}$$

Ph4 or 4A — INP — First Cycle

P_o = P_1 $\underline{Q_5}$

P_1 $\underline{Q_5}$

Selection Code

A1.6 ALPHA SIGNALS - ADDITION LOGIC

I_1' = $\underline{H}$ $\underline{F}$ M X $\underline{S_2}$ ($\underline{S_1}$ + $\underline{S_3}$) +

$\underline{H}$ $\underline{F}$ M X t_1 +

Ph2 Index mod OP Adr Only

+ H U* • (F + G Q_3 + P_1 $\underline{G}$)

+ H U* (F + G Q_3 + P_1 $\underline{G}$)

Ph4A MPY, DVU DIV MPY DIV, DVU, MPY
WP 4-65 WP 66,67 WP3

+ $\underline{H}$ F [$\underline{Q_1}$ ($\underline{P_1}$ P_3 + P_1 P_2) P_0 + Q_1 [$\underline{Q_5}$ U + Q_5 ($\underline{N}$ L + N L*)]]

+ $\underline{H}$ F [$\underline{Q_1}$ (e_{10}) P_0 + Q_1 [$\underline{Q_5}$ U + Q_5 e_{11}]]

Ph4 MPT ADU SBU ADL SBL

+ H $\underline{F}$ $\underline{Q_3}$ (G P_1 $\underline{P_6}$ $\underline{U^*}$ + $\underline{P_1}$ u* + P_1 P_6 U*)

+ H $\underline{F}$ $\underline{Q_3}$ (G P_1 $\underline{P_6}$ $\underline{U^*}$ + $\underline{P_1}$ u* + P_1 P_6 U*)

DVU DIV WP 67 WP2, 66 WP 67

I_2' = $\underline{H}$ $\underline{F}$ [$\underline{b_c}$ V + b_c ($\underline{N}$ L + N L*)] + $\underline{H}$ F ($\underline{Q_1}$ P_5 + Q_1 V)

$\underline{H}$ $\underline{F}$ e_7 + $\underline{H}$ F ($\underline{Q_1}$ P_5 + Q_1 V)

Ph2 Not EX L EX L Ph4 MPT ADU ADL SBU SBL

+ H P_1 P_6 ($\underline{F}$ $\underline{G}$ Q_3 + $\underline{F}$ G $\underline{Q_3}$ + F Q_3 P_7)

+ H P_1 P_6 (f_1 Q_3 + f_5 $\underline{Q_3}$ + F Q_3 P_7)

Ph4A MPY WP3 DIV, DVU ODD WP 5-65
Odd WP MPY

$$+ H \underline{P_1} (\underline{N} L + N L^*) (\underline{G} P_7 + \underline{G} \underline{Q_3} + \underline{F} \underline{Q_3} P_7)$$

$$+ H \underline{P_1} \quad e_{11} \quad (\underline{G} P_7 + \underline{G} \underline{Q_3} + \underline{F} \underline{Q_3} P_7)$$

Ph4A Even WP WP2, MPY Even WP 4-64 DVU DIV WP 2,66 DVU DIV

A1.7 ALPHA SIGNALS - SUBTRACTION CONTROL

$$S = \underline{H} F Q_1 Q_4 + H \left[\underline{F} \underline{G} Q_3 + \underline{F} G P_6 \right.$$

$$\underline{H} F Q_1 Q_4 + H \left[f_1 \quad Q_3 + f_5 P_6 \right.$$

Ph3 or 4 SBU SBL MPY WP2, 3 MPY DIV DVU WP 66,67

$$\left. + (F + \underline{G}) \underline{Q_3} (P_6 P_7 + \underline{P_6} \underline{P_7}) \right]$$

$$\left. + (F + \underline{G}) \underline{Q_3} (P_6 P_7 + \underline{P_6} \underline{P_7}) \right]$$

DVU DIV WP2-65

A1.8 ALPHA SIGNALS - MISCELLANEOUS

$$e_1 = \underline{U} V (\underline{N} L + N L^*)$$

$$\underline{U} V \quad e_{11}$$

$$e_2 = A I_1 I_2 + A \underline{I_1} \underline{I_2} + \underline{A} I_1 \underline{I_2} + \underline{A} \underline{I_1} I_2$$

Adder

$$e_3 = \underline{R} + \underline{Q_1} \underline{Q_2} Q_3 Q_4 \underline{Q_5}$$

$$\underline{R} + \quad k_{25}$$

Not repeat or LDC

$$e_4 = G (Q_2 + \underline{F}) \underline{t_6} + H Q_4$$

$e_5 = I_2 (I_1 \underline{S} + \underline{I_1} S)$

$e_6 = \underline{I_2} (I_1 S + \underline{I_1} \underline{S})$

$e_7 = \underline{b_c} V + b_c (\underline{N} L + N L^*)$

$\underline{b_c} V + b_c \quad e_{11}$

Not Ex L Ex L

$e_8 = \underline{Q_1} + U$

$e_9 = \underline{b_c} \underline{V} + b_c (\underline{N} \underline{L} + N \underline{L^*})$

$\underline{b_c} \underline{V} + b_c \quad e_{12}$

Not Ex L Ex L

$e_{10} = \underline{P_1} P_3 + P_1 P_2$

$e_{11} = \underline{N} L + N L^*$

Non-lengthen Lengthen

$e_{12} = \underline{N} \underline{L} + N \underline{L^*}$

Non-lengthen Lengthen

$e_{13} = U \underline{V} (\underline{N} L + N L^*)$

$U \underline{V} \quad e_{11}$

A1.9 ALPHA SIGNALS - PHASE CONTROL

$f_1 = \underline{F} \underline{G}$

Ph 1 or 4A

$f_2 = \underline{F}\ G\ \underline{H}$

$f_5\ \underline{H}$

Ph2

$f_3 = F\ \underline{G}\ t_6$

Ph3 Last Bit

$f_4 = F\ G$

Ph4 or 4A

$f_5 = \underline{F}\ G$

Ph2 or 4A

$f_6 = \underline{F}\ S_2 + F\ \underline{S_2}$

Ph1 NI Adr Ph3 OP Adr

$f_7 = \underline{G}\ \underline{H}\ \underline{S_1}\ S_3\ (\underline{F}\ S_2 + F\ \underline{S_2})\ (\underline{M} + \underline{Q_2})$

$= \underline{G}\ \underline{H}\ \underline{S_1}\ S_3 \qquad f_6 \qquad (\underline{M} + \underline{Q_2})$

Ph 1,3, Track Time First Cycle Only, if INP

$f_8 = \underline{F}\ G\ \underline{H}\ S_1\ S_3\ s_3$

$f_2 \qquad t_3$

Ph2 Order Time

$f_9 = \underline{F}\ \underline{P_1} + G$

$f_{10} = \underline{G}\ (F + P_1)$

$f_{11} = F\ G\ t_6$

Ph4 Last Bit or Ph4A

f_{12} = H P_1 t_6 (Q_3 + Q_4)

H P_1 t_6 (k_{34})

Ph4A Odd WP, Last Bit Not INP

f_{13} = $\underline{F}$ + $\underline{G}$

Ph1, 2, 3 or 4A

f_{14} = F G t_6 $\underline{H}$ (K_{25} + $\underline{R}$)

f_{11} $\underline{H}$ e_3

End Phase 4

A1.10 ALPHA SIGNALS - COMMAND

k_1 = (F G + H) $\underline{Q_1}$ Q_2 $\underline{Q_3}$ $\underline{Q_4}$ $\underline{Q_5}$

(f_4 + H) k_6 $\underline{Q_5}$

Ph4 or Ph4A INP

k_2 = F $\underline{G}$ S_1 S_3 $\underline{Q_2}$ Q_5 Q_1 $\underline{Q_3}$ $\underline{Q_4}$

F $\underline{G}$ S_1 S_3 $\underline{Q_2}$ Q_5 k_{10}

Ph3 order PRU

k_3 = H Q_3 $\underline{Q_4}$ $\underline{S_2}$ s_2 $\left[P_3\ \underline{P_4} + \underline{P_3}\ P_4 + P_3\ P_4\ \underline{P_5}\ (\underline{N}\ \underline{L} + N\ \underline{L^*})\right]$

k_5 $\underline{Q_4}$ t $\left[P_3\ \underline{P_4} + \underline{P_3}\ P_4 + P_3\ P_4\ \underline{P_5}\ e_{12}\right]$

Ph4 SLT, S SLC Overflow or End Shift

k_4 = F G $\underline{Q_1}$ Q_2 Q_5 Q_3 Q_4

= f_4 k_{12} Q_3 Q_4

Ph4 MPT

$k_5 = H \; Q_3$

Ph4 MPY SRT SLT SLC

$k_6 = \underline{Q}_1 \; Q_2 \; \underline{Q}_3 \; \underline{Q}_4$

INP EXC

$k_8 = \underline{G} \; \underline{H} \; \underline{S}_1 \; S_3 \; (\underline{F} \; S_2 + F \; \underline{S}_2) \; (\underline{M} + \underline{Q}_2)$

Ph1 and 3 Track Time

$+ (F \; G + H) \; \underline{Q}_1 \; Q_2 \; \underline{Q}_3 \; \underline{Q}_4 \; \underline{Q}_5 + F \; \underline{G} \; S_1 \; S_3 \; \underline{Q}_2 \; Q_5 \; Q_1 \; \underline{Q}_3 \; \underline{Q}_4$

k_2

Ph3 order PRU

$k_9 = Q_1 + \underline{Q}_2 + Q_3 + Q_4 + \underline{Q}_5 + \underline{P}_5 + R$

$k_{19} + k_{34} + \underline{Q}_5 + \underline{P}_5 + R$

Not EXC (U $\longrightarrow$ X) Unless repeat

$k_{10} = Q_1 \; \underline{Q}_3 \; \underline{Q}_4$

PRD PRU STU STL

$k_{11} = \underline{Q}_1 \; \underline{Q}_2 \; \underline{Q}_4$

SNS CXE SAU MST

$k_{12} = \underline{Q}_1 \; Q_2 \; Q_5$

EXC DIV SLC MPT

$k_{13} = \underline{Q}_1 \; Q_3 \; \underline{Q}_4$

SAU MST SRT SLT SLC

$k_{14} = \underline{Q}_1 \; Q_3 \; Q_4 \; Q_5$

MPT LDX

$k_{15} = Q_1 \; Q_3 \; Q_4$

TMI TBC SBU SBL

$k_{16} = (\underline{N} + \underline{S_2} \; s_2 \; s_1) \; \underline{Q_3} \; \underline{Q_4}$

$(\underline{N} + \quad t_8 \quad) \; \underline{Q_3} \; \underline{Q_4}$

$k_{17} = Q_1 + Q_3 + Q_4 + Q_5$

Not SNS, HLT, INP

$k_{18} = H \; Q_4$

Ph4 MPY DIV DVU

$k_{19} = Q_1 + \underline{Q_2}$

$k_{20} = \underline{Q_1} \; Q_2 \; \underline{Q_5}$

$k_{21} = \underline{Q_1} \; Q_2 \; \underline{Q_3} \; Q_4$

DVU DIV

$k_{22} = F \; G \; \underline{H} \; Q_4 \; V$

$f_4 \quad \underline{H} \; Q_4 \; V$

Ph4 or 4A MEM

$k_{23} = Q_5 + P_7$

$k_{24} = \underline{Q_1} + Q_2 + \underline{Q_3} + \underline{Q_4}$

Not (LDC LDX)

$k_{25} = \underline{Q_1}\ \underline{Q_2}\ Q_3\ Q_4\ \underline{Q_5}$

$\underline{Q_1}\ k_{38}\ Q_4\ \underline{Q_5}$

LDC

$k_{26} = \underline{Q_2}\ Q_3\ \underline{Q_4}$

$k_{38}\ \underline{Q_4}$

SAU MST CME CMG

$k_{27} = \underline{G}\ \underline{H}\ \underline{S_1}\ S_3\ (\underline{F}\ S_2 + F\ \underline{S_2})\ (\underline{M} + \underline{Q_2})$

f_7

Ph1, 3 Track Time — First cycle only, if INP

$+ (F\ G + H)\ \underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5}$

$+ \quad k_1$

Ph4 or 4a

$k_{28} = \underline{G}\ \underline{H}\ \underline{S_1}\ S_3\ (\underline{F}\ S_2 + F\ \underline{S_2})\ (\underline{M} + \underline{Q_2})$

f_7

$+ P_1\ (F\ G + H)\ \underline{Q_1}\ Q_2\ \underline{Q_3}\ \underline{Q_4}\ \underline{Q_5}$

$+ P_1\ k_1$

$+ P_1\ F\ \underline{G}\ S_1\ S_3\ Q_1\ \underline{Q_2}\ \underline{Q_3}\ \underline{Q_4}\ Q_5 + H\ Q_3\ \underline{S_2\ s_2}$

$+ P_1 \qquad k_2 \qquad + k_5 \quad \underline{t_6}$

Ph4 MPY SRT

SLT SLC

$k_{29} = H\ Q_3\ \underline{Q_4}$

$k_5\ \underline{Q_4}$

Ph4 SRT SLT SLC

k_{30} = $\underline{Q_1}$ Q_2 $\underline{Q_3}$ $\underline{Q_4}$ Q_5

k_6 Q_5

EXC

k_{31} = H P_1 t_6 Q_4

H P_1 t_6 Q_4

Ph4 Even WP MPY DVU DIV

k_{32} = F G $\underline{Q_1}$ Q_2 Q_3 Q_4 Q_5 + H Q_3

k_4 + k_5

Ph4 MPT Ph4 MPY SRT

SLT SLC

k_{33} = F G $\underline{S_2}$ s_2 $\underline{H}$ $\underline{R}$ Q_4

f_{11} $\underline{H}$ $\underline{R}$ Q_4

Ph4 Last WP

k_{34} = Q_3 + Q_4

k_{36} = Q_1 Q_2 Q_3

ADU ADL SBU SBL

k_{38} = $\underline{Q_2}$ Q_3

k_{39} = F $\underline{G}$ M $\underline{Q_1}$ Q_2 $\underline{Q_3}$ $\underline{Q_4}$ $\underline{Q_5}$

F $\underline{G}$ M k_6 $\underline{Q_5}$

Ph3 Not 1st cycle INP

k_{40} = $\underline{Q_5}$ $\underline{P_7}$

SRT

A1.11 ALPHA SIGNALS - TIMING

$t_1 = \underline{S_2}\ (\underline{S_1} + \underline{S_3})$

Operand Address

$t_2 = \underline{S_1}\ S_2\ S_3$

Next Instruction Track

$t_3 = S_1\ S_3\ s_3$

Order Time

$t_4 = S_3\ s_2\ \underline{s_3}$

Bit 31

$t_5 = \underline{S_2}\ \underline{S_3}$

OP Sector

$t_6 = \underline{S_2}\ s_2$

Sign time

$t_8 = \underline{S_2}\ s_2\ s_1$

$= t_6\ s_1$

Sign time of word 7

APPENDIX 2

RPC 4500 SYSTEM - FUNCTIONS AND LOGIC EQUATIONS

TABLES

Penciled change Mod 4/3 4/3

APPENDIX 2

RPC-4500 SYSTEM—FUNCTIONS AND LOGIC EQUATIONS

A2.1 SYSTEM CONTROL FUNCTIONS - Sect. A2.5, page A2-8

Subscript "c" refers to Computer-controlled (on-line) operation.
Subscript "m" refers to Manual-controlled (off-line) operation.

I_c, I_m	Input Flip-Flops	"Input" or "read" mode.
A_c, A_m	Advance Flip-Flops	Initiate a read cycle.
C	Copy Flip-Flop	"Input-duplication" mode (on-line only).
B_1 --- 7	Bit FF's - (on-line)	Store the character to be processed.
H_1 --- 7	Tape hole FF's (off-line)	
$\underline{B}'$, $\underline{H}'$		Reset B or H FF's.
B*, B_1*---B_7*	Bit information (on-line)	Information received from an input device.
H*, H_1*---H_7*	Hole information (off-line)	Information received from an input device.
E	Parity Error signal	Indicates the presence of an odd number of bits forming a character.
M	Metered input signal	Provides the start (Zs) during the "Single-character" input mode (on-line).
G_c, G_m	"Go-ahead" signals	Initiate an output cycle.
S	Select signal	Device selection or mode selection (on-line).
U	Unselect signal	Disengages all previously selected output or input and output devices ("Master-reset" on-line).
K_c, K_m	O.K. to type signal	Indicates when a selected typewriter will be understood (as input device).
Z_i	Input enable	
Z_o	Output enable	Synchronizing Signals to the computer (on-line) only.
Z_b	Input Begin	
Z_s	Start Compute	

Z_r	"Ready" Synchronism	
Z_q	Non-Readiness Query	
Y_i, Y_o, P_o, P_{20}---P_{70}		Signals from the computer (on-line).
F	Typewriter function	Represents characters not accepted by computer when L_b is not depressed.

A2.2 SWITCH FUNCTIONS

ON-LINE		TYPE
L_b	Single Character Mode Select switch	Latching (L)
L_c	Parity Error Reset switch	Non-Latching (N-L)
L_d	Parity Monitor Inhibit switch	L
L_e	Reset Aux. Units ("Unselect") switch	N-L
L_f	Input Duplication ("Copy") Mode Reset switch	N-L
L_g	Input Duplication ("Copy") Mode Select switch	N-L
L_h	Start Read (Select Input Mode) switch	N-L
L_i	Stop Read (Reset Input Mode) switch	N-L
L_j	Start Compute (Start Compute, Stop Input) switch	N-L
L_m	Typewriter to Computer	N-L
L_n	Reader to Computer	N-L
L_p	Computer to Typewriter	N-L
L_q	Computer to Punch	N-L
L_o	Auxiliary Typewriter to Computer	N-L
L_r	Computer to Auxiliary Typewriter	N-L

OFF-LINE		
L_s	Conditional Stop (ignore stop code) switch	L

L_t	Tape Feed switch	N-L
L_x	Start Read (Select Read Mode) switch	N-L
L_y	Stop Read (Reset Read Mode) switch	N-L
L_z	Single Character Mode Select switch	L
L_v	Reader Select	L
L_w	Punch Select	L
L_u	Typewriter Select	L

A2.3 PUNCH & READER CONTROL FUNCTIONS - Sect. A2.6, page A2-10

Q_r	Reader Select FF	Indicate that a device is active On-Line.
Q_p	Punch Select FF	
O_p	Output FF	Activates punch clutch and indicates that a punching cycle is incomplete.
L_n	Reader Select Sw.	Enables a device for On-Line operation.
L_q	Punch Select Sw.	
L_v	Reader Manual Operation Sw.	Indicate and enable a device for Off-Line operation (switches activate relays W & X)
L_w	Punch Manual Operation Sw.	
$T_1 \rightarrow 8$	Tape Holes 1, through 8	Holes in tape at reader brushes.

A2.4 TYPEWRITER CONTROL FUNCTIONS - Sect. A2.7, page A2-11

Q_i	Typewriter-input Select FF	Indicate that the typewriter is active On-Line.
Q_o	Typewriter-output Select FF	
L_m	Typewriter-input Select Sw.	Enables typewriter for On-Line operation.
L_o	Typewriter-output Select Sw.	
L_u	Typewriter Manual Operation Sw.	Indicates and enables the typewriter for Off-Line operation.
O_t	Typewriter-output FF	Initiates and indicates execution of typing cycle.
N_{46}	Key to Platen "sampling" signal	Indicates that a character is being presented by the typewriter (input).

A2.5 SYSTEM CONTROL FUNCTIONS—LOGIC EQUATIONS

A2.5.1 ON-LINE FUNCTIONS

$$I_c' = Y_i + L_h$$

$$\underline{I_c}' = Z_s + S + Z_b L_b + L_i$$

$$A_c' = I_c Z_q \ (= I_c Z_r R_3)$$

$$\underline{A_c}' = \frac{d}{dt} B^* \quad \text{(trailing edge)}$$

$$C' = S B_1 \underline{B_2} B_3 B_4 B_5 B_6 + L_g$$

$$\underline{C}' = S \underline{B_1} B_2 B_3 B_4 B_5 B_6 + L_f$$

$$B_1' = B_1^* + Y_o P_{70} + L_e + L_c$$

$$B_2' = B_2^* + Y_o P_{60} + L_e + L_c$$

$$B_3' = B_3^* + Y_o P_{50} + L_e + L_c$$

$$B_4' = B_4^* + Y_o P_{40} + L_e + L_c$$

$$B_5' = B_5^* + Y_o P_{30} + L_e + L_c$$

$$B_6' = B_6^* + Y_o P_{20}$$

$$B_7' = B_7^* + Y_o (\underline{B}') E + L_e + L_c$$

$$\underline{B_1}' \text{ --- } \underline{B_5}' = \underline{B}'$$

$$\underline{B_6}' = \underline{B}' + L_e + L_c$$

$$\underline{B_7}' = \underline{B}'$$

$$\underline{B}' = \frac{d}{dt} Y_o \text{ (leading)} + \frac{d}{dt} B^* \text{ (leading)}$$

$$E = (\underline{B_1} + \underline{B_2} + \underline{B_3} + \underline{B_4} + \underline{B_5} + \underline{B_6})$$

Not Delete Code

$$\Big\{\Big[(B_1 B_2 + \underline{B_1}\,\underline{B_2})\ (B_3 B_4 + \underline{B_3}\,\underline{B_4})$$

$$+ \ (B_1 \underline{B_2} + \underline{B_1} B_2)\ (B_3 \underline{B_4} + \underline{B_3} B_4)\Big]$$

B_{1-4} Even

$$\Big[(B_5 B_6 + \underline{B_5}\,\underline{B_6})\ B_7 + (B_5 \underline{B_6} + \underline{B_5} B_6)\ \underline{B_7}\Big] +$$

B_{5-7} Odd

$$\Big[(B_1 B_2 + \underline{B_1}\,\underline{B_2})\ (B_3 \underline{B_4} + \underline{B_3} B_4)$$

$$+ \; (B_1 \; \underline{B_2} + \underline{B_1} \; B_2) \; \; (B_3 \; B_4 + \underline{B_3} \; \underline{B_4})\Big]$$

B_{1-4} Odd

$$\Big[(B_5 \; B_6 + \underline{B_5} \; \underline{B_6}) \; \underline{B_7} + (B_5 \; \underline{B_6} + \underline{B_5} \; B_6) \; B_7\Big]\Big]$$

B_{5-7} Even

$M = \frac{d}{dt} \; B^*$ (trailing) (750 ms delay)

$Z_s = (L_d + \underline{E}\;) \Big[\underline{L_b} \; \underline{B_1} \; \underline{B_2} \; \underline{B_3} \; B_4 \; \underline{B_5} \; \underline{B_6} \; (\underline{B'}) \; B^* + L_b \; M\Big] + L_j$

$Z_r = R_i \; \underline{L_h} \; (\underline{E} + L_d)$

$Z_o = Z_r \; (R_2 + P_o)$

$Z_i = \underline{B^*} \; \underline{L_j}$ — Point in be Not Reset B — Single Char

$Z_b = B^* \; (\underline{B'}) \; \Big[L_b + (\underline{B_1} + \underline{B_2} + \underline{B_3} + \underline{B_4} + \underline{B_5} + \underline{B_6}) \; \underline{F}\Big]$

$F = \underline{B_5} \; \underline{B_6}$

$G_c = \Big[\frac{d}{dt} \; A_c$ (leading)$\Big] \; C + Y_o \; \underline{P_o}$

$K_c = Z_r \; I_c$

$S = P_o \; \underline{(B')} \; Y_o + L_e$

$U = B_1 \; B_2 \; B_3 \; B_4 \; B_5$

$Z_q = Z_r \; R_3$

A2.5.2 OFF-LINE FUNCTIONS

~~$I_m' = L_x$~~ Next Page

$\underline{I_m'} = L_y + H^* \; \underline{(H')} \; (L_z + \underline{H_1} \; \underline{H_2} \; \underline{H_3} \; \underline{H_4} \; \underline{H_5} \; \underline{H_6}) \; \underline{L_s} + \frac{d}{dt} \; L_v$ (leading)

$A_m' = R_5 \; K_m$

$\underline{A_m'} = \frac{d}{dt} \; H^*$ (trailing)

$(H_{1\rightarrow 7})' = H_{1\rightarrow 7}^*$

$\underline{(H_{1\rightarrow 7})'} = \underline{H'}$

~~$\underline{H'} = \frac{d}{dt} \; H^*$ (leading) + L_t~~ Next Page

$G_m = \frac{d}{dt} \; A_m$ (leading) + L_t

$K_m = I_m \; R_4$

All 4343 Mode on these pages

$R_5 \quad = \underline{L}_x (N_{46} L_u + R_{e2} R_{e4} L_w)$

A2.6 PUNCH AND READER CONTROL LOGIC

A2.6.1 PUNCH LOGIC

P_e (punch enable) = Po/s1 (Reverse Tape Feed Mode)

Po/s1' = [d/dt Op (leading)] (Punch Pwr On) (Punch Trob. Sw)

Po/s1' = Po/s1' (4.5 ms delay)

Po/s2' = d/dt Po/s1 (trailing)

Po/s2' = Po/s2' (13.5 ms delay)

$Q_p' \quad = S_1 B_1 \underline{B}_4 \underline{B}_5 + L_q$

$\underline{Q}_p' \quad = SU + \frac{d}{dt} (Lw)$ leading

$O_p' \quad = (Q_p G_c \underline{L}_w + G_m L_w + L_t$ + Buzz Sw') Po/s2

G_r = % P_e

$\underline{Q}_p' \quad =$ ~~(Punch cam 4) + $\underline{Q}_p$ $\underline{L}_w$~~ d/dt Po/s2 (trailing) + d/dt Power On

PUNCH CLUTCH = O_p (Punch Cam 1) · (Punch Tape-Trouble Switches)

FORWARD TAPE FEED = ~~O_p (Punch Cam 1) · (Punch Tape Trouble Switches)~~

Po/s1 (Reverse Tape-Feed Mode)

REVERSE TAPE FEED = (Reverse Tape-Feed Mode) Po/s1

FEED-(INDEX) HOLE MAGNET = ~~(Reverse Tape Feed Mode) · (Punch cam 5)~~ Forward Tape Feed

CHARACTER PUNCH MAGNETS$_{1 \rightarrow 8}$ = P_e($B_{1 \rightarrow 8}$ ($\underline{L}$w) + $H_{1 \rightarrow 8}$ (Lw)) ~~(Punch cam 2)~~

$R_1 \quad =$ ~~(Punch cam 3)~~ $\underline{O}_p$ $\underline{L}$w + $\underline{Q}_p$ Lw

$R_4 \quad =$ ~~(Punch cam 3)~~ $\underline{O}_p$ Lw + $\underline{L}$w

$R_2 \quad = Q_p$

start Rdr. off-line Tr. Rdr.

$I_m' = L_x (L_u + L_v)$

Ro/s1' = d/dt Tape Feed (leading)

R_r = d/dt Ro/s1 (trailing) + d/dt Power On

3.0 6.0

A2.6.2 READER LOGIC

$Q_r' \quad = S \underline{B}_3 \underline{B}_4 \underline{B}_5 \underline{B}_6 + L_n$

$\underline{Q}_r' \quad = S \underline{B}_6 (\underline{Q}_r') + \frac{d}{dt} (L_v)$ leading

$B^* \quad =$ ~~(Reader cam 1)~~ $Q_r A_c \underline{L}_v$

$H^* \quad =$ ~~(Reader cam 1)~~ $A_m L_v$

$\underline{R}_8'$ = d/dt Tape Feed (leading)

H' = d/dt H* (leading) + L_t + Buzz Sw.

$B_{1 \rightarrow 8}^* \quad = T_{1 \rightarrow 8}$ (B*)

$H_{1 \rightarrow 8}^* \quad = T_{1 \rightarrow 8}$ (H*)

TAPE FEEDS = ~~A_c Q_r L_v + A_m L_v~~ B* $\underline{L}$v + H* Lv

READER CLUTCH = $Q_r R_{e3} + \underline{L}_v I_m$

$R_3 \quad =$ ~~[illegible]~~ R_r (Rdr. Power On) (Reader Tape-Trouble Switches) ~~[illegible]~~ $Q_r \underline{L}_v$ On line

$R_5 \quad =$ ~~(R_{e2} R_{e4}) L_v~~ R_r (Rdr Power On) (Reader Tape-Trouble Switches) ~~[illegible]~~ LV Off line

A2.7 TYPEWRITER LOGIC

$Q_o' = S\ B_2\ \underline{B_4}\ \underline{B_5} + L_p$

$\underline{Q_o}' = SU + \frac{d}{dt}\ (L_u)$ leading

$O_t' = Q_o\ G_c\ \underline{L_u} + G_m\ L_u$

$\underline{O_t}' = \frac{d}{dt}\ (N_{46})$ leading $+ \underline{Q_o}\ \underline{L_u} + L_u\ \underline{L_v} + Q_i\ A_c\ \underline{L_u}$

Translator Enable $= O_t$

Translator Bit Drive $= B_{1 \longrightarrow 6}\ (\underline{L_u}) + H_{1 \longrightarrow 6}\ (L_u)$

$R_1 = \underline{O_t}\ \underline{L_u} + \underline{Q_o}\ L_u$

$R_4 = \underline{O_t}\ L_u + \underline{L_u}$

$R_2 = Q_o\ \underline{L_u}$

$Q_i' = S\ B_3\ \underline{B_4}\ \underline{B_5}\ \underline{B_6} + L_m$

$\underline{Q_1}' = S\ \underline{B_6}\ (\underline{Q_1'}) + \frac{d}{dt}\ (L_u)$ leading

$B^* = \underline{L_u}\ A_c\ Q_i\ N_{46}$

$H^* = L_u\ \underline{L_v}\ A_m\ N_{46}$

$B_{1 \longrightarrow 7}^*$ = (Encoder bits: 1, 2, 4, 8, F, A, P) B^*

$H_{1 \longrightarrow 7}^*$ = (Encoder bits) H^*

$R_3 = \underline{L_u}\ Q_i\ N_{46}$

$R_5 = L_u\ \underline{L_v}\ N_{46}$

O.K. TO TYPE LIGHT $= \underline{L_u}\ Q_i\ K_c + L_u\ \underline{L_v}\ K_m$

TABLE A2-1

LOCATION OF SIGNALS WITHIN RPC-4430

SIGNAL		CARD (OR CONNECTORS) OF ORIGIN	CARD(S) (OR CONNECTORS) USED ON
A_c	Advance FF	6	
$\underline{A_c}$	(On-Line)	6	
A_m	Advance FF	12	25, 46
$\underline{A_m}$	(Off-Line)	12	
A_p	Power Output of A_c	6	17, 25, 27, 31, 32, 42, 46
B_1	Bit_1 FF (On-Line)	1	3, 4, 45
$\underline{B_1}$		1	3, 4
B_{1p}	Power Output of B_1	1	8, 11, 14, 29, 42
B_1*	Input to B_1	21, 26, 31, 42	1, 27
B_2	Bit_2 FF (On-Line)	1	3, 4, 45
$\underline{B_2}$		1	3, 4
B_{2p}	Power Output of B_2	1	8, 11, 14, 29, 42
B_2*	Input to B_2	21, 26, 31, 42	1, 27
B_3	Bit_3 FF (On-Line)	1	3, 4, 45
$\underline{B_3}$		1	3, 4
B_{3p}	Power Output of B_3	1	8, 11, 14, 29, 42
B_3*	Input to B_3	21, 26, 31, 42	1, 27
B_4	Bit_4 FF (On-Line)	1	3, 4, 45
$\underline{B_4}$		1	3, 4
B_{4p}	Power Output of B_4	1	8, 11, 14, 29, 42
B_4*	Input to B_4	21, 26, 31, 42	1, 27
B_5	Bit_5 FF (On-Line)	2	3, 4, 45
$\underline{B_5}$		2	3, 4
B_{5p}	Power Output of B_5	2	8, 11, 14, 29, 42
B_5*	Input to B_5	21, 26, 31, 42	2, 27
B_6	Bit_6 FF (On-Line)	2	3, 4, 45
$\underline{B_6}$		2	3, 4
B_{6p}	Power Output of B_6	2	8, 11, 14, 29, 42
B_6*	Input to B_6	21, 26, 31, 42	2, 27
B_7	Bit_7 FF (On-Line)	2	
$\underline{B_7}$		2	3
B_{7p}	Power Output of B_7	2	11, 42
B_7*	Input to B_7	21, 26, 31, 42	2
B*	Input Sampling signal (On-Line)	21, 26, 31, 42	6, 27
$\underline{B}$*		6	4, 5
$\underline{B}$'	B FF reset	5	1, 2, 4
C	Copy FF	4	6
$\underline{C}$		4	6

TABLE A2-1

LOCATION OF SIGNALS WITHIN RPC-4430 (Cont.)

SIGNAL		CARD (OR CONNECTORS) OF ORIGIN	CARD(S) (OR CONNECTORS) USED ON
E	Parity Error	3	2
F	Typewriter Function Character	3	
G_c	Output Go-ahead (On-Line)	6	5
$\underline{G}_c$		5	22, 25, 27, 32, 42
$\underline{G}_m$	(Off-Line)	12	22, 25, 27, 46
H_1	Bit_1 FF (Off-Line)	13	9, 15
$\underline{H}1$		13	
H_1*	H_1 Input	21, 26	13
H_2	Bit_2 FF (Off-Line)	13	9, 15
$\underline{H}_2$		13	
H_2*	H_2 Input	21, 26	13
H_3	Bit_3 FF (Off-Line)	13	9, 15
$\underline{H}_3$		13	
H_3*	H_3 Input	21, 26	13
H_4	Bit_4 FF (Off-Line)	13	9, 15
$\underline{H}_4$		13	
H_4*	H_4 Input	21, 26	13
H_5	Bit_5 FF (Off-Line)	13	9, 15
$\underline{H}_5$		13	
H_5*	H_5 Input	21, 26	13
H_6	Bit_6 FF (Off-Line)	13	9, 15
$\underline{H}_6$		13	
H_6*	H_6 Input	21, 26	13
H_7	Bit_7 FF (Off-Line)	12	9
$\underline{H}_7$		12	
H_7*	H_7 Input	21, 26	12
H*	Input Sampling Signal (Off-Line)	21, 26	12
$\underline{H}$*		12	12
$\underline{H}$'	H FF reset	12	12, 13
I_c	Input FF	5	
$\underline{I}_c$	(On-Line)	5	6
I_m	Input FF	12	
$\underline{I}_m$	(Off-Line)	12	12, 21
K_c	OK to type (On-Line)	6	25, 31, 42
K_m	OK to type (Off-Line)	12	25
L_1	Next Character	7	47
L_2	Next Character	7	47

TABLE A2-1

LOCATION OF SIGNALS WITHIN RPC-4430 (Cont.)

SIGNAL		CARD (OR CONNECTORS) OF ORIGIN	CARD(S) (OR CONNECTORS) USED ON
L_3	Next Character	7	47
L_4	Next Character	7	47
L_5	Next Character	7	47
L_6	Next Character	7	47
L_7	Next Character	7	47
L_8	Error Lamp	11	46
L_9	Reader Tape Trouble	8	46
L_{10}	Punch Tape Trouble	9	46
L_{b-3}	Single	47	5
L_{b-4}	Character	3	47
L_{b-5}	Input Mode	47	5
L_{b-7}	Switch	4	47
L_{b-8}	Signals	5	47
L_{c-13}	Parity Monitor Reset	3	47
L_{d-3}	Parity Monitor Inhibit	3	6, 47
L_{d-6}	Switch Signals	3	5, 47
L_{e-1}	Master Reset	47	1, 2
L_{e-4}	Switch Signals	5	47
L_{f-1}	Input Duplicator Reset SW	4	47
L_{f-13}	Input Duplicator Reset Lamp	6	47
L_{g-1}	Input Duplicator Set Switch	4	47
L_{g-13}	Input Duplicator Set Lamp	6	47
L_{h-1}	Start Read Sw. Signal	47	5
L_{i-1}	Stop Read Sw. Signal	47	5
L_{j-1}	Start compute Sw. Signal	47	5
L_{m-1}	TW to comp. Switch Signal	46	14
L_{m-13}	TW to comp. Lamp	17	46
L_{o-1}	Aux TW to comp. SW Signal	46	29
L_{o-13}	Aux TW to comp. Lamp	32	46
L_{p-1}	Comp. to TW Sw. Signal	46	17
L_{p-13}	Comp. to TW Lamp	17	46
L_{q-1}	Comp. to Punch Sw. Signal	46	11
L_{q-13}	Comp. to Punch Lamp	11	46
L_{r-1}	Comp. to Aux. TW Sw. Signal	46	32
L_{r-13}	Comp. to Aux. TW Lamp	32	46
L_{s-2}	Conditional Stop Sw. Signal	12	46
L_{s-3}	Conditional Stop Sw. Signal	46	12

TABLE A2-1

LOCATION OF SIGNALS WITHIN RPC-4430 (Cont.)

SIGNAL		CARD (OR CONNECTORS) OF ORIGIN	CARD(S) (OR CONNECTORS) USED ON
L_{t-2}	Tape Feed Sw. Signal	46	12
L_{u-3}	TW Select Sw. Signal	46	17
L_{u-4}	TW Select Sw. Signal	46	25, 26
L_{v-3}	TW Output Enable	46	17, 25
L_{v-4}	Reader Select Sw. Signal	46	21
L_{v-8}	Reader Select Sw. Signal	46	8
L_{w-1}	Punch Select Sw. Signal	46	22
L_{x-1}	Start Read (Off-Line) Sw. Signal	46	12
L_{y-1}	Stop Read (Off-Line) Sw. Signal	46	12
$\underline{M}$	Single-Char. Mode 1 Shot Signal	4	47
N_a	Misc. Lamp Voltages	49	43, 44, 46, 50
N_b		49	46
N_c		49	47
N_d		49	47
N_e		49	46
N_f		49	43, 44, 50
N_g			
N_1	Off-Line Start Signal	13	46
N_2	Punch fwd. Tape-feed Sol.	49	50
N_3	Signal to Aux TW from B_{1p}	30	29
N_4	Index Punch Sol.	49	50
N_5	Reverse Tape-feed Sol.	49	50
N_6	Tape-Backspace Relay Sol	49	14
N_7	Prime TW Soft KP Echo	44	17
N_8	Reader Cam 1	50	7
N_9	Reader B*, H* 1-shot	7	50
N_{10}	$\underline{TO}$ Reader cam 1	8	50
N_{11}	$\underline{TO}$ Reader cam 1	50	8
N_{12}	Reader cam 3	50	8
N_{13}	Reader Primary and Secondary Tape-feed Solenoid	8	50
N_{14}	Reader Clutch Solenoid	8	50
N_{15}	$\underline{TO}$ Reader cam 2	50	8
N_{16}	Reader Tape Trouble	50	8
N_{17}	$\underline{TO}$ Punch cam 4	50	9
N_{18}	Punch Clutch Solenoid	9	49, 50

TABLE A2-1

LOCATION OF SIGNALS WITHIN RPC-4430 (Cont.)

SIGNAL		CARD (OR CONNECTORS) OF ORIGIN	CARD(S) (OR CONNECTORS) USED ON
N_{19}	Punch Tape Trouble	50	9
N_{20}	TO Punch cam 1	9	50
N_{21}	Punch cam 1	50	9
N_{22}	Punch cam 2	50	10
N_{23}	Punch Solenoid 1	10	50
N_{24}	Punch Solenoid 2	10	50
N_{25}	Punch Solenoid 3	10	50
N_{26}	Punch Solenoid 4	10	50
N_{27}	Punch Solenoid 5	10	50
N_{28}	Punch Solenoid 6	10	50
N_{29}	Punch Solenoid 7	10	50
N_{30}	Punch cam 3	50	10
N_{31}	To Selection Monitor Resistor and Lamp	21, 22, 25, 28	11
N_{32}	For Tape-Backspace	22	25
Primary Typewriter Signals			
N_{33}	Translator "1" Drive	15	44
N_{34}	Translator "2" Drive	15	44
N_{35}	Translator "4" Drive	15	44
N_{36}	Translator "8" Drive	15	44
N_{37}	Translator "F" Drive	15	44
N_{38}	Translator "A" Drive	15	44
N_{39}	Encoder Output "1"	16	44
N_{40}	Encoder Output "2"	16	44
N_{41}	Encoder Output "4"	16	44
N_{42}	Encoder Output "8"	16	44
N_{43}	Encoder Output "F"	16	44
N_{44}	Encoder Output "A"	16	44
N_{45}	Encoder Output "P"	16	44
N_{46}	Key at Platen (KP)	44	16
N_{47}	O.K. to Type Lamp	16	44
Auxiliary Typewriter Signals			
N_{48}	Signal from B_{2p}	30	29
N_{49}	Signal from B_{3p}	30	29
N_{50}	Signal from B_{4p}	30	29
N_{51}	Signal from B_{5p}	30	29
N_{52}	Signal from B_{6p}	30	29
N_{53}	Translator "1" Drive	30	43
N_{54}	Translator "2" Drive	30	43
N_{55}	Translator "4" Drive	30	43

TABLE A2-1

LOCATION OF SIGNALS WITHIN RPC-4430 (Cont.)

SIGNAL		CARD (OR CONNECTORS) OF ORIGIN	CARD(S) (OR CONNECTORS) USED ON
N_{56}	Translator "8" Drive	30	43
N_{57}	Translator "F" Drive	30	43
N_{58}	Translator "A" Drive	30	43
N_{59}	Encoder Output "1"	31	43
N_{60}	Encoder Output "2"	31	43
N_{61}	Encoder Output "4"	31	43
N_{62}	Encoder Output "8"	31	43
N_{63}	Encoder Output "F"	31	43
N_{64}	Encoder Output "A"	31	43
N_{65}	Encoder Output "P"	31	43
N_{66}	Key at Platen (KP)	43	31
N_{67}	O.K. to type Lamp	31	43
N_{68}	B*, H* 1-Shot	31	
N_{69}	"Soft" KP Echo	43	32
N_{70}	Prime TW B*, H* 1-Shot	16	
O_p	Punch Output FF	9	50
$\underline{O}_p$		9	
O_t	Typewriter Output FF	17	44
$\underline{O}_t$		17	
O_x	Aux TW Output FF	32	43
$\underline{O}_x$		32	
Computer Print Signals			
$\underline{P}_o$	Non-Selection Printout	45	5, 6
P_{20}	P_2	45	2
P_{30}	P_3	45	2
P_{40}	P_4	45	1
P_{50}	P_5	45	1
P_{60}	P_6	45	1
P_{70}	P_7	45	1
Q_i	Typewriter input	14	17, 25
$\underline{Q}_i$	Select FF	14	16
Q_o	Typewriter Output	17	
$\underline{Q}_o$	Select FF	17	25
Q_o'		14	17
Q_p	Punch Select FF	11	
$\underline{Q}_p$		11	22
Q_r	Reader Select FF	8	21
$\underline{Q}_r$		8	21

TABLE A2-1

LOCATION OF SIGNALS WITHIN RPC-4430 (Cont.)

SIGNAL		CARD (OR CONNECTORS) OF ORIGIN	CARD(S) (OR CONNECTORS) USED ON
Q_y	Aux. TW Input	29	31, 32
$\underline{Q}_y$	Select FF	29	31
Q_z	Aux. TW Output	32	
$\underline{Q}_z$	Select FF	32	32
Q_z'		29	32
$\underline{R}_1$	Output Device non-ready	32	6, 22, 25, 27, 42
$\underline{r}_1$	(On-Line)	42	6
R_2	Output Device Selection	42	5, 22, 25, 32
r_2	Ready (On-Line)	42	5
R_3	Input Device Ready	42	6, 21, 25, 31
r_3		42	6
$\underline{R}_4$	Output Device non-ready (Off-Line)	22, 25	12, 28
R_5	Input Device Ready (Off-Line)	21, 25	12, 28, 46
S	Select	5	4, 8, 11, 14, 17, 29, 32, 42
T_1	Tape Holes	50	7
T_2	Tape Holes	50	7
T_3	Tape Holes	50	7
T_4	Tape Holes	50	7
T_5	Tape Holes	50	7
T_6	Tape Holes	50	7
T_7	Tape Holes	50	7
U	Unselect	4	11, 17, 32, 42
Typewriter On-Off Line Relay V_I			
V_{1b}	B* or H*	16	26
V_{2b}	B_1* or H_1*	16	26
V_{3b}	B_2* or H_2*	16	26
V_{4b}	B_3* or H_3*	16	26
V_{5b}	B_4* or H_4*	16	26
V_{6b}	B_5* or H_5*	16	26
V_{7b}	B_6* or H_6*	16	26
V_{8b}	B_7* or H_7*	16	26
V_{9a}	Signal from H_1	15	26
V_{9b}	Signal to Translator "1" Drivers	26	15
V_{9c}	Signal from B_{1p}	14	26
V_{10a}	From H_2	15	26
V_{10b}	To Translator "2" Drivers	26	15
V_{10c}	From B_{2p}	14	26

TABLE A2-1

LOCATION OF SIGNALS WITHIN RPC-4430 (Cont.)

SIGNAL		CARD (OR CONNECTORS) OF ORIGIN	CARD(S) (OR CONNECTORS) USED ON
V_{11a}	From H_3	15	26
V_{11b}	To Translator "4" Drivers	26	15
V_{11c}	From B_{3p}	14	26
V_{12a}	From H_4	15	26
V_{12b}	To Translator "8" Drivers	26	15
V_{12c}	From B_{4p}	14	26
V_{13a}	From H_5	15	26
V_{13b}	To Translator "F" Drivers	26	15
V_{13c}	From B_{5p}	15	26
V_{14a}	From H_6	15	26
V_{14b}	To Translator "A" Drivers	26	15
V_{14c}	From B_{6p}	14	26
Typewriter On-Off Line Relay V_{II}			
V_{1y}	For Selection Monitor Light	17	25
V_{2y}	$\underline{R}_1$ or $\underline{R}_4$	17	25
V_{3y}	$\underline{R}_1$ or R_2	17	25
V_{4y}	Resets O_t FF with $\underline{Q}_o$ (On-Line)	25	17
V_{5y}	$\underline{G}_c$ or $\underline{G}_m$	25	17
V_{6x}	Reset for Q_i and Q_o	25	14, 17
V_{6z}	Ground Signal for gating R_3 and N_{70}	25	16
V_{7y}	R_3 or R_5	25	16
V_{8y}	A_p or A_m	25	16
V_{9y}	K_c or K_m	25	16
V_{10y}	Q_i or L_{u-3} (inhibits Type-out during Type-input)	25	16
V_{11y}	For Tape-Backspace	14	9, 25
Reader Relays (On-Off Line)			
W_{2-a}	Pull Negative Resistor	7	21
W_{2-b}	Q_i or Negative	21	8
W_{3-b}	R_3 or R_5	21	50
W_{4-b}	$\underline{Q}_r$ or $\underline{I}_m$	21	8
W_{5-b}	Selection Monitor Light	8	21
W_{6-b}	B_1* or H_1*	21	7
W_{7-b}	B_2* or H_2*	21	7
W_{8-b}	B_3* or H_3*	21	7
W_{9-b}	B_4* or H_4*	21	7
W_{10-b}	B_5* or H_5*	21	7
W_{11-b}	B_6* or H_6*	21	7

TABLE A2-1

LOCATION OF SIGNALS WITHIN RPC-4430 (Cont.)

SIGNAL		CARD (OR CONNECTORS) OF ORIGIN	CARD(S) (OR CONNECTORS) USED ON
W_{12-b}	B_7* or H_7*	21	7
W_{13-b}	B* or H*	21	7
W_{14-b}	Q_i reset	21	8, 12
Punch On-Off Line Relays			
X_{1-b}	For Selection Monitor	11	22
X_{2-b}	For Tape-Backspace	22	44
X_{3-b}	For Q_p reset	22	11
X_{4-a}	Signal From H_1	9	22
X_{4-b}	To Solenoid "1" Driver	22	10
X_{4-c}	Signal From B_{1p}	11	22
X_{5-a}	From H_2	9	22
X_{5-b}	To Solenoid "2" Driver	22	10
X_{5-c}	From B_{2p}	11	22
X_{6-a}	From H_3	9	22
X_{6-b}	To Solenoid "3" Driver	22	10
X_{6-c}	From B_{3p}	11	22
X_{7-a}	From H_4	9	22
X_{7-b}	To Solenoid "4" Driver	22	10
X_{7-c}	From B_{4p}	11	22
X_{8-a}	From H_5	9	22
X_{8-b}	To Solenoid "5" Driver	22	10
X_{8-c}	From B_{5p}	11	22
X_{9-a}	From H_6	9	22
X_{9-b}	To Solenoid "6" Driver	22	10
X_{9-c}	From B_{6p}	11	22
X_{10-a}	From H_7	9	22
X_{10-b}	To Solenoid "7" Driver	22	10
X_{10-c}	From B_{7p}	11	22
X_{11-b}	$\underline{G}_c$ or $\underline{G}_m$	22	9
X_{12-b}	O_p reset (from $\underline{Q}_p$)	22	9
X_{13-b}	$\underline{R}_1$ or $\underline{R}_4$	22	10
X_{14-b}	$\underline{R}_1$ or R_2	11	22
Signals From Computer			
$\underline{Y}_i$	Non (Start Input)	45	5
Y_o	Start Output	2	1, 2, 6
$\underline{Y}_o$		45	2, 5
Signals To Computer			
Z_b	Begin Input	5, 47	45
Z_i	Input Enable	6, 47	45

TABLE A2-1

LOCATION OF SIGNALS WITHIN RPC-4430 (Cont.)

SIGNAL		CARD (OR CONNECTORS) OF ORIGIN	CARD(S) (OR CONNECTORS) USED ON
Z_o	Output Enable	5	45
$\underline{Z}_q$	Non-Readiness Query	6	45
Z_r	Ready Synchronism	6	47
$\underline{Z}_r$		6	5
Z_s	Start Signal	5	45

APPENDIX 3

RPC-4000 SYSTEM SCHEMATICS

PART I - CENTRAL COMPUTER

PART II - INPUT-OUTPUT (ON-LINE)

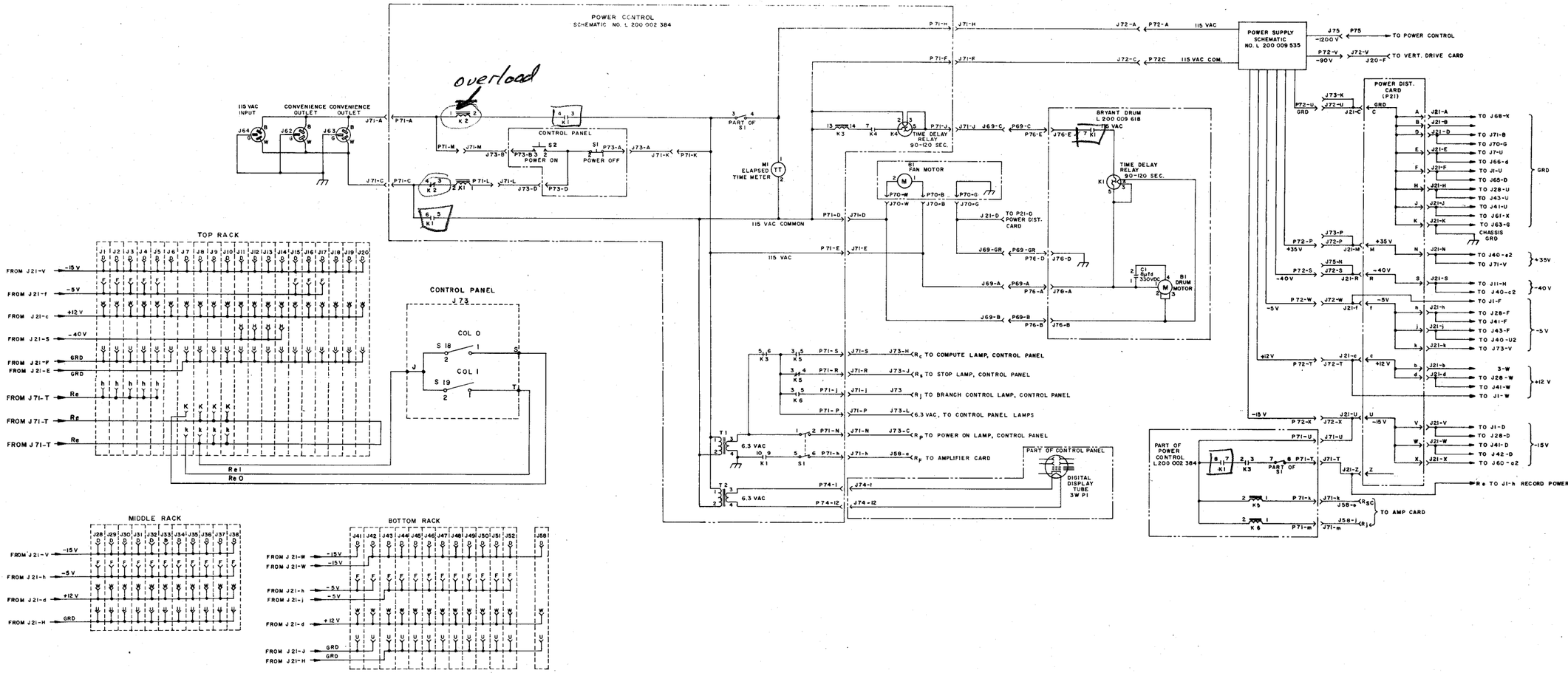
PART III - INPUT-OUTPUT (OFF-LINE)

PART IV - SIMPLIFIED SYSTEM SCHEMATICS - RPC-4500

PART IV (Cont.)

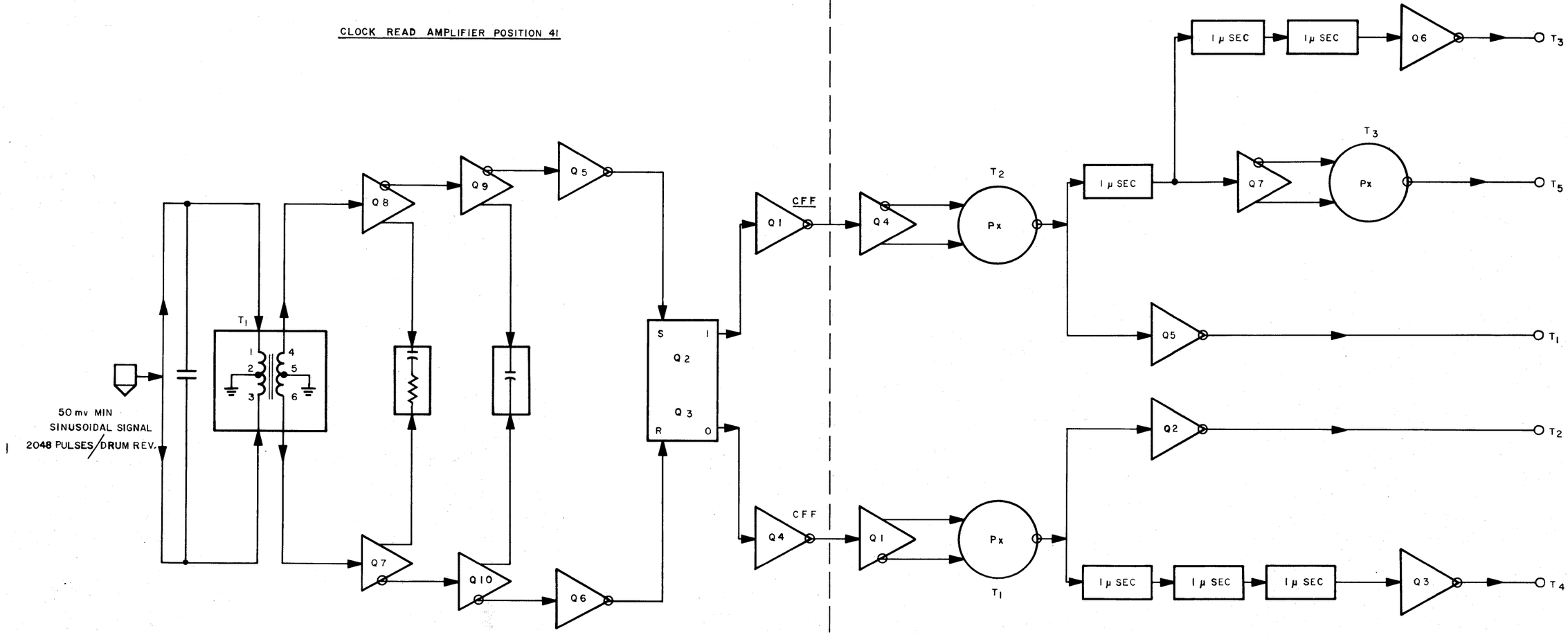
PART IV (Cont.)

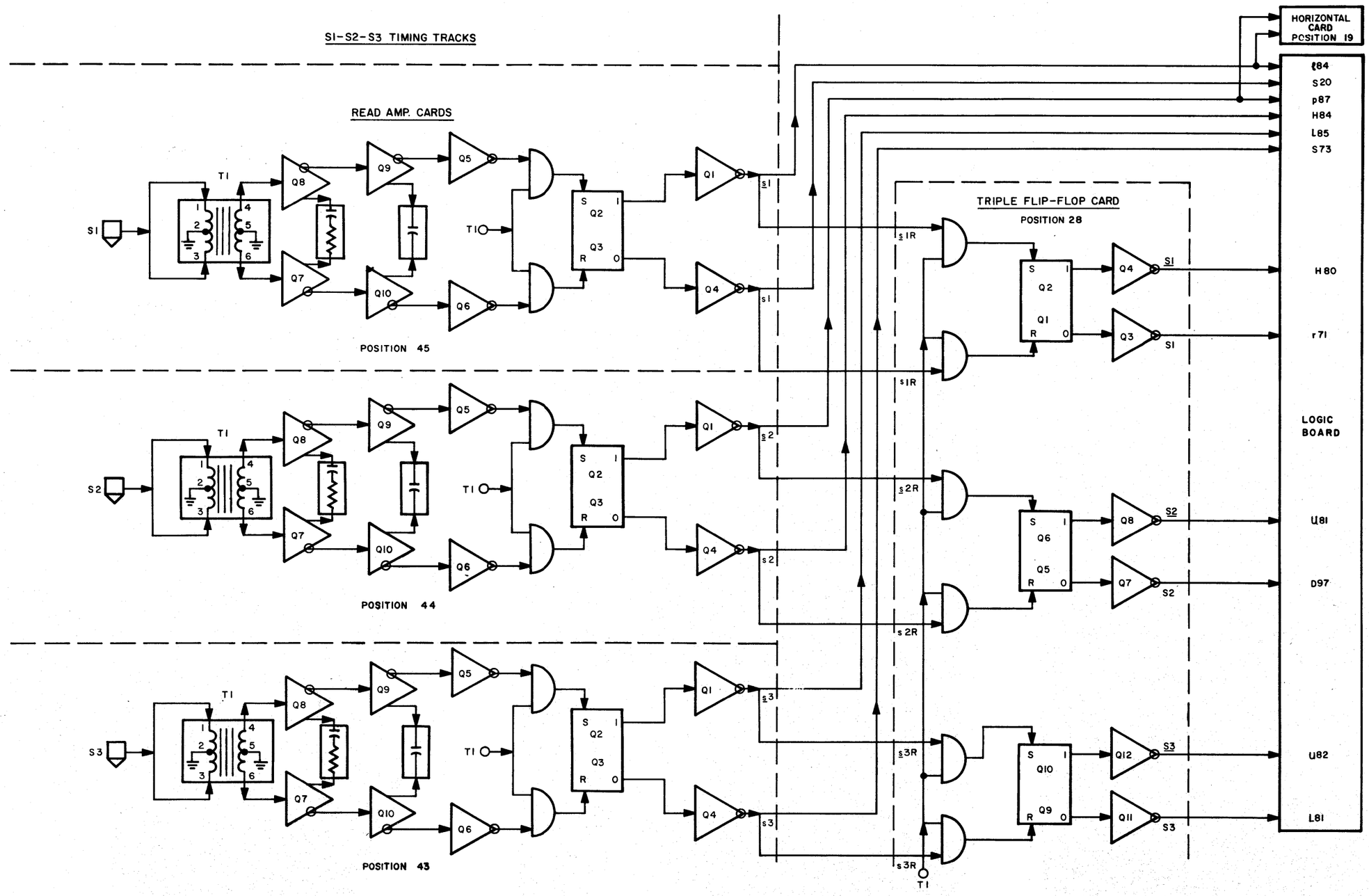
DRAWING NO.		PAGE
53	$O_t' = G_c \underline{L}_u \qquad G_c = Y_o P_o$ $\underline{O}_t' = \frac{d}{dt}$ (N-46) LEADING	A3-91
54	$K_m = I_m R_4 \qquad R_4 = (PU\text{-}3\ \underline{O}_p L_w + \underline{L}_w)(\underline{O}_t L_u + \underline{L}_u)$	A3-92
55	$A_m' = K_m R_5$	A3-93
56	$R_3 = (Re\text{-}2\ Re\text{-}4)\ Q_r \underline{L}_v$ (R.T.T.S.) + $\underline{L}_u Q_i$ N-46 $R_5 = (Re\text{-}2\ Re\text{-}4)\ L_v$ (R.T.T.S.) + $Lu\ \underline{L}_v$ N-46	A3-94

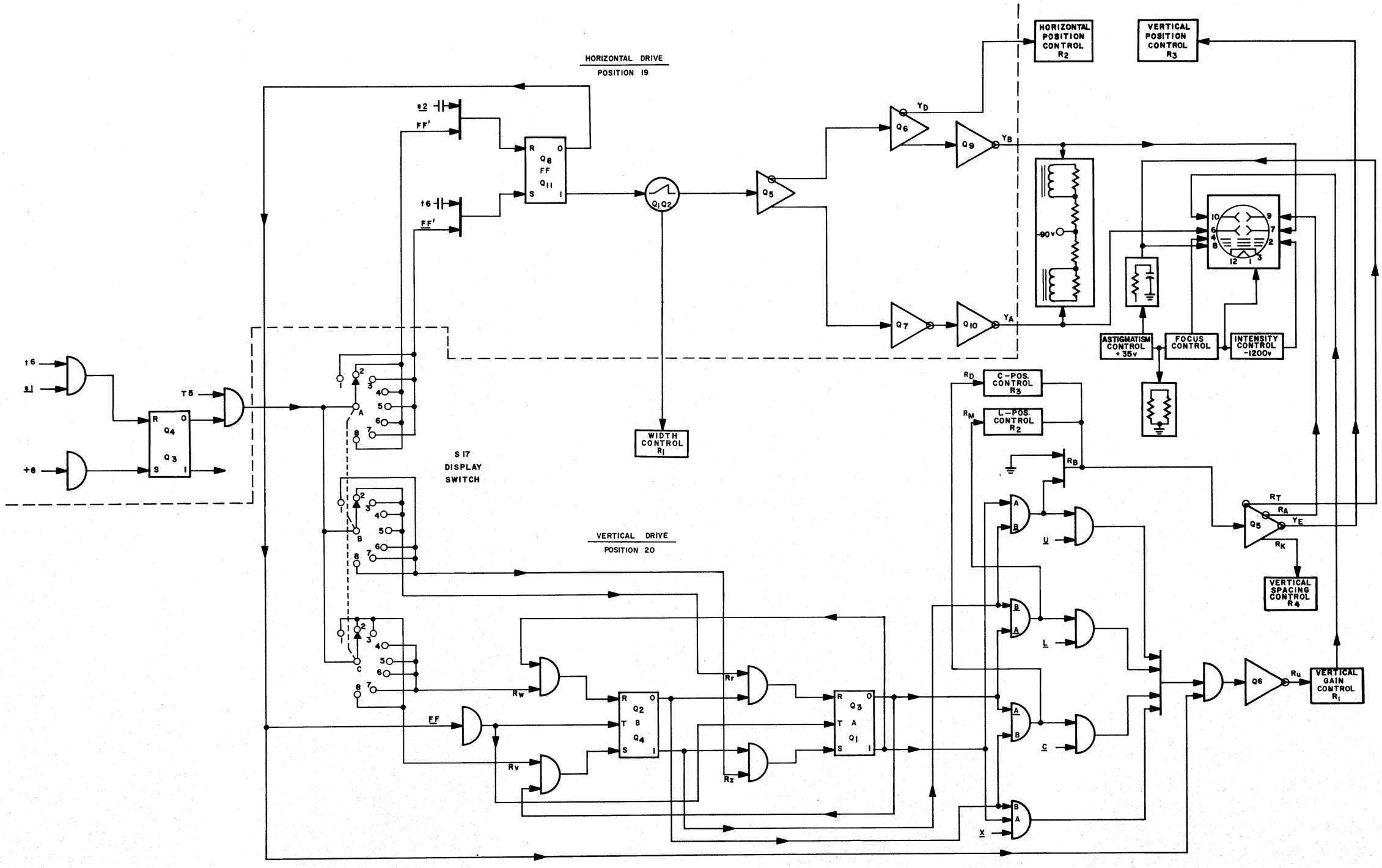

POWER CONTROL
SCHEMATIC NO. L 200 002 384
overload
115 VAC INPUT
CONVENIENCE OUTLET
CONVENIENCE OUTLET
CONTROL PANEL
S2 POWER ON
S1 POWER OFF
M1 ELAPSED TIME METER
PART OF S1
TIME DELAY RELAY 90-120 SEC.
115 VAC COMMON
115 VAC
B1 FAN MOTOR
TO P21-D POWER DIST. CARD
BRYANT DRUM L 200 009 618
TIME DELAY RELAY 90-120 SEC.
C1 .5uFd 330VDC
B1 DRUM MOTOR
POWER SUPPLY SCHEMATIC NO. L 200 009 535
-1200 V
TO POWER CONTROL
-90V
TO VERT. DRIVE CARD
115 VAC COM.
POWER DIST. CARD (P21)
GRD
+35V
-40V
-5V
+12V
-15V
CHASSIS GRD
TO J68-K
TO J71-B
TO J70-G
TO J7-U
TO J66-6
TO J1-U
TO J65-D
TO J28-U
TO J43-U
TO J41-U
TO J61-X
TO J63-6
TO J40-e2
TO J71-V
TO J11-H
TO J40-c2
TO J1-F
TO J28-F
TO J41-F
TO J43-F
TO J40-U2
TO J73-V
3-W
TO J28-W
TO J41-W
TO J1-W
TO J1-D
TO J28-D
TO J41-D
TO J42-D
TO J60-e2
Re TO J1-h RECORD POWER
TO AMP CARD
TOP RACK
MIDDLE RACK
BOTTOM RACK
CONTROL PANEL
J 73
COL 0
COL 1
Rel
Re 0
TO COMPUTE LAMP, CONTROL PANEL
TO STOP LAMP, CONTROL PANEL
TO BRANCH CONTROL LAMP, CONTROL PANEL
6.3 VAC, TO CONTROL PANEL LAMPS
TO POWER ON LAMP, CONTROL PANEL
TO AMPLIFIER CARD
PART OF CONTROL PANEL
DIGITAL DISPLAY TUBE 3W P1
6.3 VAC
PART OF POWER CONTROL L200 002 384
PART OF S1

CLOCK READ AMPLIFIER POSITION 41

CLOCK GENERATOR POSITION 42




S1-S2-S3 TIMING TRACKS
READ AMP. CARDS
T1
S1
Q8
Q9
Q5
Q7
Q10
Q6
T1
S Q2 1
Q3
R 0
Q1
Q4
s1
POSITION 45
S2
POSITION 44
S3
POSITION 43
TRIPLE FLIP-FLOP CARD
POSITION 28
s1R
s2R
s3R
Q2
Q1
Q6
Q5
Q10
Q9
Q12
Q11
S1
S2
S3
HORIZONTAL CARD POSITION 19
ℓ84
S20
p87
H84
L85
S73
H80
r71
LOGIC BOARD
U81
D97
U82
L81


HORIZONTAL DRIVE
POSITION 19
VERTICAL DRIVE
POSITION 20
S 17
DISPLAY
SWITCH
HORIZONTAL POSITION CONTROL R2
VERTICAL POSITION CONTROL R3
WIDTH CONTROL R1
ASTIGMATISM CONTROL +35v
FOCUS CONTROL
INTENSITY CONTROL -1200v
C-POS. CONTROL R3
L-POS. CONTROL R2
VERTICAL SPACING CONTROL R4
VERTICAL GAIN CONTROL R1
+90v
Q1 Q2
Q5
Q6
Q7
Q9
Q10
Q11
Q2
Q3
Q4
Q5
Q6
YD
YB
YA
YE
RT
RA
RK
Ru
RB
RD
RM
RW
Rr
Rv
Rz
FF
T5
+6
+1
+2
+6
U
L
C
X

"D" READ AMPLIFIER CARD POSITION 47 TRK 127

READ-BACK SIGNAL

D

T1

Q8 Q9 Q5 Q7 Q10 Q6

T1

S I Q2 Q3 R O

Q1 d

Q4 d

NOT USED

TRIPLE FLIP FLOP CARD (TYP)

POSITION 29,30,31

VERTICAL CARD POSITION 20

C L U

	y96
	y93
	p35
u	y90
X	M99
C	H94
L*	K83
L	NN88
U*	K42
U	TT95
X	D88
C	y75
L*	AA35
L	AA32
U*	p32
U	XX81
	AA11

LOGIC BOARD

M100 X'

y80 C'

TT91 L'

AA92 U'

READ AMPLIFIER CARD (TYP.) POSITION 46,48,49,50,51,52

READ-BACK SIGNALS

X C L U

T1

Q8 Q9 Q5 Q7 Q10 Q6

T1

S I Q2 Q3 R O

Q1

Q4

NOT USED

X C L U

T1

S I Q4 Q6 R O

Q2 Q7 Q3 Q5

T2

Q1

-15 v

C.T.

D

RECORD SIGNAL

"D" RECORD AMPLIFIER CARD POSITION 2

RECORD AMPLIFIER CARD (TYP) POSITION 1,3,4,5

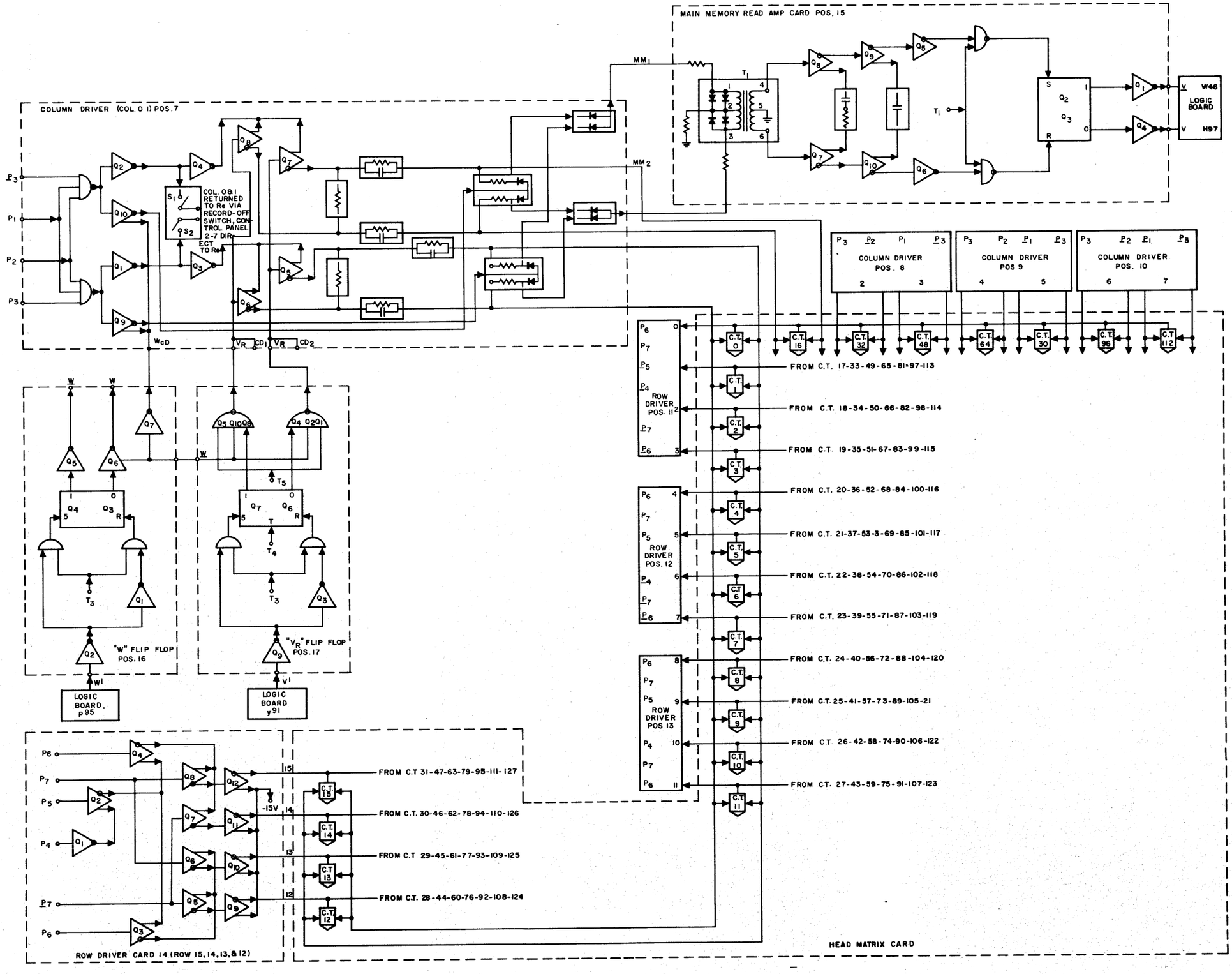
-15 v

C.T.

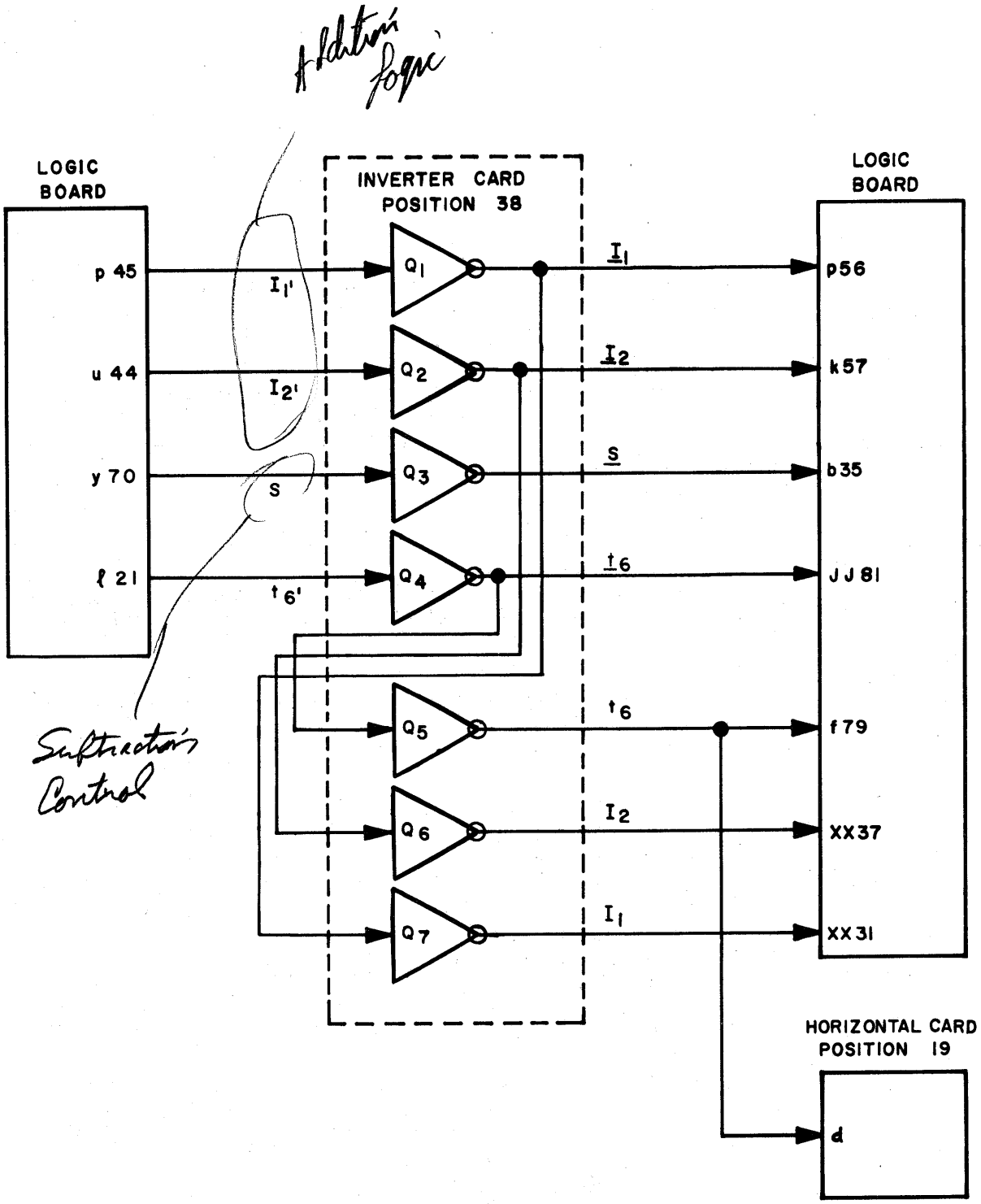
X C L U

RECORD SIGNALS

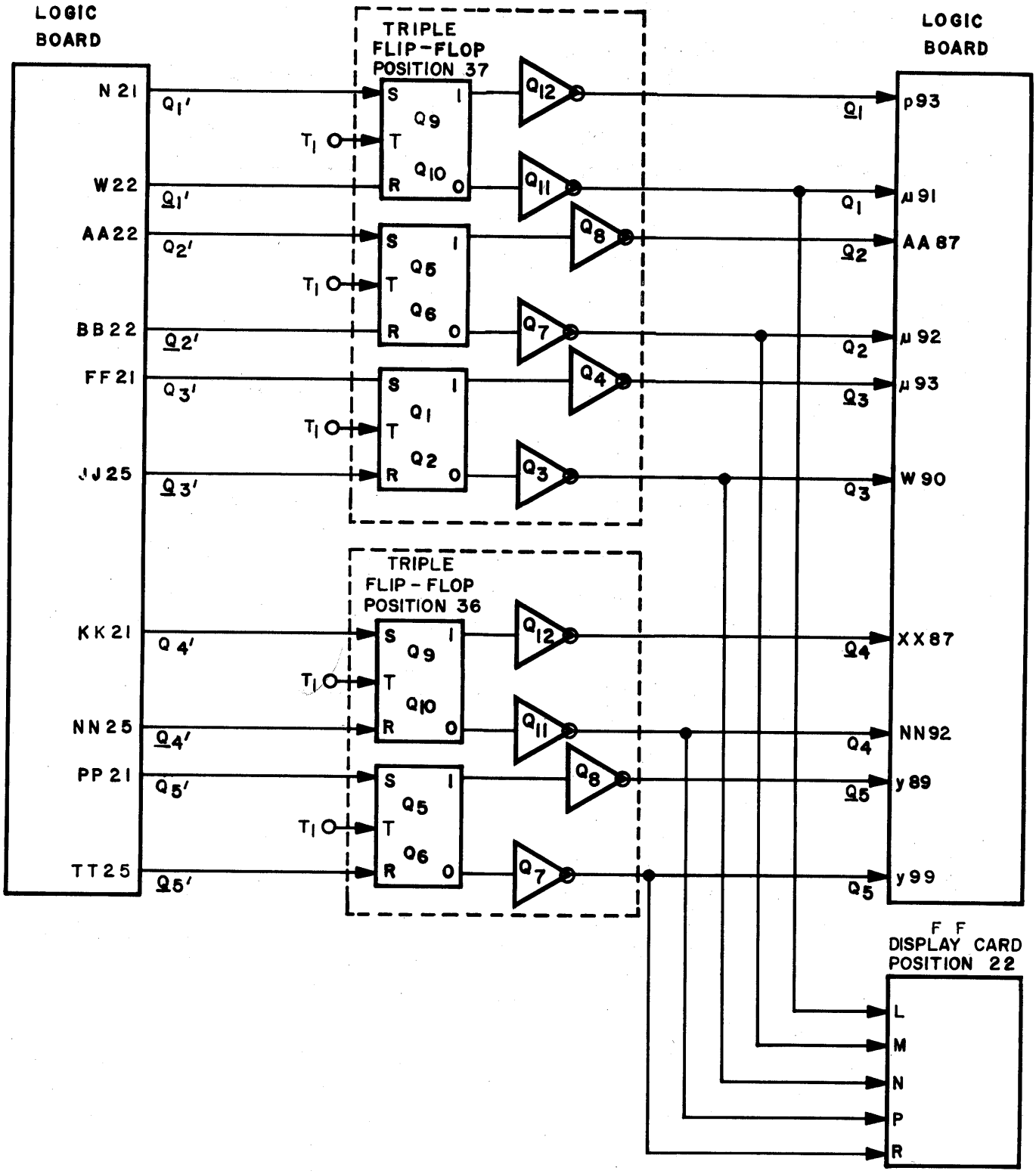
CIRCULATING LINES

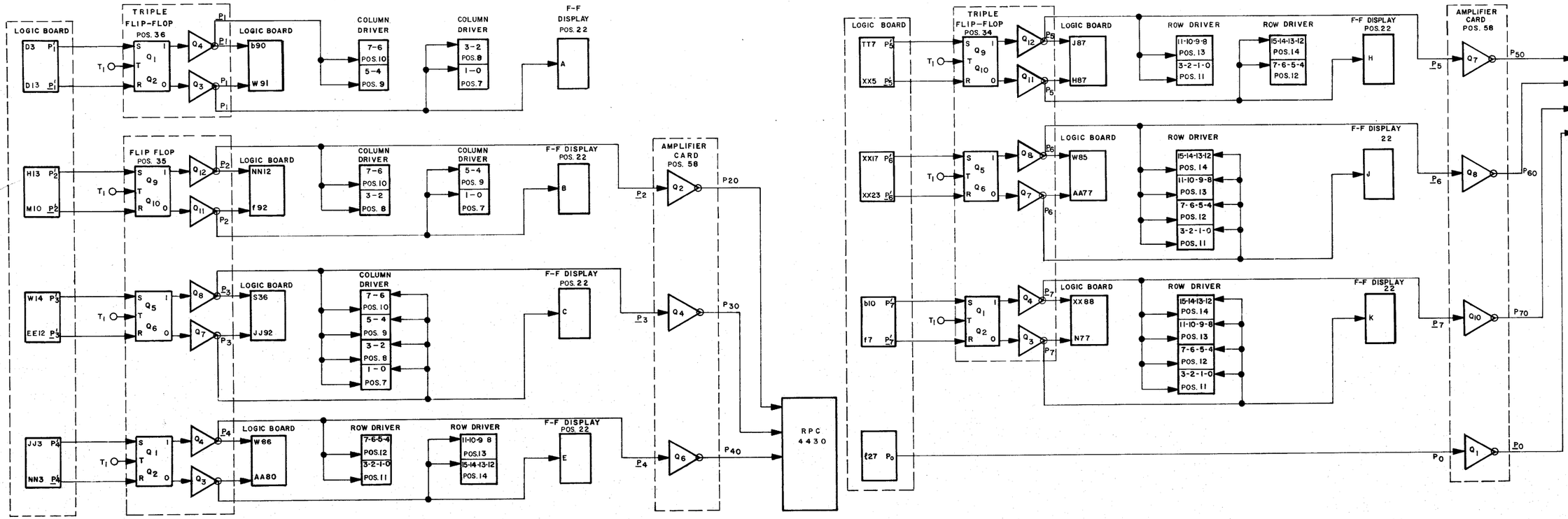


HEAD MATRIX SELECTION

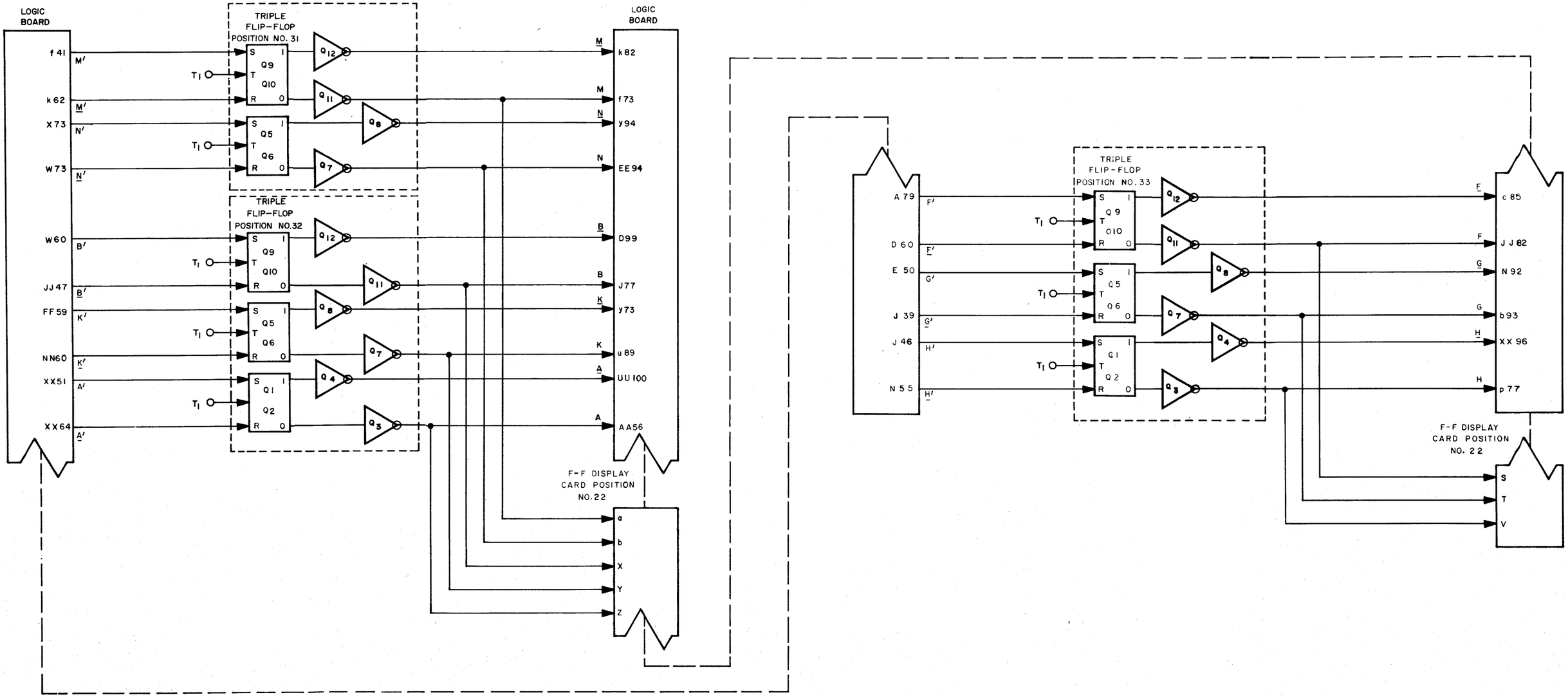


INVERTER CARD


LOGIC BOARD
N 21
W 22
AA 22
BB 22
FF 21
JJ 25
KK 21
NN 25
PP 21
TT 25
TRIPLE FLIP-FLOP POSITION 37
TRIPLE FLIP-FLOP POSITION 36
LOGIC BOARD
p 93
μ 91
AA 87
μ 92
μ 93
W 90
XX 87
NN 92
y 89
y 99
F F DISPLAY CARD POSITION 22
L
M
N
P
R



P_1, P_2, P_3, P_4, P_5, P_6, P_7 FLIP-FLOPS



M, N, B, K, A, F, G, H SIGNALS

DRAWING 10

A3-23

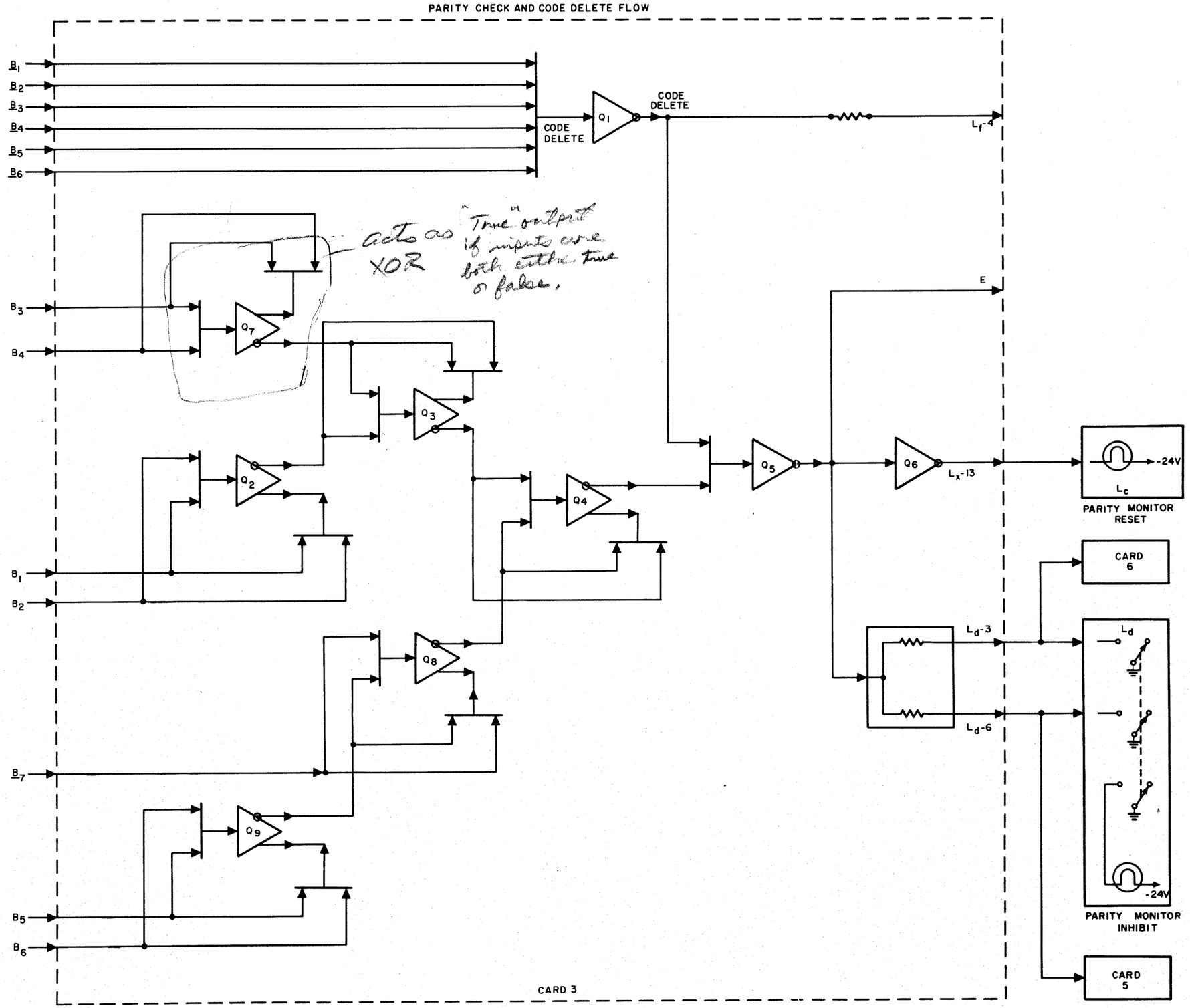
APPENDIX 3

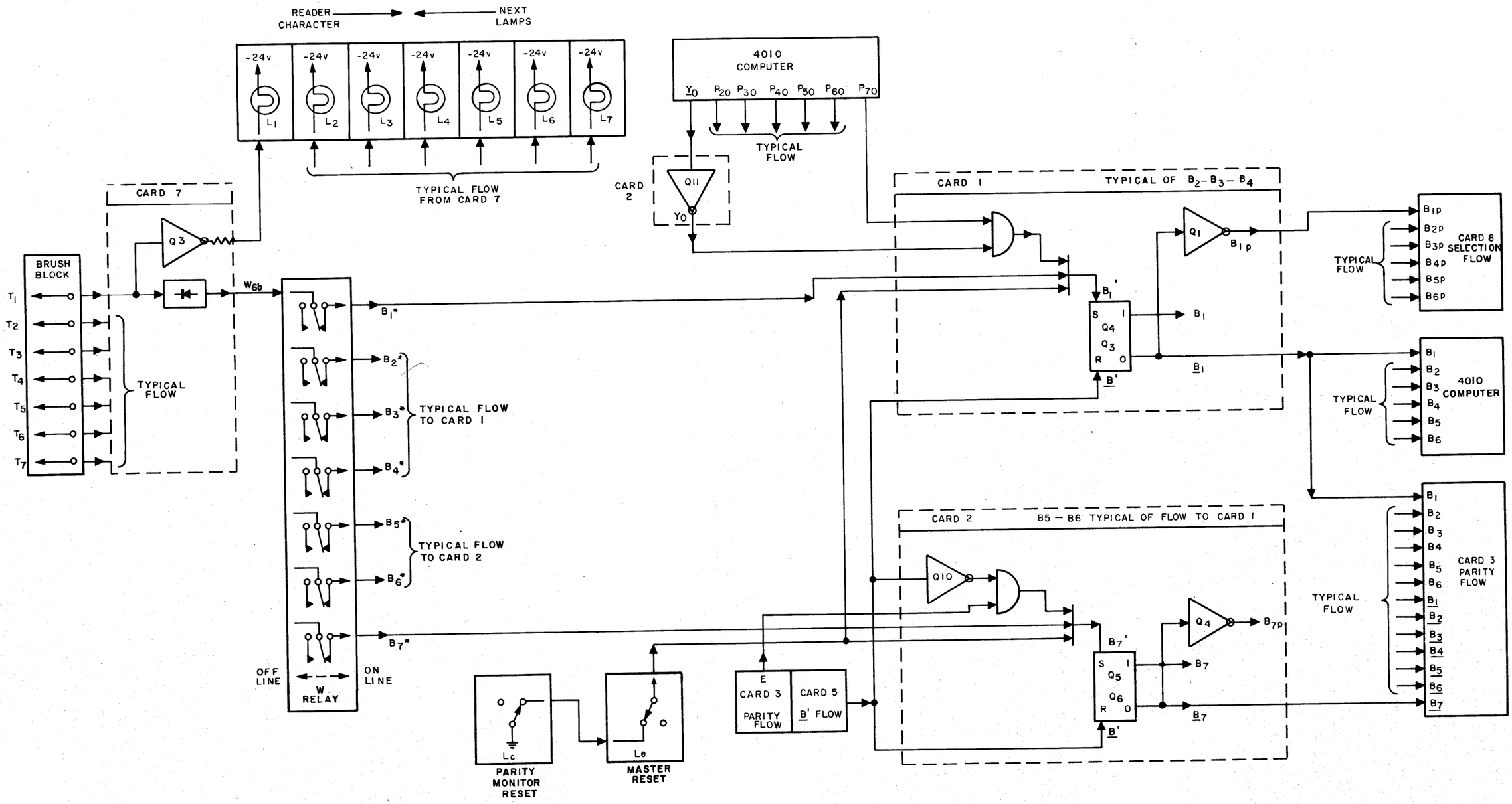
RPC-4000 SYSTEM SCHEMATICS

PART II

~~CENTRAL COMPUTER~~
INPUT-OUTPUT (ON-LINE)

PARITY CHECK AND CODE DELETE FLOW





SETTING B FLIP-FLOPS

DRAWING 12

4010 COMPUTER Yi

Start Input Device

Start Compute

REFER TO SIGNALS TO COMPUTER FLOW CHART Zs

SINGLE CHARACTER MODE Lb

Zb

STOP READ Ll

CARD 5

-24v

Lb3

Ll-1

Read Mode

S I R O Ic

-24v

Lh

START READ

READER TO COMPUTER Ln

Im

OFF LINE ON

W RELAY

READER CLUTCH DRIVE CAM

R•3

M B

210° 45°

N/C

READER CLUTCH SOLENOID

-24v

ON OFF

K2 AC RELAY

B5p B4p B3p B6p

Q3

S

Q4

-24v

d/dt Lv LEADING

I Qr O Qr

CARD 8

Q6

Q7

Qr

Lv8

Q5

BRUSH INTERRO-GATE CAM

M B

15° 45°

195° 225°

Rel

N/O

-24v

CARD 5

Q6

Q7

B'

S

Le-4

Le

S5 MASTER RESET

Yo Po

4010 COMPUTER

-24v

MECHANICAL PAWL DELAY

DRIVE

BEGINS STOPS

45° 190°

225° 360°

ROLLER

COMMON CONTACT

B*

Ic

Q4

Ac'

Instantly Ready Signal

S I Q2 Q1 R O Ac

Ac

Q3

Ap

Input Request

LEADING d/dt B*

CARD 6

Non-Ready Query (Selected unit Ready)

Zq

REFER TO SIGNALS TO COMPUTER FLOW CHART

A3-33

B* OR H*

ONE SLOT

S Q1 Q2 R I O

CARD 7

Am

OFF LINE ON LINE

VII RELAY

ON LINE Ap Am

Lv

OFF LINE

READER SELECT

REFER TO SIGNAL V8v ON CARD 16 OFF LINE TYPEWRITER PUNCH SELECT FLOW CHART

OFF LINE ON LINE

W RELAY

B*

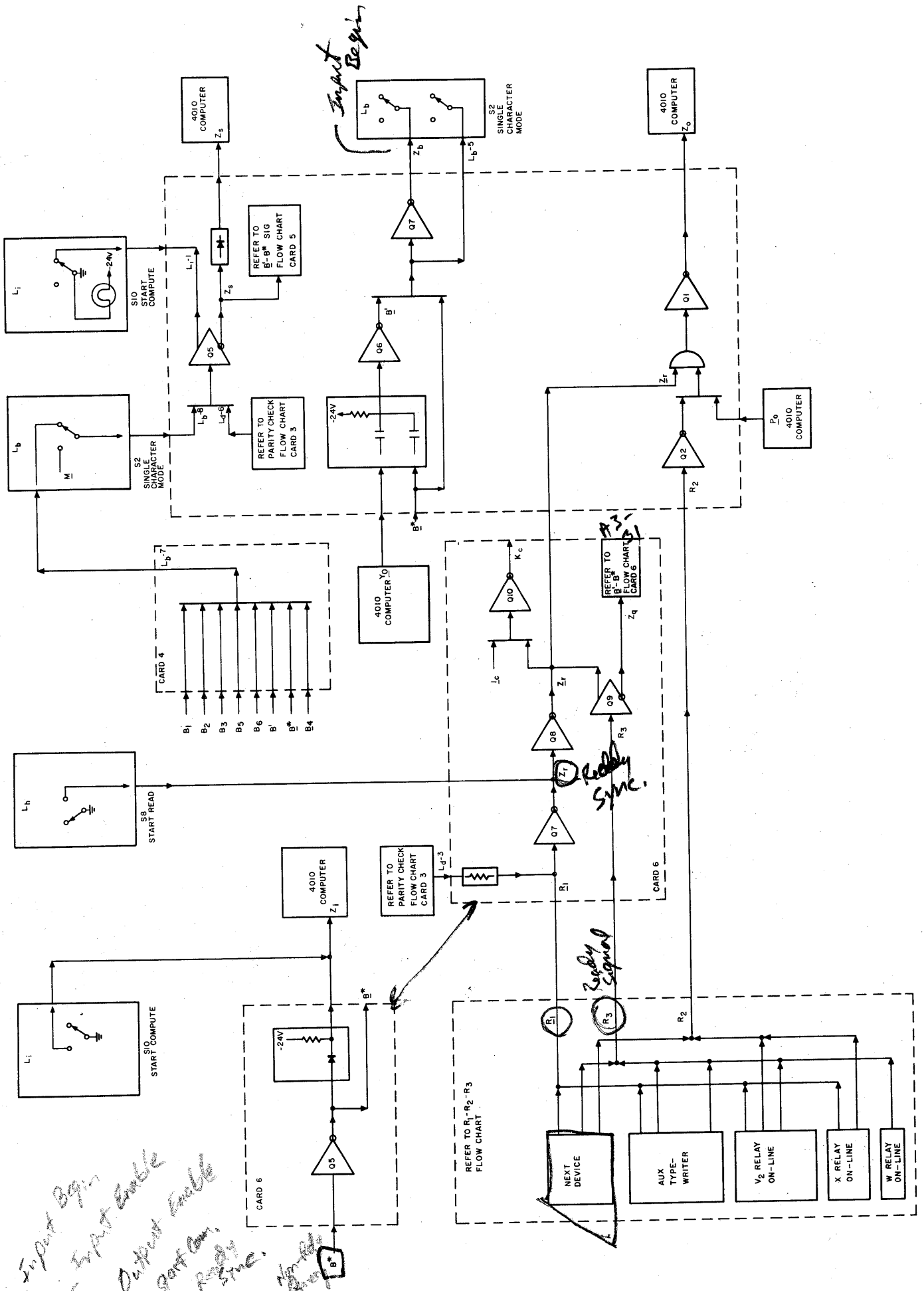
CARD 6

Q5

B*

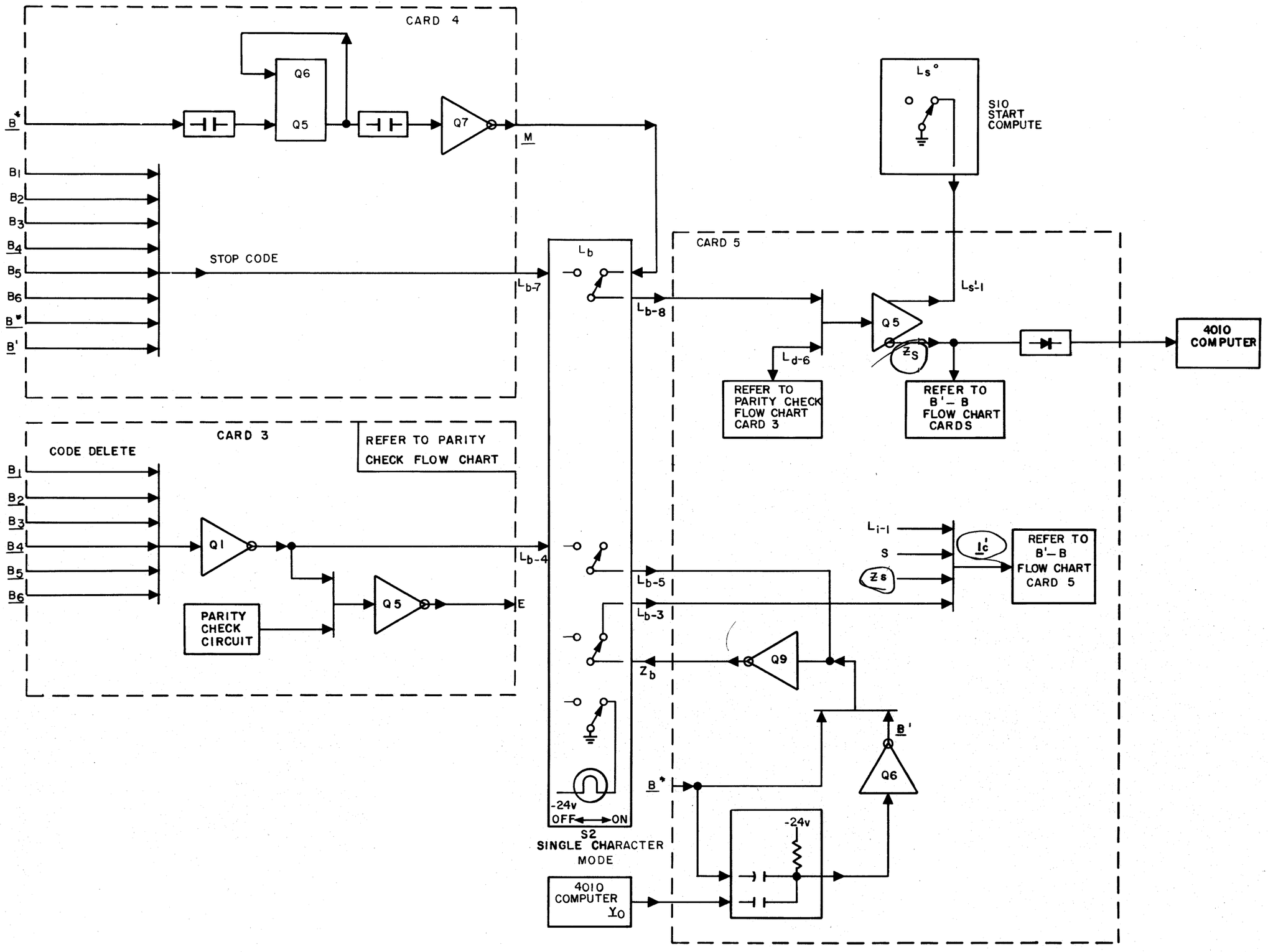
B' AND B* SIGNALS

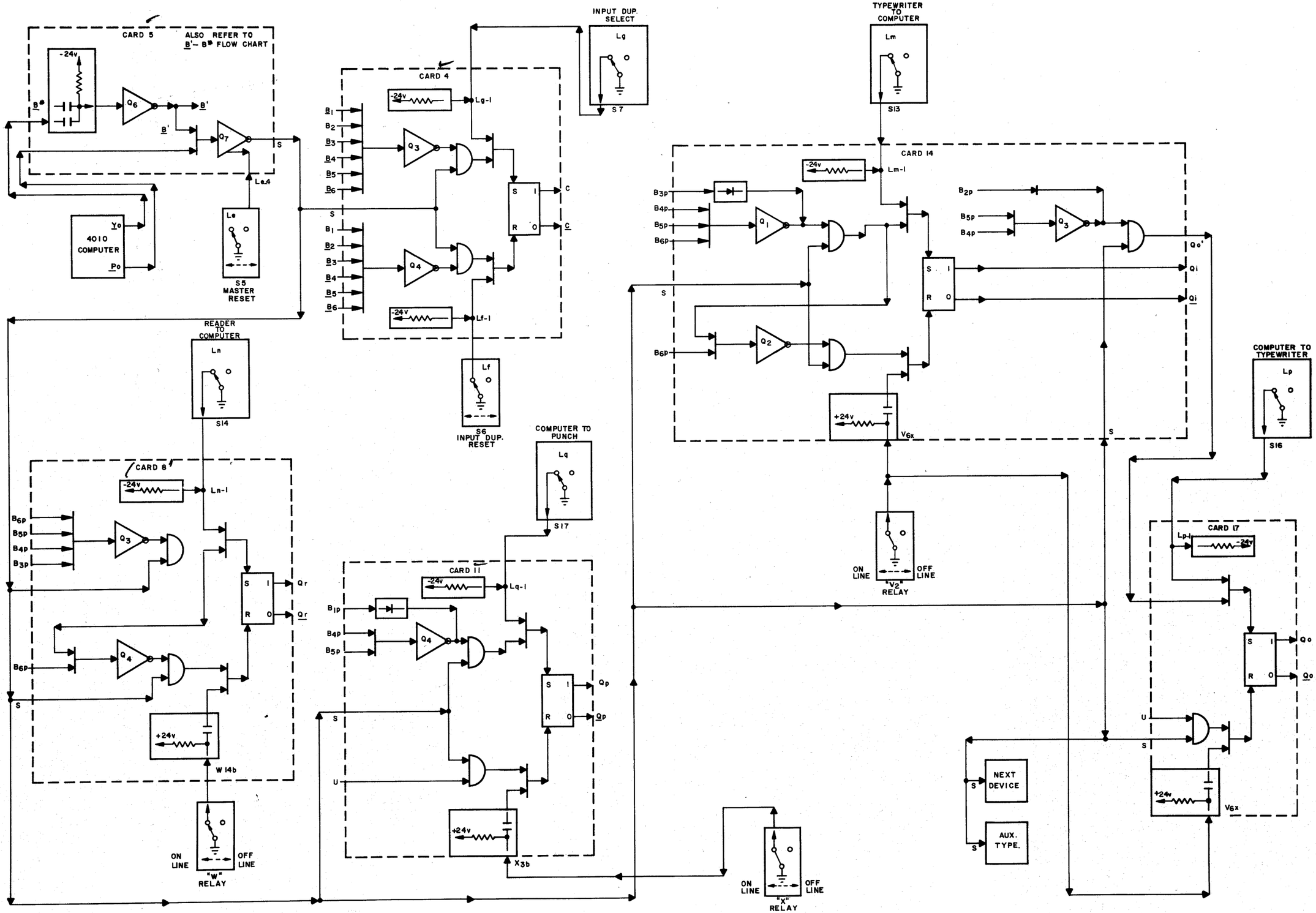
DRAWING 13 A3-31



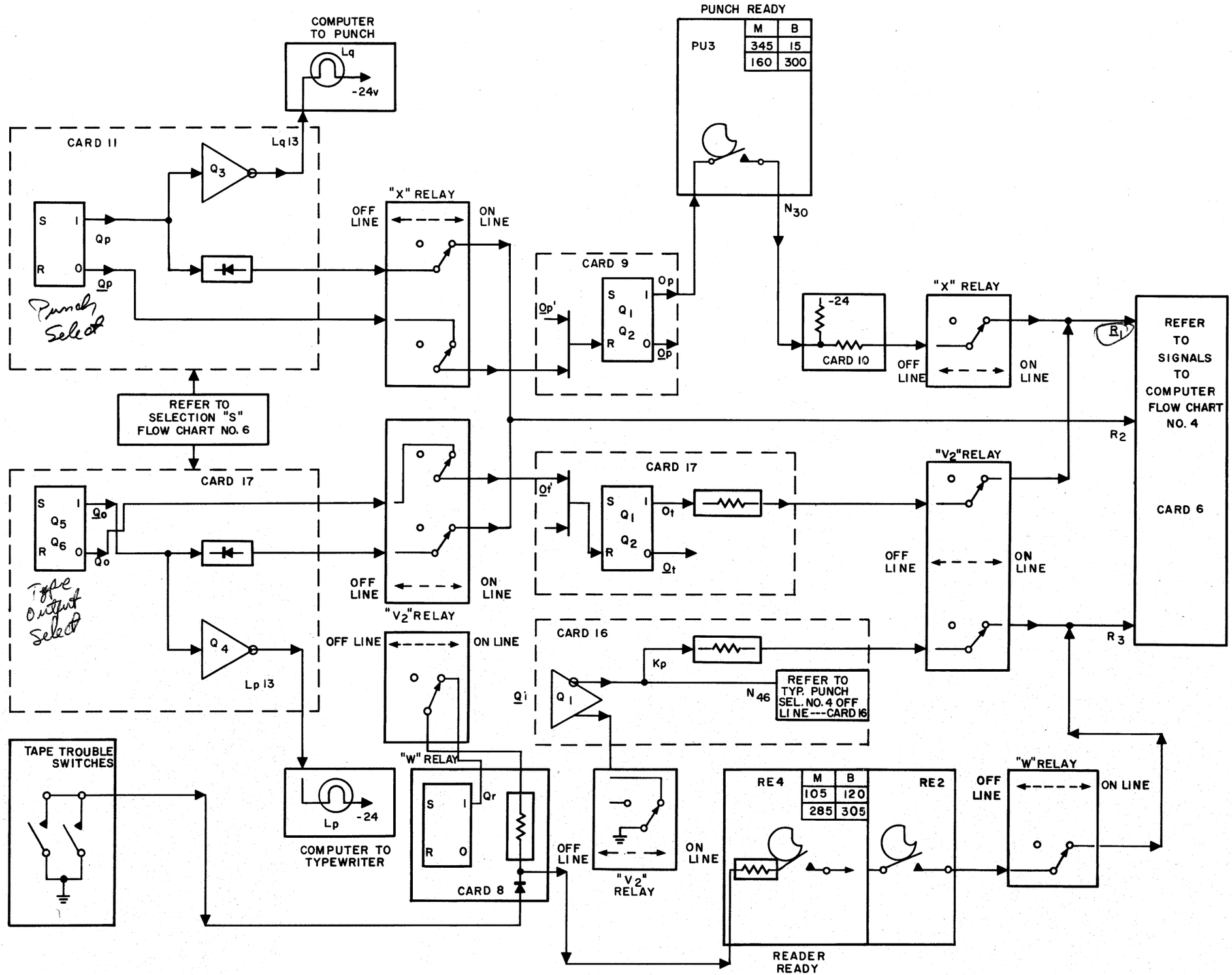
Z_b, Z_i, Z_o, Z_s, Z_r, $\underline{Z}_r$, $\underline{Z}_q$ - SIGNALS TO COMPUTER

DRAWING 14

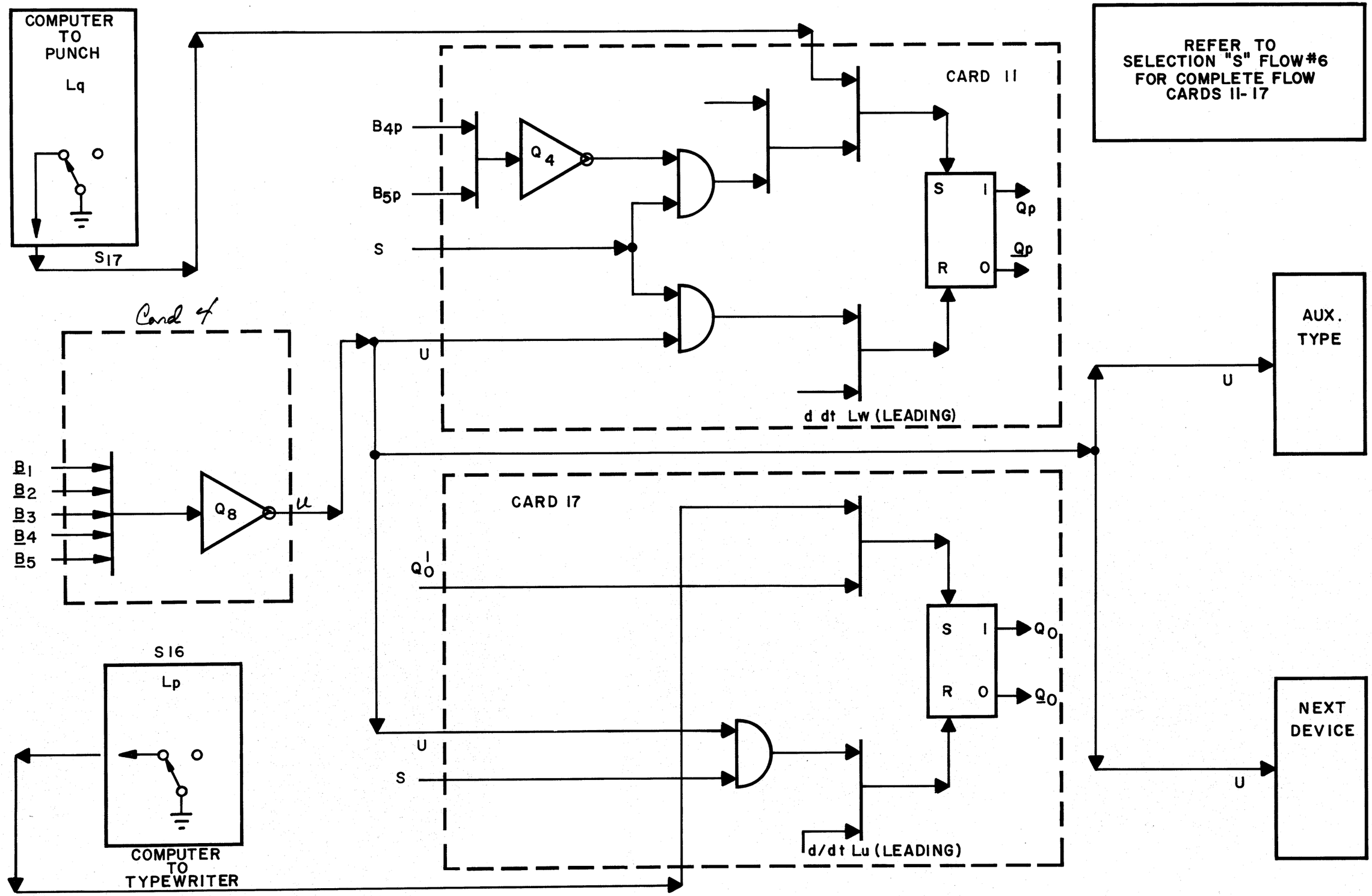

CARD 4
Q6
Q5
Q7
B*
M
B1
B2
B3
B4
B5
B6
B*
B'
STOP CODE
Lb-7
Lb
Lb-8
Ls°
SIO
START
COMPUTE
CARD 5
Ls'-1
Q5
Zs
Ld-6
4010
COMPUTER
REFER TO
PARITY CHECK
FLOW CHART
CARD 3
REFER TO
B'— B
FLOW CHART
CARDS
CARD 3
CODE DELETE
REFER TO PARITY
CHECK FLOW CHART
B1
B2
B3
B4
B5
B6
Q1
Q5
PARITY
CHECK
CIRCUIT
Lb-4
E
Li-1
S
Zs
Ic'
REFER TO
B'— B
FLOW CHART
CARD 5
Lb-5
Lb-3
Zb
Q9
B'
Q6
B*
-24v
-24v
OFF ON
S2
SINGLE CHARACTER
MODE
4010
COMPUTER
Yo



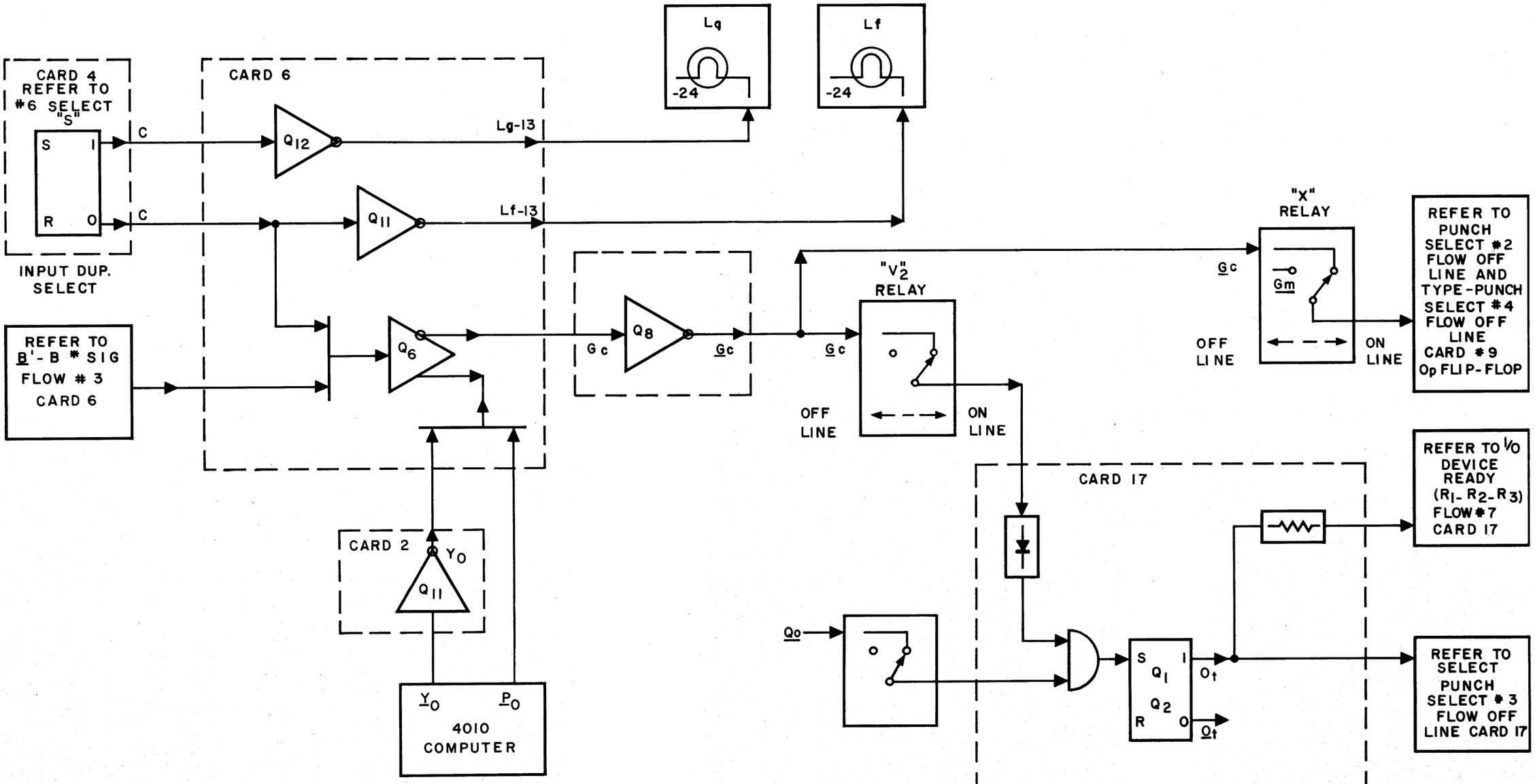
S - SELECTION SIGNAL



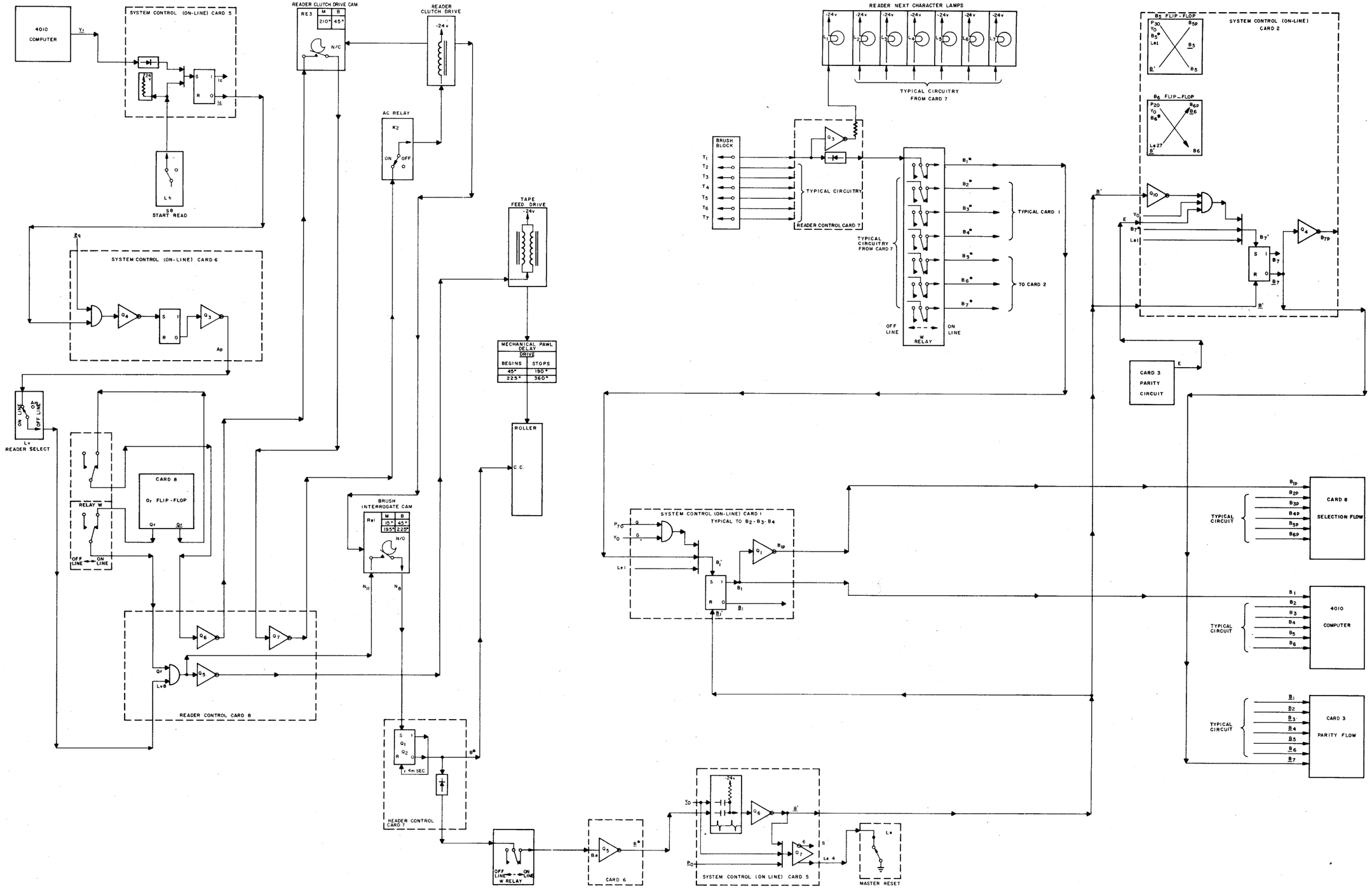
R_1, R_2, R_3 - INPUT-OUTPUT DEVICE READY



U- UNSELECT SIGNAL (MASTER RESET)

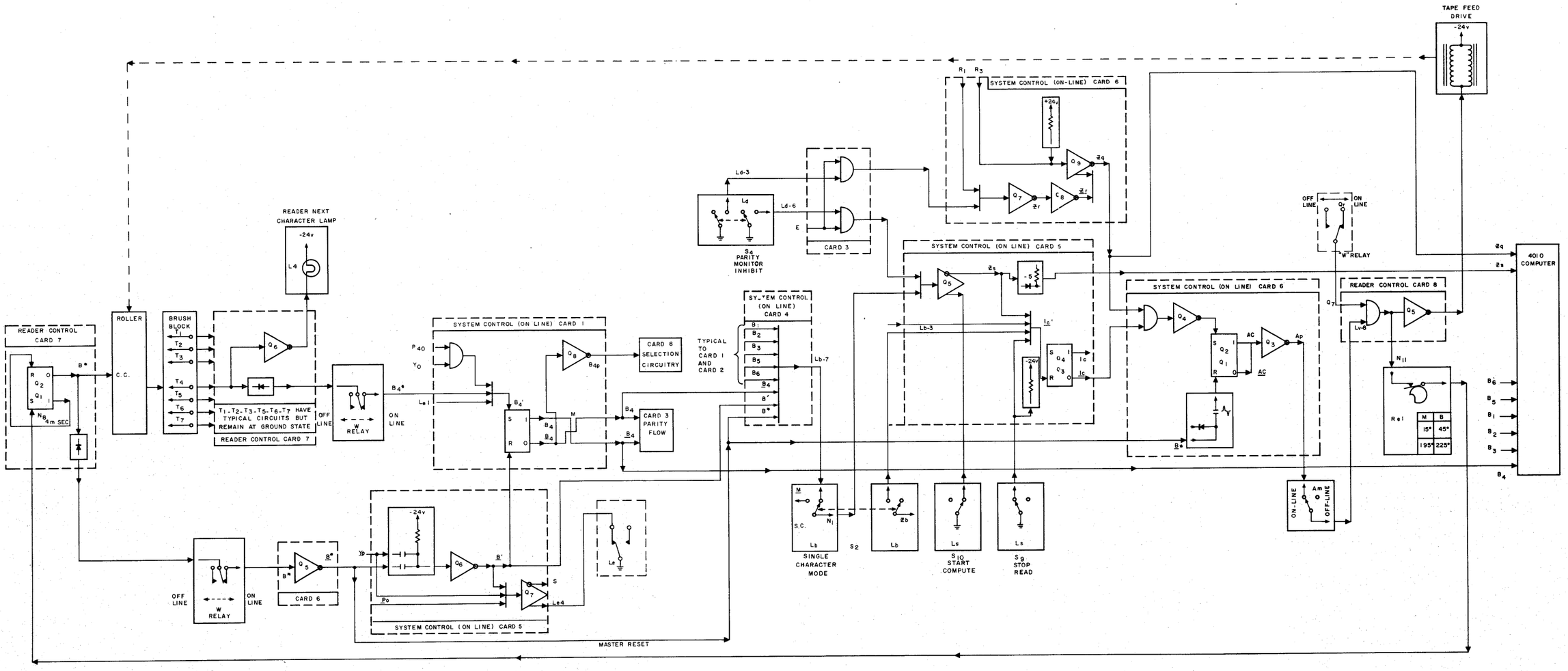


G_c - GO AHEAD SIGNAL



TAPE FEED CHARACTER RECOGNITION

DRAWING 20 A3-45



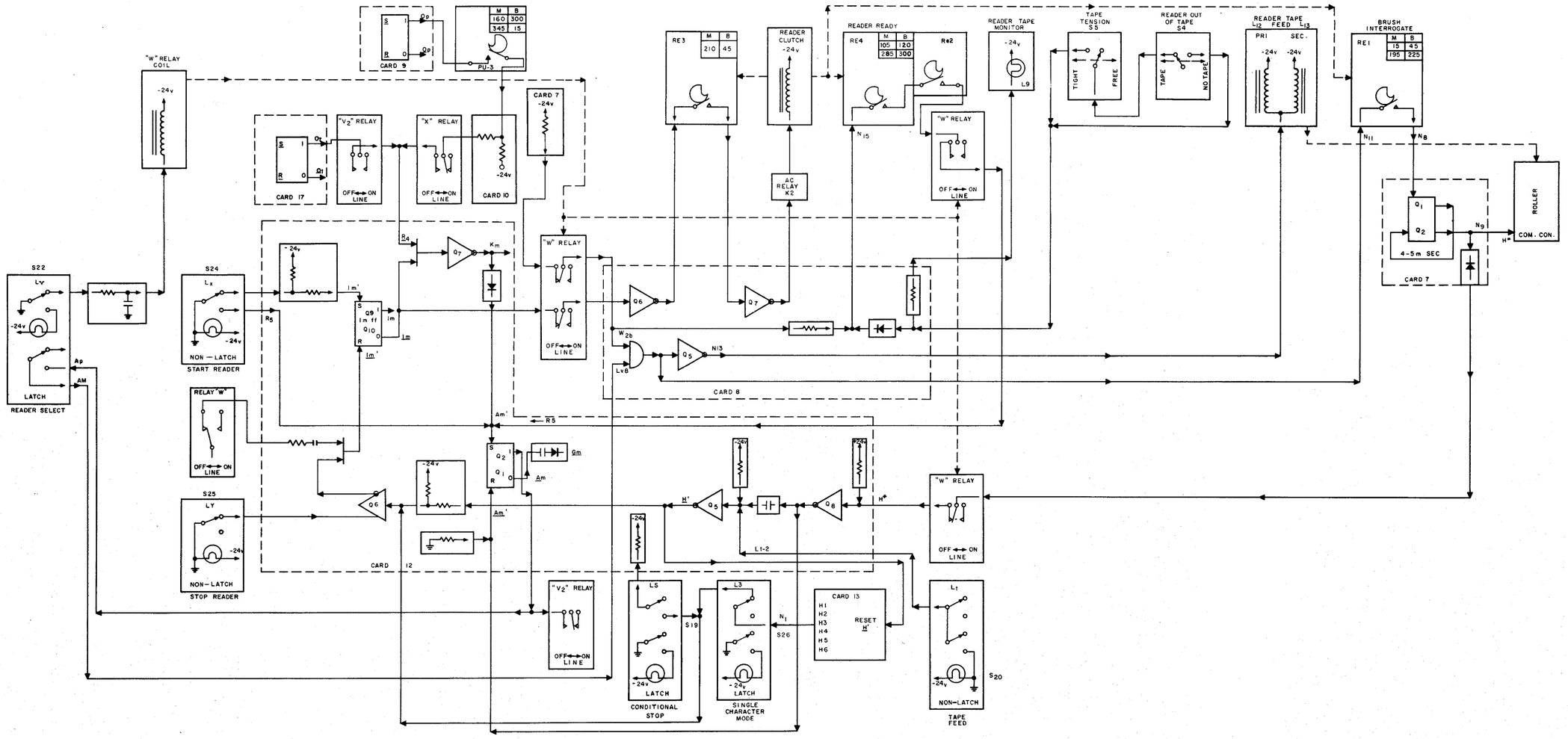
STOP CODE - START SIGNAL

APPENDIX 3

RPC-4000 SYSTEM SCHEMATICS

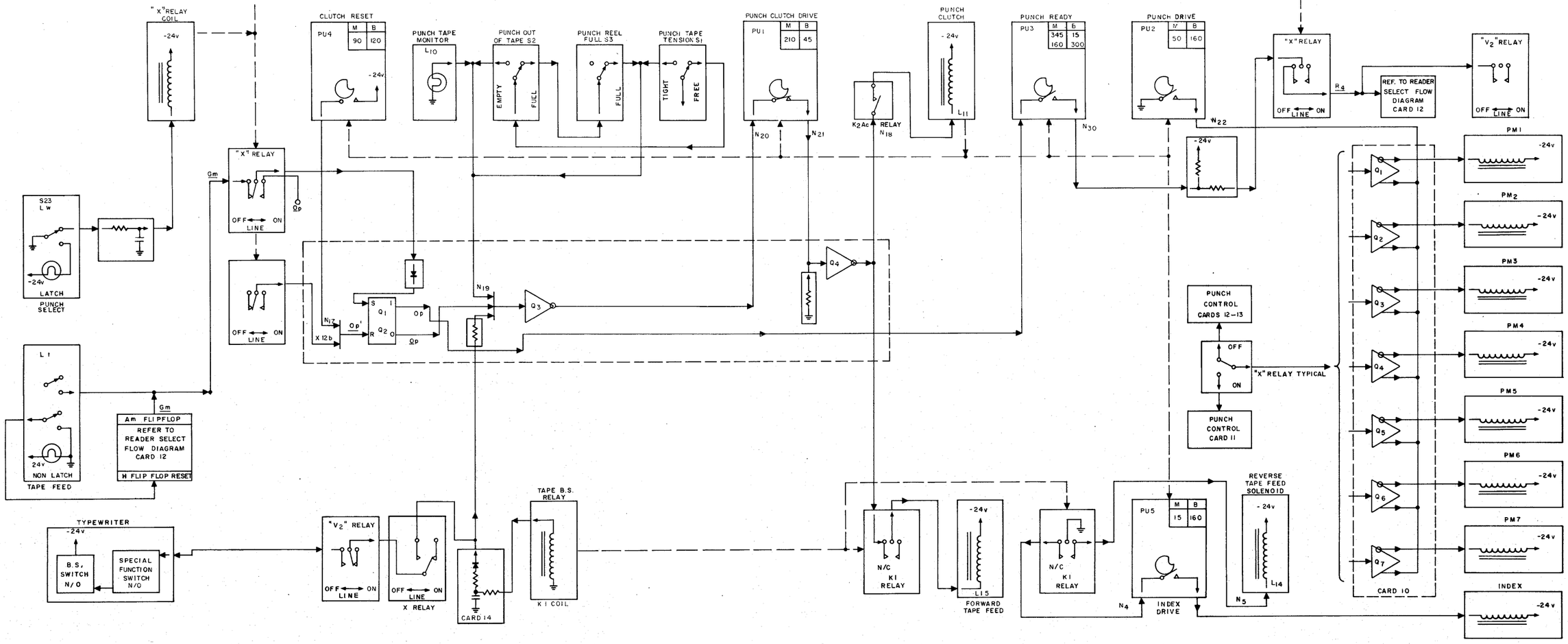
PART III

INPUT-OUTPUT (OFF-LINE)



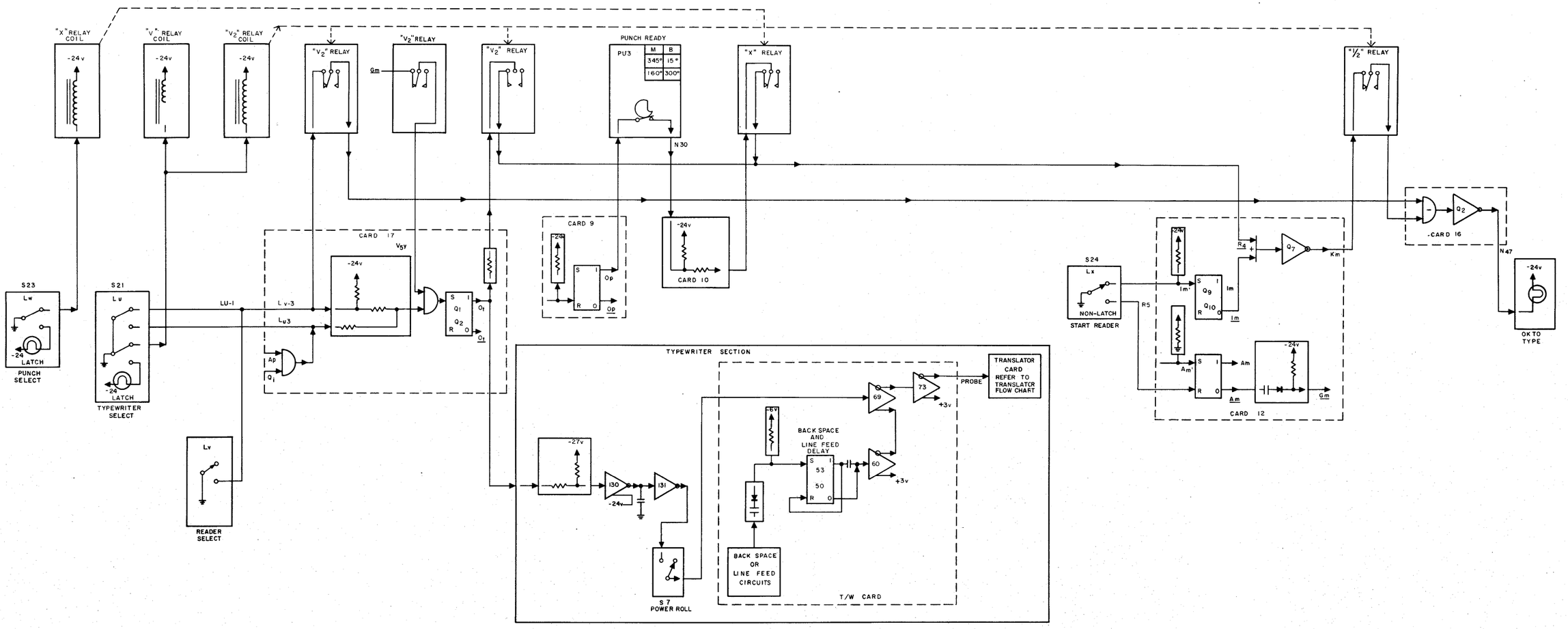
READER SELECT

DRAWING 22 A3-51

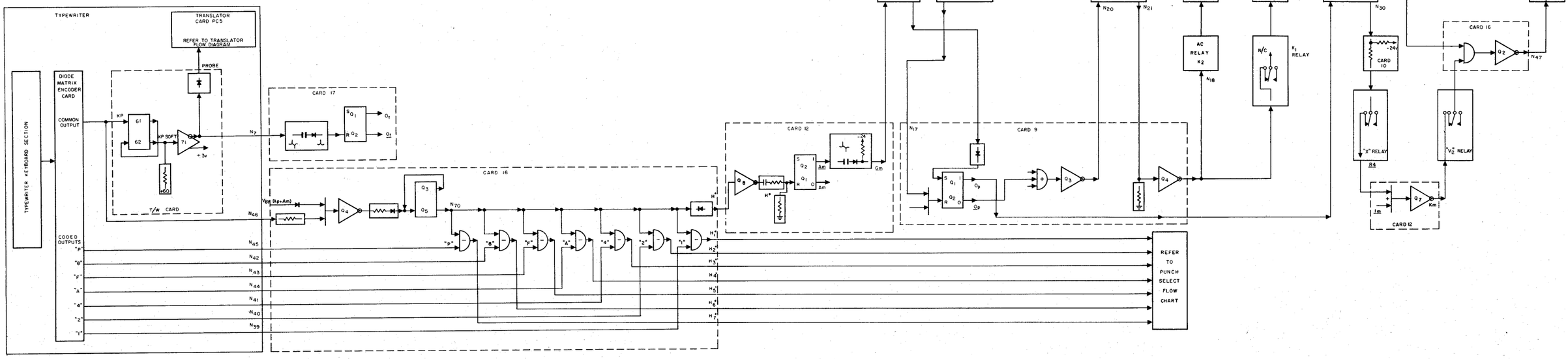


PUNCH SELECT

DRAWING 23 A3-53



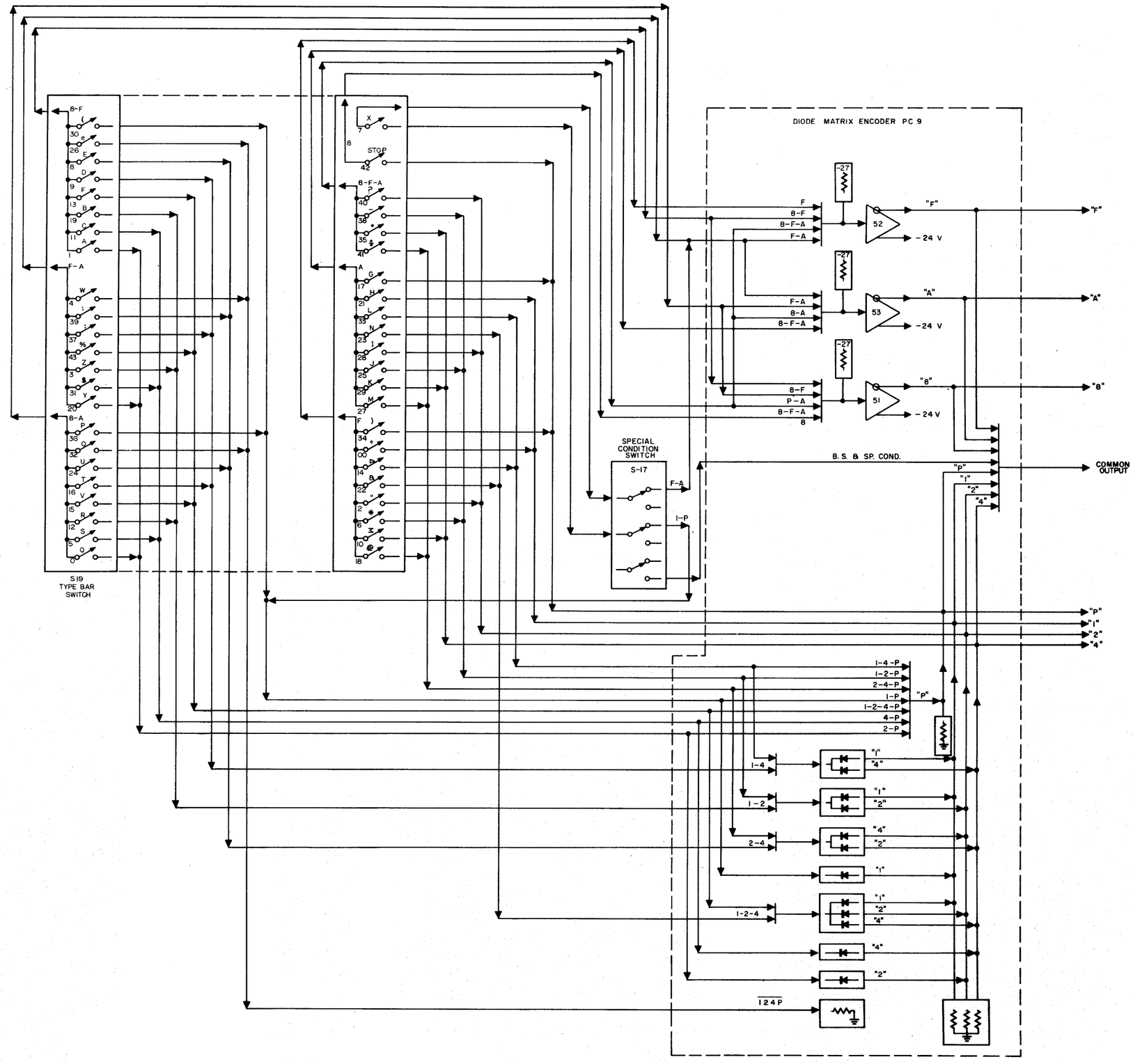
TYPEWRITER SELECT - PUNCH SELECT



TYPEWRITER/PUNCH SELECT

DRAWING 25

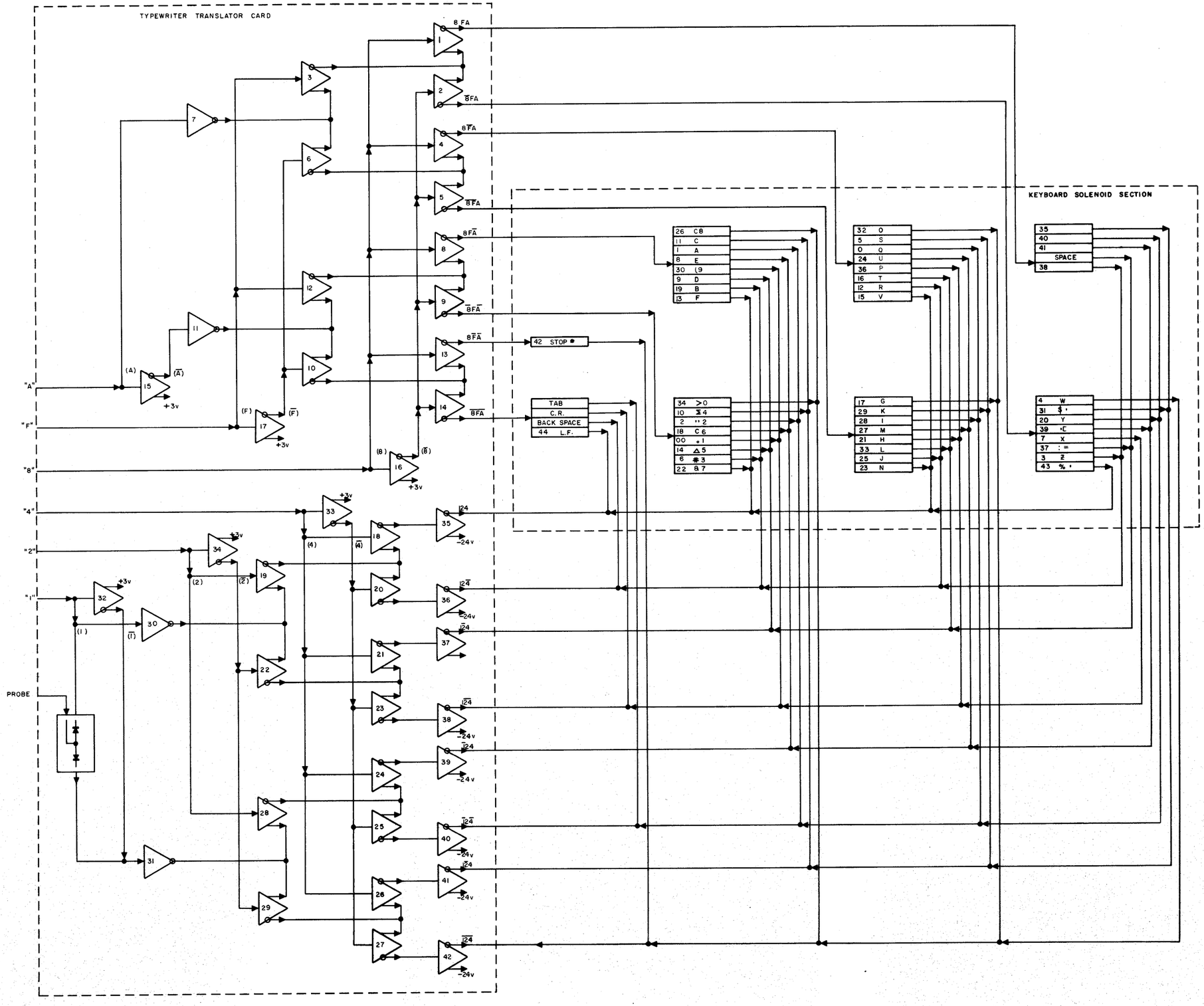
A3-57

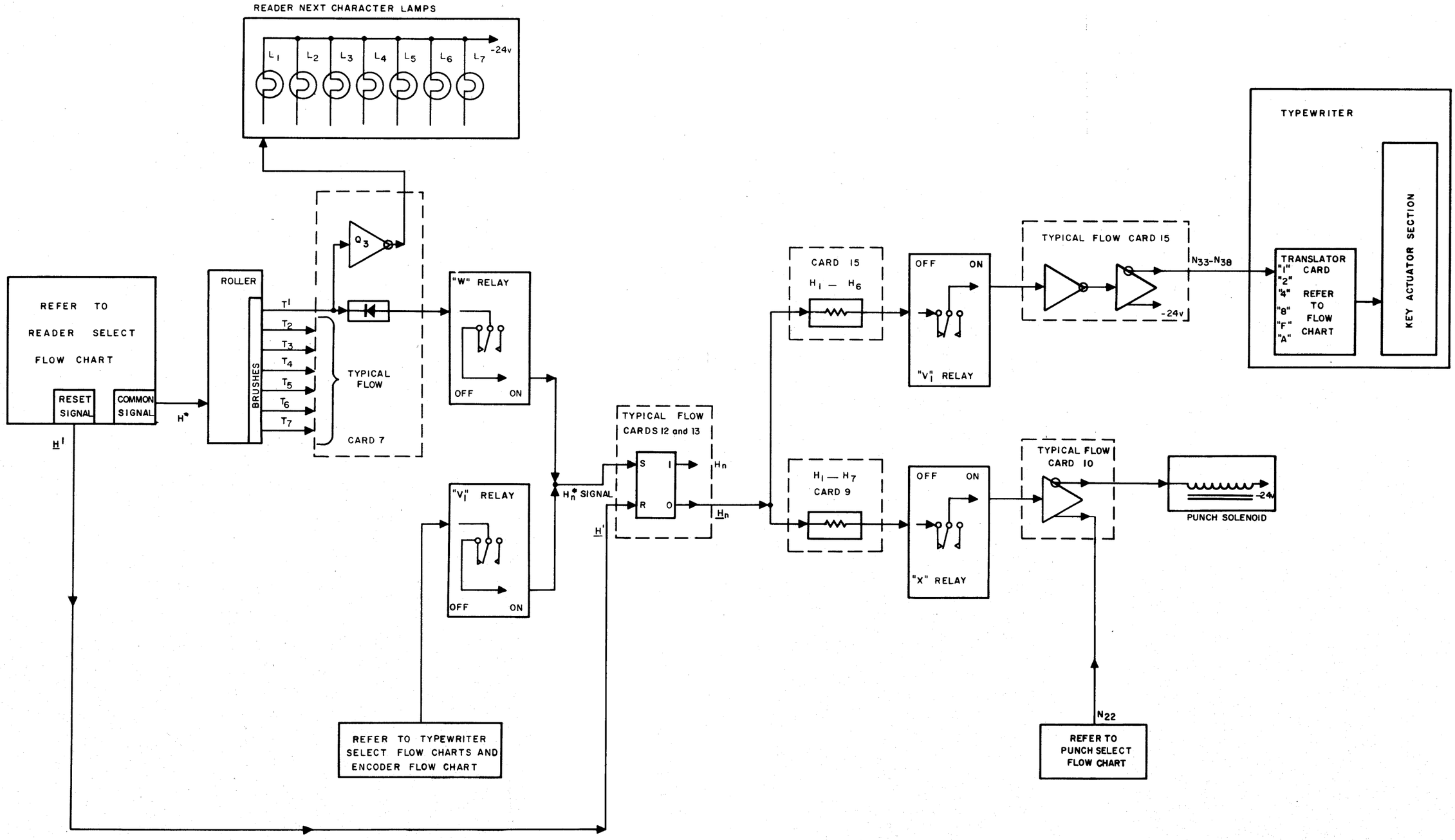


TYPEWRITER KEY-TO-ENCODER FLOW DIAGRAM

DRAWING 26

A3-59


TYPEWRITER TRANSLATOR CARD
KEYBOARD SOLENOID SECTION
"A"
"F"
"8"
"4"
"2"
"1"
PROBE
+3v
-24v
42 STOP *
TAB
C.R.
BACK SPACE
44 L.F.
SPACE
26 C8
11 C
1 A
8 E
30 (9
9 D
19 B
13 F
34 >0
10 Σ4
2 " 2
18 C6
00 ∘1
14 △5
6 #3
22 87
32 0
5 S
0 Q
24 U
36 P
16 T
12 R
15 V
17 G
29 K
28 I
27 M
21 H
33 L
25 J
23 N
35
40
41
38
4 W
31 $ '
20 Y
39 ¢
7 X
37 : =
3 2
43 % '



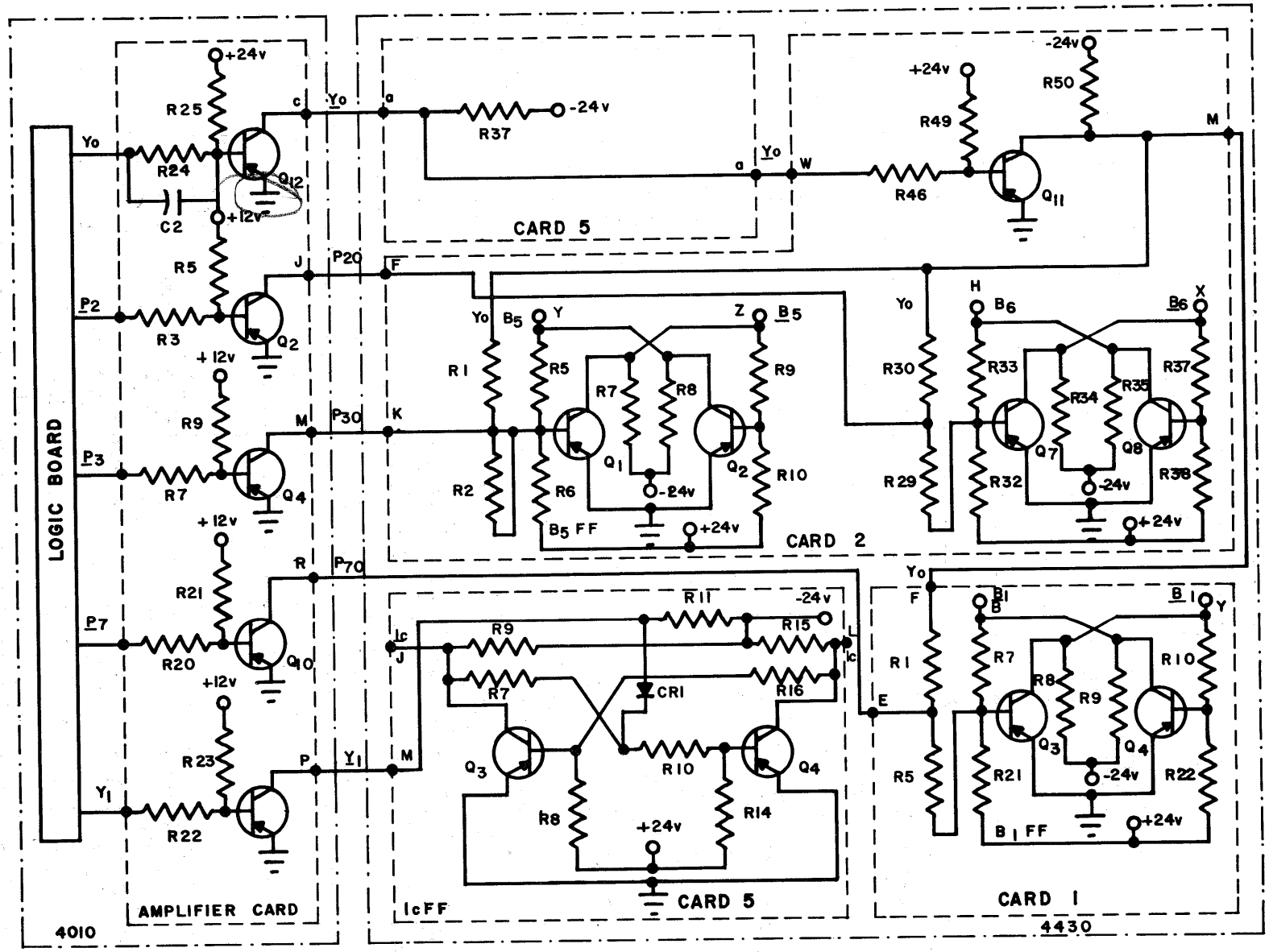
OFF-LINE READER SELECT, PUNCH-TYPEWRITER SELECT FLOW DIAGRAM

APPENDIX 3

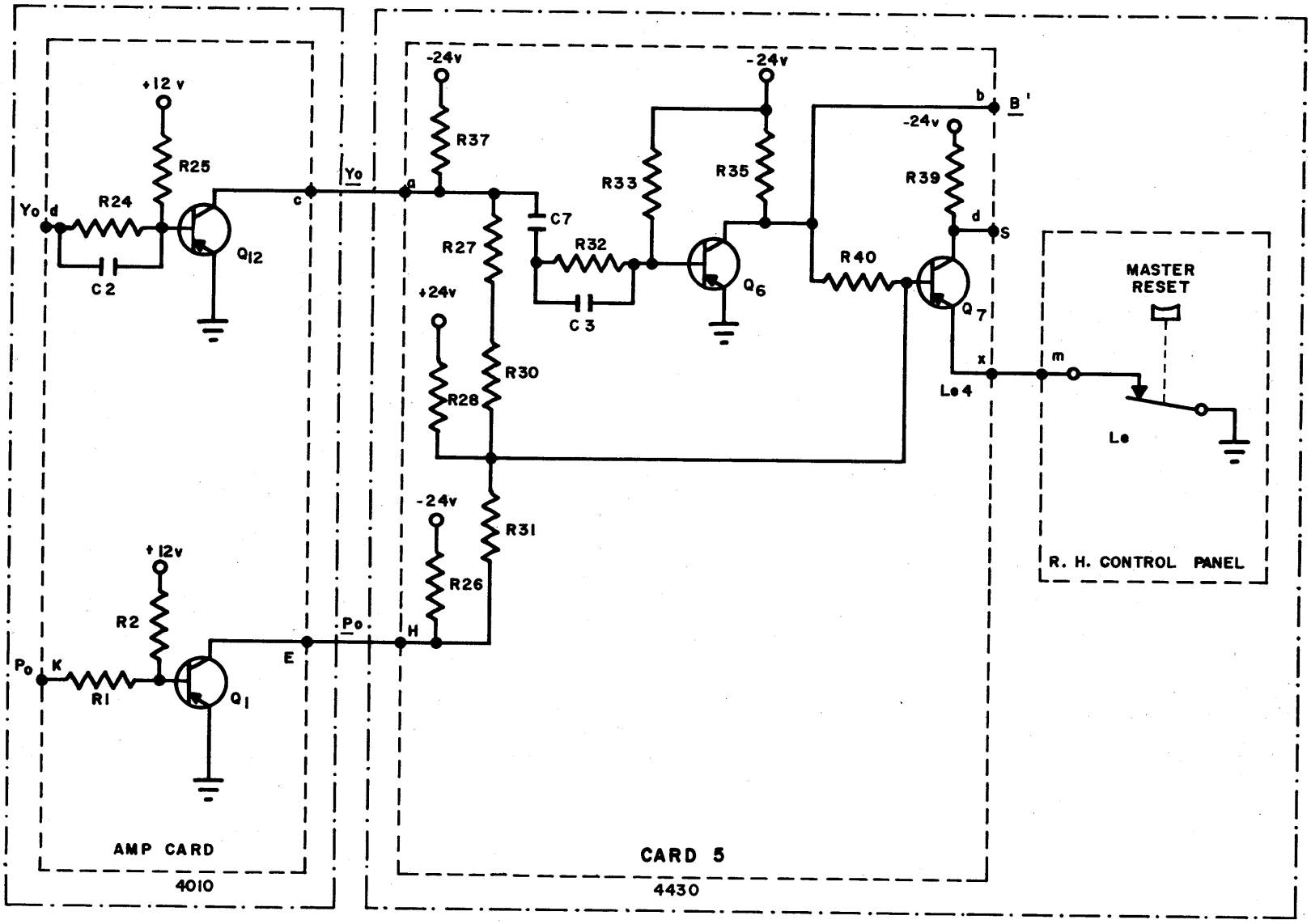
RPC-4000 SYSTEM SCHEMATICS

PART IV

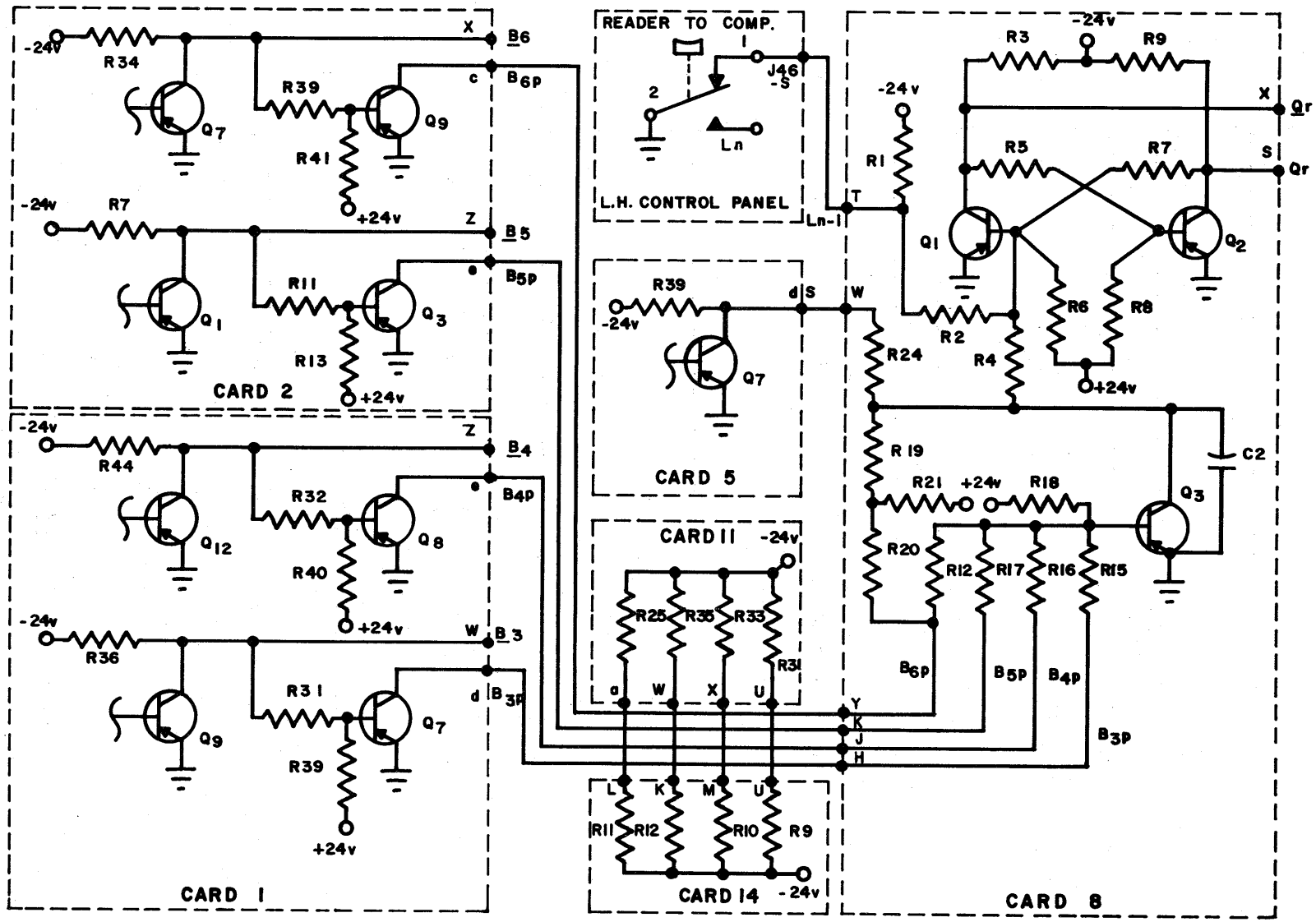
SIMPLIFIED SYSTEM SCHEMATICS - RPC-4500



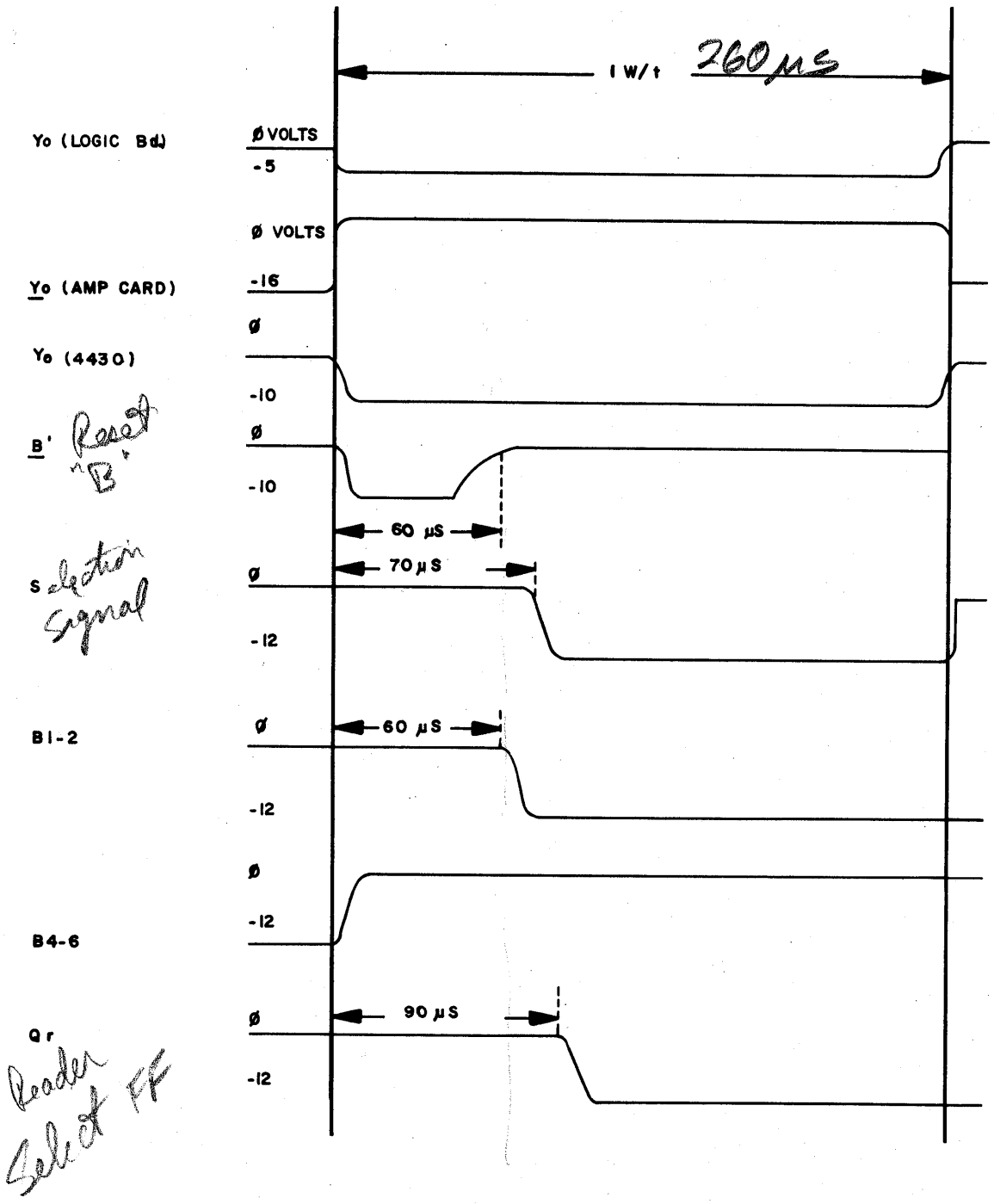
4010 SIGNALS



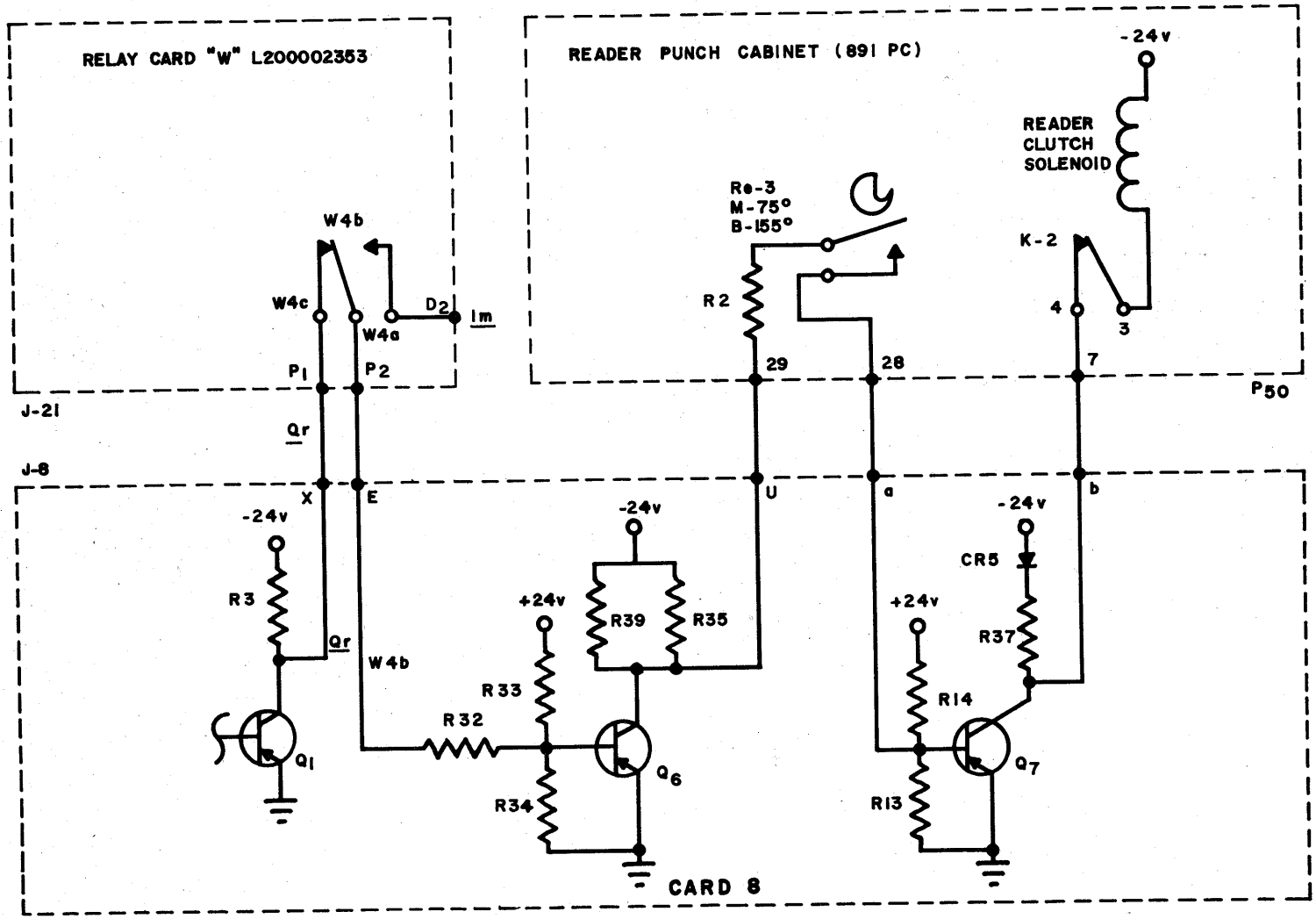
$$S = P_o \underline{(B')} Y_o + L_e$$



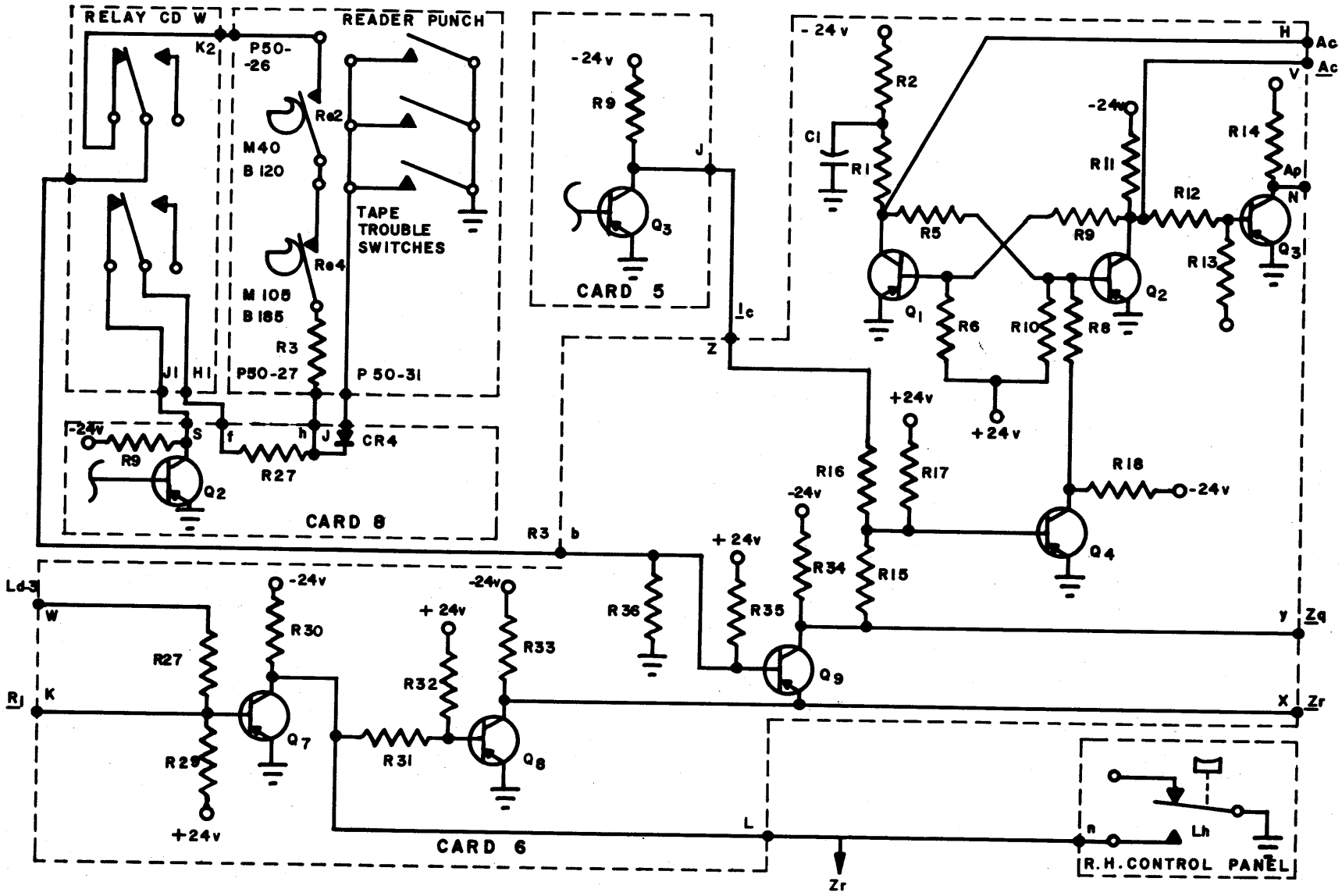
$$Q_r' = \underline{B}_3\ \underline{B}_4\ \underline{B}_5\ \underline{B}_6 + L_n$$



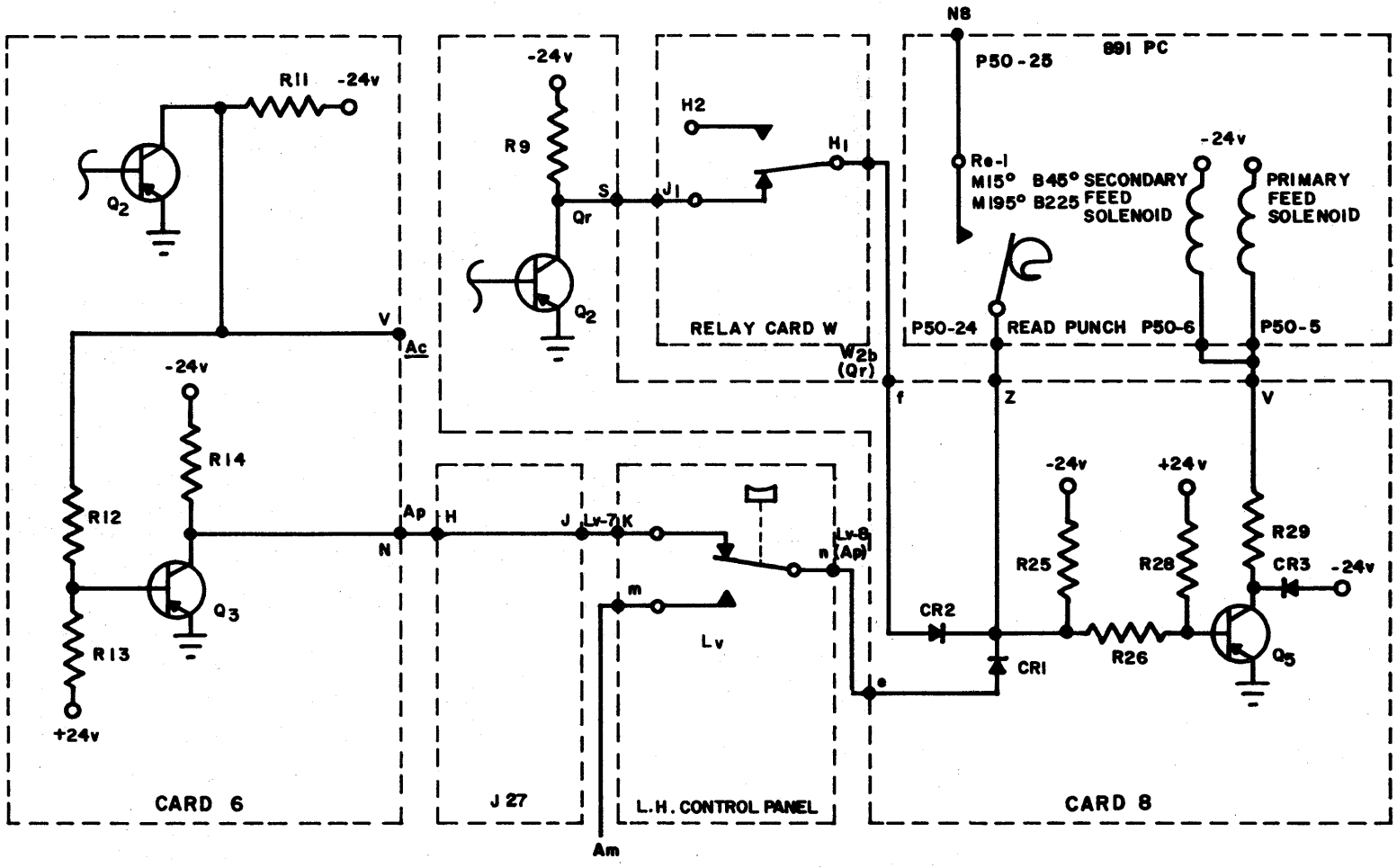
READER SELECT TIMING WAVEFORMS



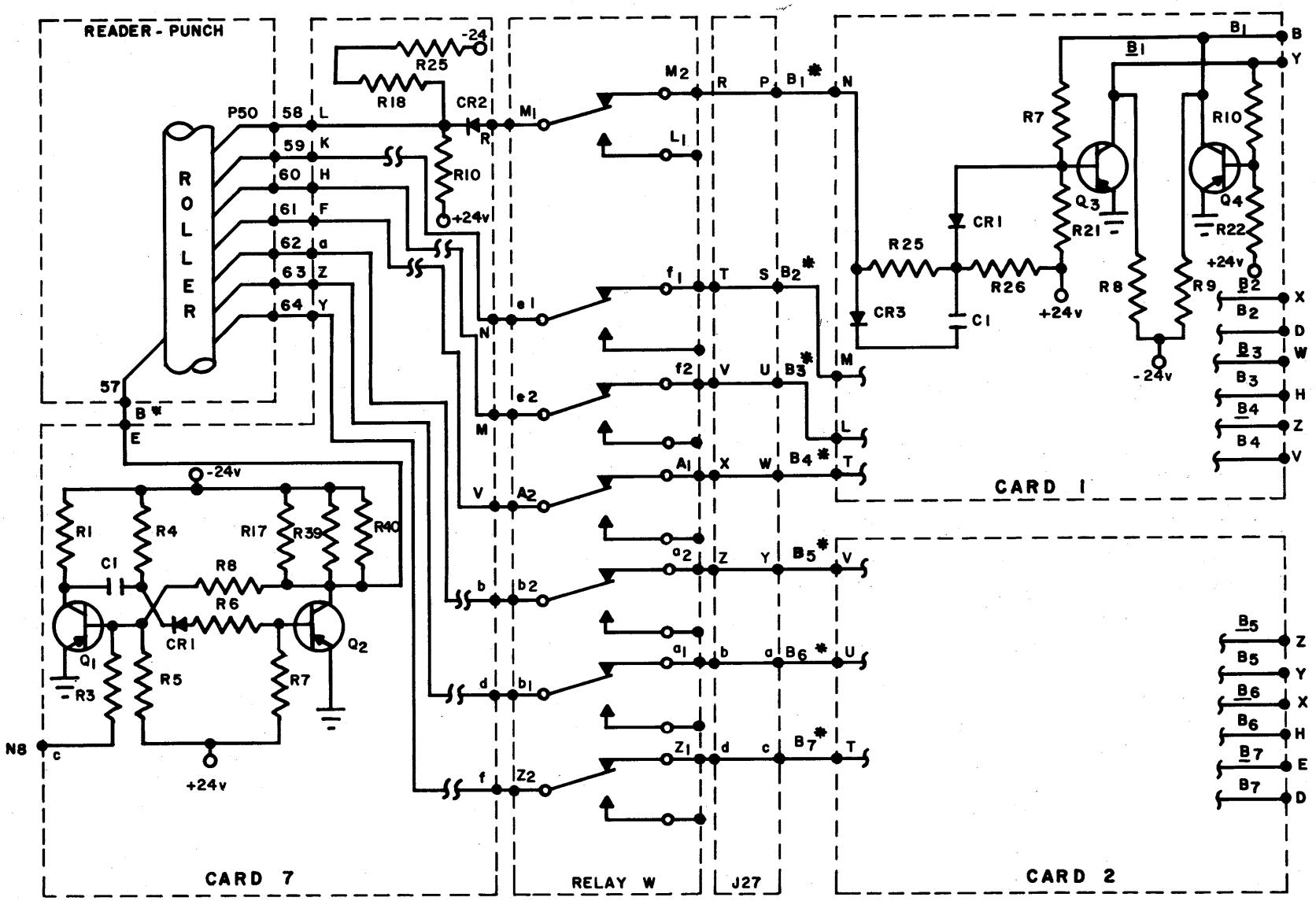
READER CLUTCH = Q_r Re-3



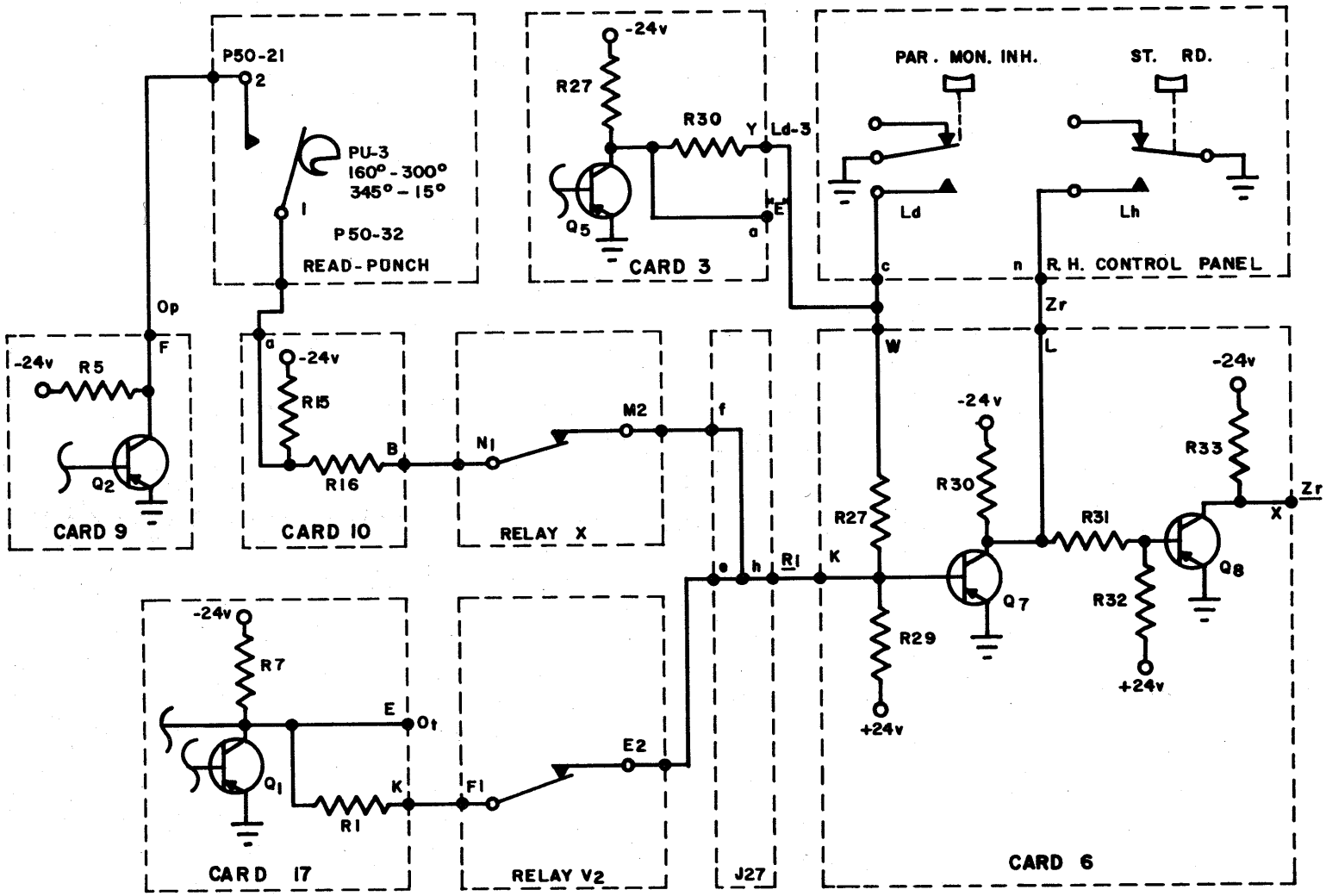
$A_c' = I_c\ Z_q \qquad Z_q = Z_r\ R_3 \qquad R_3 = Q_r\ \underline{L}_v$ (R.T.T.S.) (Re-2 Re-4)



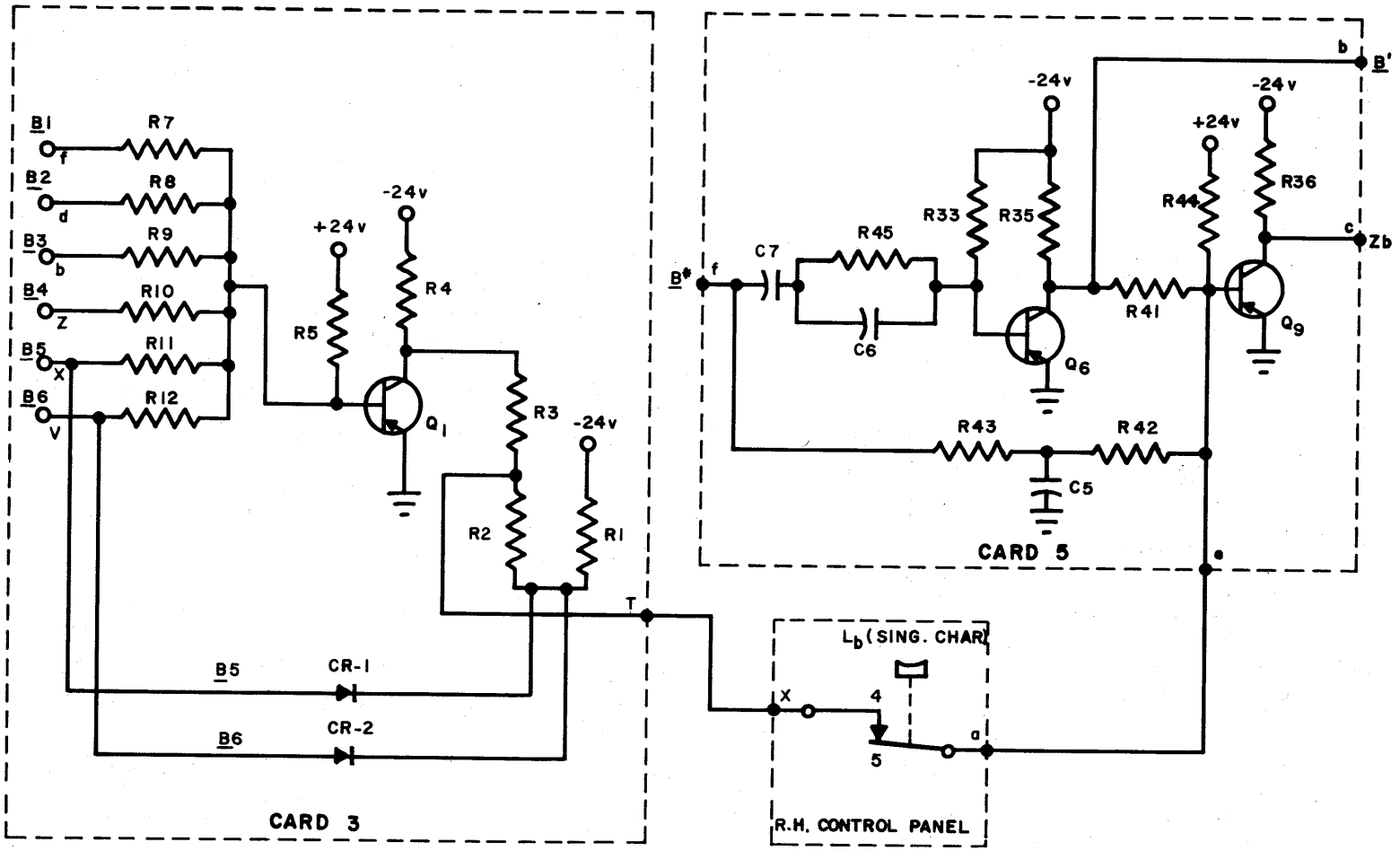
READER TAPE FEED = $A_c\ Q_r\ \underline{L}_v + \ldots$


READER - PUNCH
ROLLER
P50
57
58
59
60
61
62
63
64
L
K
H
F
a
Z
Y
B*
E
-24
R25
R18
CR2
R10
+24v
M1
L1
M2
R
P
B1*
N
e1
e2
M
V
A2
f1
f2
T
S
B2*
V
U
B3*
L
A1
X
W
B4*
T
b
b2
a2
Z
Y
B5*
V
d
b1
a1
b
a
B6*
U
Z1
d
c
B7*
T
f
Z2
R1
R4
R17
R39
R40
C1
R8
R6
CR1
Q1
Q2
R3
R5
R7
N8
c
+24v
CARD 7
RELAY W
J27
R7
R10
Q3
Q4
R21
R22
R25
R26
CR1
CR3
C1
+24v
R8
R9
-24v
B1
B
Y
B2
X
D
B3
W
H
B4
Z
V
CARD 1
B5
Z
Y
B6
X
H
B7
E
D
CARD 2

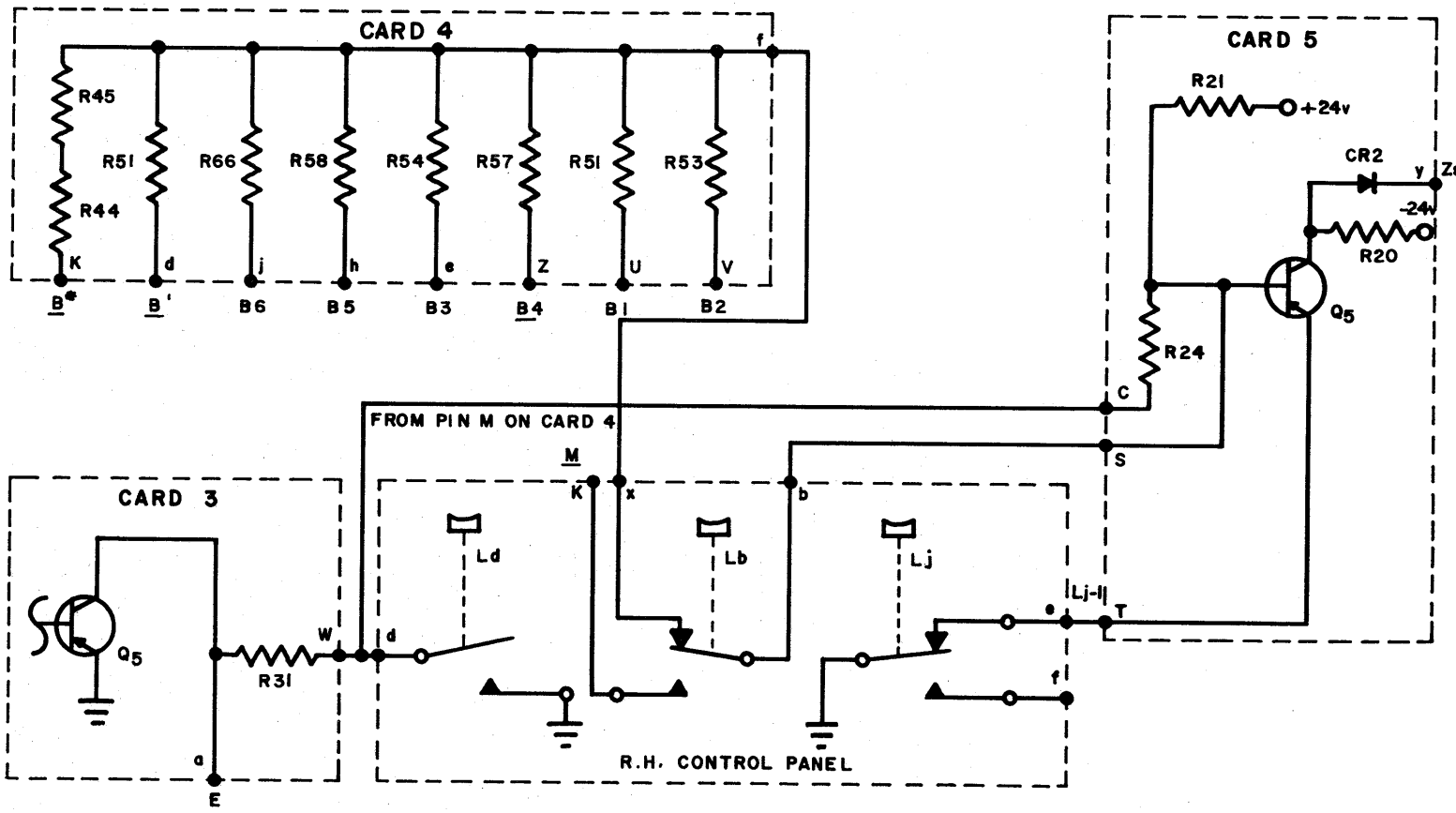
$B_{1-7}^{*} = T_{1-7}\ (B^{*})$



$Z_r = R_1 \underline{L}h\ (\underline{E} + L_d)$ $\qquad$ $R_1 = (PU\text{-}3)\ \underline{O}p\ \underline{L}w\ (\underline{O}t\ \underline{L}u)$

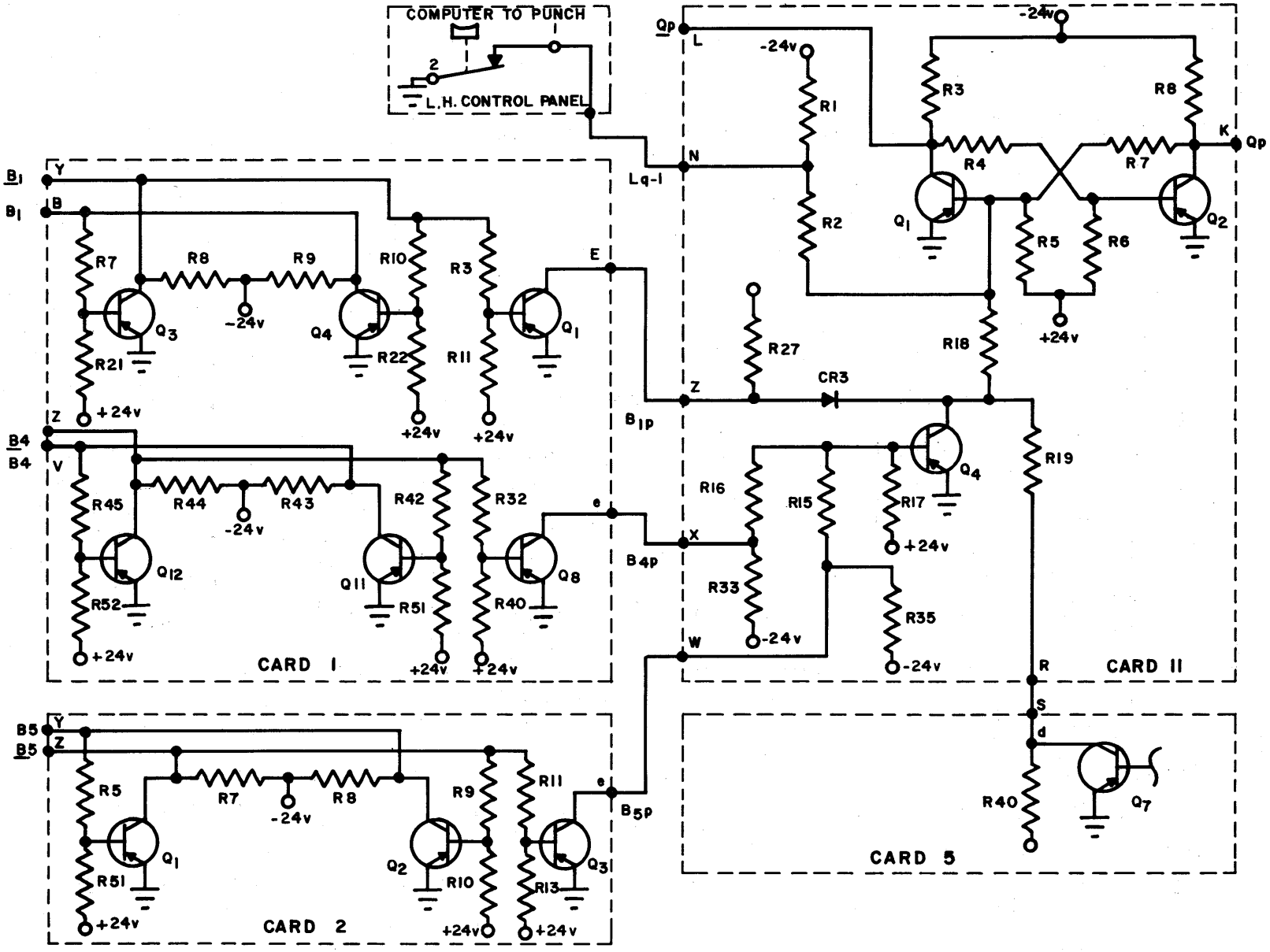


$$Z_b = B^* \underline{(B')} \left[L_b \left(\underline{B}_1 + \underline{B}_2 + \underline{B}_3 + \underline{B}_4 + \underline{B}_5 + \underline{B}_6 \right) \underline{F} \right]$$

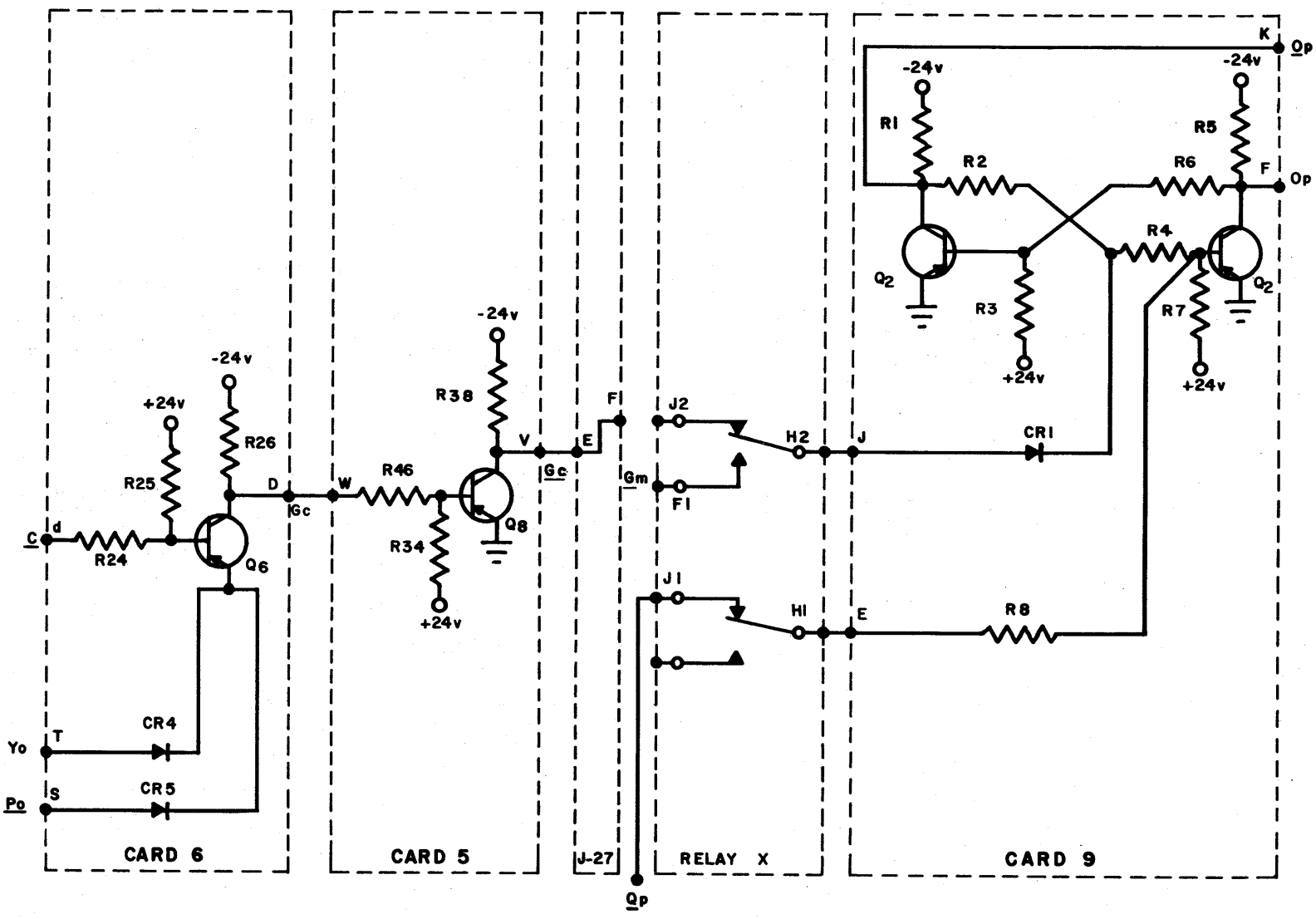


$$Z_s = (L_d + \underline{E}) \left[\underline{L_b}\ \underline{B_1}\ \underline{B_2}\ \underline{B_3}\ \underline{B_4}\ \underline{B_5}\ \underline{B_6}\ \underline{(B')}\ B^* + L_b\ M\right] + L_j$$

DRAWING 39

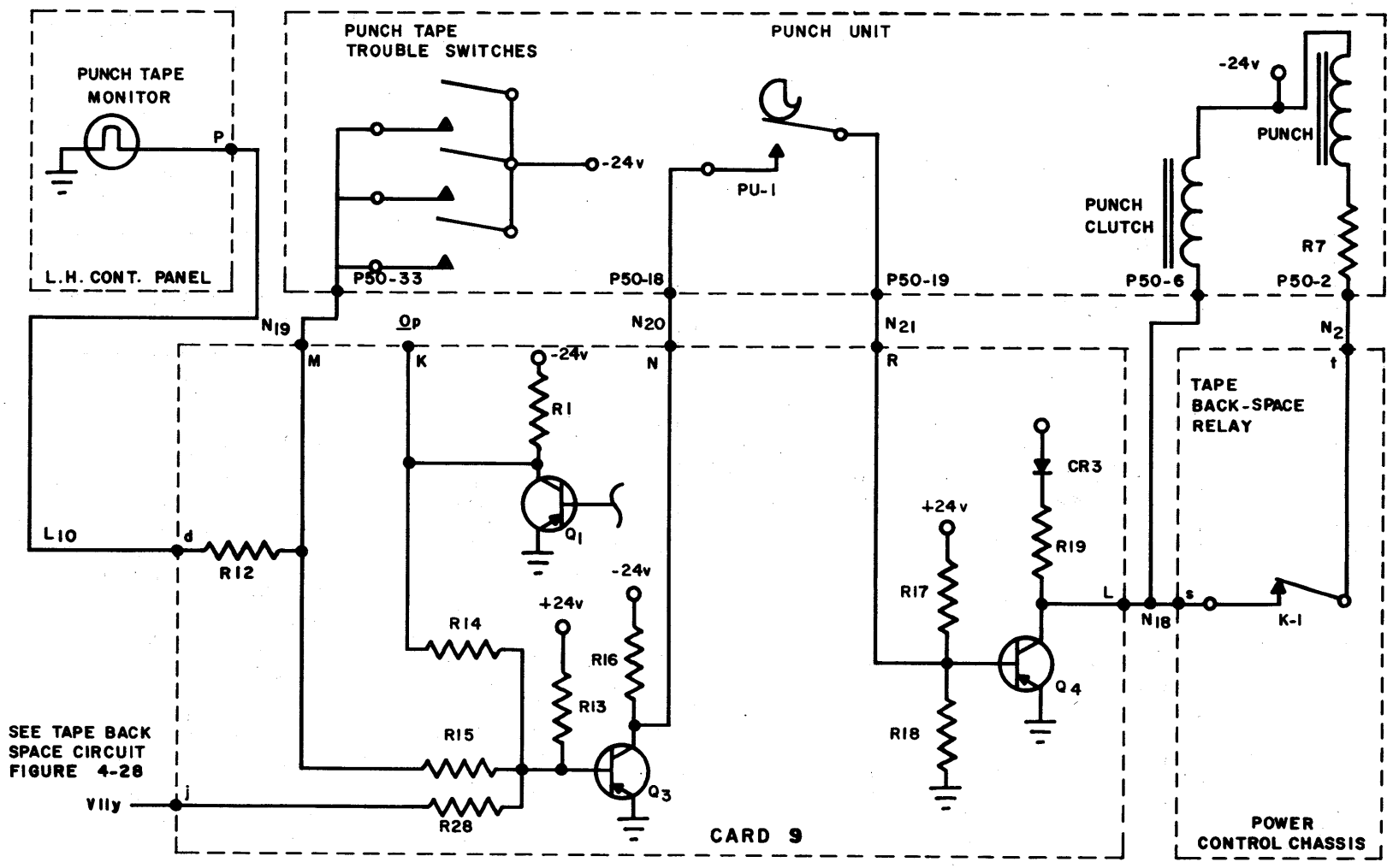


$$Q_p' = S\ B_1\ \underline{B}_4\ \underline{B}_5 + L_q$$



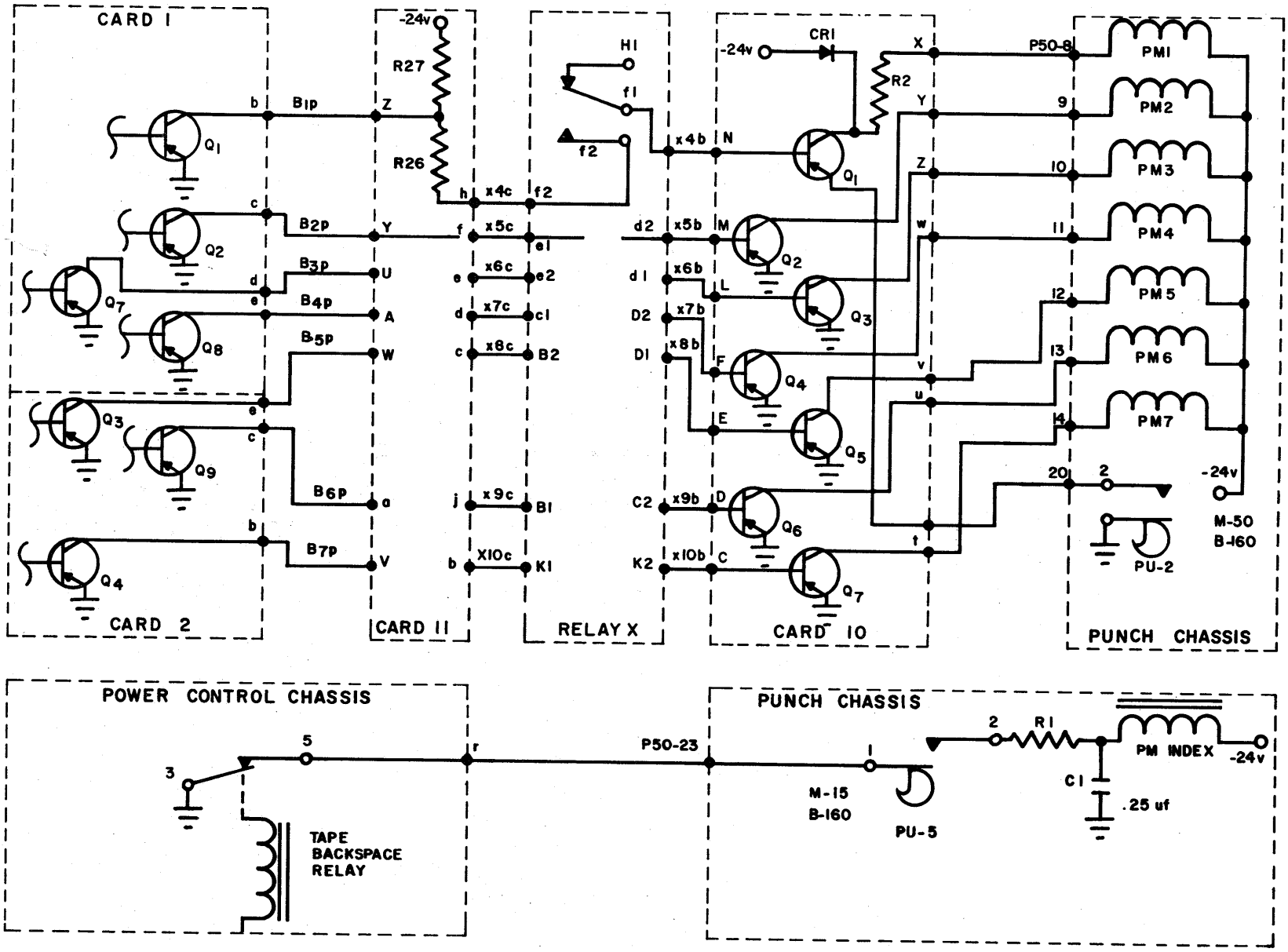
$$O_p' = Q_p\ G_c\ \underline{L}_w + \ldots \qquad G_c = Y_o\ P_o$$

DRAWING 41



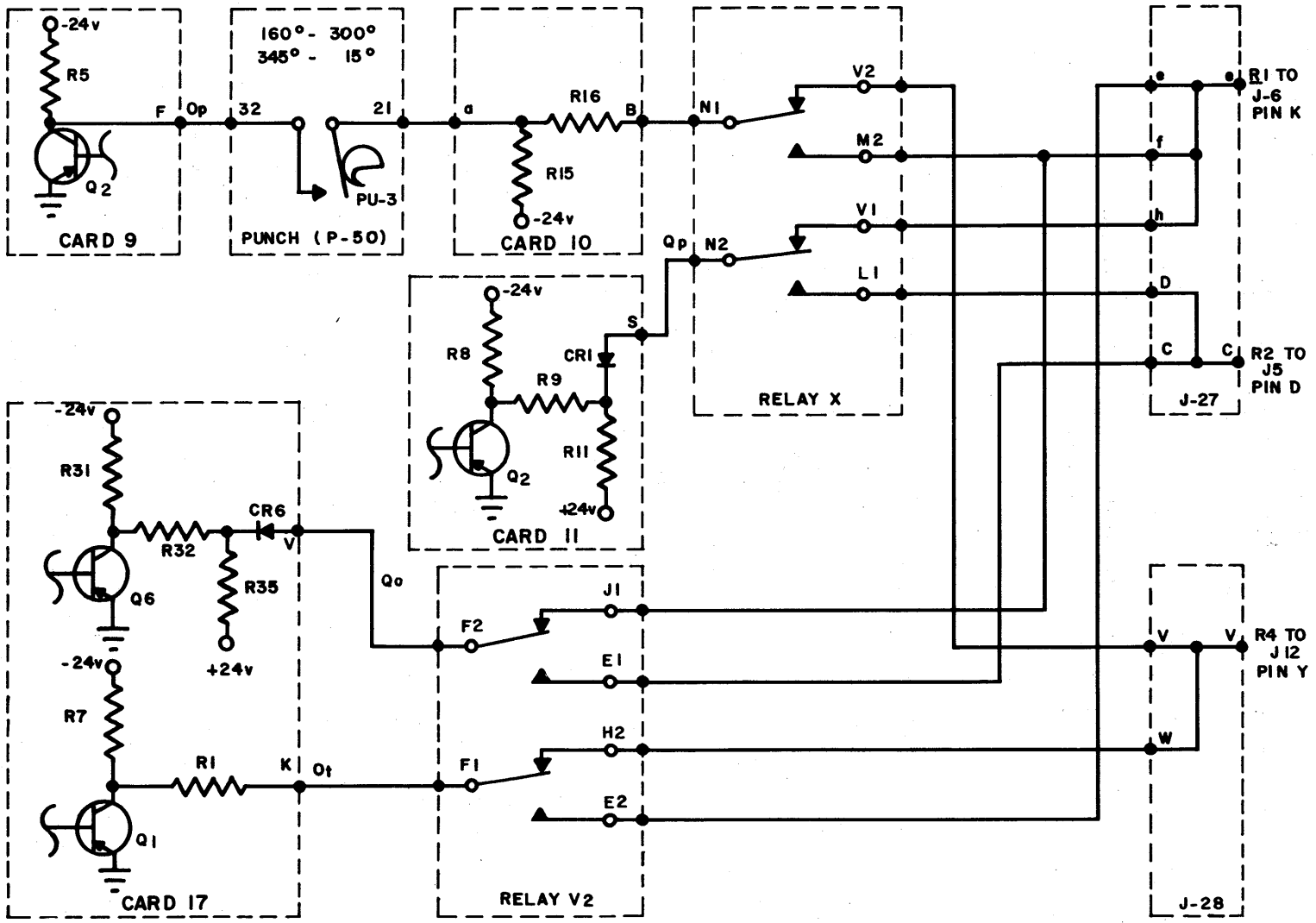
PUNCH FORWARD = O_p (PU-1)(P.T.T.S.)(R.T.F.M.)

PUNCH CLUTCH = O_p (PU-1)(P.T.T.S.)



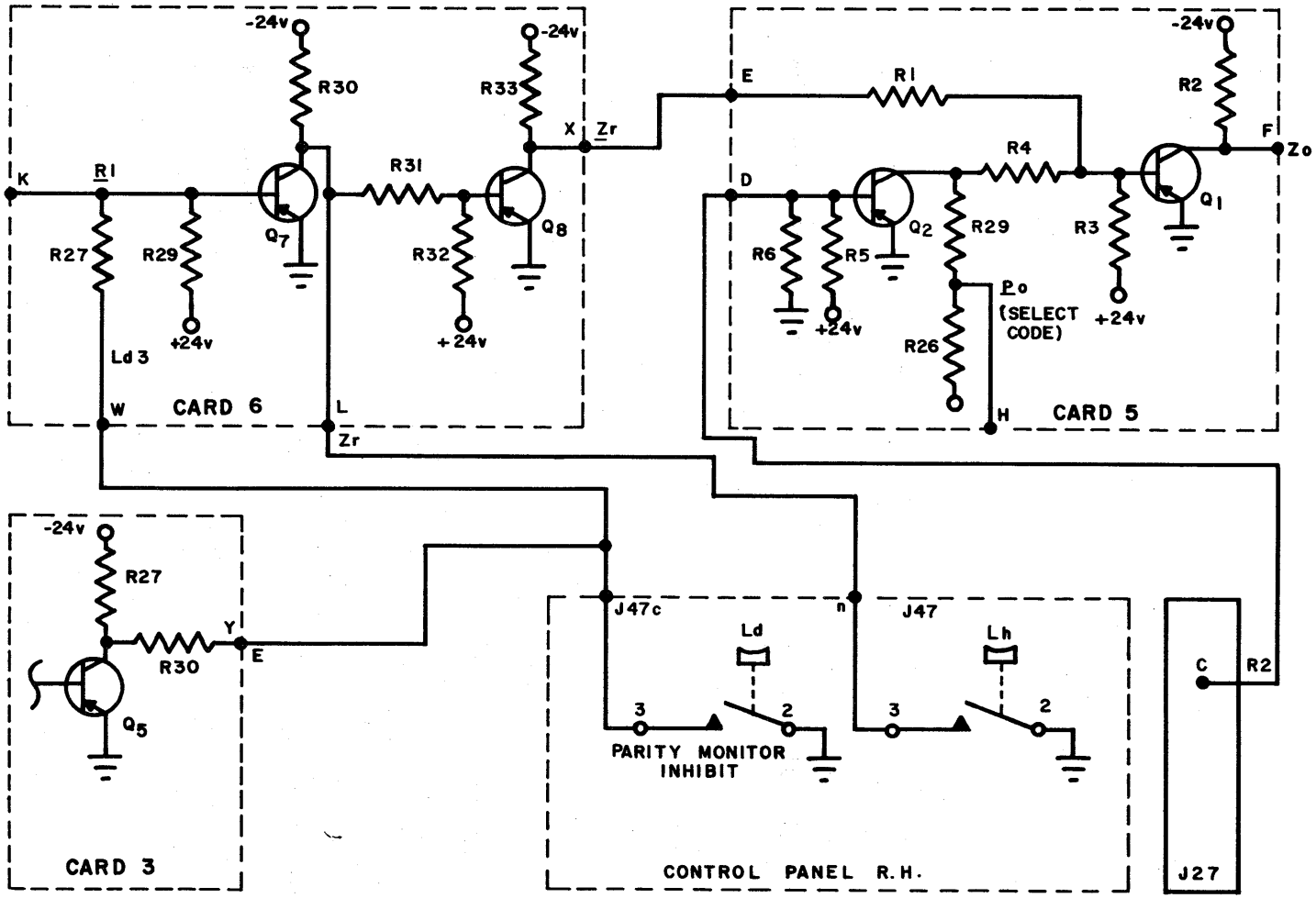
PUNCH MAGNETS = PCH CAM 2 ($B_{1-7}\ \underline{L_W} + H_{1-7}\ L_W$)

INDEX MAGNET = (R.T.F.M.) PCH CAM 5

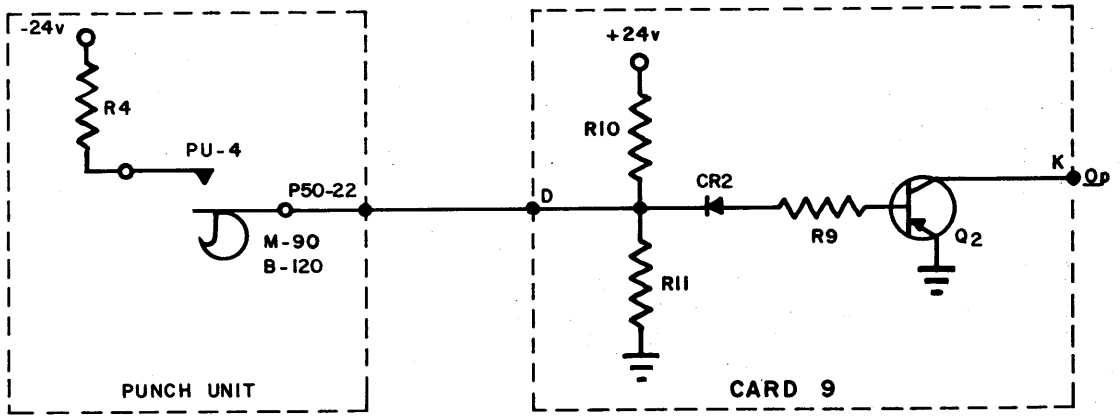


$R_1 = (PU\text{-}3\ \underline{Q}_p\ \underline{L}_w + \underline{Q}_p\ L_w)(\underline{Q}_t\ \underline{L}_u + \underline{Q}_o\ L_u)$

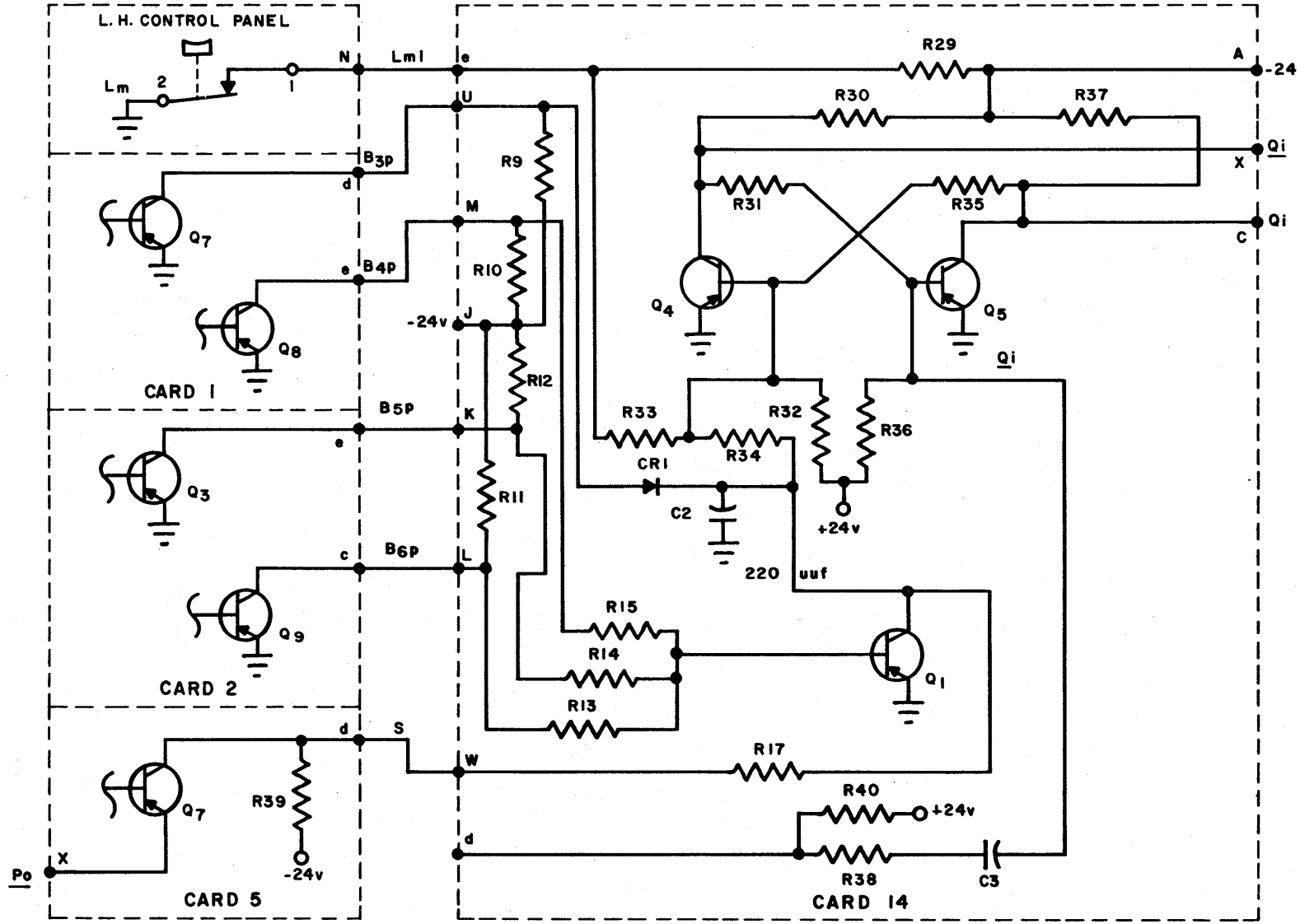
$R_2 = Q_p\ \underline{L}_w = Q_o\ \underline{L}_u$ $\qquad$ $R_4 = (PU\text{-}3\ \underline{Q}_p\ L_w + \underline{L}_w)(\underline{Q}_t\ L_u + \underline{L}_u)$


-24v
R30
R33
X
Zr
K
R1
R31
Q7
Q8
R27
R29
R32
+24v
+24v
Ld 3
W
CARD 6
L
Zr
E
R1
R2
F
Zo
R4
D
Q1
Q2
R29
R3
R6
R5
Po
(SELECT CODE)
+24v
+24v
R26
H
CARD 5
-24v
R27
Y
R30
E
Q5
CARD 3
J47c
n
J47
Ld
Lh
3
2
3
2
PARITY MONITOR INHIBIT
CONTROL PANEL R.H.
C
R2
J27

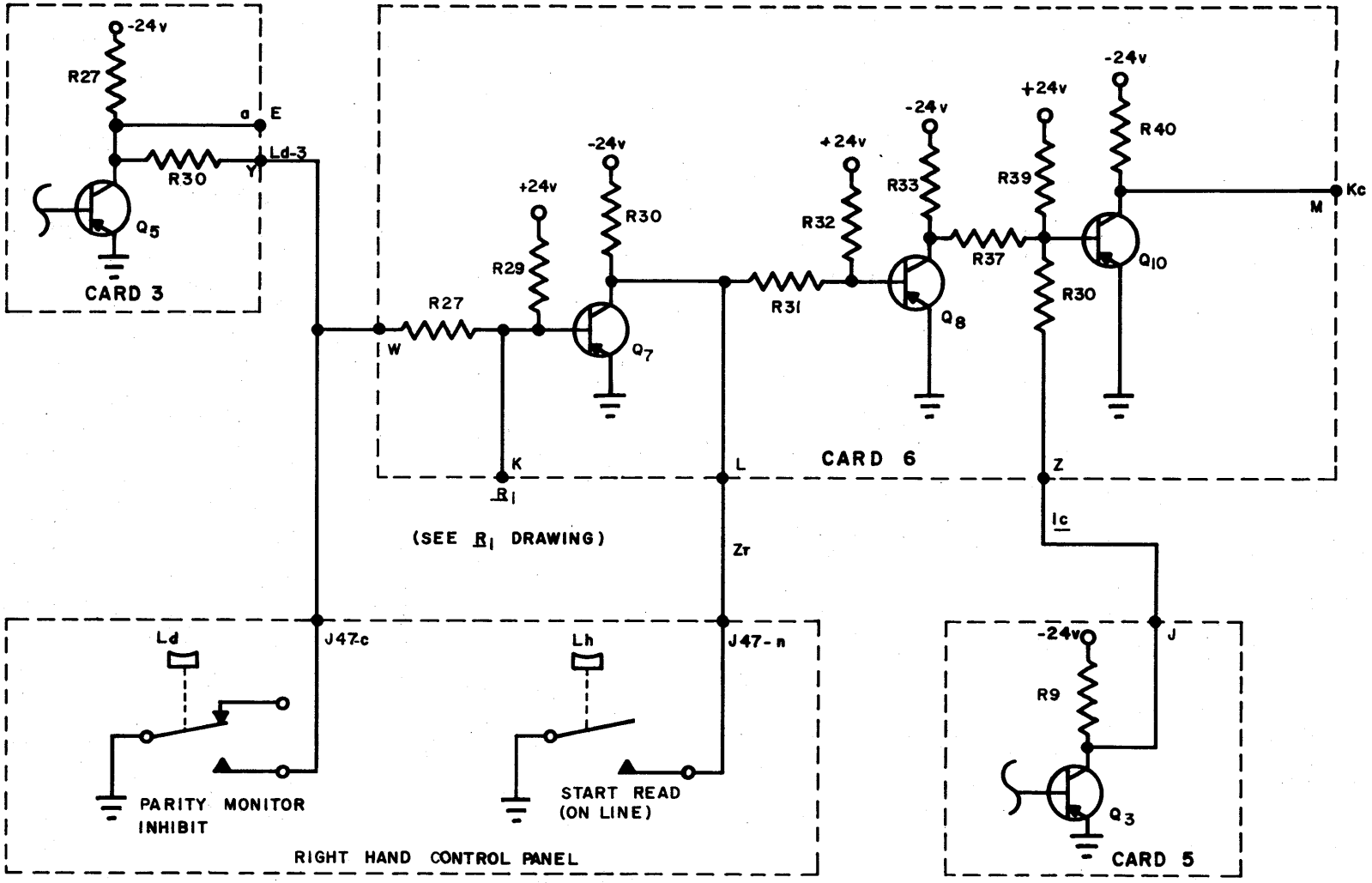
$$Z_o = Z_r \ (R_2 + P_o)$$



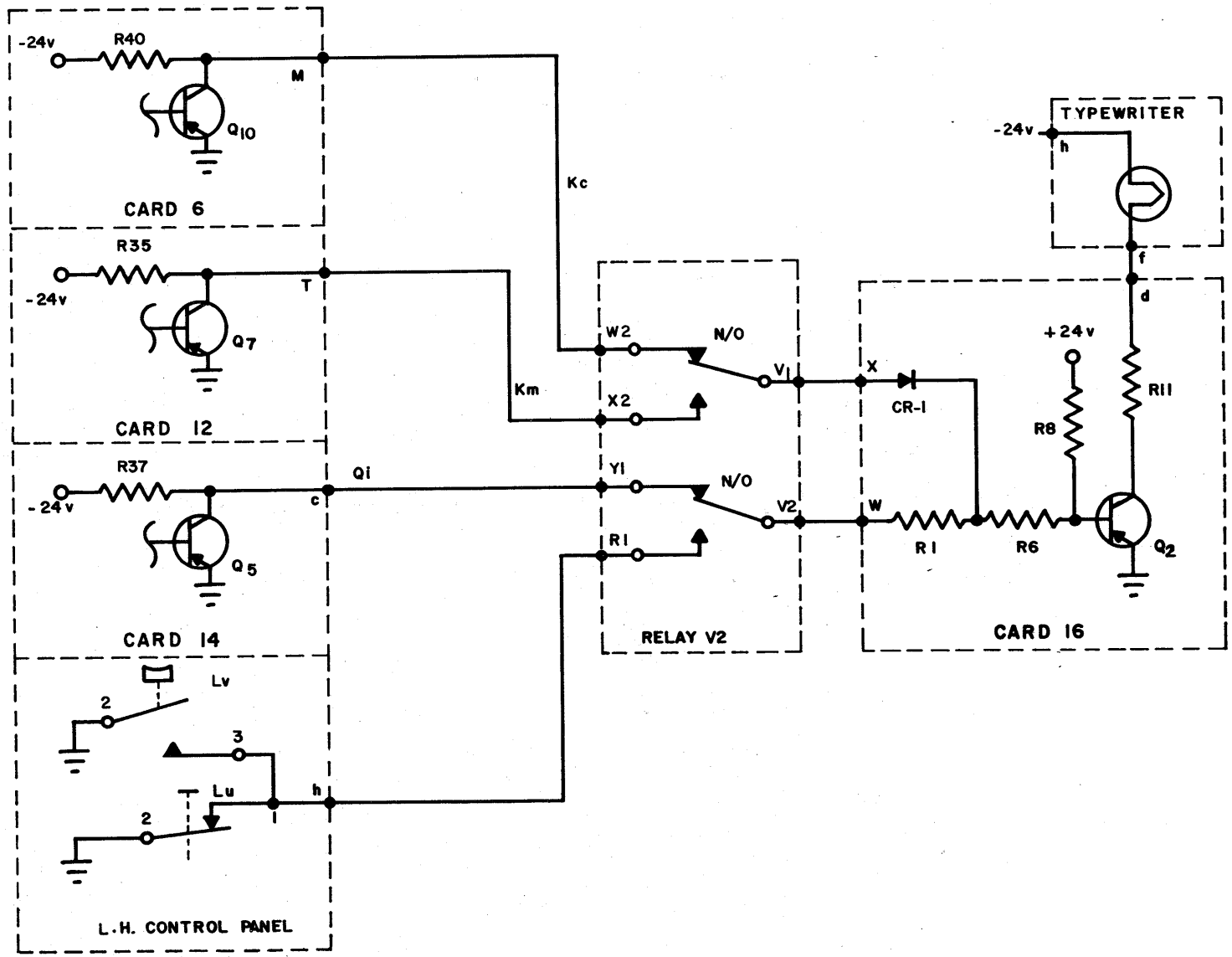
$$O_p' = PU\text{-}4 + \underline{Q}_p \, \underline{LW}$$



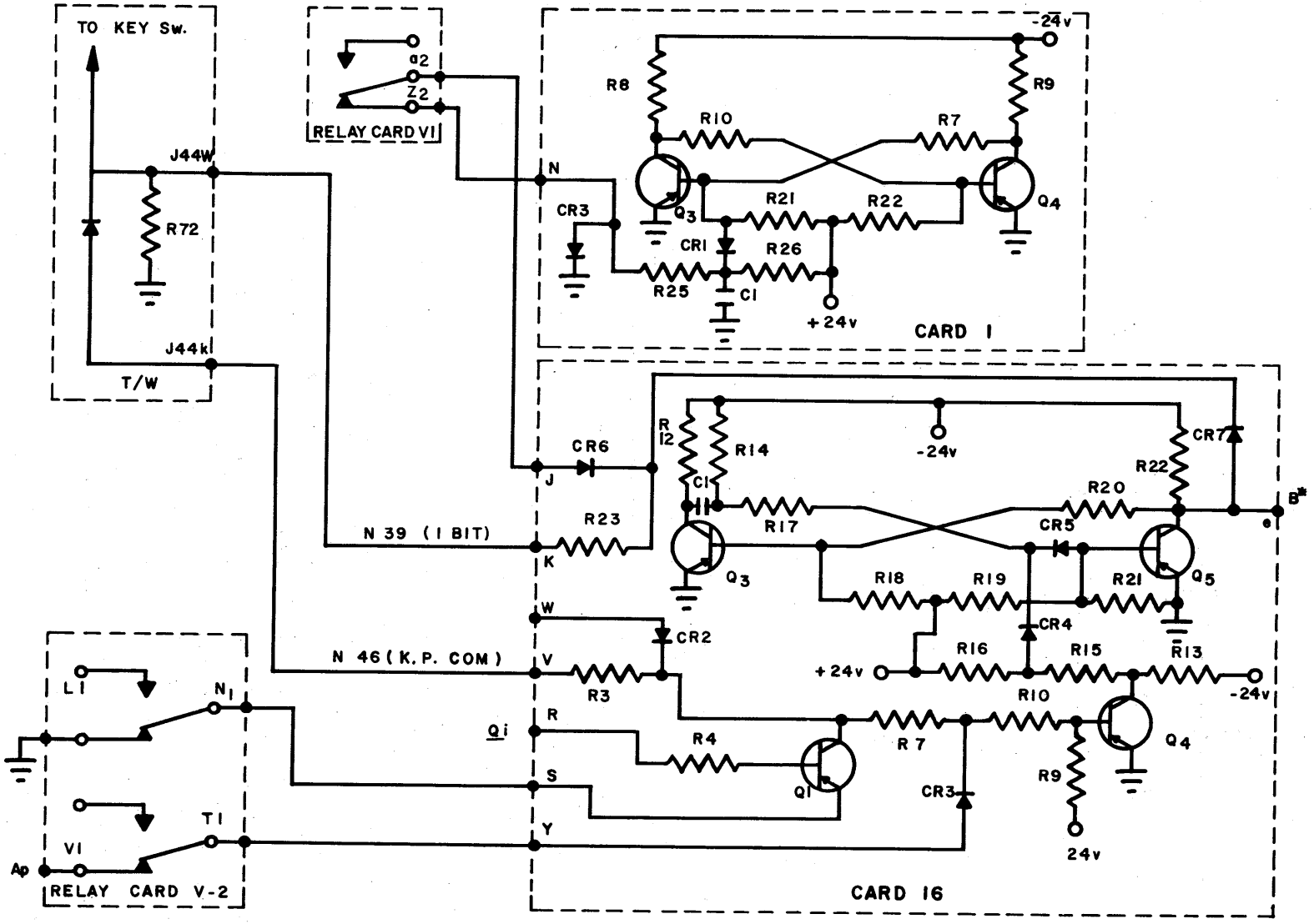
$$Q_i' = S\ B_3\ \underline{B}_4\ \underline{B}_5\ \underline{B}_6 + L_m$$


-24v
R27
a
E
Ld-3
R30
Y
Q5
CARD 3
+24v
R29
-24v
R30
W
R27
Q7
K
R1
(SEE R1 DRAWING)
+24v
R32
-24v
R33
R31
Q8
+24v
R39
-24v
R40
R37
Q10
R30
Kc
M
CARD 6
L
Z
Zr
Ic
Ld
J47-c
Lh
J47-n
PARITY MONITOR
INHIBIT
START READ
(ON LINE)
RIGHT HAND CONTROL PANEL
-24v
J
R9
Q3
CARD 5

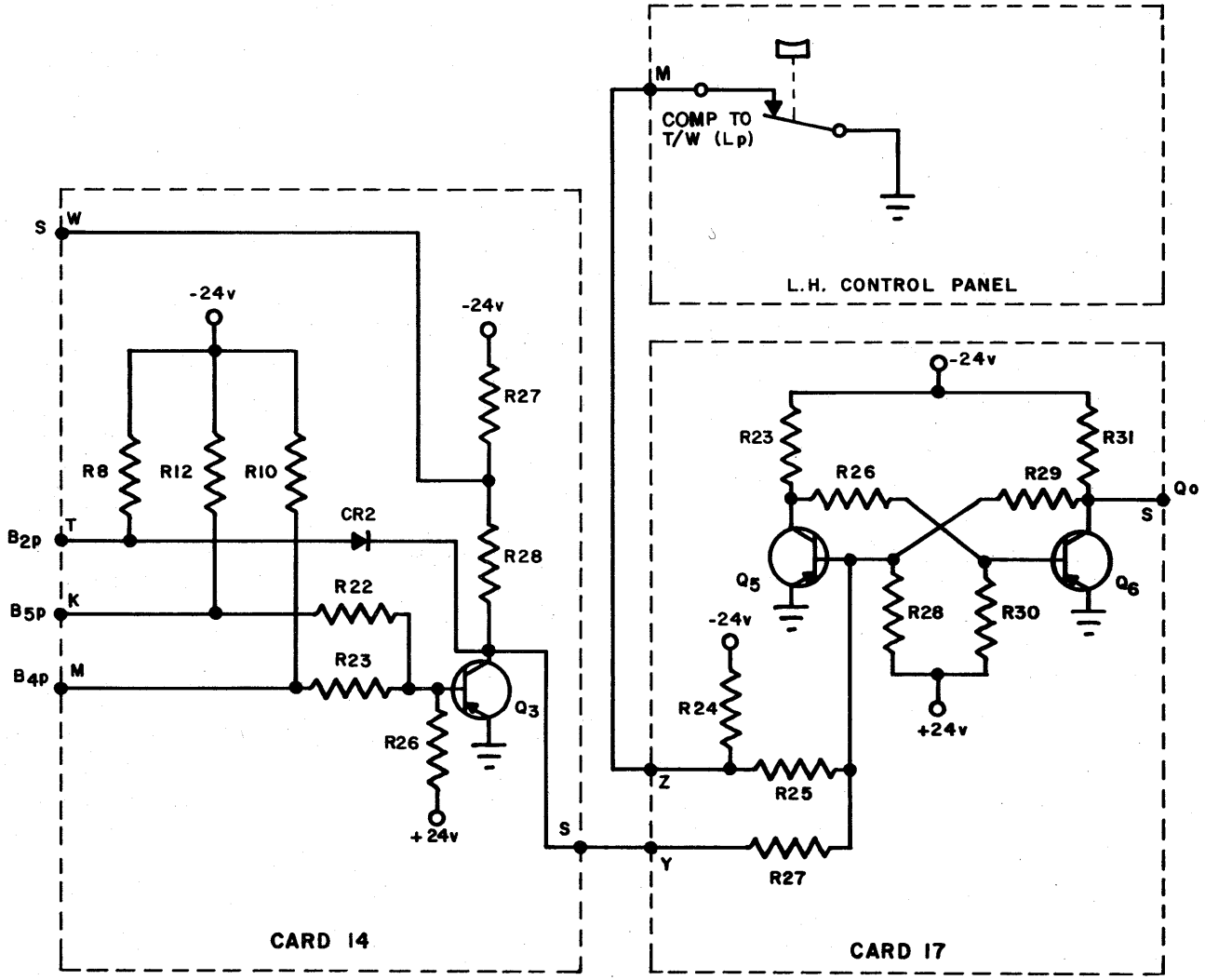
$$K_c = Z_r \; I_c$$



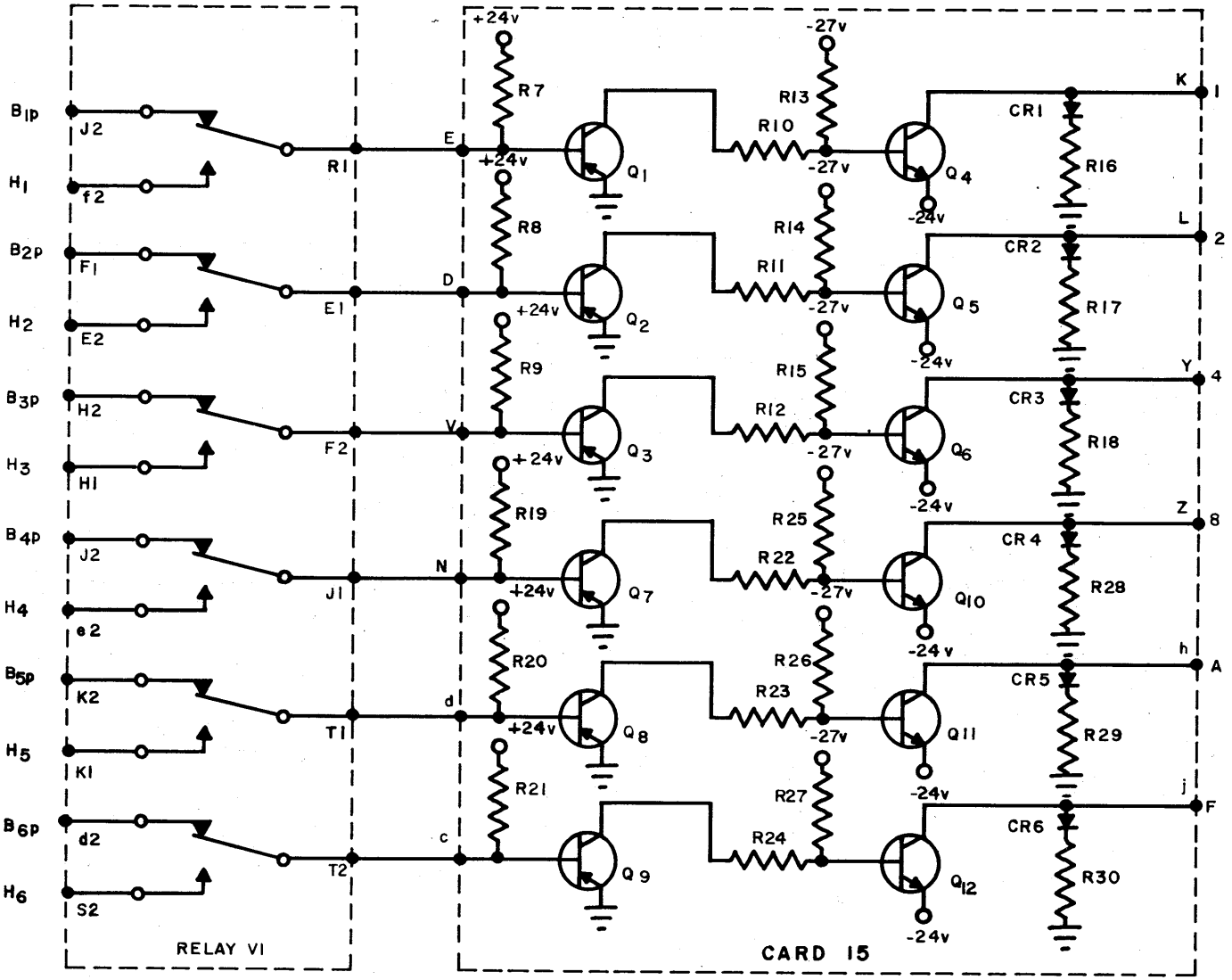
OK TO TYPE = $\underline{L}_u\, Q_i\, K_c + L_u\, \underline{L}_v\, K_m$



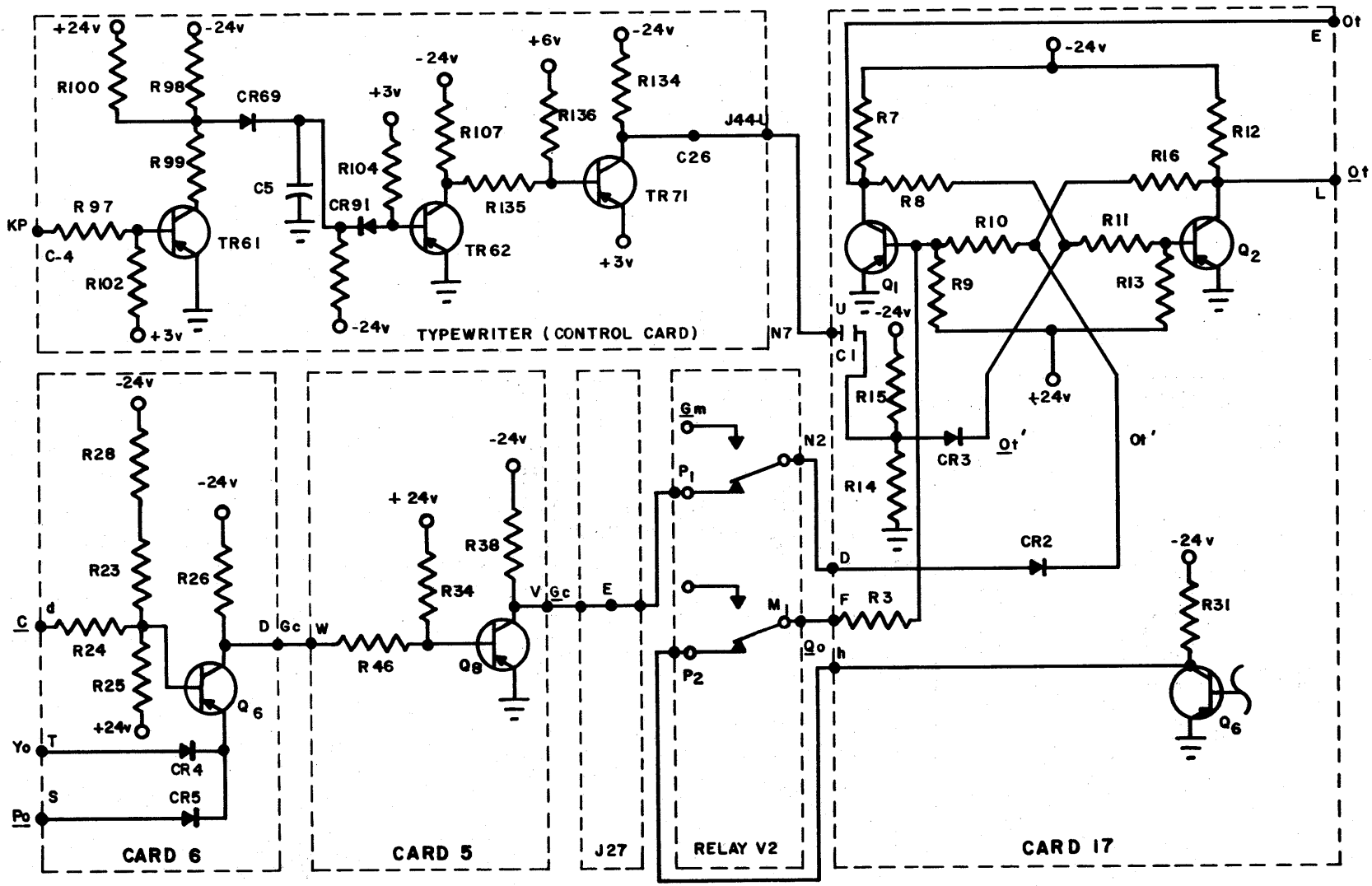
$B^* = N_{46}\ \underline{L}_u\ Q_i\ A_c$ B^*_{1-7} = (Encoder Bits 1-7) B*



$$Q_o = S\ B_2\ \underline{B}_4\ \underline{B}_5 + L_p$$



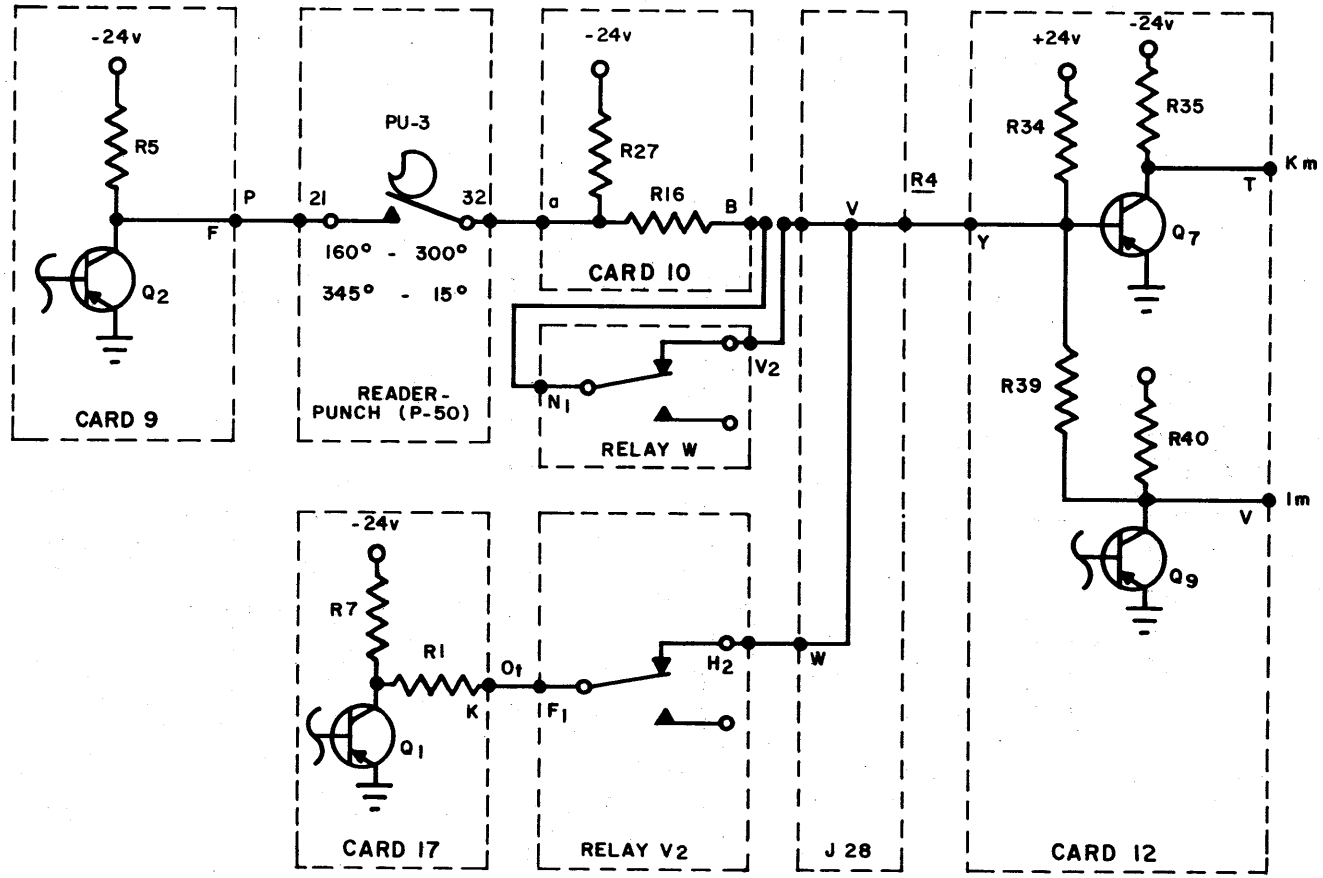
TRANSLATOR BIT DRIVE = $B_{1-6}\ \underline{L_u} + H_{1-6}\ L_u$



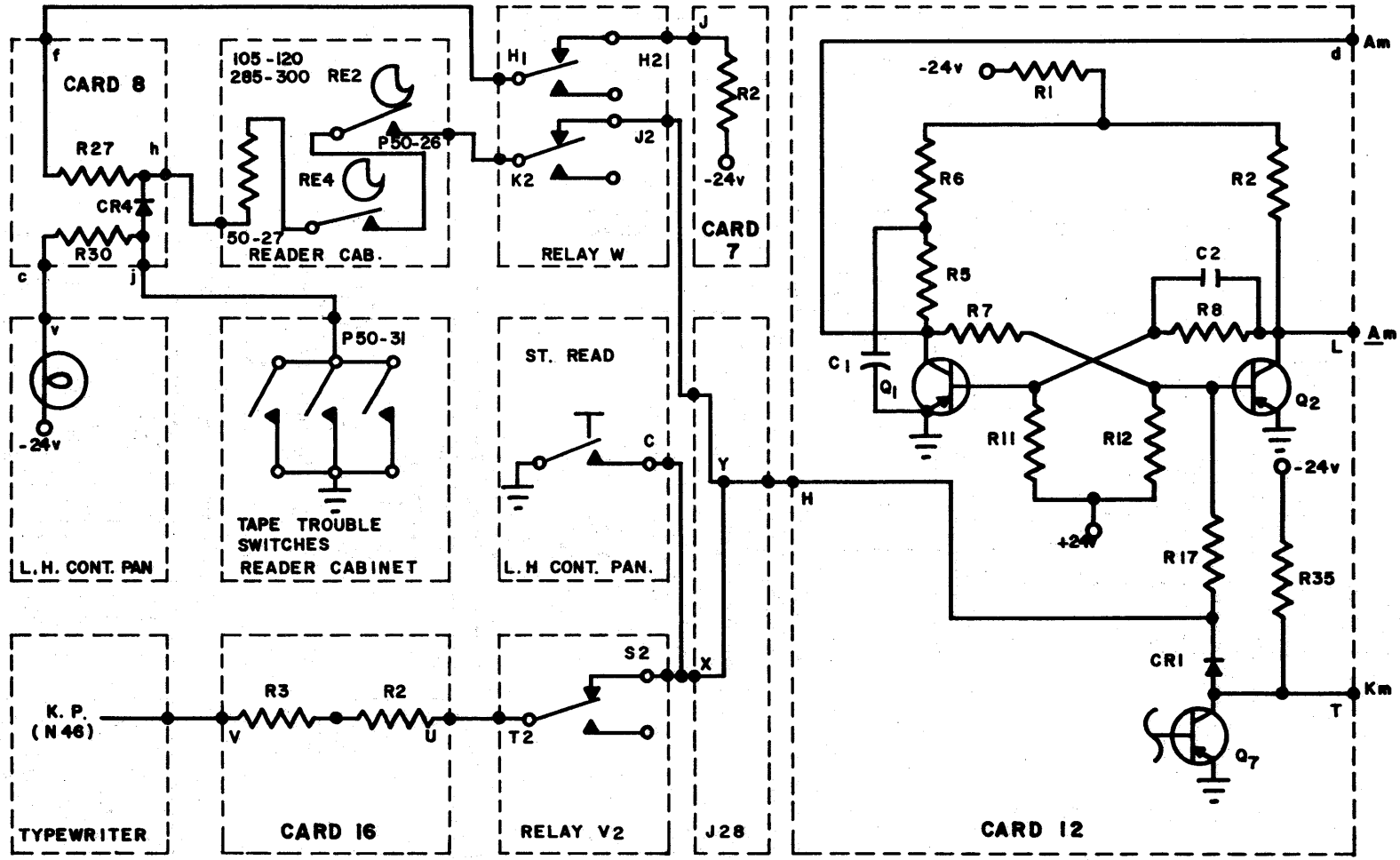
$O_t' = G_c \underline{L}_u \qquad G_c = Y_o P_o \qquad \underline{O}_t' = \frac{d}{dt}$ (N-46) LEADING

DRAWING 53

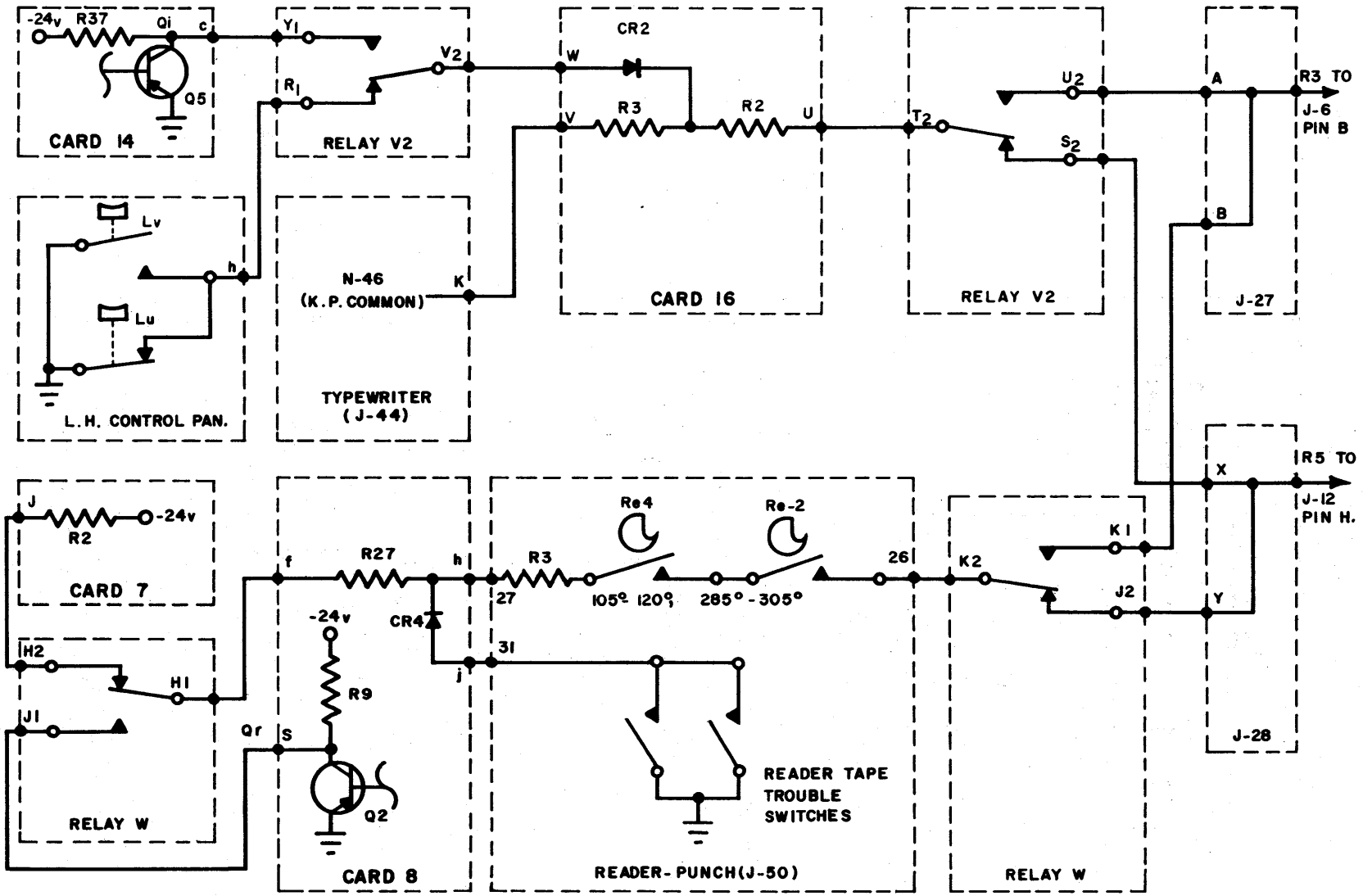
A3-91



$K_m = I_m R_4$ $\qquad R_4 = (PU\text{-}3\ \underline{O}_p L_w + \underline{L}_w)(\underline{O}_t L_u + \underline{L}_u)$


CARD 8
f
R27
h
CR4
R30
c
j
v
-24v
L.H. CONT. PAN
105-120
285-300
RE2
RE4
50-27
READER CAB.
P50-26
P50-31
TAPE TROUBLE
SWITCHES
READER CABINET
H1
H2
K2
J2
RELAY W
ST. READ
C
L.H CONT. PAN.
J
R2
-24v
CARD 7
Y
X
S2
T2
K.P.
(N46)
TYPEWRITER
R3
R2
V
U
CARD 16
RELAY V2
J28
H
-24v
R1
d
Am
R6
R2
R5
C2
R7
R8
C1
Q1
L
Am
Q2
R11
R12
+24v
-24v
R17
R35
CR1
Km
T
Q7
CARD 12

$$A_m' = K_m R_5$$



$$R_3 = (Re\text{-}2\ Re\text{-}4)\ Q_r\ \underline{L_v}\ (\underline{R.T.T.S.}) + \underline{L_u}\ Q_i\ N\text{-}46$$

$$R_5 = (Re\text{-}2\ Re\text{-}4)\ L_v\ (\underline{R.T.T.S.}) + L_u\ \underline{L_v}\ N\text{-}46$$

APPENDIX 4

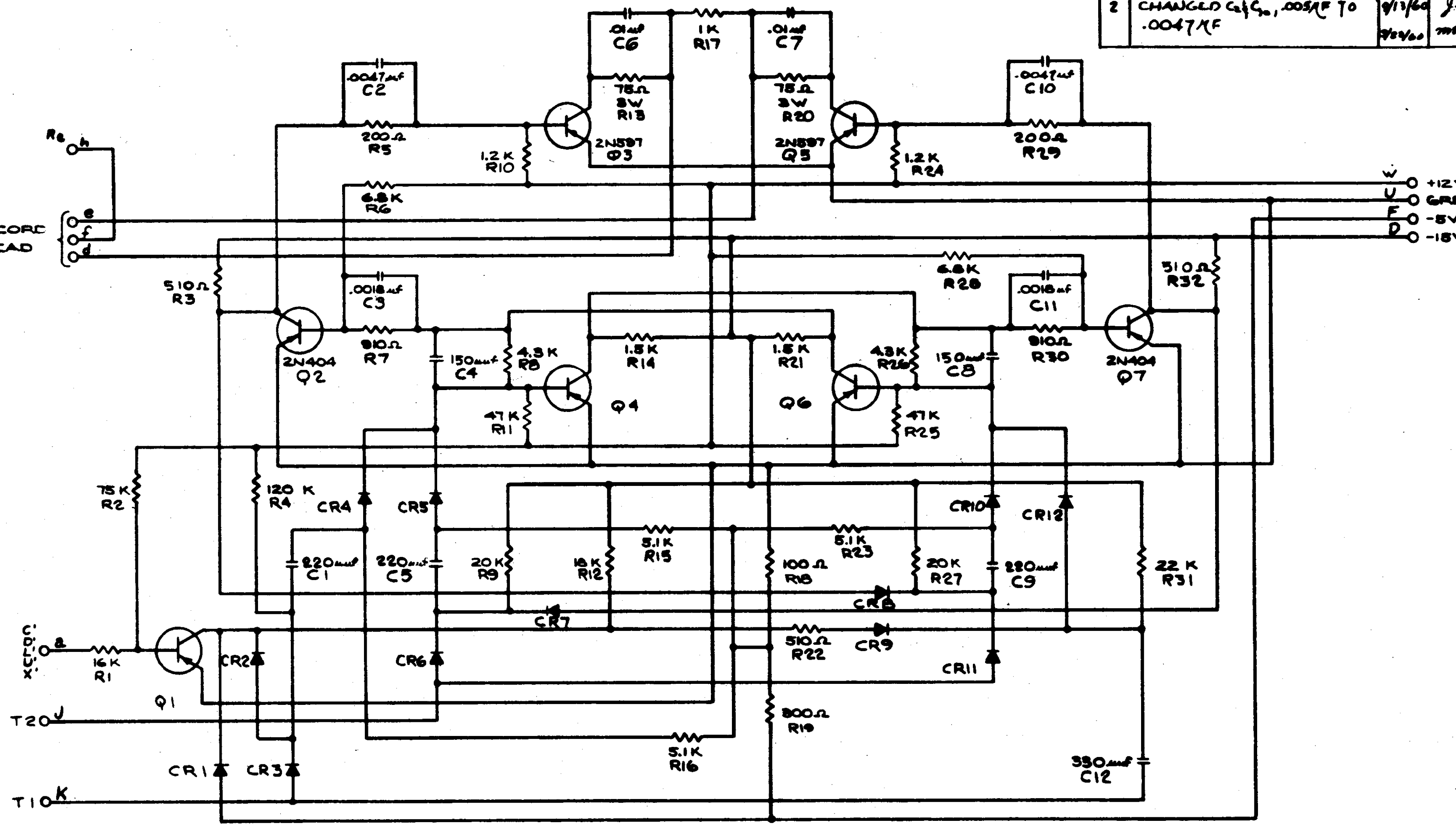
RPC-4010 CENTRAL COMPUTER SCHEMATICS

NOTES:

1. ALL RESISTORS 1/2 W ± 5% EXCEPT WHERE NOTED
2. 3W RESISTORS SPRAGUE BLUE JACKET # 242E7505 OR EQUIV. PER L600001517
3. ALL DIODES ARE SYLVANIA D1243 OR EQUIV. PER L200006440.
4. Q1, Q4 & Q6 ARE 2N1301 OR EQUIV. PER L200006441.

REVISIONS

SYM	DESCRIPTION	DATE	APPROVAL
1	E.O. 51921 SEE E.O. FOR CHANGES	8-4-60 8-9-60	[illegible] A. JAFFE
2	EO# 54779 CHANGED C2 & C10, .005μF TO .0047μF	9/13/60 9/24/60	J. K[illegible]



LIST OF MATERIAL

ITEM	REQ'D	LIBRASCOPE NO.	DESCRIPTION	MATL.	MATL. SPEC.	UNIT WT.

L535000863	4010
NEXT ASSY.	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

DO NOT SCALE THIS DRAWING

MATERIAL

DRAFTSMAN: [signature] DATE 8-26-59

CHECKER

ENGINEER: [signature] 9/22/60

APPROVAL: [signature] [signature] 9/2[illegible]

CONTRACT NO.

SCHEMATIC - RECORD AMPLIFIER

SCALE: NONE

UNIT WT.

L200006162

DRAWING 1

A4-5

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
2	REVISED & REDRAWN PER E.O. 60168	12-7-60	DR DOYLE

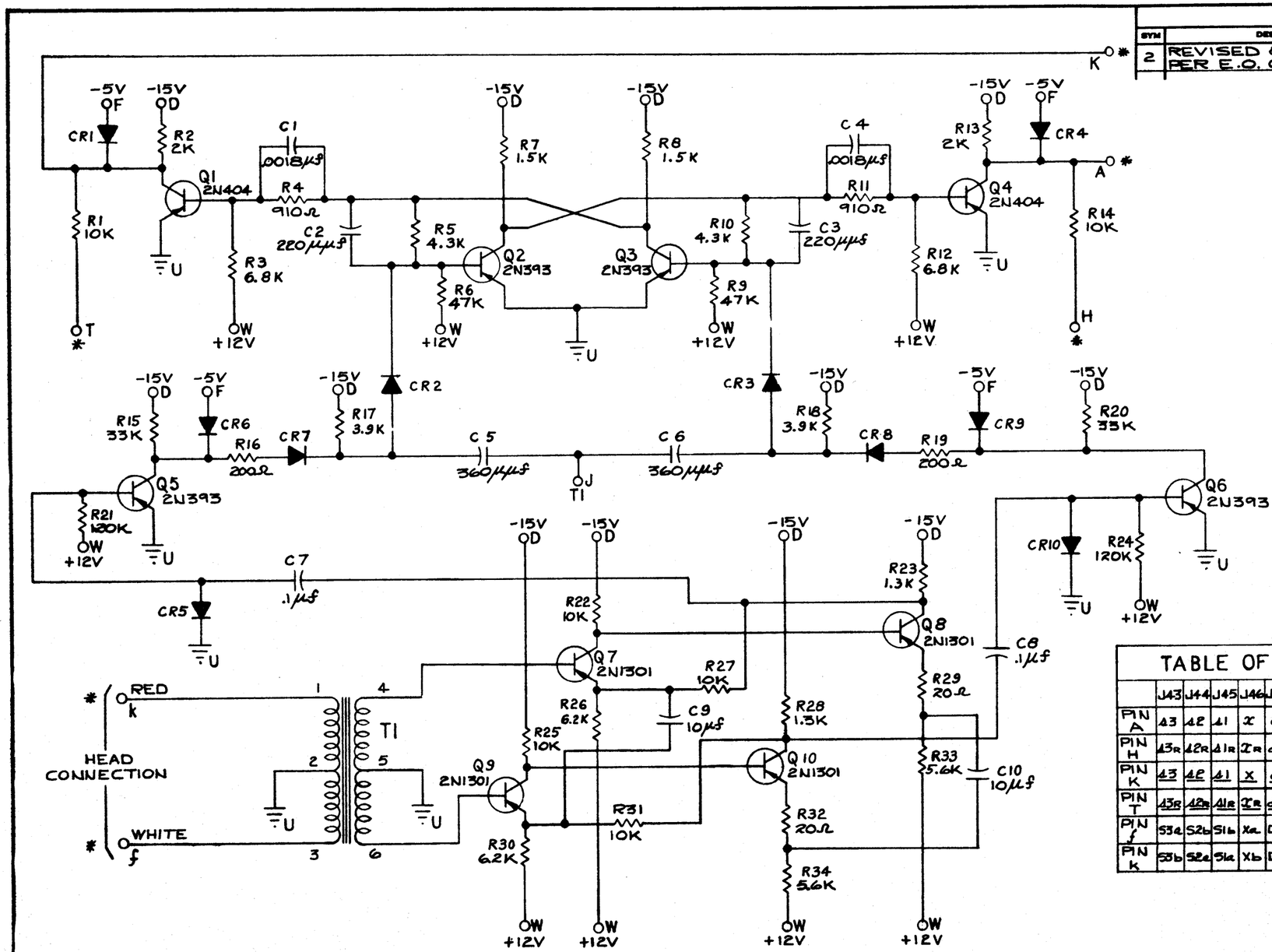


TABLE OF FUNCTION										
	J43	J44	J45	J46	J47	J48	J49	J50	J51	J52
PIN A	A3	A2	A1	X	d	c	L*	L	U*	U
PIN H	A3R	A2R	A1R	XR	dR	cR	LR*	LR	UR*	UR
PIN K	A3	A2	A1	X	d	c	L*	L	U*	U
PIN T	A3R	A2R	A1R	XR	dR	cR	LR*	LR	UR*	UR
PIN f	S3a	S2b	S1b	Xa	Da	Ca	La*	La	Ua*	Ub
PIN k	S3b	S2a	S1a	Xb	Db	Cb	Lb*	Lb	Ub*	Ua

L200007300

ITEM	REQ'D	NO.	DESCRIPTION	MATL.	MATL. SPEC.	UNIT WT.

LIST OF MATERIAL

L 535003526	4010
NEXT ASSY.	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DIMENSIONS
FRACTIONAL ± 2 PLACES ± .010, ± 4 PLACES ± .0025
ANGLES ± 1° BREAK EDGES .005 MAX.
SURFACE FINISH 125
DO NOT SCALE THIS DRAWING
MATERIAL

DRAFTSMAN	J. ZIEBA	DATE 4 AUG 60
CHECKER		
ENGINEER	J.M. LOWRY	19 AUG 60
APPROVAL	C.W. JOHNSON	8-19-60
CONTRACT NO.		

SCHEMATIC
READ AMPLIFIER
RECIRCULATING LINES
SERIAL 1 THRU 60

SCALE NONE | UNIT WT.

L200007300

NOTES:
1. ALL RESISTORS TO BE 1/2 W ± 5% CARBON UNLESS OTHERWISE STATED.
2. DIODES TO BE PER L531000552.
3. FOR SIGNAL FUNCTIONS SEE TABLE.

L200009984

SYM	DESCRIPTION	DATE	APPROVAL
1	REVISED PER E.O. 68446	2 JUNE 64	
2	REVISED PER E.O. 68518	13 JULY 64	
3	REVISED PER E.O. 90815	23 JUNE 65	

SEE TABLE A

SEE TABLE K

SEE TABLE T

SEE TABLE H

G -5V.

TWO STAGE A.C. DIFFERENTIAL AMPLIFIER
MINIMUM GAIN 4 VOLTS PEAK TO PEAK
SECOND STAGE GAIN MAY BE RAISED BY
CHANGING R34 TO 20 OHMS ON
MAIN MEMORY ONLY.

TABLE OF FUNCTION										
	J43	J44	J45	J46	J47	J48	J49	J50	J51	J52
PIN A	$\overline{d3}$	$\overline{d2}$	$\overline{d1}$	x	d	c	$\overline{L^*}$	$\overline{L}$	$\overline{u^*}$	$\overline{u}$
PIN H	$\overline{d3}_R$	$\overline{d2}_R$	$\overline{d1}_R$	x_R	d_R	c_R	$\overline{L^*}_R$	$\overline{L}_R$	$\overline{u^*}_R$	$\overline{u}_R$
PIN K	$\overline{d3}$	$\overline{d2}$	$\overline{d1}$	$\overline{x}$	$\overline{d}$	$\overline{c}$	$\overline{L^*}$	$\overline{L}$	$\overline{u^*}$	$\overline{u}$
PIN T	$\overline{d3}_R$	$\overline{d2}_R$	$\overline{d1}_R$	$\overline{x}_R$	$\overline{d}_R$	$\overline{c}_R$	$\overline{L^*}_R$	$\overline{L}_R$	$\overline{u^*}_R$	$\overline{u}_R$
PIN f	$S3_a$	$S2_b$	$S1_b$	X_a	D_a	C_a	L^*_a	L_a	U^*_a	U_b
PIN k	$S3_b$	$S2_a$	$S1_a$	X_b	D_b	C_b	L^*_b	L_b	U^*_b	U_a

PIN LAYOUT OF CARD

SEE TABLE | -15V | -5V | SEE TABLE | T1 | SEE TABLE | SEE TABLE | +12V | SEE TABLE | SEE TABLE

A B C D E F H J K L M N P R S T U V W X Y Z a b c d e f h j k

D.C LEVEL TO BE WITHIN
-4.8 VOLTS TO -6.8 VOLTS.

D.C. LEVEL TO BE WITHIN
-1 VOLT TO -3 VOLTS.

R35 OR R29 MAY BE CHANGED TO
BALANCE OUTPUT OF Q9 TO Q10.

NOTES:
1. ALL RESISTORS TO BE 1/2W, ±5%
2. DIODES TO BE PER L531 000 582.

L535003708	4010
NEXT ASSY.	USED ON
APPLICATION	

LIST OF MATERIAL

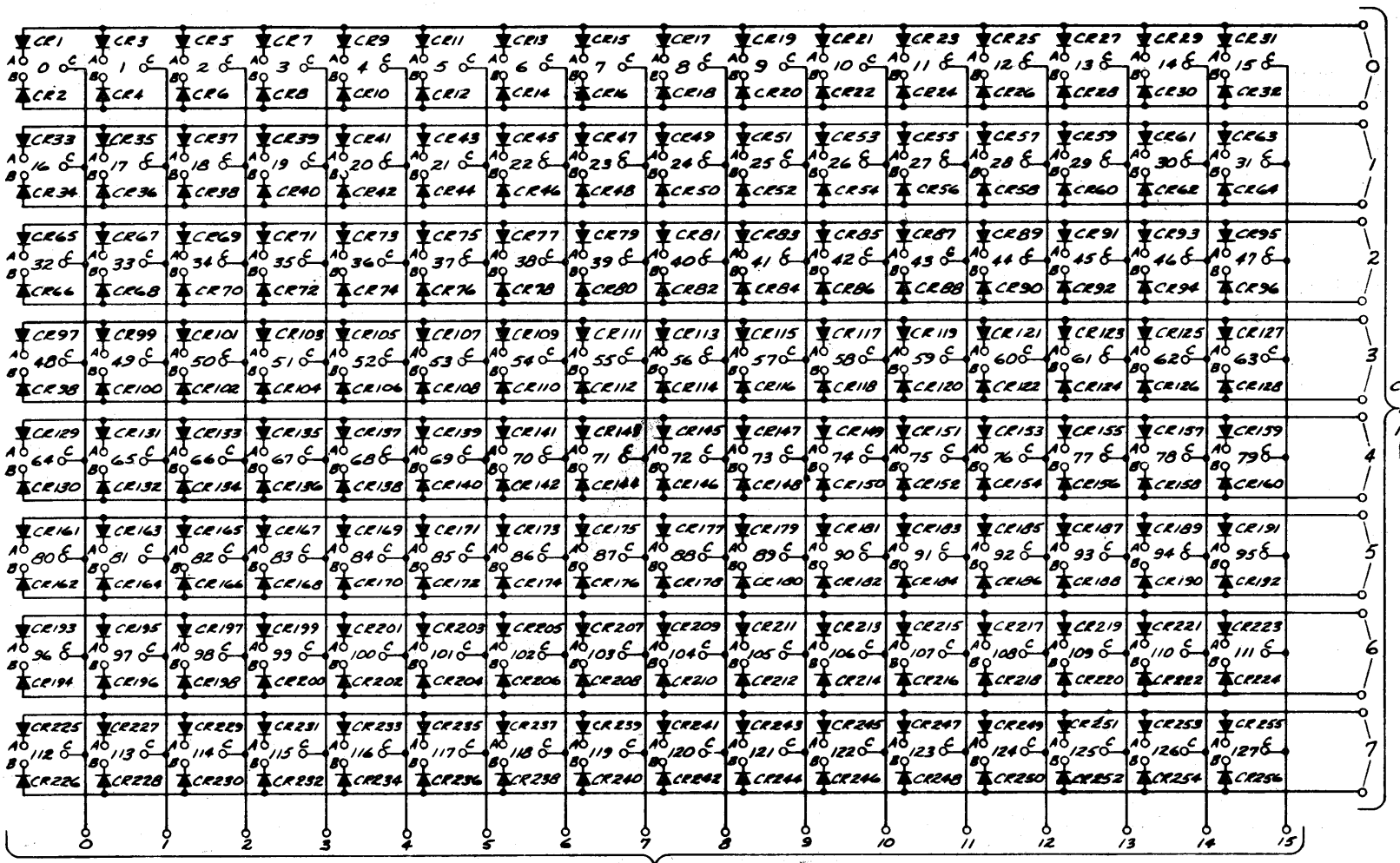
SCHEMATIC
READ AMPLIFIER
RECIRCULATING LINES
SERIALS 61 & UP

L200009984

DRAWING 3

A4-9

NOTES:
1. DIODES ARE IN2069 PER L531000529 OR EQUIV. PER ESL531000529.
2. NUMBERS 0 THRU 127 IDENTIFY MAGNETIC HEADS ON MEMORY DRUM.



REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL

ITEM	DWG'S	NO.	DESCRIPTION	MATL.	MATL. SPEC.	UNIT WT.
LIST OF MATERIAL						

L536000518	7010
NEXT ASSY.	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DIMENSIONS
FRACTIONAL ± 2 PLACES ± .010, 3 PLACES ± .05, 4 PLACES ± .0025
ANGULAR ± 1° BREAK EDGES .005 MAX.
SURFACE FINISH
DO NOT SCALE THIS DRAWING
MATERIAL

DRAFTSMAN	W.P.K. MATZIS	DATE 5 MAY 1960
CHECKER		
ENGINEER		1 JUNE 1960
APPROVAL		5-31-60
CONTRACT NO.		

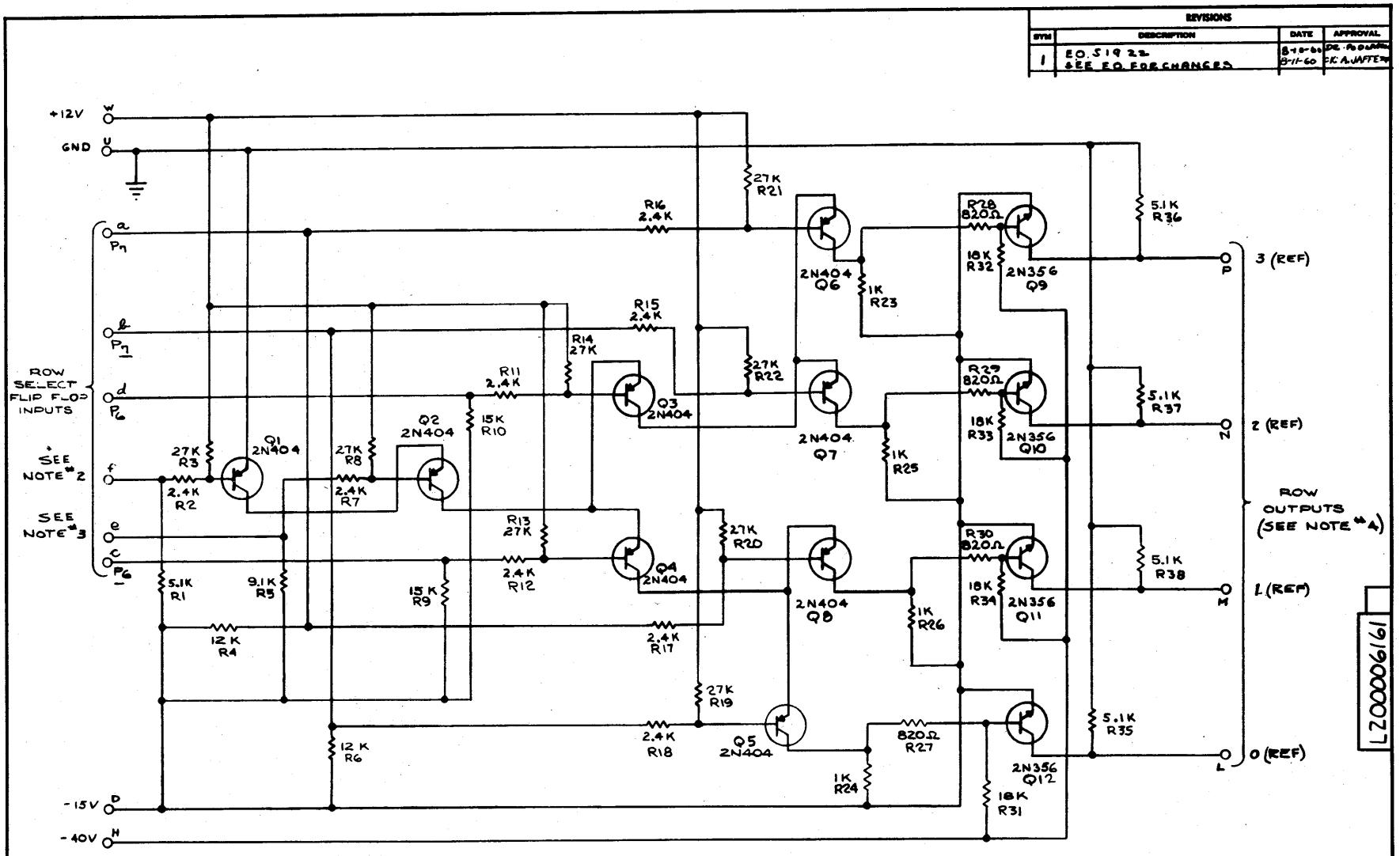
SCHEMATIC
MAIN MEMORY
HEAD MATRIX

SCALE | UNIT WT.

L200006484

L200006484

DRAWING 4



REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
1	EO. 519122 SEE EO FOR CHANGES	8-10-60 9-11-60	DE. R.D.M. C.K. A. JAFFE

4. OUTPUT CONNECTIONS: CARD 11 - ROW 0, 1, 2, & 3; CARD 12 - ROW 4, 5, 6 & 7; CARD 13 - ROW 8, 9, 10 & 11; CARD 14 - ROW 12, 13, 14 & 15.
3. CONNECT CARD 11 & 13 TO $\overline{P_5}$ & CARD 12 & 14 TO P_3.
2. CONNECT CARD 11 & 12 TO $\overline{P_4}$ & CARD 13 & 14 TO P_4.
1. ALL RESISTORS 1/2 W. 5%.

NOTES:

ITEM	SIZE'S	PART NO.	DESCRIPTION	MATL	MATL SPEC	UNIT WT	NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
			LIST OF MATERIAL				L5950000845	4010		
							APPLICATION		QUANTITY REQD.	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON DIMENSIONS: 2 PLACES ± .010, 3 PLACES ± .005, 4 PLACES ± .0005, ANGULAR ± 1°. BREAK EDGES .005 MAX.

MATERIAL

TREATMENT

FINISH

DRAFTSMAN — DATE

CHECKER

ENGINEER — DATE 9/23/60

ENGINEER

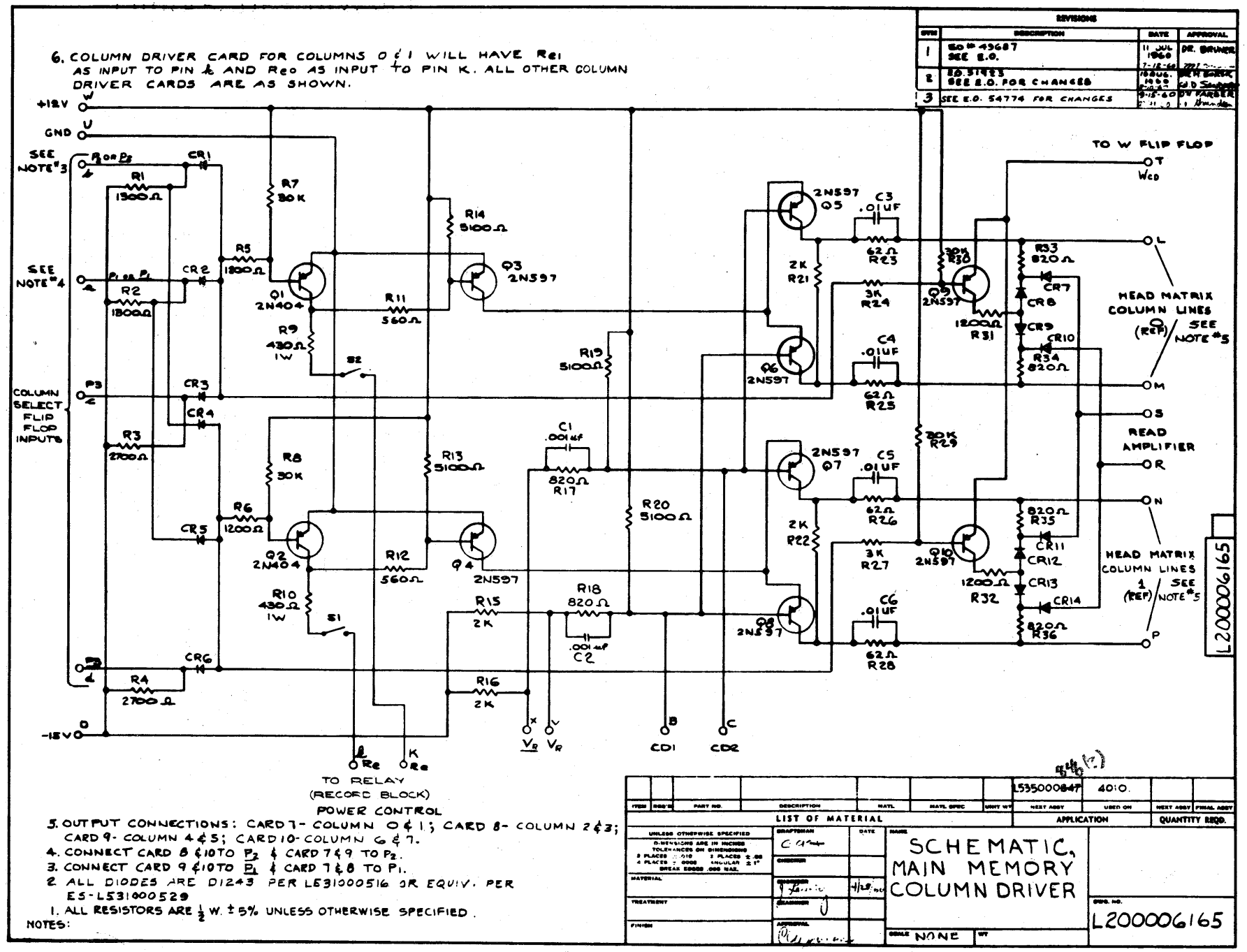
APPROVAL — DATE 11-7-60

NAME: SCHEMATIC, ROW DRIVER

SCALE — WT

DWG. NO. L2000006161

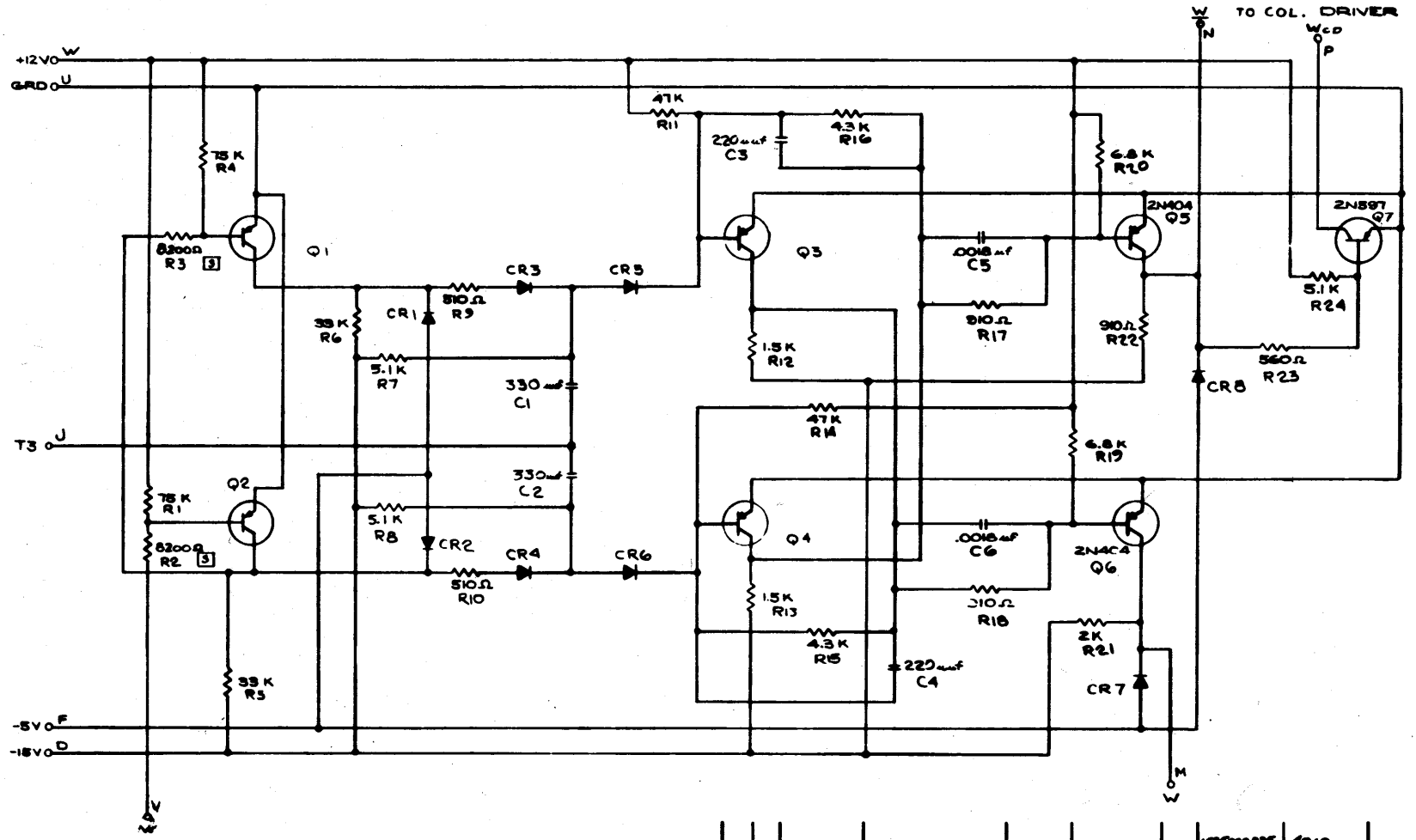
L2000006161


6. COLUMN DRIVER CARD FOR COLUMNS 0 & 1 WILL HAVE Re1 AS INPUT TO PIN & AND Re0 AS INPUT TO PIN K. ALL OTHER COLUMN DRIVER CARDS ARE AS SHOWN.
REVISIONS
1 SO # 49687 SEE E.O. 11 JUL 1960 DR. BRUNER
2 SO 51823 SEE E.O. FOR CHANGES 10 AUG. 1960 DR. BRUNER
3 SEE E.O. 54774 FOR CHANGES 9-12-60 DV PARKER
+12V
GND
-15V
SEE NOTE #3
SEE NOTE #4
COLUMN SELECT FLIP FLOP INPUTS
P1 or P2
P3
R1 1500Ω
R2 1800Ω
R3 2700Ω
R4 2700Ω
CR1
CR2
CR3
CR4
CR5
CR6
R5 1200Ω
R6 1200Ω
R7 30K
R8 30K
R9 430Ω 1W
R10 430Ω 1W
R11 560Ω
R12 560Ω
R13 5100Ω
R14 5100Ω
R15 2K
R16 2K
R17 820Ω
R18 820Ω
R19 5100Ω
R20 5100Ω
C1 .001 MF
C2 .001 MF
Q1 2N404
Q2 2N404
Q3 2N597
Q4 2N597
S1
S2
Re
K Re
TO RELAY (RECORD BLOCK) POWER CONTROL
VR
V VR
B CD1
C CD2
2N597 Q5
2N597 Q6
2N597 Q7
2N597 Q8
2N597 Q9
2N597 Q10
C3 .01 UF
C4 .01 UF
C5 .01 UF
C6 .01 UF
62Ω R23
62Ω R25
62Ω R26
62Ω R28
2K R21
2K R22
3K R24
3K R27
30K R29
30K R30
1200Ω R31
1200Ω R32
R33 820Ω
R34 820Ω
R35 820Ω
R36 820Ω
CR7
CR8
CR9
CR10
CR11
CR12
CR13
CR14
TO W FLIP FLOP
T WCD
L
M
S
READ AMPLIFIER
R
N
P
HEAD MATRIX COLUMN LINES 0 (REF) SEE NOTE #5
HEAD MATRIX COLUMN LINES 1 (REF) SEE NOTE #5
L200006165
5. OUTPUT CONNECTIONS: CARD 7- COLUMN 0 & 1; CARD 8- COLUMN 2 & 3; CARD 9- COLUMN 4 & 5; CARD 10- COLUMN 6 & 7.
4. CONNECT CARD 8 & 10 TO P2 & CARD 7 & 9 TO P2.
3. CONNECT CARD 9 & 10 TO P1 & CARD 7 & 8 TO P1.
2. ALL DIODES ARE D1243 PER L531000516 OR EQUIV. PER ES-L531000529
1. ALL RESISTORS ARE 1/2 W. ± 5% UNLESS OTHERWISE SPECIFIED.
NOTES:
L535000847 4010.
LIST OF MATERIAL
APPLICATION
QUANTITY REQD.
SCHEMATIC, MAIN MEMORY COLUMN DRIVER
SCALE NONE
DWG. NO. L200006165

NOTE:

1. ALL RESISTORS 1/2 WATT 5%
2.
3. ALL DIODES SYLVANIA D1243 OR EQUIV PER L200006440
4. Q1, Q2, Q3 & Q4 ARE 2N1301 OR EQUIV PER L200006441.

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
1	EO# 49529 SEE EO FOR CHANGES	6-21-66	DR. BRUNER
2	EO 51419 SEE EO FOR CHANGES	8-4-66	
3-2	REVISED PER E.O. 56877		



LIST OF MATERIAL	APPLICATION	QUANTITY REQD.

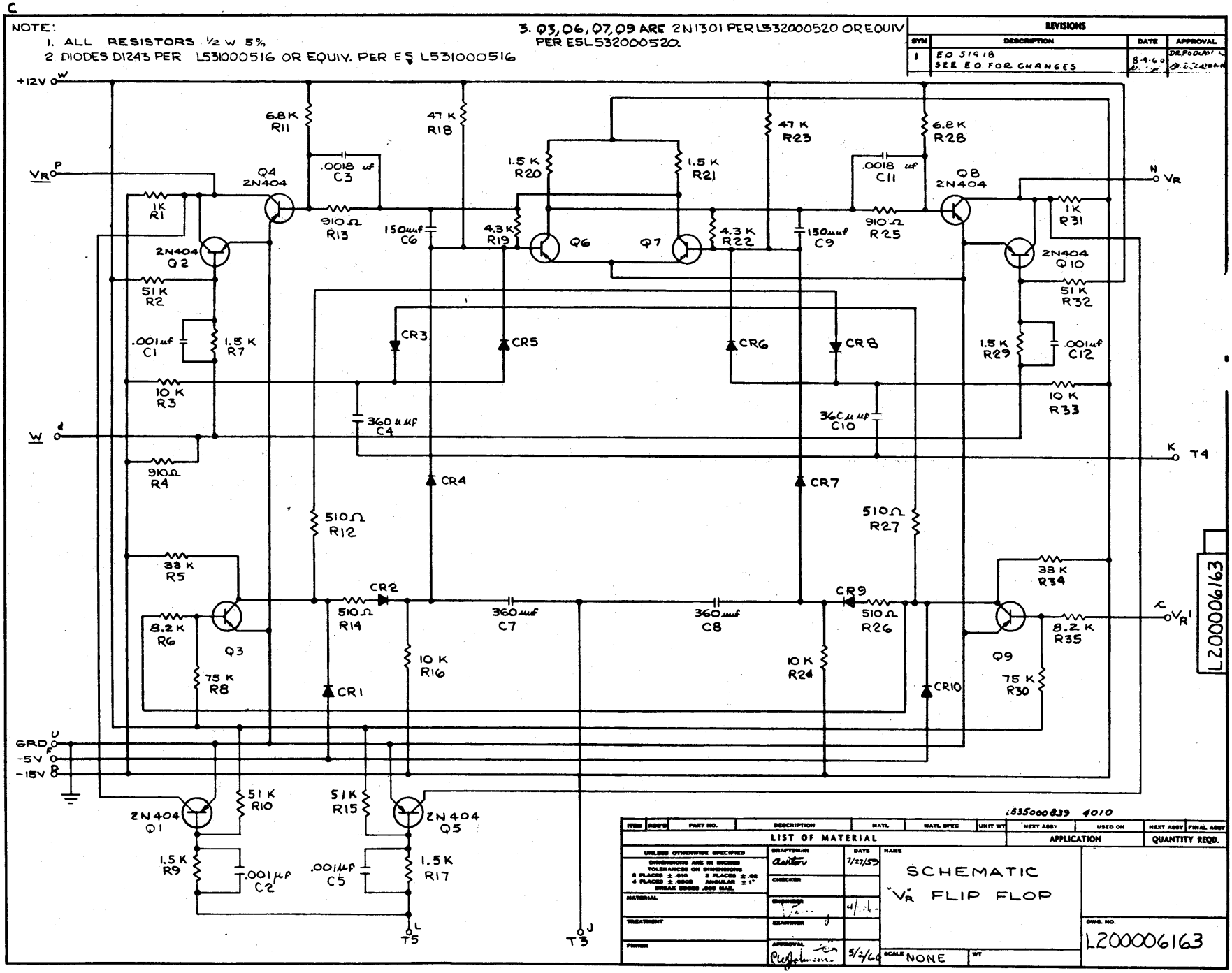
SCHEMATIC, W FLIP-FLOP

L200006056

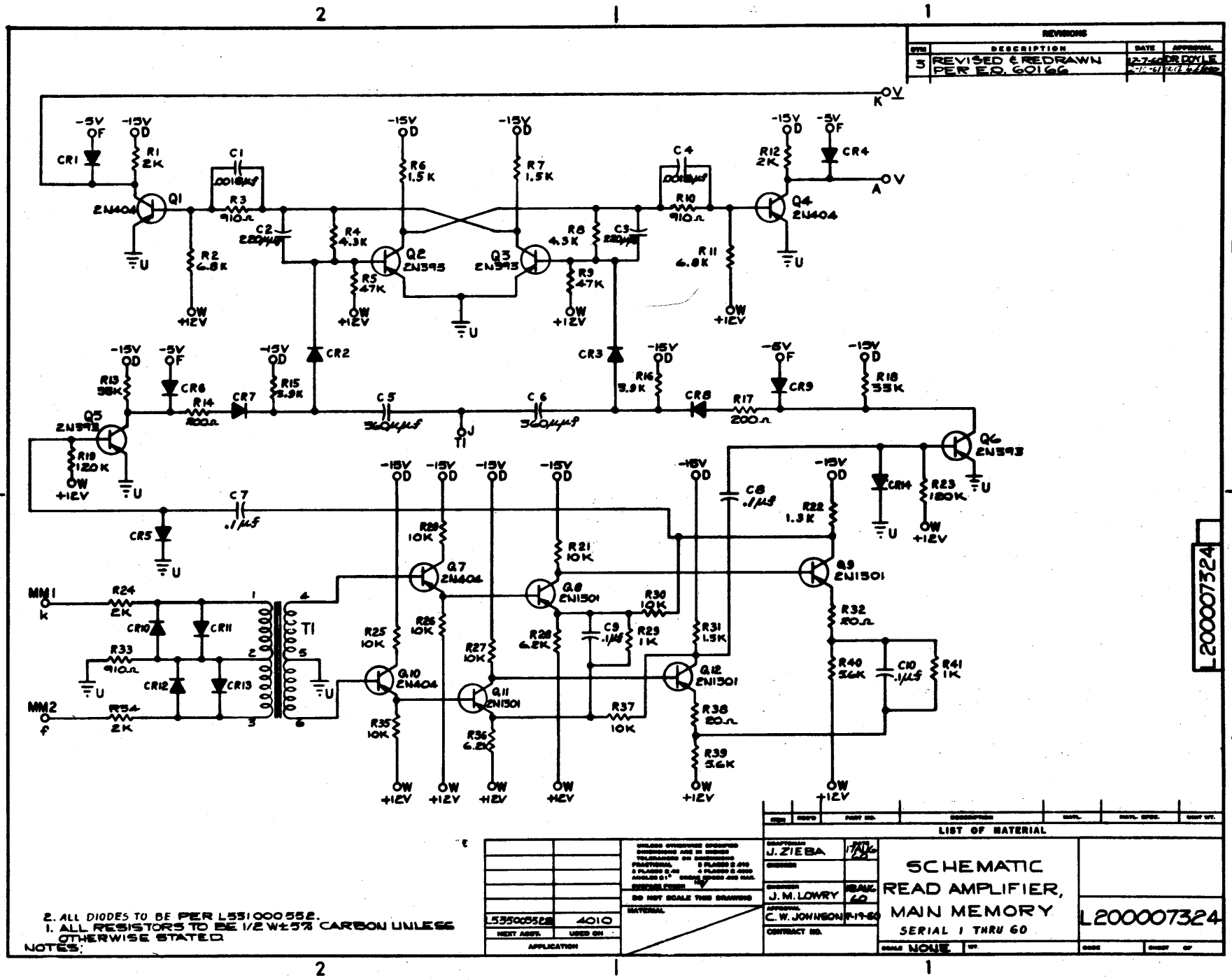
L200006056

B

2 1


NOTE:
1. ALL RESISTORS ½ W 5%
2. DIODES D1243 PER L531000516 OR EQUIV. PER ES L531000516
3. Q3, Q6, Q7, Q9 ARE 2N1301 PER L532000520 OR EQUIV PER ESL532000520.
REVISIONS
SYM | DESCRIPTION | DATE | APPROVAL
1 | ED. 51918 SEE EO FOR CHANGES | 8-9-60
+12V
VR
W
GRD
-5V
-15V
Q1 2N404
Q2 2N404
Q3
Q4 2N404
Q5 2N404
Q6
Q7
Q8 2N404
Q9
Q10 2N404
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
CR10
T3
T4
T5
VR'
LIST OF MATERIAL
SCHEMATIC "VR" FLIP FLOP
L200006163
SCALE NONE

DRAWING 9 A4-16



NOTES:
1. ALL RESISTORS TO BE 1/2 W ±5% CARBON UNLESS OTHERWISE STATED.
2. ALL DIODES TO BE PER L551000552.

LIST OF MATERIAL

L550005528	4010
NEXT ASSY.	USED ON
APPLICATION	

DO NOT SCALE THIS DRAWING

DRAFTSMAN	J. ZIEBA	11 AUG 60
ENGINEER	J. M. LOWRY	11 AUG 60
APPROVAL	C. W. JOHNSON	8-19-60
CONTRACT NO.		

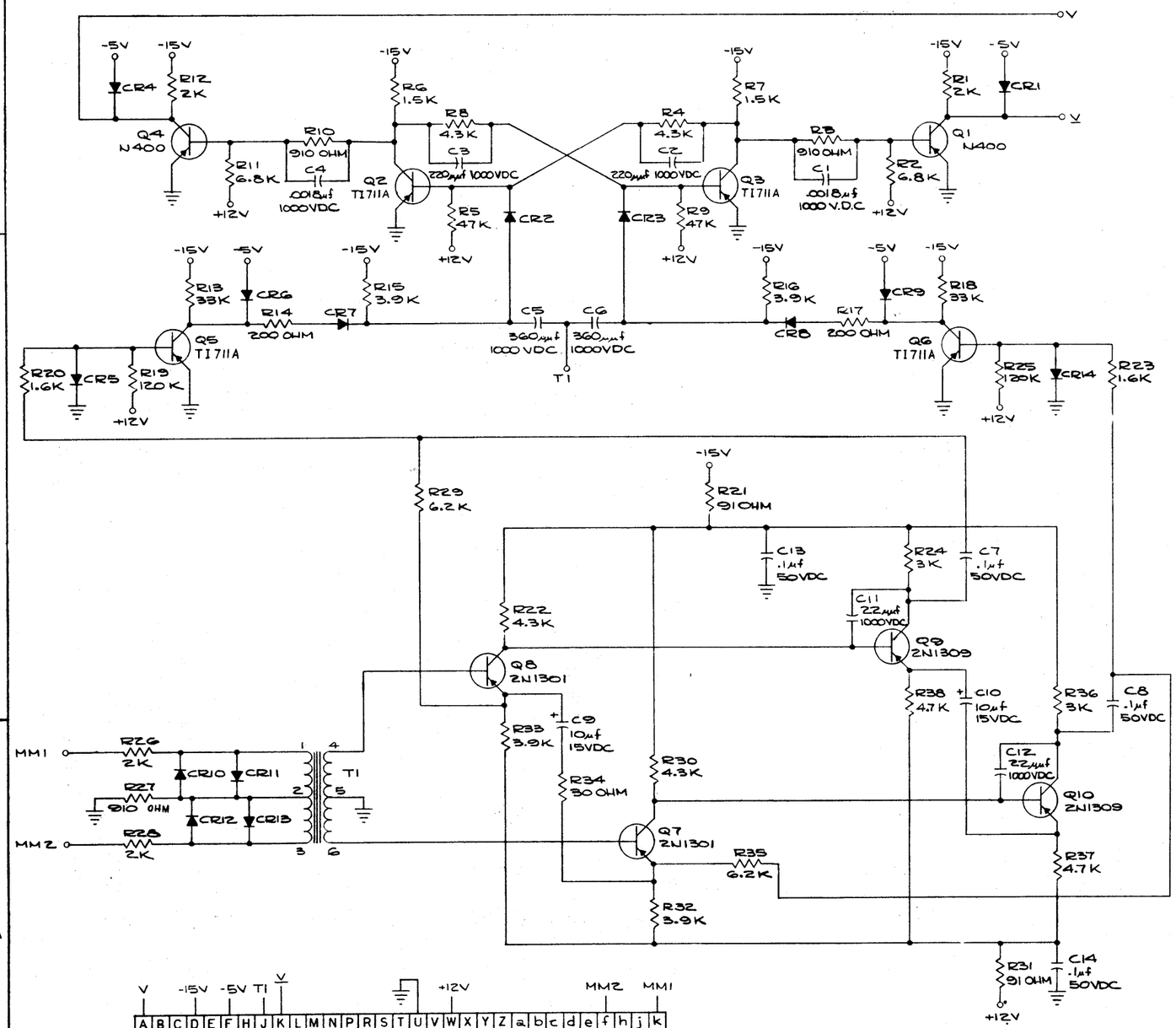
SCHEMATIC READ AMPLIFIER, MAIN MEMORY
SERIAL 1 THRU 60

L200007324

SCALE NONE

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
1.	REVISED PER E068447	20 NOV 31	J. Hartford
2	REVISED PER E.O. 68519	19 DEC 31	J. Hartford

L200 009 985



NOTES

1. ALL RESISTORS TO BE 1/2W, ±5%.
2. DIODES TO BE PER L531 000 552.

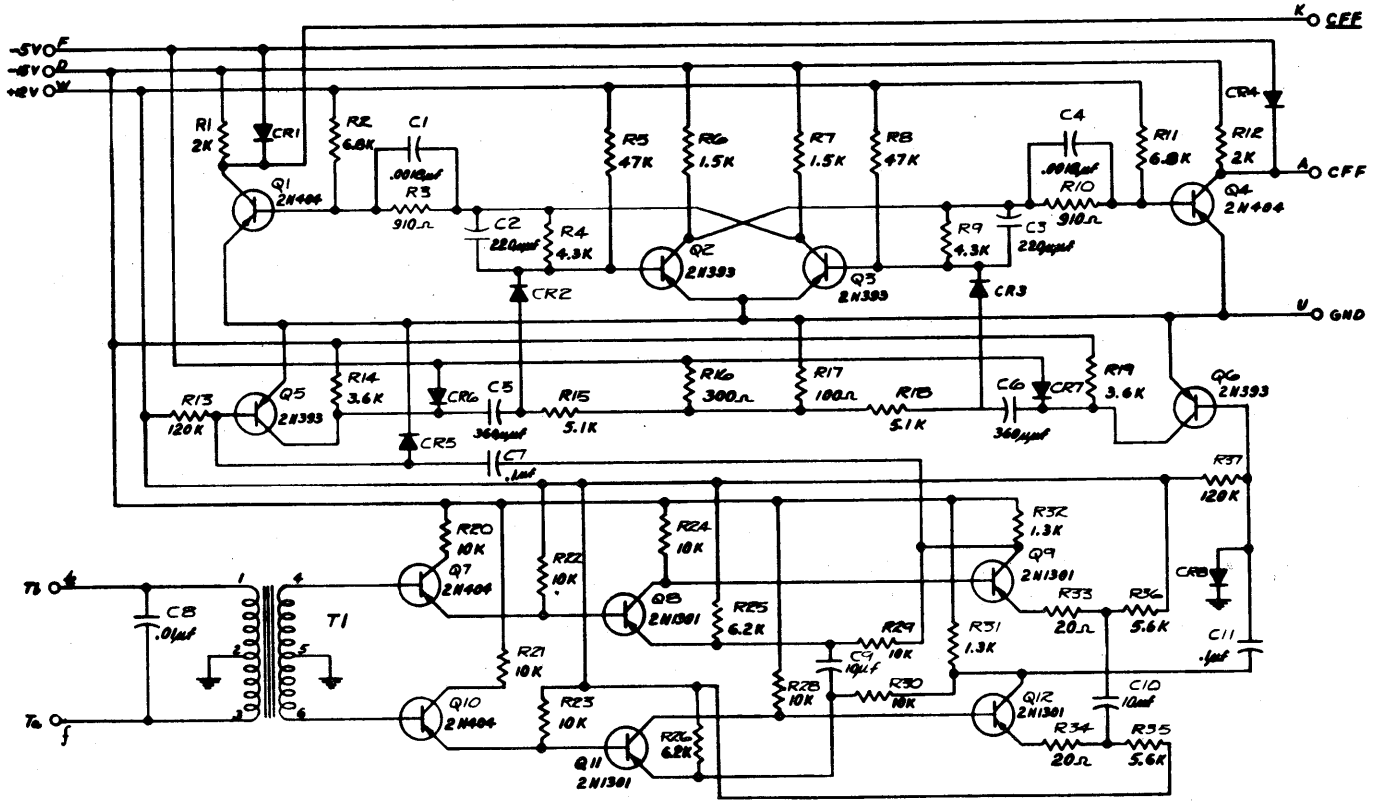
L200 009 985

L535003709	A010	DRAFTSMAN	DATE 31 JUNE
NEXT ASSY.	USED ON	CHECKER	
APPLICATION		ENGINEER	
		APPROVAL	
		CONTRACT NO.	

SCHEMATIC
READ AMPLIFIER
MAIN MEMORY
SERIAL 61 & UP

L200 009 985

SCALE | WT. | CODE | SHEET OF



REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
2	REVISED & REDRAWN PER EO. 56979		

2. DIODES TO BE PER L531000552.
1. ALL RESISTORS TO BE 1/2W ±5% CARBON UNLESS OTHERWISE STATED.

NOTES:

LIST OF MATERIAL

ITEM	REV'D	LIBRASCOPE NO.	DESCRIPTION	DATE	DATE SPEC.	UNIT WT.

L335000849	4010
NEXT ASSY.	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON DIMENSIONS: FRACTIONAL ± 2 PLACES ± .010, 3 PLACES ± .005, 4 PLACES ± .0050; ANGLES ± 1°; SURFACE FINISH: [illegible]

DO NOT SCALE THIS DRAWING

MATERIAL

DRAFTSMAN	J. ZIEBA	10 Nov 1960
CHECKER		
ENGINEER	J.M. Lowry	10 Nov 1960
APPROVAL	C.W. Johnson	11-10-60
CONTRACT NO.		

SCHEMATIC
READ AMPLIFIER
CLOCK
SERIAL 1 THRU 60

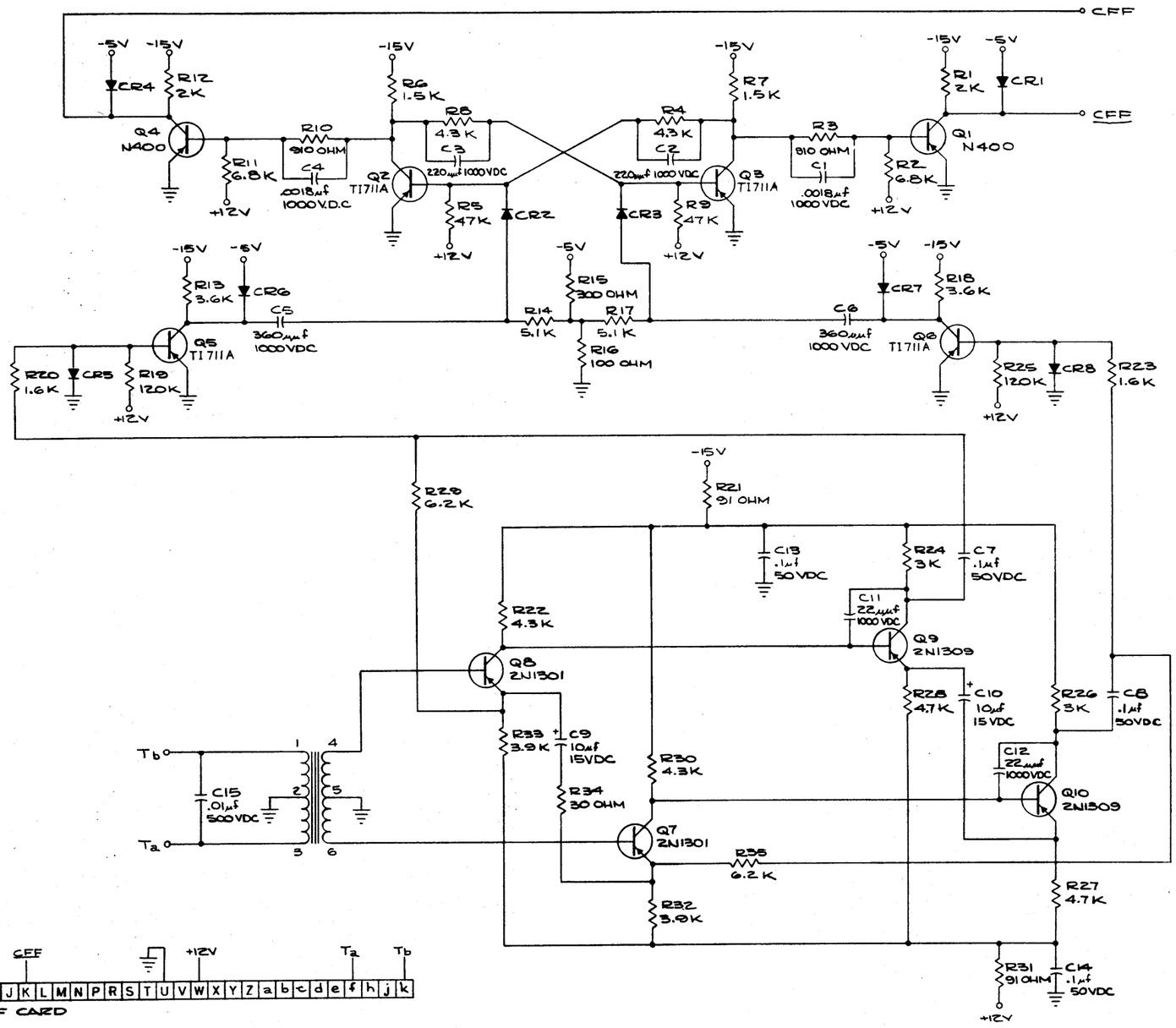
SCALE | UNIT WT.

L200 006 160

L200 006 160

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
1.	REVISED PER EO 68439	20 NOV 69	
2	REVISED PER EO 68517	29 DEC 69	

L200009983



E. O'S ATTACHED

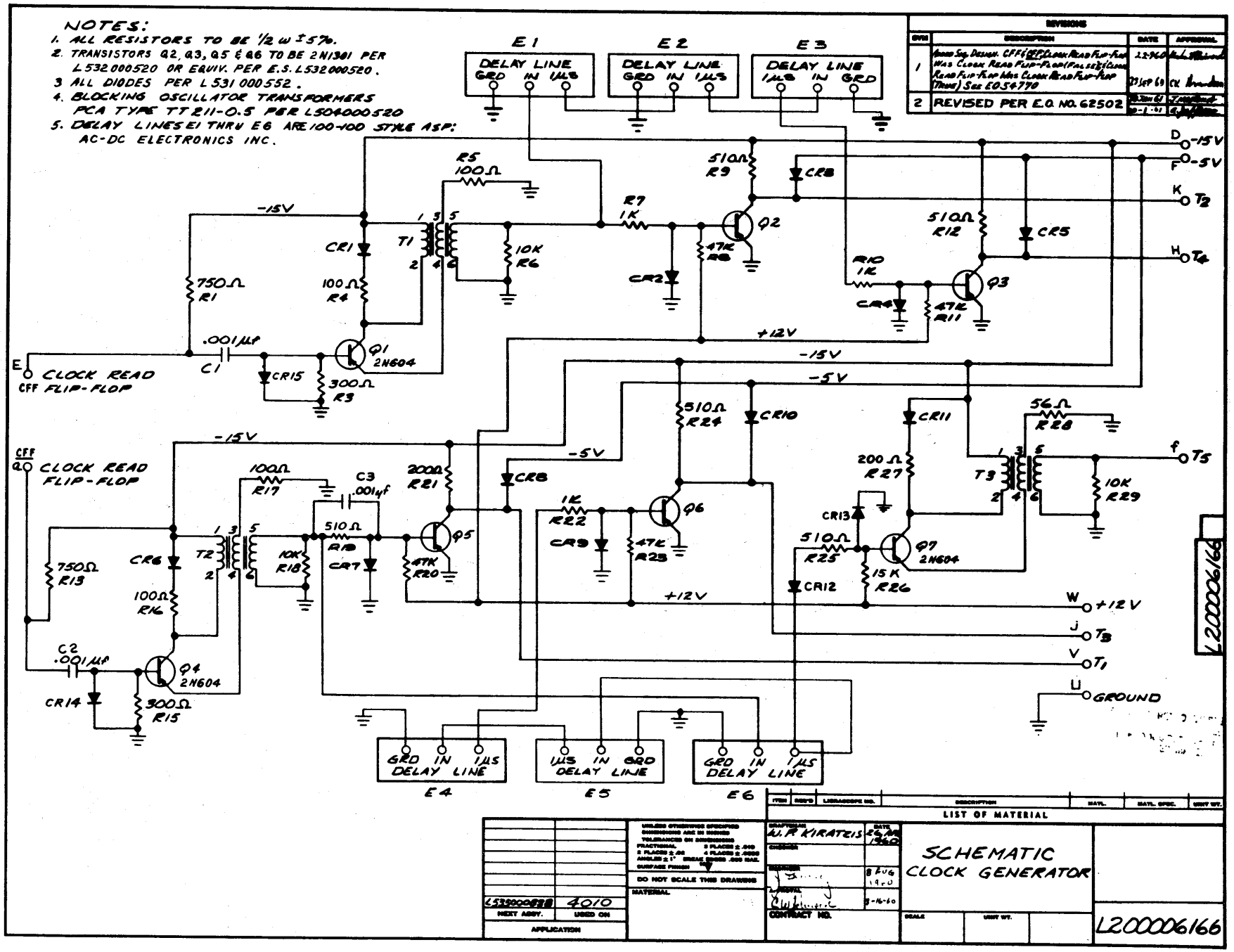
NOTES:
1. ALL RESISTORS TO BE 1/2 W, ±5%.
2. DIODES TO BE PER L551 000 552.

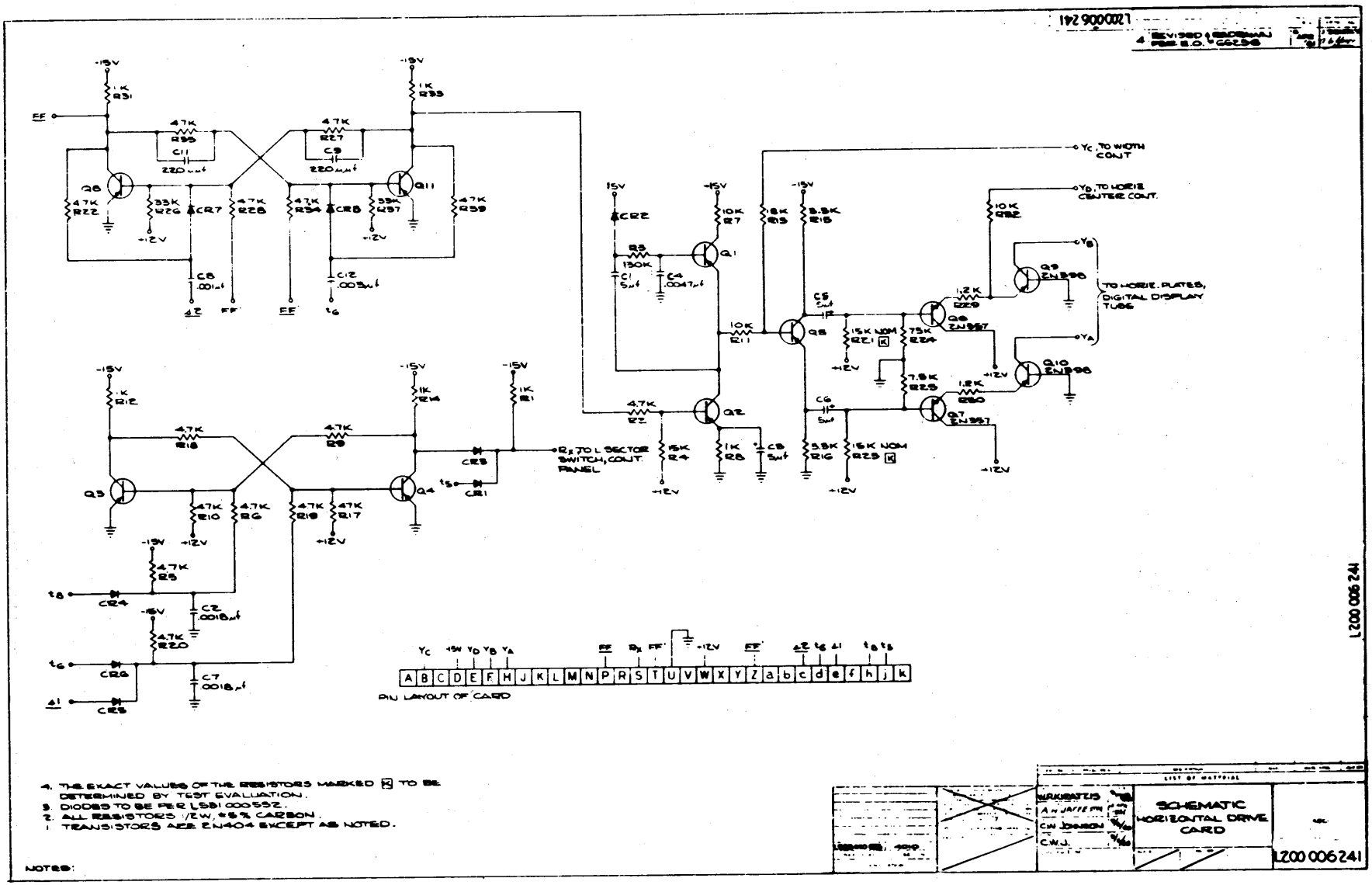
L556 OR 8 TOT	4010	DRAFTSMAN	DATE 25 JUNE 69
HDBY ASSY.	USED ON	ENGINEER	DATE 25 JUNE 69
APPLICATION		CONTRACT NO.	DATE 7/7/69

SCHEMATIC
READ AMPLIFIER
CLOCK
SERIAL 61 & UP

L200009983

SHEET 1 OF 1


NOTES:
1. ALL RESISTORS TO BE 1/2 w ±5%.
2. TRANSISTORS Q2, Q3, Q5 & Q6 TO BE 2N1301 PER L532000520 OR EQUIV. PER E.S. L532000520.
3 ALL DIODES PER L531000552.
4. BLOCKING OSCILLATOR TRANSFORMERS PCA TYPE TT211-0.5 PER L504000520
5. DELAY LINES E1 THRU E6 ARE 100-100 STYLE ASP: AC-DC ELECTRONICS INC.
REVISIONS
1
2 REVISED PER E.O. NO. 62502
E1 DELAY LINE GRD IN 1µS
E2 DELAY LINE GRD IN 1µS
E3 DELAY LINE 1µS IN GRD
R5 100Ω
510Ω R9
CR8
R7 1K
Q2
510Ω R12
CR5
R10 1K
Q3
47K R11
CR4
CR1
T1
10K R6
CR2
47K R8
750Ω R1
100Ω R4
.001µF C1
Q1 2N604
CR15
300Ω R3
E CLOCK READ CFF FLIP-FLOP
-15V
-5V
+12V
D -15V
F -5V
K T2
H T4
510Ω R24
CR10
CR11
56Ω R28
200Ω R27
T3
10K R29
f T5
CR13
510Ω R25
Q7 2N604
15K R26
CR12
W +12V
J T3
V T1
U GROUND
CFF Q CLOCK READ FLIP-FLOP
100Ω R17
C3 .001µF
200Ω R21
CR8
1K R22
Q6
CR9
47K R23
510Ω R19
CR7
47K R20
Q5
T2
CR6
100Ω R16
750Ω R13
10K R18
C2 .001µF
Q4 2N604
CR14
300Ω R15
GRD IN 1µS DELAY LINE E4
1µS IN GRD DELAY LINE E5
GRD IN 1µS DELAY LINE E6
LIST OF MATERIAL
DO NOT SCALE THIS DRAWING
L533000838 4010
NEXT ASSY. USED ON
APPLICATION
CONTRACT NO.
SCHEMATIC CLOCK GENERATOR
L200006166



4. THE EXACT VALUES OF THE RESISTORS MARKED [K] TO BE DETERMINED BY TEST EVALUATION.
3. DIODES TO BE PER L5810005Z.
2. ALL RESISTORS 1/2 W, ±5% CARBON.
1. TRANSISTORS ARE 2N404 EXCEPT AS NOTED.

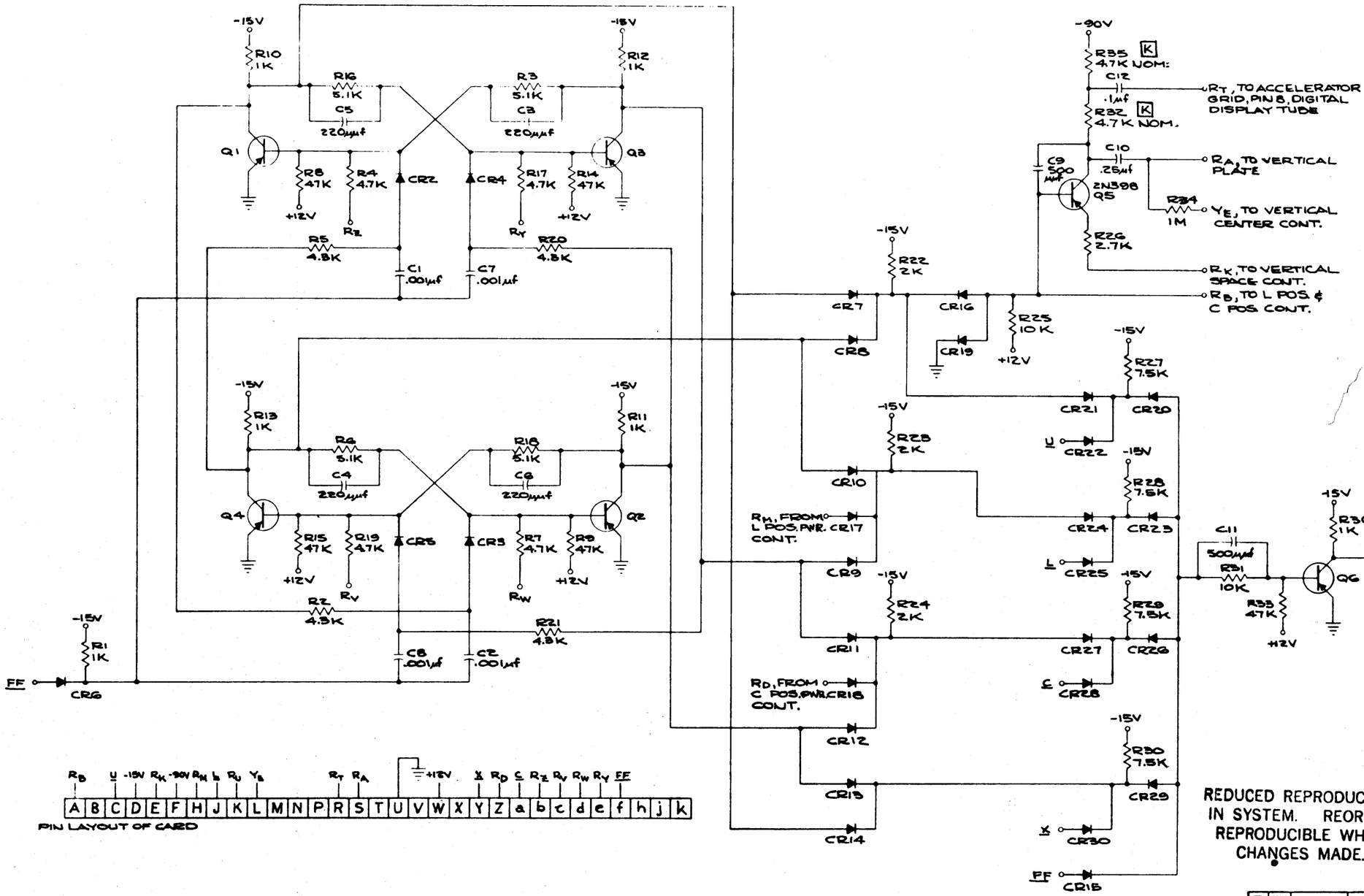
NOTES:

DRAWN BY		SCHEMATIC HORIZONTAL DRIVE CARD	
A. H. JAFFE			
CW JOHNSON			
C.W.J.			L200 006241

L200 006241

L200006242

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
3	REVISED & REDRAWN PER E.O. 65420	APR 6[illegible]	



RB U -15V RK -90V RH L RU YE RT RA +12V X RD C RZ RV RW RY FF

A B C D E F H J K L M N P R S T U V W X Y Z a b c d e f h j k

PIN LAYOUT OF CARD

4. DIODES TO BE PER L5310005552.
3. THE EXACT VALUES OF THE RESISTORS MARKED [K] TO BE DETERMINED BY TEST EVALUATION.
2. ALL RESISTORS ARE 1/2W ± 5% CARBON
1. TRANSISTORS ARE 2N404 EXCEPT AS NOTED.

NOTES

REDUCED REPRODUCIBLE IN SYSTEM. REORDER REPRODUCIBLE WHEN CHANGES MADE.

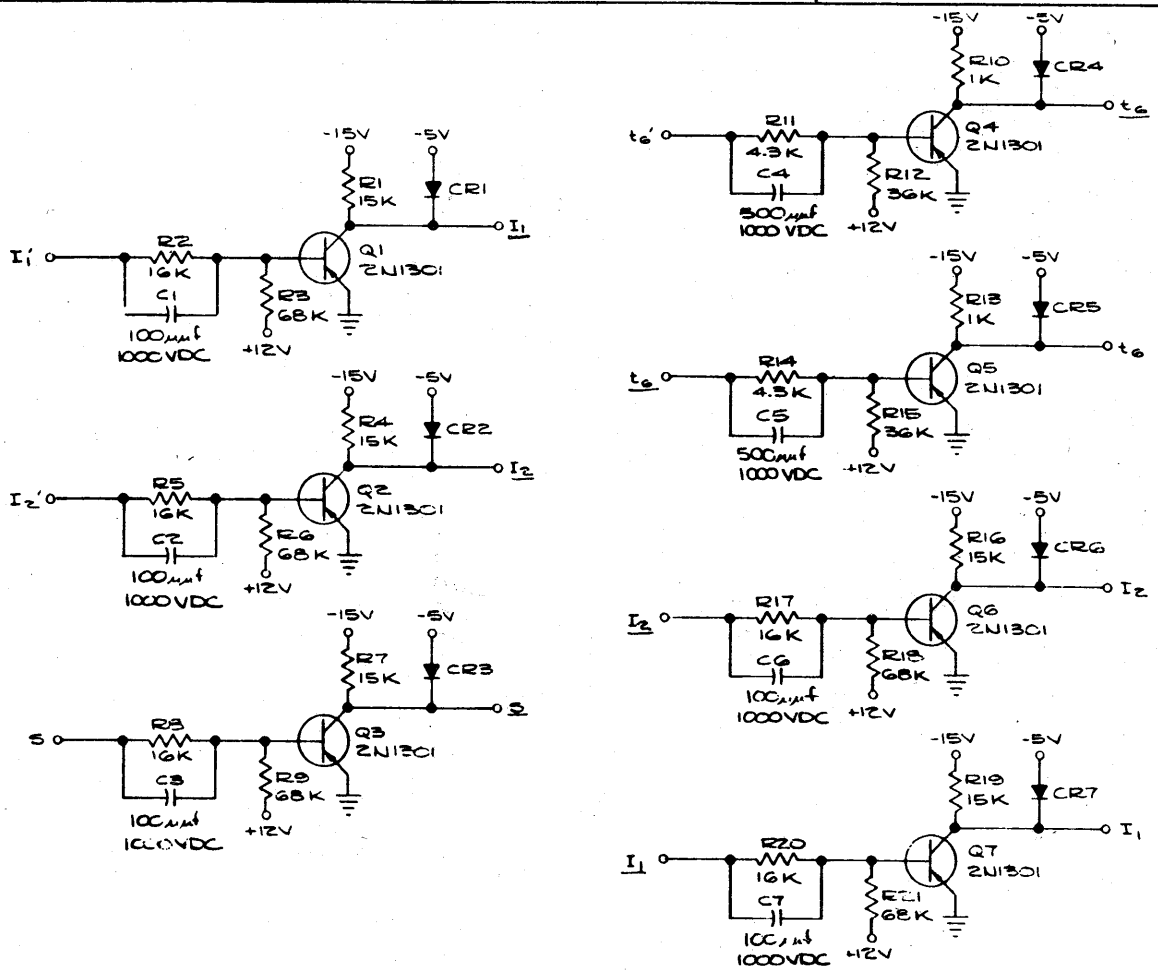
LIST OF MATERIAL

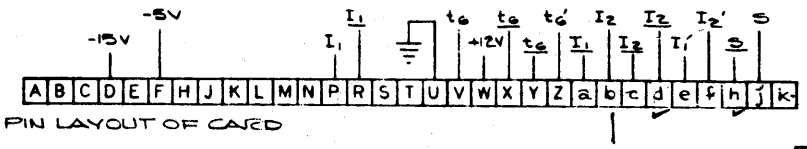
DRAFTSMAN	W.P. KIRATZIS
ENGINEER	C.W. JOHNSON
APPROVAL	C.W.J.
CONTRACT NO.	
DO NOT SCALE THIS DRAWING	
MATERIAL	
L5350005558 / NEXT ASSY	4010 / USED ON
APPLICATION	

SCHEMATIC VERTICAL DRIVE CARD

L200 006 242

L200006242





REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
2	REVISED & REDRAWN PER E.O. 65935	5-2nd/61 5-1-61	DR. GEARY

NOTES:
1. ALL RESISTORS ARE 1/2 W. ±5%.
2. DIODES TO BE PER L531 000 552.

DRAFTSMAN	ASHTON	7/6/60
CHECKER		
ENGINEER	C.W. JOHNSON	9/6/60
APPROVAL	C.W.J.	9/6/60
CONTRACT NO.		
NEXT ASSY.	USED ON 4010	

SCHEMATIC
INVERTER
CARD

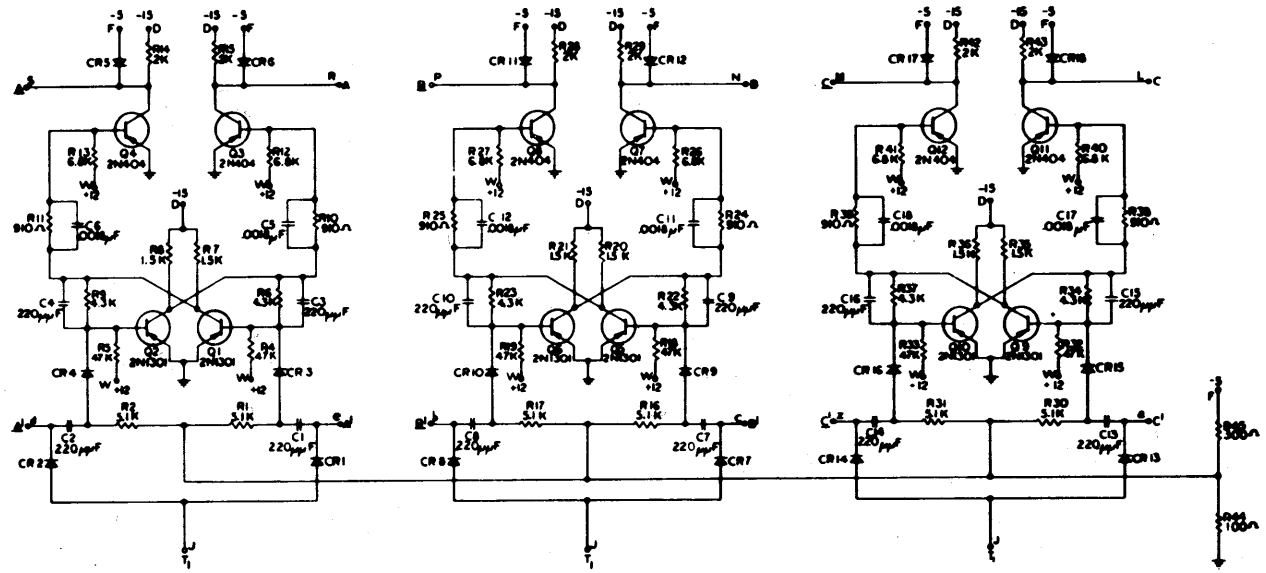
L200006164

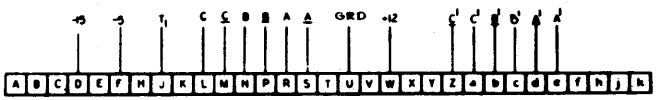
L200006164

NOTES:

1. ALL DIODES, SYLVANIA D1243 PER L531000516 OR EQUIV. PER ES-L531000516
2. ALL RESISTORS ½ W ± 5 %
3. TRANSISTORS 2N1301 PER L532000520 OR EQUIV PER ES-L532000520.
4. TRANSISTORS 2N404 PER L532000087 OR EQUIV. PER ES-L532000087.

REVISIONS			
ZONE	DESCRIPTION	DATE	APPROVAL
1	REVISED PER E.O. # 54709	10-11-60	DUBANT





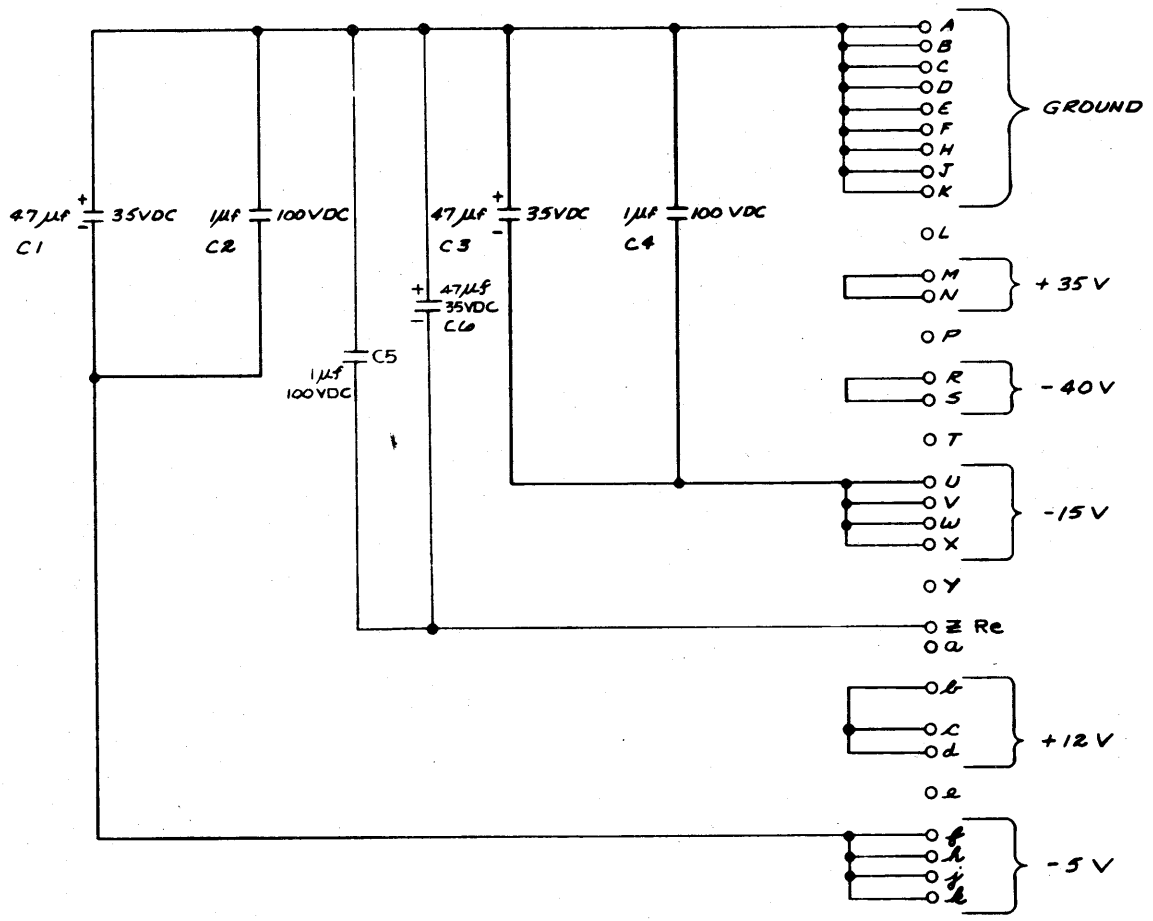
REDUCED REPRODUCIBLE IN SYSTEM. REORDER REPRODUCIBLE WHEN CHANGES MADE.

			LIST OF MATERIAL		
			C. A. H		SCHEMATIC, TRIPLE FLIP-FLOP
			L. WALTER JOHNSON 4/13/60		
L535000847	4010				L200006167
NEXT ASSY.	USED ON				
APPLICATION		DO NOT SCALE THIS DRAWING	CONTRACT NO.	SCALE NONE	SHEET 1 OF 1

L200006167

NOTES:
1. CAPACITORS C2 & C4 ARE FIXED, FILM-DIELECTRIC PER L6050001571 OR EQUIV.
2. CAPACITORS C1 & C3 ARE FIXED-ELECTROLYTIC PER L6050000750 OR EQUIV.

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
1	E.O. 51920 SEE E.O. FOR CHANGES	8/18/60 8-9-60	DR. DOYLE R. JAFFESON
2	Was 2, Added A Terminal To +12 V Bracket. See EO 51969	9-12-60 9-23-60	DR. FARBER R.O.



L200007293 2

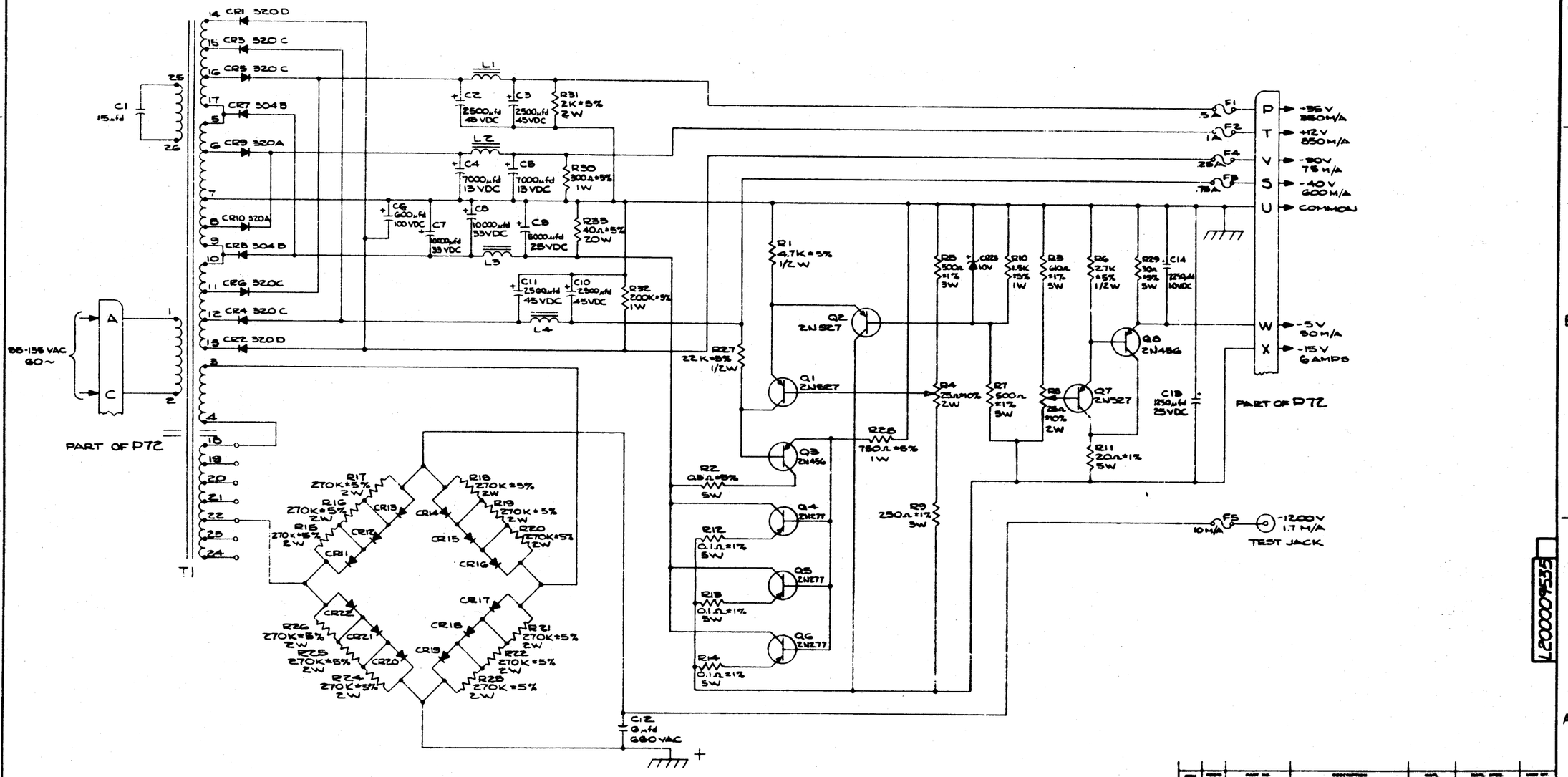
LIST OF MATERIAL

DRAWN W.P. KIRATZIS	DATE 2 June 1960	SCHEMATIC POWER DISTRIBUTION	
CHECKED			
ENGINEER	13 June 1960		
APPROVED	9/1/60		
CONTRACT NO.		SCALE	UNIT WT.
L585000892	4010		L200007293
NEXT ASSY.	USED ON		
APPLICATION			

DO NOT SCALE THIS DRAWING

MATERIAL

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
1	REVISED & REDRAWN PER E.O. G2846	16 FEB '61	



1 SCHEMATIC REFERENCE: POWER EQUIPMENT CO., GALION, OHIO.

NOTES:

L200009535

LIST OF MATERIAL			
HARRIS	SCHEMATIC POWER SUPPLY		L200009535
L200002286 4010			

DRAWING 20 A4-33

REVISIONS			
DASH	DESCRIPTION	DATE	APPROVED
2	ADDED SHEET 2 PER E.O. 68463		

L200 009535

SECTION 5 — CR6 320-F — C13 250 100VDC, R6 0.1 MEG .5W — F6 1/16 AMP

SECTION 3 — CR5 320-C — L4 — C11 1000 45VDC, C12 1000 45VDC, R5 6800 OHM 1W — F5 3/4 AMP

SECTION 4 — CR4 320-B — L3 — C9 1000 45VDC, C10 1000 45VDC, R4 900 OHM 5W — F4 1/2 AMP

SECTION 1 — CR3 320-A — L2 — C7 1900 15VDC, C8 1900 15VDC, R3 150 OHM 2W — F3 1 AMP

SECTION 2 — CR2 320-A — L6 — C5 70,000 6VDC, C6 70,000 6VDC, R2 220 OHM 1W — F2 5 AMP — R8 50 HM 10W

L1 — C3 0.1 2000V, C4 1.0 1500V, R1 9 MEG 2W — -1200V TEST JACK

T1 — C1 .12 660VAC — T3 — F1 1/16 AMP — CR1 IN1696

80-135 VAC 60~ — A, C — PART OF PT2

T2 — CR7 304-A — C2 .12 660VAC — L5 — C14 10000 25VDC, C15 10000 25VDC, C16 10000 25VDC, C17 10000 25VDC, R7 250 OHM 5W — F7 7 AMP

V -90V
S -40V
P +35V
T +12V
W -5V
X -15V
U GRD

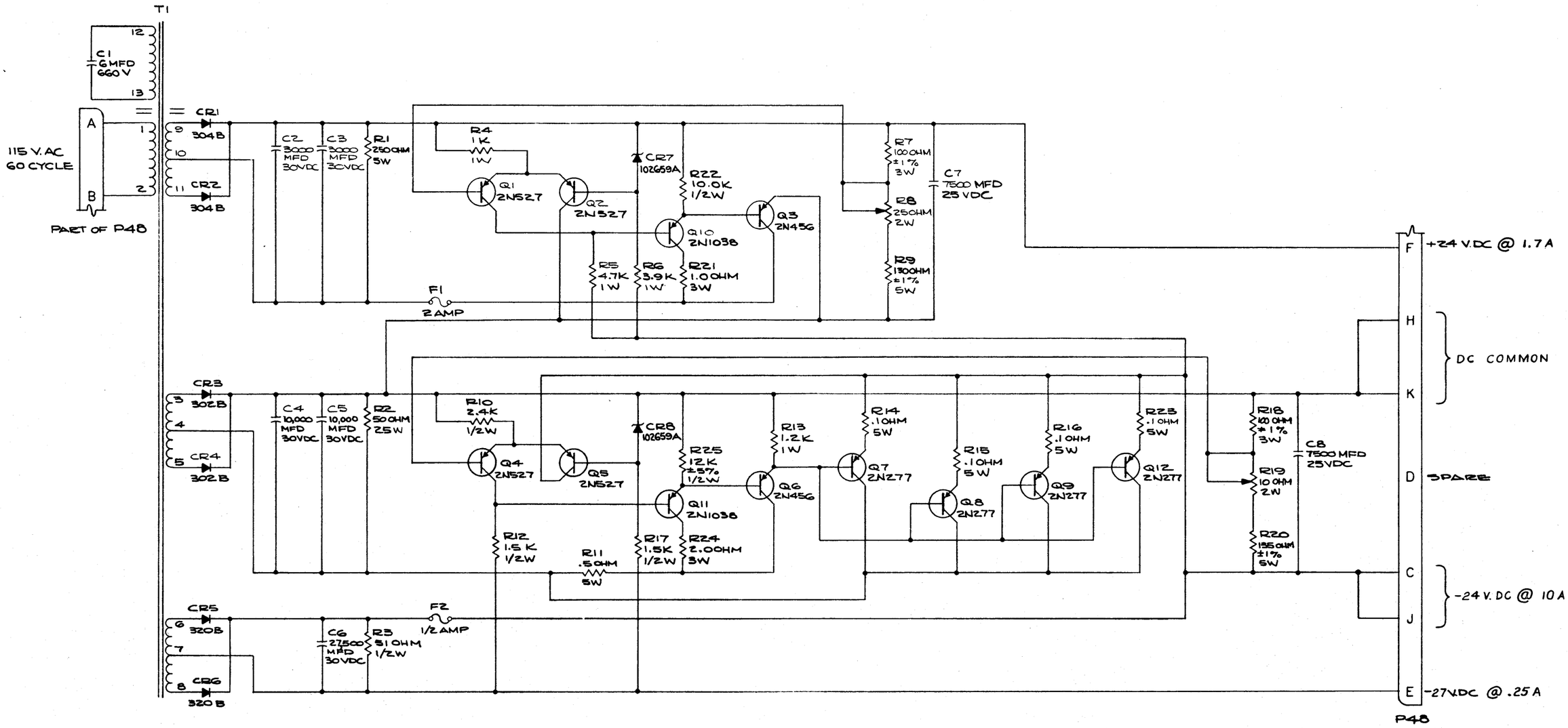
PART OF PT2

2. ALL CAPACITORS ARE IN μfd.
1. SCHEMATIC REFERENCE: ACME ELECTRIC CORP'N, CUBA, N.Y. POWER SUPPLY TYPE 41090

NOTES: UNLESS OTHERWISE SPECIFIED.

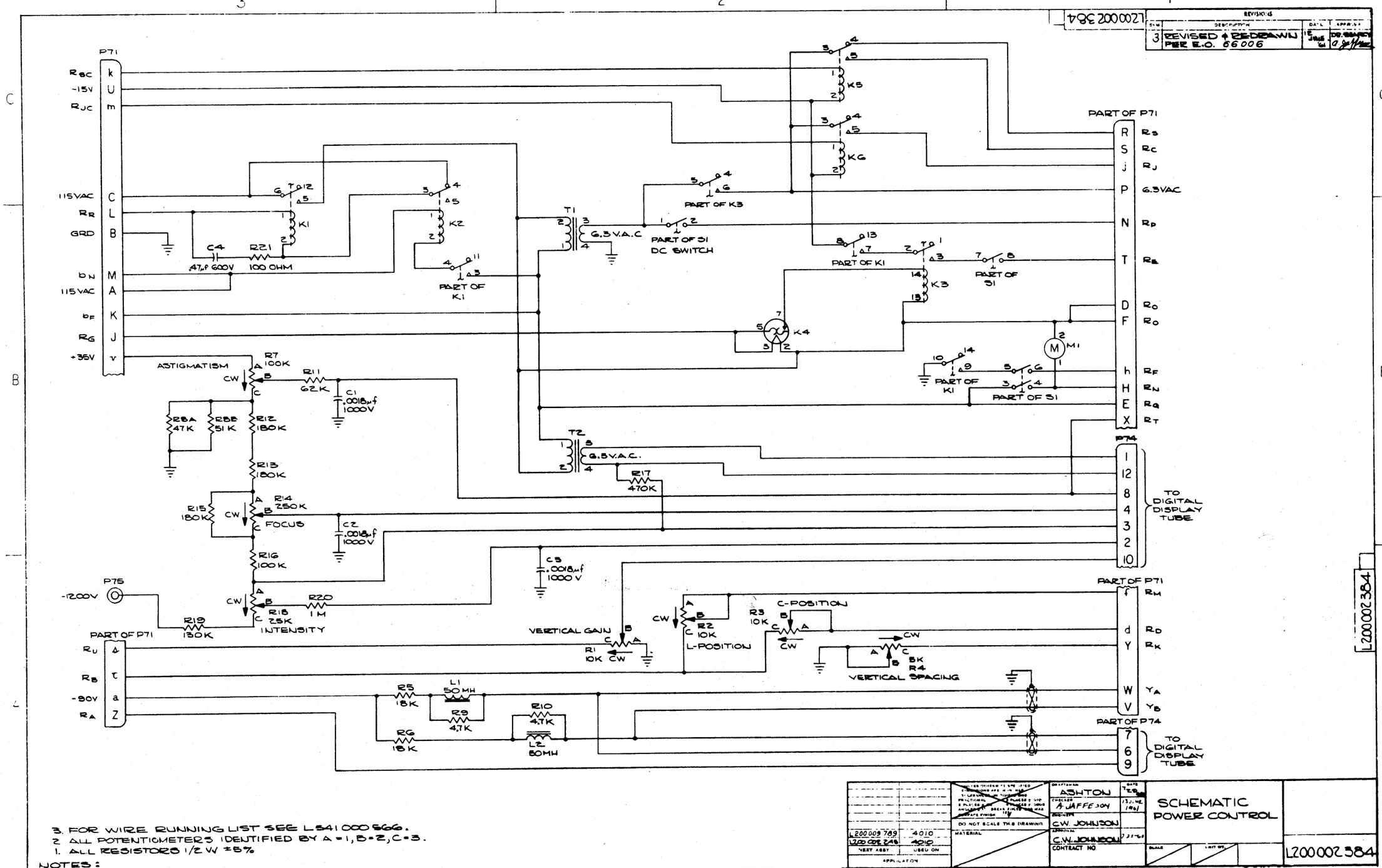
L200002786	40IC	T. Searcy	8-5-61	SCHEMATIC POWER SUPPLY SER. 61 & UP	L200009535
NEXT ASSY	USED ON	A. Heath	27 JULY 1961		
APPLICATION		CONTRACT NO.		SCALE	SHEET 2 OF 2

L200009535



1. SCHEMATIC REFERENCE : POWER EQUIPMENT CO. GALION PLANT - GALION, OHIO

NOTES:



NOTES:

3. FOR WIRE RUNNING LIST SEE L541000566.
2. ALL POTENTIOMETERS IDENTIFIED BY A=1, B=2, C=3.
1. ALL RESISTORS 1/2 W ±5%

REVISIONS			
DWG	DESCRIPTION	DATE	APPROVED
3	REVISED & REDRAWN PER E.O. 66006	15 JUNE 64	

L200002384

L200009769	4010	
L200004248	4010	
NEXT ASSY	USED ON	
APPLICATION		

DO NOT SCALE THIS DRAWING

MATERIAL

DRAFTSMAN	ASHTON	DATE 7-29-64
CHECKED	A. JAFFE 30N	13 JUNE 1961
ENGINEER	C.W. JOHNSON	
APPROVAL	C.W. JOHNSON	7-31-64
CONTRACT NO		

SCHEMATIC POWER CONTROL

L200002384

DRAWING 23

A4-39

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
5	INCORPORATED E.O. 62670 - REVISED & REDRAWN PER E.O. 66012	11 MAY 61 / 5 MAY 1961	NE SEARCH / CH

S1 POWER OFF

DS1 COMPUTE

DS2 STOP

S/DS2 POWER ON

VERT. POS. 500K R3

HORIZ. POS. 10K R2

S/DS10 START COMPUTE

S/DS 9 ONE OPERATION

S/DS 8 SET INPUT MODE

S/DS 7 EXECUTE LOWER ACCUMULATOR

S/DS 5 BRANCH CONT.

R1 100K WIDTH

L-SECTOR DISPLAY SWITCH

S17 A B C

S/DS11 SENSE 1

S/DS 12 SENSE 2

S/DS13 SENSE 4

S/DS14 SENSE 8

S/DS15 SENSE 16

S/DS16 SENSE 32

S18 RECORD COL-0

S19 COL-1

6.3VAC

P73

PART OF P73

HORIZ. CONT.

FROM HORIZ. DRIVE CARD

TO VERTICAL DRIVE CARD

POWER CONT. FROM HORIZ. DRIVE CARD

NOTES:

1. FOR WIRE RUNNING LIST SEE L841 000 568

DRAWN	L. HANIL 7DH	9/10	LIST OF MATERIAL
CHECKED	A.H. JAFFESON		SCHEMATIC, CONTROL PANEL
ENGINEER	C.W. JOHNSON	5/5/61	
APPROVAL	C.W.J. PT.	5/5/61	
CONTRACT NO.			L200 006 159

DO NOT SCALE THIS DRAWING

MATERIAL

L523 000 568 | 4010 — NEXT ASSY. | USED ON — APPLICATION

L200 006 159

APPENDIX 5

RPC-4500 TYPEWRITER AND READER-PUNCH SCHEMATICS

APPENDIX 5 (Cont.)

APPENDIX 5 RPC-4500 - TYPEWRITER AND READER/PUNCH SCHEMATICS

PREFACE--Preceding each of the RPC-4430 schematic drawings (Card numbers 1 through 17) on the following pages is a Connector Chart that indicates the interconnecting wiring throughout the system. Each chart contains the following data:

1. Connector pin numbers in top to bottom order.
2. Signal identification for each pin.
3. Connector symbol and pin designation for all interconnecting circuit points.
4. System symbol for interconnecting points.

Following the schematic drawings for cards 1 through 17 is a group of schematics for the relay boards in the 4430. Each of these schematics is preceded by a Relay Location Chart in addition to a Connector Chart. These connector charts show:

1. Contact number: these correspond to contact numbers on the relay board schematic.
2. Contact state:
   NO= normally open = on-line
   NC= normally closed = off-line
   OS= operating strap
3. The switch point: shows connector pin designation of associated points, i.e., NO or NC is followed by its OS, and an OS is followed by both its NO and NC contacts.

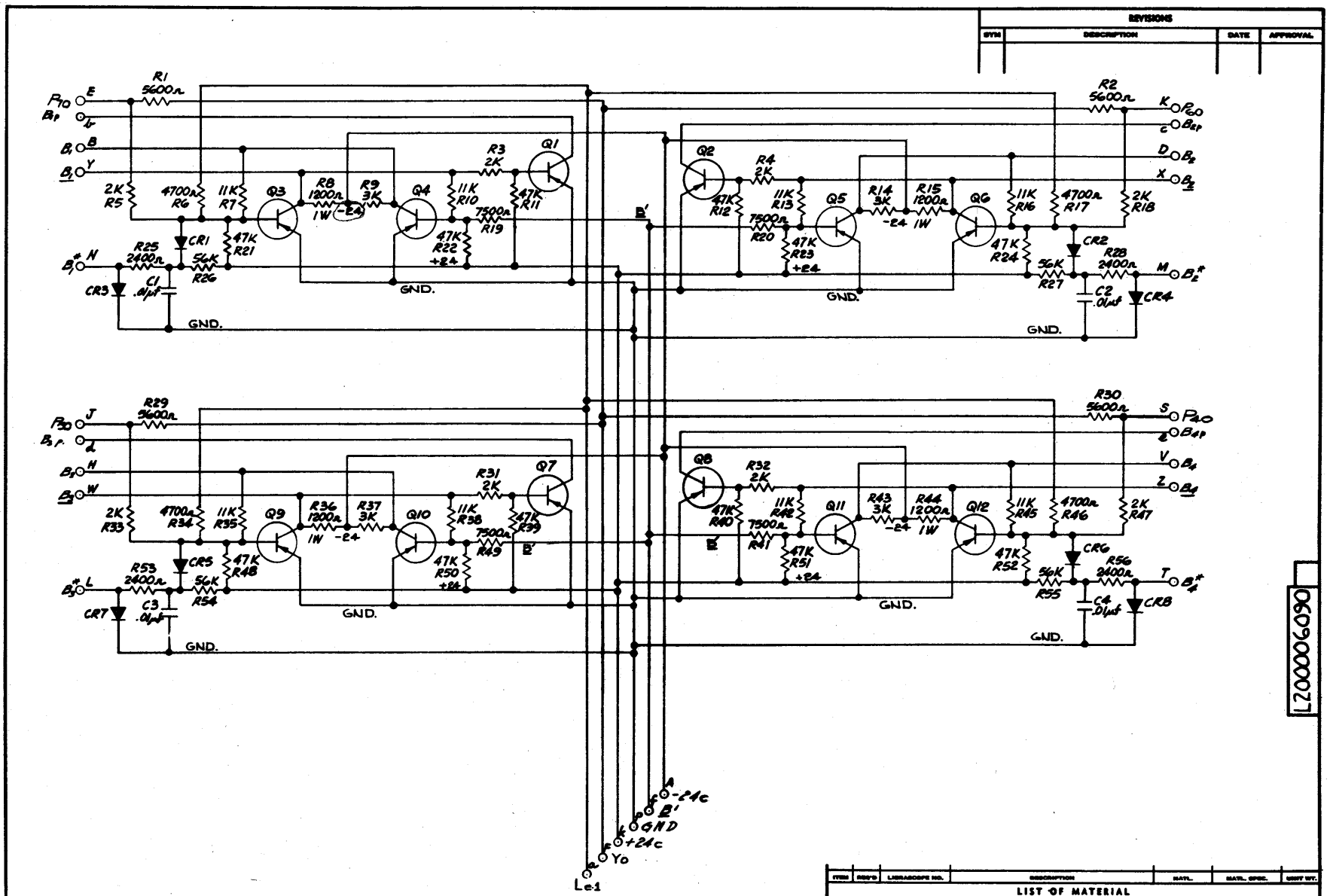
Finally, following the schematic for Relay Board V_1 is a Connector Chart for junction strips J27 and J28 and some miscellaneous signals having many tie points. This Buss Circuit Connector Chart shows the signals in order by symbol.

The table on the following page shows the abbreviations for system or unit nomenclature.

RPC-4430 CARD IDENTIFICATION CHART			
CONNECTOR NUMBER	SYMBOL	SYSTEM OR UNIT NAME	
J1 - J6	NSC	ON-LINE SYSTEM CONTROL	
J7 - J8	RC	READER CONTROL	
J9 - J11	PC	PUNCH CONTROL	
J12 - J13	FSC	OFF-LINE SYSTEM CONTROL	
J14 - J17	T/WC	T/W CONTROL	
J21	WR	W RELAY CARD - READER	
J22	XP	X RELAY CARD - PUNCH	
J25	V_2 T/W	V_2 RELAY CARD - T/W	
J26	V_1 T/W	V_1 RELAY CARD - T/W	
J27 - J28	JUNC	JUNCTION CARD	
J29 - J32	A T/W C	AUXILIARY T/W CONTROL	
J42	ND	NEXT DEVICE	
J43	A T/W U	AUXILIARY T/W UNIT	
J44	T/W U	T/W UNIT	
J45	COMP	COMPUTER (4010)	
J46	ACP	L.H. CONTROL PANEL	
J47	PCP	R.H. CONTROL PANEL	
P49	PCU	POWER CONTROL UNIT	
P50	RPU	READER/PUNCH UNIT	

J1 (NSC) CARD 1 ON-LINE SYSTEM CONTROL

PIN	LOGIC TERM	TIE POINTS												
A	-24c	POWER												
B	B_1	J45-F	COMP	J3-c	NSC	J4-U	NSC							
C														
D	B_2	J45-E	COMP	J3-e	NSC	J4-V	NSC							
E	P_{70}	J45-T	COMP											
F	Y_o	J2-M	NSC	J6-T	NSC									
H	B_3	J45-D	COMP	J3-E	NSC	J4-e	NSC							
J	P_{50}	J45-R	COMP											
K	P_{60}	J45-S	COMP											
L	B_3*	J27-V	JUNC	J27-U	JUNC	J21-f2	WR	J26-U2	V_1T/W	J31-L	AT/WC	J42-D	ND	
M	B_2*	J27-S	JUNC	J27-T	JUNC	J21-fi	WR	J26-Y2	V_1T/W	J31-H	AT/WC	J42-C	ND	
N	B_1*	J27-P	JUNC	J27-R	JUNC	J21-M2	WR	J26-Z2	V_1T/W	J31-J	AT/WC	J42-B	ND	
P	GND													
R														
S	P_{40}	J45-P	COMP											
T	B_4*	J27-W	JUNC	J27-X	JUNC	J21-A1	WR	J26-V2	V_1T/W	J31-E	AT/WC	J42-F	ND	
U														
V	B_4	J45-C	COMP	J3-C	NSC	J4-S	NSC							
W	$\underline{B}_3$	J3-b	NSC	J4-Y	NSC									
X	$\underline{B}_2$	J3-d	NSC	J4-W	NSC									
Y	$\underline{B}_1$	J3-f	NSC	J4-X	NSC									
Z	$\underline{B}_4$	J3-Z	NSC	J4-Z	NSC									
a	L_{e1}	J47-k	PCP	J2-L	NSC									
b	B_{1p}	J42-f	ND	J8-D	RC	J11-Z	PC	J14-N	T/WC	J29-N	AT/WC			
c	B_{2p}	J42-j	ND	J8-F	RC	J11-Y	PC	J14-T	T/WC	J29-T	AT/WC			
d	B_{3p}	J42-k	ND	J8-H	RC	J11-U	PC	J14-U	T/WC	J29-U	AT/WC			
e	B_{4p}	J42-n	ND	J8-J	RC	J11-X	PC	J14-M	T/WC	J29-M	AT/WC			
f	$\underline{B}'$	J2-a	NSC	J4-d	NSC	J5-b	NSC							
h														
j														
k	+24c	POWER												



NOTES:

1. ALL RESISTORS 1/2 W ±5% CARBON UNLESS OTHERWISE STATED.
2. ALL TRANSISTORS TO BE 2N1130, PER L532000521 OR EQUIV, PER E.S. L532000521.
3. ALL DIODES TO BE CTP 790 PER L531000583.

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL

LIST OF MATERIAL

ITEM	REQ'D	LIBRASCOPE NO.	DESCRIPTION	MATL.	MATL. SPEC.	UNIT WT.

L535000577	4430
NEXT ASSY.	USED ON
APPLICATION	

DO NOT SCALE THIS DRAWING

MATERIAL

DRAFTSMAN: CAGIVIN — DATE: 4-9-59

CHECKER

ENGINEER: Norman P. Van Ness — 5/16/60

APPROVAL: C.W. Johnson — 5/16/60

CONTRACT NO.

SCHEMATIC
SYSTEM CONTROL
(ON LINE) CARD #1

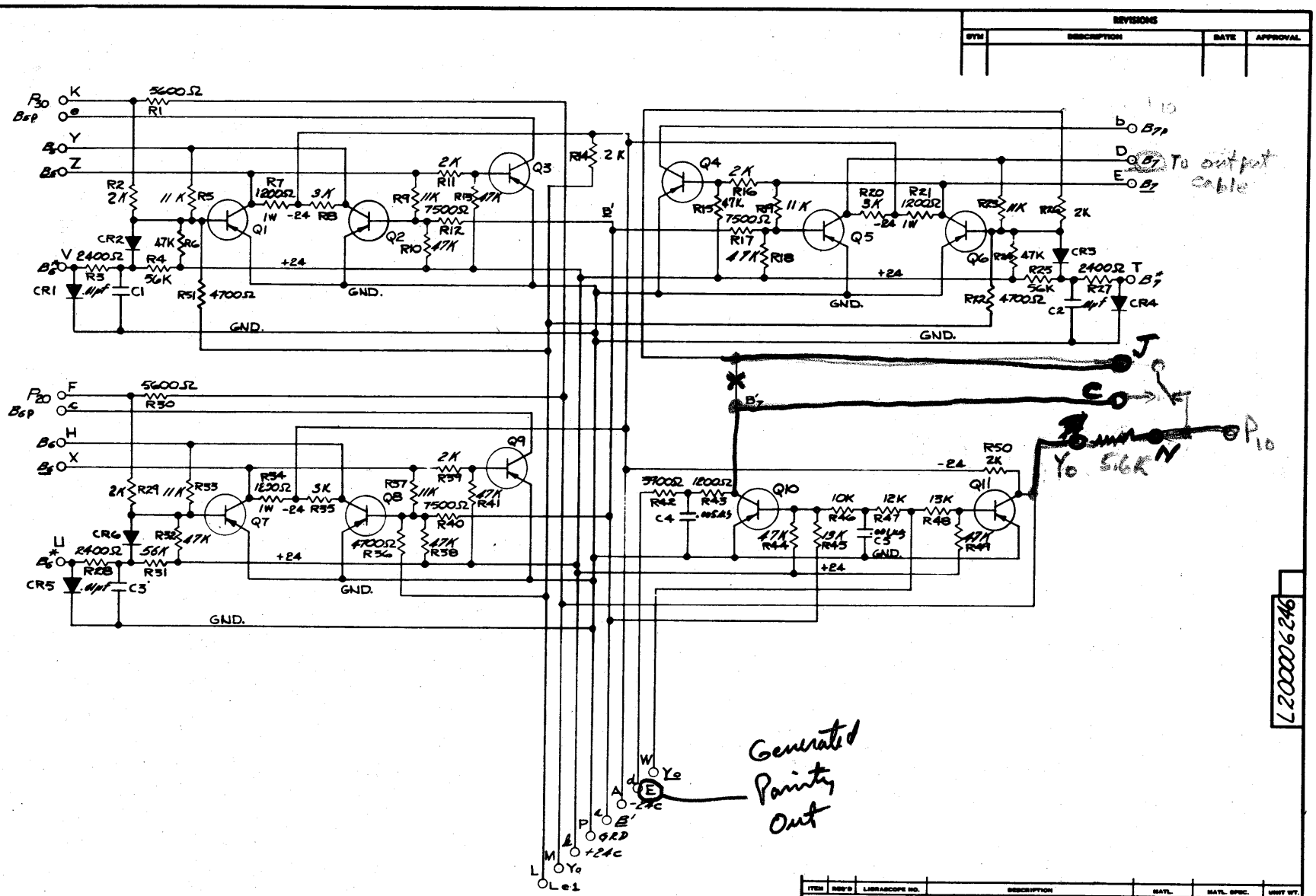
SCALE | UNIT WT.

L200006090

L200000027

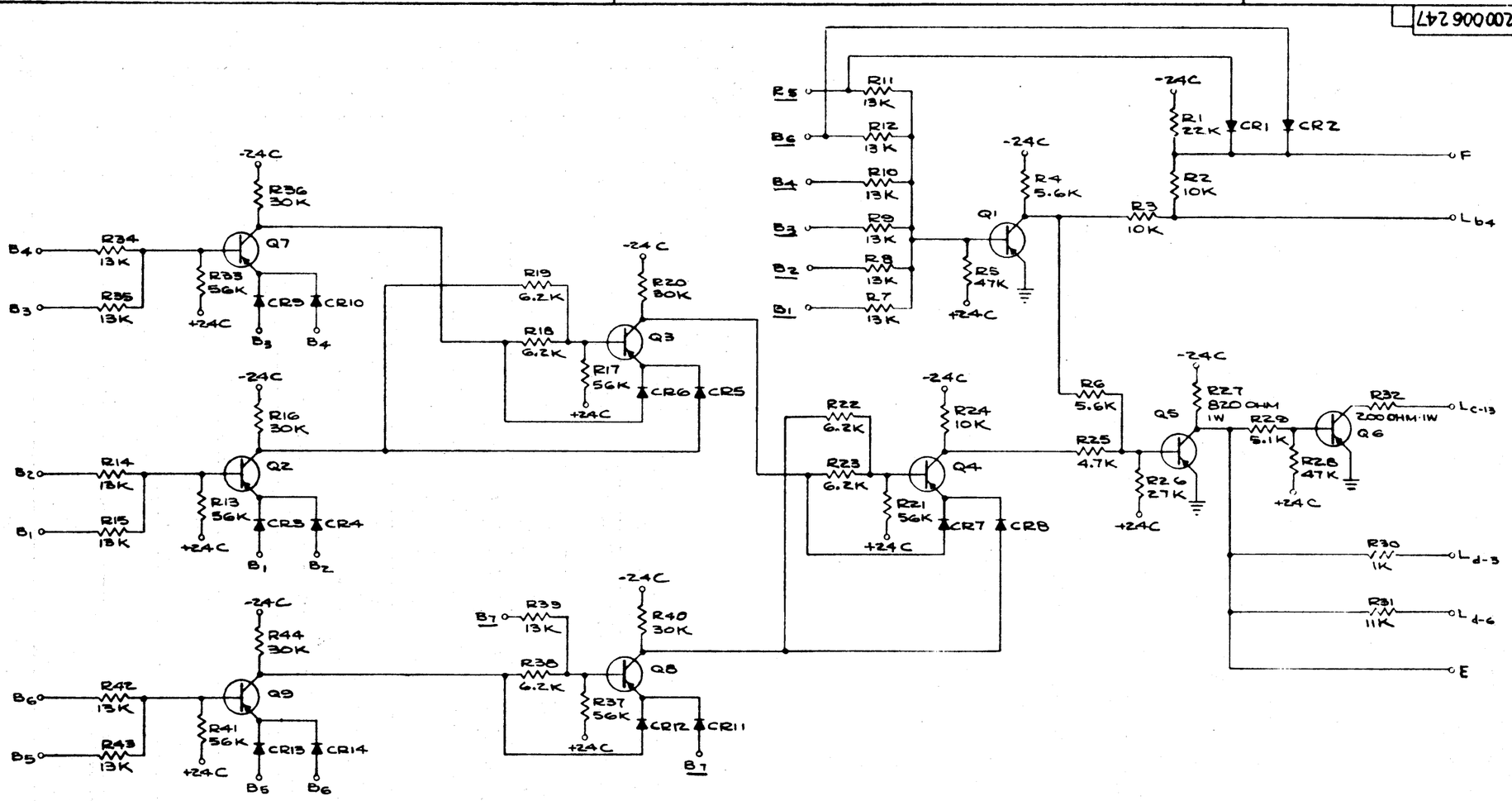
J2 (NSC) CARD 2 ON-LINE SYSTEM CONTROL

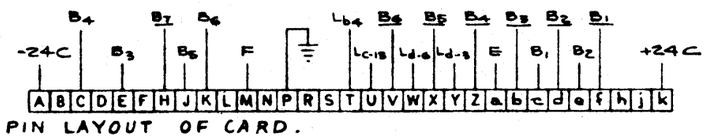
PIN	LOGIC TERM	TIE POINTS											
A	-24c	POWER											
B													
C													
D	B_7												
E	$\underline{B}_7$	J3-H	NSC										
F	P_{20}	J45-M	COMP										
H	B_6	J45-A	COMP	J3-K	NSC	J4j	NSC						
J													
K	P_{30}	J45-N	COMP										
L	L_{e1}	J1-a	NSC	J47-k	PCP								
M	Y_o	J1-F	NSC	J6-T	NSC								
N													
P	GND												
R													
S													
T	B_7*	J27-c	JUNC	J27-d	JUNC	J21-Z1	WR	J26-k1	V_1T/W	J31-a	AT/WC	J42-L	ND
U	B_6*	J27-a	JUNC	J27-b	JUNC	J21-a1	WR	J26-k2	V_1T/W	J31-C	AT/WC	J42-K	ND
V	B_5*	J27-Y	JUNC	J27-Z	JUNC	J21-a2	WR	J26-W1	V_1T/W	J31-N	AT/WC	J42-H	ND
W	$\underline{Y}_o$	J45-V	COMP	J5-a	NSC								
X	$\underline{B}_6$	J3-V	NSC	J4-b	NSC								
Y	B_5	J45-B	COMP	J3-J	NSC	J4-h	NSC						
Z	$\underline{B}_5$	J3-X	NSC	J4-a	NSC								
a	$\underline{B}'$	J1-f	NSC	J4-d	NSC	J5-b	NSC						
b	B_{7p}	J42-s	ND	J11-V	PC								
c	B_{6p}	J42-r	ND	J8-Y	RC	J11-a	PC	J14-L	T/WC	J29-L	AT/WC		
d	E	J3-a	NSC										
e	B_{5p}	J42-p	ND	J8-K	RC	J11-W	PC	J14-K	T/WC	J29-K	AT/WC		
f													
h													
j													
k	+24c	POWER											


REVISIONS
SYM | DESCRIPTION | DATE | APPROVAL
P30 K 5600Ω R1
B6P
Y
B5
Z
R2 2K
11K R5
R7 1200Ω 1W -24 3K R8
Q1
Q2
R9 11K 7500Ω R10
R11 2K R12 47K
Q3
R14 2K
B'
CR2
47K R6
V 2400Ω R3
R4 56K
CR1 .1μf C1
R51 4700Ω
+24
GND.
Q4 2K R16 47K R15 7500Ω R17 47K R18
Q5
Q6
R20 3K -24 1W R21 1200Ω
R22 11K R23 2K
CR3
R25 56K
2400Ω T
R27
C2 .1μf
CR4
R24 47K
R12 4700Ω
b B7P
D B7
E B7
To output cable
J
C
P10
Y0 56K N
P20 F 5600Ω R30
B6P
c
H
B6
X
B5
2K R29 11K R33
R34 1200Ω 1W -24 3K R35
Q7
Q8
R37 11K 7500Ω R40
R39 2K R41 47K
Q9
CR6
R32 47K
U
B6
2400Ω R28
56K R31
CR5 .1μf C3
R36 4700Ω
+24
GND.
R42 39000Ω R43 1200Ω
C4 .005μf
Q10
Q11
R44 47K
R46 10K 13K R45
C5 .001μf
R47 12K
R48 13K
R49 47K
R50 2K -24
W Y0
d
E
A -24c
B'
P GRD
+24c
M Y0
L Le1
Generated Parity Out
ITEM | REQ'D | LIBRASCOPE NO. | DESCRIPTION | MATL. | MATL. SPEC. | UNIT WT.
LIST OF MATERIAL
NOTES:
3. ALL DIODES TO BE CTP 790 PER L5510005Z3.
2. ALL TRANSISTORS TO BE 2N1130, PER L5320005Z1, OR EQUIV. PER ES. L5320005Z1.
1. ALL RESISTORS 1/2W ±5% CARBON UNLESS OTHERWISE STATED.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DIMENSIONS
FRACTIONAL ± 2 PLACES ± .010
± 3 PLACES ± .06 4 PLACES ± .0025
ANGLES ± 1° BREAK EDGES .005 MAX.
SURFACE FINISH 125
DO NOT SCALE THIS DRAWING
MATERIAL
L5350005Z3 | 4430
NEXT ASSY. | USED ON
APPLICATION
DRAFTSMAN CAGWIN DATE 4-11-55
CHECKER
ENGINEER 5/23/60
APPROVAL 5/31/60
CONTRACT NO.
SCHEMATIC SYSTEM CONTROL (ON-LINE) CARD # 2
SCALE | UNIT WT.
L2000006246
9290002027

J3 (NSC) CARD 3 ON-LINE SYSTEM CONTROL

PIN	LOGIC TERM	TIE POINTS						
A	-24c	POWER						
B								
C	B_4	J1-V	NSC	J4-S	NSC	J45-C	COMP	
D								
E	B_3	J1-H	NSC	J4-e	NSC	J45-D	COMP	
F								
H	$\underline{B}_7$	J2-E	NSC					
J	B_5	J2-Y	NSC	J4-h	NSC	J45-B	COMP	
K	B_6	J2-H	NSC	J4-j	NSC	J45-A	COMP	
L								
M								
N								
P	GND							
R								
S								
T	L_{b-4}	J47-X	PCP					
U	L_{c-13}	J47-H	PCP					
V	$\underline{B}_6$	J2-X	NSC	J4-b	NSC			
W	L_{d-6}	J47-d	PCP	J5-C	NSC			
X	$\underline{B}_5$	J2-Z	NSC	J4-a	NSC			
Y	L_{d-3}	J47-c	PCP	J6-W	NSC			
Z	$\underline{B}_4$	J1-Z	NSC	J4-Z	NSC			
a	E	J2-d	NSC					
b	$\underline{B}_3$	J1-W	NSC	J4-Y	NSC			
c	B_1	J1-B	NSC	J4-U	NSC	J45-F	COMP	
d	$\underline{B}_2$	J1-X	NSC	J4-W	NSC			
e	B_2	J1-D	NSC	J4-V	NSC	J45-E	COMP	
f	$\underline{B}_1$	J1-Y	NSC	J4-X	NSC			
h								
j								
k	+24c	POWER						





PIN LAYOUT OF CARD.

NOTES:

1. ALL RESISTORS 1/2 W ±5% CARBON UNLESS OTHERWISE SPECIFIED.
2. ALL DIODES TO BE PER L531000552.
3. ALL TRANSISTORS TO BE N400A PER L532000563.

REVISIONS			
DASH	DESCRIPTION	DATE	APPROVAL
2	REVISED & REDRAWN PER EO 68459		

L200006247

		DRAFTSMAN B. NORVELL	DATE 7-11-80
		APPROVED A.H. MAY	DATE 7-11-80
		DESIGNED L. BUCHANAN	DATE 7-10-80
L 595.300 Rev.	4430	APPROVED L. W. JOHNSON	DATE 8-28-80
NEXT ASSY	USED ON	CONTRACT NO.	
APPLICATION			

SCHEMATIC SYSTEM CONTROL (ONLINE) CARD #3

L200 006 247

CODE | SHEET OF

L200006247

J4 (NSC) CARD 4 ON-LINE SYSTEM CONTROL

PIN	LOGIC TERM	TIE POINTS											
A	-24c	POWER											
B	$\underline{C}$	J6-d	NSC										
C	C	J6-e	NSC										
D													
E	L_{g-1}	J47-j	PCP										
F													
H	L_{f-1}	J47-h	PCP										
J													
K	$\underline{B}$*	J5-f	NSC	J6-U	NSC								
L													
M	$\underline{M}$	J47-K	PCP										
N													
P	GND												
R													
S	B_4	J3-C	NSC	J1-V	NSC	J45-C	COMP						
T	S	J42-V	ND	J5-d	NSC	J8-W	RC	J11-R	PC	J14-W	T/WC	J17-d	T/WC
		J32-d	AT/WC	J29-W	AT/WC								
U	B_1	J3-c	NSC	J1-B	NSC	J45-P	COMP						
V	B_2	J3-e	NSC	J1-D	NSC	J45-E	COMP						
W	$\underline{B_2}$	J3-d	NSC	J1-X	NSC								
X	$\underline{B_1}$	J3-f	NSC	J1-Y	NSC								
Y	$\underline{B_3}$	J3-b	NSC	J1-W	NSC								
Z	$\underline{B_4}$	J3-Z	NSC	J1-Z	NSC								
a	$\underline{B_5}$	J3-X	NSC	J2-Z	NSC								
b	$\underline{B_6}$	J3-V	NSC	J2-X	NSC								
c	U	J42-W	ND	J11-M	PC	J17-j	T/WC	J32-j	AT/WC				
d	$\underline{B'}$	J2-a	NSC	J5-b	NSC	J1-f	NSC						
e	B_3	J3-E	NSC	J1-H	NSC	J45-D	COMP						
f	L_{b-7}	J47-W	PCP										
h	B_5	J3-J	NSC	J2-Y	NSC	J45-B	COMP						
j	B_6	J3-K	NSC	J2-H	NSC	J45-A	COMP						
k	+24c	POWER											

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
	REVISED & REDRAWN PER E.O. 66068		DK SEARCY

L200006248

Copy FF

-24C
R2 2K
R3 11K
R4 11K
R5 3.3K
C
Q1 2N1130
Q2 2N1130
R9 47K
R10 47K
+24C
R1 12K
R7 12K
R8 2K
R11 2K
R12 12K
R6 12K
L4-1
S
R18 6.8K
B1 R13 15K
B2 R14 18K
B3 R16 18K
B4 R17 15K
B5 R25 15K
B6 R26 15K
Q8' 2N1130
R15 47K
3
R19 6.2K
B1 R21 18K
B2 R22 15K
B3 R23 15K
B4 R24 15K
B6 R33 15K
B5 R34 15K
Q4 2N1130
R20 47K

R29 33K
R30 3.3K
R27' 10K.
R28 3.3K
R31 6.8K
CR1
C1 .033 uf 100VDC
Q6 2N1130
R38 682K
R39 3K
Q5 2N1130
R36 20K
R37 56K
R35 20K
C3 .01uf 500VDC
B*
K
C2 .01uf 500VDC
R41 6.8K
R40 10K
R42 47K
Q7 2N1130
R32 2K
R43 10K
M

Start on S.C. Mode

Note: PDP-8/C model (Eliminate delay)

B4 R48 5.1K
B5 R50 5.1K
B3 R55 5.1K
B2 R56 5.1K
B1 R59 5.1K
Q8 2N1130
CR2
R49 3.3K
U
Unused

B6 R60 13K
B5 R58 13K
B4 R57 13K
B3 R54 13K
B2 R53 13K
B1 R51 13K
B' R47 5.6K R46 5.6K C5 .001 uf 1000VDC
B* R44 13K R45 10K C4 .01 uf 500VDC
R52 5.1K
L6-7

C -24C | L4-1 C | B* L4-1 | M | B4 S | B1 B2 | B2 B1 | B3 B4 | B5 B6 | U B | J L6-7 | B5 B6 | +24C

A B C D E F H J K L M N P R S T U V W X Y Z a b c d e f h j k

PIN LAYOUT OF CARD

2. ALL DIODES TO BE PER L531000552.
1. ALL RESISTORS 1/2 W ±6% CARBON UNLESS OTHERWISE SPECIFIED.

NOTES:

MFG KIRTLAND		SCHEMATIC SYSTEM CONTROL (ON LINE) CARD 4	L200006248
APPROVED AH V.			
DRAWN R.F. MAGNELL			
CHK BRANN			
NEXT ASSY.	USED ON		
APPLICATION	CONTRACT NO.		

L200006248

J5 (NSC) CARD 5 ON-LINE SYSTEM CONTROL

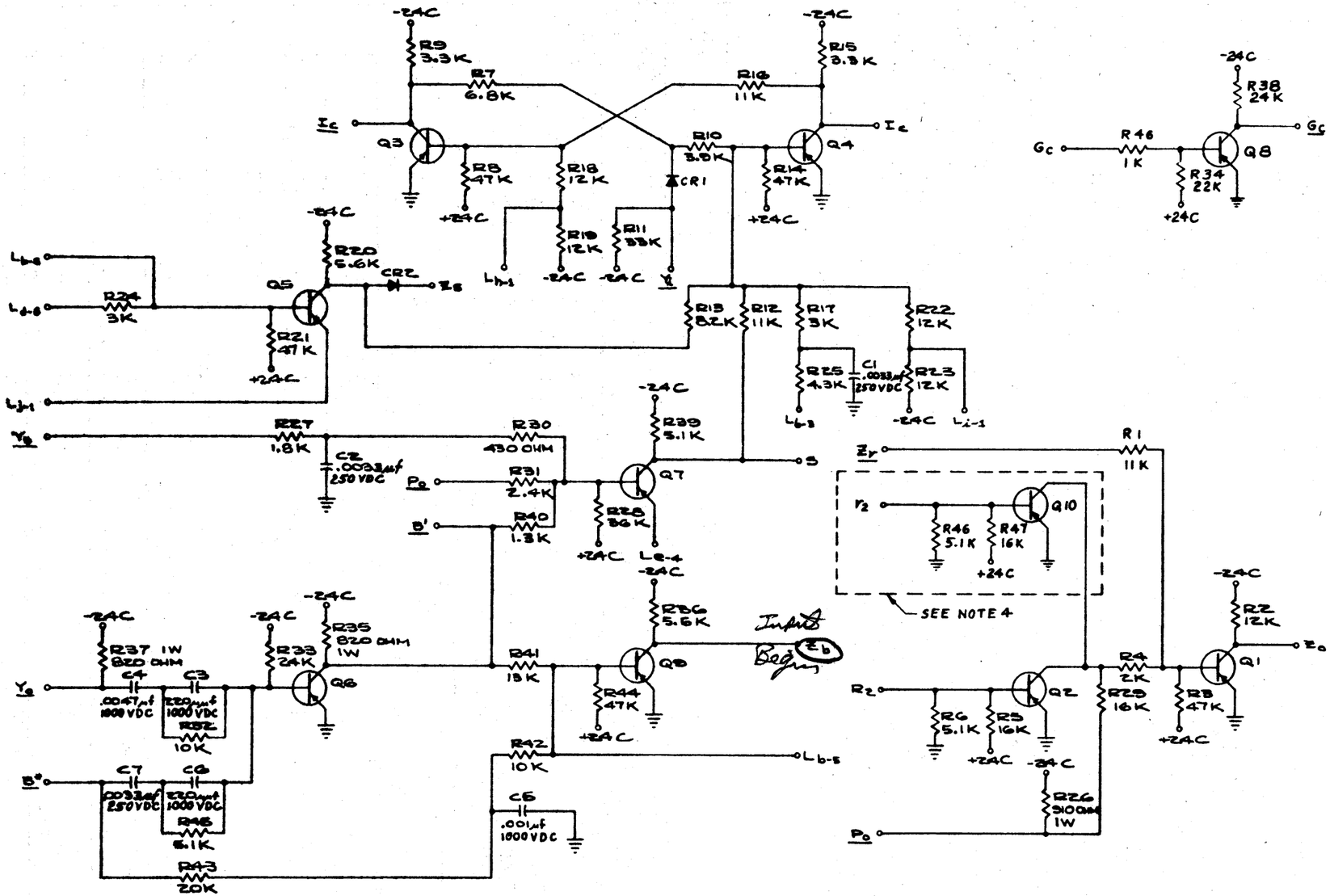
PIN	LOGIC TERM	TIE POINTS											
A	-24c	POWER											
B													
C	L_{d-6}	J3-W	NSC	J47-d	PCP								
D	R_2	J27-C	JUNC	J27-D	JUNC	J22-L1	XP	J25-E1	V_2T/W	J32-V	AT/WC	J42-b	ND
E	$\underline{Z}_r$	J6-X	NSC										
F	Z_o	J45-K	COMP										
H	$\underline{P}_o$	J45-V	COMP	J6-S	NSC								
J	$\underline{I}_c$	J6-Z	NSC										
K	L_{h-1}	J47-p	PCP										
L	I_c												
M	$\underline{Y}_i$	J45-W	COMP										
N													
P	GND												
R													
S	L_{b-8}	J47-b	PCP										
T	L_{j-1}	J47-e	PCP										
U	L_{b-3}	J47-Y	PCP										
V	$\underline{G}_c$	J27-E	JUNC	J27-F	JUNC	J22-J2	XP	J25-P1	V_2T/W	J32-D	AT/WC	J42-e	ND
W	G_c	J6-D	NSC										
X	L_{e-4}	J47-m	PCP										
Y	Z_s	J45-L	COMP										
Z	L_{i-1}	J47-E	PCP										
a	$\underline{Y}_o$	J2-W	NSC	J45-V	COMP								
b	$\underline{B}'$	J4-d	NSC	J2-a	NSC	J1-f	NSC						
c	Z_b	J45-H	COMP	J47-Z	PCP								
d	S	J42-V	ND	J4-T	NSC	J8-W	RC	J11-R	PC	J14-W	T/WC	J17-d	T/WC
		J32-d	AT/WC	J29-W	AT/WC								
e	L_{b-5}	J47-a	PCP										
f	$\underline{B}^*$	J4-K	NSC	J6-U	NSC								
h	r2	J42-c	ND										
j													
k	+24c	POWER											

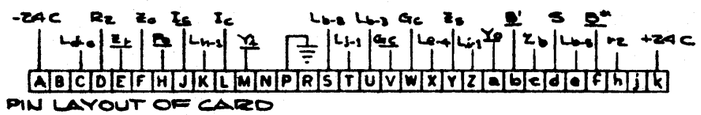
Z_b disconnected from J45H

Z_s disconnected from J45L

102 L00 0027

SYM	REVISIONS DESCRIPTION	DATE	APPROVAL
3	REVISED & REDRAWN PER E.O. 68472	[illegible]	[illegible]





PIN LAYOUT OF CARD

4. CIRCUIT USED ONLY WHEN SYSTEM CONTAINS MORE THAN 31 OUTPUT DEVICES (RE: Vz CIRCUIT.)
3. ALL TRANSISTORS TO BE N400A PER L532000563.
2. ALL DIODES TO BE PER L531000552.
1. ALL RESISTORS 1/2W ±5% CARBON UNLESS OTHERWISE SPECIFIED.

NOTES:

		DRAFTSMAN N.K.VELU	DATE 8-20
		CHECKED A.U.FFESON	8-21-70
		ENGINEER N.V.NARASIMHALU	8-25-70
		APPROVAL K.W.JOHNSON	8-25-70
L5340008735	4480	CONTRACT NO.	
NEXT ASSY.	USED ON		
APPLICATION			

SCHEMATIC SYSTEM CONTROL (ON LINE) CARD 6

L200007201

SCALE | QTY | SHEET | SHEET OF

L200007201

J6 (NSC) CARD 6 ON-LINE SYSTEM CONTROL

PIN	LOGIC TERM	TIE POINTS											
A	-24c	POWER											
B													
C													
D	G_c	J5-W	NSC										
E	B*	J42-A	ND	J27-M	JUNC	J27-N	JUNC	J21-Y1	WR	J26-b2	V_1T/W	J31-c	AT/WC
F	Z_i	J45-j	COMP	J47-f	PCP								
H	A_c												
J													
K	$\underline{R}_1$	J27-e	JUNC	J27-f	JUNC	J27-h	JUNC	J22-M2	XP	J22-V1	XP	J25-E2	V_2T/W
		J25-J1	V_2T/W	J32-K	AT/WC	J42-Y	ND						
L	Z_r	J47-n	PCP										
M	K_c	J42-T	ND	J31-X	AT/WC	J25-W2	V_2T/W						
N	A_p	J27-H	JUNC	J27-J	JUNC	J25-W	V_2T/W	J31-Y	AT/WC	J46-k	ACP	J32-B	AT/WC
		J17-B	T/WC	J42-S	ND								
P	GND												
R													
S	$\underline{P}_o$	J5-H	NSC	J45-U	COMP								
T	Y_o	J2-M	NSC	J1-F	NSC								
U	$\underline{B}$*	J5-f	NSC	J4-K	NSC								
V	$\underline{A}_c$												
W	L_{d-3}	J3-Y	NSC	J47-c	PCP								
X	$\underline{Z}_r$	J5-E	NSC										
Y	$\underline{Z}_q$	J45-Y	COMP										
Z	$\underline{I}_c$	J5-J	NSC										
a	r_3	J42-P	ND										
b	R_3	J27-A	JUNC	J27-B	JUNC	J21-K1	WR	J25-V2	V_2T/W	J31-U	AT/WC	J42-N	ND
c	$\underline{r}_1$	J42-Z	ND										
d	$\underline{C}$	J4-B	NSC										
e	C	J4-C	NSC										
f	L_{g-13}	J47-J	PCP										
h	L_{f-13}	J47-L	PCP										
j													
k	+24c	POWER											

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
1	EO # 49532 SEE EO FOR CHANGES	6-22-60	DR. BRUNER
		6-22-60	CH. Jeffries
2	REVISED PER E.O. 57032	11/10/60	DR DOYLE

4343 MOD

Advance

Input Enable

4. PHANTOM COMPONENTS ARE NEEDED ONLY WHEN SYSTEM CONTAINS MORE THAN 31 OUTPUT DEVICES (RE: Y_1 CIRCUIT), OR 31 INPUT DEVICES (RE: Y_3 CIRCUIT).
3. ALL DIODES TO BE CTP 790, PER L531000523.
2. ALL TRANSISTORS TO BE 2N1130 PER L532000521 OR EQUIV PER ES L532000521.
1. ALL RESISTORS 1/2 W ±5% CARBON UNLESS OTHERWISE STATED.

L535000577	4450
NEXT ASSY.	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DIMENSIONS
FRACTIONAL ± 2 PLACES ± .010
± 2 PLACES ± .02 ± 4 PLACES ± .0005
ANGLES ± 1° BREAK EDGES .005 MAX.
SURFACE FINISH 125

DO NOT SCALE THIS DRAWING

MATERIAL

ITEM	REQ'D	NO.	DESCRIPTION	MATL.	MATL. SPEC.	UNIT WT.

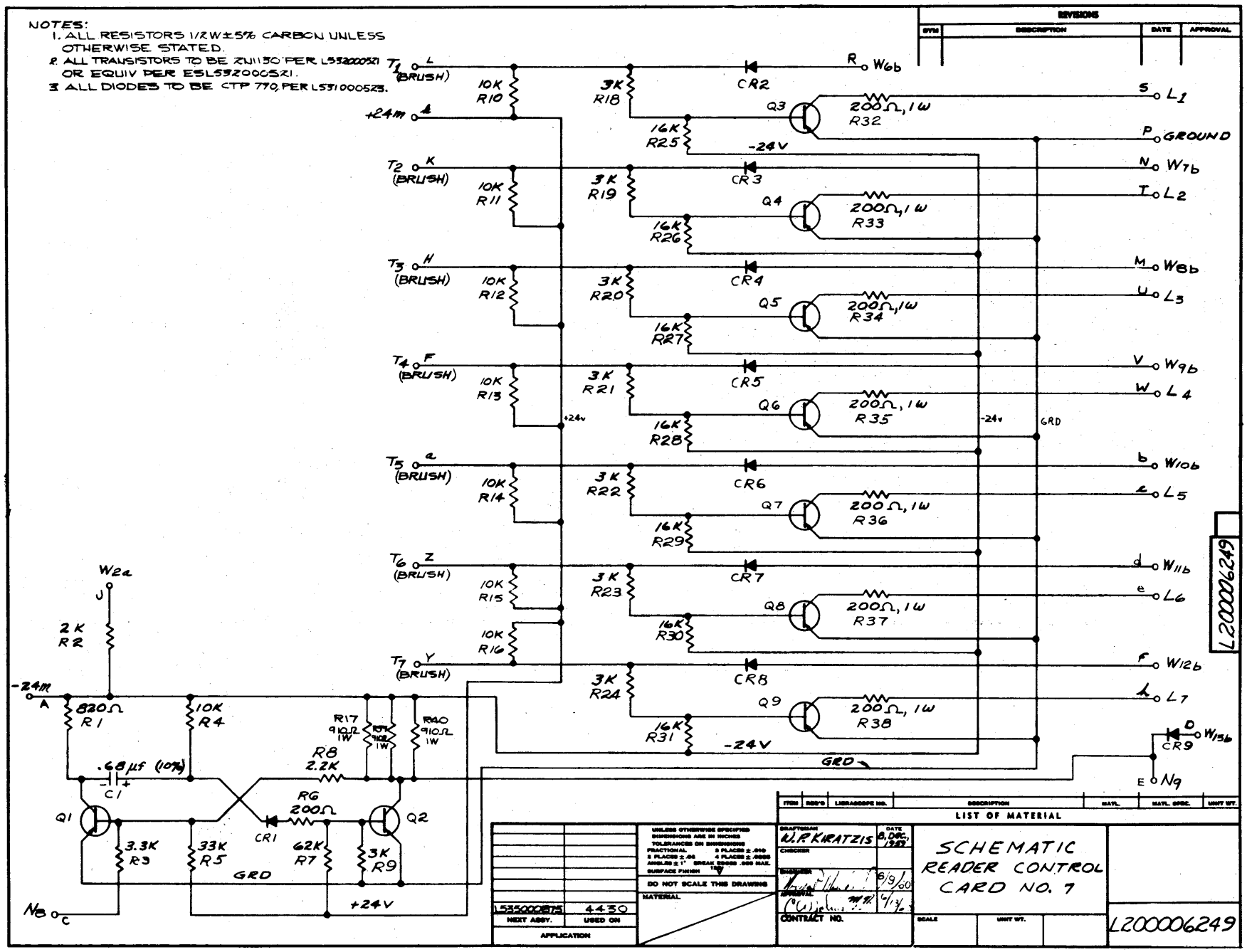
LIST OF MATERIAL

DRAFTSMAN NORVELL	DATE 11-6-59	SCHEMATIC SYSTEM CONTROL (ON LINE) CARD G
CHECKER		
ENGINEER W. P. Marshall	9/26/60	
ENGR. MGR. C. W. Johnson	9/26/60	
CONTRACT NO.	SCALE	UNIT WT.

L2000006236

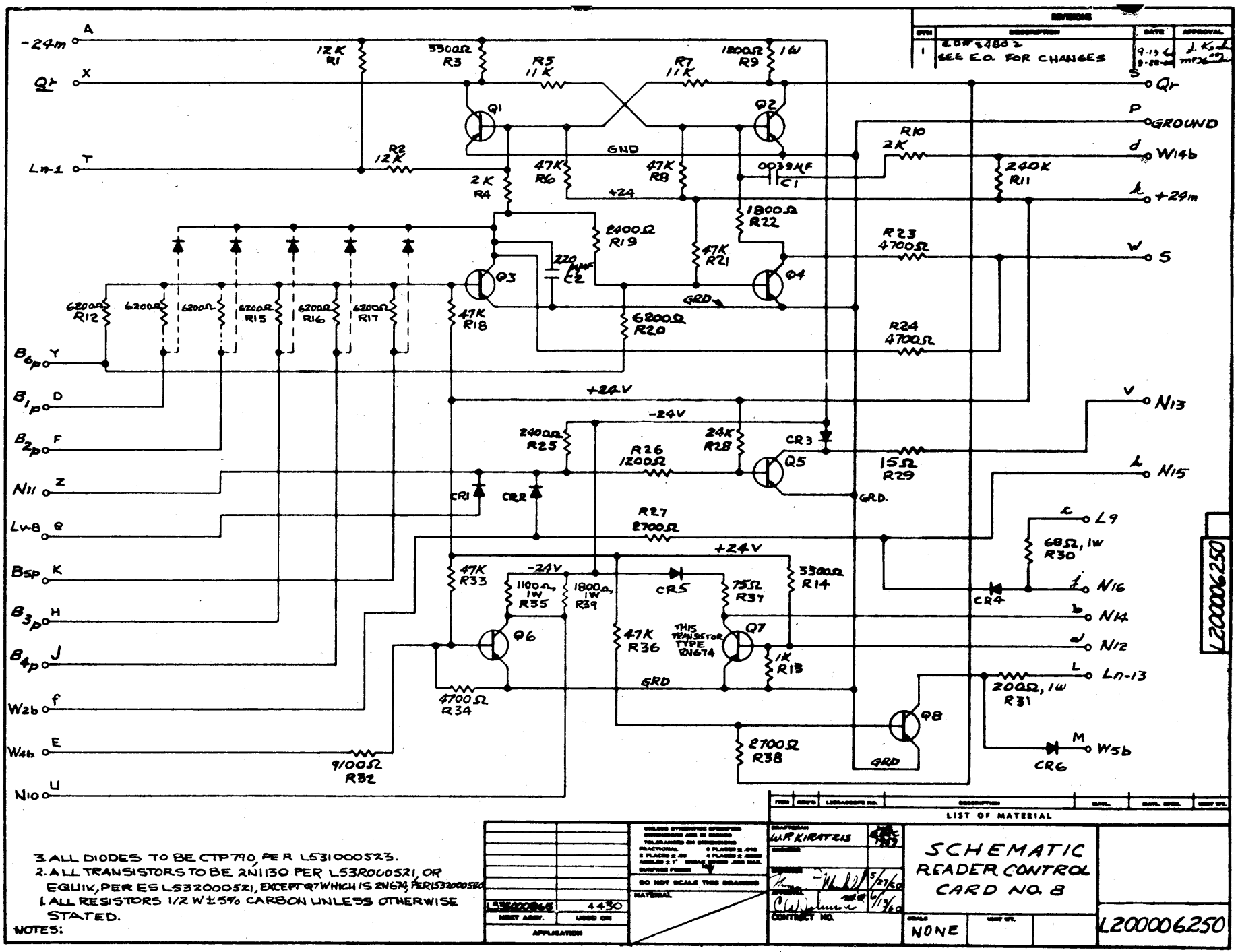
J7 (RC) CARD 7 READER CONTROL

PIN	LOGIC TERM	TIE POINTS		
A	-24m	POWER		
B				
C	N_8	P50-25	RPU	
D	W_{13b}	J21-Y2	WR	
E	N_9	P50-57	RPU	
F	T_4	P50-61	RPU	
H	T_3	P50-60	RPU	
J	W_{2a}	J21-H2	WR	
K	T_2	P50-59	RPU	
L	T_1	P50-58	RPU	
M	W_{8b}	J21-e2	WR	
N	W_{7b}	J21-e1	WR	
P	GND	J22-E2	XP	
R	W_{6b}	J21-M1	WR	
S	L_1	J47-U	PCP	
T	L_2	J47-T	PCP	
U	L_3	J47-S	PCP	
V	W_{9b}	J21-A2	WR	
W	L_4	J47-R	PCP	
X				
Y	T_7	P50-64	RPU	
Z	T_6	P50-63	RPU	
a	T_5	P50-62	RPU	
b	W_{10b}	J21-62	WR	
c	L_5	J47-P	PCP	
d	W_{11b}	J21-b1	WR	
e	L_6	J47-N	PCP	
f	W_{12b}	J21-Z2	WR	
h	L_7	J47-M	PCP	
j				
k	+24m	POWER		


NOTES:
1. ALL RESISTORS 1/2W ±5% CARBON UNLESS OTHERWISE STATED.
2. ALL TRANSISTORS TO BE 2N1130 PER L5322005Z1 OR EQUIV PER ESL5320005Z1.
3 ALL DIODES TO BE CTP 770, PER L5310005Z5.
REVISIONS
SYM | DESCRIPTION | DATE | APPROVAL
T1 L (BRUSH)
T2 K (BRUSH)
T3 H (BRUSH)
T4 F (BRUSH)
T5 a (BRUSH)
T6 Z (BRUSH)
T7 Y (BRUSH)
+24m
-24m
10K R10
10K R11
10K R12
10K R13
10K R14
10K R15
10K R16
3K R18
3K R19
3K R20
3K R21
3K R22
3K R23
3K R24
16K R25
16K R26
16K R27
16K R28
16K R29
16K R30
16K R31
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
Q3
Q4
Q5
Q6
Q7
Q8
Q9
200Ω, 1W R32
200Ω, 1W R33
200Ω, 1W R34
200Ω, 1W R35
200Ω, 1W R36
200Ω, 1W R37
200Ω, 1W R38
R
S
P
N
T
M
U
V
W
b
c
d
e
f
h
D
E
W6b
L1
GROUND
W7b
L2
W8b
L3
W9b
L4
W10b
L5
W11b
L6
W12b
L7
W15b
Ng
-24V
GRD
+24v
W2a
J
2K R2
820Ω R1
10K R4
.68µf (10%) C1
R17 910Ω 1W
R18 10K 1W
R40 910Ω 1W
R8 2.2K
RG 200Ω
Q1
Q2
CR1
3.3K R3
33K R5
62K R7
3K R9
NB
C
A
LIST OF MATERIAL
ITEM | REQ'D | LIBRASCOPE NO. | DESCRIPTION | MATL. | MATL. SPEC. | UNIT WT.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DIMENSIONS
FRACTIONAL ± 2 PLACES ± .010
3 PLACES ± .005 4 PLACES ± .0050
ANGLES ± 1° BREAK EDGES .005 MAX.
SURFACE FINISH 125
DO NOT SCALE THIS DRAWING
MATERIAL
DRAFTSMAN W.P.KRATZIS DATE 8 DEC 1959
CHECKER
ENGINEER 8/9/60
APPROVAL 8/12/60
CONTRACT NO.
SCHEMATIC READER CONTROL CARD NO. 7
SCALE
UNIT WT.
L200006249
L535000875
NEXT ASSY.
4430
USED ON
APPLICATION
6429000027
New 4343 Mod

J8 (RC) CARD 8 READER CONTROL

PIN	LOGIC TERM	TIE POINTS											
A	-24m	POWER											
B													
C													
D	B_{1p}	J1-b	NSC	J11-Z	PC	J42-f	ND	J14-N	T/WC	J29-N	AT/WC		
E	W_{4b}	J21-P2	WR										
F	B_{2p}	J42-j	ND	J1-c	NSC	J11-Y	PC	J14-T	T/WC	J29-T	AT/WC		
H	B_{3p}	J42-k	ND	J1-d	NSC	J11-U	PC	J14-U	T/WC	J29-U	AT/WC		
J	B_{4p}	J42-n	ND	J1-e	NSC	J11-X	PC	J14-M	T/WC	J29-M	AT/WC		
K	B_{5p}	J42-p	ND	J2-e	NSC	J11-W	PC	J14-K	T/WC	J29-K	AT/WC		
L	L_{n-13}	J46-V	ACP										
M	W_{5-b}	J21-N2	WR										
N													
P	GND												
R													
S	Q_r	J21-J1	WR										
T	L_{n-1}	J46-S	ACP										
U	N_{10}	P50-29	RPU										
V	N_{13}	P50-5	RPU	P50-4	RPU								
W	S	J42-V	ND	J4-T	NSC	J5-d	NSC	J11-R	PC	J14-W	T/WC	J17-d	T/WC
		J32-d	AT/WC	J29-W	AT/WC								
X	$\underline{Q}_r$	J21-P1	WR										
Y	B_{6p}	J42-r	ND	J2-c	NSC	J11-a	PC	J14-L	T/WC	J29-L	AT/WC		
Z	N_{11}	P50-24	RPU										
a	N_{12}	P50-28	RPU										
b	N_{14}	P50-7	RPU										
c	L_9	J46-v	ACP										
d	W_{14b}	J21-R1	WR	J12-Z	FSC								
e	L_{v-8}	J46-n	ACP										
f	W_{2b}	J21-H1	WR										
h	N_{15}	P50-27	RPU										
j	N_{16}	P50-31	RPU										
k	+24m	POWER											



NOTES:
1. ALL RESISTORS 1/2 W ±5% CARBON UNLESS OTHERWISE STATED.
2. ALL TRANSISTORS TO BE 2N1130 PER L53R000521, OR EQUIV, PER ES L53200052I, EXCEPT Q7 WHICH IS 2N674, PER L53200056I
3. ALL DIODES TO BE CTP790, PER L53I000523.

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
1	ECN# 24802 SEE E.O. FOR CHANGES	9-13-62 9-28-62	J.K. mrk

LIST OF MATERIAL

DRAFTSMAN	W.P. KIRATZES
CHECKED	
ENGINEER	
MATERIAL	
CONTRACT NO.	

SCHEMATIC READER CONTROL CARD NO. 8

NONE

L200006250

L200006250

New 4343 Mod.

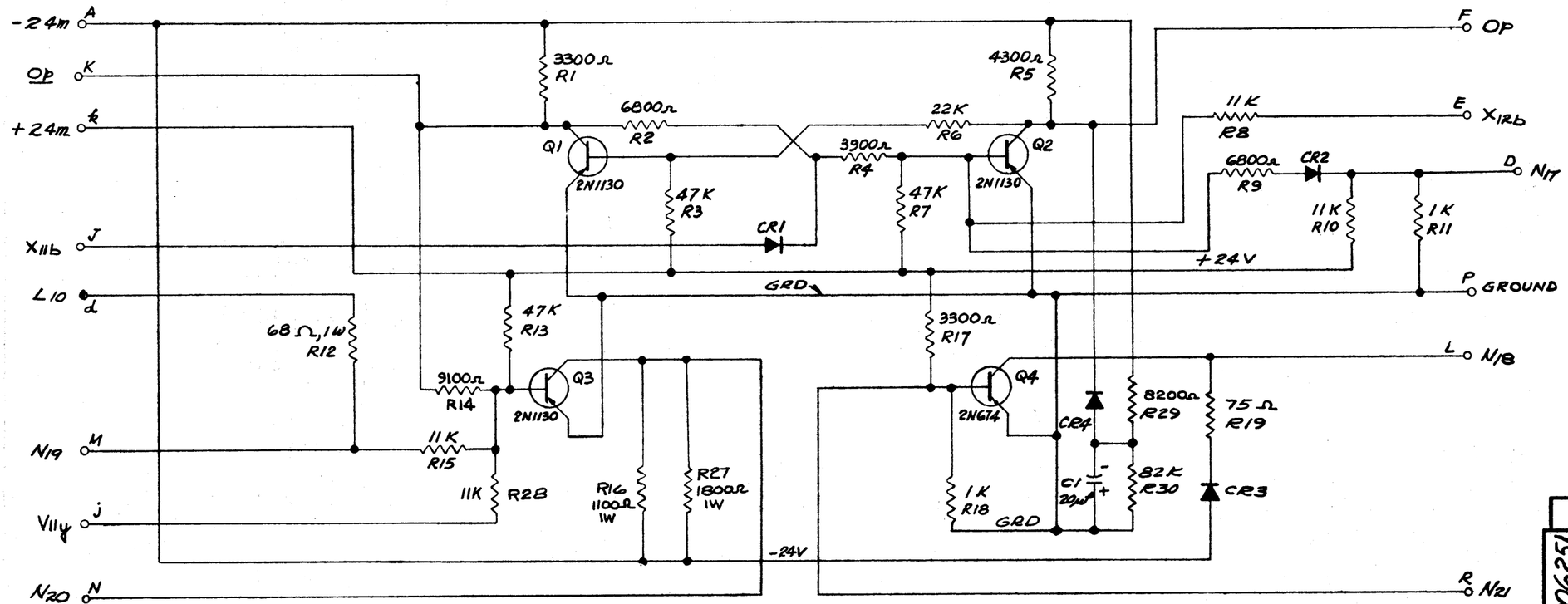
J9 (PC) CARD 9 PUNCH CONTROL

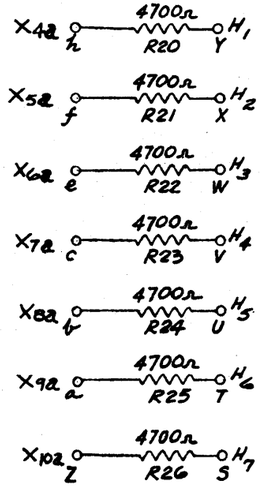
PIN	LOGIC TERM	TIE POINTS			
A	-24m	POWER			
B					
C					
D	N_{17}	P50-22 RPU	J22-M1	XP	
E	X_{12b}	J22-H1 XP			
F	O_p	P50-21 RPU			
H					
J	X_{11b}	J22-H2 XP			
K	$\underline{O}_p$				
L	N_{18}	P49-s PCU	P50-6	RPU	
M	N_{19}	P50-33 RPU			
N	N_{20}	P50-19 RPU			
P	GND				
R	N_{21}	P50-18 RPU			
S	H_7	J12-F FSC			
T	H_6	J13-b FSC	J15-f	T/WC	
U	H_5	J13-c FSC	J15-e	T/WC	
V	H_4	J13-d FSC	J15-W	T/WC	
W	H_3	J13-e FSC	J15-X	T/WC	
X	H_2	J13-f FSC	J15-H	T/WC	
Y	H_1	J13-h FSC	J15-F	T/WC	
Z	X_{10a}	J22-F2 XP			
a	X_{9a}	J22-E1 XP			
b	X_{8a}	J22-A2 XP			
c	X_{7a}	J22-A1 XP			
d	L_{10}	J46-p ACP			
e	X_{6a}	J22-b2 XP			
f	X_{5a}	J22-c1 XP			
h	X_{4a}	J22-c2 XP			
j	V_{11Y}	J14-R T/WC	J25-X1	V_2T/W	
k	+24m	POWER			

NOTES:

1. ALL RESISTORS 1/2W ± 5% CARBON UNLESS OTHERWISE STATED.
2. ALL TRANSISTORS TO BE 2N1130, PER L532000521 OR EQUIV., PER ES L532000521, EXCEPT Q4 WHICH IS 2N674, PER L532000530.
3. ALL DIODES TO BE CTP-790, PER L531000523.

REVISIONS			
SYM	DESCRIPTION	DATE	
1	ADDED CAPACITOR C1, DIODE CR4, RESISTORS R28, R29, R30, & PWJ Vnly EO 51707	6 AUG 1960	





ITEM	REQ'D	NO.	DESCRIPTION	MATL.	MATL. SPEC.	UNIT WT.

LIST OF MATERIAL

L532000817	4430
NEXT ASSY.	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DIMENSIONS
FRACTIONAL ± PLACES ± .010
2 PLACES ± .02 4 PLACES ± .0005
ANGLES ± 1° BREAK EDGES .005 MAX.
SURFACE FINISH 125
DO NOT SCALE THIS DRAWING
MATERIAL

DRAFTSMAN	W. P. KIRATZIS	DATE 8 DEC 1959
CHECKER		
ENGINEER		5/27/60
APPROVAL		6/13/60
CONTRACT NO.		

SCHEMATIC PUNCH CONTROL CARD NO. 9

SCALE | UNIT WT.

4343 MOD (NEW)

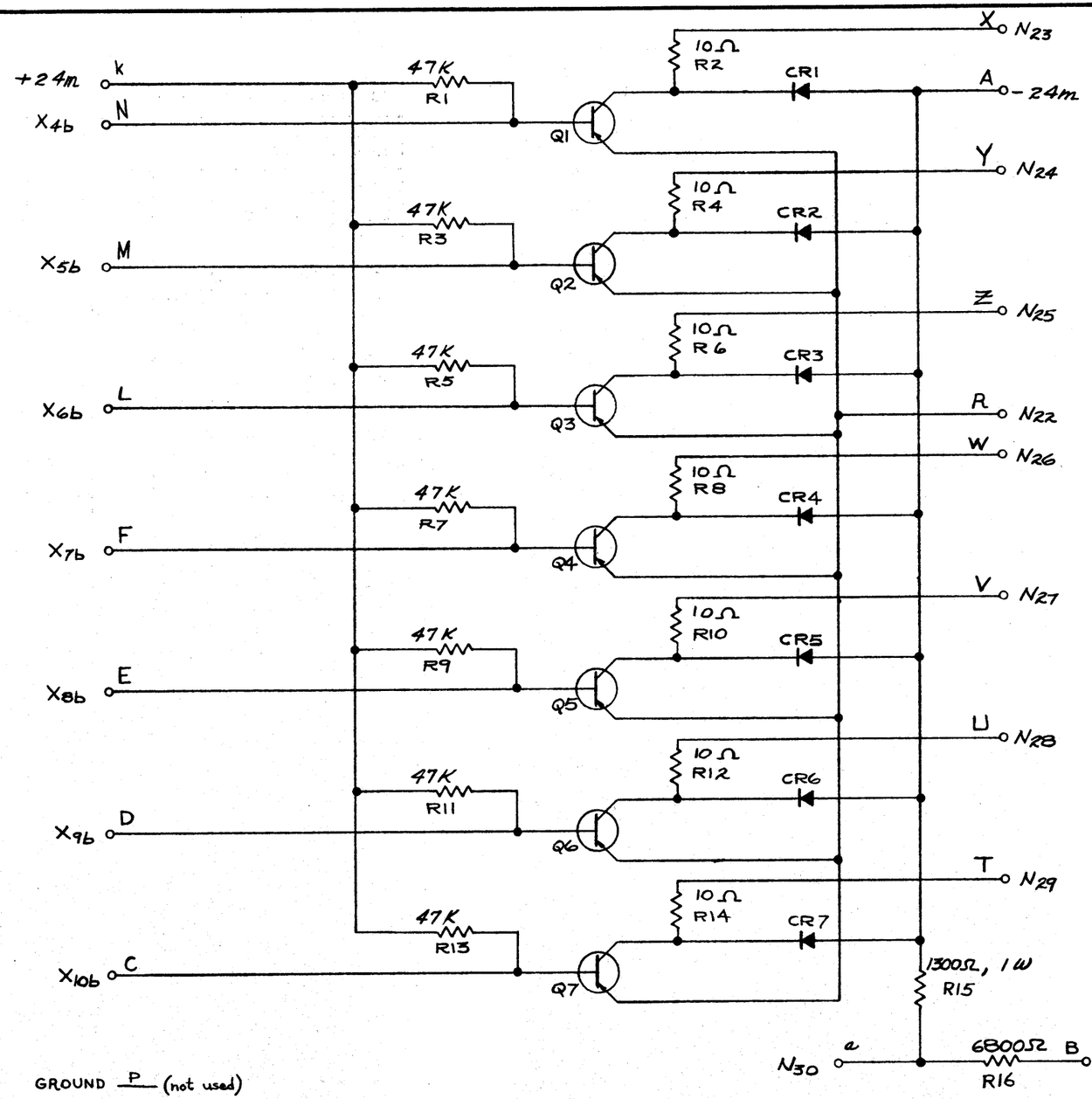
L200006251

L200006251

J10 (PC) CARD 10 PUNCH CONTROL

PIN	LOGIC TERM	TIE POINTS		
A	-24m	POWER		
B	X_{13b}	J22-N1	XP	
C	X_{10b}	J22-K2	XP	
D	X_{9b}	J22-C2	XP	
E	X_{8b}	J22-D1	XP	
F	X_{7b}	J22-D2	XP	
H				
J				
K				
L	X_{6b}	J22-d1	XP	
M	X_{5b}	J22-d2	XP	
N	X4b	J22-f1	XP	
P	GND			
R	N_{22}	P50-20	RPU	
S				
T	N_{29}	P50-14	RPU	
U	N_{28}	P50-13	RPU	
V	N_{27}	P50-12	RPU	
W	N_{26}	P50-11	RPU	
X	N_{23}	P50-8	RPU	
Y	N_{24}	P50-9	RPU	
Z	N_{25}	P50-10	RPU	
a	N_{30}	P50-32	RPU	
b				
c				
d				
e				
f				
h				
j				
k	+24m	POWER		

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
1	E.O.# 5658A - SIGNAL SYM AT TERMINAL B WAS X14b	9-22-60	D.W. FARBER



3. ALL DIODES TO BE CTP790, PER L531000523.
2. ALL TRANSISTORS TO BE 2N1130 PER L532000521 OR EQUIV., PER ESL532000521.
1. ALL RESISTORS 1/2W ±5% CARBON UNLESS OTHERWISE STATED.

NOTES:

L535000900	4430
NEXT ASSY.	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DIMENSIONS
FRACTIONAL 3 PLACES ±.010
2 PLACES ±.02 4 PLACES ±.0005
ANGLES ±1° BREAK EDGES .005 MAX.
SURFACE FINISH 125

DO NOT SCALE THIS DRAWING

MATERIAL

LIST OF MATERIAL

ITEM	REQ'D	DESCRIPTION	MATL.	MATL. SPEC.	UNIT WT.

DRAFTSMAN	W.P. KIRATZIS	DATE 7 DEC. 1959
CHECKER		
ENGINEER APPROVAL		6/3/60
		6/6/60
CONTRACT NO.		

SCHEMATIC PUNCH CONTROL CARD NO. 10

4343 MOD (NEW)

L200006252

SCALE	UNIT WT.	

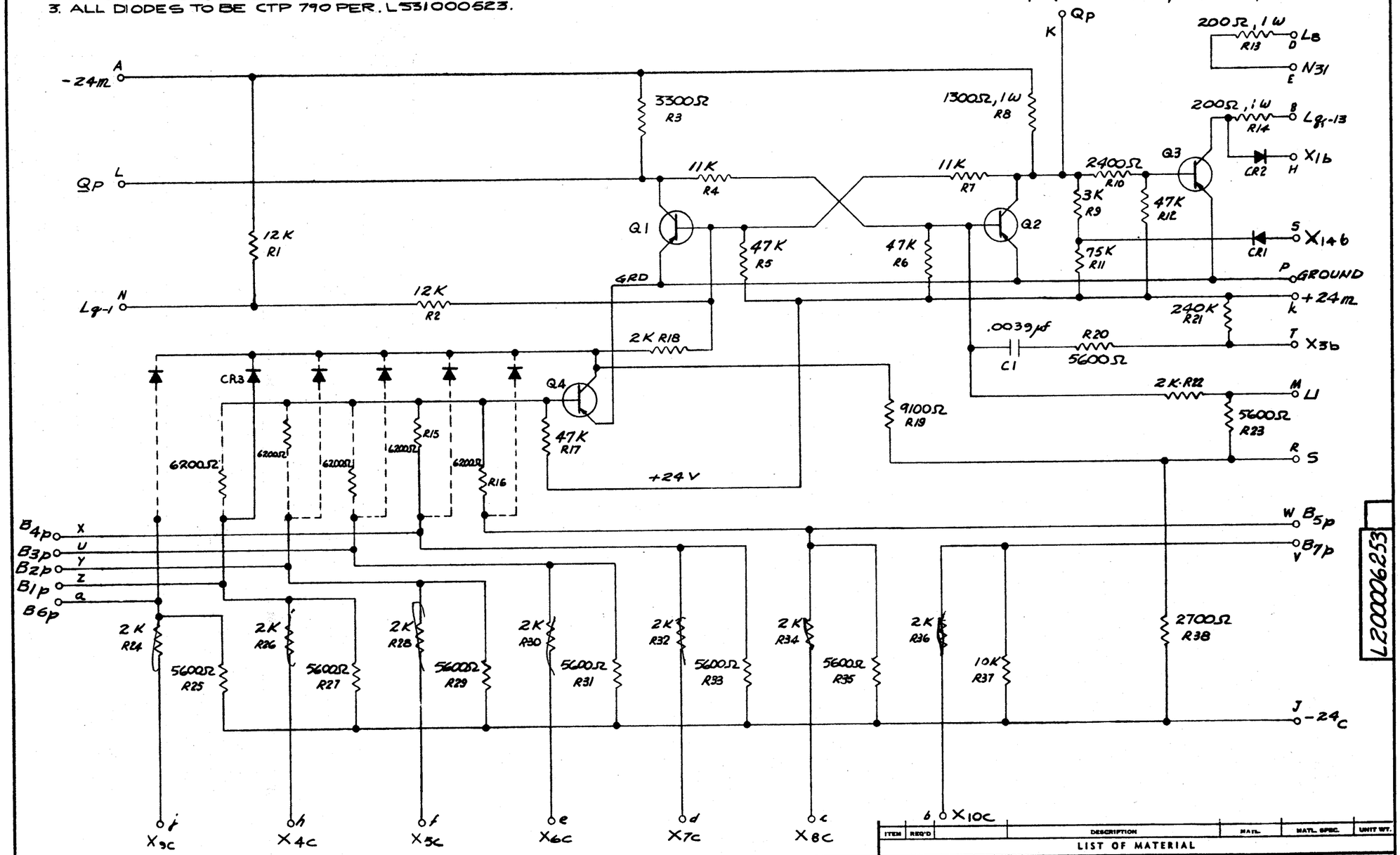
L200006252

J11 (PC) CARD 11 PUNCH CONTROL

PIN	LOGIC TERM	TIE POINTS											
A	-24m	POWER											
B	L_{q-13}	J46-U	ACP										
C													
D	L_8	J46-s	ACP										
E	N_{31}	J28-j	JUNC	J28-k	JUNC	J21-L2	WR	J22-Y1	XP	J25-H1	V_2T/W		
F													
H	X_{1b}	J22-Y2	XP										
J	-24c	POWER											
K	Q_p												
L	$\underline{Q}_p$	J22-J1	XP										
M	U	J42-W	ND	J4-c	NSC	J17-j	T/WC	J32-j	AT/WC				
N	L_{q-1}	J46-T	ACP										
P	GND												
R	S	J42-V	ND	J4-T	NSC	J5-d	NSC	J8-W	RC	J14-W	T/WC	J17-d	T/WC
		J32-d	AT/WC	J29-W	AT/WC								
S	X_{14b}	J22-N2	XP										
T	X_{3b}	J22-Z2	XP										
U	B_{3p}	J42-k	ND	J1-d	NSC	J8-H	RC	J14-U	T/WC	J29-U	AT/WC		
V	B_{7p}	J42-s	ND	J2-b	NSC								
W	B_{5p}	J42-p	ND	J2-e	NSC	J8-K	RC	J14-K	T/WC	J29-K	AT/WC		
X	B_{4p}	J42-n	ND	J1-e	NSC	J8-J	RC	J14-M	T/WC	J29-M	AT/WC		
Y	B_{2p}	J42-j	ND	J1-c	NSC	J8-F	RC	J14-T	T/WC	J29-T	AT/WC		
Z	B_{1p}	J42-f	ND	J1-b	NSC	J8-D	RC	J14-N	T/WC	J29-N	AT/WC		
a	B_{6p}	J42-r	ND	J2-c	NSC	J8-Y	RC	J14-L	T/WC	J29-L	AT/WC		
b	X_{10c}	J22-K1	XP										
c	X_{8c}	J22-B2	XP										
d	X_{7c}	J22-C1	XP										
e	X_{6c}	J22-e2	XP										
f	X_{5c}	J22-e1	XP										
h	X_{4c}	J22-f2	XP										
j	X_{9c}	J22-B1	XP										
k	+24m	POWER											

NOTES:
1. ALL RESISTORS TO BE 1/2W ± 5% UNLESS OTHERWISE STATED.
2. ALL TRANSISTORS TO BE 2N1130 PER L532000521, OR EQUIV., PER ES.L532000521.
3. ALL DIODES TO BE CTP 790 PER. L531000523.

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
1	EO# 34801 CHANGED C1, .004μF TO .0039μF	9-13-60 9-22-60	



ITEM	REQ'D	DESCRIPTION	MATL.	MATL. SPEC.	UNIT WT.

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DIMENSIONS
FRACTIONAL ± 2 PLACES ± .010
± PLACES ± .02 4 PLACES ± .0008
ANGLES ± 1° BREAK EDGES .005 MAX.
SURFACE FINISH 125

DO NOT SCALE THIS DRAWING

MATERIAL

L535000901	4430
NEXT ASSY.	USED ON
APPLICATION	

		DATE
DRAFTSMAN	W.P. KIRATZIS	7, DEC. 1959
CHECKER		
ENGINEER		6/6/60
APPROVAL	(DW) M.H.	6/6/60
CONTRACT NO.		

SCHEMATIC PUNCH CONTROL CARD NO. 11

4343 MOD

L200006253

SCALE | UNIT WT.

L200006253

J12 (FSC) CARD 12 OFF-LINE SYSTEM CONTROL

PIN	LOGIC TERM	TIE POINTS										
A	-24m	POWER										
B												
C												
D												
E	H*	J21-T2	WR	J26-c1	V_1T/W							
F	H_7	J9-S	PC									
H	R_5	J28-X	JUNC	J28-Y	JUNC	J21-J2	WR	J25-S2	V_2T/W	J46-c	ACP	
J												
K	L_{s-2}	J46-K	ACP									
L	$\underline{A}_m$											
M	$\underline{G}_m$	J27-K	JUNC	J27-L	JUNC	J22-F1	XP	J28-K1	V_2T/W	J46-E	ACP	
N												
P	GND											
R												
S												
T	K_m	J25-X2	V_2T/W									
U	L_{t-2}	J46-H	ACP	J22-P2 XP								
V	$\underline{I}_m$	J21-D2	WR									
W	L_{x-1}	J46-b	ACP									
X	I_m											
Y	$\underline{R}_4$	J28-V	JUNC	J28-W	JUNC	J22-V2	XP	J25-H2	V_2T/W			
Z	W_{14b}	J8-d	RC	J21-R1	WR							
a	L_{y-1}	J46-a	ACP									
b	L_{s-3}	J46-L	ACP									
c	$\underline{H}^*$											
d	A_m	J46-m	ACP	J25-S1	V_2T/W							
e	$\underline{H}_7$											
f	H_7*	J21-C1	WR	J26-h2	V_1T/W							
h	$\underline{H}'$	J13-V	FSC									
j												
k	+24m	POWER										

NOTES:
1. ALL RESISTORS 1/2W ±5% CARBON UNLESS OTHERWISE STATED.
2. ALL TRANSISTORS TO BE 2N1130, PER L532000521 OR EQUIV., PER ES L531000521.
3. ALL DIODES TO BE CTP-790 PER L531000523.

SYM	DESCRIPTION	DATE	APPROVAL
1	EO# 54804 CHANGED C_9 1 .004MF TO 0.003MF	9-13-60 9-22-60	

K 30K R1 -24V
Ls-2
Am d
2K R5
R6 100Ω
C1 47µf 100µf
GND.
R7 11K
R8 11K
C2 .001µf
2K R2
Q1 Q2
47K R11
47K R12
GRD
+24V
5100Ω R17
2K R16
CR1
H* c
C4 .01µf
3900Ω R15
Km T
R5 H
Am L
f H7
e H7
2K R3
R9 11K
R10 11K
2K R4
Q3 Q4
47K R13
47K R14
A -24m
F H7
k +24m
GND.
56K R19
CR3
C3 .01µf
R18 2400Ω
CR2
5100Ω R20
h H'
R21 6800Ω
+24V
-24V
56K R24
2K R25
C5 .003µf
R23 15K
20K R22
Q5
R31 10K
Lt-2 U
GRD
C6 .05µf #22
62K R26
CR4
10K R32 300K
30K R33
R27 20K
R28 10K
47K R29
5600Ω R30 Im'
Q6
C7 .01µf
a Ly-1
b Ls-3
47K R38
-24V
820Ω 1W R37
Q8
R43 2400Ω
E H*
.01µf C8
CR5
P GROUND
L2000006254
18K R36
27K R35
47K R34
R4 Y
Im V
R39 11K
Q7
GND.
M Gm
X Im
2K R40
R41 11K
2K R42
R44 11K
Q9 Q10
47K R46
47K R47
+24V
GRD
12K R45
12K R49
2K R48
Z W146
W Lx-1
.0039µf C9

L535000902	4430
NEXT ASSY.	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DIMENSIONS
FRACTIONAL 2 PLACES ± .010
3 PLACES ± .02 4 PLACES ± .0005
ANGLES ± 1° BREAK EDGES .005 MAX.
SURFACE FINISH 125
DO NOT SCALE THIS DRAWING
MATERIAL

ITEM	REQ'D	NO.	DESCRIPTION	MATL.	MATL. SPEC.	UNIT WT.

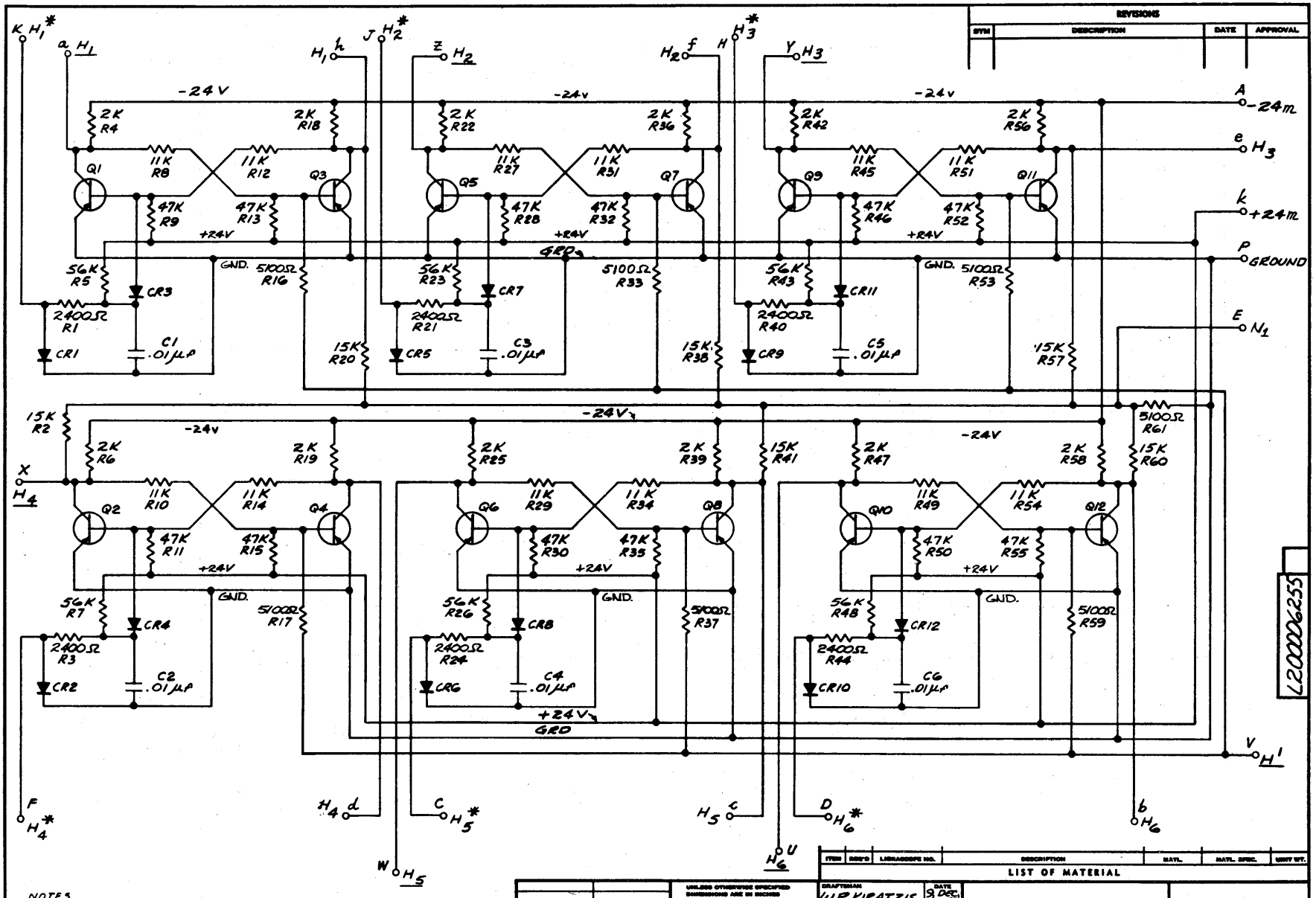
LIST OF MATERIAL

DRAFTSMAN W.P. KIRATZIS	DATE 11 DEC. 1959	SCHEMATIC SYSTEM CONTROL (OFF-LINE) CARD #12
CHECKER		
ENGINEER	6/3/60	
APPROVAL	6/6/60	
CONTRACT NO.		SCALE / UNIT WT.

4343 MOD
L2000006254

J13 (FSC) CARD 13 OFF-LINE SYSTEM CONTROL

PIN	LOGIC TERM	TIE POINTS				
A	-24m	POWER				
B						
C	H_5*	J21-c1	WR	J26-X2	V_1T/W	
D	H_6*	J21-c2	WR	J26-D1	V_1T/W	
E	N_1	J46-J	ACP			
F	H_4*	J21-B1	WR	J26-X1	V_1T/W	
H	H_3*	J21-d1	WR	J26-d1	V_1T/W	
J	H_2*	J21-d2	WR	J26-Z1	V_1T/W	
K	H_1*	J21-L1	WR	J26-a1	V_1T/W	
L						
M						
N						
P	GND					
R						
S						
T						
U	$\underline{H_6}$					
V	$\underline{H'}$	J12-h	FSC			
W	$\underline{H_5}$					
X	$\underline{H_4}$					
Y	$\underline{H_3}$					
Z	$\underline{H_2}$					
a	$\underline{H_1}$					
b	H_6	J9-T	PC	J15-f	T/WC	
c	H_5	J9-U	PC	J15-e	T/WC	
d	H_4	J9-V	PC	J15-W	T/WC	
e	H_3	J9-W	PC	J15-X	T/WC	
f	H_2	J9-X	PC	J15-H	T/WC	
h	H_1	J9-Y	PC	J15-F	T/WC	
j						
k	+24m	POWER				


REVISIONS
SYM
DESCRIPTION
DATE
APPROVAL
-24 V
+24V
GND
2K R4
2K R18
11K R8
11K R12
47K R9
47K R13
Q1
Q3
56K R5
5100Ω R16
CR3
2400Ω R1
CR1
C1 .01μF
15K R20
2K R22
2K R36
11K R27
11K R31
47K R28
47K R32
Q5
Q7
56K R23
5100Ω R33
CR7
2400Ω R21
CR5
C3 .01μF
15K R38
2K R42
2K R56
11K R45
11K R51
47K R46
47K R52
Q9
Q11
56K R43
5100Ω R53
CR11
2400Ω R40
CR9
C5 .01μF
15K R57
A -24m
e H3
k +24m
P GROUND
E N1
15K R2
2K R6
2K R19
11K R10
11K R14
47K R11
47K R15
Q2
Q4
56K R7
5100Ω R17
CR4
2400Ω R3
CR2
C2 .01μF
2K R25
2K R39
11K R29
11K R34
47K R30
47K R35
Q6
Q8
56K R26
5100Ω R37
CR8
2400Ω R24
CR6
C4 .01μF
15K R41
2K R47
2K R58
11K R49
11K R54
47K R50
47K R55
Q10
Q12
56K R48
5100Ω R59
CR12
2400Ω R44
CR10
C6 .01μF
5100Ω R61
15K R60
V H1
X H4
F H4*
H4 d
C H5*
W H5
H5 c
D H6*
b H6
U H6
NOTES.
1. ALL RESISTORS ½ W ± 5% CARBON UNLESS OTHERWISE STATED.
2. ALL TRANSISTORS TO BE 2N1130, PER L532000521 OR EQUIV. PER ES-L532000521.
3. ALL DIODES TO BE CTP 790, PER L531000523
LIST OF MATERIAL
ITEM
ASS'D
LIBRASCOPE NO.
DESCRIPTION
MATL.
MATL. SPEC.
UNIT WT.
L535000864
4430
NEXT ASSY.
USED ON
APPLICATION
DO NOT SCALE THIS DRAWING
MATERIAL
DRAFTSMAN
W.P. KIRATZIS
DATE
9 DEC. 1959
CHECKER
ENGINEER APPROVAL
CONTRACT NO.
SCHEMATIC
SYSTEM CONTROL
(OFF-LINE) CARD #13
SCALE
UNIT WT.
200006255

J14 (T/WC) CARD 14 T/W

PIN	LOGIC TERM	TIE POINTS											
A	-24m	POWER											
B	V_{9c}	J26-j2	V_1T/W										
C	V_{10c}	J26-F1	V_1T/W										
D	V_{11c}	J26-H2	V_1T/W										
E	V_{12c}	J26-J2	V_1T/W										
F	V_{14c}	J26-d2	V_1T/W										
H	V_{13c}	J26-K2	V_1T/W										
J	-24c	POWER											
K	B_{5p}	J42-p	ND	J2-e	NSC	J8-K	RC	J11-W	PC	J29-K	AT/WC		
L	B_{6p}	J42-r	ND	J2-c	NSC	J8-Y	RC	J11-a	PC	J29-L	AT/WC		
M	B_{4p}	J42-n	ND	J1-e	NSC	J8-J	RC	J11-X	PC	J29-M	AT/WC		
N	B_{1p}	J42-f	ND	J1-b	NSC	J8-D	RC	J11-Z	PC	J29-N	AT/WC		
P	GND												
R	V_{11y}	J9-j	PC	J25-X1	V_2T/W								
S	Q_o'	J17-Y	T/WC										
T	B_{2p}	J42-j	ND	J1-c	NSC	J8-F	RC	J11-Y	PC	J29-T	AT/WC		
U	B_{3p}	J42-k	ND	J1-d	NSC	J8-H	RC	J11-U	PC	J29-U	AT/WC		
V	N_6	P49-n	PCU										
W	S	J42-V	ND	J4-T	NSC	J5-d	NSC	J8-W	RC	J11-R	PC	J17-d	T/WC
		J32-d	AT/WC	J29-W	AT/WC								
X	$\underline{Q_i}$	J16-R	T/WC										
Y													
Z													
a													
b													
c	Q_i	J25-Y1	V_2T/W	J17-R	T/WC	J17-C	T/WC						
d	V_{6x}	J25-J2	V_2T/W	J17-c	T/WC								
e	L_{m-1}	J46-N	ACP										
f													
h													
j													
k	+24m	POWER											

NOTES
1. ALL RESISTORS 1/2W ±5% CARBON UNLESS OTHERWISE STATED.
2. ALL TRANSISTORS TO BE 2N1130 PER L532000521 OR EQUIV PER ES. L532000521.
3. ALL DIODES TO BE CTP 790 PER. L531000523.
4. SYMBOLS ENCLOSED BY DASHED LINES APPLY ONLY WHEN CARD 14 IS USED AT CARD POSITION 29, FOR 2nd TYPEWRITER.

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
1	CHANGED .004μf TO .0039μf, CIRCUIT BOARD TO SCHEMATIC AD DED [1] TERMINAL SYMBOLS, NOTE 4 EDS 4800	11/16/64	
2	REVISED PER E.O. 57033	11/18/64	DEDOYLE

B1P B32P B3P B64P B6P B65P S GRD -24m
N U L W J A
B2P B4P B5P -24c +24m
T M K k

Vgc B R1 5600Ω — 9100Ω R7
V10c C R2 5600Ω — 9100Ω R8
V11c D R3 5600Ω — 9100Ω R9
V12c E R4 5600Ω — 9100Ω R10
V14c F R5 5600Ω — 9100Ω R11
V13c H R6 5600Ω — 9100Ω R12

6200Ω R13 · 6200Ω R14 · 6200Ω R15 · 6200Ω · 6200Ω · 6200Ω
CR1
4700Ω R17 · 4700Ω R21
Q1 · Q1' · Q2 · Q2'
2400Ω R18 · 6200Ω R19
47K R16 · C2 220 μμf · 47K R20
GND · +24V

2700Ω R27 · 9100Ω R28
6200Ω R22 · 6200Ω R23 · 6200Ω · 6200Ω · 6200Ω
Q3 · CR2 · 47K R26 · +24V · GND

3300Ω R30 · −24V · 1200Ω 1W R37
R31 11K · R35 [2] 9.1K
Q4 · Q5
47K R32 · 47K R36
GND. · +24V
12K R29 · 12K R33 · 2K R34
[1] .0039 μf C3 · 2K R38 · 1800Ω R39 · 240K R40

X Qy Qc
c Qy Qc
e Lo-1 Lm-1
NOT USED V6x

NOT USED R V11y
NOT USED V N6
1500Ω R24 · 47Ω R25 · C1 20μf · GND.
CR3
S Q'o Q'y

L200007202 1

L535000 814	4450		
NEXT ASSY.	USED ON		
APPLICATION			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DIMENSIONS
FRACTIONAL 3 PLACES ±.
2 PLACES ±.02 4 PLACES ±.005
ANGLES ±1° BREAK EDGES .005 MAX
SURFACE FINISH 125
DO NOT SCALE THIS DRAWING
MATERIAL

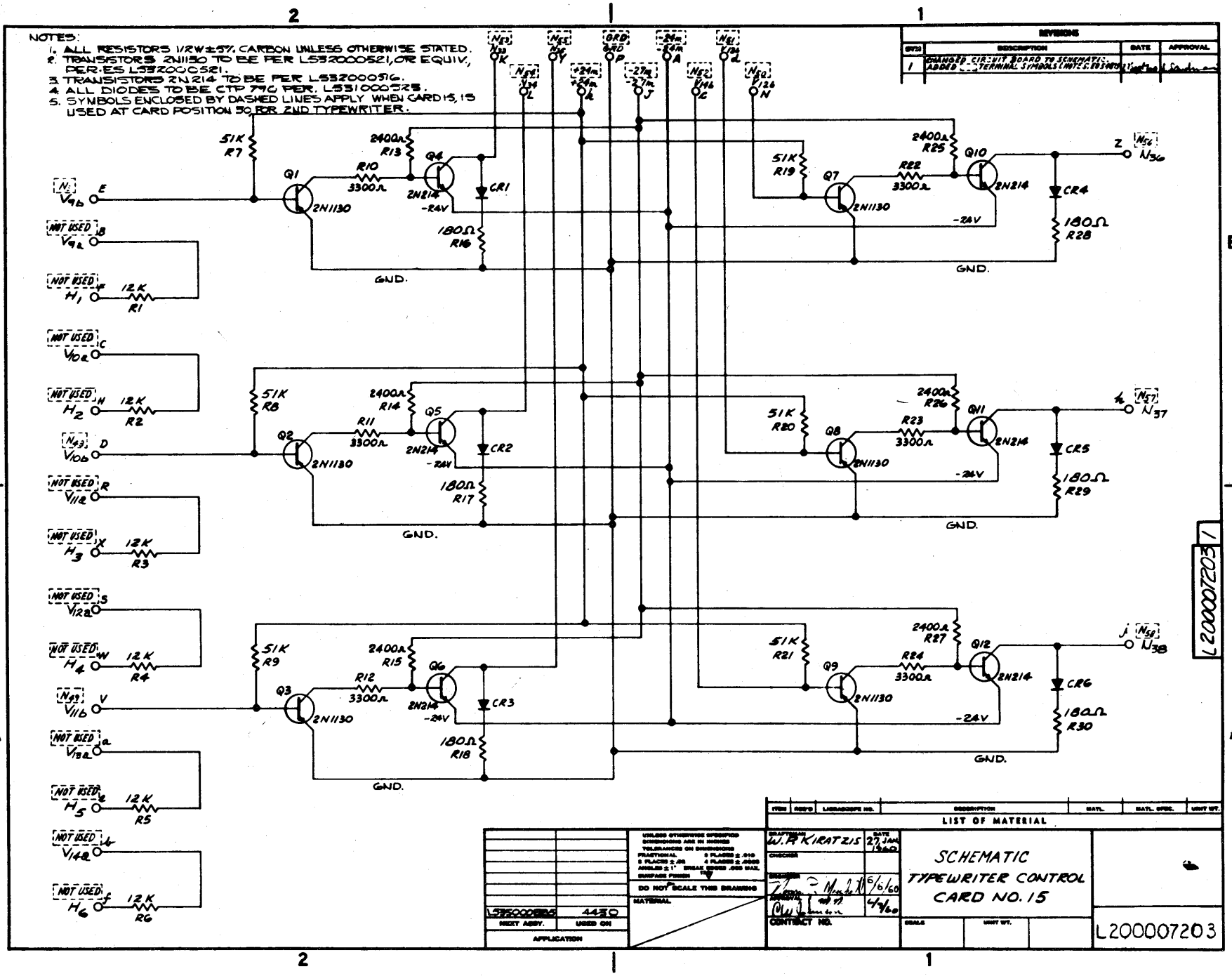
LIST OF MATERIAL

DRAFTSMAN W.R.K / RATZIS	DATE 28 JAN 1960	SCHEMATIC TYPEWRITER CONTROL CARD NO. 14
CHECKER		
ENGINEER		
APPROVAL	4/5/60	
CONTRACT NO.	SCALE	UNIT WT.

L200007202

J15 (T/WC) CARD 15 T/W CONTROL

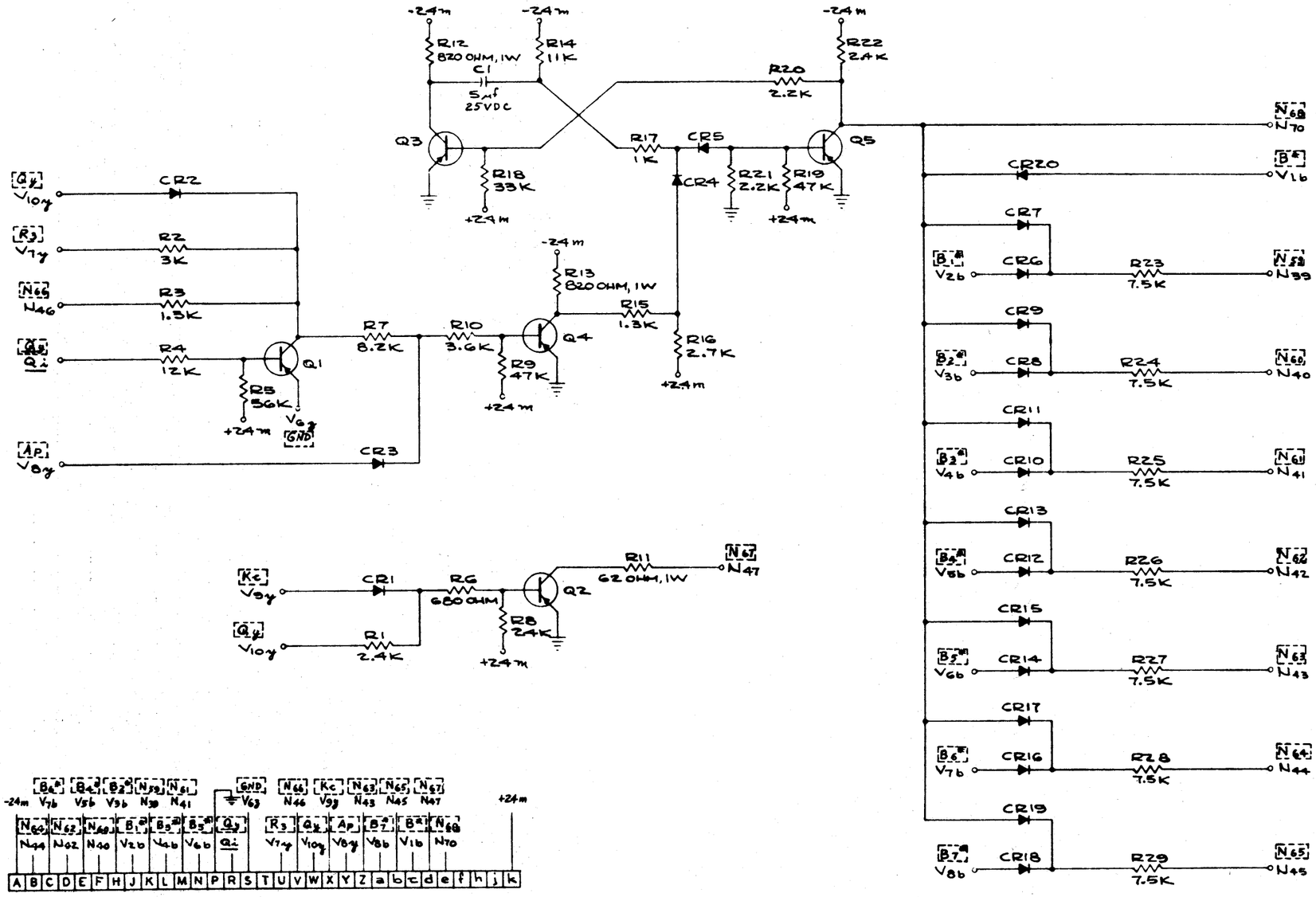
PIN	LOGIC TERM	TIE POINTS				
A	-24m	POWER				
B	V_{9a}	J26-f2	V_1T/W			
C	V_{10a}	J26-E2	V_1T/W			
D	V_{10b}	J26-E1	V_1T/W			
E	V_{9b}	J26-h1	V_1T/W			
F	H_1	J13-h	FSC	J9-Y	PC	
H	H_2	J13-f	FSC	J9-X	PC	
J	-27m	POWER				
K	N_{33}	J44-AA	T/WU			
L	N_{34}	J44-BB	T/WU			
M						
N	V_{12b}	J26-J1	V_1T/W			
P	GND					
R	V_{11a}	J26-H1	V_1T/W			
S	V_{12a}	J26-e2	V_1T/W			
T						
U						
V	V_{11b}	J26-F2	V_1T/W			
W	H_4	J13-d	FSC	J9-V	PC	
X	H_3	J13-e	FSC	J9-W	PC	
Y	N_{35}	J44-CC	T/WU			
Z	N_{36}	J44-DD	T/WU			
a	V_{13a}	J26-K1	V_1T/W			
b	V_{14a}	J26-S2	V_1T/W			
c	V_{14b}	J26-T2	V_1T/W			
d	V_{13b}	J26-T1	V_1T/W			
e	H_5	J13-c	FSC	J9-U	PC	
f	H_6	J13-b	FSC	J9-T	PC	
h	N_{37}	J44-EE	T/WU			
j	N_{38}	J44-FF	T/WU			
k	+24m	POWER				


NOTES:
1. ALL RESISTORS 1/2W ±5% CARBON UNLESS OTHERWISE STATED.
2. TRANSISTORS 2N1130 TO BE PER L5532000521, OR EQUIV., PER ES L5532000521.
3. TRANSISTORS 2N 214 TO BE PER L5532000516.
4. ALL DIODES TO BE CTP 796 PER. L5531000325.
5. SYMBOLS ENCLOSED BY DASHED LINES APPLY WHEN CARD IS, IS USED AT CARD POSITION 30 FOR 2ND TYPEWRITER.
REVISIONS
DESCRIPTION
DATE
APPROVAL
CHANGED CIRCUIT BOARD TO SCHEMATIC; ADDED TERMINAL SYMBOLS (NOTE 5, E03460)
SCHEMATIC
TYPEWRITER CONTROL
CARD NO. 15
L200007203
LIST OF MATERIAL
DO NOT SCALE THIS DRAWING
W.F.K/RAT 2.15
27 JAN 1960
6/6/60
4/4/60
L5500080
4430
NEXT ASSY.
USED ON
APPLICATION
CONTRACT NO.
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
2N1130
2N214
CR1
CR2
CR3
CR4
CR5
CR6
51K R7
51K R8
51K R9
2400Ω R13
2400Ω R14
2400Ω R15
2400Ω R25
2400Ω R26
2400Ω R27
R10 3300Ω
R11 3300Ω
R12 3300Ω
R22 3300Ω
R23 3300Ω
R24 3300Ω
180Ω R16
180Ω R17
180Ω R18
180Ω R28
180Ω R29
180Ω R30
51K R19
51K R20
51K R21
12K R1
12K R2
12K R3
12K R4
12K R5
12K R6
GND.
-24V
NOT USED
E
B
F
C
H
D
R
X
S
W
V
a
k
b
f
Z
h
j

J16 (T/WC) CARD 16 T/W CONTROL

PIN	LOGIC TERM	TIE POINTS		
A	-24m	POWER		
B	N_{44}	J44-c	T/WU	
C	V_{7b}	J26-D2	V_1T/W	
D	N_{42}	J44-a	T/WU	
E	V_{5b}	J26-V1	V_1T/W	
F	N_{40}	J44-X	T/WU	
H	V_{3b}	J26-Y1	V_1T/W	
J	V_{2b}	J26-a2	V_1T/W	
K	N_{39}	J44-W	T/WU	
L	V_{4b}	J26-U1	V_1T/W	
M	N_{41}	J44-Y	T/WU	
N	V_{6b}	J26-W2	V_1T/W	
P	GND			
R	$\underline{Q_i}$	J14-X	T/WC	
S	V_{6z}	J25-N1	V_2T/W	
T				
U	V_{7y}	J25-T2	V_2T/W	
V	N_{46}	J44-k	T/WU	
W	V_{10y}	J25-V2	V_2T/W	
X	V_{9y}	J25-V1	V_2T/W	
Y	V_{8y}	J25-T1	V_2T/W	
Z	N_{43}	J44-b	T/WU	
a	V_{8b}	J26-j1	V_1T/W	
b	N_{45}	J44-Z	T/WU	
c	V_{1b}	J26-b1	V_1T/W	
d	N_{47}	J44-f	T/WU	
e	N_{70}			
f				
h				
j				
k	+24m	POWER		

SYM	DESCRIPTION	DATE	APPROVAL
2	REVISED & REDRAWN PER E.O. 68454	11/15/67	T. GARCY



PIN LAYOUT OF CARD

4. SYMBOLS ENCLOSED BY DASHED LINES APPLY WHEN CARD 16 IS USED - AT CARD POSITION 31, TYPEWRITER 4480.
3. ALL TRANSISTORS TO BE N400A PER L532000563.
2. ALL DIODES PER L531 000552.
1. ALL RESISTORS 1/2 W, ±5% CARBON UNLESS OTHERWISE SPECIFIED.

NOTES:

DRAFTSMAN	W.P. KIRATZIS	DATE	5 JAN 66
DESIGNER	[illegible]		5 FEB 66
ENGINEER	W.R. MARSHALL		2/11/66
APPROVAL	CAL JOHNSON		2/14/66
CONTRACT NO.			
5595 000 8716	4480		
NEXT ASSY	USED ON		
APPLICATION			

SCHEMATIC TYPEWRITER CONTROL CARD #16

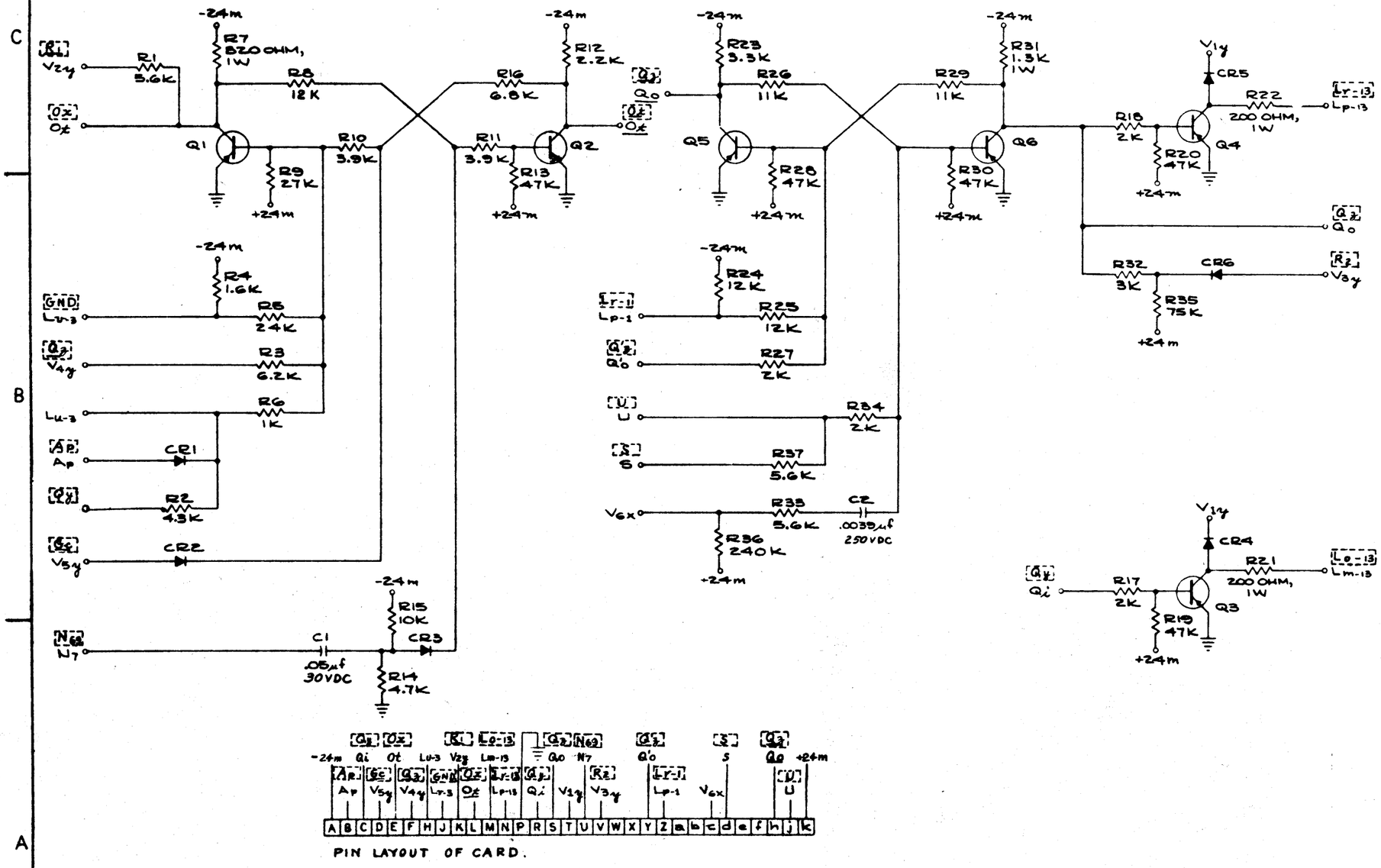
L200007204

J17 (T/WC) CARD 17 T/W CONTROL

PIN	LOGIC TERM	TIE POINTS											
A	-24m	POWER											
B	A_p	J27-H	JUNC	J27-J	JUNC	J6-N	NSC	J25-U1	V_2T/W	J31-Y	AT/WC	J46-k	ACP
		J32-B	AT/WC	J42-S	ND								
C	Q_i	J17-R	T/WC	J14-c	T/WC	J25-Y1	V_2T/W						
D	V_{5y}	J25-N2	V_2T/W										
E	O_t	J44-j	T/WU										
F	V_{4y}	J25-M1	V_2T/W										
H	L_{u-3}	J46-e	ACP										
J	L_{v-3}	J46-h	ACP	J25-R1	V_2T/W								
K	V_{2y}	J25-F1	V_2T/W										
L	$\underline{O_t}$												
M	L_{m-13}	J46-P	ACP										
N	L_{p-13}	J46-R	ACP										
P	GND												
R	Q_i	J14-c	T/WC	J17-C	T/WC	J25-Y1	V_2T/W						
S	Q_o												
T	V_{1y}	J25-D2	V_2T/W										
U	N_7	J44-U	T/WU										
V	V_{3y}	J25-F2	V_2T/W										
W													
X													
Y	Q_o'	J14-S	T/WC										
Z	L_{p-1}	J46-M	ACP										
a													
b													
c	V_{6x}	J14-d	T/WC	J25-J2	V_2T/W								
d	S	J42-V	ND	J4-T	NSC	J5-d	NSC	J8-W	RC	J11-R	PC	J14-W	T/WC
		J32-d	AT/WC	J29-W	AT/WC								
e													
f													
h	$\underline{Q_o}$	J25-P2	V_2T/W										
j	U	J42-W	ND	J4-c	NSC	J11-M	PC	J32-j	AT/WC				
k	+24m	POWER											

L200 007 205

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
3	REVISED & REDRAWN PER E.C. 68455	2 NOV 60	DR MARCY

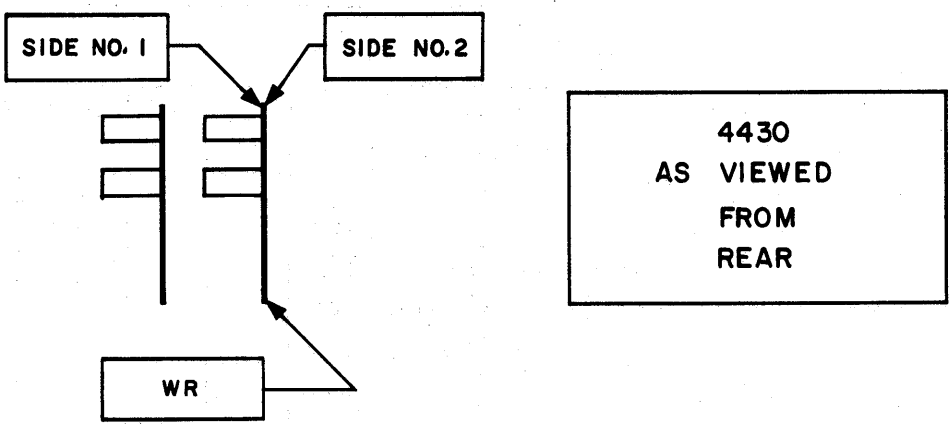


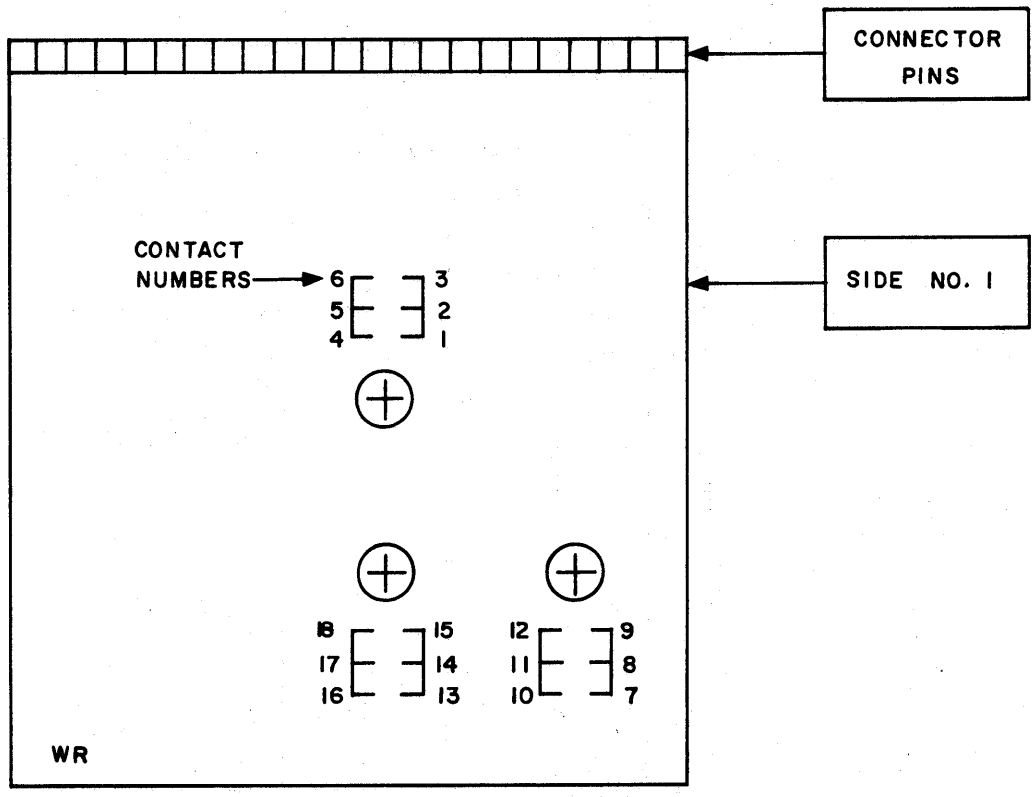
4. SYMBOLS ENCLOSED BY DASHED LINES APPLY WHEN CARD 17 IS USED. AT CARD POSITION 32, TYPEWRITER 4480.
3. ALL TRANSISTORS TO BE N400A PER L532 000563.
2. ALL DIODES PER L531 000552.
1. ALL RESISTORS 1/2W. ± 5% CARBON UNLESS OTHERWISE SPECIFIED.

NOTES:

		DRAFTSMAN J.P.KYRATZIS	9/1/60	SCHEMATIC TYPEWRITER CONTROL CARD NO.17
		ENGINEER A.M.JAFFRAY	9/1/60	
		ENGINEER J.P.MARSHALL	9/1/60	
L530 020 06	4480	APPROVAL C.M. JOHNSON	9/1/60	L200 007 205
MFG ASSY.	MODEL NO.	CONTRACT NO.		
APPLICATION				

L200 007 205





RELAY BOARD W - RELAY LOCATION DIAGRAM

J21 (WR) W READER RELAY CARD

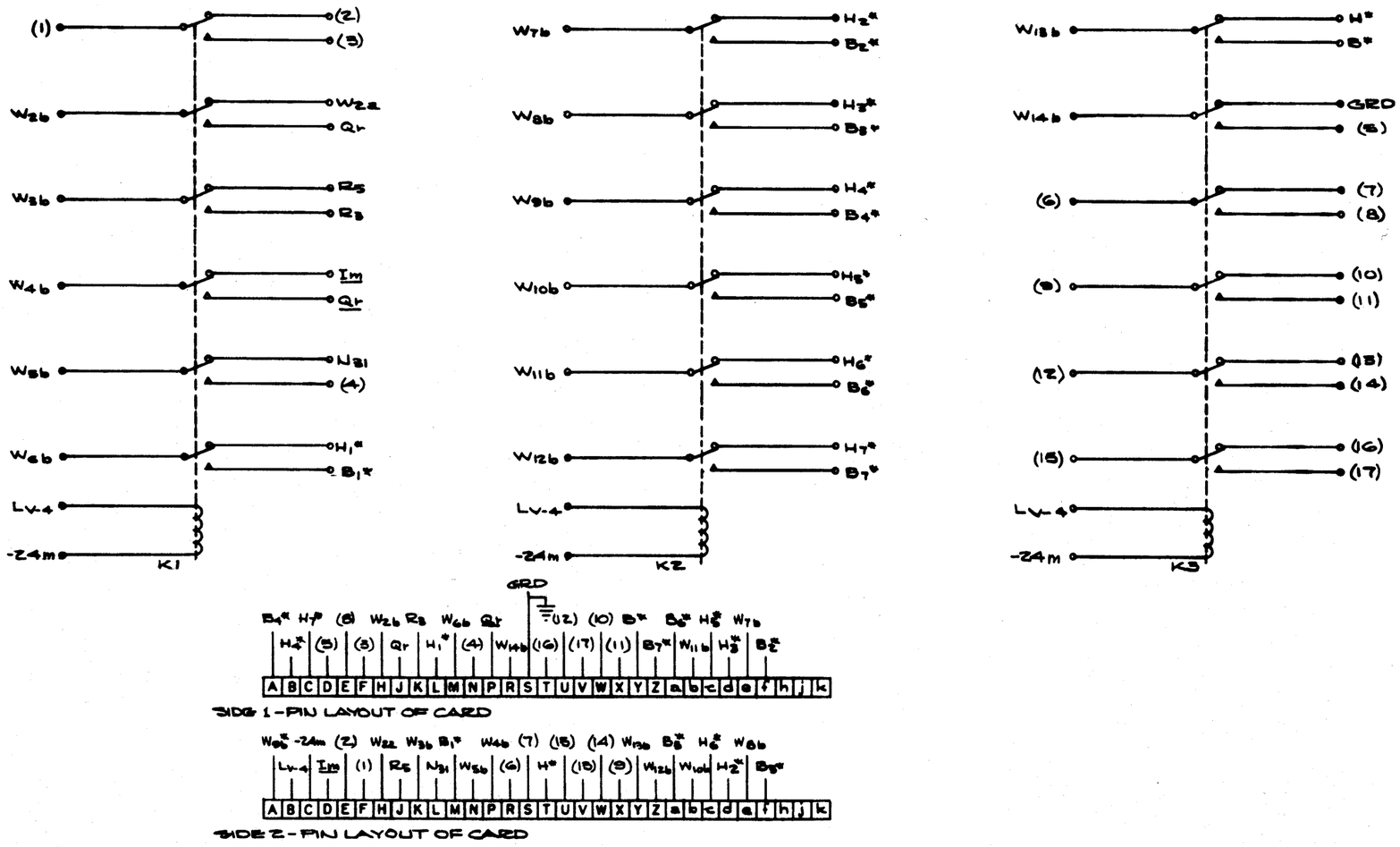
PIN	LOGIC TERM	CONTACT	SWITCH POINTS	TIE POINTS							
A1	B_4*	9NO	A2	J27-X	JUNC	J27-W	JUNC	J1-T	NSC	J26-V2	V_1T/W
				J31-E	AT/WC	J42-F	ND				
A2	W_{9b}	9OS	A1,B1	J7-V	RC						
B1	H_4*	9NC	A2	J13-F	FSC	J26-X1	V_1T/W				
B2	L_{v4}			J46-j	ACP	(RELAY COIL)					
C1	H_7*	12NC	Z2	J12-f	FSC	J26-h2	V_1T/W				
C2	-24m			J28e	JUNC	(RELAY COIL)					
D1		14NO	R1								
D2	$\underline{I}$m	4NC	P2	J12-V	FSC						
E1	$\underline{Q}$r	15NO	R2	JUMPER	ON CARD TO:			P-1	4NO		
E2		1NC	F2								
F1		1NO	F2								
F2		1OS	E2,F1								
H1	W_{2b}	2OS	H2,J1	J8-f	RC						
H2	W_{2a}	2NC	H1	J7-J	RC						
J1	Q_r	2NO	H1	J8-S	RC						
J2	R_5	3NC	K2	J28-Y	JUNC	J28-X	JUNC	J12-H	FSC	J25-S2	V_2T/W
				J46-c	ACP						
K1	R_3	3NO	K2	J27-B	JUNC	J27-A	JUNC	J6-b	NSC	J25-U2	V_2T/W
				J31-U	AT/WC	J42-N	ND				
K2	W_{3b}	3OS	J2,K1	P50-26	RPU						
L1	H_1*	6NC	M1	J13-K	FSC	J26-a1	V_1T/W				
L2	N_{31}	5NC	N2	J28-k	JUNC	J28-j	JUNC	J11-E	PC	J22-Y1	XP
				J25-H1	V_2T/W						
M1	W_{6b}	6OS	L1,M2	J7-R	RC						
M2	B_1*	6NO	M1	J27-R	JUNC	J27-P	JUNC	J1-N	NSC	J26-Z2	V_1T/W
				J31-J	AT/WC	J42-B	ND				
N1		5NO	N2								
N2	W_{5b}	5OS	L2,N1	J8-M	RC						
P1	$\underline{Q}_r$	4NO	P2	J8-X	RC						
P2	W_{4b}	4OS	D2,P1	J8-E	RC						
R1	W_{14b}	14OS	S1,D1	J8-d	RC	J12-Z	FSC				
R2	W_{4b}	15OS	S2,E1	JUMPER	ON CARD TO:			P-2	4OS		
S1	GND	14NC	R1	J28D	JUNC						
S2	I_m	15NC	R2	JUMPER	ON CARD TO:			D-2	4NC		
T1		18NC	U2								
T2	H*	13NC	Y2	J12-E	FSC	J26-c1	V_1T/W				

J21 (WR) W READER RELAY CARD

PIN	LOGIC TERM	CONTACT	SWITCH POINTS	TIE POINTS							
U1		17OS	V2,W2								
U2		18OS	T1,V1								
V1		18NO	U2								
V2		17NC	U1								
W1		16NC	X2								
W2		17NO	U1								
X1		16NO	X2								
X2		16OS	W1,X1								
Y1	B*	13NO	Y2	J27-N	JUNC	J27-M	JUNC	J6-E	NSC	J26-b2	V_1T/W
				J31-c	AT/WC	J42-A	ND				
Y2	W_{13b}	13OS	T2,Y1	J7-D	RC						
Z1	B_7*	12NO	Z2	J27-d	JUNC	J27-c	JUNC	J2-T	NSC	J26-k1	V_1T/W
				J31-a	AT/WC	J42-L	ND				
Z2	W_{12b}	12OS	C1,Z1	J7-f	RC						
a1	B_6*	11NO	b1	J27-b	JUNC	J27-a	JUNC	J2-U	NSC	J26-k2	V_1T/W
				J31-C	AT/WC	J42-K	ND				
a2	B_5*	10NO	b2	J27-Z	JUNC	J27-Y	JUNC	J2-V	NSC	J26-W1	V_1T/W
				J31-N	AT/WC	J42-H	ND				
b1	W_{11b}	11OS	c2,a1	J7-d	RC						
b2	W_{10b}	10OS	c1,a2	J7-b	RC						
c1	H_5*	10NC	b2	J13-C	FSC	J26-X2	V_1T/W				
c2	H_6*	11NC	b1	J13-D	FSC	J26-D1	V_1T/W				
d1	H_3*	8NC	e2	J13-H	FSC	J26-d1	V_1T/W				
d2	H_2*	7NC	e1	J13-J	FSC	J26-Z1	V_1T/W				
e1	W_{7b}	7OS	d2,f1	J7-N	RC						
e2	W_{8b}	8OS	d1,f2	J7-M	RC						
f1	B_2*	7NO	e1	J27-T	JUNC	J27-S	JUNC	J1-M	NSC	J26-Y2	V_1T/W
				J31-H	AT/WC	J42-C	ND				
f2	B_3*	8NO	e2	J27-V	JUNC	J27-U	JUNC	J1-L	NSC	J26-U2	V_1T/W
				J31-L	AT/WC	J42-D	ND				
h1											
h2											
j1											
j2											
k1											
k2											

L200002353

DWG	DESCRIPTION	DATE	APPROVAL
2	REVISED & REDRAWN PER E.C.N. 44052	8 Aug 61	



L200002353

NOTES:

1. NUMBERS IN ( ) ARE FOR IDENTIFICATION ONLY REF. TO PRINTED CIRCUITRY

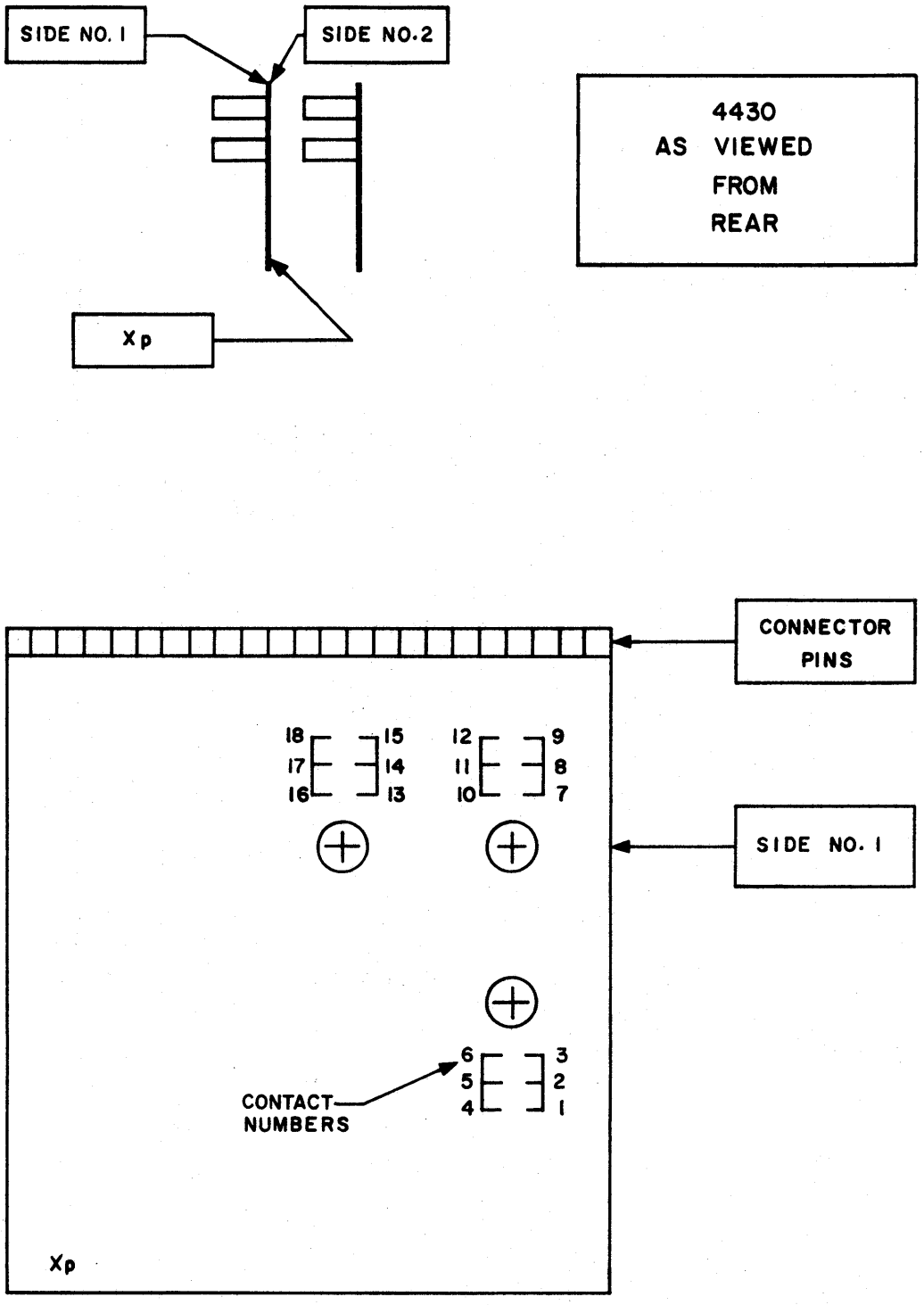
L536000511	4430
NEXT ASSY.	USED ON
APPLICATION	

DRAFTSMAN [illegible] DATE 11-16-59
CHECKED A. [illegible]
ENGINEER N.P. MALONE 12-1-60
APPROVAL
CONTRACT NO.

SCHEMATIC RELAY BOARD W

L200002353

SCALE NONE CODE SHEET OF



RELAY BOARD X - RELAY LOCATION DIAGRAM

J22 (XP) X PUNCH RELAY CARD

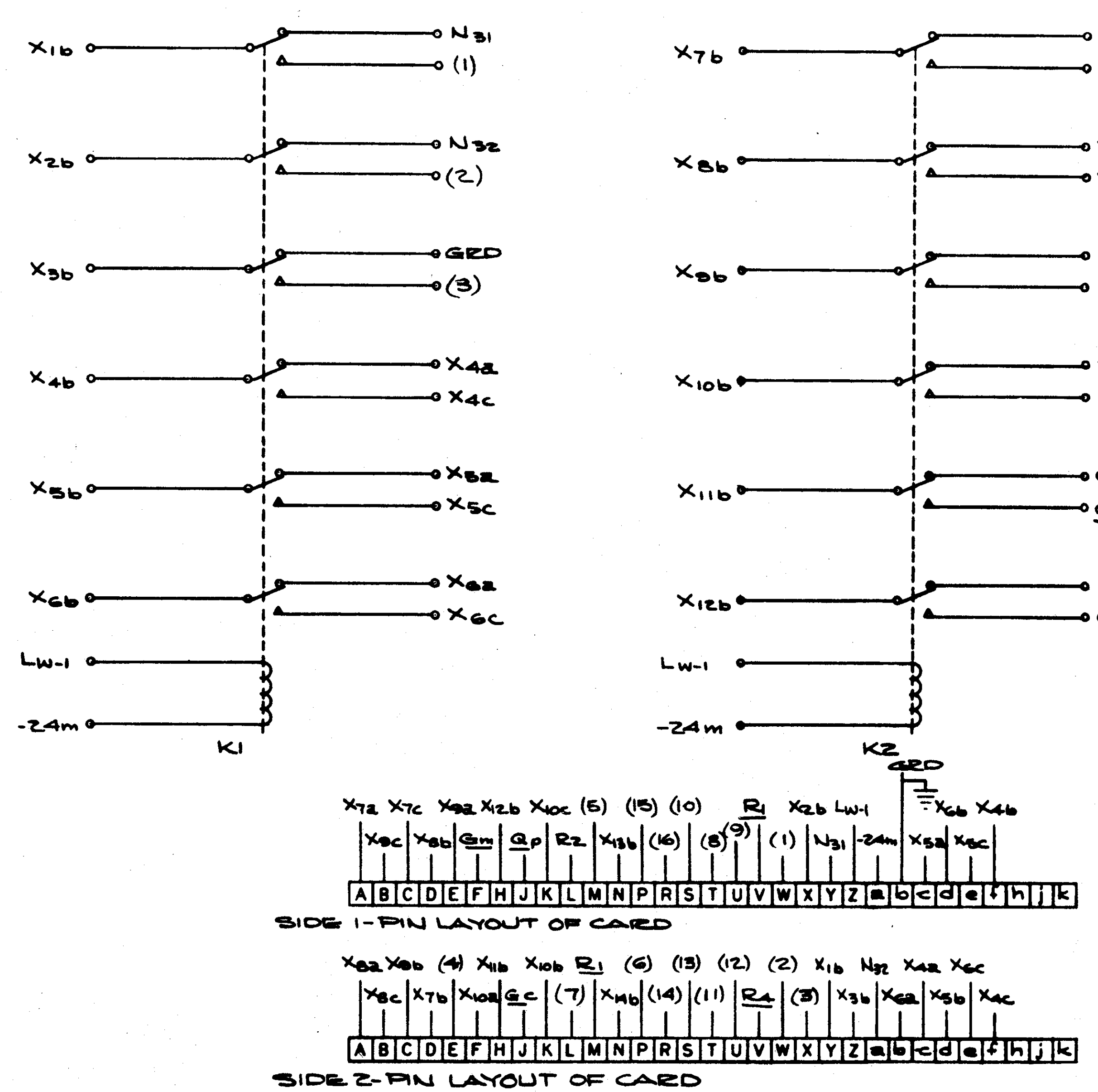
PIN	LOGIC TERM	CONTACT	SWITCH POINTS	TIE POINTS							
A1	X_{7a}	7NC	D2	J9-c	PC						
A2	X_{8a}	8NC	D1	J9-b	PC						
B1	X_{9c}	9NO	C2	J11-j	PC						
B2	X_{8c}	8NO	D1	J11-c	PC						
C1	X_{7c}	7NO	D2	J11-d	PC						
C2	X_{9b}	9OS	E1,B1	J10-D	PC						
D1	X_{8b}	8OS	A2,B2	J10-E	PC						
D2	X_{7b}	7OS	A1,C1	J10-F	PC						
E1	X_{9a}	9NC	C2	J9-a	PC						
E2		12NC	H1	J7-P	RC						
F1	$\underline{G}_m$	11NC	H2	J27-K	JUNC	J27-L	JUNC	J12-M	FSC	J25-K1	V_2T/W
				J46-E	ACP						
F2	X_{10a}	10NC	K2	J9-Z	PC						
H1	X_{12b}	12OS	E2,J1	J9-E	PC						
H2	X_{11b}	11OS	F1,J2	J9-J	PC						
J1	$\underline{Q}_p$	12NO	H1	J11-L	PC						
J2	$\underline{G}_c$	11NO	H2	J27-F	JUNC	J27-E	JUNC	J5-V	NSC	J25-P1	V_2T/W
				J32-D	AT/WC	J42-e	ND				
K1	X_{10c}	10NO	K2	J11-b	PC						
K2	X_{10b}	10-OS	F2,K1	J10-C	PC						
L1	R_2	14NO	N2	J27-D	JUNC	J27-C	JUNC	J5-D	NSC	J25-E1	V_2T/W
				J32-V	AT/WC	J42-b	ND				
L2		15NO	M1								
M1		15OS	P2,L2	J9-D	PC						
M2	$\underline{R}_1$	13NO	N1	J27-f	JUNC	J27-e	JUNC	J27-h	JUNC	J6-K	NSC
				J22-V1	XP	J25-E2	V_2T/W	J25-J1	V_2T/W	J32-K	AT/WC
				J42-Y	ND						
N1	X_{13b}	13OS	V2,M2	J10-B	PC						
N2	X_{14b}	14OS	V1,L1	J11-S	PC						
P1		18NC	R2								
P2		15NC	M1	J12-U	FSC						
R1		18NO	R2								
R2		18OS	P1,R1								
S1		16NO	T1								
S2		17NO	T2								
T1		16OS	U1,S1								
T2		17OS	U2,S2								

J-22 (XP) X PUNCH RELAY CARD

PIN	LOGIC TERM	CONTACT	SWITCH POINTS	TIE POINTS							
U1		16NC	T1								
U2		17NC	T2								
V1	$\underline{R_1}$	14NC	N2	J27-h	JUNC	J27-e	JUNC	J27-f	JUNC	J6-K	NSC
				J22-M2	XP	J25-E2	V_2T/W	J25-J1	V_2T/W	J32-K	AT/WC
				J42-Y	ND						
V2	$\underline{R_4}$	13NC	N1	J28-V	JUNC	J28-W	JUNC	J12-Y	FSC	J25-H2	V_2T/W
W1		1NO	Y2								
W2		2NO	X1								
X1	X_{2b}	2OS	a2,W2	J44-F	T/WU						
X2		3NO	Z2								
Y1	N_{31}	1NC	Y2	J28-j	JUNC	J28-k	JUNC	J11-E	PC	J21-L2	WR
				J25-H1	V_2T/W						
Y2	X_{1b}	1OS	Y1,W1	J11-H	PC						
Z1	L_{w-1}			J46-f	ACP	(RELAY	COIL)				
Z2	X_{3b}	3OS	b1,X2	J11-T	PC						
a1	-24m			J28-f	JUNC	(RELAY	COIL)				
a2	N_{32}	2NC	X1	J25-R2	V_2T/W						
b1	GND	3NC	Z2	J28-C	JUNC						
b2	X_{6a}	6NC	d1	J9-e	PC						
c1	X_{5a}	5NC	d2	J9-f	PC						
c2	X_{4a}	4NC	f1	J9-h	PC						
d1	X_{6b}	6OS	b2,e2	J10-L	PC						
d2	X_{5b}	5OS	c1,e1	J10-M	PC						
e1	X_{5c}	5NO	d2	J11-f	PC						
e2	X_{6c}	6NO	d1	J11-e	PC						
f1	X_{4b}	4OS	c2,f2	J10-N	PC						
f2	X_{4c}	4NO	f1	J11-h	PC						
h1											
h2											
j1											
j2											
k1											
k2											

SYM	DESCRIPTION	DATE	APPROVAL
3	REVISED & REDRAWN PER E.O. # 66083	1 AUG 61	DR. SEARCY

L200002354



1. NUMBERS IN ( ) ARE FOR IDENTIFICATION ONLY REF. TO PRINTED CIRCUITRY.

NOTES :

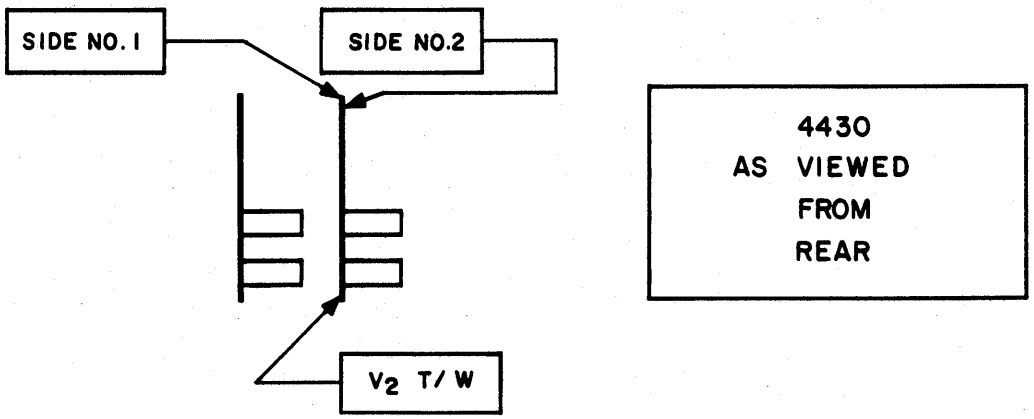
		DRAFTSMAN: L. COPPING	
		CHECKER	
		ENGINEER: N.P. MARSHALL	2/21/60
L536000509	4430	APPROVAL	
NEXT ASSY.	USED ON	CONTRACT NO.	
APPLICATION			

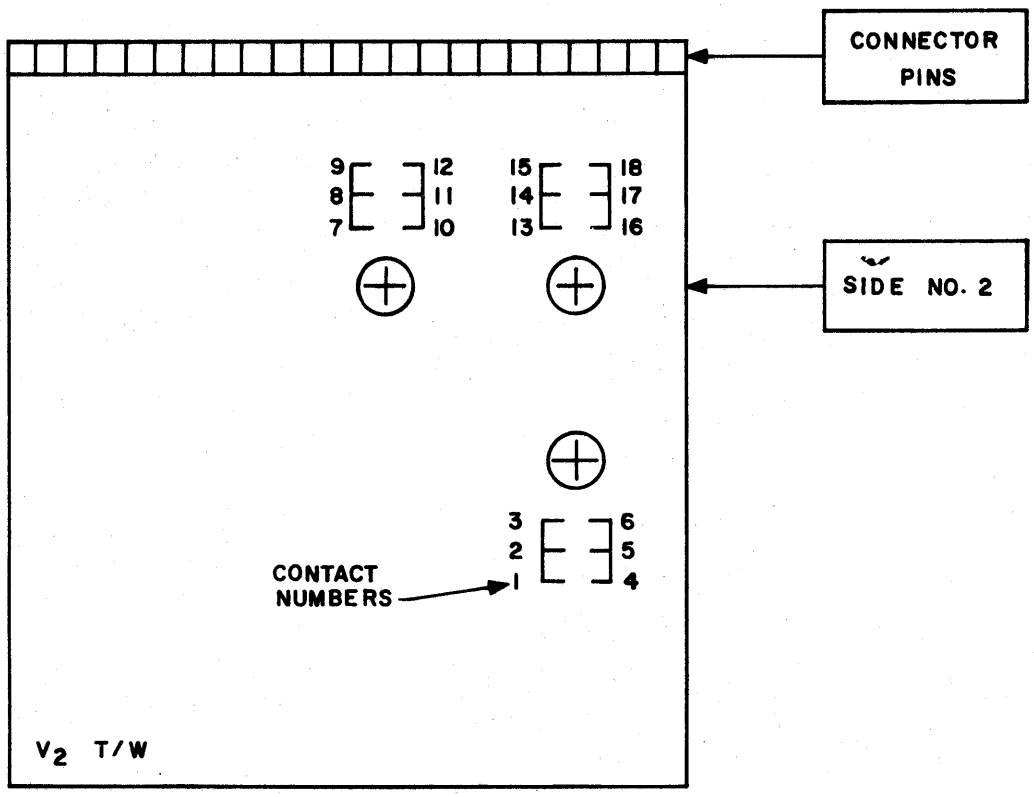
SCHEMATIC RELAY BOARD X

L200002354

SCALE | WT | CODE | SHEET 1 OF 1

L200002354





RELAY BOARD V_2 - RELAY LOCATION DIAGRAM

J25 (V_2 T/W) V_2 TYPEWRITER RELAY CARD

PIN	LOGIC TERM	CONTACT	SWITCH POINTS	TIE POINTS							
A1											
A2											
B1											
B2											
C1											
C2											
D1		1NO	D2								
D2	V_{1y}	1OS	H1,D1	J17-T	T/WC						
E1	R_2	3NO	F2	J27-C	JUNC	J27-D	JUNC	J5-D	NSC	J22-L1	XP
				J32-V	AT/WC	J42-b	ND				
E2	$\underline{R}_1$	2NO	F1	J27-e	JUNC	J27-f	JUNC	J27-h	JUNC	J6-K	NSC
				J22-M2	XP	J22-V1	XP	J25-J1	V_2T/W	J32-K	AT/WC
				J42-Y	ND						
F1	V_{2y}	2OS	H2,E2	J17-K	T/WC						
F2	V_{3y}	3OS	J1,E1	J17-V	T/WC						
H1	N_{31}	1NC	D2	J28-j	JUNC	J38-k	JUNC	J11-E	PC	J21-L2	WR
				J22-Y1	XP						
H2	$\underline{R}_4$	2NC	F1	J28-V	JUNC	J28-W	JUNC	J12-Y	FSC	J22-V2	XP
J1	$\underline{R}_1$	3NC	F2	J27-e	JUNC	J27-f	JUNC	J27-h	JUNC	J6-K	NSC
				J22-M2	XP	J22-V1	XP	J25-E2	V_2T/W	J32-K	AT/WC
				J42-Y	ND						
J2	V_{6x}	6NC	L1	J14-d	T/WC	J17-c	T/WC				
K1	$\underline{G}_m$	5NC	N2	J27-K	JUNC	J27-L	JUNC	J12-M	FSC	J22-F1	XP
				J46-E	ACP						
K2	L_{u-4}	RELAY	COIL	J27-j	JUNC	J27-k	JUNC	J26-f1	V_1T/W	J46-d	ACP
L1	GND	6OS	J2,N1	J28-C							
L2	-24m	RELAY	COIL	J28-a							
M1	V_{4y}	4OS	M2,P2	J17-F	T/WC						
M2		4NC	M1								
N1	V_{6z}	6NO	L1	J16-S	T/WC						
N2	V_{5y}	5OS	K1,P1	J17-D	T/WC						
P1	$\underline{G}_c$	5NO	N2	J27-E	JUNC	J27-F	JUNC	J5-V	NSC	J22-J2	XP
				J32-D	AT/WC	J42-e	ND				
P2	$\underline{Q}_o$	4NO	M1	J17-h	T/WC						
R1	L_{v-3}	10NC	V2	J17-J	T/WC	J46-h	ACP				
R2	N_{32}	11NC	X1	J22-a2	XP						
S1	A_m	8NC	T1	J12-d	FSC	J46-m	ACP				

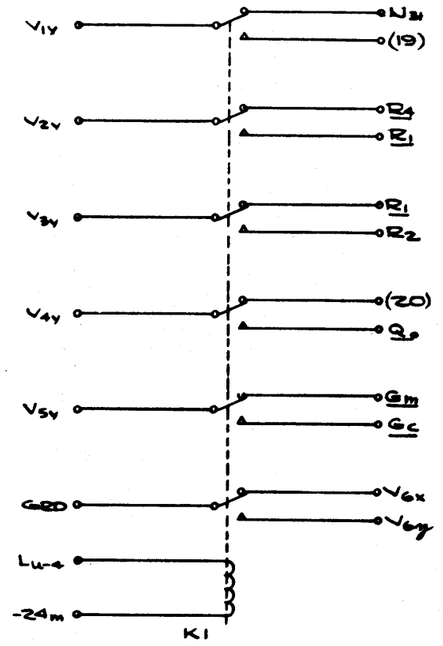
J25 (V_2 T/W) V_2 TYPEWRITER RELAY CARD

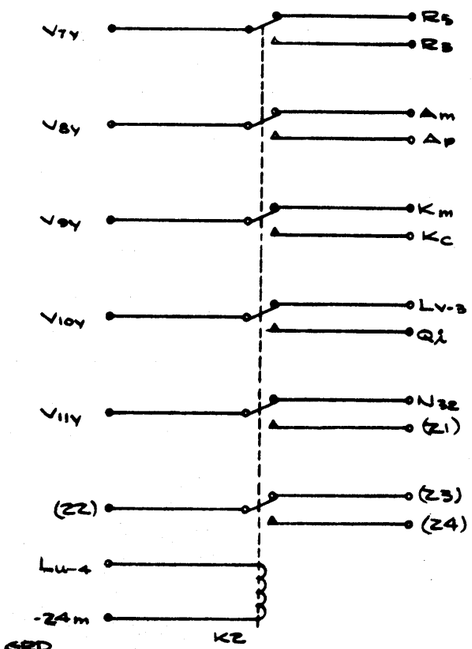
PIN	LOGIC TERM	CONTACT	SWITCH POINTS	TIE POINTS							
S2	R_5	7NC	T2	J28-X	JUNC	J28-Y	JUNC	J12-H	FSC	J21-J2	WR
				J46-c	ACP						
T1	V_{8y}	8OS	S1,U1	J16-Y	T/WC						
T2	V_{7y}	7OS	S2,U2	J16-U	T/WC						
U1	A_p	8NO	T1	J27-H	JUNC	J27-J	JUNC	J6-N	NSC	J31-Y	AT/WC
				J46-k	ACP	J32-B	AT/WC	J17-B	T/WC	J42-S	ND
U2	R_3	7NO	T2	J27-A	JUNC	J27-B	JUNC	J6-b	NSC	J21-K1	WR
				J31-U	AT/WC	J42-N	ND				
V1	V_{9y}	9OS	X2,W2	J16-X	T/WC						
V2	V_{10y}	10OS	R1,Y1	J16-W	T/WC						
W1		12NC	Z2								
W2	K_c	9NO	V1	J31-X	AT/WC	J42-T	ND	J6-M	NSC		
X1	V_{11y}	11OS	R2,Y2	J14-R	T/WC	J9-j	PC				
X2	K_m	9NC	V1	J12-T	FSC						
Y1	Q_i	10NO	V2	J14-c	T/WC	J17-R	T/WC	J17-C	T/WC		
Y2		11NO	X1								
Z1		12NO	Z2								
Z2		12OS	W1,Z1								
a1		13OS	b1,c2								
a2		16NO	f1								
b1		13NC	a1								
b2		16NC	f1								
c1		14NO	d1								
c2		13NO	a1								
d1		14OS	d2,c1								
d2		14NC	d1								
e1		15NC	f2								
e2		15NO	f2								
f1		16OS	b2,a2								
f2		15OS	e1,e2								
h1		18OS	h2,k2								
h2		18NC	h1								
j1		17NO	j2								
j2		17OS	k1,j1								
k1		17NC	j2								
k2		18NO	h1								

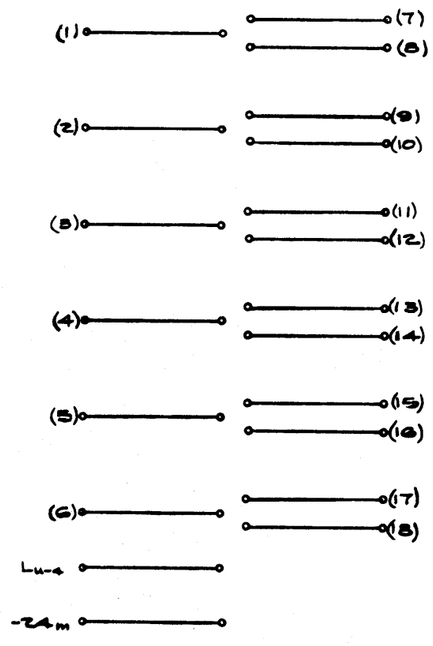
L200002350

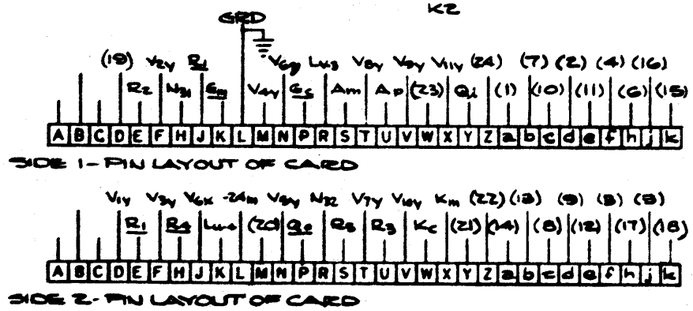
REVISIONS			
BY M	DESCRIPTION	APPROVAL	
2	REVISED & REDRAWN PER CO.'s COMMENTS	AUG 81	DR. SEVERCY

L200002350







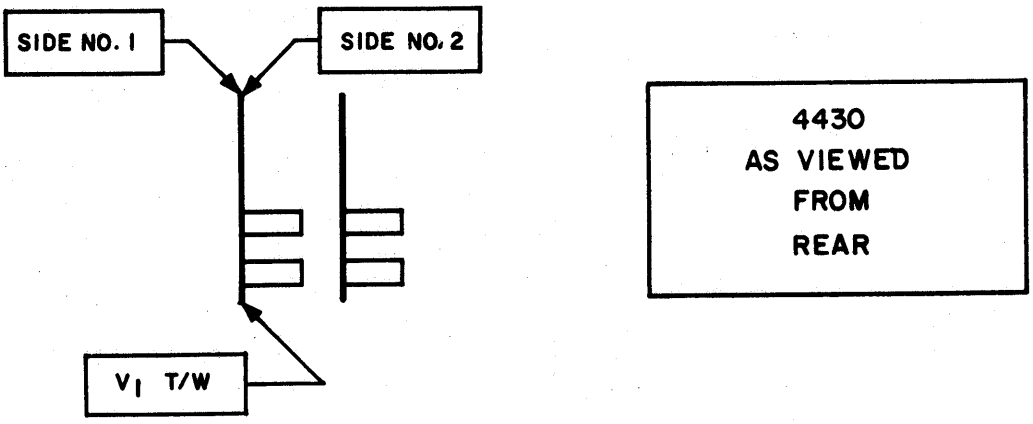


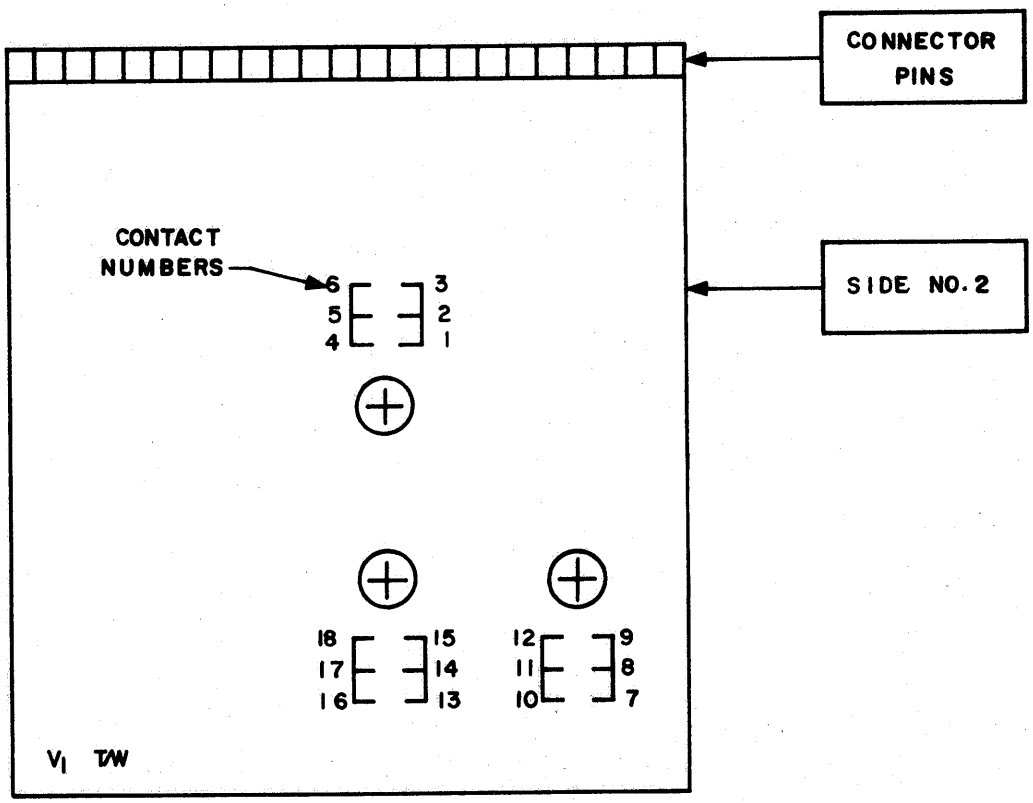
1. ALL NUMBERS IN ( ) ARE FOR IDENTIFICATION ONLY REF. TO PRINTED CIRCUITRY

NOTES:

		DRAFTSMAN C. L. COPPINGS	DATE 9/24/80	SCHEMATIC RELAY BOARD V2
		DESIGNER		
		ENGINEER R.P. MACSHANE	9/24/80	
		APPROVAL		
L5/85-000 308	4430	CONTRACT NO.		L200002355
NEXT ASSY.	USED ON			
APPLICATION		SCALE	SHT.	SHEET OF

L200002355





RELAY BOARD V_1 - RELAY LOCATION DIAGRAM

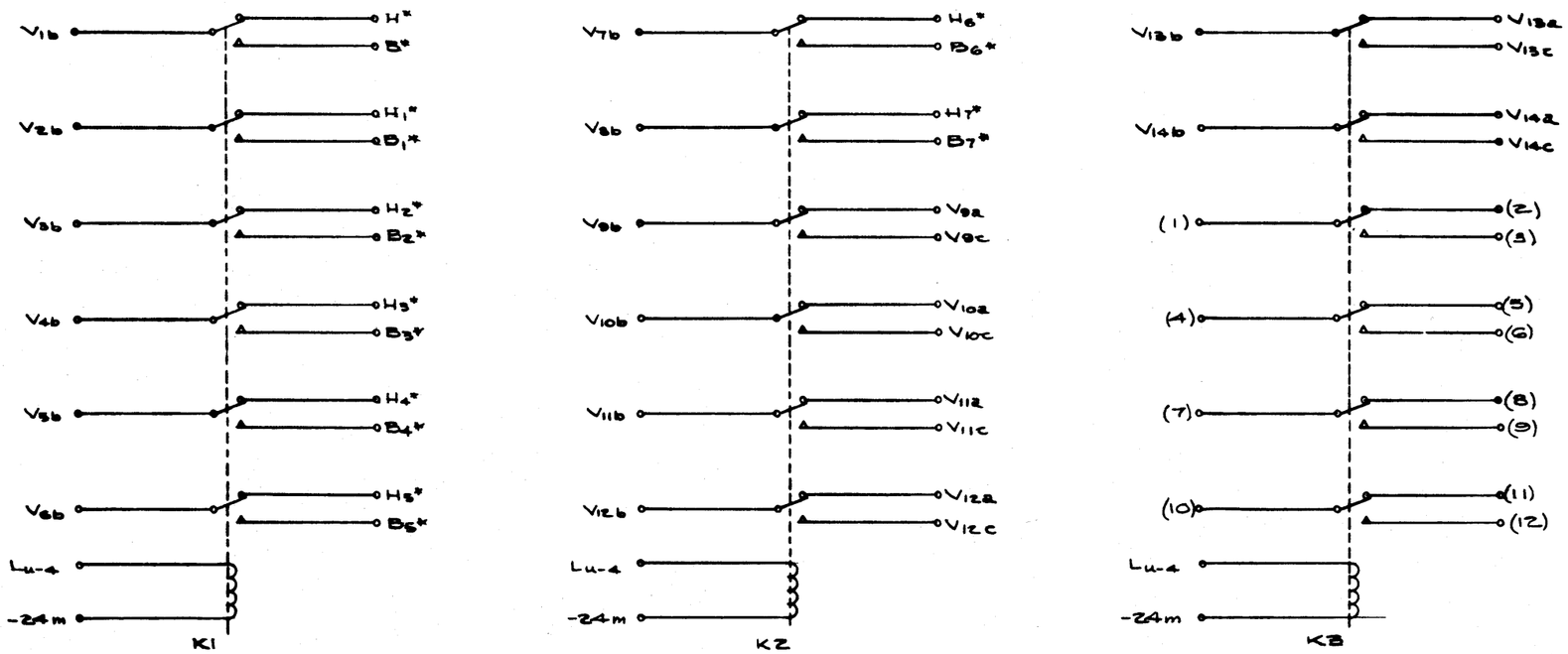
J26 (V_1 T/W) V_1 TYPEWRITER RELAY CARD

PIN	LOGIC TERM	CONTACT	SWITCH POINTS	TIE POINTS							
A1											
A2											
B1											
B2											
C1											
C2											
D1	H_6*	7NC	D2	J13-D	FSC	J21-c2	WR				
D2	V_{7b}	7OS	D1,k2	J16-C	T/WC						
E1	V_{10b}	10OS	E2,F1	J15-D	T/WC						
E2	V_{10a}	10NC	E1	J15-C	T/WC						
F1	V_{10c}	10NO	E1	J14-C	T/WC						
F2	V_{11b}	11OS	H1,H2	J15-V	T/WC						
H1	V_{11a}	11NC	F2	J15-R	T/WC						
H2	V_{11c}	11NO	F2	J14-D	T/WC						
J1	V_{12b}	12OS	e2,J2	J15-N	T/WC						
J2	V_{12c}	12NO	J1	J14-E	T/WC						
K1	V_{13a}	13NC	T1	J15-a	T/WC						
K2	V_{13c}	13NO	T1	J14-H	T/WC						
L1		16OS	L2,M2								
L2		16NC	L1								
M1		17NO	N2								
M2		16NO	L1								
N1		17NC	N2								
N2		17OS	N1,M1								
P1		18OS	R2,P2								
P2		18NO	P1								
R1		15NC	S1								
R2		18NC	P1								
S1		15OS	R1,c2								
S2	V_{14a}	14NC	T2	J15-b	T/WC						
T1	V_{13b}	13OS	K1,K2	J15-d	T/WC						
T2	V_{14b}	14OS	S2,d2	J15-c	T/WC						
U1	V_{4b}	4OS	d1,U2	J16-L	T/WC						
U2	B_3*	4NO	U1	J27-U	JUNC	J27-V	JUNC	J21-f2	WR	J1-L	NSC
				J31-L	AT/WC	J42-D	ND				
V1	V_{5b}	5OS	X1,V2	J16-E	T/WC						
V2	B_4*	5NO	V1	J27-W	JUNC	J27-X	JUNC	J1-T	NSC	J21-A1	
				J31-E	AT/WC	J42-F	ND				

J26 (V_1 T/W) V_1 TYPEWRITER RELAY CARD

PIN	LOGIC TERM	CONTACT	SWITCH POINTS	TIE POINTS							
W1	B_5*	6NO	W2	J27-Y	JUNC	J27-Z	JUNC	J2-V	NSC	J21-a2	WR
				J31-N	AT/WC	J42-H	ND				
W2	V_{6b}	6OS	X2,W1	J16-N	T/WC						
X1	H_4*	5NC	V1	J13-F	FSC	J21-B1	WR				
X2	H_5*	6NC	W2	J13-C	FSC	J21-c1	WR				
Y1	V_{3b}	3OS	Z1,Y2	J16-H	T/WC						
Y2	B_2*	3NO	Y1	J27-S	JUNC	J27-T	JUNC	J1-M	NSC	J21-f1	WR
				J31-H	AT/WC	J42-C	ND				
Z1	H_2*	3NC	Y1	J13-J	FSC	J21-d2	WR				
Z2	B_1*	2NO	a2	J27-P	JUNC	J27-R	JUNC	J1-N	NSC	J21-M2	WR
				J31-J	AT/WC	J42-B	ND				
a1	H_1*	2NC	a2	J13-K	FSC	J21-L1	WR				
a2	V_{2b}	2OS	a1,Z2	J16-J	T/WC						
b1	V_{1b}	1OS	c1,b2	J16-c	T/WC						
b2	B*	1NO	b1	J27-M	JUNC	J27-N	JUNC	J6-E	NSC	J21-Y1	WR
				J31-c	AT/WC	J42-A	ND				
c1	H*	1NC	b1	J12-E	FSC	J21-T2	WR				
c2		15NO	S1								
d1	H_3*	4NC	U1	J13-H	FSC	J21-d1	WR				
d2	V_{14c}	14NO	T2	J14-F	T/WC						
e1	-24m	RELAY	COIL	J28-b	JUNC						
e2	V_{12a}	12NC	J1	J15-S	T/WC						
f1	L_{u-4}	RELAY	COIL	J27-k	JUNC	J27-j	JUNC	J25-K2	V_2T/W	J46-d	ACP
f2	V_{9a}	9NC	h1	J15-B	T/WC						
h1	V_{9b}	9OS	f2,j2	J15-E	T/WC						
h2	H_7*	8NC	j1	J12-f	FSC	J21-C1	WR				
j1	V_{8b}	8OS	L2,k1	J16-a	T/WC						
j2	V_{9c}	9NO	h1	J14-B	T/WC						
k1	B_7*	8NO	j1	J27-c	JUNC	J27-d	JUNC	J2-T	NSC	J21-Z1	WR
				J31-a	AT/WC	J42-L	ND				
k2	B_6*	7NO	D2	J27-a	JUNC	J27-b	JUNC	J2-U	NSC	J21-a1	WR
				J31-C	AT/WC	J42-K	ND				

			L200002356
2	REVISED & REDRAWN PER ECO 66054		



V10a V11c V13c (6) (12) V14a B3* V6b B2* V2b (3) V12a H7* B6*

V7b V11b V12c (5) (7) (11) V14b B4* H5* B1* B* V14c V9a V9c

A B C D E F H J K L M N P R S T U V W X Y Z a b c d e f h j k

SIDE 2 - PIN LAYOUT OF CARD

V10b V11a V13a (9) (10) (1) V4b B5* V3b H1* H* -24m V8b B7*

H6* V10c V12b (4) (8) (2) V13b V5b H4* H2* V1b H3* Lu-4 V8a

A B C D E F H J K L M N P R S T U V W X Y Z a b c d e f h j k

SIDE 1 - PIN LAYOUT OF CARD

L200002356

NOTES:

1. NUMBERS IN ( ) ARE FOR IDENTIFICATION ONLY REF. TO PRINTED CIRCUITRY.

		DRAFTSMAN C.L. COPPING	DATE 11/14/61	SCHEMATIC RELAY BOARD V1
		CHECKER		
		ENGINEER N.P. MARSHALL	4/4/60	
		APPROVAL		
4336002510	4430	CONTRACT NO.		L200002356
NEXT ASSY.	USED ON			
APPLICATION		SCALE	WT	CODE / SHEET OF

BUSS CIRCUITS (JUNCTION CARDS)

LOGIC TERM	TIE POINTS										
B*	J27-M	JUNC	J27-N	JUNC	J6-E	NSC	J21-Y1	WR	J26-b2	V_1T/W	
	J31-c	AT/WC	J42-A	ND							
B_1*	J27-P	JUNC	J27-R	JUNC	J1-N	NSC	J21-M2	WR	J26-Z2	V_1T/W	
	J31-J	AT/WC	J42-B	ND							
B_2*	J27-S	JUNC	J27-T	JUNC	J1-M	NSC	J21-f1	WR	J26-Y2	V_1T/W	
	J31-H	AT/WC	J42-C	ND							
B_3*	J27-U	JUNC	J27-V	JUNC	J1-L	NSC	J21-f2	WR	J26-U2	V_1T/W	
	J31-L	AT/WC	J42-D	ND							
B_4*	J27-W	JUNC	J27-X	JUNC	J1-T	NSC	J21-A1	WR	J26-V2	V_1T/W	
	J31-E	AT/WC	J42-F	ND							
B_5*	J27-Y	JUNC	J27-Z	JUNC	J2-V	NSC	J21-a2	WR	J26-W1	V_1T/W	
	J31-N	AT/WC	J42-H	ND							
B_6*	J27-a	JUNC	J27-b	JUNC	J2-U	NSC	J21-a1	WR	J26-k2	V_1T/W	
	J31-C	AT/WC	J42-K	ND							
B_7*	J27-c	JUNC	J27-d	JUNC	J2-T	NSC	J21-Z1	WR	J26-k1	V_1T/W	
	J31-a	AT/WC	J42-L	ND							
$\underline{R}_1$	J27-e	JUNC	J27-f	JUNC	J27-h	JUNC	J6-K	NSC	J22-M2	XP	
	J22-V1	XP	J25-E2	V_2T/W	J25-J1	V_2T/W	J32-K	AT/WC	J42-Y	ND	
R_2	J27-C	JUNC	J27-D	JUNC	J5-D	NSC	J22-L1	XP	J25-E1	V_2T/W	
	J32-V	AT/WC	J42-b	ND							
R_3	J27-A	JUNC	J27-B	JUNC	J6-b	NSC	J21-K1	WR	J25-U2	V_2T/W	
	J31-U	AT/WC	J42-N	ND							
$\underline{R}_4$	J28-V	JUNC	J28-W	JUNC	J12-Y	FSC	J22-V2	XP	J25-H2	V_2T/W	
R_5	J28-X	JUNC	J28-Y	JUNC	J12-H	FSC	J21-J2	WR	J25-S2	V_2T/W	
	J46-c	ACP									
$\underline{G}_m$	J27-K	JUNC	J27-L	JUNC	J12-M	FSC	J22-F1	XP	J25-K1	V_2T/W	
	J46-E	ACP									
$\underline{G}_c$	J27-E	JUNC	J27-F	JUNC	J5-V	NSC	J22-J2	XP	J25-P1	V_2T/W	
	J32-D	AT/WC	J42-e	ND							
A_p	J27-H	JUNC	J27-J	JUNC	J6-N	NSC	J25-U1	V_2T/W	J31-Y	AT/WC	
	J46-k	ACP	J32-B	AT/WC	J17-B	T/WC	J42-S	ND			
N_{31}	J28-j	JUNC	J28-k	JUNC	J11-E	PC	J21-L2	WR	J22-Y1	XP	
	J25-H1	V_2T/W									
L_{u-4}	J27-j	JUNC	J27-k	JUNC	J25-K2	V_2T/W	J26-f1	V_1T/W	J46-d	ACP	

BUSS CIRCUITS (DO NOT GO TO JUNCTION CARD)

LOGIC TERM	TIE POINTS									
B_{1p}	J42-f	ND	J1-b	NSC	J8-D	RC	J11-Z	PC	J14-N	T/WC
	J29-N	AT/WC								
B_{2p}	J42-j	ND	J1-c	NSC	J8-F	RC	J11-Y	PC	J14-T	T/WC
	J29-T	AT/WC								
B_{3p}	J42-k	ND	J1-d	NSC	J8-H	RC	J11-U	PC	J14-U	T/WC
	J29-U	AT/WC								
B_{4p}	J42-n	ND	J1-e	NSC	J8-J	RC	J11-X	PC	J14-M	T/WC
	J29-M	AT/WC								
B_{5p}	J42-p	ND	J2-e	NSC	J8-K	RC	J11-W	PC	J14-K	T/WC
	J29-K	AT/WC								
B_{6p}	J42-r	ND	J2-c	NSC	J8-Y	RC	J11-a	PC	J14-L	T/WC
	J29-L	AT/WC								
B_{7p}	J42-s	ND	J2-b	NSC			J11-V	PC		
$\underline{r}_1$	J42-Z	ND	J6-c	NSC						
r_2	J42-c	ND	J5-h	NSC						
S	J42-V	ND	J4-T	NSC	J5-d	NSC	J8-W	RC	J11-R	PC
	J14-W	T/WC	J17-d	T/WC	J32-d	AT/WC	J29-W	AT/WC		
U	J42-W	ND	J4-c	NSC	J11-M	PC	J17-j	T/WC	J32-j	AT/WC
K_c	J42-T	ND	J6-M	NSC	J31-X	AT/WC	J25-W2	V_2T/W		

NOTES:
1. LAMPS ARE TYPE #1829 EXCEPT READER NEXT CHARACTER LAMPS.
2. READER NEXT CHARACTER LAMPS ARE L570000510.
3. SWITCHES S1 AND S4 ARE 4PDT, LATCHING, NON-SHORTING.
4. SWITCH S2 IS 4PDT, LATCHING, SHORTING.
5. SWITCHES S3, S5, S6, S7 AND S9 ARE 4PDT NON-LATCHING, NON-SHORTING.
6. SWITCHES S8 & S10 ARE 4PDT, NON-LATCHING, SHORTING.

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
1	FOR CHANGES SEE E.O. #54950	9-8-60 20 SEP 60	DN KIRATZIS
2	REVISED PER EO NO. 60373	12-20-60 12-27-60	[illegible] ANG

P-47

S4 LATCHING

S1 LATCHING

S2 LATCHING SHORTING

115V ACC (Nd)

115V ACC LINE

DS1 La

SYSTEM POWER

DS4 Ld

VLC

PARITY MONITOR INHIBIT

S10 NON-LATCHING SHORTING

DS 10 Lj

START COMPUTE

S3 NON-LATCHING

DS-3 Lc

PARITY MONITOR RESET

DS 2 Lb

SINGLE CHARACTER MODE

S7 NON-LATCHING

S6 NON-LATCHING

DS7 Lg

DS6 Lf

INPUT SELECT

DUPLICATION RESET

S8 NON-LATCHING SHORTING

DS 8 Lh

START READ

S5 NON-LATCHING

DS5 Le

MASTER RESET

S9 NON-LATCHING

DS 9 Li

VLC

STOP READ

DS11

READER NEXT CHARACTER LAMPS

P-47

L200007258

ITEM	REQ'D	LIBRASCOPE NO.	DESCRIPTION	MATL.	MATL. SPEC.	UNIT WT.

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DIMENSIONS
FRACTIONAL 3 PLACES ±.010
2 PLACES ±.02 4 PLACES ±.0005
ANGLES ±1° BREAK EDGES .005 MAX.
SURFACE FINISH 125

DO NOT SCALE THIS DRAWING

MATERIAL

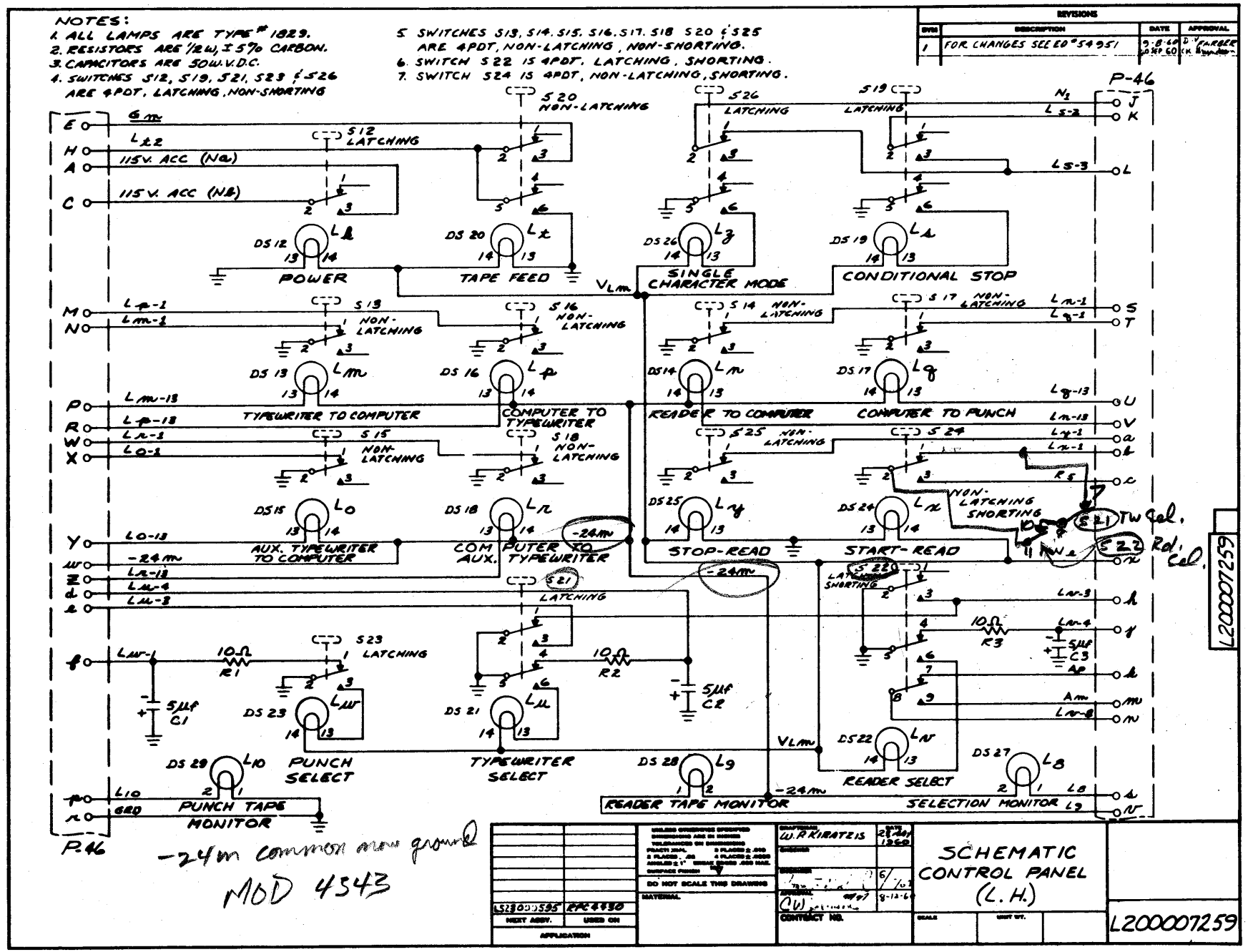
L522000507 | RPC 4430
NEXT ASSY. | USED ON
APPLICATION

DRAFTSMAN W. P. KIRATZIS — DATE 19 MAY 1960
CHECKER
ENGINEER
APPROVAL
CONTRACT NO.

SCHEMATIC CONTROL PANEL (R.H.)

SCALE | UNIT WT.

L200007258


NOTES:
1. ALL LAMPS ARE TYPE # 1829.
2. RESISTORS ARE 1/2 W, ± 5% CARBON.
3. CAPACITORS ARE 50 W.V.D.C.
4. SWITCHES S12, S19, S21, S23 & S26 ARE 4PDT, LATCHING, NON-SHORTING
5. SWITCHES S13, S14, S15, S16, S17, S18 S20 & S25 ARE 4PDT, NON-LATCHING, NON-SHORTING.
6. SWITCH S22 IS 4PDT, LATCHING, SHORTING.
7. SWITCH S24 IS 4PDT, NON-LATCHING, SHORTING.
REVISIONS
DWG | DESCRIPTION | DATE | APPROVAL
1 | FOR CHANGES SEE ECO #54951 | 9-8-60 20 SEP 60 | D. V. FARBER CH.
P-46
S20 NON-LATCHING
S12 LATCHING
S26 LATCHING
S19 LATCHING
115 V. ACC (Na)
115 V. ACC (Nb)
POWER
TAPE FEED
SINGLE CHARACTER MODE
CONDITIONAL STOP
S13 NON-LATCHING
S16 NON-LATCHING
S14 NON-LATCHING
S17 NON-LATCHING
TYPEWRITER TO COMPUTER
COMPUTER TO TYPEWRITER
READER TO COMPUTER
COMPUTER TO PUNCH
S15 NON-LATCHING
S18 NON-LATCHING
S25 NON-LATCHING
S24 NON-LATCHING
AUX. TYPEWRITER TO COMPUTER
COMPUTER TO AUX. TYPEWRITER
STOP-READ
START-READ
NON-LATCHING SHORTING
S21 LATCHING
S22 LATCHING SHORTING
S23 LATCHING
10Ω R1
10Ω R2
10Ω R3
5μf C1
5μf C2
5μf C3
PUNCH SELECT
TYPEWRITER SELECT
READER SELECT
PUNCH TAPE MONITOR
READER TAPE MONITOR
SELECTION MONITOR
-24 m
VLm
GRD
P-46
-24m Common now ground
MOD 4543
DO NOT SCALE THIS DRAWING
MATERIAL
W. P. KIRATZIS
SCHEMATIC CONTROL PANEL (L.H.)
L200007259
L5230005595
EPC 4830

L200 007 251

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
3	REVISED & REDRAWN PER E.O.# 66045	28 JUNE '61	LAL SEARS
4	REVISED PER EO 66070	19 June '61	GE STANLEY

POWER SUPPLY OUTPUT -27c — E — PART OF J48

FROM PUNCH CLUTCH COLLECT. — A — N18

BACK SPACE RELAY DRIVE — N — N6 — PART OF J49

TAPE BACKSPACE RELAY (D.C.) K1

GROUND — K, H

POWER SUPPLY OUTPUTS -24c J, +24c F — PART OF J48

R1 20 OHM, 10W

R2 20 OHM, 10W

C3 .47 mf 400 V.DC. — R5 100 OHM 1/2 W

DEVICE POWER RELAY (A.C.) K2

C2 .47 mf 400 VDC — R4 100 OHM, 1/2 W

TO DEVICE POWER SW-2 — P — Nb

115 V. ACC FROM LINE — C

115 V. AC. FROM LINE — A

TO SYSTEM POWER SW-2 — E — Nd — PART OF J49

F1-8A

F2-8A

C4 .47 mf 400 VDC — R6 100 OHM 1/2 W

SYSTEM POWER RELAY (A.C.) K3

R3 100 OHM 1/2 W

C1 .47 mf 400 V.DC.

PART OF J49

PART OF J48 — B, A — Na — ACC 115 V. A.C. — POWER SUPPLY INPUT

Ng

d, c, b	-27 m
Nz	TO FWD. TAPE FEED SOLENOID (PUNCH)
N4	TO INDEX PUNCH SOLENOID
N5	TO REVERSE TAPE FEED SOLENOID
F, D	GROUND
j	+24 c
a, Z	-24 c
Nc	-Vlc
Ne	-Vlm
Y, X, W, V, U	-24 m
h, f, e	+24 m
Nf	
T, X, S, R	115 V. AC.
H	ACC (115V) TO SYSTEM PWR. SWITCH 3
w, N, L, K, J	TO DEVICE POWER SWITCH 3 — 115 V. ACC

1. FOR WIRE RUNNING LIST SEE L541 000 587.

NOTES:

L5733	NEXT ASSY.
NEXT ASSY.	USED ON
APPLICATION	
DRAFTSMAN	
CHECKER	
ENGINEER	
APPROVAL	
CONTRACT NO.	

SCHEMATIC POWER-CONTROL CHASSIS

L200 007 251

SCALE — WT — SHEET OF

A-5-45