70|45 PROCESSOR OPERATING MANUAL

SPECTRA 70

RADIO CORPORATION OF AMERICA • ELECTRONIC DATA PROCESSING

RCA

PROCESSOR

70|45

OPERATING MANUAL

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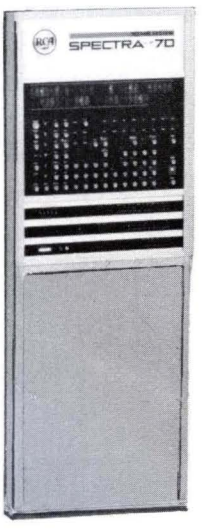


70/45 MAINTENANCE
CONSOLE PANEL

70/97 CONSOLE

Frontispiece — Model 70/45 Processor and Model 70/97 Operator's Console

DESCRIPTION

GENERAL

◆ The RCA Model 70/45 Processor is a solid state, general purpose, digital processor. It is the main element of a system handling medium-large data processing applications. Because of its storage capacity, and data transmission and computation rates, this processor is applicable to both data processing and scientific-problem solving. The internal logic is controlled by Elementary Operation (EO's) stored in a read-only control memory.

The 70/45 Processor may be any one of the model numbers listed in Table 1. The memory size (capacity in bytes) and number of racks required to accommodate these sizes are also given in this table. The method of operation is the same for the different models and is described in the Operation portion of this manual.

The 70/45 is a variable-format processor, consisting of a Main Memory, Read-Only Memory, Non-addressable Memory, Fast Memory, Program Control, and Input/Output Control.

Table 1. Spectra 70/45 Model Numbers

Model Number	Capacity (in bytes)	Rack Number Identification	Remarks
70/45 C	16,384	20 and 21	Rack numbers and their design functions: 20 = Power Supply 21 = Basic Processor Unit 22 = Memory Addition 23 = Memory Addition
70/45 D	32,768	20 and 21	
70/45 E	65,536	20 and 21	
70/45 F	131,072	20, 21, and 22	
70/45 G	262,144	20, 21, 22, and 23	

FUNCTIONAL

Processor States

◆ The RCA 70/45 Processor has four processor states that provide control of system and program interrupts. Programs may be executed in any one of these states, because each state is completely independent and has its own set of registers (except floating point register). The four processor states and their functions are as follows:

1. *Processor State* P_1 — normally interprets and executes the user's program. The processing state is the problem-oriented state.
2. *Processor State* P_2 — performs specific program tasks as dictated by the Interrupt Control State P_3.
3. *Processor State* P_3 — is automatically entered when an interrupt is recognized other than one caused by a machine check or power failure.
4. *Processor State* P_4 — is entered whenever a machine check or power failure occurs.

Upon detection of interrupt the hardware initiates Processor State 3 or 4. It is the programs responsibility to determine what action is to be taken in any processor state.

Organization of Data

◆ The following definitions describe the various levels of data organization for the 70/45 Processor:

Bit — A bit is a single binary digit having the value of either zero or one.

Byte — A byte consists of eight information bits.

Halfword — A halfword consists of two consecutive bytes beginning on a main memory location that is a multiple of two.

Word — A word consists of four consecutive bytes beginning on a main memory location that is a multiple of four.

Doubleword — A doubleword consists of eight consecutive bytes beginning on a main memory location that is a multiple of eight.

Data Formats

◆ The basic unit of information in the 70/45 Processor is a byte, which is the smallest addressable unit.

The internal code representation in the 70/45 is either the Extended Binary-Coded-Decimal Interchange Code (EBCDIC) or the American Standard Code for Information Interchange (ASCII) as specified by program. (See Appendices A, B, C, and D.)

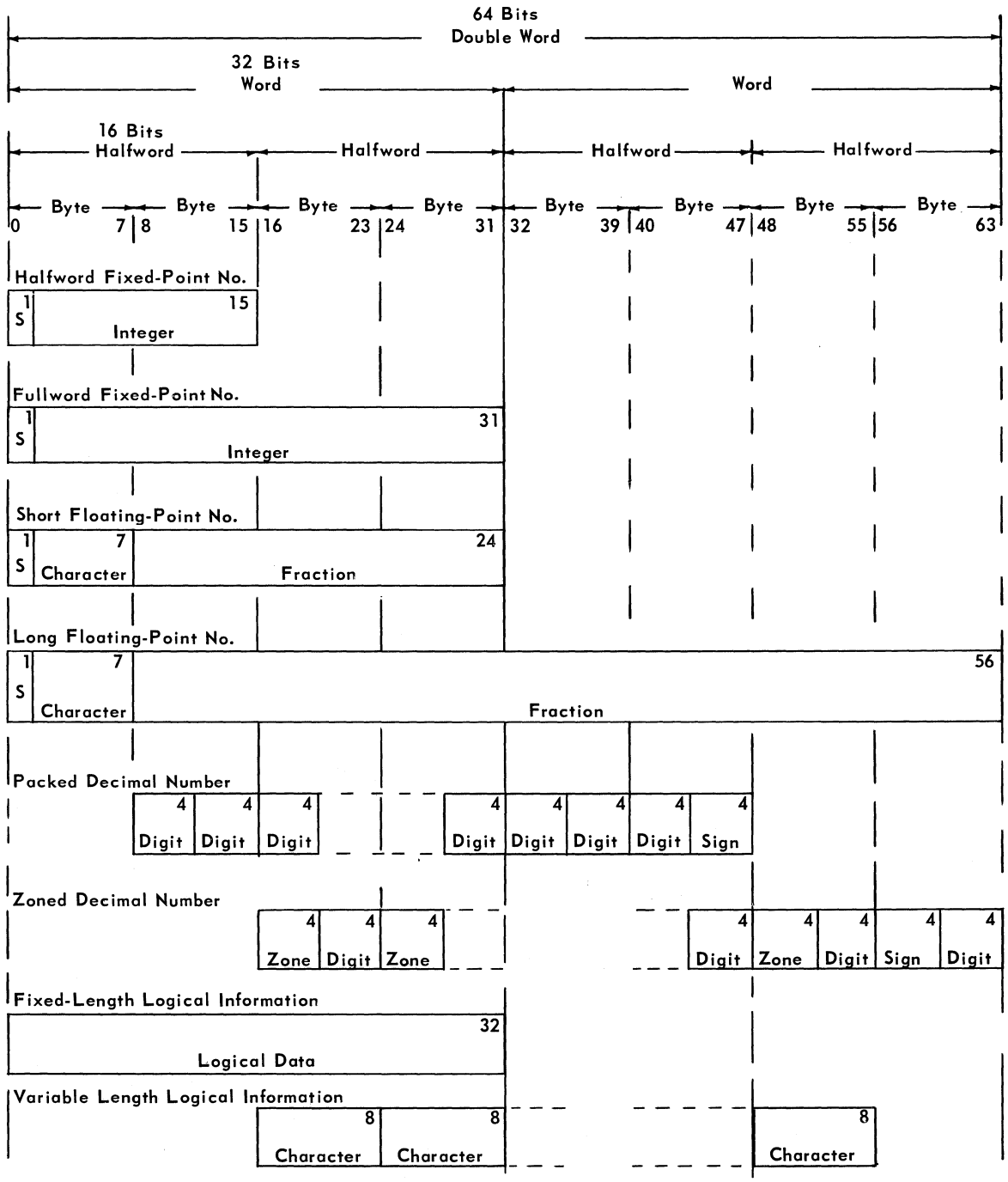
There are eight distinct formats for data in main memory as shown in Figure 1.

Numbering Systems

◆ The hexadecimal numbering system is used to represent characters and addresses in the 70/45 Processor. The hexadecimal system has a base of 16. The first ten marks are represented by decimal numbers zero (0) through nine (9); marks eleven through fifteen are represented by the letters A through F. Table 2 illustrates the decimal, binary, and hexadecimal representations of numbers zero through fifteen.

Table 2. Basic Hexadecimal Marking System

Hexadecimal (Base 16)	Binary (Base 2)	Decimal (Base 10)
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
A	1010	10
B	1011	11
C	1100	12
D	1101	13
E	1110	14
F	1111	15



NOTE: Numbers in upper right corners of blocks indicate number of bits used.

Figure 1. Data Formats

Instructions

◆ There are five basic instruction formats which express, in general terms, the operations to be performed. These instructions are:

1. RR = register——register operation.
2. RX = register——indexed storage operation.
3. RS = register——storage operation.
4. SI = storage——immediate operand operation.
5. SS = storage——storage operation.

The detailed format of each instruction is shown in Figure 2, and the instruction sub-fields are defined as follows:

R_1, R_2, R_3 = 4 bit operand register specification
X_2 = 4 bit index register specification
B_1, B_2 = 4 bit base register specification
D_1, D_2 = 12 bit displacement
I_2 = 8 bit immediate operand
L_1, L_2 = 4 bit operand length specification
L = 8 bit operand length specification

Addressing Main Memory

◆ The effective storage address is computed from the following binary components:

1. Base (contents of the designated base register, B_1 or B_2)
2. Displacement (D_1, D_2)
3. Index (contents of the designated index register, X_2) for RX instructions.

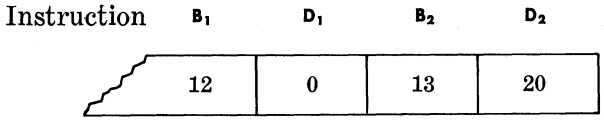
In computing the address, the base and index are treated as unsigned 18-bit positive binary integers in bits 14-31 of the designated register. The displacement is treated as a 12-bit positive binary integer. The effective address is computed by adding the components as binary numbers, ignoring overflow.

Note: If register 0 is specified as the base register and/or the index register, then a zero quantity is to be added, *regardless* of the contents of register 0.

The following examples use decimal addresses for convenience:

EXAMPLE 1

Assume Reg. 12 2000
Reg. 13 0480



The effective address of B_1, D_1 is 2000

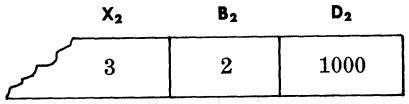
The effective address of B_2, D_2 is 0500

Addressing Main Memory (Cont'd)

EXAMPLE 2

Assume Reg. 3 30010
Reg. 2 00200

Instruction



The effective address of X_2, B_2 and D_2 is

$$30010 + 00200 + 1000 = 31210$$

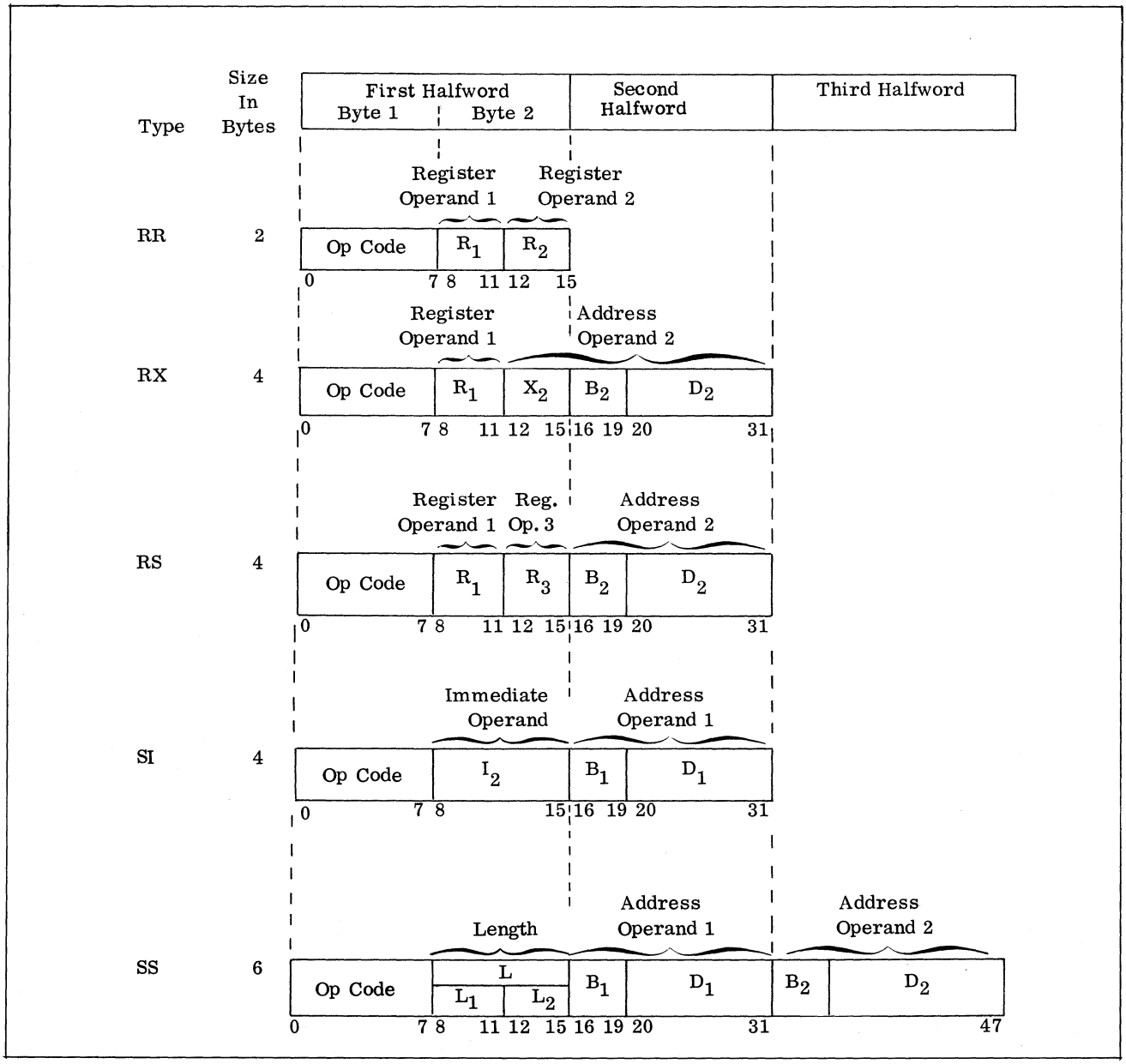
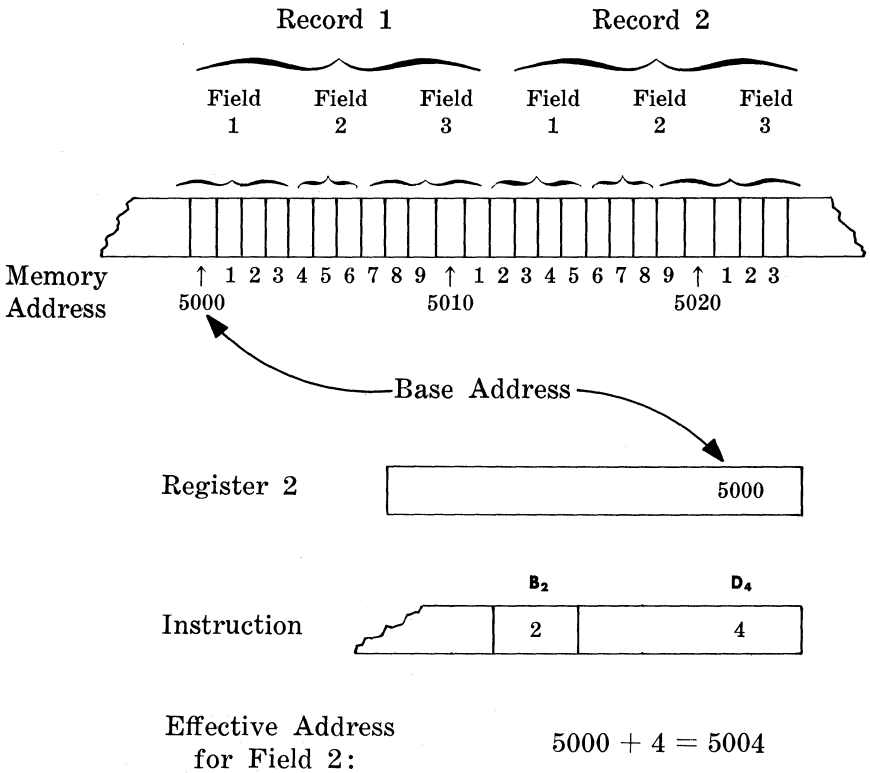


Figure 2. 70/45 Instruction Formats

Addressing Main Memory (Cont'd)

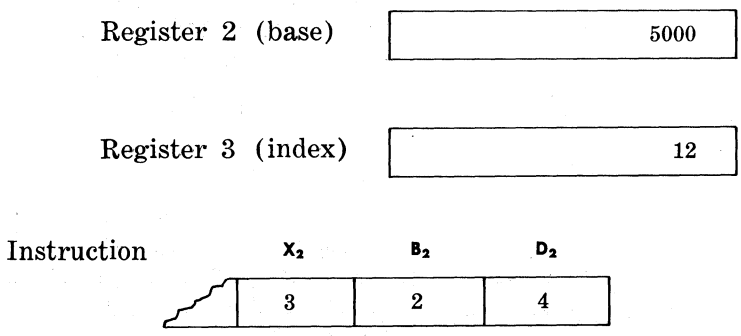
EXAMPLE 3



Effective Address for Field 2: $5000 + 4 = 5004$

To process Record 2, the contents of Register 2 are increased by 12, the size of Record 1. The instruction field in (example 3) would then refer to Field 2 of Record 2.

If the instruction is an index-type instruction, a second general-purpose register, called an index register, is also used to generate the address. In example 3, the index register (Register 3) would initially be cleared to zero. After the first record is processed, the contents of Register 3 are increased by the record size. Then the instructions using Registers 2 and 3 for addressing would refer to Record 2. An illustration of this follows:



Effective Address for Field 2,

Record 2: $5000 + 12 + 4 = 5016$

Input/Output Channels

◆ The Model 70/45 Processor has two types of input/output channels, selector channels and a multiplexor channel.

Selector Channels — Up to three selector channels (optional) can be attached to a Model 70/45 Processor. Each selector channel can address up to 256 peripheral devices.

Each selector channel has two standard interface trunks and each standard interface trunk can be connected to the control electronics of an input/output device. A device control electronics controls one device (i.e., Card Reader, Printer), or a number of devices (i.e., Tape Controller: up to 16 Tape Stations).

Only one device can operate on a selector channel at one time. However, all selector channels can operate simultaneously with, and independently of, normal processor operation.

Multiplexor Channel — The multiplexor channel is standard on the Model 70/45 Processors, and can address up to 256 devices.

The multiplexor channel has eight standard interface trunks, each of which can be connected to a device control electronics. This permits the multiplexor channel to operate devices on all eight trunks simultaneously. The limit as to the number of input/output devices that can be connected is determined by the device control electronics. A ninth trunk is provided on the multiplexor channel for exclusive use by the Model 70/97 Console.

Figure 3 depicts the logical connection of the I/O channels and I/O devices.

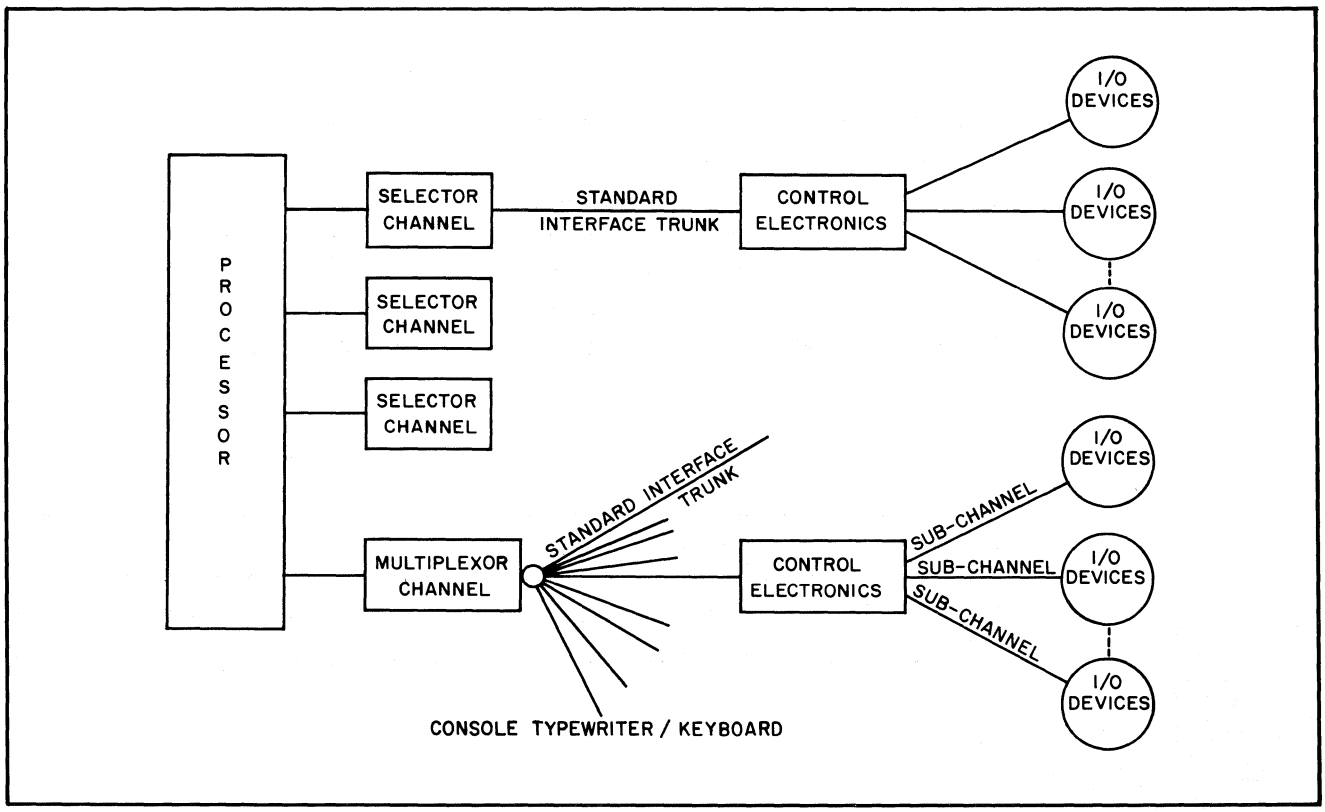


Figure 3. 70/45 Input/Output Flow

SUB-UNITS

Basic Processing Unit

◆ The Basic Processing Unit (BPU) (See Figures 4 and 5), in response to an internally stored program, can effect internal data transmission, perform arithmetic operations, execute decisions and control instructions, and perform branching operations. In addition, the BPU can operate peripheral devices in either an input or an output mode.

Main Memory

◆ The Main Memory consists of expandable magnetic core storage and is available in the expandable sizes as indicated in Table 1. Memory-cycle time is 1.44 microseconds. This is the time to transfer two bytes from the main memory to the memory register and to regenerate the bytes in storage. The processor normally operates on two 8-bit bytes at a time, although the minimum addressable data unit is one byte.

Non-Addressable Memory

◆ This memory is a portion of the main memory that cannot be addressed by program. A set of registers that services the devices attached to a multiplexor channel is contained in the non-addressable main memory. The size of this memory will vary in accordance with the capacity of the main memory selected. Non-addressable memory is in addition to the main memory capacity of the system.

Fast Memory

◆ The fast memory is a micromagnetic storage device consisting of 128 four-byte words, the cycle time of which is 300 nanoseconds. Each word in a fast memory is uniquely addressed.

The following registers are contained in the fast memory of a 70/45 Processor.

1. *Processor Utility Registers* — All locations designated as processor utility registers are used by the processor for program control and cannot be used by the program.

2. *General Registers* — These locations are the general registers for each processor state. These registers are used by the program for base addressing, for indexing, or for storing operands.

3. *Interrupt Mask Registers* — An Interrupt Mask register for each processor state permits or inhibits 32 interrupt conditions.

	P_1	P_2	P_3	P_4	
Interrupt Mask	40	44	50	14	See Interrupt Flags

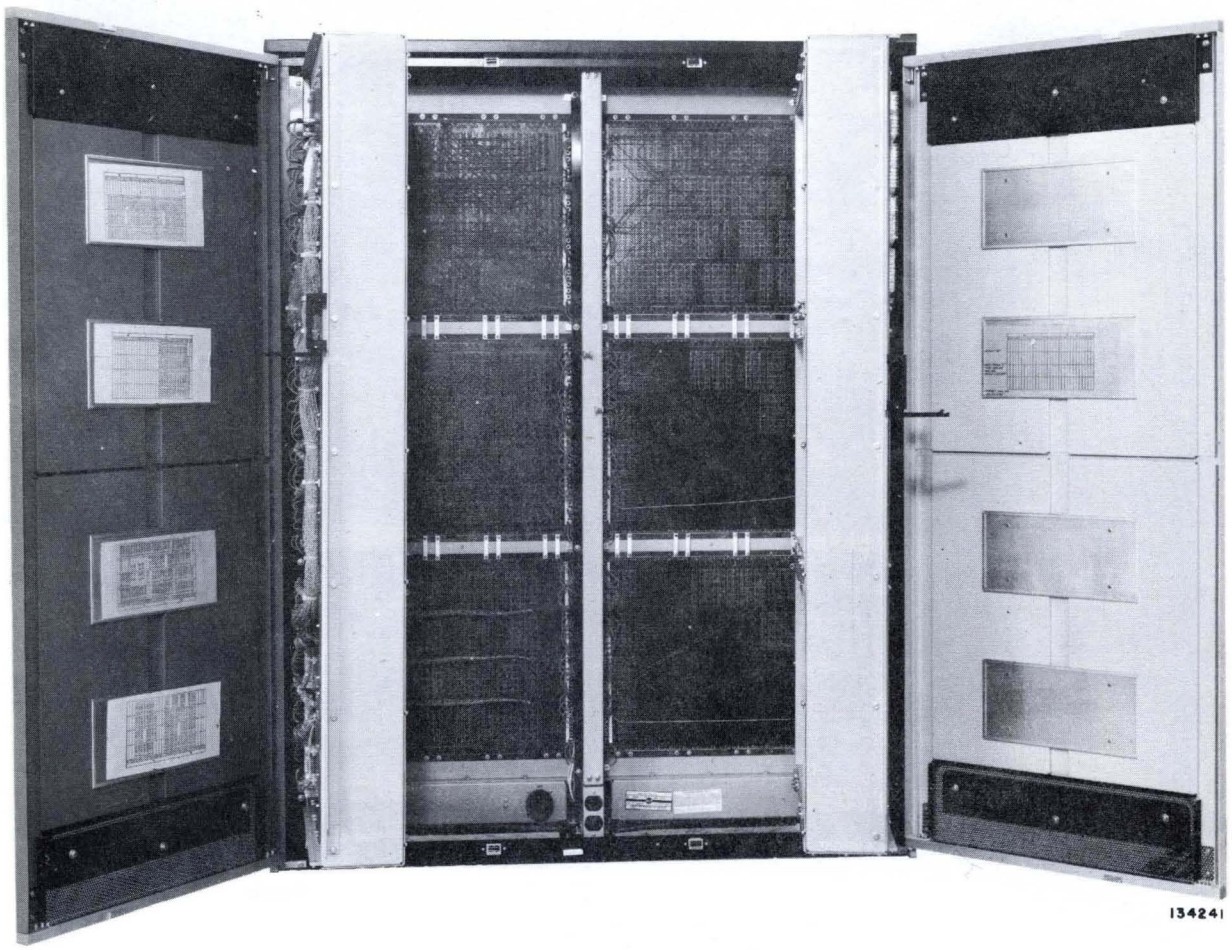


Figure 4. Interior Model 70/45 Processor (Rear View Showing Frame Opened)

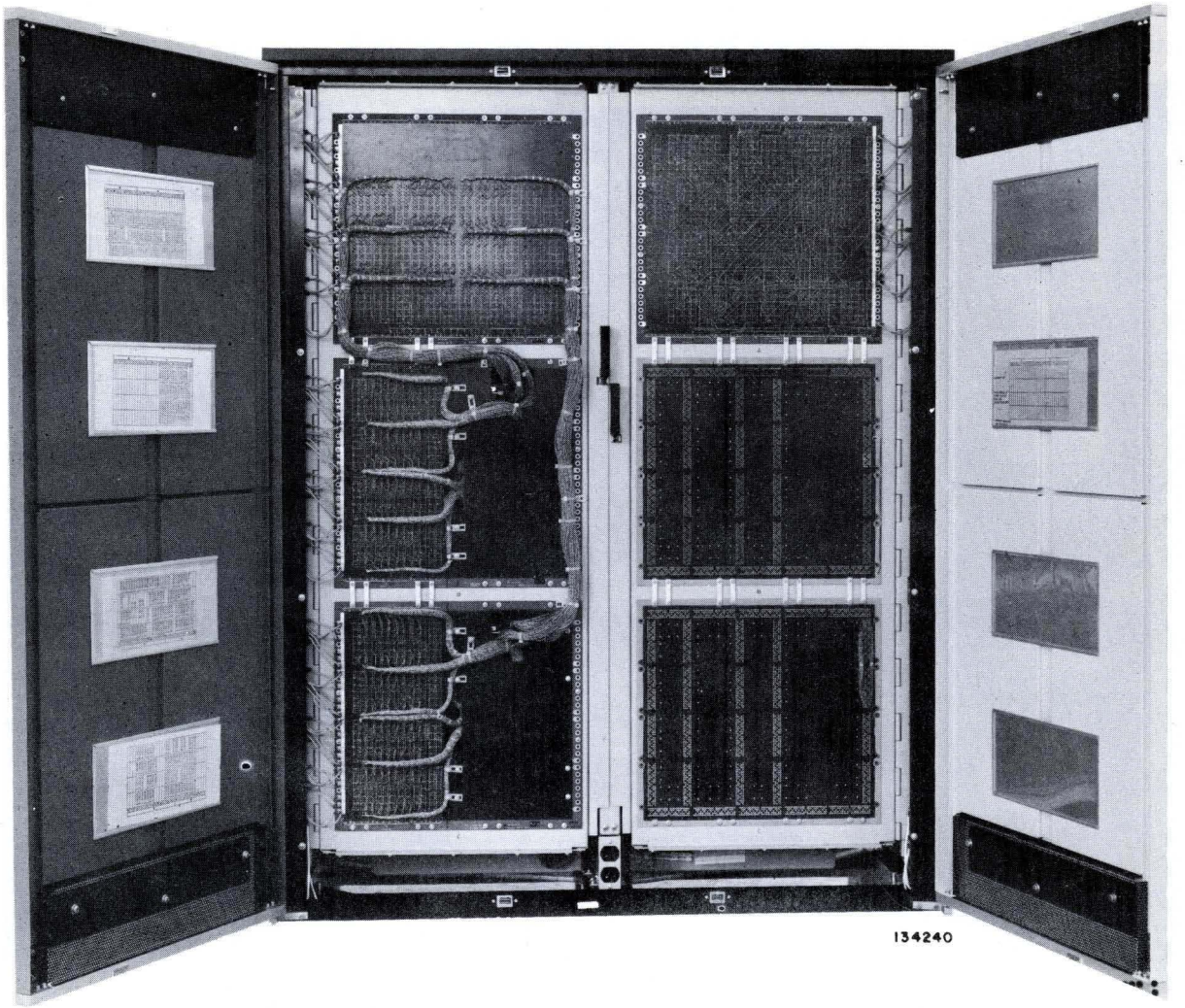


Figure 5. Interior Model 70/45 Processor (Rear View Showing Frame Closed)

Fast Memory (Cont'd)

4. *Interrupt Status Registers* — An Interrupt Status register for each processor state stores interrupt identification information and operational control information. This register contains indications of the last state interrupted, the protection key, the decimal mode (ASCII or EBCDIC), the privileged mode bit and the supervisor call identification.

	P_1	P_2	P_3	P_4	DR0		DR1		DR2		DR3	
Interrupt Status Register	41	45	51	15	ISI	0	KEY	A	0	0	CALL	
					ISI	0	KEY	0	0	0		
					ISI	0	KEY	0	0	0		
					0	0	KEY	N	0	0		

5. *Program Counter* — A Program Counter for each processor state contains the main memory address of the next instruction to be executed, the condition code and the instruction length code of the last instruction in which an interrupt occurred, and the program mask.

	P_1	P_2	P_3	P_4	DR0		DR1	DR2	DR3
P — Register	42	46	52	16	ILC	Sig Err	PROGRAM COUNTER		
					ILC	Exp Und			
					CC	Dec Ov			
					CC	FP Ov			

6. *Input/Output Channel Registers* — A set of four registers for each selector channel controls input/output operation. A set of four registers for the multiplexor channel controls initiation and termination of input/output operations on the multiplexor channel.

Fast Memory (Cont'd)

7. *Floating-Point Registers* — Four floating-point registers (each is two words long) are used in floating-point arithmetic.

	MUX	SEL1	SEL2	SEL3	I/O Channel Registers
Assembly and Status	25	35	65	75	DR0, DR1, DR2 } Assy DR3: Man. Req. / Int. Pend. / Dev. Busy / Cont. Busy SDB: Dev. End / Sec. Ind. / Dev. Inop. / Stat. Mod.
CCR 1	24	34	64	74	DR0: 0 / 0 / 0 / 0 (Command Code) DR1, DR2, DR3: Data Address of first byte or location of new CCW if command is a transfer in channel.
CCR 2	23	33	63	73	DR0: CD / CC / SLI / SKIP; PCI / 0 / 0 / 0 DR1: PCI / IL / Prog. Chk. / Prot. Chk. DR2: Ch. Data / Ch. Contr'l / TIP / TI DR3: Byte Count
C A R	22	32	62	72	DR0: Device Number DR1, DR2, DR3: Address of next CCW

Fast Memory (Cont'd)

8. *Interrupt Flag Register* — One interrupt Flag register is provided. When an interrupt condition occurs, a bit associated with this condition is set in the Interrupt Flag register.

Interrupt Flags (43)	DR0		DR1		DR2		DR3	
	Test Mode 7C	Sig. Err. 6C	Add. Err. 5C	Not Spec. 4C	MUX 3C	SEL. #3 2C	EXT. #6 1C	EXT. #2 C
	F.P. Ov. 78	Div. Err. 68	Op. Trap 58	Not Spec. 48	SEL. #6 32	SEL. #2 28	EXT. #5 18	EXT. #1 8
	Dec. Ov. 74	Exp. Ov. 64	Priv. Op. 54	Cons. Int. 44	SEL. #5 34	SEL. #1 24	SEL. #4 14	Mach. Check 4
	Exp. Under 70	Data Err. 60	Sup. Call 50	ETC 40	SEL. #4 30	Not Spec. 20	EXT. #3 10	Power Fail. 0

Read-Only Memory

◆ Read-Only Memory (ROM) is an integral part of the 70/45 Processor. The standard 70/45 ROM consists of two banks of 1,024 54-bit words each. Each word contains one microinstruction of 53-bit length. In addition, the 70/45 ROM contains a 12-bit address register.

The wired-in microprogram logic contained in the read-only memory banks control the elementary operations of the 70/45. The cycle time of one ROM bank is 960 nanoseconds. The effective cycle time of both ROM banks operating alternately is 480 nanoseconds with a 54-bit access.

The 70/45 Processor is obtainable with two additional ROM banks containing the microinstructions for any combination of the available Emulator features. (Refer to Optional Features.)

Program Control and Arithmetic Unit

◆ The program control and arithmetic unit in the Model 70/45 Processors interprets and executes the instructions stored in main memory. Registers and indicators monitor the sequence of operations, perform automatic accuracy checks, and communicate with the RCA standard interface in the control of input/output devices.

Operator's Console

◆ The Model 70/97 Operator's Console is a free standing, self-contained unit which consists of two portions: the Console Typewriter and the Operator's Console/Display Panel, mounted together on a Console table. (See Figure 6.) The console panel provides the controls and indicators to enable system operation in conjunction with operating system programs. The operator has complete control of the system and communicates with the system via a set of control switches and the console typewriter.

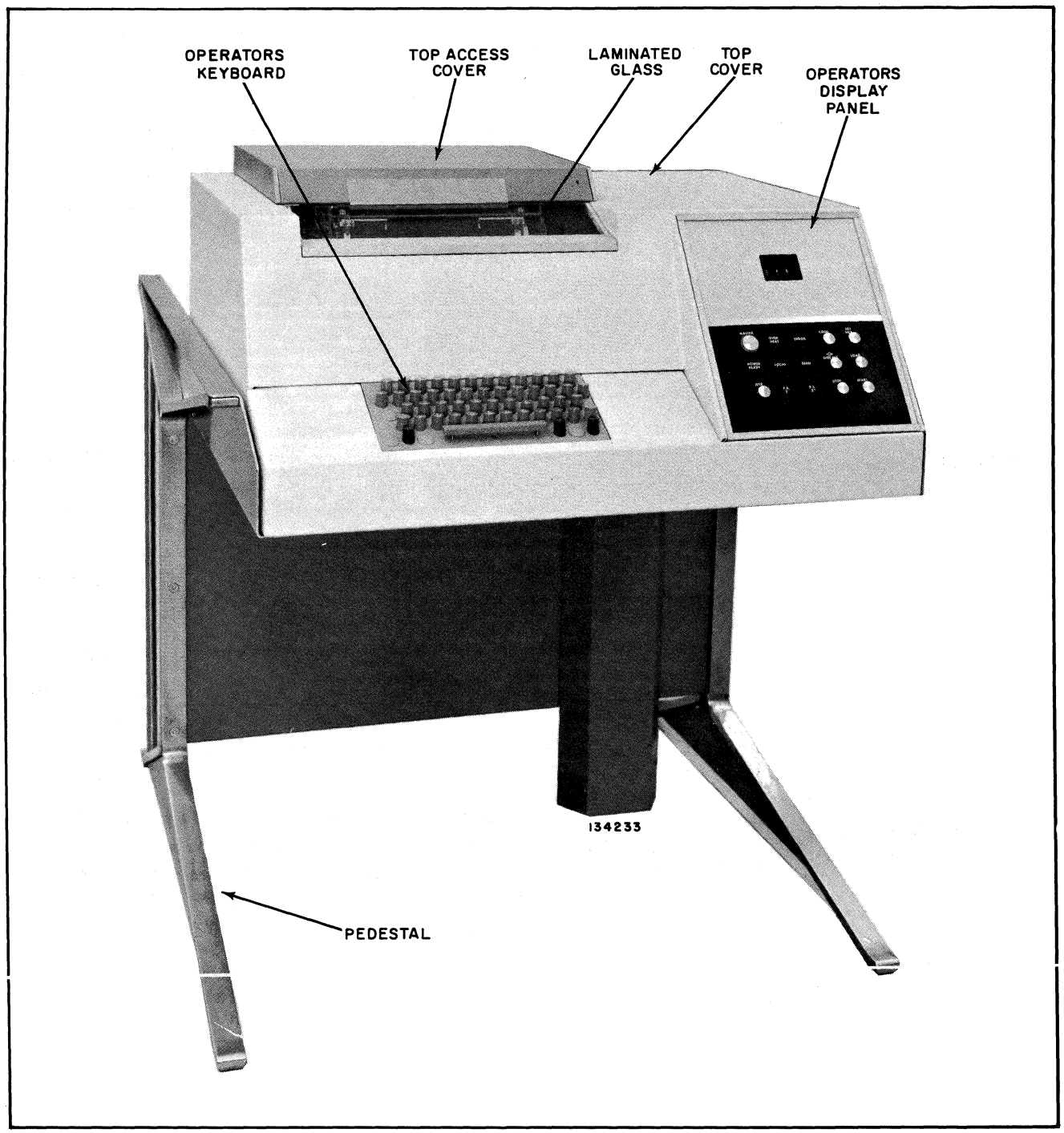


Figure 6. Operator's Console (Model 70/97)

Maintenance Console Panel

◆ The Maintenance Console for the 70/45 Processor consists of two panels: the Maintenance Panel and the Auxiliary Maintenance Panel. These two panels are physically mounted on the power supply rack and incorporate controls and indicators to enable system operation without the assistance of operating system programs for maintenance purposes. Refer to Tables 4 and 5 for description and functions of the indicators and controls of these panels. (See Figure 7.)

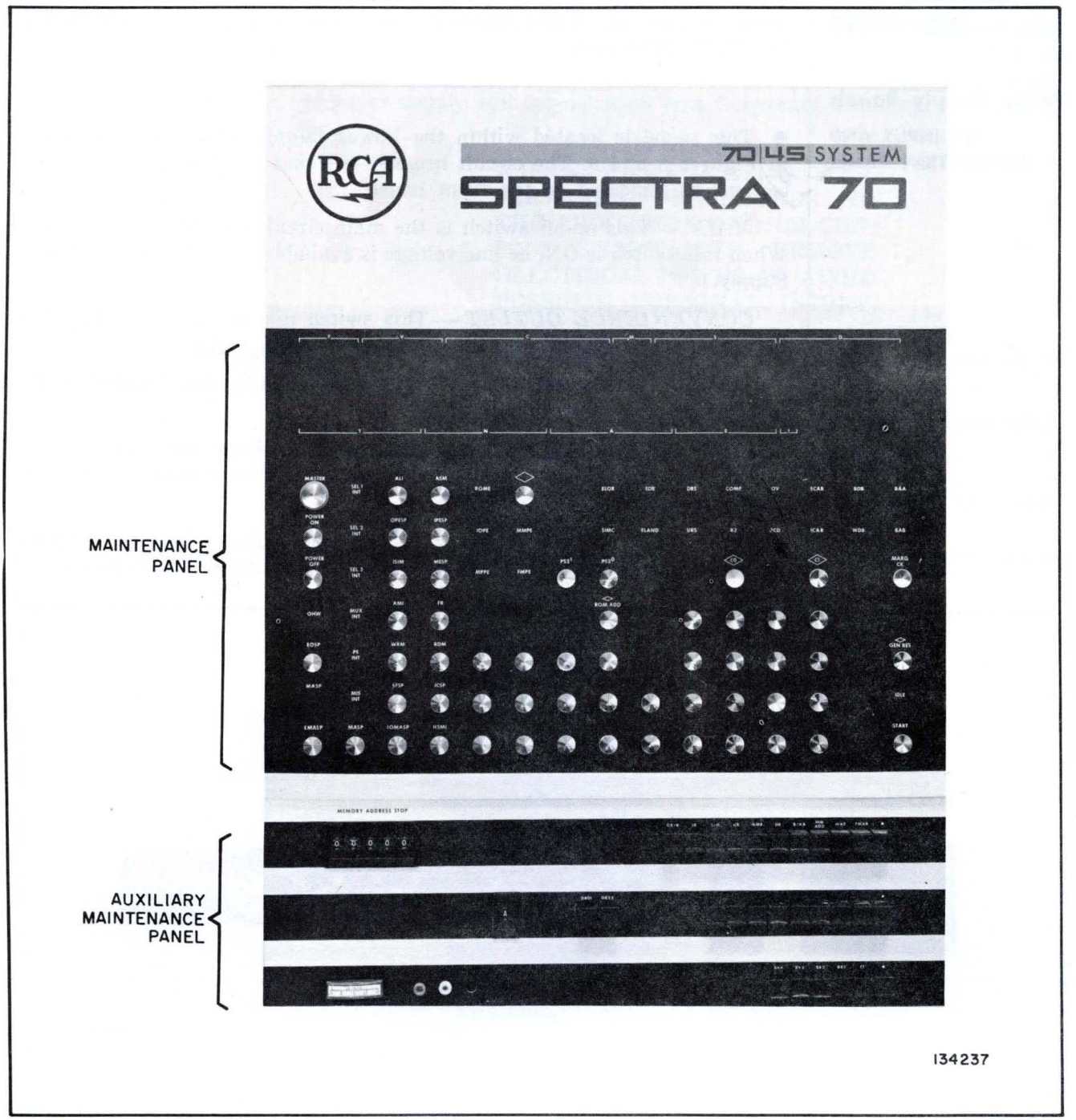


Figure 7. Model 70/45 Maintenance Console Panel (Showing Maintenance and Auxiliary Panels)

Power Supply

◆ The 70/45 Processor Power Supply furnishes power to the Basic Processing Unit and to the High-Speed Memory in addition to the Operator's Console. Contained within the Power Supply rack are the Typing Control and Power Supply electronics. Refer below for description and functions of the Controls and Indicators provided on the Power Supply Control Panel and the AC Input and Distribution Panel.

CONTROLS AND INDICATORS

◆ The following describes the operational functions of the circuit breakers, pushbutton and indicators that comprise operator's controls for the 70/45 Processor.

Power Supply Panels

AC INPUT AND DISTRIBUTION PANEL

◆ This panel is located within the Power Supply cabinet and is shown in Figures 8 and 9. The circuit breaker switches provide AC power protections as indicated on the front panel.

MAIN — This on-off switch is the main circuit breaker for ac power. When this switch is ON, ac line voltage is available to the Processor Power Supply.

CONVENIENCE OUTLET — This switch provides ac line voltage to the convenience outlets located in the power supply racks.

FANS — This switch provides ac line voltage to the fans located within the various processor racks.

CONTROLS — This switch provides ac line voltage protections to the thermostat warning signal controls located in the Power Supply and Basic Processor Unit racks.

−5; +30/+20/+10; +50/+5/−30 — These circuit breakers protect the individual power supply voltages as supplied throughout the processor.

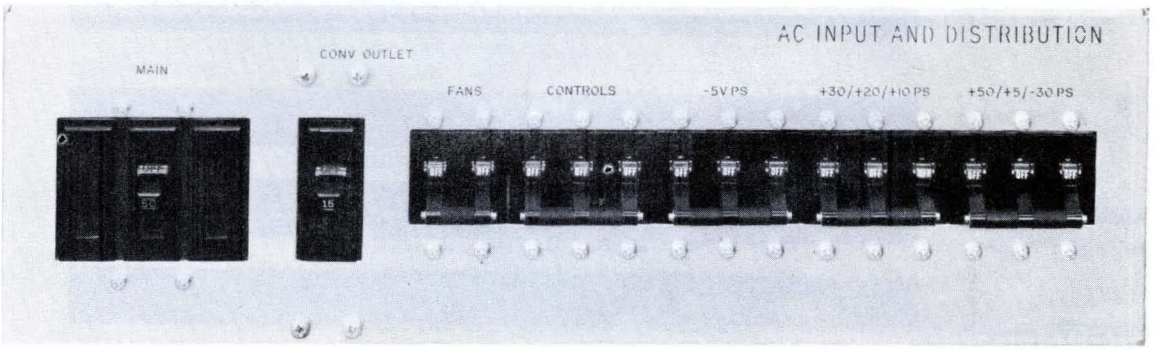


Figure 8. AC Input and Distribution Panel

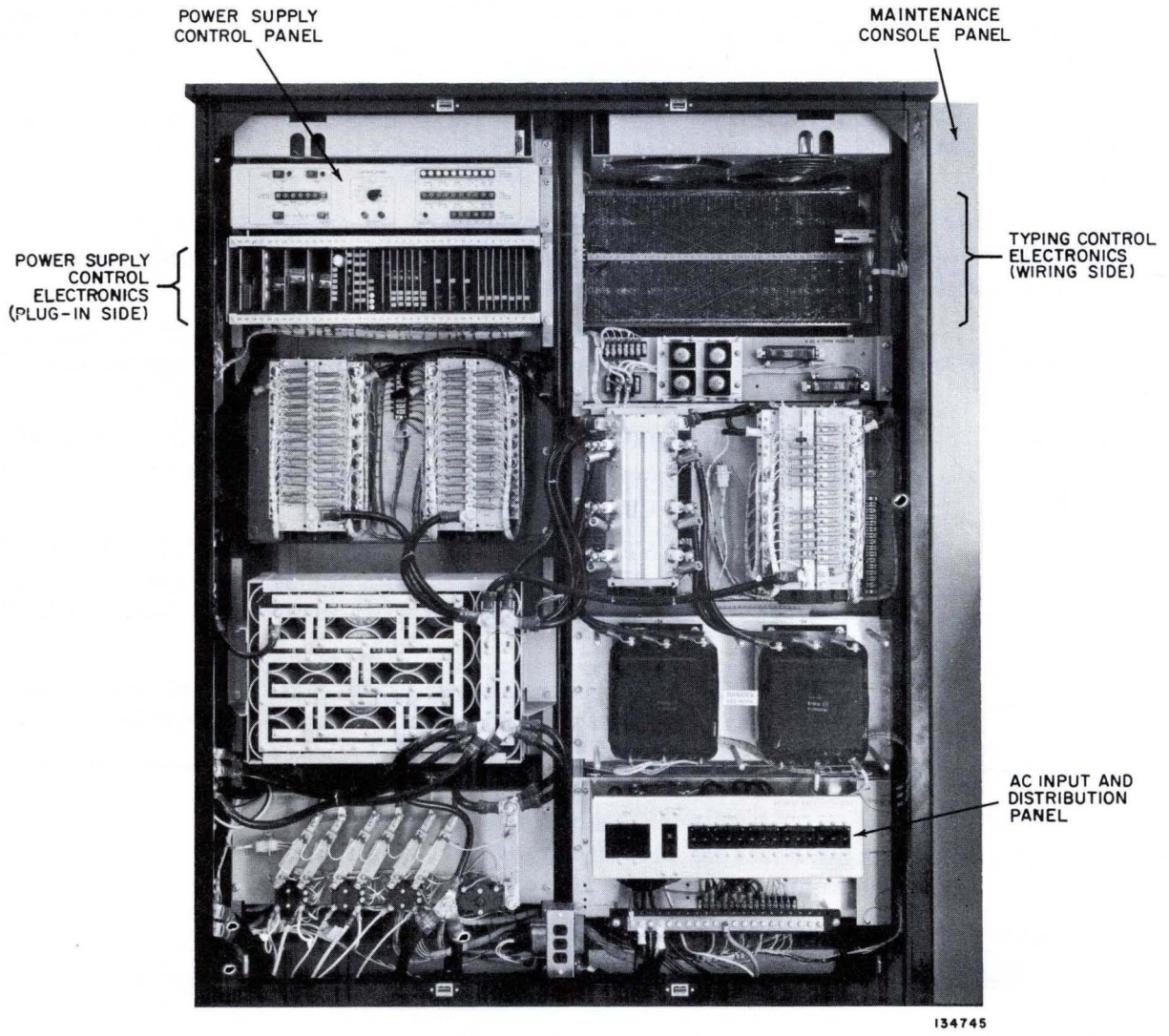


Figure 9. Power Supply and Control Electronics Rack (Rear View)

POWER SUPPLY CONTROL PANEL

◆ This panel is located within the Power Supply rack as shown in Figures 9 and 10. Essentially this panel is utilized for maintenance purposes. However, the functions of the controls and indicators pertaining to this panel are described herein, as an aid to the operating personnel.

TEST — This switch is used to turn on the DC power in the test mode. The DC power is isolated from the logic rack(s). Pressing the pushbutton will light its associated indicator.

RESET — Pressing this pushbutton will reset all of the power supply sensing functions. The indicator is lit after a fault is detected and will go off after the POWER SUPPLY is reset.

CURRENT OVERLOAD — These indicators will light whenever a specific current overload (as noted on the panel) is detected in the power supply input.

VOLTAGE OUT OF TOL — When the OPERATE and/or TURN ON indicators are displayed, the indication is that the protection circuits have detected a voltage error.

VOLTMETER — This nine position rotary switch and its associated test jacks, are used for monitoring the output voltage as determined by the positioning of the switch.

TEMP. WARNING IN FRAME — When indicator is lit, a temperature sensor is approaching the maximum safe limits. The location of the sensor is as identified by the markings on the panel.

TEMP. OVERHEAT IN FRAME AND TEMP. OVERHEAT IN COOLER — The indicator associated with the sensor when lit, indicates an overheating condition. The location of the sensor is as identified by the markings on the panel.

LAMP TEST — Pressing this button will cause all Control Panel lamps to light, thus enabling the identification of any defective bulb.

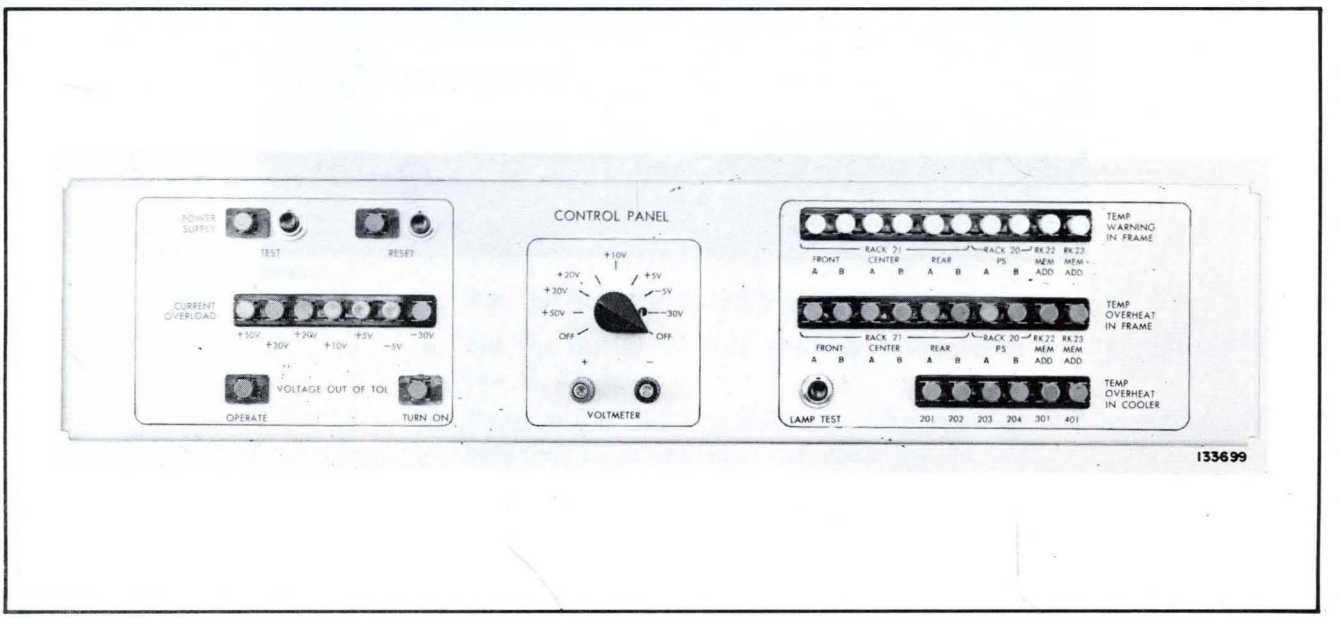


Figure 10. Power Supply Control Panel

Operator's Console Display Panel

◆ By means of the three Digi-Switches and pushbuttons, an operator can perform an initial program load function from any input device; start and stop the computer; or interrupt the program in order to initiate communication with the software via the typewriter. The following listing describes the type and use of the various switches and indicators that comprise the Operator's Display Panel. (See Figure 11 and Table 3.)

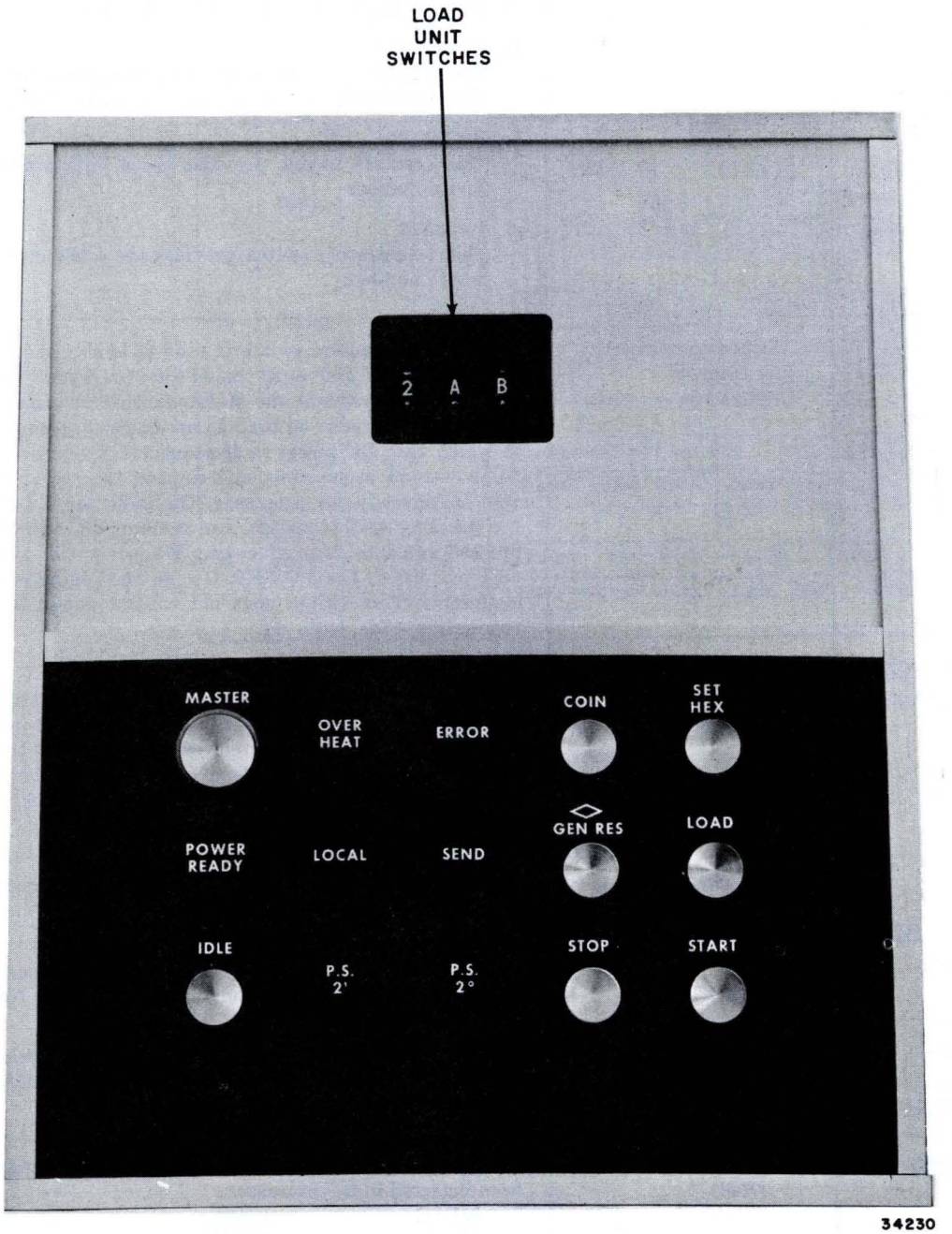


Figure 11. Model 70/97 Operator's Console Display Panel

Table 3. Operator's Console Panel (Indicators and Controls)

(Reference Fig. 11)

Panel Designation	Type	Description and Function
Load Unit Switches (No markings on panel)	Digi-Switches	The three digi-switches provide for the entry of the I/O channel and device number for initial program load function and are used in conjunction with the LOAD switch. All three switches have sixteen positions labeled 0 through 9 and A through F. Each switch is used as follows: a. *Switch 1* This (leftmost) switch provides the three bit channel address of which only positions 0 through 7 are used. b. *Switch 2* This (center) switch provides the 4 high order bits of the device number. c. *Switch 3* This (rightmost) switch provides the 4 low order bits of the device number.
MASTER	Pushbutton Switch/ Indicator (Green)	This alternate action switch is used to enable the power supply control circuits and must be in the ON condition before the POWER ON switch at the Maintenance Panel can be activated. This switch can also be used as an emergency power off switch, in which case DC power is disconnected, by-passing the normal DC power off sequencing, and causing the power failure interrupt to be set in the processor. The indicator is turned on upon the pressing of this switch, and remains on, until the switch is pressed again to turn off power. Whenever this switch is in its OFF condition, the POWER ON on the Maintenance Panel is ineffective. This switch does not control power to the console typewriter (See Note 1).
POWER READY	Indicator (Green)	This indicator is turned on to indicate that the processor DC power is on and that the processor is ready for operation. This occurs when the processor power sequencing is completed and remains on until power is removed from the processor, either at the completion of power off sequencing, or emergency power off procedures.
IDLE	Indicator (Yellow/Red Border)	This indicator is turned on when the Idle instruction is operating. (See Note 2.)
OVER HEAT	Indicator (Red)	This indicator is turned on whenever the temperature in the processor exceeds its environmental design. (See Note 2.)
LOCAL	Indicator (Yellow)	This indicator is turned on whenever the Console typewriter LOCAL-OFF-LINE switch is positioned to LOCAL, or when DC power is off in the processor.
ERROR	Indicator (Red)	This indicator is turned on whenever the following errors have been detected in the processor: MPPE IOPE MMPE ROME FMPE PEINT (During load operation) The particular error which has been detected can be determined from the specific indicators on the Maintenance Panel.

Table 3. Operator's Console Panel (Indicators and Controls) (Cont'd)

(Reference Fig. 11)

Panel Designation	Type	Description and Function
SEND	Indicator (Yellow/Red Border)	When lit, indicates that the Processor is ready to receive input from the Console typewriter. The indicator is turned on whenever a read typewriter operation is initiated. The indicator is turned off when either the EOT key or the Error key on the keyboard is activated.
P. S. 2^1 P. S. 2^0	Indicators (Yellow)	Displays the current program state when the processor is halted as follows: P.S. 2^1 / P.S. 2^0 / Program State 0 / 0 / 4 0 / 1 / 3 1 / 0 / 2 1 / 1 / 1 (See Note 3)
COIN (Console Interrupt Switch)	Pushbutton Switch	When this momentary contact switch is set, the Console Interrupt Flag is set in the Processor, thus notifying the Operating System software of console operator intervention via the Console Typewriter.
◇ GEN RES	Pushbutton Switch	Pressing this momentary contact switch will reset the system conditions to a state which permits orderly start-up. (See Note 3.)
STOP	Pushbutton Switch/ Indicator (Yellow)	Pressing this momentary contact switch causes the processor to halt after completion of the current instruction being performed and any I/O operation currently in progress.
SET HEX	Pushbutton Switch/ Indicator (Green)	This alternate action switch when activated will set the Console typewriter electronics to operate in Hexadecimal mode.
LOAD	Pushbutton Switch/ Indicator (Yellow)	When this switch is pressed, program/data from the input device designated by the Load Unit switches are loaded to main memory. The associated indicator and the RUN indicator are lit when the Load Switch is pressed. Upon successful completion of loading the Load indicator is turned off.
START	Pushbutton Switch/ Indicator (Green)	This momentary contact switch when pressed and then released will start the processor. The indicator is lit when the processor is running.

Notes: 1. This switch is duplicated on the 70/45 Maintenance Panel.
2. This indicator is duplicated on the 70/45 Maintenance Panel.
3. These indicators are duplicated on the Maintenance Panel.

OPERATOR'S KEYBOARD

◆ The following describes the functions of the keys on the Operator's Keyboard. Figure 12 illustrates the Keyboard layout.

RETURN — Pressing down on this keylever will cause the type box and printing carriages to return to the left-hand margin and the paper feed mechanism to advance. One or two lines will advance, depending on the position of the feed mechanism control.

REPT (Repeat) — When this keylever is pressed simultaneously with another keylever or the space bar and held down, it will cause that character or function to repeat as long as the Repeat keylever is held down.

SHIFT — When pressed simultaneously with a character keylever, this keylever will cause the "upper case" character of the character keylever to be printed.

SPACE Bar — Pressing this bar will cause the typewriter to perform a print function on a blank space of the type box. This will cause a blank space on the paper, the size of one character. If the computer is reading from the typewriter a space character is sent to HSM.

ERROR — This keylever is used to terminate a Read Command when a typographic error is detected. Pressing down on this keylever, the SEND lamp will go out and the Read Command will terminate with an indication of a data error.

EOT (End of Transmission) — This keylever is used to terminate a Read Command upon completion of the message. When this keylever is pressed, the SEND lamp will extinguish and the Read Command will be terminated.

LOC LF (Local Line Feed) — When this keylever is held pressed, paper will advance through the mechanism without the carriage return function. Paper is fed out smoothly, not incrementally as when pressing the RETURN keylever.

LOC CR (Local Carriage Return) — Pressing this keylever will cause the type box and printing carriages to return to the left-hand margin without feeding paper through the mechanism.

Non-slip Paper Feed — Continuous non-slip form feeding is accomplished by the sprocket pins located in the platen which engage corresponding holes in the form feed paper being utilized.

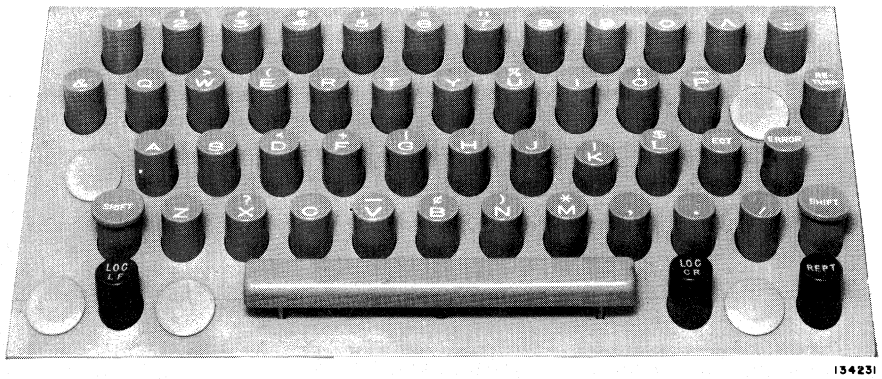


Figure 12. Model 70/97 Operator's Console Keyboard Layout

MAINTENANCE CONSOLE PANELS

MAINTENANCE PANEL

◆ Table 4 lists the various controls and indicators available on the Maintenance Panel. In addition, the type of control (Pushbutton/Switch and/or Indicator) and a brief description or function of the control and/or indicator are also given. The figure reference number contained in Table 4 is indicated on Figure 13. *(Actually these reference numbers do not appear on the panel, they are supplied herein as an aid for orienting the switch and/or indicator.)*

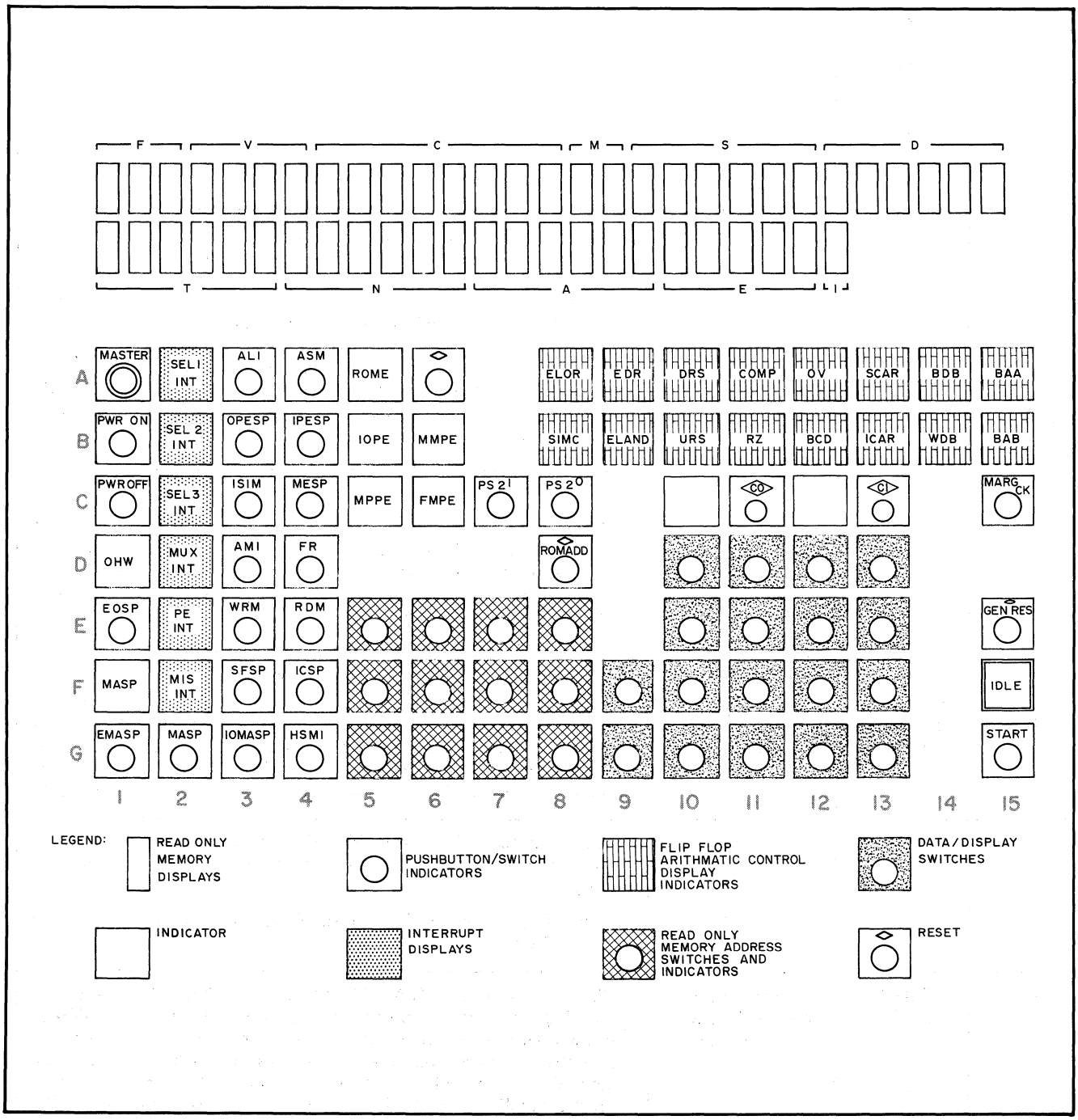


Figure 13. Model 70/45 Maintenance Panel

Table 4. Model 70/45 Maintenance Panel (Indicators and Controls)

(Reference Fig. 13)

Figure Reference No.	Panel Designation	Type	Description and Function
As shown	F V C M S D T N A E I	Indicators (Yellow)	Refer to text for the functions of these READ ONLY MEMORY REGISTER Displays. (Page 30.)
A 1	MASTER	Pushbutton Switch/Indicator (Green)	This alternate action switch is used to enable the power supply control circuits and must be in the ON condition before the POWER ON switch can be activated. The switch can be used as an emergency off switch, in which case DC power is disconnected by passing the normal DC power off sequencing and causing the power failure interrupt to be set in the processor. The indicator is turned on upon the pressing of this switch and remains on until the switch is pressed again to turn off power. Whenever this switch is in its OFF condition, the POWER ON on the Operator's Display Panel is ineffective. *Note:* This switch is duplicated on the 70/97 Operator's Console Panel.
B 1	POWER ON	Pushbutton Switch/Indicator (Green)	When this POWER ON momentary contact switch is pressed it will permit the DC voltage of the processor to be turned on. The indicator is turned on only at the completion of the power-up sequence and remains on until power is turned off. *IMPORTANT:* This switch is ineffective until both MASTER switches are ON.
C 1	POWER OFF	Pushbutton Switch/Indicator (Green)	This POWER OFF momentary contact switch and indicator is used to cause normal power off sequencing of the DC voltages in the Processor. After pressing this switch the indicator will remain lit until the AC power line in the Processor is disconnected.
D 1	OHW	Indicator (Red)	This OVERHEAT WARNING indicator will light whenever the temperature in the Processor has exceeded its environmental design. *Note:* This indicator is duplicated on the Operator's Display Panel.
E 1	EOSP	Pushbutton Switch/Indicator (Yellow)	This READ ONLY MEMORY ADDRESS STOP alternate action switch provides the means for making Read Only Memory Address comparisons. When this switch is set the indicator is turned on and the Processor compares the address of each EO to be performed with the address set in Memory Address Stop switches on the Auxiliary Panel. When equality is met, the separate MASP equality indicator is turned on and the Processor is halted.

Table 4. Model 70/45 Maintenance Panel (Indicators and Controls) (Cont'd)

(Reference Fig. 13)

Figure Reference No.	Panel Designation	Type	Description and Function
F 1	MASP	Indicator (Yellow)	This MEMORY ADDRESS STOP indicator is turned on when the memory address and the address set in the Memory Address Stop Switches on the Auxiliary Panel are equal for the conditions imposed by the setting of the EOSP, MASP, EMASP and IOMASP operate switches.
G 1	EMASP	Pushbutton Switch/Indicator (Yellow)	This MEMORY ADDRESS STOP Execute alternate action switch provides the main memory address comparison during instruction executions. When this switch is set, the Processor will compare the address of each main memory location accessed during instruction execution (including I/O initiation and interrupt processing but excluding I/O servicing) with the address set in the Memory Address Stop Switches on the Auxiliary Maintenance Panel. (See Table 5.) The indicator is turned on when the switch is set. When equality is met, the separate MASP equality indicator is turned on and the Processor is halted. *Note:* This switch may be set in combination with other MASP operate switches.
A 2	SEL 1 INT	Indicators (Green)	These six Interrupt Display indicators display the state (set or reset as indicated by the condition of the indicator, either on or off) of the processor interrupt flags. These are designated as follows: SEL 1 Int = I/O Selector Channel 1 SEL 2 Int = I/O Selector Channel 2 SEL 3 Int = I/O Selector Channel 3 MUX Int = I/O Multiplexor Channel PE Int = Program Error (indicator on if any of the following interrupt flags are set): Privileged Operation OP — Code Trap Address Error Data Error Exponent Overflow Divide Error Significant Error Exponent Underflow Decimal Overflow Fixed Point Overflow MIS Int = Miscellaneous (indicator on if any of the following interrupt flags are set): External Signals 1 through 6 Elapsed Time Clock Console Interrupt Request Supervisor Call Instruction Debug Mode
B 2	SEL 2 INT		
C 2	SEL 3 INT		
D 2	MUX INT		
E 2	PE INT		
F 2	MIS INT		

Table 4. Model 70/45 Maintenance Panel (Indicators and Controls) (Cont'd)

(Reference Fig. 13)

Figure Reference No.	Panel Designation	Type	Description and Function
G 2	MASP	Pushbutton Switch/Indicator (Yellow)	The purpose of this MEMORY ADDRESS STOP-STATICIZING alternate action switch is to provide the main memory address comparison when instructions are staticized. When switch is set the indicator is turned on and the processor compares the address of each instruction staticized with the address in the Memory Address Stop Switches on the Auxiliary Maintenance Panel. (See Table 5.) The comparison is made on the location of the operation code only. When equality is reached the separate MASP equality indicator is turned on and the processor is halted.
A 3	ALI	Pushbutton Switch/Indicator (Yellow with Red border)	When this ALARM INHIBIT alternate action switch is set, the Processor will not execute actions normally performed as a result of machine errors. The error indicator(s) will be lit but in all other respects the error will be ignored. *Notes:* 1. The indicator may also be turned on by the IDLE instruction with Field bit 2^0 set. 2. This switch does not inhibit error actions at I/O control electronics. 3. This switch may be pressed while processor is running.
B 3	OPESP	Pushbutton Switch/Indicator (Yellow)	When this PROGRAM ERROR ORDERLY STOP alternate action switch is set, subsequently detected program errors will cause the Processor to be halted after completion of the current instruction. I/O servicing (e.g., data transfer) may continue to completion. Pressing this switch turns on the indicator. *Note:* A maximum of 10 seconds may elapse between detection of a program error and processor halt. Interrupts occurring during this time will not be taken, however, the hardware interrupt flag will be set.
C 3	ISIM	Pushbutton Switch/Indicator (Yellow)	This INHIBIT SIMULTANEITY alternate action switch is used to perform normal processing and Input/Output servicing in a serial mode. When an I/O instruction is initiated, no further processing will take place until the termination of the input/output occurs through an interrupt. The switch must be set prior to the initiation of the I/O. If an interrupt occurs during an I/O execution, with ISIM set, the interrupt is made and then serviced after the I/O has been completed.
D 3	AMI	Pushbutton Switch/Indicator (Yellow)	When this ADDRESS MODIFICATION INHIBIT alternate action switch is set, a normal address incrementing is inhibited to allow repeated addressing of the memory location currently being accessed. Pressing the switch turns on the indicator.
E 3	WRM	Pushbutton Switch/Indicator (Yellow)	When this WRITE MEMORY alternate action switch is set, data entered to the Utility Register by means of the Data/Display switches are written to a specified memory location when the START switch is pressed. Pressing this switch turns on the indicator.

Table 4. Model 70/45 Maintenance Panel (Indicators and Controls) (Cont'd)

(Reference Fig. 13)

Figure Reference No.	Panel Designation	Type	Description and Function
F 3	SFSP	Pushbutton Switch/Indicator (Yellow)	The SINGLE FUNCTION STOP alternate action switch provides the means for manually stepping through an instruction, one function at a time.
G 3	IOMASP	Pushbutton Switch/Indicator (Yellow)	The MEMORY ADDRESS STOP I/O SERVICING alternate action switch provides the main memory address comparison at the main memory locations addressed during I/O data service. When this switch is set the indicator is turned on. When equality is reached the separate MASP equality indicator is turned on and the Processor is halted.
A 4	ASM	Pushbutton Switch/Indicator (Yellow/Red Border)	This ADDRESS SHADED MEMORY alternate action switch allows the addressing of non-addressable memory for display or modification. Pressing this switch causes the indicator to be lit.
B 4	IPESP	Pushbutton Switch/Indicator (Yellow)	This PROGRAM ERROR IMMEDIATE STOP alternate action switch is used to halt the Processor upon detection of a program error. When switch is pressed the indicator is turned on.
C 4	MESP	Pushbutton Switch/Indicator (Yellow)	The MACHINE ERROR STOP alternate action switch is used to halt the Processor immediately upon detection of a machine error. Pressing this switch will turn on the indicator.
D 4	FR	Pushbutton Switch/Indicator (Yellow)	This FUNCTION REPEAT alternate action switch when pressed will cause the repetition of a single function to be performed by the Processor and will light the indicator.
E 4	RDM	Pushbutton Switch/Indicator (Yellow)	This READ MEMORY alternate action switch is used to read data from memory into the UR register which can be displayed on the Data/Display switches. Pressing this switch will turn on the indicator light.
F 4	ICSP	Pushbutton Switch/Indicator (Yellow)	This INSTRUCTION COMPLETE STOP alternate action switch when pressed will cause the processor to halt at the completion of the current instruction. Pressing this switch will turn on the indicator light. Pressing the START switch while ICSP is activated will cause the Processor to execute one instruction and stop. *Note:* This switch may be used to stop the Processor in the same manner as that of the STOP switch on the Operator's Display Panel.
G 4	HSMI	Pushbutton Switch/Indicator (Yellow)	The HIGH SPEED MEMORY INHIBIT alternate action switch is used to inhibit accessing of the main memory locations during operation. The indicator is turned on when the switch is set.
A 5	ROME	Indicator (Red)	This READ ONLY MEMORY ERROR indicator when lit indicates that an error has been detected in the Read Only Memory.

Table 4. Model 70/45 Maintenance Panel (Indicators and Controls) (Cont'd)

(Reference Fig. 13)

<table>
<tr><th>Figure Reference No.</th><th>Panel Designation</th><th>Type</th><th>Description and Function</th></tr>
<tr><td>B 5</td><td>IOPE</td><td>Indicator (Red)</td><td>The INPUT/OUTPUT PARITY ERROR indicator is turned on whenever the Processor detects any Read Parity Error from an input device or if any I/O error occurs during a load operation.</td></tr>
<tr><td>C 5</td><td>MPPE</td><td>Indicator (Red)</td><td>The MEMORY PROTECTION PARITY ERROR indicator when lit indicates that a parity error has been detected in accessing the memory protection key.</td></tr>
<tr><td>A 6</td><td>(ALR) Not marked on panel</td><td>Pushbutton Switch</td><td>This ALARM RESET momentary switch is used to reset MPPE, MMPE, IOPE, FMPE, and ROME indications on the processor.</td></tr>
<tr><td>B 6</td><td>MMPE</td><td>Indicator (Red)</td><td>This MAIN MEMORY PARITY ERROR indicator is lit whenever a parity error has been detected in the main memory.</td></tr>
<tr><td>C 6</td><td>FMPE</td><td>Indicator (Red)</td><td>This FAST MEMORY PARITY ERROR indicator is lit whenever a parity error has been detected in the fast memory of the Processor.</td></tr>
<tr><td>C 7</td><td>PS 2^1</td><td rowspan="2">Pushbutton Switches and Indicators (Yellow)</td><td rowspan="2">These two PROCESSOR STATE momentary switches when used permit the processor state to be changed when the Processor is halted. The indicators display the processor state. This indication is:
<table>
<tr><th>PS 2^1</th><th>PS 2^0</th><th>Processor State</th></tr>
<tr><td>0</td><td>0</td><td>4</td></tr>
<tr><td>0</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>2</td></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
</table>
Thus, to change from state 1 (11) to state 2 (10) press switch PS 2^0. GEN RES sets PS2^1 and PS2^0, pressing either pushbutton resets its corresponding indicator.</td></tr>
<tr><td>C 8</td><td>PS 2^0</td></tr>
<tr><td>D 8</td><td>◇ ROM ADD</td><td>Pushbutton Switch/Indicators (Green)</td><td>This READ ONLY ADDRESS MEMORY momentary switch is the RESET pushbutton switch for the Read Only Memory Address switches.</td></tr>
<tr><td>E 5
F 5
G 5
E 6
F 6
G 6
E 7
F 7
G 7
E 8
F 8
G 8</td><td>NONE</td><td>Pushbutton Switch/Indicators (Green)</td><td>These READ ONLY MEMORY ADDRESS momentary contact switch indicators are used to display the address of the ROM location that is being addressed and to select a particular ROM location for display. Whenever the Processor is stopped the next ROM address is displayed and the contents of the last location addressed are displayed in the Read Only Memory display. These switches must not be pressed while the Processor is running.</td></tr>
</table>

Table 4. Model 70/45 Maintenance Panel (Indicators and Controls) (Cont'd)

(Reference Fig. 13)

Figure Reference No.	Panel Designation	Type	Description and Function
A 8 A 9 A 10 A 11 A 12 A 13 A 14 A 15 B 8 B 9 B 10 B 11 B 12 B 13 B 14 B 15	As Noted in Description and Functions	Indicators (Green)	These groups of indicators display the state of the following Processor flip-flops: *Reference* — *Label* — *Flip-Flop Name* A 8 — ELOR — Enable Logical OR A 9 — EDR — Enable Data Register A 10 — DRS — Data Register Sign A 11 — COMP — Complement A 12 — OV — Overflow A 13 — SCAR — Sum Carry A 14 — BDB — Byte Divider Bit A 15 — BAA — Byte Address A B 8 — SIMC — Simulate Carry (for logical operation) B 9 — ELAND — Enable Logical AND B 10 — URS — Utility Register Sign B 11 — RZ — Result Zero B 12 — BCD — Binary Coded Decimal B 13 — ICAR — Initial Carry B 14 — WDB — Word Divider Bit B 15 — BAB — Byte Address B When the flip-flop is set, the indicator is on.
C 10 C 12	None	Indicators (Yellow)	Parity Indicators — When MMR is displayed, C10 displays the parity bit for the most significant byte and C12 displays parity bit for the least significant byte. When DR or a FM location is displayed C10 displays the parity bit for the two bytes selected. Odd parity is used. The other registers do not have a parity bit associated with them.
C 11 C 13	C 0 C 1	Pushbutton Switch/Indicators (Yellow)	These C0 and C1 RESET momentary contact switches are used for resetting the Data/Display indicators, i.e., one for each byte.
D 10 D 11 D 12 D 13 E 10 E 11 E 12 E 13 F 9 F 10 F 11 F 12 F 13 G 9 G 10 G 11 G 12 G 13	NONE	Pushbutton Switch/Indicators (Yellow)	These DATA/DISPLAY momentary contact switches are used to display or modify the contents of hardware registers, fast memory or main memory as selected by the appropriate switches. Selection of register or memory location to be displayed is determined by the applicable switches on the auxiliary maintenance panel.

Table 4. Model 70/45 Maintenance Panel (Indicators and Controls) (Cont'd)

(Reference Fig. 13)

Figure Reference No.	Panel Designation	Type	Description and Function
C 15	MARG CK	Pushbutton Switch/Indicator (Yellow/Red border)	When MARGINAL CHECK indicator is lit it indicates that main memory is in the marginal check mode. When any position of the Memory Bank Selection switch on the Auxiliary Maintenance Panel is pressed, this indicator is turned on and remains on until the switch is reset. This switch is a lamp check switch.
E 15	GEN RES	Pushbutton Switch	This GENERAL RESET momentary contact switch when pressed will reset the system conditions to a state enabling an orderly start-up. *Note:* This switch is duplicated on the Operator's Display Panel.
F 15	IDLE	Indicator (Yellow/Red border)	This indicator is turned on when the Idle instruction is operating. *Note:* This indicator is duplicated on the Operator's Display Panel.
G 15	START	Pushbutton Switch/Indicator (Green)	Pressing and releasing this START momentary contact switch will start the Processor. The indicator is also lit at the same time, and will remain lit until the Processor is halted. The indicator is also turned on whenever a Load operation, from the Operator's Display Panel, has been initiated. *Note:* This indicator is duplicated on the Operator's Display Panel.

Read Only Memory Register Display

The 53 indicators on the Read Only Memory Display portion of the Maintenance Panel correspond to the 53 bits comprising a 70/45 Elementary Operation (EO). When the processor is running, these indicators will display the EO's at processor speeds. When the processor is halted, they display the EO in the Read Only Memory location as selected by the Read Only Memory Address switches, or the last Elementary Operation executed if no selection has been made. The panel designations are as follows:

EO Fields	Panel Marking	Function
Function Control	F	Function of EO
	V	Variation of EO
	C	Counter
Data Movement Control	M	Memory
	S	Source
	D	Destination
Branch Control	T	Test
	N	Normal
	A	Alternate
Exception Check Control	E	Exception
Inhibit Control	I	Inhibit

AUXILIARY MAINTENANCE PANEL

◆ Figure 14 illustrates the controls and indicators located on the Auxiliary Maintenance Panel. Table 5 lists the use and description of these controls.

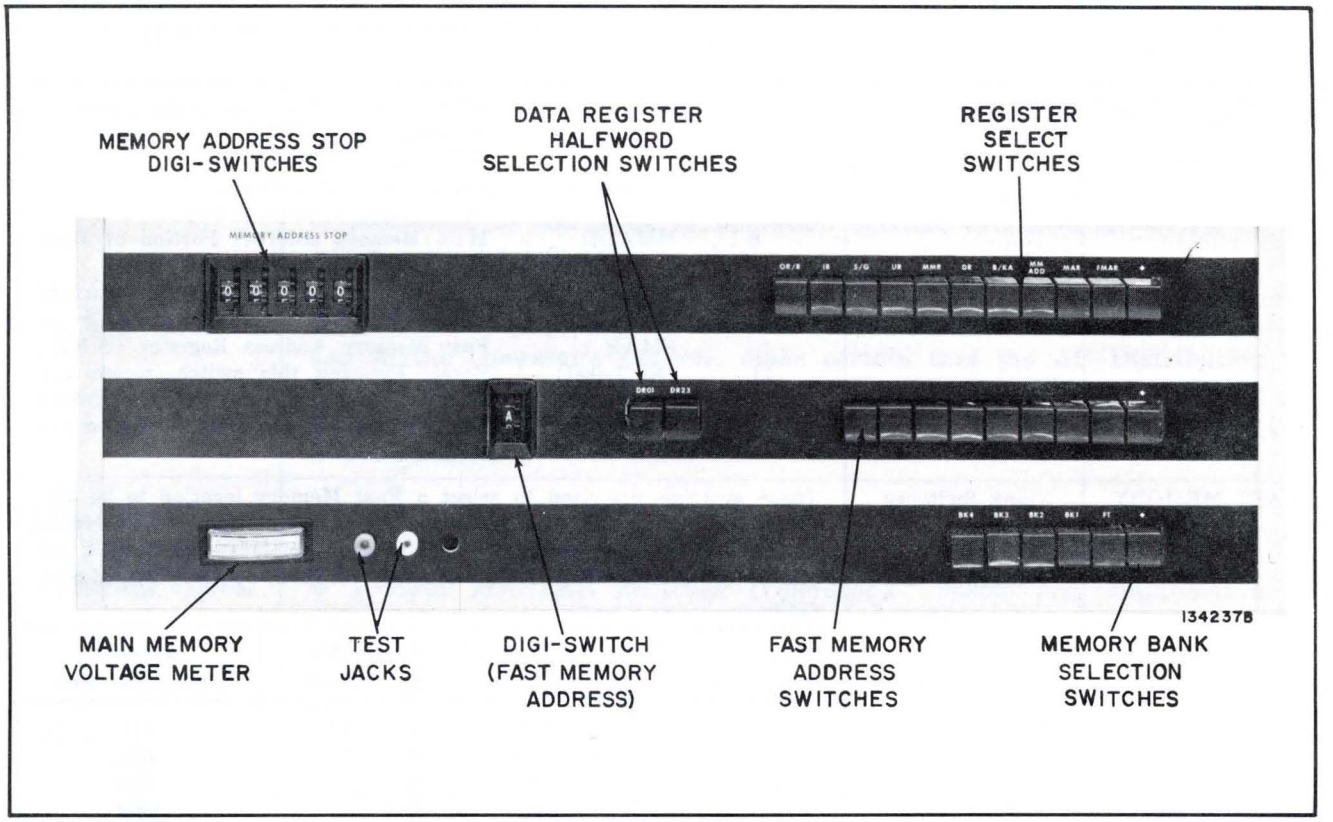


Figure 14. Model 70/45 Auxiliary Maintenance Panel

Table 5. Model 70/45 Auxiliary Maintenance Panel (Indicators and Controls)

(Reference Fig. 14)

Name and/or Panel Designation	Type	Description and Function
MEMORY ADDRESS STOP	Digi-Switches	This group of five digi-switches provides the means for entering the address on which the Processor is to perform Memory Address Stop comparison. Each switch has 16 positions, ranging from 0 to 9, and A to F, for entry of the address in hexadecimal digits.
REGISTER SELECT	Gang Switches (All positions)	This group of eleven switches is used to select hardware registers whose contents are to be displayed or modified by the Data/Display switches. The switches are labeled as follows: *Switch Position* / *Control Label* / *Register* 1 / OR/R / Operation Code Register (8 bits); R Register (8 bits) 2 / IR / Intermediate Register (16 bits) 3 / S/G / S Register (8 bits); G Register (8 bits) 4 / UR / Utility Register (16 bits) 5 / MMR / Main Memory Register (18 bits) 6 / DR / Data Register (34 bits)

Table 5. Model 70/45 Auxiliary Maintenance Panel (Indicators and Controls) (Cont'd)

(Reference Fig. 14)

<table>
<tr><th>Name and/or Panel Designation</th><th>Type</th><th>Description and Function</th></tr>
<tr><td>REGISTER SELECT (Cont'd)</td><td></td><td>
7 B/KA — B Register (4 bits); Protection Key (4 bits); ASCII Mode (1 bit); Emulation Control (2 bits); Non-Privileged Mode (1 bit)
8 MMADD — Main Memory Address Portion of Data Register — next address (18 bits)
9 MAR — Main Memory Address Register — current address (18 bits)
10 FMAR — Fast Memory Address Register (7 bits)
11 (No Label) — Reset: Pressing this switch, resets any other previously set position. This switch must be pressed before the processor can be started.
</td></tr>
<tr><td>FAST MEMORY ADDRESS</td><td>Gang Switches (9 positions) and Digi-Switch</td><td>
These switches are used to select a Fast Memory location to be displayed or modified by the Data/Display switches. The leftmost eight positions of the gang switch are used to select the least significant three bits of the address of the Fast Memory location, and initiates a read cycle.
<table>
<tr><th>Switch Position</th><th>3 Least Significant Bits</th><th>Switch Position</th><th>3 Least Significant Bits</th></tr>
<tr><td>7 (leftmost)</td><td>111</td><td>3</td><td>011</td></tr>
<tr><td>6</td><td>110</td><td>2</td><td>010</td></tr>
<tr><td>5</td><td>101</td><td>1</td><td>010</td></tr>
<tr><td>4</td><td>100</td><td>0</td><td>000</td></tr>
</table>
The ninth position ◇ performs a write to the selected Fast Memory location of data previously entered to the Data/Display switches.
The Digi-switch is used to select the four most significant bits of the Fast Memory Address. This switch has 16 positions, ranging from 0 to 9, and A to F, for entry of the four bits.
</td></tr>
<tr><td>MEMORY BANK SELECTION</td><td>Gang Switches (6 positions)</td><td>The purpose of this gang switch is to select a main memory bank for marginal voltage testing. The four leftmost positions of these switches are labeled BK1 through BK4, respectively. The next position, labeled FT, is the Function Test switch which sets all Memory banks for testing. Pressing one of these switches enables the associated Voltage Meter and Voltage Adjustment screw, and turns on the Marginal Check indicators on the Maintenance Panel. The last position ◇ , is used to reset the other switches.</td></tr>
<tr><td>DR 01
DR 23</td><td>Gang Switches (2 positions)</td><td>The purpose of these switches is to cause the display of alternate halfwords of the Data Register. When the Data Register or Fast Memory location has been selected for the display in the Data/Display switches, the setting of this switch determines which halfword will be displayed. Pressing the DR01 causes the left halfword (17 bits) of the register to be displayed in the Data/Display switches. Pressing the DR23 causes the right halfword of the register to be displayed in the Data/Display switches. The DR01 signifies byte 0 and byte 1 of the register; DR23 signifies byte 2 and byte 3. DR23 must be pressed before the processor can be started.</td></tr>
<tr><td>NONE</td><td>Voltage Meter/ Range 0–25 and Meter Jacks</td><td>This Voltage Meter provides visual indication of the voltage being applied to the Main Memory bank. Associated with the meter is the voltage adjusting screw and two separate pairs of meter jacks for maintenance use only.</td></tr>
</table>

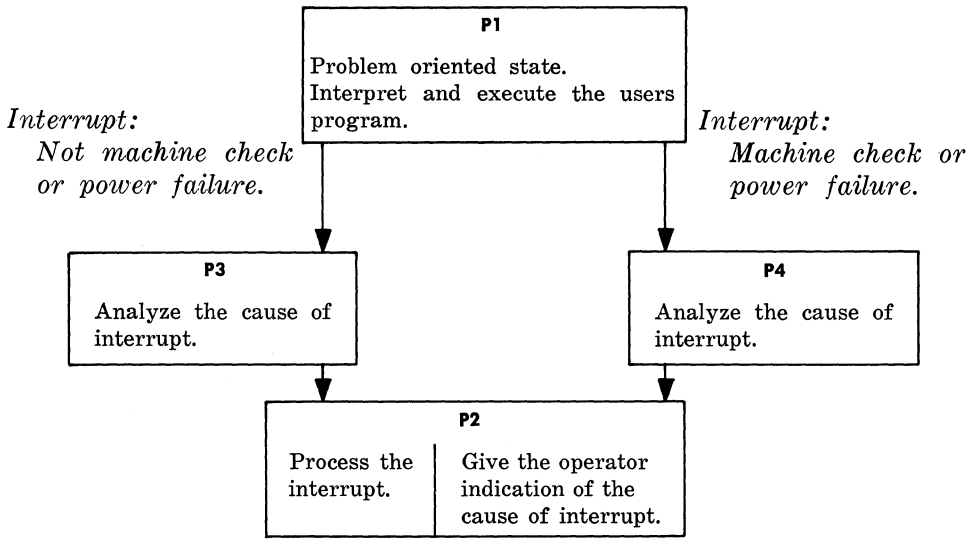
FEATURES

Interrupt

◆ The Model 70/45 Processor has four distinct processor states to provide extremely fast interrupt servicing. Combined with the program systems control, these processor states provide efficient interrupt handling.

Upon detection of interrupt the hardware initiates Processor States 3 and 4. It is the programs responsibility to determine what action is to be taken in any processor state.

As an example the Processor States may be used as follows:



Register addressing in each of the processor states is given in Table 6.

Table 6. Register Addressing in the Processor States

Register Number	Processor States			
	P_1	P_2	P_3	P_4
0	GR	GR	IMR, P_1 State	Processor Utility
1	GR	GR	ISR, P_1 State	Processor Utility
2	GR	GR	P counter, P_1 State	Processor Utility
3	GR	GR	Interrupt Flag Register	Processor Utility
4	GR	GR	IMR, P_2 State	Processor Utility
5	GR	GR	ISR, P_2 State	Processor Utility
6	GR	GR	P counter, P_2 State	Processor Utility
7	GR	GR	GR	Processor Utility
8	GR	GR	IMR, P_3 State	GR
9	GR	GR	ISR, P_3 State	GR
10	GR	GR	P counter, P_3 State	GR
11	GR	GR	GR	GR
12	GR	GR	GR	IMR, P_4 State
13	GR	GR	GR	ISR, P_4 State
14	GR	GR	GR	P counter, P_4 State
15	GR	GR	GR/Weight	GR/Weight

GR = General Register
IMR = Interrupt Mask Register
ISR = Interrupt Status Register

Interrupt (Cont'd)

Since each processing state has its own General-Purpose registers, Interrupt Status register, and Interrupt Mask register, the need for storing and reloading registers during interrupt processing is virtually eliminated.

Program interrupts occur as a result of errors in data or instruction specifications, input/output operations, external signals, equipment malfunctions, or arithmetic errors. The instruction being executed at the time of interrupt may be completed, suppressed, or terminated depending on the cause of the interrupt.

Any interrupt may be inhibited or permitted in any state by the program. If an interrupt occurs and is permitted, conditions existing in the interrupted state will be automatically stored. Control is then passed to the Interrupt Control State (P_3) or Machine Condition State (P_4) depending upon the cause of the interrupt. The priority of the interrupt is established and an analysis is made to determine the proper linkage to the Interrupt Response State (P_2) so that the interrupt may be processed. Once interrupt processing has been completed, control is returned to the state which was last interrupted and normal processing is resumed.

If several interrupts occur at the same time, the one having the highest priority will be processed. The remaining interrupts will be processed in turn depending upon their priority.

Table 7 summarizes all of the interrupt conditions, their respective priorities, the interrupt state which each initiates, and a brief description of the cause of interrupt.

Accuracy Control

◆ The following accuracy controls are incorporated within the 70/45 Processor:

1. Each byte read out of HSM is automatically checked for odd parity.
2. Each data byte read in from a peripheral device is automatically checked for odd parity.
3. Each half-word read out of FM is automatically checked for odd parity.
4. The Read Only Memory (ROM) has a built in automatic error detection scheme.
5. Each four bit key read out of the Memory Protect Memory (optional) is automatically checked for odd parity.

Notes: 1. If a ROM Error or a Memory Protect parity error occurs, the Processor will stop.

2. If a HSM or DR or I/O parity error occurs the interrupt routine will be initiated. However, if a HSM or DR parity error occurs when the machine is in Processor State 4, the Processor will stop.

Table 7. 70/45 Interrupt Conditions

Priority	Condition	State Initiated	Explanation
1	Power Failure	4	Power failure in processor or memory.
2	Machine Check	4	Parity error or equipment malfunction.
3	External Signal 1	3	Signal received on one of the six external lines associated with the direct-control feature.
4	External Signal 2	3	
5	External Signal 3	3	
6	External Signal 4	3	
7	External Signal 5	3	
8	External Signal 6	3	
9	Not Specified		
10	Selector 1	3	A device on the associated selector channel requires servicing
11	Selector 2	3	
12	Selector 3	3	
13	Not specified		
14	Not specified		
15	Not specified		
16	Multiplexor	3	A device on the multiplexor channel requires servicing.
17	Elapsed Time Clock	3	Elapsed time count has expired.
18	Console Request	3	Manual request for interrupt by the operator.
19	Not specified		
20	Not specified		
21	Supervisor Call	3	Result of execution of Supervisor Call instruction to utilize programmed routines.
22	Privileged Operation	3	Privileged instruction attempted in non-privileged mode.
23	Op-Code Trap	3	Op Code attempted which is invalid for this processor.
24	Address Error	3	Invalid address, specification, or memory protect violation.
25	Data Error	3	Sign of operand incorrect in decimal arithmetic and editing, or incorrect field overlap.
26	Exponent Overflow	3	Result characteristic of floating-point operation is greater than 127.
27	Divide Error	3	Rules pertaining to Divide instruction have been violated.
28	Significance Error	3	Result of floating-point add or subtract has zero fraction.
29	Exponent Underflow	3	Result characteristic of floating-point operation is less than zero.
30	Decimal Overflow	3	Result field is too small to contain the result of a decimal operation.
31	Fixed-Point Overflow	3	High-order carry or high-order significant bits lost in fixed-point operation.
32	Test Mode	3	Allows program control over processor during program testing.

OPTIONAL FEATURES

◆ A variety of optional features are available to enhance the operation of the 70/45 Processor. These features provide specific functions and are incorporated into the electronic controls of the processor. The functions are described briefly below:

Memory Protect

◆ *Feature 5001-45* — Protects the Main Memory from being destroyed by either Programming or by an input device.

Elapsed Time Clock

◆ *Feature 5002-45* — Incorporates real time control operation within the Processor.

Direct Control

◆ *Feature 5003-45* — Provides the means for the transfer of control and synchronizing of information between Processors.

Selector Channels

◆ *Feature 5015* — This feature provides two Selector Channels for controlling the transfer of data to and from a peripheral device.

Feature 5016 — This feature provides three Selector Channels for controlling the transfer of data to and from a peripheral device.

Emulator Options

◆ A number of emulator optional features are used for executing programs coded for other computers on the 70/45:

301 Emulator — Feature 5005-45 — Provides the ability of running 301 System programs utilizing the 70/45 Processor.

1401 Emulator — Feature 5006-45 — Provides the ability of running 1401 System programs utilizing the 70/45 Processor.

501 Emulator — Feature 5007-45 — Provides the ability of running 501 System programs utilizing the 70/45 Processor.

1410 Emulator — Feature 5026-45 — Provides the ability of running 1410 System programs utilizing the 70/45 Processor.

301/501 Emulator — Feature 5036-45 — Provides the ability of running 301/501 System programs utilizing the 70/45 Processor.

1410/1401 Emulator — Feature 5046-45 — Provides the ability of running 1410/1401 System programs utilizing the 70/45 Processor.

OPERATION

PREPARATION FOR OPERATION

◆ Prior to undertaking the NORMAL OPERATING procedures, the following should be performed:

Operator's Console

◆ 1. Inspect that there is a sufficient supply of paper and examine the condition of the inked ribbon. (Refer to EQUIPMENT CARE.)

2. Check that the switch (located behind the Operator's Display Panel) is positioned to the mode of operation desired, i.e., LOCAL — OFF — LINE. Lift the Top Cover to obtain access to this switch.

Power Supply Rack

◆ Prior to the application of power to the Maintenance Console Panel and to the Operator's Console, make certain that the AC Distribution Panel circuit breaker switches are all in their ON condition. Ascertain that there are no malfunctioning alarm displays on the Power Supply Control Panel.

NORMAL OPERATION

Applying Power

◆ 1. Both MASTER switches (Operator's Console and Maintenance Panel) must be in their ON position to enable DC power control circuits. Press MASTER switch on the Operator's Console, the indicator will light. Press MASTER switch on the Maintenance Panel, its indicator will light. The MASTER switches may be used for emergency POWER OFF switches if it becomes necessary to do so.

2. Press the POWER ON switch on the Maintenance Panel. The indicator will light upon the completion of the power-up sequence cycle, thus indicating the DC power has been applied. The POWER OFF indicator at the Maintenance Panel will be turned off and the POWER READY indicator on the Operator's Console will be turned on.

3. Press and hold down the IDLE pushbutton on the Operator's Console. This provides a lamp check for the console. Ascertain that all indicators on the console are lit. Pressing the IDLE pushbutton will also light the OHW indicator on the Maintenance Panel. Therefore, ascertain that the indicator at the Maintenance Panel is also turned on.

4. Press and hold down the MARG CK pushbutton on the Maintenance Panel. This will provide a lamp check for all indicators and controls on the Maintenance Panel. Ascertain that all indicators and controls on the Maintenance Panel (except POWER OFF and OHW), are lit.

5. Upon the application of power, listen to the fans or blower motors in each equipment rack and make certain that they are operating. Examine filters and clean if necessary. Refer to *Equipment Care* for details.

6. Press the GEN RES switch on either the Operator's Display Panel or the Maintenance Panel. The Processor is now conditioned for operation.

Removing Power

◆ 1. Press the POWER OFF switch on the Maintenance Panel. The DC power will cycle down and when the DC power is removed, the POWER ON indicator will go off and the POWER OFF indicator will light.

2. Press the MASTER switch to remove power.

INITIAL PROGRAM LOADING

◆ Initial Program Loading is accomplished from the Operator's Console in the following manner.

1. *Initial Program Load from Operator's Console*

   Note: It is assumed that the processor power is ready and the Maintenance/Auxiliary Maintenance Panel switches are reset.

   a. Establish required conditions at input device.

   b. Press GEN RES switch to clear the processor to establish the required condition for start-up. Refer to step 6, under Applying Power.

   c. Enter the channel and device number of loading device to the Load Unit Switches.

   d. Press LOAD switch. (One record, card or block will be read from input device to main memory starting at address zero.) After completion of the read instructions are executed starting at location zero.

   e. When loading has been completed successfully, it will be indicated by the LOAD indicator light being turned off. The START (Run Indicator) will remain lit, (Program Running).

   f. In the event that in the process of loading, the loading is terminated due to an error condition the START (Run Indicator) will be turned off and the LOAD indicator will stay lit. In addition, the processor detected errors (MPPE, MMPE, FMPE, IOPE, ROME or PEINT) indicators on the Maintenance Panel and the ERROR indicator on the Operator's Display Panel will be lighted.

   g. To re-attempt an Initial Load function repeat from step a.

2. *Read and Write Main Memory via the Maintenance Panel*
   Read Main Memory

   The procedures for reading and displaying the contents of a Main Memory location using the Maintenance Panel is described as follows:

   Note: It is assumed that the processor is halted and the Maintenance Panel switches are reset.

   a. Press MMADD position of the Register Selection Switch on the Auxiliary Maintenance Panel.

   b. Enter main memory address to MMADD via the DATA/DISPLAY switches. (This address is an 18 bit, halfword oriented address, of which the least significant bit is unused.)

   c. Press the Reset position of Register Select Switches.

   d. Press the RDM switch.

   e. Press the START switch. The machine will stop with ROM address $(0400)_8$ displayed.

   f. Press the UR position of the Register Selection Switch on the Auxiliary Maintenance Panel. The contents of the two main memory bytes addressed, will be displayed in the Data/Display Switches.

INITIAL PROGRAM LOADING *(Cont'd)*

g. To read and display the next halfword addressed main memory location, reset the UR position of the Register Selection Switch and repeat steps e and f above.

Note: The above steps e through g need only to be repeated to read and display successive halfwords of main memory since MMADD address is incremented and retained on each subsequent read out operation.

3. *Write to Main Memory*

The procedures for writing to the Main Memory location using the Maintenance Panel is as follows:

Note: It is assumed that the processor is halted and that the Maintenance Panel switches are reset.

a. Press the MMADD position of the Register Selection Switch on the Auxiliary Maintenance Panel.

b. Enter Main Memory address MMADD via the Data/Display switches (18 bit, halfword address, of which the least significant bit is unused).

c. Press Reset position of the Register Select switches.

d. Press WRM switch.

e. Press UR position of the Register Selection switch on the Auxiliary Maintenance Panel.

f. Enter data via Data/Display switches. Entry data consists of two data bytes (16 bits) without parity.

g. Press Reset position of Register Select Switches.

h. Press the START switch.

i. To write to the next main memory halfword, repeat steps e through h.

Note: The above steps e through h need only to be repeated to write to successive halfwords of main memory since the MMADD address is incremented and retained on each subsequent write operation.

4. *Read and Write to Main Memory* (Combined in One Procedure)

The procedures for reading and writing to Main Memory in a single sequence of steps is as follows:

Note: It is assumed that the Processor is halted and that the Maintenance Panel Switches have been reset.

a. Press MMADD position of Register Selection Switch on Auxiliary Maintenance Panel.

b. Enter main memory address to MMADD via Data/Display switches (18 bit, halfword address).

c. Press Reset position of Register Select switches.

d. Press RDM and WRM switches.

Note: When both are set, RDM takes precedence.

INITIAL PROGRAM LOADING *(Cont'd)*

e. Press AMI switch to inhibit address incrementing.

f. Press START switch to read.

g. Press UR position of Register Selection switch. Two data bytes, are displayed in the Data/Display switches.

h. Enter data (two bytes without parity) via Data/Display switches.

i. Press Reset position of Register Select switches.

j. Press RDM switch to reset (WRM switch remains set).

k. Press AMI switch to reset.

l. Press START switch to write.

m. To read and write to next halfword of main memory press RDM switch to set and repeat step e.

Note: The reading and writing of subsequent half-words is accomplished by repeating steps e through m only, since MMADD address is incremented and retained.

5. *Read Fast Memory*

The procedures for reading Fast Memory location using the Maintenance Panel is as follows:

Note: It is assumed that the processor is halted and that the Maintenance Panel switches are reset.

a. Dial the hexadecimal value of the high order 4 bits of the desired Fast Memory Address in the Digi-Switch of the Fast Memory Address switch group.

b. Press the switch position corresponding to the low order 3 bits of the desired Fast Memory address in the gang switch of the Fast Memory switch group.

c. A halfword (16 bits) of the addressed Fast Memory location with its parity bit is displayed in the Data/Display switches. Determination of the halfword displayed is made by use of the DR01 and DR23 switches. Setting the DR01 switch causes display of the first halfword, setting the DR23 switch causes display of the second halfword.

6. *Write Fast Memory*

The procedure for writing to Fast Memory location using the Maintenance Panel is as follows:

Note: It is assumed that the processor is halted and the Maintenance Panel switches are reset.

a. Dial the hexadecimal value of the high order 4 bits of the desired Fast Memory address in the Digi-Switch of the Fast Memory Address switch group.

b. Press the switch position corresponding to the low order 3 bits of the desired Fast Memory Address in the gang switch of the Fast Memory Address switch group.

c. Select the first halfword to which data are to be entered using the DR01 switch.

INITIAL PROGRAM LOADING *(Cont'd)*

d. Enter data via the Data/Display switches (16 bits).

e. Set the DR23 switch.

f. Enter data via the Data/Display switches.

g. Press the reset position of the Fast Memory Address gang switch to write.

7. *Program Execution*

To execute a program that has been previously loaded into HSM, perform the following:

a. Press the GEN RES pushbutton.

b. Place the starting address in FM location for program counter P1; digi-switch position 4 and gang switch position 2. Place the least significant 16 bits of the address in DR23 and the most significant 2 bits of the address in the least significant bits of DR01.

c. Press the START pushbutton.

8. *Single Instruction Execution*

A single instruction of a given program may be individually staticized and executed as follows:

a. Follow and observe steps a and b of the Program Execution, given above.

b. Press the ICSP (Instruction Complete Stop) pushbutton.

c. Press the START pushbutton. The selected instruction will be executed and the Processor will halt after a ten second delay which allows for I/O termination. Successively pressing the START pushbutton will cause additional instructions in sequence, to be executed. However, there is *no* ten second delay on any of the subsequent instructions executed (after the initial selected instruction).

9. *Manual Instruction Set-up*

Single instructions can be inserted and executed by observing the following:

a. Press the GEN RES pushbutton.

b. Enter the instruction into the desired Main Memory locations. (Refer to Write to Main Memory.)

c. Press the WRM pushbutton, thus causing it to be released.

d. Place the instruction address in the Fast Memory location for program counter P1.

e. Press the GEN RES pushbutton.

f. Press the ICSP pushbutton.

g. Press the START pushbutton to execute the instruction.

INITIAL PROGRAM LOADING *(Cont'd)*

10. *Error Detection and Interpretation*

There are five error display indicators located on the Maintenance Panel and one on the Operator's Display Panel.

The error display indicators on the Maintenance Panel are ROME, IOPE, MPPE, MMPE and FMPE.

The error indicator on the Operator's Display Panel is identified as ERROR. To turn off these indicators press the alarm reset or GEN RES pushbuttons.

The ROME indicator is lit whenever a Read Only Memory Error is detected. This error will also light the ERROR indicator. When this error is detected the processor will stop.

The IOPE indicator is lit whenever a character containing incorrect parity is received from a peripheral device; or during a Load operation whenever a specified device cannot be initiated. This error will also light the ERROR indicator. If this error is detected during a Load operation the processor will stop.

The MPPE indicator is lit whenever a character containing incorrect parity is read out of the Memory Protect memory. This error will also light the ERROR indicator. When this error is detected the processor will stop.

Note: The Memory Protect memory is an optional feature.

The MMPE indicator is lit when a character containing incorrect parity is read out of the Main Memory. This error also lights the ERROR indicator. If this error occurs when the processor is in Processor State 4 or during the Interrupt EO flow, or when the MESP switch is set the machine will stop.

The FMPE indicator is lit when the data read out of the Fast Memory has detected incorrect parity. This error also lights the ERROR indicator and if this error occurs when the machine is in Processor State 4 or during the Interrupt EO flow, or when the MESP switch is set the machine will stop.

The ERROR indicator is also lit if a Program Error is detected while performing a Load Operation. If this occurs the machine will stop.

Error Recovery

◆ Error recovery is effected according to the particular System Recovery Procedure.

SPECIAL OPERATIONS

◆ Tables 8, 9, 10 and 11 are furnished as reference material when performing special operations.

Table 8. Summary of Special Operations

Purpose	Initial ROM Address	Description
All zero check, odd bank	0105	All zero location, odd bank
All zero check, even bank	3250	All zero location, even bank
All one's check, odd bank	0113	All one's location, odd bank
All one's check, even bank	2260	All one's location, even bank
Writing to consecutive main memory locations	3451	One memory cycle consists of 3 EO times; 3451: $(AAD)_{23} \rightarrow$ MAR1; Inc. +2 - The address in FM location AAD is transferred to the main memory address register. The contents of AAD is incremented by two. 3452: IR → MMR2 - The contents of IR is transferred to the main memory register and written to memory. 1263: Test EO - This EO does not change the state of the machine. Allows time for completion of the write cycle.
Reading from consecutive main memory locations	1213	One memory cycle consists of 3 EO times; 1213: $(BAD)_{23} \rightarrow$ MAR2; Inc. +2 - The address in FM location BAD is transferred to the main memory address register. The contents of BAD is incremented by two. — : Blank EO time. No Action. 1216 or 1222: MMR → UR - The contents of the main memory register is transferred to UR.
Writing one half-word to consecutive FM locations	2704	2704: IR → (G); Trig. G-1 - Transfer the contents of IR to the FM location addressed by G. The contents of G is decremented by one.
Writing one full-word to consecutive FM locations	2717	2717: DR → (G) Trig. G-2 - Transfer the contents of DR to the FM location addressed by G. The contents of G is decremented by two.
Writing one half-word to one FM location continuously	2706	2706: IR → (G); No trig. - Transfer the contents of IR to the FM location addressed by G. G is not changed.
Writing one full-word to one FM location continuously	3713	3713: DR → (G); No Trig. - Transfer the contents of DR to the FM location addressed by G. G is not changed.
Reading from consecutive FM locations	2506	2506: (G) → UR; Trig. G-1 - Transfer the contents of the FM location addressed by G to UR. The contents of G is decremented by one.
Reading from one FM location continuously	2500	2500: (G) → UR; No Trig. - Transfer the contents of the FM location addressed by G to UR. G is not changed.

Table 9. Conversion Table (FM Address Switches, Hexadecimal Address)

DIGI-SWITCH (DESIGNATION)	GANG SWITCH							
	7	6	5	4	3	2	1	0
0	07	06	05	04	03	02	01	00
1	0F	0E	0D	0C	0B	0A	09	08
2	17	16	15	14	13	12	11	10
3	1F	1E	1D	1C	1B	1A	19	18
4	27	26	25	24	23	22	21	20
5	2F	2E	2D	2C	2B	2A	29	28
6	37	36	35	34	33	32	31	30
7	3F	3E	3D	3C	3B	3A	39	38
8	47	46	45	44	43	42	41	40
9	4F	4E	4D	4C	4B	4A	49	48
A	57	56	55	54	53	52	51	50
B	5F	5E	5D	5C	5B	5A	59	58
C	67	66	65	64	63	62	61	60
D	6F	6E	6D	6C	6B	6A	69	68
E	77	76	75	74	73	72	71	70
F	7F	7E	7D	7C	7B	7A	79	78

Table 10. Table of Instructions

	FORMAT	MSD	LSD 0	LSD 1	LSD 2	LSD 3	LSD 4	LSD 5	LSD 6	LSD 7	LSD 8	LSD 9	LSD A	LSD B	LSD C	LSD D	LSD E	LSD F
BRANCHING AND STATUS SWITCHING	RR	0					SPM SET PROGRAM MASK	BALR BRANCH AND LINK	BCTR BRANCH ON COUNT	BCR BRANCH ON CONDITION	SSK SET STORAGE KEY	ISK INSERT STORAGE KEY	SVC SUPERVISOR CALL					
FIXED POINT FW AND LOGICAL	RR	1	LPR LOAD POSITIVE	LNR LOAD NEGATIVE	LTR LOAD AND TEST	LCR LOAD COMPLEMENT	NR AND	CLR COMPARE LOGICAL	OR OR	XR EXCLUSIVE OR	LR LOAD WORD	CR COMPARE WORD	AR ADD WORD	SR SUBTRACT WORD	MR MULTIPLY WORD	DR DIVIDE	ALR ADD LOGICAL	SLR SUBTRACT LOGICAL
FLOATING POINT LONG	RR	2	LPDR LOAD POSITIVE (LONG)	LNDR LOAD NEGATIVE (LONG)	LTDR LOAD AND TEST (LONG)	LCDR LOAD COMPLEMENT (LONG)	HDR HALVE (LONG)				LDR LOAD (LONG)	CDR COMPARE (LONG)	ADR ADD NORMALIZED (LONG)	SDR SUBTRACT NORMALIZED (LONG)	MDR MULTIPLY (LONG)	DDR DIVIDE (LONG)	AWR ADD UNNORMALIZED (LONG)	SWR SUBTRACT UNNORMALIZED (LONG)
FLOATING POINT SHORT	RR	3	LPER LOAD POSITIVE (SHORT)	LNER LOAD NEGATIVE (SHORT)	LTER LOAD AND TEST (SHORT)	LCER LOAD COMPLEMENT (SHORT)	HER HALVE (SHORT)				LER LOAD (SHORT)	CER COMPARE (SHORT)	AER ADD NORMALIZED (SHORT)	SER SUBTRACT NORMALIZED (SHORT)	MER MULTIPLY (SHORT)	DER DIVIDE (SHORT)	AUR ADD UNNORMALIZED (SHORT)	SUR SUBTRACT UNNORMALIZED (SHORT)
FIXED POINT HALFWORD AND BRANCHING	RX	4	STH STORE HALFWORD	LA LOAD ADDRESS	STC STORE CHARACTER	IC INSERT CHARACTER	EX EXECUTE	BAL BRANCH AND LINK	BCT BRANCH ON ACCOUNT	BC BRANCH ON CONDITION	LH LOAD HALFWORD	CH COMPARE HALFWORD	AH ADD HALFWORD	SH SUBTRACT HALFWORD	MH MULTIPLY HALFWORD		CVD CONVERT TO DECIMAL	CVB CONVERT TO BINARY
FIXED POINT FW AND LOGICAL	RX	5	ST STORE WORD				N AND	CL COMPARE LOGICAL	O OR	X EXCLUSIVE OR	L LOAD WORD	C COMPARE WORD	A ADD WORD	S SUBTRACT WORD	M MULTIPLY WORD	D DIVIDE	AL ADD LOGICAL	SL SUBTRACT LOGICAL
FLOATING POINT LONG	RX	6	STD STORE (LONG)								LD LOAD (LONG)	CD COMPARE (LONG)	AD ADD NORMALIZED (LONG)	SD SUBTRACT NORMALIZED (LONG)	MD MULTIPLY (LONG)	DD DIVIDE (LONG)	AW ADD UNNORMALIZED (LONG)	SW SUBTRACT UNNORMALIZED (LONG)
FLOATING POINT SHORT	RX	7	STE STORE (SHORT)								LE LOAD (SHORT)	CE COMPARE (SHORT)	AE ADD NORMALIZED (SHORT)	SE SUBTRACT NORMALIZED (SHORT)	ME MULTIPLY (SHORT)	DE DIVIDE (SHORT)	AU ADD UNNORMALIZED (SHORT)	SU SUBTRACT UNNORMALIZED (SHORT)
BRANCHING, STATUS SWITCHING AND SHIFTING	RS/SI	8	IDL IDLE		PC PROGRAM CONTROL	DIG DIAGNOSE	WRD WRITE DIRECT	RDD READ DIRECT	BXH BRANCH ON INDEX HIGH	BXLE BRANCH ON INDEX LOW OR EQUAL	SRL SHIFT RIGHT SINGLE LOGICAL	SLL SHIFT LEFT SINGLE LOGICAL	SRA SHIFT RIGHT SINGLE	SLA SHIFT LEFT SINGLE	SRDL SHIFT RIGHT DOUBLE LOGICAL	SLDL SHIFT LEFT DOUBLE LOGICAL	SRDA SHIFT RIGHT DOUBLE	SLDA SHIFT LEFT DOUBLE
LOGICAL AND I/O	RS/SI	9	STM STORE MULTIPLE	TM TEST UNDER MASK	MVI MOVE		NI AND	CLI COMPARE LOGICAL	OI OR	XI EXCLUSIVE OR	LM LOAD MULTIPLE				SDV START DEVICE	TDV TEST DEVICE	HDV HALT DEVICE	CKC CHECK CHANNEL
	RS/SI	A																
	RS/SI	B																
	SS	C																
LOGICAL	SS	D	SSP STORE SCRATCH-PAD	MVN MOVE NUMERICS	MVC MOVE	MVZ MOVE ZONES	NC AND	CLC COMPARE LOGICAL	OC OR	XC EXCLUSIVE OR	LSP LOAD SCRATCH-PAD				TR TRANSLATE	TRT TRANSLATE AND TEST	ED EDIT	EDMK EDIT AND MARK
	SS	E																
DECIMAL	SS	F		MVO MOVE WITH OFFSET	PACK PACK	UNPK UNPACK					ZAP ZERO AND ADD	CP COMPARE DECIMAL	AP ADD DECIMAL	SP SUBTRACT DECIMAL	MP MULTIPLY DECIMAL	DP DIVIDE DECIMAL		

INSTRUCTION FORMAT

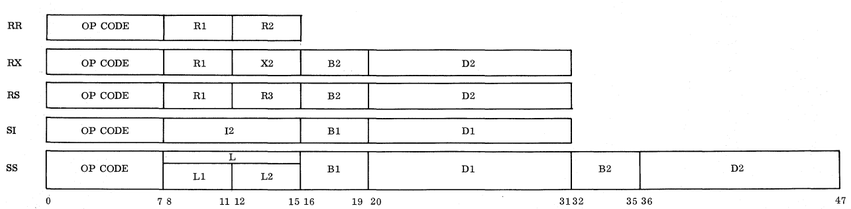


Table 11. Fast Memory Layout and Register Assignment

DIGI-SWITCH (DESIGNATION)	GANG SWITCH 7	6	5	4	3	2	1	0
F	7F UTILITY NO. 3	7E UTILITY NO. 2	7D ASSEMBLY STATUS REGISTER	7C CHANNEL COMMAND REGISTER I	7B CHANNEL COMMAND REGISTER II	7A CHANNEL ADDRESS REGISTER	79 PROCESSOR UTILITY NO. 19	78 PROCESSOR UTILITY NO. 18
	I/O CHANNEL REGISTERS - SELECTOR NO. 6							
E	77 FLOATING POINT REGISTER NO. 6	76	75 FLOATING POINT REGISTER NO. 4	74	73 FLOATING POINT REGISTER NO. 2	72	71 FLOATING POINT REGISTER NO. 0	70
D	6F GENERAL PURPOSE REGISTER NO. 15 P1	6E GENERAL PURPOSE REGISTER NO. 14 P1	6D GENERAL PURPOSE REGISTER NO. 13 P1	6C GENERAL PURPOSE REGISTER NO. 12 P1	6B GENERAL PURPOSE REGISTER NO. 11 P1	6A GENERAL PURPOSE REGISTER NO. 10 P1	69 GENERAL PURPOSE REGISTER NO. 9 P1	68 GENERAL PURPOSE REGISTER NO. 8 P1
C	67 GENERAL PURPOSE REGISTER NO. 7 P1	66 GENERAL PURPOSE REGISTER NO. 6 P1	65 GENERAL PURPOSE REGISTER NO. 5 P1	64 GENERAL PURPOSE REGISTER NO. 4 P1	63 GENERAL PURPOSE REGISTER NO. 3 P1	62 GENERAL PURPOSE REGISTER NO. 2 P1	61 GENERAL PURPOSE REGISTER NO. 1 P1	60 GENERAL PURPOSE REGISTER NO. 0 P1
B	5F UTILITY NO. 3	5E UTILITY NO. 2	5D ASSEMBLY STATUS REGISTER	5C CHANNEL COMMAND REGISTER I	5B CHANNEL COMMAND REGISTER II	5A CHANNEL ADDRESS REGISTER	59 PROCESSOR UTILITY NO. 17	58 PROCESSOR UTILITY NO. 16
	I/O CHANNEL REGISTERS - SELECTOR NO. 5							
A	57 UTILITY NO. 3	56 UTILITY NO. 2	55 ASSEMBLY STATUS REGISTER	54 CHANNEL COMMAND REGISTER I	53 CHANNEL COMMAND REGISTER II	52 CHANNEL ADDRESS REGISTER	51 PROCESSOR UTILITY NO. 15	50 PROCESSOR UTILITY NO. 14
	I/O CHANNEL REGISTERS - SELECTOR NO. 4							
9	4F GENERAL PURPOSE REGISTER NO. 15 P2	4E GENERAL PURPOSE REGISTER NO. 14 P2	4D GENERAL PURPOSE REGISTER NO. 13 P2	4C GENERAL PURPOSE REGISTER NO. 12 P2	4B GENERAL PURPOSE REGISTER NO. 11 P2	4A GENERAL PURPOSE REGISTER NO. 10 P2	49 GENERAL PURPOSE REGISTER NO. 9 P2	48 GENERAL PURPOSE REGISTER NO. 8 P2
8	47 GENERAL PURPOSE REGISTER NO. 7 P2	46 GENERAL PURPOSE REGISTER NO. 6 P2	45 GENERAL PURPOSE REGISTER NO. 5 P2	44 GENERAL PURPOSE REGISTER NO. 4 P2	43 GENERAL PURPOSE REGISTER NO. 3 P2	42 GENERAL PURPOSE REGISTER NO. 2 P2	41 GENERAL PURPOSE REGISTER NO. 1 P2	40 GENERAL PURPOSE REGISTER NO. 0 P2
7	3F UTILITY NO. 3	3E UTILITY NO. 2	3D ASSEMBLY STATUS REGISTER	3C CHANNEL COMMAND REGISTER I	3B CHANNEL COMMAND REGISTER II	3A CHANNEL ADDRESS REGISTER	39 PROCESSOR UTILITY NO. 13	38 PROCESSOR UTILITY NO. 12
	I/O CHANNEL REGISTERS - SELECTOR NO. 3							
6	37 UTILITY NO. 3	36 UTILITY NO. 2	35 ASSEMBLY STATUS REGISTER	34 CHANNEL COMMAND REGISTER I	33 CHANNEL COMMAND REGISTER II	32 CHANNEL ADDRESS REGISTER	31 PROCESSOR UTILITY NO. 11	30 PROCESSOR UTILITY NO. 10
	I/O CHANNEL REGISTERS - SELECTOR NO. 2							
5	2F GENERAL PURPOSE REGISTER NO. 15 (WEIGHT) P3	2E GENERAL PURPOSE REGISTER NO. 14 P3	2D GENERAL PURPOSE REGISTER NO. 13 P3	2C GENERAL PURPOSE REGISTER NO. 12 P3	2B GENERAL PURPOSE REGISTER NO. 11 P3	2A PROGRAM COUNTER P3	29 INTERRUPT STATUS REGISTER P3	28 INTERRUPT MASK REGISTER P3
4	27 GENERAL PURPOSE REGISTER NO. 7 P3	26 PROGRAM COUNTER P2	25 INTERRUPT STATUS REGISTER P2	24 INTERRUPT MASK REGISTER P2	23 INTERRUPT FLAG REGISTER	22 PROGRAM COUNTER P1	21 INTERRUPT STATUS REGISTER P1	20 INTERRUPT MASK REGISTER P1
3	1F UTILITY NO. 3	1E UTILITY NO. 2	1D ASSEMBLY STATUS REGISTER	1C CHANNEL COMMAND REGISTER I	1B CHANNEL COMMAND REGISTER II	1A CHANNEL ADDRESS REGISTER	19 PROCESSOR UTILITY NO. 9	18 PROCESSOR UTILITY NO. 8
	I/O CHANNEL REGISTERS - SELECTOR NO. 1							
2	17 UTILITY NO. 3	16 UTILITY NO. 2	15 STATUS REGISTER	14 CHANNEL COMMAND REGISTER I	13 CHANNEL COMMAND REGISTER II	12 CHANNEL ADDRESS REGISTER	11 UTILITY NO. 1	10 PROCESSOR UTILITY NO. 7
	I/O CHANNEL REGISTERS - MULTIPLEXOR							
1	0F GENERAL PURPOSE REGISTER NO. 15 (WEIGHT) P4	0E PROGRAM COUNTER P4	0D INTERRUPT STATUS REGISTER P4	0C INTERRUPT MASK REGISTER P4	0B GENERAL PURPOSE REGISTER NO. 11 P4	0A GENERAL PURPOSE REGISTER NO. 10 P4	09 GENERAL PURPOSE REGISTER NO. 9 P4	08 GENERAL PURPOSE REGISTER NO. 8 P4
0	07 BAD B ADDRESS REGISTER	06 AAD A ADDRESS REGISTER	05 PROCESSOR UTILITY NO. 6	04 PROCESSOR UTILITY NO. 5	03 PROCESSOR UTILITY NO. 4	02 PROCESSOR UTILITY NO. 3	01 PROCESSOR UTILITY NO. 2	00 PROCESSOR UTILITY NO. 1

NUMBER IN UPPER LEFT-HAND CORNER IS HEXADECIMAL ADDRESS

SPECIAL OPERATIONS (Cont'd)

Manual Initiation of I/O

◆ An I/O device may be initiated directly from the Maintenance Console by observing the following procedure:

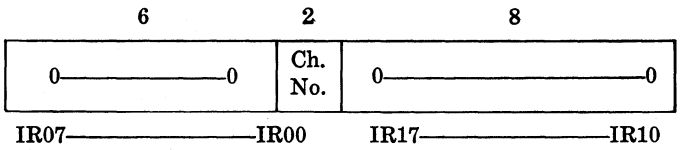
1. Set ICSP switch.
2. Set up Utility Registers 1, 2, 3 and 4 in the FM as indicated below.

Utility No.	Hex. Address	FM Switches: Digi-Switch	FM Switches: Gang Switch	Contents
1.	$(00)_{16}$	0	0	8 / 8 / 8 / 8 Device No. | 0——0 | 0——0 Unused | 0——0 DR07——DR00 DR17——DR10 DR27——DR20 DR37——DR30
2.	$(01)_{16}$	0	1	4 / 4 / 8 / 8 / 8 Key | 0——0 | 0——0 | 0——0 Unused | 0——0 DR07——DR00 DR17——DR10 DR27——DR20 DR37——DR30 Note 1.
3.	$(02)_{16}$	0	2	8 / 6 / 2 / 8 / 8 Command Code | 0——0 | Data Address of First Byte DR07——DR00 DR17——DR10 DR27——DR20 DR37——DR30
4.	$(03)_{16}$	0	3	5 / 3 / 8 / 8 / 8 Flags | 000 | 0——0 | Byte Count | Count DR07——DR00 DR17——DR10 DR27——DR20 DR27——DR30 Note 2.

Notes: 1. If the memory protect feature is not installed the key should be set equal to zero. If the memory protect feature is installed the proper key should be set. If an all zero key is set memory protection will not occur.

2. Byte count = 0 is the maximum count.

3. Press the GEN RES pushbutton.
4. Place $(9C)_{16}$ in the OR register.
5. Place the proper channel number in the IR register.



6. Push the ROMADD clear pushbutton. Set up $(3602)_8$ on the ROMADD pushbuttons.
7. Press the START pushbutton.

ROM Check

◆ A partial check of the ROM (Read Only Memory) can be made from the Maintenance Panel.

The ROM consists of two standard banks, one bank contains Elementary Operations (EO's) whose addresses are odd, and the other bank contains EO's whose addresses are even. There are two standard locations in each bank, one of which is wired with an all one pattern and the other is wired with an all zero pattern.

To check these locations proceed as follows:

1. Press the GEN RES pushbutton.
2. Press the SFSP pushbutton.
3. Press the ROMADD clear pushbutton.
4. Set the ROMADD pushbutton to the desired ROM address.
5. Press the START pushbutton.
6. Check the EO field pattern displayed on the Maintenance Panel. If the pattern displayed is incorrect, the machine is malfunctioning and service is necessary.

ROM Address	*Correct EO Field Pattern*
$(0113)_8$	All ones
$(0105)_8$	All zeros
$(2260)_8$	All ones
$(3250)_8$	All zeros

Note: When the above procedure is followed, the ROME indicator will light. This is a *normal* occurrence and should not be taken as an indication of an alarm condition.

The aforementioned procedure, selects and displays ROM EO pattern. If it is desired to continuously cycle on the EO; i.e., repeatedly address and read out of the ROM, the following steps should be taken:

a. Press the GEN RES pushbutton.
b. Press the FR (Function Repeat) pushbutton.
c. Press the ALI (Alarm Inhibit) pushbutton.
d. Press the ROMADD clear pushbutton.
e. Set the ROMADD pushbuttons to the desired ROM address.
f. Press the START pushbutton.
g. Check the EO field pattern displayed on the Maintenance Panel. If the pattern is incorrect the machine is malfunctioning and service should be requested.
h. To stop the machine press the SFSP pushbutton.

IMPORTANT

It is to be emphasized that the above must be considered as a partial check. Even though the previous checks are correct, it is still possible to have an incorrect EO pattern at some other ROM address.

Writing to Consecutive Main Memory Locations

◆ This procedure can be used to clear the Main Memory.

1. Press the GEN RES pushbutton.
2. Press the FR pushbutton.
3. Press the ROMADD clear pushbutton.
4. Set the ROMADD pushbutton to $(3451)_8$.
5. Set the initial starting address in FM location for AAD. The FM hexadecimal is 06 and the correct switch positions are 06.
6. Set the desired two bytes to be written in IR.
7. Press the START pushbutton. The memory will by cycled through consecutive locations, writing into each location the halfword stored in IR.
8. To stop the cycle, press the SFSP (Single Function Stop) pushbutton. To write one location continuously proceed as above, but before pressing START, press AMI (Address Modification Inhibit).

Reading from Consecutive Main Memory Locations

◆ This procedure can be used to check for and locate parity errors in Main Memory.

1. Press the GEN RES pushbutton.
2. Press the MESP (Machine Error Stop) pushbutton.
3. Press the FR (Function Repeat) pushbutton.
4. Press the ROMADD Clear pushbutton.
5. Set the ROMADD address pushbutton to $(1213)_8$.
6. Set the initial starting address in FM location for BAD. The FM hexadecimal address is 07 and the correct switch positions are 07.
7. Press the START pushbutton. The memory will be read from consecutive locations and the data put in the UR Register.

   Note: If a parity error is detected the machine will stop. If no error is detected the address will wrap around and it is then necessary to press the SFSP to stop the cycle.
8. To read one location continuously proceed as above, but before pressing START, press AMI (Address Modification Inhibit).

Writing to Consecutive Fast Memory Locations

◆ This procedure can be used to clear Fast Memory. Either a halfword or a full word can be written to FM. If a halfword is written, the halfword not written in a particular cycle is checked for correct parity. If one word is written per cycle, no parity check occurs.

1. Press the GEN RES pushbutton.
2. Press the FR (Function Repeat) pushbutton.
3. Press the ROMADD clear pushbutton.

If halfword operation:

4. Set the ROMADD pushbuttons to $(2704)_8$.

Writing to Consecutive Fast Memory Locations (Cont'd)

5. Set the initial starting address in the seven most significant bits of the G Register. The least significant bit of G Register determines which half of the FM word will be written to initially. If GO = 1, the 16 least significant bits of FM word will be written to initially. If GO = 0 the 16 most significant bits of the FM word will be written to initially.
6. Set the desired halfword to be written to IR.
7. Press the START pushbutton. The memory will be cycled through consecutive locations, writing into each halfword the data placed in IR.
8. To stop the cycle, press the SFSP (Single Function Stop) pushbutton.

If full-word operation:

4. Set the ROMADD pushbutton to $(2717)_8$.
5. Set the initial starting address in the seven most significant bits of the G Register.
6. Set the desired word in DR.
7. Press the START pushbutton. The memory will be cycled through consecutive locations, writing into each word the data placed in DR.
8. To stop the cycle, press the SFSP (Single Function Stop) pushbutton.

To write a halfword to one FM location continuously;

In step 4 of the halfword operation set ROMADD pushbutton to $(2706)_8$.

To write a full word to one FM location continuously;

In step 4 of the full word operation set ROMADD pushbuttons to $(3718)_8$.

Reading From Consecutive Fast Memory Locations

◆ This procedure can be used to check for and locate parity errors in Fast Memory.

1. Press the GEN RES pushbutton.
2. Press the MESP (Machine Error Stop) pushbutton.
3. Press the FR (Function Repeat) pushbutton.
4. Press the ROMADD clear pushbutton.
5. Set the ROMADD address pushbutton to $(2506)_8$.
6. Set the initial starting address in the seven most significant bits of the G Register.
7. Press the START pushbutton. The memory will be read from consecutive locations and the data put in UR.

   Note: If a parity error is detected the machine will stop. If no error is detected the address will wrap around and it is then necessary to depress SFSP to stop the cycle.

To read one location continuously, in step 5 above set the ROMADD pushbutton to $(2500)_8$.

EQUIPMENT CARE

General

◆ The equipment care schedule for the 70/45 Processor and 70/97 Operator's Console should not interfere with the operating schedule of the system or with its associated equipment. The schedule for cleaning and performing other routine maintenance procedures should be pre-determined for the operating shift. With a well planned schedule there will be a minimum of overlap between operating time and equipment care time.

Inspection

◆ It is recommended that a pre-operational inspection be conducted prior to placing the Processor into operation. Operators should be alert at all times to note any unusual condition or warning indications. Replacement of paper supply will depend upon how frequently it is used.

WARNING

WHEN PERFORMING ANY SERVICING PROCEDURES TO THE PROCESSOR AND/OR CONSOLE TYPEWRITER, REMOVE ELECTRICAL POWER TO AVOID POSSIBLE PERSONAL INJURY.

Filters

◆ The filters are housed in a tray assembly at the bottom of the platter frame. To remove proceed as follows: (See Figure 15.)

1. Unlock the slide fasteners located at each side of the tray assembly.
2. Pull the filter forward and remove from tray assembly.
3. Clean filter by washing through a mild soap detergent, rinse thoroughly and dry.

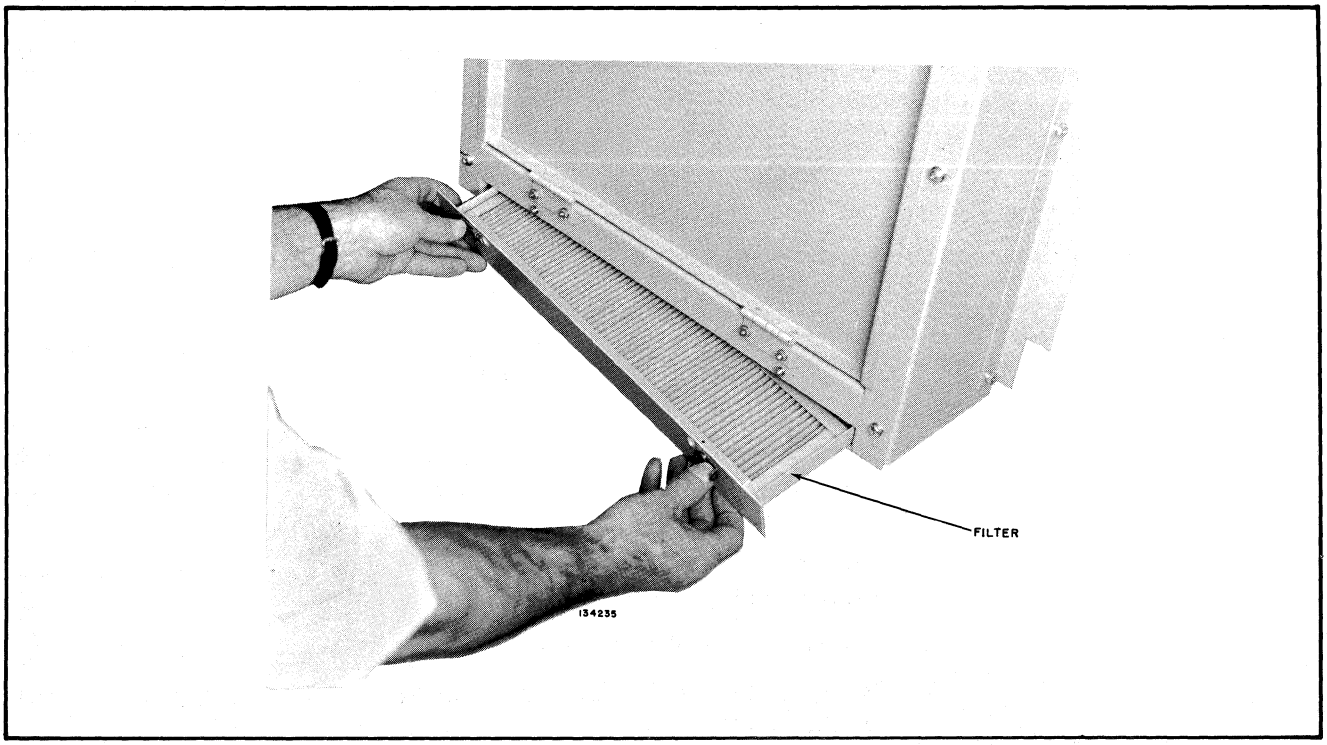


Figure 15. Removing Filters

Loading Paper

◆ To replenish the paper supply proceed as follows:

1. Raise the Top Cover.
2. Place the fan-fold (Form No. 8513 or equivalent) paper onto the rear shelf of the console. Position to align with typewriter sprocket feed mechanism.
3. Feed the paper through the slot in the rear of the cover. (Reference Figure 16.)
4. Push the release lever toward the rear to raise the paper retainer fingers off the platen.
5. Feed the paper under the platen and engage the first hole on each side of the paper with the sprocket pin protruding on each side of the lower front side of the platen.
6. Feed out approximately 3 inches of paper by pressing the LOC LF keylever if the typewriter has power applied, or by utilizing the manual platen knob if the typewriter does not have power applied.
7. Place the paper under the paper retainer fingers and push the fingers down against the platen.
8. Close the Top Cover and ensure that the paper is properly situated to enable it to move freely when typewriter is in operation.

Ribbon Replacement

◆ To install a new ribbon in the typewriter proceed as follows: (Reference Figure 17.)

1. Obtain access to the typewriter by raising the Top Cover.
2. Snap the spring latch which secures each spool in position, upward.
3. Raise the inked ribbon up over the roller and out of the ribbon reverse levers on both sides of the typing unit.
4. Remove the ribbon from the two ribbon guides on the type box carriage.
5. Lift both spools and the ribbon off the typing unit.
6. Unwind and disconnect the ribbon from one of the spools. Discard the other spool and the ribbon.
7. Connect the end of the new inked ribbon to the empty spool and wind on enough ribbon to cover the metal eyelet on the end of the ribbon.
8. Install both spools on their respective mechanisms. Rotate each spool slightly to ensure that each spool is properly engaged with the pin on the mechanism.
9. Slip the ribbon around each roller and into the ribbon reverse levers on both sides of the typing unit.
10. Position the ribbon in the two guides on the type box carriage.
11. Snap the two spring latches downward to secure the spools on their mechanisms.
12. Place the paper in the typing position and lower the cover.

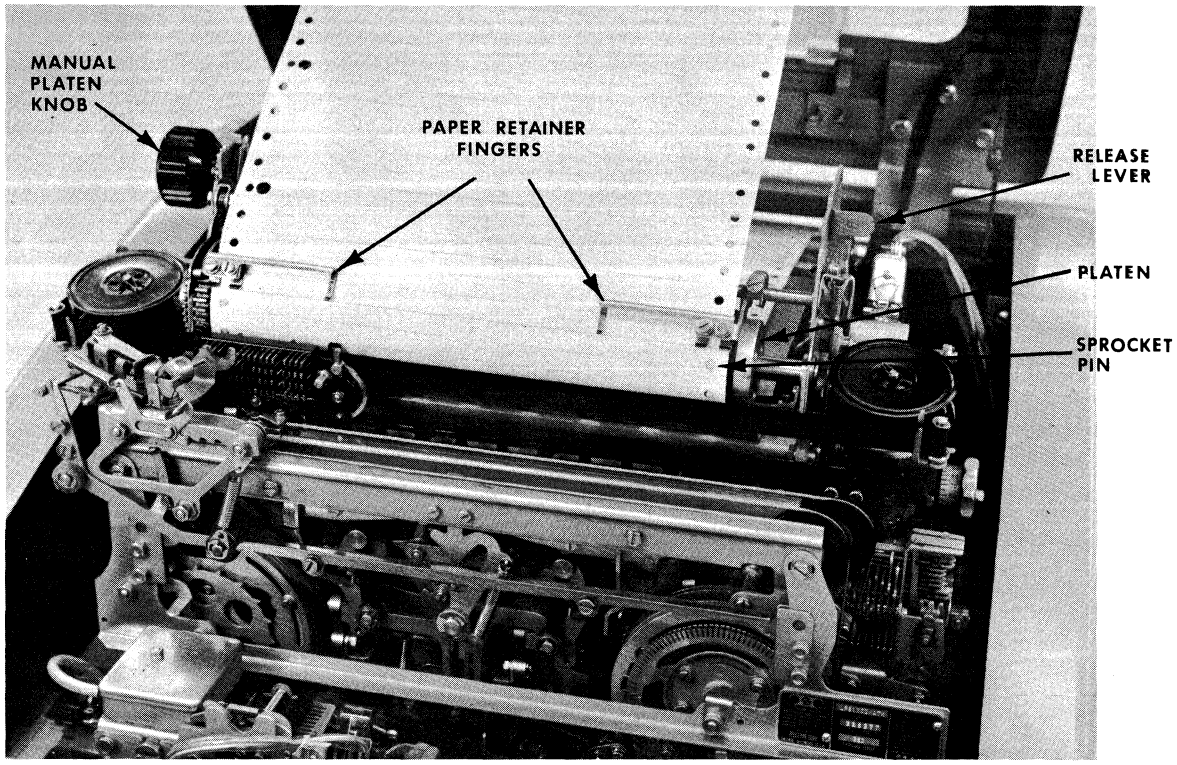


Figure 16. Loading Paper

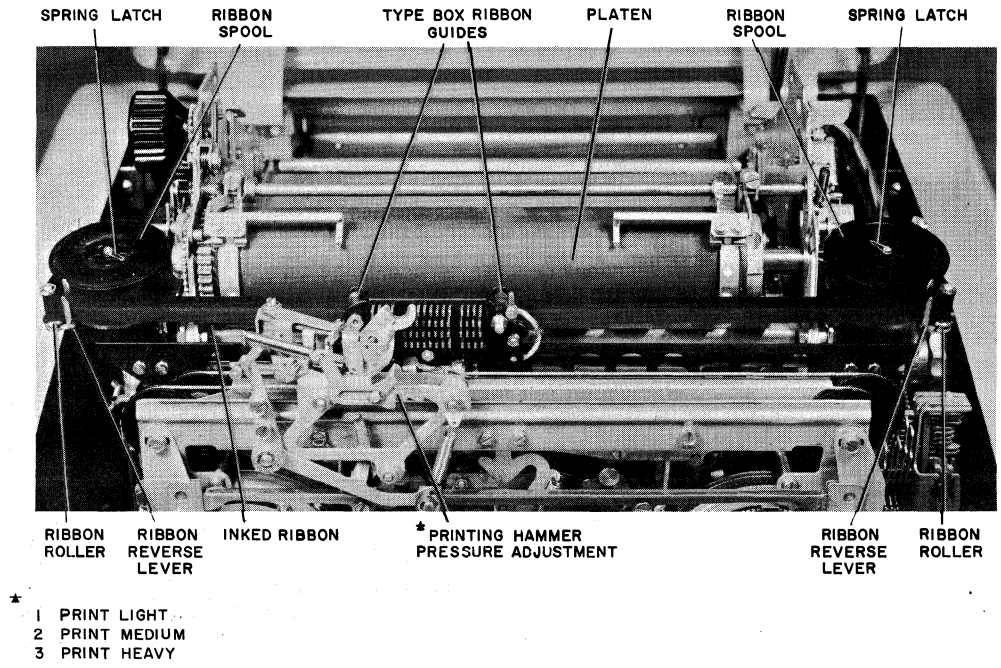


Figure 17. Ribbon Replacement

Lamp Replacement

DISPLAY INDICATOR LAMPS

◆ To replace defective indicator lamps (Figures 18 and 19) in either the Operator's Display Console or Maintenance Panel, proceed as follows:

1. Obtain access to the interior of the Maintenance Panel by opening the front hinged cover. Obtain access to the Operator's Display Panel by raising the cover upward and freeing it from its holding latches.
2. Using a Bulb Extractor tool, carefully grasp the envelope of the defective bulb and with moderate pressure remove bulb from its socket. (See Figure 20.)
3. Install a new light bulb (G. E. Type #334). Make certain bulb base is firmly fitted into its socket.
4. Perform lamp check test to assure that bulbs are indicating properly.

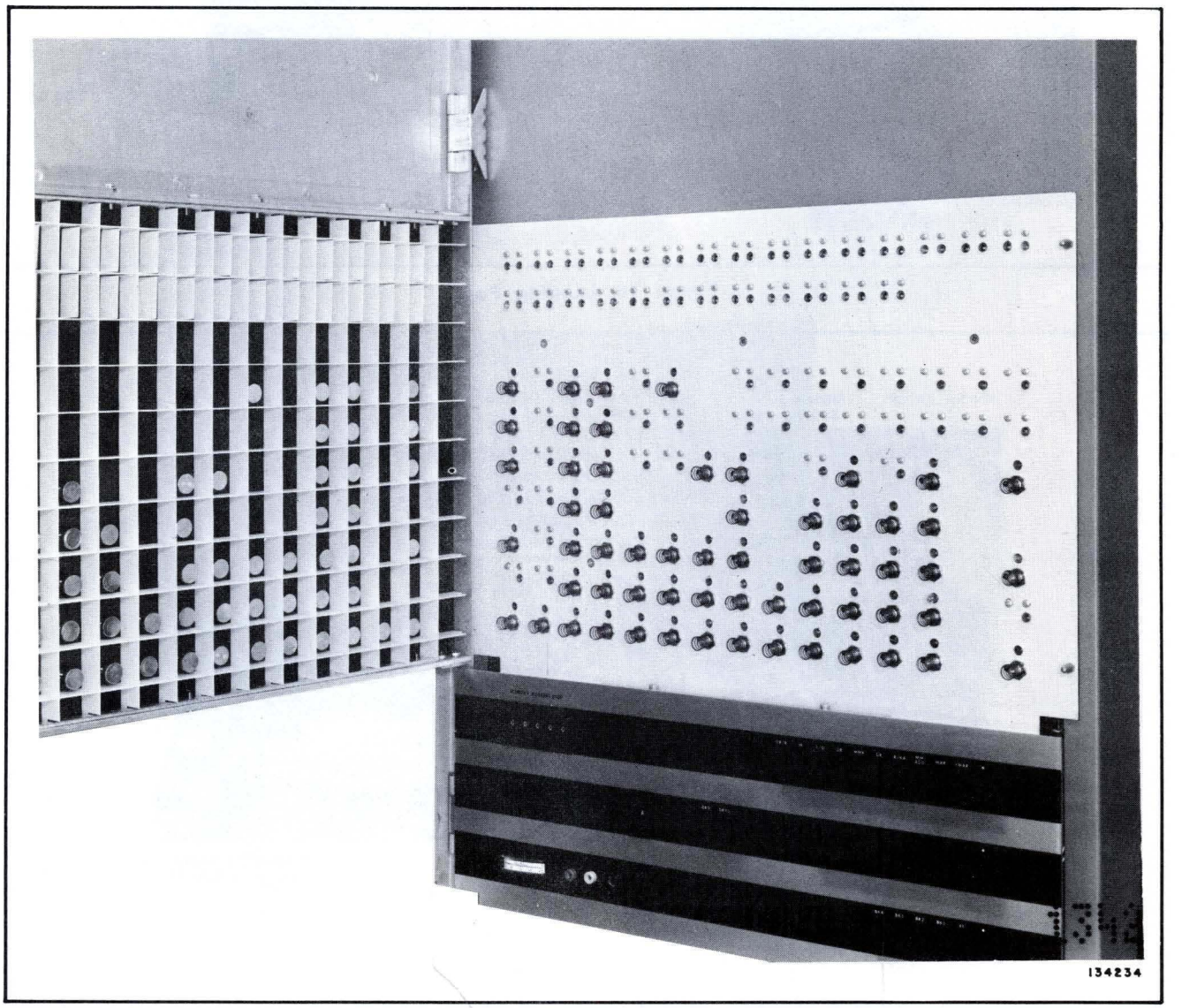


Figure 18. Interior View of 70/45 Processor Maintenance Panel

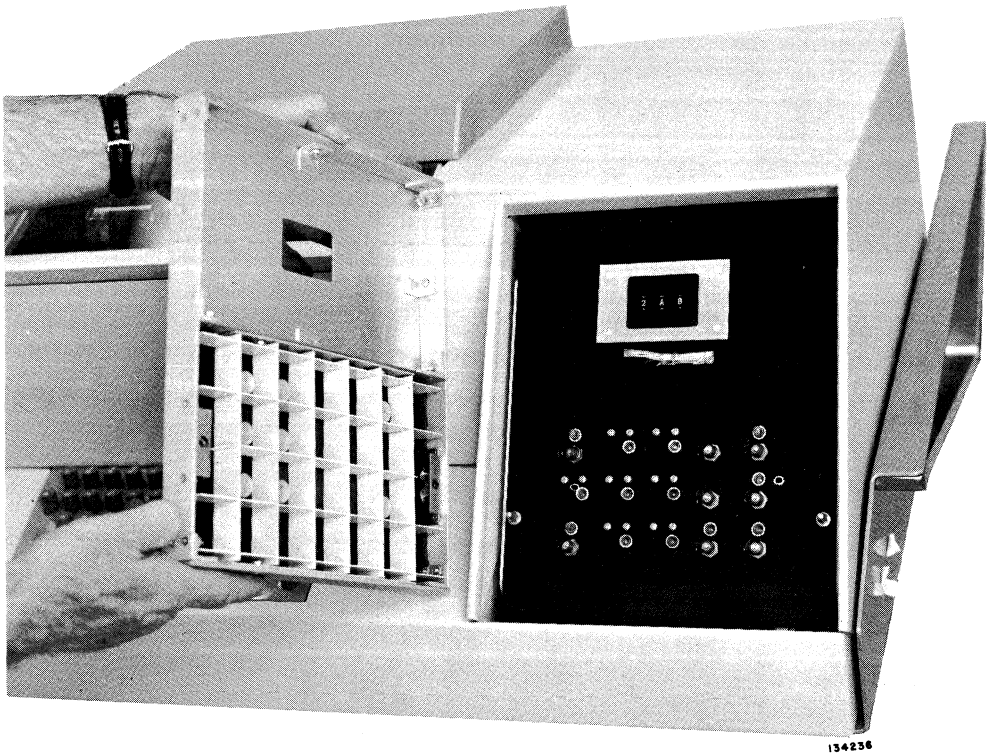


Figure 19. Removal of Operator's Display Panel Cover

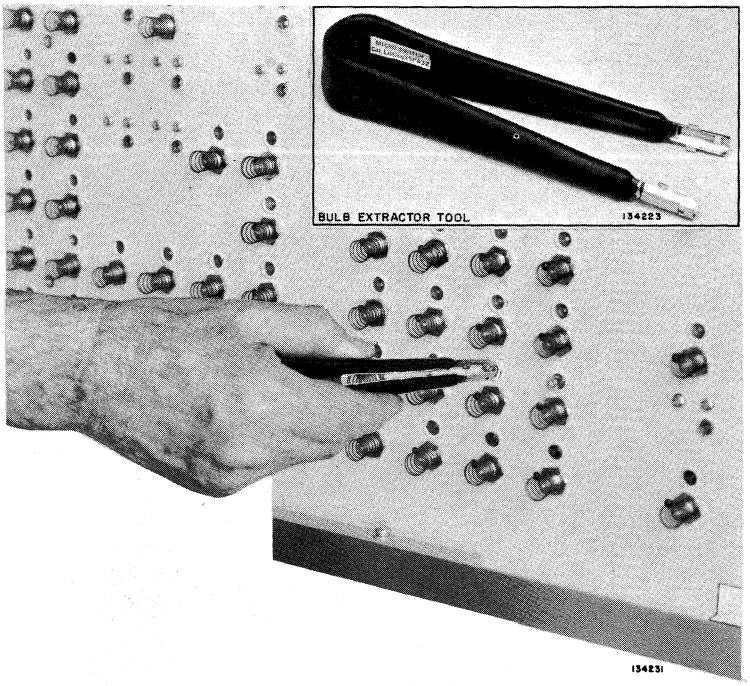


Figure 20. Light Bulb Replacement

TYPEWRITER LIGHT

◆ To replace the lamp bulb located under the Top Cover of the Operator's Console proceed as follows:

1. Raise the entire Top Cover of the Operator's Console.
2. Remove the defective lamp by pushing and turning it counter-clockwise until the lamp is released from the bayonette type socket. (See Figure 21.)
3. Insert new lamp (G. E. 1314X) into the socket with the lamp pins coinciding with the slot in the bayonette socket. Twist the lamp in a clockwise direction until it is locked into place.
4. Lower Top Cover.

Fuse Replacement

◆ The Operator's Console is equipped with two tubular glass fuses which are accessible when the top cover of the Console is raised. (See Figure 22.)

CAUTION

Never attempt to replace a fuse with the power on. Whenever a fuse is being replaced make certain that the power switch is in its OFF position.

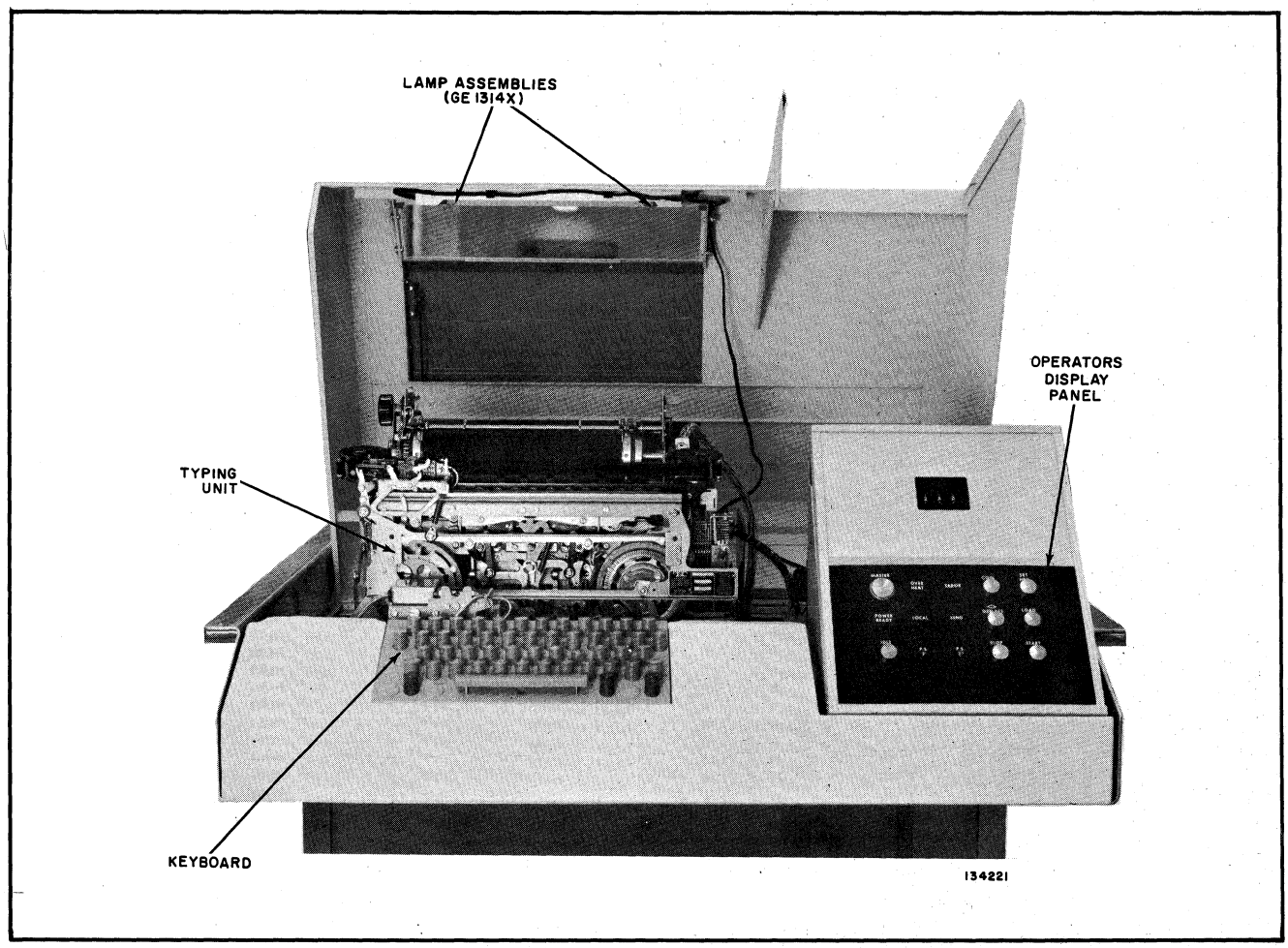


Figure 21. 70/97 Operator Console (Top Cover Ass'y Raised)

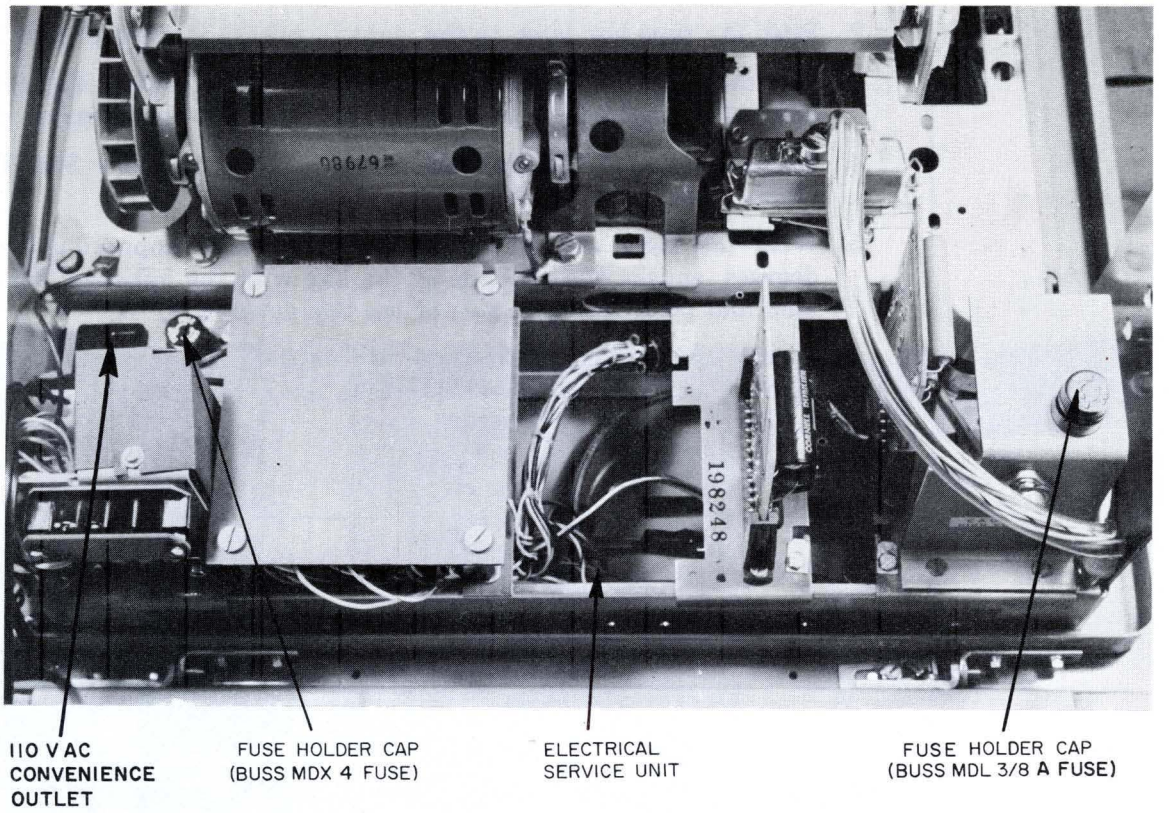


Figure 22. Fuse Locations (Rear View of the Electrical Unit)

Fuse Replacement (Cont'd)

To replace a fuse proceed as follows:

1. Raise the Top Cover.
2. Determine which of the two fuses has blown by the following:
   a. The MDL ⅜ ampere fuse when blown, will remove the current from the signal line and will be evidenced by excessive chattering in the typing unit.
   b. The MDX 4 ampere fuse, when blown, will remove all electrical power from the typewriter.
3. Turn the fuse holder cap counter-clockwise and lift the cap with the attached fuse from the fuse holder.
4. Slide the defective fuse out of the cap.
5. Install a new fuse into the cap.
6. Insert the cap and fuse into the fuse holder, ensuring the slot in the fuse holder and the catch on the cap are aligned.
7. Push the cap downward and turn it clockwise to secure it in position.
8. Place power switch to its ON position.

   Note: If the replaced fuse blows the first time power is applied or shortly thereafter, call the Customer Service Representative.

Cleaning the Type Pallets

◆ To remove and clean the type pallets proceed as follows:

1. Raise the Top Cover.
2. Push the type box latch to the right to release it. (See Figure 23.)
3. Lift the right side of the type box up to approximately 45 degrees and pull to the right to disengage it from the left-hand bearing stud.
4. Clean the face of the type pallets using Eberhard Faber Star Type Cleaner No. 1226.
5. With the right side of the type box elevated approximately 45 degrees, engage the left side of the box with the left-hand bearing stud and push the right side of the box downward.
6. Ensure that the box is firmly seated on the bearing stud. Place the point of the latch in the notch on the box and raise the latch to the left in its locked position.
7. Lower the Top Cover.

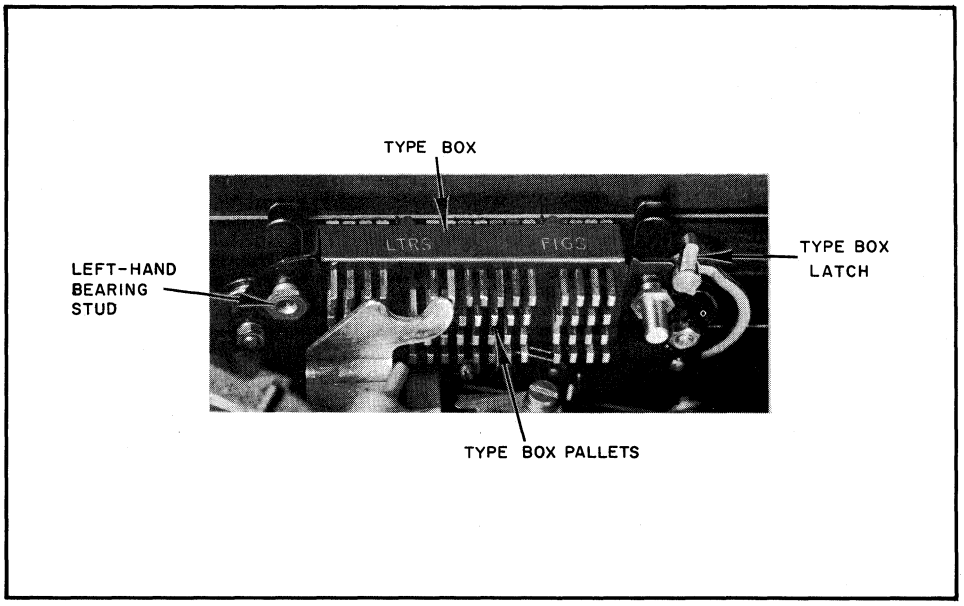


Figure 23. Removal of the Type Box

Cleaning the Platen

◆ To clean the typewriter platen proceed as follows:

1. Raise the Top Cover.
2. Using the manual platen knob, back the paper completely out of contact with the platen.
3. Using a clean lint-free cloth and an approved cleaning agent, clean the entire rubber portion of the platen.
4. Wipe the platen with a dry, clean, lint-free cloth.
5. Install the paper in the typewriter (refer to LOADING PAPER).
6. Close the Top Cover.

GLOSSARY

A Rack ◆ The left side of the Processor as viewed from the front.

AC ◆ Alternating current as provided by the building power source; used by the Processor Power Supply to generate dc voltage.

Address ◆ A numerical configuration used to reference a byte location in memory.

Alternate Action Pushbutton Switch ◆ A switch having two conditions or states.

B Rack ◆ The right side of the Processor as viewed from the front.

Binary ◆ A numbering system founded on the base two.

Bit ◆ A unit notation, represented by zero or one, indicating the exponential power in the binary system by virtue of its position with respect to zero (reading from right to left).

BPU ◆ The Basic Processing Unit (excluding Memory, Power Supply, and peripheral devices) responsible for all data handling, data processing, decision, and control functions.

Branching ◆ Causing an instruction sequence to be altered by transferring to another portion of the program if a preassigned condition is sensed.

Busy ◆ A signal used internally to indicate that a particular device, Control Electronics (CE), or function is presently engaged in a previously initiated operation.

Byte ◆ A group of binary digits usually operated on as a unit.

Character ◆ One of a set of digits or letters that may be combined to express information. A group of characters in one configuration may be considered as a single character in another configuration.

Code ◆ A system of symbols and the rules for their use in representing information.

Command ◆ An electronic signal, generated as the result of an instruction (such as read, write, etc.), that causes an input/output device to respond.

Console ◆ The main control center, accessible to the operator, of the Processor.

Core ◆ A single magnetic unit, capable of storing one bit of a byte storage location in memory. Information is represented by polarizing the core.

C.S.R. ◆ Customer Service Representative.

Cycle ◆ A Processor electronic cycle; the time required to decode and execute one phase of an operation. In the 70/45 1.44 microseconds duration.

Data ◆ The basic information entered into the system for processing.

DC ◆ Direct current as transformed by the Processors Power Supply; used by the Processor electronics.

Display ◆ The contents of selected registers represented on the console by a series of indicators. A lit indicator implies the presence of a "one" bit.

Elementary Operations (EO's) ◆ Fixed microprogramming instructions which control basic computer operations. Instruction execution is accomplished by executing a sequence of EO's.

Emulator ◆ An optional memory storage feature which when employed with the 70/45 Processor will provide the means for the direct execution of most programs written for the specific optional emulator feature selected. The added storage contains microprograms which cause the Processor to decode and execute instructions, through the EO facilities of the 70/45 Processor.

Error Recovery ◆ The method or methods utilized to continue (or restart if necessary) a program when a mechanical or electronic malfunction has occurred.

Execute ◆ Perform the operation as specified by the OP code of an instruction.

Fast Memory ◆ A fast micromagnetic storage device containing the General Purpose, Floating Point, and various other registers to facilitate processor and program control. (Refer to Table 11.) A small, very fast memory (relative to the processor's main memory) used to replace registers for the storage of data. (Also referred to as Scratch Pad.

Flip-Flop ◆ A device, sometimes called a trigger having two stable states termed ON and OFF, 0 and 1, set and reset, etc.

GEN RES ◆ A manually generated signal used to reset certain registers and parity indicators in the Processor.

Halt ◆ An orderly ending to processing activity upon completion of an instruction or program.

Hardware ◆ The individual components, such as electrical and mechanical parts that comprise Computers, Readers, Printers and Tape Units, from which a Computer system is developed.

Hexadecimal ◆ A numbering system founded on the base sixteen.

HSM ◆ High Speed Memory.

Illegal ◆ Referring to an instruction or operation which is not part of the 70/45 repertoire.

Initialize ◆ To set a condition, routine, or word to its original (or beginning) state.

Interrupt ◆ A temporary interruption of normal processing, resulting from the occurrence of unique conditions, and requiring special handling peculiar to those conditions.

Indicator ◆ A light, located on Maintenance Console Panel (Maintenance/Auxiliary Panels), Operator's Display Panel or Power Supply Control Panel, etc., that is lit to indicate a particular condition occurring in the Processor, typewriter or Power Supply.

Initiate ◆ To start.

Input ◆ Information taken from an external or secondary device into the internal storage of the Processor.

I/O Device ◆ An I/O device (input/output) is used to transmit data to or receive data from the Processor or secondary device. A Card Reader, Typewriter, or Paper Tape Unit is considered an I/O device.

Instruction ◆ A set of characters or symbols that are used to define an operation.

Item/Field ◆ An item/field consists of any number of bytes that specify a particular unit of information (numeric field, alphabetic name, street address, stock number, etc.).

Load ◆ The operation of transferring data from an input device into storage.

Location ◆ A unit storage (byte) position in high-speed memory. (HSM)

Mode ◆ A logical arrangement of internal components provided to accommodate or process particular operations: a method of operation. The Processing State (P1) and the Interrupt State (P2) are two such modes.

Momentary Contact Pushbutton Switch ◆ A switch having one stable state.

MAR ◆ Memory Address Register

MPE ◆ Memory Parity Error

Non-addressable Memory ◆ That portion of the main memory of a processor which is reserved for input/output data; thus it is not available to the programmer. (Also referred to as "shaded memory.")

Operable ◆ Meaning that an input/output is in a state of readiness that will permit it to respond to an instruction calling for a specific acion referenced to that device.

Operator ◆ The person who actually manipulates the Processor/Console controls, places information media into the input devices, removes the output, presses the START button, etc.

Output ◆ Information transferred from a Processor to an external storage unit, or to an external device.

Panel ◆ A section of a console containing controls, indicator lights, etc., arranged in ordered groupings of allied functions, such as the Operator's Display panel and the Maintenance Console panel.

Parity ◆ A scheme of checking "correctness" of a binary digit where the total number of ones must always be odd (odd parity) or even (even parity) depending on the requirements for the particular device or system.

Peripheral ◆ Referring to equipment, such as Typewriters, Paper Tape Devices, etc., that are sub-units of a computer system but are physically located external of the main Processor cabinet.

Processing State ◆ The normal mode of operation of the Processor in which the main program is executed.

Processor ◆ The central processing unit containing the main storage device (memory), power supply, and necessary electronics to perform all the logical processing and modifications of data of a Computer system.

Program ◆ A sequence of step-by-step operations which are to be performed by the Processor in order to solve a problem, modify or rearrange data.

Pushbutton ◆ A switch activated by depression.

Pushbutton Indicator ◆ A light, associated with a given pushbutton, which will be turned on when the function of that pushbutton is invoked.

Read Only Memory (ROM) ◆ A memory for storing fixed, or invariant data. The reading operation is nondestructive of the data.

Record ◆ The data contained between two identifying symbols such as: record gaps, storage marks, column 0 and column 80, etc.

RDM ◆ Read Memory

Reset ◆ To return Computer components to a specified initial or static state.

Set ◆ To force a storage device or indicator to a prescribed state.

Self-Terminating ◆ An I/O device which will effect an orderly halt upon recognition of a gap on tape, column 80 on cards, etc.

Sub routine ◆ A segment of a program usually stored apart from the main program and entered into and out by a branch instruction.

Transfer ◆ Cause data to be moved from one storage area or device to another.

Write ◆ (1) Transmit data from memory storage to an input device (e.g., write to tape, write to punch, etc.).

(2) Enter data into memory storage (e.g., write to memory).

WRM ◆ Write to Memory. Enter data into memory storage.

APPENDIX A

EXTENDED BINARY-CODED-DECIMAL INTERCHANGE CODE (EBCDIC)

4567 →

HEX	→	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
↓	0123	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0	0000	NUL				PF	HT	LC	DEL								
1	0001					RES	NL	BS	IL								
2	0010					BYP	LF	EOB	PRE			SM					
3	0011					PN	RS	UC	EOT								
4	0100	SPACE										¢	.	<	(	+	|
5	0101	&										!	$	*	)	;	¬
6	0110	–	/									^	,	%	_	>	?
7	0111											:	#	@	'	=	"
8	1000		a	b	c	d	e	f	g	h	i						
9	1001		j	k	l	m	n	o	p	q	r						
A	1010			s	t	u	v	w	x	y	z						
B	1011																
C	1100		A	B	C	D	E	F	G	H	I						
D	1101		J	K	L	M	N	O	P	Q	R						
E	1110			S	T	U	V	W	X	Y	Z						
F	1111	0	1	2	3	4	5	6	7	8	9						¤

Bit Positions: 0 1 2 3 4 5 6 7

Significance: 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0

Control Characters:

NUL — All Zero-Bits
PF — Punch Off
HT — Horizontal Tab
LC — Lower Case
DEL — Delete
RES — Restore
NL — New Line
BS — Backspace
IL — Idle
BYP — Bypass
LF — Line Feed
EOB — End of Block
PRE — Prefix
SM — Set Mode
PN — Punch On
RS — Reader Stop
UC — Upper Case
EOT — End of Transmission

APPENDIX B

AMERICAN STANDARD CODE FOR INFORMATION INTERCHANGE

(ASCII) (EXTENDED TO 8 BITS)

4321 →

HEX	→	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
↓	76X5	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0	0000	NUL	SOH	STX	ETX	EOT	ENQ	ACK	BEL	BS	HT	LF	VT	FF	CR	SO	SI
1	0001	DLE	DC1	DC2	DC3	DC4	NAK	SYN	ETB	CAN	EM	SS	ESC	FS	GS	RS	US
2	0010																
3	0011																
4	0100	SP	!	"	#	$	%	&	'	(	)	*	+	,	−	.	/
5	0101	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
6	0110																
7	0111																
8	1000																
9	1001																
A	1010	`	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
B	1011	P	Q	R	S	T	U	V	W	X	Y	Z	[	~	]	^	_
C	1100																
D	1101																
E	1110	@	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
F	1111	p	q	r	s	t	u	v	w	x	y	z	{	¬	}	|	DEL

Bit Positions: 7 6 X 5 4 3 2 1

Significance: 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0

Control Characters:

NUL — Null
SOH — Start of Heading (CC)
STX — Start of Text (CC)
ETX — End of Text (CC)
EOT — End of Transmission (CC)
ENQ — Enquiry (CC)
ACK — Acknowledge (CC)
BEL — Bell (audible or attention signal)
BS — Backspace (FE)
HT — Horizontal Tabulation (punch card skip) (FE)
LF — Line Feed (FE)
VT — Vertical Tabulation (FE)
FF — Form Feed (FE)
CR — Carriage Return (FE)
SO — Shift Out
SI — Shift In
DLE — Data Link Escape (CC)
DC1 — Device Control 1
DC2 — Device Control 2
DC3 — Device Control 3
DC4 — Device Control 4 (stop)
NAK — Negative Acknowledge (CC)
SYN — Synchronous Idle (CC)
ETB — End of Transmission Block (CC)
CAN — Cancel
EM — End of Medium
SS — Start of Special Sequence
ESC — Escape
FS — File Separator (IS)
GS — Group Separator (IS)
RS — Record Separator (IS)
US — Unit Separator (IS)
DEL — Delete
SP — Space (normally non-printing)
(CC) — Communication Control
(FE) — Format Effector
(IS) — Information Separator

APPENDIX C
CHARACTER CODES

Decimal	Hexadecimal	EBCDIC	Character Set Punch Combination	Printer Graphics
0	00	0000 0000	12,0,9,8,1	
1	01	0000 0001	12,9,1	
2	02	0000 0010	12,9,2	
3	03	0000 0011	12,9,3	
4	04	0000 0100	12,9,4	
5	05	0000 0101	12,9,5	
6	06	0000 0110	12,9,6	
7	07	0000 0111	12,9,7	
8	08	0000 1000	12,9,8	
9	09	0000 1001	12,9,8,1	
10	0A	0000 1010	12,9,8,2	
11	0B	0000 1011	12,9,8,3	
12	0C	0000 1100	12,9,8,4	
13	0D	0000 1101	12,9,8,5	
14	0E	0000 1110	12,9,8,6	
15	0F	0000 1111	12,9,8,7	
16	10	0001 0000	12,11,9,8,1	
17	11	0001 0001	11,9,1	
18	12	0001 0010	11,9,2	
19	13	0001 0011	11,9,3	
20	14	0001 0100	11,9,4	
21	15	0001 0101	11,9,5	
22	16	0001 0110	11,9,6	
23	17	0001 0111	11,9,7	
24	18	0001 1000	11,9,8	
25	19	0001 1001	11,9,8,1	
26	1A	0001 1010	11,9,8,2	
27	1B	0001 1011	11,9,8,3	
28	1C	0001 1100	11,9,8,4	
29	1D	0001 1101	11,9,8,5	
30	1E	0001 1110	11,9,8,6	
31	1F	0001 1111	11,9,8,7	
32	20	0010 0000	11,0,9,8,1	
33	21	0010 0001	0,9,1	
34	22	0010 0010	0,9,2	
35	23	0010 0011	0,9,3	
36	24	0010 0100	0,9,4	
37	25	0010 0101	0,9,5	
38	26	0010 0110	0,9,6	
39	27	0010 0111	0,9,7	
40	28	0010 1000	0,9,8	
41	29	0010 1001	0,9,8,1	
42	2A	0010 1010	0,9,8,2	
43	2B	0010 1011	0,9,8,3	
44	2C	0010 1100	0,9,8,4	
45	2D	0010 1101	0,9,8,5	
46	2E	0010 1110	0,9,8,6	
47	2F	0010 1111	0,9,8,7	
48	30	0011 0000	12,11,0,9,8,1	
49	31	0011 0001	9,1	
50	32	0011 0010	9,2	
51	33	0011 0011	9,3	
52	34	0011 0100	9,4	
53	35	0011 0101	9,5	
54	36	0011 0110	9,6	

APPENDIX C
CHARACTER CODES (Continued)

Decimal	Hexadecimal	EBCDIC	Character Set Punch Combination	Printer Graphics
55	37	0011 0111	9,7	
56	38	0011 1000	9,8	
57	39	0011 1001	9,8,1	
58	3A	0011 1010	9,8,2	
59	3B	0011 1011	9,8,3	
60	3C	0011 1100	9,8,4	
61	3D	0011 1101	9,8,5	
62	3E	0011 1110	9,8,6	
63	3F	0011 1111	9,8,7	
64	40	0100 0000		Space
65	41	0100 0001	12,0,9,1	
66	42	0100 0010	12,0,9,2	
67	43	0100 0011	12,0,9,3	
68	44	0100 0100	12,0,9,4	
69	45	0100 0101	12,0,9,5	
70	46	0100 0110	12,0,9,6	
71	47	0100 0111	12,0,9,7	
72	48	0100 1000	12,0,9,8	
73	49	0100 1001	12,8,1	
74	4A	0100 1010	12,8,2	¢ (cents)
75	4B	0100 1011	12,8,3	. (period)
76	4C	0100 1100	12,8,4	< (Less than)
77	4D	0100 1101	12,8,5	((open parenthesis)
78	4E	0100 1110	12,8,6	+ (plus)
79	4F	0100 1111	12,8,7	| (vertical)
80	50	0101 0000	12	& (ampersand)
81	51	0101 0001	12,11,9,1	
82	52	0101 0010	12,11,9,2	
83	53	0101 0011	12,11,9,3	
84	54	0101 0100	12,11,9,4	
85	55	0101 0101	12,11,9,5	
86	56	0101 0110	12,11,9,6	
87	57	0101 0111	12,11,9,7	
88	58	0101 1000	12,11,9,8	
89	59	0101 1001	11,8,1	
90	5A	0101 1010	11,8,2	! (exclamation)
91	5B	0101 1011	11,8,3	$ (dollar sign)
92	5C	0101 1100	11,8,4	* (asterisk)
93	5D	0101 1101	11,8,5	) (close parenthesis)
94	5E	0101 1110	11,8,6	; (semicolon)
95	5F	0101 1111	11,8,7	¬ (logical NOT)
96	60	0110 0000	11	— (minus)
97	61	0110 0001	0,1	/ (slash)
98	62	0110 0010	11,0,9,2	
99	63	0110 0011	11,0,9,3	
100	64	0110 0100	11,0,9,4	
101	65	0110 0101	11,0,9,5	
102	66	0110 0110	11,0,9,6	
103	67	0110 0111	11,0,9,7	
104	68	0110 1000	11,0,9,8	
105	69	0110 1001	0,8,1	
106	6A	0110 1010	12,11	∧ (logical AND)
107	6B	0110 1011	0,8,3	, (comma)
108	6C	0110 1100	0,8,4	% (percent)
109	6D	0110 1101	0,8,5	_ (underline)

APPENDIX C
CHARACTER CODES (Continued)

Decimal	Hexadecimal	EBCDIC*	Character Set Punch Combination	Printer Graphics
110	6E	0110 1110	0,8,6	> (greater than)
111	6F	0110 1111	0,8,7	? (question mark)
112	70	0111 0000	12,11,0	
113	71	0111 0001	12,11,0,9,1	
114	72	0111 0010	12,11,0,9,2	
115	73	0111 0011	12,11,0,9,3	
116	74	0111 0100	12,11,0,9,4	
117	75	0111 0101	12,11,0,9,5	
118	76	0111 0110	12,11,0,9,6	
119	77	0111 0111	12,11,0,9,7	
120	78	0111 1000	12,11,0,9,8	
121	79	0111 1001	8,1	
122	7A	0111 1010	8,2	: (colon)
123	7B	0111 1011	8,3	# (number sign)
124	7C	0111 1100	8,4	@ (at the rate of)
125	7D	0111 1101	8,5	' (apostrophe)
126	7E	0111 1110	8,6	= (equals)
127	7F	0111 1111	8,7	" (quote)
128	80	1000 0000	12,0,8,1	
129	81	1000 0001	12,0,1	
130	82	1000 0010	12,0,2	
131	83	1000 0011	12,0,3	
132	84	1000 0100	12,0,4	
133	85	1000 0101	12,0,5	
134	86	1000 0110	12,0,6	
135	87	1000 0111	12,0,7	
136	88	1000 1000	12,0,8	
137	89	1000 1001	12,0,9	
138	8A	1000 1010	12,0,8,2	
139	8B	1000 1011	12,0,8,3	
140	8C	1000 1100	12,0,8,4	
141	8D	1000 1101	12,0,8,5	
142	8E	1000 1110	12,0,8,6	
143	8F	1000 1111	12,0,8,7	
144	90	1001 0000	12,11,8,1	
145	91	1001 0001	12,11,1	
146	92	1001 0010	12,11,2	
147	93	1001 0011	12,11,3	
148	94	1001 0100	12,11,4	
149	95	1001 0101	12,11,5	
150	96	1001 0110	12,11,6	
151	97	1001 0111	12,11,7	
152	98	1001 1000	12,11,8	
153	99	1001 1001	12,11,9	
154	9A	1001 1010	12,11,8,2	
155	9B	1001 1011	12,11,8,3	
156	9C	1001 1100	12,11,8,4	
157	9D	1001 1101	12,11,8,5	
158	9E	1001 1110	12,11,8,6	
159	9F	1001 1111	12,11,8,7	
160	A0	1010 0000	11,0,8,1	
161	A1	1010 0001	11,0,1	
162	A2	1010 0010	11,0,2	
163	A3	1010 0011	11,0,3	
164	A4	1010 0100	11,0,4	

APPENDIX C
CHARACTER CODES (Continued)

Decimal	Hexadecimal	EBCDIC	Character Set Punch Combination	Printer Graphics
165	A5	1010 0101	11,0,5	
166	A6	1010 0110	11,0,6	
167	A7	1010 0111	11,0,7	
168	A8	1010 1000	11,0,8	
169	A9	1010 1001	11,0,9	
170	AA	1010 1010	11,0,8,2	
171	AB	1010 1011	11,0,8,3	
172	AC	1010 1100	11,0,8,4	
173	AD	1010 1101	11,0,8,5	
174	AE	1010 1110	11,0,8,6	
175	AF	1010 1111	11,0,8,7	
176	B0	1011 0000	12,11,0,8,1	
177	B1	1011 0001	12,11,0,1	
178	B2	1011 0010	12,11,0,2	
179	B3	1011 0011	12,11,0,3	
180	B4	1011 0100	12,11,0,4	
181	B5	1011 0101	12,11,0,5	
182	B6	1011 0110	12,11,0,6	
183	B7	1011 0111	12,11,0,7	
184	B8	1011 1000	12,11,0,8	
185	B9	1011 1001	12,11,0,9	
186	BA	1011 1010	12,11,0,8,2	
187	BB	1011 1011	12,11,0,8,3	
188	BC	1011 1100	12,11,0,8,4	
189	BD	1011 1101	12,11,0,8,5	
190	BE	1011 1110	12,11,0,8,6	
191	BF	1011 1111	12,11,0,8,7	
192	C0	1100 0000	12,0	
193	C1	1100 0001	12,1	A
194	C2	1100 0010	12,2	B
195	C3	1100 0011	12,3	C
196	C4	1100 0100	12,4	D
197	C5	1100 0101	12,5	E
198	C6	1100 0110	12,6	F
199	C7	1100 0111	12,7	G
200	C8	1100 1000	12,8	H
201	C9	1100 1001	12,9	I
202	CA	1100 1010	12,0,9,8,2	
203	CB	1100 1011	12,0,9,8,3	
204	CC	1100 1100	12,0,9,8,4	
205	CD	1100 1101	12,0,9,8,5	
206	CE	1100 1110	12,0,9,8,6	
207	CF	1100 1111	12,0,9,8,7	
208	D0	1101 0000	11,0	
209	D1	1101 0001	11,1	J
210	D2	1101 0010	11,2	K
211	D3	1101 0011	11,3	L
212	D4	1101 0100	11,4	M
213	D5	1101 0101	11,5	N
214	D6	1101 0110	11,6	O
215	D7	1101 0111	11,7	P
216	D8	1101 1000	11,8	Q
217	D9	1101 1001	11,9	R
218	DA	1101 1010	12,11,9,8,2	
219	DB	1101 1011	12,11,9,8,3	

APPENDIX C
CHARACTER CODES (Continued)

Decimal	Hexadecimal	EBCDIC	Character Set Punch Combination	Printer Graphics
220	DC	1101 1100	12,11,9,8,4	
221	DD	1101 1101	12,11,9,8,5	
222	DE	1101 1110	12,11,9,8,6	
223	DF	1101 1111	12,11,9,8,7	
224	E0	1110 0000	0,8,2	
225	E1	1110 0001	11,0,9,1	
226	E2	1110 0010	0,2	S
227	E3	1110 0011	0,3	T
228	E4	1110 0100	0,4	U
229	E5	1110 0101	0,5	V
230	E6	1110 0110	0,6	W
231	E7	1110 0111	0,7	X
232	E8	1110 1000	0,8	Y
233	E9	1110 1001	0,9	Z
234	EA	1110 1010	11,0,9,8,2	
235	EB	1110 1011	11,0,9,8,3	
236	EC	1110 1100	11,0,9,8,4	
237	ED	1110 1101	11,0,9,8,5	
238	EE	1110 1110	11,0,9,8,6	
239	EF	1110 1111	11,0,9,8,7	
240	F0	1111 0000	0	0
241	F1	1111 0001	1	1
242	F2	1111 0010	2	2
243	F3	1111 0011	3	3
244	F4	1111 0100	4	4
245	F5	1111 0101	5	5
246	F6	1111 0110	6	6
247	F7	1111 0111	7	7
248	F8	1111 1000	8	8
249	F9	1111 1001	9	9
250	FA	1111 1010	12,11,0,9,8,2	
251	FB	1111 1011	12,11,0,9,8,3	
252	FC	1111 1100	12,11,0,9,8,4	
253	FD	1111 1101	12,11,0,9,8,5	
254	FE	1111 1110	12,11,0,9,8,6	
255	FF	1111 1111	12,11,0,9,8,7	¤ (lozenge)

APPENDIX D
POWERS OF TWO TABLE

2^n	n	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 45
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0.000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0.000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0.000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0.000 000 000 029 103 830 456 733 703 613 281 25
68 719 476 736	36	0.000 000 000 014 551 915 228 366 851 806 640 625
137 438 953 472	37	0.000 000 000 007 275 957 614 183 425 903 320 312 5
274 877 906 944	38	0.000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888	39	0.000 000 000 001 818 989 403 545 856 475 830 078 125
1 099 511 627 776	40	0.000 000 000 000 909 494 701 772 928 237 915 039 062 5

APPENDIX E

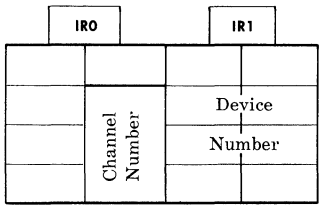
I/O OPERATION INFORMATION

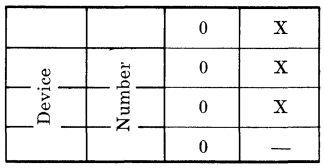
I/O INSTRUCTION FORMAT (SI)

OP		I		B_1		D_1
9C	SDV	0	0			
9E	HDV	0	0	(B_1)	$+D_1=$	Channel and Device
9D	TDV	0	0			
9F	CKC	0	0			

CHANNEL	
000	= MUX
001	=SEL1
002	= SEL2
003	= SEL3

IR AFTER STAT.





SHADED MEMORY ADDRESSING

XXX	LOCATION ADDRESSED
010	$CCR1_{01}$
011	$CCR1_{23}$
100	$CCR2_{01}$
101	$CCR2_{23}$
110	CAR_{01}
111	CAR_{23}

CAW	K	0		Address of CCW				
HSM	E	0						
LOC	Y	0						
48_{16}		0						
CCW1	Command Code		Address of First Data Byte or Address of Next CCW if Command is XFER in Channel					
CCW2	CD	PCI	0	0				
	CC	0	0	0		Byte	Count	
	SLI	0	0	0				
	SKIP	0	0	0				

COMMAND CODE	OPERATION
MMMM0001	SENSE
MMMB0010	READ REVERSE
MMMB0011	WRITE
MMMB0100	WRITE ERASE
MMMB0101	READ
MMMM0111	WRITE CONTROL
MMMM1001	TRANSFER IN CHANNEL

M (Modifier) — Indicates variations of the operation. Definition is provided in the Applicable I/O Device Manuals.

B — Burst Mode Bit.

CC	START DEVICE	HALT DEVICE	TEST DEVICE	CHECK CHANNEL
0	Operation Initiated	Operation not Terminated, Channel or Sub-Channel not Busy	Device Available	Channel Available
1	Operation not Initiated, Check CSB and SDB	Operation not Terminated, Check CSB and SDB	Device not Available, Check CSB and SDB	Term. Interrupt Pending in Selector Channel
2	Operation not Initiated, Channel or Sub-Channel Busy or Term Interrupt Pending	Operation was Terminated	Device not Available, Channel or Sub-Channel Busy	Selector Busy or MUX in Burst Mode Busy
3	Channel or Sub-Channel Inoperable	Not Terminated, Channel or Sub-Channel Inoperable	Device not Available, Channel or Sub-Channel Inoperable	Channel Inoperable

APPENDIX F
TYPEWRITER GRAPHICS AND CODES

Symbol	EBCDIC
A	1100 0001
B	1100 0010
C	1100 0011
D	1100 0100
E	1100 0101
F	1100 0110
G	1100 0111
H	1100 1000
I	1100 1001
J	1101 0001
K	1101 0010
L	1101 0011
M	1101 0100
N	1101 0101
O	1101 0110
P	1101 0111
Q	1101 1000
R	1101 1001
S	1110 0010
T	1110 0011
U	1110 0100
V	1110 0101
W	1110 0110

Symbol	EBCDIC
X	1110 0111
Y	1110 1000
Z	1110 1001
ø	1111 0000
1	1111 0001
2	1111 0010
3	1111 0011
4	1111 0100
5	1111 0101
6	1111 0110
7	1111 0111
8	1111 1000
9	1111 1001
EOT	—— ——
ERROR	—— ——
TOSL	XXXX 0101
CR LF	0001 0101
SPACE	0100 0000
¢	0100 1010
.	0100 1011
<	0100 1100
(	0100 1101
+	0100 1110

Symbol	EBCDIC
|	0100 1111
&	0101 0000
!	0101 1010
$	0101 1011
*	0101 1100
)	0101 1101
;	0101 1110
¬	0101 1111
-	0110 0000
/	0110 0001
^	0110 1010
,	0110 1011
%	0110 1100
_	0110 1101
>	0110 1110
?	0110 1111
:	0111 1010
#	0111 1011
@	0111 1100
'	0111 1101
=	0111 1110
"	0111 1111

EOT — End of Transmission
TOSL — Turn on Send Lamp
CR LF — Carriage Return Line Feed

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ELECTRONIC DATA PROCESSING
CAMDEN, NEW JERSEY 08101