2/20/68

# RCA 1600 USERS GUIDE

Preliminary

## Introduction

The RCA 1600 is made up of several functional blocks and registers. The functional flow diagram of the RCA 1600 shows how these are interconnected functionally.

## Main Memory

The RCA 1600 has a memory cycle of 1.8 microseconds for accessing an 18 bit word. This includes 16 data bits, a memory protect bit, and a parity list. Odd parity is used. The RCA 1600 core memory comes in modules of 1K, 2K, 4K, 8K, 16K, 32K and 64K bytes. Memory can be accessed either by byte or word.

## Standard Registers

There are sixteen 16-bit registers formed physically from 16 integrated circuit chips. These are the standard registers of the RCA 1600. They are addressed as full words (16 bits) or bytes (8 bits). They serve as Basic Instruction Counters (BIC), address registers, high speed I/O registers, as well as working storage registers as required by programs.

The standard registers are divided into two sets. While the use of the standard register is largely a matter of application definition, they have specific functions as shown on the functional flow diagram. Which register set the instruction fields are referring to is designated by the X Register (Program State) defined below. Referring to the Register Matrix of the Functional Flow diagram it will be noted that the Register Set one is grouped from A0A1 to H0H1. A0 refers to the most significant byte of the word and A1 the least. H0H1 is the Basic Instruction Counter of Register Set 1. Register Set Two is grouped from I0I1 to P0P1. N0N1 contains the I/O memory address and 0001 contains the byte count. These are used in conjunction with the high speed I/O channel of the RCA 1600. P0P1 is the Basic Instruction Counter for Register Set 2. The purpose of the N0N1 and 0001 registers is to accommodate devices with high transfer rates.

## The X Register (Program State)

Which Register Set the instruction fields are referring to and which Basic Instruction Counter is sequencing the next instruction fetch is designated by the 3-bit Program State (X) Register. The register settings have the following meanings:

X0=0 Basic Instruction Counter H0H1 and the Register Set 1 is used for MA field.

X0=1 Basic Instruction Counter P0P1 is used and the Register Set 2 is used for MA field.

X1=0 R Field uses Register Set 1

X1=1 R field used Register Set 2

X2=0 Automatic Interrupt Permitted.

X2=1 Automatic Interrupt Inhibited.

Normal use of the RCA 1600 system would have all three bits set either zero or one. Thus, all zeroes refer to Program State 1 and all ones refer to Program State 2. However, each bit may be set individually as required for specific applications.

## The W Register (Control)

This register is utilized for testing of conditions resulting from actions of basic instructions and/or for program linkage. The bits of the W Register have the following meaning:

| | | |
|---|---|---|
| W0 | Carry 1 | - Indicates carry from most significant bit ($2^7$ or $2^{15}$) of an arithmetic operation. |
| W1 | NZD | - Indicates arithmetic operation was zero or not zero. |
| W2 | | - Used for program use. |
| W3 | | - Used for program use. |
| W4 | Carry 2 | - Indicates a carry from the next most significant bit ($2^6$ or $2^{14}$) of an arithmetic operation. |

W5 - Used for program use.

W6 BIT Test - Indicates result for Bit operation Basic Instruction or sign of arithmetic operation.

W7 Program Indicator - Sets Program Indicator Light on Console.

DAD Register (Device Address)

The I/O Device Address Register is a one byte (8 bit) register associated with device address lines. This serves as an address to the Control Electronics (CE's) for utilizing the BIN and BOUT lines. Depending upon the system requirements, more than one address may be utilized by a single CE. Out of the 256 combinations available, 5 have been permanently assigned:

$(00)_{16}$ Assigned to High Speed I/O Service Request. (Not used by the Programmer)

$(01)_{16}$ Reserved for Basic I/O

$(02)_{16}$ Assigned to identification of Class 1 interrupts.

$(03)_{16}$ Assigned to identification of Class 2 interrupts.

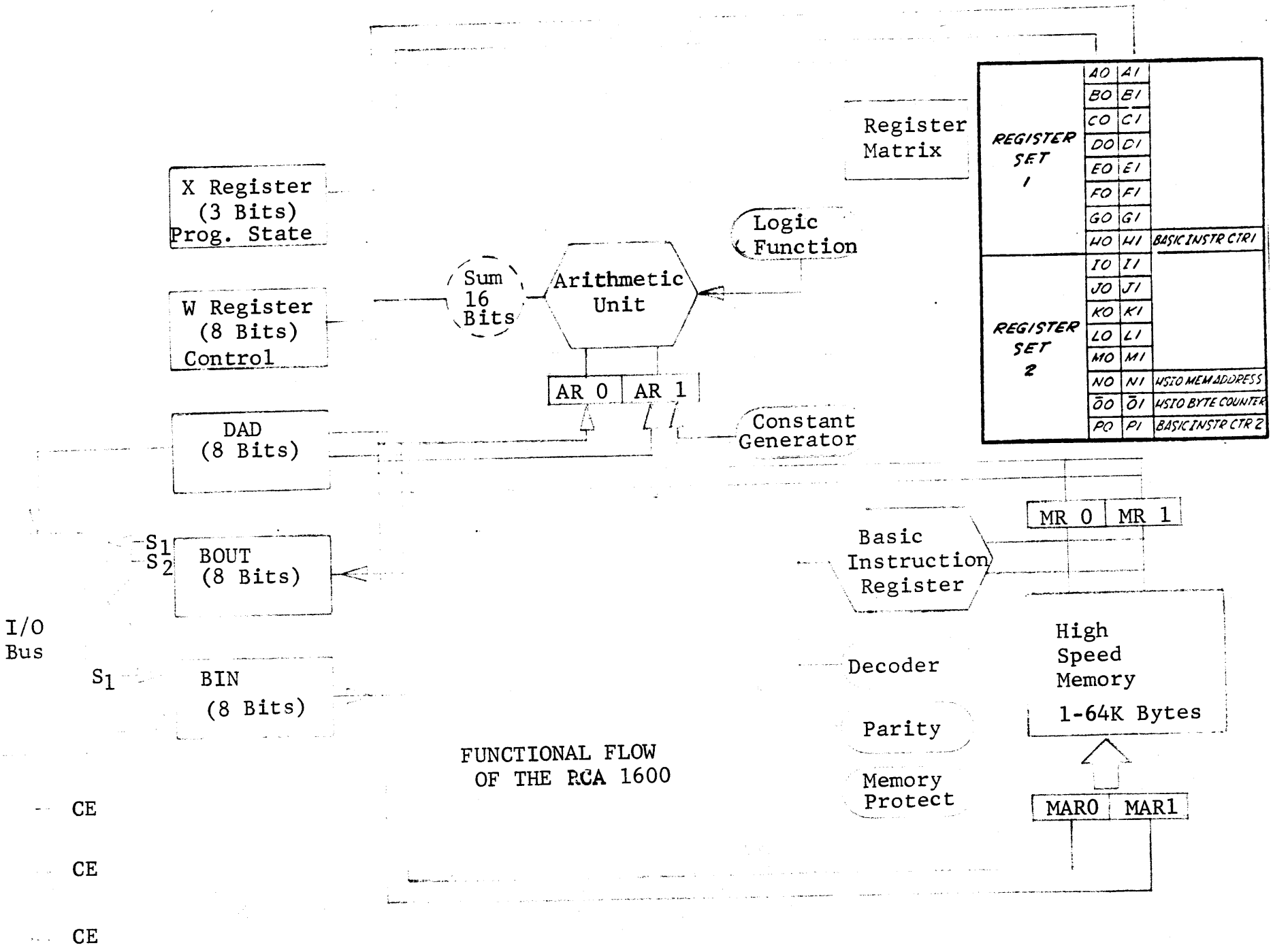
$(FF)_{16}$ Reserved for Test and Maintenance Programming.

Assignment of other DAD addresses is usually at system installation time.

BOUT (Bus Output) Register

BOUT consists of 8 output lines and one of the two Strobe lines. BOUT-S1 is the output register of one byte connected to the 8-BOUT lines and Strobe 1 which in turn are connected to the I/O Bus. When BOUT-S1 is addressed by one of the basic instructions, the information byte is transferred to the CE via the BOUT lines of the I/O Bus and Strobe 1 signal via the Strobe 1 line. Which CE will accept the information and the resulting actions are defined by the current DAD address and CE specifications.

BOUT-S2 is identical with BOUT-S1 except the Strobe 2 line is used in place of Strobe 1.




FUNCTIONAL FLOW
OF THE RCA 1600

## BIN (Bus Input) Register

A Bus Input Register physically consisting of the 8 BIN lines of the I/O Bus. The contents of the BIN lines are determined by the DAD address and the CE specifications. BIN-S0 refers to the 8 BIN lines and with no strobe lines used. The basic instruction may address the register as individual bits or as an entire byte. When addressing individual bits, the least significant position ($2^0$) of BIN is designated as BIN0 to the most significant position ($2^7$) of BIN or BIN7. A CE is not affected or notified when BIN-S0 is addressed.

BIN-S1 consists of the 8 BIN lines and Strobe 1 of the I/O Bus. When BIN-S1 is addressed, a Strobe 1 signal is transmitted via the strobe one line. Which CE will accept this signal and the resulting actions are defined by the current DAD address and the CE specifications.

## Arithmetic Unit

The RCA 1600 arithmetic unit physically is an 8-bit binary adder. The Basic Instruction arithmetic functions are for 8 or 16 bit operations. Since 16 bit operations are automatically cycled in two steps through the adder, the system is functionally a 16 bit arithmetic unit.

MAR Register is the Memory Address Register. MAR0 and MAR1 refer to the most and least significant byte of the word respecitively.

MR Register is the Memory Register and holds the most (MR0) and least (MR1) significant byte of the word.

BIR Register is the Basic Instruction Register. The contents are functionally decoded, parity checked, and Memory Protect is checked here.

The Basic Instructions total 29. They are logically divided into 3 groups. The formats of these groups are as follows:

Group 1 Memory to Register 10 Instructions

| F<br>Function Code | MA | I | S | R |
|---|---|---|---|---|
| 5 Bits | 3 Bits | 3 Bits | 1 Bit | 4 Bits |
| $2^{15}$ $2^{11}$ | $2^{10}$ $2^{8}$ | $2^{7}$ $2^{5}$ | $2^{4}$ | $2^{3}$ $2^{0}$ |

The instructions of Group I are:

| Instruction | Mnemonic |
|---|---|
| Write to Memory | WTM |
| Read Memory and Transfer | RMT |
| Read Memory and Add | RMA |
| Read Memory and Subtract | RMS |
| Read Memory and Add with Carry | RMAC |
| Read Memory and Subtract with Carry | MMSC |
| Read Memory and Compare | RMC |
| I/O Transfer to Memory | IOTM |
| I/O Transfer from Memory | IOFM |
| Memory Protect Set and Reset | MPSR |

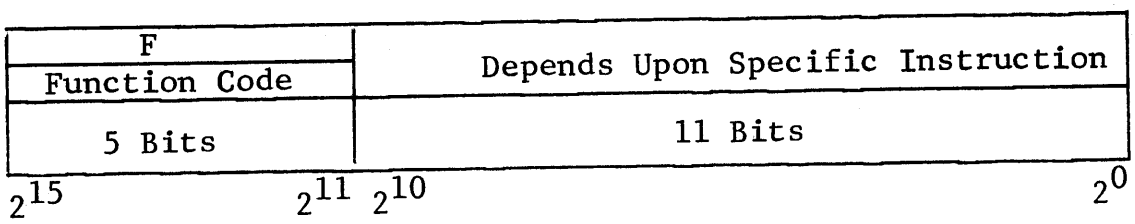
Group II Register to Register 10 Instructions

| F<br>Function Code | R1 | SF | S | R2 |
|---|---|---|---|---|
| 5 Bits | 4 Bits | 2 Bits | 1 Bit | 4 Bits |
| $2^{15}$ $2^{11}$ | $2^{10}$ $2^{7}$ | $2^{6}$ $2^{5}$ | $2^{4}$ | $2^{3}$ $2^{0}$ |

The instructions of Group II are:

| Instruction | Mnemonic |
|---|---|
| Add | ABR |
| Subtract | SBR |
| Add with Carry | ABRC |
| Subtract with Carry | SBRC |
| Compare | CMPR |
| And | ANDR |
| Or | ORR |
| Exclusive Or | XORR |
| Transfer | TRR |
| Standard Register Set Transfer | SRST |

Group III General Instructions 9 Instructions




The formats of the 9 general instructions vary according to their specific function. The 9 instructions are:

| Instruction | Mnemonic |
|---|---|
| Halt | Halt |
| Shift | SFT |
| Test and Branch | TAB |
| I/O Test and Branch | IOB |
| Decrement and Branch | DAB |
| Increment and Decrement | IDR |
| Bit Operation | BIT |
| Constant to Standard Register | CSTR |
| Constant to Special Register | CSPR |

| F<br>Function Code | MA | I | S | R |
|---|---|---|---|---|
| 10010 | 3 Bits | 3 Bits | 1 Bit | 4 Bits |

$2^{15}$ $2^{11}$ $2^{10}$ $2^{8}$ $2^{7}$ $2^{5}$ $2^{4}$ $2^{3}$ $2^{0}$

Bit Position

Instruction Time - Byte Operation 3.6 us
Word Operation 4.5 us

This instruction performs a compare between two operands, one from memory and the other from a standard register. The operands are unchanged at the termination of the RMC instruction and the results of the compare can be tested through the W Register (Control Register).

R • (MA)

The contents of the memory location addressed by the contents of the standard register specified by the MA field is one operand. The contents of the standard register indicated by the R field is the other operand. The results of the instruction modify the Control Register (W) bits as follows:

The initial setting of the control register does not effect this operation. However, RMC modifies bits of the W register (Control Register) as follows:

| W Register Bit | Action On |
|---|---|
| $2^{0}$ Carry 1 | Set to one if carry, set to zero if no carry from most significant bit of operation ($2^{7}$ for byte and $2^{15}$ for word operations). |
| $2^{4}$ Carry 2 | Set to one if carry, set to zero if no carry from next most significant bit of operation ($2^{6}$ for byte and $2^{14}$ for word operations). |

RMC Continued

| W Register Bit | Action On |
|---|---|
| $2^1$ NZD | Set to zero if result of operation is zero, set to one if operation is non-zero. |
| $2^6$ Bit Operation Test | Set to zero if most significant bit of result is zero and set to one if it is one ($2^7$ for byte and $2^{15}$ for word operations). |

and are interpreted as follows:

| CONTROL REGISTER (W) | |
|---|---|
| W0 | CARRY 1 - INDICATES CARRY FROM ($2^7$ OR $2^{15}$) OF ARITHMETIC OPERATION |
| W1 | NZD - INDICATES ARITHMETIC OPERATION RESULT WAS NOT ZERO |
| W2 | INDICATOR FOR PROGRAM USE |
| W3 | INDICATOR FOR PROGRAM USE |
| W4 | CARRY 2 - INDICATES CARRY FROM ($2^6$ OR $2^{14}$) OF ARITHMETIC OPERATION |
| W5 | INDICATOR FOR PROGRAM USE |
| W6 | BIT OP TEST - INDICATES RESULT OF BIT OP BIT OR SIGN OF ARITHMETIC OPERATION |
| W7 | PROGRAM INDICATOR - SETS PI LIGHT ON CONSOLE |

| if | Then W bits are set as follows: |
|---|---|
| MA = R | $2^1$ of W = Ø (Binary) |
| MA ≠ R | $2^1$ of W = 1 (Binary) |
| MA ≥ R | $2^0$ of W = 1 (Binary) |
| MA < R | $2^0$ of W = Ø (Binary) |
| MA = R | $2^1$ of W = Ø (Signed) |
| MA ≠ R | $2^1$ of W = 1 (Signed) |
| MA ≥ R | $2^6$ of W = Ø (Signed) |
| MA < R | $2^6$ of W = 1 (Signed) |

RMC Continued

The S field indicates whether one byte or one word operations are executed. If S = 0, a byte operation is performed and if S = 1, a word operation is performed.

The I field specifies the amount of increment or decrement of the contents of the standard register specified by the MA field. The amount is programmed as follows:

I FIELD

| 7 6 5 | INC/DEC |
|---|---|
| 0 0 0 | 0 |
| 0 0 1 | +1 |
| 0 1 0 | +2 |
| 0 1 1 | +4 |
| 1 0 0 | +6 |
| 1 0 1 | -1 |
| 1 1 0 | -2 |
| 1 1 1 | -4 |

The setting of the Program State (X) Register bits $2^0$ and $2^1$ conditions the R and MA fields as follows:

R FIELD

| 3 2 1 0 | MATRIX REG XI = 0 | MATRIX REG XI = 1 | SPECIAL REGISTER (RP) |
|---|---|---|---|
| 0 0 0 0 | A0 | I0 | BIN 0 |
| 0 0 0 1 | A1 | I1 | |
| 0 0 1 0 | B0 | J0 | BIN 1 |
| 0 0 1 1 | B1 | J1 | |
| 0 1 0 0 | C0 | K0 | BOUT 2 |
| 0 1 0 1 | C1 | K1 | |
| 0 1 1 0 | D0 | L0 | BOUT 1 |
| 0 1 1 1 | D1 | L1 | |
| 1 0 0 0 | E0 | M0 | DAD |
| 1 0 0 1 | E1 | M1 | |
| 1 0 1 0 | F0 | N0 | W |
| 1 0 1 1 | F1 | N1 | |
| 1 1 0 0 | G0 | $\bar{O}0$ | X |
| 1 1 0 1 | G1 | $\bar{O}1$ | |
| 1 1 1 0 | H0 | P0 | |
| 1 1 1 1 | H1 | P1 | |

MA FIELD

| 10 9 8 | XO = 0 | XO = 1 |
|---|---|---|
| 0 0 0 | A | I |
| 0 0 1 | B | J |
| 0 1 0 | C | K |
| 0 1 1 | D | L |
| 1 0 0 | E | M |
| 1 0 1 | F | N |
| 1 1 0 | G | $\bar{O}$ |
| 1 1 1 | H | P |

NOTE: If S=1, $2^0$ of the R field are $2^7$ of the MA register is ignored and the full word is used for this operation.

RMT Read Memory and Transfer to Matrix MPXF

| F<br>Function Code | MA | I | S | R |
|---|---|---|---|---|
| 11010 | 3 Bits | 3 Bits | 1 Bit | 4 Bits |

$2^{15}$ $2^{11}$ $2^{10}$ $2^{8}$ $2^{7}$ $2^{5}$ $2^{4}$ $2^{3}$ $2^{0}$

Bit Position

Instruction Time - Byte or Word 3.6 us

This instruction loads the contents of a memory location to a standard register. The MA field specifies the standard register which contains the word memory address of the data to be transferred to a register specified by the R field.

The S field specifies whether one byte or one word is stored. If S = 0, a byte is stored; if S = 1, a word is stored.

The I field specifies the amount of increment or decrement of the contents of the standard register identified in the MA field. The amount is specified in the I field as follows:

I FIELD

| 7 6 5 | INC/DEC |
|---|---|
| 0 0 0 | 0 |
| 0 0 1 | +1 |
| 0 1 0 | +2 |
| 0 1 1 | +4 |
| 1 0 0 | +6 |
| 1 0 1 | -1 |
| 1 1 0 | -2 |
| 1 1 1 | -4 |

The setting of the Program State Register (X) Bits $2^0$ and $2^1$ conditions the R and MA field as follows:

| CONTROL REGISTER (W) | |
|---|---|
| W0 | CARRY 1-INDICATES CARRY FROM (2⁷ OR 2¹⁵) OF ARITHMETIC OPERATION |
| W1 | NEQ-INDICATES ARITHMETIC OPERATION RESULT WAS NOT ZERO |
| W2 | INDICATOR FOR PROGRAM USE |
| W3 | INDICATOR FOR PROGRAM USE |
| W4 | CARRY 2-INDICATES CARRY FROM (2⁶ OR 2¹⁴) OF ARITHMETIC OPERATION |
| W5 | INDICATOR FOR PROGRAM USE |
| W6 | BIT OP TEST-INDICATES RESULT OF BITOP BIT OR SIGN OF ARITHMETIC OPERATION |
| W7 | PROGRAM INDICATOR-SETS PI LIGHT ON CONSOLE |

MA FIELD

| 10 9 8 (2 2 2) | X0 = 0 | X0 = 1 |
|---|---|---|
| 0 0 0 | A | I |
| 0 0 1 | B | J |
| 0 1 0 | C | K |
| 0 1 1 | D | L |
| 1 0 0 | E | M |
| 1 0 1 | F | N |
| 1 1 0 | G | $\bar{O}$ |
| 1 1 1 | H | P |

R FIELD

| 3 2 1 0 (2 2 2 2) | MATRIX REG X1 = 0 | MATRIX REG X1 = 1 | SPECIAL REGISTER (RP) |
|---|---|---|---|
| 0 0 0 0 | A0 | I0 | BIN0 |
| 0 0 0 1 | A1 | I1 | |
| 0 0 1 0 | B0 | J0 | BIN1 |
| 0 0 1 1 | B1 | J1 | |
| 0 1 0 0 | C0 | K0 | BOUT2 |
| 0 1 0 1 | C1 | K1 | |
| 0 1 1 0 | D0 | L0 | BOUT1 |
| 0 1 1 1 | D1 | L1 | |
| 1 0 0 0 | E0 | M0 | DAD |
| 1 0 0 1 | E1 | M1 | |
| 1 0 1 0 | F0 | N0 | W |
| 1 0 1 1 | F1 | N1 | |
| 1 1 0 0 | G0 | $\bar{O}0$ | X |
| 1 1 0 1 | G1 | $\bar{O}1$ | |
| 1 1 1 0 | H0 | P0 | |
| 1 1 1 1 | H1 | P1 | |

The Control Register (W) is not affected nor does it affect this instruction.

Note: If S = 1 - The 2 bit of the R field is ignored and the 2 bit of the MA register is ignored and the full word from memory is stored into the register.

RMA Read Memory and Add MPADD

| F<br>Function Code | MA | I | S | R |
|---|---|---|---|---|
| 11001 | 3 Bits | 3 Bits | 1 Bit | 4 Bits |
| $2^{15}$ $2^{11}$ | $2^{10}$ $2^{8}$ | $2^{7}$ $2^{5}$ | $2^{4}$ | $2^{3}$ $2^{0}$ |

Bit Position

Instruction Time - Byte Operation 3.6 us
Word Operation 4.5 us

This instruction performs a binary add of two operands, one from memory and the other from a standard register. The result is stored in the standard register.

$$R + (MA) \longrightarrow R$$

The contents of a memory locations addressed by the contents of the standard register, indicated by the MA field is one operand. The contents of the standard register, indicated by the R field, is the other operand. The result is stored in the standard register identified in the R field.

The S field identifies whether one byte or one word operations are performed. If S = 0, a byte operation is performed; if S = 1, a word operation is performed.

The I field states the amount of increment or decrement of the contents of the standard register identified in the MA field. The amount is specified in the I field as follows:

IFIELD

| 7 6 5 | INC/DEC |
|---|---|
| 0 0 0 | 0 |
| 0 0 1 | +1 |
| 0 1 0 | +2 |
| 0 1 1 | +4 |
| 1 0 0 | +6 |
| 1 0 1 | -1 |
| 1 1 0 | -2 |
| 1 1 1 | -4 |

The setting of the Program State Register (X) bits $2^0$ and $2^1$ conditions the MA and R fields as follows:

| CONTROL REGISTER (W) | |
|---|---|
| W0 | CARRY1-INDICATES CARRY FROM ($2^7$ OR $2^{15}$) OF ARITHMETIC OPERATION |
| W1 | NZD-INDICATES ARITHMETIC OPERATION RESULT WAS NOT ZERO |
| W2 | INDICATOR FOR PROGRAM USE |
| W3 | INDICATOR FOR PROGRAM USE |
| W4 | CARRY2-INDICATES CARRY FROM ($2^6$ OR $2^{14}$) OF ARITHMETIC OPERATION |
| W5 | INDICATOR FOR PROGRAM USE |
| W6 | BIT OP TEST-INDICATES RESULT OF BITOP BIT OR SIGN OF ARITHMETIC OPERATION |
| W7 | PROGRAM INDICATOR-SETS PI LIGHT ON CONSOLE |

MA FIELD

| 10 9 8 | X0= 0 | X0= 1 |
|---|---|---|
| 0 0 0 | A | I |
| 0 0 1 | B | J |
| 0 1 0 | C | K |
| 0 1 1 | D | L |
| 1 0 0 | E | M |
| 1 0 1 | F | N |
| 1 1 0 | G | $\bar{O}$ |
| 1 1 1 | H | P |

R FIELD

| $2^3$ $2^2$ $2^1$ $2^0$ | MATRIX REG X1= 0 | MATRIX REG X1= 1 | SPECIAL REGISTER (RP) |
|---|---|---|---|
| 0 0 0 0 | A0 | I0 | BIN0 |
| 0 0 0 1 | A1 | I1 | |
| 0 0 1 0 | B0 | J0 | BIN1 |
| 0 0 1 1 | B1 | J1 | |
| 0 1 0 0 | C0 | K0 | BOUT2 |
| 0 1 0 1 | C1 | K1 | |
| 0 1 1 0 | D0 | L0 | BOUT1 |
| 0 1 1 1 | D1 | L1 | |
| 1 0 0 0 | E0 | M0 | DAD |
| 1 0 0 1 | E1 | M1 | |
| 1 0 1 0 | F0 | N0 | W |
| 1 0 1 1 | F1 | N1 | |
| 1 1 0 0 | G0 | $\bar{O}0$ | X |
| 1 1 0 1 | G1 | $\bar{O}1$ | |
| 1 1 1 0 | H0 | P0 | |
| 1 1 1 1 | H1 | P1 | |

The setting of the Control Register (W) does not affect this instruction. However, the RMA modifies bits of the W Register as follows:

| W Bit | Action On |
|---|---|
| $2^0$ Carry 1 | Set to one if carry, set to zero if no carry from the most significant bit of operation ($2^7$ for byte operation, $2^{14}$ for word operation). |
| $2^4$ Carry 2 | Set to one if carry, set to zero if no carry from next most significant bit of operation ($2^6$ for byte operation, $2^{14}$ for word operation). |
| $2^1$ NZD | Set to zero if result of operation is zero, set to one if result of operation is non-zero. |

| W Bit | Action On |
|---|---|
| $2^6$ Bit Operation Test | Set to zero if most significant bit ($2^7$ for byte operation, $2^{15}$ for word operation) of the result is zero. Set to one if most significant bit of result is one. |

Note: If S = 1 - $2^0$ of the R field and $2^0$ of the MA register is ignored and the full words are used for this operation.

RMAC Read Memory and Add With Carry MPAC

| F<br>Function Code | MA | I | S | R |
|---|---|---|---|---|
| 11011 | 3 Bits | 3 Bits | 1 Bit | 4 Bits |

$2^{15}$ $2^{11}$ $2^{10}$ $2^{8}$ $2^{7}$ $2^{5}$ $2^{4}$ $2^{3}$ $2^{0}$

Bit Positions

Instruction Time - Byte Operation 3.6 us
Word Operation 4.5 us

RMAC performs a binary add of two operands, one from memory and the other from a standard register, plus an initial carry setting, and stores the result at the standards register.

$$R + (MA) + WO(2^0) \longrightarrow R$$

The contents of a memory location addressed by the contents of the standard register specified in the MA field is one operand. The standard register addressed by the R field in the other operand. The contents to carry 1 ($2^0$ of the W register) provides the initial carry. The result is stored at R.

The S field indicates whether one byte or one word operations are performed. If S = 0, a byte operation is performed. If S = 1, a word operation is indicated.

The I field specifies the amount of increment or decrement desired for the standard register addressed in the MA field. The amount is as follows:

IFIELD

| 7 6 5 | INCR DEC |
|---|---|
| 0 0 0 | 0 |
| 0 0 1 | +1 |
| 0 1 0 | +2 |
| 0 1 1 | +4 |
| 1 0 0 | +6 |
| 1 0 1 | -1 |
| 1 1 0 | -2 |
| 1 1 1 | -4 |

The setting of the Program State (X) Register bits $2^0$ and $2^1$ affects the R and MA fields as follows:

| CONTROL REGISTER (W) | |
|---|---|
| W0 | CARRY 1-INDICATES CARRY FROM ($2^0$ OR $2^{15}$) OF ARITHMETIC OPERATION |
| W1 | NZD-INDICATES ARITHMETIC OPERATION RESULT WAS NOT ZERO |
| W2 | INDICATOR FOR PROGRAM USE |
| W3 | INDICATOR FOR PROGRAM USE |
| W4 | CARRY 2-INDICATES CARRY FROM ($2^6$ OR $2^{14}$) OF ARITHMETIC OPERATION |
| W5 | INDICATOR FOR PROGRAM USE |
| W6 | BIT OR TEST-INDICATES RESULT OF BITOP BIT OR SIGN OF ARITHMETIC OPERATION |
| W7 | PROGRAM INDICATOR-SETS PI LIGHT ON CONSOLE |

MA FIELD

| $2^{10}$ $2^9$ $2^8$ | XO= 0 | 1 |
|---|---|---|
| 0 0 0 | A | I |
| 0 0 1 | B | J |
| 0 1 0 | C | K |
| 0 1 1 | D | L |
| 1 0 0 | E | M |
| 1 0 1 | F | N |
| 1 1 0 | G | $\bar{O}$ |
| 1 1 1 | H | P |

R FIELD

| $2^3$ $2^2$ $2^1$ $2^0$ | MATRIX REG XI = 0 | 1 | SPECIAL REGISTER (RP) |
|---|---|---|---|
| 0 0 0 0 | A0 | I0 | BIN0 |
| 0 0 0 1 | A1 | I1 | |
| 0 0 1 0 | B0 | J0 | BIN1 |
| 0 0 1 1 | B1 | J1 | |
| 0 1 0 0 | C0 | K0 | BOUT2 |
| 0 1 0 1 | C1 | K1 | |
| 0 1 1 0 | D0 | L0 | BOUT1 |
| 0 1 1 1 | D1 | L1 | |
| 1 0 0 0 | E0 | M0 | DAD |
| 1 0 0 1 | E1 | M1 | |
| 1 0 1 0 | F0 | N0 | W |
| 1 0 1 1 | F1 | N1 | |
| 1 1 0 0 | G0 | $\bar{O}0$ | X |
| 1 1 0 1 | G1 | $\bar{O}1$ | |
| 1 1 1 0 | H0 | P0 | |
| 1 1 1 1 | H1 | P1 | |

The initial setting of the W Register affects the operation as follows:

| W Register Bits | Action On |
|---|---|
| $2^0$ Carry 1 | The setting of this position is used as a carry into $2^0$ position of the operation. |

and the instruction modifies bits of the W Register as follows:

| | |
|---|---|
| $2^0$ Carry 1 | Set to one if carry, set to zero if no carry from the most significant bit of the operation ($2^7$ for byte and $2^{15}$ for word operations). |
| $2^0$ Carry 2 | Set to one if carry, set to zero if no carry from next most significant bit of operation ($2^6$ for byte and $2^{14}$ for word operations). |
| $2^1$ NZD | If result of this operation is a zero, this bit will remain unchanged from its initial condition. If the result of the operation is non-zero, the bit is set to one. |

| W Register Bits | Action On |
|---|---|
| 2 Bit Operation Test | Set to zero if most significant bit of result is zero. Set to one if most significant bit of result is one. ($2^7$ for byte and $2^{15}$ for word operations). |

Note: If S = 1 - $2^0$ of the R and MA register is ignored and the full word operation is performed.

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| W Register Bits | Action On |
|---|---|
| $2^6$ Bit Operation Test | Set to zero if most significant bit of the result is zero and set to one if it is one ($2^7$ for byte and $2^{15}$ for word operations). |

Note: 1. The difference is placed in the subtrahend rather than the minuend. In Register to Register Subtract, the result replaces the minuend.

2. If S = 1, $2^0$ bits of the R field and MA register are ignored and the full word is used for this operation.

The setting of the Program State (X) Register Bits $2^0$ and $2^1$ conditions the R and MA fields as follows:

R FIELD

| $2^3$ $2^2$ $2^1$ $2^0$ | MATRIX REG XI = 0 | MATRIX REG XI = 1 | SPECIAL REGISTER (RP) |
|---|---|---|---|
| 0 0 0 0 | A0 | I0 | BIN0 |
| 0 0 0 1 | A1 | I1 | |
| 0 0 1 0 | B0 | J0 | BIN1 |
| 0 0 1 1 | B1 | J1 | |
| 0 1 0 0 | C0 | K0 | BOUT2 |
| 0 1 0 1 | C1 | K1 | |
| 0 1 1 0 | D0 | L0 | BOUT1 |
| 0 1 1 1 | D1 | L1 | |
| 1 0 0 0 | E0 | M0 | DAD |
| 1 0 0 1 | E1 | M1 | |
| 1 0 1 0 | F0 | N0 | W |
| 1 0 1 1 | F1 | N1 | |
| 1 1 0 0 | G0 | $\overline{G0}$ | X |
| 1 1 0 1 | G1 | $\overline{G1}$ | |
| 1 1 1 0 | H0 | P0 | |
| 1 1 1 1 | H1 | P1 | |

MA FIELD

| $2^{10}$ $2^9$ $2^8$ | K0 = 0 | K0 = 1 |
|---|---|---|
| 0 0 0 | A | I |
| 0 0 1 | B | J |
| 0 1 0 | C | K |
| 0 1 1 | D | L |
| 1 0 0 | E | M |
| 1 0 1 | F | N |
| 1 1 0 | G | $\overline{G}$ |
| 1 1 1 | H | P |

CONTROL REGISTER (W)

| | |
|---|---|
| W0 | CARRY1-INDICATES CARRY FROM ($2^7$ OR $2^{15}$) OF ARITHMETIC OPERATION |
| W1 | NZD-INDICATES ARITHMETIC OPERATION RESULT WAS NOT ZERO |
| W2 | INDICATOR FOR PROGRAM USE |
| W3 | INDICATOR FOR PROGRAM USE |
| W4 | CARRY2-INDICATES CARRY FROM ($2^6$ OR $2^{14}$) OF ARITHMETIC OPERATION |
| W5 | INDICATOR FOR PROGRAM USE |
| W6 | BITOPTEST-INDICATES RESULT OF BITOP BIT OR SIGN OF ARITHMETIC OPERATION |
| W7 | PROGRAM INDICATOR-SETS PI LIGHT ON CONSOLE |

The initial setting of the W Register affects this instruction as follows:

| W Register Bits | Action On |
|---|---|
| $2^0$ Carry 1 | The setting of this position is used as a carry into $2^0$ position of the operation. |

and the instruction modifies bits of the W register as follows:

| | |
|---|---|
| $2^0$ Carry 1 | Set to one if carry, set to zero if no carry from most significant bit of operation ($2^7$ for byte and $2^{15}$ for word operation). |
| $2^4$ Carry 2 | Set to one if carry, set to zero if no carry from next most significant bit of operation. ($2^6$ for byte and $2^{14}$ for word operations). |
| $2^1$ NZD | If the result of this operation is a zero, this bit will remain unchanged from initial conditions. If the result of the operation is non-zero, the bit is set to one. |

IOFM I/O Transfer From Memory (Transfer Memory to Bout) MPXFB

| F Function Code | MA | I | S | R | | | |
|---|---|---|---|---|---|---|---|
| 10000 | 3 Bits | 3 Bits | X | X | X | | X |
| $2^{15}$ $2^{11}$ | $2^{10}$ $2^{8}$ | $2^{7}$ $2^{5}$ | $2^{4}$ | $2^{3}$ | $2^{2}$ | $2^{1}$ | $2^{0}$ |

Bit Position

Instruction Time - 3.6 us

This instruction transfers the contents of a one byte memory location to an input/output Control Electronics (CE). The CE is specified by the previously set Device Address Register (DAD). The memory byte location is specified by the contents of the standard register designated by the MA field (an odd memory address specifies the low order byte, an even the high order byte of the memory word). The transfer over the I/O Bus is conditioned with Strobe 1 or Strobe 2 as indicated by the R field. The R settings are as follows:

XX0X Bout 2
XX1X Bout 1 (X means don't care case)

The S field is ignored since all operations are one byte.

The I field designates the amount of increment or decrement of the MA register as follows:

I FIELD

| $2^7$ $2^6$ $2^5$ | INC/DEC |
|---|---|
| 0 0 0 | 0 |
| 0 0 1 | +1 |
| 0 1 0 | +2 |
| 0 1 1 | +4 |
| 1 0 0 | +6 |
| 1 0 1 | -1 |
| 1 1 0 | -2 |
| 1 1 1 | -4 |

The W (Control) Register does not affect nor is it modified by their instruction.

IOFM Continued

The setting of the X (Program State) Register $2^0$ bit conditions the MA field as follows:

MA FIELD

| $2^{10}$ | $2^9$ | $2^8$ | X0 = 0 | X0 = 1 |
|---|---|---|---|---|
| 0 | 0 | 0 | A | I |
| 0 | 0 | 1 | B | J |
| 0 | 1 | 0 | C | K |
| 0 | 1 | 1 | D | L |
| 1 | 0 | 0 | E | M |
| 1 | 0 | 1 | F | N |
| 1 | 1 | 0 | G | $\overline{O}$ |
| 1 | 1 | 1 | H | P |

IOTM I/O Transfer to Memory WTBM
(Write Bin to Memory)

| F<br>Function Code | MA | I | S | R | | | |
|---|---|---|---|---|---|---|---|
| 11000 | 3 Bits | 3 Bits | X | X | X | | X |
| $2^{15}$ $2^{11}$ | $2^{10}$ $2^{8}$ | $2^{7}$ $2^{5}$ | $2^{4}$ | $2^{3}$ | $2^{2}$ | $2^{1}$ | $2^{0}$ |

Bit Position

Instruction Time - 3.6 us

This instruction provides the ability to transfer 8 bits to a one byte memory location from the Input/Output Bus. The CE (Control Electronics) is specified by the previously set Device Address Register (DAD). The memory byte location is specified by the contents of the standard register designated by the MA field. (An odd memory address specifies the low order 8 bit byte of the memory word and the even memory address designates the high order 8 bit byte of the memory word.) The CE may or may not be notified of the transfer as indicated by the R field. When Bin 0 is designated, no strobe is sent and when Bin 1 is designated, strobe 1 is sent.

The valid R settings are as follows:

XX0X Bin 0 (X means don't care case)
XX1X Bin 1

The S field is ignored since all operations are one byte.

The I field provides the ability to increment or decrement the MA register as follows:

I FIELD

| 7 6 5 | INC/DEC |
|---|---|
| 0 0 0 | 0 |
| 0 0 1 | +1 |
| 0 1 0 | +2 |
| 0 1 1 | +4 |
| 1 0 0 | +6 |
| 1 0 1 | -1 |
| 1 1 0 | -2 |
| 1 1 1 | -4 |

IOTM Continued

The W (Control) Register does not affect nor is it modified by this instruction.

The setting of the X (Program State) Register $2^0$ bit conditions the MA field as follows:

MA FIELD

| $2^{10}$ | $2^9$ | $2^8$ | XO= 0 | XO= 1 |
|---|---|---|---|---|
| 0 | 0 | 0 | A | I |
| 0 | 0 | 1 | B | J |
| 0 | 1 | 0 | C | K |
| 0 | 1 | 1 | D | L |
| 1 | 0 | 0 | E | M |
| 1 | 0 | 1 | F | N |
| 1 | 1 | 0 | G | $\overline{O}$ |
| 1 | 1 | 1 | H | P |

| F<br>Function Code | MA | I | S | R |
|---|---|---|---|---|
| 10001 | 3 Bits | 3 Bits | 1 Bit | 4 Bits |
| $2^{15}$ $2^{11}$ | $2^{10}$ $2^{8}$ | $2^{7}$ $2^{5}$ | $2^{4}$ | $2^{3}$ $2^{0}$ |

Bit Position

Instruction Time - Byte Operation 3.6 us
Word Operation 4.5 us

The instruction performs a binary subtract between two operands, one from memory and the other from a standard register. The result is stored in the standard register.

$$(MA) - R \longrightarrow R$$

The contents of the memory location, addressed by the contents of the standard register indicated in the MA field, is the minuend. The contents of the standard register, indicated by the R field is the subtrahend. The result is stored in the standard register specified by the R field.

The S field indicates whether the instruction operates on bytes or words. If S = 0, a byte operation is executed. If S = 1, a word operation is performed.

The I field provides the ability to increment or decrement the register specified in the MA field. The amount is specified below:

I FIELD

| 7 6 5 | INC/DEC |
|---|---|
| 0 0 0 | 0 |
| 0 0 1 | +1 |
| 0 1 0 | +2 |
| 0 1 1 | +4 |
| 1 0 0 | +6 |
| 1 0 1 | -1 |
| 1 1 0 | -2 |
| 1 1 1 | -4 |

RMS Continued

The setting of the Program State Register (X) conditions the MA and R fields as follows:

| CONTROL REGISTER (W) | |
|---|---|
| W0 | CARRY 1 - INDICATES CARRY FROM ($2^7$ OR $2^{15}$) OF ARITHMETIC OPERATION |
| W1 | NZD - INDICATES ARITHMETIC OPERATION RESULT WAS NOT ZERO |
| W2 | INDICATOR FOR PROGRAM USE |
| W3 | INDICATOR FOR PROGRAM USE |
| W4 | CARRY 2 - INDICATES CARRY FROM ($2^6$ OR $2^{14}$) OF ARITHMETIC OPERATION |
| W5 | INDICATOR FOR PROGRAM USE |
| W6 | BITOP TEST - INDICATES RESULT OF BITOP OR SIGN OF ARITHMETIC OPERATION |
| W7 | PROGRAM INDICATOR - SETS PI LIGHT ON CONSOLE |

MA FIELD

| $2^{10}$ | $2^9$ | $2^8$ | X0 = 0 | X0 = 1 |
|---|---|---|---|---|
| 0 | 0 | 0 | A | I |
| 0 | 0 | 1 | B | J |
| 0 | 1 | 0 | C | K |
| 0 | 1 | 1 | D | L |
| 1 | 0 | 0 | E | M |
| 1 | 0 | 1 | F | N |
| 1 | 1 | 0 | G | $\overline{O}$ |
| 1 | 1 | 1 | H | P |

R FIELD

| $2^3$ | $2^2$ | $2^1$ | $2^0$ | MATRIX REG X1 = 0 | MATRIX REG X1 = 1 | SPECIAL REGISTER (RP) |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | A0 | I0 | BIN0 |
| 0 | 0 | 0 | 1 | A1 | I1 | |
| 0 | 0 | 1 | 0 | B0 | J0 | BIN1 |
| 0 | 0 | 1 | 1 | B1 | J1 | |
| 0 | 1 | 0 | 0 | C0 | K0 | BOUT2 |
| 0 | 1 | 0 | 1 | C1 | K1 | |
| 0 | 1 | 1 | 0 | D0 | L0 | BOUT1 |
| 0 | 1 | 1 | 1 | D1 | L1 | |
| 1 | 0 | 0 | 0 | F0 | M0 | DAD |
| 1 | 0 | 0 | 1 | E1 | M1 | |
| 1 | 0 | 1 | 0 | F0 | N0 | W |
| 1 | 0 | 1 | 1 | F1 | N1 | |
| 1 | 1 | 0 | 0 | G0 | $\overline{O}0$ | X |
| 1 | 1 | 0 | 1 | G1 | $\overline{O}1$ | |
| 1 | 1 | 1 | 0 | H0 | P0 | |
| 1 | 1 | 1 | 1 | H1 | P1 | |

The initial setting of the W Register (Control) does not affect this instruction. However RMS modifies bits of the Control Register as follows:

| W Bit | Action On |
|---|---|
| $2^0$ Carry 1 | Set to one if carry, set to zero if no carry from the most significant bit of the operation. ($2^7$ for byte and $2^{15}$ for word operations) |
| $2^4$ Carry 2 | Set to one if carry, set to zero if no carry from the next most significant bit of operation. ($2^6$ for byte one $2^{14}$ for word operations). |
| $2^1$ NZD | Set to zero if result of the operation is a zero, set to one if result is non-zero. |

| W Bit | Action On |
|---|---|
| $2^6$ Bit Operation Test | Set to zero if most significant bit of result is zero. Set to one if most significant bit of result is one. ($2^7$ of for byte and $2^{15}$ for word operations). |

Note: 1. This instruction places the difference in the subtrahend rather than the minuend. However, the Register to Register subtract instruction places the difference in the minuend.

2. If S = 1 - $2^0$ of the R field and MA register is ignored and the full words are used for this operation.

WTM Write to Memory WTM

| F<br>Function Code | MA | I | S | R |
|---|---|---|---|---|
| 01000 | 3 Bits | 3 Bits | 1 Bit | 4 Bits |

$2^{15}$ $2^{11}$ $2^{10}$ $2^{8}$ $2^{7}$ $2^{5}$ $2^{4}$ $2^{3}$ $2^{0}$ Bit Position

Instruction Time - Byte or Word 3.6 us

This instruction stores the contents of a standard register to high speed memory. The contents of a register specified by the R field is stored at memory location specified by the word contents of the standard register specified by the MA field.

The S field specifies whether one byte or one word is stored. If S = 0, a byte is stored. If S = 1, a word is stored.

The I field specifies the amount of increment or decrement of the contents of the standard register specified by the MA field. The amount is specified in the I field as follows:

I FIELD

| 7 6 5 | INCR DEC |
|---|---|
| 0 0 0 | 0 |
| 0 0 1 | +1 |
| 0 1 0 | +2 |
| 0 1 1 | +4 |
| 1 0 0 | +6 |
| 1 0 1 | -1 |
| 1 1 0 | -2 |
| 1 1 1 | -4 |

WTM Continued

The setting of the Program State (X) Register Bit $2^0$ and $2^1$ conditions the R and MA fields as follows:

R FIELD

| $2^3$ $2^2$ $2^1$ $2^0$ | MATRIX REG XI = 0 | MATRIX REG XI = 1 | SPECIAL REGISTER (RP) |
|---|---|---|---|
| 0 0 0 0 | A0 | I0 | BIN0 |
| 0 0 0 1 | A1 | I1 | |
| 0 0 1 0 | B0 | J0 | BIN1 |
| 0 0 1 1 | B1 | J1 | |
| 0 1 0 0 | C0 | K0 | BOUT2 |
| 0 1 0 1 | C1 | K1 | |
| 0 1 1 0 | D0 | L0 | BOUT1 |
| 0 1 1 1 | D1 | L1 | |
| 1 0 0 0 | E0 | M0 | DAD |
| 1 0 0 1 | E1 | M1 | |
| 1 0 1 0 | F0 | N0 | W |
| 1 0 1 1 | F1 | N1 | |
| 1 1 0 0 | G0 | $\bar{O}0$ | X |
| 1 1 0 1 | G1 | $\bar{O}1$ | |
| 1 1 1 0 | H0 | P0 | |
| 1 1 1 1 | H1 | P1 | |

MA FIELD

| $2^{10}$ $2^9$ $2^8$ | XO = 0 | XO = 1 |
|---|---|---|
| 0 0 0 | A | I |
| 0 0 1 | B | J |
| 0 1 0 | C | K |
| 0 1 1 | D | L |
| 1 0 0 | E | M |
| 1 0 1 | F | N |
| 1 1 0 | G | $\bar{O}$ |
| 1 1 1 | H | P |

The Control Register (W) does not affect or is it modified by this instruction.

NOTE: If S = 1 - $2^0$ of the R field is ignored and $2^0$ of the MA register is ignored and the full word is stored in memory.

| F<br>Function Code | MA | I | S | R | | | |
|---|---|---|---|---|---|---|---|
| 01010 | 3 Bits | 3 Bits | X | X | X | X | |
| $2^{15}$ $2^{11}$ | $2^{10}$ $2^{8}$ | $2^{7}$ $2^{5}$ | $2^{4}$ | $2^{3}$ | $2^{2}$ | $2^{1}$ | $2^{0}$ |

Bit Position

Instruction Time - 3.6 us

This instruction provides the function of setting or resetting the memory protect bit ($2^{16}$) of a memory word. The MA fields give the location of the memory word. The S field has no effect on this instruction and $2^{0}$ of the MA field is ignored and a full word operation is performed. However, the $2^{0}$ position of the R field indicates set or reset as follows:

$2^{0} = 1$ Memory Protect Set
$2^{0} = 0$ Memory Protect Reset

The I field specifies the amount of increment or decrement of the standard register designated by the MA field. The amount is as follows:

IFIELD

| 7 6 5 | INCR DEC |
|---|---|
| 2 2 2 | |
| 0 0 0 | 0 |
| 0 0 1 | +1 |
| 0 1 0 | +2 |
| 0 1 1 | +4 |
| 1 0 0 | +6 |
| 1 0 1 | -1 |
| 1 1 0 | -2 |
| 1 1 1 | -4 |

MPSR Continued

The setting of the Program State Register (X) bit $2^0$ conditions MA fields as follows:

MA FIELD

| $2^{10}$ | $2^9$ | $2^8$ | X0 = 0 | X0 = 1 |
|---|---|---|---|---|
| 0 | 0 | 0 | A | I |
| 0 | 0 | 1 | B | J |
| 0 | 1 | 0 | C | K |
| 0 | 1 | 1 | D | L |
| 1 | 0 | 0 | E | M |
| 1 | 0 | 1 | F | N |
| 1 | 1 | 0 | G | $\overline{O}$ |
| 1 | 1 | 1 | H | P |

Note: This instruction has no effect on the data portion of the memory word. Addressing a memory word with the memory protect bit set with this instruction will not cause $2^5$ of the W (Control) Register to be set. Thus, the Control Register (W) setting has no initial effect nor is it modified by this instruction.

CMPR Compare RPCOM

(Register Perform - Compare)

| F Function Code | R1 | SF | S | R2 |
|---|---|---|---|---|
| 10110 | 4 Bits | 2 Bits | 1 Bit | 4 Bits |

$2^{15}$ $2^{11}$ $2^{10}$ $2^{7}$ $2^{6}$ $2^{5}$ $2^{4}$ $2^{3}$ $2^{0}$

Bit Position

Instruction Time - Byte Operation 1.8 us

Word Operation 2.7 us

This instruction performs a compare between two operands which are registers. The operands are not modified at termination of this instruction and the results of the compare are tested through the W (Control Register).

R1 • R2

The contents of the registers specified by the R1 and R2 fields are the operands. The results of the instruction modify the Control Register Bits by the below rules. (The initial setting of the W Register does not affect this instruction).

| W Register Bit | Action On |
|---|---|
| $2^{0}$ Carry 1 | Set to one if R1 operand is greater or equal to R2 operand and set to zero if less (Binary absolute). |
| $2^{1}$ NZD | Set to one if R1 operand is equal to R2 operand (Binary - absolute). |
| $2^{1}$ NZD | Two's complement (signed) comparison is one if not zero, zero if equal. |
| $2^{6}$ Bit Operation Test | Is zero if R1 operand is greater or equal to R2 operand and is one if less. |

and are interpreted as follows:

| CONTROL REGISTER (W) | |
|---|---|
| W0 | CARRY 1-INDICATES CARRY FROM($2^7$ OR $2^{15}$) OF ARITHMETIC OPERATION |
| W1 | NFD-INDICATES ARITHMETIC OPERATION RESULT WAS NOT ZERO |
| W2 | INDICATOR FOR PROGRAM USE |
| W3 | INDICATOR FOR PROGRAM USE |
| W4 | CARRY 2-INDICATES CARRY FROM($2^6$ OR $2^{14}$) OF ARITHMETIC OPERATION |
| W5 | INDICATOR FOR PROGRAM USE |
| W6 | BIT OP TEST-INDICATES RESULT OF BITOP BIT OR SIGN OF ARITHMETIC OPERATION |
| W7 | PROGRAM INDICATOR-SETS PI LIGHT ON CONSOLE |

| if | Then W bits are set as follows: |
|---|---|
| R1=R2 | $2^1$ of W = Ø (Binary) |
| R1≠R2 | $2^1$ of W = 1 (Binary) |
| R1≥R2 | $2^0$ of W = 1 (Binary) |
| R1<R2 | $2^0$ of W = Ø (Binary) |
| R1=R2 | $2^1$ of W = Ø (Signed) |
| R1≠R2 | $2^1$ of W = 1 (Signed) |
| R1≥R2 | $2^6$ of W = Ø (Signed) |
| R1<R2 | $2^6$ of W = 1 (Signed) |

The SF field indicates whether the register addresses are to be treated as standard or special register. This is indicated by setting the Sub-Function (SF) field as follows:

| SF Setting | | Action |
|---|---|---|
| $2^6$ | $2^5$ | |
| 0 | 0 | R1 . R2 |
| 0 | 1 | S . R2 |
| 1 | 0 | S . R2 |

Where S is the only one of the following valid registers for this instruction:

BIN0 BIN1
DAD
W
X

CMPR Continued

The S field indicates a byte (S = 0) or word (S = 1) operation.

When an R field designates a Standard Register, it is conditioned by the Program State (X) Register bit $2^1$ as follows:

R FIELDS

| R1 $2^{10}$ $2^{9}$ $2^{8}$ $2^{7}$ / R2 $2^{3}$ $2^{2}$ $2^{1}$ $2^{0}$ | MATRIX REG XI = 0 | MATRIX REG XI = 1 | SPECIAL REGISTER (RP) |
|---|---|---|---|
| 0 0 0 0 | A0 | I0 | BIN0 |
| 0 0 0 1 | A1 | I1 | |
| 0 0 1 0 | B0 | J0 | BIN1 |
| 0 0 1 1 | B1 | J1 | |
| 0 1 0 0 | C0 | K0 | BOUT2 |
| 0 1 0 1 | C1 | K1 | |
| 0 1 1 0 | D0 | L0 | BOUT1 |
| 0 1 1 1 | D1 | L1 | |
| 1 0 0 0 | E0 | M0 | DAD |
| 1 0 0 1 | E1 | M1 | |
| 1 0 1 0 | F0 | N0 | W |
| 1 0 1 1 | F1 | N1 | |
| 1 1 0 0 | G0 | $\bar{O}0$ | X |
| 1 1 0 1 | G1 | $\bar{O}1$ | |
| 1 1 1 0 | H0 | P0 | |
| 1 1 1 1 | H1 | P1 | |

Note if a Special Register is designated, $2^0$ and $2^7$ bits of the instruction are don't care cases.

NOTES:
1. When a Special Register is indicated, the S field of the instruction is ignored and the operation is byte only.
2. If S = 1, $2^0$ of the R2 and $2^7$ of the R1 fields are ignored and the full data words are used for this instruction.

ABR Add RPADD

(Register Perform - Add)

| F<br>Function Code | R1 | SF | S | R2 |
|---|---|---|---|---|
| 11101 | 4 Bits | 2 Bits | 1 Bit | 4 Bits |
| $2^{15}$ $2^{11}$ | $2^{10}$ $2^{7}$ | $2^{6}$ $2^{5}$ | $2^{4}$ | $2^{3}$ $2^{0}$ |

Bit Position

Instruction Time - Byte Operation 1.8 us
Word Operation 2.7 us

This instruction performs a binary add of two operands - both from registers. The result is stored at one of the registers. The contents of the registers indicated by the R1 and R2 registers are the operands. The result is stored in R1 or R2 depending upon the setting of the SF (sub-function) field. The SF field also indicates whether register addresses are to be interpreted as standard or special registers as follows:

| SF Setting | | Action |
|---|---|---|
| $2^{6}$ | $2^{5}$ | |
| 0 | 0 | R1 + R2 → R1 |
| 0 | 1 | S + R2 → R2 |
| 1 | 0 | S + R2 → S |

where S is only one of the following special registers for this instruction:

BIN 0 BIN 1
DAD
W
X

The S field indicates whether one byte or one word operations are to be performed. If S = 0, one byte operations are performed; and if S = 1, one word operations are performed.

ABR Continued

When an R field designates a standard register, it is conditioned by the X Register (Program State) bit $2^1$ as follows:

R FIELDS

| R1 $2^{10}$ $2^9$ $2^8$ $2^7$ | MATRIX REG X1 = | | SPECIAL REGISTER (RP) |
|---|---|---|---|
| R2 $2^3$ $2^2$ $2^1$ $2^0$ | 0 | 1 | |
| 0 0 0 0 | A0 | I0 | BIN0 |
| 0 0 0 1 | A1 | I1 | |
| 0 0 1 0 | B0 | J0 | BIN1 |
| 0 0 1 1 | B1 | J1 | |
| 0 1 0 0 | C0 | K0 | BOUT2 |
| 0 1 0 1 | C1 | K1 | |
| 0 1 1 0 | D0 | L0 | BOUT1 |
| 0 1 1 1 | D1 | L1 | |
| 1 0 0 0 | E0 | M0 | DAD |
| 1 0 0 1 | E1 | M1 | |
| 1 0 1 0 | F0 | N0 | W |
| 1 0 1 1 | F1 | N1 | |
| 1 1 0 0 | G0 | $\bar{O}$0 | X |
| 1 1 0 1 | G1 | $\bar{O}$1 | |
| 1 1 1 0 | H0 | P0 | |
| 1 1 1 1 | H1 | P1 | |

| CONTROL REGISTER (W) | |
|---|---|
| W0 | CARRY 1-INDICATES CARRY FROM ($2^7$ OR $2^{15}$) OF ARITHMETIC OPERATION |
| W1 | NZD-INDICATES ARITHMETIC OPERATION RESULT WAS NOT ZERO |
| W2 | INDICATOR FOR PROGRAM USE |
| W3 | INDICATOR FOR PROGRAM USE |
| W4 | CARRY 2-INDICATES CARRY FROM ($2^6$ OR $2^{14}$) OF ARITHMETIC OPERATION |
| W5 | INDICATOR FOR PROGRAM USE |
| W6 | BIT OP TEST-INDICATES RESULT OF BIT OP EQ OR SIGN OF ARITHMETIC OPERATION |
| W7 | PROGRAM INDICATOR-SETS PI LIGHT ON CONSOLE |

Note that if a special register is designated, the $2^0$ and $2^7$ bits of the instruction are don't care cases.

The initial setting of the W Register (Control) does not affect this instruction. However, the operation modifies bits of the W Register as follows:

| W Register Bit | Action On |
|---|---|
| $2^0$ Carry 1 | Set to one if carry, set to zero if no carry from most significant bit of operation. ($2^7$ for byte and $2^{15}$ for word operations). |
| $2^4$ Carry 2 | Set to one if carry, set to zero if no carry from next most significant bit of operation. ($2^6$ for byte and $2^{14}$ for word operations). |
| $2^1$ NZD | Set to zero if result of operation is a zero, set to one if result is non-zero. |

| W Register Bit | Action On |
|---|---|
| 2 Bit Operation Test | Set to zero if most significant bit (2 for byte and 2 for word operations) of result is zero. Set to one if most significant bit of result is one. |

NOTES: 1. When a Special Register is indicated for an R field, the S field is ignored and the operation is byte only.

2. If S = 1, $2^0$ of the R2 and $2^7$ of the R1 fields are ignored and the full data words are used for this instruction.

SBR Subtract
(Register Perform - Add 2's Complement)

RPADD2

| F<br>Function Code | R1 | SF | S | R2 |
|---|---|---|---|---|
| 10101 | 4 Bits | 2 Bits | 1 Bit | 4 Bits |
| $2^{15}$ $2^{11}$ | $2^{10}$ $2^{7}$ | $2^{6}$ $2^{5}$ | $2^{4}$ | $2^{3}$ $2^{0}$ |

Bit Position

Instruction Time - Byte Operation 1.8 us
Word Operation 2.7 us

This instruction performs a binary subtract of two operands, both from registers, and stores the result at one of the registers. The contents of the register indicated by the R1 field is the minuend and the contents of the register indicated by the R2 field is the subtrahend. The result is stored in R1 or R2 depending upon the setting of the Sub-Function (SF) field. The setting of the SF field also indicates whether register addresses are to be interpreted as standard or special register as follows:

| SF Setting | |
|---|---|
| $2^6$ | $2^5$ |
| 0 | 0 |
| 0 | 1 |
| 1 | 0 |

Action

R1 - R2 → R1
S - R2 → R2
S - R2 → S

where S is only one of the following special registers that are valid for this instruction:

BIN 0 BIN 1
DAD
W
X

The S field indicates a byte or word execution. If S = 0, a byte operation is performed and if S = 1, a word operation is performed.

When an R field designates a standard register, it is conditioned by the X (Program State) register bit $2^1$ as follows:

R FIELDS

| | 10 9 8 7 | MATRIX REG XI = | | SPECIAL REGISTER (RP) |
|---|---|---|---|---|
| R1 | 2 2 2 2 | 0 | 1 | |
| R2 | $2^3 2^2 2^1 2^0$ | | | |
| | 0 0 0 0 | A0 | I0 | BIN0 |
| | 0 0 0 1 | A1 | I1 | |
| | 0 0 1 0 | B0 | J0 | BIN1 |
| | 0 0 1 1 | B1 | J1 | |
| | 0 1 0 0 | C0 | K0 | BOUT2 |
| | 0 1 0 1 | C1 | K1 | |
| | 0 1 1 0 | D0 | L0 | BOUT1 |
| | 0 1 1 1 | D1 | L1 | |
| | 1 0 0 0 | E0 | M0 | DAD |
| | 1 0 0 1 | E1 | M1 | |
| | 1 0 1 0 | F0 | N0 | W |
| | 1 0 1 1 | F1 | N1 | |
| | 1 1 0 0 | G0 | $\bar{0}0$ | X |
| | 1 1 0 1 | G1 | $\bar{0}1$ | |
| | 1 1 1 0 | H0 | P0 | |
| | 1 1 1 1 | H1 | P1 | |

| CONTROL REGISTER (W) | |
|---|---|
| W0 | CARRY 1-INDICATES CARRY FROM ($2^7$ OR $2^{15}$) OF ARITHMETIC OPERATION |
| W1 | NZD-INDICATES ARITHMETIC OPERATION RESULT WAS NOT ZERO |
| W2 | INDICATOR FOR PROGRAM USE |
| W3 | INDICATOR FOR PROGRAM USE |
| W4 | CARRY 2-INDICATES CARRY FROM ($2^6$ OR $2^{14}$) OF ARITHMETIC OPERATION |
| W5 | INDICATOR FOR PROGRAM USE |
| W6 | BIT OP TEST-INDICATES RESULT OF BITOP BIT OR SIGN OF ARITHMETIC OPERATION |
| W7 | PROGRAM INDICATOR-SETS PI LIGHT ON CONSOLE |

Note that if a special register is designated, the $2^0$ and $2^7$ bits of the instructions are don't care cases.

The initial setting of the W Register (Control) does not affect this instruction. However, it does modify bits of the W Register as follows:

| W Register Bit | Action On |
|---|---|
| $2^0$ Carry 1 | Set to one if carry, set to zero if no carry from most significant bit of operation ($2^7$ for byte and $2^{15}$ for word operations). |
| $2^4$ Carry 2 | Set to one if carry, set to zero if no carry from next most significant bit ($2^6$ for byte and $2^{14}$ for word operations). |
| $2^1$ NZD | Set to zero if result of operation is a zero, set to one if result of operation is non-zero. |

| W Register Bit | Action On |
|---|---|
| $2^6$ Bit Operation Test | Set to zero if most significant of the result is zero and to one if most significant bit of result is a one ($2^7$ for byte and $2^{15}$ for word operations). |

NOTE: 1. Register to Register Subtract Difference replaced the minuend whereas Memory to Register Subtract Difference replaces the subtrahend.

2. When a Special Register is indicated for an R field, the S field is ignored and the operation is byte only.

3. If S = 1, $2^0$ of the R fields are ignored and the full data words are used for this instruction.

ABRC Add with Carry RPAC
(Register Perform - Add With Carry)

| F<br>Function Code | R1 | SF | S | R2 |
|---|---|---|---|---|
| 11111 | 4 Bits | 2 Bits | 1 Bit | 4 Bits |

$2^{15}$ $2^{11}$ $2^{10}$ $2^{7}$ $2^{6}$ $2^{5}$ $2^{4}$ $2^{3}$ $2^{0}$

Bit Position

Instruction Time - Byte Operation 1.8 us
Word Operation 2.7 us

This instruction performs a binary add of two operands from registers, plus an initial carry setting, and stores the result at one of the registers. The contents of the registers specified in R1 and R2 fields are the operands. The contents of carry 1 ($2^0$ of the W Register) provides the initial carry. The Result is stored in R1 or R2 depending upon the setting of the Sub-Function (SF) field. The SF field also indicates whether or not register addresses are to be interpreted as standard or special registers. This is indicated as follows:

| SF Setting | | Action |
|---|---|---|
| $2^6$ | $2^5$ | |
| 0 | 0 | R1 + R2 + W0 → R1 |
| 0 | 1 | S + R2 + W0 → R2 |
| 1 | 0 | S + R2 + W0 → S |

where S is only one of the following special registers that are valid for this instruction:

BIN 0 BIN 1
DAD
W
X

The S field indicates a byte or word operation. If S = 0, a byte operation is performed and if S = 1, a word operation is executed.

ABRC Continued

When an R field designates a standard register, it is conditioned by the X (Program State) register bit $2^1$ as follows:

R FIELDS

| R1 / R2 | $2^{10}$ $2^9$ $2^8$ $2^7$ | MATRIX REG XI = 0 | MATRIX REG XI = 1 | SPECIAL REGISTER (RP) |
|---|---|---|---|---|
| | $2^5$ $2^2$ $2^1$ $2^0$ | | | |
| | 0 0 0 0 | A0 | I0 | BIN0 |
| | 0 0 0 1 | A1 | I1 | |
| | 0 0 1 0 | B0 | J0 | BIN1 |
| | 0 0 1 1 | B1 | J1 | |
| | 0 1 0 0 | C0 | K0 | BOUT2 |
| | 0 1 0 1 | C1 | K1 | |
| | 0 1 1 0 | D0 | L0 | BOUT1 |
| | 0 1 1 1 | D1 | L1 | |
| | 1 0 0 0 | E0 | M0 | DAD |
| | 1 0 0 1 | E1 | M1 | |
| | 1 0 1 0 | F0 | N0 | W |
| | 1 0 1 1 | F1 | N1 | |
| | 1 1 0 0 | G0 | $\bar{O}0$ | X |
| | 1 1 0 1 | G1 | $\bar{O}1$ | |
| | 1 1 1 0 | H0 | P0 | |
| | 1 1 1 1 | H1 | P1 | |

| CONTROL REGISTER (W) | |
|---|---|
| W0 | CARRY 1 - INDICATES CARRY FROM (2TO 2[5]) OF ARITHMETIC OPERATION |
| W1 | NZD - INDICATES ARITHMETIC OPERATION RESULT WAS NOT ZERO |
| W2 | INDICATOR FOR PROGRAM USE |
| W3 | INDICATOR FOR PROGRAM USE |
| W4 | CARRY 2 - INDICATES CARRY FROM (2[6] OR 2[14]) OF ARITHMETIC OPERATION |
| W5 | INDICATOR FOR PROGRAM USE |
| W6 | BIT OR TEST - INDICATES RESULT OF BITOP 21 OR SIGN OF ARITHMETIC OPERATION |
| W7 | PROGRAM INDICATOR - SETS PI LIGHT ON CONSOLE |

Note if a special register is designated, $2^0$ and $2^7$ bits of the instruction are don't care cases.

The initial setting of the W (Control) Register affects the operation as follows:

| W Register Bit | Action On |
|---|---|
| $2^0$ Carry 1 | The setting of this position is used as a carry into $2^0$ position of the operation. |
| $2^4$ Carry 2 | Set to one if carry, set to zero if no carry from next most significant bit of operation ($2^6$ for byte and $2^{14}$ for word operations). |
| $2^1$ NZD | If result of operation is zero, this bit is set to zero, if non-zero, it is set to one. |

| W Register Bit | Action On |
|---|---|
| $2^6$ Bit Operation Test | Set to zero if most significant bit of result is zero, set to one if not zero ($2^7$ for byte and $2^{15}$ for word operations). |

NOTE: 1. When a Special Register is indicated for an R field, the S field is ignored and the operation is byte only.

2. If S = 1, $2^0$ of the R2 and $2^7$ of the R1 fields are ignored and the full data words are used for this instruction.

SBRC Subtract With Carry RPSC
(Register Perform - Subtract With Carry)

| F<br>Function Code | R1 | SF | S | R2 |
|---|---|---|---|---|
| 10111 | 4 Bits | 2 Bits | 1 Bit | 4 Bits |

$2^{15}$ $2^{11}$ $2^{10}$ $2^{7}$ $2^{6}$ $2^{5}$ $2^{4}$ $2^{3}$ $2^{0}$

Bit Position

Instruction Time - Byte Operation 1.8 us
Word Operation 2.7 us

SBRC performs a binary subtract between two operands from registers only, adding an initial carry setting, and stores the result at one of the registers. The contents of the R1 register is the minuend. The content of the R2 register is the subtrahend. The contents of carry 1 ($2^0$ of the W Register) provides the initial carry. The result is stored at the R1 or R2 register depending upon the setting of the SF (Sub-Function) field. The SF field also indicates whether or not register addresses are to be interpreted as standard or special registers. This is indicated as follows:

| SF Setting | | Action |
|---|---|---|
| $2^6$ | $2^5$ | |
| 0 | 0 | R1 - R2 + W0 → R1 |
| 0 | 1 | S - R2 + W0 → R2 |
| 1 | 0 | S - R2 + W0 → S |

where S is only one of the following special registers that are valid for this instruction:

BIN0 BIN1
DAD
W
X

The S field indicates a byte (S = 0) or word (S = 1) operation.

When an R field designates a standard register, it is conditioned by the Program State (X) Register bit $2^1$ as follows:

| CONTROL REGISTER (W) | |
|---|---|
| W0 | CARRY1-INDICATES CARRY FROM(27 OR 215) OF ARITHMETIC OPERATION |
| W1 | INFO-INDICATES ARITHMETIC OPERATION RESULT WAS NOT ZERO |
| W2 | INDICATOR FOR PROGRAM USE |
| W3 | INDICATOR FOR PROGRAM USE |
| W4 | CARRY0-INDICATES CARRY FROM(26 OR 214) OF ARITHMETIC OPERATION |
| W5 | INDICATOR FOR PROGRAM USE |
| W6 | BITOPTEST-INDICATES RESULT OF BITOP OR SIGN OF ARITHMETIC OPERATION |
| W7 | PROGRAM INDICATOR-SETS PI LIGHT ON CONSOLE |

R FIELDS

| R1 $2^{10}2^9 2^8 2^7$ / R2 $2^3 2^2 2^1 2^0$ | MATRIX REG X1 = 0 | 1 | SPECIAL REGISTER (RP) |
|---|---|---|---|
| 0 0 0 0 | A0 | I0 | BIN0 |
| 0 0 0 1 | A1 | I1 | |
| 0 0 1 0 | B0 | J0 | BIN1 |
| 0 0 1 1 | B1 | J1 | |
| 0 1 0 0 | C0 | K0 | BOUT2 |
| 0 1 0 1 | C1 | K1 | |
| 0 1 1 0 | D0 | L0 | BOUT1 |
| 0 1 1 1 | D1 | L1 | |
| 1 0 0 0 | E0 | M0 | DAD |
| 1 0 0 1 | E1 | M1 | |
| 1 0 1 0 | F0 | N0 | W |
| 1 0 1 1 | F1 | N1 | |
| 1 1 0 0 | G0 | $\bar{0}0$ | X |
| 1 1 0 1 | G1 | $\bar{0}1$ | |
| 1 1 1 0 | H0 | P0 | |
| 1 1 1 1 | H1 | P1 | |

Note if a special register is designated, $2^0$ and $2^7$ bits of the instruction are don't care cases.

The initial setting of the W (Control) Register affects the operation as follows:

| W Register Bit | Action On |
|---|---|
| $2^0$ Carry 1 | The setting of this position is used as a carry into $2^0$ position of the operation. |

The instruction modifies W Register Bits as follows:

| | |
|---|---|
| $2^0$ Carry 1 | Set to one if carry, set to zero if no carry from most significant bit of operation ($2^7$ for byte and $2^{15}$ for word operations). |

SBRC Continued

| W Register Bit | Action On |
|---|---|
| $2^4$ Carry 2 | Set to one if carry, set to zero if no carry from next most significant bit of operation ($2^6$ for byte and $2^{14}$ for word operation). |
| $2^1$ NZD | If result of SBRC is zero, this bit remains unchanged from initial setting. If the result of SBRC is not zero, it is set to one. |
| $2^6$ Bit Operation Test | Set to zero if most significant bit of result is zero and set to one if non-zero ($2^7$ for byte and $2^{15}$ for word operations). |

NOTE: 1. Register to Register Subtract places result in minuend and Memory to Register Subtract places result in subtrahend.

2. When a Special Register is indicated for an R field, the S field of the instruction is ignored and the operation is byte only.

3. If S = 1, $2^0$ of the R2 and $2^7$ of the R1 fields are ignored and the full data words are used for this instruction.

ANDR And RPAND
(Register Perform - And)

| F<br>Function Code | R1 | SF | S | R2 |
|---|---|---|---|---|
| 10100 | 4 Bits | 2 Bits | 1 Bit | 4 Bits |

$2^{15}$ $2^{11}$ $2^{10}$ $2^{7}$ $2^{6}$ $2^{5}$ $2^{4}$ $2^{3}$ $2^{0}$

Bit Position

Instruction Time - Byte Operation 1.8 us
Word Operation 2.7 us

ANDR performs a logical "And" between two operands which are registers, and stores the result at one of the registers. The contents of the registers indicated by the R1 field and R2 field are the operands. The result is stored at the R1 or R2 register depending upon the setting of the SF (Sub-Function) field. The SF field also indicates whether a Standard or Special Register is to be interpreted by ANDR. This is indicated as follows:

| SF Setting | | Action |
|---|---|---|
| $2^6$ | $2^5$ | |
| 0 | 0 | R1 anded R2 → R1 |
| 0 | 1 | S anded R2 → R2 |
| 1 | 0 | S anded R2 → S |

where S above is only of the special registers that are valid for this instruction:

BIN0 BIN1
DAD
W
X

The S field of the instruction indicates a byte (S=0) or word (S=1) operation.

When an R field designates a standard register, it is conditioned by the Program State (X) Register $2^1$ bit as follows:

| CONTROL REGISTER (W) | |
|---|---|
| W0 | CARRY1-INDICATES CARRY FROM (7 OR $2^{15}$) OF ARITHMETIC OPERATION |
| W1 | NZD-INDICATES ARITHMETIC OPERATION RESULT WAS NOT ZERO |
| W2 | INDICATOR FOR PROGRAM USE |
| W3 | INDICATOR FOR PROGRAM USE |
| W4 | CARRY2-INDICATES CARRY FROM ($2^6$ OR $2^{14}$) OF ARITHMETIC OPERATION |
| W5 | INDICATOR FOR PROGRAM USE |
| W6 | BITOPTEST-INDICATES RESULT OF BITOP BIT OR SIGN OF ARITHMETIC OPERATION |
| W7 | PROGRAM INDICATOR-SETS PI LIGHT ON CONSOLE |

R FIELDS

| R1 $2^{10}$ $2^9$ $2^8$ $2^7$ | R2 $2^3$ $2^2$ $2^1$ $2^0$ | MATRIX REG XI = 0 | MATRIX REG XI = 1 | SPECIAL REGISTER (RP) |
|---|---|---|---|---|
| 0 0 0 0 | | A0 | I0 | BIN0 |
| 0 0 0 1 | | A1 | I1 | |
| 0 0 1 0 | | B0 | J0 | BIN1 |
| 0 0 1 1 | | B1 | J1 | |
| 0 1 0 0 | | C0 | K0 | BOUT2 |
| 0 1 0 1 | | C1 | K1 | |
| 0 1 1 0 | | D0 | L0 | BOUT1 |
| 0 1 1 1 | | D1 | L1 | |
| 1 0 0 0 | | E0 | M0 | DAD |
| 1 0 0 1 | | E1 | M1 | |
| 1 0 1 0 | | F0 | N0 | W |
| 1 0 1 1 | | F1 | N1 | |
| 1 1 0 0 | | G0 | $\bar{O}0$ | X |
| 1 1 0 1 | | G1 | $\bar{O}1$ | |
| 1 1 1 0 | | H0 | P0 | |
| 1 1 1 1 | | H1 | P1 | |

Note if a Special Register is designated, $2^0$ and $2^7$ bits of the instruction are don't care cases.

The initial setting of the W (Control) Register is not affected by this instruction. However, ANDR affects the NZD bit ($2^1$) of the W Register. If the result of the instruction is zero, set NZD to zero, otherwise set to one. Thus,

$2^1$ (NZD) of W = 0 if result in R = 0
$2^1$ (NZD) of W = 1 if result in R $\neq$ 0

NOTES:
1. When a Special Register is indicated for an R field, the S field is ignored and the operation is <u>byte</u> only.
2. If S=1, $2^0$ of the R2 and $2^7$ of the R1 fields are ignored and the full data words are used for this function.

SRST Standard Register Set Transfer RMXF
(Matrix to Matrix Transfer Across X1 Bit Boundary)

| F<br>Function Code | R1 | SF | S | R2 |
|---|---|---|---|---|
| 01001 | 4 Bits | 2 Bits | 1 Bit | 4 Bits |

$2^{15}$ $2^{11}$ $2^{10}$ $2^{7}$ $2^{6}$ $2^{5}$ $2^{4}$ $2^{3}$ $2^{0}$

Bit Position

Instruction Time - 1.8 us

This instruction performs a transfer between two registers which can be of different Standard Register Sets. The R2 register is the source and the R1 register is the destination.

R1 ⟶ R2

The SF field is not standard for this instruction but has the following meaning for SRST.

| SF EFFECT | | | | |
|---|---|---|---|---|
| $2^6$ | $2^5$ | X1 | R1 (DEST) | R2 (SOURCE) |
| 0 | 0 | 0 | A ⟶ H | A ⟶ H |
| 0 | 1 | 0 | A ⟶ H | I ⟶ P |
| 1 | 0 | 0 | I ⟶ P | A ⟶ H |
| 1 | 1 | 0 | I ⟶ P | I ⟶ P |
| 0 | 0 | 1 | I ⟶ P | I ⟶ P |
| 0 | 1 | 1 | I ⟶ P | A ⟶ H |
| 1 | 0 | 1 | A ⟶ H | I ⟶ P |
| 1 | 1 | 1 | A ⟶ H | A ⟶ H |

Note the Program State Register (X) Bit 2 also affects the SF field. This is interpreted as follows:

SRST Continued

| SF Setting | |
|---|---|
| $2^6$ | $2^5$ |
| 0 | 0 |
| 0 | 1 |
| 1 | 0 |
| 1 | 1 |

| Interpretation of | |
|---|---|
| R1 | R2 |
| Current State ← | Current State |
| Current State ← | Other State |
| Other State ← | Current State |
| Other State ← | Other State |

When $2^1$ of X Register = 0
Current State = Register Set 1 A0A1 through H0H1
Other State = Register Set 2 I0I1 through P0P1

When $2^1$ of X Register = 1, the sets are reversed.

The S field of the instruction indicates a byte (S=0) or word (S=1) operation.

The R fields are specified as follows:

R FIELDS

| R1 | | MATRIX REG XI = | |
|---|---|---|---|
| R2 | $2^{10}\ 2^9\ 2^8\ 2^7$ | | |
| | $2^3\ 2^2\ 2^1\ 2^0$ | 0 | 1 |
| | 0 0 0 0 | A0 | I0 |
| | 0 0 0 1 | A1 | I1 |
| | 0 0 1 0 | B0 | J0 |
| | 0 0 1 1 | B1 | J1 |
| | 0 1 0 0 | C0 | K0 |
| | 0 1 0 1 | C1 | K1 |
| | 0 1 1 0 | D0 | L0 |
| | 0 1 1 1 | D1 | L1 |
| | 1 0 0 0 | E0 | M0 |
| | 1 0 0 1 | E1 | M1 |
| | 1 0 1 0 | F0 | N0 |
| | 1 0 1 1 | F1 | N1 |
| | 1 1 0 0 | G0 | $\bar{O}$0 |
| | 1 1 0 1 | G1 | $\bar{O}$1 |
| | 1 1 1 0 | H0 | P0 |
| | 1 1 1 1 | H1 | P1 |

Note that this instruction does not manipulate any of the special registers.

The W (Control) Register does not affect nor is it affected by this instruction.

NOTES:
1. If S=1, 2 of R2 and 2 of R1 fields are ignored and full words (16 bits) are transferred.
2. If S=0, odd addresses transfer the low order byte and even the high order byte.

TRR Transfer RPXF
(Register to Register Transfer)

| F<br>Function Code | R1 | SF | S | R2 |
|---|---|---|---|---|
| 01011 | 4 Bits | 2 Bits | 1 Bit | 4 Bits |
| $2^{15}$ $2^{11}$ | $2^{10}$ $2^{7}$ | $2^{6}$ $2^{5}$ | $2^{4}$ | $2^{3}$ $2^{0}$ |

Bit Positions

Instruction Time - Byte or Word Operation - 1.8 us

This instruction executes a transfer between two registers. The register indicated by the R2 field is the source and the register designated by the R1 field is the destination when SF=0. However, the Sub-Function field also designates standard or special registers. This is indicated as follows:

| SF Setting | | Action |
|---|---|---|
| $2^6$ | $2^5$ | |
| 0 | 0 | R2 → R1 |
| 0 | 1 | S → R2 |
| 1 | 0 | S → R1 |

Where S is one of the following special registers that are valid for this instruction:

BIN0 BIN1
BOUT1 BOUT2
DAD
W
X

The S field of the instruction indicates a byte (S=0) or word (S=1) operation.

When an R field designates a standard register, it is conditioned by the Program State (X) Register $2^1$ bit as follows:

| CONTROL REGISTER (W) | |
|---|---|
| W0 | CARRY 1-INDICATES CARRY FROM ($2^7$ OR $2^{15}$) OF ARITHMETIC OPERATION |
| W1 | NEQ0-INDICATES ARITHMETIC OPERATION RESULT WAS NOT ZERO |
| W2 | INDICATOR FOR PROGRAM USE |
| W3 | INDICATOR FOR PROGRAM USE |
| W4 | CARRY 2-INDICATES CARRY FROM ($2^6$ OR $2^{14}$) OF ARITHMETIC OPERATION |
| W5 | INDICATOR FOR PROGRAM USE |
| W6 | BIT OP TEST-INDICATES RESULT OF BIT OP PI OR SIGN OF ARITHMETIC OPERATION |
| W7 | PROGRAM INDICATOR-SETS PI LIGHT ON CONSOLE |

R FIELDS

| R1 | | | | | MATRIX REG X1 = | | SPECIAL REGISTER (RP) |
|---|---|---|---|---|---|---|---|
| R2 | $2^3$ | $2^2$ | $2^1$ | $2^0$ | 0 | 1 | |
| | 0 | 0 | 0 | 0 | A0 | I0 | BIN0 |
| | 0 | 0 | 0 | 1 | A1 | I1 | |
| | 0 | 0 | 1 | 0 | B0 | J0 | BIN1 |
| | 0 | 0 | 1 | 1 | B1 | J1 | |
| | 0 | 1 | 0 | 0 | C0 | K0 | BOUT2 |
| | 0 | 1 | 0 | 1 | C1 | K1 | |
| | 0 | 1 | 1 | 0 | D0 | L0 | BOUT1 |
| | 0 | 1 | 1 | 1 | D1 | L1 | |
| | 1 | 0 | 0 | 0 | E0 | M0 | DAD |
| | 1 | 0 | 0 | 1 | E1 | M1 | |
| | 1 | 0 | 1 | 0 | F0 | N0 | W |
| | 1 | 0 | 1 | 1 | F1 | N1 | |
| | 1 | 1 | 0 | 0 | G0 | $\bar{0}0$ | X |
| | 1 | 1 | 0 | 1 | G1 | $\bar{0}1$ | |
| | 1 | 1 | 1 | 0 | H0 | P0 | |
| | 1 | 1 | 1 | 1 | H1 | P1 | |

Note if a special register is designated, $2^0$ and $2^7$ bits of the instruction are don't care cases.

The W (Control) Register is not affected nor does it affect this instruction.

NOTE: 1. When a Special Register is indicated for an R field, the S field is ignored and the operation byte oriented.

2. If S=1, $2^0$ of R2 and $2^7$ of R1 fields are ignored and full data words (16 bits) are used for this instruction.

XORR Exclusive Or RPEXO
(Register Perform - Exclusive Or)

| F<br>Function Code | R1 | SF | S | R2 |
|---|---|---|---|---|
| 11100 | 4 Bits | 2 Bits | 1 Bit | 4 Bits |
| $2^{15}$ $2^{11}$ | $2^{10}$ $2^{7}$ | $2^{6}$ $2^{5}$ | $2^{4}$ | $2^{3}$ $2^{0}$ |

Bit Positions

Instruction Time - Byte Operation 1.8 us
Word Operation 2.7 us

This instruction performs a logical "exclusive or" between two register operands and stores the result in one of the registers. The contents of the R1 and R2 registers are the operands. The result is stored at the R1 or R2 register depending upon the SF setting. The Sub-Function (SF) field also indicates whether special registers are used. This is specified as follows:

| SF Setting | | Action |
|---|---|---|
| $2^{6}$ | $2^{5}$ | |
| 0 | 0 | R1 Xor R2 → R1 |
| 0 | 1 | S Xor R2 → R2 |
| 1 | 0 | S Xor R2 → S |

Where S is one of the following valid special registers for this instruction:

BIN0 BIN1
DAD
W
X

The S field of the instruction indicates a byte (S=0) or word (S=1) operation.

When an R field designates a standard register, it is conditioned by the Program State (X) register bit $2^1$ as follows:

| CONTROL REGISTER (W) | |
|---|---|
| W0 | CARRY-INDICATES CARRY FROM (TO) $2^{15}$ OF ARITHMETIC OPERATION |
| W1 | NZD-INDICATES ARITHMETIC OPERATION RESULT WAS NOT ZERO |
| W2 | INDICATOR FOR PROGRAM USE |
| W3 | INDICATOR FOR PROGRAM USE |
| W4 | CARRY-INDICATES CARRY FROM ($2^6$ OR $2^{14}$) OF ARITHMETIC OPERATION |
| W5 | INDICATOR FOR PROGRAM USE |
| W6 | ETYOPTEST-INDICATES RESULT OF BITOP BIT OR SIGN OF ARITHMETIC OPERATION |
| W7 | PROGRAM INDICATOR-SETS PI LIGHT ON CONSOLE |

R FIELDS

| R1 / R2 | $2^{10}$ $2^9$ $2^8$ $2^7$ | $2^3$ $2^2$ $2^1$ $2^0$ | MATRIX REG XI = 0 | MATRIX REG XI = 1 | SPECIAL REGISTER (RP) |
|---|---|---|---|---|---|
| | 0 0 0 0 | | A0 | I0 | BIN0 |
| | 0 0 0 1 | | A1 | I1 | |
| | 0 0 1 0 | | B0 | J0 | BIN1 |
| | 0 0 1 1 | | B1 | J1 | |
| | 0 1 0 0 | | C0 | K0 | BOUT2 |
| | 0 1 0 1 | | C1 | K1 | |
| | 0 1 1 0 | | D0 | L0 | BOUT1 |
| | 0 1 1 1 | | D1 | L1 | |
| | 1 0 0 0 | | E0 | M0 | DAD |
| | 1 0 0 1 | | E1 | M1 | |
| | 1 0 1 0 | | F0 | N0 | W |
| | 1 0 1 1 | | F1 | N1 | |
| | 1 1 0 0 | | G0 | $\bar{O}0$ | X |
| | 1 1 0 1 | | G1 | $\bar{O}1$ | |
| | 1 1 1 0 | | H0 | P0 | |
| | 1 1 1 1 | | H1 | P1 | |

Note if a special register is designated, $2^1$ and $2^7$ bits of the instruction are don't care cases.

The initial setting of the Control (W) Register does not affect this instruction. However, Exclusive Or modifies the NZD ($2^1$) bit of the W Register. NZD is set to zero if the result is zero and to ones if the result is not zero. Thus,

NZD ($2^1$) of W Register = 0 if Result = 0
NZD ($2^1$) of W Register = 1 if Result $\neq$ 0

NOTE: 1. When a Special Register is indicated for an R field, the S field is ignored and the operation is byte oriented.

2. If S=1, $2^0$ of R2 and $2^7$ of R1 fields are ignored and full data words (16 bits) are used for this instruction.

ORR Or

(Register Perform - Or) RPOR

| F | | | | |
|---|---|---|---|---|
| Function Code | R1 | SF | S | R2 |
| 11110 | 4 Bits | 2 Bits | 1 Bit | 4 Bits |
| $2^{15}$ $2^{11}$ | $2^{10}$ $2^{7}$ | $2^{6}$ $2^{5}$ | $2^{4}$ | $2^{3}$ $2^{0}$ |

Bit Positions

Instruction Time - Byte Operation 1.8 us
Word Operation 2.7 us

This instruction performs a logic "or" between two operands from registers and stores the result in one of the registers. The contents of the R1 and R2 registers are the operands and the result is stored at R1 or R2 depending upon the SF setting. The SF (Sub-Function) field also indicates whether the register addresses are interpreted as standard or special register. This is specified as follows:

| SF Setting | | Action |
|---|---|---|
| $2^6$ | $2^5$ | |
| 0 | 0 | R1 or R2 → R1 |
| 0 | 1 | S or R2 → R2 |
| 1 | 0 | S or R2 → S |

Where S is only one of the following valid special registers for this instruction:

BINO BIN
DAD
W
X

The S field indicates a byte (S=0) or word (S=1) operation.

When an R field designates a standard register, it is conditioned by the Program State (X) Register bit $2^1$ as follows:

| CONTROL REGISTER (W) | |
|---|---|
| W0 | CARRY-INDICATES CARRY FROM(2^7 OR 2^15) OF ARITHMETIC OPERATION |
| W1 | NZD-INDICATES ARITHMETIC OPERATION RESULT WAS NOT ZERO |
| W2 | INDICATOR FOR PROGRAM USE |
| W3 | INDICATOR FOR PROGRAM USE |
| W4 | CARRY-INDICATES CARRY FROM(2^6 OR 2^14) OF ARITHMETIC OPERATION |
| W5 | INDICATOR FOR PROGRAM USE |
| W6 | BIT OR TEST-INDICATES RESULT OF BIT OP AT OR SIGN OF ARITHMETIC OPERATION |
| W7 | PROGRAM INDICATOR-SETS PI LIGHT ON CONSOLE |

R FIELDS

| R1 / R2 | MATRIX REG XI = | | SPECIAL REGISTER (RP) |
|---|---|---|---|
| $2^{10}\ 2^9\ 2^8\ 2^7$ / $2^3\ 2^2\ 2^1\ 2^0$ | 0 | 1 | |
| 0 0 0 0 | A0 | I0 | BIN0 |
| 0 0 0 1 | A1 | I1 | |
| 0 0 1 0 | B0 | J0 | BIN1 |
| 0 0 1 1 | B1 | J1 | |
| 0 1 0 0 | C0 | K0 | BOUT2 |
| 0 1 0 1 | C1 | K1 | |
| 0 1 1 0 | D0 | L0 | BOUT1 |
| 0 1 1 1 | D1 | L1 | |
| 1 0 0 0 | E0 | M0 | DAD |
| 1 0 0 1 | E1 | M1 | |
| 1 0 1 0 | F0 | N0 | W |
| 1 0 1 1 | F1 | N1 | |
| 1 1 0 0 | G0 | $\bar{O}0$ | X |
| 1 1 0 1 | G1 | $\bar{O}1$ | |
| 1 1 1 0 | H0 | P0 | |
| 1 1 1 1 | H1 | P1 | |

Note if a special register is designated, $2^0$ and $2^7$ bits of the instruction are don't care cases.

The initial setting of the Control (W) Register does not affect this instruction. However ORR modifies the NZD ($2^1$) bit of the W Register. NAD is set to zero if result is zero and set to one if it is not. Thus,

NZD ($2^1$) of W Register = 0 if Result = 0
NZD ($2^1$) of W Register = 1 if Result $\neq$ 0

NOTE: 1. When a Special Register is indicated for an R field, the S field is ignored and the operation is byte only.

2. If S=1, $2^0$ of the R2 and $2^7$ of the R1 fields are ignored and the full data words are used for this instruction.

TAB Test and Branch
(Test and Branch)

TBR

| F | T | B | ± |
|---|---|---|---|
| Function Code | | | |
| 00100 | 4 Bits | 6 Bits | 1 Bit |

$2^{15}$ $2^{11}$ $2^{10}$ $2^{7}$ $2^{6}$ $2^{1}$ $2^{0}$

Bit Position

Instruction Time - Branch 1.8 us
No Branch 1.8 us

This instruction performs a specified test. If the test is true, a branch is taken; if not true, the next instruction in sequence is taken.

The Test (T) field designates the following tests:

T FIELD

| $2^{10}$ $2^{9}$ $2^{8}$ $2^{7}$ | TBR | |
|---|---|---|
| 0 0 0 0 | W0 = 1 | |
| 0 0 0 1 | W1 = 1 | |
| 0 0 1 0 | W2 = 1 | |
| 0 0 1 1 | W3 = 1 | |
| 0 1 0 0 | W4 = 1 | |
| 0 1 0 1 | W5 = 1 | |
| 0 1 1 0 | W6 = 1 | |
| 0 1 1 1 | W7 = 1 | |
| 1 0 0 0 | W0 = 0 | |
| 1 0 0 1 | W1 = 0 | |
| 1 0 1 0 | B.P. SWITCH | TEST BREAKPOINT SWITCH |
| 1 0 1 1 | W0 ≠ W4 | |
| 1 1 0 0 | INTERRUPT | TEST CLASS I - BRANCH IF TRUE |
| 1 1 0 1 | INTERRUPT-PS2 | TEST CLASS I - SET P.S. 2 IF TRUE |
| 1 1 1 0 | | NOT USED |
| 1 1 1 1 | | NOT USED |

Note that test patterns 1110 and 1111 are not utilized and a no-branch (next instruction in sequence) will be executed.

| CONTROL REGISTER (W) | |
|---|---|
| W0 | CARRY1-INDICATES CARRY FROM(2$^0$ OR 2$^{15}$) OF ARITHMETIC OPERATION |
| W1 | NZ1D-INDICATES ARITHMETIC OPERATION RESULT WAS NOT ZERO |
| W2 | INDICATOR FOR PROGRAM USE |
| W3 | INDICATOR FOR PROGRAM USE |
| W4 | CARRY2-INDICATES CARRY FROM(2$^0$ OR 2$^{15}$) OF ARITHMETIC OPERATION |
| W5 | INDICATOR FOR PROGRAM USE |
| W6 | BITOPTEST-INDICATES RESULT OF BITOP BIT OR SIGN OF ARITHMETIC OPERATION |
| W7 | PROGRAM INDICATOR-SETS PI LIGHT ON CONSOLE |

The Branch Field indicates an increment or decrement of 0 to 63 words from the address of the next instruction in sequence.

| Branch Field Bits | | | | | | | Action |
|---|---|---|---|---|---|---|---|
| if | | | $2^0 = 0$ | | | | increment |
| | | | $2^0 = 1$ | | | | decrement |
| | | | and | | | | No. of Words |
| $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | | |
| 0 | 0 | 0 | 0 | 0 | 0 | | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | | 2 |
| 0 | 0 | 0 | 0 | 1 | 1 | | 3 |
| | | | | | | thru | |
| 1 | 1 | 1 | 1 | 1 | 0 | | 62 |
| 1 | 1 | 1 | 1 | 1 | 1 | | 63 |

TAB Continued

Since the increment or decrement is made to BIC (Basic Instruction Counter) when positioned at the next instruction in sequence, a zero quantity will take the next instruction in sequence.

The X (Program State) Register Bit $2^0$ (Basic Instruction Indicator) determines which BIC will be affected.

when

| | | | |
|---|---|---|---|
| X2 = 0 | BIC | H0H1 | is affected |
| X2 = 1 | BIC | P0P1 | is affected |

The W (Control) Register has no affect other than the specific tests as indicated and is not affected by this instruction.

NOTE: The increment/decrement is by words and not bytes.

SFT Shift (Register Shift) RS

| F Function Code | SHIFT | Not Used | | | S | R |
|---|---|---|---|---|---|---|
| 00111 | 4 Bits | X | X | X | 1 Bit | 4 Bits |
| $2^{15}$ $2^{11}$ | $2^{10}$ $2^{8}$ | $2^{7}$ | $2^{6}$ | $2^{5}$ | $2^{4}$ | $2^{3}$ $2^{0}$ |

Bit Position

Instruction Time - Byte or Word Operation 1.8 us
(Shift one Bit only)

This instruction shifts left or right the contents of a byte or word size standard register by one bit. The instruction may indicate a previous stored carry in or stored carry out.

The R field designates the standard register whose contents are to be shifted. The S field determines byte (S=0) or word (S=1) operations. The R field is also conditioned by the Program State (X) Register Bit $X^1$ as follows:

R FIELD

| $2^3$ $2^2$ $2^1$ $2^0$ | MATRIX REG X1 = 0 | MATRIX REG X1 = 1 |
|---|---|---|
| 0 0 0 0 | A0 | I0 |
| 0 0 0 1 | A1 | I1 |
| 0 0 1 0 | B0 | J0 |
| 0 0 1 1 | B1 | J1 |
| 0 1 0 0 | C0 | K0 |
| 0 1 0 1 | C1 | K1 |
| 0 1 1 0 | D0 | L0 |
| 0 1 1 1 | D1 | L1 |
| 1 0 0 0 | E0 | M0 |
| 1 0 0 1 | E1 | M1 |
| 1 0 1 0 | F0 | N0 |
| 1 0 1 1 | F1 | N1 |
| 1 1 0 0 | G0 | O0 |
| 1 1 0 1 | G1 | O1 |
| 1 1 1 0 | H0 | P0 |
| 1 1 1 1 | H1 | P1 |

| PROGRAM STATE REGISTER (X) | | |
|---|---|---|
| $2^0=0$ | SELECTS BI COUNTER (H) | AND MA REGISTER SET |
| $2^0=1$ | SELECTS BI COUNTER (P) | |
| $2^1=0$ | REGISTER SET 1 (A-H) | |
| $2^1=1$ | REGISTER SET 2 (I-P) | |
| $2^2=0$ | AUTOMATIC INTERRUPT PERMITTED | |
| $2^2=1$ | AUTOMATIC INTERRUPT INHIBITED | |

SFT Continued

The Shift Field defines the shift functions as follows:

| SHIFT FIELD | | | | | | Action | Result |
|---|---|---|---|---|---|---|---|
| $2^{10}$ | $2^9$ | $2^8$ | $2^7$ | $2^6$ | $2^5$ | | |
| 0 | 0 | 0 | X | X | X | Shift left, zero carry-in, shift out lost | 1 |
| 0 | 0 | 1 | X | X | X | Shift left, zero carry-in, shift out into $2^0$ of W | 2 |
| 0 | 1 | 0 | X | X | X | Shift left, $2^0$ of W carry-in, shift out is lost | 3 |
| 0 | 1 | 1 | X | X | X | Shift left, $2^0$ of W carry-in, shift out into $2^0$ of W | 4 |
| 1 | 0 | 0 | X | X | X | Shift right, zero carry-in, shift out is lost | 5 |
| 1 | 0 | 1 | X | X | X | Shift right, zero carry-in, shift out into $2^0$ of W | 6 |
| 1 | 1 | 0 | X | X | X | Shift right, $2^0$ of W carry-in, shift out is lost | 7 |
| 1 | 1 | 1 | X | X | X | Shift right, $2^0$ of W carry-in, shift out into $2^0$ of W | 8 |

"X" means don't care cases. However note that the numbers:

| Numbers | Result |
|---|---|
| 0-7 | 1 |
| 8-15 | 2 |
| 16-23 | 3 |
| 24-31 | 4 |
| 32-39 | 5 |
| 40-47 | 6 |
| 48-55 | 7 |
| 56-63 | 8 |

if put into the full shift field ($2^5$-$2^{10}$) yield the same 8 results.

SFT Continued

The W (Control Register) Register affects the operation as follows:

| W Register Bit | Action |
|---|---|
| $2^0$ Carry 1 | as described in the Shift Field |

and the W Register is modified by this instruction as follows:

| | |
|---|---|
| $2^0$ Carry 1 | 1. When Shift bit $2^8$ = 0, then carry 1 is not modified from initial setting.<br>2. When Shift bit $2^8$ = 1, then carry 1 is set to one when:<br>Shift Left, byte shift, carry from $2^7$<br>Shift Left, word shift, carry from $2^{15}$<br>Shift Right, byte or word, carry from $2^0$<br>3. When there is no carry in the above cases, carry 1 is set to zero. |
| $2^4$ Carry 2 | 1. When Shift bit $2^8$ = 0, then carry 2 is not modified from initial setting.<br>2. When Shift bit $2^8$ = 1, then carry 2 is set to one when:<br>Shift left, byte shift, carry from $2^6$<br>Shift left, word shift, carry from $2^{14}$<br>Shift right, byte or word, carry from $2^1$<br>3. When there is no carry in the above cases, carry 2 is set to zero. |

NOTE: When S=1, the $2^0$ bit of the R field is ignored and a full 16 bits are manipulated.

IOB I/O Test and Branch (I/O Test and Branch)

IOTBR

| F | T | B | ± |
|---|---|---|---|
| Function Code | | | |
| 01100 | 4 Bits | 6 Bits | 1 Bit |

$2^{15}$ $2^{11}$ $2^{10}$ $2^{7}$ $2^{6}$ $2^{1}$ $2^{0}$

Bit Position

Instruction Time - Branch 1.8 us
No Branch 1.8 us

IOB performs a specified test which is associated with I/O operations. If the test is true, a branch is taken; if not true, the next instruction in sequence is taken.

The test (T) field designates the following tests:

T FIELD

| $2^{10}$ $2^{9}$ $2^{8}$ $2^{7}$ | IOTBR |
|---|---|
| 0 0 0 0 | BIN0 = 1 |
| 0 0 0 1 | BIN1 = 1 |
| 0 0 1 0 | BIN2 = 1 |
| 0 0 1 1 | BIN3 = 1 |
| 0 1 0 0 | BIN4 = 1 |
| 0 1 0 1 | BIN5 = 1 |
| 0 1 1 0 | BIN6 = 1 |
| 0 1 1 1 | BIN7 = 1 |
| 1 0 0 0 | ANY BIN = 1 |
| 1 0 0 1 | MSB = 1 |
| 1 0 1 0 | |
| 1 0 1 1 | |
| 1 1 0 0 | |
| 1 1 0 1 | |
| 1 1 1 0 | |
| 1 1 1 1 | |

IOB Continued

*Note* that 1010 (10) through 1111 (IS) are not utilized and a no-branch (next instruction in sequence) will be executed.

| PROGRAM STATE REGISTER (X) | | |
|---|---|---|
| $2^0=0$ | SELECTS BI COUNTER (H) | AND MA REGISTER SET |
| $2^0=1$ | SELECTS BI COUNTER (P) | |
| $2^1=0$ | REGISTER SET 1 (A-H) | |
| $2^1=1$ | REGISTER SET 2 (I-P) | |
| $2^2=0$ | AUTOMATIC INTERRUPT PERMITTED | |
| $2^2=1$ | AUTOMATIC INTERRUPT INHIBITED | |

The Branch Field indicates an increment or decrement of 0 to 63 words from the address of the next instruction in sequence.

| Branch Field Bits | | | | | | | Action | No. of Words |
|---|---|---|---|---|---|---|---|---|
| if | $2^0$ | = | 0 | | | | increment | |
| | $2^0$ | = | 1 | | | | decrement | |
| and | | | | | | | | |
| $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | | | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | | | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | | | 2 |
| 0 | 0 | 0 | 0 | 1 | 1 | | | 3 |
| | | | | | | thru | | |
| 1 | 1 | 1 | 1 | 1 | 0 | | | 62 |
| 1 | 1 | 1 | 1 | 1 | 1 | | | 63 |

IOB Continued

Since the increment or decrement is made to BIC (Basic Instruction Counter) when positioned at the next instruction in sequence, a zero quantity will take the next instruction in sequence.

The X (Program State) Register Bit $2^0$ (Basic Instruction Indicator) determines which BIC will be affected.

When

| | | |
|---|---|---|
| $X2^0 = 0$ | BIC H0H1 | is affected |
| $X2^0 = 1$ | BIC P0P1 | is affected |

The W (Control) Register has no effect other than the specific tests described above and is not modified by this instruction.

NOTE: The increment/decrement is by words and not by bytes.

CSPR Constant to Special Register (Constant to Special Register) CSPR

| F | R | C |
|---|---|---|
| Function Code | | |
| 01111 | 3 Bits | 8 Bits |

$2^{15}$ $2^{11}$ $2^{10}$ $2^{8}$ $2^{7}$ $2^{0}$

Bit Position

Instruction Time - Constant to Bout 2.7 us
Other Registers 1.8 us

This instruction transfers the literal field C to one of the Special Registers. Depending on the nature of the Special Register, the instruction performs a variety of operations.

The R field specifies only the following Special Registers as follows:

| R Field | | | Special Register | Affect |
|---|---|---|---|---|
| $2^{10}$ | $2^{9}$ | $2^{8}$ | | |
| 0 | 1 | 1 | Bout 1 | I/O output, Strobe 1 |
| 0 | 1 | 0 | Bout 2 | I/O output, Strobe 2 |
| 1 | 0 | 0 | DAD | Loads I/O Device Address |
| 1 | 0 | 1 | Control (W) | Affects Register Settings |
| 1 | 1 | 0 | State (X) | Affects State of System |

Other combinations are not valid addresses for this instruction. If these are used, they will be specified at a later date.

The initial setting of the X and W registers do not affect this instruction. However, both can be changed by this instruction if they are designated in the R field or described above.

The C field can have the values:

C - a character constant
NN - a hexadecimal constant
0-255 - an absolute value or an absolute symbol representing 0-255.

DAB Decrement and Branch (Decrement and Branch) DECBR

| F | R | B | ± |
|---|---|---|---|
| Function Code | | | |
| 01110 | 4 Bits | 6 Bits | 1 Bit |

$2^{15}$ $2^{11}$ $2^{10}$ $2^{7}$ $2^{6}$ $2^{1}$ $2^{0}$

Bit Position

Instruction Time - Branch 2.7 us
No Branch 1.8 us

This instruction decrements by one, the contents of one of the Byte Standard Registers and branches if the result is non-zero. If result is zero, the next instruction in sequence is taken.

The R field designates a Byte Size Standard Register and is conditioned by the 2 bit of the X (Program State Register) Register also. Both are indicated below:

R FIELD

| $2^{10}$ $2^{9}$ $2^{8}$ $2^{7}$ | MATRIX REG XI = 0 | MATRIX REG XI = 1 |
|---|---|---|
| 0 0 0 0 | A0 | T0 |
| 0 0 0 1 | A1 | T1 |
| 0 0 1 0 | B0 | J0 |
| 0 0 1 1 | B1 | J1 |
| 0 1 0 0 | C0 | K0 |
| 0 1 0 1 | C1 | K1 |
| 0 1 1 0 | D0 | L0 |
| 0 1 1 1 | D1 | L1 |
| 1 0 0 0 | E0 | M0 |
| 1 0 0 1 | E1 | M1 |
| 1 0 1 0 | F0 | N0 |
| 1 0 1 1 | F1 | N1 |
| 1 1 0 0 | G0 | $\bar{0}0$ |
| 1 1 0 1 | G1 | $\bar{0}1$ |
| 1 1 1 0 | H0 | P0 |
| 1 1 1 1 | H1 | P1 |

| PROGRAM STATE REGISTER (X) | | |
|---|---|---|
| $2^0 = 0$ | SELECTS BI COUNTER (H) | AND MA REGISTER SET |
| $2^0 = 1$ | SELECTS BI COUNTER (F) | |
| $2^1 = 0$ | REGISTER SET 1 (A-H) | |
| $2^1 = 1$ | REGISTER SET 2 (I-P) | |
| $2^2 = 0$ | AUTOMATIC INTERRUPT PERMITTED | |
| $2^2 = 1$ | AUTOMATIC INTERRUPT INHIBITED | |

DAB Continued

The Branch Field (B) indicates an increment or decrement of 0 to 63 words from the address of the next instruction in sequence.

| Branch Field Bits | | | | | | | | Action |
|---|---|---|---|---|---|---|---|---|
| if $2^0 = 0$ | | | | | | | | increment |
| $2^0 = 1$ | | | | | | | | decrement |
| | | | and | | | | | |
| | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | | No. of Words |
| | 0 | 0 | 0 | 0 | 0 | 0 | | 0 |
| | 0 | 0 | 0 | 0 | 0 | 1 | | 1 |
| | 0 | 0 | 0 | 0 | 1 | 0 | | 2 |
| | 0 | 0 | 0 | 0 | 1 | 1 | | 3 |
| | | | | | | | thru | |
| | 1 | 1 | 1 | 1 | 1 | 0 | | 62 |
| | 1 | 1 | 1 | 1 | 1 | 1 | | 63 |

Since the increment or decrement is made to BIC (Basic Instruction Counter) when positioned at the next instruction in sequence, a zero quantity will take the next instruction in sequence.

The X (Program State) Register Bit $2^0$ (Basic Instruction Indicator) determines which BIC will be affected.

When

X2 = 0 BIC H0H1 is affected
X2 = 1 BIC P0P1 is affected

The W (Control) Register is not affected nor does it affect this instruction.

NOTE: The amount of increment/decrement is by words and not bytes to the BIC. However, the Byte Standard Register indicated in the R field is decrement by binary "1".

IDR Increment/Decrement (Increment/Decrement) INCR

| F | R | | I | ± |
|---|---|---|---|---|
| Function Code | | | | |
| 00110 | 4 Bits | X | 6 Bits | 1 Bit |

$2^{15}$ $2^{11}$ $2^{10}$ $2^{8}$ $2^{7}$ $2^{6}$ $2^{1}$ $2^{0}$

Bit Positions

Instruction Time - 1.8 us

IDR permits a limited unconditional increment or decrement to one of the word size Standard Registers. When the BIC (Basic Instruction Counter) is selected, this instruction serves as an Unconditional Transfer.

The R Field designates a word size Standard Register and is also conditioned by the $2^1$ Bit of the X (Program State) Register. These are indicated below.

| R Field | | | | $X2^1=0$ | $X2^1=1$ |
|---|---|---|---|---|---|
| $2^{10}$ | $2^9$ | $2^8$ | $2^7$ | Word Register | |
| 0 | 0 | 0 | X | A0A1 | I0I1 |
| 0 | 0 | 1 | X | B0B1 | J0J1 |
| 0 | 1 | 0 | X | C0C1 | K0K1 |
| 0 | 1 | 1 | X | D0D1 | L0L1 |
| 1 | 0 | 0 | X | E0E1 | M0M1 |
| 1 | 0 | 1 | X | F0F1 | N0N1 |
| 1 | 1 | 0 | X | G0G1 | O0O1 |
| 1 | 1 | 1 | X | H0H1 | P0P1 |

"X" represents don't care cases.

IDR Continued

The Increment/Decrement (I) Field indicates an increment or decrement of 0 to 63 words from the contents of the register specified by the R field (amount of 0 to 126 bytes in steps of two). If the contents of the register represents a memory address, then the increment/decrement field can be thought of having a range of 0 to 63 addresses or instructions. The I field is interpreted as follows:

| I Field Bit | Action |
|---|---|
| if $2^0 = 0$ | increment |
| $2^0 = 1$ | decrement |

| and | | | | | | | No. of | |
|---|---|---|---|---|---|---|---|---|
| $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | | Bytes | Words |
| 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | | 2 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | | 4 | 2 |
| 0 | 0 | 0 | 0 | 1 | 1 | | 6 | 3 |
| | | | | | | thru | | |
| 1 | 1 | 1 | 1 | 1 | 0 | | 124 | 62 |
| 1 | 1 | 1 | 1 | 1 | 1 | | 126 | 63 |

(The I field represents a positive binary quantity).

If R refers to a BIC (Basic Instruction Counters = H0H1 or P0P1) then:

1. The Basic Instruction Indicator ($2^0$ position of the X Register) and Register Set Indicator ($2^1$ Position of the X Register) should be set as "00" or "11".

2. The I field is applied to the BIC counter as indicated by the X Register. Thus, I indicates the number of words (0 to 63) to branch. The I field is applied the BIC which is positioned at the next instruction in sequence. Therefore, a zero quantity in the I field will take the next instruction in sequence.

The W Register (Control) does not affect nor is it affected by this instruction.

CSTR Constant to Standard Register CMR
(Constant to Matrix Register)

| F | R | C |
|---|---|---|
| Function Code | | |
| 01101 | 3 Bits | 8 Bits |

$2^{15}$ $2^{11}$ $2^{10}$ $2^{8}$ $2^{7}$ $2^{0}$

Bit Positions

Instruction Time 1.8 us

CSTR transfers a constant as given in C to a byte sized standard register.

The R field designates a limited set of byte size standard registers and is conditioned by the setting of the Register Set Indicator (2 of the X Register) as shown below:

| R Field | | | $X2^1 = 0$ | $X2^1 = 1$ |
|---|---|---|---|---|
| $2^{10}$ | $2^9$ | $2^8$ | Register | Register |
| 0 | 0 | 0 | A0 | I0 |
| 0 | 0 | 1 | A1 | I1 |
| 0 | 1 | 0 | B0 | J0 |
| 0 | 1 | 1 | B1 | J1 |
| 1 | 0 | 0 | C0 | K0 |
| 1 | 0 | 1 | C1 | K1 |
| 1 | 1 | 0 | D0 | L0 |
| 1 | 1 | 1 | D1 | L1 |

Note Registers E-H and M-P cannot be addressed by this instruction.

The C Field provides a literal quantity that is transferred to the designated register. The numerical value can be 0-255 or an absolute symbol with a value of 0-255.

The W Register is not affected nor does it affect this instruction.

BIT Bit Operation
(Bit Operation)

BITOP

| F<br>Function Code | Z | SF | | | R |
|---|---|---|---|---|---|
| 00101 | 3 Bits | X | 4 Bits | X | |

$2^{15}$ $2^{11}$ $2^{10}$ $2^{8}$ $2^{7}$ $2^{6}$ $2^{5}$ $2^{4}$ $2^{3}$ $2^{0}$

Bit Position

Instruction Time 1.8 us

BIT provides the ability to set, reset, or test an individual bit within a byte size standard register.

The R field designates a byte size Standard Register and is conditioned by the $2^{1}$ bit of the X (Program State) Register as follows:

R FIELD

| 3 2 1 0 | MATRIX REG XI = 0 | XI = 1 |
|---|---|---|
| 0 0 0 0 | A0 | I0 |
| 0 0 0 1 | A1 | I1 |
| 0 0 1 0 | B0 | J0 |
| 0 0 1 1 | B1 | J1 |
| 0 1 0 0 | C0 | K0 |
| 0 1 0 1 | C1 | K1 |
| 0 1 1 0 | D0 | L0 |
| 0 1 1 1 | D1 | L1 |
| 1 0 0 0 | E0 | M0 |
| 1 0 0 1 | E1 | M1 |
| 1 0 1 0 | F0 | N0 |
| 1 0 1 1 | F1 | N1 |
| 1 1 0 0 | G0 | $\bar{O}0$ |
| 1 1 0 1 | G1 | $\bar{O}1$ |
| 1 1 1 0 | H0 | P0 |
| 1 1 1 1 | H1 | P1 |

| CONTROL REGISTER (W) | |
|---|---|
| W0 | CARRY 1-INDICATES CARRY FROM ($2^{7}$ OR $2^{15}$) OF ARITHMETIC OPERATION |
| W1 | NED-INDICATES ARITHMETIC OPERATION RESULT WAS NOT ZERO |
| W2 | INDICATOR FOR PROGRAM USE |
| W3 | INDICATOR FOR PROGRAM USE |
| W4 | CARRY 2-INDICATES CARRY FROM ($2^{6}$ OR $2^{14}$) OF ARITHMETIC OPERATION |
| W5 | INDICATOR FOR PROGRAM USE |
| W6 | BIT OP TEST-INDICATES RESULT OF BITOP BIT OR SIGN OF ARITHMETIC OPERATION |
| W7 | PROGRAM INDICATOR-SETS PI LIGHT ON CONSOLE |

| PROGRAM STATE REGISTER (X) | | |
|---|---|---|
| $2^{0}=0$ | SELECTS BI COUNTER (H) | AND MA REGISTER SET |
| $2^{0}=1$ | SELECTS BI COUNTER (F) | |
| $2^{1}=0$ | REGISTER SET 1 (A-H) | |
| $2^{1}=1$ | REGISTER SET 2 (I-P) | |
| $2^{2}=0$ | AUTOMATIC INTERRUPT PERMITTED | |
| $2^{2}=1$ | AUTOMATIC INTERRUPT INHIBITED | |

BIT Continued

The Z Field specifies the bit in the Standard Register as given by the R field to be operated on. It is specified as follows:

| Z Field | | | Bit Position of Byte Register |
|---|---|---|---|
| $2^{10}$ | $2^9$ | $2^8$ | |
| 0 | 0 | 0 | $2^0$ |
| 0 | 0 | 1 | $2^1$ |
| 0 | 1 | 0 | $2^2$ |
| 0 | 1 | 1 | $2^3$ |
| 1 | 0 | 0 | $2^4$ |
| 1 | 0 | 1 | $2^5$ |
| 1 | 1 | 0 | $2^6$ |
| 1 | 1 | 1 | $2^7$ |

The SF Field designates the specific operation on the bit as follows:

| SF | | | | Operation |
|---|---|---|---|---|
| $2^7$ | $2^6$ | $2^5$ | $2^4$ | |
| X | 0 | 0 | X | No Operation |
| X | 0 | 1 | X | Test Bit |
| X | 1 | 0 | X | Reset Bit (to 0) |
| X | 1 | 1 | X | Set Bit (to 1) |

"X" specifies don't care fields.

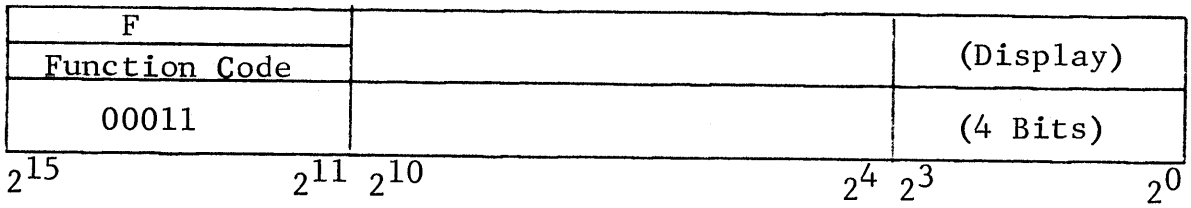
The Test Bit Operation is as follows:

1. If tested bit = zero, set $2^6$ (test bit indicator) Bit of W Register to zero.

2. If tested bit = one, set $2^6$ (test bit indicator) Bit of W Register to one.

The initial setting of the W Register (Control) does not affect this instruction. However, BIT may modify the Test Bit ($2^6$ of W Register) as described above.

Halt Halt HLT
(Halt - Normal Operation)




Bit Positions

Instruction Time 1.8 us

This instruction halts the system. It is the programmer's responsibility to check for I/O completions before issuing this instruction. The low order 4 bits ($2^3$-$2^0$) are displayed on the operators panel for communication purposes. If the start button is depressed after a halt instruction, the machine will start with the next instruction in sequence.

The X and W Registers do not affect nor are they modified by this instruction.

NOTE: The S bits of the function code provide 32 combinations of which 29 are utilized including Halt. The other three are also Halts except they will light the operator's Panel Error Indicator. This can be reset by any of the following switches: RDM, WRM, Step Halt, Start, and General Reset. The illegal Halt Function Codes are:

00000
00001
00010