1600 System

Systems Information Manual

RCA Computers

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BD-000-1-00

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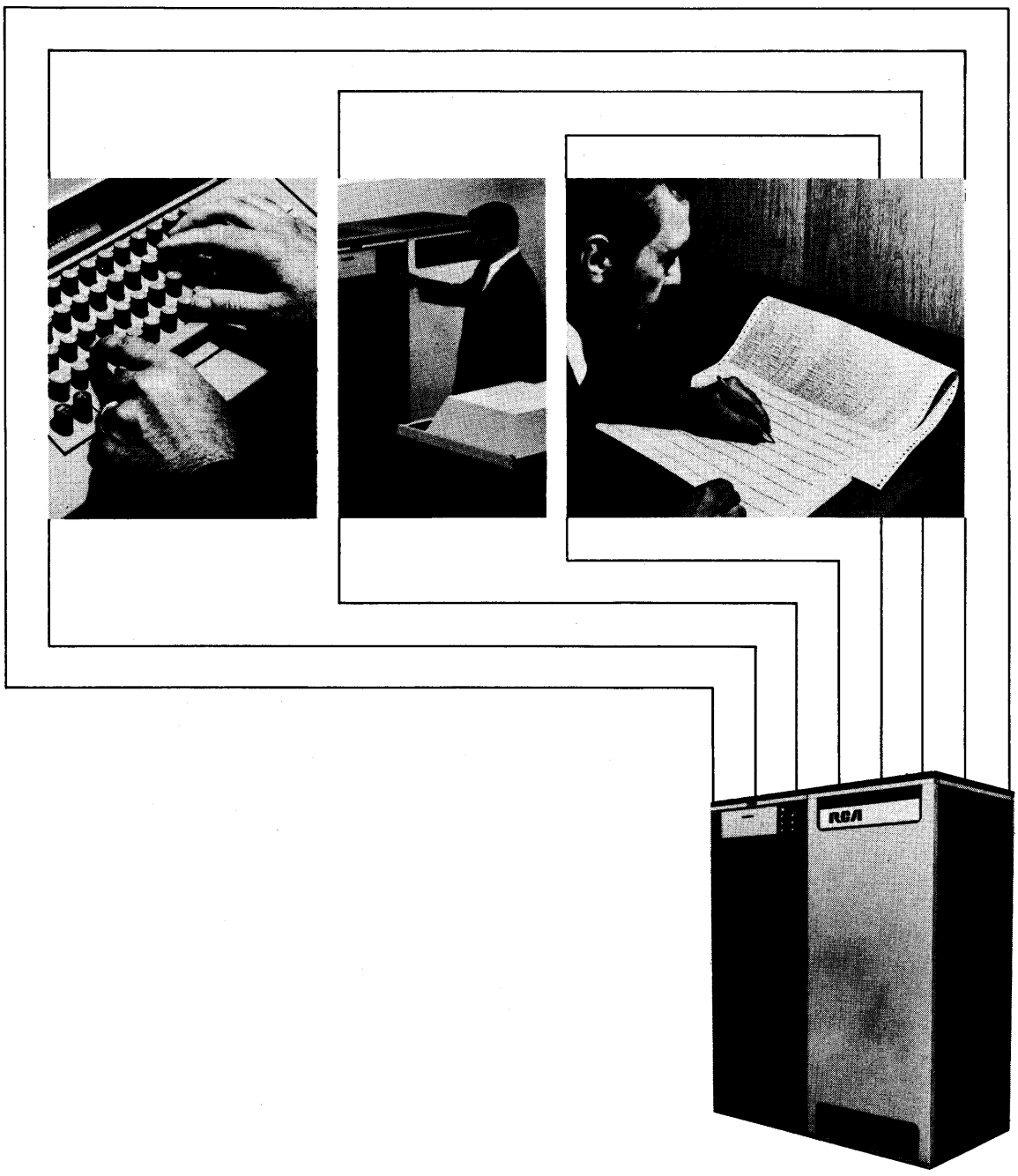
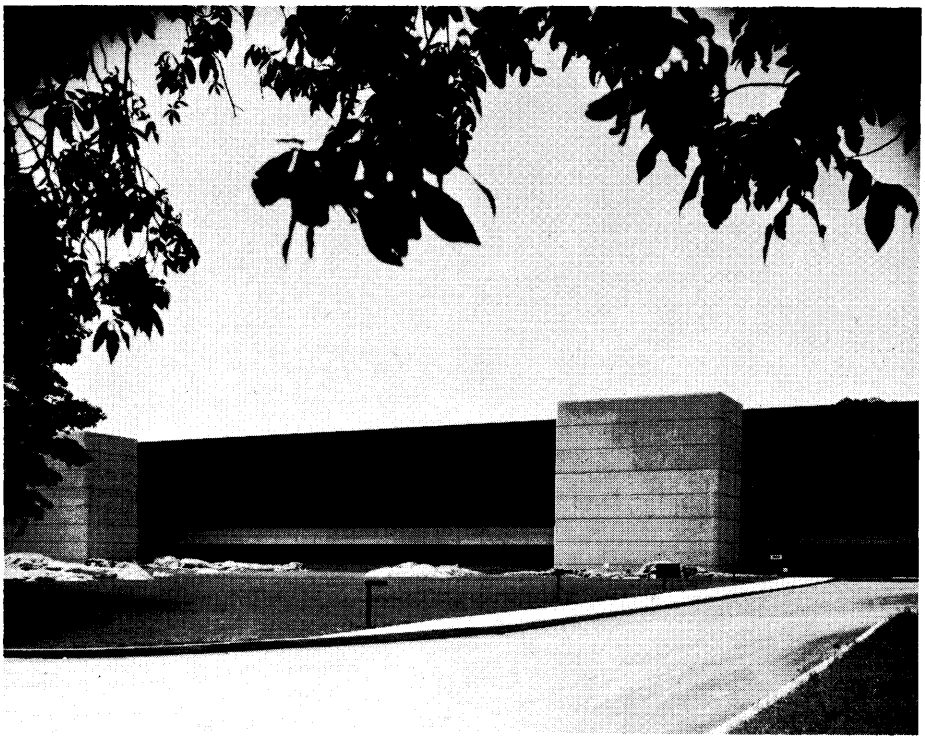

RCA

1. INTRODUCTION

Man's future progress depends on the solution of many problems in today's complex society. The computer plays a key role in meeting the challenge of this age. In practically every industry and profession the computer has been used as a tool to work problems more quickly, with less drudgery, and with greater accuracy than was ever dreamed possible. Computers do all types of tasks; they process business data, control communications, do simulation, control manufacturing processes, and store and retrieve information. As man continues to discover new applications for the use of this tool, the need for more versatile and flexible computers has also grown.

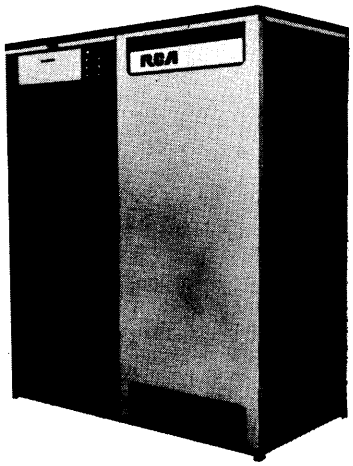
In answer to this need, RCA engineers have spent two years designing and developing a truly unique equipment - the RCA 1600 System. This system is a small but flexible computer that incorporates a modularity feature for a variety of special applications. The RCA 1600 System was developed at RCA's West Palm Beach facility in Florida. The processor was subjected to extreme environmental conditions, and in every test it performed without a malfunction. Users of this class of equipment require the operation of remotely located systems in a wide range of severe environmental conditions. The RCA 1600 System has been thoroughly tested to give the reliability performance needed for these applications. The peripheral devices used with the RCA 1600 were developed and are manufactured at RCA's facility in Marlboro, Massachusetts.

West Palm Beach Plant (Florida), with 370,000 square feet of floor space, where 1600 System was developed and is now in production.



Marlboro Plant (Massachusetts), with 250,000 square feet of floor space, where 1600 System peripheral devices are now in production.

SUMMARY OF BASIC SPECIFICATIONS
1600 SYSTEM



Memory Capacity *8,192 to 65,536 bytes. Field expandable from 8,192 to 16,384 and from 32,768 to 65,535 bytes.*

Memory cycle time *1.6 microseconds.*

Word size *18 bits including memory protection bit and parity bit.*

Registers *16 bits each.*

Instruction *29.*

Instruction speeds *1.7 to 4.1 microseconds.*

Controller space per main frame *9 rows.*

Total expansion racks *2 per 1600 System.*

Maximum controller space per system *22 rows.*

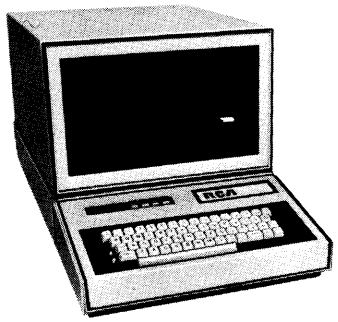
Direct hardware interface with RCA 2, 3, 6, and 7 *Yes.*

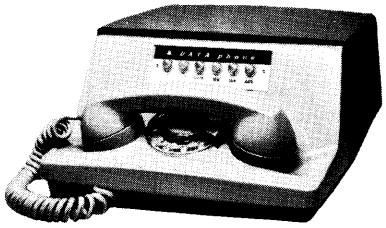
High-speed cycle stealing *1.6 microseconds per character.*

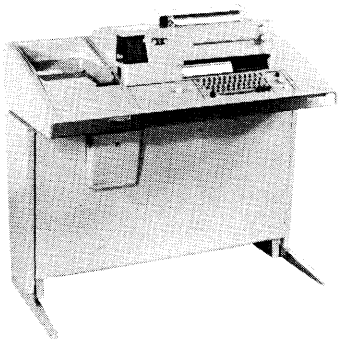
Programming Support *I/O Interfacing, Utilities*

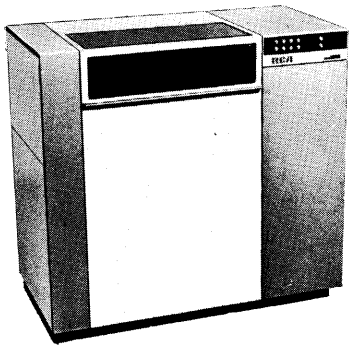
COMMUNICATIONS

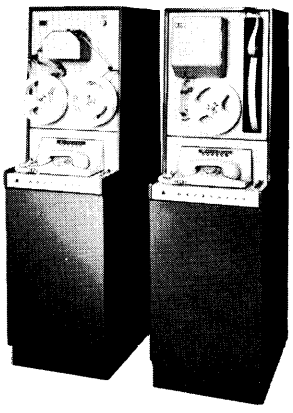
Communication controls (DSC, DSLC and TLC) provide telephone and telegraph transmission for use with teletypewriter, video data terminals (reference should be made to Appendix B for sample video configurations), and remote printer/card readers. For military applications, a direct tie-in with the Automatic Digital Network (AUTODIN) can be made.











REMOTE COMMUNICATIONS

2. SYSTEM DESCRIPTION

GENERAL

The RCA 1600 System is a digital, stored program, data processing system. Its memory sizes range from 8,192 to 65,536 bytes, and the cycle time for a word operation is 1.6 microseconds. Instructions are flexible, and 29 are available for programming use. Execution times range from 1.7 to 4.1 microseconds.

Other important features include the packaging of the 1600 Processor, which is shown in the frontispiece. A basic rack houses the 1600 power supply, logic, core memory, channel for servicing I/O devices, Programmer/Maintenance Panel, the standard 1600 Processor Operating Panel, and as many as nine rows of controls.

In addition to conventional I/O capability for printers, paper tape, magnetic tape, and card equipment, the 1600 System has a complete facility for disc storage and teletypewriter operation, video display, and other communication capability. Effective throughput performance is achieved through high-speed and low-speed channels, which permit connection of multiple devices to the systems.

The 1600 System has the internal ability to combine high processing speeds with a full line of standard and special purpose input/output devices. This fact permits the design of a system with a good balance between performance and price.

The 1600 can be used as an RCA Series Controller for special purpose peripheral equipment or as a control processor in a dedicated, special purpose application system. Under these two conditions, the 1600 either operates with an RCA 2, 3, 6, or 7 system or as a stand-alone, dedicated, special purpose processor operating on a limited number of programs.

Utilities, assemblers, simulators, diagnostics, and an input/output processing system are provided. A 1600 program can be assembled on an RCA Series Processor or a 1600 Processor.

Additional detailed information may be found in the 1600 System Equipment Reference Manual and 1600 System Processor Operating Manual.

CONFIGURING THE SYSTEM

Orderable equipment elements of the 1600 System are termed "components." Each 1600 System component is identified by a six-digit component number; the first two digits are 1 6. Where RCA Series equipment is utilized, the nomenclature of RCA Series models and features is maintained.

A 1600 System consists of a processor, controls (control electronic units), and associated input/output and/or communication devices. The 1600 Processor has a single input/output channel (I/O bus) for data transmission between processor and the input/output components. Refer to figure 1.

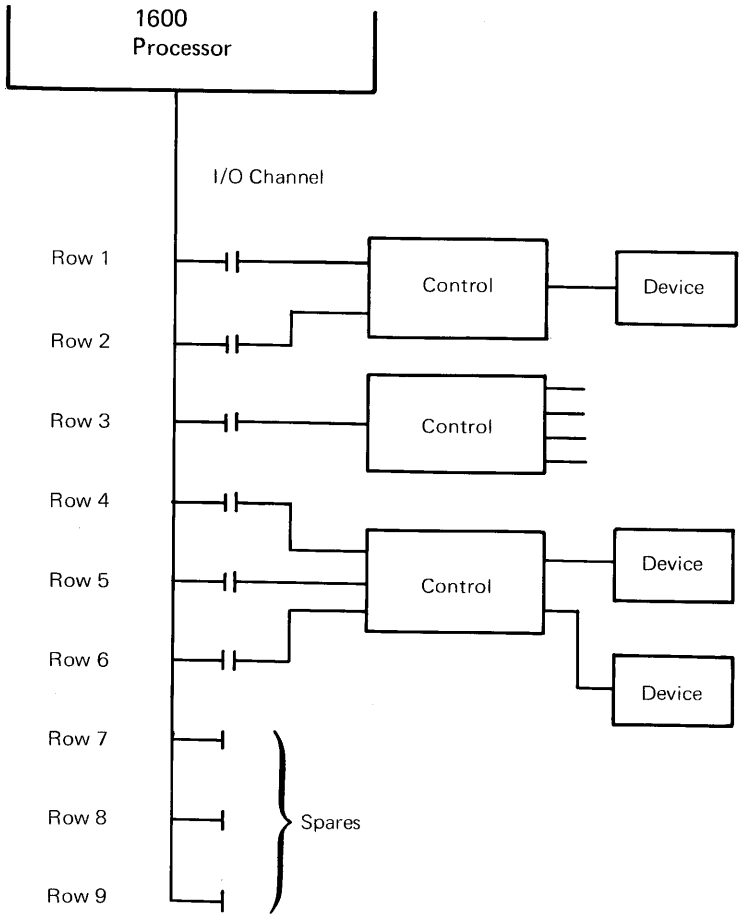


FIGURE 1. TYPICAL ASSIGNMENTS OF ROWS

Each input/output device is connected to a control that fits physically into the 1600 Processor rack. These controls vary in size from one to three rows of plug-in electronics, depending on their function. When configuring a system, care must be exercised that the number of rows does not exceed the capacity of nine provided by the processor. (Two optional expansion racks are available; the first provides seven additional rows for a total capacity of 16, and the second provides six additional rows for a total capacity of 22.)

Row allocations in no way affect priority or performance. However, magnetic tape controls and disc controls (non-RCA drives) must be installed in the Processor Main Frame because they depend on the processor's power source.

The 1600 Processor contains a high-speed and a low-speed channel, analogous to an RCA Series Processor selector channel and multiplexor channel, as shown in figure 2. However, the channel consists, physically, of one cable, and data flows in and out on program-designated lines to devices that have high-speed and low-speed data rates.

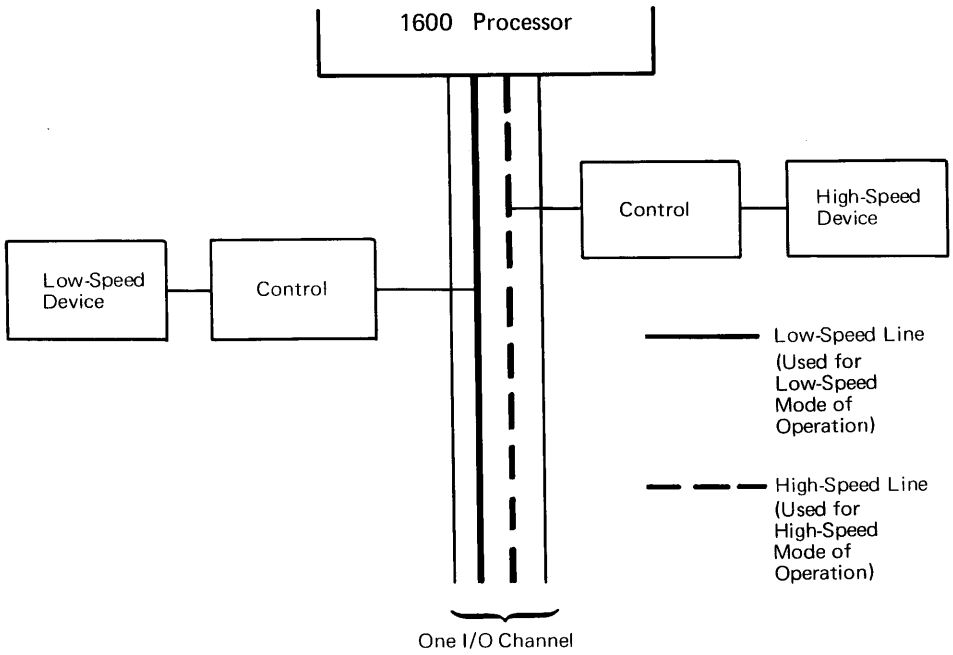


FIGURE 2. 1600 I/O TRANSFER FLOW

INPUT/OUTPUT CAPABILITY

RCA Series

Input/output devices from the RCA 2, 3, 6, and 7 systems can be connected to the 1600 Systems with a Standard Interface Control. These devices are mentioned later in this manual.

Console Typewriter

A Console Typewriter (ASR, automatic send/receive; or KSR, keyboard send/receive) equipped with a paper tape reader feature provides a complete subsystem having paper tape facilities operating at speeds of 10 characters per second.

Magnetic Tape Devices

The 8432-1 Magnetic Tape Units provide the capability of processing industry-compatible 9-level tape or 7-level tape, with feature 5411 added, at speeds up to 30 kb at various packing densities; for example, 200, 556, or 800 bpi. Two tape units (four tape decks) are permitted for each control.

Automatic Message Accounting (AMA)

A special purpose control is available for AMA Conversion Systems used for off-line conversion of AMA paper tape and magnetic tape. This system is employed by the operating telephone companies of the Bell System.

Random Access

The 8564 Disc Storage Unit, with its 7.25-million byte capacity and an average access time of 75 milliseconds, can be installed as part of the 1600 System. Four disc units are permitted for each control for a total random-access capacity of 29.0 million bytes for each control.

Timer

A time-of-day control can generate interrupts at specified intervals and is capable of being controlled externally by a master clock system.

Data Exchange

The data exchange channel provides for memory-to-memory transmission of data between a 1600 System and an RCA Series System, or another 1600 System equipped with a Standard Interface Control.

3. EQUIPMENT DESCRIPTION

PROCESSOR

The 1600 Processor, as shown in figure 3, is available in four memory sizes as follows:

Component Number	Memory Size (bytes)
161108	8,192
161116	16,384
161132	32,768
161164	65,536

Memory increments are modular and field expandable to permit system growth and increased processing power. Memory speed is 1.6 microseconds for an 18-bit access.

Each word of the 1600 Processor is made up of 18 bits. Sixteen of these bits represent data, one bit represents memory protection, and one bit provides odd parity.

The control of the 1600 Processor is implemented by 29 basic instructions from which more complex instructions or subroutines can be formed. The basic instructions are designed to manipulate 8-bit bytes or 16-bit words.

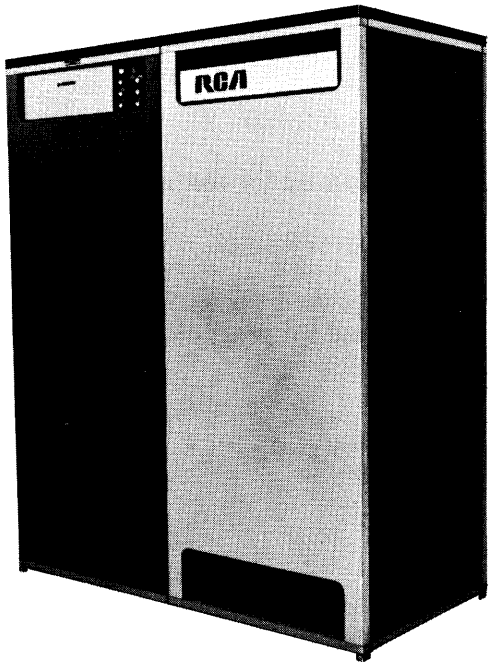


FIGURE 3. 1600 PROCESSOR

Arithmetic Operations

The basic arithmetic instructions are specified to permit the user to operate in two number systems, binary or signed, and in 8-bit or 16-bit operands. Other number systems or operand sizes are handled by subroutines.

The signed system has positive and negative values, while the binary system is unsigned and has only positive values. The same instructions can be used for either system, provided that the rules for carry and overflow are utilized.

Memory Protection

Each word contains a memory protection bit. If the memory protection bit is set to 1 and the memory protect mode is set on the Programmers/Maintenance Panel, the memory word is protected. If an attempt is made by the program, or an input/output operation, to write to a protected word, it is a memory-protect violation. The processor will halt at the end of the memory cycle in which a memory violation is detected.

Standard Registers

Sixteen 16-bit registers, formed physically from 16 integrated circuit chips, are used as standard registers. These registers may be addressed either as 16-bit or 8-bit registers. They serve as basic instruction counters, address registers, and high-speed I/O registers, as well as miscellaneous functional registers as required by the program.

Special Registers

The special registers, as contrasted with the standard registers, act functionally as seven registers.

Program State Register (X)

This register is used for controlling the state of the system.

Control Register (W)

This register is used for testing conditions resulting from actions of the basic instructions and for program linkage.

DAD

This is the I/O Device Address register associated with the device address lines.

BIN S0

This is the Bus Input register that consists of the eight BIN lines of the I/O bus. A STROBE signal is not associated with this register.

BIN S1

This is the Bus Input register that consists of the STROBE 1 line and the eight BIN lines of the I/O bus.

BOUT S1

This is the Bus Output Register that is connected to the BOUT lines of the I/O bus. The STROBE 1 line is associated with this register.

BOUT S2

This is the Bus Output register that is connected to the BOUT lines of the I/O bus. The STROBE 2 line is associated with this register.

Interrupts

Interrupts provide the capability for the control electronics to signal the processor. Typical causes for an interrupt are a low-speed data service request or a device termination.

There are two classes of interrupts. Class 1 interrupts are honored, when interrupt is not inhibited, at the end of each basic instruction. Class 2 interrupts are honored at the user's discretion, which would normally be at the end of a subroutine. The class of interrupt for each control is specified at installation time.

Input/Output Channel

The control of data transmission between the processor and an associated peripheral device is accomplished through an input/output channel. A channel may be considered as an independent unit which controls data flow between an input/output device and the processor. As a result, the processor can function simultaneously with the input/output operation. Input/output on the 1600 Processor has two forms: a single high-speed mode handles data transfers independently of the program; a low-speed mode handles multiple devices and incorporates all servicing under control of basic instruction routines. Both modes are initiated by programming.

High-Speed Mode

A single high-speed I/O channel has been implemented on the 1600 Processor. It handles the normal I/O service request in a manner separate from the multiplex I/O procedures. When a control electronics operating in the high-speed mode signals a service request, a memory cycle is "stolen" at the end of the current basic instruction, and the service is handled by hardware control.

The purpose of this mode is to accommodate devices with high-speed transfer rates. Two standard registers are assigned for the high-speed mode, and the initial loading of these registers, as well as initiation procedures to the control electronics, are under program control. Upon termination, the control electronics signals the processor through the normal interrupt procedures.

During a high-speed mode service request, one byte is transferred. The time required is 1.6 microseconds. Only one device may operate in the high-speed mode at a time, although more than one control electronics may be connected to the channel.

Low-Speed Mode

The low-speed mode is analogous to a multiplexor channel. Servicing of I/O operations is under the control of the program. A program interrupt to a second program state (with an independent set of programming registers) is provided.

Devices such as the typewriter console, paper tape reader/punch, and communications are normally operated in this mode.

Power Failure

The removal of power, either intentional or through a line failure, will not destroy the contents of the main memory. The power supply for the 1600 Processor can override power fluctuations of less than 8 milliseconds in duration.

External Error Alarm

The 1600 Processor provides an external failure alarm signal when any of the following take place:

1. Memory Parity Error.

2. Dc Power Failure.

3. Memory Protect Violation.

4. Nonvalid Op Code Halt.

5. Operator Initiated Stop from Operators Panel or from Programmers/Maintenance Panel.

6. The 2^5 bit of the Control Register (W) is set by the program.

Instructions

A total of 29 instructions are available. The formats fall into the following three groups:

Group I: Memory to Register or Register to Memory (10 instructions).

Group II: Register to Register (10 instructions).

Group III: General (9 instructions).

All instructions are 16 bits in length. It is a system restriction that instructions must be stored in memory within word boundaries. Therefore, instructions can be accessed in one memory cycle (1.6 microseconds).

Group I

The format of Group I is as follows:

Memory to Register (or Register to Memory) **10 Instructions**

Function Code (F)					MA			I			S	R			
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

The instructions of Group I are:

Instruction	Mnemonic
Write to Memory	WTM
Read Memory and Transfer	RMT
Read Memory and Add	RMA
Read Memory and Subtract	RMS
Read Memory and Add with Carry	RMAC
Read Memory and Subtract with Carry	RMSC
Read Memory and Compare	RMC
I/O Transfer to Memory	IOTM
I/O Transfer from Memory	IOFM
Memory Protect Set and Reset	MPSR

Group II

The format of Group II is as follows:

Register to Register **10 Instructions**

Function Code (F)					R1				SF		S	S2			
2^{15}	2^{14}	2^{13}	2^{12}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}

The instructions of Group II are:

Instruction	Mnemonic
Add	ABR
Subtract	SBR
Add with Carry	ABRC
Subtract with Carry	SBRC
Compare	CMPR
AND	ANDR
OR	ORR
Exclusive OR	XORR
Transfer	TRR
Standard Register Set Transfer	SRST

Group III

The format of Group III is as follows:

Function Code (F)					Depends Upon Specific Instruction										
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

The formats of the nine general instructions vary according to their specific function. The nine instructions are:

Instruction	Mnemonic
Halt	HALT
Shift	SFT
Test and Branch	TAB
I/O Test and Branch	IOB
Decrement and Branch	DAB
Increment and Branch	IDR
Bit Operation	BIT
Constant to Standard Register	CSTR
Constant to Special Register	CSPR

Instruction Timing

All timing that applies to the instructions described are shown in table 1.

TABLE 1. INSTRUCTION TIMING

Instruction	Mnemonic	Timing (Microseconds)
Write to Memory	WTM	3.3 per byte
Read Memory and Transfer	RMT	3.3 per byte
Read Memory and Add	RMA	3.3 per byte 4.1 per word
Read Memory and Subtract	RMS	3.3 per byte 4.1 per byte
Read Memory and Add with Carry	RMAC	3.3 per byte 4.1 per word
Read Memory and Subtract with Carry	RMSC	3.3 per byte 4.1 per word
Read Memory and Compare	RMC	3.3 per byte 4.1 per word
I/O Transfer to Memory	IOTM	3.3 per byte
I/O Transfer from Memory	IOFM	3.3 per byte

(Continued)

Instruction	Mnemonic	Timing (Microseconds)
Memory Protect Set and Reset	MPSR	3.3 per byte
Add	ABR	1.7 per byte 2.5 per word
Subtract	SBR	1.7 per byte 2.5 per word
Add with Carry	ABRC	1.7 per byte 2.5 per word
Subtract with Carry	SBRC	1.7 per byte 2.5 per word
Compare	CMPR	1.7 per byte 2.5 per word
AND	ANDR	1.7 per byte 2.5 per word
OR	ORR	1.7 per byte 2.5 per word
Exclusive OR	XORR	1.7 per byte 2.5 per word
Transfer	TRR	1.7 per byte
Standard Register Set Transfer	SRST	1.7 per byte
Shift	SFT	1.7 per byte
Test and Branch	TAB	1.7 (branch) 1.7 (no branch)
I/O Test and Branch	IOB	1.7 (branch) 1.7 (no branch)
Decrement and Branch	DAB	2.5 (branch) 1.7 (no branch)
Increment/Decrement	IDR	1.7 per byte
Bit Operation	BIT	1.7 per byte
Constant to Standard Register	CSTR	1.7 per byte
Constant to Special Register	CSPR	2.5 (Constant to BOUT) 1.7 (other registers)
Halt	HALT	1.7 per byte

Note: Basic instruction time is increased by 0.8 microsecond whenever an address requires a carry to the most significant byte. This happens at each 256-byte boundary. Four areas where this can occur are:

1. Update the basic instruction counter during instruction fetch.

2. Increment/Decrement instruction to an MA register.

3. Branch instruction incrementing or decrementing the basic instruction counter.

4. Execution of the Increment/Decrement instruction.

Addressing

A patch board is provided with each control to assign the device address (DAD) at installation time. A suggested list of standards may be found by referring to Appendix C.

CONTROLS AND INDICATORS

Operator Panel

The Operator Panel, shown in figure 4, is clearly marked and is easy to operate.

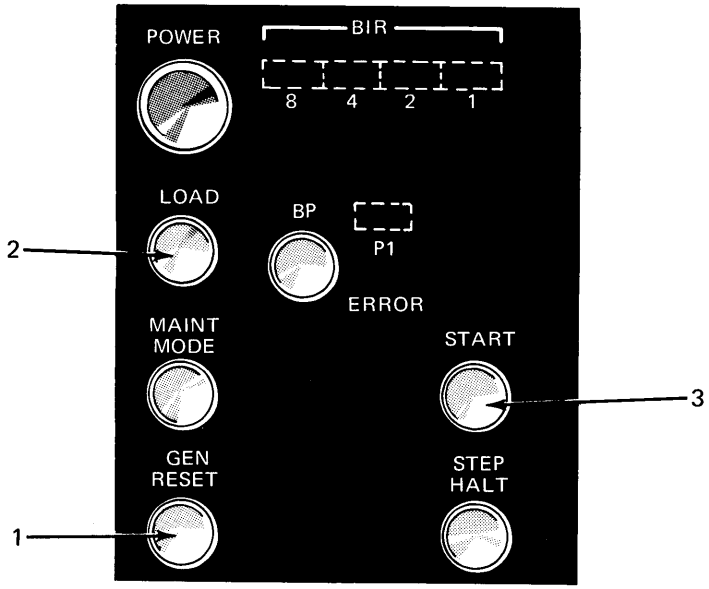


FIGURE 4. OPERATOR PANEL, CONTROLS AND INDICATORS

The normal operator sequence to load a program is to press the GEN RESET (1), LOAD (2), and START (3) pushbuttons.

Programmer/Maintenance Panel

Figure 5 shows the Programmer/Maintenance Panel, which is physically within the 1600 Processor Mainframe. It contains the necessary switches and indicators required for manual control of the Processor. This gives the computer service representative (CSR) and/or the programmer the ability to display an internal condition in order to troubleshoot the Processor or to test a new program.

The 1600 System Configurator shown in figure 6 depicts the equipment of the entire 1600 product line. Information pertaining to the individual controls and devices may be found in the following pages of this section.

EXPANSION RACK (COMPONENT 169902)

The 1600 Processor Expansion Rack, shown in figure 7, provides a means for adding up to seven rows of Control space to the 1600 Processor (which contains nine rows). In addition, this rack contains its own power supply capable of supporting the added rows of controls (except the 8432-1 Magnetic Tape Units). The Magnetic Tape Control and Disc Control (non-RCA drives) cannot be housed in an Expansion Rack due to power considerations. The second Expansion Rack is identical to the first except that it adds up to six rows of Control space to the first Expansion Rack for a total of 13 rows.

STANDARD INTERFACE

The Standard Interface Control provides a means to connect most RCA Series I/O device controllers to the 1600 Processor. The exceptions are:

1. 8551 Random Access Controller.

2. 8590 Direct Access Storage System.

3. 8668 Communication Controller-Multichannel (CCM).

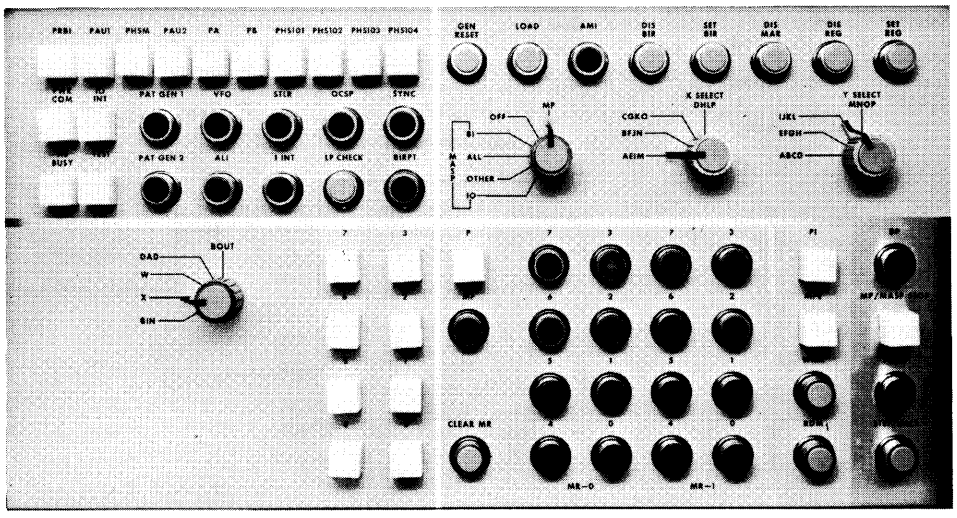


FIGURE 5. PROGRAMMER/MAINTENANCE PANEL

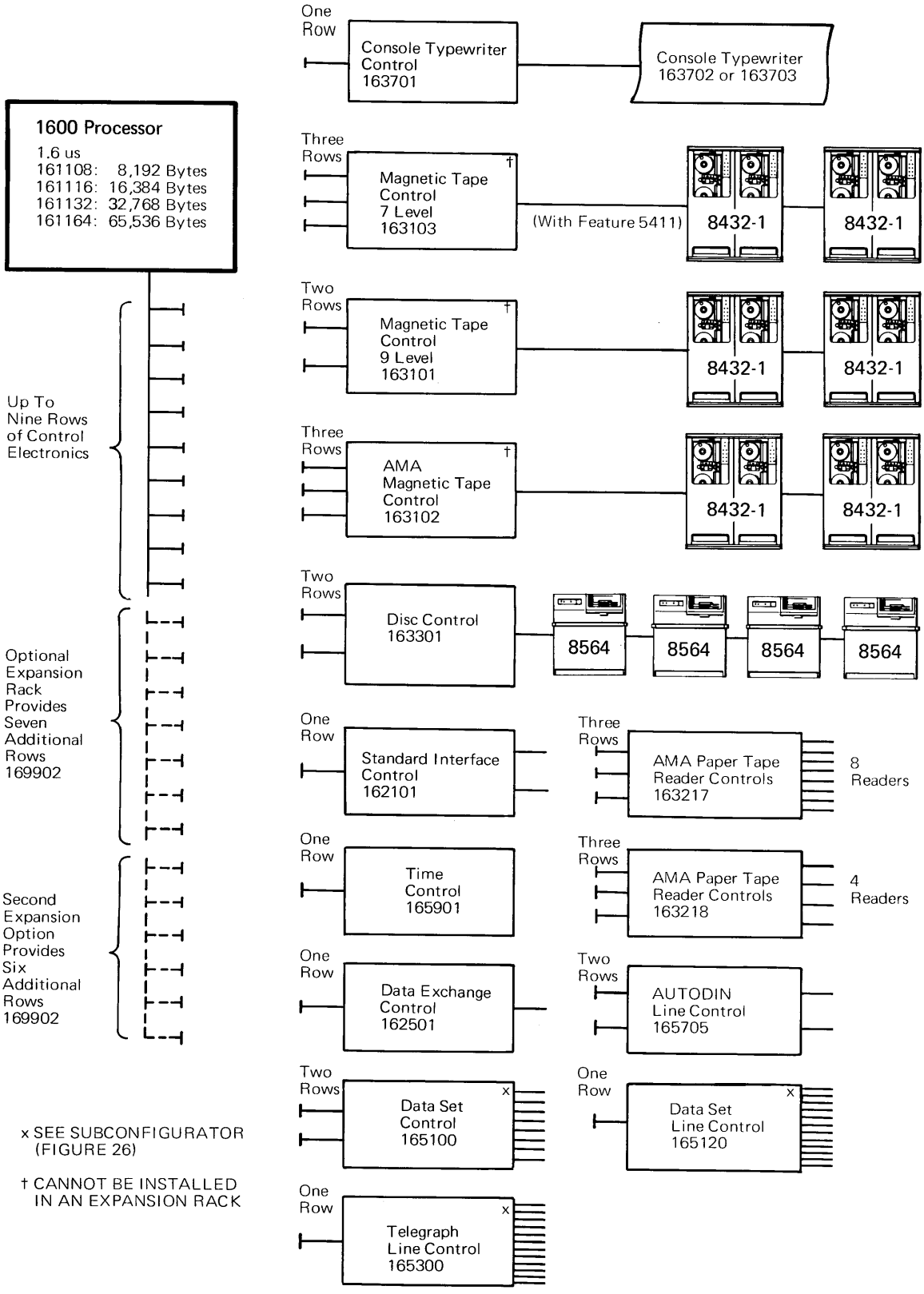


FIGURE 6. SYSTEM CONFIGURATOR

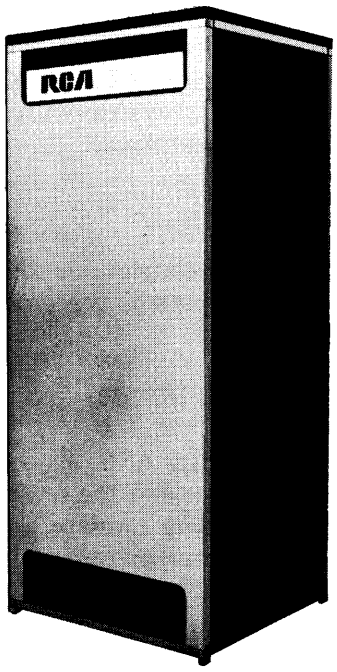


FIGURE 7. 1600 EXPANSION RACK

STANDARD INTERFACE CONTROL (COMPONENT 162101)

The Standard Interface Control occupies one row of space within the 1600 Processor rack, as shown in figure 8. This control is connected to RCA Series devices by means of the RCA standard interface cable.

The control contains a 1 X 2 switch (under program control only) to permit connection of one or two RCA devices of the same speed class. Only one RCA Series device can operate at a time.

The standard Interface Control provides the user of a 1600 Processor, the capability to program the commands and sequences required by the RCA standard interface.

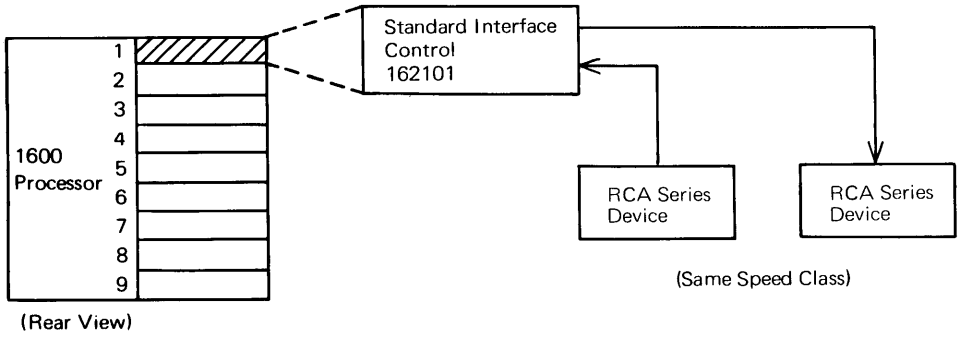


FIGURE 8. STANDARD INTERFACE CONTROL

CONSOLE TYPEWRITER

The Console Typewriter ASR or KSR is a modified teletypewriter that provides a complete subsystem with optional paper tape facilities capable of speeds of 100 words per minute.

Console Control (Component 163701)

The console control occupies one row of space within the 1600 Processor, as shown in figure 9. It permits typewriter operation as far as 100 feet from the 1600 Processor.

Console Typewriter ASR (Component 163702)

The Console Typewriter ASR, shown in figures 10 and 11, is an automatic send-receive typewriter and the most versatile member of the teletypewriter family. It is a complete message and data center. The ASR consists of a send-receive page printer, an optional tape punch and reader, all of which may be used in various combinations.

The ASR has all of the operational capabilities of the Console Typewriter KSR described later. The ASR typewriter is similar to the RCA Model 6740-21 Teletypewriter.

Console Typewriter KSR (Component 163703)

The Console Typewriter KSR is shown in figures 12 and 13. It can send and receive page-printed information and is equipped with a sprocket platen. Its keyboard and controls are similar to those of the Console Typewriter ASR.

Paper Tape Read (PTR) Feature (Component 163704)

The PTR Feature permits reading of light-level punched paper tape from the Console Typewriter at a speed of 10 bytes per second. It can be used to load programs at low speed.

This typewriter features an automatic keyboard lock. This mechanism senses an open-circuit condition and locks the keyboard to prevent any further transmission and loss of characters. Another important feature of the keyboard is that it generates even vertical parity for error detection. This typewriter is similar to the RCA Model 6741-21 Teletypewriter.

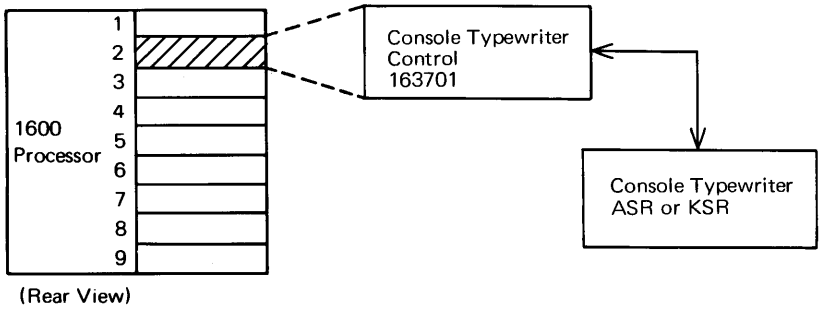


FIGURE 9. CONSOLE TYPEWRITER ASR OR KSR

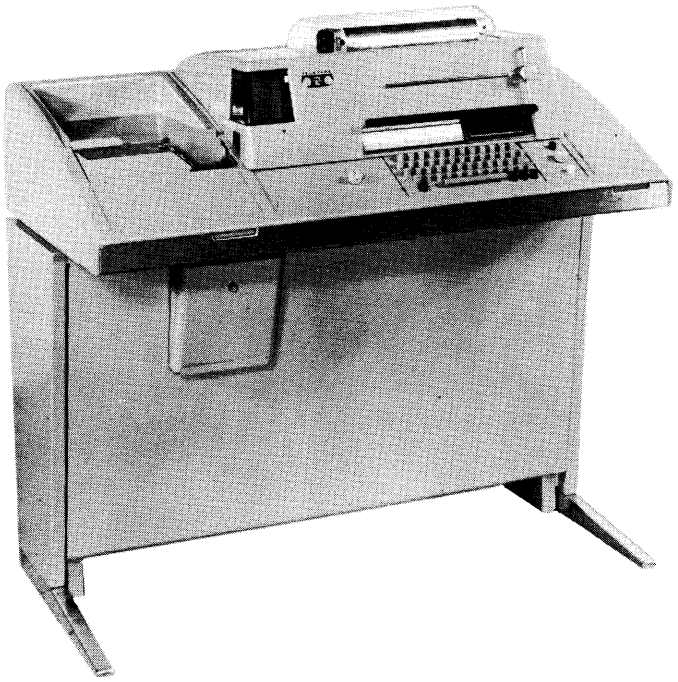


FIGURE 10. CONSOLE TYPEWRITER ASR

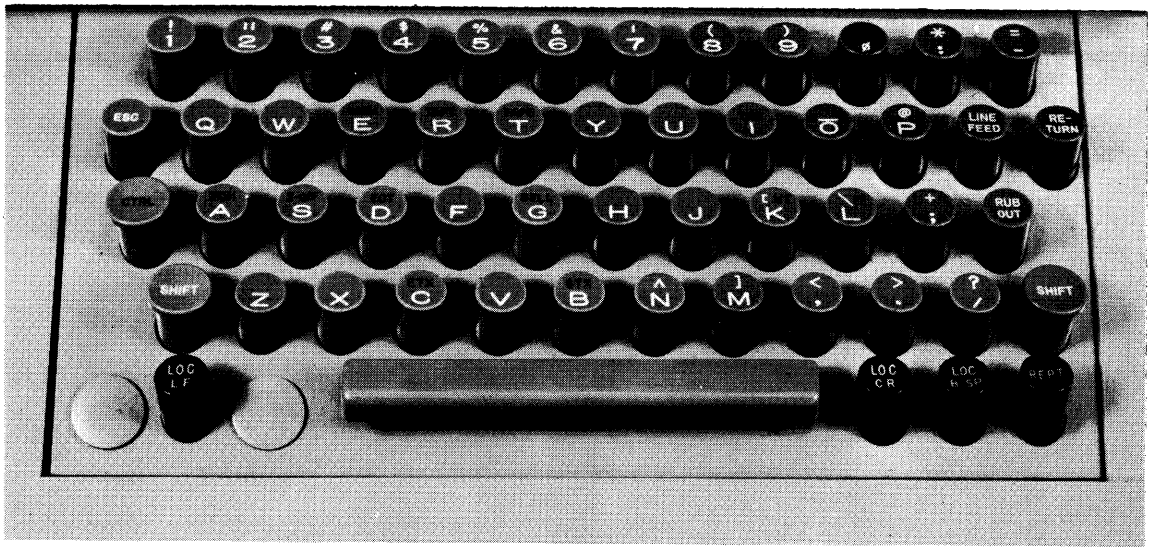


FIGURE 11. CONSOLE TYPEWRITER ASR KEYBOARD

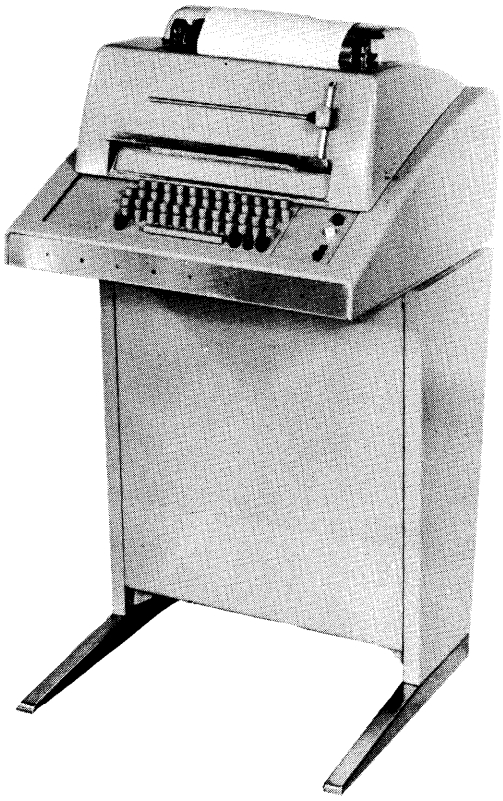


FIGURE 12. CONSOLE TYPEWRITER KSR

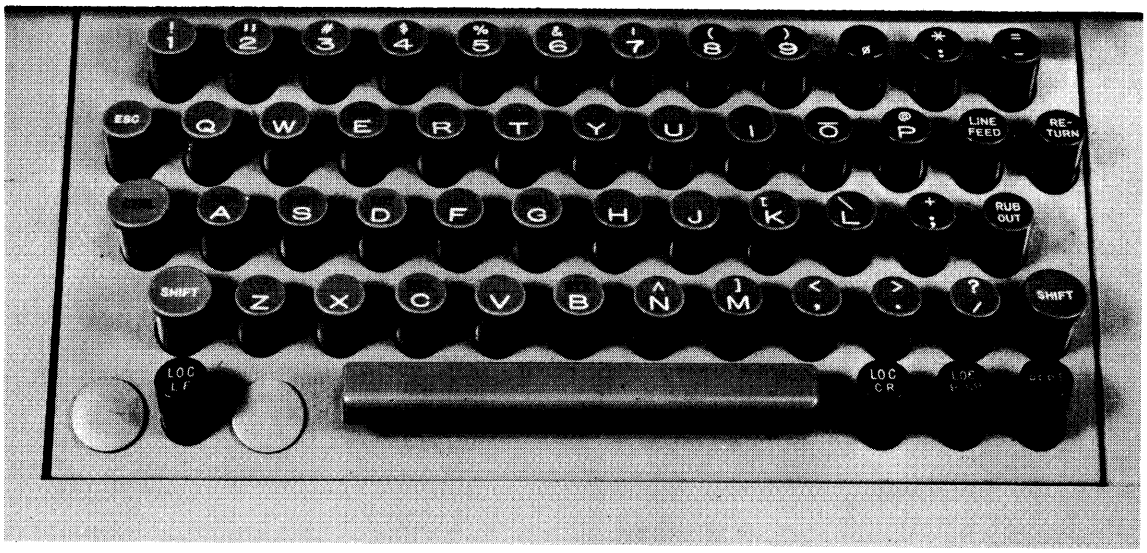


FIGURE 13. CONSOLE TYPEWRITER KSR KEYBOARD

The characteristics of the Console Typewriters ASR and KSR are listed in table 2.

TABLE 2. ASR/KSR CONSOLE TYPEWRITER CHARACTERISTICS

Code	8-level ANSCII, consisting of 1 spacing start-bit, 8 information bits forming even vertical parity, and 2 marking stop-bits.
PRINTER CHARACTERISTICS	
Platen	Sprocket feed for 8-1/2-inch continuous-fold business forms.
Speed	10 characters per second
Characters per inch	10
Characters per line	75
Lines per inch	6
Spacing	Single or double
Keyboard	4 row ANSCII
PAPER TAPE CHARACTERISTICS	
Type	8-levels 1-inch wide, fully perforated
Speed	10 characters per second
Density	10 characters per inch
Reel capacity	1000 feet

MAGNETIC TAPE EQUIPMENT

System components for processing magnetic tape are:

1. Magnetic Tape Control 9-level.
2. Magnetic Tape Control 7-level.
3. Magnetic Tape Control for special applications (see AMA Component).
4. 8432-1 Magnetic Tape Unit (dual drives).

Magnetic Tape Control 9-Level (Component 162101)

The Magnetic Tape Control (9-level) occupies two rows of space within the 1600 Processor, as shown in figure 14, and provides the means to connect one or two 8432-1 Magnetic Tape Units in a 9-level mode, 800-bits-per-inch, industry-compatible packing density.

For 9-level tape applications, the 8432-1 Magnetic Tape Unit is used with the Magnetic Tape Control (9-level). It permits tape operation as far as 50 feet from the 1600 Processor.

The Control permits one tape unit to be engaged in an on-line type of operation at a time. Read, write, and erase operations are performed serially and occupy the high-speed input/output channel. Off-line types of operation, such as rewind and unwind, may proceed concurrently on all units.

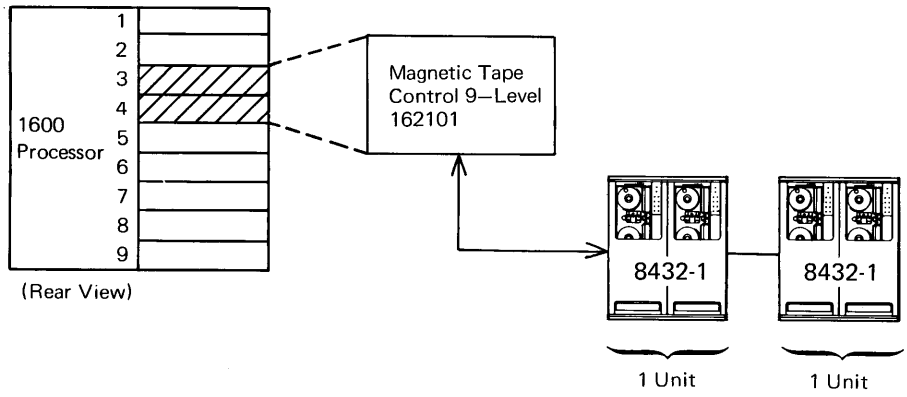


FIGURE 14. MAGNETIC TAPE CONTROL INTERFACE, 9 LEVEL

Magnetic Tape Control, 7-Level (Component 163103)

For 7-level tape applications, the 8432-1 Magnetic Tape Unit, with the 7-level feature 5411, is used with the Magnetic Tape Control (7-level).

The Magnetic Tape Control (7-level) occupies three rows of space within the 1600 Processor, as shown in figure 15, and is similar to Magnetic Tape Control (9-level) except that recording densities in the 7-level component are 200, 556, and 800 bits per inch under program control, at transfer rates of 7.5, 20.8, and 30.0 kHz, respectively, including pack/unpack capabilities.

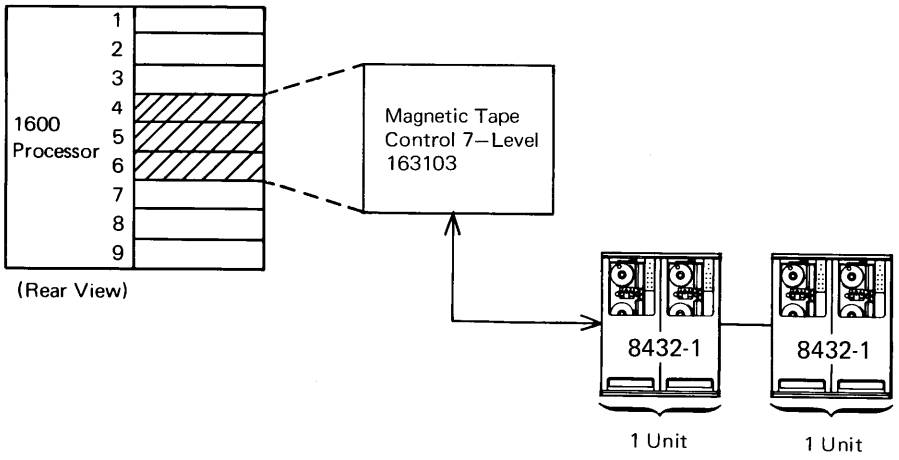


FIGURE 15. MAGNETIC TAPE CONTROL INTERFACE, 7-LEVEL

Model 8432-1 Magnetic Tape Unit

The Model 8432-1 Magnetic Tape Unit shown in figure 16 consists of two tape stations contained within one rack. Each tape station is capable of reading and writing ½ inch, 9-level, magnetic polyester tape at rates up to 30,000 bytes per second. Reading, writing, and erasing may be accomplished in the forward direction only. The Model 8432-1 Magnetic Tape Unit is completely compatible with all 800-bits-per-inch IBM 2400 Series Tape Units.

With Feature 5411, the 8432-1 Magnetic Tape Unit will read and write 7-level instead of 9-level tape. This Feature provides the ability to read and write tapes prepared on IBM 727, 729, 7330, and 2400 Series Tape Units and the RCA Model 3485 Tape Station (even parity, IBM mode).

Characteristics of this unit are listed in table 3.

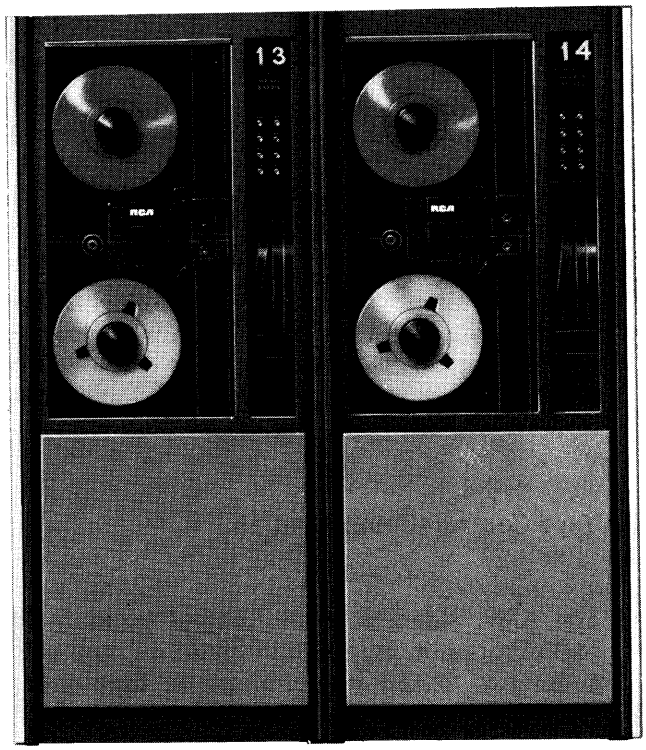


FIGURE 16. 8432-1 TAPE UNIT

TABLE 3. TAPE STATION CHARACTERISTICS

Characteristics	9-Level	7-Level
Data rate	30 kb	7.5,20.85, or 30 kHz
Tape speed (inches per second)	37.5	37.5
Tape rewind speed (inches per second)	100	100
Recording density (bits per inch)	800	200,556, and 800
Gap size (inches)	0.6	0.75
Tape parity	Odd	Odd or even (program selectable)
Average start/stop time (milliseconds)	16	20
Reel dimensions (inches)	10.5	10.5
Reel capacity (feet)	2400	2400

AUTOMATIC MESSAGE ACCOUNTING (AMA)

A special purpose control is available for Automatic Message Accounting (AMA) Conversion Systems used for off-line conversion of AMA Paper Tape and Magnetic Tape. This system is employed by the operating companies of the Bell System and is provided for telephone industry use.

AMA Magnetic Tape Control (Component 163102)

The AMA Magnetic Tape Control occupies three rows of space within the 1600 Processor, as shown in Figure 17, and is the interface between the RCA 1600, two 8432-1 9-level Magnetic Tape units, which accept magnetic tapes generated by the Bell System's Automatic Message Accounting System (AMA). When one of the 8432-1 tape units is reading an AMA Magnetic tape (written in ANSCII at 200 bits-per-inch, 9-level), the other tape unit writes the latter in the same format at 800-bits-per-inch EBCDIC.

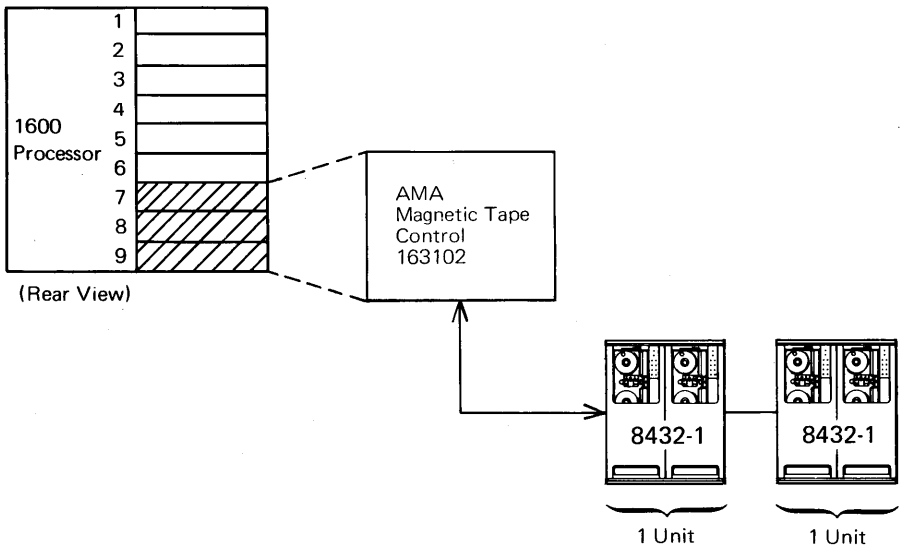


FIGURE 17. AMA MAGNETIC TAPE CONTROL INTERFACE

AMA Paper Tape Reader Control – Eight Readers (Component 163217)

The AMA Paper Tape Reader Control occupies three rows of space within the 1600 Processor, as shown in figure 18. It is the interface between the RCA 1600 and as many as eight Bell System AMA Paper Tape Readers. It permits data to be read into the RCA 1600. The output of this application is a magnetic tape recorded as 800-bit-per-inch EBCDIC.

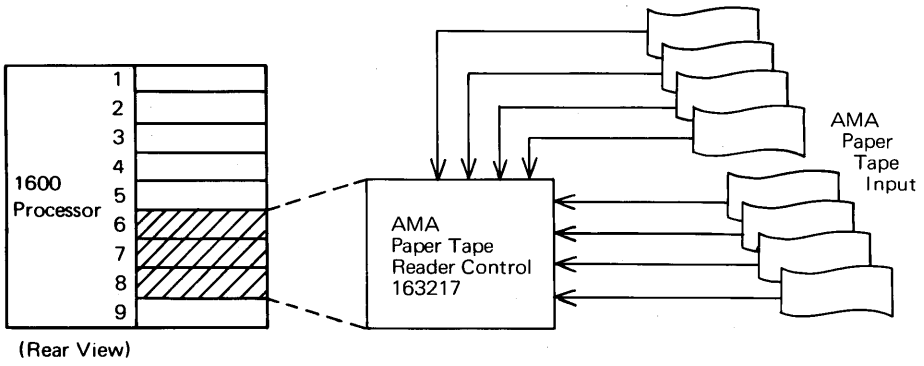


FIGURE 18. AMA PAPER TAPE READER CONTROL INTERFACE
(EIGHT READERS FURNISHED BY CUSTOMER)

AMA Paper Tape Reader Control - Four Readers (Component 1623218)

The Control shown in figure 19 is the same as AMA Control 163217 (described above), except that it serves as the interface between the RCA 1600 and as many as four AMA Paper Tape Readers.

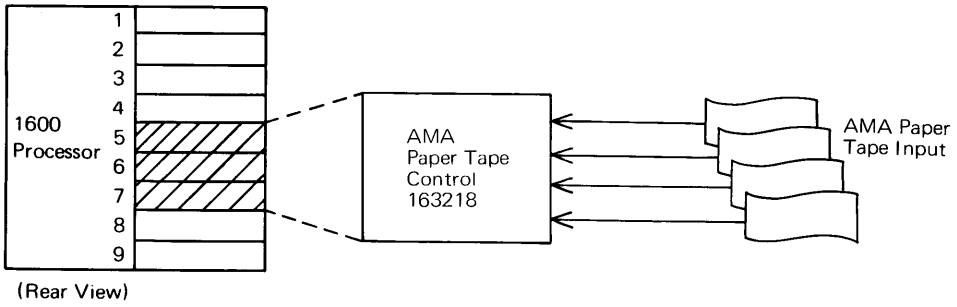


FIGURE 19. AMA PAPER TAPE READER CONTROL INTERFACE (FOUR READERS FURNISHED BY CUSTOMER)

AMA Cable, 25-Foot (Component 169951)

This cable connects the AMA Paper Tape Readers to either of the AMA Paper Tape Reader Controls.

AMA Cable, 50-Foot (Component 169952)

The function of the component is the same as that of Component 169951.

RAMDOM ACCESS

System components for discs are:

1. Disc Control
2. 8564 Disc Unit.

Disc Control (Component 163301)

The Disc Control occupies two rows of space within the 1600 Processor, as shown in figure 20. It permits disc operation as far as 50 feet from the 1600 Processor.

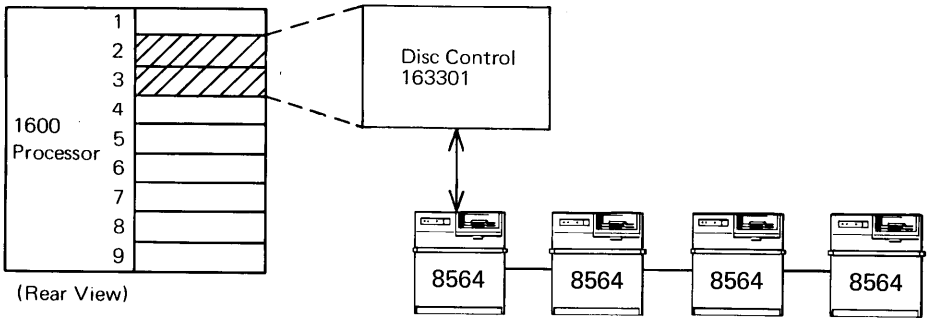


FIGURE 20. 8564 DISC CONTROL INTERFACE

The Disc Control is capable of operating up to four modified RCA Model 8564 Disc Storage Units by means of the 1600 Series high-speed channel. Only one drive may transfer data at a time. One drive may be seeking out a new track while the other drive is also seeking or transferring data. (Note that if non-RCA drives are employed, then only two alien drives are permitted, and the Disc Control, Component No. 163301, must be physically mounted within the 1600 Processor Main Frame.)

The Controller records information on RCA Model 506 Disc packs with a format incompatible with the formats used by other RCA Series Processors or with the IBM 2311. However, the controller has the ability to read an RCA-generated disc pack which has been uniquely written for this purpose. The pack remains removable and interchangeable. In this context, the term "interchangeability" denotes the ability of any Model 8564 Disc Storage Unit to read disc pack information previously written by any other Model 8564 Disc Storage Unit, regardless of which 1600 Controller created it.

Two levels of data buffering are provided in the Controller so that delays in response to data service requests will not cause service-request-not-honored conditions.

Model 8564 Disc Storage Unit

When the Model 8564 Disc Storage Unit, shown in figure 21, is equipped with an RCA Model 506 Disc pack, it provides random access storage for 7.58 million bytes when prepared by the Disc Control. Information is recorded at a density of 1100 bits per inch and transferred at a rate of 156 kilobytes per second.

FIGURE 21. 8564 DISC STORAGE UNIT

The 8564 Disc Units are slightly modified (sector pulses differ) when they are interfaced with a 1600 System Characteristics of this disc unit are listed in table 4.

TABLE 4. DISC UNIT CHARACTERISTICS

Transfer rate	156kb
Disc speed	2400 rpm
Positioning (seek) time	25 ms minimum 135 ms maximum 75 ms average
Rotational delay	25 ms (average latency 12.5 ms)
Track-to-track access time	25 ms
Maximum data record size	3774 bytes
Number of tracks per cylinder	10
Number of cylinders per unit	203
Number of tracks per surface	203
Number of tracks per head	203
Number of tracks per unit	2030

TIMER

The time-of-day control generates interrupts at specified intervals and is capable of being controlled externally by an optional impulse type master clock system.

TIME CONTROL (COMPONENT 165901)

The Time Control occupies one row of space within the 1600 Processor, as shown in figures 22 and 23. It generates, and makes available to the 1600 Processor, time-of-day records and generated interrupts at specified intervals.

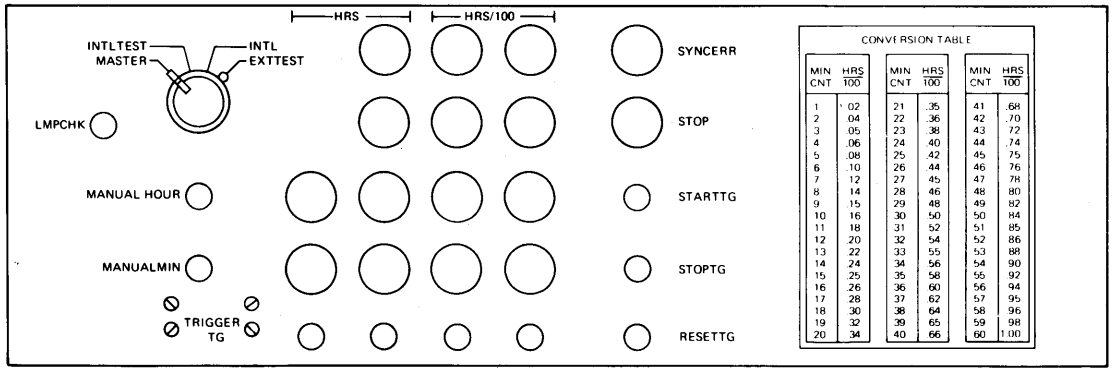


FIGURE 22. TIME CONTROL

The Time Control, which is driven from an internal or external source of 60-second pulses, maintains time-of-day data in the form H_{10}-H_1-$H_{0.1}$-$H_{0.01}$ where H is a digit (0 through 9) representing tens, units, tenths, and hundredths of an hour. $H_{0.01}$ has values 0, 2, 4, 5, 6, and 8, which represent time to the nearest hundredth of an hour. The Elapse Timer provides the 1600 with the capability of obtaining a program interrupt after a specified interval of time. The time interval is specified by a binary count (1-255). After a time change, the Time Control indicates time availability to the 1600 Processor. The Processor then causes the Time Control to read out two bytes representing the time of day, the least significant digit first. The basic time interval used by the Time Control is pin-board selected at installation. There are provisions for attaching the Time Control to an external master clock system. The selected time interval can be any of the following:

948 nanoseconds.

9.48 microseconds.

94.8 microseconds.

948.0 microseconds.

9.48 milliseconds.

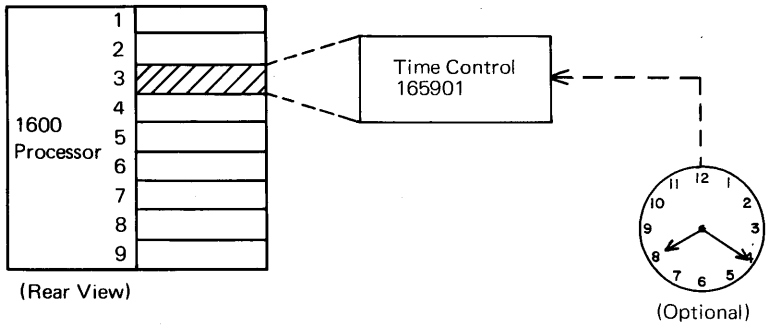


FIGURE 23. TIME CONTROL INTERFACE

DATA EXCHANGE

Memory-to-memory transmission permits direct connection between a 1600 System and an RCA Series System, or between a 1600 System and another 1600 System equipped with a Standard Interface Control, Component No. 162101.

DATA EXCHANGE CONTROL (COMPONENT 162501)

The Data Exchange Control occupies one row of space within the 1600 Processor, as shown in figure 24. It permits a 1600 Processor and an RCA Series Processor to transmit data from one to the other. It also permits a 1600 System and another 1600 System equipped with a Standard Interface Control, Component No. 162101, to transmit data from one to the other. Data transmission may be in either direction but in only one direction at a given time. Either computer can originate a transmission, provided that the proper program is available in each computer. Variable byte-length messages can be transmitted via the Data Exchange Control. The data transfer rate is variable, being dependent on the RCA Series Processor Channel and the 1600 Control program.

The 1600 Processor is connected to the controller via the 1600 I/O bus. The RCA Series Processor is connected to an RCA Series multiplex channel or selector channel. Operating mode selection by the 1600 program is independent of the type of channel to which the standard interface I/O trunk is connected.

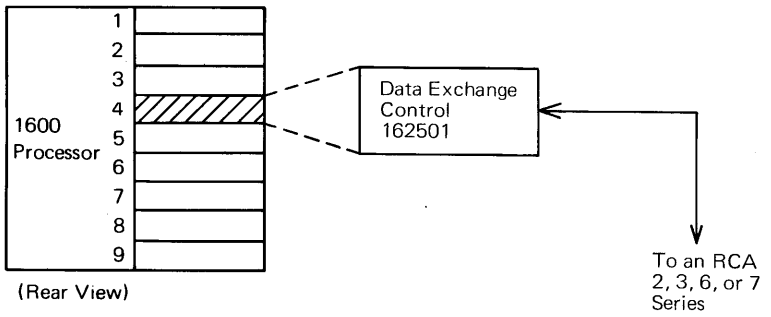


FIGURE 24. DATA EXCHANGE CONTROL INTERFACE

COMMUNICATIONS

The RCA 1600 communication capability is expanded into three areas:

1. Telephone (data set).
2. Telegraph (teletypewriter).
3. AUTODIN (Automatic Digital Network).

Each area is a well-designed extremely flexible "front-end." Listed in this section is a complete breakdown of the controls and their features, along with table of applicable data sets and their characteristics.

Data Set Control (Component 165100)

The Data Set Control occupies two rows of space within the 1600 Processor, as shown in figure 25. It is the communications interface to voice-grade telephone lines through AT&T (or equivalent engineering-approved) data sets. The Data Set Control (DSC) accommodates up to eight half-duplex or four full-duplex asynchronous or synchronous communication lines.

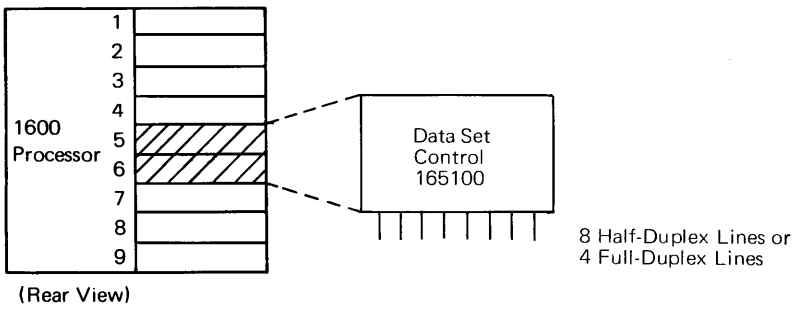


FIGURE 25. DATA SET CONTROL INTERFACE

Either a DSC Asynchronous Adapter or a DSC Synchronous Adapter must be specified for each half-duplex communication line. For full-duplex operation, a DSC Full-Duplex Interface must be specified (each interface modifies two DSC Adapters, either Asynchronous or Synchronous) to provide a full-duplex line. Refer to figure 26. The selection of Asynchronous or Synchronous Adapters is based upon the type of line required by the remote terminal.

The DSC controls the transfer of data characters between the processor memory and the data set adapter. Character recognition and generation, error detection, as well as all other aspects of communications line control, are accommodated by a processor Line Control Program.

Data Set Control Asynchronous Adapter (Component 165101)

As a subcomponent of the Component No. 165100 Data Set Control, one DSC Asynchronous Adapter is required for each half-duplex asynchronous line. For speeds up to 100 characters per second, the AT&T Data Set Model 202C is used for dial-network operations, and a Model 202D is used with leased/private line operations. For the lower speeds of 10 to 15 characters per second, the Model 103A is used for dial network operations, and the Model 103F is used for leased/private line operations.

Data Set Control Synchronous Adapter (Component 165102)

As a subcomponent of the Component No. 165100 Data Set Control, one DSC Synchronous Adapter is required for each half-duplex synchronous line. The AT&T Data Set Model 201A is used in dial-network operations, and the Model 201B is used in leased/private line operations.

Data Set Control Full-Duplex Interface (Component 165104)

A DSC Full-Duplex Interface is required for each asynchronous or synchronous full-duplex line. Two like adapters, either asynchronous or synchronous, are required for each full-duplex interface.

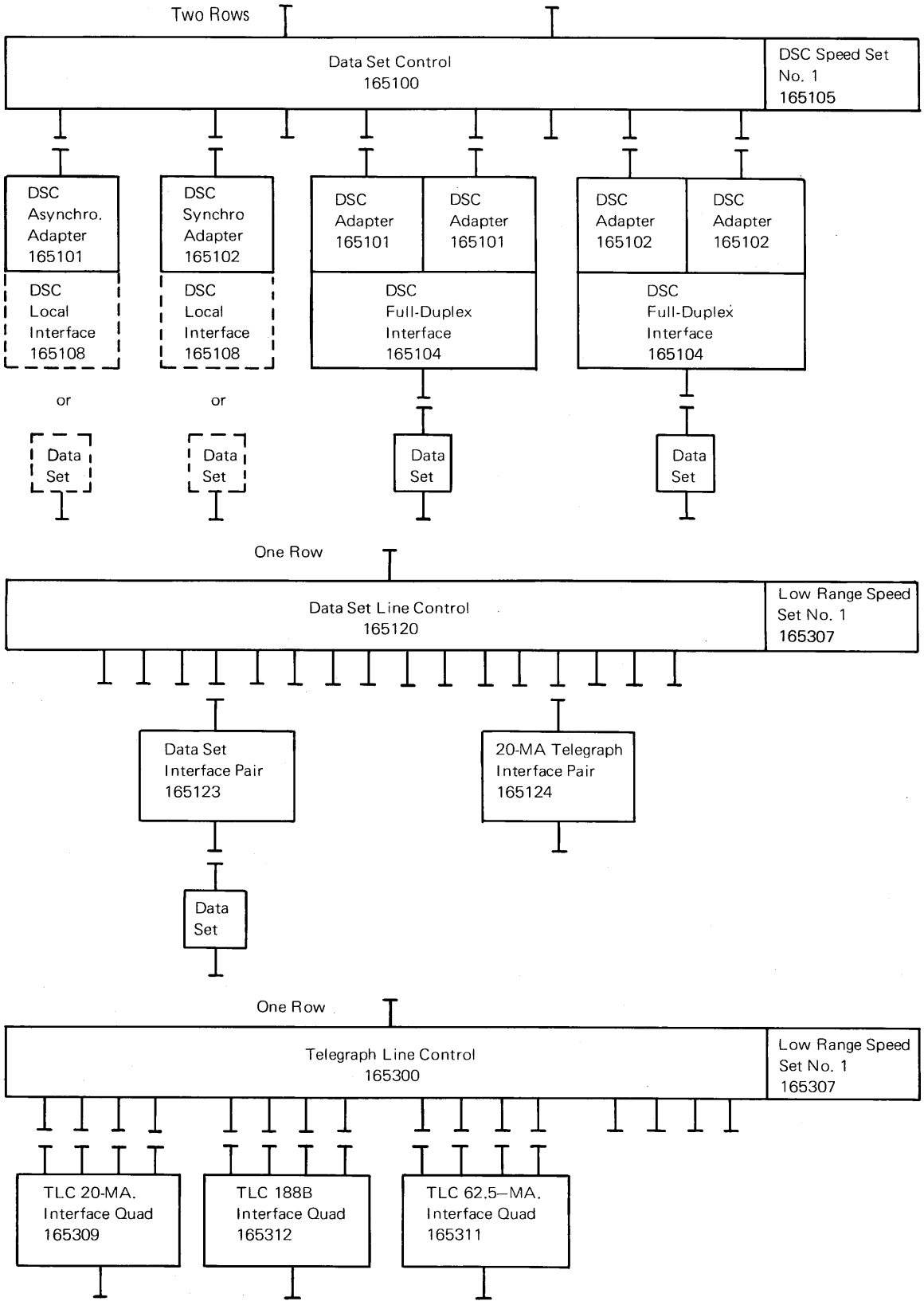


FIGURE 26. COMMUNICATIONS SUBCONFIGURATOR

Data Set Control Speed Set No. 1 (Component 165105)

The DSC Speed Set, which is an integral part of Component No. 165100 Data Set Control, is a clocking mechanism that synchronizes the baud rate over voice-grade lines. DSC Speed Set No. 1 sets a clock rate for the DSC of 110, 150, 1200, asynchronous bauds, and 2400 bauds for synchronous local interface.

Data Set Control Local Interface (Component 165108)

If the distance between the 1600 and the communications terminal or terminal control is less than 50 feet, the DSC Local Interface may be used rather than data sets at each end of the line. This is valid for either asynchronous or synchronous operation.

The data set subunits and their characteristics are listed in table 5.

TABLE 5. DATA SET SUBUNITS

Subunit	Component	Characteristics	Notes
Data Set Control	165100	Accommodates up to 8 half-duplex or up to 4 full-duplex adapters.	—
DSC Asynchronous	165101	Interfaces for Model 103A, 103F, 202C, or 202D data sets.*	1,2,5
DSC Synchronous Adapter	165102	Interface for Model 210A or 201 B data sets.*	2,3,5
DSC Full-Duplex Interface	165104	Enables two adapters to operate with the appropriate full-duplex data sets.	—
DSC Speed Set No. 1	165105	Supplies 110, 150, 1200 bps timing to the adapter.	—
DSC Local Interface	165108	Interface for a data terminal on a local basis without data sets, either synchronous or asynchronous.	1,4

*These data sets are manufactured by AT&T.

Notes:

1. Bit timing is provided by the controller. All transmitted signal elements are integral value.

2. Four-wire (or equivalent), half-duplex operation permitted for fast turnaround.

3. Bit timing is provided by the data set for operation at data speeds of 2000 or 2400 bits per second.

4. Bit timing is provided by controller for local operation without data sets.

5. Equivalent engineering-approved data sets can be substituted for the AT&T models listed in this table.

Two types of lines (private or dialed/switched network) can be accommodated by use of appropriate adapters. The characteristics of the adapters are listed in table 6.

TABLE 6. CHARACTERISTICS OF DATA SET CONTROL ADAPTERS

Type	AT&T Data Set	Service	Operating Characteristics
I	103A	Message network	Asynchronous, half-duplex
	103F	Message network	Asynchronous, half-duplex
	202C	Message network	Asynchronous, half-duplex
II	103A	Message network	Asynchronous, full-duplex
	103F	Message network	Asynchronous, full-duplex
	202D	Private line	Asynchronous, full-duplex
III	201A	Message network	Synchronous, half-duplex
IV	201B or 201A	Private line	Synchronous, full-duplex

Data Set Line Control (Component 165120)

The Data Set Line Control occupies one row of space within the 1600 Processor, as shown in figure 27, and interfaces up to 16 AT&T data sets.

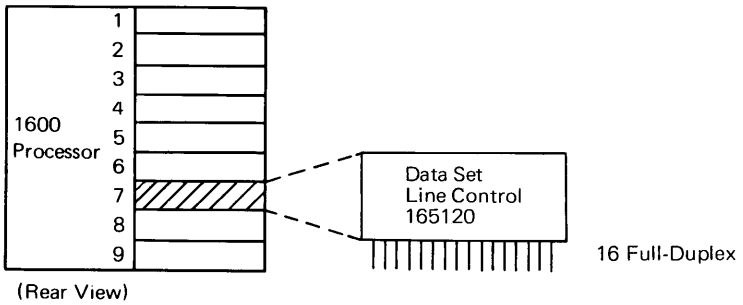


FIGURE 27. DATA SET LINE CONTROL

The Data Set Line Control, controls the transfer of data bits between the 1600 Processor memory and adapters located within the Data Set Line Control. Character assembly, character disassembly, deletion and insertion of stop-start bits as well as all other aspects of communications line control are accommodated by the 1600 Processor program.

Each adapter (components 165123 and 165124) within the Data Set Line Control, operates full duplex, asynchronously at data speeds as determined by the internal Low-Range Speed Set No. 1 (Component 165307). Provisions are also made to permit operation with telegraph lines utilizing 20-milliampere neutral signalling.

A built-in interval timer generates interrupts once every 100-milliseconds, and provides the software with a time base which can be used for timing intercharacter gaps, polling responses, and other control functions.

Data Set Interface Pair (Component 165123)

This subcomponent of the Data Set Line Control enables two adapters to interface two AT&T Model 103A/F data sets or equivalent engineering-approved data sets.

Telegraph 20-Milliampere Interface Pair (Component 165124)

This subcomponent of the Data Set Line Control enables two adapters to interface two telegraph lines which utilize 20-miliampere neutral signalling.

Low-Range Speed Set No. 1 (Component 165307)

The Low-Range Speed Set No. 1 is a clocking device that synchronizes the baud rate over the interfacing lines. The speed set establishes a clock rate for the DSLC at 75, 110, and 150 bits-per-second. However, only two clock rates out of the given three can be utilized in any combination. The Data Set Line Control subunits and their characteristics are listed in table 7.

TABLE 7. DATA SET LINE CONTROL SUBUNITS

Subunit	Component	Characteristics	Note
Data Set Line Control (DSLC)	165120	Accommodates up to 16 adapters and associated interface units.	1
Data Set Interface Pair	165123	Includes 2 adapters with two 103A/F data set* interfaces.	2,4,5
Telegraph 20-ma Interface Pair	165124	Includes 2 adapters with two 20-ma neutral interfaces.	3,4
Low-Range Speed Set No. 1	165307	Supplies 75, 110, or 150 bits-per-second timing to the adapter	

* This data set is manufactured by AT&T.

Notes:

1. Data Set Line Control (Component 165120) consists of DSLC control logic, an Interval Timer, and a Low-Range Speed Set No. 1 (Component 165307).

2. Data Set Interface Pair (Component 165123) consists of two DSLC Adapters and two Data Set Interfaces.

3. Telegraph 20-milliampere Interface Pair (Component 165124) consists of two DSLC Adapters and two 20-ma Telegraph Interfaces.

4. Each Adapter within the Interface Pair is separately addressable.

5. Equivalent engineering-approved data sets can be substituted for the AT&T model listed in this table.

Video Data Systems

Video Data Terminals can be used with the 1600 in a variety of ways, as shown in Appendix B. The following RCA Series video data equipment along with their applicable features can be used with the 1600 system:

8751 Video Data Terminal (VDT).

8752-100 Video Data Terminal (VDT).

8752-200 Video Data Terminal (VDT).

8755-200 Video Data Switch (VDS).

8756 Video Data Generator (VDG).

8759 Video Data Control (VDC).

Telegraph Line Control (Component 165300)

The Telegraph Line Control occupies one row of space within the 1600 Processor, as shown in figure 28. It provides control of up to 16 half-duplex teletypewriter lines or as many as eight full-duplex teletypewriter lines for bit-serial transmission of data up to 150 bits per second.

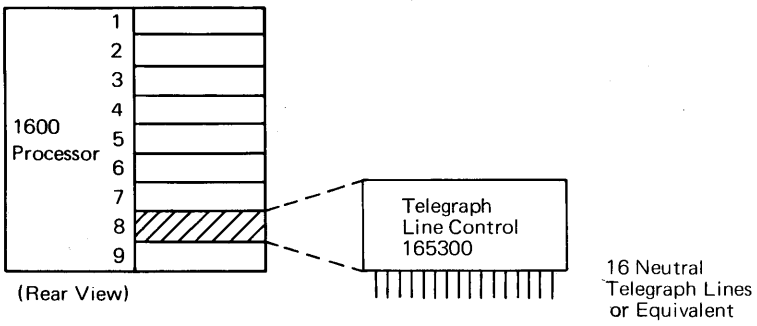


FIGURE 28. TELEGRAPH LINE CONTROL INTERFACE

Either 20-milliampere lines or 62.5-milliampere lines can be interfaced, depending on the remote device requirement.

Line adapter-interfaces are packaged in sets of four and are specified as quads. Refer to figure 26. Proper interface quads No. 165309 or 165311 are required as stated below.

Telegraph Line Control, 20-Milliampere Interface Quad (Component 165309)

This component provides the adapter-interface for up to four 20-milliampere telegraph circuits.

Telegraph Line Control, 62.5-Milliampere Interface Quad (Component 165311)

Provides the adapter-interface for up to four 62.5-milliampere telegraph circuits. Table 8 lists the Telegraph Line Subunits and their characteristics.

TABLE 8. TELEGRAPH LINE SUBUNITS

Subunit	Component	Characteristics	Note
Telegraph Line Control	165300	TLC will accommodate up to four 20-ma interface quads or any four 62.5-ma interface quads or any four of combinations of above quads.	3
TLC 20-ma Interface Quad	165309	Includes four adapters with 20-ma interface.	3
TLC 62.5-ma Interface Quad	165311	Includes four adapters with 62.5-ma interface.	1,2
TLC 188B Interface Quad	165312	Includes four adapters with 188B Interface	4,5
Low Range Speed Set No. 1	165307	Provides bit timing to adapters operating at 75, 110, or 150 bits-per-second.	

Notes:

1. Battery for this interface is supplied by the user, common carrier, or by Power Supply Model 6793.

2. Maximum open circuit voltage that can be applied to this interface is 270 volts.

3. This interface supplies battery. The transmission path can be up to 1 mile long.

4. TLC's using a 188B Interface cannot accommodate either the 62.5-ma or 20-ma Interface.

5. All connections between the line interface and the 1600 will be through a twisted-pair connection which is less than 750 feet long. Each buffer will require one twisted pair in the simplex mode and two twisted pairs in the half-duplex mode. Screw connections are provided for the conductor, conductor ground, and possible shielded covering.

Telegraph Line Control 188 B Interface Quad (Component 165312)

Refer to Military Communications Systems Standard MIL-STD 188 B.

Low-Range Speed Set No. 1 (Component 165307)

The functions of this component are the same as those described under Data Set Line Control.

AUTODIN

The AUTODIN Line Control, as shown in figure 29, provides the 2400 or 4800 bit-per-second synchronous interface to the Department of Defense Automatic Digital Network, AUTODIN. The Control includes a full-duplex Synchronous Line Adapter, Terminal Control Panel, and Junction Box.

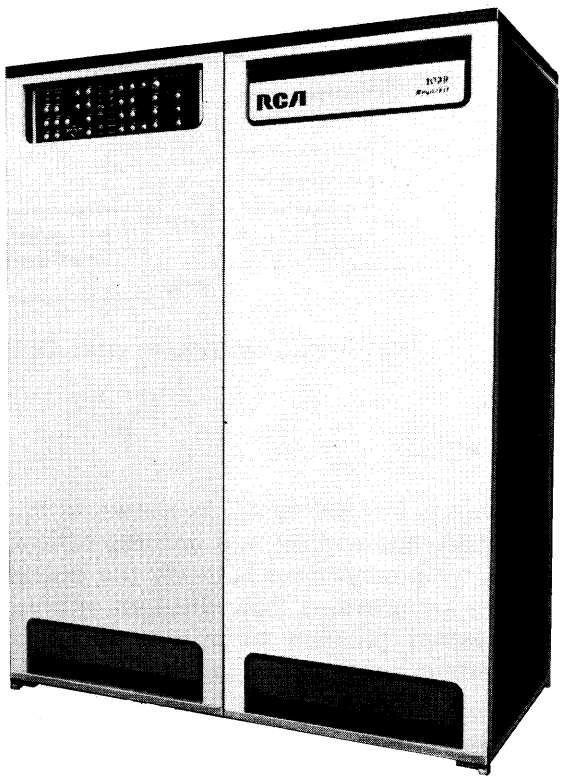


FIGURE 29. AUTODIN LINE CONTROL

A 1600 System can utilize this control in conjunction with other 1600 System components for AUTODIN interface to function as a remote AUTODIN message exchange terminal.

Functional AUTODIN interface program modules are available to provide line control. The line control procedures implemented are as described in the AUTODIN criteria specifications.

AUTODIN Line Control (Component 165705)

The AUTODIN Line Control occupies two rows of space within the 1600 Processor, as shown in figure 30, and interfaces the AUTODIN Network (overseas or continental United States). The operation is full-duplex and synchronous at speeds of 150, 300, 600, 1200, 2400, or 4800 bits per second. The data transfer between the controller and the line is bit-serial with the least significant bit transferred first. The data transfer between the controller and the 1600 Processor is eight-bit parallel-character serial.

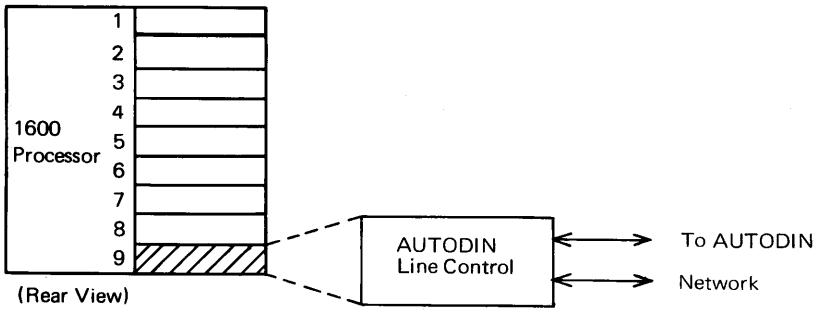


FIGURE 30. AUTODIN LINE CONTROL INTERFACE

Controls and Indicators

A Terminal Control Panel, as shown in figure 31, is a component of the AUTODIN line control and consists of a display/control panel. The panel permits communication between the operator and the controller. Control switches are provided that, when set or pressed by the operator, instruct the fixed stored program to assume specific operational status or execute predetermined routines.

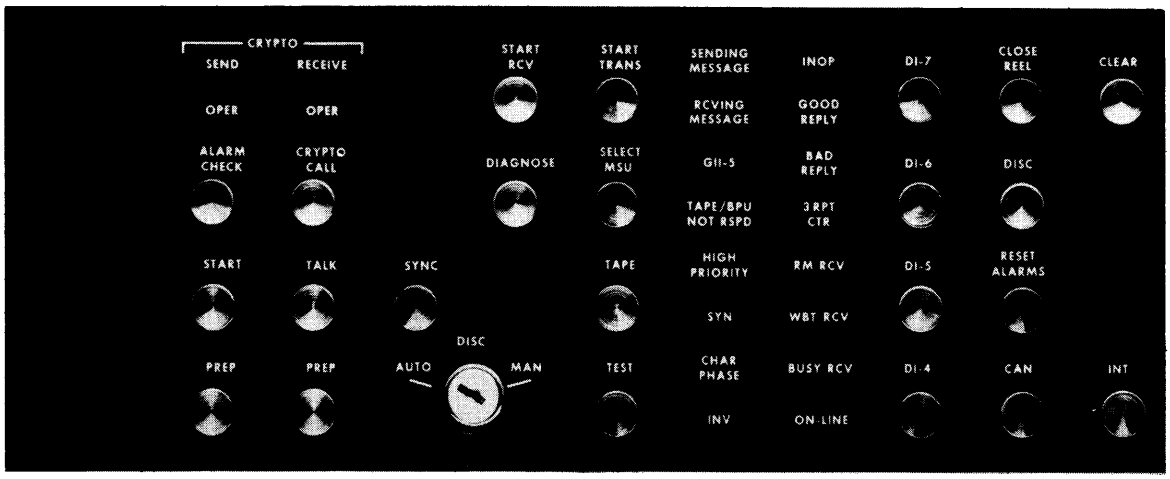


FIGURE 31. AUTODIN TERMINAL CONTROL PANEL

The following signals can be connected to customer-supplied external alarm systems.

1. A signal to indicate that dc power has failed.

2. A signal to indicate that the audible alarm is ON.

3. A signal to indicate that the 13-second timer on the operator's panel has expired.

The indicators are turned on or off by the fixed stored program. They display status or alarm conditions that may be of interest to the operator or to maintenance personnel, or that require operator intervention. An audible alarm is provided that can be activated independently or in conjunction with one or more indicators.

The controls and indicators on the panel are accessible and clearly marked.

4. PROGRAMMING SYSTEMS

The RCA programs developed to support the 1600 System can be divided into two categories: the first category includes Programs which operate on RCA Series Processors under the Tape Operating System (TOS) or Tape Disc Operating System (TDOS) environment; the second category includes support software which operates on the 1600 Processor.

1600 SOFTWARE

The Macro Assembler, the Simulator, and the Format Converter operate on RCA Series Processors.

Macro Assembler

The Macro Assembler is a machine-oriented, symbolic-programming, language processor that operates on an RCA Processor to expedite the writing of programs for the 1600 Processor. The programming language consists of five basic types of statements: symbolic machine instructions, assembler control statements, macro instructions, extended machine instructions, and comment statements.

Symbolic machine instructions are one-for-one symbolic representations of 1600 Processor machine instructions. The Assembler produces an equivalent machine instruction in the object output for each symbolic machine instruction encountered in the source input.

Assembler control statements provide auxiliary functions that assist the programmer in checking, documenting, and debugging his program, as well as in controlling the assignment of memory location, in defining input/output constants and storage areas, and in controlling the Assembler itself. With few exceptions, these statements do not result in the generation of object output.

Macro instructions enable the programmer to retrieve specially coded symbolic routines from preestablished libraries. These routines may be modified according to information specified within the macro instruction and incorporated as source statements.

Extended machine instructions are mnemonic codes that permit the programmer to specify two or more symbolic machine instructions with a single line of coding.

Comment statements permit the programmer to annotate the program listing prepared by the Assembler.

The Macro Assembler produces an object program output and a program listing. The object program output is the machine language equivalent of the source input in loadable card-image format. The program listing is a graphic representation of the source and object program. It reflects each source statement and the equivalent, machine language generated for it by the Assembler. Errors detected in the source input are indicated through a flag (or flags) recorded on the listing. The programmer has partial control over the format and content of the listing. The object output of the Assembler is a card deck (or card images on magnetic tapes) in a format which permits a program to be loaded into the designated area of 1600 memory. Object output is relocatable and consists of six card types:

1. External Symbol Dictionary Card (ESD) – Identifies the external symbol dictionary.

2. Test Card (TST) – Contains the program instructions, data, and constants.

3. Relocation Card (RLD) – Contains the relocation dictionary.

4. End Card (END) – Designates the end of the program deck and specifies a beginning execution address.

5. Transfer Card (XFR) – Specifies a beginning execution address for a program phase.

6. Memory Protect Card (MPD) – Contains the memory protect dictionary.

Each object card contains an identification field and a sequence number. Each text card specifies the number of bytes of text that it contains and the memory loading address of the text.

The program listing is a graphic representation of the program processed by the Assembler. It serves as documentation of the program and as an aid to program debugging and checkout.

The listing reflects the symbol table compiled by the Assembler and shows the memory address associated with each symbol in the table.

Each source language statement is recorded on the listing with the memory location assigned to the resultant object output, the actual machine language equivalent of the statement, and the sequence number of the object card containing it. Error flags appear on the listing for those statements in which errors have been detected.

The comment statement permits the programmer to annotate his program listing for purposes of documentation. Through assembly control statements, the programmer may specify heading lines for his listing and control page changing.

Macro Assembler Interface

The object program output of the Macro Assembler may be fed directly to the 1600 Simulator for execution. If the object program is to be executed on the 1600 Processor, it may be fed through a program format converter to produce a reformatted version of the object program on magnetic tape or punched paper tape.

1600 Simulator

The 1600 Simulator loads the object program output of the 1600 Macro Assembler and simulates the execution of the 1600 program. The simulator operates on the RCA Series Processors.

The simulator provides simulation of the internal 1600 commands and, where feasible, simulation of peripheral commands. Special facilities are provided for 1600 Disc Simulation.

Since the primary objective of the simulator is the facilitation of program checkout, the 1600 Simulator includes a complete set of diagnostic aids. This includes full and partial trace, static and dynamic memory dumps, instruction stops, and operator console control.

Input

Input to the 1600 Simulator consists of object programs in assembly output format and control statements which specify the parameters required to control and direct simulator operation.

Object Program

Object programs to be executed by the simulator must be in the standard format prescribed by the 1600 Macro Assembler. Input may be entered into the system from card or card images on magnetic tape.

Control Statements

The operation of the 1600 Simulator is directed through control information provided through the job stream and by operator console messages. The job stream control statements include parameters which may specify:

1. Dump Points.

2. Trace Points.

3. Input/Output Devices.

4. Address Halts.

Through console messages, the operator may direct the simulator to:

1. Display and/or change the contents of 1600 memory.

2. Display and/or change the contents of specified 1600 registers.

3. Eliminate or assign instruction halts.

4. Eliminate dump and/or trace points.

5. Terminate the 1600 program simulation.

6. Continue simulation after program halt.

Output

The 1600 Simulator produces the following output:

1. Console Log – Reflects all console messages, commands, control statements, and requested displays.

2. Diagnostic Listings – Includes static and dynamic memory dumps and trace output. All trace output and memory dumps are written to magnetic tape and printed at simulator termination.

3. Input/Output Log – Reflects each instruction that has been operated with or addressed in an input/output register.

1600 Diagnostics

The Diagnostics are initiated through control statements and console commands. They produce the following output data:

1. Trace Dump – The simulator will execute a complete or selective type trace dump as directed by control statements.

2. Memory Dump – Initiated at program initiation, termination, or at selected 1600 Processor operating locations within the program through control statements and operator requests. A memory dump is automatically provided on termination.

3. Address Stop – Interrupts the simulator and turns control over to the console routines. The address stop is initiated by control statements and/or console requests.

4. Console Display – When the simulator is interrupted, control is given to the console routines. These routines allow the operator to display and/or change 1600 memory locations and registers through console requests.

Program Format Converter

The Program Format Converter reformats the card image output of the Macro Assembler and creates loadable 1600 programs on a different input media. Converter output may be punched paper tape or magnetic tape. The diagram on the next page illustrates the flow of programs through the Phase I 1600 software system.

Basic Assembly

The Basic Assembler converts programs from symbolic language to object coding. The symbolic language corresponds to that defined for the Macro Assembler; however, macro capabilities are not available.

The system operates on a 16-kb minimum processor and provides for input from punched cards, punched paper tape, or magnetic tape. Output from the card and magnetic tape versions is applied to a magnetic tape and a printer. Output from the paper tape version is recorded on punched paper tape and a keyboard printer. All input and output functions are controlled through the 1600 Input/Output Processing System.

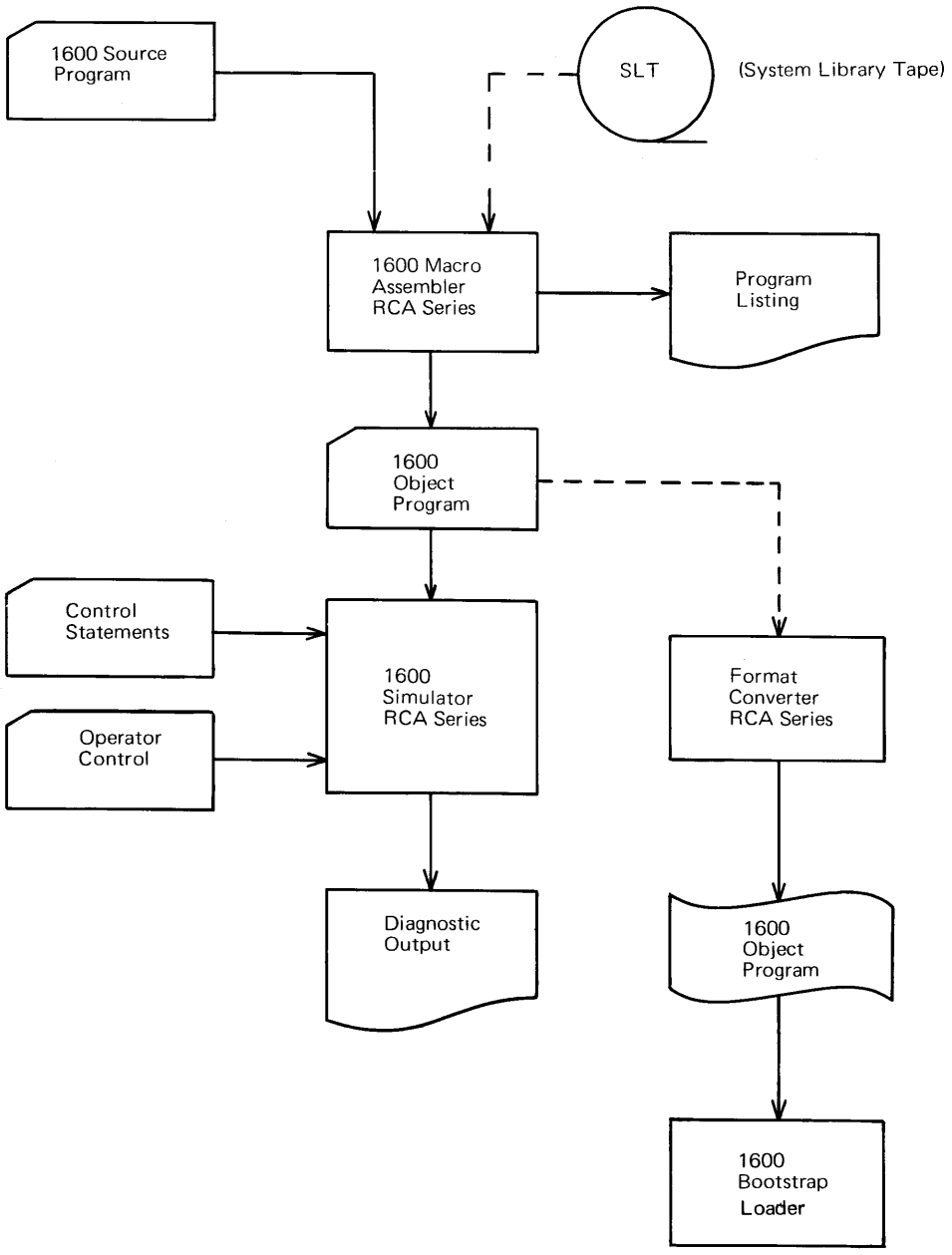


FIGURE 32. ASSEMBLY FLOW

Bootstrap Loaders

The 1600 Bootstrap Loaders load programs into the 1600 Processor for execution. They are free-standing 1600 programs which are brought into processor memory through the 1600 Processor's LOAD function. Loaders are provided for the 1600 Console Typewriter's paper tape reader and for 9-level magnetic tape.

The bootstrap loaders process assembler output which has been formatted to paper tape or magnetic tape. They load text data into the processor memory at the assembled origin. The object program receives control at the address specified in its END or XFR record. The bootstrap loaders do not support relocation.

Standard Loaders

The 1600 Standard Loaders provide the facilities for translating the object output of the 1600 assemblers into executable programs in processor memory. Loaders support the RCA 8237 Card Reader, 8432-1 magnetic tape, 7-level or 9-level, and DXC through RCA Series and disc.

The punched card and magnetic tape loaders permit the loading of multiple module programs and support a limited relocation, or "float" capability. Both loaders use the facilities provided by the 1600 Input/Output Processing System for I/O control. They must be loaded into memory by one of the 1600 bootstrap loaders.

Input/Output Control Software

The 1600 Input/Output Processing System (IOPS) provides input/output support for Phase II 1600 software and for 1600 user programs. It is a generalized, physical level input/output control system that includes facilities for controlling the following 1600 input/output devices:

7-Level Magnetic Tape.

9-Level Magnetic Tape.

Standard Interface Control Electonics.

8242 or 8243 Printer.

8237 Card Reader.

8234 or 8236 Card Punch.

Console Typewriters.

Data Exchange Controls.

Terminal Control Panel.

Time Control.

Data Set Control.

Telegraph Line Control.

Disc Control.

IOPS is presented as a series of macros which may be assembled into an object program through the 1600 Macro Assembler. Generally speaking, IOPS cannot be assembled using the Basic Assembly System, which operates on the 1600 Processor.

IOPS consists of (1) an input/output processor that initiates, controls, and services peripheral devices, and (2) a series of interrelated tables and calling sequences that control the operation of the I/O processor. The I/O processor must be assembled using the 1600 Macro Assembler; however, tables and calling sequences may be coded in the user program and assembled using the Basic Assembler. The interfaces between the object program and the I/O Processor may be accomplished by use of EQU statements. This technique permits the user to assemble his I/O processor at a fixed location and to assemble object programs that use IOPS with the Basic Assembly System on the 1600 Processor.

Error analysis is provided within the I/O processor for all devices supported by IOPS. Error recovery facilities are provided for all I/O devices except the card punch. Card punch error recovery must be handled by the user program.

UTILITIES

The 1600 Utility System consists of a set of programs and routines of general usefulness to 1600 System users. The utility routines are functionally grouped into five categories: Conversion, Loader, Service, Subroutine, and Diagnostics.

Conversion Routines

Conversion routines are provided to convert standard RCA Series input format to 1600 System format. There are two such routines: MTFC and PTFC.

MTFC

The Card/Magnetic Tape Format Converter (MTFC) converts program output of the Assembler to a magnetic tape format acceptable for loading by the Bootstrap Loader – Nine Level Magentic Tape (BLMT). It also validates and sequence checks all program input and optionally provides for the maintenance of previously created program load tapes.

PTFC

The Card/Paper Tape Format Converter (PTFC) produces loadable paper tape input for the 1600 Processor. The PTFC transcribes Assembler output on eight-channel paper tape in a format that is acceptable to the Bootstrap Loader – I/O Typewriter.

Loader Routines

The loader routines provide the means for loading 1600 System formatted programs into the processor for exectuion. The loader routines consist of the following routines: BLMT, CLDRS, and MTLDR.

BLMT

The Bootstrap Loader, Nine-Level Magnetic Tape (BLMT) is a freestanding routine that processes 1600 Basic Assembler output on 1600 Macro Assembler output that has been formatted to paper tape. BLTW and the program that it loads are recorded on eight-channel paper tape.

CLDRS

Card Loader-SICE (CLDRS) loads, for execution, programs that have been processed by one of the 1600 Assemblers. Programs to be loaded must conform to the card-image format prescribed by the 1600 Assemblers. They must be input through a Model 8237 Card Reader that is connected to the 1600 Processor through a Standard Interface Control Electronics (SICE).

The Card Loader routine must be loaded by one of the 1600 Bootstrap loaders. It cannot be loaded by the processor's initial load function. Input to the Card Loader routine consists of 1600 System Assembler output in card-image format.

MTLDR

The Nine-Level Magnetic Tape Loader (MTLDR) loads programs that have been processed by the 1600 System into the 1600 processor for execution. Programs must conform to the tape format prescribed by the 1600 System Basic Assembler. They must be input through a Model 8432-1 Magnetic Tape Unit attached to MT-9 CE. The Magnetic Tape Loader can be loaded by one of the 1600 System bootstrap loaders or by the Card Loader-SICE. It cannot be loaded by the Processor's initial function.

Input to this loader consists of 1600 System Basic Assembler output, the Breakpoint indicator, and parameters that are entered through the Programmer's and Maintenance Console.

Service Routines

System Service Routines

The 1600 Disc Initializer (DKINI) is a utility program that prepares 506 disc packs for processing by Series 1600 programs. The 506 disc pack is mounted on an RCA 8564 disc drive attached to a 1600 Disc Control Electronics. Before using this program, the user should be familiar with the operation of the Series 1600 Disc Control.

The Disc Initializer is designed as a macro and must be assembled as described in the 1600 Basic Assembly System Reference Manual.

All input/output functions within the program are performed as described in the 1600 System Input/Output Processing System Reference Manual.

Program functions are selected by submitting Control Statements through an input parameter device. The program processes Control Statements individually; that is, it requests a Control Statement, validates it, and, finding it valid, performs the functions requested. Thus, the program is perpetually self-initializing, and the various functions can be individually and repeatedly performed with a single program load.

Subroutine Systems

The 1600 Subroutine System is a collection of macro subroutines designed to assist the user in accomplishing various commonly required arithmetic functions. The subroutines are as follows:

BDIV	Binary Divide.
BMPY	Binary Multiply.
BTOD	Binary to Decimal Conversion.
DTOB	Decimal to Binary Conversion.

Input to the subroutines consists of the macro call and parameters required to generate the subroutine and the actual object data to be processed by the subroutine.

Output of the subroutines consists of the coding generated in response to the macro call with parameters and the result produced by the subroutine when executed as part of the user program.

Basically, the macro subroutines fall into two categories: those that generate in-line coding, and those that generate a calling sequence to out-of-line coding. The first type generates substantially the same lines of coding each time it is called. The second type generates the subroutine coding as well as the calling sequence to the subroutine on the first occurrence. On subsequent calls, it generates only the calling sequence.

Diagnostic Routines

Diagnostic routines are provided for program testing. The routines included with diagnostic functions are listed as follows:

DKPRT	Disc Print - SICE.
DEBUG	Debugging.
MDMT	Memory Dump to Magnetic Tape.
MDPRS	Memory Dump to Printer - SICE.
TPPRT	Tape Print - SICE.
TYDMP	Memory Dump to I/O Typewriter.

DKPRT

The Disc Print – SICE (DKPRT) program selectively prints the contents of a 506 disc pack. The disc pack is mounted on a 8564 disc drive attached to a 1600 Disc Control Electronics (DCE).

DKPRT is loaded by one of the 1600 loaders. All input/output is accomplished through the Series 1600 Input/Output Processing System (IOPS).

The disc print program processes fixed-sector or variable-sector input records. Disc contents are displayed in hexidecimal form with graphic equivalents on a 8242 or 8243 Printer attached to a Standard Interface Control Electronics (SICE).

Depending upon the option specified at the time of program generation, parameters specifying the disc extent to be printed may be entered through the 1600 Programmer/Maintenance Console or through a 1600 Console Typewriter attached to a 1600 Console Typewriter Electronics (CTCE).

Debug

The 1600 System Debugging Package (DEBUG) is a software diagnostic routine that can be incorporated in a user program through facilities available within the 1600 Input/Output Processing System (IOPS). DEBUG facilitates on-line program checkout and debugging. It enables the operating program to dynamically dump the contents of memory and selected registers on the 1600 Console Typewriter Keyboard Printer. It also enables the operator to display and/or change the contents of memory and/or selected registers. All communication between the operator and the DEBUG PACKAGE is accomplished through the 1600 Console Typewriter.

MDMT

The 1600 Memory Dump to Magnetic Tape (MDMT) is a freestanding, segmented routine that provides the ability to dump a specified portion of memory to a nine-level magnetic tape in a format acceptable to the RCA Series TOS Tape Edit (TPEDIT) routine as described in the TOS Utility Routines Manual.

The only data required as input to the Memory Dump is the ending dump address as described in Operation Procedures.

MDPRS

The Memory Dump to Printer – SICE (MDPRS) is a freestanding, two-load program that provides the ability to dump a portion of 1600 Memory to a 8242 or 8243 Printer through the 1600 System Standard Interface Control Electronics (SICE). MDPRS is written as a macro so that each user can tailor his memory dump to the options that he requires. MDPRS is assembled from the 1600 System Macro library, using the 1600 System Macro Assembler.

TPPRT

The 1600 System Tape Print – SICE (TPPRT) is a diagnostic program that prints the contents of 1600-System-compatible magnetic tape under selectable options. Tapes must be input through an 8432-1 Magnetic Tape Unit attached to an MT-9 CE.

TPPRT must be loaded by one of the 1600 loaders. All input/output is accomplished through the 1600 Input/Output Processing System (IOPS).

Optionally, the Tape Print routine processes fixed-length or variable-length input records. Tape contents are displayed in hexadecimal form with graphic equivalents or in predicted form. Output is printed on an 8242 or 8243 Printer attached to a Standard Interface Control Electronics (SICE).

TYDMP

The Memory Dump to I/O Typewriter (TYDMP) is a debugging and testing aid that provides a full or partial listing of memory. It is a self-loading 1600 program that provides facilities for displaying the contents of 1600 memory on the Console Typewriter.

APPENDIX A

1600 SYSTEM – SPECIAL FUNCTIONS

BA

ASSEMBLY MNEMONIC	07	06
IOTM	1	1
IOFM	1	0
WTM	0	1
RMT	1	1
** RMC	1	0
RMA	1	1
RMAC	1	1
RMS	1	0
RMSC	1	0
MPSR	0	1
SRST	0	1
TRR	0	1
** CMPR	1	0
ABR	1	1
ABRC	1	1
SBR	1	0
SBRC	1	0
ANDR	1	0
XORR	1	1
ORR	1	1
CSPR	0	1
CSTR	0	1
BIT	0	0
SFT	0	0
TAB	0	0
IOB	0	1
DAB	0	1
IDR	0	0
HALT	0	0

(CSPR) SPEC. REG.	(BITOP) BIT
	2^0
	2^1
BOUT 2	2^2
BOUT 1	2^3
DAD	2^4
W	2^5
X	2^6
	2^7

FIELD
UE EXCEPT $(1101)_2$

IOTBR
BIN0=1
BIN1=1
BIN2=1
BIN3=1
BIN4=1
BIN5=1
BIN6=1
BIN7=1
ANY BIN=1
HSB=1

**DOES NOT MODIFY EITHER OPERAND IN STD REG OR MEMORY

(10) REGISTER SET FOR SRST

SF EFFECT				
16	15	X1	R1 (DEST)	R2 (DEST)
0	0	0	A → H	A → H
0	1	0	A → H	I → P
1	0	0	I → P	A → H
1	1	0	I → P	I → P
0	0	1	I → P	I → P
0	1	1	I → P	A → H
1	0	1	A → H	I → P
1	1	1	A → H	A → H

(11) SHIFT

02	01	00	
0	–	–	Shift Left
1	–	–	Shift Right
–	0	–	Shift in Zero
–	1	–	Shift in From W0
–	–	0	Shift Out is Lost
–	–	1	Shift Out Into W0 & W4

(12) SF EFFECT

16	15	BIT OP
0	0	NO OP
0	1	TEST BIT
1	0	RESET BIT
1	1	SET BIT

(13) BIN ONLY–0=NO STROBE 1=STROBE 1

(14) BOUT ONLY–0=STROBE 2 1=STROBE 1

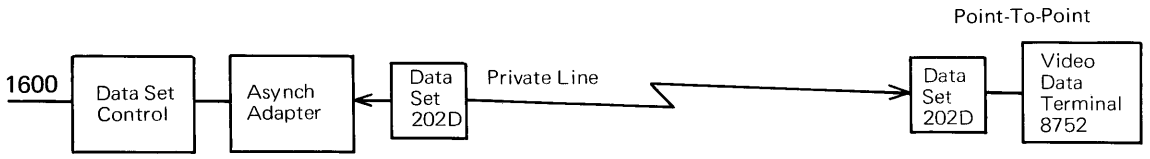
HEX	07	0
0	0	
	0	
1	0	
	0	
2	0	
	0	
3	0	
	0	
4	0	
	0	
5	0	
	0	
6	0	
	0	
7	0	
	0	
8	1	
	1	
9	1	
	1	
A	1	
	1	
B	1	
	1	
C	1	
	1	
D	1	
	1	
E	1	
	1	
F	1	
	1	

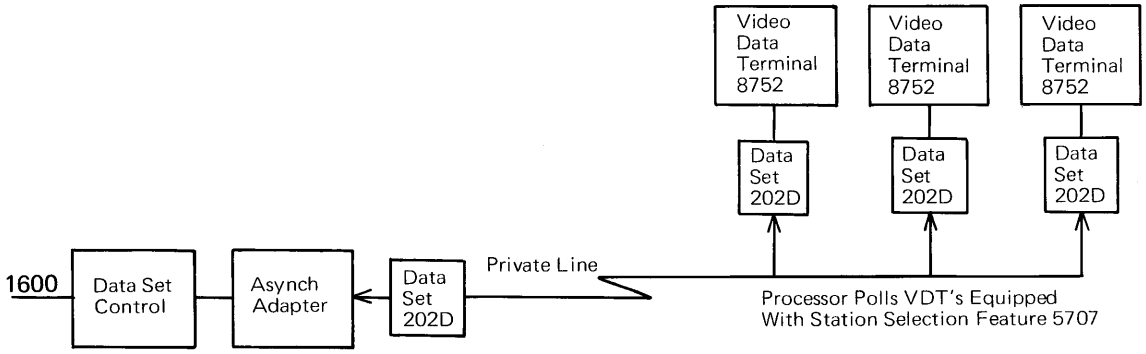
REGISTER DESIGNATION

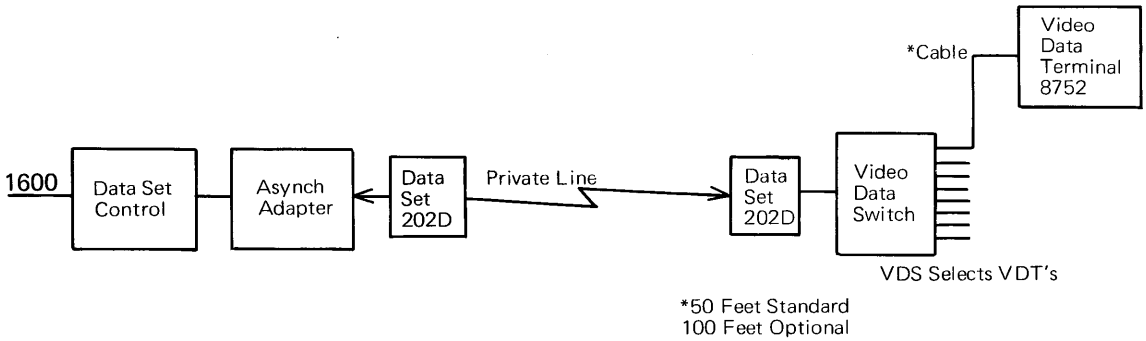
A1	
B1	
C1	
D1	
E1	
F1	
G1	
H1	BASIC INSTR. CTR 1
I1	
J1	
K1	
L1	
M1	
N1	HSIO MEM. ADDRESS
O1	HSIO BYTE COUNTER
P1	BASIC INSTR. CTR 2

APPENDIX B

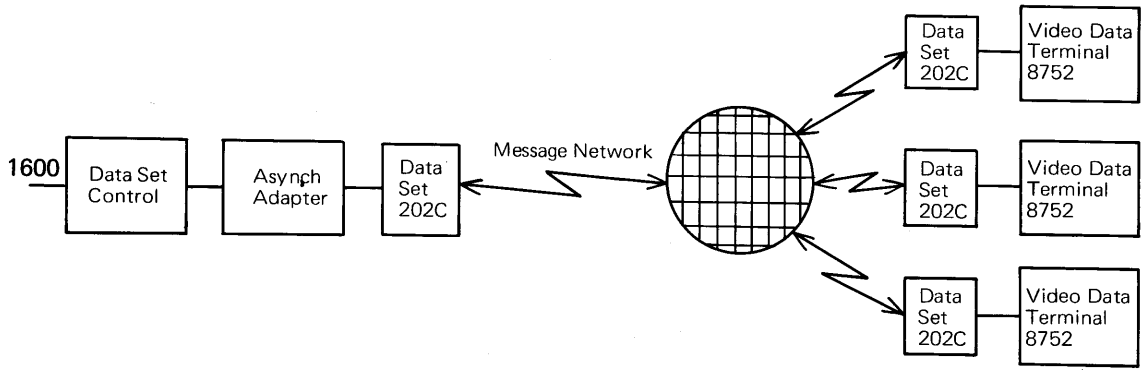
EXAMPLES OF VIDEO CONFIGURATIONS

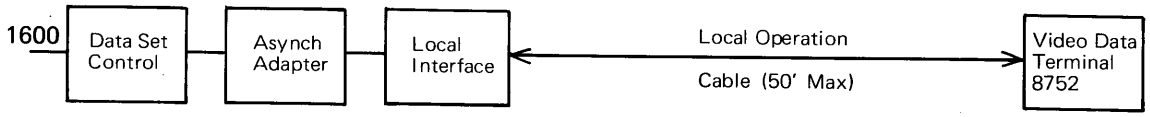


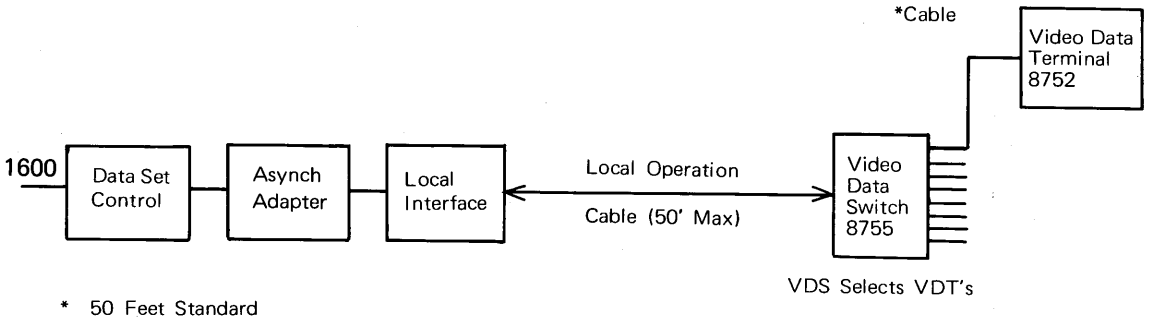




EXAMPLES OF VIDEO CONFIGURATIONS (Cont'd)

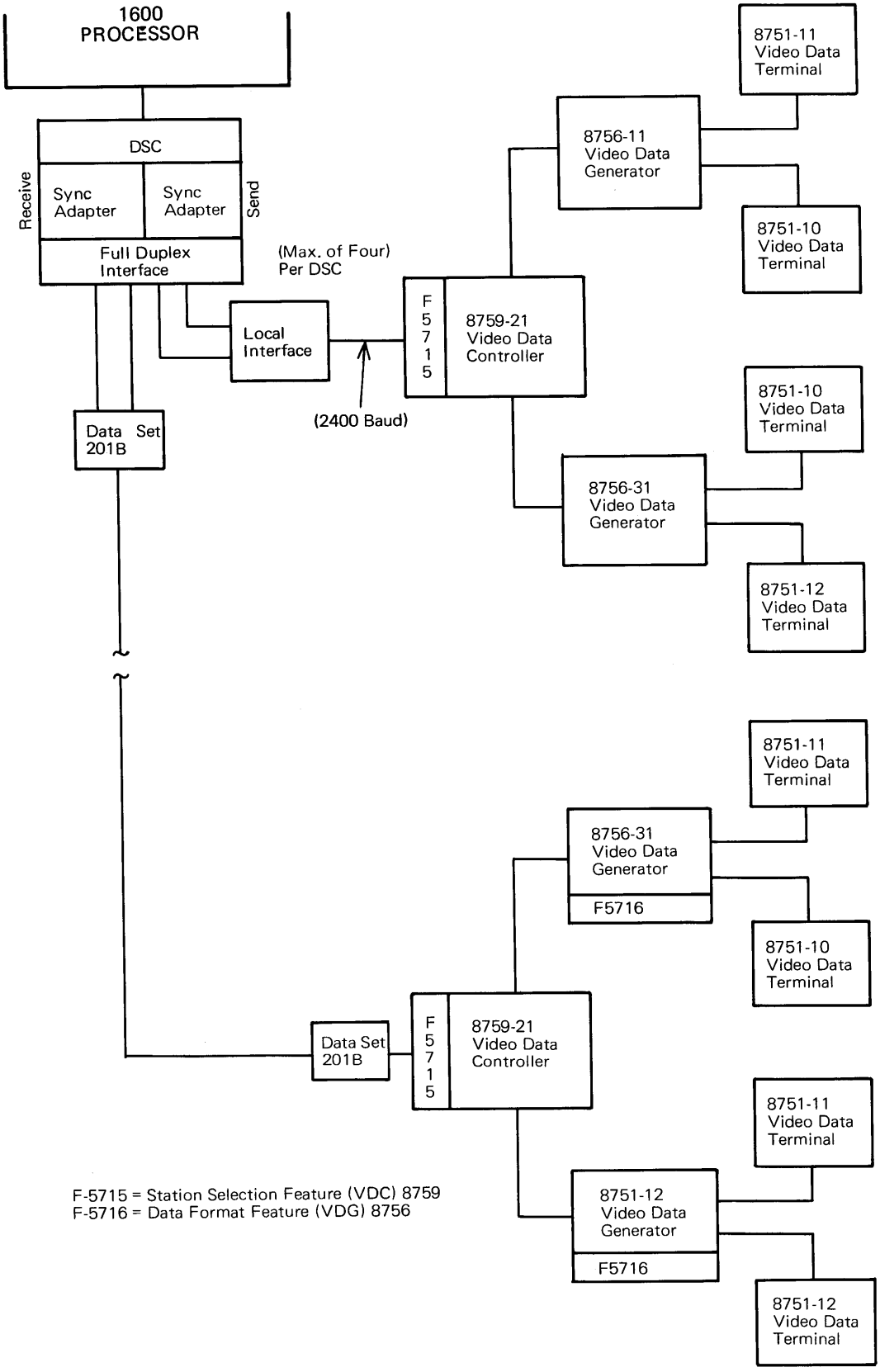






* 50 Feet Standard
100 Feet Optional

EXAMPLES OF VIDEO CONFIGURATIONS (Cont'd)



APPENDIX C

STANDARD DADS

Device Type	DAD Assignments		Device Type	Dad Assignments	
High Speed Ser. Req.	00000000	(00)	PTP Punch	011110XX	(78)
Reserved for Test Prog.	00000001	(01)	Spare	011111XX	(7C)
Class 1 Interrupt Ident.	00000010	(02)	Spare	100000XX	(80)
Class 2 Interrupt Iden.	00000011	(03)	Video Comp	100001XX	(84)
*Drum #1	000001XX	(04)	Spare	100010XX	(88)
*Drum #2	000010XX	(08)	Spare	100011XX	(8C)
*Data Exchange Control	000011XX	(0C)	AMA Paper Tape Control #1	100100XX	(90)
*Reserved	000100XX	(10)	AMA Paper Tape Control #2	100101XX	(94)
*Console Typewriter Control	000101XX	(14)	AMA Magnetic Tape Control #1	100110XX	(98)
*Magnetic Tape Control #1	000110XX	(18)	AMA Magnetic Tape Control #2	100111XX	(9C)
*Magnetic Tape Control #2	000111XX	(1C)	Telegraph Line Control #1	101000XX	(A0)
*Card Rd #	001000XX	(20)	Telegraph Line Control #2	101001XX	(A4)
*Card Rd #2	001001XX	(24)	Telegraph Line Control #3	101010XX	(A8)
*PTP Tape RDR	001010XX	(28)	Telegraph Line Control #4	101011XX	(AC)
*Reserved	001011XX	(2C)	Telegraph Line Control #5	101100XX	(B0)
*Reserved	001100XX	(30)	Telegraph Line Control #6	101101XX	(B4)
*Disc Control #1	001101XX	(34)	Telegraph Line Control #7	101110XX	(B8)
*Disc Control #2	001110XX	(39)	Telegraph Line Control #8	101111XX	(BC)
*Reserved	001111XX	(3C)	Data Set Control #1	110000XX	(C0)
			Data Set Control #2	110001XX	(C4)
Time Control	010000XX	(40)	Data Set Control #3	110010XX	(C8)
Control Panel	010001XX	(44)	Data Set Control #4	110011XX	(CC)
Printer #1	010010XX	(48)	Autodin Line Control	110100XX	(D0)
Printer #2	010011XX	(4C)	Autodin Line Control	110101XX	(D4)
Standard Interface Control #1	010100XX	(50)	Data Set Line Control #1	110110XX	(D8)
Standard Interface Control #2	010101XX	(54)	Data Set Line Control #2	110111XX	(DC)
Standard Interface Control #3	010110XX	(58)	Data Set Line Control #3	111000XX	(E0)
Card Punch	010111XX	(5C)	Data Set Line Control #4	111001XX	(E4)
Spare	011000XX	(60)	Spare	111010XX	(E8)
Spare (Reserved for Future Expansion)	011001XX	(64)	Spare	111011XX	(EC)
Spare (Reserved for Future Expansion)	011010XX	(68)	Spare	111100XX	(F0)
Spare (Reserved for Future Expansion)	011011XX	(6C)	Spare	111101XX	(F4)
Spare (Reserved for Future Expansion)	011100XX	(70)	Spare	111110XX	(F8)
Spare (Reserved for Future Expansion)	011101XX	(74)	Reserved for Diagnostics	11111100	(FC)
				11111101	(FD)
				11111110	(FE)
				11111111	(FF)

*Load Devices

Note:

Users of special purpose CE's should exercise care so that selected DADS do not conflict with above system standards

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Date December 1970

RCA Computer Systems

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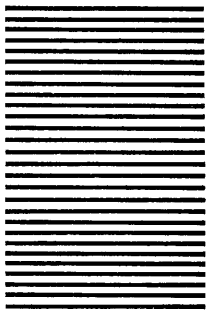

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