703 IC SYSTEMS COMPUTER

REFERENCE AND INTERFACE MANUAL

RAYTHEON COMPUTER • 2700 SO. FAIRVIEW ST., SANTA ANA, CALIFORNIA 92704 (714) 546-7160 TWX 910-595-1570

RAYTHEON

NOTICE

The contents of this manual are subject to change without notice.

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Section 1

GENERAL DESCRIPTION

1-1 GENERAL

The Raytheon 703 Computer is a general-purpose computer designed as the control element in data acquisition processing and control systems. The 703 features low cost, integrated circuits, and the reliability inherent to third generation refinements. The basic characteristics of the 703 are:

- 16-bit word length
- Two's complement arithmetic
- Direct and indexed addressing
- Memory expandable from 4096 to 32, 768 words
- 1. 75 μ sec cycle time
- Byte and word addressing
- Byte manipulation instructions
- High-speed Direct Memory Access I/O channels
- Direct Input/Output to the Central Processor Unit permitting program word transfer
- Interrupt system

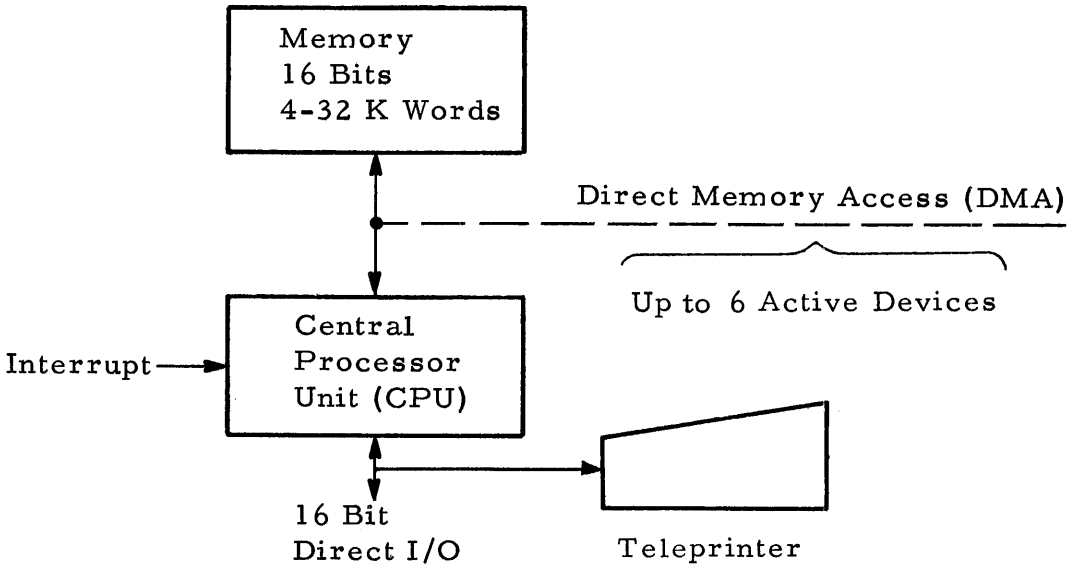


Figure 1-1. Raytheon Model 703 Computer

The Raytheon 703 uses a parallel structured central processor as shown in figure 1-2. The following operational registers are available to the programmer:

ACR: The 16-bit accumulator used as a full-word and byte accumulator.

PCR: The 15-bit program counter

IXR: The 16-bit index register

EXR: The 5-bit memory address extension register

The following registers are not available to the programmer:

INR: The 8-bit instruction register that holds the current instruction code

MAR: The 16-bit memory address register that contains the current operand address

MBR: The 16-bit memory buffer register used to hold operand words transmitted to and from memory

The Raytheon 703 Memory consists of one or more memory modules of 4096 words providing a capacity from 4096 to 32, 768 words. The word size is 16 bits. Basic memory cycle time is 1. 75 μ sec.

Select and Complement (S/C) Gates A and B gate the various registers into the arithmetic circuits at the proper time. These two gates also provide two's complementation for the accumulators. The Adder is comprised of the Carry, and Logic and Sum Generators which perform the arithmetic and logical functions in the CPU.

The CPU Control function coordinates the operation of the other units in the Central Processor Unit. The status of the Overflow, High, Low, and Global functions is retained in Status Storage.

Receivers and Drivers of the Direct Input/Output pass data directly to and from the Accumulator (ACR). These circuits are discussed in detail in Section 4.

1-2 WORD FORMATS

Note that in the following description of word formats, bit positions within a word are numbered from left to right, bit 0 being the most significant and bit 15 the least significant.

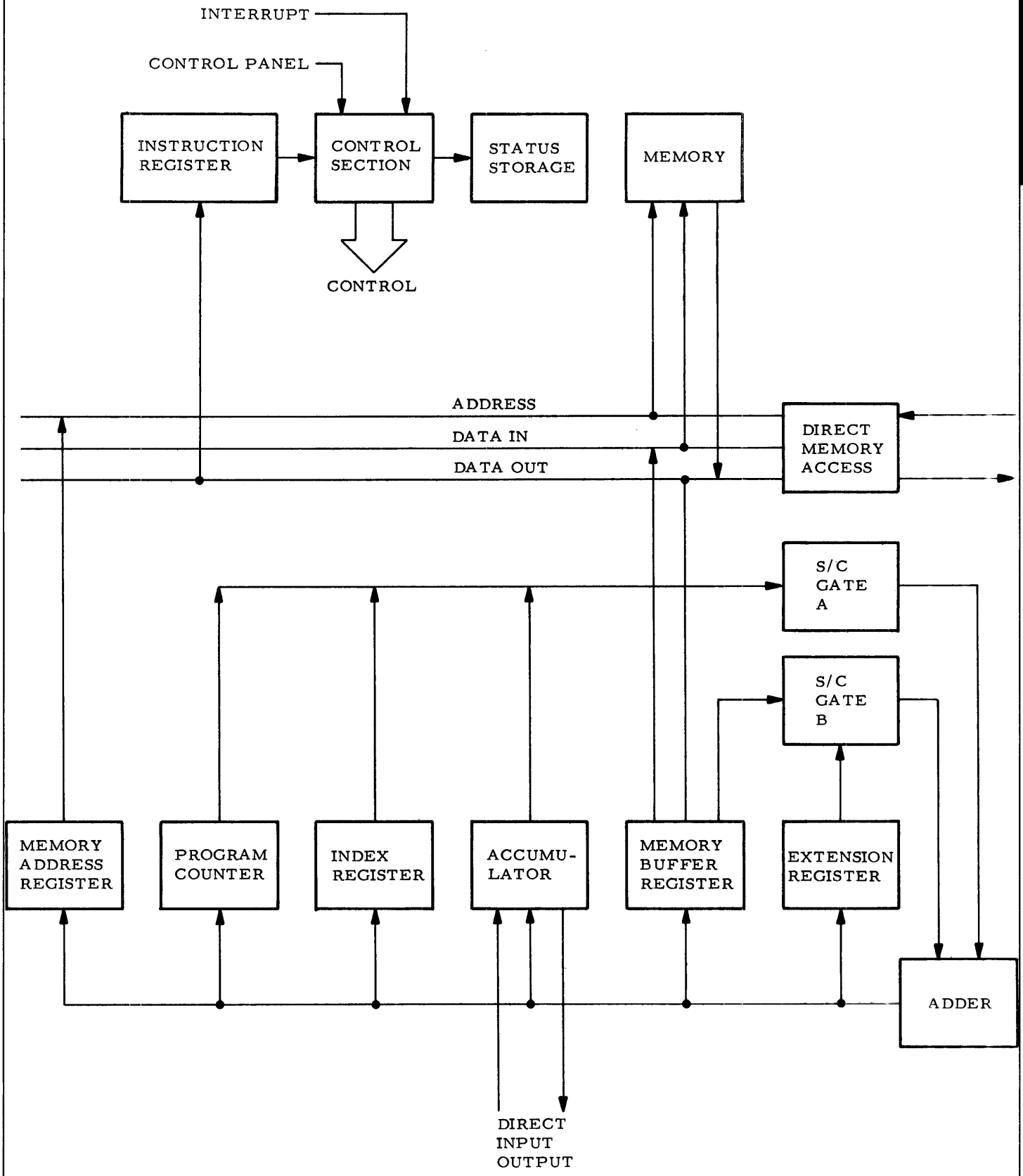
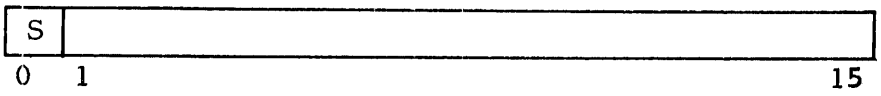


Figure 1-2. Central Processor Unit, Block Diagram

1-2.1 DATA WORDS

Single precision numbers have the following format:

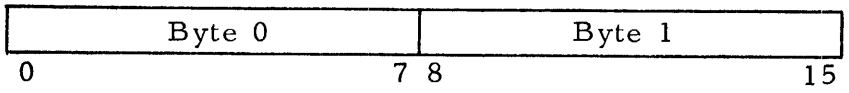


Single precision data are held in a 16-bit two's complement numbers format. Bit-0, the sign bit, is a zero for positive numbers and a one for negative numbers. The number range is defined:

FRACTIONAL: $-1 \leq N < +1$

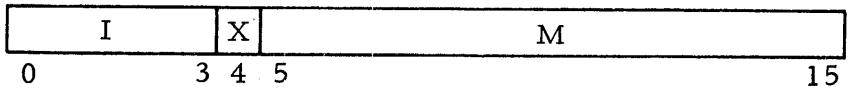
INTEGER: $-2^{15} \leq N < +2^{15} - 1$

Two 8-bit bytes are contained in a word in the following format:



1-2.2 INSTRUCTION WORDS

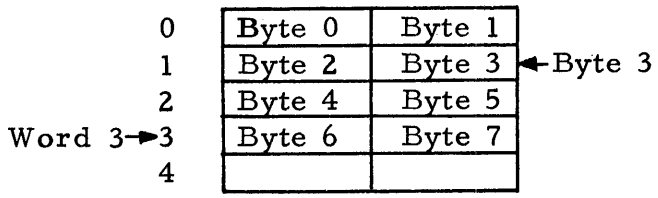
The instruction word format is:



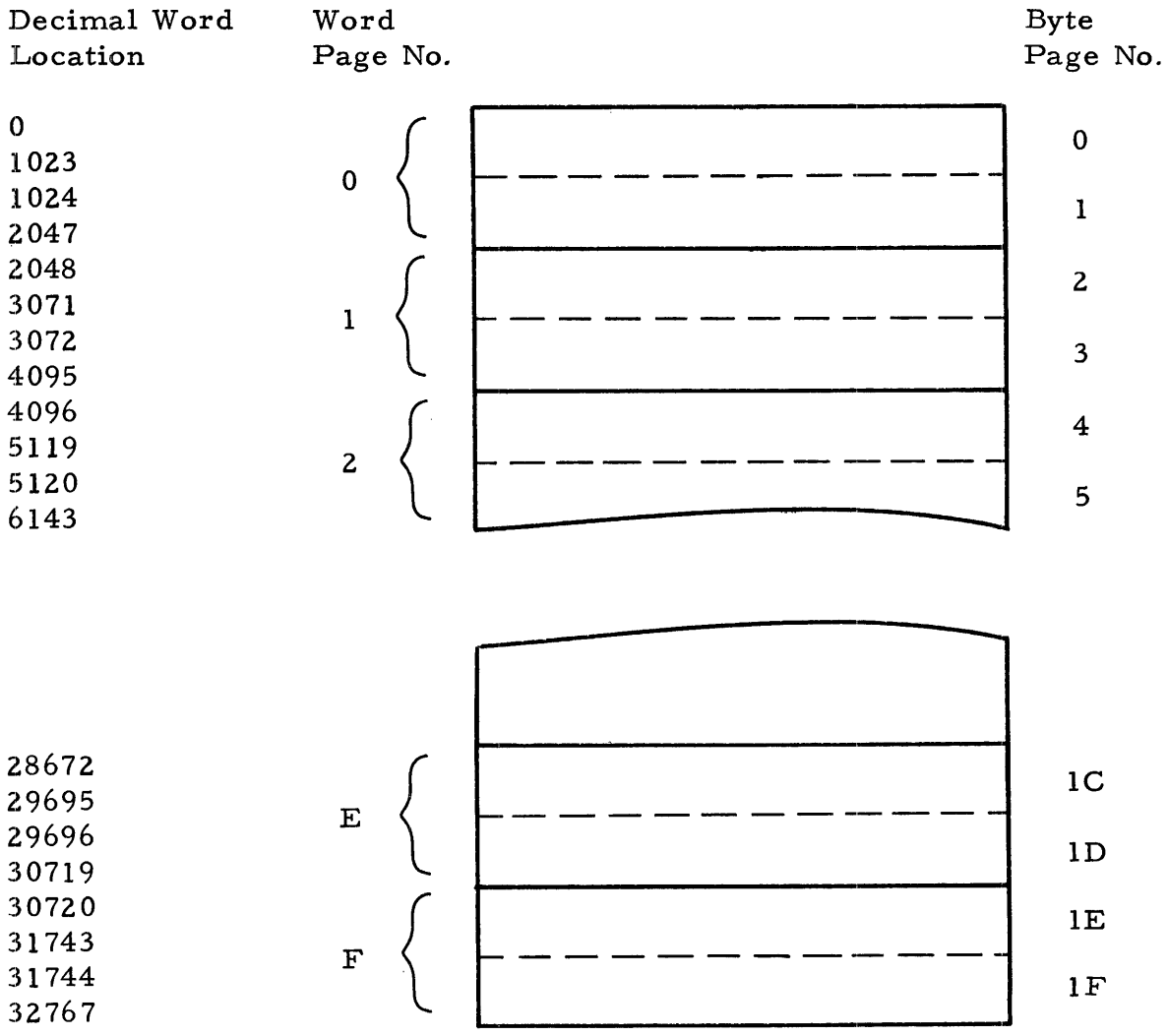
Bits 0-3 designate the instruction code (I). Bit 4 is the index flag (X). Bits 5-15 are the memory address (M). Certain extended instructions that do not require memory reference use the M field to further specify instruction function. The format for each instruction is defined in Section 2.

1-3 ADDRESSING

Addressing in the Raytheon 703 is according to instruction type. The effective address, i, of a word instruction designates the i^{th} word of memory, while the i^{th} byte is designated for a byte instruction. For example, the execution of a byte instruction with address 3 specifies byte address 3 as shown below. The execution of a word instruction with address 3 specifies word address 3 as shown below.



The 32, 768 memory words are accessed by a memory paging technique. The memory is divided both into word pages containing 2, 048 words and byte pages of 2, 048 bytes. These pages are designated by either a word or byte page number as shown below:



Since there are two byte pages in each word page, dividing a byte page number by two defines the word page containing the associated byte page. The remainder of this division indicates the first or second byte page within the word page.

The page used as a base address for executing a memory reference instruction is specified by an extension register, EXR. The contents of this 5-bit register (a byte page number) are concatenated to the 11-bit address, M, to form a 16-bit byte address when a byte instruction is executed. The most significant four bits of the contents of EXR are used to form a 15-bit word address for word instructions. In this manner the contents of EXR designate a word page, and one of the two byte pages within that word page.

The contents of EXR may be set to any memory page by executing the SML (select memory lower) or SMU (select memory upper) instructions. After executing the memory reference instruction, the contents of EXR are replaced by bits 1 thru 5 of the program counter. Base addresses are thus automatically contained within the local page (the page containing the instruction to be executed), unless an SML or SMU instruction designates another page for the next memory reference instruction.

The Raytheon 703 uses three forms of addressing -- direct, indexed local, and indexed global.

1-3.1 DIRECT ADDRESSING

Bit 4 of the instruction word specifies either direct or indexed addressing. If bit 4 is a zero, direct addressing is specified. The base address formed by the concatenation of the contents of EXR to the address field of the instruction (M) is used directly as the effective address.

1-3.2 INDEXED ADDRESSING

A one in bit 4 of the instruction word specifies indexing. Two modes of indexing are provided, local and global.

In the local mode, a base address is formed using the extension register. The contents of the index register (IXR) are added to this base address to form the effective address.

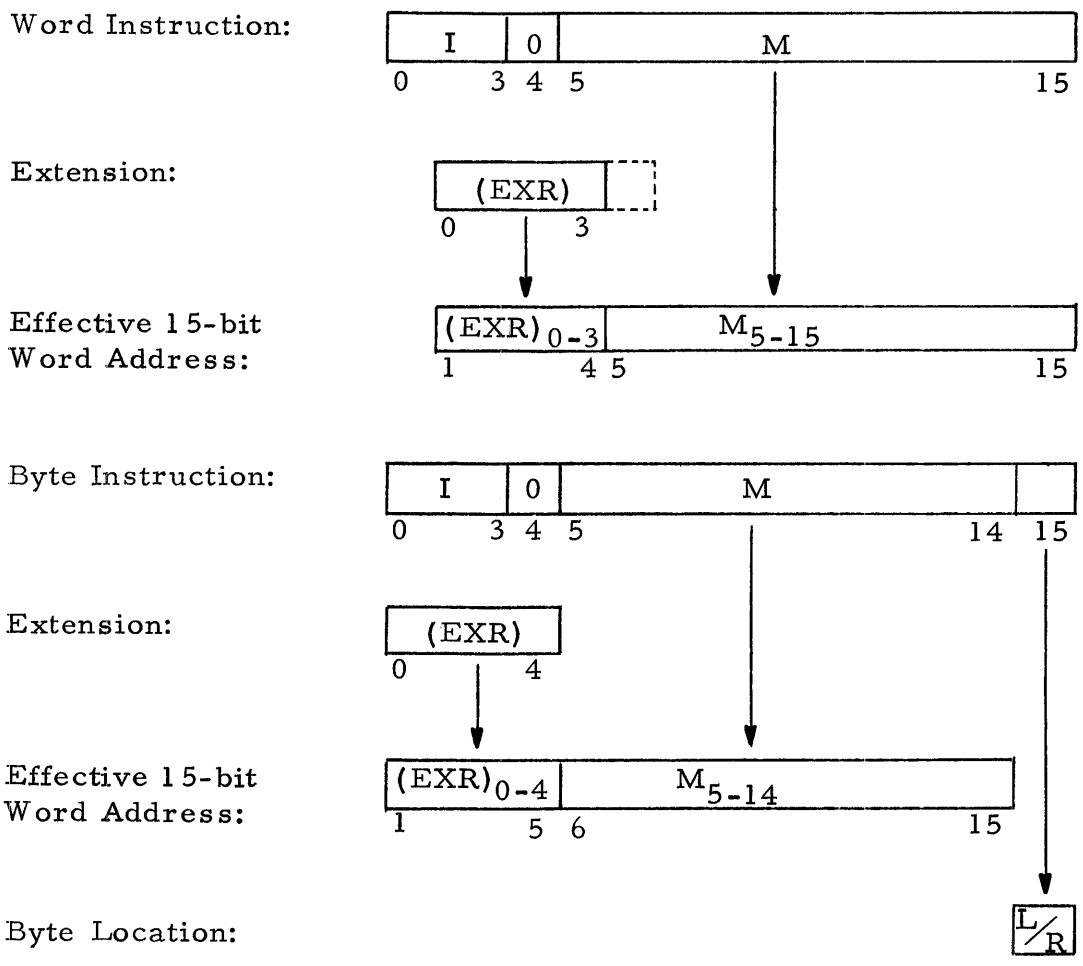
In the global mode, zeros are substituted for the contents of the extension register when the base address is formed. This base address is added to the contents of the index register to form the effective address.

The machine may be set to either the local or global mode using SLM or SGM instructions. Execution of a JSX instruction automatically selects the global mode prior to the jump.

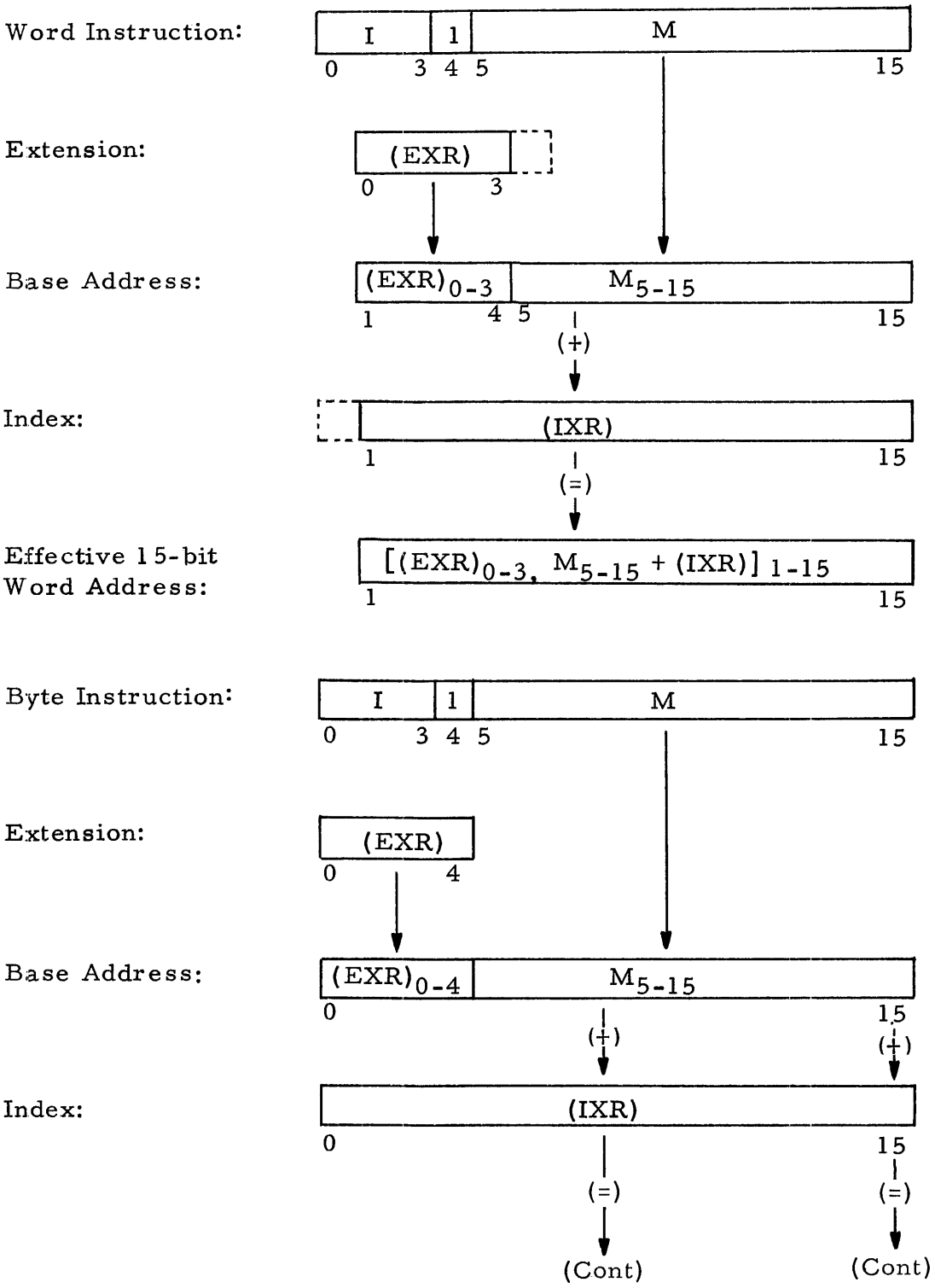
1-3.3 ADDRESSING SUMMARY

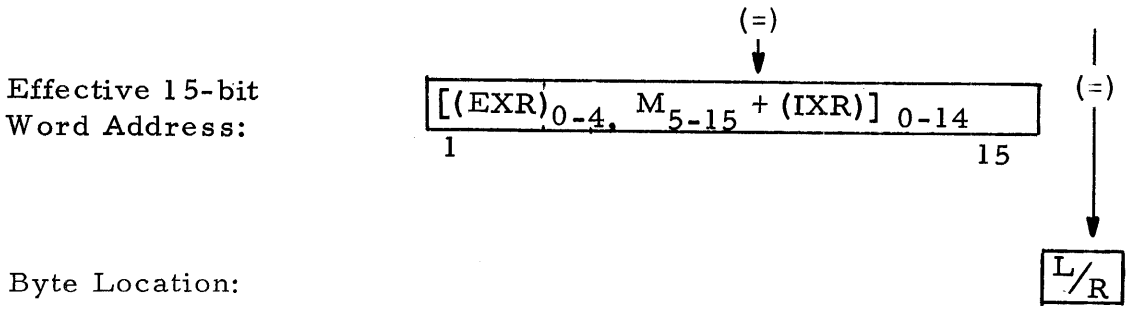
The effect of the various modes of address modification are illustrated below. Note that the L/R adjacent to the Byte Locations indicates left or right byte.

1-3.3.1 Direct

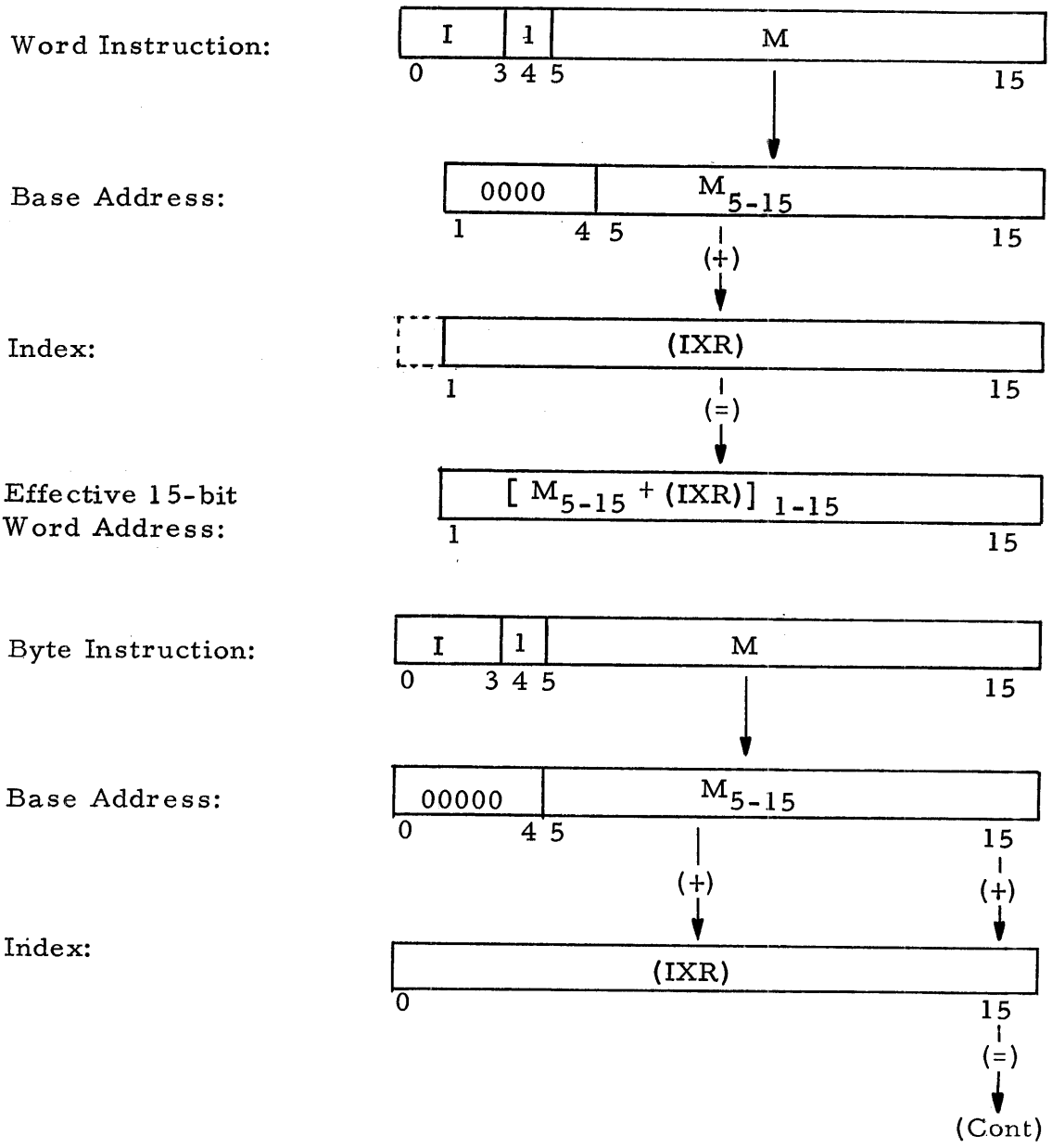


1-3.3.2 Indexed Local

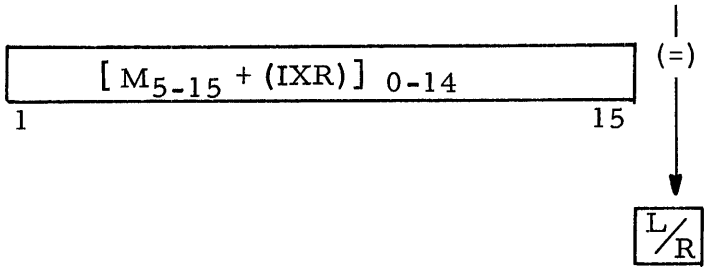




1-3.3.3 Indexed Global



Effective 15-bit Word Address:



Byte Location:

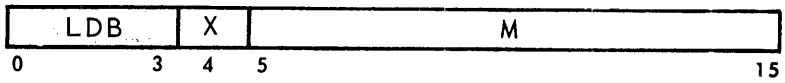
Section 2.
INSTRUCTIONS

2-1 GENERAL

This section defines the function of each instruction and its effect on the various registers and the memory of the machine. Unless a register or the memory is specifically mentioned, it is unaffected by the instruction. The mnemonic, format, and timing in terms of memory cycles and equations are also defined for each instruction. The equation terms and symbols are defined in table 2-1.

2-2 LOAD/STORE

LDB Load Byte

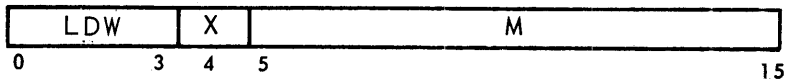


T: 2

$(ACR)_{8-15} \longleftarrow (M_B)$

The contents of the memory byte location specified by the effective address replace the contents of bits 8-15 of the accumulator. The contents of memory remain unchanged. Execution of this instruction copies the local page address to the extension register.

LDW Load Word

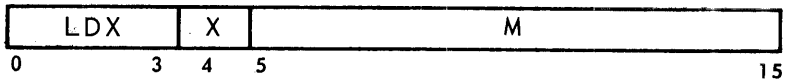


T: 2

$(ACR) \longleftarrow (M_W)$

The contents of the memory word location specified by the effective address replace the contents of the accumulator. The contents of memory remain unchanged. Execution of this instruction copies the local page address to the extension register.

LDX Load Index



T: 2

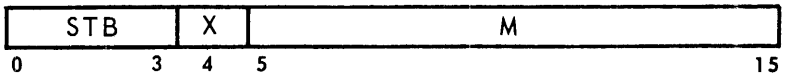
$(IXR) \longleftarrow (M_W)$

The contents of the memory word location specified by the effective address replace the contents of the index register. The contents of memory remain unchanged. Execution of this instruction copies the local page address to the extension register.

Table 2-1. Definition of Instruction Equation Terms and Symbols

Terms and Symbols	Definitions
(ACR)	The contents of the accumulator
(IXR)	The contents of the index register
(M_W)	The contents of the memory word location M
(PCR)	The contents of the program counter
(M_B)	The contents of the memory byte location M
(EXR)	The contents of the extension register
M	The memory address field of the instruction
$(X)_{n-m}$	The n^{th} through m^{th} bits of the contents of the register or memory location X
A←B	A is replaced by B
+	Arithmetic sum
-	Arithmetic difference
∧	Logical AND
∨	Logical OR
⊕	Logical exclusive OR
$(\overline{X})$	Logical inversion of the contents of X
(ADFNEG)	The contents of the "negative" comparison flip flop
(ADFEQL)	The contents of the "equals" comparison flip flop
[Expression]	The logical value of the expression
(ADFOVF)	The contents of the overflow flip flop
(CCFGLB)	The contents of the global flip flop

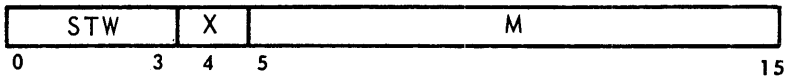
STB Store Byte



T: 3
$(M_B) \longleftarrow (ACR)_{8-15}$

The contents of bits 8-15 of the accumulator replace the contents of the memory byte location specified by the effective address. The contents of the accumulator remain unchanged. Execution of this instruction copies the local page address to the extension register.

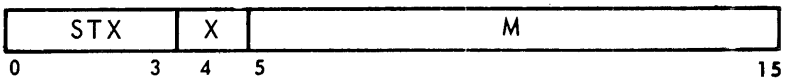
STW Store Word



T: 2
$(M_W) \longleftarrow (ACR)$

The contents of the accumulator replace the contents of the memory word location specified by the effective address. The contents of the accumulator remain unchanged. Execution of this instruction copies the local page address to the extension register.

STX Store Index

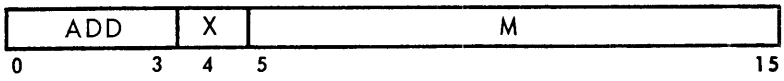


T: 2
$(M_W) \longleftarrow (IXR)$

The contents of the index register replace the contents of the memory word location specified by the effective address. The contents of the index register remain unchanged. Execution of this instruction copies the local page address to the extension register.

2-3 ARITHMETIC

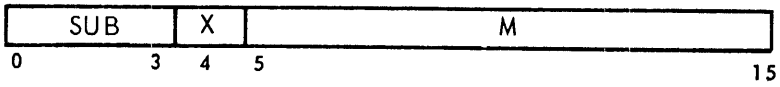
ADD Add



T: 2
$(ACR) \longleftarrow (ACR) + (M_W)$

The arithmetic sum of the original contents of the accumulator plus the contents of the memory word location specified by the effective address replaces the contents of the accumulator. The contents of memory remain unchanged. Execution of this instruction copies the local page address to the extension register. The overflow flip flop is set if the result of an addition is less than -2^{15} or greater than $2^{15} - 1$.

SUB Subtract

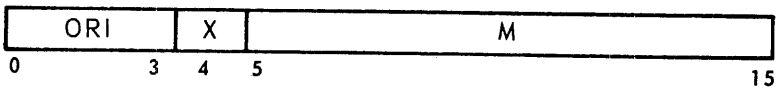


T: 2
(ACR) ⟵ (ACR) - (M_W)

The arithmetic difference between the original contents of the accumulator minus the contents of the memory word location specified by the effective address replaces the contents of the accumulator. The contents of memory remain unchanged. Execution of this instruction copies the local page address to the extension register. The overflow flip flop is set if the result of a subtraction is less than -2^{15} or greater than $2^{15} - 1$.

2-4 LOGICAL

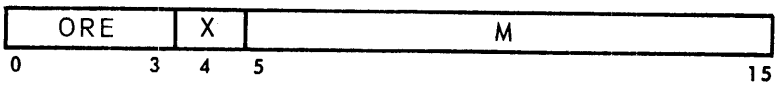
ORI Inclusive OR



T: 2
(ACR) ⟵ (ACR) ∨ (M_W)

The logical sum of the contents of the accumulator and the contents of memory word location specified by the effective address replaces the contents of the accumulator. The contents of memory remain unchanged. Execution of this instruction copies the local page address to the extension register.

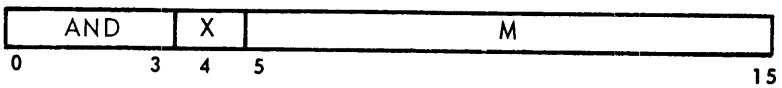
ORE Exclusive OR



T: 2
(ACR) ⟵ (ACR)⊕(M_W)

The logical Exclusive OR between the contents of the accumulator and the contents of the memory word location specified by the effective address replaces the contents of the accumulator. The contents of memory remain unchanged. Execution of this instruction copies the local page address to the extension register.

AND Logical AND

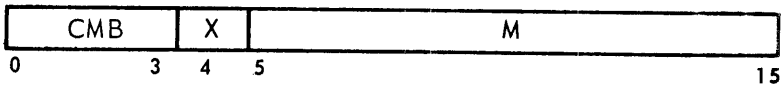


T: 2
(ACR) ⟵ (ACR) ∧ (M_W)

The logical product of the original contents of the accumulator and the contents of the memory word location specified by the effective address replaces the contents of the accumulator. The contents of memory remain unchanged. Execution of this instruction copies the local page address to the extension register.

2-5 COMPARE

CMB Compare Byte



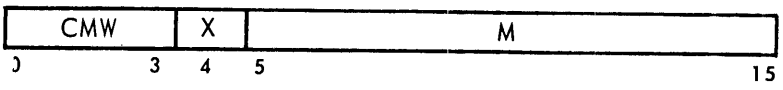
T: 2

$(ADFNEG) \leftarrow [(ACR)_{8-15} - (M_B) < 0]$

$(ADFEQL) \leftarrow [(ACR)_{8-15} - (M_B) = 0]$

The contents of the memory byte location specified by the effective address are compared to the contents of bits 8-15 of the accumulator. The result of the comparison is stored in a comparison register specifying whether the contents of bits 8-15 of the accumulator were less than, equal to, or greater than the contents of the memory byte position specified by the effective address. Neither the contents of the register or memory are affected. Execution of this instruction copies the local page address to the extension register. Bytes are treated as signed two's complement 8-bit numbers.

CMW Compare Word



T: 2

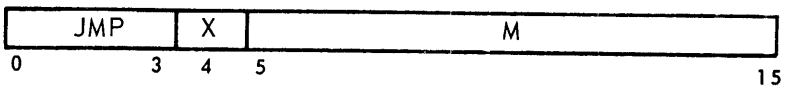
$(ADFNEG) \leftarrow [(ACR) - (M_W) < 0]$

$(ADFEQL) \leftarrow [(ACR) - (M_W) = 0]$

The contents of the memory word location specified by the effective address are compared to the contents of the accumulator. The result of the comparison is stored in the comparison register specifying whether the contents of the accumulator are less than, equal to, or greater than the contents of the memory location specified by the effective address. Neither the contents of the accumulator nor the contents of memory are affected. Execution of this instruction copies the local page address to the extension register. Words are treated as signed two's complement 16-bit numbers.

2-6 JUMPS

JMP Unconditional Jump

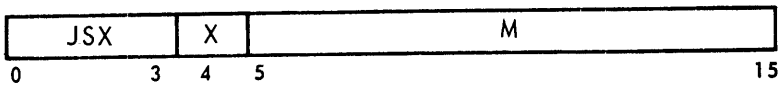


T: 1

$(PCR) \leftarrow M_W$

The effective word address replaces the contents of the program counter. Execution of this instruction copies the local page address to the extension register.

JSX Jump and Store Return In Index



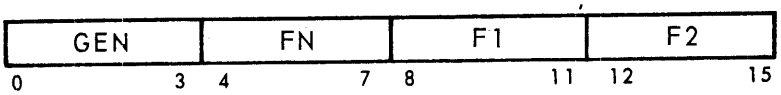
T: 2

(IXR) ← (PCR); (PCR) ← M_W

The contents of the index register are replaced by the contents of the program counter. The contents of the program counter are replaced by the effective word address. Execution of this instruction copies the local page address to the extension register. Execution of this instruction forces the computer into global addressing mode prior to the transfer.

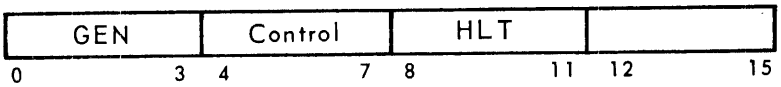
2-7 GENERICS

Generics are non-memory reference instructions which share a common instruction code. As shown in the format below, bits 4-7 (FN) are used to designate the major function or functional class of the instruction to be performed. Bits 8-11 (F1) may be used to designate a subclass of a basic generic instruction class.



2-7.1 CONTROL GENERICS

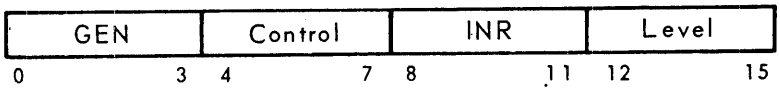
HLT Halt



T: 1

The central processing unit is placed in the idle state. To resume computation the run switch on the control panel must be activated.

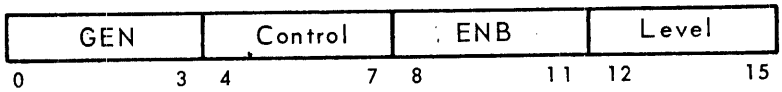
INR Interrupt Return



T: 3

The interrupting level must be specified in bits 12-15 of the instruction to effect a correct return. Memory word locations accessed by the execution of the INR instruction are relative to the specified interrupt level. The contents of the program counter and machine status (MS) are restored and the interrupt level is returned to the Idle state.

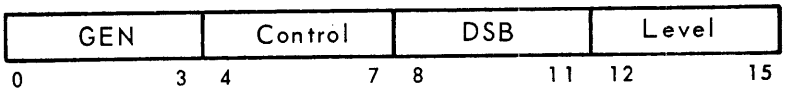
ENB Enable Interrupt



T: 1

The interrupt level specified is enabled, permitting it to respond to interrupts. Bits 12-15 of the instruction word specify which interrupt level is enabled.

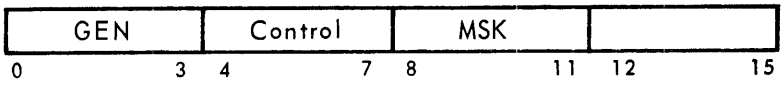
DSB Disable Interrupt



T: 1

The interrupt level specified is disabled, preventing any response to interrupts. Bits 12-15 of the instruction word specify which interrupt level is disabled.

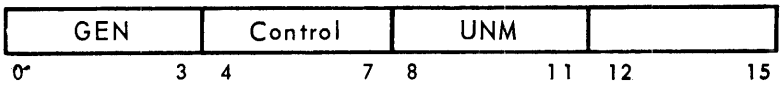
MSK Mask Interrupts



T: 1

The interrupt system is inhibited from processing any interrupts which may occur. The interrupt condition of each level will remain pending and will be processed when the inhibit condition is removed. An interrupt subroutine in process is not affected by execution of this instruction. Bits 12-15 are unused.

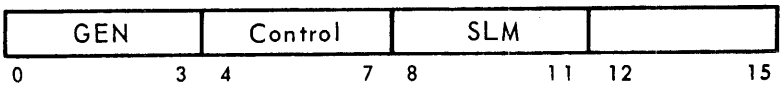
UNM Unmask Interrupts



T: 1

The interrupt system is unmasked to allow enabled interrupts to be serviced as required. Bits 12-15 are unused.

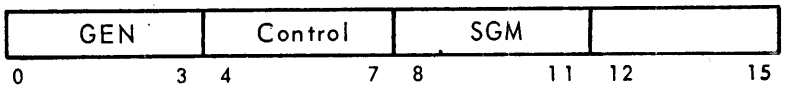
SLM Set Local Mode Addressing



T: 1
(CCFGLB) ← 0

The central processing unit is placed in the local addressing mode causing the contents of the extension register (EXR) to be used in forming the base address of index instructions.

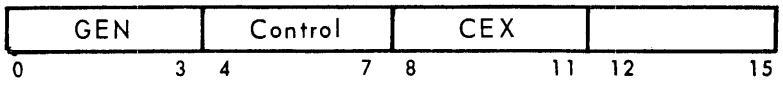
SGM Set Global Mode



T: 1
(CCFGLB) ← 1

The central processing unit is placed in the global addressing mode. The contents of the extension register (EXR) are not used in forming the base address of index instructions. The bit positions normally provided by the EXR are set to 0.

CEX Copy Extension to Index

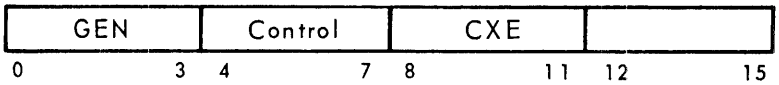


T: 1

$(IXR)_{0-4} \leftarrow (EXR)$

The contents of bits 0-4 of the index register are replaced by the contents of the extension register. The contents of the extension register and the contents of the remaining bits of the index register remain unchanged.

CXE Copy Index to Extension

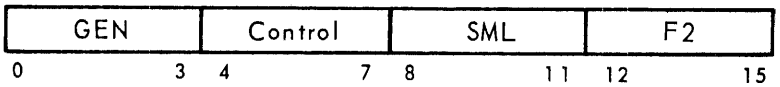


T: 1

$(EXR) \leftarrow (IXR)_{0-4}$

The contents of the extension register are replaced by the contents of bits 0-4 of the index register. The contents of the index register remain unchanged.

SML Select Memory Lower

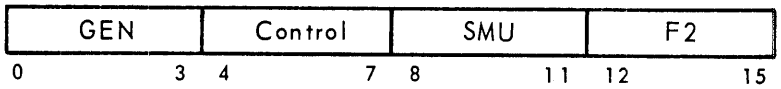


T: 1

$(EXR)_0 \leftarrow 0$; $(EXR)_{1-4} \leftarrow F_2$

The contents of bits 1 to 4 of the extension register are replaced by bits 12-15 (F2) of the instruction. Bit 0 of the extension register is set to zero.

SMU Select Memory Upper



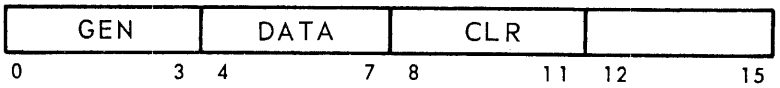
T: 1

$(EXR)_0 \leftarrow 1$; $(EXR)_{1-4} \leftarrow F_2$

The contents of bits 1 to 4 of the extension register are replaced by bits 12-15 (F2) of the instruction. Bit 0 of the extension register is set to one.

2-7.2 DATA GENERICS

CLR Clear Accumulator

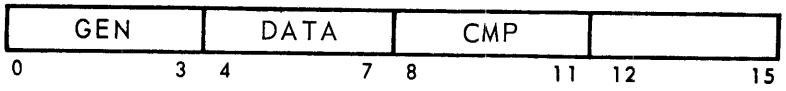


T: 1

$(ACR) \leftarrow 0$

The contents of the accumulator are replaced by 0.

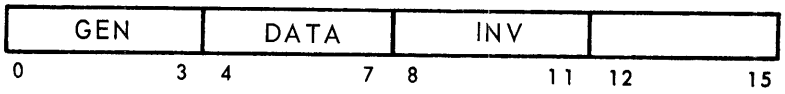
CMP Complement Accumulator



T: 1
(ACR) ⟵ - (ACR)

The contents of the accumulator are replaced by the two's complement of the contents of the accumulator. The overflow flip flop will be set if the number -2^{15} is complemented.

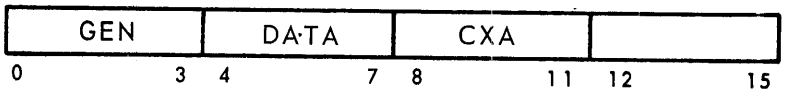
INV Invert Accumulator



T: 1
(ACR) ⟵ $(\overline{ACR})$

The contents of the accumulator are replaced by the one's complement of the contents of the accumulator.

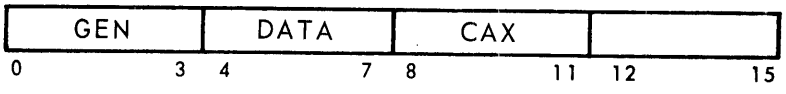
CXA Copy Index to Accumulator



T: 1
(ACR) ⟵ (IXR)

The contents of the accumulator are replaced by the contents of the index register. The contents of the index register are not affected.

CAX Copy Accumulator to Index

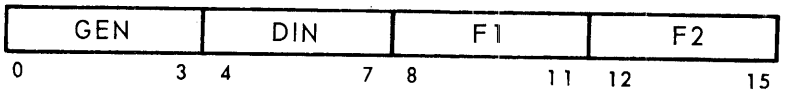


T: 1
(IXR) ⟵ (ACR)

The contents of the index register are replaced by the contents of the accumulator. The contents of the accumulator are not affected.

2-7.3 I/O GENERICS

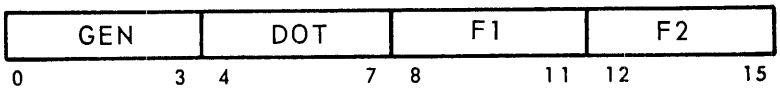
DIN Direct Input



T: 2
(ACR) ⟵ $(DIN)_{0-15}$

Bits 8-15 of the instruction (F1 and F2) are transferred to the DIO address bus and an input strobe is generated. At the trailing edge of the input strobe, the contents of the accumulator are replaced by the data applied to the DIO input data bus. Bits 8-11 (F1) of the instruction word designate the device selected for input and bits 12-15 (F2) of the instruction designate the selected function.

DOT Direct Output



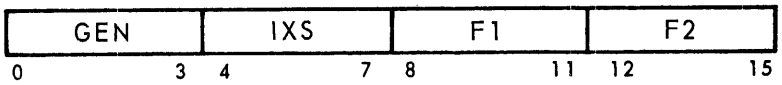
T: 2

$(DOT)_{0-15} \leftarrow (ACR)$

Bits 8-15 of the instruction (F1 and F2) are transferred to the DIO address bus, the contents of the accumulator are transferred to the DIO output data bus, and an output strobe is generated. The contents of the accumulator are not affected. Bits 8-11 (F1) of the instruction word designate the device selected for output and bits 12-15 of the instruction word (F2) designate the selected function.

2-7.4 LITERAL GENERICS

IXS Increment Index and Skip if ≥ 0

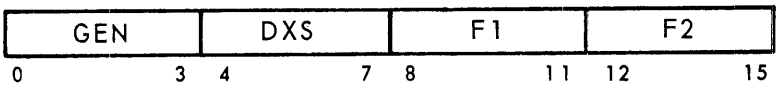


T: 2

$(IXR) \leftarrow (IXR) + M_{8-15}$; $(PCR) \leftarrow (PCR) + 1 + [(IXR) \geq 0]$

The algebraic sum of the contents of the index register plus the unsigned literal, bits 8-15 of the instruction word, replace the contents of the index register. If the sum is greater than or equal to zero the next instruction in sequence is skipped; otherwise, the next instruction in sequence is taken.

DXS Decrement Index and Skip if < 0

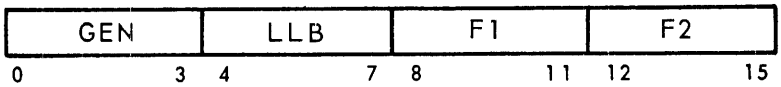


T: 2

$(IXR) \leftarrow (IXR) - M_{8-15}$; $(PCR) \leftarrow (PCR) + 1 + [(IXR) < 0]$

The algebraic difference between the contents of the index register and the unsigned literal, bits 8-15 of the instruction word replace the contents of the index register. If the contents of the index register are less than zero the next instruction in sequence is skipped; otherwise, the next instruction in sequence is taken.

LLB Load Literal Byte

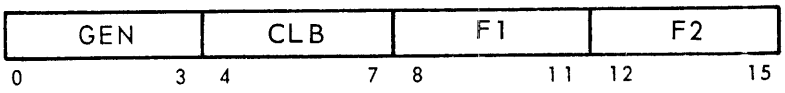


T: 1

$(ACR)_{8-15} \leftarrow M_{8-15}$

The contents of bits 8-15 of the accumulator are replaced by the literal, bits 8-15 of the instruction word. The contents of bits 0-7 of the accumulator are unaffected.

CLB Compare Literal Byte



T: 1

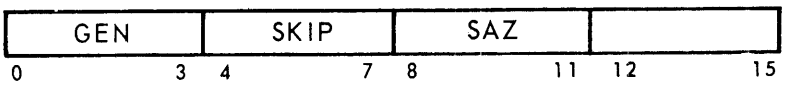
$(ADFNEG) \leftarrow [(ACR)_{8-15} - M_{8-15} < 0]$

$(ADFEQL) \leftarrow [(ACR)_{8-15} - M_{8-15} = 0]$

The contents of bits 8-15 of the accumulator are compared to the literal, bits 8-15 of the instruction word, and the result stored in the comparison register specifying whether the contents of bits 8-15 of the accumulator were less than, equal to, or greater than the literal. Both the literal and the contents of bits 8-15 of the accumulator are treated as 8-bit two's complement numbers for the purpose of this comparison.

2-7.5 SKIP GENERICS

SAZ Skip on Accumulator Zero

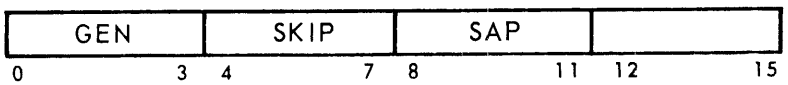


T: 1

$(PCR) \leftarrow (PCR) + 1 + [(ACR) = 0]$

If the contents of the accumulator are zero, the next instruction in sequence is skipped; otherwise, the next instruction in sequence is taken. The contents of the accumulator are not affected.

SAP Skip on Accumulator Plus

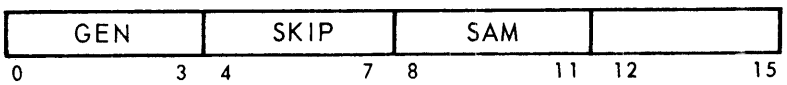


T: 1

$(PCR) \leftarrow (PCR) + 1 + [(ACR) \geq 0]$

If the contents of the accumulator are greater than or equal to zero, the next instruction in sequence is skipped; otherwise, the next instruction in sequence is taken. The contents of the accumulator are not affected.

SAM Skip on Accumulator Minus

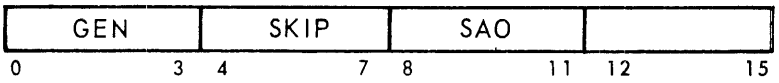


T: 1

$(PCR) \leftarrow (PCR) + 1 + [(ACR) < 0]$

If the contents of the accumulator are less than 0, the next instruction in sequence is skipped; otherwise, the next instruction in sequence is taken. The contents of the accumulator are not affected.

SAO Skip on Accumulator Odd

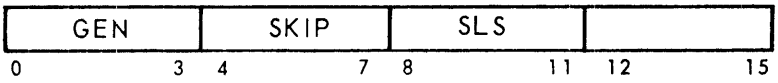


T: 1

$(PCR) \leftarrow (PCR) + 1 + [(ACR)_{15} = 1]$

If the contents of bit 15 of the accumulator is equal to 1, the next instruction in sequence is skipped; otherwise, the next instruction in sequence is taken.

SLS Skip on Compare Less

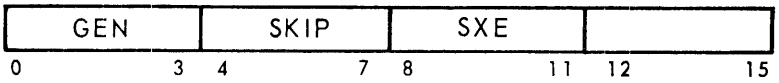


T: 1

$(PCR) \leftarrow (PCR) + 1 + [(ADFNEG) = 1]$

If the contents of the comparison storage register specify that the contents of the accumulator were less than the operand of the last previous compare instruction, the next instruction in sequence is skipped; otherwise, the next instruction in sequence is taken. The contents of the accumulator are not affected.

SXE Skip on Index Even

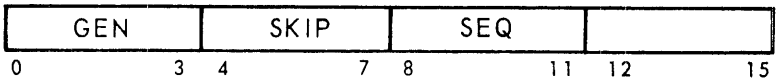


T: 1

$(PCR) \leftarrow (PCR) + 1 + [(IXR)_{15} = 0]$

If the contents of bit 15 of the index is equal to 0, the next instruction in sequence is skipped; otherwise, the next instruction in sequence is taken.

SEQ Skip on Compare Equal

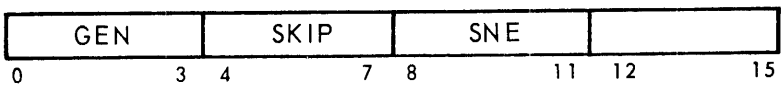


T: 1

$(PCR) \leftarrow (PCR) + 1 + [(ADFEQL) = 1]$

If the contents of the comparison storage register specify that the contents of the accumulator were equal to the operand of the last previous compare instruction, the next instruction in sequence is skipped; otherwise, the next instruction in sequence is taken. The contents of the accumulator are not affected.

SNE Skip on Compare Not Equal

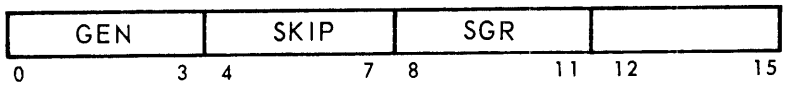


T: 1

(PCR) ← (PCR) + 1 + [(ADFEQL) = 0]

If the contents of the comparison storage register specify that the contents of the accumulator were not equal to the operand of the last previous compare instruction, the next instruction in sequence is skipped; otherwise, the next instruction in sequence is taken. The contents of the accumulator are not affected.

SGR Skip on Compare Greater

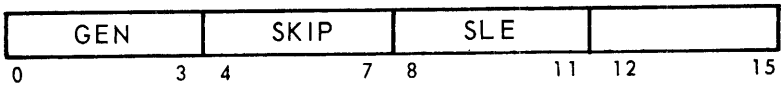


T: 1

(PCR) ← (PCR) + 1 + [(ADFEQL) = 0] ∧ [(ADFNEG) = 0]

If the contents of the comparison storage register specify that the contents of the accumulator were greater than the operand of the last previous compare instruction, the next instruction in sequence is skipped; otherwise, the next instruction in sequence is taken. The contents of the accumulator are not affected.

SLE Skip on Compare Less Than or Equal

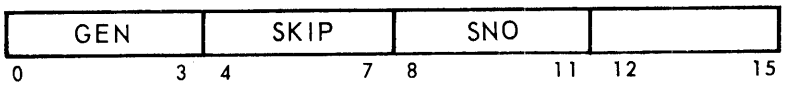


T: 1

(PCR) ← (PCR) + 1 + [(ADFNEG) = 1] ∨ [(ADFEQL)= 1]

If the contents of the comparison storage register specify that the contents of the accumulator were less than or equal to the operand for the last previous compare instruction, the next instruction in sequence is skipped; otherwise, the next instruction in sequence is taken. The contents of the accumulator are not affected.

SNO Skip on No Overflow

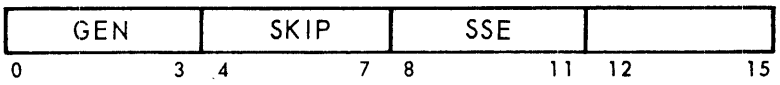


T: 1

(PCR) ← (PCR) + 1 + [(ADFOVF) = 0]; (ADFOVF) ← 0

If the contents of the overflow storage flip flop is zero, the next instruction in sequence is skipped; otherwise, the next instruction in sequence is taken. The content of the overflow storage flip flop is set to zero.

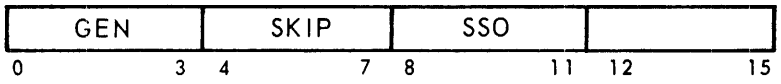
SSE Skip on Sense External



T: 1
(PCR) ← (PCR) + 1 + [SSE = 0]

If the external sense line is false, the next instruction in sequence is skipped; otherwise, the next instruction in sequence is taken.

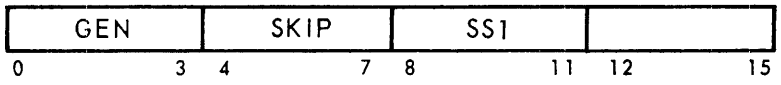
SS0 Skip on Sense Switch Zero False



T: 1
(PCR) ← (PCR)+ 1 + [SS0 = 0]

If sense switch zero is false, the next instruction in sequence is skipped; otherwise, the next instruction in sequence is taken.

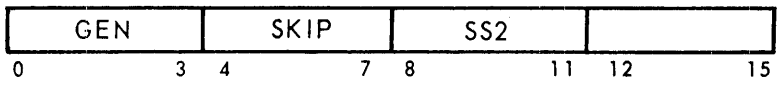
SS1 Skip on Sense Switch One False



T: 1
(PCR) ← (PCR) + 1 + [SS1 = 0]

If sense switch one is false, the next instruction in sequence is skipped; otherwise, the next instruction in sequence is taken.

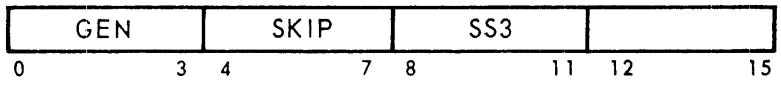
SS2 Skip on Sense Switch Two False



T: 1
(PCR) ← (PCR) + 1 + [SS2 = 0]

If sense switch two is false, the next instruction in sequence is skipped; otherwise, the next instruction in sequence is taken.

SS3 Skip on Sense Switch Three False



T: 1
(PCR) ← (PCR) + 1 + [SS3 = 0]

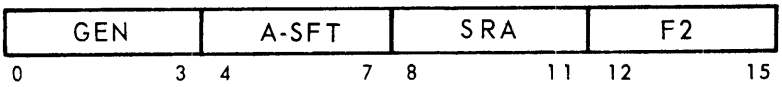
If sense switch three if false, the next instruction in sequence is skipped; otherwise, the next instruction in sequence is taken.

2-7.6 SHIFT GENERICS

Two basic classes of shift instructions, arithmetic and logical, are provided in which the shift type is specified by bits 4-7 of the instruction word (F1). Open and circular shifts, as well as their direction, and single or double precision are specified by bits 8-11. All single length shifts affect only the accumulator while double length shifts affect both the accumulator and index register, where the index register is treated as the right extension of the accumulator. The shift length is designated by bits 12-15 of the instruction word (F2).

2-7.6.1 Arithmetic Shifts

SRA Shift Right Arithmetic

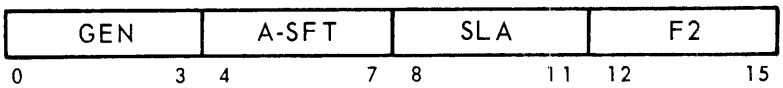


T: 2-5

$(ACR) \longleftarrow (ACR) \div 2^{M_{12-15}}$

The contents of the accumulator are shifted F2 positions to the right, as specified by bits 12-15 of the instruction word. The sign bit of the accumulator is unchanged by this operation and is shifted to bit 1 of the accumulator. Bits shifted off the right end of the register are lost.

SLA Shift left Arithmetic

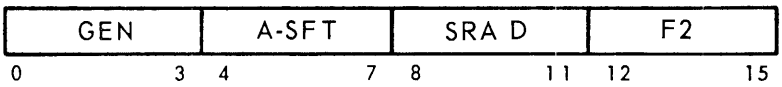


T: 2-5

$(ACR) \longleftarrow (ACR) \times 2^{M_{12-15}}$

The contents of the accumulator are shifted F2 positions to the left, as specified by bit positions 12-15 of the instruction word. Bits shifted from position 0 are lost and zeros replace the vacated bit positions on the right end of the accumulator. If the sign bit of the accumulator is changed by this operation, the overflow storage flip flop is set.

SRA D Shift right Arithmetic Double

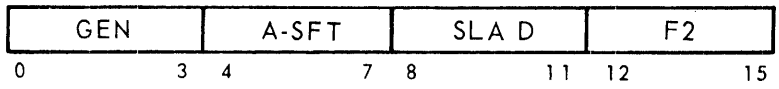


T: 2-5

$(ACR, IXR) \longleftarrow (ACR, IXR) \div 2^{M_{12-15}}$

The contents of the accumulator and index register are shifted F2 positions to the right as specified by bits 12-15 of the instruction word. The sign bit of the accumulator is unchanged by this operation, and is shifted to bit 1 of the accumulator. Bit 15 of the accumulator is shifted to bit 0 of the index register. Bits shifted off the right end of the index register are lost.

SLA D Shift left Arithmetic Double



T: 2-5

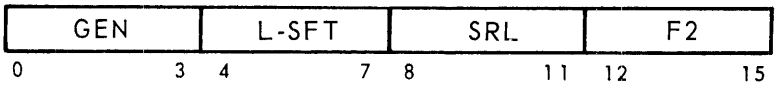
(ACR, IXR) ← (ACR, IXR) X $2^{M_{12-15}}$

The contents of the accumulator and index register are shifted F2 positions to the left, as specified by bit positions 12-15 of the instruction word. Bits shifted from bit position 0 of the accumulator are lost and zeros replace vacated bit positions on the right end of the index register. Bit 0 of the index register is shifted to bit 15 of the accumulator. If the sign bit of the accumulator is changed by this operation the overflow storage flip flop is set.

2-7.6.2 Logical Shifts

To keep the explanation of the logical shift functions as simple as practicable, the shift logic equations have been omitted from this section.

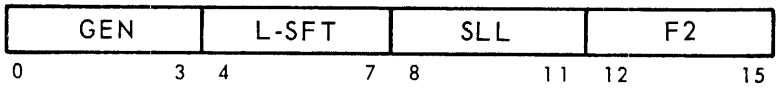
SRL Shift right logical



T: 2-5

The contents of the accumulator are shifted F2 positions to the right, as specified by bits 12-15 of the instruction word. Bits shifted off the right end of the accumulator are lost and zeros replace the vacated bit positions at the left end of the accumulator.

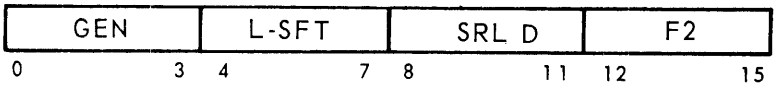
SLL Shift left logical



T: 2-5

The contents of the accumulator are shifted F2 positions to the left, as specified by bits 12-15 of the instruction word. Bits shifted off the left end of the accumulator are lost and zeros replace the vacated bit positions on the right end of the accumulator.

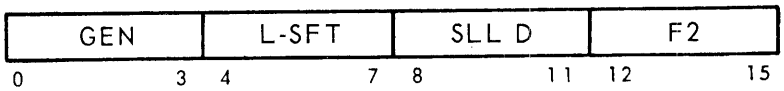
SRL D Shift right logical Double



T: 2-5

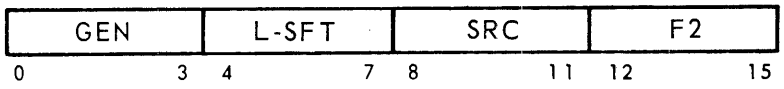
The contents of the accumulator and index register are shifted F2 positions to the right, as specified by bits 12-15 of the instruction word. Bit 15 of the accumulator is shifted into bit 0 of the index register. Bits shifted off the right end of the index register are lost and zeros replace the vacated bit positions on the left end of the accumulator.

SLL D Shift left logical Double
T: 2-5



The contents of the accumulator and index register are shifted F2 positions to the left, as specified by bits 12-15 of the instruction word. Bits shifted off the left end of the accumulator are lost and zeros replace the vacated bit positions on the right end of the index register. Bit 0 of the index register is shifted to bit 15 of the accumulator.

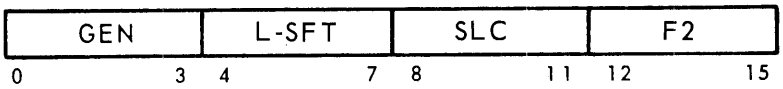
SRC Shift right circular



T: 2-5

The contents of the accumulator are shifted F2 positions to the right as specified by bits 12-15 of the instruction word. During this operation bit 15 of the accumulator is shifted to bit 0 in the accumulator.

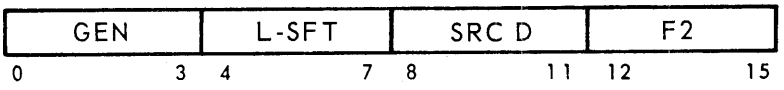
SLC Shift left circular



T: 2-5

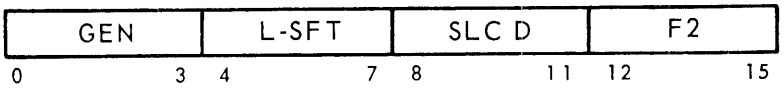
The contents of the accumulator are shifted F2 positions to the left, as specified by bits 12-15 of the instruction word. During this operation bit 0 of the accumulator is shifted to bit 15 of the accumulator.

SRC D Shift right circular Double
T: 2-5



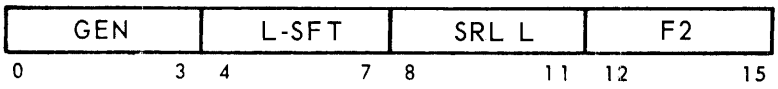
The contents of the accumulator and index register are shifted F2 positions to the right, as specified by bits 12-15 of the instruction word. During this operation bit 15 of the index register is shifted to bit zero of the accumulator. Bit 15 of the accumulator is shifted to bit 0 of the index register.

SLC D Shift left circular Double
T: 2-5



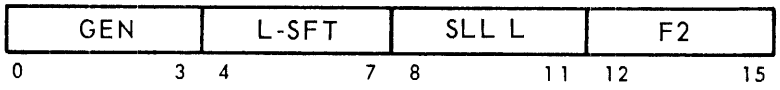
The contents of the accumulator and index register are shifted F2 positions to the left, as specified by bits 12-15 of the instruction word. During this operation bit 0 of the index register is shifted to bit 15 of the accumulator and bit 0 of the accumulator is shifted to bit 15 of the index register.

SRL L Shift right logical
Left byte
T: 2-5



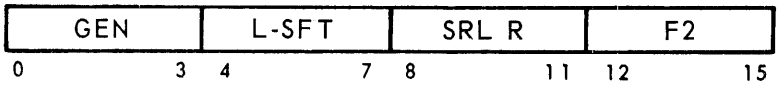
The contents of bits 0-7 of the accumulator are shifted F2 positions to the right as specified by bits 12-15 of the instruction word. Bits shifted out of bit position 7 are lost and zeros are inserted into bit position 0. The contents of bit positions 8-15 of the accumulator are not affected by this instruction.

SLL L Shift left logical
Left byte
T: 2-5



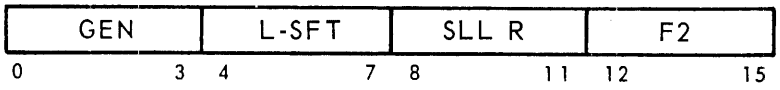
The contents of bit positions 0-7 of the accumulator are shifted F2 positions to the left as specified by bits 12-15 of the instruction word. Bits shifted out of bit position 0 are lost and zeros are inserted into bit position 7. The contents of bit positions 8-15 of the accumulator are not affected by this instruction.

SRL R Shift right logical
Right byte
T: 2-5



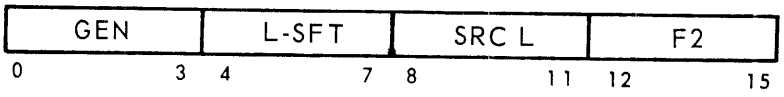
The contents of bit positions 8-15 of the accumulator are shifted F2 positions to the right, as specified by bits 12-15 of the instruction word. Bits shifted out of bit position 15 are lost and zeros are inserted into bit position 8. The contents of bit positions 0-7 of the accumulator are not affected by this instruction.

SLL R Shift left logical
Right byte
T: 2-5



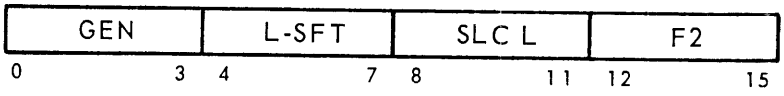
The contents of bit positions 8-15 of the accumulator are shifted F2 positions to the left as specified by bits 12-15 of the instruction word. Bits shifted out of bit position 8 are lost and zeros are inserted into bit position 15. The contents of bit positions 0-7 of the accumulator are not affected by this instruction.

SRC L Shift right circular
Left Byte
T: 2-5



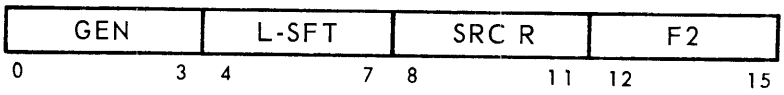
The contents of bit positions 0-7 of the accumulator are shifted F2 positions to the right as specified by bits 12-15 of the instruction word. During this operation bit 7 of the accumulator is shifted into bit 0 of the accumulator. The contents of bit positions 8-15 of the accumulator are not affected by this instruction.

SLC L Shift left circular
Left byte
T: 2-5



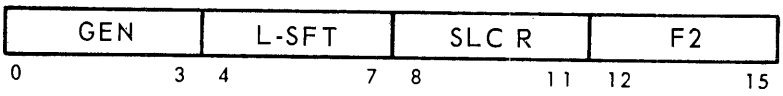
The contents of bit positions 0-7 of the accumulator are shifted F2 positions to the left as specified by bits 12-15 of the instruction word. During this operation bit 0 of the accumulator is shifted to bit 7 of the accumulator. The contents of bit positions 8-15 of the accumulator are not affected by this instruction.

SRC R Shift right circular
Right byte
T: 2-5



The contents of bit positions 8-15 of the accumulator are shifted F2 positions to the right as specified by bits 12-15 of the instruction word. During this operation bit 15 of the accumulator is shifted to bit 8 of the accumulator. The contents of bit positions 0-7 of the accumulator are not affected by this instruction.

SLC R Shift left circular
Right byte
T: 2-5



The contents of bit positions 8-15 of the accumulator are shifted F2 positions to the left as specified by bits 12-15 of the instruction word. During this operation bit 8 of the accumulator is shifted to bit 15 of the accumulator. The contents of bit positions 0-7 of the accumulator are not affected by this instruction.

Section 3

INTERRUPT

3-1 GENERAL

The priority interrupt system of the Raytheon 703 permits rapid response by the computer to events occurring external to the central processing unit (CPU). One level of interrupt is included with the basic system; however, expansion up to 16 levels is optionally available. Each level in the interrupt system may assume one of four states.

Disabled: The interrupt level is unable to respond to an interrupt. An interrupt signal sent from an external device is ignored.

Idle: The interrupt level is able to respond to an interrupt signal, but none has been received. The interrupt signal must have a pulse width greater than 1.75 microseconds.

Wait: An interrupt signal has been received, accepted, and the level is awaiting processing.

Active: The CPU has processed the interrupt by execution of a fixed hardware instruction sequence. The interrupt remains in the Active state until the program specifies an Interrupt Return or a Disable Interrupt.

Interrupt levels are numbered from 0 to 15. The lowest enabled interrupt level has the lowest priority. Level 0 is lowest. Level 15 is highest. Each interrupt level is allocated three unique words in the lower address portion of memory for storage of the program counter, an interrupt linkage address and machine status. Memory interrupt locations are assigned as follows:

00000	Interrupt Level 0	PCR Save
00001		Linkage Address
00002		Machine Status Save
00003		Unused by Interrupt Sequence
00004	Interrupt Level 1	PCR Save
00005		Linkage Address
00006		Machine Status Save
00007		Unused by Interrupt Sequence
--	--	--
00060	Interrupt Level 15	PCR Save
00061		Linkage Address
00062		Machine Status Save
00063		Unused by Interrupt Sequence

3-2 PROGRAMMING WITH THE INTERRUPT SYSTEM

The Raytheon 703 has five instructions which allow the user to achieve full utilization of the priority interrupt system. These instructions are Mask Interrupts (MSK), Unmask Interrupts (UNM), Enable Interrupt (ENB), Disable Interrupt (DSB), and Interrupt Return (INR).

To allow an interrupt subroutine to complete at least a few essential operations before it is itself interrupted, the Mask Interrupts (MSK) instruction may be employed. Execution of the MSK instruction inhibits all levels from causing interruptions to the current program. However, the interrupt conditions remain pending and will be serviced by the 703 CPU when the interrupt inhibit mask is removed. The interrupt inhibit mask is removed by the execution of the Unmask Interrupts (UNM) instruction.

Initialization of the Raytheon 703 (power ON or RESET) sets all interrupt levels to the Disabled state and removes the interrupt inhibit mask. Each interrupt level may advance from the Disabled state to the Idle state by execution of an Enable Interrupt (ENB) instruction which specifies the particular level. The Disable Interrupt (DSB) instruction changes the referenced interrupt level from its present state (Idle, Wait, or Active) to the Disabled state.

When the interrupt subroutine completes its operation, the interrupt level can be returned to the Idle state and control returned to the interrupted program by execution of the Interrupt Return (INR) instruction. The INR instruction specifies the interrupt level being returned to the Idle state and restores the program counter and machine status to what they were at time of interrupt.

3-3 OPERATION OF THE INTERRUPT SYSTEM

The operation of an interrupt level is shown in the flow chart, Figure 3-1. When power is turned on, or when the RESET switch on the control panel is activated, all interrupt levels are set to the Disabled state and the inhibit interrupt mask is set off. Interrupt levels, on an individual basis, may be transferred from the Disabled state to the Idle state by the ENB instruction.

When an interrupt level is in the Idle state, any interrupt signal to that level with duration greater than 1.75 microseconds causes an advance to the Wait state. An interrupt level in the Wait state is advanced to the Active state when there is no higher priority interrupt level in the Active or the Wait state, the inhibit interrupt mask is off, and the execution of the current instruction is completed by the 703 CPU.

When an interrupt level advances to the Active state a fixed hardware sequence stores the contents of the program counter, stores the machine status, places the central processor in global mode, and transfers to the interrupt linkage address. Machine status consists of the contents of the extension register, the overflow indicator, the comparison indicators, and the memory addressing mode (local/global) at the time of interrupt. An interrupt level remains in the Active state until the interrupt subroutine is completed. The INR instruction returns the interrupt to the Idle state and restores the program counter and the machine status to their previous condition at time of interrupt.

An interrupt level in the Active state does not necessarily imply that the 703 CPU is still under control of this particular level of interrupt. The 703 CPU can be under control of a higher priority interrupt subroutine. Priority control allows the highest level in the Wait or Active state to postpone lower priority interrupts that are pending. For example, if interrupt level 7 is in the Active state, interrupt levels 0 to 6 that are in the Wait state will not be serviced by the 703 CPU. The pending lower priority interrupts will not occur until interrupt level 7 is changed to the Idle or the Disabled state by either the INR or the DSB instruction. However, if any interrupt level from 8 to 15 should change to Wait state while interrupt level 7 is in the Active state, an interrupt would occur and control transferred to the higher priority subroutine.

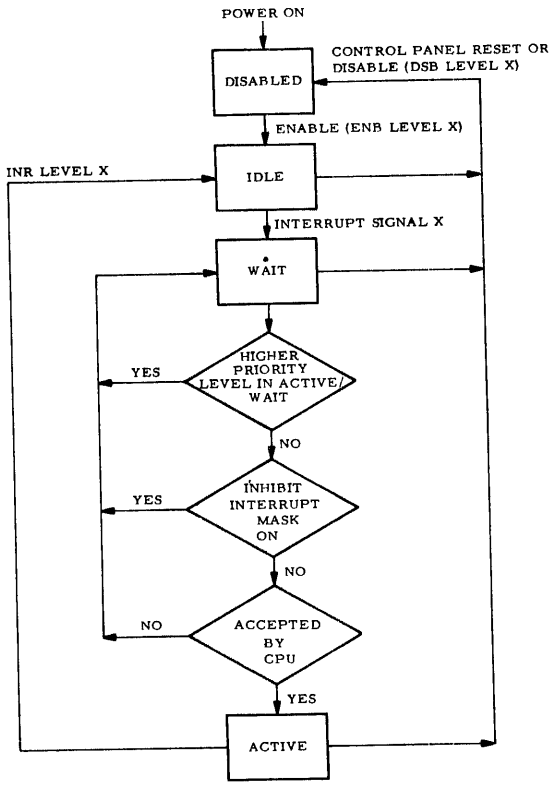


Figure 3-1.
Interrupt Operation for Level X
(X = 0, 1, 2..... 15)

Section 4

INPUT / OUTPUT

4-1 GENERAL

The Raytheon 703 has two types of input/output communication channels, Direct Input/Output (DIO) and Direct Memory Access (DMA). The DIO channel permits direct exchange of 16-bit data words between the accumulator register and a selected external device under direct program control. The DMA channel allows exchange of 16-bit data words between 703 memory and up to six external devices simultaneously, interlaced with computation.

4-2 DIRECT INPUT/OUTPUT

4-2.1 GENERAL DESCRIPTION

Exchange of information directly between external devices and the 703 CPU is provided by the direct input/output channel (see figure 4-1). This channel consists of an 8-bit external address bus, a 16-bit output bus, a 16-bit input bus and two strobe lines.

Operation of this channel is controlled by two instructions, Direct Input (DIN) and Direct Output (DOT). A DIN instruction causes its 8-bit DIO address to be placed on the address bus and produces an input strobe signal (ISB). The data placed on the input bus by the addressed device are transferred to the accumulator at the trailing edge of the strobe signal. Execution of a DOT instruction causes the address to be placed on the address bus, the contents of the accumulator to be placed on the data output bus, and an output strobe signal (OSB). Data may be taken from the output bus by the external device at any point during the OSB period.

The 8-bit DIO address has the following format.

Bits 8-11 designate the selected external device. Bits 12-15 designate the function to be performed. Each external device is assigned a unique device code and may use as many of the 16 function codes as necessary.

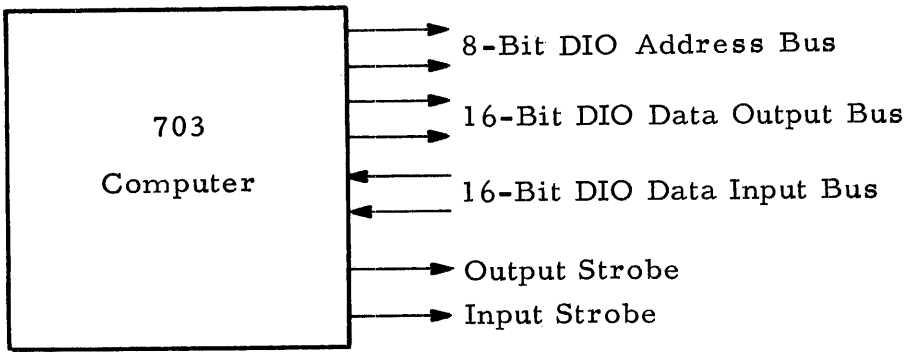


Figure 4-1. Direct Input/Output Channel

4-2.2 APPLICATIONS INFORMATION

4-2.2.1 Interface

All DIO signals are available on connector J2, a 90 pin ELCO connector mounted on the back panel of the 703 central processor chassis, and on the last connector of the I/O system. (Mating connector is Raytheon PN 530724-500.) These signals are as follows:

DAD08 - to DAD15 -	8-bit address bus
DOT00 - to DOT15 -	16-bit data output bus
DIN00 - to DIN15 -	16-bit data input bus
DOSB -	Data output strobe
DISB -	Data input strobe
KEXT -	External clock
EXSENS -	External sense input
INTRPT00 - to INTRPT15	Interrupt inputs
REXT -	External reset output
V+3.6	Power
MT0 -	Memory timing pulse 0
MT2 -	Memory timing pulse 2
MT4 -	Memory timing pulse 4

Table 4-1 defines pin locations of the signals on this connector.

The following design rules apply when interfacing with the 703 I/O communication channels:

1. Drivers should be Raytheon 844 Power Gates or their equivalents.

2. The receivers may be any diode transistor logic (DTL) circuits.

3. DIO output lines using Raytheon 844 drivers will drive up to 50 feet of twisted pair cable with up to 15 loads. The external equipment on the last position of the line must provide a resistor network termination as shown in figure 4-2.

Table 4-1. Direct I/O Connector J2

Signal	Signal Pin	Ground Pin
DIN00 -	A	J
DIN01 -	B	J
DIN02 -	H	J
DIN03 -	C	L
DIN04 -	D	L
DIN05 -	K	L
DIN06 -	E	N
DIN07 -	F	N
DIN08 -	M	N
DIN09 -	R	AE
DIN10 -	X	AE
DIN11 -	AM	AE
DIN12 -	S	Z
DIN13 -	T	Z
DIN14 -	Y	Z
DIN15 -	U	AB
DOT00 -	V	AB
DOT01 -	AA	AB
DOT02 -	P	W
DOT03 -	AC	W
DOT04 -	AD	W
DOT05 -	AF	AP
DOT06 -	AH	AP
DOT07 -	AN	AP
DOT08 -	AJ	AS
DOT09 -	AK	AS
DOT10 -	AR	AS
DOT11 -	AL	AU
DOT12 -	AT	AU
DOT13 -	AY	AU
DOT14 -	AV	BA
DOT15 -	AW	BA
DAD08 -	AZ	BA

Signal	Signal Pin	Ground Pin
DAD09 -	AX	BC
DAD10 -	BB	BC
DAD11 -	BH	BC
DAD12 -	BD	BK
DAD13 -	BE	BK
DAD14 -	BJ	BK
DAD15 -	BL	BN
DOSB -	BM	BN
DISB -	BF	BN
KEXT -	BP	BX
EXSENS -	BR	BX
REXT -	BS	BZ
V+3.6A -	BT	BZ
V+3.6B -	CZ	DA
V+3.6C -	DB	DA
MT0 -	BY	BZ
MT2 -	BU	CB
MT4 -	BV	CB
INTRPT00 -	BW	BX
INTRPT01 -	CA	CB
INTRPT02 -	CC	CE
INTRPT03 -	CD	CE
INTRPT04 -	CV	CE
INTRPT05 -	CF	CP
INTRPT06 -	CH	CP
INTRPT07 -	CN	CP
INTRPT08 -	CJ	CS
INTRPT09 -	CK	CS
INTRPT10 -	CR	CS
INTRPT11 -	CL	CU
INTRPT12 -	CM	CU
INTRPT13 -	CT	CU
INTRPT14 -	CW	CX
INTRPT15 -	CY	CX

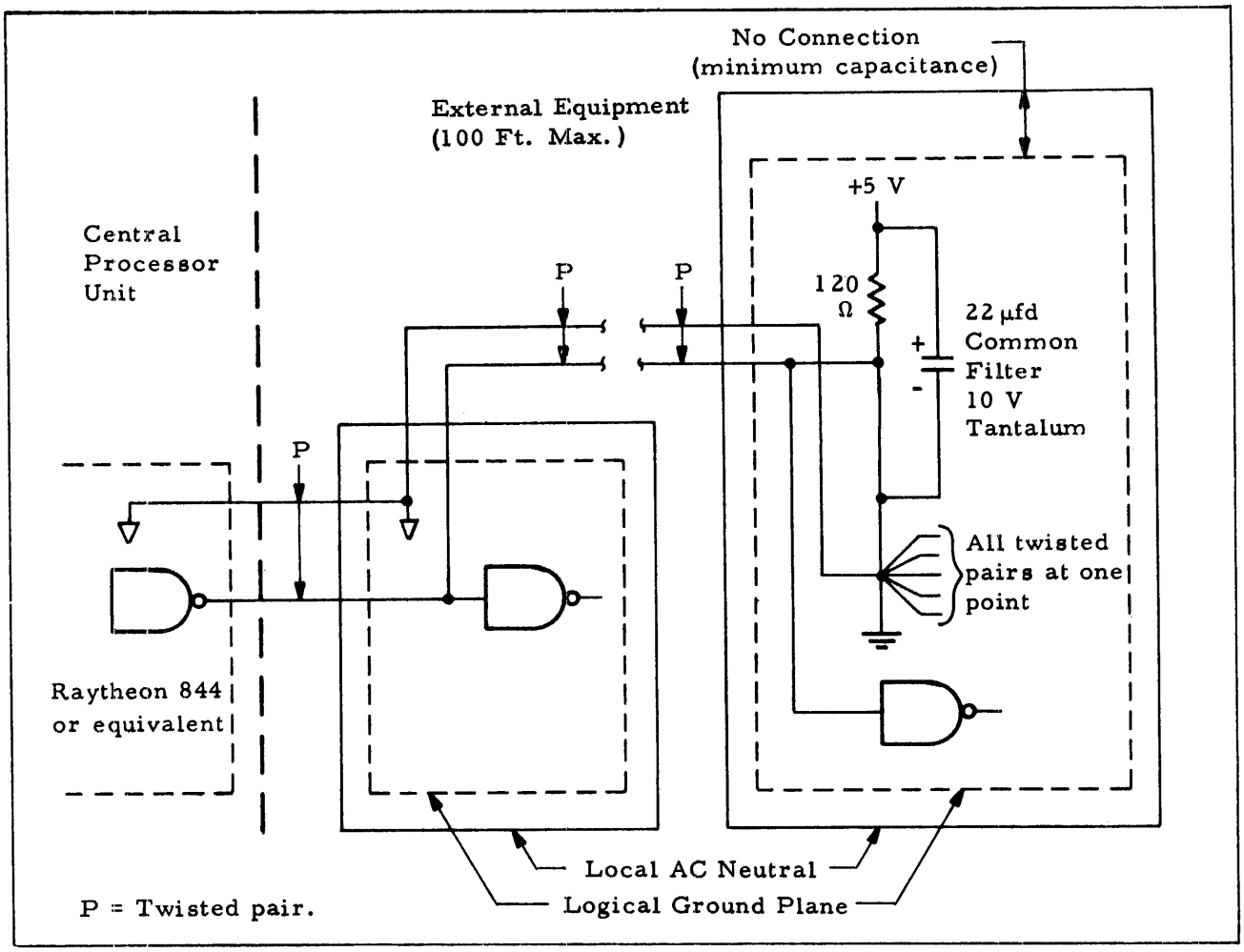


Figure 4-2. DIO Output Line Terminations

4. In the external equipment, DIO input lines should be treated as bus lines driven by Raytheon 844 Power Gates. When an external equipment is not communicating with the DIO, the drivers within that equipment should be disabled with at least one input to the 844 held false. Each DIO input line may be driven by 16 drivers in parallel. The processor provides proper terminations for the ends of the DIO input lines. The external equipment on the last position of the DIO input lines must provide proper terminations for the other ends of the lines. The terminations are as shown in figure 4-3.

5. The resistor terminations in the external equipment may be placed in an end cap to facilitate changing the location of these terminations when the relative position of the external equipment is changed.

6. All DIO input and output signal levels are negative true as follows:

True "1"	Nominal 0V
False "0"	Nominal +3.6V

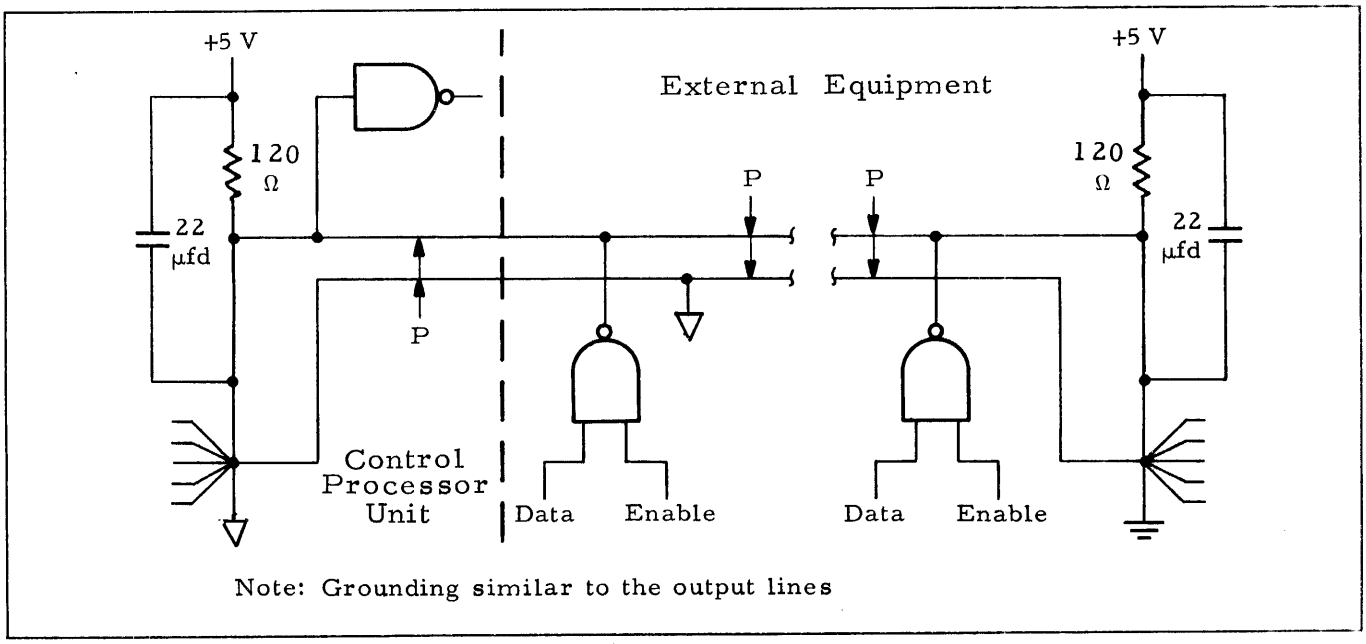


Figure 4-3. DIO Input Line Terminations

4-2.2.2 Timing

Figure 4-4 illustrates the timing of the DIO interface.

Note that for direct output, the address and data are stable at least 700 nsec before and 350 nsec after the output strobe. For direct input, data may be applied to the input bus during the first 1.05 µsec of the data strobe, and must be stable during the final 350 nsec of this strobe. DIO data and address outputs are not gated with the strobe signals.

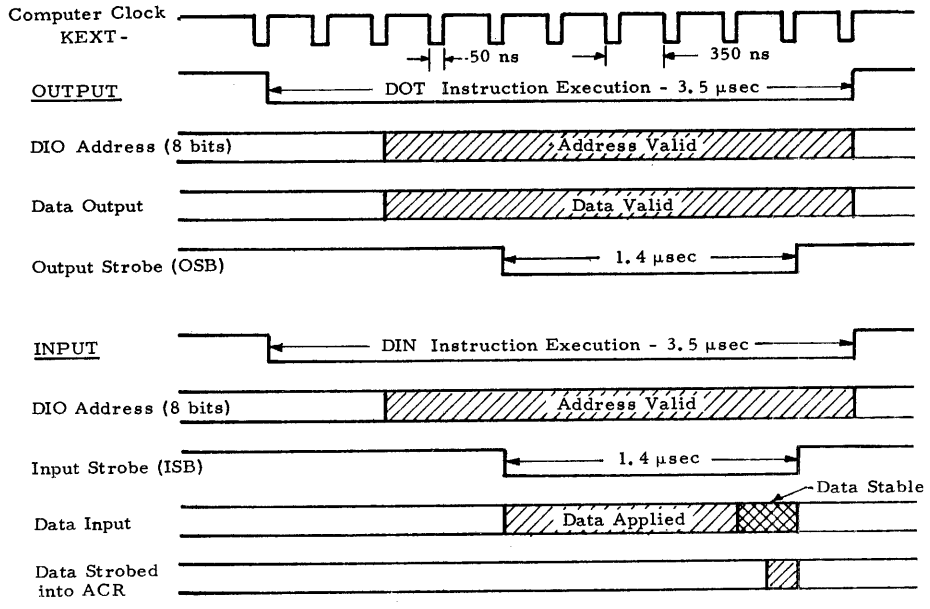


Figure 4-4. DIO Interface Timing

4.3 DIRECT MEMORY ACCESS

4-3.1 GENERAL DESCRIPTION

Exchange of information between the 703 memory and external devices is provided by the direct memory access channel option, see figure 4-5. Operation of this channel is independent of the operation of the 703 CPU.

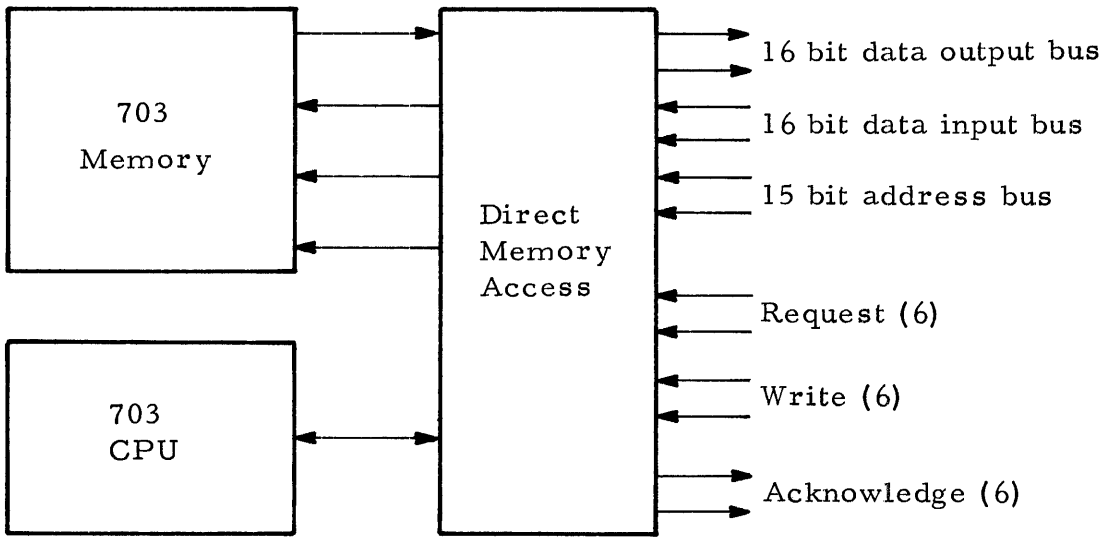


Figure 4-5. Direct Memory Access

Six external devices may communicate with the memory simultaneously on an interlaced, fixed priority basis. Each device uses three control lines to effect a memory operation:

1. Request - A signal produced by the device to request a transfer.

2. Write - A signal produced by the device to indicate a write operation. If false, a read operation occurs.

3. Acknowledge - A signal produced by the DMA to initiate and control the requested transfer.

Data and address must be applied to the input bus lines only during the acknowledge. Data may be taken from the output bus during the acknowledge period on the occurrence of timing strobe MT2. Memory access priority is assigned on a fixed basis; a higher numbered channel will gain access over lower numbered channels.

4-3.2 APPLICATION INFORMATION

4-3.2.1 Interface

All DMA signals are available on connector J5, a 120 pin ELCO connector mounted on the back panel of the 703 central processor chassis. (Mating connector is Raytheon PN 530724-006) These signals are as follows:

MMAD01 - to MMAD15 -	15-bit address bus
MMDI00 - to MMDI15 -	16-bit data input bus
MMDO00 - to MMDO15 -	16-bit data output bus
MRQ2 - to MRQ7 -	Six request control inputs
MWT2 - to MWT7 -	Six write control inputs
MAK2 - to MAK7 -	Six acknowledge control outputs
MT0 -	Timing strobe 0
MT2 -	Timing strobe 2
MT4 -	Timing strobe 4
KEXT -	External clock
REXT -	External reset
V+3.6	Power

Table 4-2 defines pin locations of these signals on the connectors. All DMA input and output signal levels are "negative true" as follows:

True "1"	Nominal 0V
False "0"	Nominal +3.6V

4-3.2.2 Timing

Figure 4-6 illustrates the timing of the DMA interface. Note that for read, data is available from the beginning of MT2 through the following MT4. If writing, the address input and the data input must be enabled with the acknowledge signal. The memory request line may be applied any time prior to MT2, but it must be stable from MT2 to MT4, and must be removed no later than the start of the next MT0 during which the access is granted.

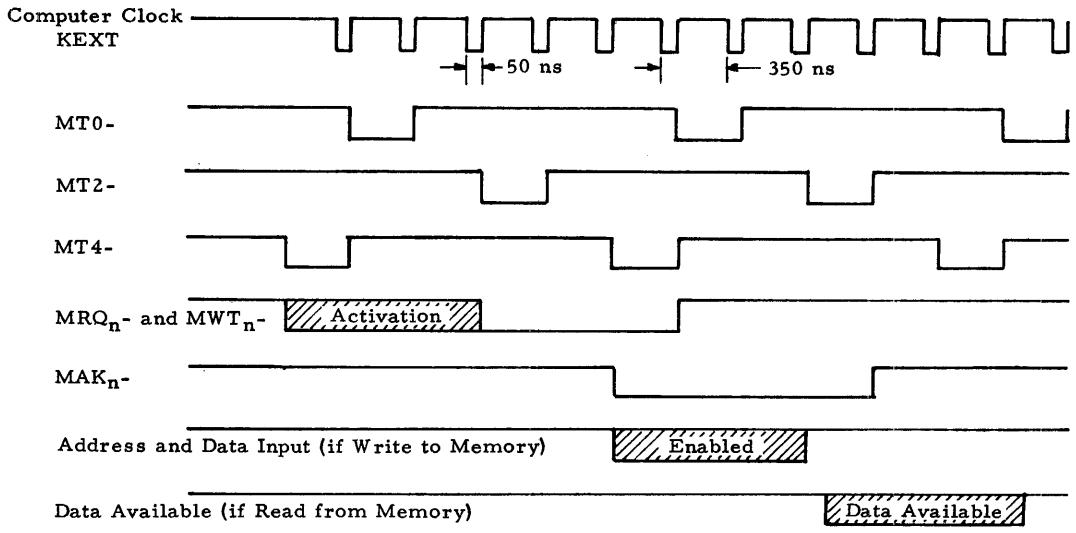


Figure 4-6. DMA Interface Timing

Table 4-2. Direct Memory Access Connector J5

Signal	Signal Pin	Ground Pin	Signal	Signal Pin	Ground Pin
MRQ2 -	A	L	MMDI04 -	BH	BW
MRQ3 -	B	L	MMDI05 -	BP	BW
MRQ4 -	K	L	MMDI06 -	CC	BW
MRQ5 -	C	N	MMDI07 -	BJ	BS
MRQ6 -	D	N	MMDI08 -	BK	BS
MRQ7 -	M	N	MMDI09 -	BR	BS
MAK2 -	E	R	MMDI10 -	BL	BY
MAK3 -	F	R	MMDI11 -	BT	BY
MAK4 -	P	R	MMDI12 -	BX	BY
MAK5 -	H	T	MMDI13 -	BU	CB
MAK6 -	J	T	MMDI14 -	BV	CB
MAK7 -	S	T	MMDI15 -	CA	CB
MWT2 -	V	AE	MMDO00 -	BZ	CF
MWT3 -	W	AE	MMDO01 -	CD	CF
MWT4 -	AD	AE	MMDO02 -	CE	CF
MWT5 -	X	AH	MMDO03 -	CH	CK
MWT6 -	Y	AH	MMDO04 -	CJ	CK
MWT7 -	AF	AH	MMDO05 -	CL	CK
MMAD01 -	AJ	AK	MMDO06 -	CM	CX
MMAD02 -	AB	AM	MMDO07 -	CN	CX
MMAD03 -	AC	AM	MMDO08 -	CW	CX
MMAD04 -	AL	AM	MMDO09 -	CP	CZ
MMAD05 -	U	AN	MMDO10 -	CR	CZ
MMAD06 -	AW	AN	MMDO11 -	CY	CZ
MMAD07 -	AX	AN	MMDO12 -	CS	DB
MMAD08 -	AP	AZ	MMDO13 -	CT	DB
MMAD09 -	AR	AZ	MMDO14 -	DA	DB
MMAD10 -	AY	AZ	MMDO15 -	CU	DD
MMAD11 -	AS	BB	MT0 -	DJ	DU
MMAD12 -	AT	BB	MT2 -	DT	DU
MMAD13 -	BA	BB	MT4 -	DM	DW
MMAD14 -	AU	BD	KEXT -	DV	DW
MMAD15 -	AV	BD	REXT -	DN	DY
MMDI00 -	BC	BD	V+3.6G	EF	EE
MMDI01 -	BE	BN	V+3.6H	EH	EK
MMDI02 -	BF	BN	V+3.6J	EJ	EK
MMDI03 -	BM	BN	V+3.6K	EL	EK

Section 5

CONTROLS AND INDICATORS

5-1 GENERAL

Each of the controls and indicators appearing on the front panel of the 703 are described below.

PROGRAM COUNTER Switch-Indicators

The PROGRAM COUNTER switch-indicators provide direct access to the Program Counter for both alteration and display. The indicators continually monitor the contents of the PROGRAM COUNTER for display purposes. The switches allow entry of a specific memory address. Note that the PROGRAM COUNTER is always active for both entry and display.

Program Counter CLEAR Switch

Actuating this switch resets the Program Counter Register.

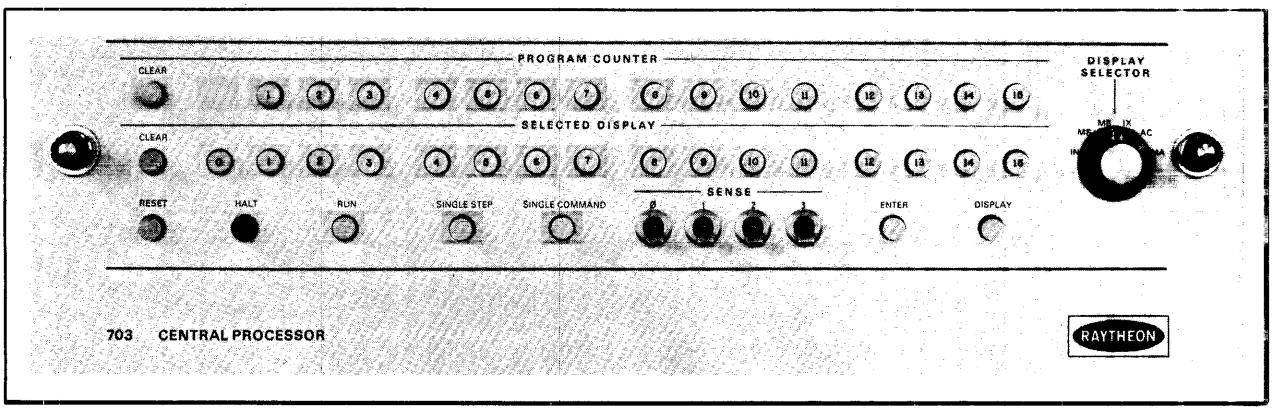


Figure 5-1. Raytheon 703 Control Panel

DISPLAY SELECTOR Switch

The DISPLAY SELECTOR switch has six positions -- MS, IN, MA, MB, IX, and AC. The switch permits register selection for display or data entry. The specific function of each position is described below:

MS This position displays machine status which includes the extension register, the comparison flip-flops, the overflow flip-flop, the local/global mode flip-flop, and the sequence register. In this position, the adjacent SELECTED DISPLAY indicators 0-4 display the extension register, indicator 5 displays ADFNEG, indicator 6 displays ADFEQL, indicator 7 displays overflow, indicator 8 displays local/global mode, and indicators 12-15 display the sequence register. This position of the switch is active for display only.

IN This position displays the contents of the Instruction register in 0-7 of the SELECTED DISPLAY indicators. This position of the switch is active for display only.

MA This position displays the 16-bit Memory Address Register (MAR) onthe SELECTED DISPLAY indicators. This position of the switch is active for display only.

MB This position provides direct access to the Memory Buffer Register (MBR) for both alteration and display. The SELECTED DISPLAY indicators display the contents of the MBR and the SELECTED DISPLAY switches allow entry of data directly into the MBR. Prior to entering data in this position, the adjacent CLEAR switch must be actuated to reset the MBR. This position illuminates the ENTER and DISPLAY indicators.

IX This position provides direct access to the Index Register for both alteration and display in a manner similar to the Memory Buffer Register.

AC This position provides direct access to the Accumulator for both alteration and display in a manner similar to the Memory Buffer Register.

The position of the DISPLAY SELECTOR can be changed while the program is running.

Display CLEAR Switch-Indicator

Actuating this switch clears the register associated with DISPLAY SELECTOR positions MB, IX, or AC.

ENTER Switch Indicator

Actuating this switch enters the contents of Memory Buffer Register (MBR) into the memory location specified by the 15-bit Program Counter Register (PCR) and increments the PCR by one count. This switch is illuminated when MB is selected.

DISPLAY Switch Indicator

Actuating this switch fetches data from the memory location specified by the Program Counter Register (PCR) and enters the data into the Memory Buffer Register (MBR). The PCR is then incremented by one count. This switch is illuminated when MB is selected.

SINGLE COMMAND Switch

Each actuation of the switch executes one instruction (manually entered or stored in memory), then halts. This switch is normally used when debugging programs.

SINGLE STEP Switch

This switch is primarily a maintenance aid and inhibits the SINGLE COMMAND and RUN mode switches. The operator can execute single instructions on a step-by-step basis and can observe the performance of the computer via the DISPLAY SELECTOR switch and the SELECTED DISPLAY indicators. The SINGLE STEP mode can only be terminated by the HALT switch. By actuating HALT, the instruction being executed on a step-by-step basis is completed and the computer is put in the HALT state.

RESET Switch

This is the master reset switch that resets all registers and peripherals.

RUN Switch

Actuating the RUN switch initiates a program process.

HALT Switch

Actuating the HALT switch halts the program being executed at the completion of the current instruction. This applies to both the RUN mode and the SINGLE STEP mode.

SENSE SWITCHES Toggles

These four switches permit the operator to modify a program by selecting a specific branch (or skip) condition within the program. The SENSE SWITCHES are operator setable and program testable. When the switch is in the down (false) position, the branch condition is selected.

Section 6

HARDWARE MULTIPLY/DIVIDE

6-1 GENERAL

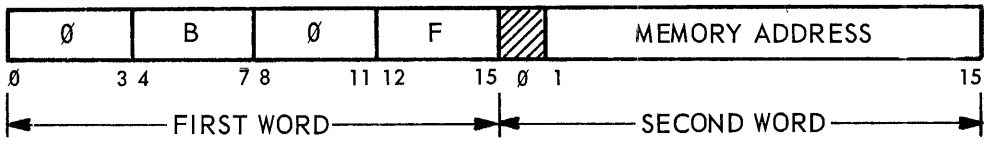
Hardware multiply/divide is an option which performs a 16-bit, 2's complement multiply or divide. In each case, a double length result is produced.

The multiply/divide instruction format requires two consecutive memory locations. The first location defines the instruction, multiply or divide, and the second location defines a 15-bit address which contains the multiplicand for a multiply or the divisor for a divide. The 15-bit address allows either instruction to reference any location in memory without using the index register. The index register is not available for address modification during the execution of multiply and divide instructions. It is utilized with the accumulator (ACR) to form the double precision register required by the operation.

6-2 MULTIPLICATION

The multiply instruction has an execution time of 12.25 to 17.5 microseconds and a format as shown below:

Multiply (MPY)



The multiply instruction utilizes a 16-bit multiplier which resides in the accumulator and a 16-bit multiplicand which resides in the memory location specified by the instruction. Negative numbers are expressed in 2's complement form.

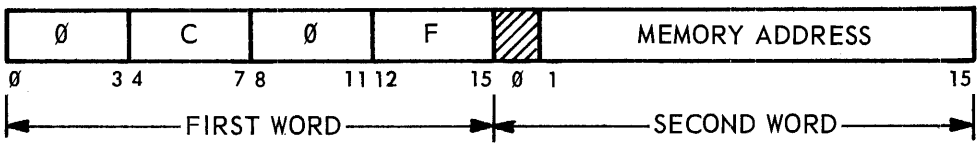
Execution of the multiply instruction produces a 31-bit algebraic product in the index register and the accumulator. The most significant 16 bits of the product reside in the index register. The least significant 15 bits of the product reside in bits 1-15 of the accumulator. The most significant bit of

the accumulator is set to the most significant bit of the index register. The product, if negative, is expressed in 2's complement form. No overflow can result from the multiply instruction.

6-3 DIVISION

The divide instruction has an execution time of 24.5 microseconds and a format as shown below:

Divide (DIV)



The divide instruction utilizes a 31-bit dividend which resides in the accumulator and the index register. The most significant 16 bits of the dividend reside in the index register and the least significant 15 bits are located in bits 1-15 of the accumulator. The most significant bit of the accumulator has no effect on the divide instruction. The 16-bit divisor resides in the memory location specified by the instruction. Negative numbers are expressed in 2's complement form.

Execution of the divide instruction produces a 16-bit algebraic quotient in the accumulator and a 16-bit remainder in the index register. The sign of the remainder is the same as that of the dividend. Both numbers, if negative, are expressed in 2's complement form.

Care must be exercised in the set-up of the divide instruction to avoid an overflow condition. An overflow condition exists when the quotient is greater than 16 bits. The overflow indicator is turned ON and the dividend contained in the index register and the accumulator remains unchanged, except the most significant bit of the accumulator is set to the most significant bit of the index register. The execution time of the divide instruction for this condition is 8.75 microseconds.

APPENDICES

Appendix A

MNEMONIC INDEX OF INSTRUCTIONS

Mnemonic	Op Code	Operation Name	Number of Cycles	Time in μs	Page
ADD	A	Add	2	3.5	2-3
AND	E	Logical AND	2	3.5	2-4
CAX	013	Copy Accumulator to Index	1	1.75	2-9
CEX	006	Copy Extension to Index	1	1.75	2-8
CLB	07	Compare Literal Byte	1	1.75	2-11
CLR	010	Clear Accumulator	1	1.75	2-8
CMB	4	Compare Byte	2	3.5	2-5
CMP	011	Complement Accumulator	1	1.75	2-9
CMW	F	Compare Word	2	3.5	2-5
CXA	014	Copy Index to Accumulator	1	1.75	2-9
CXE	007	Copy Index to Extension	1	1.75	2-8
DIN	02	Direct Input	2	3.5	2-9
DOT	03	Direct Output	2	3.5	2-10
DSB	003	Disable Interrupt	1	1.75	2-7
DXS	05	Decrement Index and Skip if less than 0	2	3.5	2-10
ENB	002	Enable Interrupt	1	1.75	2-6
HLT	000	Halt	1	1.75	2-6
INR	001	Interrupt Return	3	5.25	2-6
INV	012	Invert Accumulator	1	1.75	2-9
IXS	04	Increment Index and Skip if greater than 0	2	3.5	2-10
JMP	1	Unconditional Jump	1	1.75	2-5
JSX	2	Jump and Store Return in Index	2	3.5	2-6
LDB	5	Load Byte	2	3.5	2-1
LDW	8	Load Work	2	3.5	2-1
LDX	9	Load Index	2	3.5	2-1
LLB	06	Load Literal Byte	1	1.75	2-10
MSK	00A	Mask Interrupts	1	1.75	2-7
ORE	D	Exclusive OR	2	3.5	2-4
ORI	C	Inclusive OR	2	3.5	2-4
SAM	082	Skip on Accumulator Minus	1	1.75	2-11
SAO	083	Skip on Accumulator Odd	1	1.75	2-12
SAP	081	Skip on Accumulator Plus	1	1.75	2-11
SAZ	080	Skip on Accumulator Zero	1	1.75	2-11
SEQ	086	Skip on Compare Equal	1	1.75	2-12

Appendix A

MNEMONIC INDEX OF INSTRUCTIONS (CONT.)

Mnemonic	Op Code	Operation Name	Number of Cycles	Time in μs	Page
SGM	005	Set Global Mode	1	1.75	2-7
SGR	088	Skip on Compare Greater	1	1.75	2-13
SLA	091	Shift Left Arithmetic	2-5	3.5 - 8.75	2-15
SLA D	093	Shift Left Arithmetic Double	2-5	3.5 - 8.75	2-16
SLC	0A5	Shift Left Circular	2-5	3.5 - 8.75	2-17
SLC D	0A7	Shift Left Circular Double	2-5	3.5 - 8.75	2-17
SLC L	0AD	Shift Left Circular Left Byte	2-5	3.5 - 8.75	2-19
SLC R	0AF	Shift Left Circular Right Byte	2-5	3.5 - 8.75	2-19
SLE	089	Skip on Compare Less Than or Equal	1	1.75	2-13
SLL	0A1	Shift Left Logical	2-5	3.5 - 8.75	2-16
SLL D	0A3	Shift Left Logical Double	2-5	3.5 - 8.75	2-17
SLL L	0A9	Shift Left Logical Left Byte	2-5	3.5 - 8.75	2-18
SLL R	0AB	Shift Left Logical Right Byte	2-5	3.5 - 8.75	2-18
SLM	004	Set Local Mode	1	1.75	2-7
SLS	084	Skip on Compare Less	1	1.75	2-12
SML	008	Select Memory Lower	1	1.75	2-8
SMU	009	Select Memory Upper	1	1.75	2-8
SNE	087	Skip on Compare Not Equal	1	1.75	2-13
SNO	08A	Skip on No Overflow	1	1.75	2-13
SRA	090	Shift Right Arithmetic	2-5	3.5 - 8.75	2-15
SRA D	092	Shift Right Arithmetic Double	2-5	3.5 - 8.75	2-15
SRC	0A4	Shift Right Circular	2-5	3.5 - 8.75	2-17
SRC D	0A6	Shift Right Circular Double	2-5	3.5 - 8.75	2-17
SRC L	0AC	Shift Right Circular Left Byte	2-5	3.5 - 8.75	2-19
SRC R	0AE	Shift Right Circular Right Byte	2-5	3.5 - 8.75	2-19
SRL	0A0	Shift Right Logical	2-5	3.5 - 8.75	2-16
SRL D	0A2	Shift Right Logical Double	2-5	3.5 - 8.75	2-16
SRL L	0A8	Shift Right Logical Left Byte	2-5	3.5 - 8.75	2-18
SRL R	0AA	Shift Right Logical Right Byte	2-5	3.5 - 8.75	2-18
SSE	08B	Skip on Sense External	1	1.75	2-14
SS0	08C	Skip on Sense Switch Zero False	1	1.75	2-14
SS1	08D	Skip on Sense Switch One False	1	1.75	2-14
SS2	08E	Skip on Sense Switch Two False	1	1.75	2-14
SS3	08F	Skip on Sense Switch Three False	1	1.75	2-14
STB	3	Store Byte	3	5.25	2-3

Appendix A

MNEMONIC INDEX OF INSTRUCTIONS (CONT.)

Mnemonic	Op Code	Operation Name	Number of Cycles	Time in μs	Page
STW	7	Store Word	2	3.5	2-3
STX	6	Store Index	2	3.5	2-3
SUB	B	Subtract	2	3.5	2-4
SXE	085	Skip on Index Even	1	1.75	2-12
UNM	00B	Unmask Interrupts	1	1.75	2-7

Appendix B

OP CODES INDEX OF INSTRUCTIONS

Op Code	Mnemonic	Operation Name	Number of Cycles	Time in μs	Page
0	GEN	Generics			2-6
1	JMP	Jump	1	1.75	2-5
2	JSX	Jump and Store Return in Index	2	3.5	2-6
3	STB	Store Byte	3	5.25	2-3
4	CMB	Compare Byte	2	3.5	2-5
5	LDB	Load Byte	2	3.5	2-1
6	STX	Store Index	2	3.5	2-3
7	STW	Store Word	2	3.5	2-3
8	LDW	Load Word	2	3.5	2-1
9	LDX	Load Index	2	3.5	2-1
A	ADD	Add	2	3.5	2-3
B	SUB	Subtract	2	3.5	2-4
C	ORI	Inclusive OR	2	3.5	2-4
D	ORE	Exclusive OR	2	3.5	2-4
E	AND	Logical AND	2	3.5	2-4
F	CMW	Compare Word	2	3.5	2-5
000	HLT	Halt	1	1.75	2-6
001	INR	Interrupt Return	3	5.25	2-6
002	ENB	Enable Interrupt	1	1.75	2-6
003	DSB	Disable Interrupt	1	1.75	2-7
004	SLM	Set Local Mode	1	1.75	2-7
005	SGM	Set Global Mode	1	1.75	2-7
006	CEX	Copy Extension to Index	1	1.75	2-8
007	CXE	Copy Index to Extension	1	1.75	2-8
008	SML	Select Memory Lower	1	1.75	2-8
009	SMU	Select Memory Upper	1	1.75	2-8
00A	MSK	Mask Interrupts	1	1.75	2-7
00B	UNM	Unmask Interrupts	1	1.75	2-7
010	CLR	Clear Accumulator	1	1.75	2-8
011	CMP	Complement Accumulator	1	1.75	2-9
012	INV	Invert Accumulator	1	1.75	2-9
013	CAX	Copy Accumulator to Index	1	1.75	2-9
014	CXA	Copy Index to Accumulator	1	1.75	2-9
02	DIN	Direct Input	2	3.5	2-9
03	DOT	Direct Output	2	3.5	2-10
04	IXS	Increment Index and Skip if Greater than Zero	2	3.5	2-10

Appendix B

OP CODES INDEX OF INSTRUCTIONS (CONT.)

Op Code	Mnemonic	Operation Name	Number of Cycles	Time in μs	Page
05	DXS	Decrement Index and Skip if Less than Zero	2	3.5	2-10
06	LLB	Load Literal Byte	1	1.75	2-10
07	CLB	Compare Literal Byte	1	1.75	2-11
080	SAZ	Skip on Accumulator Zero	1	1.75	2-11
081	SAP	Skip on Accumulator Plus	1	1.75	2-11
082	SAM	Skip on Accumulator Minus	1	1.75	2-11
083	SAO	Skip on Accumulator Odd	1	1.75	2-12
084	SLS	Skip on Compare Less	1	1.75	2-12
085	SXE	Skip on Index Even	1	1.75	2-12
086	SEQ	Skip on Compare Equal	1	1.75	2-12
087	SNE	Skip on Compare Not Equal	1	1.75	2-13
088	SGR	Skip on Compare Greater	1	1.75	2-13
089	SLE	Skip on Compare Less or Equal	1	1.75	2-13
08A	SNO	Skip on No Overflow	1	1.75	2-13
08B	SSE	Skip on Sense External False	1	1.75	2-14
08C	SS0	Skip on Sense Switch 0 False	1	1.75	2-14
08D	SS1	Skip on Sense Switch 1 False	1	1.75	2-14
08E	SS2	Skip on Sense Switch 2 False	1	1.75	2-14
08F	SS3	Skip on Sense Switch 3 False	1	1.75	2-14
090	SRA	Shift Right Arithmetic	2-5	3.5 - 8.75	2-15
091	SLA	Shift Left Arithmetic	2-5	3.5 - 8.75	2-15
092	SRA D	Shift Right Arithmetic Double	2-5	3.5 - 8.75	2-15
093	SLA D	Shift Left Arithmetic Double	2-5	3.5 - 8.75	2-16
0A0	SRL	Shift Right Logical	2-5	3.5 - 8.75	2-16
0A1	SLL	Shift Left Logical	2-5	3.5 - 8.75	2-16
0A2	SRL D	Shift Right Logical Double	2-5	3.5 - 8.75	2-16
0A3	SLL D	Shift Left Logical Double	2-5	3.5 - 8.75	2-17
0A4	SRC	Shift Right Circular	2-5	3.5 - 8.75	2-17
0A5	SLC	Shift Left Circular	2-5	3.5 - 8.75	2-17
0A6	SRC D	Shift Right Circular Double	2-5	3.5 - 8.75	2-17

OP CODES INDEX OF INSTRUCTIONS (CONT.)

Op Code	Mnemonic	Operation Name	Number of Cycles	Time in μs	Page
0A7	SLC D	Shift Left Circular Double	2-5	3.5 - 8.75	2-17
0A8	SRL L	Shift Right Logical Left Byte	2-5	3.5 - 8.75	2-18
0A9	SLL L	Shift Left Logical Left Byte	2-5	3.5 - 8.75	2-18
0AA	SRL R	Shift Right Logical Right Byte	2-5	3.5 - 8.75	2-18
0AB	SLL R	Shift Left Logical Right Byte	2-5	3.5 - 8.75	2-18
0AC	SRC L	Shift Right Circular Left Byte	2-5	3.5 - 8.75	2-19
0AD	SLC L	Shift Left Circular Left Byte	2-5	3.5 - 8.75	2-19
0AE	SRC R	Shift Right Circular Right Byte	2-5	3.5 - 8.75	2-19
0AF	SLC R	Shift Left Circular Right Byte	2-5	3.5 - 8.75	2-19

Appendix C

POWERS OF 2 AND 16

2^n and 16^m	m	n	2^{-n} and 16^{-m}
1	0	0	1.0
2		1	0.5
4		2	0.25
8		3	0.125
16	1	4	0.062 5
32		5	0.031 25
64		6	0.015 625
128		7	0.007 812 5
256	2	8	0.003 906 25
512		9	0.001 953 125
1 024		10	0.000 976 562 5
2 048		11	0.000 488 281 25
4 096	3	12	0 000 244 140 625
8 192		13	0 000 122 070 312 5
16 384		14	0 000 061 035 156 25
32 768		15	0 000 030 517 578 125
65 536	4	16	0 000 015 258 789 062 5
131 072		17	0 000 007 629 394 531 25
262 144		18	0 000 003 814 697 265 625
524 288		19	0 000 001 907 348 632 812 5
1 048 576	5	20	0 000 000 953 674 316 406 25
2 097 152		21	0 000 000 476 837 158 203 125
4 194 304		22	0 000 000 238 418 579 101 562 5
8 388 608		23	0 000 000 119 209 289 550 781 25
16 777 216	6	24	0 000 000 059 604 644 775 390 625
33 554 432		25	0 000 000 029 802 322 387 695 312 5
67 108 864		26	0 000 000 014 901 161 193 847 656 25
134 217 728		27	0 000 000 007 450 580 596 923 828 125
268 435 456	7	28	0 000 000 003 725 290 298 461 914 062 5
536 870 912		29	0 000 000 001 862 645 149 230 957 031 25
1 073 741 824		30	0 000 000 000 931 322 574 615 478 515 625
2 147 483 648		31	0 000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	8	32	0 000 000 000 232 830 643 653 869 628 906 25
8 589 934 592		33	0 000 000 000 116 415 321 826 934 814 453 125
17 179 869 184		34	0 000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368		35	0 000 000 000 029 103 830 456 733 703 613 281 25
68 719 476 736	9	36	0 000 000 000 014 551 915 228 366 851 806 640 625
137 438 953 472		37	0 000 000 000 007 275 957 614 183 425 903 320 312 5
274 877 906 944		38	0 000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888		39	0 000 000 000 001 818 989 403 545 856 475 830 078 125
1 099 511 627 776	10	40	0.000 000 000 000 909 494 701 772 928 237 915 039 062 5
2 199 023 255 552		41	0.000 000 000 000 454 747 350 886 464 118 957 519 531 25
4 398 046 511 104		42	0.000 000 000 000 227 373 675 443 232 059 478 759 765 625
8 796 093 022 208		43	0.000 000 000 000 113 686 837 721 616 029 739 379 882 812 5
17 592 186 044 416	11	44	0.000 000 000 000 056 843 418 860 808 014 869 689 941 406 25
35 184 372 088 832		45	0.000 000 000 000 028 421 709 430 404 007 434 844 970 703 125
70 368 744 177 664		46	0.000 000 000 000 014 210 854 715 202 003 717 422 485 351 562 5
140 737 488 355 328		47	0.000 000 000 000 007 105 427 357 601 001 858 711 242 675 781 25
281 474 976 710 656	12	48	0.000 000 000 000 003 552 713 678 800 500 929 355 621 337 890 625

Appendix D

MISCELLANEOUS REFERENCE DATA

COMMON CONSTANTS		
	DECIMAL	HEX
e	2.718 281 828 5	2.B7E1 5163
1/e	.367 879 441 2	0.5E2D 58D9
$\log_{10} e$	.434 294 481 9	0.6F2D EC55
$\log_e 10$	2.302 585 093 0	2.4D76 3777
$\log_e 2$	.693 147 180 6	0.B172 17F8
$\log_{10} \pi$	.497 149 872 7	0.7F45 36CC
$\log_e \pi$	1.144 729 885 8	1.250D 048E
π	3.141 592 653 6	3.243F 6A89
$1/\pi$	.318 309 886 2	0.517C C1B7
$\sqrt{\pi}$	1.7 724 538 509	1.C5BF 891C
γ	0.5 772 156 649	0.93C4 67E4
$\log_e \gamma$	-0.5 495 393 129	-0.8CAE 9BC3

FACTORIALS		
	DECIMAL	HEX
1!	1	001
2!	2	002
3!	6	006
4!	24	018
5!	120	078
6!	720	2D0
7!	5 040	1 3B0
8!	40 320	9 D80
9!	362 880	58 980
10!	3 628 800	375 EBA
11!	39 916 800	2 611 500
12!	479 001 600	1B 8CF C00
13!	6 227 020 800	173 291 A20
14!	87 178 291 200	1 44C 3B2 800

RECIPROCALS		
n	1/n (DECIMAL)	1/n (HEXADECIMAL)
2	+.5000000000	+.800000000
3	+.3333333333	+.555555555
4	+.2500000000	+.400000000
5	+.2000000000	+.333333333
6	+.1666666667	+.2AAAAAAAA
7	+.1428571428	+.249249249
8	+.1250000000	+.200000000
9	+.1111111111	+.1C71C71C7
10	+.1000000000	+.199999999
11	+.0909090909	+.1745D1745
12	+.0833333333	+.155555555
13	+.0769230769	+.13B13B13B
14	+.0714285714	+.124924924
15	+.0666666667	+.111111111
16	+.0625000000	+.100000000
17	+.0588235294	+.0F0F0F0F0
18	+.0555555555	+.0E38E38E3
19	+.0526315789	+.0D79435E5
20	+.0500000000	+.0CCCCCCCC
21	+.0476190476	+.0C30C30C3
22	+.0454545454	+.0BA2E8BA2
23	+.0434782609	+.0B21642C8
24	+.0416666667	+.0AAAAAAAA
25	+.0400000000	+.0A3D70A3D
26	+.0384615384	+.09D89D89D
27	+.0370370370	+.097B425ED
28	+.0357142857	+.092492492
29	+.0344827586	+.08D3DCB08
30	+.0333333333	+.088888888

SQUARE ROOTS		
	DECIMAL	HEX
$\sqrt{2}$	1.414 213 562 4	1.6A0 9E6 681
$\sqrt{3}$	1.732 050 807 6	1.BB6 7AE 85A
$\sqrt{5}$	2.236 067 977 5	2.3C6 EF3 730
$\sqrt{6}$	2.449 489 742 8	2. 731 1C2 813
$\sqrt{7}$	2.645 751 311 1	2. A54 FF5 3A8
$\sqrt{8}$	2.828 427 124 8	2. D41 3CC D02
$\sqrt{10}$	3.162 277 660 2	3. 298 B07 5B7

MISCELLANEOUS CONSTANTS			
		DECIMAL	HEX
1° = 1/360 of a circle		0.002 777 777 8	0.00B60B
1° = .017 453 292 5 radians		0.017 453 292 5	0.0477D1
Euler's Constant	y =	0.577 215 664 9	0.93C467

Appendix E

HEXADECIMAL - TO - DECIMAL CONVERSION

GENERAL

This appendix contains Hexadecimal-To-Decimal conversion tables for positive numbers, negative numbers, and fractions. Conversion of binary numbers to decimal or hexadecimal and conversion of hexadecimal numbers to decimal are also discussed.

BINARY NUMBER CONVERSION TO DECIMAL

Prior to explaining the specifics of the number systems, observe the following basics of number systems.

Any positional number system can be defined by its base (radix). The base is the number of unique symbols that can occupy a position in the number system. As an example, the decimal system has a base of 10 because symbols (numbers in this case) 0, 1, 2, 3, 4, 5, 6, 7, 8, and 9 can occupy a position in the number system. In the binary system, there are two symbols, 0 and 1, that can occupy a position. Therefore, a binary system is base 2. In the hexadecimal system, symbols 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F can occupy a position in the number system. Therefore, it is a base 16 system. In converting from binary or hexadecimal to decimal, the symbol represents a coefficient, and, its position in the number, the exponent of the base -- examples of this are given below.

DECIMAL NUMBER SYSTEM

Given a decimal number of 159, state it as a function of its base.

The number 159 can be restated as 100 plus 50 plus 9 or:

$$1\,(10^2) + 5\,(10^1) + 9\,(10^0) = 159$$

BINARY NUMBER SYSTEM

Given the binary number 1011, convert it to decimal.

$$1\,(2^3) + 0\,(2^2) + 1\,(2^1) + 1\,(2^0) = 11$$

Given the binary numbers 0 through 15, convert them to hexadecimal numbers.

Binary-to-Hexadecimal Conversion Table		
Binary	Hexadecimal	Decimal
0000	0	0
0001	1	1
0010	2	2
0011	3	3
0100	4	4
0101	5	5
0110	6	6
0111	7	7
1000	8	8
1001	9	9
1010	A	10
1011	B	11
1100	C	12
1101	D	13
1110	E	14
1111	F	15

HEXADECIMAL NUMBER SYSTEM

Given the hexadecimal number 4F2, convert it to decimal. (For the conversion of F refer to the table under the Binary Number System).

$$4\,(16^2) + F\,(16^1) + 2\,(16^0) = 4\,(256) + 15\,(16) + 2\,(1) = 1266$$

Note that the exponent for the base was determined (in all cases) by counting from the right, the symbols position in the number.

INTEGER TABLE EXTENSION

For numbers outside the range of the integer table add the following values to those of the Hexadecimal to Positive Decimal Integer table.

Hexadecimal	Decimal
1000	4096
2000	8192
3000	12288
4000	16384
5000	20480
6000	24576
7000	28672
8000	32768
9000	36864
A000	40960
B000	45056
C000	49152
D000	53248
E000	57344
F000	61440

HEXADECIMAL - TO - POSITIVE INTEGER CONVERSION TABLE

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
010	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
020	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
030	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
040	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
050	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
060	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
070	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
080	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
090	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
0A0	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175
0B0	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
0C0	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207
0D0	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
0E0	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
0F0	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
100	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271
110	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287
120	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303
130	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319
140	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335
150	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351
160	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367
170	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383
180	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399
190	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415
1A0	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431
1B0	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447
1C0	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463
1D0	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479
1E0	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495
1F0	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511
200	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527
210	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543
220	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559
230	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575
240	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591
250	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607
260	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623
270	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639
280	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655
290	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671
2A0	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687
2B0	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703
2C0	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719
2D0	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735
2E0	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751
2F0	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767
300	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783
310	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799
320	800	801	802	803	804	805	806	807	808	809	810	811	812	813	814	815
330	816	817	818	819	820	821	822	823	824	825	826	827	828	829	830	831
340	832	833	834	835	836	837	838	839	840	841	842	843	844	845	846	847
350	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863
360	864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879
370	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895
380	896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911
390	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927
3A0	928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943
3B0	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959
3C0	960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975
3D0	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991
3E0	992	993	994	995	996	997	998	999	1000	1001	1002	1003	1004	1005	1006	1007
3F0	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023

HEXADECIMAL - TO - POSITIVE INTEGER CONVERSION TABLE (CONT.)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
400	1024	1025	1026	1027	1028	1029	1030	1031	1032	1033	1034	1035	1036	1037	1038	1039
410	1040	1041	1042	1043	1044	1045	1046	1047	1048	1049	1050	1051	1052	1053	1054	1055
420	1056	1057	1058	1059	1060	1061	1062	1063	1064	1065	1066	1067	1068	1069	1070	1071
430	1072	1073	1074	1075	1076	1077	1078	1079	1080	1081	1082	1083	1084	1085	1086	1087
440	1088	1089	1090	1091	1092	1093	1094	1095	1096	1097	1098	1099	1100	1101	1102	1103
450	1104	1105	1106	1107	1108	1109	1110	1111	1112	1113	1114	1115	1116	1117	1118	1119
460	1120	1121	1122	1123	1124	1125	1126	1127	1128	1129	1130	1131	1132	1133	1134	1135
470	1136	1137	1138	1139	1140	1141	1142	1143	1144	1145	1146	1147	1148	1149	1150	1151
480	1152	1153	1154	1155	1156	1157	1158	1159	1160	1161	1162	1163	1164	1165	1166	1167
490	1168	1169	1170	1171	1172	1173	1174	1175	1176	1177	1178	1179	1180	1181	1182	1183
4A0	1184	1185	1186	1187	1188	1189	1190	1191	1192	1193	1194	1195	1196	1197	1198	1199
4B0	1200	1201	1202	1203	1204	1205	1206	1207	1208	1209	1210	1211	1212	1213	1214	1215
4C0	1216	1217	1218	1219	1220	1221	1222	1223	1224	1225	1226	1227	1228	1229	1230	1231
4D0	1232	1233	1234	1235	1236	1237	1238	1239	1240	1241	1242	1243	1244	1245	1246	1247
4E0	1248	1249	1250	1251	1252	1253	1254	1255	1256	1257	1258	1259	1260	1261	1262	1263
4F0	1264	1265	1266	1267	1268	1269	1270	1271	1272	1273	1274	1275	1276	1277	1278	1279
500	1280	1281	1282	1283	1284	1285	1286	1287	1288	1289	1290	1291	1292	1293	1294	1295
510	1296	1297	1298	1299	1300	1301	1302	1303	1304	1305	1306	1307	1308	1309	1310	1311
520	1312	1313	1314	1315	1316	1317	1318	1319	1320	1321	1322	1323	1324	1325	1326	1327
530	1328	1329	1330	1331	1332	1333	1334	1335	1336	1337	1338	1339	1340	1341	1342	1343
540	1344	1345	1346	1347	1348	1349	1350	1351	1352	1353	1354	1355	1356	1357	1358	1359
550	1360	1361	1362	1363	1364	1365	1366	1367	1368	1369	1370	1371	1372	1373	1374	1375
560	1376	1377	1378	1379	1380	1381	1382	1383	1384	1385	1386	1387	1388	1389	1390	1391
570	1392	1393	1394	1395	1396	1397	1398	1399	1400	1401	1402	1403	1404	1405	1406	1407
580	1408	1409	1410	1411	1412	1413	1414	1415	1416	1417	1418	1419	1420	1421	1422	1423
590	1424	1425	1426	1427	1428	1429	1430	1431	1432	1433	1434	1435	1436	1437	1438	1439
5A0	1440	1441	1442	1443	1444	1445	1446	1447	1448	1449	1450	1451	1452	1453	1454	1455
5B0	1456	1457	1458	1459	1460	1461	1462	1463	1464	1465	1466	1467	1468	1469	1470	1471
5C0	1472	1473	1474	1475	1476	1477	1478	1479	1480	1481	1482	1483	1484	1485	1486	1487
5D0	1488	1489	1490	1491	1492	1493	1494	1495	1496	1497	1498	1499	1500	1501	1502	1503
5E0	1504	1505	1506	1507	1508	1509	1510	1511	1512	1513	1514	1515	1516	1517	1518	1519
5F0	1520	1521	1522	1523	1524	1525	1526	1527	1528	1529	1530	1531	1532	1533	1534	1535
600	1536	1537	1538	1539	1540	1541	1542	1543	1544	1545	1546	1547	1548	1549	1550	1551
610	1552	1553	1554	1555	1556	1557	1558	1559	1560	1561	1562	1563	1564	1565	1566	1567
620	1568	1569	1570	1571	1572	1573	1574	1575	1576	1577	1578	1579	1580	1581	1582	1583
630	1584	1585	1586	1587	1588	1589	1590	1591	1592	1593	1594	1595	1596	1597	1598	1599
640	1600	1601	1602	1603	1604	1605	1606	1607	1608	1609	1610	1611	1612	1613	1614	1615
650	1616	1617	1618	1619	1620	1621	1622	1623	1624	1625	1626	1627	1628	1629	1630	1631
660	1632	1633	1634	1635	1636	1637	1638	1639	1640	1641	1642	1643	1644	1645	1646	1647
670	1648	1649	1650	1651	1652	1653	1654	1655	1656	1657	1658	1659	1660	1661	1662	1663
680	1664	1665	1666	1667	1668	1669	1670	1671	1672	1673	1674	1675	1676	1677	1678	1679
690	1680	1681	1682	1683	1684	1685	1686	1687	1688	1689	1690	1691	1692	1693	1694	1695
6A0	1696	1697	1698	1699	1700	1701	1702	1703	1704	1705	1706	1707	1708	1709	1710	1711
6B0	1712	1713	1714	1715	1716	1717	1718	1719	1720	1721	1722	1723	1724	1725	1726	1727
6C0	1728	1729	1730	1731	1732	1733	1734	1735	1736	1737	1738	1739	1740	1741	1742	1743
6D0	1744	1745	1746	1747	1748	1749	1750	1751	1752	1753	1754	1755	1756	1757	1758	1759
6E0	1760	1761	1762	1763	1764	1765	1766	1767	1768	1769	1770	1771	1772	1773	1774	1775
6F0	1776	1777	1778	1779	1780	1781	1782	1783	1784	1785	1786	1787	1788	1789	1790	1791
700	1792	1793	1794	1795	1796	1797	1798	1799	1800	1801	1802	1803	1804	1805	1806	1807
710	1808	1809	1810	1811	1812	1813	1814	1815	1816	1817	1818	1819	1820	1821	1822	1823
720	1824	1825	1826	1827	1828	1829	1830	1831	1832	1833	1834	1835	1836	1837	1838	1839
730	1840	1841	1842	1843	1844	1845	1846	1847	1848	1849	1850	1851	1852	1853	1854	1855
740	1856	1857	1858	1859	1860	1861	1862	1863	1864	1865	1866	1867	1868	1869	1870	1871
750	1872	1873	1874	1875	1876	1877	1878	1879	1880	1881	1882	1883	1884	1885	1886	1887
760	1888	1889	1890	1891	1892	1893	1894	1895	1896	1897	1898	1899	1900	1901	1902	1903
770	1904	1905	1906	1907	1908	1909	1910	1911	1912	1913	1914	1915	1916	1917	1918	1919
780	1920	1921	1922	1923	1924	1925	1926	1927	1928	1929	1930	1931	1932	1933	1934	1935
790	1936	1937	1938	1939	1940	1941	1942	1943	1944	1945	1946	1947	1948	1949	1950	1951
7A0	1952	1953	1954	1955	1956	1957	1958	1959	1960	1961	1962	1963	1964	1965	1966	1967
7B0	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983
7C0	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999
7D0	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015
7E0	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
7F0	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047

HEXADECIMAL - TO - POSITIVE INTEGER CONVERSION TABLE (CONT.)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
800	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063
810	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079
820	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095
830	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111
840	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127
850	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143
860	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159
870	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175
880	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191
890	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207
8A0	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223
8B0	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239
8C0	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255
8D0	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271
8E0	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287
8F0	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303
900	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319
910	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335
920	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351
930	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367
940	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383
950	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399
960	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415
970	2416	2417	2418	2419	2420	2421	2422	2423	2424	2425	2426	2427	2428	2429	2430	2431
980	2432	2433	2434	2435	2436	2437	2438	2439	2440	2441	2442	2443	2444	2445	2446	2447
990	2448	2449	2450	2451	2452	2453	2454	2455	2456	2457	2458	2459	2460	2461	2462	2463
9A0	2464	2465	2466	2467	2468	2469	2470	2471	2472	2473	2474	2475	2476	2477	2478	2479
9B0	2480	2481	2482	2483	2484	2485	2486	2487	2488	2489	2490	2491	2492	2493	2494	2495
9C0	2496	2497	2498	2499	2500	2501	2502	2503	2504	2505	2506	2507	2508	2509	2510	2511
9D0	2512	2513	2514	2515	2516	2517	2518	2519	2520	2521	2522	2523	2524	2525	2526	2527
9E0	2528	2529	2530	2531	2532	2533	2534	2535	2536	2537	2538	2539	2540	2541	2542	2543
9F0	2544	2545	2546	2547	2548	2549	2550	2551	2552	2553	2554	2555	2556	2557	2558	2559
A00	2560	2561	2562	2563	2564	2565	2566	2567	2568	2569	2570	2571	2572	2573	2574	2575
A10	2576	2577	2578	2579	2580	2581	2582	2583	2584	2585	2586	2587	2588	2589	2590	2591
A20	2592	2593	2594	2595	2596	2597	2598	2599	2600	2601	2602	2603	2604	2605	2606	2607
A30	2608	2609	2610	2611	2612	2613	2614	2615	2616	2617	2618	2619	2620	2621	2622	2623
A40	2624	2625	2626	2627	2628	2629	2630	2631	2632	2633	2634	2635	2636	2637	2638	2639
A50	2640	2641	2642	2643	2644	2645	2646	2647	2648	2649	2650	2651	2652	2653	2654	2655
A60	2656	2657	2658	2659	2660	2661	2662	2663	2664	2665	2666	2667	2668	2669	2670	2671
A70	2672	2673	2674	2675	2676	2677	2678	2679	2680	2681	2682	2683	2684	2685	2686	2687
A80	2688	2689	2690	2691	2692	2693	2694	2695	2696	2697	2698	2699	2700	2701	2702	2703
A90	2704	2705	2706	2707	2708	2709	2710	2711	2712	2713	2714	2715	2716	2717	2718	2719
AA0	2720	2721	2722	2723	2724	2725	2726	2727	2728	2729	2730	2731	2732	2733	2734	2735
AB0	2736	2737	2738	2739	2740	2741	2742	2743	2744	2745	2746	2747	2748	2749	2750	2751
AC0	2752	2753	2754	2755	2756	2757	2758	2759	2760	2761	2762	2763	2764	2765	2766	2767
AD0	2768	2769	2770	2771	2772	2773	2774	2775	2776	2777	2778	2779	2780	2781	2782	2783
AE0	2784	2785	2786	2787	2788	2789	2790	2791	2792	2793	2794	2795	2796	2797	2798	2799
AF0	2800	2801	2802	2803	2804	2805	2806	2807	2808	2809	2810	2811	2812	2813	2814	2815
B00	2816	2817	2818	2819	2820	2821	2822	2823	2824	2825	2826	2827	2828	2829	2830	2831
B10	2832	2833	2834	2835	2836	2837	2838	2839	2840	2841	2842	2843	2844	2845	2846	2847
B20	2848	2849	2850	2851	2852	2853	2854	2855	2856	2857	2858	2859	2860	2861	2862	2863
B30	2864	2865	2866	2867	2868	2869	2870	2871	2872	2873	2874	2875	2876	2877	2878	2879
B40	2880	2881	2882	2883	2884	2885	2886	2887	2888	2889	2890	2891	2892	2893	2894	2895
B50	2896	2897	2898	2899	2900	2901	2902	2903	2904	2905	2906	2907	2908	2909	2910	2911
B60	2912	2913	2914	2915	2916	2917	2918	2919	2920	2921	2922	2923	2924	2925	2926	2927
B70	2928	2929	2930	2931	2932	2933	2934	2935	2936	2937	2938	2939	2940	2941	2942	2943
B80	2944	2945	2946	2947	2948	2949	2950	2951	2952	2953	2954	2955	2956	2957	2958	2959
B90	2960	2961	2962	2963	2964	2965	2966	2967	2968	2969	2970	2971	2972	2973	2974	2975
BA0	2976	2977	2978	2979	2980	2981	2982	2983	2984	2985	2986	2987	2988	2989	2990	2991
BB0	2992	2993	2994	2995	2996	2997	2998	2999	3000	3001	3002	3003	3004	3005	3006	3007
BC0	3008	3009	3010	3011	3012	3013	3014	3015	3016	3017	3018	3019	3020	3021	3022	3023
BD0	3024	3025	3026	3027	3028	3029	3030	3031	3032	3033	3034	3035	3036	3037	3038	3039
BE0	3040	3041	3042	3043	3044	3045	3046	3047	3048	3049	3050	3051	3052	3053	3054	3055
BF0	3056	3057	3058	3059	3060	3061	3062	3063	3064	3065	3066	3067	3068	3069	3070	3071

HEXADECIMAL - TO - POSITIVE INTEGER CONVERSION TABLE (CONT.)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
C00	3072	3073	3074	3075	3076	3077	3078	3079	3080	3081	3082	3083	3084	3085	3086	3087
C10	3088	3089	3090	3091	3092	3093	3094	3095	3096	3097	3098	3099	3100	3101	3102	3103
C20	3104	3105	3106	3107	3108	3109	3110	3111	3112	3113	3114	3115	3116	3117	3118	3119
C30	3120	3121	3122	3123	3124	3125	3126	3127	3128	3129	3130	3131	3132	3133	3134	3135
C40	3136	3137	3138	3139	3140	3141	3142	3143	3144	3145	3146	3147	3148	3149	3150	3151
C50	3152	3153	3154	3155	3156	3157	3158	3159	3160	3161	3162	3163	3164	3165	3166	3167
C60	3168	3169	3170	3171	3172	3173	3174	3175	3176	3177	3178	3179	3180	3181	3182	3183
C70	3184	3185	3186	3187	3188	3189	3190	3191	3192	3193	3194	3195	3196	3197	3198	3199
C80	3200	3201	3202	3203	3204	3205	3206	3207	3208	3209	3210	3211	3212	3213	3214	3215
C90	3216	3217	3218	3219	3220	3221	3222	3223	3224	3225	3226	3227	3228	3229	3230	3231
CA0	3232	3233	3234	3235	3236	3237	3238	3239	3240	3241	3242	3243	3244	3245	3246	3247
CB0	3248	3249	3250	3251	3252	3253	3254	3255	3256	3257	3258	3259	3260	3261	3262	3263
CC0	3264	3265	3266	3267	3268	3269	3270	3271	3272	3273	3274	3275	3276	3277	3278	3279
CD0	3280	3281	3282	3283	3284	3285	3286	3287	3288	3289	3290	3291	3292	3293	3294	3295
CE0	3296	3297	3298	3299	3300	3301	3302	3303	3304	3305	3306	3307	3308	3309	3310	3311
CF0	3312	3313	3314	3315	3316	3317	3318	3319	3320	3321	3322	3323	3324	3325	3326	3327
D00	3328	3329	3330	3331	3332	3333	3334	3335	3336	3337	3338	3339	3340	3341	3342	3343
D10	3344	3345	3346	3347	3348	3349	3350	3351	3352	3353	3354	3355	3356	3357	3358	3359
D20	3360	3361	3362	3363	3364	3365	3366	3367	3368	3369	3370	3371	3372	3373	3374	3375
D30	3376	3377	3378	3379	3380	3381	3382	3383	3384	3385	3386	3387	3388	3389	3390	3391
D40	3392	3393	3394	3395	3396	3397	3398	3399	3400	3401	3402	3403	3404	3405	3406	3407
D50	3408	3409	3410	3411	3412	3413	3414	3415	3416	3417	3418	3419	3420	3421	3422	3423
D60	3424	3425	3426	3427	3428	3429	3430	3431	3432	3433	3434	3435	3436	3437	3438	3439
D70	3440	3441	3442	3443	3444	3445	3446	3447	3448	3449	3450	3451	3452	3453	3454	3455
D80	3456	3457	3458	3459	3460	3461	3462	3463	3464	3465	3466	3467	3468	3469	3470	3471
D90	3472	3473	3474	3475	3476	3477	3478	3479	3480	3481	3482	3483	3484	3485	3486	3487
DA0	3488	3489	3490	3491	3492	3493	3494	3495	3496	3497	3498	3499	3500	3501	3502	3503
DB0	3504	3505	3506	3507	3508	3509	3510	3511	3512	3513	3514	3515	3516	3517	3518	3519
DC0	3520	3521	3522	3523	3524	3525	3526	3527	3528	3529	3530	3531	3532	3533	3534	3535
DD0	3536	3537	3538	3539	3540	3541	3542	3543	3544	3545	3546	3547	3548	3549	3550	3551
DE0	3552	3553	3554	3555	3556	3557	3558	3559	3560	3561	3562	3563	3564	3565	3566	3567
DF0	3568	3569	3570	3571	3572	3573	3574	3575	3576	3577	3578	3579	3580	3581	3582	3583
E00	3584	3585	3586	3587	3588	3589	3590	3591	3592	3593	3594	3595	3596	3597	3598	3599
E10	3600	3601	3602	3603	3604	3605	3606	3607	3608	3609	3610	3611	3612	3613	3614	3615
E20	3616	3617	3618	3619	3620	3621	3622	3623	3624	3625	3626	3627	3628	3629	3630	3631
E30	3632	3633	3634	3635	3636	3637	3638	3639	3640	3641	3642	3643	3644	3645	3646	3647
E40	3648	3649	3650	3651	3652	3653	3654	3655	3656	3657	3658	3659	3660	3661	3662	3663
E50	3664	3665	3666	3667	3668	3669	3670	3671	3672	3673	3674	3675	3676	3677	3678	3679
E60	3680	3681	3682	3683	3684	3685	3686	3687	3688	3689	3690	3691	3692	3693	3694	3695
E70	3696	3697	3698	3699	3700	3701	3702	3703	3704	3705	3706	3707	3708	3709	3710	3711
E80	3712	3713	3714	3715	3716	3717	3718	3719	3720	3721	3722	3723	3724	3725	3726	3727
E90	3728	3729	3730	3731	3732	3733	3734	3735	3736	3737	3738	3739	3740	3741	3742	3743
EA0	3744	3745	3746	3747	3748	3749	3750	3751	3752	3753	3754	3755	3756	3757	3758	3759
EB0	3760	3761	3762	3763	3764	3765	3766	3767	3768	3769	3770	3771	3772	3773	3774	3775
EC0	3776	3777	3778	3779	3780	3781	3782	3783	3784	3785	3786	3787	3788	3789	3790	3791
ED0	3792	3793	3794	3795	3796	3797	3798	3799	3800	3801	3802	3803	3804	3805	3806	3807
EE0	3808	3809	3810	3811	3812	3813	3814	3815	3816	3817	3818	3819	3820	3821	3822	3823
EF0	3824	3825	3826	3827	3828	3829	3830	3831	3832	3833	3834	3835	3836	3837	3838	3839
F00	3840	3841	3842	3843	3844	3845	3846	3847	3848	3849	3850	3851	3852	3853	3854	3855
F10	3856	3857	3858	3859	3860	3861	3862	3863	3864	3865	3866	3867	3868	3869	3870	3871
F20	3872	3873	3874	3875	3876	3877	3878	3879	3880	3881	3882	3883	3884	3885	3886	3887
F30	3888	3889	3890	3891	3892	3893	3894	3895	3896	3897	3898	3899	3900	3901	3902	3903
F40	3904	3905	3906	3907	3908	3909	3910	3911	3912	3913	3914	3915	3916	3917	3918	3919
F50	3920	3921	3922	3923	3924	3925	3926	3927	3928	3929	3930	3931	3932	3933	3934	3935
F60	3936	3937	3938	3939	3940	3941	3942	3943	3944	3945	3946	3947	3948	3949	3950	3951
F70	3952	3953	3954	3955	3956	3957	3958	3959	3960	3961	3962	3963	3964	3965	3966	3967
F80	3968	3969	3970	3971	3972	3973	3974	3975	3976	3977	3978	3979	3980	3981	3982	3983
F90	3984	3985	3986	3987	3988	3989	3990	3991	3992	3993	3994	3995	3996	3997	3998	3999
FA0	4000	4001	4002	4003	4004	4005	4006	4007	4008	4009	4010	4011	4012	4013	4014	4015
FB0	4016	4017	4018	4019	4020	4021	4022	4023	4024	4025	4026	4027	4028	4029	4030	4031
FC0	4032	4033	4034	4035	4036	4037	4038	4039	4040	4041	4042	4043	4044	4045	4046	4047
FD0	4048	4049	4050	4051	4052	4053	4054	4055	4056	4057	4058	4059	4060	4061	4062	4063
FE0	4064	4065	4066	4067	4068	4069	4070	4071	4072	4073	4074	4075	4076	4077	4078	4079
FF0	4080	4081	4082	4083	4084	4085	4086	4087	4088	4089	4090	4091	4092	4093	4094	4095

HEXADECIMAL - TO - NEGATIVE INTEGER CONVERSION TABLE

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
FFF0	-1	-2	-3	-4	-5	-6	-7	-8	-9	-10	-11	-12	-13	-14	-15	-16
FFE0	-17	-18	-19	-20	-21	-22	-23	-24	-25	-26	-27	-28	-29	-30	-31	-32
FFD0	-33	-34	-35	-36	-37	-38	-39	-40	-41	-42	-43	-44	-45	-46	-47	-48
FFC0	-49	-50	-51	-52	-53	-54	-55	-56	-57	-58	-59	-60	-61	-62	-63	-64
FFB0	-65	-66	-67	-68	-69	-70	-71	-72	-73	-74	-75	-76	-77	-78	-79	-80
FFA0	-81	-82	-83	-84	-85	-86	-87	-88	-89	-90	-91	-92	-93	-94	-95	-96
FF90	-97	-98	-99	-100	-101	-102	-103	-104	-105	-106	-107	-108	-109	-110	-111	-112
FF80	-113	-114	-115	-116	-117	-118	-119	-120	-121	-122	-123	-124	-125	-126	-127	-128
FF70	-129	-130	-131	-132	-133	-134	-135	-136	-137	-138	-139	-140	-141	-142	-143	-144
FF60	-145	-146	-147	-148	-149	-150	-151	-152	-153	-154	-155	-156	-157	-158	-159	-160
FF50	-161	-162	-163	-164	-165	-166	-167	-168	-169	-170	-171	-172	-173	-174	-175	-176
FF40	-177	-178	-179	-180	-181	-182	-183	-184	-185	-186	-187	-188	-189	-190	-191	-192
FF30	-193	-194	-195	-196	-197	-198	-199	-200	-201	-202	-203	-204	-205	-206	-207	-208
FF20	-209	-210	-211	-212	-213	-214	-215	-216	-217	-218	-219	-220	-221	-222	-223	-224
FF10	-225	-226	-227	-228	-229	-230	-231	-232	-233	-234	-235	-236	-237	-238	-239	-240
FF00	-241	-242	-243	-244	-245	-246	-247	-248	-249	-250	-251	-252	-253	-254	-255	-256
FEF0	-257	-258	-259	-260	-261	-262	-263	-264	-265	-266	-267	-268	-269	-270	-271	-272
FEE0	-273	-274	-275	-276	-277	-278	-279	-280	-281	-282	-283	-284	-285	-286	-287	-288
FED0	-289	-290	-291	-292	-293	-294	-295	-296	-297	-298	-299	-300	-301	-302	-303	-304
FEC0	-305	-306	-307	-308	-309	-310	-311	-312	-313	-314	-315	-316	-317	-318	-319	-320
FEB0	-321	-322	-323	-324	-325	-326	-327	-328	-329	-330	-331	-332	-333	-334	-335	-336
FEA0	-337	-338	-339	-340	-341	-342	-343	-344	-345	-346	-347	-348	-349	-350	-351	-352
FE90	-353	-354	-355	-356	-357	-358	-359	-360	-361	-362	-363	-364	-365	-366	-367	-368
FE80	-369	-370	-371	-372	-373	-374	-375	-376	-377	-378	-379	-380	-381	-382	-383	-384
FE70	-385	-386	-387	-388	-389	-390	-391	-392	-393	-394	-395	-396	-397	-398	-399	-400
FE60	-401	-402	-403	-404	-405	-406	-407	-408	-409	-410	-411	-412	-413	-414	-415	-416
FE50	-417	-418	-419	-420	-421	-422	-423	-424	-425	-426	-427	-428	-429	-430	-431	-432
FE40	-433	-434	-435	-436	-437	-438	-439	-440	-441	-442	-443	-444	-445	-446	-447	-448
FE30	-449	-450	-451	-452	-453	-454	-455	-456	-457	-458	-459	-460	-461	-462	-463	-464
FE20	-465	-466	-467	-468	-469	-470	-471	-472	-473	-474	-475	-476	-477	-478	-479	-480
FE10	-481	-482	-483	-484	-485	-486	-487	-488	-489	-490	-491	-492	-493	-494	-495	-496
FE00	-497	-498	-499	-500	-501	-502	-503	-504	-505	-506	-507	-508	-509	-510	-511	-512
FDF0	-513	-514	-515	-516	-517	-518	-519	-520	-521	-522	-523	-524	-525	-526	-527	-528
FDE0	-529	-530	-531	-532	-533	-534	-535	-536	-537	-538	-539	-540	-541	-542	-543	-544
FDD0	-545	-546	-547	-548	-549	-550	-551	-552	-553	-554	-555	-556	-557	-558	-559	-560
FDC0	-561	-562	-563	-564	-565	-566	-567	-568	-569	-570	-571	-572	-573	-574	-575	-576
FDB0	-577	-578	-579	-580	-581	-582	-583	-584	-585	-586	-587	-588	-589	-590	-591	-592
FDA0	-593	-594	-595	-596	-597	-598	-599	-600	-601	-602	-603	-604	-605	-606	-607	-608
FD90	-609	-610	-611	-612	-613	-614	-615	-616	-617	-618	-619	-620	-621	-622	-623	-624
FD80	-625	-626	-627	-628	-629	-630	-631	-632	-633	-634	-635	-636	-637	-638	-639	-640
FD70	-641	-642	-643	-644	-645	-646	-647	-648	-649	-650	-651	-652	-653	-654	-655	-656
FD60	-657	-658	-659	-660	-661	-662	-663	-664	-665	-666	-667	-668	-669	-670	-671	-672
FD50	-673	-674	-675	-676	-677	-678	-679	-680	-681	-682	-683	-684	-685	-686	-687	-688
FD40	-689	-690	-691	-692	-693	-694	-695	-696	-697	-698	-699	-700	-701	-702	-703	-704
FD30	-705	-706	-707	-708	-709	-710	-711	-712	-713	-714	-715	-716	-717	-718	-719	-720
FD20	-721	-722	-723	-724	-725	-726	-727	-728	-729	-730	-731	-732	-733	-734	-735	-736
FD10	-737	-738	-739	-740	-741	-742	-743	-744	-745	-746	-747	-748	-749	-750	-751	-752
FD00	-753	-754	-755	-756	-757	-758	-759	-760	-761	-762	-763	-764	-765	-766	-767	-768
FCF0	-769	-770	-771	-772	-773	-774	-775	-776	-777	-778	-779	-780	-781	-782	-783	-784
FCE0	-785	-786	-787	-788	-789	-790	-791	-792	-793	-794	-795	-796	-797	-798	-799	-800
FCD0	-801	-802	-803	-804	-805	-806	-807	-808	-809	-810	-811	-812	-813	-814	-815	-816
FCC0	-817	-818	-819	-820	-821	-822	-823	-824	-825	-826	-827	-828	-829	-830	-831	-832
FCB0	-833	-834	-835	-836	-837	-838	-839	-840	-841	-842	-843	-844	-845	-846	-847	-848
FCA0	-849	-850	-851	-852	-853	-854	-855	-856	-857	-858	-859	-860	-861	-862	-863	-864
FC90	-865	-866	-867	-868	-869	-870	-871	-872	-873	-874	-875	-876	-877	-878	-879	-880
FC80	-881	-882	-883	-884	-885	-886	-887	-888	-889	-890	-891	-892	-893	-894	-895	-896
FC70	-897	-898	-899	-900	-901	-902	-903	-904	-905	-906	-907	-908	-909	-910	-911	-912
FC60	-913	-914	-915	-916	-917	-918	-919	-920	-921	-922	-923	-924	-925	-926	-927	-928
FC50	-929	-930	-931	-932	-933	-934	-935	-936	-937	-938	-939	-940	-941	-942	-943	-944
FC40	-945	-946	-947	-948	-949	-950	-951	-952	-953	-954	-955	-956	-957	-958	-959	-960
FC30	-961	-962	-963	-964	-965	-966	-967	-968	-969	-970	-971	-972	-973	-974	-975	-976
FC20	-977	-978	-979	-980	-981	-982	-983	-984	-985	-986	-987	-988	-989	-990	-991	-992
FC10	-993	-994	-995	-996	-997	-998	-999	-1000	-1001	-1002	-1003	-1004	-1005	-1006	-1007	-1008
FC00	-1009	-1010	-1011	-1012	-1013	-1014	-1015	-1016	-1017	-1018	-1019	-1020	-1021	-1022	-1023	-1024

HEXADECIMAL - TO - NEGATIVE INTEGER CONVERSION TABLE (CONT.)

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
FBF0	-1025	-1026	-1027	-1028	-1029	-1030	-1031	-1032	-1033	-1034	-1035	-1036	-1037	-1038	-1039	-1040
FBE0	-1041	-1042	-1043	-1044	-1045	-1046	-1047	-1048	-1049	-1050	-1051	-1052	-1053	-1054	-1055	-1056
FBD0	-1057	-1058	-1059	-1060	-1061	-1062	-1063	-1064	-1065	-1066	-1067	-1068	-1069	-1070	-1071	-1072
FBC0	-1073	-1074	-1075	-1076	-1077	-1078	-1079	-1080	-1081	-1082	-1083	-1084	-1085	-1086	-1087	-1088
FBB0	-1089	-1090	-1091	-1092	-1093	-1094	-1095	-1096	-1097	-1098	-1099	-1100	-1101	-1102	-1103	-1104
FBA0	-1105	-1106	-1107	-1108	-1109	-1110	-1111	-1112	-1113	-1114	-1115	-1116	-1117	-1118	-1119	-1120
FB90	-1121	-1122	-1123	-1124	-1125	-1126	-1127	-1128	-1129	-1130	-1131	-1132	-1133	-1134	-1135	-1136
FB80	-1137	-1138	-1139	-1140	-1141	-1142	-1143	-1144	-1145	-1146	-1147	-1148	-1149	-1150	-1151	-1152
FB70	-1153	-1154	-1155	-1156	-1157	-1158	-1159	-1160	-1161	-1162	-1163	-1164	-1165	-1166	-1167	-1168
FB60	-1169	-1170	-1171	-1172	-1173	-1174	-1175	-1176	-1177	-1178	-1179	-1180	-1181	-1182	-1183	-1184
FB50	-1185	-1186	-1187	-1188	-1189	-1190	-1191	-1192	-1193	-1194	-1195	-1196	-1197	-1198	-1199	-1200
FB40	-1201	-1202	-1203	-1204	-1205	-1206	-1207	-1208	-1209	-1210	-1211	-1212	-1213	-1214	-1215	-1216
FB30	-1217	-1218	-1219	-1220	-1221	-1222	-1223	-1224	-1225	-1226	-1227	-1228	-1229	-1230	-1231	-1232
FB20	-1233	-1234	-1235	-1236	-1237	-1238	-1239	-1240	-1241	-1242	-1243	-1244	-1245	-1246	-1247	-1248
FB10	-1249	-1250	-1251	-1252	-1253	-1254	-1255	-1256	-1257	-1258	-1259	-1260	-1261	-1262	-1263	-1264
FB00	-1265	-1266	-1267	-1268	-1269	-1270	-1271	-1272	-1273	-1274	-1275	-1276	-1277	-1278	-1279	-1280
FAF0	-1281	-1282	-1283	-1284	-1285	-1286	-1287	-1288	-1289	-1290	-1291	-1292	-1293	-1294	-1295	-1296
FAE0	-1297	-1298	-1299	-1300	-1301	-1302	-1303	-1304	-1305	-1306	-1307	-1308	-1309	-1310	-1311	-1312
FAD0	-1313	-1314	-1315	-1316	-1317	-1318	-1319	-1320	-1321	-1322	-1323	-1324	-1325	-1326	-1327	-1328
FAC0	-1329	-1330	-1331	-1332	-1333	-1334	-1335	-1336	-1337	-1338	-1339	-1340	-1341	-1342	-1343	-1344
FAB0	-1345	-1346	-1347	-1348	-1349	-1350	-1351	-1352	-1353	-1354	-1355	-1356	-1357	-1358	-1359	-1360
FAA0	-1361	-1362	-1363	-1364	-1365	-1366	-1367	-1368	-1369	-1370	-1371	-1372	-1373	-1374	-1375	-1376
FA90	-1377	-1378	-1379	-1380	-1381	-1382	-1383	-1384	-1385	-1386	-1387	-1388	-1389	-1390	-1391	-1392
FA80	-1393	-1394	-1395	-1396	-1397	-1398	-1399	-1400	-1401	-1402	-1403	-1404	-1405	-1406	-1407	-1408
FA70	-1409	-1410	-1411	-1412	-1413	-1414	-1415	-1416	-1417	-1418	-1419	-1420	-1421	-1422	-1423	-1424
FA60	-1425	-1426	-1427	-1428	-1429	-1430	-1431	-1432	-1433	-1434	-1435	-1436	-1437	-1438	-1439	-1440
FA50	-1441	-1442	-1443	-1444	-1445	-1446	-1447	-1448	-1449	-1450	-1451	-1452	-1453	-1454	-1455.	-1456
FA40	-1457	-1458	-1459	-1460	-1461	-1462	-1463	-1464	-1465	-1466	-1467	-1468	-1469	-1470	-1471	-1472
FA30	-1473	-1474	-1475	-1476	-1477	-1478	-1479	-1480	-1481	-1482	-1483	-1484	-1485	-1486	-1487	-1488
FA20	-1489	-1490	-1491	-1492	-1493	-1494	-1495	-1496	-1497	-1498	-1499	-1500	-1501	-1502	-1503	-1504
FA10	-1505	-1506	-1507	-1508	-1509	-1510	-1511	-1512	-1513	-1514	-1515	-1516	-1517	-1518	-1519	-1520
FA00	-1521	-1522	-1523	-1524	-1525	-1526	-1527	-1528	-1529	-1530	-1531	-1532	-1533	-1534	-1535	-1536
F9F0	-1537	-1538	-1539	-1540	-1541	-1542	-1543	-1544	-1545	-1546	-1547	-1548	-1549	-1550	-1551	-1552
F9E0	-1553	-1554	-1555	-1556	-1557	-1558	-1559	-1560	-1561	-1562	-1563	-1564	-1565	-1566	-1567	-1568
F9D0	-1569	-1570	-1571	-1572	-1573	-1574	-1575	-1576	-1577	-1578	-1579	-1580	-1581	-1582	-1583	-1584
F9C0	-1585	-1586	-1587	-1588	-1589	-1590	-1591	-1592	-1593	-1594	-1595	-1596	-1597	-1598	-1599	-1600
F9B0	-1601	-1602	-1603	-1604	-1605	-1606	-1607	-1608	-1609	-1610	-1611	-1612	-1613	-1614	-1615	-1616
F9A0	-1617	-1618	-1619	-1620	-1621	-1622	-1623	-1624	-1625	-1626	-1627	-1628	-1629	-1630	-1631	-1632
F990	-1633	-1634	-1635	-1636	-1637	-1638	-1639	-1640	-1641	-1642	-1643	-1644	-1645	-1646	-1647	-1648
F980	-1649	-1650	-1651	-1652	-1653	-1654	-1655	-1656	-1657	-1658	-1659	-1660	-1661	-1662	-1663	-1664
F970	-1665	-1666	-1667	-1668	-1669	-1670	-1671	-1672	-1673	-1674	-1675	-1676	-1677	-1678	-1679	-1680
F960	-1681	-1682	-1683	-1684	-1685	-1686	-1687	-1688	-1689	-1690	-1691	-1692	-1693	-1694	-1695	-1696
F950	-1697	-1698	-1699	-1700	-1701	-1702	-1703	-1704	-1705	-1706	-1707	-1708	-1709	-1710	-1711	-1712
F940	-1713	-1714	-1715	-1716	-1717	-1718	-1719	-1720	-1721	-1722	-1723	-1724	-1725	-1726	-1727	-1728
F930	-1729	-1730	-1731	-1732	-1733	-1734	-1735	-1736	-1737	-1738	-1739	-1740	-1741	-1742	-1743	-1744
F920	-1745	-1746	-1747	-1748	-1749	-1750	-1751	-1752	-1753	-1754	-1755	-1756	-1757	-1758	-1759	-1760
F910	-1761	-1762	-1763	-1764	-1765	-1766	-1767	-1768	-1769	-1770	-1771	-1772	-1773	-1774	-1775	-1776
F900	-1777	-1778	-1779	-1780	-1781	-1782	-1783	-1784	-1785	-1786	-1787	-1788	-1789	-1790	-1791	-1792
F8F0	-1793	-1794	-1795	-1796	-1797	-1798	-1799	-1800	-1801	-1802	-1803	-1804	-1805	-1806	-1807	-1808
F8E0	-1809	-1810	-1811	-1812	-1813	-1814	-1815	-1816	-1817	-1818	-1819	-1820	-1821	-1822	-1823	-1824
F8D0	-1825	-1826	-1827	-1828	-1829	-1830	-1831	-1832	-1833	-1834	-1835	-1836	-1837	-1838	-1839	-1840
F8C0	-1841	-1842	-1843	-1844	-1845	-1846	-1847	-1848	-1849	-1850	-1851	-1852	-1853	-1854	-1855	-1856
F8B0	-1857	-1858	-1859	-1860	-1861	-1862	-1863	-1864	-1865	-1866	-1867	-1868	-1869	-1870	-1871	-1872
F8A0	-1873	-1874	-1875	-1876	-1877	-1878	-1879	-1880	-1881	-1882	-1883	-1884	-1885	-1886	-1887	-1888
F890	-1889	-1890	-1891	-1892	-1893	-1894	-1895	-1896	-1897	-1898	-1899	-1900	-1901	-1902	-1903	-1904
F880	-1905	-1906	-1907	-1908	-1909	-1910	-1911	-1912	-1913	-1914	-1915	-1916	-1917	-1918	-1919	-1920
F870	-1921	-1922	-1923	-1924	-1925	-1926	-1927	-1928	-1929	-1930	-1931	-1932	-1933	-1934	-1935	-1936
F860	-1937	-1938	-1939	-1940	-1941	-1942	-1943	-1944	-1945	-1946	-1947	-1948	-1949	-1950	-1951	-1952
F850	-1953	-1954	-1955	-1956	-1957	-1958	-1959	-1960	-1961	-1962	-1963	-1964	-1965	-1966	-1967	-1968
F840	-1969	-1970	-1971	-1972	-1973	-1974	-1975	-1976	-1977	-1978	-1979	-1980	-1981	-1982	-1983	-1984
F830	-1985	-1986	-1987	-1988	-1989	-1990	-1991	-1992	-1993	-1994	-1995	-1996	-1997	-1998	-1999	-2000
F820	-2001	-2002	-2003	-2004	-2005	-2006	-2007	-2008	-2009	-2010	-2011	-2012	-2013	-2014	-2015	-2016
F810	-2017	-2018	-2019	-2020	-2021	-2022	-2023	-2024	-2025	-2026	-2027	-2028	-2029	-2030	-2031	-2032
F800	-2033	-2034	-2035	-2036	-2037	-2038	-2039	-2040	-2041	-2042	-2043	-2044	-2045	-2046	-2047	-2048

HEXADECIMAL - TO - NEGATIVE INTEGER CONVERSION TABLE (CONT.)

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
F7F0	-2049	-2050	-2051	-2052	-2053	-2054	-2055	-2056	-2057	-2058	-2059	-2060	-2061	-2062	-2063	-2064
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F7D0	-2081	-2082	-2083	-2084	-2085	-2086	-2087	-2088	-2089	-2090	-2091	-2092	-2093	-2094	-2095	-2096
F7C0	-2097	-2098	-2099	-2100	-2101	-2102	-2103	-2104	-2105	-2106	-2107	-2108	-2109	-2110	-2111	-2112
F7B0	-2113	-2114	-2115	-2116	-2117	-2118	-2119	-2120	-2121	-2122	-2123	-2124	-2125	-2126	-2127	-2128
F7A0	-2129	-2130	-2131	-2132	-2133	-2134	-2135	-2136	-2137	-2138	-2139	-2140	-2141	-2142	-2143	-2144
F790	-2145	-2146	-2147	-2148	-2149	-2150	-2151	-2152	-2153	-2154	-2155	-2156	-2157	-2158	-2159	-2160
F780	-2161	-2162	-2163	-2164	-2165	-2166	-2167	-2168	-2169	-2170	-2171	-2172	-2173	-2174	-2175	-2176
F770	-2177	-2178	-2179	-2180	-2181	-2182	-2183	-2184	-2185	-2186	-2187	-2188	-2189	-2190	-2191	-2192
F760	-2193	-2194	-2195	-2196	-2197	-2198	-2199	-2200	-2201	-2202	-2203	-2204	-2205	-2206	-2207	-2208
F750	-2209	-2210	-2211	-2212	-2213	-2214	-2215	-2216	-2217	-2218	-2219	-2220	-2221	-2222	-2223	-2224
F740	-2225	-2226	-2227	-2228	-2229	-2230	-2231	-2232	-2233	-2234	-2235	-2236	-2237	-2238	-2239	-2240
F730	-2241	-2242	-2243	-2244	-2245	-2246	-2247	-2248	-2249	-2250	-2251	-2252	-2253	-2254	-2255	-2256
F720	-2257	-2258	-2259	-2260	-2261	-2262	-2263	-2264	-2265	-2266	-2267	-2268	-2269	-2270	-2271	-2272
F710	-2273	-2274	-2275	-2276	-2277	-2278	-2279	-2280	-2281	-2282	-2283	-2284	-2285	-2286	-2287	-2288
F700	-2289	-2290	-2291	-2292	-2293	-2294	-2295	-2296	-2297	-2298	-2299	-2300	-2301	-2302	-2303	-2304
F6F0	-2305	-2306	-2307	-2308	-2309	-2310	-2311	-2312	-2313	-2314	-2315	-2316	-2317	-2318	-2319	-2320
F6E0	-2321	-2322	-2323	-2324	-2325	-2326	-2327	-2328	-2329	-2330	-2331	-2332	-2333	-2334	-2335	-2336
F6D0	-2337	-2338	-2339	-2340	-2341	-2342	-2343	-2344	-2345	-2346	-2347	-2348	-2349	-2350	-2351	-2352
F6C0	-2353	-2354	-2355	-2356	-2357	-2358	-2359	-2360	-2361	-2362	-2363	-2364	-2365	-2366	-2367	-2368
F6B0	-2369	-2370	-2371	-2372	-2373	-2374	-2375	-2376	-2377	-2378	-2379	-2380	-2381	-2382	-2383	-2384
F6A0	-2385	-2386	-2387	-2388	-2389	-2390	-2391	-2392	-2393	-2394	-2395	-2396	-2397	-2398	-2399	-2400
F690	-2401	-2402	-2403	-2404	-2405	-2406	-2407	-2408	-2409	-2410	-2411	-2412	-2413	-2414	-2415	-2416
F680	-2417	-2418	-2419	-2420	-2421	-2422	-2423	-2424	-2425	-2426	-2427	-2428	-2429	-2430	-2431	-2432
F670	-2433	-2434	-2435	-2436	-2437	-2438	-2439	-2440	-2441	-2442	-2443	-2444	-2445	-2446	-2447	-2448
F660	-2449	-2450	-2451	-2452	-2453	-2454	-2455	-2456	-2457	-2458	-2459	-2460	-2461	-2462	-2463	-2464
F650	-2465	-2466	-2467	-2468	-2469	-2470	-2471	-2472	-2473	-2474	-2475	-2476	-2477	-2478	-2479	-2480
F640	-2481	-2482	-2483	-2484	-2485	-2486	-2487	-2488	-2489	-2490	-2491	-2492	-2493	-2494	-2495	-2496
F630	-2497	-2498	-2499	-2500	-2501	-2502	-2503	-2504	-2505	-2506	-2507	-2508	-2509	-2510	-2511	-2512
F620	-2513	-2514	-2515	-2516	-2517	-2518	-2519	-2520	-2521	-2522	-2523	-2524	-2525	-2526	-2527	-2528
F610	-2529	-2530	-2531	-2532	-2533	-2534	-2535	-2536	-2537	-2538	-2539	-2540	-2541	-2542	-2543	-2544
F600	-2545	-2546	-2547	-2548	-2549	-2550	-2551	-2552	-2553	-2554	-2555	-2556	-2557	-2558	-2559	-2560
F5F0	-2561	-2562	-2563	-2564	-2565	-2566	-2567	-2568	-2569	-2570	-2571	-2572	-2573	-2574	-2575	-2576
F5E0	-2577	-2578	-2579	-2580	-2581	-2582	-2583	-2584	-2585	-2586	-2587	-2588	-2589	-2590	-2591	-2592
F5D0	-2593	-2594	-2595	-2596	-2597	-2598	-2599	-2600	-2601	-2602	-2603	-2604	-2605	-2606	-2607	-2608
F5C0	-2609	-2610	-2611	-2612	-2613	-2614	-2615	-2616	-2617	-2618	-2619	-2620	-2621	-2622	-2623	-2624
F5B0	-2625	-2626	-2627	-2628	-2629	-2630	-2631	-2632	-2633	-2634	-2635	-2636	-2637	-2638	-2639	-2640
F5A0	-2641	-2642	-2643	-2644	-2645	-2646	-2647	-2648	-2649	-2650	-2651	-2652	-2653	-2654	-2655	-2656
F590	-2657	-2658	-2659	-2660	-2661	-2662	-2663	-2664	-2665	-2666	-2667	-2668	-2669	-2670	-2671	-2672
F580	-2673	-2674	-2675	-2676	-2677	-2678	-2679	-2680	-2681	-2682	-2683	-2684	-2685	-2686	-2687	-2688
F570	-2689	-2690	-2691	-2692	-2693	-2694	-2695	-2696	-2697	-2698	-2699	-2700	-2701	-2702	-2703	-2704
F560	-2705	-2706	-2707	-2708	-2709	-2710	-2711	-2712	-2713	-2714	-2715	-2716	-2717	-2718	-2719	-2720
F550	-2721	-2722	-2723	-2724	-2725	-2726	-2727	-2728	-2729	-2730	-2731	-2732	-2733	-2734	-2735	-2736
F540	-2737	-2738	-2739	-2740	-2741	-2742	-2743	-2744	-2745	-2746	-2747	-2748	-2749	-2750	-2751	-2752
F530	-2753	-2754	-2755	-2756	-2757	-2758	-2759	-2760	-2761	-2762	-2763	-2764	-2765	-2766	-2767	-2768
F520	-2769	-2770	-2771	-2772	-2773	-2774	-2775	-2776	-2777	-2778	-2779	-2780	-2781	-2782	-2783	-2784
F510	-2785	-2786	-2787	-2788	-2789	-2790	-2791	-2792	-2793	-2794	-2795	-2796	-2797	-2798	-2799	-2800
F500	-2801	-2802	-2803	-2804	-2805	-2806	-2807	-2808	-2809	-2810	-2811	-2812	-2813	-2814	-2815	-2816
F4F0	-2817	-2818	-2819	-2820	-2821	-2822	-2823	-2824	-2825	-2826	-2827	-2828	-2829	-2830	-2831	-2832
F4E0	-2833	-2834	-2835	-2836	-2837	-2838	-2839	-2840	-2841	-2842	-2843	-2844	-2845	-2846	-2847	-2848
F4D0	-2849	-2850	-2851	-2852	-2853	-2854	-2855	-2856	-2857	-2858	-2859	-2860	-2861	-2862	-2863	-2864
F4C0	-2865	-2866	-2867	-2868	-2869	-2870	-2871	-2872	-2873	-2874	-2875	-2876	-2877	-2878	-2879	-2880
F4B0	-2881	-2882	-2883	-2884	-2885	-2886	-2887	-2888	-2889	-2890	-2891	-2892	-2893	-2894	-2895	-2896
F4A0	-2897	-2898	-2899	-2900	-2901	-2902	-2903	-2904	-2905	-2906	-2907	-2908	-2909	-2910	-2911	-2912
F490	-2913	-2914	-2915	-2916	-2917	-2918	-2919	-2920	-2921	-2922	-2923	-2924	-2925	-2926	-2927	-2928
F480	-2929	-2930	-2931	-2932	-2933	-2934	-2935	-2936	-2937	-2938	-2939	-2940	-2941	-2942	-2943	-2944
F470	-2945	-2946	-2947	-2948	-2949	-2950	-2951	-2952	-2953	-2954	-2955	-2956	-2957	-2958	-2959	-2960
F460	-2961	-2962	-2963	-2964	-2965	-2966	-2967	-2968	-2969	-2970	-2971	-2972	-2973	-2974	-2975	-2976
F450	-2977	-2978	-2979	-2980	-2981	-2982	-2983	-2984	-2985	-2986	-2987	-2988	-2989	-2990	-2991	-2992
F440	-2993	-2994	-2995	-2996	-2997	-2998	-2999	-3000	-3001	-3002	-3003	-3004	-3005	-3006	-3007	-3008
F430	-3009	-3010	-3011	-3012	-3013	-3014	-3015	-3016	-3017	-3018	-3019	-3020	-3021	-3022	-3023	-3024
F420	-3025	-3026	-3027	-3028	-3029	-3030	-3031	-3032	-3033	-3034	-3035	-3036	-3037	-3038	-3039	-3040
F410	-3041	-3042	-3043	-3044	-3045	-3046	-3047	-3048	-3049	-3050	-3051	-3052	-3053	-3054	-3055	-3056
F400	-3057	-3058	-3059	-3060	-3061	-3062	-3063	-3064	-3065	-3066	-3067	-3068	-3069	-3070	-3071	-3072

HEXADECIMAL - TO - NEGATIVE INTEGER CONVERSION TABLE (CONT.

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
F3F0	-3073	-3074	-3075	-3076	-3077	-3078	-3079	-3080	-3081	-3082	-3083	-3084	-3085	-3086	-3087	-3088
F3E0	-3089	-3090	-3091	-3092	-3093	-3094	-3095	-3096	-3097	-3098	-3099	-3100	-3101	-3102	-3103	-3104
F3D0	-3105	-3106	-3107	-3108	-3109	-3110	-3111	-3112	-3113	-3114	-3115	-3116	-3117	-3118	-3119	-3120
F3C0	-3121	-3122	-3123	-3124	-3125	-3126	-3127	-3128	-3129	-3130	-3131	-3132	-3133	-3134	-3135	-3136
F3B0	-3137	-3138	-3139	-3140	-3141	-3142	-3143	-3144	-3145	-3146	-3147	-3148	-3149	-3150	-3151	-3152
F3A0	-3153	-3154	-3155	-3156	-3157	-3158	-3159	-3160	-3161	-3162	-3163	-3164	-3165	-3166	-3167	-3168
F390	-3169	-3170	-3171	-3172	-3173	-3174	-3175	-3176	-3177	-3178	-3179	-3180	-3181	-3182	-3183	-3184
F380	-3185	-3186	-3187	-3188	-3189	-3190	-3191	-3192	-3193	-3194	-3195	-3196	-3197	-3198	-3199	-3200
F370	-3201	-3202	-3203	-3204	-3205	-3206	-3207	-3208	-3209	-3210	-3211	-3212	-3213	-3214	-3215	-3216
F360	-3217	-3218	-3219	-3220	-3221	-3222	-3223	-3224	-3225	-3226	-3227	-3228	-3229	-3230	-3231	-3232
F350	-3233	-3234	-3235	-3236	-3237	-3238	-3239	-3240	-3241	-3242	-3243	-3244	-3245	-3246	-3247	-3248
F340	-3249	-3250	-3251	-3252	-3253	-3254	-3255	-3256	-3257	-3258	-3259	-3260	-3261	-3262	-3263	-3264
F330	-3265	-3266	-3267	-3268	-3269	-3270	-3271	-3272	-3273	-3274	-3275	-3276	-3277	-3278	-3279	-3280
F320	-3281	-3282	-3283	-3284	-3285	-3286	-3287	-3288	-3289	-3290	-3291	-3292	-3293	-3294	-3295	-3296
F310	-3297	-3298	-3299	-3300	-3301	-3302	-3303	-3304	-3305	-3306	-3307	-3308	-3309	-3310	-3311	-3312
F300	-3313	-3314	-3315	-3316	-3317	-3318	-3319	-3320	-3321	-3322	-3323	-3324	-3325	-3326	-3327	-3328
F2F0	-3329	-3330	-3331	-3332	-3333	-3334	-3335	-3336	-3337	-3338	-3339	-3340	-3341	-3342	-3343	-3344
F2E0	-3345	-3346	-3347	-3348	-3349	-3350	-3351	-3352	-3353	-3354	-3355	-3356	-3357	-3358	-3359	-3360
F2D0	-3361	-3362	-3363	-3364	-3365	-3366	-3367	-3368	-3369	-3370	-3371	-3372	-3373	-3374	-3375	-3376
F2C0	-3377	-3378	-3379	-3380	-3381	-3382	-3383	-3384	-3385	-3386	-3387	-3388	-3389	-3390	-3391	-3392
F2B0	-3393	-3394	-3395	-3396	-3397	-3398	-3399	-3400	-3401	-3402	-3403	-3404	-3405	-3406	-3407	-3408
F2A0	-3409	-3410	-3411	-3412	-3413	-3414	-3415	-3416	-3417	-3418	-3419	-3420	-3421	-3422	-3423	-3424
F290	-3425	-3426	-3427	-3428	-3429	-3430	-3431	-3432	-3433	-3434	-3435	-3436	-3437	-3438	-3439	-3440
F280	-3441	-3442	-3443	-3444	-3445	-3446	-3447	-3448	-3449	-3450	-3451	-3452	-3453	-3454	-3455	-3456
F270	-3457	-3458	-3459	-3460	-3461	-3462	-3463	-3464	-3465	-3466	-3467	-3468	-3469	-3470	-3471	-3472
F260	-3473	-3474	-3475	-3476	-3477	-3478	-3479	-3480	-3481	-3482	-3483	-3484	-3485	-3486	-3487	-3488
F250	-3489	-3490	-3491	-3492	-3493	-3494	-3495	-3496	-3497	-3498	-3499	-3500	-3501	-3502	-3503	-3504
F240	-3505	-3506	-3507	-3508	-3509	-3510	-3511	-3512	-3513	-3514	-3515	-3516	-3517	-3518	-3519	-3520
F230	-3521	-3522	-3523	-3524	-3525	-3526	-3527	-3528	-3529	-3530	-3531	-3532	-3533	-3534	-3535	-3536
F220	-3537	-3538	-3539	-3540	-3541	-3542	-3543	-3544	-3545	-3546	-3547	-3548	-3549	-3550	-3551	-3552
F210	-3553	-3554	-3555	-3556	-3557	-3558	-3559	-3560	-3561	-3562	-3563	-3564	-3565	-3566	-3567	-3568
F200	-3569	-3570	-3571	-3572	-3573	-3574	-3575	-3576	-3577	-3578	-3579	-3580	-3581	-3582	-3583	-3584
F1F0	-3585	-3586	-3587	-3588	-3589	-3590	-3591	-3592	-3593	-3594	-3595	-3596	-3597	-3598	-3599	-3600
F1E0	-3601	-3602	-3603	-3604	-3605	-3606	-3607	-3608	-3609	-3610	-3611	-3612	-3613	-3614	-3615	-3616
F1D0	-3617	-3618	-3619	-3620	-3621	-3622	-3623	-3624	-3625	-3626	-3627	-3628	-3629	-3630	-3631	-3632
F1C0	-3633	-3634	-3635	-3636	-3637	-3638	-3639	-3640	-3641	-3642	-3643	-3644	-3645	-3646	-3647	-3648
F1B0	-3649	-3650	-3651	-3652	-3653	-3654	-3655	-3656	-3657	-3658	-3659	-3660	-3661	-3662	-3663	-3664
F1A0	-3665	-3666	-3667	-3668	-3669	-3670	-3671	-3672	-3673	-3674	-3675	-3676	-3677	-3678	-3679	-3680
F190	-3681	-3682	-3683	-3684	-3685	-3686	-3687	-3688	-3689	-3690	-3691	-3692	-3693	-3694	-3695	-3696
F180	-3697	-3698	-3699	-3700	-3701	-3702	-3703	-3704	-3705	-3706	-3707	-3708	-3709	-3710	-3711	-3712
F170	-3713	-3714	-3715	-3716	-3717	-3718	-3719	-3720	-3721	-3722	-3723	-3724	-3725	-3726	-3727	-3728
F160	-3729	-3730	-3731	-3732	-3733	-3734	-3735	-3736	-3737	-3738	-3739	-3740	-3741	-3742	-3743	-3744
F150	-3745	-3746	-3747	-3748	-3749	-3750	-3751	-3752	-3753	-3754	-3755	-3756	-3757	-3758	-3759	-3760
F140	-3761	-3762	-3763	-3764	-3765	-3766	-3767	-3768	-3769	-3770	-3771	-3772	-3773	-3774	-3775	-3776
F130	-3777	-3778	-3779	-3780	-3781	-3782	-3783	-3784	-3785	-3786	-3787	-3788	-3789	-3790	-3791	-3792
F120	-3793	-3794	-3795	-3796	-3797	-3798	-3799	-3800	-3801	-3802	-3803	-3804	-3805	-3806	-3807	-3808
F110	-3809	-3810	-3811	-3812	-3813	-3814	-3815	-3816	-3817	-3818	-3819	-3820	-3821	-3822	-3823	-3824
F100	-3825	-3826	-3827	-3828	-3829	-3830	-3831	-3832	-3833	-3834	-3835	-3836	-3837	-3838	-3839	-3840
F0F0	-3841	-3842	-3843	-3844	-3845	-3846	-3847	-3848	-3849	-3850	-3851	-3852	-3853	-3854	-3855	-3856
F0E0	-3857	-3858	-3859	-3860	-3861	-3862	-3863	-3864	-3865	-3866	-3867	-3868	-3869	-3870	-3871	-3872
F0D0	-3873	-3874	-3875	-3876	-3877	-3878	-3879	-3880	-3881	-3882	-3883	-3884	-3885	-3886	-3887	-3888
F0C0	-3889	-3890	-3891	-3892	-3893	-3894	-3895	-3896	-3897	-3898	-3899	-3900	-3901	-3902	-3903	-3904
F0B0	-3905	-3906	-3907	-3908	-3909	-3910	-3911	-3912	-3913	-3914	-3915	-3916	-3917	-3918	-3919	-3920
F0A0	-3921	-3922	-3923	-3924	-3925	-3926	-3927	-3928	-3929	-3930	-3931	-3932	-3933	-3934	-3935	-3936
F090	-3937	-3938	-3939	-3940	-3941	-3942	-3943	-3944	-3945	-3946	-3947	-3948	-3949	-3950	-3951	-3952
F080	-3953	-3954	-3955	-3956	-3957	-3958	-3959	-3960	-3961	-3962	-3963	-3964	-3965	-3966	-3967	-3968
F070	-3969	-3970	-3971	-3972	-3973	-3974	-3975	-3976	-3977	-3978	-3979	-3980	-3981	-3982	-3983	-3984
F060	-3985	-3986	-3987	-3988	-3989	-3990	-3991	-3992	-3993	-3994	-3995	-3996	-3997	-3998	-3999	-4000
F050	-4001	-4002	-4003	-4004	-4005	-4006	-4007	-4008	-4009	-4010	-4011	-4012	-4013	-4014	-4015	-4016
F040	-4017	-4018	-4019	-4020	-4021	-4022	-4023	-4024	-4025	-4026	-4027	-4028	-4029	-4030	-4031	-4032
F030	-4033	-4034	-4035	-4036	-4037	-4038	-4039	-4040	-4041	-4042	-4043	-4044	-4045	-4046	-4047	-4048
F020	-4049	-4050	-4051	-4052	-4053	-4054	-4055	-4056	-4057	-4058	-4059	-4060	-4061	-4062	-4063	-4064
F010	-4065	-4066	-4067	-4068	-4069	-4070	-4071	-4072	-4073	-4074	-4075	-4076	-4077	-4078	-4079	-4080
F000	-4081	-4082	-4083	-4084	-4085	-4086	-4087	-4088	-4089	-4090	-4091	-4092	-4093	-4094	-4095	-4096

HEXADECIMAL - TO - DECIMAL FRACTION TABLE

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
.000	.00000	.00024	.00049	.00073	.00098	.00122	.00146	.00171	.00195	.00220	.00244	.00269	.00293	.00317	.00342	.00366
.010	.00391	.00415	.00439	.00464	.00488	.00513	.00537	.00562	.00586	.00610	.00635	.00659	.00684	.00708	.00732	.00757
.020	.00781	.00806	.00830	.00854	.00879	.00903	.00928	.00952	.00977	.01001	.01025	.01050	.01074	.01099	.01123	.01147
.030	.01172	.01196	.01221	.01245	.01270	.01294	.01318	.01343	.01367	.01392	.01416	.01440	.01465	.01489	.01514	.01538
.040	.01562	.01587	.01611	.01636	.01660	.01685	.01709	.01733	.01758	.01782	.01807	.01831	.01855	.01880	.01904	.01929
.050	.01953	.01978	.02002	.02026	.02051	.02075	.02100	.02124	.02148	.02173	.02197	.02222	.02246	.02271	.02295	.02319
.060	.02344	.02368	.02393	.02417	.02441	.02466	.02490	.02515	.02539	.02563	.02588	.02612	.02637	.02661	.02686	.02710
.070	.02734	.02759	.02783	.02808	.02832	.02856	.02881	.02905	.02930	.02954	.02979	.03003	.03027	.03052	.03076	.03101
.080	.03125	.03149	.03174	.03198	.03223	.03247	.03271	.03296	.03320	.03345	.03369	.03394	.03418	.03442	.03467	.03491
.090	.03516	.03540	.03564	.03589	.03613	.03638	.03662	.03687	.03711	.03735	.03760	.03784	.03809	.03833	.03857	.03882
.0A0	.03906	.03931	.03955	.03979	.04004	.04028	.04053	.04077	.04102	.04126	.04150	.04175	.04199	.04224	.04248	.04272
.0B0	.04297	.04321	.04346	.04370	.04395	.04419	.04443	.04468	.04492	.04517	.04541	.04565	.04590	.04614	.04639	.04663
.0C0	.04687	.04712	.04736	.04761	.04785	.04810	.04834	.04858	.04883	.04907	.04932	.04956	.04980	.05005	.05029	.05054
.0D0	.05078	.05103	.05127	.05151	.05176	.05200	.05225	.05249	.05273	.05298	.05322	.05347	.05371	.05396	.05420	.05444
.0E0	.05469	.05493	.05518	.05542	.05566	.05591	.05615	.05640	.05664	.05688	.05713	.05737	.05762	.05786	.05811	.05835
.0F0	.05859	.05884	.05908	.05933	.05957	.05981	.06006	.06030	.06055	.06079	.06104	.06128	.06152	.06177	.06201	.06226
.100	.06250	.06274	.06299	.06323	.06348	.06372	.06396	.06421	.06445	.06470	.06494	.06519	.06543	.06567	.06592	.06616
.110	.06641	.06665	.06689	.06714	.06738	.06763	.06787	.06812	.06836	.06860	.06885	.06909	.06934	.06958	.06982	.07007
.120	.07031	.07056	.07080	.07104	.07129	.07153	.07178	.07202	.07227	.07251	.07275	.07300	.07324	.07349	.07373	.07397
.130	.07422	.07446	.07471	.07495	.07520	.07544	.07568	.07593	.07617	.07642	.07666	.07690	.07715	.07739	.07764	.07788
.140	.07812	.07837	.07861	.07886	.07910	.07935	.07959	.07983	.08008	.08032	.08057	.08081	.08105	.08130	.08154	.08179
.150	.08203	.08228	.08252	.08276	.08301	.08325	.08350	.08374	.08398	.08423	.08447	.08472	.08496	.08521	.08545	.08569
.160	.08594	.08618	.08643	.08667	.08691	.08716	.08740	.08765	.08789	.08813	.08838	.08862	.08887	.08911	.08936	.08960
.170	.08984	.09009	.09033	.09058	.09082	.09106	.09131	.09155	.09180	.09204	.09229	.09253	.09277	.09302	.09326	.09351
.180	.09375	.09399	.09424	.09448	.09473	.09497	.09521	.09546	.09570	.09595	.09619	.09644	.09668	.09692	.09717	.09741
.190	.09766	.09790	.09814	.09839	.09863	.09888	.09912	.09937	.09961	.09985	.10010	.10034	.10059	.10083	.10107	.10132
.1A0	.10156	.10181	.10205	.10229	.10254	.10278	.10303	.10327	.10352	.10376	.10400	.10425	.10449	.10474	.10498	.10522
.1B0	.10547	.10571	.10596	.10620	.10645	.10669	.10693	.10718	.10742	.10767	.10791	.10815	.10840	.10864	.10889	.10913
.1C0	.10937	.10962	.10986	.11011	.11035	.11060	.11084	.11108	.11133	.11157	.11182	.11206	.11230	.11255	.11279	.11304
.1D0	.11328	.11353	.11377	.11401	.11426	.11450	.11475	.11499	.11523	.11548	.11572	.11597	.11621	.11646	.11670	.11694
.1E0	.11719	.11743	.11768	.11792	.11816	.11841	.11865	.11890	.11914	.11938	.11963	.11987	.12012	.12036	.12061	.12085
.1F0	.12109	.12134	.12158	.12183	.12207	.12231	.12256	.12280	.12305	.12329	.12354	.12378	.12402	.12427	.12451	.12476
.200	.12500	.12524	.12549	.12573	.12598	.12622	.12646	.12671	.12695	.12720	.12744	.12769	.12793	.12817	.12842	.12866
.210	.12891	.12915	.12939	.12964	.12988	.13013	.13037	.13062	.13086	.13110	.13135	.13159	.13184	.13208	.13232	.13257
.220	.13281	.13306	.13330	.13354	.13379	.13403	.13428	.13452	.13477	.13501	.13525	.13550	.13574	.13599	.13623	.13647
.230	.13672	.13696	.13721	.13745	.13770	.13794	.13818	.13843	.13867	.13892	.13916	.13940	.13965	.13989	.14014	.14038
.240	.14062	.14087	.14111	.14136	.14160	.14185	.14209	.14233	.14258	.14282	.14307	.14331	.14355	.14380	.14404	.14429
.250	.14453	.14478	.14502	.14526	.14551	.14575	.14600	.14624	.14648	.14673	.14697	.14722	.14746	.14771	.14795	.14819
.260	.14844	.14868	.14893	.14917	.14941	.14966	.14990	.15015	.15039	.15063	.15088	.15112	.15137	.15161	.15186	.15210
.270	.15234	.15259	.15283	.15308	.15332	.15356	.15381	.15405	.15430	.15454	.15479	.15503	.15527	.15552	.15576	.15601
.280	.15625	.15649	.15674	.15698	.15723	.15747	.15771	.15796	.15820	.15845	.15869	.15894	.15918	.15942	.15967	.15991
.290	.16016	.16040	.16064	.16089	.16113	.16138	.16162	.16187	.16211	.16235	.16260	.16284	.16309	.16333	.16357	.16382
.2A0	.16406	.16431	.16455	.16479	.16504	.16528	.16553	.16577	.16602	.16626	.16650	.16675	.16699	.16724	.16748	.16772
.2B0	.16797	.16821	.16846	.16870	.16895	.16919	.16943	.16968	.16992	.17017	.17041	.17065	.17090	.17114	.17139	.17163
.2C0	.17187	.17212	.17236	.17261	.17285	.17310	.17334	.17358	.17383	.17407	.17432	.17456	.17480	.17505	.17529	.17554
.2D0	.17578	.17603	.17627	.17651	.17676	.17700	.17725	.17749	.17773	.17798	.17822	.17847	.17871	.17896	.17920	.17944
.2E0	.17969	.17993	.18018	.18042	.18066	.18091	.18115	.18140	.18164	.18188	.18213	.18237	.18262	.18286	.18311	.18335
.2F0	.18359	.18384	.18408	.18433	.18457	.18481	.18506	.18530	.18555	.18579	.18604	.18628	.18652	.18677	.18701	.18726
.300	.18750	.18774	.18799	.18823	.18848	.18872	.18896	.18921	.18945	.18970	.18994	.19019	.19043	.19067	.19092	.19116
.310	.19141	.19165	.19189	.19214	.19238	.19263	.19287	.19312	.19336	.19360	.19385	.19409	.19434	.19458	.19482	.19507
.320	.19531	.19556	.19580	.19604	.19629	.19653	.19678	.19702	.19727	.19751	.19775	.19800	.19824	.19849	.19873	.19897
.330	.19922	.19946	.19971	.19995	.20020	.20044	.20068	.20093	.20117	.20142	.20166	.20190	.20215	.20239	.20264	.20288
.340	.20312	.20337	.20361	.20386	.20410	.20435	.20459	.20483	.20508	.20532	.20557	.20581	.20605	.20630	.20654	.20679
.350	.20703	.20728	.20752	.20776	.20801	.20825	.20850	.20874	.20898	.20923	.20947	.20972	.20996	.21021	.21045	.21069
.360	.21094	.21118	.21143	.21167	.21191	.21216	.21240	.21265	.21289	.21313	.21338	.21362	.21387	.21411	.21436	.21460
.370	.21484	.21509	.21533	.21558	.21582	.21606	.21631	.21655	.21680	.21704	.21729	.21753	.21777	.21802	.21826	.21851
.380	.21875	.21899	.21924	.21948	.21973	.21997	.22021	.22046	.22070	.22095	.22119	.22144	.22168	.22192	.22217	.22241
.390	.22266	.22290	.22314	.22339	.22363	.22388	.22412	.22437	.22461	.22485	.22510	.22534	.22559	.22583	.22607	.22632
.3A0	.22656	.22681	.22705	.22729	.22754	.22778	.22803	.22827	.22852	.22876	.22900	.22925	.22949	.22974	.22998	.23022
.3B0	.23047	.23071	.23096	.23120	.23145	.23169	.23193	.23218	.23242	.23267	.23291	.23315	.23340	.23364	.23389	.23413
.3C0	.23437	.23462	.23486	.23511	.23535	.23560	.23584	.23608	.23633	.23657	.23682	.23706	.23730	.23755	.23779	.23804
.3D0	.23828	.23853	.23877	.23901	.23926	.23950	.23975	.23999	.24023	.24048	.24072	.24097	.24121	.24146	.24170	.24194
.3E0	.24219	.24243	.24268	.24292	.24316	.24341	.24365	.24390	.24414	.24438	.24463	.24487	.24512	.24536	.24561	.24585
.3F0	.24609	.24634	.24658	.24683	.24707	.24731	.24756	.24780	.24805	.24829	.24854	.24878	.24902	.24927	.24951	.24976
.400	.25000	.25024	.25049	.25073	.25098	.25122	.25146	.25171	.25195	.25220	.25244	.25269	.25293	.25317	.25342	.25366
.410	.25391	.25415	.25439	.25464	.25488	.25513	.25537	.25562	.25586	.25610	.25635	.25659	.25684	.25708	.25732	.25757
.420	.25781	.25806	.25830	.25854	.25879	.25903	.25928	.25952	.25977	.26001	.26025	.26050	.26074	.26099	.26123	.26147
.430	.26172	.26196	.26221	.26245	.26270	.26294	.26318	.26343	.26367	.26392	.26416	.26440	.26465	.26489	.26514	.26538
.440	.26562	.26587	.26611	.26636	.26660	.26685	.26709	.26733	.26758	.26782	.26807	.26831	.26855	.26880	.26904	.26929
.450	.26953	.26978	.27002	.27026	.27051	.27075	.27100	.27124	.27148	.27173	.27197	.27222	.27246	.27271	.27295	.27319
.460	.27344	.27368	.27393	.27417	.27441	.27466	.27490	.27515	.27539	.27563	.27588	.27612	.27637	.27661	.27686	.27710
.470	.27734	.27759	.27783	.27808	.27832	.27856	.27881	.27905	.27930	.27954	.27979	.28003	.28027	.28052	.28076	.28101
.480	.28125	.28149	.28174	.28198	.28223	.28247	.28271	.28296	.28320	.28345	.28369	.28394	.28418	.28442	.28467	.28491
.490	.28516	.28540	.28564	.28589	.28613	.28638	.28662	.28687	.28711	.28735	.28760	.28784	.28809	.28833	.28857	.28882
.4A0	.28906	.28931	.28955	.28979	.29004	.29028	.29053	.29077	.29102	.29126	.29150	.29175	.29199	.29224	.29248	.29272
.4B0	.29297	.29321	.29346	.29370	.29395	.29419	.29443	.29468	.29492	.29517	.29541	.29565	.29590	.29614	.29639	.29663
.4C0	.29687	.29712	.29736	.29761	.29785	.29810	.29834	.29858	.29883	.29907	.29932	.29956	.29980	.30005	.30029	.30054
.4D0	.30078	.30103	.30127	.30151	.30176	.30200	.30225	.30249	.30273	.30298	.30322	.30347	.30371	.30396	.30420	.30444
.4E0	.30469	.30493	.30518	.30542	.30566	.30591	.30615	.30640	.30664	.30688	.30713	.30737	.30762	.30786	.30811	.30835
.4F0	.30859	.30884	.30908	.30933	.30957	.30981	.31006	.31030	.31055	.31079	.31104	.31128	.31152	.31177	.31201	.31226

HEXADECIMAL - TO - DECIMAL FRACTION TABLE (CONT.)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
.500	.31250	.31274	.31299	.31323	.31348	.31372	.31396	.31421	.31445	.31470	.31494	.31519	.31543	.31567	.31592	.31616
.510	.31641	.31665	.31689	.31714	.31738	.31763	.31787	.31812	.31836	.31860	.31885	.31909	.31934	.31958	.31982	.32007
.520	.32031	.32056	.32080	.32104	.32129	.32153	.32178	.32202	.32227	.32251	.32275	.32300	.32324	.32349	.32373	.32397
.530	.32422	.32446	.32471	.32495	.32520	.32544	.32568	.32593	.32617	.32642	.32666	.32690	.32715	.32739	.32764	.32788
.540	.32812	.32837	.32861	.32886	.32910	.32935	.32959	.32983	.33008	.33032	.33057	.33081	.33105	.33130	.33154	.33179
.550	.33203	.33228	.33252	.33276	.33301	.33325	.33350	.33374	.33398	.33423	.33447	.33472	.33496	.33521	.33545	.33569
.560	.33594	.33618	.33643	.33667	.33691	.33716	.33740	.33765	.33789	.33813	.33838	.33862	.33887	.33911	.33936	.33960
.570	.33984	.34009	.34033	.34058	.34082	.34106	.34131	.34155	.34180	.34204	.34229	.34253	.34277	.34302	.34326	.34351
.580	.34375	.34399	.34424	.34448	.34473	.34497	.34521	.34546	.34570	.34595	.34619	.34644	.34668	.34692	.34717	.34741
.590	.34766	.34790	.34814	.34839	.34863	.34888	.34912	.34937	.34961	.34985	.35010	.35034	.35059	.35083	.35107	.35132
.5A0	.35156	.35181	.35205	.35229	.35254	.35278	.35303	.35327	.35352	.35376	.35400	.35425	.35449	.35474	.35498	.35522
.5B0	.35547	.35571	.35596	.35620	.35645	.35669	.35693	.35718	.35742	.35767	.35791	.35815	.35840	.35864	.35889	.35913
.5C0	.35937	.35962	.35986	.36011	.36035	.36060	.36084	.36108	.36133	.36157	.36182	.36206	.36230	.36255	.36279	.36304
.5D0	.36328	.36353	.36377	.36401	.36426	.36450	.36475	.36499	.36523	.36548	.36572	.36597	.36621	.36646	.36670	.36694
.5E0	.36719	.36743	.36768	.36792	.36816	.36841	.36865	.36890	.36914	.36938	.36963	.36987	.37012	.37036	.37061	.37085
.5F0	.37109	.37134	.37158	.37183	.37207	.37231	.37256	.37280	.37305	.37329	.37354	.37378	.37402	.37427	.37451	.37476
.600	.37500	.37524	.37549	.37573	.37598	.37622	.37646	.37671	.37695	.37720	.37744	.37769	.37793	.37817	.37842	.37866
.610	.37891	.37915	.37939	.37964	.37988	.38013	.38037	.38062	.38086	.38110	.38135	.38159	.38184	.38208	.38232	.38257
.620	.38281	.38306	.38330	.38354	.38379	.38403	.38428	.38452	.38477	.38501	.38525	.38550	.38574	.38599	.38623	.38647
.630	.38672	.38696	.38721	.38745	.38770	.38794	.38818	.38843	.38867	.38892	.38916	.38940	.38965	.38989	.39014	.39038
.640	.39062	.39087	.39111	.39136	.39160	.39185	.39209	.39233	.39258	.39282	.39307	.39331	.39355	.39380	.39404	.39429
.650	.39453	.39478	.39502	.39526	.39551	.39575	.39600	.39624	.39648	.39673	.39697	.39722	.39746	.39771	.39795	.39819
.660	.39844	.39868	.39893	.39917	.39941	.39966	.39990	.40015	.40039	.40063	.40088	.40112	.40137	.40161	.40186	.40210
.670	.40234	.40259	.40283	.40308	.40332	.40356	.40381	.40405	.40430	.40454	.40479	.40503	.40527	.40552	.40576	.40601
.680	.40625	.40649	.40674	.40698	.40723	.40747	.40771	.40796	.40820	.40845	.40869	.40894	.40918	.40942	.40967	.40991
.690	.41016	.41040	.41064	.41089	.41113	.41138	.41162	.41187	.41211	.41235	.41260	.41284	.41309	.41333	.41357	.41382
.6A0	.41406	.41431	.41455	.41479	.41504	.41528	.41553	.41577	.41602	.41626	.41650	.41675	.41699	.41724	.41748	.41772
.6B0	.41797	.41821	.41846	.41870	.41895	.41919	.41943	.41968	.41992	.42017	.42041	.42065	.42090	.42114	.42139	.42163
.6C0	.42187	.42212	.42236	.42261	.42285	.42310	.42334	.42358	.42383	.42407	.42432	.42456	.42480	.42505	.42529	.42554
.6D0	.42578	.42603	.42627	.42651	.42676	.42700	.42725	.42749	.42773	.42798	.42822	.42847	.42871	.42896	.42920	.42944
.6E0	.42969	.42993	.43018	.43042	.43066	.43091	.43115	.43140	.43164	.43188	.43213	.43237	.43262	.43286	.43311	.43335
.6F0	.43359	.43384	.43408	.43433	.43457	.43481	.43506	.43530	.43555	.43579	.43604	.43628	.43652	.43677	.43701	.43726
.700	.43750	.43774	.43799	.43823	.43848	.43872	.43896	.43921	.43945	.43970	.43994	.44019	.44043	.44067	.44092	.44116
.710	.44141	.44165	.44189	.44214	.44238	.44263	.44287	.44312	.44336	.44360	.44385	.44409	.44434	.44458	.44482	.44507
.720	.44531	.44556	.44580	.44604	.44629	.44653	.44678	.44702	.44727	.44751	.44775	.44800	.44824	.44849	.44873	.44897
.730	.44922	.44946	.44971	.44995	.45020	.45044	.45068	.45093	.45117	.45142	.45166	.45190	.45215	.45239	.45264	.45288
.740	.45312	.45337	.45361	.45386	.45410	.45435	.45459	.45483	.45508	.45532	.45557	.45581	.45605	.45630	.45654	.45679
.750	.45703	.45728	.45752	.45776	.45801	.45825	.45850	.45874	.45898	.45923	.45947	.45972	.45996	.46021	.46045	.46069
.760	.46094	.46118	.46143	.46167	.46191	.46216	.46240	.46265	.46289	.46313	.46338	.46362	.46387	.46411	.46436	.46460
.770	.46484	.46509	.46533	.46558	.46582	.46606	.46631	.46655	.46680	.46704	.46729	.46753	.46777	.46802	.46826	.46851
.780	.46875	.46899	.46924	.46948	.46973	.46997	.47021	.47046	.47070	.47095	.47119	.47144	.47168	.47192	.47217	.47241
.790	.47266	.47290	.47314	.47339	.47363	.47388	.47412	.47437	.47461	.47485	.47510	.47534	.47559	.47583	.47607	.47632
.7A0	.47656	.47681	.47705	.47729	.47754	.47778	.47803	.47827	.47852	.47876	.47900	.47925	.47949	.47974	.47998	.48022
.7B0	.48047	.48071	.48096	.48120	.48145	.48169	.48193	.48218	.48242	.48267	.48291	.48315	.48340	.48364	.48389	.48413
.7C0	.48437	.48462	.48486	.48511	.48535	.48560	.48584	.48608	.48633	.48657	.48682	.48706	.48730	.48755	.48779	.48804
.7D0	.48828	.48853	.48877	.48901	.48926	.48950	.48975	.48999	.49023	.49048	.49072	.49097	.49121	.49146	.49170	.49194
.7E0	.49219	.49243	.49268	.49292	.49316	.49341	.49365	.49390	.49414	.49438	.49463	.49487	.49512	.49536	.49561	.49585
.7F0	.49609	.49634	.49658	.49683	.49707	.49731	.49756	.49780	.49805	.49829	.49854	.49878	.49902	.49927	.49951	.49976
.800	.50000	.50024	.50049	.50073	.50098	.50122	.50146	.50171	.50195	.50220	.50244	.50269	.50293	.50317	.50342	.50366
.810	.50391	.50415	.50439	.50464	.50488	.50513	.50537	.50562	.50586	.50610	.50635	.50659	.50684	.50708	.50732	.50757
.820	.50781	.50806	.50830	.50854	.50879	.50903	.50928	.50952	.50977	.51001	.51025	.51050	.51074	.51099	.51123	.51147
.830	.51172	.51196	.51221	.51245	.51270	.51294	.51318	.51343	.51367	.51392	.51416	.51440	.51465	.51489	.51514	.51538
.840	.51562	.51587	.51611	.51636	.51660	.51685	.51709	.51733	.51758	.51782	.51807	.51831	.51855	.51880	.51904	.51929
.850	.51953	.51978	.52002	.52026	.52051	.52075	.52100	.52124	.52148	.52173	.52197	.52222	.52246	.52271	.52295	.52319
.860	.52344	.52368	.52393	.52417	.52441	.52466	.52490	.52515	.52539	.52563	.52588	.52612	.52637	.52661	.52686	.52710
.870	.52734	.52759	.52783	.52808	.52832	.52856	.52881	.52905	.52930	.52954	.52979	.53003	.53027	.53052	.53076	.53101
.880	.53125	.53149	.53174	.53198	.53223	.53247	.53271	.53296	.53320	.53345	.53369	.53394	.53418	.53442	.53467	.53491
.890	.53516	.53540	.53564	.53589	.53613	.53638	.53662	.53687	.53711	.53735	.53760	.53784	.53809	.53833	.53857	.53882
.8A0	.53906	.53931	.53955	.53979	.54004	.54028	.54053	.54077	.54102	.54126	.54150	.54175	.54199	.54224	.54248	.54272
.8B0	.54297	.54321	.54346	.54370	.54395	.54419	.54443	.54468	.54492	.54517	.54541	.54565	.54590	.54614	.54639	.54663
.8C0	.54687	.54712	.54736	.54761	.54785	.54810	.54834	.54858	.54883	.54907	.54932	.54956	.54980	.55005	.55029	.55054
.8D0	.55078	.55103	.55127	.55151	.55176	.55200	.55225	.55249	.55273	.55298	.55322	.55347	.55371	.55396	.55420	.55444
.8E0	.55469	.55493	.55518	.55542	.55566	.55591	.55615	.55640	.55664	.55688	.55713	.55737	.55762	.55786	.55811	.55835
.8F0	.55859	.55884	.55908	.55933	.55957	.55981	.56006	.56030	.56055	.56079	.56104	.56128	.56152	.56177	.56201	.56226
.900	.56250	.56274	.56299	.56323	.56348	.56372	.56396	.56421	.56445	.56470	.56494	.56519	.56543	.56567	.56592	.56616
.910	.56641	.56665	.56689	.56714	.56738	.56763	.56787	.56812	.56836	.56860	.56885	.56909	.56934	.56958	.56982	.57007
.920	.57031	.57056	.57080	.57104	.57129	.57153	.57178	.57202	.57227	.57251	.57275	.57300	.57324	.57349	.57373	.57397
.930	.57422	.57446	.57471	.57495	.57520	.57544	.57568	.57593	.57617	.57642	.57666	.57690	.57715	.57739	.57764	.57788
.940	.57812	.57837	.57861	.57886	.57910	.57935	.57959	.57983	.58008	.58032	.58057	.58081	.58105	.58130	.58154	.58179
.950	.58203	.58228	.58252	.58276	.58301	.58325	.58350	.58374	.58398	.58423	.58447	.58472	.58496	.58521	.58545	.58569
.960	.58594	.58618	.58643	.58667	.58691	.58716	.58740	.58765	.58789	.58813	.58838	.58862	.58887	.58911	.58936	.58960
.970	.58984	.59009	.59033	.59058	.59082	.59106	.59131	.59155	.59180	.59204	.59229	.59253	.59277	.59302	.59326	.59351
.980	.59375	.59399	.59424	.59448	.59473	.59497	.59521	.59546	.59570	.59595	.59619	.59644	.59668	.59692	.59717	.59741
.990	.59766	.59790	.59814	.59839	.59863	.59888	.59912	.59937	.59961	.59985	.60010	.60034	.60059	.60083	.60107	.60132
.9A0	.60156	.60181	.60205	.60229	.60254	.60278	.60303	.60327	.60352	.60376	.60400	.60425	.60449	.60474	.60498	.60522
.9B0	.60547	.60571	.60596	.60620	.60645	.60669	.60693	.60718	.60742	.60767	.60791	.60815	.60840	.60864	.60889	.60913
.9C0	.60937	.60962	.60986	.61011	.61035	.61060	.61084	.61108	.61133	.61157	.61182	.61206	.61230	.61255	.61279	.61304
.9D0	.61328	.61353	.61377	.61401	.61426	.61450	.61475	.61499	.61523	.61548	.61572	.61597	.61621	.61646	.61670	.61694
.9E0	.61719	.61743	.61768	.61792	.61816	.61841	.61865	.61890	.61914	.61938	.61963	.61987	.62012	.62036	.62061	.62085
.9F0	.62109	.62134	.62158	.62183	.62207	.62231	.62256	.62280	.62305	.62329	.62354	.62378	.62402	.62427	.62451	.62476

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
.A00	.62500	.62524	.62549	.62573	.62598	.62622	.62646	.62671	.62695	.62720	.62744	.62769	.62793	.62817	.62842	.62866
.A10	.62891	.62915	.62939	.62964	.62988	.63013	.63037	.63062	.63086	.63110	.63135	.63159	.63184	.63208	.63232	.63257
.A20	.63281	.63306	.63330	.63354	.63379	.63403	.63428	.63452	.63477	.63501	.63525	.63550	.63574	.63599	.63623	.63647
.A30	.63672	.63696	.63721	.63745	.63770	.63794	.63818	.63843	.63867	.63892	.63916	.63940	.63965	.63989	.64014	.64038
.A40	.64062	.64087	.64111	.64136	.64160	.64185	.64209	.64233	.64258	.64282	.64307	.64331	.64355	.64380	.64404	.64429
.A50	.64453	.64478	.64502	.64526	.64551	.64575	.64600	.64624	.64648	.64673	.64697	.64722	.64746	.64771	.64795	.64819
.A60	.64844	.64868	.64893	.64917	.64941	.64966	.64990	.65015	.65039	.65063	.65088	.65112	.65137	.65161	.65186	.65210
.A70	.65234	.65259	.65283	.65308	.65332	.65356	.65381	.65405	.65430	.65454	.65479	.65503	.65527	.65552	.65576	.65601
.A80	.65625	.65649	.65674	.65698	.65723	.65747	.65771	.65796	.65820	.65845	.65869	.65894	.65918	.65942	.65967	.65991
.A90	.66016	.66040	.66064	.66089	.66113	.66138	.66162	.66187	.66211	.66235	.66260	.66284	.66309	.66333	.66357	.66382
.AA0	.66406	.66431	.66455	.66479	.66504	.66528	.66553	.66577	.66602	.66626	.66650	.66675	.66699	.66724	.66748	.66772
.AB0	.66797	.66821	.66846	.66870	.66895	.66919	.66943	.66968	.66992	.67017	.67041	.67065	.67090	.67114	.67139	.67163
.AC0	.67187	.67212	.67236	.67261	.67285	.67310	.67334	.67358	.67383	.67407	.67432	.67456	.67480	.67505	.67529	.67554
.AD0	.67578	.67603	.67627	.67651	.67676	.67700	.67725	.67749	.67773	.67798	.67822	.67847	.67871	.67896	.67920	.67944
.AE0	.67969	.67993	.68018	.68042	.68066	.68091	.68115	.68140	.68164	.68188	.68213	.68237	.68262	.68286	.68311	.68335
.AF0	.68359	.68384	.68408	.68433	.68457	.68481	.68506	.68530	.68555	.68579	.68604	.68628	.68652	.68677	.68701	.68726
.B00	.68750	.68774	.68799	.68823	.68848	.68872	.68896	.68921	.68945	.68970	.68994	.69019	.69043	.69067	.69092	.69116
.B10	.69141	.69165	.69189	.69214	.69238	.69263	.69287	.69312	.69336	.69360	.69385	.69409	.69434	.69458	.69482	.69507
.B20	.69531	.69556	.69580	.69604	.69629	.69653	.69678	.69702	.69727	.69751	.69775	.69800	.69824	.69849	.69873	.69897
.B30	.69922	.69946	.69971	.69995	.70020	.70044	.70068	.70093	.70117	.70142	.70166	.70190	.70215	.70239	.70264	.70288
.B40	.70312	.70337	.70361	.70386	.70410	.70435	.70459	.70483	.70508	.70532	.70557	.70581	.70605	.70630	.70654	.70679
.B50	.70703	.70728	.70752	.70776	.70801	.70825	.70850	.70874	.70898	.70923	.70947	.70972	.70996	.71021	.71045	.71069
.B60	.71094	.71118	.71143	.71167	.71191	.71216	.71240	.71265	.71289	.71313	.71338	.71362	.71387	.71411	.71436	.71460
.B70	.71484	.71509	.71533	.71558	.71582	.71606	.71631	.71655	.71680	.71704	.71729	.71753	.71777	.71802	.71826	.71851
.B80	.71875	.71899	.71924	.71948	.71973	.71997	.72021	.72046	.72070	.72095	.72119	.72144	.72168	.72192	.72217	.72241
.B90	.72266	.72290	.72314	.72339	.72363	.72388	.72412	.72437	.72461	.72485	.72510	.72534	.72559	.72583	.72607	.72632
.BA0	.72656	.72681	.72705	.72729	.72754	.72778	.72803	.72827	.72852	.72876	.72900	.72925	.72949	.72974	.72998	.73022
.BB0	.73047	.73071	.73096	.73120	.73145	.73169	.73193	.73218	.73242	.73267	.73291	.73315	.73340	.73364	.73389	.73413
.BC0	.73437	.73462	.73486	.73511	.73535	.73560	.73584	.73608	.73633	.73657	.73682	.73706	.73730	.73755	.73779	.73804
.BD0	.73828	.73853	.73877	.73901	.73926	.73950	.73975	.73999	.74023	.74048	.74072	.74097	.74121	.74146	.74170	.74194
.BE0	.74219	.74243	.74268	.74292	.74316	.74341	.74365	.74390	.74414	.74438	.74463	.74487	.74512	.74536	.74561	.74585
.BF0	.74609	.74634	.74658	.74683	.74707	.74731	.74756	.74780	.74805	.74829	.74854	.74878	.74902	.74927	.74951	.74976
.C00	.75000	.75024	.75049	.75073	.75098	.75122	.75146	.75171	.75195	.75220	.75244	.75269	.75293	.75317	.75342	.75366
.C10	.75391	.75415	.75439	.75464	.75488	.75513	.75537	.75562	.75586	.75610	.75635	.75659	.75684	.75708	.75732	.75757
.C20	.75781	.75806	.75830	.75854	.75879	.75903	.75928	.75952	.75977	.76001	.76025	.76050	.76074	.76099	.76123	.76147
.C30	.76172	.76196	.76221	.76245	.76270	.76294	.76318	.76343	.76367	.76392	.76416	.76440	.76465	.76489	.76514	.76538
.C40	.76562	.76587	.76611	.76636	.76660	.76685	.76709	.76733	.76758	.76782	.76807	.76831	.76855	.76880	.76904	.76929
.C50	.76953	.76978	.77002	.77026	.77051	.77075	.77100	.77124	.77148	.77173	.77197	.77222	.77246	.77271	.77295	.77319
.C60	.77344	.77368	.77393	.77417	.77441	.77466	.77490	.77515	.77539	.77563	.77588	.77612	.77637	.77661	.77686	.77710
.C70	.77734	.77759	.77783	.77808	.77832	.77856	.77881	.77905	.77930	.77954	.77979	.78003	.78027	.78052	.78076	.78101
.C80	.78125	.78149	.78174	.78198	.78223	.78247	.78271	.78296	.78320	.78345	.78369	.78394	.78418	.78442	.78467	.78491
.C90	.78516	.78540	.78564	.78589	.78613	.78638	.78662	.78687	.78711	.78735	.78760	.78784	.78809	.78833	.78857	.78882
.CA0	.78906	.78931	.78955	.78979	.79004	.79028	.79053	.79077	.79102	.79126	.79150	.79175	.79199	.79224	.79248	.79272
.CB0	.79297	.79321	.79346	.79370	.79395	.79419	.79443	.79468	.79492	.79517	.79541	.79565	.79590	.79614	.79639	.79663
.CC0	.79687	.79712	.79736	.79761	.79785	.79810	.79834	.79858	.79883	.79907	.79932	.79956	.79980	.80005	.80029	.80054
.CD0	.80078	.80103	.80127	.80151	.80176	.80200	.80225	.80249	.80273	.80298	.80322	.80347	.80371	.80396	.80420	.80444
.CE0	.80469	.80493	.80518	.80542	.80566	.80591	.80615	.80640	.80664	.80688	.80713	.80737	.80762	.80786	.80811	.80835
.CF0	.80859	.80884	.80908	.80933	.80957	.80981	.81006	.81030	.81055	.81079	.81104	.81128	.81152	.81177	.81201	.81226
.D00	.81250	.81274	.81299	.81323	.81348	.81372	.81396	.81421	.81445	.81470	.81494	.81519	.81543	.81567	.81592	.81616
.D10	.81641	.81665	.81689	.81714	.81738	.81763	.81787	.81812	.81836	.81860	.81885	.81909	.81934	.81958	.81982	.82007
.D20	.82031	.82056	.82080	.82104	.82129	.82153	.82178	.82202	.82227	.82251	.82275	.82300	.82324	.82349	.82373	.82397
.D30	.82422	.82446	.82471	.82495	.82520	.82544	.82568	.82593	.82617	.82642	.82666	.82690	.82715	.82739	.82764	.82788
.D40	.82812	.82837	.82861	.82886	.82910	.82935	.82959	.82983	.83008	.83032	.83057	.83081	.83105	.83130	.83154	.83179
.D50	.83203	.83228	.83252	.83276	.83301	.83325	.83350	.83374	.83398	.83423	.83447	.83472	.83496	.83521	.83545	.83569
.D60	.83594	.83618	.83643	.83667	.83691	.83716	.83740	.83765	.83789	.83813	.83838	.83862	.83887	.83911	.83936	.83960
.D70	.83984	.84009	.84033	.84058	.84082	.84106	.84131	.84155	.84180	.84204	.84229	.84253	.84277	.84302	.84326	.84351
.D80	.84375	.84399	.84424	.84448	.84473	.84497	.84521	.84546	.84570	.84595	.84619	.84644	.84668	.84692	.84717	.84741
.D90	.84766	.84790	.84814	.84839	.84863	.84888	.84912	.84937	.84961	.84985	.85010	.85034	.85059	.85083	.85107	.85132
.DA0	.85156	.85181	.85205	.85229	.85254	.85278	.85303	.85327	.85352	.85376	.85400	.85425	.85449	.85474	.85498	.85522
.DB0	.85547	.85571	.85596	.85620	.85645	.85669	.85693	.85718	.85742	.85767	.85791	.85815	.85840	.85864	.85889	.85913
.DC0	.85937	.85962	.85986	.86011	.86035	.86060	.86084	.86108	.86133	.86157	.86182	.86206	.86230	.86255	.86279	.86304
.DD0	.86328	.86353	.86377	.86401	.86426	.86450	.86475	.86499	.86523	.86548	.86572	.86597	.86621	.86646	.86670	.86694
.DE0	.86719	.86743	.86768	.86792	.86816	.86841	.86865	.86890	.86914	.86938	.86963	.86987	.87012	.87036	.87061	.87085
.DF0	.87109	.87134	.87158	.87183	.87207	.87231	.87256	.87280	.87305	.87329	.87354	.87378	.87402	.87427	.87451	.87476
.E00	.87500	.87524	.87549	.87573	.87598	.87622	.87646	.87671	.87695	.87720	.87744	.87769	.87793	.87817	.87842	.87866
.E10	.87891	.87915	.87939	.87964	.87988	.88013	.88037	.88062	.88086	.88110	.88135	.88159	.88184	.88208	.88232	.88257
.E20	.88281	.88306	.88330	.88354	.88379	.88403	.88428	.88452	.88477	.88501	.88525	.88550	.88574	.88599	.88623	.88647
.E30	.88672	.88696	.88721	.88745	.88770	.88794	.88818	.88843	.88867	.88892	.88916	.88940	.88965	.88989	.89014	.89038
.E40	.89062	.89087	.89111	.89136	.89160	.89185	.89209	.89233	.89258	.89282	.89307	.89331	.89355	.89380	.89404	.89429
.E50	.89453	.89478	.89502	.89526	.89551	.89575	.89600	.89624	.89648	.89673	.89697	.89722	.89746	.89771	.89795	.89819
.E60	.89844	.89868	.89893	.89917	.89941	.89966	.89990	.90015	.90039	.90063	.90088	.90112	.90137	.90161	.90186	.90210
.E70	.90234	.90259	.90283	.90308	.90332	.90356	.90381	.90405	.90430	.90454	.90479	.90503	.90527	.90552	.90576	.90601
.E80	.90625	.90649	.90674	.90698	.90723	.90747	.90771	.90796	.90820	.90845	.90869	.90894	.90918	.90942	.90967	.90991
.E90	.91016	.91040	.91064	.91089	.91113	.91138	.91162	.91187	.91211	.91235	.91260	.91284	.91309	.91333	.91357	.91382
.EA0	.91406	.91431	.91455	.91479	.91504	.91528	.91553	.91577	.91602	.91626	.91650	.91675	.91699	.91724	.91748	.91772
.EB0	.91797	.91821	.91846	.91870	.91895	.91919	.91943	.91968	.91992	.92017	.92041	.92065	.92090	.92114	.92139	.92163
.EC0	.92187	.92212	.92236	.92261	.92285	.92310	.92334	.92358	.92383	.92407	.92432	.92456	.92480	.92505	.92529	.92554
.ED0	.92578	.92603	.92627	.92651	.92676	.92700	.92725	.92749	.92773	.92798	.92822	.92847	.92871	.92896	.92920	.92944
.EE0	.92969	.92993	.93018	.93042	.93066	.93091	.93115	.93140	.93164	.93188	.93213	.93237	.93262	.93286	.93311	.93335
.EF0	.93359	.93384	.93408	.93433	.93457	.93481	.93506	.93530	.93555	.93579	.93604	.93628	.93652	.93677	.93701	.93726

HEXADECIMAL - TO - DECIMAL FRACTION TABLE (CONT.)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
.F00	.93750	.93774	.93799	.93823	.93848	.93872	.93896	.93921	.93945	.93970	.93994	.94019	.94043	.94067	.94092	.94116
.F10	.94141	.94165	.94189	.94214	.94238	.94263	.94287	.94312	.94336	.94360	.94385	.94409	.94434	.94458	.94482	.94507
.F20	.94531	.94556	.94580	.94604	.94629	.94653	.94678	.94702	.94727	.94751	.94775	.94800	.94824	.94849	.94873	.94897
.F30	.94922	.94946	.94971	.94995	.95020	.95044	.95068	.95093	.95117	.95142	.95166	.95190	.95215	.95239	.95264	.95288
.F40	.95312	.95337	.95361	.95386	.95410	.95435	.95459	.95483	.95508	.95532	.95557	.95581	.95605	.95630	.95654	.95679
.F50	.95703	.95728	.95752	.95776	.95801	.95825	.95850	.95874	.95898	.95923	.95947	.95972	.95996	.96021	.96045	.96069
.F60	.96094	.96118	.96143	.96167	.96191	.96216	.96240	.96265	.96289	.96313	.96338	.96362	.96387	.96411	.96436	.96460
.F70	.96484	.96509	.96533	.96558	.96582	.96606	.96631	.96655	.96680	.96704	.96729	.96753	.96777	.96802	.96826	.96851
.F80	.96875	.96899	.96924	.96948	.96973	.96997	.97021	.97046	.97070	.97095	.97119	.97144	.97168	.97192	.97217	.97241
.F90	.97266	.97290	.97314	.97339	.97363	.97388	.97412	.97437	.97461	.97485	.97510	.97534	.97559	.97583	.97607	.97632
.FA0	.97656	.97681	.97705	.97729	.97754	.97778	.97803	.97827	.97852	.97876	.97900	.97925	.97949	.97974	.97998	.98022
.FB0	.98047	.98071	.98096	.98120	.98145	.98169	.98193	.98218	.98242	.98267	.98291	.98315	.98340	.98364	.98389	.98413
.FC0	.98437	.98462	.98486	.98511	.98535	.98560	.98584	.98608	.98633	.98657	.98682	.98706	.98730	.98755	.98779	.98804
.FD0	.98828	.98853	.98877	.98901	.98926	.98950	.98975	.98999	.99023	.99048	.99072	.99097	.99121	.99146	.99170	.99194
.FE0	.99219	.99243	.99268	.99292	.99316	.99341	.99365	.99390	.99414	.99438	.99463	.99487	.99512	.99536	.99561	.99585
.FF0	.99609	.99634	.99658	.99683	.99707	.99731	.99756	.99780	.99805	.99829	.99854	.99878	.99902	.99927	.99951	.99976

RAYTHEON

March 25, 1968

ERRATA SHEET
703 REFERENCE AND INTERFACE MANUAL
SP-248B

PAGE	LOCATION	CHANGE
1-6	3rd Paragraph	Replace with: The EXR may point to any page merely by setting its contents to the selected page number. This may easily be accomplished by execution of either of the literal instructions, SML (Set Memory Lower) or SMU (Select Memory Upper). Typically, the extension register, or page pointer, references the current page from which instructions are executed. This is predominant, since every memory reference forces the EXR to be set to the local page, the page containing the next instruction to be executed. This feature permits ease of local address operations, since frequent global memory references, i.e., memory references outside the local page, are usually made in an indexed mode in which case the EXR is not used. The extension register is most effective when used for local addressing and single-reference addressing outside the current page. Infrequent global memory references are conveniently made by utilizing the extension register and the SML/SMU instructions in coordination with the memory reference instruction. Thus, the index register is

PAGE	LOCATION	CHANGE
1-6	3rd Paragraph	Continued: reserved for its primary purpose, indexed operations where a multitude of data is being processed.
	4th Paragraph	Add: Direct and Indexed Local provide addressing within the current page or single reference addressing outside the current page. In the latter case one of the SMU/SML instructions is used to select page prior to the memory reference. Indexed Global provides an efficient method of referencing multi-data located anywhere in memory.
2-15	2-7.6	Add to paragraph: One machine cycle is required for instruction set up. In addition the following time is required: 1-4 bit shift, 5-9 bit shift, 10-14 bit shift, and 15 bit shift are 1 cycle, 2 cycles, 3 cycles and 4 cycles, respectively.
4-2	4-2.2.1	Change 530724-500 to 530724-005.
4-3	Table 4-1	In second column: change KEXT- to KEXT1-, REXT- to REXT1-, and INTRPT- to IRPT-.
4-4	Figure 4-2	Change plus 5V to plus 3.6V. Delete line between connector below 120 ohm resistor and connector to minus side of 22 μfd capacitor. Change 100 ft. to 50 ft.
4-5	Figure 4-3	Change plus 5V to plus 3.6V. Delete line between connector below 120 ohm resistor and connector to minus side of 22 μfd capacitor.
	Figure 4-4	Replace with attached Figure 4-4.

PAGE	LOCATION	CHANGE
4-8	Table 4-2	In second column: change MT0- to DMT0-, MT2- to DMT2-, MT4- to DMT4-, KEXT- to KEXT2-, and REXT- to REXT2-.
6-2	Second and Third Lines	Delete "No." Capitalize "overflow". Delete period following instruction. Add "when a maximum negative number is multiplied by a maximum negative multiplier".
	Last Paragraph	Replace "set to the most significant bit of the index register" with "indeterminate".
A-1	IXS	Insert after "than", "or equal".
	JXS	Replace "2" cycles with "1". Replace "3.5" with "1.75".
	LDW	Change "Work" to "Word".
B-1	2	Replace "2" cycles with "1". Replace "3.5" with "1.75".
	04	Insert after "than", "or equal".

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