DIFFERENCES BETWEEN POLY 88 BUS AND ALTAIR 8800 OR IMSAI 8080 BUS

Front-panel Control Signals - a number of signals generated or used by the Altair/Imsai front panel are not used by the POLY 88 system. These include 21(UNPROT), 22(SS), 53(SSWI-), 54(EXTCLR), 56(STSTB), 57(FRDY), 69(PS-), 70(PROT), and 71(RUN).

Status Signals - Four status signals defined in the Altair/Imsai bus are not present in the POLY 88. The SSTACK (98) signal is not generated and the SM1(44) signal is used only internally on the processor card. The PWAIT (pin 27) and PINTE (pin 28) signal are not brought out to the bus but are available as test points on the CPU card.

DMA Control Signals - In the POLY 88 system the DMA (direct memory access) is not controlled as in the Altair or IMSAI. The POLY 88 CPU may continue processing during DMA cycles by using it onboard memory and I/O. This also allows more than one processor card to share a common bus (backplane) with little conflict.

Bus contention for DMA and multiprocessing is handled by the DMA/multiprocessing controller card. The control lines defined in the Altair/Imsai may be used but go to the controller and are not present on the CPU card. Pins 18 (STAT DSB-), 19(C/S DSB-), 22 (ADDR DSB-), 23 (DO DSB-), 26 (PHLDA), and 74 (PHOLD-) are affected.

POLY-88 BUS

1	+8V	Unregulated voltage, regulated to +5V on card
2	+16V	Unregulated voltage, regulated to +12V on car
3	XRDY+	External ready--ready input to CPU
4	VIØ-	Vectored interrupt line
5	VI1-	Vectored interrupt line
6	VI2-	Vectored interrupt line
7	VI3-	Vectored interrupt line
8	VI4-	Vectored interrupt line
9	VI5-	Vectored interrupt line
10	VI6-	Vectored interrupt line
11	VI7-	Vectored interrupt line
12	XRDY2	External ready 2
13	--	Reserved for bus control
14	--	Reserved for bus control
15	--	Reserved for bus control
16	--	Reserved for bus control
17	--	Reserved for bus control
18	--	Reserved for bus control
19	--	Reserved for bus control
20	--	Unused
21	--	Unused
22	--	Reserved for bus control
23	--	Reserved for bus control
24	Ø2+	Phase 2 clock from CPU

25	Ø1+	Phase 1 clock from CPU
26	--	Reserved for bus control
27	--	Unused
28	--	Unused
29	A5+	Address line
30	A4+	Address line
31	A3+	Address line
32	A15+	Address line
33	A12+	Address line
34	A9+	Address line
35	DO1+	Data out line
36	DOØ+	Data out line
37	AlØ+	Address line
38	DO4+	Data out line
39	DO5+	Data out line
40	DO6+	Data out line
41	DI2+	Data in line
42	DI3+	Data in line
43	DI7+	Data in line
44	--	Unused
45	SOUT+	Output -- during this machine cycle data is transferred from the CPU to an output port.
46	SINP+	Input -- during this machine cycle data is transferred from an input port to CPU.
47	SMEMR+	Memory read cycle
48	SHLTA+	Halt -- CPU has entered a halt
49	CLOCK-	Phase 2 clock
50	GND	System ground

51	+8V	Unregulated voltage regulated on card to +5V
52	-16V	Unregulated voltage regulated on card to -12V or -5V
53	--	Unused
54	--	Unused
55	RTC+	Real time clock--half wave rectified 50/60 Hz signal
56	--	Unused
57	--	Unused
58	--	Unused
59	--	Reserved
60	--	Reserved
61	--	Reserved
62	--	Reserved
63	--	Reserved for MP/DMA controller
64	--	Reserved for MP/DMA controller
65	--	Reserved for MP/DMA controller
66	--	Reserved for MP/DMA controller
67	PHANTOM-	Used to disable RAM and I/O addressing
68	MWRTTE+	Memory--write strobe for memory cycle
69	--	Unused
70	--	Unused
71	--	Unused
72	PRDY+	Processor ready--ready input to CPU
73	PINT-	Processor Interrupt--used only with external interrupt controller
74	--	Reserved for bus control
75	PRESET-	Reset--from front bus control panel push-button--set PC to 0

76	PSYNC+	Sync--identifies beginning of machine cycle
77	PWR-	Write--CPU write strobe
78	PDBIN+	Data in--CPU read strobe
79	AØ+	Address line
80	A1+	Address line
81	A2+	Address line
82	A6+	Address line
83	A7+	Address line
84	A8+	Address line
85	A13+	Address line
86	A14+	Address line
87	A11+	Address line
88	DO2+	Data out line
89	DO3+	Data out line
90	DO7+	Data out line
91	DI4+	Data in line
92	DI5+	Data in line
93	DI6+	Data in line
94	DI1+	Data in line
95	DIØ+	Data in line
96	SINTA+	Interrupt acknowledge cycle
97	SWO-	Write/output--machine cycle to write to memory or output to port
98	--	Unused
99	POC-	Power on clear--generated by PRESET+ or power turn on used to reset CPU and I/O devices.
100	GND	System ground