# MicroMate

## Technical Manual

Personal Micro Computers, Inc. 475 Ellis St. Mt. View, CA 94043 (415) 962-0220

Personal Micro Computers, Inc.

# MicroMate Technical Manual

## MODEL PMC-101

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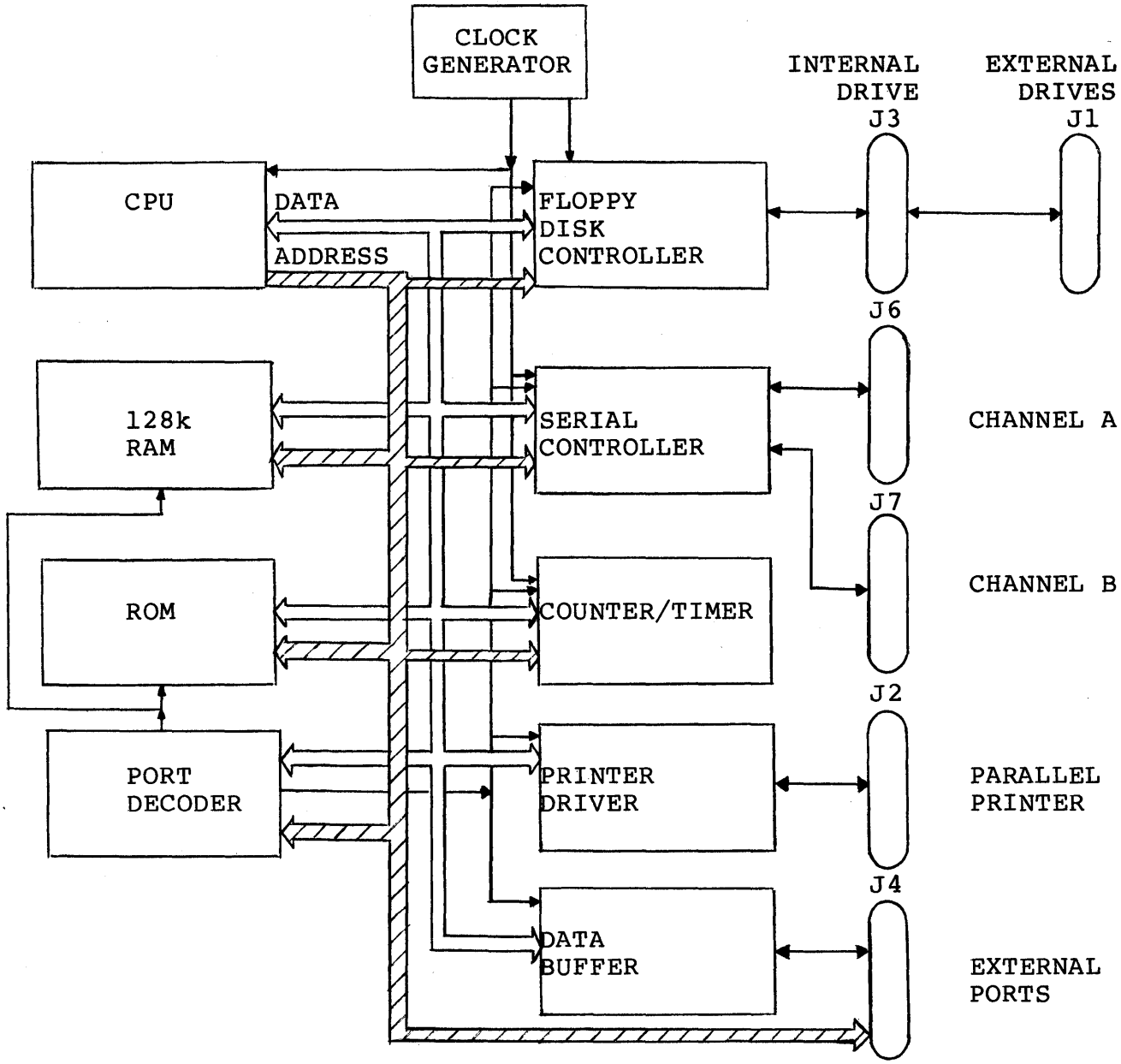


FIGURE 1

MicroMate BLOCK DIAGRAM

# SECTION 1

# THEORY OF OPERATION

## 1.1 Sheet 1 of 3 (SCHEMATIC 10-0303)

### 1.1.1 CPU AND BUFFERS

Z29 is the Z80A CPU with D0 through D7 being the eight bi-directional data lines and A0 through A15 being the sixteen address lines. The remaining lines form the various control signals. ICs Z27 and Z28 buffer the address lines from the CPU. One half of IC Z40 and one half of IC Z22 form the control line buffers.

### 1.1.2 RESET AND CLOCK

The front panel reset switch is tied to IC Z24 which forms a de-bounce latch. The latch output (Z24 pin 6) goes to one input of reset gate Z20. The other input to Z20 is from the power-on RC time delay circuit formed by R21 and C25. When either of these inputs to Z20 is low (ie, reset switch depressed or power-on) the output of Z20 at pin 8 goes to a low level which resets the CPU and all associated circuitry.

The system clock is derived from a 4.0 MHZ clock input to one gate of buffer IC Z22. The output of this gate (Z22 pin 5) goes to a clock driver formed by Z26, Q1 and associated components. The output of this clock driver is an NMOS compatible 4.0 MHZ clock as required by the CPU and its peripherals.

### 1.1.3 EPROM AND MEMORY DECODE

ICs Z38, Z42, Z43 and Z44 form the memory decode section. The purpose of the memory decoder is to select the appropriate memory device (EPROM, main RAM or banked RAM) in response to the CPU address lines during a memory request. IC Z42 pins 9 (main RAM) 10 (EPROM) and 11 (banked RAM) select the device depending upon the status of input pins 13 and 14 during a memory request (pin 15).

IC Z38 pin 8 (connected to Z42 pin 14) is a low level when address lines 12 through 15 are low (hex addresses 0000 through 07FF) and the EPROM is enabled (Z38 pin 10 is at a low level).

IC Z44 pin 6 (connected to Z42 pin 13) is a low level when bank select is enabled ( Z44 pins 1, 2 and 4 are at a high level) and Z44 pin 8 is at a high level. Z44 pin 8 goes to a high level in response to any of the three outputs of Z43 being low (pins 3, 6 or 11). The outputs of Z43 are conditioned by three jumpers (JP1, JP2 and JP3) and output pins 4, 5 and 6 of Z42. Z42 output pins are low in response to the state of address lines 14 and 15 from the CPU as follows:

| ADDRESS | | Z42 OUTPUTS | | | ADDRESS | Z43 |
|---|---|---|---|---|---|---|
| 15 | 14 | 4 | 5 | 6 | RANGE (HEX) | JUMPER |
| 0 | 0 | 0 | 1 | 1 | 0000 - 3FFF | JP1 |
| 0 | 1 | 1 | 0 | 1 | 4000 - 7FFF | JP2 |
| 1 | 0 | 1 | 1 | 0 | 8000 - BFFF | JP3 |
| 1 | 1 | ------ not used---------- | | | | |

TABLE 1

The MicroMate has JP2 and JP3 installed. As can be seen from the table above, when bank select is enabled, the output at Z44 pin 6 will go low over the hex address range of 4000 to BFFF.

IC Z35 is a 32K EPROM which is enabled by Z25 pin 5 and Z42 pin 10 both being low. When Z35 is enabled it places data selected by the address lines on the data lines to be read by the CPU. Z35 is always selected after a power-on sequence or after the front panel reset button has been depressed via the reset signal to IC Z20 pin 5.

### 1.1.4 I/O PORT DECODE

ICs Z15, Z16, Z20 and Z21 form the I/O port decode section. The read and write signals from the CPU are OR'D together at Z20 pin 11 which is ANDED at Z16 pin 8 with the CPU I/O request to form one of the select inputs to IC Z21 (pin 4). The other two select inputs to Z21 are CPU addresses 6 and 7 which must be low and high respectively along with a low at pin 4 to select an I/O port. The I/O port selected is determined by CPU addresses 2, 3 and 4 on pins 1, 2 and 3 of Z21. Since CPU addresses 0 and 1 are not decoded by Z21, each I/O port selected has four addresses available for further decoding. An example of this is Z15, when pin 1 is low (from Z21 pin 11) CPU addresses 0 and 1 on pins 2 and 3 are decoded to determine which output is selected (pins 4, 5, 6 or 7).

Z21 output decoding is as follows:

| Z21 PIN NUMBER | ADDRESS RANGE (HEX) | *READ/ WRITE | FUNCTION |
|---|---|---|---|
| 15 | 80 THRU 83 | R/W | FLOPPY DISK CONTROLLER |
| 14 | 84 THRU 87 | W | FLOPPY DRIVE SELECT |
| 13 | 88 THRU 8B | R/W | SERIAL INTERFACE |
| 12 | 8C THRU 8F | R/W | PARALLEL PRINTER |
| 11 | 90 THRU 93 | --- | SEE Z15 DESCRIPTION |
| 10 | 94 THRU 97 | R | BANK/BAUD RATE STATUS |
| 9 | 98 THRU 9B | --- | ---NOT USED------ |
| 8 | 9C THRU 9F | R/W | COUNTER / TIMER |

TABLE 2

Z15 output decoding is as follows:

| Z15 PIN NUMBER | ADDRESS (HEX) | *READ/ WRITE | FUNCTION |
|---|---|---|---|
| 4 | 90 | R/W | DISABLE EPROM |
| 5 | 91 | R/W | ENABLE EPROM |
| 6 | 92 | W | SET BANKS |
| 7 | 93 | W | SET SERIAL BAUD RATES |

*note: R/W for explanatory purpose only.
Outputs will select for an I/O read OR write.

TABLE 3

Notice that CPU address 7 must be high during I/O to select Z21. This reserves the top 128 I/O ports for MicroMate use (ports 80 through FF hex).

### 1.1.5 PARALLEL PRINTER

ICs Z4, Z5, Z6 and Z12 form the parallel printer port which is connected to card edge connector J2.

During a read from port 8C hex, IC Z12 pin 1 is enabled by IC Z5 pin 3 which places the printer status (busy, paper empty, select and fault) on data lines D7 through D4 (respectivly) allowing it to be read by the CPU.

When the CPU writes to the printer (port 8C hex) it places the data to be sent on data lines D0 through D7. At the end of the write command, IC Z5 pin 11 goes from a low level to a high level which latches the data (D0 through D7) into IC Z6 and at the same time triggers one-shot IC Z4. Pin 4 of IC Z4 then goes to a low level for approximately 2 micro-seconds (pulse) which strobes the data on the output of IC Z6 into the printer.

### 1.1.6 EXTERNAL PARALLEL PORTS

ICs Z5, Z7 and Z16 form the control for the external ports connected to J4. IC Z16 pin 6 goes low and enables the external ports during a CPU I/O request when address line 7 is low. Buffered address lines 0 through 6 are brought out to connector pins of J4 thus allowing an external device connected to these pins to decode 128 individual I/O ports (ports 00 through 7F hex).

During an I/O write to an external port, IC Z5 pin 8 (J4 pin 19) goes to a low level which informs the external device connected to J4 to accept the data present at the outputs of IC Z7.

During an I/O read from an external port, IC Z5 pin 6 (J4 pin 17) goes to a low level which performs two functions. The first function is to change IC Z7 from an output device to an input device . This action places the data lines at J4 onto the CPU data lines (D0 through D7). The second function is to inform the external device to present data ( D0 through D7) to IC Z7 at J4.

The external port connector (J4) outputs RESET, +5 volts, +12 volts, -12 volts and ground for external device use. The external device using the voltages should not exceed the current limits as follows:

| | |
|---|---|
| +5 volts | 1.0 amp max. |
| +12 volts | 250 milliamps max. |
| -12 volts | 250 milliamps max. |

TABLE 4

J4 has one input signal called TRG1 (pin 21). This input is routed to one channel of the COUNTER/TIMER IC (Z30 sheet 2) for use as a general purpose clock or trigger input under user created program control.

## 1.2 Sheet 2 of 3 (SCHEMATIC 10-0303)

### 1.2.1 128k RAM MEMORY

The MicroMate uses 16 64k RAM ICs (Z47 through Z54 and Z56 through Z64) arranged in two rows of 8 RAMs each to achieve 128k of total RAM memory. This arrangement is necessary as each 64k RAM IC has only one input and one output bit therefore, 8 RAMs are required to supply D0 through D7 to the CPU. The RAM arrangement is as follows:

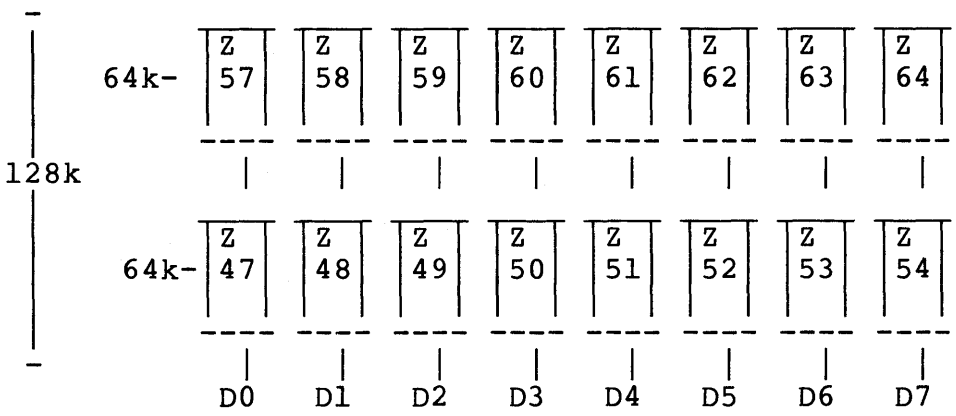


FIGURE 2

Each 64k RAM stores data bits in a matrix of 256 rows by 256 columns. Data bits are accessed by first applying a row address and strobe followed by a column address and strobe (ie, 0,0 = bit at row 0, column 0 ; 1,0 = bit at row 1, column 0 ; etc.).

In the MicroMate the row and column addresses are generated by address multiplexers Z45 and Z46 for rams Z47 through Z54 and multiplexers Z55 and Z56 for rams Z57 through Z64. Pin 1 of each multiplexer controls which eight address lines are applied to the rams. When pin 1 is low the row address is output and when pin 1 is high the column address is output. Pin 10 of multiplexer Z55 is connected to IC Z34 pin 16. Z34 is the bank select control port (92 hex). When Z34 pin 15 is set to a high level by data bit 7 (D7) of I/O port 92, bank select is enabled. Data bit 1 (D1) of I/O port 92 then sets the state of Z34 pin 16 which controls the most significant bit of the column address for rams Z57 through Z64. This divides these 64k rams in half giving program control over which 32k section is accesed.

### 1.2.1 128k RAM MEMORY (cont)

ICs Z39, Z40 and Z41 generate the multiplexer and strobe timing. Z40 is a buffer for clock and control signals from the CPU. Upon receipt of a memory request from the CPU, Z40 pin 3 outputs the row address strobe to the ram. At the next rising edge of the buffered CPU clock from Z40, Z39 latches the state of memory request at pins 8 and 9. As memory request is an active low signal, pin 9 will go low and pin 8 will go high. Z39 pin 8 going to a high level causes the address multiplexers to change from row address output to column address output. The buffered CPU clock from Z40 then gets inverted by transistor Q2 and applied to Z39 pin 3. At the next rising edge of the inverted clock at pin 3, Z39 latches the state at pin 2 (from Z39 pin 9) on output pin 5. When Z39 pin 5 goes low, it is steered by the memory decoder through IC Z41 pins 6 and 8 to generate the column address strobe for the selected ram. If the memory request is a write function, Z41 steers the buffered write signal from Z40 pin 5 to the selected ram at pins 3 and 11. The CPU generates a row refresh address to insure that data is retained in the ram memory. The REFRESH signal is buffered by Z40 and applied to Z39 pin 10 which forces Z39 pin 9 to remain at a high level as long as the REFRESH signal is present. This prevents Z39 from responding to the memory request during refresh time so the multiplexer addresses are held at the row address state.

### 1.2.2 COUNTER/TIMER

IC Z30 is a four channel counter/timer that is fully under program control. CPU access to Z30 is at I/O ports 9C through 9F hex. In the MicroMate, Z30 is programmed to generate IM2 mode interrupts for the real time clock, upon a transition on pin 22 (external port trigger) and after approximately ten transitions on pin 21 (index pulses from the disk drive). The interrupt generated by pin 21 transitions will cause the disk drive motors to turn off if no further disk accesses are pending (this is done under program control). The IEI line (Z30 pin 13) is used to form an interrupt priority chain with IC Z31 for CPU interrupts.

### 1.2.3 SERIAL I/O

IC Z31 is a dual channel serial receiver/transmitter which is under program control. CPU access to Z31 is at I/O ports 88 through 8B hex. The channel A serial input, serial output and controls are through ICs Z32 and Z33 (level converters) which are connected to J6. The channel B serial input, serial output and controls are through ICs Z36 and Z37 (level converters) which are connected to J7.

The data (baud) rate of Z31 is set individually for channels A and B by the baud rate generator IC Z17. Pin 17 output of Z17 sets the channel A baud rate and pin 3 output of Z17 sets the channel B rate. The baud rates are selected at Z17 by the output of latch Z13 which is located at I/O port 93 hex. The CPU, under program control, sets the baud rates by writing data bits D0 through D7 to I/O port 93. Data bits D0 through D3 set the channel B baud rates while data bits D4 through D7 set channel A.

Port decoder IC Z15 allows the CPU to read the status of the bank select at port 94 hex through IC Z22 and to read the current baud rate setting at port 95 hex through IC Z23.

## 1.3 Sheet 3 of 3 (SCHEMATIC 10-0303)

### 1.3.1 5 1/4 INCH DISK CONTROLLER

IC Z18 and crystal Y2 form a 4.0 MHZ oscillator which supplies the clock for the CPU clock driver and, through divider IC Z19, a 1.0 MHZ clock for the disk controller IC Z10.

Z10 is a floppy disk controller interface IC which performs the data translation and timing required to allow the CPU to store and retrieve information on a 5 1/4 inch floppy disk drive. Z10 is accessed by the CPU at I/O ports 80 through 83 hex and is fully under program control.

ICs Z8 (voltage controlled oscillator), Z9 (data seperator/write precompensation) and Z14 (4 phase clock generator) work in conjunction with Z10 to insure proper timing of read and write data sent to the disk drive. IC Z1 forms constant read and write pulse widths into and out of the disk drive. IC Z4 pins 10 and 12 provide a time delay to Z10 prior to all initial disk accesses to insure the disk drive is ready for operation with head(s) loaded, thus, no head load delay need be specified in software.

Three control lines from Z10 (pins 15, 16 and 25) control the disk drive head motion and side select. The outputs of IC Z11 control the drive select and motor-on lines to the disk drives. Z11 pin 6 output sets the desired data density (single or double) to Z9 and Z10. Z11 outputs are set through IC Z16 pin 11 by a CPU write to I/O port 84 hex.

All outputs to the disk drives connected to card edge connector J1 or internal connector J3 are through ICs Z2 and Z3. Z2 and Z3 are open collector inverters which allow up to four disk drives to be connected in parallel. The first disk drive (drive 0) is assigned to the internal MicroMate drive connected to J3. All other disk drives are connedted to J1. Only one disk drive is allowed to be active (selected) at a time to avoid conflict of data and status signals. When connecting external disk drives to J1, the proper drive select jumper must be set (1, 2 or 3) in the added disk drive. All external disk drives must have their signal and control line terminating resistors removed as the internal MicroMate disk drive contains the required terminators and double line terminations are not allowed.

There are three adjustments for the floppy disk controller that are set as follows:

Z8 VCO (set with no drive activity):

1st) Adjust R10 for 1.4 VDC at pin 2 of Z8.

2nd) Adjust R11 for a frequency of 2.0 MHZ at pin 7 of Z8.

1.3.1 5 1/4 INCH DISK CONTROLLER (cont)

Z14 CLOCK GENERATOR (set with disk writing data to a track number greater than 43):

Adjust R18 for the desired write precompensation value by observing the pulse width at pin 7 of Z14. The observed pulse width will be the precomp delay (typically 100 to 300 nanoseconds).

NOTE : The Z8 VCO adjustments (R10 and R11) are factory pre-set and no adjustment should be necessary. The Z14 CLOCK GENERATOR adjustment is NOT factory pre-set as the MicroMate disk drive is a 40 TRACK disk drive which does not require write precompensation.

SECTION 2

## 2.0 MEMORY MAP

The CPU has an address range of 64k, from 0000 to FFFF hex. This is reffered to as the LOGICAL address space of the CPU. The MicroMate has 128k of RAM memory and 32k (4k by 8 bits) of EPROM memory which, under program control, is mapped into the CPU's LOGICAL address space. The EPROM and each 64k row of RAM (the two rows comprising 128k total) have individual address and control signals to which they respond and are reffered to as the PHYSICAL address for each device. It is up to the program to map the correct PHYSICAL device into the CPU's LOGICAL address space. In the MicroMate, this mapping function is controlled by the operating system and is totally transparent to the user.

The memory map below shows the CPU's LOGICAL address along with each PHYSICAL device (along with the PHYSICAL address and control) which may be mapped into this space :

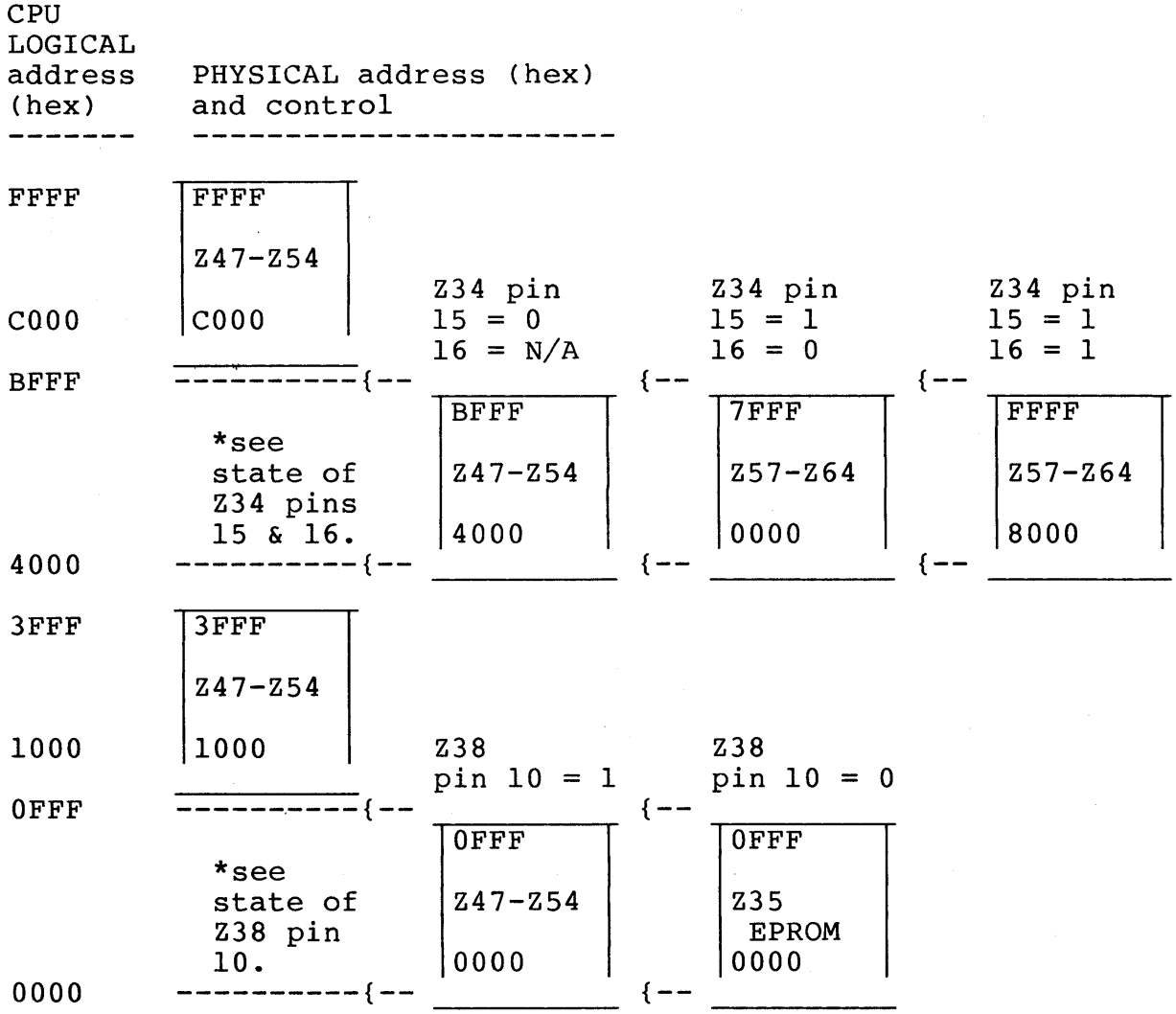


FIGURE 3

# APPENDIX A

SUGGESTED REFERENCE MATERIAL-

a) ZILOG Technical Manuals — ZILOG Part Number

| | |
|---|---|
| Z80 CPU | 03-0029-01 |
| Z8430 CTC | 03-0036-02 |
| Z80 SIO | 03-3033-01 |

b) ZILOG Product Specs. — ZILOG Part Number

| | |
|---|---|
| Z8400 Z80 CPU | 00-2001-02 |
| Z8430 CTC | 00-2041-A0 |
| Z8440 SIO | 00-2042-A0 |
| Z8470 DART | 00-2044-A0 |

c) WESTERN DIGITAL 1983 Components Handbook

d) MicroMate User's Guide

# APPENDIX A

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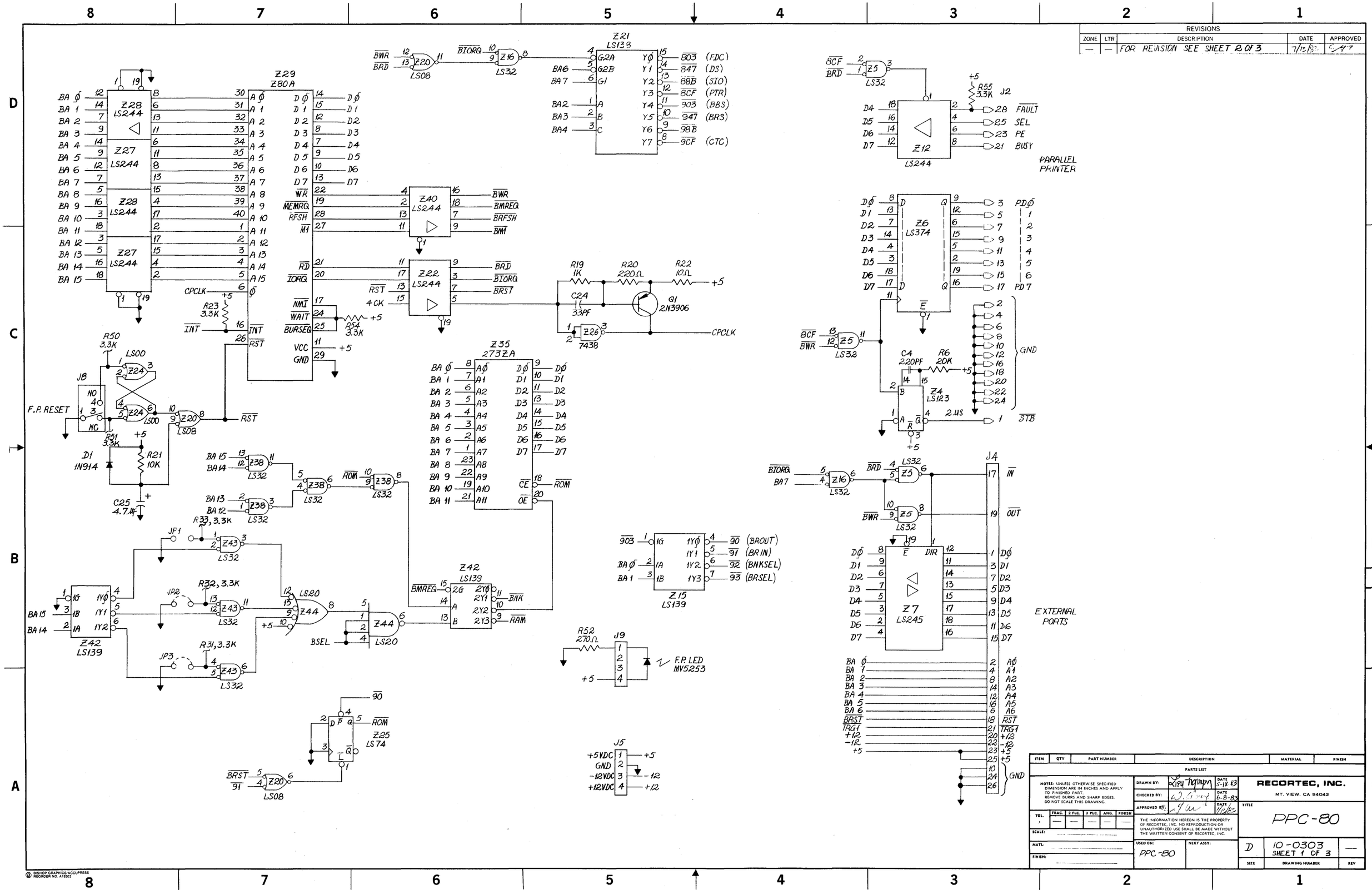
# APPENDIX B

SCHEMATIC DIAGRAM 10-0303



REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
— | — | FOR REVISION SEE SHEET 2 OF 3 | 7/13/83 | 547
Z29 Z80A
Z28 LS244
Z27 LS244
Z21 LS138
Z40 LS244
Z22 LS244
Z35 273ZA
Z42 LS139
Z15 LS139
Z12 LS244
Z6 LS374
Z4 LS123
Z7 LS245
Z25 LS74
Q1 2N3906
PARALLEL PRINTER
EXTERNAL PORTS
F.P. RESET
F.P. LED MV5253
J4
J5
J8
J9
J2
GND
STB
IN
OUT
+5VDC
GND
-12VDC
+12VDC
PARTS LIST
ITEM | QTY | PART NUMBER | DESCRIPTION | MATERIAL | FINISH
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APPROVED BY: DATE 7/12/83
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|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APPROVED |
| -- | -- | FOR REVISION SEE SHEET 2 OF 3 | 7/13/83 | |

Z46 LS157 — BA Ø, BA 1, BA 2, BA 3, BA 8, BA 9, BA 10, BA 11 → OA, OB, OC, OD, 1A, 1B, 1C, 1D; A, B, C, D; Ē, S; R34 1RAØ, R35 1RA1, R36 1RA2, R38 1RA3, 33Ω (X4); Ē → RASEL

Z45 LS157 — BA 4, BA 5, BA 6, BA 7, BA 12, BA 13, BA 14, BA 15 → OA, OB, OC, OD, 1A, 1B, 1C, 1D; A, B, C, D; Ē, S; R39 1RA4, R40 1RA5, R37 1RA6, R41 1RA7, 33Ω (X4); Ē → RASEL

Z56 LS157 — BA Ø, BA 1, BA 2, BA 3, BA 8, BA 9, BA 10, BA 11 → OA, OB, OC, OD, 1A, 1B, 1C, 1D; A, B, C, D; Ē, S; R42 2RAØ, R43 2RA1, R44 2RA2, R46 2RA3, 33Ω (X4); Ē → RASEL

DØ ~ D7

4164 (Z47-Z54) (X8) DØ-D7 — 1RAØ, 1RA1, 1RA2, 1RA3, 1RA4, 1RA5, 1RA6, 1RA7 → AØ, A1, A2, A3, A4, A5, A6, A7; DI; RAS, CAS, WE; DO; BRAS, 1CAS, 2RWR

DØ ~ D7

4164 (Z57-Z64) (X8) DØ-D7 — 2RAØ, 2RA1, 2RA2, 2RA3, 2RA4, 2RA5, 2RA6, 2RA7 → AØ, A1, A2, A3, A4, A5, A6, A7; DI; RAS, CAS, WE; DO; BRAS, 2CAS, 2RWR

DØ ~ D7

Z30 Z80 CTC — DØ, D1, D2, D3, D4, D5, D6, D7; CE, CS0, CS1, M1, IORQ, RD, RST; CLK/TRG0, ZC/TO0, CLK/TRG1, ZC/TO1, CLK/TRG2, ZC/TO2, CLK TRG3, INT, IEI, IEO, CLK; GND, +5; R53 3.3K +5 → TRG1; IP; INT; CPCLK

Z31 Z-80 DART OR 3IOØ — DØ, D1, D2, D3, D4, D5, D6, D7; BBB, BRST, BM1, BIORQ, BRD, BAØ, BA 1, INT, +5, CP CLK; CE, RST, M1, IORQ, RD, B/Ā, C/D, INT, IEI, IEO, CLK; TXDA, RXDA, TXCA, RXCA, RIA, RTSA, CTSA, DTRA, DCDA, TXDB, RXDB, RXCXCB, RIB, RTSB, CTSB, DRTB, DCDB; GND, YCC, +5

MC1489 ×4 (Z32, Z33, Z36, Z37) — MC1488 ×4 (Z33, Z37)

J6 — GND, GND, TD, RD, DSR, RTS, CTS, DTR, CD

RS-232 CHAN. A

J7 — TD, RD, RI, RTS, CTS, DTR, CD, GND, GND

RS-232 CHAN. B

Z40 LS244 — BMREQ, BRFSH, CPCLK, BWR; R26 33Ω → BRAS

Z39 LS74 ×2 — RASEL; R15 300Ω +5; R24, 10K; Q2 2N5172; C36 100PF

RAM, BNK; Z41 LS32 ×2 — R27 33Ω → 1CAS; R29 33Ω → 2CAS

CHANNEL "B" FREQ

CHANNEL "A" FREQ

Z13 LS374 — DØ, D1, D2, D3, D4, D5, D6, D7; 93; D, Ē, Q

Z17 COM5016 — RA, RB, RC, RD, TA, TB, TC, TD, STR, STT; FR, FT, XTAL, XTAL; Y1 5.0688 MHZ; +5; +12; JP4

Z23 LS244 — DØ, D1, D2, D3, D4, D5, D6, D7

Z22 LS244 — BS 15, BSEL; DØ, D1, D7

Z15 LS139 — 947, BAØ, BA1; G, A, B; YO, Y1

Z34 LS374 — BS 15; DØ, D1, D2, D3, D4, D5, D6, D7; 92; D, Ē, Q → BSEL

Z55 LS157 — BA 4, BA 5, BA 6, BA 7, BA 12, BA 13, BA 14 → OA, OB, OC, OD, 1A, 1B, 1C, 1D; A, B, C, D; Ē, S; R47 2RA4, R48 2RA5, R45 2RA6, R49 2RA7, 33Ω (X4); Ē → RASEL

R28 33Ω → 1RWR; R30 33Ω → 2RWR

| ITEM | QTY | PART NUMBER | DESCRIPTION | MATERIAL | FINISH |
|---|---|---|---|---|---|
| PARTS LIST | | | | | |

NOTES: UNLESS OTHERWISE SPECIFIED, DIMENSION ARE IN INCHES AND APPLY TO FINISHED PART. REMOVE BURRS AND SHARP EDGES. DO NOT SCALE THIS DRAWING.

| TOL. | FRAC. | 2 PLC. | 3 PLC. | ANG. | FINISH |
|---|---|---|---|---|---|
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SCALE: —

MATL: —

FINISH: —

DRAWN BY: Steve Nguyen DATE 5-16-83

CHECKED BY: W. Chang DATE 6-8-83

APPROVED BY: DATE 7/12/83

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USED ON: PPC-80

NEXT ASSY:

RECORTEC, INC.
MT. VIEW, CA 94043

TITLE: PPC-80

SIZE: D | DRAWING NUMBER: 10-0303 SHEET 2 OF 3 | REV: —

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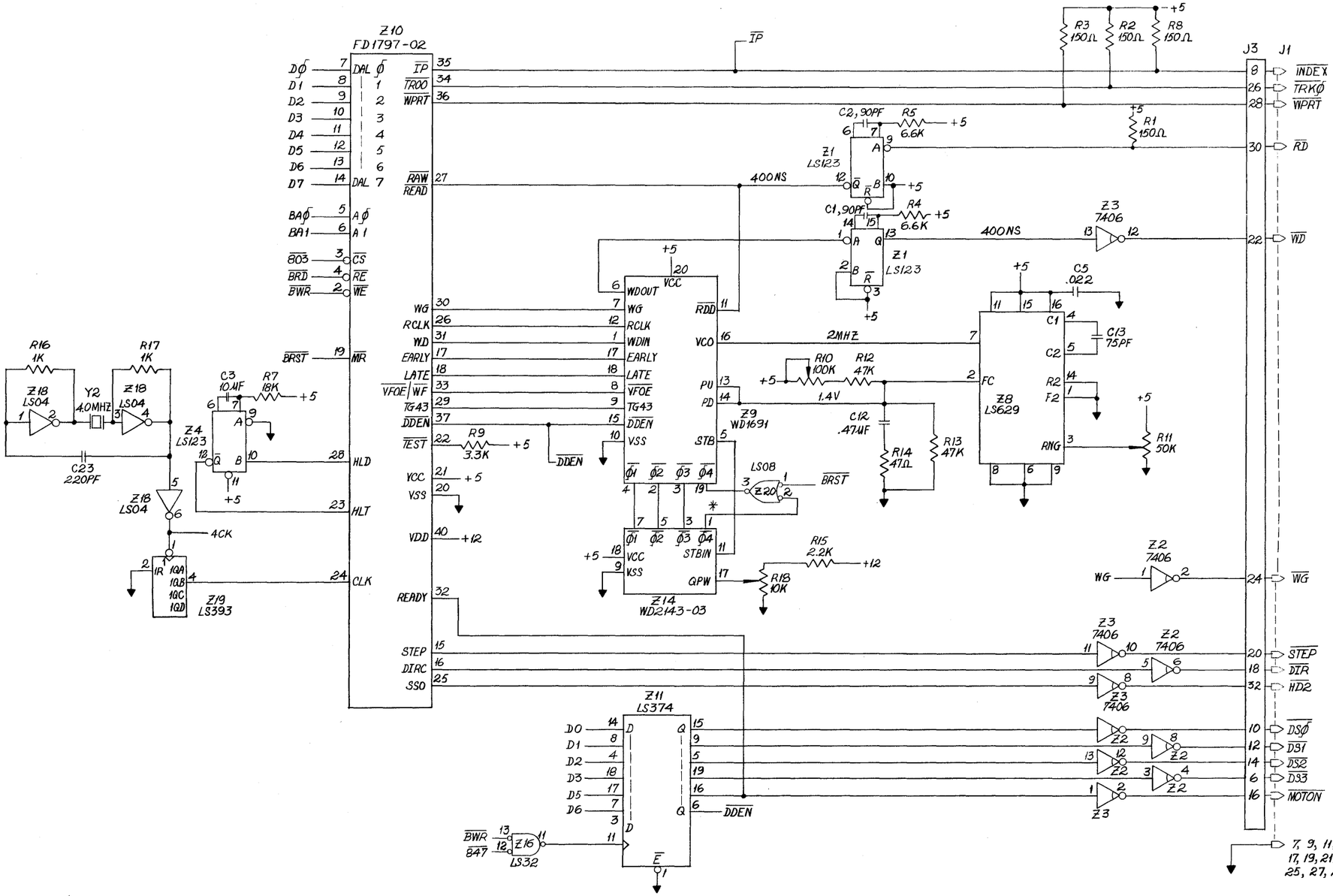
| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APPROVED |
| — | — | RELEASE FOR PRODUCTION | 7/10/82 | |




✳ NOTE: BOARDS UP TO REVISION D ARE CONNECTED TO Z14 PIN 2 WHICH DISABLES Z14. BOARDS REVISION D AND UP ARE CONNECTED AS SHOWN WHICH ENABLES Z14.

| ITEM | QTY | PART NUMBER | DESCRIPTION | MATERIAL | FINISH |
|---|---|---|---|---|---|

PARTS LIST

NOTES: UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES AND APPLY TO FINISHED PART. REMOVE BURRS AND SHARP EDGES. DO NOT SCALE THIS DRAWING.

| TOL. | FRAC. | 2 PLC. | 3 PLC. | ANG. | FINISH |
|---|---|---|---|---|---|
| ± | — | — | — | — | — |

SCALE:

MATL:

FINISH:

DRAWN BY: Lieu Nguyen DATE 5-16-83
CHECKED BY: W. Chung DATE 6-8-83
APPROVED BY: DATE 7/6/83

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