MOTOROLA® CMOS MACROCELL ARRAY LIBRARY

June 1985

p-cad™
PERSONAL CAD SYSTEMS INC.

000-0084-00

PERSONAL CAD SYSTEMS

MOTOROLA(R) CMOS MACROCELL ARRAY LIBRARY

SCHEMATIC SYMBOLS

Preliminary

000-0084-00
June 1985

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CONTENTS

INTRODUCTION

This manual and the Motorola CMOS Macrocell Array Library Symbol Diskette comprise the P-CAD Motorola CMOS Macrocell Array Library.

The library diskettes contain the following files for use with the PC-CAPS schematic capture program:

- Component files
- Special symbol files
- Layer structure file, ICLAYS.SCH
- Standard-size drawing sheet files, ASIZE.SCH through ESIZE.SCH.

The library has been developed at the request of our users, and we welcome any suggestions for improvements or additions.

The first section of the manual outlines a directory structure that is recommended for storage of the library files. The second section describes the special library files provided for translation of the user's schematic netlist into a LOGCAP(TM) output that is compatible with Motorola CAD systems. The third section provides guidelines on the design of a circuit for use with the NX-MLCP interface program.

The remainder of the manual is devoted to lists of components by sequence and function, component pin sequences, and component plots.

DIRECTORY STRUCTURE

For more efficient storage and easier access to the library, P-CAD recommends that you store the library within a directory structure tailored to your particular applications and design methods. Figure 1 is an example of an efficient directory structure for storage of the library symbols and parts.

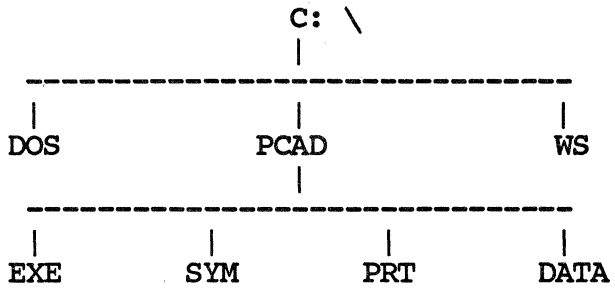


Figure 1. Directory Structure

In this example, symbols are stored in the SYM directory, and parts are stored in the PRT directory.

SPECIAL FILES AND SYMBOLS

In addition to the standard Motorola component symbols, the P-CAD Motorola CMOS Macrocell Array Library contains a special layer structure file, standard-size drawing sheet files, and special symbol files. These special files are used to translate the user's schematic netlist into a format that is compatible with Motorola CAD systems. Each of these files is discussed below.

Layer Structure File

The ICLAYS.SCH layer structure shown below is a modified version of the standard P-CAD layer structure (LAYS.SCH). ICLAYS.SCH was used to create the Motorola CMOS symbols included in this library.

Layer	Name	Pen	Status	Use
1	WIRES	1	OFF	Interconnecting wires
2	BUS	1	OFF	Interconnecting busses/wires
3	GATE	2	ABL	Gate geometry/symbol
4	IEEE	2	OFF	Not used
5	PINFUN	3	OFF	Not used
6	PINNUM	1	OFF	Translator grouping

Layer	Name	Pen	Status	Use
7	PINNAM	6	ABLE	Pin names
8	PINCON	4	ABL	Pin connections (dot)
9	REFDES	2	OFF	Translator grouping
10	ATTR	6	OFF	Visable attributes
11	SDOT	1	OFF	Not used
12	DEVICE	5	ABL	Macrocell ID
13	OUTLIN	5	ABL	Macrocell outline
14	ATTR2	6	OFF	Invisible attributes
15	NOTES	6	OFF	Notes/text
16	NETNAM	4	OFF	Net names
17	CMPNAM	5	OFF	Component instance names
18	BORDER	5	OFF	Drawing border

Drawing Sheet Files

The library includes standard-size drawing sheet files, ASIZE.SCH through ESIZE.SCH, for circuit design. These files provide the ICLAYS.SCH layer structure plus a drawing sheet border. They can be used in place of the ICLAYS.SCH layer structure.

Special Symbol Files

In addition to the standard Motorola component symbols, the library includes special "non-component" symbols. These symbols are interpreted by the NX-MLCP Motorola IC Interface program, which translates the user's design information into a LOGCAP format compatible with Motorola CAD systems. Each symbol used in the circuit is described on a line of the LOGCAP output. The symbols include:

- PADIN.SYM and PADOUT.SYM to represent circuit inputs and outputs
- TRIBUS2.SYM through TRIBUS5.SYM, TRIBUS8.SYM, and TRIBUS16.SYM for tri-state bus structures with 2, 3, 4, 5, 8, and 16 inputs
- WIRED2.SYM through WIRED8.SYM for wired functions with from two to eight inputs.

A test schematic containing the special symbols is shown in Figure 2, and the corresponding LOGCAP output is shown in Figure 3. Refer to the appropriate Motorola documentation or consult Motorola technical support personnel for further information on the use of special symbols in a specific circuit design.

For a complete description of the NX-MLCP interface program, see the NX-MLCP User's Manual.

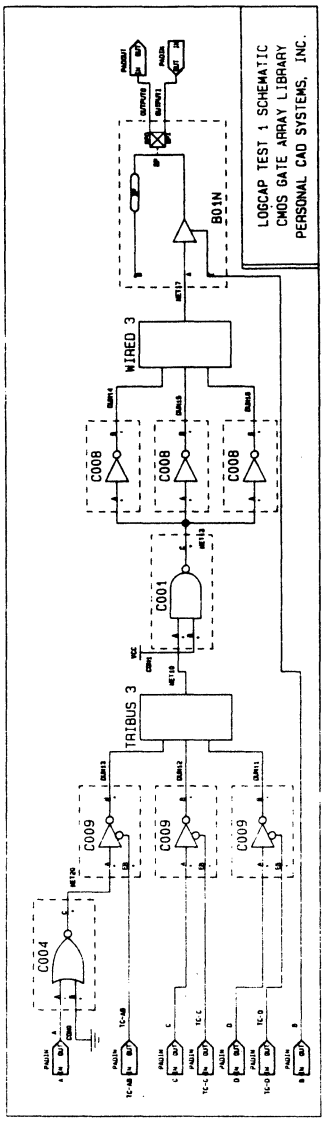


Figure 2. CMOS Gate Array Schematic

```
$$*****************************************************
$$                                                    *
$$  Copyright (C) 1985 - Personal CAD Systems, Inc.   *
$$                                                    *
$$  Program  :   NX-MLCP  VERSION 1.24                *
$$  Date     :   May 14 1985                          *
$$  Time     :   08:38:53 AM                          *
$$  File In  :   CLCPTST1.NLT                         *
$$  File Out :   CLCPTST1.LCP                         *
$$  Format   :   LOGCAP LIST                          *
$$                                                    *
$$*****************************************************

$NETWORK
$INP A TC-AB C TC-C D TC-D B OUTPUTI
$OUT OUTPUTO
$TRIBUS 0 0
NET10 3 DUM13 DUM12 DUM11
$WIRED 0 0
NET17 3 DUM14 DUM15 DUM16
$SUBU B01N
OUTPUTO * / &
B NET17 OUTPUTI
$SUBU C004
NET20 * * / &
A CON0 * * * *
$SUBU C009
DUM12 DUM13 / &
C TC-C NET20 TC-AB
$SUBU C009
DUM11 * / &
D TC-D * *
$SUBU C001
NET13 * * / &
NET10 CON1 * * * *
$SUBU C008
DUM14 DUM15 DUM16 * / &
NET13 NET13 NET13 *
```

Figure 3. LOGCAP Output

CIRCUIT DESIGN

To design the circuit, run PC-CAPS. After the menu is displayed, select FILE/LOAD. Load the ICLAYS.SCH layer structure or one of the drawing sheets supplied with the library (ASIZE.SCH through ESIZE.SCH).

Create the design by entering the appropriate components, wires, text, instance, and net names. Step-by-step instructions are given in the tutorial section of your PC-CAPS User's Manual.

Each PC-CAPS symbol contains the electrical "intelligence" required to create schematics and extract data.

Input and Output Signals

For each input signal to the circuit there must be a PADIN.SYM with input and output pins. A net must be connected to each output pin. A net connected to the output pin of a PADIN.SYM will be listed as an input signal on the $INP line of the LOGCAP output. This signal can be viewed as the input signal to the circuit from an external source.

For each output from the circuit there must be a PADOUT.SYM with input and output pins. A net connected to the input pin of a PADOUT.SYM will be listed as an output signal on the $OUT line of the LOGCAP output. This signal can be viewed as the output signal to the external environment.

Tribus Structures

A Tribus structure must be explicitly represented by a TRIBUS.SYM with the correct number of inputs. The library provides TRIBUS symbols for Tribus structures with 2, 3, 4, 5, 8, and 16 inputs. For each TRIBUS.SYM in the circuit there will be a $TRIBUS statement in the LOGCAP output. See Figure 2 for an example of a TRIBUS configuration and Figure 3 for an example of the $TRIBUS statement.

Wired Functions

A Wired function must be represented by a WIRED.SYM with the correct number of inputs. The library provides WIRED symbols for Wired functions with from 2 to 8 inputs. For each WIRED.SYM in the circuit there will be a $WIRED statement in the LOGCAP output.

Bidirectional Symbols

The BPI pin of a bidirectional symbol must be connected to an input pad, and the BPO pin must be connected to an output pad. See Figure 2 for an example.

COMPONENT LIST BY SEQUENCE

COMPONENT LIST BY FUNCTION

Bidirectional Buffers

B01N	3-state out - short ckt inp
B01U	3-state out - short ckt inp with pull-up
B01D	3-state out - short ckt inp with pull-down
B02N	3-state out - TTL inp (non-inv)
B02U	3-state out - TTL inp (non-inv) with pull-up
B02D	3-state out - TTL inp (non-inv) with pull-down
B03N	3-state out - CMOS inp (inv)
B03U	3-state out - CMOS inp (inv) with pull-up
B03D	3-state out - CMOS inp (inv) with pull-down
B04N	3-state out - CMOS inp (non-inv)
B04U	3-state out - CMOS inp (non-inv) with pull-up
B04D	3-state out - CMOS inp (non-inv) with pull-down
B05N	3-state out - Schmitt trig inp (non-inv)
B05U	3-state out - Schmitt trig inp (non-inv) with pull-up
B05D	3-state out - Schmitt trig inp (non-inv) with pull-down

Output Buffers

Y01N	Output only (non-inv)
Y02N	Open drain output
Y03N	Short ckt output

Input Buffers

I01N	TTL input (non-inv)
I01U	TTL input (non-inv) with pull-up
I01D	TTL input (non-inv) with pull-down
I02N	CMOS input (inv)
I02U	CMOS input (inv) with pull-up
I02D	CMOS input (inv) with pull-down
I03N	CMOS input (non-inv)
I03U	CMOS input (non-inv) with pull-up
I03D	CMOS input (non-inv) with pull-down
I04N	Short ckt input
I04U	Short ckt input with pull-up
I04D	Short ckt input with pull-down
I05N	Schmitt trigger input (non-inv)
I05U	Schmitt trigger input (non-inv) with pull-up
I05D	Schmitt trigger input (non-inv) with pull-down
I06N	Schmitt trig clk driver input (n-i)
I06U	Schmitt trig clk driver input (n-i) with pull-up
I06D	Schmitt trig clk driver input (n-i) with pull-down
I07N	Clock buffer input (inv)
I07U	Clock buffer input (inv) with pull-up
I07D	Clock buffer input (inv) with pull-down

Input Buffers (Cont'd)

I08N	Clock buffer input (n-i)
I08U	Clock buffer input (n-i) with pull-up
I08D	Clock buffer input (n-i) with pull-down

Buffers/Inverters

C007	Triple inverting buffer
C008	Quad inverter
C009	Dual 3-state inverter buffer
C010	3-state non-inverting buffer

Gates

C001	Triple 2-input nand
C002	Dual 3-input nand
C003	Dual 2-input nand/and
C004	Triple 2-input nor
C005	Dual 3-input nor
C006	Dual 2-input nor/or
C017	Triple 4-input nand
C019	Triple 3-input nand/and
C020	Triple 4-input nor
C022	Triple 3-input nor/or
C053	2-input x-or buffer
C054	2-input 2 wide or-and/invert
C055	2-input 2 wide and-or/invert
C057	5-input nand/and
C058	5-input nor/or

Schmitt Trigger

C025	Schmitt trigger

Latches

C012	Nand latch and 2-input nand
C013	Nor latch and 2-input nor
C026	D latch with reset (L) and enable (L)
C027	Triple nand latch
C031	Triple nor latch

Flip-Flops

C034	Parallel load D F/F with reset (L)
C035	Multiplexed D F/F with reset (L)
C036	Toggle enable F/F with reset (L)
C037	J-K F/F with reset and set
C059	Buffered D F/F
C060	D F/F with reset (L) and set (L)

Data Selectors/Multiplexers

C028	4-to-1 multiplexer with 3-state enable (L)
C029	4-to-1 data multiplexer
C056	2-to-1 multiplexer buffer

Decoders

C033	1-to-4 decoder with outputs (L) and 2 inverts

Shift Registers

C039	2-bit serial in/serial parallel out shift register
C042	2-bit serial/parallel shift register

Counters

C038	1-bit presettable up/down counter with set

Arithmetic Circuits

C032	Full adder
C040	1-bit ALU - 7 functions
C041	2-bit magnitude comparator

Miscellaneous Functions

C030	4-bit parity checker

Special Symbols

TRIBUS2	2-input Tribus
TRIBUS3	3-input Tribus
TRIBUS4	4-input Tribus
TRIBUS5	5-input Tribus
TRIBUS8	8-input Tribus
TRIBUS16	16-input Tribus

Special Symbols (Cont'd)

WIRED2	2-input Wired
WIRED3	3-input Wired
WIRED4	4-input Wired
WIRED5	5-input Wired
WIRED6	6-input Wired
WIRED7	7-input Wired
WIRED8	8-input Wired
PADIN	Input Pad
PADOUT	Output Pad

COMPONENT PIN SEQUENCES

B01N:	BPO	B	E	A	BPI
B01U:	BPO	B	E	A	BPI
B01D:	BPO	B	E	A	BPI
B02N:	BPO	B	E	A	BPI
B02U:	BPO	B	E	A	BPI
B02D:	BPO	B	E	A	BPI
B03N:	BPO	B	E	A	BPI
B03U:	BPO	B	E	A	BPI
B03D:	BPO	B	E	A	BPI
B04N:	BPO	B	E	A	BPI
B04U:	BPO	B	E	A	BPI
B04D:	BPO	B	E	A	BPI
B05N:	BPO	B	E	A	BPI
B05U:	BPO	B	E	A	BPI
B05D:	BPO	B	E	A	BPI
Y01N:	BPO	A			
Y02N:	BPO	A			
Y03N:	BPO	A			
I01N:	A	BPI			

I01U:	A	BPI
I01D:	A	BPI
I02N:	A	BPI
I02U:	A	BPI
I02D:	A	BPI
I03N:	A	BPI
I03U:	A	BPI
I03D:	A	BPI
I04N:	A	BPI
I04U:	A	BPI
I04D:	A	BPI
I05N:	A	BPI
I05U:	A	BPI
I05D:	A	BPI
I06N:	A	BPI
I06U:	A	BPI
I06D:	A	BPI
I07N:	A	BPI
I07U:	A	BPI
I07D:	A	BPI

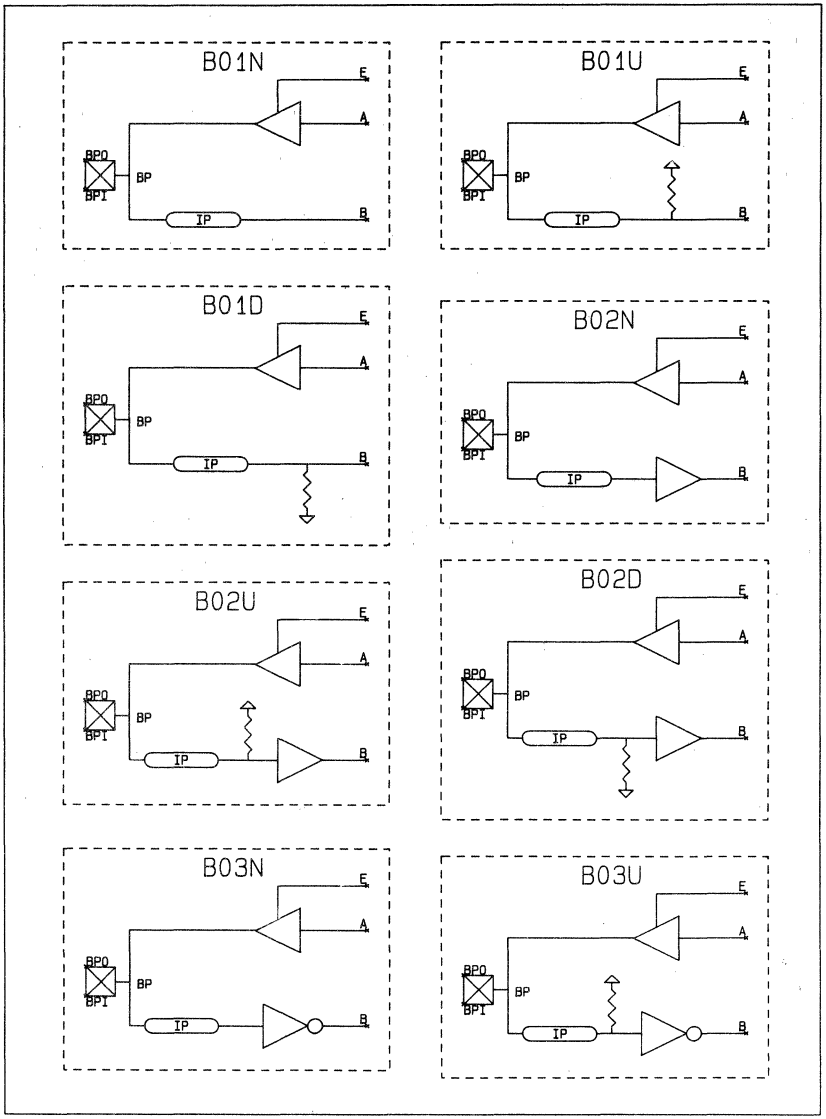
I08N:	A	BPI			
I08U:	A	BPI			
I08D:	A	BPI			
C001:	C	A	B		
C002:	D	A	B	C	
C003:	C	D	A	B	
C004:	C	A	B		
C005:	D	A	B	C	
C006:	C	D	A	B	
C007:	B	A			
C008:	B	A			
C009:	B	A	EB		
C010:	B	A	E		
C012:	C SB	Q RB	QB	A	B
C013:	C R	Q S	QB	A	B
C017:	E	A	B	C	D
C019:	D	E	A	B	C
C020:	E	A	B	C	D
C022:	D	E	A	B	C

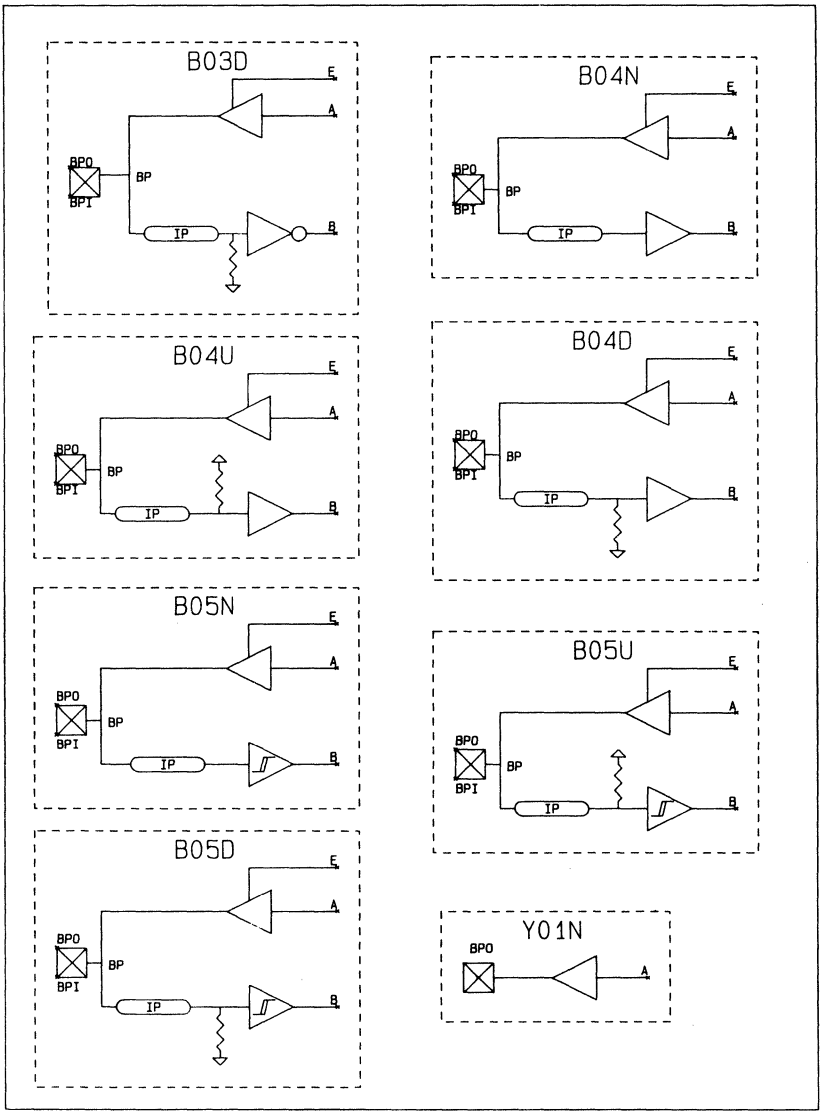
C025:	B	A			
C026:	Q	QB	D	EB	RB
C027:	Q	QB	SB	RB	
C028:	Y	D0	D1	D2	D3
	SL0	SL1	SL2	SL3	EB
C029:	Y	YB	D0	D1	D2
	D3	SLA	SLB		
C030:	Y	A	B	C	D
	EO				
C031:	Q	QB	R	S	
C032:	CO	SM	A	B	CI
C033:	Y0B	Y1B	Y2B	Y3B	A
	B	EB			
C034:	Q	QB	PEB	PD	D
	CK	R			
C035:	Q	QB	D0	D1	SL
	CK	R			
C036:	Q	QB	CK	TE	RB
C037:	Q	QB	S	J	CK
	K	R			
C038:	Q	TOB	S	PD	PEB
	CK	TIB	MD		
C039:	Q0	Q1	DO	D	CK
	R				

C040:	CO F1	FO F2	CF3	A	B
C041:	AGO A0	AEO B0	ALO AGI	A1 AEI	B1 ALI
C042:	Q0 PEB	Q1 PD0	DO PD1	DI	CK
C053:	C	A	B		
C054:	E D	F	A	B	C
C055:	E D	F	A	B	C
C056:	C	A	SL	B	
C057:	F D	G E	A	B	C
C058:	F D	G E	A	B	C
C059:	Q	QB	D	CK	
C060:	Q RB	QB	SB	D	CK
TRIBUS2:	OUT	IN1	IN2		
TRIBUS3:	OUT	IN1	IN2	IN3	
TRIBUS4:	OUT	IN1	IN2	IN3	IN4
TRIBUS5:	OUT IN5	IN1	IN2	IN3	IN4

TRIBUS8:	OUT	IN1	IN2	IN3	IN4
	IN5	IN6	IN7	IN8	
TRIBUS16:	OUT	IN1	IN2	IN3	IN4
	IN5	IN6	IN7	IN8	IN9
	IN10	IN11	IN12	IN13	IN14
	IN15	IN16			
WIRED2:	OUT	IN1	IN2		
WIRED3:	OUT	IN1	IN2	IN3	
WIRED4:	OUT	IN1	IN2	IN3	IN4
WIRED5:	OUT	IN1	IN2	IN3	IN4
	IN5				
WIRED6:	OUT	IN1	IN2	IN3	IN4
	IN5	IN6			
WIRED7:	OUT	IN1	IN2	IN3	IN4
	IN5	IN6	IN7		
WIRED8:	OUT	IN1	IN2	IN3	IN4
	IN5	IN6	IN7	IN8	
PADIN:	OUT	IN			
PADOUT:	OUT	IN			

COMPONENT PLOTS

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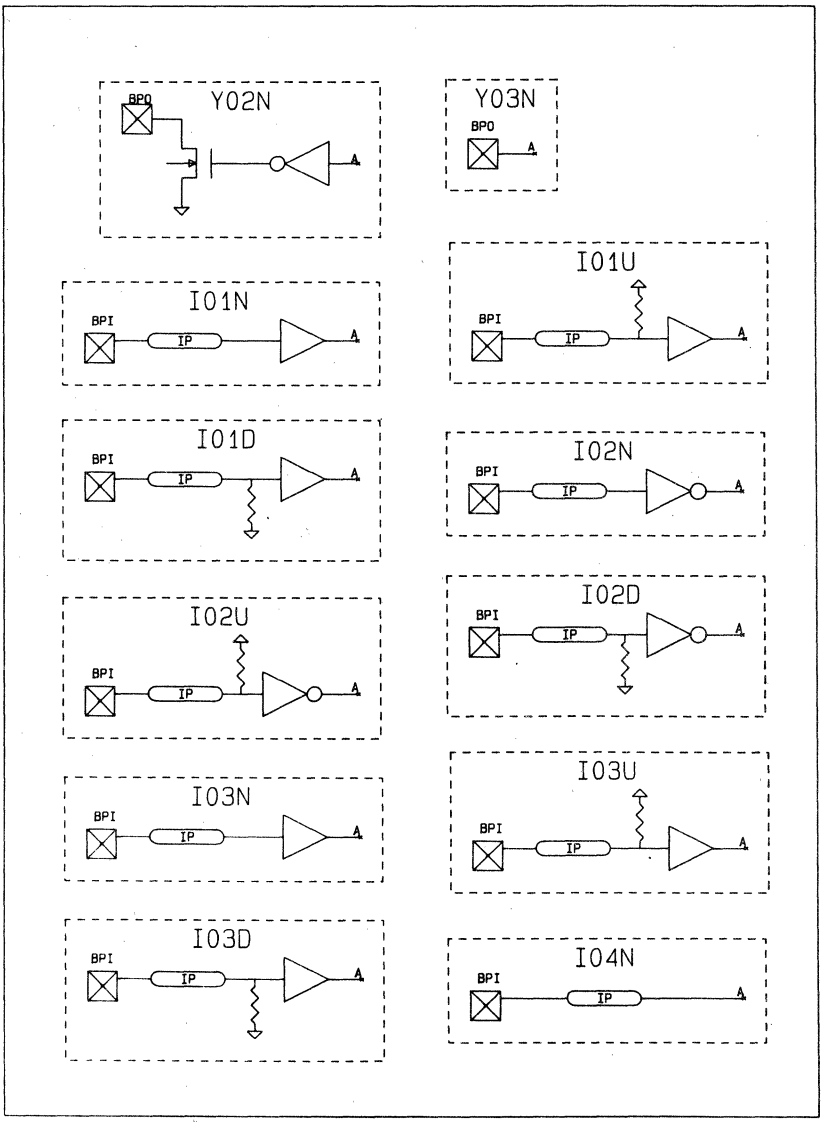
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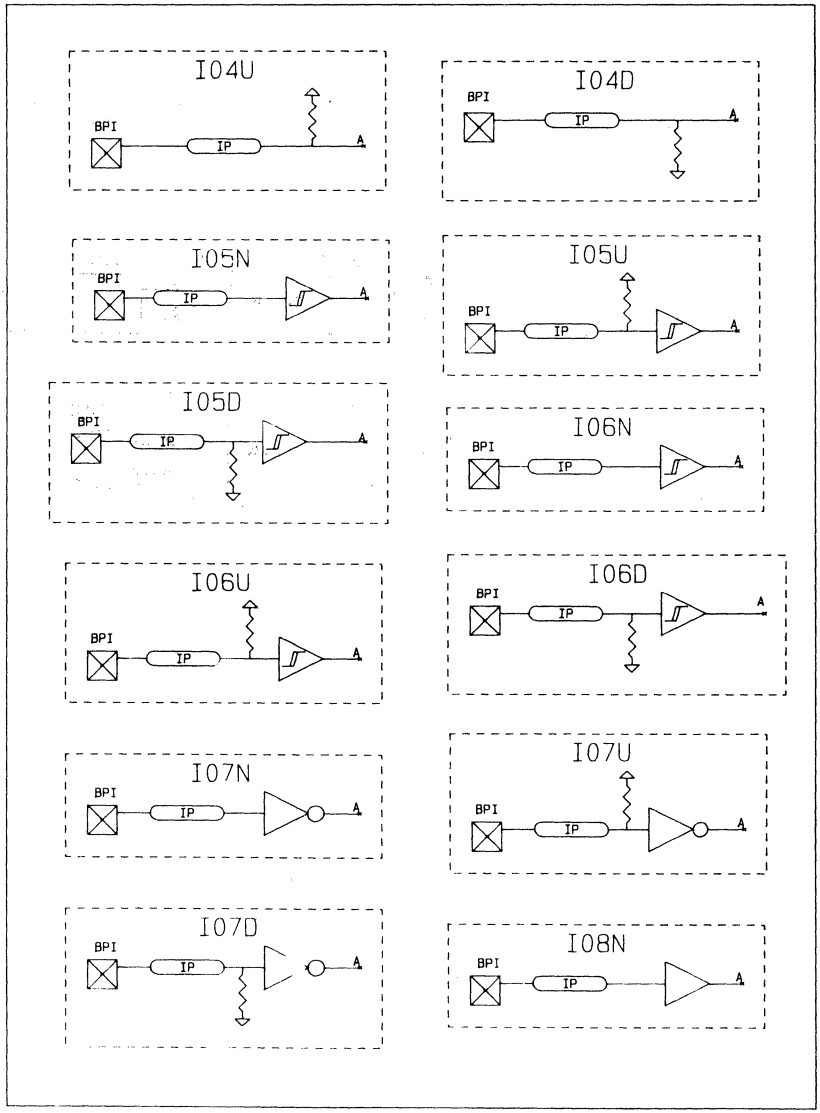
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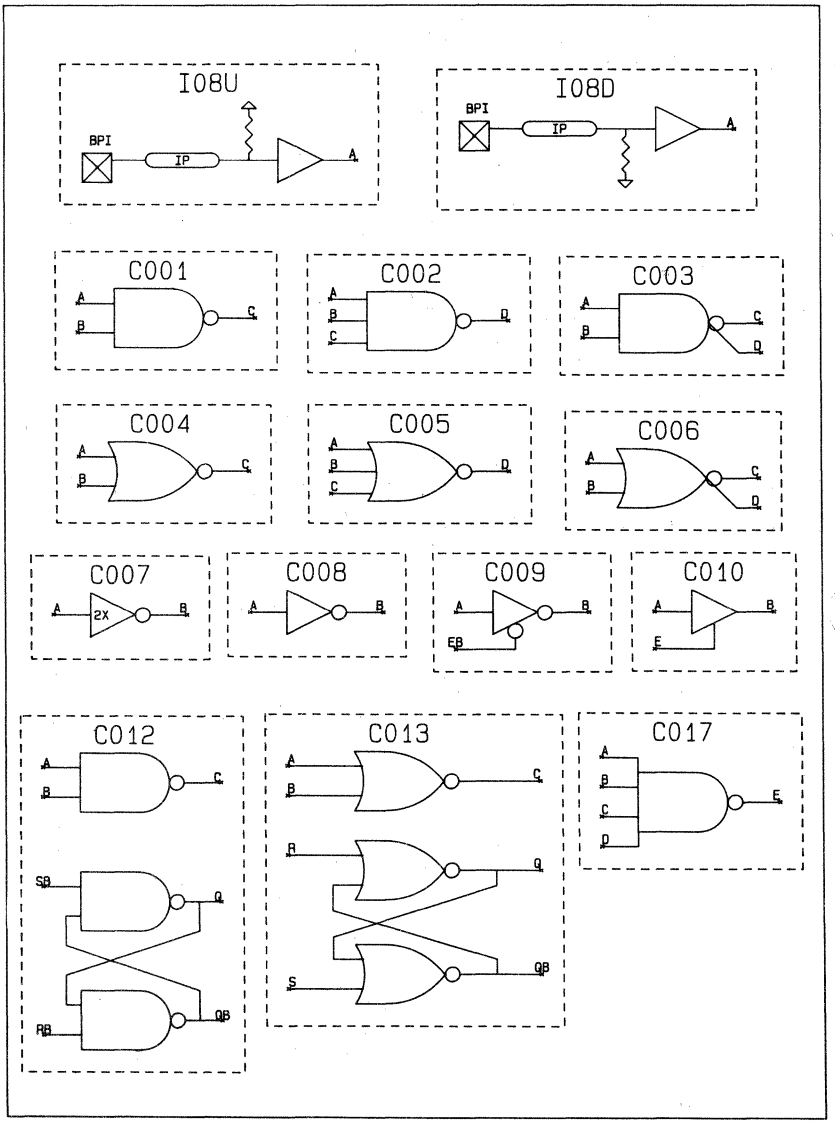
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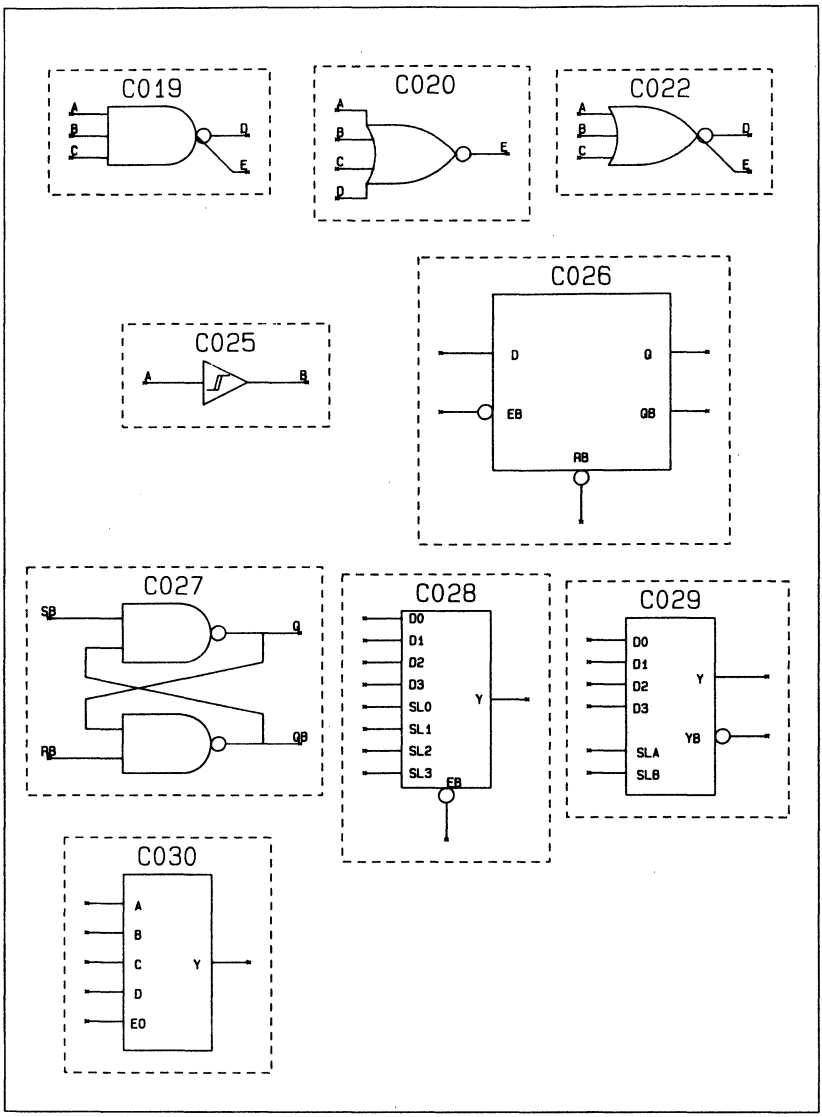
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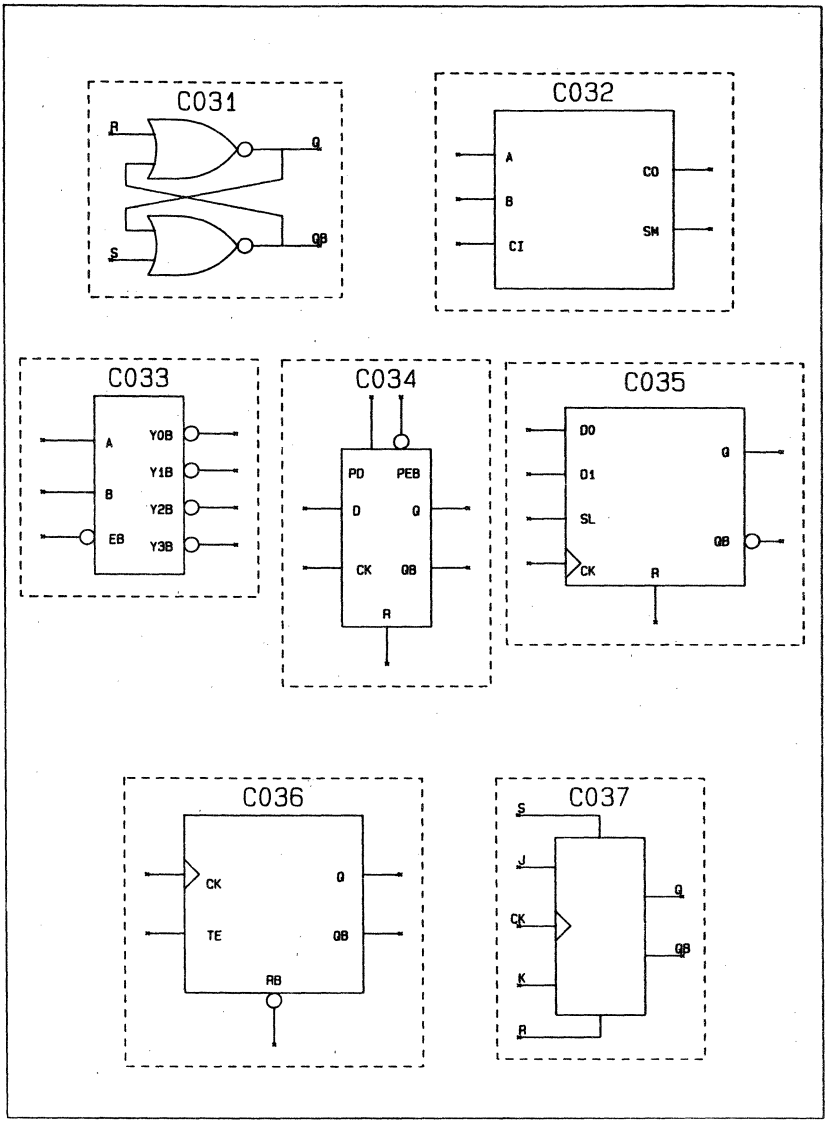
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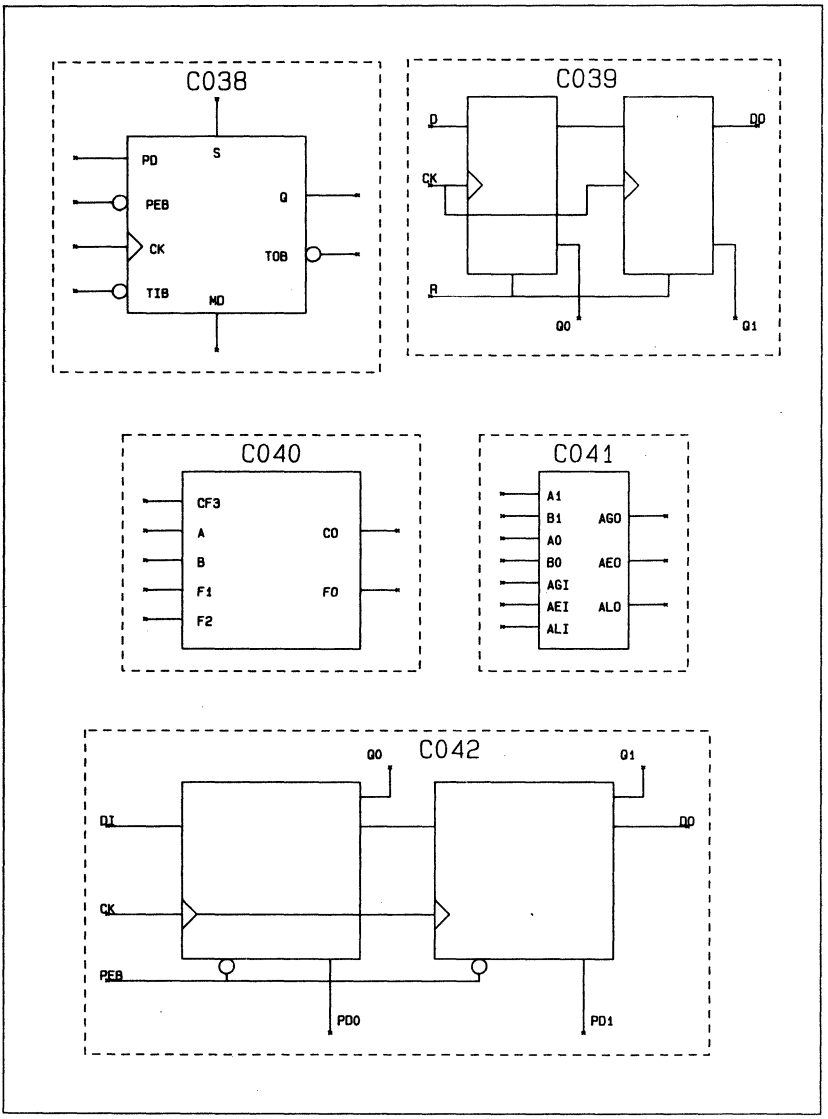
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PEB
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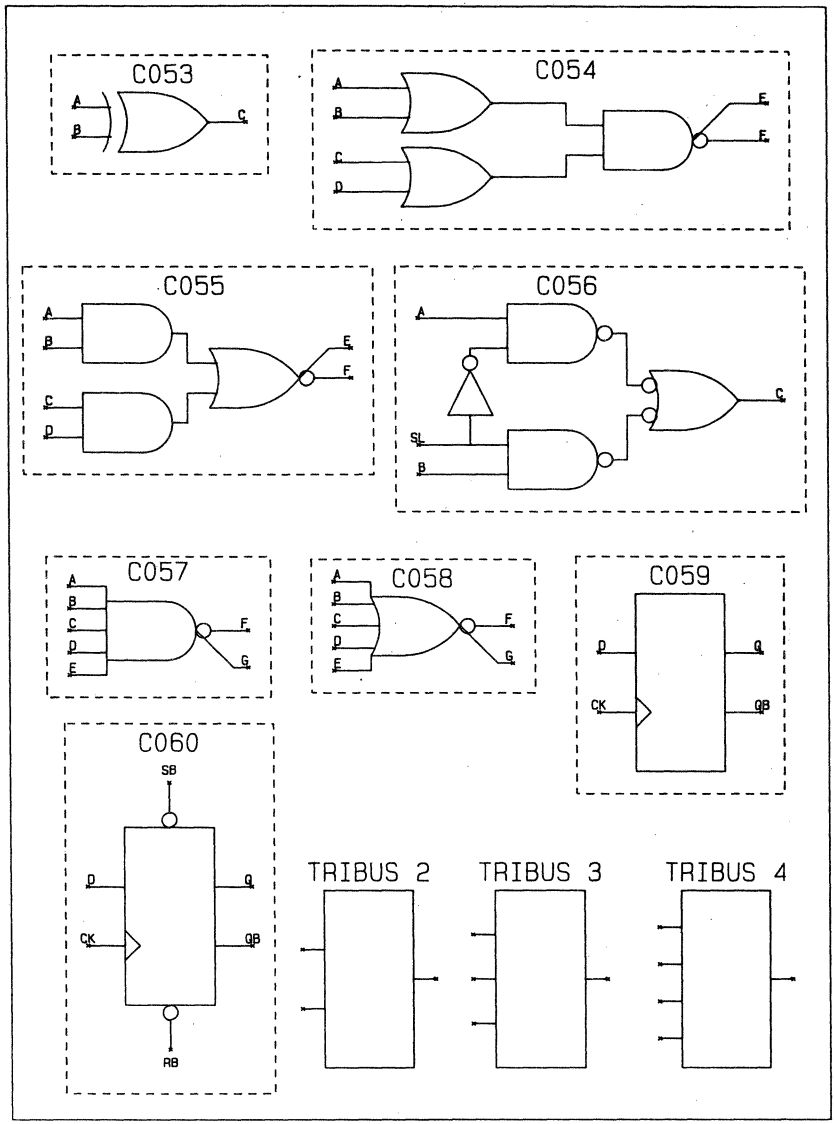
PD1


C053
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C054
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SL
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C
C057
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C058
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C
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QB
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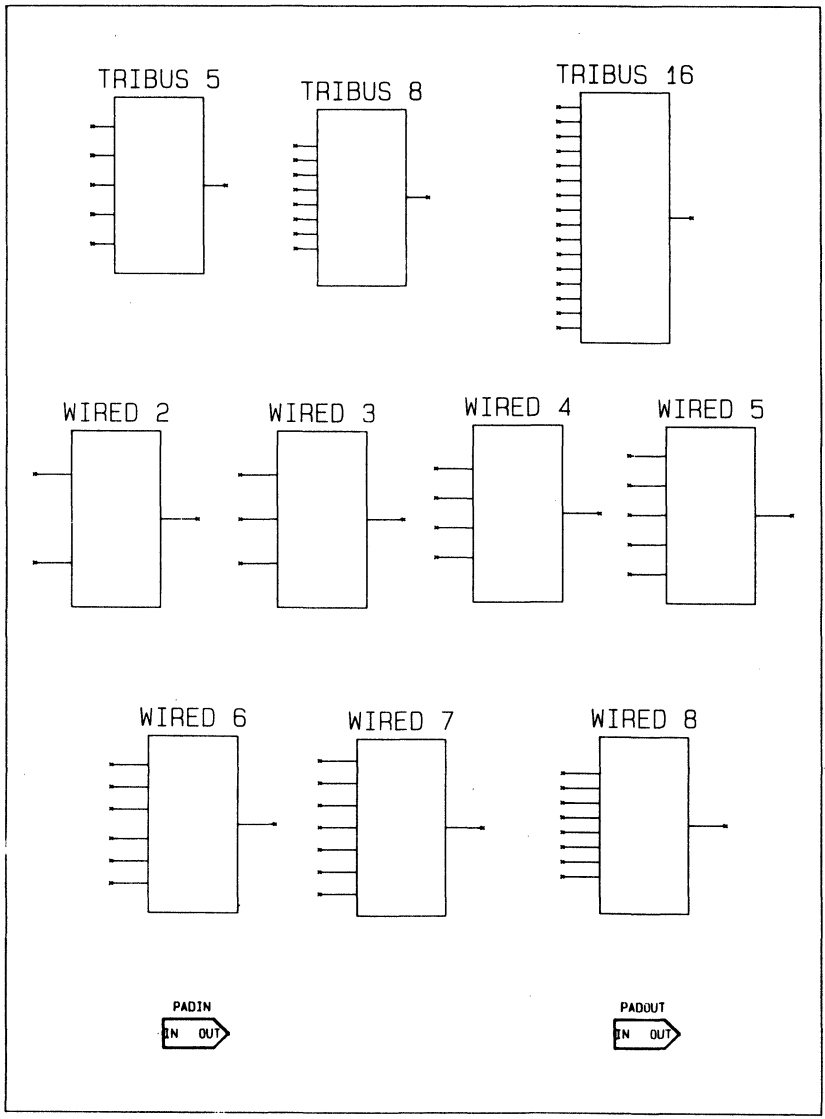
TRIBUS 2
TRIBUS 3
TRIBUS 4


TRIBUS 5
TRIBUS 8
TRIBUS 16
WIRED 2
WIRED 3
WIRED 4
WIRED 5
WIRED 6
WIRED 7
WIRED 8
PADIN
IN OUT
PADOUT
IN OUT