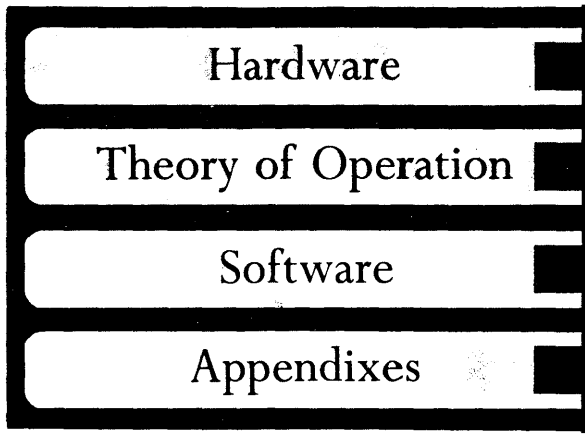
Attaché
Portable Computer
Technical Manual



O T R O N A

Attache

Portable Computer

Technical Manual

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PREFACE

How to Use This Manual

This manual is intended for readers with knowledge of electronics or software who seek information about Attache's design or interface capabilities.

The manual is divided into three sections. The first section is an overview of Attache hardware, which contains a general description of the five Attache modules: the processor board, the display, the diskette drives, the keyboard, and the power supply.

The second section is the theory of operations, which contains a description of system logic flow and the theory of operations for each of the seven logic sections on the processor board.

The logic sections are clearly marked on the board with white borders. Each section corresponds to a schematic page in Appendix A. The logic of the modules is also described.

The third section of the manual concerns Attache software. This chapter describes BIOS (Basic Input/Output System), ROM (Read-Only Memory) software, and memory locations.

Common programming functions are included with the appropriate software topic, and are also listed as illustrations on page viii for quick referencing.

Appendix A contains Attache schematics.

Appendix B is a list of referenced publications.

Appendix C is a list of acronymns.

Appendix D is the glossary.

Appendix E is the index.

Contents

I. Hardware

II. Theory of Operations

APPENDIXES

List of Illustrations

Hardware Page

List of Illustrations

Software Page

Hardware

CONTENTS

Hardware Overview

This section is an overview of Attache system hardware. Attache is divided into five basic modules: the processor board, the display, the diskette drives, the keyboard, and the power supply.

Processor Board

Contains the system control and interface logic.

Display Screen

5.5" diagonal CRT with 24 lines of 80 characters (or 24 lines of 40 double-size characters) and 320 x 240 dot array for graphics.

Diskette Drives

Two 5-1/4" double-sided, double-density 48 track per inch diskette drives.

Keyboard

Full alphanumeric Selectric (IBM^{tm}) style arrangement with additional cursor direction, delete, and multi-function keys.

Power Supply

Switching style power supply that operates from 95 to 135 volts or 190 to 270 volts, 48 to 440 Hz.

The modules are interconnected with cables, so any module can be quickly and easily disconnected from the system.

Attache System

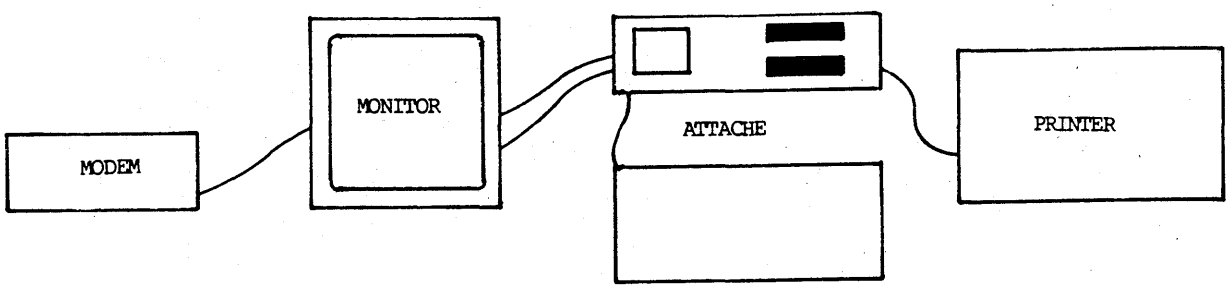


Illustration 1-1 Attache System

Ports - Attache is designed with two full-function ports to attach printers, modems, direct communication lines, and other peripheral equipment. The 15-pin connectors are the standard RS-422/423 connectors, but contain signal lines for asynchronous RS-232 connections as well.

Jumpers on the processor board are factory set for RS-232C operation but may be easily changed for RS-422/423 connection.

In all of the local cable uses, Attache appears as a Data Communication Equipment (DCE) device to the peripheral. The peripheral appears as a Data Terminal Equipment (DTE) to Attache.

Asynchronous transmission rates of 19200, 9600, 4800, 2400, 1800, 1200, 600, 150, 134.5, 110, or 75 baud may be independently selected for each port via keyboard control.

Monitor - Attache connects easily with a larger display screen for simultaneous display via the standard RCA-type pin plug at the back of the unit. Any industry standard NTSC compatible monitor used with microcomputers will function with Attache.

Expansion option - A plate can be removed from the rear panel to allow insertion of a 5 x 11 inch option board. This expansion option allows a variety of external devices to interface with Attache.

Physical Dimensions:

Height	- 5.75 inches	(14.6 cm)
Width	- 12 inches	(30.5 cm)
Depth	- 13.6 inches	(34.5 cm)
Weight	- 18 pounds	(8.1 kg)

Processor Board

The processor board is double-sided with components on one side. The board is divided into seven logical sections which are clearly delineated on the board. The sections are:

Processor	**Memory**
I/O RTC	**Floppy**
Display	**Graphics**
Serial	

These logic sections are described in Chapter 2 of this manual, however a brief discussion follows.

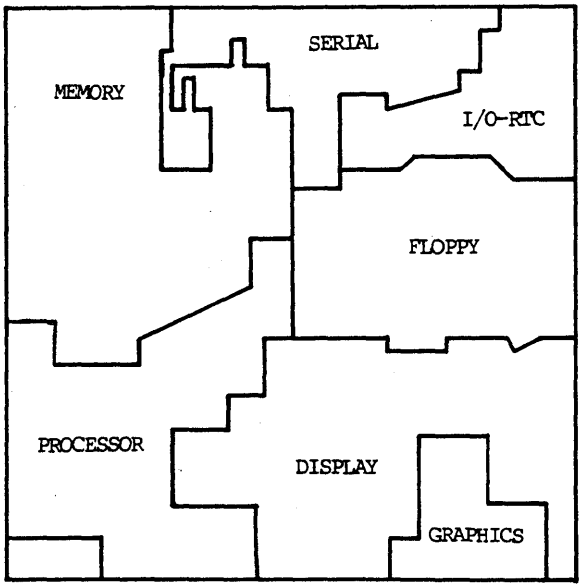


Illustration 1-2 Processor Board

Processor

The Central Processing Unit (CPU) is a Zilog Z80A which operates at 4 MHz. A 9517A (or compatible) Direct Memory Access (DMA) controller operates in parallel with the CPU, and provides excellent response time on Attache.

Memory

The memory provides the user 64K (65,536) bytes. A 4K byte Read-Only Memory chip (ROM) contains the Terminal Emulation routine, the Monitor Mode, diagnostic programs, and pointers to the CP/M load routines. The ROM is mapped in and out of main memory, so the entire 64K bytes of memory is user accessible.

I/O RTC (Real-Time Clock)

Input/Output is designed for maximum throughput with minimum response time. Attache uses a Z80 PIO for efficient interface between the system and the keyboard, the RTC, the sound effects generator, and the CMOS Random Access Memory chip (RAM).

A battery powered OKI MSM5832 (or equivalent) RTC performs continuous time of day and date functions.

The AY-3-8912 Sound Chip is user programmable. The chip drives the speaker which emits key click sounds, alarms and additional programmable audio feedback.

A 5101 CMOS RAM stores system parameters, such as keyboard volume, key sounds, baud rates, etc., which may be programmed via the keyboard.

Floppy Disk

Attache uses a D765A Floppy Disk Controller chip. Data transfers are handled by the Direct Memory Access controller. High reliability, a wide range of capability, and maximum throughput are provided with this method of disk control.

Display

A CRT 5027 controller chip provides control for the various display attributes and capabilities which are generated in this section of the processor board. The display section contains 4K bytes of alphanumeric display Random Access Memory (RAM).

Graphics

The graphics control and 10K bytes of graphics memory for the 320 dot wide by 240 dot high screen are contained in this area.

Serial

The Z80 Serial Input/Output controller (SIO) handles two independent full-duplex ports with separate control and status lines. These ports may be used to attach printers or modems to the system.

By setting the jumpers within the system, Attache can be configured for RS-232, -422, or -423.

Attache CP/M configures the SIO software for commonly used asynchronous protocol. The system is delivered with jumpers installed for the popular RS-232C interface. This serial interface is used by virtually every serial peripheral manufactured.

By changing the standard jumper settings, Attache's AM26LS30 drivers and AMLS2632 receivers use RS-422 and -423 standards. These interfaces allow transmissions at very high baud rates for long distances (up to 10,000 feet in some cases) with low-cost wiring.

Expansion Option

An internal connector will interface with the system bus. This allows a variety of external devices to interface with Attache.

Display

Attache contains a high-resolution display designed for personal viewing distance.

Alphanumeric Display

The 5.5" diagonal display is 24 lines of 80 characters each. Attache's display optimizes user efficiency with software selectable features, such as double size characters and multiple character sets. The entire screen can be updated in as little as 1/60th of a second.

Display attributes greatly enhance the display effectiveness. Attache has all of the following standard capabilities:

Reverse image	**Subscript**
Boldface	**Superscript**
Underline	**Double size**
Strikethrough	**Highlight**

Graphic Display

Attache handles the requirements of computer graphics with a very high-resolution display. This is accomplished with a 320 dot wide by 240 dot high display. Attache's resolution provides +/- .25% accuracy in the vertical scale, with even greater accuracy horizontally. Text information is easily presented along with the graphics for a "complete" display.

Diskette Drives

Attache contains two 5-1/4" mini-floppy diskette drives. The drives use a direct drive motor for fast response, highly accurate data transfer, and very high reliability.

The two drives are shock-mounted in the disk drive module assembly. The module has two separate cables and modular connectors; one for data transfers and one for powering the drives.

Attache responds quickly to shut-down the drives after the data has been transferred. This approach prolongs media life substantially, while minimizing usage of the drives themselves. The drives are up-to-speed and transferring data in less than .5 seconds.

Standard Format

The drives are formatted for CP/M usage on the Attache with 360K bytes of user storage. The data is formatted with 512 bytes per sector, 10 sectors per track, 46 tracks on the top side, 50 tracks on the bottom. Some data space is reserved for CP/M and directories, leaving 360K bytes of storage.

Keyboard

The Attache keyboard is a full alphanumeric key set laid out in the IBM Selectric^{tm} keyboard configuration. Additionally, cursor movement, delete, and multi-function keys are located on the keyboard.

A 16 keystroke buffer handles the burst speed that can occur with short words. The key stroke speed capability is calculated at approximately 60 key strokes per second, or 720 words per minute.

All keys will enter an auto-repeat mode if depressed for more than 1/2 second. This allows the user efficient data entry and system control capability. The repeat speed during auto-repeat is easily adjusted, on the rear of the keyboard, to the optimum needs of each user.

The audible feedback of the keys are adjustable via Set-up Mode's "volume" and "click" options.

The keyboard's construction makes the keys virtually impervious to contamination.

The keyboard is designed to connect to the system in a modular fashion. The connector on the system and the keyboard uses a telephone-style, 4-wire modular connector. A standard phone coil cord can be used to provide up to 10 feet of keyboard distance.

Multi-Function Keys

Keys on the top row of the keyboard are used to perform several functions in addition to numeric and special character typewriter functions. Multi-functions are activated by pressing two or more keys at the same time, as instructed by the keyboard template.

The keys which activate the multi-functions are the **CTRL** key, **SHIFT** and **CTRL** keys, and **CTRL** and **ESC** keys.

10-Key Mode

The Attache keyboard may be used as a 10-Key pad for entering columns of figures. Certain letter keys are converted to numbers when 10-Key Mode is activated and the letter keys are used in lower case.

10-Key Mode is activated by pressing **CTRL** and **CAPS LOCK** simultaneously. Press **CAPS LOCK** to return to upper case, or press **CTRL** and **CAPS LOCK** simultaneously to return to lower case.

Power Supply

The power supply contains built-in self-checking circuitry and indicator lights to verify proper operation.

A thermistor controlled, DC brushless motor fan is contained in the power supply module to provide cooling for Attache. The fan runs quietly, and causes no electronic noise that could interfere with system operation.

The constant internal temperature provides consistent trouble-free operation as well as reducing component degradation.

The power supply operates from 95 to 135 volts or 190 to 270 volts with a frequency range of 48 to 440 Hz.

Attache may be operated anywhere in the world by setting the voltage selector card and with use of the correct power cord or international adapter.

Setting the Voltage

1. Remove the fuse.

2. Remove the printed circuit board at the base of the fuse box.

3. Turn the card so the required voltage setting (100, 120, 220, or 240) is facing you.

4. Reinstall the printed circuit board in the fuse box with the desired setting facing you.

5. Reinstall the fuse; use either Slo-Blo 2A 115V or Slo-BLo 1A 230V, depending on your voltage selection.

Where conventional power is not available, the DC power option allows instant operation from 10 to 16 volt automobile or marine batteries, 20 to 32 volt aircraft systems, or from portable battery packs.

Theory of Operation

CONTENTS

This section describes the theory of operations for Attache logic, beginning with a system block diagram and a general description of overall system logic flow.

Dotted lines divide the system block diagram into sections which contain page references to their corresponding theory descriptions and Appendix A's schematic pages.

Each schematic page corresponds to a processor board division and to a topic in this chapter. The topic headings are titled the same as the board sections, and the schematic pages are presented in the same order as the topics.

Each theory topic in this chapter contains a block diagram and a specific discussion of operation.

The topics describe the seven logic sections of the processor board, and the logic of the four remaining Attache modules: the display, the keyboard, the power supply, and the diskette drives.

Note - Logic signal levels in this manual are identified as "high" or "low." A high signal represents voltage greater than +2.4 volts. A low signal represents voltage less than +.8 volts.

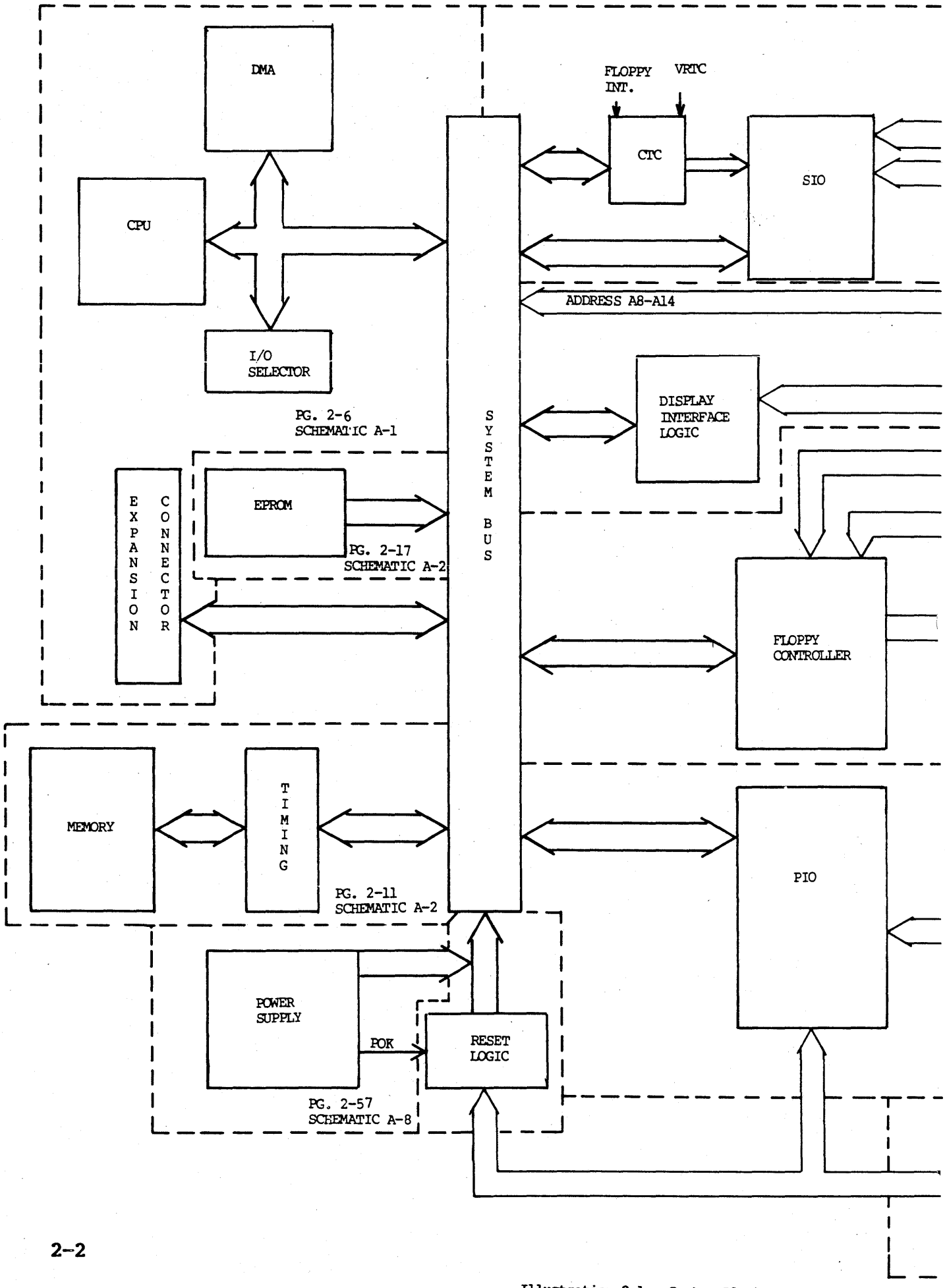
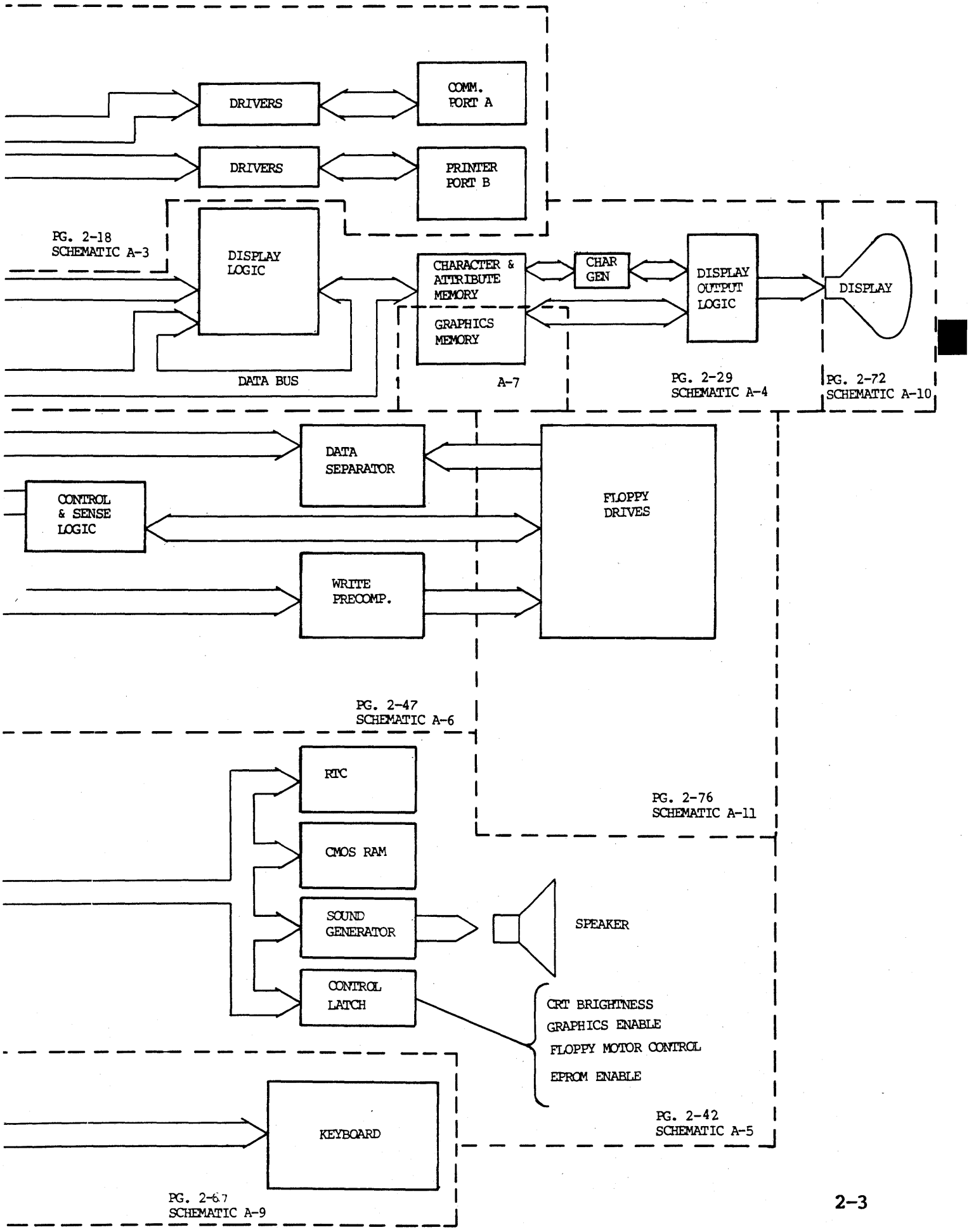


Illustration 2-1 System Block Diagram


DRIVERS
COMM. PORT A
DRIVERS
PRINTER PORT B
PG. 2-18 SCHEMATIC A-3
DISPLAY LOGIC
CHARACTER & ATTRIBUTE MEMORY
CHAR GEN
DISPLAY OUTPUT LOGIC
DISPLAY
GRAPHICS MEMORY
DATA BUS
A-7
PG. 2-29 SCHEMATIC A-4
PG. 2-72 SCHEMATIC A-10
DATA SEPARATOR
CONTROL & SENSE LOGIC
FLOPPY DRIVES
WRITE PRECOMP.
PG. 2-47 SCHEMATIC A-6
RTC
CMOS RAM
PG. 2-76 SCHEMATIC A-11
SOUND GENERATOR
SPEAKER
CONTROL LATCH
CRT BRIGHTNESS
GRAPHICS ENABLE
FLOPPY MOTOR CONTROL
EPROM ENABLE
KEYBOARD
PG. 2-42 SCHEMATIC A-5
PG. 2-67 SCHEMATIC A-9

Logic Overview

Attache's logic sections on the processor board are the processor, memory, serial, display, Input/Output and Real-Time Clock (I/O - RTC), floppy, and graphics.

The four remaining Attache modules contain separate logic boards and are also described in this chapter. These are the power supply, the keyboard, the display module, and the diskette drives.

Illustration 2-1, System Block Diagram, depicts the overall system logic flow.

The Central Processing Unit (CPU) is the central intelligence of the Attache system. The CPU's address and data lines form a system bus. This system bus provides the means for the logic sections, hardware modules, and peripheral devices to interface.

The Direct Memory Access controller (DMA) operates in parallel with the CPU. The DMA handles data transfers between memory locations and Input/Output (I/O) devices by taking control of the system bus. Either the DMA or the CPU controls the system bus at any given time.

An I/O selector identifies the I/O device which interfaces with the processor.

An Erasable Programmable Read-Only Memory (EPROM) chip loads the bootstrap routine into Random Access Memory (RAM). The bootstrap routine is the program which starts up the system. The EPROM is then disabled, which allows RAM to be accessed.

The EPROM contains the Terminal Emulation routine, the Monitor Mode, system diagnostics, and pointers to the diskette location to load the Control Program for Microcomputers (CP/M) operating system.

An Expansion Connector allows a variety of external devices to interface with the Attache system via the system bus.

The memory block represents 64K bytes of Random Access Memory (RAM). Attache uses Dynamic RAM, which requires refreshing. These refreshes are timed by Row Address Strobe/Column Address Strobe (RAS/CAS). Virtual mapping allows software to relocate any 8K byte memory region to any other memory region.

Attache's 23 KHz switching power supply powers all the system modules. The Power Okay signal ensures power is properly stabilized before the processor is initialized.

Two ports allow peripheral devices to communicate with the system via the Serial Input/Output controller (SIO). A Counter Timer Controller (CTC) generates two clock signals which produce baud rates for the ports. Additionally, two CTC channels are used in the 60 Hz Interrupt Routine and Floppy Interrupt Routine process.

The display logic contains a CRT controller which synchronizes the video signals and addresses data transfers between the display and the processor. The display constantly reads information from the display memory as it refreshes the screen. The CPU updates the display memory as display data changes.

Display memory is 4K bytes of alphanumeric RAM and 10K bytes of graphic RAM. The alphanumeric data is combined with the attributes and a character generator EPROM outputs the data bits which comprise the ASCII characters. The data is then shifted to the display module.

Data is read back from the display memory to the processor through the same logic paths.

The floppy controller writes or reads data from the diskette. Data and clock information are written on the same diskette track. Clock pulses are separated from the data by a data separator as data is read back to the processor. Write precompensation ensures that data is written at the correct diskette location.

A Parallel Input/Output controller (PIO) allows additional devices to interface with the system bus without increasing the capacitive load on the bus.

The devices which connect to the PIO are:

- the Real-Time Clock (RTC), which performs time of day functions,
- Complementary Metal-Oxide Semiconductor Random Access Memory (CMOS RAM), which stores system parameters,
- a sound synthesizer, which provides keyboard feedback and is software programmable for other sounds,
- a control latch that controls CRT brightness, generates EPROM enable, controls the floppy motor, and generates graphic enable, and
- the keyboard, which provides system reset control, data input, and control input.

Processor

The processor section of the processor board consists of the Central Processing Unit (CPU), the Direct Memory Access controller (DMA), Input/Output (I/O) Selection, and the Expansion Connector.

The Central Processing Unit (CPU) is the overall controller of system flow. The Direct Memory Access controller (DMA) operates in parallel with the CPU to route data to the proper I/O and memory addresses. The I/O Selection works in conjunction with the DMA to access the external devices during I/O data transfers. The Expansion Connector gives Attache the ability to connect boards containing such devices as additional CPUs, additional memory, peripheral attachments, and so forth.

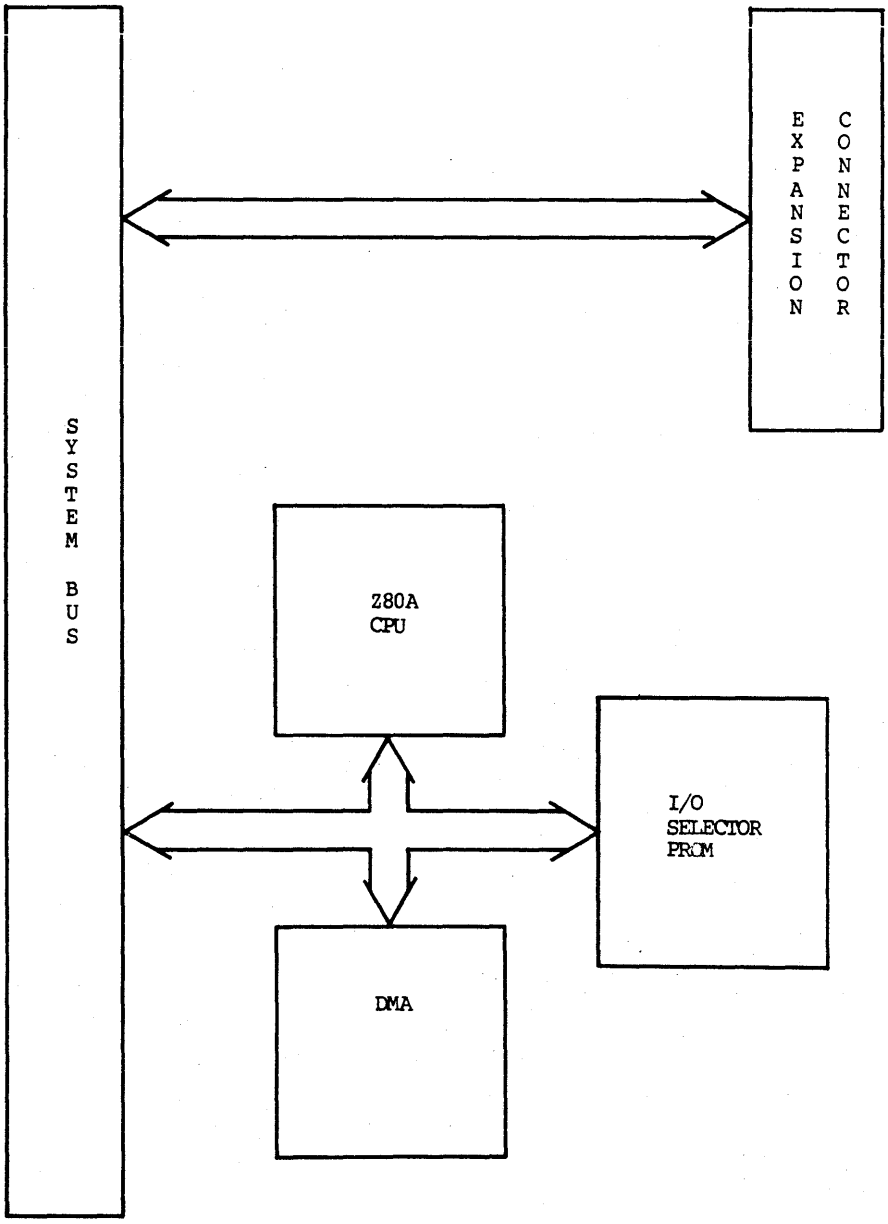


Illustration 2-2 Processor Block Diagram

Central Processing Unit

The Attache Central Processing Unit (CPU) is a Zilog - Z80A. The CPU provides the intelligence and processing control of the Attache system.

Either the CPU or the DMA has control of the system bus. The data lines are connected directly to the DMA in parallel with the CPU, as are the lower address bits.

The pin functions are described here briefly. For more information refer to the Zilog Handbook.

Pin Functions

Lines A0 - A15 form an address bus for memory and data bus exchanges and for I/O exchanges.

Lines D0 - D7 are a data bus for data exchanges with memory and I/O.

Reset, Int (interrupt), NMI (non-masked interrupt), and Wait are input signals from the system to the CPU.

Int and NMI are interrupt request signals which cause the CPU to halt current processing and handle the interrupt.

Reset initializes the system.

Wait notifies the CPU that a memory address or I/O device is not ready for a data transfer.

The CPU outputs system control signals on the lines: RFSH, MREQ, IOREQ, M1, RD, and WR.

RFSH is used to refresh the system's dynamic memory.

MREQ requests a memory read or memory write operation at the address on the address bus. IOREQ requests an I/O read or write operation at the address on the address bus.

M1 is machine cycle one and is used for system timing.

RD indicates the CPU wants to read data, and WR indicates that the CPU has data to be written to the addressed memory or I/O location.

The BUSRQ input line indicates to the CPU that another device requires usage of the system bus. BUSAK is the CPU's output signal, to notify the device requesting the bus that it can have control of the system bus.

The Direct Memory Access Controller

Attache uses an AMD 9517A (or equivalent) Direct Memory Access controller (DMA). The DMA is an interface circuit which allows external devices and memory to directly transfer data. A memory or device address is specified, the DMA moves the data to that Random Access Memory (RAM) location, and advances the address counter by one for each byte of incoming data. The DMA operates in parallel with the CPU; either the DMA or the CPU has control of the system bus at any given time.

A brief description of pin functions follows. For more information consult the Advanced Micro Device Handbook.

Pin Functions

RDY (ready) is an input which extends the memory read and write timing cycle.

HREQ (hold request) is an output to the CPU to request control of the system bus. Hold request is gated with AEN (address enable), the signal which allows the upper eight address bits to be sent to the bus. This keeps the processor from taking over the bus before DMA is finished with the bus.

HACK (hold acknowledge) is an input which signals the DMA that the CPU has relinquished control of the system bus.

DREQ0 - DREQ3 (DMA requests) are input lines the peripherals use to request a DMA cycle. DACK0 - DACK3 (DMA acknowledges) are output lines to notify a peripheral it has been allotted this DMA cycle.

ADST B (address strobe) is an output to strobe the upper address byte into an external latch (U253).

IORD (Input/Output read) is a bidirectional line to read control registers when the DMA is idle, or to access I/O data during an I/O data transfer. IOWR (input/output write) is a bidirectional line to receive information from the CPU when the DMA is idle, or to control data transfers to I/O devices.

MEMRD (memory read) accesses data from memory during memory transfers. MEMWR (memory write) is used to write data during memory transfers.

CS (chip select) is an input from the CPU to select the DMA as an I/O device when the DMA is idle.

EOP (end of process) terminates the DMA cycle.

DMA Operation

The DMA operates in two states: Active or Idle. In an Idle state the CPU is active. The DMA samples the input lines for a DMA request. During the DMA's active state the CPU is idle, and the DMA performs memory to I/O transfers.

The Attache DMA functions in a single transfer mode, making one memory transfer at a time. The DMA updates two internal registers as it does its transfers: the word count register, and the address register. The word count register contains the number of bytes of transfers the DMA is to perform. The address register contains the address the DMA uses to receive or send the data.

The DMA has four independent channels. Three of the four channels are used to transfer data in single byte mode. The fourth channel, which connects to the Expansion Connector, works in cascade mode to allow the interface expansion to include additional devices.

Data lines (D0 - D7) and the low order address bits (A0 - A7) connect directly to the DMA. Since the DMA does not have enough pins to send all sixteen address bits together, the DMA first uses the data lines (D0 - D7) to send the high order part of the address. A buffer (U247) on the data lines is constantly enabled, allowing the upper address to be latched into memory by latch U246. This designates the upper address during a DMA transfer, providing the full sixteen address lines necessary for a memory address.

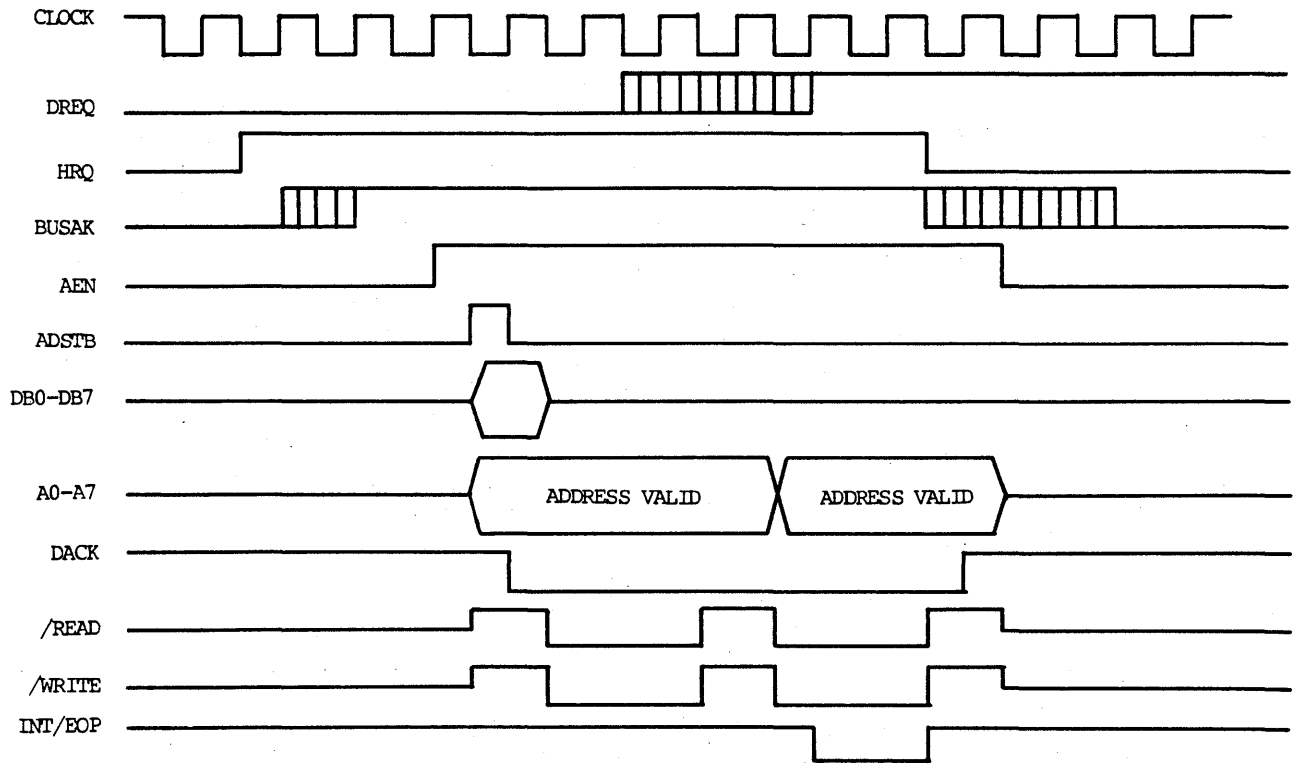


Illustration 2-3 DMA Timing

A DMA operation begins when the DMA receives a request for a data move from one of the four channels. The DMA controller sends a request for the CPU to release the bus. The CPU responds with a Hold Acknowledge to the DMA, giving the DMA control of the system bus.

The DMA sends Address Enable to enable the latch (U246) which contains the upper eight address bits. Enabling U246 gates the address bits to the bus. Address strobe at a true state makes this a valid address, and the system address bus contains the address for the DMA's data transfer.

The address is established on the bus, so the DMA sends Data Acknowledge to the device that requested the DMA service. This notifies the device that it has use of the DMA to do its transfer.

The DMA outputs the read/write pulse to allow the device to accomplish its desired transfer. The read/write signals are: I/O Read, I/O Write, Memory Read, and Memory Write.

The read and write pulse is issued simultaneously. Data to be transferred is read from the device (or memory location), and written to the desired location at the same time. For example, during an I/O read to memory, an I/O Read pulse and a Memory Write pulse are issued at the same time. Data are read from the I/O device and simultaneously written to memory.

U104 is a tri-state buffer, gated by the Hold Acknowledge signal. When Hold Acknowledge is active, the buffer outputs I/O read/write signals to the Serial Input/Output (SIO).

The read, write, and processor signal lines are pulled up with resistors so they will stay in a high state during their transition to eliminate phony timing signals.

I/O Selection

I/O selection is accomplished through the Programmable Read-Only Memory (PROM) chip (U110). I/O addresses normally uses only 8-bit addresses, though they can be used in 16-bit mode. Most I/O devices in Attache use an 8-bit mode. The PROM translates the eight address lines directly to generate the I/O device select.

The PROM is also used to generate a signal to notify external devices that an I/O transfer is occurring on the CPU board. This signal is called On Board.

Expansion Connector

The Expansion Connector contains data and address lines from the system bus. The Bus Request line allows the attachment on the connector use of the system bus. A Multifunction GPIB Board and/or Memory Board may be ordered from Otrona which interfaces with Attache via the connector.

Memory

The memory section of the processor board consists of thirty-two 1 bit by 16,384 bit memory chips, an Erasable Programmable Read-Only Memory (EPROM) chip, Row Address Strobe/Column Address Strobe (RAS/CAS) timing, and memory map control.

Attache memory inputs use multiplexing, so the chips require only seven of their pins as address pins (as opposed to fourteen). A clock divides the addresses into two halves entered at different times. The clock is called Row Address Strobe / Column Address Strobe (RAS/CAS).

Attache uses dynamic Random Access Memory (RAM). Dynamic RAM is a capacitive memory method which requires periodic refreshing to maintain the integrity of the data in storage. A refresh is accomplished by sending RAS to all of the chips concurrently.

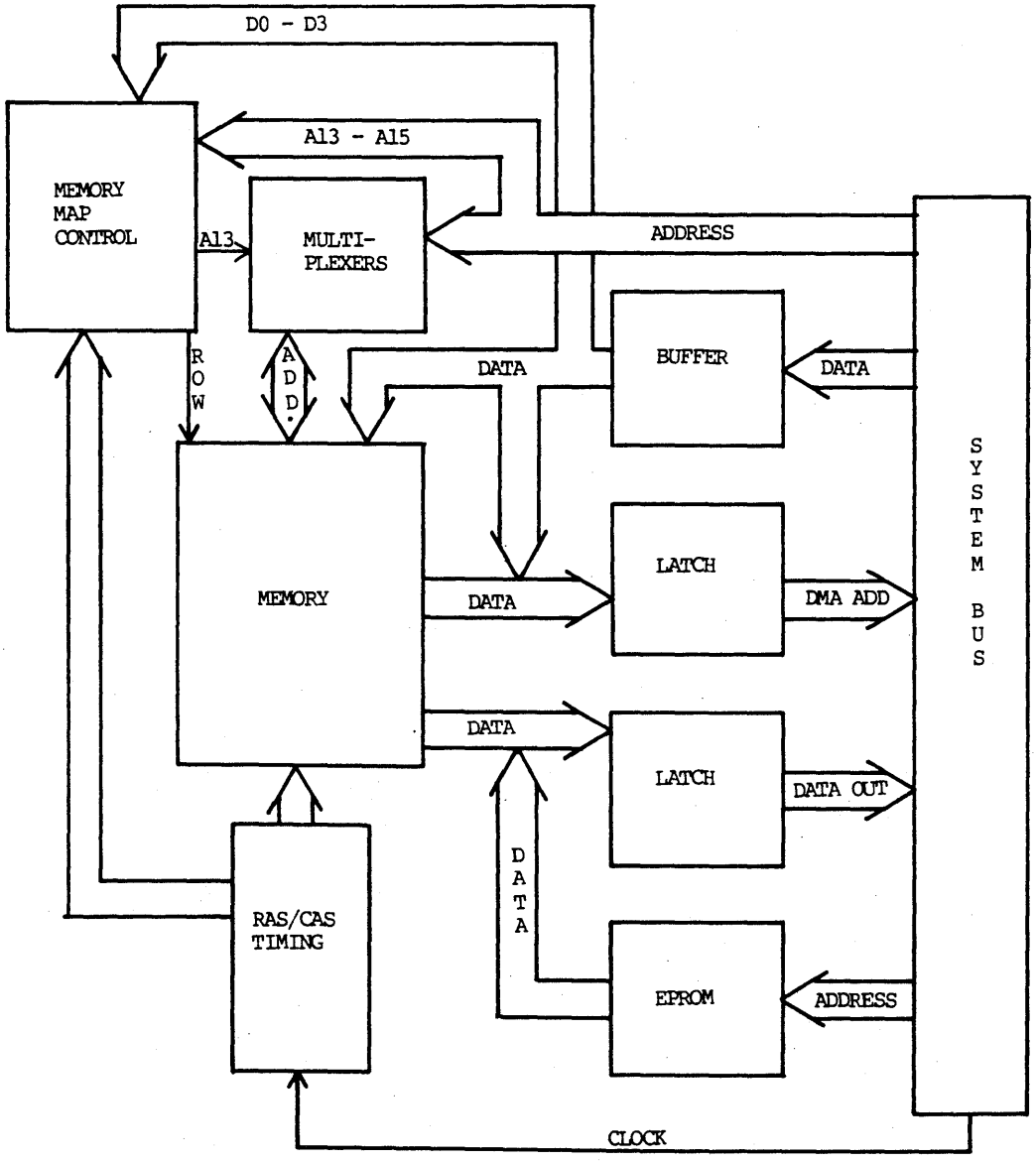


Illustration 2-4 Memory Block Diagram

Addressing RAM

To address Attache memory, the least significant address bits are put onto the address bus. The leading edge of the signal RAS is generated and strobes in those address bits. The second half of the address is then put on the address bus. The leading edge of CAS is generated, which loads the full address.

This multiplexing uses two memory address multiplexers, U244 and U245. Address bus lines A0 - A12 (plus A13 after mapping) are their inputs. The low order address lines (A0 - A6) are the A side input lines, and the high order address lines (A7 - A13) are the B side.

The outputs of the multiplexers (U244 and U245) select the individual address in two stages. At the RAS pulse the multiplexers' outputs contain the A0 - A6 address bits. At the CAS pulse the output lines contain the A7 - A12 (plus A13 after mapping) address bits. Output drivers maintain the voltage levels required by memory chips.

These, however, are only fourteen of the sixteen address lines necessary to designate a 64K byte address. The three upper address bits (A13, A14 and A15) are input lines to a RAM (U248), which allows memory to be mapped. Refer to Illustration 2-5.

The three address lines are output by the RAM into decoder U249 which selects a 16K byte bank. In the example given in Illustration 2-5, A and B are high, so the decoder enables Y3 and selects the upper 16K bank. U248 pin 9 connects to the multiplexer (U244). This line is now the fourteenth address select line, which designates the upper or lower 8K byte region of the 16K byte bank.

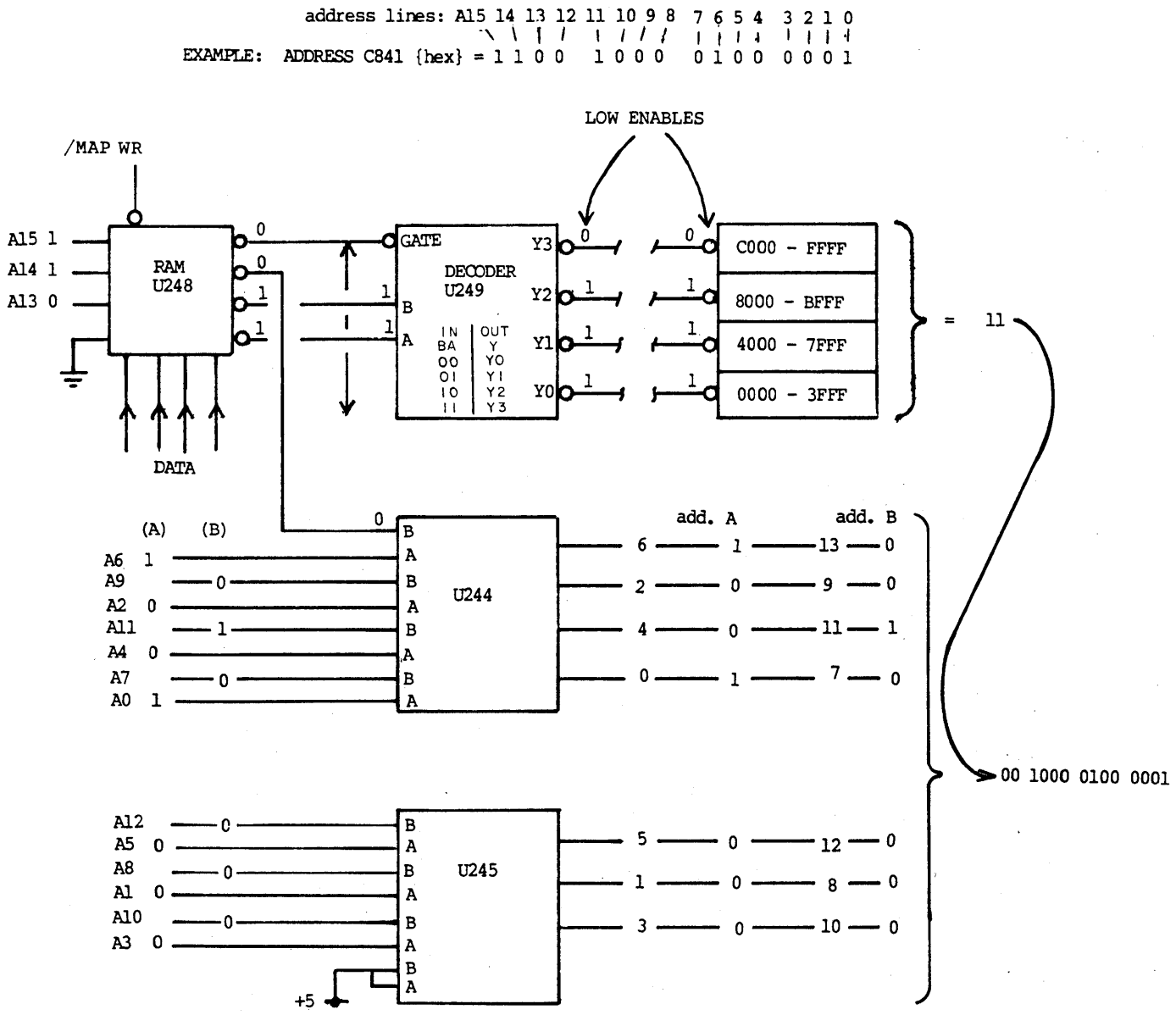


Illustration 2-5 Addressing Memory

Writing or Reading Data

The data to be read or written is transferred on the system data bus lines D0 - D7. Each byte of write data passes through the buffer (U247) to the memory chips.

As Illustration 2-6 depicts, the chips are built in an array. Address lines are run to all chips; the data lines are criss-crossed into columns and rows. Each data line connects to four chips in different rows, so each data line can input data to any of the four rows selected by RAS. The chips function in a 1 bit by 16,384 format.

Each of the 8 bits of one data byte is stored in each separate chip of one 8 chip row. In Illustration 2-6's example, bits comprising "35" are loaded into location 0000 of chips U200 - 207. Locations 0001 of the chips contain the data byte "A1", 0002 contains F0, etc.

Data to be read from memory are output into a latch (U253), and then onto the data bus. The latch performs transfers at maximum speed (the speed of an instruction fetch cycle). Attache therefore uses its software memory tests with complete accuracy. A program might otherwise pass a memory test, and yet not run because it was not tested at the maximum system speed.

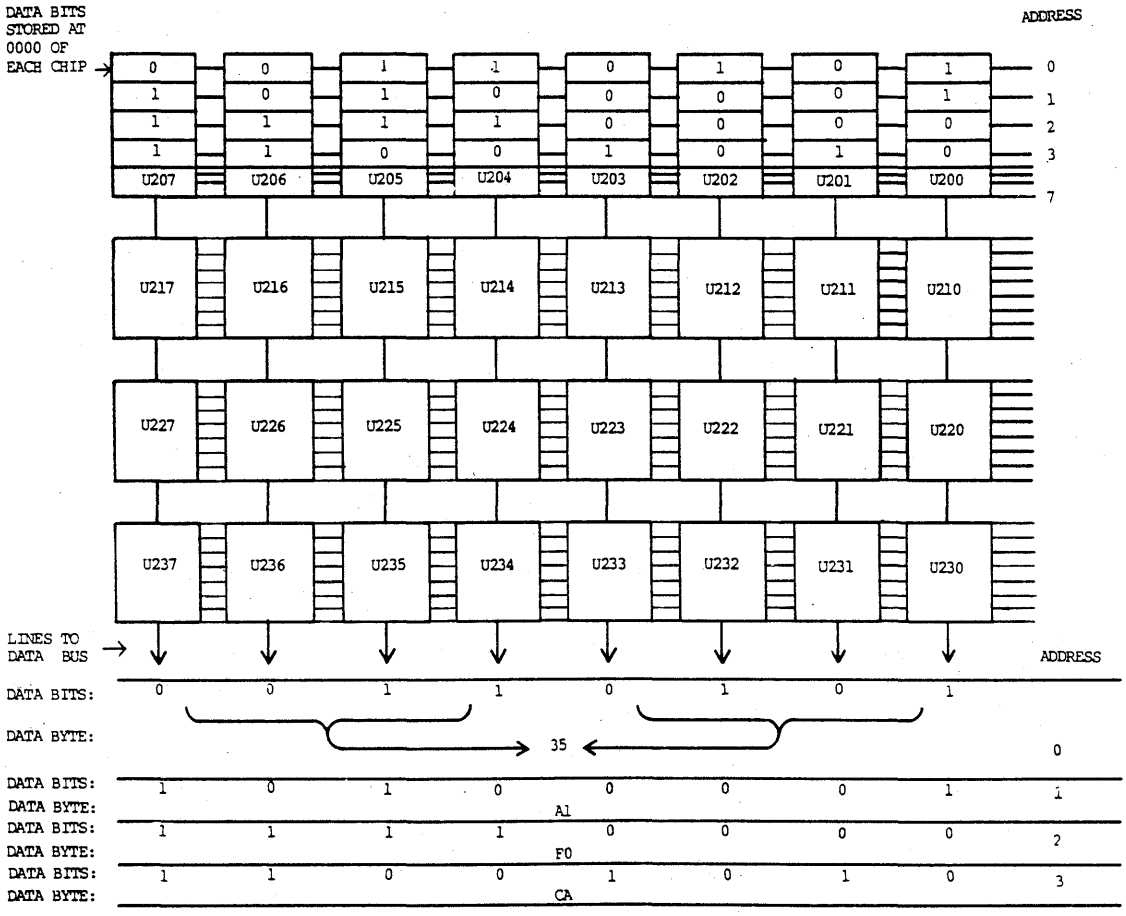


Illustration 2-6 Reading Data from Memory

Generating RAS/CAS

A Single Shot Trigger (U228) generates RAS timing. The single shot is driven directly from Memory Request.

If the system is generating a memory refresh, the RFSH signal will be true before the MEMREQ is received. Memory is refreshed by sending RAS to all of the chips at the same time. A signal, /RFSH, sent to inverter U238 drives RAS on all the memory address lines in parallel. The refresh signal also shuts off CAS.

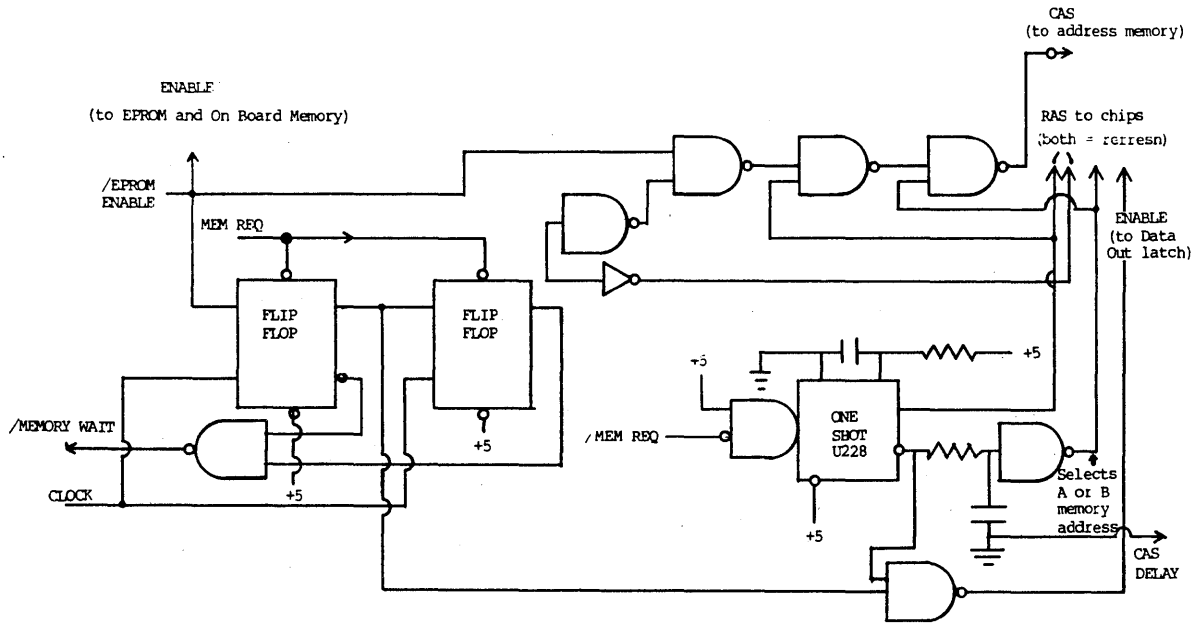


Illustration 2-7 RAS/CAS Schematic

As Illustration 2-7 depicts, the one-shot (U228) generates RAS if there is a memory request. Memory requests to addresses less than 2000 {hex} generate RAS only if the EPROM is not enabled.

The resistor - capacitor network (R206 and C204) and gates (U305 and U239) delay RAS, which creates the signal CAS. CAS gates with RAS at U239 to shut CAS off with RAS, and to guard against data lingering on the bus.

The timing for a write cycle for the processor, the DMA, and a memory chip are different, so a write signal is resynthesized at U228. When a Memory Request is received, the one shot (U228) triggers. The one shot is gated with Read such that if no read signal is received, then this is a Write, and the circuitry generates proper write timing. This keeps all RAM write cycles the same, regardless of what device accesses RAM.

Memory Mapping

Memory mapping makes the storage address appear to the processor as a specified address, while actually using another address. For example, the user simultaneously runs two different programs, both defined as starting at 0000 (hex). The processor treats these programs as if they were both at the specified address of 0000, yet one program would in fact be located at a different address. (See Illustration 2-8.)

Memory mapping also allows for future expansion of Attache. Any block of memory may be disabled by turning off the enable bit. An additional memory board could be added to Attache, and by enabling the addresses on one board while disabling addresses on the other board, the second memory board would be transparent to the processor.

Mapping is achieved through the RAM U248. The RAM has four outputs, one of which (O4) is a gate for the memory row select outputs (O1 and O2). The fourth output (O3) designates the high or low 8K memory segment of that address bank. The memory map circuit is depicted in Illustration 2-5, page 2-13.

The bank selection signals feed into a multiplexer, (U249), which decodes them into the four outputs (Y0 - Y3) that specify the address bank. Data loaded into RAM chip (U248) determine the status of the chips output lines and cause decoder U249 to select a translated 16K byte memory bank.

Memory mapping in Attache further divides the memory segments into 8K byte blocks. This is accomplished by the address bit generated in the map controller (U248 output O3). If this bit is high (following its inversion), the map selects the upper 8K byte block of the selected row. If the bit is low, the map selects the lower 8K bytes.

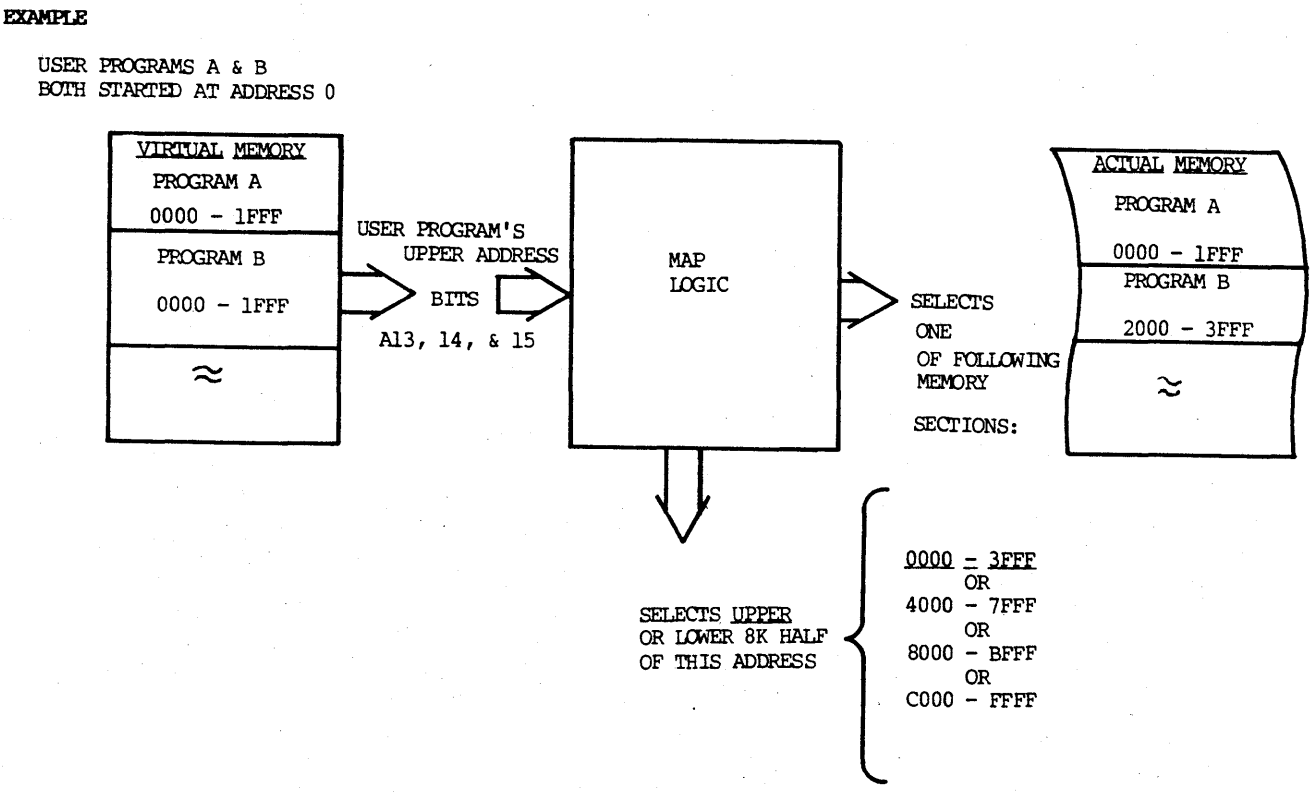


Illustration 2-8 Memory Mapping

Erasable Programmable Read-Only Memory

The Erasable Programmable Read-Only Memory (EPROM) contains the bootstrap routine to bring up the system, the Terminal Emulation routine, the Monitor Mode, and system diagnostics. The bootstrap routine forces Attache to load CP/M from the system diskette. The EPROM is then disabled and is not used until the next system reset.

The EPROM uses latch U253 to provide additional timing control. The latch (U253) receives a RAS pulse. At the falling edge of RAS the latch normally ignores any additional data until the next RAS pulse is received.

However, the EPROM operates at a slower speed than RAM. To compensate, the U240 flip-flop generates a wait state signal called /MWAIT. This signal times the data flow to accommodate the longer access time of the EPROM.

The address lines A13, A14, and A15 are gated with EPROM enable and Read at U242. A true state enables the EPROM, and activates the U240 flip-flop which generates the 250 nanosecond wait state necessary for the EPROM.

Serial

The serial section of the processor board contains the system clock, the system reset, the Counter Timer Circuit (CTC), the Serial Input/Output controller (SIO), and the serial ports.

The system clock generates the timing pulses for the logic. The reset circuitry generates a system reset via the keyboard or powering off. The CTC generates the clocks for the baud rates of the serial ports, and provides interrupt vector and priority control. The SIO controls the ports. The serial ports allow Attache to interface with external devices such as a printer, and with other systems.

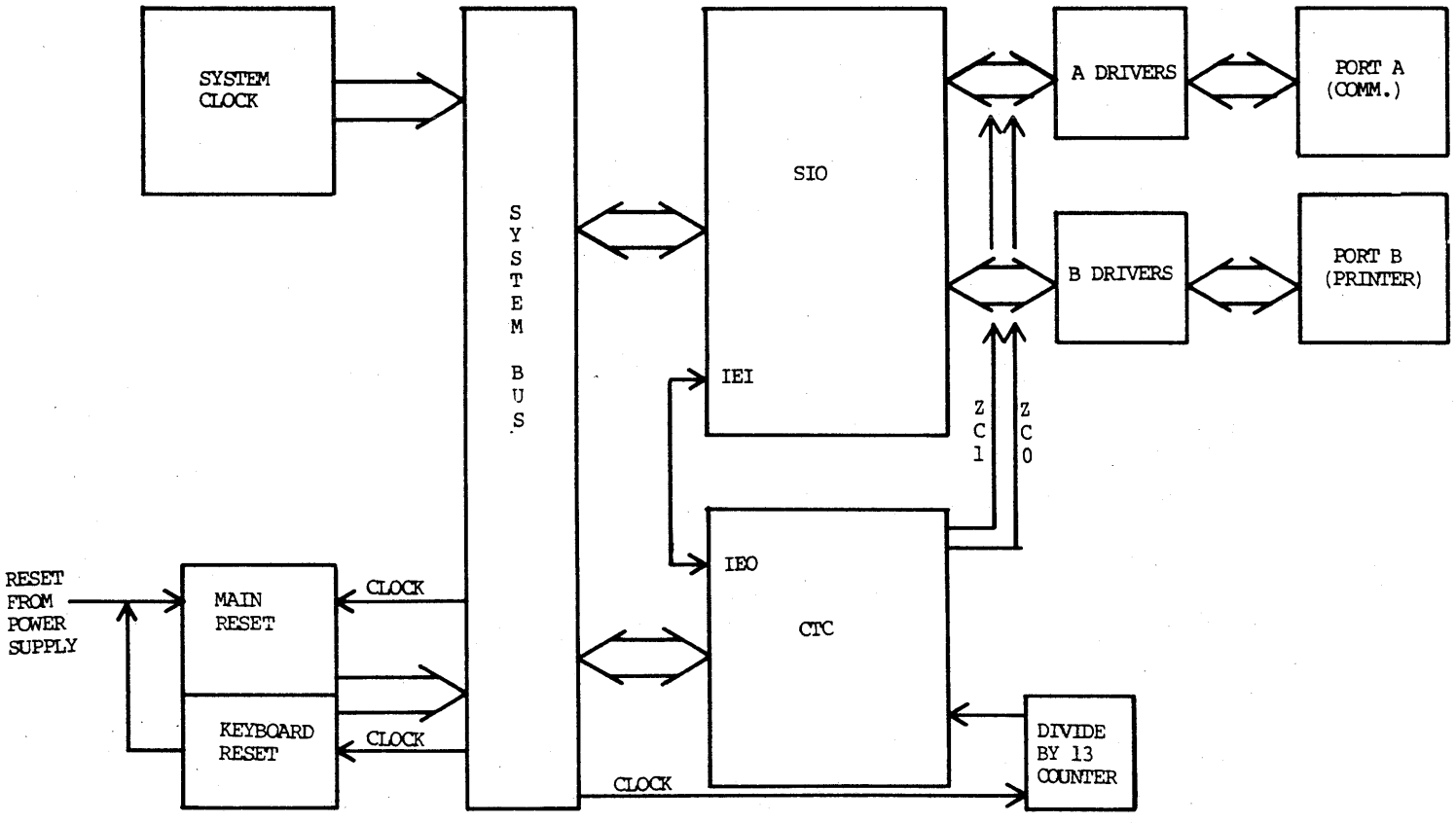


Illustration 2-9 Serial Block Diagram

Clock

The clock generator is an 8 MHz crystal oscillator (Q302). The 8 MHz signal goes to a flip-flop (U302), where the signal is divided by two to produce a 4 MHz clock signal. The output of this flip-flop (U302 pin 9) has a driver to ensure sharp edges on the resulting +5 volts to ground signal swing.

The same chip (U302) contains another flip-flop which divides the 4 MHz signal to a 2 MHz signal. This 2 MHz signal is used in several sections of the logic, such as the Direct Memory Access controller (DMA).

A Binary Divider (U307) provides two other frequencies: 500 KHz and 250 KHz. These frequencies are used by the floppy controller.

Additional circuitry in the clock generator is provided to allow a 6 MHz option in Attache, should one be used in the future. By changing jumper positions (J311) and changing the crystal oscillator (X301) to a 12 MHz crystal, the flip-flop (U301) circuitry is a divide by three counter. The 12 MHz signal is divided by three to produce the necessary 4 MHz clock, while the binary divider U307 provides a 6 MHz frequency to the system bus, as well.

Reset

The system reset provides a reset pulse to the processor without disturbing the contents of memory. This is important for debugging. For example, if a program were to loop or hang, the user can reset the system, enter Monitor mode, and display (or print via the "S" command) the memory contents at the time of the lock up.

Reset is synchronized with the M1 (machine cycle one) signal. The synchronization protects the memory contents, and ensures that the system does not reset before an M1 pulse is present.

U306 controls the timing of the reset state. A flip-flop (U303) receives an M1 signal from the system bus, and generates a pulse. At the next clock signal, this pulse shuts off, so the reset pulse to the flip-flop (U306) is one clock width.

The counter (U307) is used to determine the width of the reset pulse. The inputs to the counter are Reset and a 250 KHz clock signal. The 250 KHz frequency are pulses of 28 - 38 nanoseconds. This frequency is a clock input to U306, so the reset pulses are typically 28 to 38 microseconds long.

Serial Input/Output Controller

The Serial Input/Output controller (SIO) is a zero bonded Z80 SIO with dual synchronous channels. The SIO pins are described briefly. Refer to the Zilog Handbook for further detail.

Pin Functions

TxDA and TxBA (transmit data) transmit the data to the ports serially. RxDA and RxDB receives the data from the ports.

DTRA and DTRB (data terminal ready) are outputs to inform the external device that Attache is in a ready state.

RTSA and RTSB (request to send) is an output to the external device that the SIO wants to send data. CTSA and CTSB (clear to send) is an input from the port that the device is ready to receive data.

TxCA and TXCB (transmitter clocks), and RxCA and RxCB (receiver clocks) are the clocks driven by the Counter Timer Circuit. They generate the baud rate.

IORQ (input/output request) is used to signal the Central Processing Unit (CPU) that the SIO needs to transfer commands or data.

W/RDYA and W/RDYB (wait ready) are ready line outputs to the direct memory access (DMA) controller.

RES (reset) is an input which disables the ports.

INT (interrupt request) is an output signal the SIO uses to request an interrupt.

M1 (machine cycle one) is an input to keep the SIO functions synchronized with the processor.

RD (read cycle status) is an input signal from the CPU that a read data operation is in process.

B/A is used to access the proper SIO channel, port A or port B. C/D (control or data select) is an input from the processor that defines whether the transfer between the SIO and the CPU is data or control information.

CE (chip enable) is an input the CPU uses to select the SIO.

IEI (interrupt enable in) and IEO (interrupt enable out) are used to determine the priority of interrupts. IEI is input to the SIO from the CTC to signal the SIO that no higher priority device is being serviced. IEO is the output which then blocks any lower priority devices from interrupting while a higher priority device is being serviced.

SIO Operation

The SIO serves as the primary interface between the ports and the processor. Data is input to the SIO, and output serially to the ports.

The SIO channels require a clock sixteen times the baud rate. Consequently, a clock rate which is programmable for the applicable baud rate is provided by the Z80 Counter Timer Circuit (CTC).

A 4 MHz clock is input into a binary counter (U304). The counter divides the clock by thirteen, to produce a frequency of 307.692 KHz. This is approximately sixteen times the maximum Attache baud rate of 19.2 KHz. The clock inputs to the CTC go to the jumpers (J309, J310 and J312) which patch the ports to clock CT0 or CT1.

The buffers on the outside of each of these channels are approximately the same. The only difference is the receive and transmit clock lines are tied together in channel B, the printer port.

The channels may be programmed to function as synchronous or asynchronous ports.

The Ports

The ports are driven by driver/receiver chips which work with any of the peripheral standards: RS-422, -423, or -232. The standard used is selected by jumpers.

RS-422 is the most sophisticated line standard. It gives differential outputs accepted directly by the port. This differentiated output features enhanced noise immunization to allow cable lengths of 4000 feet.

RS-423 and RS-232 are single-ended. One of their inputs is grounded, the other input is the signal. RS-232 is most commonly used communication standard used by virtually every serial peripheral manufactured. The standard Attache jumper positions are set for RS-232. RS-232 cables may be 50 feet maximum.

RS-423 standards may be used without changing Attache's standard jumper positions. RS-423 allows cable lengths of up to 2000 feet.

The transmit lines use drivers (U313, U312, and U310). The drivers work differently according to the status of the input line named Mode. If Mode is low, the driver outputs will work as two differential drivers for RS-422 standards. The Transmit Data signal is output in both its true and its complement form. If Mode is high, the drivers work as four independent, non-inverting, single-ended drivers. This is used for RS-423 or -232.

The status of Mode is set by jumper J308 pins 1-3 for channel A (Communications) and jumper J307 pins 4-6 for channel B (Printer). The jumpers allow the Mode line to be patched to either +5 or to ground. These jumpers are set to ground for RS-422 standards, and to +5 for RS-232 or RS-423.

Jumpers J310 pins 4-6 and J306 pins 4-6 control whether the driver that controls the clock is on or off. (External or internal clocking.)

The jumpers to pin 8 on both transmitters (J312 and J304) go to either -5 volts or ground. This controls the voltage levels going to the transmit buffers. For RS-232 and -423, this should be patched to -5 volts because the signal swing is from +5 to -5 volts. For RS-422, this should be jumpered for ground to +5 volts signal swing.

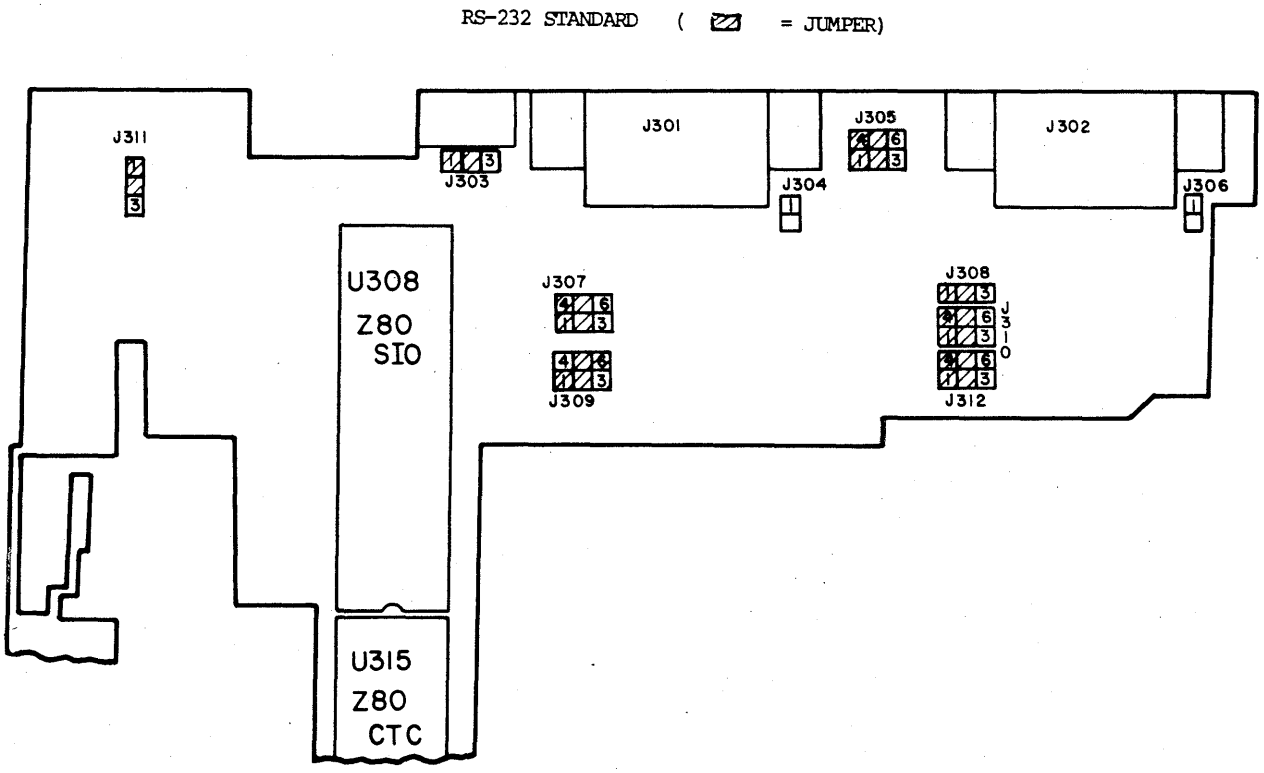


Illustration 2-10 Jumper Options

PORT A (COMMUNICATIONS)

Jumper	Function	Setting		RS-232 Jumper
J307 1,2	+5 volt output for external accessories	1-2 Jumpered +5 tied to conn. pin 15	1-2 open conn. pin 15 open	open
J308 1,2,3	Mode of Port A output drivers and Port B clock output driver.	1-2 Jumpered Single ended (RS-232,423)	2-3 Jumpered Differential (RS-422)	1-2
J312 1,2,3	Voltage swing of Port A output drivers and Port B clock output driver	1-2 Jumpered -5v to +5v (RS-232,423)	2-3 Jumpered 0v to +5v (RS-422)	1-2
J310 4,5,6	Direction of external clock pins for Differential (-422) (Set to Output for -232, 423)	4-5 Jumpered Clock output from Attache	5-6 Jumpered Clock Input to Attache	4-5
J310 1,2,3	Transmit Clock selection	1-2 Jumpered Internal clock	2-3 Jumpered External clock	
J312 4,5,6	Receive Clock selection	4-5 Jumpered Internal clock	5-6 Jumpered External clock	

PORT B (PRINTER)

Jumper	Function	Setting		RS-232 Jumper
J304 1,2	+5v output for external accessories	1-2 Jumpered +5v tied to conn. pin 15	1-2 Open pin 15 open	open
J307 4,5,6	Mode of Port B output drivers (except clock output driver)	4-5 Jumpered Single-ended (RS-232,423)	5-6 Jumpered Differential (RS-422)	4-5
J309 1,2,3	Voltage swing of Port B output drivers (except clock output driver)	1-2 Jumpered -5v to +5v (RS-232,423)	2-3 Jumpered 0v to +5 v (RS-422)	1-2
J307 1,2,3	Direction of External Clock pins for differential (RS-422) (Set to Output for -232,- 423)	1-2 Jumpered Clock Output	2-3 Jumpered Clock Input	1-2
J309 4,5,6	Transmit/Receive clock selection	4-5 Jumpered External clock	5-6 Jumpered Internal clock	4-5

Early Board versions contained additional jumpers that should always be set as follows:

Jumper	Setting
J303 1,2,3	1-2 Jumpered
J305 1,2,3	1-2 Jumpered
J305 4,5,6	4-5 Jumpered

Local RS-232 Device

RS-232C Pin	Function	Direction	Attache Pin
1	Ground	Not Applicable	1
2	Transmitted Data	To DCE	4
3	Received Data	From DCE	2
5	Clear to Send	From DCE	9
6	Data Set Ready	From DCE	3
7	Ground	Not Applicable	8
7	Transmitted Data Return	From DCE	11
7	Data Terminal Ready Return	From DCE	12
8	Received Signal Detector	From DCE	10
20	Data Terminal Ready	To DCE	5

Communications RS-232 Device

RS-232C Pin	Function	Direction	Attache Pin
1	Protective Ground Shield	Not Applicable	1
2	Transmitted Data	To DCE	2
3	Received Data	From DCE	4
4	Request to Send	To DCE	10
5	Clear to Send	From DCE	5
7	Signal Ground	Not Applicable	8
7	Received Data Return	To DCE	11
7	Clear to Send Return	To DCE	12
20	Data Terminal Ready	To DCE	9

Note: In local cable uses, Attache appears as a DCE to the peripheral. The peripheral appears as DTE to Attache.

Counter Timer Circuit

The Counter Timer Circuit (CTC) is used to generate the baud rates for the external ports, and in interrupt control.

Channels 0 and 1 are used to generate the clocks for the ports' baud rates. The clocks CT0 and CT1 are 16 times the maximum baud rate.

Channels 2 and 3 are used in interrupt processing as described in the following discussion, Interrupts.

A brief description of CTC pin functions follows. Consult the Zilog Handbook for further detail.

Pin Functions

IEI (interrupt enable in) and IEO (interrupt enable out) are signals used to control the priority of interrupts. IEI is the input which indicates no device of higher priority is being serviced. IEO is the output which blocks other devices of lower priority from interrupting while a higher priority interrupt device is being serviced.

CE (chip enable) is an input the CPU uses to enable the CTC.

INT (interrupt request) is an output signal to the CPU that a device on one of the CTC channels requires an interrupt.

M1 is an input signal from the CPU which keeps the CTC functions synchronized with the processor.

IORQ (input/output request) is an input used to transfer data and control words between the CPU and the CTC.

RD (read cycle status) is an input used in conjunction with CE and IORQ to transfer information between the CTC and the CPU.

RES (reset) is an input which disables the CTC.

CS0 and CS1 (channel select) selects one of the four CTC channels for an I/O transfer.

ZC0 and ZC1 (zero count) is an output which indicates the status of the interrupt.

CT0 - CT3 (external counter trigger) are inputs, one for each CTC channel. They are used to decrement the down-counter used for interrupts.

Interrupts

An interrupt is a signal sent to the CPU that an external device requires attention or use of the system bus. The interrupting device places an address on the system bus, which the CPU uses to locate the interrupt routine in the Basic I/O System. The interrupt routines are discussed in Chapter 3, beginning on page 3-48. A discussion of Attache's hardware for interrupt processing follows.

Two types of interrupts are generated by Attache devices: Floppy Interrupts and 60 Hz Interrupts. The hardware logic is also supplied to handle peripherals' interrupts from the SIO and the Expansion Connector. However, Attache Basic I/O System does not currently use SIO interrupts, as even the maximum baud rate does not necessitate interrupt usage.

The 60 Hz Interrupts and the Floppy Interrupts do not have all the information that the CPU needs to handle an interrupt properly. The signals do not give the processor their priority or their location. The internal logic in the CTC supplies this information to the CPU.

CTC signals an interrupt to the CPU and places an interrupt byte on the system bus. This is the low order of a two byte address used to locate the interrupt routine in the BIOS. DA {hex} is the start of the interrupt page, the high order half of the vector address.

Attache's interrupt handling is accomplished through two channels, channels 2 and 3. Channel 2 is the 60 Hz interrupt, with higher priority than channel 3, the Floppy Interrupt. Both channels are set to count down to one. Whenever they count down as a result of an interrupt, they generate the proper interrupt signals for the processor.

The 60 Hz frequency used by 60 Hz Interrupts is input from the CRT controller; the vertical retrace. The 60 Hz Interrupt signal continuously checks the keyboard for a signal indicating that a key has been pressed and several other functions. These functions are discussed in Chapter 3, page 3-52.

Illustration 2-11 depicts the logic Attache uses to allow I/O driven interrupt capability.

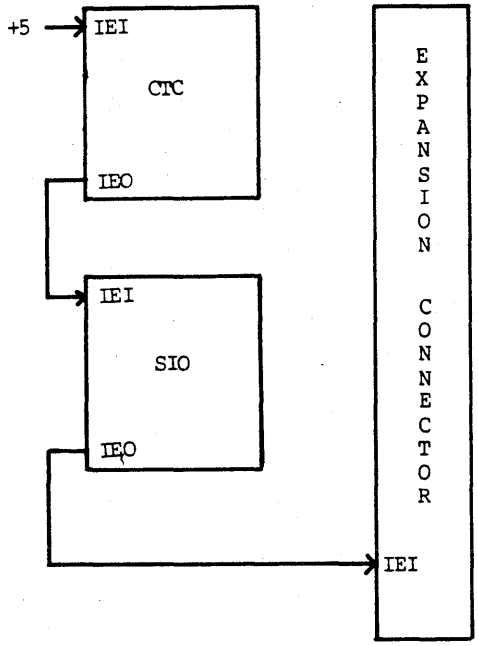


Illustration 2-11 Daisy Chained Interrupts

The logic for peripheral interrupts is set up in a daisy chain. The interrupt signals are coupled through IEO and IEI. This assigns interrupt priority. The IEI line is the higher priority interrupt, the IEO is the lower. Since the SIO chip is below the CTC chip in priority it is tied to the CTC's IEO. IEO from the Serial Input/Output controller goes to the Expansion connector. This is the lowest priority.

Refer to Chapter 3, page 48, "Interrupt Structure" for more information on interrupts.

Display

The display section of the processor board controls the Attache display module. The logic performs CRT control, reading and writing to display memory, timing aspects, screen attributes, and graphics.

The circuitry contained in the CRT module itself is described in the Display Module section of this chapter. However, a brief introduction to CRTs follows.

The display block diagram, Illustration 2-12, is located on the following page.

The graphics block diagram, Illustration 2-25, is located on page 2-56.

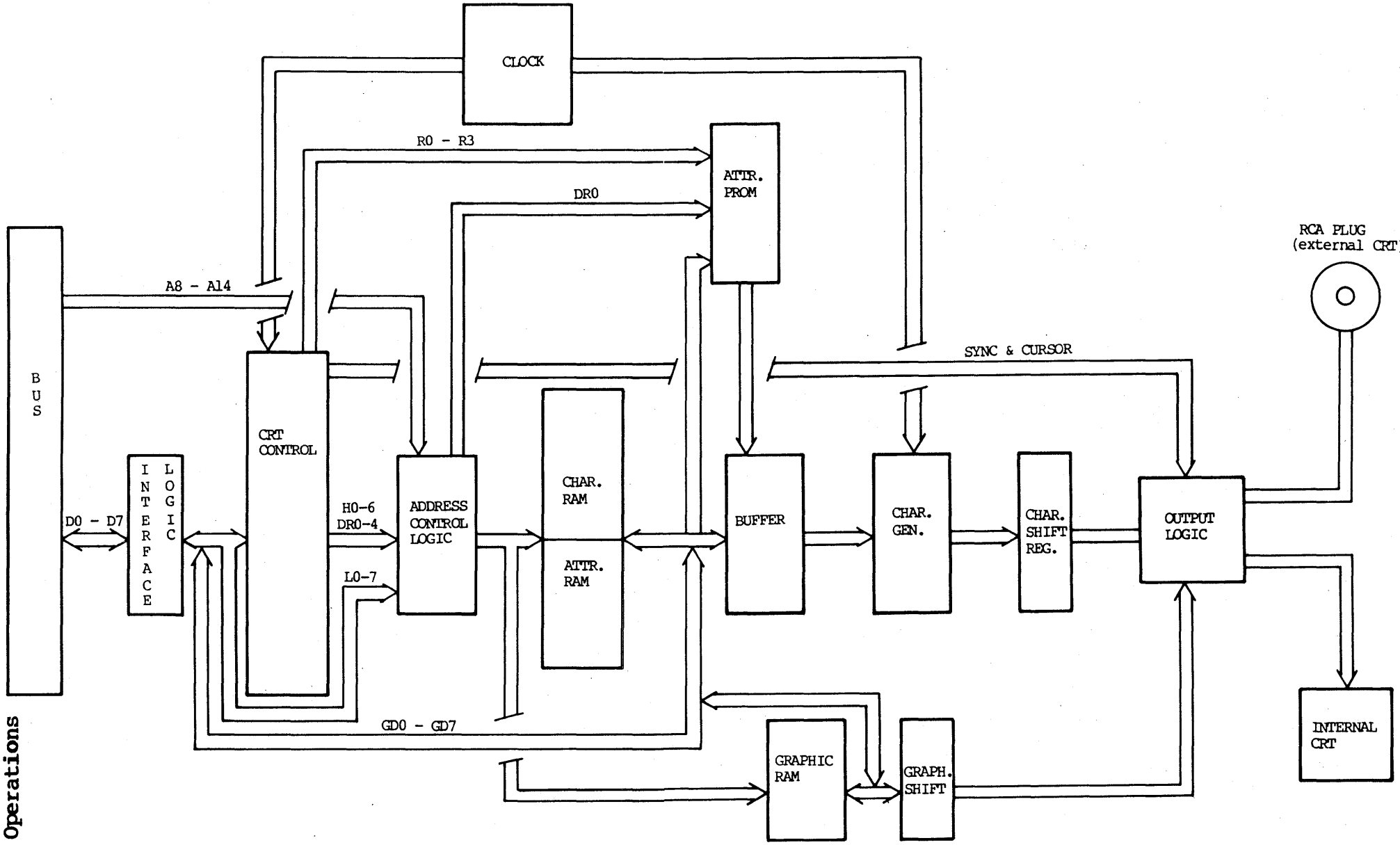


Illustration 2-12 Display Block Diagram

Cathode Ray Tube (CRT)

The Cathode Ray Tube (CRT) produces an electron beam which scans the screen. The background of the screen is composed of a phosphorous material which glows when charged by the electron beam. Horizontal and vertical deflection coils in the display module cause the beam to move across the screen.

The scan starts at the upper left hand corner and moves to the right hand corner. It then retraces to the left, one scan width lower. This process repeats ten times for each line on the screen, 240 times per screen. (There are 24 lines on the Attache screen.) From the bottom left hand corner, the scan returns diagonally to the upper left hand corner.

The horizontal and vertical retraces are blanked out with a signal called "blanking pulse" to keep the return scans from being seen. Refer to Illustration 2-13.

The frequencies required for the beam sweep are generated in the display module: the sawtooth wave frequency and the lower frequency vertical scan. The control chip generates the signals which keep these frequencies synchronized.

The video display is driven by two output signals: internal video and external video. Internal video contains the vertical pulses, horizontal pulses, and the video signal. External video, also called composite sync, contains all of the information necessary to generate the display (the data, the cursor location, and sync pulses).

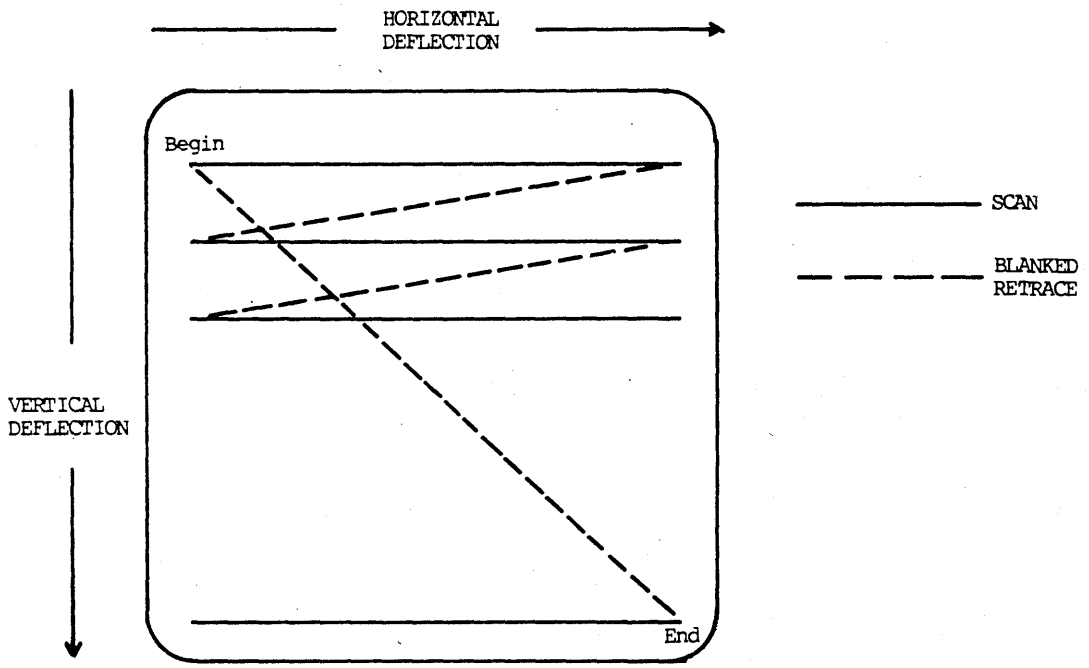


Illustration 2-13 CRT Screen

CRT Controller

The CRT controller is programmed during system initialization with specific information pertaining to the Attache CRT. This includes such information as the number of lines on the display (24), the number of visible scans per line (10), the number of blanked scans (262), and the number of characters on each line (80).

For European operation at 50 Hz, the CRT controller is initialized to refresh the entire screen at 50 frames per second, 24 lines of 10 scans each, and 312 blanked scans.

The controller outputs all of the timing signals necessary to control the display (vertical sync, horizontal sync, composite sync). The controller also determines cursor positioning, the blanking pulse, and display RAM addressing.

The CRT controller's pin functions are described briefly. Consult the Standard Microsystems Handbook for further information.

Pin Functions

Three sets of output lines are used in conjunction to constantly address the exact location the beam is to write on the display:

H0 - H6 are the Character Counter Outputs. This seven bit address determines the horizontal character position.

R0 - R3 are the Scan Counter Outputs. This counts through for each of the ten scans which form a character on the CRT line.

DR0 - 4 are the Data Row Counter Outputs. This counts to the line position the display is currently addressing.

CRV (cursor video) defines the cursor location on the screen. BL (blank) is an output pulse which blanks out the horizontal and vertical retraces. H Syn (horizontal sync) initiates the horizontal retrace. V Syn (vertical sync) initiates vertical retrace. C Syn (composite sync) provides a composite wave form.

DS (data strobe) is an input which strobes the data from the data bus into the appropriate internal register, or strobes the cursor address onto or from the data bus. CS (chip select) signals the CRT controller that it is being addressed.

A0 - A3 are input register address bits for selecting one of the internal CRT controller registers.

DB0 - DB7 is the bidirectional data bus used for initializing the CRT controller.

Timing

A 12.324 MHz crystal supplies the initial clock. Each clock pulse is the time that it takes to write one dot to the display. This is called the dot clock. A counter (U429) divides the clock by eight, so each output clock pulse from the counter is one character length. (Each character cell on the Attache display is 8 dots wide.)

A character is written on the screen one scan at a time. The CRT beam starts in the upper left hand corner, writes the dots for the characters on this scan, moves all the way to the right, returns, writes the dots for this next scan, and returns. This requires ten scans for each line of characters. The timing must therefore be kept absolutely constant between the amount of time it takes the beam to move one scan length, and the amount of time it requires to return. Otherwise the scans' placements of dots to form a character would not match.

When the CRT beam reaches the right of the screen, some time has to be allocated for the beam to return to the left. This time interval is the CRT controller output, Blanking Pulse (Pin 17).

The Dot Clock continues to count during the blanking pulse. The blanking pulse's frequency is therefore kept the same as one scan's frequency. This ensures that the signal is still synchronized at the start of the next line.

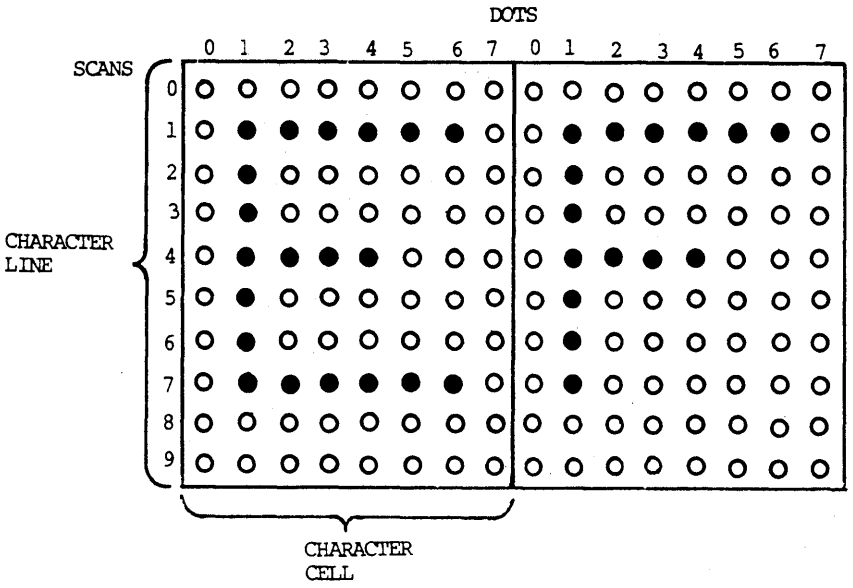


Illustration 2-14 Video Characters

In the example in Illustration 2-14, scan 0 of "E" and "F" is written; the beam returns and writes scan 1 of both characters. The process occurs ten times per character line. The beam uses the same time interval for each scan, and each retrace.

Timing is interfaced between the processor and the display module via the connector (J501 on schematic page 5). These timing signals are the horizontal sync, and the vertical sync. The horizontal sync is a pulse which occurs once for each scan line and times each trace. The vertical sync controls the oscillator in the display which generates the timing for the vertical motion of the beam.

Note: The video signal is also input to the display module through connector J501. The video is the beam control information going to the screen; (ie. the voltage to control the intensity of the beam).

Latching is used in various stages. This is required because of the different access times of the RAM (U432) and the ROM (U416). Consequently, some of the outputs are delayed. This is called "pipe lining."

For example: a given character cell is addressed. The data comes out of the RAM, and is then latched into latches (U414 and U415). During the next character time the ROM is accessed. So, at the end of that access time the output is latched into a shift register (U417). This means the data is actually two character cell locations behind its original address. In order to compensate, the sync signals are latched once internally, then are latched again (U412). All lines are delayed once more by register U419 alleviate timing differences caused by the combination of latches.

The character cycle (the time required to write one character) is divided into a CPU write cycle and a Display write cycle. This is to prevent data from being written to the display while the CPU is in the process of changing it.

Illustration 2-15 summarizes the timing aspects of the display, depicting the display sections waveforms.

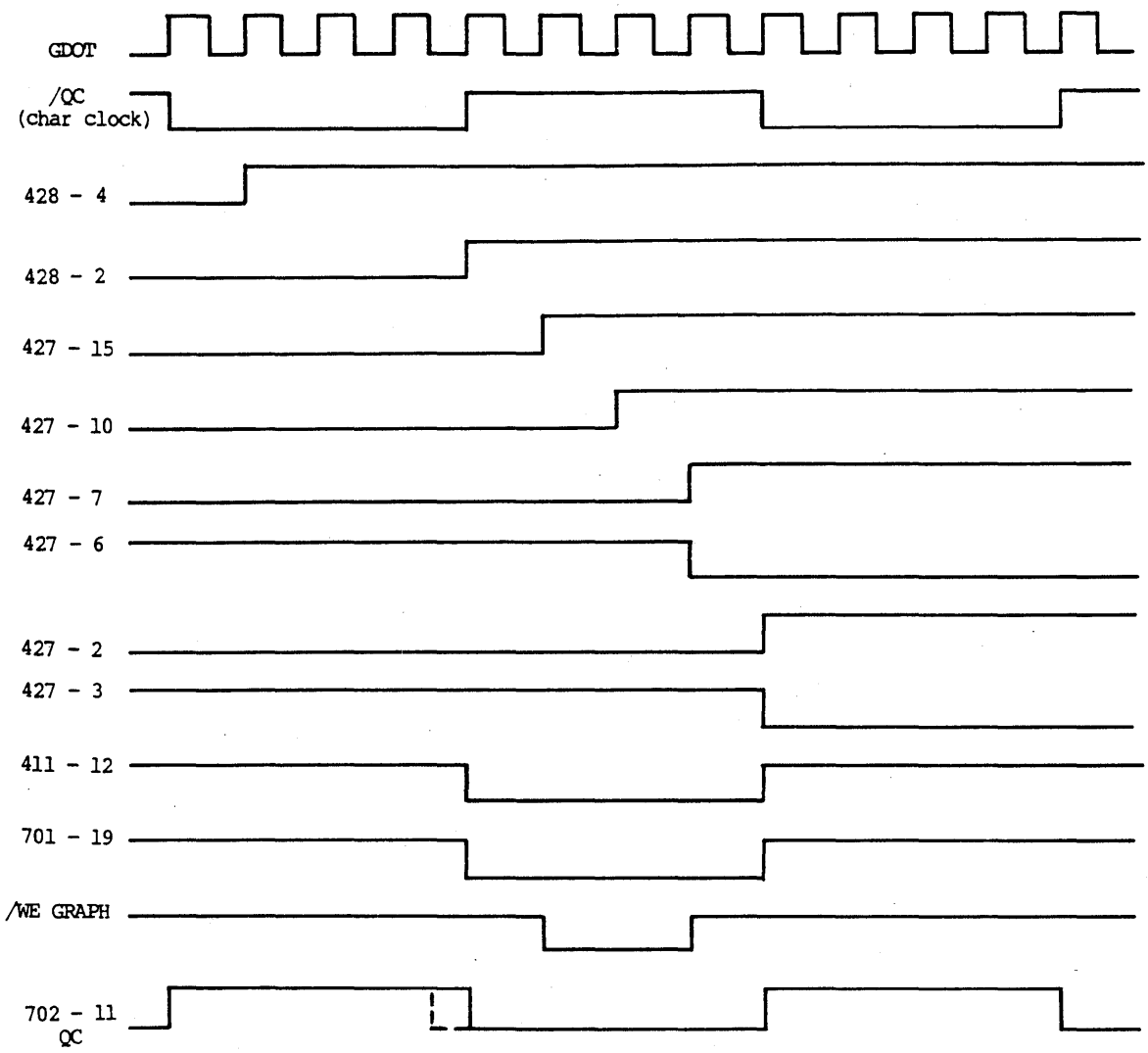


Illustration 2-15 Display Timing

During the display cycle, the display reads from the display memory. During the CPU cycle, the CPU writes to or reads from display memory. The CPU only uses its cycle if the CPU has information to transfer. Halving the cycle ensures data is not written from the CPU to the display at the same time as the display is accessing its memory. The flip-flops (U427 and U428) maintain the proper synchronization for these cycles.

Reading or Writing to the Screen

Two types of data transfers to the screen are possible: the reading from display memory that always occurs as a function of maintaining a screen, and writing that the CPU initiates to change the data on the screen or to display messages. The multiplexers (U422, U431, and U430) with selectable gating allow the video RAM chips to be addressed by either a write from the processor, to change the video data; or a read from memory addressed by the CRT controller, to refresh existing data.

The logic in the CRT controller sequentially addresses all of the screen's character positions as the screen is scanned, addressing the data stored in display memory to be written. For the CPU to write to the screen, the CPU must take over the memory addressing. The CPU writes to the proper RAM address; this data is then transferred to the screen.

The logic for reading or writing to the screen is discussed in two parts: selecting the address, and writing (or reading) the data.

Selecting the Address

The addressing bits from the CPU are stored initially in internal registers within the CPU, and external register U404. Register U404's upper three bits decode to one of five graphic segments, the CRT controller, or the attribute or character RAM. The lower five bits are the CRT's line number. Register B contains the character position on that line; the upper address bits (A14 - A8), input directly into multiplexers (U431 and U430) to address the RAM. The external register A contains the data to be sent. Register C contains the display port address bits, Ddspy (Data Display).

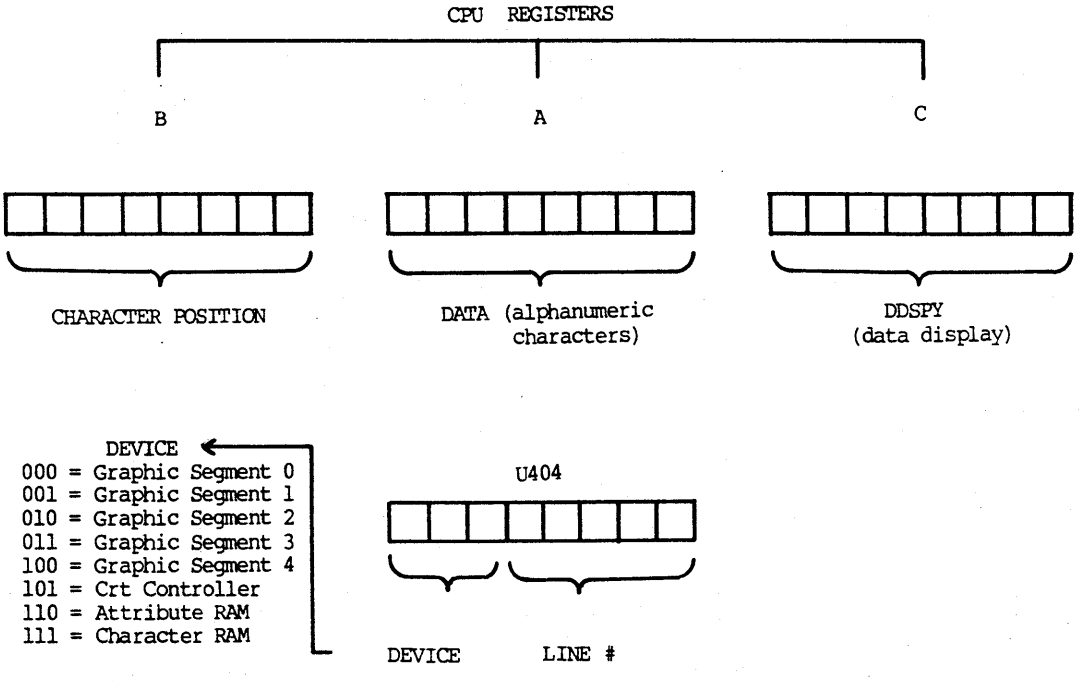


Illustration 2-16 Addressing the Display

As depicted in Illustration 2-16, latch U404 contains the three upper order address bits which select the specific display device. These upper bits are multiplexed by U405. The signals are multiplexed such that during a CPU transfer they are direct inputs to decoder U426. The decoder can select one of five graphic RAM chips, the CRT controller, the Attribute RAM, or the Character RAM.

The CRT controller is selected during initialization. The CPU writes screen parameters to the controller at this time. The RAM banks, alphanumeric or graphic, are selected when the CPU transfers data to the display.

The select signals from U426 to the RAM chips are gated. In most cases of alphanumeric data, both U433 and U432 are selected because the screen attributes are generally included with the characters.

The "A" input lines of the multiplexers (L1 - L4 of U422) select the proper line on the CRT. A14 - A8 into multiplexers U431 and U430 select the character address within that line. The CPU puts the ASCII character to be displayed on the data bus, and selects the "A" side of the multiplexers to address the data.

The outputs of the address multiplexers input to an adder (U423) which is used as a means to use memory more efficiently. In display RAM, the minimum number of necessary address lines results in more address combinations than are actually used. The adder strips off the unused address combinations.

The number of input lines necessary to designate a number in hex is equal to the positions needed to represent the number in binary. For example, to designate the number 8, four lines are necessary; (1000 binary = four positions). So, four input lines would be the minimum number of lines required to address an 8, whether or not the addresses 9 - F (hex) were used.

The number of character positions, 80 needs 7 lines, and the number of character lines, 24 needs 5 lines, leaving many unused address combinations. Therefore, to utilize the invalid RAM address combinations, some of the upper address bits of the CRT lines and character positions are combined by U423. RAM is consequentially used more efficiently, as the otherwise unused addresses are reassigned.

Writing Data on the Screen

Data to be written are in the form of ASCII character and attribute codes. These data are gated through the Transmit / Receiver chips (U424 and U425) to the display memory. U425 gates attributes, such as highlight or boldface, while U424 gates the characters.

The EPROM combines data from the Attribute RAM (subscript, superscript, double size, and underline) and the character RAM, and translates this to generate eight bits. These eight bits correspond to the eight dots which comprise one scan for a character. This process repeats a total of ten times to write the ASCII character.

The EPROM shifts the character into U417, where it is serially shifted into U418, and then to the analog diode - resistor network. This network multiplexes the attributes and cursor, separates the internal from the external video, and routes the resulting signals to internal video or external display.

The CPU writes to the display by placing data on the data bus and activating the signals /IOWR and /CRT. Both signals /IOWR and /CRT at a true state activates signal /CRTWR, which gates the data through buffer U403, onto the display data bus.

/IOWR and /CRT cause flip-flops U427 and U428 to output a display wait state back to the CPU, which allows the address time to establish on the bus. The flip-flops also output write pulses. The write pulses are gated to the multiplexers (U422, U431, and U430) and cause the multiplexers to select the CPU address inputs ("A" input lines).

The proper display RAM is selected according to the high order device address selected by the CPU. Normally, both the attribute and character RAM chips are selected. The flip-flops write pulses clock the data from the display data bus, through the transmit - receiver chips (U424 and U425), to the character generating circuitry.

Reading from display memory to the CPU incorporates the same principles as a CPU write operation. The inputs /IORD and /CRT are true, and A4 is low. This activates signal /CRTRD which enables flip-flop U402 (instead of U403 in a write operation). The transmit - receiver chips (U424 and U425) transfer data from their A side to their B side (instead of B to A in write) and into flip-flop U402.

Refer to Illustration 2-15, page 2-35 for additional timing information concerning display writing and reading.

Attributes

There are two different sets of screen attributes on Attache which may be selected for each character to be written on the screen. One set of attributes is sent to the character generator to be output with the ASCII character code. These attributes are: subscript, superscript, and underline. A second set of attributes: bold, highlight, reverse video, and alternate character set are delayed, then shifted to internal video. The attribute Double-size requires a separate portion of logic.

Although a character is ten scans high there is actually room for sixteen scans of information for each character in the character generator PROM. The final two scans for each character are used to store the information for the attributes.

Subscript, superscript, and underline are decoded by a PROM (U413). The attribute affects the character code sent to the video according to the character generator's programming. An underline represents a solid bar. Strikethrough is the same code as underline, except it is written in scan four of the character, while underline is written in scan ten.

Subscript adds one scan count to the characters scan line input. The character is thereby translated so that the data otherwise intended for scan 0 is now the data for scan 1. As a result, the data to be written to the screen is one scan lower. Conversely, superscript shifts the data up one scan.

Double-size requires a separate section of logic. The logic uses flip-flops to cut the character counter clock in half. The circuitry cuts the clock rate going to the shift register sending out the characters, and it inhibits the load signal at the end of the first character time. It regenerates a load signal at the end of the second character time. So, this circuitry spreads one character over two character times by only using every other clock pulse and every other load signal.

The attribute data to the PROM may be used in combination, with one exception. As subscript and superscript for the same character is mutually exclusive, their combined code is a strikethrough.

Bold, highlight, reverse video, and alternate character set are sent to the video without being translated by the attribute PROM (U413). These signals are instead input directly to buffer U414, then to latch U412.

The CRT controller sends into latch U412 the following signals as well: cursor video, which indicates the cursor address and that the cursor is displayed; blank, which is the blanking pulse for retrace; the CRT sync signals; and video. The latch has output lines to a multiplexer, U418.

U418 is a multiplexer selector which is driven by video, graphics, and the Exclusive OR of Reverse Video and Cursor. Any combination into the multiplexer generates the proper two attribute levels. The screen can therefore output four brightness levels: Black, high intensity, low, and medium intensity. Highlight, for example, uses medium intensity for the character, low intensity for the background. Boldface uses high intensity for the character, black for the background.

Latch (U412) delays the attribute set by one clock pulse. Attributes are therefore presented to the CRT at the same time as the first set of attributes, previously delayed by the PROM's access time.

Graphics

The bus (GD0 - GD7) into the flip-flop (U403) is a common bus to the attribute, character, and graphics RAM.

Graphics use a RAM in parallel with the character generator. Graphic data enters a delay latch (U418) and are sent to the display by the same external circuitry the character display uses.

A character cell is 10 scans by 8 dots. Scans, however, are twice the length of a dot. Consequently, graphics combines a pair of dots per scan, so four graphic dots comprise the width of one alphanumeric character cell.

A character cell is divided into five segments. Each segment has eight dots. Each of the five graphic RAM chips address one of the segments in the character cell. In order to fill one character cell, five bytes of data must be sent, one from each RAM chip.

U701 is a buffer for reading or writing data into the graphic RAM segments. Chip select comes from U426. A quad multiplexer (U702) with a built in latch performs the signal combining and timing necessary to select graphic storage.

U703 is an eight-bit shift register. The dot pairs are combined on its input lines. According to which scan row is to be addressed, either the upper or the lower four bits of data are selected, and the data goes to the corresponding four dot address.

The bus to address graphics for read and write occurs at GD0 - 7. The same addressing scheme is used, and the same timing principles are used as in generating alphanumeric video data.

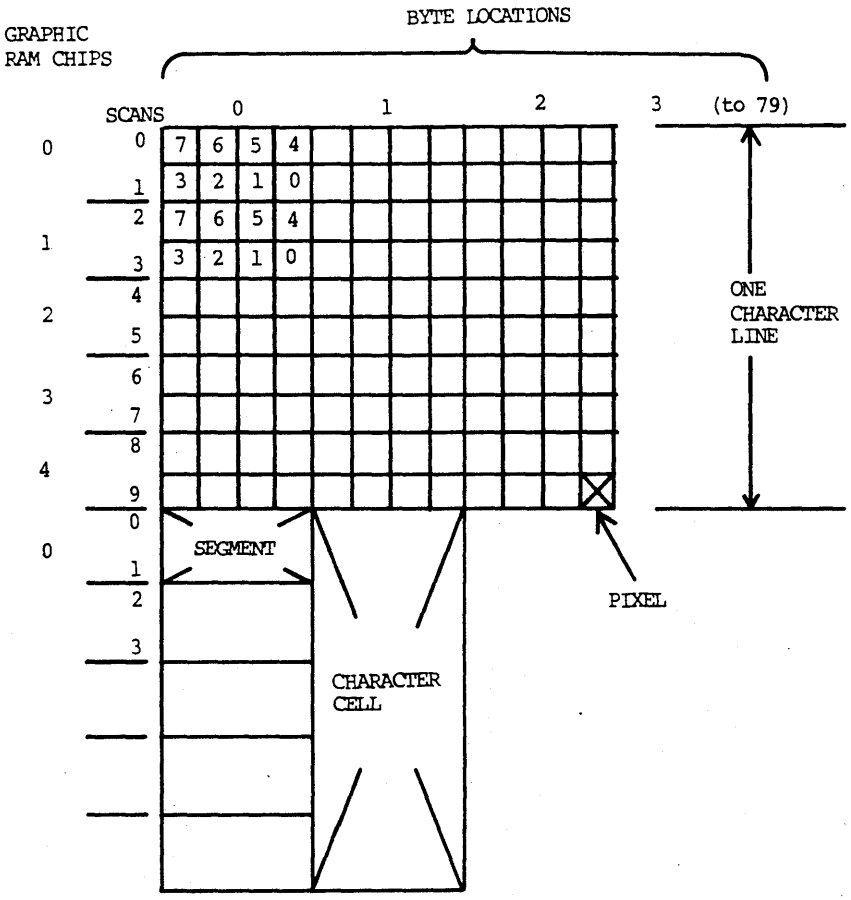


Illustration 2-17 Graphic Pixels

Input/Output and Real-Time Clock

The Input/Output and Real-Time Clock (I/O RTC) section of the board contains the Parallel Input/Output controller (PIO), the sound generator, CMOS RAM (Complementary Metal-Oxide Semiconductor Random Access Memory), a control latch, and a Real-Time Clock (RTC). The I/O - RTC section also contains the keyboard connector.

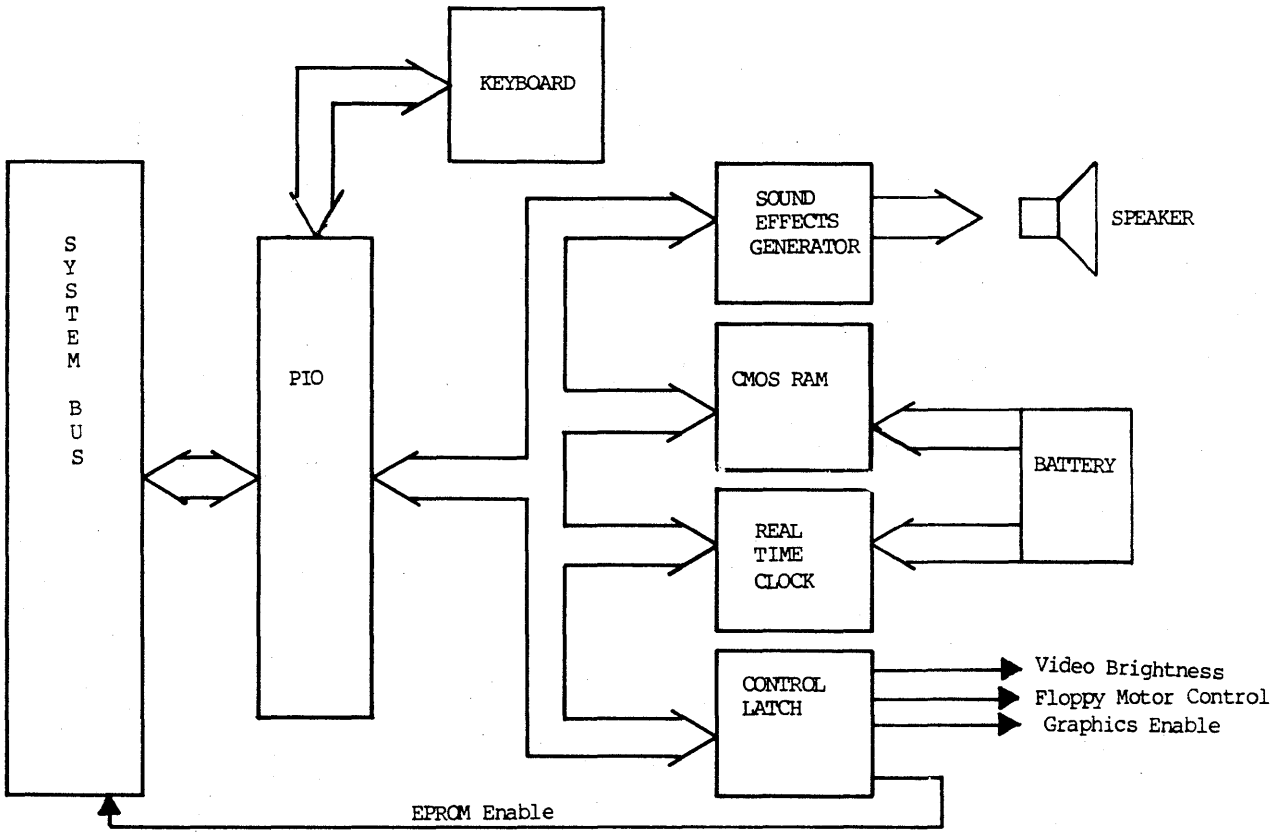


Illustration 2-18 I/O - RTC Block Diagram

Parallel Input/Output Controller

The Parallel Input/Output controller (PIO) Attache uses is a dual channel, programmable Z80 PIO. The sound generator, keyboard interface, RAM for set-ups, and the Real-Time Clock all interface with the system through the PIO. A PIO controller is used to allow latching on data to the chips and to limit the amount of capacitive loading on the bus. Direct interface to the bus would result in five additional loads on each data line.

The pin functions are described briefly. Consult the Zilog Handbook for further detail.

Pin Functions

Address lines A0 - A7 and B0 -B7 are bidirectional bus lines for each port. B lines in Attache are used for control functions. B2 - B4 generate a code that indicates which device is accessed. Data is strobed into the selected device or from the device by pulsing line B5 low.

CE (chip enable) allows the PIO to accept command or data transfers with the CPU.

B/A (port A or B select) defines which port is accessed during a data transfer between the CPU and the PIO.

C/D (control or data select) defines the type of data transfer to be performed between the CPU and the PIO.

D0 - D7 is the system data bus.

IORQ (input/output request) is used in conjunction with B/A, C/D, CE and RD to transfer commands and data between the CPU and the PIO.

Sound Effects Generator

The Sound Effects Generator is a General Instruments AY-3-8912. It produces the keyboard feedback sounds and any additional sounds for which the Attache is programmed. The audio generator is U506. Data are written to the generator by putting data on the data bus (A0 - A7) from the PIO.

The sound generator uses this PIO bus as both an address and a data bus. The function of the bus is determined by the Channel B output lines from the PIO. Lines B2 - B4 are decoded by U502. BDir determines whether the chip is reading or writing, and BC1 determines whether the bus is used for data or address bits.

When PIO lines B2 - B4 are set low and line B5 is pulsed low, an address is loaded from PIO Channel A into the generator. This selects a generator register. When B2 is high and B3 - B4 are low, data is loaded into the previously selected register.

Analog Channels A, B, and C are combined to form the waveform sent to the audio amplifier (U505). The amplified signal is then sent to the connector on the power supply (J501) to drive the speaker (located in the power supply).

CMOS Random Access Memory

The CMOS RAM (Complementary Metal-Oxide Semiconductor Random Access Memory) stores the set-up information such as baud rates and keyboard feedback volume. The user may specify these values, or leave them at a default. The values are stored indefinitely in CMOS RAM unless changed by the user. They are automatically read from the RAM during system boot.

The status of line R/W (Read/Write) determines whether the data bus to the RAM will be used to read data from the RAM or write data to the RAM.

The addressing of the CMOS RAM is supplied by lines A4 - A7 of PIO's Channel A. Two additional RAM address bits are supplied from lines B0 and B1 of the PIO.

CMOS lines D0 - D3 are bidirectional data lines, input from PIO lines A0 - A3. Data are either read or written on these lines, according to the status of the Read/Write input line.

The CMOS RAM is powered by a battery, which maintains data integrity even when Attache is powered off.

Control Latch

Set-up control, additional to data in the CMOS RAM, is controlled via a latch (U508). The upper five bits of the latch control a software programmable load to video intensity. The latch varies the resistance on the ground to the internal video, and as a result, varies the screen brightness.

The signal /EPROM Enable generates when the control latch is reset. This signals the EPROM (U252) to load the bootstrap to bring up the system.

The latch also generates Graphic Enable. Graphics can therefore be written to graphics memory without display, and then be presented to the display as the complete screen of graphic information.

One bit of the latch enables the floppy motor.

Real-Time Clock

The Real-Time Clock performs date and time of day functions for Attache. One of two brands of RTC's can be used in the Attache. The Attache software detects which type of RTC is functioning, and selects the corresponding RTC dependent software.

The RTC uses a 32.768 KHz oscillator which serves as the time base for the circuit.

The RTC contains several registers that increment from once each second to once each year. The specific register is selected by the status of the address lines, A0 - A3. These connect to A4 - A7 of the PIO.

D0 - D3 are bidirectional bus lines controlled by the input line Read/ Write, and connect to A0 - A3 of the PIO.

Power is supplied to both the RTC and the CMOS RAM by a battery (Input VCC of CMOS, VDD of RTC). This maintains the functions of the chip even when Attache is powered off.

Keyboard Interface

The I/O RTC section of the processor board contains the connector to the Attache keyboard (J502). Lines B6 and B7 of the PIO offer simple serial interface to the keyboard. Refer to "Keyboard" page 2-67 for additional logic information concerning the keyboard.

The keyboard logic monitors all the keys. When the logic detects a pressed key, it pulls data line 4 of connector J502 to a low level. U511 is a voltage comparator which senses the low signal from line 4, and sends a high signal to B6 of the PIO. The internal PIO logic recognizes the B6 signal as an indication of a pressed key.

The processor monitors PIO line B6 to check for a character waiting. If a character is waiting, the processor sends clock pulses to PIO line B7, and serially reads the 7 keycode data bits (plus shift and control bits) on B6. The processor then translates these bits into an ASCII keycode, corresponding to the key pressed.

The voltage comparator (U511) is also used to detect system reset from the keyboard. The comparator checks for specific voltage levels from the keyboard. If the voltage level is below one and a half volts, this indicates a reset. The comparator then generates the signal KB Reset. The comparator also checks the POK (Power Okay) line and generates a PB Reset signal accordingly.

The POK line is delayed through a resistor - capacitor network to protect the EPROM Enable, CMOS RAM, and RTC from being written to erroneously while the power level is changing.

Power for the keyboard is supplied by a +12 volt line on pin 2 of the keyboard connector. The line uses resistors to protect the keyboard.

Floppy

Logic for the floppy is composed of a 765 floppy controller, the bus connector to the two floppy disk drives, and additional logic components on the driver side of the floppy controller.

The logic for controlling the floppy disks may be divided into two basic categories: logic for the basic mechanism of the drives, such as head selection and enabling the motor; and logic for reading and writing.

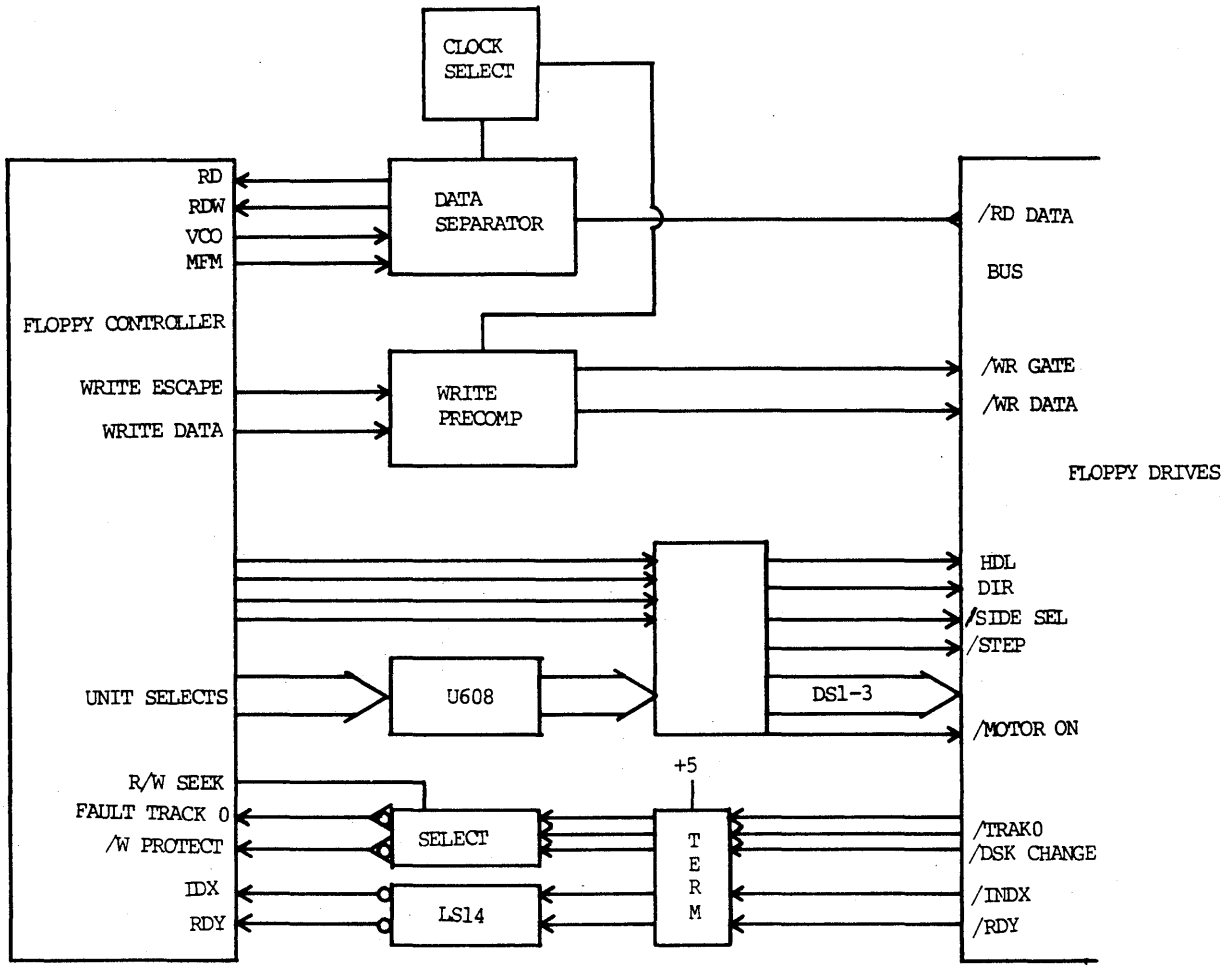


Illustration 2-19 Floppy Block Diagram

Basic Mechanism

The basic mechanism logic concerns such functions as moving the heads and turning on the drive motor. This is accomplished through the use of status lines.

Several status signals go from the floppy disks into the floppy controller. Their functions are: write protect, track 0, disk change, index, and ready. All of these signals are terminated. This produces additional noise immunization, and pulls the signal swing from a 0 - 2.5 volt swing to the full 0 - 5 volt swing.

Write Protect tells the controller whether or not data may be written on the diskette in the selected drive. An LED on the drive detects the presence of a write protect notch on the diskette.

Track 0 is the outer most track on the diskette. This signal is used to reference the location of the head on the diskette.

The "index" on the diskette is a small hole in the diskette itself. The Index line is used to count revolutions and to aid in determining head location on the diskette track. Ready tells the controller that the disk is up to speed. Disk Change is referenced in Attache software.

The functions of the status signals from the floppy controller to the drives are as follows: Direction Control, Head Load, Side Select, Motor On, Unit Select 0 and 1, and Step Control. The drivers for these signal lines are open collectors, allowing Attache to select either disk drive and bring the data back on a common set of lines.

Direction and step are used to "step" the head to the proper location for writing or reading. Head load is not used, as the heads are mechanically loaded when the drive door is shut. Side selects the proper side of the diskette.

Motor on is controlled by the processor to allow the disk drive motor to be shut off when the drives are not in use. This saves power and diskette wear. Unit select 0 and unit select 1 are inputs to a selector which decodes them into four signals. This allows the capability of four drives, though Attache currently uses two. The drives use the input drive selection signals 1 and 2.

Read/Write

Most of the logic in the floppy circuitry concerns the read/write process. The logic units involved in the read/write process are: the write precompensation, the clock select, the data separator, and additional logic contained in the floppy controller.

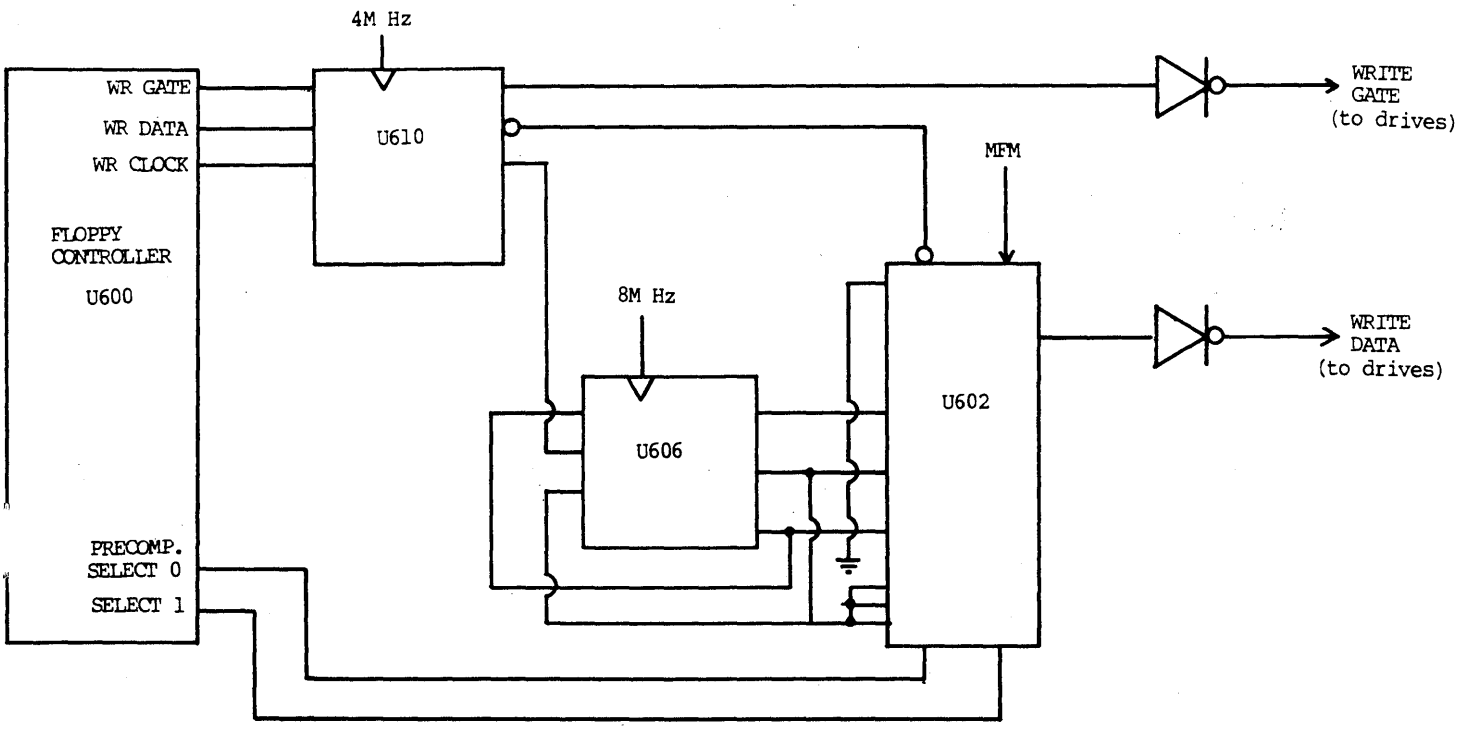


Illustration 2-20 Write Precompensation

Writing Data on the Diskette

The encoding circuitry involved in writing data on the diskette uses Write Precompensation. When writing data on a diskette, it is necessary to record both the clock pulses and the data pulses on the same track. This means that two pulses are often recorded close together. Due to the width of the head and the magnetic effects of the media, there tends to be a combining of the two signals. Consequently, when this data is read back, the pulses appear to be at a different location then they were actually written. This phenomenon is commonly called bit shift.

Write precompensation "compensates" for this by anticipating the distortion. The precomp logic writes the data initially to a location which will appear correct when the data is read. This is accomplished by either delaying or advancing the signals by 125 nanoseconds.

The input signals to the precomp logic from the controller are: write gate, write data, write clock, precomp select 0, and precomp select 1. The floppy controller attempts to present all of these signals at the same time, which would cause important time delays to be lost. The latch (U610) delays the write gate and write data by 250 nanoseconds, so that the precompensation select lines are properly settled before precomp receives data signals.

The next flip-flop (U606) causes the actual precompensation on the diskette write by delaying or "accelerating" the data signal. The flip-flop is clocked at 125 nanoseconds. Since a signal cannot be accelerated, the flip-flop actually delays the precomp input by two clock pulses. Data to be accelerated, then, is not delayed. Data to be written at normal time is delayed by one 125 nanosecond clock pulse, and data to be delayed is delayed twice.

Jumpers to J604 allow Attache the proper write precompensation circuitry for 8 inch floppies, which use precompensation only some of the time. The standard jumper position allows Attache to use precompensation in normal operation, (using MFM on double density 5 1/4" diskettes).

MFM and FM

The data and the clock pulses are recorded on the same track. In FM, the clock pulses are sent to the diskette, and the data is put between two clock pulses. This, however, limits the capacity of the diskette because there is a limitation to how close any transition, data or clock, can be placed together. The limitation is caused by the physical limitation of how quickly the diskette drive's head can reverse its magnetic fields.

Frequency Modulation (FM) requires a clock transition per bit of data. Modified Frequency Modulation (MFM) doubles the capacity of the diskette by eliminating unnecessary clock transitions. This allows data pulses to be written twice as closely as FM, as there is no clock transition until two zeroes of data. Since fewer clock transitions are present, more data transitions can be present, so write frequency is doubled.

The "missing" clock pulses in MFM are resynthesized later after the data is read back from the diskette.

Illustration 2-21 depicts FM and MFM clock and data signals.

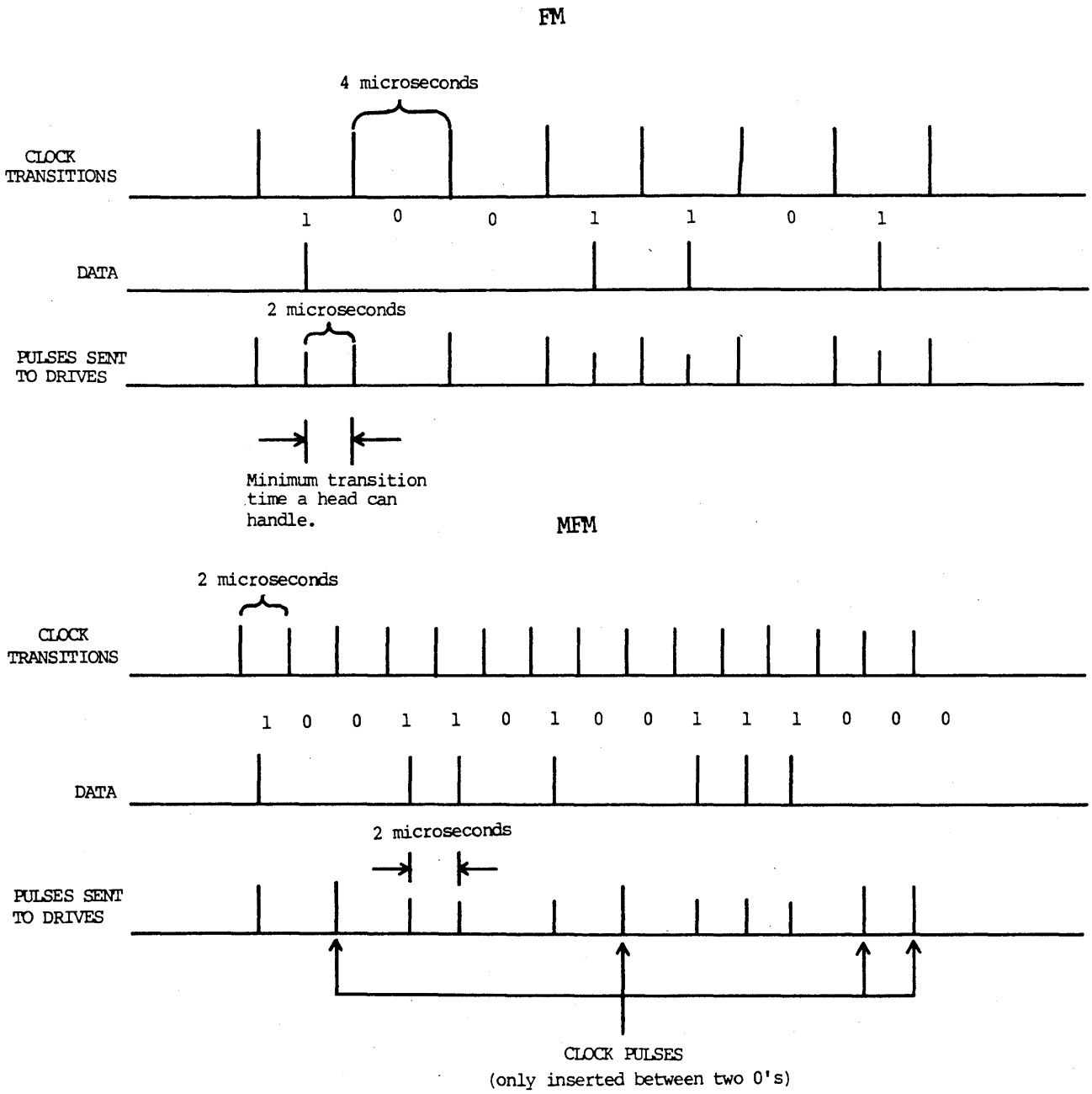


Illustration 2-21 Clock and Data Timing

Reading Data on the Diskette

The logic for reading data from the diskette is: a clock selector, a "state machine" data separator, and internal logic in the floppy controller.

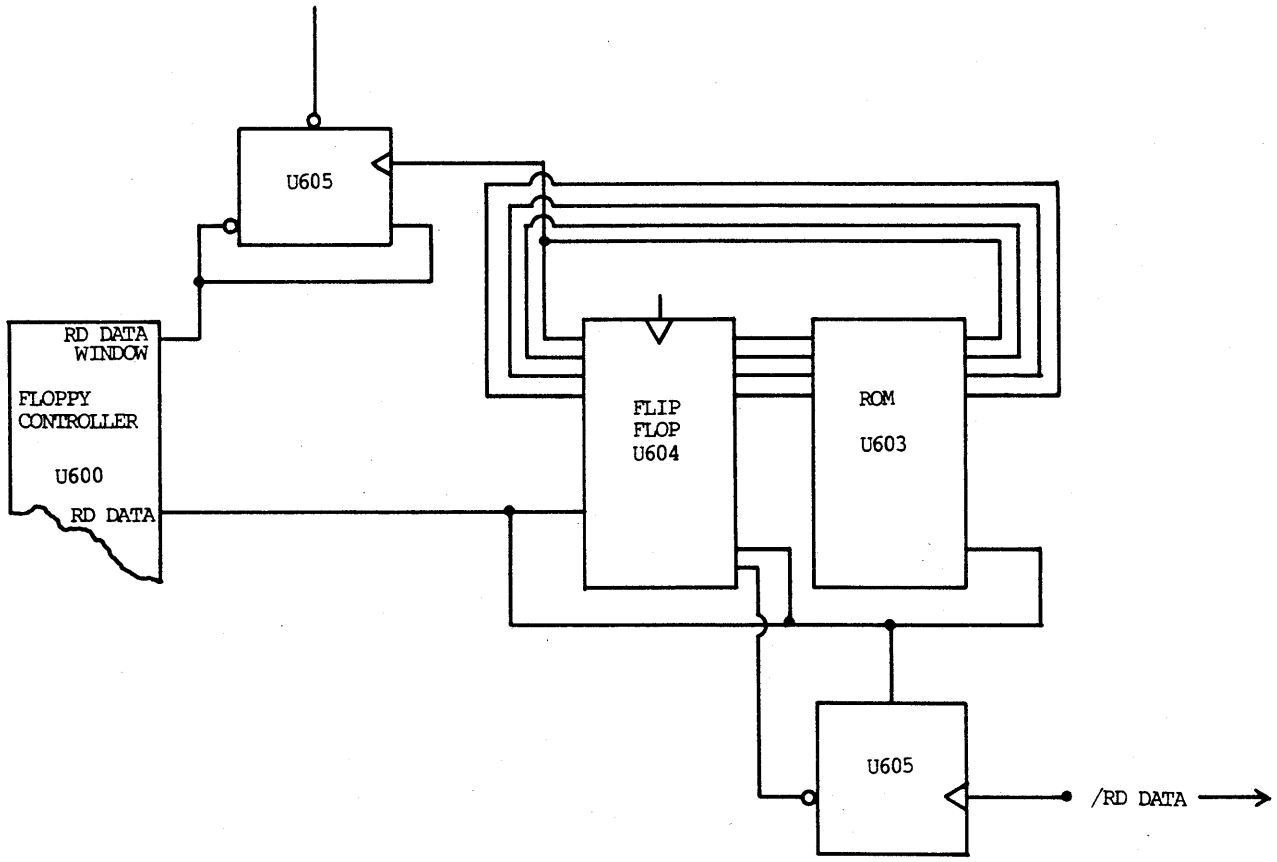


Illustration 2-22 Data Separator

The data on the disk is written with the clock pulses and the data combined. In order to read the data correctly, then, it is necessary to separate the data from the clock. The data separator takes the data coming from the diskette, and separates this signal into Read Data, and Read Window. These are the two signals required for the separation of data from clock to be implemented in the controller chip. The data is actually separated from the clock inside the floppy controller.

In order for the controller to be able to properly discern the data from the clock, it is necessary for the read logic to reconstruct the clock. This is necessary because the speed of the motor may differ from the time the data was written to the time that it is now being read.

The regeneration of the clock is accomplished by a state machine. A state machine is composed of a clock selector, a ROM, and a register functioning together as a counter.

The clock runs at sixteen times the write clock frequency. The state machine is designed to generate one read window per sixteen input clock pulses. The logic adjusts the generation of this window such that the data pulse is centered in the window.

The ROM contains 32 addresses. Sixteen of the addresses are "free run" addresses used when no read data is detected. The read window generation is not adjusted in free run. When read data is detected, the state machine uses the remaining sixteen addresses to center the read window around the data pulse.

The data pulse occurs during one of the sixteen clock pulses. Each pulse references one of the addresses in the ROM. Each address manipulates the read window generation according to the location of its corresponding clock pulse. For example, to center the data pulse in the window, the data must occur on the ninth clock pulse of the window. If the data pulse is detected on the eleventh pulse, the corresponding eleventh address causes the read window to advance by two counts.

The resulting signals back to the controller are read data, which is the data pulses, and read data window, which is the regenerated clock pulses.

Diskette Format

The diskettes Attache use have forty-six tracks on the top side and fifty tracks on the bottom side, with ten sectors per track, 512 bytes (one-half K) per sector. Each diskette has an index hole. A photo-electric sensor in the diskette drive senses this hole to use as a reference for the start of each track.

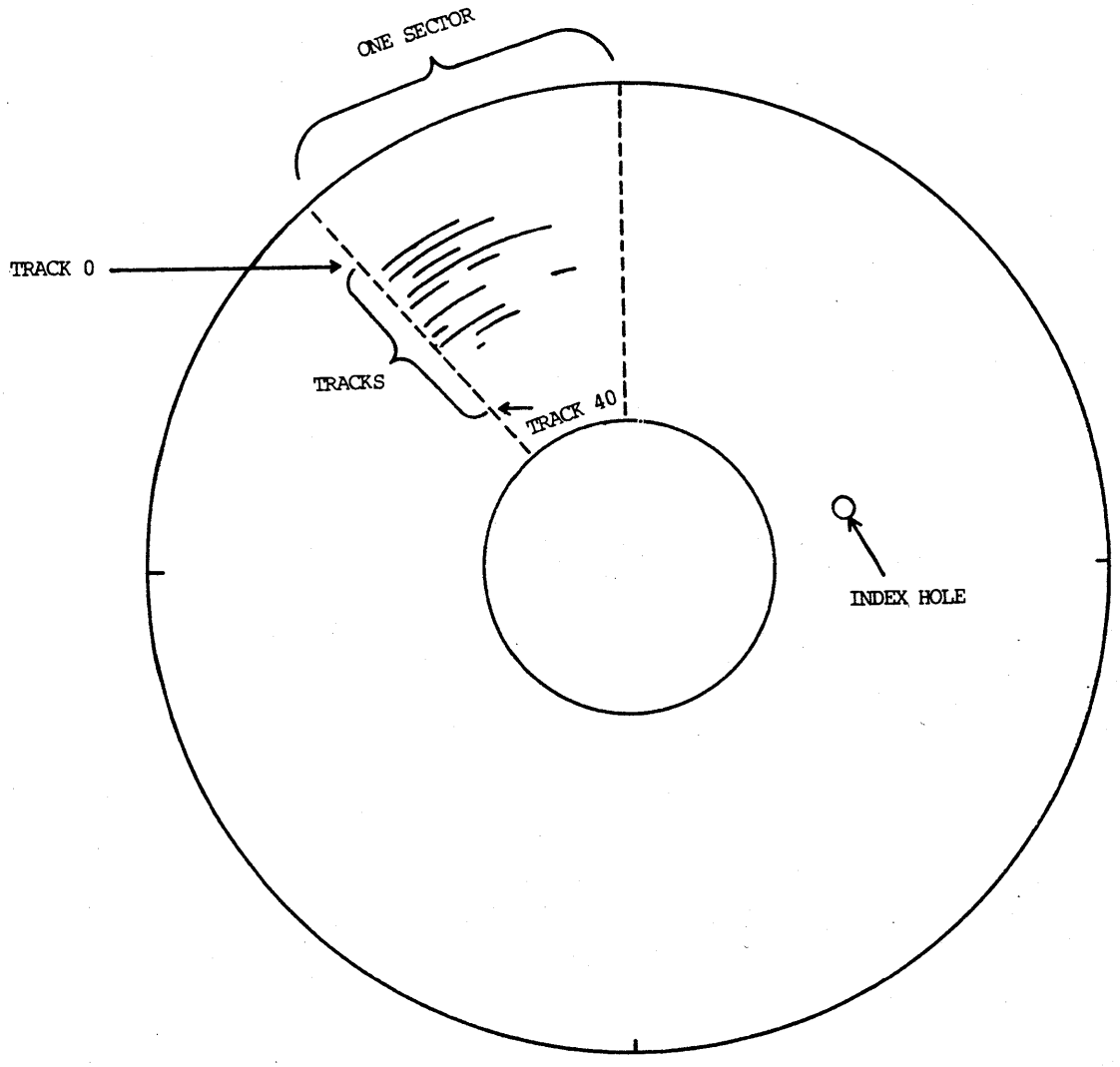


Illustration 2-23 Diskette Format

Diskette Track Format

Attache senses the index pulses, steps the head until signal Track 0 is true, and writes the diskette format for every track between each pair of index pulses.

Address marks are written to divide each sector. There are two address marks per sector, the first notes the start of the sector address, the second to mark the start of data.

Two cyclic redundancy codes (CRCs) are written as checks to ensure the data written was identical when read back. The code is generated when the information is written, and computed again when it is read.

Gaps are written to allow the drive time to switch the head's function between the read and write operations it performs. During a write to the diskette, the head must read first to locate the correct sector. The head waits for the gap, then turns on the write head.

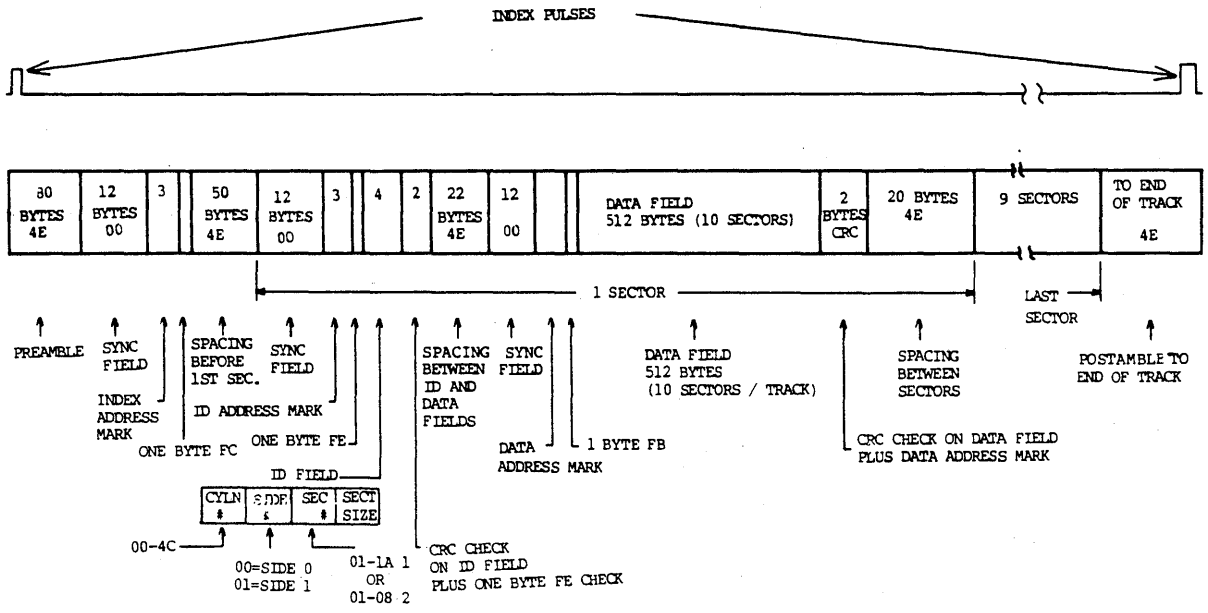


Illustration 2-24 Diskette Track Format

Graphics

The graphics section of the processor board contains five Random Access Memory (RAM) chips, a storage selector multiplexer, a buffer, and a shift register.

Data to be read or written to graphics goes into a buffer (U701). Each RAM chip stores the information for each graphic segment to compose one character cell. A multiplexer (U702) performs the necessary signal combinations and timing operations to select the proper graphic RAM location. The data is then shifted into an eight bit shift register (U703), where it is serially output to the video controls.

Graphics is discussed more extensively in the display section of this chapter, page 2-41.

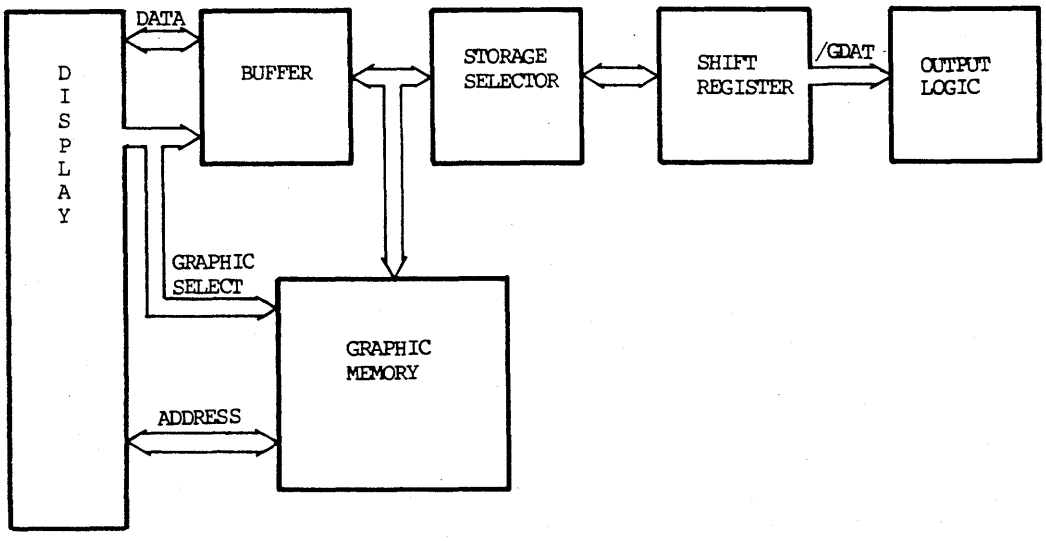


Illustration 2-25 Graphic Block Diagram

Power Supply

The Attache power supply is comprised of a main board and a high voltage board. Illustration 2-26, the Power Supply Block Diagram, outlines the major components of these boards.

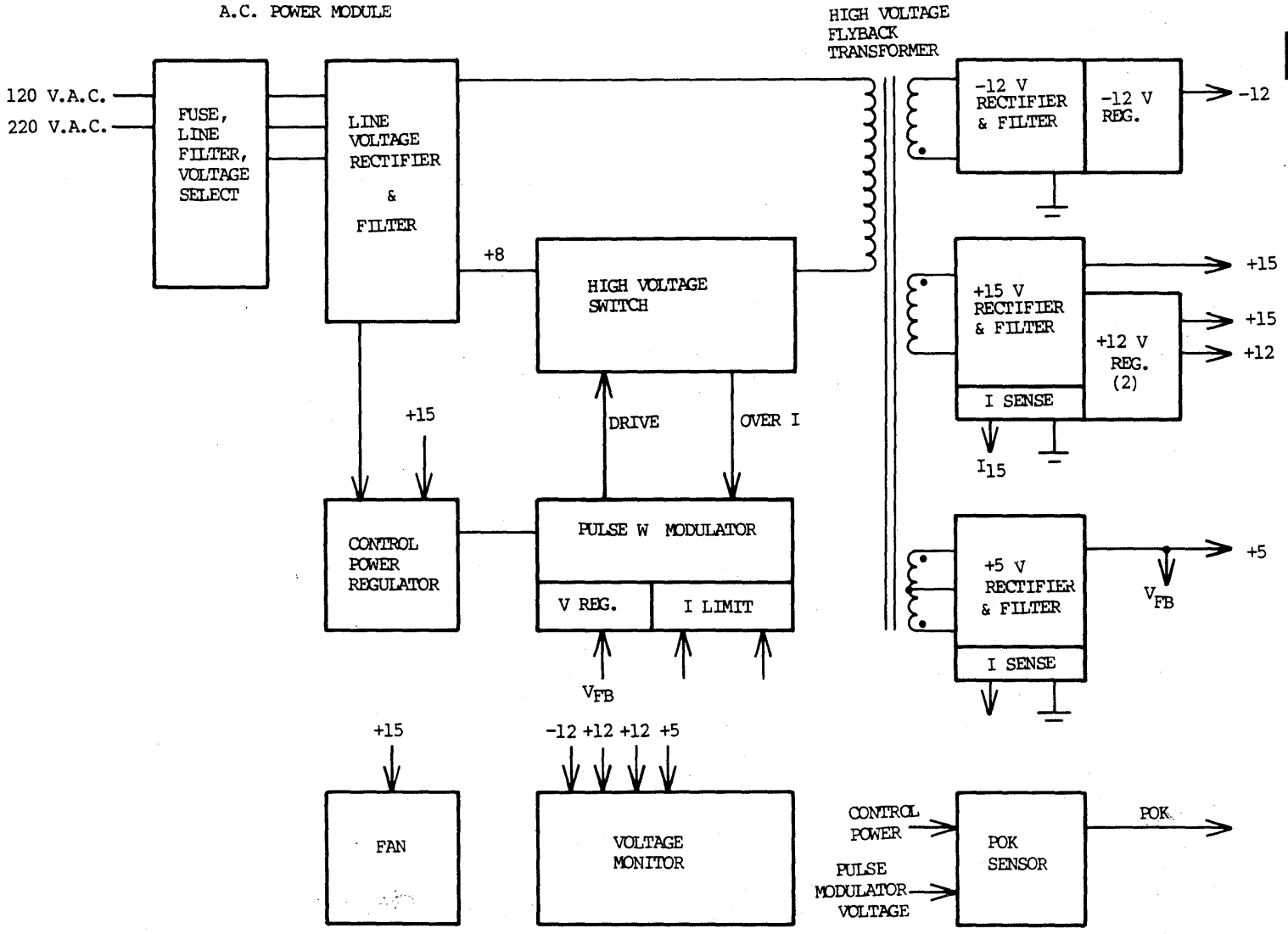


Illustration 2-26 Power Supply Block Diagram

Introduction

The Attache power supply uses a 23 KHz Flyback switcher. The supply provides high efficiency line voltage switching, allowing use of smaller, lighter components.

Attache accepts multiple line voltages and frequencies: 95 - 135 or 190 to 270 volts, 48 - 440 Hz. The supply processes the AC line voltage directly without transforming the input to a lower voltage and produces multiple output voltages: +5, +12, -5, and -12 volts, with 80 watts of power.

The power supply provides a Power Okay (POK) signal to the processor to initialize the system only when power is properly stabilized.

AC Power Module

The AC Power Module consists of the power plug, the fuse, the voltage select, the DC option connector, and the line voltage rectifier and filter.

Four different types of power plugs can be used on Attache, according to the input voltage. These cords are shown in Illustration 2-27.

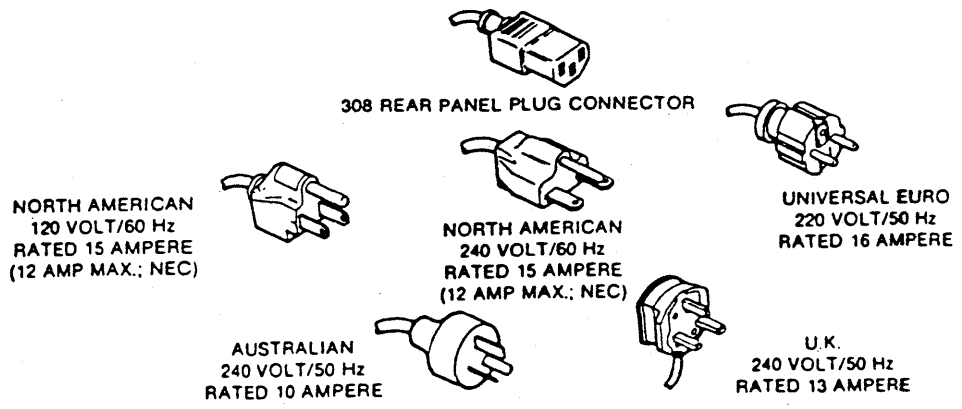


Illustration 2-27 Power Cords

Attache's fuse is a Slo-Blo 2 amp., 115 volt fuse, or a Slo-Blo 1 amp. 230 volt fuse, depending on the AC input voltage.

The supplies' voltage select allows the system to accept inputs in 100, 120, 220, and 240 volt ranges. A removable printed circuit board at the base of the fuse box may be rotated to select Attache's voltage according to the input voltage.

Voltage is factory set at 120 VAC. To change this setting:

1. Disconnect the power cord and remove the fuse.
2. Remove the P.C. board at the base of the fuse box. The side of the card facing you will read "120."
3. Turn the card so the required voltage setting (100, 120, 220, 240) is facing you.
4. Replace the P.C. Board and the fuse.

The card patches the power supply circuitry such that the line voltage rectifier operates differently according to the voltage selection.

The line voltage rectifier consists of the modular bridge rectifier D1, transient voltage protection V1 and V2, a surge protection resistor R7, and 1000 mf, 200 volt energy storage capacitors, C2 and C3.

For 220 and 240 volt operation, the bridge rectifier D1 is connected directly across the line, and supplies DC to the C2, C3 capacitors in series. The circuit acts as a full-wave rectifier. R4 and R5 are dropping resistors which distribute the voltage evenly to the capacitors.

At 100 to 130 volts, rectifier D1 functions as a voltage doubler. The center tap between the capacitors is attached to one side of the line, and only one section of the bridge is used to half-wave rectify the line voltage. The rectifier alternately stores energy in C2 and C3 at opposite cycles of the AC input, which results in twice the voltage potential across the capacitors as in full-wave operation.

The filter in the AC module provides noise elimination to meet commercial RFI specifications. The filter is composed of an RF isolation transformer and capacitors on both the line and neutral leads to ground at the power plug and lead side of the transformer.

Two series capacitors, C2 and C3, retain energy for over .25 seconds of operation to provide input voltage drop-off protection. An optional DC connection monitors the output of T1 for voltage drop off, and can automatically switch to the DC option in a power outage. (Battery pack and DC power options are discussed in the literature for those optional components.)

Power up switching is provided by triac Q1, controlled directly by the power on switch. Q1 can handle large surge currents and is used with R7 to sense the current limit when charging C2 and C3 during power up.

Control Power Regulator

The Attache power supply incorporates control circuitry. The control power regulator is a three terminal +8 volt regulator, U1. Control power is supplied to the Pulse Width Modulator circuitry, which generates the switching functions and monitors for over-voltage and over-current conditions.

The control power transformer, T1, initially generates 12 volts of DC to supply control voltage to the control power regulator. This voltage is regulated at +8 volts.

The regulator U1 is bootstrapped up by the 15 volt supply, and T1's output then is no longer used. This supply takes control of the regulator through D9 and reverse biases the bridge rectifier on the output of T1 at D3.

Pulse Width Modulator

The Pulse Width Modulator (PWM) varies the amount of energy stored in the flyback inductor on the High Voltage Driver board by varying the amount of time that the high voltage power switch (Q2) is on. This mechanism generates variable width drive pulses to the high voltage switch. The wider the pulse, the greater the current the flyback inductor establishes.

The major component of the PWM circuitry is U4, a TL494. The TL494 contains an on-chip 5 volt reference, an error amplifier, a current-limit amplifier, an oscillator, a dead time control comparator, and output control circuitry.

The PWM produces variable drive width pulses at 23 KHz and outputs these pulses to the high voltage switcher Q2 on the High Voltage Driver Board. This output is U4, pin 8 and connects to the High Voltage Driver Board through J7 via buffer transistor Q16.

The TL494 contains an internal +5 volt reference voltage. This voltage is used as the reference for the 5 volt regulator and to determine the current limits for the +5 volt supply. The reference voltage is also used in the under-voltage control lockout circuit, the dead time adjustment, and the POK circuit.

The voltage reference output appears on pin 14 and is divided by two by R55 and R58 to form the reference bias on -ER.

+ER and -ER (error) signals are voltage inputs to an internal operational amplifier used in the +5 voltage regulation loop. +ER is U4's sample of the +5 volt bus at pin 1. -ER is the inverting input on pin 2 from the compensating network R57 and C41 and the reference voltage divider.

The resulting control output voltage from the operational amplifier is pin 3. This compensating voltage feeds into the section of U4 which determines the pulse width (a comparator that compares voltage on pin 3 to a ramp from a sawtooth clock circuit). The clock is a 23 KHz sawtooth. The ramp of the sawtooth is compared to the control voltage output on pin 3. The higher the voltage on pin 3, the narrower the pulse that is sent to the high voltage switcher, and the less energy converted by the power supply.

PWM Dead Time

The pulse width must be limited to a maximum width. The time available to extract stored energy from transformer T3 is limited. If more energy is stored then there is time to extract, the sine of feedback loop changes and the circuit is forced into a lockup.

To avoid this lockup, a sensor is built into U4 which sets the maximum pulse width, called the Dead Time control. A voltage divider which contains R40, a screw driver adjustment, sets the dead time.

The resulting Dead Time Control Voltage is input to U4 pin 4, and is then fed to a comparator which forces the PWM to turn off at a predetermined ramp voltage of the clock. This forces the output pulse width to terminate at the maximum width.

Over-Current and Soft Start

External circuitry shuts down the power supply by pulling the Pulse Width Modulator's control voltage up to the +5 volt reference level. The circuitry is the + 5 volt bus over-current sensing circuit, +15 volt bus over-current sensing circuit, consisting of two sections of U5 and transistors Q10, 11, 12, and 13, and a soft start circuit, C28, R31, R34, D11, D12, D13, and Q12.

This over- and under-voltage sensing circuitry monitors for low voltage conditions on the control power regulator output. The circuit compares the 8 volt control power bus with the +5 volt reference and requires that the 8 volt bus be at least 3 diode drops above the 5 volt reference, 7.1 volts minimum, before the PWM is allowed to become active.

Q12 is a shunt to the soft start capacitor. When the control voltage is high enough, the shunt is released across the soft start capacitor, C28, and its voltage slowly builds up to soft start the supply.

The +5 volt bus and +15 volt bus have over-current protection circuitry. Operational amplifiers monitor the voltage across shunt resistors on the return lines of each of these supplies. If the shunt voltage exceeds a given threshold, the circuitry abruptly shuts down the PWM and requires a soft start. This serves as protection in case of a short circuit.

Additional protection circuitry has been incorporated into the power supply. Q17 and Q18 form a flip-flop as part of a shut down to the high voltage board if an over-voltage in the +5 volt bus occurs or an over-current condition on the high voltage driver board occurs.

If the over-voltage condition occurs, zener diode D18 breaks down and produces a current through D17. This turns Q18 on, which turns off Q17 and removes the capability to drive the high voltage driver.

An over-current sensing circuit on the high voltage board senses when the switch transistor current is close to its current handling capabilities. The signal enters an optical isolator, and latches the Q17, Q18 flip-flop.

The flip-flop can only be reset by powering down and then powering back on the system.

High Voltage Driver Board

The power supplies' basic power switch is Q2. The collector circuit of Q2 connects to the flyback transformer T3 and performs the actual power switching.

The base drive waveform on Q2 is critical to its high voltage operation, as the device has to be switched off quickly. A negative base drive current shuts Q2 off rapidly, which is provided by Q1 switching the negative voltage stored on C1.

Q16 drives 1:1 isolation transformer T1 on the high voltage driver board with a 6 volt pulse. The secondary 6 volt pulse is referenced to a floating bus, formed by the intersection of R1, R2, R3, D2, and D3. The Q2 base current during positive drive is determined by R3, the return resistor to Q2's emitter.

The voltage drop across R3 also provides the voltage to charge C1. The pulse charges C1 through D2 resulting in negative voltage on the emitter of Q1. After Q2's positive drive pulse from T1 terminates, Q1 is driven on, which forces a reverse current through the base of Q2, forcing it off faster.

A snubber is formed by D4, R6, and C3 across the high voltage output leads to the flyback. This snubber prevents the voltage from going so high as to destroy transistor Q2.

The snubber limits the rise time of the voltage on the collector of Q2. This, along with reverse base drive, allows Q2 to be operated at a safe level. R5 is a current shunt to sense the switching currents on Q2. If excessive, R5 forward biases the LED optical isolator D1 and triggers the Q17 and Q18 shutdown circuit.

Flyback Transformer

The transformer is a gapped pot core with a bobbin. The primary circuit has two windings. One is driven by Q2, and the other is an over-voltage clamp winding used to ensure that the flyback voltage does not exceed twice the raw DC voltage output from the storage energy capacitors.

There are four secondary windings. One winding is used for the -12 volt supply. One is used for the +15 volt supply. Two windings are used for the +5 volt supply. This shares current through the windings and rectifier diodes to keep the current within the diode's current limits, and reduces the losses in the +5 volt transformer windings.

When Q2 turns on, energy builds up in the transformer's magnetic field due to the current in the primary windings. At the end of the PWM drive pulse, the power switch transistor turns off and the stored energy induces an opposite polarity voltage in the secondary windings.

This voltage is rectified and stored in filter capacitors. C18 stores voltage for the -12 volt supply, C19 and C23 for the +5, C20 and C21 for the +15 supply.

Output Supply Rectifiers and Filters

The +5 volt C19 and 23 are the main storage capacitors for the 5 volt winding's pulsed current input. This pulsed current causes some voltage ripple which necessitates additional filtering. The filter is the L3 inductor and C24, 25, and 29. L3 is effective at high frequencies.

The use of several capacitors distributes the noise currents, and reduces the lead inductance effects. Additionally, the capacitors have different frequency responses, thereby improving noise elimination.

R30 is a current sensing resistor for the over-current feedback sensing of the 5 volt supply.

The only supply which is directly regulated is the +5 supply. The others are tracking supplies. Variations due to leakage and IR voltage drops are controlled by three regulators, U2 for -12 volts, U7 and U3 for the +12 volt supplies.

The +15 volt supply uses C20 and 21 as energy storage capacitors. L4, C22 and 35 are the noise filter. R28 is the shunt resistor.

Post regulators U3 and U7 regulate +15 volts down to the +12 voltage for the processor board and disk drives use. U3 is a three terminal variable voltage regulator. U3 requires R36 and R35 to set its operating point, and uses C26 as a stability capacitor on its output. C26 reduces the possibility of regulator oscillation due to load variation and lead inductance.

The -12 volt supply is a three terminal regulator supply. D5 is its rectifier, C18 is its storage capacitor, L2 and C17 the filter. The regulator has an inherent current limiter. C38 is a stabilizing output capacitor.

Power Okay (POK) Sensor

The POK sensor generates a reset signal to the computer when the power supply is not operating properly. The sensor ensures that the voltage of the +5 bus is within tolerance, and the pulse width from the Pulse Width Monitor is not approaching the dead time limit.

R41 in the voltage divider supplying U4 pin 4 is the trip level adjust for POK. The POK circuitry senses when the PWM pulse width is getting close to the dead time limit and shuts off POK before the pulse reaches maximum.

U5 pins 2 and 3 compare the control voltage on U4 pin 3 with potentiometer R41's wiper voltage. If the dead time is close to maximum, U5, pin 1 output is high. If the PWM pulse width is within tolerance, pin 1 output is low.

The +5 volt sensor, Q14 and Q15, compare the +5 bus with the +5 volt reference. The bus must be above 4.4 volts to issue the POK signal. If the voltage is below 4.4 volts, Q15 turns on.

Either of the two erroneous conditions turns Q20 on: U5 pin 1 high from dead time at maximum, or Q15 on from the +5 volt bus less than 4.4 volts. This shunts the voltage on timing capacitor C49 to ground. The POK signal is consequentially not issued.

If the pulse width and the +5 volts are within tolerance, Q20 turns off, allowing C49 to charge up from current through R67. U5's output consequentially switches low when C49's voltage exceeds +5R. Q19 then pulls the POK signal high and allows the processor to start up.

Once the power supply is within tolerance, the C49 and R67 circuit causes a one second delay before POK is output to the processor.

Voltage Monitor

The voltage monitor lights a green LED, which is a service aid that indicates the voltage outputs are within tolerance.

The monitor samples the four output voltages with a resistor network and U6. The circuitry contains summing resistors and three comparators. The sum of the output voltages must fall within a narrow range of voltages for the LED to light.

Fan Driver

The supply uses a DC brushless, three-phase motor fan. A ring oscillator steps the motor from one phase to the other, driving the fan.

A thermistor control senses the heat output from the power supply. The hotter the supply becomes, the faster the fan runs.

Connectors

J1 is a triac power switch connector, which interacts with J2, the line voltage input. J3 is the connector between the main power supply board and the high voltage driver board. J7 is the high voltage driver board connector and over-current sensing feedback.

J4 is the DC option connector, which provides the battery powering capabilities to Attache, when AC line power is not be available.

The remaining connectors attach to the Attache modules. J5 is the video monitor power and drive. J6 provides power to the disk drives. J8 connects the supply to the processor board power and the speaker.

Keyboard

The keyboard is an Attache module that interfaces with the processor board through a four-wire connector (J1). The major components of the keyboard module are the keyboard itself, a counter, a shift register, and an oscillator.

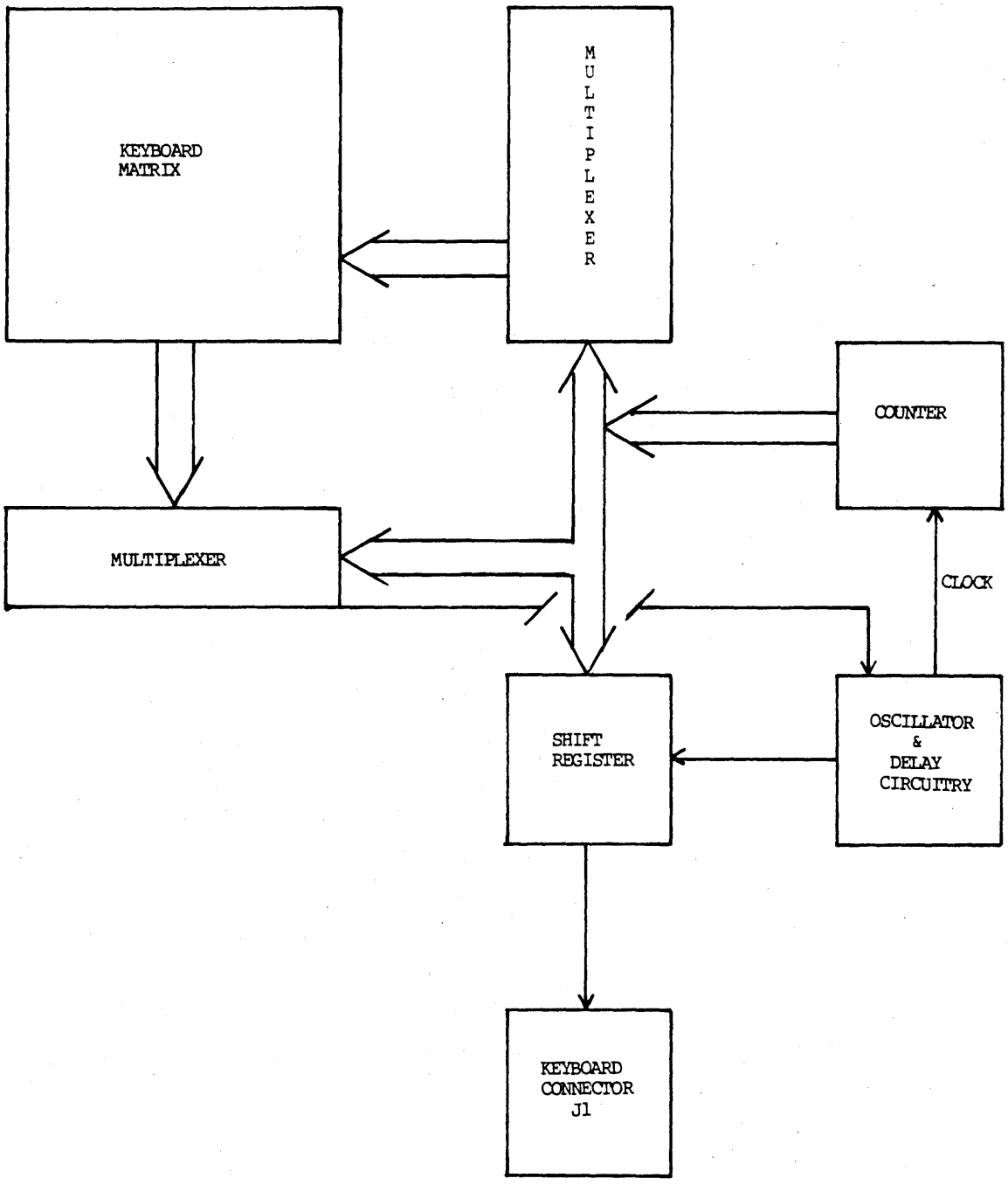


Illustration 2-28 Keyboard Block Diagram

Introduction

The keyboard is set up in a grid pattern. Two multiplexers are attached to the keyboard grid lines. The multiplexers receives a binary counter's output which sequentially enables each grid line.

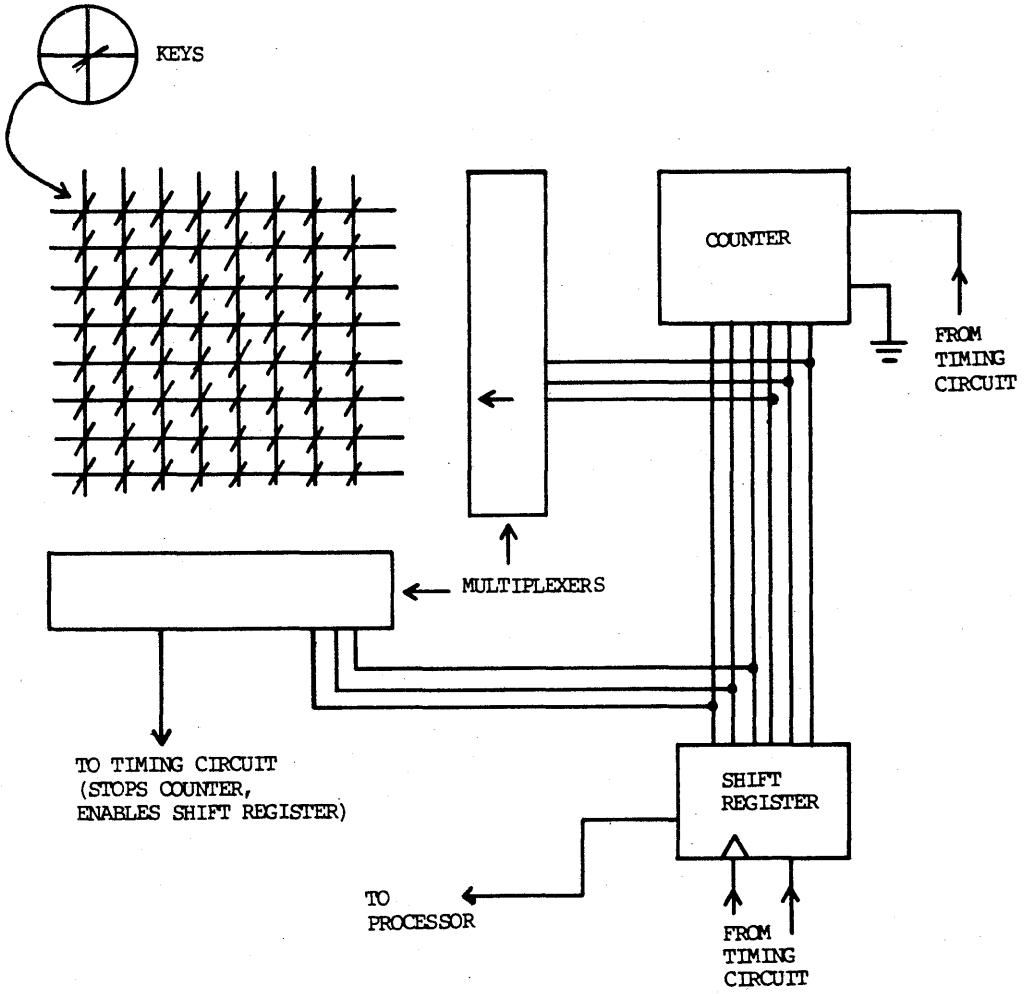


Illustration 2-29 Keyboard Grid

A pressed key creates a short to output a high signal that stops the counter and enables a shift register. The character code from the corresponding key loads into this register in parallel. System clock pulses shift the data bits of the keycode out serially to the processor, via the Parallel Input/Output controller (PIO).

Basic Keyboard Logic

The NAND gate U5, combined with the resistor - capacitor components R9, R10, and C9, form a 4 KHz oscillator. The oscillator drives a binary counter U8, and flip-flop U3, at 4 KHz.

The counter inputs high pulses to two 8-channel analog multiplexer / demultiplexer. The multiplexers contain 8 bidirectional analog switches and connect to sides of the keyboard grid. The counter's pulses sequentially enable each of the switches, which connect to a grid line and to pin 3.

When a key is pressed a short is created between the multiplexers which outputs the high enable from the counter through the corresponding grid lines, to U9 pin 3.

This signal is gated into the flip-flop U3 (pin 6) by an oscillator clock pulse. The signal is inverted at U3 pin 2, so NOR gate U4 receives a low signal.

This low signal couples an oscillator clock pulse into the flip-flop, U6. The flip-flop (U6) is now set, indicating a key is down. This drives the load input (pin 9) of the shift register (U7) high which loads the key code from counter (U8).

U7 is a parallel-to-serial register. Pin 9 high latches parallel input; pin 9 low enables serial output. Each pressed key causes six data bits of keycode data to be loaded into the shift register (U7). Two more bits are added: one bit represents the status of the shift key, and the other represents the status of the control key.

U6 sends a signal to pin 2 of a NAND gate (U5) simultaneously with its load signal to U7. This pulls connector J1 pin 4 to the PIO low, which signals the processor via the PIO that a key has been pressed.

The processor sends system clock pulses through connector J1 pin 3 to U7 pin 10, and simultaneously sends reset pulses to U6. Reset sets the U7 shift register's parallel load pin 9 low, enabling serial output. The data bits are clocked out U7 pin 3, through J1 pin 4 to the processor via the PIO.

Additional Circuitry Functions

A feedback loop (U3 pin 2 to U4 pin 2), and a delay (C5 and R6) keep the state of U3 from changing too rapidly. This is an allowance for key bounce.

Key repeat is a function of the counter, U2. U2 starts counting when a key is pressed. After a short period of time (set by the potentiometer at the back of the keyboard) U2 drives its output high. The next clock pulse enables the flip-flop (U6). U3 pin 14 goes low, which gates the output of U2 pin 13 through gate U4. This generates a string of pulses. Each pulse sets U6, sending the key code held down to the processor.

The line from the shift key goes through a diode. The diode prevents using the left Shift key and the Reset key to cause a system reset. (An accidental system reset from pressing both keys would otherwise be easy.)

---- POSITION OF PHYSICAL KEYS IN KEYBOARD MATRIX --
(UN-SHIFTED)

	0	1	2	3	4	5	6	7
0	BS	TAB	LF	XXXXX	XXXXX	CR	XXXXX	LOCK
1	SPACE	XXXXX	XXXXX	ESC	LEFT	RIGHT	UP	DOWN
2	0	1	2	3	4	5	6	7
3	8	9	'	;	,	=	.	/
4	`	a	b	c	d	e	f	g
5	h	i	j	k	l	m	n	o
6	p	q	r	s	t	u	v	w
7	x	y	Z	[	\	]	-	DEL

Illustration 2-30 Keyboard Layout

Additional information on keyboard layout is contained in the Software chapter of this manual. Refer to "Generating Keyboard Codes", page 3-53.

ASCII Character Codes

ASCII Code (decimal)	(hex)	ASCII Char.	ASCII Code (decimal)	(hex)	ASCII Char.	ASCII Code (decimal)	(hex)	ASCII Char.
000	00	NUL	043	2B	+	086	56	V
001	01	SOH	044	2C	,	087	57	W
002	02	STX	045	2D	-	088	58	X
003	03	ETX	046	2E	.	089	59	Y
004	04	EOT	047	2F	/	090	5A	Z
005	05	ENQ	048	30	0	091	5B	[
006	06	ACK	049	31	1	092	5C	\
007	07	BEL	050	32	2	093	5D	]
008	08	BS	051	33	3	094	5E	^
009	09	HT	052	34	4	095	5F	_
010	0A	LF	053	35	5	096	60	`
011	0B	VT	054	36	6	097	61	a
012	0C	FF	055	37	7	098	62	b
013	0D	CR	056	38	8	099	63	c
014	0E	SO	057	39	9	100	64	d
015	0F	SI	058	3A	:	101	65	e
016	10	DLE	059	3B	;	102	66	f
017	11	DC1	060	3C	<	103	67	g
018	12	DC2	061	3D	=	104	68	h
019	13	DC3	062	3E	>	105	69	i
020	14	DC4	063	3F	?	106	6A	j
021	15	NAK	064	40	@	107	6B	k
022	16	SYN	065	41	A	108	6C	l
023	17	ETB	066	42	B	109	6D	m
024	18	CAN	067	43	C	110	6E	n
025	19	EM	068	44	D	111	6F	o
026	1A	SUB	069	45	E	112	70	p
027	1B	ESCAPE	070	46	F	113	71	q
028	1C	FS	071	47	G	114	72	r
029	1D	GS	072	48	H	115	73	s
030	1E	RS	073	49	I	116	74	t
031	1F	US	074	4A	J	117	75	u
032	20	SPACE	075	4B	K	118	76	v
033	21	!	076	4C	L	119	77	w
034	22	"	077	4D	M	120	78	x
035	23	#	078	4E	N	121	79	y
036	24	$	079	4F	O	122	7A	z
037	25	%	080	50	P	123	7B	{
038	26	&	081	51	Q	124	7C	|
039	27	'	082	52	R	125	7D	}
040	28	(	083	53	S	126	7E	~
041	29	)	084	54	T	127	7F	DEL
042	2A	*	085	55	U			

Illustration 2-31 ASCII Chart

Display Module

The display module consists of the Cathode Ray Tube (CRT) and the logic circuitry necessary to drive the CRT; ie. the vertical circuits, the horizontal circuits, and the video circuits.

An electron beam within the CRT moves across the screen in a sawtooth waveform from the screens upper left corner to the lower right. The beam charges the particles of the screen's phosphorous background. Horizontal and vertical deflection coils in the display module control the beam's scanning movement.

Power for the module is supplied from connector J2, pin 3. A 708 12 volt regulator generates the +12 volt output necessary to drive the display. Resistors are strapped across the regulator to move some of the power load from the regulator on to the resistors.

The frequencies required by the display are produced by two oscillators: one vertical axis and one horizontal axis. The horizontal oscillator runs at 15.75 KHz. The vertical runs at 60 Hz.

Synchronization for the oscillators is provided by vertical and horizontal sync signals from the CRT controller in the display section of the processor board. A third signal, video, which determines the voltage output of the electron beam, is also input from the display section.

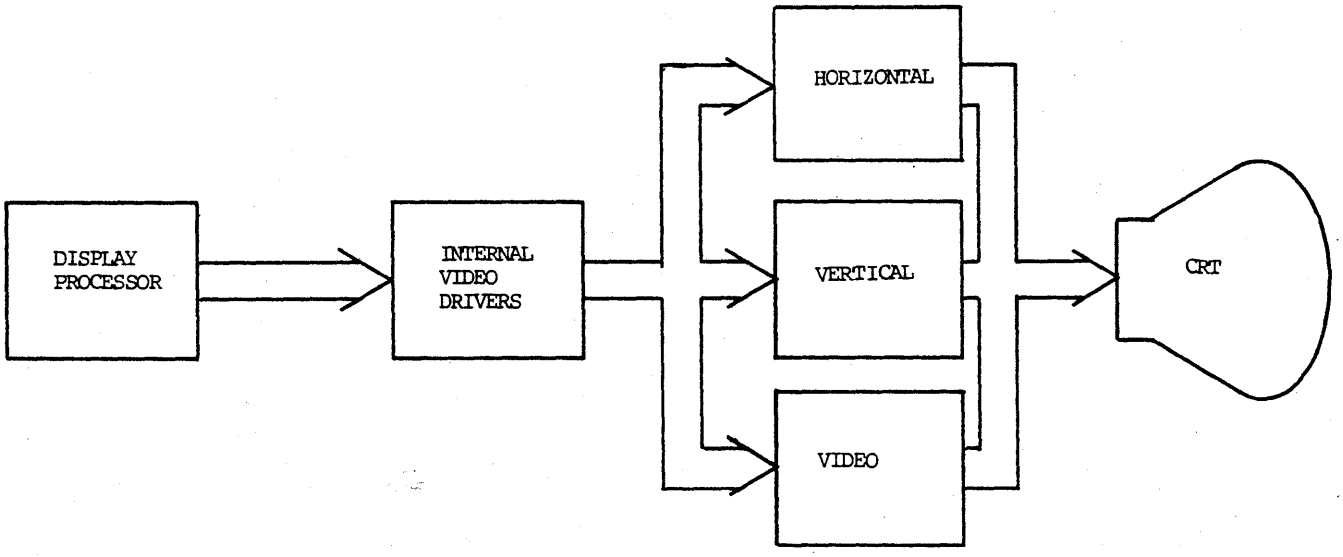


Illustration 2-32 Display Module Block Diagram

Horizontal

The horizontal circuitry consists of the horizontal oscillator, the high voltage generator, the horizontal yoke drive, the constant cut-off control, brightness control, and focus control.

The horizontal oscillator provides a continuous stream of synchronized timing pulses. The high voltage generator provides the second anode voltage for the electron beam. The horizontal yoke drive controls the horizontal deflection of the electron beam. Constant cut-off control keeps uniform brightness and size across the screen.

The display requires 10K volts, as well as several other voltages for focusing and brightness control. The horizontal circuits use a flyback transformer to produce this high voltage.

The horizontal sync signal from the processor board is input from J2 connector pin 5, and is sent to transistor 2sc1213. This signal drives the flyback transformer to drive the transistor which handles the bulk of the current, 2sc2373. When this signal turns on, the transistor turns on and drives the flyback transformer, charging it to +12 volts across winding pin 1 to 4. When horizontal sync turns off, the charged voltage is released, which generates the output voltage of 400 volts.

Voltage dividers are used to derive the proper voltages for focus and brightness control. A regulator circuit turns off the drive voltage in the event no horizontal sync input has been received. This protects the transistors in the logic.

The deflection yoke consists of interleaved coils of wire. They are wrapped around the CRT at the start of the tube funnel. The horizontal yoke produces horizontal beam motion from a sawtooth current input.

The deflection yoke current increases as +12 volts is input across its coil. A much higher voltage is required to discharge this voltage, which the high voltage flyback transformer generates. When the driving voltage is shut off, the flyback swings to high voltage to discharge the current in the yoke. A fast retrace for the short end of the sawtooth results.

A CRT does not maintain focus or brightness evenly across its screen. Constant cut-off control compensates for this. The cut-off circuit consists of the diode - capacitor - resistor network on pin 8 of the flyback transformer. The circuit modulates the brightness voltage according to the beam's screen location.

Vertical

Vertical circuitry in the display modules consists of a vertical oscillator and a vertical yoke driver. The oscillator provides a continuous stream of synchronized timing pulses. The vertical yoke drive controls the vertical deflection of the electron beam.

The vertical motion of the electron beam is derived from vertical deflection coils when a sawtooth ramp of current is applied to the vertical windings.

An integrated circuit chip generates a sawtooth wave at a 60 Hz frequency. This sawtooth must be generated with no DC component in the deflection yoke to magnetically attract the beam towards the components. The yoke is therefore AC coupled with two 1000 mf. capacitors.

The height adjustment adjusts the gain of the sawtooth ramp. Linearity control makes the ramp non-linear to compensate for the non-linearity of the yoke.

Video

The video circuit consists of the circuitry necessary to provide video buffering, video amplification, and video power drive.

The system's input to the video circuits is the alphanumeric or graphic data signal to be written on the screen. This signal is buffered, and then amplified.

A cascade amplifier increases the signal voltage to the level the cathode of the CRT requires. A peaking coil is used to counter-act the capacitance of the tube.

The electron beam is intensity modulated to write the data to the screen in the proper locations.

CRT

The CRT consists of a heater, a cathode, grid 1 - 5 voltage, an anode funnel, and the face plate.

The heater heats the cathode to boil off the electrons which form the beam. The cathode's potential is affected by the video frequency, which produces the modulated electron beam flow and writes on the screen.

Voltage potential generates from different grid voltages to form beam control voltages. Grid 1 voltage sets the beam brightness. Grid 2 voltage, the screen grid, accelerates the beam and sets its spot size. Grid 4 voltage focuses the beam.

The second anode funnel contains a high voltage surface for beam acceleration. Two conductive surfaces at different potentials are separated by glass to form a large capacitor. Grid 3 and 5 voltages, at second anode voltage, provide this further acceleration.

The face plate is the surface the beam strikes. The surface is coated with a phosphorous material which glows when hit by the electron beam.

Diskette Drive

This is a general discussion of diskette drive logic. Attache uses one of two types of diskette drives. If the Attache diskette handle pivots open or shut, as in Illustration 2-33a, refer to schematic page A-11a.

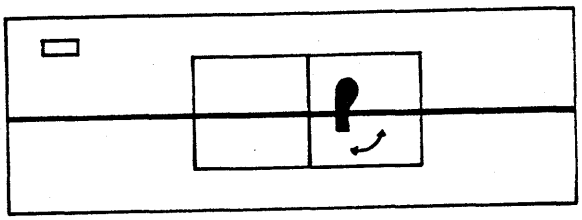


Illustration 2-33a Drive Handle

If the diskette drive handle presses open or shut, as in Illustration 2-33b, refer to schematic page A-12a.

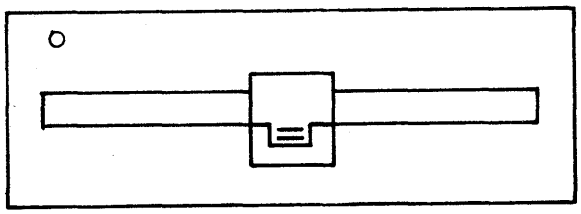


Illustration 2-33b Drive Handle

The drives use 5 1/4" diskettes with 48 tracks per inch. The diskette format is described in Illustrations 2-23 and 2-24, pages 2-54 and 2-55.

The diskette drive logic is located on two different boards. The main board contains the channel which controls the read and write, the head stepper motor driver, and sensors. The second board controls the spindle; (ie. the mechanism which turns the diskette).

The diskette drive circuits are composed of logic for moving the diskette head, for writing, reading, and driving the diskette drive's motor.

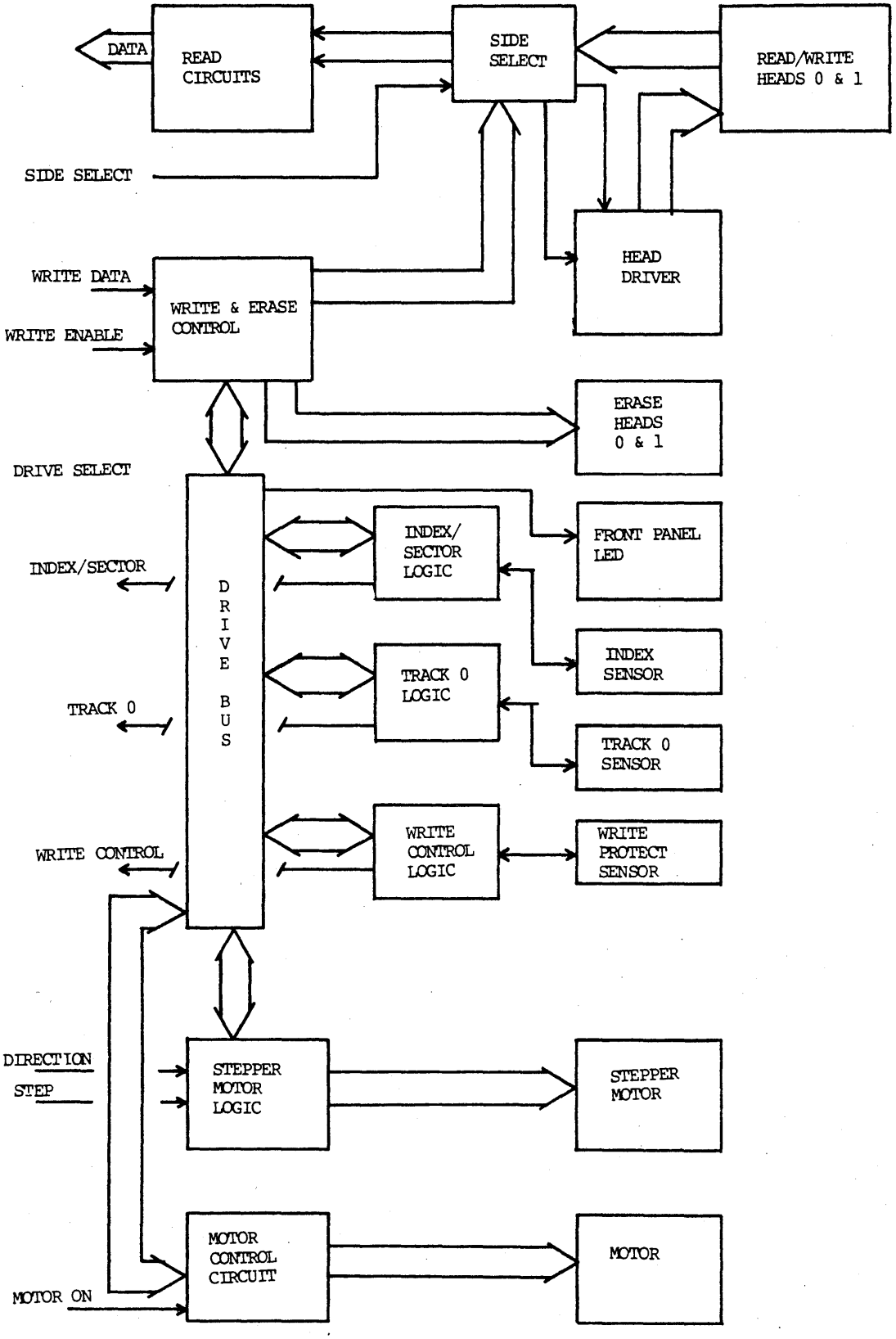


Illustration 2-34 Diskette Drive Block Diagram

Head Movement

The logic control for moving the head is located on the main board. The main board has two connectors; one sends and receives signals to or from the floppy control on the processor board; the other four pin connector receives voltage for the drive: +5 volts, +12 volts, and their respective returns.

Three drive select lines can be patched to the drive select line. A Head Select signal is used from the drive for selecting the head. Write gate and Write Data are used to control writing to the diskette. The signals are buffered and inverted. Direction and Step control the head movement.

Two flip-flops act as a counter and use input signals Direction and Step to drive the four states required for the four phases of the stepper motor.

The motor phases are on opposite sides of the flip-flops. An Exclusive OR gate serves to reverse the direction of the step. It changes the next state of the motor stepper corresponding to the direction the motor is moving.

Each stepper phase consists of driver circuits which drive two of the windings differentially. Each step moves the head one track.

Sensors

The three optical sensors on the drive send signals to the main board. These sensors are for the write protect notch, the track 0, and the index.

Write control, write protect, and index are gated directly to the floppy control logic. Track 0 is gated with two of the phase signals of the stepper motor, which improves the resolution of the Track 0 detector. If the motor is in proper phase and the track 0 detector is on, then the track 0 signal is passed back to the floppy control logic. Index and Write Protect is gated straight out. All of the signals are gated with drive select.

The front panel LED is tied directly to drive select. Motor on goes to the motor board and the spindle.

Writing

The signal, Write Gate, enables or disables writing to the drive. A low signal enables data to be written. A high signal enables data to be read.

Write data is input from the system in the form of write pulses. At each pulse, the direction of the head polarity is switched by driving the opposite side of a coil. The diskette media is thereby magnetized in opposite polarities at each pulse transition.

The head coil used for writing on diskettes consists of a coil with a grounded center tap. Incoming write data pulses cause a flip-flop to change states. The outputs of the flip-flop are gated with side select to select the proper head.

The coil windings are wound in opposite directions on either side of the center tap. The flip-flop's toggles cause write drivers to drive one side of the coil, or the other. Consequently, magnetic fields of opposite polarities are written to diskette.

Write amplifiers are supplied by a constant current source through a transistor's collector lead to the +12 volt supply. The current switches to one side or the other by the appropriate driver.

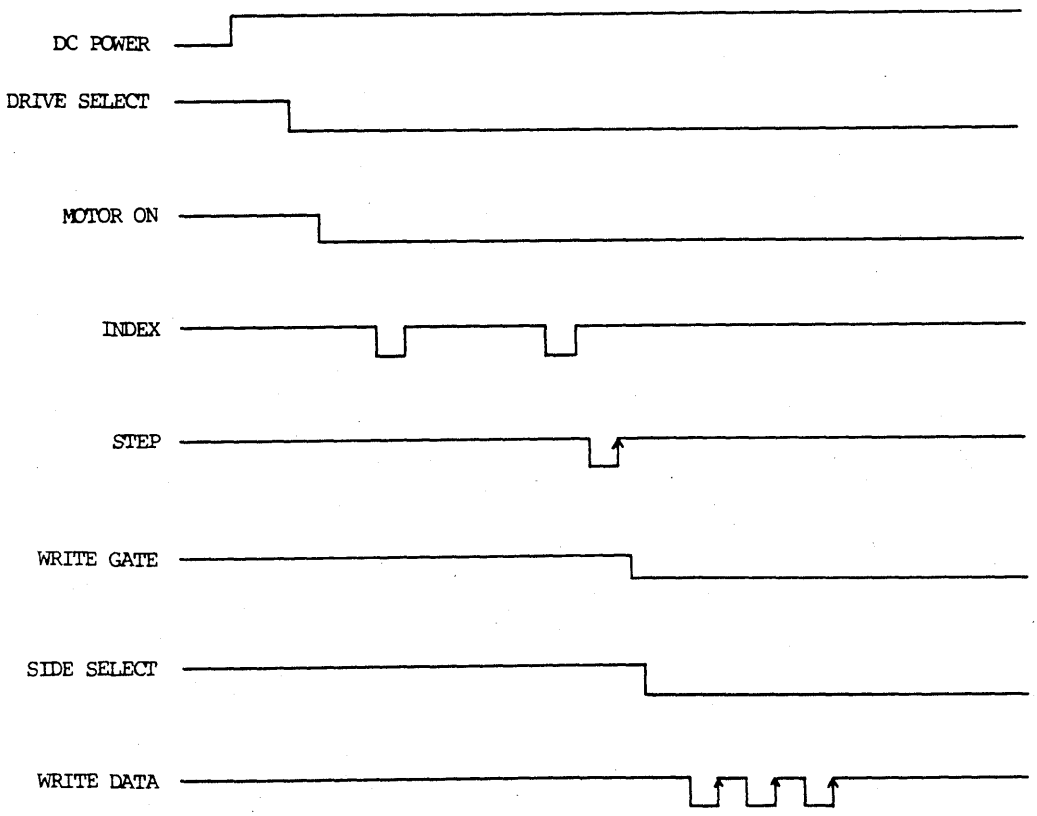


Illustration 2-35 Write Timing

A sensing circuit monitors the +5 volts to the drive. The circuit shuts off write current if the voltage drops below +3.9 volts. This protects against writing on disk while the system is powering up or down.

The drives use tunnel erase. Data is written to the disk in wide bands. Two erase sections of the head erase either side of the band to improve the density of data on the diskettes and eliminate excessive crosstalk between tracks.

The erase head is staggered behind the read/write portion of the head. The erase current is enabled shortly after write data is present. The first bit of write data triggers a signal which triggers a delay one-shot. The output of the one-shot triggers a second delay one-shot to the erase current.

The erase head continues its operation after the write current is shut off. The erase current is held on by the output of the first one-shot delay when no write data is present, shutting off with the one-shot.

A power on reset circuit erases a one shot when the drive is first powered on.

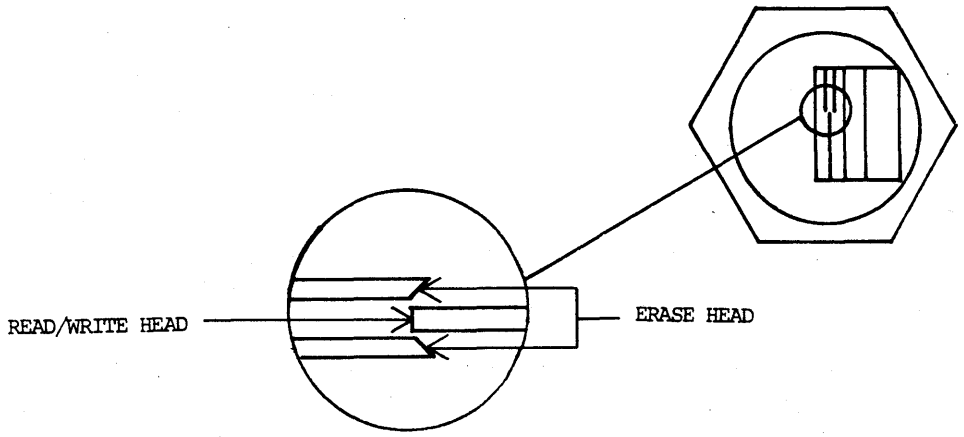


Illustration 2-36 Head Diagram

Reading

Data is returned to the logic from one of two heads during a read operation. A CMOS multiplexer switch selects which of the two heads is reading. Side select is enabled for the appropriate head output.

During a read operation, the heads develop a current induced by the magnetized diskette media. Flux transitions on the diskette create current pulses whose polarity is determined by the direction of flux lines. These pulses are amplified twice. A differentiator takes the derivative of these amplified pulses. A digitizer then interprets the zero crossings of the differentiated signal as high and low transitions.

The read control section of the diskette drive must take magnetic flux direction changes and interpret these changes as digital highs and lows. A MC3740 chip performs this function. The 3740 contains a preamp and filter, another amplifier and filter, a differentiator and a digitizer.

An amplifier amplifies the read signal. A preamp has a built-in, rudimentary low-pass filter. Following the preamp is another filter and AC coupling. A second amplifier enlarges the signal further. Balance control compensates for offsets between the two amplifier stages.

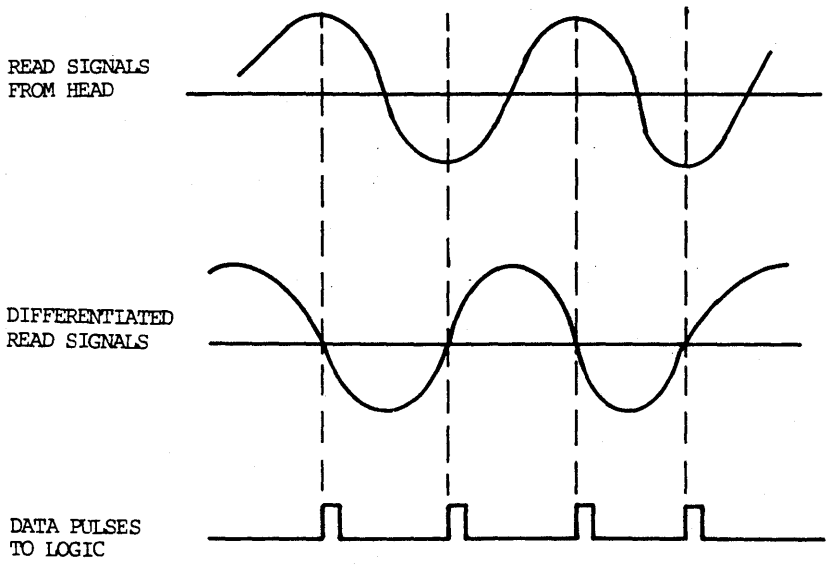


Illustration 2-37 Read Signals

Turning the Diskette

The diskette spindle is driven at 300 RPM by a direct drive, brushless, DC motor. The spindle motor driver is a closed - loop motor servo system. Tacometer pulses are generated from a tacometer in the motor. A reference signal is created by a resistor - capacitor network.

The constant stream of pulses from the reference signal is compared to the tacometer pulses. Unless the pulse trains are identical, an error signal is derived from the difference between the two signals and is input to the motor. The error signal acts to either increase or decrease the speed of the motor respectively.

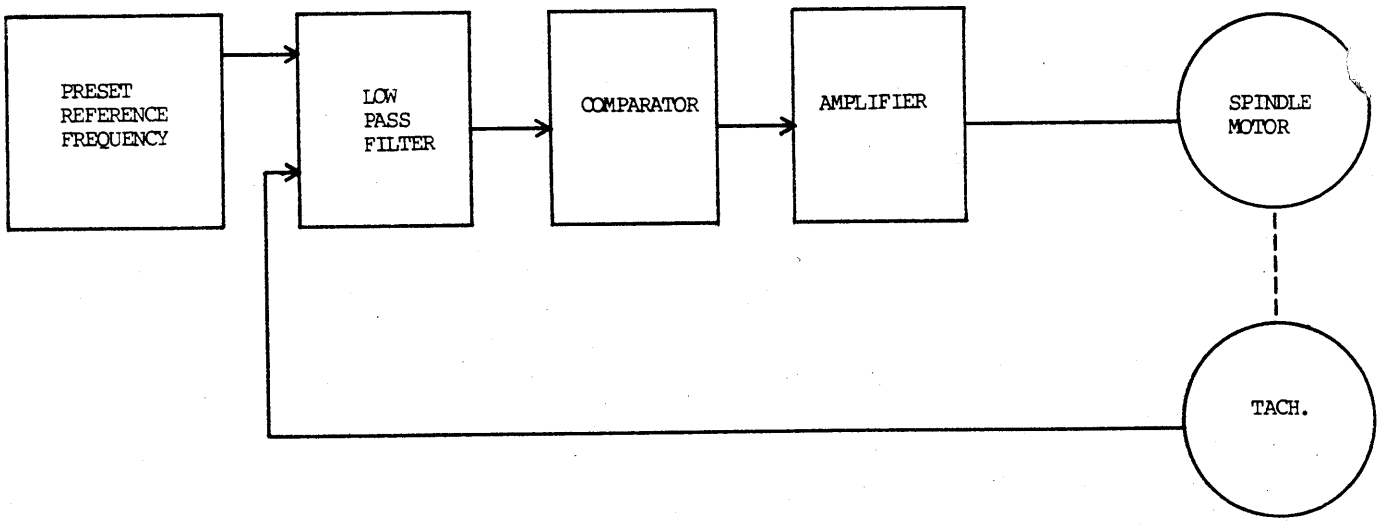


Illustration 2-38 Servo System

Software

Hardware

Theory of Operation

Software

Appendixes

CONTENTS

Software

The software section of this manual is intended for readers with programming knowledge who wish to learn about Attache's software or to make adaptations for specific applications.

Attache uses CP/M (Control Program for Microcomputers), a commonly used microcomputer operating system written by Digital Research. One section of CP/M, the BIOS (Basic Input/Output System), is written specifically for Attache, so the majority of this chapter concerns BIOS.

This chapter contains a general discussion of the routines which comprise the BIOS. These routines are divided into the following topics: Boot Loader, Disk Driver, I/O Drivers, Display Driver, the CMOS Random Access Memory (RAM) and Clock routines, the Interrupt Structure, and Valet routines.

Charts of commonly used programming functions are located in the appropriate section of the BIOS description. These are listed as illustrations on page viii for quick referencing.

Descriptions of memory locations and Read-Only Memory (ROM) software, such as Terminal Emulation, are also provided in this chapter.

An introduction to CP/M follows.

CP/M Introduction

Attache uses CP/M (Control Program for Microcomputers). CP/M is an operating system which allows software to interface with the hardware.

CP/M is divided into four parts: BIOS (Basic Input/Output System), BDOS (Basic Disk Operating System), CCP (Console Command Processor), and TPA (Transient Program Area).

BIOS is the hardware dependent section of CP/M. The BIOS is specifically tailored for Attache. It defines the hardware in which CP/M executes. The BIOS interfaces with the BDOS to execute program instructions at a physical level.

BDOS performs disk I/O and all of the logical level system I/O. BDOS defines four logical I/O devices: the List, the Console, the Punch, and the Reader. BDOS performs system reset, console I/O, reader input, punch output, list output, and logical disk read and write functions. BIOS then translates these logical device operations into physical device operations.

CCP provides the initial interface between the user and CP/M. CCP reads and interprets commands entered through the console (i.e. the display and keyboard) when the CP/M prompt "A>" or "B>" is displayed, or when a submit file is processing. CCP processes the initial user commands, then passes control to the requested program. CCP can then be overlayed.

Each requested program is loaded from disk into the Transient Program Area, and receives control from CCP. The TPA contains the program until the next program is requested or the system is booted.

A complete discussion of CP/M is found in "The Attache CP/M Guide."

CP/M Memory Locations

Attache's memory of 64K bytes equals 256 pages of 256 bytes each. The lowest page of memory is reserved for system use. The next 195 pages comprise the Transient Program Area for loading user programs. Another eight pages contain the Console Command Processor. This area can be overlayed after control is passed to the transient program, which allows approximately 52K bytes of user program memory.

The 14 memory pages above CCP contain the Basic Disk Operating System. The highest 38 pages of memory are reserved for the BIOS. Illustration 3-1 is a chart of CP/M memory.

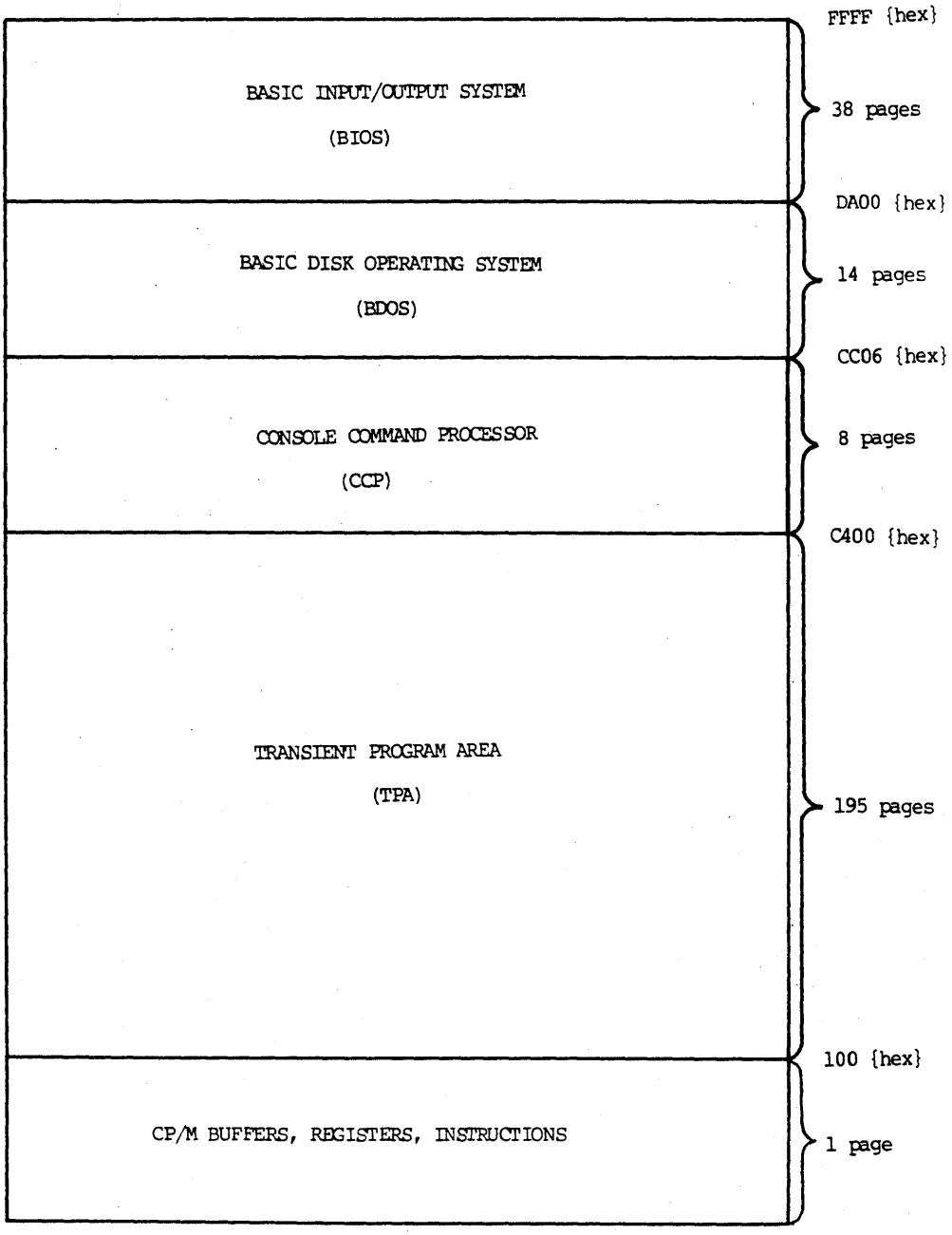


Illustration 3-1 CP/M Memory Map

Low Memory Map

Page 0, or "base page", is the first 256 bytes of memory. These bytes are reserved for CP/M registers, pointers, and instructions. Illustration 3 - 2 is a chart of the bytes.

Page Zero

Hex Address	Contents
0000 - 0002	Jump instruction to warm boot entry at CCP + 1603 {hex}. This allows a simple programmed restart (JMP 0000H) or a manual restart from the keyboard.
0003	IOBYTE
0004	Current default drive number (0 = A, 1 = B).
0005 - 0007	Jump instruction to BDOS. JMP 0005H provides the primary entry point to the BDOS; LHLD 006H brings the address field of the instruction (the highest address in the TPA if CCP is overlayed) to the HL register pair.
0008 - 0027	Interrupt locations 1 - 5. Not Used.
0030 - 0037	Interrupt location 6. Not Used. Reserved.
0038 - 003A	Restart 7 : Jump instruction into the DDT or SID program when running in debug. Not otherwise used.
003B - 003F	Not Used. Reserved.
0040 - 004F	Scratch area for BIOS. Reserved.
0050 - 005B	Not Used. Reserved.
005C - 007C	Default file control block produced for a transient program by the Console Command Processor.
007D - 007F	Optional default random record position.
0080 - 00FF	Default logical 128 byte disk buffer. (Also the command line when a transient is loaded under CCP.)

Illustration 3-2 Low Memory Maps

The first instruction in the base page is Jump to Warm Boot. A warm boot is performed every time a program is exited. This reloads the CCP, in case CCP was overlayed.

The next byte contains the IOBYTE. IOBYTE is a facility which enables Attache to assign different logical devices to different physical devices. IOBYTE is one byte at location 0003 {hex} which identifies the logical device to the physical device. The byte is divided into four two bit fields, each representing one device.

Use of the IOBYTE is described on page 3-6.

A Jump to BDOS instruction resides in bytes 5 - 7 and is used for BDOS functions.

Locations 5C - 7C {hex} contain the default File Control Block (FCB). All disk I/O operations use File Control Blocks, which contain the file name, extent, drive, and allocation numbers. The FCB identifies to BDOS which Allocation Units are assigned to a file. Illustration 3-3 shows a File Control Block in detail.

The last 128 bytes in the base page are used as a default disk buffer.

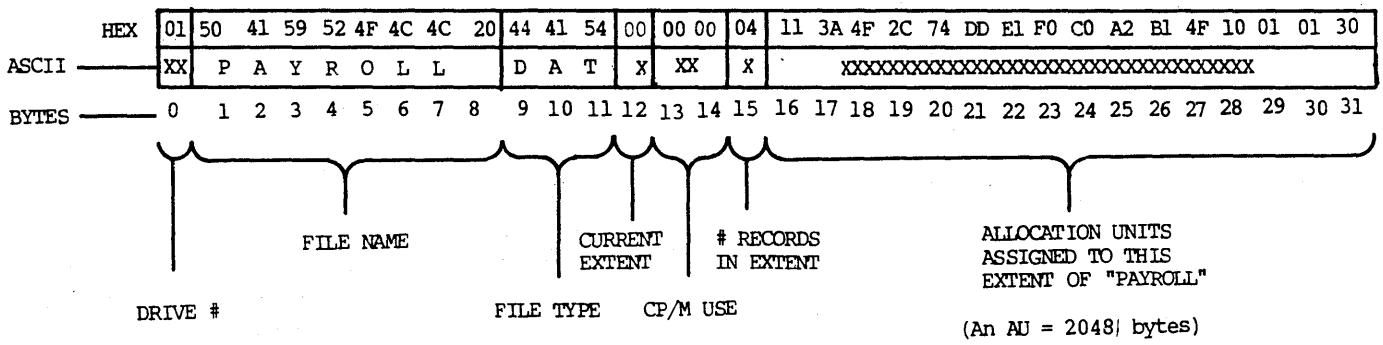


Illustration 3-3 File Control Block

IOBYTE

The IOBYTE is a byte which determines which logical device is assigned to which physical device. BDOS uses four logical devices: the Console, the List, the Punch, and the Reader. BIOS uses three physical devices: the Printer Port, the Console, and the Communication Port.

When an Input/Output operation is requested, BIOS checks the IOBYTE to determine which physical device to use. For example, a List I/O is required. BIOS interrogates the two high order bits of the IOBYTE and reads "10." BIOS calls the line printer as the physical device in this example.

The CP/M STAT command may be used to change the logical to physical device assignments of the system. For example, to change the list device from the printer to the communication device, type in "STAT LST: = TTY:" from the A> prompt.

Illustration 3-4 is the Attache implementation of the system device and the IOBYTE structure.

CP/M DEVICE	LOGICAL DEVICE	IOBITS	PHYSICAL DEVICE
LST:	TTY:	00	Comm. Port
	CRT:	01	Internal CRT
	LPT:	10	Printer Port
	UL1:	11	Printer Port
PUN:	TTY:	00	Comm. Port
	PTP:	01	Internal CRT
	UP1:	10	Printer Port
	UR2:	11	Comm. Port
RDR:	TTY:	00	Comm. Port
	PTR:	01	Printer Port
	UR1:	10	Internal Crt
	UR2:	11	Comm. Port
CON:	TTY:	00	Comm. Port
	CRT:	01	Internal CRT
	BAT:	10	Printer Port
	UC1:	11	Internal Crt

IOBYTE Default Values

PHYSICAL DEVICES	LST:	PUN:	RDR:	CON:
INITIAL VALUES	10	00	00	01
BIT POSITIONS	76	54	32	10

Default Devices

LST: = LPT:
PUN: = TTY:
RDR: = TTY:
CON: = CRT:

Illustration 3-4 IOBYTE

Read-Only Memory Software

Attache contains four Read-Only Memory chips (ROMs). One is used by the hardware for I/O device selection. This ROM works in conjunction with the Direct Memory Access controller (DMA) for I/O transfers.

A second ROM, an Erasable Programmable ROM (EPROM), is used in the Display section of the processor board. The ROM displays dot patterns which depict ASCII characters. The ASCII bytes are sent to the internal video, and the ASCII character is displayed on the screen. Changing this ROM would change the character set displayed.

The third ROM is located in the Floppy control section of the processor board. The ROM is part of the data separator which discerns data from clock pulses when the diskette is read.

The fourth ROM is an EPROM that contains the initial software which locates the Boot Loader portion of BIOS on disk. It also contains the Terminal Emulation routine, and the Monitor routine which turns on diagnostics.

The EPROM loads an initial bootstrap to FE00 {hex}, then passes control to FE00 {hex}. The EPROM bootstrap is a routine which loads the BIOS bootstrap from disk. The BIOS bootstrap then loads the CP/M.

Terminal Emulation is a terminal look-alike routine which allows Attache to emulate two different non-intelligent terminals.

The Monitor routine allows the user to run diagnostics, communications, to manually alter memory, and to pass system control.

Attache Terminal Emulation Mode

The system enters Terminal Emulation upon reset when no disk is in Drive A or the Bootstrap Loader cannot be read from the disk.

Terminal Emulation Mode provides direct interface with other asynchronous devices, allowing Attache to emulate two different non-intelligent terminals (the Lear Siegler ADM-3A and the DEC VT-52). This mode is a superset of both the ADM-3A and VT-52 and not separate modes for each.

Lear Siegler ADM-3A functions are fully supported, with the exception of the lock and unlock keyboard functions. Illustration 3-5 is a list of control code functions in ADM-3A emulation. For more information, refer to the ADM-3A Operator's Handbook.

CTRL G	Sounds audible beep
CTRL H	Backspace
CTRL J	Line Feed (moves cursor down one line)
CTRL K	Moves cursor up one line
CTRL M	Carriage Return
CTRL Z	Clear Screen
CTRL ^	Home

Illustration 3-5 ADM-3A Control Codes

All **except** the following DEC VT-52 functions are supported: ESC (033 076), exits alternate keypad mode and returns to numeric keypad; ESC Z, requests a terminal identification; ESC [/ ESC (033 134), enters / exits Hold-screen mode; and Printer Option escape codes. (ESC I does not perform a scroll.)

Illustration 3-6 is a list of supported DEC VT-52 escape code functions. For more information, consult the Digital Direct Sales Catalog.

ESC A	Moves cursor up one line
ESC B	Moves cursor down one line
ESC C	Moves cursor one column to the right
ESC D	Moves cursor one column to the left
ESC H	Moves cursor home
ESC I	Moves cursor up one line
ESC J	Erases data from cursor to screen end
ESC K	Erases data from cursor to end of line
ESC Y	Moves cursor to specified screen position

Illustration 3-6 DEC VT52 Escape Codes

Pressing **CTRL** and **LINE FEED** puts the system in Monitor Mode. Monitor mode allows the user to run diagnostics, to manually alter memory, and to run communications. Pressing **CTRL** and **LINE FEED** again takes Attache out of Monitor Mode and back to Terminal Mode.

Terminal Emulation is initialized at 9600 baud. This baud rate may be changed through the Monitor Mode by using the "S" command. This command allows you to activate one or both ports and specify baud rates for each.

Selections default to the communications port if neither port is selected. If both ports are selected, input is accepted from either and output is sent to both.

To change the baud rate or to select a different port:

1. Enter Monitor Mode by pressing **CTRL** and **LINE FEED** at the same time.

2. Enter the 'S' command for the desired baud rate. The format for S is as follows:

```
bbpcS
||||_____ communications port  (0 = deselect, 1 = select)
|||_______________ printer port  (0 = deselect, 1 = select)
||__ communications baud rate  (see Baud Rate Table *)
|_____________ printer baud rate  (see Baud Rate Table *)
```

*** Baud Rate Table**

0 = no change	4 = 600 Baud	8 = 9600 Baud
1 = 110 Baud	5 = 1200 Baud	9 = 19200 Baud
2 = 150 Baud	6 = 2400 Baud	
3 = 300 Baud	7 = 4800 Baud	

The four characters to the left of "S" determine which port or ports are active and the baud rate selection for each. Codes for selecting communications port baud rates only are as follows:

0110S = 110 Baud	0410S = 600 Baud	0710S = 4800 Baud
0210S = 150 Baud	0510S = 1200 Baud	0810S = 9600 Baud
0310S = 300 Baud	0610S = 2400 Baud	0910S = 19200 Baud

3. **RETURN** is not required. The selections are changed automatically when the S command is issued.

4. Return to Terminal Emulation Mode by pressing **CTRL** and **LINE FEED** at the same time.

Illustration 3-7 Changing Baud Rates in Terminal Emulation

Monitor Mode - Diagnostics

Monitor Mode contains diagnostics which test all of the major functions of Attache. These diagnostics may be run by keying in the commands which follow.

Enter Monitor Mode:
1) Remove diskette from drive A.
2) Press **SHIFT** and **RESET** simultaneously.
3) Press **CTRL** and **LINE FEED** simultaneously.

List of Tests:

G - Generate Display Pattern

H - Display RAM Test

I - Input Test

J - Jump

K - Keyboard Test

L - Loop Tests

M - Memory Map Test

O - Output Test

P - Format Diskette

Q - CMOS Memory Test

R - Main Memory Test

S - Select Output Port

T - Real-Time Clock Test

U - United Tests

V - Read Disk Sector

W - Write Disk Sector

X - I/O Port Transmit Test

Y - I/O Port Receive Test

Z - Disk Drive Test

Illustration 3-8 Monitor Mode Diagnostics

G - Generate Display Pattern - G

Format: G

Description: The display screen fills with the character "+" in every position of the display except the cursor position (the lower right hand corner).

Exit: Press any key to return Attache to the monitor command entry mode.

Reporting: No errors are detected or reported.

H - Display Ram Test - H

Format: H

Description: Tests all bits and locations of the alphanumeric, graphic, and attribute display memories.

Exit: Automatic at end of test. Test completes in approximately 3 seconds.

Reporting: Errors are reported in the format "llccddff", where:
ll = line containing error.
cc = character position of the error.
dd = two 1's in bit positions in error.
ff = frame in which the error is located:
00 - 80 = graphics RAM
C0 = alphanumeric RAM
E0 = attribute RAM

The frame code corresponds directly to the display memory IC's on the processor board as follows:

00 = U704	40 = U706	80 = U708	E0 = U432
20 = U705	60 = U707	C0 = U433	

I - Input Test - I

Format: nnI where nn = port number

Description: Allows one byte to be read from the selected port. Can be used in conjunction with the output command to read status or data from a port.

Exit: Automatic after byte is read.

Reporting: None.

J - Jump - J

Format: addrJ where addr = address to which system is to jump.

Description: System jumps to the address specified and begins program execution.

If no address is specified, a jump to the monitor entry point occurs; if a system diskette is in Drive A, a system boot occurs, otherwise the system enters Terminal Mode.

Exit: None.

Reporting: None.

K - Keyboard Test - K

Format: K

Description: All keys pressed after "K" are displayed, followed by their hexadecimal value. Note that both upper and lower case codes may be returned.

Exit: Type the character "^".

Reporting: No errors are detected or reported.

L - Loop Tests - L

Format: L

Description: Tests entered after "L" run continuously.

Exit: Press any key to return the system to monitor command mode.

Reporting: The looping test reports errors as during normal test execution.

M - Map Test - M

Format: M

Description: The memory is mapped, and numbers 7-1 are written in the first location of each block 1-7. The memory is then remapped to the standard configuration, and the numbers are read back.

Exit: Automatic at end of test, less than 3 seconds.

Reporting: Any virtual block which returns an erroneous number reports an error as "vn", where v is the virtual block number and n is the number the block returned.

O - Output Test - O

Format: nnmmO where nn = port number; mm = data to send.

Description: Sends a byte to the specified port. Can be used in conjunction with the input command to send data to a port and then read status or data from the port.

For example: **F244O** sends ASCII character "D" to the printer port.

Exit: Automatic after byte is sent, less than 3 seconds.

Reporting: None.

P - Format Diskette - P

Format: P or 1P where P = format the Drive A diskette, and 1P = format Drive B diskette.

Description: Diskette in specified drive is formatted.

Exit: Automatic at end of format, or immediately by pressing any key to return the system to monitor command entry mode. Formatting requires less than 35 seconds.

Reporting: Reports diskette error status.

Note: The format produced is not the same format CP/M uses. Use the P test for testing purposes only. Do not use a diskette which contains valuable data or programs when running this test.

Q - CMOS RAM Test - Q

Format: Q

Description: Runs a memory test of each bit of the CMOS RAM.

Exit: Automatic at end of test. Test completes in approximately .5 seconds.

Reporting: Any bad location is reported as "aadd", where aa = address 00 - 3F {hex} and dd = the data bits 0 - F {hex} which failed.

Note: This test may cause CMOS RAM to reset to its default values, depending upon the EPROM version of the system. If the Terminal Mode header is "Otrona Attache", the Set-up Mode parameters will reset to their default settings. If the header is "Otrona Attache x" (where "x" is any letter), the parameters will remain at their current settings.

R - Main RAM Test - R

Format: nR where n is the RAM row number 0 - 3.

Description: The main RAM is constructed in four rows of 16K bytes each. The R test maps the row being tested to virtual address 8000 - BFFF {hex} and tests each memory location with all data bits.

Exit: Automatic at end of test. Test completes in approximately 2.5 minutes.

Reporting: The first 9 errors found are reported as "aaaa-dd", where aaaa = the address displacement of the bad location from the row's starting address, and dd = data bits in error.

S - Select Output Ports - S

Format: bbpcS where 0 = deselect; 1 = select

```
||||
||| --- communications port
|| ---- printer port
| ----- communication baud rate
 ------ printer baud rate
```

Baud Rates

0 = not changed
1 = 110 baud
2 = 150 baud
3 = 300 baud
4 = 600 baud
5 = 1200 baud
6 = 2400 baud
7 = 4800 baud
8 = 9600 baud
9 = 19,200 baud

Description: The printer and communications ports are selected to print test commands and results. The selections of the "S" command are also used by the X and Y, transmit and receive, tests.

If Terminal Mode is entered from the Monitor, Attache defaults to the communication port if neither port is selected. If both ports are selected, input is accepted from either port, and output is sent to both.

Reporting: No errors are detected or reported.

T - Real-Time Clock Test - T

Format: T

Description: Tests the real-time clock function without disturbing the current clock setting.

Exit: Automatic at end of test. Test completes in approximately 2 seconds.

Reporting: A "?" is displayed if the clock fails.

U - United Tests - U

Format: U {test(s)} **RETURN**

Description: Runs the test(s) entered after "U" in sequence.

For example: **UHQT** runs the Display RAM, CMOS RAM, and Real-Time Clock Tests in sequence.

If no test is specified after the "U", the following tests are performed:

H, Q, T, M, 0R, 1R, 2R, 3R, 0Z, 1Z

Exit: Automatic at end of test(s), or immediately by pressing any key to return the system to monitor command entry mode.

Reporting: Each test reports errors as in normal execution.

V - Read a Sector From a Disk - V

Format:

```
cchsV
||||
|||sector number
||side:
||     0 = drive 0, head 0
||     1 = drive 1, head 0
||     4 = drive 0, head 1
||     5 = drive 1, head 1
cylinder number (0 - 27 {hex})
```

Description: The specified disk sector is read into memory at FF00 - FFFF {hex}.

Exit: Automatic at end of data transfer, less than 5 seconds.

Reporting: An error detected in the transfer reports as cchs-ssee where cchs = the sector selected; ss = controller status register ST0; and ee = controller status register ST1.

ssee is interpreted as (X - Don't Care):

0000 = Error in transfer from controller to RAM
2X0X = Error cased by: drive select jumpermissing, door not closed, head not loaded, no disk in logged drive, or disk not spinning properly.
4X01 = Missing address mark
4X01 = Missing sector ID
4X20 = CRC error in data or ID field.
4800 = Drive not ready.

Any other code = error caused by floppy disk controller.

W - Write a Sector to a Disk - W

Format:
```
cchsV
||||
|||sector number
||side:
||     0 = drive 0, head 0
||     1 = drive 1, head 0
||     4 = drive 0, head 1
||     5 = drive 1, head 1
cylinder number (0 - 27 {hex})
```

Description: The specified disk sector is written to from the memory at address FF00 - FFFF {hex}.

Exit: Automatic at end of data transfer.

Reporting: An error detected in the transfer reports as cchs-ssee where cchs = the sector selected; ss = ST0; and ee = ST1. "ssee" is interpreted the same as in the V Test.

X - I/O Port Transmit - X

Format: nnnnmmmmX where nnnn = number of bytes to transmit {hex}; mmmm = start of data area from which to transmit.

Description: Transmit data to another system through the port(s) selected by "S" command to another system in Y (receive) Test mode. Data format is as follows:

```
CR
nn
nn
etc.
CR
```

where "nn" is two characters per data byte, sent in pseudo-hex (0,1,2,3,4,5,6,7,8,9,:,;,<,>,?) MSB sent first.

Exit: Automatic at end of data transfer.

Reporting: No errors are detected or reported.

Y - I/O Port Receive - Y

Format: nnnnY where nnnn = address for start of data load.

Description: Receives data from another system through the printer port from a system in X (transmit) Test mode.

Exit: Automatic at end of data transfer.

Reporting: No errors are detected or reported.

Z - Do Automatic Disk Test - Z

Format: Z or 1Z where Z = Drive A, 1Z = Drive B.

Description: The disk in the specified drive is extensively tested in automatic sequence.

Test sequence:

1 - format the diskette with "E5"
2 - write a worst-case test pattern in sector 1, each track of side 0.
3 - read back the test pattern from sector 1 of each side 0 track.
4 - repeat steps 2 and 3 for each sector on side 0.
5 - repeat steps 2 and 4 for side 1

Note: Both Z and 1Z tests require a diskette inserted in Drive A. 1Z Test requires a diskette in Drive B as well.

Exit: Automatic at end of test. Test completes in approximately 5 minutes and 40 seconds.

Reporting: Errors are reported in the following format:

```
cchs-ssee
|||| ||||
|||| ||controller status register ST1 |see chart
|||| controller status register ST0   |
||||
|||sector
||side:
||   0 = drive 0, head 0
||   1 = drive 1, head 0
||   4 = drive 0, head 1
||   5 = drive 1, head 1
cylinder number (0 - 27 {hex})
```

ssee is interpreted as (X - Don't Care):

0000 = Error in transfer from controller to RAM
2X0X = Error cased by: drive select jumper missing, door not closed, head not loaded, no disk in logged drive, or disk not spinning properly.
4X01 = Missing address mark
4X01 = Missing sector ID
4X20 = CRC error in data or ID field.
4800 = Drive not ready.

Any other code = error caused by floppy disk controller.

Note: The entire contents of the diskette are erased in this test. Disk tests are only as reliable as the media being used. Be sure that the inserted diskette is functional.

BIOS (Basic Input/Output System) Introduction

BIOS is the tailor-made portion of CP/M which defines the Attache hardware environment to the non-hardware dependent portions of CP/M.

This description of Attache's BIOS is divided into the following subjects: Bootstrap, Disk Driver, I/O Drivers, Display Driver, Interrupt Structure, CMOS RAM and Clock routines, and Valet service routines.

This section also contains charts of commonly used programming functions. These charts are referenced in the List of Illustrations on page viii.

BIOS resides on the first three tracks of a system diskette. BIOS is loaded into memory at power on if the system diskette is properly inserted in Drive A.

An Erasable Progammable Read-Only Memory chip contains the initial software to load the BIOS Bootstrap Loader from disk. The BIOS Bootstrap loads the CP/M operating system.

When BIOS first loads, the Attache sign-on screen displays:

CP/M 2.2.x OTRONA ATTACHE [56K]

where "2.2" is the current version of CP/M, and ".x" is Attache's revision. [56K] is CP/M's calculation of the memory available to the user after CP/M has loaded.

Boot Loader

The Boot Loader, or Bootstrap, is a two-part routine. The first section, located in EPROM, merely loads the second section, located on track 0, sector 1 of the system diskette.

The second part of the routine loads the CP/M operating system into memory from C400 {hex} to F9FF {hex}. (F9FF {hex} to FFFF {hex} is a reserved BIOS storage area.) The routine also loads system parameters from CMOS RAM (Complementary Metal-oxide Semiconductor Random Access Memory). The user specifies these system parameters in set-up mode (ie. the options described on top of the keyboard template).

Cboot

After the system boots, Attache goes to a routine called CBOOT. Cboot sets up the system. It initializes the system values by accessing the parameters stored in CMOS RAM. These parameters are: keytone, brightness, printer Baud rates, Communication Baud rates, bell, volume, and shift lock.

Cboot looks at the CMOS RAM to see if it is set. It looks for a 5 in location 1, and an E in location 0. If the values are not there, the CMOS RAM has either never been initialized or the battery has run down. Cboot will then reinitialize the RAM and reset the devices to default values.

Cboot initializes the IOBYTE and the remaining values in page 0.

Attache uses one of two different brands of clocks with different BIOS clock routines. Cboot looks to see which brand of clock is being used, and calls the routine accordingly.

(Programming CMOS RAM, and the sound generator is accomplished by writing escape codes to the Display Driver. The clock is programmed via the TIME.COM program. These instructions begin on page 3-44, immediately following the Display Driver section.)

Disk Driver

The disk driver section of BIOS contains the routines which handle the physical disk operations. The routines set up the floppy controller and the Direct Memory Access controller (DMA) for disk operations, send disk I/O commands, and handle the physical read, write, and format operations.

The disk driver routines perform two major functions: blocking/deblocking, and physical read/write.

Blocking/Deblocking

CP/M is written to expect 128 byte disk sectors. Attache uses 512 byte sectors. The blocking/deblocking routines in BIOS perform the translation from BDOS's logical sectors of 128 bytes, to the physical 512 byte sector size.

Four logical sectors exist in each physical sector. Blocking/Deblocking routines receive the logical address for a requested sector, and calculate the physical address on diskette. The logical sector is then stored at the address specified by the DMA Address field in CP/M.

Physical Read/Write

Disk routines are interrupt driven. Three types of routines work together to perform the physical read/write operations. These are the Read Host/Write Host routines, the Floppy routines, and the Floppy Interrupt routine.

The interface between the three routine types is accomplished via a status byte called Disk Cycle. Disk Cycle is continuously updated to reflect current status of the read/write operation.

During a disk operation, BDOS passes control to the Read Host or Write Host routines. Read Host or Write Host uses the translated addresses from the Blocking/Deblocking routine to set up registers A, B, C, D, E, and HL. These registers contain the sector address information.

Read Host or Write Host then loops on the Disk Cycle byte and checks for either a successful completion code or an error code. The routine returns control to BDOS when the operation completes successfully.

If an error code is stored in the Disk Cycle status byte, Read Host or Write Host calls a disk error routine which gives the user the options to retry, warmboot, or ignore the error.

If the register contains a successful completion code, Read Host or Write Host returns the processor to the calling program.

The Floppy routines control the actual read, write, or format on diskette. The routines set up the Direct Memory Access controller (DMA) and the floppy controller (FDC) to initiate the disk operation. Floppy routines issue the commands which start the motor, recalibrate, seek, and initiate read, write or format.

When the disk operation is complete, the DMA issues a terminal count to the FDC, which in turn issues an interrupt.

Every time a floppy interrupt is issued by the floppy controller, the Floppy Interrupt routine is called. The interrupt routine checks the status of the Disk Cycle byte, and calls the next appropriate portion of the Floppy routine. The interrupt routine then updates Disk Cycle.

The Floppy routine initiates its current function, and the FDC issues another interrupt when the function is complete. This process repeats until the entire disk operation is complete, and the interrupt updates the Disk Cycle to reflect a successful completion. Consequently, Read Host or Write Host returns to the calling program.

Disk operations also use the 60 Hz Interrupt routine during Motor Start Up. The 60 Hz routine updates the Disk Cycle byte according to the status of the Start Up operation.

The 60 Hz Interrupt turns the floppy motor off and checks for disk time outs. The routine puts a wait condition in the Disk Cycle until the motor has come up to speed. It also puts a time out error code in Disk Cycle if the disk has not completed an operation within one second.

Illustration 3-9 shows an example of the physical read/write portion of the disk driver. The example is a simplified read operation for illustrative purposes only. The illustration is intended to demonstrate the general software flow of floppy interrupts.

NOTE - Recalibrate is performed twice to ensure accuracy of the diskette head location. The head recalibrates once, seeks to track 4, then recalibrates a second time.

Devices (or routines)

BDOS
Read Host
60 Hz Interrupt routine
Disk
Floppy Disk Controller (FDC)
Floppy Interrupt Routine
Floppy routine

Chronological Actions

0. If motor already running, then skip to Step 7a.

1. Start disk motor.

2. Wait 2/3 second for motor to come up to speed; set Disk Cycle to 8 (waiting for ready).

3. After 2/3 second, issue Sense Drive Status command to FDC.

4. If status Okay, issue Recal command to FDC; set Disk Cycle to 4 (first recalibrate). Else Error.

5. Floppy Interrupt: Read result bytes from previous operation. If Okay, issue seek to track 4, set Disk Cycle to 5 (seek to track 4). Else Error.

6. Floppy Interrupt: Read result bytes from previous operation. If Okay, issue Recal command to FDC; set Disk Cycle to 6 (second recalibrate). Else Error.

7. Floppy Interrupt: Read result bytes from previous operation. If Okay,
7a. issue Seek to Track (desired track for I/O); set Disk Cycle to 7 (seek to track). Else Error.

8. Floppy Interrupt: Read result bytes from previous operation. If Okay, issue Read; set Disk Cycle to 3 (data read). Else Error.

9. Floppy Interrupt: Read result bytes from previous operation. If Okay, Return; set Disk Cycle to 0 (successful completion). Else Error.

Illustration 3-9 Disk Read Operation

Input/Output Driver

The Input/Output (I/O) Drivers define the physical I/O devices to the software. A standard table of jump vectors to logical I/O devices is loaded at page DA00 {hex}. This table allows BDOS and user application programs to call logical I/O Driver routines. The logical routines then interrogate the IOBYTE and pass control to the appropriate physical I/O Driver routine.

I/O Driver routines are divided into two types of routines. These routines are physical routines which deal with the actual device, and logical routines which deal with the device as the CP/M software describes it.

The logical routines are: Conin (console character input), Conout (console character output), Const (console status), List, Listst (list device test), Punch, and Reader.

The physical routines are: Crtout, Crtin, Ttyin (tele-type character input), Ttyout (tele-type character output), Ptrin (printer character input), Lptout (line printer output), Tsttty (test tele-type device), and Lpttst (line printer test).

Additional Functions

I/O Drivers are also used to service the control latch, and to access the sound generator.

The control latch performs CRT brightness control, enables the floppy motor, enables the EPROM, and enables graphic memory. The control latch is a history dependent latch which cannot be read. A register, L Latch preserves the state of that latch. A bit can be gated to the latch to clear or set bits in the latch.

The sound routine reads a 15 byte table. The sound generator chip requires fourteen bytes. A fifteenth counter byte determines the time length of the sound. The sound routine loads register HL with the beginning address of the table. The routine then reads the table and sends it to the sound generator.

The generator creates the Attache audio feedback. The counter byte is loaded into a timer which is decremented by the 60 Hz routine. Every 60th of a second the count decrements. When the count gets to zero, the 60 Hz routine shuts the sound off.

The sound routine is accessed directly by sending escape codes to the Display Driver. Programming the sound generator is discussed on page 3-46.

Programming I/O Devices : Z80 SIO Initialization

	Data Address	Status Address	SIO Channel
Communications Port:	F0 Hex	F1 Hex	A
Printer Port:	F2 Hex	F3 Hex	B

Register	Hex	Binary
0	D8	1 1 0 1 1 0 0 0

```
  |   |     |_____ Register 0
  |   |___________ Channel Reset
  |_______________ Reset Tx Underrun/EOM Latch
```

Register	Hex	Binary
1	60	0 1 1 0 0 0 0 0

```
| | |  |  | | |_____ Ext Int Enable
| | |  |  | |_______ Tx Int Enable
| | |  |  |_________ Status Effects Vector-B
| | |  |____________ Rx Int Disable
| | |_______________ Wait/Ready on R/T
| |_________________ Wait/Ready Function
|___________________ Wait/Ready Enable
```

Register	Hex	Binary
3	C1	1 1 0 0 0 0 0 1

```
|  | | | | | | |_____ Rx Enable
|  | | | | | |_______ Sync Character Load Inhibit
|  | | | | |_________ Address Search Mode (SDLC)
|  | | | |___________ Rx CRC Enable
|  | | |_____________ Enter Hunt Phase
|  | |_______________ Auto Enables
|  |_________________ Rx 8 Characters/Bit
```

Register	Hex	Binary
4	44	0 1 0 0 0 1 0 0

```
|   |   |  | | |_____ Parity Enable
|   |   |  | |_______ Parity Even/Odd
|   |   |  |_________ 1 Stop Bit/Character
|   |   |____________ 8 Bit Sync Character
|   |________________ X16 Clock Mode
```

Register	Hex	Binary
5	EA	1 1 1 0 1 0 1 0

```
|  |  | | | | | |_____ Tx CRC Enable
|  |  | | | | |_______ RTS
|  |  | | | |_________ SDLC/CRC-16
|  |  | | |___________ Tx Enable
|  |  | |_____________ Send Break
|  |  |_______________ Tx 8 Bits/Character
|  |_________________ DTR
```

Programming the SIO BAUD Rate

The baud rates of the ports may be changed within a program by sending escape codes to the Display Driver. The procedure requires writing to the CMOS RAM, and setting the baud rates.

The printer baud rate is at location 7 of the CMOS RAM; communications baud rate is at location 8.

The following chart contains the data to be written to the CMOS RAM.

DATA	BAUD
0	75
1	110
2	134.5
3	150
4	300
5	600
6	1200
7	2400
8	4800
9	9600
A	19200

Setting the baud rate requires sending the proper escape code to the Display Driver. An **ESC ;** sets the printer baud, and **ESC <** sets the communications baud.

The following example sets the Communications baud rate to 300.

Example

```
MVI C,1BH
CALL CONOUT
MVI C,"@"
CALL CONOUT
MVI C,8
CALL CONOUT
MVI C,4
CALL CONOUT
MVI C,1BH
CALL CONOUT
MVI C,"<"
CALL CONOUT
```

Illustration 3-11 Programming Baud Rates

NOTE: A special communications feature has been added to BIOS, called the Break key. Pressing **CTRL** and **LINE FEED** puts a high level to the communication port for two seconds to signal the communication device.

The baud rates of the ports are controlled by a Z80 Counter Timer Circuit. The CTC is I/O mapped at:

Communication Port CTC = address 00F4 {hex}
Printer Baud CTC = address 00F5 {hex}

Baud rates may also be programmmed by sending bytes to the CTC, instead of accessing the Display Driver. However:

NOTE: Baud rates set by a program remain in effect until a power on or a shift - reset. Therefore, any program which changes the Baud rate, should restore the initial Baud rate before returning to CP/M.

The VALET SET-UP will not reflect programmed Baud rates.

Determine the bytes to send to the CTC from the following table:

Baud Rate {hex}	Command Byte {hex}	Data Byte {hex}
75.0	0037	000D
110.0	0057	00AF
134.5	0057	008F
150.0	0057	0080
300.0	0057	0040
600.0	0057	0020
1200.0	0057	0010
2400.0	0057	0008
4800.0	0057	0004
9600.0	0057	0002
19200.0	0057	0001

Illustration 3-12 Writing to the CTC

I/O Ports

The following chart, Illustration 3-13, is a list of I/O port locations and functions.

The Z80A Central Processing Unit uses an output signal, /IORequest, to indicate that the lower half of the address bus contains one of these I/O addresses. As a result, memory need not be utilized to access I/O locations.

```
00E0        FPYBCA    =    0E0H      ;FLOPPY STATUS PORT
00E1        FPYBWR    =    0E1H      ;FLOPPY DATA PORT
00E2        DSPBCA    =    0E2H      ;DISPLAY BASE & CURRENT ADDRESS
00E3        DSPBWR    =    0E3H      ;DISPLAY BASE & WORD COUNT
00E4        STDBCA    =    0E4H      ;STD BUS BASE & CURRENT ADDRESS
00E5        STDBCA    =    0E5H      ;STD BUS BASE & WORD COUNT
00E6        SIOBCA    =    0E6H      ;SIO BASE & CURRENT ADDRESS
00E7        SIOBWR    =    0E7H      ;SIO BASE & WORD COUNT
00E8        DMACSR    =    0E8H      ;DMA COMMAND/STATUS REGISTER
00E9        DMAWRR    =    0E9H      ;DMA WRITE REQUEST REGISTER
00EA        DMAWSM    =    0EAH      ;DMA WRITE SINGLE MASK BIT
00EB        DMAWMR    =    0EBH      ;DMA WRITE MODE REGISTER
00EC        DMACBP    =    0ECH      ;DMA CLEAR BYTE FLIP-FLOP
00ED        DMATMP    =    0EDH      ;DMA TEMP REG & MASTER CLEAR
00EE        SDSPY     =    0EEH      ;DISPLAY COMMAND/STATUS
00EF        DMAWAM    =    0EFH      ;DMA WRITE ALL MASK REG BITS
00F0        DCOMM     =    0F0H      ;COMM PORT DATA
00F1        SCOMM     =    0F1H      ;COMM PORT STATUS
00F2        DPRTR     =    0F2H      ;PRINTER PORT DATA
00F3        SPRTR     =    0F3H      ;PRINTER PORT STATUS
00F4        BAUDC     =    0F4H      ;BAUD TIMER FOR COMM PORT
00F5        BAUDP     =    0F5H      ;BAUD TIMER FOR PRINTER PORT
00F6        DSPINT    =    0F6H      ;DISPLAY INTERRUPT (60 HZ)
00F7        FPYINT    =    0F7H      ;FLOPPY INTERRUPT TIMER
```

(continued on next page)

```
00F8        DPIOA       =       0F8H        ;       PIO PORT A DATA
                                            ;       A0-7    =   LATCH DATA OUT:
                                            ;       L0      =   MOTOR ON
                                            ;       L1      =   GRAPHICS ENABLE
                                            ;       L2      =   /EPROM ENABLE
                                            ;       L3-7    =   DISPLAY BRIGHTNESS
                                            ;       A0-7    =   8910 DATA I/O:
                                            ;       A0-3    =   5832 D0-3 I/O
                                            ;       A4-7    =   5832 A0-3 OUT
                                            ;       A0-3    =   5101 D0-3 I/O
                                            ;       A4-7    =   5101 A0-3 OUT
00F9        SPIOA       =       0F9H        ;PIO PORT A COMMAND
00FA        DPIOB       =       0FAH        ;PIO PORT B DATA
                                            ;       B0-1    =   5101 A4-5
                                            ;       B2-4    =   OPERATION SELECT
                                            ;           0   =   8910 ADDR LOAD
                                            ;           1   =   8910 DATA LOAD
                                            ;           2   =   5832 WRITE
                                            ;           3   =   5832 READ
                                            ;           4   =   5101 WRITE
                                            ;           5   =   5101 READ
                                            ;           6   =   LATCH LOAD
                                            ;           7   =   NO-OP
                                            ;         B5    =   /'138 OPERATION STROBE
                                            ;         B6    =   /KEYBOARD DATA IN
                                            ;         B7    =   /KEYBOARD CLOCK OUT
00FB        SPIOB       =       0FBH        ;PIO PORT B COMMAND
00FC        SFLPY       =       0FCH        ;FLOPPY COMMAND/STATUS
00FD        DFLPY       =       0FDH        ;FLOPPY DATA
00FE        DDSPY       =       0FEH        ;DISPLAY DATA
00FF        DMAP        =       0FFH        ;RAM VIRTUAL MAP DATA
```

Illustration 3-13 I/O Ports

Display Driver

The Display Driver is the largest portion of the BIOS. The display driver contains the routines the system needs to interface with the display. The routines read from, or write to, the Attache screen.

The Display Driver may be accessed via escape codes or control codes. Each code points to a routine within the Display Driver which performs that function. These codes are loaded into the Z80 CPU register C, and Conout is called to perform the code's corresponding function.

The codes necessary to access the display driver with Assembly language are contained in this chapter. The codes for accessing the display in Basic are found in the Attache "Basic-80" handbook.

The complete set of ASCII character codes is listed in both decimal and hexadecimal in Illustration 2-31, page 2-71. Note that BASIC-80 interprets ASCII codes in decimal.

Accessing The Display Driver

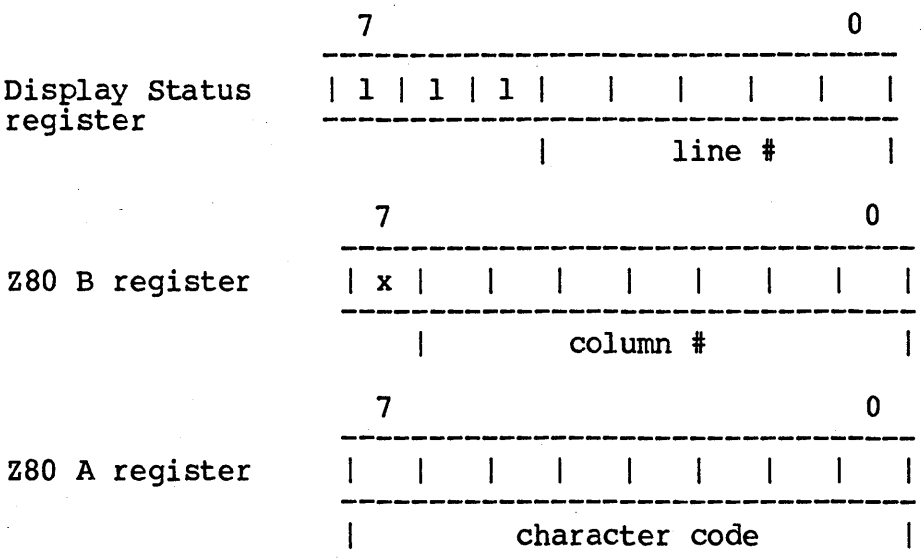
The display subsystem is I/O mapped at the following addresses:

Address	Type	Function
00EE	W	Command
00FE	R/W	Data

Commands written to the command address are held in a display register to be used with the A8 - A15 address bus lines to determine the screen location of the data.

Data to and from the display is transferred via the data address.

Character Transmission

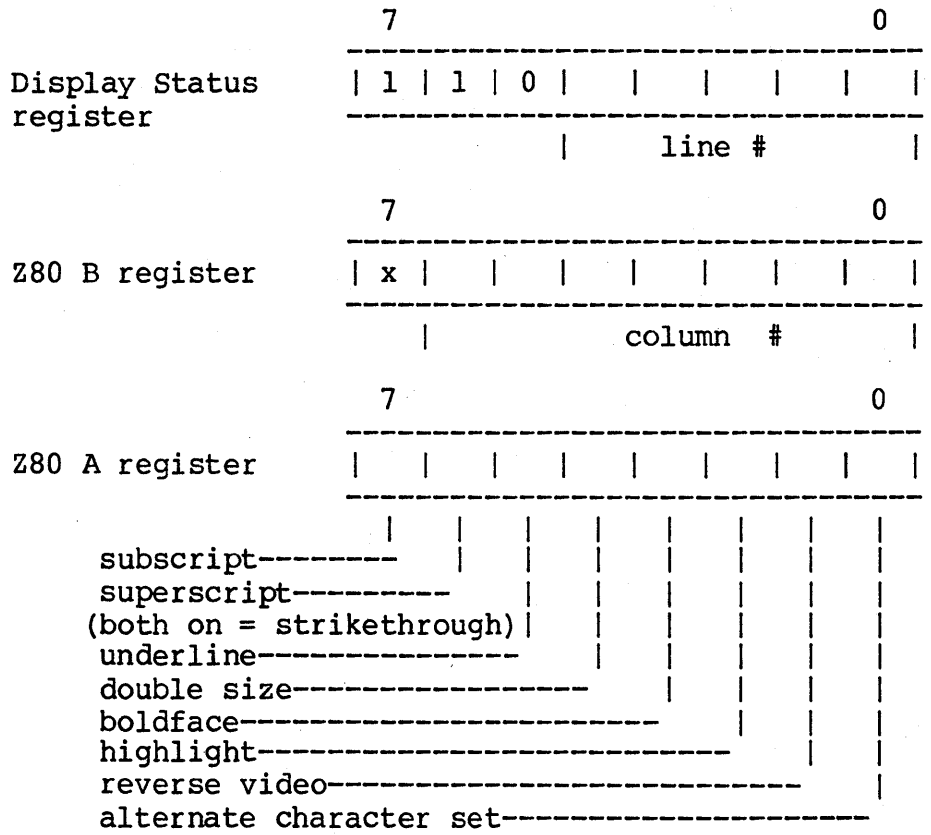


Example

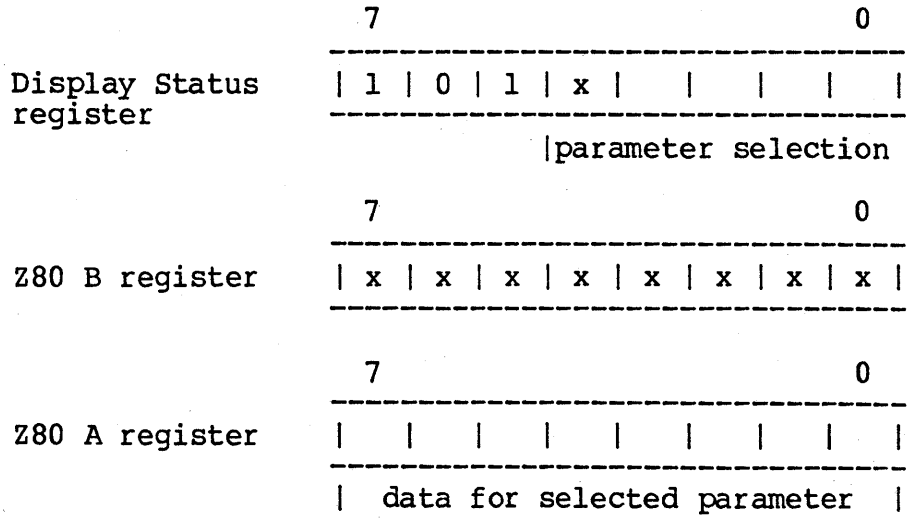
send an ASCII X character to row 1, column 1.

```
CMD     EQU  00EEH        ; display register I/O port number
INFO    EQU  00FEH        ; data for display I/O port number
CHAR    EQU  00E0H        ; display command for character transmission
;
X:      MVI  A , CHAR     ; character transmission command
        OR   1            ; combine above with line #
        OUT  CMD          ; send to display register
        MVI  B,1          ; column # to appear on address lines of bus
        MVI  A,'X'        ; data for display
        MVI  C,INFO       ; I/O port for display information
        OUT  (C),A        ; transfer information to display
        RET
```

Attribute Transmission



Display Control Parameters Transmission



Graphic Data Transmission

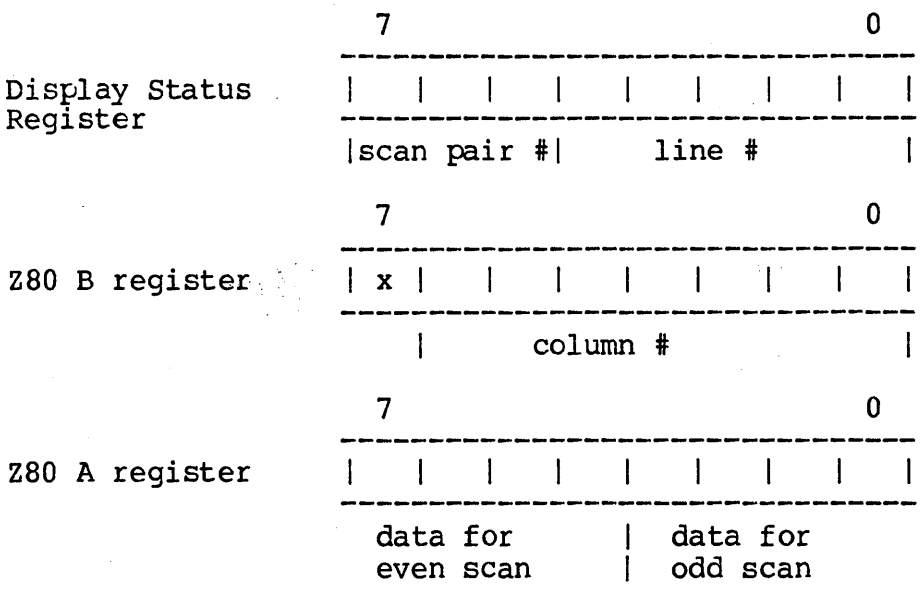


Illustration 3-14 Writing to the Display

Note: When accessing graphics, the display status register uses the three high order bits to select one of the five graphic scan pairs (ie. segments), and the five low order bits to select one of the 24 lines. See Illustration 2-17, page 2-41 for a diagram of graphic segments.

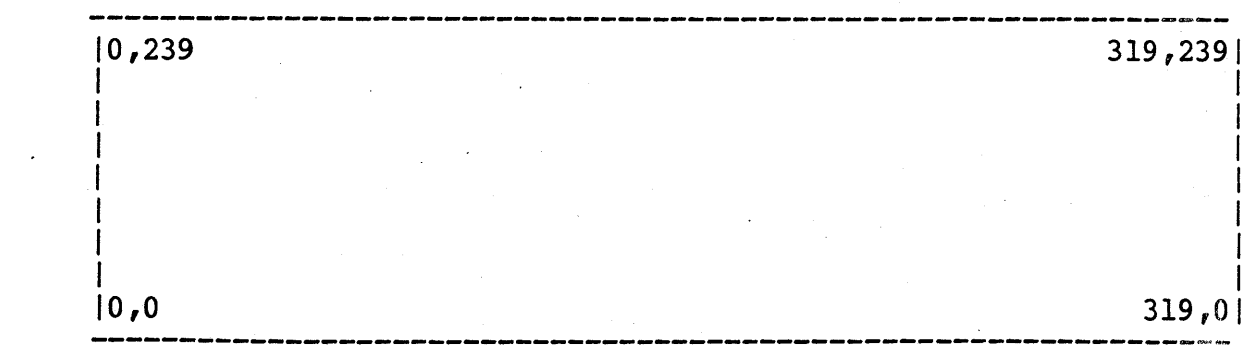
Attache Escape Codes

Escape and Control codes are used to invoke Display Driver functions. These codes are summarized in the following tables. The escape code precedes a character string that passes instructions to the display driver. These codes must be keyed in upper case to be recognized.

Graphic Escape Codes

ESC 0xxyy	Plot Point - plots to points specified by (xx) and (yy).
ESC 1xxyy	Plot Vector - plots a vector from last point plotted to (xx,yy).
ESC 2xxyyxxyy	Block Draw - specifies two points (xxyy) and (xxyy) and draws a rectangle using those points as diagonal corners (upper left and lower right).
ESC 3	Clear Graphics and Plot Bright - clears graphics memory and sets to plot.
ESC 4xxyyxxyy	Block Fill - specifies two points (xxyy) and (xxyy) and fills a rectangle using those points as diagonal corners (upper left and lower right).
ESC 5 m1m2	Set Masks - sets pattern for block fill with bytes m1 and m2 as bit maps for the block fill mask.
ESC 6	Disable Graphic Image - turns off graphics memory.
ESC 7	Enable Graphic Image - turns on graphics memory.
ESC 8	Set to Plot Bright - sets to plot graphics.
ESC 9	Set to Plot Dark - sets to erase graphics.

The screen locations are designated as follows:



Coordinate pairs are expressed as xxyy where xx is 0 - 319 modulo 64 and yy is 0 - 239 modulo 64. **Note:** A 40 {hex} offset can be added to the x and y coordinates when using BDOS function calls or high level languages.

Cursor Control Escape Commands

Note: ESC Xtb sets active region where t = top line, and b = bottom line.

ESC A	Cursor Up - moves cursor up one line, but not beyond the active region (see ESC I for movement above active region).
ESC B	Cursor Down - moves cursor down one line, but not below active region.
ESC C	Cursor Right - moves cursor right one column, but not past right end of the line.
ESC D	Cursor Left - moves cursor left one column, but not past left end of line.
ESC H	Home - moves cursor to the upper left-most location in the active region.
ESC I	Reverse Line Feed - moves cursor up one position and scrolls active region down if the cursor is at the top of the active region.
ESC Ylc	Direct Cursor Move - moves cursor to location specified as line l, column c of the active region. Variables l and c must have a 20 {hex} offset added
ESC =lc	Direct Cursor Move - moves cursor to location specified by bytes lc (offset by 20H).
ESC c	Cursor off - turns off display of the cursor.
ESC d	Cursor On - displays the cursor

Clear and Delete Escape Commands

ESC J	Erase to End of Screen - deletes all characters from the cursor position to the end of the active region.
ESC K	Erase to End of Line - deletes all characters to the end of the cursor line.
ESC M	Delete Line - deletes a line at the current cursor line. The lines below within the active region are moved up one line and the bottom line is filled with blanks.
ESC P	Delete Character - deletes character at cursor position. All characters to the right of the cursor move one position to the left.

Insertion Escape Commands

ESC L	Insert Line - inserts a line at the current cursor line.
ESC Q	Insert Character Mode On - activates Insert Mode.
ESC R	Insert Character Mode Off - deactivates Insert Mode.

Screen Parameter Escape Commands

ESC Nc..cESC	Set Tabs - sets tabs at position(s) "c" (add offset 2 {hex}).
ESC O	Clear Tabs - clear all tab stops.
ESC Sa	Select Character Size - sets character size "a" (30 or 31 {hex}) to be used until ESC Sa is issued again. a = 1 for a: 0 = 80 column format 1 = 40 column format
ESC Ta	Select Character Set - sets characters set "a" (30 - 33 {hex}) to be used until ESC Ta is issued again. a: 0 = Standard ASCII character set. 1 = Forms ruling set 2 = Greek lower case and math 3 = Greek upper case and math 4 - 7 are unassigned
ESC Ua	Select Attribute - sets screen attribute(s) to be used until ESC Ua is issued again. a: (use Illustration 3-18, Coding Screen Attributes)
ESC Va	Select Alternate Lead-In - sets alternate lead-in "a" to be used in addition to ESC. Allows easier programming in different languages. Both the alternate lead-in and ESC are active.

(continued on next page)

ESC Xtb	Set Active Region - sets top (t) and bottom (b) of active region (add offset 20 {hex}).
ESC Z	Reset Parameters - resets tabs to every eight columns, alternate lead-in to ESC, active region to full screen, character set and size to standard, attributes to off.
ESC \	Clear Screen and Reset Parameters - clears the screen and resets parameters (as in ESC Z).
ESC [	Save Parameters (System Use Only) - saves tabs, alternate lead-in, current active region and cursor position, character set and size, and current attribute selections.
ESC]	Recall Parameters (System Use Only) - recalls all parameters previously saved by ESC [.
ESC ^	Word Wrap Off - sets word wrap flag to "off."
ESC _	Word Wrap On - sets word wrap flag to "on."
ESC `	WordStar Flag Set (On) - enables WordStar keyboard translation.
ESC a	WordStar Flag Reset (Off) - disables WordStar keyboard translation.

Illustration 3-15 Display Driver Escape Codes

System Control Escape Codes

The following control functions may be performed by sending escape codes to the display driver:

ESC Wsl-sl5	Fill Tone Table and Execute - fills a table with 15 bytes to be used by sound generator and makes that sound.
ESC b	Sound Tone From Tone Table - generates sound from table previously set by ESC W.
ESC :	Read Date - reads the date from the real-time clock and places it in the keyboard buffer.
ESC ;	Set Printer Baud From CMOS RAM - reads location 7 in CMOS RAM and uses this value to set printer baud rate.
ESC <	Set Comm Baud Rate From CMOS RAM - reads location 8 in CMOS RAM and uses this value to set communications baud rate.
ESC >	Read Time - reads the time from the real-time clock and places it in the keyboard buffer.
ESC ?a	Read CMOS RAM - reads 4 bit nybble from address "a" and places the value or'ed with 30H in the keyboard buffer (see CMOS Allocation table on 9-1).
ESC @ad	Write to CMOS RAM - writes the least significant nybble of "d" to address "a".

Attache Control Character Codes

CTRL G (07H) Bell

CTRL H (08H) Backspace

CTRL I (09H) Tab

CTRL J (0AH) Line Feed

CTRL K (0BH) Rev. Line Feed

CTRL L (0CH) Right Cursor

CTRL M (0DH) Carriage Return

CTRL X (18H) Clear Keyboard Buffer

CTRL Z (1AH) Clear Active Region/Home Cursor/Clear Graphics Memory

CTRL ^ (1EH) Cursor Home

Illustration 3-17 Control Character Codes

Screen Attribute Codes

ESC Ua (1B 55 __ {hex} or 27 85 __ {decimal})

(where "a" is an ASCII character which represents a hexadecimal or decimal value).

The ESC Ua command selects an attribute(s) to be applied to all characters until another ESC Ua command is issued for another set of attributes. These attributes may be selected alone or in combination in accordance with the table that follows:

ASCII	HEX	DECIMAL	STRIKETHROUGH	SUBSCRIPT	SUPERSCRIPT	UNDERLINE	BLOCK	HIGHLIGHT	REVERSE	INTENSITY	BACKGROUND
SP	20	32	-	-	-	-	-	-	-	MED	OFF
!	21	33	-	-	-	-	-	-	X	OFF	MED
"	22	34	-	-	-	-	-	X	-	MED	LOW
#	23	35	-	-	-	-	-	X	X	OFF	HIGH
$	24	36	-	-	-	-	X	-	-	HIGH	OFF
%	25	37	-	-	-	-	X	-	X	LOW	MED
&	26	38	-	-	-	-	X	X	-	HIGH	LOW
'	27	39	-	-	-	-	X	X	X	LOW	HIGH
(	28	40	-	-	-	X	-	-	-	MED	OFF
)	29	41	-	-	-	X	-	-	X	OFF	MED
*	2A	42	-	-	-	X	-	X	-	MED	LOW
+	2B	43	-	-	-	X	-	X	X	OFF	HIGH
,	2C	44	-	-	-	X	X	-	-	HIGH	OFF
-	2D	45	-	-	-	X	X	-	X	LOW	MED
.	2E	46	-	-	-	X	X	X	-	HIGH	LOW
/	2F	47	-	-	-	X	X	X	X	LOW	HIGH
0	30	48	-	-	X	-	-	-	-	MED	OFF
1	31	49	-	-	X	-	-	-	X	OFF	MED
2	32	50	-	-	X	-	-	X	-	MED	LOW
3	33	51	-	-	X	-	-	X	X	OFF	HIGH
4	34	52	-	-	X	-	X	-	-	HIGH	OFF
5	35	53	-	-	X	-	X	-	X	LOW	MED
6	36	54	-	-	X	-	X	X	-	HIGH	LOW
7	37	55	-	-	X	-	X	X	X	LOW	HIGH
8	38	56	-	-	X	X	-	-	-	MED	OFF

ASCII	HEX	DECIMAL	STRIKETHROUGH	SUBSCRIPT	SUPERSCRIPT	UNDERLINE	BOLDFACE	HIGHLIGHT	REVERSE	INTENSITY	BACKGROUND
9	39	57	-	-	X	X	-	-	X	OFF	MED
:	3A	58	-	-	X	X	-	X	-	MED	LOW
;	3B	59	-	-	X	X	-	X	X	OFF	HIGH
<	3C	60	-	-	X	X	X	-	-	HIGH	OFF
=	3D	61	-	-	X	X	X	-	X	LOW	MED
>	3E	62	-	-	X	X	X	X	-	HIGH	LOW
?	3F	63	-	-	X	X	X	X	X	LOW	HIGH
@	40	64	-	X	-	-	-	-	-	MED	OFF
A	41	65	-	X	-	-	-	-	X	OFF	MED
B	42	66	-	X	-	-	-	X	-	MED	LOW
C	43	67	-	X	-	-	-	X	X	OFF	HIGH
D	44	68	-	X	-	-	X	-	-	HIGH	OFF
E	45	69	-	X	-	-	X	-	X	LOW	MED
F	46	70	-	X	-	-	X	X	-	HIGH	LOW
G	47	71	-	X	-	-	X	X	X	LOW	HIGH
H	48	72	-	X	-	X	-	-	-	MED	OFF
I	49	73	-	X	-	X	-	-	X	OFF	MED
J	4A	74	-	X	-	X	-	X	-	MED	LOW
K	4B	75	-	X	-	X	-	X	X	OFF	HIGH
L	4C	76	-	X	-	X	X	-	-	HIGH	OFF
M	4D	77	-	X	-	X	X	-	X	LOW	MED
N	4E	78	-	X	-	X	X	X	-	HIGH	LOW
O	4F	79	-	X	-	X	X	X	X	LOW	HIGH
P	50	80	X	-	-	-	-	-	-	MED	OFF
Q	51	81	X	-	-	-	-	-	X	OFF	MED
R	52	82	X	-	-	-	-	X	-	MED	LOW
S	53	83	X	-	-	-	-	X	X	OFF	HIGH
T	54	84	X	-	-	-	X	-	-	HIGH	OFF
U	55	85	X	-	-	-	X	-	X	LOW	MED
V	56	86	X	-	-	-	X	X	-	HIGH	LOW
W	57	87	X	-	-	-	X	X	X	LOW	HIGH
X	58	88	X	-	-	X	-	-	-	MED	OFF
Y	59	89	X	-	-	X	-	-	X	OFF	MED
Z	5A	90	X	-	-	X	-	X	-	MED	LOW
[	5B	91	X	-	-	X	-	X	X	OFF	HIGH
\	5C	92	X	-	-	X	X	-	-	HIGH	OFF
]	5D	93	X	-	-	X	X	-	X	LOW	MED
^	5E	94	X	-	-	X	X	X	-	HIGH	LOW
_	5F	95	X	-	-	X	X	X	X	LOW	HIGH

Illustration 3-18 Coding Screen Attributes

Attache Character Sets

ESC Tn (1B 54 __ {hex} or 27 84 __ {decimal})

(where "n" is 0, 1, 2, or 3)

The ESC Tn command selects a character set to be used for all characters until another ESC Tn command is issued for another character set.

Characters sets are as follows:

0 = (standard) ASCII upper and lower case
1 = (alternate-1) Forms ruling set
2 = (alternate-2) Greek lower case and math
3 = (alternate-3) Greek upper case and math

Standard	Alt-1	Alt-2	Alt-3	Standard	Alt-1	Alt-2	Alt-3
@	─	¿	∞	T	┬	◤	⌠
A	├	¡	J	U	┣	↑	⌡
B	┴	←	•	V	└	▽	○
C	┘	Φ	÷	W	┳	Ω	⌈
D	┤	Δ	⌋	X	┻	∈	⌋
E	┐	◥	⌉	Y	┐	£	⌜
F	┼	↕	⌊	Z	└	¶	|
G	┼	Γ	⌋	[	┼	Ø	≅
H	┤	Θ	∠	\	┃	₧	α
I	┬	↑	‖	]	╋	Ü	≠
J	├	∂	⊥	^	|	Ä	≡
K	┳	↓	≤	_	─	Å	±
L	┻	∆	≥	`		¡	⌅
M	┤	→	∴	a	!	α	◆
N	┘	≈	..	b	"	ß	▒
O	┻	Ö	≈	c	#	φ	╞
P	┫	π	≃	d	$	δ	⌠
Q	┏	'	⌠	e	%	∈	╘
R	┌	◤	⌡	f	&	ø	°
S	╋	Σ	⌊	g	'	⁄	±

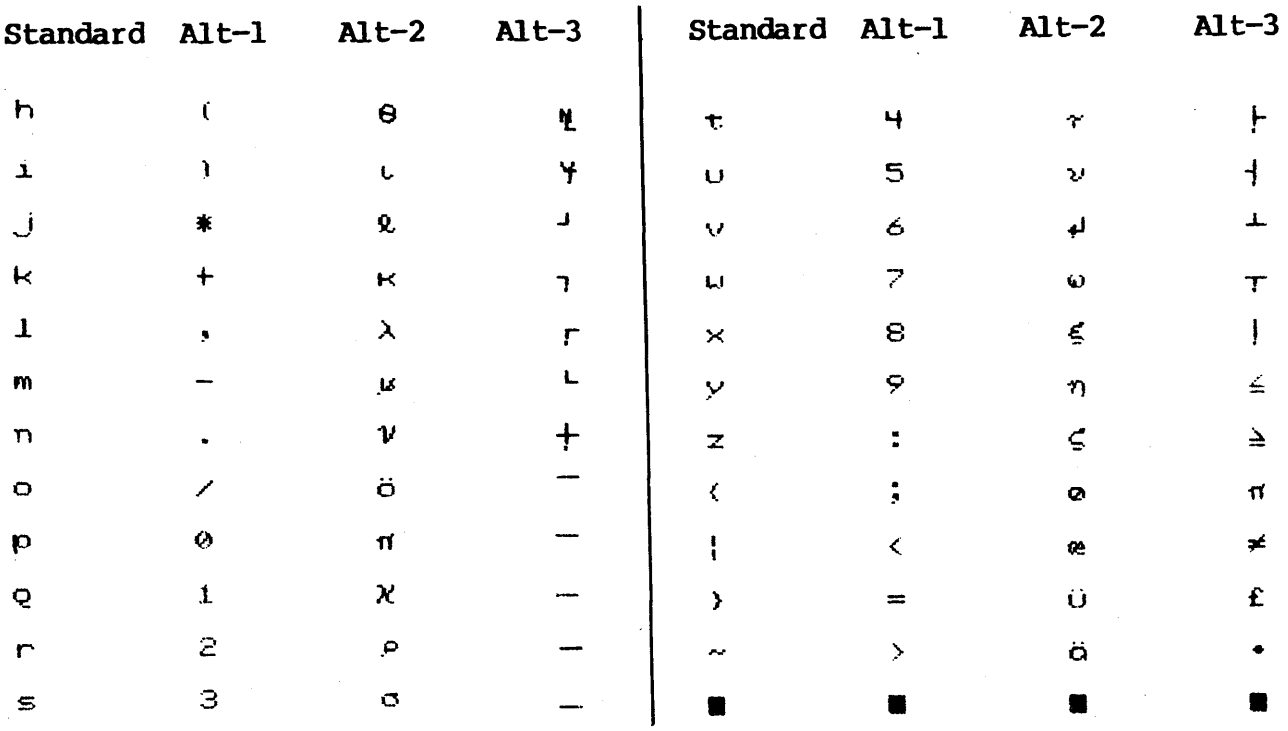


Illustration 3-19 Character Sets

Character Size Selection

ESC Sn (1B 53 __ {hex} or 27 83 __ {decimal})

(where "n" is 0 or 1).

ESC Sn selects a character size to be used for all characters until another ESC Sn command is issued for another character size.

Character sizes are as follows:

0 = 80 column format

1 = 40 column format

CMOS RAM, Clock, and Sound Generator

The BIOS routines to handle the CMOS RAM and the sound generator are accessed through the Display Driver. CMOS RAM is accessible from the set-up mode, at power on, and from VALET. The CMOS RAM, the real-time clock, and the sound generator are all accessible by sending escape codes to the screen.

CMOS Memory Allocation

Read/Write to CMOS RAM is achieved by sending escape codes to the Attache screen. Memory appears organized as 4 bit nybbles to the Z80 CPU. Addresses are 6 bits long and data are 4 bits long. Addresses and data are copied as the least significant bits of a byte. Unused high order bits are ignored by the display driver.

CMOS RAM Organization

Address: 000001
Data: 0101

Z80 Representation of CMOS RAM

Address: **000001
Data: ****0101

* = ignored

CMOS Allocation (Location & Uses) {hex}		Values {hex}
0	System Initialization	E = initialized
1	System Initialization	5 = initialized
2	50 Hz Flag	9 = 50 Hz (otherwise 60 Hz)
3	Time Initialization	E = initialized
4	Date Initialization	5 = initialized
5	Bell Flag	even = on, odd = off
6	Volume	0 - F
7	Printer Baud	0 - A (see Illus. 3-21)
8	Communications Baud	0 - A (see Illus. 3-21)
9	Key Sound	0 - 4 (see Illus. 3-22)
0A	Brightness High	00 - 1F
0B	Brightness Low	00 - 1F
0C	Year Low	0 - 9
0D	Year High	0 - 9
0E	Shift Lock Flag	0 = off, F = on
0F	Next Alarm - Month	1 - C, (F = none set)
10	Next Alarm - Day High	0 - 3
11	Next Alarm - Day Low	0 - 9
12	Next Alarm - Hour High	0 - 2
13	Next Alarm - Hour Low	0 - 9
14	Next Alarm - Minute High	0 - 6
15	Next Alarm - Minute Low	0 - 9
16	Next Alarm - Alarm Number	1 - 6
17	Alarm Type - Next execution mode	0 = message, 1 = command 2 = immediate command

Illustration 3-20 CMOS Allocation Table

Baud Rate Table

Value	Baud
0	75.0
1	110.0
2	134.5
3	150.0
4	300.0
5	600.0
6	1200.0
7	2400.0
8	4800.0
9	9600.0
A	19200.0

Illustration 3-21 Baud Rates

Key Sound Table

Value	Sound
0	Off
1	Click
2	Dink
3	Beep1
4	Beep2

Illustration 3-22 Key Sounds

Programming Sounds or Alarms

The sound generator is user programmable. This section of BIOS changes after CP/M version 2.2.3. The following examples program the sound generator:

CP/M Version 2.2.3

```
10  REM MAKE SOUND
20  PRINT CHR$(27); "W";
30  FOR S=1 TO 15
40  PRINT CHR$(VAL(Z$(S)));
50  NEXT S
```

CP/M Version 2.2.4

```
10  REM MAKE SOUND
20  FOR S=1 TO 15
30  Q=15-S
40  PRINT CHR$(27); "W";CHR$(Q OR &H20);
50  S1=&H30 OR INT(VAL(Z$(S))/16)
60  SUB=(S1 AND &HF)*16
70  S2=&H30 OR (VAL(Z$(S))-SUB)
80  PRINT CHR$(S1);CHR$(S2);
90  NEXT S
```

CP/M Version 2.2.3: Z$(S) is a dimensioned variable where S = 1-15. The first value is the duration (1/60th of a second). Each following value is one register starting with envelope shape/cycle. R14 is loaded first, R0 last. {Print CHR$(27);"b" makes a sound from a table used previously.}

CP/M Version 2.2.4 (and later versions): The bytes are divided into the least significant nybble and the most significant nybble. All bytes are sent with an offset of 20H. The bytes are no longer sent as a block, but are sent individually to the specific register in the format:

```
ESC W ADDR MSN LSN
       |    |   |
       |    |   least significant nybble offset by 20H
       |    most significant nybble offset by 20H
       the synthesizer register offset by 20H
```

In either version, the sound is not executed until **ESC b** is sent to the display driver.

The following sample program accesses the sound generator directly:

```
DPIOA     EQU  0F8H       ; PIO PORT A DATA
SPIOA     EQU  0F9H       ; PIO PORT A STATUS
DPIOB     EQU  0FAH       ; PIO PORT B DATA
SOUND:    DI                ; KEYBOARD DISABLED
          LXI  H,EXPLODE  ; POINT TO EXPLODE SOUND TABLE
          MVI  A,0CFH     ; BIT I/O MODE
          OUT  SPIOA
          XRA  A          ; ALL 8 BITS OUTPUT
          OUT  SPIOA
          MVI  A,0FFH     ; NO DEVICES SELECTED
          OUT  DPIOB
          LXI  B,14*256+DPIOA  ; BYTE COUNT + PIO A DATA PORT
LOOP      DCR  B
          OUT  (C),B      ; SOUND GENERATOR REGISTER NUMBER
          INR  B
          MVI  A,0C3H     ; ENABLE CHIP SELECT, COMMAND
          OUT  DPIOB
          MVI  A,0E3H     ; DISABLE CHIP SELECT, COMMAND
          OUT  DPIOB
          OUTI              ; SOUND GENERATOR REGISTER DATA
          MVI  A,0E7H     ; DISABLE SELECT, DATA
          OUT  DPIOB
          MVI  A,0C7H     ; ENABLE CHIP SELECT, DATA
          OUT  DPIOB
          MVI  A,0E7H     ; DISABLE CHIP SELECT, DATA
          OUT  DPIOB
          JRNZ LOOP
          EI                ; KEYBOARD ENABLED
          RET
EXPLODE:  DB   0          ; R13 ENVELOPE -> DECAY, 1 CYCLE
          DB   56         ; R12 PERIOD = 2.05 SECONDS
          DB   0          ; R11 -|SELECT FULL AMPLITUDE RANGE
          DB   0          ; R10 -|UNDER DIRECT CONTROL OF
          DB   16         ; R9  -|ENVELOPE GENERATOR
          DB   16         ; R8  -|
          DB   16         ; R7  NOISE ONELY, CHANNELS A,B,C
          DB   0          ; R6  SET NOISE PERIOD TO MAXIMUM
          DB   0,0,0,0    ; R5-R2
          DB   0,0        ; R1,R0
NOTONE:   DB   0,0,0,0    ; R13-R10   NOTE: IT MAY BE NECESSARY
          DB   0FH,0FH    ; R9,R8           TO TERMINATE A SOUND
          DB   0FH,0FH    ; R7,R6           USING THIS TABLE -
          DB   0,0,0,0    ; R5-R2           THIS SEQUENCE TURNS
          DB   0,0        ; R1,R0           OFF ANY SOUND
```

Refer to the following chart for programming the sound generator:

Register		Bits B7	B6	B5	B4	B3	B2	B1	B0
R0 R1	Channel A Tone Period	8 Bit Fine Tune A xxxxxxxxxxxxxxxxxx					4 Bit Coarse Tune A		
R2 R3	Channel B Tone Period	8 Bit Fine Tune B xxxxxxxxxxxxxxxxxx					4 Bit Coarse Tune B		
R4 R5	Channel C Tone Period	8 Bit Fine Tune C xxxxxxxxxxxxxxxxxx					4 Bit Coarse Tune C		
R6	Noise Period	xxxxxxxxxxxxxx			5 Bit Period Control				
R7	/Enable	/In - Out		/Noise			/Tone		
		10B	10A	C	B	A	C	B	A
R8	Channel A Amplitude	xxxxxxxxxxxxxx		M	L3	L2	L1	L0	
R9	Channel B Amplitude	xxxxxxxxxxxxxx		M	L3	L2	L1	L0	
R10	Channel C Amplitude	xxxxxxxxxxxxxx		M	L3	L2	L1	L0	
R11 R12	Envelope Period	8 Bit Fine Tune E 8 Bit Coarse Tune E							
R13	Envelope Shape/Cycle	xxxxxxxxxxxxxxxxxx				Cont	Att	Alt	Hold
R14	Sound Duration	equals 0 until a key is pressed							

xxxx = not used

Illustration 3-23 Programming Alarms

Attache Clock

Read Date ESC : (1B 3A {hex} or 27 58 {decimal})

Read Time ESC > (1B 3E {hex} or 27 62 {decimal})

The real-time clock is accessed by writing escape codes to the Display Driver. The requested information is placed into the keyboard buffer as ASCII characters. These characters may be read by applications programs from the keyboard buffer as sequential character strings. If the clock has not been set, the only character returned is "?".

The date and time are placed into the keyboard buffer as:

Date		Time	
Day of Week:	(1-7 - Sunday = 1)	Seconds:	(units)
Day:	(units)	Seconds:	(tens)
Day:	(tens)	Minutes:	(units)
Month:	(units)	Minutes:	(tens)
Month:	(tens)	Hours:	(units)
Year:	(units)	Hours:	(tens)
Year:	(tens)		

Example:

BASIC access to DATE

```
10 PRINT CHR$(27);":"
20 WKDAY$ = INKEY$:
30 DAY$   = INKEY$
40 TDAY$  = INKEY$
50 MO$    = INKEY$
60 TMO$   = INKEY$
70 YR$    = INKEY$
80 TYR$   = INKEY$
90 DATE$  = TMO$ + MO$ + "/"
            + TDAY$ + DAY$ + "/"
            + TYR$ + YR$
100 IF WKDAY$ = "?" THEN DATE$
              = "CLOCK NOT SET"
```

BASIC access to TIME

```
10 PRINT CHR$(27);">"
20 SEC$   = INKEY$
30 TSEC$  = INKEY$
40 MIN$   = INKEY$
50 TMIN$  = INKEY$
60 HR$    = INKEY$
70 THR$   = INKEY$
80 TIME$  = THR$ + HR$ + ":"
            + TMIN$ + MIN$ + ":"
            + TSEC$ + SEC$
90 IF SEC$ = "?" THEN TIME$
           = "CLOCK NOT SET"
```

Illustration 3-24 Accessing the Clock

Interrupt Structure

Introduction

The Attache interrupt structure consists of three types of interrupts: Input/Output device interrupts, floppy disk interrupts, and 60 Hz interrupts.

The 60 Hz Interrupts and Floppy interrupts are processed via a Z80 Counter Timer Circuit. The Z80 CTC contains four channels with the necessary hardware for interrupt processing.

The logic for the CTC is designed to use a daisy-chain interrupt structure. This is accomplished via Interrupt Enable Input lines (IEI) and Interrupt Enable Output lines (IEO). The IEO line of each device on the chain is tied to the lower priority next device's IEI. When a device's IEI line is enabled, its IEO line is disabled. The next device of lower priority is therefore unable to be granted an interrupt until the higher priority device's interrupt is complete.

The CTC's IEI is tied to a high level. The CTC's IEO is tied to the Serial I/O's IEI. The hardware for the SIO is thereby capable of issuing interrupts for the communication and printer ports. The IEO of the SIO goes to the Expansion Connector. Therefore, a device attached via the external connector is the interrupt lowest priority.

Interrupt priority is also assigned to the interrupt channels within the CTC. Channels 0 and 1 are not used for interrupts; channel 0 generates the communication baud rate, and channel 1 generates the printer baud rate. Channel 2 has the highest interrupt channel priority. This is used to issue 60 Hz Interrupts. Channel 3 has the next priority. It issues floppy disk controller interrupts.

Attache uses vectored interrupts, Z80 Interrupt Mode 2. The interrupting device places the least significant byte of the interrupt vector address on the system bus. The CPU appends this byte to a high order byte stored in the CPU Interrupt Register. This high order byte is the address of an interrupt vector table within the first page of the BIOS, which is currently DA {hex}.

For example, an interrupt vector resides at DA62 {hex}. The CPU Interrupt Register contains the byte "DA {hex}". The interrupting device's Interrupt Register contains the byte "62."

I/O Device Interrupts

Attache does not currently use I/O device interrupts. Hardware for interrupt driven I/O is provided, should this type of interrupt be required for a particular user application.

The interrupts can be incorporated into the software by adding no more than five addresses to the interrupt vector table from DAC0 - DAC9 {hex}, and imbedding interrupt service routines at the addresses specified in the table. Interrupt driven I/O devices may then be attached to the communication port, the printer port, or the Expansion Connector.

Interrupt driven I/O can be effectively performed on Attache providing the following points are remembered:

1) Z80 Interrupt Mode 2 (i.e. vectored interrupts) is used by Attache.

2) The devices have the following system priority:

    1) Direct Memory Access (DMA) data transfers
    2) Z80 Counter Timer Circuit (with two channels using interrupt mode)
    3) Z80 Serial I/O (currently polled by Attache BIOS)
    4) Expansion Connector devices (using daisy chain priority)

3) Attache BIOS uses the CTC channels as follows:

    0) Communication baud rate (non-interrupt mode)
    1) Printer baud rate (non-interrupt mode)
    2) 60 Hz interrupt
    3) Floppy Controller Interrupt

4) Nested interrupts are not supported by the BIOS.

5) The Z80A's Interrupt Register is initialized to DA {hex} by BIOS. **This should never be changed.**

6) There is space for an interrupt vector table at DAC0 {hex} consisting of no more than five addresses of interrupt service routines.

Example

This is an example of an ASM program using interrupt driven I/O. The program waits until a character is received by the communication port and then displays it on the internal CRT. This example is provided for illustrative purposes only. Any real application would have the interrupt service routines imbedded within the software.

```
;
;   Z80 SIO Interrupt driven I/O
;
BDOS:    EQU     0005H    ; BDOS entry point
DTA:     EQU     00F0H    ; SIO  A  Data
CTRLA:   EQU     00F1H    ; SIO  A  Status
DTB:     EQU     00F2H    ; SIO  B  Data
CTRLB:   EQU     00F3H    ; SIO  B  Status
SIOR1:   EQU 01111000B    ; INT on all Rx Characters
VECT:    EQU     00C0H    ; Interrupt Vector
TABLE:   EQU    0DAC0H    ; address of interrupt table in BIOS
;
         ORG     0100H    ; TPA
         LXI     H,SERV   ; Load interrupt service routine address
         SHLD    TABLE    ; store at interrupt table in BIOS
         MVI     A,2      ; SIO register number 2
         OUT     CTRLB    ; point to register 2 of SIO channel B
         MVI     A,Vect   ; data for register 2 of SIO channel B
         OUT     CTRLB    ; set-up interrupt vector for SIO
         MVI     A,1      ; SIO register number 1
         OUT     CTRLA    ; point to register 1 of SIO channel A
         MVI     A,SIOR1  ; data for register 1 of SIO channel A
         OUT     CTRLA    ; enable Rx INT on all characters
LOOP:    NOP              ; wait for interrupt
         JMP     LOOP
;
SERV:    IN      DTA      ; get character from SIO
         MOV     E,A      ; pass character to register for BDOS
         MVI     C,2      ; console out BDOS function
         CALL    BDOS     ; pass control to the BDOS
         EI               ; enable interrupts
         DB      0EDH     ; return from interrupt
         DB      04DH     ;    (second byte)
         END
```

Illustration 3-25 Programming Interrupt Driven I/O

Floppy Interrupts

This is a summary of the floppy interrupt structure. Floppy interrupts are discussed in the Disk Driver section of the BIOS on page 3-21.

Floppy interrupts are issued by the floppy controller chip (FDC) on the processor board. The floppy controller places a byte on the system data bus. This byte is the displacement into the Interrupt Vector Table which contains the address of the floppy interrupt routine.

The floppy interrupt routine uses a disk status register called Disk Cycle. The register reflects the current state of the disk operation. Every time a floppy interrupt is issued, the interrupt routine checks the status of Disk Cycle, and calls the proper portion of Disk routine accordingly. The interrupt routine then updates the status register.

A disk driver routine loops on the Disk Cycle register. When the routine detects a successful completion code in the register, the routine returns the system to the program calling point.

This interrupt method ensures that the disk routine performs the proper function at the correct time. The processor does not have to be totally dedicated to the disk operation, as it is performed automatically by the Disk Driver routines.

Disk operations also use the 60 Hz interrupt routine. 60 Hz interrupts turn the floppy motor on, and ensure that the disk is up to speed before any read/write operations are performed. The 60 Hz routine also checks for time outs on disk and issues an error condition accordingly. The 60 Hz routine performs these functions by updating the Disk Cycle register.

60 Hz Interrupts

The 60 Hz interrupt is an interrupt which operates every 60th of a second. This interrupt performs many functions for the system. It checks for pressed keys, generates the proper corresponding key code, checks alarms, checks for Valet enabled, turns off key click and other sounds, times out the floppy motor, and performs Attache tailored keyboard functions.

Keys from the keyboard are set in an 8 x 8 matrix of signal lines. This matrix generates a pattern every time a key is pressed. As soon as key is depressed a signal is output that notifies the 60 Hz interrupt that a key is depressed. The interrupt routine toggles out the data from the matrix and builds a byte from the eight bits. The routine then adds this byte to the beginning of a key table which contains the ASCII codes. (See pages 3-53 - 58, "Generation of Keyboard Character Code" for more information).

The routine turns off key clicks sounds by counting down a timer. When the counter decrements to zero, the routine shuts off the key click. The interrupt routine also shuts off alarms in the same manner.

The 60 Hz interrupt checks for timeout conditions on the diskette drive and issues a timeout error code with the occurrence. Additionally, the 60 Hz routine acts as a timer for the diskette motor. After a certain time elapse with no diskette access, the 60 Hz routine will shut off the diskette motor, thereby reducing diskette wear.

The interrupt routine also performs special keyboard functions for Attache. These functions include special Wordstar key translations used with Wordstar-plus (the routine generates multiple key strokes); entering Valet, Set-up mode, and 10 Key mode.

Generation of Keyboard Character Code

The following charts show the physical keyboard layout and character codes. Two keys, control and shift, affect the code which generates when a key is pressed.

The character codes in the **CTRL** and **CTRL SHIFT** tables are that of Wordstar. Multiple key strokes are automatically combined by the Wordstar version of character codes.

While in Wordstar mode, 6 keys are position dependent: the four arrow keys, **CTRL ^**, and **CTRL -**. An up arrow is 05 {hex}, left arrow is 13 {hex}, right arrow is 04 {hex}, down arrow is 18 {hex}, **CTRL ^** is A8 {hex}, and **CTRL -** is 86 {hex}.

------- PHYSICAL KEYBOARD LAYOUT -------

ESC	1	2	3	4	5	6	7	8	9	0	-	=	BS
TAB	Q	W	E	R	T	Y	U	I	O	P	[	]	LF
CTRL	CAPS	A	S	D	F	G	H	J	K	L	;	'	RTRN
RST	SHFT	Z	X	C	V	B	N	M	,	.	/	SHFT	UP
DEL	`	\				SPACE					LFT	RIT	DWN

ASCII Translation

------- SHIFT -------

1B	21	40	23	24	25	26	2A	28	29	5E	5F	2B	08
09	51	57	45	52	54	59	55	49	4F	50	7B	7D	0A
NA	FE	41	53	44	46	47	48	4A	4B	4C	3A	22	0D
NA	NA	5A	58	43	56	42	4E	4D	3C	3E	3F	NA	1A
07	7E	7C				20					01	06	17

------- CTRL/SHIFT --------

FF	85	C8	D3	B3	B0	A2	AB	B6	A3	1E	0C	0C	08
09	11	17	05	12	14	19	15	09	0F	10	1B	1D	0A
NA	FD	01	13	04	06	07	08	0A	0B	0C	3B	27	0D
NA	NA	1A	18	03	16	02	0E	0D	2C	2E	2F	NA	92
19	00	1C			20						93	84	83

------- NORM -------

1B	31	32	33	34	35	36	37	38	39	30	2D	3D	08
09	71	77	65	72	74	79	75	69	6F	70	5B	5D	0A
NA	NA	61	73	64	66	67	68	6A	6B	6C	3B	27	0D
NA	NA	7A	78	63	76	62	6E	6D	2C	2E	2F	NA	0B
7F	60	5C				20					08	0C	0A

------- CTRL -------

FF	11	FB	0F	10	0B	16	02	D8	C9	CE	1F	81	FC
09	11	17	05	12	14	19	15	09	0F	10	1B	1D	FB
NA	FD	01	13	04	06	07	08	0A	0B	0C	3B	27	0D
NA	NA	1A	18	03	16	02	0E	0D	2C	2E	2F	NA	12
14	00	1C				20					01	06	03

Note: Codes FF through FB {hex} are used internally.

Determining the Character Code

The following charts may be used to determine the logical locations of the keyboard characters as stored in BIOS. The BIOS address of the keyboard character code is found by using the coordinates of the charts.

See the following example.

BIT # =	7	6	5	4	3	2	1	0
OFFSET FROM TABLE START =	NOT SHIFT	CTRL	Y			X		

EXAMPLE: FIND THE UPPER CASE "A" CHARACTER.

(A) FIRST DEDUCE THE 4 DETERMINING CONDITIONS.

CONDITIONS FOR UPPER CASE A WOULD BE:

(1)	SHIFT DEPRESSED	NOT SHIFT = 0 BINARY
(2)	CONTROL NOT DEPRESSED	CONTROL = 0 BINARY
(3)	Y COORD. = 4 =	100 BINARY
(4)	X COORD. = 1 =	001 BINARY

(B) THEN CONSTRUCT THE OFFSET BYTE.

BIT # =	7	6	5	4	3	2	1	0
OFFSET =	0	0	1	0	0	0	0	1

(C) ADD THE OFFSET BYTE TO THE BEGINNING OF THE CHARACTER TABLE.

OFFSET = 00100001 BINARY = 21 HEXADECIMAL
CHARACTER IS AT (TABLE BEGINNING)+21H
IF YOU LOOK AT THIS ADDRESS YOU SHOULD SEE
A 41H (WHICH IS THE ASCII CODE FOR CAPITAL "A")

IN A 56K BYTE CP/M SYSTEM (ATTACHE'S CURRENT SIZE), THE BEGINNING CHARACTER TABLE ADDRESS IS STORED AT LOCATION DAB0 {hex}.

Note: The ASCII chart is listed in Illustration 2-31, page 2-71.

Illustration 3-26 Generating Keyboard Character Codes

---- POSITION OF PHYSICAL KEYS IN KEYBOARD MATRIX --
(UN-SHIFTED)

	0	1	2	3	4	5	6	7
0	BS	TAB	LF	XXXXX	XXXXX	CR	XXXXX	LOCK
1	SPACE	XXXXX	XXXXX	ESC	LEFT	RIGHT	UP	DOWN
2	0	1	2	3	4	5	6	7
3	8	9	'	;	,	=	.	/
4	`	a	b	c	d	e	f	g
5	h	i	j	k	l	m	n	o
6	p	q	r	s	t	u	v	w
7	x	y	z	[	\	]	-	DEL

------- POSITION OF PHYSICAL KEYS IN KEYBOARD MATRIX -------
(SHIFTED)

	0	1	2	3	4	5	6	7
0	BS	TAB	LF	XXXXX	XXXXX	CR	XXXXX	LOCK
1	SPACE	XXXXX	XXXXX	ESC	LEFT	RIGHT	UP	DOWN
2	^	!	@	#	$	%	&	*
3	(	)	"	:	<	+	>	?
4	~	A	B	C	D	E	F	G
5	H	I	J	K	L	M	N	O
6	P	Q	R	S	T	U	V	W
7	X	Y	Z	{	|	}	_	DEL

Character Codes as Stored in BIOS

The following tables are the ASCII keycodes as stored within BIOS. The beginning address of the Shift Key Table is stored at location DAB0 {hex}, (currently 1CAC {hex} from BIOS's beginning address). The hexadecimal displacement of each key from the beginning of the Shift table may be calculated by the procedure on page 3-55.

NOTE: While in Wordstar mode, the four arrow keys, **CTRL ^**, and **CTRL -** are position dependent. The Wordstar keys in hex of arrows are: up = 05, left = 13, right = 04, and down = 18. **CTRL ^** = A8, and **CTRL -** = 86.

SHIFT Key Table

08	09	0A	00	00	0D	00	FE
20	00	00	1B	01	06	1A	17
5E	21	40	23	24	25	26	2A
28	29	22	3A	3C	2B	3E	3F
7E	41	42	43	44	45	46	47
48	49	4A	4B	4C	4D	4E	4F
50	51	52	53	54	55	56	57
58	59	5A	7B	7C	7D	5F	07

CTRL & SHIFT Key Table

08	09	0A	00	00	0D	00	FD
20	00	00	FF	93	84	92	83
1E	85	C8	D3	B3	B0	A2	AB
B6	A3	27	3B	2C	0C	2E	2F
00	01	02	03	04	05	06	07
08	09	0A	0B	0C	0D	0E	0F
10	11	12	13	14	15	16	17
18	19	1A	1B	1C	1D	0C	19

NORMAL Key Table

08	09	0A	00	00	0D	00	FE
20	00	00	1B	08	0C	0B	0A
30	31	32	33	34	35	36	37
38	39	27	3B	2C	3D	2E	2F
60	61	62	63	64	65	66	67
68	69	6A	6B	6C	6D	6E	6F
70	71	72	73	74	75	76	77
78	79	7A	5B	5C	5D	2D	7F

CTRL Key Table

FC	09	FB	00	00	0D	00	FD
20	00	00	FF	01	06	12	03
CE	11	0A	0F	10	0B	16	02
D8	C9	27	3B	2C	81	2E	2F
00	01	02	03	04	05	06	07
08	09	0A	0B	0C	0D	0E	0F
10	11	12	13	14	15	16	17
18	19	1A	1B	1C	1D	1F	14

KEYPAD Table

2A	2C	3D	2E	2F	60	61	62	63	64	65	66	67	68
35	31	32	33	30	6E	36	2B	71	72	73	74	34	

Changing a Keycode in Memory

The definition of keyboard characters may be temporarily modified within a program. The procedure locates the key table beginning, locates the character(s) within the table, and substitutes the new ASCII character code.

The beginning address of the keycode table is stored in location DAB0 {hex}.

In the following example, upper shift "A" is changed to "0".

EXAMPLE

```
10 ADDRESS = PEEK (&HDAB1) * 256 + PEEK (&HDAB0)
20 KEY = ADDRESS + &H21
30 POKE KEY, &H30
```

Statement 10 calculates the table beginning (stored at address DAB0). Statement 20 adds the displacement within the table of the character "A". Statement 30 substitutes the ASCII value of "0".

The displacement within the keycode table for the keyboard character you wish to change may be calculated by the procedure on page 3-55. An ASCII Character chart is located on page 2-71, Illustration 2-31.

Valet

Valet is a software package that allows the user to interrupt a program to perform other functions and then return to the program.

The Valet routines perform alarm functions, screen dumps, printer installation for screen dumps, and calculator functions.

The BIOS Valet routines interrupt the entire system at any time.

A complete description of Valet is located in the Attache "Valet Guide."

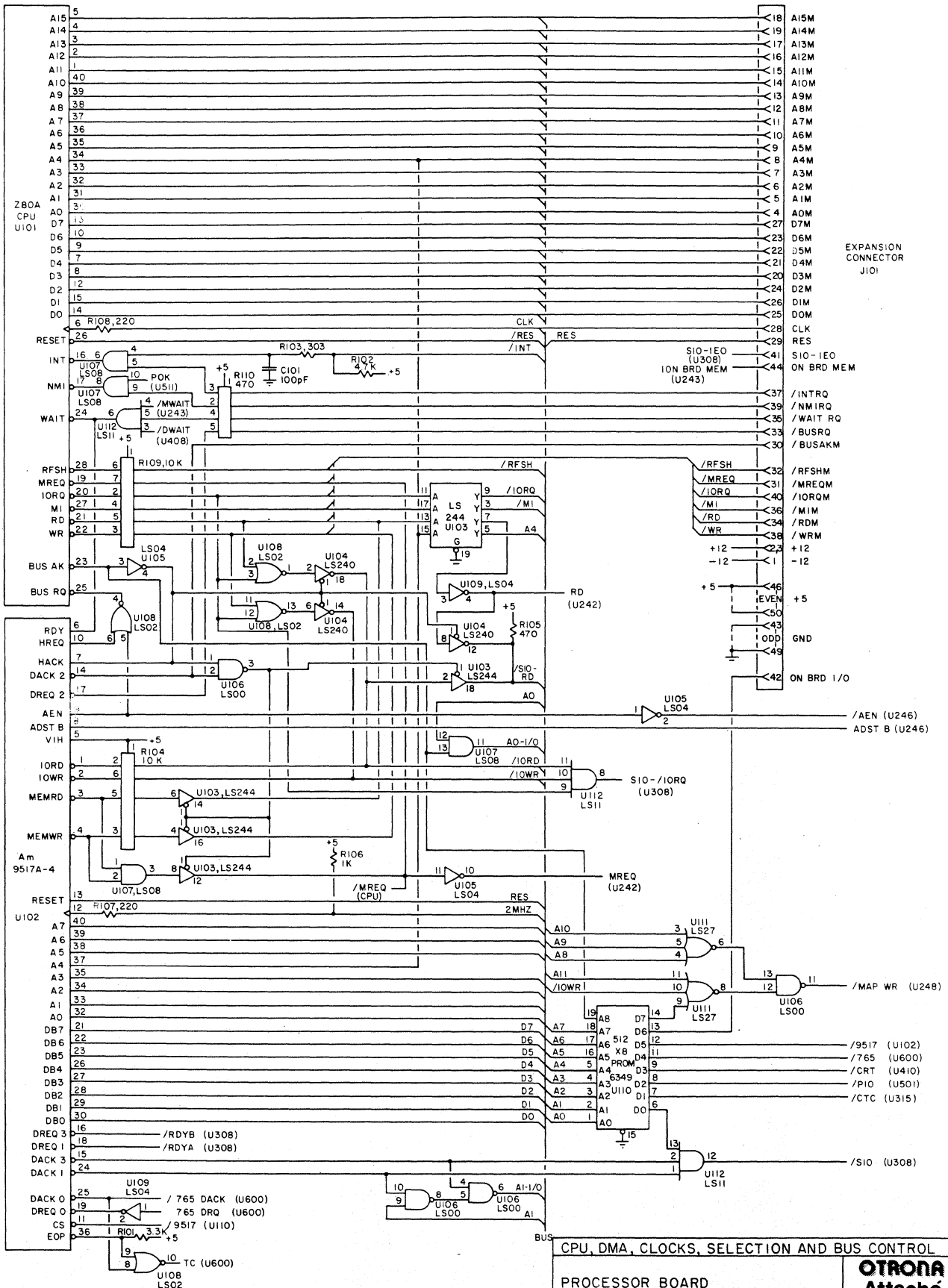
Hexadecimal Conversion Chart

H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	00	000
0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	0
1	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	256	4096
2	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	512	8192
3	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	768	12288
4	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	1024	16384
5	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	1280	20480
6	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	1536	24576
7	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	1792	28672
8	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	2048	32768
9	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	2304	36864
A	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	2560	40960
B	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	2816	45056
C	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	3072	49152
D	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	3328	53248
E	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	3584	57344
F	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	3840	61440

Illustration 3-28 Hexadecimal Conversion Chart

Appendixes

CONTENTS

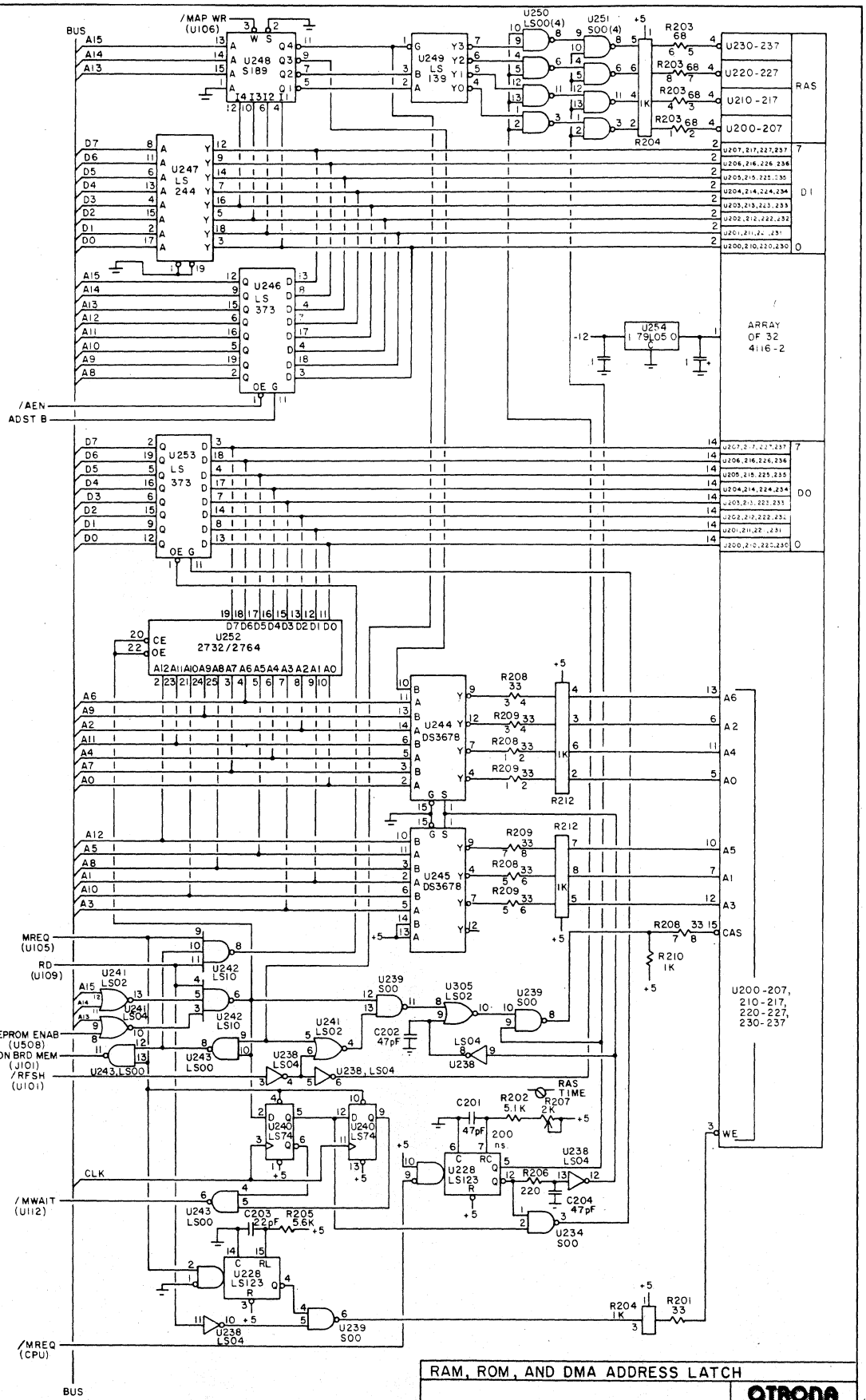


CPU, DMA, CLOCKS, SELECTION AND BUS CONTROL

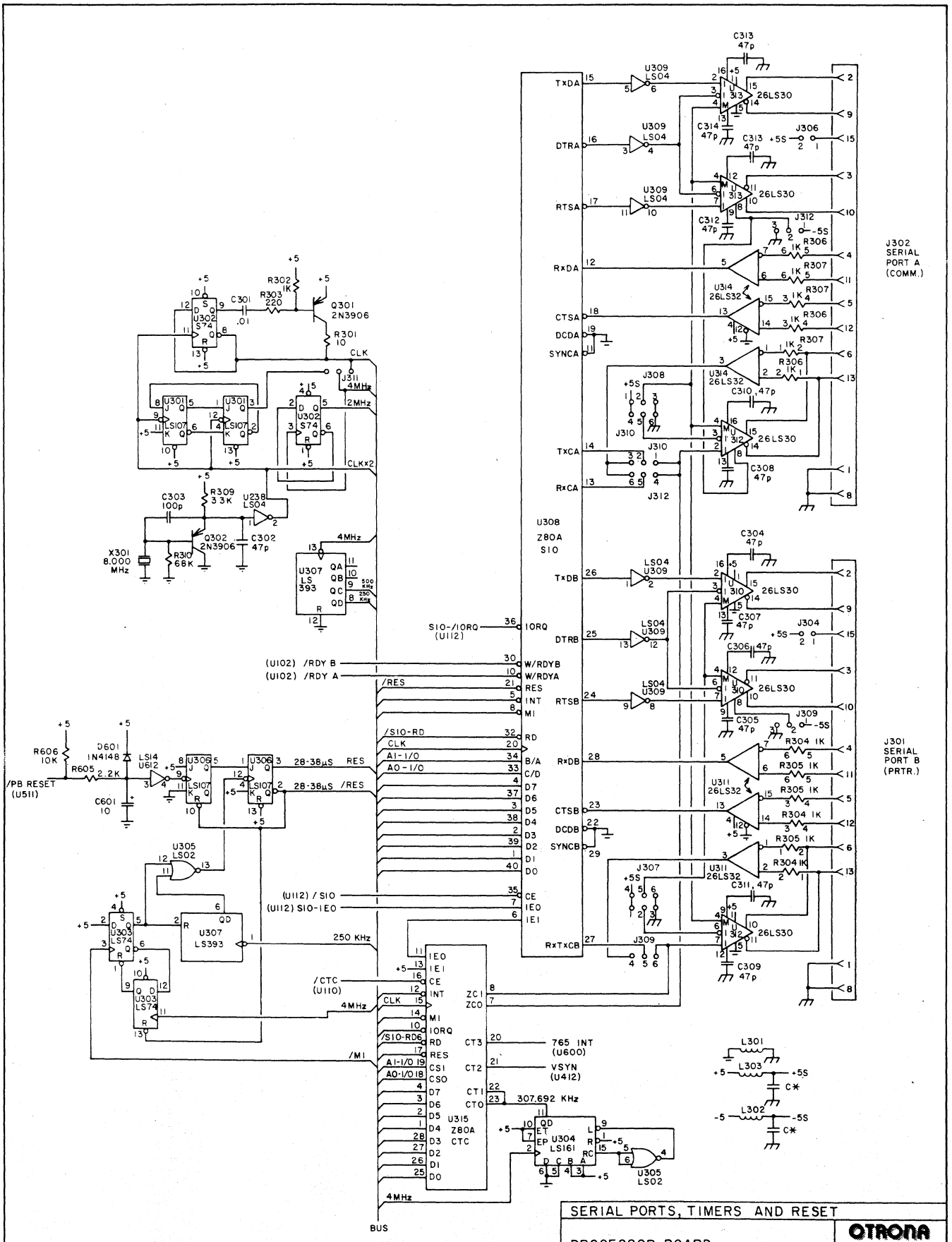
PROCESSOR BOARD

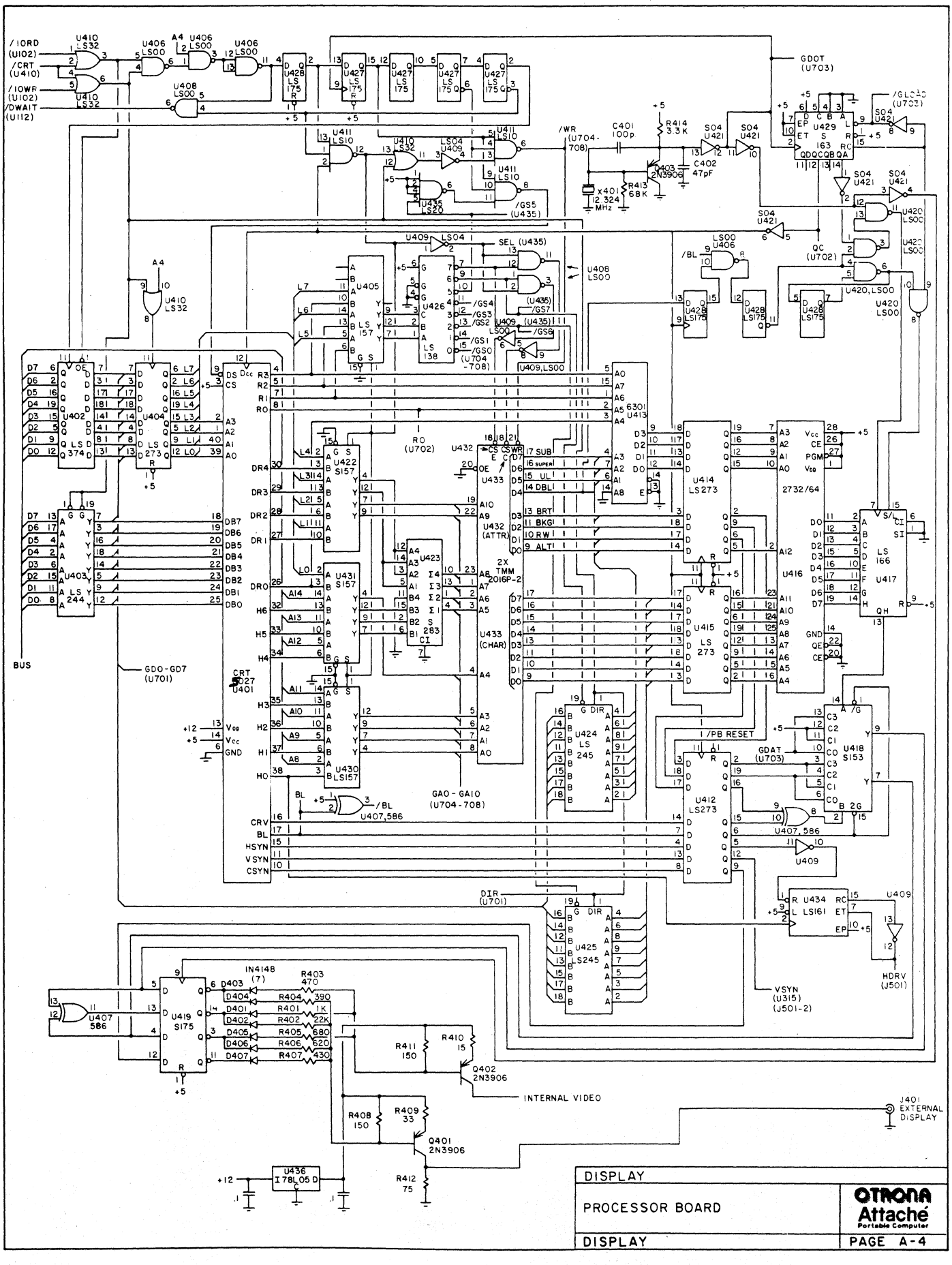
OTRONA Attaché Portable Computer

PROCESSOR



RAM, ROM, AND DMA ADDRESS LATCH	
PROCESSOR BOARD	OTRONA Attaché Portable Computer
MEMORY	PAGE A-2


SERIAL PORTS, TIMERS AND RESET
PROCESSOR BOARD
SERIAL
OTRONA Attaché Portable Computer
PAGE A-3
J302 SERIAL PORT A (COMM.)
J301 SERIAL PORT B (PRTR.)
U308 Z80A SIO
U315 Z80A CTC
TxDA
DTRA
RTSA
RxDA
CTSA
DCDA
SYNCA
TxCA
RxCA
TxDB
DTRB
RTSB
RxDB
CTSB
DCDB
SYNCB
RxTxCB
U309 LS04
26LS30
U314 26LS32
U311 26LS32
U310 26LS30
U312 26LS30
U313 26LS30
J306
J307
J308
J309
J310
J311
J312
J304
C313 47p
C314 47p
C312 47p
C310 47p
C308 47p
C304 47p
C307 47p
C306 47p
C305 47p
C311 47p
C309 47p
R306 1K
R307 1K
R304 1K
R305 1K
+5S
-5S
C*
L301
L303
L302
Q301 2N3906
Q302 2N3906
R302 1K
R303 220
R301 10
C301 .01
R309 3.3K
C303 100p
C302 47p
R310 68K
X301 8.000 MHz
U238 LS04
U307 LS 393
500 KHz
250 KHz
CLK
4MHz
2MHz
CLKx2
U302 S74
U301 LS107
R606 10K
R605 2.2K
D601 IN4148
C601 10
LS14 U612
U306 LS107
28-38µS
RES
/PB RESET (U511)
U305 LS02
U303 LS74
U307 LS393
250 KHz
/CTC (U110)
/MI
/RES
/SIO-RD
A1-I/O
A0-I/O
(U102) /RDY B
(U102) /RDY A
SIO-/IORQ (U112)
(U112) / SIO
(U112) SIO-IEO
765 INT (U600)
VSYN (U412)
307.692 KHz
U304 LS161
U305 LS02
BUS



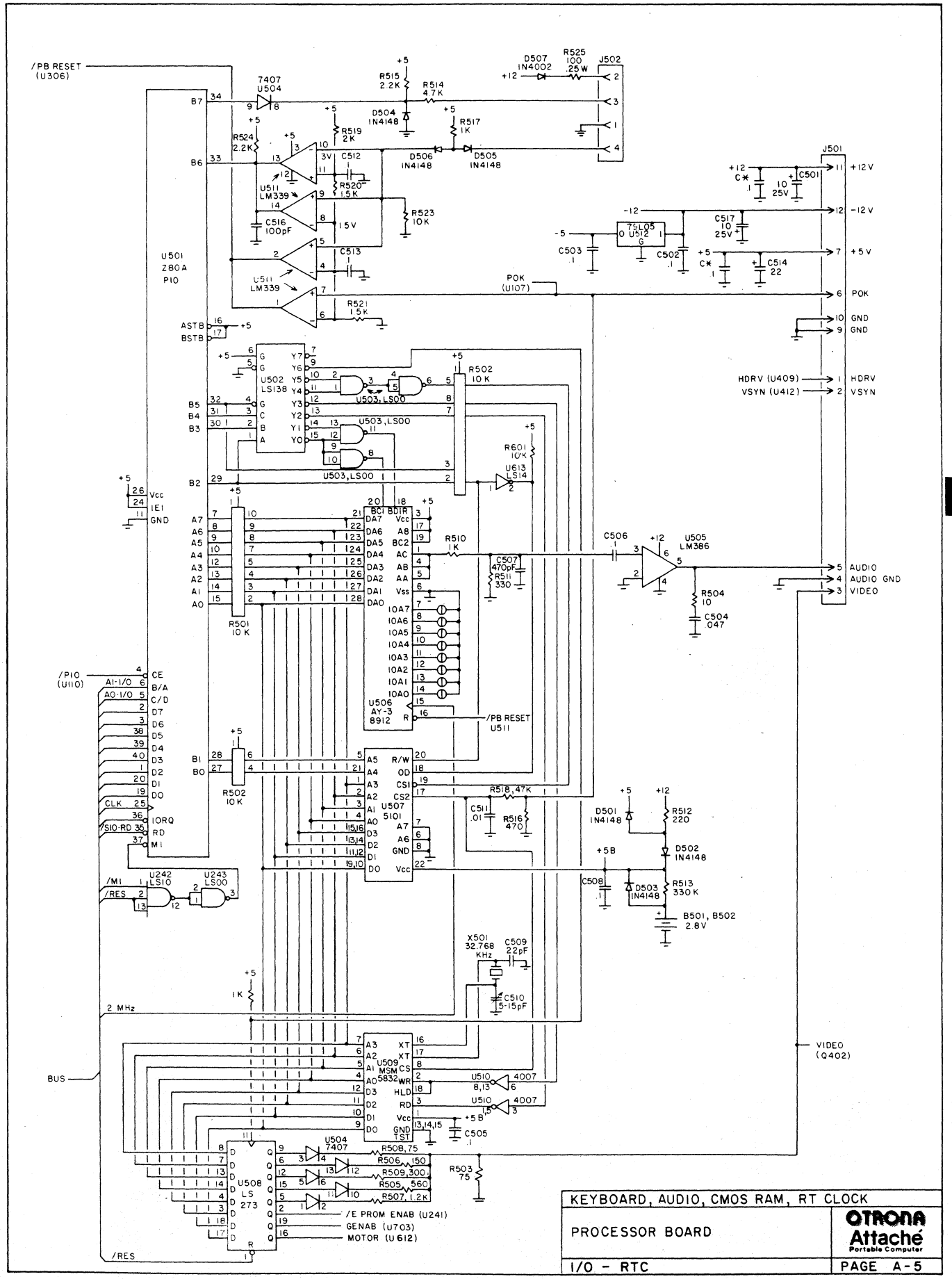
DISPLAY

PROCESSOR BOARD

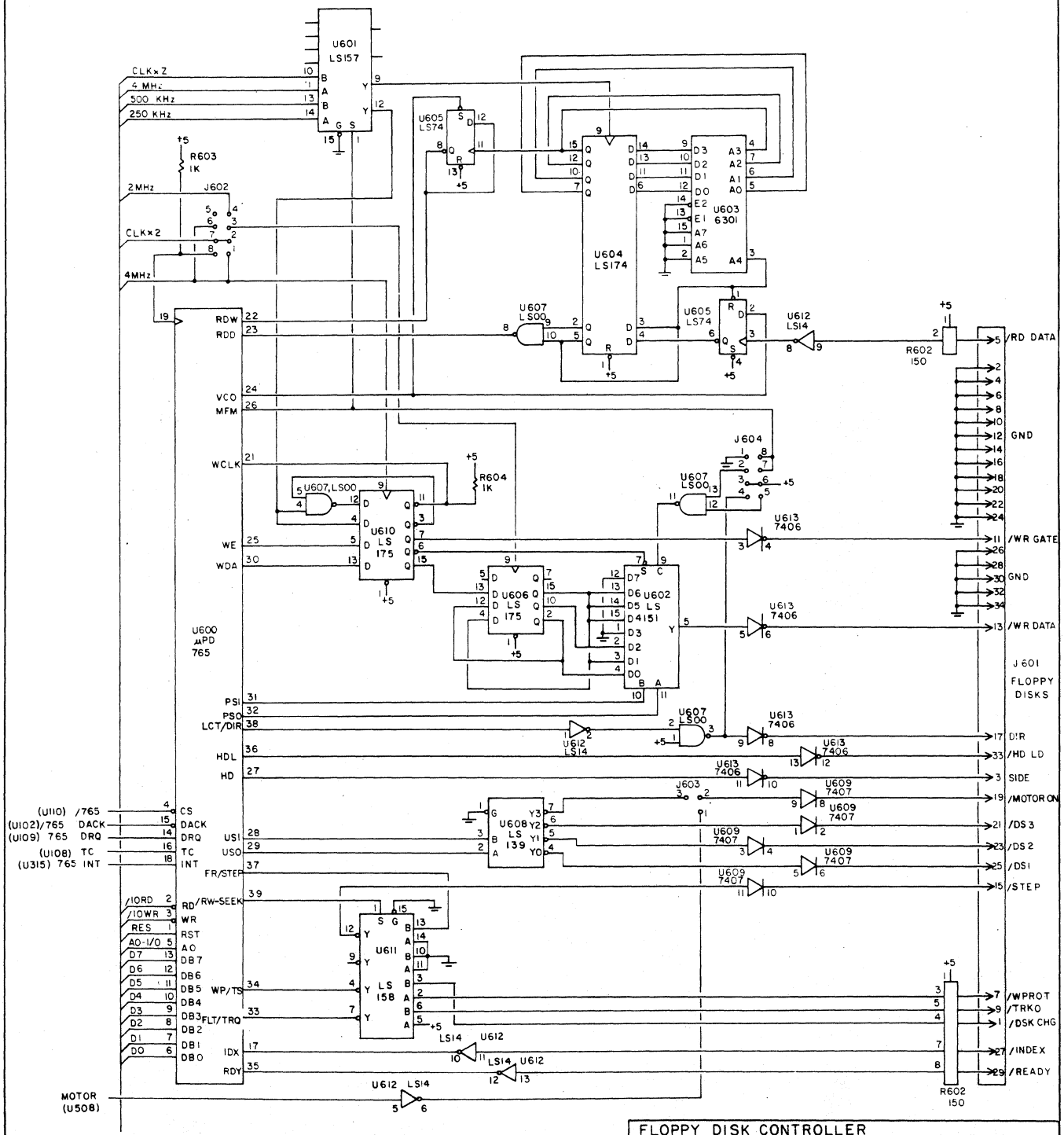
DISPLAY

OTRONA Attaché Portable Computer

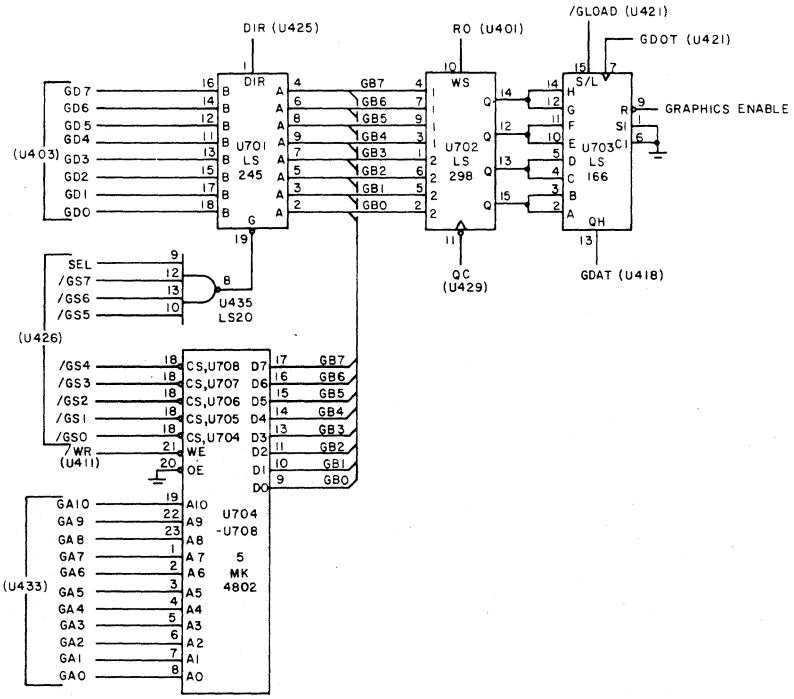
PAGE A-4



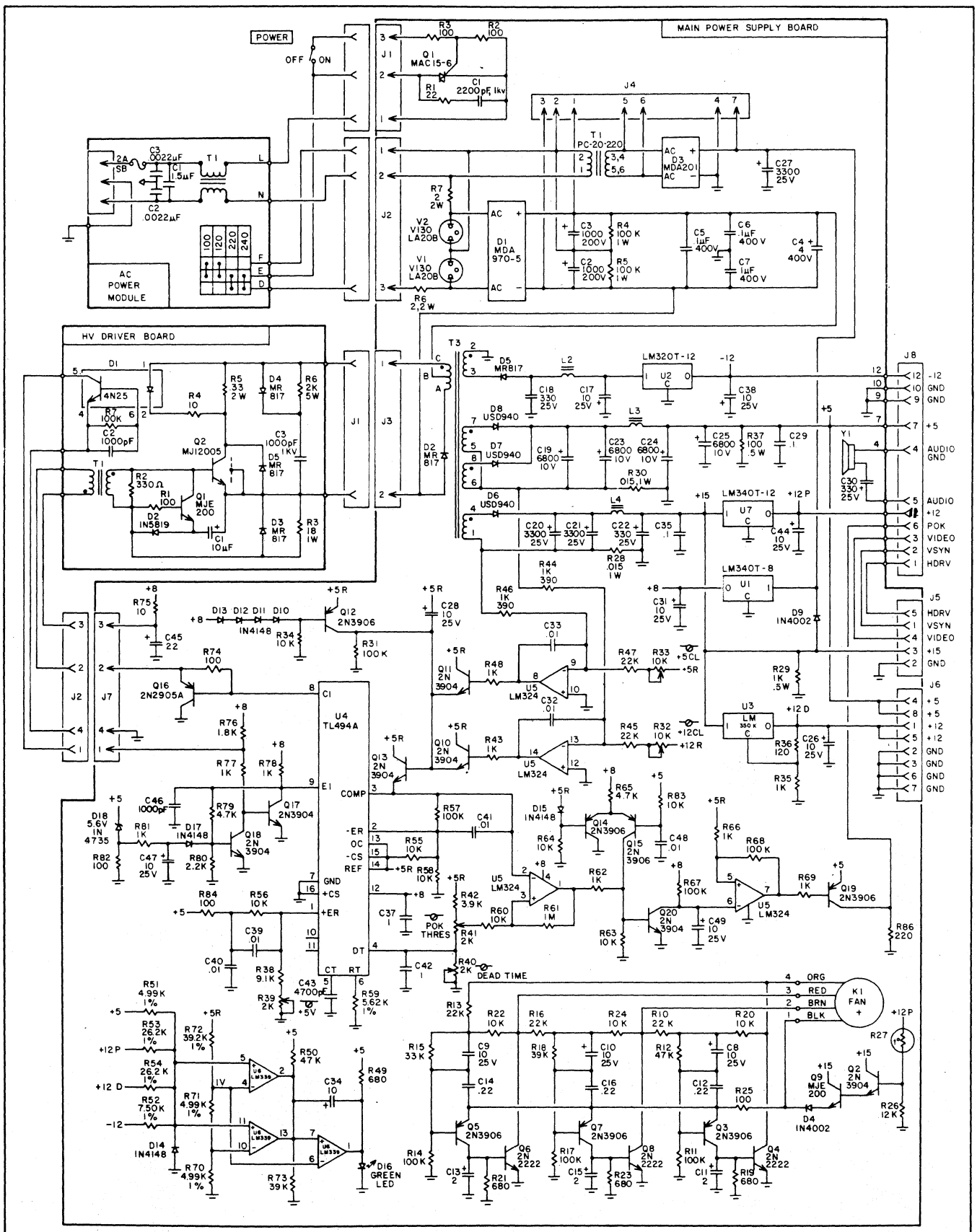
KEYBOARD, AUDIO, CMOS RAM, RT CLOCK	
PROCESSOR BOARD	OTRONA Attaché Portable Computer
I/O - RTC	PAGE A-5



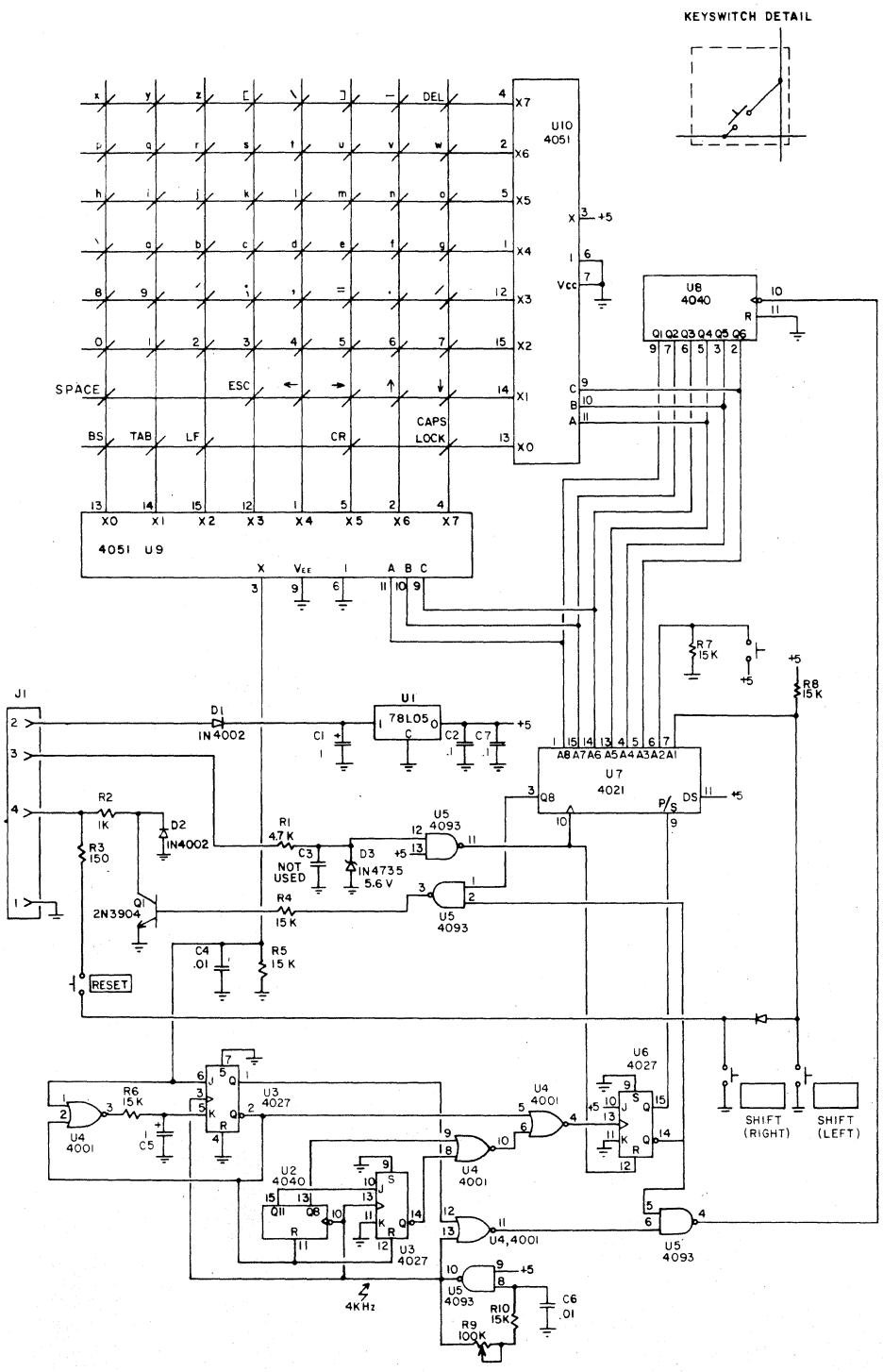
FLOPPY DISK CONTROLLER	
PROCESSOR BOARD	OTRONA Attaché Portable Computer
FLOPPY	PAGE A-6



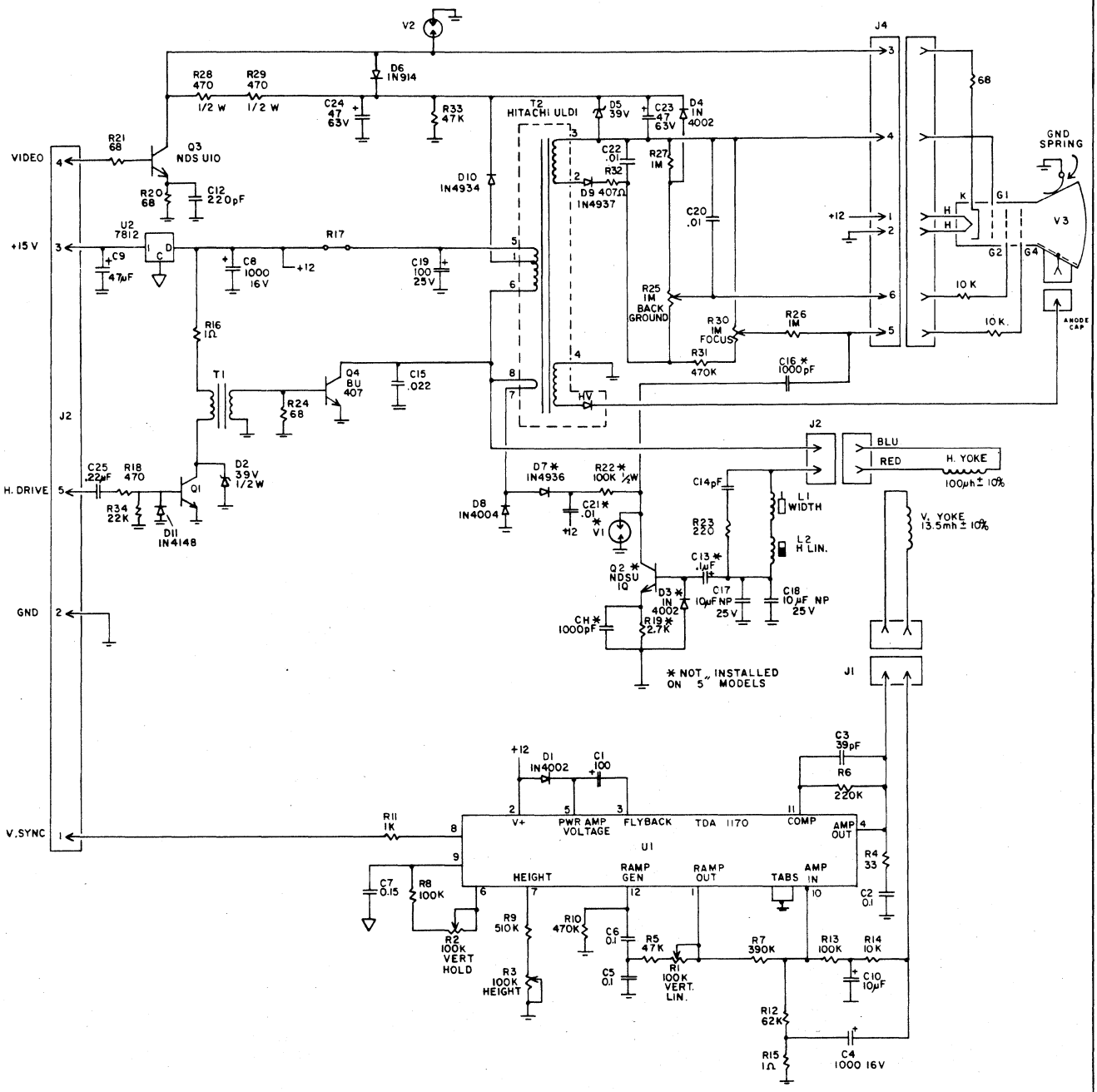
GRAPHICS OPTION	
PROCESSOR BOARD	OTRONA Attaché Portable Computer
GRAPHICS	PAGE A-7



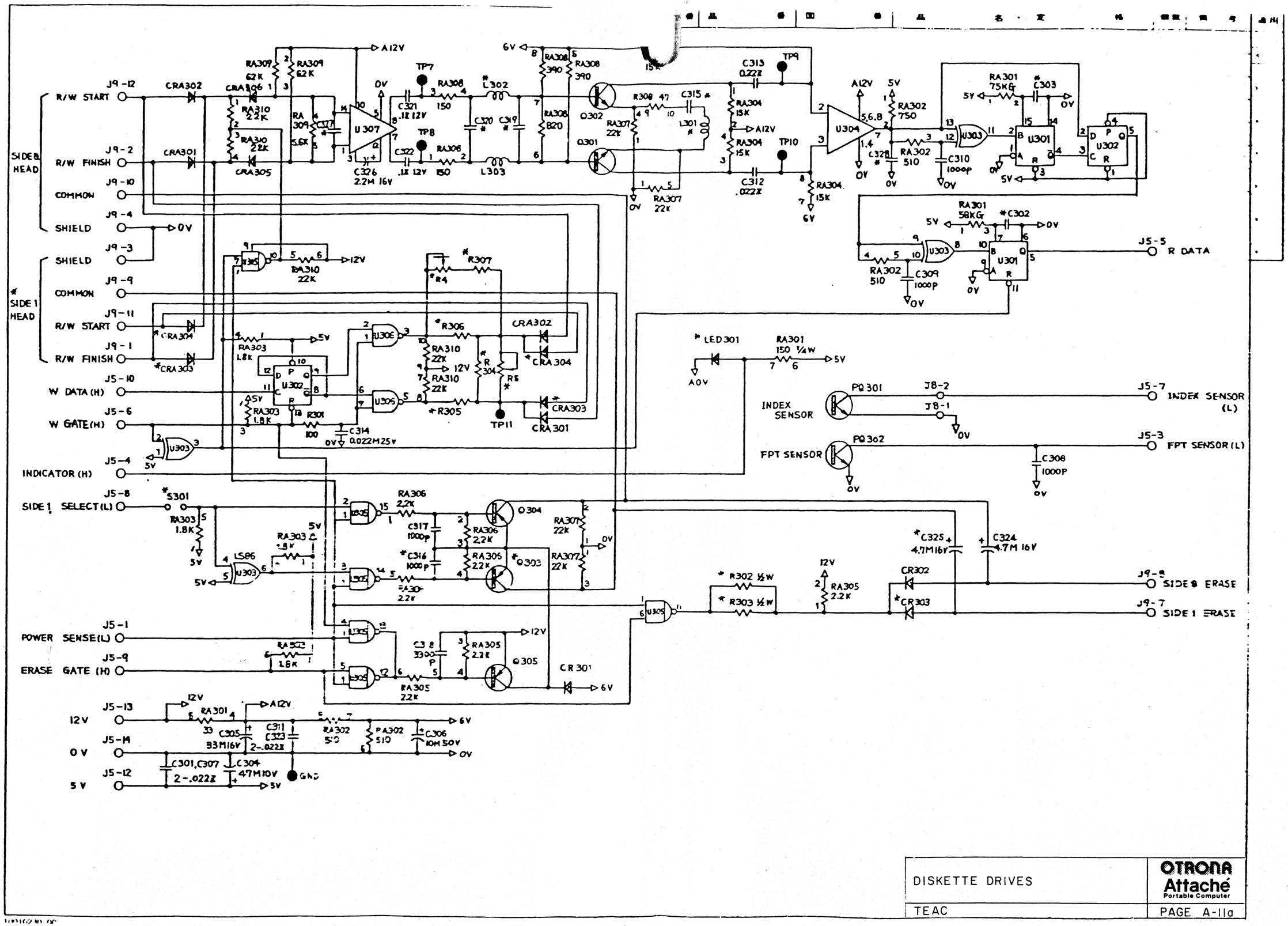
POWER SUPPLY	OTRONA Attaché Portable Computer
POWER SUPPLY	PAGE A-8



KEYBOARD	OTRONA Attaché Portable Computer
KEYBOARD	PAGE A-9

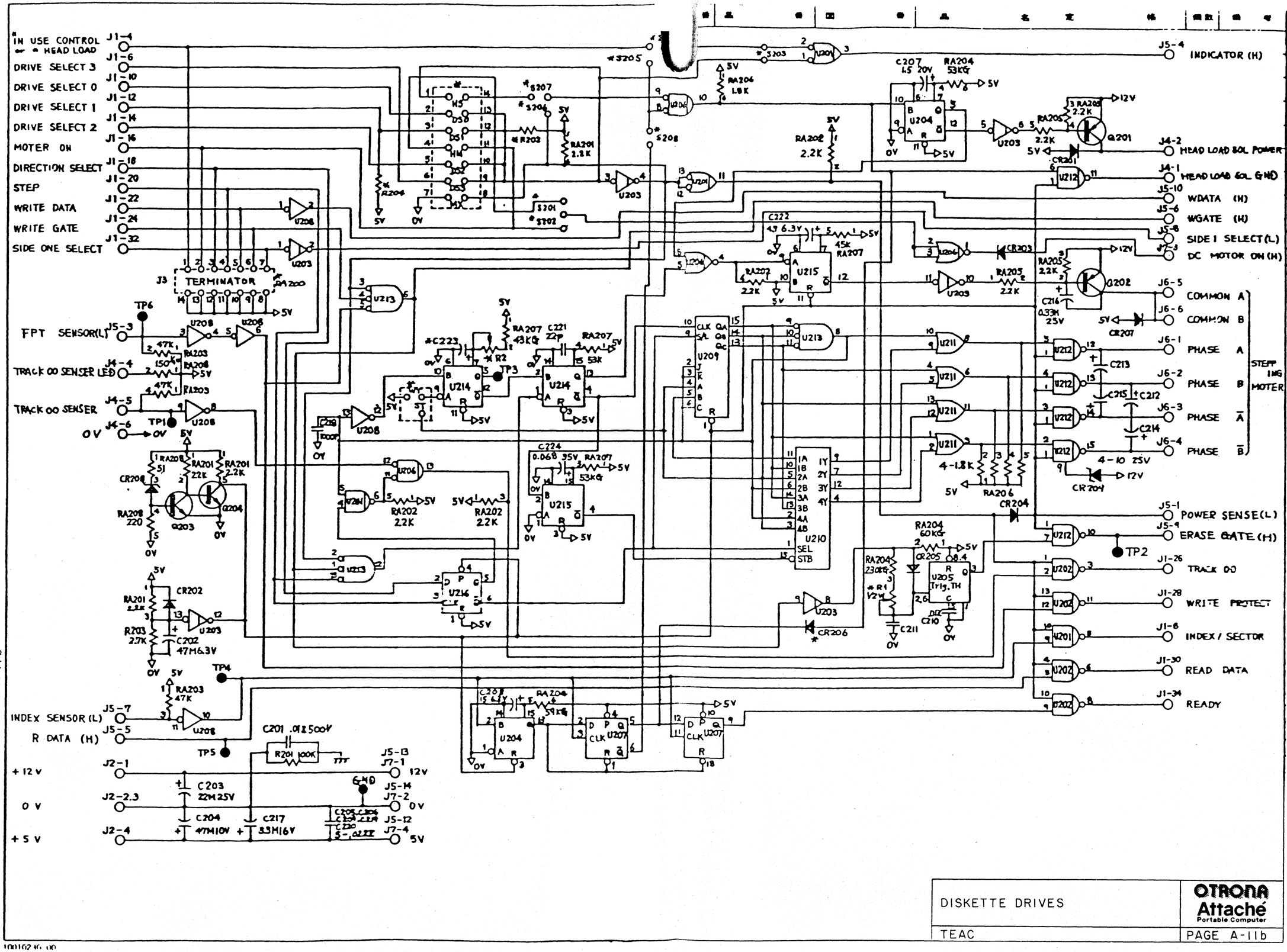


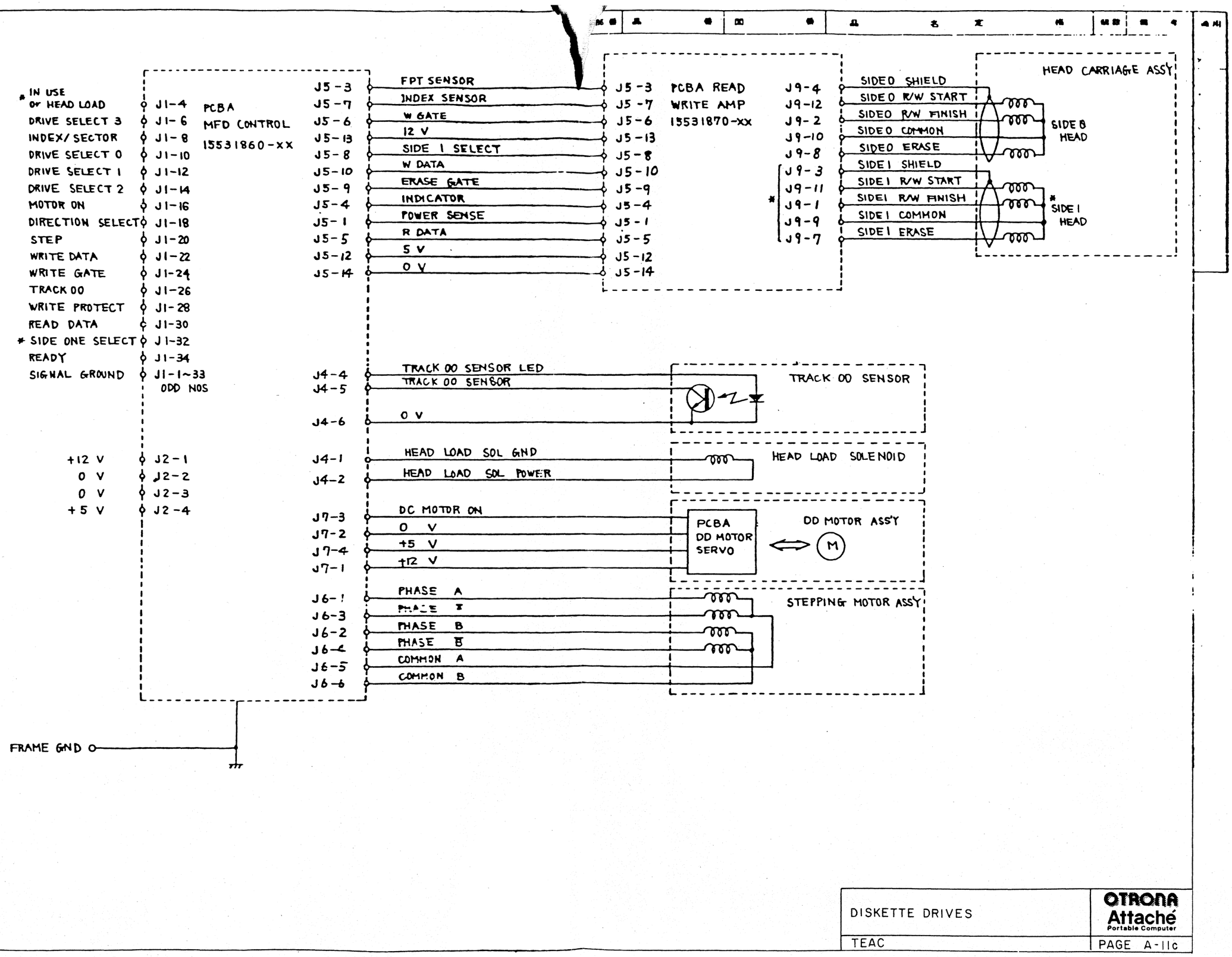
DISPLAY MODULE	OTRONA Attaché Portable Computer
DISPLAY MODULE	PAGE A-10



PAGE A-11a

DISKETTE DRIVES	OTRONA Attaché Portable Computer
TEAC	PAGE A-11a


IN USE CONTROL
HEAD LOAD
DRIVE SELECT 3
DRIVE SELECT 0
DRIVE SELECT 1
DRIVE SELECT 2
MOTER ON
DIRECTION SELECT
STEP
WRITE DATA
WRITE GATE
SIDE ONE SELECT
J1
J1-4
J1-6
J1-10
J1-12
J1-14
J1-16
J1-18
J1-20
J1-22
J1-24
J1-32
J3 TERMINATOR
RA200
FPT SENSOR(L)
J5-3
TRACK 00 SENSER LED
J4-4
TRACK 00 SENSER
J4-5
0V
J4-6
TP6
TP1
TP3
TP4
TP5
TP2
INDEX SENSOR(L)
J5-7
R DATA (H)
J5-5
+12 V
+5 V
J2-1
J2-2.3
J2-4
C203 22M25V
C204 47M10V
C217 33M16V
C201 .01 500V
R201 100K
J5-13
J7-1
12V
J5-14
J7-2
0V
J5-12
J7-4
5V
GND
INDICATOR (H)
J5-4
HEAD LOAD SOL POWER
J4-2
HEAD LOAD SOL GND
J4-1
WDATA (H)
J5-10
WGATE (H)
J5-6
SIDE 1 SELECT(L)
J5-8
DC MOTOR ON (H)
J5-3
COMMON A
J6-5
COMMON B
J6-6
PHASE A
J6-1
PHASE B
J6-2
PHASE Ā
J6-3
PHASE B̄
J6-4
STEPP IMG MOTER
POWER SENSE(L)
J5-1
ERASE GATE (H)
J5-9
TRACK 00
J1-26
WRITE PROTECT
J1-28
INDEX / SECTOR
J1-6
READ DATA
J1-30
READY
J1-34
U201
U202
U203
U204
U205 Trig.TH
U206
U207
U208
U209
U210 SEL STB
U211
U212
U213
U214
U215
U216
Q201
Q202
Q203
Q204
CR201
CR202
CR203
CR204
CR205
CR206
CR207
RA201 2.2K
RA202 2.2K
RA203 47K
RA204 53KΩ
RA205 2.2K
RA206 1.8K
RA207 45K
RA208 220
C202 47M6.3V
C207 4.5 20V
C211
C212
C213
C214
C215
C216 0.33M 25V
C221 22P
C222 4.7 6.3V
C223
C224 0.068 35V
C210
4-1.8K
4-10 25V
R1 V24
R2
R203 2.7K
TERMINATOR
DISKETTE DRIVES
TEAC
OTRONA Attaché Portable Computer
PAGE A-11b


* IN USE or HEAD LOAD
DRIVE SELECT 3
INDEX/SECTOR
DRIVE SELECT 0
DRIVE SELECT 1
DRIVE SELECT 2
MOTOR ON
DIRECTION SELECT
STEP
WRITE DATA
WRITE GATE
TRACK 00
WRITE PROTECT
READ DATA
* SIDE ONE SELECT
READY
SIGNAL GROUND
J1-4
J1-6
J1-8
J1-10
J1-12
J1-14
J1-16
J1-18
J1-20
J1-22
J1-24
J1-26
J1-28
J1-30
J1-32
J1-34
J1-1~33 ODD NOS
PCBA MFD CONTROL 15531860-xx
+12 V
0 V
0 V
+5 V
J2-1
J2-2
J2-3
J2-4
J5-3
J5-7
J5-6
J5-13
J5-8
J5-10
J5-9
J5-4
J5-1
J5-5
J5-12
J5-14
FPT SENSOR
INDEX SENSOR
W GATE
12 V
SIDE 1 SELECT
W DATA
ERASE GATE
INDICATOR
POWER SENSE
R DATA
5 V
0 V
J5-3
J5-7
J5-6
J5-13
J5-8
J5-10
J5-9
J5-4
J5-1
J5-5
J5-12
J5-14
PCBA READ WRITE AMP 15531870-xx
J9-4
J9-12
J9-2
J9-10
J9-8
J9-3
J9-11
* J9-1
J9-9
J9-7
SIDE0 SHIELD
SIDE0 R/W START
SIDE0 R/W FINISH
SIDE0 COMMON
SIDE0 ERASE
SIDE1 SHIELD
SIDE1 R/W START
SIDE1 R/W FINISH
SIDE1 COMMON
SIDE1 ERASE
HEAD CARRIAGE ASSY
SIDE 0 HEAD
* SIDE 1 HEAD
J4-4
J4-5
J4-6
TRACK 00 SENSOR LED
TRACK 00 SENSOR
0 V
TRACK 00 SENSOR
J4-1
J4-2
HEAD LOAD SOL GND
HEAD LOAD SOL POWER
HEAD LOAD SOLENOID
J7-3
J7-2
J7-4
J7-1
DC MOTOR ON
0 V
+5 V
+12 V
PCBA DD MOTOR SERVO
DD MOTOR ASS'Y
M
J6-1
J6-3
J6-2
J6-4
J6-5
J6-6
PHASE A
PHASE Ā
PHASE B
PHASE B̄
COMMON A
COMMON B
STEPPING MOTOR ASS'Y
FRAME GND

100102X0 00

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APPRVD
X	[illegible]	[illegible]	PILOT RELEASE	TA	[illegible]	[illegible]
X2	[illegible]	[illegible]	SEE ECO	TA	[illegible]	[illegible]

REVISION STATUS		
FAB	SCHEM	ASSY
X1	X1	X1
X1	X2	X2

DESC	LAST USED	NOT USED
RESISTOR	R19	
CAPACITOR	C27	C8
I.C.	U3	
TRANSISTOR	Q2	
ZENER	Z2	

P8
TACH +1 1
TACH -2 2
C23, 4.7µF 35V
R18 1K
C22 22µF 35V
C21 22µF 35V

UPC 1043C
PREAMP
SCHMITT TRIGGER
TIMING PULSE GEN
Z3
SAMPLE AND HOLD
SAWTOOTH WAVE GEN
DC SERVO AMP
POWER
C27 47000pf 50V
R19 270K
C24 .47µF 50V
R20 1M
C15 10,000pf 50V
C26 47µF 35V
C25 47µF, 35V
C19 33,000pf 50V
C20 1µF, 50V
R10 18K

P5
MOTOR ON *1 1
+12V 4 4
POWER GND 3 3
C1 220µF 16V
Q1 2SC2785
R14 3.9K
R13 1K
R4 470
R5 220
R6 330
R7 330
Q2 2N4401
R11 50K
R8 360K
R9 15K
C18 15,000pf 50V
VR2 RD 2.2EC
C16 2200pf 50V
C17 6800pf 50V

P8
HALL CURRENT SOURCE 12 12
HALL CURRENT RTN 13 13
R12 100
VR1 RD 2.2EC

HALL ELEMENTS
U+ 10 7
U- 11 6
V+ 5 11
V- 6 10
W+ 3 8
W- 4 9

HALL AMPLIFER
3Ø PULSE GEN
PRE-DRIVER
Z1 HA11714
FWD / REV CONTROL
CONTROL AMP
MOTOR CURRENT DETECTOR

HA11715
Z2
U PHASE DRIVER
V PHASE DRIVER
W PHASE DRIVER
FDBK AMP
C13 47000pf 50V
C12 47000pf 50V
C14 47000pf 50V
NPP REF
NPP SENSING
C11 1500pf 50V
C9 1500pf 50V
C10 1500pf 50V
R15
R16
R17

+12V
C5 4.7µF 35V
R1 100
C4 47µF 35V
C3 4.7µF 35V
R2 100
C2 47µF 35V
C7 4.7µF 35V
R3 100
C6 47µF 35V
P8
WINDING U
WINDING V
WINDING W

PAGE A-12a

DISKETTE DRIVES
REMEX
OTRONA Attaché Portable Computer
PAGE A-12a

1749620-001 X2

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APPR'D
			SHEET			

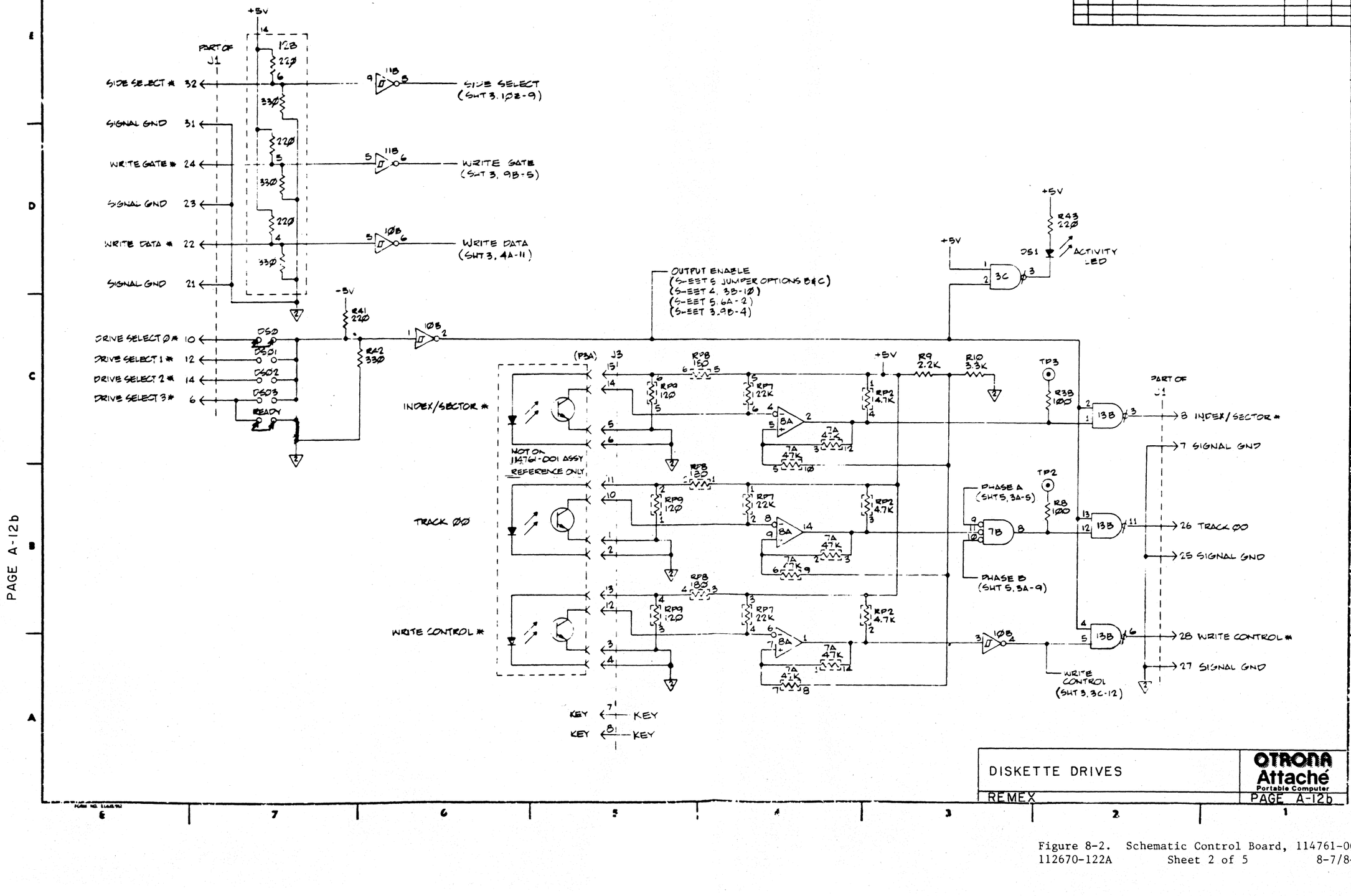


Figure 8-2. Schematic Control Board, 114761-001.
112670-122A Sheet 2 of 5 8-7/8-8

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APPRD
			SEE SH. ONE			

HEAD OUTPUT (A) (SHT 3, 7D-2)

R33 8.2K

HEAD OUTPUT (B) (SHT 3, 7D-5)

5D

TP8

C19 + 22/25V

L3 330

L3 B2

TP6

C17

C14 510pF ±5%

R28 1866 ±2%

TP7

C18 + 22/25V

L4 330

L2 B2

TP5

C24 .1 ±10%

+12VF

R32 1Ω

C25 .1

+5VF

R26 1Ω

R29 1Ω

C13 .1

R30 8.2K

C20 .1

R31 8.9K

C22 390pF ±5% 100V

C21 100pF ±5%

5D

TP4

R34 100

158

PART OF J1

→ 30

→ 29

READ DATA

TP9

OUTPUT ENABLE (SHT 2, 10B-2) (SHT 5, 6A-2) (SHT 3, 9B-4) (SHT 5, JUMPER OPTION B9C)

C16 1000 pF ±5%

R23 47Ω

L1 33

R24 50K 1/2W

CW

R27 10K

HEAD SHIELD (SHT 3, J6-5)

PAGE A-12c

DISKETTE DRIVES

REMEX

OTRONA Attaché Portable Computer

PAGE A-12c

DWG NO. 114762-001 REV K0

Figure 8-2. Schematic Control Board, 114761-001.
112670-122A Sheet 4 of 5 8-11/8-12

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APPRD
			SEE SHT 1			

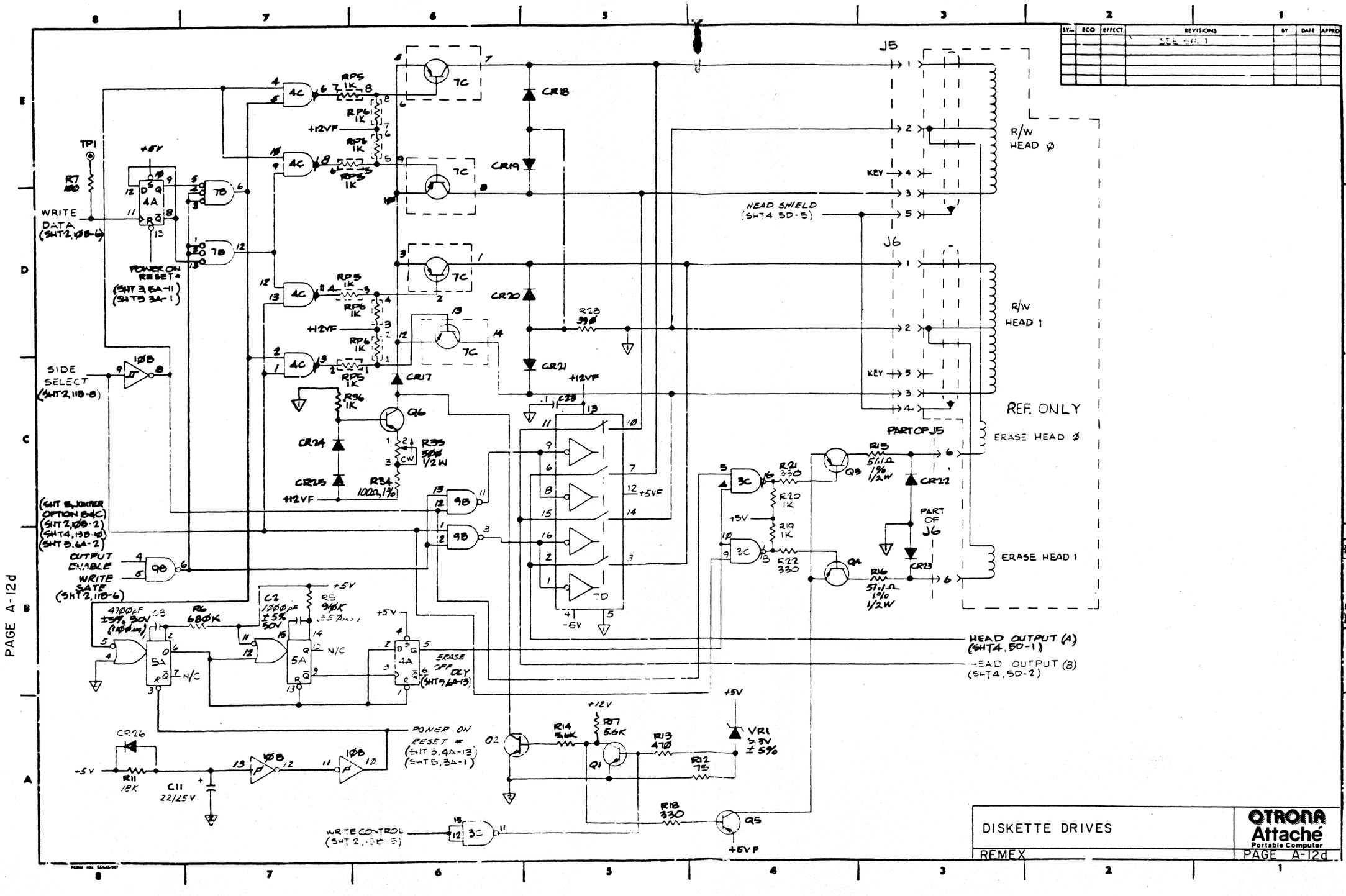


Figure 8-2. Schematic Control Board, 114761-001.
112670-122A Sheet 3 of 5 8-9/8-10

ITM	ECO	EFFECT	REVISIONS	BY	DATE	APPRD
			SEE SH. ONE			

PART OF J1

DIRECTION IN * 18
SIGNAL GND 17
STEP * 20
SIGNAL GND 19
OUTPUT ENABLE (SHT 2,10B-2) (SHT 4,13B-10) (SHT 3,9B-4) (SHT 5, JUMPER OPTION B&C)
POWER ON RESET * (S-T 3,5A-11) (SHT 3,4A-13)
ERASE OFF DELAY (SHT 3,4A-6)
PHASE B (SHT 2,7B-10)
PHASE A (SHT 2,7B-9)

J2

+12V 1
PWR GND 2, 3
+5V 4
PART OF J1
MOTOR ON * 16
SIG GND 15
(SHT 3 9B-4)(SHT 4 13B-10) (SHT 2,10B-2)(SHT 5, 6A-2) OUTPUT ENABLE

J3

17 MOTOR ON *
9 +12V
18 PWR GND

J4

+12V 6
5 STEPPER DRIVER SUPPLY
9 PHASE 1
10
1 PHASE 2
2
STEPPER MOTOR COILS
N/C 4 N/C
KEY 3 KEY
8 N/C

PAGE A-12e

DISKETTE DRIVES

REMEX

OTRONA Attaché Portable Computer

PAGE A-12e

114762-001

Figure 8-2. Schematic Control Board, 114761-001.
112670-122A Sheet 5 of 5 8-13/8-14

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List of Acronyms

AC	Alternating Current
ASCII	American Standard Code for Information Interchange
BASIC	Beginner's All-purpose Symbolic Instruction Set
BDOS	Basic Disk Operating System
BIOS	Basic Input Output System
CCP	Console Command Processor
CTC	Counter Timer Circuit
CMOS RAM	Complementary Metal-Oxide Semi-conductor Random Access Memory
CP/M	Control Program for Microcomputers
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CRT	Cathode Ray Tube
DC	Direct Current
DCE	Data Communication Equipment
DMA	Direct Memory Access
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EPROM	Erasable Programmable Read-Only Memory
FDC	Floppy Disk Controller
FM	Frequency Modulation
IEI	Interrupt Enable Input
IEO	Interrupt Enable Output
IC	Integrated Circuit
I/O	Input/Output
LED	Light-Emitting Diode
LPT	Line Printer
MFM	Modified Frequency Modulation
MODEM	MOdulator - DEModulator
NAND	Not AND
NMI	Non-Masked Interrupt
NOR	Not OR
PC	Printed Circuit
PIO	Parallel Input/Output
POK	Power Okay
PROM	Programmable Read-Only Memory
PWM	Pulse Width Modulator
RAM	Random Access Memory
ROM	Read-Only Memory
RAS/CAS	Row Address Strobe/Column Address Strobe
ROM	Read Only Memory
RTC	Real Time Clock
RTS	Request To Send
R/W	Read/Write
RxD	Receive Data
SDLC	Standard Data Link Control
SIO	Serial Input/Output
TPA	Transient Program Area
TTY	Tele-Type device
TxD	Transmit Data

Glossary

Access Time — The length of time between an enable pulse and valid output.

Adder — A device which outputs the sum of two or more binary number inputs.

Address — A group of bits that identify a specific memory location or I/O device.

Address Bus — A unidirectional bus over which digital information identifies a specific memory location or I/O device.

Address Mark — Flag bytes on a disk cylinder which signify that the data which follows as either an address (ID Address Mark) or data (Data Address Mark).

Address Translation — The transparent process of transforming one address into another.

Addressing — The process of identifying a device or memory location.

Amplifier — A device which increases the size of its input signal.

A-to-D Converter — A circuit that translates analog voltage or current changes into digital (high state or low state) output.

AND Gate — A circuit with two or more inputs and a single output, in which the output is high only when all inputs are high, and the output is low when any input is low.

ASCII Code — The American Standard Code for Information Interchange. A seven bit code which represents alphanumeric characters.

Asynchronous Comm. — A method of transmitting data in which the timing of the characters is not critical. The transmitted characters are enclosed in start and stop bit pairs.

Attributes — Features such as underline, boldface, subscript, superscript, reverse video, and highlighting that may be activated for characters that are displayed or printed.

BASIC-80 — Microsoft's BASIC programming language.

Battery Pack — An auxiliary unit for Attache which provides power to the components when conventional AC power is not available.

Baud Rate — The number of bits per second transmitted between two electronic devices.

BDOS — Basic Disk Operating System. The part of Attache's operating system which handles all I/O, especially disk I/O, at a logical level.

Bias — A voltage applied to a transistor to establish an operational voltage reference level.

Binary — A numbering system using a base number of two, using the digits 0 and 1.

Binary Counter — An interconnection of flip-flops with a single input to permit binary counting. The counter changes state with each input pulse and tabulates the number of input pulses.

BIOS — Basic Input/Output System. The part of Attache's operation system which defines the system's hardware to the remaining portions of the operating system.

Bit — An abbreviation for binary digit which designates one binary value or binary decision.

Bit Shift — A distortion on diskettes due to the magnetic effects of the media in which data pulses attract, and consequentially, shift from their location when initially recorded.

Blanking Pulse — A pulse sent to the display module from the CRT controller which times the display beam's retrace and keeps the retrace from becoming visible.

Blocking — The process of defining the beginning and ending boundaries of a unit of information to the physical device.

Bootstrap — The loading of CP/M programs and/or execution of diagnostics that occur when Attache is powered up, reset, or when **CTRL C** is executed from A>. Also known as "Booting" or "Rebooting".

Breakdown — The state in which a device, such as a diode, fails to act as an insulator and, instead, permits current flow.

Break Key — The **CTRL** and **LINE FEED** pressed simultaneously. This emits a high signal output to the communications port.

Bridge Rectifier — Part of the power supply circuitry which converts AC to DC such that the AC input may be either 110 or 220 volts.

Buffer — A digital circuit element which handles several inputs and can: delay them, supply additional drive, invert the output values, and match impedances with other digital elements.

Bus — A path over which digital information is transferred from a computer source to a computer destination. Only one transfer of information can take place at any one time on the bus.

Byte — A unit of information composed of eight contiguous bits.

Capacitor — A device consisting of two conduction surfaces separated by an insulating material. The capacitor stores direct current, and permits the flow of alternating current.

Cascade Mode — A DMA mode of operation which allows system expansion by connecting device signals such that the first device's output connects to the next device's input.

CBOOT — The name of an Attache BIOS routine which sets up the system.

CCP — Console Command Processor. Part of Attache's operating system which provides the initial user interface to the software.

Central Processing Unit — A single chip that performs data transfer, control, input/output and logical instructions by executing instructions obtained from memory.

Channel — A path along which signals can be sent.

Character Cell — The space which one normal size character occupies on the screen, equal to 8 dots wide by 10 scans high.

Character Set — The specific language or character coding which Attache is programmed to display or print.

Chip — A small piece of semiconductor material on which electronic components are etched to form circuits.

Chip Enable — The primary device selection pin.

Clock — Any device which generates one or more clock pulses. It serves to control the timing of clocked logic devices and to regulate their operating speed.

Clock Input — The terminal on a flip-flop whose condition controls the data flow. The clock permits data signals to enter the flip-flop, and then directs the flip-flop to change states accordingly.

Clock Pulse — One complete logic cycle from low to high and back to low, or high to low and back to high.

CMOS RAM — Complementary Metal-Oxide Semiconductor Random Access Memory. An Attache chip driven by a battery which stores system parameters until the user changes the parameters.

Cold Boot — The bootstrap operation that occurs when Attache is powered up or when **RESET** and the right **SHIFT** keys are pressed simultaneously.

Communications — The transmission of data from one electronic device to another.

Communications Port — The connector on the back of Attache for attaching a cable to communicate with another electronic device.

Comparator — A device which samples an input voltage and compares it to a reference voltage to produce a compensating error voltage.

Composite Signal — Another name for external video. The signal to the display module which contains the video, blanking pulses, and sync signals.

Console — The keyboard and the display screen.

Control Character Code — Program code used to address the display driver.

Control Latch — An Attache chip which controls video intensity, enables the EPROM, enables graphics, and controls the disk drives' motors.

Counter — A device capable of changing states in a specified sequence. The output of the counter indicates the number of pulses received.

Counter Timer Circuit — A chip in Attache which generates the clocks for the ports' baud rates, and which assigns interrupt priorities and vectors for floppy and 60 Hz interrupts.

CP/M — The operating system used by Attache.

CPU	See Central Processing Unit.
Cross-Talk	Signal interference between two tracks of data on a diskette.
CRT	Cathode Ray Tube, which is the display screen.
Crystal	An element which emits clock pulses.
CTC	See Counter Timer Circuit.
Cursor	The movable, highlighted rectangle on the display screen that indicates the current typing position.
Cycle Time	The interval between input and output of a device.
Cyclic Redundancy Check	An error checking method on diskette whereby a character is generated when data is written which must match when the data is read back, or an error is detected.
Daisy Chain	A method of connecting devices such that one device's input is tied to the next device's output.
Data	A general term for digital information which can be processed by a computer.
Data Bus	A path in which digital information is transferred.
Deblocking	The process which inputs a physical block and outputs a logical block.
Debugging	The process of removing errors from a computer program.
Differential Signal	A signal derived from the differences between two input signals. The input signals to a differential circuit are often complementary signals, so the differential signal is line noise.
Digital	A mode of operation which uses two-state (binary) information.
Diode	A two-electrode semiconductor device which passes current in one flow direction only.
Disk Cycle	A one byte location in BIOS where the current status of the disk operation is stored.

Diskette	A small flexible magnetic medium where computerized information is stored; also known as "floppy" disk.
Display	A device that offers visual presentations from an electronic signal.
DMA	Direct Memory Access controller. A chip which performs high-speed data transfers.
Dot Clock	The clock in the display section of the processor board whose pulse is the amount of time required to write on dot on the screen.
Driver	A digital circuit element coupled to the output of a circuit to increase the power or current-handling capabilities of that circuit.
DTR	Data Terminal Ready. The signal output from a system to notify the communicating device it is ready for data transfers.
Dump	To transfer the contents of memory to the display screen or the printer.
Dynamic RAM	A method of capacitive data storage which requires periodic refreshes to maintain the integrity of the data.
Electron Beam	A narrow stream of electrons moving in the same direction under control of a magnetic field.
(to) Enable	Permit the passage of a digital signal into or through a digital device or circuit.
EPROM	Erasable Programmable Read Only Memory. The storage chips within Attache which contain memory burnt in to the chip.
Error Voltage	A voltage used to correct an under- or over-voltage condition.
Escape Codes	Program codes used to address the display driver.
Exclusive-OR Gate	A binary circuit with two inputs and a single output, in which the output is high when the inputs are at different logic levels, and low if both inputs are at the same logic levels.
Expansion Connector	A connector in Attache which may be used to attach additional boards to the system.
External Video	A signal which contains all of the information necessary to generate the display; the data, the cursor location, and sync pulses.

File Control Block — A data structure in memory used for keeping track of files in use.

Flip-flop — A circuit having two stable states and the capability to change states upon receipt of a control signal, and remain in that state after the signal is removed.

Floppy — Another name for diskette.

Flyback — A type of transformer capable of handling large AC voltages.

Format — The process of preparing new diskettes for use with Attache.

Frequency Modulation — Method of single-density diskette storage where one data pulse occur between two clock pulses.

Gain — The degree of amplification a signal receives from an amplifying device.

Gap — The absence of information for a specified distance on magnetic diskettes.

Gate (logic device) — A binary circuit with two or more inputs and one output, the output of which is determined by the input combination.

Gate (gating device) — A circuit having two or more inputs and one output. One input can be defined as data, the remaining inputs as gating inputs to determine whether or not the input data can appear at the output.

(to) Gate — To control the passage of a digital signal through a circuit.

Gate Pulse — A pulse that enables a gated circuit to pass a signal.

Graphics — Display of data in shapes and drawings.

Hardware — The physical equipment that forms a computer system.

Head — An electromagnetic device used in magnetic media recording to convert a signal to a magnetic pattern, and vice versa.

Hertz — A unit of frequency equal to one cycle per second.

Hexadecimal — A numbering system which uses base 16, which uses the numbers 0 - 9, and letters A - F.

High Signal — A voltage greater than +2.4 volts.

Home — Placement of the cursor in the upper left-hand corner of the display screen.

Increment — To increase the value of a binary unit by one.

Index — A small hole in the diskette used a location reference point on the diskette.

Input/Output Device — The equipment used to transfer data to or from a computer.

Instruction — A set of characters which define an operation and which cause the computer to perform that operation.

Integrated Circuit — An electronic circuit contained within a single chip.

Internal CRT — The signal to the display module which contains video, sync pulses, and blanking pulses.

Interrupt — A break in normal execution which indicates that the external interrupting device requires service or use of the system bus.

Interrupt Routine — A software subroutine designed to service an interrupting device.

Inverter — A digital device which outputs the opposite (or complement) state of the input.

Jump — A software instruction which controls the transfer of operations from one point in the software to another.

Latch — A simple logic storage element used to retain its logic state after input signal removal.

LED — A diode which glows as it passes current.

LINE FEED Key — A key used for indicating the end of a line during program editing, but not used for word processing. **LINE FEED** can be used in conjunction with **CTRL** to generate a high signal on the communication port.

Linear — Having an output which varies in direct proportion to input.

List — The logical level term for a printer.

Local Device — The I/O device attached to Attache's printer port, usually the printer.

Logical Level — The definitions of information units and devices according to the software other than BIOS.

Low Level — Voltage less than +.8 volts.

Machine Cycle — A period of time during which a related group of actions occurs within the microprocessor chip.

Mapping — A transformation from one memory location to another.

Matrix — A data structure that groups characters or integers into a rectangular array.

Memory — Any device that can store logic states such that bits can be accessed and retrieved.

Memory Address — The location of a byte within storage.

MFM — See Modified Frequency Modulation.

Microcomputer — A fully operational digital computer based upon a microprocessor chip or chip family.

Mode — One of a computer's operating states which provide the means for keyboard multi-functions and other tasks where internal interpretations depend upon the operating state currently active.

Modem — Modulation/Demodulation. A device which allows computers to communicate over telephone wires by converting data pulses to tones and vice versa.

Modified Frequency Modulation — A method of double-density diskette data storage which writes clock pulses on the medium only between two 0's of data. The clock is later resynthesized.

Modifier Keys — The **CTRL** and **SHIFT** keys, which are used alone or together in conjunction with the multi-function keys, arrow keys, or **DEL** key to perform a variety of tasks.

Monitor — A large screen which may be connected to Attache via the RCA jack at the back of the system.

Monitor Mode — The operating state Attache enters from Terminal Emulation mode if the **CTRL** and **LINE FEED** keys are pressed simultaneously. Monitor mode contains system diagnostics.

Multi-Function Keys — Keys on the top row of the keyboard that have capabilities in addition to normal upper and lower case when used in conjunction with one or more keyboard modifier keys.

Multiplexer — A digital device that can select one of a number of inputs and pass the state of that input.

Multiplexing — A method of data transmission whereby the same signal lines are used to transmit data of two or more meanings by gating the data's storage device.

NAND Gate — A binary circuit with two or more inputs and one output. The output is low if all inputs are high, and high if any input is low.

Nanosecond — One billionth of a second.

Noise — Any unwanted signal or disturbance which modifies the transmitting or recording of data.

Non-Masked Interrupt — An immediate, urgent interruption to the processor, such as a system power off.

NOR Gate — A binary circuit in which the output is low if any input is high, and high only if all the inputs are low.

Nybble — Half of a byte. For example, byte "1E" contains two nybbles, "1" and "E".

Operating System — The set of programs that run the computer hardware and interpret software commands. Attache uses an enhanced version on the CP/M operating system.

OR Gate — A binary circuit with two or more inputs in which the output is high if any input is high, and low if all the inputs are low.

Oscillator — A source of alternating current, sustained by a transistor.

Page — A segment of 256 consecutive bytes.

Parallel I/O — A dual-port chip which provides direct interface between the CPU and the keyboard, the control latch, the sound generator, and CMOS RAM.

Parity Bit — A binary bit appended to a group of bits to make the sum of all the bits always even or always odd.

Patch — To change a circuit or a routine.

Peripheral Device — An auxiliary machine which may be controlled by the computer.

Physical Level — The definitions for devices and units of information according to BIOS.

PIO — See Parallel I/O.

Pipelining — A technique for speeding up a computer by performing operations concurrently; staggering and overlapping sequential operations.

Pixel — An abbreviation for picture element. A small, rectangular division of the video screen.

Pointer — Two bytes (a word) giving the address of another memory location.

Polarity — The difference between two points with respect to charge, negative or positive.

Polling — A periodic checking of Input/Output devices to determine their condition or status.

Port — The connectors on the back of Attache for attachment of printer or communication cables.

Precompensation — Circuitry in the floppy disk section of the processor which corrects for bit shift distortion by making allowances at the time of data recording.

Printer Port — The connector on back of Attache for attaching a cable to transmit data to a printer.

Priority Interrupts — An ordering of interrupts by degree of importance so that some interrupting devices take precedence over others.

Pulse Width Modulator — A control circuit which functions by controlling the width of its output pulse.

Punch — The communications port as defined by BDOS.

Random Access Memory — A semiconductor memory into which high or low states can be written (stored) and later retrieved.

RAS/CAS — Row Address Strobe/Column Address Strobe. A clock in RAM which divides memory addresses into columns and rows.

Read — To transmit data from a specific memory device or location to another device.

Reader — The keyboard and display as defined by BDOS.

Read-Only Memory — A semiconductor memory from which data can be repeatedly read out, but whose data has been permanently written into the chip during construction.

Real-Time Clock — A device that provides interrupts at regular time intervals to maintain an accurate time of day clock and to measure elapsed time.

Recalibrate — A diskette handling process in which the head returns to track zero, either as a means of determining head location, or during system boot.

Record — A collection of related fields, such as fields which describe a single inventory item.

(to) Record — To write data on a diskette.

Rectify — To convert AC into DC.

Refreshing — A process of constantly reactivating information that decays when left idle.

Register — A short-term digital storage circuit. The storage capacity of a register is usually one byte.

Reset — An asynchronous input used to control the logic state of a flip-flop's output.

Resistor — A device which introduces a specified impedance (resistance) to current

Retrace — The motion of the CRT beam when the beam returns, as opposed to when it writes on the screen.

Reverse Video — A screen attribute in which characters are dark, and the background is bright.

Scan — One left-to-right horizontal motion of the display screen's beam.

Screenful — The number of text lines on the screen display at one time.

Scrolling — The function that "rolls" lines of text or entire "screenfuls" of text up or down on the screen.

Sectors — Locations of a specific size on a diskette where data is stored. Attache uses diskettes with ten sectors per track.

Semiconductor — A material with electrical conductivity capabilities between that of metal or an insulator.

Sensor — A device whose input measures some external physical occurrence, and whose output can be read by a computer.

Serial I/O — A dual-channel device which provides interface between the processor and peripheral devices connected to the ports.

Servo System — An automatic control circuit which compares actual values to desired values and adjusts its control element accordingly.

Set-up Mode — An operating state used for setting or changing screen brightness, keyboard click sounds, volume level, baud rates, etc.

Shift Keys — Used for activating upper case as on a typewriter, and as modifier keys when used in conjunction with other multi-function keys.

Shift Register — A register in which stored data can be serially output.

Shunt — A resistor placed in parallel with a device to provide electrical protection.

Single Transfer Mode — A DMA operating state which performs one data transfer at a time.

SIO — See Serial I/O.

Snubber — A circuit which protects transistor from damage due to excessive current or voltage.

Software — The sum of programs and routines used to extend the capabilities of the computer.

Spindle — The mechanism which turns the diskette.

State Machine — A circuit within the floppy section of the processor board which separates data pulses from clock pulses during diskette reads.

Stepper Motor — A motor which rotates by a fixed amount each time it receives a pulse.

(to) Strobe — To activate a digital circuit.

Switching Supply — A power supply which uses semiconductors alternately in on or off states to produce high frequency AC before its final rectification.

Synchronize — To lock one element of a system into step with another.

Synchronous — Operation of a clocked logic system wherein all actions take place in synchronization with the clock, or operation of two systems in step.

System — The necessary hardware and software for a functionally complete computer.

Teletype — The communications port device as defined to BIOS.

Terminal — A device connected to or part of a computer which allows user interface and which contains a keyboard and a display.

Terminal Emulation — An operating state in which Attache functions as a computer terminal.

Thermistor — A digital component having resistance that varies with temperature.

Threshold — The current or voltage limit which will cause the device to breakdown if surpassed.

TIME — A utility program that sets the time and date.

TPA — See Transient Program Area.

Track 0 — The outermost track on which the boot routine resides.

Transformer — A coil whose primary to secondary coil ratios determine the output voltage.

Transient Program — A software program which is not permanently in memory, such as a user program.

Transient Program Area — A part of Attache's operating system in which transient programs reside.

Transistor — A solid-state device made from semiconductor materials which can act as electrical insulators or conductors, depending on the input charges.

Trigger — A pulse which starts an action.

Tri-state Device — A logic device that has a high impedance state in addition to high and low states. In the high impedance state output is not changed.

Tunnel Erase — A diskette handling process in which portions of the head are staggered on opposite sides of the diskette track to eliminate excessive pulse amplitudes.

Valet — An Attache software package which allows all processing to be interrupted to perform functions such as mathematical calculations.

Vectored Interrupt — Each device points (vectors) the computer's control to a specific software service routine for that interrupting device.

Video Signal — The part of the composite sync signal which controls beam intensity.

Virtual Memory — Translated memory locations after the mapping process.

Wait State — The state a device enters when a synchronizing signal is not present.

Warm Boot — Bootstrap operation that occurs when **CTRL** and **C** are pressed at the same time while the cursor is at A>.

Window — A pulse used to discriminate data pulses by ensuring that the data pulse occurs within the window pulse.

Word — Two contiguous bytes.

WordStar — A word processing package for microcomputers of which Attache uses an enhanced version.

Word Wrap — A word processing function that moves the cursor and the word being typed to the next line when the right margin is encroached during text entry.

Write — To transmit data from another device or memory location into a specific memory location or medium.

Write Protect — A notch in the diskette jacket which, when covered, keeps the diskette data from being overwritten.

Yoke — The tapered portion of the display module furthest from the screen which contains the deflection coils.

Zener Diode — A diode characterized by a sharp reverse current at a certain negative potential (breakdown).

Index