MOTOROLA

M68KVSWIN/D1

VME/10
Microcomputer System
Winchester Disk Controller
User's Manual

MICROSYSTEMS

QUALITY • PEOPLE • PERFORMANCE

M68KVSWIN/D1

JANUARY 1984

VME/10

MICROCOMPUTER SYSTEM

WINCHESTER DISK CONTROLLER

USER'S MANUAL

First Edition

PREFACE

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on a high to low transition.

Refer to the VME/10 Microcomputer System Equipment Manual, publication number M68KVSEM, for all external signal and power wiring information to the Winchester Disk Controller (WDC).

TABLE OF CONTENTS

TABLE OF CONTENTS (cont'd)

LIST OF ILLUSTRATIONS

LIST OF TABLES

CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, hardware configuration, operation, functional description, and support information for the M68RWIN1 Winchester Disk Controller (WDC).

1.2 SPECIFICATIONS

The WDC specifications are identified in Table 1-1.

1.3 GENERAL DESCRIPTION

The WDC is an intelligent interface between the VME/10 I/O Channel and the Winchester disk drive and floppy disk drive.

The WDC performs high-level commands such as read/write data, format track, verify data, etc., and includes implied seeks, automatic track/head switching, alternate sectoring, and error checking. Data is sent between the VME/10 and the WDC through interrupt-initiated block transfers, interrupt-initiated byte transfers, or by processor polling.

TABLE 1-1. WDC Specifications

CHARACTERISTICS	SPECIFICATIONS
Microcontroller	Signetics 8X305
Clock signal	Crystal controlled 16.0 MHz and 8.0 MHz
Interrupts	Four (jumper selectable)
Buffer	4K-byte (16 sector FIFO)
Sectors	
Winchester	256 bytes
Floppy	128/256/512/1024 bytes
Operating temperature	0° to 60° C
Power requirements	+5 Vdc @ 6.0 A (max.) -5 Vdc or -8 to -20 Vdc @ 90 mA (max.)
Dimensions	
Width x height	12.70 in. (32.26 cm) x 8.25 in. (20.96 cm)
Board thickness	0.875 in. (2.22 cm)

HDWE CONFIG.

CHAPTER 2

HARDWARE CONFIGURATION

2.1 INTRODUCTION

This chapter provides hardware configuration for the WDC.

2.2 HARDWARE CONFIGURATION

Figure 2-1 illustrates the location of the headers, LED indicator, and power connection. The VME/10 is shipped with factory-installed jumper configurations for normal development operation. A list of the headers is shown below:

a. Power connection (J1, J9)

b. Winchester data termination select (J7, J8)

c. I/O interrupt select (J10)

d. I/O Channel address select (J11)

e. Winchester and floppy disk drive parameters select (J16)

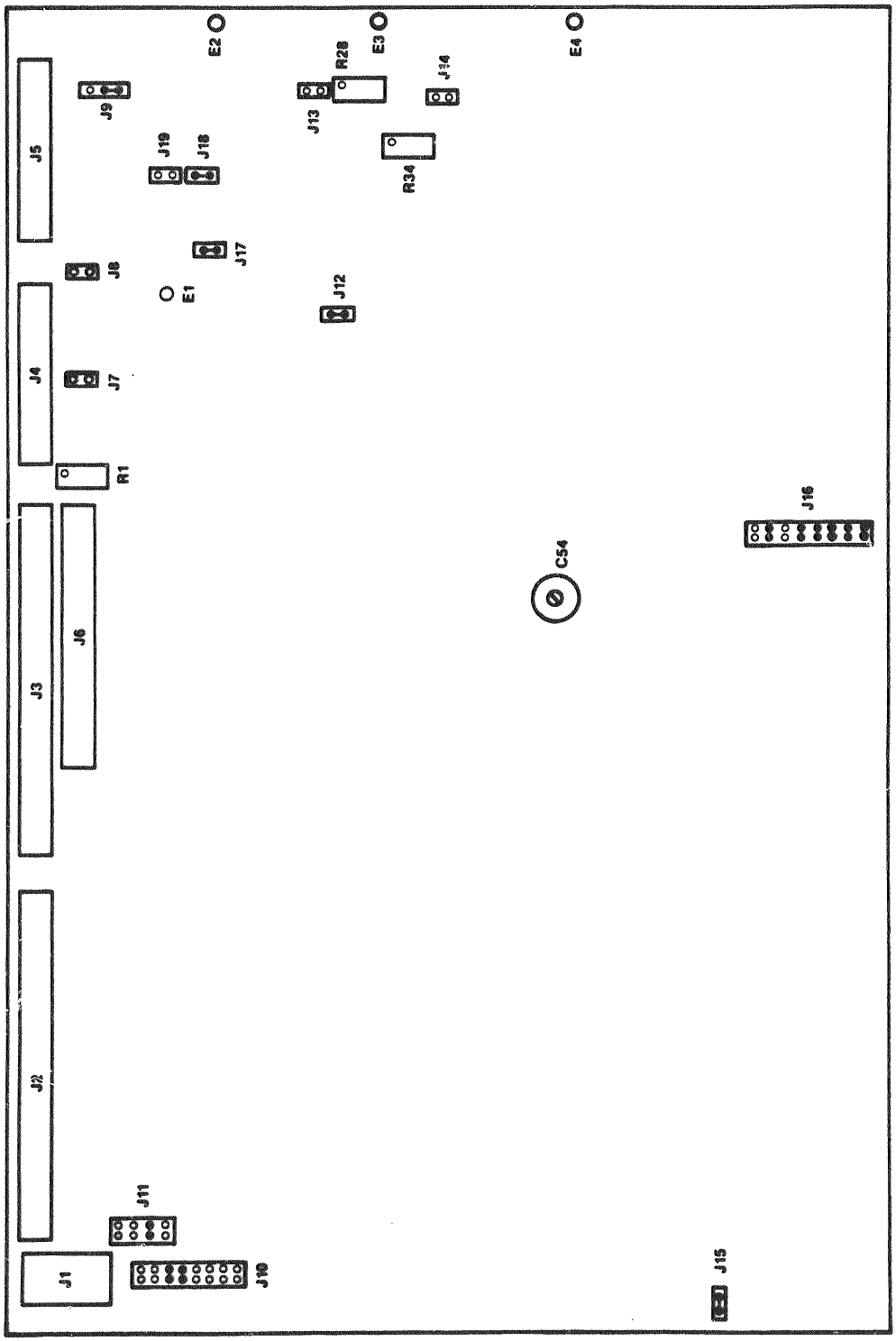


FIGURE 2-1. Option Locations

2.2.1 Power Connection (J1, J9)

The WDC requires +5 Vdc @ 6.0 A (max.) and -5 Vdc @ 90 mA or -8 to -20 Vdc @ 90 mA for operation. Connector J1 on the upper left of the module provides a convenient means of applying power to the WDC. Figure 2-2 shows the pin numbers and power requirements for J1.

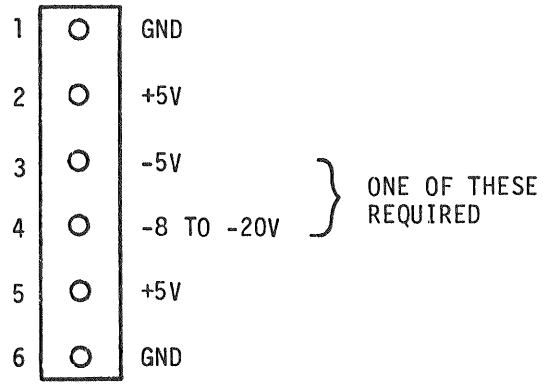


FIGURE 2-2. Power Connection (J1)

Header J9 is used in conjunction with the application of -5 Vdc or -8 to -20 Vdc. When -5 Vdc is applied to J1 pin 3, the jumper is positioned between pins 1 and 2 on header J9. The factory-installed position between pins 2 and 3 is used when -8 to -20 Vdc is applied to J1 pin 4 (see Figure 2-3).

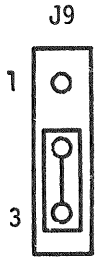


FIGURE 2-3. Power Connection (J9)

2.2.2 Winchester Data Termination Select (J7, J8)

Headers J7 and J8 apply only to the WDC designed for use with Winchester 8 inch drives (SA1000-compatible). Jumpers must be installed on headers J7 and J8 when used with the SA1000-type drives. The jumpers must be removed for any other operation.

2.2.3 I/O Interrupt Select (J10)

Header J10 allows the user to select one of four interrupt lines. Two types of interrupts are generated by the WDC -- command interrupt and data request interrupt. The WDC is shipped with jumpers positioned between pins 5 and 6 and between pins 7 and 8 (see Figure 2-4). Table 2-1 lists the jumper connections for each interrupt level.

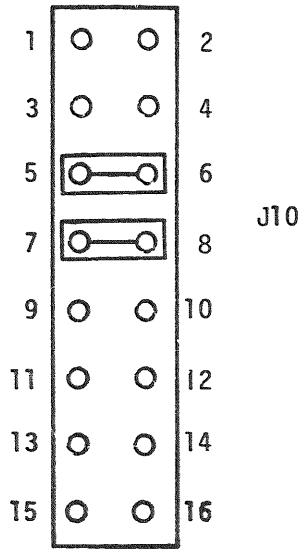


FIGURE 2-4. I/O Interrupt Select (J10)

TABLE 2-1. I/O Interrupt Select (J10)

JUMPER CONNECTIONS	FUNCTION
1-2	Data interrupt request - INT4*
5-6	Data interrupt request - INT3*
9-10	Data interrupt request - INT2*
13-14	Data interrupt request - INT1*
3-4	Command interrupt request - INT4*
7-8	Command interrupt request - INT3*
11-12	Command interrupt request - INT2*
15-16	Command interrupt request - INT1*

2.2.4 I/O Channel Address Select (J11)

Header J11 is used to select the address range to which the WDC is to respond. This is the address range reserved by the host to access the WDC. The factory-installed jumper between pins 5 and 6 on header J11 configures the WDC to respond to address range XXXXD1-XXXXDF. (XXXX is the host base address for the I/O Channel bus.) (See Figure 2-6.) Table 2-2 lists the jumper connections for each address range.

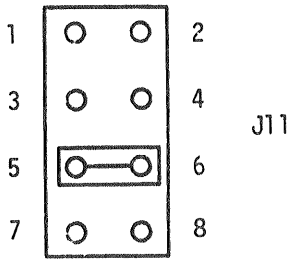


FIGURE 2-5. I/O Channel Address Select (J11)

TABLE 2-2. I/O Channel Address Select (J11)

JUMPER CONNECTIONS				ACCESS ADDRESSES
1 to 2	3 to 4	5 to 6	7 to 8	
IN	IN	IN	IN	XXXX01-XXXX0F
IN	IN	IN	OUT	XXXX11-XXXX1F
IN	IN	OUT	IN	XXXX21-XXXX2F
IN	IN	OUT	OUT	XXXX31-XXXX3F
IN	OUT	IN	IN	XXXX41-XXXX4F
IN	OUT	IN	OUT	XXXX51-XXXX5F
IN	OUT	OUT	IN	XXXX61-XXXX6F
IN	OUT	OUT	OUT	XXXX71-XXXX7F
OUT	IN	IN	IN	XXXX81-XXXX8F
OUT	IN	IN	OUT	XXXX91-XXXX9F
OUT	IN	OUT	IN	XXXXA1-XXXXAF
OUT	IN	OUT	OUT	XXXXB1-XXXXBF
OUT	OUT	IN	IN	XXXXC1-XXXXCF
OUT	OUT	IN	OUT	XXXXD1-XXXXDF
OUT	OUT	OUT	IN	XXXXE1-XXXXEF
OUT	OUT	OUT	OUT	XXXXF1-XXXXFF

NOTE: XXXX is the base address for the I/O Channel bus.

2.2.5 Factory-Use-Only Headers (J7, J8, J12, J13, J14, J15, J17, J18, J19)

Headers J7, J8, J12, J13, J14, J15, J17, J18, and J19 are for factory use only and have no user value. The jumpers on J12, J15, J17, and J18 must remain in place.

2.2.6 Winchester and Floppy Disk Drive Parameters Select (J16)

Header J16 is factory configured as shown in Figure 2-6. Table 2-3 lists the available parameters and the pin connections on header J16. Table 2-4 lists the pin connections on header J16 for the head stepping timing selection.

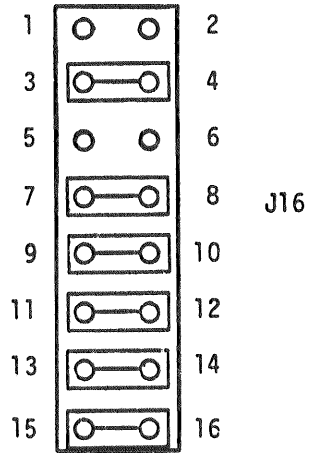


FIGURE 2-6. Winchester and Floppy Disk Drive Parameters (J16)

TABLE 2-3. Winchester and Floppy Disk Drive Parameters (J16)

JUMPER CONNECTION		PARAMETER
PINS	JUMPER	
1 to 2	IN	48 TPI track density for floppy disk drives
1 to 2	OUT	96 TPI track density for floppy disk drives
3 to 4	IN	5-1/4 inch floppy disk drives
3 to 4	OUT	8 inch floppy disk drives
5 to 6		Floppy step rate (see Table 2-4)
7 to 8		Floppy step rate (see Table 2-4)
9 to 10	IN	Fixed Winchester drive for WD1
9 to 10	OUT	Cartridge Winchester drive for WD1
11 to 12	IN	Buffered step for WD1
11 to 12	OUT	No buffered step for WD1
13 to 14	In	Fixed Winchester drive for WD0
13 to 14	OUT	Cartridge Winchester drive for WD0
15 to 16	IN	Buffered step for WD0
15 to 16	OUT	No buffered step for WD0

TABLE 2-4. Head Stepping Timing (J16)

JUMPER CONNECTIONS		FLOPPY DISK HEAD STEPPING TIMING
5 to 6	7 to 8	
IN	IN	3.2 msec between steps
OUT	IN	10.0 msec between steps
IN	OUT	20.0 msec between steps
OUT	OUT	35.0 msec between steps

CHAPTER 3

OPERATING INSTRUCTIONS

3.1 INTRODUCTION

This chapter provides necessary information to operate the WDC and recognize the error codes which may be encountered during operation of the WDC in a typical system configuration.

3.2 INDICATOR

LED indicator DS1, located on the upper right corner, illuminates for any one of the following:

a. When the WDC is initialized, the LED flashes for approximately 60 seconds during the self-test and drive spin-up.

b. When a failure occurs during the initialization period, the LED stops flashing and illuminates continuously.

c. When an I/O Channel reset or a selected reset command is applied to the WDC, the LED illuminates while the reset is active.

3.3 OPERATING PROCEDURE

The WDC is designed to operate with any host which uses an I/O Channel bus.

The driver software needed to operate the WDC is included in VERSAdos version 4.2 and above. VERSAdos 4.2 operates both MVME110 and VM02 I/O Channel masters.

The user may write a driver program to operate the WDC. Chapter 4 contains sufficient information for the purpose.

3.4 FORMATS

The WDC supports the following disk formats:

a. Winchester Disks (5-1/4 inch)

256 bytes per sector

32 sectors per track

MFM (modified frequency modulation)

b. Floppy Disks (5-1/4 inch)

128/256/512/1024 bytes per sector in FM (frequency modulation) mode

256/512/1024 bytes per sector in MFM mode

Track capacities based on sector size and FM/MFM are shown below:

FM	SSC (1)	Bytes/Sector	Sectors/Track 5-1/4 in.
0	0	128 FM	16
0	1	256 FM	8
0	2	512 FM	4
0	3	1024 FM	2
1	0	(2)	(2)
1	1	256 MFM (3)	16
1	2	512 MFM (3)	8
1	3	1024 MFM (3)	4

NOTES:

(1) SSC = Sector Size Code

(2) Not supported.

(3) The format drive command formats track 0 (i.e., cyl 0, side 0) at 128/256 or 512 FM automatically when MFM is requested according to the standard 1D/2D format.

Typical FM sector (128 byte) IBM 3740 format is shown below:

NO. OF BYTES:DATA (HEX)	
6:00	SYNC
1:FE	IDAM
1:XX	CYLINDER NUMBER
1:XX	SIDE NUMBER
1:XX	SECTOR NUMBER
1:00	SECTOR LENGTH 0 = 128 BYTES
2:XX	CRC
11:FF	GAP
6:00	SYNC
1:FB	DAM
128:E9	DATA
2:XX	CRC
27:FF	GAP

Typical MFM sector (256 bytes) IBM 34 format is shown below:

NO. OF BYTES:DATA (HEX)	
12:00	SYNC
3:A1	
1:FE	IDAM
1:XX	CYLINDER NUMBER
1:XX	SIDE NUMBER
1:XX	SECTOR NUMBER
1:01	SECTOR LENGTH 01 = 256 BYTES
2:XX	CRC
22:4E	GAP
12:00	SYNC
3:A1	
1:FB	DAM
256:E9	DATA
2:XX	CRC
54:FF	GAP

Winchester typical good sector (314 bytes total) is shown below:

NO. OF BYTES:DATA (HEX)	
12:00	SYNC
2:A1FE	IDAM
2:XX	FLAG (2 bits), CYLINDER NUMBER (14 bits) FLAG 00 = Good sector 01 = Alternate sector
1:XX	HEAD NUMBER (3 bits) SECTOR NUMBER (5 bits)
4:XX	ECC
2:00	PAD (write splice)
11:00	SYNC
2:A1F8	DAM
256:4E	DATA
4:XX	ECC
2:00	PAD
16:4E	GAP

Winchester typical defective sector (314 bytes total) is shown below:

NO. OF BYTES:DATA (HEX)	
12:00	SYNC
2:A1FE	IDAM
2:XX	FLAG (2 bits), CYLINDER NUMBER (14 bits) FLAG 10 = Defective sector
1:XX	HEAD NUMBER (3 bits), SECTOR NUMBER (5 bits)
4:XX	ECC
2:00	PAD
11:00	SYNC
2:A1F8	DAM
2:XX	CYLINDER
1:XX	ALTERNATE HEAD NUMBER (3 bits) ALTERNATE SECTOR NUMBER (5 bits)
4:XX	ECC
2:00	PAD
32:4E	GAP
77:XX	Same as first 77 bytes Ensures one header and alternate field is accessible.
77:XX	Same as first 77 bytes
77:XX	Same as first 77 bytes
6:4E	GAP

FUNCTIONAL DESCR.

CHAPTER 4

FUNCTIONAL DESCRIPTION

4.1 INTRODUCTION

This chapter provides a functional description of the WDC. The information presented should be sufficient for the user to write a driver program. Refer to Figure 4-1 for memory map.

4.2 FUNCTIONAL DESCRIPTION

The WDC appears to the VME/10 as a set of registers on the I/O Channel -- eight write registers for passing commands, parameters, and data to the WDC; eight read registers for passing status, sense, and data to the VME/10.

4.2.1 Write Registers

The eight write registers are listed below with descriptions of each register.

Register	Offset From Base Address	Function
WR0	0	Command block
WR1	1	Data interrupt enable
WR2	2	Selected reset
WR3	3	Not used
WR4-WR7	4-7	Write data

4.2.1.1 Command Block (WR0). Commands are passed to the WDC by writing a series of bytes to WR0. The first byte (byte 0) contains the command type and operation code, while the subsequent bytes contain information necessary for command execution. All bytes are required for each command (see Table 4-1). No command shortening is allowed.

TABLE 4-1. Command Block

FORMAT	DATA BITS							
	D7	D6	D5	D4	D3	D2	D1	D0
TYPE 0	EXCEPT CONFIGURE DRIVE							
BYTE 0	0	0	0	<-------- OP CODE --------				>
BYTE 1	0	<--LUN-->		<-------- LSN2 --------				>
BYTE 2	<---------- LSN1 ----------							>
BYTE 3	<---------- LSN0 ----------							>
BYTE 4	<---------- N ----------							>
BYTE 5	TD	SN	MF	<-- SSC -->		DS	CIE	DMA
TYPE 6	CONFIGURE DRIVE							
BYTE 0	1	1	0	<-------- OP CODE --------				>
BYTE 1	0	<--LUN-->		0	0	0	0	0
BYTE 2	<-- MAX HEAD -->			<-------- MAX CYL 1 --------				>
BYTE 3	<---------- MAX CYL 0 ----------							>
BYTE 4	<---------- START PRECOMP CYC NO. ----------							>
BYTE 5	0	0	0	0	0	0	CIE	0

NOTES:

OP CODE - describes the function to be performed (0-1F)

LUN - logical unit number (0-3)
0,1 = Winchester drives
2,3 = floppy drives

LSN - logical sector number (0-1FFFFF)

N - number of sectors to be read, written, or scanned. Interleave factor during format use 0 or 1. (1-FF, 0 where 0 = 100)

TD - track density of media (0-1)
0 = 48 TPI (may be read on 96 TPI drive)
1 = 96 TPI (must be 96 TPI drive)

SN - sector numbering (0-1) used when accessing floppy disks only (LUN 2 or LUN 3)
0 = sectors are formatted 1 to X on both sides
1 = sectors are formatted 1 to X on side 0 and (X+1) to 2X on side 1

MF - recording method (0-1) used when accessing floppy disk only (LUN 2 or LUN 3)
0 = FM
1 = MFM

SSC - sector size code (0-3) used when accessing floppy disk only (LUN 2 or LUN 3)
0 = 128 bytes per sector
1 = 256 bytes per sector
2 = 512 bytes per sector
3 = 1024 bytes per sector

DS - diskette sides (0-1) used when accessing floppy disk only (LUN 2 or LUN 3)
0 = single sided media
1 = double sided media

CIE - command interrupt enable (0-1)
0 = no command interrupts
1 = set I/O Channel interrupt on completion of command (normal or error)

DMA - data request mode (0-1)
0 = block (128 bytes) level data request
1 = byte level data request

4.2.1.2 Data Interrupt Enable (WR1). By writing a one (01) to this register, an I/O Channel interrupt (jumper selected) is generated simultaneously with the data request bit. Writing a zero (00) disables this interrupt (see paragraph 4.2.7).

4.2.1.3 Selected Reset (WR2). A write to this location forces the controller to reset and self-test diagnostics to be executed.

4.2.1.4 Write Data Registers (WR4-WR7). A write to any of these registers causes the data byte to be stored in the on-board FIFO buffer.

4.2.2 Read Registers

The eight read registers are listed below with descriptions of each register.

Register	Offset From Base Address	Function
RR0	0	Sense block
RR1	1	Controller status
RR2	2	Not used
RR3	3	Not used
RR4-RR7	4-7	Read data

4.2.2.1 Sense Block (RR0). A series of reads from this register accesses the 10 WDC sense bytes. These bytes are used to pass detailed information concerning the last command executed to the host. The sense block is defined in Table 4-2. One sense byte is returned with each read of RR0. The first read accesses byte 0, the second read accesses byte 1, and so on, until the eleventh read, which reverts back to byte 0. As many bytes may be read as required by the host. A write to WR0 (command block) takes the WDC out of the read sense mode and to the command block mode.

TABLE 4-2. Sense Block

FORMAT	DATA BITS							
	D7	D6	D5	D4	D3	D2	D1	D0
TYPE 0								
BYTE 0	<---------- ERROR CODE ---------->							
BYTE 1	RST	<--LUN-->		N/U	RDY	SKC	W/P	N/U
BYTE 2	<------ PHYSICAL CYLINDER NUMBER (MSB) ------>							
BYTE 3	<------ PHYSICAL CYLINDER NUMBER (LSB) ------>							
BYTE 4	<-- HEAD NUMBER --><---- SECTOR NUMBER ------>							
BYTE 5	<---------- N ---------->							
BYTE 6-9	Detailed information as a function of error code (see paragraphs 4.2.4 and 4.2.10).							

NOTES:

ERROR CODE - the error code for the last command executed (see paragraph 4.2.4)

RST - 1 to indicate reset status

LUN - logical unit number (0-3)
0,1 = Winchester drives
2,3 = floppy drives

N/U - not used

RDY - drive ready if RST = 0

SKC - seek complete if RST = 0

W/P - write protected if RST = 0

4.2.2.2 Controller Status (RR1). This register describes the state of the WDC as shown in Table 4-3. This register goes to A0 at reset, and is set to 08 after successful self-test or 28 on a self-test detected error.

TABLE 4-3. Controller Status

FORMAT	DATA BITS							
	D7	D6	D5	D4	D3	D2	D1	D0
RR1	CB	CI	FLT	DI	DRQ	CIE	DMA	DIE

NOTES:

CB - controller busy; indicates the WDC is executing a command. While busy, the controller does not accept a new command or respond to a read sense.

CI - command interrupt; a command has terminated with CIE = 1. This bit is reset by a new command block or a read sense.

FLT - fault; an error is detected in decoding or executing a command. This bit is reset by a new command block or read sense.

DI - data request interrupt;
DRQ = 1 and DIE = 1

DRQ - data request;
read - read data is available in the FIFO buffer.
write - space for write data is available in the FIFO buffer.

CIE - command interrupt enable;
copy of the CIE bit from command byte 5.

DMA - copy of the DMA bit from command byte 5.
0 = block transfer mode - at least 128 bytes may be read/written to the FIFO buffer for each data request.
1 = byte transfer mode - at least one byte may be read/written to the FIFO buffer for each data request.

DIE - data interrupt enable; copy of the DIE bit from WR1.

4.2.2.3 Read Data Register (RR4-RR7). A read from any of these registers accesses the next byte of read data from the FIFO buffer.

4.2.3 Command Description

The type/code of the command and function of each is listed below:

Type/Code (T/C) (Hex)	Function
0/0	Check drive status
0/1	Recalibrate
0/4	Format drive
0/6	Format track
0/7	Format DEF/ALT track (Winchester only)
0/8	Read sectors
0/9	Scan sectors
0/A	Write sectors
0/B	Seek
0/C	Read track (Winchester only)
0/D	Read ECC (Winchester only)
0/E	Write ECC (Winchester only)
6/0	Configure drive

4.2.3.1 Check Drive Status (0/0). The drive defined by the LUN is selected, and status is returned in sense byte 1.

4.2.3.2 Recalibrate (0/1). The drive defined by the LUN is selected and stepped to track 0.

4.2.3.3 Format Drive (0/4). The entire drive defined by LUN and configuration is formatted according to interleave factor n. Sectors are numbered so that the next sector number equals the last sector number plus n.

where: n = 0-1 0,1,2.....
= 2 0,2,4,6.....
= 16 0,16,1,17.....

4.2.3.4 Format Track (0/6). Format track is similar to format drive except only one track defined by the LSN is formatted.

4.2.3.5 Format DEF/ALT Track (Winchester Only) (0/7). The drive defined by the LUN is positioned to the track (cylinder and head) which is defined by the LSN. It is formatted according to the subsequent 256-byte format descriptor written to the WDC FIFO buffer by the host. The format descriptor provides information for sector interleaving and alternate sector allocation.

Format Descriptor

Five bytes are required for each of the 32 physical sectors on the track, followed by fill bytes to 256, and are defined as follows:

BYTE 0 - 00 if sector is to be marked good
40 if sector is an alternate
80 if sector is a defective sector

BYTE 1 - Logical sector number for this track (00-1F). This allows sector interleaving. Each number may appear only once for each track.

BYTE 2 - Cylinder number (MSB) of alternate sector.

BYTE 3 - Cylinder number (LSB) of alternate sector.

BYTE 4 - Head number (0-7) of alternate sector. Logical sector number (0-1F) of alternate sector.

Bytes 2, 3, and 4 are relevant only if sector is marked defective (see paragraph 4.2.5).

4.2.3.6 Read Sectors (0/8). Read n sectors, from the drive specified by the LUN, starting at the sector specified as LSN (see paragraph 4.2.5). The DRQ (WDC status) and/or interrupt indicate data is available in the FIFO buffer to be unloaded by the host (see paragraph 4.2.8). The WDC remains busy until the host unloads the last byte from the FIFO.

4.2.3.7 Scan Sectors (0/9). Scan sectors is similar to the read sectors command except no data is transmitted to the host. All sector headers, data sectors, and alternate sectors are checked for correct ECC.

4.2.3.8 Write Sectors (0/A). Write n sectors to the drive specified by the LUN, starting with the sector specified by LSN (see paragraph 4.2.5). DRQ (WDC status) and/or interrupt indicate space is available in the FIFO buffer to be loaded by the host (see paragraph 4.2.8).

4.2.3.9 Seek (0/B). Position the heads of the drive specified by the LUN at the cylinder specified by the LSN. This command does not access the disk.

4.2.3.10 Read Track (Winchester Only) (0/C). Reads 8704 bytes from the track specified by LSN and drive specified by LUN. 272 bytes are transferred for each physical sector as follows:

2 - IDAM (A1FE)
2 - Cylinder number
1 - Head, sector number
4 - Header ECC
1 - 00
2 - DAM (A1F8)
256 - Data
4 - ECC

The FIFO buffer state is not checked by the controller. Therefore, it is left to the host to unload the buffer fast enough so as not to cause an overrun. The controller loads the buffer at approximately the disk data rate (e.g., 1.6 usec/byte for 5-1/4 inch Winchester).

4.2.3.11 Read ECC (Winchester Only) (0/0). 260 bytes are read from the drive specified by LUN at the sector specified by LSN. The controller returns 256 bytes from the data field, together with four bytes of ECC.

4.2.3.12 Write ECC (Winchester Only) 0/E). 260 bytes are written to the drive specified by LUN at the sector specified by LSN. The controller writes the first 256 bytes into the data field, followed by four bytes into the ECC field.

4.2.3.13 Configure Drive (6/0). This command allows the host to specify the maximum cylinder number and maximum head number for each drive in the configuration (see paragraph 3.5). Reset sets these parameters for each drive to maximum cylinder = 0 and maximum heads = 0.

This command, in conjunction with a seek, may be used to position the heads of a disk with a shipping zone past the last data cylinder.

The WDC uses the maximum head for detecting the requirement for a cylinder switch. Maximum cylinder is used to detect an out-of-range LSN and precompensated cylinder number to set the low write-current to drive and perform write-precompensation on the data at cylinders greater than the precompensated cylinder number. This command also performs a recalibrate on the specified LUN.

4.2.4 Error Codes

Byte 0 of the sense block contains the error code for the last command executed. The error codes and definitions are listed below.

Error Code (Hex)	Definition
0	No error - normal completion
1	No index
2	No track 000
3	Invalid LSN
4	Drive not ready
5	No seek complete
6	ID header not found
7	Data mark not found
8	Nested alternate error
9-B	Not used
C	Invalid command
D-11	Not used
12	Uncorrectable data error
13	Correctable data error
14	Write protect
15	Write fault
16-40	Not used
41	Floppy disk controller fault
42	Invalid floppy format
43	Media/drive incompatible
44	Floppy controller detected error
45-7F	Not used
80	Reset/self-test detected error

Error code definitions are as follows:

Error Code	Definition
1	No index The index pulse from the LUN was not detected.
2	No track 000 Track 000 signal from the LUN was not detected in 1024 steps during a recalibrate command.
3	Invalid LSN A command attempted to access a sector on a cylinder greater than the maximum cylinder number for the LUN as specified in the drive configuration. A configuration command for the LUN was not received. Default value for the maximum cylinder number is 0.
4	Drive not ready Winchester - the specified LUN is not ready or does not exist. Floppy - the drive door is open, there is no diskette in the drive, or the drive specified is not in the system.
5	No seek complete Seek complete signal was not received from the Winchester after a step.
6	ID header not found A sector header with the correct cylinder, head, and sector information could not be found within five revolutions of the disk. A seek error can cause the ID header not found error. Unformatted media can cause the ID header not found error.
7	Data mark not found A correct sector header was found but the expected data mark was not found.
8	Nested alternate error The alternate sector for a sector marked bad is also marked bad.
C	Invalid command The type and op code in command byte 0 is undefined.
12	Uncorrectable data error A burst error of more than seven bits or more than one burst error occurred when reading the last sector.

13 Correctable data error

A burst error of seven or less bits was detected in the last sector. Sense bytes 6 and 7 contain the byte offset from the first byte of the last sector. Sense bytes 7 and 8 contain the correction mask to be XORed with the two data bytes at (offset) and (offset + 1) (i.e., correct data at offset = (offset) + sense byte 8; correct data at offset + 1 = (offset + 1) + sense byte 9).

14 Write protect

A write was attempted to a protected disk.

15 Write fault

The drive detected loss of write current in the write head.

41 Floppy disk controller error

The floppy disk controller IC failed to respond to a command. If this condition is detected, the WDC attempts to reset the floppy disk controller IC in preparation for an expected retry from the host.

42 Invalid floppy format

The command attempted to format or write specifying 128-byte sectors in MFM mode. This format is not supported.

43 Media/drive incompatible

The command byte 5 specified floppy media which is incompatible with the drive as follows:

Read or write two-sided media on a single-sided drive.

Write 48 TPI format on a 96 TPI drive.

Read or write 96 TPI format on a 48 TPI drive.

44 Unexpected floppy disk controller interrupt

A non-decoded error was detected by the floppy disk controller IC. Sense bytes 6-9 contain the controller status ST0-2.

80 Self-test detected error

Sense byte 1 identifies the error

D7	D6	D5	D4	D3	D2	D1	D0
1	N/U	N/U	N/U	FDC ERROR	FIFO R/W ERROR	FIFO CNTR ERROR	RAM ERROR

4.2.5 Alternate Sectors

The WDC provides a method to assign alternate sectors to defective areas of a particular drive. These areas are defined by the drive manufacturer for each drive by cylinder number, head number, and byte displacement from the index. The defective physical sector can be calculated by:

$$\text{Defective physical sector} = \frac{\text{byte displacement}-16}{314}$$

Where the range is 0 to 31, a calculated value of greater than 31 should be considered to be 31.

At format time, these defective areas should be mapped to an area reserved for alternate sectors (see paragraph 4.2.3). Normal manufacturer's criteria allows up to 12 defective areas per disk surface. Therefore, space should be allowed for 12 alternate sectors per surface.

When a sector marked defective is encountered by the WDC during a read/scan/write/read ECC/write ECC command, the alternate sector information is read from the disk. This information is duplicated four times in the sector with the defect to ensure accessability. The WDC seeks to the alternate sector, checks the alternate sector mark, performs the read/scan/write on the alternate sector, and returns to the logical sector immediately following the defect.

4.2.6 Logical Sector Number (LSN)

The positions on the disk are referenced by LSN.

where:

LSN = (CYL NO. *(NO. HDS/CYL + HD NO.)*
(NO. SECTORS/TRACK) + SECTOR NO.

For commands such as seek or format track, the LSN may be any sector on the desired track.

4.2.7 Interrupts

Two types of interrupts are generated by the WDC -- command interrupt and data request interrupt.

4.2.7.1 Command Interrupt. This interrupt is generated when command execution is terminated due to completion or an error condition, and the command interrupt enable (CIE) bit of the command block is equal to 1. This interrupt is turned off upon receipt of a new command or a read sense.

4.2.7.2 Data Request Interrupt. This interrupt is generated when data is available for a read operation or space is available for a write operation, and the data interrupt enable (DIE) bit in WR1 is equal to 1 (see paragraph 4.2.8).

4.2.8 FIFO Buffer

The WDC includes a 4K-byte FIFO buffer for passing data to/from the host. Immediately after reset, before the first command, the host may read/write the FIFO to perform testing. When the first command byte is received, the host access to the FIFO is inhibited until an entire command block is received and decoded by the WDC. At this time, the FIFO is read enabled for a read command, or write enabled for a write or format command. The state of the DRQ bit and/or the data interrupt line reflects the state of the FIFO.

The WDC monitors the state of the FIFO and suspends a command until the required space/data is available to read/write an entire sector. This eliminates overrun or underrun conditions due to differences in transfer rates between the host and the disk drive.

For the two transfer modes (read, write), DRQ indicates slightly different states of the FIFO, as shown in the following two paragraphs.

NOTE

> For write operations, DRQ reflects only the state of the FIFO and is not a function of the size of the transfer requested. For example, if a write requires 256 bytes, the DRQ signal remains active after 256 bytes have been received, because there is still space available.

When a command ends (CB=0), DRQ remains active, and dummy accesses to the FIFO are allowed. Read data is invalid and write data is thrown away by the controller. This allows the host software to perform the data transfer for the entire command, checking for errors only after all the data has been transferred.

4.2.8.1 Non-DMA Mode (DMA=0 CPU Polling). In a read operation, DRQ is on while there is at least one 128-byte block of data in the FIFO. Data is read from the FIFO in 128-byte blocks, and DRQ is checked only between blocks.

In a write operation, DRQ is on while there is space for at least one 125-byte block of data in the FIFO. Data is written to the FIFO in 128-byte blocks, and DRQ is checked only between blocks.

4.2.8.2 DMA Mode (DMA=1. In a read operation, DRQ is on while there is at least one byte of data in the FIFO.

In a write operation, DRQ is on while there is space for at least one data byte in the FIFO.

4.2.9 Floppy Disk Drives (96TPI)

The WDC has the capability to control either 48TPI or 96TPI drives. With 96TPI drives, diskettes recorded at 48TPI may be read but not written. Byte 5 of the command block identifies the media as 48TPI, which causes the WDC to issue double steps to the drive. This mode is transparent to the host.

4.2.10 Reset/Self-Test

Upon receipt of an I/O Channel reset or a selected reset command, the WDC performs the following:

Sets busy and exception in RR1.

Tests internal RAM.

Tests the FIFO buffer and associated counter.

Initializes the internal registers.

Tests and initializes the floppy disk controller IC.

Delays 55 seconds if in cold start (dc power-up) to allow Winchester drive to come up to speed.

Polls drives, attempts to recalibrate the drives found ready, and stores status for each drive in sense bytes 6-9.

If there are no self-test errors, exception is reset. Drive faults during polling are not considered errors.

Enables the host to write/read the FIFO buffer (diagnostics).

Resets the busy signal.

Sense bytes 0-9 reflect the status of the reset/self-test sequence as shown in Table 4-4.

TABLE 4-4. Sense Bytes

FORMAT	DATA BITS								COMMENT
	D7	D6	D5	D4	D3	D2	D1	D0	
BYTE 0	0	0	0	0	0	0	0	0	No error
	1	0	0	0	0	0	0	0	Self-test error
BYTE 1	1	0	0	0	FDC	FIFO	CTR	RAM	Failed test ID
BYTES 2-5	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U	
BYTE 6	WSM	F/C	0	0	RDY	SKC	W/P	TRK0	LUN 0
BYTE 7	WSM	F/C	0	0	RDY	SKC	W/P	TRK0	LUN 1
BYTE 8	<--	FSR	-->	5/8	TPI	RDY	SKC	W/P	TRK0 LUN 2
BYTE 9	<--	FSR	-->	5/8	TPI	RDY	SKC	W/P	TRK0 LUN 3

NOTES:

FDC - Floppy disk controller IC

FIFO - First in first out buffer

CTR - FIFO counter

RAM - Random access memory

WSM - Winchester stepping mode
0 = buffered step -- 12 us
1 = 3.2 ms

F/C - Fixed or cartridge Winchester drive
0 = fixed
1 = cartridge

RDY - LUN indicated ready

SKC - LUN indicated seek complete

W/P - LUN is write protected

TRK0 - LUN is at track 0 (recalibrated)

FSR - Floppy stepping rate
00 = 3.2 ms
01 = 10 ms
10 = 20 ms
11 = 35 ms

5/8 - Floppy size (5-1/4 inch)
0 = 5-1/4 inch

TPI - Floppy track density
0 = 48 TPI
1 = 96 TPI

4.3 DISK ERROR RECOVERY

The following procedure should be followed to ensure data integrity when an ECC error is detected.

a. The read of the error sector should be retried five times to eliminate soft errors.

b. If the error is correctable, the sector read should be retried, and the offset and error mask saved (sense bytes 6-9).

c. When two consecutive retries produce the same values (sense bytes 6-9), the error data should be corrected in the host memory and rewritten to the disk.

4.4 MEMORY MAP

Figure 4-1 shows the microcontroller address space.

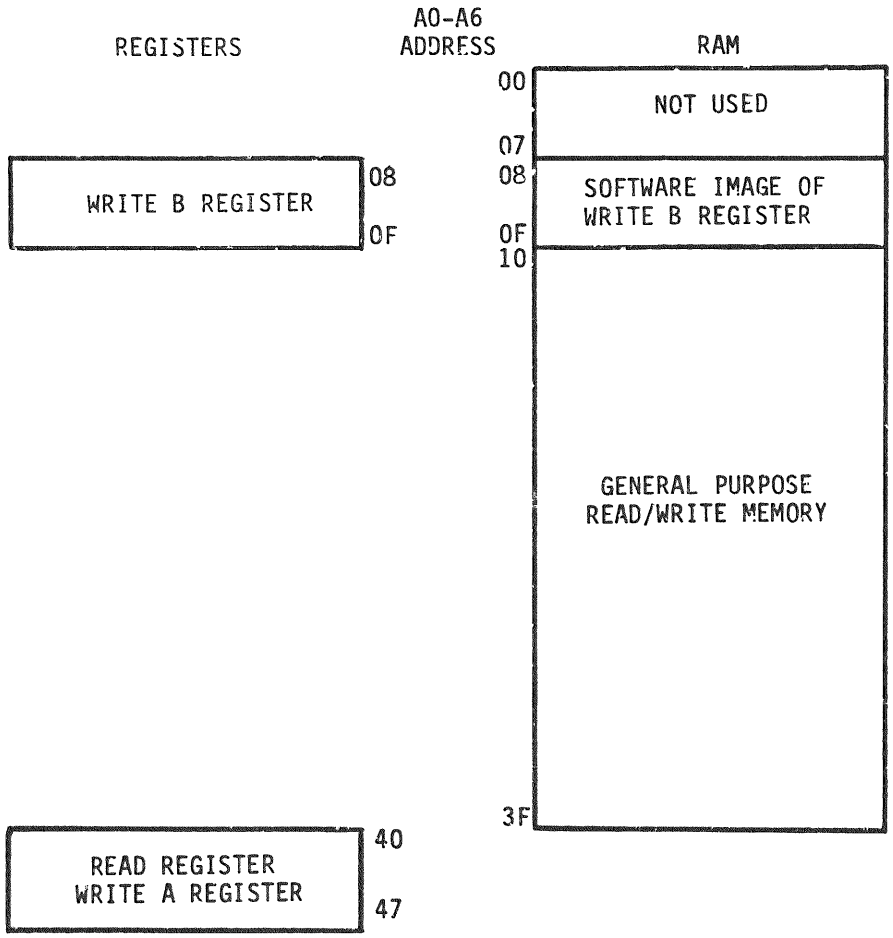


FIGURE 4-1. Memory Map

CHAPTER 5

THEORY OF OPERATION

5.1 INTRODUCTION

This chapter provides a detailed theory of operation. The WDC is an intelligent interface between the VME/10 I/O Channel and the Winchester disk drive and the floppy disk drive.

5.2 GENERAL DESCRIPTION

The WDC performs high-level commands such as read/write data, format track, verify data, etc., and includes implied seeks, automatic track/head switching, alternate sectoring, and error checking. Data is sent between the VME/10 and the WDC through interrupt-initiated block transfers, interrupt-initiated byte transfers, or by processor polling.

The WDC appears to the VME/10 as a set of registers on the I/O Channel (see Chapter 4) -- eight write registers for passing commands, parameters, and data to the WDC; eight read registers for passing status, sense, and data to the VME/10.

5.3 BLOCK DIAGRAM DESCRIPTION

A block diagram of the WDC is shown in Figure 5-1. Schematic diagrams are shown in Chapter 6. The WDC consists of the following circuit areas:

- I/O bus interface
- I/O registers
- Micro controller
- Micro controller registers
- FIFO
- Disk drive connections
- Winchester write logic
- Winchester read logic
- Winchester PLL
- Winchester data separator
- Winchester ECC generator/checker
- Floppy interface

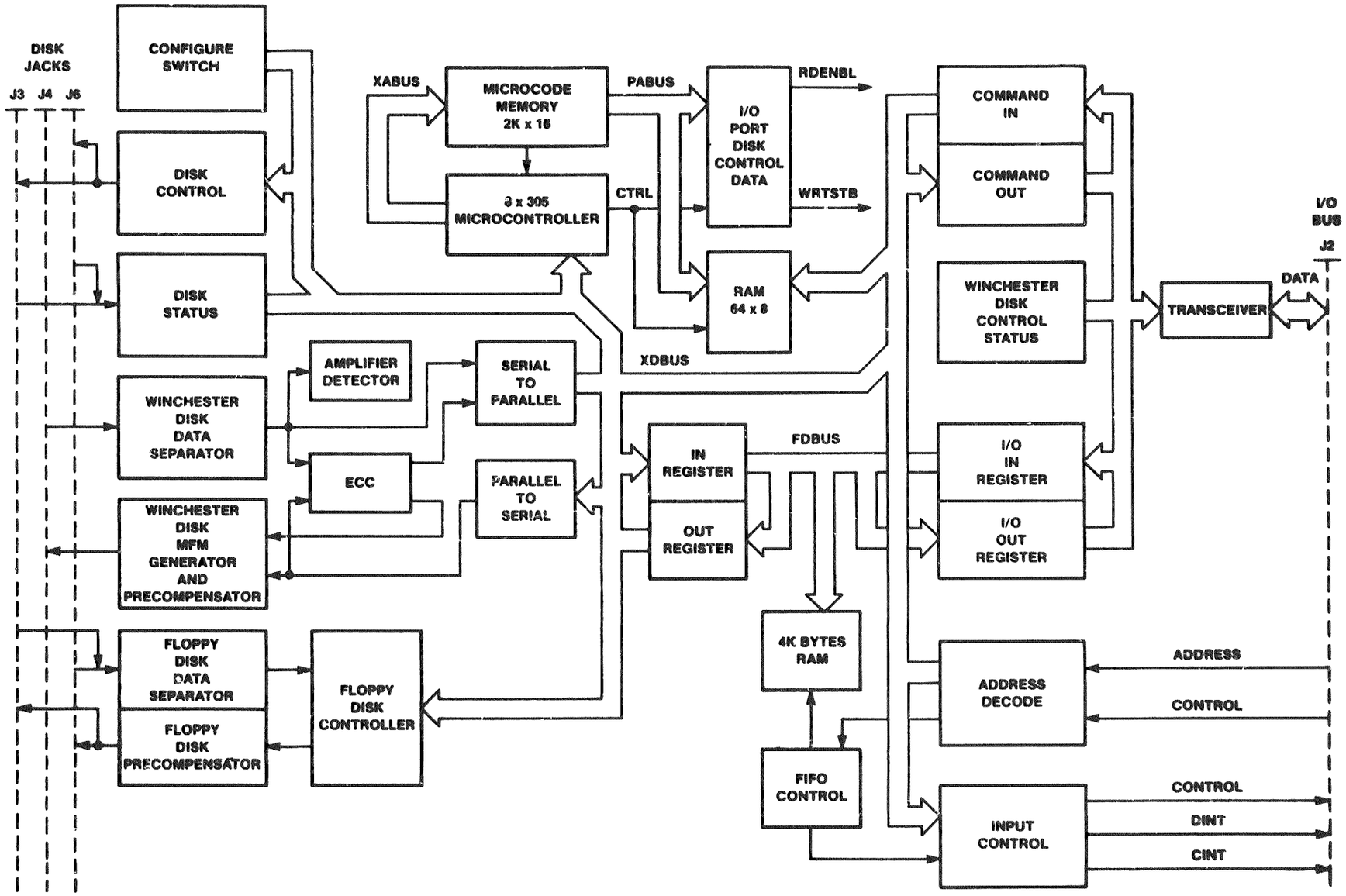


FIGURE 5-1. WDC Block Diagram

5.3.1 I/O Bus Interface

The host communicates with the WDC over the I/O bus which is described in the Input/Output Channel Specification Manual, M68RIOCS. The WDC appears to the VME/10 as eight sequentially addressed registers. Only one byte of data can be transferred between the WDC and the host during a session. When multiple bytes of data are to be transferred, multiple sessions are required.

The host initiates a session with the WDC by placing an address on the A0-A11 address line. The U1 octal comparator compares the A3-A6 address signals to the strapping pattern selected on the J11 header, and the A7-A11 address signals to a zero state. If both of these conditions are satisfied, the address is recognized as being for the WDC, and the signal at U1-19 is driven low. The U1-19 signal, the A0-A2, and WRT* signals are latched into the U2 register when the STB* signal from the I/O bus goes low. Also, when this occurs, the U21 shift register is allowed to shift at a 16-MHz rate, and the U21-5 signal goes high on the second shift pulse. This permits the U19 and U41 elements to decode the I/O address to a specific WDC register and specify whether a read or a write function is to be performed. Table 5-1 indicates the relationship between these signals and the WDC registers.

TABLE 5-1. WDC I/O Address

WRT*	A2	A1	A0	REGISTER	STATUS
0	0	0	0	Write Command	(CMD* is low)
0	0	0	1	Write Control	(CNTRL* is low)
0	0	1	0	Write Reset	(SRESET* is low)
0	0	1	1	Not used	
0	1	0	0	Write FIFO Memory	(IO WRTRAM is high)
0	1	0	1	"	"
0	1	1	0	"	"
0	1	1	1	"	"
1	0	0	0	Read Sense	(RDSNS* is low)
1	0	0	1	Read Status	(RDSTAT* is low)
1	0	1	0	Not used	
1	0	1	1	Not used	
1	1	0	0	Read FIFO Memory	(IORDRAM is high)
1	1	0	1	"	"
1	1	1	0	"	"
1	1	1	1	"	"

The ADRMTCH* signal becomes low as soon as the U1 comparator recognizes the I/O address as being for the WDC. This signal being active (low) enables the U5 inverting transceiver to transmit data in the direction specified by the IOWRT* signal. If the IOWRT* signal is low, the direction of data flow is from the I/O bus to the WDC; if IOWRT* is high, the data is from the WDC to the host on the I/O bus. The U5 transceiver is an inverting element because the microcontroller (U85) requires the data on the XDBUS to be active (logical one) when it is low and the I/O data lines are active (logical one) when they are high. The inverting element provides the compatibility between these two buses, and the resulting inverted bus is named the IODBUS. Note that for this same reason, all the signal lines which are examined by the microcontroller are labeled on the schematic with the opposite polarity to the corresponding bit in the microcontroller read and write registers.

After the WDC completes the activity required by the particular address accessed, it must drive the I/O bus XACK* signal low to allow the host to complete the session. If the session requires the WDC to furnish data to the host (read type), the data is placed on the I/O bus D0-D7 lines by the WDC. Then, after a delay of at least 125 nsec, the XACK* signal is driven low. This delay is achieved using the U21 shift register and is discussed later. If the session requires the WDC to accept data from the host (write type), no delay is required, and the XACK* signal is driven low as soon as the WDC accepts the data.

5.3.1.1 Write Command Session. The host writes to the command address to transfer the command to be performed and to specify the pertinent parameters.

The CMD* signal being low causes the CMD/SENSE* signal to be low through U59-3 and U58-6. This signal is gated into the U26 register where it is examined by the microcontroller performing a read of the STAT1 register. The CMD/SENSE* lead is low for either a write command or a read sense operation, and the microcontroller must look at th IOWRT signal to determine which address is being accessed by the host. The IOWRT signal is also present in the STAT1 register and is high (active) for the write command address and low (inactive) for the read sense address. After the microcontroller determines the address is the write command, it inputs the data from the host by reading the RDIO register. This causes the IODATARD* signal to be low to U6, and gates the host data onto the microcontroller XDBUS. The microcontroller then performs a write to the WRTIO register. This forces the IODATAWRT* low, setting the U68-5 flip-flop and driving the U21-7 lead high via U58-12. This high at U21-7 propagates through the U21 shift register at a 16-MHz rate. When U21-15 becomes high, U59-6 gate goes low, setting the U68-9 flip-flop and forcing the XACK* signal low through U58-8. When the host determines that XACK* is low, it raises the STB* signal high to terminate the session. When the U68-5 flip-flop was set by the IODATAWRT* pulse, the U58-6 was forced high to make the CMD/SENSE* line inactive (high) and prevent the microcontroller from performing a multiple read of data for a single command. The IODATAWRT* pulse going low also gates data from the microcontroller XDBUS into the U23 register. This serves no useful purpose for the write command address sequence. When the host raises the STB* signal to a high level, the I/O interface circuitry returns to a quiescent state with the U21 shift register reset, the U19 and U41 decoders disabled, and the U68-5 and U68-9 flip-flops reset.

5.3.1.2 Write Control Session. The write control address is used to control the data interrupt enable function. If data bit D0 is high, the data interrupt enable function is activated during a control write session; if D0 is low during the control write, the function is made inactive.

When the CNTRL* signal goes low, the state of the IOD0* (inverted D0 bit) is strobed into the U69-5 flip-flop. This flip-flop is set if the D0 bit is low and the U70-13 gate inhibits any interrupt request through U43-6. The U69-5 flip-flop is reset if the D0 bit is high when the control write takes place. This drives the U70-11 signal low to partially enable the gate. When the DATAINT* goes low, the gate is fully enabled and an interrupt request to the host is generated through the U43-6 gate. The CNTRL* signal being low also causes the U58-8 signal to be high, which drives the XACK* signal low through U43-3. The host then terminates the session.

5.3.1.3 Write Software Reset Session. The host is able to initialize the WDC to a reset state by performing a write to this address.

When the SRESET* goes low, the U59-11 signal is driven high to force the RESET* signal low through U43-8. This resets all of the WDC circuitry except the I/O interface which is reset when the host drives the STB* signal inactive (high). The microcontroller chip requires a reset pulse of at least 250 nsec in duration to guarantee proper initialization. This is achieved using the U21 shift register. When the SRESET* signal goes low, the U21-7 lead becomes high through U58-12, and the shifting process starts at the 16-MHz rate. When the U21-15 signal becomes active, it samples the U59-6 gate, but this is inhibited by the SRESET* signal being low. The U21-19 signal becomes active a minimum of five clock pulses after the RESET* signal is forced low, which is sufficient to satisfy the microcontroller requirements. The U21-19 signal being high forces the U42-8 signal low, the U58-8 signal high, and drives the XACK* signal low through U43-3. The host then terminates the session as described in paragraph 5.3.1.1.

5.3.1.4 Write FIFO Memory Session. As shown in Table 5-1, the host may write to the WDC FIFO memory using any one of four consecutive addresses. This allows the host to efficiently use the 68000 MOVEP instruction in writing to the FIFO memory.

When the IOWRTRAM signal goes high, the U80-5 flip-flop is set if the ENHFWRT signal is active (high). The ENHFWRT signal is controlled by the microcontroller and is used to prevent the host from writing into the FIFO memory at an illogical time. The microcontroller changes this bit by writing into the XD3 bit of the CTRL1 register. If the ENHFWRT signal is high when the IOWRTRAM signal goes high, the U80-5 flip-flop is set, the IOWRTREQ* signal goes low, and a request is generated to the FIFO controller to write the I/O bus data into FIFO memory. The mechanism of writing into the memory is discussed later. When the data has been written into the FIFO memory, the FIFO controller resets the U80-5 flip-flop, which forces the IOWRTREQ* signal high. This sets the U68-9 flip-flop, which forces the XACK* signal low through U58-9 and U43-3. The host then terminates the session as described in paragraph 5.3.1.1.

5.3.1.5 Read Sense Session. The RDSNS* signal being low causes the CMD/SENSE* signal to be low through U59-3 and U58-6. This signal is gated into the U26 register where it is examined by the microcontroller performing a read of the STAT1 register. As discussed previously, the CMD/SENSE* signal is also low for a write command operation. The microcontroller examines the IOWRT signal (XD6 bit of STATI) to determine which operation is being initiated. The IOWRT signal is low if the read sense address is accessed, and the microcontroller reads a byte of sense information from private RAM and writes it into the WRTIO register. This causes the sense byte to be placed on the XDBUS, the IODATAWRT* signal to be driven low and the sense byte to be gated into the U23 register through U29-8. When the RDSNS* signal is low, the contents of the U23 register are gated onto the IODBUS and through the U5 transceiver onto the D0-D7 leads. When the IODATAWRT* signal went low, it also set the U68-5 flip-flop, which forced the CMD/SENSE* inactive (high) and made the U21-7 lead of the shift register high via U58-12. This allows the U21 shift register to sequentially propagate a high on its outputs. When U21-15 becomes high, U59-6 is enabled low and the U68-9 flip-flop becomes set to force XACK* low through U58-8 and U43-3. The host then terminates the session as previously described in paragraph 5.3.1.1.

5.3.1.6 Read Status Session. When the RDSTAT* signal goes low, the U22 latch stores the state of its inputs (which is the WDC status) and enables this status onto the IODBUS. Bits 1, 2, 5, 6, and 7 of the status are controlled directly by the microcontroller. The microcontroller makes these bits available by writing the appropriate data into U60 CSTAT register. The remaining status bits are obtained directly from the hardware, as shown on the schematic. The functions assigned to each of these status bits are listed in Figure 5-2, and are discussed in paragraph 4.2.2. Concurrently with gating the status byte onto the IODBUS and hence to the D0-D7 leads via U5, the U21 shift register is enabled to provide the delay required by the I/O bus before XACK can be activated. This is done by the RDSTAT* signal propagating through U58-12 and forcing the U21-7 lead high. After a minimum of three periods of the 16 MHz clock, the U21-15 signal goes high, passes through U59-6, and sets the U68-9 flip-flop. This forces the U58-8 signal high and the XACK* signal at U43-3 low, and the host terminates the session.

5.3.1.7 Read FIFO Memory Session. As shown in Table 5-1, the host may read from the WDC FIFO memory using any one of four consecutive addresses. This allows the host to efficiently use the 68000 MOVEP instruction in reading from the FIFO memory.

The read FIFO memory (IORDRAM) signal goes high when any one of these four addresses is being accessed. This causes the U79-5 flip-flop to be set if the ENHFRD signal is high. The ENHFRD signal is controlled by the microcontroller as bit 2 of the CTRL1, and provides a means of denying host read access of the FIFO memory. Assuming the ENHFRD signal is active when the IORDRAM goes high, the U79-5 flip-flop is set, the IORDREQ* signal is driven low, and a request is generated for the FIFO controller to read a byte of data from the FIFO memory. The mechanism of reading from this memory is discussed later. When the byte of data has been read from memory and gated into the U4 register, the U79-5 flip-flop is reset, which drives the IORDREQ* signal inactive (high). The byte of data in the U4 register is gated onto the IODBUS because the U4-1 lead is driven low by the IORDRAM signal through the U59-8 invertor. The byte is then gated to the D0-D7 leads because the ADRMTCH* signal to U5-19 is low and the IOWRT* signal to U5-1 is high. When the IORDREQ* signal goes high, the U68-5 flip-flop is set, which causes the XACK* lead to be low after the proper delay is introduced by the U21 shift register as discussed above. The host then terminates the session, and the I/O interface returns to a quiescent state.

5.3.1.8 Controller Reset. The WDC is initialized to a reset state when any one of these three conditions exists:

a. WDC +5V power is applied
b. A reset signal is received from the I/O bus (IORES*=low)
c. The host accesses the write reset register.

When the WDC +5 volt is turned off, the C14 capacitor discharges through the CR1 diode towards ground. When the +5 volt is turned on, the C14 capacitor starts charging through resistor R19 to +5 volts. Until C14 is charged up to the threshhold of U20-6, the signal at U20-7 is high. This forces the RESET* signal to be low through U70-1, U59-11, and U43-8, and the WDC is held reset until C14 reaches approximately 1.6 volts. At this time U20-6 goes low, and the RESET* signal is forced high (inactive) through the U70-1, U59-11, and U43-8 path which allows the WDC to begin operation.

0	CONTROLLER SENSE REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
1	CONTROLLER STATUS REGISTER	BUSY	CMD INT.	EXCEP-TION	DATA INT.	DATA REQ.	CMD INT. ENABLE	DMA MODE	DINTEN
2									
3									
4-7	FIFO REGISTER	D7	D6	D5	D4	D3	D2	D1	D0

FIGURE 5-2. I/O Bus Read Registers

The WDC can also be reset through the IORES* signal from the I/O bus. When this signal is low, the RESET* signal is forced low through elements U20-4, U70-1, U59-11, and U43-8. The RESET* signal is active (low) as long as the IORES* signal stays low, and goes inactive when the IORES* goes high.

The third method of activating the RESET* signal is by the host accessing the write reset register.

5.3.1.9 WDC Interrupts to the Host. The WDC is capable of generating two different interrupt requests on the I/O bus: a data interrupt and a command interrupt. Either of these interrupts can be strapped to appear on any of the INT1*-INT4* signal lines. The same interrupt line may be chosen for both interrupts, if desired, because the controller status register reflects the state of each of the interrupts. See Figure 5-2.

The data interrupt has an enable function, DINTEN, associated with it, which must be active in order for a data interrupt to occur. DINTEN is the D0 bit of the controller control register which the host accesses on the I/O bus as shown in Figures 5-2 and 5-3. The enable function is initialized to an inactive state when power is applied and must be activated by the host to permit data interrupts. The data interrupt is used to indicate to the host when the FIFO memory is capable of transferring data with the host.

The DATAREQ* signal is low when the FIFO memory is ready to transfer data with the host. The formation of this signal is discussed later. If the DINTEN signal is low, the U70-13 goes low to force U43-6 low and generate an interrupt to the host over whichever of the INT1*-INT4* lines is selected by the strapping of the J10 header. Both the DATAREQ* and the data interrupt signals are available to the host in the controller status register as shown in Figure 5-3.

The command interrupt request is generated by the microcontroller writing a 0 into the XD6 bit of the CSTAT register. This causes the U60-5 signal to go high, which drives the U43-11 lead to a low and generates an interrupt request on one of the INT1*-INT4* lines according to the strapping pattern on the J10 header. This interrupt is normally generated at the completion of a command.

0	CONTROLLER SENSE REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
1	CONTROLLER CONTROL REGISTER								DINTEN
2	CONTROLLER RESET REGISTER (NOTE)								
3									
4-7	FIFO REGISTER	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: A write of any data pattern to this address causes a controller reset.

FIGURE 5-3. I/O Bus Write Registers

5.3.2 I/O Register Description

The WDC occupies eight sequential addresses on the I/O bus. These addresses may be configured to be any one of 16 different sets of addresses by selecting the appropriate strapping on the J11 header. These addresses are used to access three read only registers as shown in Figure 5-2, and four write only registers as shown in Figure 5-3.

5.3.2.1 Read Registers.

Address 0: Controller sense register. This register is read by the host to obtain detailed information regarding the last command executed by the microcontroller. This information may consist of up to six bytes, each of which is read sequentially from address 0. When the host requests a read of the controller sense register, two flag bits in the microcontroller read registers are updated. The IOCMD/SNS flag (bit 7 of STAT1) becomes active and the IOWRT* flag (bit 6 of STAT1) becomes inactive. If the microcontroller is not busy, it monitors these two flags; when a read sense register is request detected, the microcontroller reads the sense bytes sequentially from internal memory and places them on the I/O bus. If the microcontroller is busy executing a command, these two flags are not monitored and the read request is ignored.

Address 1: Controller Status Register. This register may be read at any time by the host since it does not require microcontroller interaction.

Bit 0. Data Interrupt Enable (DINTEN). This bit serves as an enable to allow an interrupt request to one of the I/O interrupt lines INT1*-INT4* when a data transfer with the FIFO is ready. The particular interrupt line is determined by the strapping option selected for the J10 header. The data interrupt enable bit is controlled by the host when it executes a write into address 1.

Bit 1. DMA Mode. The controller is capable of exchanging data with the host in a direct memory access (DMA) byte-by-byte mode, or the WDC can alert the host when at least 128 bytes may be exchanged. The mode is selected by the host during the command sequence. The DMA bit is active if the host specifies the DMA mode of operation.

Bit 2. Command Interrupt Enable. The host is able to instruct the controller to generate an interrupt to the host upon the completion of a command. If the host selects this option during the command sequence, the controller activates the command interrupt enable bit.

Bit 3. Data Request. The data request bit is active whenever a data transfer with the FIFO is ready. If the controller is functioning in the DMA mode, the data request is active during a disk read operation as long as the FIFO is not empty, and it is active during a disk write operation as long as the FIFO is not full. If the non-DMA mode of operation is used, the data request bit is active during a disk read operation as long as the FIFO contains at least 128 bytes of data. The bit is active during a non-DMA disk write operation as long as the FIFO has room for at least 128 bytes of data. If the data interrupt enable bit (bit 0) is also active, the controller generates an interrupt to the host when the data request bit becomes active.

Bit 4. Data Interrupt. This bit is active whenever both bit 0 (data interrupt enable) and bit 3 (data request) are active. An interrupt is also generated to the host on any one of the INT1*-INT4* lines according to the strapping option used for J10 header.

Bit 5. Exception. The exception bit is active at the conclusion of a command if a malfunction was detected during the execution of the command. It is also activated by any reset signal to the controller, and is deactivated when the self-diagnostic program has terminated successfully.

Bit 6. Command Interrupt. If the host specifies an interrupt at the completion of a command, the controller activates the command interrupt bit when the command is finished. This causes an interrupt on any one of the INT1*-INT4* lines, depending on the strapping pattern on the J10 header.

Bit 7. Busy. The controller activates this signal when a command is being executed and resets it upon completion of the command. Busy is also activated when the controller receives a reset signal, and it remains active until the microcontroller completes the self-diagnostic program. When the busy bit is active, the host cannot communicate with the microcontroller or access any registers which require microcontroller activity.

Addresses 4-7: FIFO Register. The host is permitted to read from the controller FIFO memory if the ENHOSTFIFORD* flag, which is located in the microcontroller write register CTRL1, is active. The microcontroller activates this flag when the host requires read access from the FIFO, and the host may then read from the FIFO memory without requiring any microcontroller interaction. A read from any of the addresses 4 through 7 produces the same results.

5.3.2.2 Write Registers. Address 0. Controller Command Register. This register is used to communicate information from the host to the microcontroller. A write to this address causes the IOCMD/SNS and IOWRT flags on the microcontroller STAT1 read register to become active. These flags are scanned by the microcontroller when it is in its idle mode; when the microcontroller determines the flags are active, it reads the command through its RDIO register. Several bytes of data must be transferred to the controller to specify a command.

Address 1: Controller Control Register.

Bit 0. Data Interrupt Enable. When the bit is active, an interrupt on one of the INT1*-INT4* lines to the host is generated each time the FIFO memory is ready to accept data during a disk write command, or transmit data during a disk read command. If the bit is inactive, no interrupt signal is generated.

Address 2: Controller Reset Register. Any write operation from the host to this address resets the controller and causes the microcontroller self-diagnostic program to be executed. The data pattern sent to the controller is not relevant to the operation.

Addresses 4-7: FIFO Register. The host may write into the FIFO memory if the microcontroller has activated the ENHCSTFIFOWRT* flag which is located in the microcontroller CTRL1 write register. This flag is activated whenever the microcontroller is executing a command which requires the host to have write access to the FIFO memory. A write operation to any of the addresses 4 through 7 produces the same result.

5.3.3 Microcontroller

The basic control for WDC is provided by an 8x305 bipolar microcontroller operating at 250 nsec per cycle. Figure 5-4 depicts the basic elements associated with the microcontroller and the signal buses which interconnect them. The program for the microcontroller is stored in the U84 and U119 bipolar PROM's, which provide up to 2048 addresses of instructions. The microcontroller gates the contents of its internal address register onto the XA0-XA10 bus each cycle, and receives the corresponding 16-bit instruction from the U84 and U119 PROM's. The address on the XA0-XA10 bus is also used to access a microcode instruction in the U118 PROM. This instruction is stored in the U82, U83, U99, and U117 flip-flops each cycle, and is used as an address bus to access the microcontroller registers and RAM. These bits are decoded by U74 to provide enable signals to gate data from the read registers onto the microcontroller XDBUS. The A0-A6 lines are also decoded by U72 and U73 into write strobe signals used to write data from the microcontroller XDBUS into the write A registers and the write B registers. The read registers and the write A and write B registers are described in Figures 5-7, 5-8 and 5-9, respectively. The microcode address lines are also used to access 56 bytes of memory in the RAM, which is located on the XDBUS.

The assignment of the A0-A6 address bus is shown in Figure 5-5. Address $00-07 is not used by the microcontroller. Writing data at any address from $08 to $0F results in the data being deposited both in write B registers and in the RAM. A read operation from these addresses retrieves the data from the RAM, but does not affect the write B registers. This allows the microcontroller to maintain a software copy of the state of the write B registers. Figure 5-9 lists the bit assignment for the write B registers.

Address $10-3F is dedicated to the RAM, and provides general-purpose write/read registers for the microcontroller. The $40-47 address space is used to retrieve data from the read registers during a read operation, and gate data into the write A register during a write operation. Because the microcontroller is capable of performing a read and write operation during the same 250-nsec cycle, data can be read from the read registers and deposited in the write A registers in an efficient manner.

Figure 5-6 depicts the timing relationship of some of the microcontroller signals. A cycle is defined as the 250-nsec period from the falling edge of the MCLK signal to the succeeding falling edge of MCLK. This cycle is divided into a data input phase and a data output phase of approximately equal time duration as shown by the WC+SC signal. When the WC+SC signal is low, the microcontroller expects to receive data from the selected register or RAM on the XDBUS. When the WC+SC signal is high, the data for the selected register on RAM is being driven on the XDBUS by the microcontroller.

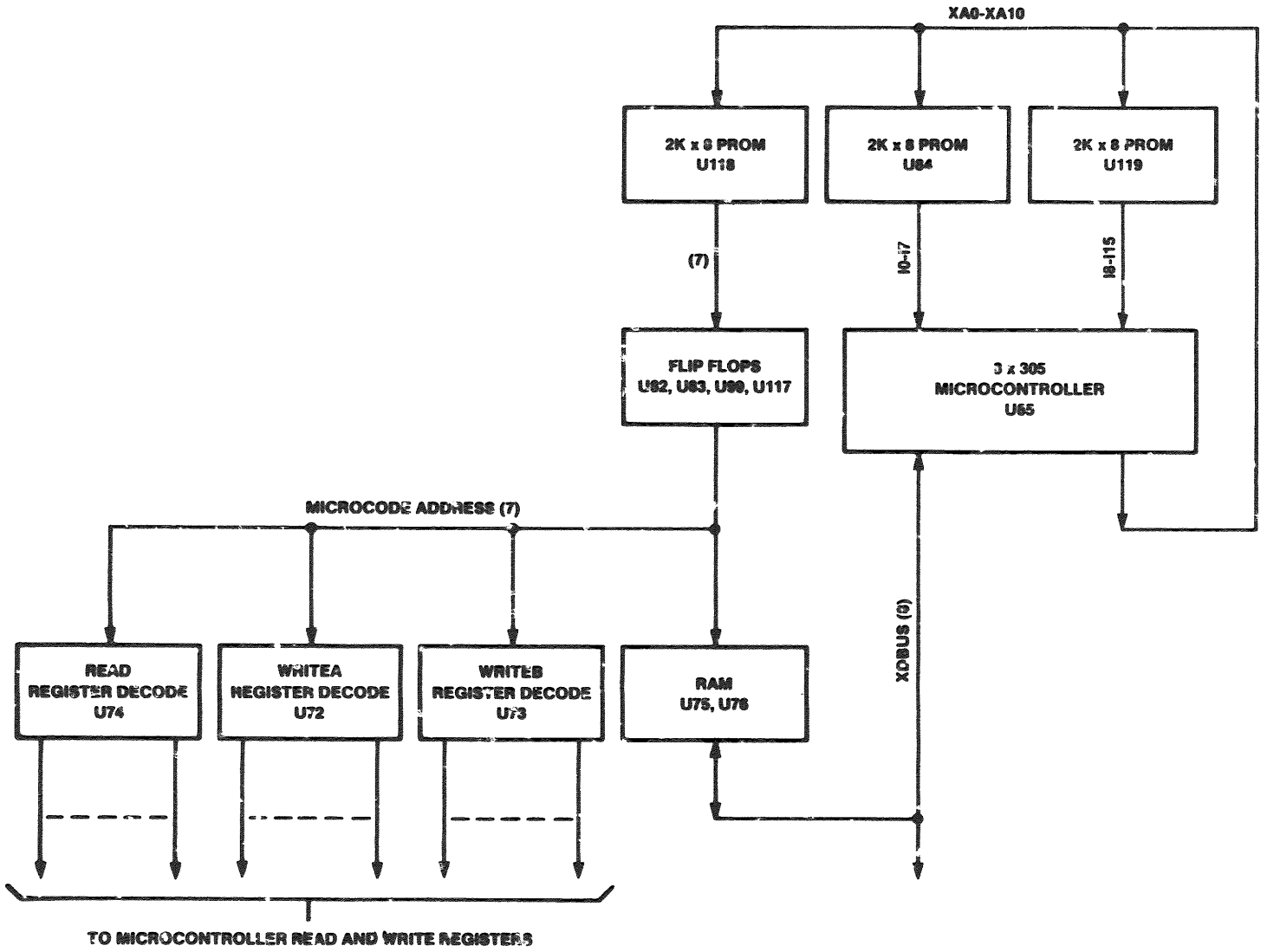


FIGURE 5-4. Microcontroller Bus Structure

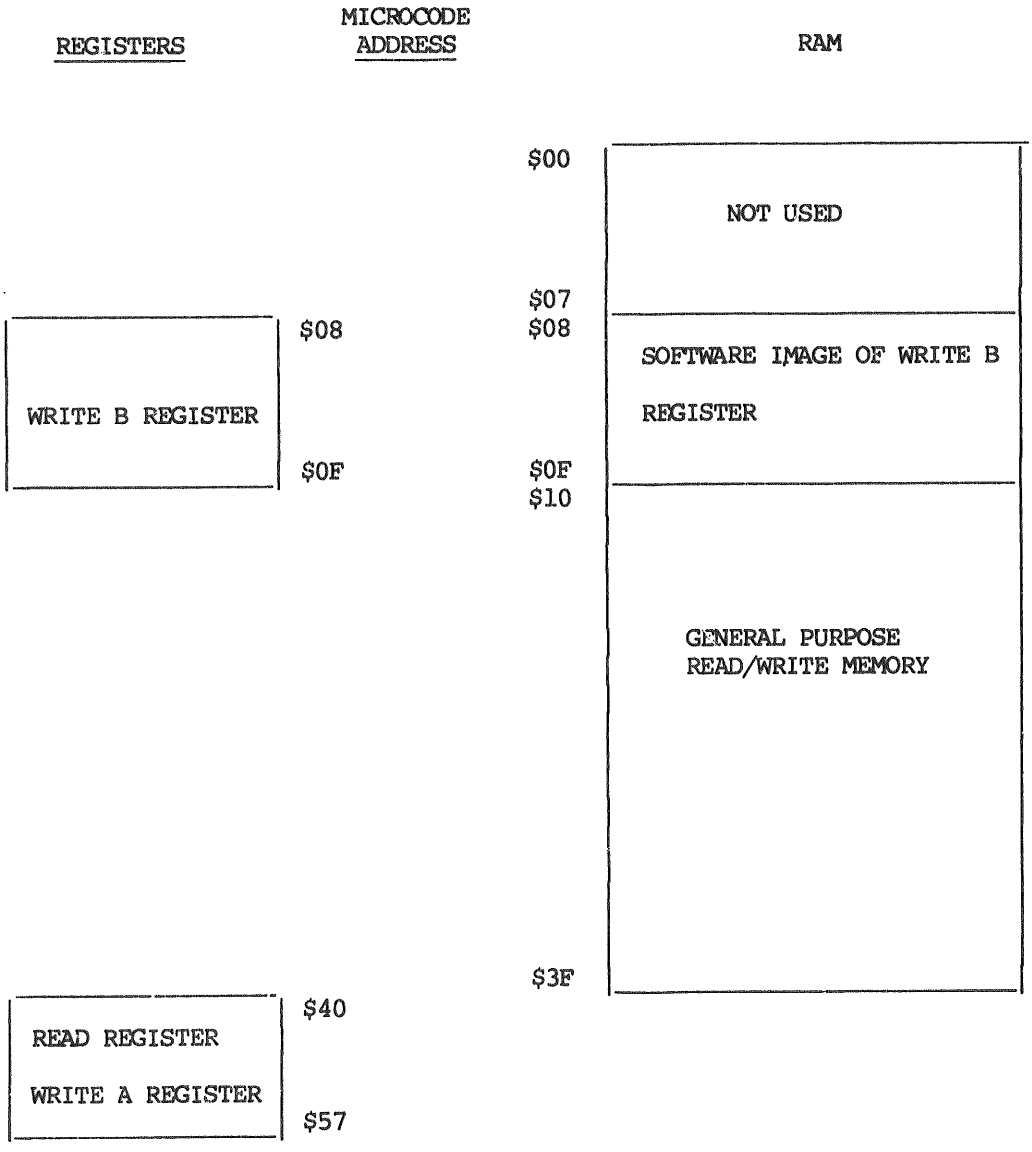


FIGURE 5-5. Microcontroller Address Space

When the U83-9 signal is low, the RAM chips at U75 and U76 are selected. If the signal at U97-8 is high, the RAM chips gate data onto the XDBUS. The timing relationship for the RAM WRT ENABLE pulse at U97-8 is shown in Figure 5-6.

When the microcontroller writes to one of the write B registers, the U82-6, U82-9 and U83-5 signals are all low which drives U73-6 high and U73-4 low to partially enable the U73 decoder. To enable the U98-3 gate, the U73-5 input goes low when the WC+SC signal and the MCLK signal both go high. This causes the output of the U73 which is selected by the U117-9, U99-5, and U99-9 signals to pulse low for the duration of the positive cycle of MCLK. The timing relationship for the pulse is shown in Figure 5-6 as the U73-15 signal. The U72 decoder is accessed in a similar manner when the microcontroller writes to the write A registers, except the U82-5 signal is low.

The U83-8 signal is low when the microcontroller accesses one of the read registers, and this drives the U74-4 decoder enable low. The U74-6 enable is high when the ERDWIN* signal is low, or the WC+SC signal is low through the U98-6 gate. The U74-4 enable is the MCLK function and is active when MCLK goes low. These signals form a pulse on the output of the U74 decoder selected by the U117-9, U99-5, and U99-9 signals. The timing of this pulse is indicated in Figure 5-6, with U74-15 being shown as typical.

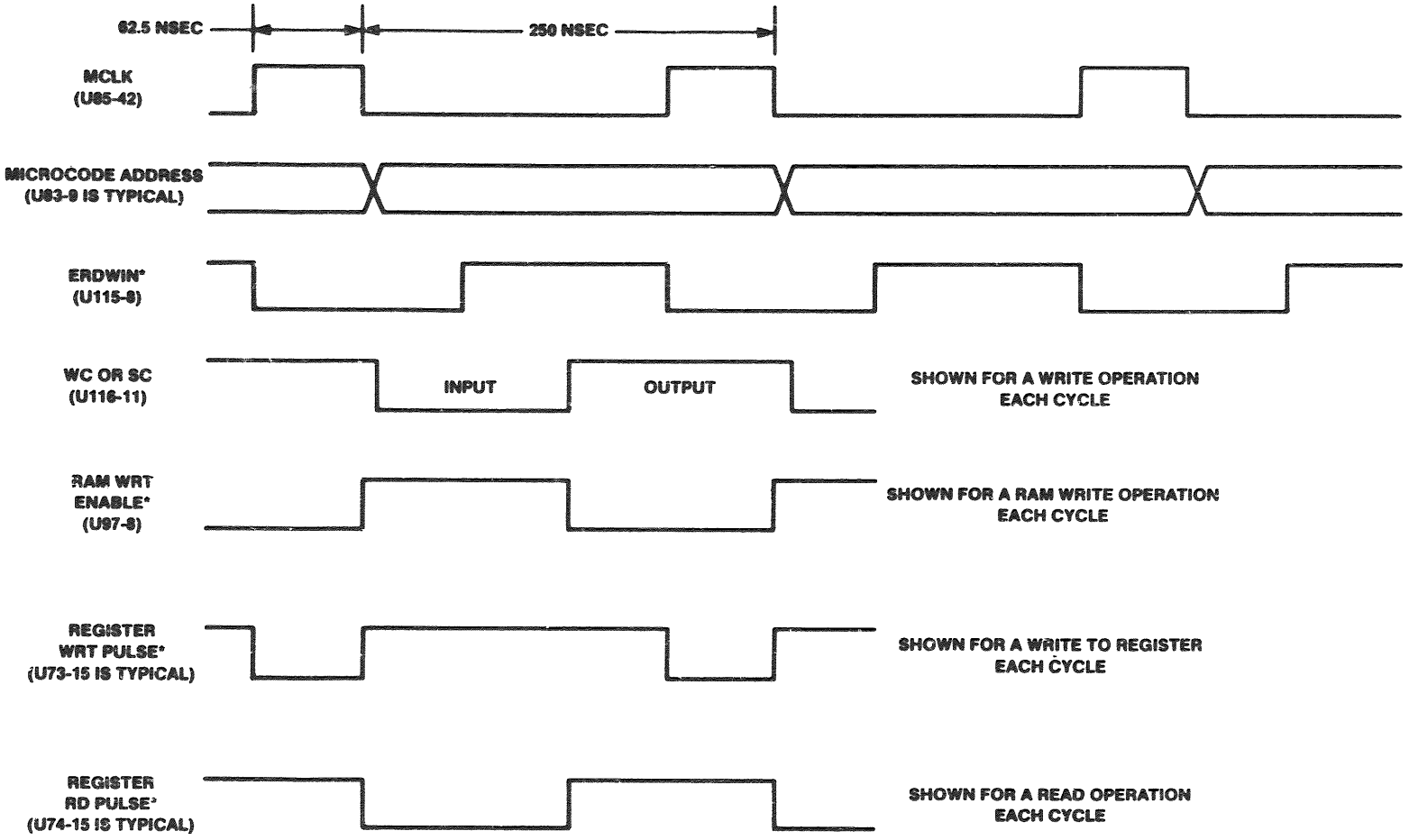


FIGURE 5-6. Composite Microcontroller Cycles

5.3.4 Microcontroller Registers

The microcontroller has access to 8 read registers and 16 write registers in addition to 56 bytes of RAM (see Figures 5-7, 5-8, and 5-9). The address for these registers and the RAM come directly from a PROM as a part of the microcontroller word and are not formed by the microcontroller. As a result, the address cannot be changed during a microcontroller cycle, but remains fixed. To enable the microcontroller to input from one register and output to a different register during the same cycle, the addresses for the eight read registers are the same as for the write A registers.

The addresses assigned to the write B registers are also assigned to the microcontroller RAM. Thus, a read of an address in the range $08-$0F accesses data from the RAM, and a write to any of these addresses writes to both the RAM and the write B register. This creates a fast software image of hardware control registers using a minimum amount of hardware.

5.3.4.1 Read Registers.

Address $40: Switch Register (SWR). The SWR is used to select options which the WDC supports for the various floppy and Winchester disks that are available. The options are selected by strapping the pins on the J16 header. This strapping pattern is input into the microcontroller when a read is performed at address $40. The strapping options are listed in Chapter 2.

Address $41: Status 1 (STAT1).

Bit 0. Seek Complete. This signal being active indicates the selected Winchester drive has completed the requested number of head steps and the head setting time has elapsed.

Bit 1. Write Fault. If a Winchester disk is selected, this bit being active indicates the drive has detected a condition which does not permit a write operation to be performed. If a floppy disk is selected, the bit being active indicates the diskette in the drive is write protected.

Bit 2. Track 0 (TRK00). This signal is active when the selected drive has its head positioned on track 0, which is the track farthest from the hub.

Bit 3. Index F/F. Each time the selected disk completes a revolution, it generates an index pulse to the WDC. This pulse sets the index flip-flop and causes bit 3 to become active. The flip-flop is reset by the microcontroller performing a write to the CTRL2 register with bit 4 being active.

Bit 4. Drive Ready (DRVRDY). This signal is active when the selected drive is capable of executing one of its commands. The 5 1/4 inch mini-floppy drive does not support this signal.

Bit 5. Cartridge Write Protect (CWPROT*). An active low level indicates the selected Winchester drive has the cartridge in a write protected condition.

Bit 6. I/O Bus Write* (IOWRT*). This signal is active whenever the host on the I/O bus is performing a write operation. The microcontroller uses this bit in conjunction with bit 7 to distinguish between a command from the host and a read sense request from the host (see Table 5-1).

Bit 7. I/O Bus Command or Sense (IO CMD/SNS). This signal is active when the host is attempting to transfer a command to the WDC or when it is requesting a read of the WDC sense information. Bit 6 is used to distinguish between the two operations. See below.

Bit 7	Bit 6	Meaning
0	0	No meaning
0	1	No meaning
1	0	Command operation
1	1	Read sense request

Address $42: Read I/O Bus (RDIO). When the microcontroller determines that the host is sending it a command, it reads this address to receive the host data.

Address $43: Status 2 (STAT2)

Bit 0: Winchester Read Data Ready (WINRDDATARDY*). This signal is active during a Winchester disk read command when the read circuitry has assembled a byte of data and transferred it to the read holding register. Bit 0 is forced inactive when the microcontroller reads the byte of data using address $44. Data from the floppy disks is assembled by the floppy disk controller chip; bit 0 is not involved.

Bit 1. Winchester Write Register Ready (WINWRTREGRDY*). This signal is active during a Winchester disk write command when the write buffer register is empty, and it serves as a flag to the microcontroller to write a byte of data to the write buffer at address $45. Performing this write also causes bit 1 to become inactive.

Bit 2. Not used. Always active.

Bit 3. Not used. Always active.

Bit 4. Synch Window (SYNCHWINDOW). This function is active when the READGATE signal is active and the read circuitry detects at least 16 successive zero pulses from the disk. This pattern occurs just prior to an address mark and is used in controlling the phase lock loop circuit and the address detection circuitry.

Bit 5. High Frequency Change (HIFREQCHNG). When the read circuitry detects 16 successive zero pulses pulses from the selected Winchester disk, the SYNCHWINDOW signal becomes active and the HIFREQCHNG signal inactive.

When the first non-zero bit is received from the disk, the HIFREQCHNG signal becomes active. If this change in HIFREQCHNG is caused by an address mark coming from the disk, then WINRDDATARDY* (bit 0) is active approximately a byte time later.

Bit 6. Floppy Disk Controller Data Request (FDCDATAREQ). This signal being active indicates to the microcontroller that the floppy disk controller (FDC) is ready to accept a byte of data from the microcontroller during a write disk operation, or that it has a byte of data ready for the microcontroller to read during a disk read operation.

Bit 7. Floppy Disk Controller Interrupt (FDCINT). This signal is active when the FDC chip generates an interrupt request to the microcontroller. The reason for the interrupt is determined by the microcontroller performing a read of the FDC chip status register.

Address $44: Read Disk Data (RDDISK). This register contains a byte of data received from a Winchester disk each time the WINRDDATARDY* signal (bit 0 of STAT2) is active. As the microcontroller reads the RDDISK register, the WINRDDATARDY* is made inactive in preparation for receiving the next byte of data.

Address $45: Read FIFO Memory Data (RDFIFO). The microcontroller requests a byte of data from the FIFO memory by performing a write to address $45. The FIFO controller then reads the data from FIFO RAM and gates it into a FIFO output register. The microcontroller can read this byte of data through address $45.

Address $46: Read Floppy Disk Data (RDFDD). The microcontroller reads this address to obtain a byte of data which the FDC chip has received from the floppy disk. The FDC informs the microcontroller when each byte has been received.

Address $47: FIFO Memory Counter (FCTR). This address contains information about the amount of data contained in the FIFO memory. The counter is reset to 0 by activating the FIFORESET bit (bit 0 of CTRL2).

Bit 0. FIFO Counter 0* (FCTR0*). When this bit is active, the FIFO memory contains at least 128 bytes of data.

Bit 1. FIFO Counter 1* (FCTR1*). When this bit is active, the FIFO memory contains at least 256 bytes of data.

Bit 2. FIFO Counter 2* (FCTR2*). When this bit is active, the FIFO memory contains at least 512 bytes of data.

Bit 3. FIFO Counter 3* (FCTR3*). When this bit is active, the FIFO memory contains at least 1024 bytes of data.

Bit 4. FIFO Counter 4* (FCTR4*). When this bit is active, the FIFO memory contains at least 2048 bytes of data.

Bit 5. FIFO Full* (FIFOFULL*). This bit will be active when the FIFO memory contains 4096 bytes of data. At this time, bits 0-4 are all inactive.

Bit 6. FIFO Empty* (FIFOEMPTY*). This bit will be active when the FIFO memory contains zero bytes of data. At this time, bits 0-4 are all inactive.

Bit 7. Not used. Always active.

	REGISTER	MSB XD7	XD6	XD5	XD4	XD3	XD2	XD1	LSB XD0
$40	SWR	WD0 BUFF STEP	WD0 CART	WD1 BUFF STEP	WD1 CART	FLOP STP RATE 1	FLOP STP RATE 0	MINI FLOPPY*	48TPI*
$41	STAT1	I/O CMD/ SNS	I/O WRT*	CWPROT*	DRV RDY	INDEX F/F	TRK00	WRT FAULT	SEEK COMPLT
$42	RDIO	D7	D6	D5	D4	D3	D2	D1	D0
$43	STAT2 (NOTE)	FDC INT	FDC DATA REQ	HIGREQ CHNG	SYNCH WINDOW	1	1	WIN WR TREG RDY*	WIN RD DATA RDY*
$44	RDDISK (NOTE)	D7	D6	D5	D4	D3	D2	D1	D0
$45	RDFIFO	D7	D6	D5	D4	D3	D2	D1	D0
$46	RDFDD	D7	D6	D5	D4	D3	D2	D1	D0
$47	FCTR	1	FIFO EMPTY*	FIFO FULL*	FCTR4*	FCTR3*	FCTR2*	FCTR1*	FCTR0*

NOTE: A read from the RDISK register resets the win RDDATA RDY* (XD0 bit of STATUS2 register)

FIGURE 5-7. Microcontroller Read Registers

5.3.4.2 Write A Register. Write A register addresses are discussed below.

Address $40: Not used.

Address $41: Not used.

Address $42: Write to I/O Bus (WRTIO). The microcontroller transmits sense information to the host over the I/O bus by writing the data to a register using this address. Performing this write also causes the XACK* function to the I/O interface to be active. This signals the host to read the register containing the data.

Address $43: Not used.

Address $44: Write to FIFO RAM (WRTFIFO). The microcontroller stores a byte of data in the FIFO RAM by writing into this register.

Address $45: Write to Winchester Disk (WRTDISK). The microcontroller transfers bytes of data to the Winchester disk write circuitry by writing to this address. This write also causes the WINWRTREGRDY* signal (bit 1 of STAT2) to become inactive. The write also causes a FIFO memory read request if the microcontroller right bank (RBANK) signal is active.

Address $46: Write Data to Floppy Disk Controller (WRTFDD). Using this address, the microcontroller transmits data to the FDC for writing to the floppy disks.

5.3.4.3 Write B Register. Write B register addresses are discussed below.

Address $08: Not used.

Address $09: Disk Select (DISKSEL)

Bits 0-3. Drive Select (DRIVESEL0*, 1*, 2*, 3*). These four bits are used to specify which one of four possible drives are to be accessed.

Bits 4-6. Head Select (HEADSEL0*, 1, 2*). When the selected drive is a Winchester unit, these three bits are used to specify up to eight different heads (head 0 through head 7). When a double-sided mini-floppy or floppy disk is used, the HEADSEL0* bit selects which side is accessed.

Bit 7. Low Current (LOWCURRNT*). When this bit is active, it instructs the disk drive to reduce the amount of current used in writing data. This is normally done on the inside half of a disk.

Address $0A: Not used.

Address $0B: Control 1 (CNTRL1):

Bit 0. Direction In (DIRIN*). This signal is used to indicate the desired direction of movement for the disk head during a stepping operation. If the signal is active, the drive is instructed to move the head toward the hub when the step signal is given. If the DIRIN* signal is inactive, the drive moves the head away from the hub when instructed to perform a step.

		MSB XD7	XD6	XD5	XD4	XD3	XD2	XD1	LSB XD0
$40									
$41									
$42	WRTIO (NOTE 1)	D7	D6	D5	D4	D3	D2	D1	D0
$43									
$44	WRTFIFO	D7	D6	D5	D4	D3	D2	D1	D0
$45	WRTDISK (NOTE 2)	D7	D6	D5	D4	D3	D2	D1	D0
$46	WRTFDD	D7	D6	D5	D4	D3	D2	D1	D0
$47									

NOTES:

1. Writing to address $42 activates the XACK* signal to I/O bus.
2. Writing to address $45 resets the WIN WRTREG EMPTY* flag (STATUS2 register bit XD1)

FIGURE 5-8. Microcontroller Write A Registers

Bit 1. Step (STEP*). The drive moves the head in the direction indicated by bit 0 (DIRIN*) when the STEP* signal is activated.

Bit 2. Enable the host to read the FIFO memory (ENHOST FIFORD*). When this signal is active, the host is given access to read the FIFO memory via the I/O bus.

Bit 3. Enable the host to write to the FIFO Memory (ENHOSTFIFOWRT*). When this signal is active, the I/O host is permitted to write data to the FIFO memory.

Bit 4. DMA Interrupt Mode (DMAINTMODE*). This bit controls the mode of transferring data between the FIFO memory and the host on the I/O bus. When bit 4 is active, the DATAREQ signal (bit 3 of the controller status register which the host can read), is active as long as the FIFO memory is capable of handling another byte of data. If the DMAINTMODE* bit is inactive, the DATAREQ signal is active as long as the FIFO memory can handle 128 bytes of data. The microcontroller sets up the MAINTMODE* bit in accordance with the command sequence received from the host; so it is the host who ultimately controls this bit.

Bit 5. Enable Write Precompensation (ENWPCMP*). When this bit is active, particular patterns of data being written to the disk are shifted in time to compensate for a subsequent time shift which occurs on the disk.

Bit 6. Fail (FAIL*). This bit controls the WDC error LED. When this bit is active, the WDC error LED is lit. This occurs each time a reset signal is received by the WDC circuit. This reset causes the self-diagnostic program to run; when it completes successfully, the microcontroller deactivates bit 6 to extinguish the LED.

Bit 7. Motor On (MOTORON*). This bit is used only with mini-floppy disk drives to control the drive motor. When the bit is active, the motor runs; when the bit is inactive, the motor does not run.

Address $0C: Control 2 (CONTRL2)

Bit 0. FIFO Memory Reset (FIFORESET*). When this bit is active, the control for the FIFO memory and the associated counters are reset. The FIFOEMPTY* signal (bit 6 of FCTR) becomes active and any data in the FIFO memory is lost.

Bit 1. Set Address Mark Request (SETAM). When the WDC writes any information on a Winchester disk, it must preface the information with an address mark to enable it to be read at a later time. Bit 1 is toggled active and then inactive to request an address mark to be written to the disk. The microcontroller then writes a 1 to the WRTDISK register, and an address mark is then written on the disk by the write circuitry.

Bit 2. Address Mark Search (AMSRCH). When this bit is active, the data separator and the address mark detector in the read circuitry are enabled. Both of these functions are disabled when the AMSRCH bit is inactive.

Bit 3. ECC Time (ECCTIME). The WDC forms a 32-bit ECC character over each sector of data as it is written on the Winchester disk. These four bytes of ECC are then written at the end of the data. The ECCTIME signal is used during the write operation to gate the ECC bytes to the disk. During a read operation, the WDC forms an ECC over the data which is read from the disk. Then, as the 32-bit ECC character from the disk is being read, the microcontroller activates the ECCTIME signal. This causes a bit-by-bit comparison of the two ECC characters, and the results are examined by the microcontroller.

Bit 4. Index Flip-Flop Reset (INDEXFFRESET). During each revolution of the selected disk (floppy or Winchester), the disk generates an index pulse. This pulse sets a flip-flop which the microcontroller can read as bit 3 of the STAT1 register. After the microcontroller finds the INDEXFF bit in an active state, it resets the flip-flop by pulsing the INDEXFFRESET signal.

Bit 5. ECC Reset (ECCRESET). When this bit is active, the 32-bit ECC character is clamped to a reset state.

Bit 6. Write Gate (WRTGATE*). This bit is an enable signal to control writing of data to a Winchester disk. When it is active, the WDC write circuitry is enabled, and the selected Winchester disk has its internal WRT GATE signal activated.

Bit 7. Read Gate* (READGATE*). This bit functions as a read enable to the WDC disk read circuitry. When it is active, the data from the selected Winchester disk is examined to find the start of a sector of data. When it is inactive, no Winchester disk data is examined.

Address $0D: Controller Status (CSTAT). This register is used to transfer status information from the microcontroller to the host on the I/O bus. The host can input this status by reading from address 1 of the I/O bus addresses assigned to the WDC. In addition to the status bits updated by the microcontroller, the host also can read through status bits at address 1 which are directly from WDC hardware.

Bit 0. Not used.

Bit 1. Direct memory access mode (DMAMODE) (see paragraph 5.3.2.1).

Bit 2. Command interrupt enable (CMDINTENABLE) (see paragraph 5.3.2.1).

Bit 3. Not used.

Bit 4. Not used.

Bit 5. Exception (see paragraph 5.3.2.1).

Bit 6. Command interrupt* (CMDINT*) (see paragraph 5.3.2.1).

Bit 7. Busy (see paragraph 5.3.2.1).

Address $0E: Write to the Floppy Disk Controller (WRTFDC). The floppy disk controller (FDC) chip is used to provide the parallel-to-serial conversion of data during a floppy disk write operation, and the serial-to-parallel conversion and address recognition during a floppy disk read operation. The WRTFDC register provides the microcontroller with the access it needs to control the FDC chip.

Bit 0. Floppy Disk Controller Reset (FDCRESET). When this bit is active, the FDC chip is clamped to a reset state.

Bit 1. Floppy Disk Controller Address 0 (FDCADR0). When this bit is active, the internal data register of the FDC chip may be accessed. The status register may be accessed when the bit is inactive.

Bit 2. Floppy Disk Controller Read (FDCRD*). When this bit is active, the direction of data transfer is from the FDC chip to the microcontroller.

Bit 3. Floppy Disk Controller Write (FDCWRT*). When this bit is active, the direction of data transfer is from the microcontroller to the FDC chip.

Bit 4. Floppy Disk Controller DMA Acknowledge (FDCDACK*). Data is transferred between the microcontroller and the FDC chip in what appears to the FDC chip to be a DMA mode of operation. As a result, the FDCDACK* line must be active whenever the microcontroller activates the FDCRD* or FDCWRT* line during a data transfer.

Bit 5. Floppy Disk Controller Terminal Count (FDCTC). When this bit is active, it indicates to the FDC chip that the present data transfer is completed.

Address $0F: Not used.

	REGISTER	MSB XD7	XD6	XD5	XD4	XD3	XD2	XD1	LSB XD0
$08									
$09	DISKSEL	LOW CURRNT*	HEAD SEL2*	HEAD SEL1* (NOTE1)	HEAD SEL0*	DRIVE SEL3*	DRIVE SEL2*	DRIVE SEL1*	DRIVE SEL0*
$0A									
$0B	CTRL1	MOTOR ON* (NOTE2)	FAIL (LED)	EN WPCMP*	DMA INT MODE*	EN HOST FIFO WT*	EN HOST FIFO RD*	STEP*	DIR IN*
$0C	CTRL2	READ GATE*	WRT GATE*	ECC RESET	INDEX F/F RESET	ECC TIME	AM SRCH	SET AM	FIFO RESET
$0D	CSTAT	BUSY	CMD INT*	EXCEP-TION			CMD INT ENABLE	DMA MODE	
$40E	WRTFDC			FDC TC	FDC DACK*	FDC WRT*	FDC RD*	FDC ADRO	FDC RESET
$0F									

NOTES:

1. Bit XD5 address $09 is HEAD LOAD* when an 8 inch floppy DSK is being controlled.
2. Bit XD7 of address $0B is used for 5-1/4 inch floppy only.

FIGURE 5-9. Micrccontroller Write B Registers

5.3.5 FIFO Memory and Control

The WDC contains 4096 bytes of RAM and control circuitry which allows this RAM to be accessed as a FIFO memory. This FIFO memory can be accessed by the microcontroller over the XDBUS or by the host over the IODBUS. The memory consists of two static RAM chips (U45 and U46), each capable of storing 2048 bytes of data, and the control is provided by an 8x60 FIFO RAM controller (FRC) at U44. The FRC detects requests for read or write accesses to the RAM, arbitrates between them, and furnishes the appropriate address to the RAM. It also determines when the RAM is completely full or entirely empty.

5.3.5.1 Read FIFO Memory (IORDRAM). When the host accesses the read FIFO memory address on the I/O bus, the IORDRAM signal is driven high and the U79-5 flip-flop is set. This causes the U81-1 signal to go low and initiates a read FIFO memory request to the FRC (U44). If the FRC is not processing a write request, the U44-3 signal is high and the read request is honored. Figure 5-10 indicates the sequence of signals that occur when the read request is processed. The FRC gates the contents of its internal read address counter to the RAM address leads and then drives U44-8 (RD*) low to enable the outputs of the U45 and U46 RAM chips. Only one of the RAM elements has its chip select input active at a time. This selection is based on the most significant address line U44-15 through the U133-6 and U133-8 elements. When U44-8 goes low, it also removes the reset signal at U71-12 and enables the 16 MHz clock to the U71 counter through the U133-3 and U64-6 elements. As that portion of the counter advances, the RCTB signal becomes active (high) and decrements the U130, U129, and U128 up/down counter. This 12-bit counter is incremented each time a byte is written into the FIFO memory, and is decremented each time a byte is read from the memory. Therefore, it maintains a count of the number of bytes in the FIFO memory. The up/down counter is clocked at 16 MHz, using an inverted OSC16 signal to allow a single count to occur during each passage of the RCTB or WCTB signals. When the U71 counter advances to the U71-9 signal output high, at least 187 nsec have elapsed since the RAM address was asserted, and the byte being read from RAM is present on the FD0*-FD7* signal lines. The U71-9 signal strobes this byte into the U4 and U25 registers, and also resets the U79 source flip-flops through the U70-4 gate. This removes the read request at U44-4 so the FRC drives the U44-8 lead high and resets the U71 counter. The RAM address lines are put into a high impedance state and the read cycle is completed. The data from the U4 register is read by the host.

The microcontroller can generate a FIFO memory read request by performing a write to the WRTDISK register ($45) with the RBANK signal high. This sets U79-9 flip-flop and causes data from the FIFO memory to be strobed into the U4 and U25 registers as described above. The microcontroller reads this data by performing a read of the RDFIFO register ($45) which activates the XFIFORD* signal and gates the byte onto the XDBUS.

5.3.5.2 Write FIFO Memory (IOWRTRAM). The IOWRTRAM signal is driven high when the host writes to the write FIFO memory address on the I/O bus. This causes the U80-5 flip-flop to be set if the ENHFWRT signal is active and if the data from the I/O bus is gated into the U3 register. The flip-flop being set causes the U81-4 signal to go low and activates a write FIFO memory request to the FRC. If the FRC is not performing a read request, U44-4 is high and the FRC processes the write request. If the U44-4 signal is low, the write request is honored after the read operation is completed and when the U44-4 signal is high. The sequence of signals which occurs during the operation of a FIFO memory write is shown in Figure 5-10. The FRC gates the contents of its internal write address

counter to the RAM address to provide the U45 and U46 RAM chips with an address. The most significant address line, U44-15, is used as the RAM chip enable, and it makes a selection between the two RAM chips through the U133-6 and U133-8 elements. If the U44-15 signal is low, the U46 RAM is selected; if the U44-15 signal is high, the U45 RAM is accessed. After the address is established, the FRC drives the U44-7 signal (WRT) low, which removes the reset signal from U71-1 and enables the 16 MHz signal to the U71 counter through U133-3 and U64-6 to allow that portion of the counter to increment. As the counter advances, the U71-4 signal (WCTB) becomes high and causes the U130, U129, and U128 up/down counter to be incremented by one. At the same time, the U64-11 gate goes low and gates the host write data (which is stored in the U3 register) onto the FD0*-FD7* signal lines. The WCTB signal being high drives U96-10 low and activates the write enable signal to the RAM chips. The data on the FD0*-FD7* leads are written into the selected RAM chip. When the counter output U71-5 becomes high, the U80 flip-flops are reset, and the write request on U44-3 becomes inactive (high). The FRC then drives the U44-7 (WRT) signal high, the U71 counter is reset, and the write cycle is completed.

The microcontroller requests a write into FIFO memory by performing a write into the WRT FIFO register ($44). This forces the FIFOWRT* signal low and sets the U80-9 flip-flop, which strobes the byte of data from the XDBUS into the U24 register. It also drives the U44-3 signal lead low to request the FRC to perform a write into the FIFO memory. The sequence is identical to that just described for the host writing into FIFO memory except gate U64-3 is enabled and the byte from the U24 register is written into the selected RAM chip.

After the U130, U129, and U128 up/down counter has been incremented or decremented, its five most significant bits, the AND of these bits, and the OR of these bits are strobed into the U124 register. The U131-9 flip-flop creates the strobe signal after the counter has had time to become stable. The AND function of the five bits is formed using the U55-11 and U126-8 gates. If the inputs to these gates are all high, the signal gated into the U124-12 register is low. When the signal is low, the FIFO memory does not have room to receive a 128-byte block of data from the I/O host, and the DATAREQ* signal at U125-8 is high. The signal at U124-12 is high if the FIFO memory has room for a 128-byte block of data from the host. The DATAREQ* signal is low because it is enabled by U125-9 and U125-10 both being high. The OR function of the five most significant bits from the up/down counters is formed by the U127-6 and U65-4 elements. The signal at U124-7 is high if the FIFO memory contains at least 128 bytes of data. This is used to form the DATAREQ* signal when the host is reading data from the FIFO memory. The DATAREQ* signal is low (active) when the FIFO memory contains at least 128 bytes of data; it is high if less than 128 bytes of data are stored in the memory. The five most significant bits of the up/down counter (as stored in the U124 register), along with the EMPTY and FULL indicators from the FRC, are strobed into the U123 register with the rising edge of the MCLKA signal. This timing is selected so that the signals are stable during the input phase of the microcontroller cycle. The microcontroller inputs this data by reading from the FCTR register ($47), which causes the FIFOCTRRD* signal to be low and gates the contents of U123 onto the XDBUS. The microcontroller uses the state of the up/down counter to determine whether there is sufficient data in the FIFO memory to transfer an entire sector of data.

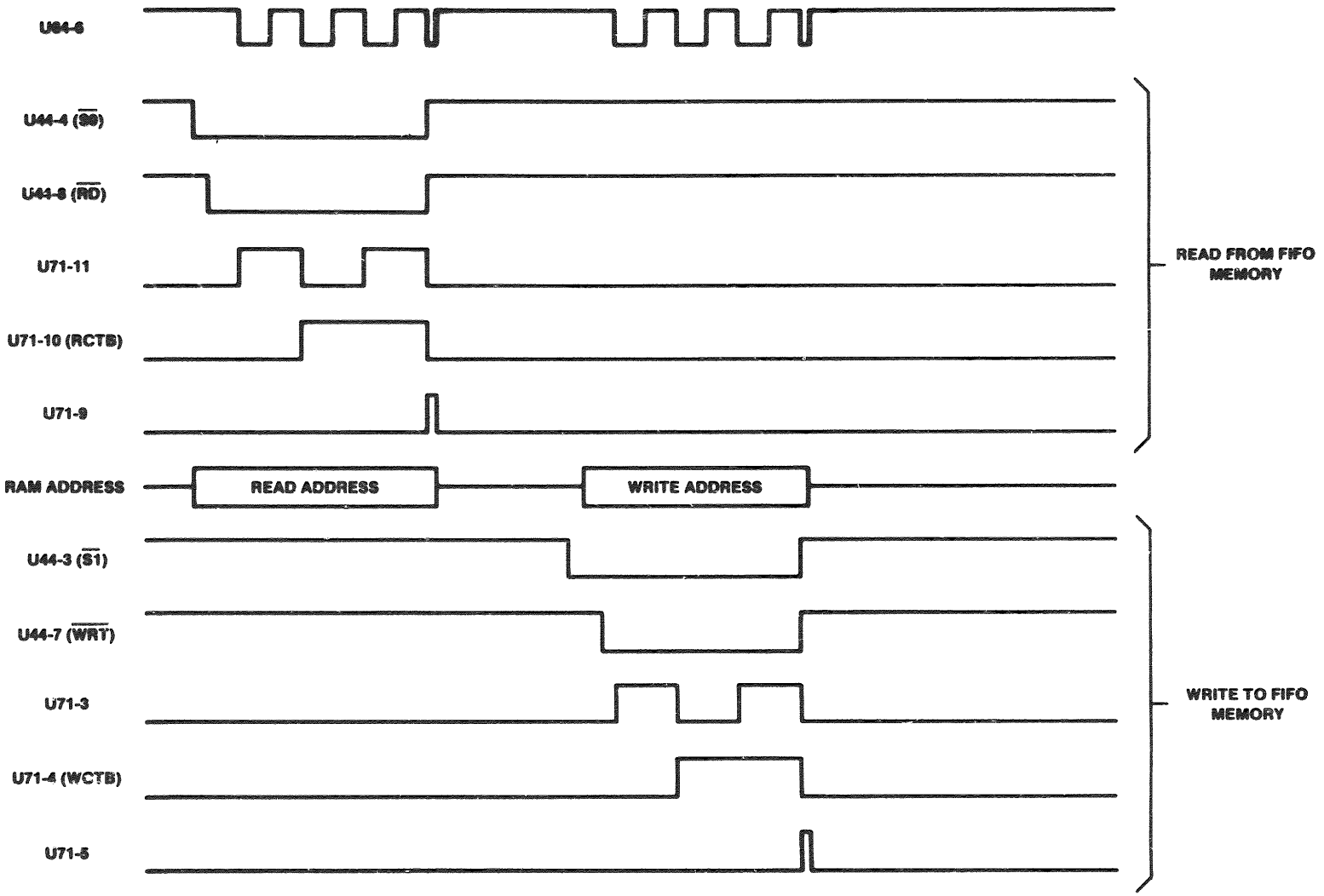


FIGURE 5-10. FIFO Memory Sequence

5.3.6 Connections to Disk Drives

The WDC supports two disk drives in the VME/10 -- a 5-1/4 inch Winchester drive and a 5-1/4 inch flexible disk drive.

Figure 5-11 illustrates the interconnection between the drives and the WDC. The 50-pin header J3 provides connection to the Winchester drive through a special 34-conductor cable. A separate 20-conductor cable is also required for the Winchester drive. The flexible disk drive is interconnected through header J6.

The WDC maintains control of the disk drives through the signal lines in the cables. The microcontroller monitors disk drive status by performing a read of the STAT1 register ($41). This forces the XSTATIRD* low and gates the contents of the U26, register onto the XDBUS where the microcontroller reads them. The microcontroller controls the disk drives by writing into DISKSEL register ($09), and the CTRL1 register ($0B). This gates data from the XDBUS into the U27 and U28 registers using the DSKSELWRT* and CTRL1WRT* signals, respectively. The bit assignment and function of these registers is discussed in paragraph 5.3.4.

5.3.7 Winchester Write Logic

Data is written to a Winchester disk under ccontrol of the microcontroller, using circuitry depicted in Figure 5-12. The data to be written is gated by the microcontroller from the XDBUS to a circuit which converts the parallel data into a serial form. The circuit informs the microcontroller each time a new byte of data is needed to ensure a continuous stream of serial data. The parallel data may originate from the FIFO memory, the microcontroller RAM, or be generated by the microcontroller. The serial data is converted into a standard modified frequency modulation (MFM) code by the MFM generator circuits. The MFM data generation may be altered under microcontroller control to produce a unqiue code, called an address mark, which is used in recognizing and retrieving a block of data from the disk. The MFM data stream is next examined by circuitry to find data patterns which cause a shift in time of the data stream when it is read back from the disk. A compensating shift in time is applied to the data bits in these patterns in the opposite direction so that when they are later retrieved, they are the proper time relationship. This is called precompensation. The data is then transmitted to the selected Winchester disk in a differential mode by a line driver circuit.

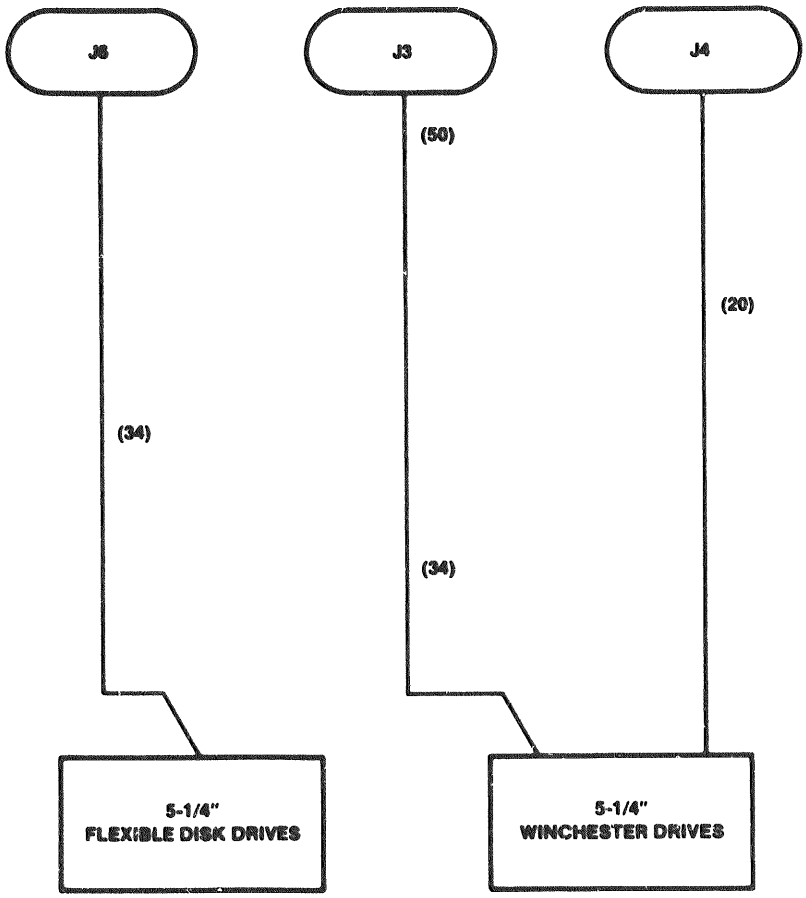


FIGURE 5-11. Disk Interconnect Cables

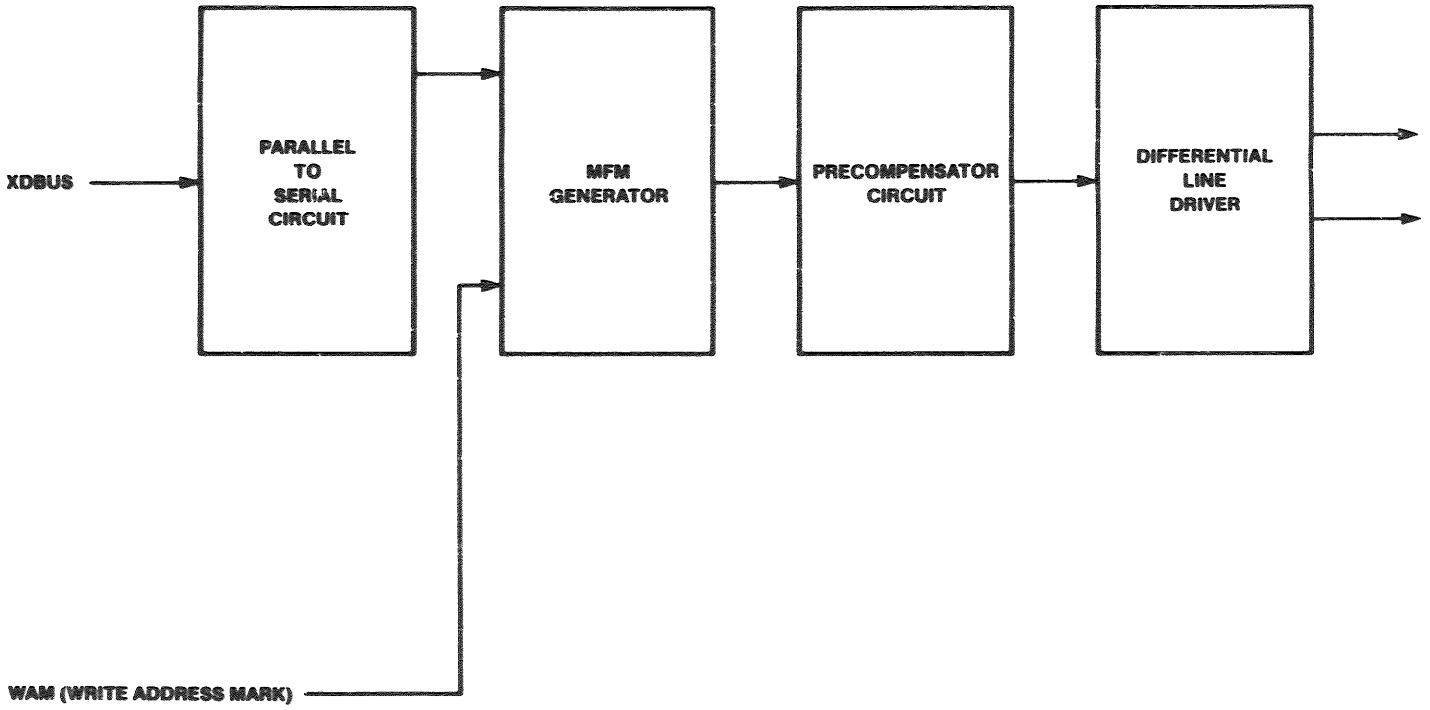


FIGURE 5-12. Write Circuit Block Diagram

5.3.7.1 Detailed Operation. The parallel-to-serial conversion of data is performed by the U33, U34, and U12 elements. The initial condition for the circuit is for the WRTGATE signal to be low, which resets the U12 counter and forces the U34-15 signal high. This puts the U34 device in a serial shift mode with input data being a high at U34-1, and the WDATA* signal at U34-13 also being a high. Prior to writing to a Winchester disk, the microcontroller writes a byte of data (usually $00) into the U33 register by performing a write into the WRTDISK register ($45). It then forces the WRTGATE signal high by writing a zero into the XD6 bit of the CTRL2 register $(0C). The WRTGATE signal also goes to the selected Winchester disk and commands it to start writing data on the disk. The data is initially a data stream of all 0's because the WDATA* signal is inactive (high). When the U12 counter reaches $F, the U12-15 signal goes high. On the next rising edge of the WRTCLK signal, U12 is preset to $8 and the byte of data from U33 is loaded into U34 to be serially shifted to the disk. At the same time, the U11-5 flip-flop is set, and the WREGRDY signal to the XD1 bit of the STAT2 register ($43) is high. This signal is a flag to the microcontroller, indicating the U33 register is ready to receive the next byte of data. The U11-5 flip-flop is reset through the XDISKWRT* signal each time a byte of data is loaded into the U33 register.

The serial data from the U34 shift register (WDATA*) is inverted through the U35-6 AND/OR gate, and is introduced into the U53 serial-to-parallel shift register, where it is shifted by the WRTCLK signal as long as the WRTGATE signal is high. The data from the U53-5 and U53-4 outputs are used to form an MFM coded signal, using the U51-6 element and the U61-9 flip-flop. An MFM data cell is one period of the WRTCLK signal, which is two periods of the 2WRTCLK. The U61-9 flip-flop is updated twice during each cell by the 2WRTCLK at U61-11. The U61-8 lead is driven high in the first half of a cell if a 1 is to be written on the disk. The U61-8 lead is driven high in the second half of a cell if a clock bit is to be written on the disk. A clock bit is written in a cell if the data for that cell is a 0 and the data for the next cell is also a 0. The U51-4 signal is high if a 1 is to be written in a cell and the U51-5 signal is high during the positive portion of the WRTCLK period. When these two conditions occur simultaneously, the U61-12 signal is low, and the U61-8 signal goes high on the next rising edge of the 2WRTCLK signal to cause an MFM one bit to be sent to the disk. If both U53-5 and U53-4 signals are low, a clock pulse is to be written to the disk and the U51-2 signal will be high. The U51-3 signal is high during the negative portion of the WRTCLK signal as long as the U55-8 signal is low. The U61-8 signal goes high with the rising edge of the 2WRTCLK signal, and an MFM clock bit is sent to the disk. The U55-8 signal is low except during a particular cell when an address mark is being written.

An address mark consists of an $A1 data byte being written on the disk with a deliberate violation of the MFM code. Figure 5-13 shows a data byte of $A1 and the resulting normal MFM code which is generated. The data bits, when present, are in the first part of the cell; the clock bits, when present, are in the second part of the cell. Also shown is the pattern generated when an address mark is to be written to the disk. Note that the two patterns are the same except the clock bit in cell 5 of the address mark is missing. This creates a unique pattern on the disk, which may later be detected by special read circuitry. When an address mark is to be written to the disk, the microcontroller sets the U11-9 flip-flop by writing a 1 into the XD1 bit of the CTRL2 register ($0C). As long as the U53 shift register contains $00, the U55-9 signal is low and the state of the U11-9 flip flop has no effect. When

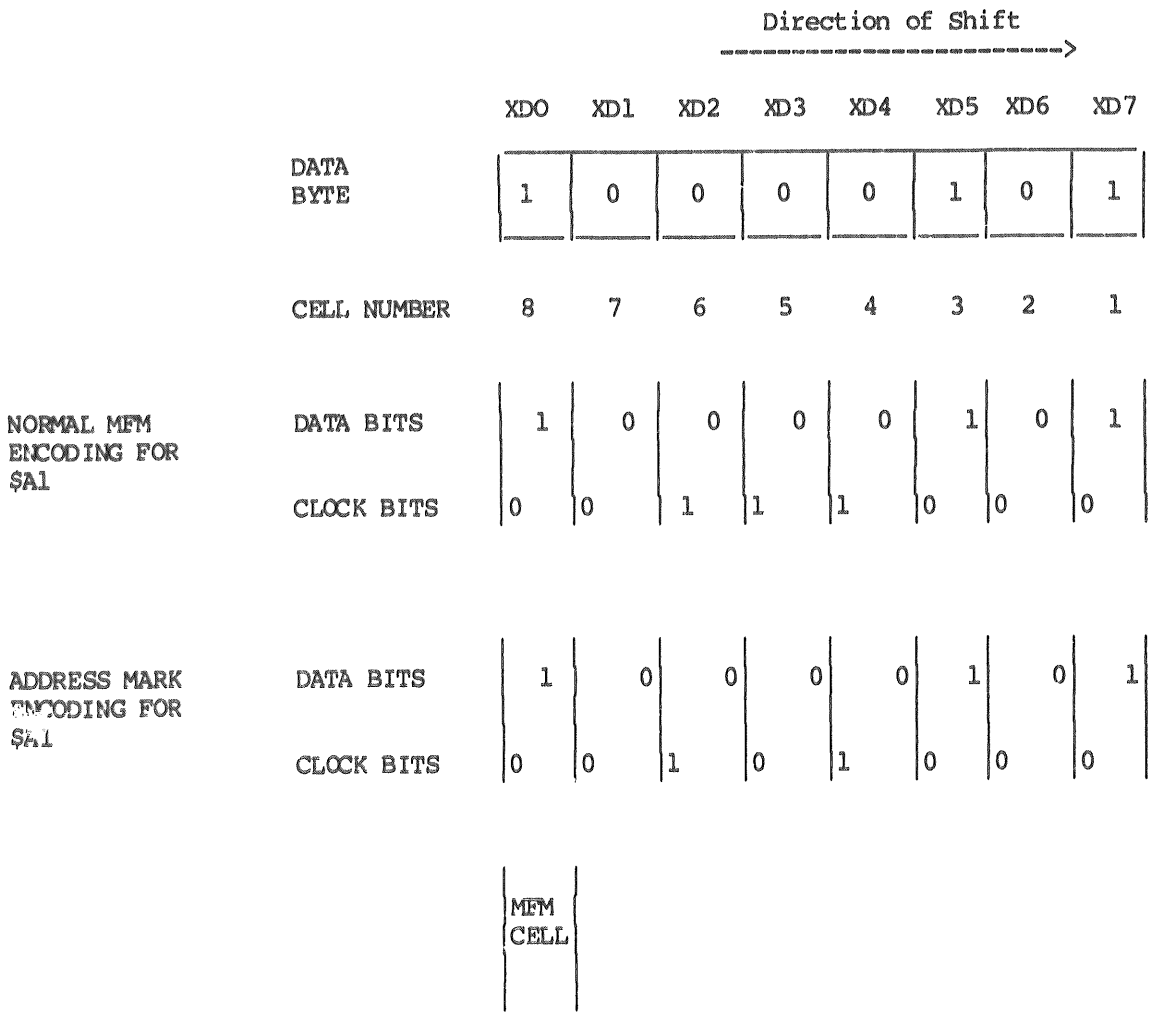


FIGURE 5-13. Address Mark Generation

the $A1 byte is shifted into U53, the first four cells of MFM data are formed normally. However, when data for the fifth cell is to be generated, the U53-12 signal is high, which forces the U55-8 signal high and inhibits the U52-4 gate. This prevents the MFM generator from causing a clock bit to be written in cell 5. On the next rising edge of the WRTCLK signal, the U53-13 signal goes high and resets the U11-98 flip-flop to disable the U55-8 gate and allow normal code generation to occur.

The data bit patterns which require a precompensating shift in time and the direction of this shift are shown in Table 5-2. The U35-8 element detects those patterns which require being written earlier than normal; the U51-8 elements detects the patterns which must be written later than the normal time. These signals are gated into the U13 flip-flops on each rising edge of the 2WRTCLK signal. The 2WRTCLK signal is delayed by 12 nsec through the DL1-12 delay line and is then used to sample the MFM data on U14-5 and the early signal on U14-6. If these two signals are both high, the U14-8 signal goes low and the MFM data (or clock) bit is sent to the disk 12 nsec before the normal time. The 2WRTCLK signal is delayed another 12 nsec through the DL1-10 delay line, and is used to test for a data (or clock) bit to be written at the normal time. If this is true, the U13 flip-flops are set and the U14-1 and U14-12 leads are high to enable U14-8 at the normal time. The 2WRTCLK is delayed for 12 more nsec through the DL1-8 delay line, and is used to test the MFM data (or clock) bit for a late pattern using U14-2 and U14-3. If a late pattern is detected, the U52-11 signal is low, and if an MFM bit (data or clock) is written, the U52-12 signal is also low to force U52-13 high. This forces the U14-8 signal low and the MFM bit is sent to the disk 12 nsec later than normal time. The precompensation circuitry may be disabled by writing a 0 into the XD5 bit of the CTRL1 register ($0B). This forces the ENWPCMP* signal low, which causes the U13 flip-flops to both be set and only the path for normal timing is permitted. Write precompensation is typically enabled only on the inner half of the disk. The MFM data is transmitted to the Winchester disks through the U15 differential driver.

TABLE 5-2. Write Precompensation

(U53-3) 2nd to be Written	(U53-4) Next to be Written	(U53-5) Bit Being Written	(U53-6) Bit Previously Written	Direction of Shift BY PRECOMP CKT
0	0	1	1	EARLY
1	0	1	1	EARLY
1	0	0	0	EARLY
0	1	1	0	LATE
1	1	1	0	LATE
0	0	0	1	LATE

5.3.8 Winchester Read Logic

Figure 5-14 shows the format used to store one section of information on a Winchester disk. The pattern is repeated for a total of 32 sectors on each track. The sector consists of an identification (ID) field and a data field, where the ID field contains the cylinder, head, and sector numbers which permit unique identification of a sector. Each field is prefaced by a 12-byte sync character which is used by a phase lock loop (PLL) circuit to achieve bit synchronization. The next byte in each field is an $A1 address mark, which is written on the disk with a missing clock bit in violation of the normal MFM encoding. This unique character is used by the disk read circuit to achieve byte synchronization. The third character is different in each field, which allows the microcontroller to determine which of the two fields is being read. The ID field also contains information specifying the cylinder, head, and sector to be uniquely recognized. The data field contains 256 bytes of data and both fields then have an ECC character which allows error control over the disk information. The next byte in each field is used as a write splice area, and the final character in the data field provides space for speed variation and write recovery time.

Figure 5-15 depicts the logical functions which are used to accept MFM encoded information from a Winchester disk and separate it into NRZ (nonreturn to zero) data and clock bits. The phase comparator, filter, and voltage controlled oscillator (VCO) form a phase locked loop circuit which is used to track the MFM disk information. The frequency of the read disk oscillator (RDOSC*) signal is controlled by the VCO. The phase of the RDOSC* signal is compared against the phase of the other input to the phase comparator. If the phase of the RDOSC* signal leads the phase of the other signal, the pump down (PMPDN) signal becomes active, and the VCO decreases the frequency of the RDOSC* signal. Similarly, the pump up (PMPUP) signal becomes active if the phase of the RDOSC* signal lags the phase of the other signal and the VCO increases the frequency of the RDOSC* signal. Continuous operation of the PLL results in the RDOSC* signal being of the same phase as the other input to the phase comparator. The ENABLE lead to the phase comparator permits a comparison and subsequent increase or decrease of the RDOSC* signal only when a bit is present on the output of the MUX. The DELAY element is provided so the enable occurs prior to the arrival of the bit at the comparator input.

The PLL circuit provides a continuous clock signal which can be synched with another signal which has a constant frequency but has pulses missing. In MFM encoding, the resulting signal appears as a signal with a given frequency but with many missing pulses. The data stream may be decoded synchronously using the continuously running clock from the PLL to separate the data and clock bits, and forming the data bits into bytes using a shift register.

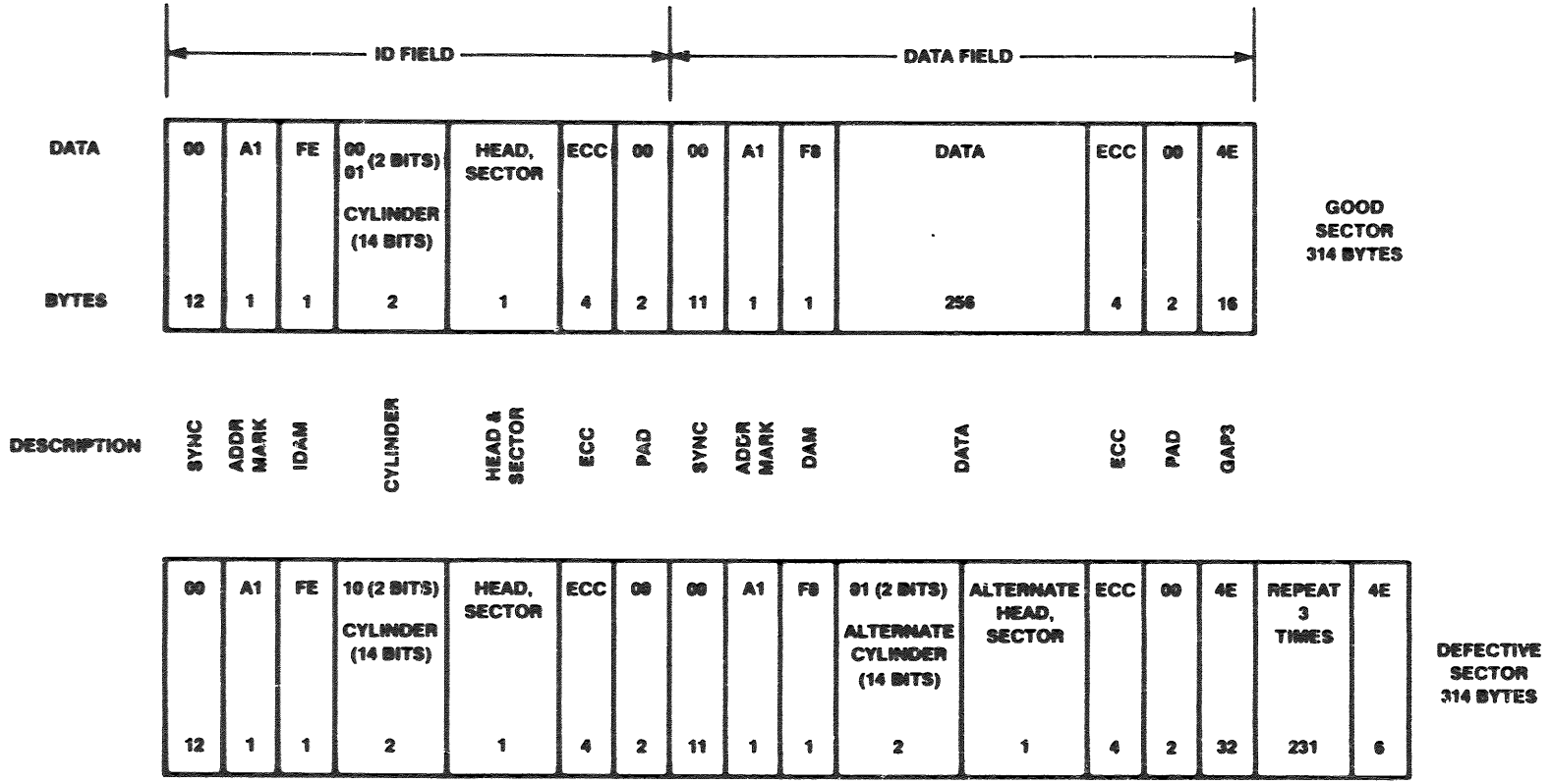


FIGURE 5-14. Format for Each Sector

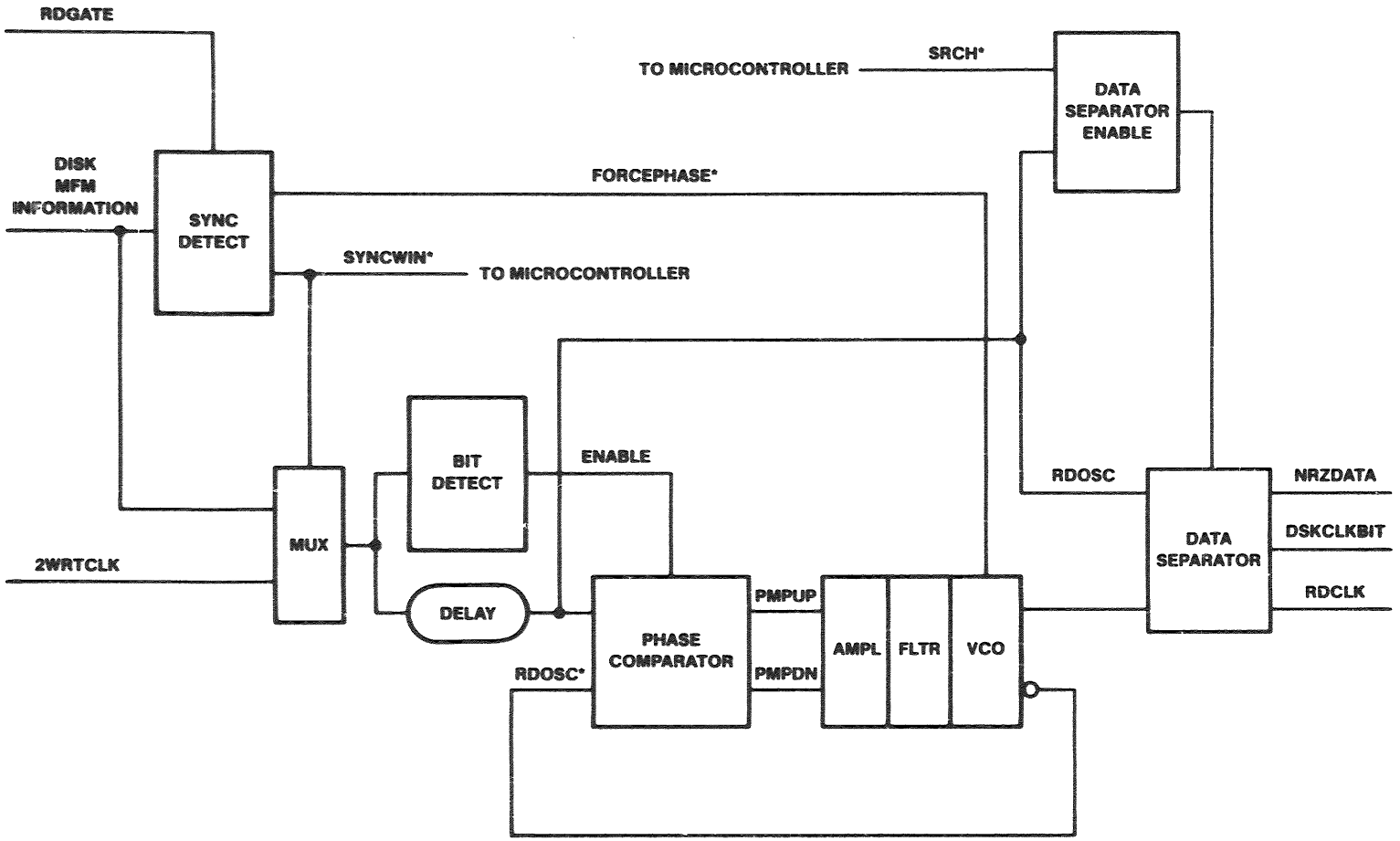


FIGURE 5-15. Disk Data Read Logic

The read gate (RDGATE) signal from the microcontroller is initially inactive, which inhibits the sync detect (sync character detection) function and gates the 2WRTCLK signal through the MUX (multiplexor) and delay functions to the phase comparator. Thus, the RDOSC* signal is initially of the same frequency and phase as the delayed 2WRTCLK signal. The MFM information from the disk appears at this frequency, but with many missing pulses. Although the MFM information was written to the disk at the WRTCLK frequency, the data bits are written in the first half of the cell; the clock bits, where appropriate, are written in the last half of the cell. This results in a signal which has pulses that correspond to a 2WRTCLK signal frequency. Figure 5-16 shows the relationship between the MFM information being read from a disk and the 2WRTCLK signal. The disk information consists of pulses which are normally 50 nsec wide and spaced at intervals of 2, 3, or 4 times the period of the 2WRTCLK. This corresponds to a separation between bits of 1, 1.5, or 2 cell times, respectively.

When the RDGATE signal becomes active, the sync detect function is permitted to look for the sync character (see Figure 5-14). The SYNCWIN* signal becomes active when the sync detect circuit recognizes two consecutive bytes of zeros. This gates the disk information through the MUX and delay circuits to the phase comparator. The sync detect function also causes a single pulse to appear on the FORCEPHASE* signal to the VCO circuit. This pulse forces the phase of the RDOSC* signal to be very close to the phase of the disk information. Each time a data or clock bit is detected by the bit detect function, the PPL circuit minimizes the phase difference between the disk information and the RDOSC* signal. No phase correction is made to the RDOSC* signal when an MFM pulse is not received during a cycle of the RDOSC* signal. When the microcontroller senses the SYNCWIN* signal being active, it waits several byte times to allow the RDOSC* signal to completely lock onto the disk information, and then activates the SRCH* signal to enable the data separation function. The data separation function decodes the MFM information into nonreturn to zero data (NRZDATA) bit, disk clock bits (DSKCLKBIT), which is also in a nonreturn to zero format, and a read data clock (RDCLK) which is used to sample the data and clock signal.

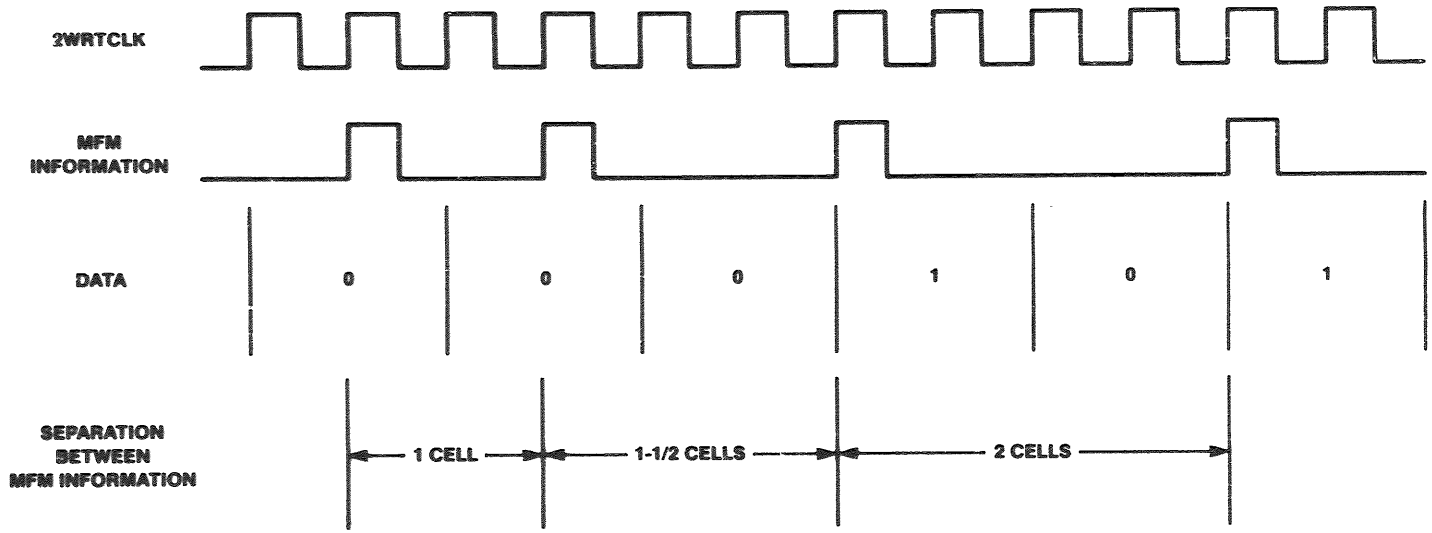


FIGURE 5-16. MFM Information Read From Each Disk

5.3.8.1 Detailed Description. The information from the Winchester disk drive 0 is present in a differential mode on pins 17 and 18 of the J4 headers. When drive 0 is selected, the DRV0SEL* signal at J4-1 is low and the data is enabled through the U17-8 mux. The polarity at this point is such that a one is a high going pulse.

The sync detect circuitry consists of the U16 retriggerable monopulser, the U37 binary counter, and the U38-5 flip-flop. The monopulser is used to detect a series of consecutive MFM zero data bits (clock bits) which, as shown in Figure 5-16, are spaced at intervals of twice the period of the 2WRTCLK signal. To do this, the pulse width of U16 is set to 2.5 times the period of the 2WRTCLK (1.25 cells) by adjusting the R1 variable resistor. This corresponds to 250 nsec for the 5-1/4 inch drives. The counter is used to determine when 16 consecutive zero data pulses have been read, and it sets the flip-flop when this occurs. As long as the RDGATEA signal is low, the sync detect circuitry is idle and reset. When the microcontroller writes a 0 into the XD7 bit of CTRL 2 ($0C), RDGATEA becomes high and an MFM information bit at U16-12 causes the monopulser to start a timing period of 1.25 cell times. Because the U16-10 lead stays high and the U16-9 lead stays low, each zero bit increments the U37 counter. If a one bit were to follow a zero, the time elapsed between the zero and the one bits would be 1.5 cell times, and the U16 monopulser would time out and reset the U37 counter. After 16 successive zero bits have been read, the U38-3 signal goes low; if the next bit is also a zero, the U38-5 flip-flop is set.

While the sync detect circuit is searching for the sync character, the 2WRTCLK signal propagates through the U17-6 MUX and resets the U57-9 bit detect flip-flop each cycle. This enables the U39 phase comparator flip-flops by removing the low signals on their set leads. The 2WRTCLK signal is delayed for 60 nsec through the DL2 delay line and then resets the U39-5 flip-flop. The U39-9 flip-flop may be either set or reset at this time, and each possibility is discussed below:

a. If the U39-9 flip-flop is set, the phase of the delayed 2WRTCLK signal is ahead of the phase of the RDOSC* signal, and the VCO circuit is instructed to increase the frequency of the RDOSC* signal. This is done by the U39-5 flip-flop forcing the PMPUP signal high and the PMPUP* signal low. As soon as the RDOSC* signal goes high, the U39-9 flip-flop is reset and the U95-6 signal goes low, which sets the U57-9 bit detect flip-flop. This forces the U39 flip-flops to be set, and the PMPUP and PMPUP* signals are active only for the length of time the delayed 2WRTCLK signal leads the RDOSC* signal. No further correction of the frequency of RDOSC* is allowed until another cycle of the 2WRTCLK signal is received and the U57-9 bit detect flip-flop is again reset.

b. If the U39-9 flip-flop is reset, the phase of the delayed 2WRTCLK signal is later than the phase of the RDOSC* signal, and the VCO circuit is instructed to decrease the frequency of the RDOSC* signal. This is accomplished by the PMPDN signal being driven high and the PMPDN* signal being driven low by the U39-9 flip-flop. As soon as the U39-5 flip-flop is reset, the U95-6 gate becomes low and the U57-9 flip-flop is set. This sets both the U39 flip-flops and terminates the PMPDN and PMPDN* signals. No further changes of the VCO frequency are permitted until the next positive passage of the 2WRTCLK signal again resets the U57-9 bit detect flip-flop and the above described processes are repeated.

   As this process continues, the RDOSC* signal is brought into phase and frequency sync with the delayed 2WRTCLK signal.

When the sync detect circuit detects 16 consecutive zeros and the U38-5 flip-flop becomes set, the following events occur:

a. The U17-6 MUX switches sources from the 2WRTCLK signal to the data being read from the disk. This means that the RDOSC* signal, which is of the same frequency as the disk data, can be phase synchronized to the disk data.

b. The FORCEPHASE* signal is forced low when both inputs to the U67-11 EXOR gate are high. The width of this signal is determined by the time it takes to reset the U38-9 and U57-5 flip-flops, which are wired in a shift register configuration. The time at which U38-9 gets reset depends upon the phase relationship between the disk read data and the 2WRTCLK signals. Hence, the FORCEPHASE* signal is low for at least one cell time. While this signal is low, the RDOSC* signal is forced high and it is allowed to oscillate again when the FORCEPHASE* signal goes high in coincidence with the disk read data. This forces the the RDOSC* signal to be in very close phase relationship to the disk read data so that only very minor adjustments are required by the PLL circuit and a very fast phase lock is achieved.

c. The syncwindow bit to the microcontroller STAT2 register is activated (goes high), signifying that the first two bytes of a sync character have been received and bit sync between the RDOSC* signal and the disk read data can be achieved within two byte times. After this 2-byte time, the microcontroller activates the AMSRCH function by writing a 1 into bit XD2 of the CTRL2 register ($0C). This causes the U92-5 flip-flop to be reset on the next rising edge of the delay data (DELDATA) signal, and the data separation enable (DSEPEN) signal goes high to enable the data separator and address mark detection circuits.

d. The HIFREQCHNG bit to the microcontroller STAT2 register is made inactive (low). This bit remains low until the sync detect circuit detects a one data bit in the disk MFM information stream by the U16-10 signal going to a low level. This resets the U54-9 flip-flop and activates the HIFREQCHNG bit. When the microcontroller determines this bit is active, it assumes that the address mark ($A1) is being read from the disk, and it monitors the WINRDDATARDY* bit of the STAT2 register for activity. If this bit is not active within two byte times, the microcontroller assumes the sync detect circuit found some contiguous bytes of zeros or ones in a data field instead of a sync character. The microcontroller then resets the read circuitry by making the RDGATE* bit of CTRL2 ($0C) inactive (high). As a part of this resetting, the U38-5 flip-flop is reset and the 2WRTCLK is selected by the U17-6 MUX as the signal for the RDOSC* to lock on. Also, the FORCEPHASE* signal pulses low which forces the RDOSC* to be in phase with the 2WRTCLK signal. The microcontroller leaves the RDGATE* bit inactive for about four byte times to ensure that the RDOSC* achieves frequency and phase lock with the 2WRTCLK signal, and then it activates the RDGATE* bit in another attempt to find a sync character and achieve byte sync by detecting an address mark.

5.3.8.2 Data Separation. Figure 5-17 indicates the timing relationship between the elements used in the actual separation of data bits from clock bits in the MFM information stream. The RDOSC* signal is in phase lock with the DELDATA signal but is at twice the frequency of the highest frequency occurrence of the DELDATA signal. When the microcontroller enables the data separation process, the DSEPEN signal is forced high, and the U94-9 flip-flop is permitted to toggle at the trailing edge of the RDOSC* signal to generate the RDCLK signal. This signal is a square wave which has a period equal to an MFM bit cell and a fixed phase relationship with the MFM bit cells. It is high at the leading edge of the DELDATA signal when a data one is being received and it is low at the leading edge of the DELDATA signal when a clock bit is being received. The leading edge of the DELDATA signal samples the state of the RDCLK and RDCLK* signals through the U93 flip-flops. U93-9 is set if the DELDATA signal represents a data bit; U93-5 is set if it represents a clock bit. The state of the U93-9 flip-flop is sampled by the RDCLK* signal into the U94-5 flip-flop, which effectively extends the data bit and centers it so it can be read as NRZ data using the RDCLK signal. In a similar fashion, the state of the U93-5 flip-flop is sampled by the RDCLK signal into the U92-9 flip-flop, where the clock bits may be read in NRZ form using the RDCLK* signal.

5.3.9 Winchester PLL

The VCO is a discrete LC oscillator circuit with a shunt capacitor consisting of the CR2 hyper-abrupt tuning diode. The capacitance of CR2 varies as a function of the magnitude of the reverse voltage applied across it, and this changes the frequency of the VCO output, RDOSC*. As the reverse voltage is increased, the capacitance of CR2 decreases and the frequency of RDOSC* increases. When the reverse voltage is decreased, the capacitance increases and the RDOSC* frequency is lowered. The nominal frequency of RDOSC* is 10 MHz. A value of 3.3 uH is used for the L3 inductor. The bias on CR2 is established by the bias divider (R16, R33-R35, C35, C45) where R34 is a variable resistor which is used to tune the RDOSC* signal to the desired value.

The frequency of the RDOSC* signal is dynamically controlled by the error amplifier (Q1 and associated resistors) and the filter (R36, R37, C36-C38). The error amplifier is a balanced differential amplifier that either sources current to or sinks current from the filter stage.

When the phase comparitor circuit determines the phase of the RDOSC* signal is ahead of the signal being compared, it pulses the PMPDN signal high and the PMPDN* signal low. This causes the Q1 error amplifier to sink current pulses from the filter stage, which lowers the voltage on the cathode of CR2 and increases its capacitance. This, in turn, produces a small decrease in the frequency of RDOSC* to match the phase of the other signal. Similarly, when the phase of RDOSC* lags the phase of the other signal, the PMPUP* signal pulses low and the PMPUP signal pulses high. This results in Q1 sourcing current pulses into the filter where they are integrated to produce an increase of the reverse bias on CR2, which decreases its capacitance. This reduction in capacitance results in a small increase in the frequency of RDOSC*, which brings it in phase coincidence with the other signal.

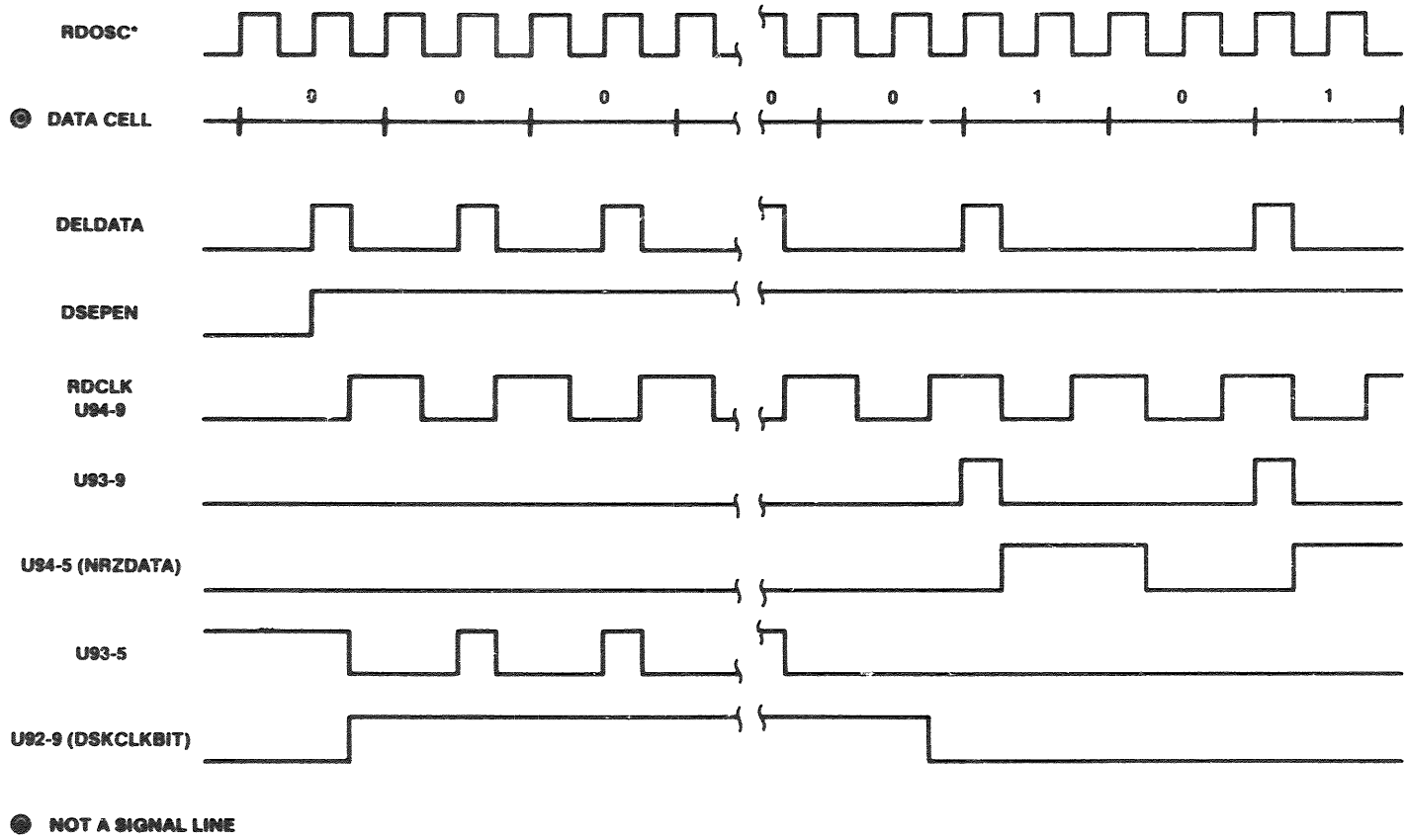


FIGURE 5-17. Data Separation Timing

5.3.10 Winchester Address Mark Detection

After the disk read logic has recognized the sync character and the RDOSC* signal has achieved bit sync with the MFM information from the disk, the microcontroller causes the DSEPEN signal to become active (high). This allows the data separation logic to convert the MFM information into the NRZ data signal (NRZDATA) and an NRZ clock signal (DSKCLKBIT). The DSEPEN signal being high also allows the address mark detection circuit (U90, U107-12, U89-9) to begin looking for an address mark. As indicated in Figure 5-13, the address mark consists of a $A1 character which is purposely written with one of the clock bits deleted. This violates the rules of MFM encoding by generating a 101 pattern for the clock signal. The signals on the DSKCLKBIT line are shifted into the U90 shift register and examined by the U107-12 NAND gate. When a 101 pattern is detected, the U89-9 flip-flop gets reset on the next rising edge of the RDCLK signal to indicate the recognition of the address mark. The NRZDATA signals propagate through the U97 MUX and are shifted into the U106 shift register concurrently with the sampling of the DSKCLKBIT signal by the U90 register. When the U89-9 flip-flop is reset, the U106 shift register contains the $A1 character. On the trailing edge of the next RDCLK signal, the U66-4 gate goes high to strobe the $A1 character into the U105 register and set the U88-9 flip-flop. This activates the WINRDDATARDY* bit in the STAT2 register ($43) to inform the microcontroller that byte synchronization of the disk data has been achieved and a byte of data is ready. The microcontroller reads the byte of data in the U105 register by performing a read of the RDDISK register ($44). This activates the DDATARD* signal and gates the U105 register contents onto the XDBUS. The DDATARD* signal being active also indirectly resets the RDATARDY flip-flop (U88-9). The DDATARD* signal may contain decoding glitches which make it unsuitable to directly reset a flip-flop so, instead, it is sampled by the ERDWIN* signal at a time when no glitches are present, and the U89-5 flip-flop is reset at this time. It, in turn, resets the U88-9 flip-flop, which then sets the U89-5 flip-flop to complete the action. The U108 counter maintains byte sync by enabling the U66-4 signal to pulse high after eight RDCLK cycles have elapsed, and gates the new byte into the U105 holding register and activates the WINRDDATARDY* flag.

When the microcontroller reads the address mark byte (the first byte of a HEADER), it compares that byte against $A1 to verify that the data separation, address mark detection, and byte synchronization processes were correct. The sync detector cannot tell an all zero field (clock bits separated by one cell) from an all one field (data bits separated by one cell). Therefore, the data separation process may result in the clock and data signals being exchanged. The address mark detector would then be monitoring data instead of clocks. If this data contains a 101 pattern, the address mark detector is activated, but the byte of data (actually clock pulses) read by the microcontroller cannot contain $A1 because alternating ones and zeros on the clock signal is not permitted in MFM encoding. If the address mark byte is not $A1, the microcontroller resets the disk read and data separation circuits and makes another attempt to correctly read an address mark and achieve byte sync. This address mark recognition involves both hardware circuits and microcontroller operation.

5.3.11 Winchester ECC

The WDC forms two separate 32-bit ECC characters as a part of each sector of disk information as shown in Figure 5-14. The first is over the ID field and the second is over the data field.

The $(X^{21}+1)(X^{11}+X^{2}+1)$ polynominal which is used in forming each ECC character permits correcting errors having up to seven consecutive bits in error. The ECC character is formed by hardware during a write operation and is checked by hardware during a disk read. The checking consists of forming an ECC character over the incoming data and also over the incoming ECC charater. The resulting ECC character is all zeros if no errors were detected and contains information needed by the microcontroller to generate correction information if an error were detected.

The ECC circuit consists of the following elements:

a. The U109-U112 shift registers. These 32 bits of shift registers are a common element used in both reading from and writing to the disk. The clock used is WRTCLK for a disk write and RDCLK when reading from the disk. This selection is done through the U91 MUX under control of the RDGATE signal.

b. The U113 parity generator/checker. This element forms an odd parity over the feedback signals from the shift registers and the input signal and introduces this parity as the input to the shift register. The feedback signals are determined by the ECC polynominal selected. The input signal is WRTDATA when a write is being performed and NRZDATA for a read operation. This selection is made through the U91 MUX, using the RDGATE signal for control.

c. The U88-5 flip-flop. This element controls the source of the data to the MFM generator on a disk write the source of data and to the serial-to-parallel circuit during a read operation. Consider a write operation. The U88-5 flip-flop is initially set, which routes the WDATA* signal through the U35-6 MUX to the input of the MFM generator circuit and eventually to be written on the disk. The WDATA* signal also propagates through the U91 MUX and becomes an input to the parity generator element (U113-13), and an ECC character is formed over the WDATA* signals as they are written to the disk. When the last byte to be written is in the U34 shift register, the microcontroller activates the ECCTME* signal by writing a 1 into the XD3 bit of CTRL2 register ($0C). When the last bit of the final byte has been shifted from U34, the U11-5 flip-flop is set and the WREGRDY signal goes high. This signal propagates through the U91 MUX and resets the U88-5 flip-flop, which drives the GECC* signal low and the GECC signal high. This enables the ECCDATA* signal to propagate through the U35-6 MUX, and the ECC character is written on the disk. As the ECC character is being shifted out to the write circuit, zeros are being shifted into the shift register when the GECC* signal at U109-1 is low.

   Now consider a read operation. The U88-5 flip-flop is initially set so the NRZDATA from the disk read circuit is gated through the U97-6 MUX into the U106 serial to parallel register. The NRZDATA signal is also routed through the U91 MUX and into the U113 parity checker element and an ECC character is formed. When the last byte of data prior to the ECC

character is being shifted into the U106 register, the microcontroller activates the ECCTME* signal by writing a 1 into the XD3 bit of CTRL2 register ($0C). As this last byte of data is gated into the U105 holding register, the U88-9 flip-flop is set, and the RDATRDY signal goes high. The RDATRDY signal propagates through the U91 MUX and resets the U88-5 flip-flop. This selects the ECC character as the source to the U106 serial-to-parallel shift register, and it also forces the input to the ECC register to be a zero. As the ECC character is received from the disk, it is essentially compared to the newly formed ECC character through the U113 parity checker. The results of this comparison becomes the data the microcontroller reads instead of the ECC character from the disk. If this character (four bytes) is zero, the data was received correctly. If the character is non-zero, it is used by the microcontroller to generate an address and a mask for the host so it can correct the data bits in error.

5.3.12 Floppy Interface

The WDC controls one 5-1/4 inch mini-floppy flexible disk drive. The IBM System 34 double-density format (MFM) and IBM 3740 single density format (FM) are both supported by the WDC. The 765 FDC (floppy disk controller) manufactured by NEC and others provides the selected encoding and format for data written to the disks and the decoding of that information when a read operation is performed. The control function for the disks -- such as drive selection, head selection, and stepping of the head, -- is accomplished directly by the microcontroller, as discussed previously. The technical specifications of the FDC are included to provide detailed information of its operation, and only the interface with the WDC is described.

The microcontroller communicates with the FDC through a byte wide bidirectional data bus by manipulating the appropriate control signals. Because the timing requirements of the FDC are not compatible with the operation of the microcontroller, the U47 register is used to store these control signals which are individually controlled by the microcontroller to achieve compatibility. The U48 three-state register is used to store bytes of information (data or commands) to be written to the FDC to conform to FDC timing requirements.

The FDC is configured in its DMA mode of operation by the command sequence written to it by the microcontroller. Each time the FDC requires a byte of information to be transferred, it activates the FDDRQ* signal, which is continuously read by the microcontroller as the XD6 bit of the STAT2 register ($43). If a write type operation is in process, the microcontroller writes the byte of data into the U48 register. The microcontroller then writes into the WRTFDC register ($0E), activating the FDCDACK*, FDCWRT*, and FDCADR0 bits in the U47 register. The U47-16 signal being low enables the data in the U48 register to the FDC, and signals the FDC of the availability of the data. The write operation is completed when the microcontroller performs another write to the WRTFDC register ($0E), deactivating the FDDACK*, FDCWRT*, and FDCADR0 bits. If a data read operation were to be performed, the microcontroller would activate the FDCDACK*, FDCRD*, and FDCADR0 bits in the WRTFDC register ($0E). The FDC then places the byte of data on the 8-bit data bus, and the microcontroller inputs this data through the U49 driver by reading from the RDFDD register (U46). The microcontroller then releases the control bits in the WRTFDC Register ($0E).

The FDC requires two clock signals in its operation -- CLK (U50-19) and WCLK (U50-21). The CLK signal is a 4 MHz square wave which is formed by dividing the 8 MHz OSC8 signal by two through the U61-5 flip-flop. This 4 MHz signal propagates through the U31 MUX on pins 10 or 11, one of which is always enabled since the 8INCHFLOP signal is always low. The WCLK signal is a positive going pulse of 250 ns width with a frequency of 500 KHz for MFM encoding and 250 KHz for FM encoding. This is twice the highest frequency of the data that appears on the disk. This allows the FDC to write data in one-half of a cell, and the clock bit, where appropriate, to be written in the other half of the bit cell. The U61-5 flip-flop, the U32 counter, the U30-9 flip-flop, the U62-4 inverter, the U55-6 AND gate, and the U32 MUX are used in the generation of WCLK. When FM encoding is specified, the MFM signal at U31-14 is low and the WCLK signal is selected as the input of U55-6 by the U31 MUX. The MFM signal is high when MFM encoding is specified and the WCLK signal is formed by the U32-12 counter.

The FDC furnishes information on the U50-32 and U50-31 signals which is used in performing a precompensating shift in time of the data to be written to the drives. The FDC examines the data patterns to be written and drives the two lines in accordance with the information in Table 5-3.

TABLE 5-3. FDC Precomp Signals

U50-31	U50-32	DIRECTION TO SHIFT DATA
L	L	NO SHIFT
L	H	WRITE DATA EARLY
H	L	WRITE DATA LATE
H	H	INVALID

The U78 shift register and the U77 MUX perform the precompensation logic on the write data. The write data is placed on the U50-32 signal line by the FDC and the corresponding shift information on the U50-31 and U50-32 signal lines. The data is shifted into U78 where it is sequentially shifted along each 125 nsec by the OSC8* signal. This delayed data then propagates through the U77 MUX along the path established by the shift pattern. Thus, data is written at normal time, or 125 nsec early, or 125 nsec late. The microcontroller enables the precompensating logic by writing a 0 into the XD5 bit of CTRL1 registers ($0B), which forces the ENWPCMP* signal high. The logic is disabled by writing a 1 into the same bit.

During a read operation, the FDC requires the encoded information (SFLPRDTA) from the disk to appear at the U50-23 input. It also requires a signal on the U50-22 line (RDATAWIN) which brackets in time the encoded information. The FDC uses the RDATAWIN signal and the knowledge of MFM and FM encoding to separate the encoded information into clock and data bits. After byte synchronization has been achieved, the FDC assembles the data bits into bytes and makes them available to the microcontroller. The generation of the RDATAWIN signal and its synchronization with the SFLPRDTA signal is achieved with the use of a PLL circuit. This consists of the U86 VCO the Q3 and Q4 transistors, the U100 PROM, and the U102 binary counter. This circuit generates a signal which follows the frequency of the data being read from the disk, including any variations of data frequency due to disk speed fluctuations. The RDATAWIN signal is generated from the PLL signal.

The frequency of the VCO signal at U86-7 is determined by the voltage level at U86-2. When this voltage increases, the signal frequency increases; when the voltage at U86-2 decreases, the VCO output frequency is lowered. This voltage is controlled by the U100 PROM through the Q3 and Q4 transistors, and the current amplifier U101.

When the FDC is not reading data from a disk, the PLL circuit must lock on a reference frequency which is at the nominal frequency of the disk data. This allows the PLL circuit to rapidly lock on the disk data when it is available. The FWCLK signal is at the correct frequency to provide this reference frequency, and it appears on the U100-15 PROM input. The VCOSYNC signal at U100-1 is low when the FDC is not reading disk data, and this causes the PROM to compare the frequency of the U102 counter with the frequency of the FWCLK signal. If the FWCLK signal occurs before the U102 counter reaches the correct value, the frequency of the VCO is too low and must be increased. The U100 PROM pulses the U100-11 lead low and maintains the U100-12 lead low. This turns Q3 on and increases the voltage at U86-2, which raises the VCO frequency as desired. If the FWCLK signal occurs after the U102 counter reaches the proper value, the frequency of the VCO is too high and must be lowered. This is accomplished by pulsing the U100-12 lead high while maintaining U100-12 at a high level, which decreases the voltage at U86-2 and lowers the VCO frequency. When the two signals occur at the same time, lock has been achieved. The VCO output is at 8 MHz when this occurs.

When a disk read operation is initiated by the microcontroller, the disk is accessed and data appears at U87-11. This data is synchronized with the clock driving the U102 counter through the U87 flip-flops, and becomes the SFLPRDTA signal to the FDC and the U100 PROM. The FDC forces the VCOSYNC signal at U100-1 high, and the PROM begins comparing the state of the U102 counter with SFLPRDTA instead of the FWCLK signal. The locking process described above is repeated, and the U102 counter operates at the same frequency as the disk data.

The RDATAWIN signal to the FDC is generated from one of the outputs of the U102 counter. This selection is made with the U103 MUX. If MFM data is being read, the U102-12 signal propagates through U103, gets divided by two by the U104-1 flip-flop, and generates a RDATAWIN signal of nominally 250 KHz. When FM data is being read, the U102-11 signal passes through U103, gets divided by two, and becomes a nominal 125 KHz RDATAWIN signal. The U103 MUX is also used to select the clock which drives the U102 counter. The VCO clock frequency divided by two is always used with 5-1/4 inch disk drives.

CHAPTER 6

SUPPORT INFORMATION

6.1 INTRODUCTION

This chapter provides the interconnection signals, parts list with parts location illustration, and schematic diagram of the WDC. Calibration procedures for the fixed disk high frequency detector, VCO, error amplifier, and the floppy disk VCO are provided in paragraph 6.3.

6.2 INTERCONNECT SIGNALS

The module interconnects with the I/O Channel through connector J2. Connector J3 is provided for interconnection of 5-1/4 inch fixed disk drives. Connector J4 is used for fixed disk radial interface. Connector J6 provides the interconnection for a 5-1/4 inch floppy disk drive.

6.2.1 I/O Channel Connector J2 Interconnect Signals

Table 6-1 lists each pin connection, signal mnemonic, and signal characteristic for the connector.

TABLE 6-1. I/O Channel Connector J2 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1	INT4*	INTERRUPT REQUEST 4 - one of four active low output signal lines used by the module to interrupt the I/O Channel master. These lines are jumper selectable.
2	GND	GROUND
3	INT3*	INTERRUPT REQUEST 3 - same as INT4* on pin 1.
4	GND	GROUND
5	INT2*	INTERRUPT REQUEST 2 - same as INT4* on pin 1.
6	GND	GROUND
7	INT1*	INTERRUPT REQUEST 1 - same as INT4* on pin 1.
8	GND	GROUND
9	IORES*	INPUT/OUTPUT RESET - active low input signal used to reset the module.
10	GND	GROUND

TABLE 6-1. I/O Channel Connector J2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
11	XACK*	TRANSMIT ACKNOWLEDGE - active low output signal used to advise the I/O Channel master that write data is latched or read data is available.
12	GND	GROUND
13		Not used.
14	GND	GROUND
15		Not used.
16	GND	GROUND
17		Not used.
18	GND	GROUND
19		Not used.
20,21	GND	GROUND
22	A11	ADDRESS bus (bit 11) - one of eleven input lines used to selectively address the module.
23	A^	ADDRESS bus (bit 9) - same as A11 on pin 22.
24	A10	ADDRESS bus (bit 10) - same as A11 on pin 22.
25	A7	ADDRESS bus (bit 7) - same as A11 on pin 22.
26	A8	ADDRESS bus (bit 8) - same as A11 on pin 22.
27	A5	ADDRESS bus (bit 5) - same as A11 on pin 22.
28	A6	ADDRESS bus (bit 6) - same as A11 on pin 22.
29	A3	ADDRESS bus (bit 3) - same as A11 on pin 22.
30	A4	ADDRESS bus (bit 4) - same as A11 on pin 22.
31	A1	ADDRESS bus (bit 1) - same as A11 on pin 22.
32	A2	ADDRESS bus (bit 2) - same as A11 on pin 22.
33	A0	ADDRESS bus (bit 0) - same as A11 on pin 22.
34	GND	GROUND
35	STB*	STROBE - an input signal. A high-to-low transition starts the cycle. A low-to-high transition stops the cycle.

TABLE 6-1. I/O Channel Connector J2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
36	GND	GROUND
37	WT*	WRITE - an input signal that is low when the I/O Channel is in the write cycle. The signal is high when the I/O Channel is in the read cycle.
38,39	GND	GROUND
40	D7	DATA bus (bit 7) - one of eight bidirectional lines used to transmit data between the I/O Channel master and the module.
41	D5	DATA bus (bit 5) - same as D7 on pin 40.
42	D6	DATA bus (bit 6) - same as D7 on pin 40.
43	D3	DATA bus (bit 3) - same as D7 on pin 40.
44	D4	DATA bus (bit 4) - same as D7 on pin 40.
45	D1	DATA bus (bit 1) - same as D7 on pin 40.
46	D2	DATA bus (bit 2) - same as D7 on pin 40.
47	D0	DATA bus (bit 0) - same as D7 on pin 40.
48-50	GND	GROUND

6.2.2 Fixed Disk Drives Connector J3 Interconnect Signals

Table 6-2 lists each pin connection, signal mnemonic, and signal characteristic for the connector J3.

TABLE 6-2. Fixed Disk Drives Connector J3 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
ALL ODD 1-33	GND	GROUND
2	RWC*	REDUCED WRITE CURRENT - this line, when active together with WRTGATE*, causes the write circuitry to write on the disk with a lower write current.
4	HDSEL2*	HEAD SELECT 2 - this line provides for the selection of head 2^2 in drives requiring this signal (see HDSEL0, pin 14).
6	WRTGATE*	WRITE GATE - the active state of this signal, or low level, enables write data to be written to the disk. The inactive state of this signal, or high level, enables data to be transferred from the drive.
8	SKCOMPL*	SEEK COMPLETE - this line goes low when the R/W heads have settled on the final track at the end of a seek.
10	TK0*	TRACK 0 - this interface signal indicates a low level only when the R/W heads are positioned at cylinder zero (the outermost data track).
12	WFAULT*	WRITE FAULT - this signal is used to indicate a condition exists at the drive that may cause improper writing on the disk. When this line is a low level, further writing and stepping is inhibited at the drive until the condition is corrected.
14	HDSEL0*	HEAD SELECT 0 - this line, together with HEAD SELECT 1, and HEAD SELECT 2 allows selection of each individual R/W head in a binary coded sequence. HEAD SELECT 2^0 is the least significant line and HEAD SELECT 2^2 is the most significant line.
16		Not used.
18	HDSEL1*	HEAD SELECT 1 - see HDSEL0* on pin 14.
20	INDEX*	INDEX - this interface signal is provided by the drive once each revolution to indicate the beginning of a track. Normally, this signal is a high level and makes the transition to a low level to indicate INDEX.
22	DRVRDY*	DRIVE READY - this interface signal when low, together with SEEK COMPLETE, indicates that the drive is ready to read, write, or seek, and that the I/O signals are valid. When this line is high, all writing and seeking is inhibited.

TABLE 6-2. Fixed Disk Drives Connector J3 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
24	STEP*	STEP - this line is a control signal which causes the R/W head to move in the direction of motion defined by the DIRECTION IN line.
26	DSEL0*	DRIVE SELECT 0 - this line, when at a low level, connects the drive 0 interface to the control lines.
28	DSEL1*	DRIVE SELECT 1 - same as DSEL0* on pin 26.
30	DSEL2*	DRIVE SELECT 2 - same as DSEL0* on pin 26.
32	DSEL3*	DRIVE SELECT 3 - same as DSEL0* on pin 26.
34	DIRIN*	DIRECTION IN - this signal defines direction of motion of the R/W heads when the STEP line is pulsed. A high level defines the direction as out and if a pulse is applied to the STEP line, the R/W heads move away from the center of the disk. A low level on this line defines the direction as in and the R/W heads move toward the center of the disk.
35-50		Not used.

6.2.3 Fixed Disk Radial Connector J4 Interconnect Signals

Connector J4 interconnects drive 0 data transfer lines, and connector J5 interconnects drive 1 data transfer lines. Table 6-3 lists each pin connection, signal mnemonic, and signal characteristic for connectors J4 and J5.

TABLE 6-3. Fixed Disk Radial Connectors J4 and J5 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1	DRV0SEL*	DRIVE SELECTED - this status line informs the host system of the selection status of the drive.
2	GND	GROUND
3		Not used.
4	GND	GROUND
5	CWPROT0*	CARTRIDGE WRITE PROTECTED - this line indicates the position of the write protect plug in the cartridge of the selected drive. When the signal is low, writing is inhibited, and if writing is attempted, the WFAULT* is activated.
6	GND	GROUND
7		Not used.
8	GND	GROUND
9	+TMNGCLKD0	TIMING CLOCK - this signal plus the -TMNGCLKD is a differential pair of clock signals. The frequency of this clock is exactly 1/16 times the bit frequency for the standardized write data.
10	-TMNGCLKD0	TIMING CLOCK - same as +TMNGCLKD0 on pin 9.
11,12	GND	GROUND
13	+MFMWDATA0	MFM WRITE DATA - this signal plus the -MFMWDATA is a differential pair that defines the transitions to be written on the track. The transition of +MFMWDATA line going more positive than the -MFMWDATA line causes a flux reversal on the track, provided WRTGATE* is active.
14	-MFMWDATA0	MFM WRITE DATA - same as +MFMWDATA on pin 13.

TABLE 6-3. Fixed Disk Radial Connector J4 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
15,16	GND	GROUND
17	+RDDATA0	MFM READ DATA - this signal plus the -RDDATA is a differential pair that transmits the data recovered by reading a prerecorded track. The transition of the +RDDATA line going more positive than the -RDDATA line represents a flux reversal on the track of the selected head.
18	-RDDATA0	MFM READ DATA - same as +RDDATA on pin 17.
19,20	GND	GROUND

6.2.4 Floppy 5-1/4 inch Drive Connector J6 Interconnect Signals

Table 6-4 lists each pin connection, signal mnemonic, and signal characteristic for connectors J6.

TABLE 6-4. Floppy 5-1/4 inch Drive Connector J6 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
ODD PINS 1-33	GND	GROUND
2,4		Not used.
6	DSEL3*	DRIVE SELECT 3 - this line, when at a low level, connects the drive 3 interface to the control lines.
8	INDEX*	INDEX - this interface signal is provided by the drive once each revolution to indicate the beginning of a track. Normally, this signal is a high level and makes the transition to a low level to indicate INDEX.
10	DSEL0*	DRIVE SELECT 0 - same as DSEL3* on pin 6.
12	DSEL1*	DRIVE SELECT 1 - same as DSEL3* on pin 6.
14	DSEL2*	DRIVE SELECT 2 - same as DSEL3* on pin 6.
16	MOTORON*	MOTOR ON - when MOTORON goes low, those drives on the daisy-chain with power on, having a diskette inserted, and the access door closed, are energized and begin accelerating to operating speed. After reaching nominal speed, the drive is available for use by the host system.
18	DIRIN*	DIRECTION IN - this signal defines direction of motion of the R/W heads when the STEP line is pulsed. A high level defines the direction as out and if a pulse is applied to the STEP line, the R/W heads move away from the center of the disk. A low level on this line defines the direction as in and the R/W heads move toward the center of the disk.
20	STEP*	STEP - this interface line is a control signal which causes the R/W heads to move in the direction of motion defined by the DIRECTION IN line.
22	FLOPWDATA*	FLOPPY WRITE DATA - this line carries encoded write data to be recorded on the diskette. The leading (negative) edge of each pulse causes the write head current to be reversed, thereby writing a flux transition on the diskette.
24	FLOPWGATE*	FLOPPY WRITE GATE - this line controls the read/write mode of the selected drive. The write circuits are enabled when FLOPWGATE* is at a low level, provided the diskette is not write protected and a STEP operation is not in progress.

TABLE 6-4. Floppy 5-1/4 inch Drive Connector J6 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
26	TK0*	TRACK 0 - this interface signal indicates a low level only when the R/W heads are positioned at cylinder zero (the outermost data track).
28	WRT PROT*	WRITE PROTECT - this signal indicates that the diskette in the selected drive is write protected.
30	FLOPRDATA*	FLOPPY READ DATA - this line transmits composite serial data from the selected drive diskette to the controller. The data consists of a series of low level pulses -- one for each flux transition recorded on the diskette.
32	HDSEL0*	HEAD SELECT 0 - When this line is high, side 0 of the diskette is accessed. When the line is low, side 1 is accessed.
34		Not used.

6.3 CALIBRATION

The module is factory-calibrated and normally does not require calibration. However, if the fixed disk high frequency detector (U16), VCO (Q2), error amplifier (Q1), floppy disk VCO (U86), (Q3), (Q4) or any associated circuitry is replaced, the following procedure may be used for calibration.

6.3.1 High Frequency Detector Calibration

To calibrate the high frequency detector (U16), proceed as follows:

a. Adjust the +5 volt power source so that the voltage at J1 pin 2 and pin 5 reads +5.0 volts.

b. Adjust the -5 volt power source so that the voltage at J1 pin 3 reads -5.0 volts.

c. Remove jumper from header J17.

d. Connect jumpers on connector J4 as follows:

Pin 9 to pin 17	+TMNGCLK to +RDDATA
Pin 10 to pin 18	-TMNGCLK to -RDDATA
Pin 2 to pin 1	GND to DRVSEL*

e. Connect a scope to test point E1 and adjust potentiometer R1 to obtain a pulse width of 250 ± 10 ns.

f. Remove jumpers from connector J4.

g. Install jumper on header J17.

This completes the calibration of the high frequency detector.

6.3.2 VCO Adjustment

To calibrate the VCO, proceed as follows:

a. Turn equipment power ON.

b. Adjust voltages as indicated in paragraph 6.3.1, steps a and b.

c. Reset the module.

d. Remove jumper from header J12 and install on header J14.

e. Connect a counter to test point E4 and adjust potentiometer R34 to obtain a frequency of 10 ± 0.001 MHz.

f. Remove jumper from header J14 and install on header J12.

This completes the calibration of the VCO.

6.3.3 Error Amplifier Calibration

To calibrate the error amplifier (Q1), proceed as follows:

a. Turn equipment power ON.

b. Adjust voltages as indicated in paragraph 6.3.1, steps a and b.

c. Reset the module.

d. Remove jumper from header J18.

e. Install jumper on header J13.

f. Connect a voltmeter to test point E2. Common to ground. Adjust potentiometer R28 to obtain a reading of 75 ± 5 MV.

g. Install jumper on header J18.

h. Install jumper on header J19.

i. Connect a voltmeter to Q1-14. Common to ground. Verify the voltage is 75 ± 50 MV.

j. Remove jumpers from headers J19 and J13.

This completes the calibration of the error amplifier.

6.3.4 Floppy Disk VCO Calibration

To calibrate the floppy disk VCO (Q3, Q4, U86), proceed as follows:

a. Turn equipment power OFF.

b. Connect the bottom of R49 to bottom (GND) of C65.

c. Connect the bottom of R47 to top (+5V) of C65.

d. Turn equipment power ON.

e. Connect a counter to test point E5.

f. Adjust C54 to obtain a reading of 7.45 $\pm$ 0.049 MHz.

g. Remove connections made in steps b, c, and e.

This completes the calibration of the floppy disk VCO.

6.4 PARTS LIST

Table 6-5 lists the components of both versions of the module. Component differences are noted in the list. The parts locations are illustrated in Figure 6-1. This parts list reflects the latest issue of hardware at the time of printing.

TABLE 6-5. Module Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
	84-W8130B01	Printed wiring board
CR1,CR3	48NW9616A03	Diode, 1N4148/1N914
CR2	48NW9616A08	Diode, MV1404
C1,C14	23NW9618A71	Capacitor, electrolytic, 47 uF @ 10 Vdc
C2	21SW992C005	Capacitor, fixed, ceramic, 68 pF @ 50 Vdc, NPO
C3-C10,C12,C13, C15-C24,C26-C35, C39-C45,C47-C53, C55-C66,C68-C85	21SW992C025	Capacitor, fixed, ceramic, 0.10 uF @ 50 Vdc
C11,C25	23NW9618A61	Capacitor, elecrolytic, 10 uF @ 25 Vdc
C36	21NW9604A58	Capacitor, fixed, ceramic, 330 pF @ 50 Vdc
C37	21SW992C040	Capacitor, fixed, ceramic, 6.8K pF @ 50 Vdc, X7R
C38	21SW992C008	Capacitor, fixed, ceramic, 150 pF @ 50 Vdc, NPO
C46	21NW9604A59	Capacitor, fixed, ceramic, 390 pF @ 50 Vdc

TABLE 6-5. Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
C54	20NW9628A02	Capacitor, trimmer, 7-25 pF
C67	21SW992C002	Capacitor, fixed, ceramic, 15 pF @ 50 Vdc, NPO
DL1	01NW9804C25	Delay line, triple, 12 ns
DL2	01NW9804B35	Delay line, 100 ns
DS1	48NW9612A23	Diode, light emitting, red
J1	28NW9802E52	Header, straight, 6 pin
J2,J3	28NW9802A90	Connector, 50 pin
J4,J5	28NW9802C73	Connector, 20 pin
J6	28NW9802B59	Connector, 34 pin
J7,J8,J12-J15, J17-J19	28NW9802D01	Header, double row post, 2 pin
J9	28NW9802D04	Header, single row post, 3 pin
J10,J16	28NW9802B34	Header, double row post, 16 pin
J11	28NW9802C43	Header, double row post, 8 pin
L1,L2	24NW9708A09	Inductor, fixed, 4.7 uH
L3	24NW9708A08	Inductor, fixed, 3.3 uH
Q1	51NW9615J28	Transistor, quad I.C. MPQ6700
Q2	48NW9610A14	Transistor, 2N3904
Q3	48NW9611A14	Transistor, MPS2907
Q4	48NW9610A22	Transistor, MPS2222
Q5	48NW9610A34	Transistor, 2N5320
R1	18NW9603A36	Resistor, variable, 10k ohm, 10%, 1/2 W, 25 turn
R2,R3,R5,R6	06SW-125A18	Resistor, fixed, film, 51 ohm, 5%, 1/2 W
R4	06SW-124A55	Resistor, fixed, film, 1.8k ohm, 5%, 1/4 W
R7-R12,R16,R20, R39,R40,R44, R45,R47,R50, R51,R55-R63, R65,R67,R68	06SW-124A49	Resistor, fixed, film, 1.0k ohm, 5%, 1/4 W

TABLE 6-5. Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
R13,R14	06SW-961C12	Resistor, fixed, film, 1.30k ohm, 1%, 1/4 W
R15	06SW-124A25	Resistor, fixed, film, 100 ohm, 5%, 1/4 W
R17,R36,R42,R54	06SW-124A37	Resistor, fixed, film, 330 ohm, 5%, 1/4 W
R18	51NW9626A67	Resistor network, 8/220-330 ohm
R19,R38,R46,R66	06SW-124A73	Resistor, fixed, film, 10k ohm, 5%, 1/4 W
R21,R24,R41	06SW-961B01	Resistor, fixed, film, 100 ohm, 1%, 1/4 W
R22,R23	06SW-961C89	Resistor, fixed, film, 8.25k ohm, 1%, 1/4 W
R25,R26	06SW-961C30	Resistor, fixed, film, 2.00k ohm, 1%, 1/4 W
R27	06SW-125A19	Resistor, fixed, film, 56 ohm, 5%, 1/2 W
R28	18NW9603A39	Resistor, variable, 200 ohm, 10%, 1/2 W, 25 turn
R29,R30	06SW-961B69	Resistor, fixed, film, 511 ohm, 1%, 1/4 W
R31,R32	06SW-961B85	Resistor, fixed, film, 750 ohm, 1%, 1/4 W
R33	06SW-124A56	Resistor, fixed, film, 2.0k ohm, 5%, 1/4 W
R34	18NW9603A40	Resistor, variable 2k ohm, 10%, 1/2 W, 25 turn
R35	06SW-124A97	Resistor, fixed, film, 100k ohm, 5%, 1/4 W
R37	06SW-124A45	Resistor, fixed, film, 680 ohm, 5%, 1/4 W
R43	06SW-124A43	Resistor, fixed, film, 560 ohm, 5%, 1/4 W
R48	06SW-124A53	Resistor, fixed, film, 1.5k ohm, 5%, 1/4 W
R49,R53	06SW-124A57	Resistor, fixed, film, 2.2k ohm, 5%, 1/4 W
R52	06SW-124A61	Resistor, fixed, film, 3.3k ohm, 5%, 1/4 W
R64	51NW9626A41	Resistor network, 9/4.7k ohm
R69,R70	06SW-124A33	Resistor, fixed, film, 220 ohm, 5%, 1/4 W
R71,R72	51NW9626A87	Resistor network, 12/330-470 ohm
U1	51NW9615H01	I.C. AM25LS2521PC
U2,U22	51NW9615E98	I.C. SN74LS373N

TABLE 6-5. Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U3,U4,U23-U26, U33,U105,U120, U123	51NW9615E99	I.C. SN74LS374N
U5	51NW9615F63	I.C. SN74LS640N
U6	51NW9615F02	I.C. 74LS244N
U7,U8,U40	51NW9615A36	I.C. MC7406P
U9,U20	51NW9615E93	I.C. SN74LS14N
U10,U12,U32, U102,U108	51NW9615C28	I.C. SN74LS161N
U11,U30,U54, U68,U69,U87, U89,U104	51NW9615C25	I.C. SN74LS74N
U13,U38,U39, U56,U57,U61,U79, U80,U82,U83,U88, U92,U93,U94,U99, U115,U117,U131	51NW9615C95	I.C. SN74S74N
U14,U125	51NW9615G43	I.C. SN74S64N
U15	51NW9615F61	I.C. MC3487P
U16	51NW9615J91	I.C. AM26S02PC
U17,U97	51NW9615F31	I.C. DM74S51N
U18	51NW9615F60	I.C. MC3486P
U19,U72,U73	51NW9615C69	I.C. SN74LS130N
U21,U27,U28, U121,U124	51NW9615F52	I.C. SN74LS273N
U29,U36,U42, U62,U63,U65	51NW9615C21	I.C. SN74LS04N
U31,U103	51NW9615E84	I.C. SN74LS153N
U34	51NW9615D28	I.C. 74166B
U35,U51,U135	51NW9615F06	I.C. SN74LS51N
U37	51NW9615C30	I.C. SN74LS193N

TABLE 6-5. Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U41,U126	51NW9615F35	I.C. DM74LS21N
U43	51NW9615G38	I.C. SN74LS38N
U44	51NW9615J06	I.C. N8X60N
U45,U46	51NW9615H79	I.C. TMM2016P-1
U47,U48	51NW9615J21	I.C. SN74LS534N
U49,U122	51NW9615E95	I.C. SN74LS240N
U50	51NW9615H02	I.C. UPD765C
U52,U66,U70,U81	51NW9615C20	I.C. SN74LS02N
U53,U78,U106, U109-U112	51NW9615F41	I.C. DM74LS164N
U55	51NW9615C22	I.C. SN74LS08N
U58,U107	51NW9615E88	I.C. SN74LS10N
U59,U64,U133	51NW9615E91	I.C. SN74LS00N
U60	51NW9615C29	I.C. SN74LS174N
U67	51NW9615C58	I.C. SN74S86N
U71	51NW9615F38	I.C. SN74LS393N
U74	51NW9615C34	I.C. SN74S138N
U75,U76	51NW9615J26	I.C. UPD2149D-2
U77	51NW9615E86	I.C. SN74LS151N
U84	(NOTE 1)	I.C. programmed
U85	51NW9615N06	I.C. N8X305N
U86	51NW9615J03	I.C. SN74S124N
U90	51NW9615F16	I.C. SN74LS175N
U91	51NW9615C27	I.C. SN74LS157N
U95,U98	51NW9615C94	I.C. SN74S00N
U96	51NW9615C96	I.C. SN74S04N
U100	(NOTE 1)	I.C. programmed

TABLE 6-5. Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U101		Not used
U113	51NW9615F12	I.C. 74LS280N
U114	51NW9615F30	I.C. DM74S05N
U116	51NW9615D27	I.C. SN74S32N
U118	(NOTE 1)	I.C. programmed
U119	(NOTE 1)	I.C. programmed
U127	51NW9615E67	I.C. SN74S260N
U128,U129,U130	51NW9615J22	I.C. SN74LS169AN
U132,U134		Not used
VR1	51NW9615H08	I.C. MC79L05ACP
Y1	48AW1015B03	Crystal oscillator, 20.00 MHz
Y2	48AW1016B01	Crystal oscillator, 16.00 MHz
	09NW9811A46	Socket, crystal, 4 pin (use at Y1, Y2)
	09NW9811A02	Socket, DIL, 14 pin (use at R71, R72)
	09NW9811A86	Socket, DIL, 16 pin (use at U100)
	09NW9811A09	Socket, DIL, 18 pin (use at U75, U76)
	09NW9811A15	Socket, DIL, 24 pin (use at U45, U46, U84, U118, U119)
	09NW9811A21	Socket, DIL, 28 pin (use at U44)
	09NW9811A22	Socket, DIL, 40 pin (use at U50)
	09NW9811A48	Socket, DIL, 50 pin (use at U85)
	29NW9805B17	Jumper, shorting (use at J9-J12, J15-J18)

NOTE: (1) When ordering, use number labeled on part.

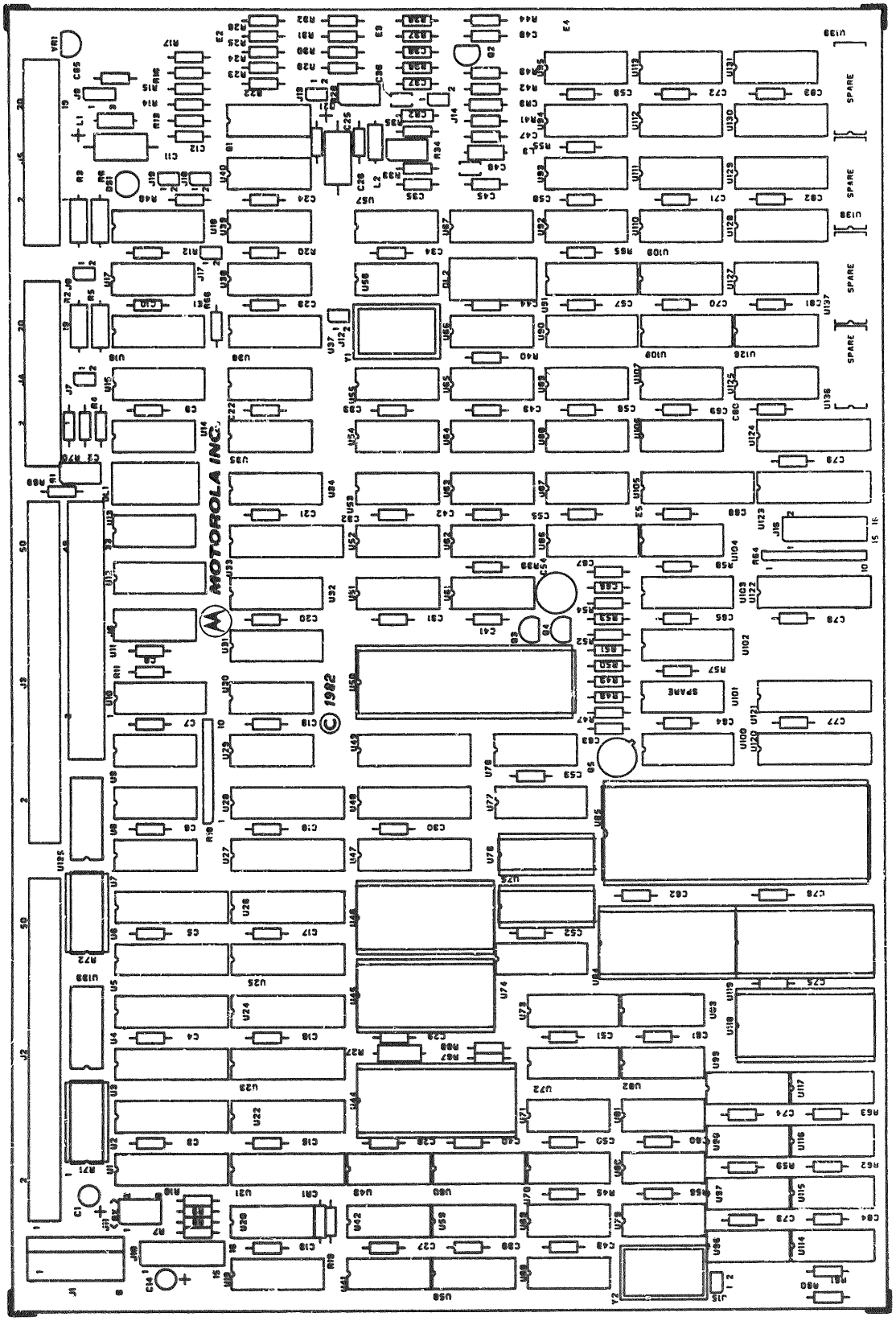


FIGURE 6-1. Module Parts Location

6.5 SCHEMATIC DIAGRAM

Figure 6-2 illustrates the schematic diagram for the module.

NOTES:

1. FOR REFERENCE DRAWINGS REFER TO BILL(S) OF MATERIAL 01-W3130B01 AND 602.
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, ± 5PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL VOLTAGES ARE DC.
3. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
4. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
5. SPECIAL SYMBOL USAGE:
   * DENOTES – ACTIVE LOW SIGNAL.
   [] DENOTES – ON BOARD SIGNAL.
6. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION.
7. PART TYPES ARE ABBREVIATED IN THE FIELD OF THE DRAWING, FOR FULL PART TYPE, REFER TO TABLE 1.
8. CODE FOR SHEET TO SHEET REFERENCES IS AS FOLLOWS:
   6 A6
   SHEET — ZONE
9. Y1 VALUE, FOR B01–MHZ
   FOR B02–17.36MHZ
10. L3 VALUE, FOR B01–3.3UH
    FOR B02–5.6UH
11. USER OPTION

TABLE 1 (7)

REF DES	TYPE (4)	GND	+5V	VBB	+5VF
U1	25LS2521	10	20		
U2	74LS373	10	20		
U3	74LS374	10	20		
U4	74LS374	10	20		
U5	75LS640	10	20		
U6	74LS244	10	20		
U7	7406	7	14		
U8	7406	7	14		
U9	74LS14	7	14		
U10	74LS161A	8	16		
U11	74LS74A	7	14		
U12	74LS161A	8	16		
U13	74S74	7	14		
U14	74S64	7	14		
U15	MC3487	8	16		
U16	26S02	8	16		
U17	74S51	7	14		
U18	MC3486	8	16		
U19	74LS138	8	16		
U20	74LS14	7	14		
U21	74LS273	10	20		
U22	74LS373	10	20		
U23	74LS374	10	20		
U24	74LS374	10	20		
U25	74LS374	10	20		
U26	74LS374	10	20		
U27	74LS273	10	20		
U28	74LS273	10	20		
U29	74LS04	7	14		
U30	74LS74A	7	14		
U31	74LS153	8	16		
U32	74LS161A	8	16		
U33	74LS374	10	20		
U34	74LS166	8	16		
U35	74LS51	7	14		
U36	74LS04	7	14		
U37	74LS193	8	16		
U38	74S74	7	14		
U39	74S74	7	14		
U40	7406	7	14		
U41	74LS21	7	14		
U42	74LS04	7	14		
U43	74LS38	7	14		
U44	8X60	2	28	1	
U44	8X60	14			
U44	8X60	21			
U45	TMM2016P-1	12	24		
U46	TMM2016P-1	12	24		

TABLE 1 (7) CONT'D

REF DES	TYPE (4)	GND	+5V	VBB	+5VF
U47	74LS534	10	20		
U48	74LS534	10	20		
U49	74LS240	10	20		
U50	UPD765	20	40		
U51	74LS51	7	14		
U52	74LS02	7	14		
U53	74LS164	7	14		
U54	74LS74A	7	14		
U55	74LS08	7	14		
U56	74S74	7	14		
U57	74S74	7	14		
U58	74LS10	7	14		
U59	74LS00	7	14		
U60	74LS174	8	16		
U61	74S74	7	14		
U62	74LS04	7	14		
U63	74LS04	7	14		
U64	74L300	7	14		
U65	74LS04	7	14		
U66	74LS02	7	14		
U67	74S86	7	14		
U68	74LS74A	7	14		
U69	74LS74A	7	14		
U70	74LS02	7	14		
U71	74LS393	7	14		
U72	74LS138	8	16		
U73	74LS138	8	16		
U74	74S138	8	16		
U75	UPD2149-2	9	18		
U76	UPD2149-2	9	18		
U77	74LS151	8	16		
U78	74LS164	7	14		
U79	74S74	7	14		
U80	74S74	7	14		
U81	74LS02	7	14		
U82	74S74	7	14		
U83	74S74	7	14		
U84	82S191	12	24		
U85	8X305	12	37		
U86	74S124	8	16		
U86	74S124	9	15		
U87	74LS74A	7	14		
U88	74S74	7	14		
U89	74LS74A	7	14		
U90	74LS175	8	16		
U91	74LS157	8	16		
U92	74S74	7	14		

TABLE 1 (7) CONT'D

REF DES	TYPE (4)	GND	+5V	VBB	+5VF
U93	74S74	7	14		
U94	74S74	7	14		
U95	74S00	7			14
U96	74S04	7	14		
U97	74S51	7	14		
U98	74S00	7	14		
U99	74S74	7	14		
U100	82S129	8	16		
U102	74LS161A	8	16		
U103	74LS153	8	16		
U104	74LS74A	7	14		
U105	74LS374	10	20		
U106	74LS164	7	14		
U107	74LS10	7	14		
U108	74LS161A	8	16		
U109	74LS164	7	14		
U110	74LS164	7	14		
U111	74LS164	7	14		
U112	74LS164	7	14		
U113	74LS280	7	14		
U114	74S05	7	14		
U115	74S74	7	14		
U116	74S32	7	14		
U117	74S74	7	14		
U118	82S191	12	24		
U119	82S191	12	24		
U120	74LS374	10	20		
U121	74LS273	10	20		
U122	74LS240	10	20		
U123	74LS374	10	20		
U124	74LS273	10	20		
U125	74S64	7	14		
U126	74LS21	7	14		
U127	74S260	7	14		
U128	74LS169	8	16		
U129	74LS169	8	16		
U130	74LS169	8	16		
U131	74S74	7	14		
U133	74LS00	7	14		
U135	74LS51	7	14		
DL1	DELAY	7	14		
DL2	DELAY	7	14		
Y1	CRYSTAL OSC	7	14		
Y2	CRYSTAL OSC	7	14		

Y2	
VR1	
U135	U132,U134
R72	
Q5	
L3	
J19	
DS1	
DL2	
CR3	
C84	
HIGHEST NUMBER USED	NOT USED
REFERENCE DESIGNATIONS	

FIGURE 6-2. Module Schematic Diagram (Sheet 1 of 16)

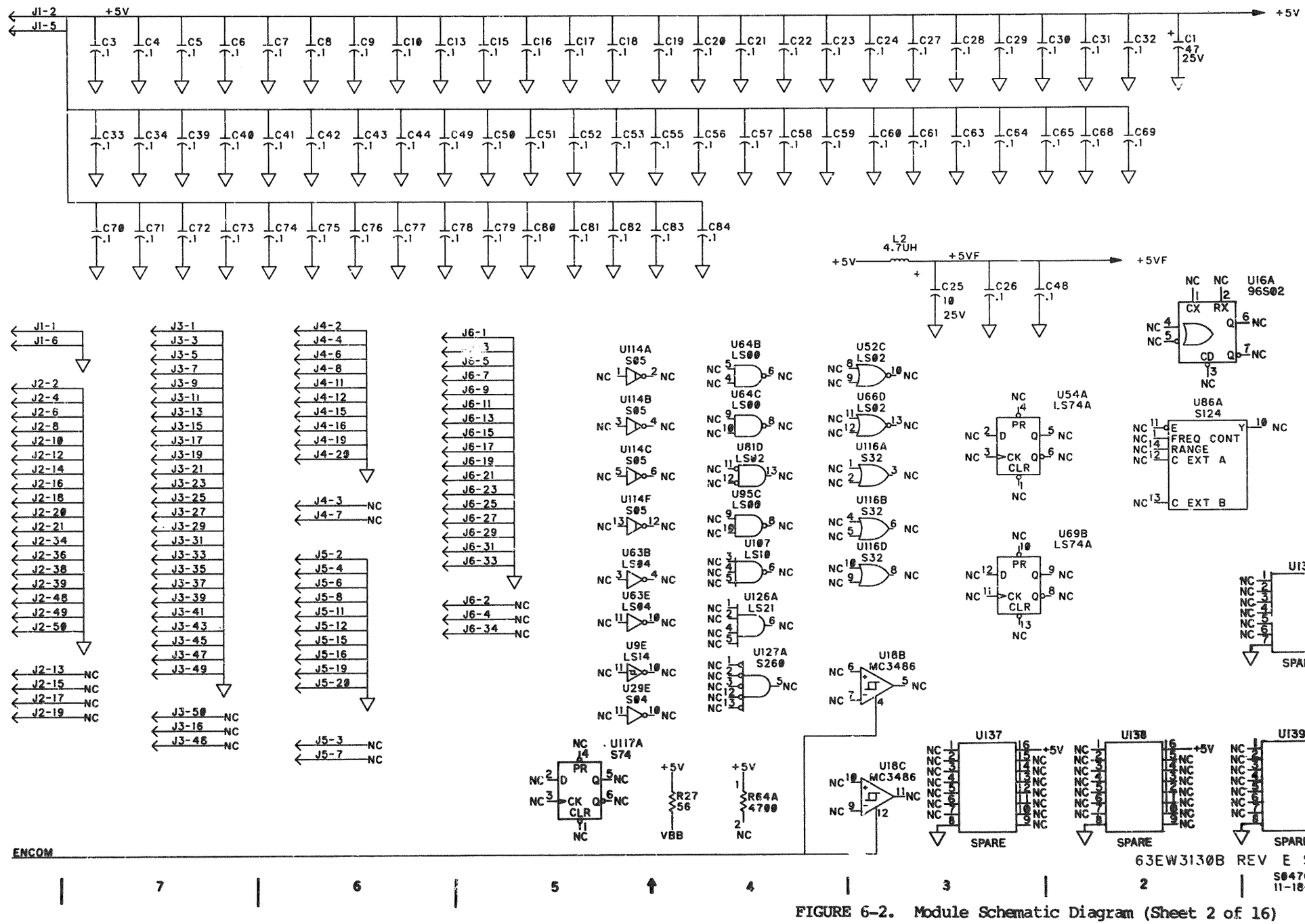
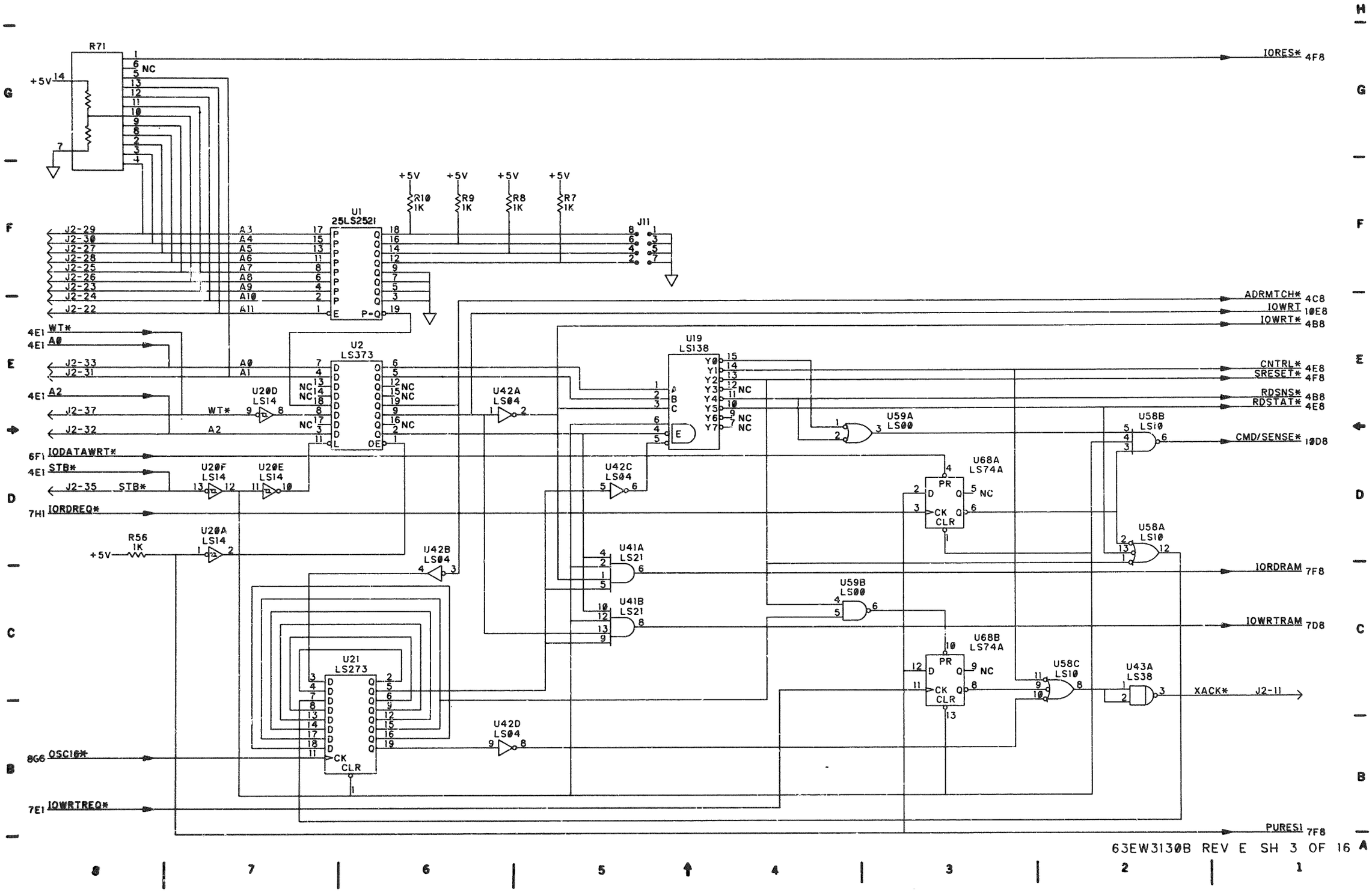


FIGURE 6-2. Module Schematic Diagram (Sheet 2 of 16) 6-21/6-22



63EW3130B REV E SH 3 OF 16

FIGURE 6-2. Module Schematic Diagram (Sheet 3 of 16) 6-23/6-24

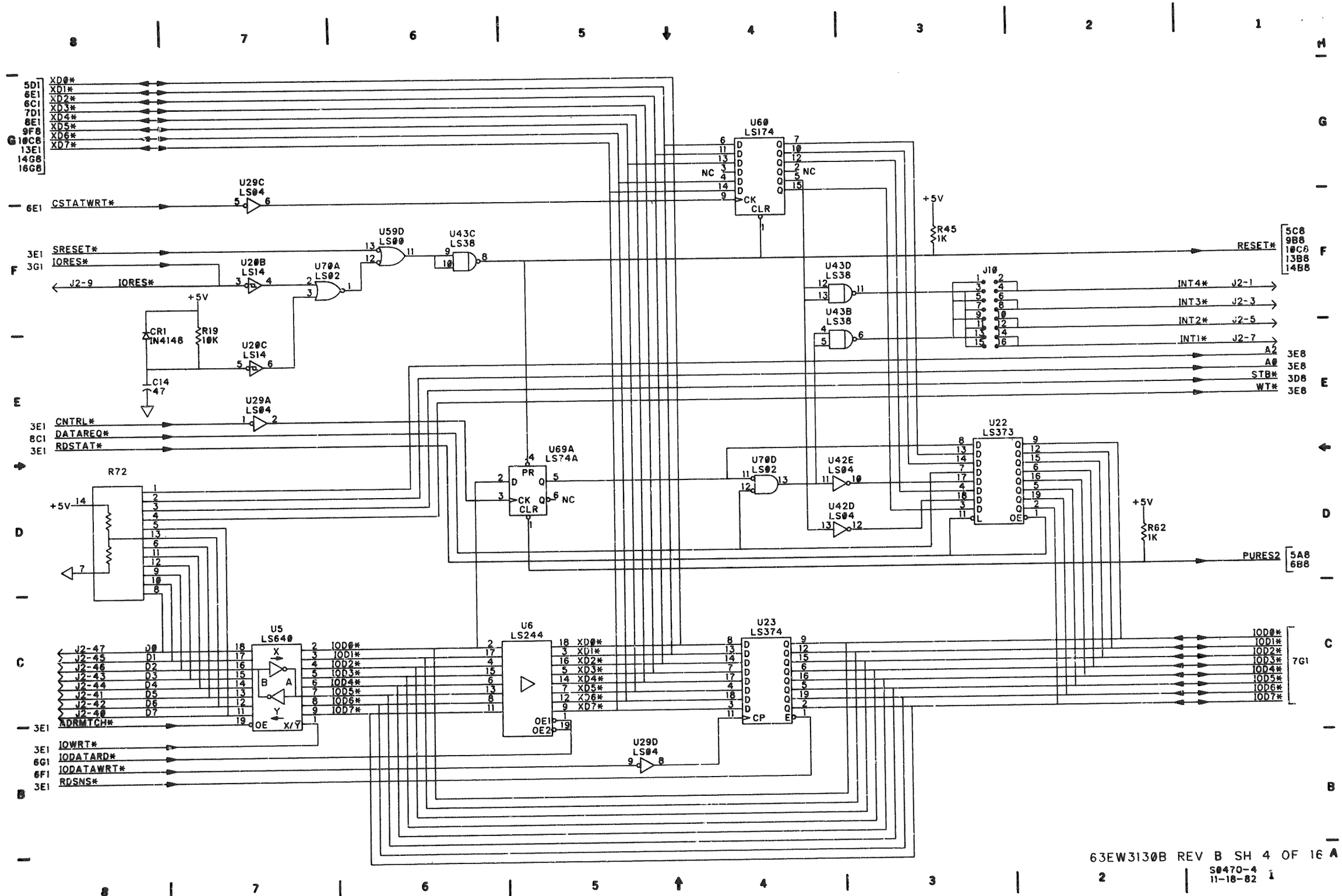
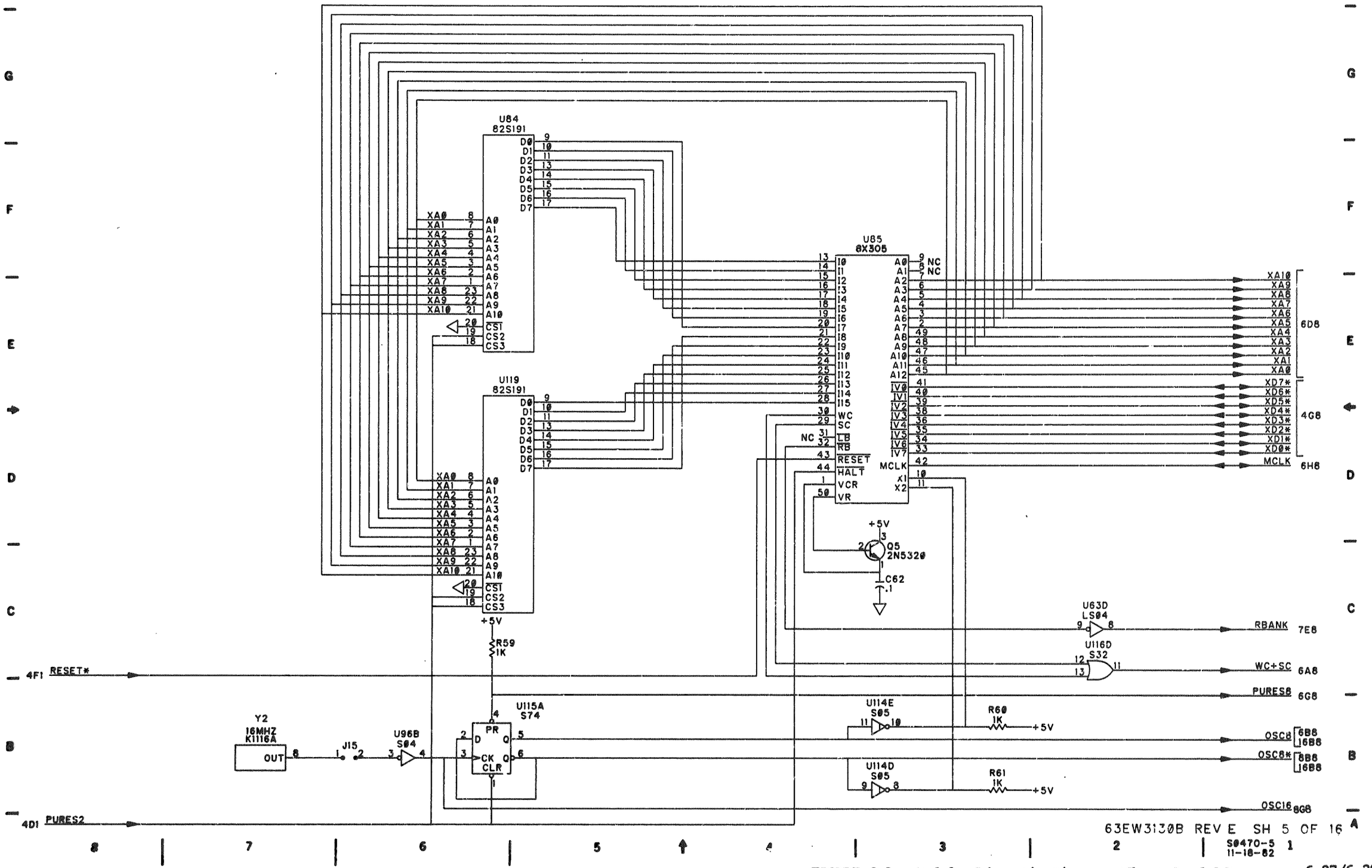


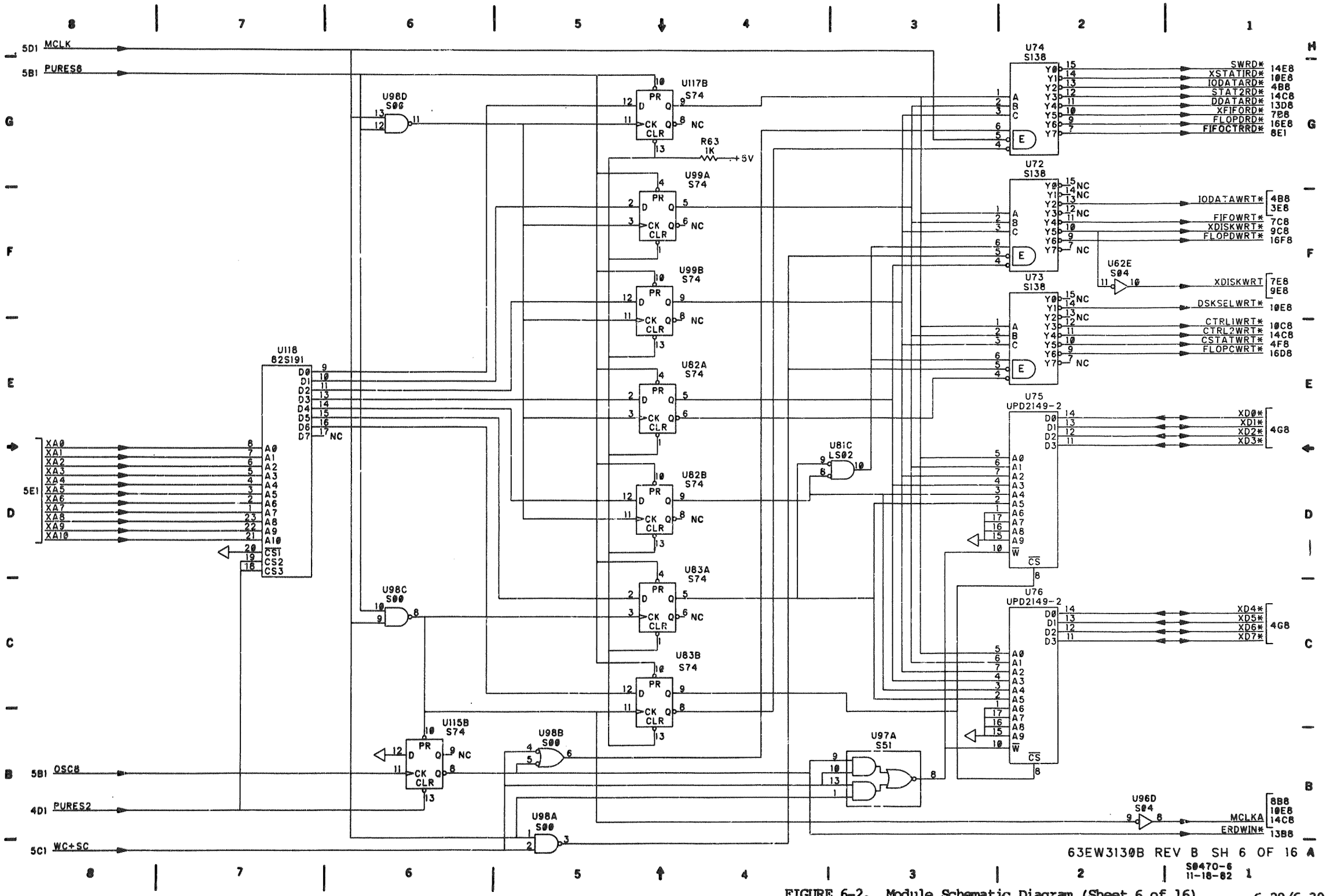
FIGURE 6-2. Module Schematic Diagram (Sheet 4 of 16)



63EW3130B REV E SH 5 OF 16

S0470-5
11-18-82

FIGURE 6-2. Module Schematic Diagram (Sheet 5 of 16)



63EW3130B REV B SH 6 OF 16

S0470-6
11-18-82

FIGURE 6-2. Module Schematic Diagram (Sheet 6 of 16)

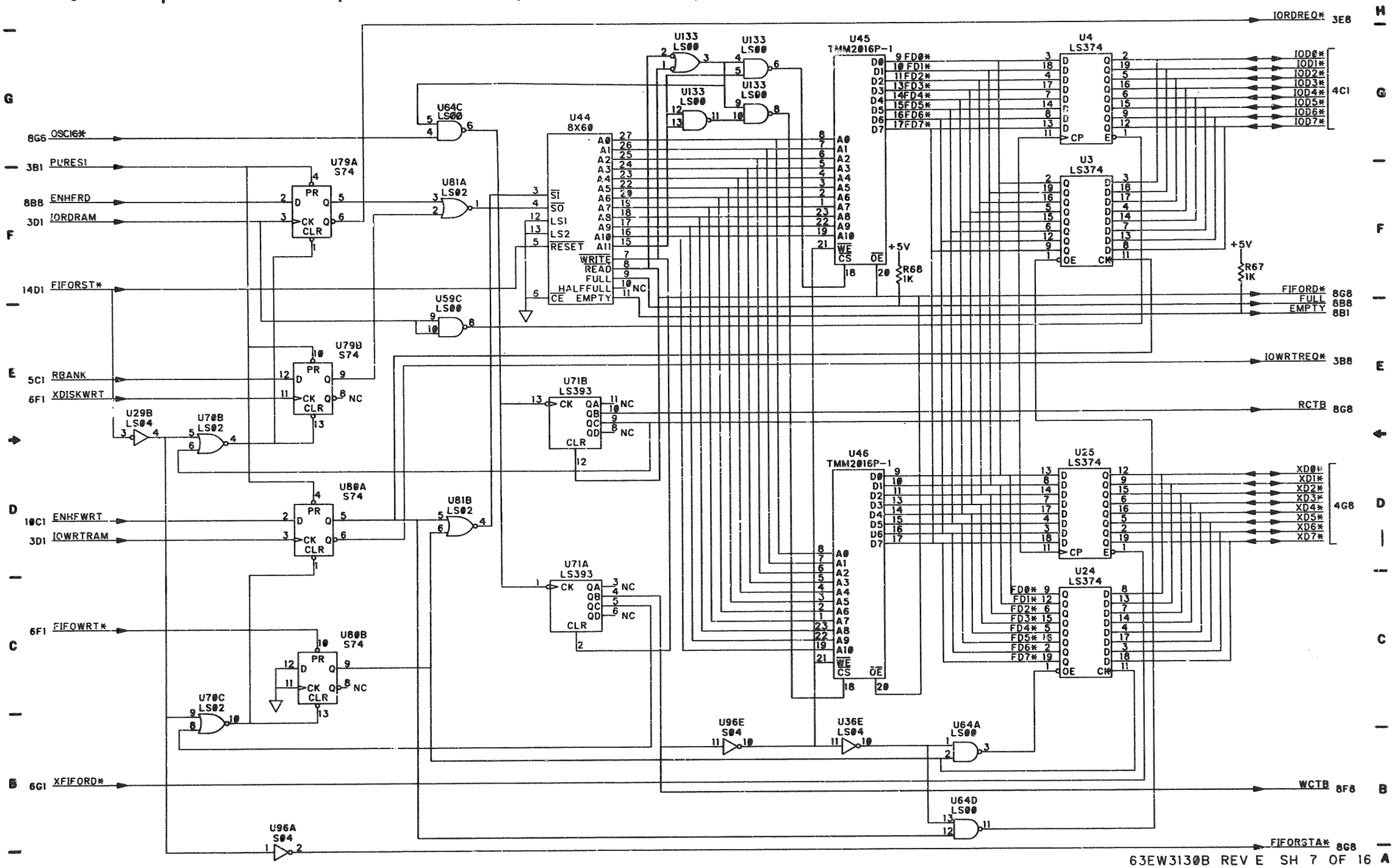
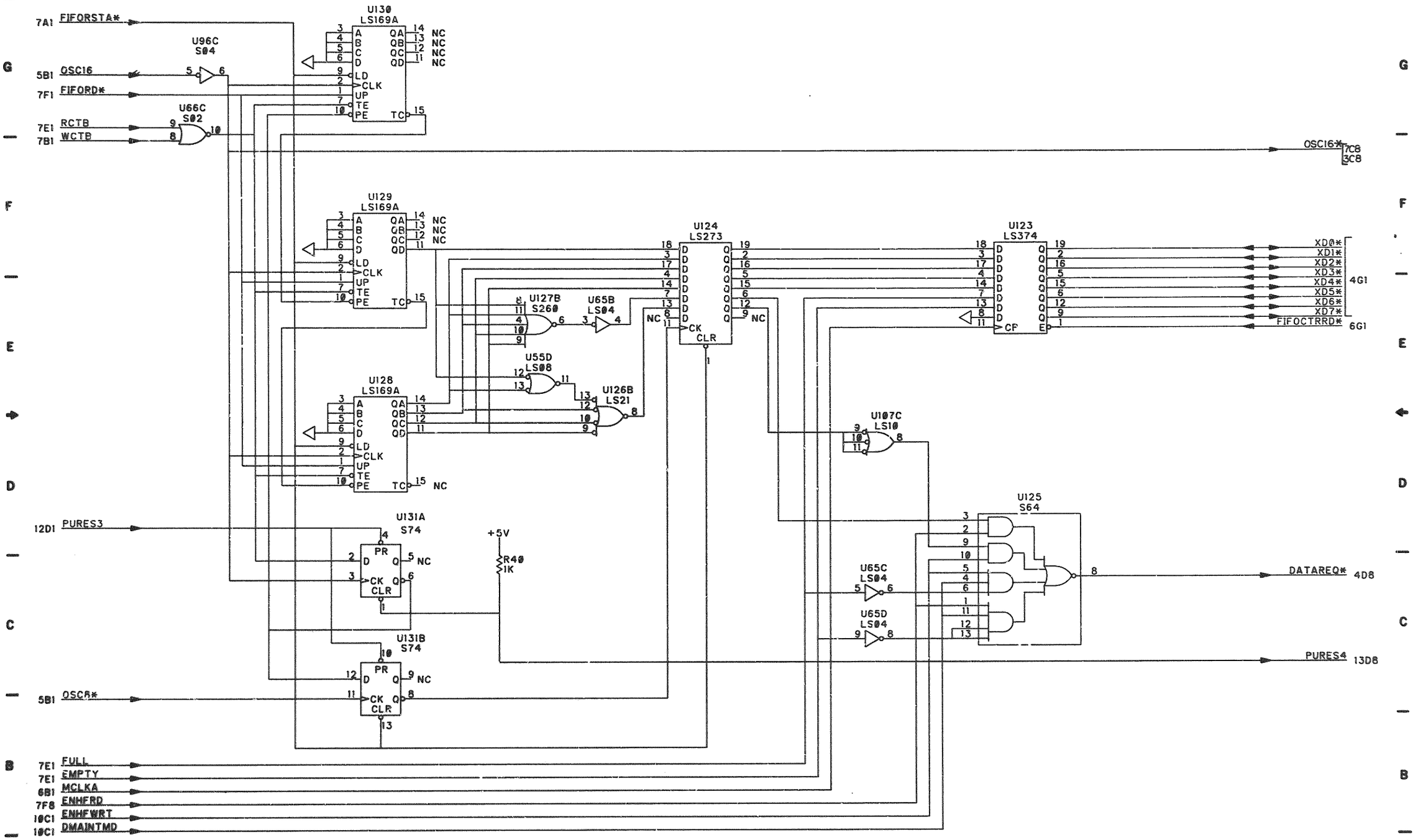


FIGURE 6-2. Module Schematic Diagram (Sheet 7 of 16) 6-31/6-32



63EW3130B REV E SH 8 OF 16

S0470-8 11-18-82

FIGURE 6-2. Module Schematic Diagram (Sheet 8 of 16)

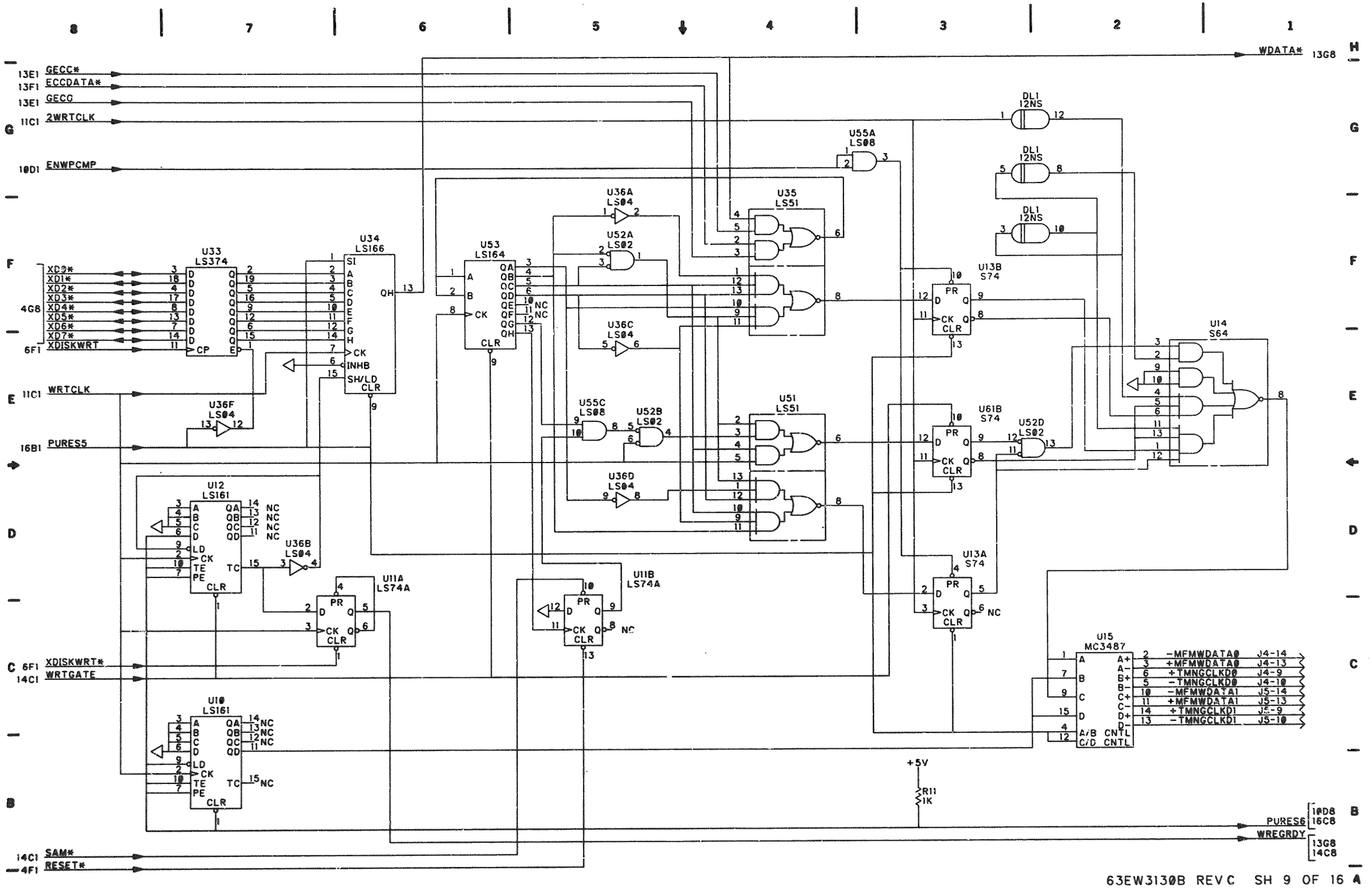


FIGURE 6-2. Module Schematic Diagram (Sheet 9 of 16)

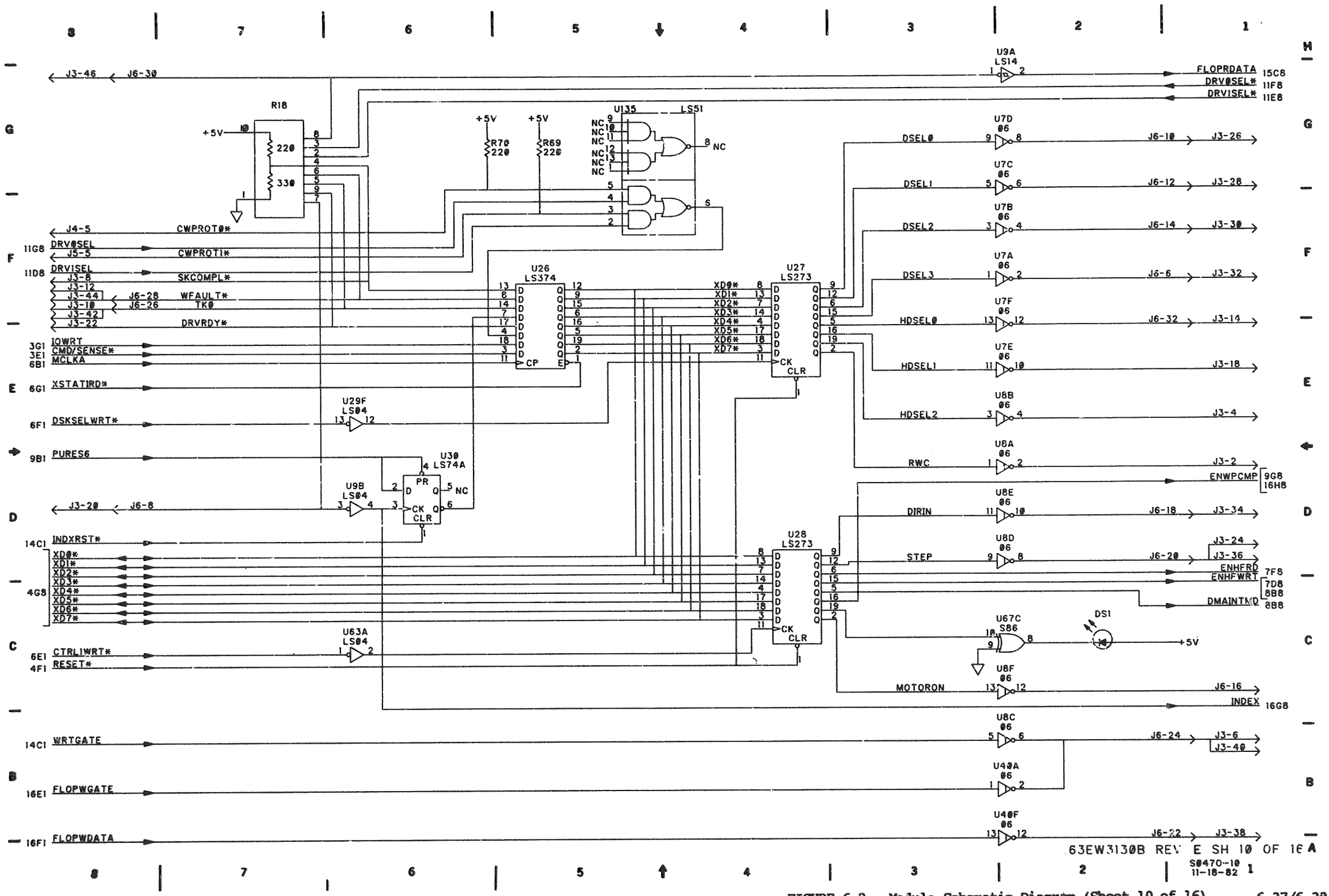
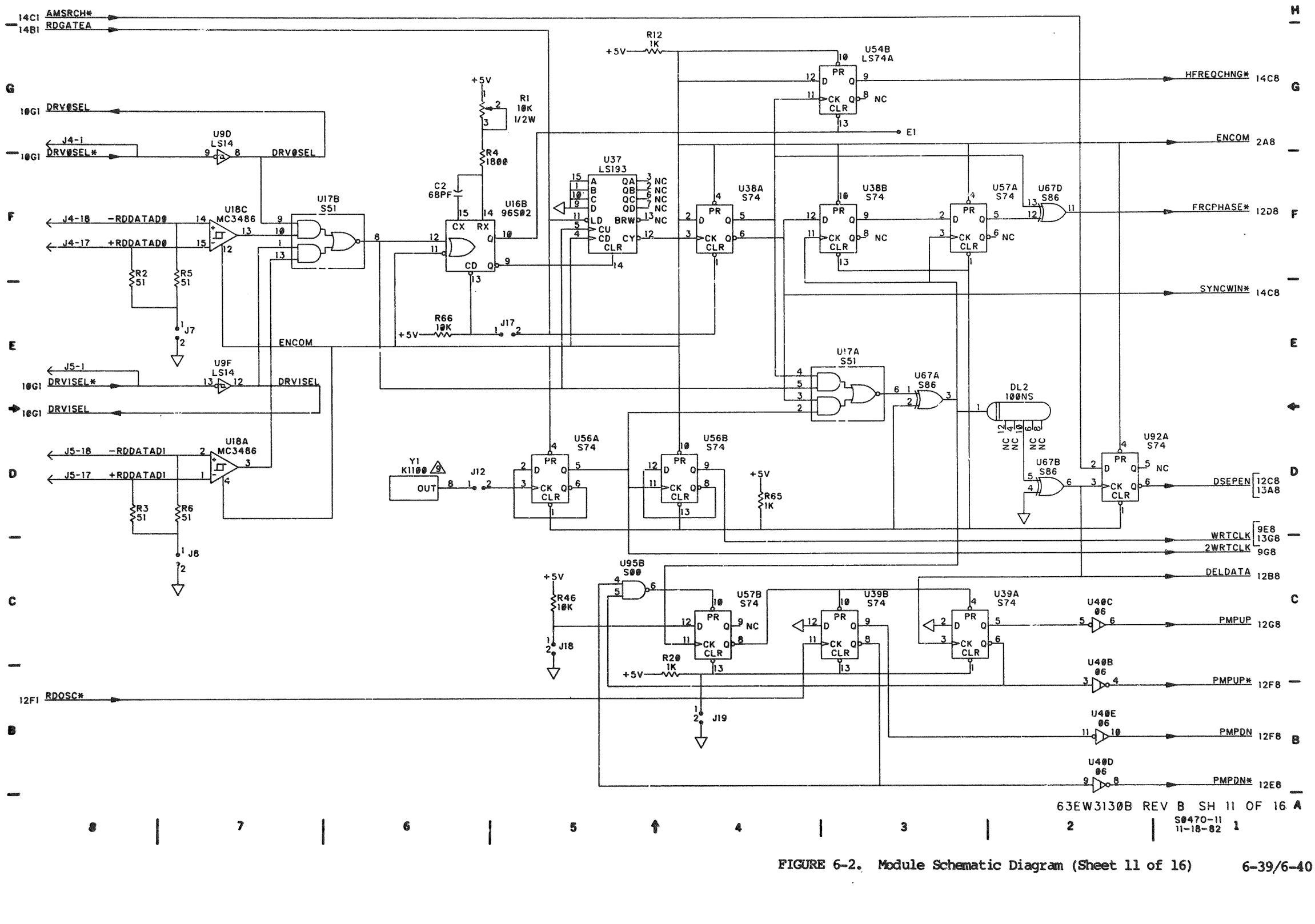


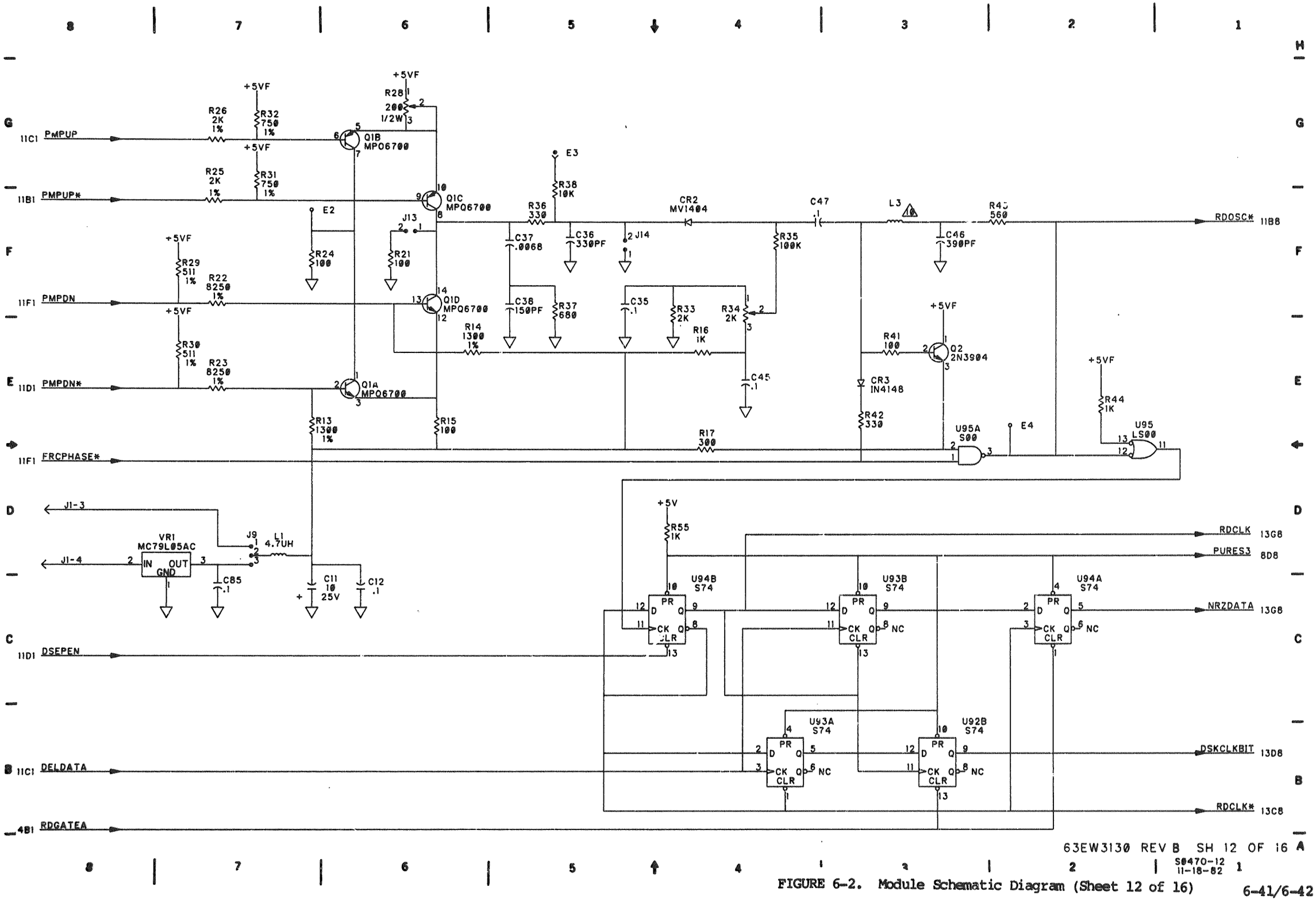
FIGURE 6-2. Module Schematic Diagram (Sheet 10 of 16)



63EW3130B REV B SH 11 OF 16

S0470-11 11-18-82

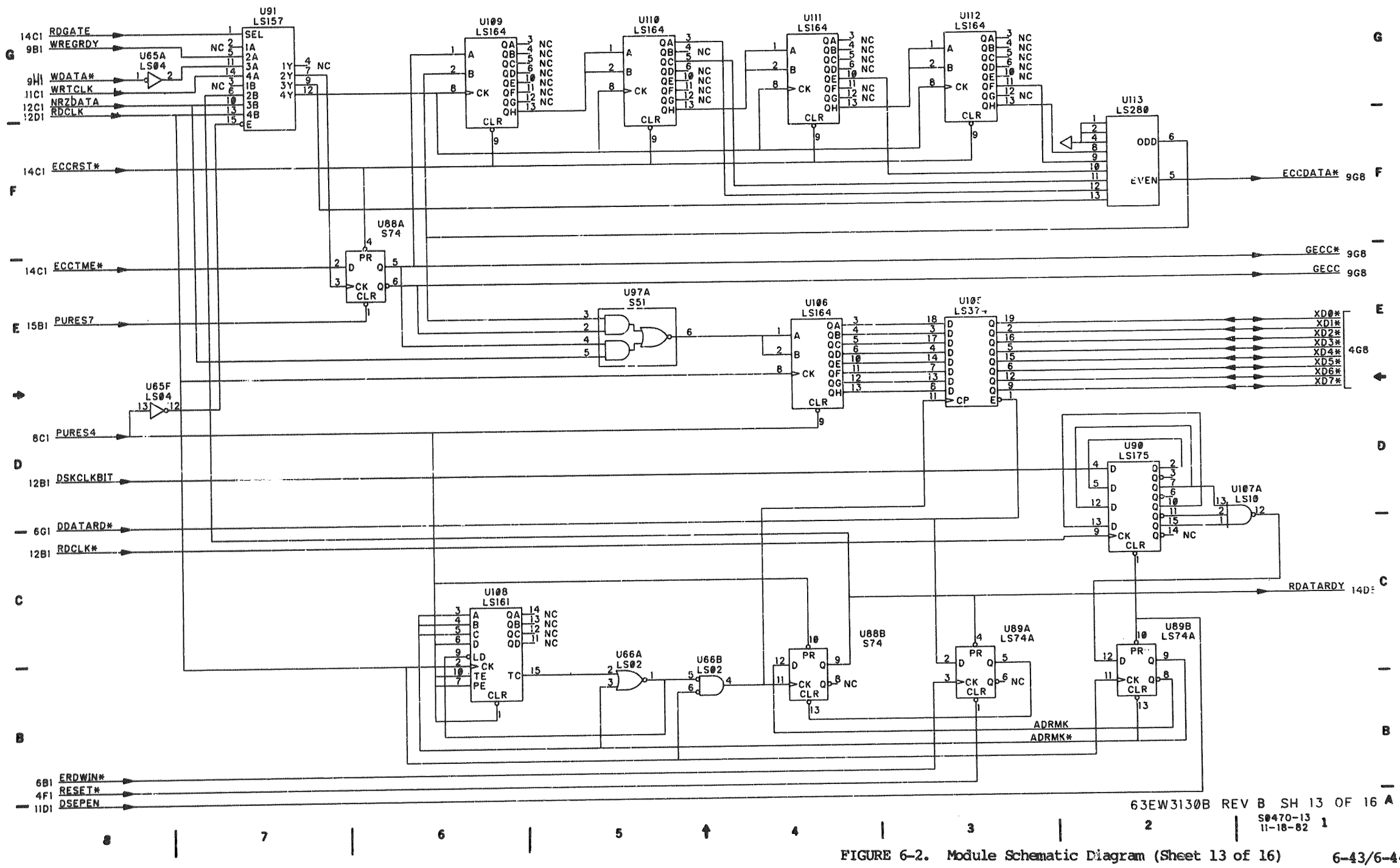
FIGURE 6-2. Module Schematic Diagram (Sheet 11 of 16)



63EW3130 REV B SH 12 OF 16

S0470-12 11-18-82

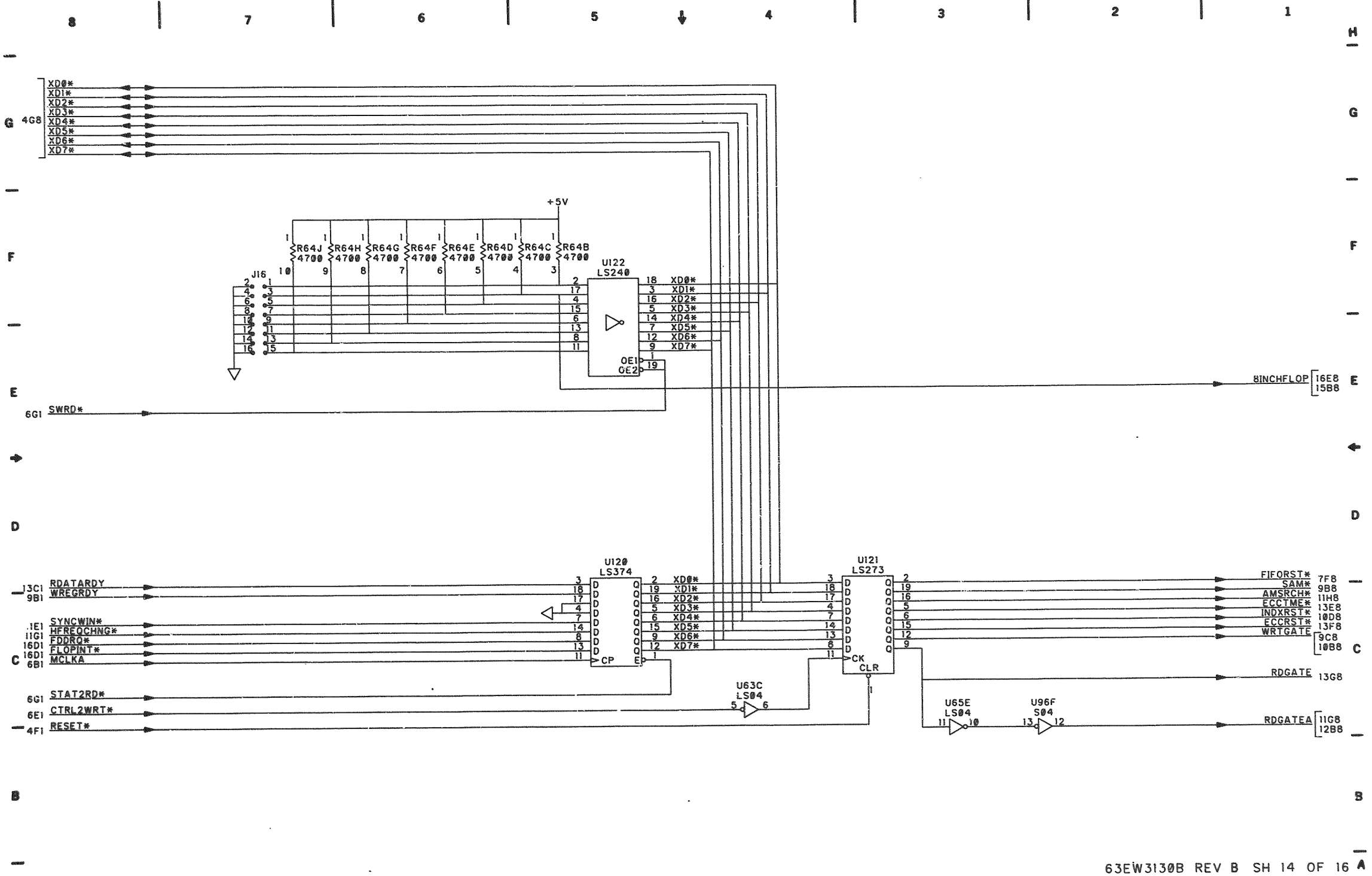
FIGURE 6-2. Module Schematic Diagram (Sheet 12 of 16)



63EW3130B REV B SH 13 OF 16

S0470-13 11-18-82

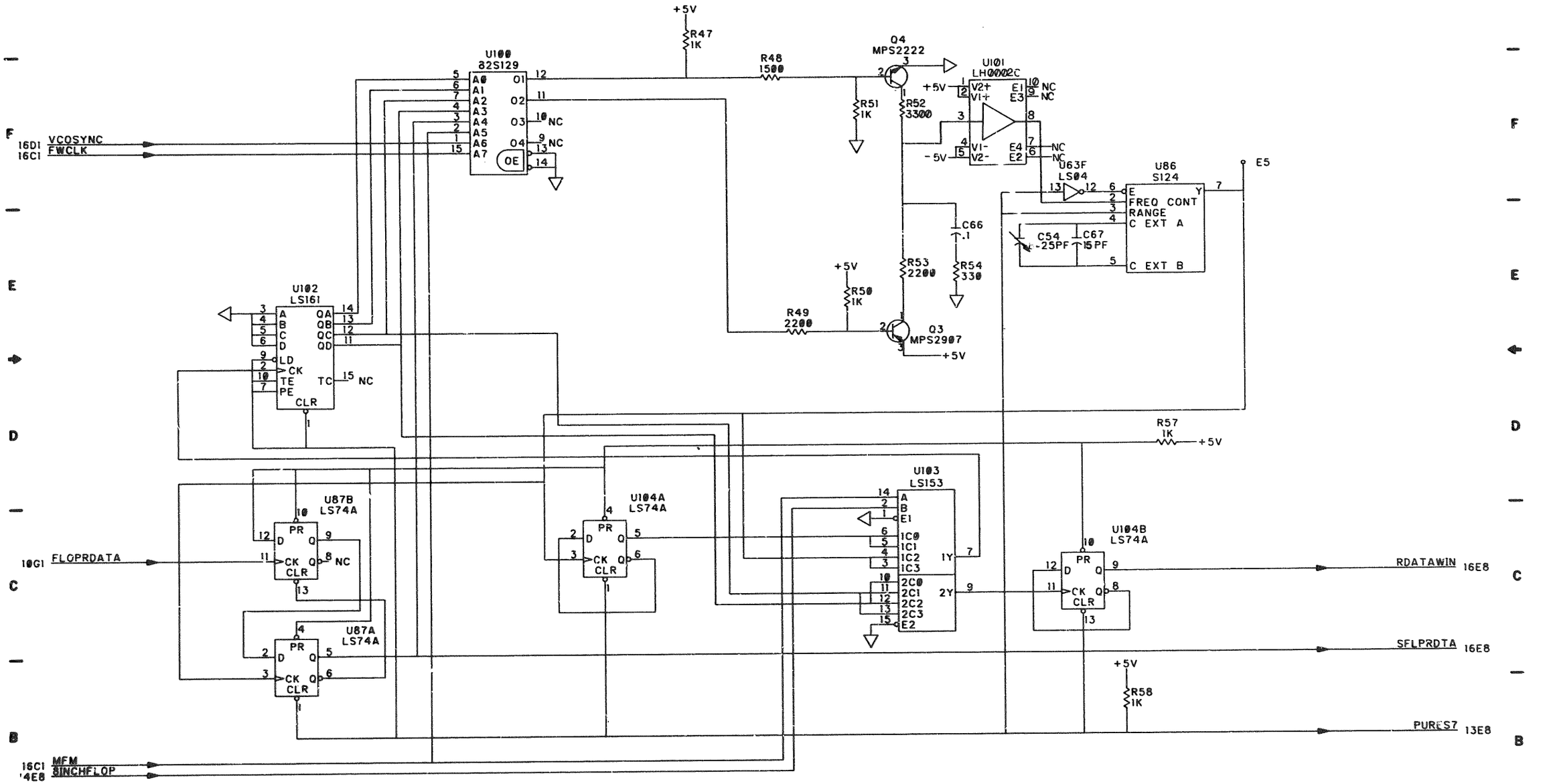
FIGURE 6-2. Module Schematic Diagram (Sheet 13 of 16)



63EW3130B REV B SH 14 OF 16

S0470-14 11-18-82

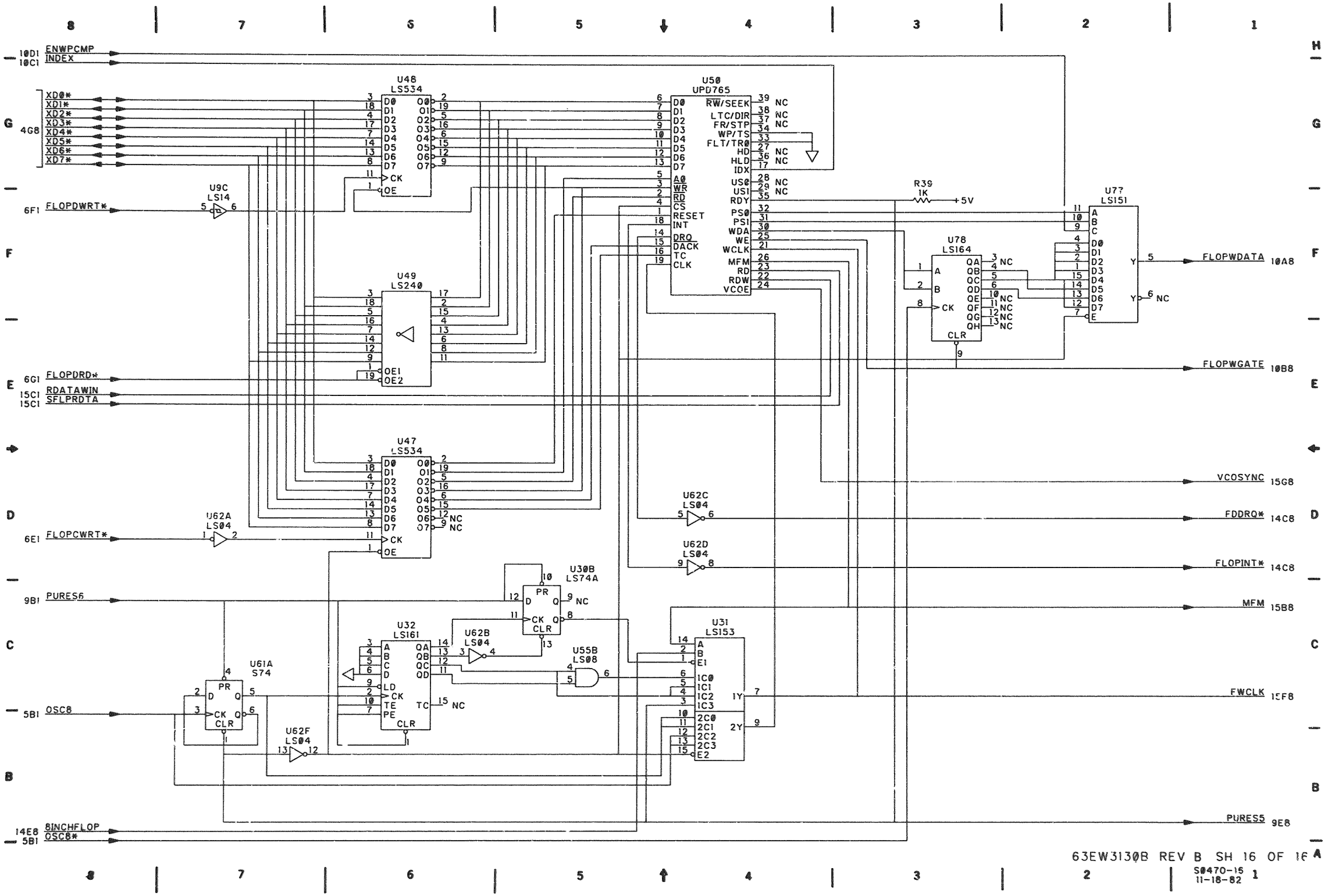
FIGURE 6-2. Module Schematic Diagram (Sheet 14 of 16)



63EW3130B REV E SH 15 OF 16

S0470-15
11-18-82

FIGURE 6-2. Module Schematic Diagram (Sheet 15 of 16)



63EW3130B REV B SH 16 OF 16

S0470-15 11-18-82

FIGURE 6-2. Module Schematic Diagram (Sheet 16 of 16)