3.11 REGISTER EXTENSION AND UTILITY INTERFACE PCB

3.11.1 General Description

The Register Extension and Utility Interface Assembly is a Multi-Function PCB within the Basic 2407 which is utilized to perform the following functions:

- Interrupts - Provision is made for 7 interrupts with selective enables, the necessary logic to interrupt the Processor to address zero and to "save" the address of the aborted instruction.

- Power Rise/Fall Detection - Circuitry is provided to monitor the bulk +5 supply prior to regulation and to provide appropriate interrupts for system power sequencing.

- Memory Expansion - Extension of the Pu "R" register is provided to extend the address capability of the 2407 to 16K words of Program Memory.

- Alarm Clock - A 16 bit "alarm clock" driven by an adjustable multivibrator R/C circuit is provided. The "clock" is presettable under program control and may be used to generate an interrupt when counted to zero.

- Scratch Pad "R" Registers - Two (2) modules of (8) eight scratch pad registers each, are provided to further facilitate programming of the 2407.

- Card Reader Interface - Provides the necessary interface to a 6002/6042 equivalent Card Reader.

- Utility Module Select - Provides necessary circuitry to selectively enable 1 out of 8 Utility Interface modules as decoded via the Microprocessor "X" Register.

- Utility Interface Buffer - Provides the necessary signal buffering logic of the 601 Microprocessor "bus" and "timing" to facilitate Utilities that may be housed within the chassis of the 2407.

3.11.2 Functional Description

In general, the assembly consists of (3) three Utility Interface Modules which are:

A. Interrupt Interface

B. Scratch Pad Interface

C. Card Reader Interface

and provides ample TTL load buffering of the basic microprocessor bus structure and timing, to supply up to (10) ten PCB Assemblies within the basic 2407 chassis herein referenced as the Register Extension Interface (REXTI).

3.11.3 Register Extension Interface (REXTI)

3.11.3.1 Utility Module Select

Utility Interface modules extending beyond the basic 2407 architecture (Ref 2.0 Figure 1) require a selective "enable" before their corresponding "R" Registers can communicate to the 601 Processor. The selective enable is generated as a function of the binary value in the "X" Register of the 601 Processor (Ref 3.3.3).

The REXTI performs a (1) one out of (16) sixteen decode of the lower order bits of the "X" Register (X_0 X_1 X_2 X_3), with the least significant bit being X_0. Also bits X_7, and X_6 must equal a binary value of Ø. Bits X_4 and X_5 are excluded from the decoder logic. The decoder logic generates active select signal lines for "X" having binary values in the ranges of ØØØ through ØØ7 to the External Utility Modules. Obviously, these lines may be extended in the External Modules by including the X register bits X_4 and X_5 to further extend the select values of X for ranges of:

a ØØØ to ØØ7

b Ø2Ø to Ø27

c Ø4Ø to Ø47

d Ø6Ø to Ø67

The decoded values of X=Ø1Ø through Ø17 and their multiple quandrents including X_4 and X_5 are reserved for selection within the basic 2407 (e.g., Card Reader and Scratch Pad).

4.11.3.2 Register Extension Buffers

The TTL circuit drive limit of the main processor block logic has been extended to provide ample loading of a

maximum of (10) ten PCB's (Utilities) with each PCB accepting one (1) unit load per buffered signal.

The logic lines which are buffered are:

1. I bus, bits I_{14}, I_{13}, I_{12}, I_{11}
   a) driving circuit type 74175
   b) 10 unit load fan out
2. "Result Bus" A_7, A_6, A_5, A_4, A_3, A_2, A_1, and $A_\emptyset$
   a) driving circuit type 74H04.
   b) 10 unit load fan out.
3. Sink
   a) driving circuit type 74H40
   b) 20 unit load fan out.
4. ØD
   a) driving circuit type 74H40
   b) 20 unit load fan out.

3.11.3.3 Address Extension Register

The REXTI provides a 2 bit "P" Address Extension Register, which allows the host 601 to reference up to 16K of Program Memory. The Address Extension Register is set from the Result Bus (A) whenever a P-upper Jump is detected.

e.g., ML,ØØØ,P

M , SØ,P.

The output of the Extension Register goes off the card to the "P" Bus and also feeds the Snap "P" Register on the Interrupt Interface (ref. 3.11.4) in the event that an Interrupt is generated. This extension register is set only on jumps. That is, it is not counted over 4K boundaries.

3.11.4 Interrupt Interface R10-13

3.11.4.1 General Introduction

One of the primary functions of this assembly, of course, is the implementation of interrupts in the basic 2407 module. Allowance is made for seven (7) External Interrupt Requests and one generated by the Power Monitoring Circuitry. The Power Control Interrupt Request exists on Channel 7 and is the highest priority request.

Provision has been made for logic by which other on-card functions can easily generate interrupts. For example, the Card Reader Interface and the Alarm Clock logic set bits in the Status Register in such a way that these ... can be "strapped" to any of the (7) seven

External Interrupt Request lines available.

In a given system, these functions need not necessarily generate an interrupt.

Interrupt generation is a function of system design and provision is made for both monitoring their existance of the above by micro-code or connecting them to the interrupt detection and generation logic.

3.11.4.2 Interface Select Enable

A decoded value of X for any one of the following values will enable the Utility to communicate to the processor.

X = Ø17

X = Ø37

X = Ø57

X = Ø77

(reference section 3.11.3.1)

3.11.4.3 "R" Register Assignment

The Interface consists of (4) four "R" addressed functions utilized for Control and Status within the assembly. These Registers have the following assignment:

a) R10 Control Register

b) R11 Utility Register 1

c) R12 Utility Register 2

d) R13 Enable Register.

3.11.4.4 Control Register (R10)

The Control Register is addressed as R10 and is both a "Control" and "Status" register. The Bit Assignment of this register are:

- Bit 7 Interrupt Lock Out - This bit, when set, inhibits the interruption control logic from going through the interruption sequence when enabled Interrupt Request(s) are present. It inhibits the occurrance of any interruption regardless of the state of the selective enable/disable bits as contained in the Enable Register. The Lock Out bit is automatically set on the occurrance of any interruption and may be set by micro-code when R10 is referenced as a Sink with Bit 7 of the result data = 1. It is cleared two jump instructions after the Control Register is referenced as a Sink with bit 7 of the result Data = Ø. A microprogrammed setting of the Lock Out which intervenes between the "clear" command and the second jump instruction cancels the "delayed"

action clear.

- Bit 6 Rise/Fall Power Acknowledge - This assembly contains circuitry which monitors the state of the power supply of the basic 2407 system. In the advent of Initial Power or a Power Failure, it generates a Interrupt Request on channel 7 and the status of Rise/Fall may be sensed in bit 6 of R10.

  On the "rise" of system power, the circuitry provides an automatic start of the system by setting bit 7 and 6 of the Control Register to a logic one (1) indicating a Power Rise, clearing the "P" address register, and generating a interrupt request on Channel 7.

  A "acknowledge" to this interrupt may be generated by micro-code when R10 is referenced as a Sink with bit 6 of the result data = 1. This will clear the Rise/Fall Status bit.

  In the event of power loss, the circuitry generates a Interrupt Request on Channel 7, saves the current "P" address and clears bit 6 of "Status" equal to ø provided the Power Rise had been acknowledged.

An acknowledge to this power interrupt (bit 6, R10) will cause the Processor to sequence to a Stop condition. The Power "Rise" will automatically restart the processor.

There is approximately (30) thirty milise-conds of usable instruction time between the "detection" of Fall Power to the period of "non-Safe" (critical +5 logic supply) logic power. The programmer should sequence the system down in a logical fashion and then issue the "Ack" fall power within 30 milliseconds after detection of a power fall.

- Bits 3 thru 5 of the Control Register Present the channel number (binary-coded) of the highest priority Interrupt Request (which is selectively enabled) which is present at any time. These bits are only a source to the Processor - when referenced as a Sink, they cannot be changed.

  These bits are normally inspected during an interrupt program to determine the cause of an interruption. They may also be inspected while the Interruption Lock/out is set (here an Interrupt Request is set and is thus a potential cause of an interruption once the Lock/out is

cleared. This sort of Interrupt Request is often called a "pending interruption". When all Interrupt Requests are disabled or an enabled Interrupt Request on Channel Ø has the highest priority, the Interrupt Number will be zero. This ambiguity can be removed by the inspection of the Interrupt Request bit.

- Bit 2 Interrupt Request - Bit 2 is zero if there is any existing Interrupt Request on a "channel" which is not selectively disabled. If there is no active Interrupt Request which is enabled, theInterrupt Request bit is one.

- Bit 1 Reader Interrupt/Enable Ack - This bit if logical (1) one when sourced by the Processor signifies that the Data Strobe (IDS) Clock for the Card Reader Interface has made a Active transition and has generated an interrupt on the "strapped" channel assigned. A micro-code result data of Ø sourced to R10 Bit 1 will acknowledge this interrupt and a result data of 1 will enable the next transistion. (Ref section 3.11.5 Card Reader Interface).

- Bit ℘ Clock Interrupt - This bit can only be a source to the processor -- when referenced as a sink no action occurs. If the bit is a logical (1) one, this signifies that the Clock has generated an Interrupt Request if enabled.

3.11.4.5 Utility Registers (R11, and R12) Interrupt Address Clock Function

Registers R11 and R12 perform two functions. In referenced as a source, the Y represent the "captured" value of the "P" Register at the time of an interruption. If referenced as a sink, the Registers are used as a presetable Alarm Clock Register.

- Snap P Register R11 and R12 - When an interruption sequence occurs, the value of the Pu, Pl and P Extension Registers are trapped in a holding Register. R11 if sourced, will contain the "saved" value of PL Address and R12 if sourced will contain the value of Pu.

- Clock Register R11 and R12 - R11 and R12 will sink the result data from the processor to form a 2 byte binary count down register to be used as a RTC. When counted to zero, the RTC will generate an Interrupt Request if enabled. The RTC is available as a strapping option and can be "wire or'ed" to

any of the External Interrupt Request Channels.

The RTC is counted by R/C Multivibrator (MV) circuit whose period is adjustable upon system configuration.

The sinking of result data to R11 and R12 will re start the MV clock and clear the Interrupt Request.

3.11.4.6 Interrupt Enable Register (R13)

This register holds the Selective Enables and Disables for each of the Interrupt Request Channels. It is both a Source and a Sink when R13 is referenced. It is bit position encoded, with bit Ø being the selective enable/disable on Interrupt Channel Ø etc. A logical (1) one in the register implies enable interrupt. Bit 7 is employed to enable Interrupt Requests from the RTC clock since the Power Monitoring Circuitry is always enabled (Channel 7)

3.11.4.7 The Interruption (Interrupt Sequence)

When the interrupt control logic detects an enabled Interrupt Request and the Interruption Lock Out is clear, an Interruption will occur.

The sequence of events which constitute an Interruption are as follows:

- The address of the next instruction of the "main-stream" program to be executed is trapped in the Snap P Register.

- The Interruption Lock Out is set, thus prohibiting any further interruptions.

- The P-Register of the Processor and the P Extension Register of the Interrupt Assembly are cleared, thus producing an automatic branch to address zero.

The initiation of an Interruption is deferred by one instruction time if the Request rises during the execution of:

- An instruction which references R10 or R13 of the Interrupt Interface.

- Any decoded Jump Instruction being executed by the Processor.

Interruptions occur normally in a system operating in instruction step mode (as directed by the Programmers Console). Interruptions are inhibited at any time during which the Programmers Console has Memory Initiates inhibited. (Reference Section 4.0 Programmers Console)

3.11.5 Card Reader Interface

3.11.5.1 General Introduction

The Card Reader Interface consists of the necessary logic to interface to a 6002 or 6042 type MDS Card Reader & enables 80 column cards to be read by the basic 2407 system. Thereby enhancing the architecture for program system support and for general application. (Reference Technical Manual M-1103-0572, 6002 Card Reader).

3.11.5.2 Interface Select Enable

A decoded value of X for any one of the following values will enable the Utility to communicate to the processor.

X = Ø1Ø

X = Ø3Ø

X = Ø5Ø

X = Ø7Ø

(Reference Section 3.11.3.1)

3.11.5.3 "R" Register Assignment

The Interface consists of (2) two "R" addressed functions utilized for Control, Status, and Data and consist of the following:

R14 Reader Data Register (RDR)

R15 Sink - Reader Control Register (RCR)

Source - Reader Status Register (RSR)

3.11.5.4 Reader Data Register (R14)

"R" 14 is a source only register to the processor and contains the "data" information of the Card Reader. The bits of R14 correspond to the Rows as read by the Reader as follows:

- Bit 7 Row 12 Data
- Bit 6 Row 11 Data
- Bit 5 Row 10 Data
- Bit 4 Row 9 Data
- Bit 3 Row 8 Data
- Bit 2 through Ø

  A binary sun decode of row 7 through 1 Data

  e.g., Row 7 + 1 = 7_8

  Row 6 + 1 = 7_8

3.11.5.5 Reader Control Register (R15)

Bit Ø of R15 is used to Initiate and Control card motion by issuing a card "pick" function.

If the "result" data issued to R15 Bit Ø is a logical (1) one, card motion will be initiated and held until the function is removed by issuing a result data of logical (Ø) zero.

A Initiate "pick" followed by a clear "pick" will result in a one (1) card feed action.

The remaining bits of R15 are not used to sink data when referenced.

3.11.5.6 Reader Status Register (R15)

The bits of R15 are used to monitor the Card Reader Status, Strobe Timing of the Data Register and are encoded as follows:

- Bit 7 Data Strobe - This bit when logical one (1) and a card is in motion signifies that the current column of data (reader data register) may be sensed. This Status represents a clocking strobe that samples the rows being read by the Reader logic.

A Interrupt from the transition of this bit may be enabled by the Interrupt Interface (reference Section 3.11.4.4).

- Bit 6 & 5 Are not used and will always appear as logic zero when sourced.

- Bit 4 Card in Read Station - This bit when logical one after a "pick" has been initiated, signifies that card motion has been initiated and that the card has entered and is in the "read photocell" station.

- Bit 3 Pick Fail - This bit will be logical one if a card has not been sensed at the read station within a set time after the "pick" command was initiated. This will remain until the trouble has been cleared.

- Bit 2 Reader Trouble - This bit will be a logical one if any one of the following error conditions exist:

  a) Card Motion error

  b) Light current error

  c) Dark current error.

- Bit 1 Hopper Empty - This bit will be a logical one when there are no cards, or the last card has left the Input Hopper Station or when a Stacker Full condition exists.

- Bit Ø Ready - This bit if logical one, signifies that the Reader is in the Ready state and is able to Accept a "pick" function. Any error condition will cause this bit to be a logical zero (Ø).

3.11.6 Scratch Pad "R" Interfaces

3.11.6.1 Introduction

There are two (2) utility modules of eight (8) scratch pad "R" registers each which are available for program utilization. They are herein described as:

Scratch Pad A (SPA) and;
Scratch Pad B (SPB)

each SP Register may be referenced as a source or sink data by the processor.

3.11.6.2 Interface Select Enables

A decoded value of X for any one of the following values will enable the Scratch Pad Registers to communicate to

the processor.

- SPA Registers R10 through R17

  X = Ø15

  X = Ø35

  X = Ø55

  X = Ø75

- SPB Registers R1Ø through R17

  X = Ø16

  X = Ø36

  X = Ø56

  X = Ø76

3.11.6.3 "R" Register Assignment

Each SP Module may be referenced as R10 through R17 as both source or sink of result data.