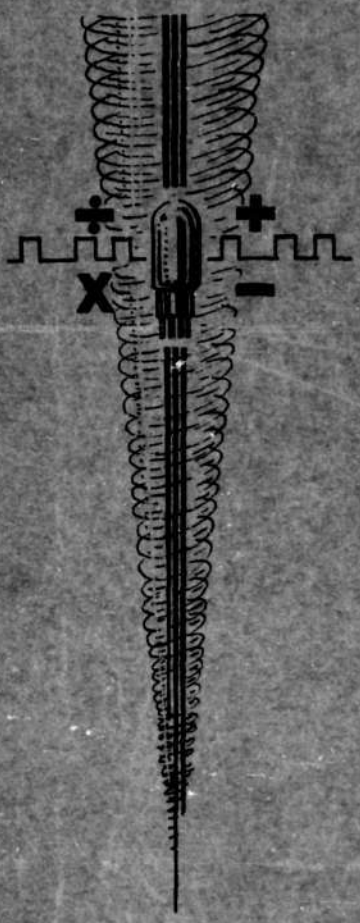

PROJECT WHIRLWIND

Contract N5ori60

SUMMARY REPORT NO. 2

VOLUME 12

INPUT AND OUTPUT
(PART II)

SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Copy 30

SPECIAL DEVICES CENTER

PROJECT WHIRLWIND
Summary Report No. 2
November, 1947

INPUT AND OUTPUT, PART II

Volume II of 22 Volumes

Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

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INTRODUCTION

There are three general types of input and output equipment required for Whirlwind I. These are:

a) Numerical

35 mm film will be used for inserting and extracting numerical information from the Whirlwind Computer. The general outline of the proposed system is given in M-73, Vol. II. The Eastman Kodak Progress Report in Vol. II describes the actual film reader-recorder in more detail. Some project work has been done on automatic conversion on a decimal keyboard to binary numbers on the film. This work is described in a thesis by David J. Crawford in Vol. 12. M-157 describes briefly some of the requirements for an output printer.

b) Mechanical and Electrical

The first work on the conversion from mechanical and electrical information to numerical information for the computer to use in simulation problems was done by H. P. Stabler. His report in Vol. II, entitled Reversible Binary Counter and Shaft Position Indicator describes this work. M-89 in Vol.II describes a simple mechanical to binary converter. The report R-129 in Vol. 12 is a survey by H. P. Stabler of the whole conversion problem from shaft position to binary numbers. Some of these methods are actually conversion from electrical quantities to binary numbers and many of them can be reversed for converting computer output data to physical quantities. The project is continuing work on these problems.

c) Graphical

No reports are given on graphical recorders. It should be possible to use one of the graphical recorders already developed by the Eastman Kodak Company for other purposes.

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A DECADE KEYBOARD FOR A BINARY REGISTER

by

DAVID J. CRAWFORD
S. B. in E. E., Massachusetts Institute of Technology
(1943)

SUBMITTED IN PARTIAL FULFILLMENT OF THE
REQUIREMENT FOR THE DEGREE OF
MASTER OF SCIENCE

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY
(1947)

Signature of Author..../s/ David J. Crawford.....
Department of Electrical Engineering, May 23, 1947

Certified by...../s/ Godfrey T. Coate.....
Thesis Supervisor

...../s/ Harold L. Hazen.....
Chairman, Department Committee on Graduate Students

The author is sincerely indebted to Professor Godfrey T. Coate for advice and encouragement during his supervision of this thesis. The writer is also grateful to Mr. Jay W. Forrester and to all other members of the Project Whirlwind (D.I.C. 6345) Staff for their continued interest and assistance in the work, and to Professor Gordon S. Brown for making available the facilities of the Servomechanisms Laboratory. The author wishes to express his appreciation to Mr. Ray L. Ellis for his aid in the construction of the working model.

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CHAPTER I

Introduction

In an electronic computer being designed at the Massachusetts Institute of Technology,[1] it was decided to use the binary number system as the basis of operation.[2] The binary system is particularly adaptable to use in electrical systems because the binary integers, zero and one, are easily represented by electrical signals of two values. In the past, the principal use of the binary number system has been in electrical circuits used to count a series of events. In this application, the problem of converting the binary count of the circuit into the equivalent decimal number is present. With high-speed computers now being designed to use the binary system of arithmetic, the opposite problem of converting a decimal number to its binary equivalent arises when it is desired to feed data into the machine. The object of this thesis was to create the necessary circuits to convert data from the decimal system to the binary system and to store the result in a binary register.

It is possible for a person to convert a decimal number into the binary system by using arithmetic methods. The result

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1. Under the Division of Industrial Cooperation, Project WHIRLWIND

2. See Appendix, page 63, for description of the binary number system.

could then be recorded on a binary register by pushing buttons that would set up the stages of the register in the correct fashion. Such a method is unduly slow, and for use with a high-speed computer, it is desirable to use a method that uses the fastest capabilities of a human operator. It is believed that a decimal keyboard of the ten-key type with associated circuits to perform the decimal-to-binary conversion automatically is a good approach to the problem. Because the problem has not arisen in the past, there has been little work performed towards the solution previous to this investigation. This paper presents one of the many possible systems that could be used to perform the automatic conversion of a decimal number to the equivalent binary number.

CHAPTER II

The General System

Basis of Operation

Selection of a ten-key keyboard in preference to a matrix-type keyboard automatically determines a requirement of the decimal-to-binary conversion circuit. On a matrix-type keyboard (such as those on a Monroe, Marchant, or Friden calculator), there are ten keys for every digit in the number to be recorded, their physical placement indicating the relation of each digit to the decimal point. For the ten-key type of keyboard (such as the one used in a Sundstrand calculator), the sequence in which the digits are recorded determines their placement with respect to the decimal point. The digits of a number are normally read from left to right, the first digit to be recorded appearing on the left in the recorded result, and the last digit appearing on the right. To accomplish this operation, each time a key is depressed the previously-recorded digits are each shifted one place to the left and the new digit entered in the units column. Shifting the digits one place to the left in the decimal system is the equivalent of multiplying the number by ten. We have therefore made the requirement that our conversion circuits must have some means for multiplying previously-recorded results by ten, each time a key is depressed.

Another requirement of almost any decimal-to-binary conversion system is that some form of binary register is necessary to store the final results. The exact form of the register is determined by other considerations, such as the use of the register to perform operations necessary in the conversion process, but these requirements will be discussed later.

If the previous requirements are met, the actual conversion of a decimal number into its binary equivalent is simplified, because decimal-binary equivalents are required only for the ten decimal integers, zero through nine. These equivalents are as follows:

Decimal Integer	Binary Equivalent
0	0
1	1
2	10
3	11
4	100
5	101
6	110
7	111
8	1000
9	1001

Such a conversion may be accomplished by a relatively simple, matrix-type of circuit.

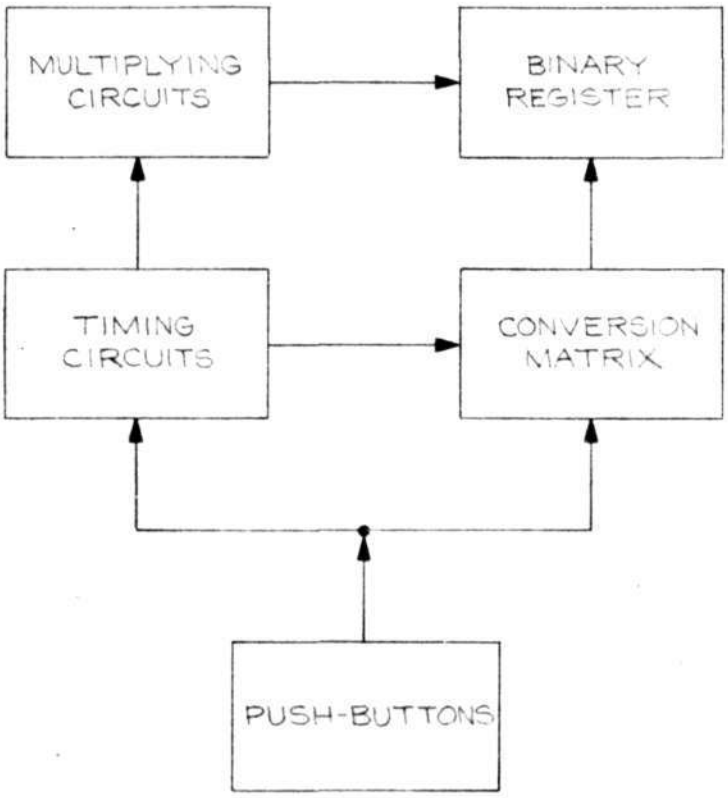
We have now considered all the elements necessary for the complete decimal-to-binary conversion system: a keyboard to enter the decimal number, a binary register for recording the final result, circuits to multiply the number in the register by ten each time a key is depressed, and a circuit to convert a decimal integer into its binary equivalent. A simplified block diagram is shown on A-30568, page 6. The sequence of operations is straightforward. Each time a key is depressed, the number in the register is multiplied by the binary equivalent of ten, and then the binary equivalent of the decimal integer corresponding to the depressed key is entered into the register.

This system will only handle decimal numbers that have no digits to the right of the decimal point. Digits that are to the right of the point, whether in the decimal or binary system represent fractions. There is no simple means of converting numbers of this nature from one number system to the other.

System Details

The push-button circuits are arranged so that depressing any push-button creates a pulse to start the timing circuits. Each button is also connected to a conversion matrix so that the circuits representing the binary components of the decimal integer are turned on. When the timing circuits pulse the conversion matrix, the binary number is added into the register.

Multiplication of a number in the binary system is entirely similar to the process used in the decimal system except that the



SIMPLIFIED BLOCK DIAGRAM OF DECIMAL-BINARY CONVERTER

USED IN D.J.C. THESIS

binary multiplication table is much smaller than the decimal multiplication table. The binary multiplication table is as follows:

$0 \times 0 = 0$ $\qquad$ $1 \times 0 = 0$

$0 \times 1 = 0$ $\qquad$ $1 \times 1 = 1$

Consider the multiplication of a binary number, 10111, for example, by the binary number 1010 (decimal number ten).

10111	multiplicand
1010	multiplier
101110	multiplication by binary 10 or (2^1)
10111000	multiplication by binary 1000 or (2^3)
11100110	result-multiplication by binary 1010 or $(2^3 + 2^1)$

Inspection of this example reveals that the desired multiplication may be achieved by first shifting the multiplicand one place to the left (multiplication by 2^1). This result shifted two additional places to the left is the multiplicand multiplied by 2^3. Adding these two partial products completes the multiplication.

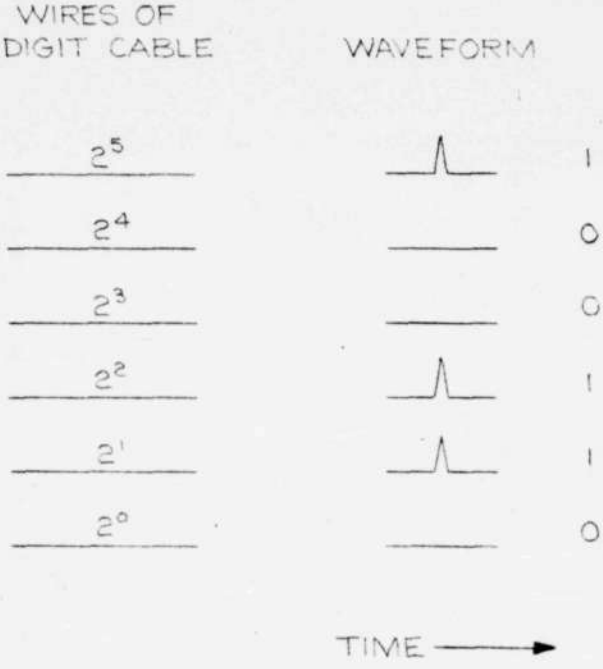
The binary register and associated circuits permit operations that cannot be performed by an ordinary binary counter. The circuits are arranged so that all digits of a binary number may be added into the register simultaneously. By means of a pulse from the timing circuits the number in the register may be shifted one binary place to the left, such a shift being the equivalent of multiplying the number by two. (This is analogous to a shift of a decimal number one place to the left being equivalent to multiplication by ten). Other circuits connected to the register permit the stored number to be read from the register in the form of pulses without erasing the stored number. The combination of these features permits the multiplication of a number in the register by the binary number 1010 in

the manner just described. The timing circuits control the operational sequence.

In view of the details just described, let us again review the sequence of operations that occur when a key is depressed. First, the push-button circuit creates a trigger that starts operation of the timing circuits and turns on the circuits in the conversion matrix that represent the binary components of the decimal integer. The trigger causes the number in the register to shift by one binary place. The number in the register is now read out, shifted two binary places and returned to the register where it is added to the number already present. The multiplication process having been completed, the circuits of the conversion matrix are read and the binary equivalent of the decimal integer is added to the count in the register. This entire process is repeated for each digit of the decimal number until all digits have been entered. At this point, the binary number in the register may be recorded or entered into the associated computer, and the binary register may be cleared.

Representation of Numbers

The binary system lends itself readily to the representation of numbers by electrical means because a zero may be represented by the absence of a signal and a one by the presence of a signal. In the circuits used in this thesis, a parallel method is used to transmit a number from one place to another. Such a scheme is shown in A-30569, page 9. A separate wire is used for each digit of the



TRANSMISSION OF THE BINARY NUMBER 100110

number and all digits are transmitted simultaneously, a pulse on a line representing a one, and absence of a pulse meaning a zero.

CHAPTER III

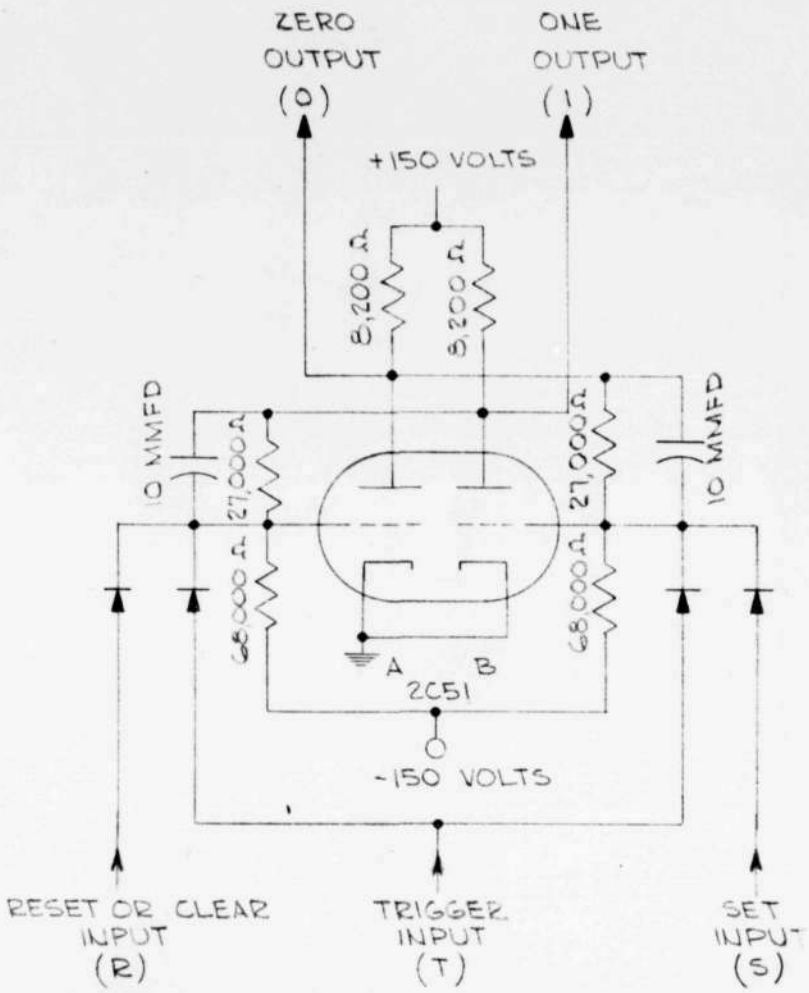
The Binary Register Operation

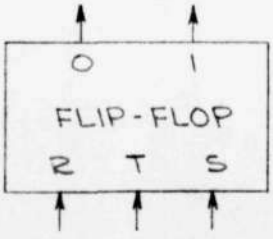
Introduction

The primary purpose of the binary register is to store the final number until needed. If suitable circuits were connected to a set of flip-flops (Eccles-Jordan trigger circuits) the flip-flops could be used as the storage elements. In the practical case, however, the register is used to perform functions other than storage and therefore must be equipped to accomplish these other duties. As previously mentioned, the register must be capable of receiving all digits of a binary number simultaneously and adding them to the number already stored. To perform the multiplication process it must be able to shift the stored number and also have circuits to read the number out of the register and add it back in at a different position. The following discussion will show how this specialized binary register is evolved from the ordinary binary counter.

Components

One of the most common forms of high-speed binary counter utilizes flip-flops as the basic element of construction. Such a trigger circuit (shown in A-30570, page 12) normally has one tube conducting and the other tube biased below cut-off by the condition of the first tube. If a suitable trigger pulse (a pulse of short duration) of either positive or negative polarity is applied to both





BLOCK SYMBOL

TYPICAL FLIP-FLOP CIRCUIT

USED IN D.J.C. THESIS

grids simultaneously, the states of the two tubes will be interchanged, the first tube becoming cut off and the second tube conducting. Another trigger will flip the circuit back to the original position. It is thus seen that two triggers are necessary to perform one complete cycle of operation, the waveform on the plate or grid of one of the tubes rising or falling only once for every two input triggers.

If the condition for tube A to be conducting is considered the zero position of the circuit when used as a binary element, then the first trigger fed to the circuit will flip it into the one position, with tube B conducting. The next trigger will flip the circuit back to the zero position and will cause a sudden negative drop in the plate potential of tube A. If this wavefront is fed into a circuit such as an R-L-C peaker[1], a trigger pulse will result that may be used to drive a succeeding flip-flop stage. Such a pulse is known as a carry pulse and is produced each time the flip-flop completes a cycle.

A reset or Clearing trigger is one that is applied to the grid of tube A and serves to restore the flip-flop from the one to the zero position. Such an operation produces an ordinary carry trigger. However, if the flip-flop is originally in the zero position when the reset is applied, it will have no effect. By coupling a series of flip-flops together through peaking circuits that produce one output trigger for every complete flip-flop cycle, a binary counter is formed. Such a counter is shown in block form in A-30571, page 14.

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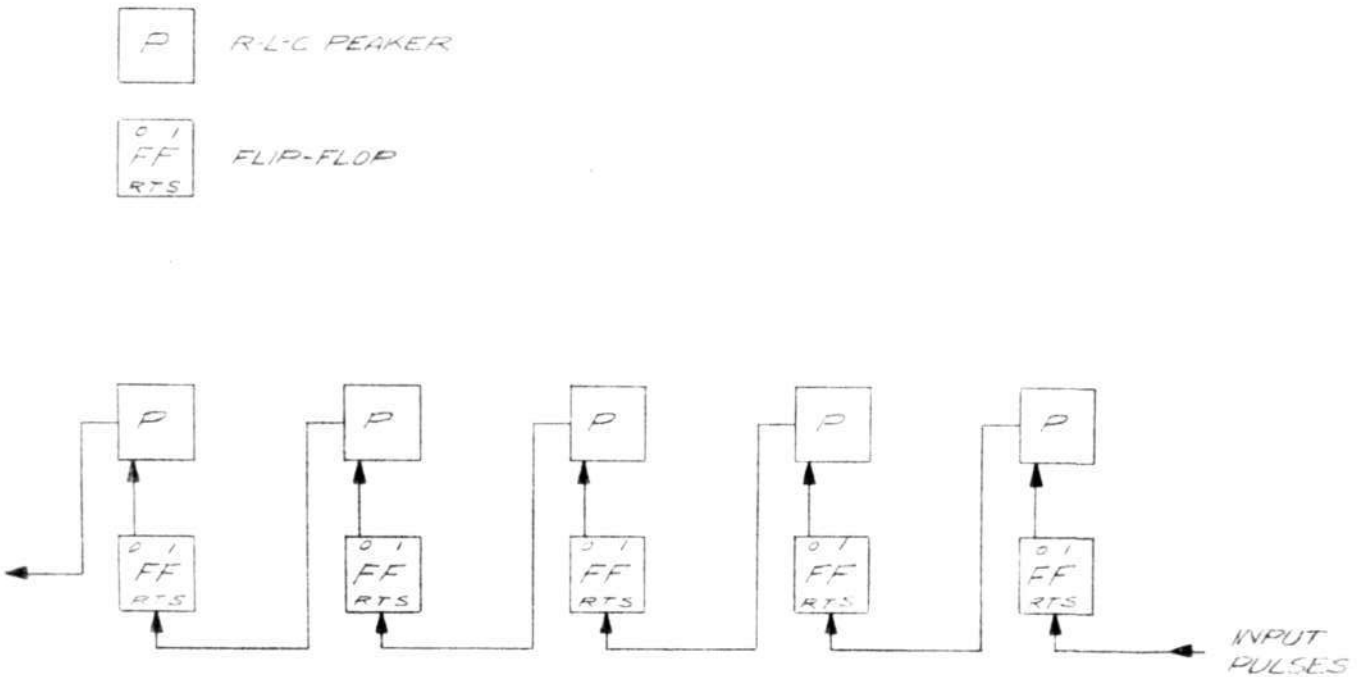
1. The operation of an R-L-C peaker is explained more fully on page 22.

A-30571



BASIC BINARY COUNTER

6345
AJC

A-30571

This ordinary type of counter may be used as a binary storage register, each succeeding stage representing the next higher power of two. To add another binary number to a number already stored in the register introduces complications if an attempt is made to introduce all digits of the new number simultaneously into their respective binary stages. The addition of the new number may generate carry pulses which would interfere with the digits being introduced. Therefore, some modification of the counter is necessary if it is desired to add all digits simultaneously.

The introduction of delay stages overcomes the difficulty in a manner that is described in the next section. When a delay stage receives a trigger pulse, it stores it for a fixed period of time before delivering the pulse at its output terminals.

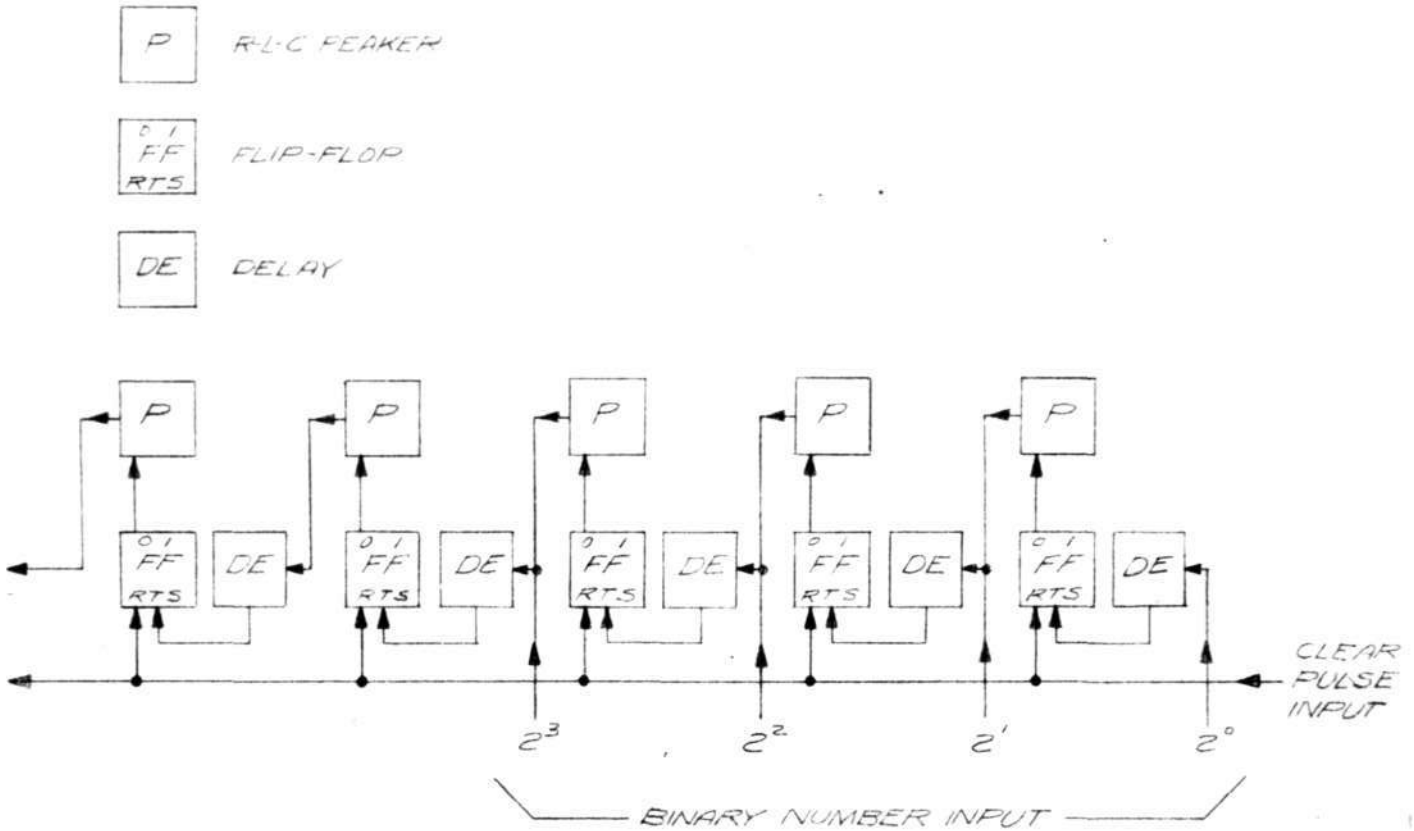
To read a number out of the register, a form of coincidence mixer, or gate circuit, is used. When pulsed, such a reading stage will produce an output pulse only if the flip-flop is in the one position.

Operations

1. Addition

The flip-flops, peakers and delay stages connected to form the binary register are shown in block form in A-30572, page 16. When a number, in the form of pulses, is added into the register, it is temporarily stored in the delay stages until the set of input pulses representing that number have subsided. The delayed pulses are then applied to the flip-flops. If a carry pulse is produced by

A-30572



BINARY REGISTER WITH DELAY STAGES

a flip-flop and its peaker, it passes through a delay stage before reaching the next flip-flop. In this manner, a carry being produced by a flip-flop cannot be interrupted by the input of a carry pulse from a previous flip-flop stage. In other words, a flip-flop always has a chance to reach equilibrium after receiving a pulse before it receives another pulse.

2. Shifting

If a clearing pulse is simultaneously applied to all the flip-flops in the register, all the flip-flops will be restored to their zero positions. All flip-flops that were originally in the one position generate carry pulses when they are restored. These carry pulses therefore represent the number that was stored in the register before it was cleared. The carry pulses are stored in the delay circuits until after the clearing pulse has subsided. When these carries are delivered, the original position of each flip-flop in the register is transmitted to each adjoining flip-flop, or, the number has been shifted by one place.

3. Reading

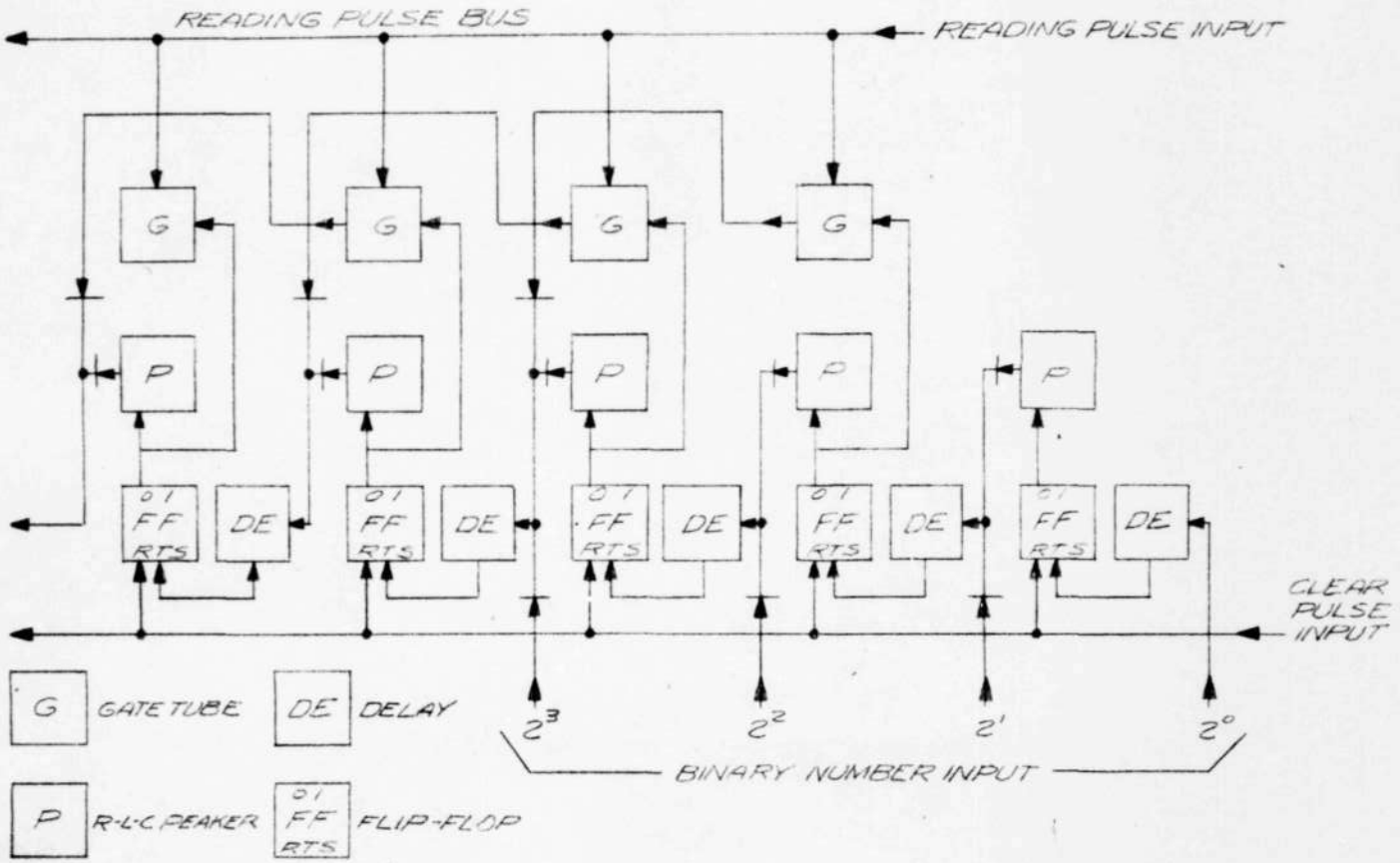
In the multiplication process previously described, after the number in the register has been shifted it is then necessary to read the number out of the register without disturbing the settings of the register flip-flops. To accomplish this result, each flip-flop except the first one in the register has a reading circuit (see page 15) connected to it. The first flip-flop is always in the zero position after a shift so it needs no reading circuit. The

arrangement of these reading circuits with respect to the register stages is shown in block form in A-30573, page 19. Each reading stage is connected so that its output is fed to the delay input of a flip-flop two stages removed from the input of the reading stage..

4. Multiplication

Let us review the multiplication process now that some of the details of the binary register have been described. The correct sequence of pulses to control the multiplication is supplied by the timing circuits that will be described in detail after their requirements have been discussed. First, a clearing pulse applied to all the register flip-flops shifts the number over one place to the left. (Multiplication by 2^1). When the shift has been completed, a reading pulse energizes the reading circuits, obtaining pulses representing the original number multiplied times 2^1. The wiring of the outputs of the reading stages shifts this number two additional places to the left. The number that is added back into the register by the reading circuits is therefore ($2^1 \times 2^2$) or 2^3 times the original number stored in the register. When this partial product is added into the register (which still contains the original number times 2^1), the net result is ($2^1 + 2^3$) times the original number.

A-30573



COMPLETE BINARY REGISTER BLOCK DIAGRAM

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A-30573

CHAPTER IV

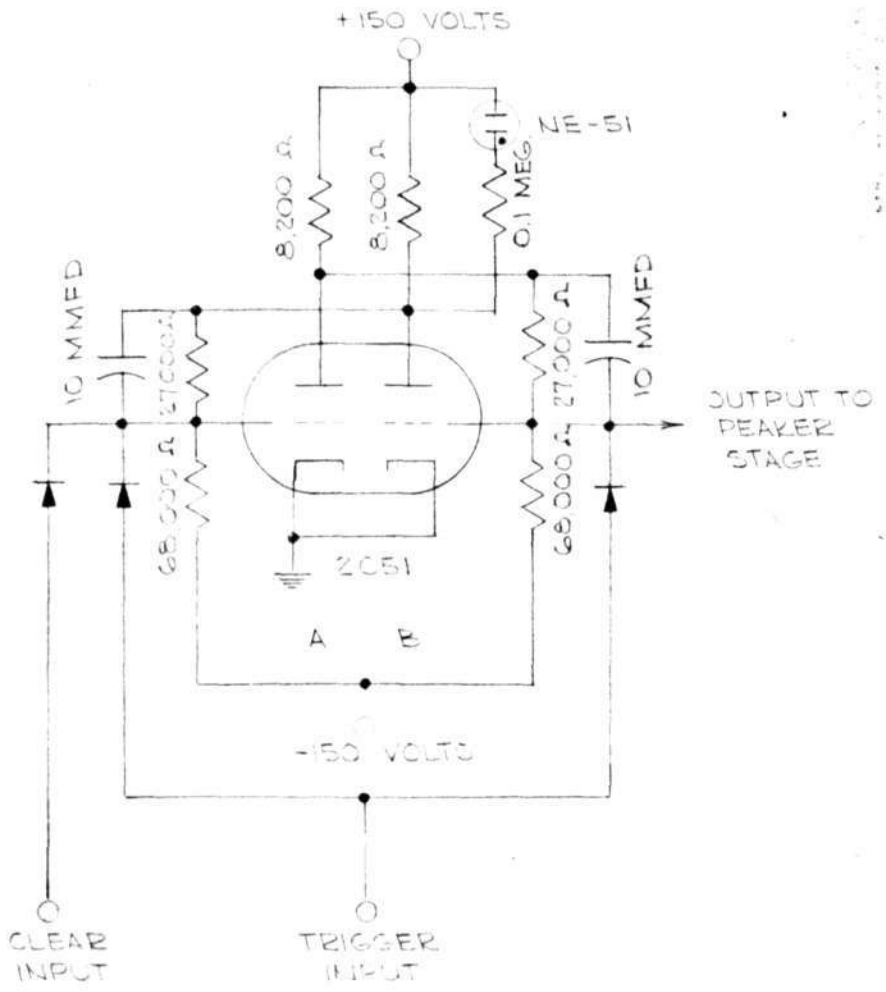
The Binary Register Circuits

In the previous chapter we considered the functions of the binary register and the requirements of the individual components of the register. We will now consider the details of the circuits used.

Flip-flop

The schematic diagram of a flip-flop stage of the register is shown in A-30574, page 21. A positive pulse at the trigger input will cause the circuit to flip over from its original state. All three germanium-crystal diodes are used as decoupling elements. The diodes connected to the trigger input prevent coupling between the two grid circuits, and the diode in the clear input prevents interaction from the other flip-flops on the clearing-pulse bus. The neon bulb glows to indicate the flip-flop is in the one position, when tube B is conducting. The small condensers tend to compensate the plate-to-grid voltage divider for the input capacitance of the tube. Both the clear and trigger input sources are biased below approximately eight volts so they do not interfere with the flip-flop operation.

The flip-flop stage will operate at a trigger repetition rate up to approximately 1.5 megacycles. When used in this decimal-binary conversion circuit the trigger repetition rate never exceeds 0.67 megacycles, so there is a margin to allow for variation



FLIP - FLOP
OF THE BINARY REGISTER

USED IN D.J.C. THESIS

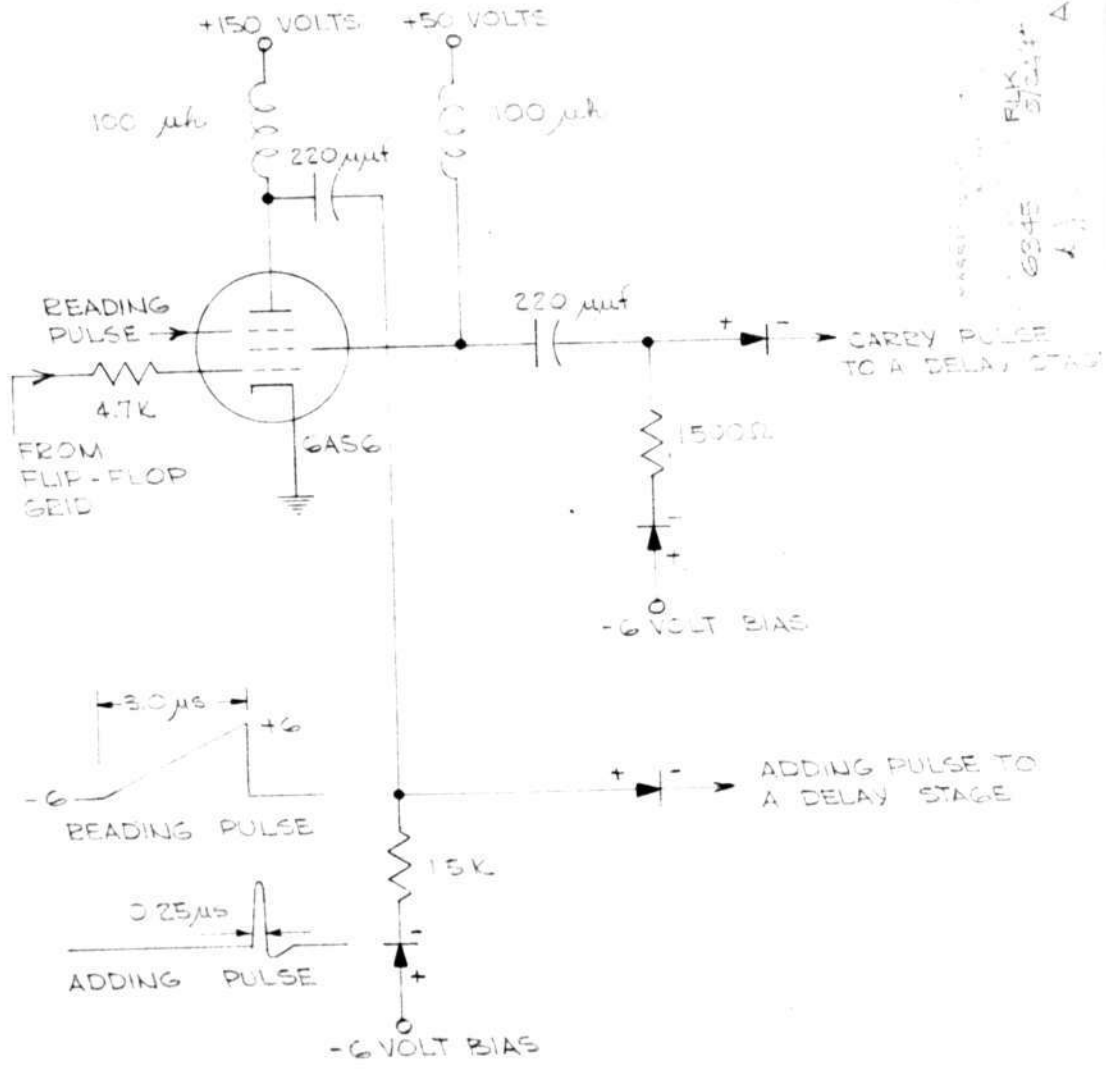
in circuit parameters. The relatively high speed of operation is not essential to the basic principles of the converter when the converter is working from a push-button input. However, the highspeed makes the delay circuits more compact and provides for the possibility that the circuit might be used with high-speed electronic input.

Gate-peaker Circuit

The functions of a peaker circuit to produce a carry pulse from a flip-flop output, and a reading circuit to determine the position of the flip-flop have been combined in a one-tube circuit shown in A-30575, page 23. It utilizes a Type 6AS6 pentode. This tube is especially designed for gating applications, having suppressor-grid characteristics similar to those of its sharp-cutoff control grid.

Let us first consider the operation of the peaker circuit. When the circuit is acting as a peaker, the plate current is cut off by a negative bias on the suppressor grid, and the plate circuit does not enter into the operation. The control grid of the 6AS6 is connected through a series resistor to the grid of the associated flip-flop. The grid of the flip-flop is normally at a positive potential of about 1.6 volts when the flip-flop is in the one position, so the series resistor is necessary to prevent the 6AS6 grid current from loading the flip-flop.

The screen grid of the 6AS6 is connected to its positive supply voltage through an inductor. When the flip-flop connected to the peaker input is in the one position, the control grid of the



GATE PEAKER CIRCUIT

4-30575

USED IN DJC THESIS

6AS6 is slightly positive with respect to the cathode and a current is built up through the screen-grid circuit inductor. When the flip-flop is triggered to the zero position, the screen-grid current of the 6AS6 is suddenly cut off. The interruption of screen-grid current causes an oscillatory transient to appear at the screen grid, the inductance resonating with the stray capacitance. If there were no load connected to the screen-grid circuit, the waveform would be an exponentially damped sinusoidal oscillation with the initial half-cycle positive.

The output of the screen grid is capacitively coupled to a damping resistor that is in series with a germanium diode. The polarity of the diode connection is such that there is practically no damping forthe initial positive swing, but the resistance damps out the oscillation on the negative part of the cycle. The value of the resistance is approximately that required for critical damping so that the transient is damped out in the shortest possible time without a positive overshoot. The output of the peaker circuit is a positive pulse that represents a carry.

When the flip-flop is returned to the one position, the control-grid potential of the 6AS6 is made positive, causing a negative pulse at the screen grid. This negative pulse is overdamped by the tube resistance and the damping circuit, however, and has no effect on succeeding circuits.

Placing the damping circuit after the coupling capacitor has advantages over the more common method of having the damping circuit

directly across the inductor. With the latter method, an extra resistor is required as the d-c return for the coupling capacitor. The extra resistor reduces the positive-pulse amplitude by introducing extra damping. If the resistor has a high value so that it does not appreciably damp the pulse, then there is danger of building up a bias on the capacitor when the next stage draws grid current. Such a condition is usually undesirable, particularly when the random repetition rate of the pulses would make the bias variable. Using the damping circuit as the d-c return for the capacitor eliminates both troubles. The resistance for the positive-pulse voltage is high, and the resistance for negative voltages is low, preventing a build-up of bias.

To read the position of the flip-flop, it is desired to obtain a pulse from the 6AS6 plate circuit if the control-grid voltage of the 6AS6 is positive. The plate circuit is similar to the screen-grid circuit, having an inductor, coupling capacitor, and damping circuit. If the plate current is allowed to build up through its inductor, and is suddenly cut off, the desired positive pulse is produced in the same manner as the pulses of the screen-grid circuit.

Certain precautions must be taken, however. The plate current has a direct effect upon the screen-grid current, an increase in the plate current causing a decrease in the screen current. If the plate current is abruptly increased, the sudden decrease in screen-grid current causes an undesired positive pulse from the screen-grid circuit. If the plate current is increased at a rate that

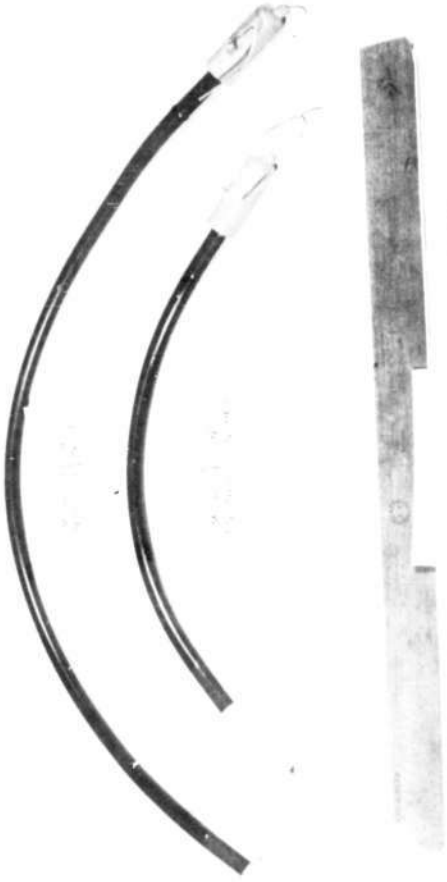
is slow compared to the period of the oscillatory transient, the slow decrease in the screen-grid current cannot produce a pulse.

The correct result is obtained by driving the suppressor grid with a sawtooth waveform. This voltage, known as the reading pulse, slowly increases the plate current (if the associated flip-flop is in the one position) and then abruptly cuts it off. A positive pulse is produced at the plate that represents the digit stored in the flip-flop and is called an adding pulse. A small negative pulse is produced at the screen grid which does no harm.

Delay Stage

The delay stages used in the binary register had to meet two main requirements. The first has already been described, namely, the circuit should be able to receive a pulse at its input, store it a definite period of time, and then deliver a pulse at its output. The nature of the particular carry circuits used in this register imposes the second requirement. The delay stage must be able to receive an input pulse at the same time it is delivering a pulse at its output. This second requirement eliminates from consideration ordinary multi-vibrator-peaker combinations, although special circuits could probably be designed. It was also desired to keep the number of tubes per binary-register stage down to a minimum.

Commercial, continuous-wound delay lines seemed to offer a good solution. These lines come in a variety of lengths and impedances, and are relatively convenient to use. A photograph of two of these lines is on page 27. The delay line could have been used in a straightforward



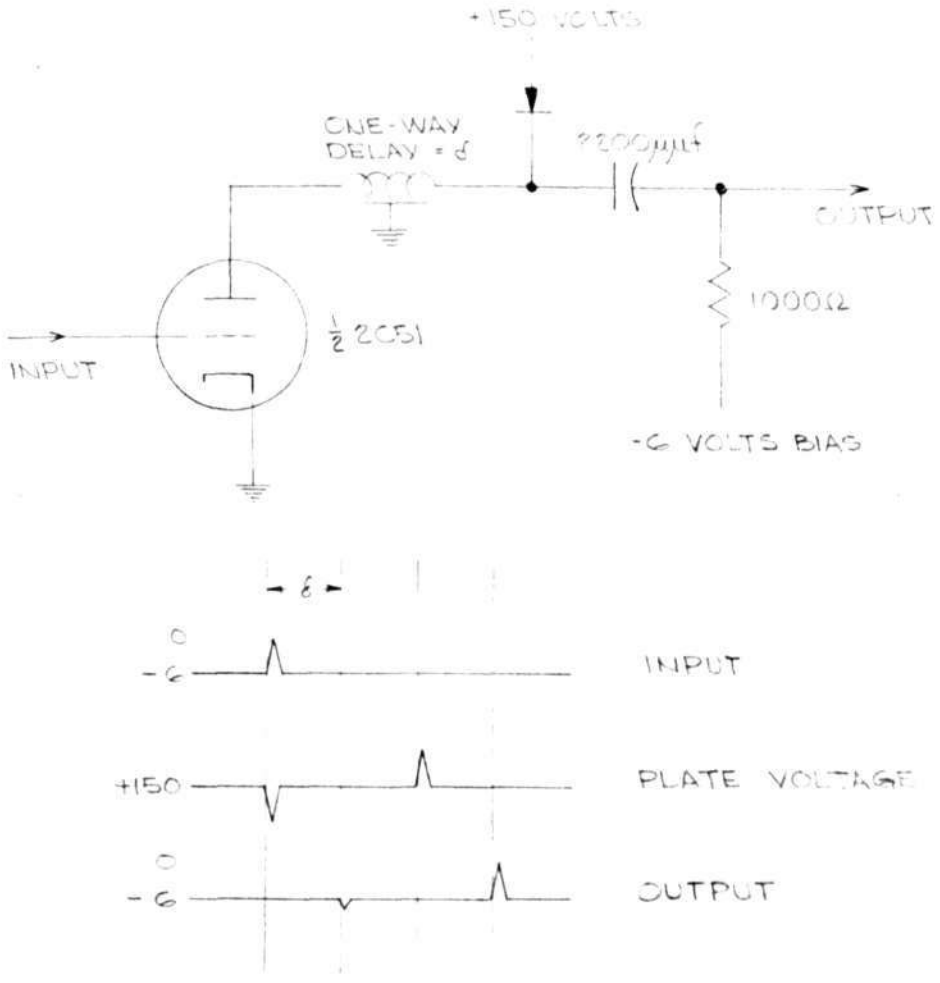
1000-OHM DELAY LINES

A-30563

circuit where the pulse is fed in at one end of the line and received at the other. The characteristics of the twin-triode flip-flops were such that it was felt a delay of at least one microsecond was necessary, more delay being desirable. A one-microsecond delay line is about twenty-two inches long, and such a line in each register stage would cause considerable contructional difficulties.

More delay per unit length was achieved by taking advantage of reflections. A single-reflection scheme, whereby a pulse of one polarity applied to a line is reflected at a short-circuit at the far end and returned as a pulse of opposite polarity, could not be used because the input and output circuits of the delay stage had to be independent. Drawing A-30576, page 29, shows the circuit used. The tube is normally biased below cutoff by the grid circuit. The grid receives positive pulses from a diode mixer that serves to isolate the two or three circuits that may feed the grid.

When a positive pulse is applied to the grid, the line temporarily appears as its characteristic impedance (1,000 ohms), and a negative pulse is generated across the line. The negative pulse travels down the line and after the one-way delay time of the line (0.5 microsecond) it appears at the far end. This end of the line is terminated in a germanium diode in parallel with the characteristic impedance of the line. The polarity of the diode is arranged so that it appears as a low resistance (approximately 100 ohms) for a negative pulse and a high resistance (greater than 0.1 megohm) for a positive pulse.



DELAY STAGE SCHEMATIC

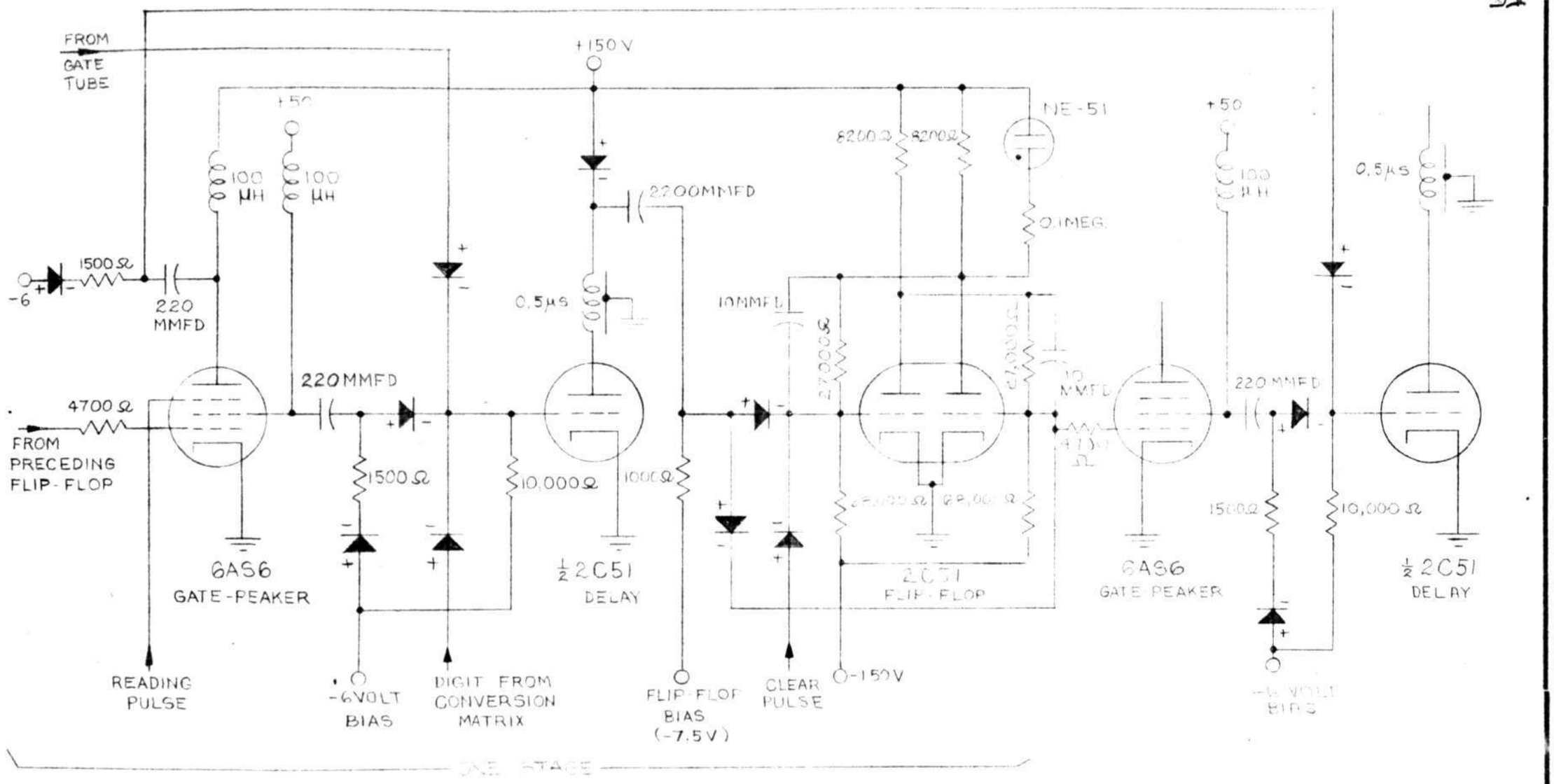
USED IN DJC THESIS

Because the line appears to be terminated in much less than its characteristic impedance, the negative pulse is returned to the tube as a positive pulse. When the positive pulse reaches the end of the line it is reflected without change of polarity, because the tube is cut off and appears as an open circuit. The reflected positive pulse travels through the line and appears across the terminating resistor at the output. As in the damping circuit for the peakers, coupling the terminating resistor through a capacitor possesses advantages. The total delay between input and output pulses is equal to three times the one-way delay of the line.

Register Stage

A single stage of the register is shown in B-30577, page 31, to illustrate the methods used to couple the stages together. Germanium diodes form mixers wherever it is necessary to feed several inputs into one point. They serve to isolate the stages. Such a need arises at the input to some of the delay stages, where it is necessary to feed carry pulses from the preceding stage, adding pulses from another stage and digit pulses (to be described later) from the conversion matrix. Direct coupling is used between the flip-flop and the peaker stage because the time between successive operations may be measured in microseconds or hours. Capacitive coupling is used to pass the pulses because they are approximately 0.25 microsecond wide and the repetition period is never less than 1.5 microseconds.

A complete stage of the register requires three triodes and a pentode, or two and one-half tube envelopes if twin triodes are used.



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BINARY REGISTER STAGE of D-B CONVERTER

SCALE:	DR.	B-30577
ENG.	CK.	APP.

USED IN DJC THESIS

CHAPTER V

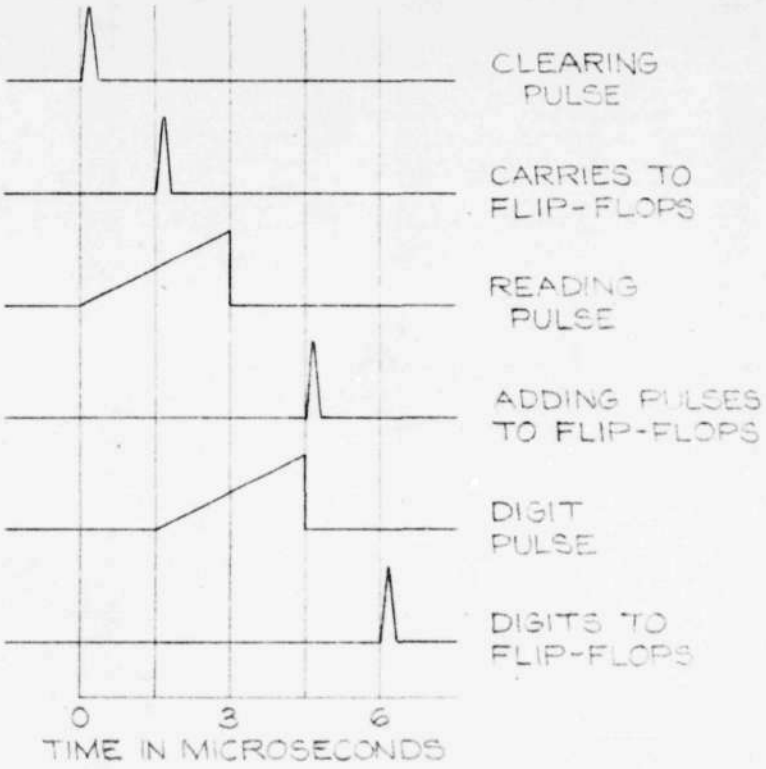
The Timing and Conversion Circuits

Timing-Circuit Requirements

The details of the binary register automatically determine most of the requirements of the timing circuits. The important waveforms are shown on A-30578, page 33. The operations, broken up into units of time (each unit 1.5 microseconds long), are as follows:

1. Clearing pulse initiated by push-button circuit which clears register flip-flops and generates carries. Carries stored in the delay stages.
2. Carries delivered from delay stages to the flip-flops, completing the shift of the number in the register.
3. End of reading pulse causes reading circuits to read the number out of register and add these adding pulses, shifted over by two places, into the delay stages.
4. Delay stages deliver the adding pulses to the flip-flops, completing the multiplication. End of digit pulse reads the binary digits of the decimal integer from the conversion circuit into the delay stages of the register.
5. Binary digits delivered from the delay stages to the flip-flops. Action of the circuits are complete except for any carries that might propagate throughout the register.

The above sequence requires three waveforms from the timing circuits, the clearing pulse, the reading pulse, and the digit pulse.



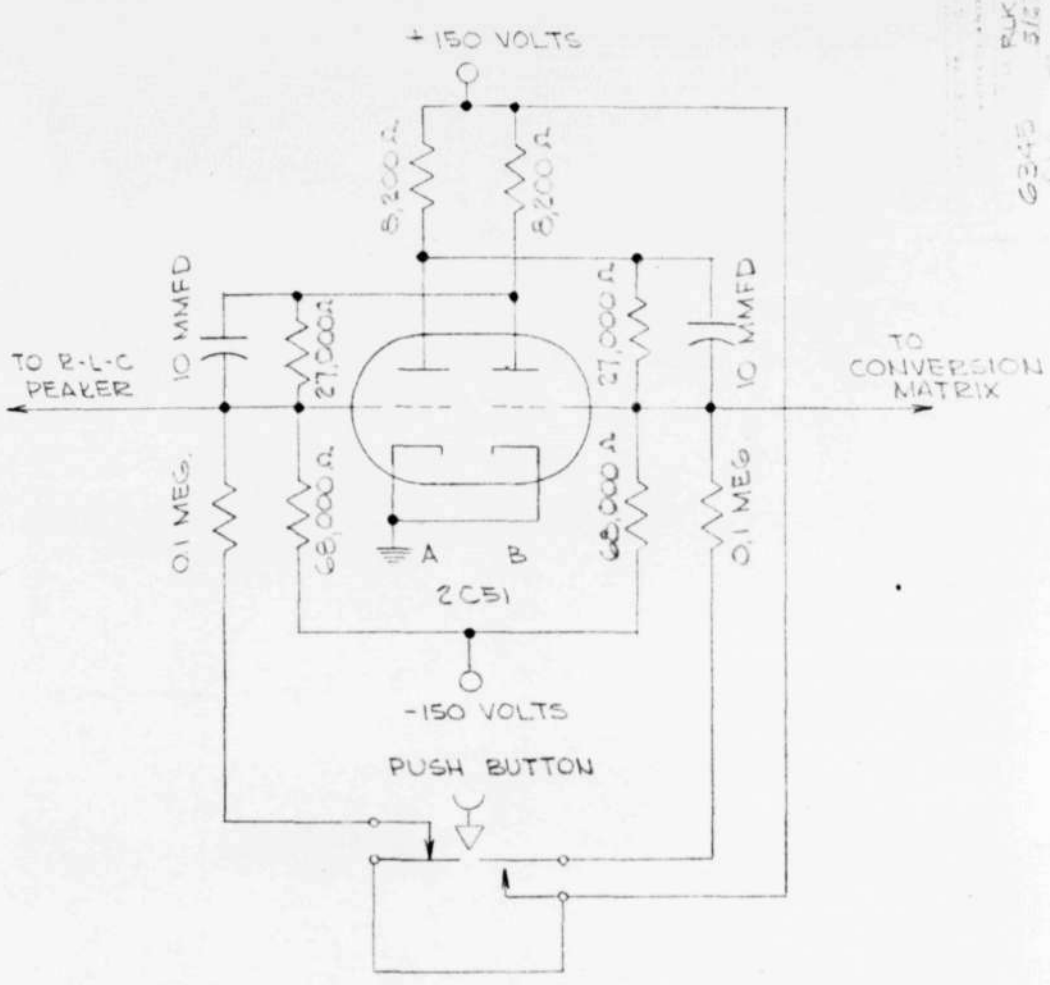
TIMING RELATIONS IN DECIMAL-BINARY CONVERTER

Because the digit pulse energizes circuits in the conversion matrix that are similar to the reading circuits of the register, it can be of the same shape as the reading pulse.

Push-Button Trigger Circuit

Because a push-button type of switch does not make a definite contact when it is depressed, a circuit must be used to insure that only one trigger is produced for each push-button operation. The first scheme attempted was the use of a flip-flop that was connected to the switch contacts. The diagram is shown in A-30579, page 35. With the circuit at rest, the normally closed contacts of the switch apply a positive potential to tube A of the flip-flop, insuring its conduction and therefore keeping tube B cut off. If the button is pushed, the normally closed contact of the switch is opened, having no effect on the flip-flop. When the button reaches the bottom of its travel, the other contact is closed, applying a positive potential to tube B of the flip-flop, causing the circuit to flip to its other stable state. Once the condition has been established, the circuit remains in that state regardless of breaks in the switch contact. When the push-button is released, the other contact is again closed, restoring the flip-flop to its original condition.

This scheme requires a flip-flop for each push-button, the grids of the flip-flops being connected through a diode mixer to an R-L-C peaker stage. The connections are arranged so that pushing any button cuts off the R-L-C peaker, producing a positive pulse. The other set of flip-flop grids are connected to the conversion matrix to set up the binary digits of the decimal integers.



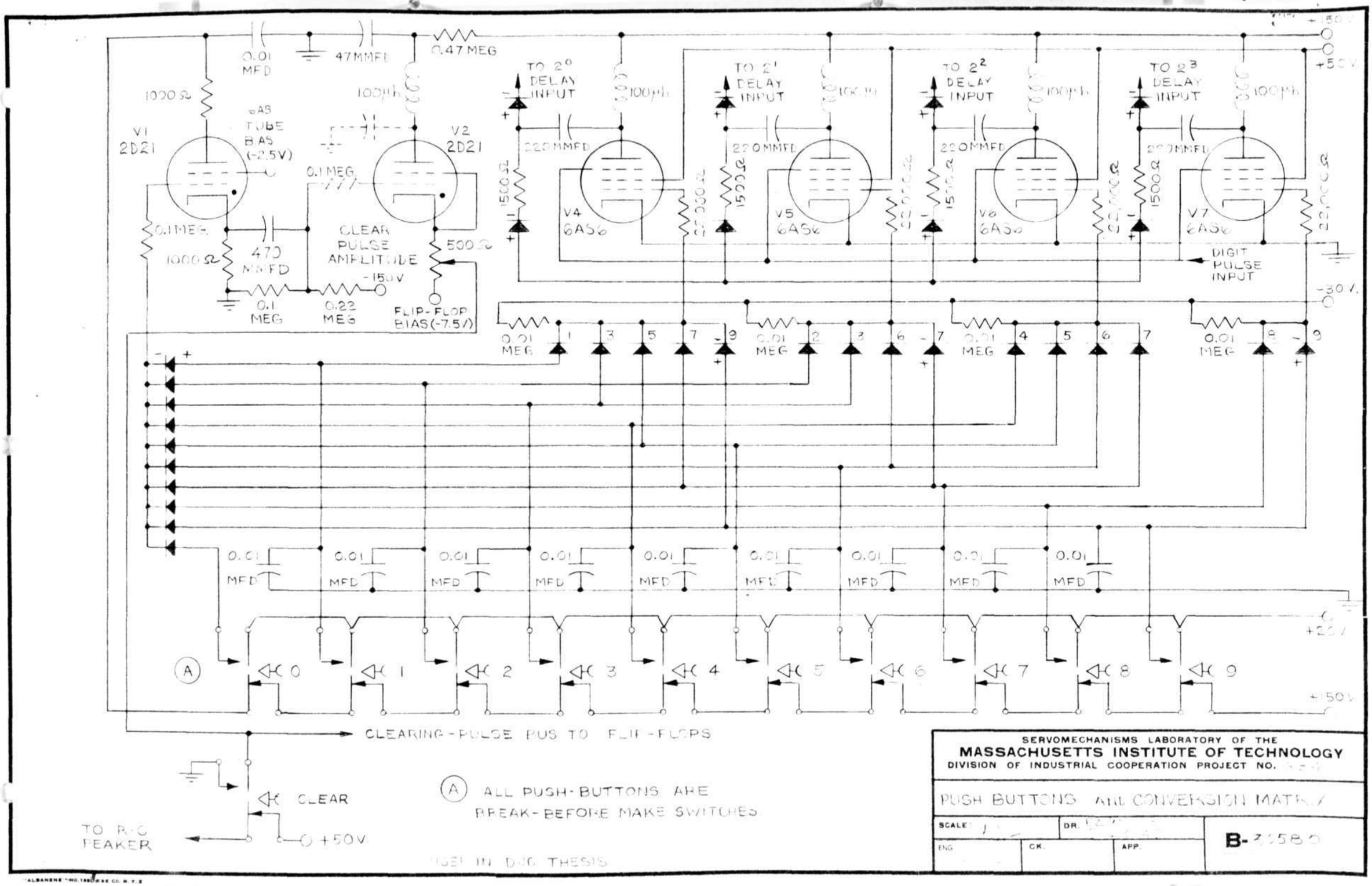
PUSH-BUTTON CONTROLLED
FLIP - FLOP

USED IN DJC THESIS

Besides requiring many tubes and circuit components, the flip-flop stages were not always stable under the severe operating conditions. The back resistance of the germanium-diode mixer circuits produced a heavy load on the flip-flop grid circuits. This loading, plus the long length of grid leads that were necessary, made the flip-flop operation erratic.

The flip-flop circuits connected to the push-button were discarded in favor of a simpler circuit composed of two gas-filled thyratons shown in B-30580, page 37. One side of all the normally open contacts of the push-buttons is connected to a positive potential of about twenty volts. The other terminals of the contacts are connected through a diode mixer to the grid of gas tube VI. There is also a parallel set of connections to these terminals that goes to diode mixers in the conversion matrix. These connections to the matrix normally provide a negative bias of about thirty volts, so that the gas-tube grid voltage is below firing potential. A negative bias on the shield grid makes the firing point of the control grid a positive potential of about eighteen volts. The normally closed contacts of the push-buttons are connected in a series circuit that permits the charging of a 0.01 microfarad capacitor to a positive potential of 150 volts.

Pushing any button breaks the charging circuit, temporarily leaving the capacitor with a net charge. When the bottom contact of the switch is closed, the control grid of the gas tube is connected to a positive, twenty-volt potential, and the tube fires, discharging



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PUSH BUTTONS AND CONVERSION MATRIX

SCALE: 1	DR.	B-33580
ENG.	CK.	APP.

ALBANENE MFG. 1880 K&E CO. N. Y. 2

the capacitor. The discharge produces a positive waveform across the cathode resistor that has a sharply rising front and an exponential trail-off. When the condenser voltage drops below a critical point, the tube goes out. The circuit cannot be operated again until the push-button is released and the condenser has time to recharge, therefore only one pulse may be produced for each push of a button.

The output pulse of thefirst gas tube does not have the correct amplitude or waveshape to act as a clearing pulse for the register flip-flops. It serves to fire the second thyratron which has a pulse-forming network in its plate circuit. The network consists of a small capacitor, an inductor, and the stray plate-to-ground capacitance of the tube. Such a pi-type network may be considered as a section of an artificial transmission line. It is normally charged up through a resistor to the 150-volt supply potential. When the wavefront from the first gas tube fires the second tube, the network is discharged, producing a single positive pulse across the cathode resistor. The pulse is about 0.25 microseconds wide at the base, and the amplitude of the output may be adjusted by means of the CLEAR-PULSE AMPLITUDE potentiometer. This second gas tube circuit could not be operated directly from the push-buttons because the storage capacitors are so small they would lose their stored charge through stray leakage during the time of push-button travel. The cathode resistor is returned to a negative bias so that the output may be directly coupled to the register flip-flop stages.

Conversion Matrix

The conversion circuits to change the decimal integers into their binary components are also shown in B-30580, page 37, and consist of four diode mixers to prevent interaction between the push-button circuits, and four gate tubes (coincidence mixers) to act as reading circuits. Each gate tube represents a binary digit and the output of each stage is connected to the delay input of the flip-flop in the register representing the particular binary digit.

The normally open contact of each push-button is connected through germanium diodes to the grid circuits of the gate tubes representing the binary components of the particular decimal integer. For example, the number seven push-button is connected to the 2^0, 2^1, and 2^2 gate tube grid circuits ($7 = 2^0 + 2^1 + 2^2$).

When a button is depressed, the grids of the associated gate tubes are turned on by the positive potential supplies through the push-button contacts. After three time units (4.5 microseconds), the gate tubes that have their control grids positive, transmit their digits into the register when the digit pulse suddenly cuts off the plate current by means of the suppressor grid.

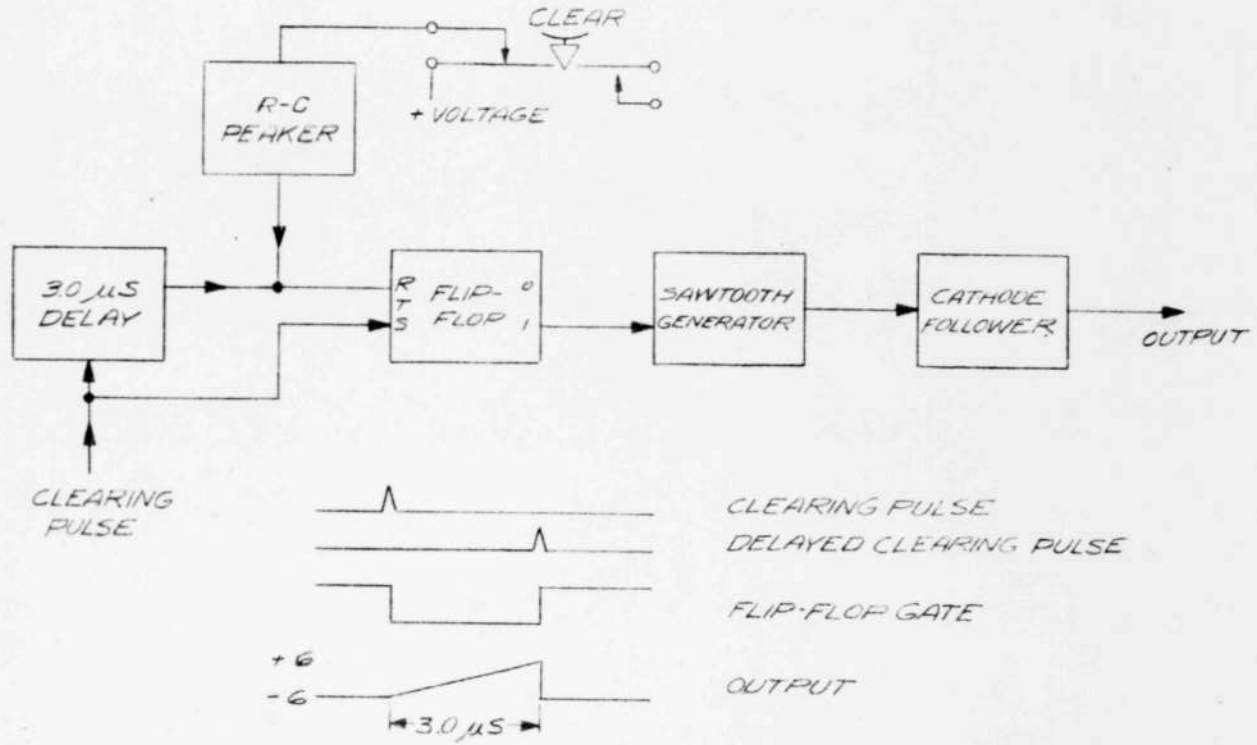
The potential applied to the control grids of the gate tubes is connected through series resistors so that grid current prevents the grids from being driven appreciably positive. The grid-return resistors are connected to a source of minus thirty volts bias to keep the tubes normally cut off. The grid-return resistors have a low value so that when adjacent gate tubes are turned on, the back

resistance of the diodes in the mixer circuits will not raise the bias of a non-energized stage above cut-off.

It is essential that the correct gate tubes have their grid voltages positive 4.5 microseconds after the push-button fires the gas tube that generates the clearing pulse. If no precaution were taken, it is possible for the push-button to make an intermittent contact that would fire the gas tube, yet permit the gate tube grids to be biased off 4.5 microseconds later when the digit pulse is supposed to read the digits from the gate tubes. To overcome this difficulty, a capacitor is connected from each push-button contact to ground, and the firing point of the gas tube purposely adjusted so that it is about eighteen volts positive. The push-button contact must be made long enough (about twenty microseconds) to charge the capacitor up to the firing voltage of the gas tube. Even if the contacts open at the instant the tube fires, the time constant of the condenser discharge is large enough so that the potential of the condenser will still be positive 4.5 microseconds later.

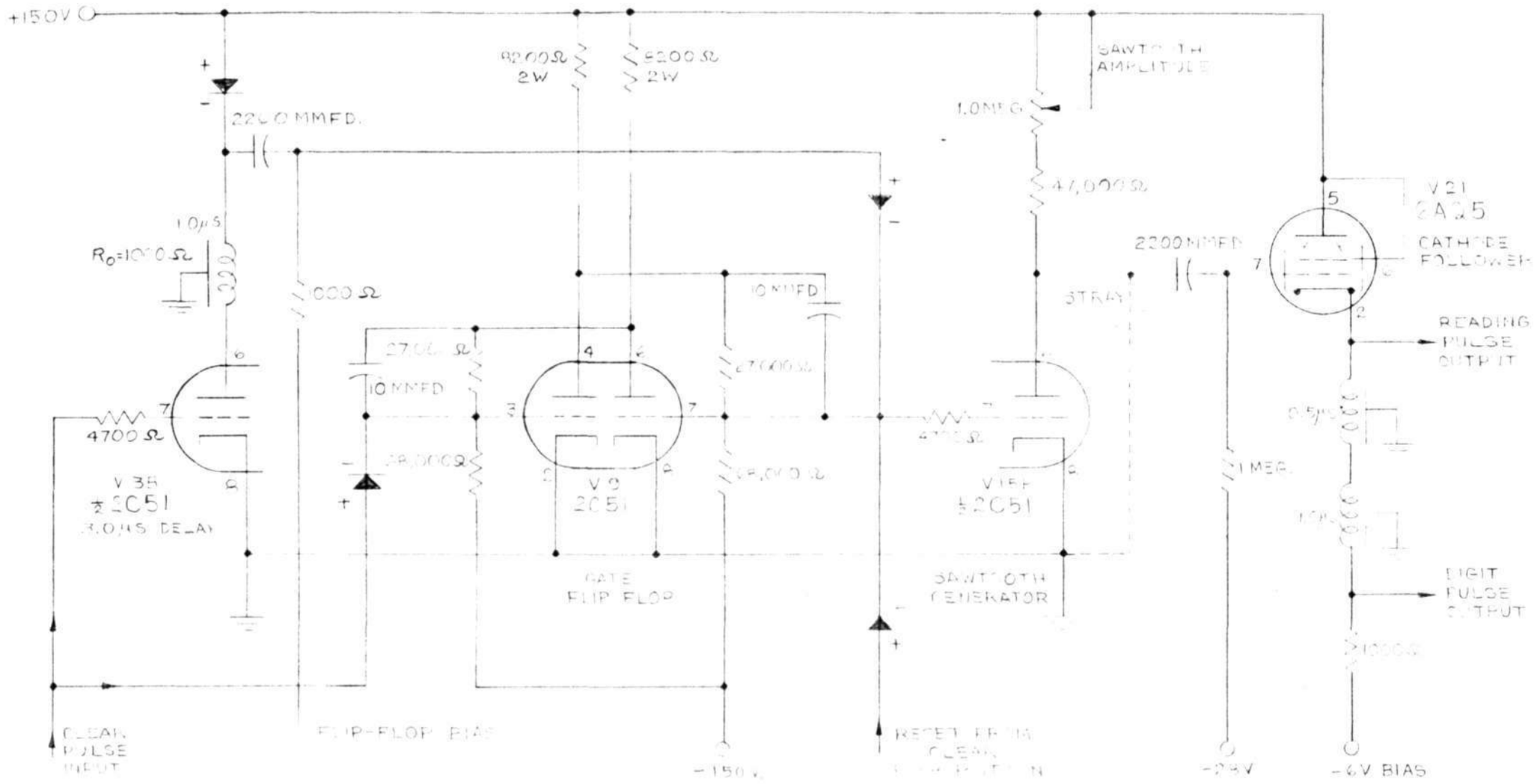
Reading-pulse Generation

The waveshape requirement on the reading pulse is that it should rise slowly and have an abrupt drop. The rise may start at any time after the clearing pulse and the drop should occur two time units (3.0 microseconds) after the clearing pulse. The circuit to generate this pulse is shown in block form in A-30581, page 41, and in detail in B-30582, page 42. It consists of a flip-flop and delay stage that is used to generate a gate three microseconds long, a sawtooth generator controlled by the gate, and a cathode follower output stage.



READING PULSE GENERATION

6345 SMA 5-27-43
HJC A-30581



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DIVISION OF INDUSTRIAL COOPERATION PROJECT NO.

SAW-TOOTH GENERATION CIRCUIT

SCALE:	DR.	B-
ENG.	CK.	APP.

USED IN D.C. THEO.

The flip-flop, which is normally in the zero position, is triggered into the one position by the clearing pulse. The clearing pulse is also applied to a delay stage. After three microseconds, the delayed clearing pulse is delivered to the opposite side of the flip-flop, resetting the flip-flop to the zero position. The whole operation produces a negative, three-microsecond gate that is applied to the sawtooth generator.

The sawtooth generator is a triode with a high value of resistance in series with the plate. The tube is normally conducting until the gate from the flip-flop cuts it off. When this occurs, the stray plate-to-ground capacitance is charged by current from the plate resistor. The plate voltage therefore rises towards the supply voltage exponentially. Before it rises by more than about forty volts, the three-microsecond gate ceases and the low resistance of the tube discharges the stray capacitance quickly, causing an abrupt fall in the plate voltage. The amplitude of the sawtooth that is produced is controlled by resistance of the SAWTOOTH AMPLITUDE rheostat which varies the time constant of the exponential rise.

The sawtooth is capacitively coupled to a triode-connected 6AQ5 cathode follower. This relatively high-perveance tube was necessary to feed the combined parallel load of a 1,000-ohm delay line, a 1,000-ohm output cable for a possible additional chassis, and the supressor grids of all the gate tubes. Because the suppressor grids are diriven positive, they form an appreciable load.

When the CLEAR push-button is depressed, complications arise, because the CLEAR button grounds the clearing-pulse bus. The operation leaves the gate-generating flip-flop in the one position unless a reset method is provided. To perform the reset, the normally closed contacts of the CLEAR button are wired so that they produce a positive pulse when the button is released, which is applied to the flip-flop.

Digit-pulse Circuit

The digit pulse to read the gate tubes of the conversion matrix has no requirement on shape except that it must suddenly cut off the suppressor grids one time-unit (1.5 microseconds) after the end of the reading pulse. For convenience, the digit pulse is formed by delaying the reading pulse through 1.5 microseconds of delay line terminated in its characteristic impedance. No simple means of using delay-line reflections to shorten the required line being available, the thirty-four inches of delay line were used directly.

CHAPTER VI

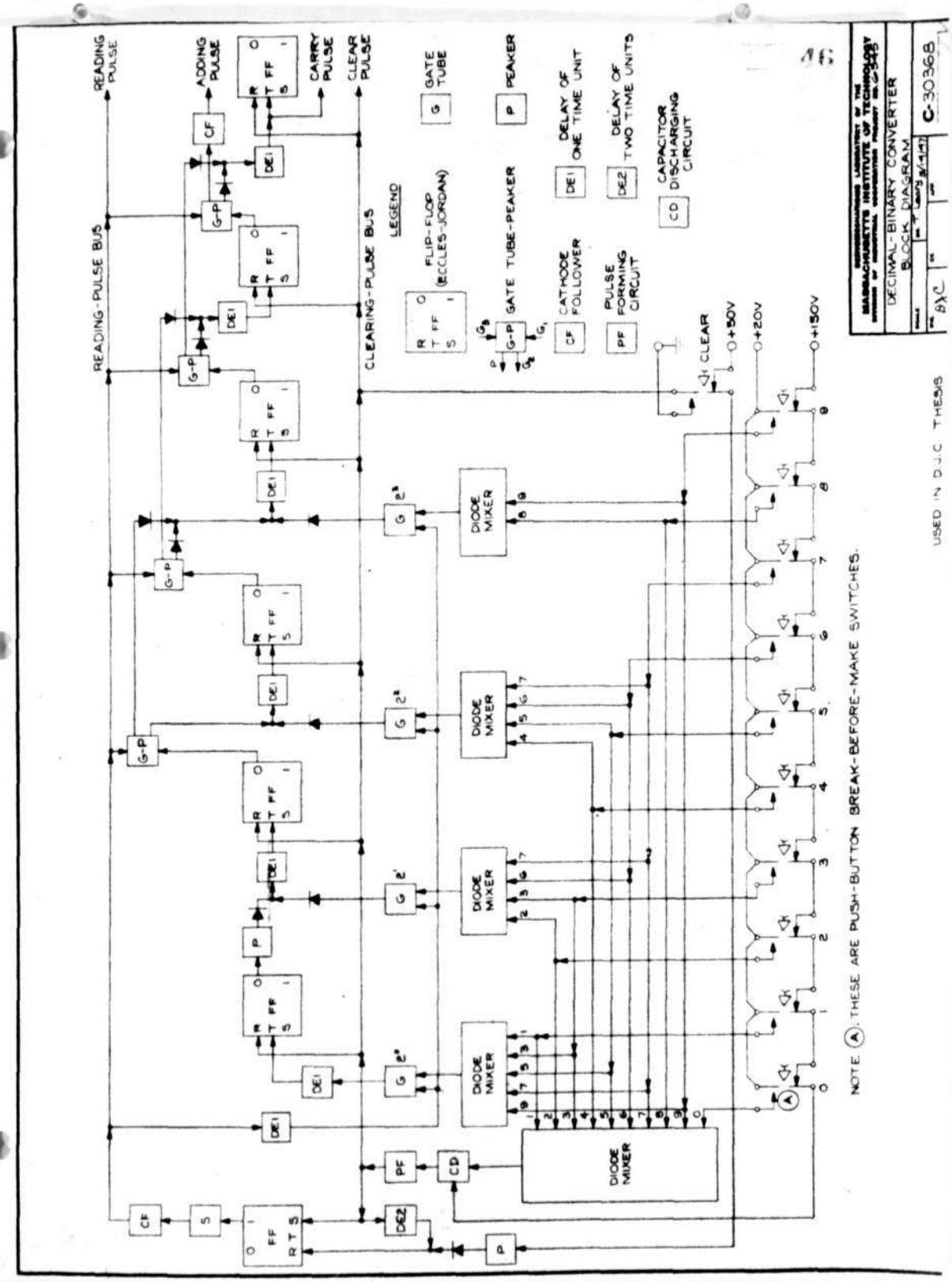
Construction and Operation

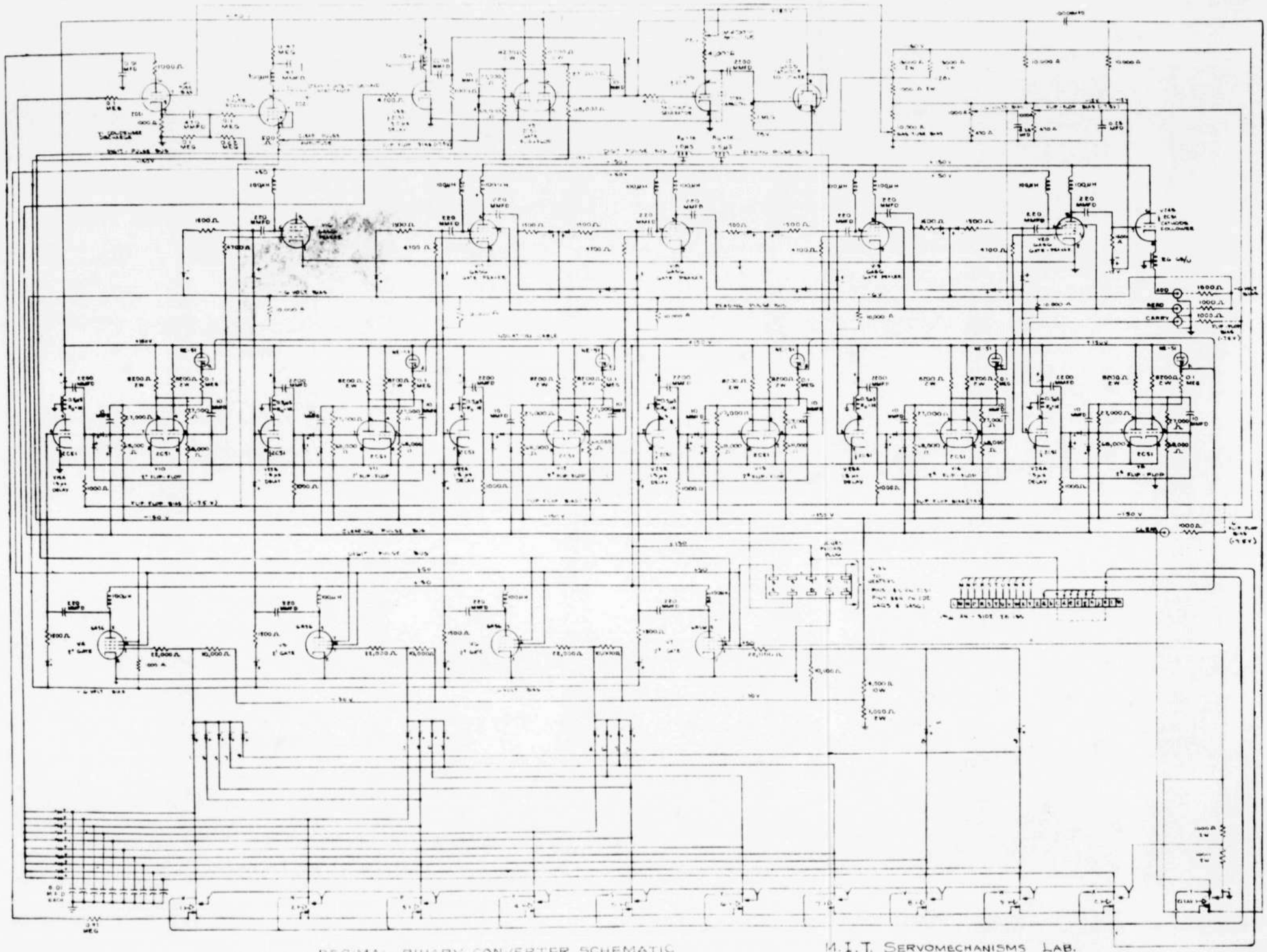
The Completed Unit

The block diagram of the whole unit is shown in C-30368, page 46, and shows how the basic parts of the converter are interconnected. The complete schematic diagram shown in E-30583, page 47, has the circuits placed in approximately the same arrangement as the block diagram. Five complete register stages were built, plus a sixth flip-flop that had no associated gate-peaker stage.

The entire unit, exclusive of power supplies, was built on a 13 by 17-inch chassis. Photographs are shown on pages 48 through 53. The chassis contains a set of input push-buttons, complete circuits to perform the decimal-to-binary conversion, neon bulbs to indicate the converted number, coaxial output jacks for connections to a chassis containing additional register stages, and a plug to connect a remote keyboard and neon-light unit. The coaxial outputs are designed for use with type RG-65/U, 1,000-ohm cable that may be terminated in its characteristic impedance when connected to an additional register chassis.

The elimination of the flip-flops associated with the push-button in favor of the gas-tube circuits accounts for the ten empty tube sockets on the chassis. At some future date some of these flip-flops may be converted into additional register stages, so they were left intact.



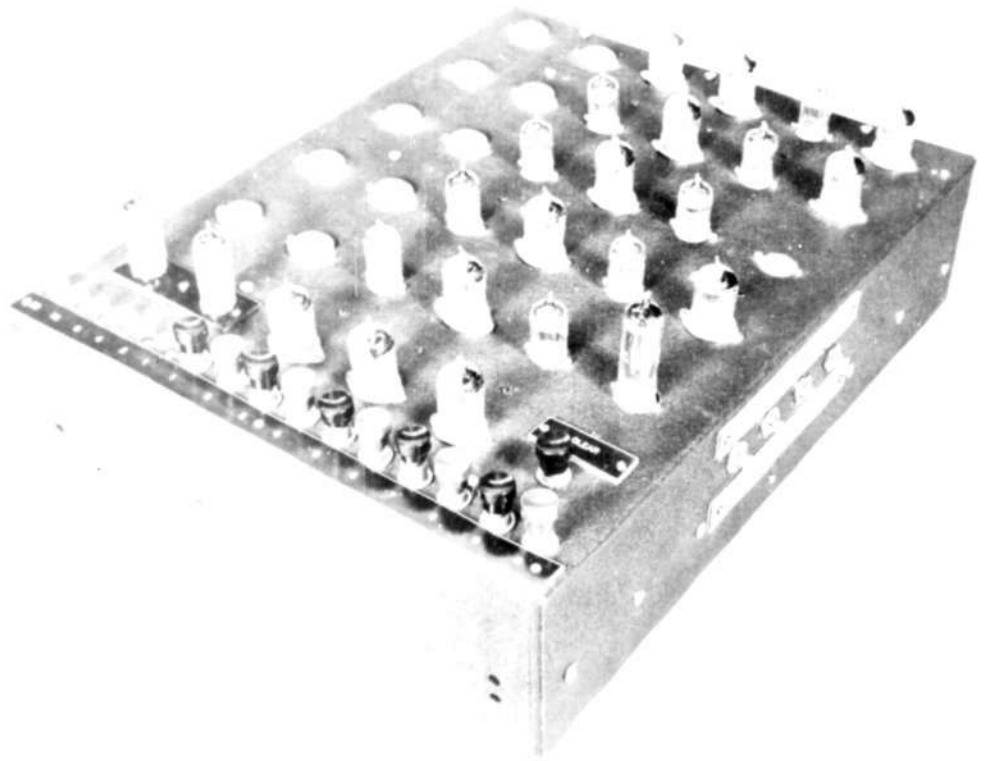


DECIMAL-BINARY CONVERTER SCHEMATIC

M.I.T. SERVOMECHANISMS LAB.
D.I.C.-C345 Drawing E-30593

A-30561

CHASSIS, FRONT VIEW



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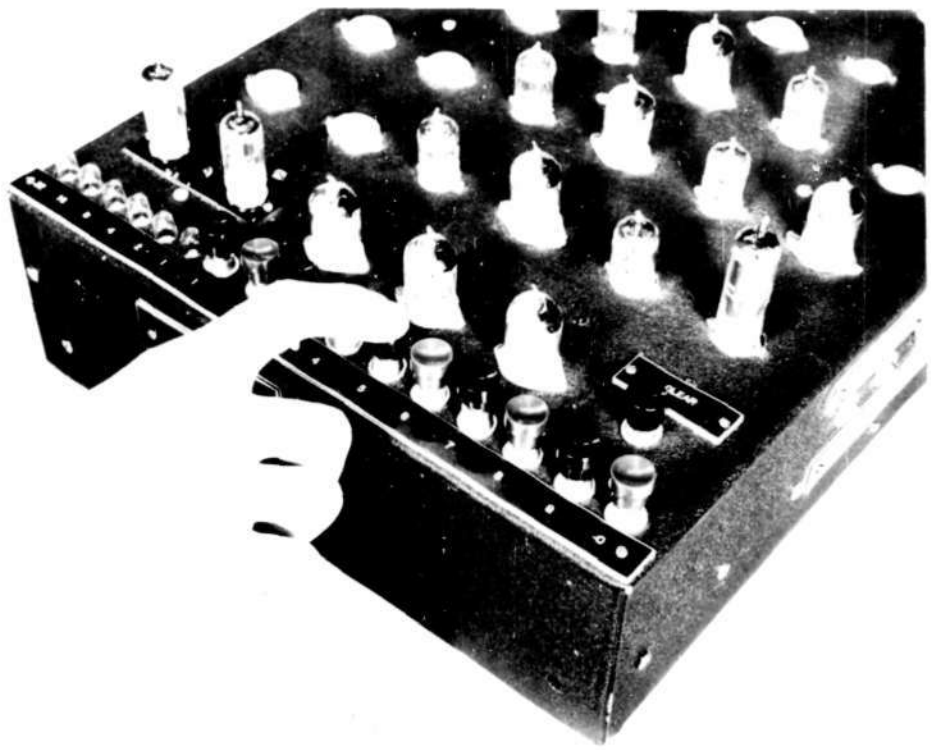
ENG. D. J. C.	A.F.	A-30561

A-30565

THE KEYBOARD



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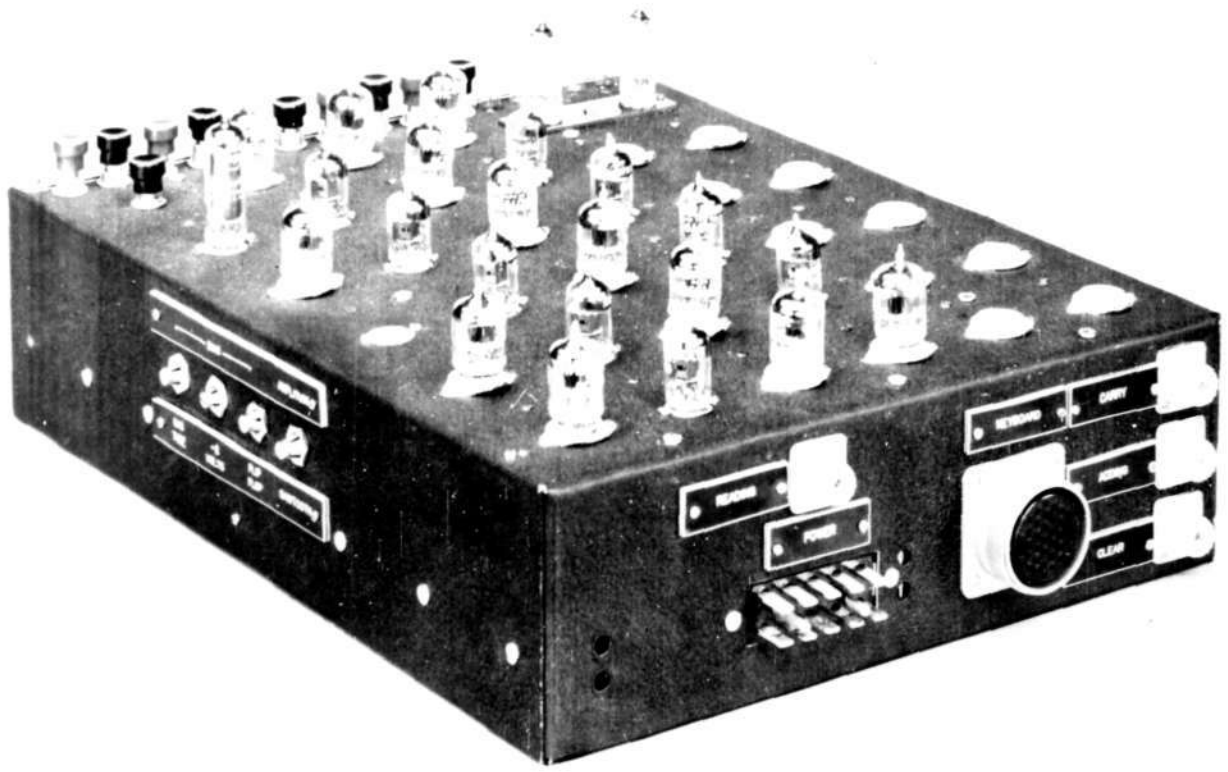
CHASSIS, END VIEW



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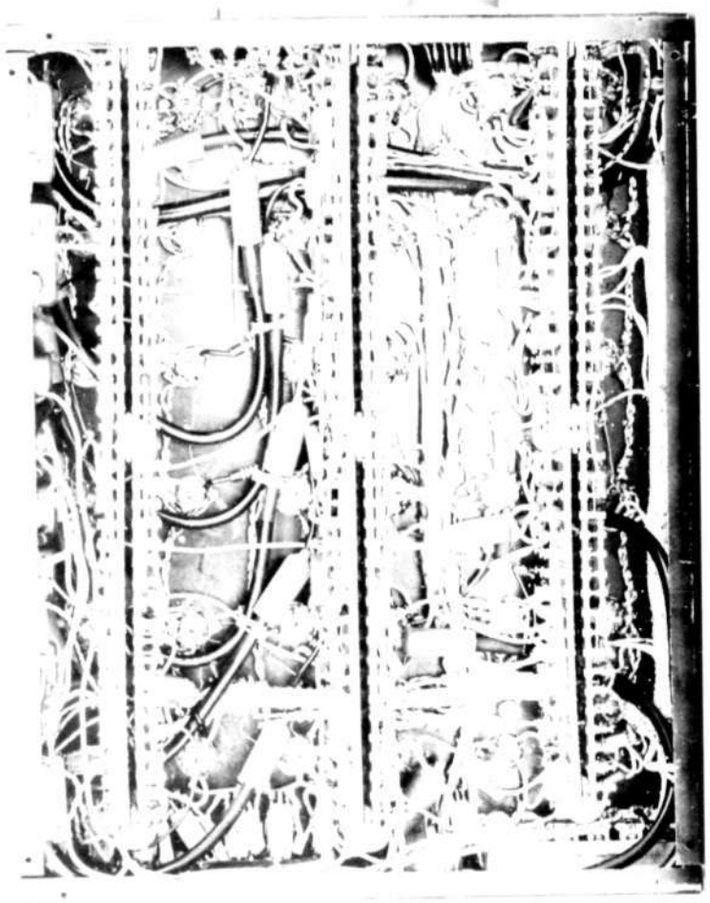
CHASSIS, BOTTOM VIEW

A-30560

USED IN D.I.C. THESIS



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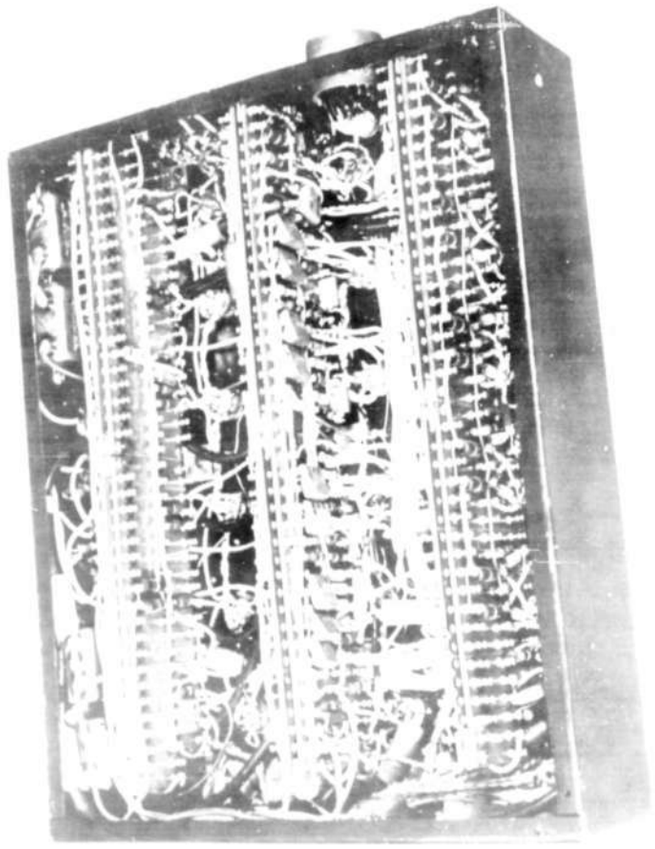
ENG. D. J. C.	APP.	A-30558

CHASSIS, BOTTOM VIEW

A-30558



MASSACHUSETTS INSTITUTE OF TECHNOLOGY
SERVOMECHANISMS LABORATORY

D. I. C. NO.	DR.	CK.
6345		
ENG. D. J. C.		

CHASSIS, BOTTOM VIEW

·30564

No special precautions were taken in wiring of the chassis. In general, all circuit components except series grid resistors and delay lines were mounted on terminal boards and leads connected from the boards to the tube sockets. The germanium crystal diodes were mounted as far as possible from power-dissipating resistors, and care was used in soldering to prevent damage to these units by overheating.

Initial Adjustment and Testing

Before the chassis is initially put into operation, there are certain adjustments that must be made. These are made by means of screwdriver controls that generally require little attention after the initial settings unless supply voltages fluctuate or tubes are changed. Simple checks, described later, may easily be made to determine if the circuits are functioning correctly.

Three d-c power supply voltages are necessary to supply the chassis,

+150 volts at 275 milliamperes

+ 50 volts at 100 milliamperes

-150 volts at 100 milliamperes

from regulated supplies. An a-c supply of 6.3 volts at about 7.2 amperes is required for the tube heaters. The power connections are made through a plug on the chassis. Other equipment desirable for initial testing should include a synchroscope, d-c voltmeter, and a pulse source. The pulse source is used to fire the pulse-forming gas tube at a continuous rate for convenience in observing steady-state circuit operation. The requirements on such a pulse source are not

very rigid, almost any shape of positive pulse that is not too long with respect to the repetition period and has a repetition frequency of less than about two thousand cycles per second is sufficient.

One of the first adjustments to be made is the GAS TUBE BIAS control. This adjustment determines the firing potential of the first gas tube and should be adjusted so that the firing point of the tube is as high as possible. One of the best methods of making the adjustment makes use of the oscilloscope by connecting it across the cathode resistor of V1 to observe any trigger produced. Start with maximum bias and repeatedly depress push-button number one. Keep decreasing the bias until the trigger is observed on the oscilloscope when the button is depressed. Repeat this operation with the nine other integer push-buttons, continuously decreasing the bias if a push-button fails to initiate a trigger. The bias is now adjusted correctly and need only be readjusted for gas-tube replacement.

The FLIP-FLOP BIAS controls the bias of the triggers applied to the flip-flops, and therefore is an indirect control on the effective trigger amplitude. It normally should be set so that the bias is -7.5 volts.

The -6 VOLT BIAS controls the bias on the delay stages and is therefore the most direct control on the trigger amplitudes. It is normally adjusted for a voltage of -6.6 volts, however, slight deviations in tube characteristics may require a slight adjustment of this voltage for best operation.

The remaining adjustments and checking are simplified by using the pulse source so that the actions of the circuits may be observed on the synchroscope. The pulse source should be connected to the grid circuit of gas tube V2 in some manner so that the gas tube is fired at a continuous rate. The exact connection depends so much upon the source impedance and the pulse amplitude, no standard may be set.

When the gas tube is firing correctly, the CLEARING PULSE AMPLITUDE control should be adjusted so that the clearing pulse rises one or two volts positive with respect to ground. If the gate-generating flip-flop, V9, is operating correctly, it should be possible to observe the sawtooth shape of the reading pulse at the suppressor terminal of any of the gate-peaker stages.

A convenient check may be made at this point to determine if the whole chassis is working correctly. Pushing any one of the integer push-buttons while the gas tube circuits are being pulsed at a continuous rate gives the same effect as pushing the button many times with the circuit working normally. This corresponds to entering a decimal number that has all digits alike. Because the last n digits of a decimal number determine the last n digits of the equivalent binary number, pushing a single integer button six times will set up a pattern on the six lights that will remain the same regardless of how any more times the same button is depressed. The same pattern is obtained if the button is pushed while the gas

tube is being fired by the pulse source. The correct patterns are as follows:

Integer	Pattern
0	000000
1	000111
2	001110
3	010101
4	011100
5	100011
6	101010
7	110001
8	111000
9	111111

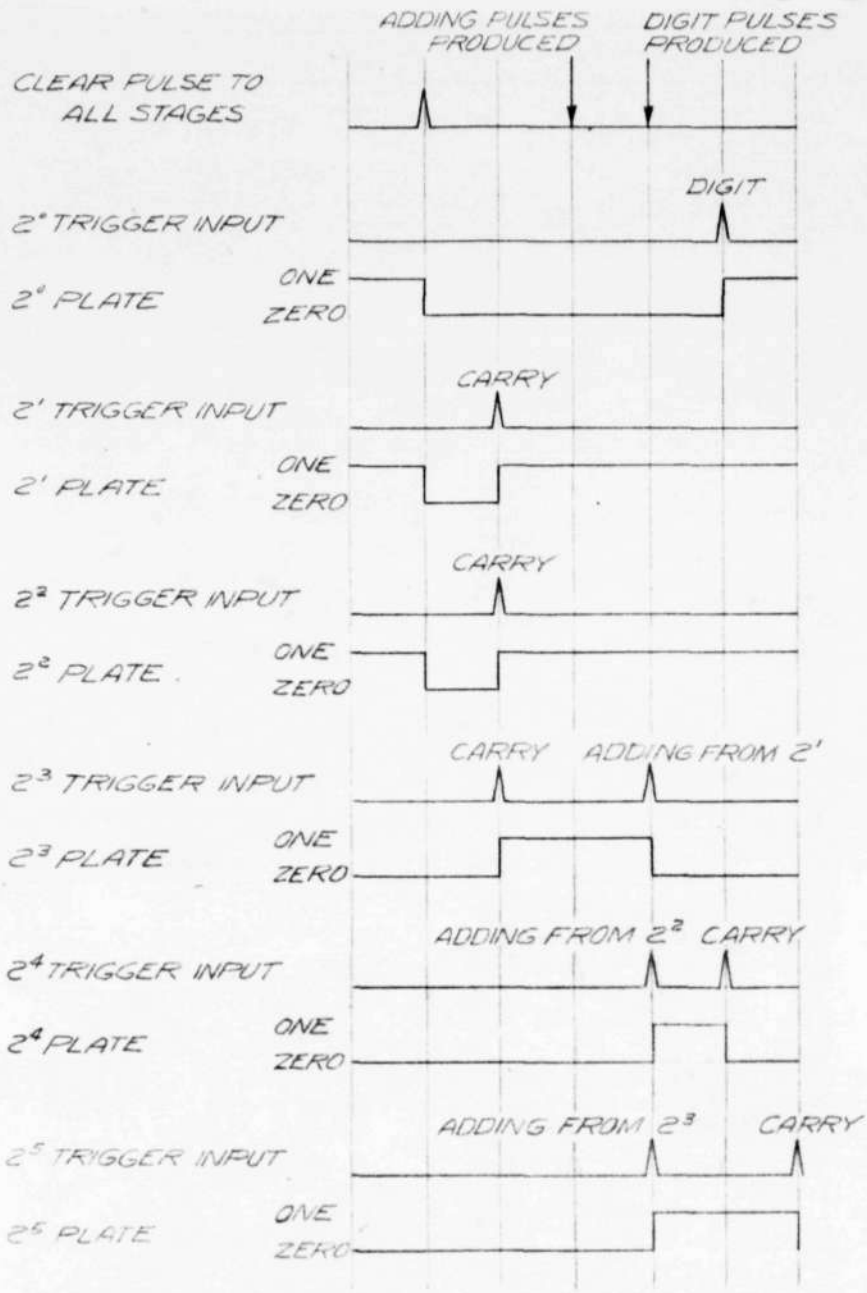
If the circuit does not produce the above patterns as the given digit button is pushed, it will be necessary to adjust the SAWTOOTH AMPLITUDE and -6 VOLT BIAS controls to get the triggers at the correct amplitude to operate the flip-flops. The SAWTOOTH AMPLITUDE control is used to adjust the adding pulses from the plate circuits of the gate-peaker stages to the same size as the carry pulses from the screen circuits of these stages. The -6 VOLT BIAS control changes the amplitude of all triggers coming from a delay stage.

If the circuits did not produce the correct patterns on the initial attempt, it is best to concentrate on one particular pattern for adjusting purposes. It is then possible to check pulse amplitudes

and flip-flop operation to determine the maladjustment. In observing flip-flop operation, it is usually best to put a small capacitor of about five micromicrofarads in series with the oscilloscope probe to prevent disturbance of the circuit operation. However, when the circuits have been correctly adjusted, a probe of twelve micromicrofarads capacitance usually produces no ill effects on the operation.

Drawing A-30584, page 59, shows the waveforms that are produced at the plates of the flip-flops and their trigger input terminals when the number one button is depressed. Unless there is a defective circuit component, an adjustment of the SAWTOOTH AMPLITUDE control to equalize the sizes of the adding and carry pulses, and the -6 VOLT BIAS control to make them the correct amplitude, will make all the flip-flops operate correctly. Similar waveforms may be figured out for the other fixed patterns, but when the adjustments have been made so that the circuit works correctly for one pattern, it usually operates satisfactorily for the others.

When the circuits appear to work correctly while being continuously pulsed, the final check is made by disconnecting the pulse source and pushing the buttons. The correct pattern should be formed after pushing a button six times and should not change by additional pushing. If this test checks correctly for all the integer push-buttons, then the entire circuit is working satisfactorily.



TEST WAVEFORMS

ALL PULSES EXCEPT CLEAR PULSE HAVE ONE TIME-UNIT DELAY BETWEEN TIME OF GENERATION AND TIME OF INTRODUCTION TO FLIP-FLOP.

CARRY, ADDING, AND DIGIT PULSES TRIGGER FLIP-FLOP IN EITHER DIRECTION. CLEAR PULSE CAN ONLY TRIGGER FLIP-FLOP FROM THE ONE TO ZERO POSITION.

CARRY PULSE PRODUCED WHEN FLIP-FLOP CHANGES FROM ONE TO ZERO.

NUMBER ONE BUTTON DEPRESSED, CIRCUIT BEING PULSED

CHAPTER VII

Summary of Results

The completed unit demonstrates that the principle of operation of this type of decimal-to-binary converter is sound. The system makes use of a ten-key type of keyboard which inherently has a higher speed of operation than the matrix-type of keyboard. The keyboard wiring is simple, making it possible to add contacts to a standard adding-machine keyboard so that the input numbers could be recorded. The length of a connecting cable is not critical, permitting the keyboard to be operated from a location separated from the conversion unit.

Although relay circuits could be designed to perform the operations required in this type of conversion system, electronic circuits possess advantages. With the particular circuits that were designed, the time of operation of the circuits is negligible when compared to the possible time of operation of the keyboard. The type of carry system that was used requires an additional unit of time for the circuit to complete its operation for each addition binary digit. With these electronic circuits, several thousand binary digits could be used before the time of circuit operation would begin to become comparable with keyboard operation time. If relays were used, a high-speed type of carry system would be necessary for the system to possess any practicability. The electronic circuits are

easily adaptable to use with an input data system that possesses a very much higher operating speed than a keyboard. In its present form, the unit requires nine tubes in the initiating and conversion circuits, and two and one-half tubes (using twin triodes) for each binary digit in the register stage. It is doubtful if relay circuits could be built to occupy less space.

It was known from the start of this project that this particular system would not handle the conversion of any numbers that had digits to the right of the decimal point. It was felt that if numbers of such a nature had to be used, they could be multiplied by appropriate powers of ten used as scale factors to shift all digits to the left of the decimal point.

Although the circuits that were designed for the unit work satisfactorily, they do not necessarily represent the ultimate in design. They do demonstrate that the detailed block diagram of the system is satisfactory. Most of the testing was done using electronically regulated power supplies as power sources. Tests using unregulated supplies were not satisfactory because the fluctuations of the particualr supply voltages used were independent of each other. It is believed that the circuits can be made to operate from unregulated supplies if changes in the a-c line voltage produce proportional changes in each of the three d-c supply voltages.

One of the chief causes of unsatisfactory operation before correct adjustment was due to the fact that the flip-flop stages are sensitive to trigger amplitude. This is not a new problem in their

design and a satisfactory solution is still being sought by several other groups working in the field of electronic computers. One solution is to use an additional stage of amplification for the triggers that would have a limiting effect and would tend to keep the trigger output a constant amplitude. Such a solution requires additional components for each stage in the register and the added complexity is not justifiable. The author believes that additional experimentation with the flip-flop parameters will provide a satisfactory solution for this particular application.

Although this thesis presents a possible solution to the problem of converting decimal numbers containing whole digits (no digits to right of decimal point) to their equivalent binary number, work still remains to design a system that will handle any kind of a decimal number. In addition, there still is the problem of designing a satisfactory system to convert binary numbers (including those with digits to the right of the binary point) into their decimal equivalents.

APPENDIX

Representation of Numbers

The decimal system utilizes ten as the number base and therefore has ten digits (0, 1, ...9). Each place in a decimal number represents a power of ten; the digit in a particular place tells how many of that particular power of ten are present. For example:

$$420.34 = 4\times10^{2} + 2\times10^{1} + 0\times10^{0} + 3\times10^{-1} + 4\times10^{-2}$$

The binary system is used in a similar manner, except two is the number base, requiring only two digits (0, 1). For example:

$$\text{Binary } 101.11 = 1\times2^{2} + 0\times2^{1} + 1\times2^{0} + 1\times2^{-1} + 1\times2^{-2}$$

Decimal to Binary Conversion

One of the most obvious methods of converting a decimal number to its binary equivalent is to extract powers of two from the number, therefore finding the binary components. For example:

Decimal number	84
extract 2^6	64
	20
extract 2^4	16
	4
extract 2^2	4
	0

Therefore, $84 = 2^6 + 2^4 + 2^2$, and the binary equivalent is 1010100.

A simpler system starts by dividing the decimal number by two and noting if there is a remainder. If a remainder is present, it indicates that there is a 2^0 component in the number (the number is odd). If such is the case, a 1 is written as the right-hand digit of the equivalent binary number. The dividend of the first operation is divided by two and the remainder of this division (0 or 1) is used as the next binary digit. This second division is the equivalent of dividing the original number by 2^2, and a remainder of 1 indicates that there is a 2^1 component in the number. By continuing the process, that is, dividing the result of each previous division by 2 and noting the remainders, the complete binary equivalent of the decimal number can be found. Here is an example of the method:

Divisions	Remainders
2) 84	0
2) 42	0
2) 21	1
2) 10	0
2) 5	1
2) 2	0
2) 1	1
0	

As before, the binary equivalent of 84 is 1010100.

Addition

The process of addition in the binary system is similar to that used in the decimal system, that is, when the sum of two digits is greater than the largest integer, a carry is added to the next column. For example:

Binary Addition Table

0 + 0 = 0	1 + 0 = 1
0 + 1 = 1	1 + 1 = 10

Sample Addition

	Decimal		Binary
Carries	11		11111 11
Addend	886	=	1101110110
Addend	743	=	1011100111
Sum	1629	=	11001011101

The same type of reasoning may be applied to the processes of multiplication and division in the binary system, in each case the actual process being a simpler operation in the binary system then the decimal system.

Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts.

SUBJECT: CONVERSION OF SHAFT POSITION TO BINARY CODE

Written by: H. P. Stabler.

Date: October 15, 1947

TABLE OF CONTENTS

ABSTRACT

This paper outlines several methods that can be used to convert shaft rotational position to binary number. Since economy of equipment requires that one conversion unit serve for several shafts, selective electronic switching is necessary. Several of the suggested components are described in some detail. A method by which shaft rotation is measured in terms of the frequency of a variable oscillator appears to be the most promising approach.

Some consideration is given also to the converse problem of converting a binary number to an electrical magnitude.

INTRODUCTION

The Whirlwind digital computer must receive input information from the rotational position of mechanical shafts. The shafts can be grouped for convenience into two types according to the degree of subdivision required of the associated information. The fine-subdivision type requires output numbers that are smooth to 1 part in 1000 to 5000, while the coarse-subdivision type requires a maximum subdivision of 1 part in 100 to 500. The fine-subdivision shafts are subject to high velocities and acceleration; the coarse-subdivision shafts are moved relatively slowly. The fine-subdivision type can tolerate some drift in zero position and calibration slope while stable calibration may be desirable for the coarse-subdivision type. This classification is somewhat artificial but is useful in any consideration of possible methods. There may be a total of some 48 different coarse-subdivision shafts and 8 fine-subdivision shafts.

The parameters associated with the shafts must be furnished to the computer in binary number form. This report is concerned chiefly with devices that can convert shaft position into binary number.

In view of the large number of shafts involved it is desirable that many shafts share the same conversion unit on the basis of sequence or other suitable controlled switching. The number of conversion units required and the maximum time that can be allotted for a conversion must be such that each parameter can be read every 1/20 second. If there is to be just one coarse-subdivision unit, the maximum time per conversion should not exceed 1 millisecond. 2.5 milliseconds has been chosen tentatively as the corresponding time for a fine-subdivision conversion. One section of this report considers the possibility of much higher conversion speeds.

The primary information sources considered include mechanical switch contacts, a variable frequency signal and d-c potentials. Problems associated with multiple-speed data are also investigated. The purpose of the report is to make a preliminary study of these different possible conversion methods. The study outlines and describes design requirements and suggests possible solutions for the associated components. Ideas that might possibly prove useful have been included even though they do not appear to be immediately applicable. The last section makes specific suggestions for the next steps in the necessary development. The output conversion problems are closely similar to the input requirements and one section of this report is concerned with the transition from binary number to electrical magnitude.

MECHANICAL COUNTER

This proposal involves the use of brush contacts or cam-operated leaf switches. It is applicable only to coarse-subdivision shafts and should not be extended to give numbers greater than 128 or 256 at the very most. The maximum speed of the controls must be small and changes infrequent.

One such arrangements is shown schematically in Figure 1. Eight binary digits (0 to 255) are provided by eight cam-operated switches. The cam discs are mounted in sets of four on two shafts. (These discs are shown above the upper carry-over pinion in Figure 1. The switches have been omitted from the drawing). The first shaft advances the switches 16 digits per revolution. The second shaft is coupled to the first by a mechanical carry-over pinion and advances 1/16th turn each revolution of the first shaft. While the second shaft is in motion it moves at the same speed as the first shaft.

The circuit schematic is shown in Figure 2. The output sides of corresponding digit switches of different parameters are connected to a common digit line which leads to a gate tube. The input sides of all digit switches for one parameter are connected together to a line from an electronic selection switch. In order to read a number, the electronic switch is set to the desired parameter, a gate pulse is applied simultaneously to all digit switches for this parameter, and a clock pulse, transmitted through the gate tubes, then reads the number into the bus.

Actually, to avoid ambiguity at the transition edges, two sets of switches are needed. In Figure 1 these are denoted Set A and Set B. Set B duplicates switches 2^1 to 2^7 inclusive of Set A; the 2^0 switch is not duplicated. All cams B are aligned with each other and displaced one digit in phase from the corresponding cams of A. All cams A 2^1 to 2^7 are aligned with each other. Cam 2^0 is displaced one-half digit from the other cams of Set A. This phasing is shown in Figure 3 (cams 2^4 to 2^7 omitted). The mechanical carry-over for B switches 2^1 to 2^7 must also be displaced 1 digit in phase. The schematic for the connections for each parameter is shown in Figure 4. In this way, the numbers advance only at the transitions of the 2^0 switch.

No readings are possible during the fly-over time of switch 2^0. If the total fly-over time represents any significant fraction of the total operation time, this switch should be a flip-flop controlled by a brush contact, or else other methods should be used.

The method has the advantages of permanency of calibration, linearity, ease of testing and, possibly most important of all, potentially high reading speed. The unit probably could be designed quite compactly, particularly if brush contacts were used. The disadvantages consist of the limitations already mentioned, and present uncertainty with respect to switch life and reliability.

VARIABLE-FREQUENCY METHODS

Here shaft position controls the frequency of a variable-frequency oscillator. The conversion unit consists of switching arrangements, a fixed crystal oscillator, pulse-forming circuits, and two counters. One counter receives variable-frequency pulses corresponding to a particular shaft position; the other counter receives the fixed-frequency crystal oscillator pulses. The parameter is read into the computer bus from one of the counters.

There are four different arrangements for obtaining the number. These will be called A, B, C, and D. Methods A and B time a fixed number of variable-frequency pulses, the parameter being read from the clock pulse counter. Methods C and D count the number of variable-frequency pulses in a fixed time interval, the parameter then being read from the variable-frequency counter. In methods A and D the parameter number decreases with increasing numbers of counts. In methods B and C the parameter number increases with increasing numbers of counts. These four arrangements have different linearity, stability, and time characteristics. Methods A and B require a clock pulse rate which is higher in frequency than the variable frequency, while with methods C and D, the variable frequency is higher. The relations between the several variables involved are derived in the following section.

1. Fundamental relations

Method A

Let r = number of variable pulse intervals being timed - a constant.

f = variable pulse frequency.

f_c = clock pulse frequency.

n = total number of clock pulses counted.

n_o = maximum number of clock pulses counted.

N = parameter number.

τ = time required for the count - a variable.

Then $N = n_o - n$ n_o a constant, and $\tau = \frac{r}{f} = \frac{n}{f_c}$

Let k = tuning range factor, i.e., $f_{max} = kf_{min}$. Suppose also

that r variable cycles can be timed to a precision of $\frac{\epsilon}{f}$ where ϵ is a fraction of a variable cycle. If the maximum uncertainty in timing is to be no greater than 1/2 a clock pulse interval (i.e. 1/2 digit) then

$$\frac{\epsilon}{f_{min}} = \frac{1}{2f_c} \qquad \text{or}$$

$$f_{min} = 2\epsilon f_c \qquad \text{Also} \quad r = \tau_{max} f_{min}$$

But
$$N_{max} = \frac{rf_c}{f_{min}} - \frac{rf_c}{f_{max}} = \frac{rf_c}{f_{min}}\left(1 - \frac{1}{k}\right)$$

$$= \tau_{max} f_c \left(1 - \frac{1}{k}\right)$$

The results listed in colum A of Table 1 follow directly from these relations.

Method B

In this case n_o = the minimum number of clock pulses counted, all the other difinitions being the same, and

$$N = n - r_o = n_o\left(\frac{f_{max}}{f} - 1\right)$$

The results are similar (or identical) to the previous case and are listed in column B of Table 1.

Method C

For this case let

r = the number of clock pulses used for timing - a constant.

n = number of variable pulses counted

n_o = minimum number of variable pulses counted.

$n = n - n_o$ = parameter number

τ = time of counting, constant.

Suppose as before that r clock cycles can be timed to a precision of $\frac{\epsilon}{f_c}$ where ϵ is a fraction of a clock pulse cycle. If the maximum uncertainty introduced by the timing is 1/2 digit, then

$$\frac{\epsilon}{f_c} = \frac{1}{2f_{max}}$$

or $f_c = 2 f_{max}$ also $r = \tau f_c$

and $N_{max} = \tau f_{max} (1 - \frac{1}{k})$

These relations lead to the values listed in column C of Table 1.

Method D

Here n_o = the maximum number of variable pulses counted and $N = n_o - n = n_o(1 - \frac{f}{f_{max}})$.

The results are listed in column D.

Reasonable values for K and ϵ appear to be k = 2, ϵ = 1/10 (36 degree

Comparison of methods

Which of the four methods is preferable depends to some extent on the stability characteristics of the oscillators. Assuming that all the oscillators associated with a single conversion unit are identical and that uncertainty in frequency is due to a fixed uncertainty dC in capacity, Method A is best. For N = 0, dC causes $\frac{1}{k^2}$ times the percentage uncertainty in frequency that the same dC causes at $N = N_{max}$. Thus referring to table 1, column A, $(dN)_{N = 0} = \frac{1}{k} (dN)_{N = N_{max}}$, a reasonable result. Each of the other methods is less favorable, D being worst.

On the other hand, if $\frac{df}{f}$ is constant over the tuning range, methods B and C are preferable to A. B has the advantage (over C) of having lower variable frequencies, for which $\frac{df}{f}$ may be expected to have lower constant values. Actually, however, $\frac{df}{f}$ is not likely to be strictly constant over the tuning range, and Method C has the advantage that f_{min} is associated with N = 0 where the uncertainty dN should be small.

If a single conversion unit has associated with it a few parameters requiring large N_{max} and many parameters requiring appreciably smaller N_{max}, Method C has some advantages. Thud dC may be approximately constant for any one oscillator but the dC for the small N_{max} oscillators may be larger than for the large N_{max} oscillators.

Stability tests of actual oscillators can best decide the choice. From the point of view of the pulse-forming circuits, it appears advantageous to have the variable pulse rate lower than the constant clock pulse rate. There is little to choose between the four methods with respect to the counting and reading problems, or linearity.

Oneconsideration can be mentioned which places an apparent restriction on the minimum size of f_{min}. If a control is changed very rapidly, undesirable transients may be set up. Suppose a shaft is turned through the whole tuning range in time t. Assuming that the rate of change of frequency is constant, it is readily shown that the maximum fractional change in frequency in the time of one cycle is $\frac{(k-1)}{f_{min}\, t}$. To avoid transients this quantity should be much smaller than $\frac{1}{Q}$ of the oscillator. If t is of the order of 1/5 sec and f_{min} is in kilocycles this requirement is well fulfilled.

2. Numerical examples

Fine subdivision. Method A.

Suppose

$N_{max} = 5000$ $k = 2$

$\tau_{max} = 2000$ sec $\epsilon = 0.1$

Then

f_c = 5 MC pulse rate

f_{min} = 1 MC pulse rate

f_{max} = 2 MC

$r = 2000$

τ_{min} = 1000 μsec.

For $N = 0$ and $dN = 1/2$

Allowable drift = 50 cycles

Allowable fractional drift = $\frac{1}{20000}$

For $N = 5000$ and $dN = 1$

Allowable drift = 400 cycles

Allowable fractional drift = $\frac{1}{5000}$

In order that the timing process shall not introduce an uncertainty greater than 1/2 digit, counting gates accurate to 1/10 μsec are required. The clock counter must operate with an input pulse rate of 5 MC. The uncertainty of end-carry delay of the variable pulse counter must be less than 1/10 μsec. The line between the control oscillators and the converter must carry sinusoidal frequencies between 1 and 2 MC.

Coarse subdivision Method A

Take

$N_{max} = 400$ $k = 2$

$\tau_{max} = 400\ \mu sec.$ $\epsilon = 0.1$

Then

f_c = 2 MC pulse rate

f_{min} = 400 KC

f_{max} = 800 KC

$r = 160$

$\tau_{min} = 200\ \mu sec.$

For N = 0 and dN = 1/2

Allowable drift = 250 cycles

Allowable fractional drift = $\frac{1}{1600}$

For N = 400 and dN = 1

Allowable drift = = 2000 cycles

Allowable fractional drift = $\frac{1}{400}$

The timing process should not introduce uncertainties greater than 1/4 μsec.

Very coarse subdivision High Speed - Method A

Suppose

$N_{max} = 64$ $k = 2$

$\tau_{max} = 26\ \mu sec$ $\epsilon = 0.1$

Then

$f_c = 5$ MC

$f_{min} = 1$ MC

$f_{max} = 2$ MC

$r = 26$

τ_{min} = 13 μsec

For N = 0 dN = 1/2

Allowable drift = 3.9 KC

Allowable fractional drift = $\frac{1}{256}$

For N = 45 dN = 1/2

Allowable drift = 15.6 KC

Allowable fractional drift = $\frac{1}{128}$

Timing must be accurate to 1/10 μsec.

Maximum over-all time $\sim$ 30 μsecs.

Very coarse subdivision Small tuning range. Method A

Suppose

N_{max} = 64 k = 1.4

τ = 45 μsec ϵ = 0.1

Then

f_c = 5 MC

f_{min} = 1 MC

f_{max} = 1.4 MC

r = 45

For N = 0 dN = 1/2

Allowable drift = 2.2 KC

Allowable fractional drift = $\frac{1}{450}$

For N = 32 dN = 1/2

Allowable drift = 4.4 KC

Allowable fractional drift = $\frac{1}{320}$

The two very-coarse-subdivision examples are useful in considering the possibilities of multiple-speed data discussed in another section.

τ_{min} = 13 μsec

For N = 0 dN = 1/2

Allowable drift = 3.9 KC

Allowable fractional drift = $\frac{1}{256}$

For N = 45 dN = 1/2

Allowable drift = 15.6 KC

Allowable fractional drift = $\frac{1}{128}$

Timing must be accurate to 1/10 μsec.

Maximum over-all time $\sim$ 30 μsecs.

Very coarse subdivision Small tuning range. Method A

Suppose

N_{max} = 64 k = 1.4

τ = 45 μsec ϵ = 0.1

Then

f_c = 5 MC

f_{min} = 1 MC

f_{max} = 1.4 MC

r = 45

For N = 0 dN = 1/2

Allowable drift = 2.2 KC

Allowable fractional drift = $\frac{1}{450}$

For N = 32 dN = 1/2

Allowable drift = 4.4 KC

Allowable fractional drift = $\frac{1}{320}$

The two very-coarse-subdivision examples are useful in considering the possibilities of multiple-speed data discussed in another section.

The odd values for r in these examples represent only typical minimums. Larger r values require higher values for either f_{min} and f_c or for τ_{max}.

3. Block diagrams

Figure 5 shows a block diagram of a complete fine-subdivision unit assuming the constants of the first example and with switching provided for 8 separate inputs.

Assume that initially FF1, FF2, FF3 are all at zero, so that GT2 is open but GT1, GT3, and GT4 are closed. Counter No. 2 reads 96, the reset value, and Counter No. 2 has accumulated a value for N. A read-out pulse is received. This triggers FF No. 1, opening GT1. The next clock pulse passes through GT1 and GT2, resets FF1, and reads N into the bus. After delay through DE3, counter No. 2 is reset by the same pulse.

Receipt of N is followed by an order setting the selection switch to the next parameter to be read. The read-in pulse from the bus sets FF2. The next variable pulse resets FF2, setting FF3 and opening both GT3 and GT4. Thus timing always starts at a definite (and very small) time after a variable pulse. FF3 is reset, stopping the count, by the fast end-carry pulse from Counter 1.

GT2 and DE2 insure that Counter 2 is not read until GT4 is closed and complete carry-over has taken place. If the scheduling of read-out pulses is such that ample time is always allowed for the count, FF1 and GT1 and GT2 can be omitted or arranged instead to operate the alarm in case of incorrect timing.

DE5 must be sufficiently long to allow for switching transients.

Change of pulse rate may cause a change in d-c restoring levels in the variable-frequency pulse shaping circuits, and a consequent slight change in phase of the pulse with respect to the pulse cycle. Investigation should be made to see whether this phase change is appreciable and how rapidly it becomes stabilized. If the required DES is long, it may be preferable to order the next selection switch setting before reading out the accumulated N.

Figure 6 is a block diagram of the fixed-frequency counter 2. Unless the program scheduling requires great economy of time, high-speed carry-over is not necessary. The output gates are arranged to read the complement number into the bus and switches are provided by which the initial reset reading can be chosen.

Although counter 2 may receive as many as 10,000 pulses during a measuring period (where N = 0), only 13 rather than 14 stages are required. If the time required for end-carry through counter 1 is 2/5 μsec (including any difference between the setting and resetting times of FF3 and the associated gates), the correct initial reading for counter 2 is the binary equivalent of 6381. If N is 1000 the counter receives 9002 pulses increment and thus reads 6381 plus 9002 less 8192 not indicated, or 7191. The 9's complement of this number is 1000, which is read into the bus. The 8192 not indicated does not lead to ambiguity because the minimum reading at the end of an accumulation is 6381 + 5000(N_{max}) + 2 = 11383, and is thus always over 8192.

Figure 7 is a corresponding diagram for counter 3. High-speed end-carry is essential. Switches which control the reset value are convenient in an experimental model but could be omitted from the final design.

The block diagrams for a coarse-subdivision unit would differ from Figs. 1, 2, and 3 only in the number of inputs to be switched and in the numbers of stages of the counters.

4. Oscillator

Clearly the success of the method depends primarily on the design of the oscillator. The allowable drift requirements of the fine-subdivision example given in section 2 are very difficult to meet over long periods of time. However, the fine-subdivision control will have the necessary smoothness provided the instantaneous rate of change of N due to random frequency shifts does not exceed 1/2 digit per 1/20th-second reading interval, or 2 digits per second averaged over a second. The stability of calibration probably would be satisfactory with a steady drift rate of 25 digits per hour (at all positions of the control) provided this is periodic with time of day or temperature. The oscillator of any good communications receiver or signal generator meets these relaxed requirements provided that there are no sudden changes of supply voltages and provided that it is not subjected to mechanical vibration.

Figure 8a shows the schematic of a simple type of oscillator with the requisite short-time stability. This is a modification of a circuit by K. A. Pullen[1]. The modification consists of increasing the cathode resistor from 600 ohms to 6K and in operating the grids at a d-c potential of about 22 volts rather than at ground. This change results in strictly class-A operation and a high impedance across the tuned circuit. The static characteristic giving the relation between e_1 and e_o (see Figure 8b) is shown in Figure 9 for two different plate supply potentials. The characteristic is suitably bent to produce amplitude stability without drawing current from either grid. The very slight change resulting from a 30% increase in plate voltage is also notable.

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1. K. A. Pullen - The Cathode-Coupled Amplifier, I.R.E. 34, P. 402, 1946. This reference was called to my attention by Mr. D. J. Crawford

Changes of pitch of the order of 100 cycles or more are produced by shunting capacitances across the 92-ohm termination, although no quantitative measurements have been made. The mechanical rigidity of the chassis was not sufficient to permit a good test of the effect of changing tubes. Change of a few kilocycles/sec (10 to 20 digits) seems likely.

The following modifications are desirable: A coil having an appreciably higher Q should be used. Possibly the fixed wiring losses are such that a somewhat higher L would give a better compromise between high over-all Q and high C. A temperature-compensated LC is desirable. Coil manufacturers should be consulted for suggestions. The biasing arrangement shown in Figure 6 is poor because the filter condenser C3 becomes part of the oscillating circuit. The best Q is obtained if the low side of the tuning condenser is placed at the DC bias potential by connecting it directly to the low side of L. If this is mechanically inconvenient, another possibility is to place both L and C1 at DC ground potential and connect their high sides to the grid through a blocking condenser. The DC bias would then be supplied to the grid through a one-megohm resistor.

An approximate analytical investigation could be made of the phase shift of the feedback voltage. It may prove preferable to provide feedback through a 100-$\mu\mu$f blocking condenser and a resistor connected either to the plate of V1B or to some point nearer B+.

An inherently poor feature of the design is that it places the cathodes at relatively high RF and DC potentials. As a result the heaters may cause some 60-cycle frequency modulation. Although the audible heterodyne notes which were observed were very clear, this is not a very adequate test. A test for 60-cycle modulation could be made easily, when a complete counting system is assembled, by starting the timing interval at different points of the 60-cycle period. Changes of the heater by-pass condensers produce changes of frequency.

A suitable transformer should be used to drive the output line rather than a cathode follower. The transformer must not discriminate between 1 MC and 2 MC, but it need not reproduce a sinusoidal waveform, and some peaking is tolerable.

By far the greatest difficulty is likely to be experienced with the mechanical design of the tuning arrangements and chassis. In order to have frequency smoothness, great rigidity, excellent bearings, and freedom from vibration are necessary. General Radio or Cardwell might be consulted to advantage.

The oscillator requirements for the coarse subdivision units are much less stringent. Possibly an output transformer can be used as part of the plate load and an output tube avoided. An electron coupled miniature pentode oscillator with a compact LC is another design possibility. A Wien bridge oscillator (if the frequency is sufficiently low) would have the advantage of giving a linear $\frac{1}{f}$ with a linear-C variable condenser. This results in a linear N (Method A or B). Even with the coarse-subdivision requirements, some noticable drift and change of calibration with tubes is likely - particularly if the unit is reduced in size and pompromises are made in its design.

5. Switching

Figure 11 shows a gating method for 8 inputs. This circuit has not been tested (even statically), and the constants are tentative. Each 6AS6 is intended to receive signals of .5 to 1.5 volts RMS. The gate selection square wave drives the suppressor to zero bias. It must have a duration of about 2.5 millisec. The screen-dropping resistor is introduced to limit the screen dissipation when the tube is cut off. The screen potential has a time

constant of about 1 sec. (during its rise).

There are many other gating methods possible which are more expensive with respect to power or tubes.

If there are as many as 48 inputs to be selected, these can be grouped in 6 sets of eight. Each set of eight has a common plate resistor and drives a second mixer tube. The six second-mixer tubes in turn have a common plate resistor.

The pulse shaping circuits present no unusual problem except that they must be preceded by one or two stages of video amplification.

Circuits have already been designed for crystal-controlled pulse generators.

D-C POTENTIAL-DIVIDER METHOD

The simplicity and linearity of potentiometers make them attractive as control elements. These features may be particularly important for some of the coarse-subdivision parameters.

A d-c voltage can be converted to a time interval. If a counter receives pulses at a constant rate during the interval, an appropriate binary number is produced. A block diagram with suggested constants is shown in Figure 12.

D-C Source and Switching

Figure 13 shows arrangements at the control station and Figure 14 the associated selection method. All cathode follower grids except the selected one are kept below ground potential by the clamping triodes. The input line to the conversion unit has a maximum time constant of 7 μsec. After 50 μsec the output voltage across the common cathode resistor will be within 0.1% of its final value.

Figure 15 gives measured departures from linearity between divisions of a control potentiometer and the output cathode voltage. The potentiometer was a finely divided Leeds and Northrup 22K slide wire. The departures indicated are comparable to the uncertainty in the readings. Variations of 10 volts in the zero reading and 1 or 2% in slope may be expected for different tubes. With regulated heater voltage, longe-time stability and over-all linearity within ± 1/2% seems feasible. With a smaller number of inputs, a higher cathode resistor and a lower transconductance tube can be used.

Higher-speed switch arrangements are shown in Figures 16A and B. They are naturally more expensive of power, and the extra cathode follower of Figure 16B introduces additional uncertainty.

Application of negative feedback could be applied more readily to the selection switching if an a-c carrier were employed. However, unless the feedback can be returned to the voltage divider itself, the loss uncertainties in the line (at the necessary high frequency) would result in decreased over-all precision.

Timing Circuits

The delay multivibrator can be a low-precision self-restoring type. Since the read-in pulse to the selection switch may be too short to produce proper triggering, TT1 may be necessary. This is conveniently a 6AC7 with its plate connected to the normally high plate of the multivibrator.

Figures 17 and 18 show circuits for the sweep generator and amplitude comparator. Except for the slight modification of two time constants, these circuits are the same as those given by Chance*. It may be necessary to take

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* B. Chance. Rev. Sci. Inst. 17, p. 400 and p. 403, 1946. See also Radiation Laboratory Series Vol. 19, Chaps. 5, 7, 13; Vol. 20, Chap. 5

the sweep output from the cathode of V2B rather than from the grid in order to have sufficiently low impedance to drive the pick-off circuit. In this case, some tailoring of the linearity provision will be necessary. Linearity of about 1/10% is possible. The stability should be satisfactory if the pick-off diode is operated with a regulated heater supply.

The counter must be reset to a value below zero determined by the time required for the sweep to reach the zero-point voltage.

Several other timing circuits are possible alternatives. (See the references cited above). In particular, a phantastron might be more economical of tubes and possibly more accurate. Its delay value is not quite as conveniently controlled, since a current rather than a voltage is required.

MULTIPLE-SPEED DATA

Fairly precise information can be obtained by properly combining two or three sets of relatively coarse weighted data. For example, if a unit dial gives a number accurate to 1 part in 32 and a sixteens dial (driven at 1/16 the speed) gives a number to the same accuracy, the combined information is accurate to 1 part in 512. The reading device must have proper rules for interpreting the data. Two such processes are discussed here.

"Saw-tooth" data

Suppose that each dial has a strict linear saw-tooth output of information which after appropriate conversion appears as counter readings. For illustration, consider first a decimal system. The units readings progress uniformly 0, 1....9, 0, 1....9 with continuous rotation of the control. The tens readings are given to tenths of a tens digit, although they are not necessarily correct to better than $\pm$ 4/10th of a tens digit. The fractions are for correct rounding off only. The tens information is staggered 5 units (.5 tens) with respect to the units information.

With the control at zero position the units dial reads 0, the tens dial -0.5 ($\pm$ 0.4). When the control is advanced a true increment of 27 units the units dial reads 7, the tens dial 2.2 ($\pm$ .4). Suppose the apparent tens reading is 1.9. To obtain the correct tens digit the rule is: add to the tens dial a number of tenths equal to the tens complement of the unit reading and then discard the fraction. Thus $1.9 + (10 - 7) \times 0.1$ gives 2 for the correct tens reading or 27 for the answer. On the other hand, if the apparent tens reading is 2.3 then $2.6 + (10 - 7) \times 0.1$ still gives 2 or 27 for the answer.

This procedure is easily carried out with binary counters. As one possibility, consider the following speed allocations.

Control Knob	64 digits per revolution (8 rev. for 512 total)	1x
Units dial information	32 digits per revolution	2x
Sixteens dial information	512 digits per 288° of revolution or 1/10x	

The ratio of the units and sixteens speeds is 20 rather than 16 because the sixteens information does not extend over a complete revolution.

Figure 19 shows the counter arrangements in the conversion unit. The sixteens counter contains 7 stages so that it registers sixteens and eighths of a sixteens digit. Consequently the sixteens information must be correct to $\pm$ 3/8ths of a sixteen digit; that is, the information conversion error must never be greater than 1 part in 43 of the full scale value. The sequence of operations is as follows:

1. Read into both counters simultaneously through GT1 and GT2, which are controlled by the associated information.
2. Read into the units register from the units counter.
3. A round-off pulse sets FF3 and opens GT3. Clock pulses are added simultaneously to the units counter and to the sixteens counter, the latter pulses being reduced by a factor of 4 by FF10 and FF11.
4. FF3 is reset and GT3 closed by the end carry from the units counter.
5. A read-out pulse reads the positions of FF00 through FF08 into the bus.
6. The counters and registers are cleared.

"Hill-and-dale" data

Here, the units data uniformly increase with rotation and then uniformly decrease at the same rate. Two sets of such units data, displaced in phase, are necessary. This is illustrated in Figure 20 for a 32 scale. The two sets of units data are denoted A and B. 360 degrees of rotation correspond to one complete up-and-down cycle, and A and B are displaced 90° in phase. The sixteens data are given by C. The value of N represented by the ABC data is given in the figure below C. The zeros of A occur for N = -17, 47, 111.... The zeros of B occur for N = -1, 63, 127...., the zero of C for N = 7. The rules for computing N from the ABC data are also given in the figure. Notice that, as before, the C reading (the sixteens digit) can be in error by as much as $\pm$ 7/16 of a sixteen digit without changing the computed answer. Actually the A and B lines may be rounded or interrupted at the top and bottom of their cycle so that the allowable C error may be somewhat less than $\pm$ 7/16 of a sixteen digit.

The computed N is easy to obtain from binary counters. Three counters are used. (Two or one can actually be used provided time is not a consideration). The A and B counters are always reset to -1 (11111). The three sets of data are converted simultaneously; the A counter reads (A-1), the B counter reads (B-1), the C counter reads C. Gates associated with the first two stages of the C counter determine how the final reading is to be obtained. For example, if C = 3 the bus receives the A counter reading and

the C reading. If C = 4 the B counter reading is substituted for the A reading. If C = 1, a single pulse is added to the A counter; the bus then receives the C reading and the 9's complement of the A counter reading. Similarly for C = 2, a pulse is first added to the B counter, and the B complement is then read out to the bus. By this choice of phasing for the original data no carry-over between A (or B) and C is needed.

Appropriate Sources

Unfortunately, 360° saw-tooth data are difficult to generate with mechanical motion, particularly if reversibility is necessary. Ideally, the discontinuity should require infinitessimal motion, or negligible time for the transitions. Four potentiometer arrangements meet this requirement with varying success.

1. Two ordinary potentiometers (for example GR 214A 10K) can be fitted with bridges for 360° rotation, mounted back to back, and staggered in phase by about 70°, so that one contact arm or the other is always on a winding. This is represented schematically in Figure 21A. Small resistors V and W keep the two contact arms at the same potential while they are simultaneously on their respective windings, except during a 10° over-lap section where the Y contact is at the high and the X contact at the low end. S1 is closed except at and near this high-low over-lap. S2 flips over in the middle of the high-low over-lap to create the saw-tooth discontinuity. S1 and S2 are cam-operated micro switches. This arrangement is easiest to set up with standard equipment. Faulty results are obtained if the control is read during the flip-over time of S2. This time is of the order of 6 milli-seconds, and if the control has very adequate subdivision (1 part in 500) for the parameter represented, this may be unimportant

2. Higher transition speed is obtained with the arrangement of Figure 21B. The potentiometer windings are arranged to have only about 3 degrees of high-low overlap. S1 is a sliding contact driven by the potentiometer shaft and is closed except for 5 degrees including the high-low overlap. In this case the discontinuity (during decay) has the time constant of the line through about 12K or perhaps 6 μsec. Slightly over 1 time constant will take the voltage below the zero point, say 30 volts. The rise time is much more rapid. This method broadens the zero position of the potentiometer to some 5 degrees, which is not serious for 1-in-32 units date.

3. A special potentiometer can be constructed with a very small gap between the high and low ends. The contact arm shorts the high and low ends during transition, and a switch similar to S1 opens the supply voltage at and near the cross-over. This has the advantage of requirin just one potentiometer for the unit data. The transition times are similiar to those of arrangement 2.

4. A special step attenuator can be constructed with perhaps 64 steps. This is shown in Figure 21C (with 8 steps). The contact arm must short adjacent contacts during a transition.

Hill-and-dale data can be obtained from a continuously wound

potentiometer tapped just 180° apart. It can also be obtained from a Helipot with high and low taps placed alternately and uniformly along the winding.

A rotating condenser with symmetrical plates provides hill-and-dale data which can be used for frequency control. The requisite linearity for 32 subdivisions should be possible, particularly if the tuning range is small.

Application to Fine-Subdivision Information

If difficulty is experienced with the stability of the fine-subdivision oscillator when its turning condenser is subject to mechanical vibration, some consideration may be given to the value of multiple-speed data, particularly if applied to just a few of the shafts. Unfortunately there is not much advantage to be gained unless the data of each of the two speeds are given to about the same precision. (For example 128 "units" given to a precision of 1 part in 128 and 64 "tens" given to a precision of ± 0.4 of a "tens" digit). This leads to unfavorable speed ratios unless a servo is available to drive the units shaft. There might be some value in using a condenser with a many-vaned rotor and correspondingly divided stator. This is likely to lead to a low tuning ratio if the required linearity (for the tens) is maintained. Another possibility is to use 3 shafts at 3 different speeds, with precision, say, of 1 in 32 for each. This would require $N_{max} = 64$. The last two numerical frequency examples (see page 7, 10), with $k = 2$ or 1.4, are applicable here. A single parameter in this way requires 5 separate oscillators and a corresponding number of switching arrangements, a high price to pay for a possible gain in smoothness and speed. While potentiometers are simpler than oscillators, they cannot be driven at high velocity by a servo-motor.

HIGH-SPEED POSSIBILITIES

It would be convenient to have the conversion time from electrical magnitude to binary number so short that the computer, after requesting a particular reading, could wait for the answer before continuing other operations. Unfortunately the required time appears to be prohibitively long unless a separate counter is associated continuously with each shaft.

The mechanical counter described at the beginning of this report has adequate speed provided low-impedance video cable is used for all the multiple-gate leads. A single flip-flop and two associated gate tubes could replace the mechanical two-way switch shown in Fig. 4.

The direction-sensitive pulse generator and reversible counter described in RLE Report No. 3 could be applied to either fine or coarse-subdivision shafts. The reversible counter circuit should be modified by applying the high-speed carry method to progression in either direction. Engraved lines, 200 to the inch, on a light aluminum disc could serve as the primary information source. This method is too expensive to apply except under unusual circumstances, but it has the requisite speed for immediate reading.

The variable-frequency method and the d-c sweep method both involve the accumulation of N by counters receiving successive unit increments. If the maximum reliable counting rate is 5 MC/sec (possibly this is too conservative),

the time for a reading can never be less than $\frac{N_{max}}{5\ MC/sec}$. If N_{max} is large, the time can be reduced by multiple-speed data. With the number of counts as small as 32 (as in the hill-and-dale d-c method) and the switching time (at considerable expense) reduced to 2 μsec, some 10 μsec would still be required for an answer. (The interval between readings also must be sufficient to allow the sweep circuits to recover).

D-C Step-Comparison Method

An alternative d-c conversion scheme may become more attractive as development proceeds. This is shown in Figure 22. It makes use of the circuits used to generate a d-c deflection voltage for the storage tubes*. At present, the maximum degree of subdivision for these voltages is 1 part in 32. This unit is called the d-c generator in the figure. Its output voltage depends on the readings of the 5 flip-flops. Assume that a parameter reference voltage has been selected and made available to the amplitude comparator. With all the flip-flops off, the pulse distributor opens GT04 and GT14 and sends an add pulse to FF04. The d-c generator sets up a voltage of 16 units (in less than 2 μsec). If 16 units exceeds the parameter voltage by as much as 1/2 unit, a pulse appears from the comparator which resets FF04, returning the d-c generator to zero. If 16 is less than the parameter voltage, FF04 remains set. The pulse distributor next opens GT03 and GT13 and sets FF03. The generator sets up 8 units (or 24 if FF04 is still on), and the amplitude comparator responds with a subtract pulse if this trial value is again too large. This process is repeated until all 5 flip-flops have been explored. The final binary number appears on the flip-flops and may be read out to the bus through gate tubes not shown. The amplitude comparator can be of the same type as that given in Figure 22 provided its recovery time is made sufficiently short. A high-voltage crystal should replace the 6H6 comparison diode.

The time required for a step comparison of this type is likely to be about 2 μsec per binary stage, or 10 μsec for subdivision to 1 in 32. This time is comparable to the d-c sweep method. If the d-c generator can be extended to give finer subdivisions, step comparison becomes increasingly advantageous. The comparator probably can be made to operate reliably with a discrimination of 1/2 volt; thus the upper limit for subdivisions cannot be made very large, even if otherwise possible.

OUTPUT DEVICES

This section considers, quite briefly, some of the related output problems.

The output of the computer must control the readings of many meters and several servos. Most of the meters provide readings to an accuracy of 1% or less, and presumably can be actuated by d-c voltages. Data switching is again desirable.

*John O. Ely. Engineering Notes No. E-31

Both the d-c sweep method and the d-c step-comparison method are quasi-reversible, while the variable-frequency method apparently cannot be directly applied to the output problem. Figure 23 indicates how a d-c sweep method can be used to convert a binary number to a d-c voltage. This should be compared with Figure 12. The circuit operates as follows.

1. Assume all output switches are open, the counter cleared.
2. Set the selection switch.
3. Read the binary number into the counter register.
4. The read-in pulse after DE1 closes the selected normally open output switch by means of its associated flip-flop.
5. C1 now can discharge through the low impedance of the sweep amplifier. C2 does not follow the discharge of C1 very rapidly because of R. C1 is considerably larger than C2.
6. After DE2, FF1 is set. This starts the sweep, and simultaneously the counter receives clock pulses. C1 rises in potential with the sweep.
7. The fast end-carry from the counter first opens the output switch, isolating C1, and then stops the saw-tooth sweep.
8. C2 charges from C1, and the vacuum-tube voltmeter reads the output voltage until the next time information is available.

Two changes would be desirable. The sweep properly should be interrupted, and the maximum voltage held on the sweep condenser (rather than being discharged) while the output switch is still open, in order to allow C1 to reach equilibrium. Probably a way can be found to do this which still does not interfere with the strict linearity of the sweep. Properly R should be replaced by a normally closed switch that is opened during the rise of the sweep and then closed again at the top. This adds considerable expense, however, and suitable compromises of time constant may be possible. Some manner of retaining the intermittent information other than on condensers would certainly be desirable.

Figure 24 gives an output switch suggestion. This has a long closing time but a short opening time. Figure 25 shows an almost conventional sweep amplifier. The cathode follower supply for the screen of V1 may not be warranted, in view of other uncertainties in the method.

With careful development, this method probably can give accuracies of the order of 1%. The time required for the conversion is comparable to that required for the input conversion. A step d-c generator like those used for the deflection circuits of the storage tubes is to be preferred to a sweep, provided the necessary subdivision is possible.

For readings that must be given to an accuracy of better than 1%, multiple weighted data should be used. The problem then becomes one of designing meters and servos which operate with multiple data and which properly interpret the weighting.

In some cases the expense of a separate binary register which is always associated with a particular servo-driven output shaft may be warranted. The servo must be able to interpret the counter as well as to make changes in the reading as the error is reduced. The methods described in RLE Report No. 3 are

expensive, but are applicable to such a problem.

DEVELOPMENT SUGGESTIONS

The variable-frequency method appears to be the most promising as an input device. Development should start with the design and testing of a fine-subdivision oscillator and also a coarse-subdivision oscillator, with some attempt to simulate actual cockpit mechanical requirements. Construction of a fairly complete fine-subdivision unit is warranted unless meanwhile a still more promising approach is formulated.

If manpower is available, the system of Figure 12 would be interesting to study since a Helipot is to be preferred to an oscillator if it can serve adequately Some preliminary experimental work could be done on potentiometer sources for multiple data.

If the programming of the computer would be significantly easier with conversion times of 8 μ sec or under for most of the coarse-subdivision information, then some investigation of switch contacts and cabling might be undertaken in connection with the mechanical counter proposal.

RPS/og H. P. Stabler

LIST OF DRAWINGS

FIGURE NO.	TITLE	DRAWING NO.
1	Mechanical Counter	A-31030
2	Block Diagram Mechanical Counter	A-31031
3	Cam Phasing	A-31032
4	Double Switch Connections	A-31033
5	Block Diagram. Variable Frequency Conversion Unit.	B-31034
6	Fixed Frequency Pulse Counter	A-31035
7	Variable Frequency Pulse Counter	A-31036
8	Cathode Coupled Oscillator	A-31037
9	Cathode Coupled Static Characteristics	A-31038
10	Oscillator Unit	A-31039
11	Input Selection Circuit Frequency Method	A-31040
12	Block-Diagram - DC Potential Divider Method	B-31041
13	Control Potentiometer	A-31042
14	Input Selectron Circuit - DC Method	A-31043
15	Cathode Follower Linearity	A-31044
16	Higher Speed Selectron Circuits	A-31045
17	Sweep Generator	A-31046
18	Amplitude Comparator and Pulse Amplifier	A-31047
19	Counters for Multiple Speed Data	A-31048
20	"Hill and Dale" Data	A-31049
21	Potentiometers for Sawtooth Data	A-31050
22	DC Step Comparison Method	A-31051
23	Binary No. to DC - Sweep Method	B-31052
24	Output Switch	A-31053
25	Sweep Amplifier	A-31054
	Table I	B-31153

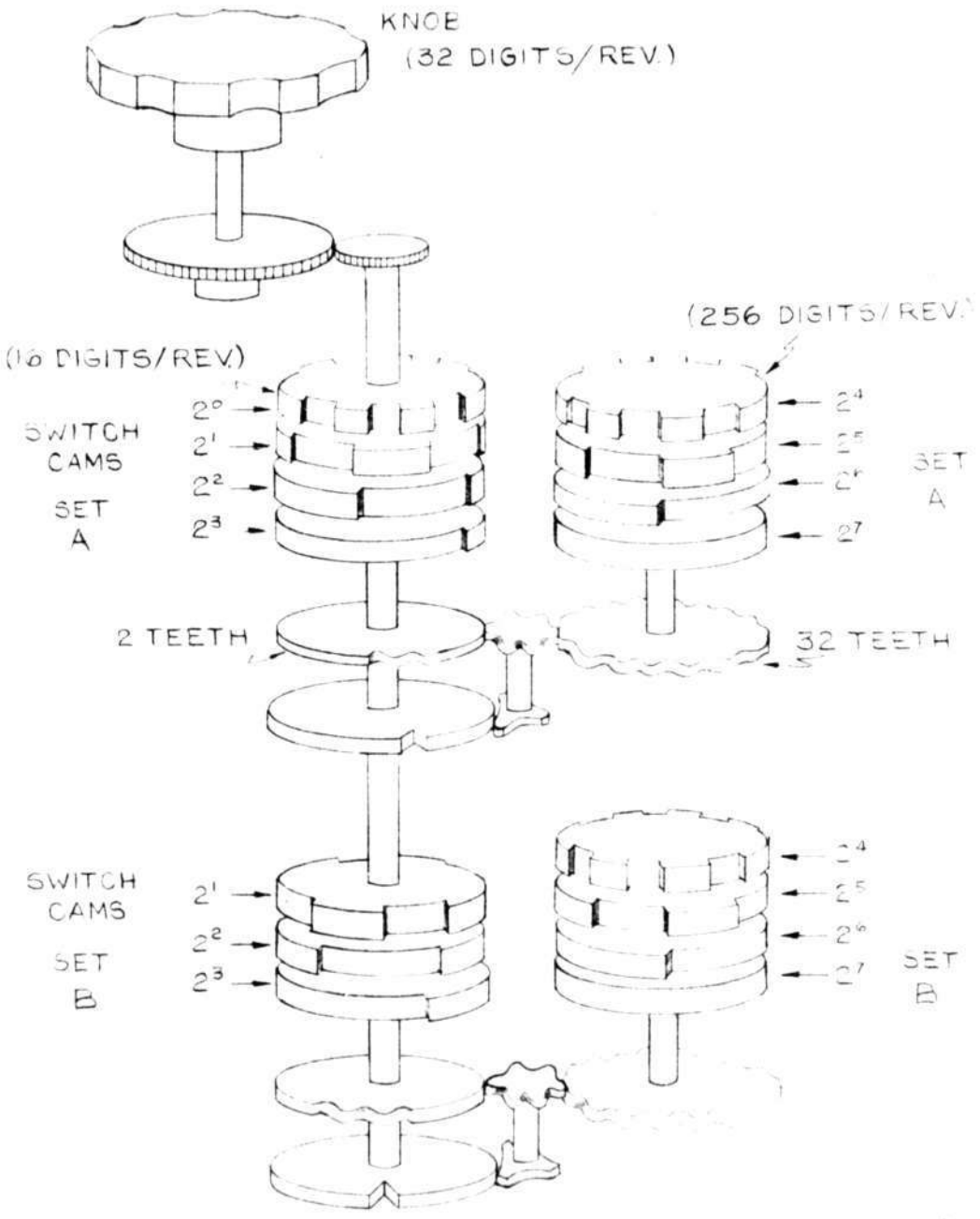


FIG. 1
MECHANICAL COUNTER

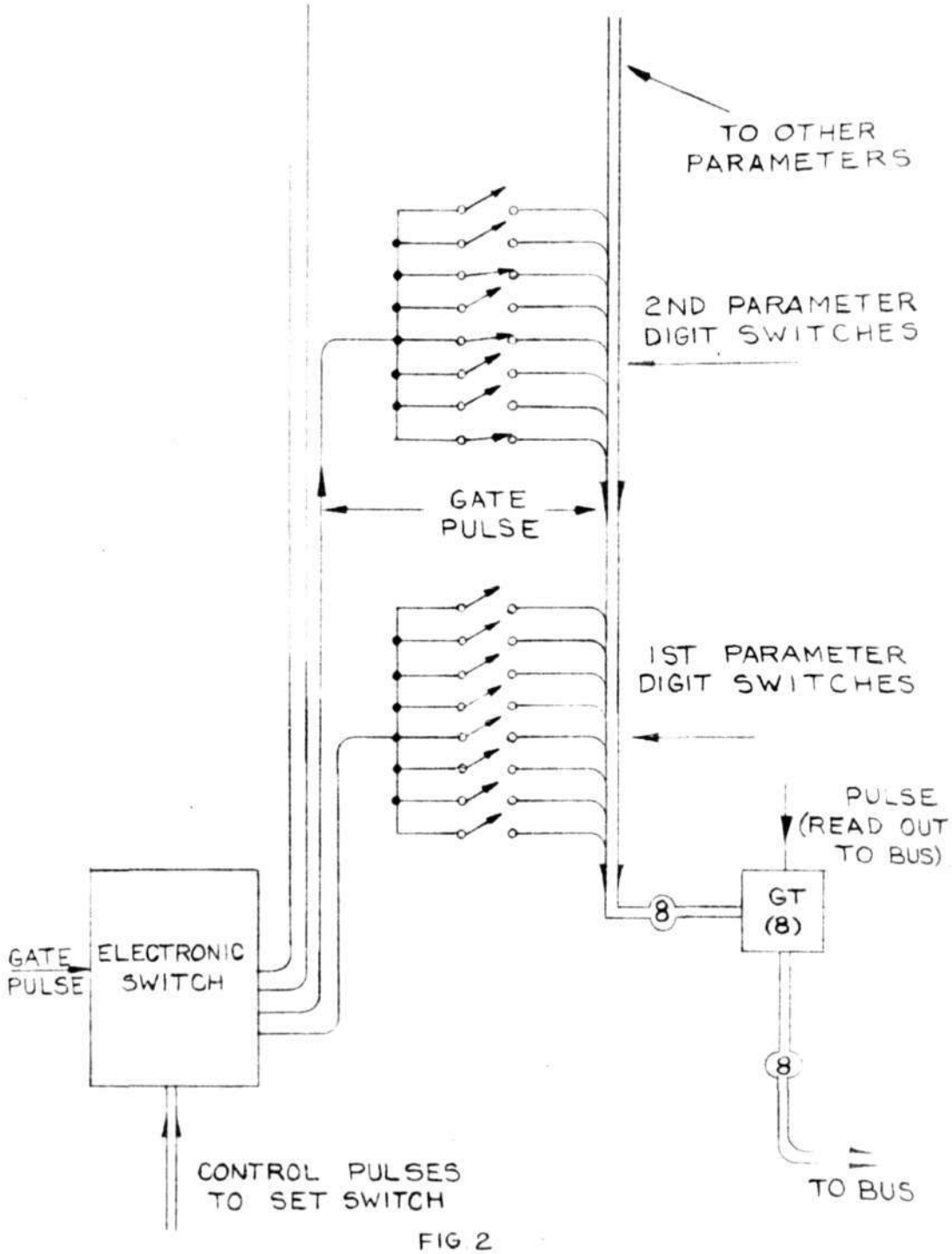


FIG 2
BLOCK DIAGRAM, MECHANICAL COUNTER

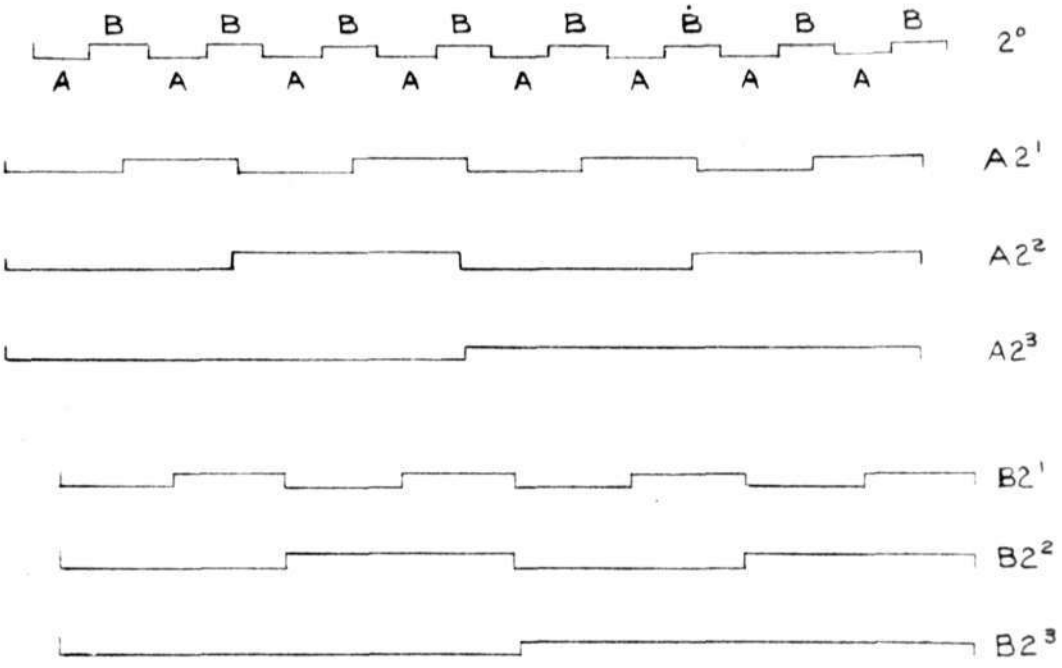


FIG. 3
CAM PHASING

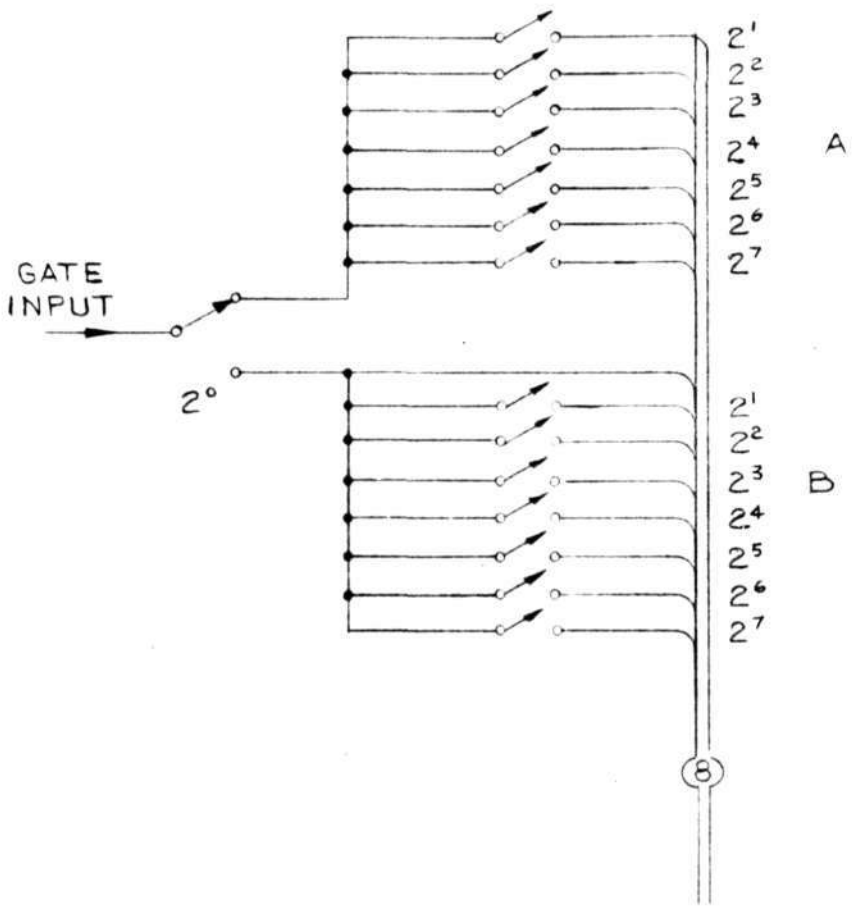


FIG. 4
DOUBLE SWITCH CONNECTIONS

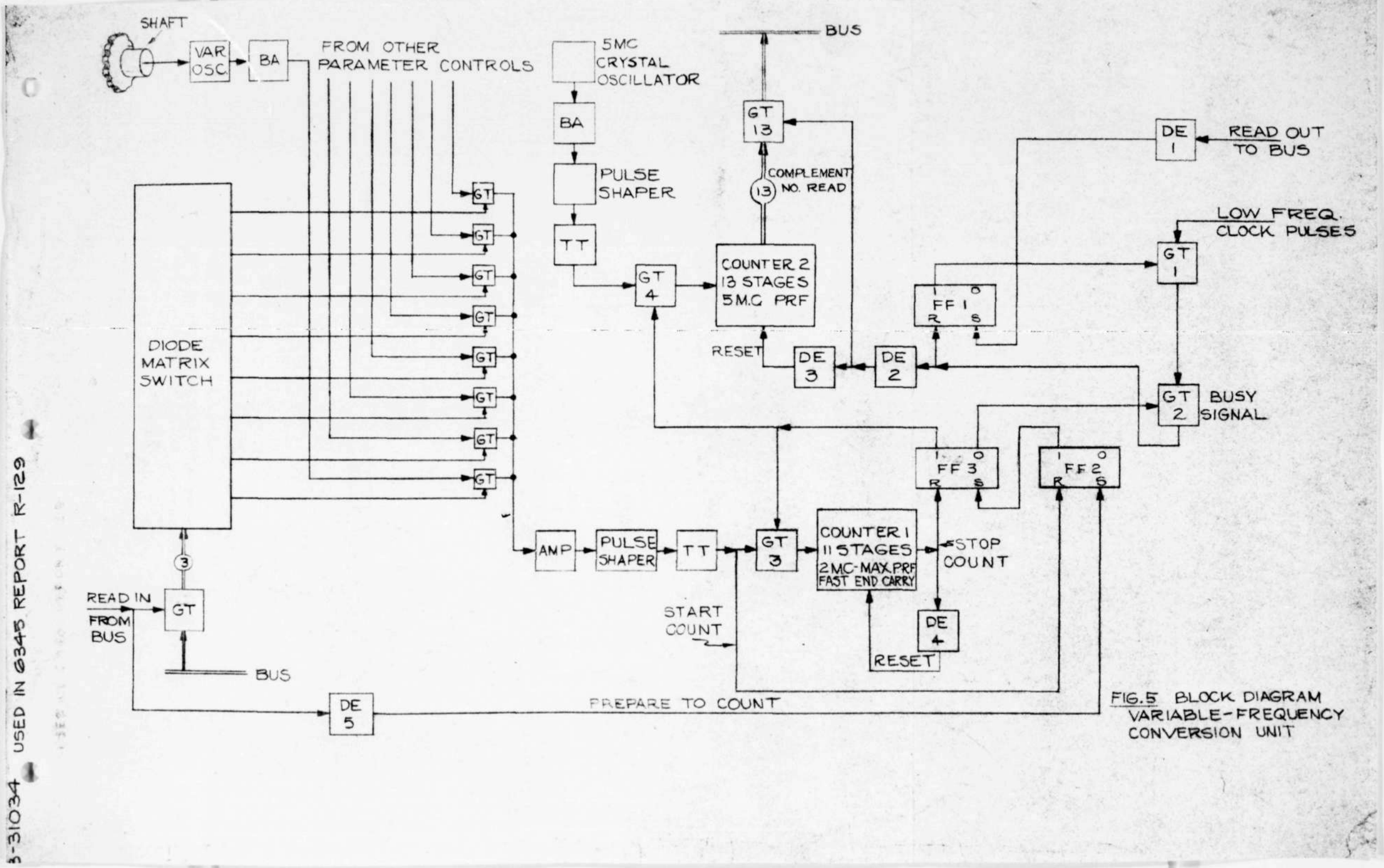


FIG.5 BLOCK DIAGRAM VARIABLE-FREQUENCY CONVERSION UNIT

3-31034 USED IN 6345 REPORT R-129

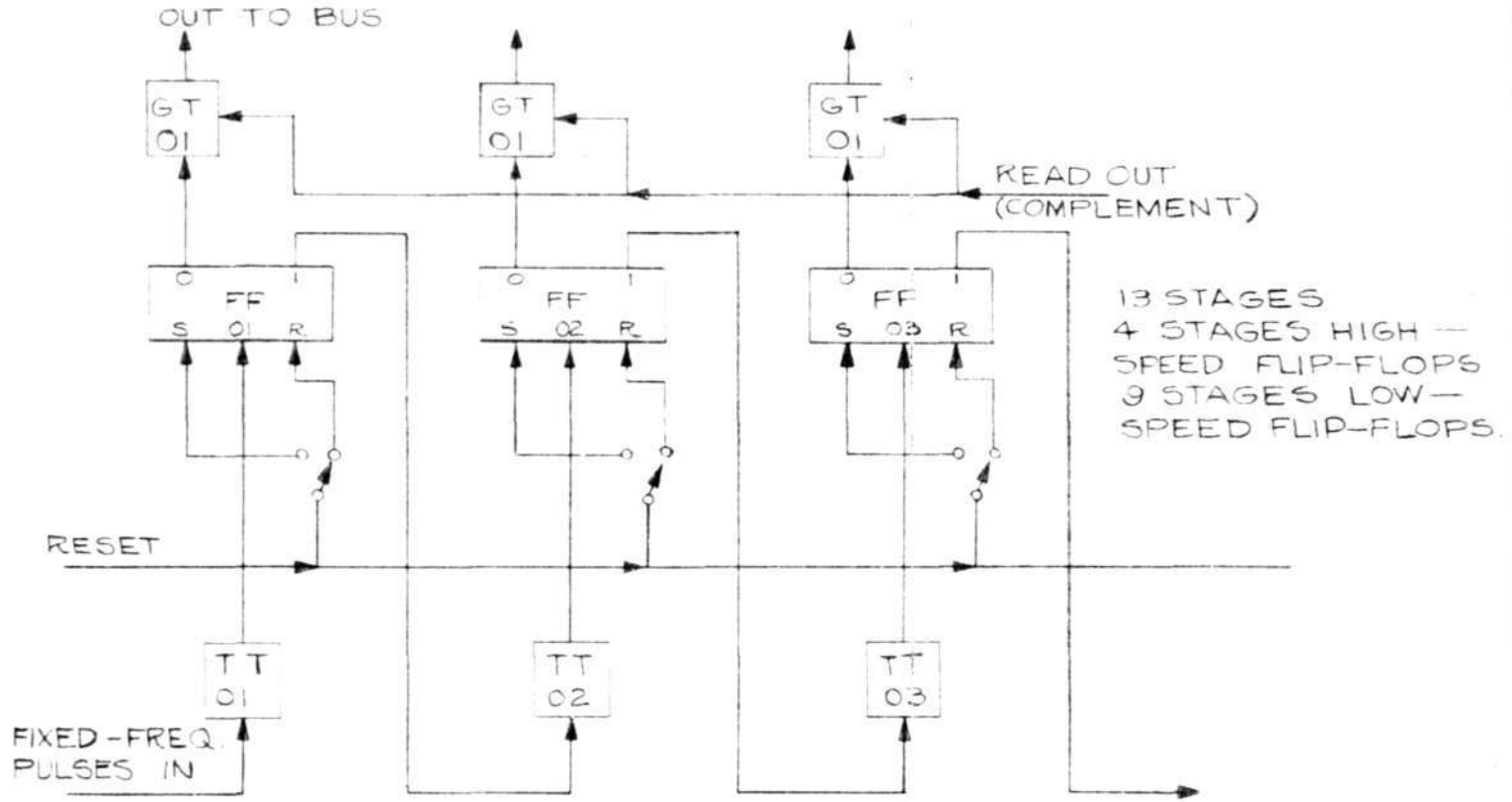
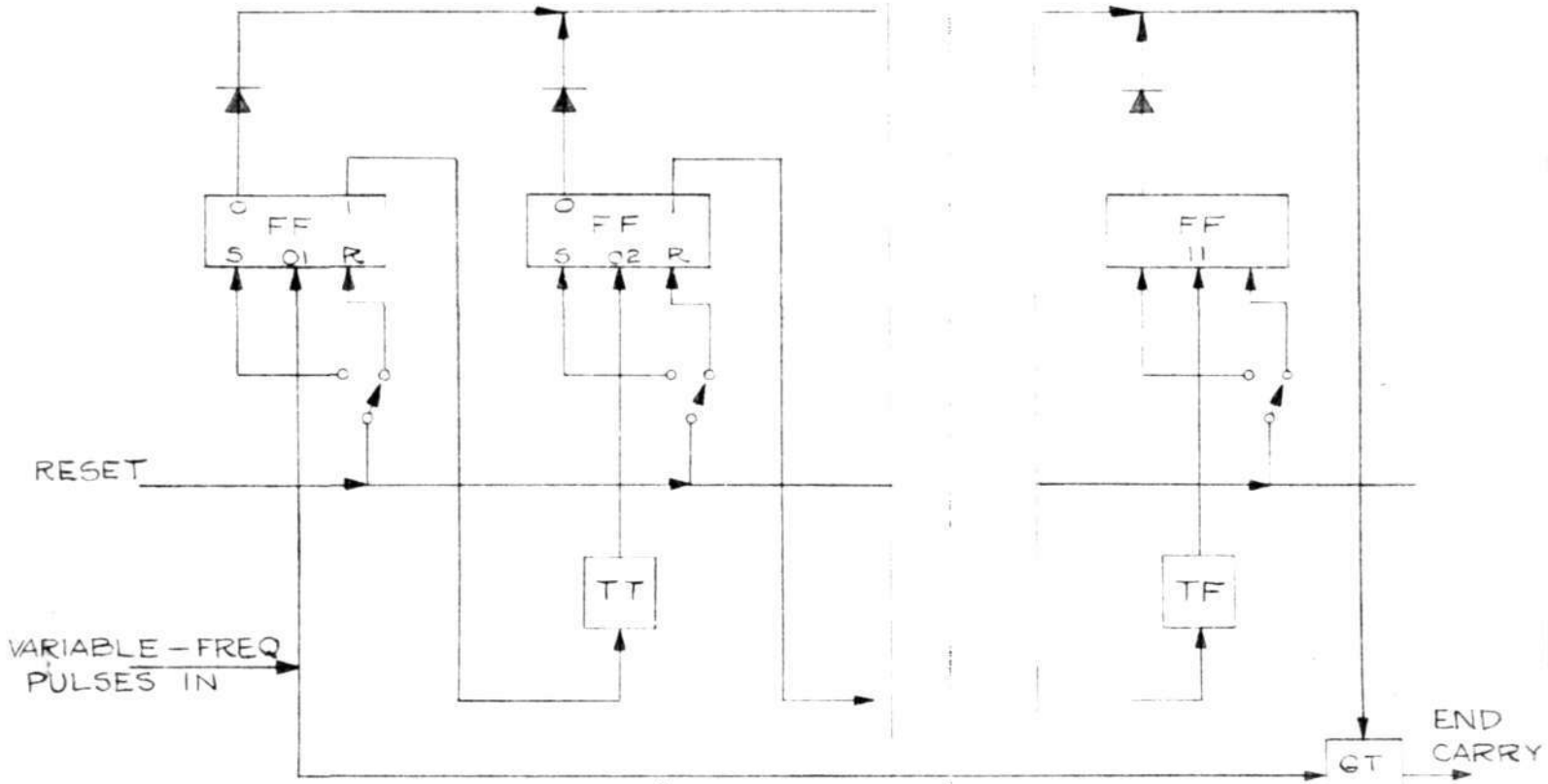


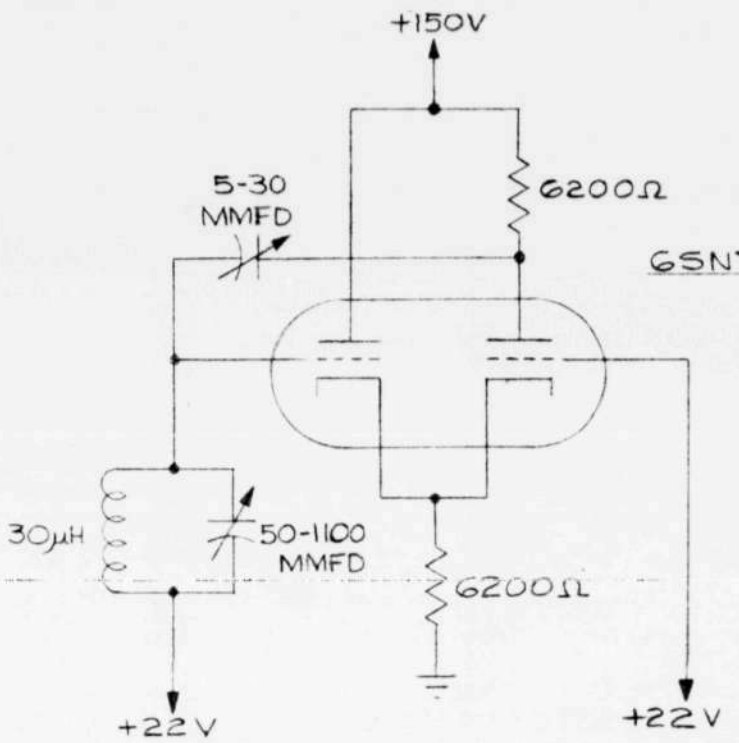
FIGURE 6
FIXED FREQ. PULSE COUNTER.



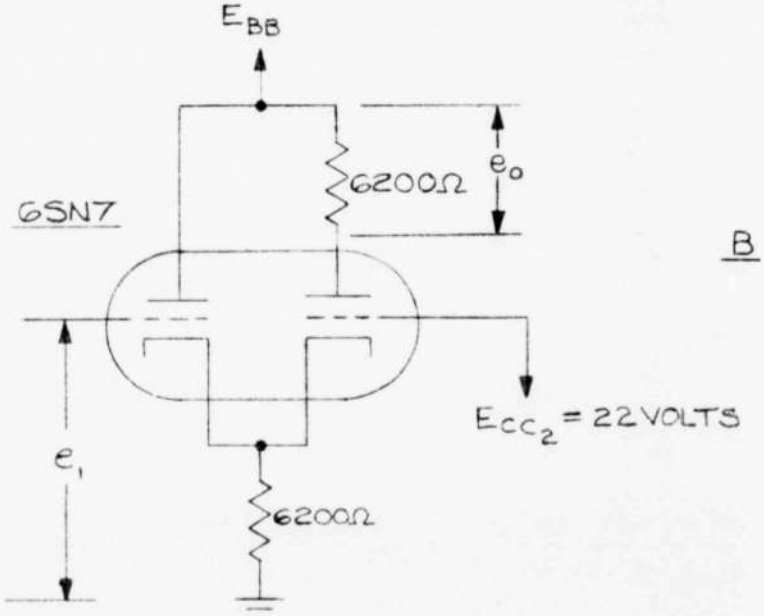
11 STAGES
2 STAGES HIGH-SPEED FLIP-FLOPS
9 STAGES LOW-SPEED FLIP-FLOPS

FIGURE 7
VARIABLE-FREQ.
PULSE COUNTER

A-31037



A



B

FIGURE 8
CATHODE-COUPLED OSCILLATOR

A-31037 USED IN G345 REPORT R-129

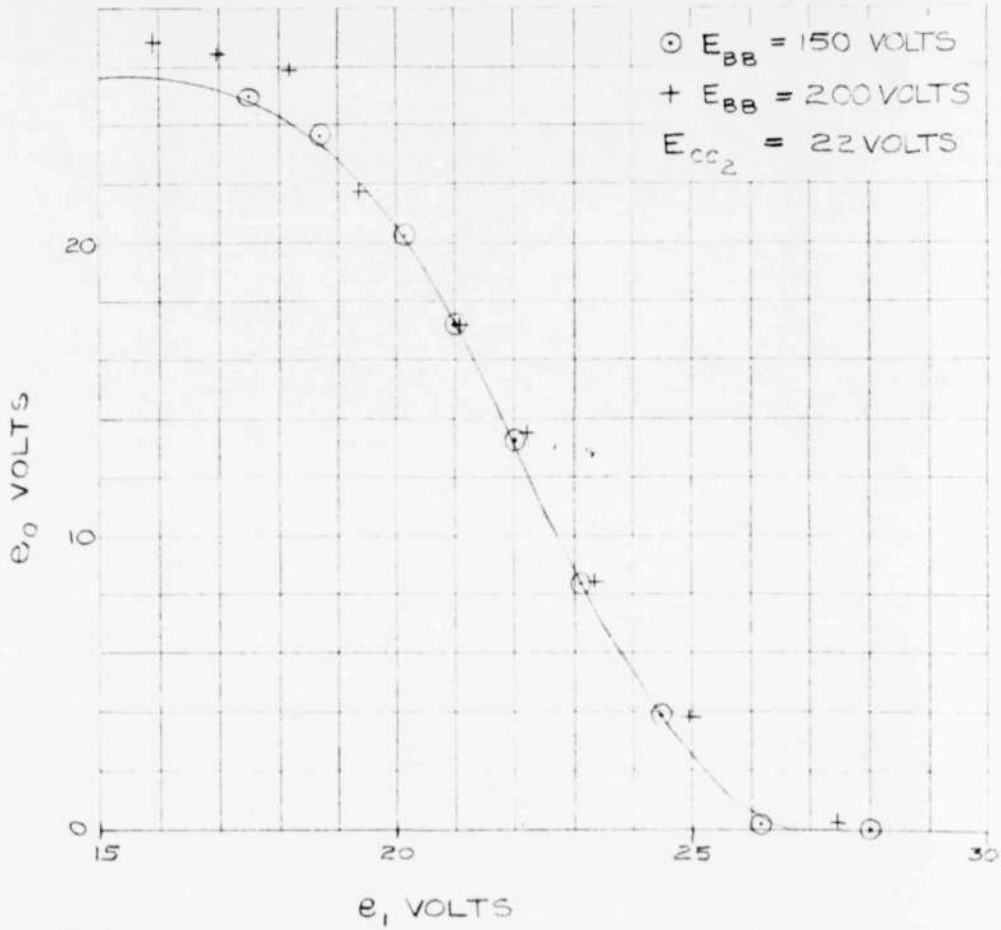


FIGURE 9.
CATHODE-COUPLED OSCILLATOR
STATIC CHARACTERISTICS

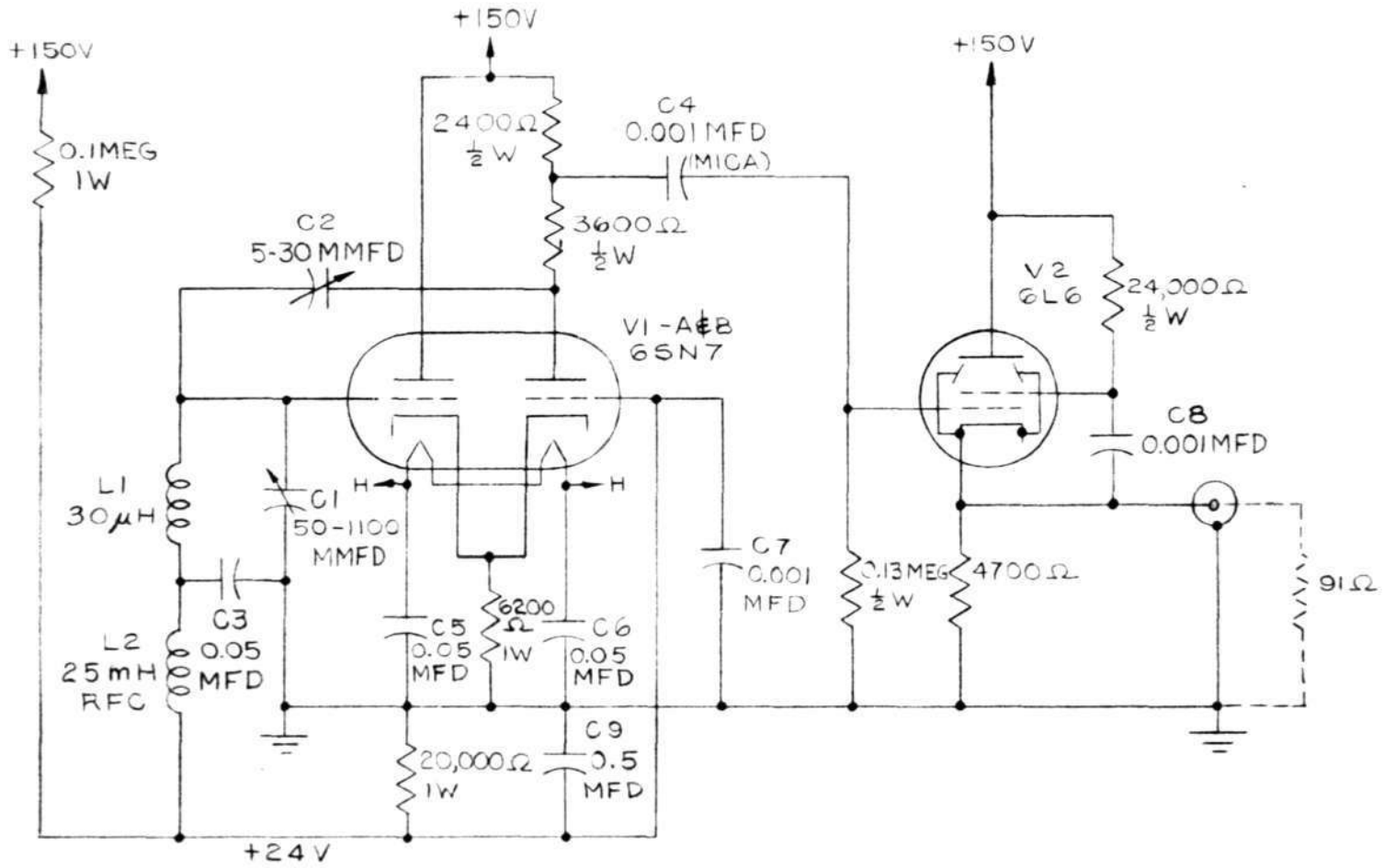
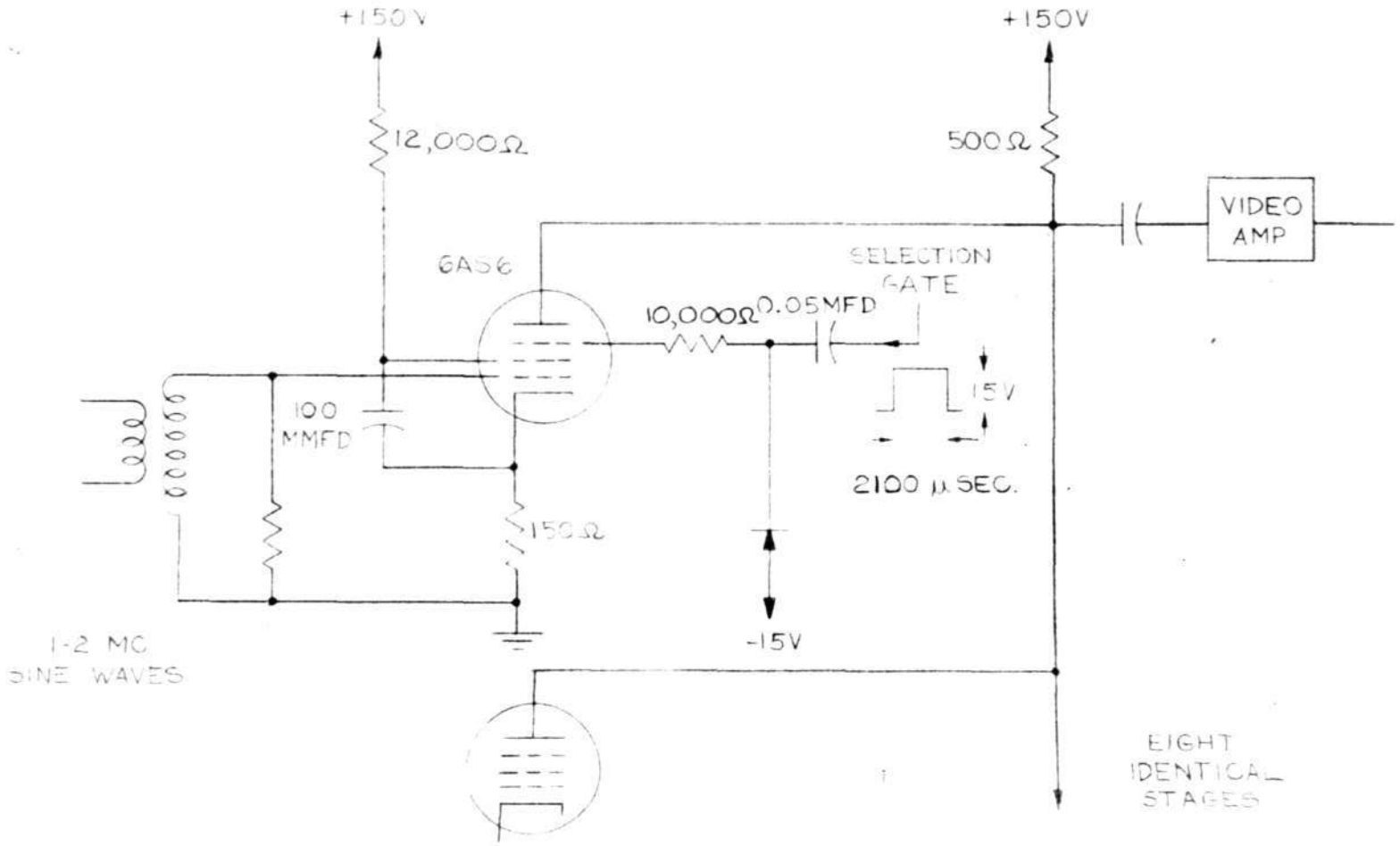


FIG. 10
OSCILLATOR UNIT

A-3104O USED IN 6345 REPORT R-129 A-3104



EIGHT INPUT SELECTION CIRCUIT

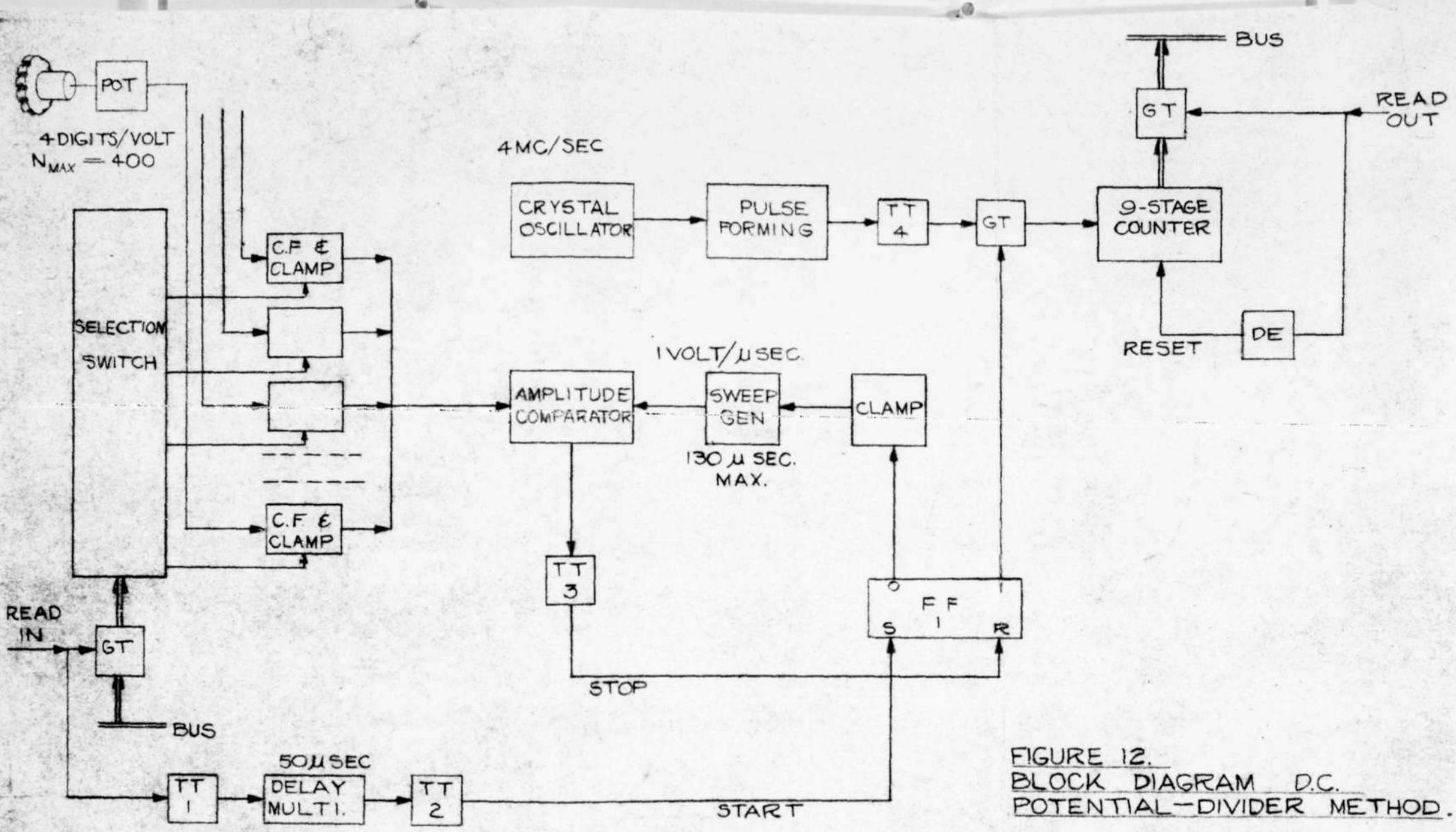


FIGURE 12.
BLOCK DIAGRAM D.C.
POTENTIAL-DIVIDER METHOD.

B-3164 USED IN 6345 REPORT R-129

A-31042

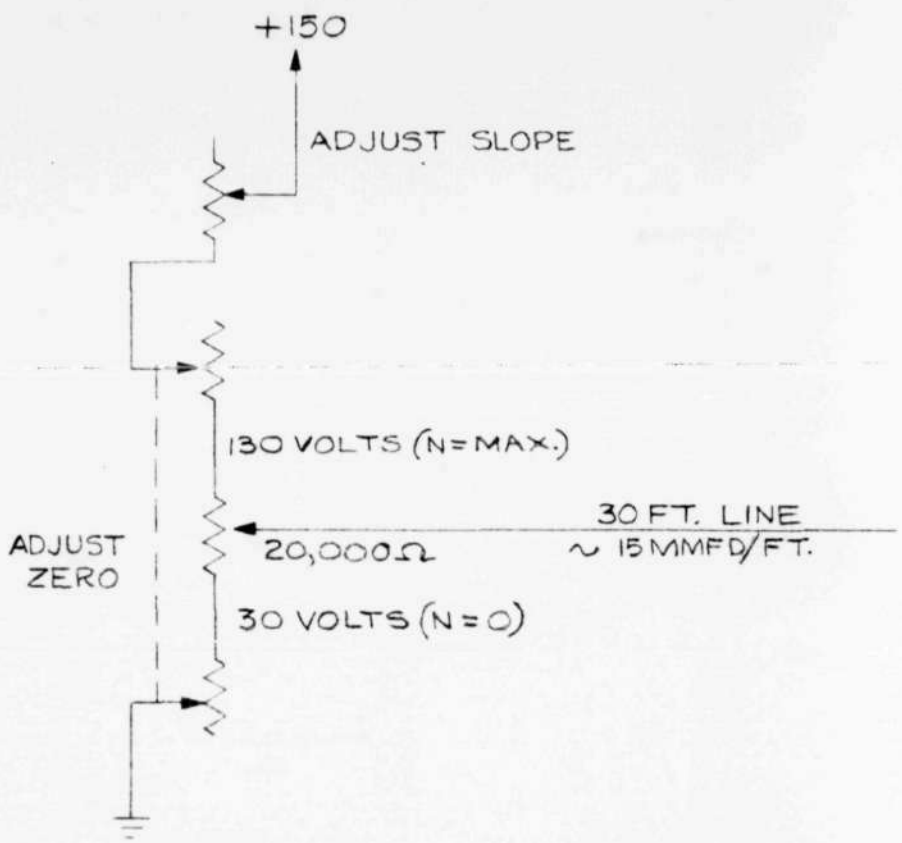


FIGURE 13
CONTROL POTENTIOMETER

A-31042 USED IN 6345 REPORT R-129

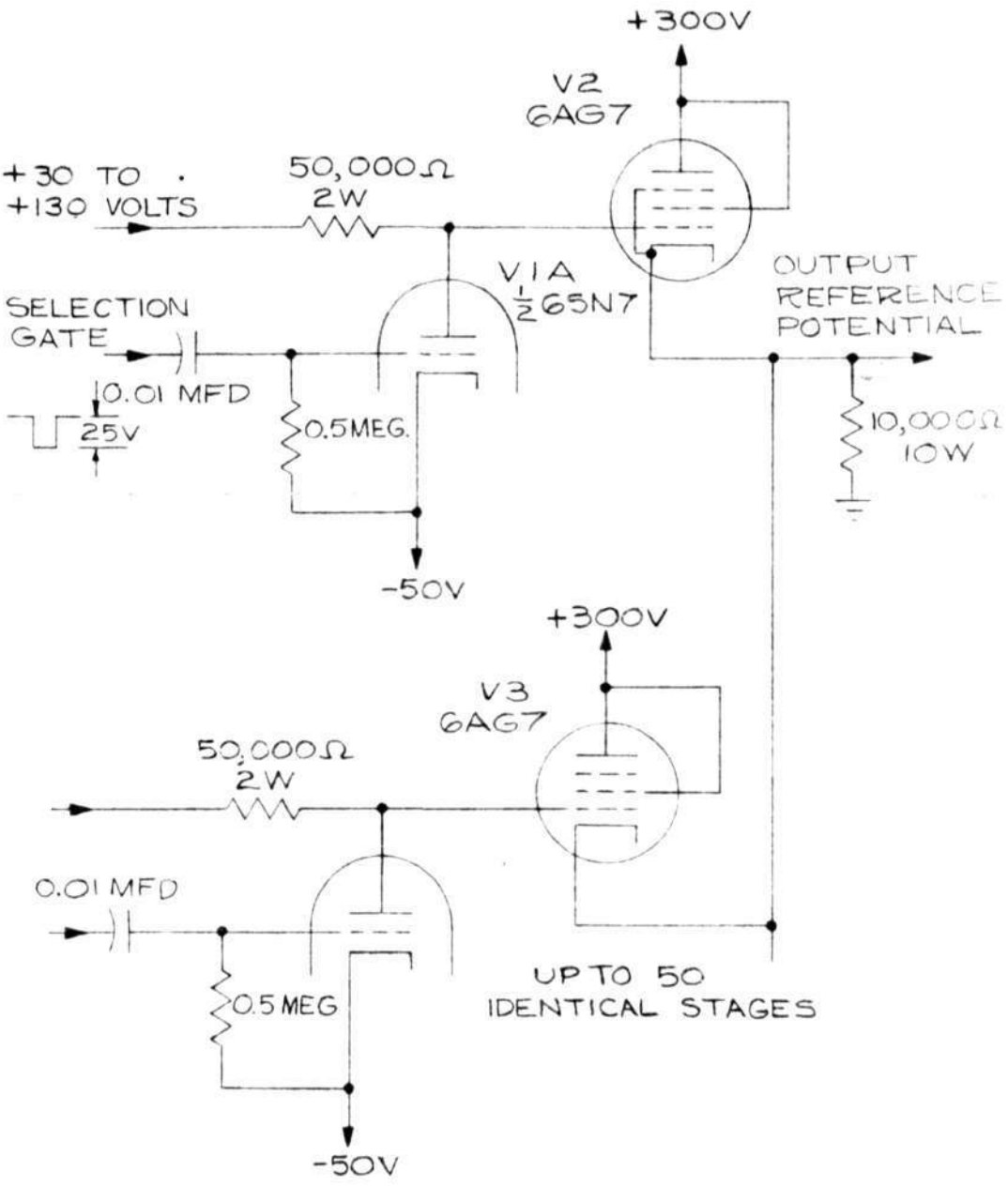


FIGURE 14.
INPUT SELECTION CIRCUIT.

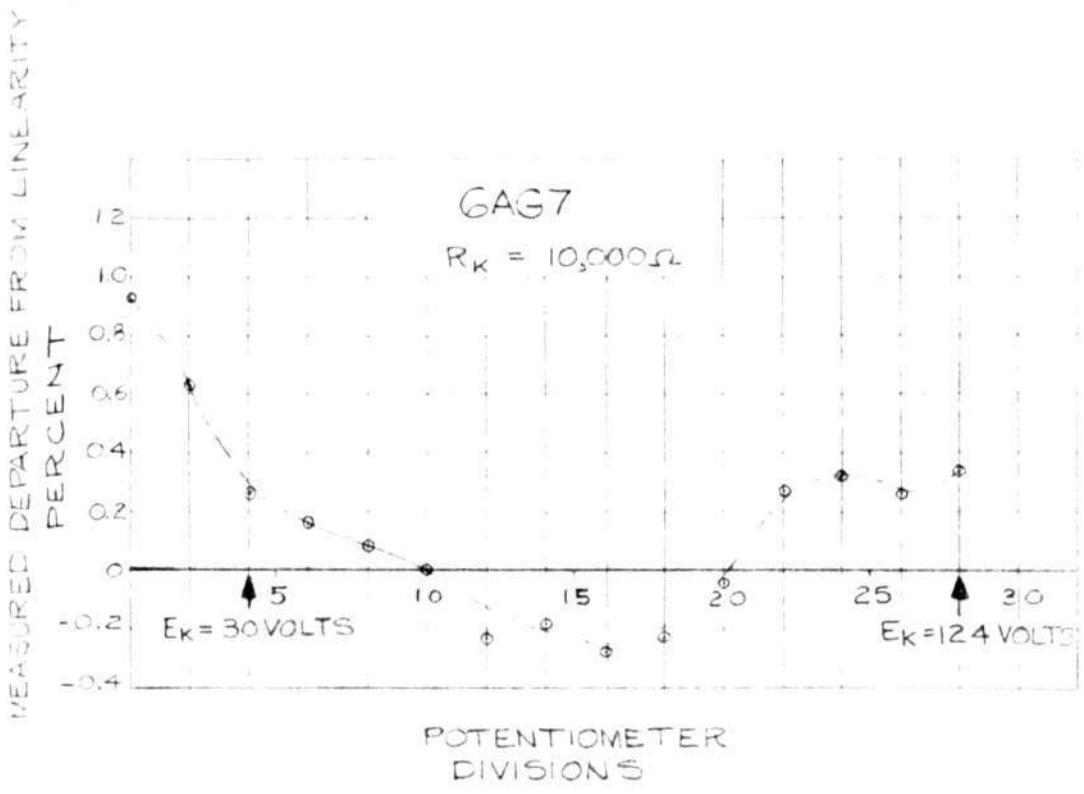
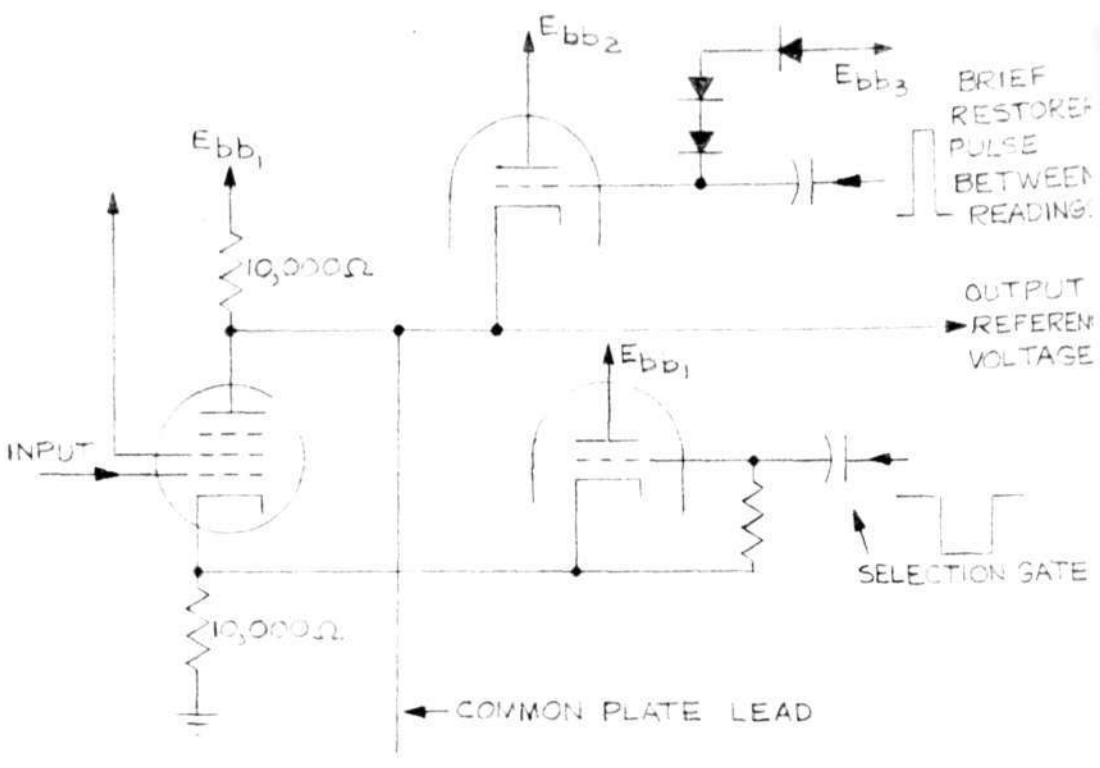


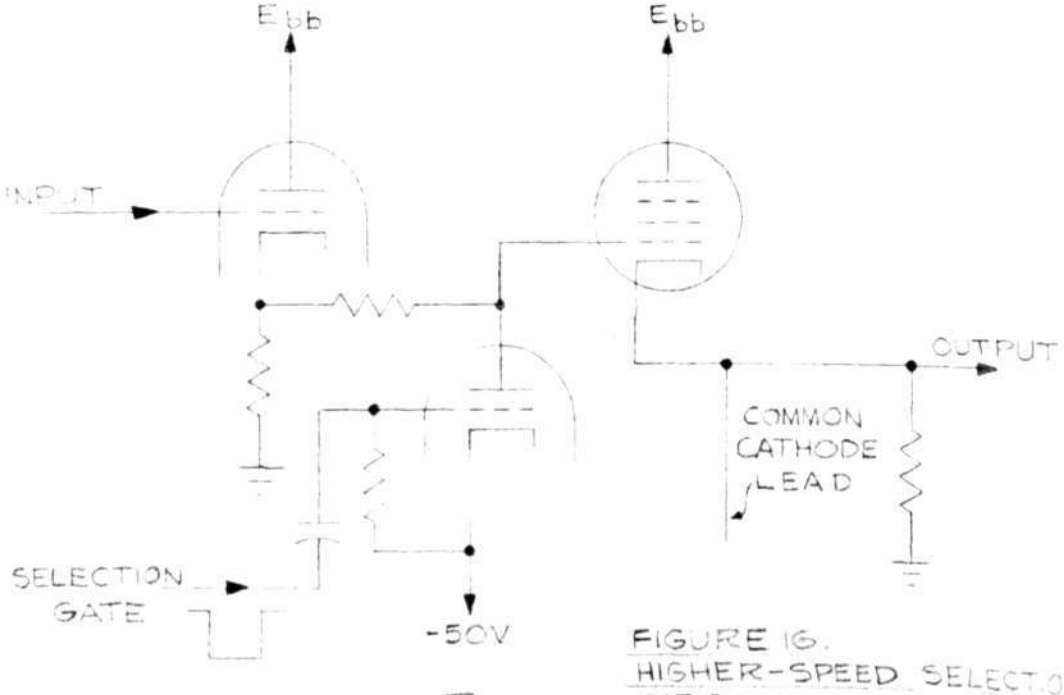
FIGURE 15

CATHODE FOLLOWER LINEARITY.

A-31045



A



B

FIGURE 16. HIGHER-SPEED SELECTION CIRCUITS.

-31045 USED IN 6345 REPORT R-139

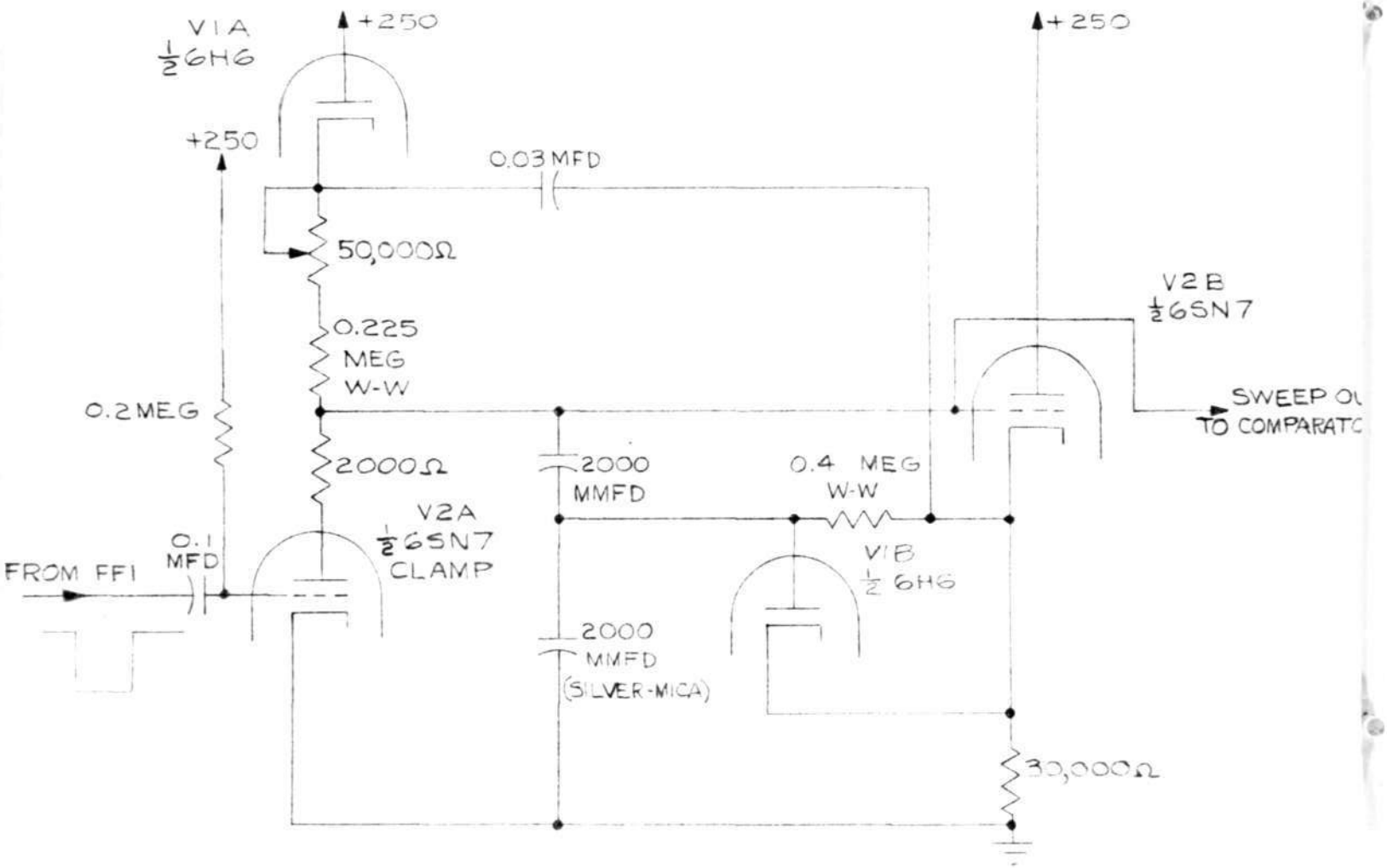


FIGURE 17
SWEEP GENERATOR.

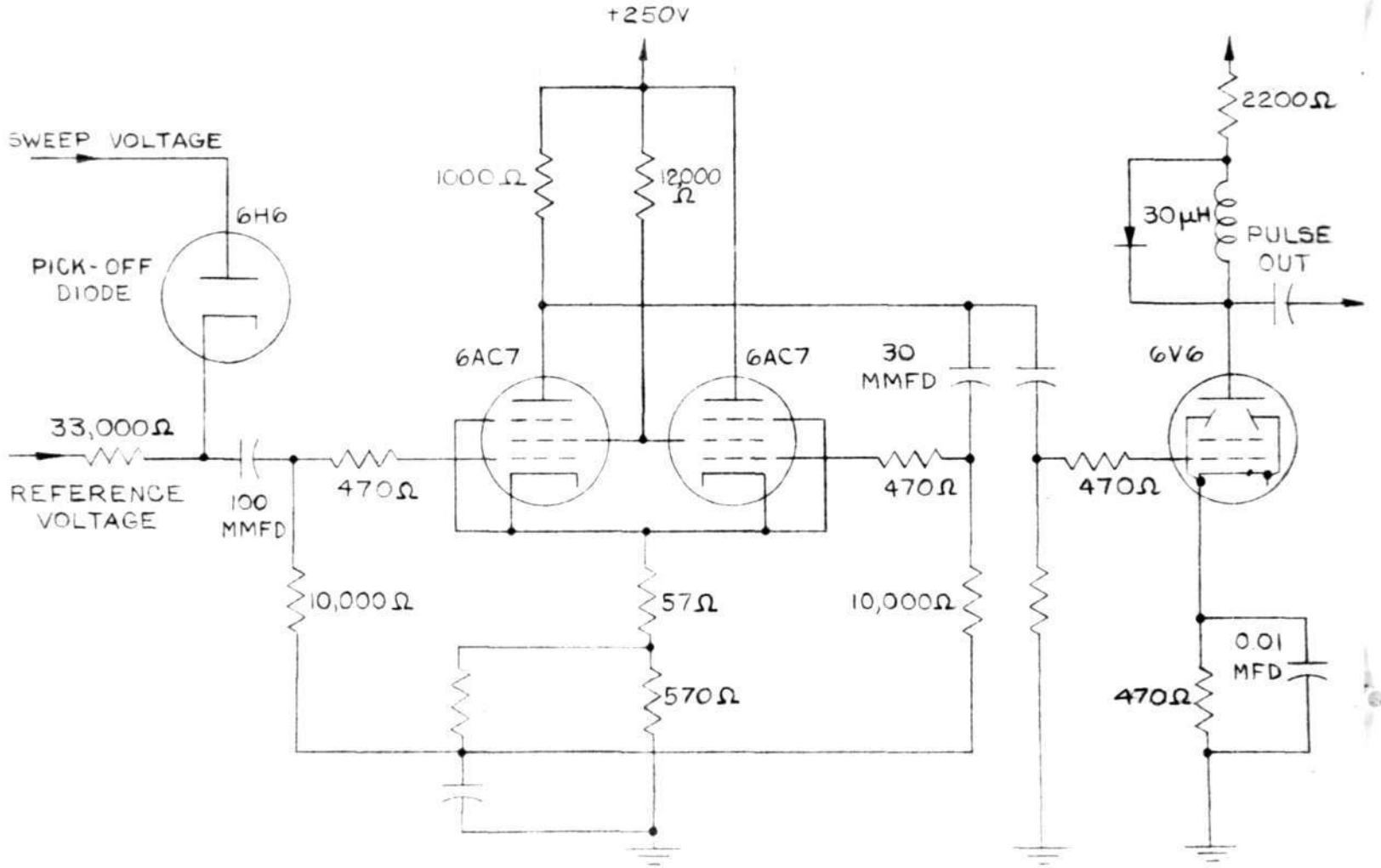


FIG. 18
AMPLITUDE COMPARATOR AND PULSE AMPLIFIER

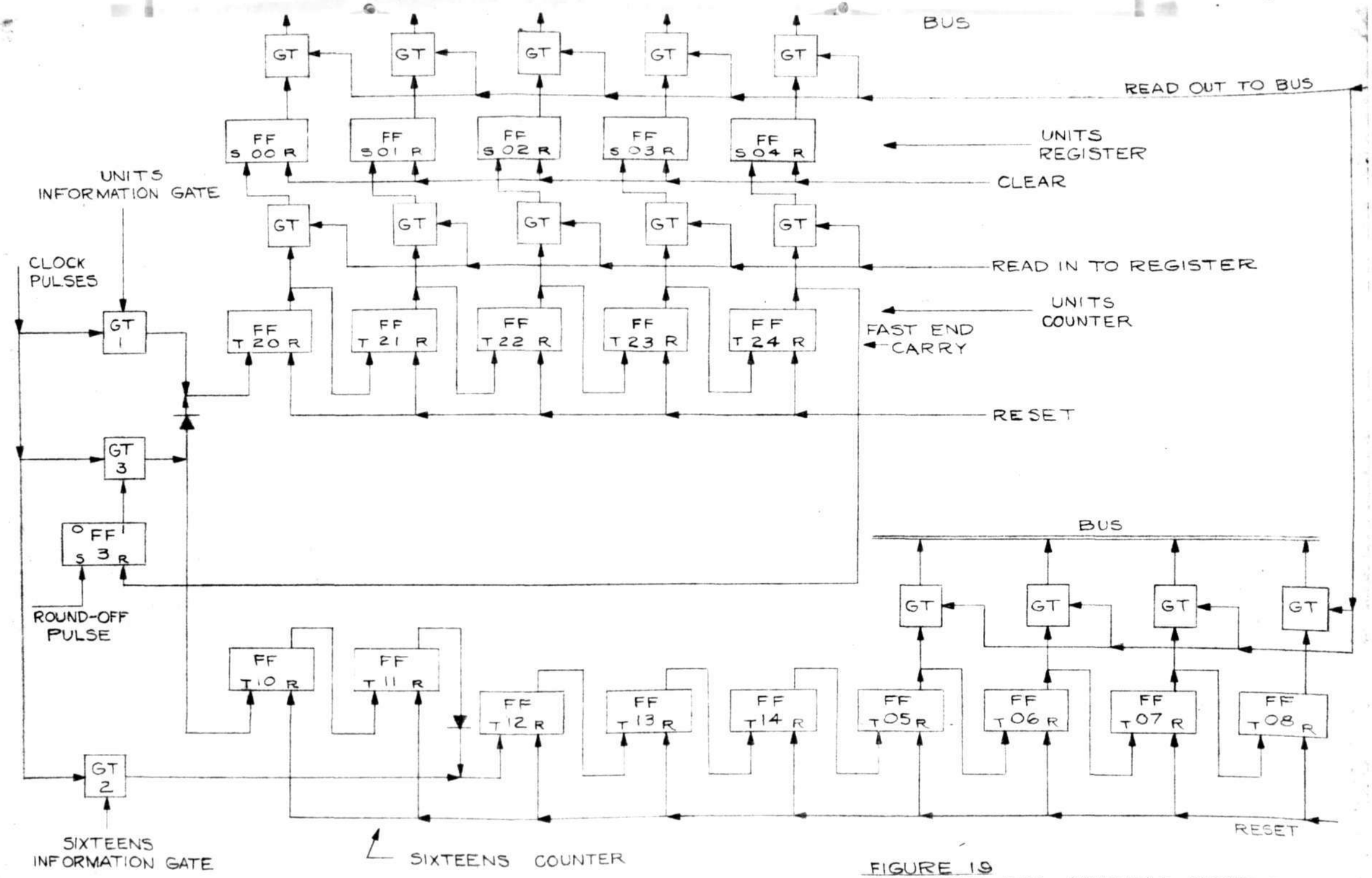
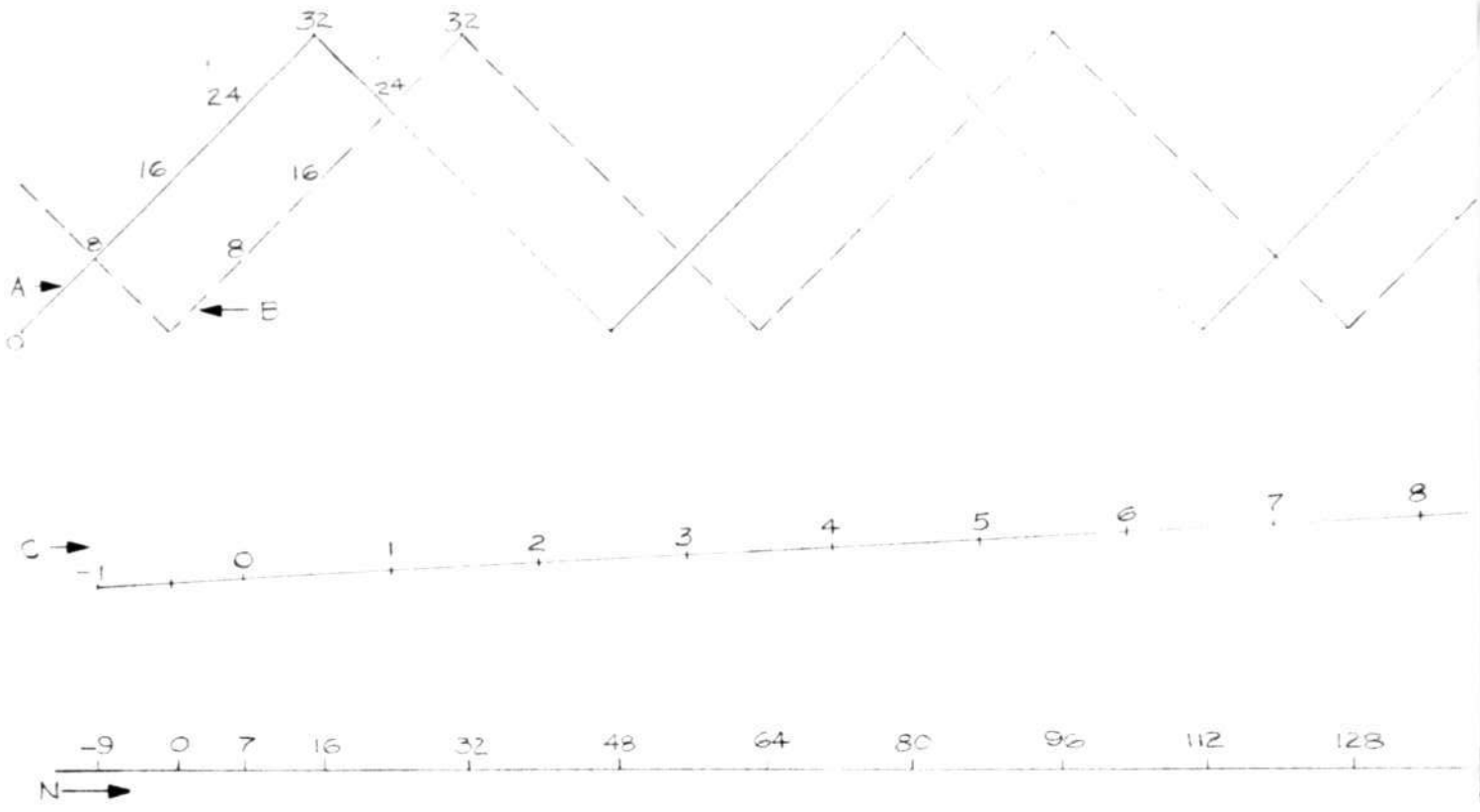


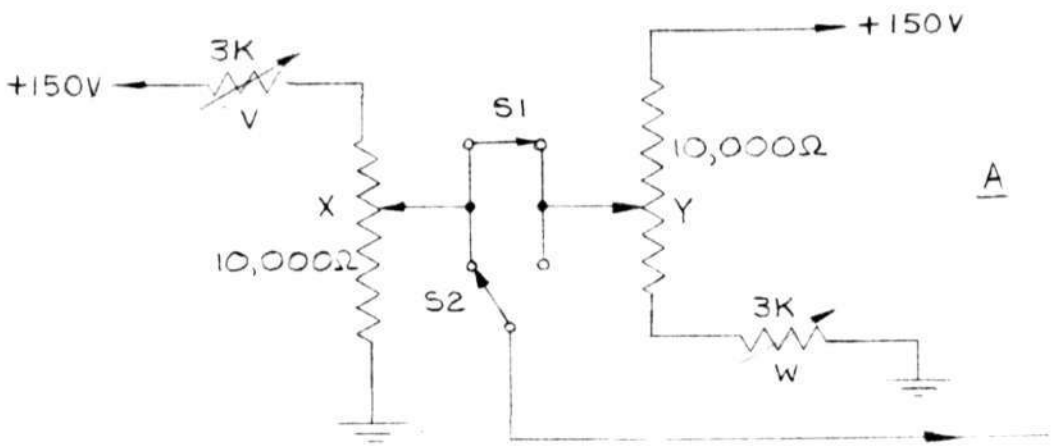
FIGURE 19
COUNTERS FOR MULTIPLE-SPEED DATA

B-31048 USED IN G345 REPORT R-129



FOR C = (-1) , 3 , 7 -- N = C x 16 + (A - 1)
C = 0 , 4 , 8 -- N = C x 16 + (B - 1)
C = 1 , 5 , 9 -- N = C x 16 + [31 - (A - 1 + 1)]
C = 2 , 6 , 10 -- N = C x 16 + [31 - (B - 1 + 1)]

FIGURE 20
HILL-AND-DALE DATA



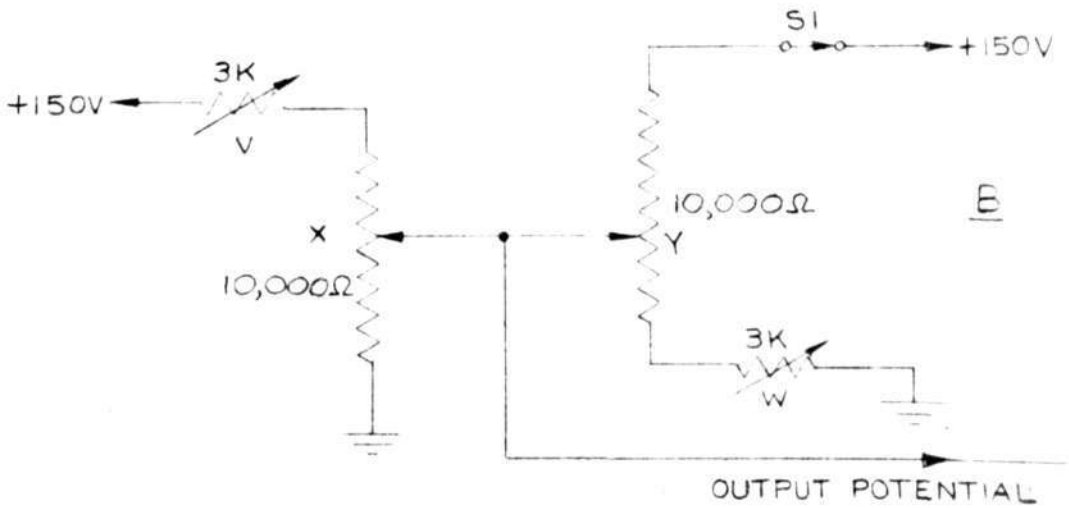


FIG 21
POTENTIOMETERS FOR SAW-TOOTH DATA

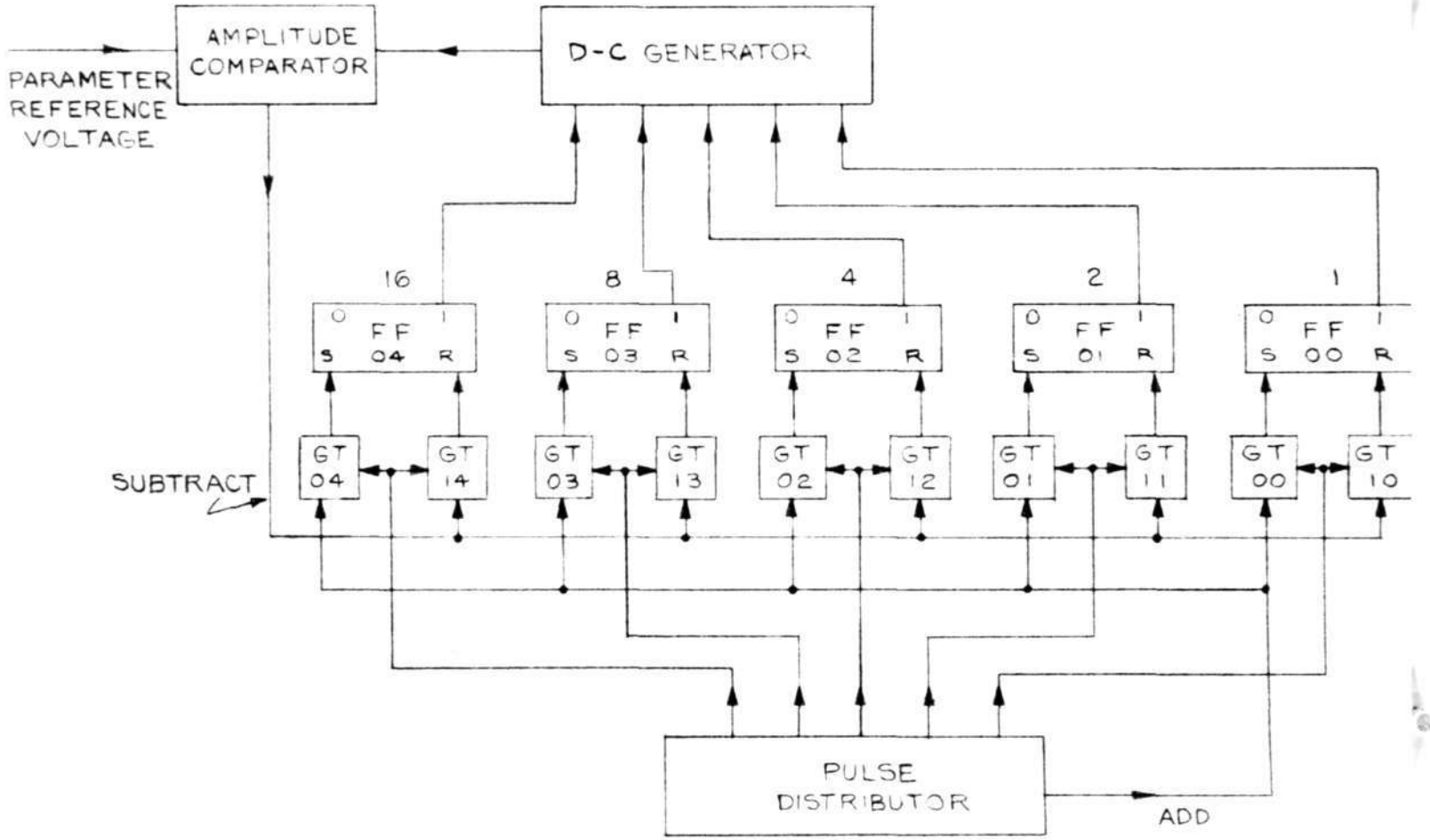


FIG. 22
D-C STEP-COMPARISON METHOD

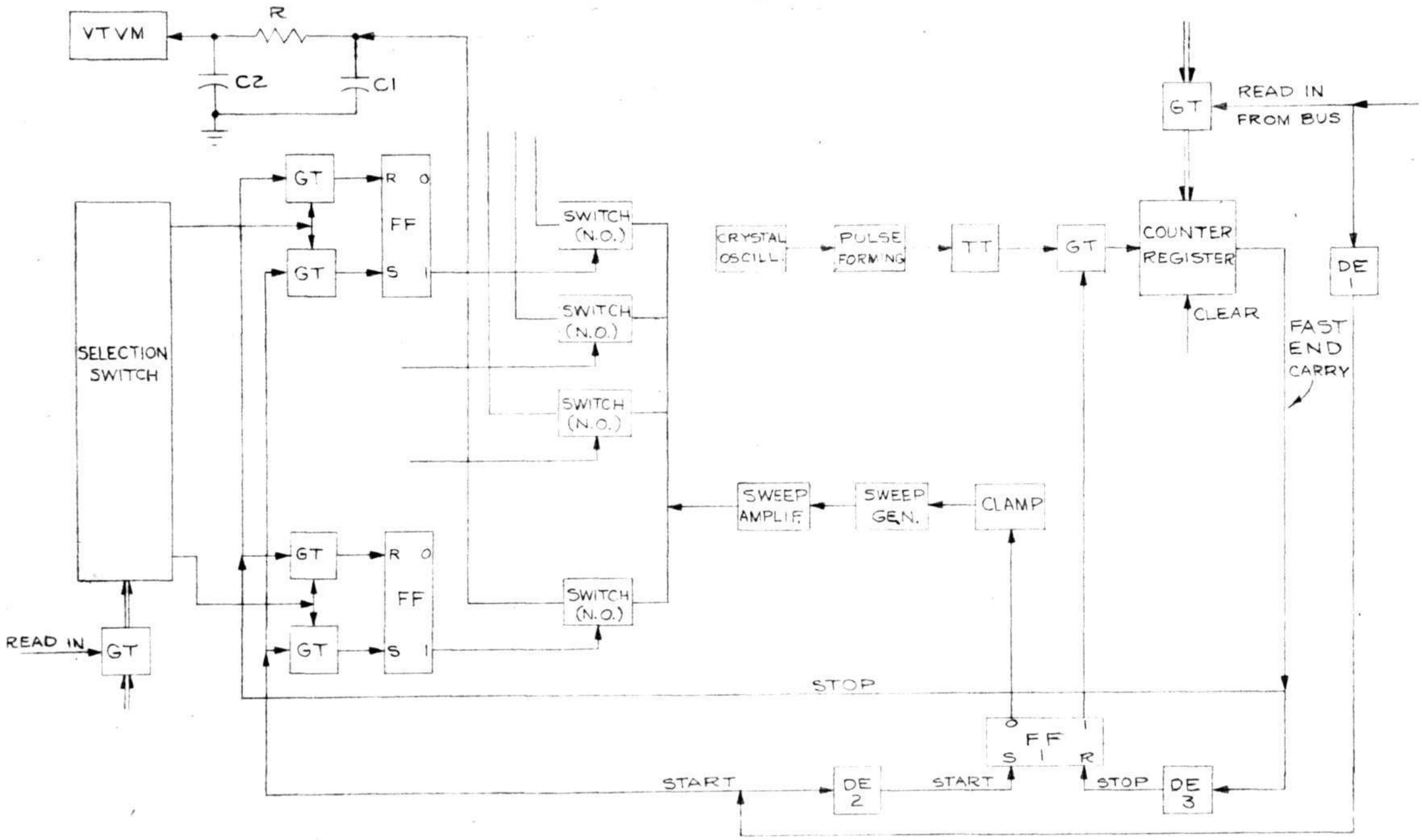


FIGURE 23.
BINARY NO. TO D-C,
SWEEP METHOD.

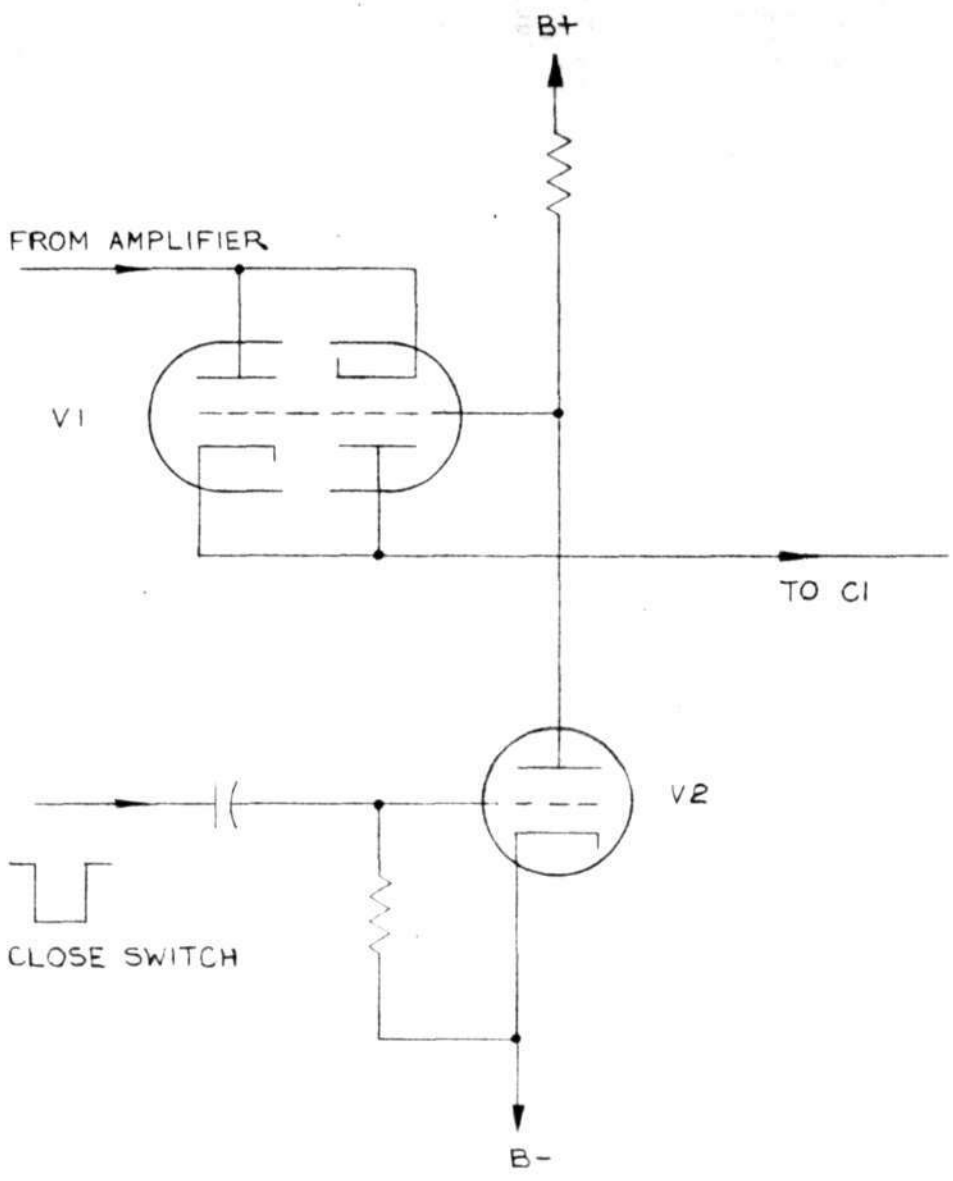


FIG. 24
OUTPUT SWITCH

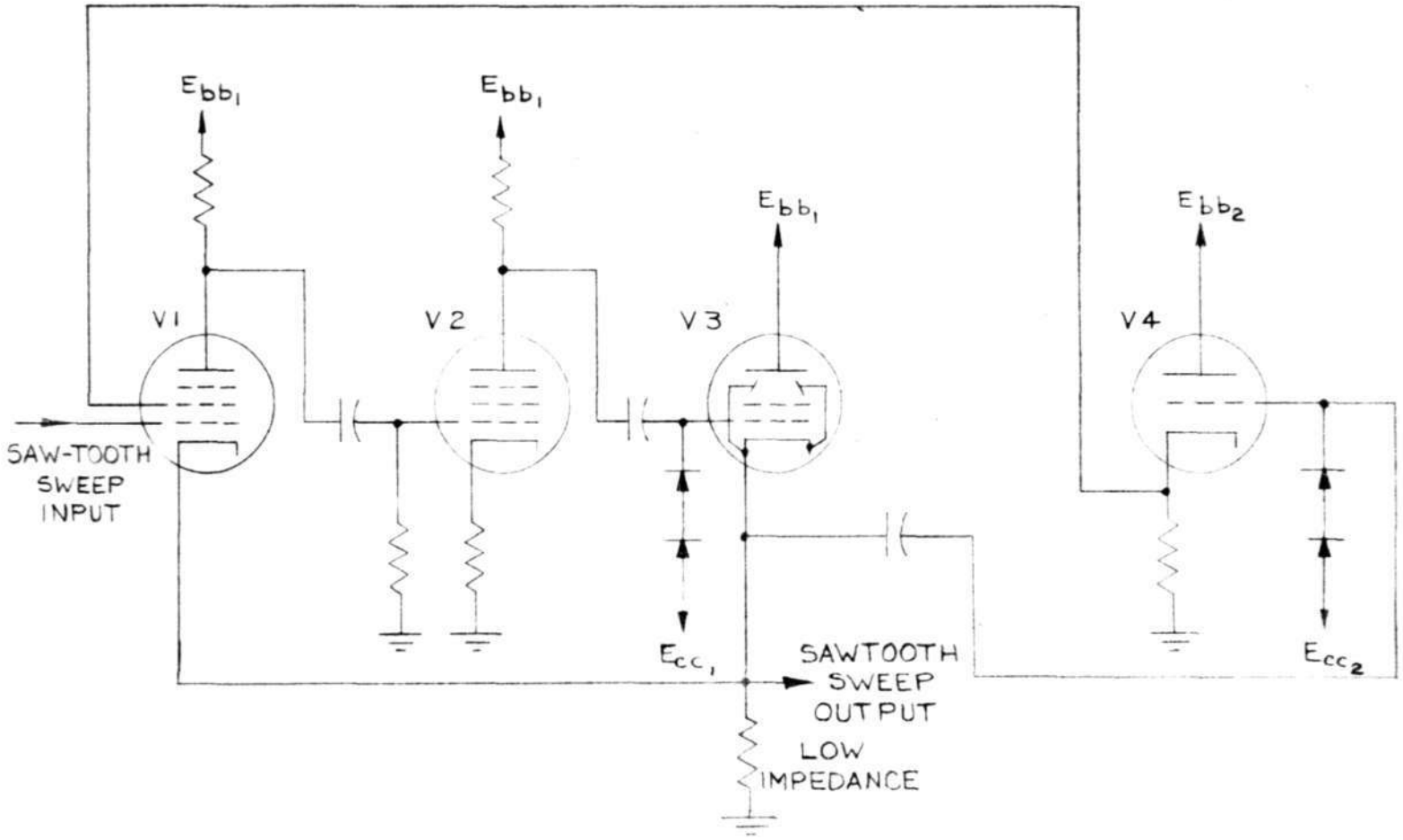


FIG. 25
SWEEP AMPLIFIER

TABLE I

	A	B	C	D
f_c	$\frac{k}{(k-1)}\frac{N_{max}}{\tau_{max}}$	$\frac{k}{(k-1)}\frac{N_{max}}{\tau_{max}}$	$\frac{2ck}{(k-1)}\frac{N_{max}}{\tau}$	$\frac{2ck}{(k-1)}\frac{N_{max}}{\tau}$
f_{min}	$\frac{2ck}{(k-1)}\frac{N_{max}}{\tau_{max}}$	$\frac{2ck}{(k-1)}\frac{N_{max}}{\tau_{max}}$	$\frac{1}{(k-1)}\frac{N_{max}}{\tau}$	$\frac{1}{(k-1)}\frac{N_{max}}{\tau}$
f_{max}	$\frac{2ck^2}{(k-1)}\frac{N_{max}}{\tau_{max}}$	$\frac{2ck^2}{(k-1)}\frac{N_{max}}{\tau_{max}}$	$\frac{k}{(k-1)}\frac{N_{max}}{\tau}$	$\frac{k}{(k-1)}\frac{N_{max}}{\tau}$
r	$\frac{2ck}{(k-1)}N_{max}$	$\frac{2ck}{(k-1)}N_{max}$	$\frac{2ck}{(k-1)}N_{max}$	$\frac{2ck}{(k-1)}N_{max}$
N_{max}	$n_o = \frac{k}{(k-1)}N_{max}$	$\frac{k}{(k-1)}N_{max}$	$\frac{k}{(k-1)}N_{max}$	$n_o = \frac{k}{(k-1)}N_{max}$
n_{min}	$\frac{N_{max}}{(k-1)}$	$n_o = \frac{N_{max}}{(k-1)}$	$n_o = \frac{N_{max}}{(k-1)}$	$\frac{N_{max}}{(k-1)}$
N	$n_o(1-\frac{f_{min}}{f})$	$n_o(\frac{N_{max}}{f}-1)$	$n_o(\frac{f}{f_{min}}-1)$	$n_o(1-\frac{f}{f_{max}})$
Uncertainty in N caused by uncertainty in f $dN =$	$(n_o-N)\frac{df}{f}$	$-(N+n_o)\frac{df}{f}$	$+(N+n_o)\frac{df}{f}$	$-(n_o-N)\frac{df}{f}$
For N = 0				
f	minimum	maximum	minimum	maximum
τ	maximum	minimum	constant	constant
* Allowable drift df	$\frac{\epsilon}{\tau_{max}}$	$-\frac{k^2\epsilon}{\tau_{max}}$	$\frac{1}{2\tau}$	$-\frac{1}{2\tau}$
Allowable fractional drift $\frac{df}{f}$	$\frac{(k-1)}{2k}\frac{1}{N_{max}}$	$-\frac{(k-1)}{2N_{max}}$	$\frac{(k-1)}{2N_{max}}$	$\frac{(k-1)}{2k}\frac{1}{N_{max}}$
For $N = N_{max}$				
f	maximum	minimum	maximum	minimum
τ	minimum	maximum	constant	constant
** Allowable drift df	$\frac{2k^2\epsilon}{\tau_{max}}$	$-\frac{2\epsilon}{\tau_{max}}$	$\frac{1}{\tau}$	$-\frac{1}{\tau}$
** Allowable fractional drift $\frac{df}{f}$	$\frac{(k-1)}{N_{max}}$	$-\frac{(k-1)}{k}\frac{1}{N_{max}}$	$\frac{(k-1)}{k}\frac{1}{N_{max}}$	$-\frac{(k-1)}{N_{max}}$
For linearity of N make	$-\frac{1}{f}$ linear	$\frac{1}{f}$ linear	f linear	-f linear

* Assuming $dN = 1/2$

** Assuming $dN = 1$