Digital Computer Laboratory
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SUBJECT: A FAST CORE-TUBE REGISTER

To: Norman H. Taylor

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The circuit to be described was developed for use in MTC, but was not used for lack of time. Its purpose is to serve as temporary storage thus taking the place of a flip-flop and two gate tubes.

A circuit diagram is given in Figure 1. The core of T_1 is a square-looped material. V_1 is used to write information into the core when hit by a "write" pulse. V_2 is used to read the information contained in the core. If a "1" is contained in the core a positive pulse appears at the output. If the core contains a zero, a small negative pulse appears at the output. Without the compensating network, R_1 and L_1, a "0" in the core would produce a small positive output. However, the effect of this compensating network is to subtract a small pulse from both the "1" and "0" output pulses. The "1" output is slightly reduced but "0" output is completely cancelled out. In fact, the "0" output may be slightly negative.

Figure 2 gives experimental results for the circuit shown in Figure 1. The output was photographed while "0's" and "1's" were read in and out alternatively. The photograph was then traced on the drawing. Many extensions and variations of this basic circuit are possible.

Signed K. H. Olsen
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Approved
N. H. Taylor,
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KHO/RP:jrt

Drawings attached:
A-54763
A-54807

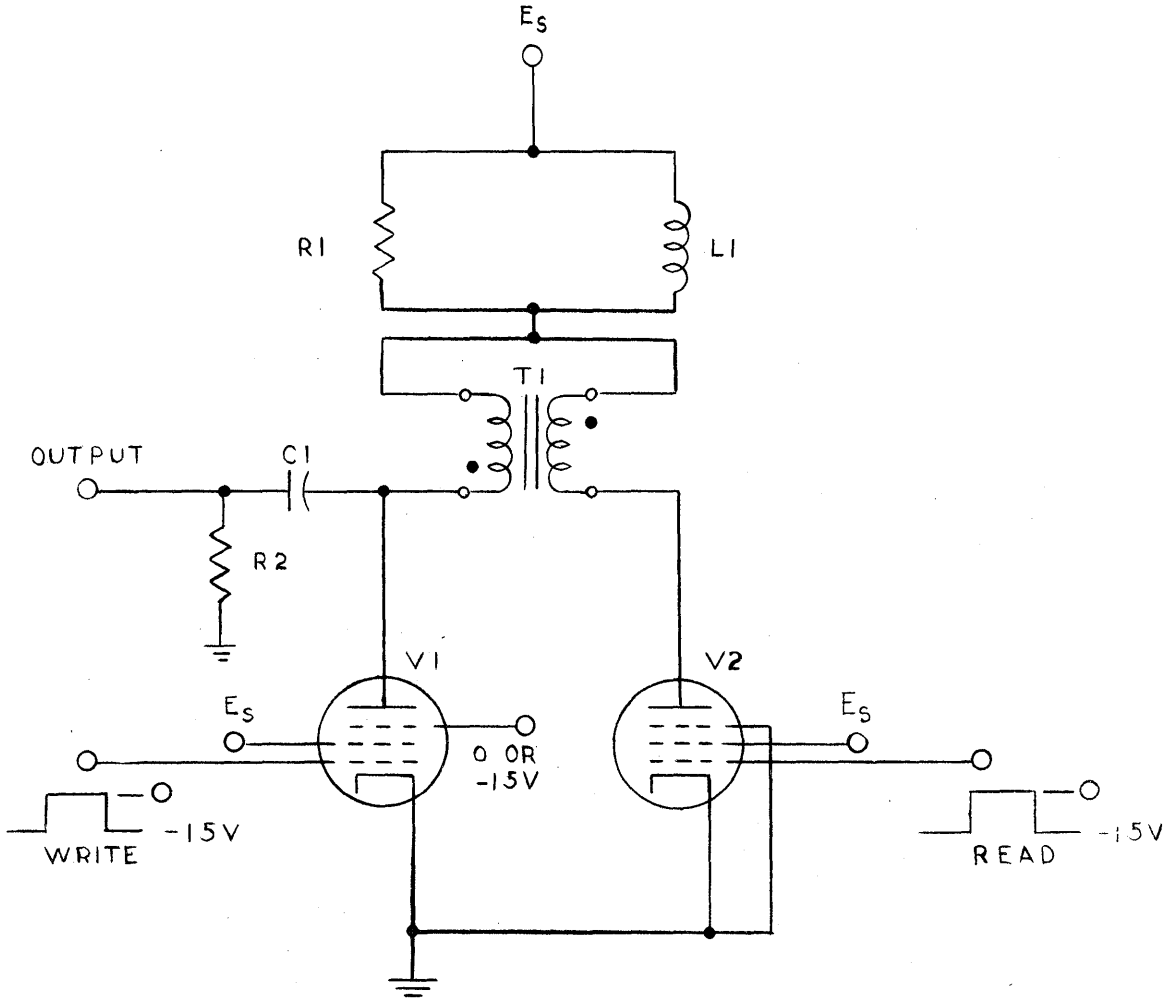

FIG. 1

A FAST CORE—TUBE REGISTER

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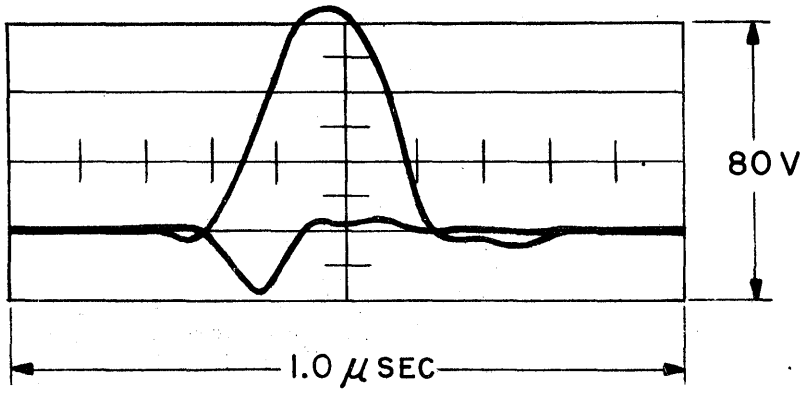

V_1, V_2 = 7AK7

T_1 = 1/4 MIL, MO-PERMALLOY, 40 WRAP TOROID; 1/8" BOBBIN, EACH WINDING 30 TURNS.

R_1 = 1000Ω

R_2 = 100 K

L_1 = 56 μH

C_1 = 56 MMFD

E_s = 250 V

READ AND WRITE PULSES 15V, 0.4 μ SEC WIDE.

FIGURE 2

EXPERIMENTAL RESULTS

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