Division 6 — Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: A TRANSISTORIZED VARIABLE DELAY UNIT

To: Group 63 Staff

From: Leonard Kleinrock Leonard Kleinrock

Date: September 12, 1957

Approved: BMG

Abstract: This transistorized variable delay unit converts a negative pulse into a 3 volt negative level whose width is adjustable over a range from 0.3 microseconds to 2.5 seconds. Greater widths may be obtained by adding capacitance externally. When loaded with 100 ohms the output level is -2.9 volts, fall time is 0.09 microseconds, and rise time is 0.03 microseconds. A compensating circuit for voltage drift is included which maintains the delay width constant within less than 0.3 per cent for a 10 per cent variation in any supply voltage. Jitter is below 0.1 per cent.

LK/md

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2. The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19 (122)-458.

TABLE OF CONTENTS

INTRODUCTION:

This variable delay unit supplies a negative level of variable duration when supplied with a negative pulse at the input. Many desirable features are built into it and its reliability is expected to be quite high. This unit will supply a 100 ohm resistive load with a -2.9 volt level whose fall time is 0.09 microseconds and whose rise time is 0.03 microseconds. Jitter is kept down to less than 0.1 per cent. The output pulse width may be varied continuously over the entire range of 0.3 microseconds to 2.5 seconds with 5 coarse positions. Longer delays are easily obtained by adding capacitance externally at the terminals provided. The output pulse width is affected only slightly by supply voltage variations, e.g. for a 10 per cent change in any supply voltage, the width changes by less than 0.3 per cent.

DEVELOPMENT:

As a first attempt in solving the problem of designing a variable delay unit, a monostable multivibrator was investigated. The emitter coupled type was eliminated because of its undesirable output pulse level, i.e., the output swing is not from ground level to -3 volts. The collector coupled monostable multivibrator showed more promise. However, the following difficulties were encountered. Referring to Figure 1, note that the delay time is directly proportional to the product of R_1C.

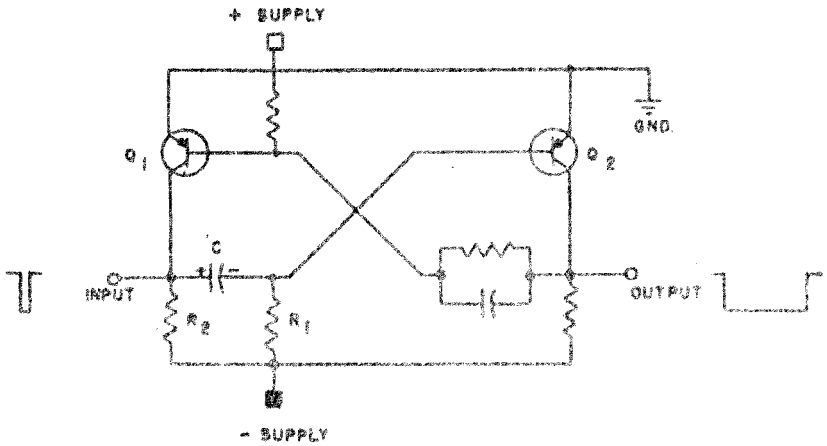


FIG. 1
MONOSTABLE MULTIVIBRATOR

However, the maximum value of R1 is limited because the d-c base current for transistor Q2 must flow through R1. If we desire a long delay time we will therefore find it necessary to increase the value of C. This brings us to a second difficulty, namely, that the recovery time (which is proportional to the product R_2C), becomes excessive. These problems were overcome by placing an emitter-follower between R2 and C as well as between R1 and the base of transistor Q2. This circuit however introduced too much delay time during the regeneration period (transition period) which resulted in a slower output waveform than could be acceptable.

It was decided that a monostable multivibrator which depends upon internal delay for its proper functioning would not be suitable, and so a circuit using external delay was investigated. As shown in Figure 2 the negative input pulse sets the flip-flop in the 0 state, and, after a time interval, a signal fed back from the RC timing circuit sets the flip-flop in the 1 state (by definition, the side which is set supplies a negative level).

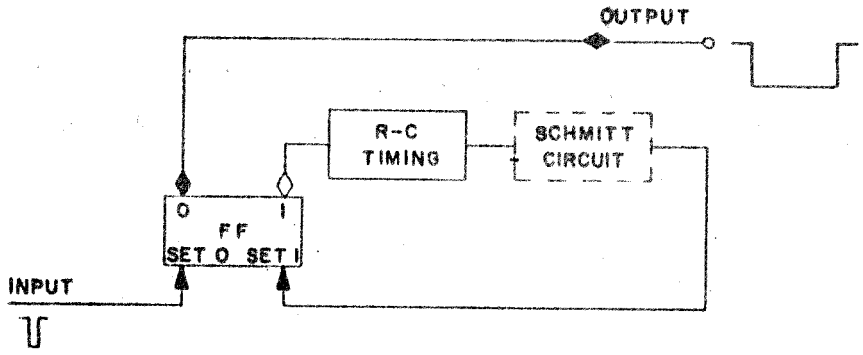


FIG. 2

FLIP-FLOP WITH EXTERNAL DELAY

The set one pulse coming from the timing circuit was too slow to give a suitable trailing edge to the output waveform, and so an emitter coupled bistable multivibrator, also known as a Schmitt circuit, was added, as shown dotted in Figure 2. This provided an extremely fast set one pulse. A Schmitt circuit responds only when the input signal exceeds a minimum amplitude, which is known as the triggering level. This triggering level is sensitive to supply voltage drifts, as is the timing circuit, and

therefore in an attempt to compensate for such drifts, both circuits were supplied from the same voltage sources. This greatly reduced the sensitivity of the delay width to supply voltage drifts. Basically this is the form of the final circuit. Further improvements are described below.

CIRCUITRY AND OPERATION:

A block diagram and a circuit schematic of the variable delay unit are shown in Figures 3 and 6, respectively. In brief, the operation of the circuit is as follows. A negative input pulse is applied to the input trigger stage. This triggers the flip-flop and sends the output from ground level to the -3v level. At the same time this initiates a timing circuit, which compensates for supply voltage drifts, and allows a time interval to pass during which the output is held at the -3v level. At the end of this time interval the Schmitt circuit is triggered which in turn triggers the flip-flop. The flip-flop then goes through a second transition returning the output to the ground level. The width of this output pulse is thereby determined by the setting of R and C only.

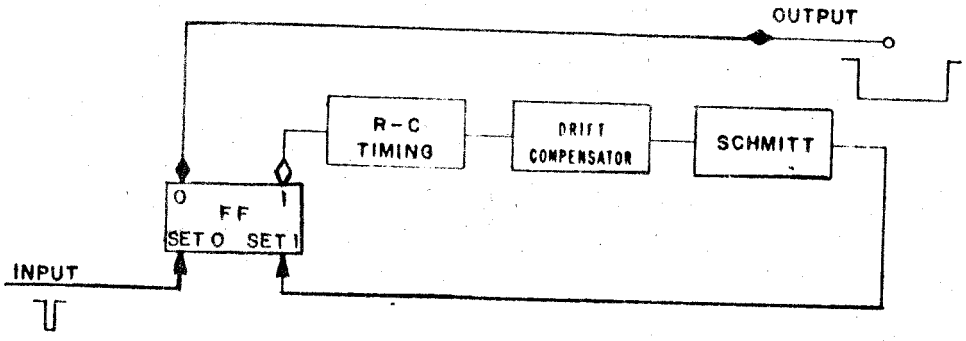


FIG. 3

BLOCK DIAGRAM, VARIABLE DELAY UNIT

In detail, the circuit operation may be described as follows. In the quiescent condition, assume that the flip-flop is in the 1 state (this is verified further on), setting the output at ground potential. When a negative pulse arrives at the input terminal, the collector of Q1 and of Q3 are both pulled toward ground, from -3 volts. This starts the transition of the flip-flop which results in the collector of Q3 remaining

at ground potential and the collector of Q_4, as well as the output terminal shifting to the -3 level. The output pulse has now started.

The base of Q6 is now pulled to ground which cuts off this transistor. The voltage across C up until this time had been 0 volts due to the clamping action of Q6. Now that Q6 has been cut off the potential at its collector begins to rise from -3 volts toward + 10 volts. The rate of rise is inversely proportional to the product RC. The emitter-follower, Q7, follows directly with the rising voltage at its base. Q6 and Q7 comprise the timing circuit.

The signal is now fed into a drift compensating circuit which functions as follows. The assumption is made that transistor Q8 does not conduct until its emitter potential equals or exceeds the potential of its base, at which time Q8 with its associated load resistor act as a standard inverter type circuit. In Figure 4 is shown a plot of the voltage at the emitter of Q8 versus time.

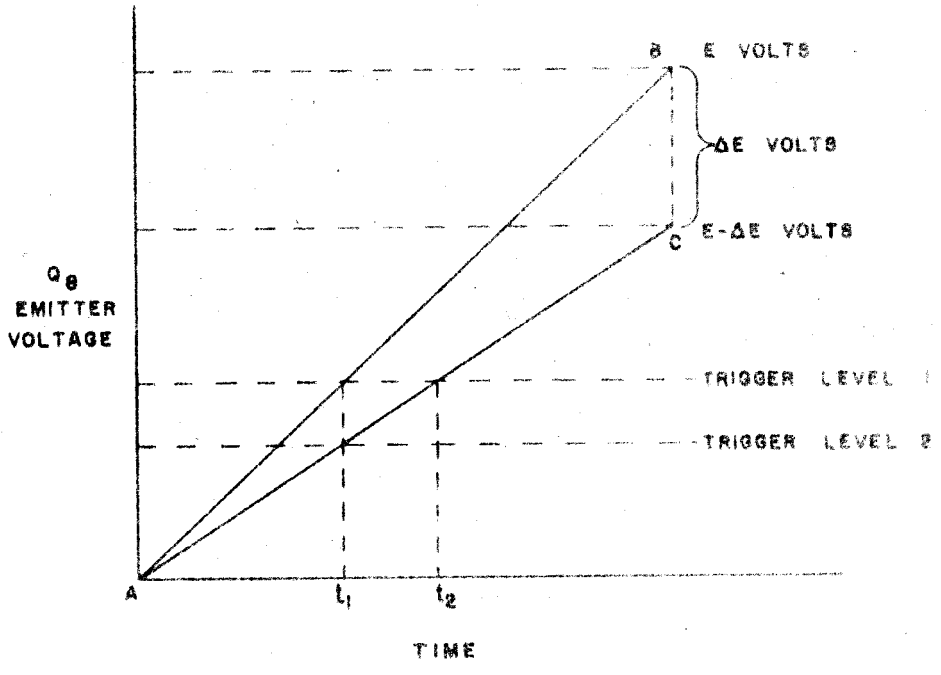


FIG 4

TRIGGER LEVEL ADJUSTMENT

Here the assumption is made that this waveshape is linear, whereas it is known that this is an exponentially rising waveform. This assumption is valid since we are dealing only with a small portion of this waveform at its beginning where it is nearly linear. In this Figure, E volts represent the absolute difference between the +10 and -3 supply voltages. Line AB represents the waveshape for a +10 supply voltage of value +10 volts. Assuming, for the moment, that the base voltage is fixed at a level which we shall call trigger level 1, it is seen that at time t1, the inverter will start to conduct. Assume now that the supply voltage drops by an amount delta E as shown in Figure 4 at point C. Line AC now represents the waveshape at the emitter of Q8. The intersection of this line and trigger level 1, occurs at a time t2 which is greater than the desired time t1. One way to compensate for this change in time is to change the trigger level from trigger level 1 to trigger level 2 which will then cause the intersection to occur at the desired time, t1. By similar triangles it is seen that,

$$\frac{\text{trigger level 2}}{\text{trigger level 1}} = \frac{E - \Delta E}{E}$$

Therefore,

$$\text{trigger level 2} = \left[\frac{E - \Delta E}{E}\right] \text{ trigger level 1}$$

This gives us the value of the new desired trigger level. One obvious way to set this new trigger level is to put the base of Q8 at this new level. This may be accomplished automatically by connecting Q8 as shown in Figure 5. From our original assumption we have defined the base voltage to be the trigger level. For the condition where the +10 supply voltage is equal to +10 volts, the trigger level is equal to

$$\text{trigger level 1} = \left[\frac{R1}{R1 + R2}\right] E.$$

If now the supply voltage changes by a quantity - ΔE the new trigger level will be

$$\text{trigger level 2} = \frac{R1}{R1 + R2}\left[E - \Delta E.\right]$$

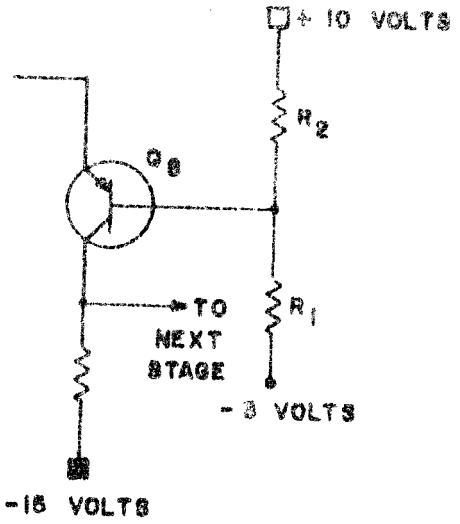


FIG. 5

DRIFT COMPENSATION FOR $+10_V$ AND -3_V SUPPLIES

Combining these two equations, we see that

$$\text{trigger level 2} = \left[\frac{E - \Delta E}{E}\right] \text{trigger level 1}$$

By comparing this trigger level 2 to the desired trigger level 2 as determined from Figure 4, we see that they are identical, and have thereby compensated for the change in the +10 supply voltage. By superposition, a change in the -3 volt supply will be compensated for in the identical manner. Note that the values of R1 and R2 do not enter into the final equations, and may therefore drift without consequence. They have been chosen to fall within the operating range of Q8.

The collector of Q8 will start rising at a time determined only by the setting of R and C and not dependent upon the supply voltage level. The inverting action through Q8 also has associated with it a large gain which effectively amplifies the slope of the waveform at its emitter. This signal is then raised roughly 3 1/2 volts through the Zener diode and appears at the base of Q9 which is the input to the Schmitt circuit.

The base voltage of Q9 is held clamped at a potential determined by the constants of the Schmitt circuit, the Zener diode, and the 5.6 K resistor. Therefore the collector of Q8 is clamped at a potential

roughly 3.5 volts negative of this. When the collector of Q8 begins to rise, the base of Q9 rises with it at higher level. The Schmitt circuit is set to trigger at a voltage roughly 1 volt positive of its clamped voltage. When the Schmitt circuit triggers, the collector of Q10 sharply rises from about -1.8 volts to a level slightly above ground, which cuts off Q2. This triggers the flip-flop and forces a transition to take place. The output at Q5 now swings from its -3v level to the ground level which thereby terminates the output pulse. The recovery time has been minimized by allowing C to recharge through the collector current of Q6.

Variations in the -15v supply alter the delay time by affecting the quiescent base voltage of Q9. However, by adding the 12K resistor from this supply to the base of Q8, a correcting signal is generated which compensates for such drifts.

The assumption made in the second paragraph of this section may now be verified. If the flip-flop were to remain in the 0 state, the timing circuit would begin functioning (since Q6 would be cut off), and this would be fed through to the Schmitt circuit, which would eventually trigger. Once triggered, the collector of Q10 jumps above ground potential, and this is fed to the base of Q2 which must therefore stop conducting. If Q2 is not conducting, the flip-flop must switch to its 1 state, Q.E.D.

PERFORMANCE:

Figure 7 shows photographs of the waveforms at critical points in the circuit. The delay time was arbitrarily set at 10 microseconds. Note the linear rise in voltage at the base of Q7, and the amplified slope of this rise at the input to the Schmitt circuit. Note also that the quiescent level at which the output signal settles is a few tenths of a volt above ground. This allows direct coupling to a transistor base, without adding positive bias. It may also be seen that the 100 ohm load hardly alters the output swing.

Figure 8 shows the variation in output pulse width as a function of the supply voltages, for a pulse width of 100 microseconds. Note that for a $\pm$ 10 per cent change in supply voltage, the pulse width remains constant within $\pm$ 0.3 per cent.

As is the practice with such circuits a number of margin check plots were made which proved quite satisfactory, giving wide margins for variations in the important parameters.

Further data in this respect may be found in Lincoln Laboratory Computation Book Number 1307.

SPECIFICATIONS AND RANGE:

1. Input: Requires a negative pulse whose minimum amplitude is -1.5 volts and whose duration should be at least 20 per cent less than that of the desired output pulse.
2. Output: (a) Minimum delay time: 0.3 microseconds,
   (b) Maximum delay time: 2.5 seconds.
   Note: Longer delays may be obtained by adding external capacitance at the terminals provided.
   (c) Fall time unloaded: 0.05 microseconds
   Rise time unloaded: 0.03 microseconds
   Fall time loaded with 100 ohms: 0.09 microseconds
   Rise time loaded with 100 ohms: 0.03 microseconds
   (d) Output swing, unloaded: -3 volts
   Output swing, loaded 100 ohms: - 2.9 volts.
3. Maximum pulse repetition frequency at minimum delay time: 3 megacycles
4. Jitter: 0.1 per cent
5. Supply voltages: +10, +10 MCV, -3, -15. Note: This circuit can also be changed for operation at -10 instead of -15 volts.
6. Semi-conductors required: 7 Philco type L-5122 transistors, 3 Philco type L-5134 transistors, 1 Texas Instrument type 65000 Zener diode.

7. Delay Range:

Delay Position	R	C	Delay Range	
Position 1	1K-100K	470 PF	0.3 μsec	- 7.5 μsec.
Position 2	"	.01 MF	1.7 μsec	- 140 μsec.
Position 3	"	.22 MF	25 μsec	- 2.5 ms.
Position 4	"	6 MF	0.65 ms.	- 90 ms.
Position 5	"	180 MF	19 ms.	- 2.5 sec.

Note: When adding external capacitance to obtain longer delays, put a 47 ohm resistor in series with the capacitor to limit excessive currents.

8. Polarity of Output Signal: The circuit described in this note gives an output that is quiescently at ground potential, and then drops to -3 volts for the duration of the pulse. If desired, an output may be obtained which normally supplies a -3v level, and rises to ground potential for the duration of the pulse. This may be accomplished by feeding the output into a clamped inverter (for low power applications) or into an inverter-cascode combination (for higher power applications) as is used in the TX-2 computer circuits.

Attachments:

Figure 6, Dwg. No. B-83082
Figure 7, Dwg. A-83295
Figure 8, Dwg. A-83265

A-83295

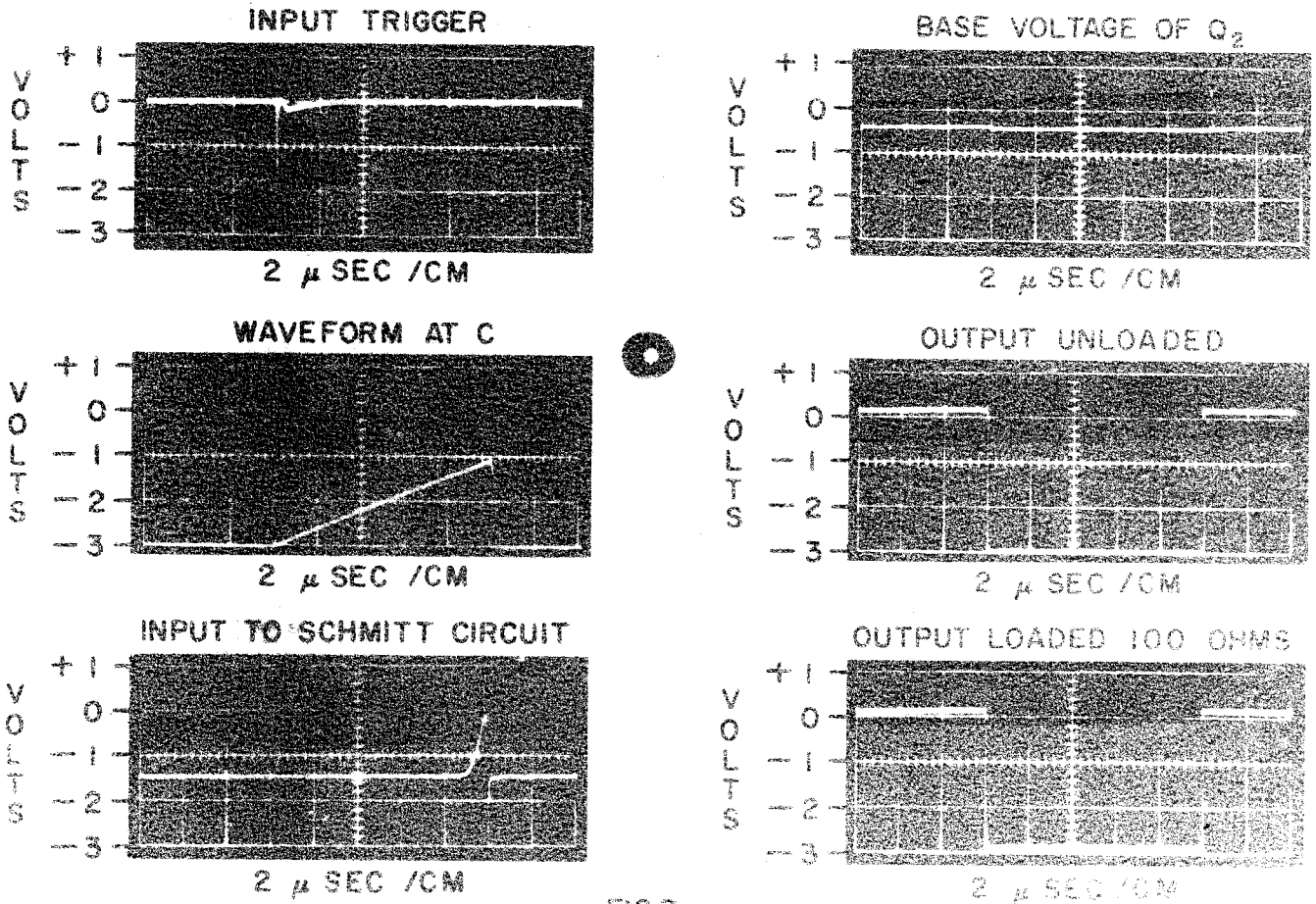
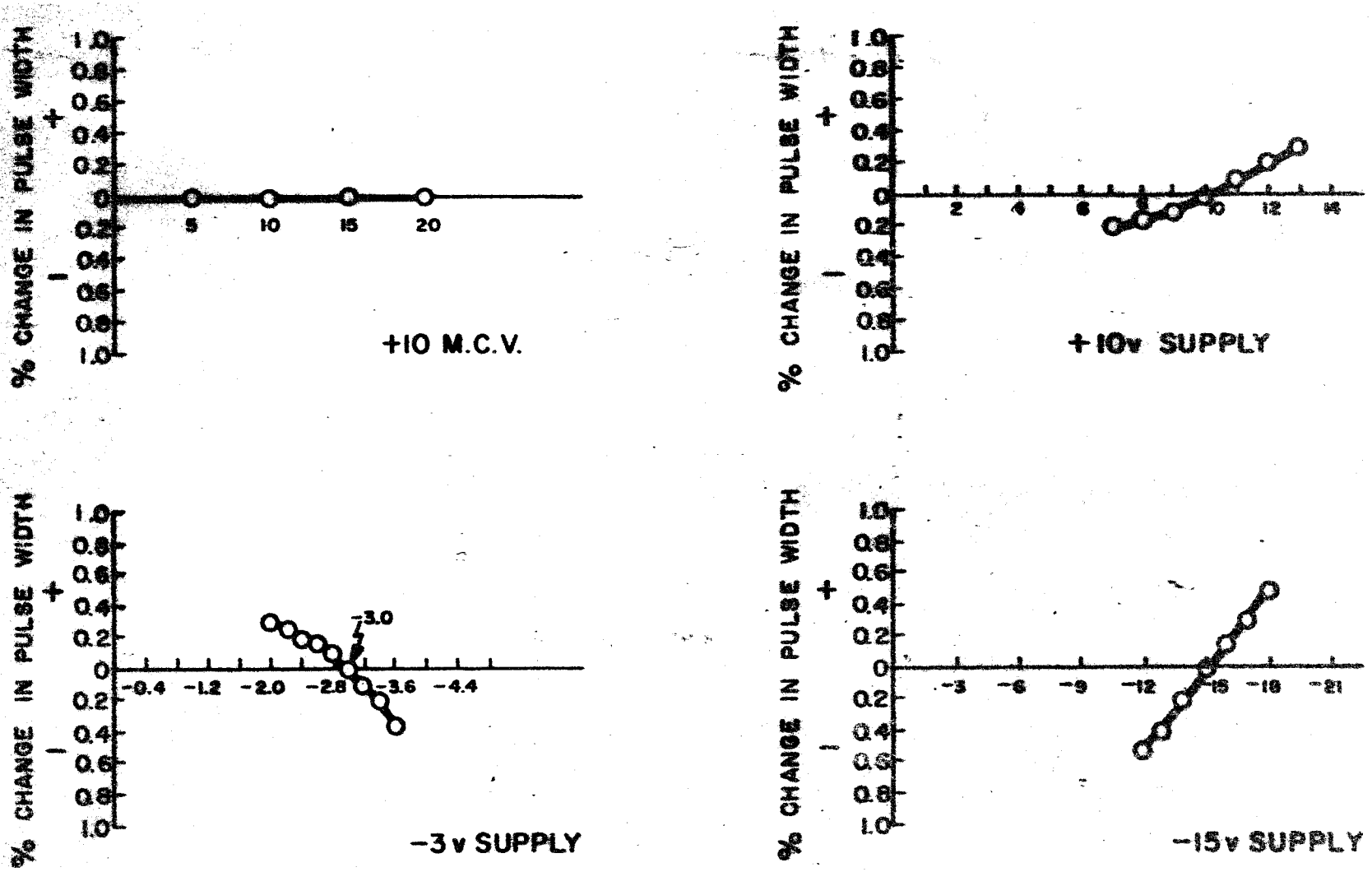


FIG. 7

VOLTAGE WAVEFORMS FOR 10 μSEC PULSE WIDTH



NOTE:
NOMINAL PULSE WIDTH SET AT 100 μ SEC.

FIG. 8

OUTPUT PULSE WIDTH AS A FUNCTION OF SUPPLY VOLTAGES

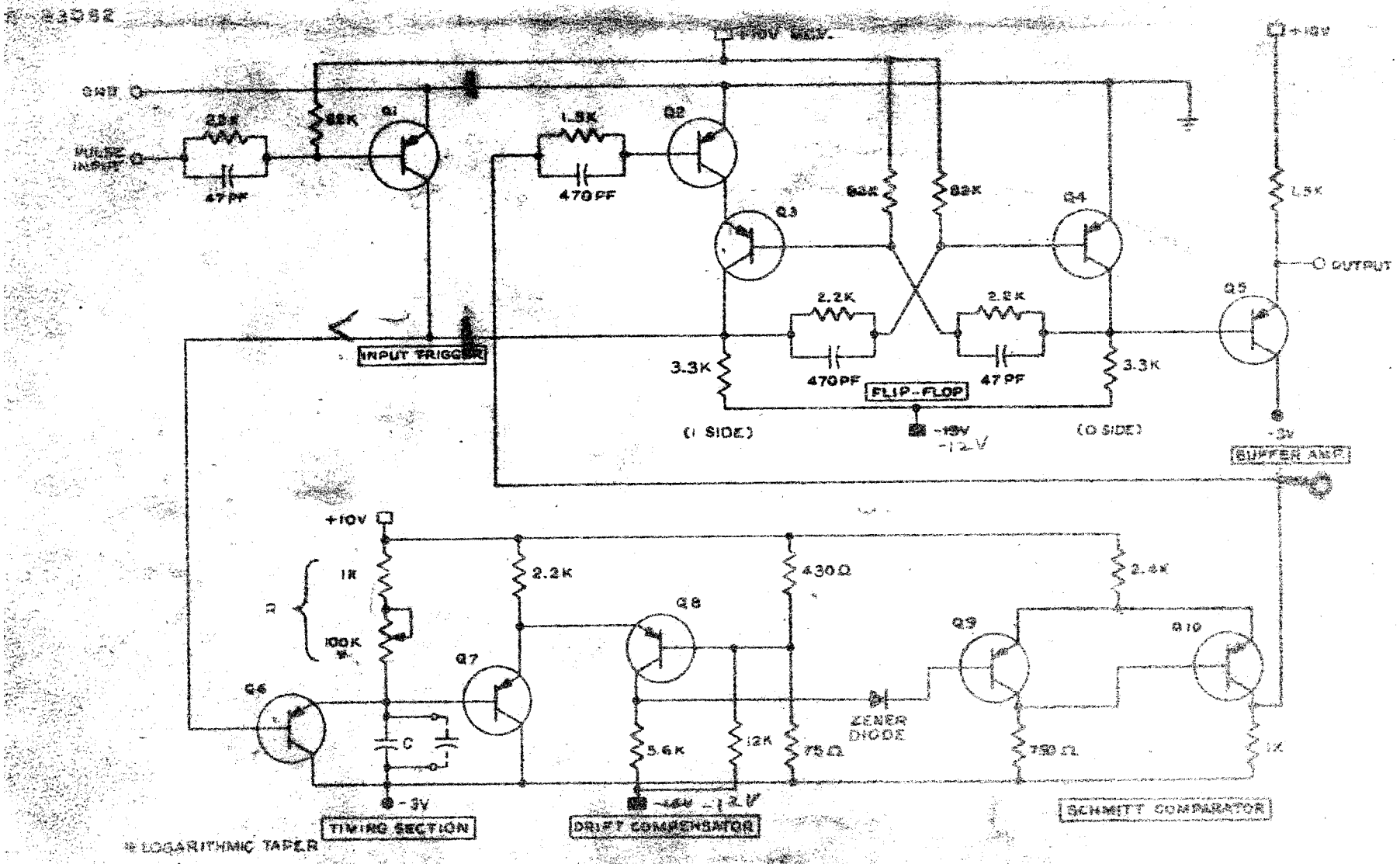
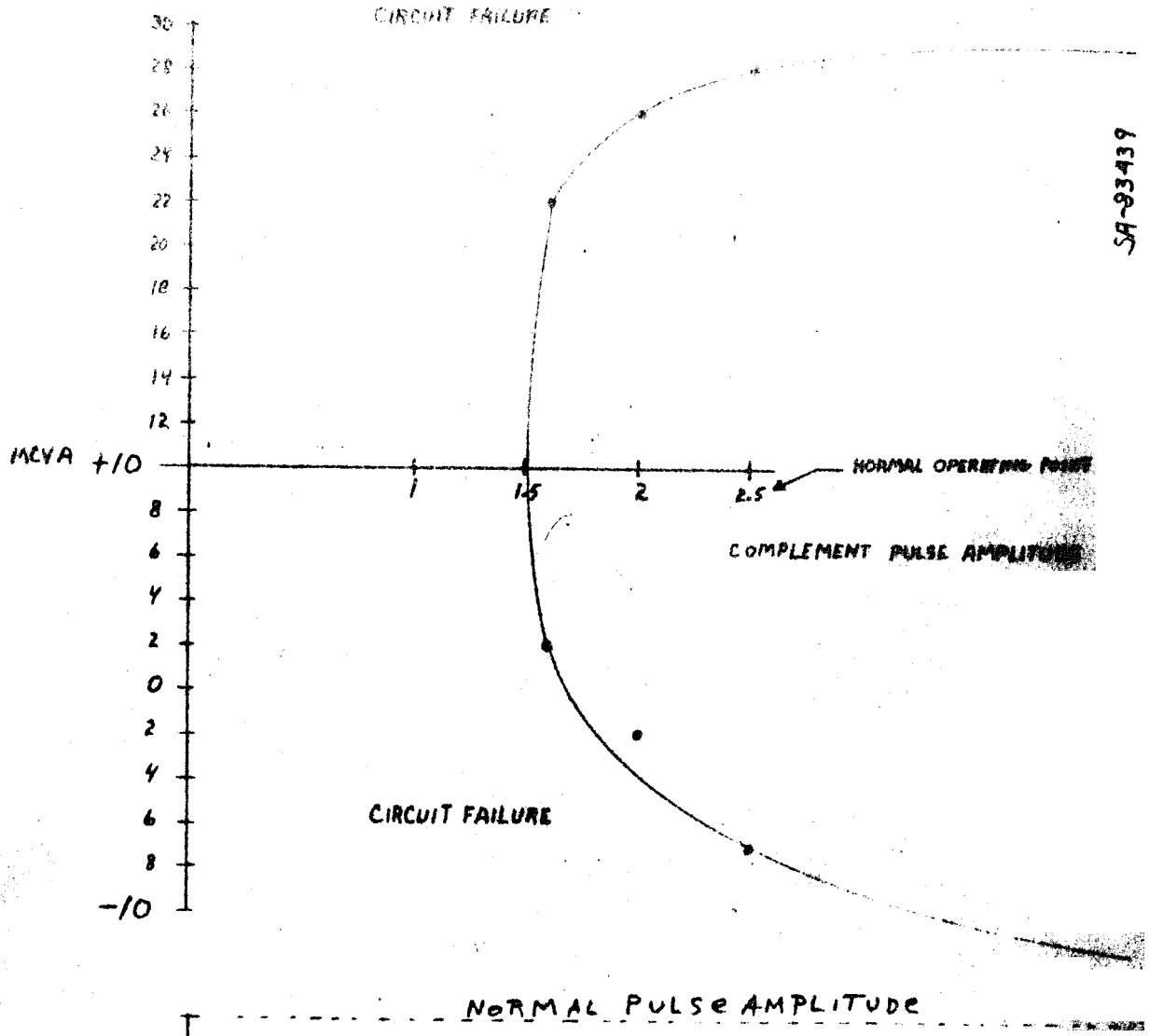


Fig. 6

SCHEMATIC CIRCUIT, VARIABLE DELAY UNIT

2N34

FIG 3A



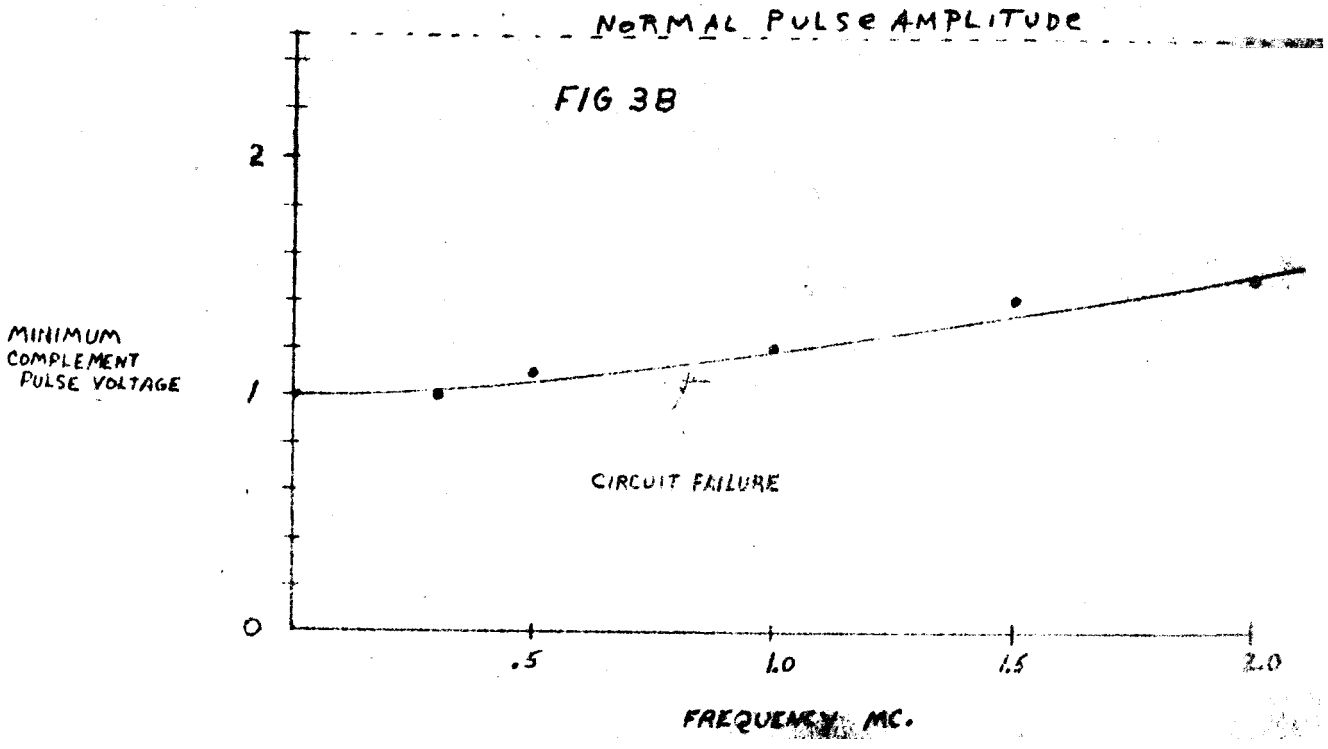


FIG 3B

SA-93439

Division 6 — Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: **A TRANSISTORIZED VARIABLE DELAY UNIT**

To: Group 63 Staff

From: Jonathan R. Fadiman Jonathan R. Fadiman

Date: January 20, 1958

Approved: BMG

Abstract: The variable delay unit described in 6M-3216 has been slightly modified for use in the TX-2 computer. Key points in the circuit are brought out to pins on the plug. The unit may be used in various ways according to the pin connections made on the plug. The proper delay range is also chosen by external pin connections. The maximum output current is 15 ma. at -3 volts, and 6 ma. at ground. The delay unit synchronizer, the delay unit auxiliary, and the variable delay coupling unit are described.

JRF:mt

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2. The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No AF 19 (122)-458.

The basic variable delay circuit has been slightly modified and adapted for use in the TX-2 computer. The -15 volt supply voltage has been changed to -10 volts, and much greater flexibility for use in TX-2 has been achieved by bringing out certain key points in the circuit to pins on the plug. There have also been some changes in circuit values in order to achieve more reliable operation. The circuit, as it is used in TX-2, is given in Figure 9. Figure 10 is a block schematic. The complete assembly and composite of the plug-in unit is given by D-84175.

For normal operation, pin J is connected to pin D, and pin N is connected to pin L. The proper capacitance is selected according to the delay range desired. The fine delay is adjusted by means of the trimpot which is a special wire-wound Bourns Trim-r made to have a minimum end resistance of only 100 ohms. The recovery time is constant for any given capacitance. The delays available and the proper in connections are given below.

Position	Pin Connection	Minimum Delay	Maximum Delay	Recovery Time
1	N-L	0.3 μsec.	6.0 μsec.	0.2 μsec.
2	N-L-F	1.7 μsec.	110 μsec.	0.5 μsec.
3	N-L-H	34 μsec.	2.4 millisec.	5.0 μsec.
4	N-L-M	1.0 millisec.	80 millisec.	130 μsec.
5	N-L-R	26 millisec.	2.2 seconds	8 millisec.

The delay as a function of capacitance is given approximately by $.14C < t < 12C$, where C is the capacitance in μfd and t is the length of delay in seconds. This holds only for $t > .5$ μseconds.

For longer delays than are available from the capacitances in the unit, added capacitance may be connected between pin L and the -3 volt supply. For example, a 4000 μfd condenser will provide a delay variable from 900 milliseconds to 54 seconds with a recovery time of 400 milliseconds. A 22 ohm resistor must be used in series with the capacitance to limit the charging current if C is greater than 10 μfd. Slight variations in delay in any one range will be noticed from unit

to unit, caused by the 20% capacitor tolerance. Sufficient overlap is provided to take care of this, but in general the capacitor should be chosen so as not to use the very end of any one range.

For synchronized operation, pin J is not connected to pin D. Instead, a gating circuit built from a P-5 unit is inserted as shown in Figure 11. The output of the Schmidt circuit, obtained from pin J, swings from ground to -3 volts. However, the -3 volt level is supplied by a 820 ohm resistor to -3 volts, which makes it necessary to use two transistors in parallel in the P-5 unit. The output of the P-5 unit will be a positive pulse from -4 volts to ground, which will occur on the coincidence of a negative 2.5 volt synchronizing pulse and a ground level output from the Schmidt trigger of the delay unit. Thus during synchronized operation, the delay time will equal the length of the variable delay setting plus the time until the next synchronizing pulse comes along.

In order for the delay unit to be controlled from the output of a decoder, pin J is connected to pin D as usual and pin N is not connected to pin L. Instead the auxiliary delay unit (Figure 12) is inserted. Any or all of pins D, J, N, and T of the auxiliary unit are connected to pin L of the variable delay unit. The length of delay will be controlled by the settings of the variable resistors in the auxiliary unit, by the decoded inputs to the diodes of the auxiliary unit, and by the capacitance range chosen.

The input to the delay unit at pin B may be a negative 2.5 volt 0.1 μsec. pulse or a negative-going 3 volt level which is at least 20% shorter than the maximum desired delay time. The collectors of other gated pulse inputs may be connected at pin T as in the standard two transistor gate to the "one" or "zero" input of a flip-flop. A positive going level may be used to trigger the delay by forming a negative pulse from it and triggering at pin B. A circuit which will

accomplish this is included in the variable delay coupling unit, to be described below.

The output of the delay unit is normally at ground, and goes to -3 volts during the delay. The maximum output current is 15 ma. at -3 volts, and 6 ma. at ground. Thus the output will drive 10 inverter bases, or 10 emitter-follower bases, or any combination of these two not exceeding 15 ma. at -3 volts. The output may also be used to drive the emitter of a single pulsed transistor.

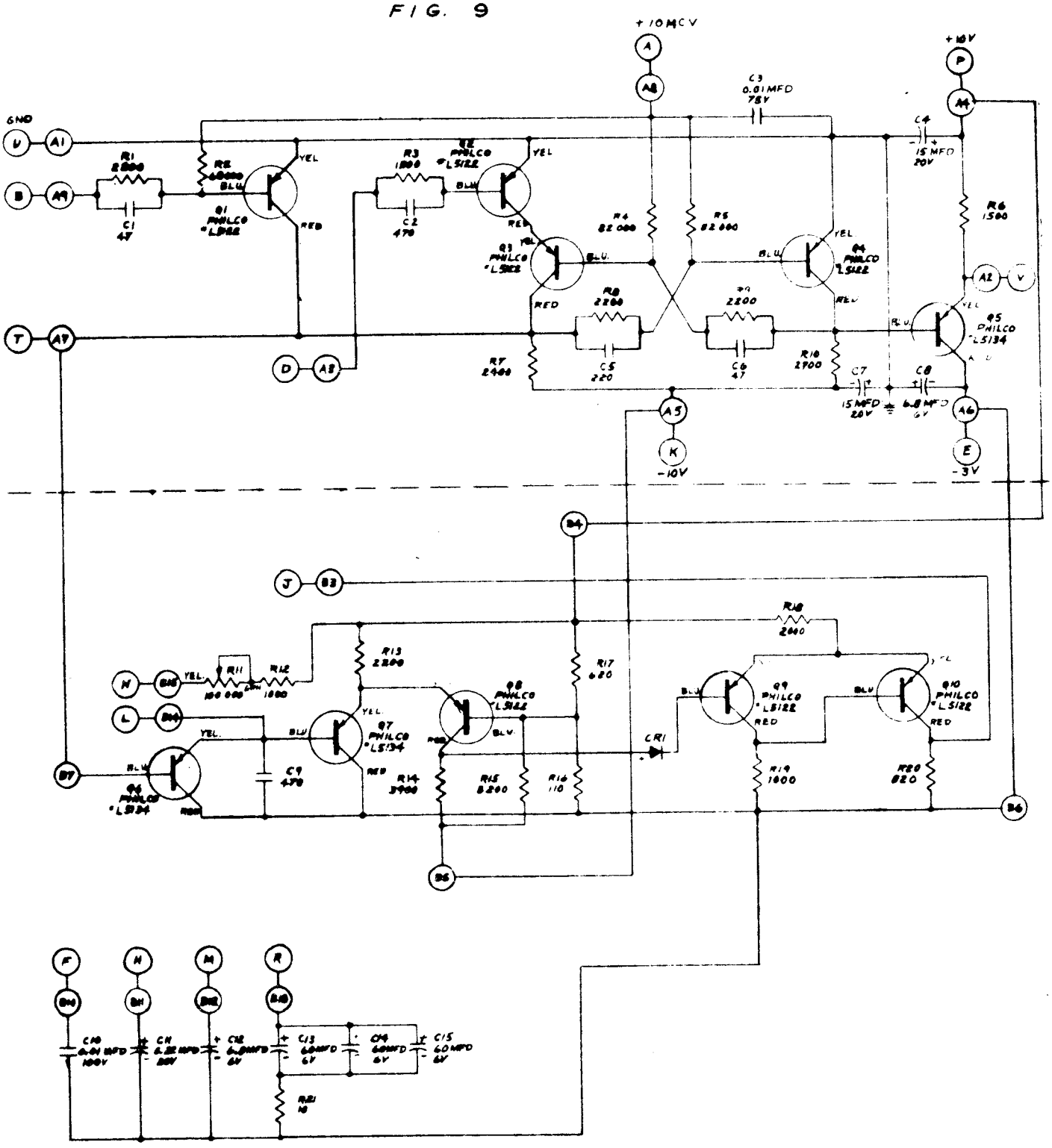
It may be desired to have a delay which will last for a given time after the last of a series of pulses. This can be done by using two variable delay units and the variable delay coupling unit. The circuit schematic of this unit is given in Figure 13. The output of VD_1 is connected to pin D of the coupling unit, and the output of VD_2 is connected in pin J. VD_2 is triggered from the negative pulse obtained from pin L of the coupling unit. Pin B of the coupling unit is connected to pin L of VD_2. The desired delay is obtained from pin V of the coupling unit. It is a level which is normally at -3 volts, and goes to ground for the length of the delay. The level goes to ground at the first pulse, and stays at ground for a length of time after the last pulse equal to the length of the first delay plus the length of the second delay. The maximum output current is 10 ma. at -3 volts, and 6 ma. at ground. In adjusting the length of the delays, VD_1 plus its recovery time must be less than VD_2. In addition, VD_1 must be greater than the recovery time of VD_2. The minimum resolution time of this circuit is equal to the length of VD_1 plus its recovery time.

Attachments:

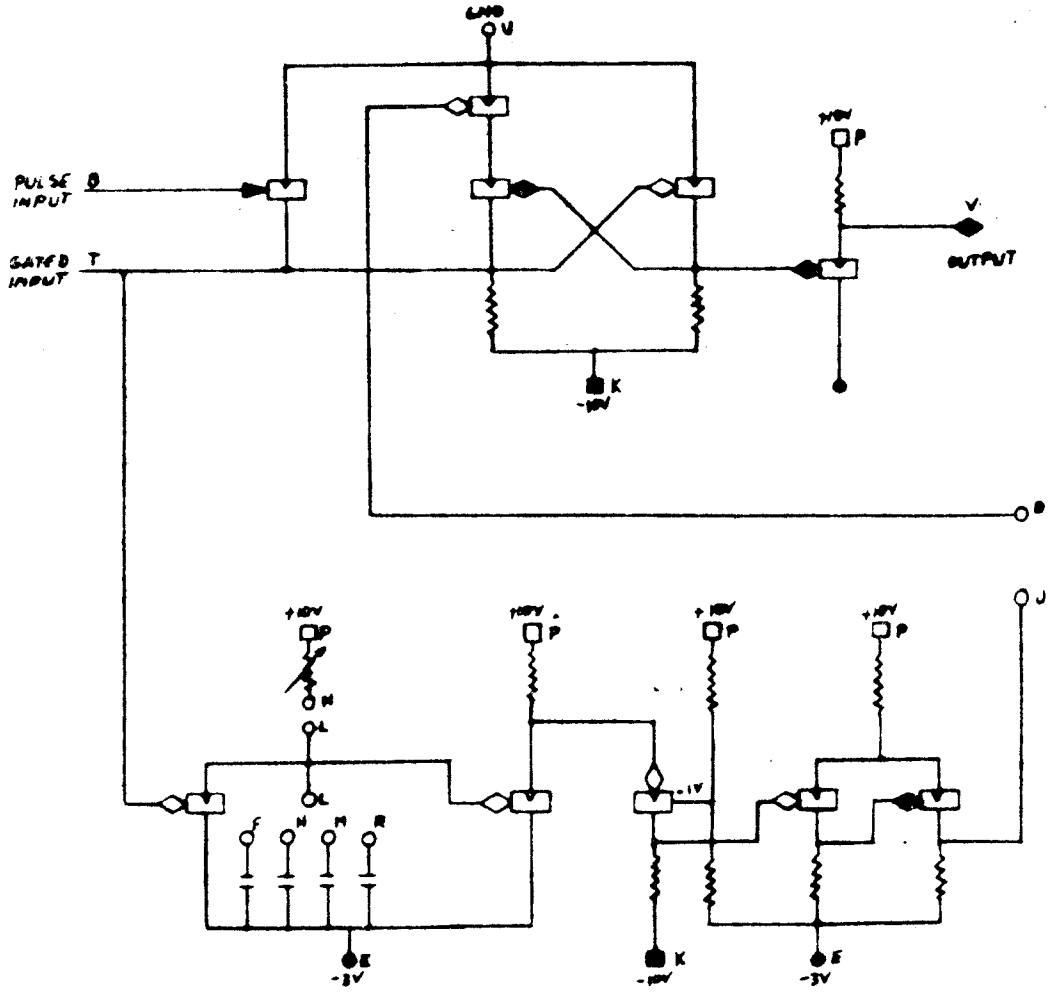
Figure 9, Dwg. No. SB-85602
Figure 10, Dwg. No. SA-85430
Figure 11, Dwg. No. SA-85603
Figure 12, Dwg. No. SA-85604
Figure 13, Dwg. No. SA-85605

SB-85602

CIRCUIT SCHEMATIC VARIABLE
DELAY UNIT
FIG. 9



SA-85430



Normal Operation

connect D-J and one of following

DELAY		CONNECT
.3 μsec	6.0 μsec	D-L
1.7 μsec	110 μsec	D-L-P
3½ μsec	2.4 millisec	D-L-E
1.0 millisec	80 millisec	D-L-M
26 millisec	2.2 seconds	D-L-R

For synchronized operation and externally controlled delay, consult 68-7216

-3V = Pin E
-10V = Pin K
+10V = Pin P
+10MC = Pin A
Gnd = Pin U

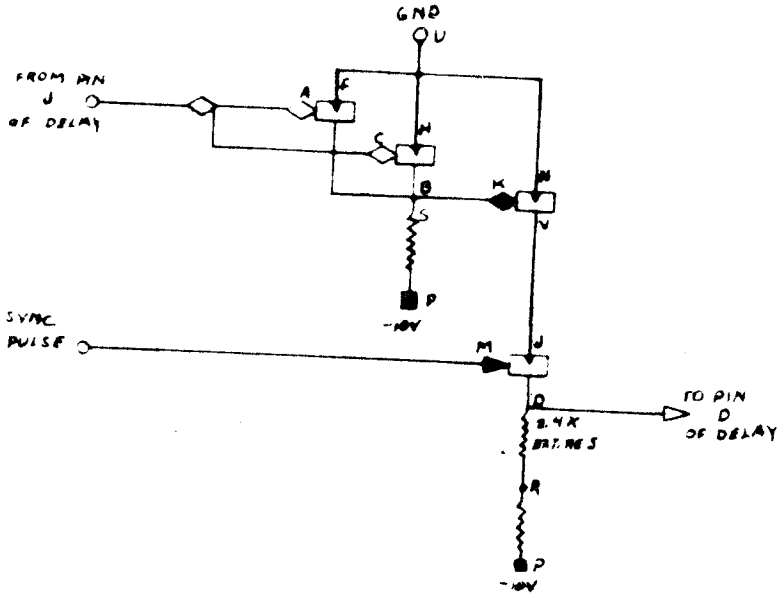
BLOCK SCHEMATIC,
VARIABLE DELAY
PLUG-IN UNIT, TX-2.

E. HARWOOD 12-30-57

Fig. 10

SA-85430

SA-85603



* NOTE: THIS UNIT USES A STANDARD P5 PLUS AN EXTERNAL 2.4K RESISTER BETWEEN PINS Q AND R.

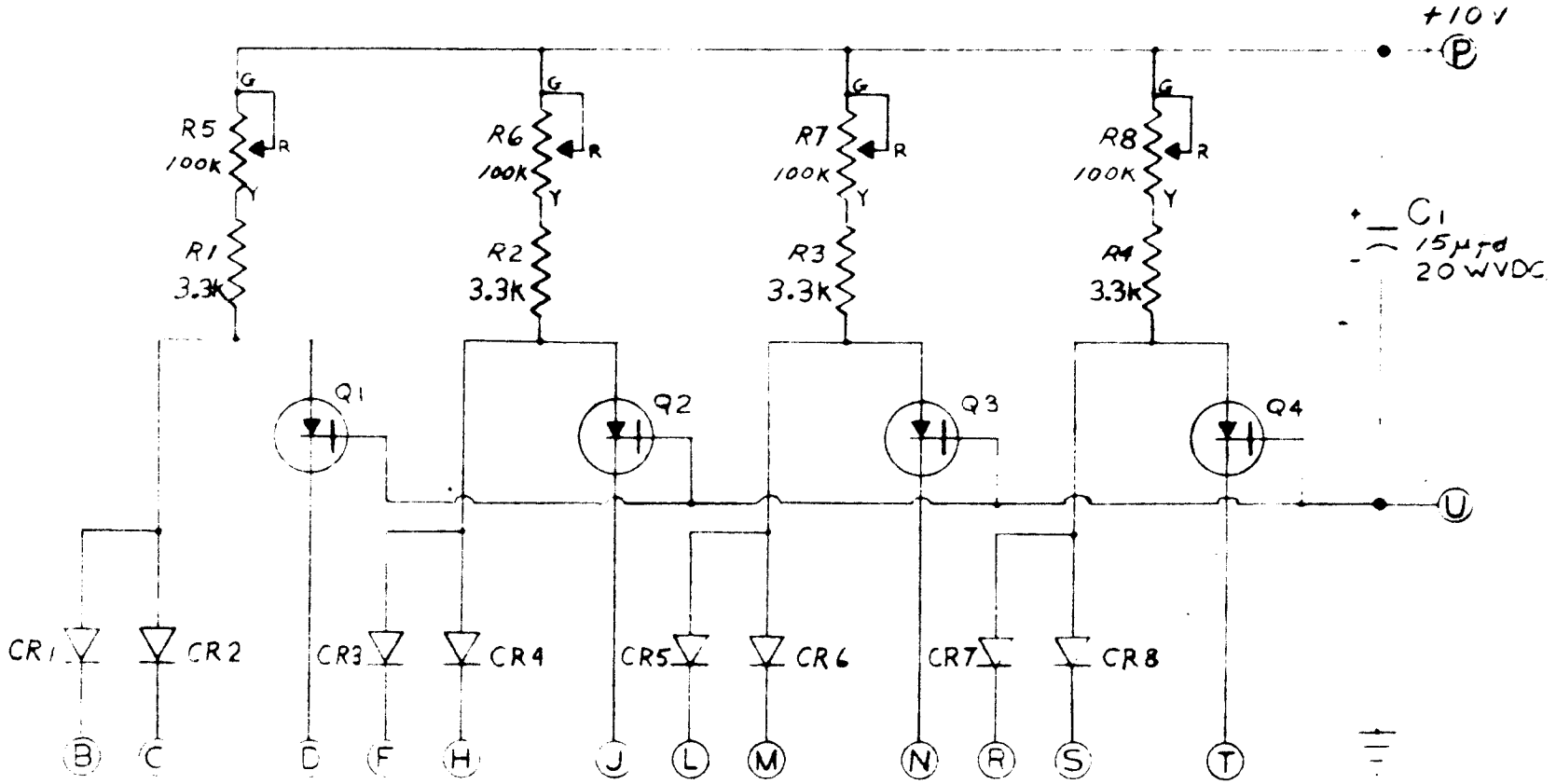
Fig. 11

BLOCK SCHEMATIC,
SYNCHRONIZER*
PLUG-IN UNIT, TX 2.
S HARWOOD 12-30-57

SA-85603

SA-85604

DELAY UNIT AUXILIARY



NOTE

Q1-Q4 are Philco L-5122
CR1-CR8 are Transitron SG-22
R1-R4 are ¼ watt ± 5%
R5-R8 are Bourns Trim-pot
C1 is Sprague Tantalex

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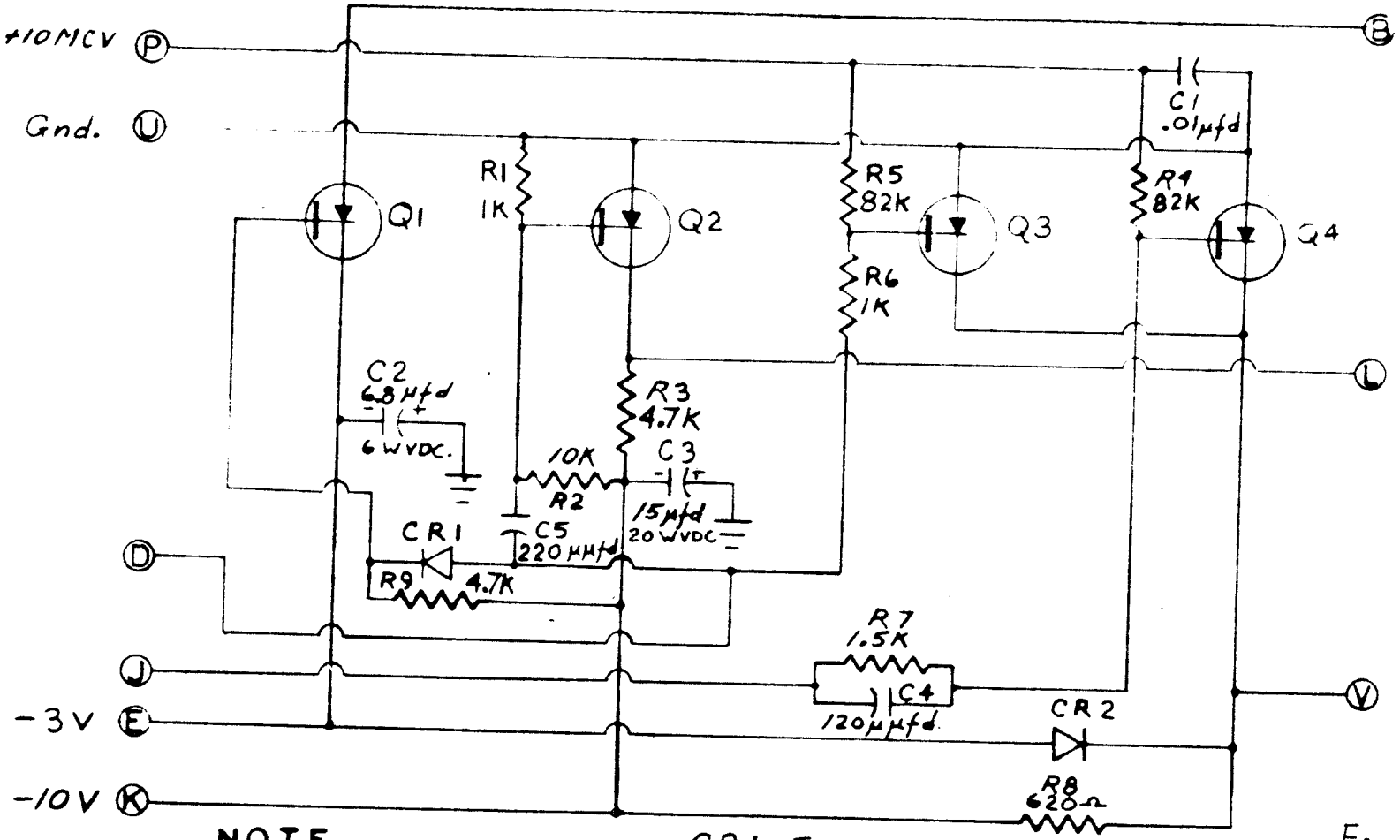
dr. 5-5
Fig. 12
SA-85604

SA-85605

VARIABLE DELAY COUPLING UNIT



NOTE

Q1, Q3, Q4 are Philco L-5134
Q2 is Philco L-5122
R1-R8 are ½ watt ±5%

CR1 - Transitron 1N625
CR2 - Transitron 1N270
C1, C4, C5, are Glenco Capts.
C2, C3 are Sprague Tantalex

Fig. 13

J. Fadiman

dr. H.T.S.

SA-85605